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By

Name

Mark L. Green
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REQUEST FOR PROVISIONAL APPLICATION UNDER 37 C.F.R. § 1.53(b)(2)

BOX PROVISIONAL PATENT APPLICATION

Assistant Commissioner for Patents

Washington, DC 20231

Dear Sir:

This is a request for filing a Provisional application for patent under 37 CFR § 1.53(b)(2) entitled A SINGLE-CHIP CMOS DIRECT-CONVERSION TRANSCEIVER by the following inventor(s):

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1. ☒ Enclosed is the Provisional application for patent as follows: 11 pages of specification, and 16 sheets of drawings.
2. ☐ A Verified Statement that this filing is by a small entity (37 CFR 1.9, 1.27, 1.28) is attached.
3. ☒ Payment of Provisional filing fee under 37 C.F.R. § 1.16(k) :
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5. ☐ Enclosed is an Assignment of the invention to _____, Recordation Form Cover Sheet and a check for \$ _____ to cover the Recordation Fee.
6. ☐ Also Enclosed:
7. ☐ The invention was made by the following agency of the United States Government or under a contract with the following agency of the United States Government:
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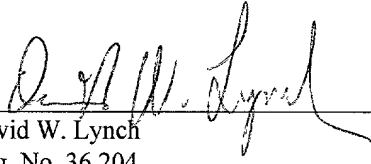
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Respectfully submitted,

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A SINGLE-CHIP CMOS DIRECT-CONVERSION TRANSCEIVER

BACKGROUND OF THE INVENTION

1. Field of the Invention.

This invention relates in general to communication systems, and more
5 particularly to a single-chip CMOS direct-conversion transceiver.

2. Description of Related Art.

Today's wireless communications markets are being driven by a multitude of
user benefits. Products such as cellular phones, cordless phones, pagers, and the like
have freed corporate and individual users from their desks and homes and are driving
10 the demand for additional equipment and systems to increase their utility. As a result
digital radio personal communications devices will play an increasingly important role
in the overall communications infrastructure in the next decade.

Mixed-signal integration and power management have taken on added
importance now that analog and mixed analog-digital ICs have become the fastest-
15 growing segment of the semiconductor industry. Integration strategies for multimedia
consoles, cellular telephones and battery-powered portables are being developed, as
well as applications for less integrated but highly specialized building blocks that serve
multiple markets. These building blocks include data converters, amplifiers and voltage
regulators. Makers of amplifiers and regulators often eschew integration in CMOS, but
20 strive for compact size and reduced costs with microminiature packaging.

One important aspect of digital radio personal communications devices is the
integration of the RF sections of transceivers. Compared to other types of integrated

circuits, the level of integration in the RF sections of transceivers is still relatively low. Considerations of power dissipation, form factor, and cost dictate that the RF/IF portions of these devices evolve to higher levels of integration than is true at present. Nevertheless, there are some key barriers to realizing these higher levels of integration.

5 A high level of integration is critical in lowering the cost of electronics for communication systems such as cellular phones, cordless phones, and wireless LANs. Increasing levels of transceiver integration are being reported, e.g., RF, baseband analog, and mixed-signal circuits have been integrated. Further, RF, baseband analog, and voltage-controlled oscillator (VCO) circuits have also been realized in a single die.

10 It can be seen that there is a need for a fully-integrated transceiver.

 It also can be seen that there is a need for a fully-integrated transceiver that incorporates RF circuits, synthesizer, baseband filters, demodulator, and extensive digital control functions.

SUMMARY OF THE INVENTION

15 To overcome the limitations in the prior art described above, and to overcome other limitations that will become apparent upon reading and understanding the present specification, the present invention discloses a single-chip CMOS direct-conversion transceiver.

BRIEF DESCRIPTION OF THE DRAWINGS

Referring now to the drawings in which like reference numbers represent corresponding parts throughout:

- Fig. 1 illustrates a block diagram of the single-chip CMOS transceiver
- 5 according to the present invention;
- Fig. 2 illustrates the low noise amplifier according to the present invention;
- Fig. 3 is a circuit diagram of the mixer and antialias filter according to the present invention;
- Fig. 4 illustrates a plot of the receiver bit error rate (BER);
- 10 Fig. 5 is a table illustrating the performance characteristics of the single-chip CMOS transceiver;
- Fig. 6 illustrates the transmit spectrum for 20 dBm output power;
- Fig. 7 illustrates the voltage controlled oscillator;
- Fig. 8 illustrates a block diagram of the synthesizer;
- 15 Fig. 9 is a phase noise plot for the single-chip CMOS transceiver;
- Fig. 10 is a plot of the unmodulated output spectrum for the single-chip CMOS transceiver;
- Fig. 11 illustrates the measured I/Q constellation for a -80dBm RF input;
- Fig. 12 illustrates a circuit diagram for the power amplifier;
- 20 Fig. 13 illustrates the die micrograph of the single-chip CMOS transceiver;
- Fig. 14 is the intermodulation (IM) plot for the entire receive path;
- Fig. 15 shows the measured step response of the channel filters; and
- Fig. 16 shows a change in the output levels of the channel filters in response to a change in the amplitude of a receive burst.

DETAILED DESCRIPTION OF THE INVENTION

In the following description of the exemplary embodiment, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration the specific embodiment in which the invention may be practiced. It is to be understood that other embodiments may be utilized as structural changes may be made without departing from the scope of the present invention.

The present invention provides a single-chip CMOS direct-conversion transceiver. As stated above, a high level of integration is critical in lowering the cost of electronics for communication systems such as cellular phones, cordless phones, and wireless LANs. The present invention provides a fully-integrated transceiver, shown in Fig. 1, that incorporates RF circuits, synthesizer, baseband filters, demodulator, and digital signal processing. The few off-chip components include an ISM band filter, a balun, an RF matching network, an RC loop filter for the PLL, a crystal resonator, and a resistor for biasing. The use of a transmit/receive (T/R) switch is avoided by sharing a single RF port between the transmitter and the receiver. An offset cancellation method attenuates offsets in the baseband without sacrificing bandwidth in the direct conversion receiver. Careful circuit, timing, and layout considerations provide isolation between the sensitive RF signal and the digital switching noise. The IC has been fabricated in 0.6- μ m CMOS and provides a complete interface between an antenna and a voiceband codec.

Architectural and circuit techniques have made it possible to achieve this level of integration without sacrificing performance. Time-division duplex (TDD) ensures isolation between the transmitter and the receiver. Direct conversion makes it possible to eliminate expensive, off-chip radio frequency (RF) image reject filters and diplexer,

and to replace off-chip intermediate frequency (IF) channel select filters with on-chip low pass filters.

Active on-chip offset reduction by means of feedback and feedforward loops has been combined with a digitally controlled automatic gain control (AGC) circuit that
5 settles within the 160- μ s preamble of the receive burst.

In a direct conversion receiver, static and varying DC offsets within the base band I and Q channel amplifiers and filters limit the architecture's usefulness. In the past, AC coupling or high pass filtering has been used to remove the DC offset from the
10 signal causing degradation to the signal. The present invention uses a combined feedback and feedforward offset cancellation technique with DC signal response to cancel the DC offset problem while at the same time providing for a DC response to the base band signals of interest.

The main feature of the feed forward offset cancellation architecture is its
15 capability to cancel low frequency (DC to 5 kHz) offsets caused by LO leakage and other non-ideal component induced offsets while at the same time maintaining a DC response to the signal. This is accomplished by two main components of the architecture.

The first main component is the signal format. A signal format was chosen such
20 that the I and Q base band signals exhibit a positive and negative peak within a certain time frame, 6.66 micro-seconds was chosen. The peaks and valleys of the I and Q signals from one time frame to the next are required to be approximately equal.

The second main component is a positive and negative peak detector which determines the peaks and valleys of the signal over a certain time frame (6.66 μ s). The
25 offset is then the addition of the positive and negative peaks divided by two.

A fully-differential analog signal path minimizes supply and substrate noise coupling. To further reduce coupling, transitions of digital signals have been minimized near the sampling edge of baseband switched-capacitor circuits. Source-coupled logic has been utilized in the PLL frequency dividers to reduce substrate noise injection,

5 while CMOS logic gates have been used in the burst-mode controller (BMC) to achieve low power dissipation and high circuit density. An automatic calibration technique has allowed the integration of a 1.8-GHz LC VCO with a wide tuning range. The receiver has a maximum gain of 106 dB and a sensitivity of -104 dBm.

The low noise amplifier (LNA) and the power amplifier (PA) designs make it

10 possible to share a common RF port, thereby eliminating the need for an external transmitter/receiver switch. The transmitter and receiver are attached to the filter/antenna port of a radio transceiver without the need for a costly antenna switch in a time division duplex system.

Radio transceivers usually require both a Low Noise Amplifier or (LNA) for

15 clear reception and a Power Amplifier or (PA) for transmitting over long distances. In a time division duplex or (TDD) transceiver, the transmitter and receiver are not utilized simultaneously. When the transmitter is on the receiver is off and when the receiver is on the transmitter is off. For a typical TDD transceiver, the receive LNA is powered down during the transmit cycle to conserve power and the transmit power amplifier is

20 powered down while the receiver is on.

In the past the LNAs and PAs have been designed utilizing bi-polar transistor technology. The bi-polar LNAs and PA's are capable of powering down, however their respective input and output impedance while in the powered down state do not allow them to be connected together in a TDD system. The powered down LNA will

25 attenuate the output power of the PA and may even be damaged by the PA. The

powered down PA will lower the impedance that the LNA “sees” and will attenuate the incoming signal from the antenna.

To get around the varying impedance problem, LNA and PA typically use their own set of different matching components to produce a 50 Ohm LNA input impedance and 50 Ohm PA output impedance. This topology is then combined with an antenna switch so that the off state impedances of either the LNA or the PA will not harm the 50 match achieved by the different matching components. However, the antenna switch can be costly, and the transmit and receive signals are still attenuated somewhat by the switch itself. In addition a control circuit must be used to switch the antenna switch.

According to the present invention, the antenna interface requires only one RF combined input/output port thereby reducing IC package pin count and number of external components. An impedance transformation network of 25 to 50 ohm network is used to ease the LNA requirement. A singly matched network is used for PA since putting required matching 50 ohm will limit the theoretical power efficiency to less than 50% and will degrade the power efficiency achieved in practice.

The LNA, shown in Fig. 2, is implemented as a cascade of two stages. The first stage employs a capacitively cross-coupled input pair, M1 and M2, that provides both gain and impedance matching in parallel with a differential pair, M3 and M4, for additional gain. The second stage of the LNA is also a differential pair. All gain stages are loaded by on-chip spiral inductors. The combined LNA gain can be set to 12 dB or 28 dB.

The PA is implemented as a three-stage, class AB amplifier. The first stage is a resistively loaded differential pair, the second stage is a common-source stage loaded with on-chip spiral inductors, and the output stage consists of large open drain devices whose drains are connected to the LNA input. The bias currents of the final stage are

provided by off-chip RF chokes. The output power, measured at the balun, can be varied from +2 dBm to +20 dBm. Refer to Fig. 12.

A diagram of the mixer and antialias filter is shown in Fig. 3. The mixer's conversion gain is 14.3 dB. The mixer uses a double balanced structure without a tail current source to increase headroom. Biasing for the RF input transistors is performed by a replica circuit that suppresses transconductance variations with process and temperature. The LO input transistors operate as switches that steer a process and temperature independent current. The output of the mixer is fed to a four-pole Butterworth antialias filter with a cut-off frequency of 2.4 MHz.

Two biquad stages form a four-pole Butterworth antialias filter with a nominal gain of 15.6 dB and a cut-off frequency of 2.4 MHz. Switched-capacitor I and Q baseband filters sample the output of the antialias filter at 24 MHz, attenuate adjacent channels, and provide AGC. Each baseband signal path comprises a fourth-order low pass Chebyshev filter, implemented with two biquad sections, followed by a group delay equalizer (GDE). The biquads and the GDE have a programmable gain of one or four. The filter is followed by a switched-capacitor variable gain amplifier (VGA) that is programmable with a gain of one, two, or four. This arrangement provides a baseband gain of 0 dB to 48 dB in 6 dB steps.

In a direct conversion receiver, LO leakage can lead to large offsets at the inputs to the baseband filters. Moreover, offsets in the switched-capacitor filter sections can accumulate and render the output signal undetectable. To overcome this problem, feedback integrators cancel offsets in the first biquad and in the GDE, as shown in Fig. 1. To prevent baseline wander from causing errors, the integrators are placed in a hold mode when data is transferred.

Switched-capacitor peak detector circuits sample the maximum and minimum values of the filtered I and Q signals. The AGC controller uses the peak detector outputs to estimate the signal levels and adjusts the baseband gain accordingly. the outputs of the peak detectors are also low pass filtered to estimate the residual offset in the outputs of the channel filters. The offset is then subtracted from the baseband filter output, and the resulting I and Q signals are fed to a BFSK demodulator.

The BFSK demodulator is implemented with switched-capacitor circuits clocked at 6 MHz. It generates a digital output based on the direction of rotation of the I/Q constellation. The digital output of the demodulator is processed by an on-chip BMC, comprising over 8000 CMOS standard cell gates, that performs clock recovery and direct sequence spreading and despreading. The receiver bit error rate (BER), shown in Fig. 4, illustrates the receiver sensitivity. Selectivity and blocking performance are given in the table in Fig. 5.

A single frequency synthesizer creates both LO and PA input signals for receive and transmit, respectively. The circuit generates channels from 900 MHz to 930 MHz in 750kHz increments. During receive, a divide-by-two circuit creates I and Q LO signals from the output of a VCO operating at twice the desired frequency in a high bandwidth PLL. During transmit, the PLL bandwidth is reduced allowing filtered transmit data to directly modulate the VCO while maintaining a constant center frequency. The transmit spectrum for 20 dBm output power is shown in Fig. 6. The VCO, shown in Fig. 7, is designed as a cross-coupled differential pair loaded by spiral inductors and by capacitors. The load capacitors include ac-coupled channel varactors, modulation varactors, and a bank of capacitors for automatic coarse frequency adjustment.

The synthesizer architecture is shown in Fig. 8. The varactors are on chip. The VCO operates at twice the carrier frequency in order to alleviate problems arising from PA pulling. Furthermore, it allows the robust creation of I and Q signals using a simple divide-by-two circuit. A phase noise plot is provided in Fig. 9, and the output spectrum is shown in Fig. 10.

The VCO is automatically calibrated in a closed loop with control circuitry that digitally adjusts the capacitive load of the tank. The measured I/Q constellation for a -80dBm RF input is shown in Fig. 11. The PA circuit is illustrated in Fig. 12. The power efficiency of the PA is 20% at +20 dBm.

The measured performance, summarized in the table of Fig. 5, demonstrates that a single-chip CMOS transceiver can successfully integrate the RF front end along with baseband analog circuits and a significant amount of standard cell digital circuits. Fig. 13 illustrates the die micrograph of the single-chip CMOS transceiver.

The intermodulation (IM) plot for the entire receive path is shown in Fig. 14. This plot was generated by applying two tones that are 6 channels away from the carrier and recording the power of the IM product at the output of the baseband filters. The tones were chosen such that the IM products are well within the bandwidth of the baseband filters. The measurements include the influence of on-chip test buffers on the receiver linearity. The input signal power was measured at the input to the chip, and the LNA gain was in its "high" settings. The 1-dB compression point is limited by the switched-capacitor circuits and occurs at approximately 5V differential amplitude.

All switched-capacitor stages in the baseband filters, peak detectors, and demodulator employ correlated double sampling (CDS) to attenuate their offsets and $1/f$ noise. To minimize offsets due to mismatch in sampling switches, NMOS rather than CMOS switches have been used. The four clock signals include two-phase, non-

overlapping and delayed phases that are driven by voltage doublers. Static charge pumps drive the gain selection switches in the baseband filters and VGA. Fig. 15 shows the measured step response of the channel filters. Fig. 16 shows a change in the output levels of the channel filters in response to a change in the amplitude of a receive burst.

5 The selectivity, as shown in the table of Fig. 5, was measured by applying a –83 dBm desired signal, then increasing the power of an interferer until the BER reached 10^{-3} . The difference between the power of the interferer and –83 dBm is the selectivity. This test was performed with the interferer within the desired channel as well as 1.5 MHz, 3 MHz, and 4.5 MHz from the carrier. When the interfering tone is 4.5 MHz
10 from the carrier, the receiver's BER is limited by the linearity of the front end. Hence, this measurement represents the blocking performance of the receiver.

 The foregoing description of the exemplary embodiment of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications
15 and variations are possible in light of the above teaching.

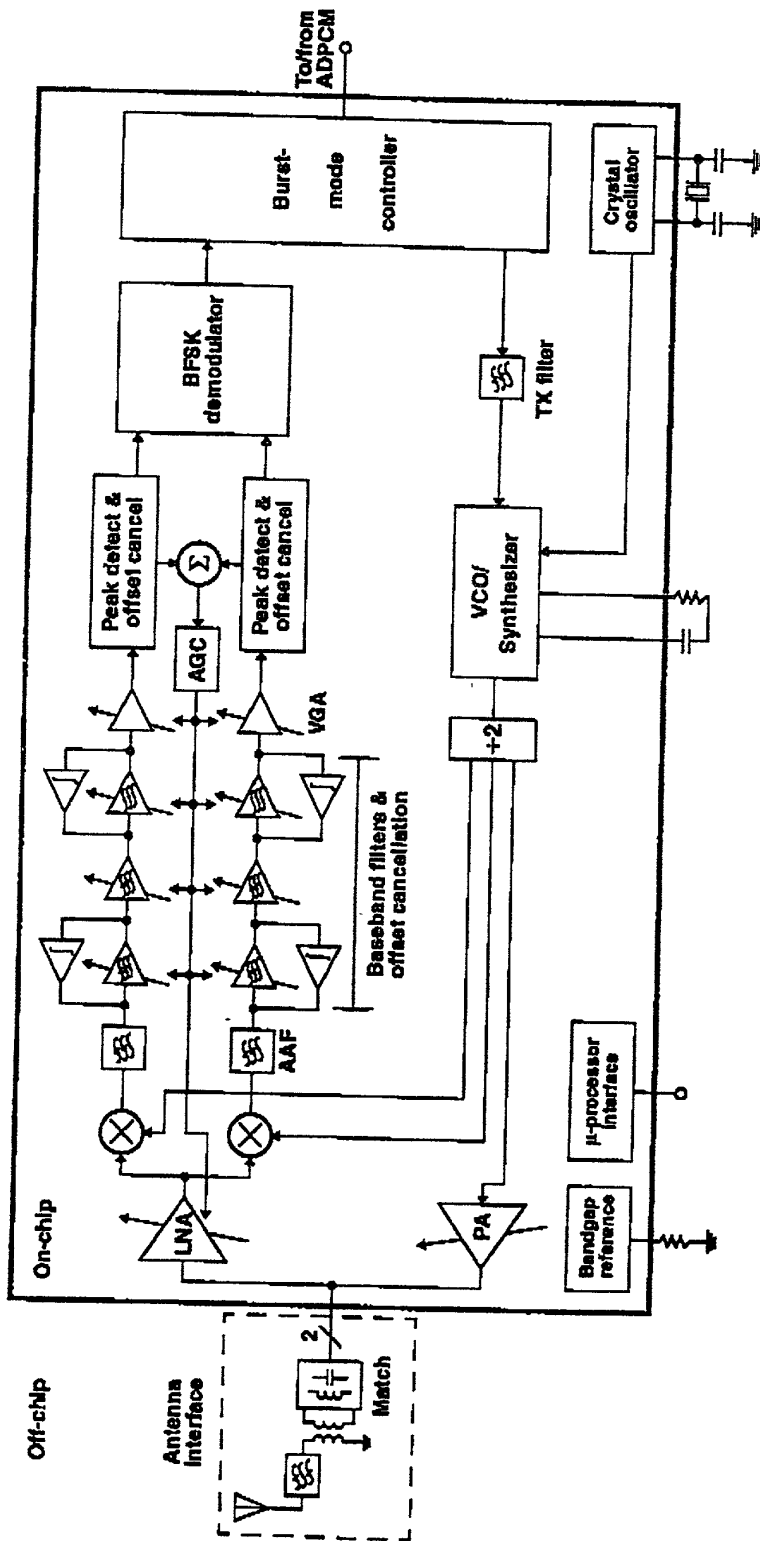
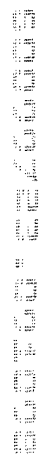
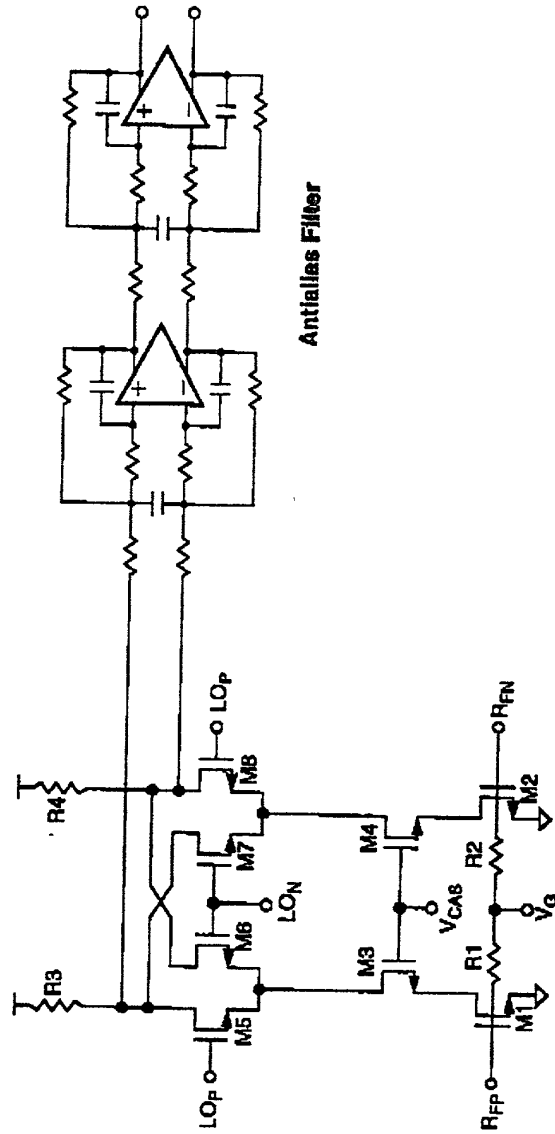


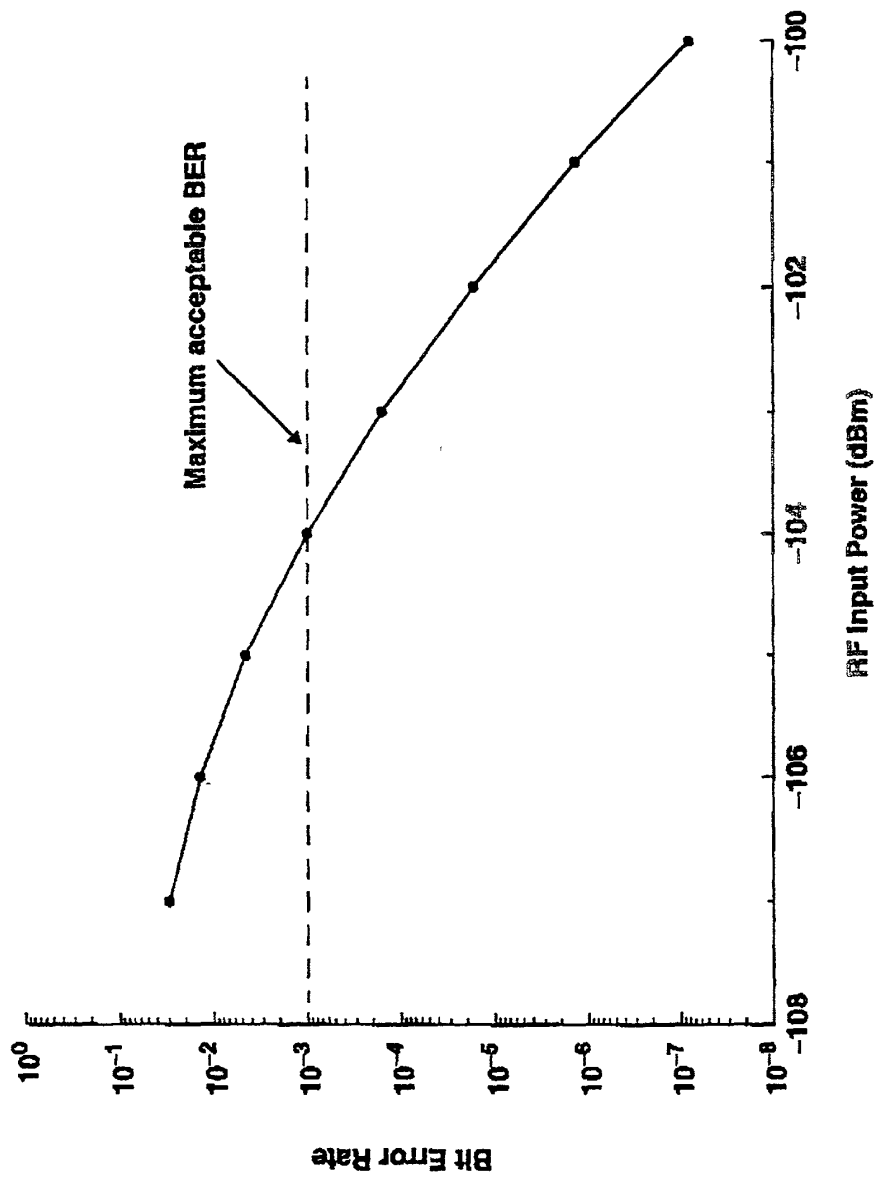
Fig. 1



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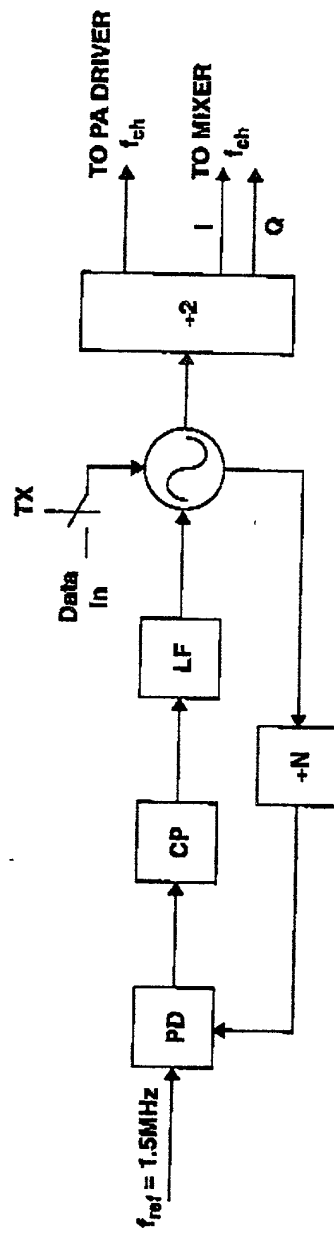
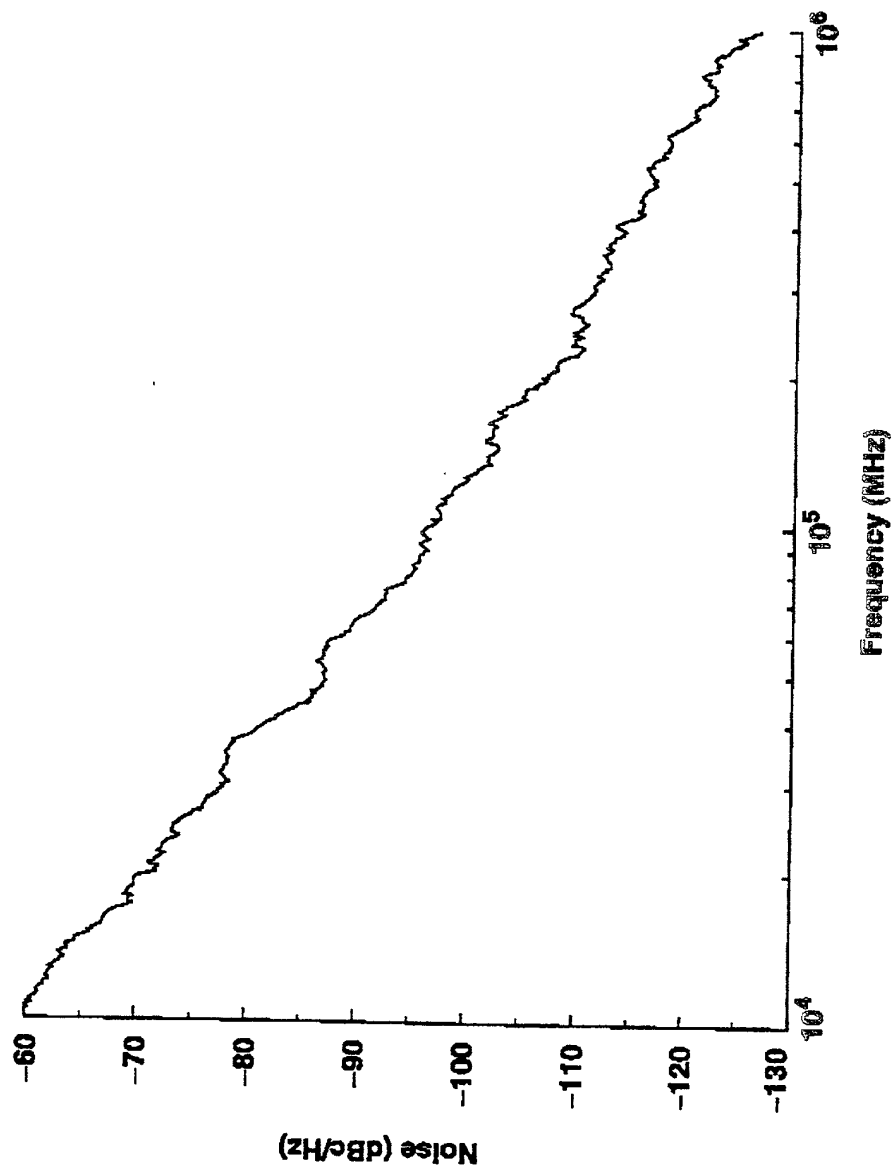


Fig. 8

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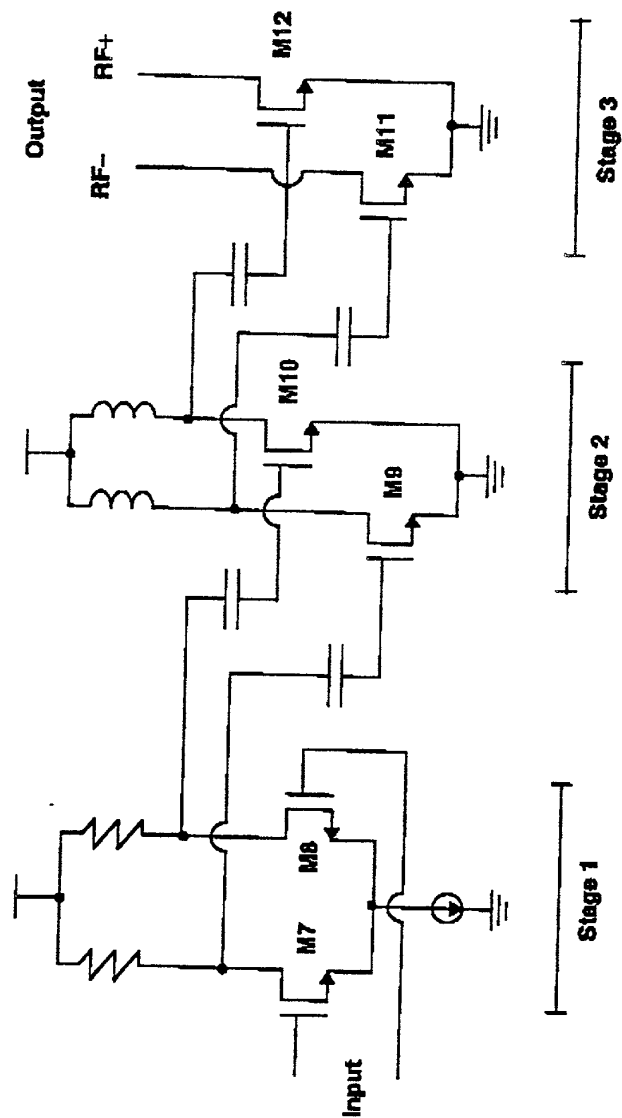


Fig. 12

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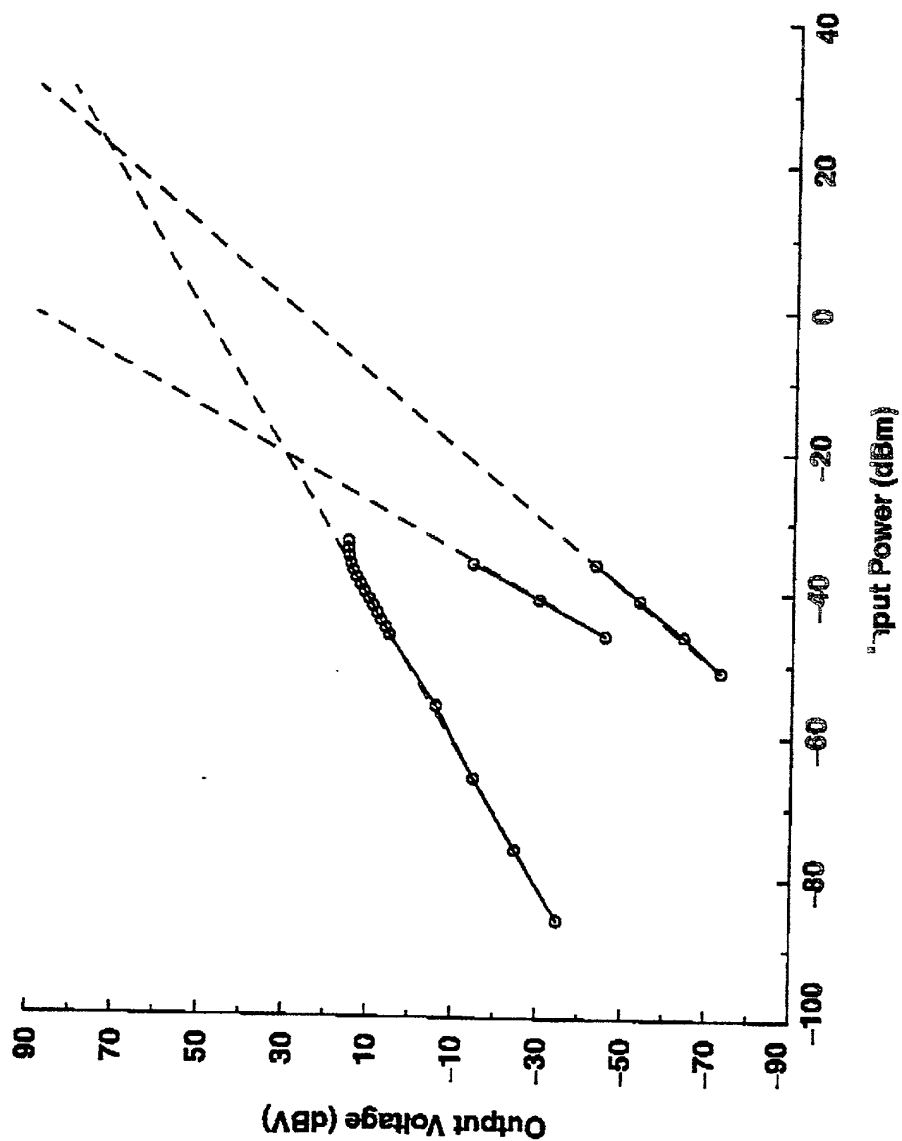


Fig. 14

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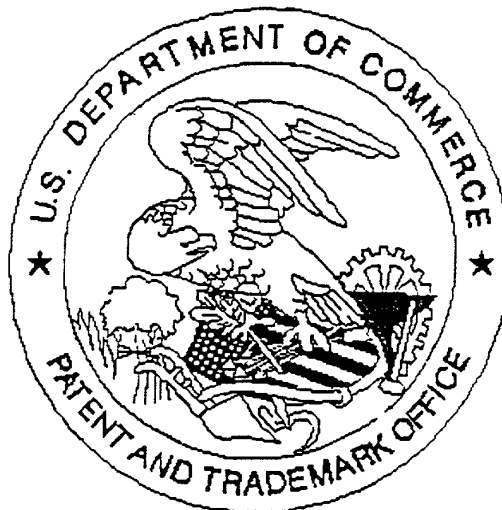
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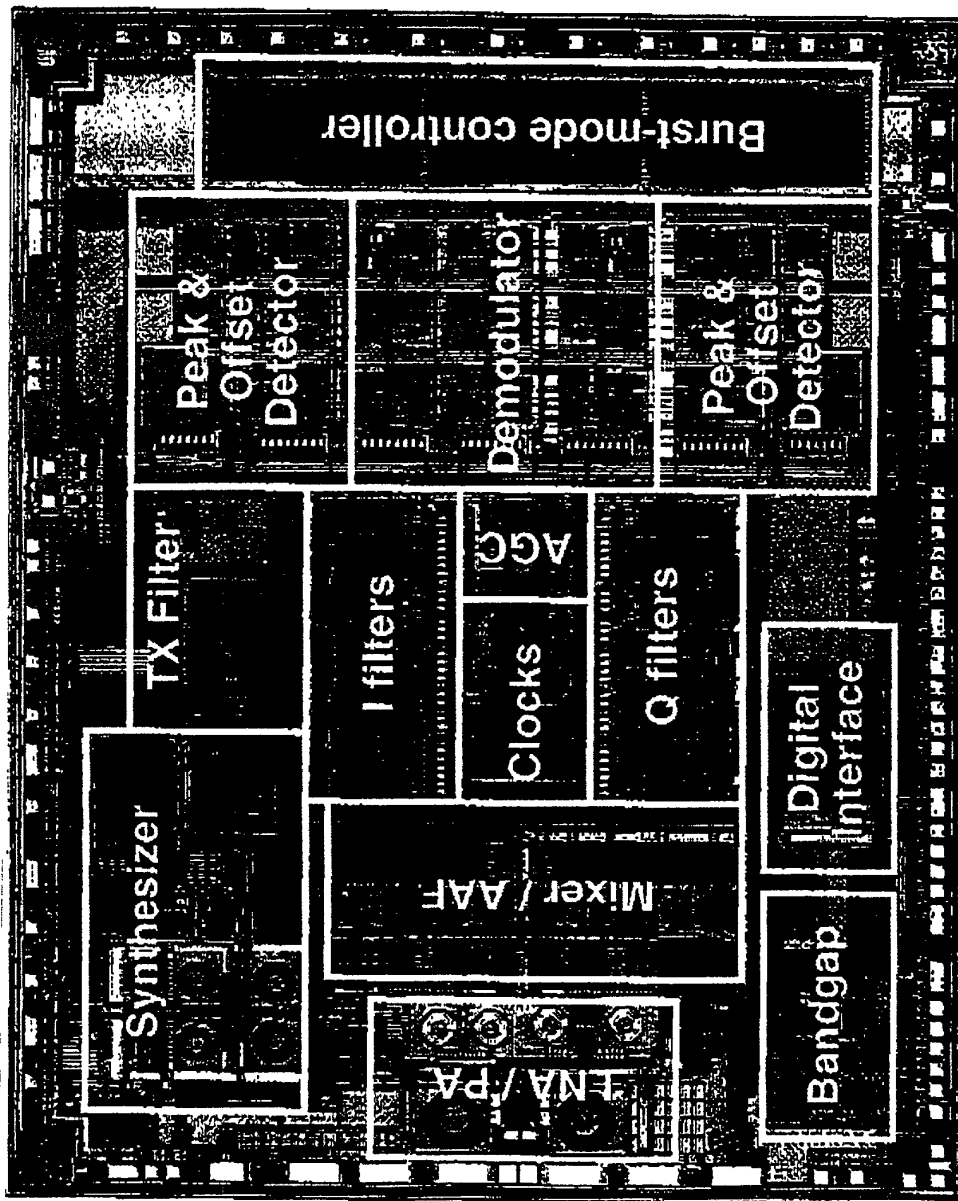


Fig. 13