

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. AND
SAMSUNG ELECTRONICS AMERICA, INC.
Petitioner

v.

SINOTECHNIX LLC
Patent Owner

Case IPR2025-00332
U.S. Patent No. 7,951,626
Claims 1, 3, 7, 9, 13, and 15

DECLARATION OF IOANNIS KYMISSIS, PH.D.
ON BEHALF OF PETITIONER

Name: Dr. Ioannis Kymissis



Signature:

Date: February 13, 2025

TABLE OF CONTENTS

	<u>Page</u>
I. Introduction.....	1
II. Relevant Law	6
A. Person of Ordinary Skill in the Art	6
B. Claim Construction	7
C. Anticipation	8
D. Obviousness.....	8
III. Summary of Opinions.....	10
IV. Technology Background.....	11
A. Light Emitting Diodes	11
B. Photolithography	12
V. Overview Of The '626 Patent.....	14
A. Alleged Problem.....	14
B. Purported Invention.....	15
C. Prosecution History	18
VI. Level Of Ordinary Skill In The Art.....	20
VII. Claim Construction.....	21
VIII. Specific Grounds of Invalidity	21
A. Ground I: Eliashevich In Combination With Rabinzohn Renders Obvious Claims 1 and 3.	21
1. Overview of Eliashevich (EX1003).....	21

2.	Rabinzohn (EX1004)	31
3.	Eliashevich In Combination With Rabinzohn ("Eliashevich-Rabinzohn")	33
1.	Claim 1	44
2.	Claim 3	59
B.	Ground II: Eliashevich In Combination With Rabinzohn And Yoo Renders Obvious Claim 7	63
1.	Claim 7	63
C.	Ground III: Eliashevich In Combination With Rabinzohn and Huang Renders Obvious Claims 9 and 15.	70
1.	Huang (EX1006)	70
2.	Eliashevich In Combination With Rabinzohn And Huang ("Eliashevich-Rabinzohn-Huang")	71
3.	Claim 9	77
4.	Claim 15	85
D.	Ground IV: Eliashevich In Combination With Rabinzohn, Huang, And Yoo Renders Obvious Claim 13	86
1.	Claim 13	86
E.	Ground V: Horio Anticipates Claims 9, 13, And 15	89
1.	Horio (EX1007)	89
2.	Claim 9	95
3.	Claim 13	117
4.	Claim 15	118

IX.	Conclusion	119
X.	Availability for Cross-Examination	119
XI.	Right to Supplement	119
XII.	Jurat.....	119

I, Ioannis Kymissis, declare as follows:

1. My name is Ioannis Kymissis.
2. I have been retained as an expert witness on behalf of Petitioner Samsung Electronics Co., LTD., and Samsung Electronics America, Inc. to provide expert opinions on the validity of U.S. Patent No. 7,951,626 (“’626 Patent”).

I. Introduction

3. I am currently the Kenneth Brayer Professor in Electrical Engineering and Vice Dean of Infrastructure and Innovation at Columbia’s school of Engineering and Applied Science in New York, NY. I have been a faculty member in the Department of Electrical Engineering since 2006.

4. I received a bachelor’s (S.B.) in Electrical Engineering and Computer Science in 1998, a master’s (M.Eng.) in Electrical Engineering and Computer Science in 1999, and a doctoral degree (Ph.D.) in Electrical Engineering and Computer Science in 2003, all from Massachusetts Institute of Technology (MIT) in Cambridge, MA. During that time, I developed the manufacturing processes for semiconductor devices, such as the manufacturing processes for double-gated silicon field emitters, organic thin-film transistors, organic TFT controlled organic field emitter, and integrated organic field-effect transistors. I was also a co-op at IBM research while I was a student, and worked at IBM’s laboratories in Yorktown

Heights, New York, and Tokyo, Japan while also pursuing my undergraduate and M. Eng degrees.

5. In 2003 I began a post-doc, also at MIT, and in 2005 I was the first employee of QDVision, a small company in Massachusetts which was developing quantum dot technologies for displays. While I worked at QDVision, I was deeply involved in a program to create quantum dot color converters for LEDs, and worked with LEDs from a number of partners (especially Luminus Devices) to integrate green and red quantum dots directly on blue emitting GaN LEDs. This technology eventually formed the basis for QLED display technologies which are in wide use today.

6. I am also a co-founder of several companies in the LED and semiconductor space, and serve as a technical advisor and board member. I have maintained my cleanroom certifications and have personally been involved in the hands-on microfabrication of LED devices using GaN including cleaning, PVD, CVD, photolithography, laser annealing, and etch. I have also led several projects transferring the fabrication process to partner cleanrooms, which operate under license to the company.

7. A copy of my curriculum vitae (“CV”) is attached as Appendix A. My CV includes my employment history, education, awards, advisory positions, publications, conference presentations, and patents.

8. In general, I am familiar with matters involving patents, including analyzing claims from the perspective of a person of ordinary skill in the art at the time the purported invention was made.

9. I am familiar with the technology described in U.S. Patent No. 7,951,626 (“’626 Patent”).

10. To my knowledge and understanding, the ’626 Patent claims priority to U.S. Patent Application No. 12/613,275, filed November 5, 2009, which is a divisional of U.S. Patent Application No. 11/993,965, filed December 26, 2007, which is a national entry application of PCT Application No. PCT/KR2006/002427, filed June 22, 2006. PCT Application No. PCT/KR2006/002427 originated from Korean Patent Application No. 10-2005-0053797, which was filed June 22, 2005, Korean Patent Application No. 10-2005-0055179, which was filed June 24, 2005, and Korean Patent Application No. 10-2006-0021801, which was filed March 8, 2006. EX1012 [FH of the ’275 Appl; ’626 Patent.], 43-44; EX1013 [FH of the ’965 Appl.].

11. I am familiar with the knowledge and capabilities of a person of ordinary skill in the art at the time of the earliest possible priority date of the ’626 Patent, which is June 22, 2005.

12. In preparation for this declaration, I have reviewed and considered the following references, which I understand to be prior art in view of the earliest possible priority date of the '626 Patent:

- PCT Application Publication No. WO2002/059983 (“Eliashevich”)
- U.S. Patent No. 5,378,309 (“Rabinzohn”)
- U.S. Patent Application Publication No. 2003/0189212 (“Yoo”)
- U.S. Patent No. 6,444,410 (“Huang”)
- U.S. Patent Application Publication No. 2005/0281303 (“Horio”)

13. Below, I provide the list of exhibits that I considered during my preparation of this Declaration. I have reviewed all of the exhibits and all documents mentioned in my Declaration. Further, my opinions are based on my technical education, experience, and training in the field.

Petitioner Exhibit No.	DESCRIPTION
1001	U.S. Patent No. 7,951,626 (“’626 Patent”)
1003	PCT Application Publication No. WO2002/059983 (“Eliashevich”)
1004	U.S. Patent No. 5,378,309 (“Rabinzohn”)
1005	U.S. Patent Application Publication No. 2003/0189212 (“Yoo”)
1006	U.S. Patent No. 6,444,410 (“Huang”)
1007	U.S. Patent Application Publication No. 2005/0281303 (“Horio”)
1008	U.S. Patent Application Publication No. 2006/0169993 (“Fan”)
1009	U.S. Patent No. 7,053,419 (“Camras”)
1010	U.S. Patent No. 6,229,160 (“Krames”)
1011	H. Xiao, “Introduction to Semiconductor Manufacturing Technology,” “Chapter 6,” Prentice Hall, 2001
1012	File History of U.S. Patent No. 7,951,626

Petitioner Exhibit No.	DESCRIPTION
1013	File History of U.S. Application No. 11/993,965
1014	L.F. Thompson, "Introduction to Microlithography," "Chapter 1. Introduction to Photolithography," <i>ACS Symposium Series</i> Vol. 219, 1983 ("Thompson") ¹
1015	D. J. Kim, "Characterization and Modeling of Positive Photoresist," Memorandum No. UCB/ERL M84/65, 1984 ("Kim")
1016	S. L. Morton et al., "Ultrasonic Sensor for Photoresist Process Monitoring," <i>IEEE Transactions on Semiconductor Manufacturing</i> , Vol. 12, No. 3, August 1999 ("Morton")
1017	E. J. Jewell et al., "The New Oxford American Dictionary," Oxford University Press, p. 1286, 2001
1021	T. Nakazawa et al., "Compact and monolithic coarse wavelength-division multiplexer-demultiplexer fabricated by use of a high-spatial-frequency transmission grating buried in a slab waveguide," Vol. 29, Issue 11, pp. 1188-1190, 2004 ("Nakazawa") ²
1022	U.S. Patent Application No. 2006/0231852 ("Kususe")
1023	H. Jansen et al., "A survey on the reactive ion etching of silicon in microtechnology," <i>Micromechanics Europe 1995 Technical Digest</i> , 1995 ("Jansen")

14. I have been retained as an expert for Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. in the field of semiconductor manufacturing, specifically manufacturing of semiconductor light emitting devices.

15. My compensation for this case is at my usual and customary rate for the time I spent on this IPR. My compensation is not and will not be affected by the outcome of this case.

¹ Available at <https://pubs.acs.org/doi/10.1021/bk-1983-0219.ch001>

² Available at <https://opg.optica.org/ol/abstract.cfm?uri=ol-29-11-1188>.

16. I have no financial interest in the outcome of the case. I also do not have any financial interest in either Samsung Electronics Co., Ltd. or Samsung Electronics America, Inc.

17. I do not have personal contact or knowledge of the named inventors in the '626 Patent.

II. Relevant Law

18. I am not an attorney. Petitioner's counsel has informed me about the following aspects of patent law, which I applied in my analysis and conclusions.

A. Person of Ordinary Skill in the Art

19. I have been informed that a patent and prior art should be reviewed from the perspective of a person of ordinary skill in the art ("POSITA"). I understand that a POSITA is an individual who is hypothetical, is of ordinary creativity, and would have been familiar with the prior art as of the patent's claimed priority date.

20. I have been informed that there are various factors that are applicable in determining the level of a person of ordinary skill in the art. These include:

- (1) the educational level of the inventor;
- (2) type of problems encountered in the art;
- (3) prior art solutions to those problems;
- (4) rapidity with which innovations are made;

(5) sophistication of the technology; and

(6) educational level of active workers in the field.

21. I have been informed that not all such factors may be present in every case, and one or more of these or other factors may predominate.

B. Claim Construction

22. I have been informed that claim construction is a matter of law that will ultimately be determined by the Board. To determine the meaning of claim terms for the purposes of the *inter partes* review, I have been informed that one should generally use the ordinary and customary meaning as understood by a POSITA at the time of the claimed priority date, in view of the claim language, patent specification, and the file history. I have been informed that the proper interpretation of the claim term should be arrived at in light of the patent's claims, specification, and file history.

23. Further, I understand that although a claim term should be read in light of the specification, limitations should not be imported into the claim from the specification. I understand that interpreting a claim term to exclude a preferred embodiment is often inaccurate. I have also been informed that the prosecution history can facilitate the meaning of a claim term or a claim by demonstrating how the inventor understood the invention and by showing whether the inventor limited

the claim term or claim during the course of prosecution or caused the claim scope to be narrower than it otherwise would be.

C. Anticipation

24. I understand that a patent claim is invalid for being anticipated if each limitation of that claim is present either explicitly, implicitly, or inherently in a single prior art reference. I also understand that, to be an inherent disclosure, the prior art reference must necessarily disclose the limitation, and the fact that the reference might possibly practice or contain a claimed limitation is insufficient to establish that the reference inherently teaches the limitation.

D. Obviousness

25. I have been informed that a claim is invalid if the claim would have been obvious from the perspective of a person of ordinary skill in the art at the time the alleged invention was made.

26. I understand that an obviousness evaluation involves consideration of several factors, including:

- a. the level of ordinary skill in the art at the time the application was filed;
- b. the scope and content of the prior art; and
- c. what differences, if any, existed between the claimed invention and the prior art.

27. In determining whether a combination based on multiple references would have been obvious, it is appropriate to consider, among other factors:

- a. whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;
- b. whether a person of ordinary skill in the art could implement a predictable variation, and would see the benefit of doing so;
- c. whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by those skilled in the art;
- d. whether a person of ordinary skill would have recognized a reason to combine known elements in the manner described in the claim;
- e. whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- f. whether the claim applies a known technique that had been used to improve a similar device or method in a similar way.

28. I understand that a claim is obvious if it combines old elements without any change to their respective functions. I also understand that a claim is obvious if the claim simply substitutes one element for another element known in the field, and the resulting combination yields predictable results. Further, while it may be helpful

for there to be a reason for the combination, I understand that it is not strictly required to find an express teaching, suggestion, or motivation to combine within the references. Market forces, such as design incentives, can prompt variations of a product, either in the same field or a different field. Further, for techniques, if a technique has been used to improve one device and if a POSITA would recognize that applying the same technique would have improved a different device in a comparable way, then it would have been obvious if common sense directs one to combine multiple prior art references or add missing factors.

29. I have been informed and understand that hindsight bias must be avoided when determining obviousness. Accordingly, the patent's claims and descriptions cannot be used as a roadmap when analyzing combinations of prior art references.

III. Summary of Opinions

30. I conclude that claims 1, 3, 7, 9, 13, and 15 of the '626 Patent unpatentable for being anticipated by, or being obvious over, the prior art reference(s) identified in each Ground below:

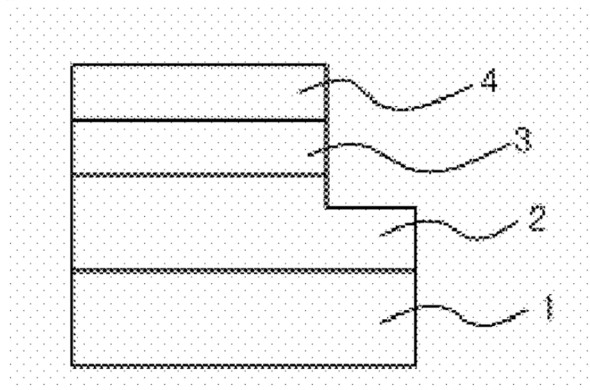
Ground	35 U.S.C.	Claims	Prior Art Reference(s)
I	§103	1, 3	Eliashevich, Rabinzohn
II	§103	7	Eliashevich, Rabinzohn, Yoo
III	§103	9, 15	Eliashevich, Rabinzohn, Huang
IV	§103	13	Eliashevich, Rabinzohn, Huang, Yoo
V	§102	9, 13, 15	Horio

IV. Technology Background

A. Light Emitting Diodes

31. When current flows through a light emitting device (“LED”), which is a semiconductor device, the LED emits light. An LED, as shown below, usually includes a P-type semiconductor layer 4 formed on an active layer 3, which is formed on an N-type semiconductor layer 2. EX1001, 2:13-26 (background). The active layer 3 provides a junction between the P-type layer 4 and the N-type layer 2 and typically, the active layer 3 generates light when a voltage is applied to the P-type layer and the N-type layer 2. EX1001, 1:28-31 (background).

[Figure 1]

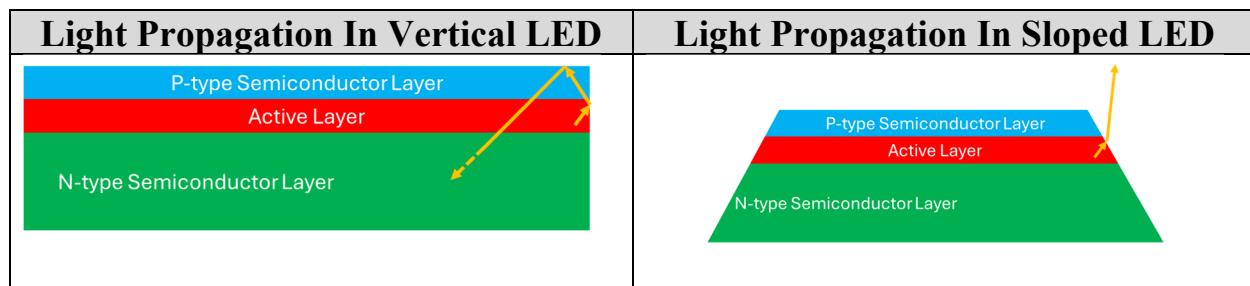


EX1001, Figure 1 (background).

32. A portion of the generated light being trapped inside the LEDs is a well-known issue of LEDs. For instance, light rays are generated in all directions by the active layer. The light can either escape the LED through refraction (making the light visible to observers on the outside) or is trapped inside the LED (because the

light is trapped entirely internally). Whether the light escapes the LED or is trapped inside the LED is based on the angle at which the generated light strikes the physical interface between the LED's surrounding material (e.g., air) and the LED. EX1009, 1:20-23; EX1003, 5:7-25. The LED's efficiency is reduced by the trapped light. EX1003, 5:26-30.

33. Reducing the amount of trapped light due to total internal reflection by sloping the side surface of the LED was well known. EX1010, 3:6-9 As illustrated below, there is a higher likelihood that light escapes the LED when the side surface of the LED is sloped, because the light strikes the interface at a shallower angle. EX1008, [0020], Figure 2.



B. Photolithography

34. LEDs and other semiconductor devices usually include several layers, and a process called photolithography is used to pattern those layers. For semiconductors, photolithography usually includes the following steps:

- Step 1: Deposit a semiconductor material as a thin film;
- Step 2: Apply on the semiconductor layer a photoresist layer;
- Step 3: Expose the photoresist layer to light through a photomask;

Step 4: Form an etching mask pattern by developing the exposed photoresist layer;

Step 5: Etch the portions of the semiconductor layer that are exposed;

Step 6: Remove the rest of the photoresist.

EX1014, 1-4, 7-9.

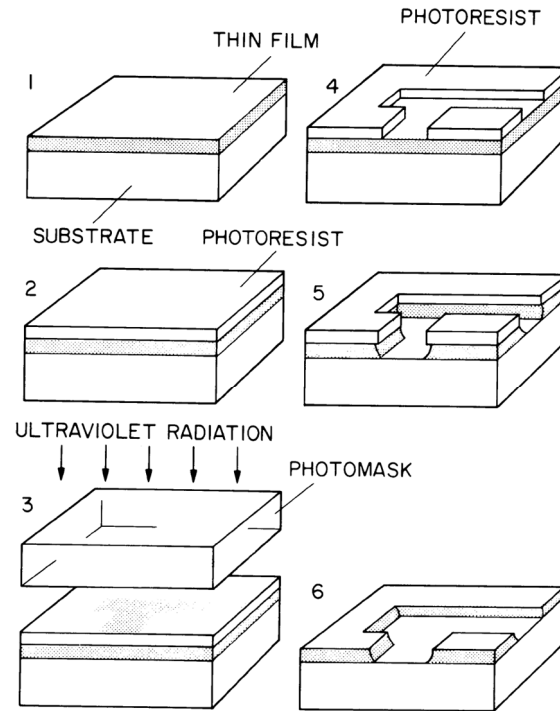
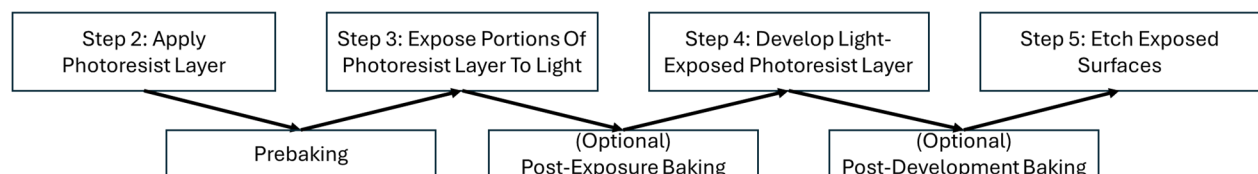


Figure 5. A typical photolithography process

EX1014, Figure 5.

35. As shown at the bottom row of the figure below, photolithography typically includes baking the photoresist layer at various stages (although not shown above in the illustration). EX1013, 22-23, 31-32, 35-36.



36. For instance, in step 2, applied on top of the underlying material layer is a photoresist in its viscous form using, for example, a spin coater. EX1013, 13-16. The photoresist undergoes a “prebaking” or “soft bake” step before step 3, which evaporates the solvent from the photoresist. EX1016, 1; EX1013, 13-14, 22-23.

37. After step 3 (i.e., after the soft-baked photoresist is selectively exposed to light) but before step 4 (i.e., before it is developed), an optional post-exposure baking (“PEB”) step is performed on the photoresist to cause the exposure pattern to be more uniform. EX1016, 1; EX1013, 31-32.

38. Optionally, “[a]fter the development [in step 4,] the resist is *often baked again at higher temperature* for better adhesion” between the underlying material and the photoresist layer. EX1015, 11; EX1013, 35-36.

V. Overview Of The '626 Patent

A. Alleged Problem

39. The '626 Patent is directed to a process of manufacturing a “light emitting device.” EX1001, 1:21-26. As stated by the '626 Patent, conventional LEDs have vertical side surfaces, which restrict the efficiency of the LEDs because “a portion of light produced within the light emitting is device is totally reflected on the etched surface that is processed vertically from a horizontal plane.” EX1001, 2:56-67.

Light produced from a light emitting layer of a light emitting device is emitted from all the surfaces of a chip, and light extraction efficiency is generally determined by a critical angle of light. However, when the conventional light emitting device is etched to expose an N-type semiconductor layer, side surfaces of the P-type semiconductor layer and the active layer are vertically processed such that ***a portion of light produced within the light emitting device is totally reflected on the etched surface that is processed vertically from a horizontal plane.*** Then, a considerable amount of light to be totally reflected is not emitted to the outside but dissipated within the light emitting device due to the internal reflection. That is, there is a problem in that luminous efficiency in which electric energy is converted into light energy and the light is then emitted to the outside of a light emitting device is low.

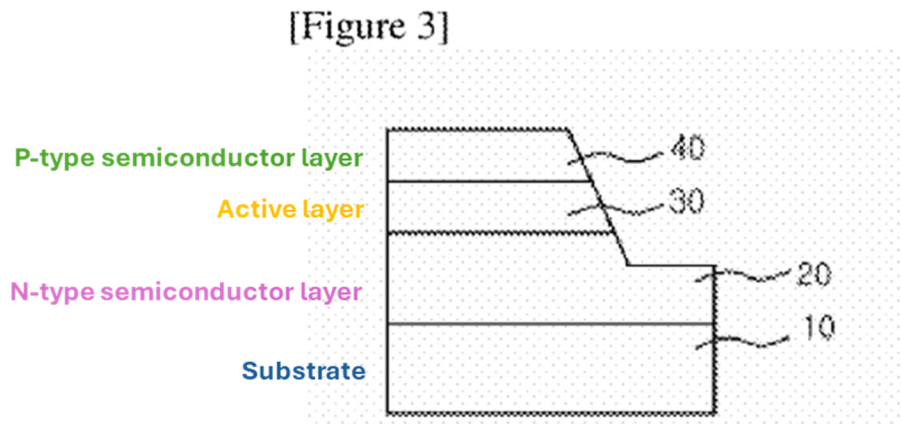
EX1001, 2:56-3:4.

B. Purported Invention

40. The '626 Patent purports to deal with the issue of the limited efficiency of conventional LEDs by having an LED with a sloped side surface, which is shown in Figure 3. A P-type semiconductor layer 40, an active layer 30, an N-type semiconductor layer 20, and a substrate 10 are included in the LED. EX1001, 5:47-56. As the '626 Patent states:

Each of side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 has ***a slope of 80 to 20° from a horizontal plane*** such that a critical angle of light can be changed by such surfaces and ***light can be easily extracted.*** Therefore, luminous efficiency of a light emitting device can be improved.

EX1001, 5:50-56.



EX1001, Figure 3³.

41. The '626 Patent states that etching the layers “using the etching mask pattern [*e.g.*, made using a photoresist] with such a slope of the side surface” forms the layers 20, 30, 40 with a sloped side surface. EX1001, 6:60-7:5. EX1001, 7:27-40.

However, in this embodiment, the photoresist is applied at a thickness of 3 to 50 um which is thicker as compared with the prior art when the etching mask pattern is formed, and the exposure process is performed after the soft-baking. Next, if the photoresist is directly developed without the hard-baking, a developed side Surface of the remaining photoresist is formed into an inclined surface not perpendicular (90) to but inclined at a predetermined slope is from a horizontal plane. *Subsequently, if exposed regions of the P-type semiconductor layer 40, the active layer 30 and the predetermined N-type semiconductor layer 20 are etched using the etching mask pattern with such a*

³ All annotations in the figures are added unless I note otherwise.

slope of the side surface, the side surfaces of the etched P-type semiconductor layer 40, active layer 30 and N-type semiconductor layer 20 can be similarly formed into an inclined surface not perpendicular (90) to but inclined at a predetermined slope from the horizontal plane.

EX1001, 6:57-7:5.

Alternatively, after a photoresist has been applied at a thickness of 3 to 50 μm on the P-type semiconductor layer 40 of FIG. 4 and light-exposed, hard-baking may be performed. In such a case, if the photoresist is hard-baked at a temperature of 100 to 140°C. and then developed, the side surface of the developed photoresist may be etched to have a slope of 80 to 20° from a horizontal plane. *For example, in a case where the hard-baking is performed at a temperature of 100°C., an etching mask pattern with a slope of about 80° from the horizontal plane can be obtained, and the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 can have a slope of about 80° from the horizontal plane using the etching mask pattern.* Further, in a case where the hard-baking is performed at a temperature of 140°C., an etching mask pattern with a slope of about 20° from the horizontal plane can be obtained, and the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 can have a slope of about 20° from the horizontal plane using the etching mask pattern.

EX1001, 7:21-7:40.

42. To form the etching mask with a sloped side surface, the '626 Patent discloses: (1) providing a photoresist layer; (2) soft-baking at a temperature of 80 to 90°C the photoresist; (3) exposing light to the layer of photoresist; and (4) developing without any baking after the light exposure such that a “developed side

surface of the remaining photoresist is formed into an inclined surface not perpendicular (90°) to but inclined at a predetermined slope ... from a horizontal plane.” EX1001, 6:57-64, 7:6-9.

43. In addition, the '626 Patent discloses that an etching mask with a side surface that is sloped can be manufactured by: carrying out (1)-(3) as above; (4) hard-baking at a temperature of 100 to 140°C the exposed photoresist layer; (5) developing the photoresist layer that has been hard-baked; and (6) etching the developed photoresist's side surface “to have a slope of 80 to 20° from a horizontal plane.” Indeed, the '626 Patent states “if the photoresist is hard-baked at a temperature of 100 to 140° C. and then developed, the side surface of the developed photoresist may be etched to have a slope of 80 to 20° from a horizontal plane.” EX1001, 7:21-40.

C. Prosecution History

44. I have reviewed the file history of the '626 Patent and its parent patent application. EX1012, EX1013. Below, I summarize the relevant information from the file history of the '626 Patent and any additional relevant information from the file history of related applications that is pertinent to my opinion.

45. The '626 Patent was filed as No. 12/613,275 (“’275 Application”) on November 5, 2009. The '626 Patent is a divisional application of U.S. Patent Application No. 11/993,965 (“’965 Application”), filed December 26, 2007. The

'965 Application is a national entry application of PCT Application No. PCT/KR2006/002427, which was filed June 22, 2006, which claims priority to Korean Patent Application No. 10-2006-0021801, filed March 8, 2006, Korean Patent Application No. 10-2005-0055179, filed June 24, 2005, and Korean Patent Application No. 10-2005-0053797, filed June 22, 2005. EX1012 [FH of the '275 Appl.; '626 Patent], 43-44; EX1013 [FH of the '965 Appl.].

46. Originally, the '275 Application included claims 1-10. EX1012, 104-107. The only independent claim 1 was directed towards a method of manufacturing an LED using an etching mask pattern having a sloped side surface. EX1012, 104.

47. The Examiner initially issued a restriction requirement, and in response, Applicant elected claims 1-2 and 5-10. EX1012, 496, 503.

48. Claims 1-2, 5-7, and 10 were rejected for being obvious over U.S. Patent No. 7,213,942 ("Jiang '942") in view of U.S. Patent Publication No. 2005/0023537 ("Salam") or U.S. Patent No. 7,598,149 ("Dawson") or U.S. Patent No. 7,057,208 ("Akimoto") in an Office Action dated December 23, 2010. EX1012, 516-520. In that Office Action, the Examiner also rejected claim 9 for being indefinite. EX1012, 515. However, claim 8 was indicated to be allowable if it is written as an independent claim. EX1012, 520.

49. In response to that Office Action: (1) claims 8 and 9 were canceled; (2) claim 1 was amended to include then-cancelled claim 8's allowable subject matter;

(3) new independent claim 11 was added to be about the subject matter of the then-cancelled claim 9; (4) new independent claims 12-17 were added that depend from claim 11, and (5) rejoinder was sought of claims 3 and 4. EX1012, 552-562.

50. Pending claims 1-7 and 10-17 were subsequently allowed and issued as claims 1-15. EX1012, 566-573, 583.

VI. Level Of Ordinary Skill In The Art

51. I have reviewed the factors relevant for determining the level of a person of ordinary skill in the relevant field or art (“POSITA”) outlined in Section II.A in the context of the ’626 Patent. The ’626 Patent relates to a method of making a semiconductor light emitting device. EX1001, Title, Abstract. The field of light emitting devices and manufacturing light emitting devices was well-researched by the earliest claimed priority date of the ’626 Patent – June 22, 2005, as explained in Section V.C. As demonstrated by prior art of record in the prosecution history of the ’626 Patent, the sort of problems seen in the art, e.g., internal reflection causing limited efficiency, and solutions to these problems, e.g., a side surface that is sloped on the light emitting diode, were all well known in the art. EX1008, [0020], Figure 2.

52. As such, a POSITA as of the earliest claimed priority date of the ’626 Patent would have had a Bachelor’s degree in Electrical Engineering, Material Science, Physics, or an equivalent field, and approximately two years of experience

in the field of semiconductor manufacturing. Lack of professional experience can be substituted by additional education, and vice versa.

53. At the time of the claimed priority date of the '626 Patent (June 22, 2005), I met and/or exceeded the above requirements for a POSITA.

VII. Claim Construction

54. I have reviewed the specification, the claims, and the relevant file histories of the '626 Patent, including the file history of the '626 Patent and its parent application.

55. I have been asked to determine if any claim term should be construed so the Board can understand how the prior art references read on the challenged claims. I have not identified any terms that the Board needs to construe for the purposes of this IPR.

VIII. Specific Grounds of Invalidity

A. Ground I: Eliashevich In Combination With Rabinzohn Renders Obvious Claims 1 and 3.

1. Overview of Eliashevich (EX1003)

56. I will begin with the description of the prior art reference called Eliashevich.

57. Eliashevich disclosed a large part of the claimed subject matter before the '626 Patent. Similar to the '626 Patent, Eliashevich describes “methods of

making light emitting diodes.... having optimized light extraction characteristics.”

EX1003, 1:4-6.⁴

The present invention relates to making optoelectronic devices, packages for such devices, and methods for making the foregoing, and particularly relates to ***methods of making light emitting diodes*** and light-emitting diode packages ***having optimized light extraction characteristics***, and methods of making the foregoing.

EX1003, 1:2-7.

58. According to Eliashevich, its LEDs include “thin layers of semiconductor material of two opposite conductivity types, referred to as p-type and n-type” (EX1003, 1:8-10), and sandwiched between the p-type and n-type layers is a junction layer that generates light (EX1003, 1:15-19).

Light-emitting diodes or “LEDs” include ***thin layers of semiconductor material of two opposite conductivity types, referred to as p-type and n-type***. The layers are disposed in a stack, one above the other, with one or more layers of the n-type material in one part of the stack and one or more layers of p-type material at the other end of the stack. For example, the various layers may be deposited in sequence on a substrate to form a wafer. *The junction between the p-type and n-type material may include directly abutting p-type and n-type layers*, or may include one or more intermediate layers which may be of any conductivity type or which may have no distinct conductivity type.

⁴ In the rest of the Declaration, when I quote a portion of a prior art reference, I will also reproduce, where appropriate, the full paragraph of the prior art reference in which the quote appears.

EX1003, 1:9-20.

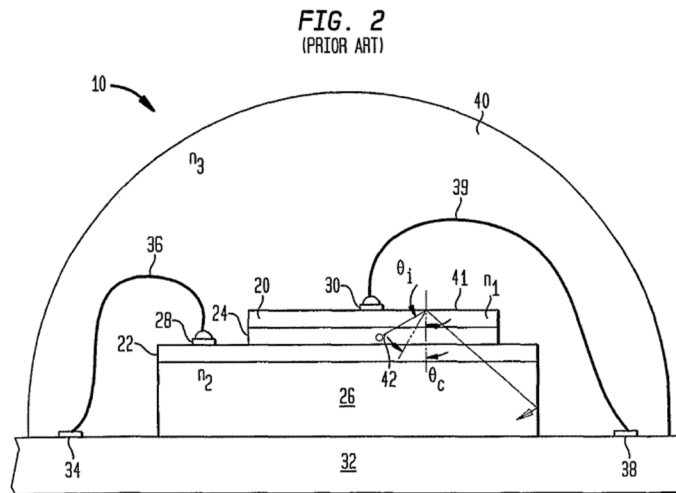
59. In a conventional LED (as shown in Figure 2 below), Eliashevich discloses that “many of the light rays generated at the junction layer are never emitted from the package, but are totally internally reflected within the package” (EX1003, 5:26-28), which causes efficiency to be reduced. EX1003, 5:7-25, FIG.

2.

In operation, the light is emitted from the LED. Because the index of refraction of the semiconductor structure (n_1) is greater than the index of refraction of the transparent encapsulant 40 (n_3), *many of the light rays generated by the LED will not be emitted from the LED package 10, but will be subject to total internal reflection.* This optical phenomenon, known as total internal reflection, causes light incident upon a medium having a lesser index of refraction (e.g., encapsulant layer 40) to bend away from the normal so that the exit angle is greater than the incident angle. The exit angle will then approach 90° for some critical incident angle θ_c that is calculated using Snell's law. When the incident angle θ_i of a light ray is greater than critical angle θ_c , there will be a total internal reflection of the light ray. Referring to FIG. 2, the incident angle θ_i of light ray 42 is greater than the critical angle θ_c at an interface 41 between p-type layer 20 and encapsulant 40. As a result, light ray 42 is not extracted from the LED, but is totally internally reflected.

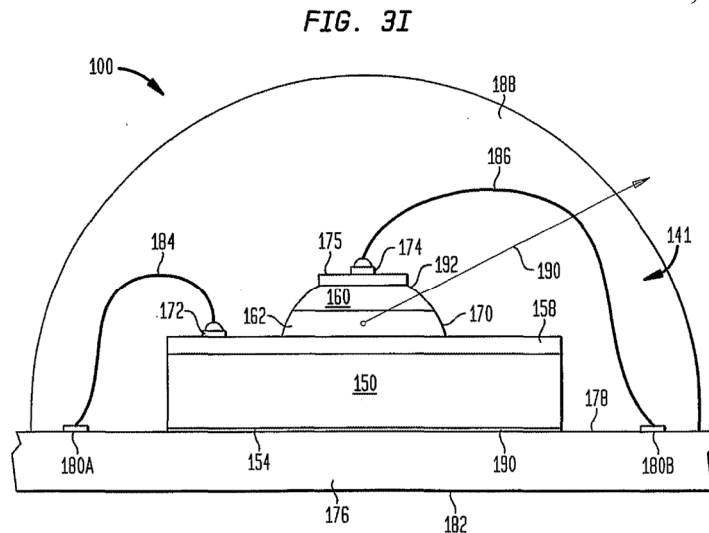
In many LED packages, many of the light rays generated at the junction layer are never emitted from the package, but are totally internally reflected within the package. Thus, there is a need for LED packages having designs that optimize the amount of light that may be extracted therefrom.

EX1003, 5:7-30.



EX1003, Figure 2.

60. Eliashevich also discloses an LED that has a non-vertical side surface, which decreases internal reflection, to improve efficiency. EX1003, 6:10-19. The LED disclosed by Eliashevich has a junction layer 162, a p-type layer 160, and an n-type layer 158 (EX1003, 14:33-15:13), and a “mesa” is formed from the junction layer 162, the p-type layer 160, and optionally a part of the n-type layer 158 (EX1003, 16:33-17:8). Eliashevich also discloses that the light that is generated by junction layer 162 is more easily extracted when the side surface 170 of the mesa is made non-vertical. EX1003, 6:11-18, 19:17-26.



EX1003, Figure 3I.

61. Eliashevich uses Figures 3A-3I to explain the process of making an LED that has a non-vertical side surface. EX1003, 14:12-14. As shown in Figures 3A-3B, Eliashevich describes a “stacked structure 110” which includes “a junction [layer] 162 between the n-type layers 158 and p-type layers 160 (EX1003, 14:33-15:13) and a substrate 150 (EX1003, 14:14-17).

FIGS. 3A-3J show a method of making an optoelectronic device package in accordance with one embodiment of the invention. A substrate 150, as shown in FIG. 3A, is provided on a support 149. The substrate 150 has a first, upwardly facing surface 152 and a second surface 154 facing in a direction opposite from the first surface 152. In certain preferred embodiments, the substrate 150 is a substantially transparent substrate. The substrate may comprise a sapphire substrate. The substrate may also comprise GaN, AlN, ZnO, SiC, or LiGaO. ***A semiconductor structure 110 comprising a stacked structure of semiconductor layers is formed on the substrate 150.*** A semiconductor material having

a first conductivity type is deposited on the first surface 152 of the substrate 150. For example, one or more n-type layers 158 are deposited on the first surface 152 of substrate 150. A semiconductor material having a second conductivity type is deposited over the semiconductor material of the first conductivity type. ***One or more p-type layers 160 having a top surface 166 are deposited over the n-type layers 158. A junction is also formed between the n-type layers 158 and p-type layers 160.***

The stacked structure 110 of FIGs. 3A-3J comprises a structure the embodiment shown in for an LED, including a junction 162 between the n-type layers 158 and p-type layers 160. The junction is shown schematically in FIG. 3B as a discrete layer interposed between the layers 158 and 160. In practice, the junction may comprise the border between directly abutting p-type and n-type layers, or one or more intermediate layers. The intermediate layers may have any conductivity type or no conductivity type. Alternatively, the junction may include additional structures in between the p-type layers 160 and n-type layers 158 or in an intermediate region. Thus, the junction may be a simple homojunction; a single heterojunction, a double heterojunction, a single quantum well, a multiple quantum well or any other type of junction structure. A person of ordinary skill in the art will appreciate that that the semiconductor structure may incorporate various layers of semiconductor materials, as well as other structures used in the optoelectronic arts.

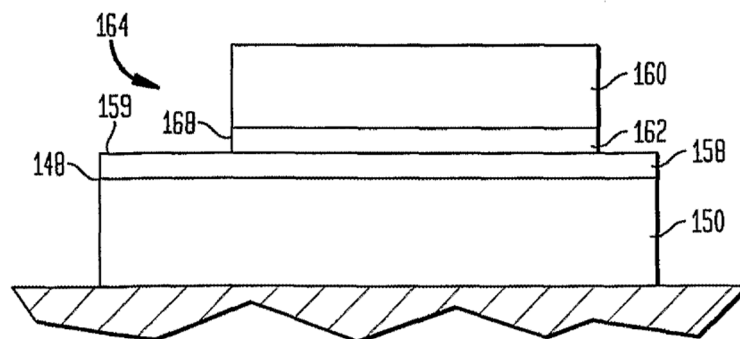
EX1003, 14:12-15:16.

62. Subsequently, “[t]he semiconductor structure 110 ... is preferably etched to form an upwardly projecting mesa 164 and a lower surface 159,” as shown below in Figure 3C. EX1003, 17:2-8.

The semiconductor structure 110 has an upper end 161 and a lower end 163. In certain preferred embodiments, an upwardly projecting mesa 164 is formed in the semiconductor structure 110. ***The semiconductor structure 110 shown in FIG. 3B is preferably etched to form an upwardly projecting mesa 164 and a lower surface 159.*** The layers of semiconductor material which form the p-type layers 160 and the junction 162 are removed by selectively etching the structure 110. In certain preferred embodiments, a portion of the n-type layers 158 is also removed. The regions in those areas which are to form the mesa 164 are protected by a mask during etching so as to form the upwardly projecting mesa 164. Such an etching process may use, for example, conventional photolithographic masking techniques. Etching to remove part of the structure 110 forms a lower surface 159. Alternatively, the lower surface 159 and mesa 164 may be formed by selective deposition. In a selective deposition or additive process, the n-type layers 158 are deposited on the substrate 150. The areas of the n-type layers 158 which are to form the lower surface 159 are covered with a masking material or otherwise protected from the deposition process. Semiconductor material for the junction 162 and p-type layers 160 are deposited on the n-type layers 158, so that the uppermost layers in the stack are not formed in these areas.

EX1003, 16:33-17:23.

FIG. 3C



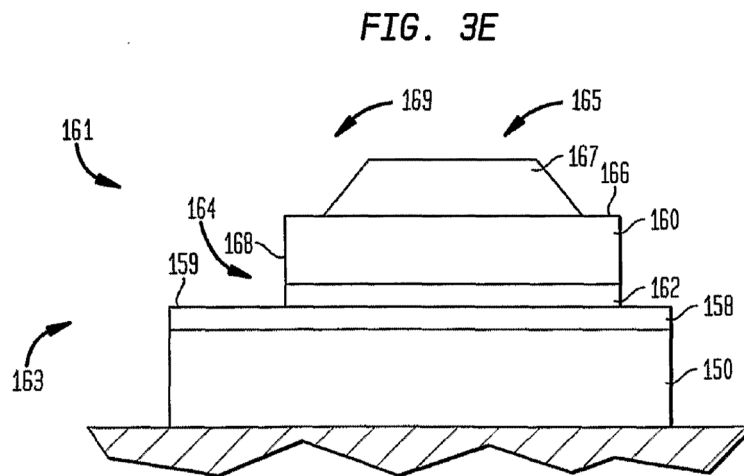
EX1003, Figure 3C.

63. Next, “[a] photoresist material 167 [is deposited]... on the top surface 166 of mesa 164 and is exposed and developed to form a mask 165 having openings 169,” as shown in Figure 3E below. EX1003, 18:19-21. As explained by Eliashevich, “[t]he *mask may be given a tapered shape*, as shown in FIG. 3D, utilizing controlled processing or baking of the photoresist....” EX1003, 18:26-31. Eliashevich states that “[t]hese techniques are known in the art,” though Eliashevich does not expressly disclose additional details. EX1003, 18:34-19:1.

Referring to FIGS. 3D-3F, mesa 164 is subjected to an etching process which removes some of the semiconductor material from the p-type layers 160. One preferred etching process includes a reactive ion etching (RIE) process. In other preferred methods, other forms of plasma etching are used, such as ICP. *A photoresist material 167 is deposited on the top surface 166 of mesa 164 and is exposed and developed to form a mask 165 having openings 169.* During etching, the walls 168 and a portion of the top surface 166 are attacked and semiconductor material is removed from the mesa 164 until a curved surface is obtained. Preferably, a portion of the top surface remains after etching, to be used for an upper electrode-pad unit, as discussed below. *The mask may be given a tapered shape, as shown in FIG. 3D, utilizing controlled processing or baking of the photoresist* and the relative etch rates for the photoresist and semiconductor materials may be tailored so as to form the curved surfaces on the mesa 164, at the upper end of the structure 110. The RIE etching removes the mask at an outside portion of the mesa first and then begins to remove semiconductor material from the p-type layers 160, as represented by the dashed lines in

FIG. 3D. *These techniques are known in the art.* In other embodiments, conventional lithographic techniques may also be used. The radial surfaces on the mesa may also be formed utilizing an additive process, as discussed above. In embodiments in which the radial surfaces are formed in an additive process, transparent dielectric or polymeric material is deposited on the p-type layers 160.

EX1003, 18:14-19:7.



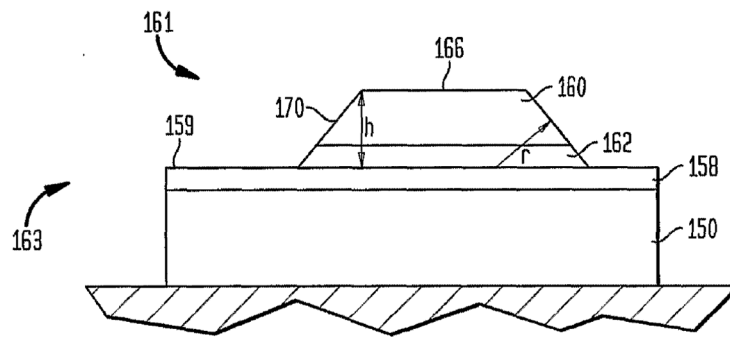
EX1003, Figure 3E.

64. Subsequently, to “form[] one or more radial surfaces 170 extending between top surface 166 and n-type layers 158 as shown in FIG. 3F,” shown below, the dry-etching step (which may be a reactive-ion etching (RIE) step), “removes the mask at an outside portion of the mesa first and then begins to remove semiconductor material from the p-type layers 160.” EX1003, 18:31-19:10. Further, “[t]he radial surface 170 optimizes the amount of light that may be extracted” EX1003, 19:14-16.

The etching process forms one or more radial surfaces 170 extending between top surface 166 and n-type layers 158 as shown in FIG. 3F. As used herein, "radial" means having a radius. It should be understood that the radial surface may not be consistent across the full length of the surface 170. The radial surface of mesa 164 is curved, preferably having a concave shape, as shown in Fig. 3F. The radial surface 170 optimizes the amount of light that may be extracted from the package, as will be described in more detail below.

EX1003, 19:8-16.

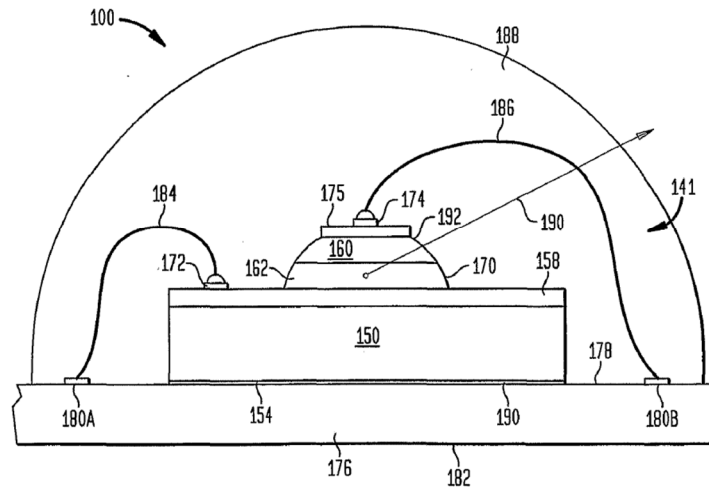
FIG. 3F



EX1003, Figure 3F.

65. Next, as disclosed by Eliashevich, electrical connections to the n-type layer 158 and p-type layer 160 are provided, and Figure 3I (below) shows the LED package. EX1003, 22:11-22.

FIG. 3I



EX1003, Figure 3I.

66. In Figure 3I, the side surface 170 has a concave shape, whereas in Figure 3F, the side surface 170 has a linear shape. That difference does not change my opinion on the validity of the challenged claims because the claims do not require a specific shape for the claimed light emitting device.

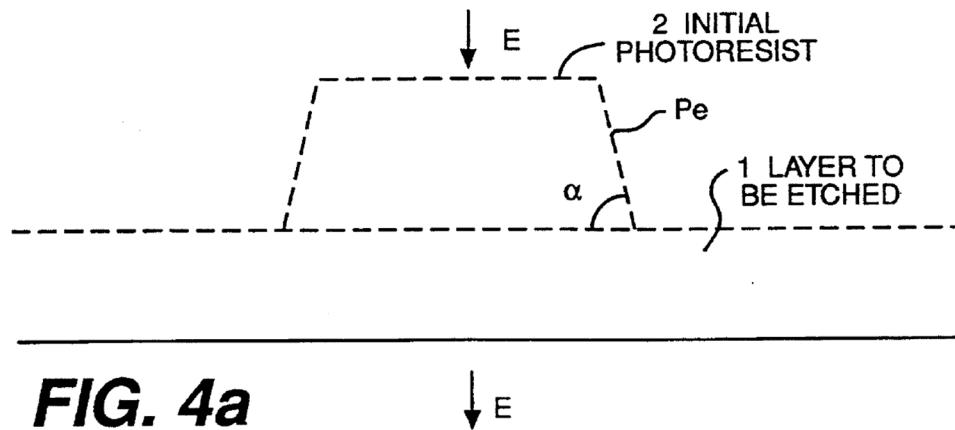
2. Rabinzohn (EX1004)

67. Rabinzohn discloses a “[m]ethod for controlling the etching profile of a layer of an integrated circuit” through using the photoresist layer’s side surface slope to transfer that slope to the underlying layer. EX1004, Title, 3:35-43, 4:1-13.

68. As an example, Rabinzohn discloses a patterned photoresist layer 2 that is provided on the layer 1 that is to be etched. EX1004, 3:31-34. The side surfaces of the patterned photoresist layer 2 are inclined at an *angle α* relative to the underlying layer 1. EX1004, 7:21-38, Figure 4a.

Alternatively, in the case of FIG. 4, the initial masking photoresist layer 2, previously to the actual etching process, has been subjected to a preetching stage, the effect of which is to generate etching flanks of slope pe inclined in relation to the free surface of the layer 1 to be etched, *assumed to be horizontal, the etching flanks of the initial masking photoresist layer 2 being thus inclined at an angle α in relation to the abovementioned free surface*. It will be noted that the preetching process may consist of a mild etching, which has the property of selectively attacking the initial masking photoresist layer 2, excluding an attack alternatively layer 1 to be etched. On the, the initial masking photoresist layer 2 can be deposited and treated so as to exhibit etching flanks which have the slope pe as shown at point a) of FIG. 4.

EX1004, 7:21-37.



EX1004, Figure 4a.

69. The sloped side surfaces on the patterned photoresist layer 2 are formed by “preetching” the photoresist layer 2. EX1004, 7:21-33, Figure 4a.

Alternatively, in the case of FIG. 4, the initial masking photoresist layer 2, previously to the actual etching process, has been subjected to a *preetching stage*, the effect of which is to generate etching flanks of slope pe inclined in relation to the free

surface of the layer 1 to be etched, assumed to be horizontal, the etching flanks of the initial masking photoresist layer 2 being thus inclined at an angle α in relation to the abovementioned free surface. It will be noted that the *preetching process* may consist of a mild etching, which has the property of selectively attacking the initial masking photoresist layer 2, excluding an attack alternatively layer 1 to be etched. On the, the initial masking photoresist layer 2 can be deposited and treated so as to exhibit etching flanks which have the slope peas shown at point a) of FIG. 4.

EX1004, 7:21-37.

70. Next, “reactive ionic etching,” which is a type of dry-etching, transfers the shape of the photoresist layer 2 to the underlying layer 1. EX1004, 4:1-23, 7:38-47, Figure 4d.

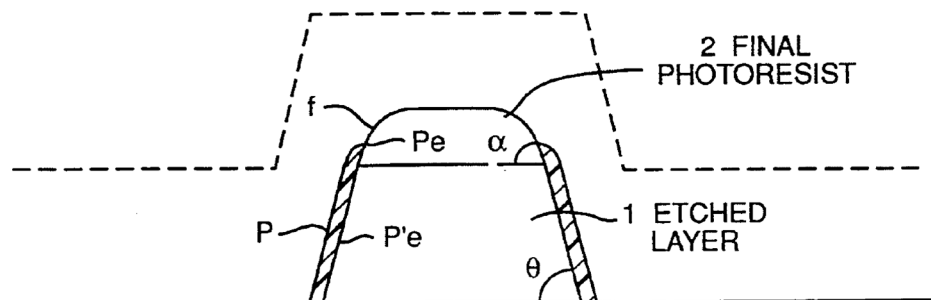


FIG. 4d

EX1004, Figure 4d.

3. Eliashevich In Combination With Rabinzohn (“Eliashevich-Rabinzohn”)

71. As explained in Section VIII.A.1 [Eliashevich] and as shown in Figure 3E, Eliashevich discloses forming an LED having a non-vertical surface 170, utilizing a tapered side surface of a photoresist layer 167. Eliashevich describes the

tapered photoresist layer 167 being formed by “utilizing controlled processing ... of the photoresist” EX1003, 18:26-29. However, Eliashevich does not give details on the process of “controlled processing... of the photoresist” that causes the photoresist layer 167 to form a tapered shape. Eliashevich instead teaches that “[t]hese techniques are known in the art.” EX1003, 18:34-19:1.

Referring to FIGS. 3D-3F, mesa 164 is subjected to an etching process which removes some of the semiconductor material from the p-type layers 160. One preferred etching process includes a reactive ion etching (RIE) process. In other preferred methods, other forms of plasma etching are used, such as ICP. A photoresist material 167 is deposited on the top surface 166 of mesa 164 and is exposed and developed to form a mask 165 having openings 169. During etching, the walls 168 and a portion of the top surface 166 are attacked and semiconductor material is removed from the mesa 164 until a curved surface is obtained. Preferably, a portion of the top surface remains after etching, to be used for an upper electrode-pad unit, as discussed below. The mask may be given a tapered shape, as shown in FIG. 3D, ***utilizing controlled processing or baking of the photoresist and the relative etch rates for the photoresist and semiconductor materials may be tailored so as to form the curved surfaces on the mesa 164, at the upper end of the structure 110.*** The RIE etching removes the mask at an outside portion of the mesa first and then begins to remove semiconductor material from the p-type layers 160, as represented by the dashed lines in FIG. 3D. ***These techniques are known in the art.*** In other embodiments, conventional lithographic techniques may also be used. The radial surfaces on the mesa may also be formed utilizing an additive process, as discussed above. In embodiments in which the radial surfaces are formed in an additive process, transparent

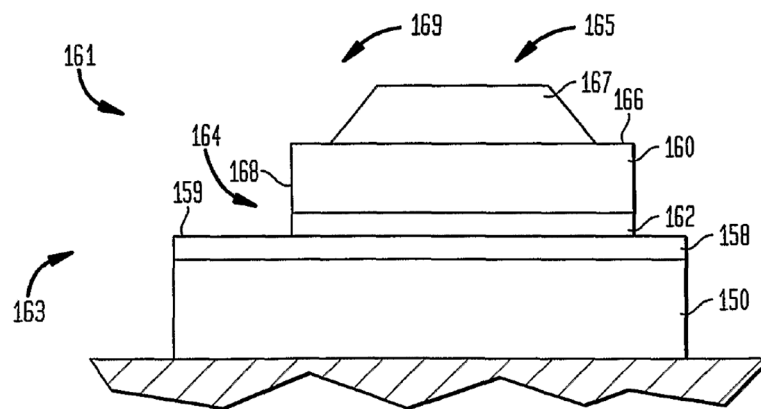
dielectric or polymeric material is deposited on the p-type layers

160.

EX1003, 18:14-19:7.

72. Accordingly, naturally, a POSITA would have looked into prior art to understand the details of the “controlled processing... of the photoresist.”

FIG. 3E



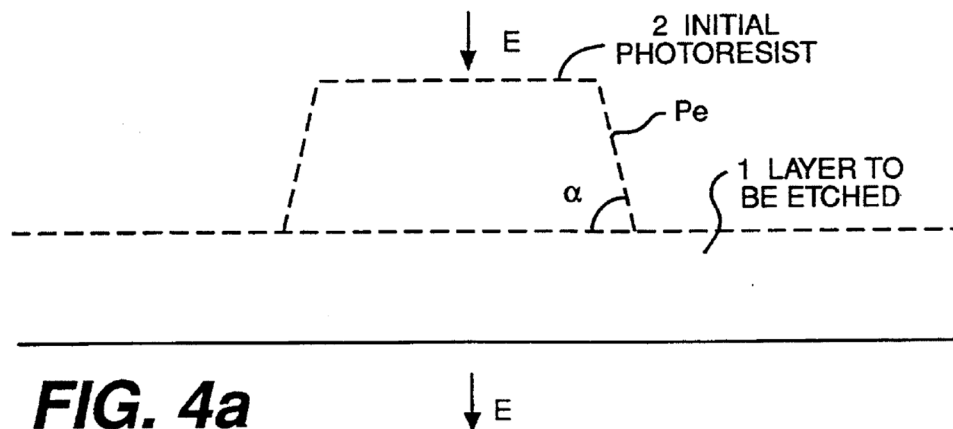
EX1003, Figure 3E.

73. As Eliashevich describes above, manufacturing a photoresist mask having a tapered surface using “controlled processing... of the photoresist” was well known in the art. EX1003, 18:26-19:1. Rabinzohn, for example, describes making a photoresist mask having sloped side surfaces, which are referred to as “flanks,” by carrying out “preetching.” In particular, Rabinzohn discloses that “in the case of FIG. 4, the initial masking photoresist layer 2, previously to the actual etching process, has been subjected to a *preetching stage*, the effect of which is to *generate etching flanks of slope Pe* inclined in relation to the free surface of the layer 1 to be

etched, assumed to be horizontal, the etching flanks of the initial masking photoresist layer 2 being thus *inclined at an angle α* in relation to the abovementioned free surface.” EX1004, 7:21-30.

Alternatively, in the case of FIG. 4, the initial masking photoresist layer 2, previously to the actual etching process, has been subjected to a preetching stage, the effect of which is to generate etching flanks of slope pe inclined in relation to the free surface of the layer 1 to be etched, assumed to be horizontal, the etching flanks of the initial masking photoresist layer 2 being thus inclined at an angle α in relation to the abovementioned free surface. It will be noted that the preetching process may consist of a mild etching, which has the property of selectively attacking the initial masking photoresist layer 2, excluding an attack alternatively layer 1 to be etched. On the, the initial masking photoresist layer 2 can be deposited and treated so as to exhibit etching flanks which have the slope pe as shown at point a) of FIG. 4.

EX1004, 7:21-36.

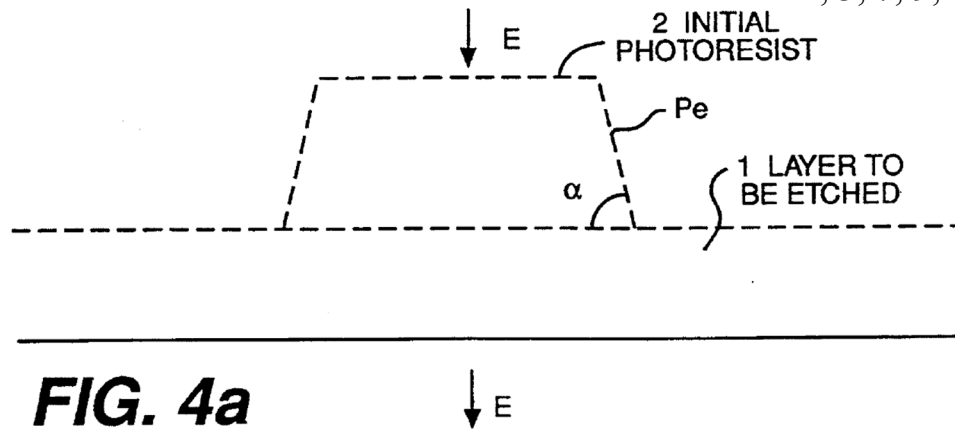


EX1004, Figure 4a.

74. As Rabinzohn explains, the “preetching” process is different from the “actual etching process” (i.e., the “reactive-ion etching process”) that etches the underlying layer 1, and the preetching process occurs before the actual etching process. EX1004, 7:21-27, 7:38-47, Figures 4b-4d. Unlike the “actual etching process,” the “preetching” process is mild and it does not etch the underlying layer 1. For example, Rabinzohn states that “[i]t will be noted that the *preetching process may consist of a mild etching*, which has the property of selectively attacking the initial masking photoresist layer 2, excluding an attack alternatively layer 1 to be etched.” EX1004, 7:30-33.

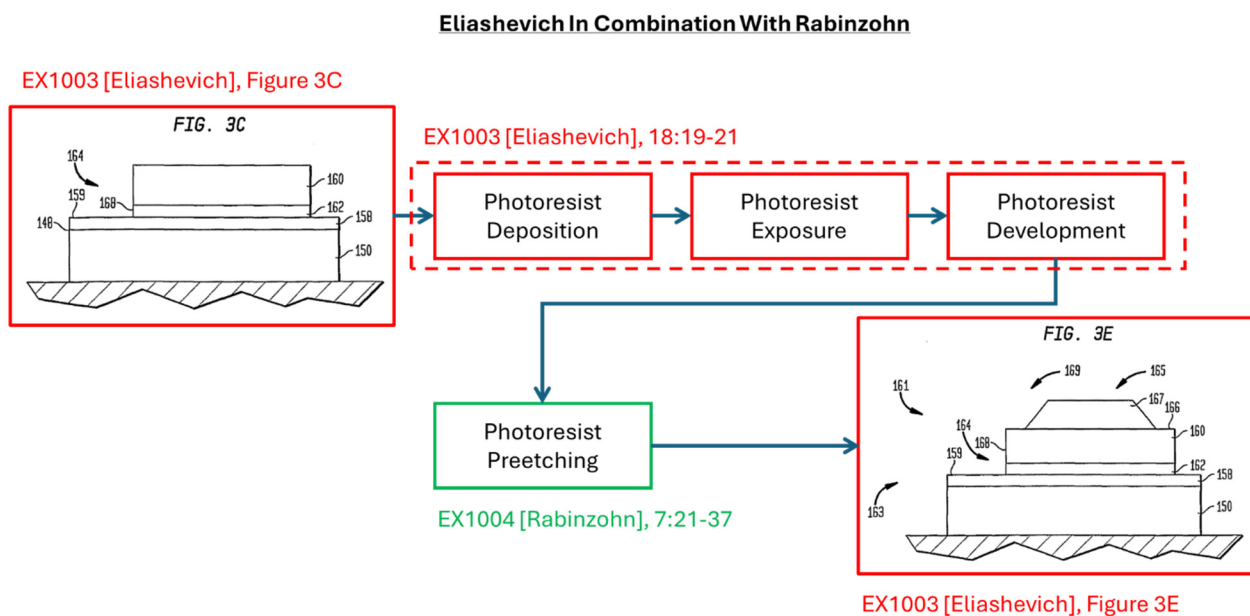
Alternatively, in the case of FIG. 4, the initial masking photoresist layer 2, previously to the actual etching process, has been subjected to a preetching stage, the effect of which is to generate etching flanks of slope α inclined in relation to the free surface of the layer 1 to be etched, assumed to be horizontal, the etching flanks of the initial masking photoresist layer 2 being thus inclined at an angle α in relation to the abovementioned free surface. *It will be noted that the preetching process may consist of a mild etching, which has the property of selectively attacking the initial masking photoresist layer 2, excluding an attack alternatively layer 1 to be etched.* On the, the initial masking photoresist layer 2 can be deposited and treated so as to exhibit etching flanks which have the slope α as shown at point a) of FIG. 4.

EX1004, 7:21-36.



EX1004, Figure 4a.

75. It would have been obvious to a POSITA to combine Eliashevich with Rabinzohn such that the photoresist of Eliashevich that has a tapered side surface is formed using Rabinzohn's preetching process. Illustrated below is the combined process:



**i. Reasons To Combine Eliashevich With Rabinzohn
With A Reasonable Expectation Of Success**

76. There would have been motivation by POSITA to combine Eliashevich with Rabinzohn in line with what was described above for at least two reasons. *First*, Eliashevich discloses forming a patterned photoresist with a tapered side surface through “controlled processing ... of the photoresist.” Eliashevich also includes suggestions that such controlled processing of the photoresist is well known in the prior art. EX1003, 18:26-29, 18:34-19:1.

Referring to FIGS. 3D-3F, mesa 164 is subjected to an etching process which removes some of the semiconductor material from the p-type layers 160. One preferred etching process includes a reactive ion etching (RIE) process. In other preferred methods, other forms of plasma etching are used, such as ICP. A photoresist material 167 is deposited on the top surface 166 of mesa 164 and is exposed and developed to form a mask 165 having openings 169. During etching, the walls 168 and a portion of the top surface 166 are attacked and semiconductor material is removed from the mesa 164 until a curved surface is obtained. Preferably, a portion of the top surface remains after etching, to be used for an upper electrode-pad unit, as discussed below. *The mask may be given a tapered shape, as shown in FIG. 3D, utilizing **controlled processing** or baking of the photoresist and the relative etch rates **for the photoresist** and semiconductor materials may be tailored so as to form the curved surfaces on the mesa 164, at the upper end of the structure 110.* The RIE etching removes the mask at an outside portion of the mesa first and then begins to remove semiconductor material from the p-type layers 160, as represented by the dashed lines in FIG. 3D. ***These techniques are known in the art.*** In other

embodiments, conventional lithographic techniques may also be used. The radial surfaces on the mesa may also be formed utilizing an additive process, as discussed above. In embodiments in which the radial surfaces are formed in an additive process, transparent dielectric or polymeric material is deposited on the p-type layers 160.

EX1003, 18:14-19:7.

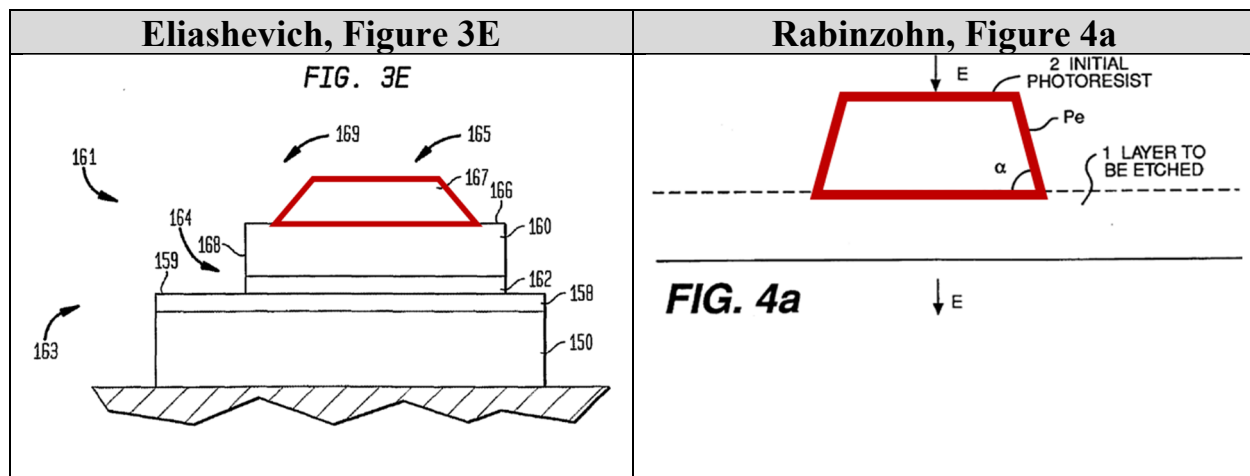
77. And as suggested by Eliashevich, such “controlled processing” is taught by Rabinzohn: Rabinzohn teaches a “preetching process” that forms a patterned photoresist with a tapered side surface. EX1004, 7:21-30, Figure 4a.

78. As such, the combination would have merely amounted to the combination would have merely amounted to carrying out Eliashevich’s manufacturing method with some of the details taught in Rabinzohn regarding how photoresist’s side surfaces can be tapered based on Eliashevich’s express suggestion that the patterned photoresist with a tapered side surface would be formed using the “controlled processing” of photoresist. EX1003, 18:26-29, 18:34-19:1, Figure 3E.

79. ***Second***, there would have been a motivation to use Rabinzohn’s preetching process to form “tapered” side surfaces on Eliashevich’s photoresist, because Rabinzohn’s preetching process forms a photoresist layer with nearly identical “sloped” side surfaces.

80. For example, Elishevich uses the “tapered” side surface on a patterned photoresist (as shown below in Figure 3E) to etch the semiconductor layer

underlying the photoresist, such that a non-vertical surface is formed on the underlying layer. EX1003, 18:14-35, Figure 3F. Similarly, Rabinzohn uses the sloped side surface on a patterned photoresist to etch the underlying semiconductor layer, such that a non-vertical surface is formed on the underlying layer. Rabinzohn's "sloped" photoresist has nearly the identical trapezoid shape as Rabinzohn's "tapered" photoresist. EX1004, 3:35-43, 4:1-13, 7:38-8:2, 8:62-68, Figures 4a, 4d. As such, it would have been readily understood by a POSITA that the preetching method as disclosed by Rabinzohn for making a "sloped" photoresist is easily applicable to the fabrication process disclosed by Eliashevich in making a "tapered" photoresist.



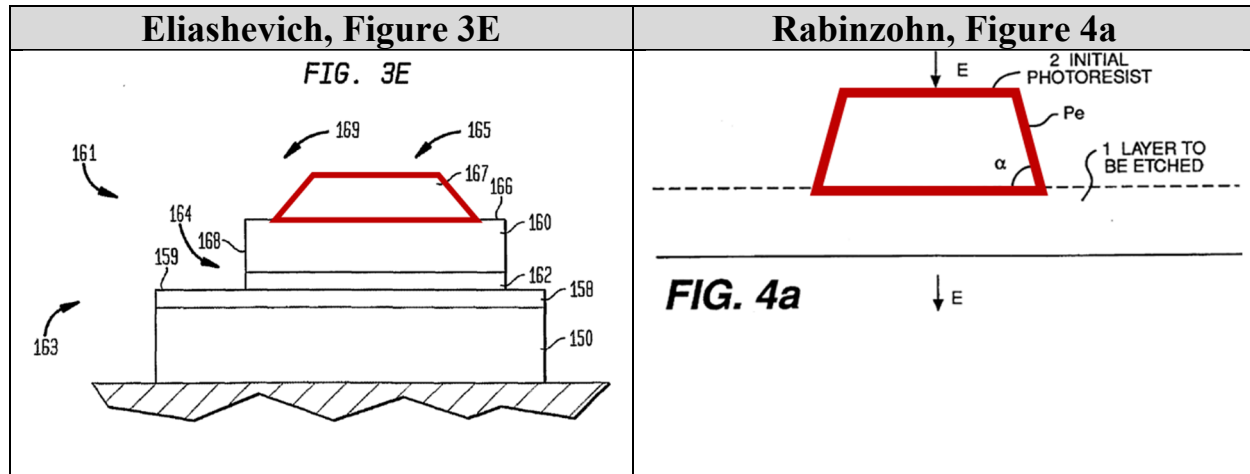
81. There would have been a reasonable expectation of success in making Eliashevich's photoresist with a tapered side surface using Rabinzohn's preetching method. **First**, Rabinzohn's preetching method is compatible with Eliashevich's

method. Rabinzohn and Eliashevich both disclose applying the sloped/tapered photoresist for etching the underlying semiconductor layer such that a non-vertical side surface is formed on the underlying layer. *See, e.g.,* EX1003, 18:14-35; EX1004, 3:35-43, 4:1-13, 7:38-8:2, 10:62-68, Figure 4d. As such, it would have been readily understood by a POSITA that Eliashevich's method of manufacturing sloped photoresists is compatible with and able to use Rabinzohn's preetching process.

82. ***Second***, it would have been readily understood by a POSITA that the subsequent dry-etching process to etch the underlying layer is not impacted by the particulars of the process of forming the tapered photoresist. Put another way, the subsequent dry-etching process is largely independent from the process of forming the tapered photoresist. A POSITA would have understood that the shape of the photoresist is what is important, rather than how the shape is formed. As such, there would have been a reasonable expectation of success in applying the preetching process of Rabinzohn as part of the manufacturing method disclosed by Eliashevich of making sloped LEDs.

83. ***Third***, a POSITA would have understood that the combination merely amounts to a simple application of the preetching process disclosed by Rabinzohn for making a sloped photoresist to create the tapered photoresist disclosed by Eliashevich to obtain predictable results of making a tapered/sloped etching mask

pattern, which is used in etching semiconductor layers under the photoresist. The process of Eliashevich and the process of Rabinzohn both form substantially similar sloped side surfaces on the photoresist etching mask pattern. Compare EX1003, Figure 3E with EX1004, Figure 4a.



84. At least, a POSITA would have found it obvious to try to apply Rabinzohn's preetching process to manufacture the tapered photoresist 167 of Eliashevich. As discussed above, Eliashevich does not teach the specifics of the controlled process of forming the tapered photoresist mask. Accordingly, a design need was present to determine a controlled process that would form the tapered photoresist. Further, it would have been readily understood that the preetching of Rabinzohn is one of the "controlled processes" that would provide for a photoresist mask that is tapered. As such, a POSITA would have found it to be common sense to at least try Rabinzohn's method to create the tapered photoresist layer of

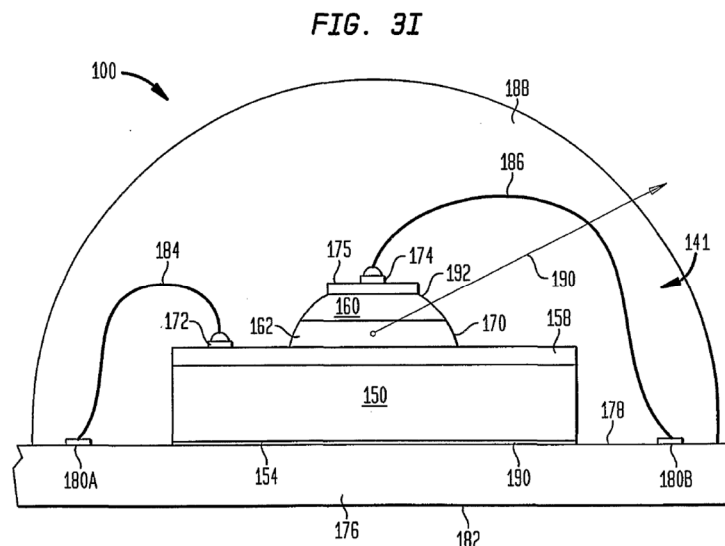
Eliashevich, and there would have been a reasonable expectation of success as described above.

1. Claim 1

i. [1Pre] A method of manufacturing a light emitting device, comprising:

85. Eliashevich teaches preamble [1Pre].

86. Eliashevich teaches “*methods of making light emitting diodes and light-emitting diode packages* having optimized light extraction characteristics, and methods of making the foregoing.” EX1003, 1:2-7. *See also* EX1003, Figures 3A-3I.



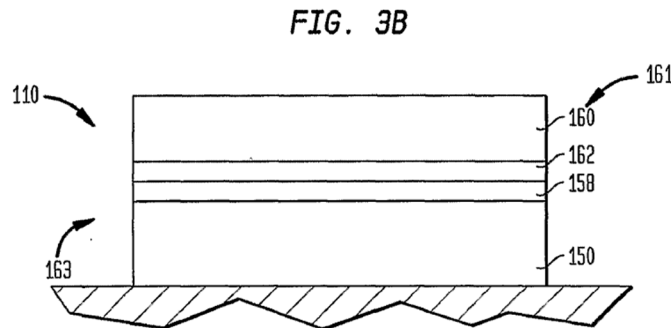
EX1003, Figure 3I.

- ii. [1A] sequentially forming an N-type semiconductor layer, active layer, and P-type semiconductor layer on a substrate;

87. Eliashevich teaches [1A]. A “substrate 150” is provided by the LED manufacturing process of Eliashevich. EX1003, 14:14-15, Figure 3A. Next, “one or more n-type layers 158 are deposited on the first surface 152 of substrate 150.” EX1003, 14:25-26. Then, “[o]ne or more p-type layers 160 having a top surface 166 are deposited over the n-type layers 158. A junction is also formed between the n-type layers 158 and p-type layers 160.” EX1003, 14:29-32.

FIGS. 3A-3J show a method of making an optoelectronic device package in accordance with one embodiment of the invention. A substrate 150, as shown in FIG. 3A, is provided on a support 149. The substrate 150 has a first, upwardly facing surface 152 and a second surface 154 facing in a direction opposite from the first surface 152. In certain preferred embodiments, the substrate 150 is a substantially transparent substrate. The substrate may comprise a sapphire substrate. The substrate may also comprise GaN, AlN, ZnO, SiC, or LiGaO. A semiconductor structure 110 comprising a stacked structure of semiconductor layers is formed on the substrate 150. A semiconductor material having a first conductivity type is deposited on the first surface 152 of the substrate 150. For example, one or more n-type layers 158 are deposited on the first surface 152 of substrate 150. A semiconductor material having a second conductivity type is deposited over the semiconductor material of the first conductivity type. *One or more p-type layers 160 having a top surface 166 are deposited over the n-type layers 158. A junction is also formed between the n-type layers 158 and p-type layers 160.*

EX1003, 14:12-32.



EX1003, Figure 3B.

88. “The junction is shown schematically in FIG. 3B as a *discrete layer* interposed between the layers 158 and 160. In practice, the *junction* may comprise ... *one* or more *intermediate layers*.” EX1003, 15:2-6. *See also* EX1003, 15:7-13. As such, it would have been understood by a POSITA that the following layers are deposited on a substrate 150 sequentially in this specific order: the *n-type layer* 158, the junction layer 162, and the *p-type layer* 160, as shown in Figure 3B.

The stacked structure 110 of FIGs. 3A-3J comprises a structure the embodiment shown in for an LED, including a junction 162 between the n-type layers 158 and p-type layers 160. *The junction is shown schematically in FIG. 3B as a discrete layer interposed between the layers 158 and 160. In practice, the junction may comprise the border between directly abutting p-type and n-type layers, or one or more intermediate layers.* The intermediate layers may have any conductivity type or no

conductivity type. Alternatively, the junction may include additional structures inbetween the p-type layers 160 and n-type layers 158 or in an intermediate region. Thus, the junction may be a simple homojunction; a single heterojunction, a double heterojunction, a single quantum well, a multiple quantum well or any other type of junction structure. A person of ordinary skill in the art will appreciate that the semiconductor structure may incorporate various layers of semiconductor materials, as well as other structures used in the optoelectronic arts.

EX1003, 14:33-15:16.

89. The claimed “N-type semiconductor layer” and “P-type semiconductor layer” are the n-type layer and p-type layer in Eliashevich, respectively, because both the n-type layer and p-type layer include semiconductor materials in a “semiconductor structure.” For example, Eliashevich states:

A semiconductor structure 110 comprising a stacked structure of semiconductor layers is formed on the substrate 150. A *semiconductor material having a first conductivity type* is deposited on the first surface 152 of the substrate 150. For example, *one or more n-type layers 158* are deposited on the first surface 152 of substrate 150. *A semiconductor material having a second conductivity type* is deposited over the semiconductor material of the first conductivity type.

EX1003, 14:21-30.

90. Further, the claimed “active layer” is disclosed by the junction layer in Eliashevich, for the following reasons: (1) light is generated by the junction layer just like the active layer of the '626 Patent (EX1003, 5:26-27, 23:18-21; EX1001, 6:24-27), (2) both the junction layer and the active layer of the '626 Patent can be a

quantum well (EX1003, 5:10-13; EX1001, 6:22-24), and (3) the **junction layer** is sandwiched between a **p-type layer** and an **n-type layer**, just like the **active layer** of the '626 Patent (EX1003, 4:3-5, 14:29-32, Figure 3B; EX1001, 6:39-43, 8:32-39, Figures 3, 6).

- iii. [1B] forming an **etching mask pattern**, of which a side surface is not perpendicular to but inclined at a slope from a horizontal plane, on the **P-type semiconductor layer**; and
[1D-1] wherein forming the **etching mask pattern** comprises: forming a **photoresist** on the **P-type semiconductor layer**;
[1D-2] exposing the **photoresist** to light; and
[1D-3] developing the light-exposed photoresist without a baking process after the light exposure.

91. Eliashevich-Rabinzohn discloses [1B], [1D-1] through [1D-3].

a. [1B] “forming an **etching mask pattern**”

92. Eliashevich-Rabinzohn teaches “forming an **etching mask pattern**.”

Indeed, as shown below in Figure 3E, Eliashevich discloses manufacturing a patterned photoresist 167 with a “tapered shape.” EX1003, 18:14-16, 18:26-31.

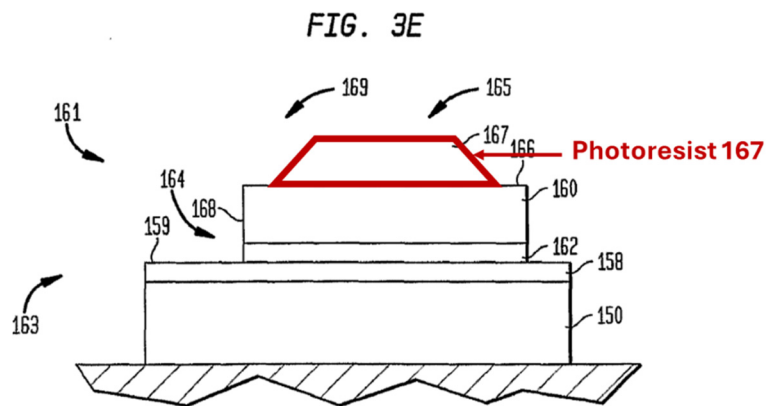
It should be appreciated that the figures are not drawn to scale. In particular, the thicknesses of the various layers have been greatly exaggerated for clarity of illustration. Typically, the entire stack including mesa 164 is on the order of five microns thick. The horizontal dimensions, such as the overall width and length are on the order of a few hundred microns as, for example, about 200-300 microns. Although FIGs. 3A-3J show a structure 110 having a single mesa 164 for a single LED device, typically

a structure 110 is formed as a wafer for a plurality of devices. Thus, a plurality of mesas 164 would be formed in a grid on the wafer and the following steps are performed for each device to be formed.

Referring to FIGS. 3D-3F, mesa 164 is subjected to an etching process which removes some of the semiconductor material from the p-type layers 160. One preferred etching process includes a reactive ion etching (RIE) process. In other preferred methods, other forms of plasma etching are used, such as ICP. A photoresist material 167 is deposited on the top surface 166 of mesa 164 and is exposed and developed to form a mask 165 having openings 169. During etching, the walls 168 and a portion of the top surface 166 are attacked and semiconductor material is removed from the mesa 164 until a curved surface is obtained. Preferably, a portion of the top surface remains after etching, to be used for an upper electrode-pad unit, as discussed below. ***The mask may be given a tapered shape, as shown in FIG. 3D, utilizing controlled processing or baking of the photoresist and the relative etch rates for the photoresist and semiconductor materials may be tailored so as to form the curved surfaces on the mesa 164, at the upper end of the structure 110.*** The RIE etching removes the mask at an outside portion of the mesa first and then begins to remove semiconductor material from the p-type layers 160, as represented by the dashed lines in FIG. 3D. These techniques are known in the art. In other embodiments, conventional lithographic techniques may also be used. The radial surfaces on the mesa may also be formed utilizing an additive process, as discussed above. In embodiments in which the radial surfaces are formed in an additive process, transparent dielectric or polymeric material is deposited on the p-type layers 160.

EX1003, 18:1-19:7.

93. Because the patterned photoresist 167 is then used to mask the p-type semiconductor layer from dry-etching, the patterned photoresist 167 is an “**etching mask pattern.**” EX1003, 18:14-24, 18:31-35, Figures 3D, 3F. *See also* Section VIII.A.1.iv [Ground I, 1C].



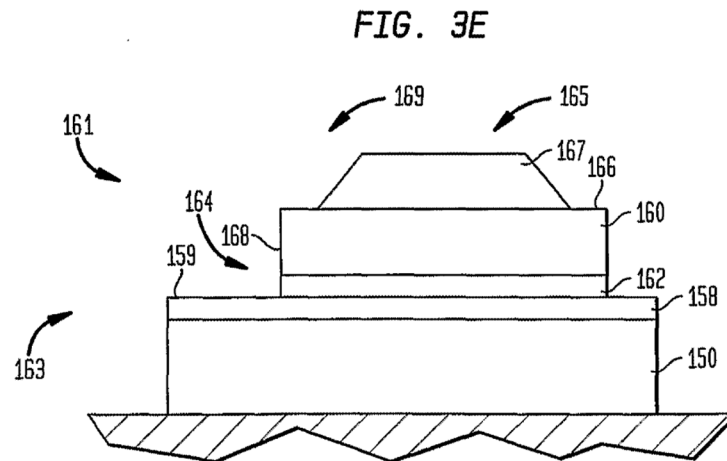
EX1003, Figure 3E.

94. As explained below, all the details recited in [1D-1] through [1D-3] are further rendered obvious by Eliashevich in combination with Rabinzohn.

(a) [1D-1] “forming a photoresist on the P-type semiconductor layer”

95. Eliashevich teaches depositing “[a] **photoresist material 167** ... on the top surface 166 of mesa 164.” EX1003, 18:19-20. The top layer of mesa 164 is a “**p-type layer 160,**” as explained in Section VIII.A.1.ii [Ground I, 1A]. EX1003, 14:29-32, Figure 3B. Figure 3E indeed shows that the **photoresist material 167** is arranged on top the **p-type layer 160**. Accordingly, depositing (i.e., the claimed

“forming”) a **photoresist material 167** (i.e., the claimed “**photoresist**”) on the **p-type layer 160** is taught by Eliashevich.



EX1003, Figure 3E.

(b) [1D-2] “exposing the **photoresist** to light;”

96. Eliashevich discloses “[a] **photoresist material 167** is deposited on the top surface 166 of mesa 164 and is **exposed** and developed to form a mask 165 having openings 169.” EX1003, 18:19-21.

97. It would have been understood by a POSITA that Eliashevich teaches exposing the **photoresist material 167** to light, because selectively patterning a **photoresist material**—where the prefix “photo” means “light” (EX1017, 3)—by exposing it to **light** was well known. See Section IV.B [Photolithography]; EX1014, 1-4, 7-9.

(c) [1D-3] “developing the light-exposed photoresist without a baking process after the light exposure.”

98. **First**, Eliashevich teaches “**developing the light-exposed photoresist.**”

Eliashevich’s photoresist is “light-exposed” as explained in Section VIII.A.1.iii.a(b)

[Ground I, 1D-2]. In addition, Eliashevich discloses that “[a] **photoresist material**

167 ... is **exposed and developed** to form a mask **165** having openings **169.**”

EX1003, 18:19-21.

Referring to FIGS. 3D-3F, mesa 164 is subjected to an etching process which removes some of the semiconductor material from the p-type layers 160. One preferred etching process includes a reactive ion etching (RIE) process. In other preferred methods, other forms of plasma etching are used, such as ICP. ***A photoresist material 167 is deposited on the top surface 166 of mesa 164 and is exposed and developed to form a mask 165 having openings 169.*** During etching, the walls 168 and a portion of the top surface 166 are attacked and semiconductor material is removed from the mesa 164 until a curved surface is obtained. Preferably, a portion of the top surface remains after etching, to be used for an upper electrode-pad unit, as discussed below. The mask may be given a tapered shape, as shown in FIG. 3D, utilizing controlled processing or baking of the photoresist and the relative etch rates for the photoresist and semiconductor materials may be tailored so as to form the curved surfaces on the mesa 164, at the upper end of the structure 110. The RIE etching removes the mask at an outside portion of the mesa first and then begins to remove semiconductor material from the p-type layers 160, as represented by the dashed lines in FIG. 3D. These techniques are known in the art. In other embodiments, conventional lithographic techniques may also be

used. The radial surfaces on the mesa may also be formed utilizing an additive process, as discussed above. In embodiments in which the radial surfaces are formed in an additive process, transparent dielectric or polymeric material is deposited on the p-type layers 160.

EX1003, 18:14-19:7.

99. *Second*, Eliashevich combined with Rabinzohn renders obvious that the **light-exposed photoresist** is developed “without a baking process after the light exposure.” Eliashevich and Rabinzohn are both silent on baking the photoresist after the light exposure. For instance, in Eliashevich, the exposed photoresist is developed without mentioning that the photoresist is subject to any baking after the light exposure: it just says that “[a] **photoresist material 167** ... is *exposed and developed*.” EX1003, 18:19-21; see also EX1003, 18:14-19:16. Likewise, in Rabinzohn, the exposed photoresist is developed without mentioning that the photoresist is being subject to any baking. EX1004, 7:21-37.

Alternatively, in the case of FIG. 4, the initial masking photoresist layer 2, previously to the actual etching process, has been subjected to a preetching stage, the effect of which is to generate etching flanks of slope α inclined in relation to the free surface of the layer 1 to be etched, assumed to be horizontal, the etching flanks of the initial masking photoresist layer 2 being thus inclined at an angle α in relation to the abovementioned free surface. It will be noted that the preetching process may consist of a mild etching, which has the property of selectively attacking the initial masking photoresist layer 2, excluding an attack alternatively layer 1 to be etched. On the, the initial masking photoresist layer 2 can be deposited and treated so as to exhibit

etching flanks which have the slope peas shown at point a) of

FIG. 4.

EX1004, 7:21-37.

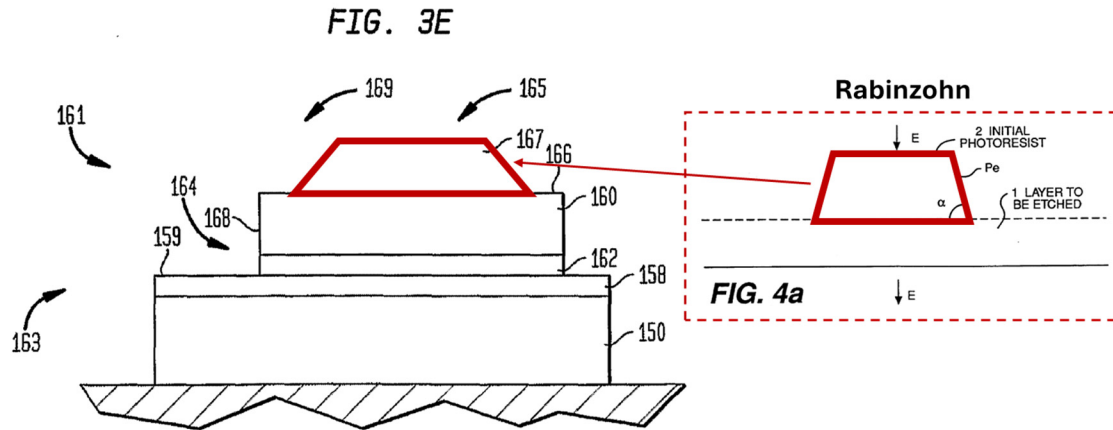
100. Further, the combination of Eliashevich-Rabinzohn does not rely on baking to form the inclined photoresist layer. Instead, the Eliashevich-Rabinzohn combination relies on the “controlled processing” taught by Eliashevich, which is implemented in this combination as the preetching process disclosed by Rabinzohn. *See* Section VIII.A.3 [Eliashevich-Rabinzohn].

(d) [1B] “forming an etching mask pattern, of which a side surface is not perpendicular to but inclined at a slope from a horizontal plane, on the P-type semiconductor layer”

101. The combination of Eliashevich-Rabinzohn also renders obvious forming the patterned photoresist 167 (claimed as the “etching mask pattern”) on a p-type layer 160, which is shown in Figure 3E of Eliashevich. EX1003, 18:26-31, Figure 3E. *See also* Section VIII.A.1.ii [Ground I, 1A]; EX1003, 14:21-30.

102. Further, the side surface of the patterned photoresist 167 being not perpendicular to but inclined at a slope from a horizontal plane is also rendered obvious by Eliashevich-Rabinzohn, as shown by the patterned photoresist 167 with the sloped side surface in Eliashevich’s Figure 3E and disclosed by Figure 4a and the preetching process in Rabinzohn. EX1003, 18:26-31, Figure 3E; EX1004, 7:21-37, Figure 4a.

Eliashevich In Combination With Rabinzohn



EX1003, Figure 3E; EX1004, Figure 4a.

- iv. [1C] removing the **etching mask pattern** and the **P-type semiconductor layer** exposed through the **etching mask pattern**;

103. Eliashevich teaches [9C].

104. **First**, Eliashevich discloses “removing the **etching mask pattern**.”

Eliashevich discloses that “[o]ne preferred etching process includes a reactive ion etching (RIE) process” and “[t]he **RIE etching removes the mask**” formed by the **patterned photoresist 167**. EX1003, 18:16-17, 31-34, Figures 3E and 3F (showing no photoresist 167).

Referring to FIGS. 3D-3F, mesa 164 is subjected to an etching process which removes some of the semiconductor material from the p-type layers 160. **One preferred etching process includes a reactive ion etching (RIE) process.** In other preferred methods, other forms of plasma etching are used, such as ICP. A photoresist material 167 is deposited on the top surface 166 of mesa 164 and is exposed and developed to form a mask 165

having openings 169. During etching, the walls 168 and a portion of the top surface 166 are attacked and semiconductor material is removed from the mesa 164 until a curved surface is obtained. Preferably, a portion of the top surface remains after etching, to be used for an upper electrode-pad unit, as discussed below. The mask may be given a tapered shape, as shown in FIG. 3D, utilizing controlled processing or baking of the photoresist and the relative etch rates for the photoresist and semiconductor materials may be tailored so as to form the curved surfaces on the mesa 164, at the upper end of the structure 110. ***The RIE etching removes the mask at an outside portion of the mesa first and then begins to remove semiconductor material from the p-type layers 160, as represented by the dashed lines in FIG. 3D.*** These techniques are known in the art. In other embodiments, conventional lithographic techniques may also be used. The radial surfaces on the mesa may also be formed utilizing an additive process, as discussed above. In embodiments in which the radial surfaces are formed in an additive process, transparent dielectric or polymeric material is deposited on the p-type layers 160.

EX1003, 18:1-19:7.

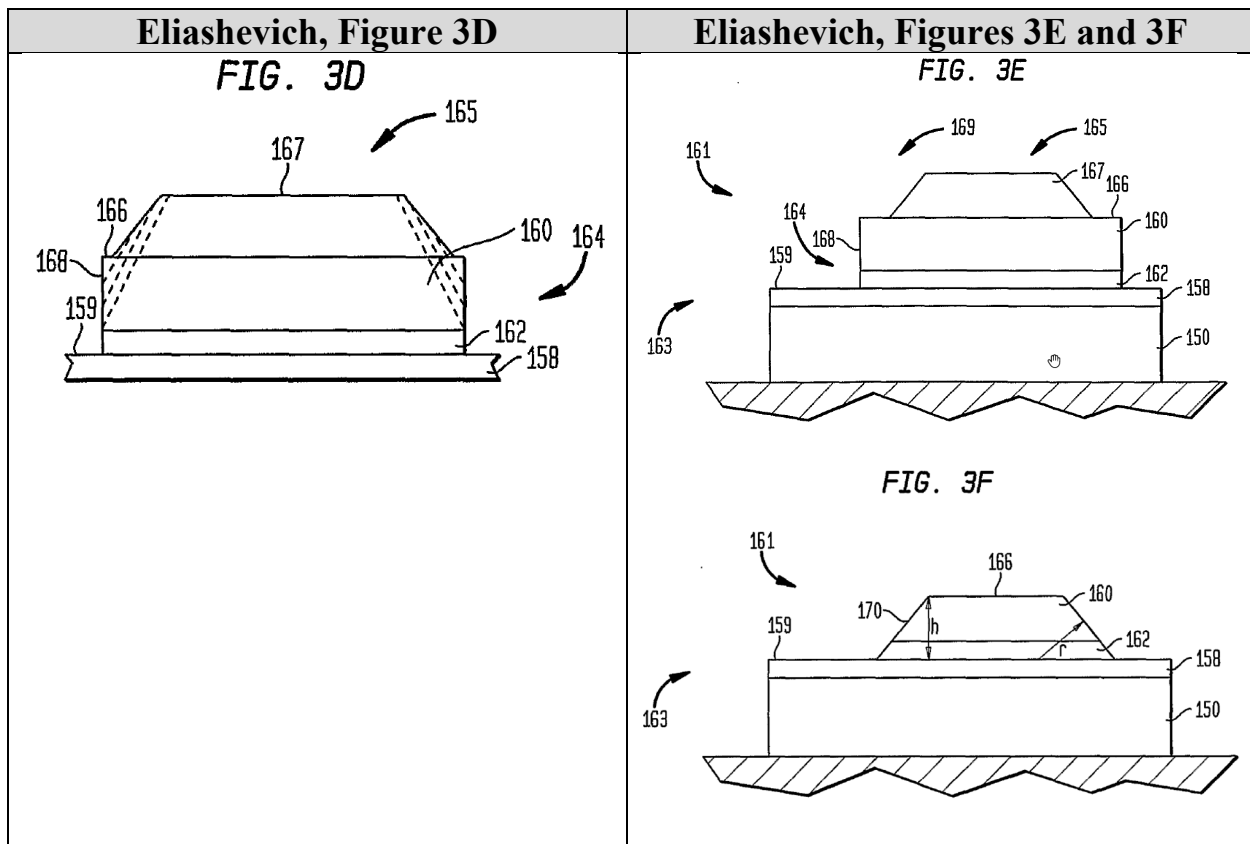
105. ***Second***, Eliashevich discloses that “mesa 164 is subjected to an ***etching process*** which ***removes*** some of the semiconductor material from the ***p-type layers 160***.” EX1003, 18:14-31. In particular, “[t]he RIE etching removes the mask at an outside portion of the mesa first and then begins to ***remove semiconductor material from the p-type layers 160***, as represented by the dashed lines in FIG. 3D.” EX1003, 18:31-35. The ***p-type layer 160*** removed by the etching process is the portion “exposed through the ***etching mask pattern***.” As explained by Eliashevich, the

photoresist material 167 is developed to “form a mask having *openings 169*,” as shown in Figure 3E. Further, the etching process “removes the mask at an outside portion of the mesa first and then begins to *remove semiconductor material from the p-type layers 160, as represented by the dashed lines in FIG. 3D*,” which is the material exposed through the etching mask pattern. EX1003, 18:31-34. Accordingly, the portion of “*p-type layer 160*” that is exposed through the photoresist mask 167 is removed by the etching process. *See also* EX1003, 19:8-10 (“The etching process forms one or more radial surfaces 170 extending between top surface 166 and n-type layers 158 as shown in FIG. 3F.”).

Referring to FIGS. 3D-3F, mesa 164 is subjected to an etching process which removes some of the semiconductor material from the p-type layers 160. One preferred etching process includes a reactive ion etching (RIE) process. In other preferred methods, other forms of plasma etching are used, such as ICP. A photoresist material 167 is deposited on the top surface 166 of mesa 164 and is exposed and developed to form a mask 165 having openings 169. *During etching, the walls 168 and a portion of the top surface 166 are attacked and semiconductor material is removed from the mesa 164 until a curved surface is obtained.* Preferably, a portion of the top surface remains after etching, to be used for an upper electrode-pad unit, as discussed below. The mask may be given a tapered shape, as shown in FIG. 3D, utilizing controlled processing or baking of the photoresist and the relative etch rates for the photoresist and semiconductor materials may be tailored so as to form the curved surfaces on the mesa 164, at the upper end of the structure 110. *The RIE etching removes the mask at an outside portion of the*

mesa first and then begins to remove semiconductor material from the p-type layers 160, as represented by the dashed lines in FIG. 3D. These techniques are known in the art. In other embodiments, conventional lithographic techniques may also be used. The radial surfaces on the mesa may also be formed utilizing an additive process, as discussed above. In embodiments in which the radial surfaces are formed in an additive process, transparent dielectric or polymeric material is deposited on the p-type layers 160.

EX1003, 18:1-19:7.

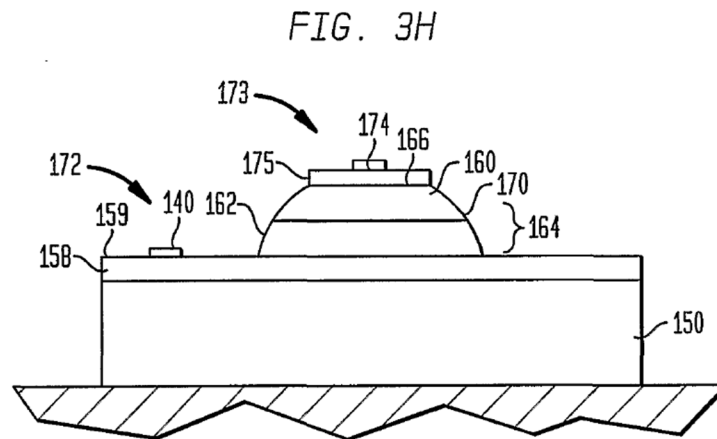


2. Claim 3

- i. [3] The method as claimed in claim 1, further comprising the step of flip-chip bonding the substrate onto an additional submount substrate after the step of removing the P-type semiconductor layer and the etching mask pattern.

106. The combination of Eliashevich-Rabinzohn renders obvious [3]. Eliashevich discloses that the process described in Figures 3A-3H can be used to manufacture the LED chip, which can be used to form an LED device by flipping and mounting the LED chip on another substrate.

107. As an example, to make the LED chip shown in Figure 3H, Eliashevich deposits electrodes 172 and 173 after forming a non-vertical surface by etching the mesa as shown in Figure 3F. EX1003, 19:26-33.



EX1003, Figure 3H.

108. Then, as shown in Figure 8 below, Eliashevich teaches that the LED shown in Figure 3H is flipped and bonded on another substrate. EX1003, 28:12-30.

As an example, in Figure 8, Eliashevich shows “a semiconductor structure [610] comprising a stacked structure of p-type, n-type and other semiconductor materials for generating light” (EX1003, 28:16-19) and “a sapphire substrate 650” (EX1003, 28:15-16).

Another type of package 600 utilizing a non-transparent electrode is shown in FIG. 8. The structure 610 has a substantially transparent back face 654 through which light will be directed. *For example, the transparent back face may comprise a sapphire substrate 650. The structure 610 is a semiconductor structure comprising a stacked structure of p-type, n-type and other semiconductor materials for generating light, as discussed above.* The structure 610 has a mesa 664 protruding from the structure and a lower surface 659. In the embodiment shown in Fig. 8, the mesa 664 has side surfaces with radial surfaces 670. In other preferred embodiments, the back face 654 incorporates a plurality of microlenses as shown in Fig. 5, and/or radial surfaces extending between the side surfaces of the substrate 650 and the back face 654.

EX1003, 28:12-25.

109. As identified by 633, 634, 638, and 641 in Figure 8, the “[s]tructure 610 [including the sapphire substrate 650] is **bonded** to the contacts of **second substrate 676** by, for example, disposing masses 686 and 684 of bonding material between each of the pads and contacts.” EX1003, 28:26-29:1, Figure 8.

An upper electrode-pad unit 675 is mounted on the mesa 664 and has a first pad 634. A lower electrode-pad unit 672 is mounted on the lower surface 659 and has a second pad 641. The first pad 634 and second pad 641 are connected to a first contact 638 and

second contact 633 on a second substrate 676. The structure 610 may be formed as discussed above, using either a subtractive or an additive process. ***Structure 610 is bonded to the contacts of second substrate 676 by, for example, disposing masses 686 and 684 of bonding material between each of the pads and contacts.*** The contacts are also connected to an electrical power source. Thus, light generated by this device is directed out the back face 654 and a transparent electrode for upper electrode pad unit is not necessary. At least some light rays generated at the junction 662 will be directed towards the mesa 664. Mesa 664 has at least one curved surface 670 for extracting light from the LED. A reflector mounted within the package 600 may be used to direct light emitted at surface 670 towards the back surface 654, if desired.

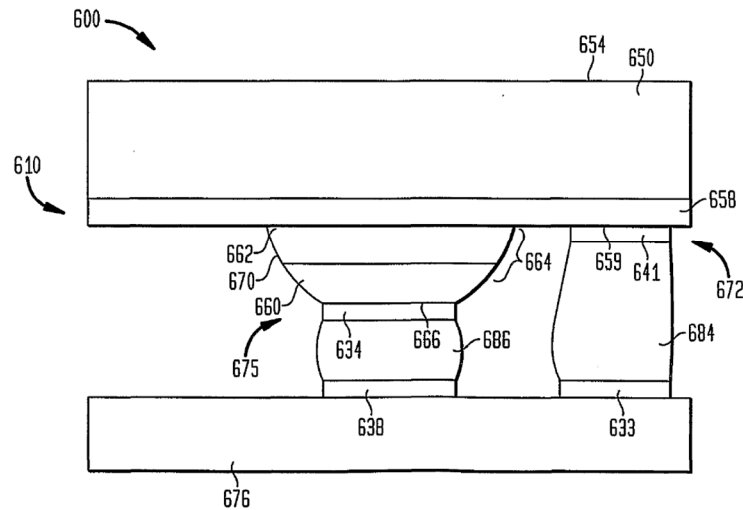
EX1003, 28:26-29:10.

110. *See also* EX1003, 34:10-12.

20. The package as claimed in claim 18, wherein said device is mounted to said second substrate so that said first substrate is adjacent said second substrate.

111. Bonding the structure 610 to the underlying substrate 676 would have needed the structure 610 to be flipped before bonding as shown in Figure 8.

FIG. 8



EX1003, Figure 8.

112. One example of the semiconductor structure 610 would have been understood by a POSITA to be the LED of Figure 3H, because the components in the semiconductor structure 610 and the components in the LED of Figure 3H are substantially similar. Indeed, Eliashevich claims a device package that includes an “optoelectronic device of claim 1” as taught in Figure 3H and “a second substrate” as taught in Figure 8. EX1003, 33:35-34:8.

18. An optoelectronic device package, comprising:

- (a) the *optoelectronic device of claim 1*;
- (b) a *second substrate* having a first conductive pad and a second conductive pad for *supporting said optoelectronic device*; and
- (c) conductive features connecting said first electrode-pad unit to said first conductive pad and said second electrode-pad unit to said second conductive pad.

EX1003, 33:35-34:8.

113. As such, “the step of removing the P-type semiconductor layer and the etching mask pattern” as shown in Figures 3D-3F would already have been performed when the semiconductor structure 610 is flipped and bonded to the second substrate 676. *See* Section VIII.A.1.iv [Ground I, 1C].

114. Accordingly, Eliashevich-Rabinzohn satisfies “the step of flip-chip bonding the substrate [sapphire substrate 650 of structure 610, corresponding to substrate 150 in Figure 3H] onto an additional submount substrate [second substrate 676] after the step of removing the P-type semiconductor layer and the etching mask pattern” as described in Figures 3D-3F.

B. Ground II: Eliashevich In Combination With Rabinzohn And Yoo Renders Obvious Claim 7.

1. Claim 7

- i. [7] The method as claimed in claim 1, wherein the photoresist with a thickness of 3 to 50 μm is used in the forming the etching mask pattern.

115. Eliashevich in combination with Rabinzohn and Yoo (“Eliashevich-Rabinzohn-Yoo”) renders obvious [7].

116. Eliashevich teaches forming the patterned photoresist layer (the claimed etching mask pattern) by depositing “[a] photoresist material 167 ... on the top surface 166 of mesa 164.” EX1003, 18:19-21. While Eliashevich does not state the thickness for the photoresist material 167, Eliashevich suggests that the deposited

photoresist is preferably thick. For example, Eliashevich discloses that the photoresist material 167 is used to shield the top surface 166 of the mesa 164 during etching and (2) “[p]referably, a portion of the top surface [of the mesa] *remains* after etching, to be used for an upper electrode-pad unit.” EX1003, 18:21-26. So it would have been understood by a POSITA that the photoresist layer is preferred to be thick, because otherwise, the photoresist layer would be completely removed by the etching step, as would the top surface 166 of the mesa 164.

117. In LED manufacturing, it was common to use a thick photoresist layer. For example, Yoo teaches using a 10-micron thick photoresist for LED manufacturing. EX1005, [0036]. In particular, Yoo teaches using dry-etching—specifically reactive ion etching (RIE)—to selectively etch LEDs’ layers. EX1005, Abstract, [0032], [0035]. To protect the LED structure against RIE’s intense plasma, Yoo teaches using a thick photoresist. EX1005, [0035]. Specifically, Yoo discloses that the thickness of the photoresist is “beneficially ... 10 microns.” EX1005, [0036] (“In the illustrated example, the photo-resist is beneficially spin coated to a thickness of about *10 microns*.”).

[0036] In the illustrated example, *the photo-resist is beneficially spin coated to a thickness of about 10 microns*. However, in general, the photo-resist thickness should be about the same as the thickness of the vertical topology GaN-based LED layer structure 120 plus the etch depth into the sapphire substrate 122. This helps ensure that the photoresist mask remains intact during

etching. Because it is difficult to form a thick photo-resist coating in one step, the photo-resist is beneficially applied in two coats, each about 5 microns thick. The first photo-resist coat is spin coated on and then soft baked at approximately 90 F. for about 15 minutes. Then, the second photo-resist coat is applied in a similar manner, but is soft baked at approximately 110 F. for about 8 minutes. The photo-resist coating is then patterned to form the scribe lines. This is beneficially performed using lithographic techniques and development. Development takes a relatively long time because of the thickness of the photo-resist coating. After development, the photo-resist pattern is hard baked at about 80 F. for about 30 minutes. Then, the hard baked photo-resist is beneficially dipped in a MCB (Metal Chlorobenzene) treatment for about 3.5 minutes. Such dipping further hardens the photo-resist.

EX1005, [0036].

118. It would have been obvious to combine Eliashevich-Rabinzohn with Yoo to form the **photoresist 167** of Eliashevich to be **10 microns thick** as taught by Yoo. **First**, using a thick photoresist, like the 10-micron thick photoresist taught by Yoo, is motivated by Eliashevich itself. *See* EX1003, 18:24-26. Further, it was common to use a **thick photoresist** (such as a **10-micron thick photoresist**) in LED manufacturing, and in fact, it was common to use such thick photoresist to form a **photoresist layer** with a sloped side surface (as in Eliashevich-Rabinzohn). *See also* EX1007, Title (“Semiconductor **Light Emitting Device** And Manufacturing Method Thereof”); [0085] (“As to the **resist layer 130** having a thickness of **approximately 10 μ m**, it is possible to form the **inclined resist layer 130 without problem.**”).

[0085] In the foregoing method for forming the resist layer 130, a contact exposure method (hard contact) is used. Thus, the pattern transfer precision of the photomask 131 is high, and a pattern is not misaligned during the exposure. A nitride semiconductor wafer laminated on a different type of substrate (sapphire) is slightly warped convexly or concavely because of difference in lattice constants (Δa) and difference in thermal expansion coefficients. However, warpage is corrected by pressing the photomask, so that the misalignment of the pattern does not occur. Furthermore, in contrast to a method with an apart photomask, the misalignment of the inclination angle due to exposure intensity and time does not occur. Furthermore, it is possible to form the inclination angle of the end portions of the resist layer with high reproducibility by only selecting the post bake condition. If the resist layer 130 is thick, the inclination angle depends on only the temperature and time of the post bake. Thus, the condition can be easily set. ***As to the resist layer 130 having a thickness of approximately 10um, it is possible to form the inclined resist layer 130 without problem.***

EX1007, [0085].

119. ***Second***, because both Eliashevich-Rabinzohn and Yoo are in the field of semiconductor manufacturing and because the dimensions of the structures in Eliashevich-Rabinzohn are commensurate with the dimensions of the structures in Yoo, a POSITA would have readily understood that Yoo's teachings are readily applicable to Eliashevich-Rabinzohn. EX1003, 18:4-5 ("Typically, the entire stack including mesa 164 is on the order of five microns thick."); EX1005, [0033] ("The vertical topology GaN-based LED layer structure 120 is beneficially less than 5 microns thick.").

120. **Third**, both Eliashevich-Rabinzohn and Yoo use a technique involving RIE. EX1003, 18:16-19; EX1005, [0035]. In addition, Yoo discloses that a **thick photoresist** (such as a **10-micron thick photoresist**) would help facilitate a RIE-based manufacturing process, because the **thick photoresist** aids in protecting the underlying structure from intense plasma. EX1005, [0035]. Thus, a POSITA would have readily recognized that a thick photoresist would also be useful in Eliashevich-Rabinzohn.

[0035] Because of the hardness of sapphire and GaN, the trenches 124 are beneficially formed in the structure of FIG. 3 using reactive ion etching, preferably inductively coupled plasma reactive ion etching (ICP RIE). Forming trenches using ICP RIE has two main steps: forming scribe lines and etching. Scribe lines are formed on the structure of FIG. 3 using a photo-resist pattern in which areas of the sapphire substrate 122 where the trenches 124 are to be formed are exposed. The exposed areas are the scribe lines and all other areas are covered by photo-resist. *The photo-resist pattern is beneficially fabricated from a relatively hard photo-resist material **that withstands intense plasma**.* For example, the photo-resist could be AZ 9260, while the developer used to develop the photo-resist to form the scribe lines could be AZ MIF 500.

EX1005, [0035].

121. **Fourth**, it would have been understood by a POSITA that the combination merely involves applying a known technique (*i.e.*, using a **10-micron thick photoresist layer** per Yoo) to a known method (*i.e.*, a semiconductor manufacturing method per Eliashevich-Rabinzohn) ready for improvement

(preventing inadvertent etching of underlying structures) to yield predictable results of manufacturing an LED according to the design specifications.

122. **Finally**, it would have been understood by a POSITA that the combination is nothing more than a simple substitution of one known element (Eliashevich-Rabinzohn's photoresist layer) for another (Yoo's 10-micron thick photoresist layer) to obtain predictable results of preventing inadvertent etching of underlying structures according to the design specifications.

123. There would have been a reasonable expectation of success to apply Yoo's thick photoresist of 10-microns in the manufacturing process of Eliashevich-Rabinzohn. For instance, Yoo teaches that a 10-micron thick photoresist was successfully used in LED manufacturing. EX1005, [0036]. Further, a thick photoresist was commonly used in semiconductor manufacturing, particularly to create a photoresist layer with an inclined side surface. *See* EX1007, Title ("Semiconductor **Light Emitting Device** And Manufacturing Method Therefore"); [0085] ("As to the resist layer 130 having a thickness of *approximately 10um*, *it is possible to form the inclined resist layer 130 without problem.*"). Accordingly, there would have been a reasonable expectation of success that the manufacturing process of Eliashevich-Rabinzohn would work well with a 10-micron thick photoresist. *See* EX1003, 18:24-26.

124. Also, there would have been a reasonable expectation of success for a semiconductor manufacturing process, such as Eliashevich-Rabinzohn's manufacturing process, to form and use a 10-micron thick photoresist layer. Indeed, it was well known that the thickness of a photoresist layer is easily controlled by the parameter related with the photoresist application technique. For example, "Introduction to Semiconductor Manufacturing," a textbook published in 2001, states that "when the photoresist is applied to a wafer using a spin coater, "[t]he PR [photoresist] thickness is related to both PR viscosity and the wafer spin rate, ... The higher the spin rate, the thinner the PR layer, ..."

6.3.3 Photoresist Coating

The photoresist coating is a deposition process in which a thin layer of photoresist is applied on the wafer surface. The wafer is placed on a spindle with a vacuum chuck that can hold the wafer during the high-speed rotation. Liquid photoresist is applied on the wafer surface, and the centrifugal force from the wafer rotation spreads the liquid over the whole wafer. After the solvents in the PR have evaporated, the wafer is coated with a thin layer of PR. ***The PR thickness is related to both PR viscosity and the wafer spin rate, as illustrated in Figure 6.9. The higher the spin rate, the thinner the PR layer,*** and the better the PR thickness uniformity. The PR thickness is inversely proportional to the square root of the spin rate. Since photoresists have high viscosity and very high surface tension, very high spin rate is required for uniform PR spin coating. The higher the viscosity, the thicker the PR films at the fixed spin rate. Viscosity of the photoresist can be controlled by the solid content

of the photoresist solution. The typical photoresist thickness in photolithography is between 5000 and 30,000 Å.

EX1011, 16-17.

125. Indeed, Yoo itself demonstrates that an LED manufacturing method is compatible with and readily uses a 10-micron thick photoresist layer. EX1005, [0036]. *See also* EX1007, [0082], [0086].

126. Further, a POSITA would have understood that selecting the thickness of the photoresist merely amounts to a routine optimization of a design parameter (e.g., the thickness) and the POSITA would have understood that optimization was well within the ordinary skill in the art.

127. At the least, a POSITA would have found it obvious to try to apply Yoo's 10-micron thick photoresist layer in Eliashevich-Rabinzohn's manufacturing process. Yoo teaches that it is feasible to form a 10-micron thick photoresist layer and that using a thick-enough photoresist was desirable to provide enough protection for the underlying semiconductor layers, which is suggested by Eliashevich. *See* EX1003, 18:24-26. As such, a POSITA would have found it to be common sense to try using the 10-micron thick photoresist layer of Yoo in Eliashevich-Rabinzohn's manufacturing process.

C. Ground III: Eliashevich In Combination With Rabinzohn and Huang Renders Obvious Claims 9 and 15.

1. Huang (EX1006)

128. Huang describes a “method of improving a photoresist profile for a semiconductor manufacturing.” EX1006, 3:54-55, 1:12-16. In conjunction with Figure 3, Huang explains the steps of: Step 301 of photoresist coating; Step 302 on a soft bake; Step 303 on exposure; Step 304 on post-exposure bake (PEB) at “about 100-120°C;” Step 305 on development; Steps 306 at “about 135-145 °C” or 307a at “about 110 °C” on a hard bake. *See* EX1006, 2:53-3:32.

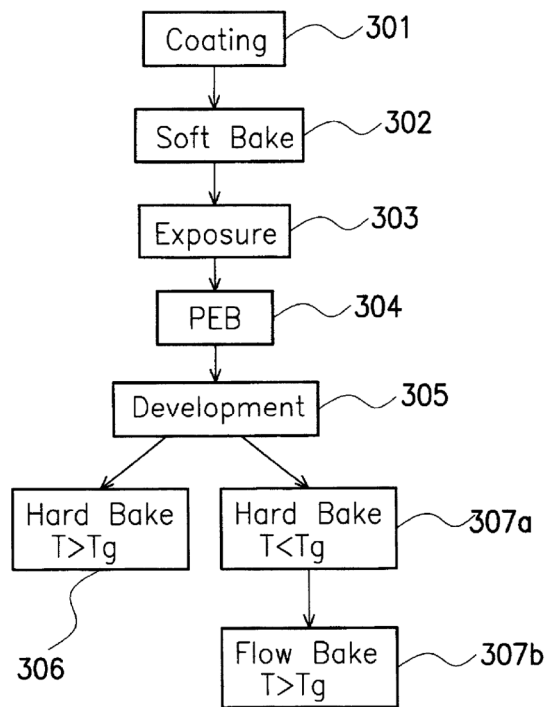


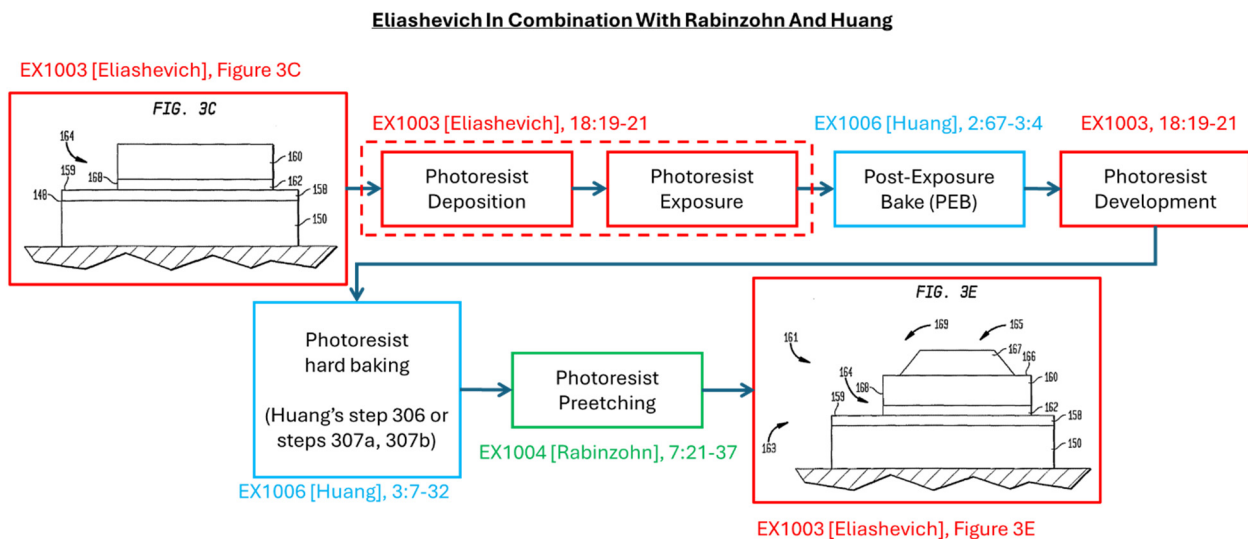
FIG. 3

EX1006, Figure 3.

2. Eliashevich In Combination With Rabinzohn And Huang (“Eliashevich-Rabinzohn-Huang”)

129. It would have been obvious to a POSITA to combine Huang's photoresist baking steps with Eliashevich-Rabinzohn (as described in Section VIII.A.3 [Eliashevich-Rabinzohn]) to improve the photoresist processing in Eliashevich-Rabinzohn. In particular, Huang teaches that before photoresist development, the photoresist is conventionally subject to PEB as Huang shows in Figure 3, and that after development, the photoresist is also hard baked.

130. As such, consistent with Figure 3 of Huang, it would have been obvious to a POSITA to modify Eliashevich-Rabinzohn's manufacturing process to include: (1) a PEB step of baking at "about 100-120°C" the exposed photoresist between the steps of exposure and development; and (2) a step for hard baking (e.g., at "about 135-145 °C" as disclosed in step 306 or "about 110 °C" as disclosed in step 307a) after the photoresist is developed as illustrated below.



i. Reasons To Combine Eliashevich-Rabinzohn with Huang

131. There would have been a motivation for the combination described above (i.e., to combine Eliashevich-Rabinzohn with Huang). Even “Introduction to Semiconductor Manufacturing Technology,” which is an elementary textbook published 5 years before the earliest priority date of the ’626 Patent discloses the steps of PEB and hard bake. *See* EX1013, 31-32, 35-36. Further, the PEB and hardbake steps being part of the “conventional method to patterning photoresist layer” is expressly stated by Huang. As such, a POSITA would have found it to be common sense to apply such conventional method to augment the Eliashevich-Rabinzohn’s manufacturing processes.

132. Further, there would have been motivation to augment Eliashevich-Rabinzohn’s manufacturing processes with the steps of PEB and hard bake of Huang, since PEB and hard bake steps were known to have benefits in semiconductor manufacturing. As an example, the PEB steps were well known generally to facilitate the smoothing of the developed photoresist layer’s side surface. “When the exposure light reflects from the photoresist-substrate interface, it can interfere with incoming exposure light and cause the standing wave effect due to the constructive and destructive interference at the different depth.” EX1011, 31.

“The standing wave effect causes striations ... through the photoresist,” which is known to cause imprecision in the subsequent etching processes. EX1011, 31.

6.3.6 Postexposure Bake

When the exposure light reflects from the photoresist-substrate interface, it can interfere with incoming exposure light and cause the standing wave effect due to the constructive and destructive interference at the different depth. The standing wave pattern is illustrated in figure 6.22.

The standing wave effect causes striations of overexposed and underexposed areas through the photoresist, as shown in Figure 6.23. The distance between two peaks is the wavelength of the exposure light (λ) divided by $2 \times$ the refractive index of the photoresist ($2n_{PR}$).

EX1011, 31.

133. It was well known that when the photoresist is subject to a “***post-exposure bake (PEB)*** between the exposure and develop processes,” the standing wave effect would be reduced. EX1011, 32. *See also* EX1016, 1.

When the feature size is large, the standing wave effect is not a big concern. As the minimum feature size shrinks, several methods are used to reduce the reflection-induced standing wave effect. Dye has been added in the photoresist to reduce the reflection intensity. Metallic and dielectric layers have been deposited on the wafer surface as antireflection coatings (ARC) to reduce and minimize the reflection from the surface of the wafer. An organic anti-reflective coating is also used, which may be applied by the photoresist spin coater prior to photoresist spin-on. ***A baking process called post-exposure bake (PEB) between the exposure and develop processes can also help to minimize the standing wave effect.***

EX1011, 31-32.

134. Likewise, a POSITA would have known that hard bake steps usually help with later photoresist processing. As an example, as explained by Huang, a hard bake step is helpful in “evaporat[ing] the remaining solvent contained in the photoresist layer”; improving “the adhesion of the photoresist layer” to the underlying structure; and “solidify[ing] the photoresist and [] form[ing] the profile of the photoresist layer.” EX1006, 1:28-35, 1:42-43.

After the steps of exposure 103, the post-exposure bake 104, and the development step 105, a hard bake step 106 is performed to **evaporate the remaining solvent contained in the photoresist layer**. In addition to minimize the containing solvent, the adhesion of the photoresist layer can also be improved. Furthermore, the hard bake step is also advantageous to resist of the subsequent etching and ion implantation processes. The selectivity of such processes can be increased to etch or implant selectively only the positions uncovered by the photoresist layer. A hot plate is typically used for performing the hard bake step. In the conventional method, as shown in FIG. 1, the temperature for the hard bake 106 is about 110° C. for about 90 seconds. The purpose is to *solidify the photoresist and to form the profile of the photoresist layer*. Therefore, an operation temperature of the bake hard step is normally less than the glass transition temperature (T) of the photoresist layer.

EX1006, 1:28-45.

135. Indeed, Xiao in the 2001 textbook “Introduction to Semiconductor Manufacturing Technology” states that:

After development, the wafer is put through a *hard bake* process. Hard bake drives out the remaining solvents in the photoresist,

strengthens the PR [photoresist], and improves the PR etch and implantation resistance via further polymerization, and also improves its adhesion to the wafer due to further thermal dehydration.

EX1011, 35.

136. There would have been a reasonable expectation of success for adding the PEB and hard bake steps to the Eliashevich-Rabinzohn's process flow, because PEB and hard bake steps are part of a "*conventional* method to patterning [a] photoresist layer" (EX1006, 1:22-27). Further, Huang in particular discloses that the steps of PEB and hard bake can be generally used in the particular order described in the combination. *See* EX1006, Figure 3. PEB and hard bake steps were well known in the art and merely involve heating up a wafer, e.g., by putting the wafer on a "hot plate." EX1011, 31-32, 35-36. EX1006, 1:38-39.

137. Thus, the combination described above would have merely involved using known techniques (Huang's PEB and hardbake steps) to improve a similar manufacturing technique (Eliashevich-Rabinzohn's manufacturing process) in the same way (performing the PEB step before the photoresist development and the hard bake step after the photoresist development, per Huang) to achieve the expected result of reducing the standing wave effect (due to PEB) (EX1011, 31-32), "evaporat[ing] the remaining solvent contained in the photoresist layer," "improving "the adhesion of the photoresist layer" to the underlying structure, "solidify[ing] the

photoresist and [] form[ing] the profile of the photoresist layer,” and improving the surface profile of the photoresist layer (due to hard bake). EX1006, 1:28-35, 1:42-43, 3:7-12; 3:30-32; EX1015, 11; EX1011, 35.

138. Likewise, the combination of Eliashevich-Rabinzohn with Huang would have merely involved applying known techniques (Huang’s PEB and hard bake steps) to a known method (Eliashevich-Rabinzohn’s LED manufacturing process) ready for improvement to yield predictable results of reducing the standing wave effect, evaporating remaining solvent contained in the photoresist layer, and improving adhesion of the photoresist layer to the underlying structure, as explained above.

139. At least, a POSITA would have found it common sense and obvious to try to apply Huang’s PEB and hard bake steps because Huang’s PEB and hard bake steps are known to be “conventional” in processes for semiconductor manufacturing (e.g., Eliashevich-Rabinzohn’s LED manufacturing). In addition, as explained above, Huang’s PEB and hard bake steps provide specific benefits with a reasonable expectation of success to the manufacturing process described by Eliashevich-Rabinzohn.

3. Claim 9

- i. [9Pre] A method of manufacturing a light emitting device, comprising:
 - [9A] sequentially forming an N-type semiconductor layer, active layer, and P-type semiconductor layer on a substrate;
 - [9B] forming an etching mask pattern, of which a side surface is not perpendicular to but inclined at a slope from a horizontal plane, on the P-type semiconductor layer; and
 - [9C] removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern;
 - [9D-1] wherein forming the etching mask pattern comprises: forming a photoresist on the P-type semiconductor layer;
 - [9D-2] exposing the photoresist to light;

140. [9Pre]-[9D-2] are the same as [1Pre]-[1D-2]. *See* Claims at Issue.

Eliashevich-Rabinzohn teaches [9Pre]-[9D-2] for the reasons provided above for [1Pre]-[1D-2].

- ii. [9D-3] hard-baking and developing the photoresist; and

141. Eliashevich-Rabinzohn-Huang teaches [9D-3].

142. *First*, Huang discloses “hard-baking ... the photoresist.” [9D-3] does not specifically require an order in which the claimed “hard-baking” step and “develop[ment]” step are performed, and I see no reason to enforce any particular order between the claimed “hard-baking” step and “develop[ment]” step. As such, as I explain below, the hard bake step 306 or the hard bake step 307a of Huang meets the claimed “hard-baking” limitation.

143. As shown by the combination of Eliashevich-Rabinzohn-Huang, Huang discloses that “a step of *hard bake* is performed.” EX1006, 3:4-7. “When a *single flow step 306* is used,” “the temperature for performing *hard bake* step ... is about *135-145° C.*” EX1006, 3:7-20. “When a *multiple flow step [307]* is used, ... the *hard bake 307a* is performed at about *110° C.*” EX1006, 3:21-30. Because both the “*hard bake 306*” step and the “*hard bake 307a*” step “*hard-bak[es]* ... the *photoresist*,” the “*hard bake 306*” step or the “*hard bake 307a*” both independently satisfy the claimed “*hard-baking.*”

When a multiple flow step is used, a flow bake 307b step is performed after performing the hard bake 307a. For a typical polymer photoresist material, the hard bake 307a is performed at about 110° C., which is lower than the glass transition temperature, for about 90 seconds. After the hard bake process 307a, the flow bake step 307b is performed at a temperature higher than the glass transition temperature. *Again, for a typical photoreist (sic) material, the temperature is about 135-145°C.* and the duration of the flow bake process is for about 60-90 seconds. The photoresist layer 20 can thus reflow to modify the profile, and the reentrant formed in the conventional method is thus eliminated.

EX1006, 3:21-32.

144. At least, the *hard bake step 306* being performed at “about *135-145° C*” (EX1006, 3:7-20) renders obvious the claimed *hard-baking* because *hard bake step 306* being performed at the range of “about *135-145°C*” overlaps with the *hard baking* temperature range of claim 15: “performed at a temperature of 100 to

140°C.” EX1001, claim 15. Further, there is nothing in the record that suggests that the required range produces novel or unexpected results, that the prior art teaches away from the claimed range of 100 to 140°C, or the claimed temperature range is non-obviousness.

145. Similarly, the step of the **hard bake 307a** occurs at “about **110° C.**” (EX1006, 3:21-30), which also falls within the temperature range of **hard baking** required by claim 15, and therefore also discloses the claimed **hard-baking**.

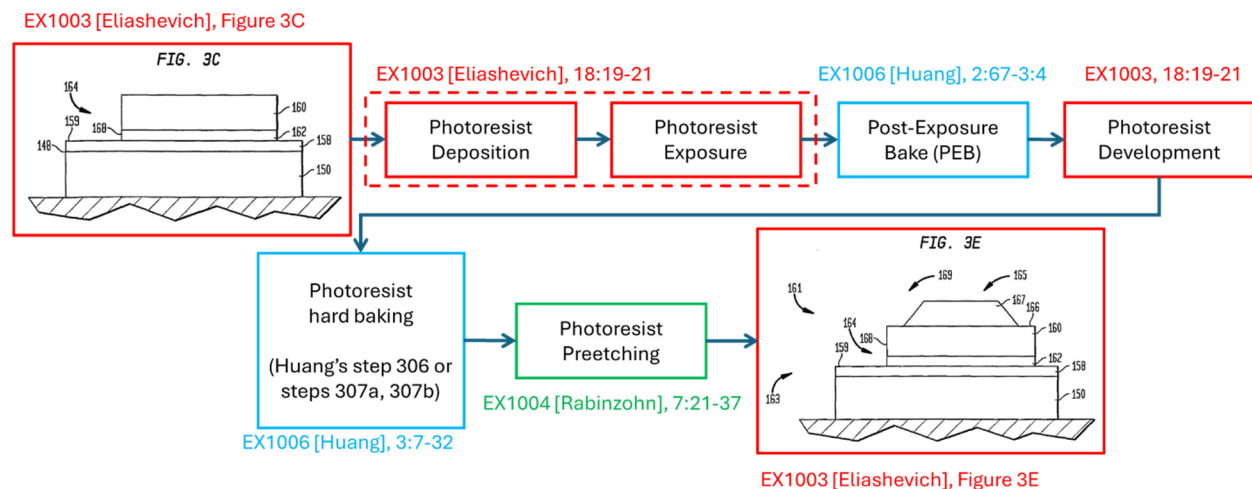
146. If the claimed “developing” step must occur after the “hard baking” step, the Eliashevich-Rabinzohn-Huang combination nevertheless discloses the claimed “hard baking,” because the **post-exposure bake (PEB) 304** step is included in the combination of Eliashevich-Rabinzohn-Huang. Huang discloses that “an exposure step 303 is performed on the **photoresist layer 20**, followed by performing the steps of **post-exposure bake (PEB) 304 ...**” EX1006, 2:66-3:2, Figure 3. “The temperature for performing the **post-exposure bake 304** is about **100-120° C.**, ...” EX1006, 3:2-4. The claimed “**hard-baking**” limitation is satisfied by the PEB step 304, because the “**hard-baking** is performed at a temperature of 100 to 140°C,” as claimed by claim 15, and the temperature of Huang’s **PEB step 304** falls inside that temperature range (EX1006, 3:2-4 (**PEB** occurring at “100-120°C”)).

After the soft bake step, an exposure step 303 is performed on the photoresist layer 20, followed by performing the steps of post-exposure bake (PEB)304 and development 305. **The**

temperature for performing the post-exposure bake 304 is about 100-120C., and the duration for such process is about 60-90 seconds. As shown in FIG. 2, after development, a step of hard bake is performed, and the temperature of the hard bake depends on which kind of flow step is performed. When a single flow step 306 is used, only the hard bake step 306 is performed to make the photoresist layer reflow, so that any reentrant structures formed can be removed thus, the profile of an opening with a substantially vertical sidewall in the photoresist layer 20, as shown in FIG. 4, can be achieved. The reentrant formed in the conventional method can thus be eliminated. The temperature of Such hard bake step is higher than the glass transition temperature of the photoresist layer 20. For a typical polymer photoresist material, the glass transition temperature (T_g) is about 130-140° C., *while the temperature for performing hard bake step for the single flow step is about 135-145 C.* The duration for such hard bake step is about 60-90 seconds.

EX1006, 2:66, 3:20.

Eliashevich In Combination With Rabinzohn And Huang



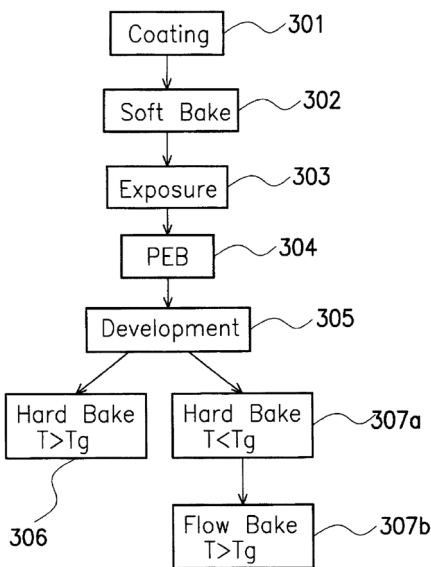


FIG. 3

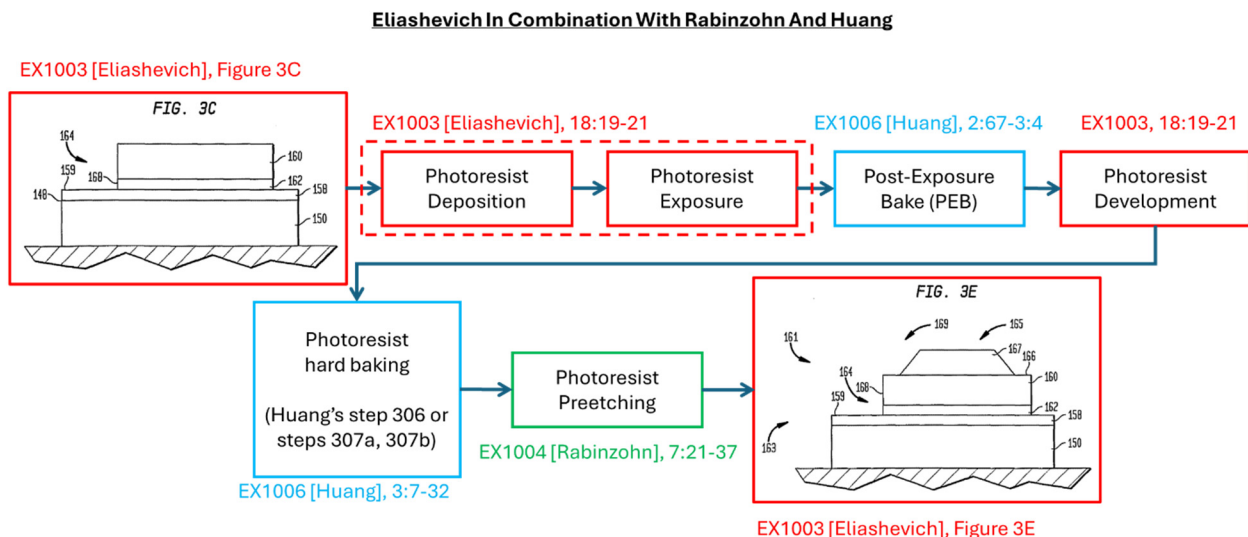
EX1006, Figure 3.

147. **Second**, Eliashevich teaches “**developing** the **photoresist**.” Eliashevich discloses that “[a] **photoresist material 167** is deposited on the top surface 166 of mesa 164 and is exposed and **developed** to form a mask 165 having openings 169” to form the mask 165. EX1003, 18:19-21.

Referring to FIGS. 3D-3F, mesa 164 is subjected to an etching process which removes some of the semiconductor material from the p-type layers 160. One preferred etching process includes a reactive ion etching (RIE) process. In other preferred methods, other forms of plasma etching are used, such as ICP. ***A photoresist material 167 is deposited on the top surface 166 of mesa 164 and is exposed and developed to form a mask 165 having openings 169.*** During etching, the walls 168 and a portion of the top surface 166 are attacked and semiconductor material is removed from the mesa 164 until a curved surface is obtained. Preferably, a portion of the top surface remains after

etching, to be used for an upper electrode-pad unit, as discussed below. The mask may be given a tapered shape, as shown in FIG. 3D, utilizing controlled processing or baking of the photoresist and the relative etch rates for the photoresist and semiconductor materials may be tailored so as to form the curved surfaces on the mesa 164, at the upper end of the structure 110. The RIE etching removes the mask at an outside portion of the mesa first and then begins to remove semiconductor material from the p-type layers 160, as represented by the dashed lines in FIG. 3D. These techniques are known in the art. In other embodiments, conventional lithographic techniques may also be used. The radial surfaces on the means may also be formed utilizing an additive process, as discussed above. In embodiments in which the radial surfaces are formed in an additive process, transparent dielectric or polymeric material is deposited on the p-type layers 160.

EX1003, 18:14-19:7.



iii. [9D-4] **etching** a side surface of the developed **photoresist** to have the **slope from the horizontal plane**.

148. Eliashevich-Rabinzohn-Huang teaches [9D-4].

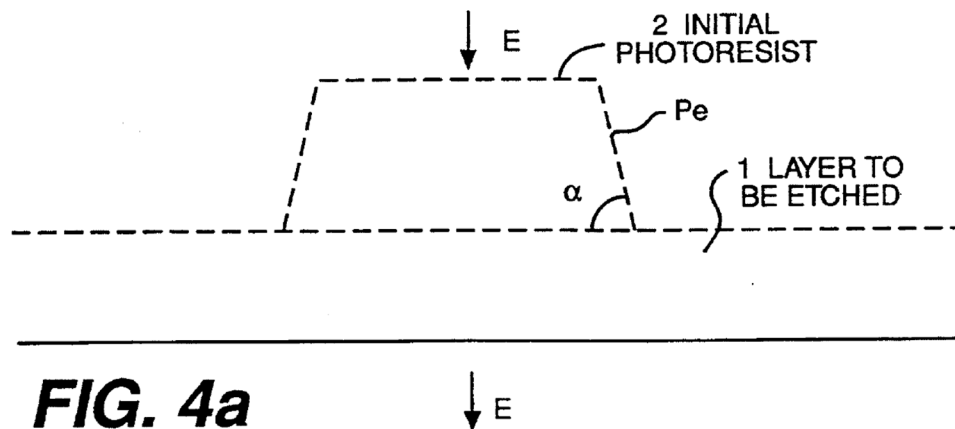
149. As explained in Section VIII.A.2 [Rabinzohn] and Section VIII.A.3

[Eliashevich-Rabinzohn], Rabinzohn teaches performing the “**preetching**” on the **photoresist layer 2** to create sloped side surfaces, which is shown below in Figure

4a. As an example, Rabinzohn discloses:

Alternatively, in the case of FIG. 4, the initial masking photoresist layer 2, previously to the actual etching process, has been subjected to a **preetching stage**, the effect of which is to generate **etching flanks of slope pe** inclined in relation to the free surface of the layer 1 to be etched, assumed to be horizontal, the **etching flanks of the initial masking photoresist layer 2 being thus inclined at an angle α** in relation to the abovementioned free surface.

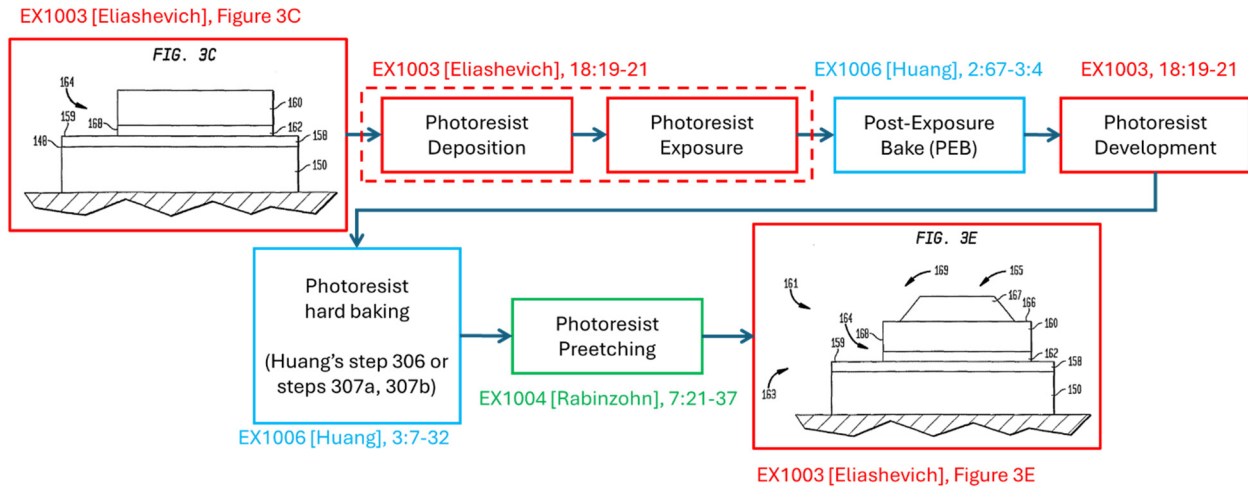
EX1004, 7:21-30.



EX1004, Figure 4a.

150. Further, in the combination of Eliashevich-Rabinzohn-Huang, the **preetching step** of Rabinzohn is applied to Eliashevich’s **photoresist**, which, as shown below, has already gone through the development step.

Eliashevich In Combination With Rabinzohn And Huang



151. As such, Eliashevich-Rabinzohn-Huang teaches that the sidewalls (the claimed “side surface” of the developed photoresist layer 2 (the claimed “developed photoresist”) are preetched (the claimed “etching”) to have, in relation to the horizontal plane, an angle α , free surface of the layer 1 (the claimed “slope from the horizontal plane”).

4. Claim 15

- i. [15] The method as claimed in claim 9, wherein the hard-baking is performed at a temperature of 100 to 140°C.

152. Eliashevich-Rabinzohn-Huang discloses the additional limitation of Claim 15. Eliashevich-Rabinzohn-Huang teaches that “the hard-baking is performed at a temperature of 100 to 140°C” for the reasons provided in Section VIII.C.3.ii [Ground III, limitation 9D-3]. See EX1006, 3:2-4 (PEB occurring at

“*100-120°C*”); 3:7-20 (*hard bake 306* occurring at “about *135-145° C*”); 3:21-30 (*hard bake 307a* occurring at “about *110° C*”).

D. Ground IV: Eliashevich In Combination With Rabinzohn, Huang, And Yoo Renders Obvious Claim 13.

1. Claim 13

- i. [13] The method as claimed in claim 9, wherein the *photoresist* with a thickness of 3 to 50 μm is used in the forming the etching mask pattern.

153. As I explained in Section VIII.B.1.i [Ground II, Claim 7], a POSITA would have found it obvious to combine Eliashevich-Rabinzohn with Yoo to make the *photoresist 167* of Eliashevich to be to be as disclosed in Yoo – *10 microns thick*. It would be obvious to a POSITA to combine Yoo with Eliashevich-Rabinzohn-Huang (as described in Section VIII.C.2) for largely the same reason to make the *photoresist 167* of Eliashevich to be *10 microns thick* as disclosed by Yoo. *See* Section VIII.B.1.i [Ground II, Claim 7].

154. As an example, a POSITA would have been motivated to combine Yoo with Eliashevich-Rabinzohn-Huang, because using a thick *photoresist*, similar to the 10-micron thick *photoresist* of Yoo, is itself motivated by Eliashevich in creating the etching mask pattern. *See* EX1003, 18:24-26. In addition, Eliashevich-Rabinzohn-Huang and Yoo are all in the field of semiconductor manufacturing. The dimensions of Yoo’s structures are similar to the dimensions of Eliashevich-Rabinzohn-Huang’s

structures. EX1003, 18:4-5; EX1005, [0033]. In fact, in the field of semiconductor manufacturing, it was common to use a 10-micron thick photoresist having an inclined surface. *See* EX1007, Title, [0085].

155. In addition, a RIE etching technique is used by both Eliashevich-Rabinzohn-Huang and Yoo (EX1003, 18:16-19; EX1005, [0035]), and as Yoo teaches, a manufacturing process based on RIE would benefit from using a thick photoresist, which can help preserve the underlying structure against intense plasma (EX1005, [0035]).

156. Such a combination would have merely amounted to applying a known technique of using the 10-micron thick photoresist layer taught by Yoo to a known method of the semiconductor manufacturing method taught by Eliashevich-Rabinzohn-Huang, which is ready for improvement (e.g., to prevent inadvertent etching of underlying structures), to yield predictable results of making semiconductor structures based on intended specifications for design.

157. Likewise, it would have been understood by a POSITA that combining Eliashevich-Rabinzohn-Huang and Yoo amounts to a straightforward substitution of a photoresist layer in Eliashevich-Rabinzohn-Huang (a known element) for a 10-micron thick photoresist layer per Yoo (another known element) to obtain predictable results of preventing inadvertent etching of underlying structures during semiconductor manufacturing.

158. There would have been a reasonable expectation of success in using Yoo's 10-micron thick photoresist in Eliashevich-Rabinzohn-Huang's manufacturing process. Yoo discloses that a 10-micron thick photoresist was successfully used in semiconductor manufacturing. EX1005, [0036]. Indeed, it was common to use such a thick photoresist in semiconductor manufacturing, specifically to form a photoresist layer with an inclined side surface. EX1007, Title; [0085] ("As to the resist layer 130 having a thickness of *approximately 10um*, it is *possible to form the inclined resist layer 130 without problem.*"). As such, a POSITA would have had a reasonable expectation that a 10-micron thick photoresist would also work well in Eliashevich-Rabinzohn-Huang's semiconductor manufacturing process, as suggested by Eliashevich. See EX1003, 18:24-26.

159. Further, in semiconductor manufacturing processes (e.g., the semiconductor manufacturing process of Eliashevich-Rabinzohn-Huang), there would have been a reasonable expectation of success in creating and utilizing a 10-micron thick photoresist layer. It was well known that the thickness of a photoresist layer is easily controlled by controlling the parameter associated with the photoresist application technique, such as spin coating. See EX1013, 17. Yoo itself serves as an example of semiconductor manufacturing that readily uses a 10-micron thick photoresist layer. See also EX1007, [0082], [0086].

160. And in fact, selecting the thickness of the photoresist would have merely amounted to a routine optimization of a design parameter—the thickness—and such routine optimization was well within the ordinary skill.

161. At least, a POSITA would have found it obvious to try to use a 10-micron thick photoresist layer as disclosed by Yoo in Eliashevich-Rabinzohn-Huang’s manufacturing process. Yoo teaches that it is feasible to form a 10-micron thick photoresist layer, and as suggested by Eliashevich, using a photoresist that is thick enough to provide adequate cover for the underlying semiconductor layers. As such, a POSITA would have found it to be common sense to try Yoo’s 10-micron thick photoresist layer in the manufacturing process described by Eliashevich-Rabinzohn.

E. Ground V: Horio Anticipates Claims 9, 13, And 15.

1. Horio (EX1007)

162. Horio addresses an LED manufacturing process that produces an LED with sloped side surfaces. The LED in Horio includes a nitride layer that “includes at least an n-type nitride semiconductor layer 101, a luminescent layer 102, and a p-type nitride semiconductor layer 103,” electrodes 104, 105, and transparent substrate 100. EX1007, [0053]-[0054], Figures 2B, 3.

[0054] The structure of the light emitting device section 1 will be described. FIGS. 2A and 2B show the detailed structure of the light emitting device Section 1. The light emitting device section

1 can include a sapphire substrate 100, a nitride semiconductor layer 11, electrodes 104 and 105, and a protective film 106. ***The nitride semiconductor layer 11 includes at least an n-type nitride semiconductor layer 101, a luminescent layer 102, and a p-type nitride semiconductor layer 103 which can be laminated in this order on the sapphire substrate 100.*** In this example, the nitride semiconductor layer 11 is designed so as to have an emission wavelength of 460 nm. The light emitting device section 1 is mounted on the support substrate section 10 with the nitride semiconductor layer 11 facing toward the support substrate section 10. Light from the luminescent layer 102 is emitted from the rear face (emission surface) 100a of the sapphire substrate 100.

EX1007, [0054].

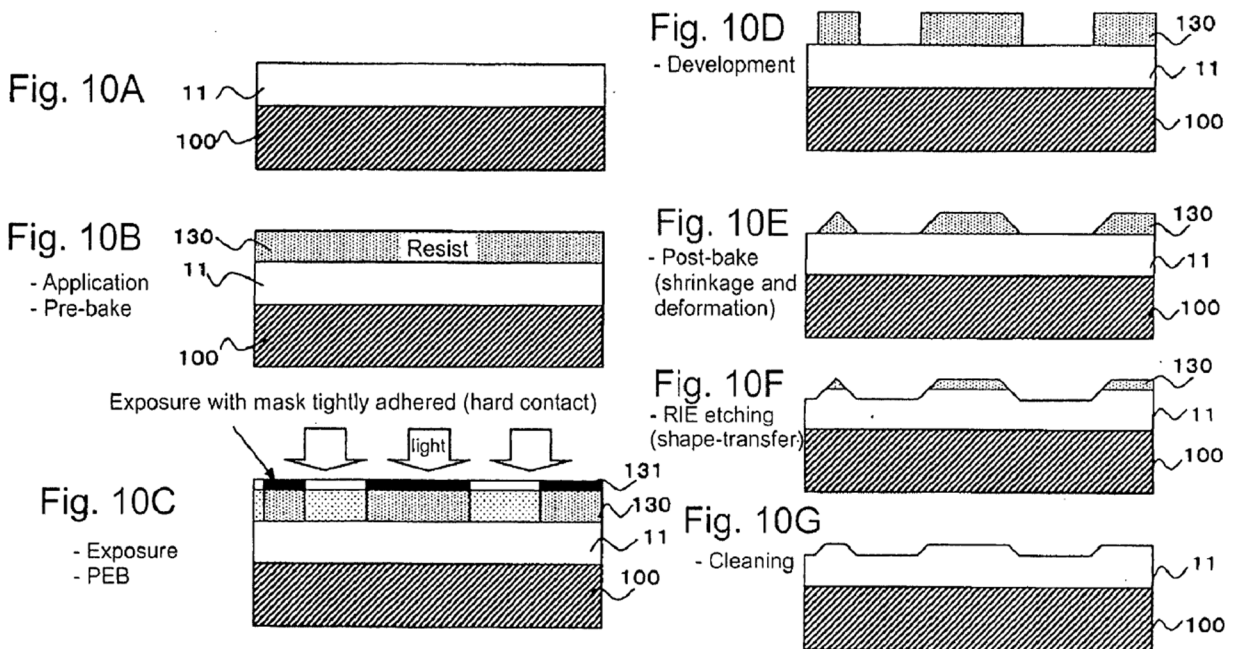
163. Horio's manufacturing method includes two specific steps of photolithography. The first step is illustrated in Figures 10A-10G and involves providing a sloped side surface on a stack of the p-type layer 103, luminescence layer 102, and a portion of the n-type layer. The second step is illustrated in Figures 12A-12G and involves creating a sloped side surface on the n-type layer 101's bottom portion that is remaining.

A protective film with low wettability has larger functional effect when being overlaid on p-type ohmic electrode.



164. Now, focusing on Figures 10A-10G, Horio discloses:

- EX1007, [0078].



EX1007, Figures 10A-10G.

165. For example, Horio states that the nitride semiconductor layer includes “at least an n-type nitride semiconductor layer 101, a luminescent layer 102, and a p-type nitride semiconductor layer 103” and is on top of a substrate 100, as shown in Figure 10A. EX1007, [0054]. Subsequently, Horio discloses, as shown in Figure 10B, that a resist layer 130 is formed through spin-coating and pre-baking. EX1007, [0079]. Horio also discloses that portions of the resist layer 130 are exposed to light and the resist layer 130 is developed, as shown in Figures 10C-10D. EX1007, [0080].

166. Horio then discloses performing a “post bake” after the development, as shown in Figure 10E. EX1007, [0080]-[0081]. In particular, Horio states that:

By adjusting temperature and time in this *post bake process*, the whole resist layer 130 shrinks. Thus, *it is possible to incline the end portions of the resist at an angle in accordance with a bake condition*. To be more specific, the end portions of the resist layer 130 incline at an inclination angle of 55 degrees on a post bake condition of *110 degrees centigrade* and 120 seconds. The inclination angle becomes 45 degrees on a post bake condition of *115 degrees centigrade* and 120 seconds, and the inclination angle becomes 35 degrees on a post bake condition of *120 degrees centigrade* and 120 seconds.

EX1007, [0081].

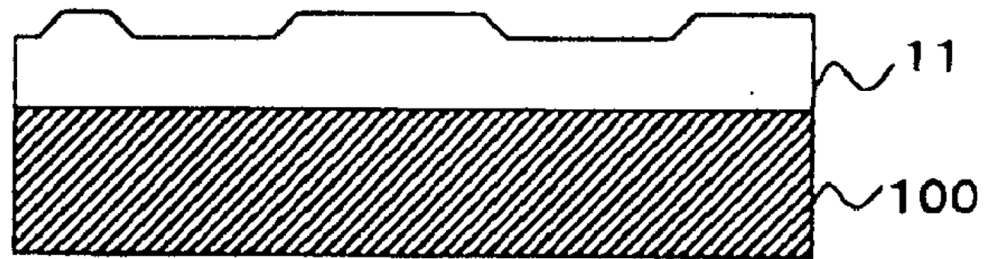
167. Next, as shown in Figure 10F, Horio describes etching the “nitride semiconductor layer 11 up to a predetermined depth by dry etching using a chlorine gas (FIG. 10F).” EX1007, [0082].

168. By undergoing the dry etching process, Horio describes that “the *end faces of the nitride semiconductor layer 11 are formed into an inclination angle which is determined by the inclination angle of the resist layer 130 and the selection ratio*.” EX1007, [0082]. The “selection ratio” is the ratio of rates at which the photoresist layer 130 and the semiconductor layer 110 are removed by the etchant. EX1007, [0086].

169. Next, Horio discloses removing the remaining photoresist from the upper surface. EX1007, Figure 10G, [0083]. As shown in Figure 10G, this method creates a stack of n-type layer 101, a luminescence layer 102, and a p-type layer 103 that has a sloped/inclined side surface.

Fig. 10G

- Cleaning



EX1007, Figure 10G.

170. To provide other LED structures shown in Figure 3, Horio describes performing another lithography process in Figures 12A-12G, which makes a sloped surface on the lower portion of the n-type layer 101. Similar to the method described in Figures 10A-10G, an inclined photoresist layer is used to create a sloped side surface on the lower portion of the n-type layer 101 in the method described in Figures 12A-12G. Both methods described in Figures 10A-10G and Figures 12A-12G form sloped side surfaces that are at a “predetermined angle θ ” with respect to the horizontal plane. EX1007, [0057].

[0057] *In this embodiment, as shown in FIG. 3, end faces of the light emitting device 12 in all directions are inclined with respect to the principal plane of the substrate 100 at a predetermined angle θ .* This is for the purpose of reflecting light, emitted from the luminescent layer 102 and propagating to the direction of the end face, to the principal plane of the substrate 100 by the high reflective n-type ohmic electrode 104, which is disposed on the end face of the n-type nitride semiconductor layer 101. Thus, propagation light from the luminescent layer 102 to the direction of the end face is emitted from the rear face 100a of the substrate 100 and an end face of

A protective film with low wettability has larger functional effect when being overlaid on p-type ohmic electrode.

[illegible]

i. [9Pre] A method of manufacturing a light emitting device, comprising:

EX1002, Page 99

Fig. 2B

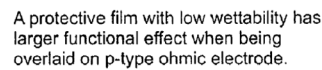
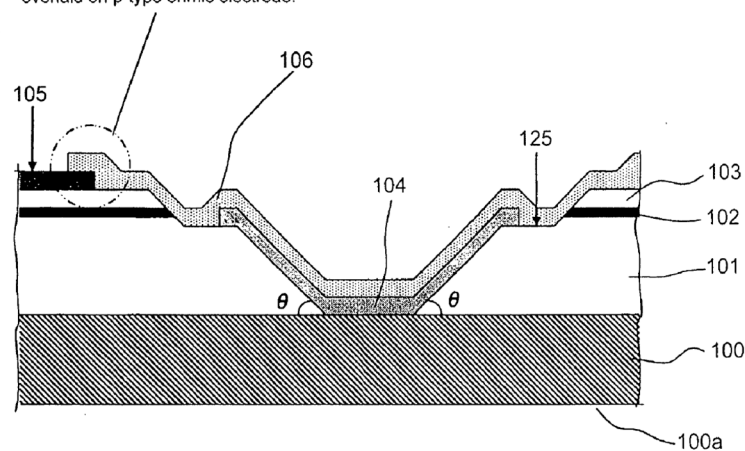
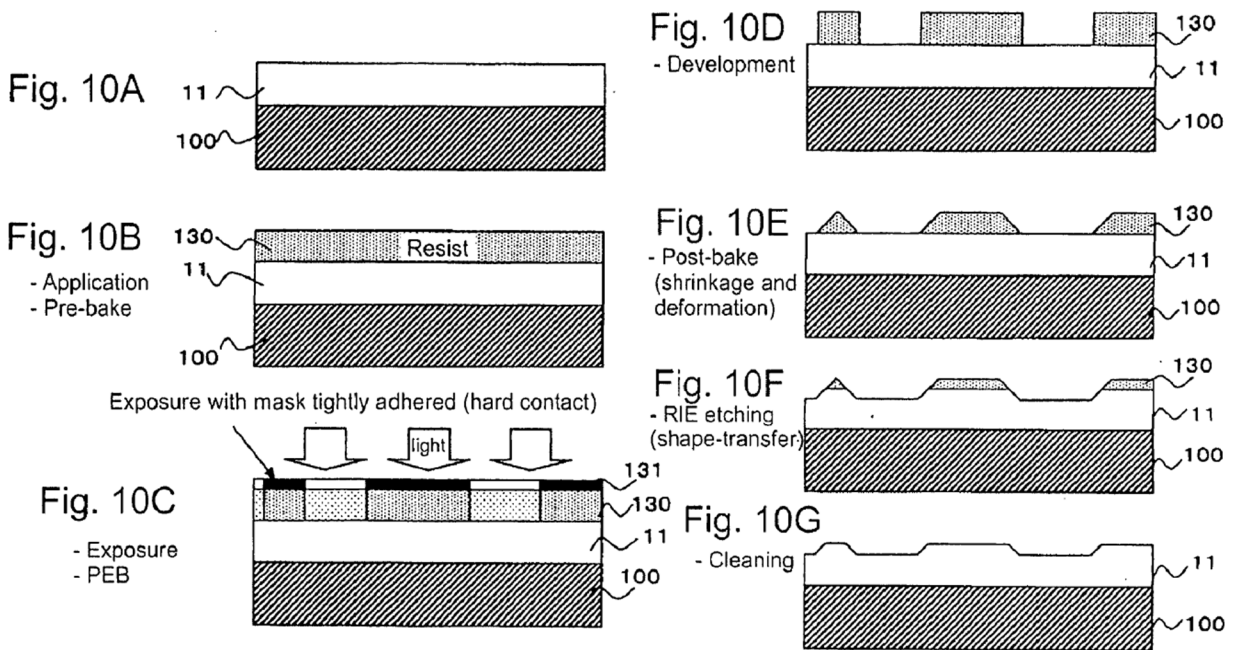


Fig. 3



includes photolithography steps for creating a sloped side surface for the LED,

which is illustrated in Figures 10A-10G and 12A-12G. For example, Horio describes utilizing the methods in Figures 10A-10G and 12A-12G to create the LED device illustrated in Figure 3. EX1007, [0088]-[0090], [0034], Figures 10A-10G, 12A-12G. *See generally* EX1007, [0077]-[0087].



EX1007, Figures 10A-10G.

- ii. [9A] sequentially forming an N-type semiconductor layer, active layer, and P-type semiconductor layer on a substrate;

173. Horio teaches [9A]. Horio discloses forming a “*nitride semiconductor layer 11* [that] includes at least an n-type nitride semiconductor layer 101, a luminescent layer 102, and a p-type nitride semiconductor layer 103 which can be laminated *in this order* on the sapphire substrate 100.” EX1007, [0054], [0079],

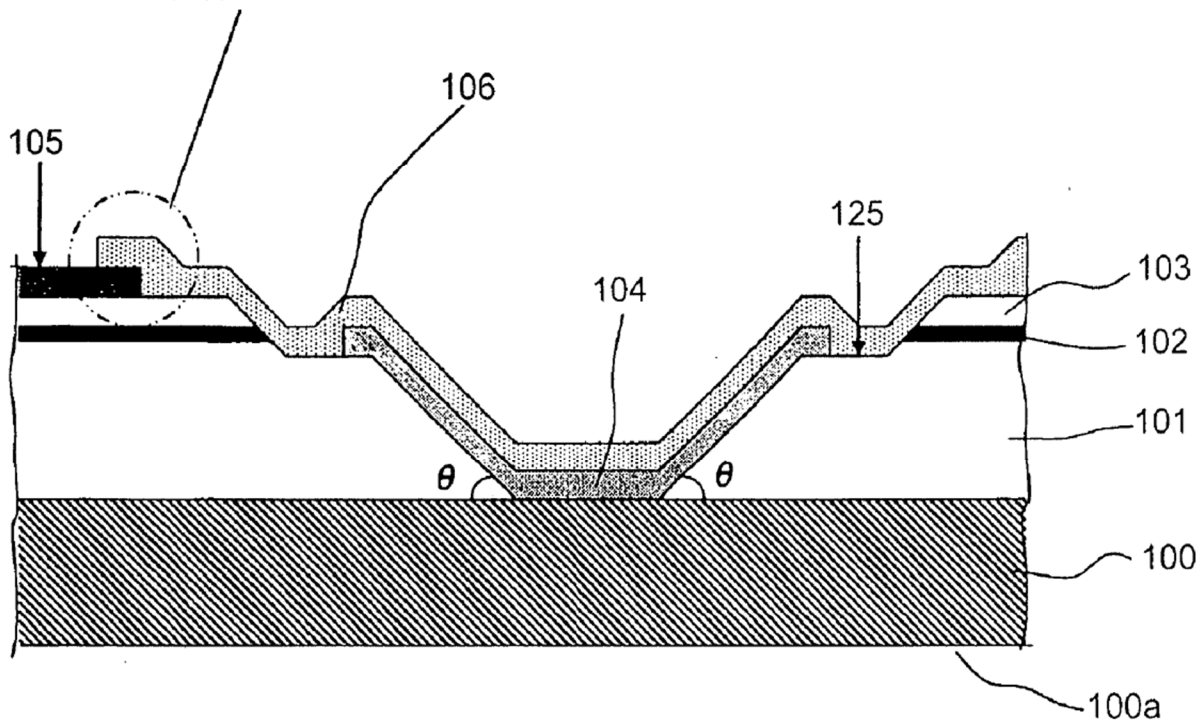
[0088]. Figure 3 shown below illustrates that the substrate 100 has the n-type nitride semiconductor layer 101 formed thereon, then the luminescent layer 102, then the p-type nitride semiconductor layer 103.

[0054] The structure of the light emitting device section 1 will be described. FIGS. 2A and 2B show the detailed structure of the light emitting device Section 1. The light emitting device section 1 can include a sapphire substrate 100, a nitride semiconductor layer 11, electrodes 104 and 105, and a protective film 106. *The nitride semiconductor layer 11 includes at least an n-type nitride semiconductor layer 101, a luminescent layer 102, and a p-type nitride semiconductor layer 103 which can be laminated in this order on the sapphire substrate 100.* In this example, the nitride semiconductor layer 11 is designed so as to have an emission wavelength of 460 nm. The light emitting device section 1 is mounted on the support substrate section 10 with the nitride semiconductor layer 11 facing toward the support substrate section 10. Light from the luminescent layer 102 is emitted from the rear face (emission surface) 100a of the sapphire substrate 100.

EX1007, [0054].

A protective film with low wettability has larger functional effect when being overlaid on p-type ohmic electrode.

Fig. 3



EX1007, Figure 3.

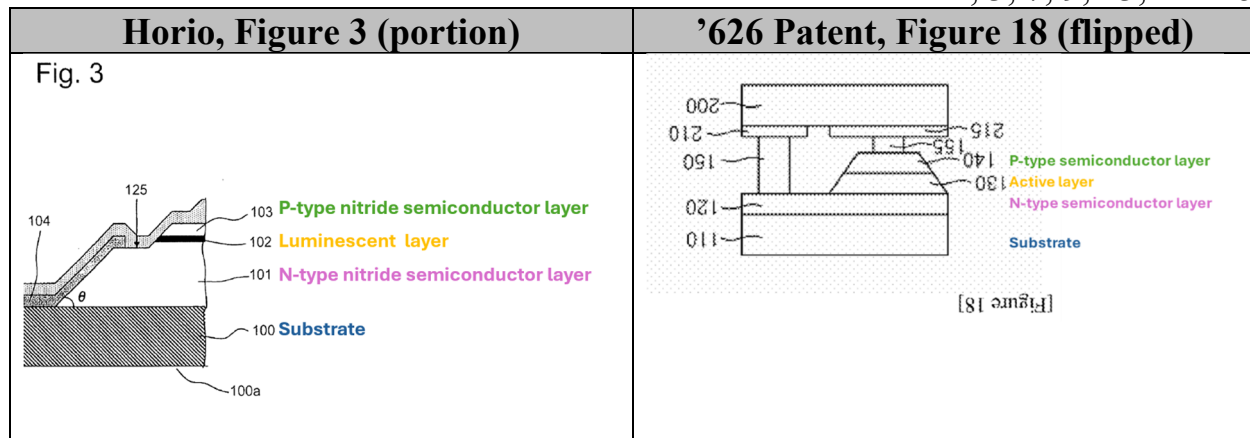
174. The claimed “active layer” is taught by the luminescent layer 102 of Horio, because the luminescent layer 102 of Horio generates light and is between the N-type and P-type semiconductor layers. EX1007, [0008] (“light is emitted from a luminescent layer”); [0054] (“Light from the luminescent layer 102 is emitted from the rear face (emission surface) 100a of the sapphire substrate 100.”).

[0054] The structure of the light emitting device section 1 will be described. FIGS. 2A and 2B show the detailed structure of the light emitting device Section 1. The light emitting device section 1 can include a sapphire substrate 100, a nitride semiconductor layer 11, electrodes 104 and 105, and a protective film 106. The

nitride semiconductor layer 11 includes at least an n-type nitride semiconductor layer 101, a luminescent layer 102, and a p-type nitride semiconductor layer 103 which can be laminated in this order on the sapphire substrate 100. In this example, the nitride semiconductor layer 11 is designed so as to have an emission wavelength of 460 nm. The light emitting device section 1 is mounted on the support substrate section 10 with the nitride semiconductor layer 11 facing toward the support substrate section 10. ***Light from the luminescent layer 102 is emitted from the rear face (emission surface) 100a of the sapphire substrate 100.***

EX1007, [0054].

175. The way the '626 Patent describes the claimed “active layer” is nearly the same as Horio’s luminescent layer 102. For example, the '626 Patent states that “[r]eferring to FIG. 18, the light emitting device comprises a light emitting layer, i.e. an N-type semiconductor layer 120, an active layer 130 and a P-type semiconductor layer 140 sequentially formed on a base substrate 110.” EX1001, 12:51-54. The '626 Patent also states that “[t]he active layer 30 has a predetermined bandgap and is a region where a quantum well is formed so that electrons and holes are recombined. ... The wavelength of light emitted through the combination of electrons and holes varies according to the kind of a material constituting the active layer 30.” EX1001, 6:22-27.



EX1007, Figure 3; EX1001, Figure 18.

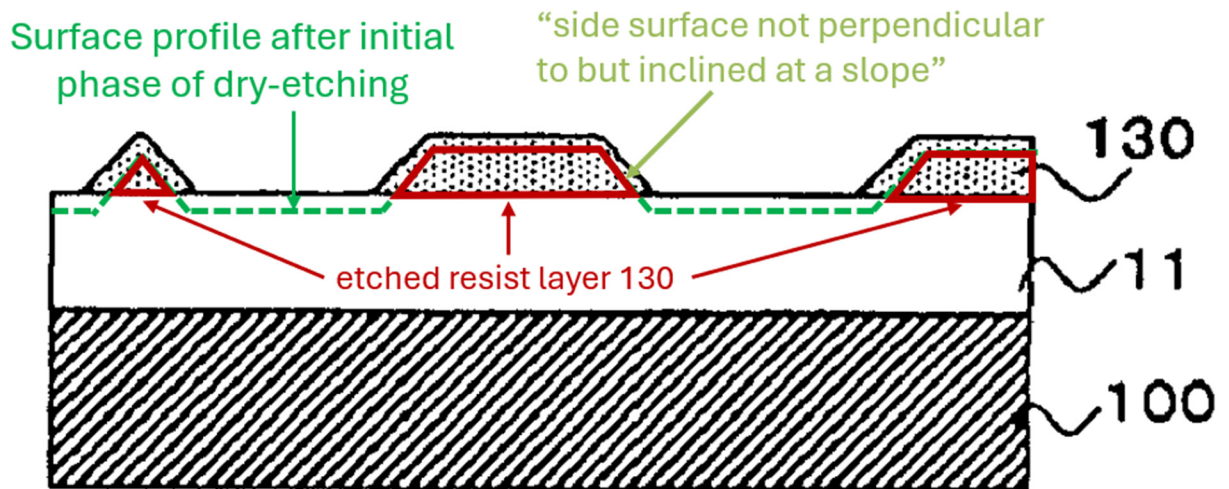
- iii. [9B] forming an **etching mask pattern**, of which a side surface is not perpendicular to but inclined at a slope from a horizontal plane, on the **P-type semiconductor layer**;
- [9D-1] wherein forming the **etching mask pattern** comprises: forming a **photoresist** on the **P-type semiconductor layer**;
- [9D-2] exposing the **photoresist** to light;
- [9D-3] **hard-baking** and **developing** the **photoresist**; and
- [9D-4] **etching** a side surface of the developed **photoresist** to have the **slope from the horizontal plane**.
- [9C] removing the **etching mask pattern** and the **P-type semiconductor layer** exposed through the **etching mask pattern**;

176. Horio teaches [9B], [9D-1]-[9D-4], and [9C].

- a. [9B] forming an **etching mask pattern**, of which a side surface is not perpendicular to but inclined at a slope from a horizontal plane, on the **P-type semiconductor layer**

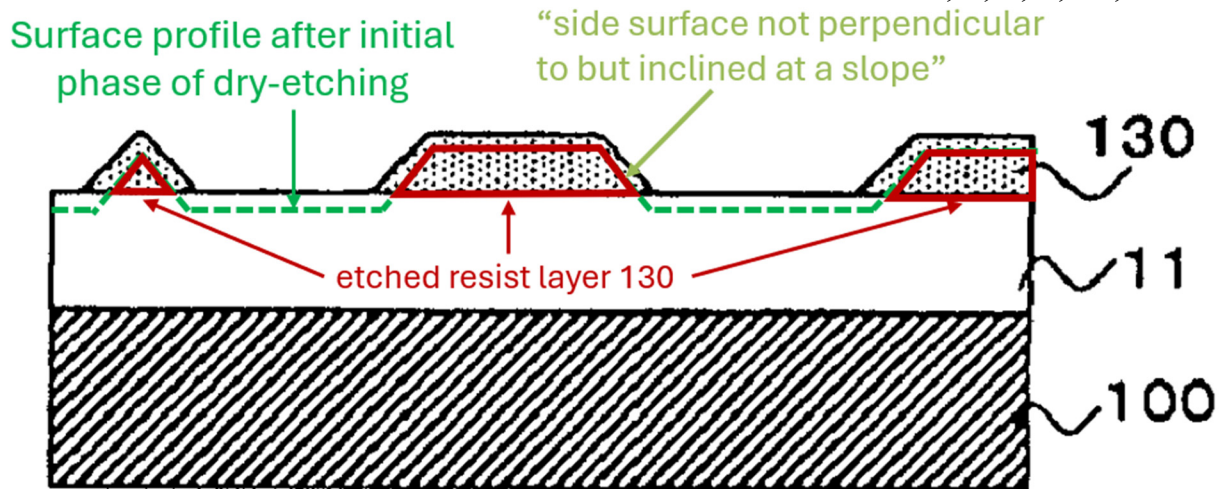
177. As I explain more fully in Section VIII.E.2.iii.b provided below, Horio discloses forming an **etched resist layer 130** as I annotated below (which corresponds

to the claimed “**etching mask pattern**”), including all requirements of the limitations [9D-1]-[9D-4].



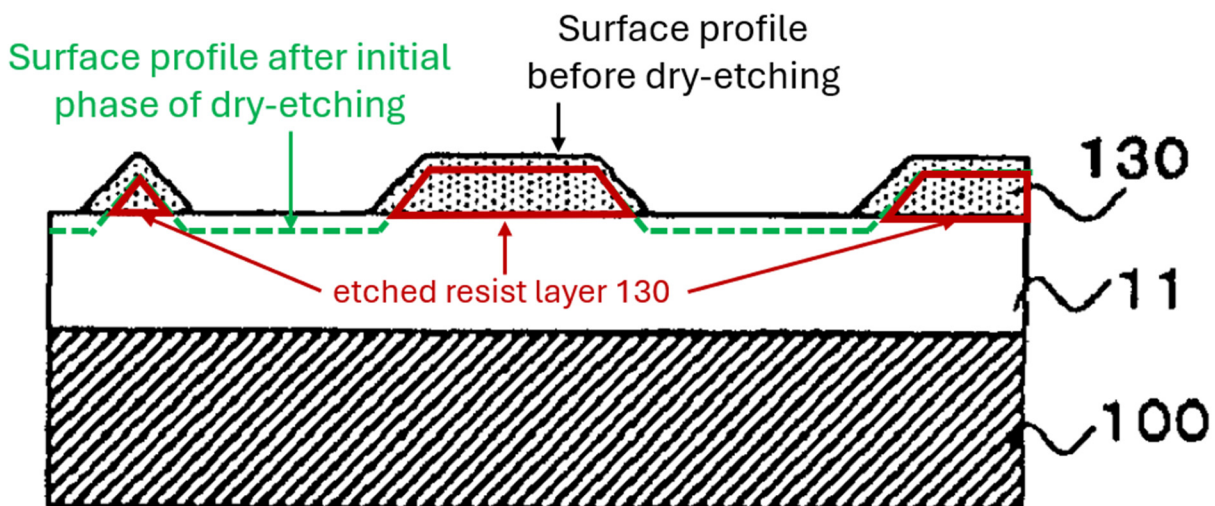
EX1007, Figure 10E (modified).

178. Horio also discloses that the **etched resist layer 130** has “a side surface [that] is not perpendicular to but **inclined at a slope** from a horizontal plane,” the **etched resist layer 130**, again, being the “**etching mask pattern**.” Specifically, as I explain below in Section VIII.E.2.iii.b(d) [Ground V, 9D-4], the initial phase of Horio’s dry-etching step etches the resist layer 130 while providing the **slope** on the side surfaces from the horizontal plane formed by the top surface of the semiconductor layer 11.



EX1007, Figure 10E (modified).

179. In addition, Horio teaches providing the **etched resist layer 130** “on the **P-type semiconductor layer.**” The semiconductor layer 11 includes as the top layer the **p-type semiconductor layer 103** (as described in Section VIII.E.2.ii [Ground V, 9A]), and the **etched resist layer 130** is formed on top of the semiconductor layer 11, as illustrated below. EX1007, [0077]-[0079].



EX1007, Figure 10E (modified).

b. “forming an etching mask pattern” Pursuant To [9D-1]-[9D-4]

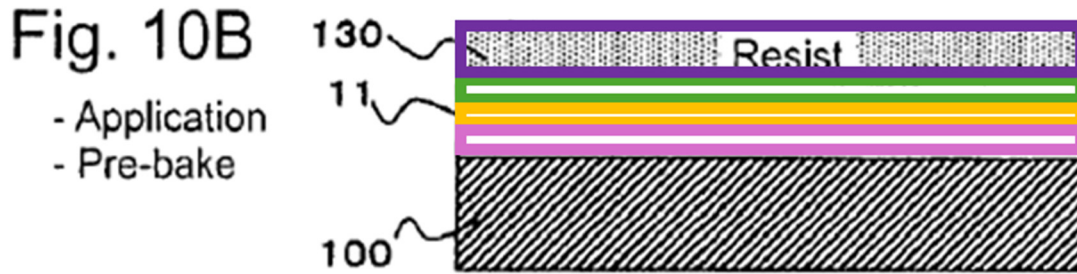
180. As explained below, Horio teaches “forming an etching mask pattern” and all the associated details in limitations [9D-1]-[9D-4], as explained below.

(a) [9D-1] “forming a photoresist on the P-type semiconductor layer;”

181. Horio discloses depositing a resist layer 130 on a nitride semiconductor layer. EX1007, Figure 10B. For example, Horio states “[t]o be more specific, a resist is evenly applied to the wafer-shaped substrate 100 in which the nitride semiconductor layer 11 is formed in advance by use of a spin coater. After a resist coating layer is formed, a resist layer 130 is formed by pre-baking (FIGS. 10A and 10B).” EX1007, [0079]. The p-type semiconductor layer is located on the uppermost layer of semiconductor layer 11, as explained in VIII.E.2.ii [Ground V, 9A] EX1007, [0054], [0079], [0088].

[0079] To be more specific, a resist is evenly applied to the wafer-shaped substrate 100 in which the nitride semiconductor layer 11 is formed in advance by use of a spin coater. After a resist coating layer is formed, a resist layer 130 is formed by pre-baking (FIGS. 10A and 10B). In the prebaking, temperature is lower and time is longer (for example, 90 degrees centigrade and 120 seconds) than those in a condition recommended by a maker of the used resist (for example, 100 degrees centigrade and 60 seconds). In this embodiment, a heat-resistant g-line positive resist (trade name: AZ6130, made by Clariant (Japan)K.K.) which is suitable for the dry etching process can be used.

EX1007, [0079].



EX1007, Figure 10B.

182. Horio states that in one example, the resist layer 130 is “a heat-resistant g-line positive resist (trade name: AZ6130, made by Clariant (Japan)K.K.).”

EX1007, [0079]. It was well known that AZ6130 from Clariant is a photoresist.

EX1021, 2 (“patterning of the photoresist (AZ6130, Clariant)”).

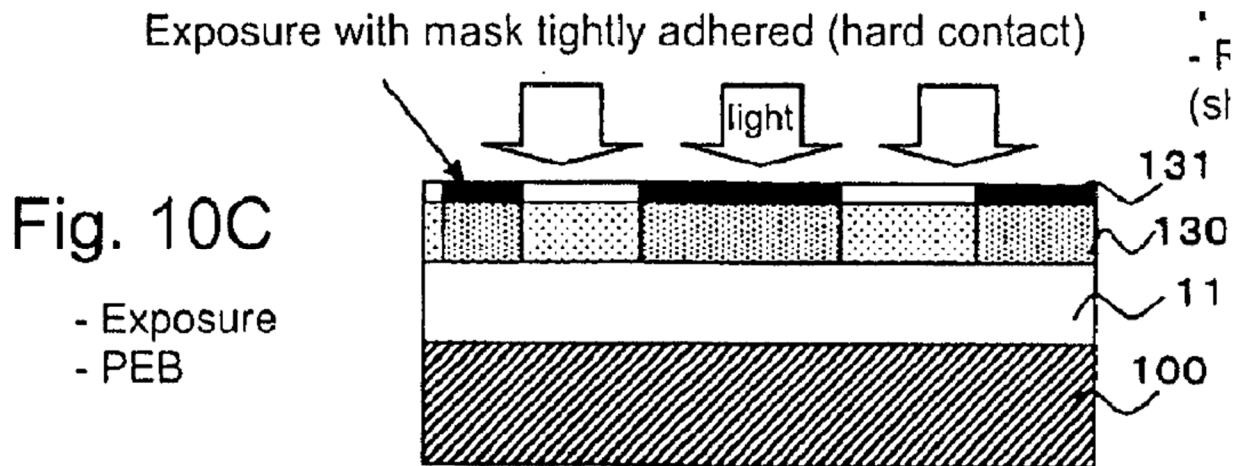
(b) [9D-2] “exposing the photoresist to light;”

183. Horio teaches using a photomask to selectively expose the resist layer 130 to light. For example, Horio states “[t]hen, a photomask for transferring a pattern and the substrate 100 with the resist layer 130 as shown in FIG. 10B are set on the mask aligner, to carry out contact exposure (hard contact) (FIG. 10C).” EX1007, [0080]. In Figure 10C, Horio expressly illustrates, using a label, that “light” is exposed to the resist layer 130.

[0080] *Then, a photomask 131 for transferring a pattern and the substrate 100 with the resist layer 130 as shown in FIG. 10B are set on the mask aligner, to carry out contact exposure (hard contact) (FIG. 10C). After the exposure, post exposed bake*

(hereinafter abbreviated as PEB) which is not included in the conditions recommended by the maker is carried out on a condition of 110 degrees centigrade and 120 seconds. After that, development is carried out by use of a developing solution (trade name: AZ300MIF, made by Clariant(Japan)K.K.), and the resist layer 130 in exposed portions are removed (FIG. 10D). At this stage, end portions of the resist layer 130 vertically rise.

EX1007, [0080].



EX1007, Figure 10C.

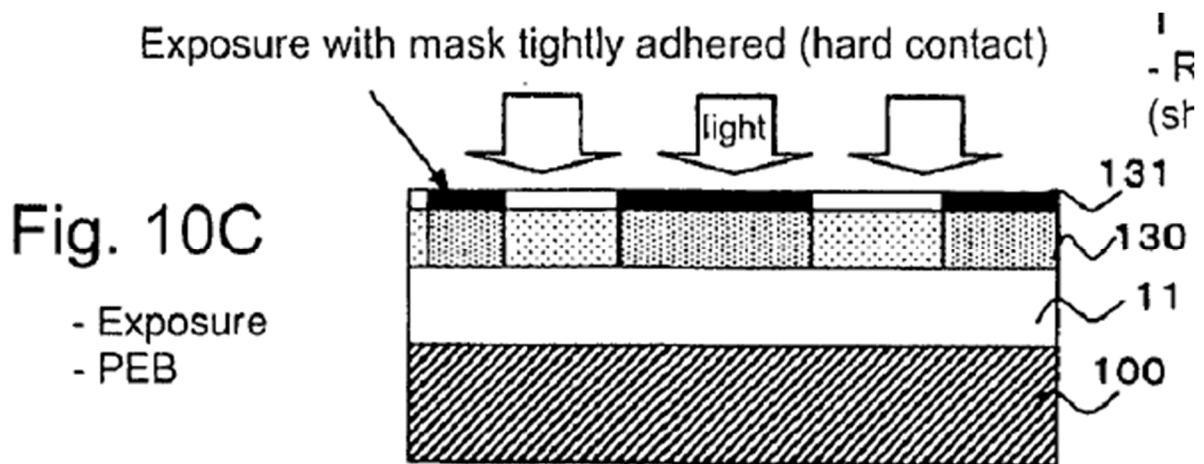
(c) [9D-3] “hard-baking and developing the photoresist; and”

184. Horio discloses developing the photoresist, as explained below. In addition, Horio teaches **baking** the photoresist before *and* after the development step. Because there is no temporal requirement in [9D-3] between the “**hard-baking**” step and the “**develop[ment]**” step, either or both **baking** steps meet the claimed “**hard-baking**” limitation.

185. In particular, Horio teaches that the **resist layer 130** is exposed to light and after the exposure, the **resist layer 130** undergoes a “*post exposed bake (hereinafter abbreviated as PEB)*,” which “is carried out on a condition of *110 degrees centigrade* and 120 seconds.” EX1007, [0080], Figure 10C.

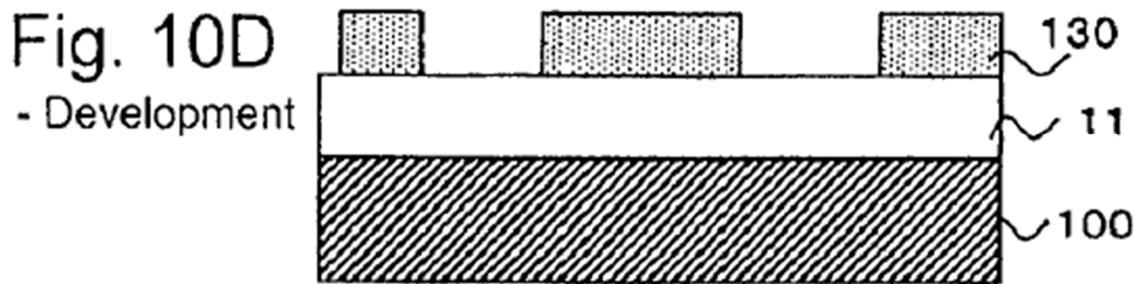
[0080] Then, a photomask 131 for transferring a pattern and the substrate 100 with the resist layer 130 as shown in FIG. 10B are set on the mask aligner, to carry out contact exposure (hard contact) (FIG. 10C). *After the exposure, post exposed bake (hereinafter abbreviated as PEB)* which is not included in the conditions recommended by the maker is *carried out on a condition of 110 degrees centigrade and 120 seconds*. After that, development is carried out by use of a developing solution (trade name: AZ300MIF, made by Clariant(Japan)K.K.), and the resist layer 130 in exposed portions are removed (FIG. 10D). At this stage, end portions of the resist layer 130 vertically rise.

EX1007, [0080].



EX1007, Figure 10C.

186. Subsequent to the **post exposure bake (PEB)**, Horio discloses that “**development** is carried out by use of a developing solution (trade name: AZ300MIF, made by Clariant(Japan)K.K.), and the **resist layer 130 in exposed portions are removed** (FIG. 10D).” EX1007, [0080]. As such, Horio discloses “**developing** the **photoresist**.”



EX1007, Figure 10D.

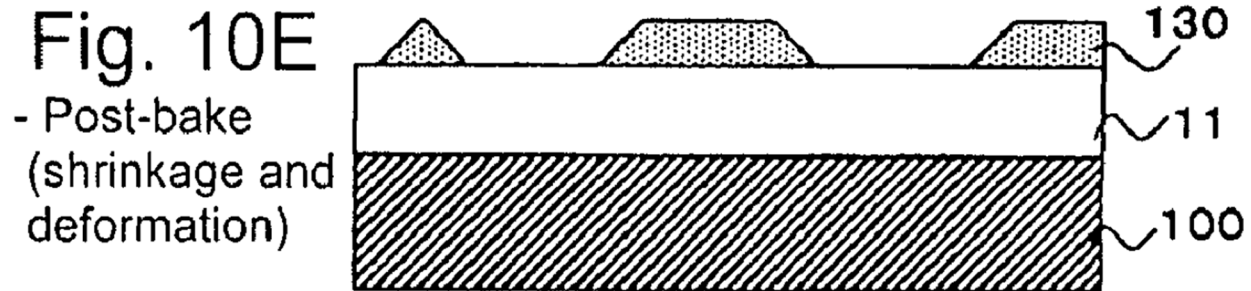
187. After development, a “**post bake**” is carried out as shown in Figure 10E, which is another **bake** for the **resist layer 130**. EX1007, [0080]-[0081]. Depending on the targeted side surface slope of **resist layer 130**, the **post bake is carried out at different temperatures, e.g., a temperature within the range of 110 to 120° C.**

To be more specific, the end portions of the **resist layer 130** incline at an inclination angle of 55 degrees on a **post bake** condition of **110 degrees centigrade** and 120 seconds. The inclination angle becomes 45 degrees on a **post bake** condition of **115 degrees centigrade** and 120 seconds, and the inclination

angle becomes 35 degrees on a **post bake** condition of **120**

degrees centigrade and 120 seconds.

EX1007, [0081].



EX1007, Figure 10E.

188. Both the **PEB** step and the **post bake** step meet the “hard baking” limitation because the temperature range of the **PEB** step and the temperature range of the **post bake** step each overlap with the temperature range of **hard baking** required by claim 15: “performed at a temperature of 100 to 140°C.” EX1001, claim 15. EX1007, [0080] (**PEB** occurring at “110°C”); [0081] (**post bake** occurring at “110°C”, “115°C”, or “120°C”).

(d) [9D-4] “**etching** a side surface of the developed **photoresist** to have the **slope** from the horizontal plane.”

189. As background, the '626 Patent discloses that “if the **photoresist** is hard-baked at a temperature of 100 to 140° C. and then developed, the side surface of the developed **photoresist** may be **etched** to have a slope of 80 to 20° from a horizontal plane.” EX1001, 7:24-27. To the extent 7:24-27 of Horio quoted above discloses a

single etching step that performs both the “etching” step of [9D-4] and the “removing” step of [9C], Horio discloses [9D-4] as explained below.

190. Horio teaches a dry-etching step that etches both the developed resist layer 130 and the lower semiconductor layer simultaneously. As an example, subsequent to developing resist layer 130, “the *substrate with the resist layer 130* that has end faces which are inclined as shown in FIG. 10E is *set on an RIE (reactive ion etching)* device.” EX1007, [0082]. As it was well known in the art, RIE is one of the widely used anisotropic (e.g., directional) dry-etching technique that etches exposed surfaces by bombarding accelerated reactive ions onto the exposed surfaces. EX1023, 2, 4.

191. Horio explains that the “selection ratio [between the resist layer 130 and the semiconductor layer 11] of this dry etching is approximately 1.” EX1007, [0082]. Thus, the dry etching step etches the semiconductor layer 11’s exposed portion and the developed resist layer 130 simultaneously.

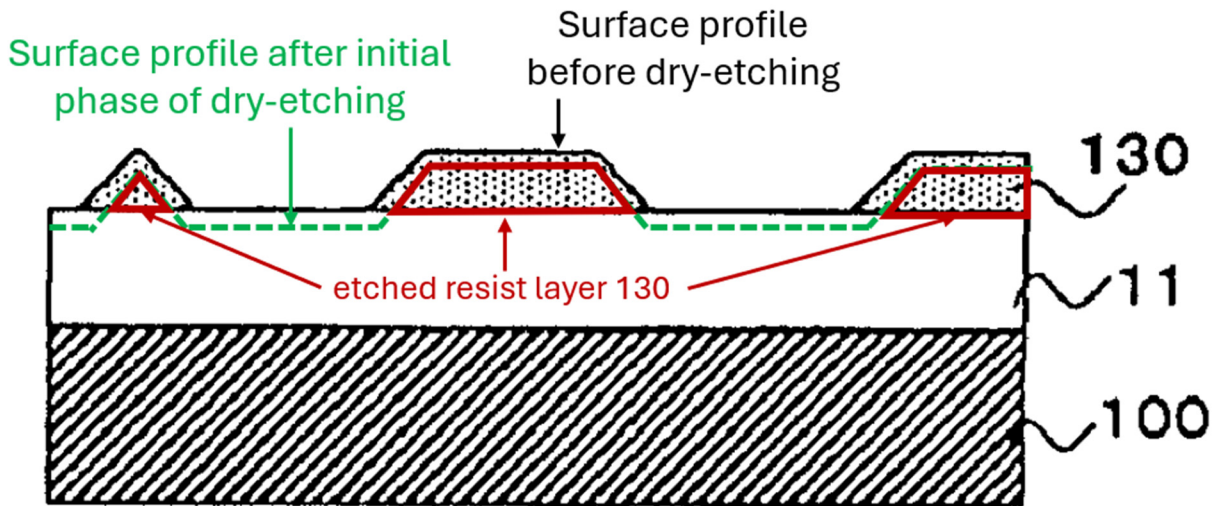
[0082] Then, *the substrate with the resist layer 130 that has end faces which are inclined as shown in FIG. 10E is set on an RIE (reactive ion etching) device, to etch the nitride semiconductor layer 11 up to a predetermined depth by dry etching using a chlorine gas (FIG. 10F).* The selection ratio of this dry etching is approximately 1, and the end faces of the nitride semiconductor layer 11 are formed into an inclination angle which is determined by the inclination angle of the resist layer 130 and the selection ratio. For example, when the *selection ratio is 1, the inclined shape of the resist layer 130 is transferred to*

the nitride semiconductor layer 11. When the etching speed of the resist layer 130 is faster than that of the semiconductor layer 11, the inclination angle of the nitride semiconductor layer 11 with respect to the sapphire substrate 100 becomes small (shallow). When the etching speed of the resist layer 130 is slower than that of the semiconductor layer 11, the inclination angle of the nitride semiconductor layer 11 becomes large.

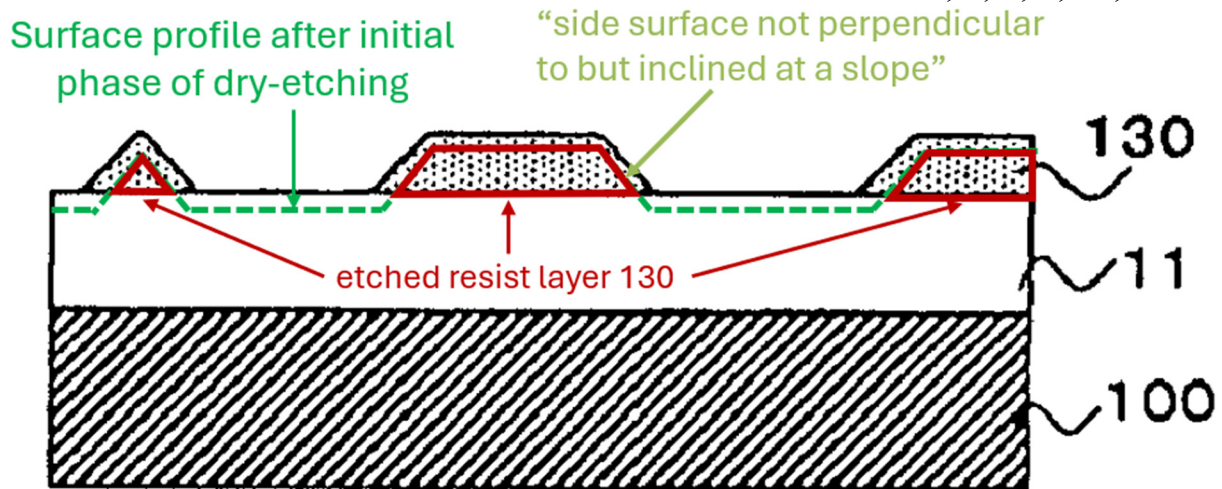
EX1007, [0082].

192. Put another way, the **RIE dry-etching step** disclosed by Horio causes the exposed nitride semiconductor layer 11 and the developed **resist layer 130** to be etched at the same time. EX1007, [0086]. And the **RIE dry-etching** causes all exposed surfaces to be etched, including the developed **resist layer 130's** side surfaces.

193. Now, focusing specifically on the *initial phase* of Horio's **dry-etching** step, that *initial phase* of **dry-etching** etches all exposed surfaces of the developed **resist layer 130** primarily in the vertical direction. See EX1022, [0227]-[0234], Figures 20A-20B. Accordingly, the *initial phase* of **dry-etching** vertically etches away a small portion of all exposed surfaces, including the developed **resist layer 130**, as illustrated below.



194. During this initial phase of **dry-etching**, the side surface of the developed **resist layer 130** is etched “to have the **slope** from the horizontal plane.” For example, as explained in Section VIII.C.3.ii [Ground V, 9D-3] and as shown in Figure 10E, the developed **resist layer 130** has **sloped side surfaces**. EX1007, [0081], [0084] (“[I]t is possible to **incline the end portions of the resist layer 130** with high reproducibility at an angle corresponding to the post bake condition ... ”); [0085]. Subsequently, the initial phase of **dry-etching** etches away the upper exposed portions of the developed pattern **resist layer 130** mostly in the vertical direction so that the **resist layer 130** has the **slope** on the side surface, as shown below. *See* EX1022, [0227]-[0234], Figures 20A-20B.



EX1007, Figure 10E (modified).

195. The resulting product, which is the developed **resist layer 130** that has gone through the initial phase of Horio’s **dry-etching**, is referred to as the “**etched resist layer 130**.” The “**etched resist layer 130**” is an **etching mask pattern**, since the **etched resist layer 130** is also utilized to mask the p-type layer from the remaining dry-etching. EX1007, [0082], Figure 10F. *See also* Section VIII.E.2.iii.c [Ground V, 9C].

c. [9C] removing the **etching mask pattern** and the **P-type semiconductor layer** exposed through the **etching mask pattern**;

196. Horio teaches [9C]. After the initial phase of the dry-etching step, the **etched resist layer 130** and the **P-type semiconductor layer** exposed through the **etched resist layer 130** continue to be removed by the remaining portion of the dry etching step.

197. In particular, Horio teaches that even after creating the **etched resist layer 130**, “the *nitride semiconductor layer 11 in the open portions* [including the **p-type layer 103** exposed through the **etched resist layer 130**] is etched to a predetermined depth of the terrace 125 by use of a dry etching technology. Thus, the *p-type nitride semiconductor layer 103*, the luminescent layer 102, and a part of the n-type nitride semiconductor layer 101 are *removed* (FIG. 10F).” EX1007, [0089]; [0082], Figure 10E.

[0089] First, portions to be the contour grooves 120, the external frame partition grooves 122, and the light emitting device region partition grooves 123 are opened by use of a photolithographic technology. A mask of a resist layer 130 in which the edges of open portions are inclined at a predetermined angle is formed by processes of FIGS. 10A to 10E. Then, *the nitride semiconductor layer 11 in the open portions is etched to a predetermined depth of the terrace 125 by use of a dry etching technology*. Thus, the p-type nitride semiconductor layer 103, the luminescent layer 102, and a part of the n-type nitride semiconductor layer 101 are removed (FIG. 10F). At this time, since the edges of the open portions of the mask of the resist layer 130 are inclined, the edges of the etched nitride layer 11 are inclined too. The resist is removed by cleaning (FIG. 10G), so that the contour grooves 120, the external frame partition grooves 122, and the light emitting device region partition grooves 123 are formed in such a depth as to expose the n-type nitride semiconductor layer 101. EX1007, [0089].

198. And for the reasons provided in Section VIII.E.2.iii.b(d) [Ground V, 9D-4], the **etched resist layer 130** is etched by the remaining dry-etching step.

EX1007, [0082], [0086]. Through the continued dry-etching, “the inclined shape of the **resist layer 130** is transferred to the nitride semiconductor layer 11.” EX1007, [0082]. As such, some portions of the **etched resist layer 130** are removed by the remaining dry-etching step.

[0082] Then, the substrate with the resist layer 130 that has end faces which are inclined as shown in FIG. 10E is set on an RIE (reactive ion etching) device, to etch the nitride semiconductor layer 11 up to a predetermined depth by dry etching using a chlorine gas (FIG. 10F). The selection ratio of this dry etching is approximately 1, and the end faces of the nitride semiconductor layer 11 are formed into an inclination angle which is determined by the inclination angle of the resist layer 130 and the selection ratio. *For example, when the selection ratio is 1, the inclined shape of the resist layer 130 is transferred to the nitride semiconductor layer 11.* When the etching speed of the resist layer 130 is faster than that of the semiconductor layer 11, the inclination angle of the nitride semiconductor layer 11 with respect to the sapphire substrate 100 becomes small (shallow). When the etching speed of the resist layer 130 is slower than that of the semiconductor layer 11, the inclination angle of the nitride semiconductor layer 11 becomes large.

EX1007, [0082].

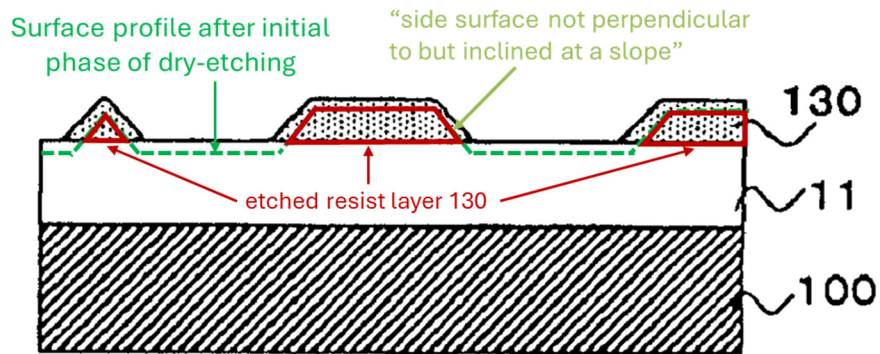
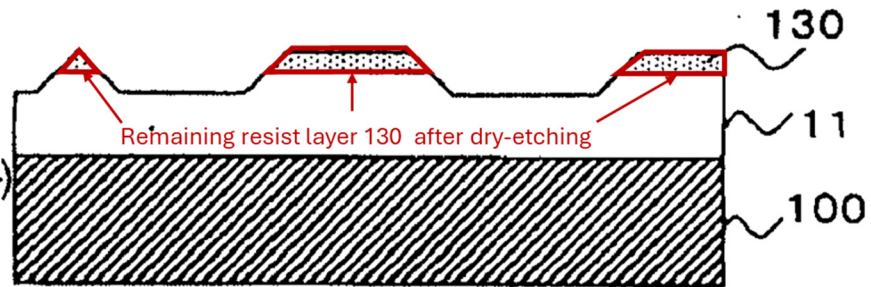


Fig. 10F
- RIE etching
(shape-transfer)



EX1007, Figures 10E(modified)-10F.

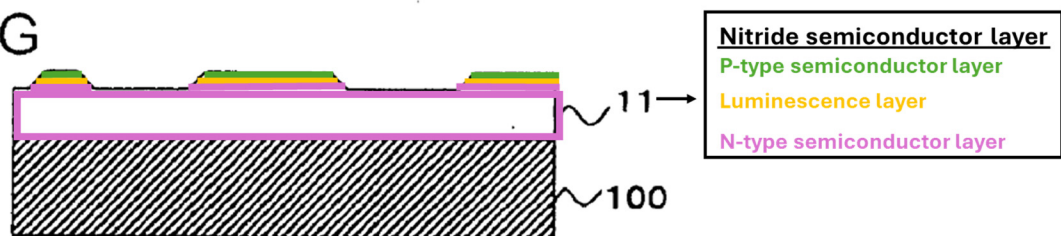
199. After completing the dry-etching, “[t]he **resist layer 130** is removed by dissolving, and cleaned lastly,” as shown in Figure 10G. EX1007, [0083]; [0089].

[0083] *The resist layer 130 is removed by dissolving, and cleaned lastly.* Therefore, the nitride semiconductor layer 11 is processed into a shape located above the terrace 125.

EX1007, [0083].

Fig. 10G

- Cleaning



EX1007, Figure 10G.

200. As such, the remaining dry-etching step along with the resist cleaning step or the remaining dry-etching step alone teaches removing the claimed “**etching mask pattern**” (“**etched resist layer 130**”) and the claimed “**P-type semiconductor layer**” (“**p-type nitride semiconductor layer 103**”) exposed through the **etched resist layer 130**.

3. Claim 13

- i. [13] The method as claimed in claim 9, wherein the **photoresist** with a thickness of 3 to 50 μm is used in the forming the **etching mask pattern**.

201. Horio teaches [13]. Horio teaches that the **resist layer 130** has a thickness of “*approximately 10 μm ,*” which is used to create the **resist layer 130** in Figure 10B, and the **resist layer 130** is then used to form the **etched resist layer 130** (the claimed **etching mask pattern**). EX1007, [0085], Figures 10B-F. *See also* Section VIII.E.2.iii.b(d) [Ground V, 9D-4].

[0085] In the foregoing method for forming the resist layer 130, a contact exposure method (hard contact) is used. Thus, the pattern transfer precision of the photomask 131 is high, and a pattern is not misaligned during the exposure. A nitride semiconductor wafer laminated on a different type of substrate (sapphire) is slightly warped convexly or concavely because of difference in lattice constants (Δa) and difference in thermal expansion coefficients. However, warpage is corrected by pressing the photomask, so that the misalignment of the pattern does not occur. Furthermore, in contrast to a method with an apart photomask, the misalignment of the inclination angle due to exposure intensity and time does not occur. Furthermore, it is

possible to form the inclination angle of the end portions of the resist layer with high reproducibility by only Selecting the post bake condition. If the resist layer 130 is thick, the inclination angle depends on only the temperature and time of the post bake. Thus, the condition can be easily set. *As to the resist layer 130 having a thickness of approximately 10um, it is possible to form the inclined resist layer 130 without problem.*

EX1007, [0085].

4. Claim 15

- i. [15] The method as claimed in claim 9, wherein the hard-baking is performed at a temperature of 100 to 140° C.

202. Horio teaches [15]. As described above in Section VIII.E.2.iii.b(c) [Ground V, 9D-3], Horio teaches that the resist layer 130 (the claimed photoresist) is hard-baked at a temperature of 100 to 140° C. As an example, Horio describes a “post exposed bake,” which is carried out at a temperature of 110° C (EX1007, [0080], Figure 10C), and a “*post bake*,” which is carried out at a temperature of 110°C, 115°C, or 120°C (EX1007, [0080]-[0081], Figure 10E). As such, the both the post bake step and/or the post exposed bake step disclose hard-baking the resist layer 130, and, thus, the hard-baking is performed at a temperature of 100 to 140° C.

To be more specific, the end portions of the resist layer 130 incline at an inclination angle of 55 degrees on a post bake condition of *110 degrees centigrade* and 120 seconds. The inclination angle becomes 45 degrees on a post bake condition of *115 degrees centigrade* and 120 seconds, and the inclination

angle becomes 35 degrees on a **post bake** condition of **120 degrees centigrade** and 120 seconds.

EX1007, [0081].

IX. Conclusion

203. Accordingly, it is my opinion that claims 1, 3, 7, 9, 13, and 15 of the '626 Patent are unpatentable.

X. Availability for Cross-Examination

204. In signing this declaration, I acknowledge that this declaration will be filed before the Patent Trial and Appeal Board of the United States and Patent Office as evidence for a case. I also acknowledge that I may be subject to cross-examination in that case and that cross examination will occur in the United States. If I am required to submit to cross-examination, I will appear for cross-examination within the United States during the time allotted for cross-examination.

XI. Right to Supplement

205. I reserve the right to supplement my opinions in the future to consider any new information as it becomes available to me and to respond to any arguments that the Patent Owner may raise.

XII. Jurat

206. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false

Declaration of Dr. Ioannis Kymissis

U.S. Patent No. 7,951,626

Claims 1, 3, 7, 9, 13, and 15

statements and the like so made are punishable by fine or imprisonment, or both,

under Section 1101 of Title 18 of the United States Code.

CLAIMS AT ISSUE

Claim 1

[1Pre] A method of manufacturing a light emitting device, comprising:

[1A] sequentially forming an N-type semiconductor layer, active layer, and P-type semiconductor layer on a substrate;

[1B] forming an etching mask pattern, of which a side surface is not perpendicular to but inclined at a slope from a horizontal plane, on the P-type semiconductor layer; and

[1C] removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern,

[1D-1] wherein forming the etching mask pattern comprises: forming a photoresist on the P-type semiconductor layer;

[1D-2] wherein forming the etching mask pattern comprises: ... exposing the photoresist to light; and

[1D-3] wherein forming the etching mask pattern comprises: ... developing the light-exposed photoresist without a baking process after the light exposure.

Claim 3

[3] The method as claimed in claim 1, further comprising the step of flip-chip bonding the substrate onto an additional submount substrate after the step of removing the P-type semiconductor layer and the etching mask pattern.

Claim 7

[7] The method as claimed in claim 1, wherein the photoresist with a thickness of 3 to 50 μm is used in the forming the etching mask pattern.

Claim 9

[9Pre] A method of manufacturing a light emitting device, comprising:

[9A] sequentially forming an N-type semiconductor layer, active layer, and P-type semiconductor layer on a substrate;

[9B] forming an etching mask pattern, of which a side surface is not perpendicular to but inclined at a slope from a horizontal plane, on the P-type semiconductor layer; and

[9C] removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern,

[9D-1] wherein forming the etching mask pattern comprises: forming a photoresist on the P-type semiconductor layer;

[9D-2] wherein forming the etching mask pattern comprises: ... exposing the photoresist to light;

[9D-3] wherein forming the etching mask pattern comprises: ... hard-baking and developing the photoresist; and

[9D-4] wherein forming the etching mask pattern comprises: ... etching a side surface of the developed photoresist to have the slope from the horizontal plane.

Claim 13

[13] The method as claimed in claim 9, wherein the photoresist with a thickness of 3 to 50 μm is used in the forming the etching mask pattern.

Claim 15

[15] The method as claimed in claim 9, wherein the hard-baking is performed at a temperature of 100 to 140°C.

APPENDIX A

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EDUCATION

Ph.D. in Electrical Engineering and Computer Science, May 2003
Massachusetts Institute of Technology, Cambridge, MA
Thesis title: Field Emission from Organic Materials
Advisor: Prof. Akintunde I. Akinwande

M.Eng. in Electrical Engineering and Computer Science, May 1999
Massachusetts Institute of Technology, Cambridge, MA
Thesis title: Morphology and Performance in Pentacene
Advisor: Prof. Akintunde I. Akinwande
Co op with IBM Research Laboratories, Yorktown Heights, NY

S.B. in Electrical Engineering and Computer Science, May 1998
Massachusetts Institute of Technology, Cambridge, MA

EMPLOYMENT

**Vice Dean of Infrastructure and
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Columbia Engineering**

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**Department Chair
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**Columbia University
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**Kenneth Brayer Professor
Electrical Engineering**

**Columbia University
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2006 present**

PI, the Columbia Laboratory for Unconventional Electronics (CLUE).

Technical consultant/Senior engineer

**QDVision, Inc. (Now Samsung
Electronics)
Watertown, MA
2005 2006**

Assisted the technical launch of the company. Built out facilities, interviewed, hired, and trained initial staff, developed the core processes and demonstration vehicles for the company. Acquired by Samsung Electronics, the company's technology is part of the QLED display platform.

Postdoctoral Associate
Laboratory for Organic Optics and
Electronics

MIT
Cambridge, MA
2003 2006

Advisor: Vladimir Bulovic.

Research Assistant
Microsystems Technology
Laboratory

MIT
Cambridge, MA
1999 2003

Thesis: Field Emission from Organic Semiconductors. Advisor: Tayo Akinwande

Summer Intern
IBM Research, Tokyo Research Lab

Yamato, Japan
Summer 1999

Developed a new characterization technique for analyzing ion density in liquid crystals and susceptibility of display alignment materials to charging and PDLC display systems. Advisor: Yoichi Taira

Co-op Student
IBM Research, T. J. Watson
Research Lab

Yorktown Heights, NY
1996-1999

Led several aspects of the organic field effect transistor effort, most notably developing a photolithographic process for fabricating transistors and investigating the role of semiconductor crystallization on macroscopic performance parameters. Also worked on a program on screen printable high K dielectrics and novel lead free soldering systems. (Three assignments, Summer 1996, 1997, June 1998 January 1999). Advisors: Christos Dimitrakopoulos and Sampath Purushothaman

AWARDS

2022 Fellow, Optica
2021 Fellow, IEEE
2021 Outstanding Volunteer Award 2021 by IEEE Kolkata Section
2019 Kenneth Brayer Professorship, Columbia University
2019 IEEE EDS Distinguished Lecturer
2018 40 under 40, Greek America Foundation
2018 Fellow, Society for Information Display
2017 Architizer A+ Award (Radiator Labs)
2016 Finalist, Verizon Powerful Answers Award (Chromotion)
2015 Winner, Verizon Powerful Answers Award (Radiator Labs)
2014 National Academy of Engineering, Frontiers of Engineering Education Meeting Attendee
2014 National Academy of Engineering, Indo American Frontiers of Science Meeting Attendee
2014 Popular Science, Invention of the Year (Radiator Labs)
2013 IBM faculty award
2012 Interdigital Innovation Challenge, first prize
2012 MIT/USDOE Clean Energy Prize, first prize
2011 Ocean Optics Blue Ocean Award
2011 Kim Award for Undergraduate Involvement
2010 IBM Faculty award
2009 Vodafone Americas Foundation Wireless Innovation Award
2008 Google faculty award

	2007 NSF CAREER award 2002 IVMC Shoulders Gray Spindt award 1998 2002 IBM Fellowship 2002 IBM Research First Plateau 2002 IBM Outstanding Technical Achievement Award 2000 2002 IBM Invention Achievement Award 1997 Tau Beta Pi, Eta Kappa Nu 1994 1998 National Merit Scholar
BEST PAPER/POSTER AWARDS	2023 CMOC Best poster award 2021 IDW MEET Best Paper Award 2020 IEEE Xplore Highlight Paper 2018 International Symposium on Wearable Computers, 20 Year Impact Award 2018 IDW Distinguished Paper Award 2018 CMOC Best poster award 2015 IDW Distinguished Paper Award 2015 NYC Media Lab Best Demo award 2014 FlexTech Alliance, second place best poster 2014 Global Interposer Technology Conference, second place best poster 2013 IGERT workshop on Energy, Transportation, and Water Infrastructure 3rd place poster 2012 MRS Fall Meeting Best Poster finalist 2011 ACM SenSys'11 Best Student Demo Award 2011 IEEE Communications Society Award, Best Paper 2002 IEEE Electron Device Society Paul Rappaport Award
ADVISORY POSITIONS	Tangible Co founder and technical advisor. BOD member. Solchroma SAB member Chromation Co founder and CTO. BOD member. Radiator Labs Co founder and technical advisor. BOD member. Lumiode Co founder and interim CEO. BOD member. Lelantos Co founder and technical advisor. BOD member.
BOOK / BOOK CHAPTERS	Ioannis Kymissis (monograph). <i>Organic Field Effect Transistors: Theory, Fabrication and Characterization</i> Springer, New York, 2009. Lamport ZA, Cavallari MR, Kymissis I. Large Area Flexible Organic Field effect Transistor Fabrication. Flexible Flat Panel Displays. 2023 Feb 14:47-66.
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SHORT COURSES

- (invited) SID Short course on MicroLED (Aug 2021)
- (invited) SID Seminar on MicroLED (Aug 2020)
- (invited, short course) SID Short Course on MicroLED, San Jose, CA, May 2019
- (invited) University of Bologna Summer School on Physical Sensing and processing; July 2019
- IEEE Expert Now online short course on organic field effect transistors (2006)

CONFERENCE PRESENTATIONS/ POSTERS/ DEMOS

- (invited) IDW 2022
- (invited, plenary) IEEE ECTC
- (invited) MRS Spring 2022
- (invited) ICDT invited presentation (TBD) (June 2021)
- (Invited, plenary) IEEE EDS Mini Colloquium on Photonics and Photovoltaics (Spain chapter) June 2020
- (Invited, plenary) IEEE EDS Brazil Chapter Seminar, Electronics on Anything, August 2020
- (invited, plenary) SID LA one day conference on Advanced Displays, Los Angeles, CA; February 2020
- (invited, plenary) MicroLED Display Summit, Nanjing China, December 2019

(invited, plenary) IEEE Frontiers In New Emerging Technology 2019 (FINE TECH) ; August 2019

(invited, plenary) IEEE EDSSC, Xi'an China, June 2019

Characterizing Image Retention for HDR OLED Displays SID Display Week 2020

Micro LED Defect Analysis via Photoluminescent and Cathodoluminescent Imaging, SID Display Week 2020

A brief survey of MicroLED Technologies, SID Display Week 2020

Bahamonde JA, Krishnaswamy H, Kymissis I. A Tunable Surface Acoustic Wave Device on Zinc Oxide via acoustoelectric interaction with AlGa_N/Ga_N 2DEG. InConference digest 2019 Jun.

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(Invited) IDW 2018, Nagoya, Japan

(Invited, plenary) INMS 2018, Hamamatsu, Japan

(invited, plenary) Second annual workshop on MicroLED, Shenzhen China

Diagnosing SLE Arthritis with Dynamic Diffuse Optical Spectroscopy 2018 ACR/ARHP Annual Meeting

Kim Y, Marone A, Thompson SM, Sowah JN, Shulevitz HJ, Kim HK, Kymissis I, Hielscher AH. Conformable, Wearable and Scalable Imaging Bands for Assessing Joints Diseases. InMicroscopy Histopathology and Analytics 2018 Apr 3 (pp. JTh3A 34). Optical Society of America.

Colon Berrios, Aida R., Hassan Edrees, Daniel De Godoy, Peter Kinget, and Ioannis

Kymissis. "Die level processing for 3 D monolithic integration of piezoelectric MEMS on CMOS." In SOI 3D Subthreshold Microelectronics Technology Unified Conference (S3S), 2017 IEEE, pp. 1-3. IEEE, 2017.

Liang, W., Alexandrou, K., Klebanov, M., Kuo, C. C., Kymissis, I., Sundaram, K. B., Liou, J. J. (2017, July). Characterization of ESD protection devices under total ionizing dose irradiation. In Physical and Failure Analysis of Integrated Circuits (IPFA), 2017 IEEE 24th International Symposium on the (pp. 1-4). IEEE.

(Invited) Integrated Light Management as a Path to Miniaturizing Spectrometers Na dia K. Pervez, Tanya C. Garza, Michael J. Gazes, James I. Scholtz, Mark F. Comerford, and Ioannis Kymissis Imaging and Applied Optics 2017 (3D, AIO, COSI, IS, MATH, pcAOP) OSA Technical Digest (online) (Optical Society of America, 2017), paper ATh2A.3

(invited) National Research Center, Athens, Greece

(Invited) 2018 Workshop on smell sensing, AIT Tullin, Austria

(invited) ICDM 2018, "Surface treatment for OFETs" Guangzhou, China

(short course) ICDM 2018, "MicroLEDs" Guangzhou, China

(Invited) CMOC 2018, New Haven, CT

(invited) IWPSD, "X ray analysis of OFETs" New Delhi, India

(short course) IWPSD, "Quantum Dots in Displays" New Delhi, India

(Keynote, panelist) Boston HubWeek 2017

(Invited) SID Annual Symposium 2017

(Invited, plenary speaker) 2017 Hai'an Workshop on Microelectronics, Hai'an China

Colon Berrios AR, Edrees H, McGinn C, Cavallari MR, Kinget P, Kymissis I. CMOS integrated ZnO thin film bulk acoustic resonator with Si₃N₄ susceptor layer for improved IR sensitivity. Device Research Conference (DRC), 2017

Bahamonde JA, Colon AR, Krishnaswamy H, Kymissis I. Acoustoelectric amplification of surface acoustic waves on ZnO deposited on AlGaN/GaN Epi. Device Research Conference (DRC), 2017

(invited) NYC Media Lab summit 2016, presentation and workshop

(Invited) CMOC 2016, New Haven, CT

Youngwan Kim, Christopher Choi, Theodore H Schwartz, Hongtao Ma, Ioannis Kymissis "Non display MicroLED devices" 2016 SID IZone demonstration, San Francisco, CA, May 2016.

A Masurkar, I Kymissis. Comparison of top and bottom contact pentacene field effect transistors using photocurrent microscopy. Device Research Conference (DRC), 2016

Radiation hardened graphene field effect transistors. K Alexandrou, A Masurkar, H Edrees, JF Wishart, Y Hao, N Petrone, J Hone, I Kymissis. Device Research Conference (DRC), 2016

(Invited) Bioelectronics and More 2016, Wiener Neustadt, Austria.

Youngwan Kim, Christopher Choi, En Chen Chen, Andy GS Daniel, Amrita Masurkar, Theodore H Schwartz, Hongtao Ma, Ioannis Kymissis "An ultra thin implantable system for cerebral blood volume monitoring using flexible OLED and OPD," 2015 IEEE International Electron Devices Meeting (IEDM), Washington, DC, 2015, pp. 29.6.1-26.6.4.

Hurst, Adam M; Chenet, Daniel; van der Zande, Arend; Kymissis, Ioannis; Hone, James; A molybdenum disulfide piezoelectric strain gauge Nanotechnology (IEEE NANO), 2015 IEEE 15th International Conference on 1122-1125 2015 IEEE

Shyuan Yang, Ioannis Kymissis. Large scale temperature monitoring system for detection of potential ebola patient Proceedings of the 8th ACM International Conference on Pervasive Technologies Related to Assistive Environments, 7/21/15

(Invited Paper) Brian R Tull, Zeynep Basaran, Dafna Gidony, Alexander B Limanov, James S Im, Ioannis Kymissis, Vincent W Lee. High Brightness, Emissive Microdisplay by Integration of III V LEDs with Thin Film Silicon Transistors. SID Symposium Digest of Technical Papers 2015/6/1

Fabio Carta, Htay Hlaing, Hassan Edrees, Shyuan Yang, Mingoo Seok, Ioannis Kymissis. Co development of complementary technology and modified CPL family for organic digital integrated circuits. MRS Proceedings, 2015 Volume 1795 19-25

Fall MRS, Boston, MA 2015.

(invited) SPIE Optics+Photonics, San Diego, CA 2015.

(invited) Fall MRS, Boston, MA 2014.

(invited) "An Implantable System for Brain Blood Flow Monitoring Using Flexible OLEDs and OPDs." Ioannis (John) Kymissis, Amrita Masurkar, Youngwan (Willis) Kim, En Chen (Patrick) Chen, Hongtao Ma, Theodore Schwartz. USAMC 17th Biannual Bioscience review, Baltimore MD. 2014.

"BEOL Integration with excimer laser recrystallization" Fabio Carta, Ioannis Kymissis. GIT 2013 (best poster award, 2nd place)

"A printable sensor for ammonia vapors." Kalpana, Shyuan Yang, Ioannis Kymissis, Howard Katz. FlexTech 2014, Phoenix, AZ.

"Metacapacitors: Printed Capacitors for High Efficiency Power Supplies." Shyuan Yang, Ioannis Kymissis. FlexTech 2014, Phoenix, AZ. (best poster award, 2nd place)

"An Implantable System for Brain Blood Flow Monitoring Using Flexible OLEDs and OPDs." FlexTech 2014, Phoenix, AZ.

(invited) "Thin Film Electronics for Mechanical Sensing and Actuation" Ioannis Kymissis. IEEE 2014 Packaging Symposium, Binghamton, NY

“Printable, High Performance Nanoparticle/Polymer Composite Capacitors” Shyuan Yang, Barry Van Tassell, Shuangyi Liu, Eli S. Leland, Daniel A. Steingart, Stephen O’Brien, Ioannis Kymissis. Fall MRS, December 2013. Boston MA

“Low Temperature Spray Deposition of Multilayer Polymer Ceramic Composite Capacitors” Barry Van Tassell, Paul Chando, Shyuan Yang, Shuangyi Liu, Limin Huang, Stephen O’Brien, Ioannis Kymissis, Daniel A Steingart. Fall MRS, December 2013. Boston MA

“Printable Ammonia Sensor Based on Organic Field Effect Transistor” Kalpana Besar, Ana Maria Rule, Patrick N. Breyse, Ioannis John Kymissis, Howard E Katz. Fall MRS, December 2013. Boston MA

“Electrophoretic Deposition of Solution Phase Ligand Exchanged Quantum Dots and Their Application in Optoelectronic Devices” Htay Hlaing, Seung Whan Lee, Irving P Herman, Ioannis Kymissis. Fall MRS, December 2013. Boston MA

“Analysis of Optimized Photovoltaic Devices Using Impedance Spectroscopy” Jonathan Beck, James Basham, David Gundlach, Ioannis Kymissis. Fall MRS, December 2013. Boston MA

“Investigation of Photocurrent and Photogeneration in Organic Field Effect Transistors” Amrita Masurkar, Ioannis Kymissis. Fall MRS, December 2013. Boston MA

“Monolithic versus Three Terminal Tandem Photovoltaics: A Detailed Balance Comparison” Octavi Escala Semonin, Paul A George, Robert A Barton, Ioannis Kymissis. Fall MRS, December 2013. Boston MA

“Graphene Electrodes for Quantum Dot Solar Cells” Robert A Barton, Octavi E Semonin, Joshua Choi, Nicholas Petrone, Yuanda Gao, James Hone, Jonathan Owen, Ioannis Kymissis. Fall MRS, December 2013. Boston MA

“Large Area CVD Graphene as Molecular Template and Transparent Electrode for Organic Solar Cells” Htay Hlaing^{1,2}, Rob Barton¹, Theanne Schiros¹, Nicholas Petrone², James Hone^{1,2}, Ioannis Kymissis, Fall MRS, December 2013. Boston, MA.

“An implantable PVDF microphone for a totally implantable cochlear implant” Andy Zhang, Elizabeth Olson, Ioannis Kymissis. SPIE Optics+Photonics, August 2013. San Diego, CA.

“Solution Processed Organic Transistors with Chemically Modified Copper Electrodes.” Chang Hyun Kim, Htay Hlaing, Fabio Carta, Yvan Bonnassieux, Gilles Horowitz, and Ioannis Kymissis. FPI 11. June 2 11 2013, Aquitaine, France.

“Integrated CMOS Quantitative Polymerase Chain Reaction Lab on Chip,” Haig Norian, Ioannis Kymissis, Kenneth Shepard. 2013 Symposium on VLSI Circuits, to appear June 2013.

“Amorphous Silicon graphene anodes for lithium ion batteries”, Filippas Farmakis, Kostas Alexandrou, Costas Elmasides, Ioannis Kymissis and Nikolaos Georgoulas, SPIE Grenoble to appear April 2013

“Demo: An adaptive multihop network testbed for energy harvesting active networked tags (EnHANTs),” R. Margolies, L. Pena, K. Kim, Y. Kim, M.Wang, M. Gorlatova, J.

Sarik, J. Zhu, P. Kinget, I. Kymissis, and G. Zussman, in Proc. IEEE INFOCOM'13, Apr. 2013.

"Project based learning within a large scale interdisciplinary research effort," M. Gorlatova, J. Sarik, I. Kymissis, and G. Zussman, in Proc. ITiCSE 2013

"Printable, flexible, high performance capacitors for power circuit application," S. Yang, B. Van Tassell, P. Chando, C. Le, S. Liu, E. S. Leland, Conference D. A. Steingart, S. O'Brien, P. R. Kinget, I. Kymissis, , FlexTech Alliance, January 2013.

"Asymmetric Leakage in (Ba, Sr)TiO₃ Nano Particle/Parylene C Composite Capacitors," S. Yang, B. R. Tull, N. K. Pervez, L. Huang, E. S. Leland, D. Steingart, S. O'Brien, I. Kymissis, MRS Conference, Best Poster Award Nominee, November 2012.

"Metacapacitor: Flexible, low cost, high performance capacitor for power electronics" S. Yang, B. Van Tassell, P. Chando, C. Le, S. Liu, E. S. Leland, D. A. Steingart, S. O'Brien, P. R. Kinget, I. Kymissis, NY Best Conference, November 2010.

J. Sarik, C. Li, and I. Kymissis, "Fabricating electronics with rapid prototyping tools," in Proc. 6th TEI, Jan. 2012.

"Use of Subwavelength Structures to Improve Optics and Transport in Organic Photovoltaics." J. H. Beck, B. Ray, C. Tsai, R. R. Grote, R. M. Osgood, D. Englund, C. T. Black, M. A. Alam, I. Kymissis. MRS Fall 2012, Boston, MA.

"Electrostrictor with Monolithically Integrated CMOS TFT Control." Fabio Carta, Yu Jen Hsu, John Sarik, Ioannis Kymissis. CIMTEC 2012. June 10 14 2012, Montecatini Terme, Italy.

(invited) "Energy Harvesting Active Network Tags (EnHANTs)" Ioannis Kymissis. IdTechEx Energy Harvesting 2012.

"Active matrix PVDF array for thermal imaging and acoustic signal processing applications." Yu Jen Hsu, Shyuan Yang, Nadia Pervez, Ioannis Kymissis. SPIE Optics+Photonics 2012.

"High throughput pH and ion sensing via CMOS FGFET arrays" Alok Prabu, Shyuan Yang, Ioannis Kymissis, Kalle Levon. SPIE Optics+Photonics 2012.

"Fabrication and Electrochemical Characterization of Multiplexed Electrode System for DNA Biosensing. " Zeynep Basaran, Janet Lee, Marisa Buzzeo, Ioannis Kymissis. SPIE Optics+Photonics 2012.

"Evaluating Photovoltaic Performance Indoors," Y. Afsar, J. Sarik, M. Gorlatova, G. Zussman, I. Kymissis, in Proc. 2012 IEEE Photovoltaic Specialist Conference, Austin, TX, June 2012.

(Invited) "An Active Matrix Microphone." Ioannis Kymissis, Y. Hsu. ISDRS 2011.

"Electrical readout of photochromic state." Hassan Edrees, Nadia Pervez, Ioannis Kymissis. SPIE Optics+Photonics 2011.

"Sequential Lateral Solidification of Silicon on Low K Dielectrics for 3D Integrated

Circuits,” V.W. Lee, G.S. Ganot, A.B. Limanov, J.S. Im, I. Kymissis. T5.20, Materials Research Society Fall Meeting 2011.

“Method for Efficient Droplet Extraction from Covered Droplet in Oil Electrowetting on Dielectric Devices.” Haig Norian, Ioannis Kymissis and Kenneth Shepard; MRS Fall Meeting 2011.

“Demo: prototyping UWB enabled enhants.” Jianxun Zhu, Gerald Stanje, Robert Margolies, Maria Gorlatova, John Sarik, Zainab Noorbhaiwala, Paul Miller, Marcin Szczodrak, Baradwaj Vigraham, Luca Carloni, Peter Kinget, Ioannis Kymissis, and Gil Zussman. In Proceedings of the 9th international conference on Mobile systems, applications, and services (MobiSys '11). ACM, New York, NY, USA, 387 388. DOI=10.1145/1999995.2000048

“Demo: Organic solar cell equipped energy harvesting active networked tag (EnHANT) prototypes” Gerald Stanje, Paul Miller, Jianxun Zhu, Alexander Smith, Olivia Winn, Robert Margolies, Maria Gorlatova, John Sarik, Marcin Szczodrak, Baradwaj Vigraham, Luca Carloni, Peter Kinget, Ioannis Kymissis, and Gil Zussman. In Proceedings of the 9th ACM Conference on Embedded Networked Sensor Systems (SenSys '11). ACM, New York, NY, USA

(Invited) “Photocurrent And Noise Analysis as Alternative Approaches to Understanding OFET Behavior,” Ioannis Kymissis. Organic Electronics Workshop 2011

“Building interactive systems using unconventional electronics” John Sarik, Ioannis Kymissis. TEI 2011. 10.1145/1935701.1935788

“A piezoelectric polymer based tone analyzer with integrated organic field effect transistors”, Yu Jen Hsu and Ioannis Kymissis. MRS Spring Meeting 2011.

“An active matrix arrayed microphone with acoustic bandwidth response”, Yu Jen Hsu and Ioannis Kymissis. Transducers 2011 Beijing.

“An active matrix arrayed microphone with acoustic bandwidth response”, Yu Jen Hsu and Ioannis Kymissis. SPIE Photonic Devices + Applications 2011.

(Invited) “Locally amplified sensors for large area systems.” MRS Spring, 2011

“Photovoltaic Device Performance Enhancement by Interfacial Decoration of Bulk Heterojunctions with Semiconducting Nanocrystals” Theodore Kramer, Ioannis Kymissis, and Irving Herman. APS March Meeting 2011.

(Invited) “Photocurrent And Noise Analysis as Alternative Approaches to Understanding OFET Behavior,” I. Kymissis, ICEL'10, Ann Arbor, MI. October 2010.

“Lab kits using the Arduino Prototyping Platform”. T3C. John Sarik and Ioannis Kymissis. ASEE/IEEE Frontiers in Education. Washington, DC October 2010

“A directly addressed monolithic LED array as a projection source,” Vincent W. Lee, Ioannis Kymissis, SPIE Optics+Photonics 2010, San Diego, CA, Aug 2010

“Strain field and magnetic field sensors with OLED indicators employing piezoelectric and magnetoresistive gated OFET,” Hsin Jung Lee, Shyuan Yang, Yu Jen Hsu, Ioannis Kymissis, SPIE Optics+Photonics 2010, San Diego, CA, Aug 2010

“Photonic crystal spectrometer,” Nadia K. Pervez, Warren Cheng, Zhang Jia, Marshall P. Cox, Hassan M. Edrees, Ioannis Kymissis, SPIE Optics+Photonics 2010, San Diego, CA, Aug 2010

“Weak 2D photonic crystals for outcoupling of multiple color bands,” Nadia K. Pervez, Warren Cheng, Chee Wei Wong, Ioannis Kymissis, SPIE Optics+Photonics 2010, San Diego, CA, Aug 2010

“Demo: Prototyping Energy Harvesting Active Networked Tags with MICA2 Motes,” Gorlatova M., Sharma T., Shrestha D., Xu E., Chen J., Skolnik A., Piao D., Kinget P., Kymissis I., Rubenstein D., Zussman G., IEEE Conference on Sensor, Mesh and Ad Hoc Communications and Networks (SECON), Boston, MA, June 2010

(invited) I. Kymissis. “Hybrid Integration using Organic Semiconductors” CMOC 2010, Storrs, CT.

Z. Jia, V.W. Lee, L. Floreano, A. Verdini, A. Cossaro, A. Morgante, I. Kymissis. “Direct observation of pentacene thiol interaction using x ray spectroscopy” II6.86, MRS Conference, Spring 2010

“Performance of graphene nanoelectromechanical resonators” Changyao Chen, Sami Rosenblatt Kirill Bolotin, William Kalb, Philip Kim, Ioannis Kymissis, Horst Stormer, Tony Heinz, James Hone. APS March Meeting, 2010

“Photonic Crystal Spectrometer” Nadia Pervez, Warren Cheng, Zhang Jia, Marshall Cox, Hassan Edrees, Ioannis Kymissis, APS March Meeting, 2010

“Direct observation of pentacene thiol interaction using x ray spectroscopy” Zhang Jia, Vincent Lee, Luca Floreano, Alberto Verdini, Albano Cossaro, Alberto Morgante, Ioannis Kymissis. APS March Meeting, 2010

“Personalizing your pixels” John Sarik, Ioannis Kymissis. 4th ACM International Conference on Tangible, Embedded, and Embodied Interaction *TEI* pp 353-356, Cambridge, MA. January 2010.

“NEMS applications of graphene” Changyao Chen; Rosenblatt, Sami; Bolotin, Kirill I.; Kim, Philip; Kymissis, Ioannis; Stormer, Horst L.; Heinz, Tony F.; Hone, James; IEEE International Electron Devices Meeting (IEDM), 2009

“A Locally Amplified Organic Transistor Strain Sensor Based on a Piezoelectric Polymer” Y.J. Hsu, Z. Jia, I. Kymissis, Aug, 2009, SID MAC Symposium on Organic and Thin Film Electronics, Cornell University.

“Novel High Frequency Surface Mounted Optical Recording System for Chronic Intracranial Optical Imaging.” Ma, H. T. and Cox, M. and Bahlke, M. and Beck, J. and Zhao, M. and Kymissis, I. and Schwartz, T. *Epilepsia*, 50 p 393, 2009.

“Semiconductor Dielectric Interfacial Study using Spectral Spatial Photocurrent Probes and 1/f Noise Probe in Organic Field Effect Transistors.” Zhang Jia, Inanc Meric, Kenneth Shepard and Ioannis Kymissis. 2009 Fall MRS, Boston, MA.

“Strain Field and Magnetic Field Sensors with OLED Indicators Employing Piezoelectric and Magnetoresistive Gated OFET.” Hsin Jung Lee, Shyuan Yang, Yu Jen Hsu and Ioannis Kymissis. 2009 Fall MRS, Boston, MA.

“Semiconductor Dielectric Interfacial Study Using Spectral Spatial Photocurrent Probes and 1/f Noise Probe in Organic Field Effect Transistors” Zhang Jia, Inanc Meric, Kenneth Shepard, and Ioannis Kymissis. 2009 ISDRS, College Park, MD.

(invited) “A locally amplified strain sensor using piezoelectric polymers and Organic Field Effect Transistors” I. Kymissis. 2009 SPIE International Symposium on Optical Science and Technology, San Diego CA.

”Challenge: Ultra Low Power Energy Harvesting Active Networked Tags (EnHANTs)” Maria Gorlatova, Peter Kinget, Ioannis Kymissis, Dan Rubenstein, Xiaodong Wang, and Gil Zussman. Mobicom 2009, Beijing, China.

”An Array of Monolithic FBAR CMOS Oscillators for Mass Sensing Applications.” M.L. Johnston, I. Kymissis, and K.L. Shepard. Transducers 2009, Denver CO.

(invited) ”Flexible Electronics Activities in the United States.” 2nd International Symposium on Flexible Organic Electronics, Halkidiki, Greece. July 2009.

(invited) “Organic semiconductor based sensors for strain and reflectivity monitoring.” 2nd International Symposium on Flexible Organic Electronics, Halkidiki, Greece. July 2009.

“Organic Photovoltaics from Extended Aromatic Molecules.” Alon A. Gorodetsky, Marshall Cox, Noah J. Tremblay, Ioannis Kymissis, Colin Nuckolls. Symposium on Organic and Thin Film Electronics, Society for Information Displays, Ithaca, NY, August 18, 2009.

“Air Stable Organic Photovoltaics from Small Molecule Acene Derivatives.” Alon A. Gorodetsky, Marshall Cox, Noah J. Tremblay, Ioannis Kymissis, Colin Nuckolls. Organic Microelectronics and Optoelectronics Workshop V, American Chemical Society and Materials Research Society, San Francisco, CA, July 6 9, 2009.

“Spin cast high k non hysteresis barium titanate nanoparticle thin film as gate dielectric in organic thin film transistors” Z. Jia, L. Huang, S. O’Brien, I. Kymissis. MRS Spring 2009, San Francisco, CA.

“Photocurrent study of traps states in pentacene thin film transistors” Z. Jia, L. Banu, I. Kymissis. MRS Spring 2009, San Francisco, CA.

“A Locally Amplified Organic Transistor Sensor Based on a Piezoelectric Polymer” Y. J. Hsu, Z. Jia, I. Kymissis. MRS Spring 2009, San Francisco, CA.

“A Locally Amplified Organic Transistor Sensor Based on a Piezoelectric Polymer” Y. J. Hsu, Z. Jia, I. Kymissis. Connecticut Microelectronic and Optoelectronic Consortium Annual Meeting, 2009.

“Photocurrent study of traps states in pentacene thin film transistors”. Z. Jia, L. Banu, I. Kymissis. Connecticut Microelectronic and Optoelectronic Consortium Annual Meeting, 2009.

(invited) ”Integrated Circuits, Optics, and Sensors using Organic Field Effect Transistors and Photodetectors” International Meeting on Information Display/Asia Display 2008. Ilseon, Korea, 2008.

(invited) "Beyond mobility: optical and electrical probes for characterizing and understanding OFETs" I. Kyymissis. 2008 International Materials Research Conference (IMRC), Chongqing, China.

(invited) "Active matrix photodetection using OFETs and printed photoconductors" I. Kyymissis. 2008 International Materials Research Conference (IMRC), Chongqing, China.

∫∞Influence of Source Drain Contact Resistance on Mobility in Organic FETs,∫∞ K. Ryu, I. Nausieda, I. Kyymissis, V. Bulovic, and C.G. Sodini, 3rd Annual Organic Microelectronics Workshop, Seattle, WA, July 2007

"An Organic Imager for Flexible Large Area Electronics" I. Nausieda, K. Ryu, I. Kyymissis, A. Akinwande, V. Bulović, C. Sodini. 2007 International Solid State Circuits Conference (ISSCC), San Francisco, CA.

(invited) "Characterization of OFETs in the linear region of operation." ACS NERM, Binghamton, NY. October 2006. I. Kyymissis, K. Ryu, A. Wang, I. Nausieda, C. Sodini, V. Bulović.

"A Locally Amplified Organic Transistor Strain Sensor Based on a Piezoelectric Polymer" Y.J. Hsu, Z. Jia, I. Kyymissis, Nov, 2008, IEEE EDS Western Region Symposium, Rochester, New York.

"Control of Parasitics in OFETs Through Self aligned Processing." Ivan A Nausieda, Ioannis Kyymissis, and Vladimir Bulović. MRS Fall 2006, San Francisco, CA.

"Molecular Organic Electronic Circuits" V. Bulović, K. Ryu, C. G. Sodini, I. Kyymissis, A. Wang, I. Nausieda, A. I. Akinwande. IEEE/ACM International Conference on Computer Aided Design, 2006. ICCAD '06. Nov. 2006 Page(s):830 831

"A Self Aligned Fully Lithographic Process for Integrated OFETs." Ioannis Kyymissis, Kevin Ryu, Akintunde I. Akinwande, Charles G. Sodini and Vladimir Bulović. MRS Spring 2005, San Francisco, CA.

"A process for integrated organic photodetection." I. Kyymissis, C.G. Sodini, A. I. Akinwande and V. Bulović, SPIE Photonics West, San Jose, CA, January 2005

"An Organic Semiconductor Based Process for Photodetecting Applications." I. Kyymissis, C.G. Sodini, A. I. Akinwande and V. Bulović. International Electron Device Meeting, 2004, San Francisco, CA, December 2004.

"Process Control of Threshold Voltage in Organic FETs." A. Wang, I. Kyymissis, V. Bulović, and A.I. Akinwande. International Electron Device Meeting, 2004, San Francisco, CA, December 2004.

(invited) "What Will be the New Oxide for Organic Semiconductors?" I. Kyymissis, A.I. Wang, A.I. Akinwande, and V. Bulović. Society for Information Display Mid Atlantic Chapter OLED Research and Technology Conference, Park Ridge, NJ, November 2004

"Physical Extraction of Mobility in OFETs" K. Ryu, I. Kyymissis, V. Bulović and C. Sodini Society for Information Display Mid Atlantic Chapter OLED Research and Technology Conference, Park Ridge, NJ, November 2004

“Pentacene Organic TFT with Al₂O₃ Gate Dielectric Deposited using Atomic Layer Deposition Method.” YongWoo Choi, JinSeong Park, Ioannis Kymissis, Annie Wang, Roy G. Gordon and Akintunde I. Akinwande. Materials Research Society Spring Meeting, San Francisco, CA, April 2004

“Fabrication of Active Devices and Logic Gates on Fibers.” YongWoo Choi, Ioannis Kymissis, Annie Wang, and Akintunde I. Akinwande, Materials Research Society Spring Meeting San Francisco, CA, April 2003

“Organic Field Emission Device Integrated with Organic Transistor.” I. Kymissis, A. I. Akinwande. International Electron Device Meeting, 2002, San Francisco, CA, December 2002.

“Field Emission from Organic Composites.” I. Kymissis, A. I. Akinwande. International Vacuum Microelectronics Conference 2002, Lyon, France, July 2002.

“Organic Conducting Composites for Field Emission Applications.” I. Kymissis, A. I. Akinwande. Materials Research Society Spring Meeting 2002, San Francisco, CA, April 2002.

“Novel CMP based process for fabricating arrays of double gated silicon field emitters.” L. Dvorson, I. Kymissis (presenting author), A. I. Akinwande. International Vacuum Microelectronics Conference 2001. Davis, CA. August 2001.

“Organic Semiconductor Thin Film Field Effect Transistors.” C. D. Dimitrakopoulos, J. Kymissis, S. Purushothaman, in Proceedings of The Int. Conf. on digital Printing Technologies, NIP16, Society of Imaging Science and Technology, Vancouver 2000, pp. 493 496.

“Organic transistors with low operating voltage and high mobility.” C. D. Dimitrakopoulos, S. Purushothaman, J. Kymissis, A. Callegari, D. A. Neumayer, P. R. Duncombe, R. B. Laibowitz, J. M. Shaw. Device Research Conference. Santa Barbara, CA 1999.

“Relatively Low Operating Voltage and High Field Effect Mobility Field Effect Transistors Based on Pentacene.” C. Dimitrakopoulos, S. Purushothaman, J. Kymissis, A. Callegari. Materials Research Society Fall Meeting, Boston, MA. December 1998.

“Parasitic power harvesting in shoes.” J. Kymissis, C. Kendall, J. Paradiso, N. Gershenfeld. IEEE Comput. Soc Digest of Papers. Second International Symposium on Wearable Computers 1998 Los Alamitos, CA.

SEMINARS AND CORPORATE PRESENTATIONS (SELECTED)

Boeing, Micron, KLA Tencor, University of Tampere (2019), ST Microelectronics, Atrate (2019), ST Microelectronics, Grenoble (2019), Rutgers (2019), SUSTECH (2018), Jordan University of Science and Technology (JUST) (2018), Kent state University (2018), McMaster University (2018), Honda research (2017), Abo Akademi (2017), Corning (2017), UCSD (2017), UDelaware (2017), IBM Research (2016), Microsoft (2016), Lehigh University (2016), University of Central Florida (2016), Checkpoint (2016), University of West Virginia (2016), KAUST (2016), Ecole Polytechnique (Paris) (2016), University of Pennsylvania (2015), Datacolor (2015), Jet Propulsion Laboratory (2015), Xerox (2014), University of Toronto (2014), UCLA (Material Science) (2014), NIST (2014), Princeton University (Mechanical Engineering) (2014), NC State (EE) (2013), Department of Physics, City College (2014), Cooper Union (2013), QDVision (2013), University of Michigan (2012), City College, Department of Chemistry, City

University of New York (2012), City College, Department of Chemical Engineering, City University of New York (2012), General Electric Global Research Center (2012), Microsoft (2012), Plextronics (2012), University of Iowa (2012), UC Irvine (2012), Ecole Polytechnique (Montreal) (2012), University of Florida (2012), Cooper Union (2011), Stanford Research Institute (2011), University of Washington (2011), Wake Forest (2010), University of Delaware (2010), Queens College (2009), University of Puerto Rico Mayagues (2009), Yale University (2009), Seoul National University (2008), Samsung Mobile Display (2008), University of Connecticut (2008), Princeton University (2008), TASC/Elettra (2008), Columbia University MRSEC colloquium (2007), Rochester Institute of Technology (2007), Cornell MSE Colloquium (2005), Binghamton EE (2005)

US PATENTS
(ISSUED)

10,859,437 Integration of optical components within a folded optical path
 10,663,361 Systems and methods for tactile sensing
 10,656,013 Nanostructure based article, optical sensor and analytical instrument and method of forming same
 10,652,963 LED display structures and fabrication of same
 10,122,345 Co integrated bulk acoustic wave resonators
 10,107,612 Systems and methods for contact localization through spatially overlapping signals
 10,041,689 Wireless automatic temperature control of radiator heating
 9,863,979 Systems, apparatus, and methods for energy monitoring
 9,666,600 Direct bandgap substrates and methods of making and using
 9,431,623 Flexible devices including semiconductor nanocrystals, arrays, and methods
 9,420,701 Flexible direct or USB plug in platform for foldable or flexible electronics
 9,390,920 Composition including material, methods of depositing material, articles including same and systems for depositing material
 9,366,571 Photonic crystal sensor apparatus and techniques
 9,293,553 Graphene electrodes for electronic devices
 9,257,606 Direct bandgap substrates and methods of making and using
 9,255,912 Monolithic FBAR CMOS structure such as for mass sensing
 9,252,013 Methods and articles including nanomaterial
 9,194,801 Systems and methods for a DNA based thermometer
 9,120,149 Methods and articles including nanomaterial
 9,099,661 OFET including PVDF TRFE CFE dielectric
 9,096,425 Methods for depositing nanomaterial, methods for fabricating a device, methods for fabricating an array of devices and compositions
 9,054,329 Light emitting devices and displays with improved performance
 8,906,804 Composition including material, methods of depositing material, articles including same and systems for depositing materials
 8,854,624 Photonic crystal spectrometer
 8,835,941 Displays including semiconductor nanocrystals and methods of making same
 8,750,517 Friend or foe detection
 8,472,758 Optical structures including nanocrystals
 8,470,617 Composition including material, methods of depositing material, articles including same and systems for depositing material
 8,441,018 Direct bandgap substrates and methods of making and using
 7,955,766 Software controlled maskless optical lithography using fluorescence feedback
 7,858,975 Organic field effect transistor systems and methods
 7,683,323 Organic field effect transistor systems and methods
 7,345,764 Apparatus and method for a slim format spectrometer
 6,870,312 Organic field emission device
 6,569,707 Method for improving performance of organic semiconductors in bottom electrode structure
 6,500,604 Method for patterning sensitive organic thin films

6,335,539 Method for improving performance of organic semiconductors in bottom electrode structure
 6,180,956 Thin film transistors with organic inorganic hybrid materials as semiconductor channels

EXPERT TESTIMONY Kumar vs. American Family Insurance, No. 3:2021 cv 00068 (S. D. of Iowa)
 Retained by Kumar, prepared expert report.

AcBel Polytech, Inc. v. Fairchild Semiconductor International, Inc., No. 1:13 cv 13046 (D. Mass.)
 Retained by AcBel Polytech. Prepared expert reports. Deposed.

Samsung Display Company, Ltd., vs. Mianyang BOE. IPR AIA review 2023 01075.
 Retained by Samsung Display. Prepared expert report, deposed. Advisory on IPR 2023 00988, IPR 2023 01075.

Samsung Display Company, Ltd., and Samsung Electronics America, Inc. vs. Mianyang BOE. ITC Investigation No. 337 TA 1378. Retained by Samsung Display.
 Prepared expert report, deposed, testified.

UNIVERSITY LEADERSHIP

Chair. Provost research advisory committee to the library research subcommittee (PACL) (2022 present)
 Chair, School at Columbia Advisory committee (2023)
 co chair, School at Columbia Advisory HOS search committee (2021 2023)
 Faculty in Residence, Hartley Hall/first year zone (2012 present)
 Columbia Maker Space, Director (2014 present)
 Member, School at Columbia Advisory committee (2020 2023)
 Provost Leadership Fellow (2017 2019)
 Member. Provost research advisory committee to the library (PACL) + research subcommittee (2018 present)
 CNI Shared Facilities, faculty Director (2016 present)
 Faculty advisor, TBP (2016 present)
 Faculty advisor, Columbia Space Initiative (2015 present)
 Nano Initiative co chair (2014 2016)
 CISE/Columbia Nano Initiative executive committee (2012 present)
 EFRC: Thrust leader and executive committee member (2008 2014)
 Institute for Data Sciences and Engineering: Space planning committee (2012 2019)
 Columbia University Cleanroom Committee (2008 present)
 NSEC: Outreach and education committee member (2008 2010)
 Columbia Environmental Health and Safety Faculty Working Group (2008 2015)

DEPARTMENT LEADERSHIP

EE Department Chair (2020 2024)
 EE Department vice chair (2019 2020)
 EE Department undergraduate program chair (2010 2019)
 EE Safety committee (2020 present)
 EE Department ombudsman (2019 2020)

UNIVERSITY ADMINISTRATIVE PROGRAMMING	Path to professorship (panelist) (2018 present) Responsible conduct of research (panelist) (2019 present) COI monitor (2017 2023) Family Weekend (EE, Makerspace programs) (various) Organizing committee, NanoDay 2009
EXTERNAL ACADEMIC SERVICE	FWO (Flanders Research Foundation) Energy, Electrical Engineering, Electronics and Mechanics External expert (2019 2023) External Evaluator, National Technical University of Athens EE program (2021)
PROGRAM COMMITTEES	IEEE IFETC Program Committee 2022 IMID: Program committee/Advisory board 2019,2018 ICDT: International Advisory Board 2022, 2021, 2020, 2019, 2018 IDW: Program committee 2019, 2018, 2017, 2016, 2015 SID: EMD program committee 2022, 2021, 2020, 2019, 2018, 2017, 2016, 2015 SID: Vice program chair, 2019 SIGGRAPH: External reviewer 2022, 2021, 2020, 2018, 2017 EMC: Program committee 2022, 2021, 2020, 2019, 2018, 2017, 2016 IEDM: Program committee 2016, 2015, 2014 MRS: Symposium organizer 2021, 2019, 2015, 2013, 2011, 2009, 2007 DRC: GenChair 2014, TPC Chair 2013, TPC VC 2012, TPC member 2011, board member (2014 present) SPIE: Symposium organizer 2023, 2022, 2021, 2020, 2019, 2018, 2017, 2016, 2015, 2014, 2013, 2012, 2011, 2010, 2009, 2003 LOPE c: VP Americas/program committee 2014, 2013, 2012, 2011 IEEE/MRS/ACS Organic Electronics Workshop: Executive committee 2009 2011 SID MAC Workshop on Organic and Thin Film Electronics, chair, 2009 CS/IEEE/MRS North East Regional Meeting, co organizer, 2006 International Vacuum Nanoelectronics Conference: Local arrangements 2004
EDITORIAL POSITIONS	Publication chair, Society for Information Display (SID) 2015 2018 Editor in Chief, Journal of the Society for Information Display (JSID). 2012 2015 Associate Editor, Journal of the Society for Information Display (JSID). 2015 present Associate Editor, KIDS Journal of Information Display (KIDS JID). 2011 2016 Associate Editor, IEEE Transactions on Electron Devices (IEEE TED). 2014 2022 Associate Editor, IEEE Open Journal of Immersive Displays (2024) Advisory Board (EDS representative) Journal of Electronic Materials (2024)
ELECTED POSITIONS	EDS Distinguished Lecturer 2019 present Armstrong Memorial Research Foundation, Board/Treasurer 2016 present President Elect, Society for Information Display. 2022 present Treasurer, Society for Information Display. 2020 2022 Secretary, Society for Information Display. 2018 2020 Director, Device Research Conference Inc. (a non profit foundation). 2014 present VP Americas East, Society for Information Display. 2017 2018 IEEE EDS Regions 1 3 & 7 SRC Vice Chair; IEEE Electron Device Society. 2012 2017 Director, Society for Information Display, Mid Atlantic Chapter. 2012 2017 Publication Chair, Society for Information Display. 2015 2018 Chairman, EDS Vice chair. IEEE New York Section Electron Device/Solid State Circuit Society Joint Chapter. 2007 present Secretary, Treasurer, Vice chair , Chair. Society for Information Display, Mid Atlantic Chapter. 2007 2011

GRADUATE THESES Completed:
SUPERVISED

Christine McGinn (PhD, NIST)
 “MicroLED and Microdevices for Next Generation Display Systems”, Keith Beherman, 2021 (PhD, Fathom Radiant)
 “Non reciprocal Acoustic Devices for RF Communications”, Columbia University EE, Jose Bhanmode 2019 (PhD, Lelantos)
 “Flexible Electronics for Large Area Sensing and Stimulation”, Columbia University EE, Caroline Yu 2019 (PhD, Apple)
 “Domain Broadening in Periodic Poling of Thinned Lithium Niobate and Spectroscopic Methods for Whole Blood Analysis” Columbia University APAM, Peter Bullen 2019 (PhD, Lumentum)
 “Optoelectronic Neural Implant Sensors for Cerebral Blood Volume Monitoring” Columbia University EE, Christopher Choi 2018 (PhD, Fenwick and West)
 “Monolithic Integration Piezoelectric Resonators on CMOS for Radio Frequency and Sensing Applications” Columbia University EE, Aida Colon Berrios 2018 (PhD, Apple)
 “Charge Injection and Transport in Pentacene Field Effect Transistors” Columbia University EE, Amrita Masurkar 2016 (PhD, BAE Systems)
 “Monolithically Integrated Acoustic Resonators on CMOS for Radio Frequency Circuit Applications” Columbia University EE, Hassan Eddrees 2016 (PhD, Apple)
 “Ionizing Radiation Effects on Graphene Based Field Effects Transistors” Columbia University EE, Kostas Alexandrou 2016 (PhD, Intel)
 “Optimization of Printed Electronics”, Columbia University EE, Shyuan Yang 2015 (PhD, Apple)
 “Excimer Laser Crystallization of Silicon Thin Films for Monolithic 3D Integration”, Columbia University EE, Fabio Carta 2015 (PhD, IBM)
 “Harvest,” School of Visual Arts, MFA Damon Ahola, 2014 (MS, Lyft)
 “Organic photovoltaic device architectures”, Columbia University EE, Jonathan Beck 2013 (PhD, Apple)
 “Systems for Pervasive Electronics and Interfaces”, Columbia University EE, John Sarik 2013 (PhD, Nanohmics)
 “Electrowetting on dielectrics”, Columbia University EE, Haig Norian (Co supervised with Ken Shepard) 2013 (PhD, ASML)
 “Processes and Materials for Organic Photovoltaics”, Columbia University EE, 2012, Marshall Cox. (PhD, Kelvin)
 “Ultrasound Data Communications for Ultra low power Wake up in Sensor Nodes”, Columbia University EE, 2012, Kshitij Yadav. Co supervised with Peter Kinget. (PhD, Qualcomm)
 “Advanced Integration of Devices Enabled by Laser Crystallized Silicon”, Columbia University EE, 2012, Vincent Lee. (PhD, NSF)
 “The Integration and Applications of Organic Thin Film Transistors and Ferroelectric Polymers” Columbia University EE, 2012, Yu Jen Hsu. (PhD, Space/X)
 “Interfacial Studies in Organic Field Effect Transistors”, Columbia University APAM, 2011, Zhang Jia. (PhD, Meta)
 Columbia University EE, Kevin Kam (PhD, Apple)
 Columbia University EE, Vikrant Kumar (PhD, Apple)

In progress:

Columbia University EE, Zicong Huang
 Columbia University EE, Peter Ballentine
 Columbia University EE, Reem Alshanbari
 Columbia University EE, Oliver Durnham

Columbia University EE, Megan Noga
Columbia University EE, Huaquan Guo
Columbia University EE, Ye Zhang

POST DOCTORAL	Completed:
ASSOCIATES	Sung Jin Kim (Chungbuk National University)
SUPERVISED	Nadia Pervez (Rice University)
	Brian Tull (Space/X)
	Htay Hliang (Applied Materials)
	En Chen Chen (KLA Tencor)
	Steve Park (KAIST)
	Marco Roberto Cavallari (State University of Campinas (Unicamp), Brazil)
	Lei (Andy) Zhang (University of Melbourne)
	Stylianios Siontas (Lelantos)
	Zachary Lamport (Exponent)
	Sayan Dey (IIT Bhubaneswar)
	Rajinder Deol (Washington University)
	Sourabh Pal (Max Planck Institute for Polymer Physics)
	Nikika Batra

In progress:

POST DOCTORAL	Completed:
ASSOCIATES	Theanne Schiros (SUNY/FIT)
CO SUPERVISED	Robert Barton (Amazon)
(50%)	Octavi Semonin (Powerhouse)