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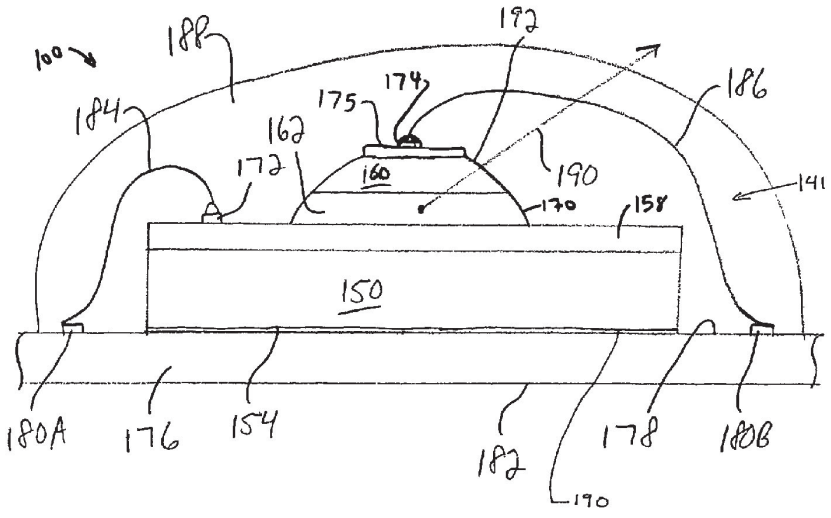
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(54) Title: LED PACKAGE HAVING IMPROVED LIGHT EXTRACTION AND METHODS THEREFOR



(57) Abstract: An optoelectronic device (100) includes a stacked structure having a first region (158) of a first conductivity type, a second region (160) of a second conductivity type and a light-emitting p-n junction (162) between those regions. The stacked structure defines a mesa with a top surface (175) and a first electrode-pad unit (174) is disposed on the top surface. The mesa has side surfaces at an upper end of the mesa. The side surfaces have at least one concave radial surface (170) formed therein for optimizing light extraction form the package. One or more radial surfaces may also be formed in the second region of the light-emitting diode and/or in the substantially transparent substrate (150). Packages having such device and methods of making the foregoing are also disclosed.

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LED PACKAGE HAVING IMPROVED LIGHT EXTRACTION AND METHODS THEREFOR

TECHNICAL FIELD

The present invention relates to making optoelectronic devices, packages for such devices, and methods for making the foregoing, and particularly relates to methods of making light-emitting diodes and light-emitting diode packages having optimized light extraction characteristics, and methods of making the foregoing.

BACKGROUND ART

Light-emitting diodes or "LEDs" include thin layers of semiconductor material of two opposite conductivity types, referred to as p-type and n-type. The layers are disposed in a stack, one above the other, with one or more layers of n-type material in one part of the stack and one or more layers of p-type material at the other end of the stack. For example, the various layers may be deposited in sequence on a substrate to form a wafer. The junction between the p-type and n-type material may include directly abutting p-type and n-type layers, or may include one or more intermediate layers which may be of any conductivity type or which may have no distinct conductivity type.

Electrodes are connected to the respective n-type and p-type layers near the top and bottom of the stack. The materials in the electrodes are selected to provide low-resistance interfaces with the semiconductor materials. The electrodes, in turn, are provided with pads suitable for connection to wires or other conductors which carry current from external sources. The pad associated with each electrode may be a part of the electrode, having the same composition and thickness of the electrode, or may be a distinct structure which differs in thickness, composition, or both from the electrode itself. The term "electrode-pad unit" is used in this disclosure to refer to the electrode and pad, regardless

of whether the pad is a separate structure or merely a region of the electrode. The wafer is cut apart to form individual dies which constitute separate LEDs.

In operation, electric current passing through the diode is carried principally by electrons in the n-type layers and by electron vacancies or "holes" in the p-type layers. The electrons and holes move in opposite directions toward the junction, and recombine with one another at the junction. Energy released by electron-hole recombination is emitted as light. As used in this disclosure, the term "light" radiation includes infrared and ultraviolet wavelength range, as well as the visible range. The wavelength of the light depends on factors including the composition of the semiconductor materials and the structure of the junction.

LEDs formed from certain semiconductor materials normally use nonconductive substrates to promote proper formation of the semiconductor layers. The nonconductive substrate typically is left in place. For example, gallium nitride-based materials such as GaN, AlGaN, InGaN and AlInGaN are used to form LEDs emitting light in various wavelength ranges including blue and ultraviolet. These materials typically are grown on insulating substrates such as sapphire or alumina.

LEDs incorporating an insulating substrate must include a bottom electrode at a location on the stack above the substrate but below the junction. Typically, the upper layer or layers of the stack are removed in a region of the stack, so as to provide an upwardly-facing lower electrode surface on a layer at or near the middle of the stack in each die. This leaves a region referred to as a "mesa" projecting upwardly from the lower electrode surface and covering the remaining area of the die. The area of the die occupied by the lower electrode surface does not emit light. It is desirable to keep the horizontal extent of this inactive area as small as possible.

The top electrode typically is formed on the top surface of the stack, i.e., the top surface of the top semiconductor layer. Typically, the layers in the stack above the junction are transparent, so that light emitted at the junction can pass out of the stack through the top surface. The top electrode is arranged so that it does not block all of the emitted light. For example, an opaque top electrode may cover only a small portion of the top surface of each die. However, "current crowding" or "current bunching", results in light emission concentrated in that area of the junction beneath the electrode, precisely where it will be most effectively blocked by the electrode. The amount of useful light reaching the outside of the die per unit of electrical current passing through the die, commonly stated as the external quantum efficiency of the die, is reduced by this phenomenon. Current crowding can also occur in the lower region, so that light emission is concentrated in the area of the junction near the lower electrode. Current crowding is a significant consideration with LEDs formed from materials having relatively high electrical resistivity, such as the gallium nitride-based materials.

To alleviate the current crowding problem, LEDs have been provided with transparent top electrodes, formed from thin layers of metals and metal compounds. A pad, which is typically opaque, is connected to the transparent electrode and occupies a small portion of the top surface. The transparent top electrode spreads the current in horizontal directions from the pad, so that current flow down through the stack is spread more evenly over the horizontal extent of the mesa.

In an example shown in FIG. 1, a light-emitting diode ("LED") comprises a semiconductor structure having layers 20 of p-type semiconductor material overlying layers 22 of n-type semiconductor material in a stack of semiconductor material.

The semiconductor material is formed on an insulating substrate 26. Typically, the stack of semiconductor material comprises a wafer for forming a plurality of LED devices. A junction, shown schematically as junction 24, is provided between the p-type layers 20 and n-type layers 22. In FIG. 1, the size of junction 24, the p-type layer 20, and n-type layer 22 are greatly exaggerated for clarity of illustration. An upper and a lower electrode-pad unit is formed for each LED of the wafer. For example, a lower electrode 28 is formed on n-type layer 22 and an upper electrode 30 is formed on p-type layer 20 as shown in FIG. 1. The wafer is then cut apart to form individual dies which constitute separate LEDs.

FIG. 2 shows a typical LED package 10 including p-type layers 20, n-type layers 22, and a substantially transparent first substrate 26. The LED package 10 is mounted atop a second substrate 32, such as a printed circuit board. The second substrate 32 comprises a dielectric element having conductive pads, leads, traces, and/or microelectronic devices, etc. The lower electrode 28 is electrically interconnected with a first conductive pad 34 of the second substrate 32 by a first wire 36. The upper electrode 30 is electrically interconnected with a second conductive pad 38 of second substrate 32 by a second wire 39. First pad 34 and second pad 38 are connected to an electrical power source. The wires 36 and 39 may be formed by wire bonding. A method known in the art, wire bonding utilizes heat, ultrasonic energy, vibration, or some combination of the foregoing, to bond small wires to the electrodes and the pads. A substantially transparent encapsulant material 40 is provided over the LED, first substrate 26, and conductive wires 36 and 39.

Each layer of the LED package 10 typically has a unique index of refraction. As used herein, the term "refraction" means the optical phenomenon whereby light passing from a

first transparent medium into a second transparent medium has its direction of travel altered. The semiconductor structure has an index of refraction designated n1, the transparent substrate 26 has an index of refraction designated n2, and encapsulant layer 40 has an index of refraction designated n3, where n1>n3.

In operation, the light is emitted from the LED. Because the index of refraction of the semiconductor structure (n1) is greater than the index of refraction of the transparent encapsulant 40 (n3), many of the light rays generated by the LED will not be emitted from the LED package 10, but will be subject to total internal reflection. This optical phenomenon, known as total internal reflection, causes light incident upon a medium having a lesser index of refraction (e.g. encapsulant layer 40) to bend away from the normal so that the exit angle is greater than the incident angle. The exit angle will then approach 90° for some critical incident angle θc that is calculated using Snell's Law. When the incident angle θi of a light ray is greater than critical angle θc, there will be total internal reflection of the light ray. Referring to FIG. 2, the incident angle θi of light ray 42 is greater than the critical angle θc at an interface 41 between p-type layer 20 and encapsulant 40. As a result, light ray 42 is not extracted from the LED, but is totally internally reflected.

In many LED packages, many of the light rays generated at the junction layer are never emitted from the package, but are totally internally reflected within the package. Thus, there is a need for LED packages having designs that optimize the amount of light that may be extracted therefrom.

DISCLOSURE OF THE INVENTION

In a first aspect of the present invention, an optoelectronic device comprises a stacked semiconductor structure including a first region of a first conductivity

type and a second region of a second conductivity type. A light-emitting p-n junction is formed between the first region and the second region. The stacked structure defines an upwardly projecting mesa having a top surface. A first electrode-pad unit is connected to the first region and a second electrode-pad unit is connected to the second region. The first electrode-pad unit is disposed on the top surface. The mesa comprises surfaces at an upper end of the structure and the surfaces of the mesa include at least one concave radial surface.

Total internal reflection can occur at an interface between the stacked structure and the surrounding medium when the index of refraction of the surrounding medium is less than the index of refraction for the stacked structure. The concave radial surface on the mesa allows more of the light rays generated at the p-n junction to strike the concave radial surface at an incident angle that is more normal to the surface, as compared to a flat surface. Accordingly, light extraction from the device is improved.

In certain preferred embodiments, the stacked structure is supported by a substantially transparent first substrate. The device preferably has at least one radial side surface on the substrate. The radial side surface on the substrate preferably comprises a concave radial side surface. Thus, light extraction is further improved by providing radial surfaces on the substrate.

In certain preferred embodiments, the first region comprises at least one n-type layer that overlies the first substrate. The second region comprises at least one p-type layer overlying the n-type layer. The p-type layers and the n-type layers form a p-n junction therebetween. The at least one p-type layer preferably comprises at least one side surface having at least one concave radial surface. The at least one n-type layer also preferably comprises side surfaces

having at least one concave radial surface. The at least one concave radial surface on the mesa may be formed using an etching process or a deposition process.

The first region of the first conductivity type preferably comprises a p-type semiconductor material and defines the top surface. The stacked structure preferably defines a lower surface and the mesa preferably projects upwardly from this lower surface. The first region is preferably disposed in the mesa and defines the top surface, whereas the second region preferably defines the lower surface. The lower surface preferably substantially surrounds the mesa. The first electrode-pad unit on the top surface preferably comprises a transparent electrode covering a substantial portion of the top surface. The transparent electrode allows light rays to pass through the electrode although the electrode covers a substantial portion of the top surface. An electrode covering a substantial portion of the top surface is preferred to address the problem of current bunching.

The mesa preferably includes a first pair of opposed side surfaces and a second pair of opposed side surfaces. Each of the side surfaces extend from the top surface of the mesa towards the lower surface. The first pair of opposed side surfaces preferably includes the at least one concave radial surface. The second pair may comprise straight vertical surfaces or concave radial surfaces.

In preferred embodiments, the mesa comprises a convex lens having a radius and a height that is selected to substantially counteract total internal reflection based upon the index of refraction for the semiconductor structure in the mesa.

In certain preferred embodiments, the at least one concave radial surface comprises a plurality of concave radial surfaces. Each concave radial surface may define a microlens.

The concave radial surfaces preferably comprise a plurality of concave radial surfaces arranged in a two-dimensional array on the top surface of the mesa. The at least one concave radial surface may also define a Fresnel lens.

In certain preferred embodiments, the stacked structure comprises material selected from the group consisting of III-V semiconductors. The first substrate may comprise sapphire, AlN, GaN, ZnO, SiC or LiGaO. The structure preferably comprises gallium nitride based semiconductors, in certain preferred embodiments.

In another aspect of the present invention, an optoelectronic device package comprises a stacked semiconductor structure including a first region of a first conductivity type and a second region of a second conductivity type and a light-emitting p-n junction between the regions. The stacked structure defines an upwardly projecting mesa having a top surface. A first electrode-pad unit is connected to the first region and a second electrode-pad unit is connected to the second region. The first electrode-pad unit is disposed on the top surface. The mesa comprises surfaces at an upper end of the structure, including at least one concave radial surface. The package further includes a second substrate having a first conductive pad a second conductive pad for supporting the optoelectronic device. Conductive features connect the first electrode-pad unit to the first conductive pad and the second electrode-pad unit to the second conductive pad. The conductive features may comprise a first wire and a second wire for interconnecting the device and the second substrate. The device may be mounted to the second substrate so that the first substrate is adjacent the second substrate. The first substrate preferably comprises a substantially transparent substrate and the package may also comprise a reflector disposed between the first substrate and the second substrate. The package also preferably comprises a

substantially transparent encapsulant surrounding at least a portion of the structure. The encapsulant preferably comprises an epoxy, elastomer or polymer. The second substrate may be adhered to the first substrate.

In another aspect of the present invention, an optoelectronic device package comprises the optoelectronic device discussed above, a second substrate having a first conductive pad and a second conductive pad supporting the optoelectronic device. Conductive features connect the first electrode-pad unit to the first conductive pad and the second electrode-pad unit to the second conductive pad. The optoelectronic device includes a substantially transparent first substrate supporting the stacked structure. The second region of the stacked structure comprises at least one n-type layer overlying the first substrate and the first region comprises at least one p-type layer overlying the n-type layer. The p-type layers and the n-type layers form a p-n junction therebetween. The at least one p-type layer comprises at least one side surface having the at least one concave radial surface.

In another aspect of the present invention, an optoelectronic device package comprises the optoelectronic device discussed above, in which the at least one concave radial surface comprises a plurality of concave radial surfaces, each defining a microlens on the mesa. The package also has a second substrate with a first conductive pad and a second conductive pad supporting the optoelectronic device. Conductive features connect the first electrode-pad unit to the first conductive pad and the second electrode-pad unit to the second conductive pad.

In another aspect of the present invention, the optoelectronic device package includes an optoelectronic device arranged with the second substrate so that the top surface faces the second substrate. Conductive features

connect the first electrode-pad unit to the first conductive pad and the second electrode-pad unit to the second conductive pad. The conductive features preferably comprise electrically conductive bonding material. The first electrode-pad unit may comprise a reflective electrode.

In another aspect of the present invention, a method of making an optoelectronic device comprises providing a first substrate and forming a semiconductor structure on the first substrate. The semiconductor structure has a first region of a first conductivity type, a second region of a second conductivity type overlying the first region and a light-emitting p-n junction therebetween. A lower surface is formed in the first region and a mesa is formed in the structure. The mesa projects upwardly from the lower surface and has a top surface. One or more radial surfaces are formed on the mesa. A first electrode-pad unit is attached to the structure at the first region and a second electrode-pad unit is attached to the structure at the second region. The second electrode-pad unit is disposed on the top surface.

The first substrate has a first surface and a second surface facing oppositely from the first surface. The step of forming the semiconductor structure may include depositing a first semiconductor material having a first conductivity type on the first surface of the substrate and depositing a second semiconductor material having a second conductivity type so that the second semiconductor material overlies the first semiconductor material. In certain preferred embodiments, a portion of the first semiconductor material is covered with a mask and semiconductor material is deposited on the portion of the first semiconductor material that is not covered by the mask to form the mesa. In other preferred embodiments, the second semiconductor material defines an upper surface of the structure and the mesa is formed by covering a portion of the upper surface with a mask and removing semiconductor material

from a portion of the semiconductor material that is not covered by the mask, forming the lower surface.

In certain preferred embodiments, the lower surface is formed in the first region so that the lower surface at least partially surrounds the mesa. A first electrode-pad unit and a second electrode-pad unit are formed by depositing metal on the top surface of the mesa and depositing metal on the lower surface of the mesa. The second electrode-pad unit preferably covers a substantial portion of the top surface. The metal deposited on the top surface may be selected to form a transparent electrode on the top surface.

In certain preferred embodiments, the mesa includes at least one wall extending from the top surface toward the lower surface, the at least one wall including the at least one radial surface. The at least one radial surface preferably comprises a concave surface. The at least one radial surface may be formed by applying a mask to the top surface of the mesa and removing semiconductor material from the mesa. The at least one radial surface is preferably formed utilizing RIE etching. The mask may be formed to have a tapered or concave shape in cross-section. The RIE etching may be designed to produce various relative etch rate for the mask and the semiconductor material such that the final etch shape of the semiconductor material can be controlled. The RIE etching is selected so that more of the semiconductor material at an outside portion of the mesa is removed than an inside portion of the mesa, thereby forming a concave radial surface. Other forms of plasma etching may also be used, such as ICP.

The at least one radial surface is preferably formed as an array of radial surfaces. In other preferred embodiments, the at one radial surface is formed on side surfaces of the first region of the structure. In certain preferred embodiments, the at one radial surface is formed on the side surfaces of the first substrate.

In another aspect of the present invention, a method of forming an optoelectronic device package comprises providing a first substrate and forming a semiconductor structure on the first substrate. The semiconductor structure has a first region of a first conductivity type and second region of a second conductivity type overlying the first region. A light-emitting p-n junction is disposed therebetween. A lower surface is formed in the first region and a mesa is formed in the structure. The mesa projects upwardly from the lower surface and has a top surface. At least one radial surface is formed on the mesa. A first electrode-pad unit is attached to the structure of the first region and a second electrode-pad unit is formed attached to the structure at the second region. The second electrode-pad unit is disposed on the top surface. The first substrate is mounted to a second substrate.

The device is preferably encapsulated with a substantially transparent encapsulant. The substantially transparent encapsulant preferably comprises an epoxy, elastomer or a polymer. In certain preferred embodiments, the first electrode-pad unit is connected to a first conductive pad of the substrate and the second electrode-pad unit is connected to a second conductive pad of the second substrate.

In certain preferred embodiments, the device is mounted to the second substrate so that the first electrode-pad unit and the second electrode-pad unit face the second substrate. An electrically conductive bonding material is preferably disposed between the first electrode-pad unit and the first pad and between the second electrode-pad unit and the second pad.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features, aspects, and advantages of the present invention will become better understood with regard to the following description, appended claims and accompanying drawings where:

FIG. 1 shows a cross-sectional view of a conventional light-emitting diode ("LED");

FIG. 2 shows a cross-sectional view of a conventional LED package including the LED of FIG. 1;

FIG. 3A shows a cross-sectional view of a substrate in a method of making an LED package in accordance with an embodiment of the present invention;

FIG. 3B shows the cross-sectional view of FIG. 3A, at a later stage in the method;

FIG. 3C shows the cross-sectional view of FIG. 3B, at a later stage in the method;

FIG. 3D is a partial view of the cross-sectional view of FIG. 3C at a later stage in the method;

FIG. 3E is a cross-sectional view of a semiconductor structure in a method of making an LED package in accordance with the embodiment of FIGS. 3A-3D;

FIG. 3F is the cross-sectional view of FIG. 3E, at a later stage in the method;

FIG. 3G is a top plan view of the structure of FIG. 3F;

FIG. 3H is a cross-sectional view of the structure in the method of making an LED package in accordance with the embodiment of FIGS. 3A-3G;

FIG. 3I is the cross-sectional view of FIG. 3H at a later stage in the method;

FIG. 3J is a partial view of the cross-sectional view of FIG. 3I;

FIG. 4 shows a cross-sectional view of an LED package, in accordance with a further embodiment of the present invention;

FIG. 5 shows a cross-sectional view of an LED package, in accordance with a still further embodiment of the present invention;

FIGS. 6A-6C show cross-sectional views of an LED package in a method of making a LED package in accordance with another embodiment of the present invention;

FIG. 7 shows a cross sectional view of an LED package in accordance with a further embodiment;

FIG. 8 shows a cross sectional view of an LED package in accordance with yet another embodiment;

FIG. 9A shows a top plan view of a wafer in a method in accordance with another embodiment;

FIG. 9B shows the cross-sectional view taken at line 9B 9B in FIG. 9A; and

FIG. 9C shows the cross-sectional view of FIG. 9B, at a later stage in the method.

MODES FOR CARRYING OUT THE INVENTION

FIGS. 3A 3J show a method of making an optoelectronic device package in accordance with one embodiment of the invention. A substrate 150, as shown in FIG. 3A, is provided on a support 149. The substrate 150 has a first, upwardly facing surface 152 and a second surface 154 facing in a direction opposite from the first surface 152. In certain preferred embodiments, the substrate 150 is a substantially transparent substrate. The substrate may comprise a sapphire substrate. The substrate may also comprise GaN, AlN, ZnO, SiC, or LiGaO. A semiconductor structure 110 comprising a stacked structure of semiconductor layers is formed on the substrate 150. A semiconductor material having a first conductivity type is deposited on the first surface 152 of the substrate 150. For example, one or more n-type layers 158 are deposited on the first surface 152 of substrate 150. A semiconductor material having a second conductivity type is deposited over the semiconductor material of the first conductivity type. One or more p-type layers 160 having a top surface 166 are deposited over the n-type layers 158. A junction is also formed between the n type layers 158 and p-type layers 160.

The stacked structure 110 of the embodiment shown in FIGs. 3A 3J comprises a structure for an LED, including a

junction 162 between the n-type layers 158 and p-type layers 160. The junction is shown schematically in FIG. 3B as a discrete layer interposed between the layers 158 and 160. In practice, the junction may comprise the border between directly abutting p-type and n-type layers, or one or more intermediate layers. The intermediate layers may have any conductivity type or no conductivity type. Alternatively, the junction may include additional structures inbetween the p-type layers 160 and n-type layers 158 or in an intermediate region. Thus, the junction may be a simple homojunction; a single heterojunction, a double heterojunction, a single quantum well, a multiple quantum well or any other type of junction structure. A person of ordinary skill in the art will appreciate that the semiconductor structure may incorporate various layers of semiconductor materials, as well as other structures used in the optoelectronic arts.

Also, each of the p-type layers 160 and n-type layers 158 can include any number of layers. Merely by way of example, the structure can incorporate a "buffer layer" at the interface with substrate 150, whereas a highly doped contact layer at the top of the stack may be included to aid in establishing ohmic contact with an upper electrode discussed below. The p-type layers 160 are typically transparent to light at the wavelength which will be emitted by the LED in service. That is, the upper region is formed entirely or principally from materials having a band gap greater than the energy of the photons which will be emitted at the junction. The structure and composition of the various layers incorporated in the stack and the sequence of layers in the stack may be selected according to known principles and techniques to provide the desired emission characteristics.

In certain preferred embodiments, the semiconductor structure 110 comprises gallium-nitride based semiconductor materials such as GaN, AlGaN, InGaN, and AlIn GaN, which are

used to form LEDs emitting light in various wavelength ranges including blue and ultraviolet. The fabrication processes used to form the stacked structure are well known. The materials are typically grown on the insulating substrate 150 by chemical vapor deposition ("CVD"), metal organic chemical vapor deposition ("MOCVD"), molecular beam epitaxy, and the like. However, those of ordinary skill in the art will appreciate that a number of other semiconductor materials for forming other types of optoelectronic devices, including LEDs, may be used. The insulating substrate can comprise any substrate that is not opaque to the emitted light, such as sapphire, alumina, silicon carbide, gallium nitride, silicon carbide or aluminum gallium nitride, for example.

The semiconductors deposited may be III-V semiconductors, i.e., materials according to the stoichiometric formula $Al_aIn_bGa_cN_xAs_yP_z$ where (a + b + c) is about 1 and (x + y + z) is also about 1. Most typically, the semiconductor materials are nitride semiconductors, i.e., III-V semiconductors in which x is 0.5 or more, most typically about 0.8 or more. Most commonly, the semiconductor materials are pure nitride semiconductors, i.e., nitride semiconductors in which x is about 1.0. The term "gallium nitride based semiconductor" as used herein refers to a nitride based semiconductor including gallium. The p-type and n-type conductivity may be imparted by conventional dopants and may also result from the inherent conductivity type of the particular semiconductor material. For example, gallium nitride based semiconductors typically are inherently n-type even when undoped. N-type nitride semiconductors may include conventional electron donor dopants such as Si, Ge, S, and O, whereas p-type nitride semiconductors may include conventional electron acceptor dopants such as Mg and Zn.

The semiconductor structure 110 has an upper end 161 and a lower end 163. In certain preferred embodiments, an

upwardly projecting mesa 164 is formed in the semiconductor structure 110. The semiconductor structure 110 shown in FIG. 3B is preferably etched to form an upwardly projecting mesa 164 and a lower surface 159. The layers of semiconductor material which form the p-type layers 160 and the junction 162 are removed by selectively etching the structure 110. In certain preferred embodiments, a portion of the n-type layers 158 is also removed. The regions in those areas which are to form the mesa 164 are protected by a mask during etching so as to form the upwardly projecting mesa 164. Such an etching process may use, for example, conventional photolithographic masking techniques. Etching to remove part of the structure 110 forms a lower surface 159. Alternatively, the lower surface 159 and mesa 164 may be formed by selective deposition. In a selective deposition or additive process, the n-type layers 158 are deposited on the substrate 150. The areas of the n-type layers 158 which are to form the lower surface 159 are covered with a masking material or otherwise protected from the deposition process. Semiconductor material for the junction 162 and p-type layers 160 are deposited on the n-type layers 158, so that the uppermost layers in the stack are not formed in these areas.

Thus, after the mesa 164 is formed, the n-type layers 158 define a lower surface 159 as shown in FIG. 3C. Surface 159 faces upwardly, away from substrate 150. The n-type layers 158 and substrate 150 have vertically extending edges 148, extending downwardly from surface 159. The mesa 164 projects upwardly from the lower surface 159. The p-type layer 160 and junction 162 preferably define the mesa 164, which has a top surface 166 and vertically extending walls 168 extending from the top surface 166 toward lower surface 159. The junction 162 and the p-type layers 160 are disposed within the upwardly projecting mesa 164. When viewed from above, the mesa 164 is typically rectangular or substantially square in shape.

It should be appreciated that the figures are not drawn to scale. In particular, the thicknesses of the various layers have been greatly exaggerated for clarity of illustration. Typically, the entire stack including mesa 164 is on the order of five microns thick. The horizontal dimensions, such as the overall width and length are on the order of a few hundred microns as, for example, about 200-300 microns. Although FIGs. 3A-3J show a structure 110 having a single mesa 164 for a single LED device, typically a structure 110 is formed as a wafer for a plurality of devices. Thus, a plurality of mesas 164 would be formed in a grid on the wafer and the following steps are performed for each device to be formed.

Referring to FIGS. 3D-3F, mesa 164 is subjected to an etching process which removes some of the semiconductor material from the p-type layers 160. One preferred etching process includes a reactive ion etching (RIE) process. In other preferred methods, other forms of plasma etching are used, such as ICP. A photoresist material 167 is deposited on the top surface 166 of mesa 164 and is exposed and developed to form a mask 165 having openings 169. During etching, the walls 168 and a portion of the top surface 166 are attacked and semiconductor material is removed from the mesa 164 until a curved surface is obtained. Preferably, a portion of the top surface remains after etching, to be used for an upper electrode pad unit, as discussed below. The mask may be given a tapered shape, as shown in FIG. 3D, utilizing controlled processing or baking of the photoresist and the relative etch rates for the photoresist and semiconductor materials may be tailored so as to form the curved surfaces on the mesa 164, at the upper end of the structure 110. The RIE etching removes the mask at an outside portion of the mesa first and then begins to remove semiconductor material from the p type layers 160, as represented by the dashed lines in FIG. 3D. These

techniques are known in the art. In other embodiments, conventional lithographic techniques may also be used. The radial surfaces on the mesa may also be formed utilizing an additive process, as discussed above. In embodiments in which the radial surfaces are formed in an additive process, transparent dielectric or polymeric material is deposited on the p-type layers 160.

The etching process forms one or more radial surfaces 170 extending between top surface 166 and n-type layers 158 as shown in FIG. 3F. As used herein, "radial" means having a radius. It should be understood that the radial surface may not be consistent across the full length of the surface 170. The radial surface of mesa 164 is curved, preferably having a concave shape, as shown in Fig. 3F. The radial surface 170 optimizes the amount of light that may be extracted from the package, as will be described in more detail below.

The concave radial surface 170 of the mesa 164 has an essentially oblong shape when viewed in plan, as shown in FIG. 3G. The concave radial surface 170 has a radius "r" and a height "h" that is preferably selected to substantially counteract total internal reflection based upon the index of refraction for the structure. In other words, the curvature of concave radial surface 170 is selected so that most of the light rays generated will strike the interface 192 at a θi; less than θc, based upon the index of refraction for the structure, n_1.

Referring to FIG. 3H, a lower electrode-pad unit 172 is formed on the lower surface 159 of n-type layer 158 and an upper electrode-pad unit 173 is formed on top surface 166 of mesa 164. The lower electrode-pad unit 172 and upper electrode-pad unit 173 comprise a conductive material such as a conductive metal. Preferred conductive metals include gold, aluminum or silver.

In certain preferred embodiments, the upper electrode-pad unit 173 comprises a transparent upper electrode 175 covering a substantial portion of the entire top surface 166 of the mesa 164. The upper electrode 175 is formed from a material which will provide a low resistance, desirably ohmic contact, with the semiconductor material of the p-type layers 160 defining the top surface 166 of the mesa. The composition and thickness of the transparent electrode 175 are selected to provide substantial transparency to light at the wavelength which will be emitted by the LED in service. Suitable materials, thicknesses and processing techniques for forming transparent electrodes to be used with particular semiconductor materials are well known. Merely by way of example, one suitable upper electrode 175 for use where the top surface 166 is defined by p-type gallium nitride can be formed by applying a layer of nickel, typically about 10 to about 500 Å thick and a layer of gold, typically about 10 to about 500 Å thick, onto the top surface 166 and annealing the contact in an oxidizing atmosphere at an elevated temperature as, for example, about 300 - 900 °C so as to oxidize the nickel. The layers of metal are applied using electron beam deposition, sputter deposition, plating, or other known methods. Preferably, the metals for upper electrode 175 are deposited so as to avoid depositing metal overlapping with the electrode to be formed on the lower electrode surface, which can short out the device.

The upper electrode-pad unit 173 also preferably includes a first pad 174 formed on the top surface of upper electrode 175 at or near the horizontal center of the top surface 166. First pad 174 is formed from appropriate materials to provide a terminal which can be connected to an external lead or contact in service as, for example, by wire bonding the lead to the pad. The materials of the pad should also be compatible with the materials in the upper electrode 175.

Merely by way of example, first pad may include a layer of titanium overlying the transparent electrode; a layer of platinum overlying the titanium layer and a layer of gold overlying the platinum layer. The exposed layer of gold provides a suitable surface for wire bonding. The first pad typically has a diameter of about 100-120 microns. Desirably, this pad is as small as possible consistent with the requirements of the bonding operation used to connect the pad to external circuitry. In other preferred embodiments, the upper electrode-pad unit 173 comprises a small pad directly on the top surface without a transparent electrode at the top surface. In other embodiments, the upper electrode 175 comprises an electrode that is essentially opaque to the light emitted by the device and the radial surface and other surfaces of the device are relied upon to transmit light.

A lower electrode-pad unit 172 is provided on the lower surface 159. This electrode-pad unit 172 preferably comprises a second pad 140 on the lower surface. Second pad 140 may be, for example, about 100 microns wide. The second pad 140 is formed from electrically conductive materials which make a good, desirably ohmic electrical contact with the lower surface 159. For example, where the lower surface 159 is formed by n type gallium nitride, the second pad 140 may be formed from layers of aluminum and titanium which are annealed at an elevated temperature. The second pad 140 also preferably includes layers adapted for bonding to external leads or other structures. For example, the second pad 140 may include a layer of platinum over the titanium and aluminum layers and a layer of gold over the platinum layer. The gold layer provides a good bonding surface. In a particularly preferred arrangement for use with gallium nitride-based semiconductors, the entire lower electrode pad unit 172 is formed from layers of aluminum, titanium, platinum and gold, deposited in that order and then annealed.

Preferably, the semiconductor materials for a plurality of devices are deposited to form a wafer. Mesas and electrode-pad units are formed for each device and then the wafer is severed into individual devices. Preferably, the wafer is cut utilizing a laser. Alternatively, mechanical scribing is used. In mechanical scribing, small scratches are made on the semiconductor materials with a diamond-tipped tool. Then, the semiconductor material is broken along the lines formed by the scratches. The wafer is severed so as to form a quadrilateral shape in plan.

The LED device is then formed into a package 100. The first pad 174 and second pad 140 are connected by conductive features 141, which may comprise wire bonds 184 and 186, to an external electrical power source. Current flows between pads 174 and 140 through the electrodes and through the stacked structure, so that light is emitted at junction 162. The light is emitted out of the structure, through the transparent first electrode 175 and other surfaces of the structure.

Referring to FIG. 3I, the LED subassembly is then mounted on a second substrate 176, such as a printed circuit board or other dielectric element having conductive pads, leads, traces, and/or microelectronic devices, etc. The second substrate 176 has a top surface 178 with a first contact 180A and a second contact 180B. The second substrate 176 has a bottom surface 182 remote from the top surface 178. In one preferred embodiment, the second surface 154 of substrate 150 is abutted against the top surface 178 of the second substrate 176. The substantially transparent substrate 150 may be adhered to second substrate 176 using an adhesive, such as a thermally conductive adhesive. In certain preferred embodiments, a reflector 190, comprising a layer of reflective material, is disposed between the substrate 150 and substrate 176. In other preferred embodiments, the reflector 190 comprises a diffraction grating disposed between the substrate

150 and second substrate 176. The diffraction grating may comprise a diffraction grating disclosed in certain embodiments of U.S. Provisional Application entitled "GaN BASED LED LIGHTING EXTRACTION EFFICIENCY USING DIGITAL DIFFRACTIVE PHASE GRATING," filed on an even date herewith, the disclosure of which is hereby incorporated by reference herein.

The LED package is then electrically interconnected with the second substrate 176. In one preferred embodiment, second pad 140 is electrically interconnected with first contact 180A using first conductive wire 184 and first pad 174 is electrically interconnected with second contact 180B by second conductive wire 186. The electrically interconnected LED package may be encapsulated with a substantially transparent encapsulant 188. Preferred encapsulants include elastomers, polymers and epoxies.

The design of the package 100 allows light generated by the LED to pass through the encapsulant layer 188. For example, a light ray 190 generated at junction layer 162 is able to pass through the interface 192 between p-type layer 160 and encapsulant layer 188. An enlarged view of light ray 190 passing through interface 192 is shown in FIG. 3J. Dashed lines in FIG. 3J show the top surface 166' and wall 168' before the radial surface 170 was formed. Without committing to any particular theory of operation, the p-type layer 160 and junction 162 have radial surface 170, which is a concave surface, so that the incident angle for the light ray 190 is substantially normal to interface 192, as compared to the incident angle for light ray 190 at surface 166'. Light ray 190 is more normal to, or perpendicular to, the interface 192 and it is believed that this feature allows ray 190 to be emitted from, rather than internally reflected in, the LED. As a result, light ray 190 passes through interface 192 and is extracted from the LED package. It is believed that many more

light rays generated by the device will be emitted, thereby providing a dramatic improvement over the prior art package shown in FIG. 2 wherein a light ray following a similar path is totally internally reflected back into the LED. Thus, providing an LED package having a mesa with one or more concave radial surfaces dramatically improves the amount of light that may be extracted from such an LED package.

FIG. 4 shows an LED package 200, in accordance with further preferred embodiments of the present invention. The package 200 has a semiconductor structure 210 with a mesa 264 that has been shaped to provide one or more concave surfaces 270 extending between a top surface 266 of mesa 264 and the lower surface 257 of n-type layers 258. The curved surface 170 may be formed as discussed above. In certain preferred embodiments, the edges 248 of n-types layer 258 and the substrate 250 also have one or more concave surfaces 272. In certain embodiments, the concave surfaces 272 extend only on the n-type layers 258 or only on the substrate 250. In other preferred embodiments, the concave surfaces 272 extend on both the n-type layer 258 and substrate 250.

After the concave surfaces are formed, the LED subassembly is preferably mounted atop a second substrate 276, such as printed circuit board, having a top surface 278 and a bottom surface 282 remote therefrom. The second substrate 276 may be a printed circuit board or other dielectric element having conductive pads, leads, conductive traces, microelectronic devices, etc. The LED package may be electrically interconnected with the second substrate 276 via a first conductive wire 284 and a second conductive wire 286. An encapsulant layer 288 is desirably deposited atop LED package for encapsulating the package.

In operation, a first light ray 290 emitted from junction layer 262 passes through concave surface 270 of mesa 264. Light ray 290 passes through interface 292 and is extracted

from LED package. This is a dramatic improvement over prior art LED packages wherein light rays following a path similar to the path of light rays 290 will is totally internally reflected back into the LED package (e.g., see FIG. 2). A second light ray 290' passes through the radial or concave surface 272 at the edge of n-type layer 258 and is also extracted from the package. Without committing to any particular theory of operation, the incident angle for the first light ray 290 and second light ray 290' is more normal to the interfaces at the curved surfaces 270 and 272 and it is believed that this enables the light rays 290 and 290' to be emitted from the device, rather than internally reflected.

FIG. 5 shows an LED package, in accordance with another preferred embodiment of the present invention. In FIG. 5, LED package 300 includes substantially transparent substrate 350 having an LED 356 mounted thereon. LED 356 includes n-type layers 358, p-type layers 360 and junction 362. P-type layers 360 are subjected to a masking and etching process that forms an array of radial surfaces 370A, 370B and 370C at the upper surface 366 of p-type layers 360. Although the present invention is not limited by any particular theory of operation, it is believed that providing a p-type layers 360 having an array of radial surfaces 370 will optimize the number of light rays that may escape from LED package 300. As shown in FIG. 5, a first light ray 390 is substantially normal to an interface 392 between p-type layer 360 and encapsulant layer 388. It is believed that, as a result, the first light ray 390 is able to pass through the interface 392 and into encapsulant layer 388. In contrast, a second light ray 390' engages a portion of p-type layer 360 that is substantially flat. As a result, the second light ray 390' is totally internally reflected back into the LED package 300. Thus, it can be seen that providing an array of radial or convex surfaces atop the p-type layer of the LED generally enhances

the amount of light that is extracted from the LED package 300.

Preferably, the electrode-pad unit 373 on the mesa comprises a transparent, current spreading electrode 375 and a pad 374. Such electrode 375 may be formed by evaporating metal or metals and allowing the evaporated metal or metals to collect on the top surface 366 of the mesa so as to cover radial surfaces 370A, 370B and 370C. The metal or metals are selected to form a transparent electrode upon annealing.

In certain preferred embodiments, an LED having a mesa with a top surface defining a plurality of concave radial surfaces defines a Fresnel lens. The Fresnel lens has a plurality of discrete surfaces each having a curvature corresponding to a portion of the surface of a lens having a continuous curved surface.

FIGS. 6A-6C show a method of making an LED package 400 having one or more radial surfaces for improving light extraction, in accordance with other preferred embodiments. In the particular embodiment shown in FIGs. 6A-6C, the one or more radial surfaces are formed using an additive process, as opposed to the removal/etching processes shown and described above. Selective re-growth of the semiconductor material is used to form the curved shape of the radial surfaces. However, in other preferred embodiments, the etching process discussed above may be used to form the package 300 shown in FIG. 5. In addition, an additive process may be used to form the packages shown in FIGS. 3I, 4, 5 or other packages having radial surfaces according to embodiments of the invention.

Referring to FIG. 6A, a semiconductor structure 410 includes a substantially transparent substrate 450 an n-type layer 458, junction layer 462 and a p-type layer 460, is provided. The p-type layer 460 and junction layer 462 are formed by depositing semiconductor materials utilizing one of the methods discussed above on a top surface 459 of the n-type

layers 458. For example, these layers may be deposited using a CVD process. Preferably, these layers are deposited while a peripheral portion 461 of the top surface 459 is covered by a mask, forming a mesa 464 having top surface 466. Mesa 464 preferably projects upwardly from a lower surface provided at the top surface 459 of n-type layer 458.

Referring to FIG. 6B, a substantially transparent material 494 is preferably deposited atop the top surface 466 of p-type layers 460. The material 494 preferably comprises a semiconductor material and will carry a pad 474. Portions of the LED package are preferably covered with a mask during this process. In preferred embodiments, the substantially transparent material 494 is a material that is substantially similar to the material comprising p-types layer 460. The substantially transparent material 494 is deposited in a manner so as to form an array of microlenses having radial surfaces 470. In other embodiments, the array of microlenses may be replaced with a single concave-shaped lens deposited on p-layers 460.

Lower contact 472 is formed on n-type layers 458 and upper contact 474 is deposited on p-type layers 460.

Referring to FIG. 6C, the LED subassembly is then mounted on a second substrate 476, having contacts 480A, 480B on a top surface 478 thereof. The upper pad 474 is then electrically interconnected with the contact 480B and lower 480A is electrically interconnected with contact 480A on the printed circuit board 476. The LED package may then be encapsulated using an encapsulant layer 488 that is preferably substantially transparent so that light generated by LED package 400 may be extracted from the package through encapsulant layer 488. A light ray 490 emitted from the junction layer 462 of the LED engages the interface 492 between the microlens designated 470H and encapsulant layer 488, as shown in FIG. 6C. Due to the concave-shaped surface

of microlens 470H, light ray 490 is substantially normal to the interface 492 between microlens 470H and encapsulant layer 488. It is believed that, as a result, light ray 490 passes through interface 492, into encapsulant layer 488, and is extracted from LED package 400.

In certain preferred embodiments, the etching of the mesa to form the radial surfaces is performed so as to remove the flat top surface. Thus, a structure shown in FIG. 7 is achieved. The mesa 164 so obtained has curved sides that meet at the top of the mesa 164, without having a flat top surface between the curved side surfaces.

Another type of package 600 utilizing a non-transparent electrode is shown in FIG. 8. The structure 610 has a substantially transparent back face 654 through which light will be directed. For example, the transparent back face may comprise a sapphire substrate 650. The structure 610 is a semiconductor structure comprising a stacked structure of p-type, n type and other semiconductor materials for generating light, as discussed above. The structure 610 has a mesa 664 protruding from the structure and a lower surface 659. In the embodiment shown in Fig. 8, the mesa 664 has side surfaces with radial surfaces 670. In other preferred embodiments, the back face 654 incorporates a plurality of microlenses as shown in Fig. 5, and/or radial surfaces extending between the side surfaces of the substrate 650 and the back face 654.

An upper electrode-pad unit 675 is mounted on the mesa 664 and has a first pad 634. A lower electrode-pad unit 672 is mounted on the lower surface 659 and has a second pad 641. The first pad 634 and second pad 641 are connected to a first contact 638 and second contact 633 on a second substrate 676. The structure 610 may be formed as discussed above, using either a subtractive or an additive process. Structure 610 is bonded to the contacts of second substrate 676 by, for example, disposing masses 686 and 684 of bonding material

between each of the pads and contacts. The contacts are also connected to an electrical power source. Thus, light generated by this device is directed out the back face 654 and a transparent electrode for upper electrode pad unit is not necessary. At least some light rays generated at the junction 662 will be directed towards the mesa 664. Mesa 664 has at least one curved surface 670 for extracting light from the LED. A reflector mounted within the package 600 may be used to direct light emitted at surface 670 towards the back surface 654, if desired.

Preferably, the first pad 634 comprises a reflective electrode. The reflective electrode may be formed as follows. After the structure 610 having the mesa 664 has been formed with the curved surface 670, the area for the first pad 634 is defined using a photolithographic mask on the top surface 666 of the mesa 664. Nickel is deposited on the top surface of the mesa 664. Gold is then deposited on the layer of nickel. The metals may be deposited utilizing electron beam deposition, sputter deposition, plating, or other known methods. The foregoing layers of metal are then oxidized so that they become transparent. A layer of reflective metal, such as gold, is then deposited on the oxidized metal. The layer of reflective metal should be thick enough to reflect the light generated by the LED through the back surface 654. For example, where gold is utilized as the reflective metal, 0.2 microns of gold would be reflective. In other embodiments, the layer of reflective metal may comprise titanium. Thus, the layer of reflective metal may be deposited on the first pad 634. In other embodiments, the first pad 634 may be comprised of one or more layers of reflective metal.

The reflective pad 634 reflects light for improved light extraction through the substrate 650. In preferred embodiments, the substrate 650 and n-type layers 658 include

radial surfaces for improved light extraction. In preferred embodiments, the layer of reflective metal deposited is thick enough so that it can be used to bond the pad 634 to the contact 638.

In other preferred embodiments, the transparent top electrode can be omitted from the devices discussed above, so that the top electrode-pad unit consists only of a pad and an electrode in the area occupied by the pad. This approach can be used, for example, where the first or upper region has relatively low resistance to current flow in the horizontal direction as, for example, where the first or upper region includes a thick layer of semiconductor material. More typically, however, at least in the case of LED's formed from nitride semiconductors such as GaN, the cost and difficulties encountered in growing such a layer to the requisite thickness with good crystal quality outweigh the cost and light transmission efficiency losses associated with the transparent top electrode.

In another preferred embodiment, a method of making an optoelectronic device utilizes a single mask for forming the mesa and for shaping the mesa. Referring to FIGS. 9A-9C, a photoresist material 767 is deposited on an upper surface 773 of the p-type layers 760 and is exposed and developed to form a mask 765 having openings 769. The mask 765 is also subjected to a controlled processing or baking to produce a tapered or concave cross-sectional shape for the mask 765. During etching, the portion of the upper surface 773 that is not covered by the mask 765 is attacked and semiconductor material is removed from the p-type layers 760 until a lower surface 759 is obtained. The etching occurs until the lower surface 759 is formed in the n-type layers 758 and a mesa 764 is formed. The same etching shapes the mesa 764 as it is formed. The tapered or concave shaped mask 765 is gradually removed in the etching process, as discussed above in

connection with Figs. 3E and 3F, so that less of the semiconductor material beneath the tapered portions of the mask 765 is removed. The etching is designed such that the final etch shape of the mesa 764 is controlled and a curved surface 770 is obtained. Preferably, a portion of the top surface remains after etching.

Although the preferred embodiments have been described above with reference to particular semiconductor materials, it should be appreciated that the invention can be applied with devices formed from semiconductor materials other than gallium nitride based semiconductors as well. Also, the conductivity types can be reversed, so that in some cases the upper region can be formed from n-type semiconductor material whereas the lower region may be formed from p type semiconductor material. In addition, the devices may comprise mesas having curved surfaces at only two of four sides of the mesa. For example, the mesa shown in FIG. 3G may comprise a rectangular mesa with two opposed side surfaces that are flat, essentially vertical surfaces and two opposed side surfaces that are concave curved surfaces. Further, the mesa shown in FIG. 3G may have a circular shape in plan.

As these and other variations and combinations of the features discussed above can be utilized without departing from the present invention, the foregoing description of the preferred embodiments should be taken by way of illustration rather than by way of limitation of the invention as defined by the claims.

WHAT IS CLAIMED IS:

1. An optoelectronic device, comprising:

(a) a stacked semiconductor structure including a first region of a first conductivity type and a second region of a second conductivity type and a light-emitting p-n junction between said regions, said stacked structure defining an upwardly projecting mesa having a top surface; and

(b) a first electrode-pad unit connected to said second region and a second electrode-pad unit connected to said first region, said first electrode-pad unit being disposed on said top surface;

(c) said mesa comprising surfaces at an upper end of said structure, said surfaces of said mesa including at least one concave radial surface.

2. The device as claimed in claim 1, further comprising a substantially transparent first substrate supporting said stacked structure.

3. The device as claimed in claim 2, wherein said device has at least one radial side surface on said substrate.

4. The device as claimed in claim 3, wherein said radial side surface on said substrate comprises a concave radial side surface.

5. The device as claimed in claim 2, wherein said first region comprises at least one n-type layer overlying said first substrate and said second region comprises at least one p-type layer overlying said n-type layer, said n-type layers and said n-type layers forming a p-n junction therebetween.

6. The device as claimed in claim 5, wherein said at least one p-type layer comprises at least one side surface having said at least one concave radial surface.

7. The device as claimed in claim 6, wherein said at least one n-type layer comprises side surfaces having at least one concave radial surface.

8. The device as claimed in claim 1, wherein said first region of a first conductivity type comprises a p-type semiconductor material and defines said top surface.

9. The device as claimed in claim 8, wherein said stacked structure defines a lower surface and said mesa projects upwardly from said lower surface, said first region being disposed in said mesa and defining said top surface, said second region defining said lower surface.

10. The device as claimed in claim 9, wherein said lower surface substantially surrounds said mesa.

11. The device as claimed in claim 9, wherein said first electrode-pad unit on said top surface comprises a transparent electrode covering a substantial portion of said top surface.

12. The device as claimed in claim 9, wherein said mesa includes a first pair of opposed side surfaces and a second pair of opposed side surfaces extending from the top surface of said mesa toward the lower surface, said first pair of opposed side surfaces including the at least one concave radial surface.

13. The device as claimed in claim 1, wherein said at least one concave radial surface comprises a plurality of concave radial surfaces, each said concave radial surface defining a microlens.

14. The device as claimed in claim 1, wherein said at least one concave radial surface defines a Fresnel lens.

15. The device as claimed in claim 1, wherein said stacked structure comprises materials selected from the group consisting of III-V semiconductors.

16. The device as claimed in claim 15, wherein said first substrate comprises a material selected from the group consisting of sapphire, AlN, GaN, ZnO, SiC and LiGaO.

17. The device as claimed in claim 1, wherein said structure comprises gallium nitride based semiconductors.

18. An optoelectronic device package, comprising:

(a) the optoelectronic device of claim 1;

(b) a second substrate having a first conductive pad and a second conductive pad for supporting said optoelectronic device; and

(c) conductive features connecting said first electrode-pad unit to said first conductive pad and said second electrode pad unit to said second conductive pad.

19. The package as claimed in claim 18, wherein said conductive features comprise a first wire and a second wire.

20. The package as claimed in claim 18, wherein said device is mounted to said second substrate so that said first substrate is adjacent said second substrate.

21. The package of claim 20, wherein said first substrate comprises a substantially transparent substrate and further comprising a reflector disposed between said first substrate and said second substrate.

22. The package as claimed in claim 18, further comprising a substantially transparent encapsulant surrounding at least a portion of said structure.

23. The package as claimed in claim 21, wherein said encapsulant is selected from the group consisting of epoxies, elastomers and polymers.

24. An optoelectronic device package, comprising:

(a) the optoelectronic device of claim 6;

(b) a second substrate having a first conductive pad and a second conductive pad supporting said optoelectronic device; and

(c) conductive features connecting said first electrode-pad unit to said first conductive pad and said second electrode-pad unit to said second conductive pad.

25. An optoelectronic device package, comprising:

(a) the optoelectronic device of claim 13;

(b) a second substrate having a first conductive pad and a second conductive pad supporting said optoelectronic device; and

(c) conductive features connecting said first electrode-pad unit to said first conductive pad and said second electrode-pad unit to said second conductive pad.

26. An optoelectronic device package, comprising:

(a) a second substrate having a first conductive pad and a second conductive pad;

(b) the optoelectronic device of claim 1, arranged with said second substrate so that said top surface faces said second substrate; and

(c) conductive features connecting said first electrode-pad unit to said first conductive pad and said second electrode-pad unit to said second conductive pad.

27. The package of claim 26, wherein said conductive features comprise electrically conductive bonding material.

28. The package of claim 26, wherein said first electrode-pad unit comprises a reflective electrode.

29. A method for making an optoelectronic device, comprising:

(a) providing a first substrate;

(b) forming a semiconductor structure on said first substrate, said semiconductor structure having a first region of a first conductivity type, a second region of a second conductivity type overlying said first region, and a light-emitting p-n junction therebetween;

(c) forming lower surface in said first region and a mesa in said structure, said mesa projecting upwardly from said lower surface and having a top surface;

(d) forming one or more radial surfaces on said mesa; and

(e) forming a first electrode-pad unit attached to said structure at said second region and a second electrode-pad unit attached to said structure at said first region, said first electrode-pad unit being disposed on said top surface.

30. The method as claimed in claim 29, wherein said lower surface is formed in said first region so that said lower surface at least partially surrounds said mesa.

31. The method as claimed in claim 30, wherein the step of forming a first electrode-pad unit and a second electrode-pad unit comprises depositing metal on said top surface of said mesa to form said first electrode-pad unit and depositing metal on said lower surface to form said second electrode-pad unit.

32. The method as claimed in claim 31, wherein said first electrode-pad unit covers a substantial portion of said top surface.

33. The method as claimed in claim 32, wherein the metal deposited on said top surface is selected to form a transparent electrode on said top surface.

34. The method as claimed in claim 29, wherein said mesa includes a least one wall extending from said top surface toward the lower surface, said at least one wall including said at least one radial surfaces.

35. The method as claimed in claim 34, wherein said at least one radial surface comprises a concave surface.

36. The method as claimed in claim 34, wherein the step of forming at least one radial surface comprises applying a mask to said top surface of said mesa and removing semiconductor material from said mesa.

37. The method as claimed in claim 36, wherein the step of forming at least one radial surface comprises RIE etching.

38. The method as claimed in claim 36, wherein said mask is formed so as to have a tapered shape in cross section and the RIE etching has a relative etch rate for said mask and said semiconductor material that is selected so that more of said semiconductor material at an outside portion of said mesa is removed than an inside portion of said mesa, thereby forming a concave radial surface.

39. The method as claimed in claim 29, wherein the forming at least one radial surfaces step includes forming an array of radial surfaces.

40. The method as claimed in claim 29, further comprising forming at least one radial surface on side surfaces of said first region of said structure.

41. The method as claimed in claim 29, further comprising forming at east one radial surface on side surfaces of said first substrate.

42. A method of forming an optoelectronic device package, comprising:

(a) providing a first substrate;

(b) forming a semiconductor structure on said first substrate, said semiconductor structure having a first region of a first conductivity type, a second region of a second conductivity type overlying said first region, and a light-emitting p-n junction therebetween;

(c) forming a lower surface in said first region and a mesa in said structure, said mesa projecting upwardly from said lower surface and having a top surface;

(d) forming at least one radial surfaces on said mesa;

(e) forming a first electrode-pad unit attached to said structure at said second region and a second electrode-pad unit attached to said structure at said first region, said first electrode-pad unit being disposed on said top surface; and

(f) mounting said first substrate to a second substrate.

43. The method as claimed in claim 42, further comprising encapsulating said device with a substantially transparent encapsulate.

44. The method as claimed in claim 43, wherein said substantially transparent encapsulant is a material selected from the group consisting of epoxies, elastomers and polymers.

45. The method as claimed in claim 42, further comprising connecting said first electrode-pad unit to a first conductive pad of said substrate and connecting said second electrode-pad unit to a second conductive pad of said second substrate.

46. The method as claimed in claim 45, wherein said device is mounted to said second substrate so that said first electrode-pad unit and said second electrode-pad unit face said second substrate.

47. The method as claimed in claim 46, wherein an electrically conductive bonding material is disposed between said first electrode-pad unit and said first pad and between said second electrode-pad unit and said second pad.

FIG. 1
(PRIOR ART)

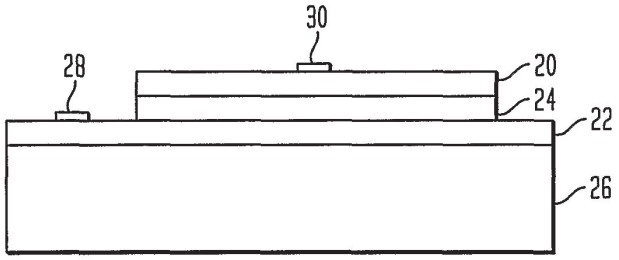


FIG. 2
(PRIOR ART)

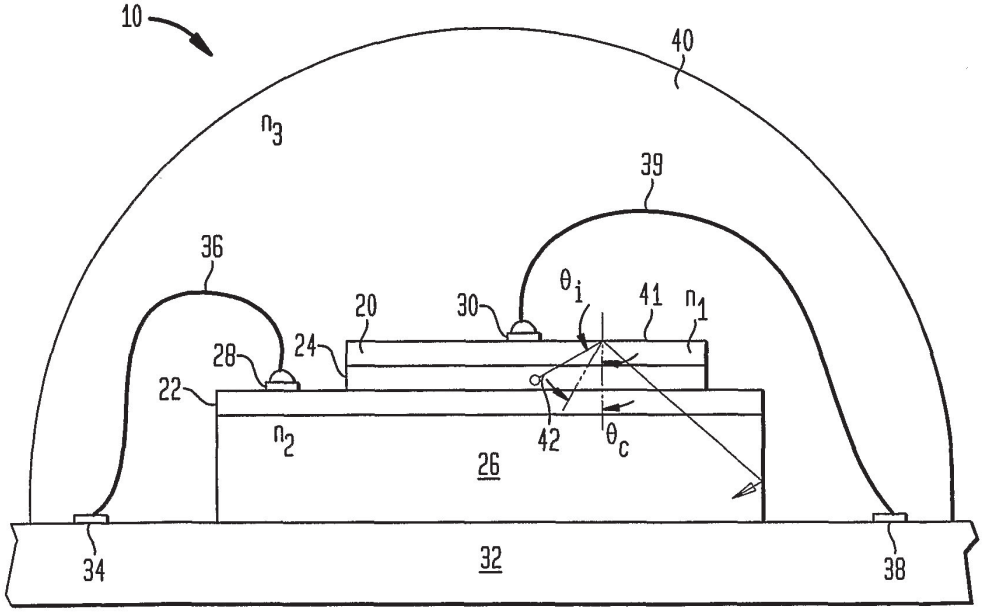


FIG. 3A

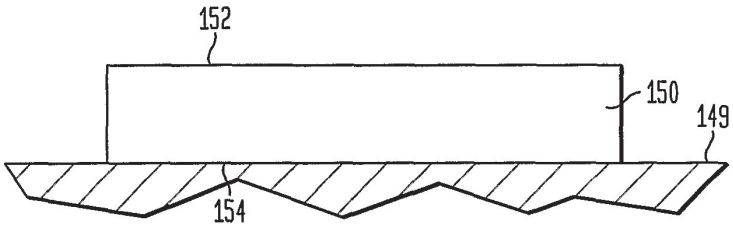


FIG. 3B

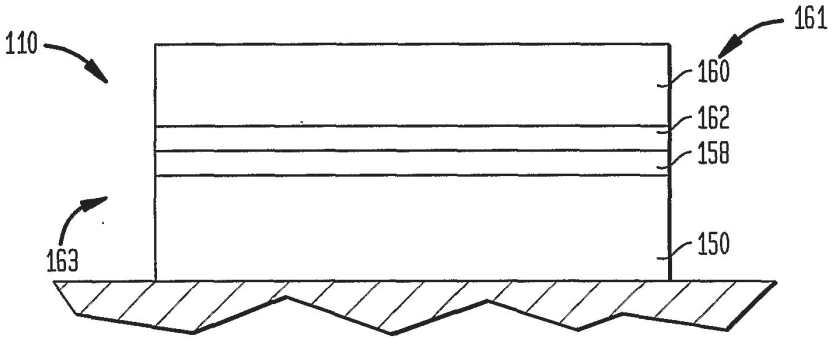


FIG. 3C

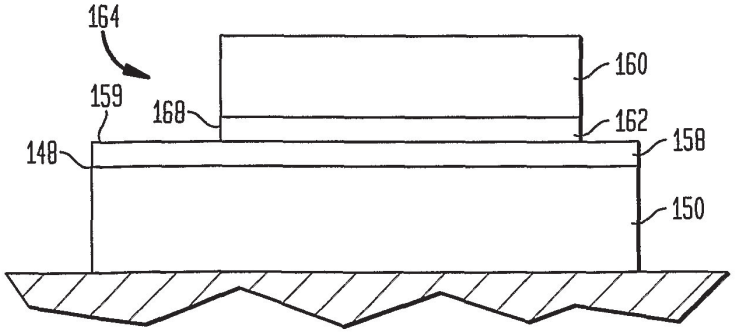


FIG. 3D

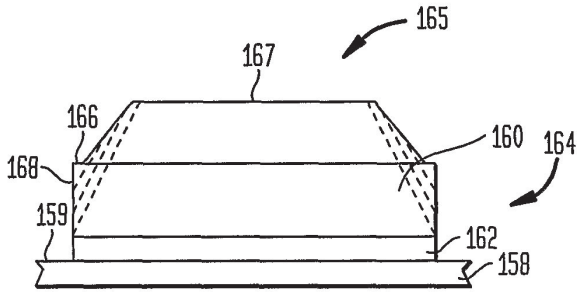

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FIG. 3E

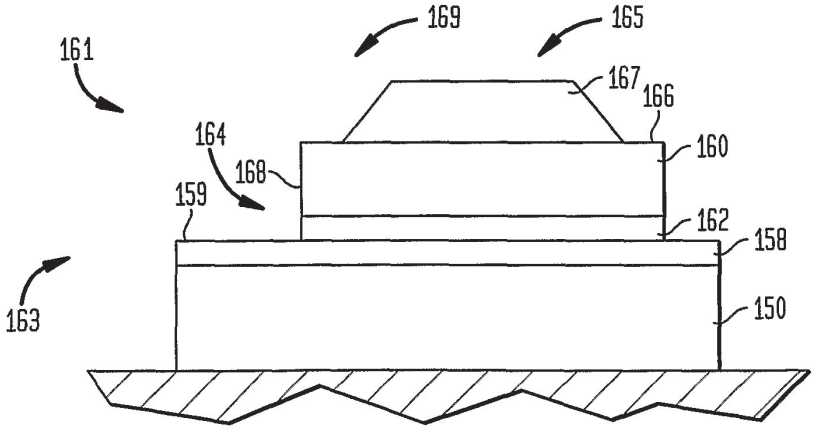

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FIG. 3F

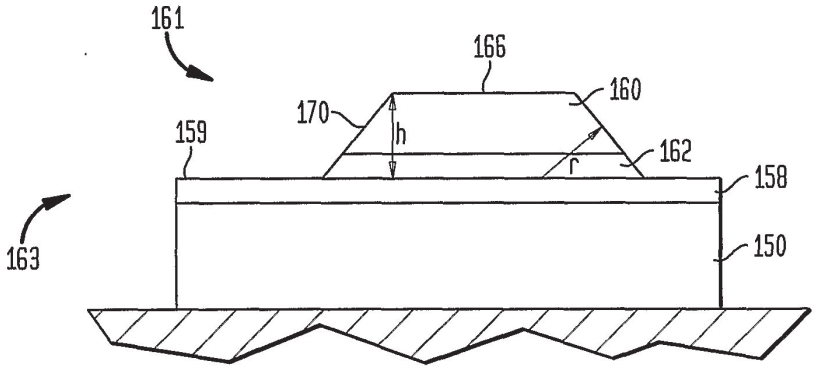


FIG. 3G

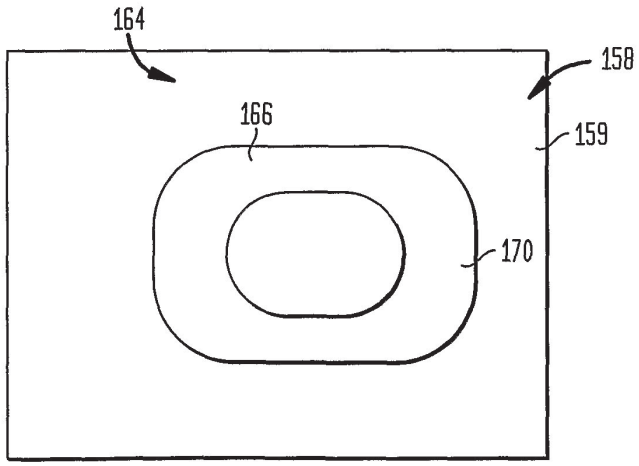


FIG. 3H

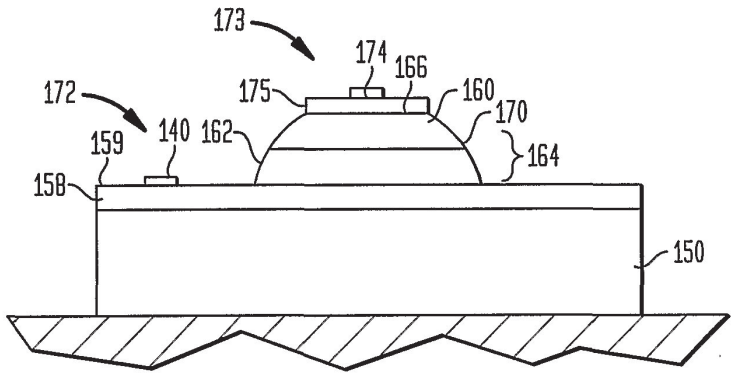

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FIG. 3I

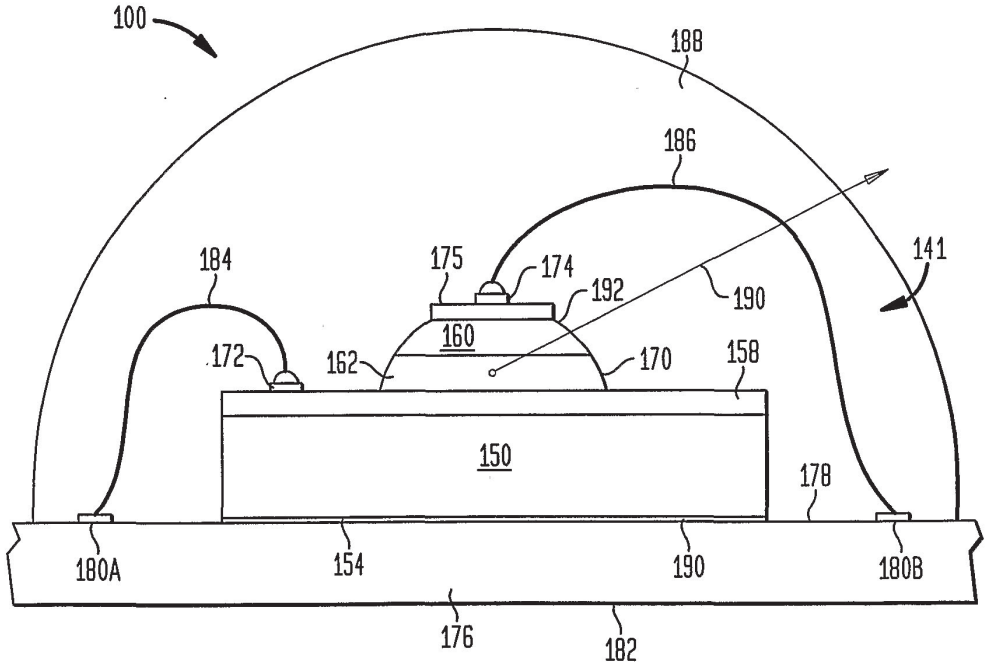

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FIG. 3J

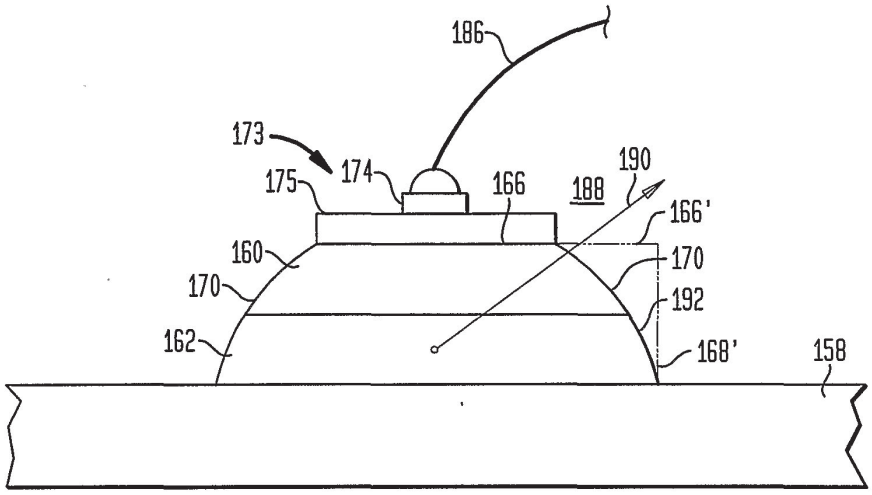


FIG. 4

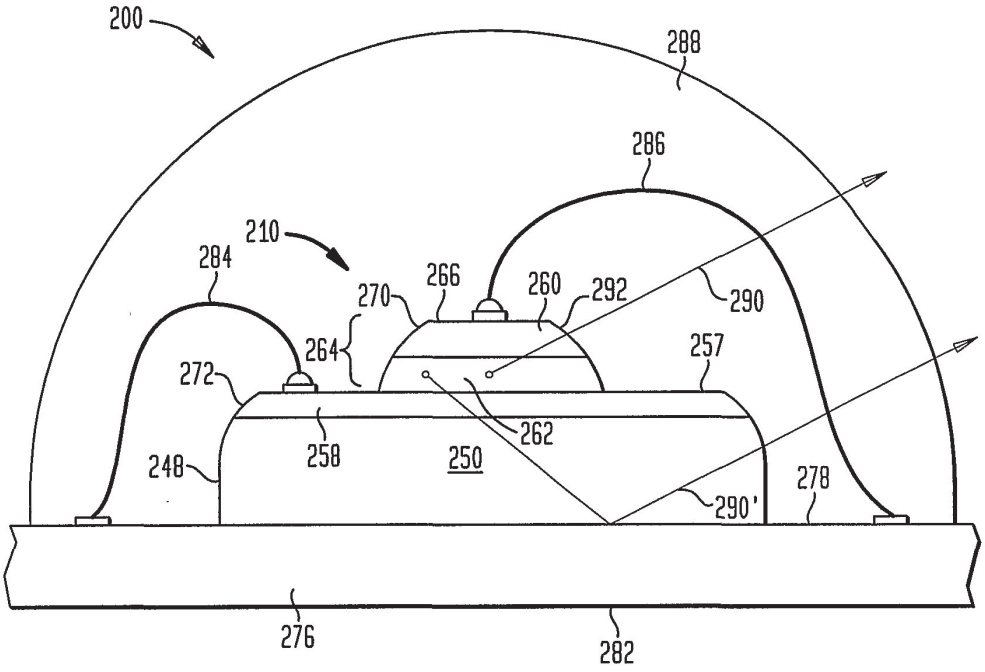

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FIG. 5

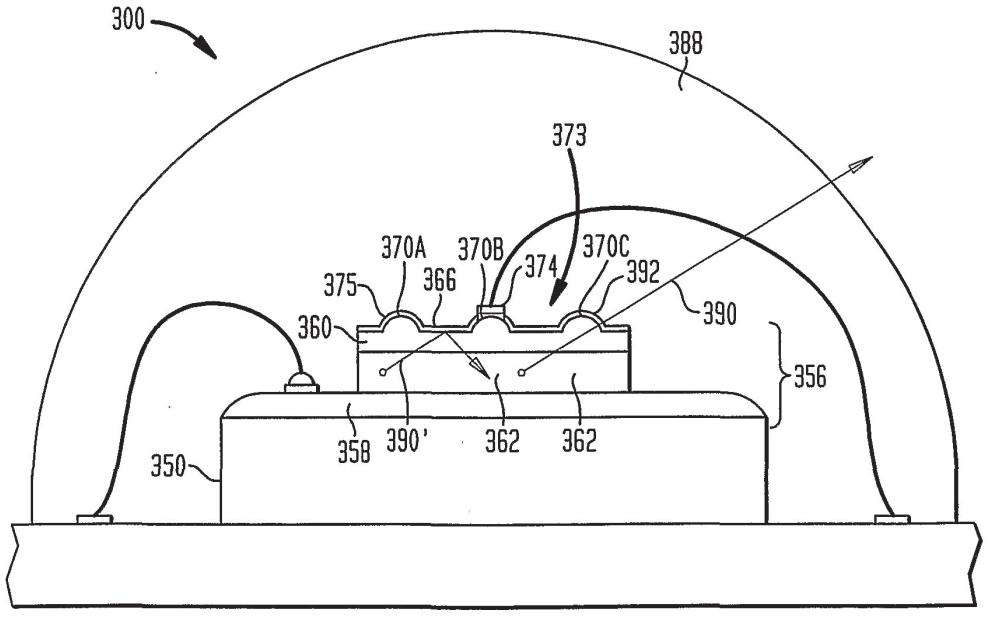

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FIG. 6A

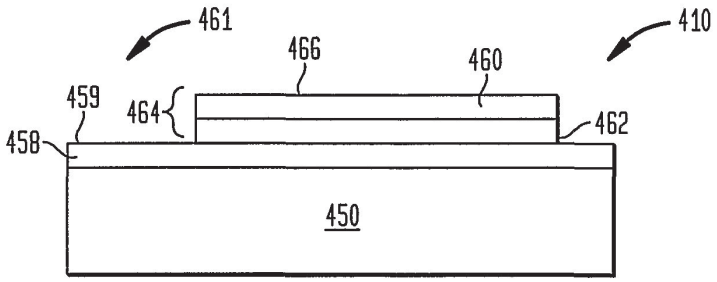


FIG. 6B

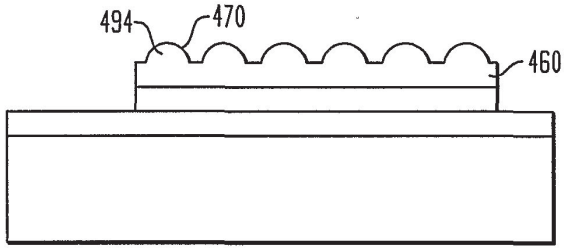


FIG. 6C

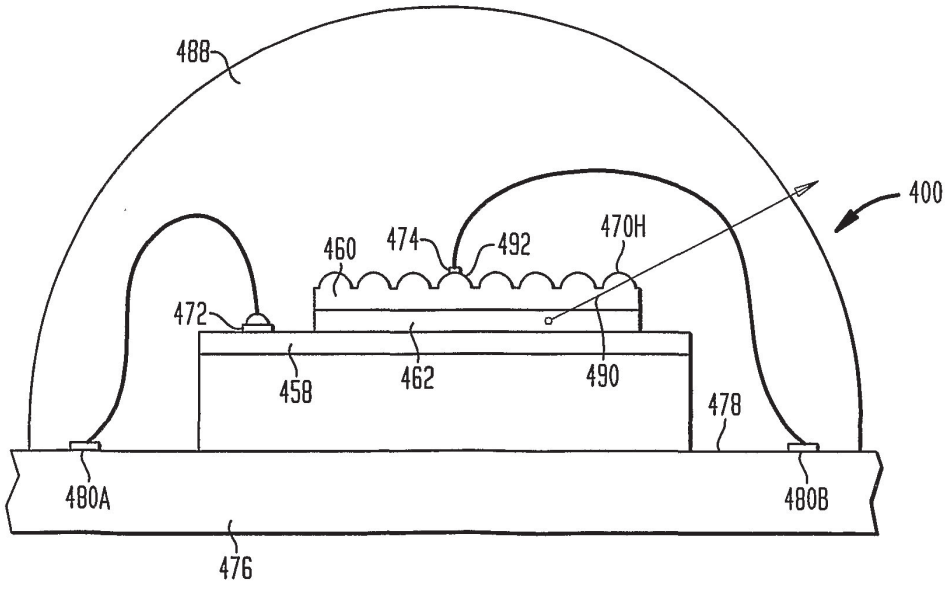


FIG. 7

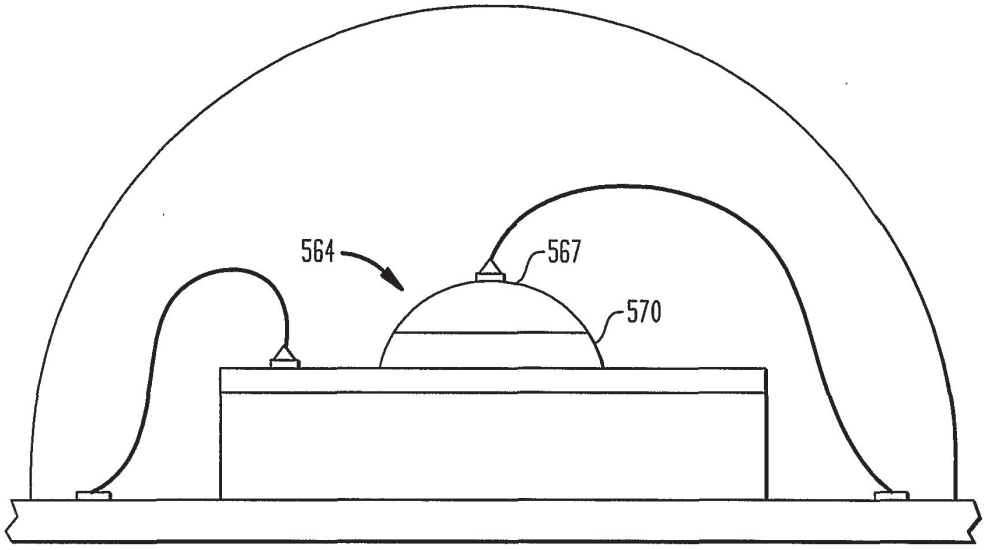

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FIG. 8

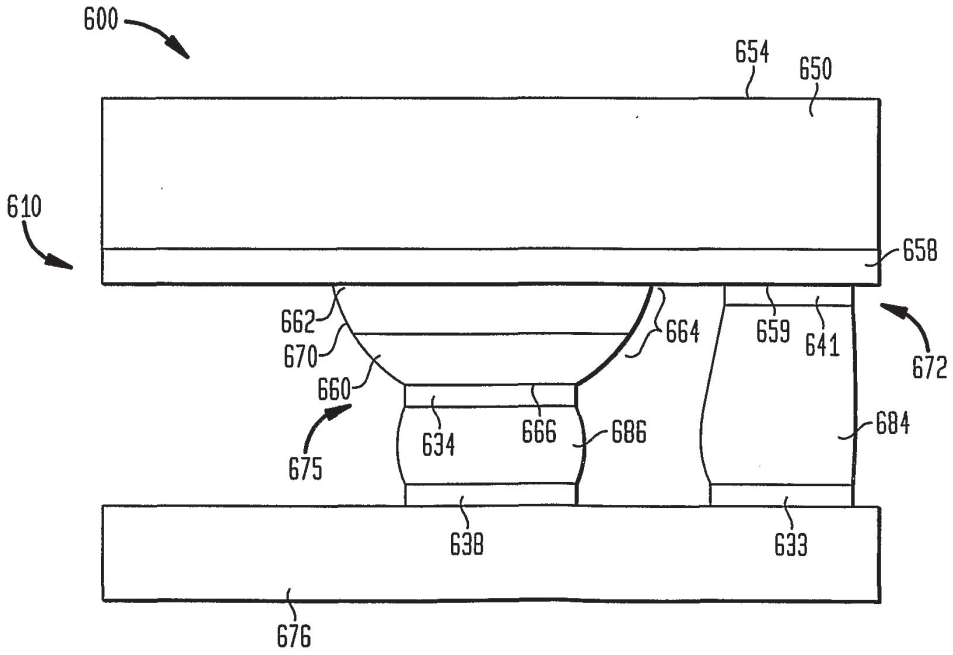

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FIG. 9A

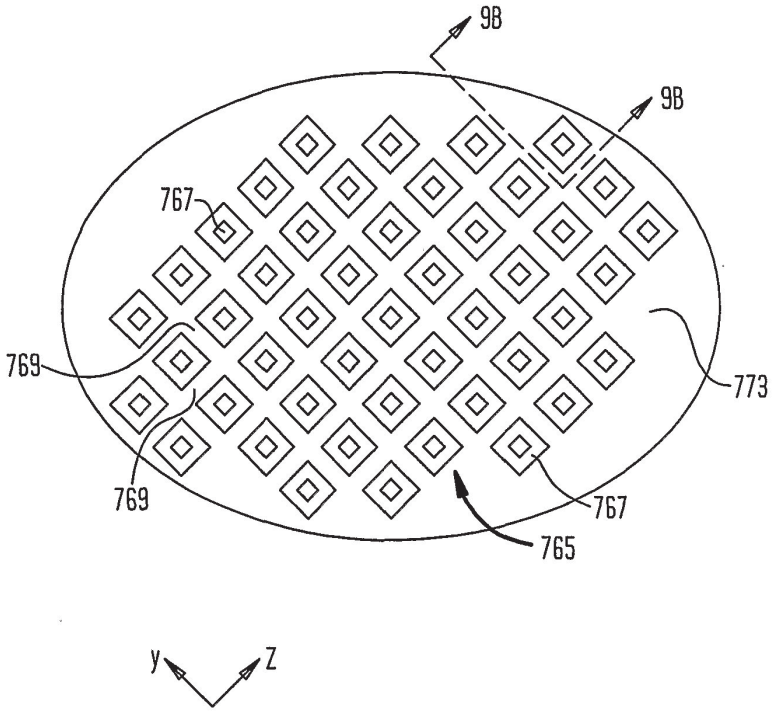


FIG. 9B

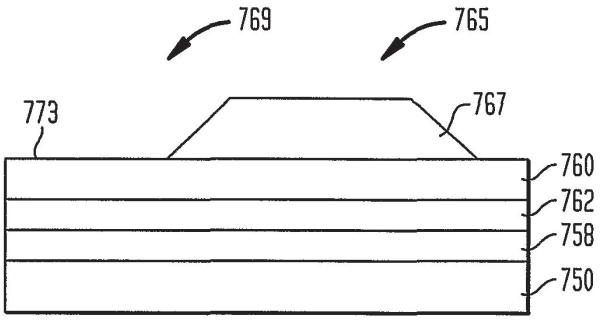
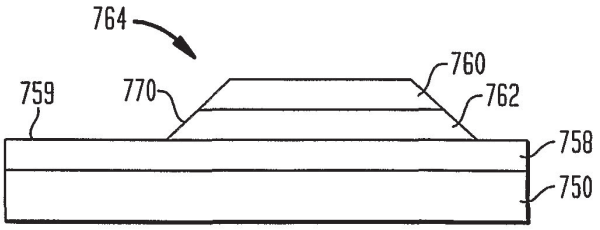


FIG. 9C



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/43515

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H01L 33/00
US CL : 257/95

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/95, 79, 94, 96, 97, 98, 99, 100

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
none

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 3,812,516 A (HAYASHI et al) 21 May 1974 (21.05.1974), figure 5.	1 --- 1-47
X --- Y	US 5,557,115 A (SHAKUDA) 17 September 1996 (17.09.1996), figure 8.	1 --- 1-47
X --- Y	US 5,248,227 A (SATOH) 27 June 1995 (27.06.1995), figure 1a.	1 --- 1-47
X --- Y	US 6,025,251 A (JAKOWETZ et al) 15 February 2000 (15.02.2000), figure 1, column 3, lines 60-63.	1 --- 1-47
X	US 4,094,752 A (VAHE) 13 June 1978 (13.06.1978), figure 2.	1

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
02 June 2002 (02.06.2002)	21 JUN 2002
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer Sara W. Crane Telephone No. (703) 308-0956

Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/43515

C. (Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,793,054 A (NIDO) 11 August 1998 (11.08.1998), column 10, lines 36-38, lines 60-62, figure 1.	2,11
Y	US 4,703,219 A (MESQUIDA) 27 October 1987 (27.10.1987), figure 2.	13
Y	US 5,633,527 A (LEAR) 27 May 1997 (27.05.1997), figure 2.	14
Y	US 5,177,593 A (ABE) 05 January 1993 (05.01.1993), figure 4b.	18-28, 42-47
Y	US 6,060,729 A (SUZUKI et al) 09 May 2000 (09.05.2000), figure 1, figure 5.	18-28, 42-47
Y	US 5,316,640 A (WAYABAYASHI et al) 31 May 1994 (31.05.1994), figure 1, figure 6.	37, 38

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US01/43515

Continuation of B. FIELDS SEARCHED Item 3:
EAST
search terms: light emitting, curvature, spherical, hemisphere, internal reflection, extraction efficiency, spherical face, shape, external quantum efficiency