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(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	2009-11-05
First Named Inventor	Jong Lam LEE
Art Unit	
Examiner Name	
Attorney Docket Number	P2317USD1

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	2	7474681		2009-01-06	Lin, et al.	
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Samsung Electronics Co., Ltd. v. Sinotechnix, LLC.
Samsung's Exhibit 1012
EX1012, Page 1

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	2	04-013916	WO		2004-02-12	Nichia Corporation		☐
	3	10-2006-0037589	KR		2006-05-03	Seoul Semiconductor Co., Ltd.		☐
	4	2002-026378	JP		2002-01-25	Kyocera Corp.		☐

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	5	10-2005-0066358	KR		2005-06-30	Samsung Electro-Mechanics Co., Ltd.		☐
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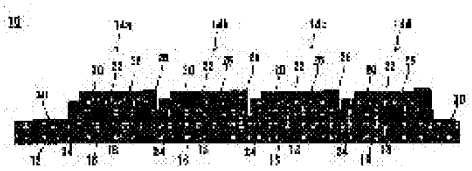
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(71)Applicant : **SANYO ELECTRIC CO LTD**
(72)Inventor : **TAKEUCHI KUNIO**

(54) **LIGHT EMITTING PARTS**



(57)Abstract:
PROBLEM TO BE SOLVED: To obtain light emitting parts which are formed as single parts and can be used suitably as a surface light source having a high luminous intensity.
SOLUTION: An n-type GaN layer 16, a light emitting layer 18, and a p-type GaN contact layer 20 are successively formed on an insulating substrate 12 in this order correspondingly to GaN light emitting diodes 14a-14d. A light transmissive electrode 22 which is a p-type side electrode is formed on the contact layer 20 in a planar form, and an n-type side electrode 24 is formed on the GaN layer 16 in such a state that the electrode 24 is extended in the widthwise direction from the vicinity of one edge of the layer 16. The members on the substrate 12 are covered with a protective film 26 and the light transmissive electrode 22 of each light emitting diode is connected in series with the p-type side electrodes 24 of its adjacent electrodes through internal wiring 28 having a width. Then pad electrodes 30 which are respectively connected to external parts are connected to the light transmissive electrode 22 of the diode at one end and the p-type side electrode 24 of the diode at the other end. Thus the light emitting parts in which the GaN light emitting diodes 14a-14d are connected in series on one insulating substrate 12 is obtained.

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CLAIMS

[Claim(s)]
[Claim 1]A light-emitting component provided with two or more 3 fellows nitride semiconductor light emitting elements which are formed on a substrate and said substrate, respectively, and are connected.
[Claim 2]The light-emitting component according to claim 1 to which said two or more 3 fellows nitride semiconductor light emitting elements are connected in series.
[Claim 3]A semiconductor layer of the 1st conductivity type with which said three fellows each nitride semiconductor light emitting element is formed on said substrate, The 1st conductivity-type lateral electrode formed [crosswise near the one end rim] on a semiconductor layer of said 1st conductivity type by extending, The 2nd conductivity-type lateral electrode formed at surface state on a semiconductor layer of the 2nd conductivity type formed on said semiconductor layer of the 1st conductivity and a semiconductor layer of said 2nd conductivity type is included, The light-emitting component according to claim 1 or 2 to which said 1st conductivity-type lateral electrode of one light emitting device of said 3 fellows nitride semiconductor light emitting element which said three fellows each nitride semiconductor light emitting element is arranged by linear shape, and adjoins mutually, and said 2nd conductivity-type lateral electrode of a light emitting device of another side are connected by internal wiring which has width.
[Claim 4]The light-emitting component according to claim 3 which will be set as R1**R2 in resistance of a semiconductor layer of said 1st conductivity type if resistance of R1 and said 2nd conductivity-type lateral electrode is set to R2.
[Claim 5]The light-emitting component according to claim 3 or 4 in which said 2nd conductivity-type lateral electrode contains a translucency electrode.
[Claim 6]The light-emitting component according to any one of claims 1 to 5 in which the number of said 3 fellows nitride semiconductor light emitting elements is determined according to driver voltage.
[Claim 7]The light-emitting component according to any one of claims 1 to 6 in which said 3 fellows nitride semiconductor light emitting element contains a GaN system light emitting device.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]Especially this invention relates to the light-emitting component for example, using 3 fellows nitride semiconductor light emitting element about a light-emitting component.
[0002]
[Description of the Prior Art]As shown in drawing 9, as the conventional GaN system light emitting device 1, That is [on the one insulating substrate 2, the pad electrode for the bonding of the couple which consists of the one translucency electrode 3, and the anode electrode 4 and the cathode terminal 5 was formed], the light emitting diode which has one light-emitting part to one chip has been used widely.
[0003]
[Problem(s) to be Solved by the Invention]since the conventional GaN system light emitting device 1 has a light-emitting part only in one place -- it -- if independent, as the surface light source, it was not suitable.
[0004]Since only one element is formed on the one insulating substrate 2 in the GaN system light emitting device 1, Since two or more GaN system light emitting devices 1 needed to be arranged on the base and it needed to connect mutually when it was going to acquire the surface light source of the large area, the interval of the GaN system light emitting device 1 which adjoins mutually had a limit, and there was a problem that the surface light source which has big luminescence intensity could not be acquired.
[0005]So, the main purpose of this invention is to provide the light-emitting component which is suitable as the surface light source which is formed as single parts and has big luminescence intensity.
[0006]
[Means for Solving the Problem]To achieve the above objects, the light-emitting component according to claim 1 is provided with two or more 3 fellows nitride semiconductor light emitting elements which are formed on a substrate and a substrate, respectively, and are connected.
[0007]As for two or more 3 fellows nitride semiconductor light emitting elements, the light-emitting component according to claim 2 is connected in series in the light-emitting component according to claim 1.
[0008]In the light-emitting component according to claim 1 or 2, the light-emitting component according to claim 3 a three fellows each nitride semiconductor light emitting

element, The 1st conductivity-type lateral electrode formed [crosswise near the one end rim] on a semiconductor layer of the 1st conductivity type formed on a substrate, and a semiconductor layer of the 1st conductivity type by extending, The 2nd conductivity-type lateral electrode formed at surface state on a semiconductor layer of the 2nd conductivity type formed on a semiconductor layer of the 1st conductivity and a semiconductor layer of the 2nd conductivity type is included, The 1st conductivity-type lateral electrode of one light emitting device of 3 fellows nitride semiconductor light emitting element which a three fellows each nitride semiconductor light emitting element is arranged by linear shape, and adjoins mutually, and the 2nd conductivity-type lateral electrode of a light emitting device of another side are connected by internal wiring which has width.

[0009]In the light-emitting component according to claim 3, resistance of a semiconductor layer of the 1st conductivity type will be set as R1**R2, if the light-emitting component according to claim 4 sets resistance of R1 and the 2nd conductivity-type lateral electrode to R2.

[0010]In the light-emitting component according to claim 3 or 4, as for the light-emitting component according to claim 5, the 2nd conductivity-type lateral electrode contains a translucency electrode.

[0011]As for the light-emitting component according to claim 6, in the light-emitting component according to any one of claims 1 to 5, the number of 3 fellows nitride semiconductor light emitting elements is determined according to driver voltage.

[0012]In the light-emitting component according to any one of claims 1 to 6, as for the light-emitting component according to claim 7, 3 fellows nitride semiconductor light emitting element contains a GaN system light emitting device.

[0013]In the light-emitting component according to claim 1, since two or more 3 fellows nitride semiconductor light emitting elements are formed and connected on one substrate using general IC manufacturing process, an interval of 3 fellows nitride semiconductor light emitting element which adjoins mutually can be made narrower than before. Therefore, it is formed as single parts and the surface light source with large luminescence intensity is acquired.

[0014]If two or more 3 fellows nitride semiconductor light emitting elements are connected in series so that it may indicate to claim 2, light quantity from a three fellows each nitride semiconductor light emitting element will be made equal.

[0015]A three fellows each nitride semiconductor light emitting element is arranged by linear shape so that it may indicate to claim 3, And connection of the 1st conductivity-type lateral electrode of one light emitting device of 3 fellows nitride semiconductor light emitting element which adjoins mutually, and the 2nd conductivity-type lateral electrode of a light emitting device of another side of internal wiring which has width will equalize more luminous intensity distributions in each 3 fellows nitride semiconductor light emitting element. If set as ** (resistance R1 of a semiconductor layer of the 1st conductivity type) (resistance R2 of the 2nd conductivity-type lateral electrode) indicate to claim 4, luminous intensity distributions in each 3 fellows nitride semiconductor light emitting element will be abbreviated-equalized.

[0016]If the number of 3 fellows nitride semiconductor light emitting elements is set up suit driver voltage of a device with which a light-emitting component is used so that it may indicate to claim 6, a light-emitting component applicable to various driver voltages will be obtained. The 2nd conductivity-type lateral electrode is formed of a translucency

electrode, and as a 3 fellows nitride semiconductor light emitting element, for example, a GaN system light emitting device is used so that it may indicate to claim 7, so that it may indicate to claim 5.

[0017]

[Embodiment of the Invention]Hereafter, this embodiment of the invention is described with reference to drawings.

[0018]With reference to drawing 1 and drawing 2, as for the light-emitting component 10 of this embodiment of the invention, the four GaN (semiconductor which contains Ga and N at least) system light emitting diodes 14a-14d are formed on the insulating substrate 12, for example including the insulating substrates 12, such as silicon-on-sapphire Hitoshi.

[0019]Namely, on the insulating substrate 12, it corresponds to each GaN system light emitting diodes 14a-14d, The n type GaN layer (Si dope) 16 used as the electrode installation layer of 3.0 micrometers of thickness, the luminous layer 18 of 0.1 micrometer of thickness, and the p type GaN contact layer (Mg dope) 20 of 0.5 micrometer of thickness are formed in this order.

[0020]On each p type GaN contact layer 20, the translucency electrode 22 which is a p type lateral electrode is formed at surface state, and, [crosswise near the one end rim] on each n type GaN layer 16, the n type lateral electrode 24 is formed. The translucency electrode 22 and the n type lateral electrode 24 are formed in parallel so that drawing 1 may show well.

[0021]And each member on the insulating substrate 12 is covered with the protective film 26, and the series connection of the translucency electrode 22 and the n type lateral electrode 24 between adjoining GaN system light emitting diodes is carried out with the internal wiring 28 which has the predetermined width W1. At this time, the end of the internal wiring 28 is extended and formed [crosswise near the one end rim] on the translucency electrode 22. Therefore, concerning one GaN system light emitting diode, in the connected part of the internal wiring 28 and the translucency electrode 22, the formation point of the n type lateral electrode 24 becomes near the edge of an opposite hand. The size of the width W1 of the internal wiring 28 is set up become for it to be a little smaller than the width W2 of the translucency electrode 22, and a little larger than length L of the n type lateral electrode 24 for example, so that drawing 1 may show.

[0022]The pad electrode 30 for connecting with external parts, respectively is connected to the translucency electrode 22 and the n type lateral electrode 24 of both ends. The pad electrode 30 as well as the internal electrode 28 is formed.

[0023]Thus, the light-emitting component 10 which carried out the series connection of the four GaN system light emitting diodes 14a-14d is obtained by connecting the translucency electrode 22 and the n type lateral electrode 24 via the internal wiring 28. The equivalent circuit of the light-emitting component 10 is shown in drawing 3.

[0024]An example of such a manufacturing method of the light-emitting component 10 is explained with reference to drawing 4.

[0025]First, as shown in drawing 4 (a), the n type GaN layer 16, the luminous layer 18, and the p type GaN contact layer 20 are grown epitaxially in this order by MOCVD (organometal chemistry vapor phase growth) on the insulating substrate 12, The p type GaN contact layer 20 of 3.0 micrometers of thickness, the n type GaN layer 16 of $N_D=10^{18}cm^{-3}$, the luminous layer 18 of 0.1 micrometer of thickness and 0.5 micrometer of thickness, and $N_A=10^{17}cm^{-3}$ is formed.

[0026]As shown in drawing 4 (b), by subsequently, the dry etching method which supplies photo lithography and gaseous chlorine with nickel mask by the pressure of 0.5 Pa. Etching removal of the p type GaN contact layer 20, the luminous layer 18, and the n type GaN layer 16 on the insulating substrate 12 is carried out, and the mesa 21 is formed. The depth of etching at this time is 0.8 micrometer.
[0027]As shown in drawing 4 (c), by the dry etching method which supplies photo lithography and gaseous chlorine with nickel mask by the pressure of 0.5 Pa, etching removal of the n type GaN layer 16 on the insulating substrate 12 is carried out, and the crevice 32 is formed so that the insulating substrate 12 may be exposed. The depth of etching is set to 3.6 micrometers and the layer which constitutes the GaN system light emitting diodes 14a-14d is separated by this, respectively.
[0028]As it continues and is shown in drawing 4 (d), by the electron beam evaporation by the pressure of $2x10^{-6}$torr. The Ni film of 2 nm of thickness and the Au membrane of 4 nm of thickness are formed in this order at the whole p type GaN contact layer 20 upper surface, and the translucency electrode 22 of surface state is formed of photo lithography. By the electron beam evaporation by the pressure of $2x10^{-6}$torr. On the n type GaN layer 16, the Ti film of 30 nm of thickness and the Al film of 500 nm of thickness are formed in this order, and the n type lateral electrode 24 prolonged by photo lithography [crosswise near the one end rim] on the n type GaN layer 16 is formed. The n type lateral electrode 24 is equivalent to the cathode terminal of a GaN system light emitting diode.
[0029]Then, as shown in drawing 4 (e), the protective film 26 which becomes the whole upper surface of the chip formed by drawing 4 (d) from SiO_2 of 300 nm of thickness is formed of electron beam evaporation.
[0030]Then, etching removal of the protective film 26 is carried out by photo lithography, and an opening is carried out so that a part of each upper surface of the translucency electrode 22 and the n type lateral electrode 24 may be exposed. Concerning one GaN system light emitting diode at this time, the opening on the translucency electrode 22 is extended and formed [of an opposite hand / crosswise near the edge] with the formation point of the n type lateral electrode 24. The opening of the n type lateral electrode 24 is also prolonged crosswise, and is formed.
[0031]And as shown in drawing 4 (f), the Ni film of 100 nm of thickness and the Au membrane of 700 nm of thickness are formed in this order by the electron beam evaporation by the pressure of $2x10^{-6}$torr at the whole upper surface of the protective film 26, and the internal wiring 28 is formed of photo lithography. Therefore, concerning one GaN system light emitting diode, the internal wiring 28 connected to the internal wiring 28 and the n type lateral electrode 24 which are connected to the translucency electrode 22 will be pulled out by the counter direction from the both ends of a GaN system light emitting diode, respectively. Although not illustrated to drawing 4 (f), the pad electrode 30 is formed simultaneously similarly. The end part connected with the translucency electrode 22 among the internal wiring 28 and the pad electrode 30 is equivalent to the anode electrode of a GaN system light emitting diode.
[0032]Thus, the light-emitting component 10 in which the series connection of the four GaN system light emitting diodes 14a-14d was carried out is formed.
[0033]Since two or more GaN system light emitting diodes 14a-14d are formed and connected on the insulating substrate 12 of one sheet using general IC manufacturing

process according to the luminescence intensity 10, the interval of the GaN system light emitting diode which adjoins mutually can be made narrower than before. Therefore, the light-emitting component 10 which is formed as single parts and is suitable as the surface light source with large luminescence intensity is obtained.

[0034]Since according to the light-emitting component 10 the GaN system light emitting diodes 14a-14d can be formed on the insulating substrate 12 at linear shape as shown in drawing 5 (a), luminescence of a large area is obtained so that drawing 5 (b) may show.

[0035]Since the GaN system light emitting diodes 14a-14d can be formed on the same insulating substrate 12, the insulated separation for GaN system light emitting diode 14a-14d and integration become easy.

[0036]Each GaN system light emitting diodes [14a-14d] luminous intensity distributions come to be shown in drawing 6. Setting resistance of Rt and the n type GaN layer 16 to Rn for resistance of the translucency electrode 22, Rp shows a part for resistance of the p type GaN contact layer 20, the contact resistance of the translucency electrode 22 and the p type GaN contact layer 20, and p-n junction phase-voltages this resistance, and each resistance presupposes it that it is thought in a field that it is fixed.

[0037]Since the n type lateral electrode 24 of one light emitting diode of the GaN system light emitting diode which each GaN system light emitting diodes 14a-14d are arranged by linear shape, and adjoins mutually, and the translucency electrode 22 of the light emitting diode of another side are connected by the internal wiring 28 which has the width W1, When resistance per unit area of the translucency electrode 22 is small (Rt**Rn), as shown in drawing 6 (a), current flows into the n type GaN layer 16 from the translucency electrode 22 whole surface, and the current which passes the luminous layer 18 becomes uniform irrespective of the position in the luminous layer 18. Therefore, as shown in drawing 6 (b) and (c), luminescence from the translucency electrode 22 becomes abbreviated homogeneity irrespective of a luminescence part, and bigger luminescence intensity is obtained.

[0038]Incidentally, when resistance per unit area of the translucency electrode 22 is strong (Rt>Rn), as shown in drawing 6 (d), the current which passes the luminous layer 18 is concentrated on the internal wiring 28, i.e., anode electrode vicinity. In this case, although the luminescence intensity in the X-X section shown in drawing 6 (e) becomes uneven, Since the n type lateral electrode 24 of one light emitting diode of the GaN system light emitting diode which each GaN system light emitting diodes 14a-14d are arranged by linear shape, and adjoins mutually, and the translucency electrode 22 of the light emitting diode of another side are connected by the internal wiring 28 which has the width W1, The luminescence intensity in the Y-Y section shown in drawing 6 (f) becomes abbreviated homogeneity. Therefore, from the case where resistance per unit area of the translucency electrode 22 mentioned above is small, luminescence intensity is equalized from unevenness and the conventional technology shown in drawing 9 at least, and luminescence intensity becomes large, although it becomes small.

[0039]As shown in drawing 7 (a) - (c), the GaN system light emitting diodes 14a-14d may be formed on the insulating substrate 12a, a series connection may be carried out to a U shape, and the light-emitting component which it is formed as single parts also in this case, and big luminescence intensity is obtained, and is suitable as the surface light source is obtained.

[0040]That is, the light-emitting component which it is formed as single parts, and big

luminescence intensity is obtained, and can be applied to the surface light source is obtained by forming and carrying out the series connection of two or more GaN system light emitting diodes on an insulating substrate so that drawing 5 and drawing 7 may show.

[0041]In order to drive a GaN system light emitting diode, it is [more than 3V] required, and circuit operation is performed using 5V power supply in many cases. When 4V grade needs per GaN system light emitting diode (for example, when sending 20-mA current), and driver voltage is 24V, six GaN system light emitting diodes should just use the light-emitting component by which the series connection was carried out. Thus, by using the GaN system light emitting diode of the number of series elements according to driver voltage, luminescence of a large area is attained, and restriction of driver voltage also decreases, and the application covered in many fields can be expected.

[0042]As shown in drawing 8, current control elements, such as resistance (drawing 8 (a)) and FET (drawing 8 (b)), may be formed on the same insulating substrate with the GaN system light emitting diodes 14a-14n, In this case, the GaN system light emitting diodes 14a-14n and a current control element can be formed on the same insulating substrate at a monolithic.

[0043]Thus, since an external element becomes unnecessary, the small and lightweight light-emitting component 10 is obtained and not only the GaN system light emitting diodes 14a-14d but a current control element can be formed with a wide gap band material, The strong light-emitting component 10 is obtained to generation of heat, and integration becomes easy. Since an element is constituted only in the one side principal surface of an insulating substrate, general IC manufacturing process also in this case is applicable. Restriction of driver voltage decreases further by it not only adjusting the number of GaN system light emitting diodes, but adding a current control element. The surge current at the time of an assembly and use can be controlled by adding resistance to the GaN system light emitting diodes 14a-14n.

[0044]Although the embodiment of drawing 1 described the case where the series connection of the four GaN system light emitting diodes 14a-14d was carried out, it cannot be overemphasized that the number of GaN system light emitting diodes is not limited to this.

[0045]In an above-mentioned embodiment, although the light emitting diode was explained to the example as a light emitting device, it may not be limited to this but may be laser.

[0046]As a 3 fellows nitride semiconductor light emitting element of the light-emitting component 10, if it is a light emitting device which consists of a 3 fellows nitride semiconductor which contains AlN, InN, BN, or InGaN, for example, arbitrary 3 fellows nitride semiconductor light emitting elements can be used.

[0047]

[Effect of the Invention]According to this invention, two or more light-emitting parts can be formed on one substrate, and the light-emitting component which it is formed as single parts, and big luminescence intensity is obtained, and is suitable as the surface light source is obtained.

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TECHNICAL FIELD

[Field of the Invention]Especially this invention relates to the light-emitting component for example, using 3 fellows nitride semiconductor light emitting element about a light-emitting component.

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PRIOR ART

[Description of the Prior Art]As shown in drawing 9, as the conventional GaN system light emitting device 1, That is [on the one insulating substrate 2, the pad electrode for the bonding of the couple which consists of the one translucency electrode 3, and the anode electrode 4 and the cathode terminal 5 was formed], the light emitting diode which has one light-emitting part to one chip has been used widely.

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EFFECT OF THE INVENTION

[Effect of the Invention]According to this invention, two or more light-emitting parts can be formed on one substrate, and the light-emitting component which it is formed as single parts, and big luminescence intensity is obtained, and is suitable as the surface light source is obtained.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]since the conventional GaN system light emitting device 1 has a light-emitting part only in one place -- it -- if independent, as the surface light source, it was not suitable.
[0004]Since only one element is formed on the one insulating substrate 2 in the GaN system light emitting device 1, Since two or more GaN system light emitting devices 1 needed to be arranged on the base and it needed to connect mutually when it was going to acquire the surface light source of the large area, the interval of the GaN system light emitting device 1 which adjoins mutually had a limit, and there was a problem that the surface light source which has big luminescence intensity could not be acquired.
[0005]So, the main purpose of this invention is to provide the light-emitting component which is suitable as the surface light source which is formed as single parts and has big luminescence intensity.

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MEANS

[Means for Solving the Problem]To achieve the above objects, the light-emitting component according to claim 1 is provided with two or more 3 fellows nitride semiconductor light emitting elements which are formed on a substrate and a substrate, respectively, and are connected.
[0007]As for two or more 3 fellows nitride semiconductor light emitting elements, the light-emitting component according to claim 2 is connected in series in the light-emitting component according to claim 1.
[0008]In the light-emitting component according to claim 1 or 2, the light-emitting component according to claim 3 a three fellows each nitride semiconductor light emitting element, The 1st conductivity-type lateral electrode formed [crosswise near the one end rim] on a semiconductor layer of the 1st conductivity type formed on a substrate, and a semiconductor layer of the 1st conductivity type by extending, The 2nd conductivity-type lateral electrode formed at surface state on a semiconductor layer of the 2nd conductivity type formed on a semiconductor layer of the 1st conductivity and a semiconductor layer of the 2nd conductivity type is included, The 1st conductivity-type lateral electrode of one light emitting device of 3 fellows nitride semiconductor light emitting element which a three fellows each nitride semiconductor light emitting element is arranged by linear shape, and adjoins mutually, and the 2nd conductivity-type lateral electrode of a light emitting device of another side are connected by internal wiring which has width.
[0009]In the light-emitting component according to claim 3, resistance of a semiconductor layer of the 1st conductivity type will be set as R1**R2, if the light-emitting component according to claim 4 sets resistance of R1 and the 2nd conductivity-type lateral electrode to R2.
[0010]In the light-emitting component according to claim 3 or 4, as for the light-emitting component according to claim 5, the 2nd conductivity-type lateral electrode contains a translucency electrode.
[0011]As for the light-emitting component according to claim 6, in the light-emitting component according to any one of claims 1 to 5, the number of 3 fellows nitride semiconductor light emitting elements is determined according to driver voltage.
[0012]In the light-emitting component according to any one of claims 1 to 6, as for the light-emitting component according to claim 7, 3 fellows nitride semiconductor light emitting element contains a GaN system light emitting device.
[0013]In the light-emitting component according to claim 1, since two or more 3 fellows nitride semiconductor light emitting elements are formed and connected on one substrate

using general IC manufacturing process, an interval of 3 fellows nitride semiconductor light emitting element which adjoins mutually can be made narrower than before. Therefore, it is formed as single parts and the surface light source with large luminescence intensity is acquired.
[0014]If two or more 3 fellows nitride semiconductor light emitting elements are connected in series so that it may indicate to claim 2, light quantity from a three fellows each nitride semiconductor light emitting element will be made equal.
[0015]A three fellows each nitride semiconductor light emitting element is arranged by linear shape so that it may indicate to claim 3, And connection of the 1st conductivity-type lateral electrode of one light emitting device of 3 fellows nitride semiconductor light emitting element which adjoins mutually, and the 2nd conductivity-type lateral electrode of a light emitting device of another side of internal wiring which has width will equalize more luminous intensity distributions in each 3 fellows nitride semiconductor light emitting element. If set as ** (resistance R1 of a semiconductor layer of the 1st conductivity type) (resistance R2 of the 2nd conductivity-type lateral electrode) indicate to claim 4, luminous intensity distributions in each 3 fellows nitride semiconductor light emitting element will be abbreviated-equalized.
[0016]If the number of 3 fellows nitride semiconductor light emitting elements is set up suit driver voltage of a device with which a light-emitting component is used so that it may indicate to claim 6, a light-emitting component applicable to various driver voltages will be obtained. The 2nd conductivity-type lateral electrode is formed of a translucency electrode, and as a 3 fellows nitride semiconductor light emitting element, for example, a GaN system light emitting device is used so that it may indicate to claim 7, so that it may indicate to claim 5.
[0017]
[Embodiment of the Invention]Hereafter, this embodiment of the invention is described with reference to drawings.
[0018]With reference to drawing 1 and drawing 2, as for the light-emitting component 10 of this embodiment of the invention, the four GaN (semiconductor which contains Ga and N at least) system light emitting diodes 14a-14d are formed on the insulating substrate 12, for example including the insulating substrates 12, such as silicon-on-sapphire Hitoshi.
[0019]Namely, on the insulating substrate 12, it corresponds to each GaN system light emitting diodes 14a-14d, The n type GaN layer (Si dope) 16 used as the electrode installation layer of 3.0 micrometers of thickness, the luminous layer 18 of 0.1 micrometer of thickness, and the p type GaN contact layer (Mg dope) 20 of 0.5 micrometer of thickness are formed in this order.
[0020]On each p type GaN contact layer 20, the translucency electrode 22 which is a p type lateral electrode is formed at surface state, and, [crosswise near the one end rim] on each n type GaN layer 16, the n type lateral electrode 24 is formed. The translucency electrode 22 and the n type lateral electrode 24 are formed in parallel so that drawing 1 may show well.
[0021]And each member on the insulating substrate 12 is covered with the protective film 26, and the series connection of the translucency electrode 22 and the n type lateral electrode 24 between adjoining GaN system light emitting diodes is carried out with the internal wiring 28 which has the predetermined width W1. At this time, the end of the internal wiring 28 is extended and formed [crosswise near the one end rim] on the

translucency electrode 22. Therefore, concerning one GaN system light emitting diode, in the connected part of the internal wiring 28 and the translucency electrode 22, the formation point of the n type lateral electrode 24 becomes near the edge of an opposite hand. The size of the width W1 of the internal wiring 28 is set up become for it to be a little smaller than the width W2 of the translucency electrode 22, and a little larger than length L of the n type lateral electrode 24 for example, so that drawing 1 may show.
[0022]The pad electrode 30 for connecting with external parts, respectively is connected to the translucency electrode 22 and the n type lateral electrode 24 of both ends. The pad electrode 30 as well as the internal electrode 28 is formed.
[0023]Thus, the light-emitting component 10 which carried out the series connection of the four GaN system light emitting diodes 14a-14d is obtained by connecting the translucency electrode 22 and the n type lateral electrode 24 via the internal wiring 28. The equivalent circuit of the light-emitting component 10 is shown in drawing 3.
[0024]An example of such a manufacturing method of the light-emitting component 10 is explained with reference to drawing 4.
[0025]First, as shown in drawing 4 (a), the n type GaN layer 16, the luminous layer 18, and the p type GaN contact layer 20 are grown epitaxially in this order by MOCVD (organometal chemistry vapor phase growth) on the insulating substrate 12, The p type GaN contact layer 20 of 3.0 micrometers of thickness, the n type GaN layer 16 of $N_D=10^{18}cm^{-3}$, the luminous layer 18 of 0.1 micrometer of thickness and 0.5 micrometer of thickness, and $N_A=10^{17}cm^{-3}$ is formed.
[0026]As shown in drawing 4 (b), by subsequently, the dry etching method which supplies photo lithography and gaseous chlorine with nickel mask by the pressure of 0.5 Pa. Etching removal of the p type GaN contact layer 20, the luminous layer 18, and the n type GaN layer 16 on the insulating substrate 12 is carried out, and the mesa 21 is formed. The depth of etching at this time is 0.8 micrometer.
[0027]As shown in drawing 4 (c), by the dry etching method which supplies photo lithography and gaseous chlorine with nickel mask by the pressure of 0.5 Pa, etching removal of the n type GaN layer 16 on the insulating substrate 12 is carried out, and the crevice 32 is formed so that the insulating substrate 12 may be exposed. The depth of etching is set to 3.6 micrometers and the layer which constitutes the GaN system light emitting diodes 14a-14d is separated by this, respectively.
[0028]As it continues and is shown in drawing 4 (d), by the electron beam evaporation by the pressure of $2x10^{-6}$torr. The Ni film of 2 nm of thickness and the Au membrane of 4 nm of thickness are formed in this order at the whole p type GaN contact layer 20 upper surface, and the translucency electrode 22 of surface state is formed of photo lithography. By the electron beam evaporation by the pressure of $2x10^{-6}$torr. On the n type GaN layer 16, the Ti film of 30 nm of thickness and the Al film of 500 nm of thickness are formed in this order, and the n type lateral electrode 24 prolonged by photo lithography [crosswise near the one end rim] on the n type GaN layer 16 is formed. The n type lateral electrode 24 is equivalent to the cathode terminal of a GaN system light emitting diode.
[0029]Then, as shown in drawing 4 (e), the protective film 26 which becomes the whole upper surface of the chip formed by drawing 4 (d) from SiO_2 of 300 nm of thickness is formed of electron beam evaporation.
[0030]Then, etching removal of the protective film 26 is carried out by photo lithography,

and an opening is carried out so that a part of each upper surface of the translucency electrode 22 and the n type lateral electrode 24 may be exposed. Concerning one GaN system light emitting diode at this time, the opening on the translucency electrode 22 is extended and formed [of an opposite hand / crosswise near the edge] with the formation point of the n type lateral electrode 24. The opening of the n type lateral electrode 24 is also prolonged crosswise, and is formed.

[0031]And as shown in drawing 4 (f), the Ni film of 100 nm of thickness and the Au membrane of 700 nm of thickness are formed in this order by the electron beam evaporation by the pressure of $2x10^{-6}$torr at the whole upper surface of the protective film 26, and the internal wiring 28 is formed of photo lithography. Therefore, concerning one GaN system light emitting diode, the internal wiring 28 connected to the internal wiring 28 and the n type lateral electrode 24 which are connected to the translucency electrode 22 will be pulled out by the counter direction from the both ends of a GaN system light emitting diode, respectively. Although not illustrated to drawing 4 (f), the pad electrode 30 is formed simultaneously similarly. The end part connected with the translucency electrode 22 among the internal wiring 28 and the pad electrode 30 is equivalent to the anode electrode of a GaN system light emitting diode.

[0032]Thus, the light-emitting component 10 in which the series connection of the four GaN system light emitting diodes 14a-14d was carried out is formed.

[0033]Since two or more GaN system light emitting diodes 14a-14d are formed and connected on the insulating substrate 12 of one sheet using general IC manufacturing process according to the luminescence intensity 10, the interval of the GaN system light emitting diode which adjoins mutually can be made narrower than before. Therefore, the light-emitting component 10 which is formed as single parts and is suitable as the surface light source with large luminescence intensity is obtained.

[0034]Since according to the light-emitting component 10 the GaN system light emitting diodes 14a-14d can be formed on the insulating substrate 12 at linear shape as shown in drawing 5 (a), luminescence of a large area is obtained so that drawing 5 (b) may show.

[0035]Since the GaN system light emitting diodes 14a-14d can be formed on the same insulating substrate 12, the insulated separation for GaN system light emitting diode 14a-14d and integration become easy.

[0036]Each GaN system light emitting diodes [14a-14d] luminous intensity distributions come to be shown in drawing 6. Setting resistance of Rt and the n type GaN layer 16 to Rn for resistance of the translucency electrode 22, Rp shows a part for resistance of the p type GaN contact layer 20, the contact resistance of the translucency electrode 22 and the p type GaN contact layer 20, and p-n junction phase-voltages this resistance, and each resistance presupposes it that it is thought in a field that it is fixed.

[0037]Since the n type lateral electrode 24 of one light emitting diode of the GaN system light emitting diode which each GaN system light emitting diodes 14a-14d are arranged by linear shape, and adjoins mutually, and the translucency electrode 22 of the light emitting diode of another side are connected by the internal wiring 28 which has the width W1, When resistance per unit area of the translucency electrode 22 is small (Rt**Rn), as shown in drawing 6 (a), current flows into the n type GaN layer 16 from the translucency electrode 22 whole surface, and the current which passes the luminous layer 18 becomes uniform irrespective of the position in the luminous layer 18. Therefore, as shown in drawing 6 (b) and (c), luminescence from the translucency electrode 22

becomes abbreviated homogeneity irrespective of a luminescence part, and bigger luminescence intensity is obtained.

[0038]Incidentally, when resistance per unit area of the translucency electrode 22 is strong (Rt>Rn), as shown in drawing 6 (d), the current which passes the luminous layer 18 is concentrated on the internal wiring 28, i.e., anode electrode vicinity. In this case, although the luminescence intensity in the X-X section shown in drawing 6 (e) becomes uneven, Since the n type lateral electrode 24 of one light emitting diode of the GaN system light emitting diode which each GaN system light emitting diodes 14a-14d are arranged by linear shape, and adjoins mutually, and the translucency electrode 22 of the light emitting diode of another side are connected by the internal wiring 28 which has the width W1, The luminescence intensity in the Y-Y section shown in drawing 6 (f) becomes abbreviated homogeneity. Therefore, from the case where resistance per unit area of the translucency electrode 22 mentioned above is small, luminescence intensity is equalized from unevenness and the conventional technology shown in drawing 9 at least, and luminescence intensity becomes large, although it becomes small.

[0039]As shown in drawing 7 (a) - (c), the GaN system light emitting diodes 14a-14d may be formed on the insulating substrate 12a, a series connection may be carried out to a U shape, and the light-emitting component which it is formed as single parts also in this case, and big luminescence intensity is obtained, and is suitable as the surface light source is obtained.

[0040]That is, the light-emitting component which it is formed as single parts, and big luminescence intensity is obtained, and can be applied to the surface light source is obtained by forming and carrying out the series connection of two or more GaN system light emitting diodes on an insulating substrate so that drawing 5 and drawing 7 may show.

[0041]In order to drive a GaN system light emitting diode, it is [more than 3V] required, and circuit operation is performed using 5V power supply in many cases. When 4V grade needs per GaN system light emitting diode (for example, when sending 20-mA current), and driver voltage is 24V, six GaN system light emitting diodes should just use the light-emitting component by which the series connection was carried out. Thus, by using the GaN system light emitting diode of the number of series elements according to driver voltage, luminescence of a large area is attained, and restriction of driver voltage also decreases, and the application covered in many fields can be expected.

[0042]As shown in drawing 8, current control elements, such as resistance (drawing 8 (a)) and FET (drawing 8 (b)), may be formed on the same insulating substrate with the GaN system light emitting diodes 14a-14n, In this case, the GaN system light emitting diodes 14a-14n and a current control element can be formed on the same insulating substrate at a monolithic.

[0043]Thus, since an external element becomes unnecessary, the small and lightweight light-emitting component 10 is obtained and not only the GaN system light emitting diodes 14a-14d but a current control element can be formed with a wide gap band material, The strong light-emitting component 10 is obtained to generation of heat, and integration becomes easy. Since an element is constituted only in the one side principal surface of an insulating substrate, general IC manufacturing process also in this case is applicable. Restriction of driver voltage decreases further by it not only adjusting the number of GaN system light emitting diodes, but adding a current control element. The

surge current at the time of an assembly and use can be controlled by adding resistance to the GaN system light emitting diodes 14a-14n.

[0044]Although the embodiment of drawing 1 described the case where the series connection of the four GaN system light emitting diodes 14a-14d was carried out, it cannot be overemphasized that the number of GaN system light emitting diodes is not limited to this.

[0045]In an above-mentioned embodiment, although the light emitting diode was explained to the example as a light emitting device, it may not be limited to this but may be laser.

[0046]As a 3 fellows nitride semiconductor light emitting element of the light-emitting component 10, if it is a light emitting device which consists of a 3 fellows nitride semiconductor which contains AlN, InN, BN, or InGaN, for example, arbitrary 3 fellows nitride semiconductor light emitting elements can be used.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a top view showing the principal part of one embodiment of this invention.
[Drawing 2]It is a sectional view showing the embodiment of drawing 1.
[Drawing 3]It is a representative circuit schematic showing the embodiment of drawing 1.
[Drawing 4]It is process drawing showing the manufacturing process of the embodiment of drawing 1.
[Drawing 5](a) is a top view showing typically the arrangement state of the GaN system light emitting diode in the embodiment of drawing 1, and (b) is a side view showing the luminescent state typically.
[Drawing 6]It is an illustration figure showing the flow of the current of a GaN system light emitting diode, and the outline of luminous intensity distributions, and as for (d) - (f), (a) - (c) shows the case where resistance of a translucency electrode is strong, respectively, when resistance of a translucency electrode is small.
[Drawing 7](a) is a representative circuit schematic showing other embodiments of this invention, (b) is a top view showing typically the arrangement state of the GaN system light emitting diode in that embodiment, and (c) is a side view showing that luminescent state typically.
[Drawing 8]It is a representative circuit schematic showing the embodiment of others of this invention, and that by which (a) added resistance to the GaN system light emitting diode, and (b) show, respectively what added FET to the GaN system light emitting diode.
[Drawing 9](a) is a top view showing conventional technology, and (b) is the end elevation.
[Description of Notations]
10 Light-emitting component
12 12a Insulating substrate
14a-14d, 14n GaN system light emitting diode
16 N type GaN buffer layer
18 Luminous layer
20 P type GaN contact layer
22 Translucency electrode
24 N type lateral electrode
26 Protective film
28 Internal wiring
30 Pad electrode
W1 Width of internal wiring

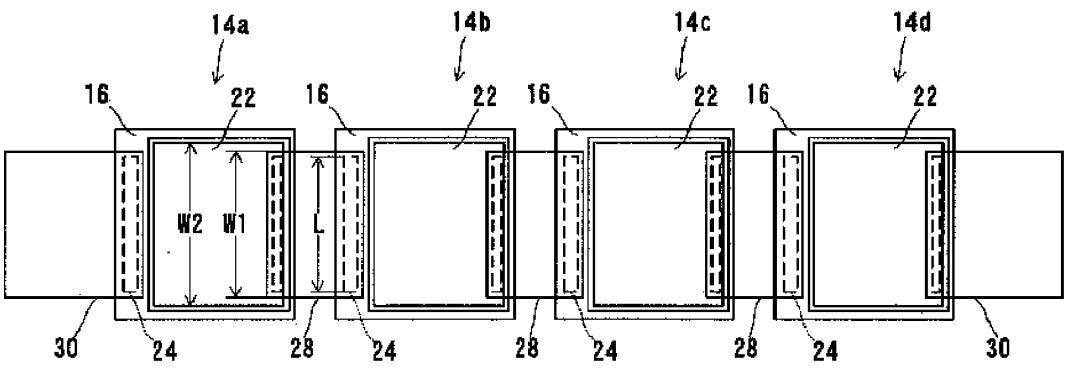
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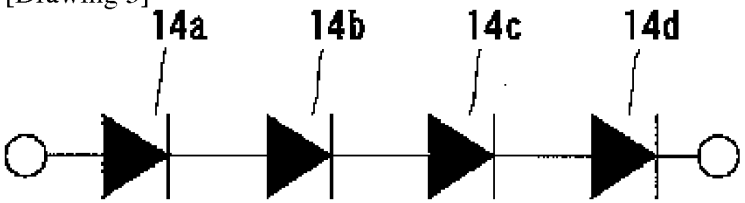
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DRAWINGS

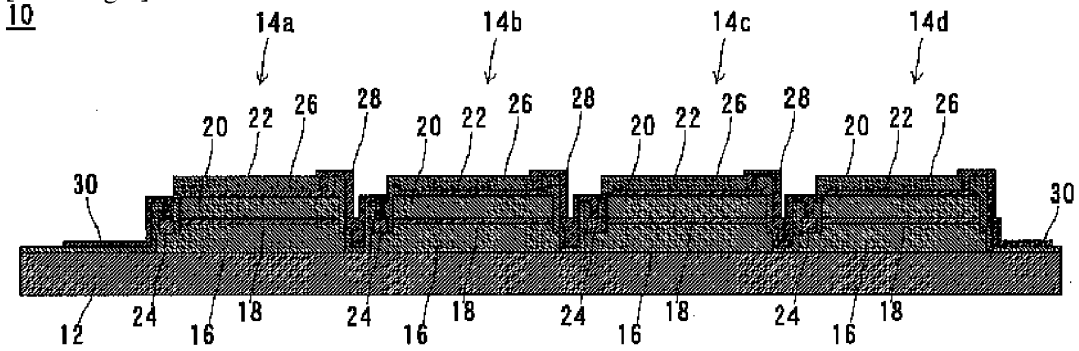
[Drawing 1]



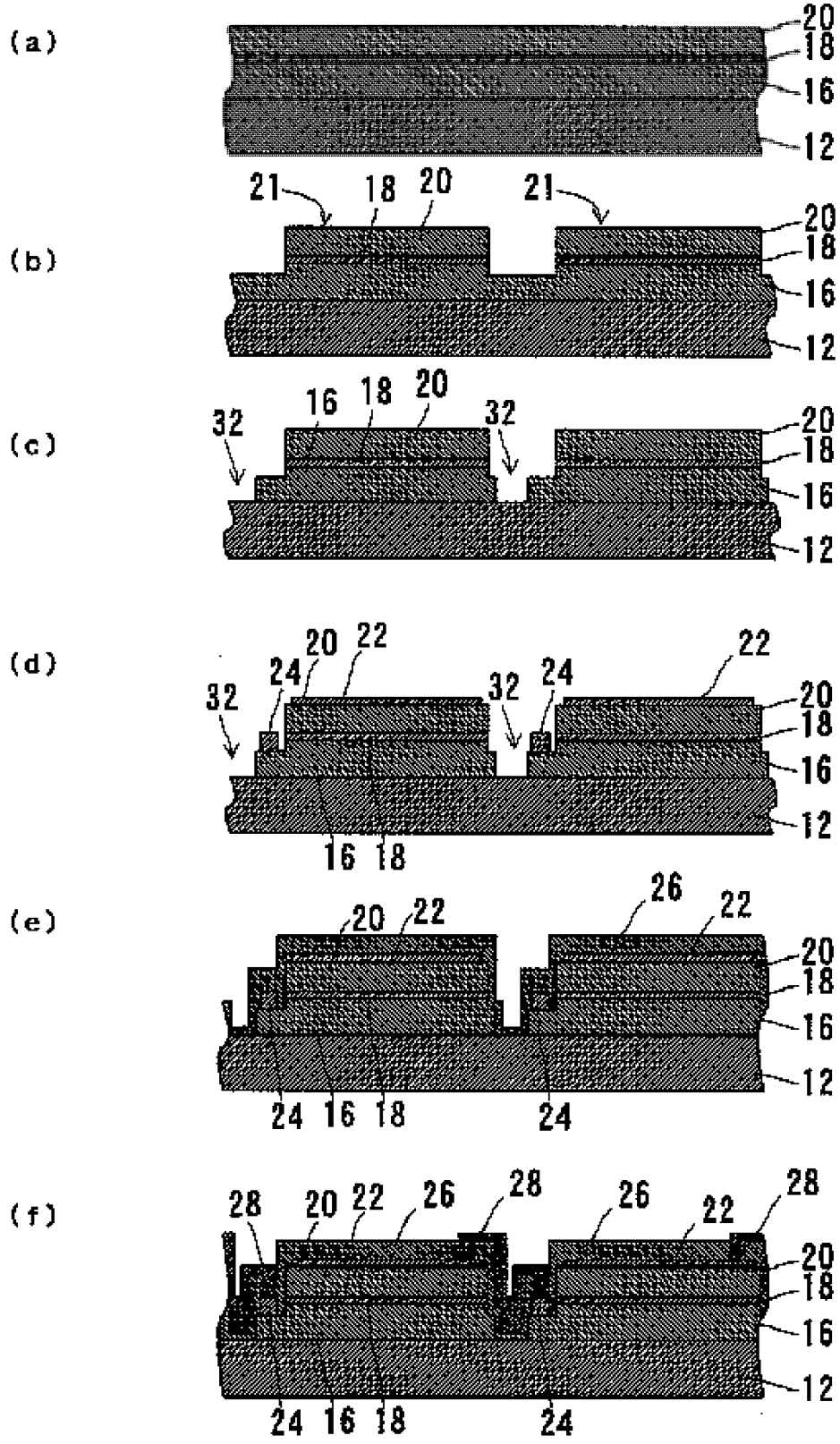
[Drawing 3]



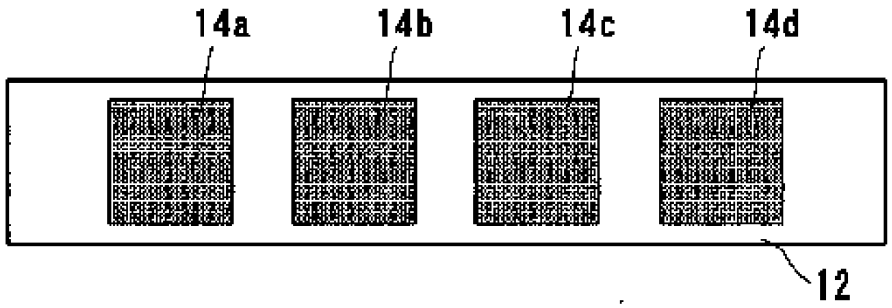
[Drawing 2]



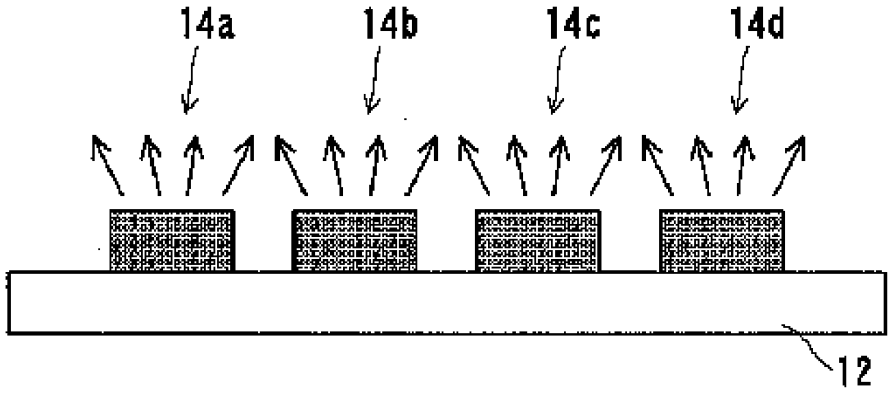
[Drawing 4]


(a)
20
18
16
12
(b)
21
18
20
21
20
18
16
12
(c)
32
16
18
20
32
20
18
16
12
(d)
20
22
24
32
32
24
22
20
18
16
12
16
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(e)
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22
26
22
20
18
16
12
24
16
18
24
(f)
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24

[Drawing 5]
(a)



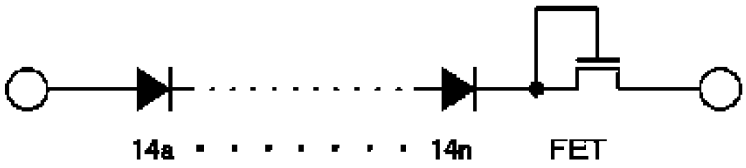
(b)



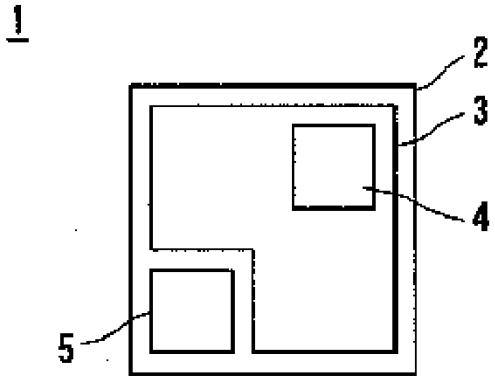
[Drawing 8]
(a)



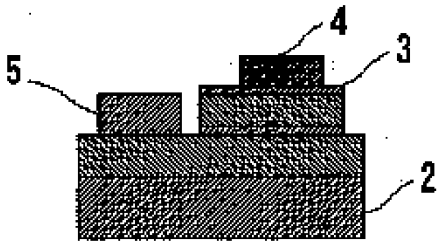
(b)



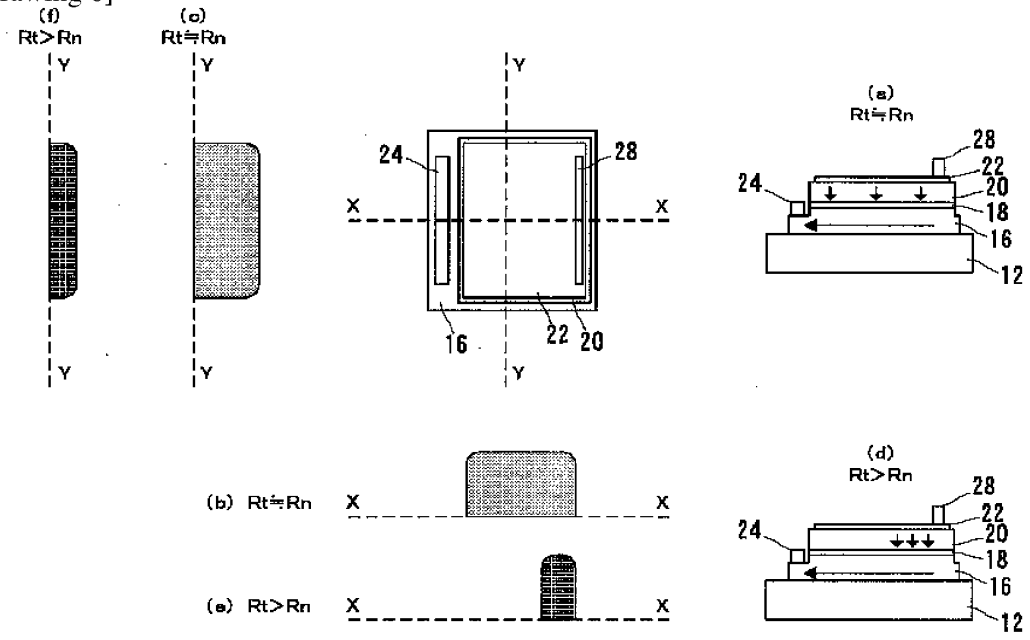
[Drawing 9]
(a)



(b)

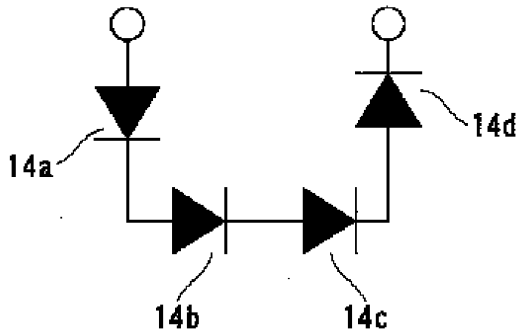


[Drawing 6]

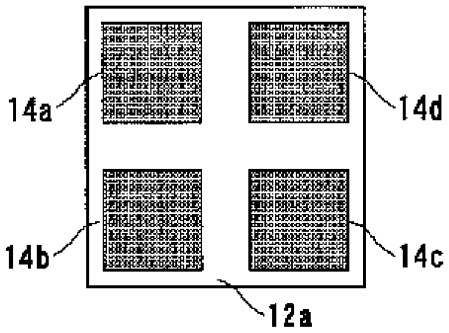

(f)
Rt>Rn
(c)
Rt≒Rn
Y
Y
Y
Y
Y
24
28
X
X
16
22
20
(a)
Rt≒Rn
28
22
20
18
16
12
24
(b) Rt≒Rn
X
X
(e) Rt>Rn
X
X
(d)
Rt>Rn
28
22
20
18
16
12
24

[Drawing 7]

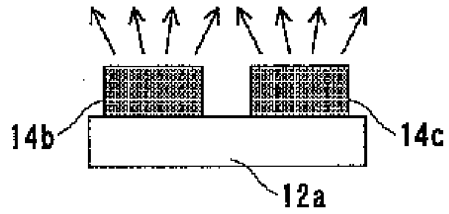
(a)



(b)



(c)



(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号

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(71)出願人　000001889
三洋電機株式会社
大阪府守口市京阪本通２丁目５番５号

(72)発明者　竹内　邦生
大阪府守口市京阪本通２丁目５番５号　三洋電機株式会社内

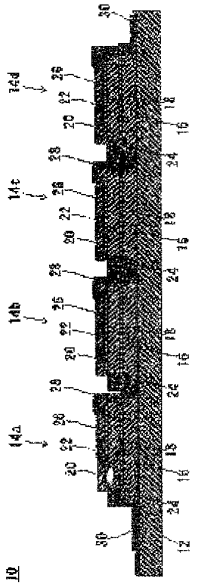
(74)代理人　弁理士　辰巳　忠宏

(54)【発明の名称】　発光部品

(57)【要約】

【課題】　単一の部品として形成されかつ大きな発光強度を有する面光源として適する発光部品を得る。

【解決手段】　絶縁性基板１２上に、各ＧａＮ系発光ダイオード１４ａ～１４ｄに対応して、ｎ型ＧａＮ層１６、発光層１８およびｐ型ＧａＮコンタクト層２０を、この順序で形成する。ｐ型ＧａＮコンタクト層２０上にはｐ型側電極である透光性電極２２を面状に形成し、ｎ型ＧａＮ層１６上の一端縁近傍かつ幅方向に延びてｎ型側電極２４を形成する。絶縁性基板１２上の各部材を保護膜２６で覆い、隣接するＧａＮ系発光ダイオード間の透光性電極２２とｎ型側電極２４とを幅を有する内部配線２８で直列接続し、両端の透光性電極２２およびｎ型側電極２４には、それぞれ外部の部品と接続するためのパッド電極３０を接続する。このようにして、１枚の絶縁性基板１２上に複数のＧａＮ系発光ダイオード１４ａ～１４ｄを直列接続した発光部品１０を得る。



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【特許請求の範囲】

【請求項１】　基板、および前記基板上にそれぞれ形成されかつ接続される複数の３族窒化物半導体発光素子を備える、発光部品。

【請求項２】　前記複数の３族窒化物半導体発光素子は直列に接続される、請求項１に記載の発光部品。

【請求項３】　前記各３族窒化物半導体発光素子は、前記基板上に形成される第１導電型の半導体層、前記第１導電型の半導体層上の一端縁近傍かつ幅方向に延びて形成される第１導電型側電極、前記第１導電性の半導体層上に形成される第２導電型の半導体層、および前記第２導電型の半導体層上に面状に形成される第２導電型側電極を含み、

前記各３族窒化物半導体発光素子は直線状に配列され、かつ相互に隣接する前記３族窒化物半導体発光素子の一方の発光素子の前記第１導電型側電極と他方の発光素子の前記第２導電型側電極とは幅を有する内部配線によって接続される、請求項１または２に記載の発光部品。

【請求項４】　前記第１導電型の半導体層の抵抗をＲ１、前記第２導電型側電極の抵抗をＲ２とすると、Ｒ１≒Ｒ２に設定される、請求項３に記載の発光部品。

【請求項５】　前記第２導電型側電極は透光性電極を含む、請求項３または４に記載の発光部品。

【請求項６】　前記３族窒化物半導体発光素子の数は駆動電圧に応じて決定される、請求項１ないし５のいずれかに記載の発光部品。

【請求項７】　前記３族窒化物半導体発光素子はＧａＮ系発光素子を含む、請求項１ないし６のいずれかに記載の発光部品。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】この発明は発光部品に関し、特にたとえば３族窒化物半導体発光素子を用いる発光部品に関する。

【０００２】

【従来の技術】図９に示すように、従来のＧａＮ系発光素子１としては、１つの絶縁性基板２上に、１つの透光性電極３、およびアノード電極４とカソード電極５とからなる一対のボンディング用のパッド電極が形成された、すなわち１つのチップに対して１ヶ所の発光部を有する、発光ダイオードが広く用いられてきた。

【０００３】

【発明が解決しようとする課題】従来のＧａＮ系発光素子１は発光部を１ヶ所しか有さないので、それ単独では面光源としては適さなかった。

【０００４】また、ＧａＮ系発光素子１では１つの絶縁性基板２上に１つの素子しか形成されないため、大面積の面光源を得ようとすると、複数のＧａＮ系発光素子１を基体上に配列して互いに接続する必要があるので相互に隣接するＧａＮ系発光素子１の間隔に限界があり、大

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きな発光強度を有する面光源を得られないという問題点があった。

【０００５】それゆえにこの発明の主たる目的は、単一の部品として形成されかつ大きな発光強度を有する面光源として適する、発光部品を提供することである。

【０００６】

【課題を解決するための手段】上記目的を達成するために、請求項１に記載の発光部品は、基板、および基板上にそれぞれ形成されかつ接続される複数の３族窒化物半導体発光素子を備える。

【０００７】請求項２に記載の発光部品は、請求項１に記載の発光部品において、複数の３族窒化物半導体発光素子は直列に接続されるものである。

【０００８】請求項３に記載の発光部品は、請求項１または２に記載の発光部品において、各３族窒化物半導体発光素子は、基板上に形成される第１導電型の半導体層、第１導電型の半導体層上の一端縁近傍かつ幅方向に延びて形成される第１導電型側電極、第１導電性の半導体層上に形成される第２導電型の半導体層、および第２導電型の半導体層上に面状に形成される第２導電型側電極を含み、各３族窒化物半導体発光素子は直線状に配列され、かつ相互に隣接する３族窒化物半導体発光素子の一方の発光素子の第１導電型側電極と他方の発光素子の第２導電型側電極とは幅を有する内部配線によって接続されるものである。

【０００９】請求項４に記載の発光部品は、請求項３に記載の発光部品において、第１導電型の半導体層の抵抗をＲ１、第２導電型側電極の抵抗をＲ２とすると、Ｒ１≒Ｒ２に設定されるものである。

【００１０】請求項５に記載の発光部品は、請求項３または４に記載の発光部品において、第２導電型側電極は透光性電極を含むものである。

【００１１】請求項６に記載の発光部品は、請求項１ないし５のいずれかに記載の発光部品において、３族窒化物半導体発光素子の数は駆動電圧に応じて決定されるものである。

【００１２】請求項７に記載の発光部品は、請求項１ないし６のいずれかに記載の発光部品において、３族窒化物半導体発光素子はＧａＮ系発光素子を含むものである。

【００１３】請求項１に記載の発光部品では、一般のＩＣ製造プロセスを用いて１枚の基板上に複数の３族窒化物半導体発光素子が形成されかつ接続されるので、相互に隣接する３族窒化物半導体発光素子の間隔を従来よりも狭くできる。したがって、単一の部品として形成されかつ発光強度が大きい面光源が得られる。

【００１４】請求項２に記載するように、複数の３族窒化物半導体発光素子が直列に接続されると、各３族窒化物半導体発光素子からの発光量が等しくされる。

【００１５】請求項３に記載するように、各３族窒化物

半導体発光素子は直線状に配列され，かつ相互に隣接する３族窒化物半導体発光素子の一方の発光素子の第１導電型側電極と他方の発光素子の第２導電型側電極とが幅を有する内部配線によって接続されると、個々の３族窒化物半導体発光素子における発光強度分布はより均一化される。請求項４に記載するように，（第１導電型の半導体層の抵抗Ｒ１）≒（第２導電型側電極の抵抗Ｒ２）に設定されると，個々の３族窒化物半導体発光素子における発光強度分布は略均一化される。

【００１６】また，請求項６に記載するように，３族窒化物半導体発光素子の数が，発光部品が用いられる装置の駆動電圧に適合するように設定されると、さまざまな駆動電圧に適用可能な発光部品が得られる。なお，請求項５に記載するように，第２導電型側電極は透光性電極によって形成され，請求項７に記載するように，３族窒化物半導体発光素子としてはたとえばＧａＮ系発光素子が用いられる。

【００１７】

【発明の実施の形態】以下，この発明の実施の形態について，図面を参照して説明する。

【００１８】図１および図２を参照して，この発明の実施の形態の発光部品１０は，たとえばサファイア基板等などの絶縁性基板１２を含み，絶縁性基板１２上に４個のＧａＮ（少なくともＧａ，Ｎを含む半導体）系発光ダイオード１４ａ～１４ｄが形成されるものである。

【００１９】すなわち、絶縁性基板１２上には，各ＧａＮ系発光ダイオード１４ａ～１４ｄに対応して，層厚３．０μｍの電極設置層となるｎ型ＧａＮ層（Ｓｉドープ）１６，層厚０．１μｍの発光層１８，および層厚０．５μｍのｐ型ＧａＮコンタクト層（Ｍｇドープ）２０が，この順序で形成される。

【００２０】また，各ｐ型ＧａＮコンタクト層２０上にはｐ型側電極である透光性電極２２が面状に形成され，各ｎ型ＧａＮ層１６上の一端縁近傍かつ幅方向にはｎ型側電極２４が形成される。図１からよくわかるように，透光性電極２２とｎ型側電極２４とは平行に形成される。

【００２１】そして，絶縁性基板１２上の各部材は保護膜２６によって覆われ，隣接するＧａＮ系発光ダイオード間の透光性電極２２とｎ型側電極２４とは所定の幅Ｗ１を有する内部配線２８によって直列接続される。このとき，内部配線２８の一端は透光性電極２２上の一端縁近傍かつ幅方向に延びて形成される。したがって，１つのＧａＮ系発光ダイオードに関していえば、内部配線２８と透光性電極２２との接続箇所は，ｎ型側電極２４の形成箇所とは反対側の端縁近傍となる。なお，図１からわかるように，内部配線２８の幅Ｗ１の寸法は，たとえば，透光性電極２２の幅Ｗ２よりやや小さくかつｎ型側電極２４の長さＬよりやや大きくなるように設定される。

【００２２】さらに，両端の透光性電極２２およびｎ型側電極２４には，それぞれ外部の部品と接続するためのパッド電極３０が接続される。パッド電極３０も内部電極２８と同様に形成される。

【００２３】このように，内部配線２８を介して透光性電極２２とｎ型側電極２４とを接続することによって、４個のＧａＮ系発光ダイオード１４ａ～１４ｄを直列接続した発光部品１０が得られる。発光部品１０の等価回路が図３に示される。

【００２４】このような発光部品１０の製造方法の一例を，図４を参照して説明する。

【００２５】まず，図４（ａ）に示すように，絶縁性基板１２上に，ｎ型ＧａＮ層１６，発光層１８およびｐ型ＧａＮコンタクト層２０をＭＯＣＶＤ（有機金属化学気相成長法）によってこの順序でエピタキシャル成長させ，膜厚３．０μｍ，$N_D = 10^{18}\,cm^{-3}$のｎ型ＧａＮ層１６，膜厚０．１μｍの発光層１８，および膜厚０．５μｍ，$N_A = 10^{18}\,cm^{-3}$のｐ型ＧａＮコンタクト層２０が形成される。

【００２６】ついで，図４（ｂ）に示すように，N_2マスクによるフォトリソグラフィーおよび塩素ガスを０．５Ｐａの圧力で供給するドライエッチング法によって，絶縁性基板１２上のｐ型ＧａＮコンタクト層２０，発光層１８およびｎ型ＧａＮ層１６がエッチング除去され，メサ２１が形成される。このときのエッチングの深さは０．８μｍである。

【００２７】さらに，図４（ｃ）に示すように，N_2マスクによるフォトリソグラフィーおよび塩素ガスを０．５Ｐａの圧力で供給するドライエッチング法によって，絶縁性基板１２上のｎ型ＧａＮ層１６がエッチング除去され，絶縁性基板１２が露出するように凹部３２が形成される。これによって、エッチングの深さは３．６μｍとなり，ＧａＮ系発光ダイオード１４ａ～１４ｄを構成する層がそれぞれ分離される。

【００２８】つづいて，図４（ｄ）に示すように，2×10^{-6}ｔｏｒｒの圧力による電子ビーム蒸着によって，ｐ型ＧａＮコンタクト層２０上面全体に，膜厚２ｎｍのＮｉ膜および膜厚４ｎｍのＡｕ膜がこの順序で成膜され，フォトリソグラフィーによって面状の透光性電極２２が形成される。また，2×10^{-6}ｔｏｒｒの圧力による電子ビーム蒸着によって，ｎ型ＧａＮ層１６上に，膜厚３０ｎｍのＴｉ膜および膜厚５００ｎｍのＡｌ膜がこの順序で成膜され，フォトリソグラフィーによってｎ型ＧａＮ層１６上の一端縁近傍かつ幅方向に延びたｎ型側電極２４が形成される。ｎ型側電極２４はＧａＮ系発光ダイオードのカソード電極に相当する。

【００２９】その後，図４（ｅ）に示すように，図４（ｄ）で形成されたチップの上面全体に膜厚３００ｎｍのSiO_2からなる保護膜２６が電子ビーム蒸着によって形成される。

【００３０】その後、透光性電極２２およびｎ型側電極２４のそれぞれの上面の一部が露出するように、フォトリソグラフィーによって保護膜２６がエッチング除去されて開口される。このとき、１つのＧａＮ系発光ダイオードに関していえば、透光性電極２２上の開口はｎ型側電極２４の形成箇所とは反対側の端縁近傍かつ幅方向に延びて形成される。また、ｎ型側電極２４の開口も幅方向に延びて形成される。

【００３１】そして、図４（ｆ）に示すように、２×１０⁻⁶ｔｏｒｒの圧力による電子ビーム蒸着によって、保護膜２６の上面全体に膜厚１００ｎｍのＮｉ膜および膜厚７００ｎｍのＡｕ膜がこの順序で成膜され、フォトリソグラフィーによって内部配線２８が形成される。したがって、１つのＧａＮ系発光ダイオードに関していえば、透光性電極２２に接続される内部配線２８およびｎ型側電極２４に接続される内部配線２８は、ＧａＮ系発光ダイオードの両端からそれぞれ反対方向に引き出されることになる。なお、図４（ｆ）には図示しないが、パッド電極３０も同様にして同時に形成される。内部配線２８およびパッド電極３０のうち、透光性電極２２と接続される一端部が、ＧａＮ系発光ダイオードのアノード電極に相当する。

【００３２】このようにして、４個のＧａＮ系発光ダイオード１４ａ～１４ｄが直列接続された発光部品１０が形成される。

【００３３】発光強度１０によれば、一般のＩＣ製造プロセスを用いて１枚の絶縁性基板１２上に複数のＧａＮ系発光ダイオード１４ａ～１４ｄが形成されかつ接続されるので、相互に隣接するＧａＮ系発光ダイオードの間隔を従来よりも狭くできる。したがって、単一の部品として形成されかつ発光強度が大きい面光源として適する発光部品１０が得られる。

【００３４】また、発光部品１０によれば、図５（ａ）にも示すように、絶縁性基板１２上にＧａＮ系発光ダイオード１４ａ～１４ｄを直線状に形成することができるので、図５（ｂ）からわかるように、大面積の発光が得られる。

【００３５】また、同一の絶縁性基板１２上にＧａＮ系発光ダイオード１４ａ～１４ｄを形成できるので、ＧａＮ系発光ダイオード１４ａ～１４ｄ間の絶縁分離、集積化が容易になる。

【００３６】各ＧａＮ系発光ダイオード１４ａ～１４ｄの発光強度分布は図６に示すようになる。透光性電極２２の抵抗をＲｔ、ｎ型ＧａＮ層１６の抵抗をＲｎとし、Ｒｐは、ｐ型ＧａＮコンタクト層２０の抵抗、透光性電極２２とｐ型ＧａＮコンタクト層２０との接触抵抗およびｐ－ｎ接合電圧相当抵抗分を示し、各抵抗は面内において一定と考えるとする。

【００３７】各ＧａＮ系発光ダイオード１４ａ～１４ｄは直線状に配列され、かつ相互に隣接するＧａＮ系発光ダイオードの一方の発光ダイオードのｎ型側電極２４と他方の発光ダイオードの透光性電極２２とが幅Ｗ１を有する内部配線２８によって接続されているので、透光性電極２２の単位面積当たりの抵抗が小さい場合（Ｒｔ≒Ｒｎ）には、図６（ａ）に示すように、透光性電極２２全面からｎ型ＧａＮ層１６に電流が流れ、発光層１８を通過する電流は発光層１８内の位置に拘わらず均一になる。したがって、図６（ｂ）および（ｃ）に示すように、透光性電極２２からの発光は発光箇所に拘わらず略均一になり、かつより大きな発光強度が得られる。

【００３８】因みに、透光性電極２２の単位面積当たりの抵抗が大きい場合（Ｒｔ＞Ｒｎ）には、図６（ｄ）に示すように、発光層１８を通過する電流は内部配線２８すなわちアノード電極近傍に集中する。この場合、図６（ｅ）に示すＸ－Ｘ断面における発光強度は不均一になるが、各ＧａＮ系発光ダイオード１４ａ～１４ｄは直線状に配列され、かつ相互に隣接するＧａＮ系発光ダイオードの一方の発光ダイオードのｎ型側電極２４と他方の発光ダイオードの透光性電極２２とが幅Ｗ１を有する内部配線２８によって接続されているので、図６（ｆ）に示すＹ－Ｙ断面における発光強度は略均一になる。したがって、上述した透光性電極２２の単位面積当たりの抵抗が小さい場合より発光強度は不均一かつ小さくなるが、少なくとも図９に示す従来技術より発光強度は均一化されかつ大きくなる。

【００３９】さらに、図７（ａ）～（ｃ）に示すように、絶縁性基板１２ａ上にＧａＮ系発光ダイオード１４ａ～１４ｄを形成しコ字状に直列接続してもよく、この場合にも、単一の部品として形成されかつ大きな発光強度が得られ面光源として適する発光部品が得られる。

【００４０】すなわち、図５および図７からわかるように、絶縁性基板上に複数個のＧａＮ系発光ダイオードを形成し直列接続することによって、単一の部品として形成されかつ大きな発光強度が得られ面光源に応用できる発光部品が得られる。

【００４１】なお、ＧａＮ系発光ダイオードを駆動するには、３Ｖ以上必要であり、５Ｖ電源を用いて回路動作を行うことが多い。１つのＧａＮ系発光ダイオードあたり４Ｖ（たとえば２０ｍＡの電流を流す場合）程度必要とすると、駆動電圧が２４Ｖの場合には６つのＧａＮ系発光ダイオードが直列接続された発光部品を用いればよい。このように、駆動電圧に応じた直列素子数のＧａＮ系発光ダイオードを用いることによって、大面積の発光が可能となり、かつ駆動電圧の制限も少なくなり、多方面にわたる応用が期待できる。

【００４２】また、図８に示すように、ＧａＮ系発光ダイオード１４ａ～１４ｎとともに抵抗（図８（ａ））やＦＥＴ（図８（ｂ））などの電流制御素子が同一絶縁性基板上に形成されてもよく、この場合、ＧａＮ系発光ダイオード１４ａ～１４ｎと電流制御素子とを同一の絶縁

性基板上にモノリシックに形成できる。

【００４３】このように外付け素子が不要になるため、小型かつ軽量の発光部品１０が得られ、また、ＧａＮ系発光ダイオード１４ａ～１４ｄだけではなく電流制御素子をもワイドギャップバンド材料によって形成できるので、発熱に対して強い発光部品１０が得られ、集積化が容易となる。さらに、絶縁性基板の一方主面にのみ素子を構成するので、この場合にも一般的なＩＣ製造プロセスを適用できる。また、ＧａＮ系発光ダイオードの数を調整するだけではなく電流制御素子を付加することにより、駆動電圧の制限がさらに少なくなる。さらに、ＧａＮ系発光ダイオード１４ａ～１４ｎに抵抗を付加することによって、組立時や使用時におけるサージ電流を抑制することができる。

【００４４】図１の実施の形態では、４個のＧａＮ系発光ダイオード１４ａ～１４ｄを直列接続する場合について述べたが、ＧａＮ系発光ダイオードの数はこれに限定されないことはいうまでもない。

【００４５】また、上述の実施の形態では、発光素子として発光ダイオードを例に説明したが、これに限定されず、レーザであってもよい。

【００４６】さらに、発光部品１０の３族窒化物半導体発光素子としては、たとえばＡｌＮ、ＩｎＮ、ＢＮまたはＩｎＧａＮなどを含む３族窒化物半導体からなる発光素子であれば、任意の３族窒化物半導体発光素子を用いることができる。

【００４７】

【発明の効果】この発明によれば、１つの基板上に発光部を複数形成でき、単一の部品として形成されかつ大きな発光強度が得られ面光源として適する発光部品が得られる。

【図面の簡単な説明】

【図１】この発明の一実施形態の主要部を示す平面図である。

【図２】図１の実施形態を示す断面図である。

＊【図３】図１の実施形態を示す等価回路図である。

【図４】図１の実施形態の製造プロセスを示す工程図である。

【図５】（ａ）は図１の実施形態におけるＧａＮ系発光ダイオードの配置状態を模式的に示す平面図であり、（ｂ）はその発光状態を模式的に示す側面図である。

【図６】ＧａＮ系発光ダイオードの電流の流れおよび発光強度分布の概略を示す図解図であり、（ａ）～（ｃ）は透光性電極の抵抗が小さい場合、（ｄ）～（ｆ）は透光性電極の抵抗が大きい場合をそれぞれ示す。

【図７】（ａ）はこの発明の他の実施の形態を示す等価回路図であり、（ｂ）はその実施の形態におけるＧａＮ系発光ダイオードの配置状態を模式的に示す平面図であり、（ｃ）はその発光状態を模式的に示す側面図である。

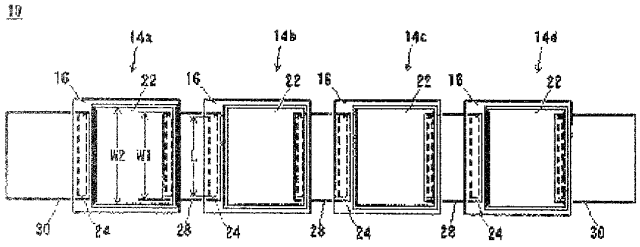
【図８】この発明のその他の実施の形態を示す等価回路図であり、（ａ）はＧａＮ系発光ダイオードに抵抗を付加したもの、（ｂ）はＧａＮ系発光ダイオードにＦＥＴを付加したものをそれぞれ示す。

【図９】（ａ）は従来技術を示す平面図であり、（ｂ）はその端面図である。

【符号の説明】

１０	発光部品
１２．１２ａ	絶縁性基板
１４ａ～１４ｄ．１４ｎ	ＧａＮ系発光ダイオード
１６	ｎ型ＧａＮバッファ層
１８	発光層
２０	ｐ型ＧａＮコンタクト層
２２	透光性電極
２４	ｎ型側電極
２６	保護膜
２８	内部配線
３０	パッド電極
Ｗ１	内部配線の幅

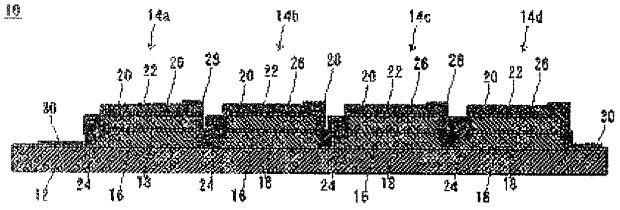
【図１】



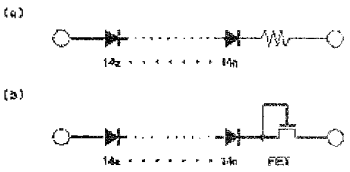
【図３】



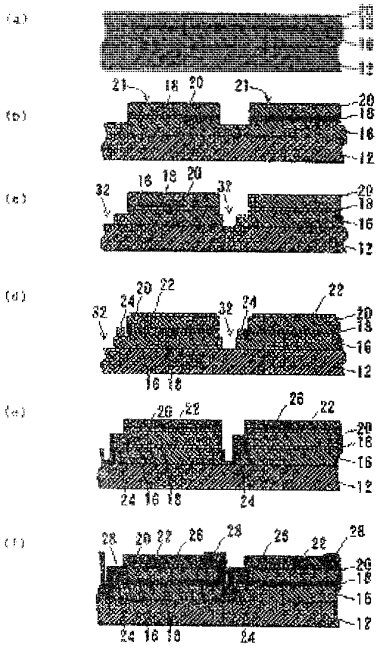
【図2】



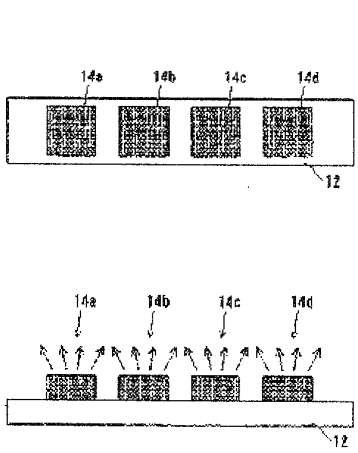
【図8】



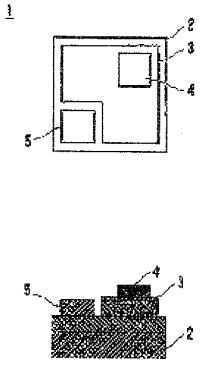
【図4】



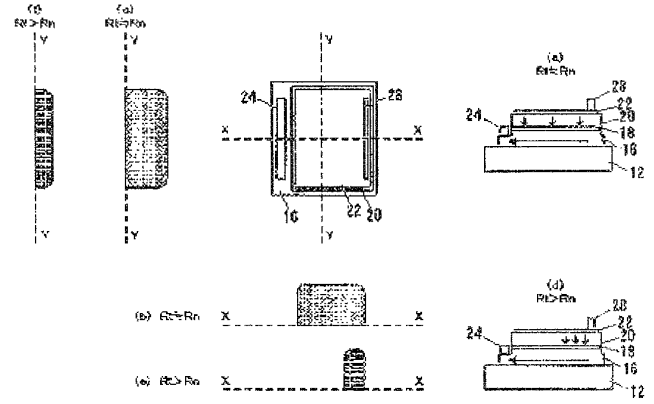
【図5】



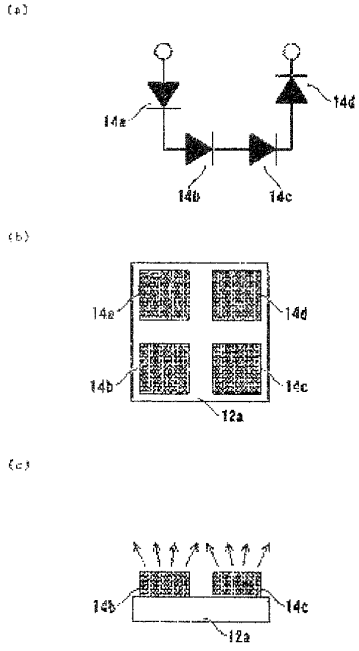
【図9】



【図６】



【図７】



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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P2317USD1
	Application Number	
Title of Invention	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
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Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jong	Lam	LEE	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Pohang-si	Country Of Residence[i]	KR
Citizenship under 37 CFR 1.41(b) [i]	KR		

Mailing Address of Applicant:

Address 1	8-1403, Gyosu Apt., Jigok-Dong, Nam-gu		
Address 2	Gyeongsangbuk-do		
City	Pohang-si	State/Province	
Postal Code	790-751	Country[i]	KR

Applicant 2 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jae	Ho	LEE	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Yongin-si	Country Of Residence[i]	KR
Citizenship under 37 CFR 1.41(b) [i]	KR		

Mailing Address of Applicant:

Address 1	309-1405, LG 3-cha Village Apt.		
Address 2	Seongbok-dong, Suji-gu, Gyeonggi-do		
City	Yongin-si	State/Province	
Postal Code	448-531	Country[i]	KR

Applicant 3 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Yeo	Jin	YOON	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Ansan-si	Country Of Residence[i]	KR

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P2317USD1
	Application Number	
Title of Invention	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME	

Citizenship under 37 CFR 1.41(b) i	KR		
Mailing Address of Applicant:			
Address 1	101-1505, Yojin Supsok Apt., Sa 1-dong, Sagnok-gu		
Address 2	Gyeonggi-do		
City	Ansan-si	**State/Province**	
Postal Code	426-738	**Country**i	KR

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Applicant Authority ◉ Inventor	○ Legal Representative under 35 U.S.C. 117	○ Party of Interest under 35 U.S.C. 118		
Prefix	**Given Name**	**Middle Name**	**Family Name**	**Suffix**
	Eu	Jin	HWANG	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Ansan-si	**Country Of Residence**i	KR
Citizenship under 37 CFR 1.41(b) i	KR		

Mailing Address of Applicant:			
Address 1	303, 1569-7, Jeongwang-dong		
Address 2	Gyeonggi-do		
City	Siheung-si	**State/Province**	
Postal Code	429-856	**Country**i	KR

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Applicant Authority ◉ Inventor	○ Legal Representative under 35 U.S.C. 117	○ Party of Interest under 35 U.S.C. 118		
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	Dae	Won	KIM	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Gireum-dong	**Country Of Residence**i	KR
Citizenship under 37 CFR 1.41(b) i	KR		

Mailing Address of Applicant:			
Address 1	303-802, Gireum New Town, 1280-2		
Address 2	Gireum-dong, Songbuk-gu		
City	Seoul	**State/Province**	
Postal Code	136-110	**Country**i	KR

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P2317USD1
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Attorney Docket Number	P2317USD1	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	12	Suggested Figure for Publication (if any)	

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Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Division of	11993965	2007-12-26
Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
11993965	a 371 of international	PCT/KR2006/002427	2006-06-22

PTO/SB/14 (07-07)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P2317USD1
	Application Number	
Title of Invention	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME	

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Remove

Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
10-2005-0053797	KR	2005-06-22	(•) Yes ( ) No

Remove

Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
10-2005-0055179	KR	2005-06-24	(•) Yes ( ) No

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Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
10-2006-0021801	KR	2006-03-08	(•) Yes ( ) No

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Assignee 1 Remove

If the Assignee is an Organization check here. ☒			
Organization Name	SEOUL OPTO DEVICE CO., LTD.		
Mailing Address Information:			
Address 1	1-36 Block, 727-5 Wonsi-dong, Danwon-gu		
Address 2	Gyeonggi-do		
City	Ansan-si	**State/Province**	
Country [i] KR		Postal Code	425-851
Phone Number		Fax Number	
Email Address			

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Signature:

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Signature	/hae-chan park/			Date (YYYY-MM-DD)	2009-11-05
First Name	Hae-Chan	Last Name	Park	Registration Number	50114

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Application Number:	
Filing Date:	
Title of Invention:	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jong Lam LEE
Filer:	Hae-Chan Park/karim sosa
Attorney Docket Number:	P2317USD1

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1090**

Electronic Acknowledgement Receipt	
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First Named Inventor/Applicant Name:	Jong Lam LEE
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1		Specification.pdf	197059 493b42e8e5401e8337edd6b0793400cfaeb370c7	yes	57
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Specification		1	52	
	Claims		53	56	
	Abstract		57	57	
Warnings:					
Information:					
2	Drawings-only black and white line drawings	Drawings.pdf	265548 28f9a9e8fe4a3a49080008bc0879a83396ddb769	no	12
Warnings:					
Information:					
3	Oath or Declaration filed	Declaration.pdf	175678 619b2fbd3d9e83778898fb0296d273f36a670704	no	4
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Warnings:					
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6	Foreign Reference	JP11-150303.pdf	1954573 999af3f1e09a0d18d42904a4ce5d4359793a7a5e	no	33
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LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of U.S. Application No. 11/993,965 filed on December 26, 2007, which is the National Stage of International Application No. PCT/KR06/02427 filed on June 22, 2006, and claims priority from and the benefit of Korean Patent Application No. 10-2005-0053797, filed on June 22, 2005, Korean Patent Application No. 10-2005-0055179, filed on June 24, 2005, and Korean Patent Application No. 10-2006-0021801, filed on March 8, 2006, which are hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] FIELD OF INVENTION

[0001] The present invention relates to a light emitting device and a method of manufacturing the same. More particularly, the present invention relates to a nitride based semiconductor light emitting device with enhanced luminous efficiency and brightness and a method of manufacturing the light emitting device.

[0003] Description of the Related Art

[0002] A light emitting device refers to an element in which minority carriers (electrons or holes) injected using a p-n junction structure of a semiconductor are produced and certain

light is emitted due to recombination of the carriers. A light emitting source is formed from any one or combination of compound semiconductor materials such as GaAs, AlGaAs, GaN, InGaN and AlGaInP, so that a variety of colors can be implemented. For example, a red light emitting device may be formed from GaAsP or the like; a green light emitting device may be formed from GaP, InGaN or the like; a blue light emitting device may be formed using an InGaN/GaN double hetero structure; and a UV light emitting device may be formed using an AlGaN/GaN or AlGaN/AlGaN structure.

[0003] In particular, GaN has a direct bandgap of 3.4eV at a normal temperature and a direct energy bandgap of 1.9eV (InN) to 3.4eV (GaN) or 6.2eV (AlN) by combining with a substance such as InN or AlN. Thus, GaN is a substance with great applicability to an optical element due to its broad wavelength range from visible light to ultraviolet light. Since the wavelength can be adjusted in such a manner, full-color implementation can be made by means of red, green and blue light emitting devices with a short wavelength range, so that the applicability to a general illumination market as well as a display device market is expected to be greatly increased.

[0004] Light emitting devices have characteristics of lower power consumption, longer lifespan, better installation in a narrow space and stronger resistance against vibration as compared with existing bulbs or fluorescent lamps. Since the light emitting devices are used as

display devices and backlights and have superior characteristics in view of the reduction in power consumption and the durability, many studies for applying the light emitting devices to a general illumination field have been recently conducted. In the future, their applicability is expected to extend to a backlight of a large-sized LCD-TV, a vehicle headlight and general illumination. To this end, it is necessary to improve luminous efficiency of light emitting devices, solve a heat dissipation problem, and achieve high brightness and output of the light emitting devices.

[0005] Many techniques for enhancing the performance of light emitting devices have been currently developed. There are various indexes indicating the performance of light emitting devices, such as luminous efficiency (lm/W), internal quantum efficiency (%), external quantum efficiency (%) and extraction efficiency (%). The extraction efficiency is determined as a ratio of electrons injected into the light emitting device to photons emitted to the outside of the light emitting device. That is, the light emitting device becomes bright as the extraction efficiency becomes high. Since the extraction efficiency of the light emitting device is much influenced by the shape and surface pattern of a chip, the structure of a chip and a packaging type, careful attention should be paid when designing the light emitting device.

[0006] Fig. 1 is a sectional view showing a conventional light emitting device with a horizontal structure.

[0007] Referring to Fig. 1, the light emitting device comprises a substrate 1, an N-type semiconductor layer 2 formed on the substrate 1, an active layer 3 formed on a portion of the N-type semiconductor layer 2 and a P-type semiconductor layer 4. That is, after the N-type semiconductor layer 2, the active layer 3 and the P-type semiconductor layer 4 have been sequentially formed on the substrate 1, predetermined regions of the P-type semiconductor layer 4 and the active layer 3 are etched to expose a portion of the N-type semiconductor layer 2. Then, a predetermined voltage is applied to top surfaces of the exposed N-type semiconductor layer 2 and the P-type semiconductor layer 4.

[0008] Fig. 2 is a sectional view showing a conventional light emitting device with a flip chip structure.

[0009] Referring to Fig. 2, the light emitting device comprises an N-type semiconductor layer 2, an active layer 3 and a P-type semiconductor layer 4, which are sequentially formed on a base substrate 1. The light emitting device further comprises a submount substrate 5 onto which the base substrate 1 is flip-chip bonded using metal bumps 8 and 9. To this end, the N-type semiconductor layer 2, the active layer 3 and the P-type semiconductor layer 4 are sequentially formed on the predetermined substrate 1, and portions of the P-type semiconductor layer 4 and the active layer 3 are etched to expose the N-type semiconductor layer 2 such that a light emitting cell can be formed. Further, the additional submount substrate 5 is prepared to form first

and second electrodes 6 and 7 thereon, and the P-type and N-type metal bumps 8 and 9 are then formed on the first and second electrodes 6 and 7, respectively. Thereafter, the light emitting cell is bonded with the submount substrate 5 such that P and N electrodes of the light emitting cell are bonded with the P-type and N-type metal bumps 8 and 9, respectively, to fabricate a light emitting device. Since such a conventional light emitting device with a flip chip structure has high heat dissipation efficiency and hardly has shield of light, there is an advantage in that its light efficiency is increased by 50% or more as compared with a conventional light emitting device. Further, since a gold wire for driving a light emitting device is not necessary, many applications to a variety of small-sized packages can be considered.

[0010] Light produced from a light emitting layer of a light emitting device is emitted from all the surfaces of a chip, and light extraction efficiency is generally determined by a critical angle of light. However, when the conventional light emitting device is etched to expose an N-type semiconductor layer, side surfaces of the P-type semiconductor layer and the active layer are vertically processed such that a portion of light produced within the light emitting device is totally reflected on the etched surface that is processed vertically from a horizontal plane. Then, a considerable amount of light to be totally reflected is not emitted to the outside but dissipated within the light emitting device due to the internal reflection. That is, there is a problem in that luminous efficiency in which electric energy is converted into light energy and

the light is then emitted to the outside of a light emitting device is low.

SUMMARY OF THE INVENTION

[0011] The present invention is conceived to solve the aforementioned problems. Accordingly, an object of the present invention is to provide a light emitting device for emitting light with high luminous intensity and brightness by enhancing characteristics of luminous efficiency, external quantum efficiency, extraction efficiency and the like and improving reliability, and a method of manufacturing the light emitting device.

[0012] According to an aspect of the present invention for achieving the objects, there is provided a light emitting device, comprising a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on a portion of the N-type semiconductor layer on a substrate. The N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell may be connected to each other, and a side surface including the N-type or P-type semiconductor layer of the light emitting cell has a slope of 20 to 80° from a horizontal plane. The light emitting device may further comprise a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell, a transparent electrode layer on the P-type semiconductor layer, and P-type and N-type ohmic metal layers containing

Cr or Au on the P-type and N-type semiconductor layers, respectively.

[0013] According to another aspect of the present invention, there is provided a light emitting device comprising a substrate formed with a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on the N-type semiconductor layer and a submount substrate flip-chip bonded onto the substrate. Preferably, the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including at least the P-type semiconductor layer of the light emitting cell has a slope of 20 to 80°from a horizontal plane. The light emitting device may further comprise a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

[0014] According to further aspect of the present invention, there is provided a method of manufacturing a light emitting device, comprising the steps of sequentially forming N-type and P-type semiconductor layers on a substrate; forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; and removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern.

[0015] According to still further aspect of the present invention, there is a method of

manufacturing a light emitting device comprising the steps of removing a portion of the N-type semiconductor layer exposed due to the removal of the P-type semiconductor layer to form a plurality of light emitting cells; and connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire.

[0016] According to still further aspect of the present invention, there is a method of manufacturing a light emitting device comprising the step of flip-chip bonding the substrate onto an additional submount substrate after the step of removing the P-type semiconductor layer and the etching mask pattern. The method of manufacturing a light emitting device may further comprise the steps of removing a portion of the N-type semiconductor layer exposed through the removal of the P-type semiconductor layer to form a plurality of light emitting cell; and connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire, after the step of removing the P-type semiconductor layer and the etching mask pattern.

[0017] The step of forming the plurality of light emitting cells may comprise the steps of forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; removing the N-type and P-type semiconductor layers exposed through the etching mask pattern to form a

plurality of light emitting cells; and removing the etching mask pattern.

[0018] The N type semiconductor layer of one light emitting cell and the P type semiconductor layer of another adjacent light emitting cell may be connected with the conductive wire through a bridge or step coverage process.

[0019] A photoresist with a thickness of 3 to 50μm may be used in the step of forming the etching mask pattern. The step of forming the etching mask pattern may comprise the steps of: applying the photoresist onto the P-type semiconductor layer; light exposing the photoresist in accordance with a predetermined mask pattern; and developing the light-exposed photoresist without a baking process after the light exposure. The step of forming the etching mask pattern may comprise the steps of: applying the photoresist onto the P-type semiconductor layer; light exposing the photoresist in accordance with a predetermined mask pattern; hard baking the light-exposed photoresist at a temperature of 100 to 140℃; and developing the hard-baked photoresist.

[0020] After the step of removing the P-type semiconductor layer and the etching mask pattern, the method of manufacturing a light emitting device may further comprise the steps of removing a rear surface of the substrate at a certain thickness; and depositing Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof onto the rear surface of the substrate.

[0021] In a light emitting device and a method of manufacturing the same according to the present invention, light produced from a side surface of a semiconductor layer, which is not

perpendicular to but inclined at a predetermined slop from a horizontal plane, is not totally reflected but emitted to the outside of the light emitting device. Therefore, more enhanced characteristics of light extraction efficiency, external quantum efficiency, luminous efficiency or the like can be obtained. Further, a light emitting device of the present invention emits light with high luminous intensity and brightness and can be applied to a variety of products in which a superior light characteristic is necessary.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] The above and other objects, features and advantages of the present invention will become apparent from the following description of preferred embodiments given in conjunction with the accompanying drawings, in which:

[0023] Figs. 1 and 2 are sectional views showing conventional light emitting devices, respectively;

[0024] Fig. 3 is a conceptual sectional view illustrating a light emitting device with a horizontal structure according to the present invention;

[0025] Figs. 4 and 5 are sectional views illustrating a process of manufacturing a light emitting device according to a first embodiment of the present invention;

[0026] Figs. 6 to 9 are sectional views illustrating a process of manufacturing a light

emitting device according to a second embodiment of the present invention;

[0027] Figs. 10 to 13 are sectional views illustrating a process of manufacturing a light emitting device according to a third embodiment of the present invention;

[0028] Figs. 14 to 17 are sectional views illustrating a process of manufacturing a light emitting device according to a fourth embodiment of the present invention;

[0029] Fig. 18 is a conceptual sectional view illustrating a light emitting device with a flip chip structure according to the present invention;

[0030] Figs. 19 to 23 are sectional views illustrating a process of manufacturing a light emitting device according to a fifth embodiment of the present invention;

[0031] Figs. 24 to 28 are sectional views illustrating a process of manufacturing a light emitting device according to a sixth embodiment of the present invention;

[0032] Fig. 29 is a sectional view showing a seventh embodiment according to the present invention; and

[0033] Figs. 30 and 31 are conceptual sectional views illustrating a difference between effects of the light emitting devices according to the prior art and the present invention;

[0034] Fig. 32 is a sectional view illustrating a light emitting diode for AC operation according to an eighth embodiment of the present invention; and

[0035] Figs. 33 to 38 are sectional views illustrating a process of manufacturing a light

emitting diode according to the eighth embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0036] Hereinafter, a light emitting device and a manufacturing method thereof according to the present invention will be described in detail with reference to the accompanying drawings. However, the present invention is not limited to the embodiments set forth herein but can be implemented in different forms. Rather, the preferred embodiments are merely provided to allow the present invention to be completely described herein and to fully convey the scope of the invention to those skilled in the art.

[0037] Fig. 3 is a conceptual sectional view illustrating a light emitting device with a horizontal structure according to the present invention.

[0038] Referring to Fig. 3, the light emitting device comprises a substrate 10, and an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40, which are sequentially formed on the substrate 10. Each of side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 has a slope of 80 to 20° from a horizontal plane such that a critical angle of light can be changed by such surfaces and light can be easily extracted. Therefore, luminous efficiency of a light emitting device can be improved.

[0039] Figs. 4 and 5 are sectional views illustrating a process of manufacturing a light emitting device according to a first embodiment of the present invention.

[0040] Referring to Fig. 4, an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40 are sequentially formed on a substrate 10.

[0041] The substrate 10 refers to a general wafer used for fabricating a light emitting device and is made of at least any one of Al_2O_3, SiC, ZnO, Si, GaAs, GaP, $LiAl_2O_3$, BN, AlN and GaN. In this embodiment, a crystal growth substrate made of sapphire is used.

[0042] A buffer layer (not shown) may be further formed on the substrate 10 to reduce lattice mismatch between the substrate 10 and the subsequent layers upon growth of crystals. The buffer layer may contain GaN or AlN that is a semiconductor material.

[0043] The N-type semiconductor layer 20 is a layer in which electrons are produced and is preferably made from GaN doped with N-type impurities. However, the N-type semiconductor layer 20 is not limited thereto but may use a material layer having a variety of semiconductor properties. The N-type semiconductor layer 20 including N-type $Al_xGa_{1-x}N(0\leq x\leq 1)$ is formed in this embodiment. Further, the P-type semiconductor layer 40 is a layer in which holes are produced and is preferably made from GaN doped with P-type impurities. However, the P-type semiconductor layer 40 is not limited thereto but may use a material layer with a variety of semiconductor properties. The P-type semiconductor layer 40 including P-type

$Al_xGa_{1-x}N(0\leq x\leq 1)$ is formed in this embodiment. Moreover, InGaN may be used as the semiconductor layer. Further, each of the N-type and P-type semiconductor layers 20 and 40 may be formed as a multiple layer.

[0044] The active layer 30 has a predetermined bandgap and is a region where a quantum well is formed so that electrons and holes are recombined. The active layer 30 may contain InGaN. The wavelength of light emitted through the combination of electrons and holes varies according to the kind of a material constituting the active layer 30. Therefore, it is preferred that a semiconductor material contained in the active layer 30 be controlled depending on a target wavelength.

[0045] The aforementioned material layers are formed through a variety of deposition and growth methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like.

[0046] Thereafter, portions of the P-type semiconductor layer 40 and the active layer 30 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 20. An etching mask pattern is formed on the P-type semiconductor layer 40, and the P-type semiconductor layer 40 and the active layer 30 are then removed through a dry or wet etching process to expose the N-type semiconductor layer 20.

[0047] Generally, in order to perform the etching process, a photoresist has been applied onto a top surface of the P-type semiconductor layer 40 at a thickness of 1 to 2μm, and then soft-baked at a temperature of 80 to 90°C is performed. Next, an exposure process in which light in a UV range is irradiated through a predetermined photo mask to transfer a pattern formed on the mask to the applied photoresist is executed. Thereafter, the photoresist is hard-baked at a temperature of 100 to 120°C, and a developing process in which the photoresist at a portion with relatively weak combination through the exposure process is melted using a solvent is executed. A predetermined etching mask pattern is formed on the P-type semiconductor layer 40 through the above process.

[0048] However, in this embodiment, the photoresist is applied at a thickness of 3 to 50μm which is thicker as compared with the prior art when the etching mask pattern is formed, and the exposure process is performed after the soft-baking. Next, if the photoresist is directly developed without the hard-baking, a developed side surface of the remaining photoresist is formed into an inclined surface not perpendicular (90°) to but inclined at a predetermined slope from a horizontal plane. Subsequently, if exposed regions of the P-type semiconductor layer 40, the active layer 30 and the predetermined N-type semiconductor layer 20 are etched using the etching mask pattern with such a slope of the side surface, the side surfaces of the etched P-type semiconductor layer 40, active layer 30 and N-type semiconductor layer 20 can be similarly

formed into an inclined surface not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane.

[0049] That is, after the photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 40 of Fig. 4 and light-exposed, a developed etching mask pattern is immediately formed without the hard-baking. The P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer 20. A portion of the exposed N-type semiconductor layer 20 may be further removed. Thereafter, if the etching mask pattern is removed, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured as shown in Fig. 5.

[0050] Alternatively, after a photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 40 of Fig. 4 and light-exposed, hard-baking may be performed. In such a case, if the photoresist is hard-baked at a temperature of 100 to 140°C and then developed, the side surface of the developed photoresist may be etched to have a slope of 80 to 20° from a horizontal plane. For example, in a case where the hard-baking is performed at a temperature of 100°C, an etching mask pattern with a slope of about 80° from the horizontal

plane can be obtained, and the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 can have a slope of about 80° from the horizontal plane using the etching mask pattern. Further, in a case where the hard-baking is performed at a temperature of 140°C, an etching mask pattern with a slope of about 20° from the horizontal plane can be obtained, and the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 can have a slope of about 20° from the horizontal plane using the etching mask pattern.

[0051] The etching mask pattern, which the photoresist with a thickness of 3 to 50μm has been light-exposed and hard-baked at a temperature of 100 to 140°C and then developed in such a manner, can be used such that the side surfaces of the etched the P-type semiconductor layer 40, active layer 30 and predetermined N-type semiconductor layer 20 have a slope of 80 to 20° from a horizontal plane similarly to the etching mask pattern. Then, light produced within a light emitting layer is not totally reflected on the etched side surface with a variety of slopes but emitted to the outside of a light emitting device.

[0052] A transparent electrode layer may be further formed on the P-type semiconductor layer 40 to reduce resistance of the P-type semiconductor layer 40 and enhancing transmittance of light, and an additional ohmic metal layer may be further formed on the P-type semiconductor layer 40 or the exposed N-type semiconductor layer 20 to facilitate current supply. The

transparent electrode layer may be made of ITO (Indium Tin Oxide), ZnO or a transparent conductive metal, and the ohmic metal layer may be made of Cr or Au. Further, for the application of voltage, a P-type electrode may be further formed on the P-type semiconductor layer 40 and an N-type electrode may be further formed on the N-type semiconductor layer 20.

[0053] Further, in order to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10.

[0054] As can be seen from this figure, a plurality of light emitting devices may be fabricated on a single substrate 10, which is cut into the individual light emitting devices. At this time, portions A shown in Fig. 5 are cutting portions used for individually cutting the plurality of light emitting devices.

[0055] Accordingly, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 is not perpendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured.

[0056] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto. Various

processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes.

[0057] Figs. 6 to 7 are sectional views illustrating a process of manufacturing a light emitting device according to a second embodiment of the present invention.

[0058] The second embodiment of the present invention is almost the same as the first embodiment. In the second embodiment, however, there is provided a light emitting device in which a plurality of light emitting cells are connected in series, parallel or series-parallel in a wafer level to reduce the size of the device, and they can be driven at proper voltage and current to be used for illustration purpose and can also be driven even with an AC power source. Descriptions overlapping with the previous embodiment will be omitted herein.

[0059] Referring to Fig. 6, an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40 are sequentially formed on a substrate 10 through various deposition methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like. A buffer layer may be further formed on the substrate 10 to reduce lattice mismatch between the substrate 10 and the subsequent layers upon growth of crystals.

[0060] Thereafter, portions of the P-type semiconductor layer 40 and the active layer 30

are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 20. That is, after the photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 40 of Fig. 6 and light-exposed, it is developed without hard-baking to form an etching mask pattern. The P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer 20. A portion of the exposed N-type semiconductor layer 20 may be further removed. Thereafter, if the etching mask pattern is removed, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured as shown in Fig. 7.

[0061] Alternatively, after a photoresist has been applied in a thickness of 3 to 50μm on the P-type semiconductor layer 40 of Fig. 6 and light-exposed, it is hard-baked at a temperature of 100 to 140° and developed such that an etching mask pattern can be formed. After the P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, have been etched, the etching mask pattern is removed such that the side surfaces of the etched P-type semiconductor layer 40 and active layer 30 can have a variety of slopes of 80 to 20°.

[0062] Next, in order to form a plurality of light emitting cells on the substrate 10, predetermined regions of the exposed N-type semiconductor layer 20 are removed such that a portion of the substrate 10 can be exposed. To this end, a predetermined mask pattern is formed on all the portions except the predetermined regions where the substrate 10 will be exposed, and regions of the N-type semiconductor layer 20 that are exposed through the mask pattern are then etched such that the plurality of light emitting cells can be electrically isolated from one another as shown in Fig. 8. At this time, the mask pattern whose side surface is inclined through the aforementioned process is formed and then used to etch the exposed N-type semiconductor layer 20 such that the side surface of the N-type semiconductor layer 20 in which the plurality of light emitting cells are separated from one another is not perpendicular to but inclined at a predetermined slope from a horizontal plane.

[0063] Referring to Fig. 9, the N-type semiconductor layer 20 of a light emitting cell and the P-type semiconductor layer 40 of the adjacent light emitting cell are connected through a predetermined wiring process. That is, the exposed N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent light emitting cell are connected through a wire 60. At this time, the conductive wire 60 for electrically connecting the N-type and P-type semiconductor layers 20 and 40 are formed through a bridge process.

[0064] The aforementioned bridge process is also called an air-bridge process. In the air-

bridge process, a photosensitive liquid is applied between chips to be connected with each other through a photo process and developed to form a photoresist pattern, a material such as metal is first formed into a thin film on the photoresist pattern through a vacuum vapor deposition method or the like, and a conductive material containing gold (Au) is applied at a predetermined thickness onto the thin film through an electroplating, electroless plating or metal vapor deposition method. Thereafter, if the photoresist pattern is removed with a solution of a solvent or the like, a lower portion of the conductive material is completely removed, and thus, only the bridge-shaped conductive material is formed in a space between the adjacent light emitting cells.

[0065] The wire 60 may be made of not only metal but also all kinds of conductive materials. It will be apparent that a silicone compound doped with impurities may be used.

[0066] Further, in order to apply an external voltage to the light emitting device, a P-type bonding pad 50 is formed on the P-type semiconductor layer 40 of the light emitting cell positioned at one edge of the substrate 10 and an N-type bonding pad 55 is formed on the exposed N-type semiconductor layer 20 of the light emitting cell positioned at the other edge of the substrate 10.

[0067] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment but is not limited thereto. Various modifications can be made or various material films can be further added. For example, in order

to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10.

[0068] Accordingly, a light emitting device in which the plurality of light emitting cells each of which side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at predetermined slope from a horizontal plane are connected with one another can be manufactured.

[0069] Figs. 10 to 13 are sectional views illustrating a process of manufacturing a light emitting device according to a third embodiment of the present invention.

[0070] The third embodiment is almost the same as the second embodiment. In the second embodiment, the N-type semiconductor layer 20 is first exposed and a portion of the exposed N-type semiconductor layer 20 is then removed to separate the light emitting cells from one another. In the third embodiment, however, a plurality of light emitting cells are first separated, and a portion of an N-type semiconductor layer 20 is then exposed. Descriptions overlapping with the previous embodiments will be omitted herein.

[0071] Referring to Fig. 10, portions of an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40, which are sequentially formed on a substrate 10, are

removed to form a plurality of light emitting cells. To this end, after a photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 40 and light-exposed, it is immediately developed without hard-baking such that an etching mask pattern can be formed. The portions of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor pattern 20, which are exposed through the etching mask pattern, and the etching mask pattern is removed to separate the light emitting cells from one another. Accordingly, a light emitting device in which entire side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at a predetermined slope can be obtained as shown in this figure. Further, the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are removed using the etching mask pattern in which a photoresist is applied at a thickness of 3 to 50μm on the P-type semiconductor layer 40 and light-exposed and hard-baked at a temperature of 100 to 140° and then developed. Accordingly, the entire side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 can be formed at various slopes of 80 to 20°.

[0072] Thereafter, as shown in Fig. 11, portions of the P-type semiconductor layer 40 and the active layer 30 are removed to expose a portion of the N-type semiconductor layer 20 through a predetermined etching process.

[0073] Referring to Fig. 12, the N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent light emitting cell are connected with each other through a bridge process.

[0074] Further, in order to apply an external voltage to the light emitting device, a P-type bonding pad 50 is formed on the P-type semiconductor layer 40 of the light emitting cell positioned at one edge of the substrate 10 and an N-type bonding pad 55 is formed on the exposed N-type semiconductor layer 20 of the light emitting cell positioned at the other edge of the substrate 10.

[0075] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment but is not limited thereto. Various modifications can be made and various material films may be further added. For example, in order to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10.

[0076] Further, even in a case where the plurality of light emitting cells are separated by etching such that the side surfaces may have various slopes as shown in Fig. 10 and then etched to expose the N-type semiconductor layer 20, a light emitting device can be manufactured using the same etching process as described above. That is, as shown in Fig. 11, the side surfaces of the

P-type semiconductor layer 40 and the active layer 30, which are etched to expose the N-type semiconductor layer 20, can be formed at various slopes.

[0077] Accordingly, a light emitting device in which the plurality of light emitting cells each of which side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at predetermined slope from a horizontal plane are connected with one another can be manufactured.

[0078] Figs. 14 to 17 are sectional views illustrating a process of manufacturing a light emitting device according to a fourth embodiment of the present invention.

[0079] The fourth embodiment is almost the same as the third embodiment. In the third embodiment, a conductive wire for electrically connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell is formed through a bridge process. In the fourth embodiment, however, the conductive wire is formed through a step coverage process. Descriptions overlapping with the previous embodiments will be omitted herein.

[0080] Referring to Fig. 14, even in a case where a plurality of light emitting cells are separated by etching such that the side surfaces may have various slopes and then etched to expose an N-type semiconductor layer 20 through the aforementioned process, the side surfaces of P-type semiconductor layer 40 and active layer 30, which are etched to expose the N-type

semiconductor layer 20, are formed with various slopes. Further, in order to reduce the resistance of the P-type semiconductor layer 40 and enhance the transmittance of light, a transparent electrode layer 85 may be further formed on a top surface of the P-type semiconductor layer 40. Further, an additional ohmic metal layer 87 for facilitating the supply of current may be further formed on a top surface of the P-type semiconductor layer 40 or the exposed N-type semiconductor layer 20. The transparent electrode layer 85 may be made of ITO (Indium Tin Oxide), ZnO or a conductive transparent metal, and the ohmic metal layer 87 may be made of Cr or Au.

[0081] Referring to Fig. 15, a continuous insulation layer 70 is formed on an entire surface of the substrate 10 with the plurality of light emitting cells formed thereon. The insulation layer 70 covers the side surfaces and top surfaces of the light emitting cells and the top surfaces of the substrate 10 between the adjacent light emitting cells. For example, the insulation layer 70 may be formed as a silicone oxide film using a CVD (Chemical Vapor Deposition) technique.

[0082] Since the side surfaces of the light emitting cells are inclined, the insulation layer 70 can easily cover the side surfaces of the light emitting cells. Since the total thickness of the N-type semiconductor layer 20 and active layer 30 is small and spaces between the adjacent P-type semiconductor layers 40 are broad, the side surfaces of the P-type semiconductor layers 40

adjacent to the exposed regions of the N-type semiconductor layers 20 can be easily covered with the insulation layer 70.

[0083] Referring to Fig. 16, an opening portion is formed on each of the exposed N-type and P-type semiconductor layers 20 and 40 of the light emitting cell by patterning the insulation layer 70 through a predetermined etching process. If the transparent electrode layer 85 and/or the ohmic metal layer 87 are formed as shown in this figure, the transparent electrode layer 85 and/or the ohmic metal layer 87 are exposed through the opening portion.

[0084] Referring to Fig. 17, a wire 80 is formed on the insulation layer 70 with the opening portion. The wire 80 connects the N-type and P-type semiconductor layers 20 and 40 through the opening portion thereof. That is, the N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent the light emitting cell are electrically connected with the wire.

[0085] The wire 80 may be formed using a plating technique. That is, after an etching mask pattern with an opening portion defining a region of the wire 80 has been formed on the insulation layer 70 and a metal layer has been plated within the opening portion, the etching mask pattern is removed and thus the wire 80 can be formed.

[0086] Further, the wire 80 may be formed using the CVD (Chemical Vapor Deposition) or PVD (Physical Vapor Deposition) technique. That is, a metal layer is formed using a vapor

deposition technique such as electron beam deposition and then patterned using a photo and etching process, so that the wire 80 can be formed. Since the side surface of the light emitting cell is inclined, the metal layer is continuously formed on the upper side surface of the light emitting cell.

[0087] The light emitting device in which the wire 80 is formed as described above has an advantage in that it is possible to prevent the wire 80 from being disconnected or shorted due to external pressure and also prevent conductive materials such as metal, which remains while the wire 80 is formed, from shorting the light emitting cell.

[0088] Accordingly, a light emitting device in which the plurality of light emitting cells each of which side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at predetermined slope from a horizontal plane are connected with one another can be manufactured.

[0089] As described above, the light emitting device according to the present invention is formed such that the side surfaces of the P-type semiconductor layer, the active layer and a portion of the N-type semiconductor layer are not perpendicular (90°) to but inclined at a predetermined slope from a horizontal plane. Therefore, luminous efficiency of the light emitting device of the present invention can be enhanced as compared with that of the conventional light emitting device. The reason is that a photon reflected on a flat surface in the prior art is not

reflected on a surface with a different angle but emitted to the outside.

[0090] Fig. 18 is a conceptual sectional view illustrating a light emitting device with a flip chip structure according to the present invention.

[0091] Referring to Fig. 18, the light emitting device comprises a light emitting layer, i.e. an N-type semiconductor layer 120, an active layer 130 and a P-type semiconductor layer 140 sequentially formed on a base substrate 110. Further, the light emitting device comprises a submount substrate 200 onto which the base substrate 110 with the light emitting layer formed thereon is flip-chip bonded through metal bumps 150 and 155. A side surface of the light emitting layer comprising the P-type semiconductor layer 140, the active layer 130 and the N-type semiconductor layer 120 is inclined at a slope of 20 to 80°from the horizontal plane and a critical angle of light is changed due to the side surface such that the light can be easily extracted. Therefore, luminous efficiency of the light emitting device can be improved.

[0092] Figs. 19 to 23 are sectional views illustrating a process of manufacturing a light emitting device according to a fifth embodiment of the present invention.

[0093] Referring to Fig. 19, an N-type semiconductor layer 120, an active layer 130 and a P-type semiconductor layer 140 are sequentially formed on a base substrate 110.

[0094] The base substrate 110 refers to a general wafer used for fabricating a light emitting device is made of a transparent substrate such as Al_2O_3, ZnO and $LiAl_2O_3$. In this

embodiment, a crystal growth substrate made of sapphire is used.

[0095] The N-type semiconductor layer 120, the active layer 130 and the P-type semiconductor layer 140 are sequentially formed on the substrate 110 through various deposition methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like. A buffer layer may be further formed on the substrate 110 to reduce lattice mismatch between the substrate 110 and the subsequent layers upon growth of crystals. The aforementioned components are the same as those in the previous embodiments, and thus, descriptions overlapping with the foregoing components will be omitted herein.

[0096] Thereafter, portions of the P-type semiconductor layer 140 and the active layer 130 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 120. This etching process is the same as that of the previous embodiments.

[0097] That is, after a photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 140 of Fig. 19 and light-exposed, it is immediately developed without hard-baking to form an etching mask pattern. The P-type semiconductor 140 and the active layer 130, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer

120. Thereafter, if the etching mask pattern is removed, side surfaces of the P-type semiconductor layer 140 and the active layer 130 which are not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane can be obtained as shown in Fig. 20.

[0098] Alternatively, after a photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 140 of Fig. 19 and light-exposed, it is hard-baked at a temperature of 100 to 140°C and then developed such that an etching mask pattern can be formed. After the P-type semiconductor layer 140 and the active layer 130, which are exposed through the etching mask pattern, have been etched, the etching mask pattern is removed such that the side surfaces of the etched P-type semiconductor layer 140 and active layer 130 can have a variety of slopes of 80 to 20°.

[0099] A reflection layer for reflecting light may be further formed on a top surface of the P-type semiconductor layer 140, and an additional ohmic metal layer for facilitating the supply of current may be further formed on a top surface of the P-type semiconductor layer 140 or the exposed N-type semiconductor layer 120. The ohmic metal layer may be made of Cr or Au.

[0100] Further, P-type and N-type metal bumps 155 and 150 are formed on the P-type and N-type semiconductor layers 140 and 120, respectively, as shown in Fig. 21. Each of the P-type and N-type metal bumps 155 and 150 may be made of at least one material selected from

the group consisting of Pb, Sn, Au, Ge, Cu, Bi, Cd, Zn, Ag, Ni, Ti and an alloy thereof. To this end, a photoresist is applied onto an entire structure and a photoresist pattern (not shown) through which portions of the P-type and N-type semiconductor layers 140 and 120 are exposed is formed through a photo-etching process using a predetermined mask. After a metal film has been deposited on the entire structure, metal film portions formed on regions other than regions on the P-type and N-type semiconductor layers 140 exposed through the photoresist pattern and the photoresist pattern are removed. Accordingly, the P-type and N-type metal bumps 155 and 150 are formed on the P-type and N-type semiconductor layers 140 and 120, respectively.

[0101] Next, referring to Fig. 22, an additional submount substrate 200 is prepared to form P-type and N-type bonding pads 215 and 210 connected to the P-type and N-type metal bumps 155 and 150, respectively.

[0102] At this time, various kinds of superior heat conductive substrates 200 are used as the submount substrate 200. That is, the submount substrate 200 may be made of SiC, Si, Ge, SiGe, AlN, metal or the like. In this embodiment, AlN with superior heat conductivity and insulation property is used. The present invention is not limited thereto, but a metallic material with superior heat and electric conductivity may be employed. In this case, an insulation or dielectric film is formed on the substrate 200 to sufficiently serve as an insulation. The dielectric film may be made of SiO2, MgO and SiN or an insulating material. Further, each of the P-type

and N-type bonding pads 210 and 215 is made of a metal with superior electric conductivity. This is formed through a screen printing process or a deposition process using a predetermined mask pattern.

[0103] Thereafter, the submount substrate 200 is flip-chip bonded onto the base substrate 110 with the light emitting layer formed thereon.

[0104] Referring to Fig. 23, in the light emitting device of the present invention, the N-type and P-type metal bumps 150 and 155 formed on the top of the light emitting layer are bonded and connected with the N-type and P-type bonding pads 210 and 215 of the submount substrate 200, respectively. At this time, the bonding pads and metal bumps may be bonded using heat or ultrasonic waves or simultaneously using the heat and ultrasonic waves. The metal bumps 150 and 155 and the lower bonding pads 210 and 215 are connected through a variety of bonding methods.

[0105] Moreover, the N-type and P-type metal bumps 150 and 155 are not formed on the top of the light emitting layer but may be formed on the submount substrate 200.

[0106] As can be seen from this figure, a plurality of light emitting devices may be fabricated on a single substrate 10, which is cut into the individual light emitting devices. At this time, portions A shown in Fig. 23 are cutting portions used for individually cutting the plurality of light emitting devices.

[0107] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto. Various processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes. For example, in the same process as the previous embodiments, the base substrate with the N-type semiconductor layer, the active layer and the P-type semiconductor layer sequentially formed thereon is prepared as shown in Fig. 19. Then, portions of the P-type semiconductor layer, the active layer and the N-type semiconductor layer are first removed to expose the substrate such that the plurality of light emitting devices can be individually isolated. At this time, the side surfaces of the P-type semiconductor layer, the active layer and the N-type semiconductor layer, which are etched through the aforementioned process, may be formed not to be perpendicular (90°) to but inclined at a predetermined slope.

[0108] Accordingly, a light emitting device with a flip chip structure, in which the side surfaces of the P-type semiconductor layer, the active layer and a portion of the N-type semiconductor layer are not perpendicular (90°) to but inclined at the predetermined slope from the horizontal plane, can be manufactured.

[0109] Figs. 24 to 28 are sectional views illustrating a process of manufacturing a light emitting device according to a sixth embodiment of the present invention.

[0110] The sixth embodiment is almost the same as the fifth embodiment. In the sixth embodiment, however, there is provided a light emitting device with a flip chip structure, in which a plurality of light emitting cells are connected in series, parallel or series-parallel in a wafer level to reduce the size of the device, and they can be driven at proper voltage and current to be used for illumination purpose and can also be driven even with an AC power source. Descriptions overlapping with the previous embodiments will be omitted herein.

[0111] Referring to Fig. 24, an N-type semiconductor layer 120, an active layer 130 and a P-type semiconductor layer 140 are sequentially formed on a base substrate 110 through various deposition methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like. A buffer layer may be further formed on the substrate 110 to reduce lattice mismatch between the substrate 110 and the subsequent layers upon growth of crystals.

[0112] Thereafter, portions of the N-type semiconductor layer 120, the active layer 130 and the P-type semiconductor layer 140, which are sequentially formed on the base substrate 110, are removed to form a plurality of light emitting cells. To this end, after a photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 140 of Fig. 24 and light-exposed, it is immediately developed without hard-baking to form an etching mask pattern.

The P-type semiconductor 140, the active layer 130 and the predetermined N-type semiconductor layer 120, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to separate the light emitting cells from one another. Next, if the etching mask pattern is removed, a light emitting device in which entire side surfaces of the etched P-type semiconductor layer 140, active layer 130 and N-type semiconductor layer 120 are not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane can be obtained as shown in Fig. 25.

[0113] Alternatively, after a photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 140 of Fig. 24 and light-exposed, it is hard-baked at a temperature of 100 to 140°C and developed such that an etching mask pattern can be formed. After the P-type semiconductor layer 140, the active layer 130 and the N-type semiconductor layer 120, which are exposed through the etching mask pattern, have been etched, the etching mask pattern is removed such that the side surfaces of the etched P-type semiconductor layer 140 and active layer 130 can be inclined at various slopes of 80 to 20°.

[0114] Next, portions of the P-type semiconductor layer 140 and the active layer 130 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 120, as shown in Fig. 26. The exposed N-type semiconductor layer 120 of one light emitting cell and the P-type semiconductor layer 140 of another adjacent light emitting

cell are connected with each other through a predetermined conductive wire. At this time, a bridge wire 160 is made of a conductive material, e.g. metal. It will be apparent that the bridge wire 160 may be made of a silicone compound doped with impurities. The bridge wire 160 is formed through a bridge process.

[0115] Further, a plurality of metal bumps are formed on the top of the light emitting cells, and P-type and N-type metal bumps 155 and 150 are further formed on the P-type semiconductor layer 140 of the light emitting cell positioned at one edge of the substrate 110 and the N-type semiconductor layer 120 of the light emitting cell positioned the other edge of the substrate, respectively.

[0116] Next, as shown in Fig. 27, an additional submount substrate 200 is prepared, on which a plurality of bonding layers 220, a P-type bonding pad 215 positioned at one edge of the submount substrate 200 and an N-type bonding pad 210 positioned at the other edge of the submount substrate are formed.

[0117] Thereafter, as can be shown in Fig. 28, the aforementioned base substrate 110 with the plurality of light emitting cells formed thereon is flip-chip bonded onto the submount substrate 200 to fabricate the light emitting device. The substrates are bonded with each other through the metal bumps 150 and 155 formed on the top of the light emitting cell and the bonding layers 220 formed on the submount substrate 200, respectively. The P-type bonding pad

215 positioned at one edge of the submount substrate 200 is connected to the P-type metal bump 155 of the light emitting cell positioned at one edge of the base substrate 110, whereas the N-type bonding pad 210 positioned at the other edge of the submount substrate 200 is connected to the N-type metal bump 150 of the light emitting cell positioned at the other edge of the base substrate 110.

[0118] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto. Various processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes. For example, in this embodiment, the conductive wire for electrically connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell is formed through a bridge process, and the base substrate is then flip-chip bonded onto the submount substrate. However, the present invention is not limited thereto. That is, a conductive wire for electrically connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cells may be formed through a step coverage process which is the same as in the fourth embodiment. Further, an electrode layer may be formed on the submount substrate when the plurality of light emitting cells are flip-chip bonded onto the submount substrate such that the N-type semiconductor layer of one light

emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are electrically connected through the metal bumps.

[0119] Accordingly, a light emitting device in which a plurality of flip chip light emitting cells each having a side surface of a light emitting layer, which is not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane, are arrayed on the submount substrate can be manufactured. The light emitting cells may be connected in various ways, i.e. in series, parallel or series-parallel, depending on the desired purpose.

[0120] Fig. 29 is a sectional view showing a seventh embodiment according to the present invention.

[0121] The seventh embodiment is almost the same as the sixth embodiment. In this embodiment, even in a case where a plurality of light emitting cells are separated by etching such that the side surfaces may have slopes as shown in Fig. 25 and then etched to expose an N-type semiconductor layer, a light emitting device can be manufactured using the same etching process as the previous embodiment. That is, side surfaces of a P-type semiconductor layer 140 and an active layer 130 etched to expose an N-type semiconductor layer 120 are formed with various slopes, as shown in Fig. 29.

[0122] Accordingly, a light emitting device in which a plurality of flip chip light emitting cells each having an entire side surface of a light emitting layer, which is not perpendicular (90°)

to but inclined at a predetermined slope from the horizontal plane, are arrayed on the submount substrate can be manufactured. The light emitting cells may be connected in various ways, i.e. in series, parallel or series-parallel, depending on the desired purpose.

[0123] As described above, the light emitting device with a flip chip structure according to the present invention is formed such that some side surfaces of a light emitting layer are not particular (90°) to but inclined at a predetermined slope from the horizontal plane. Therefore, luminous efficiency of the light emitting device of the present invention can be enhanced as compared with that of the conventional light emitting device. The reason is that a photon reflected on a flat surface in the prior art is not reflected on a surface with a different angle but emitted to the outside.

[0124] Figs. 30 and 31 are conceptual sectional views illustrating a difference between effects of the light emitting devices according to the prior art and the present invention.

[0125] The light efficiency of a light emitting device may be expressed as internal quantum efficiency and external quantum efficiency, and the internal quantum efficiency is determined in accordance with the design and quality of an active layer. The external quantum efficiency is determined in accordance with a degree where a photon produced in an active layer is emitted to the outside of a light emitting device. Referring to Fig. 30 in which a conventional light emitting device is shown, a side surface of a semiconductor layer is formed perpendicular to

a horizontal plane. In such a case, some portions of photons are not penetrated through the side surface of the semiconductor layer but reflected thereon, and totally reflected light is not emitted to the outside but dissipated within the light emitting device. However, referring to Fig. 31 in which a light emitting device according to the present invention is shown, a side surface of a semiconductor layer is not perpendicular to but inclined at a predetermined slope from a horizontal plane. In such a case, the inclined side surface makes a critical angle of light change to help the light to be more easily extracted. Therefore, light generated in an active layer is not totally reflected but emitted to the outside of the light emitting device such that external quantum efficiency can be markedly enhanced.

[0126] Fig. 32 is a sectional view illustrating a light emitting diode for AC operation according to the eighth embodiment of the present invention.

[0127] Referring to Fig. 32, a plurality of light emitting cells 56 are disposed to be spaced apart in a substrate 51. The substrate 51 may be insulating or conducting one, and may be, for example, a sapphire or a silicon carbide (SiC) substrate.

[0128] The light emitting cells 56 respectively include a lower semiconductor layer 55, an upper semiconductor layer 59 disposed in a region of the lower semiconductor layer, and an active layer 57 disposed between the lower semiconductor layer and the upper semiconductor layer. The upper and the lower semiconductor layers may be N-type and P-type, respectively.

Alternatively the upper and the lower semiconductor layers may be P-type and N-type, respectively.

[0129] The lower semiconductor layer 55, active layer 57 and upper semiconductor layer 59 may include a gallium nitride-based semiconducting material, for example, (B, Al, In, Ga)N. Elements and stoichiometry of the active layer 57 may be determined so that a light having a desired wavelength, for example, ultraviolet ray or blue light, can be emitted. The lower semiconductor layer 55 and upper semiconductor layer 59 are formed of a material having a greater bandgap compared with the active layer 57.

[0130] The lower semiconductor layer 55 and/or the upper semiconductor layer 59 may be, as illustrated, formed of a single layer or multiple layers. The active layer 57 may have a single-quantum-well structure or a multiple-quantum-well structure.

[0131] A buffer layer 53 may be disposed between the light emitting cells 56 and the substrate 51. The buffer layer 53 is employed to reduce a lattice mismatch between the substrate 51 and the lower semiconductor layer 55 formed thereon. The buffer layer 53 may be continuous as illustrated, but it is not limited thereto. The buffer layer 53 may be disposed under the lower semiconductor layers 55 to be discontinuous.

[0132] Side surfaces of the light emitting cells 56 are formed to be inclined with respect to an upper surface of the substrate 51 and get narrowed toward upside. The inclination of the

side surfaces improves emission efficiency of a light produced in the active layer 57, and helps conformal deposition of other layers which will be formed on the light emitting cells 56. In the exemplary embodiment, the inclinations of the side surfaces of the respective lower semiconductor layers 55 of the light emitting cells 56 may be in a range of approximately 15 degrees to approximately 80 degrees.

[0133] An insulation layer 69 covers an entire surface of the light emitting cells 56. The insulation layer 69 include opening portions on other regions of the lower semiconductor layers 55, for example, a region adjacent to a region on which the upper semiconductor layer 59 is formed, and include opening portions on the upper semiconductor layers 59. The opening portions are space apart from each other, and therefore, the side surfaces of the light emitting cells 56 are covered with the insulation layer 69. The insulation layer 69 may cover the substrate 51 in regions between the light emitting cells 56, or the buffer layer 53. The insulation layer 69 may include a silicon oxide (SiO2) layer.

[0134] Wires 71 are formed on the insulation layer 69. The wires 71 are electrically connected to the lower semiconductor layers 55 and the upper semiconductor layers 59 through the opening portions. In addition, the wires 71 respectively connect the lower semiconductor layers 55 and the upper semiconductor layers 59 of the adjacent light emitting cells 56 to form a series array of the light emitting cells 56. The array may be formed in plurality, and a plurality of

arrays may be connected to be reverse parallel and connected to AC power to be driven. Further, a bridge rectifier (not shown) connected to the series array of the light emitting cells may be formed, and the light emitting cells may be driven with AC power by the bridge rectifier. The bridge rectifier may be formed by connecting light emitting cells having substantially the same structure as the light emitting cells using wires 71. The wires may be formed of a conductive material, for example, a doped semiconducting material such as polycrystalline silicon or a metal.

[0135] Meanwhile, electrode pads may be disposed between other regions of the lower semiconductors 55 and the insulation layer 69. The electrode pads 67 are exposed by the opening portions formed in other regions of the lower semiconductor layers 55. The electrode pads 67 have ohmic contacts to the lower semiconductor layers 55. The wires 71 are in contact with the electrode pads 67 exposed by the opening portions to be electrically connected to the lower semiconductor layers 55.

[0136] Transparent electrode layers 65 may be disposed between the upper semiconductor layers 59 and the insulation layers 69. The transparent electrode layers 65 are exposed by the opening portions formed on the upper semiconductor layers 59. The transparent electrode layers 65 transmit light produced in the active layer 57, and disperse and supply currents to the upper semiconductor layers 59. The wires 71 are in contact with the transparent

electrode layers 65 exposed by the opening portions to be electrically connected to the upper semiconductor layers 55. Electrode pads (not shown) may be further formed on the transparent electrode layers 65 and the wires 71 may be in contact with the electrode pads.

[0137] A protecting insulation layer 73 may cover the wires 71 and the insulation layer 69. The protecting insulation layer 73 substantially reduces contamination of the wires 71 from moisture and so forth, and damage of the wires 71 from external pressure. The protecting insulation layer 73 may be formed of a light-transmitting material, for example, silicon oxide layer.

[0138] Figs. 33 to 38 are sectional views illustrating a process of manufacturing a light emitting diode according to the eighth embodiment of the present invention.

[0139] Referring to Fig. 33, a lower semiconductor layer 55, an active layer 57, and an upper semiconductor layer 59 are formed on a substrate 51. A buffer layer 53 may be formed on the substrate 51 before the lower semiconductor layer 55 is formed.

[0140] The substrate 51 may be sapphire (Al2O3), silicon carbide (SiC), zinc oxide (ZnO), silicon (Si), gallium arsenide (GaAs), gallium phosphate (GaP), lithium-alumina (LiAl2O3), boron nitride (BN), aluminum nitride (AlN) or gallium nitride (GaN). However, it is not limited thereto and may be variable according to a semiconducting material which is to be formed on the substrate 51.

[0141] The buffer layer 53 is formed to reduce lattice mismatch between the substrate 51 and the semiconductor layer 55 which is to be formed thereon. The buffer layer 53 may include, for example, gallium nitride (GaN) or aluminum nitride (AlN). When the substrate 51 is a conductive substrate, the buffer layer 53 may be formed of an insulation layer or a semi-insulation layer, for example, AlN or semi-insulating GaN.

[0142] The lower semiconductor layer 55, active layer 57 and upper semiconductor layer 59 may include a gallium nitride-based semiconducting material, for example, (B, Al, In, Ga)N. The lower and upper semiconductor layers 55 and 59 and the active layer 57 may be formed continuously or discontinuously using, for example, metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy or hydride vapor phase epitaxy (HNPE) technology.

[0143] The upper and the lower semiconductor layers may be N-type and P-type, respectively. Alternatively the upper and the lower semiconductor layers may be P-type and N-type, respectively. In the gallium nitride-based compound semiconductor layer, N-type semiconductor layer may be doped with, for example, silicon (Si), and P-type semiconductor layer may be doped with, for example, magnesium (Mg).

[0144] Photoresist patterns 63 defining light emitting cell regions are formed on the upper semiconductor layer 59. The photoresist patterns are formed to cover the light emitting cell regions. Reflow of the photoresist patterns 63 is performed so that side surfaces can be

inclined with respect to an upper surface of the substrate 51. The side surfaces of the photoresist patterns 63 may be formed to have an inclination angle in a range of approximately 15 degree to 80 degree with respect to the upper surface of the substrate 51.

[0145] Referring to Fig. 34, the upper semiconductor layer 59, the active layer 57 and the lower semiconductor layer 55 are sequentially etched using the photoresist patterns 63 as etching mask. Accordingly, the shape of the photoresist patterns 63 is reproduced in the semiconductor layers 59, 57 and 55 and the light emitting cells with inclined side surfaces are separated. The buffer layer 53 may be exposed and the exposed buffer layer 53 may be removed by over-etching.

[0146] Thereafter, the photoresist patterns 63 are removed, and the upper semiconductor layer and the active layer are patterned again to expose the etched lower semiconductor layers 55. The exposed lower semiconductor layers may be partially etched by over-etching. Accordingly, light emitting cells 56 that are spaced apart are formed on the substrate 51. Each of the light emitting cells 56 includes the lower semiconductor layer 56 which is spaced apart by etching, the upper semiconductor layer 57 disposed on an upper side of a region of the lower semiconductor layer 56, and the active layer 57 disposed between the lower semiconductor layer 55 and the upper semiconductor layer 57. Other region of the lower semiconductor layer 56 is exposed. Further, most of the side surfaces of the light emitting cells 56 are formed to be

inclined with respect to an upper surface of the substrate 51. Whereas, side surfaces of the upper semiconductor layers 59 adjacent to other regions of the lower semiconductor layers 55 may be formed to be inclined as illustrated, and alternatively, may be formed vertically.

[0147] Referring to Fig. 35, a transparent electrode layer 65 may be formed on the upper semiconductor layer 59 of the light emitting cell 56. The transparent electrode layer 65 includes a transparent metal such as indium tin oxide (ITO) layer or Ni/Au. Further, electrode pads 67 may be formed on other regions of the lower semiconductor layers 55. The electrode pads 67 have an ohmic contact with the lower semiconductor layers 55.

[0148] The transparent electrode layer 65 may be formed on the upper semiconductor layer 59 before the photoresist patterns are formed. The transparent electrode layer 65 is patterned together with the upper semiconductor layer

[0149] Referring to Fig. 36, a continuous insulation layer 69 is formed on an entire surface of the substrate 51 with the plurality of light emitting cells 56 formed thereon. The insulation layer 69 covers the side surfaces and top surfaces of the light emitting cells 56, and the top surfaces of the substrate 51 between the adjacent light emitting cells 56. For example, the insulation layer 69 may be formed as a silicone oxide film using a CVD (Chemical Vapor Deposition) technique.

[0150] Since the side surfaces of the light emitting cells 56 are inclined, the insulation

layer 69 can easily cover the side surfaces of the light emitting cells 56. Since the total thickness of the upper semiconductor layer 59 and active layer 57 is small and spaces between the upper semiconductor layers 59 are broad, the side surfaces of the upper semiconductor layers 59 adjacent to other regions of the lower semiconductor layers 55 can be easily covered with the insulation layer 69.

[0151] Referring to Fig. 37, an opening portions are formed on other regions of the lower semiconductor layers 55 and the upper semiconductor layers 59 by patterning the insulation layer 69. If the electrode pads 67 and the transparent electrode layers 65 are formed, the electrode pads 67 and the transparent electrode layers 65 are exposed through the opening portions.

[0152] The opening portions may be formed using a photo and etching process, and the electrode pads 67 substantially reduce damage of the lower semiconductor layers 55 while the insulation layer 69 is etched.

[0153] Referring to Fig. 38, wires 71 are formed on the insulation layer 69 with the opening portions. The wire 71 are electrically connected to the lower semiconductor layers 55 and the upper semiconductor layers 59 through the opening portions, and connect the lower semiconductor layers 55 and the upper semiconductor layers 59 of the adjacent light emitting cells 56 to form arrays connected in series.

[0154] The wires 71 may be formed using a plating technique. That is, the wires 71 may

be formed by forming a photoresist pattern having opening portions defining wire region on the insulation layer 69, plating a metal layer in the opening portions, and removing the photoresist pattern.

[0155] Alternatively, the wires 71 may be formed using CVD (Chemical Vapor Deposition) or PVD (Physical Vapor Deposition) technique. That is, a metal layer is formed using a vapor deposition technique such as electron beam deposition and then patterned using a photo and etching process, so that the wires 71 can be formed. Since the insulation layer 69 covers the side surfaces of the light emitting cells 56, short-circuiting of the light emitting cells 56 due to a remaining metallic material after patterning of metal layer may be prevented.

[0156] A protecting insulation layer 73 is formed on the substrate 51 with the wires 71 formed thereon. The protecting insulation layer 73 is formed of a light-transmitting material, for example, silicon oxide layer using chemical vapor deposition technique. In this way, a light emitting diode for AC operation.

[0157] According to the eighth embodiment, a reliable light emitting diode for AC operation can be provided by preventing disconnection or short circuit of wires by external pressure, and short circuit of a light emitting cell by a conductive material such as metal residue while the wires are formed may be prevented. Further, the wires may be formed to be supported by insulation layers, so that a reliable light emitting diode for AC operation can be manufactured.

[0158] Although the present invention has been described in detail in connection with the specific embodiments, it will be readily understood by those skilled in the art that various modifications and changes can be made thereto within the technical spirit and scope of the present invention. It is also apparent that the modifications and changes fall within the scope of the present invention defined by the appended claims.

WHAT IS CLAIMED IS:

1. A method of manufacturing a light emitting device, comprising the steps of:

sequentially forming N-type and P-type semiconductor layers on a substrate;

forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; and

removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern.

2. The method as claimed in claim 1, further comprising the steps of:

removing a portion of the N-type semiconductor layer exposed through the removal of the P-type semiconductor layer to form a plurality of light emitting cells; and

connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire.

3. The method as claimed in claim 1, further comprising the step of flip-chip bonding the substrate onto an additional submount substrate after the step of removing the P-type

semiconductor layer and the etching mask pattern.

4. The method as claimed in claim 3, further comprising the steps of:

removing a portion of the N-type semiconductor layer exposed due to the removal of the P-type semiconductor layer to form a plurality of light emitting cell; and

connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire, after the step of removing the P-type semiconductor layer and the etching mask pattern.

5. The method as claimed in claim 2, wherein the step of forming the plurality of light emitting cells comprises the steps of:

forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer;

removing the N-type and P-type semiconductor layers exposed through the etching mask pattern to form a plurality of light emitting cells; and

removing the etching mask pattern.

6. The method as claimed in claim 2, wherein the N type semiconductor layer of one

light emitting cell and the P type semiconductor layer of another adjacent light emitting cell are connected with the conductive wire through a bridge or step coverage process.

7. The method as claimed in claim 1, wherein a photoresist with a thickness of 3 to 50μm is used in the step of forming the etching mask pattern.

8. The method as claimed in claim 7, wherein the step of forming the etching mask pattern comprises the steps of:

applying the photoresist onto the P-type semiconductor layer;

light exposing the photoresist in accordance with a predetermined mask pattern; and

developing the light-exposed photoresist without a baking process after the light exposure.

9. The method as claimed in claim 7, wherein the step of forming the etching mask pattern comprises the steps of:

applying the photoresist onto the P-type semiconductor layer;

light exposing the photoresist in accordance with a predetermined mask pattern;

hard baking the light-exposed photoresist at a temperature of 100 to 140¡É; and

developing the hard-baked photoresist.

10. The method as claimed in claim 1, further comprising the steps of:

after the step of removing the P-type semiconductor layer and the etching mask pattern, removing a rear surface of the substrate at a certain thickness; and

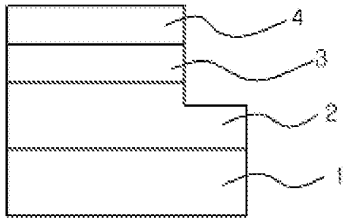
depositing Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof onto the rear surface of the substrate.

ABSTRACT OF THE DISCLOSURE

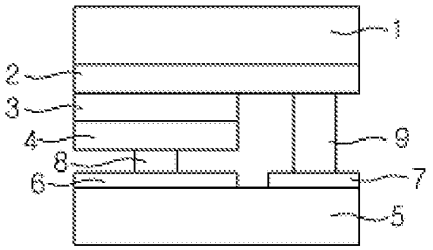
The present invention relates to a light emitting device and a method of manufacturing the light emitting device. According to the present invention, the light emitting device comprises a substrate, an N-type semiconductor layer formed on the substrate, and a P-type semiconductor layer formed on the N-type semiconductor layer, wherein a side surface including the N-type or P-type semiconductor layer has a slope of 20 to 80° from a horizontal plane. Further, the present invention provides a light emitting device comprising a substrate formed with a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on the N-type semiconductor layer, and a submount substrate flip-chip bonded onto the substrate, wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including at least the P-type semiconductor layer of the light emitting cell has a slope of 20 to 80° from a horizontal plane. Further, the present invention provides a method of manufacturing the light emitting device. Accordingly, there is an advantage in that the characteristics of a light emitting device such as luminous efficiency, external quantum efficiency and extraction efficiency are enhanced and the reliability is secured such that light with high luminous intensity and brightness can be emitted.

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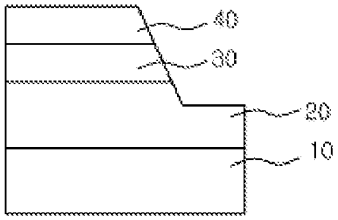
[Figure 1]



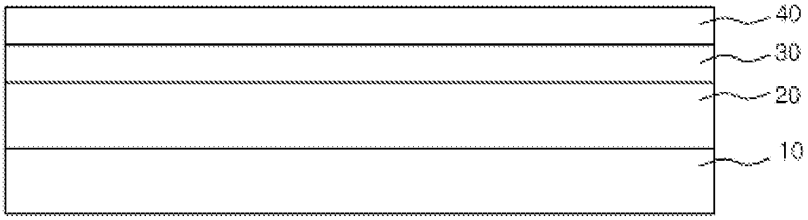
[Figure 2]



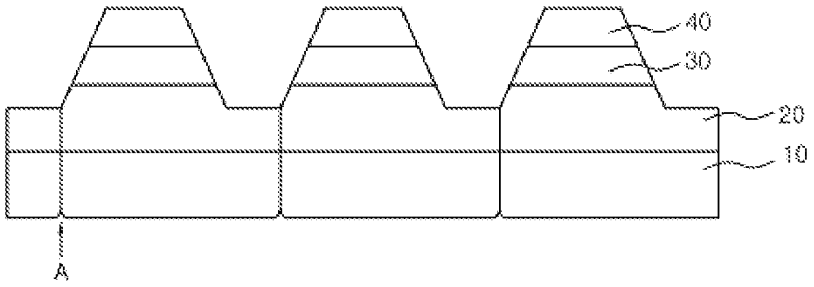
[Figure 3]



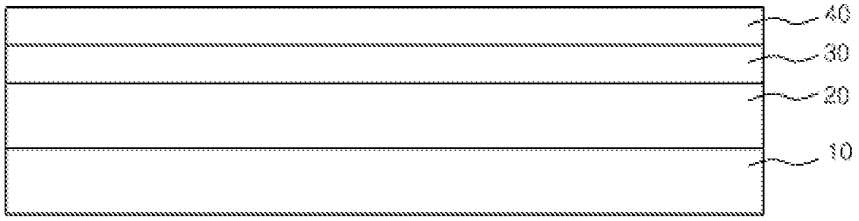
[Figure 4]



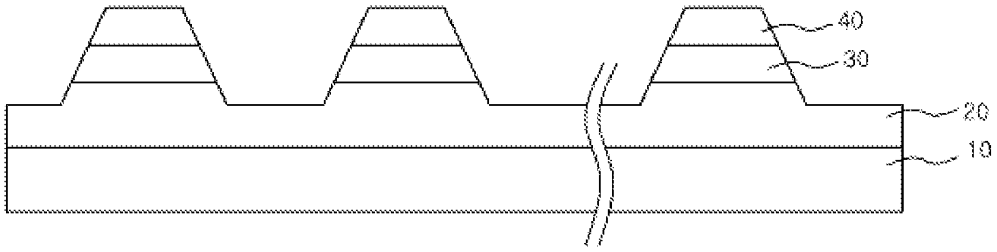
[Figure 5]



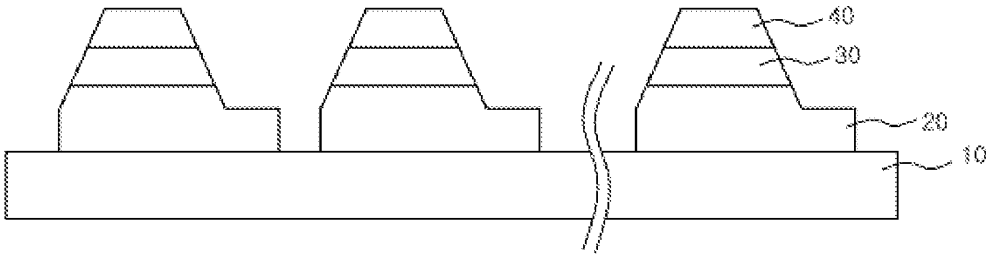
[Figure 6]



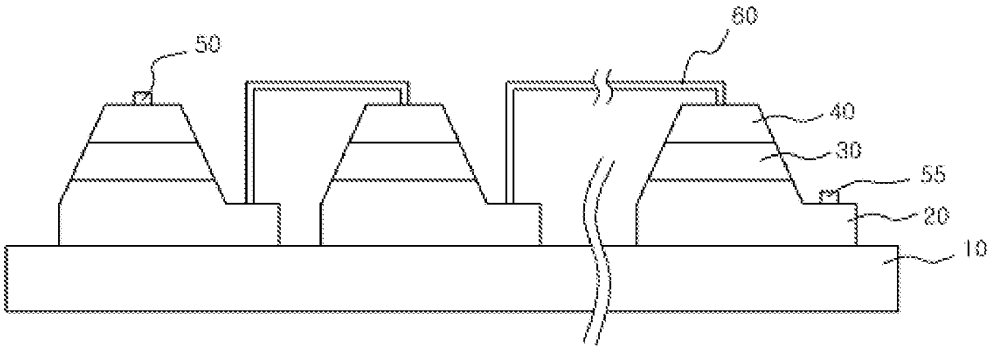
[Figure 7]



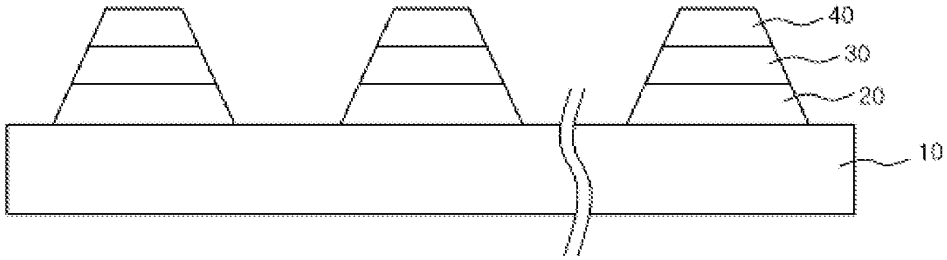
[Figure 8]



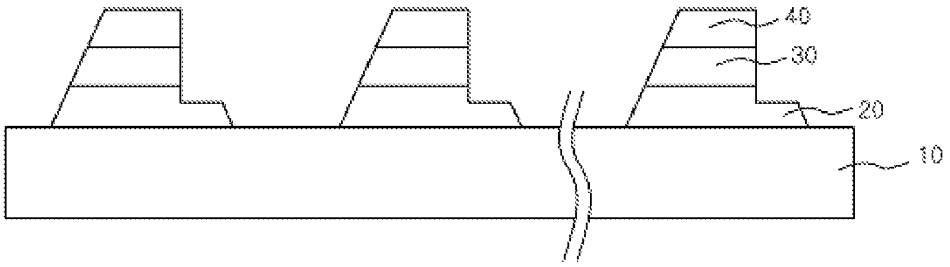
[Figure 9]



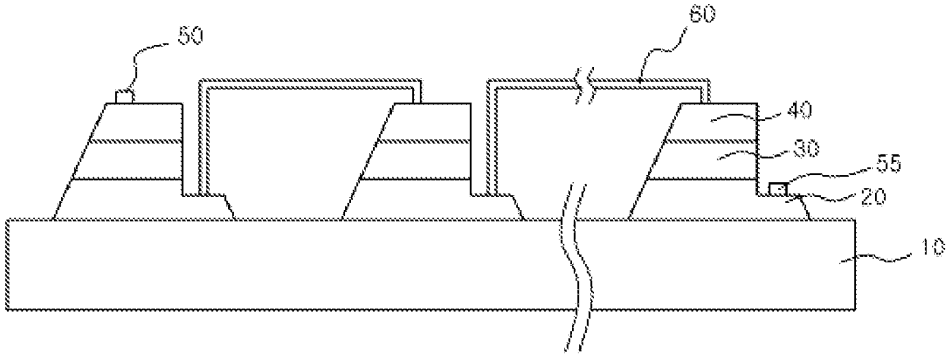
[Figure 10]



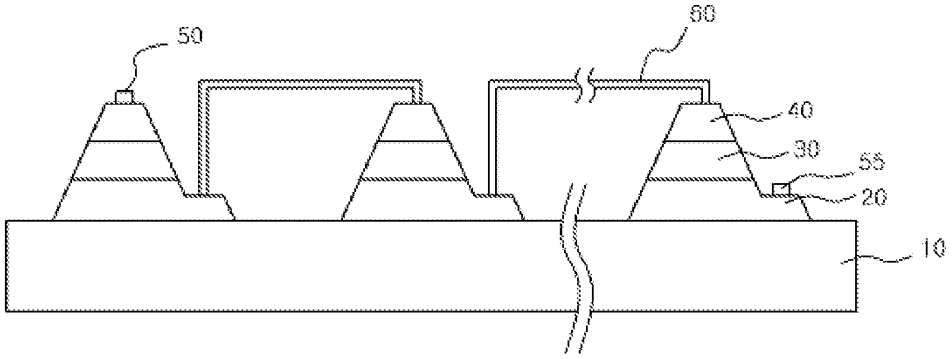
[Figure 11]



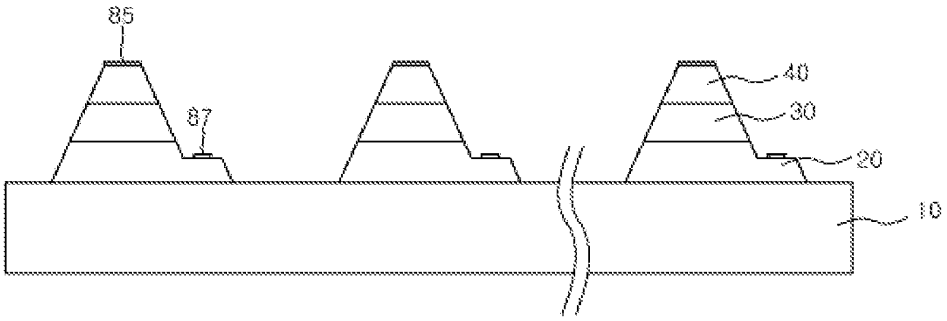
[Figure 12]



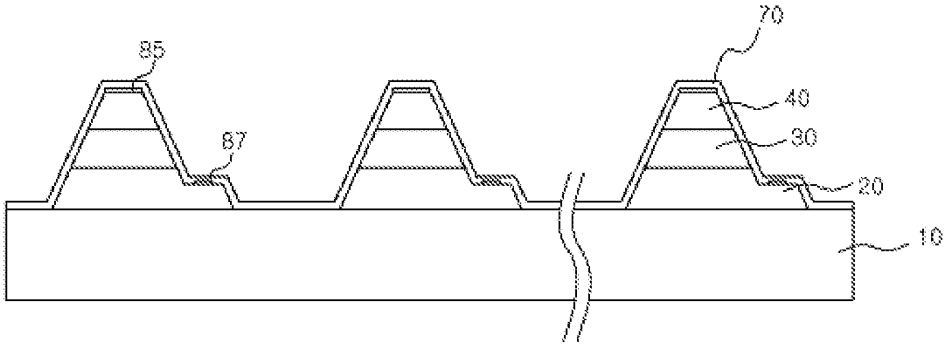
[Figure 13]



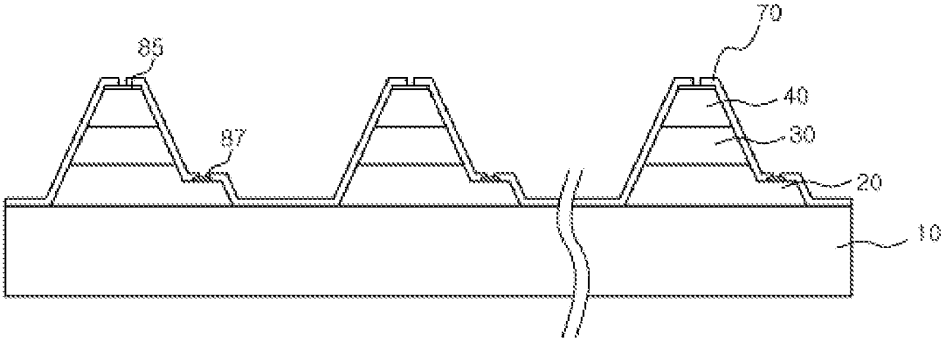
[Figure 14]



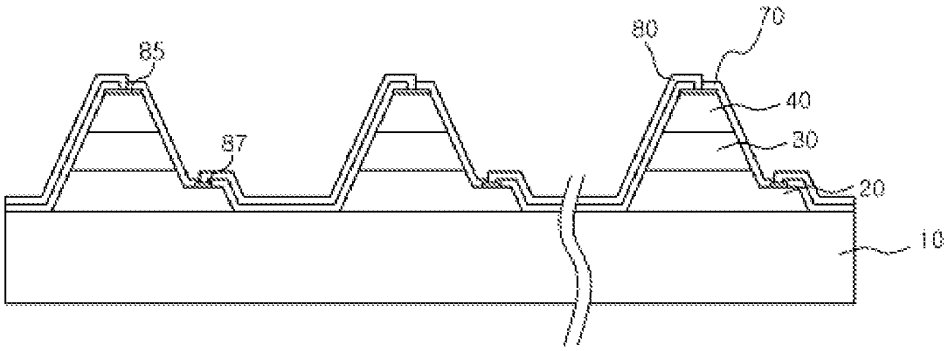
[Figure 15]



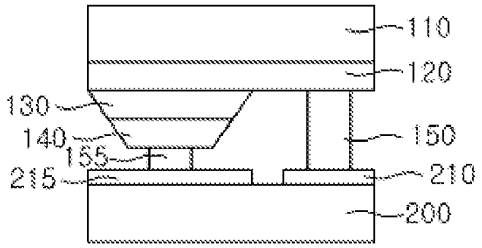
[Figure 16]



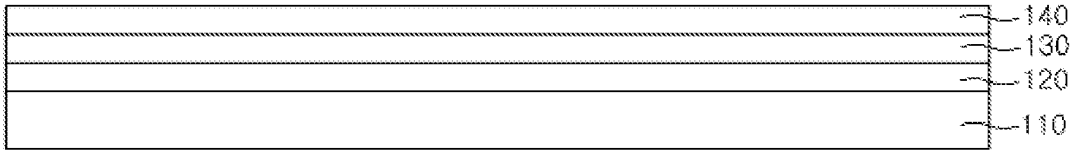
[Figure 17]



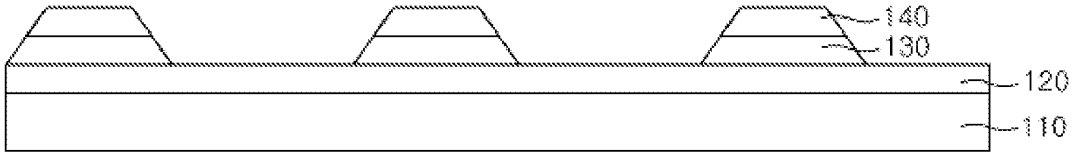
[Figure 18]



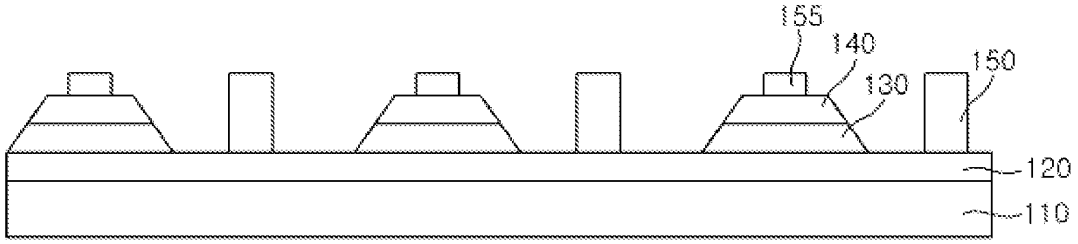
[Figure 19]



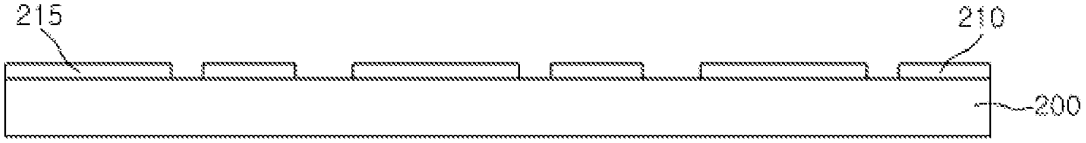
[Figure 20]



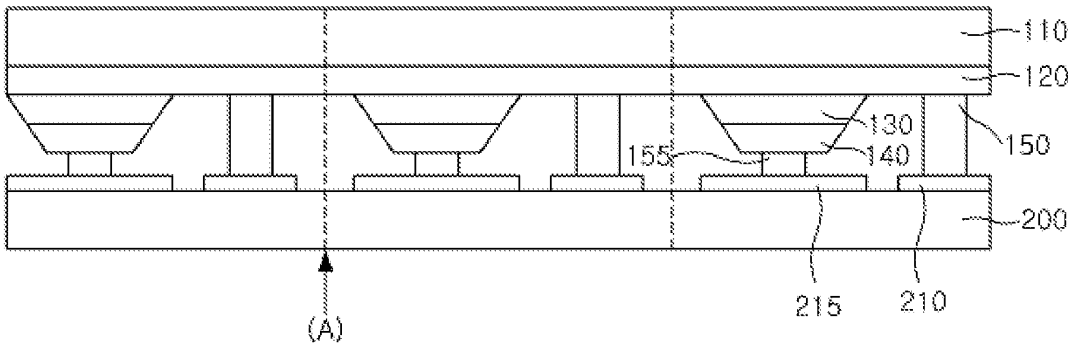
[Figure 21]



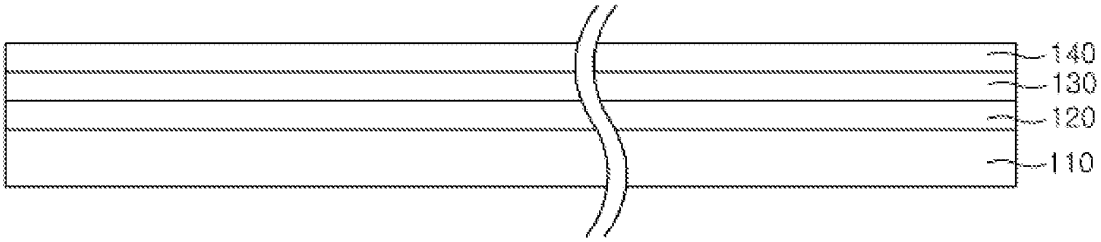
[Figure 22]



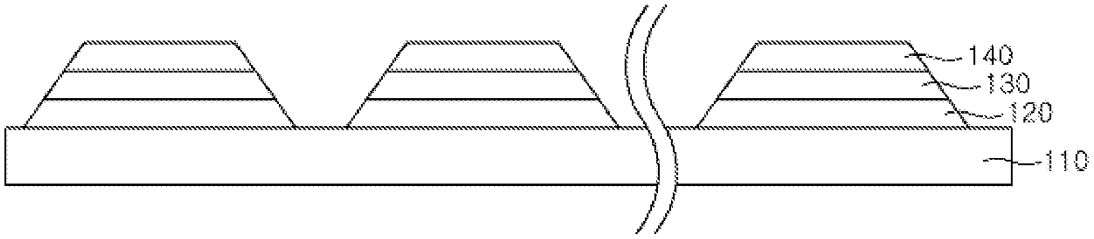
[Figure 23]



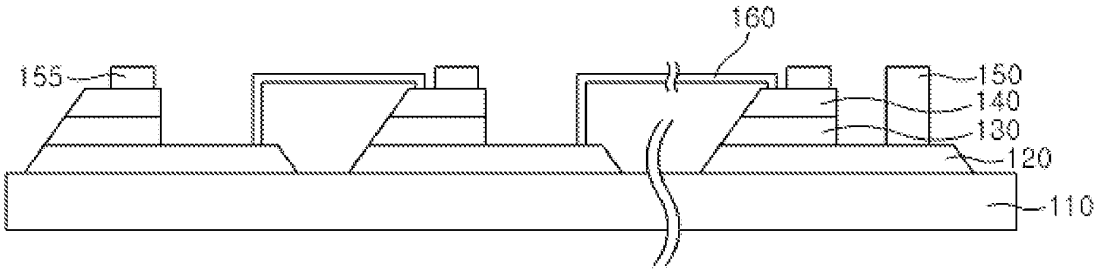
[Figure 24]



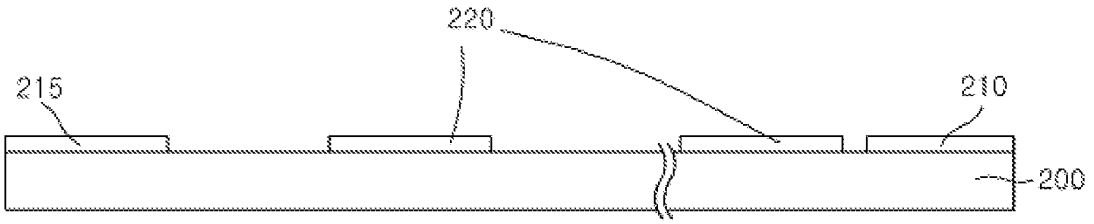
[Figure 25]



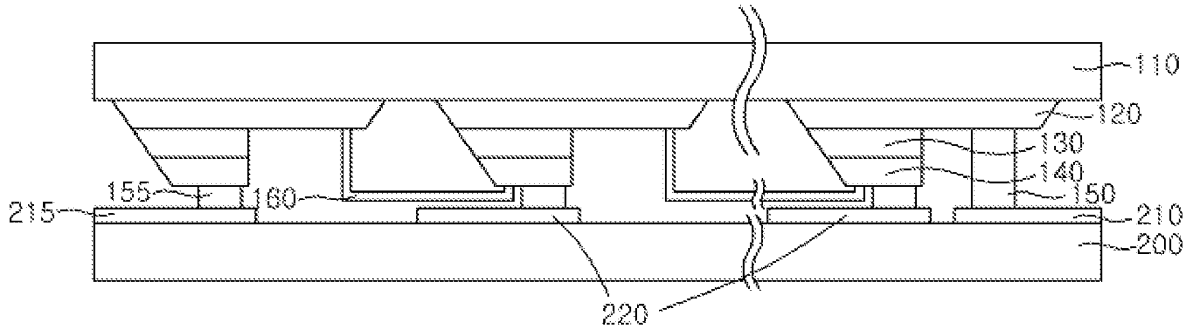
[Figure 26]



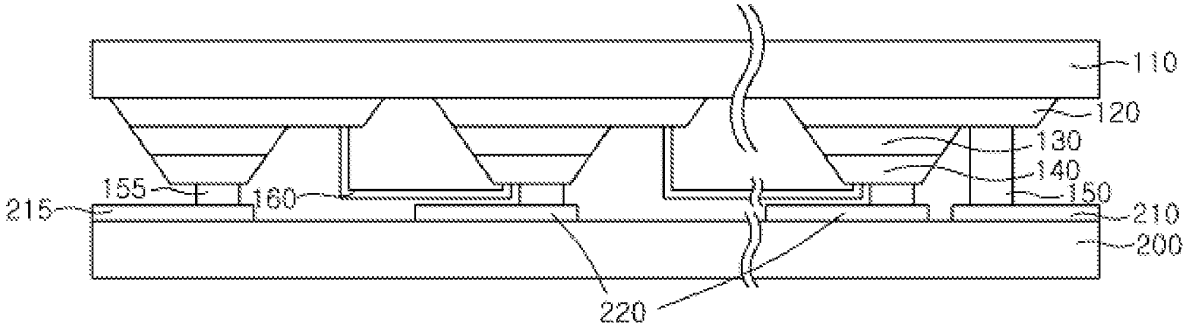
[Figure 27]



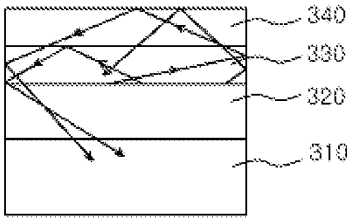
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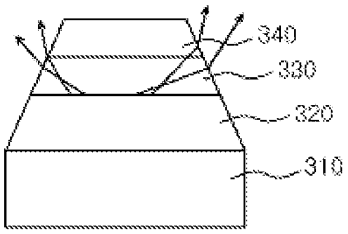
[Figure 29]



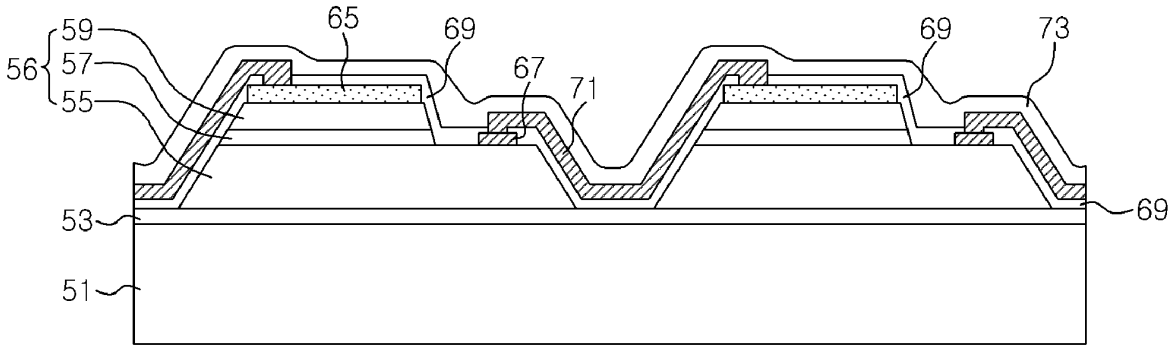
[Figure 30]



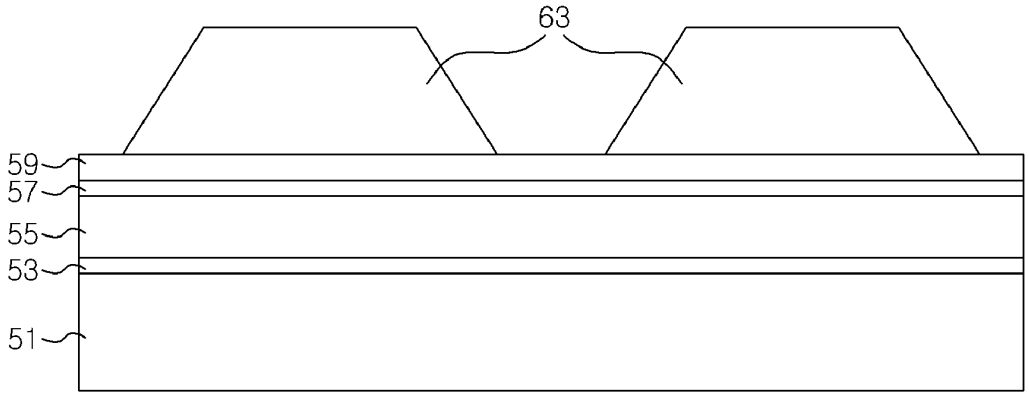
[Figure 31]



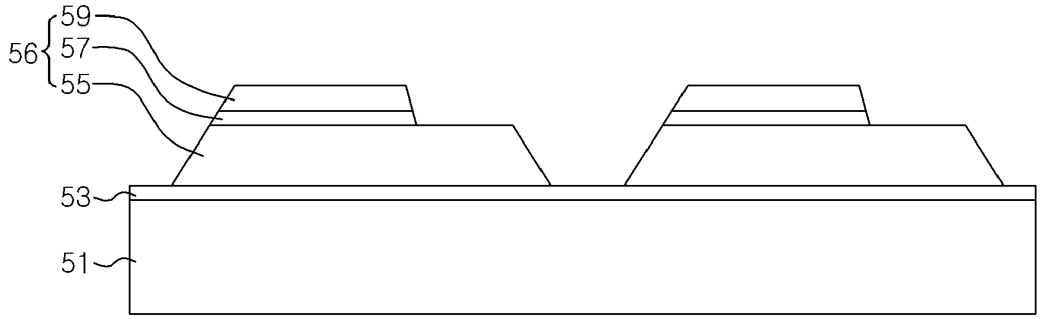
[Figure 32]



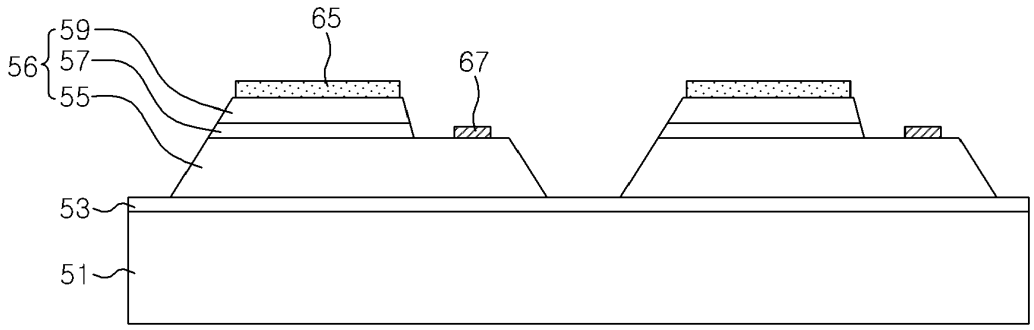
[Figure 33]



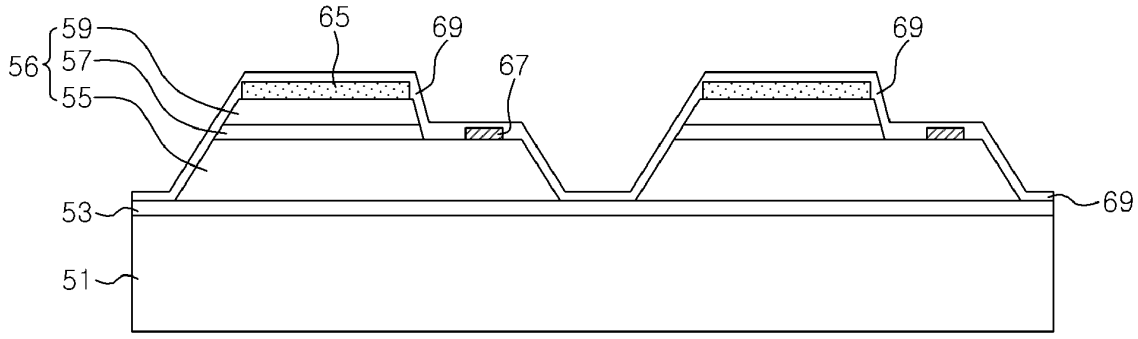
[Figure 34]



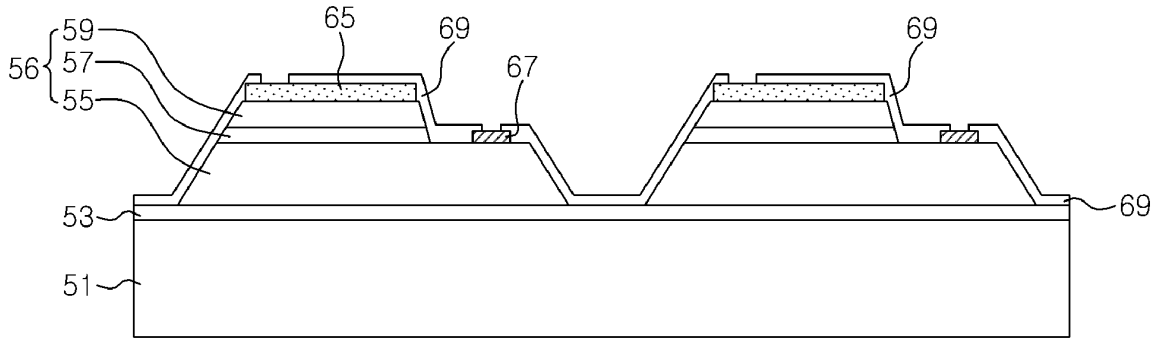
[Figure 35]



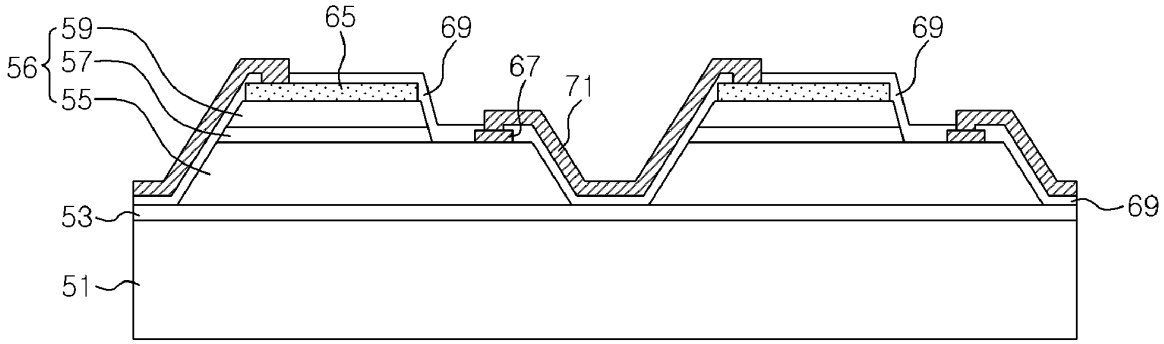
[Figure 36]



[Figure 37]



[Figure 38]



PATENT APPLICATION
Client No. PO070209

COMBINED DECLARATION AND POWER OF ATTORNEY
FILED WITH U.S. DESIGNATED OFFICE UNDER 35 U.S.C. 371(c)(4)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME**, described and claimed in international application number **PCT KR2006/002427**, filed **June 22, 2006**, which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Sec. 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Sec. 119(a)-(d) or Sec. 365(b) of any foreign application(s) for patent or inventor's certificate or Sec. 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
2005-0053979 (Number)	Republic of Korea (Country)	22 June 2005 (Day/Month/Year Filed)	☒ Yes	☐ No
2005-0055179 (Number)	Republic of Korea (Country)	24 June 2005 (Day/Month/Year Filed)	☒ Yes	☐ No
2006-0021801 (Number)	Republic of Korea (Country)	8 March 2006 (Day/Month/Year Filed)	☒ Yes	☐ No

I hereby claim the benefit under Title 35, United States Code, Sec. 119(e) of any United States provisional application listed below:

Provisional Application No. Filing Date

I hereby claim the benefit under Title 35, United States Code, Sec. 120 or §365 (c) of any PCT international application designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Sec. 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Sec. 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

PCT/KR2006/002427	22 June 2006	Pending
(Applic. Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

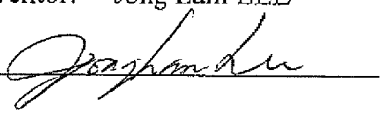
I hereby appoint the attorneys or agents associated with **Customer No. 20575** to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with the above application.

Direct all telephone calls to Hosoon Lee at (503) 222-3613 and send all correspondence to the following address associated with **Customer No. 20575**:

MARGER JOHNSON & McCOLLOM, P.C.
210 S.W. Morrison Street, Suite 400
Portland, Oregon 97204

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: Jong Lam LEE

Inventor's signature:  12/14/07 (Date)

Residence: Pohang, 790-751 Republic of Korea

Citizenship: Republic of Korea

Post Office address: 8-1403 Gyosu Apt., Jigok-Dong, Nam-Gu,
Pohang-Si, Gyeongsangbuk-Do, 790-751, Republic of Korea

Full name of sole or first inventor: Jae Ho LEE

Inventor's signature: Jae Ho, LEE 14 Dec. 2007 (Date)

Residence: Yongin, 448-531 Republic of Korea

Citizenship: Republic of Korea

Post Office address: 309-1405, LG 3-cha Village Apt, Seongbok-Dong,
Suji-Gu, Yongin-Si,Gyeonggi-Do, 448-531, Republic of Korea

Full name of sole or first inventor: Yeo Jin YOON

Inventor's signature: 14. DEC. 2007 (Date)

Residence: Ansan, 426-738 Republic of Korea

Citizenship: Republic of Korea

Post Office address: 101-1505, Yojin Supsok Apt, Sa 1-Dong,
Sagnok-Gu, Ansan-Si, Gyeonggi-Do, 426-738, Republic of Korea

Full name of sole or first inventor: Eu Jin HWANG

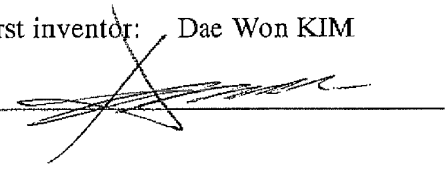
Inventor's signature: 14 Dec (Date)

Residence: Siheung, 429-856 Republic of Korea

Citizenship: Republic of Korea

Post Office address: 303, 1569-7, Jeongwang-Dong,
Siheung-Si, Gyeonggi-Do, 429-856, Republic of Korea

Full name of sole or first inventor: Dae Won KIM

Inventor's signature: 

14. Dec
(Date)

Residence: Seoul, 136-110 Republic of Korea

Citizenship: Republic of Korea

Post Office address: 303-802, Gireum New Town, 1280-2, Gireum-Dong,
Seongbuk-Gu, Seoul, 136-110, Republic of Korea

Approved

PTO/SB/80 (01-05)
Approved for use through 12/31/2008. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

[X] Practitioners associated with the Customer Number: 58027

OR

[ ] Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

[X] The address associated with Customer Number: 58027

OR

[ ] Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address:
Seoul Opto Device Co., Ltd.
1-36 Block, 727-5 Wonsi-dong, Danwon-gu
Gyeonggi-do, Ansan-si, 425-851, Republic of Korea

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record
The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	05/15/08
Name	MURUGANANDAN NITHIPALAN	Telephone	—
Title	PRESIDENT & CEO		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/96 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Jong Lam LEE, et al.

Application No./Patent No.: To be Assigned Filed/Issue Date: November 5, 2009

Entitled: LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME

Seoul Opto Device Co., Ltd., a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest; or
2. ☐ an assignee of less than the entire right, title, and interest

The extent (by percentage) of its ownership interest is _____ %

in the patent application/patent identified above by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 020368, Frame 0597, or for which a copy thereof is attached.

OR

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as shown below:

1. From:_____ To:_____
   The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

2. From:_____ To:_____
   The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

3. From:_____ To:_____
   The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet.

☐ Copies of assignments or other documents in the chain of title are attached.

[**NOTE**: A separate copy (i.e., a true copy of the original document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, if the assignment is to be recorded in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/hae-chan park/	November 5, 2009
Signature	Date
Hae-Chan Park, Reg. 50,114	703-288-5105
Printed or Typed Name	Telephone Number
Attorney	
Title	

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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SCORE Placeholder Sheet for IFW Content

Application Number: 12613275 Document Date: 11/5/2009

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

- Drawings – Other than Black and White Line Drawings

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

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- Examiners may access SCORE content via the eDAN interface.
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Form Revision Date: February 8, 2006

Filing Date: 11/05/09

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

12/613,275

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))							330
SEARCH FEE (37 CFR 1.16(k), (i), or (m))							540
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							220
TOTAL CLAIMS (37 CFR 1.16(i))	10 minus 20 =		X 26 =		OR	X 52 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =		X 110 =			X 220 =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $270 ($135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			N/A			N/A	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1090

APPLICATION AS AMENDED – PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/613,275	11/05/2009	2811	1090	P2317USD1	10	1

CONFIRMATION NO. 5984

58027
H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

FILING RECEIPT

OC000000038823505

Date Mailed: 11/20/2009

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Jong Lam LEE, Pohang-si, KOREA, REPUBLIC OF;
Jae Ho LEE, Yongin-si, KOREA, REPUBLIC OF;
Yeo Jin YOON, Ansan-si, KOREA, REPUBLIC OF;
Eu Jin HWANG, Ansan-si, KOREA, REPUBLIC OF;
Dae Won KIM, Gireum-dong, KOREA, REPUBLIC OF;

Assignment For Published Patent Application

SEOUL OPTO DEVICE CO., LTD., Ansan-si, KOREA, REPUBLIC OF

Power of Attorney: The patent practitioners associated with Customer Number 58027

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REPUBLIC OF KOREA 10-2005-0053797 06/22/2005
REPUBLIC OF KOREA 10-2005-0055179 06/24/2005
REPUBLIC OF KOREA 10-2006-0021801 03/08/2006

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 11/17/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/613,275**

Projected Publication Date: 02/25/2010

Non-Publication Request: No

Early Publication Request: No

Title

LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME

Preliminary Class

257

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/613,275	11/05/2009	Jong Lam LEE	P2317USD1

CONFIRMATION NO. 5984

58027
H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

POA ACCEPTANCE LETTER

OC000000038823092

Date Mailed: 11/20/2009

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/05/2009.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/hsarwari/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

대 한 민 국 특 허 청
KOREAN INTELLECTUAL PROPERTY OFFICE

별첨 사본은 아래 출원의 원본과 동일함을 증명함.

This is to certify that the following application annexed hereto is a true copy from the records of the Korean Intellectual Property Office.

출 원 번 호 : 10-2005-0053797
Application Number

출 원 년 월 일 : 2005년 06월 22일
Filing Date JUN. 22, 2005

출 원 인 : 서울옵토디바이스주식회사
Applicant(s) SEOUL OPTO DEVICE CO., LTD.

2009년 11월 23일

특 허 청
COMMISSIONER

【서지사항】

【서류명】 특허출원서

【권리구분】 특허

【수신처】 특허청장

【제출일자】 2005.06.22

【발명의 국문명칭】 발광 소자 및 이의 제조 방법

【발명의 영문명칭】 Light-emitting device and Method of manufacturing the same

【출원인】

【명칭】 서울옵토디바이스 주식회사

【출원인코드】 1-2003-032642-0

【대리인】

【성명】 남승희

【대리인코드】 9-2003-000036-2

【포괄위임등록번호】 2004-031626-3

【발명자】

【성명】 이종람

【성명의 영문표기】 LEE,Jong Lam

【주민등록번호】 580406-1XXXXXX

【우편번호】 790-834

【주소】 경북 포항시 남구 지곡동 756 교수숙소 E-1401

【국적】 KR

【발명자】

【성명】 이재호

【성명의 영문표기】 LEE,Jae Ho

【주민등록번호】 610216-1XXXXXX

【우편번호】 449-531

【주소】 경기 용인시 성복동 LG3차빌리지 309-1405

【국적】 KR

【심사청구】 청구

【취지】 특허법 제42조의 규정에 의한 출원, 특허법 제60조의 규정에 의한 출원심사를 청구합니다.

대리인 남승희 (인)

【수수료】

【기본출원료】	0 면	38,000 원
【가산출원료】	28 면	0 원
【우선권주장료】	0 건	0 원
【심사청구료】	12 항	493,000 원
【합계】	531,000 원	
【감면사유】	중소기업	
【감면후 수수료】	265,500 원	

【첨부서류】 1.중소기업기본법시행령 제2조에의한 중소기업에 해당함을 증명하는 서류[사업자등록증 및 원천징수이행상황신고서]_1통

【요약서】

【요약】

본 발명은 기판, 상기 기판 상에 형성된 N형 반도체층 및 상기 N형 반도체층 상에 형성된 P형 반도체층을 포함하고, 상기 N형 반도체층 또는 P형 반도체층을 포함하는 측면이 수평면으로부터 20 내지 80° 의 기울기를 갖는 것을 특징으로 하는 발광 소자 및 이의 제조 방법을 제공한다. 본 발명에 의한 발광 소자 및 이의 제조 방법은 발광 효율, 외부 양자 효율, 추출 효율 등의 특성을 향상시키고 신뢰성을 확보하여, 고광도, 고휘도의 광을 발광할 수 있는 장점이 있다.

【대표도】

도 2

【색인어】

발광 소자, LED, 발광 효율, 외부 양자 효율, 질화물 반도체

【명세서】

【발명의 명칭】

발광 소자 및 이의 제조 방법 {Light-emitting device and Method of manufacturing the same}

【도면의 간단한 설명】

<1> 도 1은 종래 발광 소자를 도시한 단면도.

<2> 도 2는 본 발명의 발광 소자를 설명하기 위한 개념 단면도.

<3> 도 3a 및 도 3b는 본 발명에 따른 제 1 실시예의 제조 공정을 설명하기 위한 단면도.

<4> 도 4a 내지 도 4d는 본 발명에 따른 제 2 실시예의 제조 공정을 설명하기 위한 단면도.

<5> 도 5a 내지 도 5d는 본 발명에 따른 제 3 실시예의 제조 공정을 설명하기 위한 단면도.

<6> 도 6a 및 도 6b는 각각 종래 기술과 본 발명에 따른 발광 소자의 효과를 설명하기 위한 개념 단면도.

<7> <도면의 주요 부분에 대한 부호의 설명>

<8> 1 : 기판 2 : N형 반도체층

<9> 3 : 활성층 4 : P형 반도체층

<10> 10 : 기판 20 : N형 반도체층

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<11> 30 : 활성층 40 : P형 반도체층

<12> 50 : P형 본딩 패드 55 : N형 본딩 패드

<13> 60 : 배선

【발명의 상세한 설명】

【발명의 목적】

【발명이 속하는 기술분야 및 그 분야의 종래기술】

<14> 본 발명은 발광 소자 및 이의 제조 방법에 관한 것으로, 보다 상세하게는 질화물계 반도체 발광 소자에 있어서 발광 효율과 휘도를 향상시키기 위한 발광 소자 및 이의 제조 방법에 관한 것이다.

<15> 발광 소자(light emission diode; LED)는 반도체의 p-n 접합 구조를 이용하여 주입된 소수 캐리어(전자 또는 양공)를 만들고 이들의 재결합에 의하여 소정의 빛을 발산하는 소자를 지칭하며, GaAs, AlGaAs, GaN, InGaN, AlGaInP 등의 화합물 반도체(compound semiconductor) 재료의 변경을 통해 발광원을 구성함으로써 다양한 색을 구현할 수 있다. 예를 들어 GaAsP 등을 이용하여 적색 발광 소자를 형성할 수 있고, GaP, InGaN 등을 이용하여 녹색 발광 소자를 형성할 수 있고, InGaN/GaN 더블 헤테로(double hetero) 구조를 이용하여 청색 발광 소자를 형성할 수 있고, AlGaN/GaN 또는 AlGaN/AlGaN 구조를 이용하여 UV 발광 소자를 형성할 수 있다. 특히, GaN은 상온에서 3.4eV의 직접 천이형 밴드갭(direct bandgap)을 가지며 질화인듐(InN), 질화알루미늄(AlN) 같은 물질과 조합하여 1.9eV (InN)에서 3.4eV (GaN),

6.2eV (AlN)까지 직접 에너지 밴드갭을 가지고 있어서 가시광에서부터 자외선 영역까지 넓은 파장 영역 때문에 광소자의 응용 가능성이 매우 큰 물질이다. 이처럼 파장 조절이 가능하여 단파장 영역의 적색, 녹색 및 청색 발광 소자에 의한 천연색(full-color) 구현이 가능해짐으로써 디스플레이 영역은 물론 일반 조명시장으로의 파급 효과가 매우 커질 것으로 예상된다.

<16> 발광 소자는 기존의 전구 또는 형광등에 비해 소모 전력이 작고 수명이 길며, 협소한 공간에 설치 가능하고 진동에 강한 특성을 보인다. 이러한 발광 소자는 표시 소자 및 백라이트로 이용되고 있으며, 소모 전력의 절감과 내구성 측면에서 우수한 특성을 갖기 때문에 최근 일반 조명 용도로 이를 적용하기 위해 활발한 연구가 진행중이다. 이후, 대형 LCD-TV 백라이트, 자동차 헤드라이트, 일반 조명에까지 응용이 확대될 것으로 예상되며, 이를 위해서는 발광 소자의 발광 효율의 개선이 필요하고, 열방출 문제를 해결하여야 하며, 발광 소자의 고휘도화, 고출력화를 달성하여야 한다.

<17> 현재 발광 소자의 성능을 높이기 위한 많은 기술들이 개발되고 있다. 발광 소자의 성능을 나타내는 지표는 발광 효율(lm/W), 내부 양자 효율(%), 외부 양자 효율(%), 추출 효율(%) 등 여러 가지가 있는데, 추출 효율은 발광 소자에 주입된 전자와 발광 소자 밖으로 방출되는 광자의 비에 의하여 결정되며 추출 효율이 높을수록 발광 소자가 밝은 것을 의미한다. 발광 소자의 추출 효율은 칩의 모양이나 표면 형태, 칩의 구조, 패키징 형태에 의하여 많은 영향을 받기 때문에 발광 소자를 설계할 때 세심한 주의가 필요하다.

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<18> 도 1은 종래 발광 소자를 도시한 단면도이다.

<19> 도면을 참조하면, 발광 소자는 기판(1)과, 기판(1) 상에 형성된 N형 반도체층(2)과, 상기 N형 반도체층(2)의 일부에 형성된 활성층(3)과, P형 반도체층(4)을 포함한다. 이는 상기 기판(1) 상에 N형 반도체층(2), 활성층(3), P형 반도체층(4)을 순차적으로 형성한 후, 소정 영역의 P형 반도체층(4)과 활성층(3)을 식각하여 N형 반도체층(2)의 일부를 노출시키고, 그 노출된 N형 반도체층(2) 상면과 P형 반도체층(2) 상면으로 각각 소정의 전압을 인가하기 위한 것이다.

<20> 발광 소자의 활성층에서 생성된 광은 칩의 6개의 면으로부터 방출되고, 광추출 효율은 일반적으로 광의 임계각에 의하여 결정된다. 그러나 종래 발광 소자는 N형 반도체층을 노출시키기 위해 식각할 때, P형 반도체층과 활성층의 측면이 수직 가공되어 발광 소자의 내부에서 생성된 광의 일부가 수평면으로부터 수직으로 가공된 식각면에서 전반사된다. 그리하여 전반사되는 상당량의 광은 내부 반사에 의하여 밖으로 방출되지 못한채 발광 소자 내부에서 소멸된다. 즉, 전기 에너지가 빛 에너지로 변환되어 소자의 외부로 빠져나오는 발광 효율이 낮은 문제점이 있다.

【발명이 이루고자 하는 기술적 과제】

<21> 본 발명은 상기 문제점을 해결하기 위한 것으로, 발광 효율, 외부 양자 효율, 추출 효율 등의 특성을 향상시키고 신뢰성을 확보하여, 고광도, 고휘도의 광을 발광할 수 있는 발광 소자 및 이의 제조 방법을 제공하는 것을 목적으로 한다.

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【발명의 구성】

<22> 상술한 목적을 달성하기 위하여, 본 발명은 기판, 상기 기판 상에 형성된 N형 반도체층 및 상기 N형 반도체층 상에 형성된 P형 반도체층을 포함하고, 상기 N형 반도체층 또는 P형 반도체층을 포함하는 측면이 수평면으로부터 20 내지 80° 의 기울기를 갖는 것을 특징으로 하는 발광 소자를 제공한다.

<23> 또한, 기판 상에 N형 반도체층, 상기 N형 반도체층의 일부에 형성된 P형 반도체층을 포함하는 발광 셀을 다수개 포함하고, 상기 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층이 연결되고, 상기 발광 셀의 N형 반도체층 또는 P형 반도체층을 포함하는 측면이 수평면으로부터 20 내지 80° 의 기울기를 갖는 것을 특징으로 하는 발광 소자를 제공한다. 상기 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층을 연결하기 위한 배선을 더 포함할 수 있다.

<24> 상기 P형 반도체층 상에 투명 전극층을 더 포함할 수 있으며, 상기 P형 반도체층과 상기 N형 반도체층 상에 Cr 또는 Au를 포함한 P형 오믹금속층과 N형 오믹금속층을 각각 더 포함할 수 있다.

<25> 또한 본 발명은 기판 상에 N형 반도체층, P형 반도체층을 순차적으로 형성하는 단계, 상기 P형 반도체층 상에 측면이 수평면으로부터 수직이 아닌 소정의 기울기를 갖는 식각 마스크 패턴을 형성하는 단계, 상기 식각 마스크 패턴에 의해 노출된 P형 반도체층과, 상기 식각 마스크 패턴을 제거하는 단계를 포함하는 발광 소자

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의 제조 방법을 제공한다.

<26> 상기 식각 마스크 패턴을 형성하는 단계는, 3 내지 50㎛ 두께의 감광막을 이용할 수 있다.

<27> 상기 식각 마스크 패턴을 형성하는 단계는, 상기 P형 반도체층 상에 상기 감광막을 도포하는 단계, 소정의 마스크 패턴에 따라 상기 감광막을 노광하는 단계, 상기 노광 후 베이킹 공정 없이 현상하는 단계를 포함할 수 있다.

<28> 또한, 상기 식각 마스크 패턴을 형성하는 단계는, 상기 P형 반도체층 상에 상기 감광막을 도포하는 단계, 소정의 마스크 패턴에 따라 상기 감광막을 노광하는 단계, 100℃ 내지 140℃의 온도에서 하드 베이킹을 하는 단계 및 현상하는 단계를 포함할 수 있다.

<29> 상기 발광 소자의 제조 방법에 있어서, 상기 P형 반도체층의 제거로 인해 노출된 N형 반도체층의 일부를 제거하여 다수개의 발광 셀을 형성하는 단계 및 브리지 배선을 통해 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층을 연결하는 단계를 더 포함할 수 있으며, 상기 브리지 배선은 브리지(Bridge) 공정 또는 스텝 커버(Step Cover) 공정을 통해 일 발광 셀의 N형 반도체층과 인접한 다른 일 발광 셀의 P형 반도체층을 연결할 수 있다.

<30> 또한 상기 P형 반도체층과 상기 식각 마스크 패턴을 제거하는 단계 이후에, 상기 기판의 배면을 소정 두께 제거하는 단계 및 상기 기판의 배면에 Al, Ti, Ag, W, Ta, Ni, Ru 또는 그 합금을 증착하는 단계를 더 포함할 수 있다.

<31> 이하, 첨부된 도면을 참조하여 본 발명에 의한 발광 소자 및 이의 제조 방법에 대하여 상세히 설명하기로 한다. 그러나 본 발명은 이하에서 개시되는 실시예에 한정되는 것이 아니라 서로 다른 다양한 형태로 구현될 것이며, 단지 본 실시예는 본 발명의 개시가 완전하도록 하며, 통상의 지식을 가진 자에게 발명의 범주를 완전하게 알려주기 위해 제공되는 것이다.

<32> 도 2는 본 발명의 발광 소자를 설명하기 위한 개념 단면도이다.

<33> 도면을 참조하면, 발광 소자는 기판(10)과, 기판(10) 상에 순차적으로 형성된 N형 반도체층(20), 활성층(30) 및 P형 반도체층(40)을 포함한다. 상기 P형 반도체층(40), 활성층(30), 소정 부분의 N형 반도체층(20)의 측면은 수평면으로부터 80 내지 20° 의 기울기를 갖고, 이러한 측면으로부터 광의 임계각을 변화시키고 용이하게 광을 추출할 수 있어 발광 소자의 발광 효율을 개선할 수 있다.

<34> 도 3a 내지 도 3b는 본 발명에 따른 제 1 실시예의 제조 공정을 설명하기 위한 단면도들이다.

<35> 도 3a를 참조하면, 기판(10) 상에 N형 반도체층(20), 활성층(30) 및 P형 반도체층(40)을 순차적으로 형성한다.

<36> 기판(10)은 발광 소자를 제작하기 위한 통상의 웨이퍼를 지칭하는 것으로, Al_2O_3, SiC, ZnO, Si, GaAs, GaP, $LiAl_2O_3$, BN, AlN 및 GaN 중 적어도 어느 하나의

기판(10)을 사용한다. 본 실시예에서는 사파이어로 구성된 결정 성장 기판을 사용한다.

<37> 상기 기판(10) 상에 결정 성장시 기판(10)과 후속층들의 격자 부정합을 줄이기 위한 버퍼층(미도시)을 더 형성할 수 있다. 버퍼층은 반도체 재료인 GaN 또는 AlN을 포함하여 형성할 수 있다.

<38> N형 반도체층(20)은 전자가 생성되는 층으로서, N형 불순물이 주입된 질화갈륨(GaN)을 사용하는 것이 바람직하고, 이에 한정되지 않고 다양한 반도체 성질의 물질층이 가능하다. 본 실시예에서는 N형 $Al_xGa_{1-x}N(0\leq x\leq 1)$을 포함하는 N형 반도체층(20)을 형성한다. 또한, P형 반도체층(40)은 정공이 생성되는 층으로서, P형 불순물이 주입된 질화갈륨(GaN)을 사용하는 것이 바람직하고, 이에 한정되지 않고 다양한 반도체 성질의 물질층이 가능하다. 본 실시예에서는 P형 $Al_xGa_{1-x}N(0\leq x\leq 1)$을 포함하는 P형 반도체층(40)을 형성한다. 뿐만 아니라 상기 반도체층으로 InGaN을 사용할 수 있다. 또한 상기의 N형 반도체층(20) 및 P형 반도체층(40)은 다층막으로 형성할 수도 있다.

<39> 활성층(30)은 소정의 밴드 갭을 가지며 양자 우물이 만들어져 전자 및 정공이 재결합되는 영역으로서, InGaN을 포함하여 이루어질 수 있다. 활성층(30)을 이루는 물질의 종류에 따라 전자 및 전공이 결합하여 발생하는 발광 파장이 변화된다. 따라서, 목표로 하는 파장에 따라 활성층(30)에 포함되는 반도체 재료를 조절하는 것이 바람직하다.

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<40> 상술한 물질층들은 유기금속 화학 증착법(MOCVD; Metal Organic Chemical Vapor Deposition), 화학 증착법(CVD; Chemical Vapor Deposition), 플라즈마 화학 증착법(PCVD; Plasma-enhanced Chemical Vapor Deposition), 분자선 성장법(MBE; Molecular Beam Epitaxy), 수소화물 기상 성장법(HVPE; Hydride Vapor Phase Epitaxy) 등을 포함한 다양한 증착 및 성장 방법을 통해 형성된다.

<41> 이후, 소정의 식각 공정을 통해 P형 반도체층(40) 및 활성층(30)의 일부를 제거하여 N형 반도체층(20)의 일부를 노출시킨다. P형 반도체층(40) 상에 식각 마스크 패턴을 형성한 다음, 건식 또는 습식 식각 공정을 실시하여 P형 반도체층(40) 및 활성층(30)을 제거하여 N형 반도체층(20)을 노출시킨다.

<42> 일반적으로 상기 식각 공정을 위하여 P형 반도체층 상면에 1 내지 2㎛ 두께로 감광막(photoresist)을 도포한 후, 80 내지 90℃의 온도에서 소프트 베이킹(soft baking)을 한다. 다음으로, 소정의 포토 마스크(photo mask)를 통해 자외선(UV) 영역의 빛을 조사하여 마스크 상에 형성된 패턴을 도포된 감광막에 전사하는 노광(exposure) 공정을 진행한다. 이후, 100 내지 120℃의 온도에서 하드 베이킹(hard baking)을 하고, 노광 공정을 통해 상대적으로 결합이 약해져 있는 부분의 감광막을 용제를 사용하여 녹여내는 현상(developing) 공정을 진행한다. 이러한 과정을 통해 상기 P형 반도체층(40) 상에 소정의 식각 마스크 패턴이 형성된다.

<43> 그러나 본 실시예는 상기 식각 마스크 패턴을 형성할 때, 3 내지 50㎛ 두께로 감광막을 종래에 비해 두껍게 도포하고 소프트 베이킹을 거쳐 노광 공정을 실시한다. 그 다음에 하드 베이킹을 통하지 않고 바로 현상하면, 남아있는 감광막의 현

상된 측면은 수평면으로부터 50 내지 80° 정도의 기울기를 갖는 경사진 면을 형성하게 된다. 이어서, 이러한 측면의 기울기를 갖는 식각 마스크 패턴을 사용하여 노출된 영역의 P형 반도체층(40), 활성층(30), 소정의 N형 반도체층(20)을 식각하면, 식각된 P형 반도체층(40), 활성층(30), 소정의 N형 반도체층(20)의 측면은 마찬가지로 수평면으로부터 50 내지 80° 정도의 기울기를 갖는 경사진 면을 얻을 수 있다.

<44> 즉, 도 3a의 P형 반도체층(40) 상에 3 내지 50㎛ 두께로 감광막을 두껍게 도포하여 노광 후 하드 베이킹 없이 바로 현상한 식각 마스크 패턴을 형성한다. 상기 식각 마스크 패턴에 의해 노출된 P형 반도체층(40), 활성층(30)을 유도 결합 플라즈마(ICP; Inductive Coupled Plasma) 또는 건식 식각 공정을 통해 제거하여 N형 반도체층(20)을 노출시킨다. 노출된 N형 반도체층(20)의 일부를 더 제거할 수 있다. 이후, 식각 마스크 패턴을 제거하면, 도 3b에 도시한 바와 같이 P형 반도체층(40), 활성층(30), 일부 N형 반도체층(20)의 측면이 수평면으로부터 수직(90°)이 아닌, 소정의 기울기를 갖는 발광 소자를 제조할 수 있다.

<45> 또한, 도 3a의 P형 반도체층(40) 상에 3 내지 50㎛ 두께로 감광막을 두껍게 도포하여 노광 후 하드 베이킹을 실시하는 경우에, 하드 베이킹 온도를 100℃ 내지 140℃로 하여 진행하고 현상을 하게 되면, 현상된 감광막의 측면이 수평면으로부터 80° 에서 20° 까지의 기울기를 갖도록 식각된 측면을 얻을 수 있다. 예를 들어, 100℃의 온도에서 하드 베이킹을 하는 경우에 수평면으로부터 80° 정도의 기울기를 갖는 식각 마스크 패턴을 얻을 수 있으며, 이를 이용하여 P형 반도체층(40), 활

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성층(30), 일부 N형 반도체층(20)의 측면이 수평면으로부터 80° 정도의 기울기를 갖도록 할 수 있다. 또한, 140℃의 온도에서 하드 베이킹을 하는 경우에 수평면으로부터 20° 정도의 기울기를 갖는 식각 마스크 패턴을 얻을 수 있으며, 이를 이용하여 P형 반도체층(40), 활성층(30), 일부 N형 반도체층(20)의 측면이 수평면으로부터 20° 정도의 기울기를 갖도록 할 수 있다.

<46> 이와 같이 3 내지 50㎛ 두께의 감광막을 노광 후 100℃ 내지 140℃의 온도에서 하드 베이킹을 하고 현상한 식각 마스크 패턴을 사용함으로써, 식각된 P형 반도체층(40), 활성층(30), 소정의 N형 반도체층(20)의 측면이 마찬가지로 수평면으로부터 80° 에서 20° 까지의 기울기를 갖도록 식각된 측면을 얻을 수 있다. 그리하여 발광층의 내부에서 생성된 광은 다양한 기울기를 갖도록 식각된 측면에 전반사되지 않고 발광 소자의 외부로 빠져나가게 된다.

<47> 상기 P형 반도체층(40) 상부에 P형 반도체층(40)의 저항을 줄이고 광의 투과율을 향상시키기 위해 투명전극층을 더 형성할 수 있으며, P형 반도체층(40) 또는 노출된 N형 반도체층(20) 상부에 전류의 공급을 원활히 하기 위한 별도의 오믹금속층을 더 형성할 수도 있다. 상기 투명전극층으로는 ITO(Indium Tin Oxide), ZnO 또는 전도성을 갖는 투명 금속을 사용할 수 있고, 상기 오믹금속층으로는 Cr, Au를 사용할 수 있다. 또한, 전압의 인가를 위해 P형 반도체층(40)의 상부에 P형 전극을 더 형성할 수 있고, N형 반도체층(20)의 상부에 N형 전극을 더 형성할 수 있다.

<48> 또한 발광 소자의 열 방출 특성을 향상시키기 위해 상기 기판(10)의 배면을 소정 두께 제거한 후에 Al, Ti, Ag, W, Ni, Ta, Ru 또는 그 합금을 기판(10)의 배

면에 증착시킬 수 있다.

<49> 도면에서 볼 수 있듯이, 다수 개의 발광 소자를 하나의 기판(10) 상에 제작할 수 있고, 이러한 경우 추후에 각각의 발광 소자로 절단하여 사용하게 된다. 이때, 도 3b의 A 부분은 이러한 다수 개의 발광 소자를 개별적으로 절단하기 위한 절단부이다.

<50> 이로써 P형 반도체층(40), 활성층(30), N형 반도체층(20) 측면의 일부가 수평면으로부터 수직이 아닌, 소정의 기울기를 갖는 발광 소자를 제조할 수 있다.

<51> 상술한 본 발명의 발광 소자의 제조 공정은 일 실시예일뿐 이에 한정되지 않고, 다양한 공정과 제조 방법이 소자의 특성 및 공정의 편의에 따라 변경되거나 추가될 수 있다.

<52> 상술한 바와 같이 본 발명에 따른 발광 소자는 P형 반도체층, 활성층, N형 반도체층의 일부 측면이 수평면으로부터 수직이 아닌, 소정의 기울기를 갖도록 형성함으로써, 종래의 발광 소자에 비하여 발광 효율을 향상시킬 수 있다. 이는 종래의 평탄한 표면에서 반사되었던 광자가 다양한 각의 표면에 의해 반사되지 않고 외부로 빠져나가기 때문이다.

<53> 도 4a 내지 도 4d는 본 발명에 따른 제 2 실시예의 제조 공정을 설명하기 위한 단면도들이다.

<54> 이는 제 1 실시예의 경우와 거의 동일하며, 단지 제 2 실시예는 웨이퍼 레벨에서 다수의 발광 셀을 직렬, 병렬 또는 직병렬 연결하여 소자의 크기를 줄이고,

적정 전압 및 전류에 구동되도록 하여 조명용으로 사용가능하며 교류 전원에서도 구동할 수 있는 발광 소자를 제공한다.

<55> 도 4a를 참조하면, 유기금속 화학 증착법, 화학 증착법, 플라즈마 화학 증착법, 분자선 성장법, 수소화물 기상 성장법 등의 다양한 증착 방법을 통해 기판(10) 상에 N형 반도체층(20), 활성층(30) 및 P형 반도체층(40)을 순차적으로 형성한다. 상기 기판(10) 상에 결정 성장시 기판(10)과 후속층들의 격자 부정합을 줄이기 위한 버퍼층을 더 형성할 수 있다. 이는 도 3a의 경우와 동일하며, 이와 중복되는 설명은 생략한다.

<56> 이후, 소정의 식각 공정을 통해 P형 반도체층(40) 및 활성층(30)의 일부를 제거하여 N형 반도체층(20)의 일부를 노출한다. 즉, P형 반도체층(40) 상에 3 내지 50㎛ 두께로 감광막을 두껍게 도포하여 노광 후 하드 베이킹 없이 바로 현상하여 식각 마스크 패턴을 형성한다. 상기 식각 마스크 패턴에 의해 노출된 P형 반도체층(40), 활성층(30)을 유도 결합 플라즈마 또는 건식 식각 공정을 통해 제거하여 N형 반도체층(20)을 노출시킨다. 노출된 N형 반도체층(20)의 일부를 더 제거할 수 있다. 이후, 식각 마스크 패턴을 제거하면, 도 4b에 도시한 바와 같이 P형 반도체층(40), 활성층(30), 소정의 N형 반도체층(20)의 측면이 수평면으로부터 50 내지 80° 정도의 기울기를 갖는 경사진 면을 얻을 수 있다.

<57> 또한 P형 반도체층(40) 상에 3 내지 50㎛ 두께로 감광막을 두껍게 도포하여 노광 후 100℃ 내지 140℃의 온도에서 하드 베이킹을 하고 현상하여 식각 마스크 패턴을 형성한다. 이러한 식각 마스크 패턴에 의해 노출된 P형 반도체층(40) 및 활

성층(30)을 식각한 후 식각 마스크 패턴을 제거하여 식각된 P형 반도체층(40) 및 활성층(30)의 측면이 80° 에서 20° 까지의 다양한 기울기를 갖도록 할 수도 있다.

<58> 다음으로 기판(10) 상에 다수 개의 발광 셀을 형성하기 위하여 노출된 N형 반도체층(20)의 소정 영역을 기판(10)이 노출되도록 제거한다. 이를 위해 상기 기판(10)이 노출될 소정 영역을 제외한 모든 부분에 소정의 마스크 패턴을 형성한 다음, 상기 마스크 패턴에 의해 노출된 영역의 N형 반도체층(20)을 식각하여 도 4c에 도시한 바와 같이 다수개의 발광 셀을 전기적으로 분리한다. 이 때, 상술한 공정을 통해 측면이 경사진 마스크 패턴을 형성하여 식각함으로써, 다수개의 발광 셀이 분리되는 N형 반도체층(20)의 측면이 수평면으로부터 수직이 아닌, 다양한 기울기를 갖도록 할 수도 있다.

<59> P형 반도체층(40) 상부에 P형 반도체층(40)의 저항을 줄이고 광의 투과율을 향상시키기 위해 ITO와 같은 투명전극층을 더 형성할 수 있으며, P형 반도체층(40) 또는 노출된 N형 반도체층(20) 상부에 Cr, Au를 사용하여 전류의 공급을 원활히 하기 위한 별도의 오믹금속층을 더 형성할 수도 있다.

<60> 도 4d를 참조하면, 소정의 배선 형성 공정을 통해 인접한 발광 셀간의 N형 반도체층(20)과 P형 반도체층(40)을 연결한다. 즉, 일 발광 셀의 노출된 N형 반도체층(20)과 이와 인접한 다른 일 발광 셀의 P형 반도체층(40)을 배선으로 연결한다. 이 때 브리지(Bridge) 공정 또는 스텝 커버(Step Cover) 등의 공정을 통해 각기 인접한 발광 셀의 N형 반도체층(20)과 P형 반도체층(40) 간을 전기적으로 연결하는 도전성 배선을 형성한다.

<61> 상술한 브리지 공정은 에어브리지 공정이라고도 하며, 서로 연결할 칩 간에 포토 공정을 이용해 감광액을 도포하고 현상하여 감광막 패턴을 형성하고, 그 위에 금속 등의 물질을 진공 증착 등의 방법으로 먼저 박막으로 형성하고, 다시 그 위에 전기 도금(electroplating), 무전해 도금(electroplating) 또는 금속 증착 등의 방법으로 금을 포함하는 도전성 물질을 일정 두께로 도포한다. 이후, 솔벤트 등의 용액으로 감광막 패턴을 제거하면 도전성 물질의 하부는 다 제거되고 브리지 형태의 도전성 물질만이 공간에 형성된다.

<62> 또한, 스탭 커버 공정은 서로 연결할 칩 간에 포토 공정을 이용해 감광액을 도포하고, 현상하여 서로 연결될 부분만을 남기고 다른 부분은 감광막 패턴으로 뒤덮고, 그 위에 전기 도금, 무전해 도금 또는 금속 증착 등의 방법으로 금을 포함하는 도전성 물질을 일정 두께로 도포한다. 이어서, 솔벤트 등의 용액으로 감광막 패턴을 제거하면 도전성 물질이 덮힌 이외의 부분은 다 제거되고 이 덮힌 부분 만이 남아 연결할 칩 사이를 전기적으로 연결시키는 역할을 하게 되다.

<63> 상기의 배선으로는 금속뿐만 아니라 전도성을 갖는 모든 물질들을 사용할 수 있다.

<64> 또한 발광 소자에 외부 전압을 인가하기 위해 일 가장자리에 위치한 발광 셀의 P형 반도체층(40)에 P형 본딩 패드(50)를 형성하고, 다른 일 가장자리에 위치한 발광 셀의 노출된 N형 반도체층(20) 상에 N형 본딩 패드(55)를 형성한다.

<65> 이로써 P형 반도체층(40), 활성층(30), N형 반도체층(20) 측면의 일부가 수

평면으로부터 수직이 아닌, 소정의 기울기를 갖는 발광 셀이 다수개 연결되어 형성된 발광 소자를 제조할 수 있다.

<66> 상술한 본 발명의 발광 소자의 제조 공정은 일 실시예일뿐 이에 한정되지 않고, 다양한 공정과 제조 방법이 소자의 특성 및 공정의 편의에 따라 변경되거나 추가될 수 있다. 예를 들어 발광 소자의 열 방출 특성을 향상시키기 위해 상기 기판의 배면을 소정 두께 제거한 후에 Al, Ti, Ag, W, Ni, Ta, Ru 또는 그 합금을 기판의 배면에 증착시킬 수 있다.

<67> 도 5a 내지 도 5d는 본 발명에 따른 제 3 실시예의 제조 방법을 설명하기 위한 단면도들이다.

<68> 이는 제 2 실시예의 경우와 거의 동일하며, 단지 제 2 실시예는 N형 반도체층(20)을 먼저 노출시킨 다음 발광 셀간의 분리를 위해 노출된 N형 반도체층(20)의 일부를 제거하였으나, 제 3 실시예는 다수개의 발광 셀을 먼저 분리한 후 N형 반도체층(20)의 일부를 노출시킨 것이다. 상기 제 2 실시예의 경우와 중복되는 설명은 생략한다.

<69> 도 5a를 참조하면, 기판(10) 상에 순차적으로 형성된 N형 반도체층(20), 활성층(30) 및 P형 반도체층(40)의 일부를 제거하여 다수개의 발광 셀을 형성한다. 이를 위해, P형 반도체층(40) 상에 3 내지 50㎛ 두께로 감광막을 두껍게 도포하여 노광 후 하드 베이킹 없이 바로 현상하여 식각 마스크 패턴을 형성한다. 상기 식각 마스크 패턴에 의해 노출된 P형 반도체층(40), 활성층(30), 소정의 N형 반도체층(20)과 상기 식각 마스크 패턴을 제거하여 발광 셀을 분리한다. 그리하여 도시한

바와 같이 P형 반도체층(40), 활성층(30), N형 반도체층(20)의 전 측면이 수평면으로부터 50 내지 80° 정도의 기울기를 갖는 경사진 면을 얻을 수 있다. 또한 P형 반도체층(40) 상에 3 내지 50㎛ 두께로 감광막을 두껍게 도포하여 노광 후 100℃ 내지 140℃의 온도에서 하드 베이킹을 하고 현상한 식각 마스크 패턴을 사용하여 P형 반도체층(40), 활성층(30), N형 반도체층(20)을 제거함으로써, P형 반도체층(40), 활성층(30), N형 반도체층(20)의 전 측면을 다양한 기울기로 형성할 수 있다.

<70> 이후, 도 5b에 도시한 바와 같이 소정의 식각 공정을 통해 P형 반도체층(40) 및 활성층(30)의 일부를 제거하여 N형 반도체층(20)의 일부를 노출한다.

<71> 또한 P형 반도체층(40) 상부에 P형 반도체층(40)의 저항을 줄이고 광의 투과율을 향상시키기 위해 투명전극층을 더 형성할 수 있으며, P형 반도체층(40) 또는 노출된 N형 반도체층(20) 상부에 전류의 공급을 원활히 하기 위한 별도의 오믹금속층을 더 형성할 수도 있다. 상기 투명전극층으로는 ITO(Indium Tin Oxide), ZnO 또는 전도성을 갖는 투명 금속을 사용할 수 있고, 상기 오믹금속층으로는 Cr, Au를 사용할 수 있다.

<72> 도 5c를 참조하면, 브리지 공정 또는 스탭 커버 등의 공정을 통해 인접한 발광 셀 간의 N형 반도체층(20)과 P형 반도체층(40)을 연결한다.

<73> 또한 발광 소자에 외부 전압을 인가하기 위해 일 가장자리에 위치한 발광 셀의 P형 반도체층(40)에 P형 본딩 패드(50)를 형성하고, 다른 일 가장자리에 위치한 발광 셀의 노출된 N형 반도체층(20) 상에 N형 본딩패드(55)를 형성한다.

<74> 상술한 본 발명의 발광 소자의 제조 공정은 일 실시예일뿐 이에 한정되지 않고, 다양한 변형과 다양한 물질막이 더 추가될 수 있다. 예를 들어 발광 소자의 열 방출 특성을 향상시키기 위해 상기 기판의 배면을 소정 두께 제거한 후에 Al, Ti, Ag, W, Ta, Ni, Ru 또는 그 합금을 기판의 배면에 증착시킬 수 있다.

<75> 또한, 도 5a에 도시한 바와 같이 측면이 다양한 기울기를 갖도록 식각하여 다수개의 발광 셀을 분리한 다음, N형 반도체층(20)을 노출시키기 위해 식각하는 경우에도 마찬가지의 식각 공정을 사용하여 발광 소자를 제조할 수 있다. 즉, 5d에 도시한 바와 같이 N형 반도체층(20)이 노출되도록 식각되는 P형 반도체층(40)과 활성층(30)의 측면이 다양한 기울기를 갖도록 형성할 수 있다. 이러한 발광 소자는 종래 수직으로 식각된 표면에서 반사되었던 광자가 다양한 각의 표면에 의해 반사되지 않고 외부로 빠져나가기 때문에 더욱 향상된 발광 효율을 얻을 수 있다.

<76> 이로써 P형 반도체층(40), 활성층(30), N형 반도체층(20)의 전체 측면이 수평면으로부터 수직이 아닌, 소정의 기울기를 갖는 발광 셀이 다수개 연결되어 형성된 발광 소자를 제조할 수 있다.

<77> 도 6a 및 도 6b는 각각 종래 기술과 본 발명에 따른 발광 소자의 효과를 설명하기 위한 개념 단면도이다.

<78> 발광 소자의 광효율은 내부 양자 효율과 외부 양자 효율로 나타낼 수 있는데, 내부 양자 효율은 활성층의 설계나 품질에 따라서 결정된다. 외부 양자 효율의 경우 활성층에서 생성되는 광자가 발광 소자의 외부로 나오는 정도에 따라서

결정된다. 종래 기술에 따른 발광 소자를 도시한 도 6a를 살펴보면, 반도체층의 측면이 수평면으로부터 수직으로 형성되는 경우에, 일부의 광자가 반도체층의 측면에서 투과하지 못하고 반사되어 나오며, 전반사된 광은 외부로 투과하지 못하고 발광 소자 내부에서 소멸된다. 그러나, 본 발명에 따른 발광 소자를 도시한 도 6b에서와 같이 반도체층의 측면을 수평면으로부터 수직이 아닌, 소정의 기울기를 갖는 경우에, 경사진 측면이 광의 임계각을 변화시켜 보다 용이하게 광을 추출할 수 있게 돕는다. 따라서 활성층에서 발생한 광이 전반사되지 않고 발광 소자의 외부로 방출될 확률이 높아져 외부 양자 효율이 현저하게 향상된다.

【발명의 효과】

<79> 본 발명에 의한 발광 소자 및 이의 제조 방법은 수평면으로부터 수직이 아닌 소정의 기울기를 갖는 반도체층의 측면에서 발생한 광이 전반사되지 않고 발광 소자의 외부로 방출됨으로써, 더욱 향상된 광추출 효율, 외부 양자 효율, 발광 효율 등의 특성을 얻을 수 있다. 또한, 본 발명의 발광 소자는 고광도, 고휘도의 광을 발광하는 것으로, 우수한 광특성이 요구되는 다양한 제품 분야에 응용될 수 있다는 장점이 있다.

EX1012, Page 155

【특허청구범위】

【청구항 1】

기판;

상기 기판 상에 형성된 N형 반도체층; 및

상기 N형 반도체층 상에 형성된 P형 반도체층을 포함하고,

상기 N형 반도체층 또는 P형 반도체층을 포함하는 측면이 수평면으로부터 20 내지 80° 의 기울기를 갖는 것을 특징으로 하는 발광 소자.

【청구항 2】

기판 상에 N형 반도체층, 상기 N형 반도체층의 일부에 형성된 P형 반도체층을 포함하는 발광 셀을 다수개 포함하고,

상기 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층이 연결되고, 상기 발광 셀의 N형 반도체층 또는 P형 반도체층을 포함하는 측면이 수평면으로부터 20 내지 80° 의 기울기를 갖는 것을 특징으로 하는 발광 소자.

【청구항 3】

청구항 2에 있어서,

상기 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층을 연결하기 위한 배선을 더 포함하는 것을 특징으로 하는 발광 소자.

【청구항 4】

청구항 1 내지 청구항 3 중 어느 한 항에 있어서,

상기 P형 반도체층 상에 투명 전극층을 더 포함하는 것을 특징으로 하는 발광 소자.

【청구항 5】

청구항 1 내지 청구항 3 중 어느 한 항에 있어서,

상기 P형 반도체층과 상기 N형 반도체층 상에 Cr 또는 Au를 포함한 P형 오믹 금속층과 N형 오믹금속층을 각각 더 포함하는 것을 특징으로 하는 발광 소자.

【청구항 6】

기판 상에 N형 반도체층, P형 반도체층을 순차적으로 형성하는 단계;

상기 P형 반도체층 상에 측면이 수평면으로부터 수직이 아닌 소정의 기울기를 갖는 식각 마스크 패턴을 형성하는 단계;

상기 식각 마스크 패턴에 의해 노출된 P형 반도체층과, 상기 식각 마스크 패턴을 제거하는 단계를 포함하는 발광 소자의 제조 방법.

【청구항 7】

청구항 6에 있어서,

상기 식각 마스크 패턴을 형성하는 단계는,

3 내지 50㎛ 두께의 감광막을 이용하는 것을 특징으로 하는 발광 소자의 제조 방법.

【청구항 8】

청구항 7에 있어서,

상기 식각 마스크 패턴을 형성하는 단계는,

상기 P형 반도체층 상에 상기 감광막을 도포하는 단계;

소정의 마스크 패턴에 따라 상기 감광막을 노광하는 단계;

상기 노광 후 베이킹 공정 없이 현상하는 단계를 포함하는 것을 특징으로 하는 발광 소자의 제조 방법.

【청구항 9】

청구항 7에 있어서,

상기 식각 마스크 패턴을 형성하는 단계는,

상기 P형 반도체층 상에 상기 감광막을 도포하는 단계;

소정의 마스크 패턴에 따라 상기 감광막을 노광하는 단계;

100℃ 내지 140℃의 온도에서 하드 베이킹을 하는 단계 및

현상하는 단계를 포함하는 것을 특징으로 하는 발광 소자의 제조 방법.

【청구항 10】

청구항 6 내지 청구항 9 중 어느 한 항에 있어서,

상기 P형 반도체층의 제거로 인해 노출된 N형 반도체층의 일부를 제거하여 다수개의 발광 셀을 형성하는 단계; 및

브리지 배선을 통해 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광

셀의 P형 반도체층을 연결하는 단계를 더 포함하는 것을 특징으로 하는 발광 소자의 제조 방법.

【청구항 11】

청구항 10에 있어서,

상기 브리지 배선은 브리지(Bridge) 공정 또는 스탭 커버(Step Cover) 공정을 통해 일 발광 셀의 N형 반도체층과 인접한 다른 일 발광 셀의 P형 반도체층을 연결하는 것을 특징으로 하는 발광 소자의 제조 방법.

【청구항 12】

청구항 6 내지 청구항 9 중 어느 한 항에 있어서,

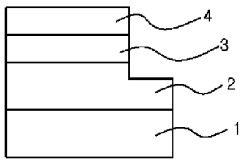
상기 P형 반도체층과 상기 식각 마스크 패턴을 제거하는 단계 이후에,

상기 기판의 배면을 소정 두께 제거하는 단계; 및

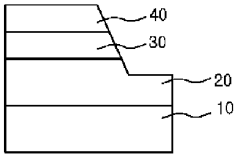
상기 기판의 배면에 Al, Ti, Ag, W, Ta, Ni, Ru 또는 그 합금을 증착하는 단계를 더 포함하는 것을 특징으로 하는 발광 소자의 제조 방법.

【도면】

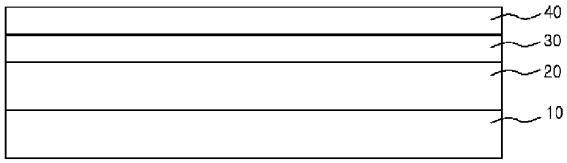
【도 1】



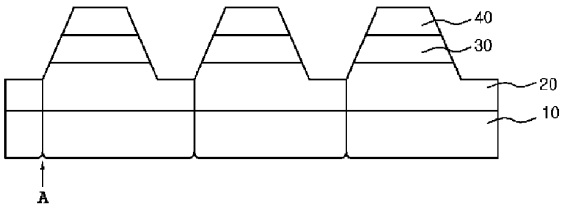
【도 2】



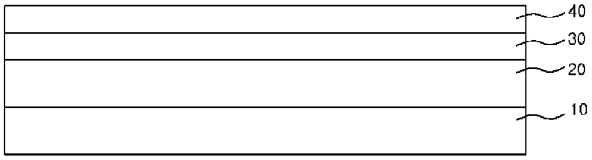
【도 3a】



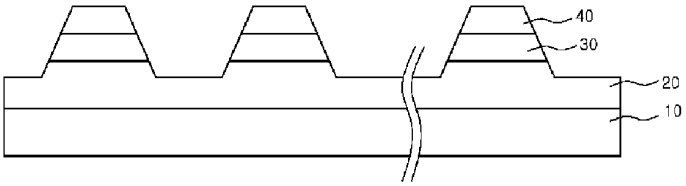
【도 3b】



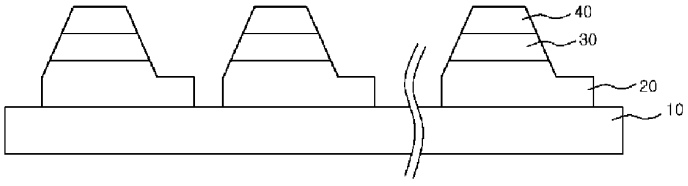
【도 4a】



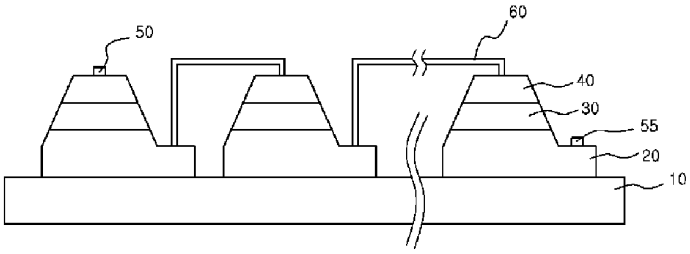
【도 4b】



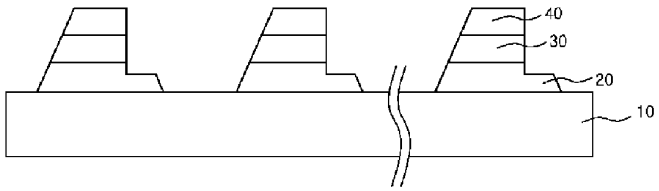
【도 4c】



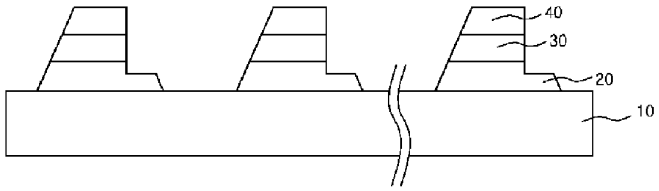
【도 4d】



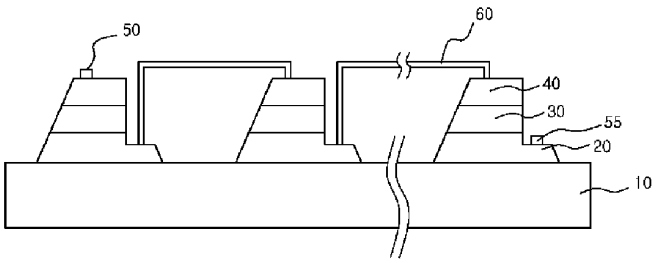
【도 5a】



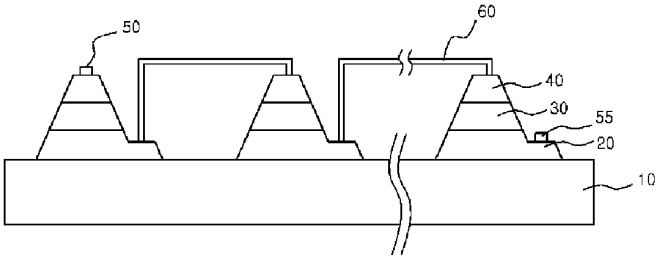
【도 5b】



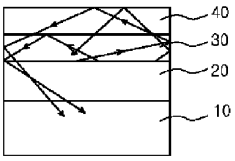
【도 5c】



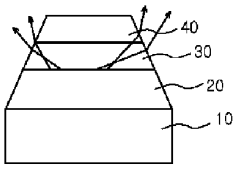
【도 5d】



【도 6a】



【도 6b】



대 한 민 국 특 허 청
KOREAN INTELLECTUAL PROPERTY OFFICE

별첨 사본은 아래 출원의 원본과 동일함을 증명함.

This is to certify that the following application annexed hereto is a true copy from the records of the Korean Intellectual Property Office.

출 원 번 호 : 10-2005-0055179
Application Number

출 원 년 월 일 : 2005년 06월 24일
Filing Date JUN. 24, 2005

출 원 인 : 서울옵토디바이스주식회사
Applicant(s) SEOUL OPTO DEVICE CO., LTD.

2009년 11월 23일

특 허 청
COMMISSIONER

【서지사항】

【서류명】 특허출원서

【권리구분】 특허

【수신처】 특허청장

【제출일자】 2005.06.24

【발명의 국문명칭】 복수 셀의 단일 발광 소자 및 이의 제조 방법

【발명의 영문명칭】 Light-emitting device having arrayed cells and Method of manufacturing the same

【출원인】

【명칭】 서울옵토디바이스 주식회사

【출원인코드】 1-2003-032642-0

【대리인】

【성명】 남승희

【대리인코드】 9-2003-000036-2

【포괄위임등록번호】 2004-031626-3

【발명자】

【성명】 이종람

【성명의 영문표기】 LEE,Jong Lam

【주민등록번호】 580406-1XXXXXX

【우편번호】 790-834

【주소】 경북 포항시 남구 지곡동 756 교수숙소 E-1401

【국적】 KR

【발명자】

【성명】 이재호

【성명의 영문표기】 LEE,Jae Ho

【주민등록번호】 610216-1XXXXXX

【우편번호】 449-531

【주소】 경기 용인시 성복동 LG3차빌리지 309-1405

【국적】 KR

【발명자】

【성명】 윤여진

【성명의 영문표기】 YOON,Yeo Jin

【주민등록번호】 720715-1XXXXXX

【우편번호】 426-738

【주소】 경기 안산시 상록구 사1동 숲속마을아파트 101-1505

【국적】 KR

【발명자】

【성명】 황의진

【성명의 영문표기】 HWANG,Eu Jin

【주민등록번호】 751018-1XXXXXX

【우편번호】 429-450

【주소】 경기 시흥시 정왕동 1569-7 303호

【국적】 KR

【심사청구】 청구

【취지】 특허법 제42조의 규정에 의한 출원, 특허법 제60조의 규정에 의한 출원심사를 청구합니다.

대리인 남승희 (인)

【수수료】

【기본출원료】 0 면 38,000 원

【가산출원료】 28 면 0 원

【우선권주장료】 0 건 0 원

【심사청구료】	10 항 429,000 원
【합계】	467,000 원
【감면사유】	중소기업
【감면후 수수료】	233,500 원
【첨부서류】	1.중소기업기본법시행령 제2조에의한 중소기업에 해당함을 증명하는 서류[사업자등록증및 원천징수이행상황신고서]_1통

【요약서】

【요약】

본 발명은 N형 반도체층과 상기 N형 반도체층 상에 형성된 P형 반도체층을 포함하는 다수개의 발광 셀이 형성된 기판 및 상기 기판이 플립칩 본딩되는 서브마운트 기판을 포함하고, 상기 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층이 연결되고, 상기 발광 셀의 적어도 P형 반도체층을 포함하는 측면이 수평면으로부터 수직이 아닌 소정의 기울기를 갖는 것을 특징으로 하는 복수 셀의 단일 발광 소자 및 이의 제조 방법를 제공한다. 본 발명에 의한 발광 소자 및 이의 제조 방법은 발광 효율, 외부 양자 효율, 추출 효율 등의 특성을 향상시키고 신뢰성을 확보하여, 고광도, 고휘도의 광을 발광할 수 있는 장점이 있다.

【대표도】

도 2

【색인어】

플립칩, 발광 소자, LED, 광추출 효율, 발광 효율, 광도

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【명세서】

【발명의 명칭】

복수 셀의 단일 발광 소자 및 이의 제조 방법 {Light-emitting device having arrayed cells and Method of manufacturing the same}

【도면의 간단한 설명】

<1> 도 1은 종래의 플립칩 구조의 발광 소자를 도시한 단면도.

<2> 도 2는 본 발명의 발광 소자를 설명하기 위한 개념 단면도.

<3> 도 3a 내지 도 3e는 본 발명에 따른 제 1 실시예의 제조 공정을 설명하기 위한 단면도.

<4> 도 4a 내지 도 4d는 본 발명에 따른 제 2 실시예의 제조 공정을 설명하기 위한 단면도.

<5> 도 5는 본 발명에 따른 제 3 실시예를 도시한 단면도.

<6> <도면의 주요 부분에 대한 부호의 설명>

<7> 10 : 기판 20 : N형 반도체층

<8> 30 : 활성층 40 : P형 반도체층

<9> 50 : N형 금속범프 55 : P형 금속범프

<10> 60 : 배선 100 : 서브 마운트 기판

<11> 110 : N형 본딩패드 115 : P형 본딩패드

<12> 120 : 본딩층

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【발명의 상세한 설명】

【발명의 목적】

【발명이 속하는 기술분야 및 그 분야의 종래기술】

<13> 본 발명은 복수 셀의 단일 발광 소자 및 이의 제조 방법에 관한 것으로, 보다 상세하게는 플립칩(Flip-Chip) 구조의 발광 소자에 있어서 발광 효율과 휘도를 향상시키기 위한 복수 셀의 단일 발광 소자 및 이의 제조 방법에 관한 것이다.

<14> 발광 소자(light emission diode; LED)는 반도체의 p-n 접합 구조를 이용하여 주입된 소수 캐리어(전자 또는 정공)를 만들고 이들의 재결합에 의하여 소정의 빛을 발산하는 소자를 지칭하며, GaAs, AlGaAs, GaN, InGaN, AlGaInP 등의 화합물 반도체(compound semiconductor) 재료의 변경을 통해 발광원을 구성함으로써 다양한 색을 구현할 수 있다. 예를 들어 GaAsP 등을 이용하여 적색 발광 소자를 형성할 수 있고, GaP, InGaN 등을 이용하여 녹색 발광 소자를 형성할 수 있고, InGaN/GaN 더블 헤테로(double hetero) 구조를 이용하여 청색 발광 소자를 형성할 수 있고, AlGaN/GaN 또는 AlGaN/AlGaN 구조를 이용하여 UV 발광 소자를 형성할 수 있다.

<15> 특히, GaN은 상온에서 3.4eV의 직접 천이형 밴드갭(direct bandgap)을 가지며 질화인듐(InN), 질화알루미늄(AlN) 같은 물질과 조합하여 1.9eV (InN)에서 3.4eV (GaN), 6.2eV (AlN)까지 직접 에너지 밴드갭을 가지고 있어서 가시광에서부터 자외선 영역까지 넓은 파장 영역 때문에 광소자의 응용 가능성이 매우 큰 물질이다. 이처럼 파장 조절이 가능하여 단파장 영역의 적색, 녹색 및 청색 발광 소자

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에 의한 천연색(full-color) 구현이 가능해짐으로써 디스플레이 영역은 물론 일반 조명 시장으로의 파급 효과가 매우 커질 것으로 예상된다.

<16> 발광 소자는 기존의 전구 또는 형광등에 비해 소모 전력이 작고 수명이 길며, 협소한 공간에 설치 가능하고 진동에 강한 특성을 보인다. 이러한 발광 소자는 표시 소자 및 백라이트로 이용되고 있으며, 소모 전력의 절감과 내구성 측면에서 우수한 특성을 갖기 때문에 최근 일반 조명 용도로 이를 적용하기 위해 활발한 연구가 진행중이다. 이후, 대형 LCD-TV 백라이트, 자동차 헤드라이트, 일반 조명에까지 응용이 확대될 것으로 예상되며, 이를 위해서는 발광 소자의 발광 효율의 개선이 필요하고, 열방출 문제를 해결하여야 하며, 발광 소자의 고휘도화, 고출력화를 달성하여야 한다.

<17> 이러한 문제를 해결하기 위해 최근에 플립칩 형태의 발광 소자에 대한 관심이 날로 높아지고 있다.

<18> 도 1은 종래의 플립칩 구조의 발광 소자를 설명하기 위한 개념 단면도이다.

<19> 도 1을 참조하면, 소정의 기판(1) 상에 N형 반도체층(5), 활성층(6), P형 반도체층(7)을 순차적으로 형성한다. P형 반도체층(7)과 활성층(6)의 일부를 식각함으로써 N형 반도체층(5)을 노출시켜 발광 셀을 형성한다. 또한, 별도의 서브 마운트 기판(2)을 준비하여 제 1 및 제 2 전극(3, 4)을 형성하고, 제 1 전극(3) 상에는 P형 솔더(8)를 형성하고, 제 2 전극(4) 상에는 N형 솔더(9)를 형성한다. 이후, 상기 발광 셀을 상기 서브 마운트 기판(2)에 본딩하되, 발광 셀의 P 전극을 P형 솔더(8)에, N 전극을 N형 솔더(9)에 본딩한다. 발광 셀이 본딩된 기판을 봉지하는 몰딩

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부(미도시)를 형성하여 발광 소자를 제작한다.

<20> 이와 같은 종래 플립칩 구조의 발광 소자는 기존의 발광 소자에 비해서 열 방출 효율이 높고, 광의 차폐가 거의 없어 광효율이 기존의 발광 소자에 비해 50% 이상 증가하는 효과가 있고, 발광 소자의 구동을 위한 금선이 필요하지 않기 때문에 여러 소형 패키지에도 많은 응용을 고려하고 있다.

<21> 발광 소자의 발광층에서 생성된 광은 칩의 모든 면으로부터 방출되고, 광추출 효율은 일반적으로 광의 임계각에 의하여 결정된다. 발광 소자의 성능을 나타내는 지표는 발광 효율(lm/W), 내부 양자 효율(%), 외부 양자 효율(%), 추출 효율(%) 등 여러 가지가 있는데, 추출 효율은 발광 소자에 주입된 전자와 발광 소자 밖으로 방출되는 광자의 비에 의하여 결정되며 추출 효율이 높을수록 발광 소자가 밝은 것을 의미한다. 그러나 종래 발광 소자는 N형 반도체층을 노출시키기 위해 식각할 때, P형 반도체층과 활성층의 측면이 수직 가공되어 발광 소자의 내부에서 생성된 광자의 일부가 수평면으로부터 수직으로 가공된 식각면에서 전반사된다. 그리하여 전반사되는 상당량의 광은 내부 반사에 의하여 밖으로 방출되지 못한채 발광 소자 내부에서 소멸된다. 즉, 전기 에너지가 빛 에너지로 변환되어 소자의 외부로 빠져나오는 발광 효율이 낮은 문제점이 있다.

【발명이 이루고자 하는 기술적 과제】

<22> 본 발명은 상술한 문제점을 해결하기 위한 것으로, 플립칩 구조의 발광 소자에 있어서 발광 효율, 외부 양자 효율, 추출 효율 등의 특성을 향상시키고 신뢰성

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을 확보하여, 고광도, 고휘도의 광을 발광할 수 있는 복수 셀의 단일 발광 소자 및 이의 제조 방법을 제공하는 것을 목적으로 한다.

【발명의 구성】

<23> 상술한 목적을 달성하기 위하여, 본 발명은 N형 반도체층과 상기 N형 반도체층 상에 형성된 P형 반도체층을 포함하는 다수개의 발광 셀이 형성된 기판 및 상기 기판이 플립칩 본딩되는 서브 마운트 기판을 포함하고, 상기 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층이 연결되고, 상기 발광 셀의 적어도 P형 반도체층을 포함하는 측면이 수평면으로부터 수직이 아닌 소정의 기울기를 갖는 것을 특징으로 하는 복수 셀의 단일 발광 소자를 제공한다. 상기 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층을 연결하기 위한 배선을 더 포함할 수 있다. 상기 소정의 기울기는 20 내지 80° 일 수 있다.

<24> 본 발명은 기판 상에 N형 반도체층과 P형 반도체층을 순차적으로 형성하여 상기 기판 상에 발광 셀을 형성하는 단계, 상기 P형 반도체층 상에 측면이 수평면으로부터 수직이 아닌 소정의 기울기를 갖는 식각 마스크 패턴을 형성하는 단계, 상기 식각 마스크 패턴에 의해 노출된 P형 반도체층과 상기 식각 마스크 패턴을 제거하는 단계 및 상기 기판을 별도의 서브 마운트 기판에 플립칩 본딩하는 단계를 포함하는 발광 소자의 제조 방법을 제공한다.

<25> 상기 기판 상에 발광 셀을 형성하는 단계는 상기 N형 반도체층 및 P형 반도

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체층의 일부를 제거하여 다수개의 발광 셀을 형성하는 단계를 포함할 수 있고, 상기 P형 반도체층과 상기 식각 마스크 패턴을 제거하는 단계 이후에, 브리지 배선을 통해 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층을 연결하는 단계를 더 포함할 수 있다. 상기 다수개의 발광 셀을 형성하는 단계는, 상기 P형 반도체층 상에 측면이 수평면으로부터 수직이 아닌 소정의 기울기를 갖는 식각 마스크 패턴을 형성하는 단계, 상기 식각 마스크 패턴에 의해 노출된 P형 반도체층 및 N형 반도체층을 제거하여 다수개의 발광 셀을 형성하는 단계 및 상기 식각 마스크 패턴을 제거하는 단계를 포함할 수 있다. 상기 브리지 배선은 브리지(Bridge) 공정 또는 스탭 커버(Step Cover) 공정을 통해 일 발광 셀의 N형 반도체층과 인접한 다른 일 발광 셀의 P형 반도체층을 연결할 수 있다.

<26> 상기 식각 마스크 패턴을 형성하는 단계는, 3 내지 50㎛ 두께의 감광막을 이용하는 것을 특징으로 할 수 있다.

<27> 상기 식각 마스크 패턴을 형성하는 단계는, 상기 P형 반도체층 상에 상기 감광막을 도포하는 단계, 소정의 마스크 패턴에 따라 상기 감광막을 노광시키는 단계 및 상기 노광 후 베이킹 공정 없이 현상하는 단계를 포함할 수 있다.

<28> 또한, 상기 식각 마스크 패턴을 형성하는 단계는, 상기 P형 반도체층 상에 상기 감광막을 도포하는 단계, 소정의 마스크 패턴에 따라 상기 감광막을 노광시키는 단계, 100℃ 내지 140℃의 온도에서 하드 베이킹을 하는 단계 및 현상하는 단계를 포함할 수 있다.

<29> 이하, 첨부된 도면을 참조하여 본 발명에 의한 발광 소자 및 이의 제조 방법에 대하여 상세히 설명하기로 한다. 그러나 본 발명은 이하에서 개시되는 실시예에 한정되는 것이 아니라 서로 다른 다양한 형태로 구현될 것이며, 단지 본 실시예는 본 발명의 개시가 완전하도록 하며, 통상의 지식을 가진 자에게 발명의 범주를 완전하게 알려주기 위해 제공되는 것이다.

<30> 도 2는 본 발명의 발광 소자를 설명하기 위한 개념 단면도이다.

<31> 도면을 참조하면, 베이스 기판(10) 상에 순차적으로 형성된 발광층, 즉 N형 반도체층(20), 활성층(30) 및 P형 반도체층(40)을 포함하고, 금속범프(50, 55)를 이용하여 상기 발광층이 형성된 베이스 기판(10)과 플립칩 본딩되는 서브 마운트 기판(100)을 포함한다. 상기 P형 반도체층(40), 활성층(30) 및 N형 반도체층(20)을 포함하는 발광층의 측면은 수평면으로부터 20 내지 80° 의 기울기를 갖고, 이러한 측면으로부터 광의 임계각을 변화시키고 용이하게 광을 추출할 수 있어 발광 소자의 발광 효율을 개선할 수 있다.

<32> 도 3a 내지 도 3e는 본 발명에 따른 제 1 실시예의 제조 공정을 설명하기 위한 단면도들이다.

<33> 도 3a를 참조하면, 베이스 기판(10) 상에 N형 반도체층(20), 활성층(30) 및 P형 반도체층(40)을 순차적으로 형성한다.

<34> 베이스 기판(10)은 발광 소자를 제작하기 위한 통상의 웨이퍼를 지칭하는 것

으로, Al_2O_3, ZnO, $LiAl_2O_3$ 등의 투명 기판을 사용한다. 본 실시예에서는 사파이어로 구성된 투명한 결정 성장 기판을 사용한다.

<35> 상기 베이스 기판(10) 상에 결정 성장시 베이스 기판(10)과 후속층들의 격자 부정합을 줄이기 위한 버퍼층(미도시)을 더 형성할 수 있다. 버퍼층은 반도체 재료인 GaN 또는 AlN을 포함하여 형성할 수 있다.

<36> N형 반도체층(20)은 전자가 생성되는 층으로서, N형 불순물이 주입된 질화갈륨(GaN)을 사용하는 것이 바람직하고, 이에 한정되지 않고 다양한 반도체 성질의 물질층이 가능하다. 본 실시예에서는 N형 $Al_xGa_{1-x}N(0\leq x\leq 1)$을 포함하는 N형 반도체층(20)을 형성한다. 또한, P형 반도체층(40)은 정공이 생성되는 층으로서, P형 불순물이 주입된 질화갈륨(GaN)을 사용하는 것이 바람직하고, 이에 한정되지 않고 다양한 반도체 성질의 물질층이 가능하다. 본 실시예에서는 P형 $Al_xGa_{1-x}N(0\leq x\leq 1)$을 포함하는 P형 반도체층(40)을 형성한다. 뿐만 아니라 상기 반도체층으로 InGaN을 사용할 수 있다. 또한 상기의 N형 반도체층(20) 및 P형 반도체층(40)은 다층막으로 형성할 수도 있다.

<37> 활성층(30)은 소정의 밴드 갭을 가지며 양자 우물이 만들어져 전자 및 정공이 재결합되는 영역으로서, InGaN을 포함하여 이루어질 수 있다. 활성층(30)을 이루는 물질의 종류에 따라 전자 및 전공이 결합하여 발생하는 발광 파장이 변화된다. 따라서, 목표로 하는 파장에 따라 활성층(30)에 포함되는 반도체 재료를 조절하는 것이 바람직하다.

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<38> 상술한 물질층들은 유기금속 화학 증착법(MOCVD; Metal Organic Chemical Vapor Deposition), 화학 증착법(CVD; Chemical Vapor Deposition), 플라즈마 화학 증착법(PCVD; Plasma-enhanced Chemical Vapor Deposition), 분자선 성장법(MBE; Molecular Beam Epitaxy), 수소화물 기상 성장법(HVPE; Hydride Vapor Phase Epitaxy) 등을 포함한 다양한 증착 및 성장 방법을 통해 형성된다.

<39> 이후, 소정의 식각 공정을 통해 P형 반도체층(40) 및 활성층(30)의 일부를 제거하여 N형 반도체층(20)의 일부를 노출시킨다. P형 반도체층(40) 상에 식각 마스크 패턴을 형성한 다음, 건식 또는 습식 식각 공정을 실시하여 P형 반도체층(40) 및 활성층(30)을 제거하여 N형 반도체층(20)을 노출시킨다.

<40> 일반적으로 상기 식각 공정을 위하여 P형 반도체층(40) 상면에 1 내지 2㎛ 두께로 감광막(photoresist)을 도포한 후, 80 내지 90℃의 온도에서 소프트 베이킹(soft baking)을 한다. 다음으로, 소정의 포토 마스크(photo mask)를 통해 자외선(UV) 영역의 빛을 조사하여 마스크 상에 형성된 패턴을 도포된 감광막에 전사하는 노광(exposure) 공정을 진행한다. 이후, 100 내지 120℃의 온도에서 하드 베이킹(hard baking)을 하고, 노광 공정을 통해 상대적으로 결합이 약해져 있는 부분의 감광막을 용제를 사용하여 녹여내는 현상(developing) 공정을 진행한다. 이러한 과정을 통해 상기 P형 반도체층(40) 상에 소정의 식각 마스크 패턴이 형성된다.

<41> 그러나 본 실시예는 상기 식각 마스크 패턴을 형성할 때, 3 내지 50㎛ 두께로 감광막을 종래에 비해 두껍게 도포하고 소프트 베이킹을 거쳐 노광 공정을 실시한다. 그 다음에 하드 베이킹을 통하지 않고 바로 현상하면, 남아있는 감광막의 현

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상된 측면은 수평면으로부터 80° 정도의 기울기를 갖는 경사진 면을 형성하게 된다. 이어서, 이러한 측면의 기울기를 갖는 식각 마스크 패턴을 사용하여 노출된 영역의 P형 반도체층(40) 및 활성층(30)을 식각하면, 식각된 P형 반도체층(40) 및 활성층(30)의 측면은 마찬가지로 수평면으로부터 80° 정도의 기울기를 갖는 경사진 면을 얻을 수 있다.

<42> 즉, 도 3a의 P형 반도체층(40) 상에 3 내지 50㎛ 두께로 감광막을 두껍게 도포하여 노광 후 하드 베이킹 없이 바로 현상한 식각 마스크 패턴을 형성한다. 상기 식각 마스크 패턴에 의해 노출된 P형 반도체층(40) 및 활성층(30)을 유도 결합 플라즈마(ICP; Inductive Coupled Plasma) 또는 건식 식각 공정을 통해 제거하여 N형 반도체층(20)을 노출시킨다. 노출된 N형 반도체층(20)의 일부를 더 제거할 수도 있다. 이후, 식각 마스크 패턴을 제거하면, 도 3b에 도시한 바와 같이 P형 반도체층(40), 활성층(30)의 측면이 수평면으로부터 수직(90°)이 아닌, 소정의 기울기를 갖는 발광 소자를 제조할 수 있다.

<43> 또한, 도 3a의 P형 반도체층(40) 상에 3 내지 50㎛ 두께로 감광막을 두껍게 도포하여 노광 후 하드 베이킹을 실시하는 경우에, 하드 베이킹 온도를 100℃ 내지 140℃로 하여 진행하고 현상을 하게 되면, 현상된 감광막의 측면이 수평면으로부터 80° 에서 20° 까지의 기울기를 갖도록 식각된 측면을 얻을 수 있다. 예를 들어, 100℃의 온도에서 하드 베이킹을 하는 경우에 수평면으로부터 80° 정도의 기울기를 갖는 식각 마스크 패턴을 얻을 수 있으며, 이를 이용하여 P형 반도체층(40) 및 활성층(30)의 측면이 수평면으로부터 80° 정도의 기울기를 갖도록 할 수 있다. 또

한, 140℃의 온도에서 하드 베이킹을 하는 경우에 수평면으로부터 20° 정도의 기울기를 갖는 식각 마스크 패턴을 얻을 수 있으며, 이를 이용하여 P형 반도체층(40) 및 활성층(30)의 측면이 수평면으로부터 20° 정도의 기울기를 갖도록 할 수 있다.

<44> 이와 같이 3 내지 50㎛ 두께의 감광막을 노광 후 100℃ 내지 140℃의 온도에서 하드 베이킹을 하고 현상한 식각 마스크 패턴을 사용함으로써, P형 반도체층(40) 및 활성층(30)의 측면이 마찬가지로 수평면으로부터 80° 에서 20° 까지의 기울기를 갖도록 식각된 측면을 얻을 수 있다. 그리하여 발광층의 내부에서 생성된 광은 다양한 기울기를 갖도록 식각된 측면에 전반사되지 않고 발광 소자의 외부로 빠져나가게 된다.

<45> 상기 P형 반도체층(40) 상부에 광의 반사를 위한 반사층을 더 형성할 수 있으며, P형 반도체층(40) 또는 노출된 N형 반도체층(20) 상부에 전류의 공급을 원활히 하기 위한 별도의 오믹금속층을 더 형성할 수도 있다. 상기 오믹금속층으로는 Cr, Au를 사용할 수 있다.

<46> 또한, 도 3c에 도시한 바와 같이 P형 반도체층(40) 상에 P형 금속범프(55, metal bumper)와, N형 반도체층(20) 상에 N형 금속범프(50)를 범핑용으로 형성한다. P형 및 N형 금속범프(55, 50)로는 Pb, Sn, Au, Ge, Cu, Bi, Cd, Zn, Ag, Ni 및 Ti 중 적어도 어느 하나를 사용할 수 있고, 이들의 합금을 사용할 수 있다. 이를 위해, 전체 구조 상에 감광막을 도포한 다음, 소정의 마스크를 이용한 사진식각 공정을 실시하여 P형 반도체층(40)과 N형 반도체층(20)의 일부를 노출시킨 감광막 패턴(미도시)을 형성한다. 전체 구조상에 금속막을 증착한 다음, 상기 감광막

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패턴에 의해 노출된 P형 반도체층(40) 상부에 형성된 금속막과, N형 반도체층(30)의 상부에 형성된 금속막을 제외한 나머지 영역의 금속막 및 상기 감광막 패턴을 제거한다. 이로써, P형 반도체층(40) 상에는 P형 금속범프(55)가 형성되고, N형 반도체층(20) 상에는 N형 금속범프(50)가 형성된다.

<47> 다음으로, 도 3d를 참조하면 별도의 서브 마운트 기판(100)을 마련하여 상기 P형 금속범프(55) 및 N형 금속범프(50)와 각각 접속될 P형 본딩패드(115) 및 N형 본딩패드(110)를 형성한다.

<48> 이 때 서브 마운트 기판(100)으로는 열전도성이 우수한 다양한 기판(100)을 사용한다. 즉, SiC, Si, Ge, SiGe, AlN, 금속 등을 사용한다. 본 실시예는 열전도성이 우수하며 절연 성질을 갖는 AlN을 사용한다. 물론 이에 한정되지 않고, 열전도율이 크며 전기 전도성이 우수한 물질인 금속성 물질을 사용할 수 있다. 이 경우에는 기판(100) 상에 절연막 또는 유전체막을 형성하여 충분한 절연 역할을 하도록 한다. 유전체막으로 SiO_2, MgO 및 SiN 또는 절연성 물질을 사용할 수 있다. 또한, 상기 N형 본딩 패드(110) 및 P형 본딩 패드(115)는 전기 전도성이 우수한 금속을 사용한다. 이는 스크린 인쇄 방법으로 형성하거나, 소정의 마스크 패턴을 이용한 증착 공정을 통해 형성한다.

<49> 이후, 상기 서브 마운트 기판(100)과, 상기 발광층이 형성된 베이스 기판(10)을 플립칩 본딩한다.

<50> 도 3e를 참조하면, 본 발명의 발광 소자는 발광층의 상부에 형성된 N형 및 P

형 금속범프(50, 55)와 서브 마운트 기판(100)의 N형 및 P형 본딩패드(110, 115)가 접속되도록 본딩된다.

<51> 이 때, 열 또는 초음파(ultrasonic)를 이용하거나, 열과 초음파를 동시에 사용하여 본딩할 수 있다. 금속범프(50, 55)와 하부 본딩 패드(110, 115)와의 접속은 다양한 본딩 방법을 통해 본딩된다.

<52> 이뿐 아니라, 발광층의 상부에 N형 및 P형 금속범프(50, 55)가 형성되지 않고, 서브 마운트 기판(100) 상에 각각의 금속범프가 형성될 수도 있다.

<53> 도면에서 볼 수 있듯이, 다수 개의 발광 소자를 하나의 기판(20) 상에 제작할 수 있고, 이러한 경우 추후에 각각의 발광 소자로 절단하여 사용하게 된다. 이 때, 도 3e의 (A) 부분은 이러한 다수 개의 발광 소자를 개별적으로 절단하기 위한 절단부이다.

<54> 이로써 P형 반도체층(40), 활성층(30), N형 반도체층(20) 측면의 일부가 수평면으로부터 수직이 아닌, 소정의 기울기를 갖는 플립칩 구조의 발광 소자를 제조할 수 있다.

<55> 상술한 본 발명의 발광 소자의 제조 공정은 일 실시예일뿐 이에 한정되지 않고, 다양한 공정과 제조 방법이 소자의 특성 및 공정의 편의에 따라 변경되거나 추가될 수 있다.

<56> 예를 들어, 상기와 동일한 공정에 있어서 도 3a와 같이 N형 반도체층, 활성층, P형 반도체층이 순차적으로 형성된 베이스 기판을 마련하고, 먼저 기판이 노출

되도록 상기 P형 반도체층, 활성층, N형 반도체층의 일부를 제거하여 다수 개의 발광 소자를 개별 분리할 수 있다. 이 때 상술한 공정을 통하여 식각되는 P형 반도체층, 활성층, N형 반도체층 측면을 수평면으로부터 수직이 아닌, 소정의 기울기를 갖도록 형성할 수도 있다.

<57> 상술한 바와 같이 본 발명은 플립칩 구조의 발광 소자에 있어서, 발광층의 일부 측면이 수평면으로부터 수직이 아닌, 소정의 기울기를 갖도록 형성함으로써, 종래의 발광 소자에 비하여 발광 효율을 향상시킬 수 있다. 이는 종래의 평탄한 표면에서 반사되었던 광자가 다양한 각의 표면에 의해 반사되지 않고 외부로 빠져나가기 때문이다.

<58> 도 4a 내지 도 4d는 본 발명에 따른 제 2 실시예의 제조 공정을 설명하기 위한 단면도들이다.

<59> 이는 제 1 실시예의 경우와 거의 동일하며, 단지 제 2 실시예는 웨이퍼 레벨에서 다수의 발광 셀을 직렬, 병렬 또는 직병렬 연결하여 소자의 크기를 줄이고, 적정 전압 및 전류에 구동되도록 하여 조명용으로 사용가능하며 교류 전원에서도 구동할 수 있는 발광 소자를 제공한다. 상기 제 1 실시예의 경우와 중복되는 설명은 생략한다.

<60> 도 4a를 참조하면, 유기금속 화학 증착법, 화학 증착법, 플라즈마 화학 증착법, 분자선 성장법, 수소화물 기상 성장법 등의 다양한 증착 방법을 통해 베이스 기판(10) 상에 N형 반도체층(20), 활성층(30) 및 P형 반도체층(40)을 순차적으로 형성한다. 상기 베이스 기판(10) 상에 결정 성장시 기판(10)과 후속층들의 격자 부

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정합을 줄이기 위한 버퍼층을 더 형성할 수 있다.

<61> 이후, 상기 베이스 기판(10) 상에 순차적으로 형성된 N형 반도체층(20), 활성층(30) 및 P형 반도체층(40)의 일부를 제거하여 다수개의 발광 셀을 형성한다. 이를 위해, P형 반도체층(40) 상에 3 내지 50㎛ 두께로 감광막을 두껍게 도포하여 노광 후 하드 베이킹 없이 바로 현상하여 식각 마스크 패턴을 형성한다. 상기 식각 마스크 패턴에 의해 노출된 P형 반도체층(40), 활성층(30), 소정의 N형 반도체층(20)을 유도 결합 플라즈마 또는 건식 식각 공정을 통해 제거하여 발광 셀을 분리한다. 다음으로 식각 마스크 패턴을 제거하면, 도 4b에 도시한 바와 같이 식각된 P형 반도체층(40), 활성층(30), N형 반도체층(20)의 전측면이 수평면으로부터 80° 정도의 기울기를 갖는 경사진 면을 얻을 수 있다.

<62> 또한 P형 반도체층(40) 상에 3 내지 50㎛ 두께로 감광막을 두껍게 도포하여 노광 후 100℃ 내지 140℃의 온도에서 하드 베이킹을 하고 현상하여 식각 마스크 패턴을 형성한다. 이러한 식각 마스크 패턴에 의해 노출된 P형 반도체층(40), 활성층(30), N형 반도체층(20)을 식각한 후 식각 마스크 패턴을 제거하여 식각된 P형 반도체층(40) 및 활성층(30)의 측면이 80° 에서 20° 까지의 다양한 기울기를 갖도록 할 수도 있다.

<63> 다음으로, 도 4c에 도시한 바와 같이 소정의 식각 공정을 통해 P형 반도체층(40) 및 활성층(30)의 일부를 제거하여 N형 반도체층(20)의 일부를 노출시킨다. 소정의 브리지 배선을 통해 일 발광 셀의 노출된 N형 반도체층(20)과 인접한 타 발광 셀의 P형 반도체층(40)을 연결한다. 이 때 브리지 배선(60)은 도전성의 물질을 이

용하되, 금속을 이용하여 형성한다. 물론, 불순물로 도핑된 실리콘 화합물을 이용할 수도 있다. 상기 브리지 배선(60)은 브리지(Bridge) 공정 또는 스탭 커버(Step Cover) 등의 공정을 통해 형성된다.

<64> 상술한 브리지 공정은 에어브리지 공정이라고도 하며, 서로 연결할 칩 간에 포토 공정을 이용해 감광액을 도포하고 현상하여 감광막 패턴을 형성하고, 그 위에 금속 등의 물질을 진공 증착 등의 방법으로 먼저 박막으로 형성하고, 다시 그 위에 전기 도금(electroplating), 무전해 도금(electroplating) 또는 금속 증착 등의 방법으로 금을 포함하는 도전성 물질을 일정 두께로 도포한다. 이후, 솔벤트등의 용액으로 감광막 패턴을 제거하면 도전성 물질의 하부는 다 제거되고 브리지 형태의 도전성 물질만이 공간에 형성된다.

<65> 스탭 커버(Step Cover) 공정은 서로 연결할 칩 간에 포토 공정을 이용해 감광액을 도포하고, 현상하여 서로 연결될 부분만을 남기고 다른 부분은 감광막 패턴으로 뒤덮고, 그 위에 전기 도금, 무전해 도금 또는 금속 증착 등의 방법으로 금을 포함하는 도전성 물질을 일정 두께로 도포한다. 이어서, 솔벤트 등의 용액으로 감광막 패턴을 제거하면 도전성 물질이 덮인 이외의 부분은 다 제거되고 도전성 물질이 덮혀진 부분 만이 남아 연결할 칩 사이를 전기적으로 연결시키는 역할을 하게 되다.

<66> 또한 각 발광 셀의 상부에 범핑용으로 형성된 다수개의 금속범프를 형성하고, 일 가장자리에 위치한 발광 셀의 P형 반도체층(40)과 다른 일 가장자리에 위치한 발광 셀의 N형 반도체층(20) 상에 각각 P형 금속범프(55) 및 N형 금속범

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프(50)를 더 형성한다. 금속범프로는 Pb, Sn, Au, Ge, Cu, Bi, Cd, Zn, Ag, Ni 및 Ti 중 한가지 또는 이들 물질의 합금을 적용한다.

<67> 다음으로, 도 4d에 도시한 바와 같이 별도의 서브 마운트 기판(100)을 마련하여, 기판(100) 상부에 다수개의 본딩층(110)과, 서브 마운트 기판(100)의 일 가장자리에 위치한 P형 본딩 패드(115)와, 다른 일 가장자리에 위치한 N형 본딩 패드(110)를 형성한다.

<68> 이후, 도 4e에서 볼 수 있듯이 앞서 설명한 다수개의 발광 셀이 형성된 베이스 기판(10)과, 서브 마운트 기판(100)을 플립칩 본딩하여 발광 소자를 제작한다. 상기 발광 셀의 상부에 형성된 금속범프(50, 55)와 상기 서브 마운트 기판(100)에 형성된 본딩층(110)을 통해 본딩한다. 서브 마운트 기판(100)의 일 가장자리에 위치한 P형 본딩 패드(115)는 일 가장자리에 위치한 발광 셀의 P형 금속범프(55)에 접속되고, 타 가장자리에 위치한 N형 본딩 패드(110)는 다른 가장자리에 위치한 발광 셀의 N형 반도체층(50)에 접속된다.

<69> 상술한 본 발명의 발광 소자의 제조 방법은 이에 한정되지 않고, 다양한 공정과 제조 방법이 소자의 특성 및 공정의 편의에 따라 변경되거나 추가될 수 있다.

<70> 예를 들어 본 실시예는 브리지 공정 또는 스텝 커버 등의 공정을 통해 각기 인접한 발광 셀의 N형 반도체층과 P형 반도체층을 전기적으로 연결하는 브리지 배선을 형성한 후, 서브 마운트 기판과 플립칩 본딩한다. 그러나 이에 한정되지 않고, 다수개의 발광 셀과 서브 마운트 기판의 플립칩 본딩시 서브 마운트 기판에 전극층을 형성하여 금속범프를 통해 인접한 발광 셀의 N형 반도체층과 P형 반도체

층이 전기적으로 연결되도록 할 수도 있다.

<71> 이로써 발광층의 측면이 수평면으로부터 수직이 아닌, 소정의 기울기를 갖는 다수의 플립칩 형태의 발광 셀이 서브 마운트 기판 상에 어레이된 발광 소자를 제조할 수 있다. 상기 발광 셀들은 원하는 목적에 따라 직렬, 병렬 또는 직병렬로 다양하게 연결될 수 있다.

<72> 도 5는 본 발명에 따른 제 3 실시예를 도시한 단면도이다.

<73> 이는 제 2 실시예의 경우와 거의 동일하며, 단지 제 3 실시예는 도 4b에 도시한 바와 마찬가지로 측면이 다양한 기울기를 갖도록 식각하여 다수개의 발광 셀을 분리한 다음, N형 반도체층을 노출시키기 위해 식각하는 경우에도 마찬가지의 식각 공정을 사용하여 발광 소자를 제조할 수 있다. 즉, 도 5에 도시한 바와 같이 N형 반도체층(20)이 노출되도록 식각되는 P형 반도체층(40)과 활성층(30)의 측면이 다양한 기울기를 갖도록 형성할 수 있다. 이러한 발광 소자는 종래 수직으로 식각된 표면에서 반사되었던 광자가 다양한 각의 표면에 의해 반사되지 않고 외부로 빠져나가기 때문에 더욱 향상된 발광 효율을 얻을 수 있다.

<74> 이로써 발광층의 전측면이 수평면으로부터 수직이 아닌, 소정의 기울기를 갖는 다수의 플립칩 형태의 발광 셀이 서브 마운트 기판 상에 어레이된 발광 소자를 제조할 수 있다. 상기 발광 셀들은 원하는 목적에 따라 직렬, 병렬 또는 직병렬로 다양하게 연결될 수 있다.

<75> 발광 소자의 광효율은 내부 양자 효율과 외부 양자 효율로 나타낼 수

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있는데, 내부 양자 효율은 활성층의 설계나 품질에 따라서 결정된다. 외부 양자 효율의 경우 발광층에서 생성되는 광자가 발광 소자의 외부로 나오는 정도에 따라서 결정된다. 종래에는 반도체층의 측면이 수평면으로부터 수직으로 형성되어, 일부의 광자가 반도체층의 측면에서 투과하지 못하고 반사되어 나오며, 전반사된 광은 외부로 투과하지 못하고 발광 소자 내부에서 소멸된다. 그러나, 본 발명에 따르면 반도체층의 측면을 수평면으로부터 수직이 아닌, 소정의 기울기를 갖는 경우에, 경사진 측면이 광의 임계각을 변화시켜 보다 용이하게 광을 추출할 수 있게 돕는다. 따라서 발광층에서 발생한 광이 전반사되지 않고 발광 소자의 외부로 방출될 확률이 높아져 외부 양자 효율이 현저하게 향상된다.

【발명의 효과】

<76> 본 발명에 의한 복수 셀의 단일 발광 소자 및 이의 제조 방법은 발광층에서 생성되는 광이 소정의 기울기를 갖는 경사면에 대해 전반사되지 않고 외부로 방출되어 광추출 효율이 향상된다. 또한 본 발명은 플립칩 구조를 이용하여 열 방출 효율이 높고, 광의 차폐가 거의 없어 광효율이 증가한다.

<77> 본 발명에 의한 복수 셀의 단일 발광 소자 및 이의 제조 방법은 발광 소자의 발광 효율, 외부 양자 효율 등의 특성을 향상시키고 신뢰성을 확보하여, 고광도, 고휘도의 광을 발광할 수 있는 장점이 있다.

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【특허청구범위】

【청구항 1】

N형 반도체층과 상기 N형 반도체층 상에 형성된 P형 반도체층을 포함하는 다수개의 발광 셀이 형성된 기판; 및

상기 기판이 플립칩 본딩되는 서브 마운트 기판을 포함하고,

상기 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층이 연결되고, 상기 발광 셀의 적어도 P형 반도체층을 포함하는 측면이 수평면으로부터 수직이 아닌 소정의 기울기를 갖는 것을 특징으로 하는 복수 셀의 단일 발광 소자.

【청구항 2】

청구항 1에 있어서,

상기 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층을 연결하기 위한 배선을 더 포함하는 것을 특징으로 하는 복수 셀의 단일 발광 소자.

【청구항 3】

청구항 1 또는 청구항 2에 있어서,

상기 소정의 기울기는 20 내지 80° 인 것을 특징으로 하는 복수 셀의 단일 발광 소자.

【청구항 4】

기판 상에 N형 반도체층과 P형 반도체층을 순차적으로 형성하여 상기 기판 상에 발광 셀을 형성하는 단계;

상기 P형 반도체층 상에 측면이 수평면으로부터 수직이 아닌 소정의 기울기를 갖는 식각 마스크 패턴을 형성하는 단계;

상기 식각 마스크 패턴에 의해 노출된 P형 반도체층과 상기 식각 마스크 패턴을 제거하는 단계; 및

상기 기판을 별도의 서브 마운트 기판에 플립칩 본딩하는 단계를 포함하는 발광 소자의 제조 방법.

【청구항 5】

청구항 4에 있어서,

상기 기판 상에 발광 셀을 형성하는 단계는 상기 N형 반도체층 및 P형 반도체층의 일부를 제거하여 다수개의 발광 셀을 형성하는 단계를 포함하고,

상기 P형 반도체층과 상기 식각 마스크 패턴을 제거하는 단계 이후에,

브리지 배선을 통해 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층을 연결하는 단계를 더 포함하는 것을 특징으로 하는 발광 소자의 제조 방법.

【청구항 6】

청구항 5에 있어서,

상기 다수개의 발광 셀을 형성하는 단계는,

상기 P형 반도체층 상에 측면이 수평면으로부터 수직이 아닌 소정의 기울기를 갖는 식각 마스크 패턴을 형성하는 단계;

상기 식각 마스크 패턴에 의해 노출된 P형 반도체층 및 N형 반도체층을 제거하여 다수개의 발광 셀을 형성하는 단계; 및

상기 식각 마스크 패턴을 제거하는 단계를 포함하는 것을 특징으로 하는 발광 소자의 제조 방법.

【청구항 7】

청구항 5에 있어서,

상기 브리지 배선은 브리지(Bridge) 공정 또는 스탭 커버(Step Cover) 공정을 통해 일 발광 셀의 N형 반도체층과 인접한 다른 일 발광 셀의 P형 반도체층을 연결하는 것을 특징으로 하는 발광 소자의 제조 방법.

【청구항 8】

청구항 4 내지 청구항 7 중 어느 한 항에 있어서,

상기 식각 마스크 패턴을 형성하는 단계는,

3 내지 50㎛ 두께의 감광막을 이용하는 것을 특징으로 하는 발광 소자의 제조 방법.

【청구항 9】

청구항 8에 있어서,

상기 P형 반도체층 상에 상기 감광막을 도포하는 단계;

소정의 마스크 패턴에 따라 상기 감광막을 노광시키는 단계; 및

상기 노광 후 베이킹 공정 없이 현상하는 단계를 포함하는 것을 특징으로 하는 발광 소자의 제조 방법.

【청구항 10】

청구항 8에 있어서,

상기 식각 마스크 패턴을 형성하는 단계는,

상기 P형 반도체층 상에 상기 감광막을 도포하는 단계;

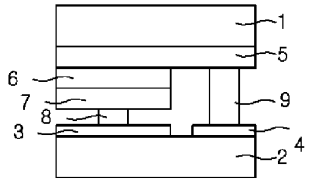
소정의 마스크 패턴에 따라 상기 감광막을 노광시키는 단계;

100℃ 내지 140℃의 온도에서 하드 베이킹을 하는 단계; 및

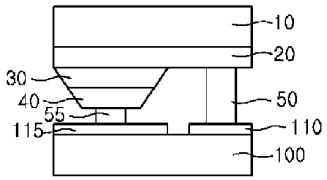
현상하는 단계를 포함하는 것을 특징으로 하는 발광 소자의 제조 방법.

【도면】

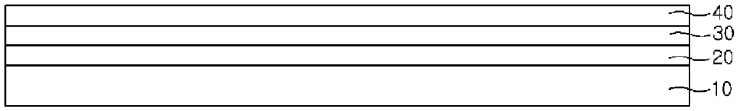
【도 1】



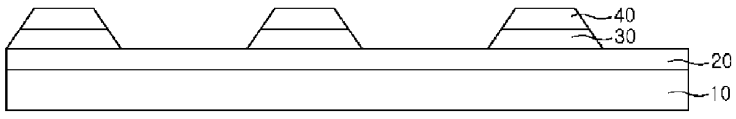
【도 2】



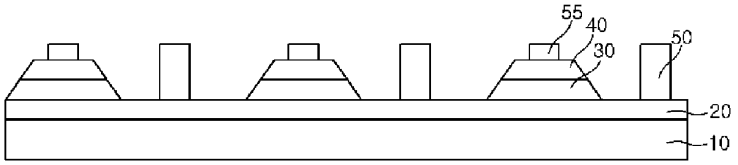
【도 3a】



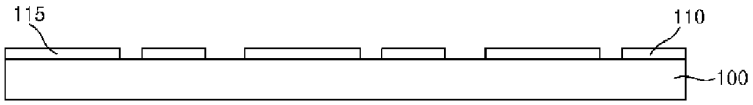
【도 3b】



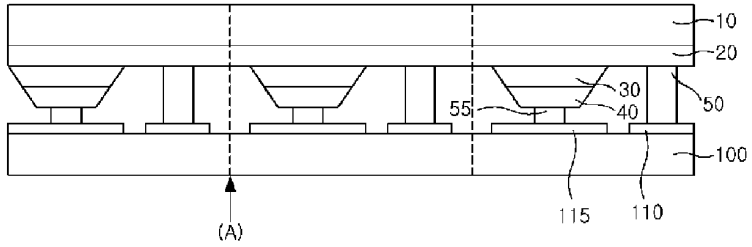
【도 3c】



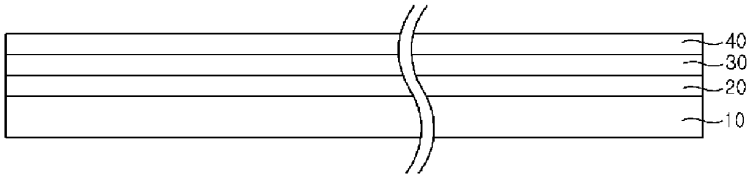
【도 3d】



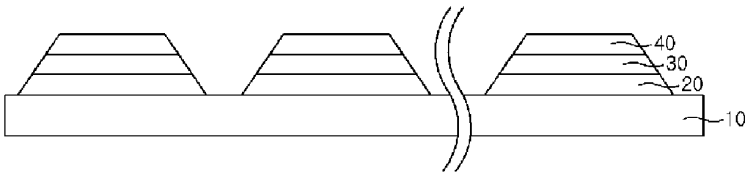
【도 3e】



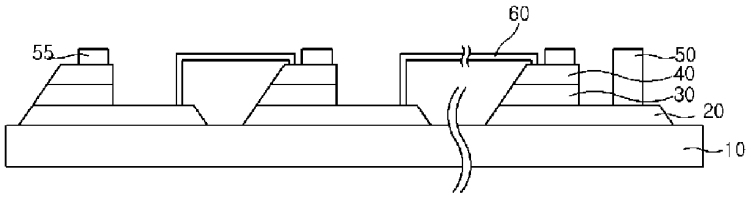
【도 4a】



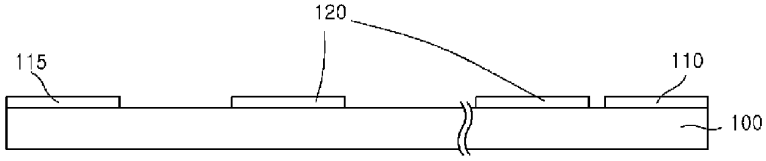
【도 4b】



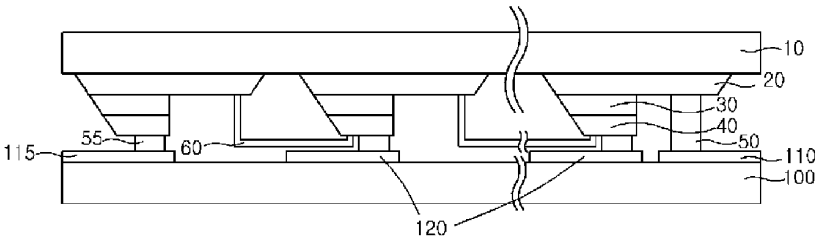
【도 4c】



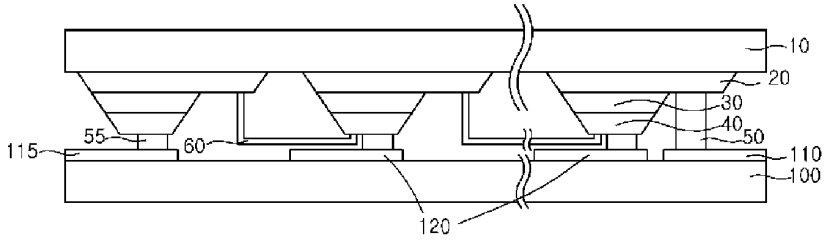
【도 4d】



【도 4e】



【도 5】



대 한 민 국 특 허 청
KOREAN INTELLECTUAL PROPERTY OFFICE

별첨 사본은 아래 출원의 원본과 동일함을 증명함.

This is to certify that the following application annexed hereto is a true copy from the records of the Korean Intellectual Property Office.

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Application Number

출 원 년 월 일 : 2006년 03월 08일
Filing Date MAR. 08, 2006

출 원 인 : 서울옵토디바이스주식회사
Applicant(s) SEOUL OPTO DEVICE CO., LTD.

2009년 11월 23일

특 허 청
COMMISSIONER

【서지사항】

【서류명】 특허출원서

【권리구분】 특허

【수신처】 특허청장

【참조번호】 0072

【제출일자】 2006.03.08

【발명의 국문명칭】 배선들을 갖는 교류용 발광 다이오드 및 그것을 제조하는 방법

【발명의 영문명칭】 LIGHT EMITTING DIODE FOR AC OPERATION WITH WIRES AND METHOD OF FABRICATING THE SAME

【출원인】

【명칭】 서울옵토디바이스주식회사

【출원인코드】 1-2003-032642-0

【대리인】

【성명】 이수완

【대리인코드】 9-1998-000352-8

【포괄위임등록번호】 2005-020694-5

【대리인】

【성명】 조진태

【대리인코드】 9-2003-000088-1

【포괄위임등록번호】 2005-020696-0

【대리인】

【성명】 윤종섭

【대리인코드】 9-2003-000089-8

【포괄위임등록번호】 2005-020697-7

【대리인】

【성명】 이성규

【대리인코드】 9-2003-000083-0

【포괄위임등록번호】 2005-020695-2

【발명자】

【성명】 윤여진

【성명의 영문표기】 YOON, Yeo Jin

【주민등록번호】 720715-1XXXXXX

【우편번호】 426-170

【주소】 경기 안산시 상록구 사동 1553 (38/3) 숲속마을아파트 101-1505

【국적】 KR

【발명자】

【성명】 이재호

【성명의 영문표기】 LEE, Jae Ho

【주민등록번호】 610216-1XXXXXX

【우편번호】 449-531

【주소】 경기 용인시 성복동 LG빌리지 309동 1405호

【국적】 KR

【발명자】

【성명】 김대원

【성명의 영문표기】 KIM, Dae Won

【주민등록번호】 710928-1XXXXXX

【우편번호】 132-861

【주소】 서울 도봉구 쌍문4동 53번지 성원아파트 101동 506호

【국적】 KR

【심사청구】 청구

【취지】 특허법 제42조의 규정에 의한 출원, 특허법 제60조의 규정에 의한 출원심사를 청구합니다.

대리인 이수완 (인)

대리인 조진태 (인)

대리인 윤종섭 (인)

대리인 이성규 (인)

【수수료】

【기본출원료】	0 면	38,000 원
【가산출원료】	25 면	0 원
【우선권주장료】	0 건	0 원
【심사청구료】	13 항	525,000 원
【합계】	563,000 원	
【감면사유】	중기업	
【감면후 수수료】	281,500 원	

【첨부서류】 1.중소기업기본법시행령 제2조에의한 중소기업에 해당함을 증명하는 서류[사업자등록증/원천징수이행상황신고서]_1통

【요약서】

【요약】

배선들을 갖는 교류용 발광 다이오드 및 그것을 제조하는 방법이 개시된다. 이 발광 다이오드는 기판 상에 서로 이격되어 위치하는 발광셀들을 포함한다. 이 발광셀들은 각각 하부 반도체층, 하부 반도체층의 일 영역 상부에 위치하는 상부 반도체층 및 하부 반도체층과 상부 반도체층 사이에 개재된 활성층을 포함한다. 또한, 발광셀들은 그 측벽들이 기판의 상부면에 대해 경사지게 형성되어 위로 갈수록 폭이 좁아진다. 한편, 절연층이 발광셀들의 전면을 덮는다. 절연층은 하부 반도체층들의 다른 영역들 및 상부 반도체층들 상에 각각 형성된 개구부들을 갖는다. 배선들이 절연층 상에 형성되어 개구부들을 통해 하부 반도체층들 및 상부 반도체층들에 전기적으로 연결된다. 배선들은 인접한 발광셀들의 하부 반도체층들과 상부 반도체층들을 각각 전기적으로 연결한다. 따라서, 배선들이 절연층 상에 형성되므로, 배선들의 단선 및 단락을 방지할 수 있어 신뢰성 있는 교류용 발광 다이오드를 제공할 수 있다.

【대표도】

도 3

【색인어】

발광 다이오드, 교류 동작, 배선, 반도체층, 절연층, 포토레지스트

【명세서】

【발명의 명칭】

배선들을 갖는 교류용 발광 다이오드 및 그것을 제조하는 방법{LIGHT EMITTING DIODE FOR AC OPERATION WITH WIRES AND METHOD OF FABRICATING THE SAME}

【도면의 간단한 설명】

<1> 도 1은 종래의 교류용 발광 다이오드를 설명하기 위한 평면도이다.

<2> 도 2는 도 1의 절취선 IV-IV를 따라 취해진 단면도이다.

<3> 도 3은 본 발명의 일 실시예에 따른 교류용 발광 다이오드를 설명하기 위한 단면도이다.

<4> 도 4 내지 도 9는 본 발명의 일 실시예에 따른 교류용 발광 다이오드를 제조하는 방법을 설명하기 위한 단면도들이다.

【발명의 상세한 설명】

【발명의 목적】

【발명이 속하는 기술분야 및 그 분야의 종래기술】

<5> 본 발명은 교류용 발광 다이오드 및 그것을 제조하는 방법에 관한 것으로, 더욱 상세하게는 배선들의 단선 및/또는 배선들에 의한 단락을 방지할 수 있는 교류용 발광 다이오드 및 그것을 제조하는 방법에 관한 것이다.

<6> 질화갈륨(GaN) 계열의 발광 다이오드가 약 10년 동안 적용되고 개발되어 왔

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다. GaN 계열의 LED는 LED 기술을 상당히 변화시켰으며, 현재 천연색 LED 표시소자, LED 교통 신호기, 백색 LED 등 다양한 응용에 사용되고 있다. 최근, 고효율 백색 LED는 형광 램프를 대체할 것으로 기대되고 있으며, 특히 백색 LED의 효율(efficiency)은 통상의 형광램프의 효율에 유사한 수준에 도달하고 있다.

<7> 일반적으로, 발광 다이오드는 순방향 전류에 의해 광을 방출하며, 직류전류의 공급을 필요로 한다. 따라서, 발광 다이오드는, 교류전원에 직접 연결하여 사용할 경우, 전류의 방향에 따라 온/오프를 반복하며, 그 결과 연속적으로 빛을 방출하지 못하고, 역방향 전류에 의해 쉽게 파손되는 문제점이 있다.

<8> 이러한 발광 다이오드의 문제점을 해결하여, 고전압 교류전원에 직접 연결하여 사용할 수 있는 발광 다이오드가 국제공개번호 WO 2004/023568(A1)호에 "발광성분들을 갖는 발광소자"(LIGHT-EMITTING DEVICE HAVING LIGHT-EMITTING ELEMENTS)라는 제목으로 사카이 등(SAKAI et. al.)에 의해 개시된 바 있다.

<9> 도 1은 상기 WO 2004/023568(A1)호에 따른 교류용 발광 다이오드를 설명하기 위한 부분적인 평면도이고, 도 2는 도 1의 절취선 IV-IV를 따라 취해진 단면도이다.

<10> 도 1 및 도 2를 참조하면, 기판(10) 상에 복수개의 발광셀들(1)이 형성된다. 또한, 발광셀들(1) 상에 p-전극(22) 및 n-전극(24)이 형성된다. 에어브리지 배선(28)이 인접한 발광셀들의 p-전극(22)과 n-전극(24)을 전기적으로 연결하여, 복수개의 발광셀들(1)을 직렬 연결한다.

<11> 각 발광셀은 n-GaN층(14), p-GaN층(20)을 포함한다. 도시하지는 않았지만, n-GaN층(14)과 p-GaN층(20) 사이에 InGaN 활성층이 개재될 수 있다. p-전극(22)은 상기 p-GaN층(20) 상에 형성되고, n-전극(24)은 상기 n-GaN층(14) 상에 형성된다. 한편, 에어브리지 배선(28)은 n-전극(24)과 p-전극(22)을 전기적으로 연결한다.

<12> 상기 WO 2004/023568(A1)호에 따르면, LED들(발광셀들)이 사파이어 기판과 같은 절연성 기판 상에 2차원적으로 직렬연결되어 LED 어레이를 형성한다. 이러한 두개의 LED 어레이들이 상기 사파이어 기판 상에서 역병렬로 연결된다. 그 결과, AC 파워 서플라이에 의해 구동될 수 있는 단일칩 발광소자가 제공된다.

<13> 그러나, 도 2에 도시한 바와 같이, p-전극(22)과 n-전극(24)을 연결하는 배선(28)은 에어브리지 배선으로, 접촉부들 이외 부분은 공중에 떠 있게 된다. 이러한 에어브리지 배선(28)은 외압에 의해 단선되기 쉬우며, 또한 외압에 의한 변형에 의해 단락을 유발하기 쉽다.

【발명이 이루고자 하는 기술적 과제】

<14> 본 발명이 이루고자 하는 기술적 과제는, 외압에 의해 배선들이 단선 또는 단락되는 것을 방지할 수 있는 교류용 발광 다이오드를 제공하는 데 있다.

<15> 본 발명이 이루고자 하는 다른 기술적 과제는, 배선들을 형성한 후에 잔존하는 금속물질이 발광셀들을 단락시키는 것을 방지할 수 있는 교류용 발광 다이오드를 제공하는 데 있다.

<16> 본 발명이 이루고자 하는 또 다른 기술적 과제는 배선들의 단선 및/또는 단

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락을 방지할 수 있는 교류용 발광 다이오드를 제조하는 방법을 제공하는 데 있다.

【발명의 구성】

<17> 상기 기술적 과제들을 이루기 위하여, 본 발명의 일 태양은 안정한(robust) 배선들을 갖는 교류용 발광 다이오드를 제공한다. 이 발광 다이오드는 기판 상에 서로 이격되어 위치하는 발광셀들을 포함한다. 상기 발광셀들은 각각 하부 반도체층, 상기 하부 반도체층의 일 영역 상부에 위치하는 상부 반도체층 및 상기 하부 반도체층과 상기 상부 반도체층 사이에 개재된 활성층을 포함한다. 또한, 상기 발광셀들은 그 측벽들이 상기 기판의 상부면에 대해 경사지게 형성되어 위로 갈수록 폭이 좁아진다. 절연층이 상기 발광셀들의 전면을 덮는다. 상기 절연층은 상기 하부 반도체층들의 다른 영역들 및 상기 상부 반도체층들 상에 각각 형성된 개구부들을 갖는다. 배선들이 상기 절연층 상에 형성되어 상기 개구부들을 통해 상기 하부 반도체층들 및 상기 상부 반도체층들에 전기적으로 연결된다. 상기 배선들은 인접한 발광셀들의 상기 하부 반도체층들과 상기 상부 반도체층들을 각각 전기적으로 연결한다. 상기 배선들이 절연층 상에 형성되므로, 배선들의 단선 및 배선들에 의한 단락을 방지할 수 있어 신뢰성 있는 교류용 발광 다이오드를 제공할 수 있다.

<18> 상기 발광셀들 각각의 하부 반도체층의 측벽들이 상기 기판의 상부면과 이루는 경사각이 15도 내지 80도의 범위 내일 수 있다. 이에 따라, 금속층을 증착한 후 패터닝하여 상기 배선들을 형성할 수 있어 안정한 배선들을 쉽게 형성할 수 있다.

<19> 전극패드들이 상기 하부 반도체층들의 다른 영역들과 상기 절연층 사이에 개

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재될 수 있다. 상기 전극패드들은 상기 하부 반도체층들의 다른 영역들 상에 형성된 개구부들에 의해 노출된다. 이에 따라, 상기 배선들은 상기 전극패드들에 접촉되어 상기 하부 반도체층에 전기적으로 연결된다.

<20> 또한 투명전극층들이 상기 상부 반도체층들과 상기 절연층 사이에 개재될 수 있다. 상기 투명전극층들은 상기 상부 반도체층들 상에 형성된 개구부들에 의해 노출된다. 이에 따라, 상기 배선들은 상기 투명전극층들에 접촉되어 상기 상부 반도체층에 전기적으로 연결된다. 상기 투명전극층들은 상기 상부 반도체층들에 전류를 분산시키며, 상기 활성층에서 생성된 광을 투과시킨다.

<21> 절연보호막이 상기 배선들 및 상기 절연층을 덮을 수 있다. 상기 절연보호막은 배선들이 외압에 의해 변형되는 것을 방지하며, 또한 수분 등에 의해 배선들이 오염되는 것을 방지한다.

<22> 상기 또 다른 기술적 과제를 이루기 위하여, 본 발명의 다른 태양은 안정한 배선들을 갖는 교류용 발광 다이오드 제조방법을 제공한다. 이 방법은 기판 상에 서로 이격된 발광셀들을 형성하는 것을 포함한다. 상기 발광셀들은 각각 하부 반도체층, 상기 하부 반도체층의 일 영역 상부에 위치하는 상부 반도체층 및 상기 하부 반도체층과 상기 상부 반도체층 사이에 개재된 활성층을 포함하고, 상기 발광셀들의 측벽들은 상기 기판의 상부면에 대해 경사지게 형성되어 위로 갈수록 폭이 좁아진다. 연속적인(conformal) 절연층이 상기 발광셀들을 갖는 기판 상에 형성된다. 이어서, 상기 절연층을 패터닝하여 상기 하부 반도체층들의 다른 영역들 및 상기 상부 반도체층들 상에 개구부들이 형성된다. 그 후, 상기 절연층 상에 배선들이 형

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성된다. 상기 배선들은 상기 개구부들을 통해 상기 하부 반도체층들 및 상기 상부 반도체층들에 전기적으로 연결되고, 인접한 발광셀들의 상기 하부 반도체층들과 상기 상부 반도체층들을 각각 전기적으로 연결한다. 본 태양에 따르면, 발광셀들의 측벽들이 경사지게 형성되므로, 상기 절연층을 연속적으로 형성하는 것이 쉽다. 또한 연속적인(conformal) 절연층을 형성할 수 있어, 상기 절연층이 발광셀들의 단락을 방지한다. 이에 더하여, 상기 절연층에 의해 지지되는 배선들을 형성할 수 있어 신뢰성 있는 교류용 발광 다이오드를 제조할 수 있다.

<23> 한편, 상기 절연층을 형성하기 전, 전극패드들이 상기 발광셀들의 하부 반도체층들의 다른 영역들 상에 형성될 수 있다. 상기 전극패드들은 상기 하부 반도체층들의 다른 영역들 상에 형성된 개구부들에 의해 노출된다. 즉, 상기 전극패드들은 상기 절연층에 개구부들을 형성하는 동안 노출되어 상기 하부 반도체층들이 노출되는 것을 방지한다. 이에 따라, 상기 하부 반도체층들이 상기 개구부들을 형성하는 동안 손상되는 것을 방지할 수 있다.

<24> 또한, 상기 절연층을 형성하기 전, 투명전극층들이 상기 발광셀들의 상부 반도체층들 상에 형성될 수 있다. 상기 투명전극층들은 상기 상부 반도체층들 상에 형성된 개구부들에 의해 노출된다. 상기 상부 반도체층들 상에 투명전극층들이 형성되므로, 상기 배선들은 상기 투명전극층들에 접촉된다. 따라서, 상기 배선들의 물질 선택의 폭이 넓어진다.

<25> 한편, 상기 발광셀들을 형성하는 것은 상기 기판 전면에 하부 반도체층, 활성층 및 상부 반도체층을 형성하는 것을 포함한다. 상기 상부 반도체층 상에 발광

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셀 영역들을 한정하는 포토레지스트 패턴들이 형성될 수 있다. 그 후, 상기 포토레지스트 패턴들의 측벽들이 상기 기판 상부면에 대해 경사지도록 상기 포토레지스트 패턴들이 리플로우(reflow)된다. 이어서, 상기 포토레지스트 패턴들을 식각마스크로 사용하여 상기 상부 반도체층, 활성층 및 하부 반도체층이 차례로 식각된다. 이에 따라, 경사진 측벽들을 갖도록 발광셀 영역들이 분리된다.

<26> 한편, 상기 포토레지스트 패턴들은 상기 포토레지스트 패턴들의 측벽들이 상기 기판 상부면에 대해 15도 내지 80도 범위 내의 경사각을 갖도록 리플로우될 수 있다. 80도 이하의 경사각은 연속적인 절연층 형성 및 배선들을 형성하기 위해 요구되며, 15도 이상의 경사각은 충분한 발광영역들을 확보하기 위해 요구된다.

<27> 이에 더하여, 상기 상부 반도체층, 활성층 및 하부 반도체층을 차례로 식각한 후, 상기 상부 반도체층 및 활성층을 다시 패터닝하여 상기 하부 반도체층을 노출시킬 수 있다. 이와 달리, 상기 상부 반도체층, 활성층 및 하부 반도체층을 차례로 식각하기 전, 상기 상부 반도체층 및 활성층을 패터닝하여 상기 하부 반도체층을 노출시킬 수도 있다.

<28> 한편, 상기 배선들을 형성하는 것은 상기 절연층 상에 배선영역들을 한정하는 개구부들을 갖는 포토레지스트 패턴을 형성하는 것을 포함할 수 있다. 이어서, 상기 개구부들 내에 금속층이 도금된다. 그 후, 상기 포토레지스트 패턴이 제거되어 배선들이 형성된다.

<29> 이와 달리, 상기 배선들을 형성하는 것은 상기 절연층을 갖는 기판 상에 금속층을 증착하는 것을 포함할 수 있다. 이어서, 상기 금속층을 패터닝함으로써 배

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선들이 형성된다. 상기 발광셀들의 측벽이 경사져 있기 때문에, 금속층은 상기 절연층 상에 연속적으로 형성된다. 따라서, 금속층을 증착하고 이를 패터닝하여 배선들을 형성하는 것이 수월하게 수행될 수 있다. 또한, 절연층이 상기 발광셀들의 측벽들을 덮고 있으므로, 금속층 물질이 발광셀들을 단락시키는 것을 방지할 수 있다.

<30> 이하, 첨부한 도면들을 참조하여 본 발명의 실시예들을 상세히 설명하기로 한다. 다음에 소개되는 실시예들은 당업자에게 본 발명의 사상이 충분히 전달될 수 있도록 하기 위해 예로서 제공되는 것이다. 따라서, 본 발명은 이하 설명되는 실시예들에 한정되지 않고 다른 형태로 구체화될 수도 있다. 그리고, 도면들에 있어서, 구성요소의 폭, 길이, 두께 등은 편의를 위하여 과장되어 표현될 수 있다. 명세서 전체에 걸쳐서 동일한 참조번호들은 동일한 구성요소들을 나타낸다.

<31> 도 3은 본 발명의 일 실시예에 따른 교류용 발광 다이오드를 설명하기 위한 단면도이다.

<32> 도 3을 참조하면, 단일 기판(51) 상에 복수개의 발광셀들(56)이 이격되어 위치한다. 상기 기판(51)은 절연 또는 도전성 기판일 수 있으며, 예컨대 사파이어 또는 탄화실리콘(SiC) 기판일 수 있다.

<33> 상기 발광셀들(56) 각각은 하부 반도체층(55), 상기 하부 반도체층의 일영역 상에 위치하는 상부 반도체층(59) 및 상기 하부 반도체층과 상부 반도체층 사이에 개재된 활성층(57)을 포함한다. 여기서, 상기 하부 및 상부 반도체층은 각각 n형 및 p형, 또는 p형 및 n형이다.

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<34> 하부 반도체층(55), 활성층(57) 및 상부 반도체층(59)은 각각 질화갈륨 계열의 반도체 물질 즉, (B, Al, In, Ga)N으로 형성될 수 있다. 상기 활성층(57)은 요구되는 파장의 광 예컨대 자외선 또는 청색광을 방출하도록 조성 원소 및 조성비가 결정되며, 하부 반도체층(55) 및 상부 반도체층(59)은 상기 활성층(57)에 비해 밴드갭이 큰 물질로 형성된다.

<35> 상기 하부 반도체층(55) 및/또는 상부 반도체층(59)은, 도시한 바와 같이, 단일층으로 형성될 수 있으나, 다층 구조로 형성될 수도 있다. 또한, 활성층(57)은 단일 양자웰 또는 다중 양자웰 구조를 가질 수 있다.

<36> 한편, 발광셀들(56)과 기판(51) 사이에 버퍼층(53)이 개재될 수 있다. 버퍼층(53)은 기판(51)과 그 위에 형성될 하부 반도체층(55)의 격자부정합을 완화시키기 위해 채택된다. 버퍼층(53)은, 도시한 바와 같이 연속적일 수 있으나, 이에 한정되는 것은 아니며, 하부 반도체층들(55) 아래에 한정되어 위치할 수 있다.

<37> 발광셀들(56)의 측벽들은 기판(51) 상부면에 대해 경사지게 형성되어 위로 갈수록 폭이 좁아진다. 상기 측벽들의 경사는 활성층(57)에서 생성된 광의 방출 효율을 향상시키며, 상기 발광셀들(56) 위에 형성될 다른 층들의 연속적인 (conformal) 증착을 돕는다. 본 실시예에 있어서, 상기 발광셀들(56) 각각의 하부 반도체층(55)의 측벽들이 기판(51)의 상부면과 이루는 경사각은 15도 내지 80도의 범위 내일 수 있다.

<38> 절연층(69)이 발광셀들(56)의 전면을 덮는다. 절연층(69)은 하부 반도체층들

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(55)의 다른 영역들, 즉 상부 반도체층(59)이 형성된 영역에 인접하는 영역 상에 개구부들을 가지며, 또한 상부 반도체층들(59) 상에 개구부들을 갖는다. 상기 개구부들은 서로 이격되어 위치하며, 따라서 발광셀들(56)의 측벽들은 절연층(69)에 의해 덮인다. 절연층(69)은 또한 발광셀들(56) 사이 영역들 내의 기판(51) 또는 버퍼층(53)을 덮을 수 있다. 절연층(69)은 실리콘산화막(SiO_2)으로 형성될 수 있다.

<39> 배선들(71)이 절연층(69) 상에 형성된다. 배선들(71)은 상기 개구부들을 통해 하부 반도체층들(55) 및 상부 반도체층들(59)에 전기적으로 연결된다. 또한 배선들(71)은 인접한 발광셀들(56)의 하부 반도체층들(55)과 상부 반도체층들(59)을 각각 전기적으로 연결하여 발광셀들(56)의 직렬 어레이를 형성한다. 이러한 어레이들이 복수개 형성될 수 있으며, 복수개의 어레이들이 서로 역병렬로 연결되어 교류전원에 연결되어 구동될 수 있다. 또한, 발광셀들의 직렬 어레이에 연결된 브리지 정류기(도시하지 않음)가 형성될 수 있으며, 상기 브리지 정류기에 의해 상기 발광셀들이 교류전원하에서 구동될 수도 있다. 상기 브리지 정류기는 상기 발광셀들(56)과 동일한 구조의 발광셀들을 배선들(71)을 이용하여 결선함으로써 형성할 수 있다. 상기 배선들은 도전 물질, 예컨대 다결정 실리콘과 같은 도핑된 반도체 물질 또는 금속으로 형성될 수 있다.

<40> 한편, 하부 반도체층들(55)의 다른 영역들과 절연층(69) 사이에 전극패드들(67)이 개재될 수 있다. 전극패드들(67)은 하부 반도체층들(55)의 다른 영역들 상에 형성된 상기 개구부들에 의해 노출된다. 전극패드들(67)은 하부반도체층들(55)

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에 오믹콘택된다. 상기 배선들(71)은 상기 개구부들에 의해 노출된 전극패드들(67)에 접촉되어 하부 반도체층들(55)에 전기적으로 연결된다.

<41> 또한, 투명전극층들(65)이 상부 반도체층들(59)과 절연층(69) 사이에 개재될 수 있다. 투명전극층들(65)은 상부 반도체층들(59) 상에 형성된 상기 개구부들에 의해 노출된다. 투명전극층들(65)은 활성층(57)에서 생성된 광을 투과시키며, 상부 반도체층들(59)에 전류를 분산시키어 공급한다. 상기 배선들(71)은 상기 개구부들에 의해 노출된 투명전극층들(65)에 접촉되어 상부 반도체층들(55)에 전기적으로 연결된다. 한편, 상기 투명전극층들(65) 상에 전극패드들(도시하지 않음)이 더 형성될 수 있으며, 상기 배선들(71)은 상기 전극패드들에 접촉될 수 있다.

<42> 한편, 절연보호막(73)이 상기 배선들(71) 및 상기 절연층(69)을 덮을 수 있다. 절연보호막(73)은 배선들(71)이 수분 등에 의해 오염되는 것을 방지하며, 외압에 의해 배선들(71)이 손상되는 것을 방지한다. 절연보호막(73)은 투광성물질, 예컨대 실리콘산화막으로 형성될 수 있다.

<43> 도 4 내지 도 9는 본 발명의 일 실시예에 따른 교류용 발광 다이오드를 제조하는 방법을 설명하기 위한 단면도들이다.

<44> 도 4를 참조하면, 기판(51) 상에 하부 반도체층(55), 활성층(57) 및 상부 반도체층(59)이 형성된다. 또한, 하부 반도체층(55)을 형성하기 전, 기판(51) 상에 버퍼층(53)이 형성될 수 있다.

<45> 상기 기판(51)은 사파이어(Al_2O_3), 탄화실리콘(SiC), 산화아연(ZnO), 실리콘

(Si), 갈륨비소(GaAs), 갈륨인(GaP), 리튬-알루미나($LiAl_2O_3$), 질화붕소(BN), 질화알루미늄(AlN) 또는 질화갈륨(GaN) 기판일 수 있으나, 이에 한정되는 것은 아니며, 기판(51) 상에 형성될 반도체층의 물질에 따라 다양하게 선택될 수 있다.

<46> 버퍼층(53)은 기판(51)과 그 위에 형성될 반도체층(55)의 격자부정합을 완화하기 위해 형성되며, 예컨대 질화갈륨(GaN) 또는 질화알루미늄(AlN)으로 형성될 수 있다. 상기 기판(51)이 도전성 기판인 경우, 상기 버퍼층(53)은 절연층 또는 반절연층으로 형성되는 것이 바람직하며, AlN 또는 반절연 GaN로 형성될 수 있다.

<47> 하부 반도체층(55), 활성층(57) 및 상부 반도체층(59)은 각각 질화갈륨 계열의 반도체 물질 즉, (B, Al, In, Ga)N로 형성될 수 있다. 상기 하부 및 상부 반도체층(55, 59) 및 활성층(57)은 금속유기화학기상증착(MOCVD), 분자선 성장(molecular beam epitaxy) 또는 수소화물 기상 성장(hydride vapor phase epitaxy; HVPE) 기술 등을 사용하여 단속적으로 또는 연속적으로 성장될 수 있다.

<48> 여기서, 상기 하부 및 상부 반도체층들은 각각 n형 및 p형, 또는 p형 및 n형이다. 질화갈륨 계열의 화합물 반도체층에서, n형 반도체층은 불순물로 예컨대 실리콘(Si)을 도핑하여 형성될 수 있으며, p형 반도체층은 불순물로 예컨대 마그네슘(Mg)을 도핑하여 형성될 수 있다.

<49> 상기 상부 반도체층(59) 상에 발광셀 영역들을 한정하는 포토레지스트 패턴들(63)이 형성된다. 상기 포토레지스트 패턴들은 발광셀 영역들을 덮도록 형성된다. 한편, 측벽들이 기판(51) 상부면에 대해 경사지도록 상기 포토레지스트

패턴들(63)은 리플로우(reflow)된다. 상기 포토레지스트 패턴들(63)의 측벽들이 기판(51) 상부면에 대해 15도 내지 80도 범위 내의 경사각을 갖도록 형성될 수 있다.

<50> 도 5를 참조하면, 상기 포토레지스트 패턴들(63)을 식각마스크로 사용하여 상부 반도체층(59), 활성층(57) 및 하부 반도체층(55)을 차례로 식각한다. 이에 따라, 포토레지스트 패턴들(63)의 형상이 상기 반도체층들(59, 57, 55)에 전사되어 측벽들이 경사진 발광셀 영역들이 분리된다. 상기 식각 공정에 의해 버퍼층(53)이 노출될 수 있으며, 노출된 버퍼층(53)은 과식각에 의해 제거될 수 있다.

<51> 그 후, 상기 포토레지스트 패턴들(63)을 제거하고, 상기 상부 반도체층 및 활성층을 다시 패터닝하여 상기 식각된 하부 반도체층들(55)을 노출시킨다. 이때, 노출된 하부 반도체층들은 과식각에 의해 부분적으로 식각될 수 있다. 그 결과, 기판(51) 상에 서로 이격된 발광셀들(56)이 형성된다. 상기 발광셀들(56) 각각은 식각되어 서로 이격된 하부 반도체층(56), 상기 하부 반도체층(56)의 일 영역 상부에 위치하는 상부 반도체층(57) 및 상기 하부 반도체층(55)과 상기 상부 반도체층(57) 사이에 개재된 활성층(57)을 포함하고, 상기 하부 반도체층(56)의 다른 영역은 노출된다. 또한, 발광셀들(56)의 측벽들 대부분은 기판(51) 상부면에 대해 경사지게 형성된다. 한편, 하부 반도체층들(55)의 다른 영역들과 인접한 상부 반도체층들(59)의 측벽들은, 도시한 바와 같이 경사지게 형성될 수 있으나, 수직하게 형성될 수도 있다.

<52> 도 6을 참조하면, 상기 발광셀(56)의 상부 반도체층(59) 상에 투명전극층(65)이 형성될 수 있다. 상기 투명전극층(65)은 인디움 틴 산화막(ITO) 또는 Ni/Au

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와 같은 투명금속으로 형성된다. 또한, 상기 하부 반도체층들(55)의 다른 영역들 상에 전극패드들(67)이 형성될 수 있다. 상기 전극패드들(67)은 상기 하부 반도체층들(55)에 오믹콘택된다.

<53> 상기 투명전극층(65)은 포토레지스트 패턴들(63)을 형성하기 전, 상부 반도체층(59) 상에 형성될 수도 있다. 이때, 투명전극층(65)은 상부 반도체층과 함께 패터닝된다.

<54> 도 7을 참조하면, 발광셀들(56)을 갖는 기판(51) 상에 연속적인 절연층(69)이 형성된다. 절연층(69)은 발광셀들(56)의 측벽 및 상부면을 덮고, 발광셀들(56) 사이 영역의 기판(51) 상부를 덮는다. 상기 절연층(69)은 화학기상증착(CVD) 기술을 사용하여 예컨대 실리콘 산화막으로 형성될 수 있다.

<55> 상기 발광셀들(56)의 측벽들이 경사지게 형성되어 있으므로, 상기 절연층(69)은 발광셀들(56)의 측벽들을 쉽게 덮을 수 있다. 상부 반도체층(59) 및 활성층(57)의 전체 두께가 얇고, 또한 상부 반도체층들(59) 사이의 공간이 넓기 때문에, 상기 하부 반도체층들(55)의 다른 영역들에 인접한 상부 반도체층들(59)의 측벽들도 절연층(69)에 의해 쉽게 덮일 수 있다.

<56> 도 8을 참조하면, 상기 절연층(69)을 패터닝하여 하부 반도체층들(55)의 다른 영역들 및 상부 반도체층들(59) 상에 개구부들이 형성된다. 전극패드들(67) 및 투명전극층들(65)이 형성된 경우, 상기 개구부들에 의해 전극패드들(67) 및 투명전극층들(65)이 노출된다.

<57> 상기 개구부들은 사진 및 식각 공정을 사용하여 형성될 수 있으며, 전극패드들(67)은 절연층(69)을 식각하는 동안 하부 반도체층들(55)이 손상되는 것을 방지한다.

<58> 도 9를 참조하면, 상기 개구부들을 갖는 절연층(69) 상에 배선들(71)이 형성된다. 상기 배선들(71)은 상기 개구부들을 통해 하부 반도체층들(55) 및 상부 반도체층들(59)에 전기적으로 연결되고, 인접한 발광셀들(56)의 하부 반도체층들(55)과 상부 반도체층들(59)을 각각 전기적으로 연결하여 직렬 연결된 어레이들을 형성한다.

<59> 상기 배선들(71)은 도금 기술을 사용하여 형성될 수 있다. 즉, 상기 절연층(69) 상에 배선 영역을 한정하는 개구부들을 갖는 포토레지스트 패턴을 형성하고, 상기 개구부들 내에 금속층을 도금한 후, 상기 포토레지스트 패턴을 제거함으로써 배선들(71)을 형성할 수 있다.

<60> 이와 달리, 상기 배선들(71)은, 화학기상증착 또는 물리기상증착 기술을 사용하여 형성될 수 있다. 즉, 전자빔 증착(e-beam evaporation)과 같은 기상증착 기술을 사용하여 금속층을 형성한 후, 이를 사진 및 식각 공정을 사용하여 패터닝함으로써 배선들(71)을 형성할 수 있다. 상기 발광셀들(56)의 측벽들이 경사져 있으므로, 금속층은 발광셀들의(56) 측벽 상부에 연속적으로 형성된다. 또한, 절연층(69)이 발광셀들(56)의 측벽들을 덮고 있으므로, 금속층 패터닝 후 잔존하는 금속물질에 의해 발광셀들(56)이 단락되는 것을 방지할 수 있다.

<61> 상기 배선들(71)이 형성된 기판(51) 상에 보호절연막(73)이 형성된다. 상기

보호절연막(73)은 화학기상증착 기술을 사용하여, 투광성 물질, 예컨대 실리콘 산화막으로 형성될 수 있다. 그 결과, 도 1의 교류용 발광 다이오드가 완성된다.

【발명의 효과】

<62> 본 발명의 실시예들에 따르면, 외압에 의해 배선들이 단선 또는 단락되는 것을 방지할 수 있어 신뢰성 있는 교류용 발광 다이오드를 제공할 수 있으며, 배선들을 형성하는 동안 잔존하는 금속 등의 도전성 물질이 발광셀들을 단락시키는 것을 방지할 수 있다. 또한, 절연층에 의해 지지되는 배선들을 형성할 수 있어 신뢰성 있는 교류용 발광 다이오드를 제조할 수 있다.

【특허청구범위】

【청구항 1】

기판 상에 서로 이격되어 위치하고, 각각 하부 반도체층, 상기 하부 반도체층의 일 영역 상부에 위치하는 상부 반도체층 및 상기 하부 반도체층과 상기 상부 반도체층 사이에 개재된 활성층을 포함하고, 측벽들이 상기 기판의 상부면에 대해 경사지게 형성되어 위로 갈수록 폭이 좁아지는 발광셀들;

상기 발광셀들의 전면을 덮되, 상기 하부 반도체층들의 다른 영역들 및 상기 상부 반도체층들 상에 각각 형성된 개구부들을 갖는 절연층;

상기 절연층 상에 형성되어 상기 개구부들을 통해 상기 하부 반도체층들 및 상기 상부 반도체층들에 전기적으로 연결되고, 인접한 발광셀들의 상기 하부 반도체층들과 상기 상부 반도체층들을 각각 전기적으로 연결하는 배선들을 포함하는 교류용 발광 다이오드.

【청구항 2】

청구항 1에 있어서,

상기 발광셀들 각각의 하부 반도체층의 측벽들이 상기 기판의 상부면과 이루는 경사각이 15도 내지 80도의 범위 내인 것을 특징으로 하는 교류용 발광 다이오드.

【청구항 3】

청구항 1에 있어서,

상기 하부 반도체층들의 다른 영역들과 상기 절연층 사이에 개재된 전극패드들을 더 포함하고, 상기 전극패드들은 상기 하부 반도체층들의 다른 영역들 상에 형성된 개구부들에 의해 노출되는 교류용 발광 다이오드.

【청구항 4】

청구항 3에 있어서,

상기 상부 반도체층들과 상기 절연층 사이에 개재된 투명전극층들을 더 포함하고, 상기 투명전극층들은 상기 상부 반도체층들 상에 형성된 개구부들에 의해 노출되는 교류용 발광 다이오드.

【청구항 5】

청구항 1에 있어서,

상기 배선들 및 상기 절연층을 덮는 절연보호막을 더 포함하는 교류용 발광 다이오드.

【청구항 6】

기판 상에 서로 이격된 발광셀들을 형성하되, 상기 발광셀들은 각각 하부 반도체층, 상기 하부 반도체층의 일 영역 상부에 위치하는 상부 반도체층 및 상기 하부 반도체층과 상기 상부 반도체층 사이에 개재된 활성층을 포함하고, 상기 발광셀들의 측벽들은 상기 기판의 상부면에 대해 경사지게 형성되어 위로 갈수록 폭이 좁아지고,

상기 발광셀들을 갖는 기판 상에 연속적인 절연층을 형성하고,

상기 절연층을 패터닝하여 상기 하부 반도체층들의 다른 영역들 및 상기 상부 반도체층들 상에 개구부들을 형성하고,

상기 절연층 상에 배선들을 형성하되, 상기 배선들은 상기 개구부들을 통해 상기 하부 반도체층들 및 상기 상부 반도체층들에 전기적으로 연결되고, 인접한 발광셀들의 상기 하부 반도체층들과 상기 상부 반도체층들을 각각 전기적으로 연결하는 것을 포함하는 교류용 발광 다이오드 제조방법.

【청구항 7】

청구항 6에 있어서,

상기 절연층을 형성하기 전, 상기 발광셀들의 하부 반도체층들의 다른 영역들 상에 전극패드들을 형성하는 것을 더 포함하고, 상기 전극패드들은 상기 하부 반도체층들의 다른 영역들 상에 형성된 개구부들에 의해 노출되는 교류용 발광 다이오드 제조방법.

【청구항 8】

청구항 7에 있어서,

상기 절연층을 형성하기 전, 상기 발광셀들의 상부 반도체층들 상에 투명전극층들을 형성하는 것을 더 포함하고, 상기 투명전극층들은 상기 상부 반도체층들 상에 형성된 개구부들에 의해 노출되는 교류용 발광 다이오드 제조방법.

【청구항 9】

청구항 6에 있어서,

상기 발광셀들을 형성하는 것은,

상기 기판 전면에 하부 반도체층, 활성층 및 상부 반도체층을 형성하고,

상기 상부 반도체층 상에 발광셀 영역들을 한정하는 포토레지스트 패턴들을 형성하고,

상기 포토레지스트 패턴들의 측벽들이 상기 기판 상부면에 대해 경사지도록 상기 포토레지스트 패턴들을 리플로우하고,

상기 포토레지스트 패턴들을 식각마스크로 사용하여 상기 상부 반도체층, 활성층 및 하부 반도체층을 차례로 식각하는 것을 포함하는 교류용 발광 다이오드 제조방법.

【청구항 10】

청구항 9에 있어서,

상기 포토레지스트 패턴들을 리플로우하는 것은 상기 포토레지스트 패턴들의 측벽들이 상기 기판 상부면에 대해 15도 내지 80도 범위 내의 경사각을 갖도록 수행되는 교류용 발광 다이오드 제조방법.

【청구항 11】

청구항 9에 있어서,

상기 상부 반도체층, 활성층 및 하부 반도체층을 차례로 식각한 후, 상기 상부 반도체층 및 활성층을 다시 패터닝하여 상기 하부 반도체층을 노출시키는 것을 더 포함하는 교류용 발광 다이오드 제조방법.

【청구항 12】

청구항 6에 있어서,

상기 배선들을 형성하는 것은

상기 절연층 상에 배선 영역을 한정하는 개구부들을 갖는 포토레지스트 패턴을 형성하고,

상기 개구부들 내에 금속층을 도금하고,

상기 포토레지스트 패턴을 제거하는 것을 포함하는 교류용 발광 다이오드 제조방법.

【청구항 13】

청구항 6에 있어서,

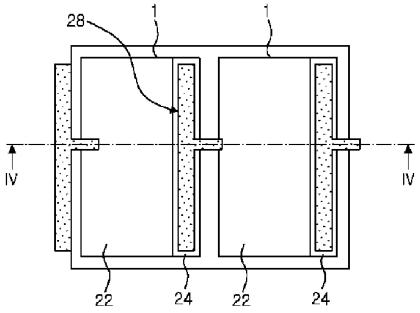
상기 배선들을 형성하는 것은

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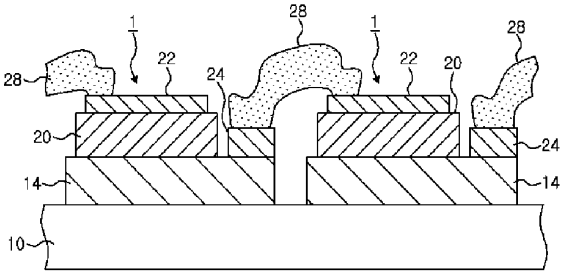
상기 금속층을 패터닝하는 것을 포함하는 교류용 발광 다이오드 제조방법.

【도면】

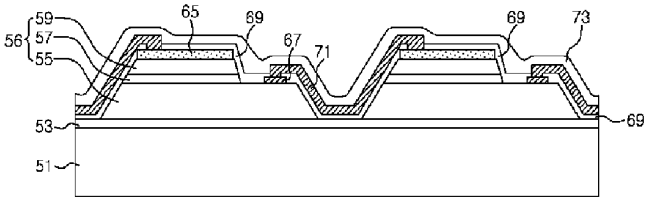
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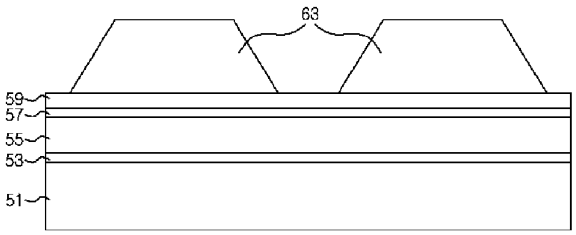
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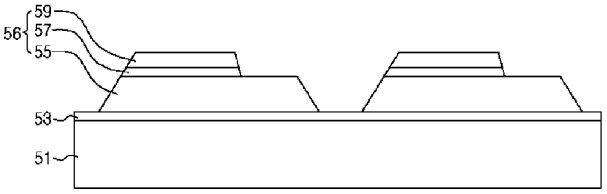
【도 3】


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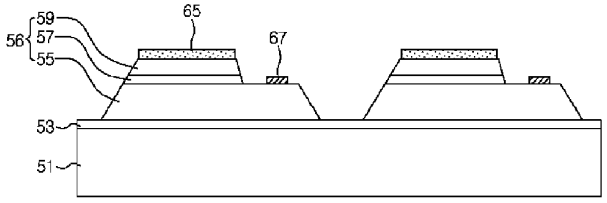
【도 4】


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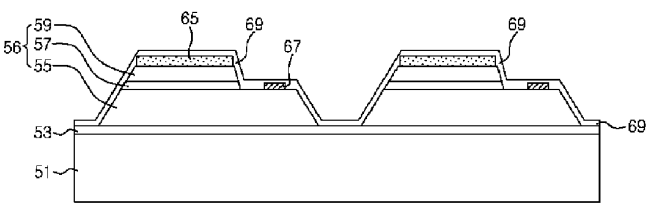
【도 5】


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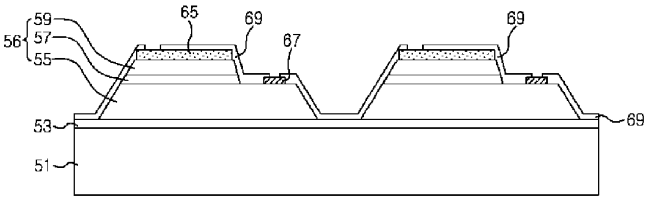
【도 6】


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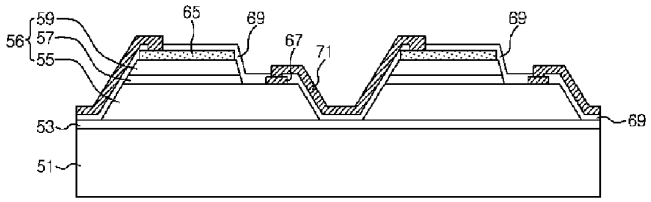
【도 7】


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【도 8】



【도 9】



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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(**Not for submission under 37 CFR 1.99)**

Application Number	12613275
Filing Date	2009-11-05
First Named Inventor	Jong Lam Lee
Art Unit	2818
Examiner Name	To be determined
Attorney Docket Number	P2317USD1

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	1	2004-071644	JP		2004-03-04	NICHIA CHEM IND LTD		☐
	2	2004-273746	JP		2004-09-30	HITACHI CABLE LTD		☐
	3	2005-136130	JP		2005-05-26	KYOCERA CORP		☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	12613275
	Filing Date	2009-11-05
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	To be determined
	Attorney Docket Number	P2317USD1

	4	2001-156331	JP		2001-06-08	NICHIA CHEM IND LTD		☐

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		☒

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Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	12613275
	Filing Date	2009-11-05
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	To be determined
	Attorney Docket Number	P2317USD1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

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PATENT ABSTRACTS OF JAPAN

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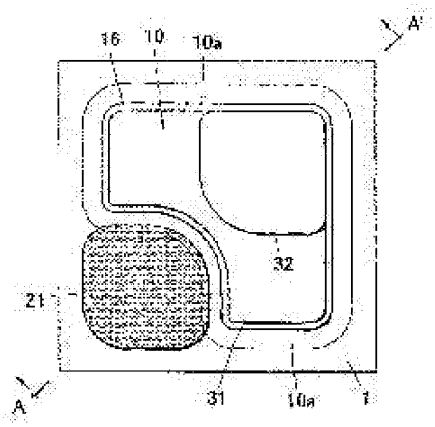
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(71)Applicant : NICHIA CHEM IND LTD
(72)Inventor : KUSUSE TAKESHI
SAKAMOTO TAKAHIKO

(54) NITRIDE SEMICONDUCTOR LIGHT EMITTING DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a nitride semiconductor light emitting device which ensures higher light emission efficiency and higher light emission efficiency.
SOLUTION: A nitride semiconductor light emitting device includes a laminated portion formed of an n-type semiconductor layer, an active layer, and a p-type semiconductor layer laminated on a substrate in order to emit the light. The side surface of the laminated portion is formed as a slope including the surface of the n-type semiconductor layer, and an n-type electrode is formed on the surface of the n-type semiconductor layer.



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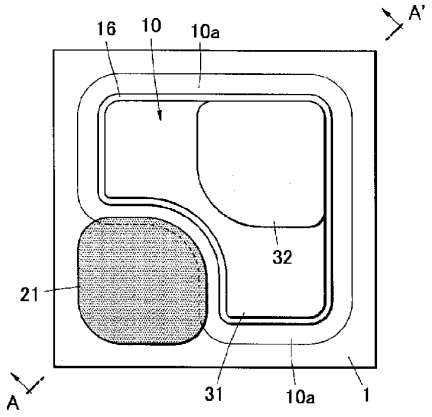
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(71)出願人　000226057
日亜化学工業株式会社
徳島県阿南市上中町岡４９１番地１００
(74)代理人　100074354
弁理士　豊栖　康弘
(74)代理人　100091465
弁理士　石井　久夫
(72)発明者　楠瀬　健
徳島県阿南市上中町岡４９１番地１００
日亜化学工業株式会社内
(72)発明者　坂本　貴彦
徳島県阿南市上中町岡４９１番地１００
日亜化学工業株式会社内

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(54)【発明の名称】窒化物半導体発光素子

(57)【要約】
【課題】発光効率が高くかつ光の出射効率が高い窒化物半導体発光素子を提供する。
【解決手段】基板上に、n型半導体層、活性層及びP型半導体層が積層されてなる積層部を有し、その積層部で発光する窒化物半導体発光素子において、積層部の側面は、n型半導体層の表面を含む傾斜面であり、そのn型半導体層の表面にn電極が形成されている。
【選択図】　図1



【特許請求の範囲】
【請求項１】
基板上に、ｎ型半導体層、活性層及びＰ型半導体層が積層されてなる積層部を有し、その積層部で発光する窒化物半導体発光素子において、
上記積層部の側面は、上記ｎ型半導体層の表面を含む傾斜面であり、そのｎ型半導体層の表面にｎ電極が形成されたことを特徴とする窒化物半導体発光素子。
【請求項２】
上記ｎ電極は上記積層部を囲むように形成された請求項１記載の窒化物半導体発光素子。
【請求項３】
上記ｎ電極を上記基板の側面から上記基板の下面にも連続して形成した請求項１又は２記載の窒化物半導体発光素子。
【請求項４】
上記積層部を円形とした請求項１～３のうちのいずれか１つに記載の窒化物半導体発光素子。
【請求項５】
上記積層部を六角形とした請求項１～３のうちのいずれか１つに記載の窒化物半導体発光素子。
【請求項６】
上記発光領域となる積層部を複数形成した請求項１～５のうちのいずれか１つに記載の窒化物半導体発光素子。
【請求項７】
上記各積層部に形成されたｎ電極は、互いに接続された共通電極として形成された請求項６記載の窒化物半導体発光素子。
【請求項８】
上記各積層部において形成された上記Ｐ型半導体層とオーミック接触するＰ側オーミック電極が互いに接続された請求項７記載の窒化物半導体発光素子。
【請求項９】
上記積層部を覆うように反射層を形成した請求項１，２，４～８のうちのいずれか１つに記載の窒化物半導体発光素子。
【請求項１０】
上記反射層は上記積層部を覆うように絶縁膜を介して金属層を形成することにより形成された請求項９記載の窒化物半導体発光素子。
【請求項１１】
上記金属層は、上記積層部のＰ型半導体層にそれぞれ形成されたＰオーミック電極を接続する接続電極である請求項１０記載の窒化物半導体発光素子。
【請求項１２】
上記反射層は誘電体多層膜からなる請求項９記載の窒化物半導体発光素子。
【請求項１３】
上記傾斜側面は、外側に膨らんだ凸曲面である請求項１～１２のうちのいずれか１つに記載の窒化物半導体発光素子。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】
本発明は、発光素子、特に窒化物半導体発光素子に関する。
【０００２】
【従来の技術】
近年、窒化ガリウム系化合物半導体を用いた発光ダイオードが、紫外域、青色等の比較的短い波長域を中心に広く用いられるようになって来ている。この窒化ガリウム系化合物半導体は直接遷移であり発光効率が高いことからもその適用範囲が拡大している。
【０００３】

【発明が解決しようとする課題】
しかしながら、窒化ガリウム系化合物半導体は通常、絶縁基板であるサファイア基板の上に成長されることに起因して、従来の窒化物半導体発光素子には以下のような課題があった。
第１に、サファイア基板が絶縁体であるために、ｎ側の電極とＰ側の電極をいずれも、サファイア基板上の窒化ガリウム半導体の上に形成する必要があり、特にｎ側の電極部分は、非発光領域となり、発光領域から生じた光が、ＧａＮ層を横方向に伝播する際の多重反射により吸収され、取り出し効率を低下させるという問題点があった。
第２に、発光した光は基板面に対して通常は垂直方向に取り出すように構成されるが、発光ダイオードの側面から出射される光の割合が比較的高く、発光した光を効果的に利用することができないという問題があった。
【０００４】
そこで、本発明は、ｎ側電極下部での多重反射をなくし、ｎ側の電極による吸収を低減し、取り出し効率の高い窒化物半導体発光素子を提供することを第１の目的とする。
また、本発明は発光した光を効果的に利用することができる窒化物半導体発光素子を提供することを第２の目的とする。
【０００５】
【課題を解決するための手段】
以上の従来の問題点を解決するために、本発明に係る窒化物半導体発光素子は、基板上に、ｎ型半導体層、活性層及びＰ型半導体層が積層されてなる積層部を有し、その積層部で発光する窒化物半導体発光素子において、
上記積層部の側面は、上記ｎ型半導体層の表面を含む傾斜面であり、そのｎ型半導体層の表面にｎ電極が形成されたことを特徴とする。
以上のように構成された窒化物半導体発光素子は、光の出射効率を高くできる。
【０００６】
本発明に係る窒化物半導体発光素子では、上記ｎ電極は上記積層部を囲むように形成されていることが好ましい。
【０００７】
また、本発明に係る窒化物半導体発光素子では、上記ｎ電極を上記基板の側面から上記基板の下面にも連続して形成することができる。このようにすると、Ｐ側オーミック電極を透光性電極としてその透光性電極を介して光を出射させる場合に、上記基板の側面及び上記基板の下面で反射した光も透光性電極を介して出力できるので、光の取り出し効率を高くできる。
【０００８】
また、本発明に係る窒化物半導体発光素子では、上記発光領域となる積層部を複数形成することもでき、これにより、大面積でかつ発光効率の高い窒化物半導体発光素子を構成できる。
【０００９】
上記積層部を複数形成した窒化物半導体発光素子では、上記各積層部に形成されたｎ電極を互いに接続して共通電極として形成することができる。
これにより、上記発光領域である積層部を容易に並列接続することが可能となる。
また、上記積層部を複数形成した窒化物半導体発光素子では、上記ｎ電極を互いに接続して共通電極として形成するとともに、上記各積層部において形成された上記Ｐ型半導体層とオーミック接触するＰ側オーミック電極を互いに接続することもできる。
これにより、上記発光領域である積層部が素子上で並列接続された窒化物半導体発光素子を提供できる。
【００１０】
また、本発明に係る窒化物半導体発光素子において、基板側から光を出力するように構成する場合には、光の出射効率を高くするために、上記積層部を覆うように反射層を形成することが好ましい。

【００１１】
また、上記窒化物半導体発光素子において、上記金属層は、上記積層部のＰ型半導体層にそれぞれ形成されたＰオーミック電極を接続する接続電極により構成することができる。
【００１２】
本発明に係る窒化物半導体発光素子において、上記反射層は上記積層部を覆うように絶縁膜を介して金属層を形成することにより形成してもよいし、誘電体多層膜により構成するようにしても良い。
【００１３】
本発明に係る窒化物半導体発光素子において、上記傾斜側面は、外側に膨らんだ凸曲面とすることもできる。
【００１４】
【発明の実施の形態】
以下、図面を参照しながら本発明に係る実施の形態の窒化物半導体発光素子について説明する。
実施の形態１．
本発明に係る実施の形態１の窒化物半導体発光素子は、図１及び図２に示すように、発光領域を構成する積層部１０の側面を内側に傾斜した傾斜面１０αとし、その傾斜面１０αに露出したｎ型コンタクト層１２とオーミック接触するようにｎ電極２１を形成することにより構成されている。
【００１５】
実施の形態１の窒化物半導体発光素子において、積層部１０は、図２に示すように、サファイア基板１上に、バッファ層１１、ｎ型コンタクト層１２、ｎ型クラッド層１３、発光層１４、Ｐ型クラッド層１５及びＰ型コンタクト層１６を順次成長させて積層構造を形成し、図１に示す平面形状（略矩形形状において、１つの隅部が円弧状に切り欠かれた形状）になるようにエッチングすることにより形成される。
【００１６】
積層部１０を構成する各層は例えば次のようなもので形成する。
バッファ層１１：４００℃～６００℃の低温で成長されたＧａＮ又はＡｌＧａＮ層、
ｎ型コンタクト層１２：Ｓｉドープのガ（例えば、厚さ６μｍ）、
ｎ型クラッド層１３：ｎ型ＡｌＧａＮ、
発光層１４：ノンドープのＩｎＧａＮ井戸層を含む（例えば、厚さ約３０Å）単一又は多重量子井戸構造、
Ｐ型クラッド層１５：Ｐ型ＡｌＧａＮ、
Ｐ型コンタクト層１６：Ｍｇがドープされたガ（例えば、厚さ約１２００Å）。
【００１７】
また、本実施の形態１において、積層部１０を形成するためのエッチングは、サファイヤの表面が露出するまで行い、積層部１０が円弧状に切り欠かれた１つの隅部にｎ電極２１を形成するためにサファィヤ基板表面を露出させる。尚、本実施の形態１では、ｎ電極２１を形成するために露出されたサファイア基板の表面と連続して積層部１０の周りを取り囲むようにサファィヤ基板の表面が露出される。
【００１８】
本実施の形態１において、ｎ電極２１は、図１及び図２に示すように、積層部１０の１つの隅部に露出させたサファィヤ基板１の表面から積層部１０の傾斜面１０αに亙って連続して形成し、傾斜面１０αに露出したｎ型コンタクト層１２とオーミック接触する。
また、Ｐ側の電極は全面電極３１とＰパッド電極３２とからなり、全面電極３１は積層部１０の最上層に位置するＰ型コンタクト層１６の表面のほぼ全面に形成され、Ｐパッド電極３２は全面電極３１上のｎ側電極２１と対角をなす位置（他方の隅部）に形成される。
【００１９】
以上のように構成された実施の形態１の窒化物半導体発光素子は、ｎ電極２１による光の吸収を極めて少なくできるので、効率良く光を出力できる。

すなわち、図２１に示す従来の構造では、基板１とｎ電極５２１の間に存在するｎ型コンタクト層５１２に発光領域で発光した光が漏れ出して導波し、基板１の上面とｎ電極１２１の裏面により繰り返して反射される間に（図２１において、Ｙ１００の符号を付して模式的に示す）、大部分の光がｎ電極１２１によって吸収されて結局外部に取り出すことができないという問題があった。しかしながら、本発明では、傾斜側面１０αに露出されたｎ型コンタクト層１２の表面でｎ電極をオーミック接触させることにより、ｎ型コンタクト層１２において光が導波する部分を無くし（図２において、Ｙ１の符号を付して模式的に示す）、従来の問題点を解決している。

また、発光した光を基板側から出射させる場合に、積層部１０の傾斜側面１０αで反射した光も基板を介して出力することができ、出射効率を向上させることができる。

【００２０】

また、発光した光を基板側から出射させる場合に、傾斜側面１０αで効果的に反射させるためには、傾斜側面１０αには通常ＳｉＯ２保護膜が形成されていることを考慮すると、傾斜側面１０αの傾斜角αを６０度以下に設定することが好ましく、４５度以下に設定することがより好ましい。

この傾斜角αは本明細書では、図２２に示すように定義し、その好ましい範囲は、臨界角θｃが$\mathrm{Sin}\theta c = n_S / n_G$（$n_G$：活性層の屈折率、$n_S$：ＳｉＯ２保護膜の屈折率）で与えられることから、求めることができる。

例えば、波長３８０ｎｍの光を発光する素子の場合、波長３８０ｎｍの光に対する$Al_xGa_{1-x}N$の屈折率は、Ｘの値が１～０の範囲であるとすると２．１５～２．８０である。この時、臨界角θｃが最も小さくなるのは、屈折率が２．８０の場合であり、この時の臨界角θｃは約３０°である。

従って、臨界角θｃを３０°以上、すなわち、傾斜角αを６０°以下に設定すると、少なくとも半導体層に平行に伝播される最も強い光は全反射されることになる。

以上のように傾斜角αを６０°以下に設定すると半導体層と平行に伝播される最も強い光は全反射されて取り出し効率を向上させることができる。しかしながら、層内を伝播される光には半導体層に平行でない光もあり、それらも効果的に全反射させるためには、傾斜角αを４５度以下に設定することがさらに好ましい。

また、傾斜側面１０αにｎ電極を形成することを考慮した場合における、傾斜側面１０αの傾斜長Ｌの上から見た投影長Ｗは、１０μｍ以上であることが好ましい。

【００２１】

以上の説明では、１つの隅部において、ｎ電極２１とｎ型コンタクト層１２とがオーミック接触するように形成した例について説明したが、本実施の形態１では、図３及び図４に示すように、ｎ電極２２は積層部１０を囲むように形成することが好ましい。このようにすると、発光領域全体に均一に電流を注入することができ、効率良く発光させることができる。

【００２２】

実施の形態２．

本発明に係る実施の形態２の窒化物半導体発光素子は、図５に示すように、発光領域を構成する積層部１１０の形状を円形にしたものである。本実施の形態２の窒化物半導体発光素子において、ｎ電極２３が積層部１１０の内側に傾斜した側面である傾斜面１１０αに露出したｎ型コンタクト層１２とオーミック接触するように形成されている点は、実施の形態１と同様である。

【００２３】

また、実施の形態２の窒化物半導体発光素子において、積層部１１０の積層構造（半導体層の構成）は実施の形態１の発光素子と同様であり、積層部１１０を形成するためのエッチングは、サファイヤの表面が露出するまで行う。

実施の形態２において、Ｐ側の電極は全面電極３３とＰパッド電極３４とからなり、全面電極３３は積層部１１０の最上層に位置するＰ型コンタクト層１６の円形表面のほぼ全面に形成され、Ｐパッド電極３４は全面電極３３中央部に形成される。

ここで、全面電極３３、Ｐパッド電極３４及び円形の積層部１１０は中心が一致するように同心円状に形成される。

【００２４】

以上のように構成された実施の形態２の窒化物半導体発光素子は、実施の形態１の発光素子と同様の作用効果を有する。

すなわち、ｎ電極２３による光の吸収を極めて少なくでき、効率良く光を出力できるとともに、積層部１１０の傾斜側面１１０αで反射した光も基板を介して出力することができ、出射効率を向上させることができる。

さらに、本実施の形態２では、図５から明らかなように、ｎ電極２３は積層部１１０を囲むように形成しているので、発光領域全体に均一に電流を注入することができ、効率良く発光させることができる。

【００２５】

実施の形態３.

本発明に係る実施の形態３の窒化物半導体発光素子は、図６、図７に示すように、発光領域を構成する積層部１１０の形状を円形にしたものであるが、本実施の形態２の窒化物半導体発光素子とは、以下の点が異なる。

すなわち、実施の形態３の窒化物半導体発光素子では、Ｐ型コンタクト層の表面に透光性を有する透光性オーミック電極３３αを形成し、その上にＰパッド電極３４を形成している。

また、実施の形態３の窒化物半導体発光素子では、図７に示すように、傾斜側面１１０αでｎ型コンタクト層とオーミック接触するｎ電極２４を基板１の側面及び裏面に連続して形成している。

この実施の形態３において、透光性オーミック電極３３αとｎ電極２４以外は、実施の形態２と同様に構成される。

【００２６】

以上のように構成された実施の形態３の窒化物半導体発光素子は、積層部１１０で発光した光を透光性オーミック電極３３αを介して出力することができ、以下のような効果を有する。

すなわち、ｎ電極２４による光の吸収を極めて少なくでき、効率良く光を出力でき、基板の側面及び裏面に形成されたｎ電極２４により光を反射して透光性オーミック電極３３αを介して出力できるので、出射効率を向上させることができる。

また、本実施の形態３では、図６から明らかなように、ｎ電極２４を積層部１１０を囲むように形成しているので、発光領域全体に均一に電流を注入することができ、効率良く発光させることができる。

【００２７】

以上の実施の形態３の窒化物半導体発光素子では、ｎ電極２４により基板全体が覆われるように構成したが、本発明はこれに限られるものではなく、図８に示すように、ｎ電極２５と基板１を覆う電極２６とを別の金属で構成してもよい。

以上のように構成しても実施の形態３と同様の作用効果が得られ、さらに以下のような効果がある。

すなわち、ｎ電極２５はｎ型コンタクト層と良好なオーミック接触が得られる金属から選択して構成し、基板１を覆う電極２６には、その機能に応じて適切な金属材料を選択して構成することができる。

具体的には、基板１の裏面をはんだ付けにより実装する場合には、電極２６の材料としてはんだ耐熱性の優れた材料を選択したり、光の反射を重視する場合には反射率の高い金属を選択して用いることができる。

【００２８】

実施の形態４.

本発明に係る実施の形態４の窒化物半導体発光素子は、図９に示すように、発光領域を構成する積層部１１１の形状を矩形にしたものである。

すなわち、実施の形態３の窒化物半導体発光素子では、Ｐ型コンタクト層の表面に全面電極３５を形成し、その上にＰパッド電極３６を形成している。
また、図９に示すように、矩形の積層部１１１の傾斜側面１１１αでｎ型コンタクト層とオーミック接触するｎ電極２７を基板の表面とｎ型コンタクト層（傾斜側面１１１αに露出したもの）とに亙って形成している。
尚、実施の形態４において、積層部の積層構造は実施の形態１～３と同様に構成される。
【００２９】
以上のように構成された実施の形態４の窒化物半導体発光素子は、実施の形態１～３と同様の作用効果を有する。
また、図９の窒化物半導体発光素子では、ｎ電極２７は積層部１１１の一辺でｎコンタクト層に接触するように形成したが、本実施の形態４では、図１０に示すように、積層部１１１の外周全体でｎコンタクト層とオーミック接触するようにｎ電極２８を形成することもでき、これにより、発光領域全体に均一に電流を注入することができ、効率良く発光させることができる。
【００３０】
実施の形態５．
実施の形態５の窒化物半導体発光素子は、図１１，図１２に示すように、複数（図１１，１２では１８個）の積層部２１０を備えた発光面積の大きい発光素子であって、素子全体の面積に占める発光領域の面積を大きくでき、発光領域全体を均一に発光させることができるという特徴を有する。
図１１は主としてｎ電極２２１の形態を示すために、Ｐ側ボンディング電極２５１及びＰ側接続電極２６１を省いて示す平面図であり、図１２はＰ側ボンディング電極２５１及びＰ側接続電極２６１を省略せずに示す平面図である。また、図１３は、図１２のＤ－Ｄ’線についての断面図である。
【００３１】
このように、発光領域を複数の部分に分割して形成するのは、大面積の発光領域を分割することなく１つの大きな領域として形成した場合に生じる、電極から離れた部分で電流が低下して発光効率が悪くなるという問題を解決するためである。しかしながら、発光領域を複数の部分に分割して形成した場合には、各発光領域間を接続する電極面積が大きくなり、いかにして発光領域の面積を確保するかが課題となる。また、図２１に示す構造の従来の素子を複数個並べた場合には、ｎ型コンタクト層を光が導波して反射を繰り返すうちにｎ電極により吸収される光により発光効率が低下する。しかしながら、本実施の形態５の窒化物半導体発光素子では、第１に各積層部の傾斜した側面にｎ型コンタクト層とオーミック接触するｎ電極を形成することにより、ｎ電極が必要とする面積を小さくして発光領域の面積を確保し、かつｎ電極による光の吸収を防止している。
【００３２】
また、本実施の形態５の窒化物半導体発光素子では、Ｐ側の全面電極による吸収も従来例に比較して抑えることができる。
すなわち、大面積の発光領域を分割することなく１つの大きな領域として形成した従来例では、図２３（ｂ）に示すように、臨界角以上でＰ側の全面電極に入射された光は、Ｐ側の全面電極７３１と、基板１と半導体層との間の境界の間で反射を繰り返すうちに、かなりの部分がＰ側の全面電極により吸収される。
また、発光領域を複数の部分に分割して形成した場合であっても、分割された発光領域が傾斜した側面を有していない場合には、図２３（ｃ）に示すように、臨界角以上でＰ側の全面電極７３１に入射された光が基板に略垂直な側面から出射されて隣接する発光領域に再入射される確率が高くなる。そのためにＰ側の全面電極により吸収される率が高くなる。
これに対して、本実施の形態５の窒化物半導体発光素子は、各発光領域が傾斜側面を有しているので、基板側から発光させる場合には、図２３（ａ）においてＡ２の符号を付して示す光のように、また、電極側から発光させる場合には、図２３（ａ）においてＡ３の符

号を付して示す光のように、隣接する発光領域に再入射されることなく（隣接する発光領域に再入射される確率を低くできる）、外部に出射される。これにより、Ｐ側の全面電極３１で吸収される率を低くできる。

【００８３】

また、実施の形態５の窒化物半導体発光素子では、発光領域を構成する積層部２１０の形状を六角形とし、その複数の積層部２１０は積層部間の面積が最も小さくなるように配列される（図１１，１２）。本実施の形態５において、隣接する積層部２１０間は基板の表面までエッチングされており（図１３）、複数の積層部２１０はそれぞれ完全に分離されている。尚、隣接する積層部２１０間の間隔は、例えば、１０μｍに設定される。

また、実施の形態５において、各積層部２１０の側面は、実施の形態１等と同様に全て傾斜面２１０αであり、その傾斜面２１０αに露出されたｎ型コンタクト層にオーミック接触するようにｎ電極２２１が形成される。

実施の形態５において、ｎ電極２２１は図１１に示すように全ての積層部２１０を取り囲むように一体として形成される。

【００８４】

実施の形態５において、各積層部２１０のＰ型コンタクト層のほぼ全面に全面電極２３１が形成され、その中央部にＰパッド電極２３２が形成される。そして、Ｐパッド電極２３２上に開口部を有する絶縁膜２７１が素子全体を覆うように形成され、その絶縁膜２７１上にＰパッド電極２３２を互いに接続する接続電極２６１（一端がＰ側ボンディング部に接続）が形成される。尚、絶縁膜２７１はｎ電極２２１のうちボンディング部２４１を開口させる開口部も有している。

【００８５】

以上のように構成された実施の形態５の窒化物半導体発光素子は、発光領域である積層部２１０の形状を六角形とし、その積層部２１０間の面積が最も小さくなるように配列し、かつ各積層部２１０の傾斜した傾斜側面にｎ電極を形成することにより、発光領域の面積が大きくなるように構成している。

これにより、発光領域を効果的に発光させることができる適切な大きさの複数の部分に分割し、かつｎ電極を形成するために必要となる面積を抑制することが可能となる。従って、発光領域の面積を低下させることなく、かつ各発光領域を効率よく発光させることができ、高い輝度を有する大面積の発光素子を構成できる。

【００８６】

実施の形態５の窒化物半導体発光素子は、基板側から光を出射するようにしても良いし、全面電極２３１を透明電極とすることにより半導体側から光を出射するようにしても良い。いずれの場合についても、発光層で発光した光は基板側とＰ型半導体側の両方に伝播されるので、出射側とは反対側に反射膜を形成することが好ましく、これにより出射効率を向上させることができる。

【００８７】

図１４は、本実施の形態５の窒化物半導体発光素子において、接続電極２６１間を更に接続する第２接続電極２６２を形成したものである。この第２接続電極２６２はＰ側ボンディング部２５１から離れた位置にある積層部２１０における電流注入量が低下するのを防止するために形成するものであり、各積層部の発光強度を均一化するものである。

しかしながら、半導体層側から光を出射させる場合には、この第２接続電極２６２が光を遮ることになるので、本構成は基板側から光を出射する場合に特に適している。

【００８８】

図１５は、半導体層側から光を出射させる場合に適した接続電極の例を示すものである。本例では、Ｐ側ボンディング部２５１に接続された第１接続電極２６３を積層部２１０の間のｎ電極上に絶縁膜を介してｎ電極と導通しないようにして形成する。この第１接続電極２６３は積層部上には形成されないので、積層部で発光した光を遮ることはない。そして、各積層部２１０のＰパッド電極と第１接続電極２６３の間は第２接続電極２６４により接続される。ここで、１つのＰパッド電極２３２と第１接続電極２６３の間は、１つの

第２接続電極２６４で接続されている。

【００３９】

図１６は、基板側から光を出射する場合の電極構造のより好ましい例を示したものである。

すなわち、図１６の窒化物半導体発光素子では、実施の形態５（図１２）の接続電極２６１（Ｐ側ボンディング部を含む）に替えて、絶縁膜２７１の上から複数の積層部を全て覆う電極層２６５を形成している。

このようにすると、各積層部の上面、特に傾斜側面からの光の漏れを防止でき（各積層部の上面及び傾斜側面で反射させることができ）、基板側から効率良く光を出射できる。

【００４０】

以上の実施の形態５の窒化物半導体発光素子では、各積層部２１０を六角形に形成した例により示したが、四角形又は円形等の他の形状であってもよい。

図２４は、積層部４１０を四角形にした具体例を示す平面図である。本例では、Ｐ側ボンディング部４５１を２つの隅部に形成された積層部４１０上にそれぞれ設け、そのＰ側ボンディング部４５１に接続された接続電極４６１により、積層部４１０のＰパッド電極間が接続される。尚、接続電極４６１は、積層部４１０の間のｎ電極上に絶縁膜を介してｎ電極と導通しないようにして形成される。

また、ｎ電極４２１は、全ての積層部４１０を取り囲むように一体として形成し、各積層部４１０の傾斜面４１０ａに露出されたｎ型コンタクト層とオーミック接触するように形成され、その一部にｎパッド電極４４１が形成される。

【００４１】

実施の形態６．

図１７は実施の形態６の窒化物半導体発光素子の全体構成を示す平面図であり、図１８は１つの積層部３１０を拡大して示す平面図である。また、図１９（ａ）は図１８のＥ－Ｅ’線についての断面図であり、図１９（ｂ）は図１８のＦ－Ｆ’線についての断面図である。

実施の形態６の窒化物半導体発光素子において、積層部３１０はそれぞれ円形形状に形成され、その中心が縦横とも１つの直線上に位置するように基板上に配列される。また、各積層部３１０の積層構造は他の実施の形態と同様であり、その外周側面は内側に傾いた傾斜面（外周傾斜面３１０ａ）とされ、その断面形状は、図１９（ａ）（ｂ）に示すように、上面を上底とする台形である。

【００４２】

各積層部３１０において、ｎオーミック電極３２１ａは外周傾斜面３１０ａに露出されたｎ側コンタクト層とオーミック接触するように外周傾斜面３１０ａの全周に形成される。また、積層部３１０の間の基板上にはそれぞれｎ接続パッド３２１ｂが形成され、各積層部３１０に形成されたｎオーミック電極３２１ａは隣接する４つのｎ接続パッド３２１ｂと接続される。

すなわち、実施の形態６の窒化物半導体発光素子において、ｎ電極３２１はｎオーミック電極３２１ａとｎ接続パッド３２１ｂとからなる。

また、各積層部３１０の上面（Ｐコンタクト層の上面）のほぼ全面に、全面電極３３１が形成され、その全面電極３３１の中央部に円形のＰパッド電極３３２が形成される。

【００４３】

以上のように、ｎオーミック電極３２１ａ、ｎ接続パッド電極３２１ｂ、全面電極３３１及びＰパッド電極３３２を形成した後、接続パッド電極３２１ｂとその周辺及びＰパッド電極３３２の上面を除いて素子全体を覆う絶縁膜３７１を形成して、各積層部３１０のＰパッド電極３３２を互いに接続するＰ側接続電極３６１を形成する。尚、Ｐ側接続電極３６１は、Ｐパッド電極３３２上に接続されたパッド接続部３６１ｂとそのパッド接続部３６１ｂ間を接続する接続部３６１とからなる。

【００４４】

以上のように構成された実施の形態６の窒化物半導体発光素子は、実施の形態１と同様、

電極による吸収を防止でき、発光した光の取り出し効率を高くできる。
実施の形態６の窒化物半導体発光素子における光の取り出し効率を確認するために以下の比較検討を行った。
【００４５】
まず、本実施の形態６の窒化物半導体発光素子として、図２５の平面図に示す積層部３１０を９個（３×３個）形成した素子を作製し、積層部３１０が１つの場合の発光素子（図２８の平面図に示す）と取り出し効率の比較を行った。
取り出し効率の測定は、図３０に示すように、マイナス側端子と一体で構成されたカップ内に発光素子をダイボンディングし、ｎパッド電極とマイナス側端子Ｔ２とをボンディングワイヤーＷ２１で接続し、Ｐパッド電極とプラス側端子Ｔ１とをボンディングワイヤーＷ３２で接続して、発光光量に対する外部に取り出される光量を測定した。
【００４６】
その結果、９個の積層部３１０を形成した実施の形態６の素子（図２５）の取り出し効率は、積層部３１０が１つの場合の発光素子（図２８）の取り出し効率を１００とした場合、８６％であった。
これに対して、比較例として作製した図２６に示す発光素子（９個の積層部を形成した素子）の取り出し効率は、図２９（ａ）に示す１つの積層部を備えた発光素子の取り出し効率を１００とした場合、７１％であった。
尚、積層部３１０が１つの場合の発光素子（図２８）の取り出し効率と、図２９（ａ）に示す１つの積層部を備えた発光素子の取り出し効率とはほぼ等しいものであった。
【００４７】
ここで、比較例の発光素子において、各積層部は実施の形態６と同様の積層構造を有し、その平面形状は略矩形に形成されている。また、ｎ電極５２１は、各積層部の１つの隅部において、ｎ型コンタクト層の表面を露出させ、その露出させた表面に形成されている。さらに、Ｐオーミック電極５３１はＰ型コンタクト層のほぼ全面に形成され、Ｐオーミック電極５３１上のｎ電極５２１と対角をなす位置にＰパッド電極５３２が形成されている。尚、図２６に示す素子では、隣接する積層部の間はサファイア基板が露出されるまでエッチングされて、隣接する積層部の間は完全に分離されている。また、各積層部の側面は、サファイア基板の上面に対してほぼ垂直に形成されている。
【００４８】
以上のように、複数の積層部を備えた実施の形態６の窒化物半導体発光素子は、同じく集合状態の比較例の窒化物半導体発光素子に比較して、取り出し効率を高くできることが確認された。
【００４９】
また、図２７は異なる比較例として作製した素子であって、図２６に示す比較例の発光素子において、隣接する積層部間においてサファイア基板が露出するまでエッチングせずに、ｎ型コンタクト層を残すようにしたものである。この図２７の比較例の素子の取り出し効率は、図２９（ｂ）に示す１つの積層部を備えた発光素子の取り出し効率を１００とした場合、６８％であった。
尚、図２９（ａ）の素子の取り出し効率と、図２９（ｂ）の素子の取り出し効率とはほぼ等しいものであった。
以上のように、複数の積層部を備えた比較例の発光素子は、いずれも実施の形態６の発光素子より取り出し効率が悪いものであった。
【００５０】
また、実施の形態６の窒化物半導体発光素子は、実施の形態５の発光素子と同様の作用効果を有し、さらに以下のような特徴を有する。
すなわち、ウエハ上に各積層部を形成した後に、要求に応じて必要な個数の積層部３１０を含む任意の大きさの素子に分割することができるので、同一のパターンにより任意の大きさの素子を作製することが可能となる。
尚、この場合、いずれかの位置にあるｎ接続パッド電極３２１ｂとパッド接続部３６１ｂ

とをボンディング電極として用いることができる。

【００５１】

以上の各実施の形態の窒化物半導体発光素子は、上述したように、基板側から光を出力するようにも構成できるし、また、半導体側から光を出力するようにも構成できる。いずれの場合についても、光を出射する方向の反対側の面には、反射層を形成することが好ましい。図７、図８及び図１６に示す構造の場合にはそれぞれ、ｎ電極２４、電極２６又は電極２６５を反射層として機能させることができることは上述した通りであるが、他の構成の場合には、反射層を別途設けることが好ましい。この反射層は、反射率の高い金属を用いて構成することもできるし、誘電体多層膜を用いて構成することもできる。誘電体多層膜を用いる場合には、例えば、図１８の絶縁層２７１を誘電体多層膜により構成することにより、絶縁機能に加え、反射機能を持たせるようにしても良い。

【００５２】

実施の形態７．

図３１は実施の形態７の窒化物半導体発光素子の全体構成を示す平面図である。実施の形態７の窒化物半導体発光素子において、積層部３１０はそれぞれ円形形状に形成され、その中心が単位格子が六角形の格子点に位置するように基板上に配置される。また、各積層部６１０の積層構造は他の実施の形態と同様であり、その外周側面は内側に傾いた傾斜面とされている。

【００５３】

各積層部６１０において、ｎオーミック電極６２１ａは外周傾斜面に露出されたｎ側コンタクト層とオーミック接触するように外周傾斜面の全周に形成される。また、６つの積層部６１０に囲まれた各六角形格子の中心には、それぞれｎ接続パッド６２１ｂが形成され、各積層部６１０に形成されたｎオーミック電極６２１ａは隣接する３つのｎ接続パッド６２１ｂと接続される。

すなわち、実施の形態７の窒化物半導体発光素子において、ｎ電極はｎオーミック電極６２１ａとｎ接続パッド６２１ｂとからなる。

また、各積層部６１０の上面（Ｐコンタクト層の上面）のほぼ全面に、全面電極が形成され、その全面電極の中央部に円形のＰパッド電極６３２が形成され、各積層部６１０のＰパッド電極６３２はＰ側接続電極３６１により互いに接続される。

【００５４】

尚、ｎオーミック電極６２１ａ、ｎ接続パッド電極６２１ｂ等のｎ側の電極と、全面電極６３１、Ｐパッド電極６３２、Ｐ側接続電極３６１等のＰ側の電極とは実施の形態６と同様にして絶縁される。

以上のように構成された実施の形態７の窒化物半導体発光素子では、１つのｎ接続パッド電極６２１ｂに対して２つの積層部が設けられており、１つのｎ接続パッド電極に対して１つの積層部が設けられた実施の形態６に比較して、発光素子全体としての発光領域の面積を大きくできる。

また、この実施の形態７のように積層部を配置した場合、外形形状が、三角形、六角形、ひし形、平行四辺形等になるように分割することができ、そのように分割する際、ＧａＮ結晶の結晶軸の方向とスクライブラインの方向を一致させることができるので、分割時の歩留まりを向上させることができる。

【００５５】

次に、上記各実施の形態の窒化物半導体発光素子において、傾斜側面を有する積層部の形成方法の一例を示す。

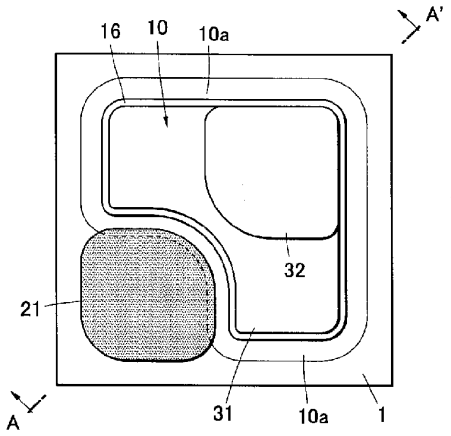
本方法では、まず、サファイア基板１の上に、バッファ層１１、ｎ型コンタクト層１２、ｎ型クラッド層１３、発光層１４、Ｐ型クラッド層１５及びＰ型コンタクト層１６を順次成長させて積層構造を形成し、その上に、図２０（ａ）に示すように、断面が台形形状のマスクＭ１を形成する。

次に、反応性イオンエッチングにより、マスクＭ１の上から積層体をエッチングする。この時、積層体をエッチングすると同時にマスクそのものもエッチングにより少しづつ除去

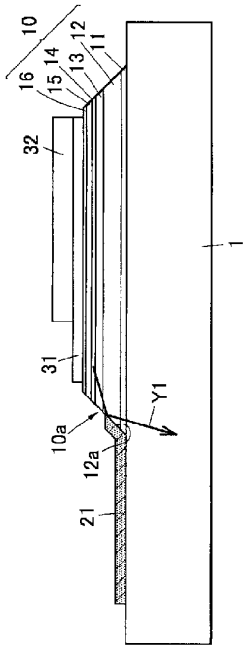
する。図２０（ｂ）において、破線と実線の間のＲ１の符号を付した部分が除去された部分である。
この工ッチングを積層部１０の周りの基板表面が露出されるまで続ける（図２０（ｃ））。
このようにすると、マスクＭ１の形状に対応した形状の、傾斜側面１０αを有する積層部１０が形成される。
本方法では、マスク材料と窒化物半導体材料のＲＩＥによる工ッチング率を考慮して、マスクＭ１形状を設定することにより、所望の傾斜側面を有する積層部が形成できる。
【００５６】
例えば、マスクＭ１の側面を外側に膨らんだ形状とすることにより、積層部の傾斜側面を外側に膨らんだ凸曲面とすることができる。
このように、傾斜側面を外側に膨らんだ凸曲面とすることにより、基板側から光を出力する場合に集光して光を出射できる。
【００５７】
以上の各実施の形態では、最も好ましい例として、積層部の周りを基板まで工ッチングした例を用いて説明したが、本発明においては積層部の周りに光が伝送されないようにすることが重要であり、光の伝送を抑制できる程度の厚さにｎ型半導体層が残っていても良い。
【００５８】
【発明の効果】
以上詳細に説明したように、本発明に係る窒化物半導体発光素子は、傾斜した側面を持った積層部を有し、その積層部の側面のｎ型半導体層の表面にｎ電極を形成することによりｎ電極による光の吸収を抑制でき、光の出射効率を高くできる。
【図面の簡単な説明】
【図１】本発明に係る実施の形態１の発光素子の平面図である。
【図２】図１のＡ－Ａ’線についての断面図である。
【図３】本発明に係る実施の形態１の変形例の発光素子の平面図である。
【図４】図３のＢ－Ｂ’線についての断面図である。
【図５】本発明に係る実施の形態２の発光素子の平面図である。
【図６】本発明に係る実施の形態３の発光素子の平面図である。
【図７】図６のＣ－Ｃ’線についての断面図である。
【図８】実施の形態３の変形例に係る発光素子の断面図である。
【図９】本発明に係る実施の形態４の発光素子の平面図である。
【図１０】実施の形態４の変形例に係る発光素子の平面図である。
【図１１】本発明に係る実施の形態５の発光素子において、Ｐ側の電極を省いて示す平面図である。
【図１２】本発明に係る実施の形態５の発光素子の平面図（Ｐ側の電極を含む）である。
【図１３】図１２のＤ－Ｄ’線についての断面図である。
【図１４】実施の形態５の第１変形例に係る発光素子の平面図である。
【図１５】実施の形態５の第２変形例に係る発光素子の平面図である。
【図１６】実施の形態５の第３変形例に係る発光素子の平面図である。
【図１７】本発明に係る実施の形態６の発光素子の平面図である。
【図１８】図１７の一部を拡大して示す平面図である。
【図１９】（ａ）は図１８のＥ－Ｅ’線についての断面図であり、（ｂ）は図１８のＦ－Ｆ’線についての断面図である。
【図２０】本発明の窒化物半導体発光素子において、傾斜側面を有する積層部の形成方法の一例を示す工程図である。
【図２１】従来例の発光素子の断面図である。
【図２２】本発明の窒化物半導体発光素子において、傾斜側面の好ましい傾斜角について説明するための模式図である。

【図２３】本発明の窒化物半導体発光素子において、Ｐ電極による光の吸収が抑制できることを説明するための図である。
【図２４】実施の形態５の第４変形例に係る発光素子の平面図である。
【図２５】本発明に係る実施の形態６において、取り出し効率の測定に用いた発光素子の平面図である。
【図２６】本発明に係る実施の形態６の比較例（その１）として、取り出し効率の測定に用いた発光素子の平面図である。
【図２７】本発明に係る実施の形態６の比較例（その２）として、取り出し効率の測定に用いた発光素子の平面図である。
【図２８】本発明に係る実施の形態６の取り出し効率の測定において、基準として用いた発光素子の平面図である。
【図２９】本発明に係る実施の形態６において、比較例の基準として用いた発光素子の平面図である。
【図３０】本発明に係る実施の形態６の取り出し効率の測定方法の概要を示す模式図である。
【図３１】本発明に係る実施の形態７の発光素子の平面図である。
【図３２】実施の形態７の発光素子の一部を拡大して示す平面図である。
【符号の説明】
１　サファイア基板、
１０，１１０，１１１，２１０，３１０　積層部、
１０ａ，１１０ａ，１１１ａ，２１０ａ，３１０ａ　傾斜面（傾斜側面）、
１１　バッファ層、
１２　ｎ型コンタクト層、
１３　ｎ型クラッド層、
１４　発光層、
１５　Ｐ型クラッド層、
１６　Ｐ型コンタクト層、
２１，２２，２３，２４，２５，２７，２８，２２１，３２１　ｎ電極、
３１，３３，３５　全面電極、
３２，３４，３６　Ｐパッド電極、
３３ａ　透光性オーミック電極。

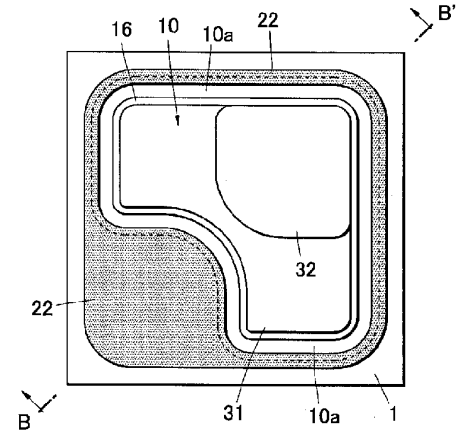
【図１】


16
10
10a
A'
32
21
A
31
10a
1

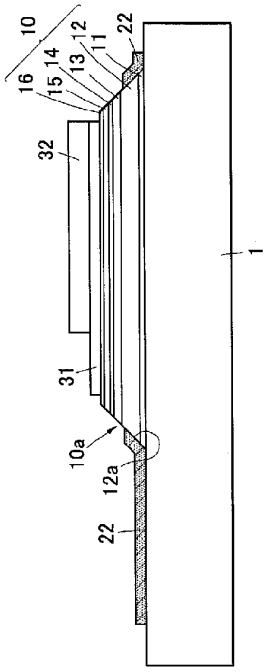
【図２】


10
12
11
14
13
16
15
32
1
31
Y1
10a
12a
21

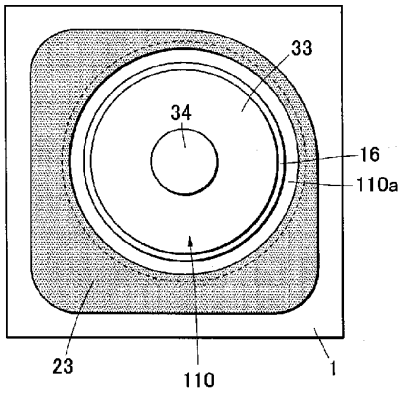
【図３】


16
10
10a
22
B'
32
22
B
31
10a
1

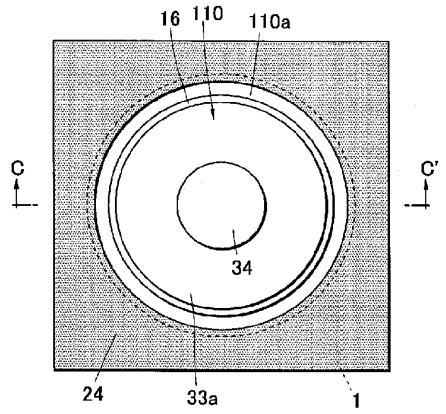
【図４】


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11
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1
31
10a
12a
22

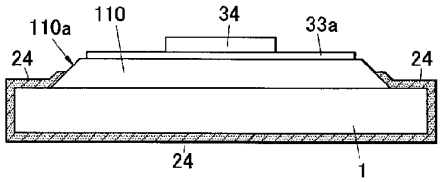
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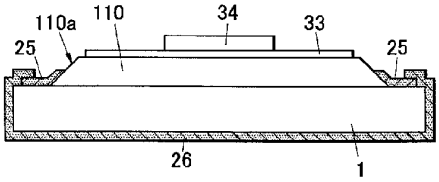
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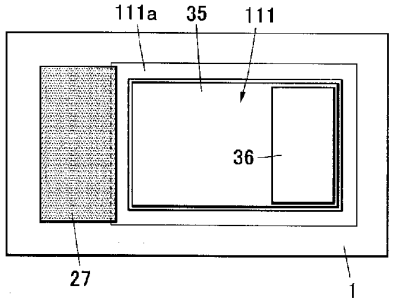
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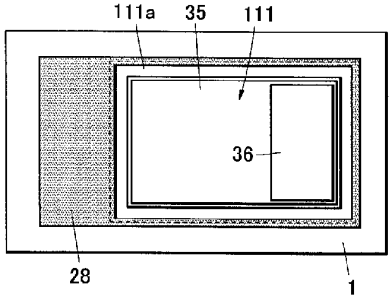
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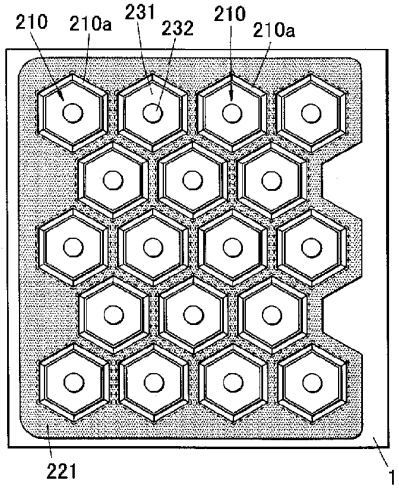
【図９】



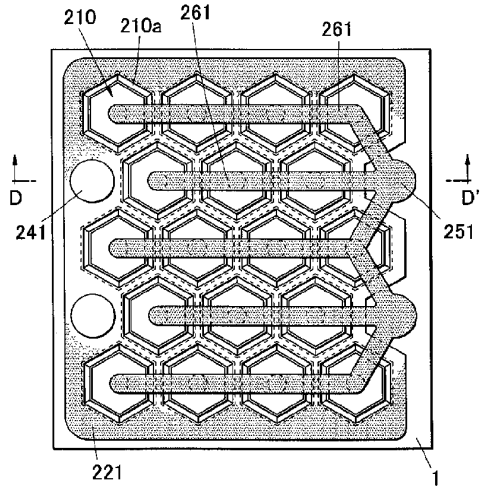
【図１０】



【図１１】

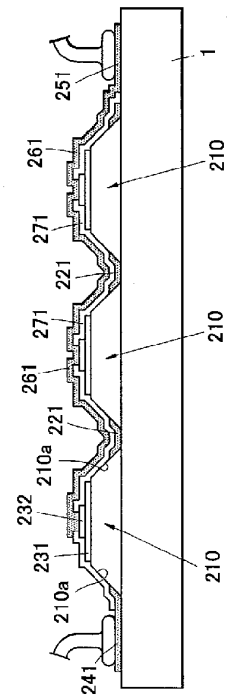


【図１２】

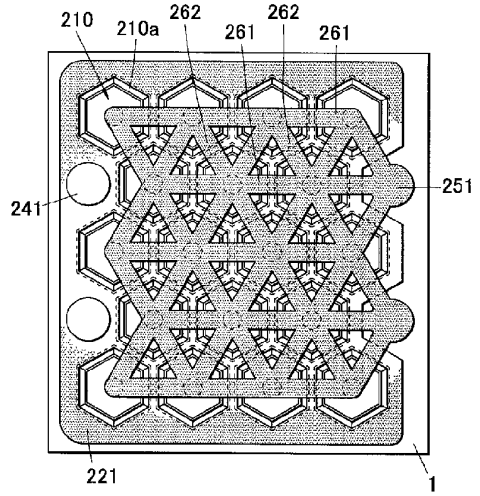


素子間接続Pパターン

【図１３】

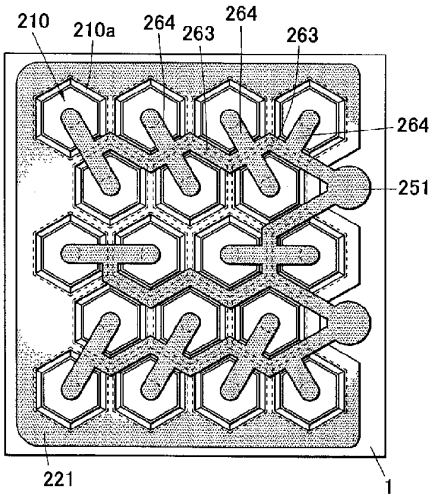


【図１４】



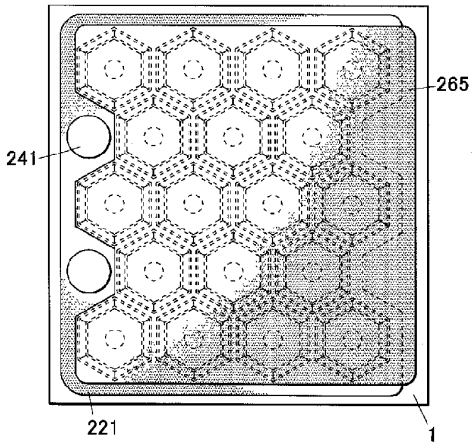
p配線例その２

【図１５】



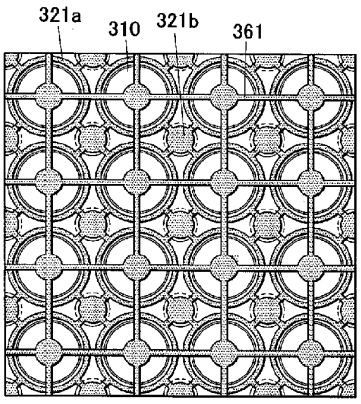
配線例4

【図１６】

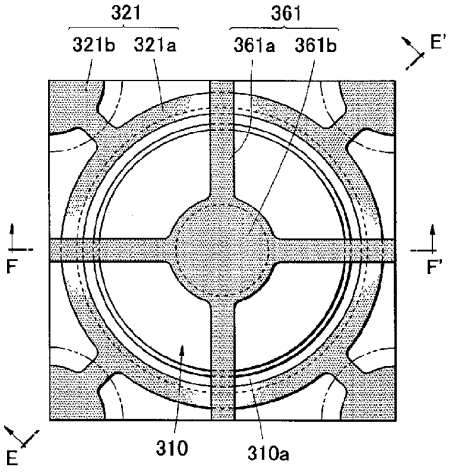


P配線例その3(FD対応型)

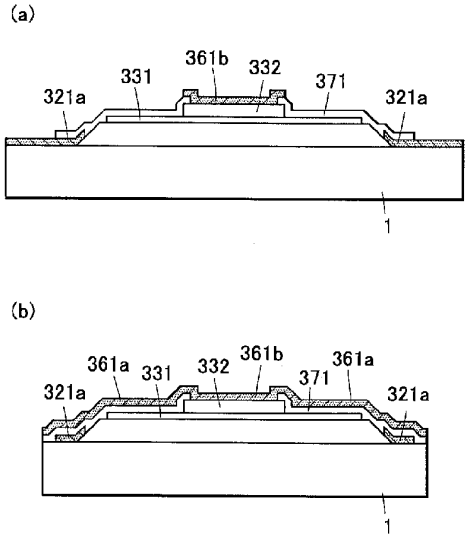
【図１７】



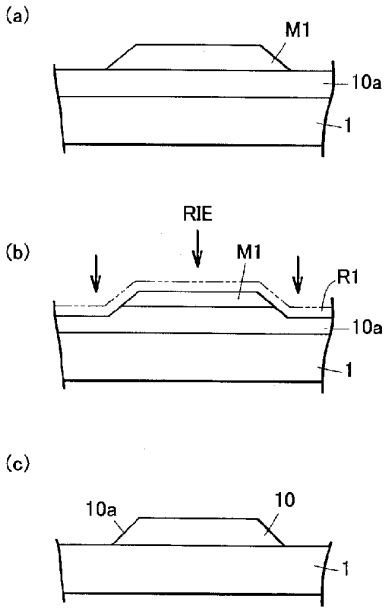
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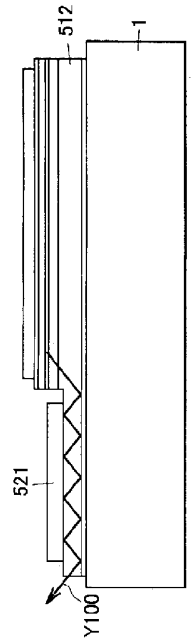
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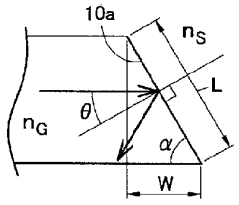
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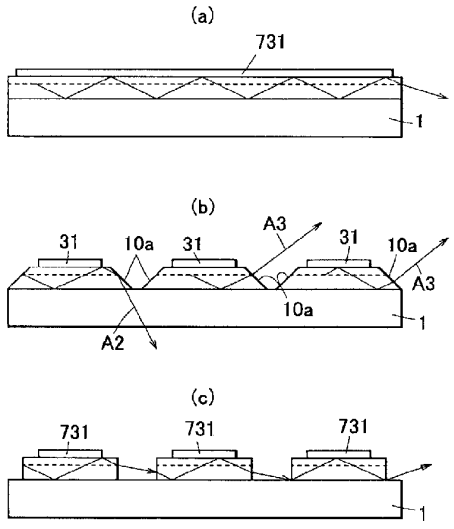
【図２１】



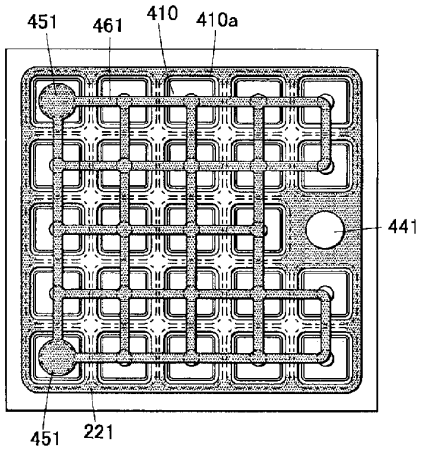
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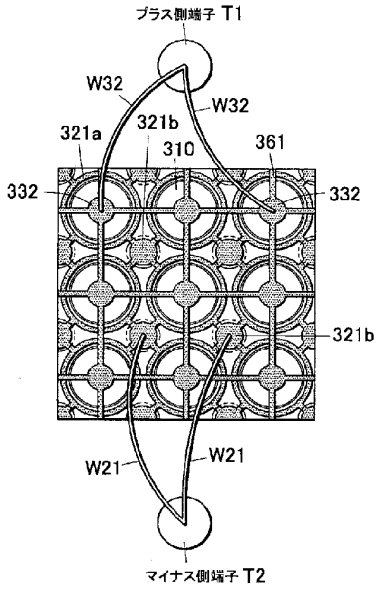
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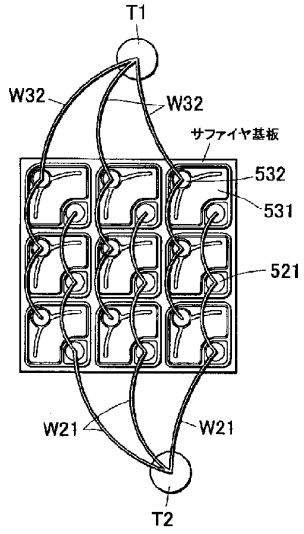
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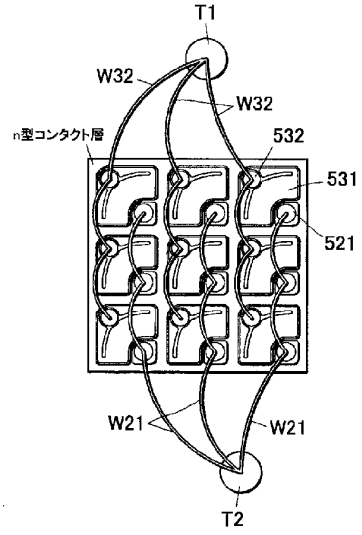
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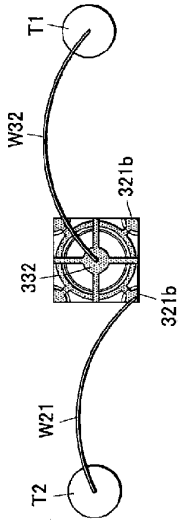
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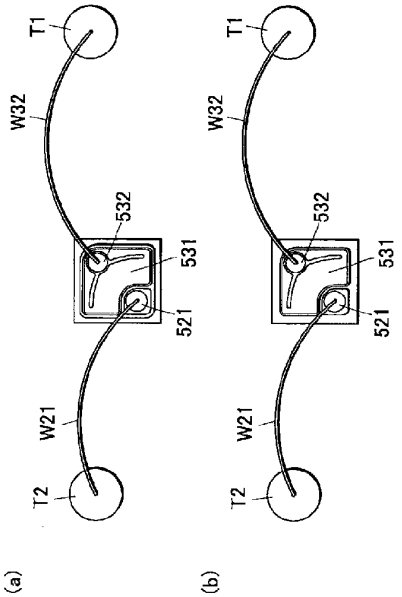
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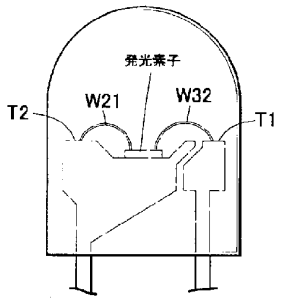
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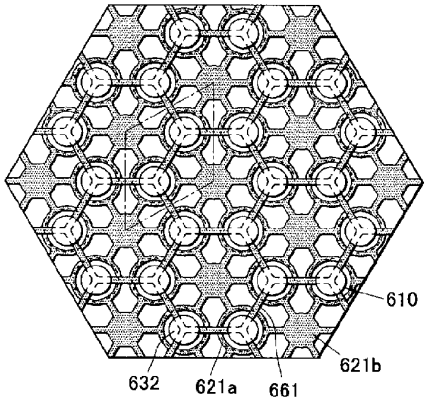
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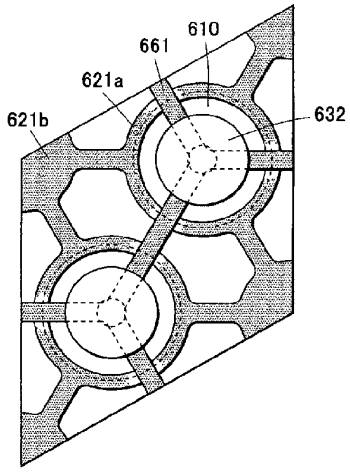
【図３０】



【図３１】



【図３２】



PATENT ABSTRACTS OF JAPAN

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(43)Date of publication of application : 30.09.2004

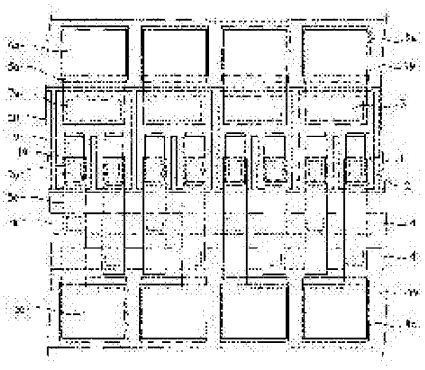
(51)Int.Cl. H01L 33/00

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(71)Applicant : HITACHI CABLE LTD
(72)Inventor : YUKIMOTO TOMIHISA
KUNITAKE EIICHI
SUGIYAMA SATOSHI
KOMORI YOSUKE
SUKEGAWA TOSHIMITSU

(54) LIGHT-EMITTING DIODE ARRAY

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a light emitting diode array capable of preventing the short-circuit of a wiring due to the residue of Au of working which is generated on the slanted surface of a level difference of mesa etching, and easy in the size control of a light emitting part while high in an yield and excellent in manufacturability.
SOLUTION: The light emitting diode array is provided with a conductive layer formed on a substrate, individually independent light emitting units formed on the conductive layer, first electrodes formed at least on one part of the upper surface of respective light emitting units and second electrodes formed on the conductive layer adjacent to the light emitting units. In such a light emitting diode array, the first electrodes are provided with a matrix common electrode for switching while the second electrodes are provided with a common electrode partitioned for every blocks. At least one of bonding pads extended from the first common electrode and the second common electrode is provided on a bonding unit formed on the conductive layer like an island, whereby respective bonding pads are formed independently.



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H01L 33/00	H01L 33/00	E	5F041

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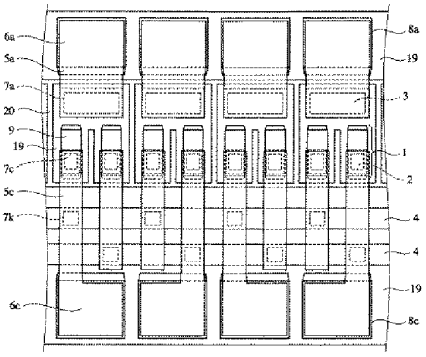
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(71)出願人　000005120
日立電線株式会社
東京都千代田区大手町一丁目６番１号
(74)代理人　100080012
弁理士　高石　橘馬
(72)発明者　行本　富久
東京都千代田区大手町一丁目６番１号　日立電線株式会社内
(72)発明者　国武　栄一
東京都千代田区大手町一丁目６番１号　日立電線株式会社内
(72)発明者　杉山　聡
東京都千代田区大手町一丁目６番１号　日立電線株式会社内

最終頁に続く

(54)【発明の名称】発光ダイオードアレイ

(57)【要約】
【課題】メサエッチング段差の斜面部分に発生するＡｕの加工残りによる配線短絡を防止するとともに発光部の寸法制御が容易で、高歩留、かつ量産性に優れた発光ダイオードアレイを提供する。
【解決手段】基板上に形成された導電層と、前記導電層上に形成された個々独立の発光部と、各発光部の上面の少なくとも一部に形成された第一の電極と、前記発光部に近接して前記導電層上に形成された第二の電極とを有する発光ダイオードアレイにおいて、前記第一の電極はスイッチ用のマトリクス共通電極を有し、前記第二の電極はブロック毎に分割された共通電極を有する発光ダイオードアレイであって、前記第一の共通電極及び前記第二の共通電極に延在するボンディングパッドの少なくとも一方は、前記導電層上に島状に形成されたボンディング部上に設けられており、もって前記ボンディングパッドは個々独立に形成されていることを特徴とする。
【選択図】　図１



【特許請求の範囲】
【請求項1】
基板上に形成された導電層と、前記導電層上に形成された個々独立の発光部と、各発光部の上面の少なくとも一部に形成された第一の電極と、前記発光部に近接して前記導電層上に形成された第二の電極とを有する発光ダイオードアレイにおいて、前記第一の電極はスイッチ用のマトリクス共通電極を有し、前記第二の電極はブロック毎に分割された共通電極を有する発光ダイオードアレイであって、前記第一の共通電極及び前記第二の共通電極に延在するボンディングパッドの少なくとも一方は、前記導電層上に島状に形成されたボンディング部上に設けられており、もって前記ボンディングパッドは個々独立に形成されていることを特徴とする発光ダイオードアレイ。
【請求項2】
請求項１に記載の発光ダイオードアレイにおいて、前記第一電極側及び前記第二電極側のボンディングパッドのどちらか一方は、メサエッチング溝部に設けられた絶縁膜上に形成されていることを特徴とする発光ダイオードアレイ。
【請求項3】
請求項１又は２に記載の発光ダイオードアレイにおいて、前記マトリクス共通電極はメサエッチング溝部に設けられた絶縁膜上に形成されていることを特徴とする発光ダイオードアレイ。

【発明の詳細な説明】
【０００１】
【発明の属する技術分野】
本発明は発光出力の大きい発光ダイオードアレイに関し、特に電子写真方式のプリンタ光源に好適な発光ダイオードアレイに関する。
【０００２】
【従来の技術】
電子写真方式のプリンタは、画像信号に応じた光により感光ドラム上に静電潜像を形成し、トナーを選択的に付着させて現像した後、紙に転写して画像を得る。潜像を形成するための光源としてはレーザ方式と発光ダイオードアレイ方式が広く用いられている。特に発光ダイオードアレイ方式の光源は、レーザ方式のように光路長を長くとる必要がないため、小型のプリンタや大サイズの印刷に適している。近年は印刷の高速・高画質化やプリンタの更なる小型化にともない、より高精細で高出力、かつ低コストの発光ダイオードアレイが求められている。
【０００３】
一般に、低コストを実現するためには、個々独立に発光ダイオードを駆動させるＩＣを備える方法（スタティック駆動方式）ではなく、２のｎ乗個の発光ダイオードを１つのブロックとし、スイッチ用のマトリクス配線を用いて時間分割駆動させ、駆動ＩＣやボンディング本数を削減する方法（ダイナミック駆動方式）が用いられている。このような発光ダイオードアレイを製造するプロセスにおいて、配線材料としてはＴｉ／ＡｕやＭｏ／Ａｕが広く用いられている。この配線を形成する方法としては、リフトオフ法（フォトレジストでパターンニング後、電子線蒸着し、不要部分をレジストと共に除去する方法）と、スパッタ～イオンミリング加工法（スパッタでウェーハ全体にＴｉ／ＡｕやＭｏ／Ａｕを沈着させた後、パターンニングされたフォトレジストやSiO_2等の絶縁膜からなるマスク材を物理的に削る方法）が用いられる。リフトオフ法ではステップカバレジが悪いのでメサエッチング段差が大きいＬＥＤでは配線層が段切れし易い。また、スパッタ～イオンミリング加工法の場合、ステップカバレジが良好で段切れが起き難い反面、メサエッチング段差部にＡｕ加工残りが発生し易いという欠点がある。特に共通電極を有するダイナミック駆動式のＬＥＤでは、このＡｕの加工残りによって、配線が短絡し、所望しないＬＥＤが発光してしまうという問題があった。
【０００４】
図４は、従来の２分割ダイナミック駆動方式の発光ダイオードアレイを示す上面図であり

、図５（ａ）は図４のうちのひとつのブロックを示す上面図である。図５（ｂ）は図５（ａ）のＡ－Ａ断面図であり、図５（ｃ）は図５（ａ）のＢ－Ｂ断面図である。ｎ型ＧａＡｓ基板１０上に形成されたｐ型ＧａＡｓ導電層１１の上に所定間隔で複数の発光部１が配置されている。各発光部１は、ｐ型ＧａＡｓ導電層１１の上に順次積層されたｐ型ＡｌＧａＡｓエッチングストッパ層１２、ｐ型ＡｌＧａＡｓクラッド層１３、ｐ型ＡｌＧａＡｓ活性層１４、ｎ型ＡｌＧａＡｓクラッド層１５及びｎ型ＧａＡｓキャップ層１６からなる。発光部１の発光領域は、ｐ型ＡｌＧａＡｓクラッド層１３、ｐ型ＡｌＧａＡｓ活性層１４及びｎ型ＡｌＧａＡｓクラッド層１５からなるダブルヘテロ構造を有する。

【０００５】

各発光部１はエピタキシャル層をメサエッチングにより除去することにより形成されている。メサエッチング溝は、発光部１とボンディング部８とを分離する第一のメサエッチング溝部１９と各ブロックを分割する役割を有する第二のメサエッチング溝部２０とからなる。

【０００６】

各発光部１の上面の一部にカソード電極２が形成されている。発光部１に近接してｐ型ＧａＡｓ導電層１１上に各ブロック毎に設けられているアノード電極３はｐ型ＧａＡｓ導電層１１の上にそれぞれ金属を蒸着・合金化することにより形成される。カソード電極２及びアノード電極３の各々のコンタクト孔７ｃ、７ａを除いて、発光部１及び露出した導電層１１の表面はＰＳＧ（リンガラス）等からなる第一絶縁膜１７により覆われている。共通電極４はカソード側のボンディング部（メサ頂面）８ｃを覆う第一絶縁膜１７上に設けられ、更に第二絶縁膜を被覆した後、この第二絶縁膜により覆われていないカソード電極２に一端部が接続するようにＡｕ配線層５ｃが形成されており、Ａｕ配線層５ｃはボンディング部８ｃの表面まで延在して共通電極４の所望部分と接続し、その他端部にはボンディングパッド６ｃが形成されている。一方、アノード電極３に一端部が接続するようにＡｕ配線層５ａが形成されており、Ａｕ配線層５ａはボンディング部（メサ頂面）８ａの表面まで延在し、Ａｕ配線層５ａの他端部にはボンディングパッド６ａが形成されている。

【０００７】

このような構造の発光ダイオードアレイは、Ａｕ配線層５を形成する方法にスパッタ～イオンミリング法を用いたとき、第一のメサエッチング溝の斜面２１にはイオンミリングによるＡｕ残りが発生し易く、Ａｕ配線の短絡を防止するうえで満足できるものではない（例えば、特許文献１参照。）。この問題は、発光部１を除く全てを第一メサエッチング溝として除去し、メサエッチング溝部の底面に配線層、共通電極及びボンディングパッドを形成すれば解決できるが、その場合には異なる問題が発生する。すなわち、発光部１を残して全てをエッチングすると、エッチング面積の大きい部分と各発光部間のエッチング面積の小さい部分の差が広がる。エッチングプロセスにおいてエッチング速度には面積依存性があるため（ローディング効果）、性能に影響する発光部の寸法制御が極めて困難になる。

【０００８】

特許文献２には半導体基板の一部に凹部を設け、この凹部内に共通電極を形成した発光ダイオードアレイが開示されている。しかしながら、この方式では共通電極部分のみが凹部内に形成されているため、メサエッチング溝の斜面に発生したＡｕ残りにより短絡が発生しやすい。

【０００９】

【特許文献１】

特開２０００－３２３７５０号公報

【特許文献２】

特開平１０－１５７１９３号公報

【００１０】

【発明が解決しようとする課題】

従って本発明の目的は、メサエッチング段差の斜面部分に発生するＡｕの加工残りによる

配線短絡を防止するとともに発光部の寸法制御が容易で、高歩留、かつ量産性に優れた発光ダイオードアレイ及びその製造プロセスを提供することである。

【００１１】

【課題を解決するための手段】

上記目的に鑑み鋭意研究の結果、本発明者らは、ボンディングパッドをメサエッチング溝によって独立したボンディング部（メサ頂面）上に形成することにより、Ａｕの加工残りによる配線短絡を防止できることを発見し、本発明に想到した。

【００１２】

すなわち、本発明の発光ダイオードアレイは、基板上に形成された導電層と、前記導電層上に形成された個々独立の発光部と、各発光部の上面の少なくとも一部に形成された第一の電極と、前記発光部に近接して前記導電層上に形成された第二の電極とを有し、前記第一の電極はスイッチ用のマトリクス共通電極を有し、前記第二の電極はブロック毎に分割された共通電極を有する発光ダイオードアレイであって、前記第一の共通電極及び前記第二の共通電極に延在するボンディングパッドの少なくとも一方は、前記導電層上に島状に形成されたボンディング部上に設けられており、もって前記ボンディングパッドは個々独立に形成されていることを特徴とする。

【００１３】

前記第一電極側及び前記第二電極側のボンディングパッドのどちらか一方は、メサエッチング溝部に設けられた絶縁膜上に形成されていてもよい。また、前記マトリクス共通電極はメサエッチング溝部に設けられた絶縁膜上に形成されているのが好ましい。

【００１４】

本発明の発光ダイオードアレイにおいて、発光部及びボンディング部は導電層上に形成されたエピタキシャル層をメサエッチング溝により個々独立・分割してなるのが好ましい。好ましい実施例による発光ダイオードアレイでは、ボンディングパッドは個々独立のボンディング部上に形成されているために、メサエッチング溝の斜面にＡｕ配線を残してもボンディングパッド間で短絡することがない。また、ボンディング部は第一のメサエッチング溝により残されたエピタキシャル層上に形成されているので、エッチング面積を増大させることがない。これによりローディング効果を避けることができ、同じく第一のメサエッチング溝により残されたエピタキシャル層である発光部の寸法制御が容易となる

【００１５】

【発明の実施の形態】

［１］　発光ダイオードアレイの構造

図１及び図２に示すように、本発明の発光ダイオードアレイは、基板１０、基板１０上に形成された複数の発光部１、各発光部１の上面に部分的に形成された第一の電極２、及び発光部１に近接する位置で導電層１１上に形成された第二の電極３を有する。図示の実施例では、各発光部１は基板１０上に均一に形成されたエピタキシャル層にメサエッチング溝部１９、２０を設け、個々独立のエピタキシャル層部としたものである。

【００１６】

（１）　基板

基板１０は、発光ダイオード用に使用し得るものであれば特に限定されず、発光部と電気的に絶縁できる構造であればよい。ｎ型基板でもｐ型基板でも用いることができ、半絶縁性ＧａＡｓ基板等の半絶縁性基板または絶縁性基板を用いてもよい。基板１０と導電層１１との間にアンドープＧａＡｓ層等の高抵抗層を設けて絶縁することもでき、また導電層１１に対して逆の極性を有する半導体層を設けて絶縁することもできる。

【００１７】

（２）　発光部

基板１０の導電層１１上に積層する化合物半導体の種類や結晶層の厚さは、所望の発光波長及び発光出力により適宜選択する。化合物半導体としては、例えばＡｌＧａＡｓ、ＡｌＧａＩｎＰ等を用いることができる。発光部１は第一導電型のクラッド層、活性層及び第二導電型のクラッド層からなるダブルヘテロ構造を有するのが好ましく、導電層上に形成

したエピタキシャル層を第一のメサエッチング溝により分割してなるのが好ましい。さらに、第二のメサエッチング溝２０は各ブロック間を分離するために導電層１１を分断している。

【００１８】

図示の実施例では、発光ダイオードアレイの発光部１は、ｎ型ＧａＡｓ基板１０の上にｐ型ＧａＡｓ導電層１１を介して順次形成されたｐ型ＡｌＧａＡｓエッチングストッパ層１２、ｐ型ＡｌＧａＡｓクラッド層１３、ｐ型ＡｌＧａＡｓ活性層１４、ｎ型ＡｌＧａＡｓクラッド層１５及びｎ型ＧａＡｓキャップ層１６からなる。ｎ型ＧａＡｓキャップ層１６は、光取り出し部９の領域ではエッチングにより除去されている。Ａｕ配線層５との短絡防止のため、第一及び第二絶縁膜１７、１８がカソード電極２を除いて発光部２の表面全体を覆っている。

【００１９】

上記発光部１のうち発光に直接関与する領域は、発光波長に対応するエネルギーバンドギャップを有するｐ型ＡｌＧａＡｓ活性層１４を、それよりもエネルギーバンドギャップの大きいｐ型ＡｌＧａＡｓクラッド層１３（第一導電型のクラッド層）及びｎ型ＡｌＧａＡｓクラッド層１５（第二導電型のクラッド層）で挟んだ、いわゆるダブルヘテロ構造を有する。

【００２０】

（３）　電極及び配線層

第一及び第二電極の一方がカソード電極で、他方がアノード電極であればよく、例えば第一の電極はカソード電極でもアノード電極でもよい。各電極はボンディング特性、下層とのオーミック接続特性が要求される。例えばアノード電極にＡｕＺｎ／Ｎｉ／Ａｕの積層電極を使用し、カソード電極にＡｕＧｅ／Ｎｉ／Ａｕ等の積層電極を使用する。

【００２１】

共通電極及びＡｕ配線層はボンディング特性、上層・下層との密着性が良好であることが要求されるため複数の金属層で構成されるのが好ましい。最上層及び最下層にはボンディング特性及び絶縁膜の接着性が良いＴｉ，Ｍｏ等の金属層を有するのが好ましい。例えば、共通電極としてＴｉ／Ａｕ／Ｔｉ、Ｍｏ／Ａｕ／Ｍｏ、ＴｉＷ／Ａｕ／ＴｉＷ等の積層電極を使用することができる。

【００２２】

各電極の金属層は抵抗加熱蒸着法、電子線加熱蒸着法、スパッタ法等で形成することができ、酸化物層は各種公知の成膜方法で形成することができる。カソード及びアノード金属層には、オーミック性を付与するため熱処理（合金化）をさらに施すのが好ましい。

【００２３】

図１及び図２に示す実施例では、各発光部１のメサ頂面にカソード電極２が形成されており、各発光部１側面及びカソード電極２周辺部は第一絶縁膜１７で覆われている。各発光部１上のカソード電極２は、コンタクト孔７によりＡｕ配線層５ｃを経由して２本の共通電極４のうち何れか一本と接続しており、個々独立したボンディング部８ｃ上にボンディングパッド６ｃを形成している。一方、各発光部１に近接する位置にアノード電極３がｐ型ＧａＡｓ導電層１１上に形成され、オーム接触している。アノード電極３は、Ａｕ配線層５ａを経由して、ボンディング部８ａのメサ頂面のボンディングパッド６ａに接続している。

【００２４】

（４）　メサエッチング溝

個々独立の発光部１及びボンディング部８を形成するため第一のメサエッチング溝部１９は、発光部１とボンディング部８とを電気的に分離するため導電層１１又はエッチングストッパ層１２まで達する第一のメサエッチング溝部１９と、発光部１の各ブロックを分断する目的で導電層１１を除去する第二のメサエッチング溝部２０とからなる。本発光ダイオードアレイの特徴的な要素である第一のメサエッチング溝部１９は発光部１を形成するほかに、個々独立のボンディング部８を形成している。

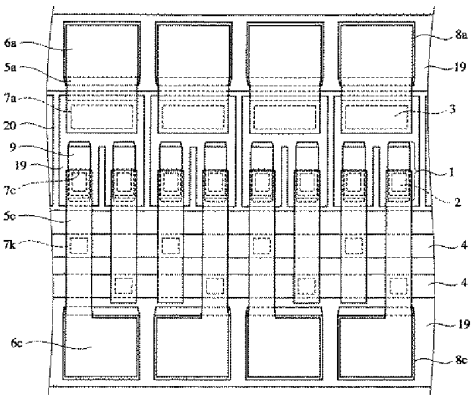
【００２５】
［２］　発光ダイオードアレイの製造方法
本発明の発光ダイオードアレイは、第一のメサエッチング溝部１９により個々独立のボンディング部８を形成する以外、従来と同じ方法により製造することができる。好ましい製造例としては、まず有機金属気相成長法（ＭＯＶＰＥ法）によりｎ型ＧａＡｓ基板１０の上面に、ｐ型ＧａＡｓ導電層１１（キャリア濃度：４×１０^{19}ｃｍ$^{-3}$、厚さ：１μｍ）、ｐ型ＡｌＧａＡｓエッチングストッパ層１２（キャリア濃度：３×１０^{19}ｃｍ$^{-3}$、厚さ：０．１μｍ）、ｐ型ＡｌＧａＡｓクラッド層１３（キャリア濃度：１×１０^{18}ｃｍ$^{-3}$、厚さ：１μｍ）、ｐ型ＡｌＧａＡｓ活性層１４（キャリア濃度：１×１０^{18}ｃｍ$^{-3}$、厚さ：１μｍ）、ｎ型ＡｌＧａＡｓクラッド層１５（キャリア濃度：２×１０^{18}ｃｍ$^{-3}$、厚さ：３μｍ）、及びｎ型ＧａＡｓキャップ層１６（キャリア濃度：１×１０^{18}ｃｍ$^{-3}$、厚さ：０．５μｍ）を順次成長させる。
【００２６】
形成した結晶層にウェットエッチングを選択的に施す。まずカソード電極２と接触する部分を残して発光部１のｎ型ＧａＡｓキャップ層１６を除去する。次に、ｐ型ＡｌＧａＡｓエッチングストッパ層１２が露出する深さにメサエッチング溝１９を設けて、ｐ型ＧａＡｓ導電層１１上のエピタキシャル層を複数の発光部１に分割するとともに、発光部１と個々独立したボンディング部８とを形成する。このとき、ローディング効果を回避できるのであれば、図３に示すようにどちらか一方のボンディング部は除去してしまっても良い。さらに第二のメサエッチング溝部２０によりｐ型ＧａＡｓ導電層１１を除去し、発光部１の各ブロックを電気的に分離する。このときのｎ型ＧａＡｓ基板１０も僅かにエッチングされるように第二のメサエッチング溝部２０の深さを設定すれば、エッチング誤差があっても導電層１１が残留することはない。
【００２７】
次いで、カソード電極２（ＡｕＧｅ／Ｎｉ／Ａｕ）及びアノード電極３（ＡｕＺｎ／Ｎｉ／Ａｕ）をそれぞれ蒸着～リフトオフ法により形成する。次に発光ダイオードアレイの上面全体を覆うように化学気相成長法（ＣＶＤ法）により第一絶縁膜１７を成長させた後、共通電極４（Ｔｉ／Ａｕ／Ｔｉ）を蒸着～リフトオフ法で形成する。さらにＣＶＤ法により第二絶縁膜１８を成長させた後、カソード電極２、アノード電極３と２本の共通電極のうち所望の一方にコンタクト孔をエッチングにより設け、Ｔｉ／Ａｕをスパッタ～イオンミリングにより、各々のボンディング部８まで延在するＡｕ配線層５を形成する。
【００２８】
ここでは共通電極を２本とした２×２構造の例を述べたが、４つの発光部を１ブロックとして４本の共通電極を持つ４×４構造でも、８×８、１６×１６…の構造でも同様である。
【００２９】
【発明の効果】
以上詳述したように、本発明の発光ダイオードアレイではボンディング部がメサエッチング溝により個々独立に形成されるので、メサエッチング溝の斜面にＡｕ配線層が残っても、或いは意図的にメサエッチング斜面をＡｕ配線層で被覆するような設計にしても配線が短絡することがなく、かつ発光部の寸法制御が容易で、高歩留の量産プロセスを提供することができる。
【図面の簡単な説明】
【図１】本発明の一実施例による発光ダイオードアレイを示す上面図である。
【図２】図１の発光ダイオードアレイを構成する単一セルを示し、（ａ）は上面図であり、（ｂ）は（ａ）のＡ－Ａ断面図であり、（ｃ）は（ａ）のＢ－Ｂ断面図である。
【図３】本発明の別の実施例による発光ダイオードアレイを構成する単一セルを示し、（ａ）は上面図であり、（ｂ）は（ａ）のＡ－Ａ断面図である。
【図４】従来の発光ダイオードアレイを示す上面図である。
【図５】図４の発光ダイオードアレイを構成する単一セルを示し、（ａ）は上面図であり

、（ｂ）は（ａ）のＡ－Ａ断面図であり、（ｃ）は（ａ）のＢ－Ｂ断面図である。

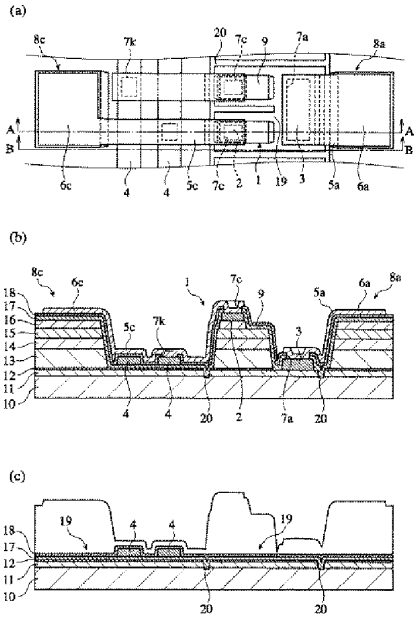
【符号の説明】

１・・・発光部
２・・・カソード電極
３・・・アノード電極
４・・・共通電極
５・・・Ａｕ配線層
５ａ・・・アノード側
５ｃ・・・カソード側
６・・・ボンディングパッド
６ａ・・・アノード側
６ｃ・・・カソード側
７・・・コンタクト孔
７ａ・・・アノード側
７ｃ・・・カソード側
７ｋ・・・共通電極上コンタクト孔
８・・・ボンディング部
８ａ・・・アノード側
８ｃ・・・カソード側
９・・・光取り出し部
１０・・・（ｎ型ＧａＡｓ）基板
１１・・・（ｐ型ＧａＡｓ）導電層
１２・・・ｐ型ＡｌＧａＡｓエッチングストッパ層
１３・・・ｐ型ＡｌＧａＡｓクラッド層
１４・・・ｐ型ＡｌＧａＡｓ活性層
１５・・・ｎ型ＡｌＧａＡｓクラッド層
１６・・・ｎ型ＧａＡｓキャップ層
１７・・・第一絶縁膜
１８・・・第二絶縁膜
１９・・・第一のメサエッチング溝部
２０・・・第二のメサエッチング溝部
２１・・・第一のメサエッチング溝の斜面

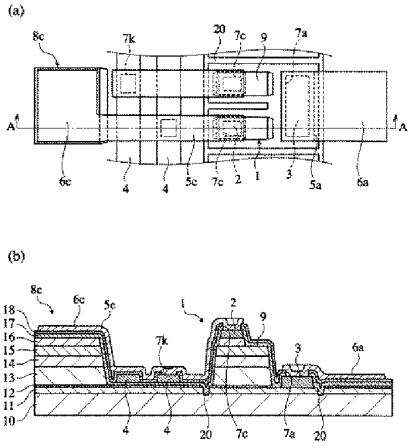
【図1】


6a
5a
7a
20
9
19
7c
5c
7k
6c
8a
19
3
1
2
4
4
19
8c

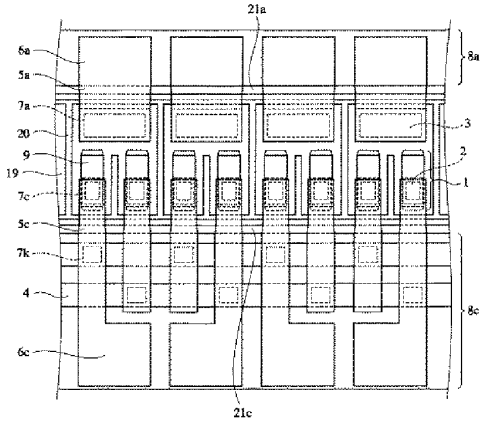
【図2】


(a)
8c
7k
20
7c
9
7a
8a
A
B
6c
4
4
5c
7c
2
1
19
3
5a
6a
(b)
8c
6c
1
7c
9
5a
6a
8a
18
17
16
15
14
13
12
11
10
5c
7k
3
4
4
20
2
7a
20
(c)
19
4
4
19
18
17
12
11
10
20
20

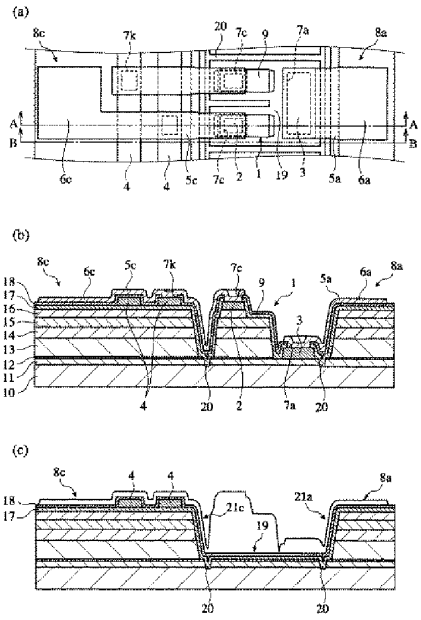
【図3】


(a)
8c
7k
20
7c
9
7a
A
A
6c
4
4
5c
7c
2
1
3
5a
6a
(b)
8c
6c
5c
1
2
9
18
17
16
15
14
13
12
11
10
7k
3
6a
4
4
20
7c
7a
20

【図4】


21a
6a
5a
7a
20
9
19
7c
5c
7k
4
6c
21c
8a
3
2
1
8c

【図5】


(a)
8c
7k
20
7c
9
7a
8a
A
B
6c
4
4
5c
7c
2
1
19
3
5a
6a
(b)
8c
6c
5c
7k
7c
9
1
5a
6a
8a
18
17
16
15
14
13
12
11
10
4
20
2
7a
20
(c)
8c
4
4
8a
18
17
21c
19
21a
20
20

(72)発明者　小森　洋介
東京都千代田区大手町一丁目６番１号　日立電線株式会社内
(72)発明者　助川　俊光
東京都千代田区大手町一丁目６番１号　日立電線株式会社内

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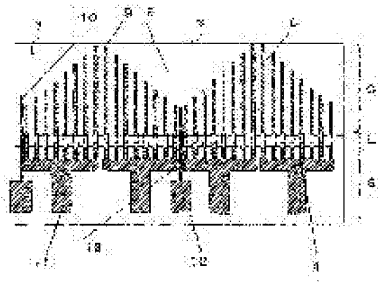
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B41J 2/455

(21)Application number : 2003-369965
(22)Date of filing : 30.10.2003

(71)Applicant : KYOCERA CORP
(72)Inventor : KITADA KATSUNOBU

(54) LIGHT EMITTING DIODE ARRAY DEVICE AND LIGHT EMITTING DIODE PRINTER USING IT

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a light emitting diode array device that can reduce the variation of the resistances of electrodes and is improved in the connection reliability of common electrodes, and to provide an LED printer.
SOLUTION: In the light emitting diode array device, a plurality of light emitting diodes 10 are arranged on a high resistance substrate 1. The device is composed of individual electrodes 4 which are commonly connected to light emitting diodes in the same group composed of N pieces of light emitting diodes, and common electrodes 50 which are connected to prescribed light emitting diodes of different groups. Of M groups of light emitting elements, the light emitting diodes 10 of the m-th group are successively connected to N pieces of common electrodes 50 from the first common electrode 5a nearest to a light emitting diode array to the first common electrode 5h farthest from the array. The light emitting diodes 10 of a group adjoining the m-th group are successively connected to the N pieces of common electrodes 50 from the first common electrode 5h farthest from the light emitting diode array to the first common electrode 5a nearest to the array.



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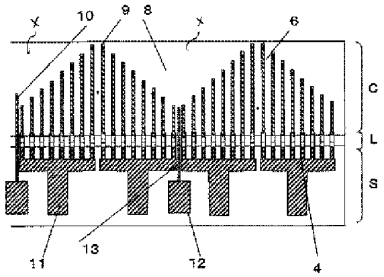
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(71)出願人　000006633
京セラ株式会社
京都府京都市伏見区竹田鳥羽殿町６番地
(72)発明者　北田　勝信
滋賀県八日市市蛇溝町長谷野１１６６番地の６　京セラ株式会社滋賀八日市工場内

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(54)【発明の名称】発光ダイオードアレイ装置及びそれを用いた発光ダイオードプリンタ

(57)【要約】
【課題】　電極抵抗のバラツキを小さくするとともに、共通電極の高い接続信頼性の発光ダイオードアレイ装置及びＬＥＤプリンタを提供することにある。
【解決手段】
本発明は、高抵抗基板１上に発光ダイオード１０を複数個配列するとともに、Ｎ個の発光ダイオードを発光素子群として、同一の発光素子群内の発光ダイオードに共通に接続する個別電極４と、異なる群に属する所定の発光ダイオードに接続する共通電極５０とからなる発光ダイオードアレイ装置である。そして、M群の発光素子群のうち、m番目の発光素子群の各発光ダイオード１０は、Ｎ個の共通電極のうち発光ダイオードアレイに最も近い側の第１の共通電極５ａから遠い側の第１の共通電極５ｈに順次に接続し、m番目の発光素子群に隣接する発光素子群の各発光ダイオード１０は、Ｎ個の共通電極のうち発光ダイオードアレイに最も遠い側の第１の共通電極５ｈから近い側の第１の共通電極５ａに順次接続する。
【選択図】図３



【特許請求の範囲】
【請求項1】
高抵抗基板上に複数の一導電型半導体層と逆導電型半導体層を設け、且つ該一導電型半導体層に共通電極を、逆導電型半導体層に個別電極を接続した発光ダイオードを複数個配列するとともに、前記複数の配列された発光ダイオードのうち、Ｎ個の発光ダイオードを発光素子群として、Ｍ群から構成される発光ダイオードアレイと、同一の発光素子群内の発光ダイオードの逆導電型半導体層に共通に接続する個別電極と、異なる群に属する所定の発光ダイオードの一導電型半導体層に接続する共通電極とからなる発光ダイオードアレイ装置において、
　共通電極は、発光ダイオードの配列方向に概略平行に延びるＮ個の第１の共通電極と、いずれか１つの第１の共通電極と同一の発光素子群のいずれか１つの発光ダイオードとを接続する第２の共通電極とから構成されるとともに
　Ｍ群の発光素子群のうち、ｍ番目の発光素子群の各発光ダイオードは、Ｎ個の共通電極のうち発光ダイオードアレイに最も近い側の第１の共通電極から遠い側の第１の共通電極に順次に第２の共通電極を介して接続するとともに、
　前記ｍ番目の発光素子群に隣接する発光素子群の各発光ダイオードは、Ｎ個の共通電極のうち発光ダイオードアレイに最も遠い側の第１の共通電極から近い側の第１の共通電極に順次に第２の共通電極を介して接続されていることを特徴とする発光ダイオードアレイ装置。
【請求項2】
前記第１の共通電極上には、第１の共通電極と第２の共通電極とを接続するコンタクトホールが形成された絶縁膜によって被覆され、且つ該絶縁基板上に第１の共通電極から共通電極側接続パッドとを接続する引出し配線が形成されているとともに、該引出し配線と第１の共通電極配線は、記前記隣接しあう発光素子群から延びる第２の共通電極の境界部分の絶縁膜に形成した第２のコンタクトホールを介して接続されていることを特徴とする請求項１記載の発光ダイオードアレイ装置。
【請求項3】
前記請求項１乃至２に記載された発光ダイオードアレイ装置と、該発光ダイオードアレイ装置の駆動を制御する駆動回路と、ページプリンタ用感光ドラムとを少なくとも有し、前記駆動回路によって発光動作する発光ダイオードアレイ装置の光を、前記ページプリンタ用感光ドラムの露光用光源に用いて、該ドラム表面に画像を形成する発光ダイオードプリンタ。

【発明の詳細な説明】
【技術分野】
【0001】
　本発明は、本発明は発光ダイオードアレイ装置、及びページプリンタ用感光ドラムの露光用光源などに用いられる発光ダイオードプリンタ（以下、単に、ＬＥＤプリンタという）に関するものである。
【背景技術】
【0002】
　通常、発光ダイオードアレイ装置の発光ダイオードの構造として、高抵抗基板の内部に一導電型半導体層、逆導電型導体層を形成すべく、ドープ材料を拡散処理して形成する構造（例えば特開平１１－４０８４２号）と、高抵抗基板上に、一導電型半導体層、逆導電型導体層をそれぞれ成膜して形成する構造（メサ型）が知られている。
【0003】
　例えば、このメサ型構造の発光ダイオードアレイ装置に関して、特開２００１－３２００８８号（特許文献１）が提案されている。その構造を図１１～図１３に示す。
【0004】
　図１１は、発光ダイオードの部分断面図、図１２は高抵抗基板上での電極配線の状況、特に下部側の電極配線の状況を示す概略平面図であり、図１３は電極配線の状況、特に上

部側の電極配線の状況を示す概略平面図である。

【0005】

図１１において、１２１は高抵抗基板であり、例えば半導体基板である。１２２は一導電型半導体層、１２３は逆導電型半導体層、１２４は個別電極、１２５は共通電極である。

【0006】

例えば、一導電型半導体層１２２は、バッファ層１２２ａ、オーミックコンタクト層１２２ｂ、電子注入層１２２ｃで構成される。また、逆導電型半導体層１２３は、発光層１２３ａ、クラッド層１２３ｂおよびオーミックコンタクト層１２３ｃで構成される。

【0007】

高抵抗基板１２１上に、一導電型半導体層１２２と逆導電型半導体層１２３とから成る発光ダイオードを設けるに当たり、一導電型半導体層１２２よりも逆導電型半導体層１２３を小面積と成すとともに、この一導電型半導体層１２２の露出部（オーミックコンタクト層１２２ｂ）に共通電極１２５が接続されている。また、逆導電型半導体層２３のオーミックコンタクト層１２３ｃに個別電極124が接続されている。なお、符号126は、窒化シリコン膜、ポリイミドなどから成る絶縁膜である。

【0008】

また、図１２に示すように発光ダイオードは、その配列方向にそって複数配列形成、平面視上、複数の発光ダイオードがアレイ状に配置されている。図では説明を簡略化のため、左端の３２の発光ダイオード素子が配列されている状態を例示している。そして、各発光ダイオードの駆動にあたっては、1つの発光素子群の構成する素子数Nを例えば８として取り扱っている。すなわち、図１２では、左側から１番目から８番目の発光ダイオード素子を群１に、９番目から１６番目の発光ダイオード素子を群２、・・・・とし、全体として群１～群M（図では、M=４までの一部を図示している）を有して構成される。

【0009】

また、各発光ダイオードの一導電型半導体層１２２には、共通電極１２５が接続されている。この共通電極125は、高抵抗基板１２１上に形成した絶縁膜１２６上に形成され逆導電型半導体層１２３には、個別電極１２４が接続されている。この個別電極１２４は、高抵抗基板１２１上においては、共通電極１２５と同様に絶縁膜１２６を介して形成されている。

【0010】

この共通電極１２５は、図１２に示すように、絶縁膜１２６上に概略コ字状形状の下地側に位置する第１の共通電極１２５ａ、１２５ｂ、１２５ｃ、１２５d、１２５ｅ、１２５ｆ、１２５ｇ、１２５hと、図１３に示すように、第１の共通電極１２５ａ、１２５ｂ、１２５ｃ、１２５d、１２５ｅ、１２５ｆ、１２５ｇ、１２５ｈを被覆された第２の絶縁膜１２７上にアレイ状の配列方向と平行に断続的に形成された上側の第２の共通電極１２８ａ、１２８ｂ、１２８ｃ、１２８ｄ、１２８ｅ、１２８ｆ、１２８ｇ、１２８ｈとで構成されている。

【0011】

ここで、共通電極１２５のうち、コ字状の下地側の第１の共通電極は、隣接する１２つの群の所定発光素子どうしを接続するように形成されている。たとえば、この第１の共通電極１２５ａ、１２５ｂ、１２５ｃ、１２５ｄ、１２５ｅ、１２５ｆ、１２５ｇ、１２５ｈどうしが交差していように配慮されており、最外周に位置する電極１２５ａは、群１（群３）の第１の番目の発光ダイオードと群２（群４）の第８番目の発光ダイオードとを接続するように概略コ字状に形成され、外周より２番目に位置する電極１２５ｂは、群１（群３）の第２の番目の発光ダイオードと群２（群４）の第７番目の発光ダイオードとを接続するように概略コ字状に形成され、外周より３番目に位置する電極１２５ｃは、群１（群３）の第３の番目の発光ダイオードと群２（群４）の第６番目の発光ダイオードとを接続するように概略コ字状に形成され、外周より４番目に位置する電極１２５ｄは、群１（群３）の第４の番目の発光ダイオードと群２（群４）の第５番目の発光ダイオードとを接

続するように概略コ字状に形成され、外周より５番目に位置する電極１２５ｅは、群１（群３）の第５の番目の発光ダイオードと群２（群４）の第４番目の発光ダイオードとを接続するように概略コ字状に形成され、
外周より６番目に位置する電極１２５ｆは、群１（群３）の第６の番目の発光ダイオードと群２（群４）の第３番目の発光ダイオードとを接続するように概略コ字状に形成され、
外周より７番目に位置する電極１２５ｇは、群１（群３）の第７の番目の発光ダイオードと群２（群４）の第１２番目の発光ダイオードとを接続するように概略コ字状に形成され、
最内周に位置する電極１２５ｈは、群１（群３）の第８の番目の発光ダイオードと群２（群４）の第１番目の発光ダイオードとを接続するように概略コ字状に形成されている。すなわち、１２ｎ－１番目の群に属する所定の発光ダイオードは、１２×ｎ番目（ｎ＝１・・・Ｎ／１２）の群に属する所定の発光ダイオードに接続している。

【0012】

これに対して、個別電極１２４は、同一群に属する発光素子の逆導電型半導体層１２３に共通的に接続している。また、この個別電極１２４には、それぞれ下地側の接続パッド１２４ａを有している。

【0013】

図１３は、図１２に示す発光ダイオードアレイ部分を除く領域上に、絶縁層１２７を被着形成し、該絶縁層１２７上に形成された電極を示している。この絶縁層１２７上に共通電極１２５を構成する複数の第２の共通電極１２８ａ、１２８ｂ、１２８ｃ、１２８ｄ、１２８ｅ、１２８ｆ、１２８ｇ、１２８ｈが形成されている。この第２の共通電極１２８ａ、１２８ｂ、１２８ｃ、１２８ｄ、１２８ｅ、１２８ｆ、１２８ｇは、１群目からＮ番目の群を互いに接続するために作用する。

【0014】

すなわち、最も外側に形成される直線状の複数の第２の共通電極１２８ａは、各群に跨がって最外周側に形成された複数の第１の共通電極１２５ａどうしを接続するものである。また、さらに内側に形成される直線状の第２の共通電極１２８ｂは、各群に跨がって形成された第１の共通電極１２５ｂどうしを接続するものであり、さらに内側に形成される直線状の第２の共通電極１２８ｃは、各群に跨がって形成された第１の共通電極１２５ｃどうしを接続するものであり、さらに内側に形成される直線状の第２の共通電極１２８ｄは、各群に跨がって形成された第１の共通電極１２５ｄどうしを接続するものであり、さらに内側に形成される直線状の第２の共通電極１２８ｅは、各群に跨がって形成された第１の共通電極１２５ｅどうしを接続するものであり、さらに内側に形成される直線状の第２の共通電極１２８ｆは、各群に跨がって形成された第１の共通電極１２５ｆどうしを接続するものであり、さらに内側に形成される直線状の第１２の共通電極１２８ｇは、各群に跨がって形成された第１の共通電極１２５ｇどうしを接続するものである。

【0015】

また、最も内側に形成される直線状の第１２の共通電極１２８ｈは、各群に跨がって形成された第１の共通電極１２５ｈどうしを接続するものである。

【0016】

そして、各第２の共通電極１２８ａ～１２８ｈの長さは、それぞれ相違しており，この相違によって形成された空白領域には、共通電極１２５の接続パッドが形成されている。図１３では、第２の共通電極１２８ａ及び第２の共通電極１２８ｂに接続する２つの外部接続パッド１２９が形成されているものの、図１３には現れない右側の領域に第２の共通電極１２８ｃ～１２８ｈに接続する接続パッド１２９が形成されている。

【0017】

また、個別電極１２４側には、上述の下地側接続パッド１２４ａに接続する個別側接続パッド１２４ｂが形成されている。

【0018】

この第１の共通電極１２５ａ～１２５ｈ及び第２の共通電極１２８ａ～１２８ｈの電気

的な接続及び個別電極１２４の下地側接続パッドと上側接続パッドとの接続は、絶縁層１２７の形成にあたり、絶縁層１２７の厚み方向に形成した開口を介して接続される。具体的には、第２の共通電極１２８ａ～１２８ｈの両端部が位置する領域に、開口が形成されている。

【特許文献1】特開２００１－３２００８８号

【発明の開示】

【発明が解決しようとする課題】

【0019】

しかしながら、発光ダイオードの動作においては、この所定の共通電極１２５と個別電極１２４とに所定電流を供給して行われる。発光ダイオードアレイにおいては、共通電極１２５そのものの構造が非常に複雑となってしまう。そして、共通電極１２５側の接続部が多いため接続部分での抵抗のバラツキが大きく、その結果発光バラツキを誘発する問題があった。例えば、図１３において、第２の共通電極１２８ａに接続する外部接続パッドから、群１～群４の所定共通電極１２５には、少なくとも１個所の接続部分を介して接続されるが、群５、群６の所定共通電極１２５に接続するまでには、３個所の接続部を経ることになり、群７、群８の所定共通電極１２５には、５個所の接続部が必要になる。

【0020】

このため、所定接続パッド１２９から、それに接続する所定発光ダイオードの共通電極１２５までの接続部分の個数が、各発光素子群によって相違するため、発光バラツキの原因となっていた。

【0021】

また、共通電極１２５の形成時に金属－半導体との接触性（オーミック性）を考慮して形成しているため、共通電極１２５の厚みサイズによる抵抗値とを両立させる必要があることから、金属材料の制約が大きく、材料が限られると言う問題もあった。

【0022】

また、共通電極１２５の形状や厚みについては、コスト増やチップサイズが増大などの問題があるが、さらに、共通電極１２５の材料については、低抵抗低材料の他に、金属－半導体の接触性を両立させる必要がある。

【0023】

第２の共通電極１２８は、その下部に、複雑な構造、例えば共通電極１２５の存在などにより、その表面に凹凸が形成されやすく、非常に平坦性の高い表面にこの電極を形成することが非常に困難となる。これによって、第２の共通電極１２８の電極形成が不安定となり、電極の抵抗バラツキが発生してしまう。

【0024】

接続パッド１２９は、所定第２の共通電極１２８が延長されて接続している。即ち、隣接しあう発光素子群の第２の共通電極１２８との間の非常に狭いスペースに、所定第２の共通電極１２８の延長部、接続パッド１２９を形成する必要があり、第２の共通電極が他の導体と接続してしまうなど接続信頼性が非常に低かった。

【0025】

本発明は上述の問題点に鑑みて案出されたものであり、その目的は、共通電極の構造及び接続構造を改良し、同時に接続パッドから発光ダイオードまで接続部分の個数を極小化させて各共通電極における電極抵抗のバラツキを小さくして発光バラツキを改善するとともに、共通電極の接続信頼性を向上した発光ダイオードアレイ装置を提供するものである。

【0026】

別の目的は、発光バラツキの少ない発光ダイオードアレイ装置を用いて、高品位な画像を形成できるＬＥＤプリンタを提供することにある。

【課題を解決するための手段】

【0027】

本発明の発光ダイオードアレイ装置は、高抵抗基板上に複数の一導電型半導体層と逆導電型半導体層を設け、且つ該一導電型半導体層に共通電極を、逆導電型半導体層に個別電

極を接続した発光ダイオードを複数個配列するとともに、前記複数の配列された発光ダイオードのうち、Ｎ個の発光ダイオードを発光素子群として、Ｍ群から構成される発光ダイオードアレイと、同一の発光素子群内の発光ダイオードの逆導電型半導体層に共通に接続する個別電極と、異なる群に属する所定の発光ダイオードの一導電型半導体層に接続する共通電極とからなる発光ダイオードアレイ装置において、

共通電極は、発光ダイオードの配列方向に概略平行に延びるＮ個の第１の共通電極と、いずれか１つの第１の共通電極と同一の発光素子群のいずれか１つの発光ダイオードとを接続する第２の共通電極とから構成されるとともに

Ｍ群の発光素子群のうち、ｍ番目の発光素子群の各発光ダイオードは、Ｎ個の共通電極のうち発光ダイオードアレイに最も近い側の第１の共通電極から遠い側の第１の共通電極に順次に第２の共通電極を介して接続するとともに、

前記ｍ番目の発光素子群に隣接する発光素子群の各発光ダイオードは、Ｎ個の共通電極のうち発光ダイオードアレイに最も遠い側の第１の共通電極から近い側の第１の共通電極に順次に第２の共通電極を介して接続されていることを特徴とする発光ダイオードアレイ装置である。

【0028】

また、第１の共通電極上には、第１の共通電極と第２の共通電極とを接続するコンタクトホールが形成された絶縁膜によって被覆され、且つ該絶縁基板上に第１の共通電極から共通電極側接続パッドとを接続する引出し配線が形成されているとともに、該引出し配線と第１の共通電極配線は、記前記隣接しあう発光素子群から延びる第２の共通電極の境界部分の絶縁膜に形成した第２のコンタクトホールを介して接続されていることを特徴とする発光ダイオードアレイ装置である。

【0029】

また、上述した発光ダイオードアレイ装置と、該発光ダイオードアレイ装置の駆動を制御する駆動回路と、ページプリンタ用感光ドラムとを少なくとも有し、前記駆動回路によって発光動作する発光ダイオードアレイ装置の光を、前記ページプリンタ用感光ドラムの露光用光源に用いて、該ドラム表面に画像を形成する発光ダイオードプリンタである。

【発明の効果】

【0030】

本発明では、複数の配列された発光ダイオードのうち、所定数の発光ダイオードを一群として、複数群から構成される発光ダイオードアレイと、同一の群内の発光ダイオードの一導電型半導体層に個別電極を接続し、異なる群に属する所定番目に配置された発光ダイオードの逆導電型半導体層に共通電極に接続した発光ダイオードアレイ装置である。

【0031】

共通電極は、発光ダイオードの配列方向に概略平行に延びる第１の共通電極及び該第１の共通電極の一部から各異なる群に属する同一番目に配置された発光ダイオードの逆導電型半導体層に接続する第２の共通電極とから構成されている。そして、Ｍ群の発光素子群のうち、ｍ番目の発光素子群の各発光ダイオードは、Ｎ個の共通電極のうち発光ダイオードアレイに最も近い側の第１の共通電極から遠い側の第１の共通電極に順次に第２の共通電極を介して接続するとともに、

Ｍ群の発光素子群のうち、ｍ番目の発光素子群に隣接する発光素子群の各発光ダイオードは、Ｎ個の共通電極のうち発光ダイオードアレイに最も遠い側の第１の共通電極から近い側の第１の共通電極に順次に第２の共通電極を介して接続されている。このため、ｍ番目の発光素子群に隣接する２つの発光素子群のうち、１つの発光素子群との間には、実質的に三角形状のスペースを有している。

【0032】

この第１の共通電極についていえば、発光ダイオードに直接接続することがなく、金属－半導体のオーミック接触性を全く考慮することなく、その材料を配線抵抗のみを考慮して選択することができる。また、この第1の共通電極は、複数の発光ダイオードアレイの配列方向に略平行に延び、しかも、実質的には発光ダイオードの配列されている略幅に渡

って形成されている。しかも、この第１の共通電極は、高抵抗基板の表面に形成された第１の絶縁膜を介して形成されることになり、非常に導体長が長い電極であっても，その形成を平坦な表面に形成するができ、第１の共通電極を安定、均一に形成することができる。

【0033】

このため、第１の共通電極は材料からしても、また、構造からしても、複数の第１の共通電極をすべて同じ状態で形成できるため、安定した導体膜であり、且つ電極抵抗も大きくなることがない。これにより、第１の共通電極の抵抗バラツキを有効に抑えることができ、発光ダイオードの安定した発光動作を行うことができる。

【0034】

しかし、発光ダイオードから第１の共通電極への接続は、各群のいずれの発光ダイオードについても、第２の共通電極から第１の共通電極へは１個所の接続部（コンタクトホール）のみ行われるため、全体として接続部を数も減少させることができる。しかも、所定の第１の共通電極から共通電極側接続パッドへも１個所の接続部（コンタクトホール）のみ行われるため、全体として共通電極側接続パッドから発光ダイオードへの接続部を数が大きく減少できる。

【0035】

従って、各共通電極における電極抵抗のバラツキを小さくでき、発光ダイオードでの発光バラツキを改善できる。また、共通電極を電極が要求される抵抗特性と、半導体と接続する金属－半導体のオーミック接触性とを両立させることができ、また、導体長さの長い第１の共通電極を低抵抗とすることも容易となり、これによっても、発光ダイオードでの発光バラツキを改善できる。

【0036】

しかも、第１の共通電極から共通電極側接続パッドへの接続部（コンタクトホール）は、上述のm番目の発光素子群に隣接する発光素子群のうち、１つの発光素子群との間に形成される実質的に三角形状のスペースに形成されている。このため、第１の共通電極と共通電極側接続パッド（または共通電極側接続パッドに接続する引出し電極）との接続部が、第１の共通電極と第２の共通電極との接続部から距離的に離して形成できる。このため、第１の共通電極と共通電極側接続パッド（または共通電極側接続パッドに接続する引出し電極）との接続部の接続信頼性が向上する。

【0037】

これにより、外部の駆動回路との接続、例えばボンディングワイヤの融着接合が、高抵抗基板の一方端部側である個別電極形成領域のみで行われるため、その接合作業が非常に簡単となり、発光ダイオードアレイ装置と駆動回路との接合が安定する。

【0038】

これは、ボンィングワイヤに限らず、例えば接続パッドに銀粉末を含有する導電性ペーストを塗布して、この銀バンプと外部の駆動回路とを接続する場合においても、上述の導電性ペーストの塗布が高抵抗基板の一方端部側である個別電極形成領域のみで行われるので、その接合作業が非常に簡単となる。

【0039】

また、このような発光ダイオードアレイ装置を安定した接合状態で駆動回路に接続して、発光制御して発光動作させることにより、ページプリンタ用感光ドラムにバラツキの少ない露光用光源となり、その結果、該ドラム表面に安定した画像を形成することができ、高い品位の印字が可能となる。

【発明を実施するための最良の形態】

【0040】

以下、本発明の発光ダイオードアレイ装置を図面に基づき詳細に説明する。

【0041】

図１～図３は本発明に係る発光ダイオードアレイ装置の一実施形態を示し、図１は本発明の横断面図であり、図２は、発光ダイオード（発光素子部）の要部拡大の断面図であり、

図３は発光ダイオードアレイ装置の平面である。なお、図４は第１の共通電極と第２の共通電極との関係を明瞭にした平面図である。

【0042】

図において、１は高抵抗基板であり、１０は発光ダイオード素子であり、２は発光ダイオード１０を構成する一導電型半導体層であり、３は発光ダイオード１０を構成する逆導電型半導体層であり、４は個別電極であり、５０は共通電極であり、５は第１の共通電極であり、６は第２の共通電極であり、７は高抵抗基板１の表面に形成された第１の絶縁膜であり、８は第１の共通電極５上に被着された第２の絶縁膜であり、本発明でいう絶縁膜とはこの第２の絶縁膜８を指す。

【0043】

高抵抗基板１は、たとえばシリコン（Ｓｉ）やガリウム砒素（ＧａＡｓ）などの単結晶半導体基板やサファイア（Al_2O_3）などの単結晶絶縁基板である。例えば、単結晶半導体基板の場合においては、（１００）面を＜０１１＞方向に２～７°オフさせた基板などが好適に用いられる。サファイアの場合においては、Ｃ面基板が好適である。

【0044】

この高抵抗基板１上の表面中央部領域に、複数の発光ダイオード１０が１列に複数配列されて形成されている。また、基板１上には、この発光ダイオード１０が配列された領域Ｌを挟んで、主に個別電極が形成される個別電極形成領域Ｓと、主に共通電極が形成される共通電極形成領域Ｃを有している。

【0045】

この発光ダイオードの主要部分の構成は、一導電型半導体層２及び逆導電型半導体層３から構成されている。

【0046】

一導電型半導体層２は、バッファ層２ａ、オーミックコンタクト層２ｂ、電子の注入層２ｃで構成される。バッファ層２ａは２～４μｍ程度の厚みに形成され、オーミックコンタクト層２ｂは０．１～１．０μｍ程度の厚みに形成され、電子の注入層２ｃは０．２～０．４μｍ程度の厚みに形成される。バッファ層２ａとオーミックコンタクト層２ｂはガリウム砒素などで形成され、電子の注入層２ｃはアルミニウムガリウム砒素などで形成される。また、オーミックコンタクト層２ｂはシリコンなどの一導電型半導体不純物を１×１０^{16}～１０^{19}ａｔｏｍｓ／ｃｍ^3 程度含有し、電子の注入層２ｃはシリコンなどの一導電型半導体不純物を１×１０^{16}～１０^{19}ａｔｏｍｓ／ｃｍ^3 程度含有する。

【0047】

バッファ層２ａは高抵抗基板１と半導体層との格子定数の不整合に基づくミスフィット転位を防止するために設けるものであり、半導体不純物を含有させる必要はない。

【0048】

この一導電型半導体層２のオーミックコンタクト層２ｂには、共通電極５０が接続される。

【0049】

また、逆導電型半導体層３は、発光層３ａ、第２のクラッド層３ｂおよび第２のオーミックコンタクト層３ｃで構成される。

【0050】

発光層３ａと第２のクラッド層３ｂは０．２～０．４μｍ程度の厚みに形成され、オーミックコンタクト層３ｃは膜厚ｄ＞（０．１５μｍ－オーミックコンタクト層膜厚）程度の厚みに形成される。発光層３ａと第２のクラッド層３ｂはアルミニウムガリウム砒素などから成り、第２のオーミックコンタクト層３ｃはガリウム砒素などから成る。発光層３ａと第２のクラッド層３ｂは、電子の閉じ込め効果と光の取り出し効果を考慮してアルミニウム砒素（ＡｌＡｓ）とガリウム砒素（ＧａＡｓ）との混晶比を異ならしめる。発光層３ａと第２のクラッド層３ｂは亜鉛（Ｚｎ）などの逆導電型半導体不純物を１×１０^{16}～１０^{21}ａｔｏｍｓ／ｃｍ^3 程度含有し、第２のオーミックコンタクト層３ｃは亜鉛などの逆導電型半導体不純物を１×１０^{19}～１０^{21}ａｔｏｍｓ／ｃｍ^3 程度含有する。

【0051】
この逆導電型半導体層３の第２のオーミックコンタクト層３ｃには、個別電極４が接続される。
【0052】
また、高抵抗基板１の共通電極形成領域Ｃ及び個別電極形成領域Ｓの大部分の領域には、第１の絶縁膜７が形成されている。
【0053】
第１の絶縁膜７は、酸化シリコンや窒化シリコンなどが例示できる。基板材料がシリコンである場合、基板表面の熱酸化処理により形成できる。また、その他の基板材料の場合に、シランガス（SiH_4）や必要に応じてアンモニアガス（NH_3）を用いてプラズマＣＶＤ法などによって被着形成する。
【0054】
共通電極５０を構成する第１の共通電極５は、高抵抗基板１の共通電極側領域Ｃの第１の絶縁膜７上に形成される。この第１の共通電極５は、発光ダイオード１０の配列方向に略平行に形成され、その長さは、実質的には、発光ダイオード１０の配列の幅と同等の長さを有している。また、この第１の共通電極は、発光ダイオード１０の駆動の単位である発光素子群を構成する発光ダイオードの構成数（Ｎ）と同一の数だけ形成される。
【0055】
第１の共通電極５は、高抵抗基板１上に形成した平坦な面を有する第１の絶縁膜７上に、例えば、下地導体膜としてＣｒを１５０Å以上形成した後、アルミニウム／金などの順次積層た多層構成などが例示できる。その厚みが例えば１μｍである。なお、下地導体膜を省略して金／クロム（Ａｕ／Ｃｒ）、アルミニウム／クロム（Ａｌ／Ｃｒ）の多層層構造であってもよい。
【0056】
この第１の共通電極５は、発光ダイオード１０の配列幅にわたり、比較的長く形成されているものの、その下面には、平坦な高抵抗基板１の表面に形成された第１の絶縁膜に形成される。即ち、基板の複雑な構造や導体膜がない状態でないため、第１の絶縁膜７の表面が非常に平坦化された表面となり、この平坦な表面に第１の共通電極５を形成されるため、複数の第１の共通電極５において構造的に均一化を図ることができる。また、材料も金を含む非常に良好な導電材料を用いているため、その抵抗のバラツキも抑えることができる。
【0057】
第２の絶縁膜８は、共通電極形成領域Ｃ、個別電極形成領域Ｓの一部、さらには、発光ダイオードの一部に形成されるものであり、例えば透明な材料で構成される。具体的には、ポリイミド合成樹脂、感光性樹脂、窒化シリコン、酸化シリコン、ポリイミドシリコンなどから成る材料などが例示できる。この第2の絶縁膜8の厚みは２０００～２００００Å程度に形成する。
【0058】
この第２の絶縁膜８は、発光ダイオード１０において、少なくともオーミックコンタクト層２ｂ、３ｃを露出するように形成され、さらに、共通電極形成領域Ｃには、２種類の開口（コンタクトホール９、１０）が形成されている。
【0059】
コンタクトホール９は、発光ダイオードのオーミックコンタクト層２ｂと第１の共通電極５を接続する第２の共通電極６が、安定して所定第１の共通電極５に接続するように形成されるものであり、例えば、所定第１の共通電極５の一部を露出するように形成されている。
【0060】
また，コンタクホール１０は、共通電極側接続パッド１２と所定第１の共通電極５を接続する引出し電極１３が、安定して所定第１の共通電極５に接続するように形成されるものである。

【0061】
このような第２の絶縁膜８は、例えば高抵抗基板１の上面に、第２の絶縁膜８となるポリイミド合成樹脂、感光性樹脂、窒化シリコン、酸化シリコン、ポリイミドシリコンなどを被着形成し、その後フォトグラフィ技術を利用して、コンタクトホール９、１０や一導電型半導体層２のオーミックコンタクト層２ｂ、逆導電型半導体層３のオーミックコンタクト層３ｃが露出すようにエッチング処理されて形成されるものである。
【0062】
ここで、コンタクトホール９は、１つの発光素子群の幅に対応する領域に、Ｎ個の第１の共通電極５を順次露出するように形成されている。図３においては、最も右側（右側から奇数番目）の発光素子群に対応するＮ個のコンタクトホール９は、右肩下がりに配列されて形成され、右から２番目（右から偶数番目）の発光素子群に対応するＮ個のコンタクトホール９は、右肩上がりに配列されて形成されている。その結果、第２番目の発光素子群と、第３番目の発光素子群と範囲に対応する共通電極形成領域Ｃには、比較的広い第２の絶縁膜の領域が形成されることになる。
【0063】
コンタクトホール１０は、Ｍ群の発光素子群の幅（アレイの全幅）に対応する領域に、Ｎ個の第１の共通電極５のいずれかを露出するように形成されている。図３においては、右側から１番目の発光素子群と右側から２番目の発光素子群との間に、右側から２数番目の発光素子群と右側から３番目の発光素子群との間に、・・・にそれぞれ形成されている。
【0064】
また、高抵抗基板１の個別電極形成領域Ｓには、複数の個別電極４が形成されている１つの個別電極４は、１つの発光素子群を成す例えば８つ個の発光素子に共通的に接続するように、例えば櫛形状に形成される。即ち、個別電極４は、発光素子群の数Ｍに対応する数だけ形成されている。この個別電極４は、第２の絶縁膜８上に形成され、発光ダイオード１０の逆導電型半導体層３ｃに接続される。
【0065】
また、各個別電極４は、個別電極側接続パッド１１を有している。また、個別電極側接続パッド１１も第２の絶縁膜８に形成されている。なお、個別電極側接続パッド１１と外部駆動回路との接続手法によっては、第２の絶縁膜８が除外されて第１の絶縁膜７上に形成してもよい。
【0066】
高抵抗基板１の共通電極形成領域Ｃには、複数の第２の共通電極６が形成されている。１つの第２の共通電極６は、１つの発光ダイオードの一導電型半導体層２のオーミックコンタクト層２ｂから所定のコンタクホール９から露出する第１の共通電極５を接続するために形成されている。即ち、第１の共通電極５は、発光ダイオード１０の配列方向に平行に延びているが、第２の共通電極６は、それと直交する方向に形成されている。
【0067】
これより、発光素子群を構成するＮ個の発光ダイオード１０は、それぞれ異なる第１の共通電極５に接続することになる。
【0068】
また、各第１の共通電極５には、それぞれ１つの共通電極側接続パッド１２に接続されている。この共通電極側接続パッド１２は、例えば個別電極形成領域Ｓ側に形成されている。そして、この共通電極側接続パッド１２と所定の第１の共通電極５は、引出し電極１３によってコンタクトホール１０を介して接続されている。なお、共通電極側接続パッド１２も第２の絶縁膜８に形成されているが、虚通電極側接続パッド１２と外部の駆動回路との接続手法によっては、第２の絶縁膜８が除外されて第１の絶縁膜７上に形成してもよい。
【0069】
また、この引出し電極１３は、各発光素子群との境界部分の間隙に、第２の絶縁膜８

上に形成されている。これにより、共通電極形成領域Ｃに形成されたコンタクトホール１０と個別電極形成領域Ｓに形成された共通電極側接続パッド１２とが引出し電極１３が接続されている。

【0070】

この第２の共通電極６や個別電極４は、オーミックコンタクト層２ｂ、３ｃに接触する電極である。このため、金／金・ゲルマニウム／クロム（Ａｕ／ＡｕＧｅ／Ｃｒ）などのから成る多層構造となっており、その厚み１μｍ程度以下に形成される。なお、この多層構造の材料を熱処理を加えて、Geを半導体層に拡散処理している。

【0071】

なお、引出し電極１３は、第２の共通電極６、個別電極４と同一工程で形成することが望ましいが、金属－半導体オーミック接触性を考慮することなく、良導電体材料を用いて構わない。また、接続パッド１１、１２の上面にも、引出し電極１３と同一の良導電体材料を被着形成してもよい。

【0072】

以上の構成した発光ダイオードアレイ装置では、高抵抗基板１の共通電極形成領域Ｃでは、高抵抗基板１上に第１の絶縁膜７が形成され、さらに、第１の共通電極５が形成され、さらに、第１の共通電極５上には第２の絶縁膜８が形成されおり、第２の絶縁膜８を介して第２の共通電極６または引出し電極１３が形成ささている構造である。

【0073】

また、高抵抗基板１の個別電極形成領域Ｓでは、高抵抗基板１上に第１の絶縁膜７、第２の絶縁膜８が形成されており、この第２の絶縁膜８上に個別電極４、個別電極側接続パッド１１、共通電極側接続パッド１２、引出し電極１３が形成されている。なお、個別電極側接続パッド１１、共通電極側接続パッド１２の直下においては、第２の絶縁膜８を省略してもよい。

【0074】

次に、図３、図４を用いて、発光ダイオードアレイ装置の電極及び接続パッド構造を詳細に説明する。

【0075】

上述の構成の発光ダイオードは、複数アレイ状に配置され、例えば、隣接するＮ個（図３、図４では８個）の発光ダイオード（素子）が１つの群として取り扱われる。図３、図４では、右側からは第１の群から第４群までの３２（８素子×４群）素子が示されているが、全体としては、Ｍ群の発光素子群を有している。

【0076】

図３、図４に示す高抵抗基板１の図の下側領域である個別電極形成領域Ｓには、１つの発光素子群を成す８つ個の発光素子に共通的に接続するように、例えば櫛形状の個別電極４が形成されている。そして、この櫛状の個別電極４には個別電極側接続パッド１１が１つ形成さている。なお、隣接する群も個別電極４の構成は同様となっている。

【0077】

つぎに、共通電極５０について言えば、第１の共通電極５と第２の共通電極６とか構成されているが、図４に示すように、第１の共通電極５は、発光ダイオードの配列方向と平行に延びるように形成されている。第１の共通電極５は、例えば発光素子群の群数Ｍに係わらず、１つの発光素子群を構成する発光ダイオード１０の数Ｎ（図ではＮ＝８）に相当する数だけ形成されている。この例では第１の共通電極５は８つの電極で構成されている。また、第２の共通電極６は、各発光ダイオードと第１の共通電極５とを接続するものであり、各発光ダイオードから第１の共通電極５のいずれかに接続するように発光ダイオードの配列方向と直交する方向に延びて形成されている。そして、第２の共通電極６の一端は１つの発光タダイオードの一導電型半導体層２のオーミックコンタクト層２ｂに重畳接続し、他端はコンタクトホール９を介して所定第１の共通電極５の一部に重畳接続する。即ち、第２の共通電極６は発光素子群１つから素子数Ｎ（例ではＮ＝８）だけ延びており、全体として、Ｎ素子×Ｍ群だけ形成されている。

【0078】
ここで、第１の共通電極５に関しては、例えば８つの第１の共通電極を区別するためには、発光ダイオードアレイに近い側から符号５ａ、５ｂ、５ｃ・・５ｈ（例では１発光素子群が８素子で構成されているためＮ＝８、最終符号は５ｈとなる）で示す。また、第２の共通電極６に関しては、例えば最も右側の発光素子群を構成する発光ダイオードで、第１の共通電極５ａに接続する第２の共通電極を符号６１ａ、そのコンタンクトホール９１ａ、第１の共通電極５ｂに接続する第２の共通電極を符号６１ｂ、そのコンタンクトホール９１ｂ、・・・・・第１の共通電極５ｈに接続する第２の共通電極を符号６１ｈ、そのコンタンクトホール９１ｈと示し、右側から２番目の発光素子群を構成する発光ダイオード１０で第１の共通電極５ａに接続する第２の共通電極を符号６２ａ、そのコンタンクトホール９２ａ、第１の共通電極５ｂに接続する第２の共通電極を符号６２ｂ、そのコンタンクトホール９２ｂ、・・・・・第１の共通電極５ｈに接続する第２の共通電極を符号６２ｈ、そのコンタンクトホール９２ｈと示す。

【0079】
この図３、図４で、右側から第１番目、３番目、５番目・・・（奇数番目）の発光素子群の発光ダイオードで、第２の共通電極を介して第１の共通電極５ａに接続する発光ダイオードは、発光素子群中最も右側に形成されものであり、第１の共通電極５ｈに接続する発光ダイオードは、発光素子群中最も左側に形成されものであり、右側から第２番目、４番目、６番目・・・（偶数番目）発光素子群の発光ダイオードで、第２の共通電極を介して第１の共通電極５ａに接続する発光ダイオードは、発光素子群中最も左側に形成されものであり、第１の共通電極５ｈに接続する発光ダイオードは、発光素子群中最も右側に形成されものであり、奇数番目の発光素子群と偶数番目の発光素子群と対象に配置されている。

【0080】
これにより、Ｍ群の発光素子群のうち、ｍ番目の発光素子群の各発光ダイオードは、Ｎ個の共通電極のうち発光ダイオードアレイに最も近い側の第１の共通電極５ａから遠い側の第１の共通電極５ｈに順次に第２の共通電極６を介して接続するとともに、Ｍ群の発光素子群のうち、ｍ番目の発光素子群に隣接する発光素子群の各発光ダイオードは、Ｎ個の共通電極のうち発光ダイオードアレイに最も遠い側の第１の共通電極５ｈから近い側の第１の共通電極５ａに順次に第２の共通電極６を介して接続されている。このため、ｍ番目の発光素子群に隣接する２つの発光素子群のうち、１つのは発光素子群との間には、実質的に三角形状のスペースＸが形成される。

【0081】
また、第１の共通電極５ａの一部は、共通電極側接続パッド１２ａに接続されており、第１の共通電極５ｂの一部は共通電極側接続パッド１２ｂに接続されており、・・・第１の共通電極５ｈの一部は共通電極側接続パッド１２ｈに接続されている。

【0082】
具体的には、図３、図4では第１の共通電極５ａに接続する共通電極側接続パッド１２ａは、第１番目の発光素子群と第２番目の発光素子群との境界部分を介して、個別電極形成領域Ｓ側に延び、個別電極側接続パッド１１に並設されている。また、第１の共通電極５ｂに接続する共通電極側接続パッド１２ｂは、第２番目の発光素子群と第３番目の発光素子群との境界部分を介して、個別電極形成領域Ｓ側に延び、個別電極側接続パッド１１に並設されている。このとき、第１の共通電極５ａと共通電極側接続パッド１２ａとは、コンタンクホール１０ａ、引出し電極１３を介して行われる。同様に、第１の共通電極５ｂ～５ｈと共通電極側接続パッド１２ｂ～１２ｈとは、コンタンクホール１０ｂ～１０ｈ、引出し電極１３を介して行われる。

【0083】
尚、図では省略しているが、共通電極側接続パッド１２を、上述のコンタクトホール１０ａ～１０ｈの形成領域を含む領域、即ち、上述の三角形状のスペースＸに形成してもよい。このときには、１つの三角形状のスペースＸに１つの第１の共通電極５に接続する１

つの共通電極側接続パッド１２を形成する。しかも、この共通電極側接続パッド１２の形成領域の直下にコンタクトホール１０ａ～１０ｈを位置させれば、引出し電極が省略できる。

【0084】

このような接続構造において、各発光素子群に係わらず、各発光タイオードの共通電極５０側においては、第２の共通電極６、コンタンクホール９を介して、所定の第１の共通極５ａ～５ｈのいずれかに接続し、さらに各第１の共通電極５ａ～５ｈから１つのコンタンクホール１０ａ～１０ｈを介して共通電極側接続パッド１２ａ～１２ｈに接続している。

【0085】

このような発光ダイオードアレイ装置は、外部の駆動回路によって、個別電極４と共通電極５０とが同時にと選択された発光ダイオード１０に電圧が印加され、その結果、それに対応する発光ダイオードが発光することになる。

【0086】

例えば、第１の共通電極５ａに相当する共通電極を選択することにより、発光し得る発光ダイオードは、各発光素子群内で１つの発光ダイオードだけとなる。即ち、図３、図４においては、右側から奇数番目の発光素子群の最も右側の発光ダイオードと、同じく偶数番目の発光素子群の最も左側の発光ダイオードに限られる。

【0087】

この時、発光素子群に共通的に接続される個別電極４で、どの発光素子群に選択するかによって、選択された発光素子群の上述の発光ダイオード１０に発光に必要な電圧が印加されて発光することになる。

【0088】

このように、第１の共通電極５ａ～５ｈに相当する共通電極５０のうち、どれの共通電極５０を選択し、個別電極４側でどの発光素子群を選択するかによって、アレイ状に配置された発光ダイオードのうち、どの発光ダイオードを発光させるかを制御できる。

【0089】

このように、個別電極４で、発光させるべき対象の発光ダイオードを含む発光素子群を選択し、共通電極５０側の第１の共通電極５ａ～５ｈを順次選択切り替えてすべての発光ダイオードを独立に制御することができる。

【0090】

しかも、発光ダイオードの配列数、即ち、発光されるビット数が６４ｂｉｔ（Ｎ＝８、Ｍ＝８）であっても、１９２ｂｉｔ（Ｎ＝８、Ｍ＝２４）であっても、８つの第１の共通電極で簡単に駆動制御が可能である。この第２の共通電極５の数は、発光素子群を構成する発光ダイオードの数に相当する数で、簡単に発光ダイオードの発光制御が可能である。

【0091】

なお、この構造は、１系統の駆動回路で発光制御することを前提として説明しているものであり、２系統の駆動回路で制御する場合には、この発光ダイオードアレイ装置を、１つの高抵抗基板１上に並設するようにしても構わない。

【0092】

このように、本発明の発光ダイオードアレイ装置によれば、複数の発光ダイオードの発生を制御するための個別電極４、共通電極５０の第１の共通電極５、第２の共通電極６とが全く別の構造で形成されており、且つ第１の共通電極５の導体材料と第２の共通電極６とを全く別の材料で構成することができる。例えば第１の共通電極５を、配線抵抗（電極抵抗）を小さくするための構造、材料を容易に選択でき、また、第２の共通電極６を、半導体－金属の接触性を考慮して、また、第１の共通電極５との接続性を考慮して、それぞれの特性が良好にするための構造、材料を選択できる。

【0093】

しかも、各発光ダイオード１０から共通電極側接続パッド１２までの接続点、例えばコンタクトホール９、１０の数を、各発光ダイオード１０で均一化することができる。

【0094】
これにより、従来例に示した発光ダイオードアレイ装置に比較して、共通電極側における発光ダイオードから共通電極側接続パッドまでの接続点の数を減少でき、また、目的に応じて導体材料の選択の容易となり、その結果、各発光ダイオードにおける共通電極５の電極抵抗のバラツキが極小化でき、発光バラツキを小さくすることができる。
【0095】
また、第１の共通電極５は、発光ダイオードアレイの配列方向に平行に形成され、第２の共通電極６は、各発光ダイオーと第１の共通電極５とを接続するように形成されている。即ち、第２の共通電極６の幅を、実質的に発光ダイオードの幅よりも小さく設計することで、発光ダイオードアレイの配列方向の寸法を極小化することができる。
【0096】
さらに、共通電極側接続パッド１２は、発光ダイオード１０の配列領域Ｌを挟んで設けられる個別共通電極形成領域Ｓに形成されている。即ち、共通電極が形成された共通電極形成領域Ｃから個別電極形成領域Ｓに、発光素子群との境界部分に形成された引出し電極１３によって接続され、この個別電極形成領域Ｓには個別電極側接続パッド１１、共通電極側接続パッド１２とが並設されている。
【0097】
これにより、外部の駆動回路との接続、例えばボンディングワイヤの融着接合が、高抵抗基板の一方端部側である個別電極形成領域のみで行われるため、その接合作業が非常に簡単となり、発光ダイオードアレイ装置と外部の駆動回路との接合が安定する。
【0098】
これは、ボンィングワイヤに限らず、例えば接続パッドに銀粉末を含有する導電性ペーストを塗布して、この銀バンプと外部の駆動回路とを接続する場合においても、上述の導電性ペーストの塗布が高抵抗基板の一方端部側である個別電極形成領域のみで行われるので、その接合作業が非常に簡単となる。
【0099】
しかも、第１の共通電極５から共通電極側接続パッド１２への接続部（コンタクトホール１０）は、上述のｍ番目の発光素子群に隣接する発光素子群のうち、１つの発光素子群との間に形成される実質的に三角形状のスペースＸに形成されている。このため、第１の共通電極５と共通電極側接続パッド１２（または共通電極側接続パッド１２に接続する引出し電極１３）との接続部（コンタクトホール１０）が、第１の共通電極５と第２の共通電極６との接続部（コンタクトホール９）から距離的に離して形成できる。このため、第１の共通電極と共通電極側接続パッド（または共通電極側接続パッドに接続する引出し電極１３）との接続部の接続信頼性が向上する。
【0100】
また、共通電極を電極が要求される抵抗特性と、半導体と接続する金属－半導体のオーミック接触性とを両立させることができ、また、導体長さの長い第１の共通電極を低抵抗とすることも容易となり、これによっても、発光ダイオードでの発光バラツキを改善できる。
【0101】
このよう発光ダイオードアレイ装置は、ＬＥＤプリンタの露光用光源として用いられる。即ち、ＬＥＤプリンタは、その主要部分の構成は、ページプリンタ用感光ドラム、この感光体ドラム上に画像を形成するための露光光源手段である発光ダイオードアレイ装置、このプリントすべき画像情報、感光体ドラムの回転測度に応じて、発光させるべき発光ダイオードの駆動を制御する駆動回路と、ドラムに電荷を印加または除去する手段、トナーを供給する手段、ドラム上に付着するトナーを記録媒体に転写する転写手段、記録媒体に転写したトナーを定着する定着手段、記録媒体を搬送する搬送手段、ドラム上の不要なトナーを除去するクリーニング手段とから構成されている。
【0102】
このようなＬＥＤプリンタにおいて、露光光源である発光ダイオードアレイ装置の発光

バラツキがすくないため、非常に安定した画像を感光体ドラムに形成することができ、よって、記録媒体に印刷される画像が非常に高品位とすることができる。

【0103】

また、このような発光ダイオードアレイ装置を安定した接合状態で駆動回路に接続して、発光制御して発光動作させることにより、その結果、該ドラム表面に安定した画像を形成することができ、高い品位の印字が可能となる。

【0104】

次に、図５～図１０及び図３、図４を用いて発光ダイオードアレイ装置の製造方法を説明する。

【0105】

まず、図５において、単結晶材料からなる高抵抗基板１を用意するとともに、その全面に第１の絶縁膜７となる絶縁膜７１を形成する。絶縁膜７１は、酸化シリコンや窒化シリコンなどが例示で、基板材料よっては、基板表面を熱酸化処理に形成したり、また、プラズマＣＶＤ法で、シランガス（SiH_4）や必要に応じてアンモニアガス（NH_3）を用いて被着形成する。

【0106】

つぎに、図６に示すに、発光ダイオード１０が形成される領域Ｌのみを、配列方向に沿って絶縁膜７１をエッチング処理して、共通電極形成領域Ｃ、個別電極形成領域にＳに第１の絶縁膜７を形成する。

【0107】

つぎに、図７、図８に示すように、高抵抗基板１が露出する配列領域Ｌに、一導電型半導体層２及び逆導電型半導体層３をＭＯＣＶＤ法などで順次積層して発光ダイオード１０の主要部分を形成する。これより、図２に示すように一導電型半導体層２は、バッファ層２ａ、オーミックコンタクト層２ｂ、電子の注入層２ｃからなり、逆導電型半導体層３は、発光層３ａ、第２のクラッド層３ｂおよび第２のオーミックコンタクト層３ｃからなる発光ダイオードの主要部分が形成される。なお、一導電型半導体層２、逆導電型半導体層３を形成する場合、高抵抗基板１を４００～５００℃に設定して２００～２０００Åの厚みにアモルファス状のガリウム砒素膜を形成した後、基板温度を７００～９００℃に上げて所望厚みの半導体層２、３を形成する。この場合、原料ガスとしてはＴＭＧ（$(CH_3)_3Ga$）、ＴＥＧ（$(C_2H_5)_3Ga$）、アルシン（AsH_3）、ＴＭＡ（$(CH_3)_3Al$）、ＴＥＡ（$(C_2H_5)_3Al$）などが用いられ、導電型を制御するためのガスとしては、シラン（SiH_4）、セレン化水素（H_2Se）、ＴＭＺ（$(CH_3)_3Zn$）などが用いられ、キャリアガスとしては、H_2などが用いられる。

【0108】

そして、隣接する発光ダイオード１０どうしが電気的に分離されるように、一導電型半導体層２、逆導電型半導体層が島状にパターニングされる。このエッチングは、硫酸過酸化水素系のエッチング液を用いたウェットエッチングやCCl_2F_2ガスを用いたドライエッチングなどで行われる。

【0109】

その後、一導電型半導体層２の一端部側の一部が露出し、且つこの一導電型半導体層２の隣接する領域部分が露出するように逆導電型半導体層３が一導電型半導体層２よりも幅狭に形成されるように逆導電型半導体層３をエッチングする。このエッチングも硫酸過酸化水素系のエッチング液を用いたウェットエッチングやCCl_2F_2ガスを用いたドライエッチングなどでおこなわれる。

【0110】

次に、図９に示すように高抵抗基板１の共通電極形成領域Ｃの絶縁膜７上に第１の共通電極５ａ～５ｈを形成する。具体的にはクロムと金を順次蒸着法やスパッタリング法で多層化された金属膜を形成しパターン化する。この形成にあたっては、パターン化の際にエッチング液が発光ダイオードの主要部分に及ぼす影響を考慮して、リフトオフ法によって形成する。

【0111】
つぎに、図１０に示すように第２の絶縁膜８を形成する。この絶縁膜８の形成において、同時に、複数のコンタクトホール９、１０が形成される。具体的には、全体にポリイミド合成樹脂、感光性樹脂、窒化シリコン、酸化シリコン、ポリイミドシリコンなどから成る材料で絶縁膜を厚み２０００～２００００Å程度に形成する。その後、フォトグラフィ技術を利用して、少なくともコンタクトホール９、１０、一導電型半導体層２のオーミックコンタクト層２ｂ、逆導電型半導体層３のオーミックコンタクト層３ｃが露出すようにエッチング処理しその後レジスト膜を剥離する。
【0112】
最後に、図４に示すように、高抵抗基板１の第２の絶縁膜８上に、個別電極４、第２の共通電極６、個別電極側接続パッド１１、共通電極側接続パッド１２を被着形成する。
【0113】
このうち、第２の共通電極６は、高抵抗基板１の中央付近に配列された発光ダイオードの配列ラインを挟み、一方側、例えば図面の上部側の第２の絶縁膜８に形成され、個別電極４、第２の共通電極６、接続パッド１１、１２は、他方側、例えば図面の下部側の第２の絶縁膜８に形成される。即ち、第２の共通電極６は、発光ダイオードの一導電型半導体層２のオーミックコンタクト層２ｃと、所定の第１の共通電極５が露出するコンタクトホール９に跨がるように形成される。また、第１の共通電極５とこの共通電極５と接続する接続パッド１１とは、コンタンクホール１０から発光素子群で区分される境界部分の間を介して延びる引出し電極１３によって、共通電極側接続パッド１２に接続されている。
【0114】
これらの第２の共通電極６、個別電極４とは、半導体－金属接触性を考慮した材料を用いる必要があり、接続パッド１１、１２は半導体－金属接触性を考慮する必要はない。従って、この第２の共通電極６、個別電極４、個別電極側接続パッド１１、共通電極側接続パッド１２とを同一工程で形成してもよいし、例えば、第２の共通電極６、個別電極４を半導体－金属接触性の良好な材料、良好な層構成で形成し、その後、個別電極側接続パッド１１、共通電極側接続パッド１２のみを良導電性の材料で形成しても構わない。
【0115】
たとえば、個別電極４、第２の共通電極6、個別電極側接続パッド１１、共通電極側接続パッド１２を同時に形成する場合に半導体－金属接触性を考慮して、クロムと金ゲルマニウムと金を蒸着法やスパッタリング法で順次積層して、Cr／AuGe／Auの層構成とすればよい。
【0116】
以上のようにして製造された発光ダイオードアレイ装置は、高抵抗基板１上に複数の一導電型半導体層２と逆導電型半導体層３を被着形成し、且つ該一導電型半導体層２に共通電極５０を、逆導電型半導体層３に個別電極４を接続した発光ダイオード１０を複数個配列するとともに、前記複数の配列された発光ダイオード１０のうち、所定数の発光ダイオード１０を一つの発光素子群として、複数発光素子群から構成される発光ダイオードアレイと、同一の群内の発光ダイオード１０の逆電型半導体層３に個別電極４を接続し、異なる群に属する所定番目に配置された発光ダイオードの一導電型半導体層２に共通電極５０に接続した発光ダイオードアレイ装置である。そして、共通電極５０は、発光ダイオード１０の配列方向に概略平行に延びる第１の共通電極５及び該第１の共通電極５の一部から各異なる群に属する所定の発光ダイオード１０の一導電型半導体層２に接続する第２の共通電極６とから構成される。
【0117】
なお、第１の共通電極５は、高抵抗基板１上に形成した第１の絶縁膜７上に形成され、前記第２の共通電極６と第１の共通電極５との間には、第２の絶縁膜８が介在され、第２の共通電極６の一部が、コンタンクトホール９を介して第１の共通電極５に重畳して接続されている。
【0118】

これにより、第１の共通電極５を、発光素子群を構成する発光ダイオード１０の数に相当する数だけ形成され、各発光ダイオード１０は、第２の共通電極６を介して、所定の第１の共通電極５に接続されている。この第２の共通電極６は、どの発光素子群に属する発光ダイオード１０でありながら、その接続構造は、実質的に同一構造となる。即ち、どの発光ダイオード１０であっても、接続部であるコンタクホール９は１個所のみとなる。これにより、発光ダイオード１０に接続する共通電極５０の構造が非常に簡素化し、接続条件が均一となるため、電極における抵抗のバラツキが小さく、これにより、発光ダイオードの発光バラツキを小さくすることができる。

【0119】

また、第１の共通電極５と第２の共通電極６、個別電極側接続パッド１１、共通電極側接続パッド１２をそれぞれ別の導体材料で構成できるため、第２の共通電極６、個別電極４では、安定した金属－半導体接触性を考慮した材料を、第１の共通電極５では、良好な導電性を考慮した材料を選択できるため、これによっても、電極抵抗のバラツキが小さくなり、これにより、発光ダイオードの発光バラツキを小さくすることができる。

【0120】

また、第１の共通電極５が高抵抗基板１に形成した第１の絶縁膜７上に形成されている。この絶縁膜７の下部には、基板の凹凸の構造物、他の導体膜の凹凸が一切ない、この絶縁膜７の表面が非常に平坦化することになる。このため、第１の共通電極５を非常に安定した形成できる。これより、第１の共通電極５は構造的にバラツキが少ないものとなる。

【0121】

また、個別電極側接続パッド１１、共通電極側接続パッド１２は、発光ダイオードの配列領域を中心に個別電極形成領域Ｓに集中されており、共通電極５０（第１の共通電極５及び第２の共通電極６の接続構造）は、発光ダイオード１０の共通電極形成領域Ｃに集中されている。

【0122】

これにより、外部の駆動回路との接続が一方側の領域のみで行われるため、駆動回路の接続が容易となる。

【0123】

また、個別電極側接続パッド１１、共通電極側接続パッド１２の下部領域には、従来のように共通電極などが全く配置されていない。従って、この接続パッド１１、１２と駆動回路が形成された回路基板とを接続するにあたり、個別電極側接続パッド１１、共通電極側接続パッド１２に半田バンプなどのように半田接合やボンディングワイヤによる接合をおこなっても、熱衝撃や機械的衝撃が個別電極側接続パッド１１、共通電極側接続パッド１２接続パッド１１、１２に印加されても、共通電極や個別電極の接続構造に悪影響を与えることが一切なく、安定した発光動作が可能となる。

【図面の簡単な説明】

【0124】

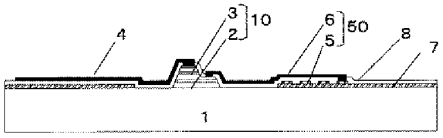
【図1】本発明に係る発光ダイオードアレイ装置の概略断面図である。
【図2】本発明に係る発光ダイオードの主要部分の断面図である。
【図3】本発明に係る発光ダイオードアレイ装置の平面図である。
【図4】本発明に係る発光ダイオードアレイ装置の電極構造を示す平面図である。
【図5】本発明に係る発光ダイオードアレイ装置の製造方法の一工程の平面図である。
【図6】本発明に係る発光ダイオードアレイ装置の製造方法の一工程の平面図である。
【図7】本発明に係る発光ダイオードアレイ装置の製造方法の一工程の平面図である。
【図8】本発明に係る発光ダイオードアレイ装置の製造方法の一工程の平面図である。
【図9】本発明に係る発光ダイオードアレイ装置の製造方法の一工程の平面図である。
【図10】本発明に係る発光ダイオードアレイ装置の製造方法の一工程の平面図である。
【図11】従来の発光ダイオードアレイ装置の主要部分の断面図である。
【図12】従来の発光ダイオードアレイ装置の下部側電極を説明する平面図である。
【図13】従来の発光ダイオードアレイ装置の上部側電極を説明する平面図である。

【符号の説明】

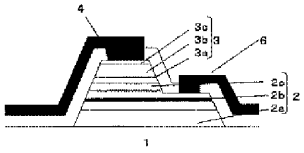
【0125】

１・・高抵抗基板
１０・・発光ダイオード
２・・・一導電型半導体層
　２ａ・・・バッファ層
２ｂ・・オーミックコンタクト層・・・第２の共通電極
２ｃ・・電子の注入層
３・・・逆導電型半導体層
　　３ａ・・・発光層
　　３ｂ・・・第２のクラッド層
　　３ｃ・・・第２のオーミックコンタクト層３・・・個別電極
４・・個別電極
５０・・・共通電極
　５・・・第１の共通電極
　６・・・第２の共通電極
７・・・第１の絶縁膜
８・・・第２の絶縁膜
９・・・コンタクトホール
１０・・コンタクトホール
１１・・個別電極側接続パッド
１２・・共通電極側接続パッド
１３・・引出し電極

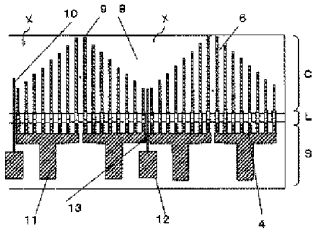
【図1】



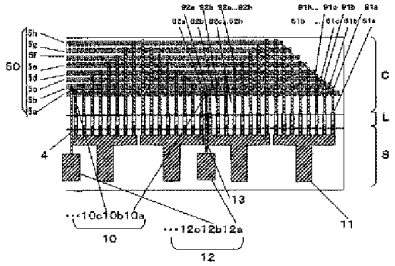
【図2】



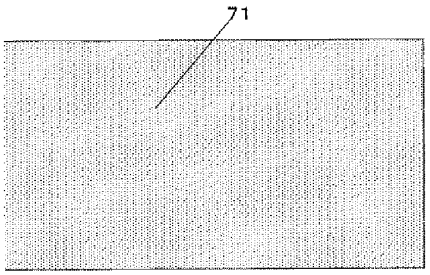
【図3】



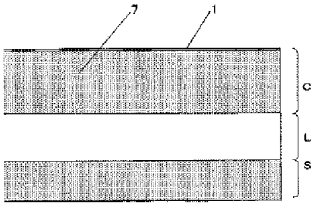
【図4】



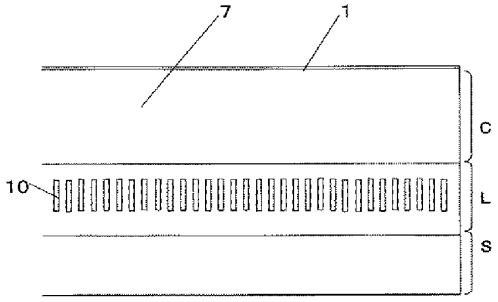
【図5】



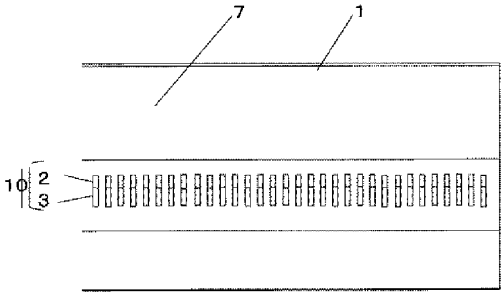
【図6】



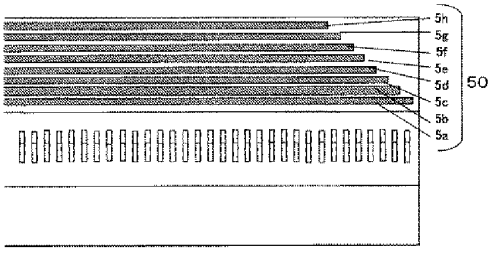
【図7】



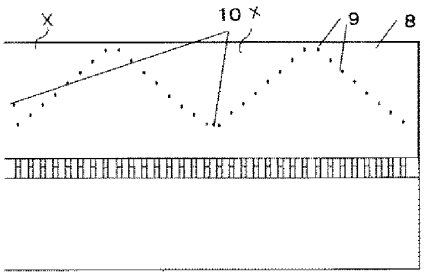
【図8】



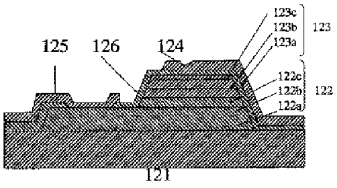
【図9】



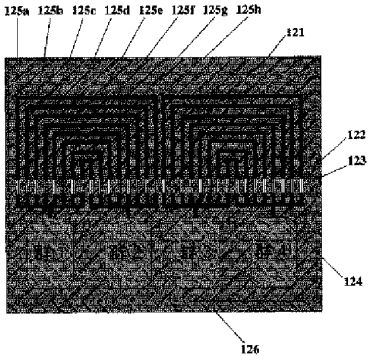
【図10】



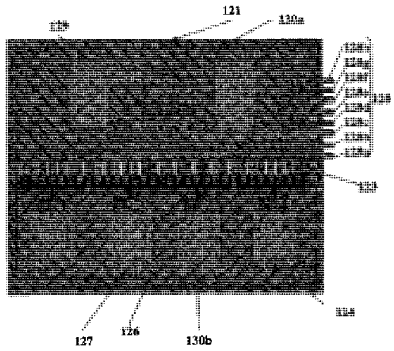
【図11】



【図12】



【図13】



PATENT ABSTRACTS OF JAPAN

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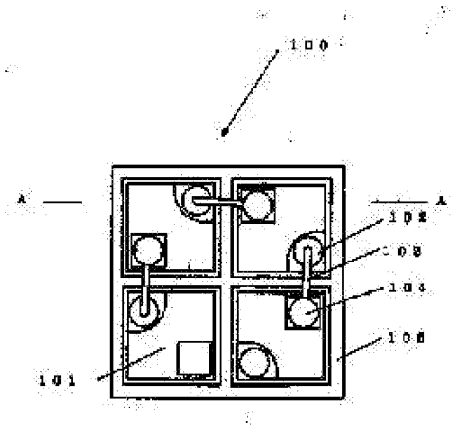
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(71)Applicant : NICHIA CHEM IND LTD
(72)Inventor : KOMAKI TOSHIO
KITANO AKIYUKI

(54) NITRIDE SEMICONDUCTOR LIGHT EMITTING ELEMENT

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a nitride semiconductor light emitting element which utilizes a nitride semiconductor and can emit high-luminance light at a high luminous efficiency.
SOLUTION: The light emitting element is constituted by laminating nitride semiconductors containing at least Ga upon a substrate in p- and n-type. Particularly, a plurality of nitride semiconductor layers is formed on the same film- forming substrate in a state where the layers are electrically separated from each other and each nitride semiconductor layer is electrically connected with a conductive wire.



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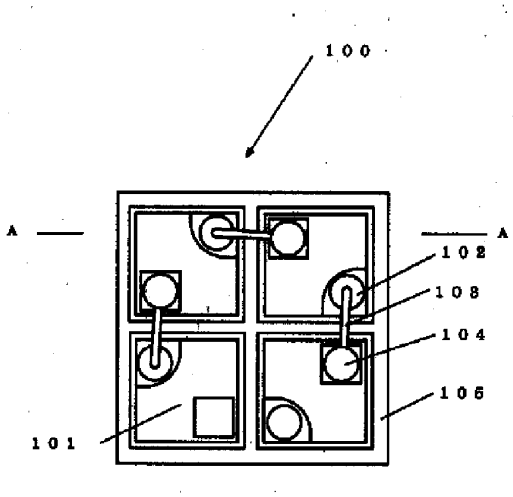
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(71)出願人　000226057
日亜化学工業株式会社
徳島県阿南市上中町岡491番地100
(72)発明者　小牧　稔生
徳島県阿南市上中町岡491番地100　日亜化学工業株式会社内
(72)発明者　北野　晃行
徳島県阿南市上中町岡491番地100　日亜化学工業株式会社内

Ｆターム(参考)　5F041 AA03 CA34 CA40 CA74 CB25 DA07

(54)【発明の名称】　窒化物半導体発光素子

(57)【要約】
【課題】窒化物半導体を利用した発光素子に関わり、特に発光効率を高めより高輝度に発光可能な窒化物半導体発光素子を提供するものである。
【解決手段】少なくともＧａを含む窒化物半導体が基板上にｐ型及びｎ型に積層された有する発光素子である。特に、窒化物半導体層は同一成膜基板上で電気的に複数分離してなり、それぞれの窒化物半導体層が導電性ワイヤで電気的に接続されている窒化物半導体発光素子である。



ていると考えられる。次に、発光効率を向上させるために、同一成膜基板上を複数の窒化物半導体を積層させ、それぞれの電極を導電性ワイヤを用いて電気的に接続させた場合、直並列接続の組合せによっては極めて狭い箇所に方向性なく強固にワイヤを密着させる必要がある。このような場合、ボールボンディングを利用し、ステッチボンディング上には再びボールを形成させることで安定性よく密着性を向上させることができる。特に、本発明のごときく極めて狭い空間でもワイヤボンディングさせる場合は、同一成膜基板にステッチボンド及びボールボンドを続けて行っても安定して密着性よく形成することができる。

【００１０】以下、本発明の窒化物半導体発光素子について図1を用いて説明する。図１は本発明の窒化物半導体発光素子を示した模式的平面図であり、図２は図１のＡＡ断面図である。略矩形状のサファイア基板１０５上に複数の島状に分離した窒化物半導体層１０１が形成されている。島状に分離した窒化物半導体層１０１はそれぞれがサファイア基板１０５上に、ＧａＮを用いたバッファ層２０１、ｎ型コンタクト層となるＧａＮ２０２、ＩｎＧａＮとＧａＮとを複数組積層させた量子井戸構造とされる発光層２０３、ｐ型クラッド層となるＡｌＧａＮ２０４、ｐ型コンタクト層となるＧａＮ２０５が順次積層されている。ｐ型コンタクト層上にはほぼ全面に透光性電極２０６及びその上にｐ型台座電極２０７が設けられている。他方、エッチングにより矩形状窒化物半導体の一部を部分的に除去してｎ型コンタクト層を露出させてある。なお、ｎ型コンタクト層の露出とサファイア基板上に各窒化物半導体を島状に分離させることをエッチングにより同時に行うこともできる。ｎ型コンタクト層上にはｎ型の台座電極が形成されており、平面状から見てｐ型台座電極とｎ型台座電極とが矩形形状の対向する隅部に配置されている。また、島状に分離された各ｐ型及びｎ型の台座電極は、サファイア基板の外周状に沿って隣り合う島状の窒化物半導体と近接して配置されている。少なくとも一箇所のｐ型及びｎ型台座電極間は金線を利用してダイボンド接続され直列接続されている。台座電極間が近接して配置されているために、金線の使用量が極めて少なくてすむ。また、対向する隅部に各ｐ型及びｎ型の台座電極が設けられていることにより、島状に分離した窒化物半導体層から均一に発光することができる。さらに、サファイア基板の外周に沿ってｐ型及びｎ型の台座電極が設けられていることにより、窒化物半導体発光素子の中心光度を向上させることができる。そのため、このような発光素子をレンズ効果のあるモールド部材で被覆させるときには光学設計を極めて簡単に行うことができる。なお、各島状の窒化物半導体層を電気的に絶縁するために絶縁性保護膜２０８を形成してもよい。

【００１１】図中では４個の島状に分離させたｐ型及びｎ型がそれぞれ積層された窒化物半導体を金線で３箇所直列に接続させてある。金線にて接続させていない隣接する窒化物半導体層上のｐ型及びｎ型の台座電極は、窒化物半導体発光素子のｐ電極及びｎ電極として機能することとなる。各ワイヤー１０３は、窒化物半導体層の一方の電極上でボールボンディングし第一のボール部１０２を形成した後、隣接する窒化物半導体層の電極とステッチボンディングする。このステッチチボンディング部にはこの上から更にボールボンディングを行い第二のボール部１０４を形成させる。以下、本発明の窒化物半導体発光素子の具体的形成方法について説明するがこれのみに限られないことはいうまでもない。

【００１２】

【実施例】あらかじめ、酸で表面を洗浄させた２インチのサファイア基板（α－アルミナ基板）をＭＯＣＶＤ法を利用する反応装置内に配置させる。真空排気後、１０００℃にまで上げクリーニングを行う。続いて、水素ガスを流しながら大気圧とさせる。次に、成膜温度を５３０℃に下げ反応装置内に、原料ガスとしてＴＭＧ（トリメチルガリウム）、窒素ガスをキャリアガスとして水素ガスと共に流し、厚さ約２００ÅのＧａＮ層を成膜させる。なお、バッファ層は窒化物半導体と基板との格子不整合を緩和させるために設けられるものであり、ＧａＮの他、ＡｌＮ、ＧａＡｌＮなどを好適に利用することができる。また、基板はサファイアの他、スピネル、ルビーなど種々のものを利用することができる。

【００１３】次に、一旦キャリアガスのみとした後に成膜温度を１０５０℃に上げる。成膜温度が一定となった後に原料ガスとしてＴＭＧガス、窒素ガス、ドーパントガスとしてシランガス、キャリアガスとして水素ガスを流しｎ型ＧａＮであるコンタクト層兼クラッド層を成膜させる。なお、窒化物半導体は静電耐圧が他の半導体に比べて低いため、ｎ型コンタクト層をアンドープのＧａＮなどでサンドイッチさせ結晶性と耐電圧を向上させ得るように構成しても良い。

【００１４】次に、活性層としてＧａＮとＩｎＧａＮの多層膜を形成させる。成膜温度を１０５０℃に維持したまま、原料ガスとしてＴＭＧガス、窒素ガス及びキャリアガスとして水素ガスを流してＧａＮ層を形成する。続いて、一旦キャリアガスのみとして、成膜温度を８００℃にまで低下させる。温度が一定となった後に、原料ガスとしてＴＭＧガス、ＴＭＩ（トリメチルインジウム）ガス、窒素ガスを流し、ＩｎＧａＮ層を形成させる。これを３回繰り返した後、最後に上述のアンドープＧａＮと同様の成膜条件にてＧａＮ層を成膜させる。これにより、多重量子井戸構造とされる活性層を成膜させる。発光素子の発光スペクトルは井戸層のバンドギャップに左右されるためＩｎＧａＮの他、ＡｌＧａＩｎＮやＡｌＧａＮなどとすることができる。同様に、Ｓｉなどのｎ型不純物やＭｇなどのｐ型不純物を含有させることもでき

る。

【００１５】活性層成膜後、成膜温度を１０５０℃に保持して、原料ガスをＴＭＡ（トリメチルアルミニウム）ガス、ＴＭＧガス、窒素ガス、ドーパントガスとしてCp_2Mgガス及びキャリアガスとして水素ガスを流し、ｐ型クラッド層となるＡｌＧａＮ層を成膜させる。ｐ型クラッド層は結晶性を向上させためにＧａＮとＡｌＧａＮの超格子構造とさせることもできる。

【００１６】成膜温度を維持したまま、原料ガスをＴＭＧガス、窒素ガス、ドーピングガスとしてCp_2Mgガス及びキャリアガスとして水素ガスを流し、ｐ型コンタクト層となるＧａＮ層を成膜させることができる。

【００１７】こうして成膜させた窒化物半導体ウエハにマスクをかけた後、エッチングにより本発明のごとく、同一成膜基板上に電気的に分離され且つ、ｐｎ接合などを持った複数の島状半導体の窒化物半導体を個々に形成する。ｎ型電極を形成させるｎ型コンタクト層の一部及び窒化物半導体を島状に分離させマスクを除去後、再び電極形成用のマスクを形成させてスパッタリング法によりｐ型透光性電極としてＡｕを成膜させる。

【００１８】ｐ型台座電極としてＮｉ／Ａｕ及びｎ型台座電極としてＷ／Ａｌを、あらかじめ図１のごとく配置できるようにマスクを形成してある。電極形成後、電極表面を残して、SiO_2により保護膜を形成させる。

【００１９】続いて島状に分離した４個の窒化物半導体をひとまとめにして、ダイサー及びスクライバーにより分離した溝に沿ってサファイア基板を切断する。

【００２０】次に、島状の窒化物半導体のｎ型台座電極と、隣り合う島状の窒化物半導体のｐ型台座電極とをワイヤボンディングにより電気的に直列接続させる。より具体的には、あらかじめ金線にボールを形成させた後、島状窒化物半導体のｎ型台座電極或いはｐ型台座電極にボールボンディングさせる。ボールボンディングさせた金線を延ばしつつ、隣り合う島状窒化物半導体のｐ型台座電極或いはｎ型台座電極にステッチボンディングさせ隣り合う島状窒化物半導体を直列接続させる。続いて、成膜基板上に形成された窒化物半導体を固定させるワークを回転させることなく、一度ステッチボンディングさせたワイヤ上に再びボールボンディングを行う。続いて、ステッチボンディング上にボールボンディングさせた金線を延ばしつつ、次に隣り合う隣り合う島状窒化物半導体のｐ型台座電極或いはｎ型台座電極にステッチボンディングさせ隣り合う島状窒化物半導体を電気的に直列接続させる。なお、窒化物半導体の大きさが極めて小さい場合、ボールボンディングをｎ型及びｐ型台座電極に直接押しつけることによって一度に直列接続させることもできる。

【００２１】同一の発光面積を持った単一窒化物半導体発光素子に比べて、同一成膜基板上に形成させた複数の窒化物半導体からなる窒化物半導体発光素子の方が発光効率が高い。そのために直列接続のみに限らず、並列接続或いは直並列接続した本発明の窒化物半導体発光素子とさせることもできる。また、各島状窒化物半導体を集中して配置させることもできるし、図３のごとく、直線上に配置させることもできる。サファイア基板３０５上に形成させた島状の窒化物半導体素子３０１を図３（Ａ）に示すようにワイヤー３０３で直列接続させる場合、各島状窒化物半導体に抵抗を少なく電流を流す必要があることからボワイヤボンディングにより直列接続させることが好ましい。特に、ボールボンディングさせた第一のボール部３０２の他方に形成されるステッチボンディング上には再びボールとして第二のボール部３０４を形成することが好ましい。同様に図３（Ｂ）に示すごとく並列接続させることもできる。

【００２２】島状窒化物半導体の個々の大きさが約１５０μｍ角として上述の窒化物半導体発光素子を形成させる。また、本発明と比較のために発光面積がほぼ同様とさせ、一つの窒化物半導体を積層させた以外は同様にして約６００μｍ角の窒化物半導体発光素子を形成させる。本発明の窒化物半導体発光素子の発光強度を１００として比較したところ、比較のための発光素子は８２％にしかすぎなかった。本発明の窒化物半導体は一つの窒化物半導体に比較して発光効率が優れていることが分かったが、島状窒化物半導体の個々の大きさがそれぞれ約８０μｍより大きく、約３００μｍ未満において、より量産性を満たしつつ効率を向上させることができる。したがって、より発光面積の大きい窒化物半導体を高輝度に発光させるためには、個々に分割させた窒化物半導体を直列に接続させた窒化物半導体とすることが好ましい。なお、図においては、正方形の窒化物半導体素子のみを示したが、サファイア基板の分離しやすさのために菱形やフリップチップ実装を考慮した長方形としたものにも応用できる。

【００２３】

【発明の効果】本発明の窒化物半導体発光素子とすることによって、大面積においても効率よく発光可能な窒化物半導体発光素子とすることができる。また、ウエッジボンダーでのステッチボンドではできなかった方向性なくボンディングすることが可能となる。したがって、異種混合されたパターンでのボンディグ可能化・ボンディグ時間の短縮・電極接合強度の向上を図ることが可能となる。

【図面の簡単な説明】

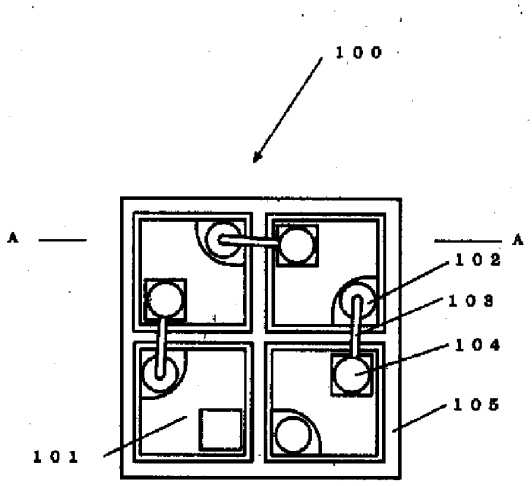
【図１】　本発明の窒化物半導体発光素子の模式的平面図である。

【図２】　図１のＡＡ断面における模式的断面図である。

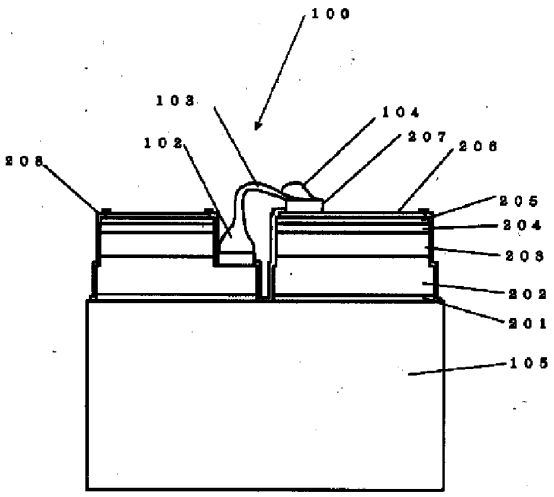
【図３】　図３（Ａ）は直列接続させた本発明の別の窒化物半導体発光素子の模式的平面図であり、図３（Ｂ）は、並列接続させた本発明の窒化物半導体発光素子の模

式的平面図である。
【図４】　本発明と比較のために示す窒化物半導体発光素子の模式的平面図である。
【符号の説明】
１００…本発明の窒化物半導体発光素子
１０１…同一成膜基板上に形成された個々の島状窒化物半導体
１０２…第一のボール部
１０３…ワイヤー
１０４…スッテチボンディグ上に形成された第二のボール部
１０５…サファイア基板
２０１…バッファ層
２０２…ｎ型コンタクト層
２０３…多重量子井戸構造とされる活性層
２０４…ｐ型クラッド層
２０５…ｐ型コンタクト層
２０６…透光性電極
２０７…ｐ型台座電極
２０８…絶縁性保護膜
３００…直列接続された本発明の窒化物半導体発光素子
３０１…同一成膜基板上に形成された個々の島状窒化物半導体
３０２…ワイヤーのボール
３０３…ワイヤー
３０４…スッテチボンディグ上に形成されたボール
３０５…サファイア基板
３０１…並列接続された本発明の窒化物半導体発光素子
４００…本発明と比較のために示された窒化物半導体発光素子
４０１…窒化物半導体層
４０２…ｎ型電極
４０３…透光性電極
４０４…ｐ型電極

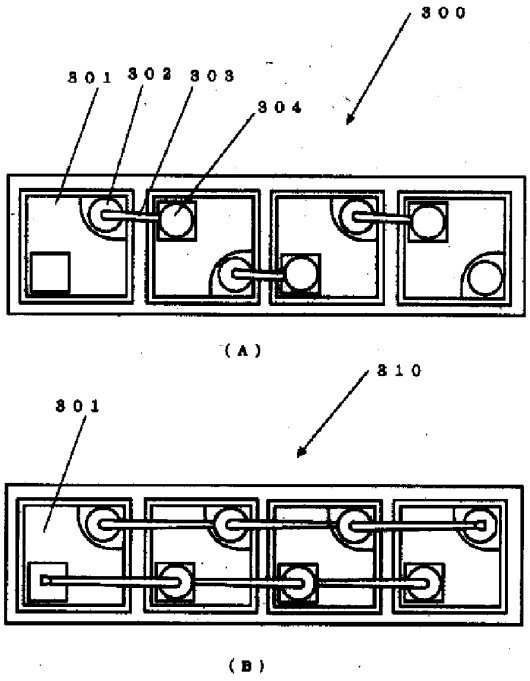
【図１】



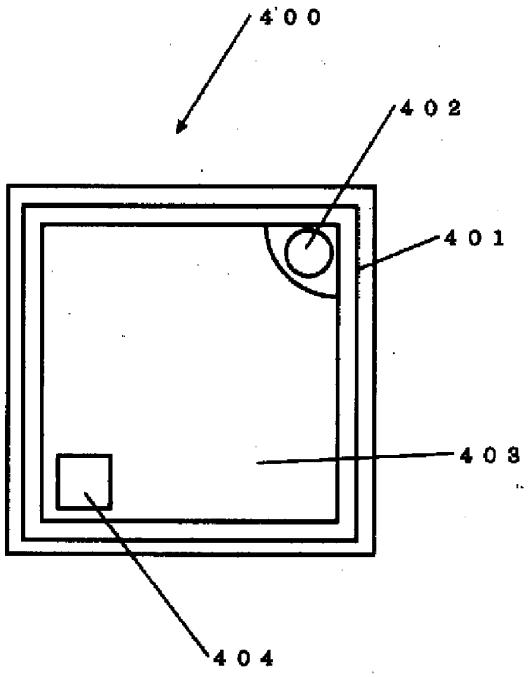
【図２】



【図3】



【図4】



Electronic Acknowledgement Receipt

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International Application Number:	
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First Named Inventor/Applicant Name:	Jong Lam LEE
Customer Number:	58027
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Attorney Docket Number	P2317USD1

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	2	7504772		2009-03-17	Yukimoto et al.	
	3	5940683		1999-08-17	Holm et al.	
	4	6608330		2003-08-19	Yamada	
	5	5652434		1997-07-29	Nakamura et al.	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12613275
	Filing Date	2009-11-05
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	
	Attorney Docket Number	P2317USD1

	1	20030010989		2003-01-16	Yukimoto	
	2	20020109147		2002-08-15	Shirai et al.	
	3	20070114542		2007-05-24	Yamazaki et al.	
	4	20050121679		2005-06-09	Nagahama et al.	
	5	20050082966		2005-04-21	Yamazaki et al.	
	6	20050254243		2005-11-17	Jiang et al.	
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	1	2004-311677	JP		2004-11-04	Matsushita Electric Works Ltd.		☐
	2	2005-142278	JP		2005-06-02	Sharp Corp.		☐

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	Art Unit	2818
	Examiner Name	
	Attorney Docket Number	P2317USD1

	3	2005-117020	JP		2005-04-28	Stanley Electric Co., Ltd.		☐
	4	2003-017740	JP		2003-01-17	Lumileds Lighting US LLC		☐
	5	2001-185755	JP		2001-07-06	Rohm Co., Ltd.		☐
	6	07-153993	JP		1995-06-16	Daido Steel Co., Ltd.		☐
	7	06-244458	JP		1994-09-02	Nichia Chem Ind Ltd.		☐

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	1	Office Action dated February 1, 2010 for co-pending application no. 12/568,630.	☐
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☒ None

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2010-02-24
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PATENT ABSTRACTS OF JAPAN

(11)Publication number : 06-244458
(43)Date of publication of application : 02.09.1994

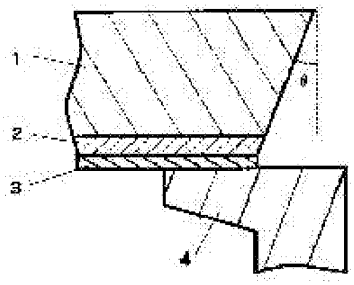
(51)Int.Cl. H01L 33/00

(21)Application number : 05-055074
(22)Date of filing : 19.02.1993

(71)Applicant : NICHIA CHEM IND LTD
(72)Inventor : TANAKA MASANOBU
NAKAMURA SHUJI

(54) BLUE-COLOR-LIGHT EMITTING DIODE

(57)Abstract:
PURPOSE: To improve the light emitting efficiency of a blue-color LED without a reflecting plate such as a cup by effectively utilizing the light emitted from the side surface of a light emitting element utilizing a gallium-nitride-based compound semiconductor, and taking out the light to the side of the observing surface.
CONSTITUTION: A light emitting element comprises at least a light transmitting substrate 1 and a gallium-nitride-based compound semiconductor 2, which is formed on the light transmitting substrate. With the light transmitting substrate 1 of the light emitting element up, the element is mounted on a lead frame 4. The entire light emitting element is sealed with a resin mold 5. In this blue- color-light emitting diode, the side surface of the light emitting element is cut at an acute angle θ downward from the upper surface of the light transmitting substrate.



(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号

特開平6－244458

(43)公開日　平成６年(1994)９月２日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
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	Ｎ	7376－4M		

審査請求　未請求　請求項の数２　ＦＤ　（全　４　頁）

(21)出願番号　特願平5－55074

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(71)出願人　000226057
日亜化学工業株式会社
徳島県阿南市上中町岡491番地100

(72)発明者　田中　政信
徳島県阿南市上中町岡491番地100　日亜化学工業株式会社内

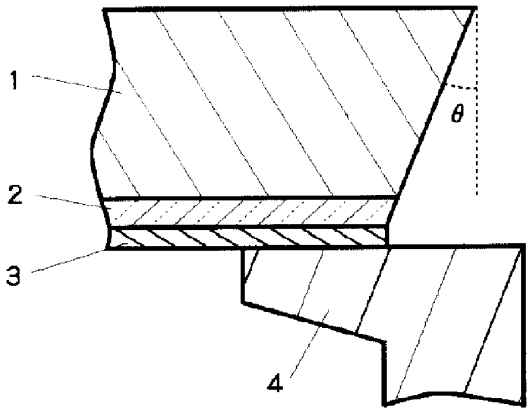
(72)発明者　中村　修二
徳島県阿南市上中町岡491番地100　日亜化学工業株式会社内

(54)【発明の名称】　青色発光ダイオード

(57)【要約】　（修正有）

【目的】　カップ等の反射板を必要とせず、窒化ガリウム系化合物半導体を利用した発光素子の側面から出る光を有効利用して、観測面側に取り出し、青色ＬＥＤの発光効率を向上させる。

【構成】　発光素子が少なくとも透光性基板１と該透光性基板に積層された窒化ガリウム系化合物半導体２とからなり、さらに該発光素子の透光性基板１を上面としてリードフレーム４上に載置し、発光素子全体を樹脂モールド５で封止してなる青色発光ダイオードにおいて、前記発光素子の側面が、透光性基板上面から鉛直方向に向かって、鋭角θで切断されていることを特徴とする。



【特許請求の範囲】
【請求項１】　発光素子が少なくとも透光性基板と該透光性基板に積層された窒化ガリウム系化合物半導体とからなり、さらに該発光素子の透光性基板を上面としてリードフレーム上に載置し、発光素子全体を樹脂モールドで封止してなる青色発光ダイオードにおいて、
前記発光素子の側面が、透光性基板上面の鉛直方向より、鋭角θで切断されていることを特徴とする青色発光ダイオード。
【請求項２】　前記鋭角θは、前記透光性基板の屈折率をｎ1、前記樹脂モールドの屈折率をｎ2とすると、$\theta \geqq \sin^{-1}(n2/n1)$の関係にあることを特徴とする請求項１に記載の青色発光ダイオード。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、透光性基板上に窒化ガリウム系化合物半導体が積層された発光素子を有する青色発光ダイオード（以下、青色ＬＥＤという。）に係り、特に該発光素子の細部の構造に関する。
【０００２】
【従来の技術】一般に、青色ＬＥＤの発光素子の材料として、ＧａＮ、ＩｎＧａＮ、ＧａＡｌＮ、ＩｎＡｌＧａＮ等の窒化ガリウム系化合物半導体が知られている。これら窒化ガリウム系化合物半導体を用いた発光素子を有する従来の青色ＬＥＤの構造を図２に示す。１は透光性基板、２は透光性基板１上に積層された窒化ガリウム系化合物半導体（以下、本明細書においては、１と２とを合わせて発光素子という。）３は窒化ガリウム系化合物半導体２上の適切な位置に設けられた電極、４は発光素子を載置するリードフレーム、５は発光素子全体を封止し、窒化ガリウム系化合物半導体２からの発光を集光する樹脂モールドである。透光性基板１の材料にはサファイア、酸化亜鉛、酸化マグネシウム等の酸化物系単結晶を使用することができ、一般的にはサファイアが用いられている。また樹脂モールド５には、エポキシ樹脂、ユリア樹脂等、耐候性に優れた透明樹脂が用いられる。この図に示すように、従来の青色ＬＥＤはそのほとんどが、発光素子の端面が垂直になるようにチップ状にカットされ、透光性基板１側が上面、即ち発光観測面となるようにしてリードフレームに載置された構造を有している。
【０００３】
【発明が解決しようとする課題】この構造の発光素子において、例えば透光性基板１をサファイアとした場合、サファイア基板１の厚さは通常数百μｍある。これに対し、窒化ガリウム系化合物半導体の厚さはせいぜい数μｍにしか過ぎず、窒化ガリウム系化合物半導体より放射される全青色発光のうち、サファイア基板１の側面に達する光は、全体の約１０～４０％である。しかも、封止樹脂をエポキシ樹脂とした場合、サファイアの屈折率を約３とし、エポキシの屈折率を約１．５とすると、サファイアとエポキシ樹脂との境界での臨界角は約３０°となり、側面に入射する３０°以下の光は、全てサファイア基板の側面から出て行ってしまい、有効利用されていない。
【０００４】ところで、リードフレームの形状をカップ状として、そのカップの底に発光素子を載置して、側面から出ていく光を、カップ側面で上部に反射させる方法もあるが、リードフレームをカップ形状にすると、透光性基板を上にして電極を下にするような構造の窒化ガリウム系化合物半導体発光素子、つまり透光性基板を利用した発光素子では、アッセンブリが生産技術上不可能である。そのため、従来の青色ＬＥＤは、そのほとんどが図２のような構造であり、この構造のＬＥＤはチップ側面より出ていく光を有効利用できず、高い順方向電圧のわりに、発光効率が低く、十分な輝度が得られないという問題があった。
【０００５】したがって本発明はこのような事情を鑑みて成されたものであり、カップ等の反射板を必要とせず、窒化ガリウム系化合物半導体を利用した発光素子の側面から出る光を有効利用して、観測面側に取り出し、青色ＬＥＤの発光効率を向上させることを目的とする。
【０００６】
【課題を解決するための手段】本発明の青色ＬＥＤは、発光素子が少なくとも透光性基板と該透光性基板に積層された窒化ガリウム系化合物半導体とからなり、さらに該発光素子の透光性基板を上面としてリードフレーム上に載置し、発光素子全体を樹脂モールドで封止してなる青色発光ダイオードにおいて、前記発光素子の側面が、透光性基板上面の鉛直方向より、鋭角θで切断されていることを特徴とするものである。
【０００７】鋭角θの角度は特に限定するものではないが、透光性基板の屈折率、樹脂モールドの屈折率によって適宜変更することができる。窒化ガリウム系化合物半導体の発光を全て透光性基板側（発光観測面側）に全反射させるためには、鋭角θは、透光性基板の屈折率をｎ1、前記樹脂モールドの屈折率をｎ2とした場合、$\sin^{-1}(n2/n1)$以上の角度、即ち臨界角以上の角度で切断されていることが好ましい。なお、この式により、全ての青色発光を発光素子側面で全反射させる場合、樹脂モールドの材料の屈折率が基板の屈折率よりも小さいものを選択することはいうまでもない。
【０００８】また、発光素子の側面を斜めにカットするには、例えばダイシングを用いることができ、刃先が所望の角度に調整されているブレードを使用することによって切断可能である。
【０００９】
【作用】図４は、本発明の一実施例に係る青色ＬＥＤにおいて、側面が鋭角θで切断された発光素子の構造を示す図である。また図３は、側面が垂直に切断された従来

の発光素子の構造を示す図である。なおこれらの図は電極、リードフレームを省略して示している。図４に示すように、発光素子の側面を、透光性基板１の上面から、鋭角θで切断することにより、窒化ガリウム系化合物半導体より発する青色発光、特に発光素子側面近傍の青色発光を、透光性基板１で反射させて発光観測面に取り出し、有効利用することが可能となる。一方、前にも説明したように、図３に示す従来の発光素子は、透光性基板１内で全反射したり、発光素子の側面から出て行ってしまう光が圧倒的に多い。なお、この図４はθを臨界角以上としていないため、一部側面から出ていく光もあるが、θを前述の式に基づいて臨界角以上で切断することにより、全て観測面側に反射させることができるのは当然である。

【００１０】このように、発光素子の側面を鋭角に切断することにより、青色発光を多く観測面に反射させることができるため、青色発光ダイオードの発光出力を向上させることができる。また、窒化ガリウム系化合物半導体を有する発光素子は、他のＧａＡｓ、ＧａＰ、ＡｌＩｎＧａＰ等の材料を用いた発光素子と異なり、材料自体にへき開性を有していないため、斜めに切断しやすいという利点を有している。このため、窒化ガリウム系化合物半導体の発光素子の側面を斜めに切断して、その側面で青色発光を反射させることは非常に重要である。

【００１１】

【実施例】予めサファイア基板の上にｎ型ＧａＮとｐ型ＧａＮとを順に積層した２インチφのウエハーを用意し、ｐ型ＧａＮ層の一部をエッチングして、ｎ型ＧａＮ層を一部露出させる。次に、露出させたｎ型ＧａＮ層と、ｐ型ＧａＮとに所定の形状で電極を蒸着した後、サファイア基板に粘着テープを張り付ける。

【００１２】一方、ウエハーを斜めにカットするため、図５に示すように刃先の中心線に向かってそれぞれ両側に３０°の傾斜を設けたブレードを用意してダイシングソーにセットする。次に、前述のウエハーをテーブルに貼付し、ダイシングでｐ型ＧａＮ層側からＸ軸をカットした後、テーブルを９０°回転させ、今度はＹ軸をカットする。

【００１３】最後にウエハーをテーブルから剥し取り、チップ状に分離した後、チップをサファイア基板面が発光観測面になるようにして、リードフレームに取り付け、電極とリードフレームとを電気的に接続した後、エポキシ樹脂でレンズ状にモールドすることにより、本発明の青色ＬＥＤを得る。

【００１４】このようにして得た青色ＬＥＤは、順方向電圧５Ｖで、発光出力２０μＷを示した。一方、側面を垂直にカットしたチップよりなる従来の青色ＬＥＤは発光出力は１０μＷとほぼ半分しかなかった。

【００１５】

【発明の効果】以上説明したように、本発明の青色ＬＥＤはその発光素子の側面を斜めにカットしているために、窒化ガリウム系化合物半導体の発光を、その側面で反射させて透光性基板から有効に取り出すことができる。しかも従来のようにカップ状のリードフレームも必要とせず、生産性にも非常に優れている。

【図面の簡単な説明】

【図１】　本発明の青色ＬＥＤに係る発光素子の側面の構造を一部拡大して示す断面図。

【図２】　従来の青色ＬＥＤの構造を示す断面図。

【図３】　従来の発光素子の構造を示す断面図。

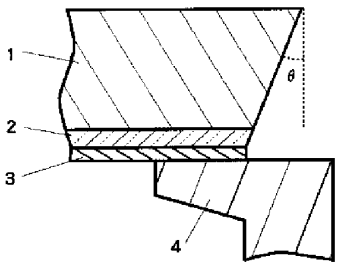
【図４】　本発明の一実施例に係る発光素子の構造を示す断面図。

【図５】　ダイシングソーのブレードの刃先角を示す断面図。

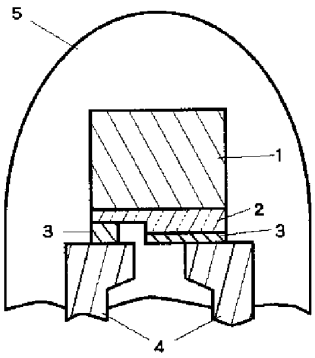
【符号の説明】

１・・・・・・透光性基板
２・・・・・・窒化ガリウム系化合物半導体
３・・・・・・電極
４・・・・・・リードフレーム
５・・・・・・樹脂モールド

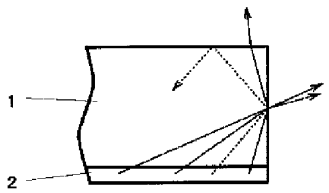
【図１】



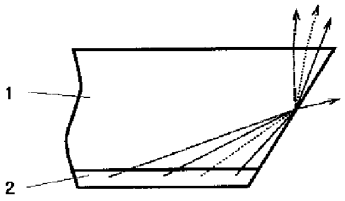
【図２】



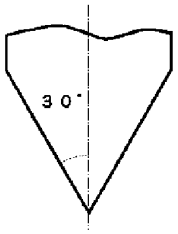
【図３】



【図４】



【図５】



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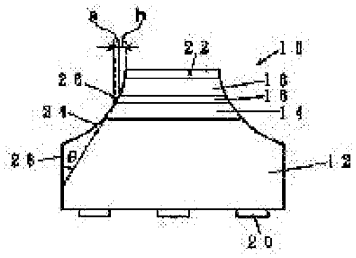
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(71)Applicant : DAIDO STEEL CO LTD
(72)Inventor : IMAIZUMI MITSURU
KATO TOSHIHIRO
SAKA TAKASHI
HIROYA MASUMI
SONE TOSHINORI
MIZUNO YOSHIYUKI

(54) LIGHT-EMITTING DIODE

(57)Abstract:
PURPOSE: To obtain high light-emitting efficiency by forming an inwardly curved slope spreading from a second clad layer toward a substrate and exposing the periphery of an active layer to the slant face.
CONSTITUTION: A second clad layer 18 is smaller in area than a substrate 12, and a slope 24 including the edge of a first clad layer 14 on the substrate 12 and the upper edge of the second clad layer 18 is inwardly curved. The slope exposes an end face 26 of an active layer 16 and the periphery including the end face 26 forms a prescribed angle θ to an end face 28 of the substrate 12. Thereby, current density becomes high so as to obtain higher light-emitting efficiency.



(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号

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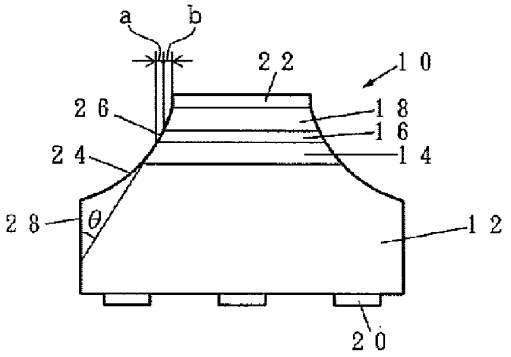
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(71)出願人　000003713
大同特殊鋼株式会社
愛知県名古屋市中区錦一丁目11番18号
(72)発明者　今泉　充
愛知県一宮市中町二丁目９番38－302号
(72)発明者　加藤　俊宏
愛知県春日井市中央台８丁目７番地の４
(72)発明者　坂　貴
愛知県名古屋市緑区鳴海町字片平20番地の37
(72)発明者　廣谷　真澄
愛知県東海市加木屋町南鹿持１－６
(74)代理人　弁理士　池田　治幸　（外２名）

最終頁に続く

(54)【発明の名称】　発光ダイオード

(57)【要約】
【目的】　高い発光効率が得られる発光ダイオードを提供する。
【構成】　ＬＥＤ（発光ダイオード）１０は、全体が略角柱状を成しているが、基板１２側よりも第２クラッド層１８側の方の面積が小さくされており、基板１２の第１クラッド層１４側の端部と、第２クラッド層１８上面の端部とを結ぶ側面２４は湾曲した斜面とされている。そのため、第１クラッド層１４、活性層１６および第２クラッド層１８は、基板１２側から先細りとなるように積層されて略四角錐台状を成し、活性層１６の端面２６を含む周縁は、基板１２の端面２８に対して所定の角θを成す斜面とされている。



【特許請求の範囲】
【請求項１】　基板上に第１クラッド層、活性層および第２クラッド層が順次積層され、該基板と該第２クラッド層との間に動作電流が通電されることによって該活性層内で発生した光を、該第２クラッド層側から取り出す面発光型発光ダイオードであって、
前記第２クラッド層から前記基板に向かうに従って外周側に向かう斜面が形成され、該斜面に前記活性層の周縁が露出させられていることを特徴とする発光ダイオード。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、発光ダイオードの発光効率を高める技術に関する。
【０００２】
【従来の技術】基板上に第１クラッド層、活性層および第２クラッド層が順次積層され、その基板と第２クラッド層との間に動作電流が通電されることによって上記活性層内で発生した光を、その第２クラッド層側から取り出す面発光型発光ダイオード（以下ＬＥＤという）が知られている。一般に、このような構造のＬＥＤでは、上記活性層内で発生した光が、光取り出し面である第２クラッド層表面に到達するまでに減衰したり反射され、或いは第２クラッド層表面以外の所からも放射されると共に、基板側に向かって放射され、その底面で反射されて側面に向かう光は、その側面への入射角が比較的大きくなるため反射されて内部で吸収されるため、第２クラッド層側から取り出されるのは発生した光の一部のみとなって、高い発光効率が得られない。そこで、発光効率を高めるために、例えばＬＥＤのアッセンブリに際して、開口部側に面する凹面内にＬＥＤを固定し、その端面から放射された光をその凹面で反射させ、第２クラッド層側から取り出される光と同じ方向に取り出すこと等が行われる。
【０００３】
【発明が解決すべき課題】しかしながら、上記のようなアッセンブリによっても発光効率の改善は未だ不充分であった。上記アッセンブリ構造では、ＬＥＤの端面から放射された光が取り出し可能となるのみであり、また、テーパ面での反射効率を十分に高くするには高精度の加工を要して多大なコスト増となるため、反射効率も低いものであったのである。
【０００４】本発明は、以上の事情を背景として為されたものであって、その目的は、高い発光効率が得られる発光ダイオードを提供することにある。
【０００５】
【課題を解決するための手段】斯かる目的を達成するために、本発明の要旨とするところは、基板上に第１クラッド層、活性層および第２クラッド層が順次積層され、その基板と第２クラッド層との間に動作電流が通電されることによって上記活性層内で発生した光を、その第２クラッド層側から取り出す面発光型発光ダイオードであって、前記第２クラッド層から前記基板に向かうに従って外周側に向かう斜面が形成され、該斜面に前記活性層の周縁が露出させられていることにある。
【０００６】
【作用および発明の効果】このようにすれば、第２クラッド層と基板との間に斜面が形成されて、活性層の周縁がその斜面に露出させられると共に、第２クラッド層は基板よりも小さい面積とされるので、その斜面は第２クラッド層側から取り出される光と同じ方向、すなわち光の取り出し方向に向かわせられる。このため、活性層の端面側から放射された光の一部は、直接光の取り出し方向に放射されることになる。また、斜面が光の取り出し方向に向かわせられているため、活性層は第２クラッド層よりも大きな面積を有することになり、第２クラッド層の表面よりも外側に位置する部分で発生して、活性層から第２クラッド層側に向かう光は、第２クラッド層表面に到達する前に取り出される。そのため、この光は、ＬＥＤ内で殆ど減衰或いは反射されることなく取り出される。また、活性層から基板側へ放射され、基板底面で反射されて側面に向かう光は、その側面が斜面とされているため反射光の入射角が小さくなり、その斜面を通って外部に取り出される。したがって、ＬＥＤの側面から放射される光が比較的多く取り出されると共に、発生した光の減衰や反射が減じられ、また、基板側に向かう光も効率良く取り出されて、高い発光効率が得られる。更に、上記のように斜面が形成された結果、活性層が基板よりも小さい面積とされているため、その面積が等しくされている場合に比較して電流密度が高くなり、一層高い発光効率が得られる。
【０００７】
【実施例】図１は、本発明の一実施例であるＬＥＤ（発光ダイオード）１０の構成を示す図である。このＬＥＤ１０は、基板１２上に、例えば有機金属化学気相成長（ＭＯＣＶＤ：Metal Organic Chemical Vapor Deposition ）法や分子線エピタキシー（ＭＢＥ：Molecular Beam Epitaxy）法、或いは気相エピタキシー（ＶＰＥ：Vapor Phase Epitaxy ）法等によって、第１クラッド層１４、活性層１６および第２クラッド層１８が順次結晶成長させられた後、基板１２の下面および第２クラッド層１８の上面に、下部電極２０および上部電極２２がそれぞれ蒸着されて構成されている。
【０００８】上記基板１２は例えば３５０μｍ程度の厚さのｎ－$Al_{0.4}Ga_{0.6}As$単結晶から成る化合物半導体、第１クラッド層１４は例えば４μｍ程度の厚さを備えた、上記基板と同じｎ－$Al_{0.4}Ga_{0.6}As$単結晶から成る化合物半導体、活性層１６は例えば１μｍ程度の厚さのｐ－ＧａＡｓ単結晶から成る化合物半導体、第２クラッド層１８は例えば４μｍ程度の厚さのｐ－Ａ

$l_{0.4}$ $Ga_{0.6}$ Ａｓ単結晶から成る化合物半導体である。また、下部電極２０は、基板１２側から順にＡｕ－Ｇｅ合金、ＮｉおよびＡｕが積層形成されており、上部電極２２は第２クラッド層１８側にＡｕ－Ｚｎ合金が、その上にＡｕが積層形成されている。これらの下部電極２０および上部電極２２はそれぞれオーミック電極である。

【０００９】上記ＬＥＤ１０は、全体が略角柱状を成しているが、基板１２側よりも第２クラッド層１８側の方の面積が小さくされており、基板１２の第１クラッド層１４側の端部と、第２クラッド層１８上面の端部とを結ぶ側面２４は、図に示すように湾曲した斜面とされている。すなわち、第２クラッド層１８から基盤１２に向かうに従って外周側に向かう斜面が形成されている。そのため、第１クラッド層１４、活性層１６および第２クラッド層１８は、基板１２側から先細りとなるように積層されて略四角錐台状を成し、活性層１６の端面２６を含む周縁は、基板１２の端面２８に対して所定の角θ（例えば６０°程度）を成す斜面とされている。なお、図において基板１２、各層１４，１６，１８および電極２０，２２等の大きさは、必ずしも正確な比率で示されていない。

【００１０】以上のように構成されたＬＥＤ１０は、下部電極２０と上部電極２２とに動作電圧が印加され、第１クラッド層１４および第２クラッド層１８間に動作電流が通電されることによって、活性層１６内で光が発生し、第２クラッド層１８の上面側からその光が取り出される。

【００１１】ここで、本実施例においては、ＬＥＤ１０の上記側面２４が斜面を成しているため、活性層１６の端部は、その厚さに $\tan\theta$ を乗じた大きさ（幅ａ）で、光取り出し方向である図の上方向に向けられている。そのため、活性層１６の端面２６から放射された光の一部は、直接光の取り出し方向に放射されることになる。また、第２クラッド層１８の上面の面積は、活性層１６の上面の面積よりも小さくされており、図の幅ｂ内で発生した光は第２クラッド層１８の上面に達する以前に第２クラッド層１８の端面から取り出されることになる。このため、この光はＬＥＤ１０内で殆ど減衰或いは反射されることなく取り出される。また、活性層１６から基板１２側へ放射され、基板１２底面で反射されて側面２４に向かう光は、その側面２４が斜面とされているため入射角が小さくなり、従来入射角が大き過ぎるために反射されて内部で吸収されていた光が、その斜面を通って外部に取り出される。したがって、側面２４から放射される光が比較的多く取り出されると共に、発生した光の減衰や反射が減じられ、また、基板１２側に向かう光も効率良く取り出されて、高い発光効率が得られる。更に、活性層１６が基板１２よりも小さい面積とされているため、その面積が等しくされている場合に比較して電流密度が高くなり、一層高い発光効率が得られる。

【００１２】上記ＬＥＤ１０は、例えば図２の（ａ）～（ｈ）の工程に従って製造される。（ａ）の工程において、多数のＬＥＤ１０を製造するための基板１２上に第１クラッド層１４、活性層１６および第２クラッド層１８を順次結晶成長させて、エピタキシャル層３０を作製する。なお、図２においては、エピタキシャル層３０の各層の境界を省略している。次いで（ｂ）の工程において、エピタキシャル層３０上にフォトリソグラフィによって所定のパターンの上部電極２２を形成し、（ｃ）の工程において、その上にフォトレジスト膜３２を形成して、フォトリソグラフィによって、ＬＥＤ１０となる個々の素子３４毎にパターニングを行う。このとき、（ｃ）に示されるように、上部電極２２はフォトレジスト膜３２に覆われた状態にされている。次いで（ｄ）の工程において、例えば燐酸および過酸化水素水を混合したエッチング液によって、エピタキシャル層３０の上面側からエッチングを行う。このエッチング液はフォトレジスト膜３２を溶解せず、エピタキシャル層３０および基板１２のみを溶解するものが好適に用いられる。このとき、エピタキシャル層３０の各層および基板１２の溶解性が略等しいため、その表面上の点Ｐを中心とした略円弧上の凹部３６が形成されるように溶解され、エッチング液の組成、濃度、処理温度および処理時間を適宜設定することにより、エピタキシャル層３０の上面が上部電極２２よりもやや小さくされる。次いで、（ｅ）の工程において、フォトレジスト膜３２を除去し、（ｆ）の工程において、個々の素子３４毎にダイシングによって分離する。このとき、前記のエッチング処理によってエピタキシャル層３０の上面からはみ出した上部電極２２の周縁部が水流或いは超音波によって除去される。次いで（ｇ）の工程において下部電極２０を形成して、図１に示されるＬＥＤ１０が製造される。このＬＥＤ１０は、（ｈ）の工程において、テーパ状の内壁面３８を備えたケース４０の底面に、下部電極２０が図示しないリードに導通がとられるように固定されると共に、上部電極２２にリード４２がボンディングされ、図示しない工程において樹脂モールド内に封入して用いられる。

【００１３】上記の製造工程においては、上記凹部３６がダイシングの切り代の幅よりも極めて大きくされていると共に、凹部３６は基板１２の上部の一部までの範囲で形成されているため、（ｆ）の工程で素子３４がダイシングによって分離されると、基板１２の下部の端面はその底面と直角になるが、エピタキシャル層３０および基板１２の一部の端面はやや湾曲した斜面を成す。したがって、エピタキシャル層３０および基板１２の一部が略四角錐台状とされた、すなわち、図１に示した、基板１２と第２クラッド層１８の上面とを結ぶ側面２４が斜面とされたＬＥＤ１０が容易に得られるのである。

【００１４】なお、本実施例では、凹部３６が形成され

た後にダイシングが行われるため、ダイシングの際に活性層１６にカッタが触れない。したがって、活性層１６等にダイシングに起因する欠けが発生せず、電流のリークが発生し難い利点がある。また、テーパ状の内壁面３８を備えたケース４０内にＬＥＤ１０が固定されているため、活性層１６の側面から第２クラッド層１８の表面と平行な方向に放射される光も、その内壁面３８によって反射されて光の取り出し方向に向かわされ、一層高い発光効率が得られる。

【００１５】図3は、前述の製造工程の（ｄ）の工程において、エッチング時間を変えた場合の光出力すなわち発光効率を表したグラフである。前述の工程においては、例えば４０乃至５０分間処理することによって、エッチング処理をしないＬＥＤに比較して約１．８倍程度の高い光出力のＬＥＤ１０が得られている。なお、最適なエッチング時間は、エッチング液の種類や濃度および処理時間や処理温度等の条件によって変動するが、短か過ぎる場合にはエピタキシャル層３０の面積が十分に小さくならないため電流密度が上がらず、また、側面の傾斜部が形成されないために、高い光出力が得られない。また、必要以上に長時間のエッチング処理をしても、電流密度は高くなるものの活性層１６すなわち発光面積が小さくなるため、ある一定値以上の光出力は得られないのである。

【００１６】図4は、上記ＬＥＤ１０において、動作電流を５０ｍＡとしたときの電流密度と光出力の関係を表したグラフである。このグラフにおいては、従来用いられていた電流密度５４ｍＡ／ｃｍ^2 程度のＬＥＤの光出力を１として、相対的な光出力を示している。図より明らかなように電流密度が高くなると相対光出力が高くなる。本実施例のＬＥＤ１０においては、前述のような構成とされた結果、電流密度が約１２８ｍＡ／ｃｍ^2 程度と高くなり、上述のように従来の１．８倍程度の高い光出力が得られるのである。なお、本図は、前述の構造のＬＥＤ１０による測定結果であるため、前述のように側面２４が斜面とされたことによる効果が含まれた光出力であり、必ずしも電流密度と相対光出力との厳密な関係を表すものではない。

【００１７】図5は、他の製造方法によったＬＥＤ４４の例である。本実施例においては、基板１２と第２クラッド層１８の上面とを結ぶ側面４６は、湾曲しない真直な斜面とされている。このような構造としても、前述の実施例と同様に、活性層１６の端面２６が斜面とされてその端面２６から放出される光が光の取り出し方向に向かわされ、また、側面４６が斜面とされて活性層１６の端部側で発生した光の減衰や反射が低減させられ、また、基板１２側へ放射されてその底面で反射された光が斜面から取り出され、更に、活性層１６が基板１２よりも小さい面積とされて電流密度が高くされているため、高い発光効率が得られるのである。更に、本実施例においては、側面４６が湾曲していないため、第２クラッド層１８上面と基板１２底面との面積比を等しくした場合には、前述のＬＥＤ１０よりも幅ａが大きくなり、一層高い発光効率が得られる。このＬＥＤ４４は、例えば、前述の図２の工程において、このようなプロファイルが得られるエッチング液を使用するか、或いはエッチング処理に代えて幅広且つ先端がテーパ状とされたダイヤモンドカッタ等で溝切り加工をし、その後図２（ｆ）の工程と同様にダイシングを行うことによって得られる。

【００１８】なお、前述のＬＥＤ１０およびＬＥＤ４４においては、第２クラッド層１８上に直接上部電極２２を形成したが、例えば、図6に示すように、第２クラッド層１８の上に第２クラッド層１８とは導電型が異なる電流ブロック層４８を設け、その上に上部電極２２を形成して、ＬＥＤ５０のような構造としても良い。前述の実施例においては、上部電極２２は例えば図７に示されるように形成されており、リード４２がボンディングされる部分すなわち上部電極２２の中央部５２は、通電されて光が発生しても上部電極２２に遮蔽されてその光が取り出し得ない。これに対して、ＬＥＤ５０では、中央部５２は電流ブロック層４８が存在するために通電され得ず、発光させられない。すなわち、上部電極２２に遮蔽されないで光が取り出される部分のみが発光させられるため、発生した光の取り出し効率が一層高くなり、高い光出力が得られる。なお、上記電流ブロック層４８は、例えばフォトリソグラフィ等によって任意の形状に形成されるものである。

【００１９】以上、本発明の一実施例を図面を参照して詳細に説明したが、本発明は更に別の態様でも実施される。

【００２０】例えば、前述の実施例においては、ＧａＡｓ／Ａｌ$_x$ＧａＡｓダブルヘテロ構造の面発光型ＬＥＤ１０等について説明したが、そのＡｌ$_x$とＧａとの組成比は適宜設定されると共に、ＧａＰ，ＩｎＰ，ＩｎＧａＡｓＰ等から成るダブルヘテロ構造のＬＥＤや、単なるｐｎ接合から成るＬＥＤにも本発明は同様に適用され得る。また、基板１２には、例えばＧａＡｓ等の他の半導体が用いられても良い。

【００２１】また、前述の実施例においては、基板１２側にｎ型半導体が、第２クラッド層１８側にｐ型半導体が用いられ、上部電極２２から下部電極２０に向かって動作電流が流れるようにされていたが、ｐ型，ｎ型を反対にして動作電流の流れる方向を反対にしても良い。

【００２２】例えば、前述の実施例においては、活性層１６の端面２６の傾斜の角度θは６０°程度とされていたが、この角度θは、１０～８０°の範囲の値を取り得るものである。

【００２３】また、前述の実施例において第１クラッド層１４が比較的厚く（例えば５０μｍ程度）されている場合は、第１クラッド層１４までが傾斜させられていて

も良い。

【００２４】また、前述の実施例においては、ＬＥＤ１０，４４，５０は全体が略角柱状に形成され、エピタキシャル層３０（すなわち第１クラッド層１４乃至第２クラッド層１８）および基板１２の一部は四角錐台状に形成されていたが、ＬＥＤ１０等の全体の形状は例えば多角柱状とされていても良く、エピタキシャル層３０および基板１２の一部は、三角錐台を含む多角錐台状或いは円錐台状とされていても良い。本発明においては、活性層１６が基板１２よりも小さい面積とされ、その端面２６を含む周縁が斜面に露出させられていれば、その効果が得られるのである。なお、ＬＥＤ１０等の形状は、例えば、図２の工程において上部電極２２およびフォトレジスト膜３２を多角形或いは円形等に形成してエッチング処理を行うことで容易に変更できる。

【００２５】その他、一々例示はしないが、本発明はその主旨を逸脱しない範囲で種々変更を加え得るものである。

【図面の簡単な説明】

【図１】本発明の一実施例である発光ダイオードの構成を示す図であり、図２の製造方法によって得られたものである。

【図２】本発明の一実施例である発光ダイオードの製造方法を示す図である。

【図３】図２の工程におけるエッチングの時間と光出力との関係を示すグラフである。

【図４】図２の工程において得られた発光ダイオードの電流密度と光出力との関係を示すグラフである。

【図５】本発明の他の実施例を示す図である。

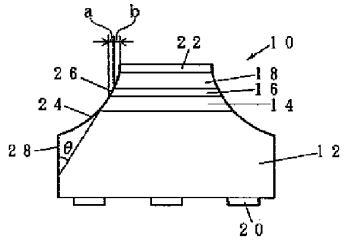
【図６】本発明の更に他の実施例を示す図である。

【図７】図１の発光ダイオードの電極の構成を示す図である。

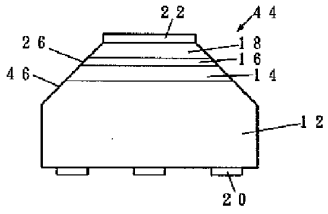
【符号の説明】

１０：ＬＥＤ（発光ダイオード）
１２：基板
１４：第１クラッド層
１６：活性層
１８：第２クラッド層
２２：上部電極
２４：側面
２６：活性層の端面（周縁）

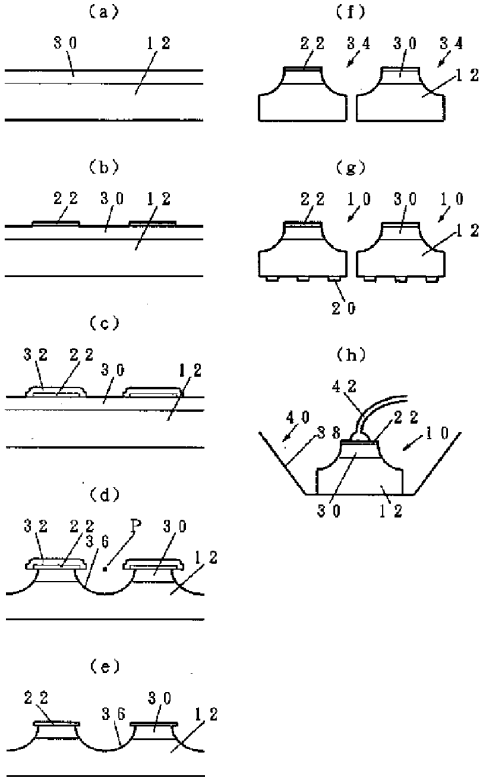
【図１】



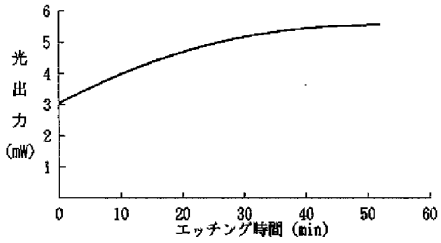
【図５】



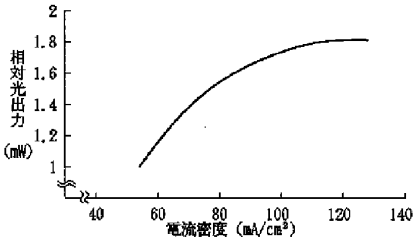
【図２】



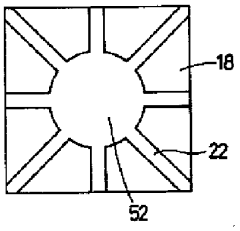
【図３】



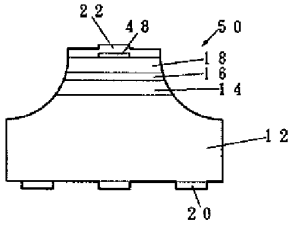
【図４】



【図７】



【図６】



フロントページの続き

(72)発明者　曽根　豪紀
愛知県東海市加木屋町南鹿持18

(72)発明者　水野　義之
愛知県名古屋市名東区高社二丁目194番地

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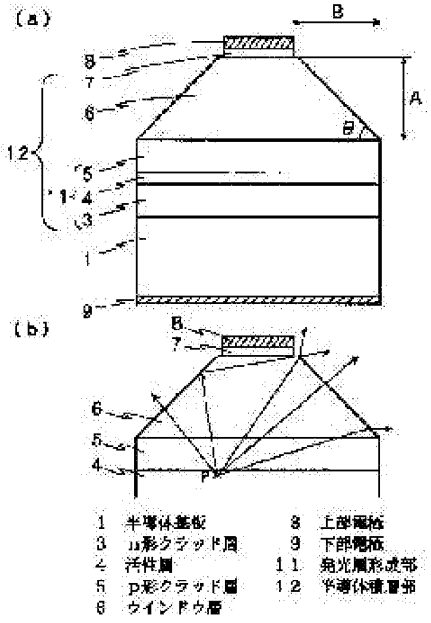
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(71)Applicant : ROHM CO LTD
(72)Inventor : HOSOMI CHUKEI
MATSUMOTO YUKIO

(54) SEMICONDUCTOR LIGHT EMITTING ELEMENT

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a semiconductor light emitting element which has a structure permitting lights emitted from a light emitting layer to be taken out possibly much outside a chip to improve the outside differential quantum efficiency.
SOLUTION: A semiconductor laminate 12 having a light emitting layer forming part 11 having an active layer 4 sandwiched between at least an n-type layer 3 and a p-type layer 5 is provided on a semiconductor substrate 1, an upper (p-side) electrode 8 is provided on the front surface of the semiconductor laminate 12, a lower (n-side) electrode 9 is provided on the back surface of the semiconductor substrate 1, and a slope narrower at the upper electrode 8 and broader at the active layer 4 is formed on the side of an upper layer of the semiconductor laminate 12 than its active layer 4.



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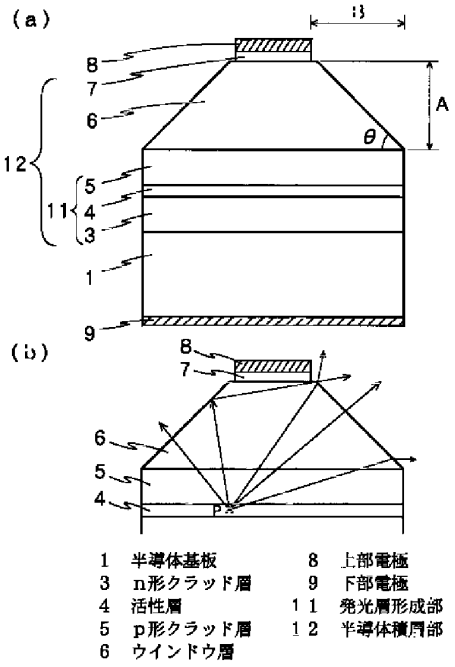
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(71)出願人　000116024
ローム株式会社
京都府京都市右京区西院溝崎町21番地
(72)発明者　細見　忠敬
京都市右京区西院溝崎町21番地　ローム株式会社内
(72)発明者　松本　幸生
京都市右京区西院溝崎町21番地　ローム株式会社内
(74)代理人　100098464
弁理士　河村　洌

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(54)【発明の名称】　半導体発光素子

(57)【要約】
【課題】　発光層で発光した光をチップの外側にできるだけ取り出せる構造とし、外部微分量子効率を向上させることができる半導体発光素子を提供する。
【解決手段】　半導体基板１の上に、少なくともｎ形層３およびｐ形層５により活性層４を挟持する発光層形成部１１を有する半導体積層部１２が設けられている。また、半導体積層部１２の表面側に上部電極（ｐ側電極）８が設けられ、半導体基板１の裏面側に下部電極（ｎ側電極）９が設けられている。そして、半導体積層部１２の活性層４より上層部に上部電極８側の幅が狭く、活性層４側で幅が広くなるように側面に傾斜面が形成されている。



【特許請求の範囲】
【請求項１】　半導体基板と、該半導体基板の上に設けられ、少なくともｎ形層およびｐ形層により活性層を挟持する発光層形成部を有する半導体積層部と、該半導体積層部の表面側に設けられる上部電極と、前記半導体基板の裏面側に設けられる下部電極とからなり、前記半導体積層部の前記活性層より上層部に前記上部電極側の幅が狭く、前記活性層側で幅が広くなるように側面に傾斜面が形成されてなる半導体発光素子。
【請求項２】　前記傾斜面が、外側が凸面となる傾斜面である請求項１記載の半導体発光素子。
【請求項３】　前記半導体積層部の表面側が、ＡｌＧａＡｓ系化合物半導体層からなり、表面側ほどＡｌの混晶比が小さくなるように組成が変化する層である請求項１または２記載の半導体発光素子。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、半導体層が積層されて発光層を形成する発光層形成部の表面側に光を取り出す構造の半導体発光素子に関する。さらに詳しくは、側面方向に光を取り出しやすくし、全体として発光する光の外部への取出し効率（外部微分量子効率）を向上させ得る構造の半導体発光素子に関する。
【０００２】
【従来の技術】従来の可視光半導体発光素子は、たとえば図５に示されるような構造になっている。すなわち、図５において、ｎ形ＧａＡｓからなる半導体基板２１上に、たとえばｎ形のＩｎＧａＡｌＰ系の半導体材料からなるｎ形クラッド層２２、クラッド層よりバンドギャップエネルギーが小さくなる組成のＩｎＧａＡｌＰ系の半導体材料からなる活性層２３、ｎ形クラッド層と同じ組成でｐ形のＩｎＧａＡｌＰ系の半導体材料からなるｐ形クラッド層２４がそれぞれエピタキシャル成長され、ダブルヘテロ構造の発光層形成部２９が形成されている。さらにその表面にＡｌＧａＡｓ系化合物半導体からなるｐ形のウインドウ層（電流拡散層）２５が設けられている。そして、その表面の中央部にＧａＡｓからなるコンタクト層２６を介して上部（ｐ側）電極２７および半導体基板の裏面に下部（ｎ側）電極２８が形成されている。
【０００３】この構造の半導体発光素子で、たとえば活性層２３のＰ点で発光した光は、四方に放射（半導体基板側にも進むが、半導体基板２１のＧａＡｓは光を吸収して表面側に取り出すことが困難であるため図示してない）され、電極以外の表面およびウインドウ層２５の側面から外部に取り出される。しかし、半導体層の屈折率は３．５程度であり、空気の屈折率は１、ランプ型にする場合など周囲を透明樹脂で被覆する場合でも、樹脂の屈折率は１．５程度であり、界面での入射角が小さくないと図５に示されるように、全反射をしてＬＥＤチップの内部を全反射しながら吸収などにより減衰してしまう。
【０００４】
【発明が解決しようとする課題】前述のように、半導体層とその外周の空気または透明樹脂などとの屈折率の差により、発光層で発光した光がチップの上面または側面で全反射する割合が高い。一方、クラッド層や活性層などは完全な透明体ではなく、発光層で発光した光を吸収し、また、半導体基板やコンタクト層などに用いられるＧａＡｓは、発光層で発光する光を吸収する材料であるため、全反射を繰り返すうちに吸収されて減衰する。そのため、外部に取り出すことができる光の割合が小さくなり、外部微分量子効率が向上しないという問題がある。
【０００５】本発明は、このような問題を解決するためになされたもので、発光層で発光した光をチップの外側にできるだけ取り出せる構造とし、外部微分量子効率を向上させることができる半導体発光素子を提供することを目的とする。
【０００６】
【課題を解決するための手段】本発明者らは、発光した光を外に有効に取り出すことができない原因を鋭意検討を重ねて調べた結果、発光層（活性層）で発光する光は四方に均一に放射されるが、とくに電流が集中して流れ電流密度が大きいチップの中心部で発光する光は、真上に行く光が上部電極で遮られ、コンタクト層で吸収されたり、反射しても再度半導体基板側に反射して吸収されてしまい、斜め方向に進む光は、上面または側面に大きな入射角で入射して全反射し、有効に取り出せないことに原因があることを見出した。そして、上面から側面にかけての界面（チップの外壁）を傾斜面とすることにより、斜め方向に進んできた光に対して入射角を小さくし、全反射させないで外に取り出すことができることを見出した。
【０００７】本発明による半導体発光素子は、半導体基板と、該半導体基板の上に設けられ、少なくともｎ形層およびｐ形層により活性層を挟持する発光層形成部を有する半導体積層部と、該半導体積層部の表面側に設けられる上部電極と、前記半導体基板の裏面側に設けられる下部電極とからなり、前記半導体積層部の前記活性層より上層部に前記上部電極側の幅が狭く、前記活性層側で幅が広くなるように側面に傾斜面が形成されている。
【０００８】この構造にすることにより、半導体積層部の上部電極が設けられた部分以外の上表面および側面が傾斜面となるため、斜めに表面側に向かってきた光も全反射することなく外側に出やすい。また、ウインドウ層（半導体積層部の上層部）の側面側に向かった光も、側面が内側に傾斜しているため、チップの外部との境界面では、その入射角が小さくなり、全反射しないで外部にでやすくなる。その結果、外部への光の取り出し効率が

向上し、外部微分量子効率を向上させることができる。

【0009】前記傾斜面が、外側が凸面となる傾斜面であれば、より一層チップ内部での入射角が小さくなり、外側へ光を取り出しやすくなる。

【0010】前記半導体積層部の表面側が、AlGaAs系化合物半導体層からなり、表面側ほどAlの混晶比が小さくなるように組成が変化する層であれば、Gaをエッチングしやすいエッチャントを用いることにより、Alの混晶比の小さい上層部はエッチングされやすく、Alの混晶比の大きい下層はエッチングされにくいため、容易に傾斜面を作りやすい。この場合、Alの組成比の変化を直線的に変化させることもできるが、上部を凸とする放物線状に変化させれば、エッチングのみで外側が凸面となる傾斜面とすることができる。

【0011】

【発明の実施の形態】つぎに、本発明による半導体発光素子について、図面を参照しながら説明をする。本発明による半導体発光素子は、図1にその一実施形態の断面説明図が示されるように、半導体基板1の上に、少なくともn形層3およびp形層5により活性層4を挟持する発光層形成部11を有する半導体積層部12が設けられている。また、半導体積層部12の表面側に上部電極（p側電極）8が設けられ、半導体基板1の裏面側に下部電極（n側電極）9が設けられている。そして、半導体積層部12の活性層4より上層部に上部電極8側の幅が狭く、活性層4側で幅が広くなるように側面に傾斜面が形成されていることに特徴がある。

【0012】発光層形成部11は、たとえば$In_{0.49}(Ga_{1-x}Al_x)_{0.51}P$（$0.6 \leqq x \leqq 0.8$、たとえばx＝0.67）からなるn形クラッド層3が0.1～2μm程度、たとえば587nm程度の発光波長とする$In_{0.49}(Ga_{1-y}Al_y)_{0.51}P$（$0.2 \leqq y \leqq 0.3$、たとえばy＝0.26）からなる活性層4が0.1～2μm程度、$In_{0.49}(Ga_{1-x}Al_x)_{0.51}P$（$0.6 \leqq x \leqq 0.8$、たとえばx＝0.67）からなるp形クラッド層5が0.1～2μm程度それぞれ成長されて形成されている。なお、発光層形成部を構成する半導体層は、InGaAlP系化合物半導体に限らず、AlGaAs系化合物半導体など、他の発光色の半導体層を用いることができる。

【0013】この発光層形成部11の表面に、$Al_zGa_{1-z}As$（$0.5 \leqq z \leqq 0.8$）からなるウインドウ層6が1～10μm程度設けられている。また、ウインドウ層6の表面には、上部電極8の下側のみにGaAsなどからなるコンタクト層7が設けられ、これらにより半導体積層部12が形成されている。

【0014】本発明の半導体発光素子においては、この半導体積層部12の活性層4より上層、たとえばウインドウ層6の側面が、半導体基板1の面に対して垂直方向ではなく、上部電極8側で幅が狭く、活性層4側で幅が広くなるように傾斜面に形成されている。図1に示される例では、たとえばピラミッド形状の4角錐の上部が上部電極8部分で底面に平行に切り取られた形状になっており、たとえばウインドウ層6の厚さAが6μm程度で、上部電極8からチップ側面までの距離Bが約50μm程度（チップの一辺が200μm程度で、上部電極8の一辺が100μm程度）であり、傾斜角θは、約7°程度になる。しかし、ウインドウ層をもっと厚くすれば傾斜角も大きくすることができ、60°以下程度であれば、外部への光の取り出し効率を向上することができた。

【0015】このような傾斜面を形成するには、たとえば半導体積層部12を形成し、その上に上部電極8を形成してコンタクト層7をパターニングした後に、ウェハの状態で、図2に示されるように、チップの境界部に開口部16aを形成したホトレジスト膜16を設け、その開口部16aから露出するウインドウ層6を、たとえば昭和電工（株）商品名ショウポリッシュによりエッチングすることにより、表面側がオーバーエッチングされて図2に示されるように凹部17が形成される。この凹部17の中心部でダイシングすることにより、チップの側面に傾斜面が形成されたLEDチップが得られる。この傾斜面の形成法としては、このようなエッチングによらなくても、機械的研磨などの方法によっても形成することができる。

【0016】また、エッチングにより形成するにしても、とくに前述のエッチャントは、Gaをよくエッチングするため、ウインドウ層として、前述の$Al_zGa_{1-z}As$を使用し、Alの組成を表面側にいくにしたがって減らすことにより、表面側ほどよくエッチングされ、傾斜面を形成しやすい。このウインドウ層6のAlの組成を順次減らすには、図3（a）に示されるように、ウインドウ層の下面から上面に直線状にまたは階段状（図示せず）に減らすこともできるし、図3（b）に示されるように、放物線状に減らすこともできる。この組成を変化させるには、後述するMOCVD法により行う場合、導入ガスの流量を変化させることにより、容易に変化させることができる。

【0017】このような放物線状にAlの組成を減らすことにより、エッチングスピードが放物線状に変化し、図4にウインドウ層6部の断面説明図が示されるように、側面の傾斜面が外側に凸の形状となる。このような外側に凸の形状になるように傾斜面を形成すると、活性層4で発光して斜め上方に向かう光はチップの境界面では凹面をなす界面に入射するため、より一層入射角が小さくなり、全反射することなく光が透過しやすくなる。その結果、より一層光の取り出し効率が向上して好ましい。

【0018】上部（p側）電極8は、たとえばAu-Be／Ni／Ti／Auなどを全面に設けた後にパターニ

ングすることにより形成されてもよいし、電極が設けられる部分以外にマスクを設けて、全面に電極材料を被膜してからマスクを除去するリフトオフ法により形成されてもよい。また、GaAsからなる半導体基板1の裏面には、全面にAu-Ge／Ni／Auなどが0.2～0.4μm程度の厚さに設けられ、n側電極9が形成されている。

【0019】本発明の半導体発光素子によれば、ウインドウ層の上面および側面が繋がった傾斜面になっているため、たとえば図1（b）に一部の発光経路が示されるように、活性層4の発光部Pで発光し、斜め方向に進んだ光は、上面や側面に大きな入射角で入射しないで、傾斜面に直接小さな入射角で入射する。すなわち、半導体層の屈折率は、3.3～3.7程度で、その外部に透明なエポキシ樹脂が設けらる場合、その屈折率は1.5～1.55程度であり、臨界角は30°程度になる。すなわち、入射角が30°程度以下であれば全反射することなくウインドウ層の界面から光が外に取り出されるが、それより大きな入射角で入射すると全反射をする。しかし、本発明によれば、斜め方向に向かう光に対して、傾斜面が対向するため、入射角が小さくなり、光が外に出やすくなる。

【0020】さらに、本発明では、上部電極を挟んで両外側に傾斜面が形成されているため、傾斜面が互いに近づくか遠ざかる方向で対向し、平行に向き合わない構造になる。そのため、たとえ全反射をしても対向する傾斜面では光が出やすくなる。その結果、チップ内部で何回も全反射を繰り返して中で減衰しないで、効率よく外に取り出すことができる。

【0021】また、前述のように傾斜面が外側に凸になるように形成されることにより、より一層傾斜面に対する入射角が小さくなり、光の取り出し効率が向上する。このような傾斜面を簡単に形成するのに、たとえばAlGaAs系化合物半導体のAl組成など、その組成を変化させることにより、選択的にエッチングをすることができ、組成の変化に応じた形状の傾斜面を形成することができる。また、前述のAlGaAs系化合物半導体のAl比率を表面側で少なくすることにより、腐食しやすいAlの露出が少なくなり、保護層の機能も果たし、より一層効果が大きい。とくに放物線状にAlの比率が小さくなることにより、Alの比率が小さくなると発光する光を吸収しやすくなるが、その層が非常に薄いため、吸収の影響も殆どなくなる。

【0022】この半導体発光素子を製造するには、たとえばn形GaAs基板1をMOCVD（有機金属化学気相成長）装置内に入れ、反応ガスのトリエチルガリウム（TEG）またはトリメチルガリウム（TMG）、アルシン（AsH_3）、トリメチルアルミニウム（TMA）、トリメチルインジウム（TMIn）、n形ドーパントとしてのH_2Se、p形層形成の場合はp形ドーパントとしてのジメチル亜鉛（DMZn）の必要なガスをそれぞれ導入し、図1（a）に示されるように、$In_{0.49}(Ga_{0.3}Al_{0.7})_{0.51}P$からなるn形クラッド層3を0.1～2μm程度、ノンドープの$In_{0.49}(Ga_{0.75}Al_{0.25})_{0.51}P$からなる活性層4を0.1～2μm程度、$In_{0.49}(Ga_{0.3}Al_{0.7})_{0.51}P$からなるp形クラッド層5を0.1～2μm程度、たとえば$Al_{0.7}Ga_{0.3}As$からなるp形ウインドウ層6を1～10μm程度、GaAsからなるコンタクト層7を0.2～1μm程度それぞれ連続的に成長する。

【0023】その後、Au-Be／Ni／Ti／Auなどをリフトオフ法、マスク蒸着、または全面に成膜した後にホトリソグラフィ法によるパターニングにより、上部（p側）電極8を形成し、さらに半導体基板1の裏面にAu-Ge／Ni／Auなどを全面に設けて下部（n側）電極9を形成する。その後、半導体積層部12の表面に上部電極8部を覆ってレジスト膜を設け、チップ境界面に開口部を設ける。この開口部の大きさは、たとえば前述のウインドウ層6の厚さAが6μm程度で、横の長さが50μm程度、ウインドウ層6の$Al_zGa_{1-z}As$のzを下面から上面まで、たとえば0.7から0.5程度に変化させる場合、幅が30μm程度の開口部を設けると良好な傾斜面が得られる。その後、エッチングによる凹部の底面でチップ化することにより図1（a）に示されるLEDチップが得られる。

【0024】

【発明の効果】本発明の半導体発光素子によれば、発光部から斜め方向に進む光に対して、チップの壁面（半導体積層部上層のたとえばウインドウ層の壁面）が傾斜面により対向しているため、斜め方向に進んできた光をそのまま外に取り出すことができ、結果的に非常に外部微分量子効率が向上する。しかも、斜め方向に進んできた光を殆どそのまま透過させるため、チップから外に出た光も四方に進みやすく、横方向の輝度が向上し、広い面積を照射する用途に適し、たとえば液晶表示装置のバックライトのように面全体を照射する光源に適する。その結果、明るい液晶表示装置用のバックライトが得られる。

【図面の簡単な説明】

【図1】本発明の一実施形態であるLEDチップの断面説明図である。

【図2】図1のLEDチップの傾斜面を形成する工程の断面説明図である。

【図3】図1のLEDチップの傾斜面を作るのに適したウインドウ層の組成の変化の例を示す図である。

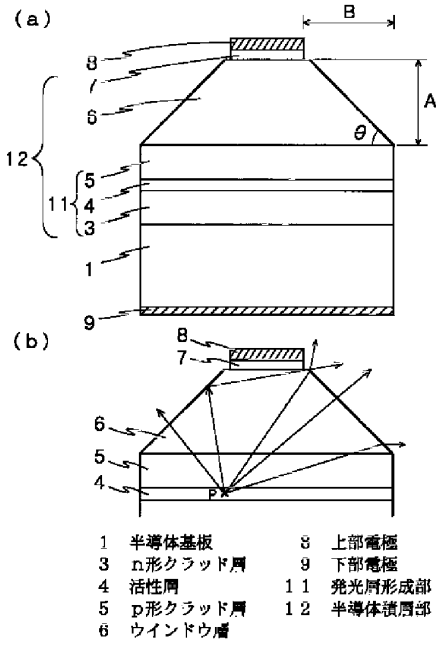
【図4】本発明による半導体発光素子における傾斜面の他の構造例を示す図である。

【図5】従来のLEDチップの構造例を示す断面説明図である。

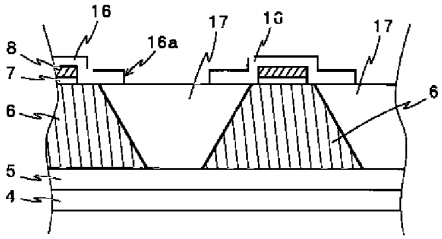
【符号の説明】

1　半導体基板
3　n形クラッド層
4　活性層
5　p形クラッド層
6　ウインドウ層
8　上部電極
9　下部電極
11　発光層形成部
12　半導体積層部

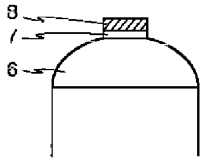
【図1】



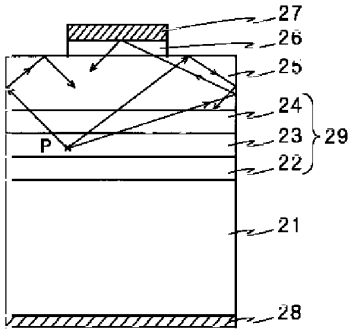
【図2】



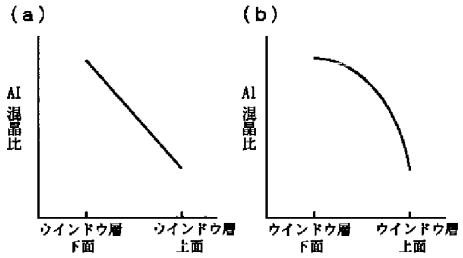
【図4】



【図5】



【図3】



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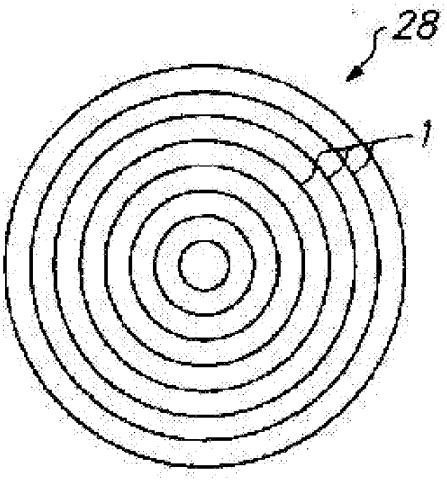
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(71)Applicant : LUMILEDS LIGHTING US LLC
(72)Inventor : POCIUS DOUGLAS W
CAMRAS MICHAEL D
HOFLER GLORIA E

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(54) FORMATION OF OPTICAL ELEMENT OF LIGHT EMITTING DEVICE FOR IMPROVING LIGHT EMITTING RATE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a light emitting device containing either one or both of a Fresnel lens and a holographic diffuser formed on the surface of a semiconductor light emitting element for improving the light emitting rate of the element, and to provide a method of forming the device.
SOLUTION: An optical element formed on the surface of the semiconductor light emitting element improves the light emitting efficiency of the element by reducing the reflection losses and total-reflection losses. The Fresnel lens and holographic diffuser can be formed on the surface of the light emitting element by using a chemical wet etching technique or dry etching technique together with a lithographic technique. The lens and diffuser can also be formed by shaving the surface of the element. Even when a stamping process which is another method of forming the optical element is used, the lens and diffuser can be formed on the surface of the element. The stamping process includes a step of pressing a shape obtained by inverting a desired optical element and a patterned stamping block against the surface of a light emitting diode.



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審査請求　未請求　請求項の数45　ＯＬ　（全 13 頁）

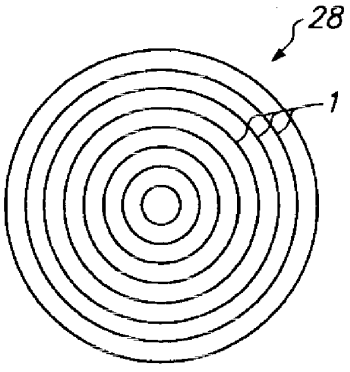
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(71)出願人　50050/009
ルミレッズ　ライティング　ユーエス　リミテッドライアビリティ　カンパニー
アメリカ合衆国　カリフォルニア州　95131　サン　ホセ　ウェスト　トリンブル　ロード　370
(72)発明者　ダグラス　ダブリュー　ポーシャス
アメリカ合衆国　カリフォルニア州　94087　サニーヴェイル　ペアー　アヴェニュー　804
(74)代理人　100059959
弁理士　中村　稔　（外９名）

最終頁に続く

(54)【発明の名称】　光取出率を改善するための発光デバイスにおける光学エレメントの形成

(57)【要約】
【課題】　光の取出率を改善するために半導体発光素子の面に形成されたフレネルレンズ及びホログラフィックディフューザの一方又は両方を含む発光デバイス、このような発光デバイスを形成するための方法を提供する。
【解決手段】　半導体発光素子の面に形成された光学エレメントは、反射損失及び全反射による損失を低減して、光の取出効率を改善する。フレネルレンズ、ホログラフィックディフューザは、化学的ウェットエッチング又はドライエッチング技術をリソグラフィー技術と共に用いて面上に形成できる。フレネルレンズ、ホログラフィックディフューザの形成は、表面に削り加工等を行ってもできる。光学エレメントを形成する別の方法であるスタンピング工程を用いても、半導体発光素子の面にフレネルレンズやホログラフィックディフューザを形成できる。スタンピングは、所望の光学エレメントを逆にした形状及びパターンスタンピングブロックを発光ダイオードの面に対してプレスする工程を含む。



【特許請求の範囲】
【請求項１】　半導体発光素子によって放射される光に作用を及ぼすよう、前記半導体発光素子の少なくとも一つの面にフレネルレンズ及びホログラフィックディフューザのうちの少なくとも一つを形成する工程を含む、発光デバイスを形成する方法。
【請求項２】　前記半導体発光素子は光を取り出すことを意図した少なくとも一つの光取出面を有し、前記形成工程を、前記半導体発光素子の少なくとも一つの光取出面において行うものである請求項１に記載の方法。
【請求項３】　前記形成工程は、スタンピングブロックを、前記半導体発光素子の少なくとも一つの面にプレスする工程を含んでいる請求項１に記載の方法。
【請求項４】　前記形成工程は、ウェハーボンディングプロセスと同時に実行され、前記ウェハーボンディングプロセスは、
前記半導体発光素子の第一のサブストレートを取り除く工程と、
第二のサブストレートを前記半導体発光素子にボンディングする工程とを含んでいる、請求項１に記載の方法。
【請求項５】　前記形成工程は、エッチング加工、削り加工、アブレーション加工、機械加工、スクライビング加工、放電加工、及びスタンピング加工から選択した少なくとも一つの方法を含んでいる請求項１に記載の方法。
【請求項６】　前記半導体発光素子の一又は二以上の側面を傾斜させる工程を含んでいる請求項１に記載の方法。
【請求項７】　請求項１に記載の方法において、前記半導体発光素子は発光層を有しており、前記方法は、さらに、前記発光層の予め選択された部分に光放射を制限することを含んでいる方法。
【請求項８】　前記制限することには、ホロニアクプロセスの適用、選択領域成長の使用、選択領域ボンディングの使用、ディフィージョンの使用、そしてイオン注入の使用の中から選択された少なくとも一つの方法が含まれている、請求項７に記載の方法。
【請求項９】　請求項１に記載の方法において、さらに、前記半導体発光素子の一又は二以上の面に反射材をコーティングする工程を含んでいる方法。
【請求項１０】　請求項１に記載の方法において、さらに、前記フレネルレンズ又は前記ホログラフィックディフューザに反射材をコーティングする工程を含んでいる方法。
【請求項１１】　請求項２に記載の方法において、さらに、前記取出面とは反対側の面に光学エレメントを形成する工程を含んでいる方法。
【請求項１２】　半導体発光素子と、
前記半導体発光素子の少なくとも一つの表面を形成する第一の光学エレメントと、を有し、前記第一の光学エレメントはフレネルレンズ及びホログラフィックディフューザのうちの一方を含んでいる発光デバイス。
【請求項１３】　請求項１２に記載のデバイスにおいて、さらに、前記デバイスの少なくもと一つの面をコーティングする反射材を含んでいるデバイス。
【請求項１４】　前記半導体発光素子の発光層が、主に前記第一の光学エレメントの予め決められた部分に向かって光子を放射するように作られた、請求項１２に記載のデバイス。
【請求項１５】　発光デバイスの少なくとも一つの面は傾斜されている、請求項１２に記載のデバイス。
【請求項１６】　前記半導体発光素子は、制限放射スポット発光ダイオードである、請求項１２に記載のデバイス。
【請求項１７】　前記半導体発光素子及び前記第一の光学エレメントは、
$(Al_xGa_{1-x})_yIn_{1-y}P$（$0 \leqq x \leqq 1$、$0 \leqq y \leqq 1$）
を含んでいる請求項１２に記載のデバイス。
【請求項１８】　前記発光ダイオードは、III-窒化物半導体化合物を含んでおり、前記第一の光学エレメントは、シリコンカーバイド及びサファイアのうちの一方を含んでいる、請求項１２に記載のデバイス。
【請求項１９】　前記半導体発光素子及び前記第一の光学エレメントは、アルミニウム・ガリウム・砒素半導体化合物を含んでいる請求項１２に記載のデバイス。
【請求項２０】　前記半導体発光素子は、フリップチップ構造を含んでいる請求項１２に記載のデバイス。
【請求項２１】　前記半導体発光素子は、前記半導体発光素子の発光層は前記フレネルレンズに対して実質的に垂直である、請求項１２に記載のデバイス。
【請求項２２】　請求項１２に記載のデバイスにおいて、前記デバイスの放射パターンは、前記第一の光学エレメントと前記半導体発光素子の発光層との距離に対する前記第一の光学エレメントの焦点距離の比によって制御されるデバイス。
【請求項２３】　前記第一の光学エレメントは、光をフォーカスする作用、光をコリメートする作用、光を発散する作用のうちの一つを達成するよう設計されたものである請求項１２に記載のデバイス。
【請求項２４】　前記第一の光学エレメントは、光を予め選択した方向に導くよう設計されたものである請求項１２に記載のデバイス。
【請求項２５】　請求項１２に記載のデバイスにおいて、さらに、前記半導体発光素子の前記第一の光学エレメントを有する面とは反対の面に第二の光学エレメントを有するデバイス。
【請求項２６】　前記第一のフレネルレンズ及び第二のフレネルレンズのうちの一方が光をフォーカスするよう設計されたものである請求項２５に記載のデバイス。

【請求項２７】　半導体発光素子によって放射される光に作用を及ぼすよう、前記半導体発光素子の少なくとも一つの面にスタンピングを行う工程を含んでいる、発光デバイスを形成するための方法。
【請求項２８】　請求項２７に記載の方法において、さらに、前記発光デバイスの面に反射層をコーティングする工程を含んでいる方法。
【請求項２９】　前記スタンピングを、前記半導体発光素子の半導体層及びサブストレート層のうちの少なくとも一方に対して行う、請求項２７に記載の方法。
【請求項３０】　前記半導体層は、アルミニウムを含む透明な化合物を含んでいる請求項２９に記載の方法。
【請求項３１】　前記プレスする工程は、室温よりも高い温度において実行される、請求項２７に記載の方法。
【請求項３２】　請求項３１に記載の方法において、さらに、前記プレス工程の後に前記半導体発光素子から前記スタンピングブロックを引き離すのを容易にするために、前記高い温度を低くする工程を含んでいる方法。
【請求項３３】　前記高い温度は、前記フレネルレンズを形成する前記少なくとも一つの面を構成する材料の延性遷移温度よりも高いものである請求項３２に記載の方法。
【請求項３４】　半導体発光素子と、
半導体発光素子の少なくとも一つの面にスタンピングされた少なくもと一つの光学エレメントとを含み、
前記光学エレメントは第一の光学エレメントである発光デバイス。
【請求項３５】　前記半導体発光素子の発光層は、主に前記第一の光学エレメントの予め選択した方向に光子を放射するよう設計されたものである請求項３４に記載のデバイス。
【請求項３６】　前記発光層及び前記第一の光学エレメントは、
$(Al_xGa_{1-x})_yIn_{1-y}P$（$0 \leqq x \leqq 1$、$0 \leqq y \leqq 1$）
を含んでいる請求項３４に記載のデバイス。
【請求項３７】　前記半導体発光素子は、III-窒化物半導体化合物を含んでおり、前記第一の光学エレメントは、シリコンカーバイド及びサファイアのうちの一方を含んでいる、請求項３４に記載のデバイス。
【請求項３８】　前記半導体発光素子及び前記第一の光学エレメントは、アルミニウム・ガリウム・砒素半導体化合物を含んでいる請求項３４に記載のデバイス。
【請求項３９】　前記発光ダイオードは、フリップチップ構造を有している請求項３４に記載のデバイス。
【請求項４０】　前記発光ダイオードは、前記発光ダイオードの発光層が前記フレネルレンズに対して実質的に垂直な構造を有している請求項３４に記載のデバイス。
【請求項４１】　複数の発光デバイスを含んでいる発光ダイオードアレーであって、
半導体発光素子と、
前記半導体発光素子の面に形成されたフレネルレンズ及びホログラフィックディフューザのうちの一つと、
を含んでいる発光ダイオードアレー。
【請求項４２】　複数の発光デバイスを含んでいる発光アレーであって、
半導体発光素子と、
前記半導体発光素子の面にスタンピングされた光学エレメントと、
を含んでいる発光アレー。
【請求項４３】　少なくとも一つの青色発光デバイス、少なくとも一つの緑色発光デバイス、少なくとも一つの赤色発光デバイスを含んだディスプレーデバイスであって、前記青色発光デバイス、緑色発光デバイス、赤色発光デバイスのうちの少なくとも一つは、
半導体発光素子と、
前記半導体発光素子の面に形成されたフレネルレンズ及びホログラフィックディフューザのうちの一つと、
を含んでいるディスプレーデバイス。
【請求項４４】　少なくとも一つの青色発光デバイス、少なくとも一つの緑色発光デバイス、少なくとも一つの赤色発光デバイスを含んだディスプレーデバイスであって、前記青色発光デバイス、緑色発光デバイス、赤色発光デバイスのうちの少なくとも一つは、
半導体発光素子と、
前記半導体発光素子の面にスタンピングされた一つの光学エレメントと、
を含んでいるディスプレーデバイス。
【請求項４５】　発光デバイスから放射される光に対して透明な材料に光学エレメントをスタンピングする工程と、
前記光学エレメントを半導体発光素子にボンディングする工程と、を含む、発光デバイスを形成する方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、発光デバイス一般に、より詳しくは、光取出率が改善された発光デバイスに関する。
【０００２】
【従来の技術】図１は、従来からの半導体発光素子１００であり、基板２０、多層構造２６、最上層２４から構成されている。半導体発光素子１００としては、例えば発光ダイオード（ＬＥＤ）又は半導体レーザーが考えられる。ＬＥＤは、電気エネルギーの入力流を電磁放射の出力流に変換するよう設計されたｐｎ接合デバイスである。ＬＥＤは、電磁スペクトルの紫外領域、可視領域、赤外領域の電磁放射を発することができる。可視ＬＥＤは通常、照明及びディスプレーに用いられ、また、電子機器とそのユーザーとの間の情報リンクとしての応用もある。赤外ＬＥＤは、オプトアイソレータ及び光ファイ

バー通信において有用である。半導体レーザーは、ＬＥＤと同様の方法で作製される。

【０００３】多層構造２６は、ここでは下部封止層（confining layer）２１、上部封止層２３、光子が発せられる活性層２２を含んでいるが、この構造に限られるものではない。上部封止層２３は、最上層２４を含んでいてもよい。半導体発光素子１００が分離した最上層２４を有していない場合は、上部封止層２３が最上層となる。

【０００４】多層構造２６の封止層２１，２３及び活性層２２は、通常、III-V半導体、III-窒化物半導体、II-VI半導体から形成される。最上層２４は、上部封止層２３上にエピタキシャル成長させることができるが、これもまた普通はIII-V半導体、III-窒化物半導体、II-VI半導体、あるいはこれらの化合物である。しかしながら、最上層２４は、封止層２１又は封止層２３を形成する材料とは異なる半導体化合物とすることもできる。最上層２４は、活性層２２によって発せられた光に対して透明となるよう、活性層２２よりも大きなバンドギャップを有する材料とすることが望ましい。ここでは「透明」という用語は、特定の半導体発光素子の放射波長において、吸収又は散乱による単光路損失が約５０％より少ない、より望ましくは約１０％より少ない状態で、光学エレメントが光を透過することを意味する。最上層２４は、上部封止層２３にウェハ・ボンディングされた透明なサブストレート（スーパーストレート）とすることができる。最上層２４はまた、その上にエピタキシャル層を成長させたサブストレートとしてもよい。

【０００５】下部封止層２１及び上部封止層２３は、活性層２２に、そしてコンタクト３１及びコンタクト３２に電気的に接続されている。通常、一方の封止層にはドナーがドープされてｎ型の封止層とされ、他方の封止層にはアクセプタがドープされてｐ型の封止層とされる。したがって、コンタクト３１と３２との間に適当な電圧を印加すると、ｎ型封止層からの電子とｐ型封止層からのホールが活性層２２内で結合して、等方的に光を発する。ＬＥＤとしての半導体発光素子１００についてのより詳細な説明については、Michael R. Kramesらに付与された「AlGaInN-based LED Having Thick Epitaxial Layer for Improved Light Extraction」と題された米国特許第６，１３３，５８９号、Fred A. Kish, Jr.らに付与された、いずれも「Transparent Substrate Light Emitting Diode with Directed Light Output」と題された米国特許第５，７９３，０６２号及び第６，０１５，７１９号を参照することができる。これらすべての特許を、参考としてここに援用する。

【０００６】半導体発光素子１００をＬＥＤ１００とすることができる。ＬＥＤについての問題は、光の取出効率が低いことである。この光の取出効率が低い原因は、ＬＥＤ１００から出ようとする光が、活性層２２によって発せられた光エネルギーのうちのわずかのみ（例えば透明基板を有するAlGaAsＬＥＤの場合、大体３０％程度）だということである。光の取出効率が低い結果、消費される電気的な入力のうちのわずかの部分だけが、外部から観測できる光に寄与する。光の取出効率は、ＬＥＤにおいて生成される光子の数に対する、ＬＥＤから出てくる光子の数の比として定義される。

【０００７】図１の経路３は、活性層２２の点光源２７から放射される光子の方向を示している。経路３によって示されるように、コンタクト３１，３２の吸収特性が、低い光の取出率に寄与する。経路３に沿って進む光子は、ＬＥＤ１００の内側面で反射されコンタクト３１によって吸収される。コンタクト３１及び３２は、金、ニッケル、アルミニウム、チタン、クロム、パラジウム、そしてこれらの合金又は化合物などの金属から形成することができる。

【０００８】低い光の取出効率を生じさせる損失の機構には、半導体発光素子内における吸収、光が一つの材料から屈折率の異なる別の材料へ入るときの反射損失、発光デバイス内で吸収されることになる全反射が含まれる。しかしながら、全反射は、活性層２２によって発せられた光子が発光デバイス１００とその周囲の材料との境界に臨界角（θc）よりも大きい角度で到達したときのみ、光子が半導体発光素子１００から出ることを妨げる。本実施例に関連する臨界角（図１にθcで示す）は、

$\theta c = arcsine(n_{surrounding} / n_{LED})$

によって定義される。ここで、$n_{surrounding}$及びn_{LED}はそれぞれ、発光デバイスの周囲の材料と発光デバイスの屈折率を示している。ＬＥＤはしばしばエポキシ内に封入されるが、その屈折率（n_{epoxy}）は大体１．５程度である。前述のIII-V半導体材料の一つで作られたＬＥＤでは、その屈折率は約２．４から約４．１までの範囲である。平均的な屈折率（n_{LED}）を約３．５とすると、θcの典型的な値は約２５°である。したがって、活性層２２内の点光源２７から発せられる光子のうち半角が２５°の「取出円錐」内の任意の表面を通るものは、ＬＥＤから外部へ放射される。ＬＥＤ１００と取出円錐の外側の材料との間の境界面に当たる光子は、全反射を繰り返し受け、例えば半導体層（活性層２２を含む）又はコンタクト３１及び３２によって吸収されることになる。すなわち、表面に垂直な軸に対して２５°よりも大きい角度で表面に当たる多くの光子は、最初の段階でＬＥＤから外部へは放射されない。発せられた光子のうちのより多くの部分が取り出される高い光の取出効率を有するＬＥＤが必要とされている。

【０００９】

【課題を解決するための手段】本発明は、半導体発光素子の光取出率を改善するとともに、所望の放射パターンを得るために光を導き、フォーカスし、そして散乱させ

るのに用いられる。本発明には、例えばフレネルレンズ、ホログラフィックディフューザなどの一又は二以上の光学エレメントに適合するようにされた半導体発光素子、そして半導体発光素子の表面をスタンピング（stamping）して光学エレメントに形成する方法が含まれる。半導体発光素子１００の一又は二以上の表面を、フレネルレンズ又はホログラフィックディフューザに形成することができる。フレネルレンズは、活性層２２から発せられたより多くの光子が垂直に近い入射角で半導体発光素子１００の表面に当たるようにし、全反射による光の損失を最小限に抑えることができるので、表面をフレネルレンズにすることは望ましい。さらに、フレネルレンズに形成された半導体発光素子の表面は、半導体発光素子を構成する材料とは異なる屈折率を有するレンズの材料によって通常引き起こされる光の反射損失を低減する。フレネルレンズ及びホログラフィックディフューザの一方又は両方を、フォトリソグラフィー、電子ビームリソグラフィー、イオンビームリソグラフィー、Ｘ線リソグラフィー、ホログラフィックリソグラフィーなどを含む（ただし、これらに限定されるものではない）リソグラフィー技術に関連したエッチングによって形成することができる。プラズマエッチング、反応性イオンエッチング（ＲＩＥ）、及び化学的手段を援用したイオンビームエッチング（ＣＡＩＢＥ）などの化学的ウェットエッチング又はドライエッチング技術を用いることができる。あるいは、イオンビーム削り加工（ion beam milling）又はフォーカスされたイオンビーム削り加工（ＦＩＢ）を用いてフレネルレンズを表面に刻印し、走査させた電子又はレーザービームを用いて表面にフレネルレンズをアブレーション加工し、または削り加工やスクライビング加工を行って機械的に半導体発光素子１００の表面にフレネルレンズを形成することもできる。

【００１０】スタンピングは、発光デバイスの表面上に光学エレメントを形成する別の方法である。スタンピングプロセスは、スタンピングを行うとする半導体材料の延性遷移点（ductile transition point）よりも高い温度で実行される。一つの実施例では、スタンピングは、ウェハ・ボンディングプロセスと統合される。ウェハ・ボンディングプロセスは通常６００℃近傍又はこれよりも高温で行われるので、ウェハ・ボンディングプロセスを容易にウェハ・ボンディングプロセスと統合することができ、これによって生産効率を向上させることができる。ウェハ・ボンディングプロセスでは、所望の品質のエピタキシャル層を成長させるためのテンプレートとして用いられた最初の吸収性のサブストレートを除去すること、そして光の取出率を改善するためにこれを透明なサブストレートと置き換えることを伴う。オプションとして、透明なサブストレートを半導体発光素子１００の第一の表面にボンディングする時点において、所望の光学エレメントの形状又はパターンの逆の形状又はパターンを有するスタンピングブロックを、半導体発光素子１００の第二の表面、透明サブストレートの表面、又はこれらの両方に対してプレスしてもよい。圧力を開放したときに、所望の光学エレメントに形作られた表面を有する発光デバイスが形成される。スタンピングに用いられるスタンピングブロックは、通常、光学エレメントの形成時に適用されるプロセス温度よりも高い融点を有する。スタンピングブロックに適する材料としてモリブデン合金、グラファイト、シリコンカーバイド、そしてサファイアなどがあるが、これらに限定されるものではない。半導体発光素子の一又は二以上の表面上に、光学エレメントを形成することができる。スタンピングプロセスは独立したプロセスであるが、ウェハ・ボンディングプロセスの前、後、あるいは同時に行うことも可能である。あるいはまた、スタンピングプロセスを、後に半導体発光素子１００に対してボンディングされる材料をスタンピングするのに用いてもよい。

【００１１】本発明は、容易に、別の応用に合うよう適合させることができる。例えば、照明用に光をコリメートするように光学エレメントを作ったり、あるいは光ファイバーに光をフォーカスするように作ることもできる。さらに、ＬＥＤの任意の表面を一又は二以上の光学エレメントに形作ったり、二以上の表面を一又は二以上のフレネルレンズに形作ったりもできる。コリメートされた光又はフォーカスされた光を所望の方向に導くために、反射コーティングを用いることもできる。半導体発光素子１００上に多数の光学エレメントを形成することによって作られるダイオードアレーを、高出力の応用目的に用いることもできる。

【００１２】光学エレメントの予め決められた部分に向かって放射される光子の割合を増大させることによって、本発明の有用性はさらに高まる。例えば、フレネルレンズが存在してもその縁部に到達する光子は有益性が小さいので、放射されたより多くの割合の光子がフレネルレンズの中心に向かって放射されるような制限放射スポット（confined-emission spot）ＬＥＤを作ることができる。光子の放射を活性層の選択した領域へ閉じ込める方法には、イオンの注入又は拡散、酸化物不活性化（oxide passivation）、選択領域成長（selective area growth）、選択領域ボンディング（selective area bonding）が含まれる。あるいは、半導体発光素子１００又は活性層２２の外側の縁部を、エッチングで取り除いてもよい。外側の縁部をエッチングで取り除くことによって、傾斜した側面を有する発光デバイスを作ることができる。

【００１３】

【発明の実施の形態】本明細書で参照する図面は、縮尺通りには描かれていない。

【００１４】本明細書において「取出面」とは、光出力面となるよう意図した発光デバイスの面を指す。発光デ

バイスは、二以上の取出面を備えることもできる。図示を簡単にするために、図では取出面を一番上の面としている。発光デバイスはＬＥＤとすることができる。ここで説明するＬＥＤの光を生成する部分は、ＬＥＤの通常の活性層である。ここで用いている「発光デバイス」は、少なくとも一つの半導体発光素子１００を有するデバイスを含んでいる。本発明は、発光デバイスの表面をスタンピングして光学素子にすることと、発光デバイスの表面にスタンピングを含む任意の方法を用いてフレネルレンズ又はホログラフィックディフューザを形成することの両方を含んでいる。本発明はまた発光デバイスの表面上に形成されたホログラフィックディフューザを含んでいるが、この例及び説明では、分かり易い例示とするために、主としてフレネルレンズを参照する。同じく分かり易い例示のために、半導体発光素子１００を発光ダイオード１００として説明する。異なる図で同じ符号を有する要素は、同じものである。

【００１５】図２Ａ、図２Ｂ、図３Ａ、図３Ｂ、図４Ａ、図４Ｂ、図５Ａ、図５Ｂに示したように、フレネルレンズ２８は、収束レンズの単一の曲面とは対照的に、表面上に一連の同心のグルーブが形成されて構成されている。グルーブ１は、屈折面として作用する湾曲した、あるいは角度をつけた面を有している。グルーブ１は、図２Ａ及び図３Ａに示すように、一定間隔とすることができる。図２Ｂ及び３Ｂに示すように、フレネルレンズ２８のグルーブが一定間隔のときは、フレネルレンズ２８を希望の焦点距離とするようにグルーブの高さを変えることができる。グルーブの形状は、例えば光線を集束させるために図２Ｂのように、または光線を発散させるために図３Ｂに示すように変えることができる。あるいは、フレネルレンズ２８のグルーブが図４Ｂ、図５Ｂに示すように同じ高さのときは、グルーブ１間の間隔を調整して、希望の焦点距離のフレネルレンズ２８とすることができる。図４Ａ及び図５Ａに示すフレネルレンズ２８は、レンズの縁に近づくにつれてグルーブの間隔が狭くなる。図４Ｂ及び図５Ｂは、光を希望する通りに導くためにグルーブ１の形状を調整できることを示している。図４Ｂのフレネルレンズは光線を集束させ、図５Ｂのフレネルレンズは光線を発散させる。フレネルレンズ２８のグルーブ１は、レンズ中心の周囲に同心的に配置することは必要ではない。例えば図６には、同心でないグルーブ１を有するフレネルレンズ２８が示してある。フレネルレンズは、非球面に基づくものとすることも、球面に基づくものとすることもできる。さらに、フレネルレンズが形成される表面は平面である必要もない。フレネルレンズを任意の形状のＬＥＤ上、例えば長方形のＬＥＤ上、楕円形のＬＥＤ上、ピラミッド型のＬＥＤ上、そして円柱形のＬＥＤ上に形成することもできる。フレネルレンズ２８を半導体発光デバイス上に形成するときは、オプションとして、図２Ｂ、図３Ｂのフレネルレンズ２８の縁の近傍の高いグルーブ、および図４Ｂ、図５Ｂのフレネルレンズ２８の縁の近傍の間隔の狭いグルーブを省くことができる。

【００１６】図２Ｂ、図３Ｂ、図４Ｂ、図５Ｂは、通常の収束又は発散レンズ２の厚さを、フレネルレンズ２８と比較している。図示のように、フレネルレンズ２８は、ほぼ同じ焦点距離を有する通常のレンズ２よりも薄くなっている。レンズ材料（すわち半導体材料）は本来的にいくぶんかの光を吸収するので、ＬＥＤへの応用目的では、厚い普通のレンズよりも薄いフレネルレンズ２８は好ましい。

【００１７】図７Ａは、フレネルレンズ２８として示した、表面上に形成された光学エレメント２８を有する発光デバイスを例示している。半導体発光素子１００の取出面に形成されたフレネルレンズ２８は半導体発光素子１００からの光の取り出しを助けるが、これは、取出面が平坦でなくグルーブ１を有している場合には、放射されたより多くの光子が垂直に近い入射角で取出面に当たるからである。垂直に近い入射角で表面に当たる光子は全反射を受けず、したがってより取り出しやすくなる。反射材４０で底面をコーティングすると、底面における反射損失又は吸収損失による光の損失を軽減するのを助ける。経路５に沿って進む光子も、減衰及び最終的な吸収を受ける。後述のように、経路５に沿って進む光子を取り出すために、底面に設けたフレネルレンズを用いることもできる。

【００１８】図７Ａ、図７Ｂ、図７Ｃは、フレネルレンズ２８の高さ、グルーブの間隔、焦点距離と同様に、距離δによって、どのように発光デバイスの放射パターンを操作するかを例示している。距離δは、活性層２２とフレネルレンズ２８の距離を示している。距離δ、フレネルレンズ２８の水平位置、そしてフレネルレンズ２８の焦点距離は、発光デバイスの発光パターンに影響する。光源を実質的に収束レンズの焦点距離近くに置いたときは、図７Ａに示すように、出て行く光線は実質的に並行になる。距離δを変えることによって、光線を実質的に図７Ｂに示すように収束させたり、図７Ｃに示すように発散させることができる。図７Ｂに示すような光を収束させるような実施例は、光ファイバーへの応用に用いることができる。

【００１９】フレネルレンズ又はホログラフィックディフューザを表面に形成する方法は数多くある。「彫刻法」は、まず、例えば多層構造２６上に最上層２４を形成し、そしてプラズマエッチング、反応性イオンエッチング、化学的手段を援用したイオンビームエッチング（ＣＡＩＢＥ）などの化学的ウェットエッチング又はドライエッチング技術によって、最上層２４に希望のパターンを形作ることが必要となる。オプションとして、エッチング技術については、リソグラフィー技術を用いることもできる。リソグラフィー技術には、フォトリソグ

ラフィー、電子ビームリソグラフィー、イオンビームリソグラフィー、Ｘ線リソグラフィー、ホログラフィックリソグラフィーが含まれる（ただし、これらに限定されるものではない）。さらに、イオンビーム削り加工又はフォーカスされたイオンビーム削り加工を用いて表面に刻印し、走査させた電子又はレーザービームを用いて表面をアブレーション加工し、放電加工（ＥＤＭ）によって表面に加工し、または削り加工やスクライビング加工を行って、機械的に半導体発光素子１００の表面に、希望の光学エレメントを形成することができる。

【００２０】フレネルレンズ又はホログラフィックディフューザを、ボンディング法を用いて形成することもできる。ボンディング法には、多層構造２６に、通常ボンディング材料を用いて光学エレメントをボンディングする必要がある。ボンディング材料は、スピニング、スパッタリング、蒸着、化学気相成長、金属・有機化学気相成長、気相エピタキシャル、液相エピタキシャル、分子ビームエピタキシャルなどの一般的な堆積技術を用いて堆積させることができる。図７Ａに示した実施例ではボンディング材料を示していないが、ボンディング材料は、光学エレメント２８と上部導電層２３の間の境界２５ａにある。しかし、発光デバイスが最上層２４を含んでいる場合には、ボンディング材料は、光学エレメント２８と最上層２４の間にあってもよい。

【００２１】ボンディング法を用いるときは、境界２５ａ又は２５ｂにおける反射光損失を最小限に抑えるために、ボンディング材料がn_{LED}又はn_{lens}（n_{LED}とn_{lens}が異なる場合）に非常に近い屈折率（$n_{bonding}$）を有することが望ましい（図７Ａ）。デバイスが温度変化を受けたときのひずみを最小限に抑えるために、半導体発光素子とフレネルレンズ２８の両方と同等の熱膨張係数を持つボンディング材料とすることができる。さらに、ボンディング材料を、活性層２２によって発せられる光の波長に対して透明にすることもできる。例えば、レンズとボンディング材料を、以下に列挙するもののうちの一つとすることができる（ただしこれらに限定されるものではない）：屈折率の大きい光学ガラス、ＧａＰ（６００ｎｍで、ｎ～３．３）ＩｎＧａＰ（６００ｎｍで、ｎ～３．７）、ＧａＡｓ（５００ｎｍで、ｎ～３．４）、ＧａＮ（５００ｎｍで、ｎ～２．４）などのIII-V半導体、ＺｎＳ（５００ｎｍで、ｎ～２．４）、ＺｎＳｅ（５００ｎｍで、ｎ～２．６）、ＣｄＳ（５００ｎｍで、ｎ～２．６）、ＣｄＴｅ（５００ｎｍで、ｎ～２．７）、ＺｎＴｅ（５００ｎｍで、ｎ～３．１）などのII-VI半導体、IV族の半導体、そしてＳｉ（５００ｎｍで、ｎ～３．５）及びＧｅ（５００ｎｍで、ｎ～４．１）などの化合物、屈折率の大きい有機半導体、屈折率の大きい有機化合物、そしてこれらの混合物又は合金。$n_{bonding}$がn_{LED}及びn_{lens}と異なる場合には、半導体発光素子とボンディング材料の境界、そしてボンディング材料とフレネルレンズ２８の境界の両方において反射光損失が生じる。

【００２２】レンズ材料は、ボンディング材料なしで、高温環境でレンズと多層構造とをプレスすることで接着されるものを選択するのがよい。ボンディング材料を使わなければ、ボンディング材料の屈折率がn_{LED}と異なることによって増える光の損失を低減させることができる。接着については、「LED with Improved Light Extraction Efficiency」と題された米国特許出願第０９／６６０，３１７号においてさらに詳しく説明されており、その内容は、参考としてここに援用する。

【００２３】本発明に用いることができるさらに別の方法は、スタンピング法である。図８Ａは、半導体発光素子１００を含む発光デバイスと、光学エレメント２８が形成された表面を示している。図８Ｂは、図８Ａの光学エレメント２８として用いることのできるホログラフィックディフューザの概略図を示す。ホログラフィックディフューザの表面には、ランダムで非周期的な多数の小型レンズ（microlenslet）が含まれている。ホログラフィックディフューザは光を発散させ、ノイズ及び色回折（color diffraction）を取り除く。図８Ｂはホログラフィックディフューザとして光学エレメント２８を示しているが、光学エレメント２８は、通常のレンズ、フレネルレンズ、あるいは反射部なと、他の任意の光学エレメントであってもよい。

【００２４】図９に例示した典型的なプロセスでは、光学エレメント２８のパターンとは逆のパターンを有するスタンピングブロック７０によって、最上層２４がスタンピングされる。図９は、光学エレメント２８としてフレネルレンズ２８を示している。このスタンピング法は、半導体発光素子１００の任意の表面に光学レンズ２８を形成するのに用いることができる。図９は、スタンピングと同時に実行されるウェハーボンディングプロセスを示しているが、スタンピングはウェハーボンディングの前又は後、あるいは完全に別な独立したプロセスとして実行することも可能であることが理解されるだろう。例えば、ウェハーボンディングされていない半導体発光素子１００上に、光学エレメントをスタンピングしてもよい。あるいはまた、最初に材料の上で光学エレメントをスタンピングし、後に材料を半導体発光素子１００に接着することもできる。

【００２５】スタンピング法では、フレネルレンズ２８が形成されるのがＬＥＤの最上層２４であることから、フレネルレンズ２８の屈折率とＬＥＤの最上層２４の屈折率が同じくなる蓋然性は高い。スタンピングプロセスでは、半導体発光素子１００を少なくとも最上層２４の延性遷移点（ductile transition point）まで加熱し、そしてスタンピングブロック７０をプレスする。必要であれば、スタンピングを容易にするために、１００ｐｓｉ又はそれ以上の圧力を加えてもよい（正確な圧力は、

使用する材料及びプロセス温度に依存する）。半導体発光素子１００の最上層２４にスタンピングしたあとは、スタンピングブロック７０を得られた発光デバイスから離し易くするために、圧力を開放し温度を下げることができる。半導体発光素子１００上に正確なフレネルレンズのパターンをスタンピングするためには、スタンピングブロックの材料は、加えられる温度及び圧力に耐えられるものでなければならない。このため、スタンピングブロックの材料は、表面にスタンピングがなされる材料（例えば半導体材料）の延性遷移点よりも高い延性遷移点を有していることが適当である。スタンピングブロックとして適当な材料の例には、ＴＺＭ（モリブデン、チタン、ジルコン、そしてカーボンの化合物）などのモリブデン合金、グラファイト、シリコンカーバイド、そしてサファイア、ステンレススチール、Hastalloy（商標）、Kovar（商標）、Nichrome（商標）、タングステン及びタングステン合金、タンタル、ニオブ、チタン合金などが含まれる。

【００２６】製造プロセスにおいて通常は別個のステップであるボンディングプロセスと異なり、スタンピングは、ウェハーボンディングと同時に実行することも（図９参照）、あるいはウェハーボンディングプロセスとは別にその前又は後に行うことも可能である。ウェハーボンディングプロセスの目的は、まず通常は光を吸収する第一のサブストレート２０．１を取り除き、そしてこれを、より多くの光が外部へ到達できる新しいサブストレート２０．２と置き換えることによって、光の取出率を改善することである。第一のサブストレート２０．１は、所望の機械的特性を持った半導体発光層を製造するのに適合する材料である。例えば、高品質のエピタキシャル成長を達成し、確実な格子整合を得るために、標準的な吸収性のサブストレート材料を利用することができる。これらの吸収性の成長サブストレートは通常、半導体発光素子の放射エネルギーより小さいか又は同等のバンドギャップを有している。多層構造２６を成長させた後、第一のサブストレート２０．１を取り除く。第一のサブストレート２０．１は、化学エッチング及びラップ仕上げ／研磨を含む方法（たたし、これらには限定されない）によって取り除くことができる。

【００２７】第一のサブストレート２０．１を取り除いたら、続いて、光学的には透明な第２のサブストレート２０．２を半導体発光素子１００に接着する。接着の手順には、新たなサブストレート２０．２を、その組成に依存して２５℃と１０００℃の間の温度に加熱することが含まれる。ウェハーボンディングプロセスについては、Fred A. Kishらに付与された「Wafer Bonding of Light Emitting Diode Layers」と題された米国特許第５，５０２，３１６号においてさらに詳しく説明されており、その内容はここに援用するものとする。新たなサブストレート２０．２とスタンピングブロック７０の両方を半導体発光素子１００に同時にプレスすることによって、スタンピングプロセスをウェハーボンディングプロセスに組み込むことができる。スタンピングブロック７０は、新たなサブストレート２０．２、最上層２４、あるいはこれらの両方に対してフレネルレンズ２８をプレスすることができる。図９では分かり易さと簡単のためにただ一つの光学エレメントを示しているが、スタンピングブロック７０には、二以上の光学エレメントのパターンを含ませることもできる。

【００２８】図１０は、側面を傾斜させた半導体発光素子１００を示している。側面を傾斜させると、経路３及び経路４の違いとして示すように、光子が反射する角度にすることによって光の取出率が向上する。側面が傾斜しているときは、活性層２２によって放射された光子は、経路３ではなく経路４（実線）に沿って進むことができる。経路３は、側面が傾斜していない半導体発光素子における経路である（図７Ａ参照）。図１０に点線で示した経路３は、側面が傾斜していないときに、活性層２２の点２７から放射される光子が側面で反射されコンタクト３１によって吸収されることを示している。しかしながら、図１０に実線で示した経路４は、傾斜させた発光デバイス内で光源２７から同じ方向に放射された光子がフレネルレンズ２８の方向へ反射され、発光デバイスから取り出されることを示している。このように側面を傾斜させると、傾斜させない場合に発光デバイスからは取り出せない光子のいくらかを取出面へ向けることによって、光の取出効率が改善される。さらに吸収を少なくするために傾斜させた側面を金属（例えば銀）又は誘電体などの反射材４０でコーティングすれば、光の取出率はさらに改善される。

【００２９】図１１は、活性層２２の断面領域がフレネルレンズ２８の断面領域よりも小さい半導体発光素子１００を含む発光デバイスを示している。ここで断面領域は、半導体発光素子１００の異なる層の境界に平行な面内にある。活性層の縁部からの電流を遮断するために、開口部又は保護リングを用いることができる。あるいは、活性層２２の縁部からの電流を遮断し又は縁部から離れるように電流を流すために、イオンの注入又は拡散を用いることができる。パターン化ウェハボンディング及びパターン化エピタキシャル成長とも呼ばれる選択領域成長（selective area growth）及び選択領域ボンディング（selective area bonding）は、光放射を閉じ込めるための二つのさらに別の方法である。選択領域成長及び選択領域ボンディングについては、米国特許第５，７９３，０６２号において議論されており、その内容は参考としてここに援用する。さらに、活性層２２の縁部に酸化物を形成して不活性化することによって、制限放射スポット（confined-emission spot）ＬＥＤを作ることができる。その一つを図１１に示した制限放射スポットＬＥＤは、ホロニアクプロセス（Holonyak process）

を用いて作ることができる。ホロニアクプロセスでは、ＬＥＤを３時間まで３７５℃と５５０℃の間の温度にすることによって、メサ（mesa）３３を形成する必要がある。ホロニアクプロセスは不要なアルミニウム酸化物の形成を防ぐために実行されるが、このプロセスにおいて制限層２３の上部には電気的絶縁性の天然の酸化物３４が形成される。ホロニアクプロセスの詳細及びその応用については、Nick Holonyak, Jr.らに付与された「AlGaAs Native Oxide」と題する米国特許第５，２６２，３６０号及びNick Holonyak, Jr.らに付与された「Semiconductor Devices Fabricated with Passivated High-Aluminum III-V Material」と題された米国特許第５，５１７，０３９号を参照することができる。これらの両特許の内容は、参考としてここに援用する。

【００３０】図１１に示した制限放射スポットＬＥＤにおいて、最上層２４は、アルミニウムを含んだｐ型の導電層とすることができる（ただしこれには限定されない）。メサ３３は、アルミニウムを含んだ透明なｐ型層とすることができる。最上層２４の体積酸化速度、あるいは特定のＬＥＤ１００が別個の最上層２４を持たない場合には上部制限層２３の体積酸化速度よりも、導電層の横方向の酸化速度の方が速くなるように、導電層（これは、例えば高アルミニウム濃度のIII-V半導体からなる）の組成として高いモル比を有するものを選択する。図１１は、アルミニウムを含む層を露出させたＬＥＤデバイスを示している。アルミニウムを含む層の異方性酸化は、メサ３３及び天然の酸化物３４を形成させる。天然の酸化物３４の絶縁特性は、電流をこれらの領域に制限し、これによって制限放射スポットＬＥＤが得られる。この例におけるアルミニウムを含むｐ型導電層である最上層２４及びメサ３３は、酸化速度においてそれぞれに適切な異方性を有する、アルミニウムを含む任意の透明な化合物から形成することができる。

【００３１】図１２及び図１３は、二つの光学エレメント２８，２９を含む本発明の実施例を示しており、二つの光学エレメントのうちの一方には反射材４０がコーティングされて反射部を形成している。図１２は、フレネルレンズ２８を有する表面とは反対の側に設けられた反射部２９としての光学エレメント２９を示している。フレネルレンズ２８と反射部２９の両方のグルーブは、入射光線をコリメートするようになパターンとされている。したがって、光源２７から放射された光子が破線で示した経路に沿って進んで反射部２９に当たると、反射部２９は、光子をコリメートして反射して上のフレネルレンズ２８の方向へ戻す。反射部２９がないと、点光源２７から放射された光子は、図７Ａに示した経路５に沿って進み、発光デバイスからは出られない。経路５に沿った光子は内部で何度も反射され、吸収され、減衰され、あるいは取出面ではない面から取り出される。

【００３２】図１３は、図１２と同様に、発光デバイスの一つの表面上のフレネルレンズ２８と、反対側の表面の反射部２９を示している。しかし、図１３の反射部２９のグルーブは、図１２のように入射した光子をコリメートするのではなく、代わりに点光源２７上にフォーカスする。図１３の発光デバイスは、図１２では経路６に沿って進んだであろう光子を、図１３の経路７に沿って進ませることによって、軸に沿って取り出される光の強度を高める。図１３の反射部２９は、距離δ、反射部２９の水平位置、グルーブのパターンのうちの一又は二以上を調整することによって、入射した光子をフレネルレンズ２８に向かって戻るようコリメートし、フォーカスし、発散させ、あるいは導くように作ることができる。同様に、光子を、ＬＥＤ内の吸収領域、例えば活性層２２、コンタクト３１及び３２から離れるように導くことができる。この分野の当業者であれば、フレネルレンズを設計し、所望の放射パターンを特定の応用目的に適合するように仕立てることができるだろう。例えば、図１３の実施例は、軸に沿った高い強度を必要とする応用目的については、図１２の実施例よりも好ましい。

【００３３】図１４及び図１５に示した例では、本発明は、取出面に光学エレメントを必要としない。点光源２７から放射された光子は、図１４ではフォーカスされ、図１５では発散される。いずれの場合も、光子は取出面に向かって上向きに反射される。図１４の実施例は図１３の実施例のように軸に沿った強度が高くなり、例えば光ファイバーへの応用といった軸に沿った高い強度を必要とする応用目的に有用である。

【００３４】図１６は、フリップチップ構造を用いた発光デバイスを示している。フリップチップ構造では、コンタクト３１と３２を同じ側、この場合の例では底面側に配置することができる。コンタクト３１及び３２はしばしば光を吸収するものであり、また光取出面の一部を占めることになるので、これらを光取出面から無くすことによって、より多くの光を取出面を通してＬＥＤデバイスから取り出すことができる。

【００３５】図１７は、封止層２１，２３及び活性層２２の向きが、取出面に対して実質的に垂直である発光デバイスを示している。図１７に示した発光デバイスは、図１の半導体発光素子１００を９０度回転させて光が半導体発光素子１００の側面から取り出されるようにしたものである。フリップチップ構造と同様に、図１７に示した構造は、取出面にコンタクトがないという点が有利である。

【００３６】本発明のＬＥＤを多数一緒にして、高出力の応用に用いることができる。例えば図１８は、図１３に示したタイプの発光デバイス三つをアレー状に配置して、高い光出力を発するようにしたものである。ＬＥＤチップ上又はウェハー上に形成することができるこれらのダイオードアレーは、通常、単一の半導体発光素子のチップに比べてより大きい面積を有する。また、本発明

のＬＥＤデバイスは、赤、緑、青のＬＥＤをピクセルエレメントとして用いるカラーディスプレーパネルに適している。このようなディスプレーは周知であり、この例を図１９に示した。ディスプレーパネル５０は、赤（５２）、緑（５４）、青（５６）のＬＥＤをそれぞれ含み、これらを周知の回路によって選択的に光らせることによって画像を表示させる発光デバイスのアレーを有している。図１９では簡単のために三つのピクセルだけを示している。一つの実施例として、発光デバイスをカラム状に配置した。他の実施例として、発光デバイスを別のパターン、例えば三角形などに配置することもできる。高い光取出率を有する発光デバイスを、ＬＣＤディスプレーのバックライト用に使用することもできる。

【００３７】本発明について、特定の実施例を挙げて例示したが、本発明の範囲を、例示したこれらの特定のあるいは好適な実施例に限定することを意図するものではない。例えば、光検出器や太陽電池などのデバイスについて、ここに開示した実施例は有益なものとなろう。

【図面の簡単な説明】

【図１】従来からの半導体発光素子の概略図である。

【図２Ａ】光を収束するよう設計された、高さの異なるグルーブを一様な間隔で設けたフレネルレンズの平面図である。

【図２Ｂ】収束レンズと図２Ａのフレネルレンズの断面を示した図である。

【図３Ａ】光を発散するよう設計された、高さの異なるグルーブを一様な間隔で設けたフレネルレンズの平面図である。

【図３Ｂ】発散レンズと図３Ａのフレネルレンズの断面を示した図である。

【図４Ａ】一様な高さのグルーブを有し、グルーブ間の間隔をレンズ中心からの距離の関数とした、収束フレネルレンズの平面図である。

【図４Ｂ】収束レンズと図４Ａのフレネルレンズの断面を示した図である。

【図５Ａ】一様な高さのグルーブを有し、グルーブ間の間隔をレンズ中心からの距離の関数とした、発散フレネルレンズの平面図である。

【図５Ｂ】発散レンズと図５Ａのフレネルレンズの断面を示した図である。

【図６】レンズ中心について同心でないグルーブを有するフレネルレンズの平面図である。

【図７Ａ】本発明に基づいて一つの取出面上に光をコリメートするフレネルレンズが形成された発光デバイスの概略図である。

【図７Ｂ】本発明に基づいて取出面上に光をフォーカスするフレネルレンズが形成された発光デバイスの概略図である。

【図７Ｃ】本発明に基づいて取出面上に光を発散するフレネルレンズが形成された発光デバイスの概略図である。

【図８Ａ】表面が光学エレメントに形作られた発光デバイスの概略図である。

【図８Ｂ】本発明で用いることができるホログラフィックディフューザの面の平面図である。

【図９】スタンピングプロセス及びウェハーボンディングプロセスを統合する典型的な例を示した概略図である。

【図１０】表面にフレネルレンズを形成した、傾斜した側面を有するＬＥＤの概略図である。

【図１１】異方性を持つ天然の酸化物を形成した制限放射スポットＬＥＤ上に形成されたフレネルレンズの概略図である。

【図１２】半導体発光素子の対向する二つの面に光をコリメートするフレネルレンズを形成し、一方を反射材でコーティングした発光デバイスの概略図である。

【図１３】半導体発光素子の対向する二つの面にフレネルレンズを形成し、反射材をコーティングしたレンズが光を活性層にフォーカスするようにした発光デバイスの概略図である。

【図１４】軸に沿った強度を高めるために、半導体発光素子の取出面ではない面に形成された、光をフォーカスするフレネルレンズの概略図である。

【図１５】半導体発光素子の取出面ではない面に形成され、反射材でコーティングされた、光を発散するフレネルレンズの概略図である。

【図１６】フリップチップ構造の発光デバイスの概略図である。

【図１７】実質的にフレネルレンズに垂直な活性層を有する発光デバイスの概略図である。

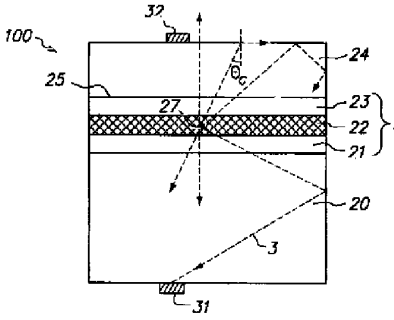
【図１８】単一のサブストレート上のダイオードアレーの概略図である。

【図１９】本発明に基づいた、発光デバイスが組み込まれたディスプレーデバイスの概略図である。

【符号の説明】

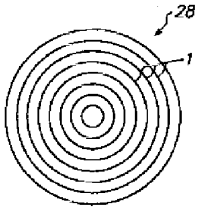
２０…サブストレート、２１…下部封止層、２２…活性層、２３…上部封止層、２４…最上層、２６…多層構造、２７…光源、２８…フレネルレンズ、３１，３２…コンタクト、３３…メサ、３４…酸化物、４０…反射材、７０…スタンピングブロック、１００…半導体発光素子、５０…ディスプレーパネル、５２…赤色ＬＥＤ、５４…緑色ＬＥＤ、５６…青色ＬＥＤ

【図1】

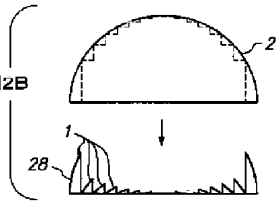


（従来技術）

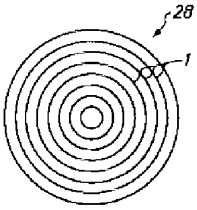
【図2A】



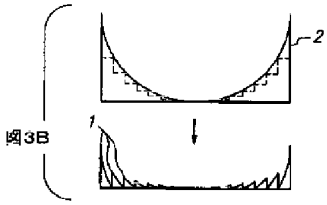
【図2B】



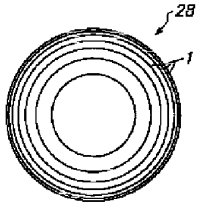
【図3A】



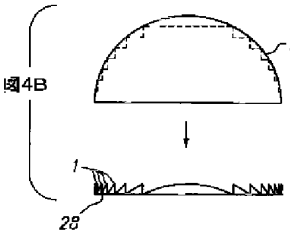
【図3B】



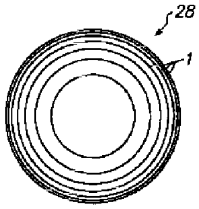
【図4A】



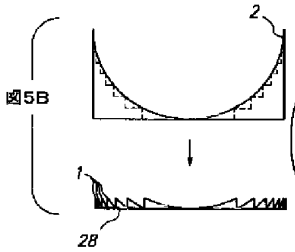
【図4B】



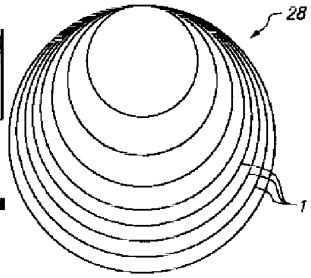
【図5A】



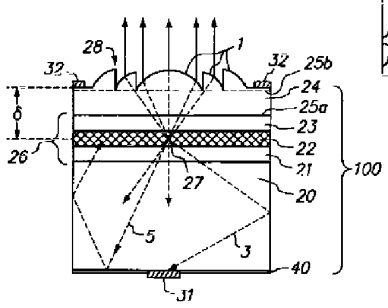
【図5B】



【図6】



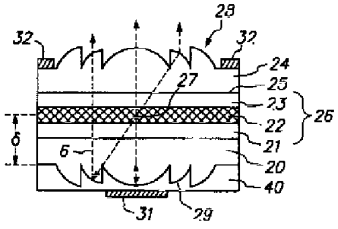
【図7A】



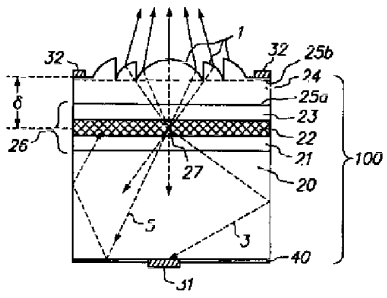
【図8B】



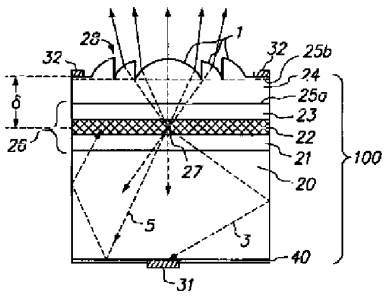
【図12】



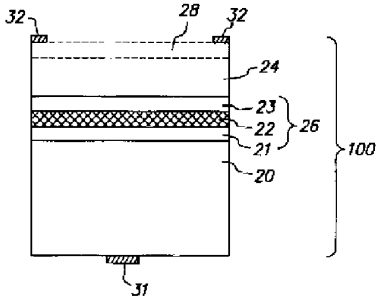
【図7B】



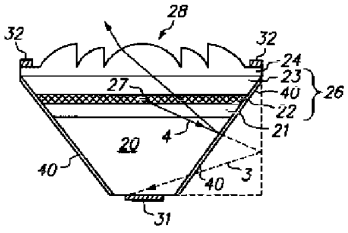
【図7C】



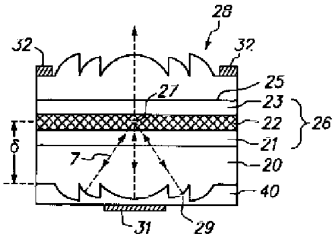
【図8A】



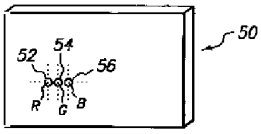
【図10】



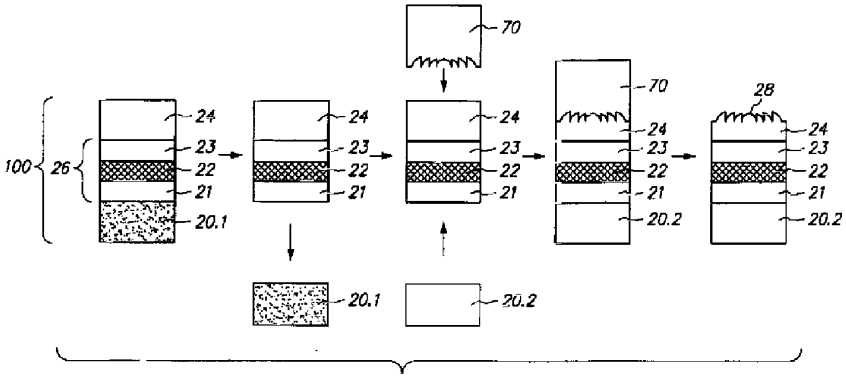
【図13】



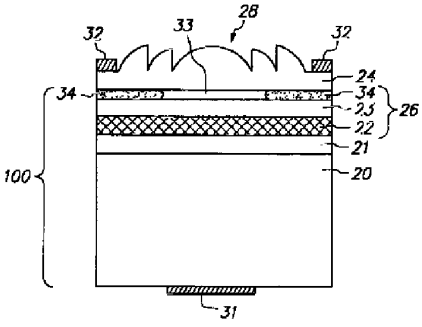
【図19】



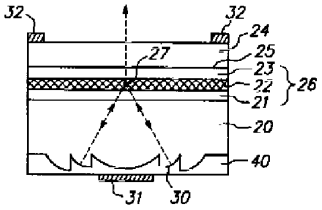
【図9】



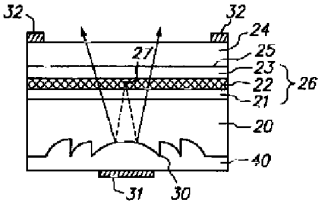
【図11】



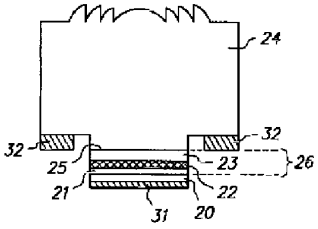
【図14】



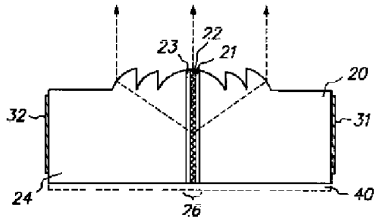
【図15】



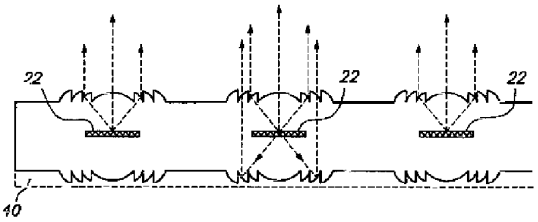
【図16】



【図１７】



【図１８】



フロントページの続き

(72)発明者　マイケル　ディー　キャムラス
アメリカ合衆国　カリフォルニア州　94087　サニーヴェイル　ピピン　アヴェニュー　890
(72)発明者　グロリア　イー　ホフラー
アメリカ合衆国　カリフォルニア州　94087　サニーヴェイル　カンバーランド　ドライヴ　863

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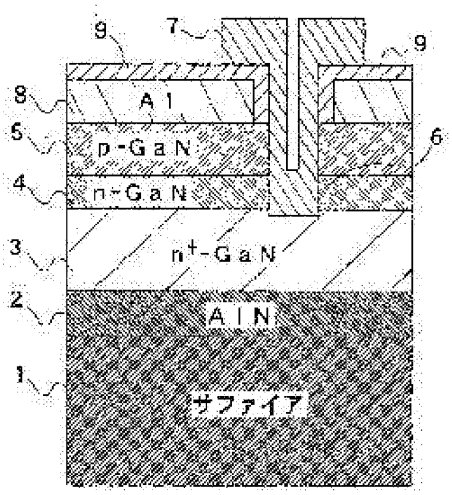
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(71)Applicant : MATSUSHITA ELECTRIC WORKS LTD
(72)Inventor : YASUIKE NORIYUKI
TAKAKURA NOBUYUKI
YASUDA MASAHARU
KUZUHARA KAZUNARI
AKEDA TAKANORI

(54) SEMICONDUCTOR LIGHT EMITTING DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a semiconductor light emitting device which can be improved in emission efficiency per unit power.
SOLUTION: The semiconductor light emitting device comprises a support substrate 1, a semiconductor layer 3 of a first conductivity type, an active layer 4 which is a light emitting layer, and a semiconductor layer 5 of a second conductivity type, all of which are stacked in this order. In the semiconductor light emitting device, a trench 6 is formed which is extended from the semiconductor layer 5 of the second conductivity type through the active layer 4 and reaches the semiconductor layer 3 of the first conductivity type. A first electrode 7 is formed in the trench 6 while a second electrode 8 is formed on the semiconductor layer 5 of the second conductivity type. At least, on a facing surface of the first electrode 7 and the second electrode 8, an insulation section 9 is formed.



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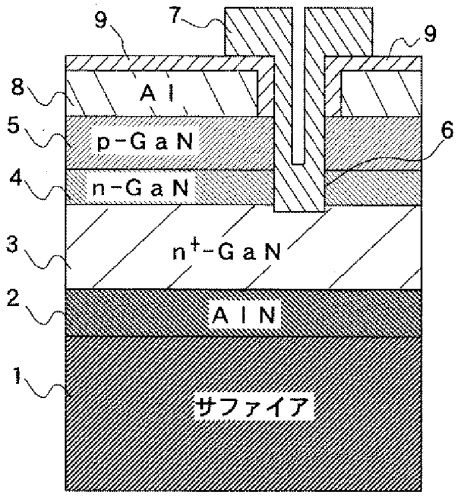
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(71)出願人　000005832
松下電工株式会社
大阪府門真市大字門真１０４８番地
(72)発明者　安池　則之
大阪府門真市大字門真１０４８番地松下電工株式会社内
(72)発明者　高倉　信之
大阪府門真市大字門真１０４８番地松下電工株式会社内
(72)発明者　安田　正治
大阪府門真市大字門真１０４８番地松下電工株式会社内
(72)発明者　葛原　一功
大阪府門真市大字門真１０４８番地松下電工株式会社内

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(54)【発明の名称】半導体発光素子

(57)【要約】
【課題】単位電力あたりの発光効率が向上するような半導体発光素子を提供する。
【解決手段】本発明に係る半導体発光素子は、支持基板１と、第１導電型半導体層３と、発光層である活性層４と、第２導電型半導体層５とを順次積層して備えた半導体発光素子であって、第２導電型半導体層５より活性層４を貫通し第１導電型半導体層３に至る溝部６を備え、溝部６に第１電極７を設け、第２導電型半導体層５に第２電極８を設けるとともに、少なくとも、第１電極７と第２電極８との対向面に絶縁部９を備える。
【選択図】　図１



【特許請求の範囲】
【請求項1】
支持基板と、第１導電型半導体層と、発光層である活性層と、第２導電型半導体層とを順次積層して備えた半導体発光素子であって、
前記第２導電型半導体層より前記活性層を貫通し前記第１導電型半導体層に至る溝部を備え、
該溝部に第１電極を設け、前記第２導電型半導体層に第２電極を設けるとともに、
少なくとも、前記第１電極と前記第２電極との対向面に絶縁部を設けたことを特徴とする半導体発光素子。
【請求項2】
前記絶縁部を、少なくとも前記溝部の側面を覆うように設けた請求項１記載の半導体発光素子。
【請求項3】
前記溝部が、平面視においてクシ歯状である請求項１又は請求項２に記載の半導体発光素子。
【請求項4】
前記第１電極及び前記第２電極を構成する材料が、透光性を有する請求項１乃至請求項３のいずれかに記載の半導体発光素子。
【請求項5】
前記絶縁部は、表面に凹凸部を備えた請求項４に記載の半導体発光素子。

【発明の詳細な説明】
【０００１】
【発明の属する技術分野】
本発明は、半導体発光素子に関し、特に発光層に電圧印加するための電極をそれぞれ支持基板の同一面側において形成した構造を有する半導体発光素子に関するものである。
【０００２】
【従来の技術】
従来の半導体発光素子としては、例えば、図５に示すように、支持基板１であるサファイア基板の上に、バッファ層２であるＡｌＮと、ｎ型窒化ガリウム系化合物半導体からなるｎ層３と、発光層であり活性層である低キャリア濃度ｎ層４であるｎ－ＧａＮと、ｐ型窒化ガリウム系化合物半導体からなるｐ層５と、ｐ層５の上面からｎ層３に至るまで形成された溝５０と、ｐ層５の上面からｎ層３に至るまで形成された孔６０と、孔６０にｎ層３と接合しｐ層５の上面にまで形成された第１電極７と、ｐ層５の上面に溝５０によって第１電極７と電気的に絶縁分離されるように形成された第２電極８とを備えたものを挙げることができる（特許文献１参照。）。
【０００３】
上述の半導体発光素子は、溝５０により第１電極７と第２電極８との電気的な絶縁分離を実現しているので、半導体発光素子を順方向バイアスにする、つまり、第２電極８をプラス電圧にし第１電極７をマイナス電圧に印加することにより、第２電極８から第１電極７に向かって電流が流れ、ｐ層５とｎ層３の界面に位置する低キャリア濃度ｎ層４にてホールと電子が結合し発光する。
【０００４】
【特許文献１】
特許第２６９６０９５号公報
【０００５】
【発明が解決しようとする課題】
上述のような半導体発光素子においては、前述の溝により第１電極と第２電極との間の電気的な絶縁分離を実現されているため、溝を形成する分だけ、半導体発光素子全体に占める活性層の面積が制約を受けてしまい、単位電力あたりの発光効率が低下するという問題点があった。

【０００６】
本発明は上記問題点を改善するためになされたものであり、単位電力あたりの発光効率が向上するような半導体発光素子を提供することを目的とするものである。
【０００７】
【課題を解決するための手段】
上述の目的を達成するために、本発明の請求項１に係る半導体発光素子は、支持基板と、第１導電型半導体層と、発光層である活性層と、第２導電型半導体層とを順次積層して備えた半導体発光素子であって、前記第２導電型半導体層より前記活性層を貫通し前記第１導電型半導体層に至る溝部を備え、該溝部に第１電極を設け、前記第２導電型半導体層に第２電極を設けるとともに、少なくとも、前記第１電極と前記第２電極との対向面に絶縁部を設けている。
【０００８】
このような構成の半導体発光素子は、少なくとも前記第１電極と前記第２電極との対向面に前記絶縁部を設けることで、半導体発光素子全体に占める前記活性層の面積割合を大きくすることができ、単位電力あたりの発光効率が向上する。
【０００９】
また、本発明の請求項２に係る半導体発光素子は、請求項１に記載の半導体発光素子において、少なくとも前記溝部の側面を覆うように設けている。
【００１０】
このような構成の半導体発光素子は、少なくとも前記溝部の側面を覆うことで、前記第２電極から前記第１電極に向けて流れる漏れ電流の経路となりうる前記溝部の側面、つまり、前記溝部の前記活性層側及び前記第２導電型半導体層側に対して少なくとも前記絶縁部を形成して、漏れ電流の影響を取り除くことで、更に単位電力あたりの発光効率が向上する。
【００１１】
また、本発明の請求項３に係る半導体発光素子は、請求項１又は請求項２に記載の半導体発光素子において、前記溝部が平面視においてクシ歯状である。
【００１２】
このような構成の半導体発光素子は、溝部が平面視においてクシ歯状に形成することで、発光に寄与する活性層を流れる電流の均一化がされるので、更に単位電力あたりの発光効率が向上する。
【００１３】
また、本発明の請求項４に係る半導体発光素子は、請求項１乃至請求項３のいずれかに記載の半導体発光素子において、前記第１電極及び前記第２電極を構成する材料が透光性を有する。
【００１４】
このような構成の半導体発光素子は、第１電極及び第２電極を構成する材料が透光性を有することで、活性層より生じる光を半導体発光素子表面（上面）からも取り出せるようになるので、更に単位電力あたりの発光効率が向上する。
【００１５】
また、本発明の請求項５に係る半導体発光素子は、請求項４に記載の半導体発光素子において、前記絶縁部は、表面に凹凸部を備えている。
【００１６】
このような構成の半導体発光素子は、絶縁部が表面に凹凸部を備えることで、絶縁部の表面で全反射する光量が低減できるため、半導体発光素子表面（上面）からの光の取り出し効率が更に向上する。
【００１７】
【発明の実施の形態】
本発明の第１実施形態を図１、図２に基づいて説明する。図１は、本発明の第１実施形態に係る半導体発光素子を示す概略断面図であり、図２は、第１実施形態に係る半導体発光

素子の変形例を示す概略断面図である。

【００１８】

第１実施形態においては、半導体発光素子は、図１に示すように、支持基板１と、バッファ層２と、第１導電型半導体である第１導電型クラッド層３と、第１導電型クラッド層３と後述の第２導電型クラッド層５とに挟まれた発光半導体層であり低キャリア濃度ｎ層である活性層４と、第２導電型半導体である第２導電型クラッド層５とが順次積層された構成であり、第２導電型クラッド層５より活性層４を貫通し第１導電型クラッド層３に至る溝部６と、Ａｌで形成された第１電極７と、Ａｌで形成された第２電極８と、絶縁部９とを備えた構成である。

【００１９】

なお、半導体発光素子の上下方向は、実際の使用状態での方位性に依存するため一義的に規定できないが、第１実施形態の記述では説明の便宜上、図１、図２に示すように、支持基板１の配置側を下（下面）側、第２導電型クラッド層５の配置側を上（上面）側というように上下方向を規定するものとする。

【００２０】

ここで、第２電極８は、第２導電型クラッド層５の上面に接続されるように形成され、第２電極８の上面及び第２電極８の溝部６側の側面には、絶縁部９を備えている。つまり、第１実施形態においては、絶縁部９は、第１電極７と第２電極８とが直接的に面する対向面に形成されている。

【００２１】

また、第１電極７は、溝部６に対して、第１導電型クラッド層３の表面が露出した露出領域に接続され、この露出領域から第２電極８の側面に設けた絶縁部９、第２電極８の上面の一部にわたり形成されている。なお、絶縁部９は、第１電極７と第２電極８との間の電気的な絶縁分離を行うために、第１電極７と第２電極８との間に少なくとも設けられていればよい。

【００２２】

ここで、支持基板１は、例えば絶縁性のサファイア基板であり、第１導電型クラッド層３は、例えばｎ型ＡｌＧａＮのようなｎ型ＧａＮよりなる高キャリア濃度ｎ＋層であり、活性層４は、例えばｎ型ＩｎＧａＮのような３族窒化物半導体を用いて形成されたものである。また、第２導電型クラッド層５は、例えばｐ型ＡｌＧａＮのようなｐ型ＧａＮよりなる高キャリア濃度ｎ＋層であり、絶縁部９は、例えば絶縁膜であり、その材料は例えば、透明性を有しているSiO_2を用いる。なお、絶縁部９は、絶縁性を備えており、更に好ましくは透明性を有するものがであればよい。

【００２３】

また、バッファ層２は支持基板１と第１導電型クラッド層３との格子不整合を緩和するために設けられるもので、例えばＡｌＮ、ＧａＮ、ＡｌＧａＮにより形成される。なお、活性層４をｎ型ＩｎＧａＮで形成する場合には、活性層４の発光色は、Ｉｎの組成比を適宜調整したり、あるいはＳｉ、Ｇｅ、Ｓ等のｎ型不純物やＺｎ、Ｍｇ等のｐ型不純物を適宜ドープすることにより、紫外～赤色の範囲で所望の色に調節可能である。

【００２４】

なお、第１導電型クラッド層３の露出領域は、例えば第１導電型クラッド層３の全面に活性層４及び第２導電型クラッド層５を積層形成した後、活性層４及び第２導電型クラッド層５のうち露出領域相当箇所上部に積層されている部分を第１導電型クラッド層３が露出するまでエッチング除去することで形成することができる。なお、溝部６は、この第１導電型クラッド層３の露出領域を含み、活性層４、第２導電型クラッド層５のエッチング除去された箇所で構成されている。

【００２５】

第２電極８は、第２導電型クラッド層５の上に、後に第２電極８の側面に設ける絶縁部９相当箇所を考慮し、溝部６を取り囲むように形成される。そして、第２電極８の上面及び第２電極８の溝部６側の側面には、絶縁部９が形成される。

【００２６】
その後、第１導電型クラッド層３の露出領域から活性層４、第２導電型クラッド層５、第２電極８の溝部６側の側面に設けた絶縁部９、第２電極８の上面に設けた絶縁部９の一部にわたって、第１導電型クラッド層３に接続した第１電極７が形成される。
【００２７】
第１電極７及び第２電極８は、例えば所定のマスクを用いて形成することができるもので、両電極の材料としてはＡｌの他に、例えばＮｉ、Ａｕ、Ｔｉ等の金属を使用することができる。
【００２８】
なお、第１実施形態においても、半導体発光素子は、順方向バイアス、すなわちｐ型である第２導電型クラッド層５に形成した第２電極８にプラス電圧にし、第１電極７をマイナス電圧に印加することにより、活性層４にてホールと電子が結合し発光する。
【００２９】
かかる半導体発光素子においては、少なくとも、第１電極７と第２電極８との対向面に絶縁部９を設けることで、従来のように、第１電極７と第２電極８とを電気的に絶縁分離するための溝を形成する必要はなくなるので、半導体発光素子全体に占める活性層４の面積割合を大きくすることができ、単位電力あたりの発光効率が向上する。
【００３０】
ここで、第１実施形態における変形例として、第１電極７及び第２電極８の材料として、透光性を有する透明電極を用いてもよい。透明電極の材料としては、例えば、In_2O_3とSnO_2の複合化合物であるＩＴＯや、Cd_2SnO_4を用いることができる。
【００３１】
この場合、第１の電極７及び第２電極８に透明電極を用いることで、活性層４より生じる光を半導体発光素子表面（上面）からも取り出せるようにすることで、更に単位電力あたりの発光効率が向上する。また、半導体発光素子の両面、つまり、表面（上面）と裏面（下面）から光の取り出しが可能なフリップチップ実装との組み合わせにおいては、単位電力あたりの発光効率が向上する。
【００３２】
また、第１電極７及び第２電極８の材料として、透光性を有する透明電極を用いた場合に、図２に示すように、半導体発光素子の絶縁部９の表面に凹凸部９１設けた構成であってもよい。なお、凹凸部９１は、例えば、サンドブラスト法で形成することができる。なお、図２において、光の取り出しの様子は矢印で示している。
【００３３】
この場合、絶縁部９の表面に凹凸部９１設けることで、絶縁部９表面での全反射が抑制されるので、半導体発光素子表面（上面）からの光の取り出し効率が更に向上する。
【００３４】
なお、第１実施形態及びその変形例においては、漏れ電流の経路となる可能性がある活性層４及び第２導電型クラッド層５は、例えば数μｍレベルと非常に薄く、ハイインピーダンス状態となるため、第２電極８から第１電極７に向けて漏れ電流は、活性層４を流れる電流に比べ、ほとんどの場合において、無視できるレベルに制限される。
【００３５】
次に、第１実施形態における絶縁部９の形成箇所の変形例を示した実施形態を、本発明の第２実施形態として図３に基づいて説明する。図３は、本発明の第２実施形態に係る半導体発光素子を示す概略断面図である。なお、第１実施形態との同一箇所には同一符号を付して、共通部分の説明は省略する。
【００３６】
第２実施形態においては、半導体発光素子は、図３に示すように、絶縁部９が溝部６にける第１導電型クラッド層３の露出領域の一部まで拡大された構成であり、この点が、第１電極７と第２電極８とが直接的に面する対向面に絶縁部９を形成した第１実施形態の構成と異なる点である。

【００３７】
第２実施形態においては、絶縁部９は、溝部６の側面及び第１導電型クラッド層３の露出領域の一部まで形成されているが、少なくとも溝部６の側面を覆うように形成されていればよい。
【００３８】
かかる半導体発光素子においては、第２電極８から第１電極７に向けて流れる漏れ電流の経路となりうる溝部６の側面、つまり、溝部６の活性層４側及び第２導電型クラッド層５側に対して、少なくとも絶縁部９を形成して漏れ電流の影響を取り除くことで、単位電力あたりの発光効率が向上する。
【００３９】
次に、第１実施形態における溝部６をクシ歯状に形成した実施形態を、本発明の第３実施形態として図４に基づいて説明する。図４は、本発明の第３実施形態に係る半導体発光素子を示す平面図及び概略断面図である（図４（ａ）は、平面図であり、図４（ｂ）は、図４（ａ）のＸ－Ｘ断面における概略断面図であり、図４（ａ）においては、平面視における絶縁部９の段差部の図示は省略している）。なお、第１実施形態との同一箇所には同一符号を付して、共通部分の説明は省略する。
【００４０】
第３実施形態においては、半導体発光素子は、図４に示すように、平面視において例えば５つのクシ歯状になるように各溝部６を備え、その各溝部６に第１電極７を設けた構成である。なお、各第１電極７は、第１電極７と一体形成されたＡｌからなるクシ芯部７１により各々電気的に接続されている。
【００４１】
かかる半導体発光素子においては、溝部６を平面視においてクシ歯状に形成したすることにより、発光に寄与する活性層４を流れる電流が均一化されるため、更に単位電力あたりの発光効率が向上する。
【００４２】
ここで、第２実施形態における溝部６をクシ歯状に形成しても勿論よい。この場合も、同様に、活性層４を流れる電流が均一化されるため、更に単位電力あたりの発光効率が向上する。また、第２実施形態及び第３実施形態において、第１実施形態における変形例に示したように、第１電極７及び第２電極８の材料として、透光性を有する透明電極を用いてもよいし、更に絶縁部９の表面に凹凸部を設けた構成であってもよい。
【００４３】
【発明の効果】
以上説明したように、本発明の請求項１に係る半導体発光素子は、第２導電型半導体層より活性層を貫通し第１導電型半導体層に至る溝部に第１電極を設け、第２導電型半導体層に第２電極を設けるとともに、少なくとも、第１電極と第２電極との対向面に絶縁部を設けることで、半導体発光素子全体に占める活性層の面積割合を大きくすることができ、単位電力あたりの発光効率が向上する。
【００４４】
また、本発明の請求項２に係る半導体発光素子は、請求項１に記載の半導体発光素子の効果に加えて、第２電極から第１電極に向けて流れる漏れ電流の経路となりうる溝部の側面、つまり、溝部の活性層側及び第２導電型半導体層側に対して少なくとも絶縁部を形成して、漏れ電流の影響を取り除くことで、更に単位電力あたりの発光効率が向上する。
【００４５】
また、本発明の請求項３に係る半導体発光素子は、請求項１又は請求項２に記載の半導体発光素子の効果に加えて、溝部が平面視においてクシ歯状であることで、発光に寄与する活性層を流れる電流の均一化がされるので、更に単位電力あたりの発光効率が向上する。
【００４６】
また、本発明の請求項４に係る半導体発光素子は、請求項１乃至請求項３のいずれかに記載の半導体発光素子の効果に加えて、第１電極及び第２電極を構成する材料が透光性を有

することで、活性層より生じる光を半導体発光素子表面（上面）からも取り出せるようになるので、更に単位電力あたりの発光効率が向上する。また、半導体発光素子の両面、つまり、表面（上面）と裏面（下面）から光の取り出しが可能なフリップチップ実装との組み合わせにおいては、単位電力あたりの発光効率が向上する。

【００４７】

また、本発明の請求項５に係る半導体発光素子は、請求項４に記載の半導体発光素子の効果に加えて、絶縁部は、表面に凹凸部を備えることで、絶縁部の表面で全反射する光量が低減できるため、半導体発光素子表面（上面）からの光の取り出し効率が更に向上する。

【図面の簡単な説明】

【図１】本発明の第１実施形態に係る半導体発光素子を示す概略断面図である。

【図２】本発明の第１実施形態に係る半導体発光素子の変形例を示す概略断面図である。

【図３】本発明の第２実施形態に係る半導体発光素子を示す概略断面図である。

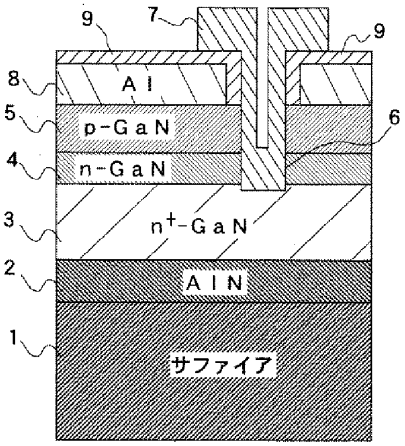
【図４】本発明の第３実施形態に係る半導体発光素子を示す平面図及び概略断面図である。

【図５】従来例に係る半導体発光素子を示す概略断面図である。

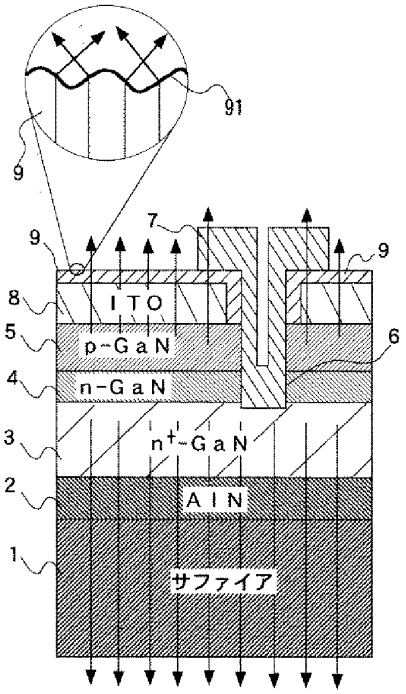
【符号の説明】

１　支持基板
２　バッファ層
３　第１導電型クラッド層
４　活性層
５　第２導電型クラッド層
６　溝部
７　第１電極
８　第２電極
９　絶縁部
９１　凹凸部

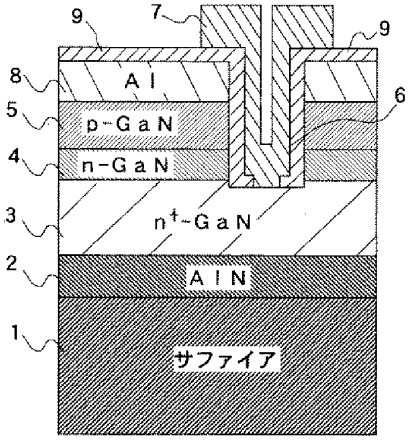
【図1】


9
7
9
8
Al
5
p-GaN
6
4
n-GaN
3
n+-GaN
2
AlN
1
サファイア

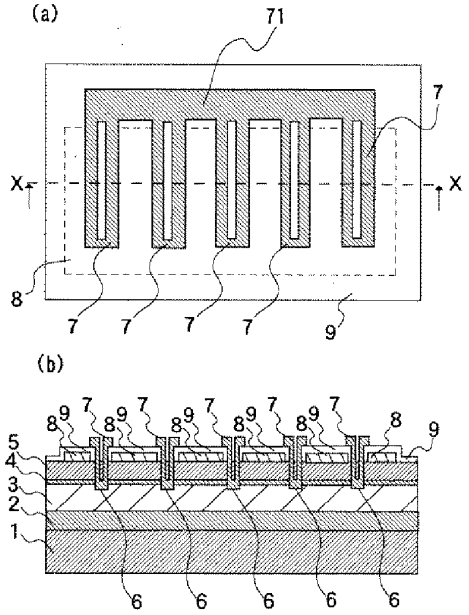
【図2】


91
9
7
9
9
8
ITO
5
p-GaN
6
4
n-GaN
3
n+-GaN
2
AlN
1
サファイア

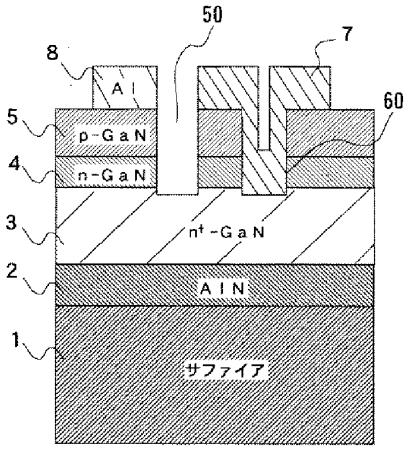
【図3】


9
7
9
8
Al
5
p-GaN
6
4
n-GaN
3
n+-GaN
2
AlN
1
サファイア

【図4】


(a)
71
7
X
X
8
7
7
7
7
9
(b)
8
9
7
5
4
3
2
1
6

【図5】



(72)発明者　明田　孝典
大阪府門真市大字門真１０４８番地松下電工株式会社内

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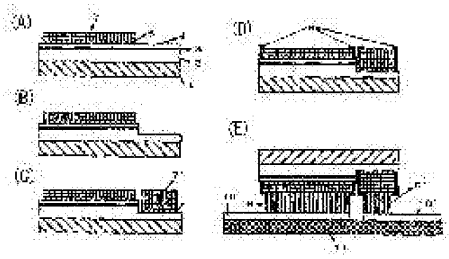
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(71)Applicant : STANLEY ELECTRIC CO LTD
(72)Inventor : TSUCHIYA MASAHIKO
HORIO TADASHI
MORIKAWA KENICHI

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(54) GALLIUM NITRIDE BASED COMPOUND SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a gallium nitride based compound semiconductor device capable of performing free process designing and having an optimum device property, and a manufacturing method of the device.
SOLUTION: As suitable materials, a Pt/Rh layer, a Pt/Ir layer or an Rh layer is used as an electrode for a p-type gallium nitride based compound semiconductor, and an Al/Rh layer, an Al/Ir layer, an Al/Pd layer or an Al/Pt layer is used as an electrode for an n-type gallium nitride based compound semiconductor. For this reason, different from any material in a conventional technology, ohmic contact can be obtained without performing annealing, and a good gallium nitride based device can be formed. Thereby, it becomes possible to perform this device process by using low heat-resistant materials. Furthermore, there can be obtained such useful effects as to avoid the deterioration of the device property caused by a thermal hysteresis of high temperature treatment and to reduce the number of processes.



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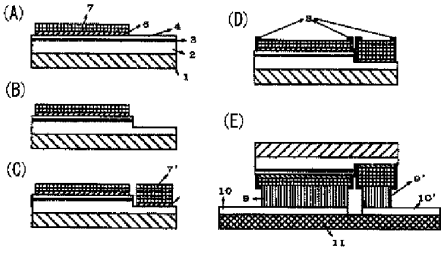
(71)出願人　000002303
スタンレー電気株式会社
東京都目黒区中目黒２丁目９番１３号
(72)発明者　土谷　正彦
東京都目黒区中目黒２丁目９番１３号　スタンレー電気株式会社内
(72)発明者　堀尾　直史
東京都目黒区中目黒２丁目９番１３号　スタンレー電気株式会社内
(72)発明者　森川　謙一
東京都目黒区中目黒２丁目９番１３号　スタンレー電気株式会社内

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最終頁に続く

(54)【発明の名称】窒化ガリウム系化合物半導体素子とその製造方法

(57)【要約】
【課題】　従来技術において、窒化ガリウム系化合物半導体上にオーミック電極を形成するためには４００℃以上のアニール処理が必須であったため、この処理によるデバイス特性の悪化やプロセス上の制約が生じていた。
【解決手段】　好適な材料としてｐ型窒化ガリウム系化合物半導体用電極としてＰｔ／Ｒｈ層，Ｐｔ／Ｉｒ層，又はＲｈ層を用い、ｎ型窒化ガリウム系化合物半導体用電極としてＡｌ／Ｒｈ層、Ａｌ／Ｉｒ層、Ａｌ／Ｐｄ層、又はＡｌ／Ｐｔ層を用いることで、従来技術にある如何なる材料とも異なり、アニール処理を行なうことなくオーミック接触を得ることができ、良好な窒化ガリウム系デバイスを形成することができる。これにより、低耐熱材料を使用して本デバイスプロセスを行なうことが可能となる。また高温処理の熱履歴によるデバイス特性の悪化の回避、工程数の削減、等有用な効果が得られる。
【選択図】　図１



【特許請求の範囲】
【請求項1】
窒化ガリウム系化合物半導体と、該窒化ガリウム系化合物半導体と接するように形成されかつオーミック接触する電極とを備えた窒化ガリウム系化合物半導体発光素子の製造方法であって、
基板上に窒化ガリウム系化合物半導体層を積層する工程と、
該窒化ガリウム系化合物半導体層の表面を露出させる工程と、
該窒化ガリウム系化合物半導体の露出表面を表面処理する工程と、
該処理表面上に窒化ガリウム系化合物半導体用電極を形成する工程を順に備え、
前記電極形成工程終了から窒化ガリウム系化合物半導体発光素子を当該素子搭載基板上に搭載する工程を行うまでの間において、オーミック接触を得るためのアニール処理を行わないことを特徴とする窒化ガリウム系化合物半導体発光素子の製造方法。
【請求項2】
前記窒化ガリウム系化合物半導体が、ｎ型窒化ガリウム系化合物半導体であることを特徴とする請求項１記載の窒化ガリウム系化合物半導体発光素子の製造方法。
【請求項3】
前記電極形成工程が、ｎ型窒化ガリウム系化合物半導体層上に厚さ１ｎｍ～１０ｎｍのＡｌ層を蒸着するサブ工程と、前記Ａｌ層上に形成されるＲｈ、Ｉｒ、Ｐｔ、Ｐｄからなる群から選択されるいずれかの金属層を蒸着するサブ工程を有し、前記オーミック接触を得るためのアニール処理を必要としないことを特徴とする請求項２に記載の窒化ガリウム系化合物半導体発光素子の製造方法。
【請求項4】
前記電極形成工程が、ｎ型窒化ガリウム系化合物半導体層上に形成される島状構造または網目状構造を有する厚さ１ｎｍ～１０ｎｍのＡｌ層を蒸着するサブ工程と、Ｒｈ、Ｉｒ、Ｐｔ、Ｐｄからなる群から選択されるいずれかの金属層を蒸着するサブ工程とを含み、サブ工程は同時にまたはＡｌ蒸着サブ工程に続いて金属蒸着サブ工程行う、前記オーミック接触を得るためのアニール処理を必要としないことを特徴とする請求項２に記載の窒化ガリウム系化合物半導体発光素子の製造方法。
【請求項5】
前記窒化ガリウム系化合物半導体が、ｐ型窒化ガリウム系化合物半導体であることを特徴とする請求項１記載の窒化ガリウム系化合物半導体発光素子の製造方法。
【請求項6】
ｐ型窒化ガリウム系化合物半導体層にオーミック接触するｐ型窒化ガリウム系化合物半導体用電極が、Ｐｄ、Ｐｔ、Ｒｈ、Ｐｔ／Ｒｈ、Ｐｔ／Ａｇ、Ｒｈ／Ａｇ、Ｐｄ／Ｒｈ、Ｐｄ／Ａｇ層からなる群から選択されるいずれかの層で構成されるとともに、前記オーミック接触を得るためのアニール処理を必要としないことを特徴とする請求項５に記載の窒化ガリウム系化合物半導体発光素子の製造方法。
【請求項7】
前記ｐ型窒化ガリウム系化合物半導体用電極がＰｔ／Ｒｈ、Ｐｔ／Ａｇのいずれかの層の場合において、前記Ｐｔ層の膜厚が０．３ｎｍ～１００ｎｍであり、及び／又は前記ＲｈもしくはＡｇ層の膜厚が５０ｎｍ～３００ｎｍであることを特徴とする請求項６に記載の窒化ガリウム系化合物半導体発光素子の製造方法。
【請求項8】
前記ｐ型窒化ガリウム系化合物半導体用電極がＰｄ，ＰｔまたはＲｈのいずれかの層の場合において、前記Ｐｄ、Ｐｔ、又はＲｈ層の膜厚が０．３ｎｍ～２００ｎｍであることを特徴とする請求項６に記載の窒化ガリウム系化合物半導体発光素子の製造方法。
【請求項9】
ｎ型窒化ガリウム系化合物半導体層およびｐ型窒化ガリウム系化合物半導体層を含むＩＩＩ族窒化物系化合物半導体積層構造と、ｎ型窒化ガリウム系化合物半導体層上に形成され

たｎ電極と、ｐ型窒化ガリウム系化合物半導体上に形成されたｐ電極とを備えたＩＩＩ族窒化物系化合物半導体発光素子であって、
　前記ｎ電極が、ｎ型窒化ガリウム系化合物半導体層と接する厚さ１ｎｍ～１０ｎｍのＡｌ層と、前記Ａｌ層上に形成されるＲｈ、Ｉｒ、Ｐｔ、Ｐｄからなる群から選択されるいずれかの金属層とからなり、アニール処理を施すことなくオーミック接触していることを特徴とするＩＩＩ族窒化物系化合物半導体発光素子。
【請求項10】
前記ｐ電極が、ｐ型窒化ガリウム系化合物半導体層と接するＰｄ、Ｐｔ、Ｒｈ、Ｐｔ／Ｒｈ、Ｐｔ／Ａｇ、Ｒｈ／Ａｇ、Ｐｄ／Ｒｈ、Ｐｄ／Ａｇ層からなる群から選択されるいずれかの層で構成され、厚みが２００ｎｍ以下であるとともに、アニール処理を施すことなくオーミック接触していることを特徴とする請求項９に記載のＩＩＩ族窒化物系化合物半導体発光素子。
【請求項11】
前記ｎ型またはｐ型窒化ガリウム系化合物半導体用電極上に、更に、共晶制限層および共晶材料層を積層してなる金属積層構造が形成されたことを特徴とする請求項９または１０に記載のＩＩＩ族窒化物系化合物半導体発光素子。
【請求項12】
前記共晶制限層は実質的にＡｇ又はＰｔで構成されており、且つ、前記共晶材料層はＡｕ，Ｓｎ，Ｉｎからなる群から選択される金属、またはこれらのうち少なくとも一つを含む合金で構成されていることを特徴とする請求項１１に記載のＩＩＩ族窒化物系化合物半導体発光素子。
【請求項13】
請求項９に記載のＩＩＩ族窒化物系化合物半導体発光素子であって、前記半導体層の側面が、前記基板の垂直方向に対して傾斜しているとともに、
　前記電極が、前記傾斜した側面に延在して形成されていることを特徴とする窒化ガリウム系化合物半導体デバイス。
【発明の詳細な説明】
【技術分野】
【0001】
　本発明は窒化ガリウム系化合物半導体を用いた素子に関する。より具体的には、窒化ガリウム系化合物半導体に最適な電極を有する素子および当該素子の製造方法（デバイスプロセス）に関する。
【背景技術】
【0002】
　従来の窒化ガリウム系化合物半導体発光素子を図６に示す。この発光素子はフリップチップ方式にて図示しない給電電極上に搭載する構成であり、電極面を下側として示している。この発光素子はサファイア基板１上にｎ型窒化ガリウム系化合物半導体層２（以後、ｎ型ＧａＮ層と記載）、活性層３、ｐ型窒化ガリウム系化合物半導体層４（以後、ｐ型ＧａＮ層と記載）がこの順で形成され、これらに対してｎ型窒化ガリウム系化合物半導体用電極５（以後、ｎ型ＧａＮ用電極と記載）と、ｐ型窒化ガリウム系化合物半導体用電極６（以後、ｐ型ＧａＮ用電極と記載）とを通じて電流を印可することで所定の波長の光を発することが可能である。ここで例示されている基板は、サファイア基板であるが、これに限定されず、ＳｉＣ基板やＳｉ基板に置き換えることができることは周知である。この基板上に、ＭＯＣＶＤ法等周知の技術により、窒化ガリウム系化合物半導体（ＡｌｘＩｎｙＧａ（１－ｘ－ｙ）Ｎ、０≦ｘ，ｙ≦１）薄膜を成膜することができる。
【0003】
　ここで、ｎ型ＧａＮ用電極５は一般にはＴｉ／Ａｌ、Ｖ／Ａｌ等の金属薄膜によって構成される。また、ｐ型ＧａＮ用電極６はＰｔ，またはＮｉ／Ａｕ等の金属薄膜によって構成されることが多い。以後、本明細書において「Ａ／Ｂ層」と表現した場合、より左に記載した材料Ａが半導体層側、より右に記載した材料Ｂが半導体層から離れた層側とする。また、フリップチップ方式で搭載する場合の光取り出し効率向上のために、ｎ型ＧａＮ用

電極５として反射率の高いＲｈ／Ａｌ層を用いてサファイア基板側において素子の発光を反射する技術や、同様にｐ型ＧａＮ用電極６として反射率の高いＲｈ／Ａｌ、Ａｇ等を用いる技術が知られている。なお図面において符号７、７で示すのは共晶電極である。

これらの従来の窒化ガリウム系化合物半導体発光素子とその製造方法については、特許文献１、特許文献２、特許文献３、特許文献４、特許文献５、特許文献６、特許文献７などが挙げられる。

【0004】

【特許文献1】特開平５－２１１３４７

【特許文献2】特開平１１－２２０１６８

【特許文献3】特開２００３－１１０１４０

【特許文献4】特開２００３－１１０１３８

【特許文献5】特開平５－２９１６２１

【特許文献6】特開２０００－３６６１９

【特許文献7】特開２０００－１８３４００

【発明の開示】

【発明が解決しようとする課題】

【0005】

特許文献１にはｉ層の窒化ガリウム系化合物半導体に接合する層をＮｉとした電極が開示されている。特許文献２にはフリップチップ型の窒化ガリウム系化合物半導体素子においてｐ型層と厚膜反射性電極層の間に薄膜金属層を設けることが開示される。特許文献３は窒化物半導体発光素子の光の取り出し効率を向上するために電極の所定の領域を高い反射率とすることを開示する。特許文献４は窒化物半導体発光ダイオードの外部量子効率を向上させるために透光性ｐ電極のシート抵抗と光の透過率との調和を図る旨を開示する。特許文献５にはｐ型不純物をドープした窒化ガリウム系化合物半導体とオーミック接触を得る材料としてＡｕ，Ｐｔ，Ａｇ，Ｎｉを使用すること、及びｎ型不純物をドープした窒化ガリウム系化合物半導体とオーミック接触を得る材料としてＡｌ，Ｃｒ，Ｔｉ，Ｉｎを使用することが開示されている。特許文献６はフリップチップ型の窒化ガリウム系化合物半導体素子においてｐ型層に接続される厚膜電極層をＡｇ，Ｒｈ，Ｒｕ，Ｐｔ，Ｐｄを用いて高反射率とすることが開示する。特許文献７にも同じくフリップチップ型の窒化ガリウム系化合物半導体素子においてｐ型層に接続される厚膜電極層を高反射率とすることが開示されている。

しかしながら、上に挙げた、従来のＧａＮ用電極は、半導体層とオーミック接触を得るために積極的なアニール処理を施さないことに関する知見は一切開示されていない。なぜならば窒化ガリウム系化合物半導体とオーミック接触を得るためにはいずれも４００℃以上のアニール処理を必要とするからである。このことは、以下のような幾つかの問題を引起す。

【0006】

（１）第１の問題点として、アニール炉における表面汚染と酸化が避けられないことが挙げられる。

【0007】

ＧａＮデバイスプロセスにおけるアニール処理の工程としてウェハに対してｉ）ｎ型ＧａＮ用電極形成－＞ アニール－＞ｐ型ＧａＮ用電極形成 －＞ アニールを順に行う工程（または、当該工程においてｐ型ＧａＮ用電極の形成とｎ型ＧａＮ用電極の形成順を逆にする）、あるいは、ｉｉ）ｎ型ＧａＮ用電極形成
－＞ ｐ型ＧａＮ用電極形成－＞アニールを順に行う工程（または、当該工程においてｐ型ＧａＮ用電極の形成とｎ型ＧａＮ用電極の形成順を逆にする）のいずれかが一般的である。

【0008】

ｉ）の工程の場合、ｎ型ＧａＮ用電極を先に形成して、オーミック接触を取るためにアニールを行うので、アニール時にはｐ型ＧａＮ用電極を形成するためのウェハ表面部分は

炉の雰囲気に直に曝されることになる。このため、この表面の炉内不純物による汚染や表面酸化が避けられず、その上にｐ型
ＧａＮ用電極を形成しても電気的特性は悪くなる。汚染や表面酸化を避けるために電極を形成するための表面を洗浄するとしても、既にｎ型ＧａＮ用電極が形成されているため、この材料が侵されるような洗浄プロセスを使うことはできず、洗浄は不完全にならざるを得ない。また、ｐ型ＧａＮ用電極を形成後にもやはりアニール処理が存在するため、ｎ型ＧａＮ用電極に余計な熱履歴を与えてしまい、結果として２回のアニール処理により電気特性が悪くなる。ｐ型ＧａＮ用電極形成を先にしてもやはり同様の問題がある。

【0009】

ｉｉ）の工程の場合、ｉ）の工程と違いアニール処理を１度で済ませるためｉ）の工程のような問題は存在しない。しかしながら、ｎ型ＧａＮ用電極またはｐ型ＧａＮ用電極のうち、温度、雰囲気、時間等のアニール条件がより過酷な条件を電極形成後のアニール処理条件として適用しなければならない。このため、より穏やかな条件で最適なオーミック特性が得られるはずの他方の電極の特性は、悪化せざるを得ない。

【0010】

ｎ型ＧａＮ用，ｐ型ＧａＮ用両電極を共通の材料と共通の条件でアニールできれば一度に蒸着とアニールとを行うことができるが、現在のところそのような材料は見つかっていない。

【0011】

例えば、ｎ型ＧａＮ用電極５が４００℃前後のアニール処理を必要とし、ｐ型ＧａＮ用電極６が７００℃前後のアニール処理を必要とする場合には、ｐ型ＧａＮ用電極６を先に形成しなければならない。なぜならｎ型ＧａＮ用電極５を先に形成した場合、同一ウェハに後から形成されたｐ型ＧａＮ用電極６のオーミック特性を得るために７００℃のアニール処理を経なければならないため、ｎ型ＧａＮ用電極５が過剰な熱を受け、電気特性が低下してしまうからである。

【0012】

（２）第２の問題点として、デバイスプロセスが制約されることが挙げられる。

【0013】

図６に示す共晶電極７、７は、Ｔｉ／Ａｕ／(Ｐｔ／Ａｕ）ｎ層やＮｉ／Ａｕ／(Ｐｔ／Ａｕ)ｎ層等の金属積層構造よりなる。共晶電極７、７'の最表面層に共晶材料層としてＡｕ層、その下に共晶制限層としてＰｔ層を用いている。これらを下にしてサブマウントや配線の側に積層したＡｕ／Ｓｎ共晶部に接続してフリップチップ接続する。接続の際には、共晶電極７、７'の最表面のＡｕ層とサブマウントの共晶部最表面のＡｕ層を接触させて３００℃程度の熱をかけることによってＡｕ／Ｓｎの共晶状態を作り出し、接合する。従って、上記のｎ型ＧａＮ用電極５を形成後に電極金属のオーミック接続を取るため４００℃以上のアニール処理を行う際に、もし成膜工程を続けて共晶電極７、７'まで成膜してしまうと、共晶用金属が融解して電極７、７'が機能しなくなってしまうことがある。故に、ｎ型ＧａＮ用，ｐ型ＧａＮ用両電極５，６を形成しアニールした後に、別工程で共晶電極７を形成しなければならない。なお、本明細書において、「（Ａ／Ｂ）ｎ層」といった表現は、材料Ａと材料Ｂとを繰り返してｎ回積層することを意味するものとする。

【0014】

一般にｎ型ＧａＮ用，ｐ型ＧａＮ用両電極とも過剰な温度によってアニールされると、半導体層側の金属層表面が荒れて反射率やオーミック特性が落ちるため好ましくない。特に、Ｐｔ，Ｒｈ，Ｐｄ等をＧａＮ系ＬＥＤ用ｐ型電極として用いた場合、熱処理によって立上り電圧（Ｖｆ）が０．０５～０．２Ｖ上昇してしまう。よって、余計なアニール処理は無い方が良い。

【0015】

このように、ウェハにかけるアニール処理の温度の高低によってデバイスプロセスの順番が決定されてしまう。あるいは、アニール処理の温度の最適化ができない。このことから必然的に、自由なデバイスプロセス設計ができない、デバイス特性を最適なものにでき

ないという問題が生じる。
本発明は、上に挙げた問題点に鑑み、自由なプロセス設計が可能であるとともに最適なデバイス特性を有する窒化ガリウム系化合物半導体素子、及びその製造方法を提供することを目的とする。
【課題を解決するための手段】
【0016】
上述の目的を達成するため、本発明は、ＧａＮ系化合物半導体デバイスプロセスにおいて、所定の積層構造電極を半導体用電極に用いることによりｎ型
ＧａＮ用電極形成、ｐ型 ＧａＮ用電極形成、共晶電極形成のいずれのプロセスにおいても積極的にアニール処理を施すことを必要としないデバイスを形成する。
本発明は、窒化ガリウム系化合物半導体と、該窒化ガリウム系化合物半導体と接するように形成されかつオーミック接触する電極とを備えた窒化ガリウム系化合物半導体発光素子の製造方法を提供するものであって、
基板上に窒化ガリウム系化合物半導体層を積層する工程と、
該窒化ガリウム系化合物半導体層の表面を露出させる工程と、
該窒化ガリウム系化合物半導体の露出表面を表面処理する工程と、
該処理表面上に窒化ガリウム系化合物半導体用電極を形成する工程を順に備え、
前記電極形成工程終了から窒化ガリウム系化合物半導体発光素子を当該素子搭載基板上に搭載する工程を行うまでの間において、オーミック接触を得るためのアニール処理を行わないことを特徴とする窒化ガリウム系化合物半導体発光素子の製造方法である（請求項１）。
ここで、窒化ガリウム系化合物半導体は、ｎ型窒化ガリウム系化合物半導体及びｐ型窒化ガリウム系化合物半導体のいずれかであることが好ましい（請求項２，５）。
ｎ型ＧａＮ半導体の場合、前記電極形成工程が、ｎ型窒化ガリウム系化合物半導体層上に厚さ１ｎｍ～１０ｎｍのＡｌ層を蒸着するサブ工程と、前記Ａｌ層上に形成されるＲｈ、Ｉｒ、Ｐｔ、Ｐｄからなる群から選択されるいずれかの金属層を蒸着するサブ工程を有することが好ましい（請求項３）。あるいは前記電極形成工程が、ｎ型窒化ガリウム系化合物半導体層上に形成される島状構造または網目状構造を有する厚さ１ｎｍ～１０ｎｍのＡｌ層を蒸着するサブ工程と、Ｒｈ、Ｉｒ、Ｐｔ、Ｐｄからなる群から選択されるいずれかの金属層を蒸着するサブ工程とを含み、サブ工程は同時にまたはＡｌ蒸着サブ工程に続いて金属蒸着サブ工程行うことが好ましい（請求項４）。
【0017】
より具体的には、好適な材料としてｐ型ＧａＮ用電極としてＰｔ／Ｒｈ層またはＰｔ／Ａｇ層を用い、ｎ型ＧａＮ用電極としてＡｌ／Ｒｈ層、Ａｌ／Ｉｒ層、Ａｌ／Ｐｄ層、又はＡｌ／Ｐｔ層を用いる。これによりアニールを行わずにＧａＮデバイスを形成することができる。これらの材料は従来技術にある如何なる材料とも違って、アニールを行わずに良好なオーミック特性を達成し得るのである。
【0018】
従来、Ａｌ単体でｎ型ＧａＮ用電極を形成できることは知られていたが、オーミック特性が悪く、また、アニール処理を経なければオーミック接触にならなかった。また、Ｒｈ，Ｐｄ，Ｉｒ，Ｐｔなどの金属ではｎ型窒化ガリウム系化合物半導体に対してオーミック接触が得られなかった。しかし、本発明者等の研究の結果、これらの材料の組合せによってアニール処理を行わずにｎ型窒化ガリウム系化合物半導体に対して良好なオーミック特性が得られることが判った。
図３はＡｌ／Ｉｒ層電極およびＡｌ／Ｐｄ層電極の接触抵抗値のアニール温度依存性を示す。なお、Ａｌ層の膜厚は３ｎｍ、Ｉｒ層またはＰｄ層の膜厚は１００ｎｍとし、真空蒸着法にてキャリア密度１×１０１８台のｎ型ＧａＮ層上に形成した。膜厚は水晶振動子を用いて蒸着厚をモニターして厚みを制御した。このようにして作製したｎ型ＧａＮ用電極を窒素雰囲気とした所定温度の電気炉内において２０秒間のアニール処理を実施した。接触抵抗率は４探針法（Transmission line model）により測定した。また、Ａｌ／Ｐｄ

の代わりにＡｌ／Ｒｈを同一条件で作成した場合Ａｌ／Ｐｄとほぼ同一であった。

ｎ型ＧａＮ層のドーピング濃度がさほど高いウェハを用いてはいないが、それでも常温において１０－６ｃｍ２台のオーミック特性が得られることが分かる。オーミック特性を得られる理由の詳細は不明であるが、本発明者等の研究により次のように考え得る。

【0019】

Ｒｈ，Ｐｄ，Ｉｒ，Ｐｔは周期律表においてＶＩＩＩ族第５，６周期の元素であって、且つその結晶はｆｃｃ構造をとることが知られている。また、格子定数の値はそれぞれＲｈは３８０．３ｐｍ，Ｐｄは３８９．０ｐｍ，Ｉｒは３８３．９４ｐｍ，Ｐｔは３９２．３ｐｍである。ここで、Ａｌはやはりｆｃｃ構造を取り、しかもその格子定数はａ＝４０４．９６ｐｍであって前記４種の金属と５％前後大きいだけである。従って、ＡｌとＲｈ等を積層した場合、相互に格子間に原子が入り込んで金属間化合物のようなものを形成し、何らかの原子間相互作用が起こるものと思われる。

また、１層目の電極材料であるＡｌと２層目の電極材料である金属元素とは原子半径が異なる。１層目の材料に２層目の電極材料に比べて原子半径の小さなＡｌを用いることで、密着性が向上しているものと推定される。

【0020】

上記のような相互作用がｎ型ＧａＮ層表面から深さ１０ｎｍ以内の領域で起こることで、半導体層／電極金属間のオーミック特性に好ましい影響を与えているものと思われる。このことは、本発明者等の実験によって確認することができた。

Ａｌ／Ｒｈ層においてＲｈ層の厚みを１００ｎｍと一定にし、Ａｌ薄膜の厚みを変えて評価した結果、Ａｌ薄膜が１０ｎｍ未満においては良好なオーミック特性が得られた。なお、この検討の際にアニール処理は実施していない。

Ａｌ薄膜の膜厚が２０ｎｍを超えるとＡｌ単層の厚膜（１００ｎｍ）をｎ型ＧａＮ層上に形成し、且つアニール処理を施した場合のオーミック特性とほぼ同等であった。即ち、Ａｌ／Ｒｈ、Ａｌ／Ｉｒ等の金属層によってｎ型ＧａＮ層とオーミック接触を得る場合、半導体層上に直接に形成する層であるＡｌ薄膜の膜厚が１０ｎｍより大きくなるとオーミック特性が急激に悪化する。本発明においてＡｌ薄膜の膜厚の望ましい範囲は１ｎｍ～１０ｎｍであり、薄膜形成時の膜厚制御性を考えるとより望ましくは１ｎｍ～５ｎｍであり、更に望ましくは２ｎｍ～４ｎｍである。また、１ｎｍより薄くなっても良好なオーミック特性が得にくくなる。

【0021】

Ａｌ層の構造については「薄膜」と定義したが、島状構造や網目構造なども同様の効果を奏するため、この「薄膜」にはこれらの構造も含む。また、ＡｌとＲｈ等の同時蒸着等何らかの手法によりＡｌ－Ｒｈ等の合金層を電極として形成した場合も同じようにアニール処理なしでオーミック接触が得られる。本発明の要点は、ＡｌとＲｈ等金属の相互作用がｎ型ＧａＮ層表面近傍で得られることによってオーミック接触が達成される点にあり、本要点を変更しない範囲で様々な応用が考えられる。

Ａｌ　３ｎｍ／Ｒｈ　１００ｎｍのＮ電極を用いて、アニール処理を行わないものと、同じ電極で５００℃のアニール処理を施したものについて取出し効率を測定したところ、アニール処理を施すことにより反射率が約２～３％低下した。また、表面反射率も低下していた。この原因はＡｌとＲｈの粒界が大きくなること、およびＡｌとｎ型ＧａＮ層の界面において拡散することが主な原因と考えられる。

なお、特許文献２には窒化ガリウム系化合物半導体とオーミック接触を得る電極材料としてＡｌも例示されている。しかしながら、Ｃｒ電極に比べるとオーミック特性が悪いことを開示するものの、積極的にアニール処理を施さない旨の記載はない。さらに、好適な厚みとしてｐ電極であるＮｉとして０．０１～０．５ミクロンとすることおよびＡｌ電極単独であることは開示するものの、半導体層と接するＡｌ層の膜厚を１０ｎｍ以下とすると積極的なアニール処理を施すことなくＡｌ単層膜に比べてオーミック特性が優れることについては一切記載されていない。

【0022】

ｐ型ＧａＮ用電極についても、ｐ型ＧａＮ層表面にＲｈまたはＰｄ，Ｐｔ，Ｐｔ／Ｒｈ，Ｐｔ／Ａｇ，Ｒｈ／Ａｇ，Ｐｄ／Ｒｈ，Ｐｄ／Ａｇ層を形成することによって、アニール処理なしでオーミック接触をなす電極が得られる（請求項６）。この時、Ｐｔ層の膜厚が０．３ｎｍ～１００ｎｍであり、及び／又は前記ＲｈもしくはＡｇ層の膜厚が５０ｎｍ～３００ｎｍであることが好ましい（請求項７）あるいは、前記Ｐｄ、Ｐｔ、又はＲｈ層の膜厚が０．３ｎｍ～２００ｎｍであることであることが好ましい（請求項８）。

これら電極の接触抵抗値のアニール温度依存性について図４に示す。

図４はＲｈ単層電極およびＰｔ／Ｒｈ層電極の接触抵抗値のアニール温度依存性を示す。なお、Ｒｈ層の膜厚は１００ｎｍ、Ｐｔ層の膜厚は１ｎｍとし、ｐ型ＧａＮ層上に真空蒸着法で形成した。膜厚は水晶振動子を用いて蒸着厚をモニターして厚みを制御した。このようにして作製したｐ型ＧａＮ用電極を窒素雰囲気とした所定温度の電気炉内において２０秒間のアニール処理を実施した。接触抵抗率は４探針法（Transmission line model）により測定した。

常温において１０－４ｃｍ２台のオーミック特性が得られることが分かる。

【0023】

これらの電極材料は、従来、アニール処理無しではオーミック接触を形成しないか、著しく抵抗が高いと思われていた。しかし、本発明者等の研究によって、アニール処理無しで実用的なほど低抵抗のｐ型ＧａＮ用電極を得ることができることが明らかになった。この場合、表面処理、特に、特開２０００－１０１１３４号公報にある脱酸素作用を有する液体、例えば王水による表面処理をｐ型ＧａＮ層表面に、電極層形成直前に行うことにより、アニール処理無しで極めて接触抵抗の低い、且つ密着性に優れたｐ型ＧａＮ用電極を得ることができた。ｐ型電極としてＰｄ、ＰｔまたはＲｈのいずれかの層を形成する場合には０．３～２００ｎｍが好適である。これより薄いと反射率が低下し、厚いと応力の問題が顕在化してくるからである。また、Ｐｔ／ＲｈまたはＰｔ／Ａｇの場合にも同様の理由によりＰｔ層の膜厚を０．３～１００ｎｍおよび／またはＡｇ層の膜厚を５０～３００ｎｍとすると良い。

【0024】

サファイア基板側を光取出し面とするフリップチップ型の実装方式を採る場合、ｐ型ＧａＮ用電極の発光波長に対する反射率はより高いほうが望ましい。しかし、アニール処理を経ることによって一般的には電極金属の反射率は低下する。熱を受けたことによって、半導体層／電極金属界面が荒れるからである。そこで、本発明の製造方法を用いれば、アニール処理を行わないため、電極金属の高い反射率をそのまま活かすことができ、光取り出し効率の上昇に大きく寄与する。

また本発明は、ｎ型窒化ガリウム系化合物半導体層およびｐ型窒化ガリウム系化合物半導体層を含むＩＩＩ族窒化物系化合物半導体積層構造と、ｎ型窒化ガリウム系化合物半導体層上に形成されたｎ電極と、ｐ型窒化ガリウム系化合物半導体上に形成されたｐ電極とを備えたＩＩＩ族窒化物系化合物半導体発光素子を提供するものであって、

前記ｎ電極が、ｎ型窒化ガリウム系化合物半導体層と接する厚さ１ｎｍ～１０ｎｍのＡｌ層と、前記Ａｌ層上に形成されるＲｈ、Ｉｒ、Ｐｔ、Ｐｄからなる群から選択されるいずれかの金属層とからなり、アニール処理を施すことなくオーミック接触していることを特徴とするＩＩＩ族窒化物系化合物半導体発光素子である（請求項９）。

この場合に、前記ｐ電極が、ｐ型窒化ガリウム系化合物半導体層と接するＰｄ、Ｐｔ、Ｒｈ、Ｐｔ／Ｒｈ、Ｐｔ／Ａｇ、Ｒｈ／Ａｇ、Ｐｄ／Ｒｈ、Ｐｄ／Ａｇ層からなる群から選択されるいずれかの層で構成され、厚みが２００ｎｍ以下であるとともに、アニール処理を施すことなくオーミック接触していることが好ましい（請求項１０）。

また、前記ｎ型またはｐ型窒化ガリウム系化合物半導体用電極上に、更に、共晶制限層および共晶材料層を積層してなる金属積層構造が形成されたることが好ましい（請求項１１）。

この場合、前記共晶制限層は実質的にＡｇ又はＰｔで構成されており、且つ、前記共晶材料層はＡｕ，Ｓｎ，Ｉｎからなる群から選択される金属、またはこれらのうち少なくと

も一つを含む合金で構成されていることが好ましい（請求項１２）。
　また本発明は、前記ＩＩＩ族窒化物系化合物半導体発光素子であって、前記半導体層の側面が、前記基板の垂直方向に対して傾斜しているとともに、
　前記電極が、前記傾斜した側面に延在して形成されていることを特徴とする窒化ガリウム系化合物半導体デバイスを提供する（請求項１３）。
【発明の効果】
【0025】
　本発明により、ＧａＮ系デバイスの電極を形成するにあたってアニール処理が不要となる。そのため、ウェハに不要な熱履歴が蓄積せず、電極のオーミック特性や反射率がプロセスにおいて劣化しないという効果がある。また、ｎ型又はｐ型ＧａＮ用電極の形成後、蒸着用真空装置から出さずに続けてＡｕ／Ｓｎ積層構造等の共晶電極を積層できるため、デバイスプロセスに要する総合的な時間を著しく短縮できる。また、蒸着真空装置から取り出すことがないためｐ型もしくはｎ型ＧａＮ用電極の汚染や表面酸化を防止することができる。また、蒸着回数が少なくて済む。さらに、プロセス設計にあたって熱に弱い有機材料が使用し得るなどの自由度が大きくなるという利点がある。
　また、アニール処理を行うと、ＧａＮ層と電極材料間の熱膨張係数の相違による応力がかかるが、本発明においては電極材料に与える熱履歴が少なくなるので応力の蓄積が著しく小さくなるため、電極の剥離が抑制され信頼性が向上する。
　特にボンディングパッド部を除く電極層の総厚みを２００ｎｍ以下とすると、剥離が殆ど発生せずに好適である。
　従って、本発明はＧａＮ系デバイス製造にあたって非常に優れた工業的価値を持つことが明らかである。なお、ＧａＮ層にて説明したが、ＡｌＧａＩｎＮ、ＡｌＧａＮ、ＩｎＧａＮ層などの窒化ガリウム系化合物半導体の場合も同様であろう。
【発明を実施するための最良の形態】
【0026】
　以下に本発明の２つの実施例を示す。両実施例ともフリップチップ方式の実装方法を前提としているが、半導体面側を光取出し面とするフェイスアップ方式であっても本発明は当然適用可能である。本実施例は発明者らが本発明の効果を確認するために行った実験のうちの幾例かを挙げたに過ぎず、本発明は実施例に限定して解釈されるべきではない。
【実施例】
【0027】
　ＭＯＣＶＤ法によってサファイア基板１上にバッファ層を介してシリコン（Ｓｉ）ドープのｎ型ＧａＮ層２、窒化ガリウムアルミインジウム系化合物からなる活性層３、マグネシウム（Ｍｇ）をドープしたｐ型ＧａＮ層４を含むデバイスウェハを得た。次いで、このウェハを以下に示すプロセスで加工した。この工程について図１を参照して説明する。
【0028】
　（１）ウェハを液温２０℃の王水（体積比で濃硝酸１：濃塩酸３）中に５分間浸漬洗浄、超純水リンスを施す表面処理工程を行ないｐ型ＧａＮ層４表面を清浄化した。その後、その表面に電子線加熱蒸着法によりｐ型ＧａＮ用電極６としてＰｔ１ｎｍ／Ｒｈ １００ｎｍを形成し、連続して共晶電極７としてＴｉ１００ｎｍ／(Ｐｔ １００ｎｍ／Ａｕ２００ｎｍ)２を形成し、その一部を除去した。（図１（Ａ）参照）
【0029】
　（２）ｐ型ＧａＮ層４の一部を周知の技術である反応性イオンエッチング法によってエッチングして、ｎ型ＧａＮ層２を部分的に露出させた。（図１（Ｂ）参照）
【0030】
　（３）露出したｎ型ＧａＮ層２表面の一部に、フォトリソグラフィと電子線加熱蒸着法とによりｎ型ＧａＮ用電極５としてＡｌ
３ｎｍ／Ｒｈ １００ｎｍを形成し、連続して共晶電極７'としてＴｉ １００ｎｍ／Ｐｔ １００ｎｍ／Ａｕ１００ｎｍ～１０００ｎｍ／Ｐｔ １００ｎｍ／Ａｕ２００ｎｍ（下層側のＡｕ層厚は設計上可変）を形成した。（図１（Ｃ）参照）

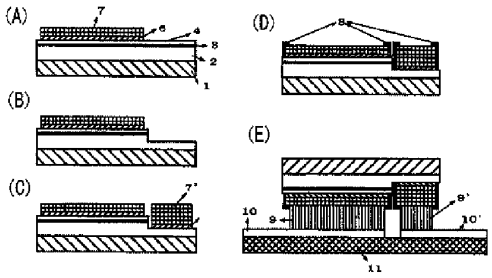
【0031】
（４）周知の技術によって、共晶電極部分を除くウェハ表面をＳｉＯ２膜８で被覆し、また、デバイス毎にウェハをカットした。（図１（Ｄ）参照）
【0032】
（５）デバイスの共晶電極部分７，７’と、別に構成したサブマウント１１の共晶部９，９’と合わせ、３００℃程度の熱圧着によってサブマウント１１にデバイスを接合した。（図１（Ｅ）参照）
【0033】
従来技術において、デバイスプロセスはｎ型ＧａＮ用電極、ｎ型ＧａＮ用電極上部共晶電極、ｐ型ＧａＮ用電極、ｐ型ＧａＮ用電極上部共晶電極の電極等を表面に形成するために、フォトリソグラフィによるパターニングと電子線加熱蒸着法による電極材料の積層工程を、４回繰り返す必要があった。しかし、本発明においては、ｎ型ＧａＮ用電極とｎ型ＧａＮ用電極上部共晶電極を続けて１回の工程で形成することができ、またｐ型ＧａＮ用電極とｐ型ＧａＮ用電極上部共晶電極を続けて１回の工程で形成することができる。すなわち、合計として２回の工程で済ませることができ、大変経済性がよい。また、デバイスの熱履歴は最高で３００℃であり、これによりデバイスの熱による劣化を抑えることができる。
【実施例】
【0034】
図２及び以下に示すデバイスプロセスにおいて、実施例１と同じウェハに対してｎ型ＧａＮ用電極を先に形成した。
【0035】
（１）ｐ型ＧａＮ層４の一部を周知の技術である反応性イオンエッチングによってエッチングして、ｎ型ＧａＮ層２を部分的に露出させた。この際、ＧａＮ層２，３，４の側面をウェハ底面となす角が４５°前後になるように傾斜させた。（図２（Ａ）参照）
【0036】
（２）露出したｎ型ＧａＮ層２表面および傾斜した側面に、フォトリソグラフィと電子線加熱蒸着法とによりｎ型ＧａＮ用電極５としてＡｌ３ｎｍ／Ｉｒ １００ｎｍを形成し、連続して共晶電極’としてＮｉ １００ｎｍ／Ｐｔ １００ｎｍ／Ａｕ １００ｎｍ／(Ｐｔ１００ｎｍ／Ａｕ ２００ｎｍ)２（下層側のＡｕ層厚は設計上可変）を形成した。（図２（Ｂ）参照）
【0037】
（３）ｐ型ＧａＮ層４表面の一部にフォトリソグラフィと電子線加熱蒸着法とによりｐ型ＧａＮ用電極６としてＰｔ１ｎｍ／Ａｇ １００ｎｍを形成し、連続して共晶電極７としてＮｉ１００ｎｍ／Ｐｔ １００ｎｍ／Ａｕ １００～１０００ｎｍ／Ｐｔ １００ｎｍ／Ａｕ２００ｎｍを形成した。（図２（Ｃ）参照）
【0038】
（４）周知の技術によって、共晶電極部分を除くウェハ表面をＳｉＯ２膜８で被覆し、また、デバイス毎にウェハをカットした。（図２（Ｄ）参照）
【0039】
（５）デバイスの共晶電極部分７，７’と、別に構成したサブマウント１１の共晶反応部分９，９’と合わせ、３００℃程度の熱圧着によってサブマウント１１にデバイスを接合した。（図２（Ｅ）参照）
【0040】
ＧａＮ層の側面を傾斜させ、その側面に延在させてｐ型および／又はｎ型ＧａＮ用電極を形成することは、層内を伝播する光を傾斜端面において透光性基板側に反射するので各層に対してほぼ垂直な端面を有する場合に比べて光取り出し効率が向上する。よって光の取り出し効率の観点から、特にフリップチップ方式を用いて実装する場合に有効な方法である。また、本発明によるこのような構成としたことで、電極形成工程において副次的に次のような効果がある。

【0041】
傾斜した側面に電極を形成し、従来の方法のようにアニールを行うと、図５の１２に示すように電極金属がだれることがある。電極層が厚くなれば大きくだれてしまい、これにより電極の短絡などの問題になりかねない。しかし、本発明においては電極に対してアニールを行なわないため、このような電極だれの問題は発生しなくなり、デバイス製造時の信頼性向上に著しい効果がある。
【0042】
なお、実施例１ではｎ型ＧａＮ用電極としてＡｌ
３ｎｍ／Ｒｈ　１００ｎｍ、ｐ型ＧａＮ用電極としてＰｔ
１ｎｍ／Ｒｈ　１００ｎｍを用い、実施例２ではｎ型ＧａＮ用電極としてＡｌ
３ｎｍ／Ｉｒ　１００ｎｍ、ｐ型ＧａＮ用電極としてＰｔ
１ｎｍ／Ａｇ　１００ｎｍを用いた。しかし、ｎ型ＧａＮ用電極としてはＡｌ／Ｒｈ，Ａｌ／Ｉｒ以外にもＡｌ／Ｐｄ，Ａｌ／Ｐｔを使用することが可能であり、また、ｐ型ＧａＮ用電極としてＰｔ／Ｒｈ，Ｐｔ／Ａｇ以外にもＲｈを使用することができることは言うまでもない。
【0043】
実施例においては、共晶電極接着のため共晶電極としてＡｕを用いた場合には３００℃程度以下の加熱で接合することができるので、３００℃より高い温度がかかることはない。これに対し、従来技術における電極のアニール処理では少なくとも４００℃以上の温度で加熱が複数回行なわれ、その温度差は少なくとも１００℃以上ある。熱がデバイスに及ぼす悪影響は、温度に対して指数関数的に大きくなる性質があるから、この１００℃の差のアニール処理が複数回行なわれるによってデバイスの性能は本発明によるデバイス性能と相当に違ってくる。共晶電極の材料を最適に選択することで、本発明のデバイスに対する最終的な熱履歴は更に減らすことができる。特に、上記したフリップチップ型の実装方式を採用する場合において、共晶電極層／共晶制限層からなる共晶電極を窒化ガリウム用電極上に形成し、共晶電極層として、Ａｕ，Ｓｎ，Ｉｎからなる群れから選択される金属、またはこれらのうちの少なくとも一つを含む合金、特にＡｕもしくはＡｕを含む合金で構成した場合には、共晶接続を行う際の熱の影響を小さくすることができ好適である。また、共晶制限層としてＡｇまたはＰｔを用いた場合には積極的なアニール処理を施さない電極を用い且つ共晶電極層としてＡｕ、Ｓｎ，Ｉｎを用いた場合において、共晶電極層材料の窒化ガリウム層もしくは該層用電極への拡散を効果的に抑止することができる。共晶電極層／共晶制限層を複数回積層した場合にはより効果的となる。各層の膜厚は好ましくは５０ｎｍ～２０００ｎｍであり、前記ｎ型またはｐ型窒化ガリウム系化合物半導体用電極と前記共晶電極との間にＴｉ層またはＮｉ層が挿入すると、より拡散を抑止することができ得る。
また、フェイスアップ方式の実装方法で、共晶電極を全く使用しないならば、実装に至るまで事実上全く熱処理工程を含まないデバイスプロセスが本発明によって実現可能である。
【図面の簡単な説明】
【0044】
【図1】（A）から（E）は本発明による窒化ガリウム系化合物半導体ウェハプロセスの一実施態様である。
【図2】（A）から（E）は本発明による窒化ガリウム系化合物半導体ウェハプロセスの他の実施態様である。
【図3】本発明によるｎ型窒化ガリウム系化合物半導体用電極の接触抵抗値のアニール温度依存性を示す図である。
【図4】本発明によるｐ型窒化ガリウム系化合物半導体用電極の接触抵抗値のアニール温度依存性を示す図である。
【図5】従来技術によるアニール処理において起こる電極のだれについて示した図である。

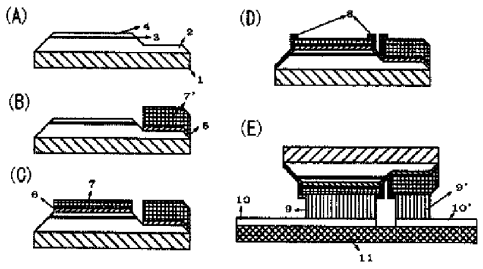
【図6】従来技術による窒化ガリウム系化合物半導体デバイスについて示した図である。
【符号の説明】
【0045】

１	サファイア基板
２	ｎ型窒化ガリウム系化合物半導体層
３	活性層
４	ｐ型窒化ガリウム系化合物半導体層
５	ｎ型窒化ガリウム系化合物半導体用電極
６	ｐ型窒化ガリウム系化合物半導体用電極
７，７’	共晶電極
８	ＳｉＯ２膜
９，９’	サブマウント側共晶部
１０，１０’	サブマウント側配線部
１１	サブマウント基板
１２	電極だれ

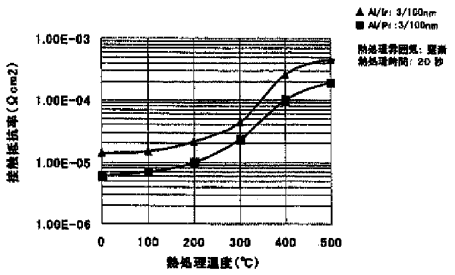
【図1】



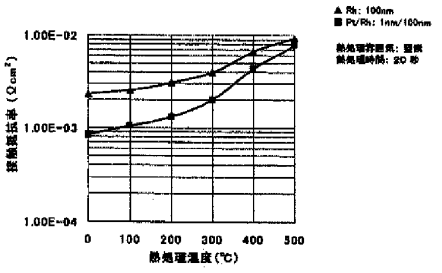
【図2】



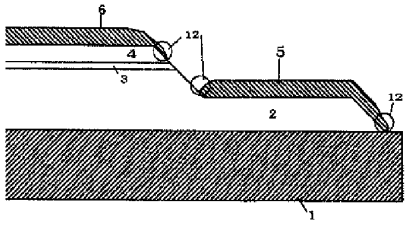
【図3】



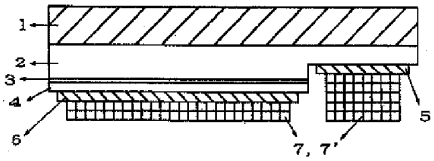
【図4】



【図5】



【図6】



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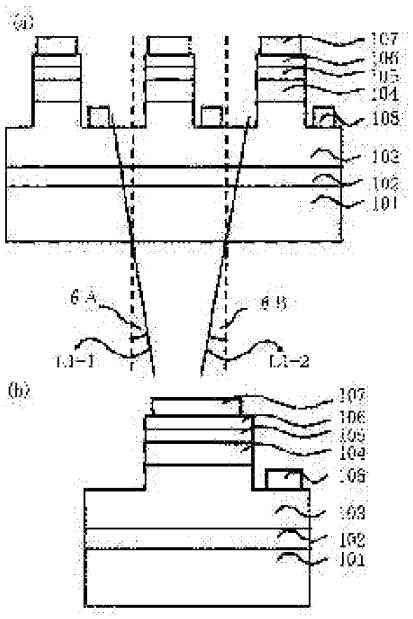
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(71)Applicant : SHARP CORP
(72)Inventor : YAMAMOTO KENSAKU
HATA TOSHIO

(54) NITRIDE SEMICONDUCTOR LIGHT-EMITTING DIODE CHIP AND ITS MANUFACTURING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a nitride semiconductor light-emitting diode chip with the light extraction efficiency is improved.
SOLUTION: The nitride-semiconductor light-emitting diode chip includes a light-transmitting substrate (101) and a nitride-semiconductor laminated structure (102 to 106) formed on the top face of the substrate (101). The nitride-semiconductor laminated structure includes a light-emitting layer (104) and a plurality of other semiconductor layers. The substrate (101) does not depend on the face azimuth and has a thickness of 120 μm or larger. Consequently, the extraction efficiency of a light from the chip is improved. At least one of the parting faces of the chip is inclined to a surface orthogonal with respect to a substrate surface, and the underside of the substrate also has an area smaller than that of the upper-side region of the nitride-semiconductor laminated structure, thus improving the extraction efficiency of the light from the chip.



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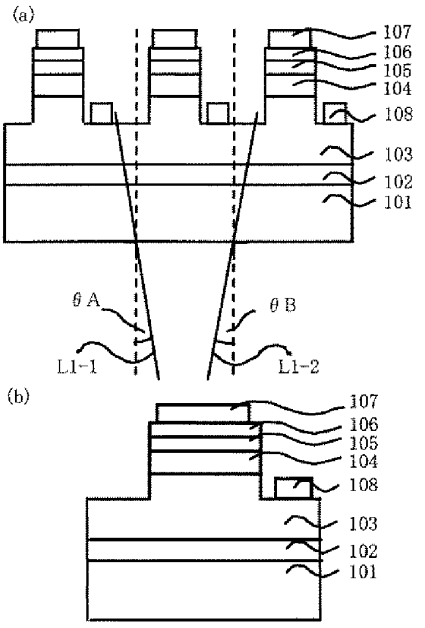
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(71)出願人　000005049
シャープ株式会社
大阪府大阪市阿倍野区長池町２２番２２号
(74)代理人　100064746
弁理士　深見　久郎
(74)代理人　100085132
弁理士　森田　俊雄
(74)代理人　100083703
弁理士　仲村　義平
(74)代理人　100096781
弁理士　堀井　豊
(74)代理人　100098316
弁理士　野田　久登
(74)代理人　100109162
弁理士　酒井　將行

最終頁に続く

(54)【発明の名称】窒化物半導体発光ダイオードチップとその作製法

(57)【要約】
【課題】　光取り出し効率の改善された窒化物半導体発光ダイオードチップを提供する。
【解決手段】　窒化物半導体発光ダイオードチップは、透光性基板（１０１）と、その基板の上面上に形成された窒化物半導体積層構造（１０２－１０６）とを含み、その窒化物半導体積層構造は発光層（１０４）と他の複数の半導体層とを含み、基板（１０１）は面方位によらずかつ１２０μｍ以上の厚さを有しており、これによってチップからの光の取り出し効率が改善されている。なお、チップの分割面の少なくとも一つは基板面に直交する面に対して傾斜させられ、かつ基板の下面は窒化物半導体積層構造の上側領域より小さい面積を有することによっても、チップからの光の取り出し効率が改善され得る。
【選択図】　図1



【特許請求の範囲】
【請求項1】
窒化物半導体発光ダイオードチップであって、透光性基板と、前記基板の上面上に形成された窒化物半導体積層構造とを含み、前記窒化物半導体積層構造は発光層とその他の複数の半導体層とを含み、前記基板は面方位によらずかつ１２０μｍ以上の厚さを有しており、これによって前記チップからの光の取り出し効率が改善されていることを特徴とする窒化物半導体発光ダイオードチップ。
【請求項2】
窒化物半導体発光ダイオードチップであって、透光性基板と、前記基板の上面上に形成された窒化物半導体積層構造とを含み、前記窒化物半導体積層構造は発光層とその他の複数の半導体層とを含み、前記基板は面方位によらないものであって、前記チップの分割面の少なくとも一つは前記基板の上面に直交する面に対して傾斜させられており、かつ前記基板の下面は前記窒化物半導体積層構造の上側領域より小さい面積を有しており、これによって前記チップからの光の取り出し効率が改善されていることを特徴とする窒化物半導体発光ダイオードチップ。
【請求項3】
前記チップの分割面の少なくとも一つは前記基板の上面に直交する面に対して傾斜させられており、かつ前記基板の下面は前記窒化物半導体積層構造の上側領域より小さい面積を有していることを特徴とする請求項１に記載の窒化物半導体発光ダイオードチップ。
【請求項4】
前記基板として絶縁性基板が用いられていることを特徴とする請求項１から３のいずれかに記載の窒化物半導体発光ダイオードチップ。
【請求項5】
前記基板としてサファイア基板または炭化珪素基板が用いられていることを特徴とする請求項１から４のいずれかに記載の窒化物半導体発光ダイオードチップ。
【請求項6】
請求項１から５のいずれかに記載された窒化物半導体発光ダイオードチップを作製するための方法であって、基板の上面上において発光層を含む複数の窒化物半導体層を結晶成長させたエピタキシャルウエハを形成する工程と、レーザ光を利用して前記ウエハから前記チップを分割する工程とを含み、これによってチップ歩留まりが改善されることを特徴とする作製法。
【請求項7】
前記レーザ光の光源として固体レーザ装置が利用されることを特徴とする請求項６に記載の作製法。

【発明の詳細な説明】
【技術分野】
【0001】
本発明はＩＩＩ－Ｖ族化合物半導体発光素子に関し、特に透光性基板上に積層された複数の窒化物系半導体層を含む発光ダイオードチップにおける光取り出し効率の改善に関するものである。
【背景技術】
【0002】
一般に、窒化物半導体発光ダイオードチップの作製においては、基板上に発光層を含む複数の窒化物半導体層が堆積されたエピタキシャルウエハが形成され、そのウエハを分割することによって複数のチップが得られる。従来の窒化ガリウム（ＧａＮ）系半導体発光ダイオードチップでは、主にサファイア等の基板が使用されており、現在ではそのようなチップを含む発光ダイオード装置が商品化されている。
【0003】
ところで、サファイア基板を用いた発光ダイオード装置では、その基板が絶縁性であるので、基板の上下両面側にｐ側電極とｎ側電極をそれぞれ設けた構造にすることが困難で

あり、透光性の電極を介して発光ダイオードチップから光を取り出す必要がある。さらに、サファイア基板の硬度が高いことから、基板を薄膜状に加工した後に、ウエハからチップに分割する必要がある。

【0004】

従来の代表的な窒化物半導体発光素子として、サファイア基板上にＧａＮ系半導体積層構造を形成して、その基板を１００μｍ程度の厚みにした後にチップ化されたものが商用化されている。例えば特開２００２－２７０９６２号公報に開示されているように、サファイア基板上に作製したＧａＮ系半導体発光素子層を分割する際に、基板厚さを８０μｍの薄さに加工している。さらに、特開２０００－６８５５６号公報では、サファイア基板上に堆積した複数の窒化物半導体層を含むエピタキシャルウエハを歩留まりよくチップ化する方法が検討されており、その方法によって８０μｍの厚みを有するウエハをチップ分割している。

【特許文献1】特開２００２－２７０９６２号公報

【特許文献2】特開２０００－６８５５６号公報

【発明の開示】

【発明が解決しようとする課題】

【0005】

上述のように、従来の窒化物半導体発光ダイオードチップにおいては、それに含まれる半導体積層構造の表面に、透光性の電極（通常はｐ側電極下）とｐ側およびｎ側の両電極とを形成する必要がある。そして、基板の裏面は支持台上に接合される。したがって、チップから外部への光の取出し効率に関して、ｐ側およびｎ側の両電極で光が遮られることによる損失が生じる。

【0006】

また、サファイア基板を含むエピタキシャルウエハから複数の発光ダイオードチップを歩留まりよく分割する場合、サファイア基板の硬度が高くてダイシングやスクライブが困難である。したがって、エピタキシャルウエハの形成後に、基板を研削するなどして１００μｍ以下の薄さにする必要がある。しかし、基板を薄くするれば、基板の側面から外部への光の取り出し効率が低下する。これらの事情から、従来のサファイア基板を含む窒化物半導体発光ダイオードチップにおいて、チップから外部へ光の取り出しを行う際の光損失が大きい。

【0007】

以上のような従来技術の状況に鑑み、本発明は、光取り出し効率の改善された窒化物半導体発光ダイオードチップを歩留まりよく提供することを主要な目的としている。

【課題を解決するための手段】

【0008】

本発明の一つの態様によれば、窒化物半導体発光ダイオードチップは、透光性基板と、その基板の上面上に形成された窒化物半導体積層構造とを含み、その窒化物半導体積層構造は発光層と他の複数の半導体層とを含み、基板は面方位によらずかつ１２０μｍ以上の厚さを有しており、これによってチップからの光の取り出し効率が改善されていることを特徴としている。

【0009】

本発明の他の態様によれば、窒化物半導体発光ダイオードチップは、透光性基板と、その基板の上面上に形成された窒化物半導体積層構造とを含み、その窒化物半導体積層構造は発光層とその他の複数の半導体層とを含み、基板は面方位によらないものであって、チップの分割面の少なくとも一つは基板面に直交する面に対して傾斜させられており、かつ基板の下面は窒化物半導体積層構造の上側領域より小さい面積を有しており、これによってチップからの光の取り出し効率が改善されていることを特徴としている。

【0010】

なお、基板としては、絶縁性基板が用いられ得る。また、絶縁性基板として、サファイア基板、炭化珪素基板、またはスピネル基板が用いられ得る。

【0011】
上述のような窒化物半導体発光ダイオードチップを作製するための方法として、基板の上面上において発光層を含む複数の窒化物半導体層を結晶成長させたエピタキシャルウエハを形成する工程と、レーザ光を利用してウエハからチップを分割する工程とを含むことができ、これによってチップ歩留まりが改善され得る。なお、レーザ光の光源として、固体レーザ装置が好ましく利用され得る。
【発明の効果】
【0012】
本発明の一つの態様によれば、窒化物半導体発光ダイオードチップに含まれる透光性基板が従来に比べて大きな１２０μｍ以上の厚さを有している。したがって、大きな厚さの基板の側面からの光放射量が増大して、発光ダイオードチップからの光の取り出し効率が改善され得る。本発明の他の態様によれば、窒化物半導体発光ダイオードチップの分割面の少なくとも一つが基板の上面に直交する面に対して傾斜させられており、かつ基板の下面は窒化物半導体積層構造の上側領域より小さい面積を有している。したがって、その基板の傾斜側面による反射や屈折の影響によって、基板の側面からの光放射量が増大し、発光ダイオードチップからの光の取り出し効率が改善され得る。
【発明を実施するための最良の形態】
【0013】
（実施例１）
図１において、本発明の実施例１によるＧａＮ系化合物半導体発光ダイオードに関するチップ分割法が模式的な断面図で図解されている。すなわち、図１（ａ）は複数の発光ダイオード構造を含むエピタキシャルウエハを表し、図１（ｂ）はそのウエハから分割された発光ダイオードチップを表している。なお、本願の図面において、種々の層の厚さや幅などの寸法関係は図面の明瞭化と簡略化のために適宜に変更されており、実際の寸法関係を表してはいない。
【0014】
図１（ａ）のウエハにおいて、厚さ４３０μｍで、Ｃ面（０００１）の面方位をもったサファイア基板１０１上に、ＧａＮバッファ層１０２、ｎ型ＧａＮコンタクト層１０３、$In_{0.08}Ga_{0.92}N$量子井戸層とＧａＮ障壁層の４ペアーからなるＭＱＷ（多重量子井戸）活性層１０４、ｐ型ＡｌＧａＮ層１０５、ｐ型ＧａＮコンタクト層１０６が順次積層されている。そして、ｐ型ＧａＮコンタクト層１０６上にｐ側コンタクト電極として透光性Ｐｄ電極１０７が形成され、ｎ型ＧａＮコンタクト層１０３上にｎ側コンタクト電極としてＴｉとＡｌを用いたｎ側電極１０８が形成されている。
【0015】
図１（ａ）のウエハの作製においては、ＭＯＣＶＤ（有機金属気相成長）法を用いて、サファイア基板１０１上に複数のＧａＮ系半導体層がエピタキシャル成長させられた。まず、サファイア基板１０１を反応室内のサセプター上に装着後、NH_3とN_2とH_2を混合した雰囲気にて１２００℃でその基板のベーキングを行った。
【0016】
その後、すみやかに基板温度を４５０℃に降温し、H_2のキャリアガスとともにトリメチルガリウム（ＴＭＧ）とアンモニア（NH_3）を用いて、厚さ３０ｎｍのＧａＮバッファ層１０２を基板上に堆積した。続いて、すみやかに基板温度を１１００℃に昇温し、トリメチルガリウム（ＴＭＧ）とNH_3およびドーパントのモノシラン（SiH_4）を用いて、バッファ層１０２上に厚さ５μｍのｎ型ＧａＮコンタクト層１０３を成長させた。
【0017】
次に、７５０℃の基板温度にて、トリメチルインジウム（ＴＭＩ）、ＴＭＧ、およびNH_3を利用して、ｎ型コンタクト層１０３上において、厚さ３ｎｍの$In_{0.08}Ga_{0.92}N$井戸層と厚さ９０ｎｍのＧａＮ障壁層の４ペアーからなるＭＱＷ活性層１０４を形成した。
【0018】

さらに、基板温度１１００℃にて、トリメチルアルミニウム（ＴＭＡ）、ＴＭＧ、NH_3、およびドーパントのシクロペンタジエニルマグネシウム（Cp_2Mg）を用いて、ＭＱＷ活性層１０４上に、Ｍｇドープのｐ型$Al_{0.08}Ga_{0.92}N$クラッド層１０５を厚さ３０ｎｍに成長させた。続いて、同じ基板温度にて、ＴＭＧ、NH_3、およびCp_2Mgを用いて、ｐ型クラッド層１０５上に厚さ１２０ｎｍのＭｇドープｐ型ＧａＮコンタクト層１０６を堆積し、基板温度を常温まで冷却した後にエピタキシャルウエハを大気中に取り出した。

【0019】

その後、エピタキシャルウエハ中のｐ型ドーパントを活性化するために、熱処理炉を用いてN_2雰囲気中で８００℃にて１５分間の熱処理を行った。次に、ウエハの上面にレジストを塗布してフォトリソグラフィを行った後、ｐ型ＧａＮ層１０６上にｐ側コンタクト電極として透光性Ｐｄ電極１０７を形成した。

【0020】

次に、有機洗浄を行ってレジストを除去した後にウエハ上面に再度レジストを塗布してフォトリソグラフィを行ない、続いて反応性イオンエッチング（ＲＩＥ）を利用して、ウエハのｐ型ＧａＮ層１０６からｎ型ＧａＮ層１０３に達するまで選択的にエッチングを行った。さらに、有機洗浄を行ってレジストを除去した後にウエハ上面に再度レジストを塗布してフォトリソグラフィを行ない、ｎ型ＧａＮ層１０３上にｎ側コンタクト電極としてＴｉとＡｌからなるｎ側電極１０８を形成した。

【0021】

続いて、有機洗浄を行ってレジストを除去した後にウエハ上面に再度レジストを塗布してフォトリソグラフィを行ない、電極部を除いてウエハ上面がSiO_2膜（図示せず）で覆われた。

【0022】

その後、ウエハをシートに貼り付けて冶具に固定し、ウエハから複数の発光ダイオードチップの分割が固体レーザ装置を用いて行われた。より具体的には、固体レーザ装置としてＹＡＧレーザ装置が利用され、２６６ｎｍまたは３５５ｎｍの高調波レーザ光が用いられた。レーザ光のエネルギに関しては、１０μＪ／ｃｍ^2～１００ｍＪ／ｃｍ^{2}程度の範囲内のパルス状または連続な状態のレーザ光を使用することができる。なお、レーザ装置としてはＹＡＧレーザ装置に限られず、２６６ｎｎから３５５ｎｍ程度の波長範囲内のレーザ光を放射し得るレーザ装置を用いて、サファイア基板の局所的な昇華または熱膨張を利用してスクライブできればよい。

【0023】

具体的には、レーザ光がサファイア基板に進入する角度を冶具によって制御して、レーザスクライブラインＬ１－１とＬ１－２に沿って、ウエハから複数の発光ダイオードチップが分割された。本実施例１においては、図１（ａ）に示されているように、スクライブラインＬ１－１とＬ１－２は、基板面に直交する破線に対して時計回りを正にして$\theta A=0°$および$\theta B=0°$の角度をなすように設定され、その状態でスクライブを行った。その結果、図１（ｂ）に示されているように、一辺が３５０μｍの正方形状平面を有するＧａＮ系発光ダイオードチップが得られた。そのような発光ダイオードチップはその基板底面が支持台上に接合され、電気的配線と樹脂モールドを介して発光ダイオード装置として完成させられる。

【0024】

従来法によれば、ダイオードチップ作製において、サファイア基板を研削研磨し、裏面よりダイアモンド製のカッターによって分割した。しかし、この方法では、サファイア面に対して、分割する角度を制御して歩留まりよくチップ分割をすることは難しかったが、本実施例の方法によれば、歩留まりよく、なおかつ分割角度の制御がよくダイオードチップの作製が可能になった。

【0025】

図１（ｂ）に示された本実施例１のＧａＮ系発光ダイオードチップの出力特性は、従来

のＧａＮ系発光ダイオードチップの出力特性と比較された。その従来の発光ダイオードチップの作製においては、図１（ａ）と同様のエピタキシャルウエハが作製された。しかし、そのウエハから複数の発光ダイオードチップを分割する際に、従来方法に従ってウエハの厚さを１００μｍ程度まで基板裏面を研削して研磨し、その後に機械的スクライブとブレーキングによってチップ分割された。こうして得られた従来の発光ダイオードチップにおいて、順方向注入電流（Ｉｆ）＝２０ｍＡのときに、光出力（Ｐｏ）＝３．０ｍＷであった。他方、本実施例１によって作製された図１（ｂ）の発光ダイオードチップにおいては、Ｉｆ＝２０ｍＡのときにＰｏ＝５．０ｍＷであった。

【0026】

すなわち、本実施例１におけるチップ分割による発光ダイオードチップは、従来に比べて光出力が顕著に改善されていることがわかる。この理由としては、従来の機械的スクライブ法では研削と研磨によってサファイア基板１０１を１００μｍ程度に薄くしなければチップ化することが困難であったが、本実施例１のようにレーザスクライブを利用する方法では基板が４３０μｍのように厚くてもチップ分割が可能であることから、発光層から放射されて基板裏面で反射された光が、基板側面から外部へ取り出されやすくなったために、光取り出し効率が向上したと考えられる。

【0027】

さらなる検討の結果では、本実施例においてサファイア基板１０１の厚さが２５０μｍである場合には、Ｉｆ＝２０ｍＡのときにＰｏ＝３．８ｍＷであることがわかった。また、サファイア基板１０１の厚さが１２０μｍ以上の場合に、従来に比べて発光ダイオードチップの光出力が向上することがわかった。

【0028】

（実施例２）

図２において、本発明の実施例２によるＧａＮ系化合物半導体発光ダイオードに関するチップ分割法が模式的な断面図で図解されている。この図２における複数層２０１～２０８の作製法は実施例１における複数層１０１～１０８の作製法と同様であるので、その説明は繰り返されない。なお、本実施例２においても、サファイア基板２０１として、実施例１と同様に４３０μｍの厚さものが使用された。また、本実施例２においても、実施例１と同様にレーザスクライブを利用して、エピタキシャルウエハから発光ダイオードチップが分割された。

【0029】

本実施例２においては、レーザ光が基板へ入射する角度を冶具で制御することによって、図２の基板面に垂直な破線方向に対するレーザスクライブラインＬ２－１およびＬ２－２の傾斜角θＣおよびθＤが制御された。このとき、図２において、光を放射する半導体層の上面領域で一辺の長さｄを３５０μｍに設定し、θＣとθＤを調整することによって基板裏面側の一辺の長さｅが２００μｍになるように設定した。ただし、図２に示されているように、スクライブラインＬ２－１とＬ２－２は、それぞれ基板面に直交する破線に対して時計回りを正にしてθＣ＜０°およびθＤ＞０°の角度をなすように設定された。

【0030】

こうして得られた本実施例２の発光ダイオードチップにおいて、Ｉｆ＝２０ｍＡの入力電流のもとで、光出力はＰｏ＝５．２ｍＷであった。すなわち、本実施例２の発光ダイオードチップにおける外部への光取り出し効率は、実施例１と比較しても向上したことがわかる。この理由としては、基板面に垂直な面に対して発光ダイオードチップの側面を傾斜させることによって、その傾斜側面による反射や屈折の影響によって、発光層からの光が基板側面から放射されやすくなったものと考えられる。

【0031】

さらなる検討の結果、ｄ＝３５０μｍに固定してｅ＝１００μｍになるように発光ダイオードチップを作製したところ、Ｉｆ＝２０ｍＡの入力電流のもとでPo＝５．４ｍＷの光出力が得られた。しかしながら、さらなる検討の結果では、基板底面の長さｅが１００μｍより小さな発光ダイオードチップを作製したところ、Ｉｆ＝２０ｍＡの入力電流のも

とで光出力がＰｏ＝４．０ｍＷになった。これは、発光層から放射されて基板裏面で反射された光が、基板側面から外部へ取り出されにくくなり、光取り出し効率が悪化したためと考えられる。

【0032】

（実施例３）

図３と図４において、本発明の実施例３によるＧａＮ系化合物半導体発光ダイオードに関するチップ分割法が模式的な断面図で図解されている。この図３と図４における複数層３０１～３０８の作製法も実施例１における複数層１０１～１０８の作製法と同様であるので、その説明は繰り返されない。なお、本実施例３においても、サファイア基板３０１として、実施例１と同様に４３０μｍの厚さのものが使用された。また、本実施例３においても、実施例１と同様にレーザスクライブを利用して、エピタキシャルウエハから発光ダイオードチップが分割された。

【0033】

本実施例３に係る図３と図４においても、実施例２の場合と同様に、レーザ光が基板へ入射する角度を冶具で制御することによって、基板面に垂直な破線方向に対するレーザスクライブラインＬ３－１およびＬ３－２の傾斜角θＥおよびθＦが制御された。そして、光を放射する半導体層の上面領域で一辺の長さｆを３５０μｍに設定し、θＥとθＦを調整することによって基板裏面側の一辺の長さｅが２００μｍになるように設定した。ただし、スクライブラインＬ３－１とＬ３－２は、基板面に直交する破線に対して時計回りを正にして、図３においてはθＥ＜０°およびθＦ＝０°の角度をなすようにそれぞれ設定され、図４においてはθＥ＜０°およびθＦ＜０°の角度をなすようにそれぞれ設定された。

【0034】

こうして得られた図３と図４のいずれの発光ダイオードチップにおいても、Ｉｆ＝２０ｍＡの入力電流のもとで、光出力はＰｏ＝５．２ｍＷであった。すなわち、本実施例３の発光ダイオードチップにおける外部への光取り出し効率も、実施例２の場合と同様に実施例１と比較しても向上したことがわかる。この理由は、実施例２の場合と同様と考えられる。

【0035】

なお、上述のいずれの実施例においても基板としてＣ面（０００１）の面方位を持ったサファイア基板を用いたが、この面方位によらずにＡ（１１－２０）面、Ｍ（１１００）面、またはR面（１１０２）の面方位を持ったサファイア基板を用いても、それらの面方位から変位させられたオフ面方位のサファイア基板であっても、同様の効果が得られる。また、基板として、ＧａＮ基板、スピネル基板、またはＳｉＣ基板を用いることもできる。さらに、上述の実施例において、サファイア基板に対するレーザ光の入射角度が基板を固定する冶具によって制御されたが、レーザ光をミラー等で制御してサファイア基板に対する入射角度を制御してもよい。

【産業上の利用可能性】

【0036】

以上のように、本発明によれば、光取り出し効率の改善された窒化物半導体発光ダイオードチップを歩留まりよく提供することができる。

【図面の簡単な説明】

【0037】

【図1】本発明の実施例１によるエピタキシャルウエハから複数のＧａＮ系化合物半導体発光ダイオードチップを分割する方法を図解する模式的断面図である。

【図2】本発明の実施例２によるエピタキシャルウエハから複数のＧａＮ系化合物半導体発光ダイオードチップを分割する方法を図解する模式的断面図である。

【図3】本発明の実施例３によるエピタキシャルウエハから複数のＧａＮ系化合物半導体発光ダイオードチップを分割する一態様を図解する模式的断面図である。

【図4】本発明の実施例３によるエピタキシャルウエハから複数のＧａＮ系化合物半導体

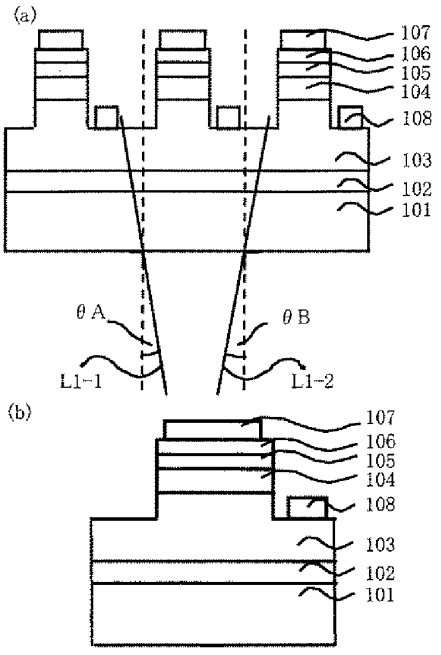
発光ダイオードチップを分割する他の態様を図解する模式的断面図である。

【符号の説明】

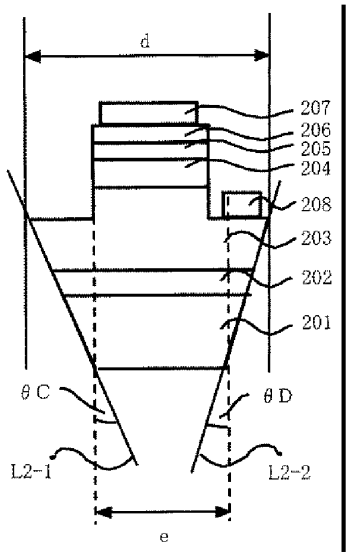
【0038】

１０１、２０１、３０１　サファイア基板、１０２、２０２、３０２　ＧａＮバッファ層、１０３、２０３、３０３　ｎ型ＧａＮコンタクト層、１０４、２０４、３０４　ＭＱＷ活性層、１０５、２０５、３０５　ｐ型ＡｌＧａＮ層、１０６、２０６、３０６　ｐ型ＧａＮコンタクト層、１０７、２０７、３０７　透光性Ｐｄ電極、１０８、２０８、３０８　ｎ側電極、Ｌ１－１、Ｌ１－２、Ｌ２－１、Ｌ２－２、Ｌ３－１、Ｌ３－２　レーザスクライブライン、θＡ、θＢ、θＣ、θＤ、θＥ、θＦ　基板面に垂直な方向に対するレーザ光の進入角度、ｄ、ｆ　半導体積層構造の光放射面側で一辺の長さ、ｅ、ｇ　基板裏面側の一辺の長さ。

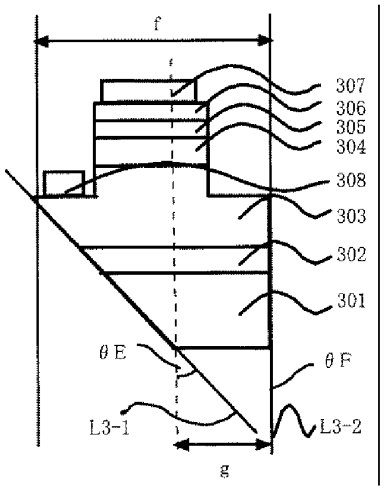
【図1】



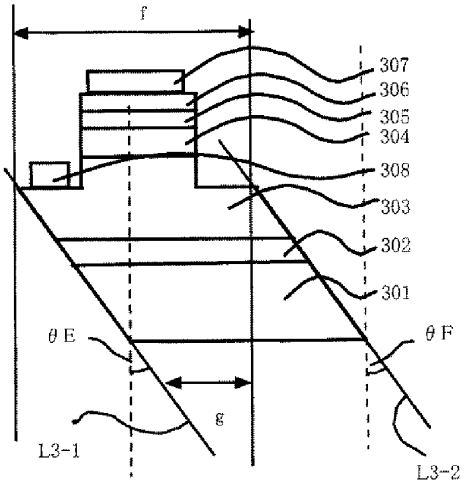
【図2】



【図3】


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【図4】


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(72)発明者　山本　健作
大阪府大阪市阿倍野区長池町２２番２２号　シャープ株式会社内
(72)発明者　幡　俊雄
大阪府大阪市阿倍野区長池町２２番２２号　シャープ株式会社内
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First Named Inventor/Applicant Name:	Jong Lam LEE
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1	Information Disclosure Statement (IDS) Filed (SB/08)	IDS_Transmittal.pdf	944280 691de5fb2bedfa2f29882922300541dd3e5409e6	no	6
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2	NPL Documents	2010-02-01_Office_Action.pdf	649569 acae82a7f2e18257fd3ec313ceeab57926540bae	no	18
Warnings:					
Information:					
3	NPL Documents	2010-02-05_Office_Action.pdf	1161309 6d1cf542cf079a50b1ffbd19f2626d1311aae363	no	31
Warnings:					
Information:					
4	Foreign Reference	JP06-244458.pdf	224920 3be0a9f137d93f40fdbd1b2fd453250dca309a6e	no	5
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58027
H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(**Not for submission under 37 CFR 1.99)**

Application Number	12613275
Filing Date	2009-11-05
First Named Inventor	Jong Lam LEE
Art Unit	2818
Examiner Name	To be assigned
Attorney Docket Number	P2317USD1

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	1	2005008791	WO		2005-01-27	Matsushita Electric Industrial Co., Ltd.		☐
	2	1469529	EP		2004-10-20	Lumileds Lighting US, LLC		☐
	3	2004006582	JP		2004-01-08	Nitride Semiconductor Co Ltd		☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
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	Filing Date	2009-11-05
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	Art Unit	2818
	Examiner Name	To be assigned
	Attorney Docket Number	P2317USD1

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	European Search Report issued February 10, 2010 by the European Patent Office in European Patent Application No. 06769008.1	☐

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Examiner Signature		Date Considered	

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	12613275
	Filing Date	2009-11-05
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	To be assigned
	Attorney Docket Number	P2317USD1

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2010-03-02
Name/Print	Hae-Chan Park	Registration Number	50114

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(11) EP 1 469 529 A2

(12) EUROPEAN PATENT APPLICATION

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(51) Int Cl.[7]: **H01L 33/00**

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(71) Applicant: **Lumileds Lighting U.S., LLC**
San Jose, California 95131 (US)

(72) Inventor: **Martin, Paul, S.**
c/o Lumileds Lighting, U.S., LLC
San Jose, CA 95131 (US)

(74) Representative: **van der Veer, Johannis Leendert**
Philips
Intellectual Property & Standards
P.O. Box 220
5600 AE Eindhoven (NL)

(54) Alternating current light emitting device

(57) A plurality of semiconductor light emitting diodes formed on a single substrate are connected in series for use with an alternating current source. In one embodiment, the series array of light emitting diodes is directly connected to an alternating current source. In other embodiments, the series array of semiconductor light emitting diodes is mounted on a submount with integrated rectifying and filtering circuitry. The submount may be, for example, a silicon integrated circuit. In some embodiments a wavelength converting material is provided over the semiconductor light emitting diodes such that light emitted by the light emitting diodes and light emitted by the wavelength converting material mix to produce while light.

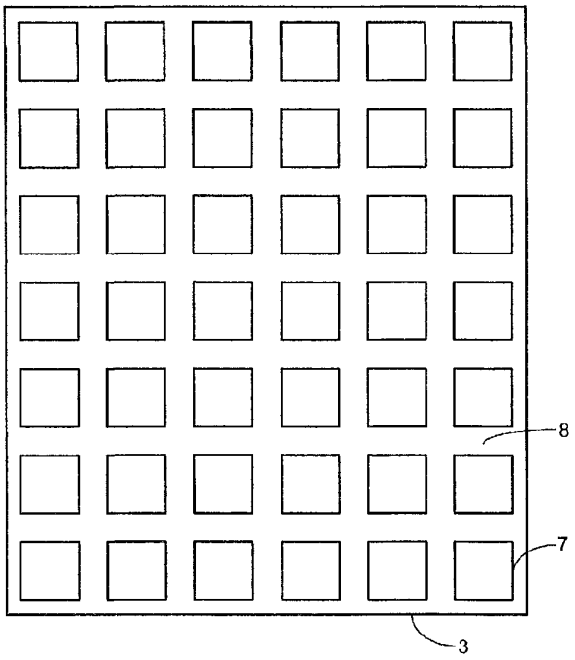


Fig. 1A

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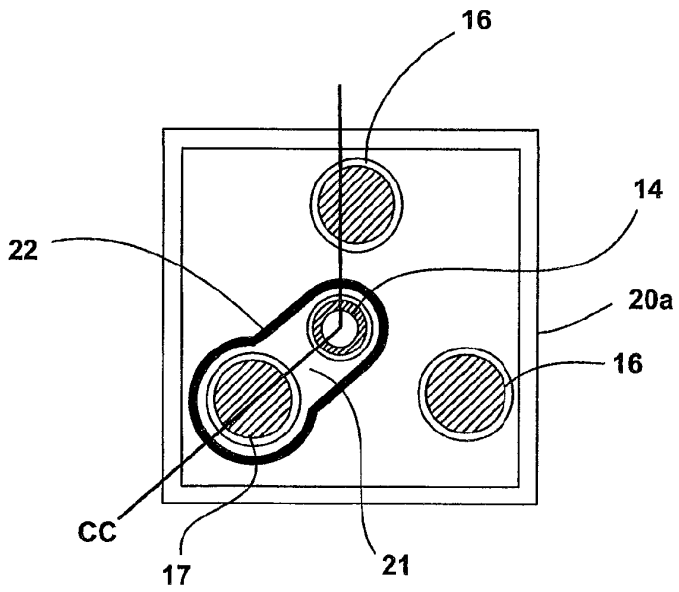


Fig. 1B

NSDOCID: <EP_____1469529A2_I_>

Description

[0001] The present invention relates to monolithic arrays of semiconductor light emitting devices powered by alternating current sources.

[0002] Wojnarowski et al., U.S. Patent 6,412,971, teach an array of separate, individual semiconductor light emitting diodes (LEDs) mounted on a conventional light bulb base for insertion into a residential 120 volt alternating current socket. Wojnarowski et al.'s devices include a rectifier and filter to provide direct current. Direct current provides a constant voltage and current to the array of LEDs, thus the LEDs are constantly on when the array is connected to the alternating current source, eliminating any visible flickering that may have occurred had unfiltered alternating current been used to power the array. Wojnarowski et al.'s devices are bulky and difficult to build and package due to the large number of separate LEDs used and due to the external filtering and rectifying circuitry. The filtering and rectifying circuitry also use power, create heat, and add cost.

[0003] In accordance with embodiments of the invention, a plurality of LEDs formed on a single substrate are connected in series for use with an alternating current source. In one embodiment, the plurality of LEDs are directly connected to an unfiltered and unrectified alternating current source. In other embodiments, the LEDs are mounted on a submount with integrated rectifying and filtering circuitry. The submount may be, for example, a silicon integrated circuit. In some embodiments a wavelength converting material is provided over the LEDs such that light emitted by the LEDs and light emitted by the wavelength converting material mix to produce light with a wavelength distribution different from that emitted by the LEDs.

[0004] Devices without external LED electrical drivers (or with rectifying and filtering circuitry integrated in the submount) offer the advantages of being small and simple to build and package. Such devices may also have reliability and cost advantages.

BRIEF DESCRIPTION OF THE DRAWINGS:

[0005]

Fig. 1A is a plan view of a monolithic array of electrically isolated LEDs.

Fig. 1B is a plan view of a single LED in the array shown in Fig. 1A.

Fig. 2 is a cross-sectional view of the device illustrated in Fig. 1B.

Fig. 3 illustrates a monolithic array of LEDs mounted on a submount.

Figs. 4 and 5 are circuit diagrams of different embodiments of the device of Fig. 3.

Fig. 6 illustrates an embodiment of the invention incorporating a zener diode.

Fig. 7 is an exploded view of a packaged light emitting device.

Fig. 8 is a cross section of a portion of a monolithic array of LEDs mounted on a submount.

Figs. 9 and 10 illustrate packaged devices.

[0006] In accordance with embodiments of the present invention, semiconductor light emitting devices such as light emitting diodes are arranged in monolithic arrays suitable for use with high voltage power sources include those using alternating current. "High voltage" refers to a voltage greater than 10 times the forward voltage of a single LED. For example, some current III-nitride devices operate at a forward voltage of about 3.5 V at a current density of about 50 A/cm^2. Such devices usually fail at current densities greater than 150 A/cm^2. If a single such device were connected to a 120 RMS V alternating current circuit, the peak voltage of about 180 V would far exceed the maximum operating current density. Accordingly, in some embodiments, multiple LEDs are connected in series in order to achieve an appropriate voltage drop and current density for each device when connected to a high voltage power source.

[0007] Fig. 1A is a plan view of a monolithic array of LEDs for use in an alternating current device. An array of individual LEDs 7 are formed on a single substrate 3. The individual LEDs in the array are electrically isolated from each other by, for example, trenches 8 etched between the devices down to substrate 3 or to an insulating layer such as an undoped semiconductor layer.

[0008] Fig. 1B is a plan view of an example of a single small junction III-nitride LED 7 (i.e., an area less than approximately one square millimeter) formed in the monolithic device illustrated in Fig. 1A. In one embodiment, the device in Fig. 1B has an area greater than 300 microns by 300 microns. Fig. 2 is a cross section of the device shown in Fig. 1B, taken along axis CC. As illustrated in Fig. 2, the device includes an n-type region 11, an active region 12, and a p-type region 13 formed over a substrate 15. Each of the n-type region 11, the active region 12, and the p-type region 13 may be, for example, III-nitride semiconductor layers, and each region may contain multiple layers with the same or different characteristics. The substrate may be, for example, sapphire, GaP, Si, or SiC.

[0009] The device shown in Figs. 1B and 2 has a single via 14 etched down to n-type layer 11. An n-contact 21 is deposited in via 14. N-via 14 is located at the center of the device to provide uniformity of current and light emission. A highly reflective p-contact 20 is deposited on p-type layer 13. A thick p-metal layer 20a is deposited over reflective p-contact 20. N-contact 21 is separated from the p-metal layers 20, and 20a by one or more dielectric layers 22. A p-submount connection 16 connects to p-metal layer 20a, and an n-submount connection 17 connects to n-metal layer 21, for connecting the device to a submount. Interconnects 16 and 17 may be, for example, solder bumps.

[0010] As illustrated in Fig. 1B, the device is connect-

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ed to a submount by p-submount connections 16 and n-submount connection 17. N-submount connection 17 may be located anywhere within n-contact region 21 (surrounded by insulating layer 22) and need not be located directly over via 14. Similarly, p-submount connections 16 may be located anywhere on p-metal layer 20a. As a result, the connection of the device to a submount is not limited by the shape or placement of p-contact 20a and n-contact 21.

[0011] Fig. 3 illustrates the monolithic array of Fig. 1A mounted on a submount. Fig. 8 illustrates a cross section of a portion monolithic array mounted on a submount. Array 3 is flipped over and mounted with the contacts closest to submount 2. The dashed lines illustrate the location of each of the individual LEDs 7. The individual LEDs 7 may be separated by a trench 87 as illustrated in Fig. 8. LED array 3 is mounted on submount 2 by electrically and physically connecting interconnects (such as solder bumps 81-84 of Fig. 8) of each LED 7 to submount 2. LED array 3 is therefore mounted in flip chip configuration, such that light is extracted from each of LEDs 7 through the substrate 15 (Fig. 2). In one embodiment, each of the LEDs are connected to each other in series by interconnects within or on the surface of submount 2. Interconnect 86 of Fig. 8, formed on the surface of submount 2, connects solder bumps 82 and 83 of the two LEDs pictured in Fig. 8. Interconnect 85, formed within submount 2, connects solder bump 81 to another LED or other circuitry (not shown). Alternatively, the individual LEDs can be connected by interconnects formed on array 3. Such interconnects are described in more detail in U.S. Patent No. 6,547,249, issued April 15, 2003, titled "Monolithic Series/Parallel LED Arrays Formed On Highly Resistive Substrates," and incorporated herein by reference. In some embodiments, the individual LEDs in array 3 may be interconnected by a combination of interconnects formed on array 3 and interconnects formed on or within submount 2. In embodiments where all or a portion of the interconnects are formed on array 3, only a portion of the LEDs in array 3 may be electrically and physically connected to submount 3.

[0012] Series interconnection reduces the voltage drop across each LED to a level that does not exceed the maximum forward voltage of each LED. Excessive forward voltage can damage the LEDs irreversibly. Bonding pads 4 and 5 are electrically connected to the positive and negative terminals of the array of LEDs and are used to electrically and physically connect the submount to a package. An example of a package is described below in reference to Fig. 7.

[0013] Fig. 3 illustrates a 6 x 7 monolithic array of LEDs mounted on submount 2. The number of LEDs in the monolithic array may be selected to achieve a particular voltage drop across each device. The voltage across each of the individual LEDs in the array is the line voltage divided by the number of LEDs in series. The number of LEDs is chosen such that the maximum voltage across each individual LED during the peak in the alternating current cycle is low enough so as to not damage the LEDs. At 120 RMS volts, the peak voltage will be about 180V. If the individual LEDs illustrated in Figs. 1B and 2 can tolerate a maximum forward voltage of 4.5V, at least 38 LEDs connected in series are required to prevent the voltage across each LED from exceeding the maximum tolerable voltage at the peak of the alternating current cycle. Sources with 240 RMS volts would require twice as many LEDs connected in series, while 60 RMS volt sources would require half as many LEDs connected in series. In some embodiments, the number of LEDs is selected to accommodate common alternating current sources, such as 100V in Japan, 120V in the United States, and 240V in Europe and parts of Asia. For example, for a 120 V alternating current circuit, the peak voltage may be about 180 V. If each of the LEDs in the 6 x 7 array of LEDs illustrated in Fig. 3 has a forward voltage of 3.5 V, each device will achieve the desired current density of 50 A/cm^2 at 3.5 x 42 = 147 V, without exceeding the maximum current density of 150 A/cm^2 at the peak voltage of 180 V. In the embodiment illustrated in Fig. 3, a single monolithic array is mounted on a single submount. In some embodiments, more than one monolithic array may be mounted on one or more submounts, in order to achieve the desired maximum voltage drop across each LED in the arrays.

[0014] Figs. 4 and 5 illustrate two examples of circuits that may be implemented in the device illustrated in Fig. 3. Fig. 4 illustrates a device with an LED array connected in series with an alternating current source, without any rectifying and filtering circuitry for converting the alternating voltage to a direct voltage. The LEDs are only on during that portion of the positive voltage half of each cycle of the alternating current where there is enough voltage to turn on the LEDs. Thus, at 60 Hz, the LEDs turn on 60 times per second.

[0015] Fig. 5 illustrates an LED array and a full wave bridge rectifier for rectifying the alternating current source. The full wave bridge rectifier can be an external component or integrated into the submount, as described below. An optional capacitor filters the rectified voltage to provide nearly direct current to the LED array. Driving the LEDs with a near-direct current source is common and an efficient drive waveform. When the line voltage drops below the turn-on voltage for the LEDs during the alternating current cycle, current is supplied from the capacitor rather than from the line. When the line voltage rises above the turn-on voltage of the LEDs, the capacitor charges. In some embodiments of the invention, rectifying and filtering circuitry, such as the capacitor and full wave bridge rectifier illustrated in Fig. 5, is formed in submount 2 shown in Fig. 3. Submount 2 may be, for example, a silicon chip. The circuitry other than the LED array illustrated in Fig. 5 can be formed on and/or in submount 2 using conventional integrated circuit fabrication techniques.

[0016] In some embodiments of the devices illustrat-

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ed in Figs. 4 and 5, one or more Zener diodes may be included in series with the LED array to control the voltage drop across the LED array, as illustrated in Fig. 6. The Zener diodes may be formed in submount 2. In addition, submount 2 may contain additional circuitry such as electrostatic discharge protection circuitry.

[0017] Fig. 7 is an exploded view of a packaged light emitting device. A heat-sinking slug 100 is placed into a leadframe 105. The leadframe 105 may be, for example, a filled plastic material molded around a metal frame that provides an electrical path. Slug 100 may include an optional reflector cup 102. The light emitting device array and submount 104, which may be any of the devices described herein, is mounted on slug 100. Bonding pads 4 and 5 on submount 2 (Fig. 3) are electrically connected to leads 106 by, for example wire bonding. An optical lens 108 may be added.

[0018] In some embodiments, one or more wavelength converting layers are formed over the LEDs to create white light. For example, blue LEDs may be used with a yellow wavelength converting layer, or with a red wavelength converting layer and a green wavelength converting layer, in order to create white light. Similarly, UV LEDs may be used with red, blue, and green wavelength converting layers to create white light. The wavelength converting layers may be, for example, any suitable phosphors, and may be deposited over each of LEDs 7 in array 3 (Fig. 3) by screen printing or electrophoretic deposition, or suspended in an encapsulant and injected into the space between device 104 and lens 108 in Fig. 7. Individual LEDs in the monolithic array may be covered with different wavelength converting materials.

[0019] Fig. 9 illustrates a monolithic LED array in a package such as an Edison base, designed to be screwed into a conventional light bulb socket. Submount 2 is connected by wire bonds 92 to the contacts in base 91. Base 91 can be screwed into a conventional light bulb socket. A glass bulb 90 may be positioned over base 91. Fig. 10 illustrates a monolithic LED array in a bi-pin base such as an MR16 base, designed to be plugged into a conventional wall socket. Submount 2 is connected by wire bonds 92 to contacts connected to the two prongs of plug 93. In the devices illustrated in Figs. 9 and 10, any necessary circuitry additional to array 3, such as electrostatic discharge protection circuitry, or rectifying and filtering circuitry, may be formed within submount 2.

[0020] Monolithic arrays of LEDs capable of operating with an alternating current source may offer several advantages. First, the use of a single monolithic array on a single submount simplifies building and packaging the device since it is only necessary to align, mount, and connect a single chip to the submount, rather than separate, individual devices. In addition, the lack of rectifying or filtering circuitry (or the integration of rectifying and filtering circuitry into the submount) makes the devices small in size and simple to package, since external driver circuitry is not required. In addition, devices without rectifying and filtering circuitry in particular are simple and inexpensive to fabricate due to the lack of additional circuitry beyond the LED array.

[0021] Having described the invention in detail, those skilled in the art will appreciate that, given the present disclosure, modifications may be made to the invention without departing from the spirit of the inventive concept described herein. For example, though some examples describe III-nitride devices, devices made from other materials systems, such as III-phosphide, III-arsenide, or II-VI materials may be used. Therefore, it is not intended that the scope of the invention be limited to the specific embodiments illustrated and described.

Claims

1. A device comprising:

   a submount; and
   a plurality of light emitting diodes formed on a single substrate, the plurality of light emitting diodes being mounted on the submount and connected in series;

   wherein the plurality of light emitting diodes are directly connected to an alternating current source.

2. The device of claim 1 wherein the plurality of light emitting diodes are connected in series by interconnects formed on a surface of the plurality of light emitting diodes.

3. The device of claim 1 wherein the plurality of light emitting diodes are connected in series by interconnects formed on or in the submount.

4. The device of claim 1 wherein the submount comprises a silicon integrated circuit.

5. The device of claim 1 wherein at least one of the light emitting diodes is a III-nitride light emitting diode.

6. The device of claim 5 wherein the III-nitride light emitting diode comprises a portion of the substrate and a plurality of semiconductor device layers, and wherein the III-nitride light emitting diode is mounted on the submount such that the plurality of semiconductor device layers are closer to the submount than the portion of the substrate.

7. The device of claim 1 further comprising at least one wavelength converting material overlying at least one of the light emitting diodes.

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8. The device of claim 7 wherein light emitted from the light emitting diodes mixed with light emitted from the at least one wavelength converting material appears white.

9. The device of claim 1 further comprising:

a plurality of leads electrically connected to the submount; and a lens overlying the plurality of light emitting devices;

wherein the alternating current source is connected to the plurality of leads.

10. The device of claim 1, wherein alternating current source has a peak voltage of at least 100 volts.

11. The device of claim 1, wherein the alternating current source has an rms voltage of at least 120 volts.

12. The device of claim 1, wherein the submount is connected to a base capable of being connected to a light bulb socket.

13. The device of claim 12, wherein the base is an Edison base.

14. The device of claim 1, wherein the submount is connected to a base capable of being connected to an alternating current outlet socket.

15. The device of claim 14, wherein the base is an MR16 base.

16. A device comprising:

a submount; and
a plurality of light emitting diodes formed on a single substrate, the plurality of light emitting diodes being mounted on the submount and connected in series;
a rectifying and filtering circuit formed in the submount and connected to the plurality of light emitting diodes.

17. The device of claim 16 wherein at least one of the light emitting diodes is a III-nitride light emitting diode.

18. The device of claim 17 wherein the III-nitride light emitting diode comprises a portion of the substrate and a plurality of semiconductor device layers, and wherein the III-nitride light emitting diode is mounted on the submount such that the plurality of semiconductor device layers are closer to the submount than the portion of the substrate.

19. The device of claim 16 further comprising at least one wavelength converting material overlying at least one of the light emitting diodes.

20. The device of claim 19 wherein light emitted from the light emitting diodes mixed with light emitted from the at least one wavelength converting material appears white.

21. The device of claim 16 wherein the rectifying and filtering circuit comprises a capacitor.

22. The device of claim 16 wherein the rectifying and filtering circuit comprises a full wave bridge rectifier.

23. A method of operating a light emitting device, the method comprising:

providing a plurality of semiconductor light emitting diodes formed on a single substrate and connected in series; and
supplying an alternating current source to the plurality of semiconductor light emitting diodes.

24. The method of claim 23 wherein the plurality of semiconductor light emitting diodes are physically mounted on and electrically connected to a submount, and supplying an alternating current source to the plurality of semiconductor light emitting diodes comprises supplying an alternating current source to the submount.

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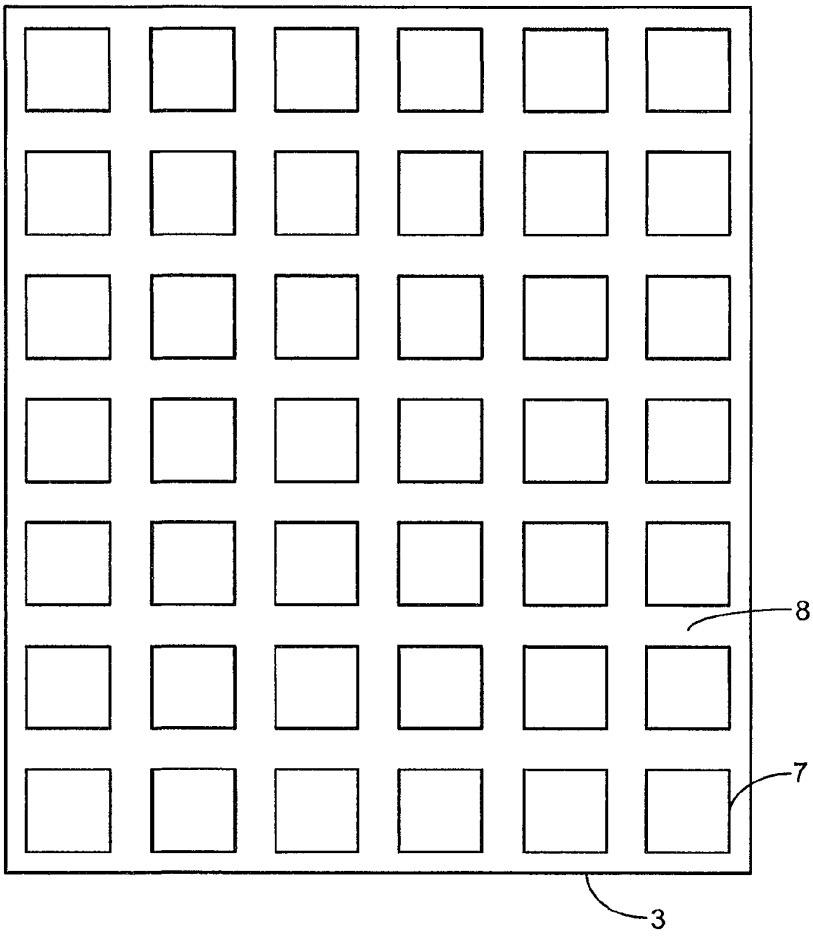


Fig. 1A

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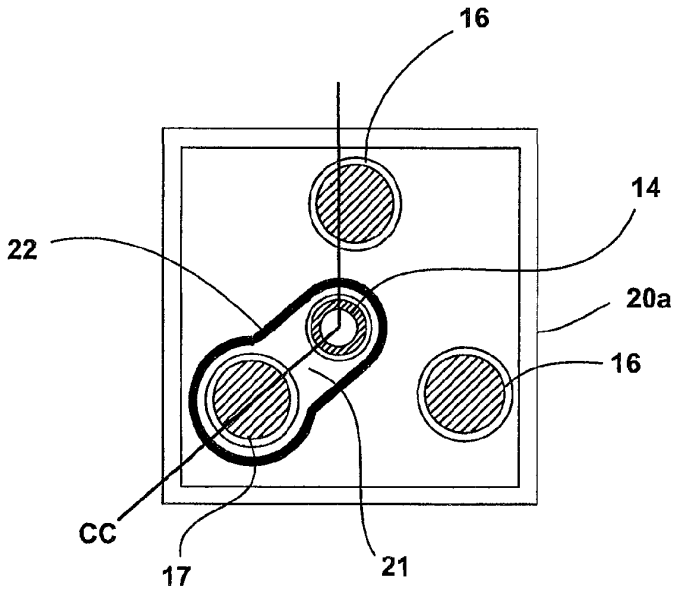


Fig. 1B

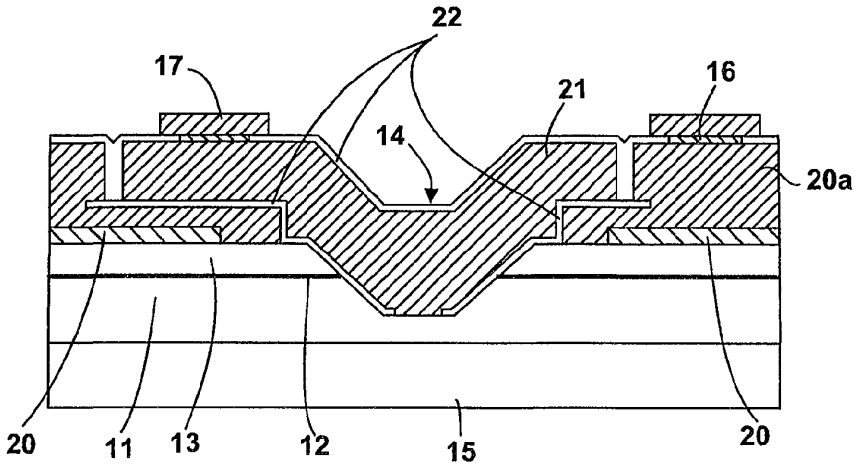


Fig. 2

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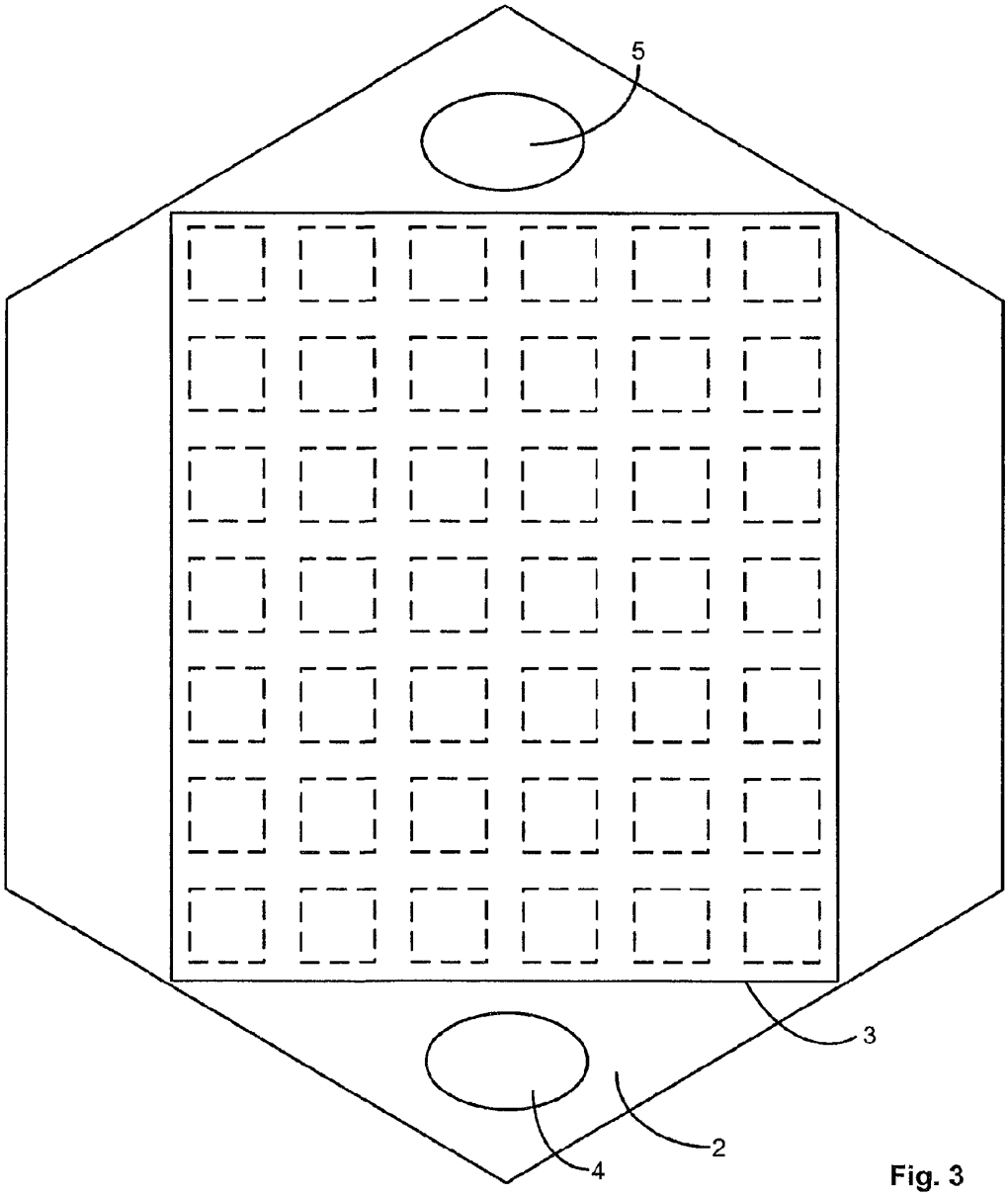


Fig. 3

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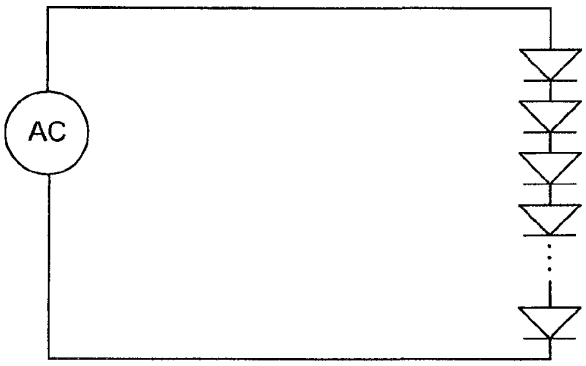


Fig. 4

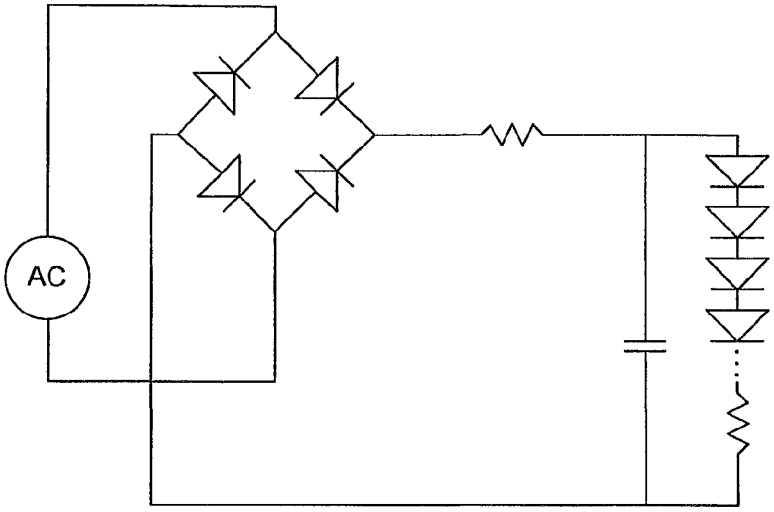


Fig. 5

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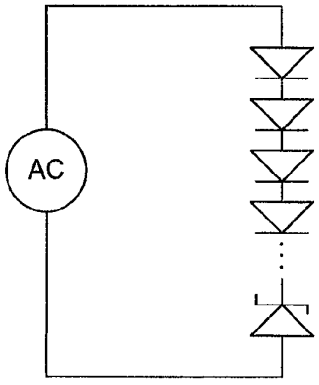


Fig. 6

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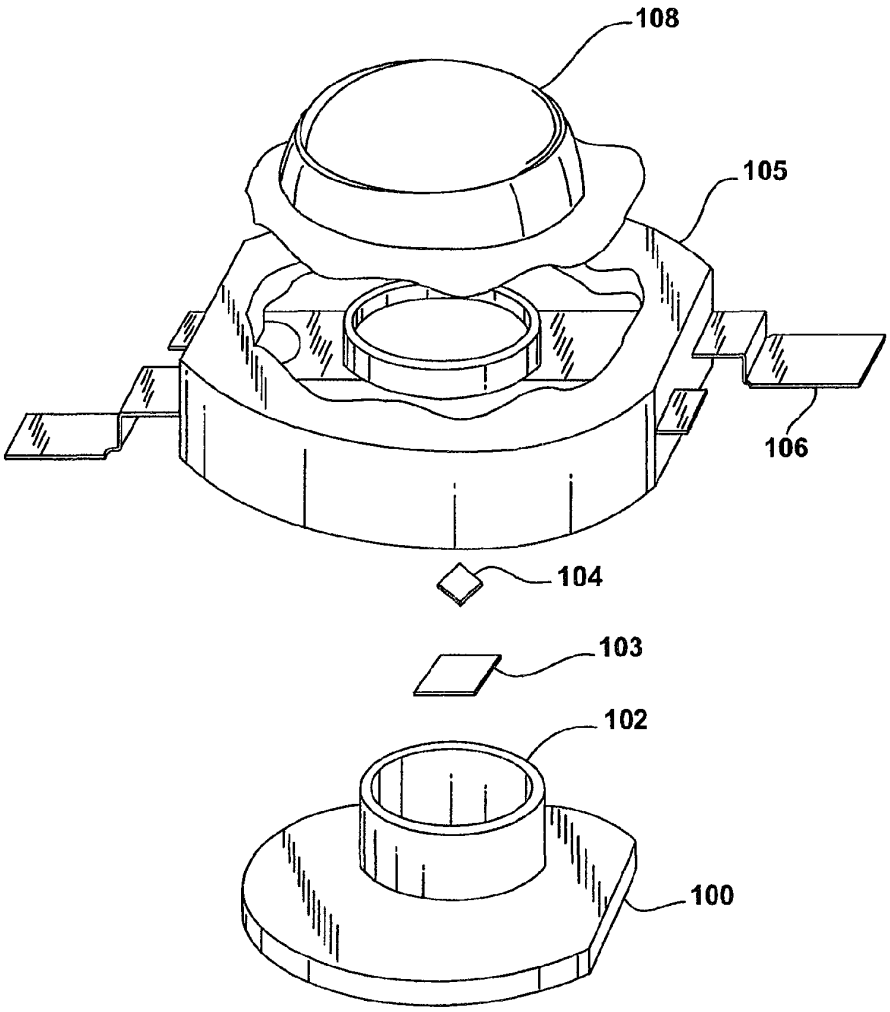


Fig. 7

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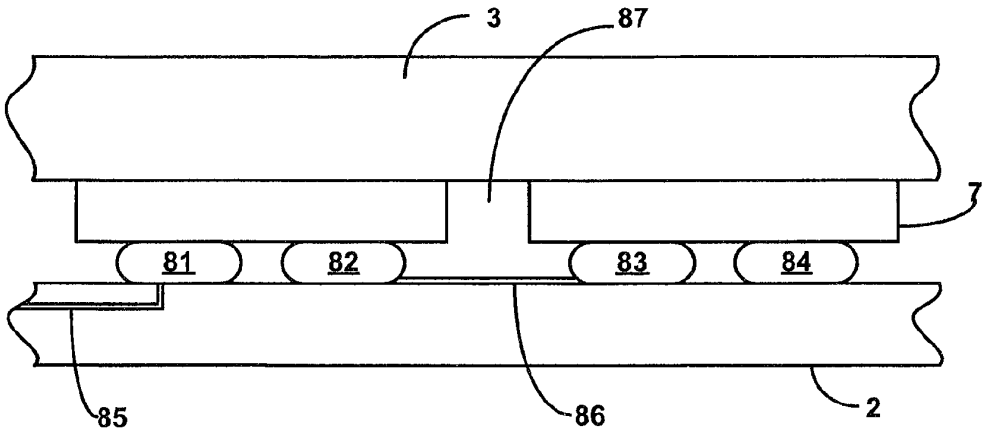


Fig. 8

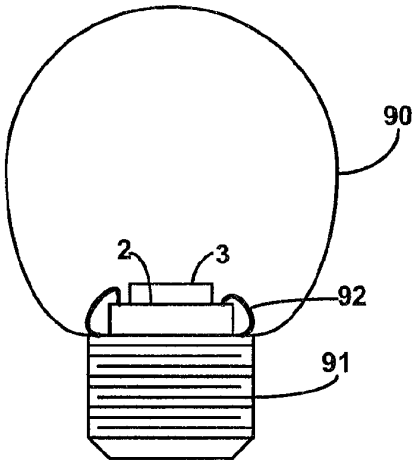


Fig. 9

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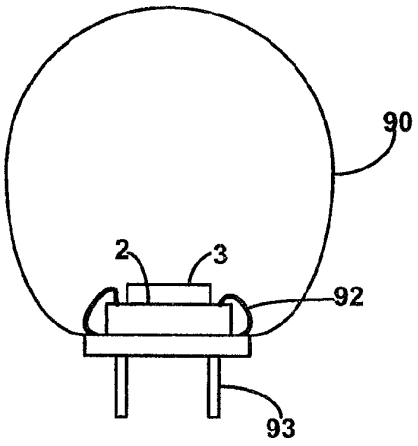


Fig. 10

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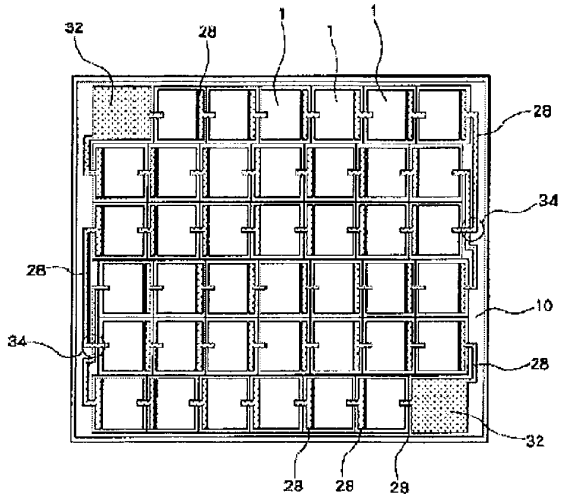
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APPLICATION NUMBER : 2002249957

APPLICANT : NITRIDE SEMICONDUCTOR CO LTD;

INVENTOR : ONO YASUO;

INT.CL. : H01L 33/00

TITLE : LIGHT EMITTING DEVICE



ABSTRACT : PROBLEM TO BE SOLVED: To provide a light emitting device which can be operated with a higher drive voltage and a lower drive current.

SOLUTION: A plurality of LEDs 1 are formed in two dimensions on an insulated substrate 10 such as sapphire with the monolithic formation process and these LEDs are connected in series to form an LED array. Two sets of LED arrays are connected in the reverse polarities to the electrode 32. An air bridge wiring 28 is formed between the LEDs 1 and between the LED 1 and electrode 32. Many LEDs 1 are formed by allocating LED arrays in zig-zag in order to obtain a higher drive voltage and a lower drive current. Since two LED arrays are connected in the reverse polarities, an AC power supply may be used as the power source.

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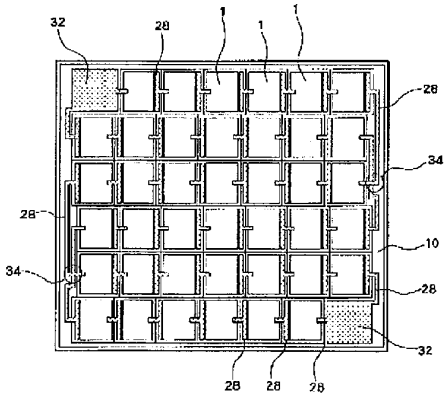
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(71)出願人　591080069
酒井　士郎
徳島県徳島市八万町中津浦１７４－４
(71)出願人　500221563
ナイトライド・セミコンダクター株式会社
徳島県鳴門市瀬戸町明神字板屋島１１５番地の７
(74)代理人　100075258
弁理士　吉田　研二
(74)代理人　100096976
弁理士　石田　純
(72)発明者　酒井　士郎
徳島県徳島市八万町中津浦１７４－４

最終頁に続く

(54)【発明の名称】発光装置

(57)【要約】
【課題】高い駆動電圧、低い駆動電流で動作できる発光装置を提供する。
【解決手段】サファイア等の絶縁基板１０上に複数のＬＥＤ１を二次元的にモノリシック形成し、複数のＬＥＤを直列接続してＬＥＤアレイとする。２組のＬＥＤアレイを互いに逆極性で電極３２に接続する。ＬＥＤ１の間及びＬＥＤ１と電極３２間はエアブリッジ配線２８とする。ＬＥＤアレイをシグザグ状に配置することで多数のＬＥＤ１を形成し、高い駆動電圧と低い駆動電流を得る。２つのＬＥＤアレイは逆極性であるため、電源として交流電源を使用できる。
【選択図】　図6



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【特許請求の範囲】
【請求項1】
絶縁基板上に複数の発光素子が形成され、前記複数の発光素子がモノリシックに直列接続されることを特徴とする発光装置。
【請求項2】
請求項１記載の装置において、
前記複数の発光素子は、前記基板上に二次元配置されていることを特徴とする発光装置。
【請求項3】
請求項１、２のいずれかに記載の装置において、
前記複数の発光素子は２組に分けられ、２個の電極に互いに反対極性となるように並列接続されることを特徴とする発光装置。
【請求項4】
請求項１～３のいずれかに記載の装置において、
前記複数の発光素子間の接続はエアブリッジ配線であることを特徴とする発光装置。
【請求項5】
請求項１～４のいずれかに記載の装置において、
前記複数の発光素子間の電気的な分離は、前記基板として使用されるサファイアにより行われることを特徴とする発光装置。
【請求項6】
請求項２記載の装置において、
前記複数の発光素子は同数ずつ２組に分けられ、各組の発光素子アレイはジグザグ状に配置され、かつ、２組の発光素子アレイは２個の電極に互いに反対極性となるように並列接続されることを特徴とする発光装置。
【請求項7】
請求項６記載の装置において、
前記２組の発光素子アレイは、互い違いに配置されることを特徴とする発光装置。
【請求項8】
請求項６、７のいずれかに記載の装置において、
前記発光素子及び電極は、平面形状が略正方形であることを特徴とする発光装置。
【請求項9】
請求項６、７のいずれかに記載の装置において、
前記発光素子及び電極は、平面形状が三角形状であることを特徴とする発光装置。
【請求項10】
請求項２記載の装置において、
前記複数の発光素子及び電極は、全体形状が略正方形となるように配置されることを特徴とする発光装置。
【請求項11】
請求項１０記載の装置において、
前記複数の発光素子からなる発光素子アレイはジグザグ状に配置されることを特徴とする発光装置。
【請求項12】
請求項６～９のいずれかに記載の装置において、
前記電極は、交流電源用電極であることを特徴とする発光装置。
【請求項13】
請求項６～９のいずれかに記載の装置において、
前記２組の発光素子アレイは、共通のｎ電極を有することを特徴とする発光装置。

【発明の詳細な説明】
【０００１】
【発明の属する技術分野】
本発明は、基板上に複数の発光素子が形成された発光装置に関する。

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【０００２】
【従来の技術】
発光素子（ＬＥＤ）等の発光手段が表示用途等に使用される場合には、その使用条件が駆動電圧約１～４Ｖ、駆動電流が約２０ｍＡとなっている。ところで、近年ＧａＮ系化合物半導体を用いた短波長ＬＥＤが開発され、フルカラーや白色等の固体光源が実用化されたことに伴い、次第にＬＥＤを照明用途にも応用することが検討されている。ＬＥＤを照明用途に応用する場合に、上述した駆動電圧１～４Ｖ、駆動電流２０ｍＡという使用条件とは異なる条件で使用される事態も生じる。このため、ＬＥＤにより大電流を流し、発光出力を大きくする工夫がなされている。大電流を流すためには、ＬＥＤのｐｎ接合面積を大きくし、電流密度を小さく抑える必要がある。
【０００３】
【発明が解決しようとする課題】
ＬＥＤを照明用光源として使用する場合には、電源として交流を使用し、１００Ｖ以上の駆動電圧で使用できることが便利である。また、同じ電力を投入して同じ発光出力を得るのであれば、低い電流値を保ちながら高い電圧を印加した方が電力損失を小さくすることができる。しかし、従来のＬＥＤでは、必ずしも十分に駆動電圧を高くすることはできなかった。
【０００４】
本発明は、上記従来技術の有する課題に鑑みなされたものであり、その目的は、高い駆動電圧で動作できる発光装置を提供することにある。
【０００５】
【課題を解決するための手段】
上記目的を達成するために、本発明は、絶縁基板上に複数の発光素子が形成され、前記複数の発光素子がモノリシックに直列接続されることを特徴とする。
【０００６】
ここで、前記複数の発光素子は、前記基板上に二次元配置されていることが好適である。
【０００７】
また、前記複数の発光素子は２組に分けられ、２個の電極に互いに反対極性となるように並列接続されることが好適である。
【０００８】
前記複数の発光素子間の接続はエアブリッジ配線とすることが好適である。
【０００９】
前記複数の発光素子間の電気的な分離は、前記基板として使用されるサファイアにより行われることが好適である。
【００１０】
また、前記複数の発光素子は同数ずつ２組に分けられ、各組の発光素子アレイはジグザグ状に配置し、かつ、２組の発光素子アレイは２個の電極に互いに反対極性となるように並列接続されることも好適であり、前記２組の発光素子アレイは、互い違いに配置することができる。
【００１１】
また、前記発光素子及び電極は、平面形状が略正方形あるいは三角形状とすることが好適である。
【００１２】
また、前記複数の発光素子及び電極は、全体形状が略正方形となるように配置されることが好適である。
【００１３】
本発明において、電極は、交流電源用電極とすることができる。
【００１４】
また、前記２組の発光素子アレイは、共通のｎ電極を有することが好適である。
【００１５】

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このように、本発明では複数の発光素子をモノリシックに、すなわち同一基板上に形成し、これらを直列接続することで、高駆動電圧を可能とする。複数の発光素子を一方向に接続することで直流駆動が可能となるが、複数の発光素子を２組に分け、各組の発光素子（発光素子アレイ）を互いに逆極性となるように電極に接続することで交流駆動も可能となる。各組の個数は同数でもよく、あるいは異なっていてもよい。

【００１６】

複数の発光素子を二次元配列する方法は種々存在するが、基板専有面積をできるだけ小さくすることが望ましい。例えば、２組の発光素子アレイをそれぞれジグザグ状に、すなわち複数の発光素子を折れ曲がった直線上に配置し、それぞれの発光素子アレイを互い違いに配置することで、基板面積を有効活用して多数の発光素子を接続することができる。２組の発光素子アレイを互い違いに配置することで、配線の交叉部分が生じる場合もあるが、発光素子間をエアブリッジ配線で接続することにより交叉部分での短絡を有効に防止できる。発光素子及び電極の形状は任意であるが、例えば平面形状が略正方形となるように形成することで全体形状も略正方形となり、標準的なマウント構造を使用できる。発光素子及び電極を正方形以外、例えば三角形とした場合でも、これらの三角形状を組み合わせることで全体として略正方形を形成すれば、同様に標準的なマウント構造を使用できるようになる。

【００１７】

【発明の実施の形態】

以下、図面に基づき本発明の実施形態について説明する。

【００１８】

図１には、本実施形態においてＧａＮ系化合物半導体発光素子としてのＬＥＤ１の基本構成が示されている。ＬＥＤ１は、基板１０上に順次ＧａＮ層１２、Ｓｉドープのｎ型ＧａＮ層１４、ＩｎＧａＮ発光層１６、ＡｌＧａＮ層１８、ｐ型ＧａＮ層２０が積層され、ｐ型ＧａＮ層２０に接してｐ電極２２、ｎ型ＧａＮ層１４に接してｎ電極２４が形成される構成である。

【００１９】

図１に示されたＬＥＤは以下のプロセスにより作製される。すなわち、まず、ＭＯＣＶＤ装置にてサファイアｃ面基板を水素雰囲気中で１１００℃、１０分間熱処理する。そして、温度を５００℃まで降温させ、シランガスとアンモニアガスを１００秒間供給して不連続なＳｉＮ膜を基板１０上に形成する。なお、このプロセスはデバイス中の転位密度を低減させるためのものであり、図ではＳｉＮ膜は省略している。次に、同一温度でトリメチルガリウム及びアンモニアガスを供給してＧａＮ層を２０ｎｍ厚成長させる。温度を１０５０℃に昇温し、再びトリメチルガリウム及びアンモニアガスを供給してアンドープＧａＮ（ｕ－ＧａＮ）層１２及びＳｉドープのｎ型ＧａＮ層１４を各２μｍ厚成長させる。その後、温度を７００℃程度まで降温してＩｎＧａＮ発光層１６を２ｎｍ厚成長させる。目標組成はｘ＝０．１５、すなわち$In_{0.15}Ga_{0.85}N$である。発光層１６成長後、温度を１０００℃まで昇温してＡｌＧａＮ正孔注入層１８を成長させ、さらにｐ型ＧａＮ層２０を成長させる。

【００２０】

ｐ型ＧａＮ層２０を成長させた後、ウエハをＭＯＣＶＤ装置から取り出し、Ｎｉ１０ｎｍ厚、Ａｕ１０ｎｍ厚を順次真空蒸着で成長層表面に形成する。５％の酸素を含む窒素ガス雰囲気中で５２０℃熱処理することで金属膜はｐ型透明電極２２となる。透明電極形成後、全面にフォトレジストを塗布し、ｎ型電極形成のためのエッチングをフォトレジストをマスクとして行う。エッチング深さは、例えば６００ｎｍ程度である。エッチングで露出したｎ型ＧａＮ層１４上にＴｉ１５ｎｍ厚、Ａｌ１５ｎｍ厚を形成し、窒素ガス雰囲気中で４５０℃、３０分間熱処理してｎ型電極２４を形成する。最後に、基板１０の裏面を１００μｍまで研磨してチップを切り出し、マウントすることでＬＥＤ１が得られる。

【００２１】

図１では、基板１０上に一つのＬＥＤ１が形成されているが、本実施形態では、基板１０

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上にＬＥＤ１をモノリシックに、かつ二次元アレイ状に複数形成し、各ＬＥＤを接続して発光装置（チップ）を構成する。

【００２２】

図２には、発光装置の等価回路図が示されている。図２において、２次元アレイ状に形成された発光素子群は同数（図では４個）ずつ２組に分けられ、各組のＬＥＤ１はそれぞれ直列接続され、２組のＬＥＤ列は電極（駆動電極）に対して逆極性となるように並列接続される。このようにＬＥＤ列が直列接続されることにより、各々の駆動電圧が加算された高い電圧でＬＥＤ１を駆動することができる。また、各ＬＥＤ列はその極性が互いに反対となるように電極に並列接続されているので、電源として交流電源を使用した場合にも、電源の各周期中に必ずどちらかのＬＥＤ列が発光していることになるので、効率のよい発光を行うことができる。

【００２３】

図３には、基板１０上にモノリシックに形成された複数のＬＥＤの部分的な平面図が示されている。また、図４は、図３のＩＶ－ＩＶ断面図が示されている。図３において、ＬＥＤ１の上面には、図１に示されるようにｐ電極２２及びｎ電極２４が形成されている。隣接するＬＥＤ１のｐ電極２２とｎ電極２４との間がエアブリッジ配線２８により接続され、複数のＬＥＤ１が直列接続される。

【００２４】

図４において、各ＬＥＤ１は説明の都合上簡略的に示されている。すなわち、ｎ－ＧａＮ層１４、ｐ－ＧａＮ層２０、ｐ－電極２２、ｎ－電極２４のみが示されている。実際には図１に示されるようにＩｎＧａＮ発光層１６等が存在することは云うまでもない。エアブリッジ配線２８は、ｐ電極２２からｎ電極２４までを空中を介して接続する。これにより、素子表面に絶縁膜を塗布し、この上に電極を形成してｐ電極２２とｎ電極２４とを電気的に接続する方法に比べ、エッチング溝に沿って電極を配置する必要が無くなるので、配線切れや絶縁膜からｎ層、ｐ層へ絶縁材料を構成する元素が熱拡散してＬＥＤ１を劣化させるという問題を回避できる。エアブリッジ配線２８は、ＬＥＤ１間のみならずＬＥＤ１と図示しない電極との間の接続にも使用される。

【００２５】

また、図４に示されるように、各ＬＥＤ１は互いに独立し、電気的に絶縁される必要がある。このため、各ＬＥＤ１はサファイア基板１０上で分離された構成となっている。サファイアはそれ自身絶縁体であるので、ＬＥＤ１をそれぞれ電気的に分離することができる。このように、サファイア基板１０をＬＥＤの電気的な分離を行うための抵抗体として使用することにより、容易かつ確実にＬＥＤの電気的な分離を行うことができる。

【００２６】

なお、発光素子としては、ｐｎ接合を有するＬＥＤの他、ＭＩＳとすることもできる。

【００２７】

図５には、発光装置の他の等価回路図が示されている。図において、２０個のＬＥＤ１が直列接続されて１つのＬＥＤアレイを形成しており、２つのＬＥＤアレイ（合計４０個のＬＥＤ）が電源に並列に接続されている。ＬＥＤ１の駆動電圧は５Ｖに設定されており、各ＬＥＤアレイの駆動電圧は１００Ｖとなっている。２つのＬＥＤアレイは図２と同様に互いに反対極性となるように電源に並列接続されており、電源の極性がいずれであっても必ずどちらかのＬＥＤアレイが発光することになる。

【００２８】

図６には、二次元アレイが具体的に示されている。図２の等価回路図に対応するものである。図において、サファイア基板１０上に合計４０個のＬＥＤ１が形成されており、それぞれ２０個ずつ２組に分けられ、エアブリッジ配線２８により直列接続されて２つのＬＥＤアレイを形成している。より詳細には、各ＬＥＤ１は全て同形の正方形で同サイズであり、１つのＬＥＤアレイは上から６個、７個、７個とそれぞれ直線上に配置され、上から第１列目（６個）と第２列目（７個）は互いに逆向きに形成され、第２列目と第３列目も互いに逆向きに形成される。第１列目と第２列目、第２列目と第３列目は互いに離間して

配置されている。これは、後述するように他方のＬＥＤアレイの列が交互に挿入されるためである。第１列目の右端のＬＥＤ１と第２列目の右端のＬＥＤ１とはエアブリッジ配線２８により接続される。第２列目の左端のＬＥＤ１と第３列目の左端のＬＥＤ１もエアブリッジ配線２８で接続されてジグザグ配列となる。第１列目の左端のＬＥＤ１は基板１０の左上部に形成された電極（パッド）３２にエアブリッジ配線２８で接続され、第３列目の右端のＬＥＤ１は基板１０の右下部に形成された電極（パッド）３２にエアブリッジ配線２８で接続される。２つの電極（パッド）３２もＬＥＤ１と同形の正方形である。他方のＬＥＤアレイは上述した一方のＬＥＤアレイの間隙に互い違いとなるように形成される。すなわち、他方のＬＥＤアレイは上から７個、７個、６個とそれぞれ直線上に配置され、上から第１列目は一方のＬＥＤアレイの第１列目と第２列目の間に形成され、第２列目は一方のＬＥＤアレイの第２列目と第３列目の間に形成され、第３列目は一方のＬＥＤアレイの第３列目の下に形成される。他方のＬＥＤアレイの第１列目と第２列目、及び第２列目と第３列目も互いに逆方向となるように形成され、第１列目の右端のＬＥＤ１は第２列目の右端のＬＥＤ１にエアブリッジ配線２８で接続され、第２列目の左端のＬＥＤ１は第３列の左端のＬＥＤ１にエアブリッジ配線２８で接続されてジグザグ状となる。他方のＬＥＤアレイの第１列目の左端のＬＥＤは基板１０の左上部に形成された電極３２にエアブリッジ配線２８で接続され、第３列目の右端のＬＥＤ１は基板１０の右下部に形成された電極３２にエアブリッジ配線２８で接続される。一方のＬＥＤアレイと他方のＬＥＤアレイの電極３２に対する極性は互いに逆である。発光装置（チップ）の全体形状は長方形である。電源が供給される２つの電極３２は、長方形の対角位置に離間して形成される点も着目されたい。

【００２９】

図７には、図６の回路図が示されている。それぞれのＬＥＤアレイはジグザグ状に屈曲しつつ直列接続され、２つのＬＥＤアレイはジグザグ状の各列が互いの列の間に形成される様子が明らかとなろう。このような配置とすることで、多数のＬＥＤ１を小さな基板１０上に配置することができる。また、４０個のＬＥＤ１に対して電極３２が２個でよいので、この点でも基板１０の使用効率を向上させることができる。また、各ＬＥＤ１を分離するためにＬＥＤ１を個別に形成する場合にはウエハをカットして分離する必要があるのに対し、本実施形態では各ＬＥＤ１の分離をエッチングで行うことができるので、ＬＥＤ１の間隔を狭くすることができる。これにより、サファイア基板１０の大きさをより小さくすることができる。ＬＥＤ１同士の分離は、フォトレジストや反応性イオンエッチング、ウエットエッチングを併用することでＬＥＤ１以外の領域を基板１０に達するまでエッチング除去することで達成される。各ＬＥＤアレイは交互に発光するので、発光効率を向上できるとともに放熱特性も向上させることができる。また、直列接続させるＬＥＤ１の数を変更すれば、全体としての駆動電圧も変更できる。また、ＬＥＤ１の面積を小さくすると、１つのＬＥＤ当たりの駆動電圧を高くすることもできる。ＬＥＤ１を２０個直列に接続した場合、商用電源（１００Ｖ、６０Ｈｚ）で駆動すると、およそ１５０ｍＷの発光出力を得ることができる。この場合の駆動電流としては２０ｍＡ程度である。

【００３０】

なお、図７から分かるように、２つのＬＥＤアレイをジグザグ状に交互に配列する場合、エアブリッジ配線２８に交叉部分３４が必然的に発生する。例えば、他方のＬＥＤアレイの第１列目と第２列目を接続する際に、一方のＬＥＤアレイの第１列目と第２列目を接続するための配線部分と交叉する。しかし、本実施形態のエアブリッジ配線２８は、上述したように基板１０に接着しておらず、基板１０から離れて空中を通過するので、交叉部分３４においてエアブリッジ配線２８同士が接触し、短絡することを容易に回避することができる。エアブリッジ配線２８を用いる利点の一つである。エアブリッジ配線２８は、例えば以下のようにして形成される。すなわち、全面に２μｍの厚さのフォトレジストを塗布し、エアブリッジ配線の形状に穴を開けた後にポストベークする。その上に、真空蒸着でＴｉを１０ｎｍ、Ａｕを１０ｎｍ、この順序で蒸着する。さらにその上の全面に２μｍ厚さでフォトレジストを再度塗布し、エアブリッジ配線を形成する部分のみに穴を開ける

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。次いで、ＴｉとＡｕを電極として電解液中でイオンプレーティング（メッキ）により電極全面に３～５μｍの厚さのＡｕを付着させる。その後、試料をアセトンに浸し、超音波洗浄によりフォトレジストを溶解除去してエアブリッジ配線２８が完成する。

【００３１】

このように、複数のＬＥＤ１を二次元アレイ状に配置することで、基板面積を有効に活用しつつ高駆動電圧、特に商用電源での駆動も可能となるが、二次元アレイのパターンとしてはこの他にも種々のパターンが可能である。一般に、二次元アレイパターンとしては、以下の条件を備えることが望ましい。

【００３２】

（１）各ＬＥＤに均一に電流を流し、均一な発光を得るためには各ＬＥＤの形状、電極位置が同一であることが望ましい。

【００３３】

（２）ウエハをカットしてチップにするためには、各ＬＥＤの辺は直線であることが望ましい。

【００３４】

（３）光取り出し効率を向上させるため、標準的なマウントを使用して周辺からの反射を利用するためにはＬＥＤは平面形状が正方形に近い形状が望ましい。

【００３５】

（４）２つの電極（ボンディングパット）の大きさは１００μｍ角程度で、互いに離れていることが望ましい。

【００３６】

（５）ウエハ面積の有効利用のため、配線、パッドの占める割合は小さい方が望ましい。

【００３７】

もちろん、これらは必須ではなく、例えば各ＬＥＤの形状としては平面形状三角形を用いることも可能であろう。各ＬＥＤの形状が三角形であっても、これらを組み合わせることで全体形状を略正方形とすることができる。以下、二次元アレイパターンの例をいくつか示す。

【００３８】

図８には、合計６個のＬＥＤ１を二次元に配置した例が示されており、図９にはその回路図が示されている。図８の配置は、基本的には図６の配置と同様であり、合計６個のＬＥＤアレイは同数ずつ２組に分けられ、それぞれ直列接続された３個のＬＥＤから構成される。一方のＬＥＤアレイはジグザグ状に配列され、上から第１列目は１個のＬＥＤ１、第２列目は２個のＬＥＤ１が形成される。第１列目のＬＥＤと第２列目の右端のＬＥＤ１はエアブリッジ配線２８で直列接続され、第２列目の２個のＬＥＤ１もエアブリッジ配線２８で直列接続される。基板１０の左上部と左下部に電極（パッド）３２が形成され、第１列目のＬＥＤ１は左上部の電極３２にエアブリッジ配線で接続され、第２列目の左端のＬＥＤ１は左下部の電極３２に接続される。他方のＬＥＤアレイもジグザグ状に配列され、上から第１列目は２個のＬＥＤ１、第２列目は１個のＬＥＤ１が形成される。他方のＬＥＤアレイの第１列目は前記一方のＬＥＤアレイの第１列目と第２列目の間に形成され、他方のＬＥＤアレイの第２列目は前記一方のＬＥＤアレイの第２列目の下方に形成される。第１列目の右端のＬＥＤ１は第２列目のＬＥＤ１にエアブリッジ配線２８で直列接続され、第１列目の２個のＬＥＤ１同士もエアブリッジ配線２８で直列接続される。第１列目の左端のＬＥＤ１は左上部の電極３２にエアブリッジ配線２８で接続され、第２列目のＬＥＤ１は左下部の電極３２にエアブリッジ配線２８で接続される。図９から分かるように、この例でも２つのＬＥＤアレイは互いに並列に電極３２に接続され、かつ、互いに逆極性となるように接続される。したがって、交流電源を供給した場合、２つのＬＥＤアレイは交互に発光することになる。

【００３９】

図１０には、合計１４個のＬＥＤを二次元配置した例が示されており、図１１にはその回路図が示されている。合計１４個のＬＥＤアレイは２組に分けられ、それぞれ直列接続さ

れた７個のＬＥＤから構成される。一方のＬＥＤアレイはジグザグ状に配列され、上から第１列目は３個のＬＥＤ１、第２列目は４個のＬＥＤ１が形成される。第１列目の左端のＬＥＤと第２列目の左端のＬＥＤ１はエアブリッジ配線２８で直列接続され、第１列目の３個のＬＥＤ同士、及び第２列目の４個のＬＥＤ１同士もエアブリッジ配線２８で直列接続される。基板１０の右上部と右下部に電極（パッド）３２が形成され、第１列目の右端のＬＥＤ１は右上部の電極３２にエアブリッジ配線で接続され、第２列目の右端のＬＥＤ１は右下部の電極３２に接続される。他方のＬＥＤアレイもジグザグ状に配列され、上から第１列目は４個のＬＥＤ１、第２列目は３個のＬＥＤ１が形成される。他方のＬＥＤアレイの第１列目は前記一方のＬＥＤアレイの第１列目と第２列目の間に形成され、他方のＬＥＤアレイの第２列目は前記一方のＬＥＤアレイの第２列目の下方に形成される。第１列目の左端のＬＥＤ１は第２列目の左端のＬＥＤ１にエアブリッジ配線２８で直列接続される。第１列目の４個のＬＥＤ１同士、及び第２列目の３個のＬＥＤ１同士も直列接続される。第１列目の右端のＬＥＤ１は右上部の電極３２にエアブリッジ配線２８で接続され、第２列目の右端のＬＥＤ１は右下部の電極３２にエアブリッジ配線２８で接続される。図１１から分かるように、この例でも２つのＬＥＤアレイは互いに並列に電極３２に接続され、かつ、互いに逆極性となるように接続される。したがって、交流電源を供給した場合、２つのＬＥＤアレイは交互に発光することになる。

【００４０】

図６、図８、図１０の二次元パターンに共通する特徴としては、各ＬＥＤ１が略正方形の同形、同サイズであること、２つの電極（パッド）も略正方形であり、隣接形成されていない（離間形成されている）こと、２つのＬＥＤアレイの組み合わせであること、２つのＬＥＤアレイは屈曲しつつチップ上に互いに交錯するように形成されること、２つのＬＥＤアレイは互いに逆極性となるように電極に接続されること、等である。

【００４１】

図１２には、平面形状が三角形のＬＥＤを二次元配列した場合の例が示されており、図１３にはその回路図が示されている。図１２において、合計６個のＬＥＤ１ａ、１ｂ、１ｃ、１ｄ、１ｅ、１ｆがその平面形状が三角形状となるように形成されている。ＬＥＤ１ａとＬＥＤ１ｅが三角形の一辺で対向して２つで略正方形となるように配置され、ＬＥＤ１ｂと１ｆが対向して２つで略正方形となるように配置される。また、ＬＥＤ１ｄと電極３２が対向して接続し、ＬＥＤ１ｃと電極３２が対向して接続する。２つの電極３２もＬＥＤと同様に平面形状が三角形状であり、同様に略正方形となるように配置される。ＬＥＤ同士の対向する辺はｎ電極２４を構成し、すなわち、対向する２つのＬＥＤはｎ電極２４を共有する。ＬＥＤと電極３２もｎ電極接続である。この配置も、上述した例と同様に合計６個のＬＥＤは２組に分けられる。一方のＬＥＤアレイは、ＬＥＤ１ａ、ＬＥＤ１ｂ、ＬＥＤ１ｃからなるアレイであり、ＬＥＤ１ａのｐ電極２２は電極３２にエアブリッジ配線２８で接続され、そのｎ電極２４はＬＥＤ１ｂのｐ電極２２とエアブリッジ配線２８で接続される。ＬＥＤ１ｂのｎ電極２４はＬＥＤ１ｃのｐ電極２２とエアブリッジ配線２８で接続される。ＬＥＤ１ｃのｎ電極２４は電極３２に接続される。他方のＬＥＤアレイは、ＬＥＤ１ｄ、ＬＥＤ１ｅ、ＬＥＤ１ｆから構成され、電極３２とＬＥＤ１ｆのｐ電極２２はエアブリッジ配線２８で接続され、ＬＥＤ１ｆのｎ電極２４はＬＥＤ１ｅのｐ電極２２とエアブリッジ配線２８で接続され、ＬＥＤ１ｅのｎ電極２４とＬＥＤ１ｄのｐ電極２２はエアブリッジ配線２８で接続され、ＬＥＤ１ｄのｎ電極２４は電極３２に接続される。

【００４２】

図１３において、一方のＬＥＤアレイを構成するＬＥＤ１ａと他方のＬＥＤアレイを構成するＬＥＤ１ｅのｎ電極が接続されており、一方のＬＥＤアレイを構成するＬＥＤ１ｂと他方のＬＥＤアレイを構成するＬＥＤ１ｆのｎ電極が接続されている点にも着目されたい。２組のＬＥＤアレイのいくつかのｎ電極を共有することで、回路配線を削減することができる。また、この例においても、２つのＬＥＤアレイは並列に電極３２に接続され、かつ、互いに逆極性となるように接続される。また、各ＬＥＤは同形、同サイズであり、各

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ＬＥＤを一つの辺で対向させるとともに電極３２も三角形状とすることでＬＥＤ及び電極を高密度に形成して必要な基板面積を小さくすることができる。

【００４３】

図１４には、平面形状が三角形のＬＥＤを二次元配列した他の例が示されており、図１５にはその回路図が示されている。この例では、合計１６個のＬＥＤ１ａ～１ｒが二次元形成されている。ＬＥＤ１ａと１ｊ、１ｂと１ｋ、１ｃと１ｍ、１ｄと１ｎ、１ｅと１ｐ、１ｆと１ｑ、１ｇと１ｒがそれぞれ三角形の一つの辺で対向する。対向する辺にはｎ電極２４が共通形成されている。また、ＬＥＤ１ｉと電極３２が対向し、ＬＥＤ１ｈと電極３２が対向する。一方のＬＥＤアレイはＬＥＤ１ａ、１ｂ、１ｃ、１ｄ、１ｅ、１ｆ、１ｇ、１ｈから構成され、他方のＬＥＤアレイはＬＥＤ１ｒ、１ｑ、１ｐ、１ｎ、１ｍ、１ｋ、１ｊ、１ｉから構成される。ＬＥＤ１ｂのｎ電極２４はエアブリッジ配線２８によりＬＥＤ１ｃのｐ電極２２に接続され、ＬＥＤ１ｅのｎ電極２４もエアブリッジ配線２８によりＬＥＤ１ｆのｐ電極２２に接続される。また、ＬＥＤ１ｑのｎ電極２４もエアブリッジ配線２８によりＬＥＤ１ｐのｐ電極２２に接続され、ＬＥＤ１ｍのｎ電極２４もエアブリッジ配線２８によりＬＥＤ１ｋのｐ電極２２に接続される。図１４においても、図１２と同様に交叉部分が生じるが、エアブリッジ配線２８により短絡を回避できる。また、この例においても２組のＬＥＤアレイのいくつかのｎ電極２４を共有構造とすることで必要な配線を削減している。また、この例においても２つのＬＥＤアレイは並列で互いに逆極性で電極３２に接続されており、交流駆動が可能である。図１２においては合計６個のＬＥＤの場合、図１４においては合計１６個のＬＥＤの場合について示したが、他の個数のＬＥＤでも同様に二次元配列できる。本願出願人は、３８個のＬＥＤを二次元配列した発光装置も作成している。

【００４４】

以上、交流駆動の場合について説明したが、直流駆動も可能であることは言うまでもない。この場合、ＬＥＤアレイを互いに逆極性となるように電極に接続するのではなく、直流電源の極性の向きに合わせてＬＥＤアレイを順方向に接続すればよい。複数のＬＥＤを直列接続することで、高電圧駆動が可能である。以下、直流駆動の場合についても説明する。

【００４５】

図１６には、２個のＬＥＤを直列接続した例が示されており、図１７にはその回路図が示されている。各ＬＥＤ１は平面形状が矩形状であり、２個のＬＥＤ間はエアブリッジ配線２８で接続される。電極３２は各ＬＥＤ１の近傍に形成されており、電極３２とＬＥＤ１とで長方形の領域を形成する。すなわち、電極３２は長方形領域の一部を占有し、長方形領域の他の領域にＬＥＤ１が形成されている。

【００４６】

図１８には、合計４個のＬＥＤを二次元配列した例が示されており、図１９にはその回路図が示されている。図１６のＬＥＤ１を２個に分割し、それぞれを並列に接続したものである。２個のＬＥＤからなるＬＥＤアレイを２組並列に順方向接続したと云うこともできる。ＬＥＤ１ａと１ｂで一つのＬＥＤアレイを構成し、ＬＥＤ１ｃと１ｄでもう一つのＬＥＤアレイを構成する。ＬＥＤ１ａとＬＥＤ１ｃはｐ電極２２及びｎ電極２４を共有し、ＬＥＤ１ｂとＬＥＤ１ｄもｐ電極２２及びｎ電極２４を共有する。この構成によれば、図１６に比べて電流が均一化する効果がある。

【００４７】

図２０は、合計３個のＬＥＤを二次元配列した例が示されており、図２１にはその回路図が示されている。ＬＥＤ１ａ、１ｂ、１ｃは同形ではなく、ＬＥＤ１ａの一部に電極３２が形成されている。ＬＥＤ１ａのｎ電極２４とＬＥＤ１ｂのｐ電極はＬＥＤ１ｂの上を跨ぐエアブリッジ配線２８で接続される。各ＬＥＤの形状及び配置を工夫することで、３個のＬＥＤであっても発光装置（チップ）全体の外観形状を略正方形とすることができる。

【００４８】

図２２には、合計６個のＬＥＤを二次元配列した例が示されており、図２３にはその回路

図が示されている。各ＬＥＤ１ａ～１ｆは同形、同サイズである。ＬＥＤ１ａ～１ｆは直列接続される。ＬＥＤ１ａ～１ｃは直線上に配置され、ＬＥＤ１ｄ～１ｆは他の直線上に配置される。ＬＥＤ１ｃとＬＥＤ１ｄはエアブリッジ配線２８で接続される。この例においても、チップの全体形状を略正方形とすることができる。

【００４９】

図２４には、合計５個のＬＥＤを二次元配列した例が示されており、図２５にはその回路図が示されている。ＬＥＤ１ａ～１ｅは同形（長方形）、同サイズである。この例においても、全体形状を略正方形とすることができる。

【００５０】

以上、本発明の実施形態について説明したが、本発明はこれに限定されるものではなく種々の変更が可能である。特に、複数の発光素子（ＬＥＤ等）を二次元配置する場合のパターンは上述したパターン以外にも可能である。この場合、隣接する発光素子間で電極を共有して配線を少なくすること、全体形状を正方形あるいは長方形とすること、複数組の発光素子アレイを電極に並列接続すること、交流駆動の場合に複数組の発光素子アレイを互い逆極性とすること、複数組の発光素子アレイをそれぞれジグザグ状に屈曲させて組み合わせること、等が好適である。

【００５１】

図２６～図３１には、これらの変更例のいくつかが例示されている。図２６は交流駆動の場合の二次元配置であり、合計４０個のＬＥＤが配置されている。図２７はその回路図である。図６と異なる点は、２組のＬＥＤアレイのいくつかがｎ電極２４を共有する点である（図５参照）。例えば、一方のＬＥＤアレイの第１列の右端から２番目に位置するＬＥＤ（図中αで示す）のｎ電極２４は、他方のＬＥＤアレイの第１列の右端に位置するＬＥＤ（図中βで示す）のｎ電極２４と共有されている。なお、ＬＥＤアレイの端部（図中γ部分）におけるエアブリッジ配線２８は、交叉させることなく共通形成されている。

【００５２】

図２８は、交流駆動の場合の二次元配置であり、合計１４個のＬＥＤが配置されている。図２９はその回路図である。図１０と異なる点は、２組のＬＥＤアレイのいくつかがｎ電極２４を共有する点である。例えば、一方のＬＥＤアレイの第１列の左端のＬＥＤ（図中αで示す）のｎ電極２４は、他方のＬＥＤアレイの第１列の右端から２番目に位置するＬＥＤ（図中βで示す）のｎ電極２４と共有されている。また、端部（図中γ部分）におけるエアブリッジ配線２８は共通形成されている。

【００５３】

図３０は、交流駆動の場合の二次元配置であり、合計６個のＬＥＤが配置されている。図３１はその回路図である。この例においても、端部（γ部）のエアブリッジ配線２８が共通形成されている。この構成も、一方のＬＥＤアレイにおけるｎ電極２４と他方のＬＥＤアレイにおけるｎ電極２４が共有されていると云うことができる。

【００５４】

【発明の効果】

以上説明したように、本発明によれば、高い駆動電圧で駆動し発光させることができる。

【図面の簡単な説明】

【図１】発光素子（ＬＥＤ）の基本構成図である。

【図２】発光装置の等価回路図である。

【図３】２個のＬＥＤの平面図である。

【図４】図３のＩＶ－ＩＶ断面図である。

【図５】発光装置の他の等価回路図である。

【図６】４０個のＬＥＤを二次元配列した説明図である。

【図７】図６の回路図である。

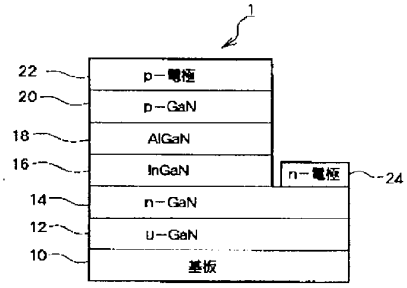
【図８】６個のＬＥＤを二次元配列した説明図である。

【図９】図８の回路図である。

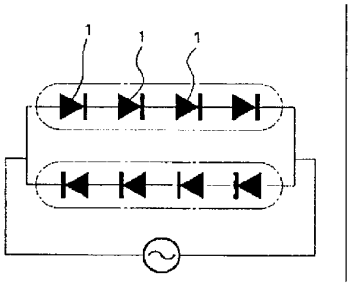
【図１０】１４個のＬＥＤを二次元配列した説明図である。

【図１１】図１０の回路図である。
【図１２】６個のＬＥＤを二次元配列した説明図である。
【図１３】図１２の回路図である。
【図１４】１６個のＬＥＤを二次元配列した説明図である。
【図１５】図１４の回路図である。
【図１６】２個のＬＥＤを配列した説明図である。
【図１７】図１６の回路図である。
【図１８】４個のＬＥＤを二次元配列した説明図である。
【図１９】図１８の回路図である。
【図２０】３個のＬＥＤを二次元配列した説明図である。
【図２１】図２０の回路図である。
【図２２】６個のＬＥＤを二次元配列した説明図である。
【図２３】図２２の回路図である。
【図２４】５個のＬＥＤを二次元配列した説明図である。
【図２５】図２４の回路図である。
【図２６】他の二次元配置説明図である。
【図２７】図２６の回路図である。
【図２８】他の二次元配置説明図である。
【図２９】図２８の回路図である。
【図３０】他の二次元配置説明図である。
【図３１】図３０の回路図である。
【符号の説明】
１０　基板（ウエハ）、１２　ｕ－ＧａＮ層、１４　ｎ型ＧａＮ層、１６　ＩｎＧａＮ発光層、１８　ＡｌＧａＮ層、２０　ｐ－ＧａＮ層、２２　ｐ－電極、２４　ｎ－電極。

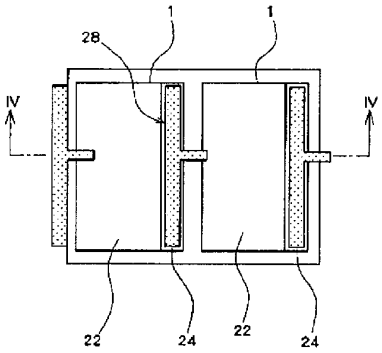
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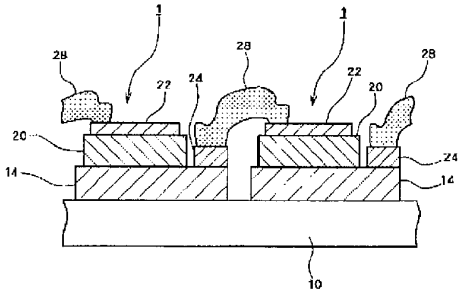
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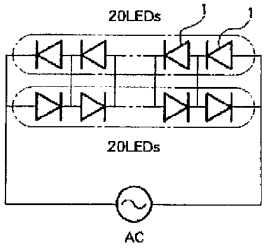
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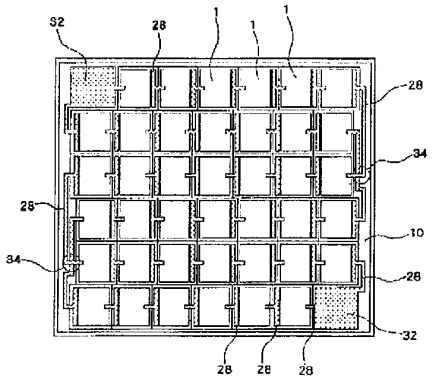
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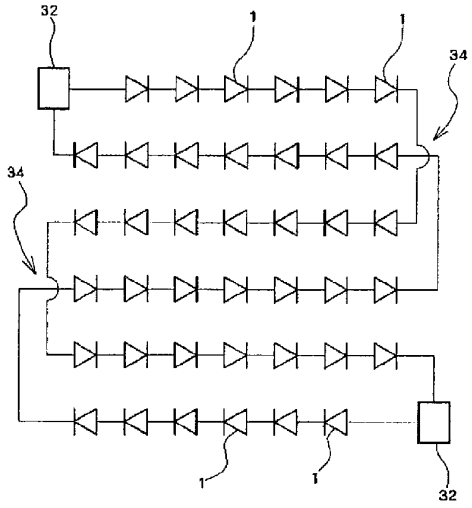
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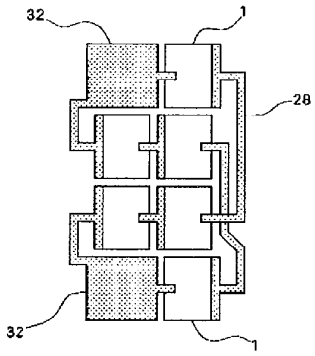
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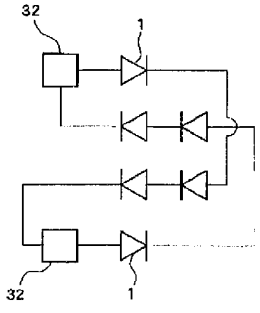
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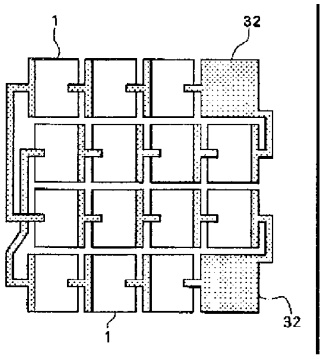
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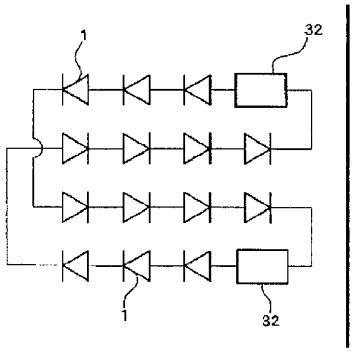
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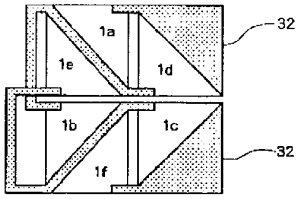


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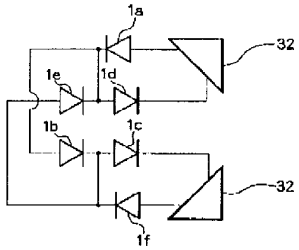


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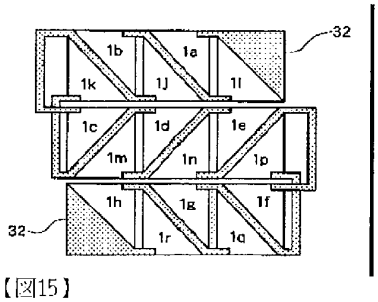
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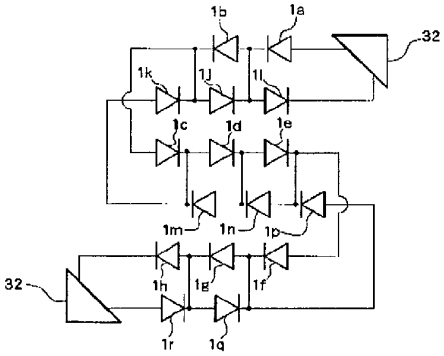
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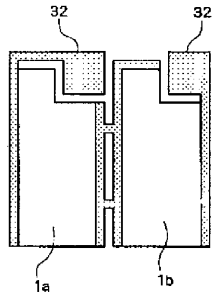
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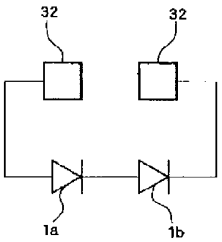
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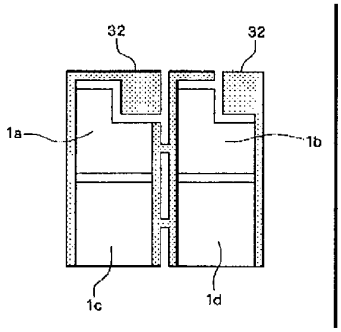
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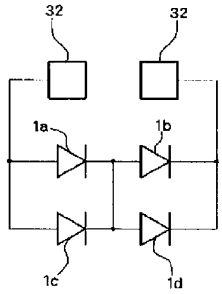
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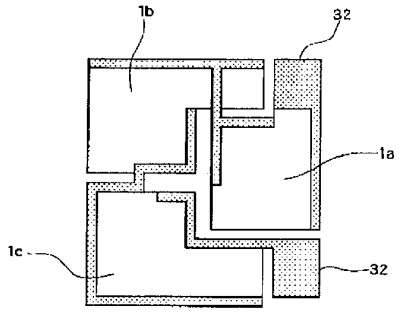
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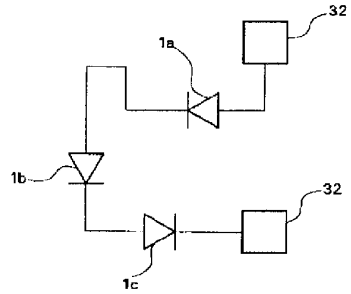
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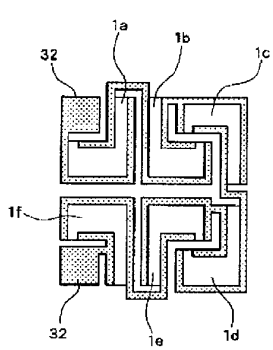
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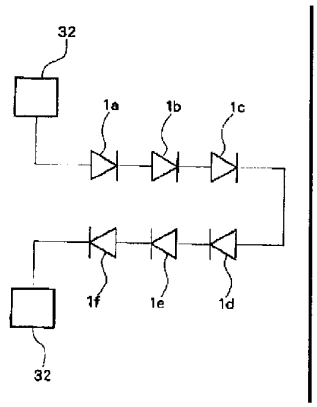
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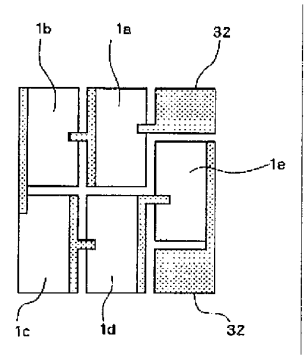
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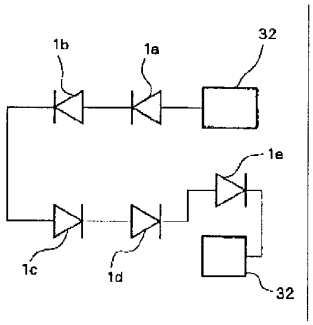
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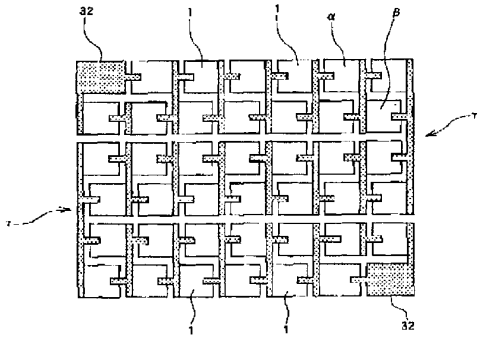
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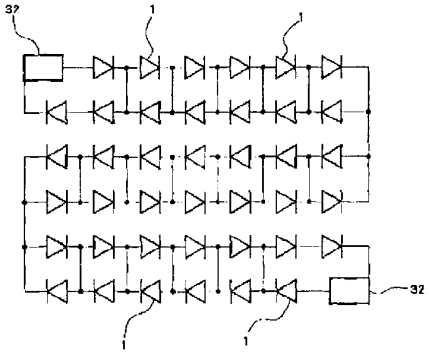
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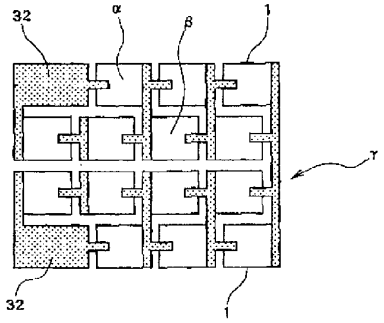
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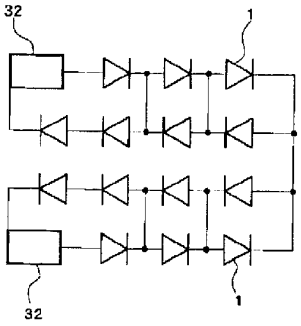
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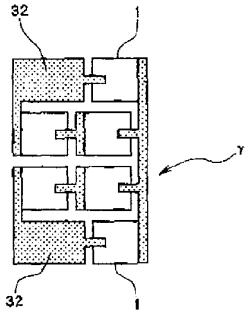
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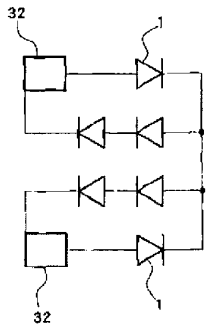
【図29】



【図30】



【図31】



(72)発明者　敖　金平
徳島県徳島市南常三島町２　１　徳島大学内
(72)発明者　大野　泰夫
徳島県徳島市八万町大坪２２１－１－８－１０３
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(71) Applicant *(for all designated States except US)*: **MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.** [JP/JP]; 1006, Oazakadoma, Kadoma-shi, Osaka 5718501 (JP).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: **NAGAI, Hideo**.

(74) Agent: **NAKAJIMA, Shiro**; 6F, Yodogawa 5-Bankan, 2-1 Toyosaki 3-chome, Kita-ku, Osaka-shi, Osaka 5310072 (JP).

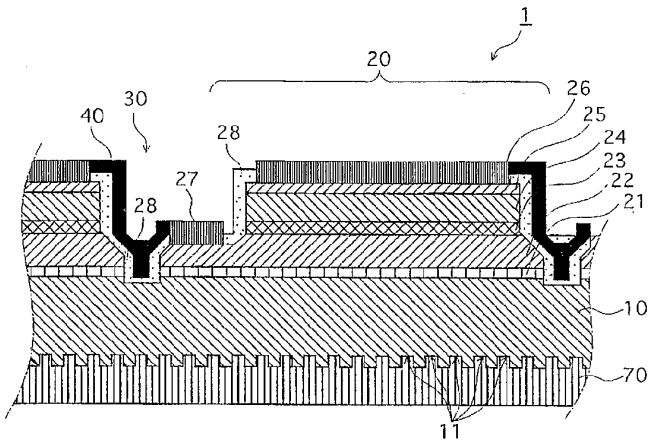
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(54) Title: SEMICONDUCTOR LIGHT EMITTING DEVICE, METHOD OF MANUFACTURING THE SAME, AND LIGHTING APPARATUS AND DISPLAY APPARATUS USING THE SAME



(57) Abstract: The present invention aims to provide a semiconductor light emitting device that may be firmly attached to a substrate with maintaining excellent light emitting efficiency, and a manufacturing method of the same, and a lighting apparatus and a display apparatus using the same. In order to achieve the above object, the semiconductor light emitting device according to the present invention includes a luminous layer, a light transmission layer disposed over a main surface of the luminous layer, and having depressions on a surface facing away from the luminous layer, and a transmission membrane disposed on the light transmission layer so as to follow contours of the depressions, and light from the luminous layer is irradiated so as to pass through the light transmission layer and the transmission membrane.

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DESCRIPTION

SEMICONDUCTOR LIGHT EMITTING DEVICE, METHOD OF MANUFACTURING THE SAME, AND LIGHTING APPARATUS AND DISPLAY APPARATUS USING THE SAME

Technical Field

The present invention relates to a semiconductor light emitting device and a method of manufacturing the same, as well as a lighting apparatus and a display apparatus using the same.

Background Art

Lighting apparatuses with light emitting diodes (LEDs) have been gaining attention as a new light source because of excellent properties in terms of light emitting efficiency and longevity in comparison with incandescent lamps or halogen lamps. In order to improve light output of this kind of lighting apparatus, a quick solution is to mount LEDs in high density. However, this solution is not very realistic due to current issues regarding production cost and heat dissipation in driving when LEDs are mounted in high density. A more realistic solution in order to enhance the light output is to make luminous efficiency of an LED as high as possible. Various attempts have been made to this end, and two key parameters in making such attempts are Internal Quantum Efficiency (IQE) and External Quantum Efficiency (EQE).

The IQE is a parameter indicating the amount of light generated in a luminous layer of an LED to the amount of electric

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power that is supplied to the LED. The IQE is affected by the crystallinity of a semiconductor and the structure of the luminous layer that constitute the LED.

On the other hand, the EQE is a parameter indicating an amount of light emitted outside the LED to the amount of supplied electric power, and expressed by a product of the IQE and light extraction efficiency (a proportion of the amount of light emitted outside the LED in the amount of light generated in the LED). The light extraction efficiency is affected by the shape of a bare chip, the material that covers the bare chip, and the shape of the material. In order to improve the light extraction efficiency, it is common to cover a bare chip with resin so as to minimize the refractive index difference at a boundary between the bare chip and outside of the bare chip as much as possible.

Moreover, in a case of lighting apparatuses using LEDs, it is common for a light extracting surface of a bare chip to have depressions so that an incident angle of light on the light extracting surface is not fixed to one angle, thus improving the light extraction efficiency (Japanese Patent No. 2836687, and *Compound Semiconductor*, Vol.8, No.1, pp.39-42, 2002).

As a method of mounting a bare chip on a mounting substrate, flip-chip bonding as shown in FIG.20 is commonly employed. In the flip-chip bonding as illustrated in FIG.20, a vacuum collet 1300 sticks to a light extracting surface of a bare chip 1100, and the bare chip 1100 is joined with a wiring layer 1210 of a mounting substrate 1200 using ultrasonic bonding. By mounting the bare chip 1100 in this way, the distance between

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a light emitting layer of the bare chip 1100 and the mounting substrate 1200 is shortened, thus making it possible to effectively dissipate the heat generated in the light emitting layer. In other words, the flip-chip bonding is very effective for a lighting apparatus that requires LEDs in high density, in order to ensure a high heat dissipation capacity.

However, mounting bare chips having depressions on the light extracting surface using the flip-chip bonding often causes problems such as decreases in positioning accuracy and bonding strength, and destruction of the depressions. Specifically, as shown in an enlarged view in the circle in FIG.20, depressions 1111 make it difficult for the vacuum collet 1300 to stick to the bare chip 1100 without fail, and for ultrasonic waves to propagate from the vacuum collet 1300 to the bare chips 1100 sufficiently for bonding. The same kind of problems also occur in display apparatuses having bare chips.

Disclosure of the Invention

In order to solve the above noted problems, the present invention aims to provide a semiconductor light emitting device that may be firmly attached to a substrate with maintaining excellent light emitting efficiency, and a manufacturing method of the same, and a lighting apparatus and a display apparatus using the same.

In order to achieve the above object, a semiconductor light emitting device having a luminous layer according to the present invention comprises a light transmission layer disposed over a main surface of the luminous layer, and having

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depressions on a surface facing away from the luminous layer, and a transmission membrane disposed on the light transmission layer so as to follow contours of the depressions, and light from the luminous layer is irradiated so as to pass through the light transmission layer and the transmission membrane.

The above semiconductor light emitting device has the depressions on a surface of the light transmission layer facing away from the luminous layer. Accordingly, the light emitted from the luminous layer is scattered by the depressions or transmitted efficiently, and thus high light extraction efficiency is maintained, as well as high light emission efficiency. Further, the depressions of the semiconductor light emitting device according to the present invention are filled and covered by the membrane, and therefore it is possible to suppress destruction of the depressions by ultrasonic waves applied when the bare chip is mounted to a mounting substrate. Because of this, with the semiconductor light emitting device according to the present invention, it is possible to obtain high light emission efficiency.

Moreover, with the semiconductor light emitting device according to the present invention, a loss of ultrasonic energy is not large because of the above membrane, even when the chip is mounted to the mounting substrate.

Accordingly, the semiconductor light emitting device according to the present invention has an advantage to be able to firmly attach to the mounting substrate while maintaining a high emission efficiency.

Note that it is possible to mount the chip to the mounting substrate using flip-chip bonding.

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The membrane covers the surface so as to follow the contours of the depressions, without including air or gap. Further, by saying the light transmission layer is disposed over the main surface of the luminous layer, it indicates that the light transmission layer may be disposed either directly on the main surface of the luminous layer, or indirectly above the main surface of the luminous layer.

Further, a semiconductor light emitting device usually has a structure that plural layers are formed on the substrate. The above depressions do not necessarily have to be on a surface of a layer out of the plural layers. For example, the depressions may be formed on one of the main surface of the substrate in a case of the semiconductor light emitting device that irradiate light from the luminous layer through the substrate.

When formed irregularly, the depressions serve a function of light diffusion. When the depressions are at a regular interval, a structure of such depressions is called a photonic crystal (PC) or a photonic band gap (PBG) structure, depending on how the depressions are formed. The PC and PBG structures, in general, are a cyclic structure in which depressions and projections appear cyclically at a micoron to $\lambda/4$ (λ is a wavelength in the medium) order on a surface, and have a characteristic that light having a specific wavelength is selectively reflected and transmitted. Therefore, when the semiconductor light emitting device according to the present invention has the light transmission layer having the depression in either the PC or PBG structure, it is possible to realize a function of allowing the light

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to be transmitted easily in the light transmission layer.

The above semiconductor light emitting device may be such that the membrane is formed so as to follow the contours of the depressions on the surface of the light transmission layer. However, it is more desirable that the surface of the membrane facing away from the light transmission layer is substantially flat. Specifically, when mounting the above semiconductor light emitting device to a mounting substrate, the vacuum collet sticks to a surface, from which the light is irradiated, of the device, as described above. If the surface to which the vacuum collet sticks is substantially flat, it is possible that the vacuum collet sticks more firmly. Therefore, it is possible to mount the above semiconductor light emitting device to the mounting substrate more accurately.

A main component of the membrane in the above semiconductor light emitting device may be one of polyimide, epoxy, silicone, and glass. When the glass is used as a material of the membrane, it is possible to use glass by the sol-gel method or low-melting glass. Specific examples of the glass material include (1) a glass material using metal alkoxide (such as tetramethoxysilane and tetraethoxysilane) as starting material, (2) a glass material made from polymer ceramic precursor such as perhydropolysilazane, and (3) a glass material made from such as phosphorus oxide and boronic oxide.

With any of the above listed glass materials, it is possible to form a glass layer (membrane) whose upper surface is substantially flat and filling the depressions, by applying the glass material on the depressions using such as potting

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and spin-coating, drying the glass material, and baking the glass material at a temperature of several hundred degrees centigrade.

It is also desirable that the membrane contains a luminous substance that is excited by the light from the luminous layer. It is especially desirable for a lighting apparatus using the semiconductor light emitting device according to the present invention, if the luminous substance contained in the membrane is a material that is able to convert the light from the luminous layer into the white light (such as a phosphor material).

In order to maintain high light extracting efficiency for the above semiconductor light emitting device, it is also desirable that the depressions on the surface of the light transmission layer are at an interval equal to or greater than $\lambda/4$, λ being a wavelength of the light from the luminous layer.

The luminous layer of the semiconductor light emitting device is generally disposed over a transmission substrate in a state being sandwiched between plural layers such as clad layers, contact layers, and buffer layers. The present invention may also be such that the light transmission substrate as a part or all of the light transmission layer has the depressions on one of main surfaces. It is desirable that the light transmission substrate is made of a material having a refractive index that is substantially equal to a refractive index of the luminous layer, because it is effective to maintain high light extraction efficiency. Specifically, the material for the light transmission substrate may be selected from a group of GaN, SiC, and AlN.

The above structure that is characteristics to the

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present invention may be applied to a light emitting diode device, as well as a Vertical Cavity Surface Emitting Laser device, a Resonant Cavity Light Emitting Diode device, and a Surface Mount Device.

Further, a method of manufacturing the semiconductor light emitting device according to the present invention comprises steps of forming a light transmission layer over a multi-layered body in which the luminous layer is sandwiched between a plurality of layers, the light transmission layer having depressions on a surface facing away from the luminous layer, and forming a transmission membrane on the light transmission layer so as to follow contours of the depressions.

With the above method of manufacturing the semiconductor light emitting device according to the present invention, it is possible to obtain a semiconductor light emitting device having high light extraction efficiency, because the depressions is formed on the surface of the light transmission layer facing away from the luminous layer. Further, the transmission membrane is formed on the light transmission layer so as to fill the depressions, and therefore it is possible to mount the chip firmly with protecting the depressions from destruction when the chip is mounted to the mounting substrate. Specifically, with the above manufacturing method, it is possible to increase the accuracy in mounting when the vacuum collet sticks to the chip, and to reduce a loss of ultrasonic energy in the depressions when the ultrasonic waves are applied.

Accordingly, with the above described method of manufacturing the semiconductor light emitting device

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according to the present invention, a semiconductor light emitting device that has high light emitting efficiency and may be attached to the substrate firmly may be obtained.

As described in the above, the depressions may serve different functions according to a state of the depressions. When formed irregularly, the depressions serve a function of light diffusion. When the depressions are formed regularly at a fixed interval, a structure of such depressions is called a photonic crystal (PC) or a photonic band gap (PBG) structure.

In the method of manufacturing the semiconductor light emitting device according to the present invention, it is also desirable that the membrane contains a luminous substance that is excited by the light from the luminous layer. It is especially desirable that the membrane is polished to a preferred thickness so that the device may irradiate the white light having a desirable wavelength.

Further, a lighting apparatus according to the present invention is such that the semiconductor light emitting device according to the present invention is mounted to the mounting substrate.

The above lighting apparatus has the semiconductor light emitting device including the light transmission layer having the depressions on the surface and the membrane that covers the light transmission layer, and therefore it is possible to maintain high light emitting efficiency and to firmly attach the semiconductor light emitting device to the mounting substrate.

Therefore, the lighting apparatus according to the present invention has high light emitting efficiency and stable

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quality.

As described above, the semiconductor light emitting device according to the present invention has the light transmission layer having a surface with the depressions is disposed over the luminous layer. Thus, it is possible to maintain high light extracting efficiency as well as high light emitting efficiency. Further, because the membrane is disposed over the surface so as to fill the depressions, it is possible to realize firm attachment without destroying the depressions when the semiconductor light emitting device is mounted to the mounting substrate.

Further, with the method of manufacturing the semiconductor light emitting device according to the present invention, the light transmission layer having a surface with depressions is formed over the luminous layer on a side that the device irradiate the light, and then the membrane is formed so as to follow the contours of the depressions. Therefore, it is possible to manufacture the semiconductor light emitting device having the above described advantages easily.

In addition, the lighting apparatus according to the present invention has high light emitting efficiency and stable quality, because the above explained semiconductor light emitting device is mounted to the mounting substrate.

A main component of the membrane in the above semiconductor light emitting device membrane may be one of polyimide, epoxy, silicone, glass by the sol-gel method, and low-melting glass. Specific examples of the glass material include (1) a glass material using metal alkoxide (such as tetramethoxysilane and tetraethoxysilane) as starting

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material, (2) a glass material made from polymer ceramic precursor such as perhydropolysilazane, and (3) a glass material made from such as phosphorus oxide and boronic oxide.

With any of the above listed glass materials, it is possible to form a glass layer (membrane) whose upper surface is substantially flat and filling the depressions, by applying the glass material on the depressions using such as potting and spin-coating, drying the glass material, and baking the glass material at a temperature of several hundred degrees centigrade.

Brief Description Of The Drawings

FIG.1 is a perspective view of a LED chip 1, according to a first embodiment of the present invention.

FIG.2A is a partial sectional view of the LED chip 1.

FIG.2B is a circuit wiring diagram of the LED chip 1.

FIG.3 is a process drawing illustrating a manufacturing process of the LED chip 1.

FIG.4 is a process drawing illustrating a manufacturing process of the LED chip 1.

FIG.5A is a perspective view of a LED module 100 viewed from outside.

FIG.5B is a partial sectional view of the LED module 100.

FIG.6 is a schematic view illustrating a step of flip-chip bonding of the LED chip 1 to a mounting substrate 110.

FIG.7A is a front view of the mounting substrate 110.

FIG.7B is a layout drawing of pads on a LED chip mount unit 1a.

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FIG.8A is a partial sectional view of a lighting apparatus 200 according to the first embodiment, and FIG.8B is a bottom view of the same.

FIG.9 illustrates a process drawing illustrating an attachment process of a LED module 100 to a socket 210 of the lighting apparatus 200.

FIG.10 shows emission spectrum of the lighting apparatus 200.

FIG.11A illustrates a partial sectional view of an LED chip 3 according to the second embodiment.

FIG.11B illustrates configuration of a depression 326a of the bare chip 3.

FIG.12 illustrates manufacturing steps of an LED chip 3.

FIG.13A illustrates a partial sectional view of a mounting substrate 410 on which an LED module 3 is mounted, and FIG.13B

FIG.14 shows an emission spectrum of a lighting apparatus having the LED chip 3.

FIG.15A is a perspective view of an LED display apparatus according to a third embodiment of the present invention, and FIG.15B is a sectional view to illustrate a part indicated by B in FIG.15A.

FIG.16A is a perspective view of a Vertical Cavity Surface Emitting Laser (VCSEL) device 7 according to a fourth embodiment according to the present invention, and FIG.16B is a partial sectional view of the VCSEL device 7.

FIG.17 illustrates manufacturing steps of the VCSEL device 7.

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FIG.18 also illustrates manufacturing steps of the VCSEL device 7.

FIG.19 is a sectional view illustrating a Surface Mount Device as a modified example.

FIG.20 is a schematic view showing steps in mounting a conventional LED chip 1100 to a mounting substrate 1210.

Best Mode for Carrying Out the Invention

The following describes preferred embodiments of the present invention with reference to the drawings.

[First Embodiment]

In a first embodiment, an LED bare chip (hereinafter referred to as the LED chip) 1 is used as an example of semiconductor light emitting devices.

[Structure of LED Chip 1]

The LED chip 1 is explained with reference to FIGs.1 and 2. FIG.1 shows a perspective view. FIG.2A shows a partial sectional view, and FIG.2B shows a circuit wiring diagram, of the LED chip 1.

As shown by FIG.1, the LED chip 1 is such that plural light-emitting elements 20 are formed on a non-doped GaN substrate 10. The light emitting elements 20 are disposed on the substrate 10 in a matrix of 7 × 5 in x and y directions respectively to form total 35 regions on the substrate. A size of one light emitting element 20 is 285 μm in x direction, and 400 μm in y direction. A size of the LED chip 1 is 2 mm × 2 mm, for example.

Each of the light emitting elements 20 on the LED chip 1 constitutes a diode structure, and is separated from other

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light emitting elements 20 by separation grooves 30, and a bridge wiring 40 electrically connects the 35 diode structures in series.

As shown in FIG.1, a cathode electrode 50 and an anode electrode 60 on each of a pair of opposing corners of the LED chip 1. These electrodes 50 and 60 are an n-electrode and a p-electrode, respectively, of the light emitting elements 20 that is positioned at the both edges of the 35 light emitting elements 20 serially connected by the bridge wiring 40.

Further, as shown in an enlarged part in FIG.1, a lower surface of the non-doped GaN substrate 10 has depressions 11, and a membrane 70 covers the depressions. There is no gap between the membrane 70 and the non-doped GaN substrate 10, even at bottoms of the depressions 11. In other words, a surface having depressions of the non-doped GaN substrate 10 is densely covered with the membrane 70.

A negative direction along a z-axis in FIG.1 (downside of the drawing) is a direction in which light from the LED chip 1 is irradiated. The depressions 11 on the substrate 10 are formed in order that the irradiated light is easily diffused or transmitted and to virtually lower the refractive index difference at the boundary (a irradiation surface). Details regarding this are described in the patent and non-patent references cited in the above, and further explanation is not given here.

As shown in FIG.2A, when the LED chip 1 is viewed in section, a GaN buffer layer 21 (30 nm thick), an n-GaN clad layer 22 (Si doped 3×10^{18} cm^{-3}, 2 μm thick), a (InGaN/GaN) ×6 luminous layer 23 (InGaN is 2 nm thick, and GaN is 8 nm),

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a p-GaN clad layer 24 (Mg doped 3×10^{19} cm^{-3}, 200 nm thick), and then a p-GaN contact layer 25 (Mg doped 3×10^{19} cm^{-3}, 50 nm thick) are layered on the non-doped GaN substrate 10 in a stated order, and finally p-electrodes 26 made of Rh/Pt/Au are formed on a top of the layers.

The (InGaN/GaN)×6 luminous layer 23 indicates a multiplex quantum well structure luminous layer at 6 periods of InGaN/GaN, and irradiates blue light having a wavelength of 460 nm in driving the LED chip 1.

A refractive index of the non-doped GaN substrate 10 is around 2.5, which is substantially the same as a refractive index of the (InGaN/GaN) × 6 luminous layer 23. Therefore, the non-doped GaN substrate 10 is more effective to improve the light extraction efficiency in comparison with a conventional LED chip that utilizes a sapphire (refractive index = 1.7).

The separation grooves 30 are made so as to reach the non-doped GaN substrate 10, and a Si_3N_4 membrane 28 as an insulating film covers a surface of the separation grooves 30. On the shelf shaped n-GaN clad layer 22, n-electrodes 27 made of Ti/Au are formed at the boundary between the light emitting element 20 and the separation grooves 30. The bridge wiring 40 made of Ti/Pt/Au connects the n-electrodes 27 to the n-electrodes 26 on the light emitting element 20 that is next to the n-electrodes 27, in one-to-one relation.

On the other hand, the non-doped GaN substrate 10 has the minute depressions 11 having a square-shaped cross-section (the depressions are at an interval of 1 μm, for example) on all over the lower surface. By having the depressions 11 on

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the surface of the non-doped GaN substrate 10, the irradiated light from the (InGaN/GaN) × 6 luminous layer 23 is easily diffused or transmitted. Further, as described above, the membrane 70 is formed on the surface of the non-doped GaN substrate 10 so as to fill the depressions 11. The membrane 70 is mainly made of polyimide resin that transmits light, and contains yellow phosphor material such as $(Sr, Ba)_2SiO_4:Eu^{2+}$ and ultrafine particles such as SiO_2 dispersed in the membrane. The membrane 70 is formed so as that a surface of the membrane 70 facing away from the luminous layer becomes substantially flat and a thickness is 80 μm at a thinnest part where there is no depression.

A structure of the depressions 11 is called a photonic crystal (PC) or a photonic band gap (PBG) structure, depending on how the depressions are formed, and depressions of such a structure serve a different function other than the light diffusion, i.e. such a structure allows the depressions to transmit light easily.

The thickness of the membrane 70 is set to 80 μm in order that the LED chip 1 as a whole emits white light, by mixing blue exciting light, having a peak wavelength ranged from 400 to 500 nm, from the (InGaN/GaN) × 6 luminous layer 23 and yellow light, having a peak wavelength ranged from 550 to 600 nm, generated from the membrane 70 excited by a part of the blue exciting light.

The depressions 11 of the non-doped GaN substrate 10 are square in the present embodiment, as explained above. However, a shape and size of the depressions are not restricted to the above example as long as the shape and size are set

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in a range that improves the light extraction efficiency. Round or honey-comb depressions, or straight-line grooves may be employed, for example. Note that it is desirable that the depressions 11 are formed at an interval of $\lambda/4$ or greater, when the wavelength of the light from the (InGaN/GaN) × 6 luminous layer 23 is λ.

As shown in FIG.2B, the LED chip 1 is such that the 35 light emitting elements 20 are connected in series by the bridge wiring 40 connecting the light emitting elements 20. When supplying the LED chip 1 with a power of 50 mA via the cathode electrode 50 and anode electrode 60, an operational voltage becomes 120 V. When supplying power to the LED chip 1, it is desirable to secure a path to disperse heat generated at the LED chip 1 by connecting to a mounting substrate and such.

Note that, although the LED chip 1 according to the present embodiment has a structure including the plural light emitting elements 20, it is also possible that one LED chip includes only one light emitting element.

[Method of Manufacturing LED Chip 1]

Next, a method of manufacturing the LED chip 1 is explained with reference to FIGs.3 and 4.

As shown in FIG.3A, the GaN buffer layer 21, n-GaN clad layer 22、(InGaN/GaN) × 6 luminous layer 23, p-GaN clad layer 24, and p-GaN contact layer 25 are layered in a stated order on the non-doped GaN substrate 10, which is φ5 cm and 300 μm thick, using Metal Organic Chemical Vapor Deposition (MOCVD).

Next, as shown in FIG.3B, grooves 31 are formed by etching at areas where the separation grooves 30 and n-electrodes 27 are formed. The grooves 31 are as deep as to reach the n-GaN

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clad layer 22. In forming the grooves 31, although not shown by the drawings, etching is performed after masking the rest of the areas, and the mask is removed after the grooves 31 are formed.

As shown in FIG.3C, a part of a bottom surface of each of the grooves 31 is further etched. Grooves 32 are thus formed and penetrate the n-GaN buffer layer 21 to reach the non-doped GaN substrate 10. The separation grooves 30 are formed based on the grooves 32. In order to form the grooves 32, it is possible to use a laser instead of etching.

As shown in FIG.3D, the Si_3N_4 membrane 28 is formed so as to cover an entire surface including wall surfaces of the grooves 32. The Si_3N_4 membrane 28 is formed using such as spattering, in order to achieve insulation and surface protection. By covering the surfaces of the grooves 32, the grooves 33 are formed. The grooves 32 make only low cuts in the substrate 10, and very superficial, and therefore the grooves 32 will not break the substrate 10.

Next, as shown in FIG.4E, parts of the Si_3N_4 membrane 28 where the p-electrodes 26 are to be formed are removed by etching, and then films of Rh/Pt/Au are formed by evaporation. Thus, the p-electrodes 26 are formed.

Then, as shown in FIG.4F, parts of the Si_3N_4 membrane 28 where the n-electrodes 27 are to be formed on the shelf part next to each of the separation grooves 30 are removed by etching, and then films of Ti/Au are formed by evaporation. Thus, the n-electrodes 27 are formed. Similarly, the bridge wiring 40 made of Ti/Pt/Au is formed so as to connect each p-electrode 26 and n-electrode 27 of two light emitting

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elements 20 that are next to each other.

Manufacturing steps from here are the most characteristic part in the present embodiment.

As shown in FIG.4G, a back surface of the non-doped GaN substrate 10 (downside of the drawing) is polished until thickness becomes 150 μm using lap polish. Then, as shown in an enlarged part of FIG.4G, the depressions 11 are etched on the back surface of the non-doped GaN substrate 10. The depressions 11, as described above, are formed at an interval of 1 μm, and an opening of each depression is rectangular.

As shown in FIG.4H, the polyimide acid solution, containing particles of yellow phosphor material such as $(Sr, Ba)_2SiO_4:Eu^{2+}$, and SiO_2 in a dispersed state, is applied to the back surface of the non-doped GaN substrate 10 on which the depressions 11 are formed. The solution is filled in the depressions 11 so that no air bubble is caused inside. And, after heating and hardening at a temperature of 350 °C, the membrane is formed.

The formed membrane is polished so that the LED chip 1 irradiates white light generated by the light from the (InGaN/GaN) × 6 luminous layer 23 mixed with the light excited by the phosphor material in the membrane. For polishing, lap polishing is performed until the thickness of the membrane becomes 80 μm, for example. By this, the membrane 70 is finished.

As a main component of the membrane 70, it is also possible to use such as an epoxy resin or a hard silicone resin, in addition to the above-mentioned polyimide. In this case, it is possible to harden the membrane by heating at a temperature

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150 °C. Further, the thickness of the membrane 70 varies according to a relation between the blue light from the (InGaN/GaN) × 6 luminous layer 23 and a proportion of the yellow phosphor contained in the membrane 70. Therefore, in the polishing step, the membrane 70 is polished to a thickness with which a specific color temperature is obtained without fail.

Finally, although not shown in the drawing, the LED chip 1 is finished by dicing the membrane into individual LED chips 1.

In the present embodiment, the non-doped GaN substrate 10 was used as a substrate. However, it is also possible to use a low cost substrate such that a high resistant layer such as an AlGaN layer is formed on an n-GaN substrate. In this case, it is necessary to form the separation grooves so that the high resistant layer is not removed.

[Structure of LED Module 100]

A LED module 100 having the above LED chip 1 is explained with reference to FIG.5.

As shown in FIG.5A, the LED module 100 comprises a disk shaped composite substrate 110 with a diameter of φ5 cm and three light emitting units 120 provided on the composite substrate 110. The composite substrate 110 includes a notch 110a used when the LED module is attached to the lighting apparatus 200, and terminals 130 and 140 with which power is supplied from the lighting apparatus 200. Although not shown in the drawing, the guiding hole is formed on a substantial center of the composite substrate 110 in order to improve operationality when attached to the lighting apparatus 200.

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The three light emitting units 120 on the composite substrate 110 each include the LED chip 1 mounted thereon. Details are explained with reference to a partial sectional view in FIG.5B.

As shown in FIG.5B, the LED chip 1 is mounted at a bottom surface of a depression 111 of the composite substrate 110. The LED chip 1 is mounted to the composite substrate 110 using flip-chip bonding, and has an excellent heat dispersion property. A reflective mirror 150 made of aluminum is formed so as to surround the depression 111 in which the LED chip 1 is mounted. The depression 111 surrounded by the reflective mirror 150 is filled with a resin layer 16, and thereby the LED chip 1 is sealed. Examples of material for the resin layer 160 include a silicon resin and a epoxy resin.

An entire part of the reflective mirror 150 and the resin layer 160 that covers the LED chip 1 are further covered by a lens layer 170. Such as a resin material that can be formed in one-piece by molding and a glass material may be used for the lens layer 170. An internal structure of the LED module 100 is explained using FIG.5B illustrating a sectional view taken at line A-A of FIG.5A.

As shown in an enlarged part of FIG.5B, the p-electrodes 26 and n-electrodes 27 of the LED chip 1 are connected to the wiring layer 114 of the composite substrate 110. In addition to an Au coating applied to a surface of the wiring layer 114, Au layers 180 are inserted between each of the electrodes 26 and 27 and the wiring layer 114. These Au layers are Au bumps that have been disposed on the wiring layer 114 when the LED chip 1 is mounted on the composite substrate 110 by flip-chip

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bonding.

Also as shown in an enlarged part of FIG.5B, the composite substrate 110 includes an aluminum layer 112 with 1 mm in thickness, an alumina composite insulating layer 113, and the wiring layer 114 made of copper layered in a stated order. Moreover, although not shown in FIG.5, an alumina composite insulating layer 115 is layered on the wiring layer (See FIG.6).

Thickness of the alumina composite insulating layers 113 and 115 is 100 μm, and thickness of the wiring layer 114 is 25 μm.

The p-electrodes 26 and n-electrodes 27 on the LED chip 1 are mounted on the wiring layer 114 in flip-chip bonding. In FIG.1, predetermined pads on the wiring layer 114 to which the cathode electrode 50 and anode electrode 60 are connected are electrically connected to the terminals 130 and 140, respectively. By this, when driving the LED module 100, power is supplied to the LED chip 1 via the wiring layer 114.

The LED module 100 according to the embodiment of the present invention includes three light emitting units 120, each of which has a structure described above.

While the p-electrodes 26 and n-electrodes 27 on the light emitting elements 20 that are next to each other are connected by the bridge wiring 40 as explained above, the p-electrodes 26 and n-electrodes 27 are connected by being mounted on the composite substrate 110, in order to ensure the connection within the LED chip 1 and to disperse the heat generated in the LED chip 1 to the composite substrate 110 without fail, when driving to emit light.

[Mounting LED Chip 1 to Composite Substrate 110]

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Next, a method of mounting the LED chip 1 to the composite substrate 110 with reference to FIG.6 and FIG.7.

As shown in FIG.6, the alumina composite insulating layer 115, which is a top layer of the composite substrate 110, is partially removed at an area where the LED chip 1 is mounted. The composite substrate 110 has areas on which three LED chips 1a, 1b, and 1c are mounted, respectively, as shown in FIG.7A, and the wiring layer 114 connects the positive and negative electrodes of each chip to the terminals 130 and 140, respectively.

As shown in FIG.7B, the wiring layer 114 is, at the areas where LED chips 1a, 1b, and 1c are mounted, patterned to a cathode pad 1151, an anode pad 1152, and island pads 1153 each correspond to each of 35 light emitting elements 20 of the LED chip 1. Among the pads, the cathode pad 1151 and anode pad 1152 are connected to the terminals 130 and 140, respectively, as described above. In addition, Au bumps 180 are formed on each of the pads 1151-1153.

The island pads 1153 have a function to improve the connectivity between the p-electrodes 26 and n-electrodes 27 each on the light emitting elements 20 that are next to each other, as well as a function to transmit the heat generated in the LED chip 1 to the composite substrate 110 at high efficiency. The heat transmitted to the composite substrate 110 is dispersed from the aluminum layer 112 via the wiring layer 114 and alumina composite insulating layer 113. Each of the island pads 1153 is formed independently, and has the above explained important functions.

Back to FIG.6, when the LED chip 1 is mounted to the

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composite substrate 110 by flip-chip bonding, a vacuum collet 500 sticks to a surface of the LED chip 1 on which the membrane 70 is formed and then moves down the LED chip 1 till the electrode 26 and 27 come into contact with the Au bumps 180 on the wiring layer 114 of the composite substrate 110. Next, while the electrode 26 and 27 are pressed against the Au bumps 180, ultrasonic waves are applied from the vacuum collet 500. The Au bumps 180 becomes soft by the ultrasonic waves applied to the bumps, and the bonding is finished when application of the ultrasonic waves stops.

As shown in an enlarged part of FIG.6, the membrane 70 is formed on the surface of the LED chip 1 that the vacuum collet 500 sticks to. Because the surface of the membrane 70 that the vacuum collet 500 sticks to is substantially flat as shown in the drawing, it is possible that the vacuum collet 500 sticks to the surface without fail. In addition, the surface that is substantially flat reduces loss of energy in applying the ultrasonic waves from the vacuum collet 500 via the surface.

Further, the membrane 70 also has a function to protect the depressions 11 of the non-doped GaN substrate 10 from being destroyed while the ultrasonic bonding.

[Lighting Apparatus 200 having LED module 100]

A lighting apparatus 200 having a LED module 100 is explained next with reference to FIGs.8 and 9. FIG.8 illustrates a perspective view and a bottom view of the lighting apparatus 200. FIG.9 illustrates an explosion view relating to attachment of the LED module 100.

As shown in FIG.8A, the lighting apparatus 200 comprises

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a horn-shaped member 210 and the LED module 100 that is attached inside the horn-shaped member 210. The horn-shaped member 210 includes a power conversion circuit (not shown in the drawings) for converting commercially supplied AC power (100 V and 50/60 Hz, for example) into DC power that is necessary to drive the LED module 100 to emit light.

As shown in FIG.8B, the LED module 100 is disposed so that the aluminum layer 112 of the composite substrate 110 is closely attached to an attaching surface inside the horn-shaped member 210 of the lighting apparatus 200.

Next, as shown in FIG.9, a round depression 211 that corresponds to a shape of the composite substrate 110 of the LED module 100 is formed on the attaching surface of the horn-shaped member 210 to which the LED module 100 is attached. The bottom of the depression 211 is substantially flat, and a female screw (not shown in the drawings) is disposed at a part closer to an opening of the depression 211 on an inside wall. A guide 212 and flexible terminals 213 and 214 are disposed on the inside wall between the female screw and the bottom surface. Positions of the guide 212 and the flexible terminals 213 and 214 correspond, respectively, to positions of the notch 110a and terminals 130 and 140 of the LED module 100. In addition, a guide pin 215 is disposed at a center of the bottom surface of the depression 211 of the horn-shaped member 210.

The flexible terminals 213 and 214 are flexible and not attached to the bottom surface of the depression 211 of the horn-shaped member 210. When inserting the LED module 100 into the depression 211, both the flexible terminals 213 and

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214 are flexed along the inside wall of the depression 211 in advance, before inserting the LED module 100.

In order to attach the LED module 100 to the horn-shaped member 210 having the above structure, the guide 212 is inserted into a guiding hole of the LED module 10, and the LED module 100 is set into the bottom surface of the horn-shaped member 210 by fitting the notch 110a along the guide pin 215. Then, when the LED module 100 is placed on the bottom surface of the depression 211 of the horn-shaped member 210, the flexible terminals 213 and 214 that have been flexed along the inside all of the depression 211 are cranked so as to be connected to the terminals 130 and 140 of the LED module 100, respectively. After that, an O-shaped ring 220 is placed at a circumference of the LED module 100, and a ring-shaped screw 230 is screwed into the female screw disposed on the inside wall of the depression 211. When the ring-shaped screw 230 and female screw are fully screwed together, the attachment of the LED module 100 to the horn-shaped member 210 is completed.

In the lighting apparatus 200 according to the present embodiment, silicone grease is applied between a back side of the LED module 100 and the bottom surface of the depression 211 of the horn-shaped member 210 in order to improve the heat dispersion efficiency. In addition, a high reflection finish is applied to an inside wall of a lampshade part of the horn-shaped member 210 in order to extract light from the LED module 100 at a high light extraction efficiency.

In the lighting apparatus 200 having the above structure, a current 150 mA is supplied to the LED module 100 via the terminals 130 and 140 after converting the commercially

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supplied AC power into the DC power at the power conversion circuit in the horn-shaped member. In the LED module 100 to which the current is supplied, the three light emitting units 120 emit the white light. At this time, the heat generated in the LED chip 1 is dispersed to the horn-shaped member 210 via the aluminum layer 112 of the composite substrate 110. Therefore, with the lighting apparatus 200, it is possible to suppress deterioration of the LED chip 1 and to maintain high luminous efficiency, even when the LED chip 1 is driven to emit light for an extended length of time.

Further, by high reflection finishing applied the lampshade part of the horn-shaped member 210, more than 90 % of the white light from the LED module 100 is extracted from the lighting apparatus 200.

A spectral distribution of the white light irradiated by the lighting apparatus 200 according to the present embodiment is illustrated in FIG.10. As shown in FIG.10, the lighting apparatus 200 according to the present embodiment irradiates the white light having a color temperature of 5400 K and an average color rendering index (CRI) of 70. A relative intensity of an emission spectrum becomes its peak in vicinity of wavelengths 460 nm and 560 nm, and especially sharp in vicinity of wavelengths 460 nm. A total luminous flux is 1000 lm, and an on-axis luminous intensity is 2000 cd.

With the lighting apparatus 200 according to the present embodiment, the white light is obtained by mixing blue light from the (InGaN/GaN) × 6 luminous layer 23 and yellow light that the membrane 70 emits when excited, and accordingly, the CRI is around 70. However, by having the membrane 70 contain

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such as Ca-Al-Si-O-N oxynitride phosphor glass that irradiates red light, it is possible to improve the CRI.

[Advantages of LED Chip 1, LED Module 100 Using LED Chip 1, and Lighting Apparatus 200 Using LED Chip 1]

As described above, the LED chip 1 according to the present embodiment is such that the depressions 11 are disposed on the surface of the non-doped GaN substrate 10 facing away from the luminous layer, and the membrane 70 is formed so as to cover the depressions 11. Accordingly, as in FIG.6, when the LED chip 1 is mounted by flip-chip bonding to the composite substrate 110, the depressions 11 on the non-doped GaN substrate 10 are protected. Further, misalignment of the position when mounting is suppressed, because the vacuum collet 500 sticks to the LED chip 1 firmly in flip-chip bonding. Moreover, when the vacuum collet 500 applies the ultrasonic waves, the membrane 70 prevents the ultrasonic energy from weakening in transmission between the vacuum collet 500 and the LED chip 1, and thus mounting is performed without fail.

With the LED module 100 having the LED chip 1 and the lighting apparatus 200 having the LED chip 1, it is possible to obtain high light extraction efficiency, because the depressions 11 of the non-doped GaN substrate 10 of the LED chip 1 are protected. In addition, the LED module 100 having the LED chip 1 and the lighting apparatus 200 having the LED chip 1 have high light emission efficiency, because the attachment is done firmly when mounting.

Note that the LED chip 1 according to the present embodiment also has an advantage such that there is no obstacle such as an electrode which blocks the light on a side which

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light from the luminous layer is irradiated, and therefore a shadow on an irradiated surface will not appear.

[Second Embodiment]

In a second embodiment, a LED chip 3 as an example of the semiconductor light emitting device is explained.

[Structure of LED chip 3]

The LED chip 3 according to the present embodiment has a similar appearance with the LED chip 1 shown in FIG.1. Specifically, light emitting elements 320 each having a size of 285 μm × 400 μm are disposed in a matrix of 7 × 5, and a size of the LED chip 3 is 2 × 2 mm. Below, a structure of the LED chip 3 is explained focusing on differences from the LED chip 1, with reference to FIG.11. FIG.11A illustrates a partial sectional view of the LED chip 3, and FIG.11B illustrates a top view of the LED chip 3 without a membrane 370, which will be explained later.

As shown in FIG.11A, the LED chip 3 is formed in a manner that an AlGaN buffer layer 321 (30 nm thick), an n-$Al_{0.1}Ga_{0.9}N$ clad layer 322 (Si doped 3 × 10^{18} cm^{-3}, 1.5 μm thick), an $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N$ × 5 luminous layer 323 ($In_{0.03}Ga_{0.97}N$ is 3 nm thick, and $Al_{0.05}Ga_{0.95}N$ is 5 nm thick), a p-$Al_{0.1}Ga_{0.9}N$ clad layer 324 (Mg doped 3 × 10^{19} cm^{-3}, 200 nm thick), and a p-GaN contact layer 325 (Mg doped 3 × 10^{19} cm^{-3}, 500 nm thick) are layered on the a non-doped 4H-SiC substrate 310 in a stated order. The $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N$ × 5 luminous layer 323 indicates a multiplex quantum well structure luminous layer with 5 periods of $In_{0.03}Ga_{0.97}N/Al_{0.06}Ga_{0.95}N$, and irradiates near-ultraviolet light having a wavelength of 380 nm in driving the LED chip 3.

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A refractive index of the non-doped 4H-SiC substrate 310 is around 2.3, which is substantially the same as a refractive index of the $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N$ × 5 luminous layer 323.

Structures of a separation groove 330, n-electrode 327, an Si_3N_4 membrane328, and a bridge wiring 340 are the same as in the LED chip 1, and not explained here.

As shown in FIG.11B, depressions are not formed on a back surface of the non-doped 4H-SiC substrate 310 of the LED chip 3, and an Ni/Al/Pt/Au layer 380 is formed. Further, a p-electrode 326 made of Ni/Au is formed on the p-GaN contact layer 325, and a plurality of depressions 326a are formed so as to penetrate from a surface of the p-GaN contact layer 325 to the p-electrode 326. Details about these depressions are explained with reference to FIG.11B.

As shown in FIG.11A, the depressions 326a are in a round shape formed at a period of 1 μm, and as described above, the depressions have a function to make light irradiated from the $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N$ × 5 luminous layer 323 is easily dispersed or transmitted. The depressions 326a are formed over an entire area of the p-electrode 326 that irradiates the near-ultraviolet light from the $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N$ × 5 luminous layer 323.

Back to FIG.11A, an upper surface of the LED chip 3 where electrodes 326 and 327 are formed is entirely covered by the transmission membrane 370. Although not shown in the drawing, the membrane 370 is not formed on parts corresponding to a cathode electrode 50 and an anode electrode 60 in FIG.1.

The membrane 370 is 50 μm thick, mainly composed of a

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hard silicon resin having light transmissivity, and is formed so as to fill the depressions 326a completely and so that an external surface is substantially flat. Moreover, the membrane 370 contains, in a dispersed state, a phosphor material that is excited to emit light by the near-ultraviolet light from the $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N \times 5$ luminous layer 323, and fine particles of SiO_2. The phosphor material to be selected may be any phosphor material that is excited by the near-ultraviolet light so that the white light is irradiated from the LED chip 3 as a result. Examples of such a phosphor material that may be applied are in the following.

Example 1: A combination of blue phosphor material, green phosphor material, and red phosphor material, emitting blue light, green light, and red light, respectively when excited by the near-ultraviolet light.

Example 2: A combination of the phosphor material in the Example 1, and yellow phosphor material emitting yellow light when excited by the near-ultraviolet light.

Example 3: A combination of blue phosphor material and yellow phosphor material, emitting blue light and yellow light, respectively, when excited by the near-ultraviolet light.

Example 4: A combination of the phosphor material in the Example 3, and red phosphor material emitting red light when excited by the near-ultraviolet light.

Example 5: A combination of blue phosphor material emitting blue light when excited by the near-ultraviolet light, and green phosphor material and red phosphor material, emitting green light and red light, respectively, when excited by the blue light emitted from the blue phosphor material.

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Example 6: A combination of blue phosphor material emitting blue light when excited by the near-ultraviolet light, green phosphor material emitting green light when excited by the blue light emitted from the blue phosphor material, and red phosphor material emitting red light when excited by the green light emitted from the green phosphor material.

The above examples are just examples, and do not restrict the present invention. Any other combination with which the white light is obtained from the LED chip 3 may be employed.

In addition, in the above examples, the blue light indicates light having a peak wavelength of light emission falls in a range of 400 nm to 500 nm, the green light indicates light having a peak wavelength of light emission falls in a range of 500 nm to 550 nm, the red light indicates light having a peak wavelength of light emission falls in a range of 600 nm to 680 nm, and the yellow light indicates light having a peak wavelength of light emission falls in a range of 550 nm to 600 nm.

Specifically, the following phosphor materials may be utilized.

Blue Phosphor Material:

$(Ba, Sr)MgAl_{10}O_{17}:Eu^{2+}$

$(Ba, Sr, Ca)_{10}Mg(PO_4)_6Cl_2:Eu^{2+}$

Green Phosphor Material:

$BaMgAl_{10}O_{17}:Eu^{2+}, Mn^{2+}$

$(Ba, Sr)_2SiO_4:Eu^{2+}$

$Y_3(Al, Ga)_5O_{12}:Ce^{3+}$

Yellow Phosphor Material:

$(Y, Gd)_3Al_5O_{12}:Ce^{3+}$

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$(Sr, Ba)_2SiO_4:Eu^{2+}$

Red Phosphor Material:

$La_2O_2S:Eu^{3+}$

$CaS:Eu^{2+}$

Moreover, among the substances contained in the membrane 370, SiO_2 is ultrafine particles having a diameter ranged from a couple 10 nm to a couple 100 nm. The following may be used as fine particles contained in the membrane 370, other than SiO_2 as described above: Al_2O_3, ZnO, Y_2O_3, TiO_2, ZrO_2, HfO_2, SnO_2, Ta_2O_3, Nb_2O_3, $BaSO_4$, ZnS, V_2O_5, and a mixture of any of the above substances.

A circuit configuration of the LED chip 3 of the above structure is such that the 35 light emitting elements 320 are connected in series as FIG.2B, and the near-ultraviolet light from the $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N \times 5$ luminous layer 323 is converted into the white light at the membrane 370 and irradiated from the upper surface shown in FIG.11A. Driving voltage of the LED chip 3 is 120 V, when the heat dispersion is ensured and a current of 50 mA is supplied.

[Method of Manufacturing LED Chip 3]

Next, a method of manufacturing the LED chip 3 is explained with reference to FIG.12. In manufacturing the LED chip 3, steps after the step shown in FIG.4F are explained, because the steps from the beginning to FIG.4F are the same as the method of manufacturing the LED chip 1, although material used is not the same.

FIG.12A shows a step at which formation of the p-electrode 326 and n-electrode 327 is completed.

Next, as shown in FIG.12B, the lower surface of the

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non-doped 4H-SiC substrate 310 is polished till a thickness of the substrate becomes 150 μm. After the polishing, the Ni/Al/Pt/Au layer 380 is formed on the polished surface using evaporation.

As shown in FIG.12C, the depressions 326a in a pattern shown in FIG.11B are etched to an area where the p-electrode 326 is to be formed. Etching is performed in a manner that a surface of the p-GaN contact layer 325 becomes bottom surfaces of the depressions 326a. The depressions 326a are formed at a period of 1 μm and a shape of openings of the depressions 326a is round.

Then silicon resin containing phosphor material is applied to an entire upper surface of the chip, and the membrane 370 is formed after heating the silicon resin at a temperature of 150 °C and hardening. When applying the silicon resin, a special care needs to be taken so that the depressions 326a does not include air inside. In addition, parts corresponding to the cathode electrode and anode electrode are masked so that the silicon resin is not applied.

Finally, after lap polishing is performed until the thickness of the membrane becomes 50 μm, the manufacturing of the LED chip 3 is completed by dicing the membrane into LED chips.

[Structure of LED module]

A LED module having the above LED chip 3 is explained with reference to FIG.13. FIG.13A illustrates a partial sectional view of the LED module, and FIG.13B illustrates a connection between the LED chip 3 and a wiring layer 414.

As shown in FIG.13A, main components of the LED module

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include a ceramics substrate 410 having a depression 411 whose opening has a diameter of φ3 mm, and the LED chip 3 that is connected to a bottom surface of the depression 411. A reflective mirror 450 made of aluminum (thickness: 0.5 mm, diameter of an upper part of an opening: 4 mm) is attached over the ceramics substrate 410 so as to surround the depression 411. A resin layer 460 is filled in the depression 411 surrounded by the reflective mirror 450, so as to firmly fix the LED chip 3. An upper surface of the resin layer 460 is substantially even with an upper surface of the reflective mirror 450, and a lens layer 470 is formed to cover the upper surfaces.

As shown in FIG.13A, the ceramics substrate 410 is a substrate with a diameter of φ5 cm and having a laminated structure. The ceramics substrate 410 is structured such that an AlN layer 412 with 0.5 mm in thickness, the wiring layer 414 that is 25 μm in thickness and made of copper or tungsten with, and a ceramics layer 415 are layered in a stated order on the ceramics substrate 410. At a part where the depression 411 is formed, the ceramics layer 415 as a top layer is removed, and the wiring layer 414 is patterned into two parts, a cathode electrode side and an anode electrode side. Further, an Au coating is applied to a surface of a part (pad) where the wiring layer 414 is exposed because the ceramics layer 415 is removed by the depression 411. Although not shown in the drawing, a lower surface of the ceramics substrate 410 is applied with an Au coating in order to improve the heat dispersion property.

It is possible to use a layer made of Al_2O_3, BN, MgO, ZnO, or SiC for the ceramics substrate 410, instead of the

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AlN layer 412.

The LED chip 3 is disposed on the bottom surface of the depression 411 of the ceramics substrate 410, and Au layers 480 are inserted between the Ni/Al/Pt/Au layer 380 and the wiring layer 414 of the ceramics substrate 410. The Au layers are the Au bumps that are placed on the wiring layer 414 when the chip is mounted, as explained already. As shown in FIG.13B, the LED chip 3 is connected onto a cathode pad 414a, which is a larger one of two pads (the cathode pad 414a and anode pad 414b) that are extending from facing sides of the inside wall of the depression 411. The cathode electrode 350 and anode electrode 360 of the LED chip 3 are connected to the cathode pad 414a and anode pad 414b via bonding wires 481 and 482, respectively.

In the present embodiment, the LED chip 3 and the pads 414a and 414b on the ceramics substrate 410 are connected by wire bonding. However, it is also possible, instead of connecting electrically by wire bonding, that the LED chip 3 and the pads are connected using bumps or by soldering, by a metal piece disposed in a penetrating hole in the LED chip 3 so as to dispose an electrode on a back surface of the LED chip 3.

Structures of the reflective mirror 450, the resin layer 460, and the lens layer 470 are the same as in the LED chip 1, and therefore not explained in detail.

Although not shown in the drawing, the LED module according to the present embodiment has substantially the same structure as the LED module in FIG.5, other than the structure of and connection to the LED chip 3. A lighting apparatus

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having the LED module may be the same structure as shown in FIG.8, or may have a different structure.

The lighting apparatus having the LED chip 3 according to the present embodiment irradiates white light having a color temperature of 4600 K and an average CRI of 90 by supplying a DC electricity of 150 mA to the LED module. A total luminous flux of this lighting apparatus is 1000 lm, and on-axis luminous intensity is 2000 cd. A spectral distribution of the white light irradiated by the lighting apparatus according to the present embodiment is illustrated in FIG.14.

As shown in FIG.14, a relative intensity of an emission spectrum shows a sharp peak in vicinity of wavelengths 620 nm, and is relatively high in vicinity of wavelengths between 450 nm and 620 nm.

[Advantages of LED Chip 3, LED Module Using LED Chip 3, and Lighting Apparatus Using LED Chip 3]

As described above, the LED chip 3 according to the present embodiment is such that the depressions 326a are on a side of the p-electrode 326 which the near-ultraviolet light from the $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N \times 5$ luminous layer 323 passes through, and the membrane 370 is formed so as to cover the depressions 326a. When the LED chip 3 is mounted to the ceramics substrate 410, a vacuum collet sticks to the surface of the membrane 370, then the ultrasonic waves are applied after the LED chip 3 is pressed to the ceramics substrate 410. By forming the membrane 370, it is possible to mount the LED chip 3 without fail, because the vacuum collet firmly sticks to the LED chip 3, and the ultrasonic energy is not lost in the depressions 326a of the p-electrode 326. Further, because

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the loss of the ultrasonic energy in the depressions 326a is small and the surface of the depressions 326a is protected by the membrane 370, the depressions 326a are not destroyed by application of the ultrasonic waves when the chip is mounted. Such advantages are the same as the case of the first embodiment.

Because of the above advantages that the LED chip 3 has, it is possible that the LED module and the lighting apparatus having the LED chip 3 obtains, as in the case of the first embodiment, high light extraction efficiency and excellent heat dispersion property because the LED chip 3 is firmly attached when mounting. Thus, the LED module and the lighting apparatus having the LED chip 3 have such advantages that high light-emission efficiency and longevity.

Further, as in the LED chip 3 according to the present embodiment, when the p-electrode 326 and n-electrode 327 are disposed on one side, it is necessary, in general, to remove the luminous layer at the part where the n-electrode 327 is disposed, and therefore it is unavoidable that a luminous area becomes smaller. However, in the LED chip 3 according to the present embodiment, the light emitting elements are connected using the bridge wiring 380 in the LED chip 3, and it is possible to make the n-electrode 327 smaller in comparison with a case in which the light emitting elements are connected using bonding wires or bumps (For example, the n-electrode 327 can be 10 μm square, when it is 100 μm square when using bonding wires or bumps). Thus, by using the LED chip 3, the luminous area becomes wider, because it is possible to make an area of the p-electrode 326 under which the luminous layer is formed wider according to an area that the n-electrode 327 is made

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smaller.

For example, when a size of each light emitting element of the LED chip is 285 μm × 400 μm, and an overlapping margin for attachment is 25 μm wide from an edge, an effective area becomes 82250 μm^2. Further, the luminous area per light emitting element of the LED chip 3, in which the area of the n-electrode accounts for 10 × 10 μm^2, according to the present embodiment becomes 82250 - 10 × 10 = 82150 μm^2. Calculating in the same way, a luminous area per light emitting element of a conventional LED chip, in which the area of the n-electrode accounts for 100 × 100 μm^2, becomes 72250 μm^2. In comparison, it is clear that the luminous area of the LED chip 3 according to the present embodiment is 1.13 times as large as that of the conventional LED chip.

Moreover, by making the luminous area wider, the current density may be reduced when the same current is supplied as the case in which the luminous area is smaller, and thus it is possible either to suppress the heat, or to increase quantity of light by supplying more current till the level of current density becomes the same as the case of the smaller luminous area.

As described above, the LED chip 3 according to the present embodiment has an advantage that, when the light emitting elements are connected using bridge wiring on the chip, it is possible to increase the luminous area even when the total chip area is the same, in comparison with the case in which the LED chip made of one light emitting element is connected by wire bonding or bumps.

Although the non-doped 4H-SiC substrate 310 is used as

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a substrate in the LED chip 3 according to the present embodiment, it is also possible to use a substrate of an n-SiC substrate on which a layer having a high resistance such as an AlGaN layer is formed. In this case, it is necessary that a separating groove does not completely remove the layer having high resistance.

Moreover, if the cathode electrode is connected to the n-SiC substrate in the LED chip 3, it is not necessary to use a bonding wire between the cathode pad and the cathode electrode.

As explained above, when the n-SiC substrate is used in place of the non-doped 4H-SiC substrate, it is possible to disperse the generated heat to the mounting substrate even when the luminous layer comes upper side, because the n-SiC substrate has as high heat conductance as metal.

It is also possible to use sapphire, AlN, and Si for the substrate, even though heat conductance of those material is not as good.

[Third Embodiment]

Next, a structure of an LED display apparatus 6 according to a third embodiment of the present invention is explained with reference to FIG.15.

As shown in FIG.15A, the LED display apparatus 6 according to the present embodiment is such that a reflective mirror 62 and a lens 63 are layered, in a stated order, in an area on a main surface of a composite substrate 61, and 256 light emitting units 66 are formed in 16 × 16 in this area. Connecting terminals 64 and 65 that connect between the LED display apparatus 6 and a driving circuit to drive the LED display

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apparatus 6 are formed in the other areas on the main surface of a composite substrate 61. The connecting terminals 64 and 65, respectively, are connected to the LED chip 67 that constitutes each of the light emitting units 66 via wiring layers 615 and 616 formed as a part of the composite substrate 61 (See FIG.15B).

As shown in FIG.15B, the light emitting units 66 of the LED display apparatus 6 has such a structure that the LED chip 67 is attached to a conductive land 617 that is disposed on the main surface of the composite substrate 61, i.e. the LED chip 67 is mounted to the composite substrate 61 by flip-chip bonding. Then, the reflective mirror 62 is disposed so as to surround the LED chip 67, and the lens 63 is formed so as to cover the LED chip 67 and the reflective mirror 62.

The composite substrate 61 is formed by a metal layer 611 and three insulating layers 612-614, and wiring layers 615 and 616 are formed, respectively, between the insulating layer 613 and 614 and between the insulating layers 612 and 613. The conductive land 617 and each of the wiring layers 615 and 616 are connected by a via hole.

As shown in FIG.15B, the LED chip 67 has the same structure as the light emitting element 20 in the LED chip 1 shown in FIG.2. Further, as shown in an enlarged part of FIG.15B, minute depressions 6711 having a square shaped opening are formed on an entire surface of a non-doped GaN substrate 671 on a side that the light is irradiated (upper side in the drawing). The depressions 6711 are formed at an interval of 1 μm, for example.

A membrane 672 is formed on the non-doped GaN substrate

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671 so as to fill the depressions 6711. As in the first embodiment, the membrane 672 is mainly made of a polyimide resin having transmissivity, and contains a yellow phosphor material such as $(Sr, Ba)_2SiO_4:Eu^{2+}$, and ultrafine particles such as SiO_2 in a dispersed state. The membrane 672 is formed so as to be 80 μm thick at the thinnest part (parts that do not have the depression 6711), and so that a surface is substantially flat. A structure of the membrane 672 is the same as in a case of the first embodiment.

With the LED display apparatus 6 according to the third embodiment, as in the first embodiment, it is possible to protect the depression 6711 and suppress displacement of the LED chip 67 when the LED chip 67 is mounted to the composite substrate 61 by flip-chip bonding. Further, by having the membrane 672, the ultrasonic energy applied does not become weakened between the vacuum collet and LED chip when the vacuum collet applies the ultrasonic waves.

With the LED display apparatus 6 having the above structure, the depressions 6711 on the non-doped GaN substrate 671 of the LED chip 67 are protected, and thus it is possible to obtain high light extraction efficiency, as well as high light emitting efficiency due to a firm attachment in mounting.

The LED display apparatus 6 according to the present embodiment illustrates an example of the present invention, and the present invention is not restricted by this embodiment. For example, it is possible to use TFT substrate instead of the composite substrate 61.

[Fourth Embodiment]

A structure of a fourth embodiment is explained below,

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with reference to FIG.16. In the present embodiment, a Vertical Cavity Surface Emitting Laser (hereinafter referred to as VCSEL) device is taken as an example.

As shown in FIG.16A, a VCSEL device 7 according to the present embodiment is such that a cathode electrode 72 is disposed on one of main surfaces of a SiC substrate 71 (lower surface in FIG.16A), a phosphor layer 74 is formed on a part of the other side of main surfaces (upper surface in FIG.16A), and an anode electrode 75 is disposed on the rest of the same side of main surfaces. A total number of 36 VCSEL cells 73 are formed in the area of the SiC substrate 71 that is covered by the phosphor layer 74. As shown in the drawing by a partial cutout part, an anode electrode 738 (See FIG.16B) of each of the VCSEL cells 73 and the anode electrode 75 disposed on the main surface of the SiC substrate 71 are connected by an Al bridge wiring 76.

As shown by a sectional view of FIG.16B taken at a plane indicated by C-C, there are 6 VCSEL cells 73 at the section of the VCSEL device 7. As shown in an enlarged view of FIG.16B, the VCSEL cell 73 is formed the SiC substrate 71, the cathode electrode 72 that is formed on one of the main surfaces of the SiC substrate 71, and layers that are layered on the other side of the main surfaces on which the phosphor layer 74 is formed. The layers that are layered on the other side of the main surfaces are formed on the SiC substrate 71 such that a semiconductor DBR layer 731, an n-clad layer 732, an active layer having a multiplex quantum well structure (hereinafter referred to as MQW layer) 733, and a p-clad layer 734 are layered in a stated order, and an SiN passivation layer 735 and an

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anode electrode 736 are formed so as to enclose a layered part of the above layers. Further, an ITO layer 737 and a dielectric DBR layer are layered in a stated order on a part of a surface of the p-clad layer 734 that is enclosed by the anode electrode 736.

As explained above, each of the VCSEL cells 73 of the VCSEL device 7 is structured by the SiC substrate 71, the cathode electrode 72, and the above-described more than one components 731-738. Further, a characteristics of the above VCSEL device 7 according to the present embodiment is in that the phosphor layer 74 covers an entire part where the VCSEL cells 73 are formed. Specifically, as in the first to third embodiments, covering an entire VCSEL cells 73 by the phosphor layer 74 protects the anode electrode 736 and such of each of the VCSEL cells 73 from being damaged when mounting the VCSEL device 7, and also ensures an accurate mounting. In addition, it is possible to obtain the same effect as in the first and second embodiments.

Next, a method of manufacturing the VCSEL device 7 according to the present embodiment is explained with reference to FIGs.17 and 18. Both FIGs.17 and 18 illustrate the same one of the VCSEL cells 73, for convenience.

As shown in FIG.17A, the semiconductor DBR layer 731, the n-clad layer 732, the MQW layer 733, and the p-clad layer 734 are layered, in a stated order, on one of the main surfaces of the SiC substrate 71.

As shown in FIG.17B, a mask (not shown in the drawing) is formed at an area of a surface of the p-clad layer 734, specifically, an area where the VCSEL cells 73 are formed,

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and etching is performed with the n-clad layer 732 as a stopper layer. By this etching, the MQW layer 733 and p-clad layer 734 remain in projections on an area on the surface of the n-clad layer 732.

As shown in FIG.17C, the semiconductor DBR layer 731 and n-clad layer 732 are etched so as to be slightly larger in section than the MQW layer 732 and p-clad layer 734. After this, as shown in FIG.17D, the Al bridge wiring 76 is formed so as to reach the surface of the SiC substrate 71 and a part of the surface of the n-clad layer 734.

As shown in FIG.18E, the SiN passivation layer 735 is formed so as to cover a surface that the Al bridge wiring 76 and n-clad layer 732 remain and the area of the surface the p-clad layer 734.

Next, as shown in FIG.18F, the anode electrode 736 is formed on an area of a surface of the SiN passivation layer 735 and the area of the p-clad layer 734.

As shown in FIG.18G, an ITO layer 737 and a dielectric DBR layer 738 are layered in a stated order at the area of the surface of the p-clad layer 734 surrounded by the anode electrode 736. In addition, as shown in FIG.18H, the cathode electrode 72 is formed on an entire surface of the other main surface of the SiC substrate 71.

Although not shown in the drawing, after a step shown in FIG.18H, the phosphor layer 74 is formed, where necessary, on the surface of the SiC substrate 71 where the above elements 731-738 are formed. Finally, the VCSEL cells 73 of the VCSEL device 7 is completed after the SiC substrate 71 is cut into units as shown in FIG.16.

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As described above, in manufacturing the VCSEL device 7, the phosphor layer 74 is formed so as to form an entire area where the VCSEL cells 73 to be formed. The phosphor layer 74 is formed so as that its surface becomes substantially flat. Therefore, an advantageous effect may be obtained because it is possible to mount the VCSEL device 7 to the substrate using the surface of the phosphor layer 74.

Although the present embodiment is explained by taking the VCSEL device as an example, the same effect may be obtained when applied to a Resonant Cavity Light Emitting Diode (RC-LED) that has substantially the same structure as the VCSEL device.

[Other Matters]

The first to fourth embodiments are examples to explain the characteristics of the structures and effects of the present invention, and the present invention is not restricted by these embodiments. For example, in the first and second embodiments, the white light irradiated from each of the light emitting units 120 is generated by the light from the luminous layer mixing with light generated by the luminous substance being excited by the light from the luminous layer. However, it is also possible that either the white light or mono color light is generated using mono-color LED modules, or mixing mono-color LED lights.

Moreover, although the membranes 70 and 370 in the LED chips 1 and 3 contain the phosphor material and such, the phosphor material and such do not necessarily have to be contained. Basically, these membranes are formed in order to allow the vacuum collet to stick to the LED chips 1 and 3 more firmly when the LED chips are mounted, as well as to

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reduce the loss in the ultrasonic energy. Thus, whether or not the phosphor material is contained is not an essential part of the present invention.

In addition, the examples of the material to form the membrane 70 listed in the first embodiment are organic resins such as polyimide, epoxy, and silicone. However, it is also possible to use glass by the sol-gel method or low-melting glass for the membrane 70. Specific examples of the glass material include (1) a glass material using metal alkoxide (such as tetramethoxysilane and tetraethoxysilane) as starting material, (2) a glass material made from polymer ceramic precursor such as perhydropolysilazane, and (3) a glass material made from such as phosphorus oxide and boronic oxide.

With any of the above listed glass materials, it is possible to form a glass layer (membrane) whose upper surface is substantially flat and filling the depressions, by applying the glass material on the depressions using such as potting and spin-coating, drying the glass material, and baking the glass material at a temperature of several hundred degrees centigrade.

Further, with the above semiconductor light emitting devices explained in the first to fourth embodiments, the advantages that the vacuum collet firmly sticks to the LED chip may be obtained even without applying the ultrasonic waves when the LED chip is mounted.

It is also possible to modify the structures of the display device 6 and VCSEL device 7 explained in the third and fourth embodiments, respectively, within a scope in which the effects of the present invention may be obtained.

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Moreover, the present invention may be applied to a Surface Mount Device (SMD) illustrated in FIG.19. As shown in FIG.19, an SMD 8 to which the present invention is applied is structured so that a pair of external electrodes 82a and 82b are disposed on a mounting substrate 81, and a LED chip 82 is mounted to the electrodes 82a and 82b by flip-chip bonding with bumps therebetween, and the LED chip 82 and electrodes 82a and 82b over the mounting substrate 81 are covered by a resin package 85.

As shown in an enlarged part in FIG.19, the LED chip 82 of the SMD 8, like the LED chip 67 in the second embodiment described above, has a surface with depressions 8311, and a membrane 8322 covers the LED chip 67 so as to fill the depressions. With the SDM 8 having the above structure, it is possible to obtain the same effects as the above first to fourth embodiments, because damages to the depressions in mounting the LED chip 82 to the mounting substrate 81 may be reduced.

Industrial Applicability

The present invention is effective to realize a high power semiconductor light emitting device having high light output, and a lighting apparatus and a display device using such a semiconductor light emitting device.

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CLAIMS

1. A semiconductor light emitting device having a luminous layer, comprising:

a light transmission layer disposed over a main surface of the luminous layer, and having depressions on a surface facing away from the luminous layer; and

a transmission membrane disposed on the light transmission layer so as to follow contours of the depressions, wherein

light from the luminous layer is irradiated so as to pass through the light transmission layer and the transmission membrane.

2. A semiconductor light emitting device according to Claim 1, wherein a surface of the membrane facing away from the light transmission layer is substantially flat.

3. A semiconductor light emitting device according to Claim 1, wherein a main component of the membrane is one of polyimide, epoxy, and silicone.

4. A semiconductor light emitting device according to Claim 1, wherein a main component of the membrane is glass.

5. A semiconductor light emitting device according to Claim 1, wherein the membrane contains a luminous substance that

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is excitable by the light from the luminous layer.

6. A semiconductor light emitting device according to Claim 5, wherein the light from the luminous layer is converted into white light by passing through the membrane.

7. A semiconductor light emitting device according to Claim 5, irradiating white light generated by light from the luminous substance being excited mixing with the light from the luminous layer.

8. A semiconductor light emitting device according to Claim 1, wherein the depressions are at an interval equal to or greater than $\lambda/4$, λ being a wavelength of the light from the luminous layer.

9. A semiconductor light emitting device according to Claim 1, wherein

the light transmission layer is formed from at least a light transmission substrate, and

the luminous layer is sandwiched between a plurality of layers and is disposed over the light transmission substrate.

10. A semiconductor light emitting device according to Claim 9, wherein the depressions are on a main surface of the light transmission substrate facing away from the luminous layer.

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11. A semiconductor light emitting device according to Claim 9, wherein the light transmission substrate is made of a material having a refractive index that is substantially equal to a refractive index of the luminous layer.

12. A semiconductor light emitting device according to Claim 11, wherein the material for the light transmission substrate is selected from a group of GaN, SiC, and AlN.

13. A semiconductor light emitting device according to Claim 9, wherein a reflective film is disposed on a surface of the luminous layer facing away from the light transmission layer.

14. A semiconductor light emitting device according to Claim 1, being a light emitting diode device.

15. A semiconductor light emitting device according to Claim 1, being a Vertical Cavity Surface Emitting Laser device.

16. A semiconductor light emitting device according to Claim 1, being a Resonant Cavity Light Emitting Diode device.

17. A semiconductor light emitting device according to Claim 1, being a Surface Mount Device.

18. A lighting apparatus comprising a mounting substrate, and a semiconductor light emitting device mounted on a pad

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on a surface of the mounting substrate, wherein:

the semiconductor light emitting device includes;

a luminous layer;

a light transmission layer disposed over a main surface of the luminous layer, and having depressions on a surface facing away from the luminous layer; and

a transmission membrane disposed on the light transmission layer so as to follow contours of the depressions, and

light from the luminous layer is irradiated so as to pass through the light transmission layer and the transmission membrane.

19. A lighting apparatus according to Claim 18, wherein a surface of the membrane facing away from the light transmission layer is substantially flat.

20. A lighting apparatus according to Claim 18, wherein a main component of the membrane is glass.

21. A display apparatus comprising a mounting substrate, and a plurality of semiconductor light emitting devices each mounted on a pad on a surface of the mounting substrate, wherein

each of the semiconductor light emitting devices includes:

a luminous layer;

a light transmission layer disposed over a main surface

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of the luminous layer, and having depressions on a surface facing away from the luminous layer; and

a transmission membrane disposed on the light transmission layer so as to follow contours of the depressions, and

light from the luminous layer is irradiated so as to pass through the light transmission layer and the transmission membrane.

22. A display apparatus according to Claim 21, wherein a surface of the membrane facing away from the light transmission layer is substantially flat.

23. A display apparatus according to Claim 21, wherein a main component of the membrane is glass.

24. A method of manufacturing a semiconductor light emitting device, comprising steps of:

forming a light transmission layer over a multi-layered body in which the luminous layer is sandwiched between a plurality of layers, the light transmission layer having depressions on a surface facing away from the luminous layer; and

forming a transmission membrane on the light transmission layer so as to follow contours of the depressions.

25. A method of manufacturing a semiconductor light emitting

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device according to Claim 24, wherein a material that forms the membrane contains a luminous substance that is excitable by the light from the luminous layer.

26. A method of manufacturing a semiconductor light emitting device according to Claim 25, further comprising a step of:

polishing the membrane after forming the membrane, till a thickness of the membrane becomes such that irradiated light is desirable white light.

27. A method of manufacturing a semiconductor light emitting device according to Claim 24, wherein a material that forms the membrane contains one of polyimide, epoxy, and silicone.

28. A method of manufacturing a semiconductor light emitting device according to Claim 24, wherein a material that forms the membrane contains glass.

29. A method of manufacturing a semiconductor light emitting device according to Claim 24, wherein

the light transmission layer includes at least a light transmission substrate, and

the depressions are on a main surface of the light transmission substrate facing away from the luminous layer.

30. A method of manufacturing a semiconductor light emitting device according to Claim 29, wherein the light transmission

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substrate is formed by a material selected from a group of GaN, SiC, and AlN.

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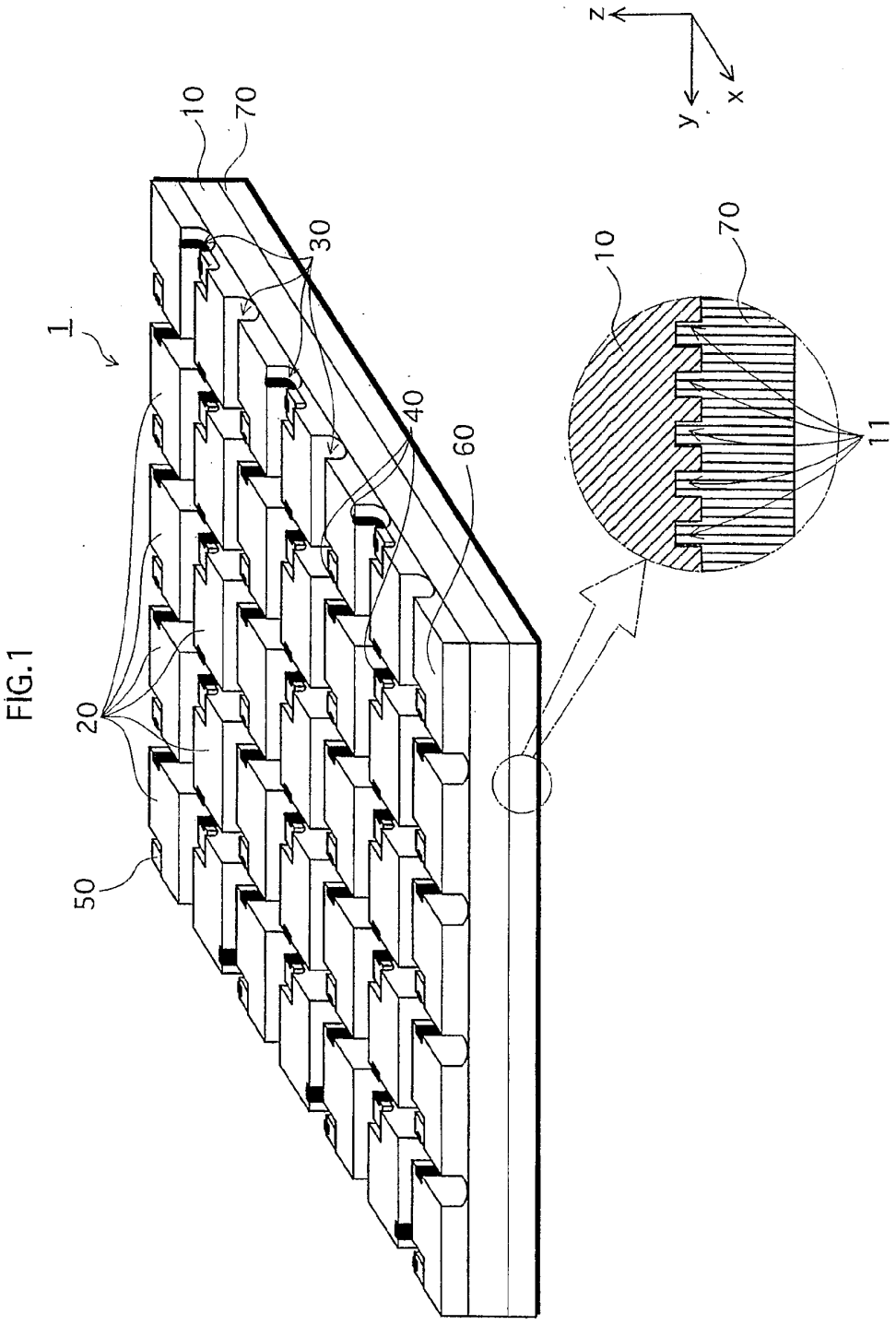


FIG.1

BNSDOCID: <WO_____2005008791A2_I_>

FIG.2A

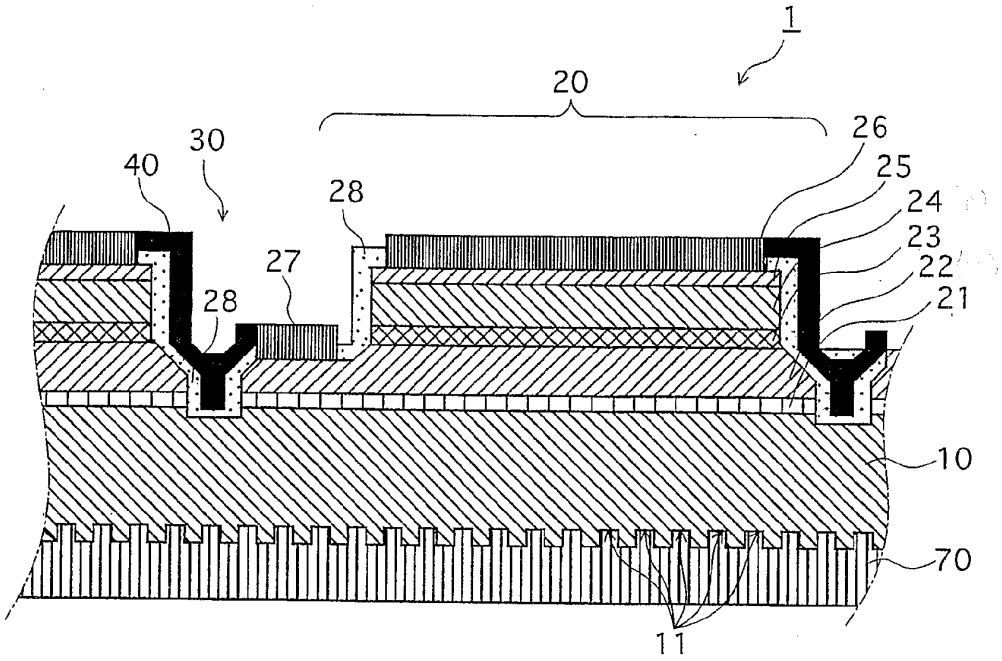
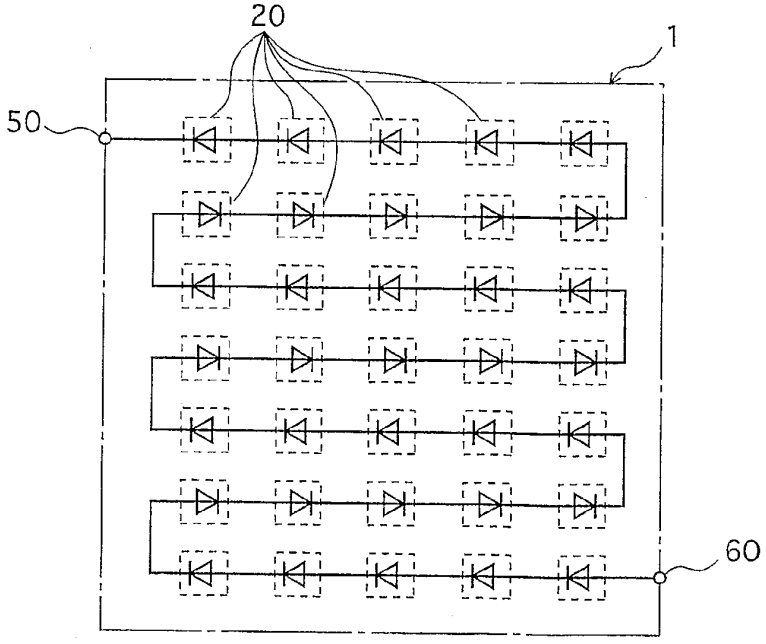


FIG.2B



ISDOCID: <WO_____2005008791A2_I_>

FIG.3A

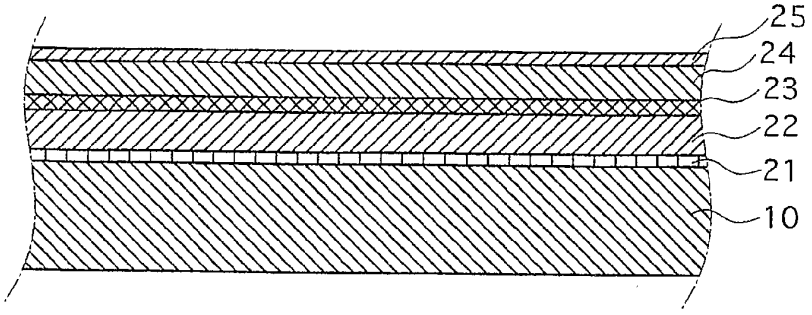


FIG.3B

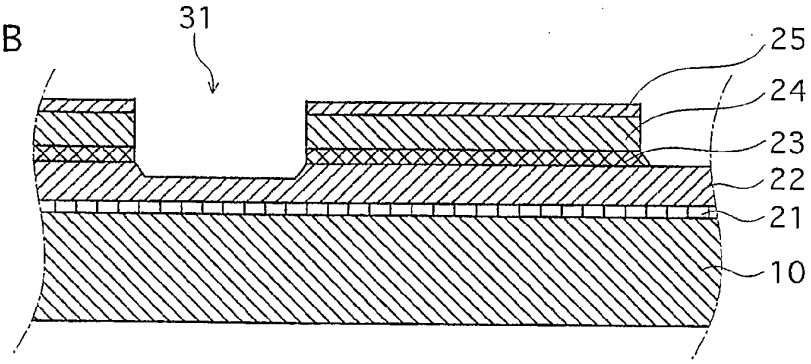


FIG.3C

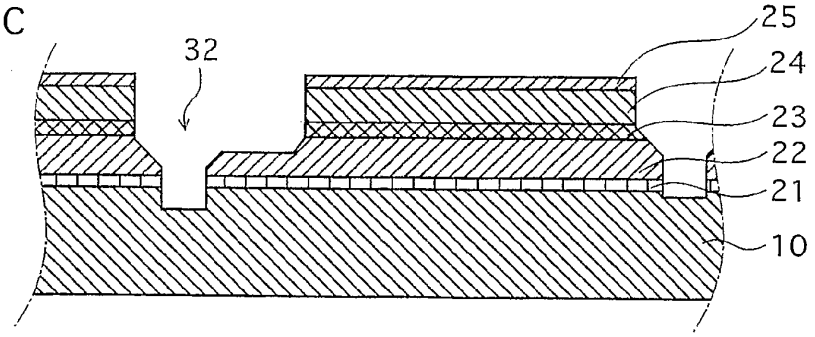
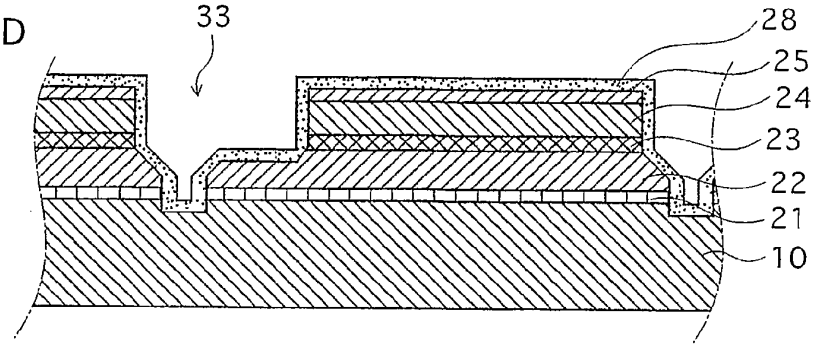


FIG.3D



BNSDOCID: <WO____2005008791A2_I_>

FIG.4E

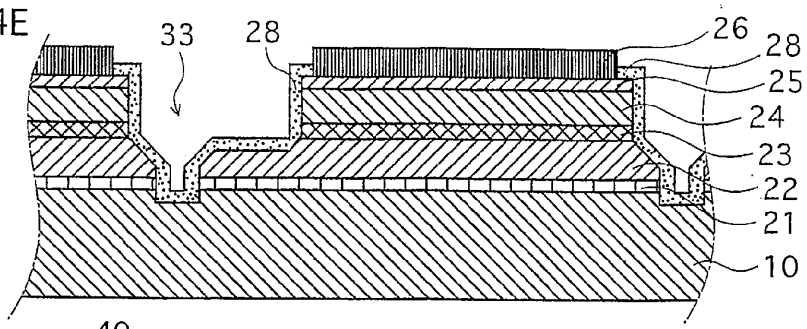


FIG.4F

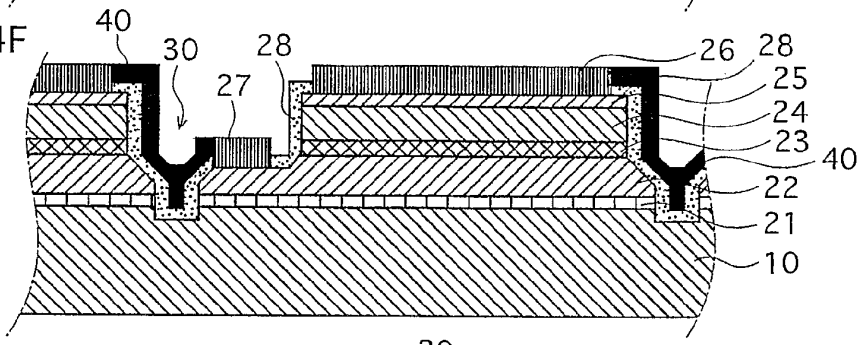


FIG.4G

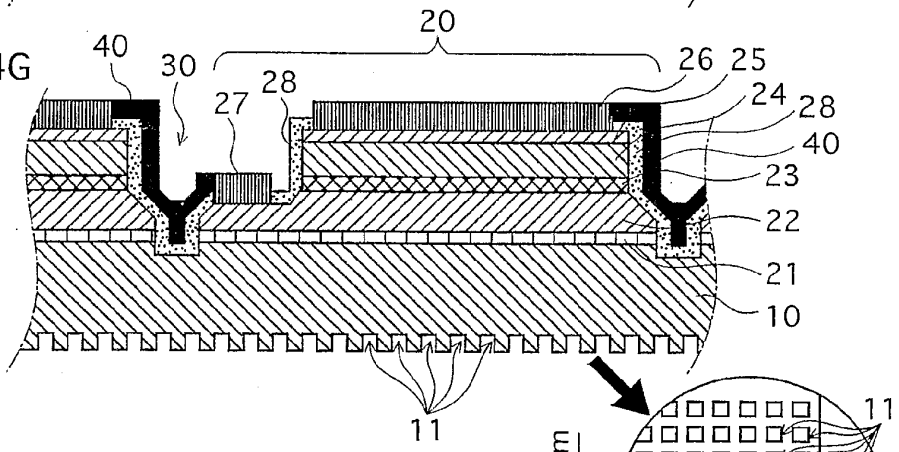
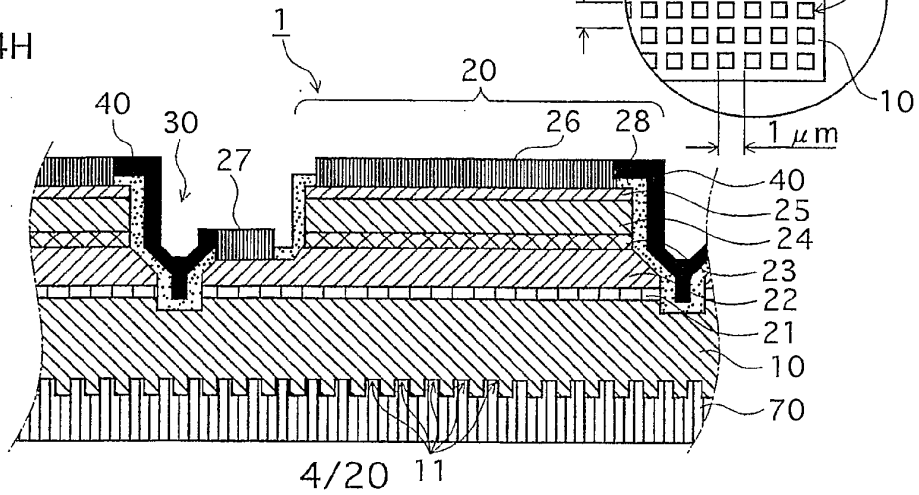


FIG.4H



ISDOCID: <WO_____2005008791A2_I_>

FIG.5A

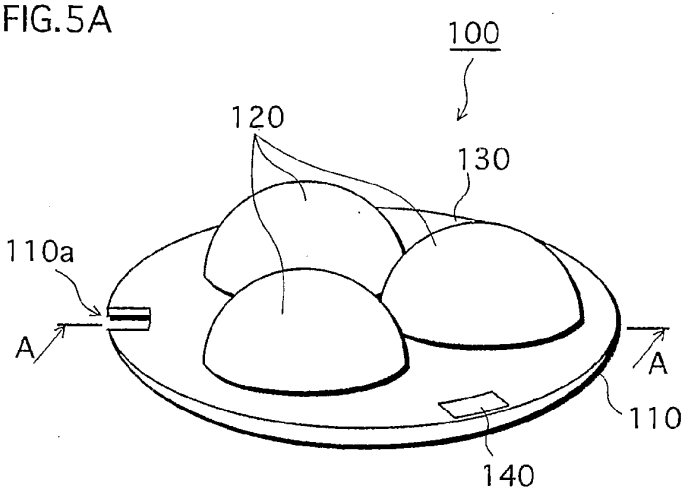
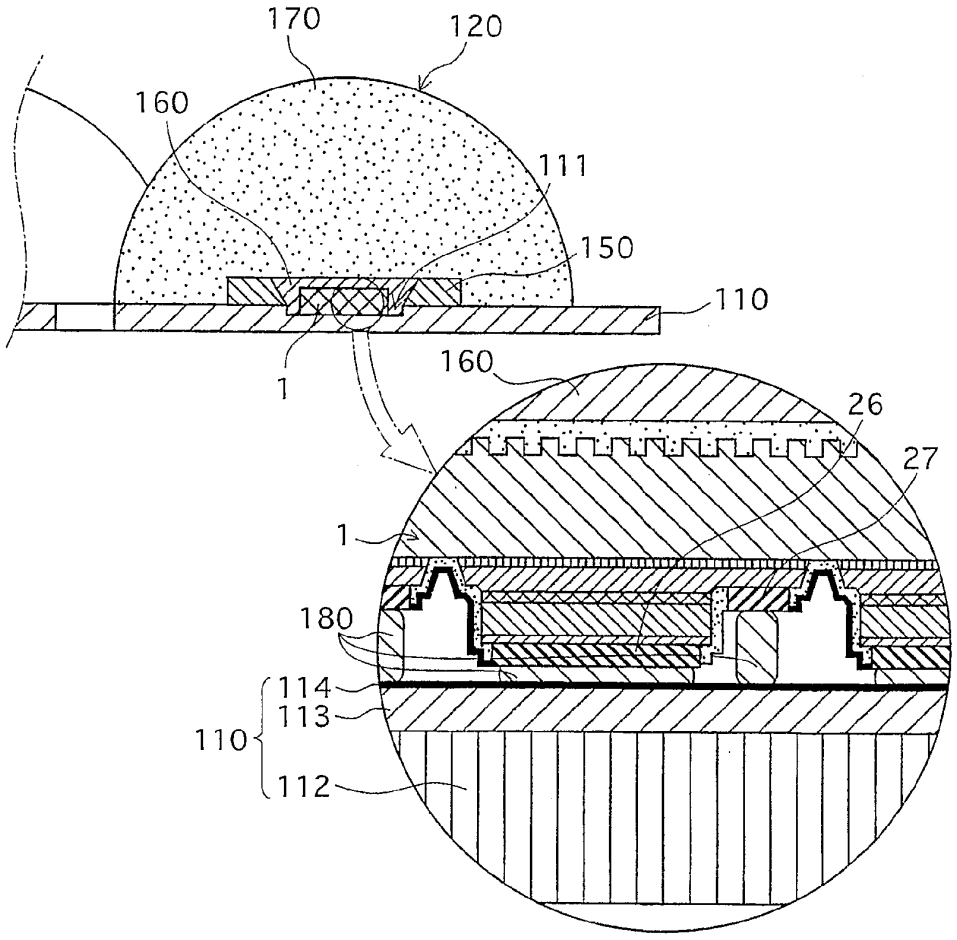
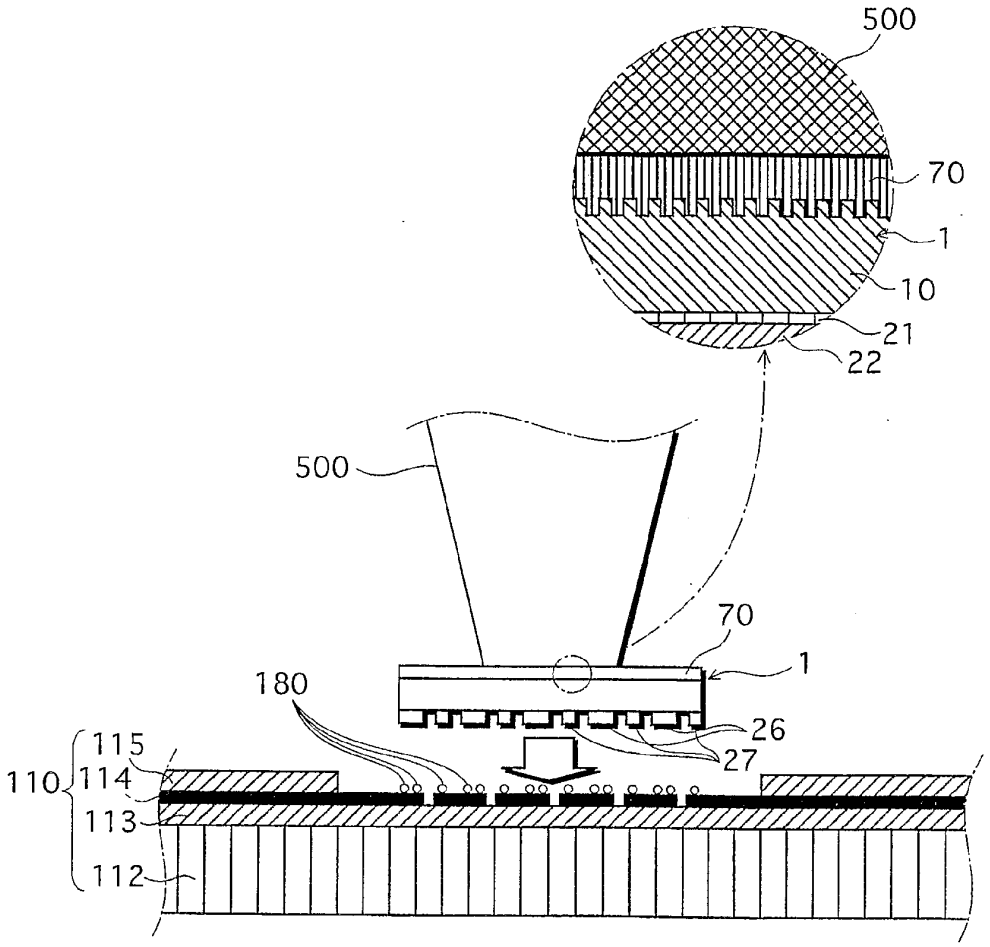


FIG.5B



BNSDOCID: <WO_____2005008791A2_I_>

FIG.6



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FIG.7A

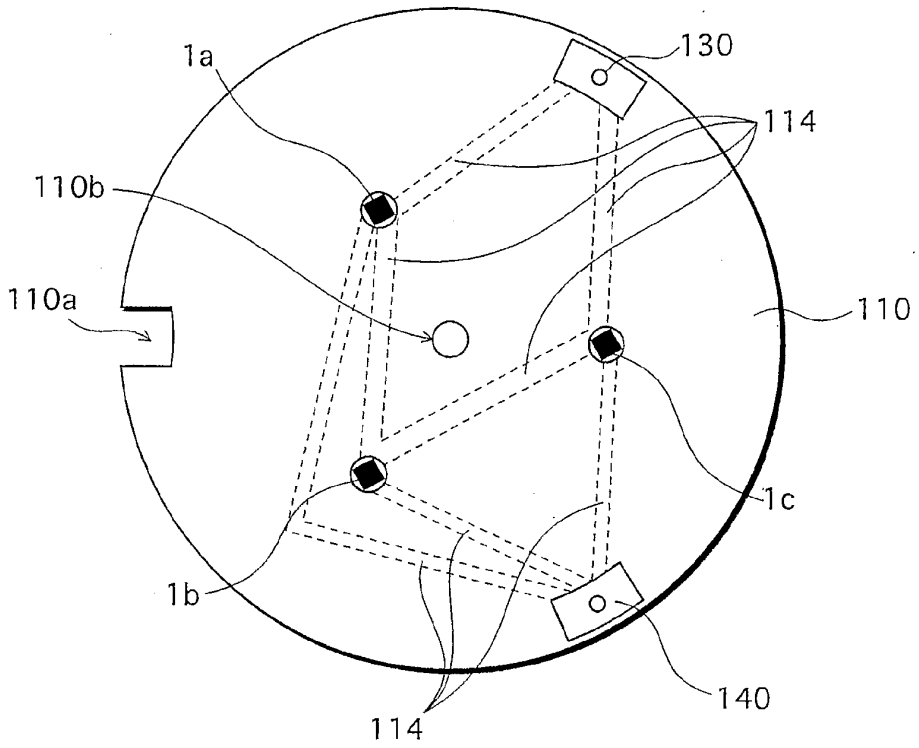
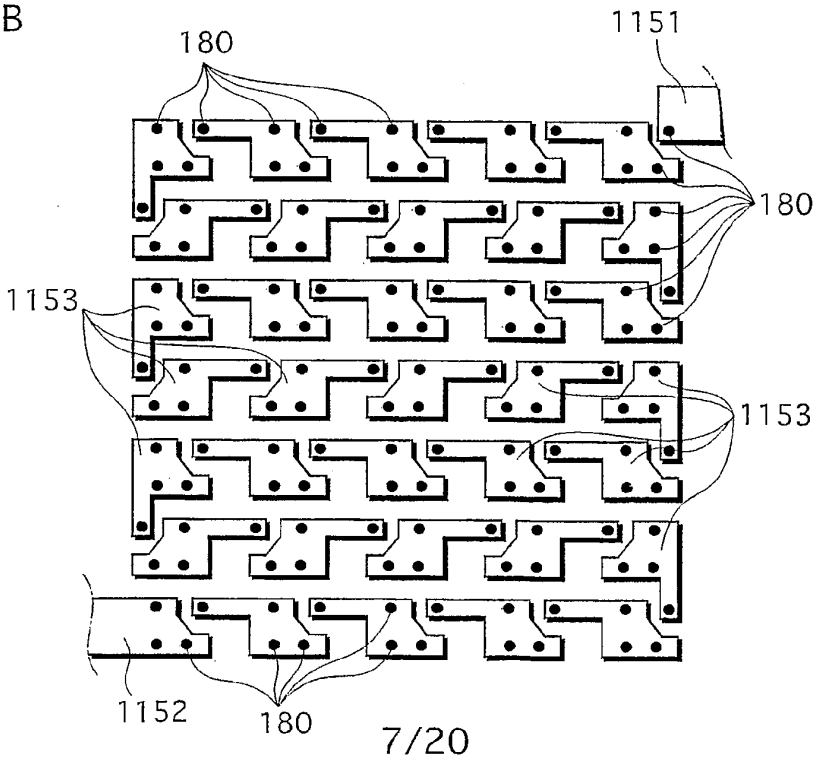


FIG.7B



BNSDOCID: <WO_____2005008791A2_I_>

FIG.8A

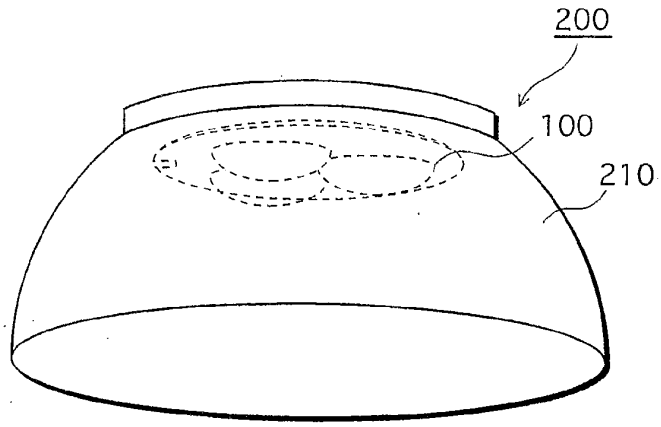
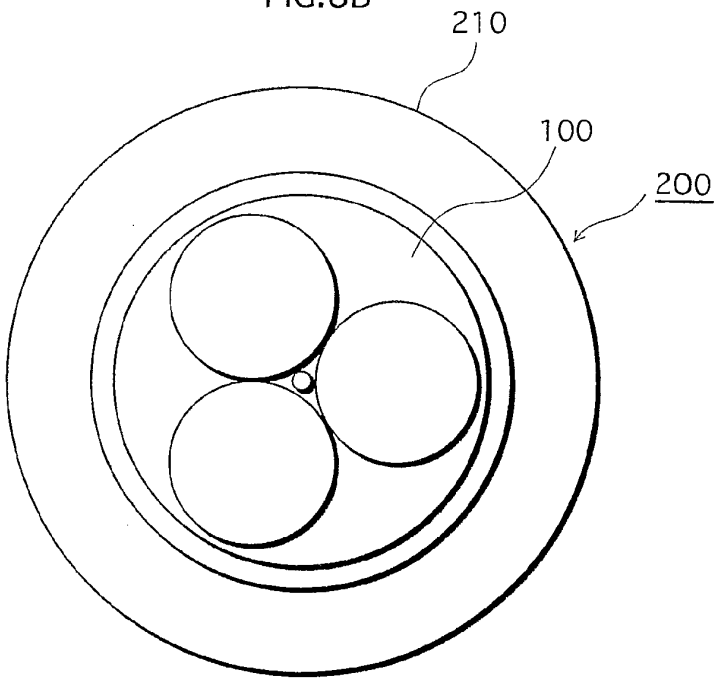
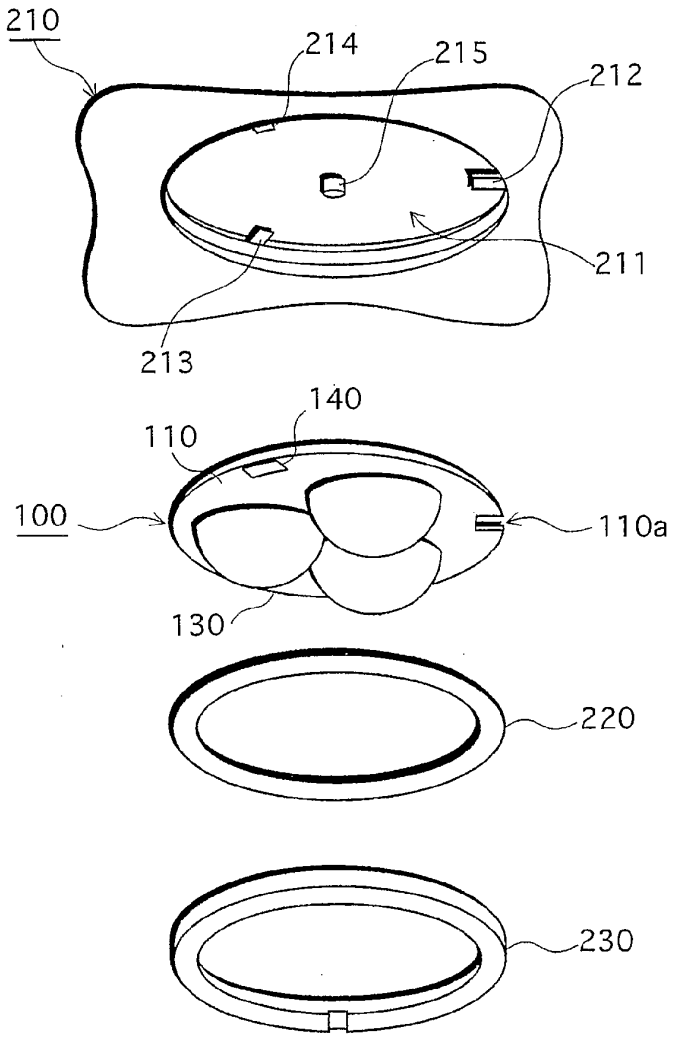


FIG.8B



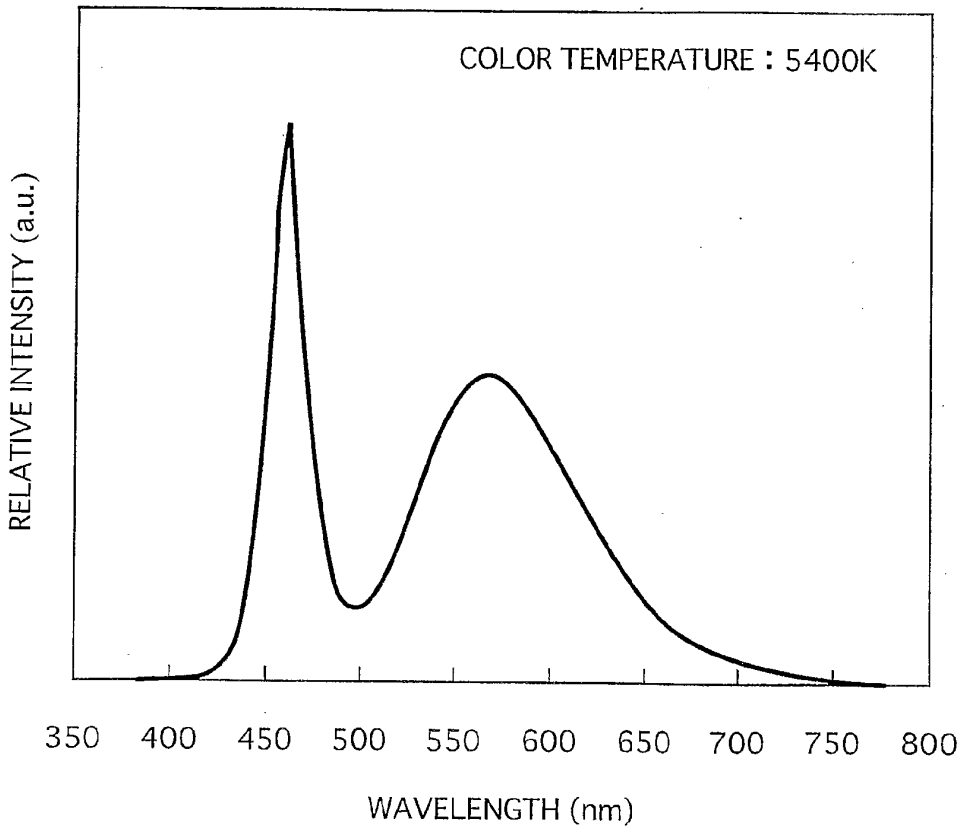
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FIG.9



BNSDOCID: <WO_____2005008791A2_I_>

FIG.10



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FIG.11A

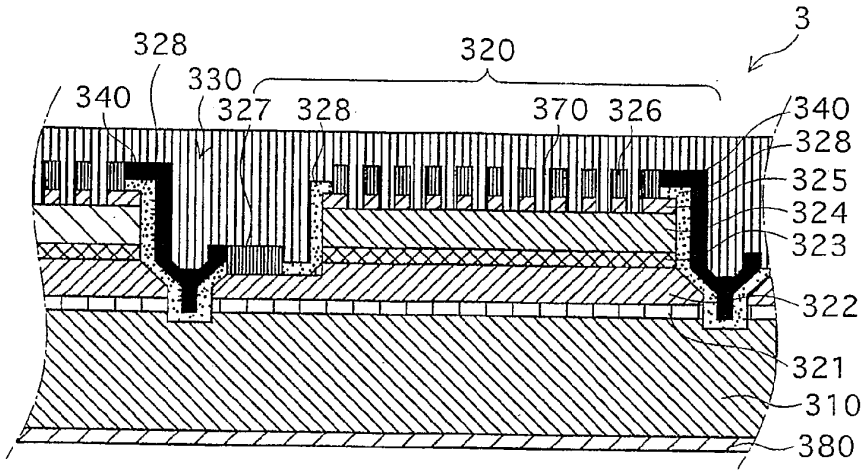
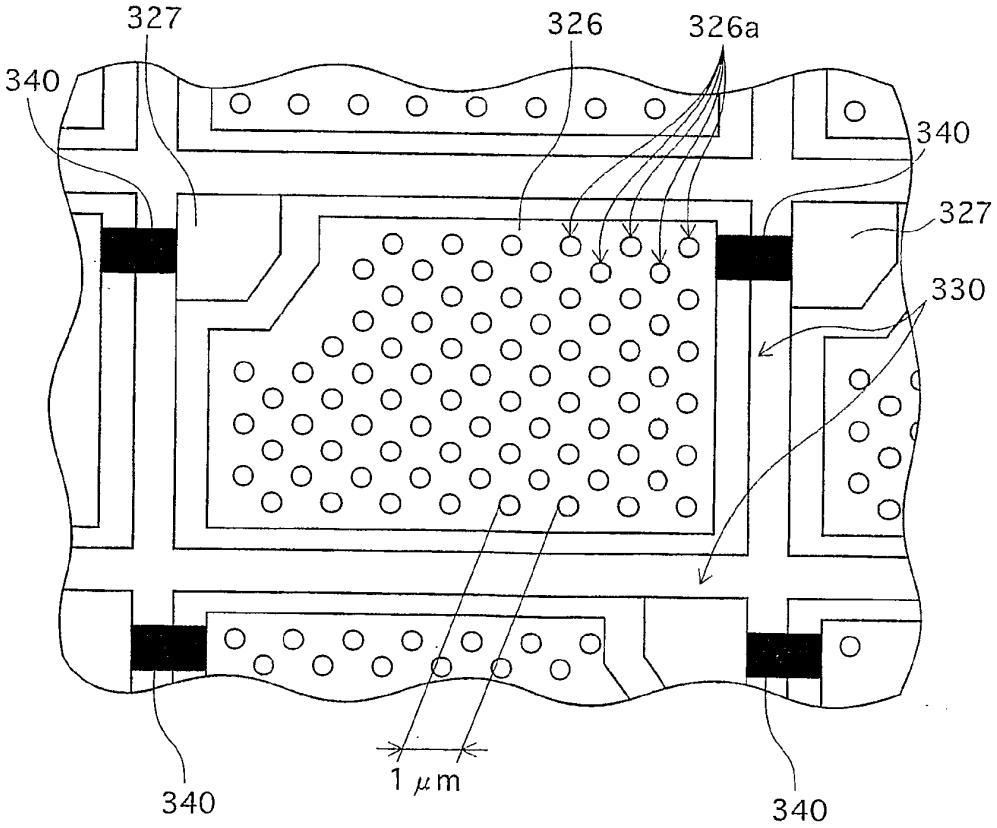


FIG.11B



BNSDOCID: <WO_____2005008791A2_I_>

FIG.12A

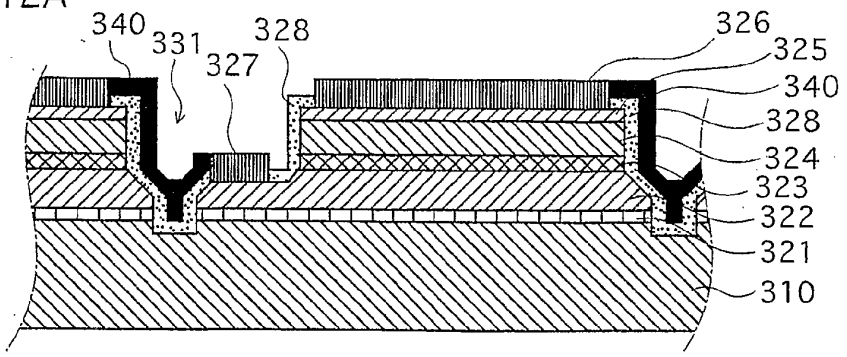


FIG.12B

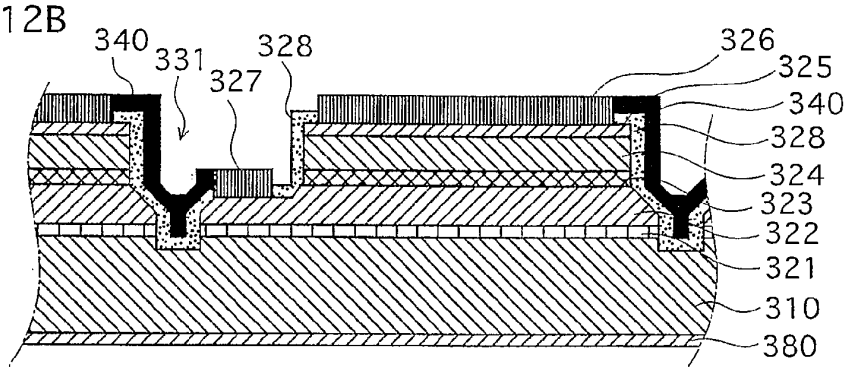


FIG.12C

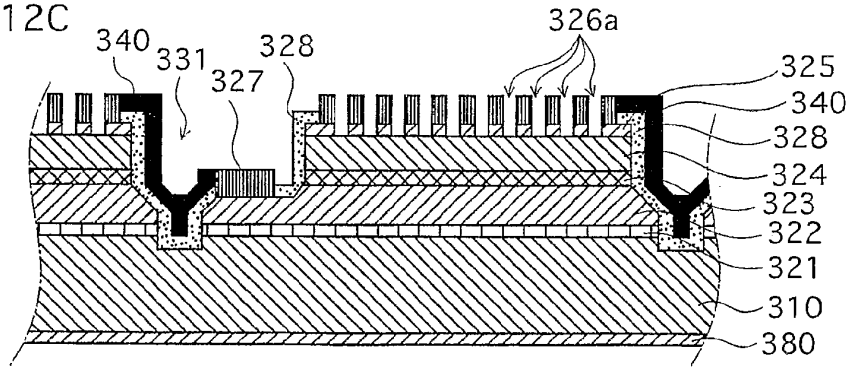
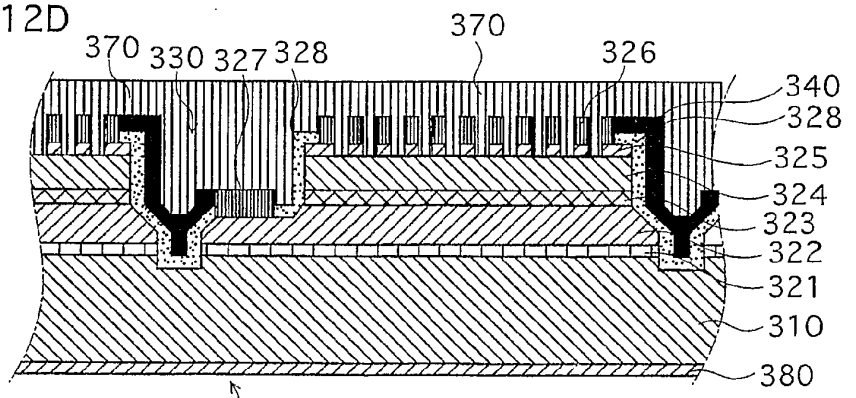


FIG.12D



SDOCID: <WO_____2005008791A2_I_>

FIG.13A

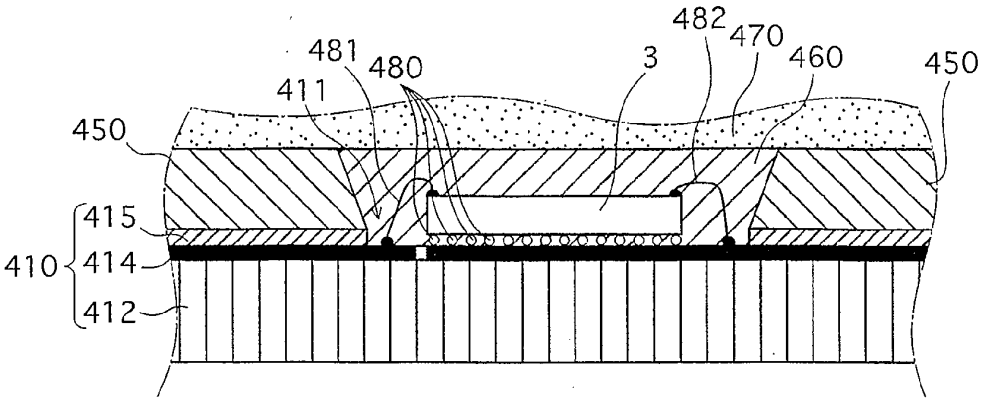
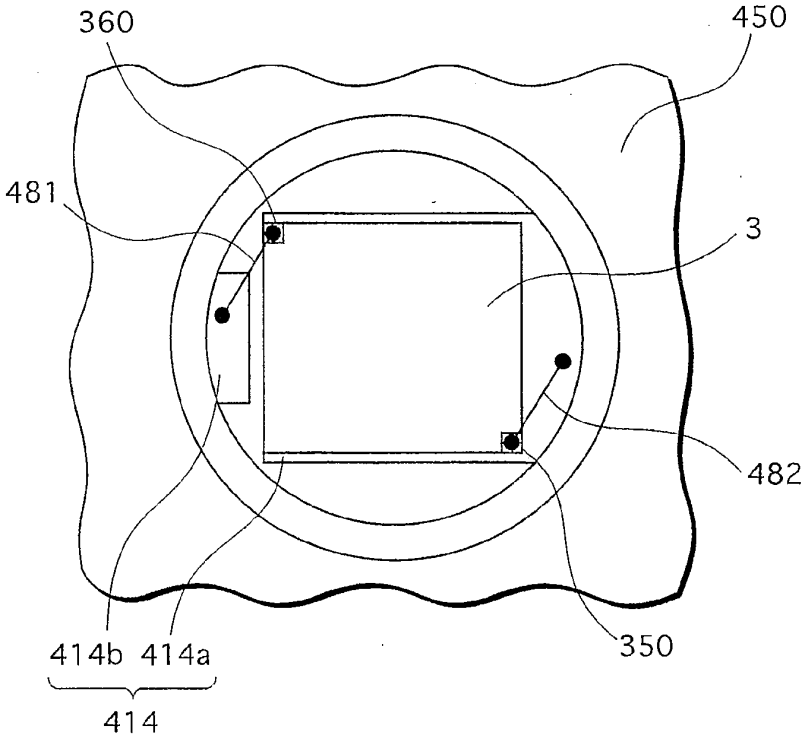
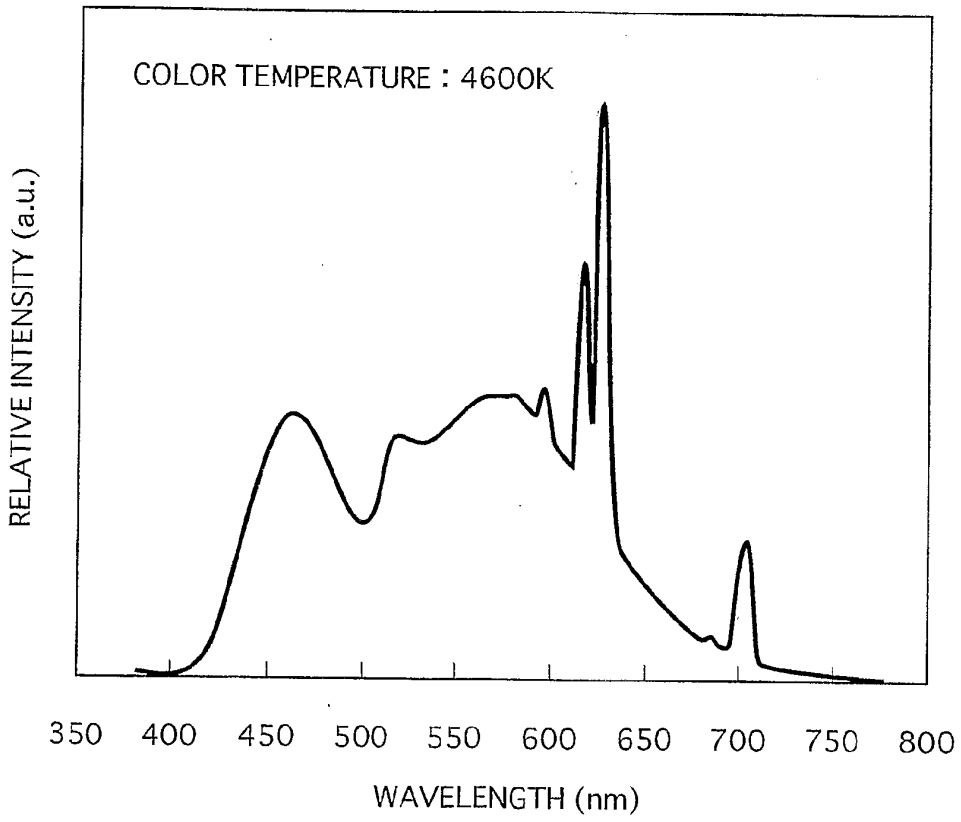


FIG.13B



BNSDOCID: <WO_____2005008791A2_I_>

FIG.14



ISDOCID: <WO_____2005008791A2_I_>

FIG.15A

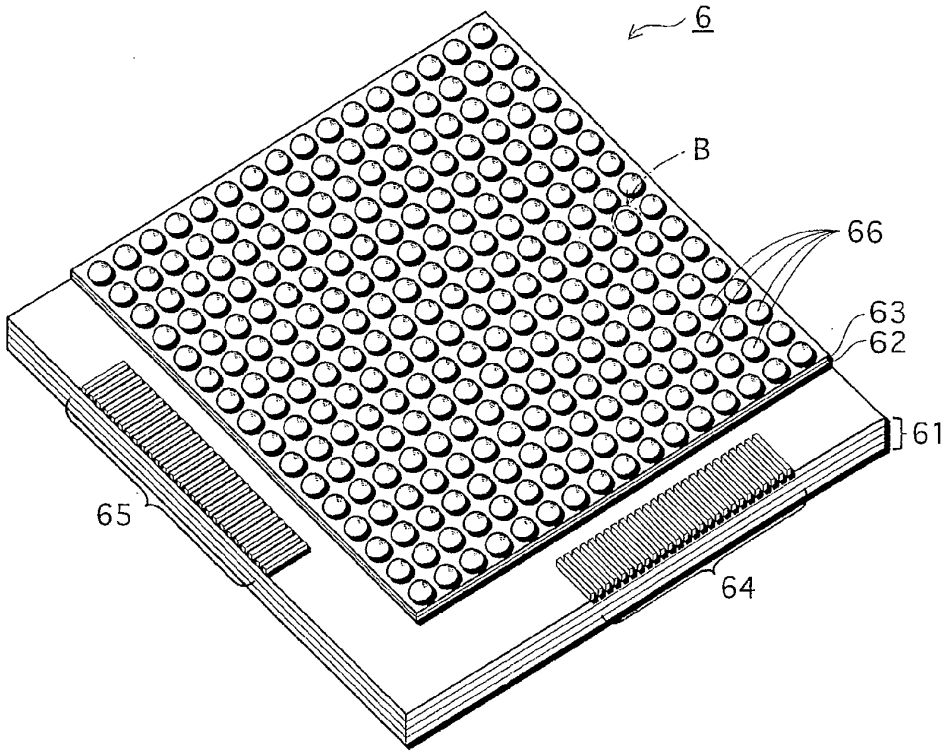
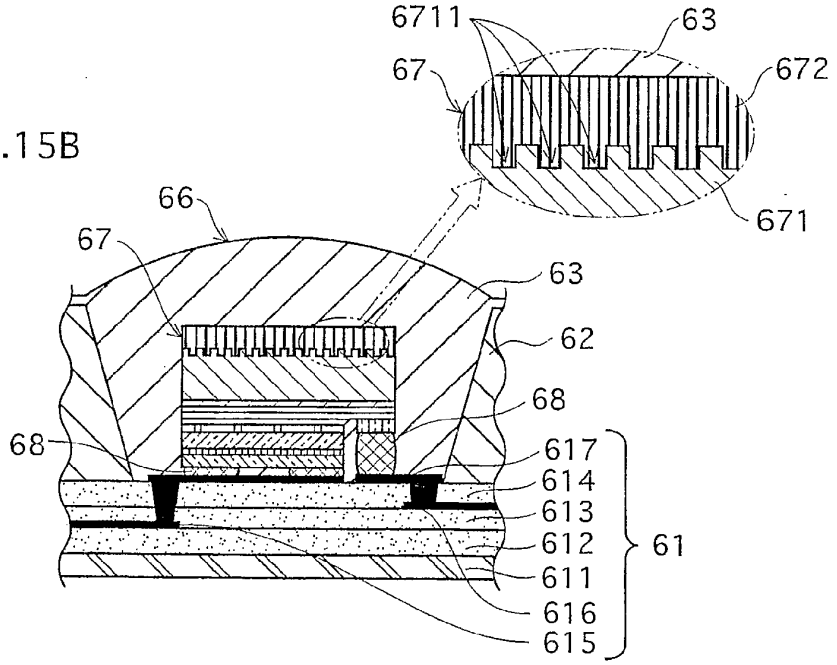


FIG.15B



BNSDOCID: <WO 2005008791A2_I_>

FIG.16A

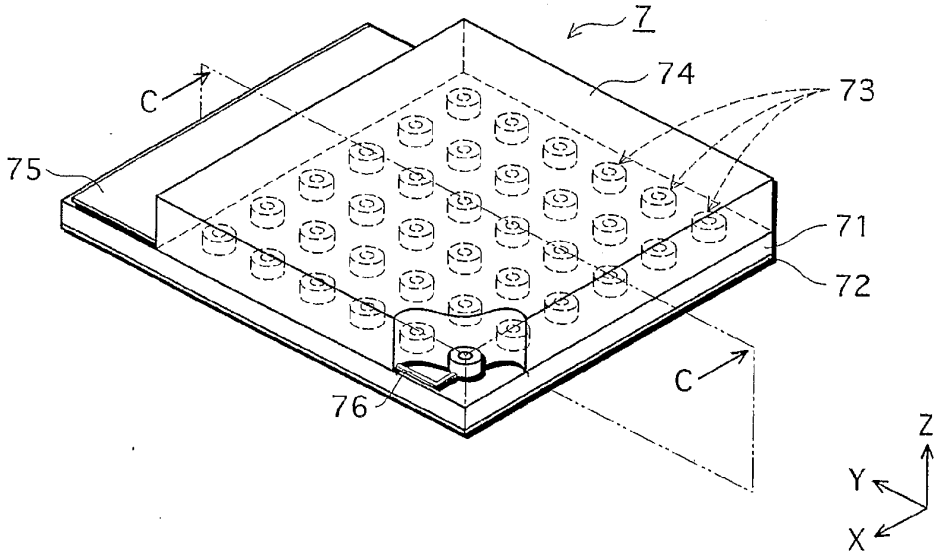
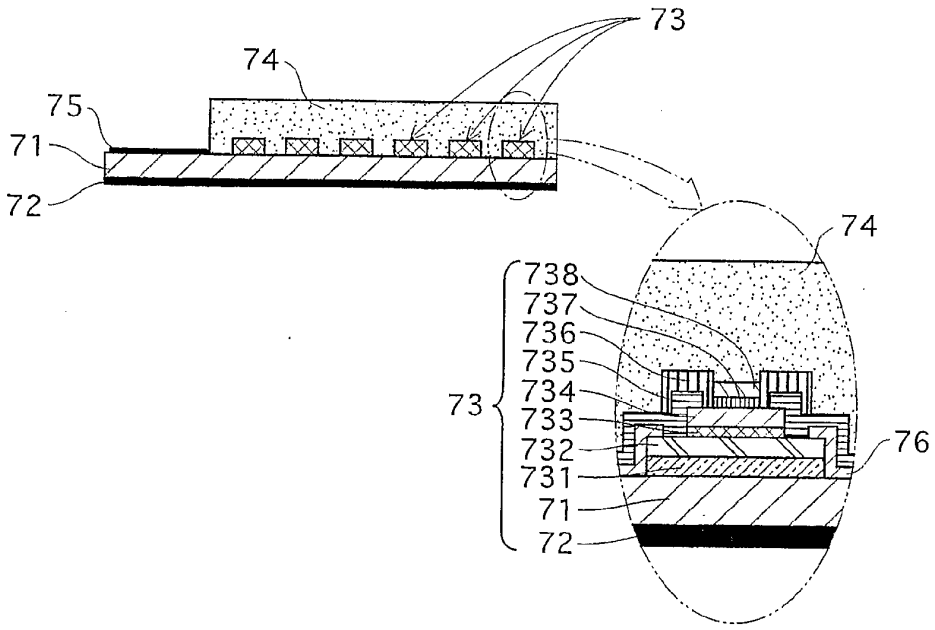


FIG.16B



ISDOCID: <WO_____2005008791A2_I_>

FIG.17A

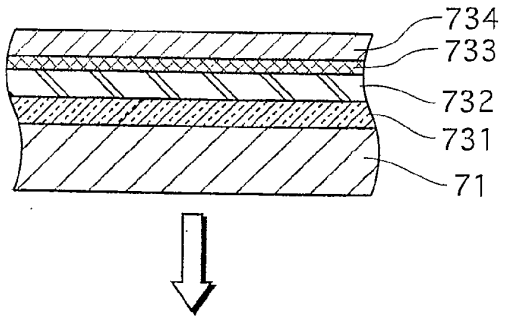


FIG.17B

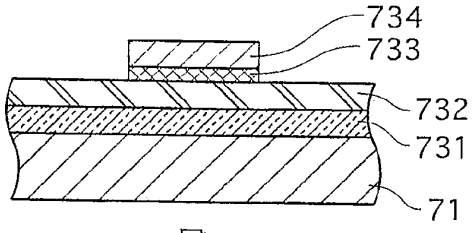


FIG.17C

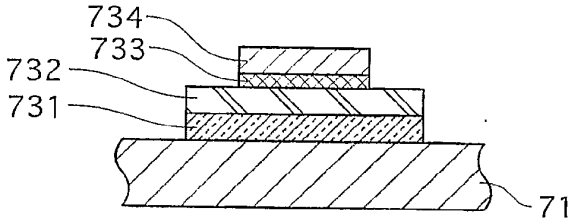
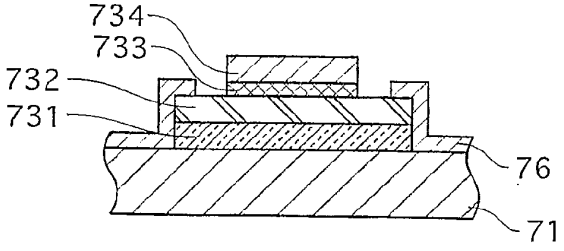


FIG.17D



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FIG.18E

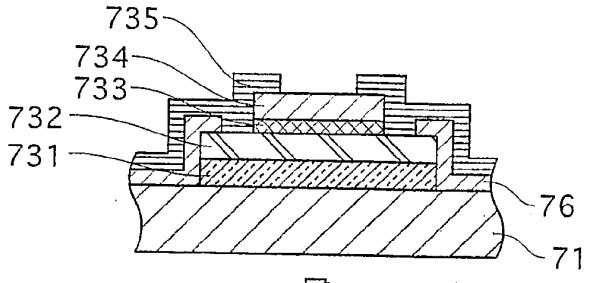


FIG.18F

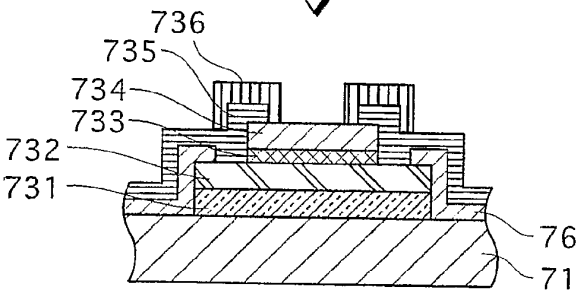


FIG.18G

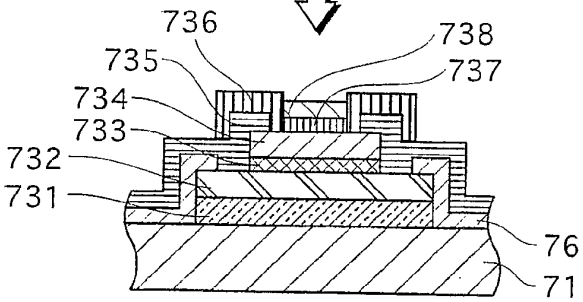
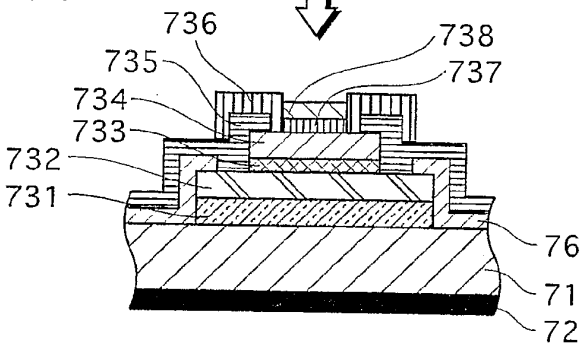
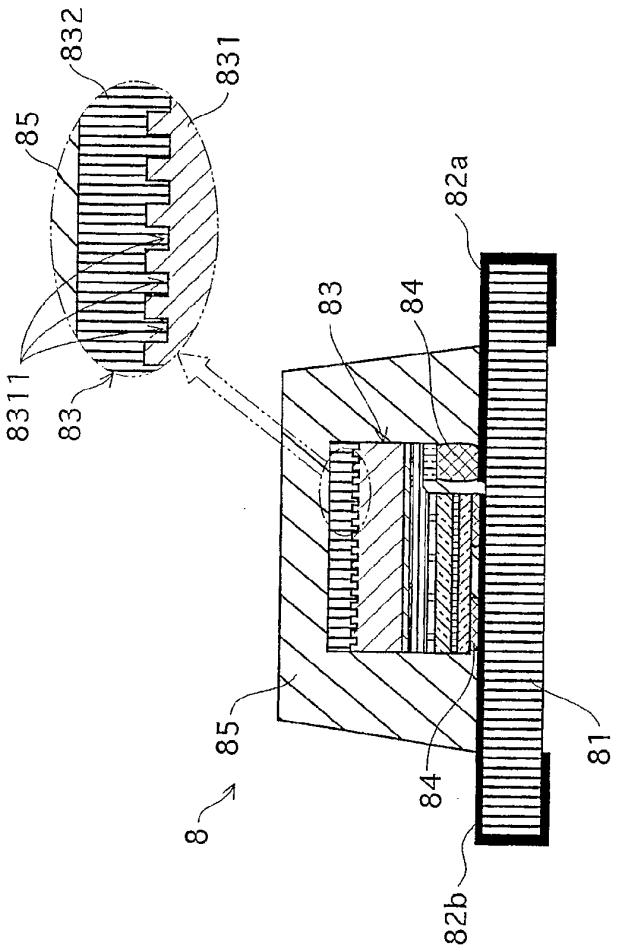


FIG.18H



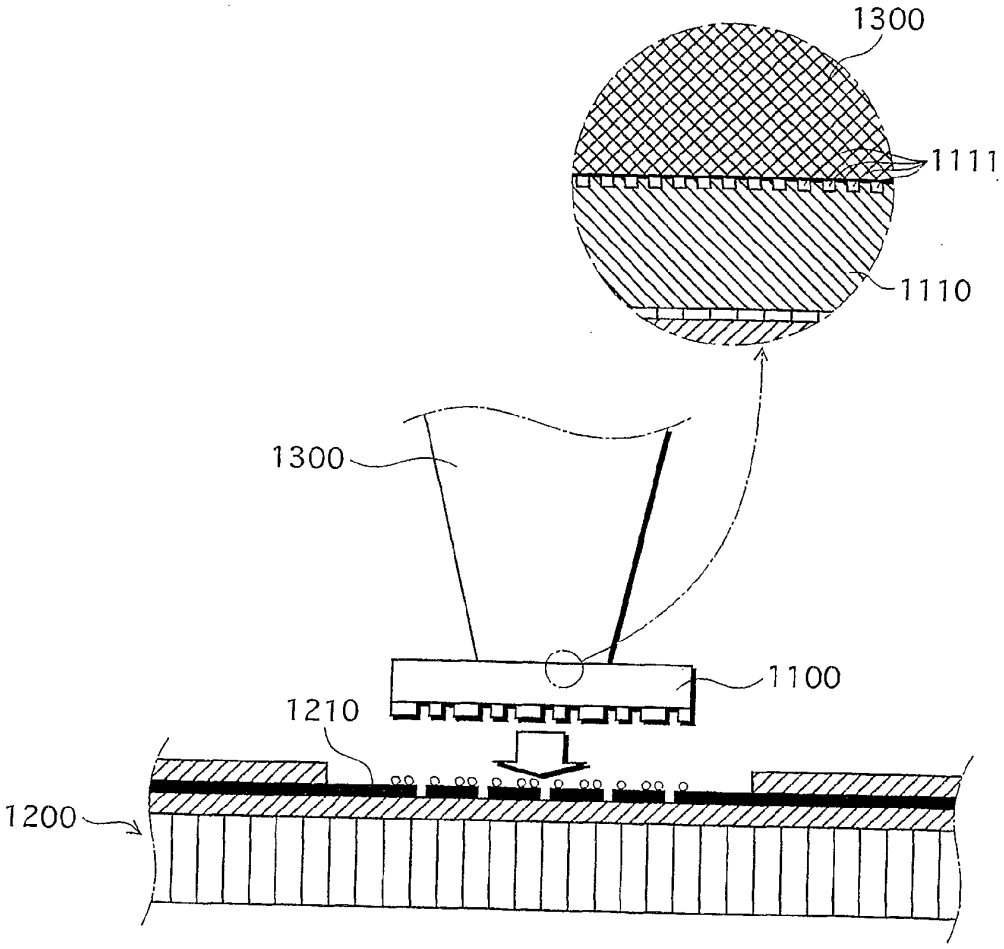
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FIG.19



BNSDOCID: <WO_____2005008791A2_I_>

FIG.20



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(71) Applicant *(for all designated States except US)*: MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. [JP/JP]; 1006, Oazakadoma, Kadoma-shi, Osaka 5718501 (JP).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: NAGAI, Hideo.

(74) Agent: NAKAJIMA, Shiro; 6F, Yodogawa 5-Bankan, 2-1 Toyosaki 3-chome, Kita-ku, Osaka-shi, Osaka 5310072 (JP).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

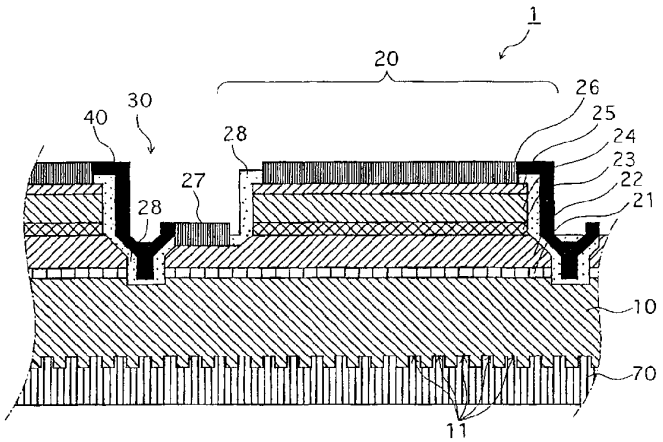
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
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— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report:
12 May 2005

[Continued on next page]

(54) Title: SEMICONDUCTOR LIGHT EMITTING DEVICE, METHOD OF MANUFACTURING THE SAME, AND LIGHTING APPARATUS AND DISPLAY APPARATUS USING THE SAME



(57) Abstract: The present invention aims to provide a semiconductor light emitting device (1) that may be firmly attached to a substrate with maintaining excellent light emitting efficiency, and a manufacturing method of the same, and a lighting apparatus and a display apparatus using the same. In order to achieve the above object, the semiconductor light emitting device (1) according to the present invention includes a luminous layer (23), a light transmission layer (10) disposed over a main surface of the luminous layer(23), and having depressions (11) on a surface facing away from the luminous layer (23), and a transmission membrane (70) disposed on the light transmission layer (10) so as to follow contours of the depressions, and light from the luminous layer (23) is irradiated so as to pass through the light transmission layer (10) and the transmission membrane (70).

WO 2005/008791 A3

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

PCT/JP2004/010244

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L33/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2001/010449 A1 (CHIU CHIEN-CHIA ET AL) 2 August 2001 (2001-08-02)	1,2,5-7, 11, 13-19, 21,22, 24,25,29
Y	paragraph '0040! - paragraph '0048!; figures 6,7	9,10,12, 20,23, 26-28,30
A		3,4,8
X	US 6 410 348 B1 (CHEN TZER-PERNG ET AL) 25 June 2002 (2002-06-25)	1-4,11, 14-19, 21,22,24
Y		8-10,20, 23,27,28
A	column 3, line 19 - column 4, line 65; figures 3-6	5-7,12, 13,25, 26,29,30

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 February 2005	07/03/2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Krause, J

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BNSDOCID: <WO_____ 2005008791A3_I_>

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 5 162 878 A (SASAGAWA ET AL) 10 November 1992 (1992-11-10) column 4, line 61 - column 8, line 48; figures 4-7	1,2, 14-17,24 3-13, 18-23, 25-30
X A	EP 0 404 565 A (MITSUBISHI KASEI POLYTEC CO; MITSUBISHI KASEI CORP; MITSUBISHI KASEI C) 27 December 1990 (1990-12-27) page 3, line 16 - line 54; figure 1	1,2,14, 24 3-13, 15-23, 25-30
X A	US 6 495 862 B1 (OKAZAKI HARUHIKO ET AL) 17 December 2002 (2002-12-17) column 4, line 1 - column 8, line 49; figures 1-3,6	1,14,24 2-13, 15-23, 25-30
Y A	EP 0 361 602 A (PHILIPS ELECTRONICS UK LIMITED; N.V. PHILIPS' GLOEILAMPENFABRIEKEN; PH) 4 April 1990 (1990-04-04) column 3, line 25 - line 49; figure 1	8 1,24
Y	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 06, 22 September 2000 (2000-09-22) -& JP 2000 077713 A (SANYO ELECTRIC CO LTD; TOTTORI SANYO ELECTRIC CO LTD), 14 March 2000 (2000-03-14) abstract	12,30
Y A	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 23, 10 February 2001 (2001-02-10) -& JP 2001 177158 A (MATSUSHITA ELECTRONICS INDUSTRY CORP), 29 June 2001 (2001-06-29) abstract	26 1,2,5-7, 14,18, 19,21, 22,25

ISDOCID: <WO_____2005008791A3_I_>

INTERNATIONAL SEARCH REPORT

Information on patent family members

PCT/JP2004/010244

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2001010449 A1	02-08-2001	TW 465123 B	21-11-2001
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JP 2000077713 A	14-03-2000	NONE	
JP 2001177158 A	29-06-2001	NONE	

BNSDOCID: <WO_____2005008791A3_I_>

Electronic Acknowledgement Receipt	
EFS ID:	7121810
Application Number:	12613275
International Application Number:	
Confirmation Number:	5984
Title of Invention:	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jong Lam LEE
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317USD1
Receipt Date:	02-MAR-2010
Filing Date:	05-NOV-2009
Time Stamp:	15:20:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	2010-03-02_P2317USD1_IDS.pdf	33425 35153d70a55ac7c7511b0f049dc7ed04226 78f3b	no	4
Warnings:					
Information:					

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2	Foreign Reference	2010-03-01_P2317US_IDSRefEP1469529.pdf	474700 409bca7e4a01fed115c271c8deaa21a5e1da3ede	no	14
Warnings:					
Information:					
3	NPL Documents	2010-03-01_P2317US_IDSRefEPSearchReport.pdf	365255 a0ade83f77732a7bbc171880c1bf5f94d6d95e17	no	9
Warnings:					
Information:					
4	Foreign Reference	2010-03-01_P2317US_IDSRefJP2004006582.pdf	831282 97c084267aaa94e0a826a3bfe4377bc4ed4cdff9	no	17
Warnings:					
Information:					
5	Foreign Reference	2010-03-01_P2317US_IDSRefWO2005008791.pdf	3289914 93de5f4bb95cb120f6d69c0ccafb056db9474b1b	no	82
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			Total Files Size (in bytes):	4994576	

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(**Not for submission under 37 CFR 1.99)**

Application Number	12613275
Filing Date	2009-11-05
First Named Inventor	Jong Lam LEE
Art Unit	2818
Examiner Name	NGUYEN, Thinh T
Attorney Docket Number	P2317USD1

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12613275
	Filing Date	2009-11-05
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, Thinh T
	Attorney Docket Number	P2317USD1

	1	Final Office Action dated June 29, 2010 in U.S. Patent Application No. 11/993,965	☐

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	12613275
	Filing Date	2009-11-05
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, Thinh T
	Attorney Docket Number	P2317USD1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2010-06-30
Name/Print	Hae-Chan Park	Registration Number	50114

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	7928474
Application Number:	12613275
International Application Number:	
Confirmation Number:	5984
Title of Invention:	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jong Lam LEE
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317USD1
Receipt Date:	30-JUN-2010
Filing Date:	05-NOV-2009
Time Stamp:	16:24:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	2010-06-30_P2317USD1_IDS.pdf	32041 0e106759c4b1442ffc6812182c04c2a184c612ff	no	4
Warnings:					
Information:					

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2	NPL Documents	2010-06-29_P2317US00_FinalOfficeAction.pdf	717765 958157f8ccbe84c1dd5ad79c1c26e12684b6c4b7	no	20
Warnings:					
Information:					
			Total Files Size (in bytes):	749806	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
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New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/613,275	11/05/2009	Jong Lam LEE	P2317USD1	5984

58027 7590 09/30/2010

H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

EXAMINER	
NGUYEN, THINH T	
ART UNIT	**PAPER NUMBER**
2818	

NOTIFICATION DATE	DELIVERY MODE
09/30/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATENT@PARK-LAW.COM

Office Action Summary	Application No.	Applicant(s)	
	12/613,275	LEE ET AL.	
	Examiner	Art Unit	
	THINH T. NGUYEN	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *1* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-10* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/ Restriction

1. Claims 1-10 are pending in this application.

2 Claims 1-21 are restricted as follows:

The claims are directed to the following patently distinct species of the claimed invention:

I/ Species I: Embodiment I. Species of Fig 4 and 5

II/Species II: Embodiment II. Species of Fig 6 through Fig 9

III/Species III: Embodiment III. Species of Fig 10 through Fig 13

IV/Species IV: Embodiment IV. Species of Fig 14 through Fig 17

V/Species V: Embodiment V. Species of Fig 19 through Fig 23

VI/Species VI: Embodiment VI. Species of Fig 24 through Fig 28

VII/Species VII: Embodiment VII. Species of Fig 29

VIII/Species VIII: Embodiment VIII. Species of Fig 32

This application contains claims directed to the patentably distinct species **as set forth above.** The species are independent or distinct because claims to the different species recite the mutually exclusive characteristics of such species. In addition, these species are not obvious variants of each other based on the current record. Currently claim 1 is generic

Applicant is required under 35 U.S.C. 121 and 35 U.S.C. 372 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable.

There is an examination and search burden for these patentably distinct species due to their mutually exclusive characteristics. The species require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search queries); and/or the prior art applicable to one species would not likely be applicable to another species; and/or the species are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species to be examined even though the requirement may be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected species, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

The election of the species may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the election of species requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected species.

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the species unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other species.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141.

3. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a diligently filed petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(h).

CONCLUSION

4 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on 9.30 AM 6.30 PM Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Loke can be

reached on (571) 272-1657. The fax phone numbers for the organization where this application or proceeding is assigned are 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thinh T Nguyen/

Patent Examiner
Art Unit 2818

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12613275	LEE ET AL.
	Examiner	**Art Unit**
	THINH T NGUYEN	2818

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/25/2010								
	1	÷								
	2	÷								
	3	÷								
	4	÷								
	5	÷								
	6	÷								
	7	÷								
	8	÷								
	9	÷								
	10	÷								

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Docket No.: P2317USD1

Jong Lam LEE, *et. al.*

Serial No.: 12/613,275 Group Art Unit: 2818

Confirmation No.: 5984

Filed: November 5, 2009 Examiner: NGUYEN, THINH T.

For: **LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO ELECTION/RESTRICTION REQUIREMENT

Sir:

In reply to the September 30, 2010 Restriction Requirement, Applicants elect Embodiment IV, Species of Figures 14-17, including claims 1-2 and 5-10, without traverse.

It is not believed that any extensions of time or fees are required. If extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned for under 37 C.F.R. §1.136(a) and associated fees may be charged to our Deposit Account No. 50-3698.

Respectfully submitted,

/hae-chan park/

Hae-Chan Park
Reg. No. 50,114

Dated: October 22, 2010

CUSTOMER NO.: 58027
H.C. Park & Associates, PLC

Electronic Acknowledgement Receipt

EFS ID:	8680455
Application Number:	12613275
International Application Number:	
Confirmation Number:	5984
Title of Invention:	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jong Lam LEE
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317USD1
Receipt Date:	22-OCT-2010
Filing Date:	05-NOV-2009
Time Stamp:	12:45:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	P2317USD1_Response_to_Election_Restriction.pdf	68599 c0532dccf201451bcf04603ebe7f78ecfb91bbcd	no	1
Warnings:					
Information:					

Total Files Size (in bytes):	68599

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)		
	Application Number	12613275
	Filing Date	2009-11-05
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317USD1

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12613275
	Filing Date	2009-11-05
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317USD1

	1	Non-Final Office Action of U.S Patent Application No. 12/630,370 issued on December 09, 2010.	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12613275
	Filing Date	2009-11-05
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317USD1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2010-12-09
Name/Print	Hae-Chan Park	Registration Number	50114

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	9000592
Application Number:	12613275
International Application Number:	
Confirmation Number:	5984
Title of Invention:	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jong Lam LEE
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317USD1
Receipt Date:	09-DEC-2010
Filing Date:	05-NOV-2009
Time Stamp:	14:30:56
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	P2317USD1_IDS.pdf	990515 28d626f7a53c18edb01cad9e4228ca76aea305c8	no	4

Warnings:
Information:

A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.

2	NPL Documents	P2317USC2_OA12_09_2010.pdf	887882 717a749d7f571468bf359d2ff607644598a68527	no	26

Warnings:

Information:

Total Files Size (in bytes):	1878397

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/613,275	11/05/2009	Jong Lam LEE	P2317USD1	5984

58027 7590 12/23/2010

H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

EXAMINER	
NGUYEN, THINH T	
ART UNIT	**PAPER NUMBER**
2818	

NOTIFICATION DATE	DELIVERY MODE
12/23/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATENT@PARK-LAW.COM

Office Action Summary	Application No.	Applicant(s)	
	12/613,275	LEE ET AL.	
	Examiner	Art Unit	
	THINH T. NGUYEN	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) *3 and 4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-7,9 and 10* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :11/05/09,01/27/10,02/24/10, 03/02/10,06/30/10,12/09/10,.

DETAILED OFFICE ACTION

1. Applicant's election of claims 1-2.5-10 pertains to Species IV for prosecution without traverse in the communication with the Office on October 22nd 2010 is acknowledged.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 9 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 is indefinite because of recitation of the unclear limitation:

-- at a temperature of 100 to 140;E' ; --

Note that the temperature has different unit system express in Fahrenheit degree or Celsius centigrade degree or absolute degree and there are no degree system specifies in claim 9, moreover, it is unclear what Applicant means by :; E'; ????

Claim Rejections - 35 USC § 103

4. The following is a quotation of U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5 Claim 1-2, 5-7, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang (U.S. Patent 7,213,942) thereafter Jang 942 in view of Salam (US patent Application Publication US 2005/0023537) thereafter Salam 537 or Dawson (US patent 7,598,149) thereafter Dawson 149 or Akimoto et al.(US patent 7,057,208) thereafter Akimoto (US patent 7,057,208)

With regard to claim 1, Jang 942 (the abstract, fig 1 to fig 4) discloses all the invention of a method of manufacturing a light emitting device, comprising the steps of: sequentially forming N-type and P-type semiconductor layers on a substrate (column 2 lines 35-50) ; forming an etching mask pattern (column 2 lines 25-40) on the P-type semiconductor layer; and removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern. (implicitly disclosed by the structure of fig 3 and fig 4 of the Jiang 942 disclosure)

Not specific in Jang 942 is the limitation wherein the mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane,

Salam 537, however, discloses a method for fabricating an LED array wherein

the side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane,(fig 3-22, paragraph [0063],paragraph [[0063])

It would have been obvious to one of ordinary skill in the art the time the invention was made to incorporate the above features as taught by Salam 537 into the method disclosed by Jiang 942 and come up with the invention of claim 1.

A person skilled in the art at the time the invention was made would have been motivate to incorporate all the advantages, taught by Salam 537 (paragraph [0008] to [0017] in order to improve the Jiang 942 method and make it a commercial success.

Moreover, note that the features wherein the side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane are well known in the art at the time the inventions was made as evident by the disclosures by Dawson 149 (the abstract, ,fig 1(a)(b) (c) (d),fig 3, fig 6) or Akimoto 208 (fig 2B, 2C). a person skilled in the art would have been motivated to use the relevant teachings by Dawson 149 or Akimoto 208 to modify the method or adapt the method disclosed by Jiang 942 in order to achieve the required sloped arrays of LED disclosed by Jiang 942.

With regard to claim 2, Jiang 942 discloses a method further comprising the steps of: removing a portion of the N-type semiconductor layer exposed through the removal of the P-type semiconductor layer to form a plurality of light emitting cells;

And connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire (implicitly disclosed by fig 3 and fig 4 of Jiang 942 , N-layer #20, P-layer # 24, wire #36, fig 3, column 4 lines 25-55) .

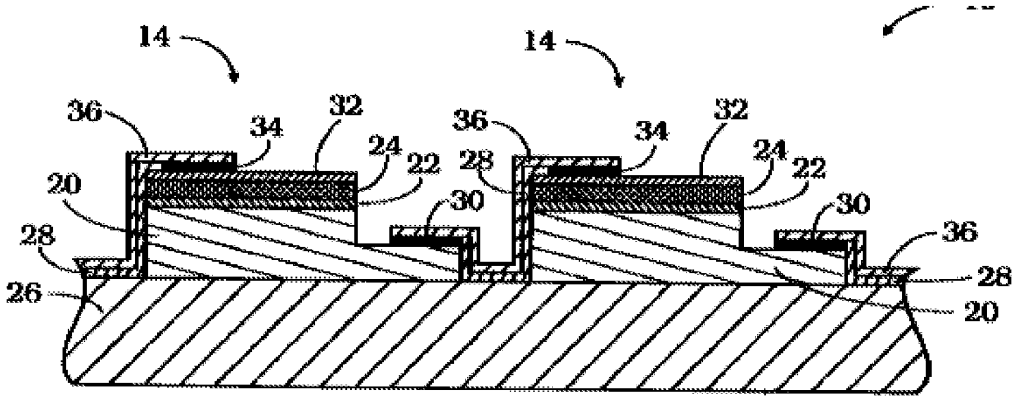


Fig. 3

JIANG 942 DISCLOSURES

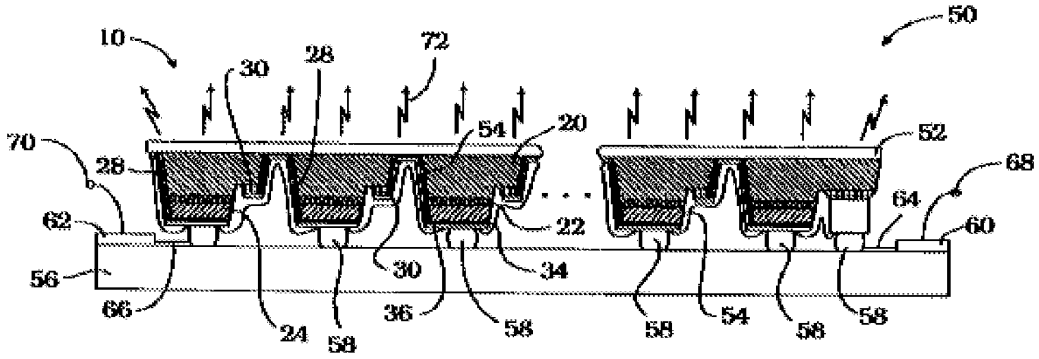


Fig. 4

JIANG 942 DISCLOSURES.

With regard to claim 5, the combined Jiang 942 in view of Salam 537 disclosures disclosed a method wherein the step of forming the plurality of light emitting cells comprises the steps of: forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; removing the N-type and P-type semiconductor layers exposed through the etching mask pattern to form a plurality of light emitting cells; and removing the etching mask pattern. (Jiang 942 fig 3, fig 4, Salam 537 fig 7 through fig 22)

With regard to claim 6, Jiang 942 discloses a method, wherein the N type semiconductor layer of one light emitting cell and the P type semiconductor layer of another adjacent light emitting cell are connected with the conductive wire through a bridge or step coverage process. (implicitly disclosed by fig 3 and fig 4 of Jiang 942, N-layer #20, P-layer # 24, wire #36, fig 3, column 4 lines 25-55) .

With regard to claim 7, as set forth in the rejection of claim 1. , the combined Jiang 942 in view of Salam 537 disclosures all the invention except for the limitation wherein a photoresist with a thickness of 3 to 50 .micron is used in the step of forming the etching mask pattern.

This limitation, however, is considered obvious for the following rationale:

The selection of parameters such as **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.,** would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.,** or in combination of the parameters would

be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ... such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA **1935);** In re Dreyfus 24 USPQ 52 (CCPA **1934).**

With regard to claim 10, as set forth in the rejection of claim 1, the combined Jiang 942 in view of Salam 537 disclosures discloses all the invention except for the specific wherein the method further comprising the steps of: after the step of removing the P-type semiconductor layer and the etching mask pattern, removing a rear surface of the substrate at a certain thickness; And depositing Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof onto the rear surface of the substrate.

The Examiner, however, takes official notice that these features are well known by a person skilled in the art at the time the invention was made because these step will provide the light emitting arrays disclosed by Jiang 942 in view of Salam 537 to increase the light emission efficiency in the required direction. , furthermore, note that both Jiang 942 and Salam 537 discloses a metallic reflecting surface provide to the substrate

(Salam 537 fig 6, element 80, paragraph [0064], Jiang 942 (column 5 lines 1-22, claim 67)

ALLOWABLE SUBJECT MATTER

6. Claim 8 is objected as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claim. Claim 8 is considered allowable since the prior fails to teach the additional limitation and step as recited in claim 8.

7. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

9. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d) which papers have been placed of record in the file.

CONCLUSION

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on Monday-Friday 9:30am-6: 30pm.If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached at 571-272-1657.The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thinh T. Nguyen/

Primary Examiner
Art Unit 2818

Notice of References Cited	Application/Control No. 12/613,275	Applicant(s)/Patent Under Reexamination LEE ET AL.	
	Examiner THINH T. NGUYEN	Art Unit 2818	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,213,942	05-2007	Jiang et al.	362/231
*	B	US-2005/0023537	02-2005	Salam, Hassan P. A.	257/079
*	C	US-7,598,149	10-2009	Dawson et al.	438/343
*	D	US-7,057,208	06-2006	Akimoto et al.	257/59
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
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*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
12613275	12613275	LEE ET AL.
	Examiner	Art Unit
	THINH T NGUYEN	2818

SEARCHED			
Class	Subclass	Date	Examiner
438	28,29,26	12/15/10	TTN

SEARCH NOTES		
Search Notes	Date	Examiner
east	12/10/10	TTN

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
*12613275	12613275	LEE ET AL.
5*	Examiner	Art Unit
	THINH T NGUYEN	2818

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/25/2010	12/15/2010							
	1	÷	✓							
	2	÷	✓							
	3	÷	N							
	4	÷	N							
	5	÷	✓							
	6	÷	✓							
	7	÷	✓							
	8	÷	O							
	9	÷	✓							
	10	÷	✓							

EAST Search History

EAST Search History (Prior Art)

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L2	179803	LEE.inv. near3 Jong. inv. near3 Lam.inv. LEE.inv. near3 Jae Ho. inv. YOON.inv. near3 Yeo.inv. Jin.inv. HWANG.inv. near3 Eu. inv. near3 Jin.inv. KIM. inv. near3 Dae.inv. near3 Won.inv.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/15 07:52
L3	666	LEE.inv. near3 Jong. inv. near3 Lam.inv. LEE.inv. near3 Jae.inv. near3 Ho.inv. YOON. inv. near3 Yeo.inv. near3 Jin.inv. HWANG. inv. near3 Eu.inv. near3 Jin.inv. KIM.inv. near3 Dae.inv. near3 Won.inv.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/15 07:52
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L5	205	3 and 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/15 08:20
L6	3214241	method.clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/15 08:20
L7	93	5 and 6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/15 08:20

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L9	5	"7535028"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/15 08:29
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L11	12	AC.as. near3 LED.as. near3 lighting.as.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/15 08:38
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EAST Search History

EAST Search History (Prior Art)

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L3	35587	hard near mask	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/15 23:03
L4	28708	hard near3 mask same (etch$4 etching)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/15 23:04
L5	399311	light near3 emitting near3 (device diode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/15 23:06
L6	1137	lumileds.as.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/15 23:07
L7	531	seoul.as. near3 opto. as.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/15 23:07
L8	2	4 and 6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/15 23:08

L9	5	4 and 7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/15 23:08
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L11	63	5 and 10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/15 23:11
L12	268	4 same slope	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/15 23:27
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L5	399311	light near3 emitting near3 (device diode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/15 23:06
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L9	5	4 and 7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/15 23:08
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L4	1137	Lumileds.as.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/16 10:39
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L7	45828	LED with arrays	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/16 10:43
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L10	84	8 and etch$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/16 10:43
L11	1050	sloped with (trench grove)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/16 10:45
L12	58148	LED same array	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/16 10:46
L13	15559	(sloped slop$4 angle) same (trench grove)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/16 10:47
L14	182	12 and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/12/16 10:47
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Doc description: Information Disclosure Statement (IDS) Filed

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(**Not for submission under 37 CFR 1.99)**

Application Number	12613275
Filing Date	2009-11-05
First Named Inventor	Jong Lam Lee
Art Unit	2818
Examiner Name	To be determined
Attorney Docket Number	P2317USD1

U.S.PATENTS

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	1	2004-071644	JP		2004-03-04	NICHIA CHEM IND LTD		☐
	2	2004-273746	JP		2004-09-30	HITACHI CABLE LTD		☐
	3	2005-136130	JP		2005-05-26	KYOCERA CORP		☐

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /T.N./

Receipt date: 01/27/2010	Application Number	12613275 12613275 - GAU: 2818
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2009-11-05
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	To be determined
	Attorney Docket Number	P2317USD1

	4	2001-156331	JP		2001-06-08	NICHIA CHEM IND LTD		☐

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NON-PATENT LITERATURE DOCUMENTS

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EXAMINER SIGNATURE

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	12613275
	Filing Date	2009-11-05
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	
	Attorney Docket Number	P2317USD1

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	1	7535028		2009-05-19	Fan et al.	
	2	7504772		2009-03-17	Yukimoto et al.	
	3	5940683		1999-08-17	Holm et al.	
	4	6608330		2003-08-19	Yamada	
	5	5652434		1997-07-29	Nakamura et al.	
	6	5862167		1999-01-19	Sassa et al.	
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Receipt date: 02/24/2010	Application Number	12613275 12613275 - GAU: 2818
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2009-11-05
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	
	Attorney Docket Number	P2317USD1

	1	20030010989		2003-01-16	Yukimoto	
	2	20020109147		2002-08-15	Shirai et al.	
	3	20070114542		2007-05-24	Yamazaki et al.	
	4	20050121679		2005-06-09	Nagahama et al.	
	5	20050082966		2005-04-21	Yamazaki et al.	
	6	20050254243		2005-11-17	Jiang et al.	
	7	20100006870		2010-01-14	Lee et al.	

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	1	2004-311677	JP		2004-11-04	Matsushita Electric Works Ltd.		☐
	2	2005-142278	JP		2005-06-02	Sharp Corp.		☐

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Receipt date: 02/24/2010	Application Number	12613275 12613275 - GAU: 2818
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2009-11-05
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	
	Attorney Docket Number	P2317USD1

	3	2005-117020	JP		2005-04-28	Stanley Electric Co., Ltd.		☐
	4	2003-017740	JP		2003-01-17	Lumileds Lighting US LLC		☐
	5	2001-185755	JP		2001-07-06	Rohm Co., Ltd.		☐
	6	07-153993	JP		1995-06-16	Daido Steel Co., Ltd.		☐
	7	06-244458	JP		1994-09-02	Nichia Chem Ind Ltd.		☐

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	1	Office Action dated February 1, 2010 for co-pending application no. 12/568,630.	☐
	2	Office Action dated February 5, 2010 for co-pending application no. 11/993,965.	☐

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Receipt date: 02/24/2010	Application Number	12613275 12613275 - GAU: 2818
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)	Filing Date	2009-11-05
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	
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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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	Application Number	12613275
	Filing Date	2009-11-05
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	To be assigned
	Attorney Docket Number	P2317USD1

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	1	5252434		1993-10-12	Blonder	

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	1	20050023537		2005-02-03	Salam	

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	1	2005008791	WO		2005-01-27	Matsushita Electric Industrial Co., Ltd.		☐
	2	1469529	EP		2004-10-20	Lumileds Lighting US, LLC		☐
	3	2004006582	JP		2004-01-08	Nitride Semiconductor Co Ltd		☐

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	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	To be assigned
	Attorney Docket Number	P2317USD1

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	1	European Search Report issued February 10, 2010 by the European Patent Office in European Patent Application No. 06769008.1	☐

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	Application Number	12613275
	Filing Date	2009-11-05
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, Thinh T
	Attorney Docket Number	P2317USD1

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Receipt date: 06/30/2010	Application Number	12613275 12613275 - GAU: 2818
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2009-11-05
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, Thinh T
	Attorney Docket Number	P2317USD1

	1	Final Office Action dated June 29, 2010 in U.S. Patent Application No. 11/993,965	☐

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	Filing Date	2009-11-05
	First Named Inventor	Jong Lam LEE
	Art Unit	
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	1	6255129		2001-07-03	Lin	
	2	7474681		2009-01-06	Lin, et al.	
	3	7271421		2007-09-18	Yukimoto, et al.	
	4	7034340		2006-04-25	Yukimoto	
	5	7525248		2009-04-28	Fan	
	6	6635902		2003-10-21	Lin	
	7	7511311		2009-03-31	Kususe, et al.	
	8	7213942		2007-05-08	Jiang, et al.	

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Receipt date: 11/05/2009	Application Number	12613275 - GAU: 2818
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	First Named Inventor	Jong Lam LEE
	Art Unit	
	Examiner Name	
	Attorney Docket Number	P2317USD1

	9	7221044		2007-05-22	Fan, et al.	
	10	7210819		2007-05-01	Jiang, et al.	
	11	6957899		2005-10-25	Jiang, et al.	
	12	6472718		2002-10-29	Lell	
	13	6547249		2003-04-15	Collins, et al.	

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	1	20040075399		2004-04-22	David HALL	
	2	20040012958		2004-01-22	Hashimoto, et al.	
	3	20050199885		2005-09-15	Hata, et al.	
	4	20060169993		2006-08-03	Fan, et al.	

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Receipt date: 11/05/2009	Application Number	12613275 - GAU: 2818
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	First Named Inventor	Jong Lam LEE
	Art Unit	
	Examiner Name	
	Attorney Docket Number	P2317USD1

	5	20050225973		2005-10-13	Eliashevich, et al.	
	6	20080230765		2008-09-25	Yoon, et al.	
	7	20060043433		2003-03-02	Matsushita	
	8	20050224973		2005-10-13	Bernier, et al.	
	9	20060044864		2006-03-02	Lin, et al.	

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	1	04-023568	WO		2004-03-18	Nitride Semiconductors Co., Ltd.		☐
	2	04-013916	WO		2004-02-12	Nichia Corporation		☐
	3	10-2006-0037589	KR		2006-05-03	Seoul Semiconductor Co., Ltd.		☐
	4	2002-026378	JP		2002-01-25	Kyocera Corp.		☐

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Receipt date: 11/05/2009	Application Number	12613275 - GAU: 2818
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	First Named Inventor	Jong Lam LEE
	Art Unit	
	Examiner Name	
	Attorney Docket Number	P2317USD1

	5	10-2005-0066358	KR		2005-06-30	Samsung Electro-Mechanics Co., Ltd.		☐
	6	2004-079867	JP		2004-03-11	Shiro SAKAI Nitride Semiconductor Co., Ltd.		☐
	7	10-2003-0022940	KR		2003-03-19	Epivalley Co., Ltd.		☐
	8	10-2005-0052474	KR		2005-06-02	Shiro SAKAI et al.		☐
	9	10-2003-0052499	KR		2003-06-27	Bae		☐
	10	10-2004-0005098	KR		2004-01-16	Kang		☐
	11	11-150303	JP		1999-06-02	Takeuchi		☐

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Application Number	12613275
Filing Date	2009-11-05
First Named Inventor	Jong Lam LEE
Art Unit	2818
Examiner Name	NGUYEN, THINH T.
Attorney Docket Number	P2317USD1

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Receipt date: 12/09/2010	Application Number	12613275 12613275 - GAU: 2818
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2009-11-05
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317USD1

	1	Non-Final Office Action of U.S Patent Application No. 12/630,370 issued on December 09, 2010.	☐

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	Docket No.: P2317USD1
Jong Lam LEE, *et al.*	
Serial No.: 12/613,275	Group Art Unit: 2818
Confirmation No.: 5984	
Filed: November 5, 2009	Examiner: NGUYEN, THINH T.

For: **LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME**

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY UNDER 37 C.F.R. § 1.111

Sir:

In response to the Non-Final Office Action dated December 23, 2010 ("Office Action"), Applicants respectfully request reconsideration of the application in view of the following Amendments and Remarks.

Amendments to the Specification begin on page 2.

Amendments to the Claims begin on page 4.

Remarks begin on page 9.

No extensions of time are required at this time. If extensions of time are necessary to prevent abandonment of this application, then they are petitioned for under 37 C.F.R. § 1.136(a). No fees for net addition of claims are required at this time. Any fees required for [further] extensions of time or for the net addition of claims may be charged to our Deposit Account No. 50-3698.

AMENDMENTS TO THE SPECIFICATION

In the Specification:

Please replace paragraph [0071] with the following amended paragraph:

[0071] Referring to FIG. 10, portions of an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40, which are sequentially formed on a substrate 10, are removed to form a plurality of light emitting cells. To this end, after a photoresist has been applied at a thickness of 3 to 50 μm on the P-type semiconductor layer 40 and light-exposed, it is immediately developed without hard-baking such that an etching mask pattern can be formed. The portions of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor pattern 20, which are exposed through the etching mask pattern with a slope of the side surface, and the etching mask pattern is removed to separate the light emitting cells from one another. Accordingly, a light emitting device in which entire side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at a predetermined slope can be obtained as shown in this figure. Further, the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are removed using the etching mask pattern in which a photoresist is applied at a thickness of 3 to 50 μm on the P-type semiconductor layer 40 and light-exposed and hard-baked at a temperature of 100 to 140° and then developed. Accordingly, the entire side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 can be formed at various slopes of 80 to 20°.

Please replace paragraph [0076] with the following amended paragraph:

[0076] Further, even in a case where the plurality of light emitting cells are separated by etching such that the side surfaces may have various slopes as shown in FIG. 10 and then etched to expose the N-type semiconductor layer 20, a light emitting device can be manufactured using the same etching process as described above. That is, as shown in FIG. [[11]]13, the side surfaces of the P-type semiconductor layer 40 and the active layer 30, which are etched to expose the N-type semiconductor layer 20, can be formed at various slopes.

Please replace paragraph [0085] with the following amended paragraph:

[0085] The wire 80 may be formed using a plating technique. That is, after an etching mask pattern with an opening portion defining a region of the wire 80 has been formed on the [[is]] insulation layer 70 and a metal layer has been plated within the opening portion, the etching mask pattern is removed and thus the wire 80 can be formed.

Please replace paragraph [0089] with the following amended paragraph:

[0089] As described above, the light emitting device according to the present invention is formed such that the side surfaces of the P-type semiconductor layer, the active layer and a [[is]] portion of the N-type semiconductor layer are not perpendicular (90°) to but inclined at a predetermined slope from a horizontal plane. Therefore, luminous efficiency of the light emitting device of the present invention can be enhanced as compared with that of the conventional light emitting device. The reason is that a photon reflected on a flat surface in the prior art is not reflected on a surface with a different angle but emitted to the outside.

AMENDMENTS TO THE CLAIMS

Please **CANCEL** claims 8-9 without prejudice or disclaimer.

Please **AMEND** claims 1-2, 5, 7, and 10 as shown below.

Please **ADD** claims 11-17 as shown below.

This claim list replaces all prior claim lists in the application.

1. (Currently amended) A method of manufacturing a light emitting device, comprising ~~the steps of~~:

sequentially forming an N-type semiconductor layer, active layer, and P-type semiconductor ~~layers~~ layer on a substrate;

forming an etching mask pattern, of which a side surface is not perpendicular to but inclined at a ~~predetermined~~ slope from a horizontal plane, on the P-type semiconductor layer; and

removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern,

wherein forming the etching mask pattern comprises:

forming a photoresist on the P-type semiconductor layer;

exposing the photoresist to light; and

developing the light-exposed photoresist without a baking process after the light exposure.

2. (Currently amended) The method as claimed in claim 1, further comprising ~~the steps of~~:

removing a portion of the N-type semiconductor layer exposed through the removal of the P-type semiconductor layer to form a plurality of light emitting cells; and

connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire.

3. (Withdrawn) The method as claimed in claim 1, further comprising the step of flip-chip bonding the substrate onto an additional submount substrate after the step of removing the P-type semiconductor layer and the etching mask pattern.

4. (Withdrawn) The method as claimed in claim 3, further comprising the steps of:

removing a portion of the N-type semiconductor layer exposed due to the removal of the P-type semiconductor layer to form a plurality of light emitting cell; and

connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire, after the step of removing the P-type semiconductor layer and the etching mask pattern.

5. (Currently amended) The method as claimed in claim 2, wherein the ~~step of~~ forming the plurality of light emitting cells comprises ~~the steps of~~:

forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer;

removing the N-type and P-type semiconductor layers exposed through the etching mask pattern to form a plurality of light emitting cells; and

removing the etching mask pattern.

6. (Original) The method as claimed in claim 2, wherein the N type semiconductor layer of one light emitting cell and the P type semiconductor layer of another adjacent light emitting cell are connected with the conductive wire through a bridge or step coverage process.

7. (Currently amended) The method as claimed in claim 1, wherein [[a]]the photoresist with a thickness of 3 to 50 μm is used in the ~~step of~~ forming the etching mask pattern.

8-9. (Canceled)

10. (Currently amended) The method as claimed in claim 1, further comprising ~~the steps of~~:

after the ~~step of~~ removing the P-type semiconductor layer and the etching mask pattern, removing a rear surface of the substrate at a certain thickness; and

depositing Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof onto the rear surface of the substrate.

11. (New) A method of manufacturing a light emitting device, comprising:

sequentially forming an N-type semiconductor layer, active layer, and P-type semiconductor layer on a substrate;

forming an etching mask pattern, of which a side surface is not perpendicular to but inclined at a slope from a horizontal plane, on the P-type semiconductor layer; and

removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern,

wherein forming the etching mask pattern comprises:

forming a photoresist on the P-type semiconductor layer;

exposing the photoresist to light;

hard-baking and developing the photoresist; and

etching a side surface of the developed photoresist to have the slope from the horizontal plane.

12. (New) The method as claimed in claim 11, further comprising:

removing a portion of the N-type semiconductor layer exposed through the removal of the P-type semiconductor layer to form a plurality of light emitting cells; and

connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire.

13. (New) The method as claimed in claim 12, wherein the forming the plurality of light emitting cells comprises:

forming an etching mask pattern, of which a side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer;

removing the N-type and P-type semiconductor layers exposed through the etching mask pattern to form a plurality of light emitting cells; and

removing the etching mask pattern.

14. (New) The method as claimed in claim 12, wherein the N type semiconductor layer of one light emitting cell and the P type semiconductor layer of another adjacent light emitting cell are connected with the conductive wire through a bridge or step coverage process.

15. (New) The method as claimed in claim 11, wherein the photoresist with a thickness of 3 to 50 μm is used in the forming the etching mask pattern.

16. (New) The method as claimed in claim 11, further comprising:

after the removing the P-type semiconductor layer and the etching mask pattern, removing a rear surface of the substrate at a certain thickness; and

depositing Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof onto the rear surface of the substrate.

17. (New) The method as claimed in claim 11, wherein the hard-baking is performed at a temperature of 100 to 140 ℃.

REMARKS

Claims 1-2, 5, 7, and 10 have been amended, claims 8-9 have been canceled without prejudice or disclaimer, and claims 11-17 have been added. The specification has been amended to correct certain informalities. Accordingly, claims 1-7 and 10-17 are currently pending in the application, of which claims 1 and 11 are independent. Applicants appreciate the indication that claim 8 contains allowable subject matter.

Applicants respectfully submit that the above amendments and new claims do not add new matter to the application and are fully supported by the specification. Support for the amendments and added claim may be found at least in original claims 1-2, 5-7, and 9-10 and at paragraphs [0050-0051] of the original specification.

In view of the above amendments and the following Remarks, Applicants respectfully request reconsideration and timely withdrawal of the pending objections and rejections for the reasons discussed below.

Request for Rejoinder

Applicants respectfully request rejoinder of claims 3 and 4. Claims 3 and 4 were previously withdrawn, but they now depend from allowable claim 1. Thus, under MPEP § 821.04, Applicants respectfully request that the restriction requirement for claims 3 and 4 be withdrawn and that these claims be rejoined and fully examined for patentability under 37 C.F.R. § 1.104. Claims 3 and 4 are allowable at least because they depend from an allowed base claim.

Rejections Under 35 U.S.C. § 112, second paragraph

Claim 9 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. By this reply, claim 9 has been canceled, thereby rendering this rejection moot.

Rejections Under 35 U.S.C. § 103

Claims 1-2, 5-7 and 10 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over U.S. Patent No. 7,213,942 issued to Jiang, *et al.* ("Jiang") in view of U.S. Patent Application Publication No. 2005/0023537 applied for by Salam ("Salam") or U.S. Patent No. 7,598,149 issued to Dawson, *et al.* ("Dawson") or U.S. Patent No. 7,057,208 issued to Akimoto, *et al.* ("Akimoto"). Applicants respectfully traverse this rejection for at least the following reasons.

By this reply, the subject matter of claim 8, which has been indicated as allowable, is incorporated into independent claim 1. Applicants do not believe that intervening claim 7 is necessary for the allowance of amended claim 1. Therefore, claim 1 is in condition for allowance. Claims depending from claim 1 are also allowable at least for this reason. Accordingly, withdrawal of this 103(a) rejection is respectfully requested.

Added Claims

Added claims 11-17 are directed to additional features of the invention, which are not disclosed or suggested in the art of record.

Other Matters

In addition to the amendments mentioned above, claims 2, 5, 7, and 10 and various paragraphs of the specification have been amended solely for informality correction, better wording, and clarification. These amendments are not made to avoid prior art or narrow the

claimed invention. Therefore, Applicants do not intend to relinquish any subject matter by these amendments.

CONCLUSION

A full and complete response has been made to the pending Office Action, and all of the stated objections and grounds for rejection have been overcome or rendered moot. Accordingly, all pending claims are allowable, and the application is in condition for allowance.

The Examiner is invited to contact Applicants' undersigned representative at the number below if it would expedite prosecution. Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully submitted,

/hae-chan park/

Hae-Chan Park
Reg. No. 50,114

Date: March 11, 2011

CUSTOMER NUMBER: 58027
H.C. Park & Associates, PLC
8500 Leesburg Pike
Suite 7500
Vienna, VA 22182
Tel: 703-288-5105
Fax: 703-288-5139
HCP/SSC/kca

Electronic Acknowledgement Receipt	
EFS ID:	9638562
Application Number:	12613275
International Application Number:	
Confirmation Number:	5984
Title of Invention:	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jong Lam LEE
Customer Number:	58027
Filer:	Hae-Chan Park/Charles Greene
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317USD1
Receipt Date:	11-MAR-2011
Filing Date:	05-NOV-2009
Time Stamp:	11:41:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P2317USD1_Reply.pdf	56103 aa6b68d1c0f326914c5758e5ca9c3c0dd0e5172d	yes	11

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Specification	2	3
	Claims	4	8
	Applicant Arguments/Remarks Made in an Amendment	9	11
Warnings:			
Information:			
	Total Files Size (in bytes):	56103	

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/613,275	11/05/2009	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	03/11/2011	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 15	Minus	** 20	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	**0**

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/Katischa R. Wanzer/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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NOTICE OF ALLOWANCE AND FEE(S) DUE

58027 7590 03/25/2011
H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

EXAMINER	
NGUYEN, THINH T	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/25/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/613,275	11/05/2009	Jong Lam LEE	P2317USD1	5984

TITLE OF INVENTION: LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	06/27/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

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If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

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Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/613,275	11/05/2009	Jong Lam LEE	P2317USD1	5984

TITLE OF INVENTION: LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	06/27/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, THINH T	2818	438-028000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee
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❑ A check is enclosed.
❑ Payment by credit card. Form PTO-2038 is attached.
❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/613,275	11/05/2009	Jong Lam LEE	P2317USD1	5984

58027 7590 03/25/2011

H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

EXAMINER	
NGUYEN, THINH T	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 03/25/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/613,275	LEE ET AL.	
	Examiner	Art Unit	
	THINH T. NGUYEN	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *03/11/2011*.

2. ☒ The allowed claim(s) is/are *1-7 and 10-17*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Thinh T Nguyen /
Primary Examiner
Art Unit: 2818

DETAILED ACTION

1. Claims 1-7, 10-17 are pending in the Application.

Reason for allowance

2. Claims 1-7,10-17 are allowed.

The following is an examiner's statement of reason for allowance:

I/ Group I : Claims 1-7,10:

None of the references of record teaches or suggests the claimed METHOD OF MANUFACTURING A LIGHT EMITTING DEVICE having the limitations/steps:

-- " removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern wherein forming the etching mask pattern comprises: forming a photoresist on the P-type semiconductor layer; exposing the photoresist to light; and developing the light-exposed photoresist without a baking process after the light exposure."--

In combination with all other limitations /steps as recited in claim 1.

Note that withdrawn claim 3-4 are rejoined and allowed pursuant to 37 CFR 1.141 because they are Species that depend or otherwise have all the limitations of allowable generic claim 1.

II/ Group II : Claims 11-17:

None of the references of record teaches or suggests the claimed METHOD OF MANUFACTURING A LIGHT EMITTING DEVICE having the limitations/steps:

-- " removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern, wherein forming the etching mask pattern comprises: forming a photoresist on the P-type semiconductor layer; exposing the photoresist to light; hard-baking and developing the photoresist; and etching a side surface of the developed photoresist to have the slope from the horizontal plane "--

In combination with all other limitations /steps as recited in claim 11.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

CONCLUSION

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on Monday-Friday 9:30am-6:30pm.If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached at 571-272-1657.The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thinh T Nguyen/
Primary Examiner

Art unit 2818

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 5984

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/613,275	11/05/2009	257	2818	P2317USD1

APPLICANTS

Jong Lam LEE, Pohang-si, KOREA, REPUBLIC OF;
Jae Ho LEE, Yongin-si, KOREA, REPUBLIC OF;
Yeo Jin YOON, Ansan-si, KOREA, REPUBLIC OF;
Eu Jin HWANG, Ansan-si, KOREA, REPUBLIC OF;
Dae Won KIM, Gireum-dong, KOREA, REPUBLIC OF;

**** CONTINUING DATA **************************

This application is a DIV of 11/993,965 12/26/2007
which is a 371 of PCT/KR2006/002427 06/22/2006

**** FOREIGN APPLICATIONS **************************

REPUBLIC OF KOREA 10-2005-0053797 06/22/2005
REPUBLIC OF KOREA 10-2005-0055179 06/24/2005
REPUBLIC OF KOREA 10-2006-0021801 03/08/2006

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

11/17/2009

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /THINH T NGUYEN/ Examiner's Signature	☑ Met after Allowance /TTN/ Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		KOREA, REPUBLIC OF	12	10	1

ADDRESS

H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182
UNITED STATES

TITLE

LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME

FILING FEE RECEIVED		
1090	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"7741228"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 21:14
L2	1	12/539836	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 21:19
L3	1	12/613275	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 21:48
L4	5	(form$4 forming) same (etch$4 near9 mask$4 near9 pattern$4) same (inclined near9 slope) same (horizontal near9 plane) same ((P-type P) near9 (semiconductor semi adj conductor))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:05
L5	5	(form$4 forming) same (etch$4 near9 mask$4 near9 pattern$4) same (inclined near9 slope) same (horizontal near9 plane) same ((P-type P) near9 (semiconductor semi adj conductor))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/20 22:28
L6	4008	(438/28,29,26).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:29
L7	4205	(257/88,81,82).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:30

L8	5043	(438/22,24,46,47).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:31
L9	4850	(form$4 forming) same (photoresist photomask $4) same (p P-type) near9 semiconductor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:33
L10	5	9 same expos$4 same (photoresist photo adj resist photo mask$4) same light same develop $4 same without same ((bake baking) near9 process) same after	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:37
L11	5	9 same expos$4 same (photoresist photo adj resist photo mask$4) same light same develop $4 same without same ((bake baking) near9 process) same after	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/20 22:37
L13	1	"12" same expos$4 same (photoresist photo adj resist photo mask$4) same light same develop $4 same without same ((bake baking) near9 process) same after	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:37
L15	2	5 and 6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/20 22:39
L16	4	5 and 7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/20 22:39
L17	0	5 and 8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/20 22:39

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp

L12	2509	(form$4 forming) same (photoresist photomask $4) same (p P-type) near9 semiconductor	USPAT; UPAD	OR	OFF	2011/03/20 22:37
L14	1	L12 same expos$4 same (photoresist photo adj resist photo mask$4) same light same develop $4 same without same ((bake baking) near9 process) same after	USPAT; UPAD	OR	OFF	2011/03/20 22:38

3/20/11 10:54:03 PM
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"7741228"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 21:14
L2	1	12/539836	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 21:19
L3	1	12/613275	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 21:48
L4	5	(form$4 forming) same (etch$4 near9 mask$4 near9 pattern$4) same (inclined near9 slope) same (horizontal near9 plane) same ((P-type P) near9 (semiconductor semi adj conductor))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:05
L5	5	(form$4 forming) same (etch$4 near9 mask$4 near9 pattern$4) same (inclined near9 slope) same (horizontal near9 plane) same ((P-type P) near9 (semiconductor semi adj conductor))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/20 22:28
L6	4008	(438/28,29,26).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:29
L7	4205	(257/88,81,82).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:30

L8	5043	(438/22,24,46,47).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:31
L9	4850	(form$4 forming) same (photoresist photomask $4) same (p P-type) near9 semiconductor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:33
L10	5	9 same expos$4 same (photoresist photo adj resist photo mask$4) same light same develop $4 same without same ((bake baking) near9 process) same after	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:37
L11	5	9 same expos$4 same (photoresist photo adj resist photo mask$4) same light same develop $4 same without same ((bake baking) near9 process) same after	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/20 22:37
L13	1	"12" same expos$4 same (photoresist photo adj resist photo mask$4) same light same develop $4 same without same ((bake baking) near9 process) same after	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:37
L15	2	5 and 6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/20 22:39
L16	4	5 and 7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/20 22:39
L17	0	5 and 8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/20 22:39
L18	15979	etch$4 same (bake baking)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/20 22:55

EAST Search History (Interference)

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L12	2509	(form$4 forming) same (photoresist photomask $4) same (p P-type) near9 semiconductor	USPAT; UPAD	OR	OFF	2011/03/20 22:37
L14	1	L12 same expos$4 same (photoresist photo adj resist photo mask$4) same light same develop $4 same without same ((bake baking) near9 process) same after	USPAT; UPAD	OR	OFF	2011/03/20 22:38
L19	7232	etch$4 same (bake baking)	USPAT; UPAD	OR	ON	2011/03/20 23:01
L20	1	L12 same expos$4 same (photoresist photo adj resist photo mask$4) same light same develop $4 same without same ((bake baking) near9 process) same after	USPAT; UPAD	OR	ON	2011/03/20 23:02

3/20/11 11:02:30 PM
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Issue Classification

Application/Control No.	Applicant(s)/Patent Under Reexamination
12613275	LEE ET AL.
Examiner	**Art Unit**
THINH T NGUYEN	2818

ORIGINAL		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
438	28	H	0	1	L	27 / 15 (2006.01.01)					

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
438	28	29	26	22	
257	81	88			

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1														
2	2														
3	3														
4	4														
5	5														
6	6														
7	7														
8	10														
9	11														
10	12														
11	13														
12	14														
13	15														
14	16														
15	17														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	15	
/THINH T NGUYEN/ Primary Examiner.Art Unit 2818	03/2011	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	FIG 29

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12613275	LEE ET AL.
	Examiner	Art Unit
	THINH T NGUYEN	2818

SEARCHED			
Class	Subclass	Date	Examiner
438	28,29,26	12/15/10	TTN
438	22,24,46,47	3/20/11	TTN
257	81,82,88	3/20/11	TTN

SEARCH NOTES		
Search Notes	Date	Examiner
east	12/10/10	TTN
east	3/20/11	TTN

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
438	28,29	3/20/11	TTN
east	text	3/20/11	TTN

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12613275	LEE ET AL.
	Examiner	**Art Unit**
	THINH T NGUYEN	2818

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/25/2010	12/15/2010	03/20/2011						
1	1	÷	✓	=						
2	2	÷	✓	=						
3	3	÷	N	=						
4	4	÷	N	=						
5	5	÷	✓	=						
6	6	÷	✓	=						
7	7	÷	✓	=						
	8	÷	O	-						
	9	÷	✓	-						
8	10	÷	✓	=						
9	11			=						
10	12			=						
11	13			=						
12	14			=						
13	15			=						
14	16			=						
15	17			=						

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2	"7741228"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 21:14
S2	1	12/539836	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 21:19
S3	1	12/613275	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 21:48
S4	5	(form$4 forming) same (etch$4 near9 mask$4 near9 pattern$4) same (inclined near9 slope) same (horizontal near9 plane) same ((P-type P) near9 (semiconductor semi adj conductor))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:05
S5	5	(form$4 forming) same (etch$4 near9 mask$4 near9 pattern$4) same (inclined near9 slope) same (horizontal near9 plane) same ((P-type P) near9 (semiconductor semi adj conductor))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/20 22:28
S6	4008	(438/28,29,26).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:29
S7	4205	(257/88,81,82).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:30

S8	5043	(438/22,24,46,47).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:31
S9	4850	(form$4 forming) same (photoresist photomask $4) same (p P-type) near9 semiconductor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:33
S10	5	S9 same expos$4 same (photoresist photo adj resist photo mask$4) same light same develop $4 same without same ((bake baking) near9 process) same after	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:37
S11	5	S9 same expos$4 same (photoresist photo adj resist photo mask$4) same light same develop $4 same without same ((bake baking) near9 process) same after	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/20 22:37
S12	1	"12" same expos$4 same (photoresist photo adj resist photo mask$4) same light same develop $4 same without same ((bake baking) near9 process) same after	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/20 22:37
S13	2	S5 and S6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/20 22:39
S14	4	S5 and S7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/20 22:39
S15	0	S5 and S8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/20 22:39
S16	15979	etch$4 same (bake baking)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/03/20 22:55

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S17	2509	(form$4 forming) same (photoresist photomask $4) same (p P-type) near9 semiconductor	USPAT; UPAD	OR	OFF	2011/03/20 22:37
S18	1	S17 same expos$4 same (photoresist photo adj resist photo mask$4) same light same develop $4 same without same ((bake baking) near9 process) same after	USPAT; UPAD	OR	OFF	2011/03/20 22:38
S19	7232	etch$4 same (bake baking)	USPAT; UPAD	OR	ON	2011/03/20 23:01
S20	1	S17 same expos$4 same (photoresist photo adj resist photo mask$4) same light same develop $4 same without same ((bake baking) near9 process) same after	USPAT; UPAD	OR	ON	2011/03/20 23:02

3/21/11 8:19:06 AM
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EAST Search History

EAST Search History (Prior Art)

<This search history is empty>

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	116549	photoresist (photo near3 resist) (hard near9 mask$4)	USPAT; UPAD	OR	ON	2011/03/21 08:31
L2	65840	(P-type P) near9 (semiconductor semi adj conductor)	USPAT; UPAD	OR	ON	2011/03/21 08:32
L3	0	1 same 2 same on	USPAT; UPAD	OR	ON	2011/03/21 08:32
L4	3027	1 same 2	USPAT; UPAD	OR	ON	2011/03/21 08:33
L5	4	2 same on	USPAT; UPAD	OR	ON	2011/03/21 08:33

3/21/11 8:34:42 AM
C:\Documents and Settings\tnguyen31\My Documents\EAST\Workspaces\thinhnew2.wsp

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/613,275	11/05/2009	Jong Lam LEE	P2317USD1	5984

TITLE OF INVENTION:

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$1810	06/27/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 H.C. PARK & ASSOCIATES, PLC
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Seoul Opto Device Co., Ltd.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Ansan-si, Republic of Korea

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:
☑ Issue Fee
☑ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _

4b. Payment of Fee(s):
☐ A check in the amount of the fee(s) is enclosed.
☑ Payment by credit card. Form PTO-2038 is attached.
☑ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 50-3698 .

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /hae-chan park/ Date April 20, 2011

Typed or printed name Hae-Chan Park Registration No. 50,114

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	Docket No.: P2317USD1
Jae Ho LEE, *et al*.	
Serial No.: 12/613,275	Group Art Unit: 2818
Confirmation No.: 5984	
Filed: November 5, 2009	Examiner: NGUYEN, THINH T.

For: **LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME**

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Sir:

Applicants appreciate the indication in the Notice of Allowance mailed March 25, 2011 that claims 1-7 and 10-17 are allowed. While Applicants agree these claims are patentable over the cited references, Applicants do not agree that patentability resides in each feature exactly as expressed in the claims, nor that each feature is required for patentability of each claim.

Respectfully Submitted,

/hae-chan park/

Hae-Chan Park
Reg. No. 50,114

Date: April 20, 2011

CUSTOMER NUMBER: 58027
HCP/SSC/es

Electronic Patent Application Fee Transmittal

Application Number:	12613275
Filing Date:	05-Nov-2009
Title of Invention:	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jong Lam LEE
Filer:	Hae-Chan Park/ethan song
Attorney Docket Number:	P2317USD1

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1810**

Electronic Acknowledgement Receipt

EFS ID:	9919162
Application Number:	12613275
International Application Number:	
Confirmation Number:	5984
Title of Invention:	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jong Lam LEE
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317USD1
Receipt Date:	20-APR-2011
Filing Date:	05-NOV-2009
Time Stamp:	17:03:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1810
RAM confirmation Number	3897
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Issue Fee Payment (PTO-85B)	P2317USD1_IssueFee_Transmittal.pdf	239033 1e3c1f86ede2caa7ba1dc883eef161b7a62ea8f2	no	2
Warnings:					
Information:					
2	Post Allowance Communication - Incoming	P2317USD1_Comments_RFA.pdf	13549 cb91247556a5d7b4ec95549fd00434e0bb68f049	no	1
Warnings:					
Information:					
3	Fee Worksheet (PTO-875)	fee-info.pdf	31877 e2f8a6354df1cb009864f3952d999ea9c55b0742	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	284459	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Receipt date: 11/05/2009	Application Number	12613275 - GAU: 2818
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)	Filing Date	2009-11-05
	First Named Inventor	Jong Lam LEE
	Art Unit	
	Examiner Name	
	Attorney Docket Number	P2317USD1

	5	20050225973		2005-10-13	Eliashevich, et al.	
	6	20080230765		2008-09-25	Yoon, et al.	
Change(s) applied to document, /S.R.R./ 4/22/2011	7	20060043433		~~2003~~ 2006-03-02	Matsushita	
	8	20050224973		2005-10-13	Bernier, et al.	
	9	20060044864		2006-03-02	Lin, et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	04-023568	WO		2004-03-18	Nitride Semiconductors Co., Ltd.		☐
	2	04-013916	WO		2004-02-12	Nichia Corporation		☐
	3	10-2006-0037589	KR		2006-05-03	Seoul Semiconductor Co., Ltd.		☐
	4	2002-026378	JP		2002-01-25	Kyocera Corp.		☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /T.N./

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)		
	Application Number	12613275
	Filing Date	2009-11-05
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317USD1

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12613275
	Filing Date	2009-11-05
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317USD1

	1	Notice of Allowance of US Patent Application No. 12/630,370 issued on May 6, 2011.	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12613275
	Filing Date	2009-11-05
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317USD1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2011-05-11
Name/Print	Hae-Chan Park	Registration Number	50114

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal	
Application Number:	12613275
Filing Date:	05-Nov-2009
Title of Invention:	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jong Lam LEE
Filer:	Hae-Chan Park/eun jo
Attorney Docket Number:	P2317USD1
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt	
EFS ID:	10065908
Application Number:	12613275
International Application Number:	
Confirmation Number:	5984
Title of Invention:	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jong Lam LEE
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317USD1
Receipt Date:	11-MAY-2011
Filing Date:	05-NOV-2009
Time Stamp:	14:35:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$180
RAM confirmation Number	852
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Information Disclosure Statement (IDS) Filed (SB/08)	P2317USD1_IDS.pdf	990400 331eed4e57385491e0928f0d0f9cd3b95a71fc7	no	4
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
2	NPL Documents	P2317USC2_NOA_5_6_2011.pdf	561268 5a5011919ee677a4051a4264b06f212552ba88d0	no	13
Warnings:					
Information:					
3	Fee Worksheet (PTO-875)	fee-info.pdf	30450 67b790d512e8fed597edcdad31722780190629eb	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	1582118	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/613,275	05/31/2011	7951626	P2317USD1	5984

58027 7590 05/11/2011

H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Jong Lam LEE, Pohang-si, KOREA, REPUBLIC OF;
Jae Ho LEE, Yongin-si, KOREA, REPUBLIC OF;
Yeo Jin YOON, Ansan-si, KOREA, REPUBLIC OF;
Eu Jin HWANG, Ansan-si, KOREA, REPUBLIC OF;
Dae Won KIM, Gireum-dong, KOREA, REPUBLIC OF;

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the Southern District of New York on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
1:16-cv-06276	8/8/2016	for the Southern District of New York

PLAINTIFF	DEFENDANT
Seoul Viosys Co., Ltd.	P3 International Corporation

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,982,207	7/19/2011	Seoul Opto Device Co., Ltd.
2	7,951,626	5/31/2011	Seoul Opto Device Co., Ltd.
3	9,203,006	12/1/2015	Seoul Semiconductor Co., Ltd.
4	8,692,282	4/8/2014	Seoul Semiconductor Co., Ltd.
5	8,168,988	5/1/2012	Seoul Opto Device Co., Ltd.

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
Ruby J. Krajick	/s/ P. Canales	8/18/2016

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AO 120 (Rev. 08/10)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court California Central District Court on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
16cv6782	9/9/2016	California Central District Court

PLAINTIFF	DEFENDANT
Seol Semiconductor	K-Mart Corp.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6942731		
2	7626209		
3	7906789		
4	7951626		
5	7,982,207		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	8,664,638		
2	8,860,331		
3	9,240,529		
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

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AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Nevada on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT Nevada
PLAINTIFF Seoul Semiconductor Co., Ltd., et al.		DEFENDANT Philcort T.V. & Electronic Leasing, Inc.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT
See attached Consent Judgment, ECF No. 22

CLERK	(BY) DEPUTY CLERK	DATE
/s/ Debra K. Kempi	/s/ Angela Reyes	8/31/18

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Patents

Cases Involving Patents
DNV-2-18-cv-00383

Seoul Semiconductor Co., Ltd. et al v. Philcor TV & Electronic Leasing, Inc. d/b/a energyavenue.com DNV-2-18-cv-00383

VIEW IN BROWSER

Patent ▲	Patent Name	First Inventor	Grant Date
7646031	Light emitting device having light emitting elements	Sakai	Jan. 12, 2010
7700960	Light emitting diode with ITO layer and method for fabricating the same	Kim	Apr. 20, 2010
7768020	AC light emitting diode	Kim	Aug. 03, 2010
7804098	Light emitting element with a plurality of cells bonded, method of manufacturing the same, and light emitting d...	Lee	Sep. 28, 2010
7951626	Light emitting device and method of manufacturing the same	Lee	May. 31, 2011
8084774	Light emitting device having light emitting elements	Sakai	Dec. 27, 2011
8168988	Light emitting element with a plurality of cells bonded, method of manufacturing the same, and light emitting d...	Lee	May. 01, 2012
8188489	Light emitting diode for AC operation	Lee	May. 29, 2012
8299476	Light emitting diode having light emitting cell with different size and light emitting device thereof	Lee	Oct. 30, 2012
8664638	Light-emitting diode having an interlayer with high voltage density and method for manufacturing the same	Yoo	Mar. 04, 2014
8680533	Light-emitting device having light-emitting elements with a shared electrode	Sakai	Mar. 25, 2014
8716946	Light emitting device for AC power operation	Lee	May. 06, 2014
8829552	Light emitting device	Seo	Sep. 09, 2014
8860331	Light emitting device for AC power operation	Lee	Oct. 14, 2014
8901575	AC light emitting diode and method for fabricating the same	Lee	Dec. 02, 2014
9093627	Light emitting diode and method of fabricating the same	Lee	Jul. 28, 2015
9450155	Light emitting device having wavelength converting layer	Jung	Sep. 20, 2016
9577157	Light emitting diode chip having distributed Bragg reflector and method of fabricating the same	Lee	Feb. 21, 2017
9627435	Light emitting device	Lee	Apr. 18, 2017
9716210	Light emitting diode and method of fabricating the same	Kim	Jul. 25, 2017

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District, Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:18-cv-00386	8/31/2018	Eastern District, Texas

PLAINTIFF	DEFENDANT
Seoul Semiconductor Co., Ltd. and Seoul Viosys Co., Ltd.	Fry's Electronics, Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	8,829,552	9/9/2014	Seoul Semiconductor Co., Ltd.
2	8,525,212	9/3/2013	Seoul Viosys Co., Ltd.
3	7,901,113	3/8/2011	Seoul Semiconductor Co., Ltd.
4	9,530,947	12/27/2016	Seoul Semiconductor Co., Ltd.
5			Please see attached for continuation

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT
CONSENT JUDGMENT AND PERMANENT INJUNCTION

CLERK	(BY) DEPUTY CLERK	DATE
David A. O'Toole	nkl	10/7/19

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	Patent or Trademark No.	Date of Patent or Trademark	Holder of Patent or Trademark
5	9,022,618	5/5/2015	Seoul Semiconductor Co. Ltd.
6	8,608,328	12/17/2013	Seoul Semiconductor Co. Ltd.
7	7,618,162	11/17/2009	Seoul Semiconductor Co. Ltd.
8	8,132,952	3/13/2012	Seoul Semiconductor Co. Ltd.
9	8,058,662	11/15/2011	Seoul Semiconductor Co. Ltd.
10	9,577,157	2/21/2017	Seoul Viosys Co., Ltd.
11	9,343,631	5/17/2016	Seoul Viosys Co., Ltd.
12	7,951,626	5/31/2011	Seoul Viosys Co., Ltd.
13	9,799,800	10/24/2017	Seoul Viosys Co., Ltd.
14	9,716,210	7/25/2017	Seoul Viosys Co., Ltd.
15	6,942,731	9/13/2005	Seoul Semiconductor Co. Ltd.

AO 120 (Rev. 08/10)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Northern District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
3:18-cv-00508-K	3/2/2018	Northern District of Texas

PLAINTIFF	DEFENDANT
Seoul Semiconductor Co Ltd, Seoul Viosys Co Ltd	Service Lighting and Electrical Supplies Inc d/b/a 1000bulbs.com

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	9,627,435	4/18/2017	Seoul Viosys Co Ltd
2	9,093,627	7/28/2015	Seoul Viosys Co Ltd
3	9,577,157	2/21/2017	Seoul Viosys Co Ltd
4	7,700,960	4/20/2010	Seoul Viosys Co Ltd
5			Please see attached for continuation

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading		
	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT
Judgment-9/12/2019

CLERK	(BY) DEPUTY CLERK	DATE
Karen Mitchell	s/E. Monk	9/12/2019

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	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
5	8,168,988	5/1/2012	Seoul Viosys Co Ltd
6	8,860,331	10/14/2014	Seoul Viosys Co Ltd
7	8,829,552	9/9/2014	Seoul Viosys Co Ltd
8	8,716,946	5/6/2014	Seoul Viosys Co Ltd
9	7,951,626	5/31/2011	Seoul Viosys Co Ltd
10	8,664,638	3/4/2014	Seoul Viosys Co Ltd