PTO-1390 (Rev. 09-2007)
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TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A SUBMISSION UNDER 35 U.S.C. 371

		ATTORNEY'S DOCKET NUMBER: 3576-053
		U.S. APPLICATION NO. (If known, see 37 CFR 1.5):
INTERNATIONAL APPLICATION NO.: PCT/KR2006/002427	INTERNATIONAL FILING DATE: June 22, 2006	PRIORITY DATE CLAIMED: June 22, 2005

TITLE OF INVENTION: LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME

APPLICANT(S) FOR DO/EO/US: Seoul Opto-Device Co., Ltd.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☑ This is a **FIRST** submission of items concerning a submission under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a submission under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☑ The US has been elected (Article 31).
5. ☑ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☑ is attached hereto (required only if not communicated by the International Bureau).
   b. ☐ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☑ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☑ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☑ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. ☑ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☑ A preliminary amendment. Please enter Preliminary Amendment before calculating fees.
14. ☑ An Application Data Sheet under 37 CFR 1.76.
15. ☐ A substitute specification.
16. ☐ A power of attorney and/or change of address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13*ter*.2 and 37 CFR 1.821- 1.825.
18. ☐ A second copy of the published International Application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).

This collection of information is required by 37 CFR 1.414 and 1.491-1.492. The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 15 minutes to complete, including gathering information, preparing, and submitting the completed form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S.

U.S. APPLICATION NO. (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
	PCT/KR2006/002427	3576-053

20. Other items or information:

International Search Report

The following fees have been submitted	CALCULATIONS	PTO USE ONLY
21. ☑ Basic national fee (37 CFR 1.492(a)) **$310**	$ 310.00	
22. ☑ Examination fee (37 CFR 1.492(c)) If the written opinion prepared by ISA/US or the international preliminary examination report prepared by IPEA/US indicates all claims satisfy provisions of PCT Article 33(1)-(4) ..... **$0** All other situations **$210**	$ 210	
23. ☑ Search fee (37 CFR 1.492(b)) If the written opinion of the ISA/US or the International preliminary examination report prepared by IPEA/US indicates all claims satisfy provisions of PCT Article 33(1)-(4) ..... **$0** Search fee (37 CFR 1.445(a)(2)) has been paid on the international application to the USPTO as an International Searching Authority ..... **$100** International Search Report prepared by an ISA other than the US and provided to the Office or previously communicated to the US by the IB ..... **$410** All other situations **$510**	$ 410	
TOTAL OF 21, 22 and 23 =	930.00	

☐ Additional fee for specification and drawings filed in paper over 100 sheets (excluding sequence listing in compliance with 37 CFR 1.821(c) or (e) in an electronic medium or computer program listing in an electronic medium) (37 CFR 1.492(j)).
The fee is **$260** for each additional 50 sheets of paper or fraction thereof.

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof (round **up** to a whole number)	RATE	
49 - 100 =	0 /50 =		x $**260**	$ 0

Surcharge of **$130.00** for furnishing any of the search fee, examination fee, or the oath or declaration after the date of commencement of the national stage (37 CFR 1.492(h)).	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	$	
Total claims	16 - 20 =	0	x $ **50**	$ 0	
Independent claims	3 - 3 =	0	x **$210**	$ 0	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$370**	$	
			TOTAL OF ABOVE CALCULATIONS =	$ 930.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. Fees above are reduced by ½.					
			SUBTOTAL =	$ 930.00	
Processing fee of **$130.00** for furnishing the English translation later than 30 months from the earliest claimed priority date (37 CFR 1.492(i)). +				$	
			TOTAL NATIONAL FEE =	$ 930.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$	
			TOTAL FEES ENCLOSED =	$ 930.00	
			Amount to be refunded:	$	
			Amount to be charged	$	

a. ☐ A check in the amount of $ _____ to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $ _____ to cover the above fees.
A duplicate copy of this sheet is enclosed.

c. ☑ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 131703. A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038. The PTO-2038 should only be mailed or faxed to the USPTO. However, when paying the basic national fee, the PTO-2038 may NOT be faxed to the USPTO.

ADVISORY: If filing by EFS-Web, do **NOT** attach the PTO-2038 form as a PDF along with your EFS-Web submission. Please be advised that this is **not** recommended and by doing so your **credit card information may be displayed via PAIR**. To protect your information, it is recommended paying fees online by using the electronic payment method.

NOTE: Where an appropriate time limit under 37 CFR 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the International Application to pending status.

SEND ALL CORRESPONDENCE TO:



SIGNATURE

Hosoon Lee

NAME

56737

REGISTRATION NUMBER

PATENT APPLICATION
Do. No. 3576-053
Client Ref.: PO070209

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Jong Lam Lee, Jae Ho Lee, Yeo Jin Yoon, Eu Jin Hwang, Dae Won Kim

Serial No. not yet assigned

Filed: Concurrently herewith

For: LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Prior to Examination, please amend the application as follows:

Amendments to the Specification begin on page 2 of this paper

Amendments to the Claims begin on page 3 of this paper

Remarks begin on page 6 of this paper.

IN THE SPECIFICATION

At page 1, line 2, please insert the following new paragraph:

--CROSS-REFERENCE TO RELATED APPLICATION

This application is a U.S. national phase application of PCT International Application No. PCT/KR2006/002427, filed June 22, 2006, which claims priority of Korean Patent Application No. 10-2005-0053797, filed June 22, 2005, Korean Patent Application No. 10-2005-0055179, filed June 24, 2005 and Korean Patent Application No. 10-2006-0021801, filed March 8, 2006 the contents of which are incorporated herein by reference in their entirety.--

IN THE CLAIMS

1. (Original) A light emitting device, comprising:
a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on a portion of the N-type semiconductor layer on a substrate,
wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including the N-type or P-type semiconductor layer of the light emitting cell has a slope of 20 to 80° from a horizontal plane.

2. (Original) The light emitting device as claimed in claim 1, further comprising a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

3. (Currently Amended) The light emitting device as claimed in claim 1 [[or 2]], further comprising a transparent electrode layer on the P-type semiconductor layer.

4. (Currently Amended) The light emitting device as claimed in claim 1 [[or 2]], further comprising P-type and N-type ohmic metal layers containing Cr or Au on the P-type and N-type semiconductor layers, respectively.

5. (Original) A light emitting device, comprising:
a substrate formed with a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on the N-type semiconductor layer; and
a submount substrate flip-chip bonded onto the substrate,
wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including at least the P-type semiconductor layer of the light emitting cell has a slope of 20 to 80° from a horizontal plane.

6. (Original) The light emitting device as claimed in claim 5, further comprising

a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

7. (Original) A method of manufacturing a light emitting device, comprising the steps of:

sequentially forming N-type and P-type semiconductor layers on a substrate; forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; and removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern.

8. (Original) The method as claimed in claim 7, further comprising the steps of: removing a portion of the N-type semiconductor layer exposed through the removal of the P-type semiconductor layer to form a plurality of light emitting cells; and connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire.

9. (Original) The method as claimed in claim 7, further comprising the step of flip-chip bonding the substrate onto an additional submount substrate after the step of removing the P-type semiconductor layer and the etching mask pattern.

10. (Original) The method as claimed in claim 9, further comprising the steps of: removing a portion of the N-type semiconductor layer exposed due to the removal of the P-type semiconductor layer to form a plurality of light emitting cell; and connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire, after the step of removing the P-type semiconductor layer and the etching mask pattern.

11. (Currently Amended) The method as claimed in claim 8 [[or 10]], wherein the step of forming the plurality of light emitting cells comprises the steps of: forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer;

removing the N-type and P-type semiconductor layers exposed through the etching mask pattern to form a plurality of light emitting cells; and
removing the etching mask pattern.

12. (Currently Amended) The method as claimed in claim 8 [[or 10]], wherein the N type semiconductor layer of one light emitting cell and the P type semiconductor layer of another adjacent light emitting cell are connected with the conductive wire through a bridge or step coverage process.

13. (Currently Amended) The method as claimed in ~~any one of claims~~ claim 7 ~~to 10~~, wherein a photoresist with a thickness of 3 to 50μm is used in the step of forming the etching mask pattern.

14. (Original) The method as claimed in claim 13, wherein the step of forming the etching mask pattern comprises the steps of:
applying the photoresist onto the P-type semiconductor layer;
light exposing the photoresist in accordance with a predetermined mask pattern; and
developing the light-exposed photoresist without a baking process after the light exposure.

15. (Original) The method as claimed in claim 13, wherein the step of forming the etching mask pattern comprises the steps of:
applying the photoresist onto the P-type semiconductor layer;
light exposing the photoresist in accordance with a predetermined mask pattern;
hard baking the light-exposed photoresist at a temperature of 100 to 140°C; and
developing the hard-baked photoresist.

16. (Currently Amended) The method as claimed in claim 7 [[or 8]], further comprising the steps of:
after the step of removing the P-type semiconductor layer and the etching mask pattern,
removing a rear surface of the substrate at a certain thickness; and
depositing Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof onto the rear surface of the substrate.

REMARKS

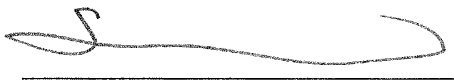
Claims 3, 4, 11, 12, 13 and 16 are amended to remove multiple dependencies.

No new matter has been added.

The Examiner is requested to call the undersigned if any questions arise concerning the above-mentioned application.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



Hosoon Lee
Reg. No. 56,737

CUSTOMER NO. 20575

MARGER JOHNSON & McCOLLOM, P.C.
210 SW Morrison Street, Suite 400
Portland, OR 97204
503-222-3613

PATENT APPLICATION
Client No. PO070209

COMBINED DECLARATION AND POWER OF ATTORNEY
FILED WITH U.S. DESIGNATED OFFICE UNDER 35 U.S.C. 371(c)(4)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME**, described and claimed in international application number **PCT KR2006/002427**, filed **June 22, 2006**, which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Sec. 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Sec. 119(a)-(d) or Sec. 365(b) of any foreign application(s) for patent or inventor's certificate or Sec. 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
2005-0053979 (Number)	Republic of Korea (Country)	22 June 2005 (Day/Month/Year Filed)	☒ Yes	☐ No
2005-0055179 (Number)	Republic of Korea (Country)	24 June 2005 (Day/Month/Year Filed)	☒ Yes	☐ No
2006-0021801 (Number)	Republic of Korea (Country)	8 March 2006 (Day/Month/Year Filed)	☒ Yes	☐ No

I hereby claim the benefit under Title 35, United States Code, Sec. 119(e) of any United States provisional application listed below:

Provisional Application No. Filing Date

I hereby claim the benefit under Title 35, United States Code, Sec. 120 or §365 (c) of any PCT international application designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Sec. 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Sec. 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

PCT/KR2006/002427	22 June 2006	Pending
(Applic. Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby appoint the attorneys or agents associated with **Customer No. 20575** to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with the above application.

Direct all telephone calls to Hosoon Lee at (503) 222-3613 and send all correspondence to the following address associated with **Customer No. 20575**:

MARGER JOHNSON & McCOLLOM, P.C.
210 S.W. Morrison Street, Suite 400
Portland, Oregon 97204

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: Jong Lam LEE

Inventor's signature: _____ 12/14/07 (Date)

Residence: Pohang, 790-751 Republic of Korea

Citizenship: Republic of Korea

Post Office address: 8-1403 Gyosu Apt., Jigok-Dong, Nam-Gu,
Pohang-Si, Gyeongsangbuk-Do, 790-751, Republic of Korea

Full name of sole or first inventor: Jae Ho LEE

Inventor's signature: Jae Ho, LEE 14. Dec. 2007 (Date)

Residence: Yongin, 448-531 Republic of Korea

Citizenship: Republic of Korea

Post Office address: 309-1405, LG 3-cha Village Apt, Seongbok-Dong,
Suji-Gu, Yongin-Si,Gyeonggi-Do, 448-531, Republic of Korea

Full name of sole or first inventor: Yeo Jin YOON

Inventor's signature: 14. DEC. 2007 (Date)

Residence: Ansan, 426-738 Republic of Korea

Citizenship: Republic of Korea

Post Office address: 101-1505, Yojin Supsok Apt, Sa 1-Dong,
Sagnok-Gu, Ansan-Si, Gyeonggi-Do, 426-738, Republic of Korea

Full name of sole or first inventor: Eu Jin HWANG

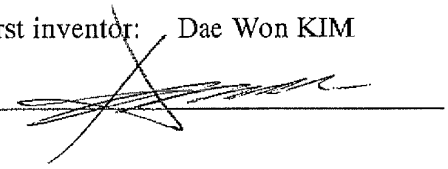
Inventor's signature: 14 Dec (Date)

Residence: Siheung, 429-856 Republic of Korea

Citizenship: Republic of Korea

Post Office address: 303, 1569-7, Jeongwang-Dong,
Siheung-Si, Gyeonggi-Do, 429-856, Republic of Korea

Full name of sole or first inventor: Dae Won KIM

Inventor's signature: 

14. Dec
(Date)

Residence: Seoul, 136-110 Republic of Korea

Citizenship: Republic of Korea

Post Office address: 303-802, Gireum New Town, 1280-2, Gireum-Dong,
Seongbuk-Gu, Seoul, 136-110, Republic of Korea

FIG. 1

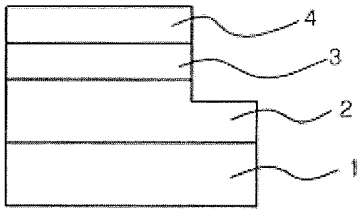


FIG. 2

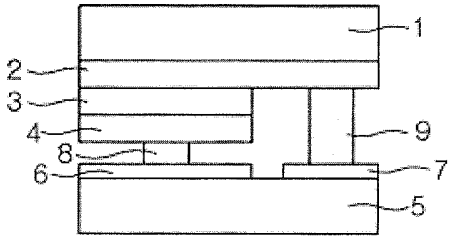


FIG. 3

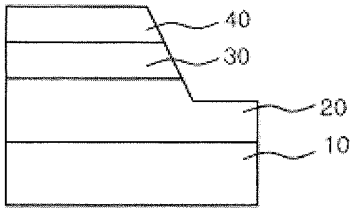


FIG. 4

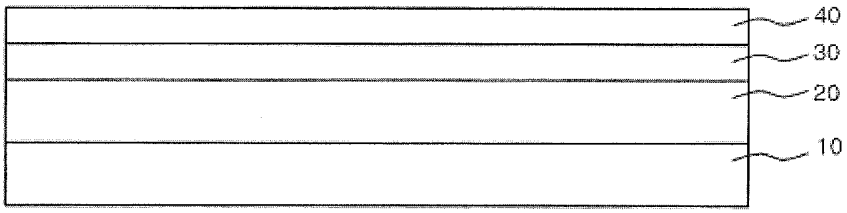


FIG. 5

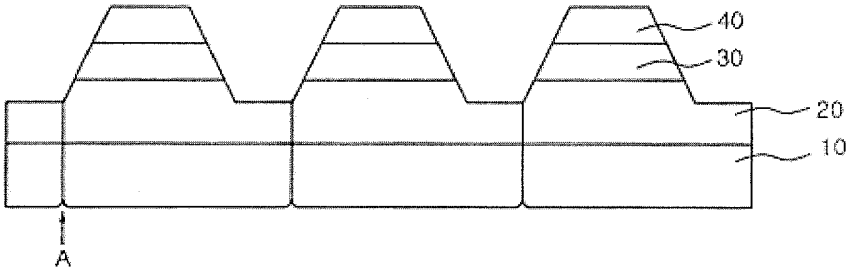


FIG. 6

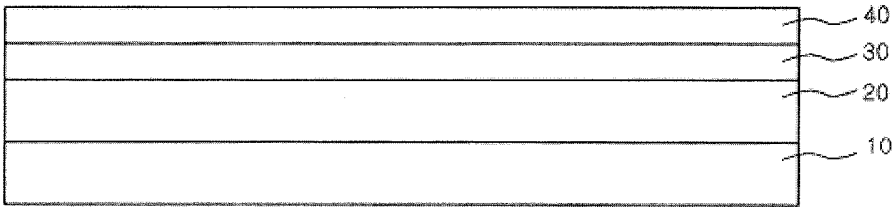


FIG. 7

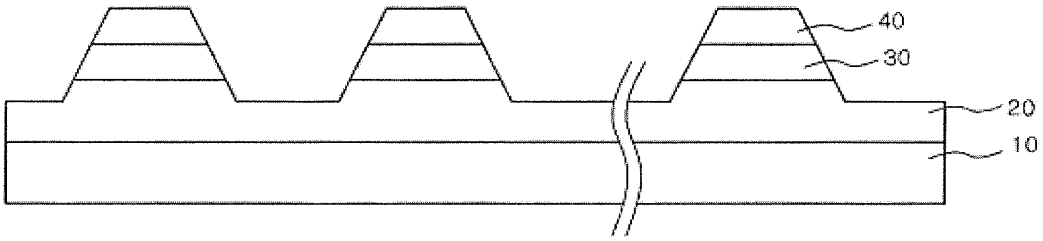


FIG. 8

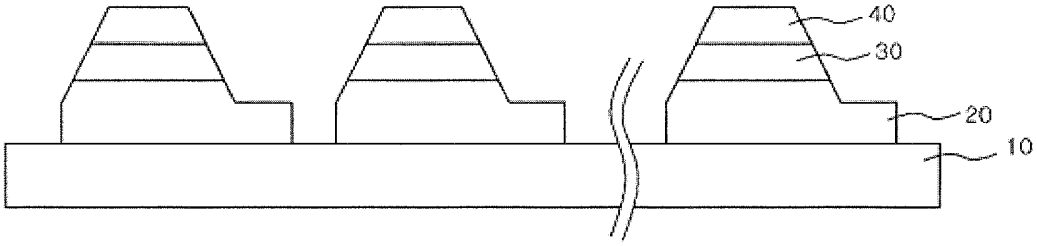


FIG. 9

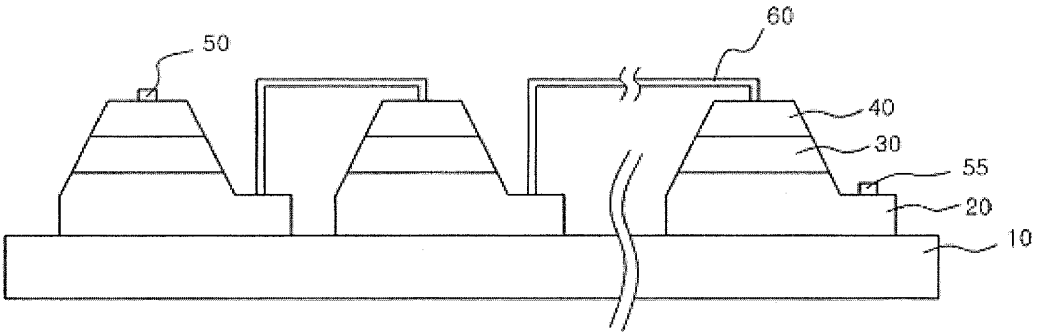


FIG. 10

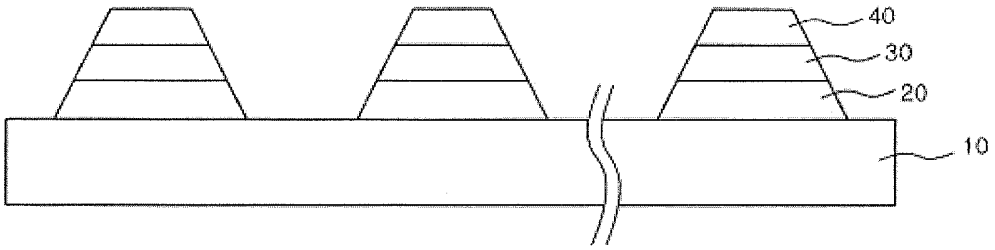


FIG. 11

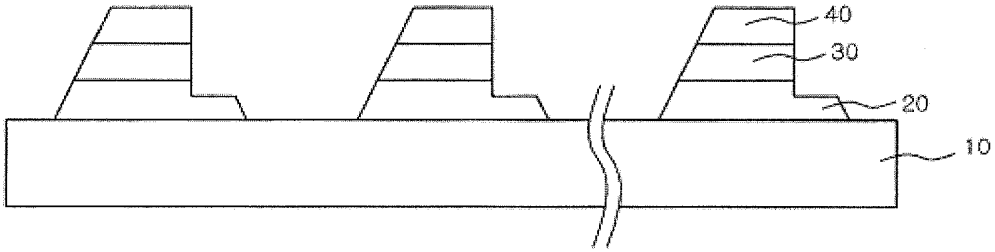


FIG. 12

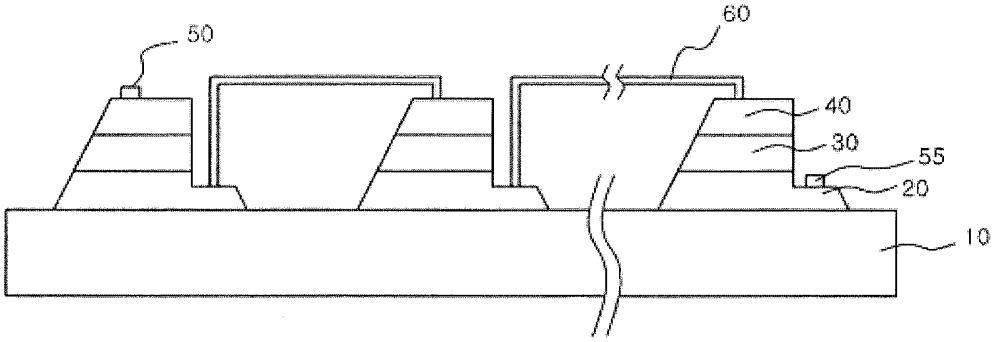


FIG. 13

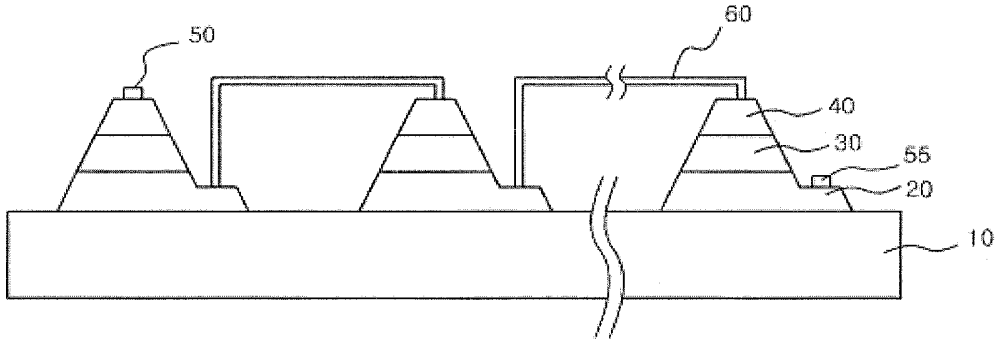


FIG. 14

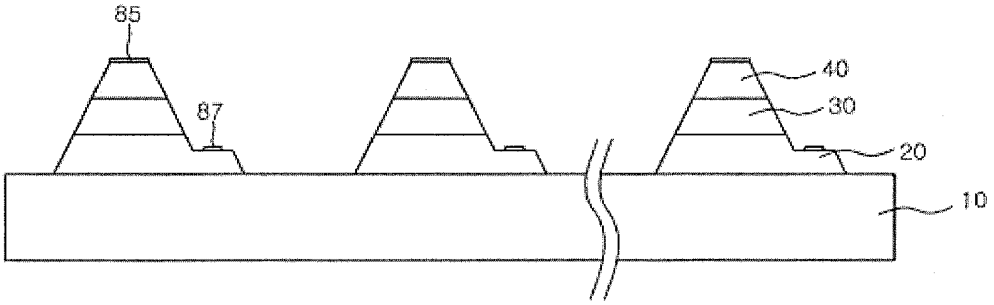


FIG. 15

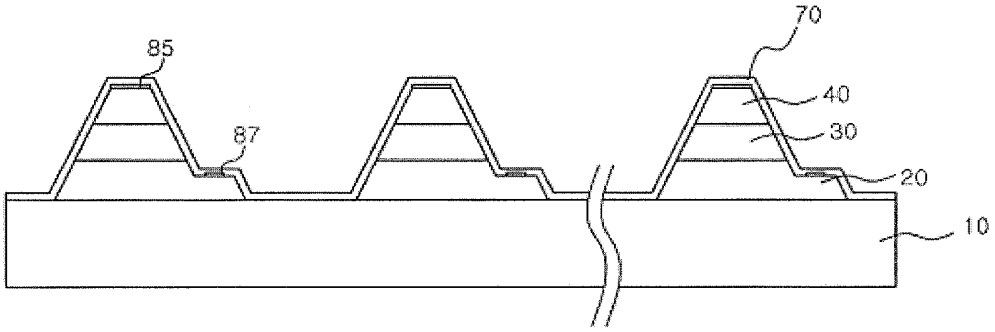


FIG. 16

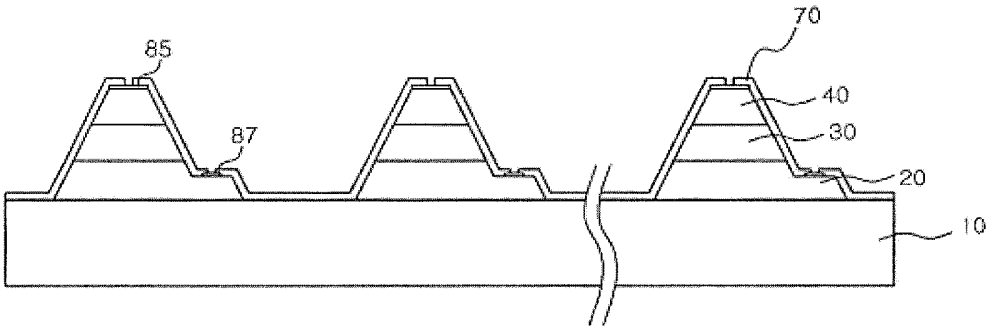


FIG. 17

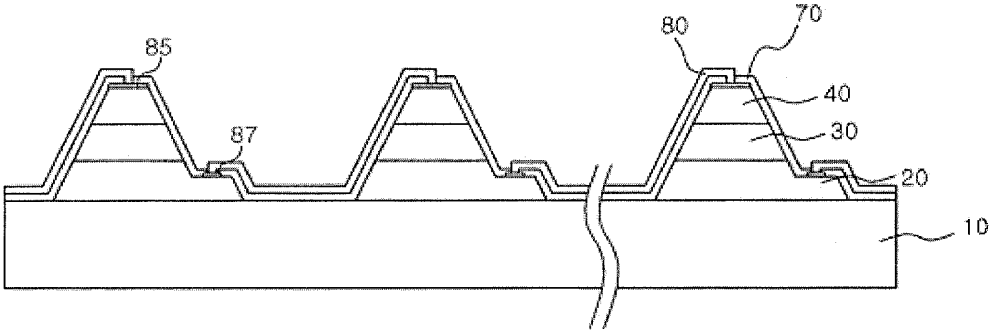


FIG. 18

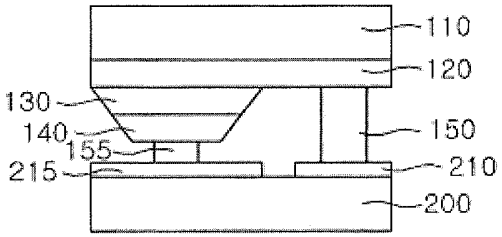


FIG. 19

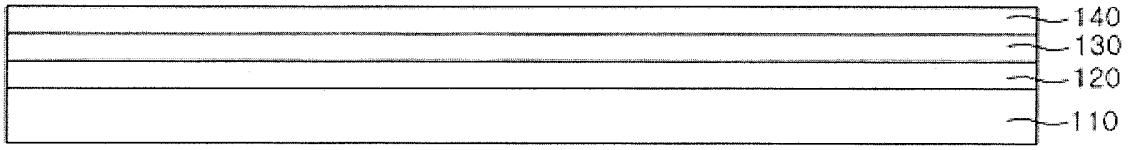


FIG. 20

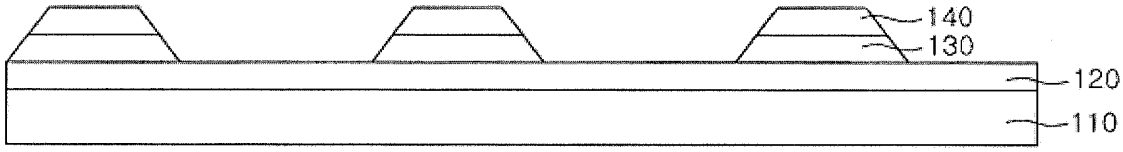


FIG. 21

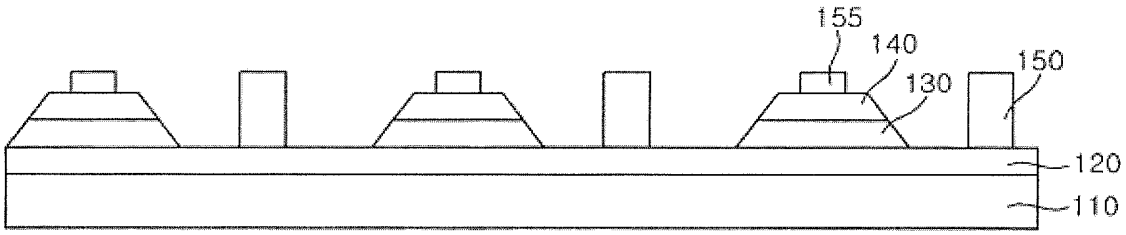


FIG. 22

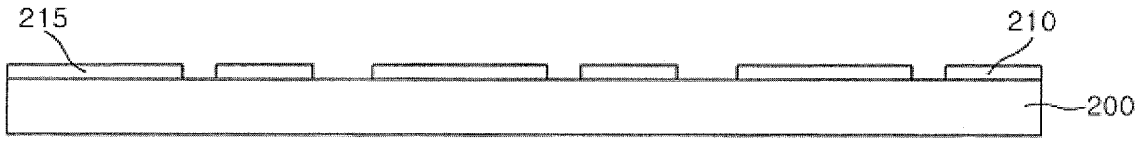


FIG. 23

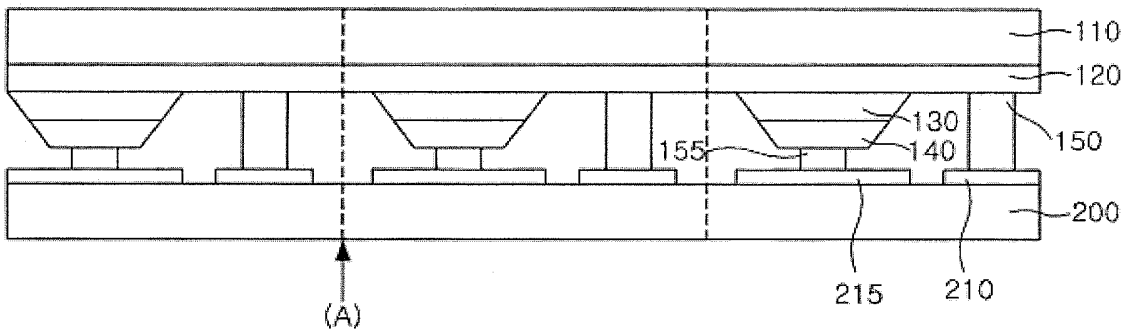


FIG. 24

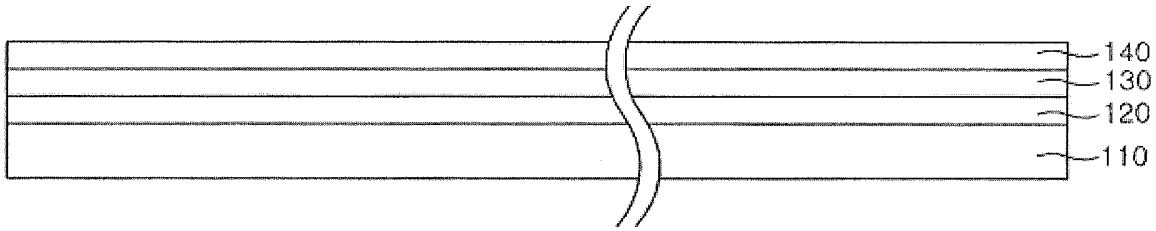


FIG. 25

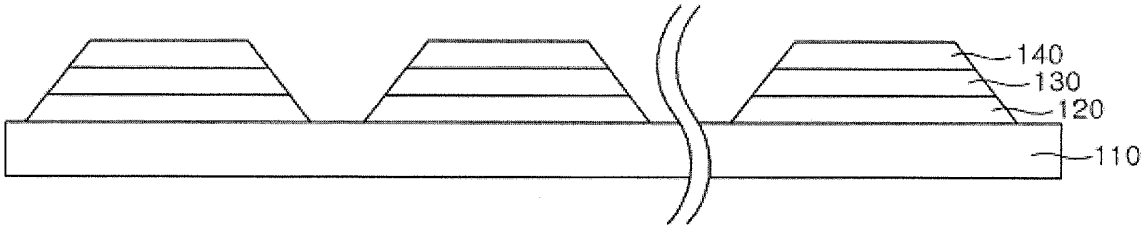


FIG. 26

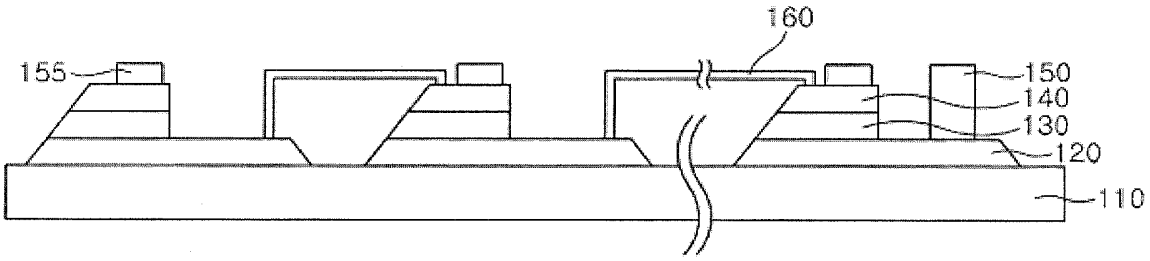
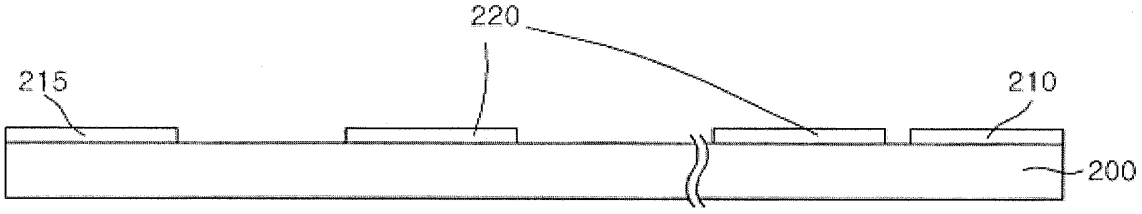


FIG. 27



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FIG. 28

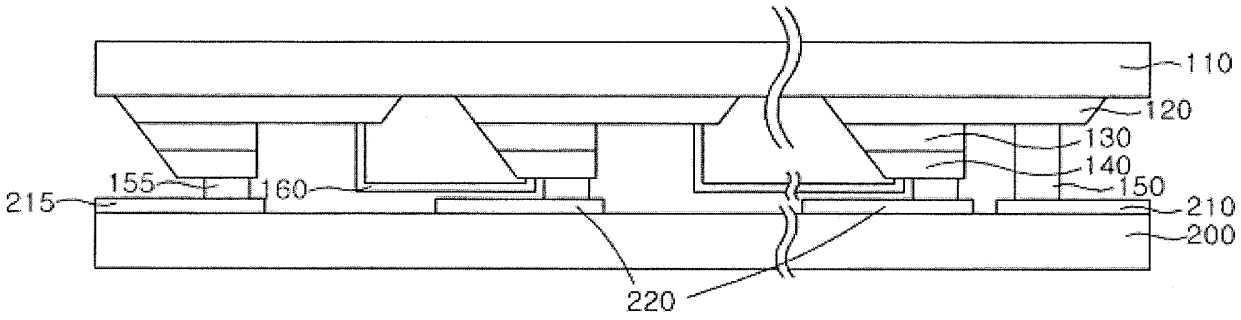


FIG. 29

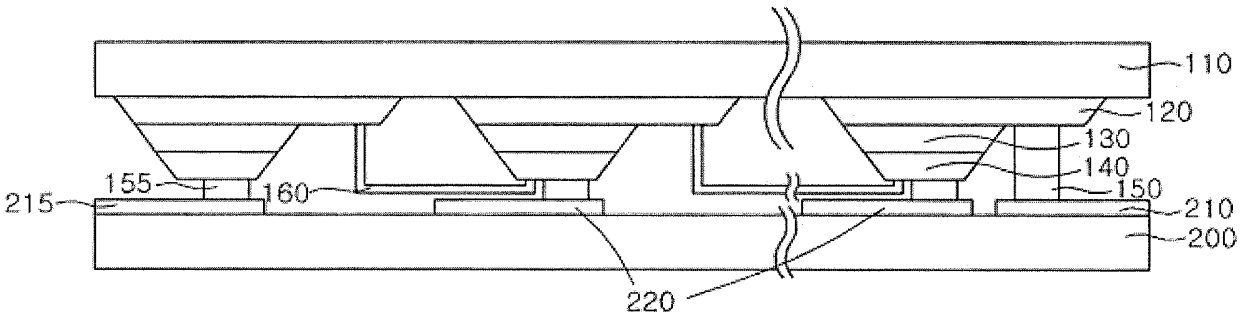


FIG. 30

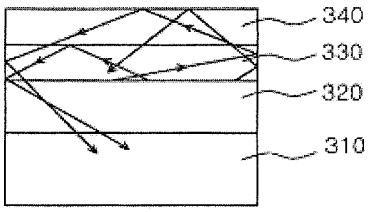
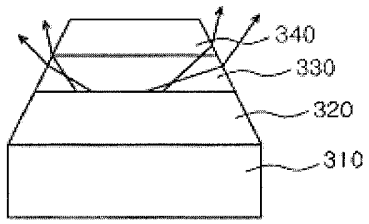


FIG. 31



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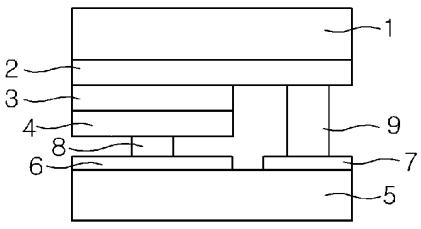
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(54) Title: LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME



(57) Abstract: The present invention relates to a light emitting device and a method of manufacturing the light emitting device. According to the present invention, the light emitting device comprises a substrate, an N-type semiconductor layer formed on the substrate, and a P-type semiconductor layer formed on the N-type semiconductor layer, wherein a side surface including the N-type or P-type semiconductor layer has a slope of 20 to 80°from a horizontal plane. Further, the present invention provides a light emitting device comprising a substrate formed with a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on the N-type semiconductor layer, and a submount substrate flip-chip bonded onto the substrate, wherein the N-type semiconductor layer of one light emitting cell and the P-type semi¬ conductor layer of another adjacent light emitting cell are connected to each other, and a side surface including at least the P-type semiconductor layer of the light emitting cell has a slope of 20 to 80°from a horizontal plane. Further, the present invention provides a method of manu¬ facturing the light emitting device. Accordingly, there is an advantage in that the characteristics of a light emitting device such as luminous efficiency, external quantum efficiency and extraction efficiency are enhanced and the reliability is secured such that light with high luminous intensity and brightness can be emitted.

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Description

LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME

Technical Field

[1] The present invention relates to a light emitting device and a method of manufacturing the same. More particularly, the present invention relates to a nitride based semiconductor light emitting device with enhanced luminous efficiency and brightness and a method of manufacturing the light emitting device.

Background Art

[2] A light emitting device refers to an element in which minority carriers (electrons or holes) injected using a p-n junction structure of a semiconductor are produced and certain light is emitted due to recombination of the carriers. A light emitting source is formed from any one or combination of compound semiconductor materials such as GaAs, AlGaAs, GaN, InGaN and AlGaInP, so that a variety of colors can be implemented. For example, a red light emitting device may be formed from GaAsP or the like; a green light emitting device may be formed from GaP, InGaN or the like; a blue light emitting device may be formed using an InGaN/GaN double hetero structure; and a UV light emitting device may be formed using an AlGaN/GaN or AlGaN/AlGaN structure.

[3] In particular, GaN has a direct bandgap of 3.4eV at a normal temperature and a direct energy bandgap of 1.9eV (InN) to 3.4eV (GaN) or 6.2eV (AlN) by combining with a substance such as InN or AlN. Thus, GaN is a substance with great applicability to an optical element due to its broad wavelength range from visible light to ultraviolet light. Since the wavelength can be adjusted in such a manner, full-color implementation can be made by means of red, green and blue light emitting devices with a short wavelength range, so that the applicability to a general illumination market as well as a display device market is expected to be greatly increased.

[4] Light emitting devices have characteristics of lower power consumption, longer lifespan, better installation in a narrow space and stronger resistance against vibration as compared with existing bulbs or fluorescent lamps. Since the light emitting devices are used as display devices and backlights and have superior characteristics in view of the reduction in power consumption and the durability, many studies for applying the light emitting devices to a general illumination field have been recently conducted. In the future, their applicability is expected to extend to a backlight of a large-sized LCD-TV, a vehicle headlight and general illumination. To this end, it is necessary to improve luminous efficiency of light emitting devices, solve a heat dissipation

problem, and achieve high brightness and output of the light emitting devices.

[5] Many techniques for enhancing the performance of light emitting devices have been currently developed. There are various indexes indicating the performance of light emitting devices, such as luminous efficiency (lm/W), internal quantum efficiency (%), external quantum efficiency (%) and extraction efficiency (%). The extraction efficiency is determined as a ratio of electrons injected into the light emitting device to photons emitted to the outside of the light emitting device. That is, the light emitting device becomes bright as the extraction efficiency becomes high. Since the extraction efficiency of the light emitting device is much influenced by the shape and surface pattern of a chip, the structure of a chip and a packaging type, careful attention should be paid when designing the light emitting device.

[6] Fig. 1 is a sectional view showing a conventional light emitting device with a horizontal structure.

[7] Referring to Fig. 1, the light emitting device comprises a substrate 1, an N-type semiconductor layer 2 formed on the substrate 1, an active layer 3 formed on a portion of the N-type semiconductor layer 2 and a P-type semiconductor layer 4. That is, after the N-type semiconductor layer 2, the active layer 3 and the P-type semiconductor layer 4 have been sequentially formed on the substrate 1, predetermined regions of the P-type semiconductor layer 4 and the active layer 3 are etched to expose a portion of the N-type semiconductor layer 2. Then, a predetermined voltage is applied to top surfaces of the exposed N-type semiconductor layer 2 and the P-type semiconductor layer 4.

[8] Fig. 2 is a sectional view showing a conventional light emitting device with a flip chip structure.

[9] Referring to Fig. 2, the light emitting device comprises an N-type semiconductor layer 2, an active layer 3 and a P-type semiconductor layer 4, which are sequentially formed on a base substrate 1. The light emitting device further comprises a submount substrate 5 onto which the base substrate 1 is flip-chip bonded using metal bumps 8 and 9. To this end, the N-type semiconductor layer 2, the active layer 3 and the P-type semiconductor layer 4 are sequentially formed on the predetermined substrate 1, and portions of the P-type semiconductor layer 4 and the active layer 3 are etched to expose the N-type semiconductor layer 2 such that a light emitting cell can be formed. Further, the additional submount substrate 5 is prepared to form first and second electrodes 6 and 7 thereon, and the P-type and N-type metal bumps 8 and 9 are then formed on the first and second electrodes 6 and 7, respectively. Thereafter, the light emitting cell is bonded with the submount substrate 5 such that P and N electrodes of the light emitting cell are bonded with the P-type and N-type metal bumps 8 and 9, respectively, to fabricate a light emitting device. Since such a conventional light emitting

device with a flip chip structure has high heat dissipation efficiency and hardly has shield of light, there is an advantage in that its light efficiency is increased by 50% or more as compared with a conventional light emitting device. Further, since a gold wire for driving a light emitting device is not necessary, many applications to a variety of small-sized packages can be considered.

[10] Light produced from a light emitting layer of a light emitting device is emitted from all the surfaces of a chip, and light extraction efficiency is generally determined by a critical angle of light. However, when the conventional light emitting device is etched to expose an N-type semiconductor layer, side surfaces of the P-type semiconductor layer and the active layer are vertically processed such that a portion of light produced within the light emitting device is totally reflected on the etched surface that is processed vertically from a horizontal plane. Then, a considerable amount of light to be totally reflected is not emitted to the outside but dissipated within the light emitting device due to the internal reflection. That is, there is a problem in that luminous efficiency in which electric energy is converted into light energy and the light is then emitted to the outside of a light emitting device is low.

Disclosure of Invention

Technical Problem

[11] The present invention is conceived to solve the aforementioned problems. Accordingly, an object of the present invention is to provide a light emitting device for emitting light with high luminous intensity and brightness by enhancing characteristics of luminous efficiency, external quantum efficiency, extraction efficiency and the like and improving reliability, and a method of manufacturing the light emitting device.

Technical Solution

[12] According to an aspect of the present invention for achieving the objects, there is provided a light emitting device, comprising a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on a portion of the N-type semiconductor layer on a substrate. The N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell may be connected to each other, and a side surface including the N-type or P-type semiconductor layer of the light emitting cell has a slope of 20 to 80°from a horizontal plane. The light emitting device may further comprise a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell, a transparent electrode layer on the P-type semiconductor layer, and P-type and N-type ohmic metal layers containing Cr or Au on the P-type and N-type semiconductor layers, respectively.

[13] According to another aspect of the present invention, there is provided a light

emitting device comprising a substrate formed with a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on the N-type semiconductor layer and a submount substrate flip-chip bonded onto the substrate. Preferably, the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including at least the P-type semiconductor layer of the light emitting cell has a slope of 20 to 80°from a horizontal plane. The light emitting device may further comprise a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

[14] According to further aspect of the present invention, there is provided a method of manufacturing a light emitting device, comprising the steps of sequentially forming N-type and P-type semiconductor layers on a substrate; forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; and removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern.

[15] According to still further aspect of the present invention, there is a method of manufacturing a light emitting device comprising the steps of removing a portion of the N-type semiconductor layer exposed due to the removal of the P-type semiconductor layer to form a plurality of light emitting cells; and connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire.

[16] According to still further aspect of the present invention, there is a method of manufacturing a light emitting device comprising the step of flip-chip bonding the substrate onto an additional submount substrate after the step of removing the P-type semiconductor layer and the etching mask pattern. The method of manufacturing a light emitting device may further comprise the steps of removing a portion of the N-type semiconductor layer exposed through the removal of the P-type semiconductor layer to form a plurality of light emitting cell; and connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire, after the step of removing the P-type semiconductor layer and the etching mask pattern.

[17] The step of forming the plurality of light emitting cells may comprise the steps of forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; removing the N-type and P-type semiconductor layers exposed through the etching mask pattern to form a plurality of light emitting cells; and removing the etching mask pattern.

[18] The N type semiconductor layer of one light emitting cell and the P type semiconductor layer of another adjacent light emitting cell may be connected with the conductive wire through a bridge or step coverage process.

[19] A photoresist with a thickness of 3 to 50□ may be used in the step of forming the etching mask pattern. The step of forming the etching mask pattern may comprise the steps of: applying the photoresist onto the P-type semiconductor layer; light exposing the photoresist in accordance with a predetermined mask pattern; and developing the light-exposed photoresist without a baking process after the light exposure. The step of forming the etching mask pattern may comprise the steps of: applying the photoresist onto the P-type semiconductor layer; light exposing the photoresist in accordance with a predetermined mask pattern; hard baking the light-exposed photoresist at a temperature of 100 to 140°C; and developing the hard-baked photoresist.

[20] After the step of removing the P-type semiconductor layer and the etching mask pattern, the method of manufacturing a light emitting device may further comprise the steps of removing a rear surface of the substrate at a certain thickness; and depositing Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof onto the rear surface of the substrate.

[21]

[22]

Advantageous Effects

[23] In a light emitting device and a method of manufacturing the same according to the present invention, light produced from a side surface of a semiconductor layer, which is not perpendicular to but inclined at a predetermined slop from a horizontal plane, is not totally reflected but emitted to the outside of the light emitting device. Therefore, more enhanced characteristics of light extraction efficiency, external quantum efficiency, luminous efficiency or the like can be obtained. Further, a light emitting device of the present invention emits light with high luminous intensity and brightness and can be applied to a variety of products in which a superior light characteristic is necessary.

Brief Description of the Drawings

[24] The above and other objects, features and advantages of the present invention will become apparent from the following description of preferred embodiments given in conjunction with the accompanying drawings, in which:

[25] Figs. 1 and 2 are sectional views showing conventional light emitting devices, respectively;

[26] Fig. 3 is a conceptual sectional view illustrating a light emitting device with a hori zontal structure according to the present invention;

[27] Figs. 4 and 5 are sectional views illustrating a process of manufacturing a light

emitting device according to a first embodiment of the present invention;

[28] Figs. 6 to 9 are sectional views illustrating a process of manufacturing a light emitting device according to a second embodiment of the present invention;

[29] Figs. 10 to 13 are sectional views illustrating a process of manufacturing a light emitting device according to a third embodiment of the present invention;

[30] Figs. 14 to 17 are sectional views illustrating a process of manufacturing a light emitting device according to a fourth embodiment of the present invention;

[31] Fig. 18 is a conceptual sectional view illustrating a light emitting device with a flip chip structure according to the present invention;

[32] Figs. 19 to 23 are sectional views illustrating a process of manufacturing a light emitting device according to a fifth embodiment of the present invention;

[33] Figs. 24 to 28 are sectional views illustrating a process of manufacturing a light emitting device according to a sixth embodiment of the present invention;

[34] Fig. 29 is a sectional view showing a seventh embodiment according to the present invention; and

[35] Figs. 30 and 31 are conceptual sectional views illustrating a difference between effects of the light emitting devices according to the prior art and the present invention.

Best Mode for Carrying Out the Invention

[36] Hereinafter, a light emitting device and a manufacturing method thereof according to the present invention will be described in detail with reference to the accompanying drawings. However, the present invention is not limited to the embodiments set forth herein but can be implemented in different forms. Rather, the preferred embodiments are merely provided to allow the present invention to be completely described herein and to fully convey the scope of the invention to those skilled in the art.

[37] Fig. 3 is a conceptual sectional view illustrating a light emitting device with a horizontal structure according to the present invention.

[38] Referring to Fig. 3, the light emitting device comprises a substrate 10, and an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40, which are sequentially formed on the substrate 10. Each of side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 has a slope of 80 to 20° from a horizontal plane such that a critical angle of light can be changed by such surfaces and light can be easily extracted. Therefore, luminous efficiency of a light emitting device can be improved.

[39] Figs. 4 and 5 are sectional views illustrating a process of manufacturing a light emitting device according to a first embodiment of the present invention.

[40] Referring to Fig. 4, an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40 are sequentially formed on a substrate 10.

[41] The substrate 10 refers to a general wafer used for fabricating a light emitting device and is made of at least any one of Al_2O_3, SiC, ZnO, Si, GaAs, GaP, $LiAl_2O_3$, BN, AlN and GaN. In this embodiment, a crystal growth substrate made of sapphire is used.

[42] A buffer layer (not shown) may be further formed on the substrate 10 to reduce lattice mismatch between the substrate 10 and the subsequent layers upon growth of crystals. The buffer layer may contain GaN or AlN that is a semiconductor material.

[43] The N-type semiconductor layer 20 is a layer in which electrons are produced and is preferably made from GaN doped with N-type impurities. However, the N-type semiconductor layer 20 is not limited thereto but may use a material layer having a variety of semiconductor properties. The N-type semiconductor layer 20 including N-type $Al_xGa_{1-x}N(0\leq x\leq 1)$ is formed in this embodiment. Further, the P-type semiconductor layer 40 is a layer in which holes are produced and is preferably made from GaN doped with P-type impurities. However, the P-type semiconductor layer 40 is not limited thereto but may use a material layer with a variety of semiconductor properties. The P-type semiconductor layer 40 including P-type $Al_xGa_{1-x}N(0\leq x\leq 1)$ is formed in this embodiment. Moreover, InGaN may be used as the semiconductor layer. Further, each of the N-type and P-type semiconductor layers 20 and 40 may be formed as a multiple layer.

[44] The active layer 30 has a predetermined bandgap and is a region where a quantum well is formed so that electrons and holes are recombined. The active layer 30 may contain InGaN. The wavelength of light emitted through the combination of electrons and holes varies according to the kind of a material constituting the active layer 30. Therefore, it is preferred that a semiconductor material contained in the active layer 30 be controlled depending on a target wavelength.

[45] The aforementioned material layers are formed through a variety of deposition and growth methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like.

[46] Thereafter, portions of the P-type semiconductor layer 40 and the active layer 30 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 20. An etching mask pattern is formed on the P-type semiconductor layer 40, and the P-type semiconductor layer 40 and the active layer 30 are then removed through a dry or wet etching process to expose the N-type semiconductor layer 20.

[47] Generally, in order to perform the etching process, a photoresist has been applied onto a top surface of the P-type semiconductor layer 40 at a thickness of 1 to 2□, and

then soft-baked at a temperature of 80 to 90°C is performed. Next, an exposure process in which light in a UV range is irradiated through a predetermined photo mask to transfer a pattern formed on the mask to the applied photoresist is executed. Thereafter, the photoresist is hard-baked at a temperature of 100 to 120°C, and a developing process in which the photoresist at a portion with relatively weak combination through the exposure process is melted using a solvent is executed. A predetermined etching mask pattern is formed on the P-type semiconductor layer 40 through the above process.

[48] However, in this embodiment, the photoresist is applied at a thickness of 3 to 50□ which is thicker as compared with the prior art when the etching mask pattern is formed, and the exposure process is performed after the soft-baking. Next, if the photoresist is directly developed without the hard-baking, a developed side surface of the remaining photoresist is formed into an inclined surface not perpendicular (90°) to but inclined at a predetermined slope from a horizontal plane. Subsequently, if exposed regions of the P-type semiconductor layer 40, the active layer 30 and the pre-determined N-type semiconductor layer 20 are etched using the etching mask pattern with such a slope of the side surface, the side surfaces of the etched P-type semi-conductor layer 40, active layer 30 and N-type semiconductor layer 20 can be similarly formed into an inclined surface not perpendicular (90°) to but inclined at a pre-determined slope from the horizontal plane.

[49] That is, after the photoresist has been applied at a thickness of 3 to 50□ on the P-type semiconductor layer 40 of Fig. 4 and light-exposed, a developed etching mask pattern is immediately formed without the hard-baking. The P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer 20. A portion of the exposed N-type semiconductor layer 20 may be further removed. Thereafter, if the etching mask pattern is removed, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 are not per-pendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured as shown in Fig. 5.

[50] Alternatively, after a photoresist has been applied at a thickness of 3 to 50□ on the P-type semiconductor layer 40 of Fig. 4 and light-exposed, hard-baking may be performed. In such a case, if the photoresist is hard-baked at a temperature of 100 to 140°C and then developed, the side surface of the developed photoresist may be etched to have a slope of 80 to 20° from a horizontal plane. For example, in a case where the hard-baking is performed at a temperature of 100°C, an etching mask pattern with a slope of about 80° from the horizontal plane can be obtained, and the side surfaces of

the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 can have a slope of about 80° from the horizontal plane using the etching mask pattern. Further, in a case where the hard-baking is performed at a temperature of 140℃, an etching mask pattern with a slope of about 20° from the horizontal plane can be obtained, and the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 can have a slope of about 20° from the horizontal plane using the etching mask pattern.

[51] The etching mask pattern, which the photoresist with a thickness of 3 to 50□ has been light-exposed and hard-baked at a temperature of 100 to 140℃ and then developed in such a manner, can be used such that the side surfaces of the etched the P-type semiconductor layer 40, active layer 30 and predetermined N-type semiconductor layer 20 have a slope of 80 to 20° from a horizontal plane similarly to the etching mask pattern. Then, light produced within a light emitting layer is not totally reflected on the etched side surface with a variety of slopes but emitted to the outside of a light emitting device.

[52] A transparent electrode layer may be further formed on the P-type semiconductor layer 40 to reduce resistance of the P-type semiconductor layer 40 and enhancing transmittance of light, and an additional ohmic metal layer may be further formed on the P-type semiconductor layer 40 or the exposed N-type semiconductor layer 20 to facilitate current supply. The transparent electrode layer may be made of ITO (Indium Tin Oxide), ZnO or a transparent conductive metal, and the ohmic metal layer may be made of Cr or Au. Further, for the application of voltage, a P-type electrode may be further formed on the P-type semiconductor layer 40 and an N-type electrode may be further formed on the N-type semiconductor layer 20.

[53] Further, in order to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10.

[54] As can be seen from this figure, a plurality of light emitting devices may be fabricated on a single substrate 10, which is cut into the individual light emitting devices. At this time, portions A shown in Fig. 5 are cutting portions used for individually cutting the plurality of light emitting devices.

[55] Accordingly, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 is not perpendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured.

[56] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto.

Various processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes.

[57] Figs. 6 to 7 are sectional views illustrating a process of manufacturing a light emitting device according to a second embodiment of the present invention.

[58] The second embodiment of the present invention is almost the same as the first embodiment. In the second embodiment, however, there is provided a light emitting device in which a plurality of light emitting cells are connected in series, parallel or series-parallel in a wafer level to reduce the size of the device, and they can be driven at proper voltage and current to be used for illustration purpose and can also be driven even with an AC power source. Descriptions overlapping with the previous embodiment will be omitted herein.

[59] Referring to Fig. 6, an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40 are sequentially formed on a substrate 10 through various deposition methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like. A buffer layer may be further formed on the substrate 10 to reduce lattice mismatch between the substrate 10 and the subsequent layers upon growth of crystals.

[60] Thereafter, portions of the P-type semiconductor layer 40 and the active layer 30 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 20. That is, after the photoresist has been applied at a thickness of 3 to 50□ on the P-type semiconductor layer 40 of Fig. 6 and light-exposed, it is developed without hard-baking to form an etching mask pattern. The P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer 20. A portion of the exposed N-type semiconductor layer 20 may be further removed. Thereafter, if the etching mask pattern is removed, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured as shown in Fig. 7.

[61] Alternatively, after a photoresist has been applied in a thickness of 3 to 50□ on the P-type semiconductor layer 40 of Fig. 6 and light-exposed, it is hard-baked at a temperature of 100 to 140°C and developed such that an etching mask pattern can be formed. After the P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, have been etched, the etching mask pattern is removed such that the side surfaces of the etched P-type semiconductor layer 40 and active layer 30 can have a variety of slopes of 80 to 20°.

[62] Next, in order to form a plurality of light emitting cells on the substrate 10, predetermined regions of the exposed N-type semiconductor layer 20 are removed such that a portion of the substrate 10 can be exposed. To this end, a predetermined mask pattern is formed on all the portions except the predetermined regions where the substrate 10 will be exposed, and regions of the N-type semiconductor layer 20 that are exposed through the mask pattern are then etched such that the plurality of light emitting cells can be electrically isolated from one another as shown in Fig. 8. At this time, the mask pattern whose side surface is inclined through the aforementioned process is formed and then used to etch the exposed N-type semiconductor layer 20 such that the side surface of the N-type semiconductor layer 20 in which the plurality of light emitting cells are separated from one another is not perpendicular to but inclined at a predetermined slope from a horizontal plane.

[63] Referring to Fig. 9, the N-type semiconductor layer 20 of a light emitting cell and the P-type semiconductor layer 40 of the adjacent light emitting cell are connected through a predetermined wiring process. That is, the exposed N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent light emitting cell are connected through a wire 60. At this time, the conductive wire 60 for electrically connecting the N-type and P-type semiconductor layers 20 and 40 are formed through a bridge process.

[64] The aforementioned bridge process is also called an air-bridge process. In the air-bridge process, a photosensitive liquid is applied between chips to be connected with each other through a photo process and developed to form a photoresist pattern, a material such as metal is first formed into a thin film on the photoresist pattern through a vacuum vapor deposition method or the like, and a conductive material containing gold (Au) is applied at a predetermined thickness onto the thin film through an electroplating, electroless plating or metal vapor deposition method. Thereafter, if the photoresist pattern is removed with a solution of a solvent or the like, a lower portion of the conductive material is completely removed, and thus, only the bridge-shaped conductive material is formed in a space between the adjacent light emitting cells.

[65] The wire 60 may be made of not only metal but also all kinds of conductive materials. It will be apparent that a silicone compound doped with impurities may be used.

[66] Further, in order to apply an external voltage to the light emitting device, a P-type bonding pad 50 is formed on the P-type semiconductor layer 40 of the light emitting cell positioned at one edge of the substrate 10 and an N-type bonding pad 55 is formed on the exposed N-type semiconductor layer 20 of the light emitting cell positioned at the other edge of the substrate 10.

[67] The aforementioned process of manufacturing a light emitting device according to

the present invention is merely a specific embodiment but is not limited thereto. Various modifications can be made or various material films can be further added. For example, in order to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10.

[68] Accordingly, a light emitting device in which the plurality of light emitting cells each of which side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at predetermined slope from a horizontal plane are connected with one another can be manufactured.

[69] Figs. 10 to 13 are sectional views illustrating a process of manufacturing a light emitting device according to a third embodiment of the present invention.

[70] The third embodiment is almost the same as the second embodiment. In the second embodiment, the N-type semiconductor layer 20 is first exposed and a portion of the exposed N-type semiconductor layer 20 is then removed to separate the light emitting cells from one another. In the third embodiment, however, a plurality of light emitting cells are first separated, and a portion of an N-type semiconductor layer 20 is then exposed. Descriptions overlapping with the previous embodiments will be omitted herein.

[71] Referring to Fig. 10, portions of an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40, which are sequentially formed on a substrate 10, are removed to form a plurality of light emitting cells. To this end, after a photoresist has been applied at a thickness of 3 to 50□ on the P-type semiconductor layer 40 and light-exposed, it is immediately developed without hard-baking such that an etching mask pattern can be formed. The portions of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor pattern 20, which are exposed through the etching mask pattern, and the etching mask pattern is removed to separate the light emitting cells from one another. Accordingly, a light emitting device in which entire side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at a pre-determined slope can be obtained as shown in this figure. Further, the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are removed using the etching mask pattern in which a photoresist is applied at a thickness of 3 to 50□ on the P-type semiconductor layer 40 and light-exposed and hard-baked at a temperature of 100 to 140°C and then developed. Accordingly, the entire side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 can be formed at various slopes of 80 to 20°.

[72] Thereafter, as shown in Fig. 11, portions of the P-type semiconductor layer 40 and the active layer 30 are removed to expose a portion of the N-type semiconductor layer 20 through a predetermined etching process.

[73] Referring to Fig. 12, the N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent light emitting cell are connected with each other through a bridge process.

[74] Further, in order to apply an external voltage to the light emitting device, a P-type bonding pad 50 is formed on the P-type semiconductor layer 40 of the light emitting cell positioned at one edge of the substrate 10 and an N-type bonding pad 55 is formed on the exposed N-type semiconductor layer 20 of the light emitting cell positioned at the other edge of the substrate 10.

[75] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment but is not limited thereto. Various modifications can be made and various material films may be further added. For example, in order to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10.

[76] Further, even in a case where the plurality of light emitting cells are separated by etching such that the side surfaces may have various slopes as shown in Fig. 10 and then etched to expose the N-type semiconductor layer 20, a light emitting device can be manufactured using the same etching process as described above. That is, as shown in Fig. 11, the side surfaces of the P-type semiconductor layer 40 and the active layer 30, which are etched to expose the N-type semiconductor layer 20, can be formed at various slopes.

[77] Accordingly, a light emitting device in which the plurality of light emitting cells each of which side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at predetermined slope from a horizontal plane are connected with one another can be manufactured.

[78] Figs. 14 to 17 are sectional views illustrating a process of manufacturing a light emitting device according to a fourth embodiment of the present invention.

[79] The fourth embodiment is almost the same as the third embodiment. In the third embodiment, a conductive wire for electrically connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell is formed through a bridge process. In the fourth embodiment, however, the conductive wire is formed through a step coverage process. Descriptions overlapping with the previous embodiments will be omitted herein.

[80] Referring to Fig. 14, even in a case where a plurality of light emitting cells are separated by etching such that the side surfaces may have various slopes and then etched to expose an N-type semiconductor layer 20 through the aforementioned process, the side surfaces of P-type semiconductor layer 40 and active layer 30, which are etched to expose the N-type semiconductor layer 20, are formed with various slopes. Further, in order to reduce the resistance of the P-type semiconductor layer 40 and enhance the transmittance of light, a transparent electrode layer 85 may be further formed on a top surface of the P-type semiconductor layer 40. Further, an additional ohmic metal layer 87 for facilitating the supply of current may be further formed on a top surface of the P-type semiconductor layer 40 or the exposed N-type semiconductor layer 20. The transparent electrode layer 85 may be made of ITO (Indium Tin Oxide), ZnO or a conductive transparent metal, and the ohmic metal layer 87 may be made of Cr or Au.

[81] Referring to Fig. 15, a continuous insulation layer 70 is formed on an entire surface of the substrate 10 with the plurality of light emitting cells formed thereon. The insulation layer 70 covers the side surfaces and top surfaces of the light emitting cells and the top surfaces of the substrate 10 between the adjacent light emitting cells. For example, the insulation layer 70 may be formed as a silicone oxide film using a CVD (Chemical Vapor Deposition) technique.

[82] Since the side surfaces of the light emitting cells are inclined, the insulation layer 70 can easily cover the side surfaces of the light emitting cells. Since the total thickness of the N-type semiconductor layer 20 and active layer 30 is small and spaces between the adjacent P-type semiconductor layers 40 are broad, the side surfaces of the P-type semiconductor layers 40 adjacent to the exposed regions of the N-type semiconductor layers 20 can be easily covered with the insulation layer 70.

[83] Referring to Fig. 16, an opening portion is formed on each of the exposed N-type and P-type semiconductor layers 20 and 40 of the light emitting cell by patterning the insulation layer 70 through a predetermined etching process. If the transparent electrode layer 85 and/or the ohmic metal layer 87 are formed as shown in this figure, the transparent electrode layer 85 and/or the ohmic metal layer 87 are exposed through the opening portion.

[84] Referring to Fig. 17, a wire 80 is formed on the insulation layer 70 with the opening portion. The wire 80 connects the N-type and P-type semiconductor layers 20 and 40 through the opening portion thereof. That is, the N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent the light emitting cell are electrically connected with the wire.

[85] The wire 80 may be formed using a plating technique. That is, after an etching mask pattern with an opening portion defining a region of the wire 80 has been formed on

the insulation layer 70 and a metal layer has been plated within the opening portion, the etching mask pattern is removed and thus the wire 80 can be formed.

[86] Further, the wire 80 may be formed using the CVD (Chemical Vapor Deposition) or PVD (Physical Vapor Deposition) technique. That is, a metal layer is formed using a vapor deposition technique such as electron beam deposition and then patterned using a photo and etching process, so that the wire 80 can be formed. Since the side surface of the light emitting cell is inclined, the metal layer is continuously formed on the upper side surface of the light emitting cell.

[87] The light emitting device in which the wire 80 is formed as described above has an advantage in that it is possible to prevent the wire 80 from being disconnected or shorted due to external pressure and also prevent conductive materials such as metal, which remains while the wire 80 is formed, from shorting the light emitting cell.

[88] Accordingly, a light emitting device in which the plurality of light emitting cells each of which side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at predetermined slope from a horizontal plane are connected with one another can be manufactured.

[89] As described above, the light emitting device according to the present invention is formed such that the side surfaces of the P-type semiconductor layer, the active layer and a portion of the N-type semiconductor layer are not perpendicular (90°) to but inclined at a predetermined slope from a horizontal plane. Therefore, luminous efficiency of the light emitting device of the present invention can be enhanced as compared with that of the conventional light emitting device. The reason is that a photon reflected on a flat surface in the prior art is not reflected on a surface with a different angle but emitted to the outside.

[90] Fig. 18 is a conceptual sectional view illustrating a light emitting device with a flip chip structure according to the present invention.

[91] Referring to Fig. 18, the light emitting device comprises a light emitting layer, i.e. an N-type semiconductor layer 120, an active layer 130 and a P-type semiconductor layer 140 sequentially formed on a base substrate 110. Further, the light emitting device comprises a submount substrate 200 onto which the base substrate 110 with the light emitting layer formed thereon is flip-chip bonded through metal bumps 150 and 155. A side surface of the light emitting layer comprising the P-type semiconductor layer 140, the active layer 130 and the N-type semiconductor layer 120 is inclined at a slope of 20 to 80° from the horizontal plane and a critical angle of light is changed due to the side surface such that the light can be easily extracted. Therefore, luminous efficiency of the light emitting device can be improved.

[92] Figs. 19 to 23 are sectional views illustrating a process of manufacturing a light

emitting device according to a fifth embodiment of the present invention.

[93] Referring to Fig. 19, an N-type semiconductor layer 120, an active layer 130 and a P-type semiconductor layer 140 are sequentially formed on a base substrate 110.

[94] The base substrate 110 refers to a general wafer used for fabricating a light emitting device is made of a transparent substrate such as Al_2O_3, ZnO and $LiAl_2O_3$. In this embodiment, a crystal growth substrate made of sapphire is used.

[95] The N-type semiconductor layer 120, the active layer 130 and the P-type semiconductor layer 140 are sequentially formed on the substrate 110 through various deposition methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like. A buffer layer may be further formed on the substrate 110 to reduce lattice mismatch between the substrate 110 and the subsequent layers upon growth of crystals. The aforementioned components are the same as those in the previous embodiments, and thus, descriptions overlapping with the foregoing components will be omitted herein.

[96] Thereafter, portions of the P-type semiconductor layer 140 and the active layer 130 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 120. This etching process is the same as that of the previous embodiments.

[97] That is, after a photoresist has been applied at a thickness of 3 to 50□ on the P-type semiconductor layer 140 of Fig. 19 and light-exposed, it is immediately developed without hard-baking to form an etching mask pattern. The P-type semiconductor 140 and the active layer 130, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer 120. Thereafter, if the etching mask pattern is removed, side surfaces of the P-type semiconductor layer 140 and the active layer 130 which are not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane can be obtained as shown in Fig. 20.

[98] Alternatively, after a photoresist has been applied at a thickness of 3 to 50□ on the P-type semiconductor layer 140 of Fig. 19 and light-exposed, it is hard-baked at a temperature of 100 to 140°C and then developed such that an etching mask pattern can be formed. After the P-type semiconductor layer 140 and the active layer 130, which are exposed through the etching mask pattern, have been etched, the etching mask pattern is removed such that the side surfaces of the etched P-type semiconductor layer 140 and active layer 130 can have a variety of slopes of 80 to 20°.

[99] A reflection layer for reflecting light may be further formed on a top surface of the P-type semiconductor layer 140, and an additional ohmic metal layer for facilitating

the supply of current may be further formed on a top surface of the P-type semiconductor layer 140 or the exposed N-type semiconductor layer 120. The ohmic metal layer may be made of Cr or Au.

[100] Further, P-type and N-type metal bumps 155 and 150 are formed on the P-type and N-type semiconductor layers 140 and 120, respectively, as shown in Fig. 21. Each of the P-type and N-type metal bumps 155 and 150 may be made of at least one material selected from the group consisting of Pb, Sn, Au, Ge, Cu, Bi, Cd, Zn, Ag, Ni, Ti and an alloy thereof. To this end, a photoresist is applied onto an entire structure and a photoresist pattern (not shown) through which portions of the P-type and N-type semiconductor layers 140 and 120 are exposed is formed through a photo-etching process using a predetermined mask. After a metal film has been deposited on the entire structure, metal film portions formed on regions other than regions on the P-type and N-type semiconductor layers 140 exposed through the photoresist pattern and the photoresist pattern are removed. Accordingly, the P-type and N-type metal bumps 155 and 150 are formed on the P-type and N-type semiconductor layers 140 and 120, respectively.

[101] Next, referring to Fig. 22, an additional submount substrate 200 is prepared to form P-type and N-type bonding pads 215 and 210 connected to the P-type and N-type metal bumps 155 and 150, respectively.

[102] At this time, various kinds of superior heat conductive substrates 200 are used as the submount substrate 200. That is, the submount substrate 200 may be made of SiC, Si, Ge, SiGe, AlN, metal or the like. In this embodiment, AlN with superior heat conductivity and insulation property is used. The present invention is not limited thereto, but a metallic material with superior heat and electric conductivity may be employed. In this case, an insulation or dielectric film is formed on the substrate 200 to sufficiently serve as an insulation. The dielectric film may be made of SiO2, MgO and SiN or an insulating material. Further, each of the P-type and N-type bonding pads 210 and 215 is made of a metal with superior electric conductivity. This is formed through a screen printing process or a deposition process using a predetermined mask pattern.

[103] Thereafter, the submount substrate 200 is flip-chip bonded onto the base substrate 110 with the light emitting layer formed thereon.

[104] Referring to Fig. 23, in the light emitting device of the present invention, the N-type and P-type metal bumps 150 and 155 formed on the top of the light emitting layer are bonded and connected with the N-type and P-type bonding pads 210 and 215 of the submount substrate 200, respectively. At this time, the bonding pads and metal bumps may be bonded using heat or ultrasonic waves or simultaneously using the heat and ultrasonic waves. The metal bumps 150 and 155 and the lower bonding pads 210 and 215 are connected through a variety of bonding methods.

[105] Moreover, the N-type and P-type metal bumps 150 and 155 are not formed on the top of the light emitting layer but may be formed on the submount substrate 200.

[106] As can be seen from this figure, a plurality of light emitting devices may be fabricated on a single substrate 10, which is cut into the individual light emitting devices. At this time, portions A shown in Fig. 23 are cutting portions used for individually cutting the plurality of light emitting devices.

[107] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto. Various processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes. For example, in the same process as the previous embodiments, the base substrate with the N-type semiconductor layer, the active layer and the P-type semiconductor layer sequentially formed thereon is prepared as shown in Fig. 19. Then, portions of the P-type semiconductor layer, the active layer and the N-type semiconductor layer are first removed to expose the substrate such that the plurality of light emitting devices can be individually isolated. At this time, the side surfaces of the P-type semiconductor layer, the active layer and the N-type semiconductor layer, which are etched through the aforementioned process, may be formed not to be perpendicular (90°) to but inclined at a predetermined slope.

[108] Accordingly, a light emitting device with a flip chip structure, in which the side surfaces of the P-type semiconductor layer, the active layer and a portion of the N-type semiconductor layer are not perpendicular (90°) to but inclined at the predetermined slope from the horizontal plane, can be manufactured.

[109] Figs. 24 to 28 are sectional views illustrating a process of manufacturing a light emitting device according to a sixth embodiment of the present invention.

[110] The sixth embodiment is almost the same as the fifth embodiment. In the sixth embodiment, however, there is provided a light emitting device with a flip chip structure, in which a plurality of light emitting cells are connected in series, parallel or series-parallel in a wafer level to reduce the size of the device, and they can be driven at proper voltage and current to be used for illumination purpose and can also be driven even with an AC power source. Descriptions overlapping with the previous embodiments will be omitted herein.

[111] Referring to Fig. 24, an N-type semiconductor layer 120, an active layer 130 and a P-type semiconductor layer 140 are sequentially formed on a base substrate 110 through various deposition methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like. A buffer layer may be further formed on the substrate 110

to reduce lattice mismatch between the substrate 110 and the subsequent layers upon growth of crystals.

[112] Thereafter, portions of the N-type semiconductor layer 120, the active layer 130 and the P-type semiconductor layer 140, which are sequentially formed on the base substrate 110, are removed to form a plurality of light emitting cells. To this end, after a photoresist has been applied at a thickness of 3 to 50□ on the P-type semiconductor layer 140 of Fig. 24 and light-exposed, it is immediately developed without hard-baking to form an etching mask pattern. The P-type semiconductor 140, the active layer 130 and the predetermined N-type semiconductor layer 120, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to separate the light emitting cells from one another. Next, if the etching mask pattern is removed, a light emitting device in which entire side surfaces of the etched P-type semiconductor layer 140, active layer 130 and N-type semiconductor layer 120 are not perpendicular (90°) to but inclined at a pre-determined slope from the horizontal plane can be obtained as shown in Fig. 25.

[113] Alternatively, after a photoresist has been applied at a thickness of 3 to 50□ on the P-type semiconductor layer 140 of Fig. 24 and light-exposed, it is hard-baked at a temperature of 100 to 140°C and developed such that an etching mask pattern can be formed. After the P-type semiconductor layer 140, the active layer 130 and the N-type semiconductor layer 120, which are exposed through the etching mask pattern, have been etched, the etching mask pattern is removed such that the side surfaces of the etched P-type semiconductor layer 140 and active layer 130 can be inclined at various slopes of 80 to 20°.

[114] Next, portions of the P-type semiconductor layer 140 and the active layer 130 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 120, as shown in Fig. 26. The exposed N-type semiconductor layer 120 of one light emitting cell and the P-type semiconductor layer 140 of another adjacent light emitting cell are connected with each other through a predetermined conductive wire. At this time, a bridge wire 160 is made of a conductive material, e.g. metal. It will be apparent that the bridge wire 160 may be made of a silicone compound doped with impurities. The bridge wire 160 is formed through a bridge process.

[115] Further, a plurality of metal bumps are formed on the top of the light emitting cells, and P-type and N-type metal bumps 155 and 150 are further formed on the P-type semiconductor layer 140 of the light emitting cell positioned at one edge of the substrate 110 and the N-type semiconductor layer 120 of the light emitting cell positioned the other edge of the substrate, respectively.

[116] Next, as shown in Fig. 27, an additional submount substrate 200 is prepared, on

which a plurality of bonding layers 220, a P-type bonding pad 215 positioned at one edge of the submount substrate 200 and an N-type bonding pad 210 positioned at the other edge of the submount substrate are formed.

[117] Thereafter, as can be shown in Fig. 28, the aforementioned base substrate 110 with the plurality of light emitting cells formed thereon is flip-chip bonded onto the submount substrate 200 to fabricate the light emitting device. The substrates are bonded with each other through the metal bumps 150 and 155 formed on the top of the light emitting cell and the bonding layers 220 formed on the submount substrate 200, respectively. The P-type bonding pad 215 positioned at one edge of the submount substrate 200 is connected to the P-type metal bump 155 of the light emitting cell positioned at one edge of the base substrate 110, whereas the N-type bonding pad 210 positioned at the other edge of the submount substrate 200 is connected to the N-type metal bump 150 of the light emitting cell positioned at the other edge of the base substrate 110.

[118] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto. Various processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes. For example, in this embodiment, the conductive wire for electrically connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell is formed through a bridge process, and the base substrate is then flip-chip bonded onto the submount substrate. However, the present invention is not limited thereto. That is, a conductive wire for electrically connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cells may be formed through a step coverage process which is the same as in the fourth embodiment. Further, an electrode layer may be formed on the submount substrate when the plurality of light emitting cells are flip-chip bonded onto the submount substrate such that the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are electrically connected through the metal bumps.

[119] Accordingly, a light emitting device in which a plurality of flip chip light emitting cells each having a side surface of a light emitting layer, which is not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane, are arrayed on the submount substrate can be manufactured. The light emitting cells may be connected in various ways, i.e. in series, parallel or series-parallel, depending on the desired purpose.

[120] Fig. 29 is a sectional view showing a seventh embodiment according to the present invention.

[121] The seventh embodiment is almost the same as the sixth embodiment. In this embodiment, even in a case where a plurality of light emitting cells are separated by etching such that the side surfaces may have slopes as shown in Fig. 25 and then etched to expose an N-type semiconductor layer, a light emitting device can be manufactured using the same etching process as the previous embodiment. That is, side surfaces of a P-type semiconductor layer 140 and an active layer 130 etched to expose an N-type semiconductor layer 120 are formed with various slopes, as shown in Fig. 29.

[122] Accordingly, a light emitting device in which a plurality of flip chip light emitting cells each having an entire side surface of a light emitting layer, which is not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane, are arrayed on the submount substrate can be manufactured. The light emitting cells may be connected in various ways, i.e. in series, parallel or series-parallel, depending on the desired purpose.

[123] As described above, the light emitting device with a flip chip structure according to the present invention is formed such that some side surfaces of a light emitting layer are not particular (90°) to but inclined at a predetermined slope from the horizontal plane. Therefore, luminous efficiency of the light emitting device of the present invention can be enhanced as compared with that of the conventional light emitting device. The reason is that a photon reflected on a flat surface in the prior art is not reflected on a surface with a different angle but emitted to the outside.

[124] Figs. 30 and 31 are conceptual sectional views illustrating a difference between effects of the light emitting devices according to the prior art and the present invention.

[125] The light efficiency of a light emitting device may be expressed as internal quantum efficiency and external quantum efficiency, and the internal quantum efficiency is determined in accordance with the design and quality of an active layer. The external quantum efficiency is determined in accordance with a degree where a photon produced in an active layer is emitted to the outside of a light emitting device. Referring to Fig. 30 in which a conventional light emitting device is shown, a side surface of a semiconductor layer is formed perpendicular to a horizontal plane. In such a case, some portions of photons are not penetrated through the side surface of the semiconductor layer but reflected thereon, and totally reflected light is not emitted to the outside but dissipated within the light emitting device. However, referring to Fig. 31 in which a light emitting device according to the present invention is shown, a side surface of a semiconductor layer is not perpendicular to but inclined at a predetermined slope from a horizontal plane. In such a case, the inclined side surface makes a critical angle of light change to help the light to be more easily extracted. Therefore, light generated in an active layer is not totally reflected but emitted to the outside of the

light emitting device such that external quantum efficiency can be markedly enhanced.

[126] Although the present invention has been described in detail in connection with the specific embodiments, it will be readily understood by those skilled in the art that various modifications and changes can be made thereto within the technical spirit and scope of the present invention. It is also apparent that the modifications and changes fall within the scope of the present invention defined by the appended claims.

[127]

[128]

Claims

[1] 1. A light emitting device, comprising:
a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on a portion of the N-type semiconductor layer on a substrate,
wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including the N-type or P-type semiconductor layer of the light emitting cell has a slope of 20 to 80°from a horizontal plane.

[2] 2. The light emitting device as claimed in claim 1, further comprising a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

[3] 3. The light emitting device as claimed in claim 1 or 2, further comprising a transparent electrode layer on the P-type semiconductor layer.

[4] 4. The light emitting device as claimed in claim 1 or 2, further comprising P-type and N-type ohmic metal layers containing Cr or Au on the P-type and N-type semiconductor layers, respectively.

[5] 5. A light emitting device, comprising:
a substrate formed with a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on the N-type semiconductor layer; and
a submount substrate flip-chip bonded onto the substrate,
wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including at least the P-type semiconductor layer of the light emitting cell has a slope of 20 to 80°from a horizontal plane.

[6] 6. The light emitting device as claimed in claim 5, further comprising a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

[7] 7. A method of manufacturing a light emitting device, comprising the steps of:
sequentially forming N-type and P-type semiconductor layers on a substrate;
forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; and
removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern.

[8] 8. The method as claimed in claim 7, further comprising the steps of:

removing a portion of the N-type semiconductor layer exposed through the removal of the P-type semiconductor layer to form a plurality of light emitting cells; and

connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire.

[9] 9. The method as claimed in claim 7, further comprising the step of flip-chip bonding the substrate onto an additional submount substrate after the step of removing the P-type semiconductor layer and the etching mask pattern.

[10] 10. The method as claimed in claim 9, further comprising the steps of:

removing a portion of the N-type semiconductor layer exposed due to the remova l of the P-type semiconductor layer to form a plurality of light emitting cell; and

connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire, after the step of removing the P-type semiconductor layer and the etching mask pattern.

[11] 11. The method as claimed in claim 8 or 10, wherein the step of forming the plurality of light emitting cells comprises the steps of:

forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer;

removing the N-type and P-type semiconductor layers exposed through the etching mask pattern to form a plurality of light emitting cells; and

removing the etching mask pattern.

[12] 12. The method as claimed in claim 8 or 10, wherein the N type semiconductor layer of one light emitting cell and the P type semiconductor layer of another adjacent light emitting cell are connected with the conductive wire through a bridge or step coverage process.

[13] 13. The method as claimed in any one of claims 7 to 10, wherein a photoresist with a thickness of 3 to 50□ is used in the step of forming the etching mask pattern.

[14] 14. The method as claimed in claim 13, wherein the step of forming the etching mask pattern comprises the steps of:

applying the photoresist onto the P-type semiconductor layer;

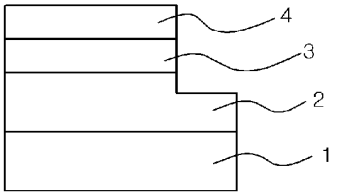
light exposing the photoresist in accordance with a predetermined mask pattern; and

developing the light-exposed photoresist without a baking process after the light exposure.

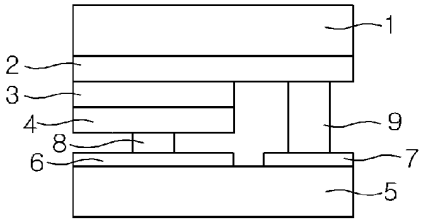
[15] 15. The method as claimed in claim 13, wherein the step of forming the etching mask pattern comprises the steps of:
applying the photoresist onto the P-type semiconductor layer;
light exposing the photoresist in accordance with a predetermined mask pattern;
hard baking the light-exposed photoresist at a temperature of 100 to 140°C; and
developing the hard-baked photoresist.

[16] 16. The method as claimed in claim 7 or 8, further comprising the steps of:
after the step of removing the P-type semiconductor layer and the etching mask pattern,
removing a rear surface of the substrate at a certain thickness; and
depositing Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof onto the rear surface of the substrate.

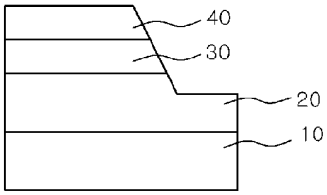
[Fig. 1]



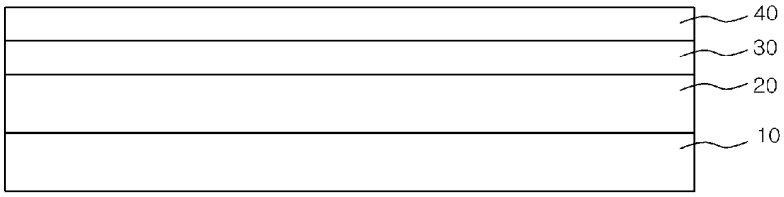
[Fig. 2]



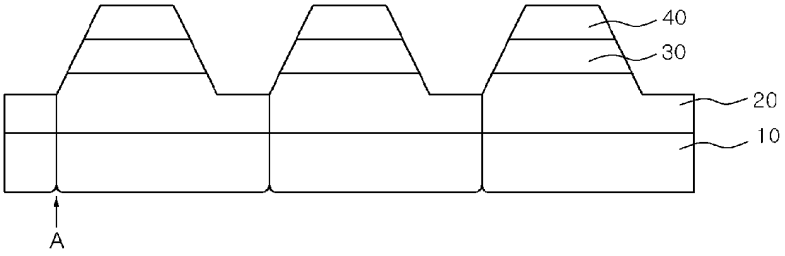
[Fig. 3]



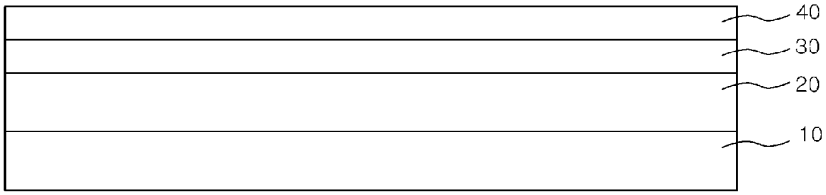
[Fig. 4]



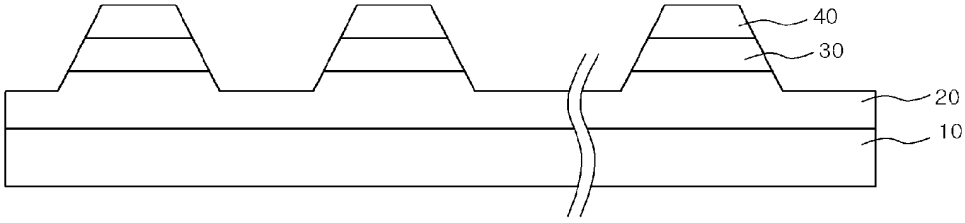
[Fig. 5]



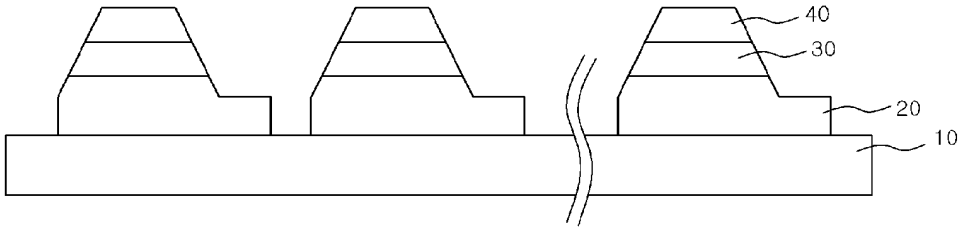
[Fig. 6]



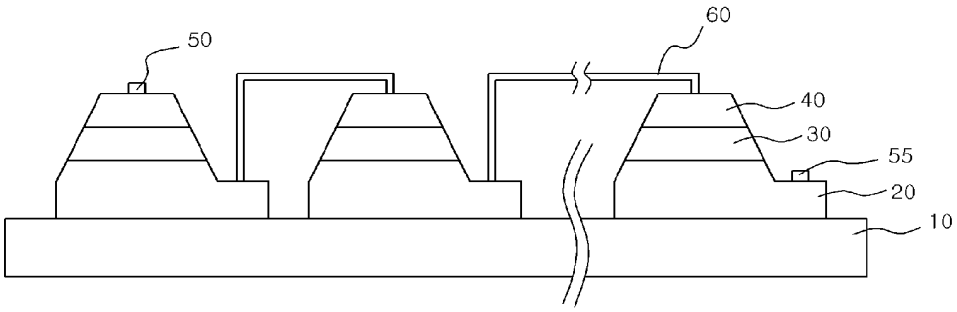
[Fig. 7]



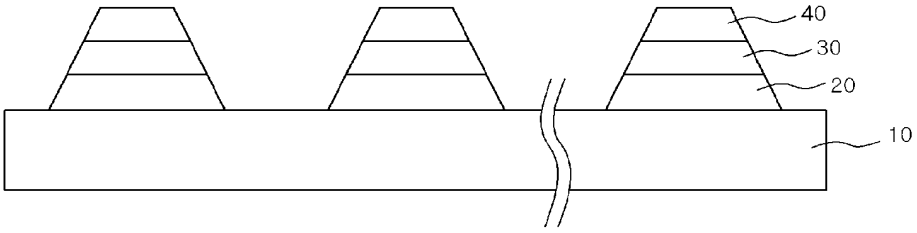
[Fig. 8]



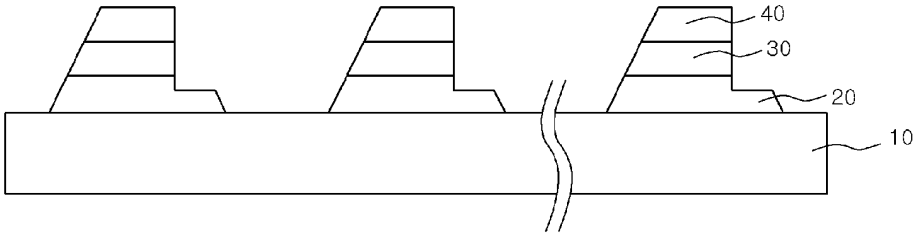
[Fig. 9]



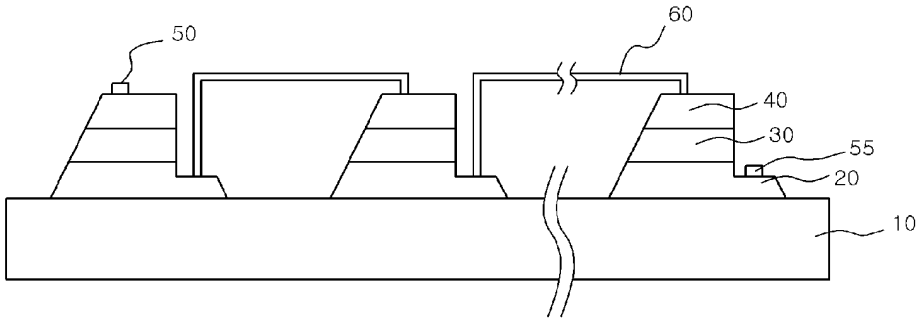
[Fig. 10]



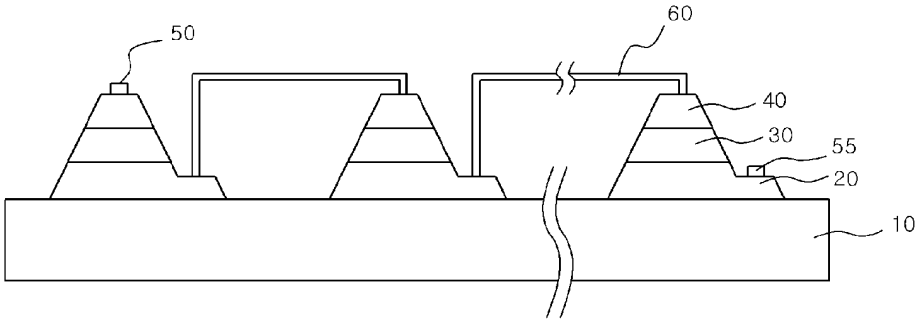
[Fig. 11]



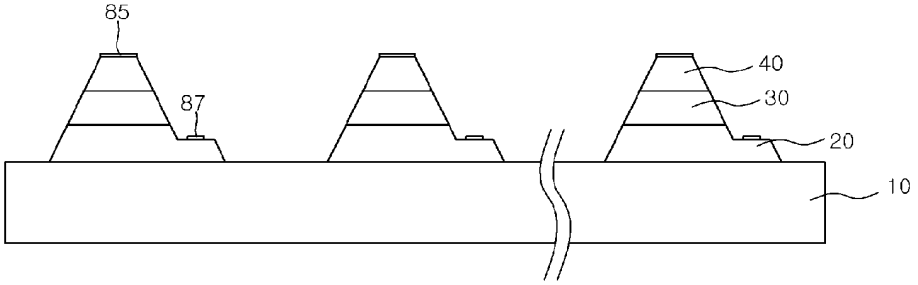
[Fig. 12]



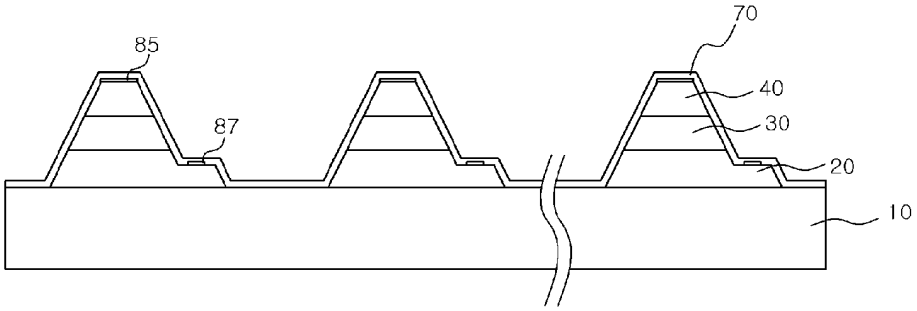
[Fig. 13]



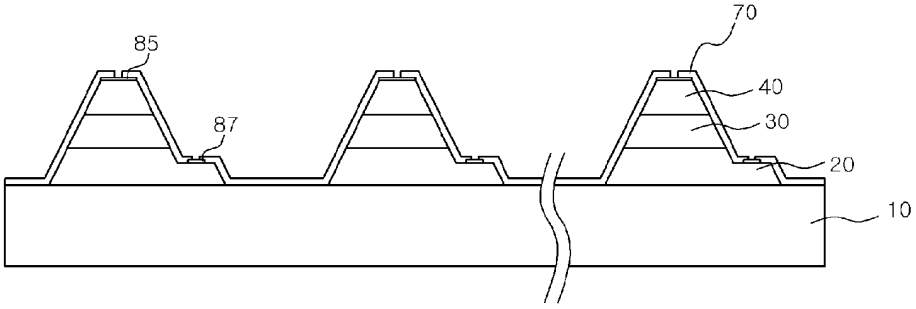
[Fig. 14]



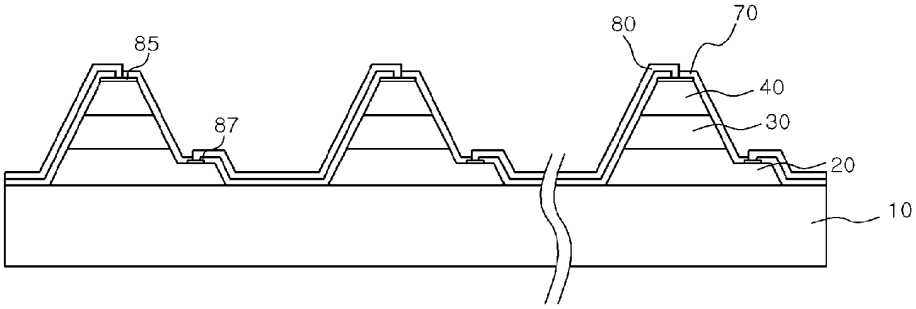
[Fig. 15]



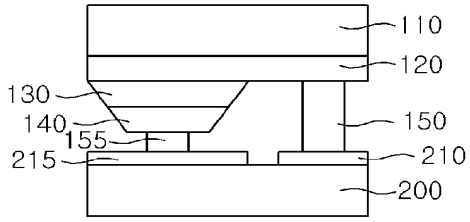
[Fig. 16]



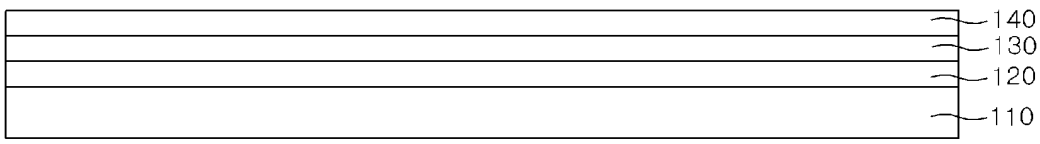
[Fig. 17]



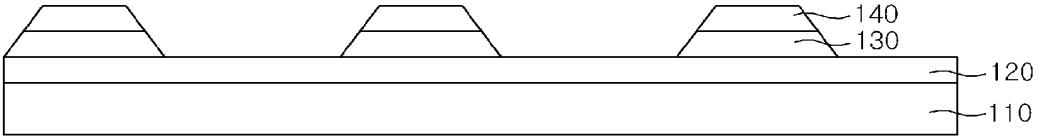
[Fig. 18]



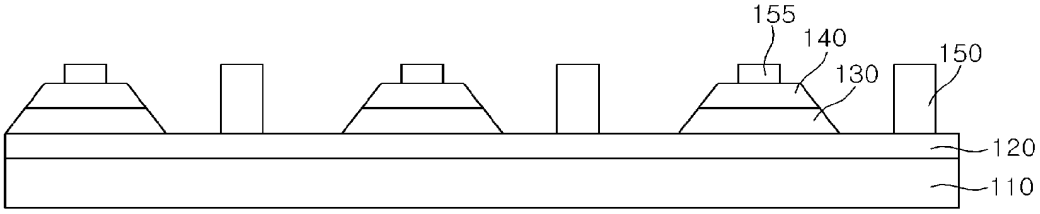
[Fig. 19]



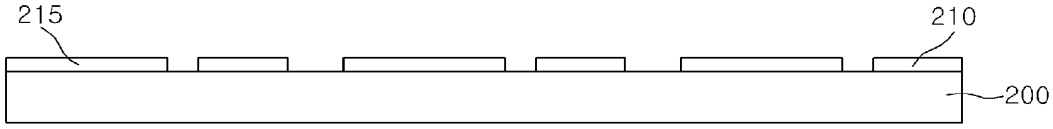
[Fig. 20]



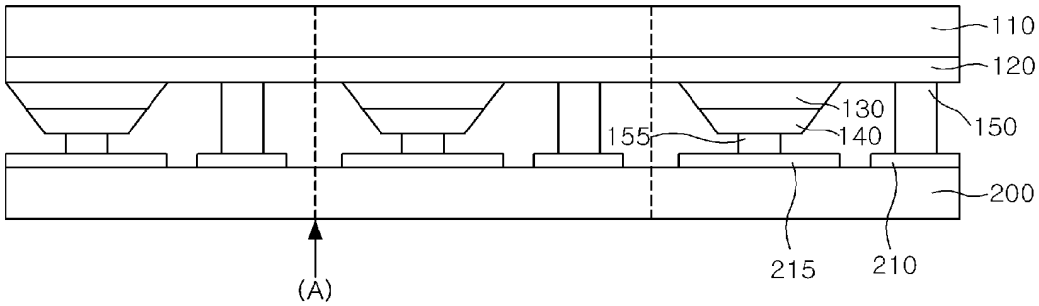
[Fig. 21]



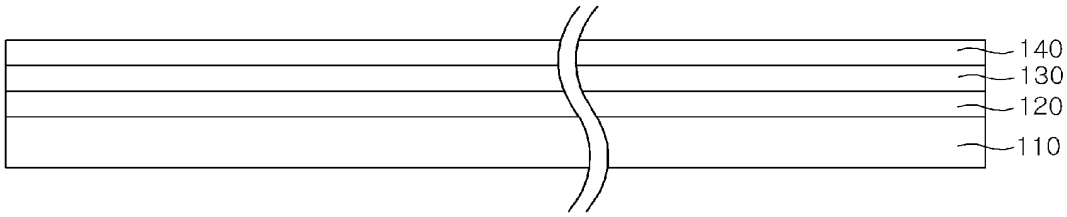
[Fig. 22]



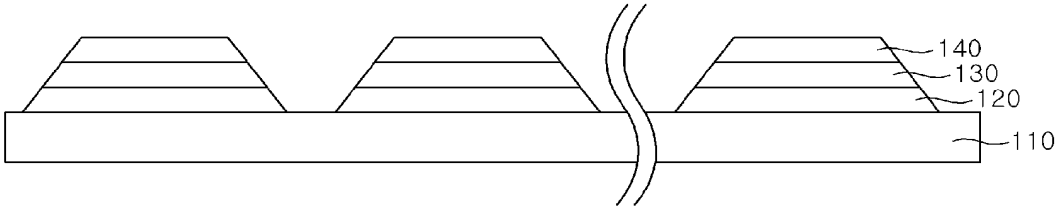
[Fig. 23]



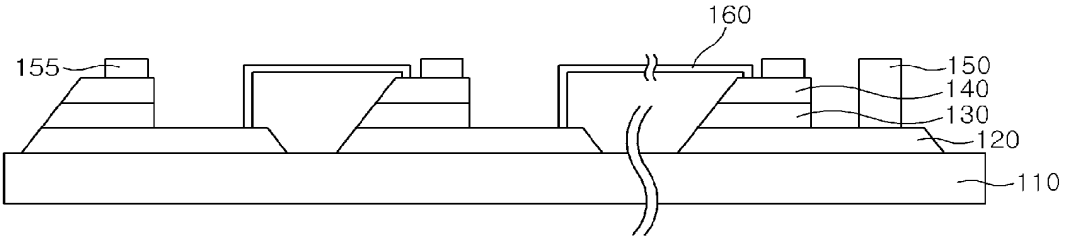
[Fig. 24]



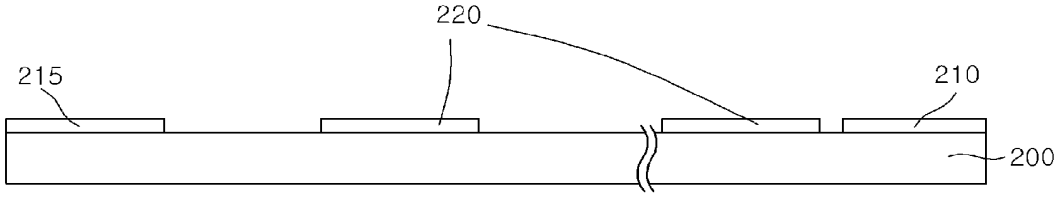
[Fig. 25]



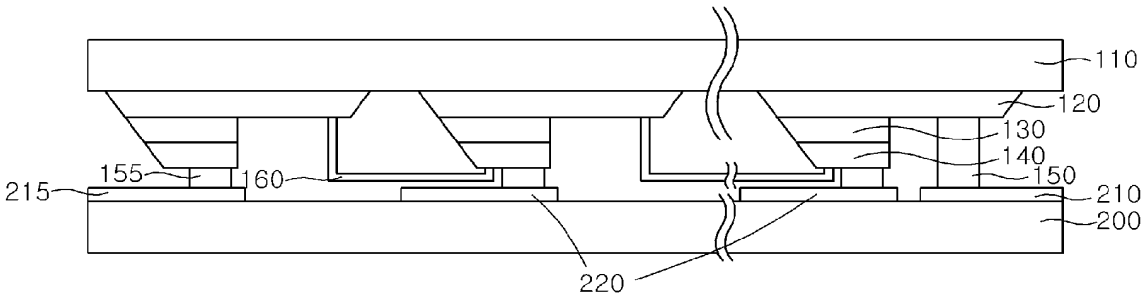
[Fig. 26]



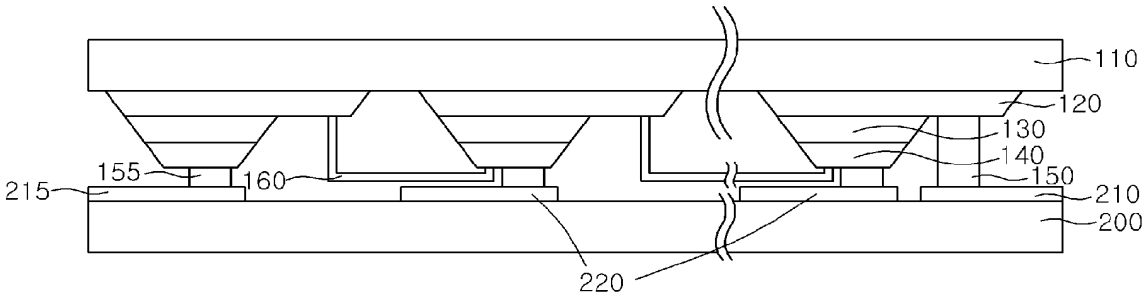
[Fig. 27]



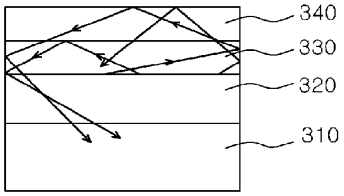
[Fig. 28]



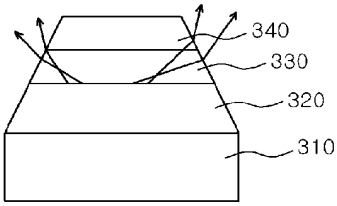
[Fig. 29]



[Fig. 30]



[Fig. 31]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2006/002427

A. CLASSIFICATION OF SUBJECT MATTER

H01L 33/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC8 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Japanese Utility models since 1975
Korean Patents and applications for inventions since 1975
Korean Utility models and applications since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKIPASS "light emitting diode, LED, semiconductor layer, luminous efficiency, Cr, Au, Slope"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	KR2003-52499(SAMSUNG ELECTRONICS CO., LTD) 27 JUN 2003 see the whole document, figures 1, 2, 3	1-16
Y	KR2004-5098(BiCHEL CO., LTD) 16 JAN 2004 see the whole document, figures 3, 4, 5, 6, 7	1-16
A	US06255129 B1(Highlink Technology Corporation) 03 JUL 2001 see the whole document, figures 1, 2, 3	1-16
A	US20040012958 A1(Hashimoto et al) 22 JAN 2004 see the whole document, figures 1, 2, 3, 4, 5, 6, 7	1-16

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☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
17 OCTOBER 2006 (17.10.2006)	**18 OCTOBER 2006 (18.10.2006)**
Name and mailing address of the ISA/KR Korean Intellectual Property Office 920 Dunsan-dong, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Authorized officer JUNG, BYEONG HONG Telephone No. 82-42-481-5752

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR2006/002427

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR2003-52499	27.06.2003	NONE	
KR2004-5098	16.01.2004	NONE	
US06255129	03.07.2001	DE10045149A1	04.04.2002
		US6255129BA	03.07.2001
US20040012958A1	22.01.2004	CN1220283C	21.09.2005
		CN1461498A	10.12.2003
		EP01398839A1	17.03.2004
		EP1398839A1	17.03.2004
		EP1398839A4	05.07.2006
		JP14319705	31.10.2002
		JP15168829	13.06.2003
		JP2002319705A2	31.10.2002
		JP2003168829A2	13.06.2003
		TW541724B	11.07.2003
		US2004012958A1	22.01.2004
		US2004012958AA	22.01.2004
		WO02089221A1	07.11.2002
		WO2002089221A1	07.11.2002

PTO/SB/08a (05-07)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	
	Filing Date	
	First Named Inventor	Jong-Lam Lee
	Art Unit	
	Examiner Name	
	Attorney Docket Number	3576-053

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	
	Filing Date	
	First Named Inventor	Jong-Lam Lee
	Art Unit	
	Examiner Name	
	Attorney Docket Number	3576-053

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
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CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

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☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Hosoon Lee/	Date (YYYY-MM-DD)	
Name/Print	Hosoon Lee	Registration Number	56737

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(19) KOREAN INTELLECTUAL PROPERTY OFFICE

KOREAN PATENT ABSTRACTS

(11)Publication number: 1020030052499 A
(43)Date of publication of application: 27.06.2003

(21)Application number: 1020010082484
(22)Date of filing: 21.12.2001

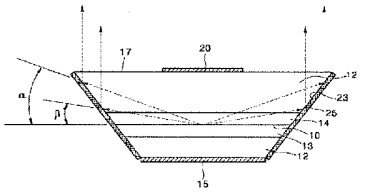
(51)Int. Cl H01L 33/00

(71)Applicant: SAMSUNG ELECTRONICS CO., LTD.
(72)Inventor: BAE, YU SEOK

(54) SEMICONDUCTOR LIGHT EMITTING DIODE

(57) Abstract:

PURPOSE: A semiconductor LED(Light Emitting Diode) is provided to be capable of controlling the angular spectrum of extracted light by using a diffracting optical element. CONSTITUTION: A semiconductor LED is provided with a P-type and N-type epitaxial layer(13,14) doped with holes and electrons, an active layer(10) located between the P-type and N-type epitaxial layer(13,14) for generating photons, a plurality of ohmic contact layers(15,20) located on the lower and upper portion of the semiconductor LED for coupling the electron and hole at the active layer(10) by supplying voltage, and a diffracting optical element(25) located at both inner sidewalls (23) or on the upper surface(17) of the semiconductor LED for extracting parallel light from the photons. Preferably, the inner sidewall(23) of the semiconductor LED has a predetermined slope.



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Legal Status
Date of request for an examination (20011221)
Notification date of refusal decision (00000000)
Final disposal of an application (rejection)
Date of final disposal of an application (20031229)
Patent registration number ( )
Date of registration (00000000)
Number of opposition against the grant of a patent ( )
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Number of trial against decision to refuse ( )
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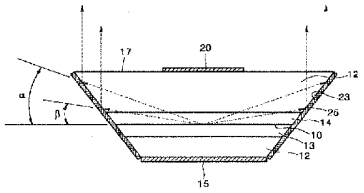
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이해영

심사청구 : 있음

(54) 반도체 발광 소자

요약

적출광의 각 스펙트럼 특성을 개선시킨 반도체 발광 소자가 개시되어 있다.

이 개시된 반도체 발광 소자는, 전자와 정공들이 도핑되어 있는 n형 및 p형 에피택시얼층; 광자들이 발생되는 활성층; 상기 활성층에서 상기 전자와 정공이 결합되도록 전압을 가하는 오믹 콘택트;를 포함하는 반도체 발광 소자에 있어서, 상기 광자들이 평행광으로 적출될 수 있도록 소자의 측벽 또는 상부면에 회절 광학 소자가 구비되는 것을 특징으로 한다.

본 발명의 반도체 발광 소자는 회절 광학 소자에 의해 적출광의 각 스펙트럼(angular spectrum)을 조절함으로써 광자가 평행광으로 방출되도록 할 수 있다.

대표도

도 2

명세서

도면의 간단한 설명

도 1은 종래의 반도체 발광 소자를 개략적으로 나타낸 도면이다.

도 2는 본 발명의 바람직한 일실시예에 따른 반도체 발광 소자를 나타낸 도면이다.

도 3은 본 발명의 다른 실시예에 따른 반도체 발광 소자를 나타낸 도면이다.

<도면 중 주요 부분에 대한 부호의 설명>

10...활성층, 13...p형 에피택시얼층

14...n형 에피택시얼층, 15,20...오믹 콘택트층

17...상부면, 23...측벽

25...회절 광학 소자

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 회절 광학 소자를 이용하여 적출광의 각 스펙트럼 특성을 개선시킨 반도체 발광 소자에 관한 것이다.

일반적으로 반도체 발광 소자(이하 LED라 함)의 발광 성능을 판별하는 기준 요소로는 발광효율이 있다. 이 발광효율은 내부 양자 효율(internal quantum efficiency, 적출 효율(extraction efficiency), 동작 전압(operation voltage)의 세가지 요소에 의해 주로 결정된다. 이 중 적출 효율은 LED를 통해 생성된 광자에 대한 칩 밖으로 빠져 나오는 양의 비율을 나타낸다. 이러한 적출 효율을 증대시키기 위한 구조가 미국 특허 US 6,229,160 B1에 개시되어 있다.

도 1을 참조하면, 이 개시된 발광 소자는 전자와 정공이 도핑된 n형 및 p형 에피택시얼 층(110)(112)과 이 층(110)(112)들 사이에 형성되고, 상기 n형 및 p형 에피택시얼 층(110)(112)으로부터 이동된 전자와 정공의 결합에 의해 광자들이 발생되는 활성층(111)과, 상기 활성층(111)으로부터 뛰어나오는 광자들이 통과되는 윈도우 층(113)을 포함한다. 또한, 상기 발광 소자의 상부면 및 하부면에 각각 제1 및 제2 전기오믹 콘택트(114)(115)가 구비된다. 상기 제1 전기오믹 콘택트(114)는 발광 소자의 상부면(117)의 일부에 형성되고 상기 상부면(117)을 통해 광자(I_1)가 적출된다. 여기서, 광자가 상기 상부면(117)을 통해 적출되도록 소정 각도로 기울어진 측벽(116)이 구비된다.

상기 구조에서 제1 및 제2 전기 오믹 콘택트(ohmic contact)(114)(115)에 각각 플러스와 마이너스 전압을 순방향으로 가하면 상기 n형 및 p형 에피택시얼 층(110)(112)에서 상기 활성층(111)으로 전자와 정공이 이동되고, 이 전자와 정공의 결합을 통하여 에너지 밴드 갭에 해당하는 에너지를 갖는 광자가 발생하게 된다. 상기 활성층(111)에서 발생된 광자들은 랜덤한 방향으로 발산되는 성질이 있으므로 여러번의 반사 끝에 결국 칩 외부로 방출되지 못하고 칩 내부에서 흡수되거나 소자의 상부면이 아닌 다른 방향(I2)으로 나가는 경우가 많다. 이와 같이 광자가 칩내부에서 흡수되는 것을 방지하여 칩 외부로 가능한 많은 수의 광자들을 탈출시킴으로써 적출 효율을 향상시키기 위해 상기 측벽(116)의 기울기 각도(δ)를 조절하고, 상기 윈도우층(113)의 두께를 조절하여 활성층(111)의 위치를 조절하는 방법 등을 사용한다.

상기 에에서는 발광 소자가 상기 활성층(111)에서 생성된 광자들의 적출효율을 높이기 위해 상기 측벽(116)을 경사지게 한 절두 역피라미드 형상을 가진다. 상기 활성층(111)에서 생성된 광자들이 상기 경사진 측벽(116)에서 반사되어 상기 상부면(117)을 통해 적출되도록 함으로써 광자가 칩 내부로 흡수되는 것을 방지한다.

그런데, 상기와 같이 하여 광자의 적출효율을 높일 수는 있지만 광자의 적출시 적출각도는 무작위적이다. 따라서, 발광 소자에서 발광되어 나오는 빔의 각 스펙트럼이 중요한 때에는 이러한 방법은 효과적인 방법이라고 할 수 없다. 특히, 적출되는 광의 각 스펙트럼이 콜리메이팅 빔이 갖는 것과 같은 정도의 형태로 되어야 할 것이 요구되는 응용 분야에서는 부적합하다.

발명이 이루고자 하는 기술적 과제

따라서, 본 발명은 상기한 문제점을 해결하기 위하여 안출된 것으로, 적출되는 광의 각 스펙트럼을 조절할 수 있도록 된 반도체 발광 소자를 제공하는데 그 목적이 있다.

발명의 구성 및 작용

상기한 목적을 달성하기 위하여 본 발명에 따른 반도체 발광 소자는, 전자와 정공들이 도핑되어 있는 n형 및 p형 에피택시얼층; 광자들이 발생되는 활성층; 상 기 활성층에서 상기 전자와 정공이 결합되도록 전압을 가하는 오믹 콘택트;

를 포함하는 반도체 발광 소자에 있어서,

상기 광자들이 평행광으로 적출될 수 있도록 소자의 측벽 또는 상부면에 회절 광학 소자가 구비되는 것을 특징으로 한다.

상기 측벽이 소정 각도로 기울어져 있는 것을 특징으로 한다.

상기 회절 광학 소자 앞에 굴절 소자가 더 구비되는 것을 특징으로 한다.

상기 회절 광학 소자가 특정한 패턴을 형성하도록 설치되는 것을 특징으로 한다.

이하, 본 발명의 바람직한 실시예에 따른 반도체 발광 소자에 대해 첨부 도면을 참조하여 상세히 설명한다.

도 2를 참조하면, 본 발명에 따른 반도체 발광 소자는 전자와 정공이 도핑된 p형 및 n형 에피택시얼 층(13)(14)과, 상기 p형 및 n형 에피택시얼 층(13)(14)들 사이에 형성되고, 광자들이 발생되는 활성층(10)과, 상기 활성층(10)으로부터 튀어나오는 광자들이 통과되는 윈도우 층(12)과, 소정 전압을 인가하는 제1 및 제2 콘택트(15)(20)를 포함한다.

또한, 상기 활성층(10)으로부터 튀어나온 광자들이 반사되어 소자의 상부면(17)을 통해 적출되도록 측벽(23)이 형성되는데, 이 측벽(23)에 회절 광학 소자(25)가 구비된다. 상기 회절 광학 소자(25)는 소자 밖으로 적출되는 광자의 각도를 조절하기 위해 상기 활성층(10)에서 발광되는 광 중 주광의 각도를 상기 측벽에 입사되는 각도로 가정하여 제작된다.

예를 들어, 상기 활성층(10)에서 발광되는 광 중 주광의 각도를 각각 각 α 와 각 β 라고 할 때, 소정의 입사각도와 파장을 가지고 입사하는 기준파와 상기 α 와 각 β 를 가지고 입사하는 광을 간섭을 일으켜 회절 광학소자를 제작한다. 이러한 직접 기록 방식 이외에 시뮬레이션을 이용하는 CGH(Computer Generated Hologram)를 사용하기나 포토레지스트가 코팅된 글라스 위에 직접 두 빛을 사용하여 프린지 패턴을 기록하고, 이온 빔 밀링이나 이온 에칭으로 가공하는 표면 릴리프 타입으로 제작 가능하다.

간접기록방식이나 직접기록방식으로 제작되는 회절광학소자는 그레이팅의 크기, 모양 그리고 주기 등에 의해 각 영역에서 회절되는 빛의 성질이 결정된다. 따라서, 회절되는 빛이 원하는 성질을 갖도록 각 영역의 그레이팅의 크기, 모양 및 주기등을 디자인을 한다.

본 발명에 따른 발광 소자에 채용되는 회절 광학 소자(25)는 상기 활성층(10)에서 발광된 광이 회절 광학 소자(25)에 입사되면 상기 상부면(17)을 통해 평행하게 나가도록 설계된다.

상기 설명에서는 상기 회절 광학 소자(25)가 상기 측벽(23)에 설치된 경우를 설명하였지만, 상기 상부면(17)에도 설치 가능함은 물론이다. 상기 측벽(23)에서 반사되어 나오는 광을 평행하게 적출되도록 할 수 있다. 이런 경우에는 투과형으로 제작되어야 한다.

상기와 같이 하여 측벽(23) 또는 상부면(17)에 회절 광학 소자를 설치하여 각 스펙트럼(angular spectrum)을 원하는 범위로 조절함과 아울러, 적출 효율을 고 려하여 상기 측벽(23)을 소정 각도로 경사지게 하는 것이 바람직하다.

한편, 도 3과 같이 상기 측벽(23)에 특정한 패턴을 가진 회절 광학 소자(26)를 설치할 수도 있다. 예를 들어, 평면 형태 뿐만 아니라 일정한 주기를 갖는 패턴이나 특정한 형상을 가진 회절 광학 소자(26)를 설치할 수 있다.

또한, 상기 측벽(23) 또는 상부면(17)에 굴절 소자(refractive element)(30)를 더 구비함으로써 상기 회절 광학 소자(26)쪽으로 입사되는 빔의 입사 각도를 조절하여 빔의 콜리메이팅 효율을 더 높일 수 있다.

발명의 효과

본 발명의 반도체 발광 소자는 측벽 또는 상부면에 구비된 회절 광학 소자에 의해 적출광의 각 스펙트럼(angular spectrum)을 조절함으로써 광자가 평행광으로 방출되도록 하여 콜리메이팅 시스템을 이용하는 많은 이용 분야에 적합하도록 한 것이다.

(57) 청구의 범위

청구항 1.
전자와 정공들이 도핑되어 있는 n형 및 p형 에피택시얼층;

광자들이 발생되는 활성층;

상기 활성층에서 상기 전자와 정공이 결합되도록 전압을 가하는 오믹 콘택트;를 포함하는 반도체 발광 소자에 있어서,

상기 광자들이 평행광으로 적출될 수 있도록 소자의 측벽 또는 상부면에 회절 광학 소자가 구비되는 것을 특징으로 하는 반도체 발광 소자.

청구항 2.
제 1항에 있어서,

상기 측벽이 소정 각도로 기울어져 있는 것을 특징으로 하는 반도체 발광 소자.

청구항 3.
제 1항 또는 제 2항에 있어서,

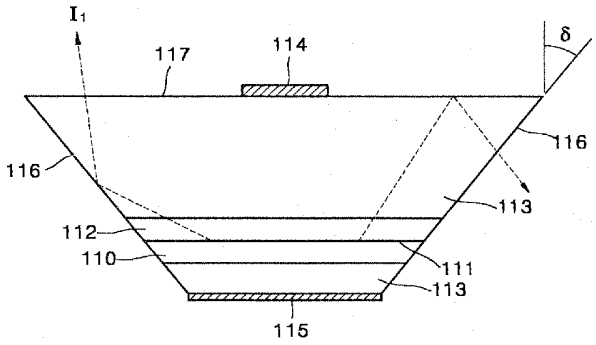
상기 회절 광학 소자 앞에 굴절 소자가 더 구비되는 것을 특징으로 하는 반도체 발광 소자.

청구항 4.
제 1항 또는 제 2항에 있어서,

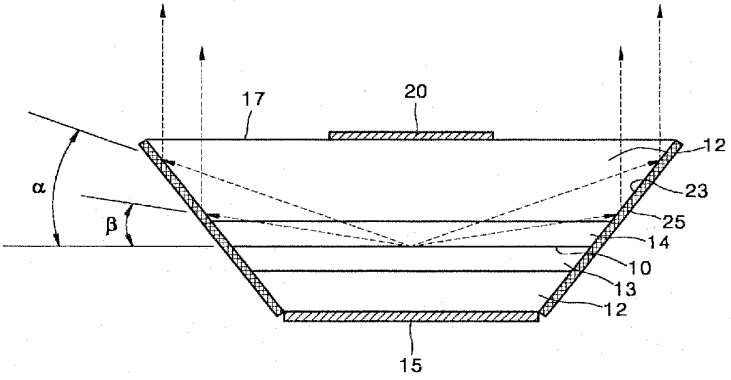
상기 회절 광학 소자가 특정한 패턴을 형성하도록 설치되는 것을 특징으로 하는 반도체 발광 소자.

도면

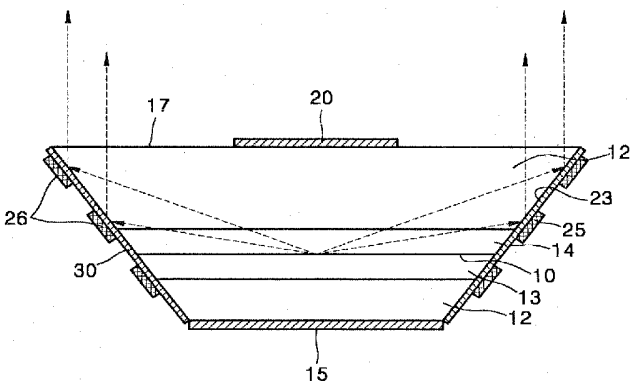
도면1



도면2



도면3



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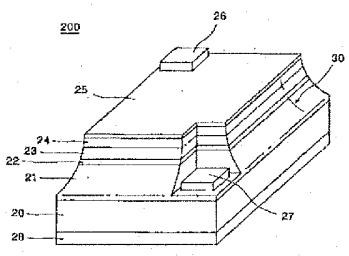
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(71)Applicant: VICHEL INC.
(72)Inventor: KANG, SANG GYU

(54) NITRIDE SEMICONDUCTOR LED AND FABRICATING METHOD THEREFOR

(57) Abstract:



PURPOSE: A nitride semiconductor LED and a fabricating method therefor are provided to reduce the consumption of chips due to a cutting process by using a scribing process and a cleaving process including a laser process. CONSTITUTION: A nitride semiconductor LED includes an active layer(22) and a p-type and n-type doping layers (24,21). The active layer(22) is formed by depositing a nitride semiconductor on a substrate(20). The p-type and n-type doping layers(24,21) are formed on an upper surface and a bottom surface of the active layer(22). An inclined portion(30) is formed on one outer side of an upper portion of the substrate(20) including the active layer(22) and the p-type and n-type doping layers(24,21). The inclined portion(30) is formed by using a scribing method including a laser process.

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(54) 질화물계 반도체 발광 소자 및 그 제조방법

요약

본 발명은 질화물계 반도체 발광 소자의 칩 생산수율과 그 자체의 광 이용효율을 극대화시킨 질화물계 반도체 발광 소자 및 그 제조방법을 제공하기 위한 것으로, 본 발명에 의하면 기판(20)상에 질화물계 반도체로 된 활성층(22)과, 이 활성층(22)의 상부 및 하부에 각각 형성된 질화물계 반도체로 된 p형 및 n형 도핑층(24, 21)을 구비하여 이루어진 질화물계 반도체 발광 소자(200; 300; 400; 500; 600)에 있어서, 상기 소자의 기판(20) 외측면 또는 활성층(22)과 상기 도핑층(21, 24)을 둘러싸는 외측면에는 레이저 가공을 통한 흠집내기(Scribing) 공정 및 절개 공정에 의해 경사지게 절개된 경사부(30; 40)가 형성되는 것을 특징으로 하는 질화물계 반도체 발광 소자가 제공된다.

대표도

도 3

색인어

질화물계, 반도체, 발광 소자, 결정 구조, 전반사, 경사부

명세서

도면의 간단한 설명

도 1은 일반적인 질화물계 발광 다이오드의 구조를 개략적으로 나타낸 도면,

도 2는 종래의 직육면체 구조의 질화물계 발광 다이오드의 수평 단면을 통해서 임의의 점광원에서 발생한 빛의 순환적인 전반사 과정을 설명하기 위한 도면,

도 3은 본 발명의 제1 실시예에 따른 질화물계 반도체 발광 소자의 구조를 개략적으로 나타낸 사시도,

도 4는 본 발명의 실시예에 따른 질화물계 반도체 발광 소자의 제조 공정에서 흠집내기 공정을 설명하기 위한 도면,

도 5는 본 발명의 실시예에 따른 질화물계 반도체 발광 소자의 제조 공정에서 홈집내기 공정의 또다른 예를 설명하기 위한 도면,

도 6은 본 발명의 제2 실시예에 따른 질화물계 반도체 발광 소자의 일예를 개략적으로 나타낸 사시도,

도 7a는 본 발명의 제2 실시예에 따른 질화물계 반도체 발광 소자의 다른 예를 개략적으로 나타낸 사시도,

도 7b는 도 7a의 평면도,

도 8은 질화물계 반도체가 가지는 정육각형 기둥 모양의 단위 결정 구조를 나타낸 도면,

도 9는 도 8의 단위 결정 구조들이 주기적으로 배열된 질화물계 반도체의 결정 구조를 (0001)면에서 바라본 것을 단순화시켜 나타낸 도면,

도 10a 내지 도 10c는 본 발명의 제2 실시예에 따른 정삼각형, 평행사변형, 사다리꼴 모양의 수평 단면을 갖는 질화물계 반도체 발광 소자의 제조 공정을 설명하기 위한 도면,

도 11a는 본 발명의 제3 실시예에 따른 질화물계 반도체 발광 소자를 설명하기 위한 도면,

도 11b는 도 11a의 평면도,

도 12는 본 발명의 실시예에 따른 질화물계 반도체 발광 소자의 제조 공정에서 홈집내기 공정의 또다른 예를 설명하기 위한 도면,

도 13a는 본 발명의 제4 실시예에 따른 질화물계 반도체 발광 소자를 설명하기 위한 도면,

도 13b는 도 13a의 평면도,

도 14는 전자 소자의 인쇄회로기판에 실장되는 본 발명의 제4 실시예에 따른 질화물계 반도체 발광 소자의 일예를 설명하기 위한 도면,

도 15는 도 14에서 인쇄회로기판 위에 플립칩 본딩되는 발광 소자의 배치를 설명하기 위한 도면.

* 도면의 주요 부분에 대한 부호의 설명 *

20 : 기판 21, 24 : 도핑층

22 : 활성층 23 : 클레드층

26, 27 : 전극 30, 40 : 경사부

72a, 72b : 전극 패턴 74a, 74b : 솔더 범프

200, 300, 400, 500, 600 : 발광 소자

700 : 인쇄회로기판

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 질화물계 반도체 발광 소자와 그 제조방법 및 이를 이용한 전자 소자에 관한 것으로, 특히 칩 생산수율(yiel

d)과 소비전력 대비 광 이용효율(quantum efficiency)을 극대화한 질화물계 반도체 발광 소자 및 그 제조방법에 관한 것이다.

일반적으로 질화물계 반도체 발광 다이오드(Nitride Semiconductor LED, 100)는 도 1에 도시된 바와 같이 기판(20) 상에 실제로 빛을 발생시키기 위한 InGaN 등의 활성층(22)과, 이 활성층(22)의 상부 및 하부에 각각 형성되어 활성층(22)에 전류를 공급할 수 있도록 다이오드 구조를 만드는 GaN 등의 n형 및 p형 도핑층(21, 24)을 구비하고 있다. 또한, 전하를 띤 캐리어들의 누적 효율을 증가시키기 위해 보다 큰 에너지 밴드갭을 갖는 AlGaN 등의 p형 클래드층(23)을 활성층(22)과 p형 도핑층(24) 사이에 추가적으로 구비하기도 한다. 도 1에서 25, 26, 27 및 28은 각각 p형 투명전극, p형 전극, n형 전극 및 반사용 금속층을 나타낸다.

한편, 종래의 질화물계 반도체 발광 다이오드는 대체로 직육면체, 즉 사각기둥의 구조를 취하고 있으며, 이러한 직육면체 구조의 질화물계 반도체 발광 다이오드를 제작하기 위해서는 일반적으로 다이아몬드 등의 절삭 공구를 이용하여 절삭을 행한다.

그러나 직육면체 구조의 발광 다이오드는 전반사 현상으로 인해 낮은 광 이용효율을 갖는다. 이는 발광 다이오드의 패키징 공정에서 칩 몰딩시 사용되는 에폭시의 굴절율이 칩의 굴절율보다 낮아서 칩 내부의 활성 영역에서 발생한 빛이 칩으로부터 에폭시쪽으로 빠져나올 때, 그 경계면에 어떤 임계각 이상으로 입사하는 모든 빛들은 빠져 나오지 못하기 때문이다.

도 2는 종래의 직육면체 구조의 질화물계 발광 다이오드의 수평 단면을 통해서 임의의 점광원에서 발생한 빛의 순환적인 전반사 과정을 설명하기 위한 도면이다. 여기서 사방으로 임계각의 원뿔 영역(빗금친 부분에 해당함)을 제외한 영역으로 경계면에 입사한 빛들은 계속해서 모든 경계면에서 전반사 영역에 머물게 되어 영원히 바깥으로 빠져나올 수 없게 된다. 도 2에서 어느 점광원에서 발생된 빛이 전반사각에 해당하는 Θ_1 로 경계면에 입사하게 되면, 다음 경계면에서는 $\Theta_2 = \Theta_{10}$ 로 입사하게 되므로 결국 순환적인 전반사가 일어나게 된다. 직사각형 형태의 대칭성으로 인해

수학식 1

$$\theta_1+\theta_2=\theta_1+\theta_{10}=\pi/2$$

가 되므로, $\theta_c<\pi/4$ 이고 $\theta_c<\theta_1<\pi/2-\theta_c$ 인 경우에는 입사각 θ_1 에 대하여 순환적인 전반사가 일어남을 다음과 같이 쉽게 입증할 수 있다.

수학식 2

$$\theta_c<\theta_2(=\theta_{10}=\pi/2-\theta_1)<\pi/2-\theta_c$$

직육면체의 경우, 실제로는 3차원이므로 임의의 광원이 접하는 면은 모두 6개가 된다. 따라서 경계면내 임의의 한 점을 생각해 볼 때, 그 점을 꼭지점으로 하여 임계각과 같은 각도로 형성된 원뿔내로 입사하는 광자들만 바깥으로 빠지나올 수 있다.

실제로, 에폭시의 굴절율은 대개 약 1.5이고 질화갈륨(GaN)의 굴절율은 약 2.5이므로, 이를 전반사 임계각에 관한 수학식 3에 넣어서 계산해 보면, 발광 다이오드 칩의 전반사 임계각 θ_c 는 약 36.9° 가 된다.

수학식 3

$$\theta_c=\arcsin(n_{epoxy}/n_{GaN})$$

결국 경계면의 수직면에 36.9° 이상 53.1° ($\pi/2-\theta_c$) 이하의 각으로 입사한 빛들은 모두 반사되어 바깥으로 빠져나올 수 없다. 다른 요소들을 고려하지 않고 이상적인 직육면체 모양의 발광 다이오드 칩을 고려하여 광 이용효율을 계산해 보면,

수학식 4

$$\eta_{trans}=3[1-\{1-(n_{epoxy}/n_{GaN})^2\}^{1/2}]$$

을 통해서 광 이용효율 $\eta_{trans}=0.6$ 의 값을 얻을 수 있다.

위의 예는 실제의 발광 다이오드와는 다른 이상적인 예이지만, 전반사 현상으로 인하여 발생된 모든 빛을 이용할 수 없다는 사실은 자명하다. 실제 발광 다이오드는 전극을 통해 넣어준 전류가 발광 다이오드의 활성 영역에서 빛으로 전환되어 상하의 p형 및 n형 도핑층을 지나서 바깥으로 나오게 되므로, 이 과정에서 전기에너지의 빛에너지로의 전환효율과 발광 다이오드내 결정층에서의 흡수, 굴절율과 다른 경계면에서 일어나는 일정량의 반사 등의 요소들을 모두 고려해 주어야만 정확한 광 이용효율을 구할 수가 있다. 더구나 대개의 발광 다이오드의 구조는 앞서 설명한 도 1에서와 같이 그 하측에 금속면을 증착하여 'n'형 전극으로 이용하거나 질화물계 반도체 발광 다이오드에서 사파이어(Al_2O_3) 등의 부도체 기판을 사용하는 경우에도 이 기판이 반사면으로 작용하기 때문에 아래쪽으로 진행하는 빛은 모두 다시 반사되어 활성 영역으로 되돌아온다. 따라서 관련된 모든 요소들을 고려해 볼 때, 일반적으로 실제 발광 다이오드는 입력된 전류량의 약 20% 미만의 광 이용효율을 가진다.

또한 질화물계 반도체는 기본적으로 정육각형(Hexagonal) 기둥 모양의 결정 구조(Crystal Structure)를 갖고 있기 때문에, 상기와 같이 다이아몬드 등의 절삭 공구를 이용하여 절삭을 행할 경우 절삭 공구가 갖는 두께와 그 두께만큼의 추가적인 웨이퍼의 손실을 가져온다. 따라서 질화물계가 아닌 다른 화합물로 된 반도체 발광 다이오드의 칩 제작시와 비교할 때, 최소 약 35% 이상의 칩 손실을 가져오게 된다.

예를 들어, 현재 보편적으로 사용되고 있는 다이아몬드 절삭 공구의 날 두께는 50㎛인데, 이를 사용하여 300㎛×300㎛ 크기의 정사각형 모양의 수평 단면 구조를 갖는 직육면체의 발광 다이오드의 칩을 만든다고 가정하자. 이 경우 절삭날이 기판을 지나가면서 절삭날 두께의 약 2배에 해당하는 100㎛ 이상의 폭에 해당하는 영역이 소실된다. 더욱이 이런 방식의 칩 제작과정에서는 절삭에 의해 생산된 칩마저 가장자리에 충격이 가해져 손상되기가 쉬우므로 실제로 이용가능한 칩의 수는 더욱 줄어든다.

한편, 이러한 광 이용효율을 고려한 기술이 대한민국 공개특허공보 제1998- 83823호에 개시되어 있다. 동 공보에는 적은 소비전력으로 높은 휘도의 광을 발생시키기 위한 것으로, 발광 다이오드의 몸체의 적어도 어느 일부분의 수평 단면을 삼각형 또는 예각을 갖는 사변형으로 하고 수직 영역의 단면적이 수직 방향으로 점차적으로 증가 또는 감소하는 형태로 하는 것이 제안되어 있다.

그러나 상기한 기술은 광 이용효율의 측면에서는 종래에 비해 다소 개선된 것이라 할 수 있으나, 본 발명의 관심사 중의 하나인 칩 생산수율의 관점에서 보면 오히려 종래의 직육면체 형태의 반도체 발광 다이오드에 비해 칩 생산수율이 더욱 저하될 수밖에 없다는 문제점을 가지고 있다. 뿐만 아니라, 상기한 공보의 어느 곳에서도 기본적으로 정육각형 기둥 모양의 단위 결정 구조를 갖는 질화물계 반도체의 특성을 고려한 점을 찾아볼 수 없으며, 따라서 상기 기술이 본 발명에서와 같은 질화물계 반도체 발광 소자에 그대로 적용될 경우 다이아몬드 절삭 공구의 과도한 사용으로 인한 칩 생산수율의 현저한 감소를 초래할 수밖에 없다는 치명적인 문제점을 내포하고 있는 것이다.

발명이 이루고자 하는 기술적 과제

본 발명은 상기한 종래 기술의 문제점을 해결하기 위하여 안출된 것으로, 본 발명의 목적은 질화물계 반도체 발광 소자 자체의 광 이용효율을 크게 향상시킨 질화물계 반도체 발광 소자를 제공하는 데 있다.

본 발명의 또다른 목적은 질화물계 반도체 발광 소자의 제작시 절삭 공구의 사용으로 인한 불필요한 칩의 손실을 없앰으로써 칩 생산수율을 종래에 비해 현저히 개선한 질화물계 반도체 발광 소자의 제조방법을 제공하는 데 있다.

본 발명의 또다른 목적은 질화물계 반도체 발광 소자의 결정구조를 고려하여 레이저 가공을 이용한 흠집내기 공정을 이용함으로써 칩 생산수율을 종래에 비해 더욱 현저히 개선하고 동시에 질화물계 반도체 발광 소자 자체의 광 이용효율을 더욱 크게 향상시킨 질화물계 반도체 발광 소자 및 그 제조방법을 제공하는 데 있다.

발명의 구성 및 작용

상기한 목적을 달성하기 위한 본 발명은 기판상에 질화물계 반도체로 된 활성층과, 이 활성층의 상부 및 하부에 각각 형성된 질화물계 반도체로 된 p형 및 n형 도핑층을 구비하여 이루어진 질화물계 반도체 발광 소자에 있어서, 상기 소자의 활성층과 도핑층을 둘러싸는 외측면 중 적어도 어느 하나의 외측면은, 레이저 가공을 이용한 흠집내기(Scribing) 공정에 의해 경사지게 절개되어, 상기 기판의 상부측 방향으로 갈수록 단면적이 감소하는 모양으로 이루어진 경사부를 포함하는 것을 특징으로 하는 질화물계 반도체 발광 소자를 제공한다.

본 발명은 또한 기판상에 질화물계 반도체로 된 활성층과, 이 활성층의 상부 및 하부에 각각 형성된 질화물계 반도체로 된 p형 및 n형 도핑층을 구비하여 이루어진 질화물계 반도체 발광 소자에 있어서, 상기 기판의 적어도 어느 하나의 외측면은, 레이저 가공을 이용한 흠집내기(Scribing) 공정에 의해 경사지게 절개되어, 상기 활성층과 상기 도핑층이 형성되어 있는 방향의 반대쪽 방향으로 갈수록 단면적이 감소하는 모양으로 이루어진 경사부를 포함하는 것을 특징으로 하는 질화물계 반도체 발광 소자를 제공한다.

본 발명에 있어서, 상기 레이저 가공은 펨토세컨드 레이저(Femtosecond Laser)를 이용하는 것이 바람직하다.

본 발명에 있어서, 상기 레이저 가공은 진공 분위기 하에서 행해지는 것이 바람직하다.

본 발명에 있어서, 질화물계 반도체 발광 소자는 질화물계 반도체의 결정 구조에 따른 정삼각형을 기본으로 하여, 이들의 조합으로 이루어진 정삼각형, 평행사변형, 사다리꼴 중 어느 하나의 수평 단면 구조를 갖는 것이 더욱 바람직하다.

본 발명은 또한 기판상에 질화물계 반도체로 된 활성층과, 이 활성층의 상부 및 하부에 각각 형성된 질화물계 반도체로 된 p형 및 n형 도핑층을 포함하여 이루어진 질화물계 반도체 발광 소자의 제조방법에 있어서, 상기 질화물계 반도체 발광 소자가 다수 형성되어 있는 웨이퍼를 개개의 칩으로 자르는 과정에서, 상기 활성층과 상기 도핑층의 외측면에 경사부가 형성되도록 레이저 가공을 이용하여 상기 웨이퍼에 흠집내기(Scribing)를 행하는 흠집내기 공정; 및 상기 흠집내기 공정에 의해 형성된 직선들을 따라 절개(Cleaving)를 행하는 절개 공정을 포함하는 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법을 제공한다.

본 발명은 또한 기판상에 질화물계 반도체로 된 활성층과, 이 활성층의 상부 및 하부에 각각 형성된 질화물계 반도체로 된 p형 및 n형 도핑층을 포함하여 이루어진 질화물계 반도체 발광 소자의 제조방법에 있어서, 상기 질화물계 반도체 발광 소자가 다수 형성되어 있는 웨이퍼를 업사이드 다운(upside-down) 방식으로 개개의 칩으로 자르는 과정에서, 상기 기판의 외측면에 경사부가 형성되도록 레이저 가공을 이용하여 상기 웨이퍼에 흠집내기(Scribing)를 행하는 흠집내기 공정; 및 상기 흠집내기 공정에 의해 형성된 직선들을 따라 절개(Cleaving)를 행하는 절개 공정을 포함하는 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법을 제공한다.

본 발명에 있어서, 상기 레이저 가공은 펨토세컨드 레이저(Femtosecond Laser)를 이용하는 것이 바람직하다.

본 발명에 있어서, 상기 레이저 가공은 진공 분위기 하에서 행해지는 것이 바람직하다. 한편, 상기 레이저 가공이 대기중에서 행해지는 경우, 레이저 가공은 생성되는 부산물을 제거하기 위해 압축 공기 분사 또는 화학 물질 주입 과정과 함께 행해지는 것이 더욱 바람직하다.

본 발명에 있어서, 상기 흠집내기 공정은, 상기 질화물계 반도체의 결정 구조를 따라 제1의 간격을 두고 제1 방향으로 다수의 흠집내기를 행하는 제1 흠집내기 공정과; 상기 질화물계 반도체의 결정 구조를 따라 제2의 간격을 두고 상기 제1 방향과 60° 의 각도를 이루는 제2 방향으로 다수의 흠집내기를 행하는 제2 흠집내기 공정; 및 상기 질화물계 반도체의 결정 구조를 따라 제3의 간격을 두고 상기 제1 방향 및 제2 방향과 각각 60° 의 각도를 이루는 제3 방향으로 다수의 흠집내기를 행하는 제3 흠집내기 공정을 포함하고, 상기 절개 공정은 상기 제1, 제2 및 제3 흠집내기 공정에 의해 형성된 직선들을 따라 절개를 행하는 것이 바람직하다.

본 발명에 있어서, 상기 제1의 간격과 제2의 간격 및 제3의 간격은 모두 동일하게 조정되는 것이 바람직하다.

본 발명에 있어서, 상기 제1의 간격과 제2의 간격은 서로 동일하며, 상기 제3의 간격은 상기 제1의 간격 및 제2의 간격의 1/2로 조정되는 것도 바람직하다.

본 발명에 있어서, 상기 흠집내기 공정은, 상기 질화물계 반도체의 결정 구조를 따라 제1의 간격을 두고 제1 방향으로 다수의 흠집내기를 행하는 제1 흠집내기 공정과; 상기 질화물계 반도체의 결정 구조를 따라 제2의 간격을 두고 상기 제1 방향과 60° 의 각도를 이루는 제2 방향으로 다수의 흠집내기를 행하는 제2 흠집내 기 공정을 포함하고, 상기 절개 공정은 상기 제1 및 제2 흠집내기 공정에 의해 형성된 직선들을 따라 절개를 행하는 절개 공정을 포함하며, 상기 제1의 간격과 상기 제2의 간격은 m:n(m, n은 양의 정수)의 비율을 가질 수 있다.

이하, 본 발명의 바람직한 실시예를 도면을 참조하여 구체적으로 설명하기로 한다.

실시예

이하에서 설명되는 본 발명은 기본적으로 네 가지 측면에서 강조된다. 첫 번째 측면에서는 질화물계 반도체 발광 소자의 기판 상부측 측면-활성층과 도핑층을 둘러싸는 외측면-에 경사부가 형성되도록 레이저 가공을 이용한 흠집내기 공정을 웨이퍼 상에 행한 후에 절개하여 소자의 측면 대칭성을 깨뜨림으로써 소자 내부에서 발생되는 광의 순환적인 전반사를 제거하여 광 이용효율을 극대화시킨다.

두 번째 측면에서는 질화물계 반도체 발광 소자가 질화물계 반도체의 결정 구조에 따른 수평 단면 구조를 갖고 그것의 기판 상부측 측면-활성층과 도핑층을 둘러싸는 외측면-에 경사부를 구비하도록 레이저 가공을 이용한 흠집내기 공정을 웨이퍼 상에 행한 후에 절개하여 소자의 평면 및 측면 대칭성을 깨뜨림으로써 소자 내부에서 발생되는 광의 순환적인 전반사를 제거하고 광 이용효율을 극대화시킬 뿐만 아니라 소자(칩)의 수율을 종래에 비해 현저히 개선한다.

세 번째 측면에서는 질화물계 반도체 발광 소자의 기판 측면에 경사부가 형성되도록 레이저 가공을 이용한 흠집내기 공정을 업사이드 다운 방식으로 웨이퍼 상에 행한 후에 절개하여 소자의 측면 대칭성을 깨뜨림으로써 소자 내부에서 발생되는 광의 순환적인 전반사를 제거하고 동시에 광 이용효율을 극대화시킨다.

네 번째 측면에서는 질화물계 반도체 발광 소자가 질화물계 반도체의 결정 구조에 따른 수평 단면 구조를 갖고 그의 기판 측면에 경사부가 형성되도록 레이저 가공을 이용한 흠집내기 공정을 업사이드 다운 방식으로 웨이퍼 상에 행한 후에 절개하여 소자의 평면 및 측면 대칭성을 깨뜨림으로써 소자 내부에서 발생되는 광의 순환적인 전반사를 제거하고 광 이용효율을 극대화시킬 뿐만 아니라 소자(칩)의 수율을 종래에 비해 현저히 개선한다.

<실시예 1>

도 3은 본 발명의 제1 실시예에 따른 질화물계 반도체 발광 소자의 구조를 개략적으로 나타낸 사시도이다.

도 3에 도시된 바와 같이, 본 발명의 제1 실시예에 따른 질화물계 반도체 발광 소자(200)는, 사파이어(Al_2O_3) 기판(20) 상에 InGaN 등의 질화물계 반도체로 된 활성층(22)과, 이 활성층(22)의 상부 및 하부에 각각 형성된 GaN 등의 질화물계 반도체로 된 p형 및 n형 도핑층(24, 21)을 구비하여 이루어진다. 또한 전하를 띤 캐리어들의 누적 효율을 증가시키기 위해 보다 에너지 밴드갭을 갖는 AlGaN 등의 클래드층(23)을 활성층(22)과 p형 도핑층(24) 사이에 추가적으로 구비할 수 있다. 그리고 상기한 p형 도핑층(24)의 상부에 형성되는 p형 투명전극(25)과, 이 p형 투명 전극(25) 위에 부분적으로 형성되는 p형 전극(26)과, 상기한 n형 도핑층(21)에 접하여 형성되는 n형 전극(27), 및 기판(20)의 제2 주면(도면에서 아래쪽 면) 상에 형성되는 반사용 금속층(28)이 적절한 형태와 크기로 소정 위치에 구비된다.

특히 본 발명의 제1 실시예에 따른 질화물계 발광 소자(200)는 그 측면- 예를 들면 상기한 활성층(22)과 도핑층(21, 24)을 둘러싸는 외측면 -에 형성된 경사부(30)를 포함한다. 이러한 경사부(30)는 일관가공(Fabrication) 과정에서 가공된 웨이퍼 상에 오목한 모양으로 흠집(32)을 내는 레이저 가공을 이용한 흠집내기 공정에 의해 형성된다. 이러한 흠집내기 공정에는 예를 들어 펨토세컨드 레이저(Femtosecond Laser) 등의 극초단 레이저가 이용되는 것이 바람직하다. 도 4는 본 발명의 레이저 가공을 이용한 흠집내기 공정을 설명하기 위한 도면이다. 도 4에 도시된 바와 같이, 펨토세컨드 레이저로 질화물계 물질을 가공하면, 그 가공면의 프로파일(profile)은 대략 반원형 또는 반타원형 모양이 된다.

극초단 레이저 가공은 먼저 아주 짧은 펄스 길이 때문에 매우 높은 파워(충격량)를 만들어 낼 수 있으며, 가공 물질로 에너지를 아주 빨리 효과적으로 전달할 수 있어 열 전달 및 확산(thermal diffusion) 현상에 의한 에너지 손실을 극소화할 수 있을 뿐만 아니라 가공중에 물질에 가해질 수 있는 열적 충격이나 변형을 극소화 할 수 있다. 또한 아주 급격한 레이저 가공 문턱선속(very abrupt threshold laser fluence) 특성은 가공 물질의 위치나 결함밀도(defect density) 등에 구애받지 않고 물질을 가공할 수 있게 함으로써 특히 투명물질의 가공시 뛰어난 가공 정확도와 미세도를 확

보할 수 있게 해준다.

예를 들어, 극초단 레이저 가공은 진공 분위기 하에서 강도를 1.6×10^{2} mJ/㎠로 하고 스캔 속도를 0.5㎜/sec로 한 펨토세컨드 레이저 선속(laser fluence)을 이용하여 반도체 소자용 질화물계 물질을 가공했을 때, 질화물계 물질에 대략 깊이 13㎛, 폭 20~30㎛의 홈이 얻어지도록 행해질 수 있다. 특히 레이저 가공은 대기중에서 행하는 경우 레이저 가공을 행한 후에 홈의 내부와 주위에 재증착되는 산화 물질이 생성되기 때문에 진공 분위기 하에서 행해질 수 있다.

한편, 위의 예에서와 같이 진공 분위기 하에서 레이저 가공을 실시하지 않고 대기중에서 행하는 경우에는, 압축 공기를 분사하여 산화 부산물을 제거하거나 화학 물질을 주입하여 산화 부산물을 처리할 수 있다.

이와 같이 본 발명에서는 극초단 레이저 가공을 적절하게 행하여 질화물계 반도체 발광 소자(200)의 기판 상부측 측면에 형성된 경사부(30)의 곡선의 기울기를 이 곡선에 접하는 접선의 기울기로 보았을 때 0° 를 초과해서 90° 미만의 범위 내에 있도록 적절하게 조정할 수 있다.

한편, 본 발명의 제1 실시예에 따른 질화물계 반도체 발광 소자는 상술한 구성으로 한정되지 않는다. 예를 들면 도 5에 도시된 바와 같이 가공된 웨이퍼의 홈집내기 공정에서 기판(20)의 소정 부분에까지 홈집(30a)을 형성할 수 있다. 이러한 경우, 홈집(30a)은 사파이어 기판(20)에서는 'V'자 형상으로 형성되고, 기판(20) 상의 질화물계 박막 형성부에서는 반원형 또는 반타원형 모양으로 형성된다. 즉 본 발명은 기판(20)의 소정 부분까지 경사부가 형성된 질화물계 반도체 발광 소자를 포함할 수 있다.

<실시예 2>

도 6은 본 발명의 제2 실시예에 따른 질화물계 반도체 발광 소자의 일예를 개략적으로 나타낸 사시도이고, 도 7a는 본 발명의 제2 실시예에 따른 질화물계 반도체 발광 소자의 다른 예를 개략적으로 나타낸 사시도이며, 도 7b는 도 7a의 평면도이다.

도 6과 도 7a 및 도 7b에 도시된 바와 같이, 본 발명의 제2 실시예에 따른 질화물계 반도체 발광 소자(300, 400)는, 본 발명의 제1 실시예에 따른 질화물계 반도체 발광 소자(200)와 유사하게, 사파이어(Al_2O_3) 기판(20) 상에 InGaN 등의 질화물계 반도체로 된 활성층(22)과, 이 활성층(22)의 상부 및 하부에 각각 형성된 GaN 등의 질화물계 반도체로 된 p형 및 n형 도핑층(24, 21)을 구비하여 이루어진다. 또한 전하를 띤 캐리어들의 누적 효율을 증가시키기 위해 보다 에너지 밴드갭을 갖는 AlGaN 등의 클래드층(23)을 활성층(22)과 p형 도핑층(24) 사이에 추가적으로 구비할 수 있다. 그리고 상기한 p형 도핑층(24)의 상부에 형성되는 p형 투명전극(25)과, 이 p형 투명전극(25) 위에 부분적으로 형성되는 p형 전극(26)과, 상기한 n형 도핑층(21)에 접하여 형성되는 n형 전극(27), 및 기판(20)의 제2 주면(도면에서 아래쪽 면) 상에 형성되는 반사용 금속층(28)이 적절한 형태와 크기로 소정 위치에 구비된다.

또한 본 발명의 제2 실시예에 따른 질화물계 반도체 발광 소자(300, 400)는 상기한 본 발명의 제1 실시예에 따른 질화물계 반도체 발광 소자(200)와 유사하게 기판(20)의 상부측 측면에 형성된 경사부(30)를 구비한다. 이러한 경사부(30)는 제1 실시예의 경우와 유사하게 일관가공 과정에서 웨이퍼 상에 홈집을 내는 레이저 가공을 이용한 홈집내기 공정에 의해 형성된다.

게다가, 본 발명의 제2 실시예에 따른 질화물계 반도체 발광 소자(300, 400)는 상기한 경사부(30)를 구비하는 것 이외에 질화물계 반도체의 결정 구조에 따른 수평 단면 구조를 갖는다. 다시 말해서, 사파이어 기판(20)과 이 기판(20)의 주면 상에 형성된 다수의 질화물계 박막층(21, 22, 23, 24)은 동일한 정육각형 기둥 모양의 결정 구조를 갖는다. 이러한 정육각형 기둥 모양의 결정 구조는 그 수평 단면 구조가 정삼각형 또는 정삼각형이 조합된 형상을 포함한다. 따라서 본 발명의 제2 실시예는 가공된 웨이퍼를 개개의 칩으로 자를 때, 상기한 결정 구조에 따라 정삼각형 또는 정삼각형이 조합된 형상-평행사변형 또는 마름모꼴 형상-으로 잘려진 칩(소자)에 의해 달성된다. 물론 본 발명의 제2 실시예에 따른 질화물계 반도체 발광 소자(300, 400)가 다수 가공되어 있는 웨이퍼를 결정 구조에 따라 자를 때에는 각 발광 소자의 기판 상부측 측면에 경사부(30)가 구비되도록 레이저 가공을 이용한 홈집내기 공정을 행해야 한다.

참고로 도 6은 수평 단면 구조가 정삼각형인 경우를 나타내고, 도 7a 및 도 7b는 수평 단면 구조가 평행사변형인 경우를 나타낸다. 또한, 도 6과 도 7a 및 도 7b에 도시된 제2 실시예에 따른 질화물계 반도체 발광 소자의 수평 단면 구조에 있 어서, 예각 꼭지점은 모두 60° 가 되고 둔각 꼭지점은 모두 120° 가 된다.

다음은 본 발명의 제2 실시예에 따른 질화물계 반도체 소자(300, 400)의 상기한 수평 단면 구조에 대한 이론적 근거를 보다 구체적으로 설명한다.

질화갈륨(GaN)을 비롯한 모든 질화물계 반도체는 상기한 바와 같이 기본적으로 정육각형(Hexagonal) 기둥 모양의 결정 구조를 갖는다. 이 기둥의 수평 단면은 정삼각형 여섯개가 모인 구조로 볼 수 있다. 도 8과 도 9는 이를 설명하기

위한 것으로, 도 8은 질화물계 반도체가 가지는 정육각형 기둥 모양의 단위 결정 구조를 나타낸 도면이고, 도 9는 도 8의 단위 결정 구조들이 주기적으로 배열된 질화물계 반도체의 결정 구조를 (0001)면에서 바라본 것을 단순화시켜 나타낸 도면이다. 도 8에서, 각각의 단위벡터에 표시된 숫자들은 결정학에서 일반적으로 사용되는 표시를 따른 것이다.

반면 갈륨비소(GaAs)를 비롯한 다른 대부분의 화합물 반도체들은 정육면체(Cubic) 결정 구조를 가지고 있는데, 이런 정육면체 결정 구조를 가진 화합물 반도체들을 이용하여 발광 다이오드를 만들 때에는 직사각형 모양의 수평 단면을 갖는 직육면체 구조의 발광 다이오드를 제조함에 있어 절삭 공구를 사용하지 않고도 그 정육면체 결정 구조의 특성을 살려서, 칩 제작시 통상적으로 사용되는 흠집내기(Scribing)와 절개(Cleaving)를 통하여 발광 다이오드 칩을 만들기 때문에 기판의 손실이 거의 없다.

그러나 질화물계 반도체를 이용하여 발광 다이오드를 제조할 경우에는 이들의 결정 구조가 정삼각형을 기본으로 하는 정육각형 기둥(Hexagonal System)의 형 태로 되어 있기 때문에 수평 단면의 모양을 직사각형의 형태로 만들기 위해서는 어쩔 수 없이 절삭용 공구를 사용해야만 한다.

본 발명의 특징 중의 하나는 이와 같은 질화물계 반도체의 결정 구조의 특성을 고려한 것으로, 정삼각형을 기본으로 하는 정육각형 기둥의 구조를 가진 반도체들은 정삼각형을 기본으로 하는 수평 단면을 지닌 모양의 발광 다이오드 칩을 만들기 위해서 절삭용 공구를 사용하지 않고도 통상적인 칩 제조방법인 흠집내기(Scribing)와 절개(Cleaving)를 통하여 발광 다이오드를 생산할 수 있다는 것이다.

도 9는 이에 대한 기하학적인 설명으로 여기서 실선들은 결정면들을 수평 단면으로 나타낸 것으로 절개가 쉽게 이루어지는 선들이다. 반면에, 점선들은 직사각형 모양의 수평 단면을 갖는 직육면체 질화물계 반도체 발광 다이오드를 만들기 위해 절삭이 불가피한 선을 나타낸다. 이런 점선들은 절개가 쉽게 이루어지지 않기 때문에 결국 절삭용 공구를 사용하여 절단(cutting)해야만 하는 것이다.

질화물계 반도체 결정 구조를 이용하여 만들 수 있는 발광 다이오드의 수평 단면 구조들의 구체적인 예들이 도 10a 내지 도 10c에 각각 도시되어 있으며, 이에 대하여는 이하에서 보다 구체적으로 나누어 설명하기로 한다.

도 9로부터 알 수 있는 바와 같이, 질화물계 반도체의 결정 구조는 정삼각형을 기본으로 하기 때문에 정삼각형을 이루는 방향으로 절개가 잘 이루어진다. 즉 [2-1-10], [-12-10], [-1-120]의 방향들이 절개가 쉽게 이루어지는 방향들이다. 따라서 이런 정삼각형을 기본으로 하는 형태의 발광 다이오드를 만드는 것이 기판을 불필요하게 소모하지 않고 모두 칩으로 제작해낼 수 있는 가장 효율적인 방법이다.

도 10a는 본 발명의 제2 실시예에 따른 정삼각형 모양의 수평 단면을 갖는 질화물계 반도체 발광 소자의 제조 공정을 설명하기 위한 도면이다.

즉 본 실시예에서는 질화물계 반도체 발광 다이오드를 제조함에 있어, 질화물계 반도체의 결정 구조를 따라 소정의 간격을 두고 [2-1-10]의 방향으로 다수의 흠집내기를 행하고, 역시 질화물계 반도체의 결정 구조를 따라 상기 소정의 간격과 동일한 간격을 두고 상기 [2-1-10]의 방향과 60° 의 각도를 이루는 [-1-120]의 방향으로 다수의 흠집내기를 행하고, 다음에 질화물계 반도체의 결정 구조를 따라 위와 동일한 간격을 두고 상기 [2-1-10]의 방향 및 [-1-120]의 방향과 각각 60° 의 각도를 이루는 [-12-10]의 방향(도면상에서 수평 방향)으로 다수의 흠집내기를 행하는 공정들을 거친 후, 이들 공정에 의해 형성된 직선들을 따라 절개를 행하였다. 얻어진 개개의 정삼형 칩의 측면에는 흠집내기 공정에서 이미 형성된 경사부(30)가 구비되어 있었다.

이와 같은 공정들에 의해 원하는 정삼각형 모양의 수평 단면을 갖고 기판(20)의 상부의 측면이 경사지게 절개된 질화물계 반도체 발광 다이오드 칩들을 얻었다. 또한 여기서 정삼각형 모양의 수평 단면을 갖는 발광 다이오드 칩의 크기는 상기한 흠집내기 간격을 조절함으로써 얼마든지 조절이 가능하다.

도 10b는 본 발명의 제2 실시예에 따른 평행사변형 모양의 수평 단면을 갖는 질화물계 반도체 발광 소자의 제조 공정을 설명하기 위한 도면이다.

즉 본 실시예에서는 질화물계 반도체 발광 다이오드를 제조함에 있어, 질화 물계 반도체의 결정 구조를 따라 소정의 간격을 두고 [2-1-10]의 방향으로 다수의 흠집내기를 행하고, 다음에 질화물계 반도체의 결정 구조를 따라 상기 소정의 간격과 동일한 간격을 두고 상기 [2-1-10]의 방향과 60° 의 각도를 이루는 [-12-10]의 방향(도면상에서 수평 방향)으로 다수의 흠집내기를 행하는 공정들을 거친 후, 이들 공정에 의해 형성된 직선들을 따라 절개를 행하였다.

이와 같은 공정들에 의해 원하는 평행사변형 모양의 수평 단면을 갖고 기판(20)의 상부의 측면이 경사지게 절개된 질화물계 반도체 발광 다이오드 칩들을 얻었다. 또한, 여기서도 평행사변형 모양의 수평 단면을 갖는 발광 다이오드 칩

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의 크기는 상기한 홈집내기 간격을 조절함으로써 얼마든지 조절이 가능하다. 한편, 본 실시예에서는 홈집내기 공정에 있어 홈집내기 간격을 동일하게 하였으나, 홈집내기 간격을 m:n(m, n은 양의 정수)의 비율을 갖도록 함으로써 다양한 크기뿐만 아니라 다양한 모양의 평행사변형 모양의 수평 단면을 갖는 발광 다이오드 칩을 제조하는 것도 가능하다.

도 10c는 본 발명의 제2 실시예에 따른 사다리꼴 모양의 수평 단면을 갖는 질화물계 반도체 발광 소자의 제조 공정을 설명하기 위한 도면이다.

본 실시예에서는 상기한 제2 실시예의 삼각형 모양의 수평 단면을 갖는 질화물계 반도체 발광 소자의 제조 공정의 경우와 동일한 공정들에 의해 질화물계 반도체 발광 다이오드를 제조하였다. 다만, 본 실시예에서는 홈집내기 공정에 있어 [2-1-10]의 방향과 [-1-120]의 방향에 대한 홈집내기 간격은 서로 동일하게 하는 반면, [-12-10]의 방향에 대한 홈집내기 간격은 그 절반으로 설정하였다.

이와 같은 공정들에 의해 원하는 사다리꼴 모양의 수평 단면을 갖고 기판(20)의 상부의 측면이 경사지게 절개된 질화물계 반도체 발광 다이오드 칩들을 얻었으며, 이 사다리꼴 면적의 1/3에 해당하는 면적을 가진 정삼각형 모양의 수평 단면 구조를 갖고 기판(20)의 상부의 측면이 경사지게 절개된 칩들도 똑같은 개수로 얻었다. 또한, 여기서도 사다리꼴 및 정삼각형 모양의 수평 단면을 갖고 기판(20) 상부의 측면이 경사지게 절개된 발광 다이오드 칩의 크기는 상기한 홈집내기 간격을 조절함으로써 얼마든지 조절이 가능하다.

이상과 같은 본 발명의 실시예상의 형태들을 기본으로 질화물계 반도체 발광 다이오드를 제조하게 되면 광 이용효율을 극대화시키면서 동시에 웨이퍼의 수율을 극대화시킬 수 있다. 광 이용효율을 극대화시키는 것에 대해서는 이하에서 보다 구체적으로 살펴보기로 한다.

본 발명의 제2 실시예에서와 같은 정삼각형, 평행사변형 또는 사다리꼴 모양의 수평 단면을 갖는 발광 소자-예를 들면 발광 다이오드-의 경우 먼저 활성 영역의 임의의 점광원에서 발생한 빛 중 칩의 수직 경계면을 향해 임계각을 벗어난 전반사 영역으로 입사한 빛들은 일단 모두 반사된다. 그러나 정삼각형, 평행사변형 또는 사다리꼴의 특성상 대칭성이 깨져서 직사각형 수평 단면의 경우에서처럼 영구적인 전반사는 일어나지 않는다. 즉 곧바로 2차, 3차 경계면에서 임계각보다 작은 입사각으로 입사하게 되기 때문에 처음에 전반사되었던 빛이라 하더라도 결국 바깥으로 빠져나오게 된다.

<실시예 3>

도 11a는 본 발명의 제3 실시예에 따른 질화물계 반도체 발광 소자의 정면도이고, 도 11b는 도 11a의 평면도이며, 도 12는 본 발명의 실시예에 따른 질화물계 반도체 발광 소자의 제조 공정에서 홈집내기 공정의 또다른 예를 설명하기 위한 도면이다.

도 11a에 도시된 바와 같이, 본 발명의 제3 실시예에 따른 질화물계 반도체 발광 소자(500)는, 사파이어(Al_2O_3) 기판(20) 상에 InGaN 등의 질화물계 반도체로 된 활성층(22)과, 이 활성층(22)의 상부 및 하부에 각각 형성된 GaN 등의 질화물계 반도체로 된 p형 및 n형 도핑층(24, 21)을 구비하여 이루어진다. 또한 본 실시예에도 제1 및 제2 실시예의 경우와 유사하게 전하를 띤 캐리어들의 누적 효율을 증가시키기 위해 보다 에너지 밴드갭을 갖는 AlGaN 등의 클래드층(미도시)을 활성층(22)과 p형 도핑층(24) 사이에 추가적으로 구비할 수 있다. 그리고 상기한 p형 도핑층(24)의 상부에 부분적으로 형성되는 p형 전극(26)과 상기한 n형 도핑층(21)에 접하여 형성되는 n형 전극(27)이 적절한 위치에 적절한 형태와 크기로 구비된다.

특히 본 발명의 제3 실시예에 따른 질화물계 반도체 발광 소자(500)는 기판(20)의 측면에 형성된 경사부(40)를 포함한다. 이러한 경사부(40)는 상기한 활성층(22)과 도핑층(21, 24)이 형성되어 있는 방향의 반대쪽 방향-도면에서 위쪽 방향-으로 갈수록 단면적이 감소되는 모양으로 이루어진다. 즉, 도 11a 및 도 11b에 도시된 것과 같이, 경사부(40)는 기판(20)이 대략 직사각형 단면 구조를 갖기 때문에 각 측면의 상단부가 중심으로 모여진 모양 또는 동축상에서 단면적이 감소하는 모양으로 형성된다. 도 11b에서 참조부호 12a는 기판(20)의 가장 위쪽 주면을 나타낸다.

또한 경사부(40)는 일관가공 과정에서 가공된 웨이퍼를 업사이드 다운방식으로 놓고 홈집을 내는 레이저를 이용한 홈집내기 공정에 의해 형성된다. 홈집내기 공정은 사파이어 기판에 'V'자 모양의 홈이 형성되도록 펨토세컨드 레이저에 의해 이루어진다. 도 12는 사파이어 기판에 레이저 가공을 이용하여 홈집내기 공정을 행한 예를 나타낸 예시도이고, 여기에서 참조부호 40은 경사부를 나타낸다. 이러한 경사부(40)는 수직 측면을 기준으로 하여 그 기울기가 0° 를 초과해서 90° 미만의 범위 내에 있도록 적절하게 조정된다.

예를 들어, 경사부(40)는 진공 분위기 하에서, 강도를 2.1×10^{4} mJ/㎠로 하고 스캔 속도를 0.025㎜/sec로 한 펨토세컨드 레이저 선속(laser fluence)을 이용하여 사파이어 기판을 가공했을 때, 사파이어 기판에 형성된 깊이 60㎛, 폭 78 ~ 86㎛의 'V'자 모양의 홈에 의해 소정 기울기로 형성된다. 한편, 본 실시예에서는 제1 실시예나 제2 실시예와는 달

리 사파이어 기판을 레이저 가공하기 때문에 부산물로서의 산화물질이 거의 발생되지 않는다. 따라서 레이저 가공을 대기중에서 행해도 크게 문제가 되지 않는다. 게다가, 레이저 가공을 대기중에서 행하는 경우에는 발생된 적은 부산물을 압축 공기나 화학 처리 등을 이용하여 용이하게 제거할 수도 있다.

<실시예 4>

도 13a는 본 발명의 제4 실시예에 따른 질화물계 반도체 발광 소자의 정면도이다.

도 13a에 도시된 바와 같이, 본 발명의 제4 실시예에 따른 질화물계 반도체 발광 소자(600)는, 사파이어(Al_2O_3) 기판(20) 상에 InGaN 등의 질화물계 반도체로 된 활성층(22)과, 이 활성층(22)의 상부 및 하부에 각각 형성된 GaN 등의 질화물계 반도체로 된 p형 및 n형 도핑층(24, 21)을 구비하여 이루어진다. 또한 본 실시예에도 제1, 제2 및 제3 실시예의 경우와 유사하게 전하를 띤 캐리어들의 누적 효율을 증가시키기 위해 보다 에너지 밴드갭을 갖는 AlGaN 등의 클래드층(미도시)을 활성층(22)과 p형 도핑층(24) 사이에 추가적으로 구비할 수 있다. 그리고 상기한 p형 도핑층(24)의 상부에 부분적으로 형성되는 p형 전극(26)과 상기한 n형 도핑층(21)에 접하여 형성되는 n형 전극(27)이 적절한 형태와 크기로 소정 위치에 구비된다.

특히 본 발명의 제4 실시예에 따른 질화물계 반도체 발광 소자(600)는 기판(20)의 측면에 형성된 경사부(40)를 포함한다. 이러한 기판(20)의 측면에 형성된 경사부(40)는 활성층(22)과 도핑층(21, 24)이 형성되어 있는 방향의 반대쪽 방향-도면에서 위쪽 방향-으로 갈수록 단면적이 감소되는 모양으로 이루어진다. 도 13b는 도 13a의 평면도이고, 여기에서 참조부호 20a는 기판(20)의 최상부측 표면을 나타낸다. 또한 경사부(40)는 일관가공 과정에서 가공된 웨이퍼를 업사이드 다운방 식으로 놓고 흡집내기를 행하는 레이저 가공을 이용한 흡집내기 공정에 의해 형성된다. 흡집내기 공정에는 제1, 제2 및 제3 실시예에서와 같이 펨토세컨드 레이저를 이용하는 것이 바람직하다.

게다가, 본 실시예에 따른 발광소자(600)는 상기한 경사부(40)를 구비하는 것에 더하여 본 발명의 제2 실시예의 경우와 유사하게 발광 소자(600)가 질화물계 반도체의 결정구조에 따른 수평단면구조를 갖는 것을 특징으로 한다. 도 13b에 도시된 바와 같이 본 발명의 제4 실시예에 따른 발광 소자는 정삼각형 또는 정삼각형이 조합된 모양-예를 들면 평행사변형, 사다리꼴 모양-을 갖는다. 도 13b에서 소자의 예각 꼭지점은 모두 60° 가 되고 둔각 꼭지점은 모두 120° 가 된다. 이에 대한 구체적인 설명은 제2 실시예의 수평단면구조에 대한 설명과 중복되므로 생략한다.

다음은 제4 실시예에 따른 질화물계 반도체 발광 소자를 인쇄회로기판에 실장하는 예를 설명한다.

도 14는 본 발명의 실시예에 따른 질화물계 반도체 발광 소자를 전자 소자의 인쇄회로기판 상에 플립칩 본딩 방식으로 실장하는 예를 설명하기 위한 도면이고, 도 15는 도 14에서 전자 소자의 인쇄회로기판 위에 플립칩 본딩되는 발광 소자의 배치를 설명하기 위한 도면이다. 한편, 본 실시예에서는 제4 실시예에 따른 질화물계 반도체 발광 소자(600)가 실장된 경우에 대하여 언급하지만 본 발명은 그러한 구성으로 한정되지 않고, 앞서 언급한 본 발명의 제3 실시예에 따른 질화물계 반도체 발광 소자(500)가 실장되는 경우에도 동일하게 적용된다.

도 14에 도시된 바와 같이, 본 발명의 제4 실시예에 따른 질화물계 반도체 발광 소자(600)가 실장된 전자 소자는 발광 소자(600)와 인쇄회로기판(700) 및 이것들을 전기적으로 연결하는 솔더 범프(74a, 74b) 등의 결합수단을 포함한다. 솔더 범프(74a, 74b)는 발광 소자(600)의 p형 및 n형 전극(26, 27)과 인쇄회로기판(700)의 p형 및 n형 전극 패턴(72a, 72b)과의 사이에 배치된다. 도 15에서와 같이, 인쇄회로기판(700)의 p형 및 n형 전극 패턴(72a, 72b)은 금(Au) 등의 도전성 재료에 의해 소정 형상으로 인쇄회로기판의 주면상에 도포되어 형성된다. 도 15에서 참조부호 27a는 n형 전극 패드 영역을 나타내고, 참조부호 74c와 74d는 더미 솔더 범프(dummy solder bump)를 나타내며, 참조부호 600a는 발광 소자(600)가 놓여지는 위치를 나타낸다. 한편 도면에는 도시하지 않았지만, p형 및 n형 전극 패턴(72a, 72b)은 금(Au) 등의 도전성 재료를 이용한 와이어 본딩에 의해 주변 회로 또는 외부 회로와 전기적으로 연결될 수 있다.

이러한 구성에 의하면, 발광 소자 내에서 생성된 빛은 소자 내부에서 순환적으로 전반사되지 않고 대부분 소자 내의 활성영역을 통해 활성화되어 기판(20)의 상부면(20a)을 통해 방출된다(도 13b 참조). 다시 말하면, 통상의 발광소자에서 사파이어 기판의 두께는 질화물계 물질의 활성영역층의 두께보다 두껍기 때문에 경사부의 각도를 확보하기 상대적으로 쉽다. 또한 사파이어 기판의 굴절률이 질화물계 물질의 굴절률보다 낮기 때문에 빛의 전반사 횟수가 적다. 따라서 제1 실시예나 제2 실시예에서는 질화물계 물질의 활성영역층 내에서 빛이 여러차례 전반사되고 그 가운데 일부가 활성층에 흡수되는 반면, 본 실시예에서와 같이 발광 소자를 업사이드 다운 방식으로 인쇄회로기판 상에 실장하는 경우에는 활성층에 의해 흡수되 는 빛이 상대적으로 적기 때문에 광효율이 매우 높아진다. 이같이 본 발명에 의하면 발광 소자에서 생성된 빛을 최대한 바깥으로 뽑아내어 이용하는 것이 가능하다.

이와 같이 본 발명의 제4 실시예에 따른 질화물계 반도체 발광 소자(600)는 소정 모양의 전극 패턴(72a, 72b)이 형성된 인쇄회로기판(700) 상에 솔더 범프(solder bump; 74a, 74b) 등을 통해 플립칩 본딩(Filp-chip bonding) 되는 것

이 바람직하다. 더욱 바람직하게는 위의 제4 실시예에서 언급한 바와 같이 플립칩 본딩되는 발광 소자가 질화물계 반도체의 결정구조에 따른 수평 단면 구조-정삼각형 또는 정삼각형이 조합된 모양-를 갖고 동시에 레이저 가공에 의해 경사부를 갖도록 이루어진다.

이상의 실시예에서는 질화물계 반도체 발광 다이오드에 대하여 설명하였으나, 본 발명은 정육각기둥 형태를 가진 질화물계 반도체를 이용하여 제조되는 모든 소자들에 적용될 수 있으므로, 단지 발광 다이오드(LED) 뿐만 아니라 레이저 다이오드(LD) 등의 모든 질화물계 반도체 발광 소자와 전자 소자들의 제작시 칩 생산수율을 최대로 높여줄 수 있는 것이다.

발명의 효과

상기한 바와 같이 본 발명에 의하면, 반도체를 이용한 모든 발광 소자 및 전자 소자들의 칩 제작시, 절삭 공구를 사용하지 않고 레이저 가공을 통한 흠집내기(Scribing)와 절개(Cleaving) 방법을 이용하여 칩을 만들기 때문에 절삭과정을 통해 소모되는 칩의 양을 거의 없게 할 수 있다. 따라서 종래의 기술에 비해 칩 생산수율을 크게 증가시킬 수 있다는 이점이 있다.

뿐만 아니라 발광 소자, 특히 발광 다이오드를 그 측면에 경사부가 구비된 구조로 제조할 경우, 영구적인 전반사 현상을 제거하여 발생한 빛의 양을 최대한 바깥으로 뽑아내어 이용할 수 있게 함으로써 광 이용효율의 극대화를 이룰 수 있으며, 나아가 전력대비 광 이용효율이 증가함에 따라 투입 전류량을 줄여서 발광 소자 자체의 수명을 연장할 수도 있다.

더욱이 질화물계 반도체 발광 소자를 이용하는 경우, 질화물계 반도체의 정육각형(Hexagonal) 기둥 형태의 결정 구조에 따라 소자의 수평 단면 구조가 형성되도록 제조하면서 동시에 레이저 가공을 통한 흠집내기를 한 후 절개하는 과정을 통해 그 측면에 경사부를 형성함으로써, 소자 내부의 순환적인 전반사 현상을 제거하여 광 이용효율을 더욱 극대화시키고 동시에 칩 생산수율을 더욱 크게 증가시킬 수 있다는 이점이 있다.

본 명세서에서 기술된 실시예들은 단지 설명의 목적으로 기재된 것이며, 따라서 당업자들에 의한 이들의 다양한 변형 내지는 사소한 변경은 본 발명의 기술적 사상의 범주에 포함되며 나아가 본 특허청구범위에 속하는 것으로 이해되어야 할 것이다.

(57) 청구의 범위

청구항 1.
기판(20)상에 질화물계 반도체로 된 활성층(22)과, 이 활성층(22)의 상부 및 하부에 각각 형성된 질화물계 반도체로 된 p형 및 n형 도핑층(24, 21)을 구비하여 이루어진 질화물계 반도체 발광 소자(200; 300; 400)에 있어서,

상기 활성층(22)과 상기 도핑층(21, 24)이 형성되어 있는 기판(20)의 상부측 외측면 중 적어도 어느 하나의 외측면은, 레이저 가공을 이용한 흠집내기(Scribing) 공정에 의해 경사지게 잘려지고 상기 기판(20)의 상부측 방향으로 갈수록 단면적이 감소하는 모양으로 이루어진 경사부(30)를 포함하는 것을 특징으로 하는 질화물계 반도체 발광 소자.

청구항 2.
기판(20)상에 질화물계 반도체로 된 활성층(22)과, 이 활성층(22)의 상부 및 하부에 각각 형성된 질화물계 반도체로 된 p형 및 n형 도핑층(24, 21)을 구비하여 이루어진 질화물계 반도체 발광 소자(500; 600)에 있어서,

상기 기판(20)의 적어도 어느 하나의 외측면은, 레이저 가공을 이용한 흠집내기(Scribing) 공정에 의해 경사지게 잘려지고 상기 활성층(22)과 상기 도핑층(21, 24)이 형성되어 있는 방향의 반대쪽 방향으로 갈수록 단면적이 감소하는 모양으로 이루어진 경사부(40)를 포함하는 것을 특징으로 하는 질화물계 반도체 발광 소자.

청구항 3.
제1항 또는 제2항에 있어서,

상기 레이저 가공은 펨토세컨드 레이저(Femtosecond Laser)를 이용하는 것을 특징으로 하는 질화물계 반도체 발광 소자.

청구항 4.
제3항에 있어서,

상기 레이저 가공은 진공 분위기 하에서 행해지는 것을 특징으로 하는 질화물계 반도체 발광 소자.

청구항 5.
제1항 또는 제2항에 있어서,

질화물계 반도체의 결정 구조에 따른 정삼각형을 기본으로 하여, 이들의 조합으로 이루어진 정삼각형, 평행사변형, 사다리꼴 중 어느 하나의 수평 단면 구조를 갖는 것을 특징으로 하는 질화물계 반도체 발광 소자.

청구항 6.
기판(20)상에 질화물계 반도체로 된 활성층(22)과, 이 활성층(22)의 상부 및 하부에 각각 형성된 질화물계 반도체로 된 p형 및 n형 도핑층(24, 21)을 포함하여 이루어진 질화물계 반도체 발광 소자(200; 300; 400)의 제조방법에 있어서,

상기 질화물계 반도체 발광 소자(200; 300; 400)가 다수 형성되어 있는 웨이퍼를 개개의 칩으로 자르는 과정에서, 상기 활성층(22)과 상기 도핑층(21, 24)의 외측면에 경사부(30)가 형성되도록 레이저 가공을 이용하여 상기 웨이퍼에 흠집내기(Scribing)를 행하는 흠집내기 공정; 및

상기 흠집내기 공정에 의해 형성된 직선들을 따라 절개(Cleaving)를 행하는 절개 공정을 포함하는 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법.

청구항 7.
기판(20)상에 질화물계 반도체로 된 활성층(22)과, 이 활성층(22)의 상부 및 하부에 각각 형성된 질화물계 반도체로 된 p형 및 n형 도핑층(24, 21)을 포함하여 이루어진 질화물계 반도체 발광 소자(500; 600)의 제조방법에 있어서,

상기 질화물계 반도체 발광 소자(500; 600)가 다수 형성되어 있는 웨이퍼를 업사이드 다운(upside-down) 방식으로 개개의 칩으로 자르는 과정에서, 상기 기판(20)의 외측면에 경사부(40)가 형성되도록 레이저 가공을 이용하여 상기 웨이퍼에 흠집내기(Scribing)를 행하는 흠집내기 공정; 및

상기 흠집내기 공정에 의해 형성된 직선들을 따라 절개(Cleaving)를 행하는 절개 공정을 포함하는 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법.

청구항 8.
제6항 또는 제7항에 있어서,

상기 레이저 가공은 펨토세컨드 레이저(Femtosecond Laser)를 이용하는 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법.

청구항 9.
제8항에 있어서,

상기 레이저 가공은 진공 분위기 하에서 행해지는 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법.

청구항 10.
제8항에 있어서,

상기 레이저 가공은 레이저 가공시 생성되는 부산물을 제거하기 위한 압축 공기 분사 또는 화학 물질 주입 과정과 함께 행해지는 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법.

청구항 11.
제6항 또는 제7항에 있어서,

상기 흠집내기 공정은, 상기 질화물계 반도체의 결정 구조를 따라 제1의 간격을 두고 제1 방향으로 다수의 흠집내기(Scribing)를 행하는 제1 흠집내기 공정과; 상기 질화물계 반도체의 결정 구조를 따라 제2의 간격을 두고 상기 제1 방향과 60° 의 각도를 이루는 제2 방향으로 다수의 흠집내기를 행하는 제2 흠집내기 공정; 및 상기 질화물계 반도체의 결정 구조를 따라 제3의 간격을 두고 상기 제1 방향 및 제2 방향과 각각 60° 의 각도를 이루는 제3 방향으로 다수의 흠집내기를 행하는 제3 흠집내기 공정을 포함하고,

상기 절개 공정은 상기 제1, 제2 및 제3 흠집내기 공정에 의해 형성된 직선들을 따라 절개(Cleaving)를 행하는 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법.

청구항 12.
제11항에 있어서,

상기 제1의 간격과 제2의 간격 및 제3의 간격은 모두 동일한 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법.

청구항 13.
제11항에 있어서,

상기 제1의 간격과 제2의 간격은 서로 동일하며, 상기 제3의 간격은 상기 제1의 간격 및 제2의 간격의 1/2인 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법.

청구항 14.
제6항 또는 제7항에 있어서,

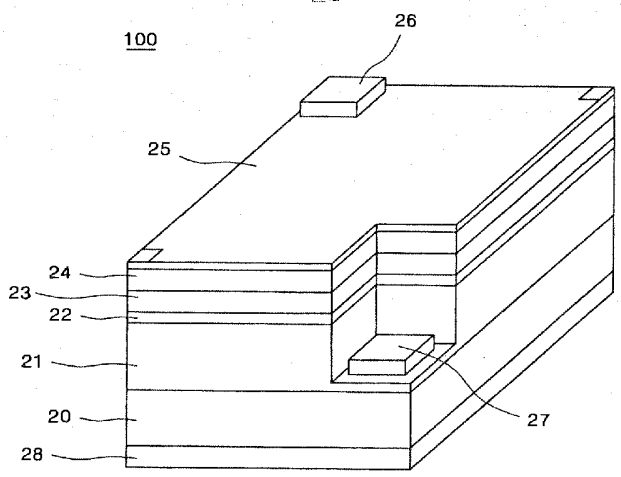
상기 흠집내기 공정은, 상기 질화물계 반도체의 결정 구조를 따라 제1의 간격을 두고 제1 방향으로 다수의 흠집내기(Scribing)를 행하는 제1 흠집내기 공정과; 상기 질화물계 반도체의 결정 구조를 따라 제2의 간격을 두고 상기 제1 방향과 60° 의 각도를 이루는 제2 방향으로 다수의 흠집내기를 행하는 제2 흠집내기 공정을 포함하고,

상기 절개 공정은 상기 제1 및 제2 흠집내기 공정에 의해 형성된 직선들을 따라 절개(Cleaving)를 행하는 절개 공정을 포함하며,

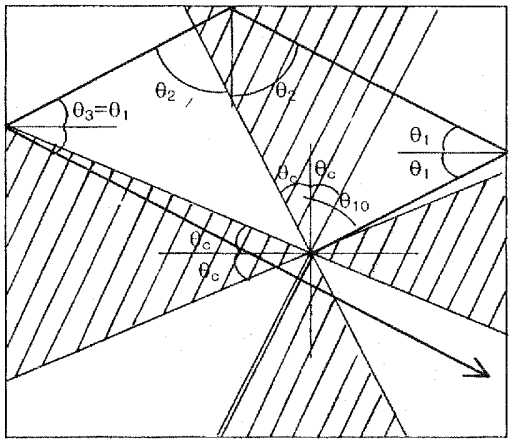
상기 제1의 간격과 상기 제2의 간격은 m:n(m, n은 양의 정수)의 비율을 갖는 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법.

도면

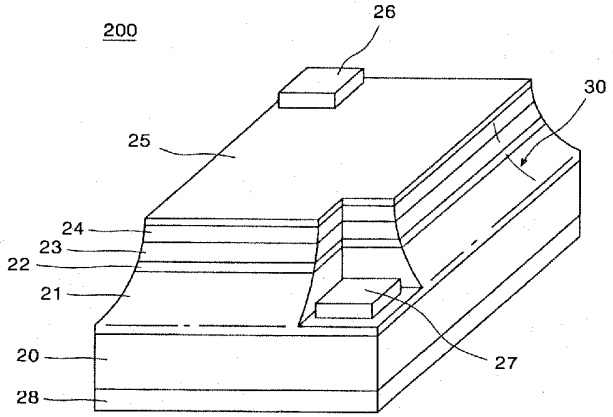
도면1



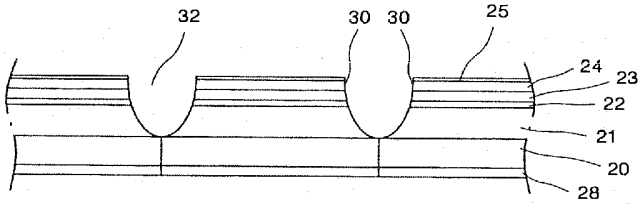
도면2



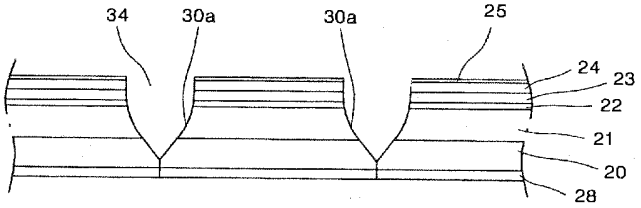
도면3



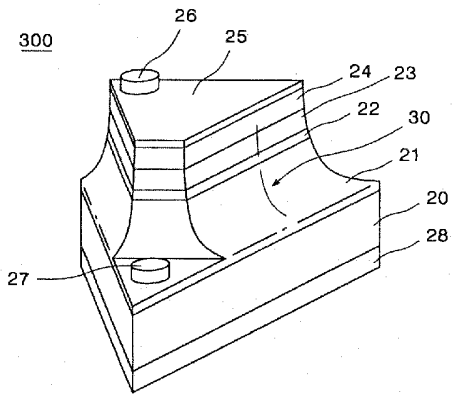
도면4



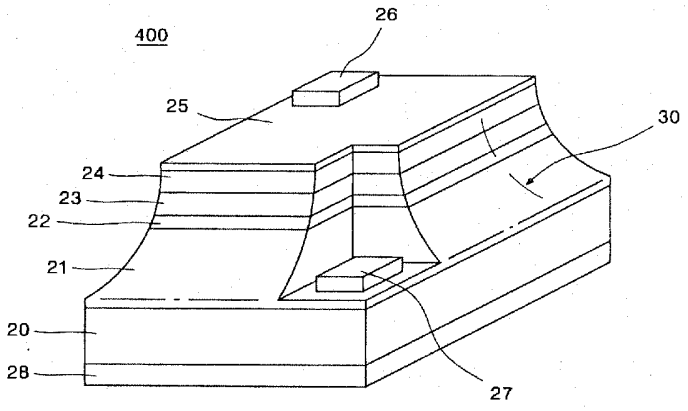
도면5



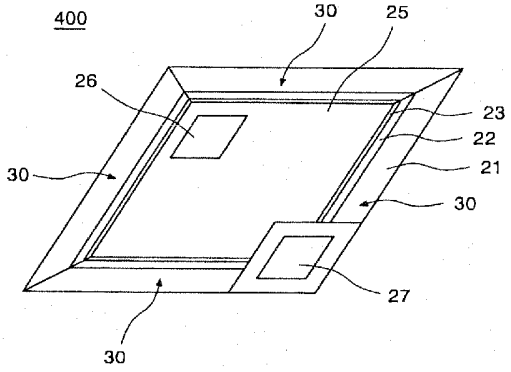
도면6



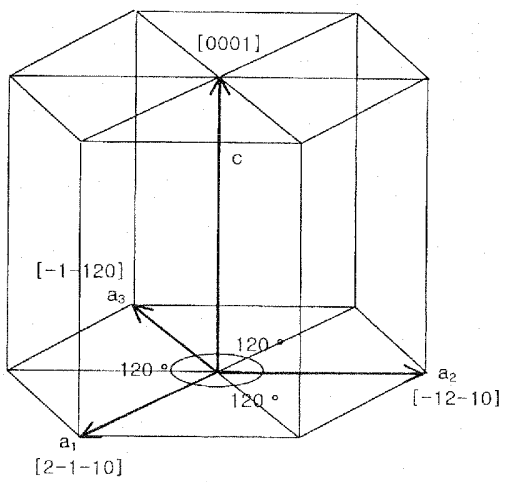
도면7a



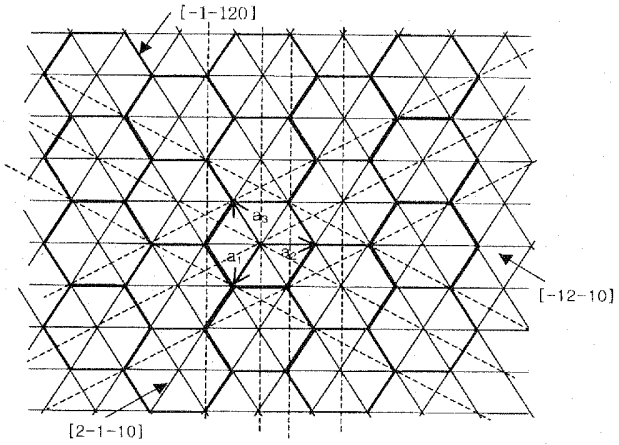
도면7b



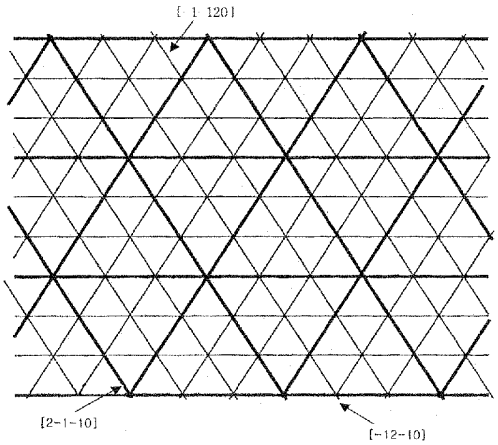
도면8



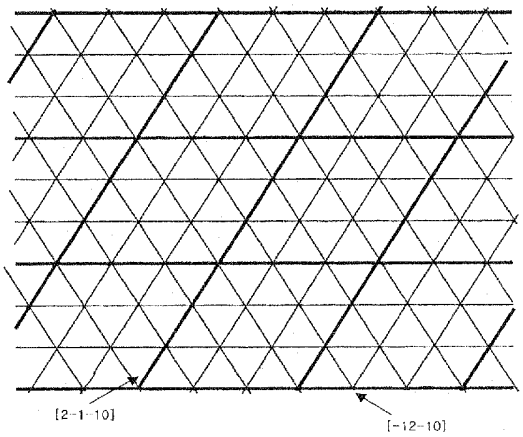
도면9



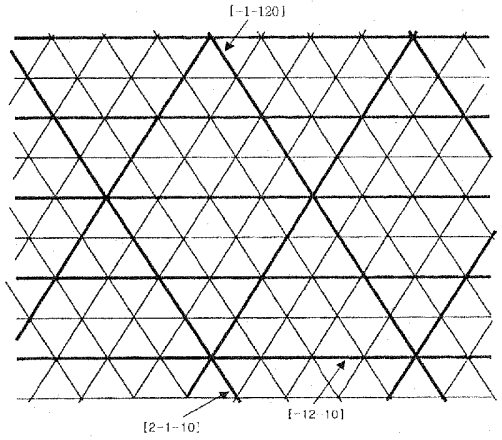
도면10a



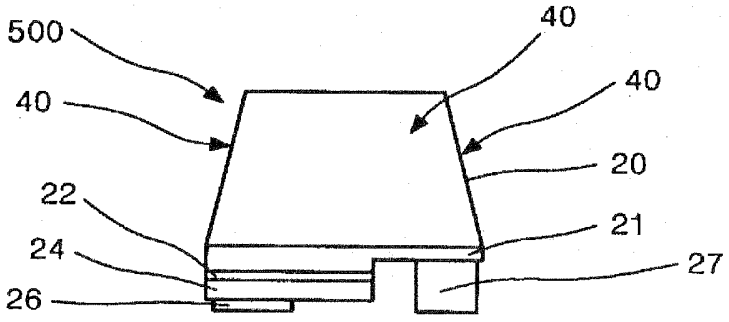
도면10b



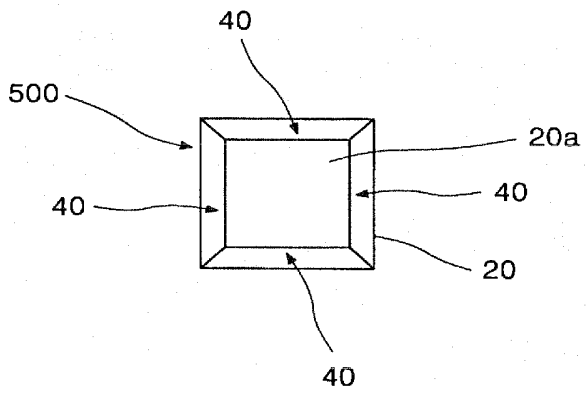
도면10c



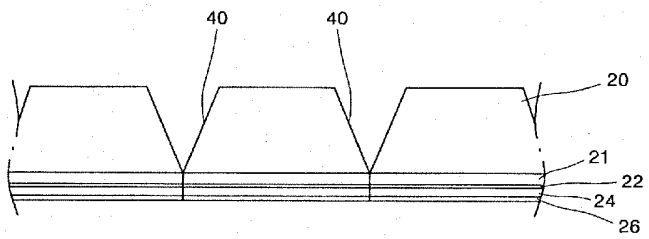
도면11a



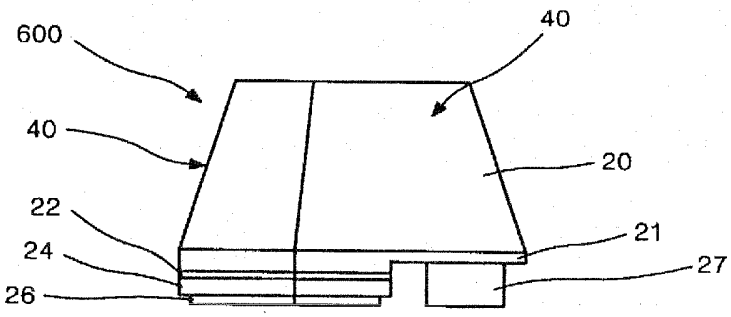
도면11b



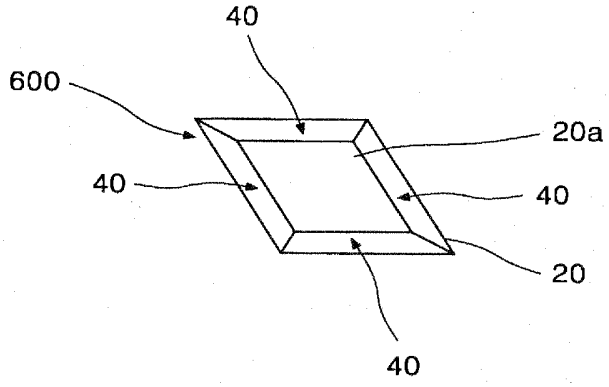
도면12



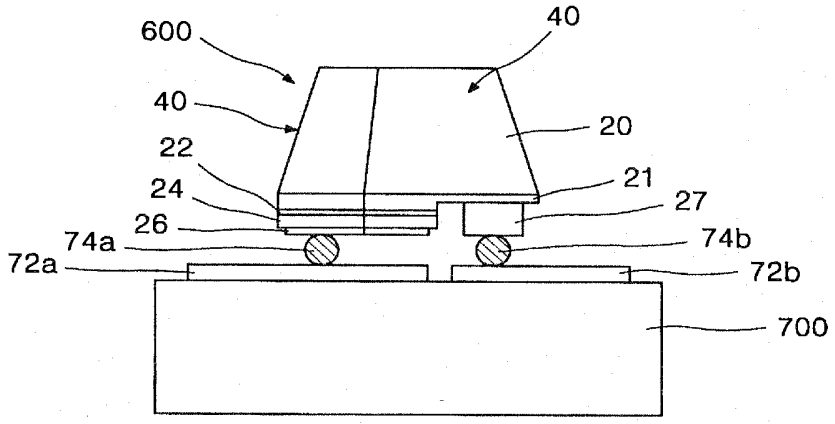
도면13a



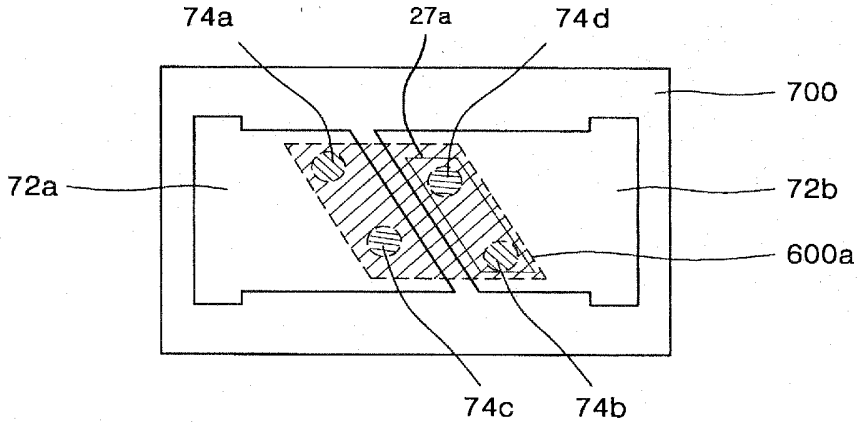
도면13b



도면14


600
40
40
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22
21
24
27
26
74a
74b
72a
72b
700

도면15


74a
27a
74d
700
72a
72b
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74c
74b

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jong Lam Lee
Filer:	Gregg James Palmer/Sue Lukas
Attorney Docket Number:	3576-053
Filed as Large Entity	

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
National Stage Fee	1631	1	310	310
Natl Stage Search Fee - Report provided	1642	1	410	410
National Stage Exam - all other cases	1633	1	210	210
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**930**

Electronic Acknowledgement Receipt

EFS ID:	2642146
Application Number:	11993965
International Application Number:	PCT/KR06/02427
Confirmation Number:	2191
Title of Invention:	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	20575
Filer:	Gregg James Palmer/Sue Lukas
Filer Authorized By:	Gregg James Palmer
Attorney Docket Number:	3576-053
Receipt Date:	26-DEC-2007
Filing Date:	
Time Stamp:	20:39:48
Application Type:	U.S. National Stage under 35 USC 371

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Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$930
RAM confirmation Number	2994
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)

1		3576_053_Application.pdf	2933422 42e0aebb0a396c33ab7a2fa2b0a1f0e28a5a9d4d	yes	38
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Specification		1	32	
	Claims		33	37	
	Abstract		38	38	
Warnings:					
Information:					
2	Application Data Sheet	3576_053_ADS.pdf	1332143 ad23863498449ea3f89c6c9af19585fa4ebfdf5b	no	6
Warnings:					
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3	Transmittal of New Application	3576_053_Transmittal.pdf	347420 576af33fc6c19d245e05a827d39d54ba48a63546	no	3
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4	Preliminary Amendment	3576_053_Amendment.pdf	325672 a41d89ee591ad2a4da2b1f7fb2d9d02688263659	no	6
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5	Oath or Declaration filed	3576_053_Declaration.pdf	269938 e95deab337ae3b5a5ed382b2236f63d8cd146d0b	no	4
Warnings:					
Information:					
6	Drawings-only black and white line drawings	3576_053_Drawings.pdf	607621 1b0dc992d87c9ec8891deb1293a206b40bb635a7	no	11
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7	Miscellaneous Incoming Letter	WO2006137711.pdf	1736776 6d37f6cae656699d08d97c2d328aecf3fac67c90	no	35
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8	Information Disclosure Statement (IDS) Filed	3576_053_IDS.pdf	978591 37971d868f869e6aa2b7ef9ab90d96f9c257e79a	no	4
Warnings:					
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9	Foreign Reference	KR2003-52499.pdf	554761 ce4485d383edb5369b6430a47c35b82e032a8f0a	no	7
Warnings:					
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10	Foreign Reference	KR2004-5098.pdf	2201079 c3b7953cc906ecbba8d4c75c88d2549f714b19ad	no	20
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11	Fee Worksheet (PTO-06)	fee-info.pdf	8436 1b5dc2ab273c8508b5d6bc5728f0248e0ed1bd88	no	2
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LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

Field of Invention

The present invention relates to a light emitting device and a method of manufacturing the same. More particularly, the present invention relates to a nitride based semiconductor light emitting device with enhanced luminous efficiency and brightness and a method of manufacturing the light emitting device.

Description of the Related Art

A light emitting device refers to an element in which minority carriers (electrons or holes) injected using a p-n junction structure of a semiconductor are produced and certain light is emitted due to recombination of the carriers. A light emitting source is formed from any one or combination of compound semiconductor materials such as GaAs, AlGaAs, GaN, InGaN and AlGaInP, so that a variety of colors can be implemented. For example, a red light emitting device may be formed from GaAsP or the like; a green light emitting device may be formed from GaP, InGaN or the like; a blue light emitting device may be formed using an InGaN/GaN double hetero structure; and a UV light emitting device may be formed using an AlGaN/GaN or AlGaN/AlGaN structure.

In particular, GaN has a direct bandgap of 3.4eV at a normal temperature and a direct energy bandgap of 1.9eV (InN) to 3.4eV (GaN) or 6.2eV (AlN) by combining with a substance such as InN or AlN. Thus, GaN is a substance with great applicability to an optical element due to its broad wavelength range from visible light to ultraviolet light. Since the wavelength can be adjusted in such a manner, full-color implementation can be

made by means of red, green and blue light emitting devices with a short wavelength range, so that the applicability to a general illumination market as well as a display device market is expected to be greatly increased.

Light emitting devices have characteristics of lower power consumption, longer lifespan, better installation in a narrow space and stronger resistance against vibration as compared with existing bulbs or fluorescent lamps. Since the light emitting devices are used as display devices and backlights and have superior characteristics in view of the reduction in power consumption and the durability, many studies for applying the light emitting devices to a general illumination field have been recently conducted. In the future, their applicability is expected to extend to a backlight of a large-sized LCD-TV, a vehicle headlight and general illumination. To this end, it is necessary to improve luminous efficiency of light emitting devices, solve a heat dissipation problem, and achieve high brightness and output of the light emitting devices.

Many techniques for enhancing the performance of light emitting devices have been currently developed. There are various indexes indicating the performance of light emitting devices, such as luminous efficiency (lm/W), internal quantum efficiency (%), external quantum efficiency (%) and extraction efficiency (%). The extraction efficiency is determined as a ratio of electrons injected into the light emitting device to photons emitted to the outside of the light emitting device. That is, the light emitting device becomes bright as the extraction efficiency becomes high. Since the extraction efficiency of the light emitting device is much influenced by the shape and surface pattern of a chip, the structure of a chip and a packaging type, careful attention should be paid when designing the light emitting device.

Fig. 1 is a sectional view showing a conventional light emitting device with a

horizontal structure.

Referring to Fig. 1, the light emitting device comprises a substrate 1, an N-type semiconductor layer 2 formed on the substrate 1, an active layer 3 formed on a portion of the N-type semiconductor layer 2 and a P-type semiconductor layer 4. That is, after the N-type semiconductor layer 2, the active layer 3 and the P-type semiconductor layer 4 have been sequentially formed on the substrate 1, predetermined regions of the P-type semiconductor layer 4 and the active layer 3 are etched to expose a portion of the N-type semiconductor layer 2. Then, a predetermined voltage is applied to top surfaces of the exposed N-type semiconductor layer 2 and the P-type semiconductor layer 4.

Fig. 2 is a sectional view showing a conventional light emitting device with a flip chip structure.

Referring to Fig. 2, the light emitting device comprises an N-type semiconductor layer 2, an active layer 3 and a P-type semiconductor layer 4, which are sequentially formed on a base substrate 1. The light emitting device further comprises a submount substrate 5 onto which the base substrate 1 is flip-chip bonded using metal bumps 8 and 9. To this end, the N-type semiconductor layer 2, the active layer 3 and the P-type semiconductor layer 4 are sequentially formed on the predetermined substrate 1, and portions of the P-type semiconductor layer 4 and the active layer 3 are etched to expose the N-type semiconductor layer 2 such that a light emitting cell can be formed. Further, the additional submount substrate 5 is prepared to form first and second electrodes 6 and 7 thereon, and the P-type and N-type metal bumps 8 and 9 are then formed on the first and second electrodes 6 and 7, respectively. Thereafter, the light emitting cell is bonded with the submount substrate 5 such that P and N electrodes of the light emitting cell are bonded with the P-type and N-type metal bumps 8 and 9, respectively, to fabricate a light emitting device. Since such a conventional

light emitting device with a flip chip structure has high heat dissipation efficiency and hardly has shield of light, there is an advantage in that its light efficiency is increased by 50% or more as compared with a conventional light emitting device. Further, since a gold wire for driving a light emitting device is not necessary, many applications to a variety of small-sized packages can be considered.

Light produced from a light emitting layer of a light emitting device is emitted from all the surfaces of a chip, and light extraction efficiency is generally determined by a critical angle of light. However, when the conventional light emitting device is etched to expose an N-type semiconductor layer, side surfaces of the P-type semiconductor layer and the active layer are vertically processed such that a portion of light produced within the light emitting device is totally reflected on the etched surface that is processed vertically from a horizontal plane. Then, a considerable amount of light to be totally reflected is not emitted to the outside but dissipated within the light emitting device due to the internal reflection. That is, there is a problem in that luminous efficiency in which electric energy is converted into light energy and the light is then emitted to the outside of a light emitting device is low.

SUMMARY OF THE INVENTION

The present invention is conceived to solve the aforementioned problems. Accordingly, an object of the present invention is to provide a light emitting device for emitting light with high luminous intensity and brightness by enhancing characteristics of luminous efficiency, external quantum efficiency, extraction efficiency and the like and improving reliability, and a method of manufacturing the light emitting device.

According to an aspect of the present invention for achieving the objects, there is provided a light emitting device, comprising a plurality of light emitting cells each including

an N-type semiconductor layer and a P-type semiconductor layer formed on a portion of the N-type semiconductor layer on a substrate. The N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell may be connected to each other, and a side surface including the N-type or P-type semiconductor layer of the light emitting cell has a slope of 20 to 80° from a horizontal plane. The light emitting device may further comprise a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell, a transparent electrode layer on the P-type semiconductor layer, and P-type and N-type ohmic metal layers containing Cr or Au on the P-type and N-type semiconductor layers, respectively.

According to another aspect of the present invention, there is provided a light emitting device comprising a substrate formed with a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on the N-type semiconductor layer and a submount substrate flip-chip bonded onto the substrate. Preferably, the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including at least the P-type semiconductor layer of the light emitting cell has a slope of 20 to 80°from a horizontal plane. The light emitting device may further comprise a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

According to further aspect of the present invention, there is provided a method of manufacturing a light emitting device, comprising the steps of sequentially forming N-type and P-type semiconductor layers on a substrate; forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal

plane, on the P-type semiconductor layer; and removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern.

According to still further aspect of the present invention, there is a method of manufacturing a light emitting device comprising the steps of removing a portion of the N-type semiconductor layer exposed due to the removal of the P-type semiconductor layer to form a plurality of light emitting cells; and connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire.

According to still further aspect of the present invention, there is a method of manufacturing a light emitting device comprising the step of flip-chip bonding the substrate onto an additional submount substrate after the step of removing the P-type semiconductor layer and the etching mask pattern. The method of manufacturing a light emitting device may further comprise the steps of removing a portion of the N-type semiconductor layer exposed through the removal of the P-type semiconductor layer to form a plurality of light emitting cell; and connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire, after the step of removing the P-type semiconductor layer and the etching mask pattern.

The step of forming the plurality of light emitting cells may comprise the steps of forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; removing the N-type and P-type semiconductor layers exposed through the etching mask pattern to form a plurality of light emitting cells; and removing the etching mask pattern.

The N type semiconductor layer of one light emitting cell and the P type semiconductor layer of another adjacent light emitting cell may be connected with the

conductive wire through a bridge or step coverage process.

A photoresist with a thickness of 3 to 50μm may be used in the step of forming the etching mask pattern. The step of forming the etching mask pattern may comprise the steps of: applying the photoresist onto the P-type semiconductor layer; light exposing the photoresist in accordance with a predetermined mask pattern; and developing the light-exposed photoresist without a baking process after the light exposure. The step of forming the etching mask pattern may comprise the steps of: applying the photoresist onto the P-type semiconductor layer; light exposing the photoresist in accordance with a predetermined mask pattern; hard baking the light-exposed photoresist at a temperature of 100 to 140°C; and developing the hard-baked photoresist.

After the step of removing the P-type semiconductor layer and the etching mask pattern, the method of manufacturing a light emitting device may further comprise the steps of removing a rear surface of the substrate at a certain thickness; and depositing Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof onto the rear surface of the substrate.

In a light emitting device and a method of manufacturing the same according to the present invention, light produced from a side surface of a semiconductor layer, which is not perpendicular to but inclined at a predetermined slop from a horizontal plane, is not totally reflected but emitted to the outside of the light emitting device. Therefore, more enhanced characteristics of light extraction efficiency, external quantum efficiency, luminous efficiency or the like can be obtained. Further, a light emitting device of the present invention emits light with high luminous intensity and brightness and can be applied to a variety of products in which a superior light characteristic is necessary.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will become apparent from the following description of preferred embodiments given in conjunction with the accompanying drawings, in which:

Figs. 1 and 2 are sectional views showing conventional light emitting devices, respectively;

Fig. 3 is a conceptual sectional view illustrating a light emitting device with a horizontal structure according to the present invention;

Figs. 4 and 5 are sectional views illustrating a process of manufacturing a light emitting device according to a first embodiment of the present invention;

Figs. 6 to 9 are sectional views illustrating a process of manufacturing a light emitting device according to a second embodiment of the present invention;

Figs. 10 to 13 are sectional views illustrating a process of manufacturing a light emitting device according to a third embodiment of the present invention;

Figs. 14 to 17 are sectional views illustrating a process of manufacturing a light emitting device according to a fourth embodiment of the present invention;

Fig. 18 is a conceptual sectional view illustrating a light emitting device with a flip chip structure according to the present invention;

Figs. 19 to 23 are sectional views illustrating a process of manufacturing a light emitting device according to a fifth embodiment of the present invention;

Figs. 24 to 28 are sectional views illustrating a process of manufacturing a light emitting device according to a sixth embodiment of the present invention;

Fig. 29 is a sectional view showing a seventh embodiment according to the present invention; and

Figs. 30 and 31 are conceptual sectional views illustrating a difference between effects of the light emitting devices according to the prior art and the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, a light emitting device and a manufacturing method thereof according to the present invention will be described in detail with reference to the accompanying drawings. However, the present invention is not limited to the embodiments set forth herein but can be implemented in different forms. Rather, the preferred embodiments are merely provided to allow the present invention to be completely described herein and to fully convey the scope of the invention to those skilled in the art.

Fig. 3 is a conceptual sectional view illustrating a light emitting device with a horizontal structure according to the present invention.

Referring to Fig. 3, the light emitting device comprises a substrate 10, and an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40, which are sequentially formed on the substrate 10. Each of side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 has a slope of 80 to 20¡Æ from a horizontal plane such that a critical angle of light can be changed by such surfaces and light can be easily extracted. Therefore, luminous efficiency of a light emitting device can be improved.

Figs. 4 and 5 are sectional views illustrating a process of manufacturing a light emitting device according to a first embodiment of the present invention.

Referring to Fig. 4, an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40 are sequentially formed on a substrate 10.

The substrate 10 refers to a general wafer used for fabricating a light emitting device

and is made of at least any one of Al_2O_3, SiC, ZnO, Si, GaAs, GaP, $LiAl_2O_3$, BN, AlN and GaN. In this embodiment, a crystal growth substrate made of sapphire is used.

A buffer layer (not shown) may be further formed on the substrate 10 to reduce lattice mismatch between the substrate 10 and the subsequent layers upon growth of crystals. The buffer layer may contain GaN or AlN that is a semiconductor material.

The N-type semiconductor layer 20 is a layer in which electrons are produced and is preferably made from GaN doped with N-type impurities. However, the N-type semiconductor layer 20 is not limited thereto but may use a material layer having a variety of semiconductor properties. The N-type semiconductor layer 20 including N-type $Al_xGa_{1-x}N(0\leq x\leq 1)$ is formed in this embodiment. Further, the P-type semiconductor layer 40 is a layer in which holes are produced and is preferably made from GaN doped with P-type impurities. However, the P-type semiconductor layer 40 is not limited thereto but may use a material layer with a variety of semiconductor properties. The P-type semiconductor layer 40 including P-type $Al_xGa_{1-x}N(0\leq x\leq 1)$ is formed in this embodiment. Moreover, InGaN may be used as the semiconductor layer. Further, each of the N-type and P-type semiconductor layers 20 and 40 may be formed as a multiple layer.

The active layer 30 has a predetermined bandgap and is a region where a quantum well is formed so that electrons and holes are recombined. The active layer 30 may contain InGaN. The wavelength of light emitted through the combination of electrons and holes varies according to the kind of a material constituting the active layer 30. Therefore, it is preferred that a semiconductor material contained in the active layer 30 be controlled depending on a target wavelength.

The aforementioned material layers are formed through a variety of deposition and growth methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD

(Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like.

Thereafter, portions of the P-type semiconductor layer 40 and the active layer 30 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 20. An etching mask pattern is formed on the P-type semiconductor layer 40, and the P-type semiconductor layer 40 and the active layer 30 are then removed through a dry or wet etching process to expose the N-type semiconductor layer 20.

Generally, in order to perform the etching process, a photoresist has been applied onto a top surface of the P-type semiconductor layer 40 at a thickness of 1 to 2μm, and then soft-baked at a temperature of 80 to 90°C is performed. Next, an exposure process in which light in a UV range is irradiated through a predetermined photo mask to transfer a pattern formed on the mask to the applied photoresist is executed. Thereafter, the photoresist is hard-baked at a temperature of 100 to 120°C, and a developing process in which the photoresist at a portion with relatively weak combination through the exposure process is melted using a solvent is executed. A predetermined etching mask pattern is formed on the P-type semiconductor layer 40 through the above process.

However, in this embodiment, the photoresist is applied at a thickness of 3 to 50μm which is thicker as compared with the prior art when the etching mask pattern is formed, and the exposure process is performed after the soft-baking. Next, if the photoresist is directly developed without the hard-baking, a developed side surface of the remaining photoresist is formed into an inclined surface not perpendicular (90°) to but inclined at a predetermined slope from a horizontal plane. Subsequently, if exposed regions of the P-type semiconductor layer 40, the active layer 30 and the predetermined N-type semiconductor layer 20 are etched using the etching mask pattern with such a slope of the side surface, the side surfaces of the

etched P-type semiconductor layer 40, active layer 30 and N-type semiconductor layer 20 can be similarly formed into an inclined surface not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane.

That is, after the photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 40 of Fig. 4 and light-exposed, a developed etching mask pattern is immediately formed without the hard-baking. The P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer 20. A portion of the exposed N-type semiconductor layer 20 may be further removed. Thereafter, if the etching mask pattern is removed, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured as shown in Fig. 5.

Alternatively, after a photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 40 of Fig. 4 and light-exposed, hard-baking may be performed. In such a case, if the photoresist is hard-baked at a temperature of 100 to 140°C and then developed, the side surface of the developed photoresist may be etched to have a slope of 80 to 20° from a horizontal plane. For example, in a case where the hard-baking is performed at a temperature of 100°C, an etching mask pattern with a slope of about 80° from the horizontal plane can be obtained, and the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 can have a slope of about 80° from the horizontal plane using the etching mask pattern. Further, in a case where the hard-baking is performed at a temperature of 140°C, an etching mask pattern with a slope of about 20° from the horizontal plane can be obtained, and the side surfaces of the P-type

semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 can have a slope of about 20° from the horizontal plane using the etching mask pattern.

The etching mask pattern, which the photoresist with a thickness of 3 to 50μm has been light-exposed and hard-baked at a temperature of 100 to 140°C and then developed in such a manner, can be used such that the side surfaces of the etched the P-type semiconductor layer 40, active layer 30 and predetermined N-type semiconductor layer 20 have a slope of 80 to 20¡Æ from a horizontal plane similarly to the etching mask pattern. Then, light produced within a light emitting layer is not totally reflected on the etched side surface with a variety of slopes but emitted to the outside of a light emitting device.

A transparent electrode layer may be further formed on the P-type semiconductor layer 40 to reduce resistance of the P-type semiconductor layer 40 and enhancing transmittance of light, and an additional ohmic metal layer may be further formed on the P-type semiconductor layer 40 or the exposed N-type semiconductor layer 20 to facilitate current supply. The transparent electrode layer may be made of ITO (Indium Tin Oxide), ZnO or a transparent conductive metal, and the ohmic metal layer may be made of Cr or Au. Further, for the application of voltage, a P-type electrode may be further formed on the P-type semiconductor layer 40 and an N-type electrode may be further formed on the N-type semiconductor layer 20.

Further, in order to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10.

As can be seen from this figure, a plurality of light emitting devices may be fabricated on a single substrate 10, which is cut into the individual light emitting devices.

At this time, portions A shown in Fig. 5 are cutting portions used for individually cutting the plurality of light emitting devices.

Accordingly, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 is not perpendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured.

The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto. Various processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes.

Figs. 6 to 7 are sectional views illustrating a process of manufacturing a light emitting device according to a second embodiment of the present invention.

The second embodiment of the present invention is almost the same as the first embodiment. In the second embodiment, however, there is provided a light emitting device in which a plurality of light emitting cells are connected in series, parallel or series-parallel in a wafer level to reduce the size of the device, and they can be driven at proper voltage and current to be used for illustration purpose and can also be driven even with an AC power source. Descriptions overlapping with the previous embodiment will be omitted herein.

Referring to Fig. 6, an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40 are sequentially formed on a substrate 10 through various deposition methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like. A buffer layer may be further formed on the substrate 10 to reduce lattice mismatch between the

substrate 10 and the subsequent layers upon growth of crystals.

Thereafter, portions of the P-type semiconductor layer 40 and the active layer 30 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 20. That is, after the photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 40 of Fig. 6 and light-exposed, it is developed without hard-baking to form an etching mask pattern. The P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer 20. A portion of the exposed N-type semiconductor layer 20 may be further removed. Thereafter, if the etching mask pattern is removed, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured as shown in Fig. 7.

Alternatively, after a photoresist has been applied in a thickness of 3 to 50μm on the P-type semiconductor layer 40 of Fig. 6 and light-exposed, it is hard-baked at a temperature of 100 to 140°C and developed such that an etching mask pattern can be formed. After the P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, have been etched, the etching mask pattern is removed such that the side surfaces of the etched P-type semiconductor layer 40 and active layer 30 can have a variety of slopes of 80 to 20°.

Next, in order to form a plurality of light emitting cells on the substrate 10, predetermined regions of the exposed N-type semiconductor layer 20 are removed such that a portion of the substrate 10 can be exposed. To this end, a predetermined mask pattern is formed on all the portions except the predetermined regions where the substrate 10 will be

exposed, and regions of the N-type semiconductor layer 20 that are exposed through the mask pattern are then etched such that the plurality of light emitting cells can be electrically isolated from one another as shown in Fig. 8. At this time, the mask pattern whose side surface is inclined through the aforementioned process is formed and then used to etch the exposed N-type semiconductor layer 20 such that the side surface of the N-type semiconductor layer 20 in which the plurality of light emitting cells are separated from one another is not perpendicular to but inclined at a predetermined slope from a horizontal plane.

Referring to Fig. 9, the N-type semiconductor layer 20 of a light emitting cell and the P-type semiconductor layer 40 of the adjacent light emitting cell are connected through a predetermined wiring process. That is, the exposed N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent light emitting cell are connected through a wire 60. At this time, the conductive wire 60 for electrically connecting the N-type and P-type semiconductor layers 20 and 40 are formed through a bridge process.

The aforementioned bridge process is also called an air-bridge process. In the air-bridge process, a photosensitive liquid is applied between chips to be connected with each other through a photo process and developed to form a photoresist pattern, a material such as metal is first formed into a thin film on the photoresist pattern through a vacuum vapor deposition method or the like, and a conductive material containing gold (Au) is applied at a predetermined thickness onto the thin film through an electroplating, electroless plating or metal vapor deposition method. Thereafter, if the photoresist pattern is removed with a solution of a solvent or the like, a lower portion of the conductive material is completely removed, and thus, only the bridge-shaped conductive material is formed in a space between the adjacent light emitting cells.

The wire 60 may be made of not only metal but also all kinds of conductive materials. It will be apparent that a silicone compound doped with impurities may be used.

Further, in order to apply an external voltage to the light emitting device, a P-type bonding pad 50 is formed on the P-type semiconductor layer 40 of the light emitting cell positioned at one edge of the substrate 10 and an N-type bonding pad 55 is formed on the exposed N-type semiconductor layer 20 of the light emitting cell positioned at the other edge of the substrate 10.

The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment but is not limited thereto. Various modifications can be made or various material films can be further added. For example, in order to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10.

Accordingly, a light emitting device in which the plurality of light emitting cells each of which side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at predetermined slope from a horizontal plane are connected with one another can be manufactured.

Figs. 10 to 13 are sectional views illustrating a process of manufacturing a light emitting device according to a third embodiment of the present invention.

The third embodiment is almost the same as the second embodiment. In the second embodiment, the N-type semiconductor layer 20 is first exposed and a portion of the exposed N-type semiconductor layer 20 is then removed to separate the light emitting cells from one another. In the third embodiment, however, a plurality of light emitting cells are first

separated, and a portion of an N-type semiconductor layer 20 is then exposed. Descriptions overlapping with the previous embodiments will be omitted herein.

Referring to Fig. 10, portions of an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40, which are sequentially formed on a substrate 10, are removed to form a plurality of light emitting cells. To this end, after a photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 40 and light-exposed, it is immediately developed without hard-baking such that an etching mask pattern can be formed. The portions of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor pattern 20, which are exposed through the etching mask pattern, and the etching mask pattern is removed to separate the light emitting cells from one another. Accordingly, a light emitting device in which entire side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at a predetermined slope can be obtained as shown in this figure. Further, the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are removed using the etching mask pattern in which a photoresist is applied at a thickness of 3 to 50μm on the P-type semiconductor layer 40 and light-exposed and hard-baked at a temperature of 100 to 140°C and then developed. Accordingly, the entire side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 can be formed at various slopes of 80 to 20°.

Thereafter, as shown in Fig. 11, portions of the P-type semiconductor layer 40 and the active layer 30 are removed to expose a portion of the N-type semiconductor layer 20 through a predetermined etching process.

Referring to Fig. 12, the N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent light emitting cell are connected

with each other through a bridge process.

Further, in order to apply an external voltage to the light emitting device, a P-type bonding pad 50 is formed on the P-type semiconductor layer 40 of the light emitting cell positioned at one edge of the substrate 10 and an N-type bonding pad 55 is formed on the exposed N-type semiconductor layer 20 of the light emitting cell positioned at the other edge of the substrate 10.

The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment but is not limited thereto. Various modifications can be made and various material films may be further added. For example, in order to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10.

Further, even in a case where the plurality of light emitting cells are separated by etching such that the side surfaces may have various slopes as shown in Fig. 10 and then etched to expose the N-type semiconductor layer 20, a light emitting device can be manufactured using the same etching process as described above. That is, as shown in Fig. 11, the side surfaces of the P-type semiconductor layer 40 and the active layer 30, which are etched to expose the N-type semiconductor layer 20, can be formed at various slopes.

Accordingly, a light emitting device in which the plurality of light emitting cells each of which side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at predetermined slope from a horizontal plane are connected with one another can be manufactured.

Figs. 14 to 17 are sectional views illustrating a process of manufacturing a light emitting device according to a fourth embodiment of the present invention.

The fourth embodiment is almost the same as the third embodiment. In the third embodiment, a conductive wire for electrically connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell is formed through a bridge process. In the fourth embodiment, however, the conductive wire is formed through a step coverage process. Descriptions overlapping with the previous embodiments will be omitted herein.

Referring to Fig. 14, even in a case where a plurality of light emitting cells are separated by etching such that the side surfaces may have various slopes and then etched to expose an N-type semiconductor layer 20 through the aforementioned process, the side surfaces of P-type semiconductor layer 40 and active layer 30, which are etched to expose the N-type semiconductor layer 20, are formed with various slopes. Further, in order to reduce the resistance of the P-type semiconductor layer 40 and enhance the transmittance of light, a transparent electrode layer 85 may be further formed on a top surface of the P-type semiconductor layer 40. Further, an additional ohmic metal layer 87 for facilitating the supply of current may be further formed on a top surface of the P-type semiconductor layer 40 or the exposed N-type semiconductor layer 20. The transparent electrode layer 85 may be made of ITO (Indium Tin Oxide), ZnO or a conductive transparent metal, and the ohmic metal layer 87 may be made of Cr or Au.

Referring to Fig. 15, a continuous insulation layer 70 is formed on an entire surface of the substrate 10 with the plurality of light emitting cells formed thereon. The insulation layer 70 covers the side surfaces and top surfaces of the light emitting cells and the top surfaces of the substrate 10 between the adjacent light emitting cells. For example, the insulation layer 70 may be formed as a silicone oxide film using a CVD (Chemical Vapor Deposition) technique.

Since the side surfaces of the light emitting cells are inclined, the insulation layer 70 can easily cover the side surfaces of the light emitting cells. Since the total thickness of the N-type semiconductor layer 20 and active layer 30 is small and spaces between the adjacent P-type semiconductor layers 40 are broad, the side surfaces of the P-type semiconductor layers 40 adjacent to the exposed regions of the N-type semiconductor layers 20 can be easily covered with the insulation layer 70.

Referring to Fig. 16, an opening portion is formed on each of the exposed N-type and P-type semiconductor layers 20 and 40 of the light emitting cell by patterning the insulation layer 70 through a predetermined etching process. If the transparent electrode layer 85 and/or the ohmic metal layer 87 are formed as shown in this figure, the transparent electrode layer 85 and/or the ohmic metal layer 87 are exposed through the opening portion.

Referring to Fig. 17, a wire 80 is formed on the insulation layer 70 with the opening portion. The wire 80 connects the N-type and P-type semiconductor layers 20 and 40 through the opening portion thereof. That is, the N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent the light emitting cell are electrically connected with the wire.

The wire 80 may be formed using a plating technique. That is, after an etching mask pattern with an opening portion defining a region of the wire 80 has been formed on the insulation layer 70 and a metal layer has been plated within the opening portion, the etching mask pattern is removed and thus the wire 80 can be formed.

Further, the wire 80 may be formed using the CVD (Chemical Vapor Deposition) or PVD (Physical Vapor Deposition) technique. That is, a metal layer is formed using a vapor deposition technique such as electron beam deposition and then patterned using a photo and etching process, so that the wire 80 can be formed. Since the side surface of the light emitting

cell is inclined, the metal layer is continuously formed on the upper side surface of the light emitting cell.

The light emitting device in which the wire 80 is formed as described above has an advantage in that it is possible to prevent the wire 80 from being disconnected or shorted due to external pressure and also prevent conductive materials such as metal, which remains while the wire 80 is formed, from shorting the light emitting cell.

Accordingly, a light emitting device in which the plurality of light emitting cells each of which side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at predetermined slope from a horizontal plane are connected with one another can be manufactured.

As described above, the light emitting device according to the present invention is formed such that the side surfaces of the P-type semiconductor layer, the active layer and a portion of the N-type semiconductor layer are not perpendicular (90°) to but inclined at a predetermined slope from a horizontal plane. Therefore, luminous efficiency of the light emitting device of the present invention can be enhanced as compared with that of the conventional light emitting device. The reason is that a photon reflected on a flat surface in the prior art is not reflected on a surface with a different angle but emitted to the outside.

Fig. 18 is a conceptual sectional view illustrating a light emitting device with a flip chip structure according to the present invention.

Referring to Fig. 18, the light emitting device comprises a light emitting layer, i.e. an N-type semiconductor layer 120, an active layer 130 and a P-type semiconductor layer 140 sequentially formed on a base substrate 110. Further, the light emitting device comprises a submount substrate 200 onto which the base substrate 110 with the light emitting layer formed thereon is flip-chip bonded through metal bumps 150 and 155. A side surface of the

light emitting layer comprising the P-type semiconductor layer 140, the active layer 130 and the N-type semiconductor layer 120 is inclined at a slope of 20 to 80°from the horizontal plane and a critical angle of light is changed due to the side surface such that the light can be easily extracted. Therefore, luminous efficiency of the light emitting device can be improved.

Figs. 19 to 23 are sectional views illustrating a process of manufacturing a light emitting device according to a fifth embodiment of the present invention.

Referring to Fig. 19, an N-type semiconductor layer 120, an active layer 130 and a P-type semiconductor layer 140 are sequentially formed on a base substrate 110.

The base substrate 110 refers to a general wafer used for fabricating a light emitting device is made of a transparent substrate such as Al_2O_3, ZnO and $LiAl_2O_3$. In this embodiment, a crystal growth substrate made of sapphire is used.

The N-type semiconductor layer 120, the active layer 130 and the P-type semiconductor layer 140 are sequentially formed on the substrate 110 through various deposition methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like. A buffer layer may be further formed on the substrate 110 to reduce lattice mismatch between the substrate 110 and the subsequent layers upon growth of crystals. The aforementioned components are the same as those in the previous embodiments, and thus, descriptions overlapping with the foregoing components will be omitted herein.

Thereafter, portions of the P-type semiconductor layer 140 and the active layer 130 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 120. This etching process is the same as that of the previous embodiments.

That is, after a photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 140 of Fig. 19 and light-exposed, it is immediately developed without hard-baking to form an etching mask pattern. The P-type semiconductor 140 and the active layer 130, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer 120. Thereafter, if the etching mask pattern is removed, side surfaces of the P-type semiconductor layer 140 and the active layer 130 which are not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane can be obtained as shown in Fig. 20.

Alternatively, after a photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 140 of Fig. 19 and light-exposed, it is hard-baked at a temperature of 100 to 140°C and then developed such that an etching mask pattern can be formed. After the P-type semiconductor layer 140 and the active layer 130, which are exposed through the etching mask pattern, have been etched, the etching mask pattern is removed such that the side surfaces of the etched P-type semiconductor layer 140 and active layer 130 can have a variety of slopes of 80 to 20°.

A reflection layer for reflecting light may be further formed on a top surface of the P-type semiconductor layer 140, and an additional ohmic metal layer for facilitating the supply of current may be further formed on a top surface of the P-type semiconductor layer 140 or the exposed N-type semiconductor layer 120. The ohmic metal layer may be made of Cr or Au.

Further, P-type and N-type metal bumps 155 and 150 are formed on the P-type and N-type semiconductor layers 140 and 120, respectively, as shown in Fig. 21. Each of the P-type and N-type metal bumps 155 and 150 may be made of at least one material selected

from the group consisting of Pb, Sn, Au, Ge, Cu, Bi, Cd, Zn, Ag, Ni, Ti and an alloy thereof. To this end, a photoresist is applied onto an entire structure and a photoresist pattern (not shown) through which portions of the P-type and N-type semiconductor layers 140 and 120 are exposed is formed through a photo-etching process using a predetermined mask. After a metal film has been deposited on the entire structure, metal film portions formed on regions other than regions on the P-type and N-type semiconductor layers 140 exposed through the photoresist pattern and the photoresist pattern are removed. Accordingly, the P-type and N-type metal bumps 155 and 150 are formed on the P-type and N-type semiconductor layers 140 and 120, respectively.

Next, referring to Fig. 22, an additional submount substrate 200 is prepared to form P-type and N-type bonding pads 215 and 210 connected to the P-type and N-type metal bumps 155 and 150, respectively.

At this time, various kinds of superior heat conductive substrates 200 are used as the submount substrate 200. That is, the submount substrate 200 may be made of SiC, Si, Ge, SiGe, AlN, metal or the like. In this embodiment, AlN with superior heat conductivity and insulation property is used. The present invention is not limited thereto, but a metallic material with superior heat and electric conductivity may be employed. In this case, an insulation or dielectric film is formed on the substrate 200 to sufficiently serve as an insulation. The dielectric film may be made of SiO2, MgO and SiN or an insulating material. Further, each of the P-type and N-type bonding pads 210 and 215 is made of a metal with superior electric conductivity. This is formed through a screen printing process or a deposition process using a predetermined mask pattern.

Thereafter, the submount substrate 200 is flip-chip bonded onto the base substrate 110 with the light emitting layer formed thereon.

Referring to Fig. 23, in the light emitting device of the present invention, the N-type and P-type metal bumps 150 and 155 formed on the top of the light emitting layer are bonded and connected with the N-type and P-type bonding pads 210 and 215 of the submount substrate 200, respectively. At this time, the bonding pads and metal bumps may be bonded using heat or ultrasonic waves or simultaneously using the heat and ultrasonic waves. The metal bumps 150 and 155 and the lower bonding pads 210 and 215 are connected through a variety of bonding methods.

Moreover, the N-type and P-type metal bumps 150 and 155 are not formed on the top of the light emitting layer but may be formed on the submount substrate 200.

As can be seen from this figure, a plurality of light emitting devices may be fabricated on a single substrate 10, which is cut into the individual light emitting devices. At this time, portions A shown in Fig. 23 are cutting portions used for individually cutting the plurality of light emitting devices.

The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto. Various processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes. For example, in the same process as the previous embodiments, the base substrate with the N-type semiconductor layer, the active layer and the P-type semiconductor layer sequentially formed thereon is prepared as shown in Fig. 19. Then, portions of the P-type semiconductor layer, the active layer and the N-type semiconductor layer are first removed to expose the substrate such that the plurality of light emitting devices can be individually isolated. At this time, the side surfaces of the P-type semiconductor layer, the active layer and the N-type semiconductor layer, which are etched through the aforementioned process, may be formed not to be perpendicular (90°) to

but inclined at a predetermined slope.

Accordingly, a light emitting device with a flip chip structure, in which the side surfaces of the P-type semiconductor layer, the active layer and a portion of the N-type semiconductor layer are not perpendicular (90°) to but inclined at the predetermined slope from the horizontal plane, can be manufactured.

Figs. 24 to 28 are sectional views illustrating a process of manufacturing a light emitting device according to a sixth embodiment of the present invention.

The sixth embodiment is almost the same as the fifth embodiment. In the sixth embodiment, however, there is provided a light emitting device with a flip chip structure, in which a plurality of light emitting cells are connected in series, parallel or series-parallel in a wafer level to reduce the size of the device, and they can be driven at proper voltage and current to be used for illumination purpose and can also be driven even with an AC power source. Descriptions overlapping with the previous embodiments will be omitted herein.

Referring to Fig. 24, an N-type semiconductor layer 120, an active layer 130 and a P-type semiconductor layer 140 are sequentially formed on a base substrate 110 through various deposition methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like. A buffer layer may be further formed on the substrate 110 to reduce lattice mismatch between the substrate 110 and the subsequent layers upon growth of crystals.

Thereafter, portions of the N-type semiconductor layer 120, the active layer 130 and the P-type semiconductor layer 140, which are sequentially formed on the base substrate 110, are removed to form a plurality of light emitting cells. To this end, after a photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 140 of Fig. 24

and light-exposed, it is immediately developed without hard-baking to form an etching mask pattern. The P-type semiconductor 140, the active layer 130 and the predetermined N-type semiconductor layer 120, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to separate the light emitting cells from one another. Next, if the etching mask pattern is removed, a light emitting device in which entire side surfaces of the etched P-type semiconductor layer 140, active layer 130 and N-type semiconductor layer 120 are not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane can be obtained as shown in Fig. 25.

Alternatively, after a photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 140 of Fig. 24 and light-exposed, it is hard-baked at a temperature of 100 to 140°C and developed such that an etching mask pattern can be formed. After the P-type semiconductor layer 140, the active layer 130 and the N-type semiconductor layer 120, which are exposed through the etching mask pattern, have been etched, the etching mask pattern is removed such that the side surfaces of the etched P-type semiconductor layer 140 and active layer 130 can be inclined at various slopes of 80 to 20°.

Next, portions of the P-type semiconductor layer 140 and the active layer 130 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 120, as shown in Fig. 26. The exposed N-type semiconductor layer 120 of one light emitting cell and the P-type semiconductor layer 140 of another adjacent light emitting cell are connected with each other through a predetermined conductive wire. At this time, a bridge wire 160 is made of a conductive material, e.g. metal. It will be apparent that the bridge wire 160 may be made of a silicone compound doped with impurities. The bridge wire 160 is formed through a bridge process.

Further, a plurality of metal bumps are formed on the top of the light emitting cells,

and P-type and N-type metal bumps 155 and 150 are further formed on the P-type semiconductor layer 140 of the light emitting cell positioned at one edge of the substrate 110 and the N-type semiconductor layer 120 of the light emitting cell positioned the other edge of the substrate, respectively.

Next, as shown in Fig. 27, an additional submount substrate 200 is prepared, on which a plurality of bonding layers 220, a P-type bonding pad 215 positioned at one edge of the submount substrate 200 and an N-type bonding pad 210 positioned at the other edge of the submount substrate are formed.

Thereafter, as can be shown in Fig. 28, the aforementioned base substrate 110 with the plurality of light emitting cells formed thereon is flip-chip bonded onto the submount substrate 200 to fabricate the light emitting device. The substrates are bonded with each other through the metal bumps 150 and 155 formed on the top of the light emitting cell and the bonding layers 220 formed on the submount substrate 200, respectively. The P-type bonding pad 215 positioned at one edge of the submount substrate 200 is connected to the P-type metal bump 155 of the light emitting cell positioned at one edge of the base substrate 110, whereas the N-type bonding pad 210 positioned at the other edge of the submount substrate 200 is connected to the N-type metal bump 150 of the light emitting cell positioned at the other edge of the base substrate 110.

The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto. Various processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes. For example, in this embodiment, the conductive wire for electrically connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell is

formed through a bridge process, and the base substrate is then flip-chip bonded onto the submount substrate. However, the present invention is not limited thereto. That is, a conductive wire for electrically connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cells may be formed through a step coverage process which is the same as in the fourth embodiment. Further, an electrode layer may be formed on the submount substrate when the plurality of light emitting cells are flip-chip bonded onto the submount substrate such that the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are electrically connected through the metal bumps.

Accordingly, a light emitting device in which a plurality of flip chip light emitting cells each having a side surface of a light emitting layer, which is not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane, are arrayed on the submount substrate can be manufactured. The light emitting cells may be connected in various ways, i.e. in series, parallel or series-parallel, depending on the desired purpose.

Fig. 29 is a sectional view showing a seventh embodiment according to the present invention.

The seventh embodiment is almost the same as the sixth embodiment. In this embodiment, even in a case where a plurality of light emitting cells are separated by etching such that the side surfaces may have slopes as shown in Fig. 25 and then etched to expose an N-type semiconductor layer, a light emitting device can be manufactured using the same etching process as the previous embodiment. That is, side surfaces of a P-type semiconductor layer 140 and an active layer 130 etched to expose an N-type semiconductor layer 120 are formed with various slopes, as shown in Fig. 29.

Accordingly, a light emitting device in which a plurality of flip chip light emitting

cells each having an entire side surface of a light emitting layer, which is not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane, are arrayed on the submount substrate can be manufactured. The light emitting cells may be connected in various ways, i.e. in series, parallel or series-parallel, depending on the desired purpose.

As described above, the light emitting device with a flip chip structure according to the present invention is formed such that some side surfaces of a light emitting layer are not particular (90°) to but inclined at a predetermined slope from the horizontal plane. Therefore, luminous efficiency of the light emitting device of the present invention can be enhanced as compared with that of the conventional light emitting device. The reason is that a photon reflected on a flat surface in the prior art is not reflected on a surface with a different angle but emitted to the outside.

Figs. 30 and 31 are conceptual sectional views illustrating a difference between effects of the light emitting devices according to the prior art and the present invention.

The light efficiency of a light emitting device may be expressed as internal quantum efficiency and external quantum efficiency, and the internal quantum efficiency is determined in accordance with the design and quality of an active layer. The external quantum efficiency is determined in accordance with a degree where a photon produced in an active layer is emitted to the outside of a light emitting device. Referring to Fig. 30 in which a conventional light emitting device is shown, a side surface of a semiconductor layer is formed perpendicular to a horizontal plane. In such a case, some portions of photons are not penetrated through the side surface of the semiconductor layer but reflected thereon, and totally reflected light is not emitted to the outside but dissipated within the light emitting device. However, referring to Fig. 31 in which a light emitting device according to the present invention is shown, a side surface of a semiconductor layer is not perpendicular to but

inclined at a predetermined slope from a horizontal plane. In such a case, the inclined side surface makes a critical angle of light change to help the light to be more easily extracted. Therefore, light generated in an active layer is not totally reflected but emitted to the outside of the light emitting device such that external quantum efficiency can be markedly enhanced.

Although the present invention has been described in detail in connection with the specific embodiments, it will be readily understood by those skilled in the art that various modifications and changes can be made thereto within the technical spirit and scope of the present invention. It is also apparent that the modifications and changes fall within the scope of the present invention defined by the appended claims.

What is claimed is:

1. A light emitting device, comprising:

a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on a portion of the N-type semiconductor layer on a substrate,

wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including the N-type or P-type semiconductor layer of the light emitting cell has a slope of 20 to 80° from a horizontal plane.

2. The light emitting device as claimed in claim 1, further comprising a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

3. The light emitting device as claimed in claim 1 or 2, further comprising a transparent electrode layer on the P-type semiconductor layer.

4. The light emitting device as claimed in claim 1 or 2, further comprising P-type and N-type ohmic metal layers containing Cr or Au on the P-type and N-type semiconductor layers, respectively.

5. A light emitting device, comprising:

a substrate formed with a plurality of light emitting cells each including an N-type

semiconductor layer and a P-type semiconductor layer formed on the N-type semiconductor layer; and

a submount substrate flip-chip bonded onto the substrate,

wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including at least the P-type semiconductor layer of the light emitting cell has a slope of 20 to 80° from a horizontal plane.

6. The light emitting device as claimed in claim 5, further comprising a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

7. A method of manufacturing a light emitting device, comprising the steps of:

sequentially forming N-type and P-type semiconductor layers on a substrate;

forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; and removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern.

8. The method as claimed in claim 7, further comprising the steps of:

removing a portion of the N-type semiconductor layer exposed through the removal of the P-type semiconductor layer to form a plurality of light emitting cells; and

connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire.

9. The method as claimed in claim 7, further comprising the step of flip-chip bonding the substrate onto an additional submount substrate after the step of removing the P-type semiconductor layer and the etching mask pattern.

10. The method as claimed in claim 9, further comprising the steps of:
removing a portion of the N-type semiconductor layer exposed due to the removal of the P-type semiconductor layer to form a plurality of light emitting cell; and
connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire, after the step of removing the P-type semiconductor layer and the etching mask pattern.

11. The method as claimed in claim 8 or 10, wherein the step of forming the plurality of light emitting cells comprises the steps of:
forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer;
removing the N-type and P-type semiconductor layers exposed through the etching mask pattern to form a plurality of light emitting cells; and
removing the etching mask pattern.

12. The method as claimed in claim 8 or 10, wherein the N type semiconductor layer of one light emitting cell and the P type semiconductor layer of another adjacent light emitting cell are connected with the conductive wire through a bridge or step

coverage process.

13. The method as claimed in any one of claims 7 to 10, wherein a photoresist with a thickness of 3 to 50μm is used in the step of forming the etching mask pattern.

14. The method as claimed in claim 13, wherein the step of forming the etching mask pattern comprises the steps of:
applying the photoresist onto the P-type semiconductor layer;
light exposing the photoresist in accordance with a predetermined mask pattern; and
developing the light-exposed photoresist without a baking process after the light exposure.

15. The method as claimed in claim 13, wherein the step of forming the etching mask pattern comprises the steps of:
applying the photoresist onto the P-type semiconductor layer;
light exposing the photoresist in accordance with a predetermined mask pattern;
hard baking the light-exposed photoresist at a temperature of 100 to 140°C; and
developing the hard-baked photoresist.

16. The method as claimed in claim 7 or 8, further comprising the steps of:
after the step of removing the P-type semiconductor layer and the etching mask pattern,
removing a rear surface of the substrate at a certain thickness; and
depositing Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof onto the rear surface of the

substrate.

ABSTRACT OF THE DISCLOSURE

The present invention relates to a light emitting device and a method of manufacturing the light emitting device. According to the present invention, the light emitting device comprises a substrate, an N-type semiconductor layer formed on the substrate, and a P-type semiconductor layer formed on the N-type semiconductor layer, wherein a side surface including the N-type or P-type semiconductor layer has a slope of 20 to 80° from a horizontal plane. Further, the present invention provides a light emitting device comprising a substrate formed with a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on the N-type semiconductor layer, and a submount substrate flip-chip bonded onto the substrate, wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including at least the P-type semiconductor layer of the light emitting cell has a slope of 20 to 80°from a horizontal plane. Further, the present invention provides a method of manufacturing the light emitting device. Accordingly, there is an advantage in that the characteristics of a light emitting device such as luminous efficiency, external quantum efficiency and extraction efficiency are enhanced and the reliability is secured such that light with high luminous intensity and brightness can be emitted.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3576-053
	Application Number	
Title of Invention	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3576-053
	Application Number	
Title of Invention	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3576-053
	Application Number	
Title of Invention	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME	

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Application Information:

Title of the Invention	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME		
Attorney Docket Number	3576-053	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3576-053
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PCT/KR2006/002427	KR	2006-06-22	(•) Yes ( ) No

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1020050053797	KR	2005-06-22	(•) Yes ( ) No

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	Application Number	
Title of Invention	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME	

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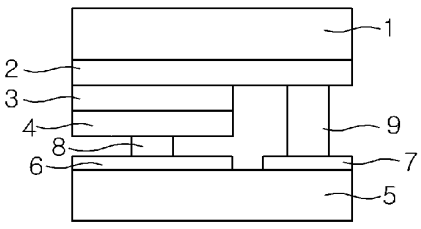
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(54) Title: LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME



(57) Abstract: The present invention relates to a light emitting device and a method of manufacturing the light emitting device. According to the present invention, the light emitting device comprises a substrate, an N-type semiconductor layer formed on the substrate, and a P-type semiconductor layer formed on the N-type semiconductor layer, wherein a side surface including the N-type or P-type semiconductor layer has a slope of 20 to 80°from a horizontal plane. Further, the present invention provides a light emitting device comprising a substrate formed with a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on the N-type semiconductor layer, and a submount substrate flip-chip bonded onto the substrate, wherein the N-type semiconductor layer of one light emitting cell and the P-type semi¬ conductor layer of another adjacent light emitting cell are connected to each other, and a side surface including at least the P-type semiconductor layer of the light emitting cell has a slope of 20 to 80°from a horizontal plane. Further, the present invention provides a method of manu¬ facturing the light emitting device. Accordingly, there is an advantage in that the characteristics of a light emitting device such as luminous efficiency, external quantum efficiency and extraction efficiency are enhanced and the reliability is secured such that light with high luminous intensity and brightness can be emitted.

WO 2006/137711 A1

Description

LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME

Technical Field

[1] The present invention relates to a light emitting device and a method of manufacturing the same. More particularly, the present invention relates to a nitride based semiconductor light emitting device with enhanced luminous efficiency and brightness and a method of manufacturing the light emitting device.

Background Art

[2] A light emitting device refers to an element in which minority carriers (electrons or holes) injected using a p-n junction structure of a semiconductor are produced and certain light is emitted due to recombination of the carriers. A light emitting source is formed from any one or combination of compound semiconductor materials such as GaAs, AlGaAs, GaN, InGaN and AlGaInP, so that a variety of colors can be implemented. For example, a red light emitting device may be formed from GaAsP or the like; a green light emitting device may be formed from GaP, InGaN or the like; a blue light emitting device may be formed using an InGaN/GaN double hetero structure; and a UV light emitting device may be formed using an AlGaN/GaN or AlGaN/AlGaN structure.

[3] In particular, GaN has a direct bandgap of 3.4eV at a normal temperature and a direct energy bandgap of 1.9eV (InN) to 3.4eV (GaN) or 6.2eV (AlN) by combining with a substance such as InN or AlN. Thus, GaN is a substance with great applicability to an optical element due to its broad wavelength range from visible light to ultraviolet light. Since the wavelength can be adjusted in such a manner, full-color implementation can be made by means of red, green and blue light emitting devices with a short wavelength range, so that the applicability to a general illumination market as well as a display device market is expected to be greatly increased.

[4] Light emitting devices have characteristics of lower power consumption, longer lifespan, better installation in a narrow space and stronger resistance against vibration as compared with existing bulbs or fluorescent lamps. Since the light emitting devices are used as display devices and backlights and have superior characteristics in view of the reduction in power consumption and the durability, many studies for applying the light emitting devices to a general illumination field have been recently conducted. In the future, their applicability is expected to extend to a backlight of a large-sized LCD-TV, a vehicle headlight and general illumination. To this end, it is necessary to improve luminous efficiency of light emitting devices, solve a heat dissipation

problem, and achieve high brightness and output of the light emitting devices.

[5] Many techniques for enhancing the performance of light emitting devices have been currently developed. There are various indexes indicating the performance of light emitting devices, such as luminous efficiency (lm/W), internal quantum efficiency (%), external quantum efficiency (%) and extraction efficiency (%). The extraction efficiency is determined as a ratio of electrons injected into the light emitting device to photons emitted to the outside of the light emitting device. That is, the light emitting device becomes bright as the extraction efficiency becomes high. Since the extraction efficiency of the light emitting device is much influenced by the shape and surface pattern of a chip, the structure of a chip and a packaging type, careful attention should be paid when designing the light emitting device.

[6] Fig. 1 is a sectional view showing a conventional light emitting device with a horizontal structure.

[7] Referring to Fig. 1, the light emitting device comprises a substrate 1, an N-type semiconductor layer 2 formed on the substrate 1, an active layer 3 formed on a portion of the N-type semiconductor layer 2 and a P-type semiconductor layer 4. That is, after the N-type semiconductor layer 2, the active layer 3 and the P-type semiconductor layer 4 have been sequentially formed on the substrate 1, predetermined regions of the P-type semiconductor layer 4 and the active layer 3 are etched to expose a portion of the N-type semiconductor layer 2. Then, a predetermined voltage is applied to top surfaces of the exposed N-type semiconductor layer 2 and the P-type semiconductor layer 4.

[8] Fig. 2 is a sectional view showing a conventional light emitting device with a flip chip structure.

[9] Referring to Fig. 2, the light emitting device comprises an N-type semiconductor layer 2, an active layer 3 and a P-type semiconductor layer 4, which are sequentially formed on a base substrate 1. The light emitting device further comprises a submount substrate 5 onto which the base substrate 1 is flip-chip bonded using metal bumps 8 and 9. To this end, the N-type semiconductor layer 2, the active layer 3 and the P-type semiconductor layer 4 are sequentially formed on the predetermined substrate 1, and portions of the P-type semiconductor layer 4 and the active layer 3 are etched to expose the N-type semiconductor layer 2 such that a light emitting cell can be formed. Further, the additional submount substrate 5 is prepared to form first and second electrodes 6 and 7 thereon, and the P-type and N-type metal bumps 8 and 9 are then formed on the first and second electrodes 6 and 7, respectively. Thereafter, the light emitting cell is bonded with the submount substrate 5 such that P and N electrodes of the light emitting cell are bonded with the P-type and N-type metal bumps 8 and 9, respectively, to fabricate a light emitting device. Since such a conventional light emitting

device with a flip chip structure has high heat dissipation efficiency and hardly has shield of light, there is an advantage in that its light efficiency is increased by 50% or more as compared with a conventional light emitting device. Further, since a gold wire for driving a light emitting device is not necessary, many applications to a variety of small-sized packages can be considered.

[10] Light produced from a light emitting layer of a light emitting device is emitted from all the surfaces of a chip, and light extraction efficiency is generally determined by a critical angle of light. However, when the conventional light emitting device is etched to expose an N-type semiconductor layer, side surfaces of the P-type semiconductor layer and the active layer are vertically processed such that a portion of light produced within the light emitting device is totally reflected on the etched surface that is processed vertically from a horizontal plane. Then, a considerable amount of light to be totally reflected is not emitted to the outside but dissipated within the light emitting device due to the internal reflection. That is, there is a problem in that luminous efficiency in which electric energy is converted into light energy and the light is then emitted to the outside of a light emitting device is low.

Disclosure of Invention

Technical Problem

[11] The present invention is conceived to solve the aforementioned problems. Accordingly, an object of the present invention is to provide a light emitting device for emitting light with high luminous intensity and brightness by enhancing characteristics of luminous efficiency, external quantum efficiency, extraction efficiency and the like and improving reliability, and a method of manufacturing the light emitting device.

Technical Solution

[12] According to an aspect of the present invention for achieving the objects, there is provided a light emitting device, comprising a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on a portion of the N-type semiconductor layer on a substrate. The N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell may be connected to each other, and a side surface including the N-type or P-type semiconductor layer of the light emitting cell has a slope of 20 to 80°from a horizontal plane. The light emitting device may further comprise a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell, a transparent electrode layer on the P-type semiconductor layer, and P-type and N-type ohmic metal layers containing Cr or Au on the P-type and N-type semiconductor layers, respectively.

[13] According to another aspect of the present invention, there is provided a light

emitting device comprising a substrate formed with a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on the N-type semiconductor layer and a submount substrate flip-chip bonded onto the substrate. Preferably, the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including at least the P-type semiconductor layer of the light emitting cell has a slope of 20 to 80°from a horizontal plane. The light emitting device may further comprise a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

[14] According to further aspect of the present invention, there is provided a method of manufacturing a light emitting device, comprising the steps of sequentially forming N-type and P-type semiconductor layers on a substrate; forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; and removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern.

[15] According to still further aspect of the present invention, there is a method of manufacturing a light emitting device comprising the steps of removing a portion of the N-type semiconductor layer exposed due to the removal of the P-type semiconductor layer to form a plurality of light emitting cells; and connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire.

[16] According to still further aspect of the present invention, there is a method of manufacturing a light emitting device comprising the step of flip-chip bonding the substrate onto an additional submount substrate after the step of removing the P-type semiconductor layer and the etching mask pattern. The method of manufacturing a light emitting device may further comprise the steps of removing a portion of the N-type semiconductor layer exposed through the removal of the P-type semiconductor layer to form a plurality of light emitting cell; and connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire, after the step of removing the P-type semiconductor layer and the etching mask pattern.

[17] The step of forming the plurality of light emitting cells may comprise the steps of forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; removing the N-type and P-type semiconductor layers exposed through the etching mask pattern to form a plurality of light emitting cells; and removing the etching mask pattern.

[18] The N type semiconductor layer of one light emitting cell and the P type semiconductor layer of another adjacent light emitting cell may be connected with the conductive wire through a bridge or step coverage process.

[19] A photoresist with a thickness of 3 to 50□ may be used in the step of forming the etching mask pattern. The step of forming the etching mask pattern may comprise the steps of: applying the photoresist onto the P-type semiconductor layer; light exposing the photoresist in accordance with a predetermined mask pattern; and developing the light-exposed photoresist without a baking process after the light exposure. The step of forming the etching mask pattern may comprise the steps of: applying the photoresist onto the P-type semiconductor layer; light exposing the photoresist in accordance with a predetermined mask pattern; hard baking the light-exposed photoresist at a temperature of 100 to 140°C; and developing the hard-baked photoresist.

[20] After the step of removing the P-type semiconductor layer and the etching mask pattern, the method of manufacturing a light emitting device may further comprise the steps of removing a rear surface of the substrate at a certain thickness; and depositing Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof onto the rear surface of the substrate.

[21]

[22]

Advantageous Effects

[23] In a light emitting device and a method of manufacturing the same according to the present invention, light produced from a side surface of a semiconductor layer, which is not perpendicular to but inclined at a predetermined slop from a horizontal plane, is not totally reflected but emitted to the outside of the light emitting device. Therefore, more enhanced characteristics of light extraction efficiency, external quantum efficiency, luminous efficiency or the like can be obtained. Further, a light emitting device of the present invention emits light with high luminous intensity and brightness and can be applied to a variety of products in which a superior light characteristic is necessary.

Brief Description of the Drawings

[24] The above and other objects, features and advantages of the present invention will become apparent from the following description of preferred embodiments given in conjunction with the accompanying drawings, in which:

[25] Figs. 1 and 2 are sectional views showing conventional light emitting devices, respectively;

[26] Fig. 3 is a conceptual sectional view illustrating a light emitting device with a hori zontal structure according to the present invention;

[27] Figs. 4 and 5 are sectional views illustrating a process of manufacturing a light

emitting device according to a first embodiment of the present invention;

[28] Figs. 6 to 9 are sectional views illustrating a process of manufacturing a light emitting device according to a second embodiment of the present invention;

[29] Figs. 10 to 13 are sectional views illustrating a process of manufacturing a light emitting device according to a third embodiment of the present invention;

[30] Figs. 14 to 17 are sectional views illustrating a process of manufacturing a light emitting device according to a fourth embodiment of the present invention;

[31] Fig. 18 is a conceptual sectional view illustrating a light emitting device with a flip chip structure according to the present invention;

[32] Figs. 19 to 23 are sectional views illustrating a process of manufacturing a light emitting device according to a fifth embodiment of the present invention;

[33] Figs. 24 to 28 are sectional views illustrating a process of manufacturing a light emitting device according to a sixth embodiment of the present invention;

[34] Fig. 29 is a sectional view showing a seventh embodiment according to the present invention; and

[35] Figs. 30 and 31 are conceptual sectional views illustrating a difference between effects of the light emitting devices according to the prior art and the present invention.

Best Mode for Carrying Out the Invention

[36] Hereinafter, a light emitting device and a manufacturing method thereof according to the present invention will be described in detail with reference to the accompanying drawings. However, the present invention is not limited to the embodiments set forth herein but can be implemented in different forms. Rather, the preferred embodiments are merely provided to allow the present invention to be completely described herein and to fully convey the scope of the invention to those skilled in the art.

[37] Fig. 3 is a conceptual sectional view illustrating a light emitting device with a horizontal structure according to the present invention.

[38] Referring to Fig. 3, the light emitting device comprises a substrate 10, and an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40, which are sequentially formed on the substrate 10. Each of side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 has a slope of 80 to 20° from a horizontal plane such that a critical angle of light can be changed by such surfaces and light can be easily extracted. Therefore, luminous efficiency of a light emitting device can be improved.

[39] Figs. 4 and 5 are sectional views illustrating a process of manufacturing a light emitting device according to a first embodiment of the present invention.

[40] Referring to Fig. 4, an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40 are sequentially formed on a substrate 10.

[41] The substrate 10 refers to a general wafer used for fabricating a light emitting device and is made of at least any one of Al_2O_3, SiC, ZnO, Si, GaAs, GaP, $LiAl_2O_3$, BN, AlN and GaN. In this embodiment, a crystal growth substrate made of sapphire is used.

[42] A buffer layer (not shown) may be further formed on the substrate 10 to reduce lattice mismatch between the substrate 10 and the subsequent layers upon growth of crystals. The buffer layer may contain GaN or AlN that is a semiconductor material.

[43] The N-type semiconductor layer 20 is a layer in which electrons are produced and is preferably made from GaN doped with N-type impurities. However, the N-type semiconductor layer 20 is not limited thereto but may use a material layer having a variety of semiconductor properties. The N-type semiconductor layer 20 including N-type $Al_xGa_{1-x}N(0\leq x\leq 1)$ is formed in this embodiment. Further, the P-type semiconductor layer 40 is a layer in which holes are produced and is preferably made from GaN doped with P-type impurities. However, the P-type semiconductor layer 40 is not limited thereto but may use a material layer with a variety of semiconductor properties. The P-type semiconductor layer 40 including P-type $Al_xGa_{1-x}N(0\leq x\leq 1)$ is formed in this embodiment. Moreover, InGaN may be used as the semiconductor layer. Further, each of the N-type and P-type semiconductor layers 20 and 40 may be formed as a multiple layer.

[44] The active layer 30 has a predetermined bandgap and is a region where a quantum well is formed so that electrons and holes are recombined. The active layer 30 may contain InGaN. The wavelength of light emitted through the combination of electrons and holes varies according to the kind of a material constituting the active layer 30. Therefore, it is preferred that a semiconductor material contained in the active layer 30 be controlled depending on a target wavelength.

[45] The aforementioned material layers are formed through a variety of deposition and growth methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like.

[46] Thereafter, portions of the P-type semiconductor layer 40 and the active layer 30 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 20. An etching mask pattern is formed on the P-type semiconductor layer 40, and the P-type semiconductor layer 40 and the active layer 30 are then removed through a dry or wet etching process to expose the N-type semiconductor layer 20.

[47] Generally, in order to perform the etching process, a photoresist has been applied onto a top surface of the P-type semiconductor layer 40 at a thickness of 1 to 2□, and

then soft-baked at a temperature of 80 to 90℃ is performed. Next, an exposure process in which light in a UV range is irradiated through a predetermined photo mask to transfer a pattern formed on the mask to the applied photoresist is executed. Thereafter, the photoresist is hard-baked at a temperature of 100 to 120℃, and a developing process in which the photoresist at a portion with relatively weak combination through the exposure process is melted using a solvent is executed. A predetermined etching mask pattern is formed on the P-type semiconductor layer 40 through the above process.

[48] However, in this embodiment, the photoresist is applied at a thickness of 3 to 50□ which is thicker as compared with the prior art when the etching mask pattern is formed, and the exposure process is performed after the soft-baking. Next, if the photoresist is directly developed without the hard-baking, a developed side surface of the remaining photoresist is formed into an inclined surface not perpendicular (90°) to but inclined at a predetermined slope from a horizontal plane. Subsequently, if exposed regions of the P-type semiconductor layer 40, the active layer 30 and the pre-determined N-type semiconductor layer 20 are etched using the etching mask pattern with such a slope of the side surface, the side surfaces of the etched P-type semi-conductor layer 40, active layer 30 and N-type semiconductor layer 20 can be similarly formed into an inclined surface not perpendicular (90°) to but inclined at a pre-determined slope from the horizontal plane.

[49] That is, after the photoresist has been applied at a thickness of 3 to 50□ on the P-type semiconductor layer 40 of Fig. 4 and light-exposed, a developed etching mask pattern is immediately formed without the hard-baking. The P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer 20. A portion of the exposed N-type semiconductor layer 20 may be further removed. Thereafter, if the etching mask pattern is removed, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 are not per-pendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured as shown in Fig. 5.

[50] Alternatively, after a photoresist has been applied at a thickness of 3 to 50□ on the P-type semiconductor layer 40 of Fig. 4 and light-exposed, hard-baking may be performed. In such a case, if the photoresist is hard-baked at a temperature of 100 to 140℃ and then developed, the side surface of the developed photoresist may be etched to have a slope of 80 to 20° from a horizontal plane. For example, in a case where the hard-baking is performed at a temperature of 100℃, an etching mask pattern with a slope of about 80° from the horizontal plane can be obtained, and the side surfaces of

the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 can have a slope of about 80° from the horizontal plane using the etching mask pattern. Further, in a case where the hard-baking is performed at a temperature of 140℃, an etching mask pattern with a slope of about 20° from the horizontal plane can be obtained, and the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 can have a slope of about 20° from the horizontal plane using the etching mask pattern.

[51] The etching mask pattern, which the photoresist with a thickness of 3 to 50□ has been light-exposed and hard-baked at a temperature of 100 to 140℃ and then developed in such a manner, can be used such that the side surfaces of the etched the P-type semiconductor layer 40, active layer 30 and predetermined N-type semiconductor layer 20 have a slope of 80 to 20° from a horizontal plane similarly to the etching mask pattern. Then, light produced within a light emitting layer is not totally reflected on the etched side surface with a variety of slopes but emitted to the outside of a light emitting device.

[52] A transparent electrode layer may be further formed on the P-type semiconductor layer 40 to reduce resistance of the P-type semiconductor layer 40 and enhancing transmittance of light, and an additional ohmic metal layer may be further formed on the P-type semiconductor layer 40 or the exposed N-type semiconductor layer 20 to facilitate current supply. The transparent electrode layer may be made of ITO (Indium Tin Oxide), ZnO or a transparent conductive metal, and the ohmic metal layer may be made of Cr or Au. Further, for the application of voltage, a P-type electrode may be further formed on the P-type semiconductor layer 40 and an N-type electrode may be further formed on the N-type semiconductor layer 20.

[53] Further, in order to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10.

[54] As can be seen from this figure, a plurality of light emitting devices may be fabricated on a single substrate 10, which is cut into the individual light emitting devices. At this time, portions A shown in Fig. 5 are cutting portions used for individually cutting the plurality of light emitting devices.

[55] Accordingly, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 is not perpendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured.

[56] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto.

Various processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes.

[57] Figs. 6 to 7 are sectional views illustrating a process of manufacturing a light emitting device according to a second embodiment of the present invention.

[58] The second embodiment of the present invention is almost the same as the first embodiment. In the second embodiment, however, there is provided a light emitting device in which a plurality of light emitting cells are connected in series, parallel or series-parallel in a wafer level to reduce the size of the device, and they can be driven at proper voltage and current to be used for illustration purpose and can also be driven even with an AC power source. Descriptions overlapping with the previous embodiment will be omitted herein.

[59] Referring to Fig. 6, an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40 are sequentially formed on a substrate 10 through various deposition methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like. A buffer layer may be further formed on the substrate 10 to reduce lattice mismatch between the substrate 10 and the subsequent layers upon growth of crystals.

[60] Thereafter, portions of the P-type semiconductor layer 40 and the active layer 30 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 20. That is, after the photoresist has been applied at a thickness of 3 to 50□ on the P-type semiconductor layer 40 of Fig. 6 and light-exposed, it is developed without hard-baking to form an etching mask pattern. The P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer 20. A portion of the exposed N-type semiconductor layer 20 may be further removed. Thereafter, if the etching mask pattern is removed, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured as shown in Fig. 7.

[61] Alternatively, after a photoresist has been applied in a thickness of 3 to 50□ on the P-type semiconductor layer 40 of Fig. 6 and light-exposed, it is hard-baked at a temperature of 100 to 140°C and developed such that an etching mask pattern can be formed. After the P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, have been etched, the etching mask pattern is removed such that the side surfaces of the etched P-type semiconductor layer 40 and active layer 30 can have a variety of slopes of 80 to 20°.

[62] Next, in order to form a plurality of light emitting cells on the substrate 10, predetermined regions of the exposed N-type semiconductor layer 20 are removed such that a portion of the substrate 10 can be exposed. To this end, a predetermined mask pattern is formed on all the portions except the predetermined regions where the substrate 10 will be exposed, and regions of the N-type semiconductor layer 20 that are exposed through the mask pattern are then etched such that the plurality of light emitting cells can be electrically isolated from one another as shown in Fig. 8. At this time, the mask pattern whose side surface is inclined through the aforementioned process is formed and then used to etch the exposed N-type semiconductor layer 20 such that the side surface of the N-type semiconductor layer 20 in which the plurality of light emitting cells are separated from one another is not perpendicular to but inclined at a predetermined slope from a horizontal plane.

[63] Referring to Fig. 9, the N-type semiconductor layer 20 of a light emitting cell and the P-type semiconductor layer 40 of the adjacent light emitting cell are connected through a predetermined wiring process. That is, the exposed N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent light emitting cell are connected through a wire 60. At this time, the conductive wire 60 for electrically connecting the N-type and P-type semiconductor layers 20 and 40 are formed through a bridge process.

[64] The aforementioned bridge process is also called an air-bridge process. In the air-bridge process, a photosensitive liquid is applied between chips to be connected with each other through a photo process and developed to form a photoresist pattern, a material such as metal is first formed into a thin film on the photoresist pattern through a vacuum vapor deposition method or the like, and a conductive material containing gold (Au) is applied at a predetermined thickness onto the thin film through an electroplating, electroless plating or metal vapor deposition method. Thereafter, if the photoresist pattern is removed with a solution of a solvent or the like, a lower portion of the conductive material is completely removed, and thus, only the bridge-shaped conductive material is formed in a space between the adjacent light emitting cells.

[65] The wire 60 may be made of not only metal but also all kinds of conductive materials. It will be apparent that a silicone compound doped with impurities may be used.

[66] Further, in order to apply an external voltage to the light emitting device, a P-type bonding pad 50 is formed on the P-type semiconductor layer 40 of the light emitting cell positioned at one edge of the substrate 10 and an N-type bonding pad 55 is formed on the exposed N-type semiconductor layer 20 of the light emitting cell positioned at the other edge of the substrate 10.

[67] The aforementioned process of manufacturing a light emitting device according to

the present invention is merely a specific embodiment but is not limited thereto. Various modifications can be made or various material films can be further added. For example, in order to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10.

[68] Accordingly, a light emitting device in which the plurality of light emitting cells each of which side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at predetermined slope from a horizontal plane are connected with one another can be manufactured.

[69] Figs. 10 to 13 are sectional views illustrating a process of manufacturing a light emitting device according to a third embodiment of the present invention.

[70] The third embodiment is almost the same as the second embodiment. In the second embodiment, the N-type semiconductor layer 20 is first exposed and a portion of the exposed N-type semiconductor layer 20 is then removed to separate the light emitting cells from one another. In the third embodiment, however, a plurality of light emitting cells are first separated, and a portion of an N-type semiconductor layer 20 is then exposed. Descriptions overlapping with the previous embodiments will be omitted herein.

[71] Referring to Fig. 10, portions of an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40, which are sequentially formed on a substrate 10, are removed to form a plurality of light emitting cells. To this end, after a photoresist has been applied at a thickness of 3 to 50□ on the P-type semiconductor layer 40 and light-exposed, it is immediately developed without hard-baking such that an etching mask pattern can be formed. The portions of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor pattern 20, which are exposed through the etching mask pattern, and the etching mask pattern is removed to separate the light emitting cells from one another. Accordingly, a light emitting device in which entire side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at a pre-determined slope can be obtained as shown in this figure. Further, the P-type semi-conductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are removed using the etching mask pattern in which a photoresist is applied at a thickness of 3 to 50□ on the P-type semiconductor layer 40 and light-exposed and hard-baked at a temperature of 100 to 140℃ and then developed. Accordingly, the entire side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 can be formed at various slopes of 80 to 20°.

[72] Thereafter, as shown in Fig. 11, portions of the P-type semiconductor layer 40 and the active layer 30 are removed to expose a portion of the N-type semiconductor layer 20 through a predetermined etching process.

[73] Referring to Fig. 12, the N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent light emitting cell are connected with each other through a bridge process.

[74] Further, in order to apply an external voltage to the light emitting device, a P-type bonding pad 50 is formed on the P-type semiconductor layer 40 of the light emitting cell positioned at one edge of the substrate 10 and an N-type bonding pad 55 is formed on the exposed N-type semiconductor layer 20 of the light emitting cell positioned at the other edge of the substrate 10.

[75] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment but is not limited thereto. Various modifications can be made and various material films may be further added. For example, in order to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10.

[76] Further, even in a case where the plurality of light emitting cells are separated by etching such that the side surfaces may have various slopes as shown in Fig. 10 and then etched to expose the N-type semiconductor layer 20, a light emitting device can be manufactured using the same etching process as described above. That is, as shown in Fig. 11, the side surfaces of the P-type semiconductor layer 40 and the active layer 30, which are etched to expose the N-type semiconductor layer 20, can be formed at various slopes.

[77] Accordingly, a light emitting device in which the plurality of light emitting cells each of which side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at predetermined slope from a horizontal plane are connected with one another can be manufactured.

[78] Figs. 14 to 17 are sectional views illustrating a process of manufacturing a light emitting device according to a fourth embodiment of the present invention.

[79] The fourth embodiment is almost the same as the third embodiment. In the third embodiment, a conductive wire for electrically connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell is formed through a bridge process. In the fourth embodiment, however, the conductive wire is formed through a step coverage process. Descriptions overlapping with the previous embodiments will be omitted herein.

[80] Referring to Fig. 14, even in a case where a plurality of light emitting cells are separated by etching such that the side surfaces may have various slopes and then etched to expose an N-type semiconductor layer 20 through the aforementioned process, the side surfaces of P-type semiconductor layer 40 and active layer 30, which are etched to expose the N-type semiconductor layer 20, are formed with various slopes. Further, in order to reduce the resistance of the P-type semiconductor layer 40 and enhance the transmittance of light, a transparent electrode layer 85 may be further formed on a top surface of the P-type semiconductor layer 40. Further, an additional ohmic metal layer 87 for facilitating the supply of current may be further formed on a top surface of the P-type semiconductor layer 40 or the exposed N-type semiconductor layer 20. The transparent electrode layer 85 may be made of ITO (Indium Tin Oxide), ZnO or a conductive transparent metal, and the ohmic metal layer 87 may be made of Cr or Au.

[81] Referring to Fig. 15, a continuous insulation layer 70 is formed on an entire surface of the substrate 10 with the plurality of light emitting cells formed thereon. The insulation layer 70 covers the side surfaces and top surfaces of the light emitting cells and the top surfaces of the substrate 10 between the adjacent light emitting cells. For example, the insulation layer 70 may be formed as a silicone oxide film using a CVD (Chemical Vapor Deposition) technique.

[82] Since the side surfaces of the light emitting cells are inclined, the insulation layer 70 can easily cover the side surfaces of the light emitting cells. Since the total thickness of the N-type semiconductor layer 20 and active layer 30 is small and spaces between the adjacent P-type semiconductor layers 40 are broad, the side surfaces of the P-type semiconductor layers 40 adjacent to the exposed regions of the N-type semiconductor layers 20 can be easily covered with the insulation layer 70.

[83] Referring to Fig. 16, an opening portion is formed on each of the exposed N-type and P-type semiconductor layers 20 and 40 of the light emitting cell by patterning the insulation layer 70 through a predetermined etching process. If the transparent electrode layer 85 and/or the ohmic metal layer 87 are formed as shown in this figure, the transparent electrode layer 85 and/or the ohmic metal layer 87 are exposed through the opening portion.

[84] Referring to Fig. 17, a wire 80 is formed on the insulation layer 70 with the opening portion. The wire 80 connects the N-type and P-type semiconductor layers 20 and 40 through the opening portion thereof. That is, the N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent the light emitting cell are electrically connected with the wire.

[85] The wire 80 may be formed using a plating technique. That is, after an etching mask pattern with an opening portion defining a region of the wire 80 has been formed on

the insulation layer 70 and a metal layer has been plated within the opening portion, the etching mask pattern is removed and thus the wire 80 can be formed.

[86] Further, the wire 80 may be formed using the CVD (Chemical Vapor Deposition) or PVD (Physical Vapor Deposition) technique. That is, a metal layer is formed using a vapor deposition technique such as electron beam deposition and then patterned using a photo and etching process, so that the wire 80 can be formed. Since the side surface of the light emitting cell is inclined, the metal layer is continuously formed on the upper side surface of the light emitting cell.

[87] The light emitting device in which the wire 80 is formed as described above has an advantage in that it is possible to prevent the wire 80 from being disconnected or shorted due to external pressure and also prevent conductive materials such as metal, which remains while the wire 80 is formed, from shorting the light emitting cell.

[88] Accordingly, a light emitting device in which the plurality of light emitting cells each of which side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at predetermined slope from a horizontal plane are connected with one another can be manufactured.

[89] As described above, the light emitting device according to the present invention is formed such that the side surfaces of the P-type semiconductor layer, the active layer and a portion of the N-type semiconductor layer are not perpendicular (90°) to but inclined at a predetermined slope from a horizontal plane. Therefore, luminous efficiency of the light emitting device of the present invention can be enhanced as compared with that of the conventional light emitting device. The reason is that a photon reflected on a flat surface in the prior art is not reflected on a surface with a different angle but emitted to the outside.

[90] Fig. 18 is a conceptual sectional view illustrating a light emitting device with a flip chip structure according to the present invention.

[91] Referring to Fig. 18, the light emitting device comprises a light emitting layer, i.e. an N-type semiconductor layer 120, an active layer 130 and a P-type semiconductor layer 140 sequentially formed on a base substrate 110. Further, the light emitting device comprises a submount substrate 200 onto which the base substrate 110 with the light emitting layer formed thereon is flip-chip bonded through metal bumps 150 and 155. A side surface of the light emitting layer comprising the P-type semiconductor layer 140, the active layer 130 and the N-type semiconductor layer 120 is inclined at a slope of 20 to 80° from the horizontal plane and a critical angle of light is changed due to the side surface such that the light can be easily extracted. Therefore, luminous efficiency of the light emitting device can be improved.

[92] Figs. 19 to 23 are sectional views illustrating a process of manufacturing a light

emitting device according to a fifth embodiment of the present invention.

[93] Referring to Fig. 19, an N-type semiconductor layer 120, an active layer 130 and a P-type semiconductor layer 140 are sequentially formed on a base substrate 110.

[94] The base substrate 110 refers to a general wafer used for fabricating a light emitting device is made of a transparent substrate such as Al_2O_3, ZnO and $LiAl_2O_3$. In this embodiment, a crystal growth substrate made of sapphire is used.

[95] The N-type semiconductor layer 120, the active layer 130 and the P-type semiconductor layer 140 are sequentially formed on the substrate 110 through various deposition methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like. A buffer layer may be further formed on the substrate 110 to reduce lattice mismatch between the substrate 110 and the subsequent layers upon growth of crystals. The aforementioned components are the same as those in the previous embodiments, and thus, descriptions overlapping with the foregoing components will be omitted herein.

[96] Thereafter, portions of the P-type semiconductor layer 140 and the active layer 130 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 120. This etching process is the same as that of the previous embodiments.

[97] That is, after a photoresist has been applied at a thickness of 3 to 50□ on the P-type semiconductor layer 140 of Fig. 19 and light-exposed, it is immediately developed without hard-baking to form an etching mask pattern. The P-type semiconductor 140 and the active layer 130, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer 120. Thereafter, if the etching mask pattern is removed, side surfaces of the P-type semiconductor layer 140 and the active layer 130 which are not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane can be obtained as shown in Fig. 20.

[98] Alternatively, after a photoresist has been applied at a thickness of 3 to 50□ on the P-type semiconductor layer 140 of Fig. 19 and light-exposed, it is hard-baked at a temperature of 100 to 140℃ and then developed such that an etching mask pattern can be formed. After the P-type semiconductor layer 140 and the active layer 130, which are exposed through the etching mask pattern, have been etched, the etching mask pattern is removed such that the side surfaces of the etched P-type semiconductor layer 140 and active layer 130 can have a variety of slopes of 80 to 20°.

[99] A reflection layer for reflecting light may be further formed on a top surface of the P-type semiconductor layer 140, and an additional ohmic metal layer for facilitating

the supply of current may be further formed on a top surface of the P-type semiconductor layer 140 or the exposed N-type semiconductor layer 120. The ohmic metal layer may be made of Cr or Au.

[100] Further, P-type and N-type metal bumps 155 and 150 are formed on the P-type and N-type semiconductor layers 140 and 120, respectively, as shown in Fig. 21. Each of the P-type and N-type metal bumps 155 and 150 may be made of at least one material selected from the group consisting of Pb, Sn, Au, Ge, Cu, Bi, Cd, Zn, Ag, Ni, Ti and an alloy thereof. To this end, a photoresist is applied onto an entire structure and a photoresist pattern (not shown) through which portions of the P-type and N-type semiconductor layers 140 and 120 are exposed is formed through a photo-etching process using a predetermined mask. After a metal film has been deposited on the entire structure, metal film portions formed on regions other than regions on the P-type and N-type semiconductor layers 140 exposed through the photoresist pattern and the photoresist pattern are removed. Accordingly, the P-type and N-type metal bumps 155 and 150 are formed on the P-type and N-type semiconductor layers 140 and 120, respectively.

[101] Next, referring to Fig. 22, an additional submount substrate 200 is prepared to form P-type and N-type bonding pads 215 and 210 connected to the P-type and N-type metal bumps 155 and 150, respectively.

[102] At this time, various kinds of superior heat conductive substrates 200 are used as the submount substrate 200. That is, the submount substrate 200 may be made of SiC, Si, Ge, SiGe, AlN, metal or the like. In this embodiment, AlN with superior heat conductivity and insulation property is used. The present invention is not limited thereto, but a metallic material with superior heat and electric conductivity may be employed. In this case, an insulation or dielectric film is formed on the substrate 200 to sufficiently serve as an insulation. The dielectric film may be made of SiO2, MgO and SiN or an insulating material. Further, each of the P-type and N-type bonding pads 210 and 215 is made of a metal with superior electric conductivity. This is formed through a screen printing process or a deposition process using a predetermined mask pattern.

[103] Thereafter, the submount substrate 200 is flip-chip bonded onto the base substrate 110 with the light emitting layer formed thereon.

[104] Referring to Fig. 23, in the light emitting device of the present invention, the N-type and P-type metal bumps 150 and 155 formed on the top of the light emitting layer are bonded and connected with the N-type and P-type bonding pads 210 and 215 of the submount substrate 200, respectively. At this time, the bonding pads and metal bumps may be bonded using heat or ultrasonic waves or simultaneously using the heat and ultrasonic waves. The metal bumps 150 and 155 and the lower bonding pads 210 and 215 are connected through a variety of bonding methods.

[105] Moreover, the N-type and P-type metal bumps 150 and 155 are not formed on the top of the light emitting layer but may be formed on the submount substrate 200.

[106] As can be seen from this figure, a plurality of light emitting devices may be fabricated on a single substrate 10, which is cut into the individual light emitting devices. At this time, portions A shown in Fig. 23 are cutting portions used for individually cutting the plurality of light emitting devices.

[107] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto. Various processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes. For example, in the same process as the previous embodiments, the base substrate with the N-type semiconductor layer, the active layer and the P-type semiconductor layer sequentially formed thereon is prepared as shown in Fig. 19. Then, portions of the P-type semiconductor layer, the active layer and the N-type semiconductor layer are first removed to expose the substrate such that the plurality of light emitting devices can be individually isolated. At this time, the side surfaces of the P-type semiconductor layer, the active layer and the N-type semiconductor layer, which are etched through the aforementioned process, may be formed not to be perpendicular (90°) to but inclined at a predetermined slope.

[108] Accordingly, a light emitting device with a flip chip structure, in which the side surfaces of the P-type semiconductor layer, the active layer and a portion of the N-type semiconductor layer are not perpendicular (90°) to but inclined at the predetermined slope from the horizontal plane, can be manufactured.

[109] Figs. 24 to 28 are sectional views illustrating a process of manufacturing a light emitting device according to a sixth embodiment of the present invention.

[110] The sixth embodiment is almost the same as the fifth embodiment. In the sixth embodiment, however, there is provided a light emitting device with a flip chip structure, in which a plurality of light emitting cells are connected in series, parallel or series-parallel in a wafer level to reduce the size of the device, and they can be driven at proper voltage and current to be used for illumination purpose and can also be driven even with an AC power source. Descriptions overlapping with the previous embodiments will be omitted herein.

[111] Referring to Fig. 24, an N-type semiconductor layer 120, an active layer 130 and a P-type semiconductor layer 140 are sequentially formed on a base substrate 110 through various deposition methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like. A buffer layer may be further formed on the substrate 110

to reduce lattice mismatch between the substrate 110 and the subsequent layers upon growth of crystals.

[112] Thereafter, portions of the N-type semiconductor layer 120, the active layer 130 and the P-type semiconductor layer 140, which are sequentially formed on the base substrate 110, are removed to form a plurality of light emitting cells. To this end, after a photoresist has been applied at a thickness of 3 to 50□ on the P-type semiconductor layer 140 of Fig. 24 and light-exposed, it is immediately developed without hard-baking to form an etching mask pattern. The P-type semiconductor 140, the active layer 130 and the predetermined N-type semiconductor layer 120, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to separate the light emitting cells from one another. Next, if the etching mask pattern is removed, a light emitting device in which entire side surfaces of the etched P-type semiconductor layer 140, active layer 130 and N-type semiconductor layer 120 are not perpendicular (90°) to but inclined at a pre-determined slope from the horizontal plane can be obtained as shown in Fig. 25.

[113] Alternatively, after a photoresist has been applied at a thickness of 3 to 50□ on the P-type semiconductor layer 140 of Fig. 24 and light-exposed, it is hard-baked at a temperature of 100 to 140℃ and developed such that an etching mask pattern can be formed. After the P-type semiconductor layer 140, the active layer 130 and the N-type semiconductor layer 120, which are exposed through the etching mask pattern, have been etched, the etching mask pattern is removed such that the side surfaces of the etched P-type semiconductor layer 140 and active layer 130 can be inclined at various slopes of 80 to 20°.

[114] Next, portions of the P-type semiconductor layer 140 and the active layer 130 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 120, as shown in Fig. 26. The exposed N-type semiconductor layer 120 of one light emitting cell and the P-type semiconductor layer 140 of another adjacent light emitting cell are connected with each other through a predetermined conductive wire. At this time, a bridge wire 160 is made of a conductive material, e.g. metal. It will be apparent that the bridge wire 160 may be made of a silicone compound doped with impurities. The bridge wire 160 is formed through a bridge process.

[115] Further, a plurality of metal bumps are formed on the top of the light emitting cells, and P-type and N-type metal bumps 155 and 150 are further formed on the P-type semiconductor layer 140 of the light emitting cell positioned at one edge of the substrate 110 and the N-type semiconductor layer 120 of the light emitting cell positioned the other edge of the substrate, respectively.

[116] Next, as shown in Fig. 27, an additional submount substrate 200 is prepared, on

which a plurality of bonding layers 220, a P-type bonding pad 215 positioned at one edge of the submount substrate 200 and an N-type bonding pad 210 positioned at the other edge of the submount substrate are formed.

[117] Thereafter, as can be shown in Fig. 28, the aforementioned base substrate 110 with the plurality of light emitting cells formed thereon is flip-chip bonded onto the submount substrate 200 to fabricate the light emitting device. The substrates are bonded with each other through the metal bumps 150 and 155 formed on the top of the light emitting cell and the bonding layers 220 formed on the submount substrate 200, respectively. The P-type bonding pad 215 positioned at one edge of the submount substrate 200 is connected to the P-type metal bump 155 of the light emitting cell positioned at one edge of the base substrate 110, whereas the N-type bonding pad 210 positioned at the other edge of the submount substrate 200 is connected to the N-type metal bump 150 of the light emitting cell positioned at the other edge of the base substrate 110.

[118] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto. Various processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes. For example, in this embodiment, the conductive wire for electrically connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell is formed through a bridge process, and the base substrate is then flip-chip bonded onto the submount substrate. However, the present invention is not limited thereto. That is, a conductive wire for electrically connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cells may be formed through a step coverage process which is the same as in the fourth embodiment. Further, an electrode layer may be formed on the submount substrate when the plurality of light emitting cells are flip-chip bonded onto the submount substrate such that the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are electrically connected through the metal bumps.

[119] Accordingly, a light emitting device in which a plurality of flip chip light emitting cells each having a side surface of a light emitting layer, which is not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane, are arrayed on the submount substrate can be manufactured. The light emitting cells may be connected in various ways, i.e. in series, parallel or series-parallel, depending on the desired purpose.

[120] Fig. 29 is a sectional view showing a seventh embodiment according to the present invention.

[121] The seventh embodiment is almost the same as the sixth embodiment. In this embodiment, even in a case where a plurality of light emitting cells are separated by etching such that the side surfaces may have slopes as shown in Fig. 25 and then etched to expose an N-type semiconductor layer, a light emitting device can be manufactured using the same etching process as the previous embodiment. That is, side surfaces of a P-type semiconductor layer 140 and an active layer 130 etched to expose an N-type semiconductor layer 120 are formed with various slopes, as shown in Fig. 29.

[122] Accordingly, a light emitting device in which a plurality of flip chip light emitting cells each having an entire side surface of a light emitting layer, which is not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane, are arrayed on the submount substrate can be manufactured. The light emitting cells may be connected in various ways, i.e. in series, parallel or series-parallel, depending on the desired purpose.

[123] As described above, the light emitting device with a flip chip structure according to the present invention is formed such that some side surfaces of a light emitting layer are not particular (90°) to but inclined at a predetermined slope from the horizontal plane. Therefore, luminous efficiency of the light emitting device of the present invention can be enhanced as compared with that of the conventional light emitting device. The reason is that a photon reflected on a flat surface in the prior art is not reflected on a surface with a different angle but emitted to the outside.

[124] Figs. 30 and 31 are conceptual sectional views illustrating a difference between effects of the light emitting devices according to the prior art and the present invention.

[125] The light efficiency of a light emitting device may be expressed as internal quantum efficiency and external quantum efficiency, and the internal quantum efficiency is determined in accordance with the design and quality of an active layer. The external quantum efficiency is determined in accordance with a degree where a photon produced in an active layer is emitted to the outside of a light emitting device. Referring to Fig. 30 in which a conventional light emitting device is shown, a side surface of a semiconductor layer is formed perpendicular to a horizontal plane. In such a case, some portions of photons are not penetrated through the side surface of the semiconductor layer but reflected thereon, and totally reflected light is not emitted to the outside but dissipated within the light emitting device. However, referring to Fig. 31 in which a light emitting device according to the present invention is shown, a side surface of a semiconductor layer is not perpendicular to but inclined at a predetermined slope from a horizontal plane. In such a case, the inclined side surface makes a critical angle of light change to help the light to be more easily extracted. Therefore, light generated in an active layer is not totally reflected but emitted to the outside of the

light emitting device such that external quantum efficiency can be markedly enhanced.

[126] Although the present invention has been described in detail in connection with the specific embodiments, it will be readily understood by those skilled in the art that various modifications and changes can be made thereto within the technical spirit and scope of the present invention. It is also apparent that the modifications and changes fall within the scope of the present invention defined by the appended claims.

[127]

[128]

Claims

[1] 1. A light emitting device, comprising:
a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on a portion of the N-type semiconductor layer on a substrate,
wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including the N-type or P-type semiconductor layer of the light emitting cell has a slope of 20 to 80°from a horizontal plane.

[2] 2. The light emitting device as claimed in claim 1, further comprising a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

[3] 3. The light emitting device as claimed in claim 1 or 2, further comprising a transparent electrode layer on the P-type semiconductor layer.

[4] 4. The light emitting device as claimed in claim 1 or 2, further comprising P-type and N-type ohmic metal layers containing Cr or Au on the P-type and N-type semiconductor layers, respectively.

[5] 5. A light emitting device, comprising:
a substrate formed with a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on the N-type semiconductor layer; and
a submount substrate flip-chip bonded onto the substrate,
wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including at least the P-type semiconductor layer of the light emitting cell has a slope of 20 to 80°from a horizontal plane.

[6] 6. The light emitting device as claimed in claim 5, further comprising a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

[7] 7. A method of manufacturing a light emitting device, comprising the steps of:
sequentially forming N-type and P-type semiconductor layers on a substrate;
forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; and
removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern.

[8] 8. The method as claimed in claim 7, further comprising the steps of:

removing a portion of the N-type semiconductor layer exposed through the removal of the P-type semiconductor layer to form a plurality of light emitting cells; and

connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire.

[9] 9. The method as claimed in claim 7, further comprising the step of flip-chip bonding the substrate onto an additional submount substrate after the step of removing the P-type semiconductor layer and the etching mask pattern.

[10] 10. The method as claimed in claim 9, further comprising the steps of:

removing a portion of the N-type semiconductor layer exposed due to the remova l of the P-type semiconductor layer to form a plurality of light emitting cell; and

connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire, after the step of removing the P-type semiconductor layer and the etching mask pattern.

[11] 11. The method as claimed in claim 8 or 10, wherein the step of forming the plurality of light emitting cells comprises the steps of:

forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer;

removing the N-type and P-type semiconductor layers exposed through the etching mask pattern to form a plurality of light emitting cells; and

removing the etching mask pattern.

[12] 12. The method as claimed in claim 8 or 10, wherein the N type semiconductor layer of one light emitting cell and the P type semiconductor layer of another adjacent light emitting cell are connected with the conductive wire through a bridge or step coverage process.

[13] 13. The method as claimed in any one of claims 7 to 10, wherein a photoresist with a thickness of 3 to 50□ is used in the step of forming the etching mask pattern.

[14] 14. The method as claimed in claim 13, wherein the step of forming the etching mask pattern comprises the steps of:

applying the photoresist onto the P-type semiconductor layer;

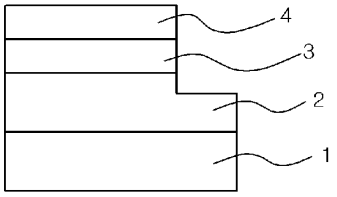
light exposing the photoresist in accordance with a predetermined mask pattern; and

developing the light-exposed photoresist without a baking process after the light exposure.

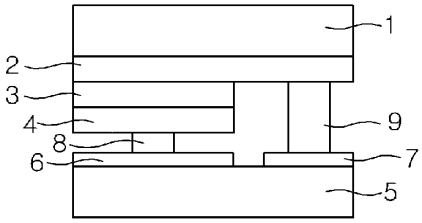
[15] 15. The method as claimed in claim 13, wherein the step of forming the etching mask pattern comprises the steps of:
applying the photoresist onto the P-type semiconductor layer;
light exposing the photoresist in accordance with a predetermined mask pattern;
hard baking the light-exposed photoresist at a temperature of 100 to 140°C; and
developing the hard-baked photoresist.

[16] 16. The method as claimed in claim 7 or 8, further comprising the steps of:
after the step of removing the P-type semiconductor layer and the etching mask pattern,
removing a rear surface of the substrate at a certain thickness; and
depositing Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof onto the rear surface of the substrate.

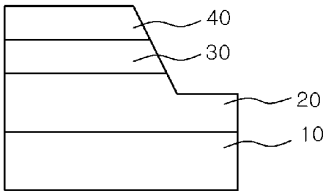
[Fig. 1]



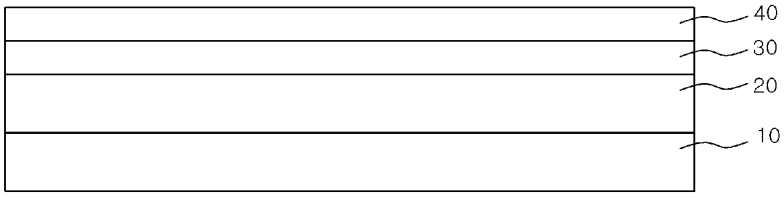
[Fig. 2]



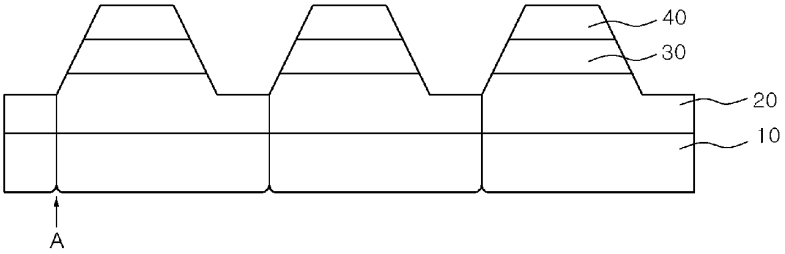
[Fig. 3]



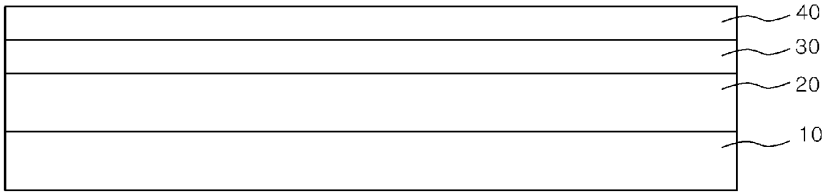
[Fig. 4]



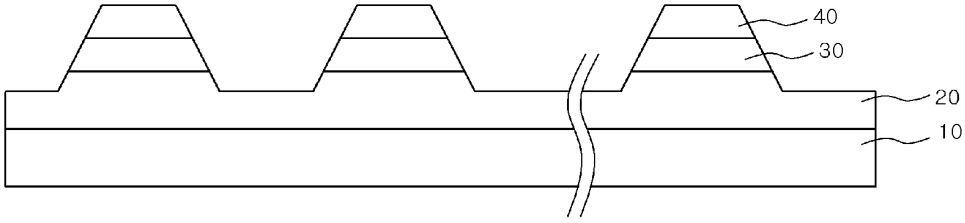
[Fig. 5]



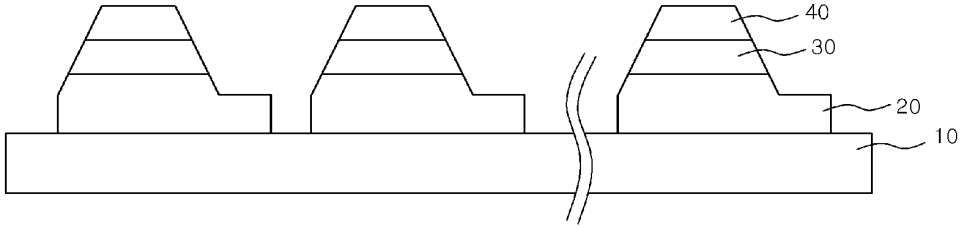
[Fig. 6]



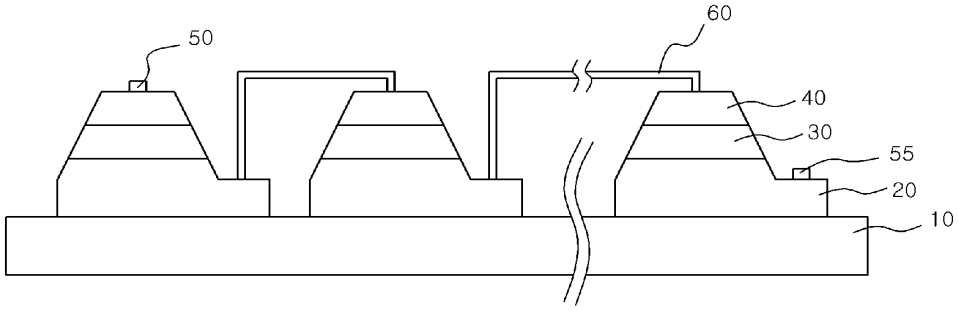
[Fig. 7]



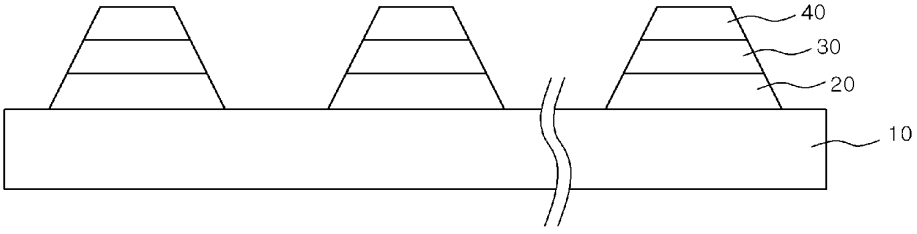
[Fig. 8]



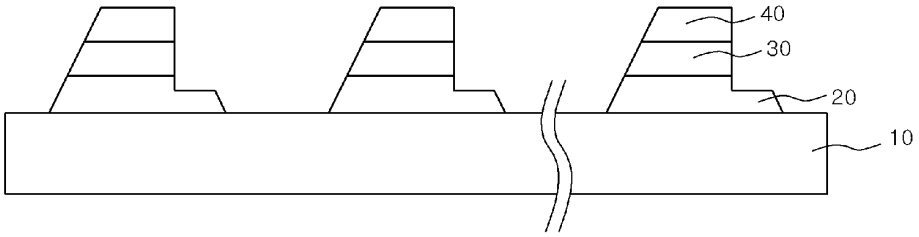
[Fig. 9]



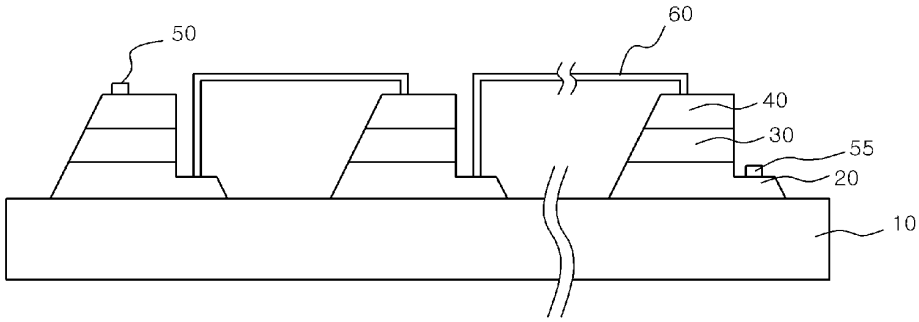
[Fig. 10]



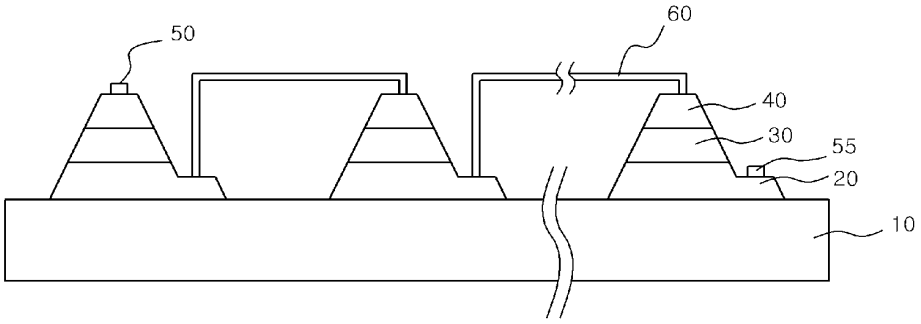
[Fig. 11]



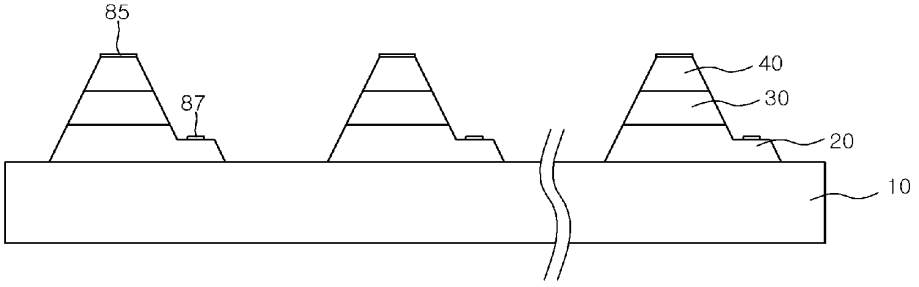
[Fig. 12]



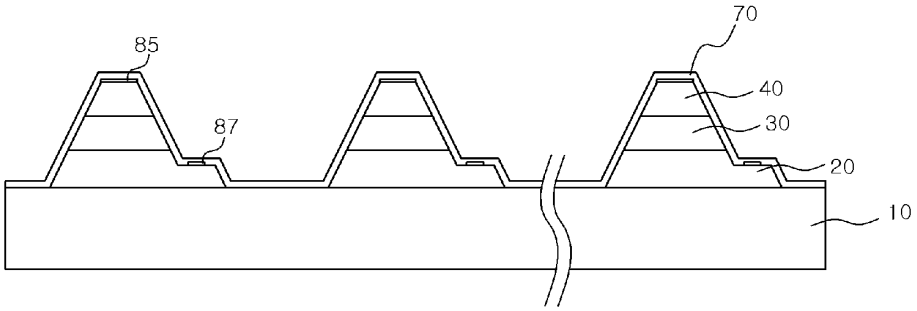
[Fig. 13]



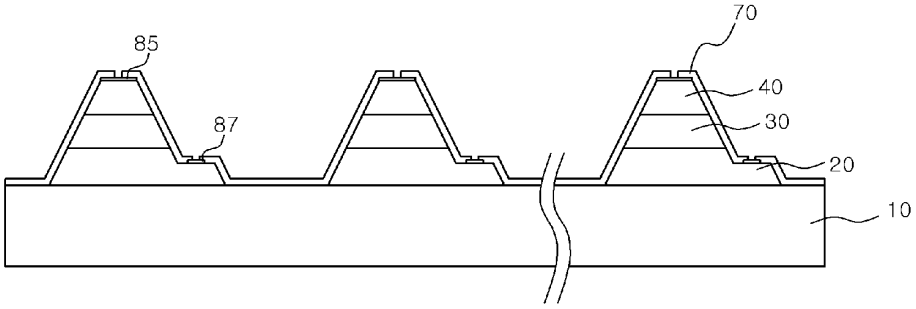
[Fig. 14]



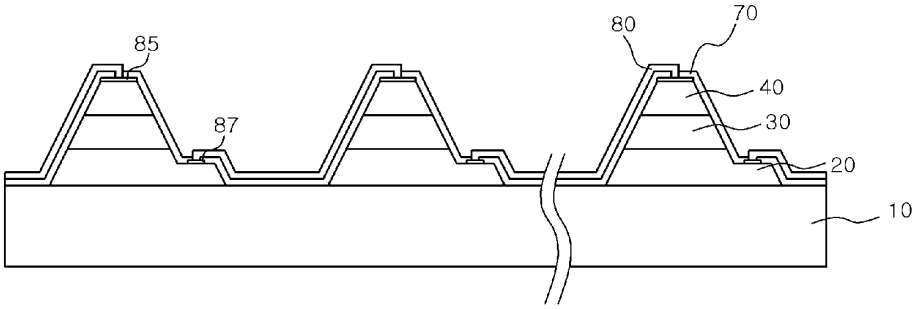
[Fig. 15]



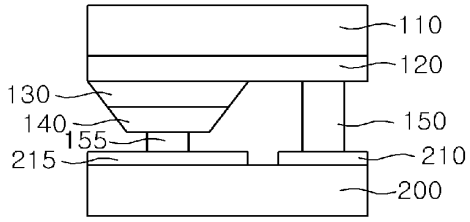
[Fig. 16]



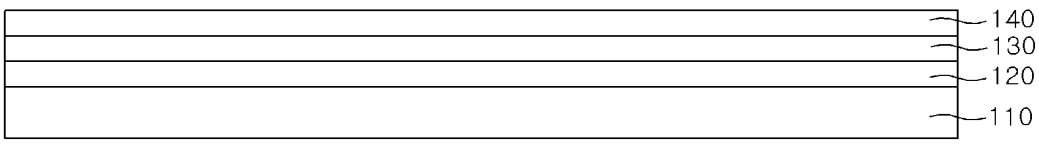
[Fig. 17]



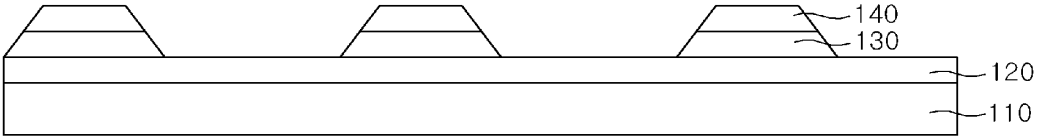
[Fig. 18]



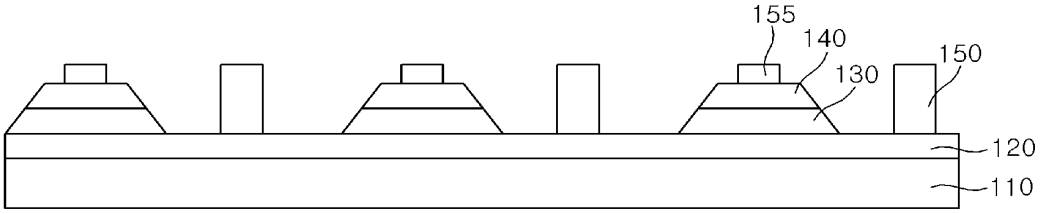
[Fig. 19]



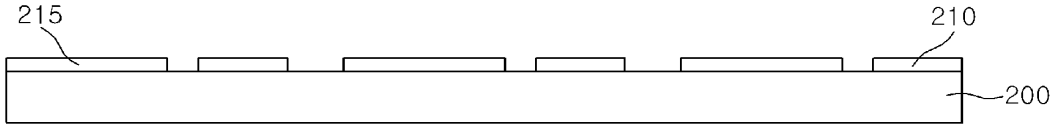
[Fig. 20]



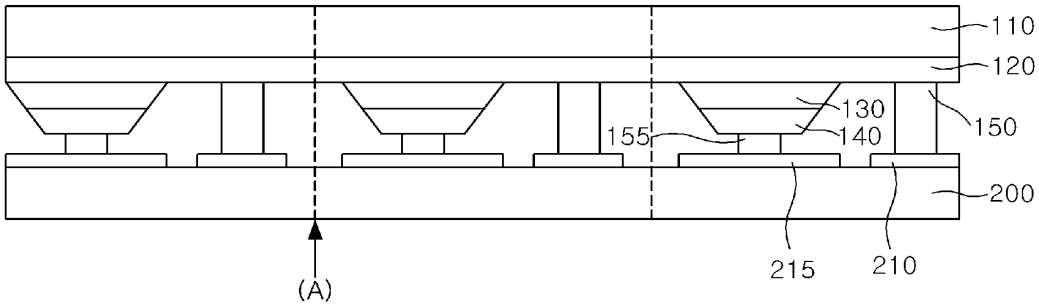
[Fig. 21]



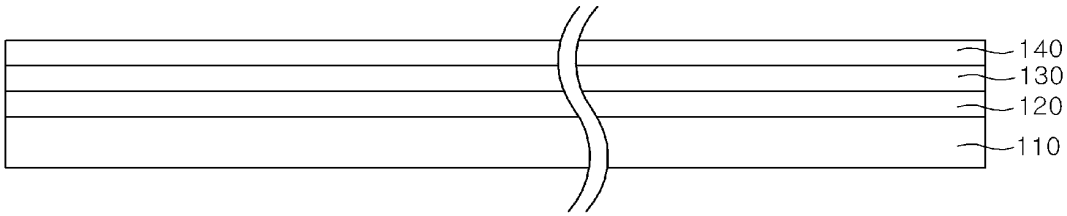
[Fig. 22]



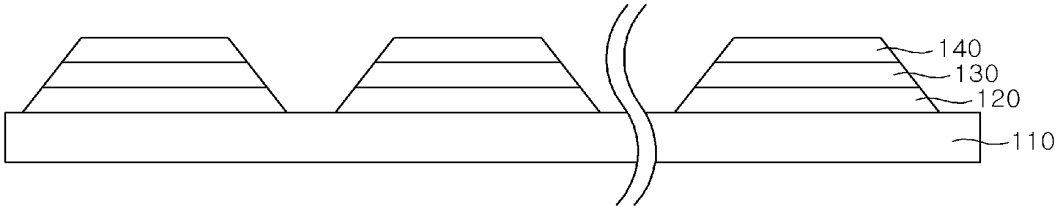
[Fig. 23]



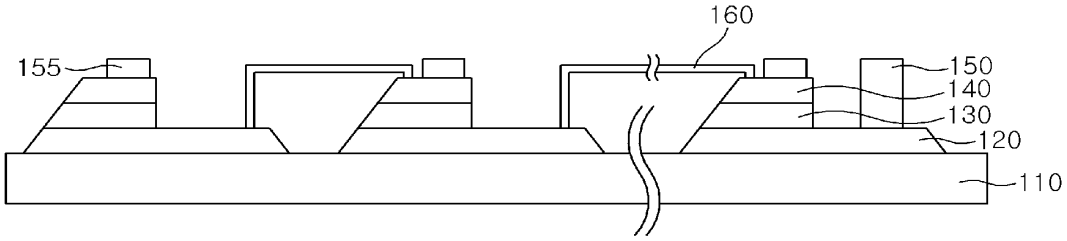
[Fig. 24]



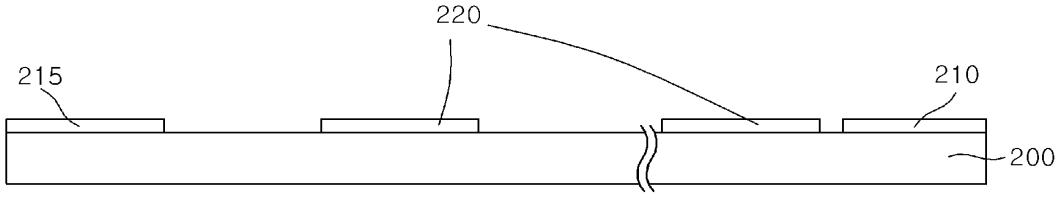
[Fig. 25]



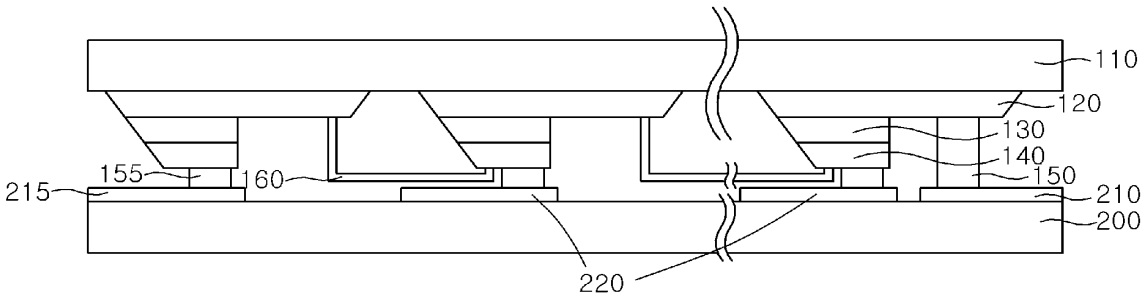
[Fig. 26]



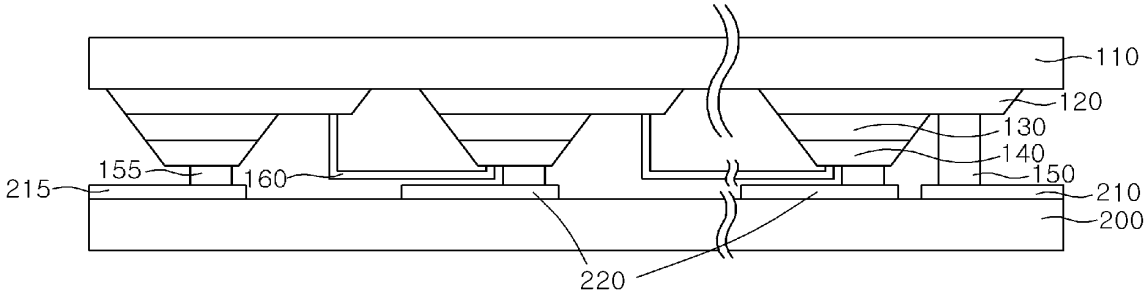
[Fig. 27]



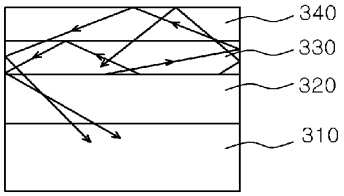
[Fig. 28]



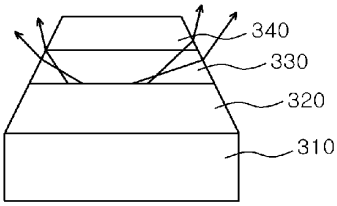
[Fig. 29]



[Fig. 30]



[Fig. 31]



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Application Number 10-2005-0053797

출 원 일 자 : 2005년 06월 22일
Date of Application JUN 22, 2005

출 원 인 : 서울옵토디바이스주식회사
Applicant(s) SEOUL OPTO DEVICE CO., LTD.

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【제출일자】 2005.06.22

【발명의 국문명칭】 발광 소자 및 이의 제조 방법

【발명의 영문명칭】 Light-emitting device and Method of manufacturing the same

【출원인】

【명칭】 서울옵토디바이스 주식회사

【출원인코드】 1-2003-032642-0

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【포괄위임등록번호】 2004-031626-3

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【취지】 특허법 제42조의 규정에 의한 출원, 특허법 제60조의 규정에 의한 출원심사를 청구합니다.

대리인 남승희 (인)

【수수료】

【기본출원료】	0	면	38,000 원
【가산출원료】	28	면	0 원
【우선권주장료】	0	건	0 원
【심사청구료】	12	항	493,000 원
【합계】	531,000 원		
【감면사유】	중소기업		
【감면후 수수료】	265,500 원		

【첨부서류】 1.중소기업기본법시행령 제2조에의한 중소기업에 해당함을 증명하는 서류[사업자등록증 및 원천징수이행상황신고서]_1통

【요약서】

【요약】

본 발명은 기판, 상기 기판 상에 형성된 N형 반도체층 및 상기 N형 반도체층 상에 형성된 P형 반도체층을 포함하고, 상기 N형 반도체층 또는 P형 반도체층을 포함하는 측면이 수평면으로부터 20 내지 80° 의 기울기를 갖는 것을 특징으로 하는 발광 소자 및 이의 제조 방법을 제공한다. 본 발명에 의한 발광 소자 및 이의 제조 방법은 발광 효율, 외부 양자 효율, 추출 효율 등의 특성을 향상시키고 신뢰성을 확보하여, 고광도, 고휘도의 광을 발광할 수 있는 장점이 있다.

【대표도】

도 2

【색인어】

발광 소자, LED, 발광 효율, 외부 양자 효율, 질화물 반도체

【명세서】

【발명의 명칭】

발광 소자 및 이의 제조 방법 {Light-emitting device and Method of manufacturing the same}

【도면의 간단한 설명】

<1> 도 1은 종래 발광 소자를 도시한 단면도.

<2> 도 2는 본 발명의 발광 소자를 설명하기 위한 개념 단면도.

<3> 도 3a 및 도 3b는 본 발명에 따른 제 1 실시예의 제조 공정을 설명하기 위한 단면도.

<4> 도 4a 내지 도 4d는 본 발명에 따른 제 2 실시예의 제조 공정을 설명하기 위한 단면도.

<5> 도 5a 내지 도 5d는 본 발명에 따른 제 3 실시예의 제조 공정을 설명하기 위한 단면도.

<6> 도 6a 및 도 6b는 각각 종래 기술과 본 발명에 따른 발광 소자의 효과를 설명하기 위한 개념 단면도.

<7> <도면의 주요 부분에 대한 부호의 설명>

<8> 1 : 기판 2 : N형 반도체층

<9> 3 : 활성층 4 : P형 반도체층

<10> 10 : 기판 20 : N형 반도체층

<11> 30 : 활성층 40 : P형 반도체층

<12> 50 : P형 본딩 패드 55 : N형 본딩 패드

<13> 60 : 배선

【발명의 상세한 설명】

【발명의 목적】

【발명이 속하는 기술분야 및 그 분야의 종래기술】

<14> 본 발명은 발광 소자 및 이의 제조 방법에 관한 것으로, 보다 상세하게는 질화물계 반도체 발광 소자에 있어서 발광 효율과 휘도를 향상시키기 위한 발광 소자 및 이의 제조 방법에 관한 것이다.

<15> 발광 소자(light emission diode; LED)는 반도체의 p-n 접합 구조를 이용하여 주입된 소수 캐리어(전자 또는 양공)를 만들고 이들의 재결합에 의하여 소정의 빛을 발산하는 소자를 지칭하며, GaAs, AlGaAs, GaN, InGaN, AlGaInP 등의 화합물 반도체(compound semiconductor) 재료의 변경을 통해 발광원을 구성함으로써 다양한 색을 구현할 수 있다. 예를 들어 GaAsP 등을 이용하여 적색 발광 소자를 형성할 수 있고, GaP, InGaN 등을 이용하여 녹색 발광 소자를 형성할 수 있고, InGaN/GaN 더블 헤테로(double hetero) 구조를 이용하여 청색 발광 소자를 형성할 수 있고, AlGaN/GaN 또는 AlGaN/AlGaN 구조를 이용하여 UV 발광 소자를 형성할 수 있다. 특히, GaN은 상온에서 3.4eV의 직접 천이형 밴드갭(direct bandgap)을 가지며 질화인듐(InN), 질화알루미늄(AlN) 같은 물질과 조합하여 1.9eV (InN)에서 3.4eV (GaN),

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6.2eV (AlN)까지 직접 에너지 밴드갭을 가지고 있어서 가시광에서부터 자외선 영역까지 넓은 파장 영역 때문에 광소자의 응용 가능성이 매우 큰 물질이다. 이처럼 파장 조절이 가능하여 단파장 영역의 적색, 녹색 및 청색 발광 소자에 의한 천연색(full-color) 구현이 가능해짐으로써 디스플레이 영역은 물론 일반 조명시장으로의 파급 효과가 매우 커질 것으로 예상된다.

<16> 발광 소자는 기존의 전구 또는 형광등에 비해 소모 전력이 작고 수명이 길며, 협소한 공간에 설치 가능하고 진동에 강한 특성을 보인다. 이러한 발광 소자는 표시 소자 및 백라이트로 이용되고 있으며, 소모 전력의 절감과 내구성 측면에서 우수한 특성을 갖기 때문에 최근 일반 조명 용도로 이를 적용하기 위해 활발한 연구가 진행중이다. 이후, 대형 LCD-TV 백라이트, 자동차 헤드라이트, 일반 조명에까지 응용이 확대될 것으로 예상되며, 이를 위해서는 발광 소자의 발광 효율의 개선이 필요하고, 열방출 문제를 해결하여야 하며, 발광 소자의 고휘도화, 고출력화를 달성하여야 한다.

<17> 현재 발광 소자의 성능을 높이기 위한 많은 기술들이 개발되고 있다. 발광 소자의 성능을 나타내는 지표는 발광 효율(lm/W), 내부 양자 효율(%), 외부 양자 효율(%), 추출 효율(%) 등 여러 가지가 있는데, 추출 효율은 발광 소자에 주입된 전자와 발광 소자 밖으로 방출되는 광자의 비에 의하여 결정되며 추출 효율이 높을수록 발광 소자가 밝은 것을 의미한다. 발광 소자의 추출 효율은 칩의 모양이나 표면 형태, 칩의 구조, 패키징 형태에 의하여 많은 영향을 받기 때문에 발광 소자를 설계할 때 세심한 주의가 필요하다.

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<18> 도 1은 종래 발광 소자를 도시한 단면도이다.

<19> 도면을 참조하면, 발광 소자는 기판(1)과, 기판(1) 상에 형성된 N형 반도체층(2)과, 상기 N형 반도체층(2)의 일부에 형성된 활성층(3)과, P형 반도체층(4)을 포함한다. 이는 상기 기판(1) 상에 N형 반도체층(2), 활성층(3), P형 반도체층(4)을 순차적으로 형성한 후, 소정 영역의 P형 반도체층(4)과 활성층(3)을 식각하여 N형 반도체층(2)의 일부를 노출시키고, 그 노출된 N형 반도체층(2) 상면과 P형 반도체층(2) 상면으로 각각 소정의 전압을 인가하기 위한 것이다.

<20> 발광 소자의 활성층에서 생성된 광은 칩의 6개의 면으로부터 방출되고, 광추출 효율은 일반적으로 광의 임계각에 의하여 결정된다. 그러나 종래 발광 소자는 N형 반도체층을 노출시키기 위해 식각할 때, P형 반도체층과 활성층의 측면이 수직 가공되어 발광 소자의 내부에서 생성된 광의 일부가 수평면으로부터 수직으로 가공된 식각면에서 전반사된다. 그리하여 전반사되는 상당량의 광은 내부 반사에 의하여 밖으로 방출되지 못한채 발광 소자 내부에서 소멸된다. 즉, 전기 에너지가 빛 에너지로 변환되어 소자의 외부로 빠져나오는 발광 효율이 낮은 문제점이 있다.

【발명이 이루고자 하는 기술적 과제】

<21> 본 발명은 상기 문제점을 해결하기 위한 것으로, 발광 효율, 외부 양자 효율, 추출 효율 등의 특성을 향상시키고 신뢰성을 확보하여, 고광도, 고휘도의 광을 발광할 수 있는 발광 소자 및 이의 제조 방법을 제공하는 것을 목적으로 한다.

【발명의 구성】

<22> 상술한 목적을 달성하기 위하여, 본 발명은 기판, 상기 기판 상에 형성된 N형 반도체층 및 상기 N형 반도체층 상에 형성된 P형 반도체층을 포함하고, 상기 N형 반도체층 또는 P형 반도체층을 포함하는 측면이 수평면으로부터 20 내지 80° 의 기울기를 갖는 것을 특징으로 하는 발광 소자를 제공한다.

<23> 또한, 기판 상에 N형 반도체층, 상기 N형 반도체층의 일부에 형성된 P형 반도체층을 포함하는 발광 셀을 다수개 포함하고, 상기 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층이 연결되고, 상기 발광 셀의 N형 반도체층 또는 P형 반도체층을 포함하는 측면이 수평면으로부터 20 내지 80° 의 기울기를 갖는 것을 특징으로 하는 발광 소자를 제공한다. 상기 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층을 연결하기 위한 배선을 더 포함할 수 있다.

<24> 상기 P형 반도체층 상에 투명 전극층을 더 포함할 수 있으며, 상기 P형 반도체층과 상기 N형 반도체층 상에 Cr 또는 Au를 포함한 P형 오믹금속층과 N형 오믹금속층을 각각 더 포함할 수 있다.

<25> 또한 본 발명은 기판 상에 N형 반도체층, P형 반도체층을 순차적으로 형성하는 단계, 상기 P형 반도체층 상에 측면이 수평면으로부터 수직이 아닌 소정의 기울기를 갖는 식각 마스크 패턴을 형성하는 단계, 상기 식각 마스크 패턴에 의해 노출된 P형 반도체층과, 상기 식각 마스크 패턴을 제거하는 단계를 포함하는 발광 소자의 제조 방법을 제공한다.

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<26> 상기 식각 마스크 패턴을 형성하는 단계는, 3 내지 50㎛ 두께의 감광막을 이용할 수 있다.

<27> 상기 식각 마스크 패턴을 형성하는 단계는, 상기 P형 반도체층 상에 상기 감광막을 도포하는 단계, 소정의 마스크 패턴에 따라 상기 감광막을 노광하는 단계, 상기 노광 후 베이킹 공정 없이 현상하는 단계를 포함할 수 있다.

<28> 또한, 상기 식각 마스크 패턴을 형성하는 단계는, 상기 P형 반도체층 상에 상기 감광막을 도포하는 단계, 소정의 마스크 패턴에 따라 상기 감광막을 노광하는 단계, 100℃ 내지 140℃의 온도에서 하드 베이킹을 하는 단계 및 현상하는 단계를 포함할 수 있다.

<29> 상기 발광 소자의 제조 방법에 있어서, 상기 P형 반도체층의 제거로 인해 노출된 N형 반도체층의 일부를 제거하여 다수개의 발광 셀을 형성하는 단계 및 브리지 배선을 통해 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층을 연결하는 단계를 더 포함할 수 있으며, 상기 브리지 배선은 브리지(Bridge) 공정 또는 스탭 커버(Step Cover) 공정을 통해 일 발광 셀의 N형 반도체층과 인접한 다른 일 발광 셀의 P형 반도체층을 연결할 수 있다.

<30> 또한 상기 P형 반도체층과 상기 식각 마스크 패턴을 제거하는 단계 이후에, 상기 기판의 배면을 소정 두께 제거하는 단계 및 상기 기판의 배면에 Al, Ti, Ag, W, Ta, Ni, Ru 또는 그 합금을 증착하는 단계를 더 포함할 수 있다.

<31> 이하, 첨부된 도면을 참조하여 본 발명에 의한 발광 소자 및 이의 제조 방법

에 대하여 상세히 설명하기로 한다. 그러나 본 발명은 이하에서 개시되는 실시예에 한정되는 것이 아니라 서로 다른 다양한 형태로 구현될 것이며, 단지 본 실시예는 본 발명의 개시가 완전하도록 하며, 통상의 지식을 가진 자에게 발명의 범주를 완전하게 알려주기 위해 제공되는 것이다.

<32> 도 2는 본 발명의 발광 소자를 설명하기 위한 개념 단면도이다.

<33> 도면을 참조하면, 발광 소자는 기판(10)과, 기판(10) 상에 순차적으로 형성된 N형 반도체층(20), 활성층(30) 및 P형 반도체층(40)을 포함한다. 상기 P형 반도체층(40), 활성층(30), 소정 부분의 N형 반도체층(20)의 측면은 수평면으로부터 80 내지 20° 의 기울기를 갖고, 이러한 측면으로부터 광의 임계각을 변화시키고 용이하게 광을 추출할 수 있어 발광 소자의 발광 효율을 개선할 수 있다.

<34> 도 3a 내지 도 3b는 본 발명에 따른 제 1 실시예의 제조 공정을 설명하기 위한 단면도들이다.

<35> 도 3a를 참조하면, 기판(10) 상에 N형 반도체층(20), 활성층(30) 및 P형 반도체층(40)을 순차적으로 형성한다.

<36> 기판(10)은 발광 소자를 제작하기 위한 통상의 웨이퍼를 지칭하는 것으로, Al_2O_3, SiC, ZnO, Si, GaAs, GaP, $LiAl_2O_3$, BN, AlN 및 GaN 중 적어도 어느 하나의 기판(10)을 사용한다. 본 실시예에서는 사파이어로 구성된 결정 성장 기판을 사용한다.

<37> 상기 기판(10) 상에 결정 성장시 기판(10)과 후속층들의 격자 부정합을 줄이기 위한 버퍼층(미도시)을 더 형성할 수 있다. 버퍼층은 반도체 재료인 GaN 또는 AlN을 포함하여 형성할 수 있다.

<38> N형 반도체층(20)은 전자가 생성되는 층으로서, N형 불순물이 주입된 질화갈륨(GaN)을 사용하는 것이 바람직하고, 이에 한정되지 않고 다양한 반도체 성질의 물질층이 가능하다. 본 실시예에서는 N형 $Al_xGa_{1-x}N(0\leq x\leq 1)$을 포함하는 N형 반도체층(20)을 형성한다. 또한, P형 반도체층(40)은 정공이 생성되는 층으로서, P형 불순물이 주입된 질화갈륨(GaN)을 사용하는 것이 바람직하고, 이에 한정되지 않고 다양한 반도체 성질의 물질층이 가능하다. 본 실시예에서는 P형 $Al_xGa_{1-x}N(0\leq x\leq 1)$을 포함하는 P형 반도체층(40)을 형성한다. 뿐만 아니라 상기 반도체층으로 InGaN을 사용할 수 있다. 또한 상기의 N형 반도체층(20) 및 P형 반도체층(40)은 다층막으로 형성할 수도 있다.

<39> 활성층(30)은 소정의 밴드 갭을 가지며 양자 우물이 만들어져 전자 및 정공이 재결합되는 영역으로서, InGaN을 포함하여 이루어질 수 있다. 활성층(30)을 이루는 물질의 종류에 따라 전자 및 전공이 결합하여 발생하는 발광 파장이 변화된다. 따라서, 목표로 하는 파장에 따라 활성층(30)에 포함되는 반도체 재료를 조절하는 것이 바람직하다.

<40> 상술한 물질층들은 유기금속 화학 증착법(MOCVD; Metal Organic Chemical Vapor Deposition), 화학 증착법(CVD; Chemical Vapor Deposition), 플라즈마 화학

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증착법(PCVD; Plasma-enhanced Chemical Vapor Deposition), 분자선 성장법(MBE; Molecular Beam Epitaxy), 수소화물 기상 성장법(HVPE; Hydride Vapor Phase Epitaxy) 등을 포함한 다양한 증착 및 성장 방법을 통해 형성된다.

<41> 이후, 소정의 식각 공정을 통해 P형 반도체층(40) 및 활성층(30)의 일부를 제거하여 N형 반도체층(20)의 일부를 노출시킨다. P형 반도체층(40) 상에 식각 마스크 패턴을 형성한 다음, 건식 또는 습식 식각 공정을 실시하여 P형 반도체층(40) 및 활성층(30)을 제거하여 N형 반도체층(20)을 노출시킨다.

<42> 일반적으로 상기 식각 공정을 위하여 P형 반도체층 상면에 1 내지 2㎛ 두께로 감광막(photoresist)을 도포한 후, 80 내지 90℃의 온도에서 소프트 베이킹(soft baking)을 한다. 다음으로, 소정의 포토 마스크(photo mask)를 통해 자외선(UV) 영역의 빛을 조사하여 마스크 상에 형성된 패턴을 도포된 감광막에 전사하는 노광(exposure) 공정을 진행한다. 이후, 100 내지 120℃의 온도에서 하드 베이킹(hard baking)을 하고, 노광 공정을 통해 상대적으로 결합이 약해져 있는 부분의 감광막을 용제를 사용하여 녹여내는 현상(developing) 공정을 진행한다. 이러한 과정을 통해 상기 P형 반도체층(40) 상에 소정의 식각 마스크 패턴이 형성된다.

<43> 그러나 본 실시예는 상기 식각 마스크 패턴을 형성할 때, 3 내지 50㎛ 두께로 감광막을 종래에 비해 두껍게 도포하고 소프트 베이킹을 거쳐 노광 공정을 실시한다. 그 다음에 하드 베이킹을 통하지 않고 바로 현상하면, 남아있는 감광막의 현상된 측면은 수평면으로부터 50 내지 80° 정도의 기울기를 갖는 경사진 면을 형성하게 된다. 이어서, 이러한 측면의 기울기를 갖는 식각 마스크 패턴을 사용하여 노

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출된 영역의 P형 반도체층(40), 활성층(30), 소정의 N형 반도체층(20)을 식각하면, 식각된 P형 반도체층(40), 활성층(30), 소정의 N형 반도체층(20)의 측면은 마찬가지로 수평면으로부터 50 내지 80° 정도의 기울기를 갖는 경사진 면을 얻을 수 있다.

<44> 즉, 도 3a의 P형 반도체층(40) 상에 3 내지 50㎛ 두께로 감광막을 두껍게 도포하여 노광 후 하드 베이킹 없이 바로 현상한 식각 마스크 패턴을 형성한다. 상기 식각 마스크 패턴에 의해 노출된 P형 반도체층(40), 활성층(30)을 유도 결합 플라즈마(ICP; Inductive Coupled Plasma) 또는 건식 식각 공정을 통해 제거하여 N형 반도체층(20)을 노출시킨다. 노출된 N형 반도체층(20)의 일부를 더 제거할 수 있다. 이후, 식각 마스크 패턴을 제거하면, 도 3b에 도시한 바와 같이 P형 반도체층(40), 활성층(30), 일부 N형 반도체층(20)의 측면이 수평면으로부터 수직(90°)이 아닌, 소정의 기울기를 갖는 발광 소자를 제조할 수 있다.

<45> 또한, 도 3a의 P형 반도체층(40) 상에 3 내지 50㎛ 두께로 감광막을 두껍게 도포하여 노광 후 하드 베이킹을 실시하는 경우에, 하드 베이킹 온도를 100℃ 내지 140℃로 하여 진행하고 현상을 하게 되면, 현상된 감광막의 측면이 수평면으로부터 80° 에서 20° 까지의 기울기를 갖도록 식각된 측면을 얻을 수 있다. 예를 들어, 100℃의 온도에서 하드 베이킹을 하는 경우에 수평면으로부터 80° 정도의 기울기를 갖는 식각 마스크 패턴을 얻을 수 있으며, 이를 이용하여 P형 반도체층(40), 활성층(30), 일부 N형 반도체층(20)의 측면이 수평면으로부터 80° 정도의 기울기를 갖도록 할 수 있다. 또한, 140℃의 온도에서 하드 베이킹을 하는 경우에 수평면으

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로부터 20° 정도의 기울기를 갖는 식각 마스크 패턴을 얻을 수 있으며, 이를 이용하여 P형 반도체층(40), 활성층(30), 일부 N형 반도체층(20)의 측면이 수평면으로부터 20° 정도의 기울기를 갖도록 할 수 있다.

<46> 이와 같이 3 내지 50㎛ 두께의 감광막을 노광 후 100℃ 내지 140℃의 온도에서 하드 베이킹을 하고 현상한 식각 마스크 패턴을 사용함으로써, 식각된 P형 반도체층(40), 활성층(30), 소정의 N형 반도체층(20)의 측면이 마찬가지로 수평면으로부터 80° 에서 20° 까지의 기울기를 갖도록 식각된 측면을 얻을 수 있다. 그리하여 발광층의 내부에서 생성된 광은 다양한 기울기를 갖도록 식각된 측면에 전반사되지 않고 발광 소자의 외부로 빠져나가게 된다.

<47> 상기 P형 반도체층(40) 상부에 P형 반도체층(40)의 저항을 줄이고 광의 투과율을 향상시키기 위해 투명전극층을 더 형성할 수 있으며, P형 반도체층(40) 또는 노출된 N형 반도체층(20) 상부에 전류의 공급을 원활히 하기 위한 별도의 오믹금속층을 더 형성할 수도 있다. 상기 투명전극층으로는 ITO(Indium Tin Oxide), ZnO 또는 전도성을 갖는 투명 금속을 사용할 수 있고, 상기 오믹금속층으로는 Cr, Au를 사용할 수 있다. 또한, 전압의 인가를 위해 P형 반도체층(40)의 상부에 P형 전극을 더 형성할 수 있고, N형 반도체층(20)의 상부에 N형 전극을 더 형성할 수 있다.

<48> 또한 발광 소자의 열 방출 특성을 향상시키기 위해 상기 기판(10)의 배면을 소정 두께 제거한 후에 Al, Ti, Ag, W, Ni, Ta, Ru 또는 그 합금을 기판(10)의 배면에 증착시킬 수 있다.

<49> 도면에서 볼 수 있듯이, 다수 개의 발광 소자를 하나의 기판(10) 상에 제작

할 수 있고, 이러한 경우 추후에 각각의 발광 소자로 절단하여 사용하게 된다. 이때, 도 3b의 A 부분은 이러한 다수 개의 발광 소자를 개별적으로 절단하기 위한 절단부이다.

<50> 이로써 P형 반도체층(40), 활성층(30), N형 반도체층(20) 측면의 일부가 수평면으로부터 수직이 아닌, 소정의 기울기를 갖는 발광 소자를 제조할 수 있다.

<51> 상술한 본 발명의 발광 소자의 제조 공정은 일 실시예일뿐 이에 한정되지 않고, 다양한 공정과 제조 방법이 소자의 특성 및 공정의 편의에 따라 변경되거나 추가될 수 있다.

<52> 상술한 바와 같이 본 발명에 따른 발광 소자는 P형 반도체층, 활성층, N형 반도체층의 일부 측면이 수평면으로부터 수직이 아닌, 소정의 기울기를 갖도록 형성함으로써, 종래의 발광 소자에 비하여 발광 효율을 향상시킬 수 있다. 이는 종래의 평탄한 표면에서 반사되었던 광자가 다양한 각의 표면에 의해 반사되지 않고 외부로 빠져나가기 때문이다.

<53> 도 4a 내지 도 4d는 본 발명에 따른 제 2 실시예의 제조 공정을 설명하기 위한 단면도들이다.

<54> 이는 제 1 실시예의 경우와 거의 동일하며, 단지 제 2 실시예는 웨이퍼 레벨에서 다수의 발광 셀을 직렬, 병렬 또는 직병렬 연결하여 소자의 크기를 줄이고, 적정 전압 및 전류에 구동되도록 하여 조명용으로 사용가능하며 교류 전원에서도 구동할 수 있는 발광 소자를 제공한다.

<55> 도 4a를 참조하면, 유기금속 화학 증착법, 화학 증착법, 플라즈마 화학 증착

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법, 분자선 성장법, 수소화물 기상 성장법 등의 다양한 증착 방법을 통해 기판(10) 상에 N형 반도체층(20), 활성층(30) 및 P형 반도체층(40)을 순차적으로 형성한다. 상기 기판(10) 상에 결정 성장시 기판(10)과 후속층들의 격자 부정합을 줄이기 위한 버퍼층을 더 형성할 수 있다. 이는 도 3a의 경우와 동일하며, 이와 중복되는 설명은 생략한다.

<56> 이후, 소정의 식각 공정을 통해 P형 반도체층(40) 및 활성층(30)의 일부를 제거하여 N형 반도체층(20)의 일부를 노출한다. 즉, P형 반도체층(40) 상에 3 내지 50㎛ 두께로 감광막을 두껍게 도포하여 노광 후 하드 베이킹 없이 바로 현상하여 식각 마스크 패턴을 형성한다. 상기 식각 마스크 패턴에 의해 노출된 P형 반도체층(40), 활성층(30)을 유도 결합 플라즈마 또는 건식 식각 공정을 통해 제거하여 N형 반도체층(20)을 노출시킨다. 노출된 N형 반도체층(20)의 일부를 더 제거할 수 있다. 이후, 식각 마스크 패턴을 제거하면, 도 4b에 도시한 바와 같이 P형 반도체층(40), 활성층(30), 소정의 N형 반도체층(20)의 측면이 수평면으로부터 50 내지 80° 정도의 기울기를 갖는 경사진 면을 얻을 수 있다.

<57> 또한 P형 반도체층(40) 상에 3 내지 50㎛ 두께로 감광막을 두껍게 도포하여 노광 후 100℃ 내지 140℃의 온도에서 하드 베이킹을 하고 현상하여 식각 마스크 패턴을 형성한다. 이러한 식각 마스크 패턴에 의해 노출된 P형 반도체층(40) 및 활성층(30)을 식각한 후 식각 마스크 패턴을 제거하여 식각된 P형 반도체층(40) 및 활성층(30)의 측면이 80° 에서 20° 까지의 다양한 기울기를 갖도록 할 수도 있다.

<58> 다음으로 기판(10) 상에 다수 개의 발광 셀을 형성하기 위하여 노출된 N형

반도체층(20)의 소정 영역을 기판(10)이 노출되도록 제거한다. 이를 위해 상기 기판(10)이 노출될 소정 영역을 제외한 모든 부분에 소정의 마스크 패턴을 형성한 다음, 상기 마스크 패턴에 의해 노출된 영역의 N형 반도체층(20)을 식각하여 도 4c에 도시한 바와 같이 다수개의 발광 셀을 전기적으로 분리한다. 이 때, 상술한 공정을 통해 측면이 경사진 마스크 패턴을 형성하여 식각함으로써, 다수개의 발광 셀이 분리되는 N형 반도체층(20)의 측면이 수평면으로부터 수직이 아닌, 다양한 기울기를 갖도록 할 수도 있다.

<59> P형 반도체층(40) 상부에 P형 반도체층(40)의 저항을 줄이고 광의 투과율을 향상시키기 위해 ITO와 같은 투명전극층을 더 형성할 수 있으며, P형 반도체층(40) 또는 노출된 N형 반도체층(20) 상부에 Cr, Au를 사용하여 전류의 공급을 원활히 하기 위한 별도의 오믹금속층을 더 형성할 수도 있다.

<60> 도 4d를 참조하면, 소정의 배선 형성 공정을 통해 인접한 발광 셀간의 N형 반도체층(20)과 P형 반도체층(40)을 연결한다. 즉, 일 발광 셀의 노출된 N형 반도체층(20)과 이와 인접한 다른 일 발광 셀의 P형 반도체층(40)을 배선으로 연결한다. 이 때 브리지(Bridge) 공정 또는 스탭 커버(Step Cover) 등의 공정을 통해 각기 인접한 발광 셀의 N형 반도체층(20)과 P형 반도체층(40) 간을 전기적으로 연결하는 도전성 배선을 형성한다.

<61> 상술한 브리지 공정은 에어브리지 공정이라고도 하며, 서로 연결할 칩 간에 포토 공정을 이용해 감광액을 도포하고 현상하여 감광막 패턴을 형성하고, 그 위에 금속 등의 물질을 진공 증착 등의 방법으로 먼저 박막으로 형성하고, 다시 그 위에

전기 도금(electroplating), 무전해 도금(electroplating) 또는 금속 증착 등의 방법으로 금을 포함하는 도전성 물질을 일정 두께로 도포한다. 이후, 솔벤트 등의 용액으로 감광막 패턴을 제거하면 도전성 물질의 하부는 다 제거되고 브리지 형태의 도전성 물질만이 공간에 형성된다.

<62> 또한, 스탭 커버 공정은 서로 연결할 칩 간에 포토 공정을 이용해 감광액을 도포하고, 현상하여 서로 연결될 부분만을 남기고 다른 부분은 감광막 패턴으로 뒤덮고, 그 위에 전기 도금, 무전해 도금 또는 금속 증착 등의 방법으로 금을 포함하는 도전성 물질을 일정 두께로 도포한다. 이어서, 솔벤트 등의 용액으로 감광막 패턴을 제거하면 도전성 물질이 덮힌 이외의 부분은 다 제거되고 이 덮힌 부분 만이 남아 연결할 칩 사이를 전기적으로 연결시키는 역할을 하게 되다.

<63> 상기의 배선으로는 금속뿐만 아니라 전도성을 갖는 모든 물질들을 사용할 수 있다.

<64> 또한 발광 소자에 외부 전압을 인가하기 위해 일 가장자리에 위치한 발광 셀의 P형 반도체층(40)에 P형 본딩 패드(50)를 형성하고, 다른 일 가장자리에 위치한 발광 셀의 노출된 N형 반도체층(20) 상에 N형 본딩 패드(55)를 형성한다.

<65> 이로써 P형 반도체층(40), 활성층(30), N형 반도체층(20) 측면의 일부가 수평면으로부터 수직이 아닌, 소정의 기울기를 갖는 발광 셀이 다수개 연결되어 형성된 발광 소자를 제조할 수 있다.

<66> 상술한 본 발명의 발광 소자의 제조 공정은 일 실시예일뿐 이에 한정되지 않고, 다양한 공정과 제조 방법이 소자의 특성 및 공정의 편의에 따라 변경되거나 추

가될 수 있다. 예를 들어 발광 소자의 열 방출 특성을 향상시키기 위해 상기 기판의 배면을 소정 두께 제거한 후에 Al, Ti, Ag, W, Ni, Ta, Ru 또는 그 합금을 기판의 배면에 증착시킬 수 있다.

<67> 도 5a 내지 도 5d는 본 발명에 따른 제 3 실시예의 제조 방법을 설명하기 위한 단면도들이다.

<68> 이는 제 2 실시예의 경우와 거의 동일하며, 단지 제 2 실시예는 N형 반도체층(20)을 먼저 노출시킨 다음 발광 셀간의 분리를 위해 노출된 N형 반도체층(20)의 일부를 제거하였으나, 제 3 실시예는 다수개의 발광 셀을 먼저 분리한 후 N형 반도체층(20)의 일부를 노출시킨 것이다. 상기 제 2 실시예의 경우와 중복되는 설명은 생략한다.

<69> 도 5a를 참조하면, 기판(10) 상에 순차적으로 형성된 N형 반도체층(20), 활성층(30) 및 P형 반도체층(40)의 일부를 제거하여 다수개의 발광 셀을 형성한다. 이를 위해, P형 반도체층(40) 상에 3 내지 50㎛ 두께로 감광막을 두껍게 도포하여 노광 후 하드 베이킹 없이 바로 현상하여 식각 마스크 패턴을 형성한다. 상기 식각 마스크 패턴에 의해 노출된 P형 반도체층(40), 활성층(30), 소정의 N형 반도체층(20)과 상기 식각 마스크 패턴을 제거하여 발광 셀을 분리한다. 그리하여 도시한 바와 같이 P형 반도체층(40), 활성층(30), N형 반도체층(20)의 전 측면이 수평면으로부터 50 내지 80° 정도의 기울기를 갖는 경사진 면을 얻을 수 있다. 또한 P형 반도체층(40) 상에 3 내지 50㎛ 두께로 감광막을 두껍게 도포하여 노광 후 100℃ 내지 140℃의 온도에서 하드 베이킹을 하고 현상한 식각 마스크 패턴을 사용하여 P

형 반도체층(40), 활성층(30), N형 반도체층(20)을 제거함으로써, P형 반도체층(40), 활성층(30), N형 반도체층(20)의 전 측면을 다양한 기울기로 형성할 수 있다.

<70> 이후, 도 5b에 도시한 바와 같이 소정의 식각 공정을 통해 P형 반도체층(40) 및 활성층(30)의 일부를 제거하여 N형 반도체층(20)의 일부를 노출한다.

<71> 또한 P형 반도체층(40) 상부에 P형 반도체층(40)의 저항을 줄이고 광의 투과율을 향상시키기 위해 투명전극층을 더 형성할 수 있으며, P형 반도체층(40) 또는 노출된 N형 반도체층(20) 상부에 전류의 공급을 원활히 하기 위한 별도의 오믹금속층을 더 형성할 수도 있다. 상기 투명전극층으로는 ITO(Indium Tin Oxide), ZnO 또는 전도성을 갖는 투명 금속을 사용할 수 있고, 상기 오믹금속층으로는 Cr, Au를 사용할 수 있다.

<72> 도 5c를 참조하면, 브리지 공정 또는 스탭 커버 등의 공정을 통해 인접한 발광 셀 간의 N형 반도체층(20)과 P형 반도체층(40)을 연결한다.

<73> 또한 발광 소자에 외부 전압을 인가하기 위해 일 가장자리에 위치한 발광 셀의 P형 반도체층(40)에 P형 본딩 패드(50)를 형성하고, 다른 일 가장자리에 위치한 발광 셀의 노출된 N형 반도체층(20) 상에 N형 본딩패드(55)를 형성한다.

<74> 상술한 본 발명의 발광 소자의 제조 공정은 일 실시예일뿐 이에 한정되지 않고, 다양한 변형과 다양한 물질막이 더 추가될 수 있다. 예를 들어 발광 소자의 열 방출 특성을 향상시키기 위해 상기 기판의 배면을 소정 두께 제거한 후에 Al, Ti, Ag, W, Ta, Ni, Ru 또는 그 합금을 기판의 배면에 증착시킬 수 있다.

<75> 또한, 도 5a에 도시한 바와 같이 측면이 다양한 기울기를 갖도록 식각하여 다수개의 발광 셀을 분리한 다음, N형 반도체층(20)을 노출시키기 위해 식각하는 경우에도 마찬가지의 식각 공정을 사용하여 발광 소자를 제조할 수 있다. 즉, 5d에 도시한 바와 같이 N형 반도체층(20)이 노출되도록 식각되는 P형 반도체층(40)과 활성층(30)의 측면이 다양한 기울기를 갖도록 형성할 수 있다. 이러한 발광 소자는 종래 수직으로 식각된 표면에서 반사되었던 광자가 다양한 각의 표면에 의해 반사되지 않고 외부로 빠져나가기 때문에 더욱 향상된 발광 효율을 얻을 수 있다.

<76> 이로써 P형 반도체층(40), 활성층(30), N형 반도체층(20)의 전체 측면이 수평면으로부터 수직이 아닌, 소정의 기울기를 갖는 발광 셀이 다수개 연결되어 형성된 발광 소자를 제조할 수 있다.

<77> 도 6a 및 도 6b는 각각 종래 기술과 본 발명에 따른 발광 소자의 효과를 설명하기 위한 개념 단면도이다.

<78> 발광 소자의 광효율은 내부 양자 효율과 외부 양자 효율로 나타낼 수 있는데, 내부 양자 효율은 활성층의 설계나 품질에 따라서 결정된다. 외부 양자 효율의 경우 활성층에서 생성되는 광자가 발광 소자의 외부로 나오는 정도에 따라서 결정된다. 종래 기술에 따른 발광 소자를 도시한 도 6a를 살펴보면, 반도체층의 측면이 수평면으로부터 수직으로 형성되는 경우에, 일부의 광자가 반도체층의 측면에서 투과하지 못하고 반사되어 나오며, 전반사된 광은 외부로 투과하지 못하고 발광 소자 내부에서 소멸된다. 그러나, 본 발명에 따른 발광 소자를 도시한 도 6b에서와 같이 반도체층의 측면을 수평면으로부터 수직이 아닌, 소정의 기울기를 갖는 경우

에, 경사진 측면이 광의 임계각을 변화시켜 보다 용이하게 광을 추출할 수 있게 돕는다. 따라서 활성층에서 발생한 광이 전반사되지 않고 발광 소자의 외부로 방출될 확률이 높아져 외부 양자 효율이 현저하게 향상된다.

【발명의 효과】

<79> 본 발명에 의한 발광 소자 및 이의 제조 방법은 수평면으로부터 수직이 아닌 소정의 기울기를 갖는 반도체층의 측면에서 발생한 광이 전반사되지 않고 발광 소자의 외부로 방출됨으로써, 더욱 향상된 광추출 효율, 외부 양자 효율, 발광 효율 등의 특성을 얻을 수 있다. 또한, 본 발명의 발광 소자는 고광도, 고휘도의 광을 발광하는 것으로, 우수한 광특성이 요구되는 다양한 제품 분야에 응용될 수 있다는 장점이 있다.

【특허청구범위】

【청구항 1】

기판;

상기 기판 상에 형성된 N형 반도체층; 및

상기 N형 반도체층 상에 형성된 P형 반도체층을 포함하고,

상기 N형 반도체층 또는 P형 반도체층을 포함하는 측면이 수평면으로부터 20 내지 80° 의 기울기를 갖는 것을 특징으로 하는 발광 소자.

【청구항 2】

기판 상에 N형 반도체층, 상기 N형 반도체층의 일부에 형성된 P형 반도체층을 포함하는 발광 셀을 다수개 포함하고,

상기 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층이 연결되고, 상기 발광 셀의 N형 반도체층 또는 P형 반도체층을 포함하는 측면이 수평면으로부터 20 내지 80° 의 기울기를 갖는 것을 특징으로 하는 발광 소자.

【청구항 3】

청구항 2에 있어서,

상기 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층을 연결하기 위한 배선을 더 포함하는 것을 특징으로 하는 발광 소자.

【청구항 4】

청구항 1 내지 청구항 3 중 어느 한 항에 있어서,

상기 P형 반도체층 상에 투명 전극층을 더 포함하는 것을 특징으로 하는 발광 소자.

【청구항 5】

청구항 1 내지 청구항 3 중 어느 한 항에 있어서,

상기 P형 반도체층과 상기 N형 반도체층 상에 Cr 또는 Au를 포함한 P형 오믹 금속층과 N형 오믹금속층을 각각 더 포함하는 것을 특징으로 하는 발광 소자.

【청구항 6】

기판 상에 N형 반도체층, P형 반도체층을 순차적으로 형성하는 단계;

상기 P형 반도체층 상에 측면이 수평면으로부터 수직이 아닌 소정의 기울기를 갖는 식각 마스크 패턴을 형성하는 단계;

상기 식각 마스크 패턴에 의해 노출된 P형 반도체층과, 상기 식각 마스크 패턴을 제거하는 단계를 포함하는 발광 소자의 제조 방법.

【청구항 7】

청구항 6에 있어서,

상기 식각 마스크 패턴을 형성하는 단계는,

3 내지 50㎛ 두께의 감광막을 이용하는 것을 특징으로 하는 발광 소자의 제조 방법.

【청구항 8】

청구항 7에 있어서,

상기 식각 마스크 패턴을 형성하는 단계는,

상기 P형 반도체층 상에 상기 감광막을 도포하는 단계;

소정의 마스크 패턴에 따라 상기 감광막을 노광하는 단계;

상기 노광 후 베이킹 공정 없이 현상하는 단계를 포함하는 것을 특징으로 하는 발광 소자의 제조 방법.

【청구항 9】

청구항 7에 있어서,

상기 식각 마스크 패턴을 형성하는 단계는,

상기 P형 반도체층 상에 상기 감광막을 도포하는 단계;

소정의 마스크 패턴에 따라 상기 감광막을 노광하는 단계;

100℃ 내지 140℃의 온도에서 하드 베이킹을 하는 단계 및

현상하는 단계를 포함하는 것을 특징으로 하는 발광 소자의 제조 방법.

【청구항 10】

청구항 6 내지 청구항 9 중 어느 한 항에 있어서,

상기 P형 반도체층의 제거로 인해 노출된 N형 반도체층의 일부를 제거하여 다수개의 발광 셀을 형성하는 단계; 및

브리지 배선을 통해 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광

셀의 P형 반도체층을 연결하는 단계를 더 포함하는 것을 특징으로 하는 발광 소자의 제조 방법.

【청구항 11】

청구항 10에 있어서,

상기 브리지 배선은 브리지(Bridge) 공정 또는 스탭 커버(Step Cover) 공정을 통해 일 발광 셀의 N형 반도체층과 인접한 다른 일 발광 셀의 P형 반도체층을 연결하는 것을 특징으로 하는 발광 소자의 제조 방법.

【청구항 12】

청구항 6 내지 청구항 9 중 어느 한 항에 있어서,

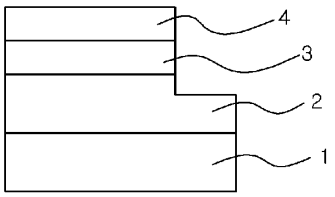
상기 P형 반도체층과 상기 식각 마스크 패턴을 제거하는 단계 이후에,

상기 기판의 배면을 소정 두께 제거하는 단계; 및

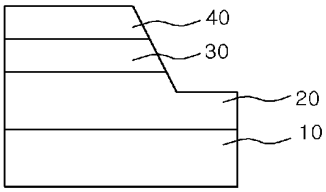
상기 기판의 배면에 Al, Ti, Ag, W, Ta, Ni, Ru 또는 그 합금을 증착하는 단계를 더 포함하는 것을 특징으로 하는 발광 소자의 제조 방법.

【도면】

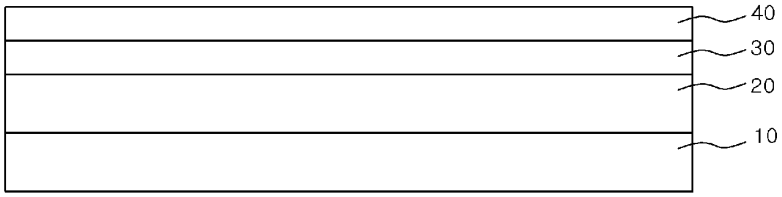
【도 1】



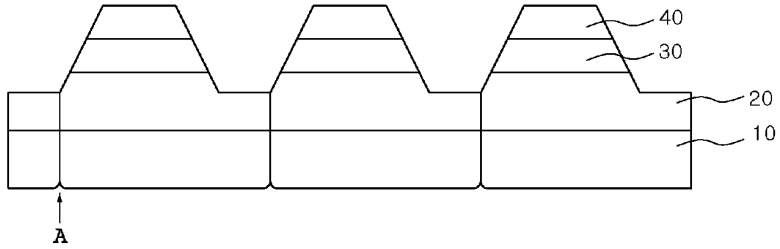
【도 2】



【도 3a】



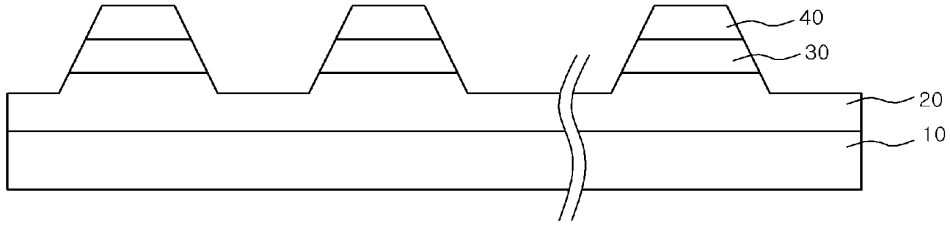
【도 3b】



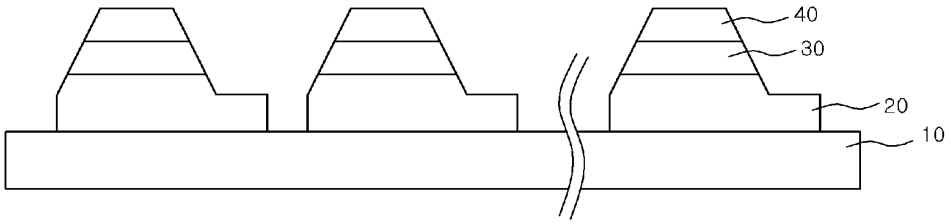
【도 4a】



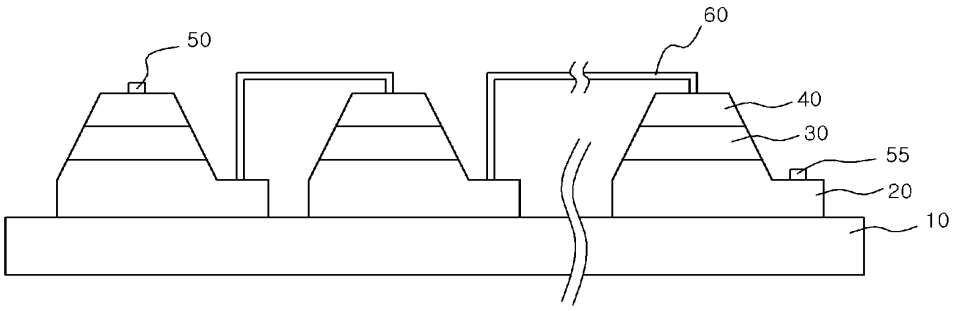
【도 4b】



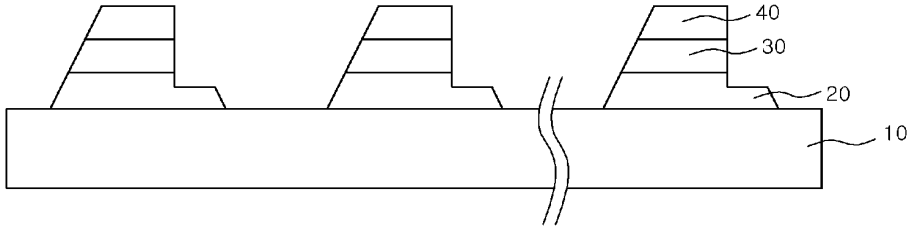
【도 4c】



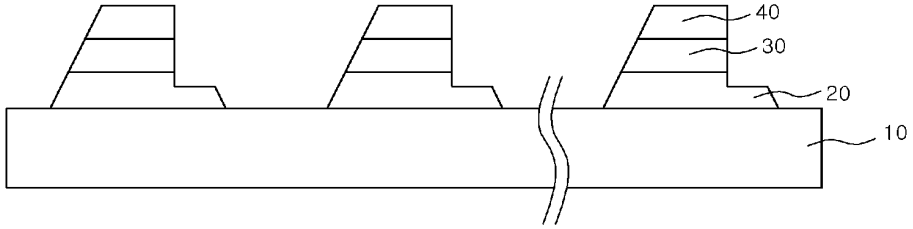
【도 4d】



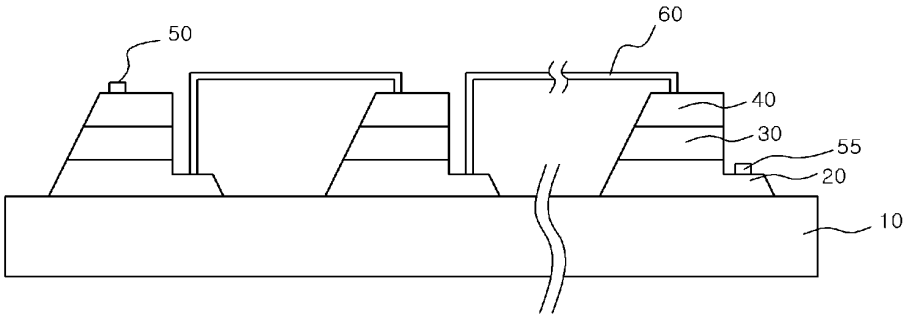
【도 5a】



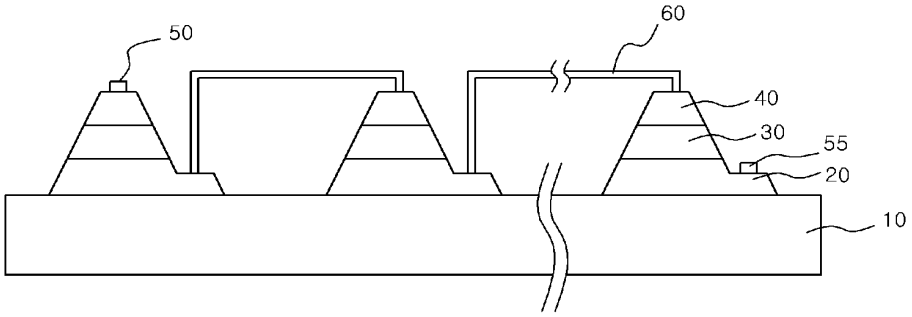
【도 5b】



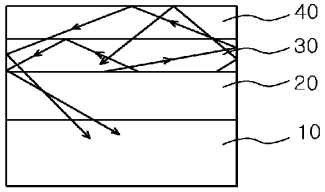
【도 5c】



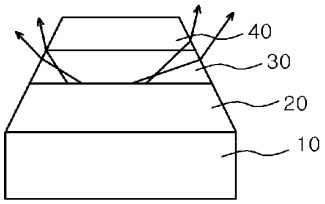
【도 5d】



【도 6a】



【도 6b】



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KOREAN INTELLECTUAL PROPERTY OFFICE

별첨 사본은 아래 출원의 원본과 동일함을 증명함.

This is to certify that the following application annexed hereto is a true copy from the records of the Korean Intellectual Property Office

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출 원 일 자 : Date of Application		2005년 06월 24일 JUN 24, 2005
출 원 인 : Applicant(s)		서울옵토디바이스주식회사 SEOUL OPTO DEVICE CO., LTD.

2006 년 07 월 10 일

특 허 청
COMMISSIONER

【서지사항】

【서류명】 특허출원서

【권리구분】 특허

【수신처】 특허청장

【제출일자】 2005.06.24

【발명의 국문명칭】 복수 셀의 단일 발광 소자 및 이의 제조 방법

【발명의 영문명칭】 Light-emitting device having arrayed cells and Method of manufacturing the same

【출원인】

【명칭】 서울옵토디바이스 주식회사

【출원인코드】 1-2003-032642-0

【대리인】

【성명】 남승희

【대리인코드】 9-2003-000036-2

【포괄위임등록번호】 2004-031626-3

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【성명의 영문표기】 LEE,Jong Lam

【주민등록번호】 580406-1051917

【우편번호】 790-834

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【국적】 KR

【발명자】

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【성명의 영문표기】 LEE,Jae Ho

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【우편번호】 449-531

【주소】 경기 용인시 성복동 LG3차빌리지 309-1405

【국적】 KR

【발명자】

【성명】 윤여진

【성명의 영문표기】 YOON,Yeo Jin

【주민등록번호】 720715-1446725

【우편번호】 426-738

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【국적】 KR

【발명자】

【성명】 황의진

【성명의 영문표기】 HWANG,Eu Jin

【주민등록번호】 751018-1531013

【우편번호】 429-450

【주소】 경기 시흥시 정왕동 1569-7 303호

【국적】 KR

【심사청구】 청구

【취지】 특허법 제42조의 규정에 의한 출원, 특허법 제60조의 규정에 의한 출원심사를 청구합니다.

대리인 남승희 (인)

【수수료】

【기본출원료】	0 면	38,000 원
【가산출원료】	28 면	0 원
【우선권주장료】	0 건	0 원
【심사청구료】	10 항	429,000 원
【합계】	467,000 원	

【감면사유】 중소기업

【감면후 수수료】 233,500 원

【첨부서류】 1.중소기업기본법시행령 제2조에의한 중소기업에 해당함을 증명하는 서류[사업자등록증및 원천징수이행상황신고서]_1통

【요약서】

【요약】

본 발명은 N형 반도체층과 상기 N형 반도체층 상에 형성된 P형 반도체층을 포함하는 다수개의 발광 셀이 형성된 기판 및 상기 기판이 플립칩 본딩되는 서브마운트 기판을 포함하고, 상기 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층이 연결되고, 상기 발광 셀의 적어도 P형 반도체층을 포함하는 측면이 수평면으로부터 수직이 아닌 소정의 기울기를 갖는 것을 특징으로 하는 복수 셀의 단일 발광 소자 및 이의 제조 방법를 제공한다. 본 발명에 의한 발광 소자 및 이의 제조 방법은 발광 효율, 외부 양자 효율, 추출 효율 등의 특성을 향상시키고 신뢰성을 확보하여, 고광도, 고휘도의 광을 발광할 수 있는 장점이 있다.

【대표도】

도 2

【색인어】

플립칩, 발광 소자, LED, 광추출 효율, 발광 효율, 광도

【명세서】

【발명의 명칭】

복수 셀의 단일 발광 소자 및 이의 제조 방법 {Light-emitting device having arrayed cells and Method of manufacturing the same}

【도면의 간단한 설명】

<1> 도 1은 종래의 플립칩 구조의 발광 소자를 도시한 단면도.

<2> 도 2는 본 발명의 발광 소자를 설명하기 위한 개념 단면도.

<3> 도 3a 내지 도 3e는 본 발명에 따른 제 1 실시예의 제조 공정을 설명하기 위한 단면도.

<4> 도 4a 내지 도 4d는 본 발명에 따른 제 2 실시예의 제조 공정을 설명하기 위한 단면도.

<5> 도 5는 본 발명에 따른 제 3 실시예를 도시한 단면도.

<6> <도면의 주요 부분에 대한 부호의 설명>

<7> 10 : 기판 20 : N형 반도체층

<8> 30 : 활성층 40 : P형 반도체층

<9> 50 : N형 금속범프 55 : P형 금속범프

<10> 60 : 배선 100 : 서브 마운트 기판

<11> 110 : N형 본딩패드 115 : P형 본딩패드

<12> 120 : 본딩층

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【발명의 상세한 설명】

【발명의 목적】

【발명이 속하는 기술분야 및 그 분야의 종래기술】

<13> 본 발명은 복수 셀의 단일 발광 소자 및 이의 제조 방법에 관한 것으로, 보다 상세하게는 플립칩(Flip-Chip) 구조의 발광 소자에 있어서 발광 효율과 휘도를 향상시키기 위한 복수 셀의 단일 발광 소자 및 이의 제조 방법에 관한 것이다.

<14> 발광 소자(light emission diode; LED)는 반도체의 p-n 접합 구조를 이용하여 주입된 소수 캐리어(전자 또는 정공)를 만들고 이들의 재결합에 의하여 소정의 빛을 발산하는 소자를 지칭하며, GaAs, AlGaAs, GaN, InGaN, AlGaInP 등의 화합물 반도체(compound semiconductor) 재료의 변경을 통해 발광원을 구성함으로써 다양한 색을 구현할 수 있다. 예를 들어 GaAsP 등을 이용하여 적색 발광 소자를 형성할 수 있고, GaP, InGaN 등을 이용하여 녹색 발광 소자를 형성할 수 있고, InGaN/GaN 더블 헤테로(double hetero) 구조를 이용하여 청색 발광 소자를 형성할 수 있고, AlGaN/GaN 또는 AlGaN/AlGaN 구조를 이용하여 UV 발광 소자를 형성할 수 있다.

<15> 특히, GaN은 상온에서 3.4eV의 직접 천이형 밴드갭(direct bandgap)을 가지며 질화인듐(InN), 질화알루미늄(AlN) 같은 물질과 조합하여 1.9eV (InN)에서 3.4eV (GaN), 6.2eV (AlN)까지 직접 에너지 밴드갭을 가지고 있어서 가시광에서부터 자외선 영역까지 넓은 파장 영역 때문에 광소자의 응용 가능성이 매우 큰 물질이다. 이처럼 파장 조절이 가능하여 단파장 영역의 적색, 녹색 및 청색 발광 소자에 의한 천연색(full-color) 구현이 가능해짐으로써 디스플레이 영역은 물론 일반

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조명 시장으로의 파급 효과가 매우 커질 것으로 예상된다.

<16> 발광 소자는 기존의 전구 또는 형광등에 비해 소모 전력이 작고 수명이 길며, 협소한 공간에 설치 가능하고 진동에 강한 특성을 보인다. 이러한 발광 소자는 표시 소자 및 백라이트로 이용되고 있으며, 소모 전력의 절감과 내구성 측면에서 우수한 특성을 갖기 때문에 최근 일반 조명 용도로 이를 적용하기 위해 활발한 연구가 진행중이다. 이후, 대형 LCD-TV 백라이트, 자동차 헤드라이트, 일반 조명에까지 응용이 확대될 것으로 예상되며, 이를 위해서는 발광 소자의 발광 효율의 개선이 필요하고, 열방출 문제를 해결하여야 하며, 발광 소자의 고휘도화, 고출력화를 달성하여야 한다.

<17> 이러한 문제를 해결하기 위해 최근에 플립칩 형태의 발광 소자에 대한 관심이 날로 높아지고 있다.

<18> 도 1은 종래의 플립칩 구조의 발광 소자를 설명하기 위한 개념 단면도이다.

<19> 도 1을 참조하면, 소정의 기판(1) 상에 N형 반도체층(5), 활성층(6), P형 반도체층(7)을 순차적으로 형성한다. P형 반도체층(7)과 활성층(6)의 일부를 식각함으로써 N형 반도체층(5)을 노출시켜 발광 셀을 형성한다. 또한, 별도의 서브 마운트 기판(2)을 준비하여 제 1 및 제 2 전극(3, 4)을 형성하고, 제 1 전극(3) 상에는 P형 솔더(8)를 형성하고, 제 2 전극(4) 상에는 N형 솔더(9)를 형성한다. 이후, 상기 발광 셀을 상기 서브 마운트 기판(2)에 본딩하되, 발광 셀의 P 전극을 P형 솔더(8)에, N 전극을 N형 솔더(9)에 본딩한다. 발광 셀이 본딩된 기판을 봉지하는 몰딩부(미도시)를 형성하여 발광 소자를 제작한다.

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<20> 이와 같은 종래 플립칩 구조의 발광 소자는 기존의 발광 소자에 비해서 열 방출 효율이 높고, 광의 차폐가 거의 없어 광효율이 기존의 발광 소자에 비해 50% 이상 증가하는 효과가 있고, 발광 소자의 구동을 위한 금선이 필요하지 않기 때문에 여러 소형 패키지에도 많은 응용을 고려하고 있다.

<21> 발광 소자의 발광층에서 생성된 광은 칩의 모든 면으로부터 방출되고, 광추출 효율은 일반적으로 광의 임계각에 의하여 결정된다. 발광 소자의 성능을 나타내는 지표는 발광 효율(lm/W), 내부 양자 효율(%), 외부 양자 효율(%), 추출 효율(%) 등 여러 가지가 있는데, 추출 효율은 발광 소자에 주입된 전자와 발광 소자 밖으로 방출되는 광자의 비에 의하여 결정되며 추출 효율이 높을수록 발광 소자가 밝은 것을 의미한다. 그러나 종래 발광 소자는 N형 반도체층을 노출시키기 위해 식각할 때, P형 반도체층과 활성층의 측면이 수직 가공되어 발광 소자의 내부에서 생성된 광자의 일부가 수평면으로부터 수직으로 가공된 식각면에서 전반사된다. 그리하여 전반사되는 상당량의 광은 내부 반사에 의하여 밖으로 방출되지 못한채 발광 소자 내부에서 소멸된다. 즉, 전기 에너지가 빛 에너지로 변환되어 소자의 외부로 빠져나오는 발광 효율이 낮은 문제점이 있다.

【발명이 이루고자 하는 기술적 과제】

<22> 본 발명은 상술한 문제점을 해결하기 위한 것으로, 플립칩 구조의 발광 소자에 있어서 발광 효율, 외부 양자 효율, 추출 효율 등의 특성을 향상시키고 신뢰성을 확보하여, 고광도, 고휘도의 광을 발광할 수 있는 복수 셀의 단일 발광 소자 및 이의 제조 방법을 제공하는 것을 목적으로 한다.

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【발명의 구성】

<23> 상술한 목적을 달성하기 위하여, 본 발명은 N형 반도체층과 상기 N형 반도체층 상에 형성된 P형 반도체층을 포함하는 다수개의 발광 셀이 형성된 기판 및 상기 기판이 플립칩 본딩되는 서브 마운트 기판을 포함하고, 상기 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층이 연결되고, 상기 발광 셀의 적어도 P형 반도체층을 포함하는 측면이 수평면으로부터 수직이 아닌 소정의 기울기를 갖는 것을 특징으로 하는 복수 셀의 단일 발광 소자를 제공한다. 상기 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층을 연결하기 위한 배선을 더 포함할 수 있다. 상기 소정의 기울기는 20 내지 80° 일 수 있다.

<24> 본 발명은 기판 상에 N형 반도체층과 P형 반도체층을 순차적으로 형성하여 상기 기판 상에 발광 셀을 형성하는 단계, 상기 P형 반도체층 상에 측면이 수평면으로부터 수직이 아닌 소정의 기울기를 갖는 식각 마스크 패턴을 형성하는 단계, 상기 식각 마스크 패턴에 의해 노출된 P형 반도체층과 상기 식각 마스크 패턴을 제거하는 단계 및 상기 기판을 별도의 서브 마운트 기판에 플립칩 본딩하는 단계를 포함하는 발광 소자의 제조 방법을 제공한다.

<25> 상기 기판 상에 발광 셀을 형성하는 단계는 상기 N형 반도체층 및 P형 반도체층의 일부를 제거하여 다수개의 발광 셀을 형성하는 단계를 포함할 수 있고, 상기 P형 반도체층과 상기 식각 마스크 패턴을 제거하는 단계 이후에, 브리지 배선을 통해 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층을

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연결하는 단계를 더 포함할 수 있다. 상기 다수개의 발광 셀을 형성하는 단계는, 상기 P형 반도체층 상에 측면이 수평면으로부터 수직이 아닌 소정의 기울기를 갖는 식각 마스크 패턴을 형성하는 단계, 상기 식각 마스크 패턴에 의해 노출된 P형 반도체층 및 N형 반도체층을 제거하여 다수개의 발광 셀을 형성하는 단계 및 상기 식각 마스크 패턴을 제거하는 단계를 포함할 수 있다. 상기 브리지 배선은 브리지(Bridge) 공정 또는 스탭 커버(Step Cover) 공정을 통해 일 발광 셀의 N형 반도체층과 인접한 다른 일 발광 셀의 P형 반도체층을 연결할 수 있다.

<26> 상기 식각 마스크 패턴을 형성하는 단계는, 3 내지 50㎛ 두께의 감광막을 이용하는 것을 특징으로 할 수 있다.

<27> 상기 식각 마스크 패턴을 형성하는 단계는, 상기 P형 반도체층 상에 상기 감광막을 도포하는 단계, 소정의 마스크 패턴에 따라 상기 감광막을 노광시키는 단계 및 상기 노광 후 베이킹 공정 없이 현상하는 단계를 포함할 수 있다.

<28> 또한, 상기 식각 마스크 패턴을 형성하는 단계는, 상기 P형 반도체층 상에 상기 감광막을 도포하는 단계, 소정의 마스크 패턴에 따라 상기 감광막을 노광시키는 단계, 100℃ 내지 140℃의 온도에서 하드 베이킹을 하는 단계 및 현상하는 단계를 포함할 수 있다.

<29> 이하, 첨부된 도면을 참조하여 본 발명에 의한 발광 소자 및 이의 제조 방법에 대하여 상세히 설명하기로 한다. 그러나 본 발명은 이하에서 개시되는 실시예에 한정되는 것이 아니라 서로 다른 다양한 형태로 구현될 것이며, 단지 본 실시예는

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본 발명의 개시가 완전하도록 하며, 통상의 지식을 가진 자에게 발명의 범주를 완전하게 알려주기 위해 제공되는 것이다.

<30> 도 2는 본 발명의 발광 소자를 설명하기 위한 개념 단면도이다.

<31> 도면을 참조하면, 베이스 기판(10) 상에 순차적으로 형성된 발광층, 즉 N형 반도체층(20), 활성층(30) 및 P형 반도체층(40)을 포함하고, 금속범프(50, 55)를 이용하여 상기 발광층이 형성된 베이스 기판(10)과 플립칩 본딩되는 서브 마운트 기판(100)을 포함한다. 상기 P형 반도체층(40), 활성층(30) 및 N형 반도체층(20)을 포함하는 발광층의 측면은 수평면으로부터 20 내지 80° 의 기울기를 갖고, 이러한 측면으로부터 광의 임계각을 변화시키고 용이하게 광을 추출할 수 있어 발광 소자의 발광 효율을 개선할 수 있다.

<32> 도 3a 내지 도 3e는 본 발명에 따른 제 1 실시예의 제조 공정을 설명하기 위한 단면도들이다.

<33> 도 3a를 참조하면, 베이스 기판(10) 상에 N형 반도체층(20), 활성층(30) 및 P형 반도체층(40)을 순차적으로 형성한다.

<34> 베이스 기판(10)은 발광 소자를 제작하기 위한 통상의 웨이퍼를 지칭하는 것으로, Al_2O_3, ZnO, $LiAl_2O_3$ 등의 투명 기판을 사용한다. 본 실시예에서는 사파이어로 구성된 투명한 결정 성장 기판을 사용한다.

<35> 상기 베이스 기판(10) 상에 결정 성장시 베이스 기판(10)과 후속층들의 격자

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부정합을 줄이기 위한 버퍼층(미도시)을 더 형성할 수 있다. 버퍼층은 반도체 재료인 GaN 또는 AlN을 포함하여 형성할 수 있다.

<36> N형 반도체층(20)은 전자가 생성되는 층으로서, N형 불순물이 주입된 질화갈륨(GaN)을 사용하는 것이 바람직하고, 이에 한정되지 않고 다양한 반도체 성질의 물질층이 가능하다. 본 실시예에서는 N형 $Al_xGa_{1-x}N(0\leq x\leq 1)$을 포함하는 N형 반도체층(20)을 형성한다. 또한, P형 반도체층(40)은 정공이 생성되는 층으로서, P형 불순물이 주입된 질화갈륨(GaN)을 사용하는 것이 바람직하고, 이에 한정되지 않고 다양한 반도체 성질의 물질층이 가능하다. 본 실시예에서는 P형 $Al_xGa_{1-x}N(0\leq x\leq 1)$을 포함하는 P형 반도체층(40)을 형성한다. 뿐만 아니라 상기 반도체층으로 InGaN을 사용할 수 있다. 또한 상기의 N형 반도체층(20) 및 P형 반도체층(40)은 다층막으로 형성할 수도 있다.

<37> 활성층(30)은 소정의 밴드 갭을 가지며 양자 우물이 만들어져 전자 및 정공이 재결합되는 영역으로서, InGaN을 포함하여 이루어질 수 있다. 활성층(30)을 이루는 물질의 종류에 따라 전자 및 전공이 결합하여 발생하는 발광 파장이 변화된다. 따라서, 목표로 하는 파장에 따라 활성층(30)에 포함되는 반도체 재료를 조절하는 것이 바람직하다.

<38> 상술한 물질층들은 유기금속 화학 증착법(MOCVD; Metal Organic Chemical Vapor Deposition), 화학 증착법(CVD; Chemical Vapor Deposition), 플라즈마 화학 증착법(PCVD; Plasma-enhanced Chemical Vapor Deposition), 분자선 성장법(MBE;

Molecular Beam Epitaxy), 수소화물 기상 성장법(HVPE; Hydride Vapor Phase Epitaxy) 등을 포함한 다양한 증착 및 성장 방법을 통해 형성된다.

<39> 이후, 소정의 식각 공정을 통해 P형 반도체층(40) 및 활성층(30)의 일부를 제거하여 N형 반도체층(20)의 일부를 노출시킨다. P형 반도체층(40) 상에 식각 마스크 패턴을 형성한 다음, 건식 또는 습식 식각 공정을 실시하여 P형 반도체층(40) 및 활성층(30)을 제거하여 N형 반도체층(20)을 노출시킨다.

<40> 일반적으로 상기 식각 공정을 위하여 P형 반도체층(40) 상면에 1 내지 2㎛ 두께로 감광막(photoresist)을 도포한 후, 80 내지 90℃의 온도에서 소프트 베이킹(soft baking)을 한다. 다음으로, 소정의 포토 마스크(photo mask)를 통해 자외선(UV) 영역의 빛을 조사하여 마스크 상에 형성된 패턴을 도포된 감광막에 전사하는 노광(exposure) 공정을 진행한다. 이후, 100 내지 120℃의 온도에서 하드 베이킹(hard baking)을 하고, 노광 공정을 통해 상대적으로 결합이 약해져 있는 부분의 감광막을 용제를 사용하여 녹여내는 현상(developing) 공정을 진행한다. 이러한 과정을 통해 상기 P형 반도체층(40) 상에 소정의 식각 마스크 패턴이 형성된다.

<41> 그러나 본 실시예는 상기 식각 마스크 패턴을 형성할 때, 3 내지 50㎛ 두께로 감광막을 종래에 비해 두껍게 도포하고 소프트 베이킹을 거쳐 노광 공정을 실시한다. 그 다음에 하드 베이킹을 통하지 않고 바로 현상하면, 남아있는 감광막의 현상된 측면은 수평면으로부터 80° 정도의 기울기를 갖는 경사진 면을 형성하게 된다. 이어서, 이러한 측면의 기울기를 갖는 식각 마스크 패턴을 사용하여 노출된 영역의 P형 반도체층(40) 및 활성층(30)을 식각하면, 식각된 P형 반도체층(40) 및 활

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성층(30)의 측면은 마찬가지로 수평면으로부터 80° 정도의 기울기를 갖는 경사진 면을 얻을 수 있다.

<42> 즉, 도 3a의 P형 반도체층(40) 상에 3 내지 50㎛ 두께로 감광막을 두껍게 도포하여 노광 후 하드 베이킹 없이 바로 현상한 식각 마스크 패턴을 형성한다. 상기 식각 마스크 패턴에 의해 노출된 P형 반도체층(40) 및 활성층(30)을 유도 결합 플라즈마(ICP; Inductive Coupled Plasma) 또는 건식 식각 공정을 통해 제거하여 N형 반도체층(20)을 노출시킨다. 노출된 N형 반도체층(20)의 일부를 더 제거할 수도 있다. 이후, 식각 마스크 패턴을 제거하면, 도 3b에 도시한 바와 같이 P형 반도체층(40), 활성층(30)의 측면이 수평면으로부터 수직(90°)이 아닌, 소정의 기울기를 갖는 발광 소자를 제조할 수 있다.

<43> 또한, 도 3a의 P형 반도체층(40) 상에 3 내지 50㎛ 두께로 감광막을 두껍게 도포하여 노광 후 하드 베이킹을 실시하는 경우에, 하드 베이킹 온도를 100℃ 내지 140℃로 하여 진행하고 현상을 하게 되면, 현상된 감광막의 측면이 수평면으로부터 80° 에서 20° 까지의 기울기를 갖도록 식각된 측면을 얻을 수 있다. 예를 들어, 100℃의 온도에서 하드 베이킹을 하는 경우에 수평면으로부터 80° 정도의 기울기를 갖는 식각 마스크 패턴을 얻을 수 있으며, 이를 이용하여 P형 반도체층(40) 및 활성층(30)의 측면이 수평면으로부터 80° 정도의 기울기를 갖도록 할 수 있다. 또한, 140℃의 온도에서 하드 베이킹을 하는 경우에 수평면으로부터 20° 정도의 기울기를 갖는 식각 마스크 패턴을 얻을 수 있으며, 이를 이용하여 P형 반도체층(40) 및 활성층(30)의 측면이 수평면으로부터 20° 정도의 기울기를 갖도록 할 수 있다.

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<44> 이와 같이 3 내지 50㎛ 두께의 감광막을 노광 후 100℃ 내지 140℃의 온도에서 하드 베이킹을 하고 현상한 식각 마스크 패턴을 사용함으로써, P형 반도체층(40) 및 활성층(30)의 측면이 마찬가지로 수평면으로부터 80° 에서 20° 까지의 기울기를 갖도록 식각된 측면을 얻을 수 있다. 그리하여 발광층의 내부에서 생성된 광은 다양한 기울기를 갖도록 식각된 측면에 전반사되지 않고 발광 소자의 외부로 빠져나가게 된다.

<45> 상기 P형 반도체층(40) 상부에 광의 반사를 위한 반사층을 더 형성할 수 있으며, P형 반도체층(40) 또는 노출된 N형 반도체층(20) 상부에 전류의 공급을 원활히 하기 위한 별도의 오믹금속층을 더 형성할 수도 있다. 상기 오믹금속층으로는 Cr, Au를 사용할 수 있다.

<46> 또한, 도 3c에 도시한 바와 같이 P형 반도체층(40) 상에 P형 금속범프(55, metal bumper)와, N형 반도체층(20) 상에 N형 금속범프(50)를 범핑용으로 형성한다. P형 및 N형 금속범프(55, 50)로는 Pb, Sn, Au, Ge, Cu, Bi, Cd, Zn, Ag, Ni 및 Ti 중 적어도 어느 하나를 사용할 수 있고, 이들의 합금을 사용할 수 있다. 이를 위해, 전체 구조 상에 감광막을 도포한 다음, 소정의 마스크를 이용한 사진식각 공정을 실시하여 P형 반도체층(40)과 N형 반도체층(20)의 일부를 노출시킨 감광막 패턴(미도시)을 형성한다. 전체 구조상에 금속막을 증착한 다음, 상기 감광막 패턴에 의해 노출된 P형 반도체층(40) 상부에 형성된 금속막과, N형 반도체층(30)의 상부에 형성된 금속막을 제외한 나머지 영역의 금속막 및 상기 감광막 패턴을 제거한다. 이로써, P형 반도체층(40) 상에는 P형 금속범프(55)가 형성되고, N형 반

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도체층(20) 상에는 N형 금속범프(50)가 형성된다.

<47> 다음으로, 도 3d를 참조하면 별도의 서브 마운트 기판(100)을 마련하여 상기 P형 금속범프(55) 및 N형 금속범프(50)와 각각 접속될 P형 본딩패드(115) 및 N형 본딩패드(110)를 형성한다.

<48> 이 때 서브 마운트 기판(100)으로는 열전도성이 우수한 다양한 기판(100)을 사용한다. 즉, SiC, Si, Ge, SiGe, AlN, 금속 등을 사용한다. 본 실시예는 열전도성이 우수하며 절연 성질을 갖는 AlN을 사용한다. 물론 이에 한정되지 않고, 열전도율이 크며 전기 전도성이 우수한 물질인 금속성 물질을 사용할 수 있다. 이 경우에는 기판(100) 상에 절연막 또는 유전체막을 형성하여 충분한 절연 역할을 하도록 한다. 유전체막으로 SiO_2, MgO 및 SiN 또는 절연성 물질을 사용할 수 있다. 또한, 상기 N형 본딩 패드(110) 및 P형 본딩 패드(115)는 전기 전도성이 우수한 금속을 사용한다. 이는 스크린 인쇄 방법으로 형성하거나, 소정의 마스크 패턴을 이용한 증착 공정을 통해 형성한다.

<49> 이후, 상기 서브 마운트 기판(100)과, 상기 발광층이 형성된 베이스 기판(10)을 플립칩 본딩한다.

<50> 도 3e를 참조하면, 본 발명의 발광 소자는 발광층의 상부에 형성된 N형 및 P형 금속범프(50, 55)와 서브 마운트 기판(100)의 N형 및 P형 본딩패드(110, 115)가 접속되도록 본딩된다.

<51> 이 때, 열 또는 초음파(ultrasonic)를 이용하거나, 열과 초음파를 동시에 사

용하여 본딩할 수 있다. 금속범프(50, 55)와 하부 본딩 패드(110, 115)와의 접속은 다양한 본딩 방법을 통해 본딩된다.

<52> 이뿐 아니라, 발광층의 상부에 N형 및 P형 금속범프(50, 55)가 형성되지 않고, 서브 마운트 기판(100) 상에 각각의 금속범프가 형성될 수도 있다.

<53> 도면에서 볼 수 있듯이, 다수 개의 발광 소자를 하나의 기판(20) 상에 제작할 수 있고, 이러한 경우 추후에 각각의 발광 소자로 절단하여 사용하게 된다. 이때, 도 3e의 (A) 부분은 이러한 다수 개의 발광 소자를 개별적으로 절단하기 위한 절단부이다.

<54> 이로써 P형 반도체층(40), 활성층(30), N형 반도체층(20) 측면의 일부가 수평면으로부터 수직이 아닌, 소정의 기울기를 갖는 플립칩 구조의 발광 소자를 제조할 수 있다.

<55> 상술한 본 발명의 발광 소자의 제조 공정은 일 실시예일뿐 이에 한정되지 않고, 다양한 공정과 제조 방법이 소자의 특성 및 공정의 편의에 따라 변경되거나 추가될 수 있다.

<56> 예를 들어, 상기와 동일한 공정에 있어서 도 3a와 같이 N형 반도체층, 활성층, P형 반도체층이 순차적으로 형성된 베이스 기판을 마련하고, 먼저 기판이 노출되도록 상기 P형 반도체층, 활성층, N형 반도체층의 일부를 제거하여 다수 개의 발광 소자를 개별 분리할 수 있다. 이 때 상술한 공정을 통하여 식각되는 P형 반도체층, 활성층, N형 반도체층 측면을 수평면으로부터 수직이 아닌, 소정의 기울기를 갖도록 형성할 수도 있다.

<57> 상술한 바와 같이 본 발명은 플립칩 구조의 발광 소자에 있어서, 발광층의 일부 측면이 수평면으로부터 수직이 아닌, 소정의 기울기를 갖도록 형성함으로써, 종래의 발광 소자에 비하여 발광 효율을 향상시킬 수 있다. 이는 종래의 평탄한 표면에서 반사되었던 광자가 다양한 각의 표면에 의해 반사되지 않고 외부로 빠져나가기 때문이다.

<58> 도 4a 내지 도 4d는 본 발명에 따른 제 2 실시예의 제조 공정을 설명하기 위한 단면도들이다.

<59> 이는 제 1 실시예의 경우와 거의 동일하며, 단지 제 2 실시예는 웨이퍼 레벨에서 다수의 발광 셀을 직렬, 병렬 또는 직병렬 연결하여 소자의 크기를 줄이고, 적정 전압 및 전류에 구동되도록 하여 조명용으로 사용가능하며 교류 전원에서도 구동할 수 있는 발광 소자를 제공한다. 상기 제 1 실시예의 경우와 중복되는 설명은 생략한다.

<60> 도 4a를 참조하면, 유기금속 화학 증착법, 화학 증착법, 플라즈마 화학 증착법, 분자선 성장법, 수소화물 기상 성장법 등의 다양한 증착 방법을 통해 베이스 기판(10) 상에 N형 반도체층(20), 활성층(30) 및 P형 반도체층(40)을 순차적으로 형성한다. 상기 베이스 기판(10) 상에 결정 성장시 기판(10)과 후속층들의 격자 부정합을 줄이기 위한 버퍼층을 더 형성할 수 있다.

<61> 이후, 상기 베이스 기판(10) 상에 순차적으로 형성된 N형 반도체층(20), 활성층(30) 및 P형 반도체층(40)의 일부를 제거하여 다수개의 발광 셀을 형성한다. 이를 위해, P형 반도체층(40) 상에 3 내지 50㎛ 두께로 감광막을 두껍게 도포하여

노광 후 하드 베이킹 없이 바로 현상하여 식각 마스크 패턴을 형성한다. 상기 식각 마스크 패턴에 의해 노출된 P형 반도체층(40), 활성층(30), 소정의 N형 반도체층(20)을 유도 결합 플라즈마 또는 건식 식각 공정을 통해 제거하여 발광 셀을 분리한다. 다음으로 식각 마스크 패턴을 제거하면, 도 4b에 도시한 바와 같이 식각된 P형 반도체층(40), 활성층(30), N형 반도체층(20)의 전측면이 수평면으로부터 80° 정도의 기울기를 갖는 경사진 면을 얻을 수 있다.

<62> 또한 P형 반도체층(40) 상에 3 내지 50㎛ 두께로 감광막을 두껍게 도포하여 노광 후 100℃ 내지 140℃의 온도에서 하드 베이킹을 하고 현상하여 식각 마스크 패턴을 형성한다. 이러한 식각 마스크 패턴에 의해 노출된 P형 반도체층(40), 활성층(30), N형 반도체층(20)을 식각한 후 식각 마스크 패턴을 제거하여 식각된 P형 반도체층(40) 및 활성층(30)의 측면이 80° 에서 20° 까지의 다양한 기울기를 갖도록 할 수도 있다.

<63> 다음으로, 도 4c에 도시한 바와 같이 소정의 식각 공정을 통해 P형 반도체층(40) 및 활성층(30)의 일부를 제거하여 N형 반도체층(20)의 일부를 노출시킨다. 소정의 브리지 배선을 통해 일 발광 셀의 노출된 N형 반도체층(20)과 인접한 타 발광 셀의 P형 반도체층(40)을 연결한다. 이 때 브리지 배선(60)은 도전성의 물질을 이용하되, 금속을 이용하여 형성한다. 물론, 불순물로 도핑된 실리콘 화합물을 이용할 수도 있다. 상기 브리지 배선(60)은 브리지(Bridge) 공정 또는 스텝 커버(Step Cover) 등의 공정을 통해 형성된다.

<64> 상술한 브리지 공정은 에어브리지 공정이라고도 하며, 서로 연결할 칩 간에

포토 공정을 이용해 감광액을 도포하고 현상하여 감광막 패턴을 형성하고, 그 위에 금속 등의 물질을 진공 증착 등의 방법으로 먼저 박막으로 형성하고, 다시 그 위에 전기 도금(electroplating), 무전해 도금(electroplating) 또는 금속 증착 등의 방법으로 금을 포함하는 도전성 물질을 일정 두께로 도포한다. 이후, 솔벤트등의 용액으로 감광막 패턴을 제거하면 도전성 물질의 하부는 다 제거되고 브리지 형태의 도전성 물질만이 공간에 형성된다.

<65> 스탭 커버(Step Cover) 공정은 서로 연결할 칩 간에 포토 공정을 이용해 감광액을 도포하고, 현상하여 서로 연결될 부분만을 남기고 다른 부분은 감광막 패턴으로 뒤덮고, 그 위에 전기 도금, 무전해 도금 또는 금속 증착 등의 방법으로 금을 포함하는 도전성 물질을 일정 두께로 도포한다. 이어서, 솔벤트 등의 용액으로 감광막 패턴을 제거하면 도전성 물질이 덮인 이외의 부분은 다 제거되고 도전성 물질이 덮혀진 부분 만이 남아 연결할 칩 사이를 전기적으로 연결시키는 역할을 하게 되다.

<66> 또한 각 발광 셀의 상부에 범핑용으로 형성된 다수개의 금속범프를 형성하고, 일 가장자리에 위치한 발광 셀의 P형 반도체층(40)과 다른 일 가장자리에 위치한 발광 셀의 N형 반도체층(20) 상에 각각 P형 금속범프(55) 및 N형 금속범프(50)를 더 형성한다. 금속범프로는 Pb, Sn, Au, Ge, Cu, Bi, Cd, Zn, Ag, Ni 및 Ti 중 한가지 또는 이들 물질의 합금을 적용한다.

<67> 다음으로, 도 4d에 도시한 바와 같이 별도의 서브 마운트 기판(100)을 마련하여, 기판(100) 상부에 다수개의 본딩층(110)과, 서브 마운트 기판(100)의 일 가

장자리에 위치한 P형 본딩 패드(115)와, 다른 일 가장자리에 위치한 N형 본딩 패드(110)를 형성한다.

<68> 이후, 도 4e에서 볼 수 있듯이 앞서 설명한 다수개의 발광 셀이 형성된 베이스 기판(10)과, 서브 마운트 기판(100)을 플립칩 본딩하여 발광 소자를 제작한다. 상기 발광 셀의 상부에 형성된 금속범프(50, 55)와 상기 서브 마운트 기판(100)에 형성된 본딩층(110)을 통해 본딩한다. 서브 마운트 기판(100)의 일 가장자리에 위치한 P형 본딩 패드(115)는 일 가장자리에 위치한 발광 셀의 P형 금속범프(55)에 접속되고, 타 가장자리에 위치한 N형 본딩 패드(110)는 다른 가장자리에 위치한 발광 셀의 N형 반도체층(50)에 접속된다.

<69> 상술한 본 발명의 발광 소자의 제조 방법은 이에 한정되지 않고, 다양한 공정과 제조 방법이 소자의 특성 및 공정의 편의에 따라 변경되거나 추가될 수 있다.

<70> 예를 들어 본 실시예는 브리지 공정 또는 스탭 커버 등의 공정을 통해 각기 인접한 발광 셀의 N형 반도체층과 P형 반도체층을 전기적으로 연결하는 브리지 배선을 형성한 후, 서브 마운트 기판과 플립칩 본딩한다. 그러나 이에 한정되지 않고, 다수개의 발광 셀과 서브 마운트 기판의 플립칩 본딩시 서브 마운트 기판에 전극층을 형성하여 금속범프를 통해 인접한 발광 셀의 N형 반도체층과 P형 반도체층이 전기적으로 연결되도록 할 수도 있다.

<71> 이로써 발광층의 측면이 수평면으로부터 수직이 아닌, 소정의 기울기를 갖는 다수의 플립칩 형태의 발광 셀이 서브 마운트 기판 상에 어레이된 발광 소자를 제조할 수 있다. 상기 발광 셀들은 원하는 목적에 따라 직렬, 병렬 또는 직병렬로 다

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양하게 연결될 수 있다.

<72> 도 5는 본 발명에 따른 제 3 실시예를 도시한 단면도이다.

<73> 이는 제 2 실시예의 경우와 거의 동일하며, 단지 제 3 실시예는 도 4b에 도시한 바와 마찬가지로 측면이 다양한 기울기를 갖도록 식각하여 다수개의 발광 셀을 분리한 다음, N형 반도체층을 노출시키기 위해 식각하는 경우에도 마찬가지의 식각 공정을 사용하여 발광 소자를 제조할 수 있다. 즉, 도 5에 도시한 바와 같이 N형 반도체층(20)이 노출되도록 식각되는 P형 반도체층(40)과 활성층(30)의 측면이 다양한 기울기를 갖도록 형성할 수 있다. 이러한 발광 소자는 종래 수직으로 식각된 표면에서 반사되었던 광자가 다양한 각의 표면에 의해 반사되지 않고 외부로 빠져나가기 때문에 더욱 향상된 발광 효율을 얻을 수 있다.

<74> 이로써 발광층의 전측면이 수평면으로부터 수직이 아닌, 소정의 기울기를 갖는 다수의 플립칩 형태의 발광 셀이 서브 마운트 기판 상에 어레이된 발광 소자를 제조할 수 있다. 상기 발광 셀들은 원하는 목적에 따라 직렬, 병렬 또는 직병렬로 다양하게 연결될 수 있다.

<75> 발광 소자의 광효율은 내부 양자 효율과 외부 양자 효율로 나타낼 수 있는데, 내부 양자 효율은 활성층의 설계나 품질에 따라서 결정된다. 외부 양자 효율의 경우 발광층에서 생성되는 광자가 발광 소자의 외부로 나오는 정도에 따라서 결정된다. 종래에는 반도체층의 측면이 수평면으로부터 수직으로 형성되어, 일부의 광자가 반도체층의 측면에서 투과하지 못하고 반사되어 나오며, 전반사된 광은 외부로 투과하지 못하고 발광 소자 내부에서 소멸된다. 그러나, 본 발명에 따르면 반

도체층의 측면을 수평면으로부터 수직이 아닌, 소정의 기울기를 갖는 경우에, 경사진 측면이 광의 임계각을 변화시켜 보다 용이하게 광을 추출할 수 있게 돕는다. 따라서 발광층에서 발생한 광이 전반사되지 않고 발광 소자의 외부로 방출될 확률이 높아져 외부 양자 효율이 현저하게 향상된다.

【발명의 효과】

<76> 본 발명에 의한 복수 셀의 단일 발광 소자 및 이의 제조 방법은 발광층에서 생성되는 광이 소정의 기울기를 갖는 경사면에 대해 전반사되지 않고 외부로 방출되어 광추출 효율이 향상된다. 또한 본 발명은 플립칩 구조를 이용하여 열 방출 효율이 높고, 광의 차폐가 거의 없어 광효율이 증가한다.

<77> 본 발명에 의한 복수 셀의 단일 발광 소자 및 이의 제조 방법은 발광 소자의 발광 효율, 외부 양자 효율 등의 특성을 향상시키고 신뢰성을 확보하여, 고광도, 고휘도의 광을 발광할 수 있는 장점이 있다.

【특허청구범위】

【청구항 1】

N형 반도체층과 상기 N형 반도체층 상에 형성된 P형 반도체층을 포함하는 다수개의 발광 셀이 형성된 기판; 및

상기 기판이 플립칩 본딩되는 서브 마운트 기판을 포함하고,

상기 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층이 연결되고, 상기 발광 셀의 적어도 P형 반도체층을 포함하는 측면이 수평면으로부터 수직이 아닌 소정의 기울기를 갖는 것을 특징으로 하는 복수 셀의 단일 발광 소자.

【청구항 2】

청구항 1에 있어서,

상기 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층을 연결하기 위한 배선을 더 포함하는 것을 특징으로 하는 복수 셀의 단일 발광 소자.

【청구항 3】

청구항 1 또는 청구항 2에 있어서,

상기 소정의 기울기는 20 내지 80° 인 것을 특징으로 하는 복수 셀의 단일 발광 소자.

【청구항 4】

기판 상에 N형 반도체층과 P형 반도체층을 순차적으로 형성하여 상기 기판 상에 발광 셀을 형성하는 단계;

상기 P형 반도체층 상에 측면이 수평면으로부터 수직이 아닌 소정의 기울기를 갖는 식각 마스크 패턴을 형성하는 단계;

상기 식각 마스크 패턴에 의해 노출된 P형 반도체층과 상기 식각 마스크 패턴을 제거하는 단계; 및

상기 기판을 별도의 서브 마운트 기판에 플립칩 본딩하는 단계를 포함하는 발광 소자의 제조 방법.

【청구항 5】

청구항 4에 있어서,

상기 기판 상에 발광 셀을 형성하는 단계는 상기 N형 반도체층 및 P형 반도체층의 일부를 제거하여 다수개의 발광 셀을 형성하는 단계를 포함하고,

상기 P형 반도체층과 상기 식각 마스크 패턴을 제거하는 단계 이후에,

브리지 배선을 통해 일 발광 셀의 N형 반도체층과 그에 인접한 다른 일 발광 셀의 P형 반도체층을 연결하는 단계를 더 포함하는 것을 특징으로 하는 발광 소자의 제조 방법.

【청구항 6】

청구항 5에 있어서,

상기 다수개의 발광 셀을 형성하는 단계는,

상기 P형 반도체층 상에 측면이 수평면으로부터 수직이 아닌 소정의 기울기를 갖는 식각 마스크 패턴을 형성하는 단계;

상기 식각 마스크 패턴에 의해 노출된 P형 반도체층 및 N형 반도체층을 제거하여 다수개의 발광 셀을 형성하는 단계; 및

상기 식각 마스크 패턴을 제거하는 단계를 포함하는 것을 특징으로 하는 발광 소자의 제조 방법.

【청구항 7】

청구항 5에 있어서,

상기 브리지 배선은 브리지(Bridge) 공정 또는 스탭 커버(Step Cover) 공정을 통해 일 발광 셀의 N형 반도체층과 인접한 다른 일 발광 셀의 P형 반도체층을 연결하는 것을 특징으로 하는 발광 소자의 제조 방법.

【청구항 8】

청구항 4 내지 청구항 7 중 어느 한 항에 있어서,

상기 식각 마스크 패턴을 형성하는 단계는,

3 내지 50㎛ 두께의 감광막을 이용하는 것을 특징으로 하는 발광 소자의 제조 방법.

【청구항 9】

청구항 8에 있어서,

상기 P형 반도체층 상에 상기 감광막을 도포하는 단계;

소정의 마스크 패턴에 따라 상기 감광막을 노광시키는 단계; 및

상기 노광 후 베이킹 공정 없이 현상하는 단계를 포함하는 것을 특징으로 하는 발광 소자의 제조 방법.

【청구항 10】

청구항 8에 있어서,

상기 식각 마스크 패턴을 형성하는 단계는,

상기 P형 반도체층 상에 상기 감광막을 도포하는 단계;

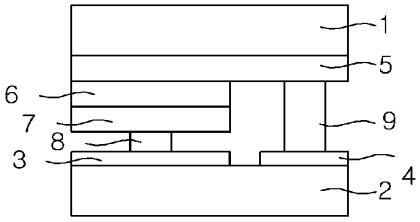
소정의 마스크 패턴에 따라 상기 감광막을 노광시키는 단계;

100℃ 내지 140℃의 온도에서 하드 베이킹을 하는 단계; 및

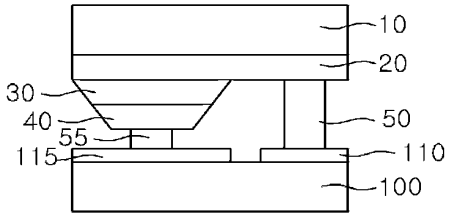
현상하는 단계를 포함하는 것을 특징으로 하는 발광 소자의 제조 방법.

【도면】

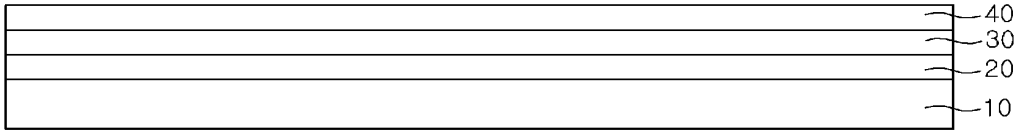
【도 1】



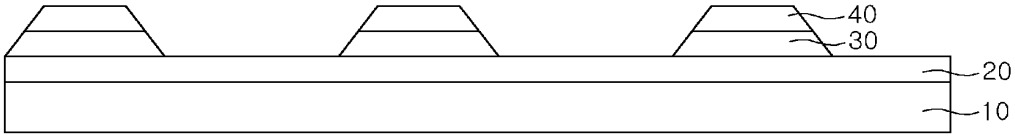
【도 2】



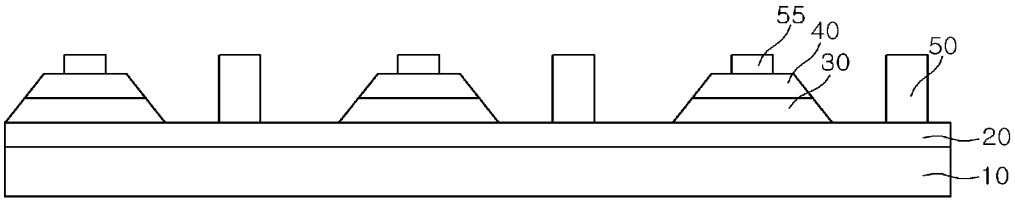
【도 3a】



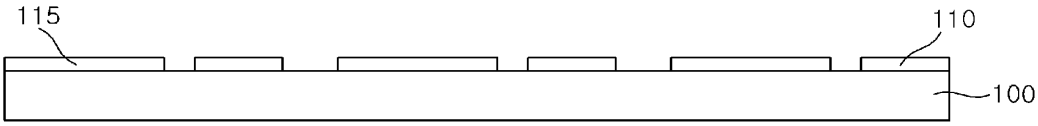
【도 3b】



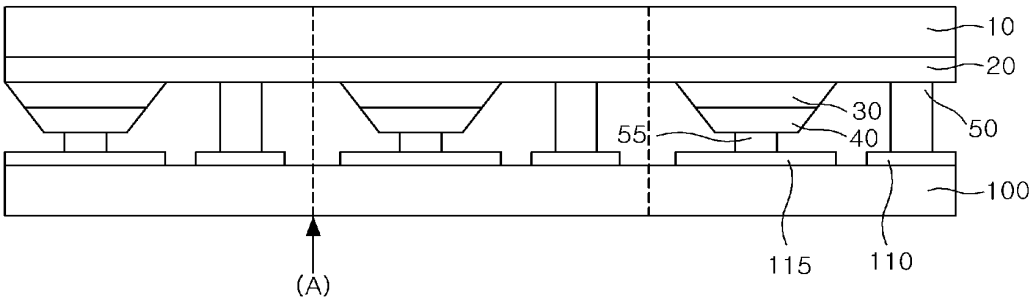
【도 3c】



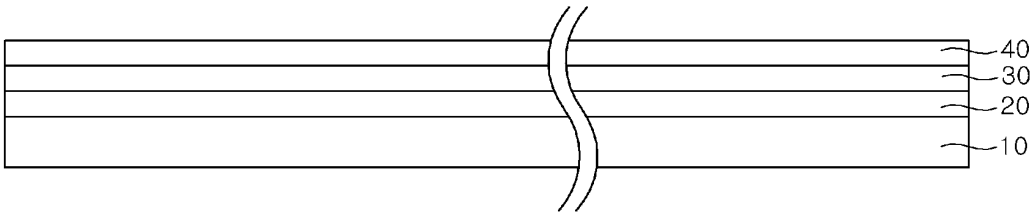
【도 3d】



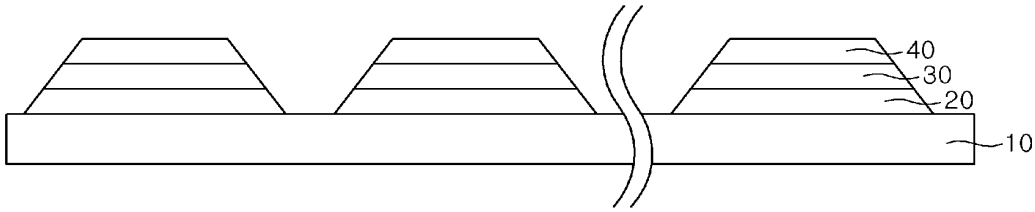
【도 3e】



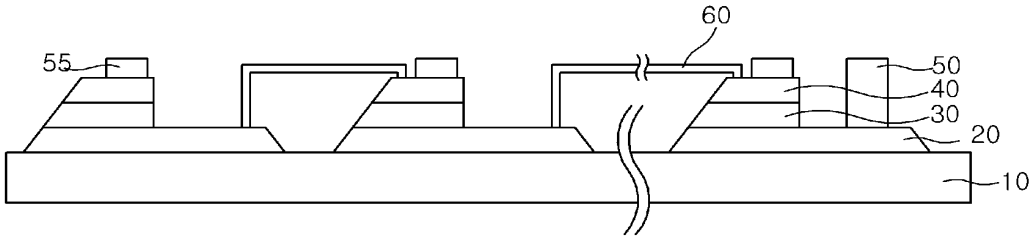
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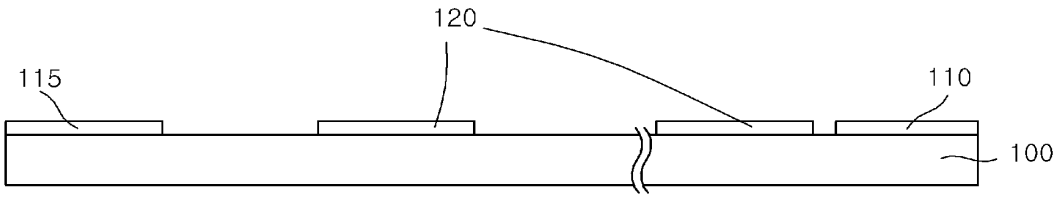
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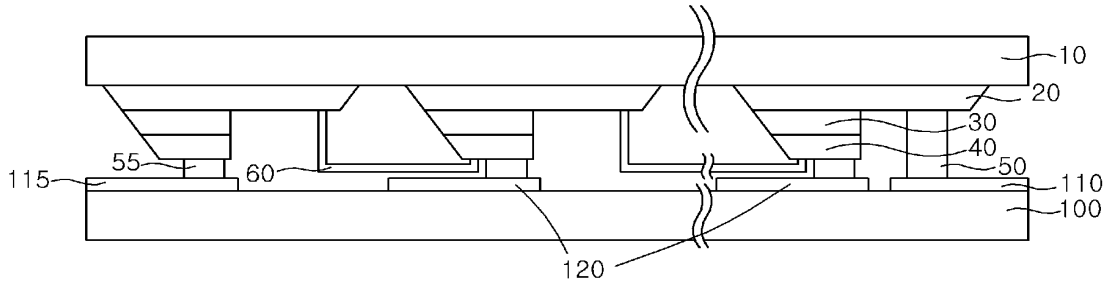
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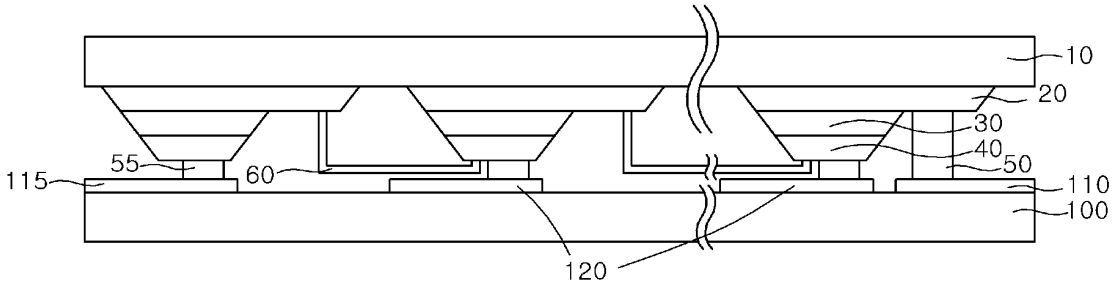
【도 4d】


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115
110
100

【도 4e】


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【도 5】


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2006 년 07 월 10 일

특 허 청
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【서지사항】

【서류명】 특허출원서

【권리구분】 특허

【수신처】 특허청장

【참조번호】 0072

【제출일자】 2006.03.08

【발명의 국문명칭】 배선들을 갖는 교류용 발광 다이오드 및 그것을 제조하는 방법

【발명의 영문명칭】 LIGHT EMITTING DIODE FOR AC OPERATION WITH WIRES AND METHOD OF FABRICATING THE SAME

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【심사청구】 청구

【취지】 특허법 제42조의 규정에 의한 출원, 특허법 제60조의 규정에 의한 출원심사를 청구합니다.

대리인 이수완 (인)

대리인 조진태 (인)

대리인 윤종섭 (인)

대리인 이성규 (인)

【수수료】

【기본출원료】	0 면	38,000 원
【가산출원료】	25 면	0 원
【우선권주장료】	0 건	0 원
【심사청구료】	13 항	525,000 원
【합계】	563,000 원	
【감면사유】	중기업	
【감면후 수수료】	281,500 원	

【첨부서류】 1.중소기업기본법시행령 제2조에의한 중소기업에 해당함을 증명하는 서류[사업자등록증/원천징수이행상황신고서]_1통

【요약서】

【요약】

배선들을 갖는 교류용 발광 다이오드 및 그것을 제조하는 방법이 개시된다. 이 발광 다이오드는 기판 상에 서로 이격되어 위치하는 발광셀들을 포함한다. 이 발광셀들은 각각 하부 반도체층, 하부 반도체층의 일 영역 상부에 위치하는 상부 반도체층 및 하부 반도체층과 상부 반도체층 사이에 개재된 활성층을 포함한다. 또한, 발광셀들은 그 측벽들이 기판의 상부면에 대해 경사지게 형성되어 위로 갈수록 폭이 좁아진다. 한편, 절연층이 발광셀들의 전면을 덮는다. 절연층은 하부 반도체층들의 다른 영역들 및 상부 반도체층들 상에 각각 형성된 개구부들을 갖는다. 배선들이 절연층 상에 형성되어 개구부들을 통해 하부 반도체층들 및 상부 반도체층들에 전기적으로 연결된다. 배선들은 인접한 발광셀들의 하부 반도체층들과 상부 반도체층들을 각각 전기적으로 연결한다. 따라서, 배선들이 절연층 상에 형성되므로, 배선들의 단선 및 단락을 방지할 수 있어 신뢰성 있는 교류용 발광 다이오드를 제공할 수 있다.

【대표도】

도 3

【색인어】

발광 다이오드, 교류 동작, 배선, 반도체층, 절연층, 포토레지스트

【명세서】

【발명의 명칭】

배선들을 갖는 교류용 발광 다이오드 및 그것을 제조하는 방법{LIGHT EMITTING DIODE FOR AC OPERATION WITH WIRES AND METHOD OF FABRICATING THE SAME}

【도면의 간단한 설명】

<1> 도 1은 종래의 교류용 발광 다이오드를 설명하기 위한 평면도이다.

<2> 도 2는 도 1의 절취선 IV-IV를 따라 취해진 단면도이다.

<3> 도 3은 본 발명의 일 실시예에 따른 교류용 발광 다이오드를 설명하기 위한 단면도이다.

<4> 도 4 내지 도 9는 본 발명의 일 실시예에 따른 교류용 발광 다이오드를 제조하는 방법을 설명하기 위한 단면도들이다.

【발명의 상세한 설명】

【발명의 목적】

【발명이 속하는 기술분야 및 그 분야의 종래기술】

<5> 본 발명은 교류용 발광 다이오드 및 그것을 제조하는 방법에 관한 것으로, 더욱 상세하게는 배선들의 단선 및/또는 배선들에 의한 단락을 방지할 수 있는 교류용 발광 다이오드 및 그것을 제조하는 방법에 관한 것이다.

<6> 질화갈륨(GaN) 계열의 발광 다이오드가 약 10년 동안 적용되고 개발되어 왔

다. GaN 계열의 LED는 LED 기술을 상당히 변화시켰으며, 현재 천연색 LED 표시소자, LED 교통 신호기, 백색 LED 등 다양한 응용에 사용되고 있다. 최근, 고효율 백색 LED는 형광 램프를 대체할 것으로 기대되고 있으며, 특히 백색 LED의 효율(efficiency)은 통상의 형광램프의 효율에 유사한 수준에 도달하고 있다.

<7> 일반적으로, 발광 다이오드는 순방향 전류에 의해 광을 방출하며, 직류전류의 공급을 필요로 한다. 따라서, 발광 다이오드는, 교류전원에 직접 연결하여 사용할 경우, 전류의 방향에 따라 온/오프를 반복하며, 그 결과 연속적으로 빛을 방출하지 못하고, 역방향 전류에 의해 쉽게 파손되는 문제점이 있다.

<8> 이러한 발광 다이오드의 문제점을 해결하여, 고전압 교류전원에 직접 연결하여 사용할 수 있는 발광 다이오드가 국제공개번호 WO 2004/023568(A1)호에 "발광성분들을 갖는 발광소자"(LIGHT-EMITTING DEVICE HAVING LIGHT-EMITTING ELEMENTS)라는 제목으로 사카이 등(SAKAI et. al.)에 의해 개시된 바 있다.

<9> 도 1은 상기 WO 2004/023568(A1)호에 따른 교류용 발광 다이오드를 설명하기 위한 부분적인 평면도이고, 도 2는 도 1의 절취선 IV-IV를 따라 취해진 단면도이다.

<10> 도 1 및 도 2를 참조하면, 기판(10) 상에 복수개의 발광셀들(1)이 형성된다. 또한, 발광셀들(1) 상에 p-전극(22) 및 n-전극(24)이 형성된다. 에어브리지 배선(28)이 인접한 발광셀들의 p-전극(22)과 n-전극(24)을 전기적으로 연결하여, 복수개의 발광셀들(1)을 직렬 연결한다.

<11> 각 발광셀은 n-GaN층(14), p-GaN층(20)을 포함한다. 도시하지는 않았지만,

n-GaN층(14)과 p-GaN층(20) 사이에 InGaN 활성층이 개재될 수 있다. p-전극(22)은 상기 p-GaN층(20) 상에 형성되고, n-전극(24)은 상기 n-GaN층(14) 상에 형성된다. 한편, 에어브리지 배선(28)은 n-전극(24)과 p-전극(22)을 전기적으로 연결한다.

<12> 상기 WO 2004/023568(A1)호에 따르면, LED들(발광셀들)이 사파이어 기판과 같은 절연성 기판 상에 2차원적으로 직렬연결되어 LED 어레이를 형성한다. 이러한 두개의 LED 어레이들이 상기 사파이어 기판 상에서 역병렬로 연결된다. 그 결과, AC 파워 서플라이에 의해 구동될 수 있는 단일칩 발광소자가 제공된다.

<13> 그러나, 도 2에 도시한 바와 같이, p-전극(22)과 n-전극(24)을 연결하는 배선(28)은 에어브리지 배선으로, 접촉부들 이외 부분은 공중에 떠 있게 된다. 이러한 에어브리지 배선(28)은 외압에 의해 단선되기 쉬우며, 또한 외압에 의한 변형에 의해 단락을 유발하기 쉽다.

【발명이 이루고자 하는 기술적 과제】

<14> 본 발명이 이루고자 하는 기술적 과제는, 외압에 의해 배선들이 단선 또는 단락되는 것을 방지할 수 있는 교류용 발광 다이오드를 제공하는 데 있다.

<15> 본 발명이 이루고자 하는 다른 기술적 과제는, 배선들을 형성한 후에 잔존하는 금속물질이 발광셀들을 단락시키는 것을 방지할 수 있는 교류용 발광 다이오드를 제공하는 데 있다.

<16> 본 발명이 이루고자 하는 또 다른 기술적 과제는 배선들의 단선 및/또는 단락을 방지할 수 있는 교류용 발광 다이오드를 제조하는 방법을 제공하는 데 있다.

【발명의 구성】

<17> 상기 기술적 과제들을 이루기 위하여, 본 발명의 일 태양은 안정한(robust) 배선들을 갖는 교류용 발광 다이오드를 제공한다. 이 발광 다이오드는 기판 상에 서로 이격되어 위치하는 발광셀들을 포함한다. 상기 발광셀들은 각각 하부 반도체층, 상기 하부 반도체층의 일 영역 상부에 위치하는 상부 반도체층 및 상기 하부 반도체층과 상기 상부 반도체층 사이에 개재된 활성층을 포함한다. 또한, 상기 발광셀들은 그 측벽들이 상기 기판의 상부면에 대해 경사지게 형성되어 위로 갈수록 폭이 좁아진다. 절연층이 상기 발광셀들의 전면을 덮는다. 상기 절연층은 상기 하부 반도체층들의 다른 영역들 및 상기 상부 반도체층들 상에 각각 형성된 개구부들을 갖는다. 배선들이 상기 절연층 상에 형성되어 상기 개구부들을 통해 상기 하부 반도체층들 및 상기 상부 반도체층들에 전기적으로 연결된다. 상기 배선들은 인접한 발광셀들의 상기 하부 반도체층들과 상기 상부 반도체층들을 각각 전기적으로 연결한다. 상기 배선들이 절연층 상에 형성되므로, 배선들의 단선 및 배선들에 의한 단락을 방지할 수 있어 신뢰성 있는 교류용 발광 다이오드를 제공할 수 있다.

<18> 상기 발광셀들 각각의 하부 반도체층의 측벽들이 상기 기판의 상부면과 이루는 경사각이 15도 내지 80도의 범위 내일 수 있다. 이에 따라, 금속층을 증착한 후 패터닝하여 상기 배선들을 형성할 수 있어 안정한 배선들을 쉽게 형성할 수 있다.

<19> 전극패드들이 상기 하부 반도체층들의 다른 영역들과 상기 절연층 사이에 개재될 수 있다. 상기 전극패드들은 상기 하부 반도체층들의 다른 영역들 상에 형성된 개구부들에 의해 노출된다. 이에 따라, 상기 배선들은 상기 전극패드들에 접촉

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되어 상기 하부 반도체층에 전기적으로 연결된다.

<20> 또한 투명전극층들이 상기 상부 반도체층들과 상기 절연층 사이에 개재될 수 있다. 상기 투명전극층들은 상기 상부 반도체층들 상에 형성된 개구부들에 의해 노출된다. 이에 따라, 상기 배선들은 상기 투명전극층들에 접촉되어 상기 상부 반도체층에 전기적으로 연결된다. 상기 투명전극층들은 상기 상부 반도체층들에 전류를 분산시키며, 상기 활성층에서 생성된 광을 투과시킨다.

<21> 절연보호막이 상기 배선들 및 상기 절연층을 덮을 수 있다. 상기 절연보호막은 배선들이 외압에 의해 변형되는 것을 방지하며, 또한 수분 등에 의해 배선들이 오염되는 것을 방지한다.

<22> 상기 또 다른 기술적 과제를 이루기 위하여, 본 발명의 다른 태양은 안정한 배선들을 갖는 교류용 발광 다이오드 제조방법을 제공한다. 이 방법은 기판 상에 서로 이격된 발광셀들을 형성하는 것을 포함한다. 상기 발광셀들은 각각 하부 반도체층, 상기 하부 반도체층의 일 영역 상부에 위치하는 상부 반도체층 및 상기 하부 반도체층과 상기 상부 반도체층 사이에 개재된 활성층을 포함하고, 상기 발광셀들의 측벽들은 상기 기판의 상부면에 대해 경사지게 형성되어 위로 갈수록 폭이 좁아진다. 연속적인(conformal) 절연층이 상기 발광셀들을 갖는 기판 상에 형성된다. 이어서, 상기 절연층을 패터닝하여 상기 하부 반도체층들의 다른 영역들 및 상기 상부 반도체층들 상에 개구부들이 형성된다. 그 후, 상기 절연층 상에 배선들이 형성된다. 상기 배선들은 상기 개구부들을 통해 상기 하부 반도체층들 및 상기 상부 반도체층들에 전기적으로 연결되고, 인접한 발광셀들의 상기 하부 반도체층들과 상

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기 상부 반도체층들을 각각 전기적으로 연결한다. 본 태양에 따르면, 발광셀들의 측벽들이 경사지게 형성되므로, 상기 절연층을 연속적으로 형성하는 것이 쉽다. 또한 연속적인(conformal) 절연층을 형성할 수 있어, 상기 절연층이 발광셀들의 단락을 방지한다. 이에 더하여, 상기 절연층에 의해 지지되는 배선들을 형성할 수 있어 신뢰성 있는 교류용 발광 다이오드를 제조할 수 있다.

<23> 한편, 상기 절연층을 형성하기 전, 전극패드들이 상기 발광셀들의 하부 반도체층들의 다른 영역들 상에 형성될 수 있다. 상기 전극패드들은 상기 하부 반도체층들의 다른 영역들 상에 형성된 개구부들에 의해 노출된다. 즉, 상기 전극패드들은 상기 절연층에 개구부들을 형성하는 동안 노출되어 상기 하부 반도체층들이 노출되는 것을 방지한다. 이에 따라, 상기 하부 반도체층들이 상기 개구부들을 형성하는 동안 손상되는 것을 방지할 수 있다.

<24> 또한, 상기 절연층을 형성하기 전, 투명전극층들이 상기 발광셀들의 상부 반도체층들 상에 형성될 수 있다. 상기 투명전극층들은 상기 상부 반도체층들 상에 형성된 개구부들에 의해 노출된다. 상기 상부 반도체층들 상에 투명전극층들이 형성되므로, 상기 배선들은 상기 투명전극층들에 접촉된다. 따라서, 상기 배선들의 물질 선택의 폭이 넓어진다.

<25> 한편, 상기 발광셀들을 형성하는 것은 상기 기판 전면에 하부 반도체층, 활성층 및 상부 반도체층을 형성하는 것을 포함한다. 상기 상부 반도체층 상에 발광셀 영역들을 한정하는 포토레지스트 패턴들이 형성될 수 있다. 그 후, 상기 포토레지스트 패턴들의 측벽들이 상기 기판 상부면에 대해 경사지도록 상기 포토레지스트

패턴들이 리플로우(reflow)된다. 이어서, 상기 포토레지스트 패턴들을 식각마스크로 사용하여 상기 상부 반도체층, 활성층 및 하부 반도체층이 차례로 식각된다. 이에 따라, 경사진 측벽들을 갖도록 발광셀 영역들이 분리된다.

<26> 한편, 상기 포토레지스트 패턴들은 상기 포토레지스트 패턴들의 측벽들이 상기 기판 상부면에 대해 15도 내지 80도 범위 내의 경사각을 갖도록 리플로우될 수 있다. 80도 이하의 경사각은 연속적인 절연층 형성 및 배선들을 형성하기 위해 요구되며, 15도 이상의 경사각은 충분한 발광영역들을 확보하기 위해 요구된다.

<27> 이에 더하여, 상기 상부 반도체층, 활성층 및 하부 반도체층을 차례로 식각한 후, 상기 상부 반도체층 및 활성층을 다시 패터닝하여 상기 하부 반도체층을 노출시킬 수 있다. 이와 달리, 상기 상부 반도체층, 활성층 및 하부 반도체층을 차례로 식각하기 전, 상기 상부 반도체층 및 활성층을 패터닝하여 상기 하부 반도체층을 노출시킬 수도 있다.

<28> 한편, 상기 배선들을 형성하는 것은 상기 절연층 상에 배선영역들을 한정하는 개구부들을 갖는 포토레지스트 패턴을 형성하는 것을 포함할 수 있다. 이어서, 상기 개구부들 내에 금속층이 도금된다. 그 후, 상기 포토레지스트 패턴이 제거되어 배선들이 형성된다.

<29> 이와 달리, 상기 배선들을 형성하는 것은 상기 절연층을 갖는 기판 상에 금속층을 증착하는 것을 포함할 수 있다. 이어서, 상기 금속층을 패터닝함으로써 배선들이 형성된다. 상기 발광셀들의 측벽이 경사져 있기 때문에, 금속층은 상기 절연층 상에 연속적으로 형성된다. 따라서, 금속층을 증착하고 이를 패터닝하여 배선

들을 형성하는 것이 수월하게 수행될 수 있다. 또한, 절연층이 상기 발광셀들의 측벽들을 덮고 있으므로, 금속층 물질이 발광셀들을 단락시키는 것을 방지할 수 있다.

<30> 이하, 첨부한 도면들을 참조하여 본 발명의 실시예들을 상세히 설명하기로 한다. 다음에 소개되는 실시예들은 당업자에게 본 발명의 사상이 충분히 전달될 수 있도록 하기 위해 예로서 제공되는 것이다. 따라서, 본 발명은 이하 설명되는 실시예들에 한정되지 않고 다른 형태로 구체화될 수도 있다. 그리고, 도면들에 있어서, 구성요소의 폭, 길이, 두께 등은 편의를 위하여 과장되어 표현될 수 있다. 명세서 전체에 걸쳐서 동일한 참조번호들은 동일한 구성요소들을 나타낸다.

<31> 도 3은 본 발명의 일 실시예에 따른 교류용 발광 다이오드를 설명하기 위한 단면도이다.

<32> 도 3을 참조하면, 단일 기판(51) 상에 복수개의 발광셀들(56)이 이격되어 위치한다. 상기 기판(51)은 절연 또는 도전성 기판일 수 있으며, 예컨대 사파이어 또는 탄화실리콘(SiC) 기판일 수 있다.

<33> 상기 발광셀들(56) 각각은 하부 반도체층(55), 상기 하부 반도체층의 일영역 상에 위치하는 상부 반도체층(59) 및 상기 하부 반도체층과 상부 반도체층 사이에 개재된 활성층(57)을 포함한다. 여기서, 상기 하부 및 상부 반도체층은 각각 n형 및 p형, 또는 p형 및 n형이다.

<34> 하부 반도체층(55), 활성층(57) 및 상부 반도체층(59)은 각각 질화갈륨 계열의 반도체 물질 즉, (B, Al, In, Ga)N으로 형성될 수 있다. 상기 활성층(57)은 요

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구되는 파장의 광 예컨대 자외선 또는 청색광을 방출하도록 조성 원소 및 조성비가 결정되며, 하부 반도체층(55) 및 상부 반도체층(59)은 상기 활성층(57)에 비해 밴드갭이 큰 물질로 형성된다.

<35> 상기 하부 반도체층(55) 및/또는 상부 반도체층(59)은, 도시한 바와 같이, 단일층으로 형성될 수 있으나, 다층 구조로 형성될 수도 있다. 또한, 활성층(57)은 단일 양자웰 또는 다중 양자웰 구조를 가질 수 있다.

<36> 한편, 발광셀들(56)과 기판(51) 사이에 버퍼층(53)이 개재될 수 있다. 버퍼층(53)은 기판(51)과 그 위에 형성될 하부 반도체층(55)의 격자부정합을 완화시키기 위해 채택된다. 버퍼층(53)은, 도시한 바와 같이 연속적일 수 있으나, 이에 한정되는 것은 아니며, 하부 반도체층들(55) 아래에 한정되어 위치할 수 있다.

<37> 발광셀들(56)의 측벽들은 기판(51) 상부면에 대해 경사지게 형성되어 위로 갈수록 폭이 좁아진다. 상기 측벽들의 경사는 활성층(57)에서 생성된 광의 방출 효율을 향상시키며, 상기 발광셀들(56) 위에 형성될 다른 층들의 연속적인 (conformal) 증착을 돕는다. 본 실시예에 있어서, 상기 발광셀들(56) 각각의 하부 반도체층(55)의 측벽들이 기판(51)의 상부면과 이루는 경사각은 15도 내지 80도의 범위 내일 수 있다.

<38> 절연층(69)이 발광셀들(56)의 전면을 덮는다. 절연층(69)은 하부 반도체층들(55)의 다른 영역들, 즉 상부 반도체층(59)이 형성된 영역에 인접하는 영역 상에 개구부들을 가지며, 또한 상부 반도체층들(59) 상에 개구부들을 갖는다. 상기 개구부들은 서로 이격되어 위치하며, 따라서 발광셀들(56)의 측벽들은 절연층(69)에 의

해 덮인다. 절연층(69)은 또한 발광셀들(56) 사이 영역들 내의 기판(51) 또는 버퍼층(53)을 덮을 수 있다. 절연층(69)은 실리콘산화막(SiO_2)으로 형성될 수 있다.

<39> 배선들(71)이 절연층(69) 상에 형성된다. 배선들(71)은 상기 개구부들을 통해 하부 반도체층들(55) 및 상부 반도체층들(59)에 전기적으로 연결된다. 또한 배선들(71)은 인접한 발광셀들(56)의 하부 반도체층들(55)과 상부 반도체층들(59)을 각각 전기적으로 연결하여 발광셀들(56)의 직렬 어레이를 형성한다. 이러한 어레이들이 복수개 형성될 수 있으며, 복수개의 어레이들이 서로 역병렬로 연결되어 교류전원에 연결되어 구동될 수 있다. 또한, 발광셀들의 직렬 어레이에 연결된 브리지 정류기(도시하지 않음)가 형성될 수 있으며, 상기 브리지 정류기에 의해 상기 발광셀들이 교류전원하에서 구동될 수도 있다. 상기 브리지 정류기는 상기 발광셀들(56)과 동일한 구조의 발광셀들을 배선들(71)을 이용하여 결선함으로써 형성할 수 있다. 상기 배선들은 도전 물질, 예컨대 다결정 실리콘과 같은 도핑된 반도체 물질 또는 금속으로 형성될 수 있다.

<40> 한편, 하부 반도체층들(55)의 다른 영역들과 절연층(69) 사이에 전극패드들(67)이 개재될 수 있다. 전극패드들(67)은 하부 반도체층들(55)의 다른 영역들 상에 형성된 상기 개구부들에 의해 노출된다. 전극패드들(67)은 하부반도체층들(55)에 오믹콘택된다. 상기 배선들(71)은 상기 개구부들에 의해 노출된 전극패드들(67)에 접촉되어 하부 반도체층들(55)에 전기적으로 연결된다.

<41> 또한, 투명전극층들(65)이 상부 반도체층들(59)과 절연층(69) 사이에 개재될 수 있다. 투명전극층들(65)은 상부 반도체층들(59) 상에 형성된 상기 개구부들에

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의해 노출된다. 투명전극층들(65)은 활성층(57)에서 생성된 광을 투과시키며, 상부 반도체층들(59)에 전류를 분산시키어 공급한다. 상기 배선들(71)은 상기 개구부들에 의해 노출된 투명전극층들(65)에 접촉되어 상부 반도체층들(55)에 전기적으로 연결된다. 한편, 상기 투명전극층들(65) 상에 전극패드들(도시하지 않음)이 더 형성될 수 있으며, 상기 배선들(71)은 상기 전극패드들에 접촉될 수 있다.

<42> 한편, 절연보호막(73)이 상기 배선들(71) 및 상기 절연층(69)을 덮을 수 있다. 절연보호막(73)은 배선들(71)이 수분 등에 의해 오염되는 것을 방지하며, 외압에 의해 배선들(71)이 손상되는 것을 방지한다. 절연보호막(73)은 투광성물질, 예컨대 실리콘산화막으로 형성될 수 있다.

<43> 도 4 내지 도 9는 본 발명의 일 실시예에 따른 교류용 발광 다이오드를 제조하는 방법을 설명하기 위한 단면도들이다.

<44> 도 4를 참조하면, 기판(51) 상에 하부 반도체층(55), 활성층(57) 및 상부 반도체층(59)이 형성된다. 또한, 하부 반도체층(55)을 형성하기 전, 기판(51) 상에 버퍼층(53)이 형성될 수 있다.

<45> 상기 기판(51)은 사파이어(Al_2O_3), 탄화실리콘(SiC), 산화아연(ZnO), 실리콘(Si), 갈륨비소(GaAs), 갈륨인(GaP), 리튬-알루미나($LiAl_2O_3$), 질화붕소(BN), 질화알루미늄(AlN) 또는 질화갈륨(GaN) 기판일 수 있으나, 이에 한정되는 것은 아니며, 기판(51) 상에 형성될 반도체층의 물질에 따라 다양하게 선택될 수 있다.

<46> 버퍼층(53)은 기판(51)과 그 위에 형성될 반도체층(55)의 격자부정합을 완화

하기 위해 형성되며, 예컨대 질화갈륨(GaN) 또는 질화알루미늄(AlN)으로 형성될 수 있다. 상기 기판(51)이 도전성 기판인 경우, 상기 버퍼층(53)은 절연층 또는 반절연층으로 형성되는 것이 바람직하며, AlN 또는 반절연 GaN로 형성될 수 있다.

<47> 하부 반도체층(55), 활성층(57) 및 상부 반도체층(59)은 각각 질화갈륨 계열의 반도체 물질 즉, (B, Al, In, Ga)N로 형성될 수 있다. 상기 하부 및 상부 반도체층(55, 59) 및 활성층(57)은 금속유기화학기상증착(MOCVD), 분자선 성장(molecular beam epitaxy) 또는 수소화물 기상 성장(hydride vapor phase epitaxy; HVPE) 기술 등을 사용하여 단속적으로 또는 연속적으로 성장될 수 있다.

<48> 여기서, 상기 하부 및 상부 반도체층들은 각각 n형 및 p형, 또는 p형 및 n형이다. 질화갈륨 계열의 화합물 반도체층에서, n형 반도체층은 불순물로 예컨대 실리콘(Si)을 도핑하여 형성될 수 있으며, p형 반도체층은 불순물로 예컨대 마그네슘(Mg)을 도핑하여 형성될 수 있다.

<49> 상기 상부 반도체층(59) 상에 발광셀 영역들을 한정하는 포토레지스트 패턴들(63)이 형성된다. 상기 포토레지스트 패턴들은 발광셀 영역들을 덮도록 형성된다. 한편, 측벽들이 기판(51) 상부면에 대해 경사지도록 상기 포토레지스트 패턴들(63)은 리플로우(reflow)된다. 상기 포토레지스트 패턴들(63)의 측벽들이 기판(51) 상부면에 대해 15도 내지 80도 범위 내의 경사각을 갖도록 형성될 수 있다.

<50> 도 5를 참조하면, 상기 포토레지스트 패턴들(63)을 식각마스크로 사용하여 상부 반도체층(59), 활성층(57) 및 하부 반도체층(55)을 차례로 식각한다. 이에 따라, 포토레지스트 패턴들(63)의 형상이 상기 반도체층들(59, 57, 55)에 전사되어

측벽들이 경사진 발광셀 영역들이 분리된다. 상기 식각 공정에 의해 버퍼층(53)이 노출될 수 있으며, 노출된 버퍼층(53)은 과식각에 의해 제거될 수 있다.

<51> 그 후, 상기 포토레지스트 패턴들(63)을 제거하고, 상기 상부 반도체층 및 활성층을 다시 패터닝하여 상기 식각된 하부 반도체층들(55)을 노출시킨다. 이때, 노출된 하부 반도체층들은 과식각에 의해 부분적으로 식각될 수 있다. 그 결과, 기판(51) 상에 서로 이격된 발광셀들(56)이 형성된다. 상기 발광셀들(56) 각각은 식각되어 서로 이격된 하부 반도체층(56), 상기 하부 반도체층(56)의 일 영역 상부에 위치하는 상부 반도체층(57) 및 상기 하부 반도체층(55)과 상기 상부 반도체층(57) 사이에 개재된 활성층(57)을 포함하고, 상기 하부 반도체층(56)의 다른 영역은 노출된다. 또한, 발광셀들(56)의 측벽들 대부분은 기판(51) 상부면에 대해 경사지게 형성된다. 한편, 하부 반도체층들(55)의 다른 영역들과 인접한 상부 반도체층들(59)의 측벽들은, 도시한 바와 같이 경사지게 형성될 수 있으나, 수직하게 형성될 수도 있다.

<52> 도 6을 참조하면, 상기 발광셀(56)의 상부 반도체층(59) 상에 투명전극층(65)이 형성될 수 있다. 상기 투명전극층(65)은 인디움 틴 산화막(ITO) 또는 Ni/Au와 같은 투명금속으로 형성된다. 또한, 상기 하부 반도체층들(55)의 다른 영역들 상에 전극패드들(67)이 형성될 수 있다. 상기 전극패드들(67)은 상기 하부 반도체층들(55)에 오믹콘택된다.

<53> 상기 투명전극층(65)은 포토레지스트 패턴들(63)을 형성하기 전, 상부 반도체층(59) 상에 형성될 수도 있다. 이때, 투명전극층(65)은 상부 반도체층과 함께

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패터닝된다.

<54> 도 7을 참조하면, 발광셀들(56)을 갖는 기판(51) 상에 연속적인 절연층(69)이 형성된다. 절연층(69)은 발광셀들(56)의 측벽 및 상부면을 덮고, 발광셀들(56) 사이 영역의 기판(51) 상부를 덮는다. 상기 절연층(69)은 화학기상증착(CVD) 기술을 사용하여 예컨대 실리콘 산화막으로 형성될 수 있다.

<55> 상기 발광셀들(56)의 측벽들이 경사지게 형성되어 있으므로, 상기 절연층(69)은 발광셀들(56)의 측벽들을 쉽게 덮을 수 있다. 상부 반도체층(59) 및 활성층(57)의 전체 두께가 얇고, 또한 상부 반도체층들(59) 사이의 공간이 넓기 때문에, 상기 하부 반도체층들(55)의 다른 영역들에 인접한 상부 반도체층들(59)의 측벽들도 절연층(69)에 의해 쉽게 덮일 수 있다.

<56> 도 8을 참조하면, 상기 절연층(69)을 패터닝하여 하부 반도체층들(55)의 다른 영역들 및 상부 반도체층들(59) 상에 개구부들이 형성된다. 전극패드들(67) 및 투명전극층들(65)이 형성된 경우, 상기 개구부들에 의해 전극패드들(67) 및 투명전극층들(65)이 노출된다.

<57> 상기 개구부들은 사진 및 식각 공정을 사용하여 형성될 수 있으며, 전극패드들(67)은 절연층(69)을 식각하는 동안 하부 반도체층들(55)이 손상되는 것을 방지한다.

<58> 도 9를 참조하면, 상기 개구부들을 갖는 절연층(69) 상에 배선들(71)이 형성된다. 상기 배선들(71)은 상기 개구부들을 통해 하부 반도체층들(55) 및 상부 반도체층들(59)에 전기적으로 연결되고, 인접한 발광셀들(56)의 하부 반도체층들(55)과

상부 반도체층들(59)을 각각 전기적으로 연결하여 직렬 연결된 어레이들을 형성한다.

<59> 상기 배선들(71)은 도금 기술을 사용하여 형성될 수 있다. 즉, 상기 절연층(69) 상에 배선 영역을 한정하는 개구부들을 갖는 포토레지스트 패턴을 형성하고, 상기 개구부들 내에 금속층을 도금한 후, 상기 포토레지스트 패턴을 제거함으로써 배선들(71)을 형성할 수 있다.

<60> 이와 달리, 상기 배선들(71)은, 화학기상증착 또는 물리기상증착 기술을 사용하여 형성될 수 있다. 즉, 전자빔 증착(e-beam evaporation)과 같은 기상증착 기술을 사용하여 금속층을 형성한 후, 이를 사진 및 식각 공정을 사용하여 패터닝함으로써 배선들(71)을 형성할 수 있다. 상기 발광셀들(56)의 측벽들이 경사져 있으므로, 금속층은 발광셀들의(56) 측벽 상부에 연속적으로 형성된다. 또한, 절연층(69)이 발광셀들(56)의 측벽들을 덮고 있으므로, 금속층 패터닝 후 잔존하는 금속 물질에 의해 발광셀들(56)이 단락되는 것을 방지할 수 있다.

<61> 상기 배선들(71)이 형성된 기판(51) 상에 보호절연막(73)이 형성된다. 상기 보호절연막(73)은 화학기상증착 기술을 사용하여, 투광성 물질, 예컨대 실리콘 산화막으로 형성될 수 있다. 그 결과, 도 1의 교류용 발광 다이오드가 완성된다.

【발명의 효과】

<62> 본 발명의 실시예들에 따르면, 외압에 의해 배선들이 단선 또는 단락되는 것을 방지할 수 있어 신뢰성 있는 교류용 발광 다이오드를 제공할 수 있으며, 배선들을 형성하는 동안 잔존하는 금속 등의 도전성 물질이 발광셀들을 단락시키는 것을

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방지할 수 있다. 또한, 절연층에 의해 지지되는 배선들을 형성할 수 있어 신뢰성 있는 교류용 발광 다이오드를 제조할 수 있다.

【특허청구범위】

【청구항 1】

기판 상에 서로 이격되어 위치하고, 각각 하부 반도체층, 상기 하부 반도체층의 일 영역 상부에 위치하는 상부 반도체층 및 상기 하부 반도체층과 상기 상부 반도체층 사이에 개재된 활성층을 포함하고, 측벽들이 상기 기판의 상부면에 대해 경사지게 형성되어 위로 갈수록 폭이 좁아지는 발광셀들;

상기 발광셀들의 전면을 덮되, 상기 하부 반도체층들의 다른 영역들 및 상기 상부 반도체층들 상에 각각 형성된 개구부들을 갖는 절연층;

상기 절연층 상에 형성되어 상기 개구부들을 통해 상기 하부 반도체층들 및 상기 상부 반도체층들에 전기적으로 연결되고, 인접한 발광셀들의 상기 하부 반도체층들과 상기 상부 반도체층들을 각각 전기적으로 연결하는 배선들을 포함하는 교류용 발광 다이오드.

【청구항 2】

청구항 1에 있어서,

상기 발광셀들 각각의 하부 반도체층의 측벽들이 상기 기판의 상부면과 이루는 경사각이 15도 내지 80도의 범위 내인 것을 특징으로 하는 교류용 발광 다이오드.

【청구항 3】

청구항 1에 있어서,

상기 하부 반도체층들의 다른 영역들과 상기 절연층 사이에 개재된 전극패드들을 더 포함하고, 상기 전극패드들은 상기 하부 반도체층들의 다른 영역들 상에 형성된 개구부들에 의해 노출되는 교류용 발광 다이오드.

【청구항 4】

청구항 3에 있어서,

상기 상부 반도체층들과 상기 절연층 사이에 개재된 투명전극층들을 더 포함하고, 상기 투명전극층들은 상기 상부 반도체층들 상에 형성된 개구부들에 의해 노출되는 교류용 발광 다이오드.

【청구항 5】

청구항 1에 있어서,

상기 배선들 및 상기 절연층을 덮는 절연보호막을 더 포함하는 교류용 발광 다이오드.

【청구항 6】

기판 상에 서로 이격된 발광셀들을 형성하되, 상기 발광셀들은 각각 하부 반도체층, 상기 하부 반도체층의 일 영역 상부에 위치하는 상부 반도체층 및 상기 하부 반도체층과 상기 상부 반도체층 사이에 개재된 활성층을 포함하고, 상기 발광셀들의 측벽들은 상기 기판의 상부면에 대해 경사지게 형성되어 위로 갈수록 폭이 좁아지고,

상기 발광셀들을 갖는 기판 상에 연속적인 절연층을 형성하고,

상기 절연층을 패터닝하여 상기 하부 반도체층들의 다른 영역들 및 상기 상부 반도체층들 상에 개구부들을 형성하고,

상기 절연층 상에 배선들을 형성하되, 상기 배선들은 상기 개구부들을 통해 상기 하부 반도체층들 및 상기 상부 반도체층들에 전기적으로 연결되고, 인접한 발광셀들의 상기 하부 반도체층들과 상기 상부 반도체층들을 각각 전기적으로 연결하는 것을 포함하는 교류용 발광 다이오드 제조방법.

【청구항 7】

청구항 6에 있어서,

상기 절연층을 형성하기 전, 상기 발광셀들의 하부 반도체층들의 다른 영역들 상에 전극패드들을 형성하는 것을 더 포함하고, 상기 전극패드들은 상기 하부 반도체층들의 다른 영역들 상에 형성된 개구부들에 의해 노출되는 교류용 발광 다이오드 제조방법.

【청구항 8】

청구항 7에 있어서,

상기 절연층을 형성하기 전, 상기 발광셀들의 상부 반도체층들 상에 투명전극층들을 형성하는 것을 더 포함하고, 상기 투명전극층들은 상기 상부 반도체층들 상에 형성된 개구부들에 의해 노출되는 교류용 발광 다이오드 제조방법.

【청구항 9】

청구항 6에 있어서,

상기 발광셀들을 형성하는 것은,

상기 기판 전면에 하부 반도체층, 활성층 및 상부 반도체층을 형성하고,

상기 상부 반도체층 상에 발광셀 영역들을 한정하는 포토레지스트 패턴들을 형성하고,

상기 포토레지스트 패턴들의 측벽들이 상기 기판 상부면에 대해 경사지도록 상기 포토레지스트 패턴들을 리플로우하고,

상기 포토레지스트 패턴들을 식각마스크로 사용하여 상기 상부 반도체층, 활성층 및 하부 반도체층을 차례로 식각하는 것을 포함하는 교류용 발광 다이오드 제조방법.

【청구항 10】

청구항 9에 있어서,

상기 포토레지스트 패턴들을 리플로우하는 것은 상기 포토레지스트 패턴들의 측벽들이 상기 기판 상부면에 대해 15도 내지 80도 범위 내의 경사각을 갖도록 수행되는 교류용 발광 다이오드 제조방법.

【청구항 11】

청구항 9에 있어서,

상기 상부 반도체층, 활성층 및 하부 반도체층을 차례로 식각한 후, 상기 상부 반도체층 및 활성층을 다시 패터닝하여 상기 하부 반도체층을 노출시키는 것을 더 포함하는 교류용 발광 다이오드 제조방법.

【청구항 12】

청구항 6에 있어서,

상기 배선들을 형성하는 것은

상기 절연층 상에 배선 영역을 한정하는 개구부들을 갖는 포토레지스트 패턴을 형성하고,

상기 개구부들 내에 금속층을 도금하고,

상기 포토레지스트 패턴을 제거하는 것을 포함하는 교류용 발광 다이오드 제조방법.

【청구항 13】

청구항 6에 있어서,

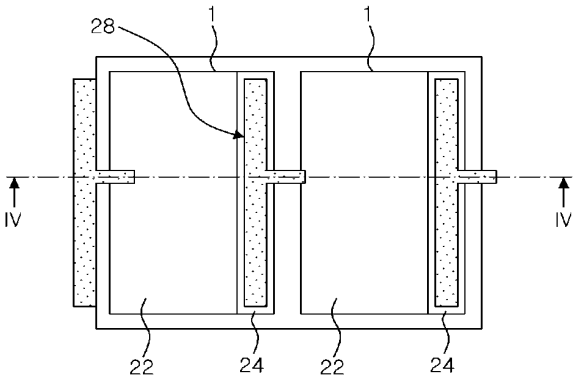
상기 배선들을 형성하는 것은

상기 절연층을 갖는 기판 상에 금속층을 증착하고,

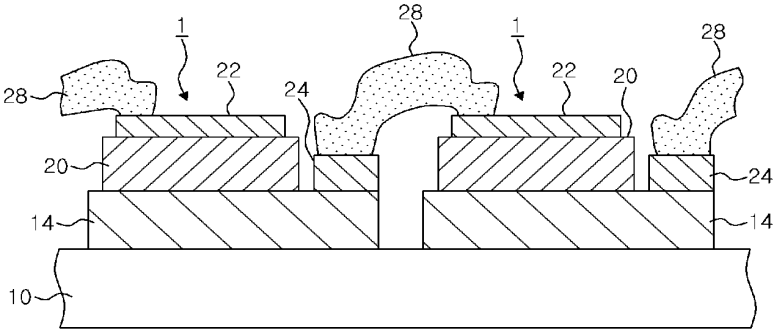
상기 금속층을 패터닝하는 것을 포함하는 교류용 발광 다이오드 제조방법.

【도면】

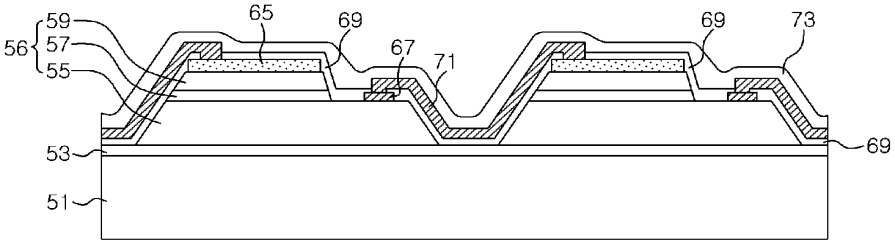
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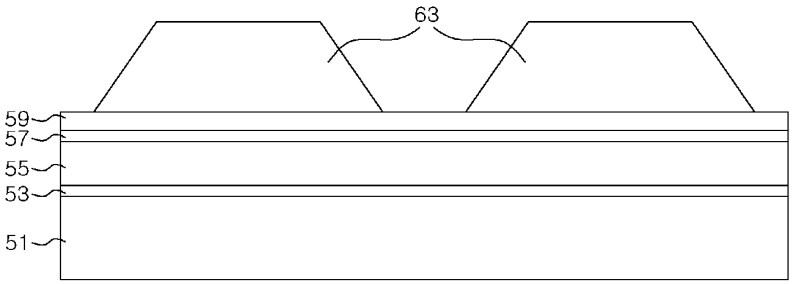
【도 2】


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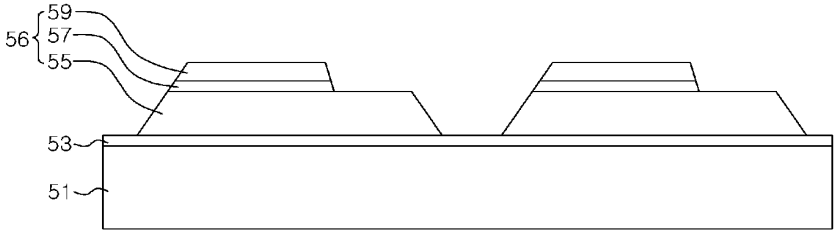
【도 3】


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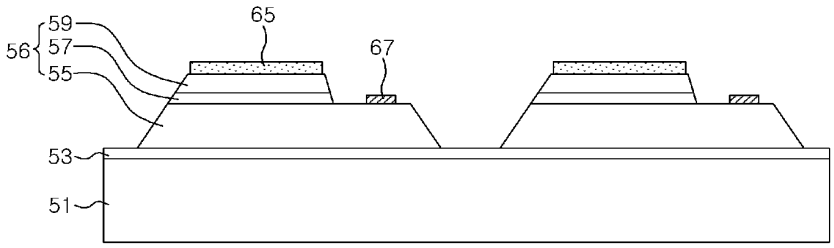
【도 4】



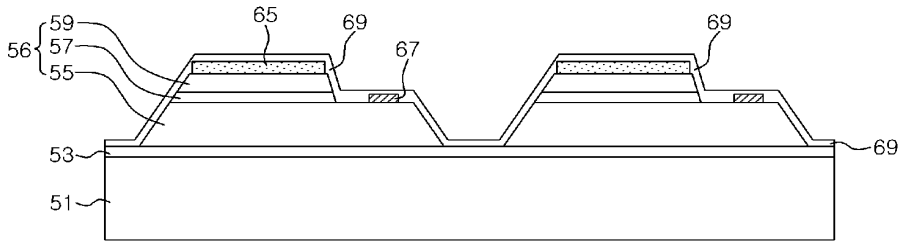
【도 5】



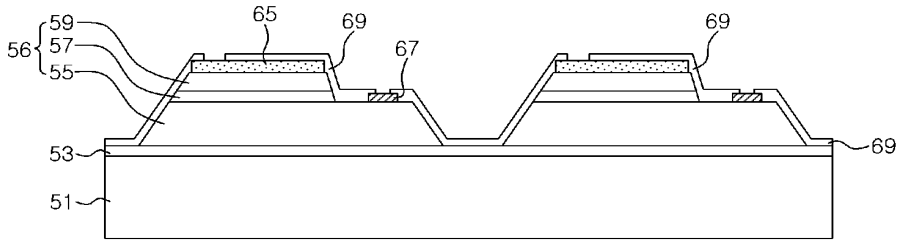
【도 6】



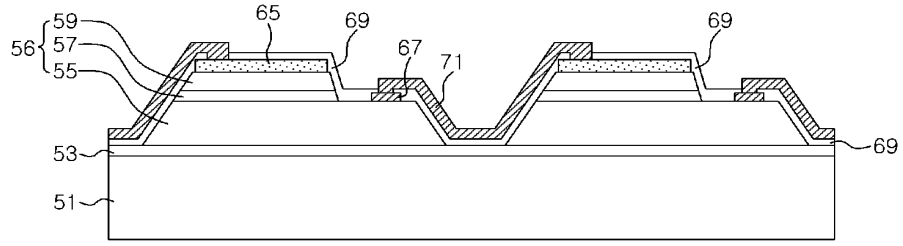
【도 7】


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【도 8】


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【도 9】


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DO/ EO WORKSHEET

Patent Application Specialist/ National Stage Division

U.S. Appl. No. 11993965 International Appl. No. PCT/KR2006/002427

Application filed by : ☐ 20 months ☑ 30 months

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INTERNATIONAL APPLICATION PAPERS IN THE APPLICATION FILE :

☑ International Application *(RECORD COPY)*

☐ Article 19 Amendments

☐ PCT/IPEA/409 IPER : ☐ EP ☐ JP ☐ SE ☐ AU ☐ US ☐ FR ☐ CN ☐ ES ☐ RU ☐ AT ☐ KR ☐ ___

☐ Annexes to 409

☐ PCT/ISA/237 : ☐ EP ☐ JP ☐ SE ☐ AU ☐ US ☐ FR ☐ CN ☐ ES ☐ RU ☐ AT ☐ KR ☐ ___

☐ PCT/IPEA/409 or PCT/ISA/237 was NOT AVAILABLE at the time of paralegal review

☐ PCT/IB/306

☐ Request form PCT/RO/101

☑ PCT/ISA/210 - Search Report : ☐ EP ☐ JP ☐ SE ☐ AU ☐ US ☐ FR ☐ CN ☐ ES ☐ RU ☐ AT ☑ KR ☐ ___ ☐ NONE

☐ Search Report References

☑ Priority Document (s) No. 3

☐ N/A

☐ Priority Document was NOT AVAILABLE at the time of paralegal review

☐ Other : _____

RECEIPTS FROM THE APPLICANT *(other than checked above) :*

☑ Basic National Fee *(or authorization to charge)*

☑ Description ☑ Claims ☑ Abstract

☑ Drawing Figure(s) - (# of drwgs. 11)

☐ Translation of Article 19 Amendments ☐ entered ☐ not entered : ☐ not a page for page substitution ☐ replaced by Article 34 Amendment

☐ Annexes to 409 ☐ entered ☐ not entered : ☐ not a page for page substitution ☐ no translation ☐ other : _____

☐ Application Data Sheet

☐ Power of Attorney

☐ Change of Address

☑ Preliminary Amendment(s) Filed on : 1. ☐ same as 371 request date 2. _____ 3. _____

☑ Information Disclosure Statement(s) Filed on : 1. ☐ same as 371 request date 2. _____ 3. _____

☐ Assignment Document (forwarded to Assignment Branch)

☐ Assignee Statement Under 37 CFR 3.73(b)

☐ Assignee PG Publication Notice

☐ Substitute Specification Filed on : 1. ☐ same as 371 request date 2. _____ 3. _____

☐ Verified Small Status Statement

☑ Oath/ Declaration (executed)

☐ Oath/ Declaration ☐ unsigned ☐ no citizenship ☐ other

☐ DNA Diskette ☐ Sequence Listing

☐ Other : _____

NOTES : ☐ I.A. used as Specification ☐ Other :

35 U.S.C. 371 - Receipt of Request (PTO-1390)	mo. 12 day 26 yr. 2007
Date Acceptable Oath/ Declaration Received	☐ Same as 371 Req. Date; ☐ mo. 12 day 26 yr. 2007
Date of Completion of requirements under 35 U.S.C. 371	☐ Same as 371 Req. Date; ☐ Same as OATH Date; ☐ mo. 12 day 26 yr. 2007
Date of Completion of DO/ EO 903 - Notification of Acceptance	
Date of Completion of DO/ EO 905 - Notification of Missing Requirements	
Date of Completion of DO/ EO 909 - Notification of Abandonment	
Date of Completion of DO/ EO 916 - Notification of Defective Response	
Date of Completion of DO/ EO 922 - Notification to Comply w/ Requirements for Patent Applications Containing Nucleotide and/or Amino Acid Sequence Disclosures	
Date of Completion of DO/ EO 923	

MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET

(FOR USE WITH FORM PTO-875)

SERIAL NO. 11/993965 | FILING DATE 12-26-07

APPLICANT(S)

CLAIMS

16/3

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
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2		1		1		
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4		2		1		
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TOTAL IND.	3		3			
TOTAL DEP.	27		13			
TOTAL CLAIMS	30		16			

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
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TOTAL IND.						
TOTAL DEP.						
TOTAL CLAIMS						

PTO-1360 (REV. 11/04)

U.S. DEPARTMENT of COMMERCE
Patent and Trademark Office

PATENT APPLICATION FEE DETERMINATION RECORD

Effective December 8, 2004

Application or Docket Number: 11993965

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)	SMALL ENTITY TYPE ☐	RATE	FEE	OR	OTHER THAN SMALL ENTITY	RATE	FEE
U.S. NATIONAL STAGE FEES									
BASIC FEE	SMALL ENT. = $ 150	LARGE ENT. = $ 300		BASIC FEE		OR		BASIC FEE	310
EXAMINATION FEE	Satisfies PCT Article 33(1)-(4) = $ 50 / $ 100	All other situations = $ 100 / $ 200		EXAM. FEE				EXAM. FEE	210
SEARCH FEE	U.S. is ISA = $ 50 / $ 100 ALL other countries = $ 200 / $ 400	ALL other situations = $ 250 / $ 500		SEARCH FEE				SEARCH FEE	410
FEE FOR EXTRA SPEC. PGS.	minus 100 =	/ 50 =		X $ 125 =				X $ 250 =	Ø
TOTAL CHARGEABLE CLAIMS	14 minus 20 =	*		X $ 25 =		OR		X $ 50 =	Ø
INDEPENDENT CLAIMS	3 minus 3 =	*		X $ 100 =		OR		X $ 200 =	Ø
MULTIPLE DEPENDENT CLAIM PRESENT	☐			+ $ 180 =		OR		+ $ 360 =	Ø
* If the difference in column 1 is less than zero, enter "0" in column 2				TOTAL		OR		TOTAL	930

CLAIMS AS AMENDED - PART II

SMALL ENTITY OR OTHER THAN SMALL ENTITY

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE	ADDI-TIONAL FEE	OR	RATE	ADDI-TIONAL FEE
AMENDMENT A	Total	*	Minus	**	=	X $ 25 =		OR	X $ 50 =	
	Independent	*	Minus	***	=	X $ 100 =		OR	X $ 200 =	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐					+ $ 180 =		OR	+ $ 360 =	
						TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE	ADDI-TIONAL FEE	OR	RATE	ADDI-TIONAL FEE
AMENDMENT B	Total	*	Minus	**	=	X $ 25 =		OR	X $ 50 =	
	Independent	*	Minus	***	=	X $ 100 =		OR	X $ 200 =	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐					+ $ 180 =		OR	+ $ 360 =	
						TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than '20', enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than '3', enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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Alexandria, Virginia 22313-1450
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U.S. APPLICATION NUMBER NO.	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
11/993,965	Jong Lam Lee	3576-053

20575
MARGER JOHNSON & MCCOLLOM, P.C.
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204

INTERNATIONAL APPLICATION NO.	
PCT/KR2006/002427	
I.A. FILING DATE	PRIORITY DATE
06/22/2006	06/22/2005

CONFIRMATION NO. 2191
371 FORMALITIES LETTER



Date Mailed: 05/13/2008

Notification of Insufficient Fees (DO/EO/US)

The following items have been submitted by the applicant or the IB to the United States Patent and Trademark Office as a Designated Office (37 CFR 1.494):

- Priority Document
- Copy of the International Application filed on 12/26/2007
- Copy of the International Search Report filed on 12/26/2007
- Preliminary Amendments filed on 12/26/2007
- Information Disclosure Statements filed on 12/26/2007
- Oath or Declaration filed on 12/26/2007
- U.S. Basic National Fees filed on 12/26/2007
- Priority Documents filed on 12/26/2007

The following items **MUST** be furnished within the period set forth below in order to complete the requirements for acceptance under 35 U.S.C. 371:

- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.492(h) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fees required for this application is $**130** for a Large Entity:
- $**130** Surcharge.

ALL OF THE ITEMS SET FORTH ABOVE MUST BE SUBMITTED WITHIN TWO (2) MONTHS FROM THE DATE OF THIS NOTICE OR BY 32 MONTHS FROM THE PRIORITY DATE FOR THE APPLICATION, WHICHEVER IS LATER. FAILURE TO PROPERLY RESPOND WILL RESULT IN ABANDONMENT.

The time period set above may be extended by filing a petition and fee for extension of time under the provisions of 37 CFR 1.136(a).

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

FORM PCT/DO/EO/923 (371 Formalities Notice)

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

DIAN S GORDON

Telephone: (703) 308-9290 EXT 125

FORM PCT/DO/EO/923 (371 Formalities Notice)

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
11/993,965	12/26/2007	2811	930	3576-053	16	3

CONFIRMATION NO. 2191

20575
MARGER JOHNSON & MCCOLLOM, P.C.
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204

FILING RECEIPT

OC00000029849621

Date Mailed: 05/13/2008

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Jong Lam Lee, Pohang, KOREA, REPUBLIC OF;
Jae Ho Lee, Yongin, KOREA, REPUBLIC OF;
Yeo Jin Yoon, Ansan, KOREA, REPUBLIC OF;
Eu Jin Hwang, Siheung, KOREA, REPUBLIC OF;
Dae Won Kim, Seoul, KOREA, REPUBLIC OF;

Assignment For Published Patent Application

SEOUL OPTO-DEVICE CO., LTD., Ansan, KR

Power of Attorney: The patent practitioners associated with Customer Number 20575

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/KR2006/002427 06/22/2006

Foreign Applications

REPUBLIC OF KOREA 1020050053797 06/22/2005
REPUBLIC OF KOREA 1020050055179 06/24/2005
REPUBLIC OF KOREA 1020060021801 03/08/2006

If Required, Foreign Filing License Granted: 05/08/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 11/993,965**

Projected Publication Date: 371 Supplemental Fees Missing

Non-Publication Request: No

Early Publication Request: No

Title

Light Emitting Device and Method of Manufacturing the Same

Preliminary Class

257

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
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U.S. APPLICATION NUMBER NO.	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
11/993,965	Jong Lam Lee	3576-053

20575
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PORTLAND, OR 97204

INTERNATIONAL APPLICATION NO.	
PCT/KR2006/002427	
I.A. FILING DATE	PRIORITY DATE
06/22/2006	06/22/2005

CONFIRMATION NO. 2191
371 ACCEPTANCE LETTER



Date Mailed: 07/10/2008

NOTICE OF ACCEPTANCE OF APPLICATION UNDER 35 U.S.C 371 AND 37 CFR 1.495

The applicant is hereby advised that the United States Patent and Trademark Office in its capacity as a Designated / Elected Office (37 CFR 1.495), has determined that the above identified international application has met the requirements of 35 U.S.C. 371, and is ACCEPTED for national patentability examination in the United States Patent and Trademark Office.

The United States Application Number assigned to the application is shown above and the relevant dates are:

12/26/2007	12/26/2007
DATE OF RECEIPT OF 35 U.S.C. 371(c)(1), (c)(2) and (c)(4) REQUIREMENTS	DATE OF COMPLETION OF ALL 35 U.S.C. 371 REQUIREMENTS

A Filing Receipt (PTO-103X) will be issued for the present application in due course. **THE DATE APPEARING ON THE FILING RECEIPT AS THE " FILING DATE" IS THE DATE ON WHICH THE LAST OF THE 35 U.S.C. 371 (c)(1), (c)(2) and (c)(4) REQUIREMENTS HAS BEEN RECEIVED IN THE OFFICE. THIS DATE IS SHOWN ABOVE.** *The filing date of the above identified application is the international filing date of the international application (Article 11(3) and 35 U.S.C. 363).* Once the Filing Receipt has been received, send all correspondence to the Group Art Unit designated thereon.

The following items have been received:

- Copy of the International Application filed on 12/26/2007
- Copy of the International Search Report filed on 12/26/2007
- Preliminary Amendments filed on 12/26/2007
- Information Disclosure Statements filed on 12/26/2007
- Oath or Declaration filed on 12/26/2007
- U.S. Basic National Fees filed on 12/26/2007
- Priority Documents filed on 12/26/2007

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

DIAN S GORDON

Telephone: (703) 308-9290 EXT 125

FORM PCT/DO/EO/903 (371 Acceptance Notice)

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
11/993,965	12/26/2007	2811	930	3576-053	16	3

CONFIRMATION NO. 2191

UPDATED FILING RECEIPT

20575
MARGER JOHNSON & MCCOLLOM, P.C.
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204



Date Mailed: 07/10/2008

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Yeo Jin Yoon, Ansan, KOREA, REPUBLIC OF;
Eu Jin Hwang, Siheung, KOREA, REPUBLIC OF;
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Assignment For Published Patent Application

SEOUL OPTO-DEVICE CO., LTD., Ansan, KR

Power of Attorney: The patent practitioners associated with Customer Number 20575

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/KR2006/002427 06/22/2006

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REPUBLIC OF KOREA 1020060021801 03/08/2006

If Required, Foreign Filing License Granted: 05/08/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 11/993,965**

Projected Publication Date: 10/16/2008

Non-Publication Request: No

Early Publication Request: No

Title

Light Emitting Device and Method of Manufacturing the Same

Preliminary Class

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PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

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Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

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set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

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Approved

PTO/SB/80 (01-05)
Approved for use through 12/31/2008. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

[X] Practitioners associated with the Customer Number: 58027

OR

[ ] Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

[X] The address associated with Customer Number: 58027

OR

[ ] Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address:
Seoul Opto Device Co., Ltd.
1-36 Block, 727-5 Wonsi-dong, Danwon-gu
Gyeonggi-do, Ansan-si, 425-851, Republic of Korea

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record
The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	05/15/08
Name	MURUGANANDAN NITHIPALAN	Telephone	—
Title	PRESIDENT & CEO		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/96 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Jong Lam LEE, et al.

Application No./Patent No.: 11/993,965 Filed/Issue Date: December 26, 2007

Entitled: LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME

Seoul Opto Device Co., Ltd., a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest; or
2. ☐ an assignee of less than the entire right, title, and interest

The extent (by percentage) of its ownership interest is _____ %

in the patent application/patent identified above by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 020368, Frame 0597, or for which a copy thereof is attached.

OR

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as shown below:

1. From:_____ To:_____
   The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

2. From:_____ To:_____
   The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

3. From:_____ To:_____
   The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet.

☐ Copies of assignments or other documents in the chain of title are attached.

[**NOTE**: A separate copy (i.e., a true copy of the original document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, if the assignment is to be recorded in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/hae-chan park/	July 11, 2008
Signature	Date
Hae-Chan Park, Reg. 50,114	703-288-5105
Printed or Typed Name	Telephone Number
Attorney	
Title	

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal

Application Number:	11993965
Filing Date:	26-Dec-2007
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Filer:	Hae-Chan Park/karim sosa
Attorney Docket Number:	3576-053
Filed as Large Entity	

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Oath/decl > 30 months from priority date	1617	1	130	130
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**130**

Electronic Acknowledgement Receipt

EFS ID:	3600388
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	20575
Filer:	Hae-Chan Park/Sarah Kuhns
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	3576-053
Receipt Date:	11-JUL-2008
Filing Date:	26-DEC-2007
Time Stamp:	11:31:04
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$130
RAM confirmation Number	6016
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)

1	Power of Attorney	Power_of_Attorney.pdf	161203 fb5649dc37516b534e9bb9b5f684412c4d131ce1	no	2
Warnings:					
Information:					
2	Fee Worksheet (PTO-06)	fee-info.pdf	8188 2e831146f2961ae3dc7311e9a9526f1043265446	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	169391		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/993,965	12/26/2007	Jong Lam Lee	3576-053

CONFIRMATION NO. 2191

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POA ACCEPTANCE LETTER

OC00000031040083

Date Mailed: 07/22/2008

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/11/2008.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/gbien-aime/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/993,965	12/26/2007	Jong Lam Lee	3576-053

CONFIRMATION NO. 2191

20575
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POWER OF ATTORNEY NOTICE

OC000000031039969

Date Mailed: 07/22/2008

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/11/2008.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/gbien-aime/

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PTO/SB/08a (03-08)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	11993965
Filing Date	2007-12-26
First Named Inventor	Jong Lam LEE
Art Unit	2811
Examiner Name	
Attorney Docket Number	P2317US00

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	1	2004-079867	JP		2004-03-11	Sakai SHIRO Nitride Semiconductor Co., Ltd.		☐
	2	10-2003-0022940	KR		2003-03-19	Epivalley Co., Ltd.		☐
	3	10-2005-0052474	KR		2005-06-02	Sakai SHIRO et al.		☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
	Art Unit	2811
	Examiner Name	
	Attorney Docket Number	P2317US00

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2008-07-30
Name/Print	Hae-Chan Park	Registration Number	50114

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2004-079867
(43)Date of publication of application : 11.03.2004

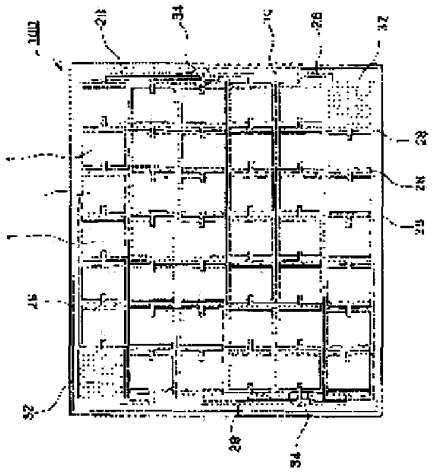
(51)Int.Cl. H01L 33/00
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(21)Application number : 2002-240116
(22)Date of filing : 21.08.2002

(71)Applicant : SAKAI SHIRO
NITRIDE SEMICONDUCTOR CO LTD
(72)Inventor : SAKAI SHIRO
YAMASHITA KENJI

(54) MANUFACTURING METHOD OF GALLIUM NITRIDE BASE COMPOUND SEMICONDUCTOR DEVICE, AND LIGHT EMITTING DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a GaN-base light emitting device having a broadband emission spectrum.
SOLUTION: An LED1 is constituted by successively forming, on a substrate 10, an n-GaN layer, an InGaN light emitting layer, a p-GaN layer, a p-electrode and an n-electrode. A plurality of such LED1's are monolithically formed on the substrate 10 so as to be connected in series, while causing the temperature distribution within the wafer plane when forming the InGaN light emitting layer and causing composition distribution therein. Thus, the light emitting device 100 having a broadband spectrum is obtained. By adjusting an In composition, the luminescent color turns to white.



(19)日本国特許庁(JP)　(12)公開特許公報(A)　(11)特許出願公開番号
特開2004-79867
(P2004-79867A)
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(51)Int.Cl.[7]	F I		テーマコード（参考）
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審査請求 未請求　請求項の数 12　OL　（全 13 頁）

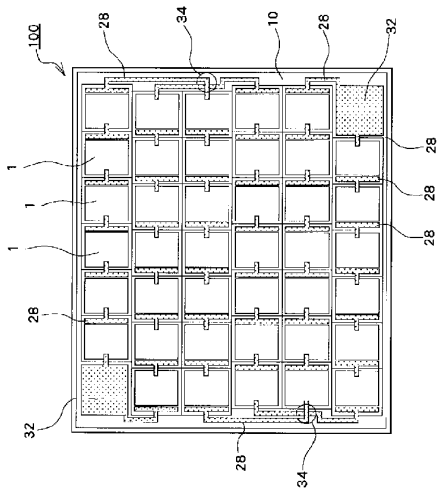
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最終頁に続く

(54)【発明の名称】窒化ガリウム系化合物半導体装置の製造方法及び発光装置

(57)【要約】
【課題】広帯域な発光スペクトルを有するGaN系発光装置を提供する。
【解決手段】ＬＥＤ１は基板１０上に順次ｎ－GaN層、ＩｎGaN発光層、Ｐ－GaN層、Ｐ－電極、ｎ－電極を形成して構成される。基板１０上に複数のＬＥＤ１をモノリシックに複数形成して直列接続するとともに、ＩｎGaN発光層を形成する際にウエハ面内で温度分布を生じさせ、組成分布を起こさせる。これにより、広帯域なスペクトルを有する発光装置１００が得られる。Ｉｎ組成を調整することで発光色が白色となる。
【選択図】　図１０



【特許請求の範囲】
【請求項１】
窒化ガリウム系化合物半導体装置を製造する方法であって、
（ａ）基板面内で温度分布を生じさせるステップと、
（ｂ）前記面内分布よりも小さいピッチで前記基板上にモノリシックに複数の窒化ガリウム系化合物半導体を形成するステップと、
（ｃ）前記複数の窒化ガリウム系化合物半導体を直列接続するステップ、
を有することを特徴とする窒化ガリウム系化合物半導体装置の製造方法。
【請求項２】
請求項１記載の方法において、
前記（ａ）ステップは、
（ａ１）前記基板の裏面に不連続的に溝を形成するステップと、
（ａ２）前記溝内に膜を形成するステップと、
（ａ３）前記基板の裏面側から加熱するステップ
を有することを特徴とする窒化ガリウム系化合物半導体装置の製造方法。
【請求項３】
請求項２記載の方法において、
前記膜はチタン膜であることを特徴とする窒化ガリウム系化合物半導体装置の製造方法。
【請求項４】
請求項１記載の方法において、
前記（ｂ）ステップは、
（ｂ１）前記基板上に複数のｎ型ＧａＮ系層を形成するステップと、
（ｂ２）前記ｎ型ＧａＮ系層上に$Al_yIn_xGa_{1-x-y}N$（但し、０≦Ｘ≦１．０≦Ｙ≦１）発光層を形成するステップと、
（ｂ３）前記発光層上にＰ型ＧａＮ系層を形成するステップと、
（ｂ４）前記ｎ型ＧａＮ系層及びＰ型ＧａＮ系層にそれぞれｎ電極及びＰ電極を接続するステップ
を有し、前記窒化ガリウム系化合物半導体は発光素子であり、複数の前記発光素子がモノリシックに直列接続されることを特徴とする窒化ガリウム系化合物半導体装置の製造方法。
【請求項５】
請求項４記載の方法において、
前記（ｂ）ステップにおいて前記基板上に形成される複数の前記発光素子の密度を不均一とすることを特徴とする窒化ガリウム系化合物半導体装置の製造方法。
【請求項６】
請求項４記載の方法において、
前記（ｂ）ステップにおいて前記基板上に形成される前記発光素子の面積を不均一とすることを特徴とする窒化ガリウム系化合物半導体装置の製造方法。
【請求項７】
請求項４記載の方法において、さらに、
（ｄ）前記発光素子を所定数毎に切り出して発光チップを形成するステップ
を有することを特徴とする窒化ガリウム系化合物半導体装置の製造方法。
【請求項８】
請求項７記載の方法において、
前記温度分布を調整することにより発光チップの発光スペクトルの半値幅を３０ｎｍ以上とすることを特徴とする窒化ガリウム系化合物半導体装置の製造方法。
【請求項９】
窒化ガリウム系化合物半導体を発光素子に用いた発光装置であって、
基板と、
前記基板上にモノリシックに直列接続された、前記基板の面内温度分布に起因して各発光

素子が異なる組成を有する複数の発光素子
を有することを特徴とする発光装置。
【請求項１０】
請求項９記載の装置において、
前記複数の発光素子のピッチは、前記組成の分布のピッチよりも小さいことを特徴とする発光装置。
【請求項１１】
請求項９記載の装置において、
前記複数の発光素子は二次元アレイ状に形成されて同数ずつ２組に分けられ、２個の電極に互いに反対極性となるように並列接続されることを特徴とする発光装置。
【請求項１２】
請求項１０記載の装置において、
前記複数の発光素子の発光スペクトルの半値幅は８０ｎｍ以上であり、
さらに、
前記複数の発光素子からの光により励起されて可視光を発光する蛍光体
を有することを特徴とする発光装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】
本発明は窒化ガリウム（ＧａＮ）系化合物半導体装置の製造方法及び発光装置に関し、特に発光スペクトルの調整に関する。
【０００２】
【従来の技術】
従来より、ＧａＮ系化合物半導体を用いた発光装置（ＬＥＤや半導体レーザ）が知られている。波長３６０～６００ｎｍ帯で発光するＬＥＤは、$In_xGa_{1-x}N$を発光層として用いる場合が多い。$In_xGa_{1-x}N$を発光層として用いた場合、組成Ｘを変化させることで発光波長は３６０ｎｍ～６００ｎｍの範囲で変化する。すなわち、Ｘ＝０の場合は発光波長３６０ｎｍであり、Ｘを増大させるほど長波長側にシフトする。３６０ｎｍ～６００ｎｍの波長帯で発光するＬＥＤは、表示用や照明用など多くの用途が考えられている。表示用の光源として考えた場合、原理的には光の３原色（Ｒ、Ｇ、Ｂ）を混ぜることで任意の色を表現できるので光源のスペクトルとしてはＲ、Ｇ、Ｂの３つの波長を有していれば足り、全ての視感度領域の波長を有する必要はない。しかしながら、より自然に近い色や、白色あるいは液晶ディスプレイのバックライトとして自然な色を表現するためには、光源の波長分布はできるだけ広く、望ましくは全ての視感度領域をカバーできる方がよい。
【０００３】
【発明が解決しようとする課題】
このような観点から、本願出願人は先に特願２００２－１０４８２１にて広い半値幅を有するＬＥＤを提案した。この技術においては、基板上にＧａＮ系化合物半導体を形成する際に、面内で温度分布を生じさせながら形成することで発光層に面内組成分布を生じさせる。発光層としてのＩｎＧａＮやＡｌＩｎＧａＮを形成する際、その組成は温度変化に対して高感度に変化し、組成変化は発光波長の変化を生じさせる。したがって、同一デバイス内で意図的に面内温度分布を生じさせることで発光波長を広範囲に変化させることができ、組成の異なる領域を同時に駆動することで多数の発光ピーク波長が互いに重畳された広帯域スペクトル特性を得ることができる。
【０００４】
ところで、一般に半導体Ｐｎ接合ＬＥＤの動作電圧はその材料のバンドギャップエネルギでほぼ決定され、バンドギャップエネルギが小さい材料ほど動作電圧は低くなる。発光スペクトルもバンドギャップエネルギで決定されるので、赤色ＬＥＤの動作電圧は青色ＬＥＤの動作電圧よりも小さくなる。したがって、面内組成分布によりバンドギャップエネル

ギが面内で変動している領域にわたって電極（透明電極）を形成し駆動した場合、バンドギャップエネルギが小さい領域に流れる電流密度が相対的に大きくなってしまう。このため、発光スペクトルを高精度に調整するためには、電極形成面内での組成変動の程度を高精度に調整する必要が生じるが、製造工程が複雑化するため容易ではない。

【０００５】

本発明は、上記課題に鑑みなされたものであり、その目的は、発光スペクトルが広く、あるいは、発光スペクトルを所望の値に設定することができる発光装置及び製造方法を提供することにある。

【０００６】

【課題を解決するための手段】

上記目的を達成するために、本発明は、窒化ガリウム系化合物半導体装置を製造する方法であって、（ａ）基板面内で温度分布を生じさせるステップと、（ｂ）前記面内分布よりも小さいピッチで前記基板上にモノリシックに複数の窒化ガリウム系化合物半導体を形成するステップと、（ｃ）前記複数の窒化ガリウム系化合物半導体を直列接続するステップを有することを特徴とする。

【０００７】

ここで、前記（ａ）ステップは、（ａ１）前記基板の裏面に不連続的に溝を形成するステップと、（ａ２）前記溝内に膜を形成するステップと、（ａ３）前記基板の裏面側から加熱するステップを有することが好適である。前記膜は、例えばチタン（Ｔｉ）膜とすることができる。

【０００８】

また、前記（ｂ）ステップは、（ｂ１）前記基板上に複数のｎ型ＧａＮ系層を形成するステップと、（ｂ２）前記ｎ型ＧａＮ系層上に$Al_yIn_xGa_{1-x-y}N$（但し、０≦ｘ≦１，０≦ｙ≦１）発光層を形成するステップと、（ｂ３）前記発光層上にＰ型ＧａＮ系層を形成するステップと、（ｂ４）前記ｎ型ＧａＮ系層及びＰ型ＧａＮ系層にそれぞれｎ電極及びＰ電極を接続するステップを有し、前記窒化ガリウム系化合物半導体は発光素子であり、複数の前記発光素子がモノリシックに直列接続されることが好適である。

【０００９】

また、前記（ｂ）ステップにおいて、前記基板上に形成される複数の前記発光素子の密度を不均一とすることが好適である。

【００１０】

また、前記（ｂ）ステップにおいて、前記基板上に形成される前記発光素子の面積を不均一とすることが好適である。

【００１１】

本方法において、さらに、（ｄ）前記発光素子を所定数毎に切り出して発光チップを形成するステップを有することができる。

【００１２】

また、前記温度分布を調整することにより発光チップの発光スペクトルの半値幅を８０ｎｍ以上とすることが好適である。

【００１３】

また、本発明は、窒化ガリウム系化合物半導体を発光素子に用いた発光装置を提供する。この装置は、基板と、前記基板上にモノリシックに直列接続された、前記基板の面内温度分布に起因して各発光素子が異なる組成を有する複数の発光素子を有することを特徴とする。

【００１４】

前記複数の発光素子のピッチは、前記組成の分布のピッチよりも小さいことが好適である。

【００１５】

また、前記複数の発光素子は二次元アレイ状に形成されて同数ずつ２組に分けられ、２個の電極に互いに反対極性となるように並列接続されることが好適である。

【００１６】
また、前記複数の発光素子の発光スペクトルの半値幅は３０ｎｍ以上であり、前記複数の発光素子からの光により励起されて可視光を発光する蛍光体を有することが好適である。
【００１７】
このように、本発明では単に温度分布を形成して発光層を成長させるのではなく、温度分布を形成して発光スペクトルを広帯域化するとともに、複数の発光素子をモノリシックに形成して互いに直列接続する。直列接続することで各発光素子に流れる電流は同一となり、バンドギャップエネルギに高低が生じていてもフラットな発光スペクトルが得られる。
【００１８】
【発明の実施の形態】
以下、図面に基づき本発明の実施形態について説明する。
【００１９】
図１には、本実施形態においてＧａＮ系化合物半導体としてのＬＥＤ１の基本構成が示されている。ＬＥＤ１は、基板１０上に順次ＧａＮ層１２、Ｓｉドープのｎ型ＧａＮ層１４、ＩｎＧａＮ発光層１６、ＡｌＧａＮ層１８、Ｐ型ＧａＮ層２０が積層され、Ｐ型ＧａＮ層２０に接してＰ型電極２２、ｎ型ＧａＮ層１４に接してｎ型電極２４が形成される構成である。
【００２０】
図１に示されたＬＥＤは以下のプロセスにより作製される。すなわち、まず、ＭＯＣＶＤ装置にてサファイアｃ面基板を水素雰囲気中で１１００℃、１０分間熱処理する。そして、温度を５００℃まで降温させ、シランガスとアンモニアガスを１００秒間供給して不連続なＳｉＮ膜を基板１０上に形成する。なお、このプロセスはデバイス中の転位密度を低減させるためのものであり、図ではＳｉＮ膜は省略している。次に、同一温度でトリメチルガリウム及びアンモニアガスを供給してＧａＮ層を２０ｎｍ厚成長させる。温度を１０５０℃に昇温し、再びトリメチルガリウム及びアンモニアガスを供給してアンドープＧａＮ（ｕ－ＧａＮ）層１２及びＳｉドープのｎ型ＧａＮ層１４を各２μｍ厚成長させる。その後、温度を７００℃程度まで降温してＩｎＧａＮ発光層１６を２ｎｍ厚成長させる。目標組成はＸ＝０．１５、すなわち$In_{0.15}Ga_{0.85}N$である。発光層１６成長後、温度を１０００℃まで昇温してＡｌＧａＮ正孔注入層１８を成長させ、さらにＰ型ＧａＮ層２０を成長させる。
【００２１】
Ｐ型ＧａＮ層２０を成長させた後、ウエハをＭＯＣＶＤ装置から取り出し、Ｎｉ１０ｎｍ厚、Ａｕ１０ｎｍ厚を順次真空蒸着で成長層表面に形成する。５％の酸素を含む窒素ガス雰囲気中で５２０℃熱処理することで金属膜はＰ型透明電極２２となる。透明電極形成後、全面にフォトレジストを塗布し、ｎ型電極形成のためのエッチングをフォトレジストをマスクとして行う。エッチング深さは、例えば６００ｎｍ程度である。エッチングで露出したｎ型ＧａＮ層１４上にＴｉ５ｎｍ厚、Ａｌ５ｎｍ厚を形成し、窒素ガス雰囲気中で４５０℃３０分間熱処理してｎ型電極２４を形成する。最後に、基板１０の裏面を１００μｍまで研磨してチップを切り出し、マウントすることでＬＥＤ１が得られる。
【００２２】
$In_{0.15}Ga_{0.85}N$発光層１６の発光ピーク波長は４５０ｎｍ、発光スペクトルの半値幅は約１５～２０ｎｍである。発光ピーク波長は、ＩｎＧａＮの成長温度に敏感で、例えば成長温度が１０℃異なると発光ピーク波長は２０ｎｍ以上変化する。これは、ＩｎＧａＮの成長温度がＩｎＮの蒸発温度（約５００℃）より高いので、$In_XGa_{1-X}N$の組成Ｘが、ＩｎＮの蒸発率とＩｎＧａＮの供給率とのバランスで決定されるからである。具体的には、温度が高いと、ＩｎＮが蒸発してＩｎ組成Ｘは低下し、組成Ｘの低下に伴い発光波長が短波長側にシフトする。
【００２３】
また、温度が低いと、ＩｎＮの蒸発が抑制され、Ｉｎ組成Ｘが増大して発光波長が長波長側にシフトする。

【００２４】
このことは、同一ウエハ面内において温度分布が存在すると、その温度分布に起因して発光ピーク波長が変化することを意味し、逆に、ウエハ面内で意図的に温度分布を生ぜしめることで異なる発光ピーク波長を有する領域を形成できることを意味する。すなわち、温度分布を形成することで複数の発光波長ピークを任意に形成できる。このような原理に基づき、ウエハ内において意図的に温度分布を形成し、これにより発光層１６の組成に分布を生ぜしめて発光ピーク波長を変化させ半値幅を増大させる。

【００２５】
図２には、面内温度分布を生成するための一つの方法が示されている。基板１０の裏面側、すなわちＧａＮ層が形成される表面と反対側に不連続的に膜を形成する。膜は、例えばＧａＮの成長温度よりも高い融点を有し、かつ、アンモニアなどの原料ガスと反応しないＴｉ等を用いることができる。膜の材料としては金属ではなく、半導体あるいは絶縁体を用いることも可能である。図２においては基板１０のある領域にＴｉ膜９が形成されている。サファイア基板１０は絶縁体で透明であり、基板１０の加熱は、ヒータ加熱された基板フォルダに基板１０を接触させて行われる。基板１０の裏面にＴｉ膜９を形成すると、基板フォルダからの放射熱はこのＴｉ膜９により吸収されて基板１０に伝達され、また、基板フォルダとの熱的接触状態が変化することでＴｉ膜９が形成された領域と形成されていない領域とで熱伝導に差が生じ、結果として基板１０に面内温度分布が生じる。従って、Ｔｉ膜９が形成された基板１０を用いて図１に示されるようなＬＥＤ１を形成すると、Ｔｉ膜９が形成された領域と形成されていない領域においてＩｎＧａＮ発光層１６のＩｎ組成Ｘに分布が生じ、発光ピーク波長が異なる領域を同一基板１０上に生成できる。

【００２６】
なお、温度分布が生じるとＩｎＧａＮの成長温度分布が生じ、これにより組成だけでなくＩｎＧａＮ層１６の厚さも変化する。ＩｎＧａＮの発光ピーク波長はその厚さにも依存するため、厳密には、温度分布により組成分布及び層厚分布が生じ、これにより発光ピーク波長がシフトすると云うこともできよう。

【００２７】
図３には、このようにして面内組成分布が生じた発光装置の平面図が示されている。発光装置のサイズは３００×２００μm^2である。図において、斜線部分が基板１０の裏面にＴｉ膜９を形成した領域である。Ｐ型透明電極２２及びｎ型電極２４は、基板１０の裏面にＴｉ膜９が形成された領域と形成されていない領域にわたって共通形成される。Ｐ型透明電極２２の一部（Ｔｉ膜９が形成された領域と形成されていない領域の境界）にワイヤボンディング用のＡｕパッド２６が形成される。両領域の面積比rをr＝（Ｔｉ形成領域面積／Ｔｉ非形成領域面積）とし、面積比rを変化させると発光スペクトルが変化する。２０ｍＡの電流を流したとき、４８２ｎｍと４９９ｎｍに２つのピークを持つスペクトルが得られる。

【００２８】
図４には、r＝１の時の発光スペクトルが示されている。r＝１の時、ピーク強度の比（４８３ｎｍ／５０５ｎｍ）は約１．４である。４８３ｎｍと５０５ｎｍの間では両方のピークの裾が重なるため、４６０～５２０ｎｍの広帯域にわたって発光スペクトルを有する光が得られる。

【００２９】
一方、既に述べたように、面内で組成変化、すなわちバンドギャップエネルギ変化が生じている領域にわたって透明電極２２、２４を形成することで、バンドギャップエネルギが小さい領域に流れる電流密度が相対的に大きくなってしまう。従って、広い発光スペクトルを有し、かつ所望の強度分布を有する発光スペクトルを得るためには、このようにバンドギャップエネルギが面内で分布していてもほぼ同一の電流密度で駆動できるような構成とすることが必要である。そこで、基板１０面内で温度分布を生じさせてＩｎＧａＮ発光層１６を形成するとともに、基板１０上にモノリシックに複数のＬＥＤ１を形成し、これら複数のＬＥＤ１を直列接続する。モノリシックに形成された複数のＬＥＤ１を直列接続

することで、各ＬＥＤ１に供給される電流密度が同一となり、これにより半値幅が約３０ｎｍ以上と広く、所望の発光スペクトルで発光する発光デバイスが得られる。

【００３０】

なお、基板１０に面内温度分布を形成するためには、図２に示されるようにＴｉ膜９を不連続的に基板１０の裏面に形成する他、図５に示されるように基板１０の裏面に不連続的に溝８を形成することによっても達成できる。溝８は、例えば所定の幅及び所定のピッチでストライプ状に形成される。溝８は、ダイヤモンド粒を埋め込んだブレードによりウエハを切断する装置を用いて形成できる。溝８の幅はブレードの厚さで決定され、例えば２００μｍとする。基板１０の裏面に溝８を形成して凹凸を形成することで熱伝導に分布が生じ、これによりＩｎＧａＮの組成分布が生じて発光ピーク波長がシフトする。

【００３１】

さらに、基板１０の裏面に溝８を形成するだけでなく、溝８内に（溝８の底に）Ｔｉ膜９を形成して面内温度分布を生成することもできる。本願出願人は、図６に示されるように溝８を形成し、さらに溝８内にＴｉ膜９を形成することで、より一層効果的に面内温度分布を形成して大きな組成変化を起こさせることができることを確認している。

【００３２】

図７には、基板１０上にモノリシックに形成された２個のＬＥＤ１を互いに直列接続する場合の構成が示されている。なお、図において、ＬＥＤ１の構成は説明の都合上簡略化して示されている。すなわち、図７において、各ＬＥＤ１は、基板１０上にｎ型ＧａＮ層１４、Ｐ型ＧａＮ層２０、Ｐ電極２２、ｎ電極２４を有して構成されている。実際には、図１に示されるようにＩｎＧａＮ発光層１６を有することは云うまでもない。２つのＬＥＤ１は、絶縁基板である基板１０により互いに分離される。ＬＥＤ１同士の分離は、フォトレジストや反応性イオンエッチング、ウエットエッチングを併用することでＬＥＤ１以外の領域を基板１０に達するまでエッチング除去することで達成される。ＬＥＤ１同士はＰ電極２２及びｎ電極２４をエアブリッジ配線２８で接続される。エアブリッジ配線２８を用いることで素子表面に絶縁膜を塗布し、この上に電極を形成してＰ電極２２とｎ電極２４とを電気的に接続する場合に比べ、エッチング溝に沿って電極を配置する必要がなくなるため、配線切れ、あるいは絶縁膜からｎ型ＧａＮ層１４やＰ型ＧａＮ層２０へ絶縁体材料を構成する元素が熱拡散してＬＥＤ１を劣化させる問題を回避できる。エアブリッジ配線２８は、ＬＥＤ１間のみならずＬＥＤ１と図示しない駆動電極との間の接続にも使用される。エアブリッジ配線２８は、例えば以下のようにして形成される。すなわち、全面に２μｍの厚さのフォトレジストを塗布し、エアブリッジ配線の形状に穴を開けた後にポストベークする。その上に、真空蒸着でＴｉを１０ｎｍ、Ａｕを１０ｎｍこの順序で蒸着する。さらにその上の全面に２μｍ厚さでフォトレジストを再度塗布し、エアブリッジ配線を形成する部分のみに穴を開ける。次いで、ＴｉとＡｕを電極として電解液中でイオンプレーティング（メッキ）により電極全面に３～５μｍの厚さのＡｕを付着させる。その後、試料をアセトンに浸し、超音波洗浄によりフォトレジストを溶解除去してエアブリッジ配線２８が完成する。

【００３３】

図８には、図６に示される方法で面内温度分布を生成しＩｎＧａＮ発光層１６のＩｎ組成に分布を生じさせた場合の組成分布と、図７に示されるように基板１０上に複数のＬＥＤ１をモノリシックに形成してエアブリッジ配線２８で直列接続した場合のピッチの関係が示されている。図において、グラフＡは基板ウエハ面内位置に対するＩｎ組成分布を示すものである。図６に示されるように溝８及びＴｉ膜９を周期的に基板１０の裏面に形成することで、Ｉｎ組成も周期的に変動する。組成分布のピッチよりも基板１０上にモノリシックに形成される複数のＬＥＤ１のピッチを小さく設定する。ＬＥＤ１の形成ピッチを小さく設定することで各ＬＥＤ１からの発光ピーク波長が組成分布を反映して異なるものとなり、しかも各ＬＥＤ１に流れる電流が均一であるから、フラットな広帯域発光スペクトルを得ることができる。ＬＥＤ１は基板１０上にモノリシックに複数形成され直列接続されるが、一次元的に形成するのではなく二次元的に形成することも可能である。二次元的

に形成する場合も、組成分布のピッチよりも各ＬＥＤ１の形成ピッチを小さくすることで、ブロードな発光スペクトルを設定できる。

【００８４】

次に、ＬＥＤ１を複数個二次元アレイ状に形成した発光装置について説明する。図９には、基板１０の裏面に溝８及びＴｉ膜９が周期的に形成された平面図が示されている。溝８は、例えば２００μｍ幅、５００μｍピッチで形成される。このようにして周期的に溝８及びその溝８内にＴｉ膜９を形成した上で基板１０を加熱しつつ基板ウエハ上に複数のＬＥＤ１をモノリシックに形成していく。

【００８５】

図１０には、４０個のＬＥＤ１が二次元アレイ状に配列した平面図が示されており、図１１には図１０の回路図、図１２にはその等価回路図が示されている。合計４０個のＬＥＤ１はそれぞれ２０個ずつ２組に分けられ、エアブリッジ配線２８によって直列接続されて２つのＬＥＤ列３０を形成している。これら２つのＬＥＤ列３０は、２個の電極３２に互いに逆極性となるように並列接続される。

【００８６】

２０個のＬＥＤ１を直列接続し、１個のＬＥＤ１当たりの駆動電圧を５Ｖとすると、全体として１００Ｖの駆動電圧となる。これは、商用電源で駆動できるレベルである。ＬＥＤ列３０を２個電極３２に逆極性で配列接続しているので、交流電圧（例えば商用の１００Ｖ、６０Ｈｚ）を印加すると各ＬＥＤ列３０が交互に発光する。このため発光効率を向上できるとともに放熱特性も向上する。

【００８７】

なお、ＬＥＤ１を二次元アレイ状に配置した場合、これを直列接続するためにはエアブリッジ配線２８に交差部分３４が必然的に生じる。エアブリッジ配線２８は図７に示されるようにサファイア基板１０等に接着しておらず、サファイア基板１０から離れて空中を通過するので交差部分３４において エアブリッジ配線２８同士が接触して短絡する事態を回避できる。エアブリッジ配線２８とする利点の一つがここにある。以下に実施例を示す。

【００８８】

【実施例】

厚さ３８０μｍのサファイアｃ面基板の裏面全面にフォトレジストを塗布し、ダイアモンドブレードで幅２００μｍ、ピッチ５００μｍ、深さ１５０μｍの溝を形成した。この面全体にＴｉを真空蒸着で形成し、アセトンの中に浸けるとフォトレジストが溶け、基板裏面の溝の底にＴｉ膜が形成された構造ができた。その後、ＭＯＣＶＤ法にて基板表面にＬＥＤ構造を成長させ、ピッチ１２０μｍ、２０個のＬＥＤを直列に接続したものを並列に接続し、合計４０個のＬＥＤアレイ（チップ）を作製した。全体の大きさは約１ｍｍ×１ｍｍである。このＬＥＤアレイにＤＣ２０ｍＡを流したときの電圧は約７０Ｖ、積分球で測定した発光出力は約６０ｍＷであった。ＤＣ駆動したときは、直列接続された２０個のＬＥＤが交互に点灯するのが確認できた。ＡＣ駆動した場合、４０個全てのＬＥＤが発光した。顕微鏡で発光を観察すると、各チップ毎に発光色が異なることが確認された。発光スペクトルは波長４７０ｎｍ～４９０ｎｍまでほぼフラットな強度を保ち、半値幅は約４６０ｎｍ～５１０ｎｍまでの５０ｎｍであった。肉眼には青緑色に見えた。

【００８９】

また、ＩｎＧａＮ発光層の成長条件を変え、平均Ｉｎ組成を大きくすると波長は長波長側にシフトした。特に、成長温度（基板ホルダ温度）を６５０℃程度まで下げ、各原料ガスの流量と成長圧力を調整するとウエハ面内でＰＬ（フォトルミネセンス）ピーク波長が４７０ｎｍから５８０ｎｍまで変化した。変化の周期は、基板裏面に形成した溝の周期５００μｍと一致していた。このウエハを用いて１ｍｍ角の２０個＋２０個のＬＥＤアレイを作製してその発光を観察した。発光色は肉眼には白色に見えた。

【００４０】

さらに、５００μｍ×５００μｍサイズで２０個のＬＥＤを直列に接続した発光装置では、発光装置の形成位置により同じ白色であってもその色合いは微妙に違って見えた。これ

は、図１８に示されるように、ウエハから５００μｍ×５００μｍの発光装置（チップ）１００を切り出す際に、ウエハの場所によって発光装置（２０個のＬＥＤを含む）内に形成された各波長帯のＬＥＤ個数が変化するためである。すなわち、あるチップは短波長側のＬＥＤの個数が相対的に多くなり、別の場所のチップは長波長側のＬＥＤの個数が相対的に多くなる。このことは、同一のウエハから、異なる発光スペクトルを有するチップを作製できることを意味する。

【００４１】

このように、本実施形態における発光装置は、ＬＥＤのピッチを十分小さくすることで、半値幅が５０ｎｍ以上でフラットな発光スペクトルを有することができ、Ｉｎ組成を調整することで肉眼で白色に見える発光スペクトルが得られる。一般に、白色のＬＥＤを作製するための方法として、（１）Ｒ，Ｇ，Ｂの３原色のＬＥＤを用いる、（２）青色ＬＥＤの上にＹＡＧ（イットリウム・アルミニウム・ガーネット）系の蛍光体を載せて黄色を発光せしめ、蛍光体を通過した青と混ぜることで白色を出す、（３）紫外線ＬＥＤにより３原色を発光する蛍光体を励起して白色を出す、（４）ＬＥＤの活性層に発光色の異なる発光層を重ね、単一のＰｎ接合から全ての発光層に電流注入を行う、等の方法がある。（１）の方法は、３種類のＬＥＤと電源が必要であり、（２）の方法は、互いに補色関係にある２原色により白色を作っているのでその色合いの調整ができないという問題がある。特に、青＋黄色の場合は、赤成分を含まないので暖かみのある色合いが出せない。（３）の方法は原理的に電圧損失が発生し、電力効率が他の方法よりも悪くなる問題がある。また、全ての色を蛍光体で出すので、エネルギ効率がほとんど蛍光体で決定され、励起する紫外線の波長によっては励起効率が悪くなる。また、蛍光体の効率に温度依存性があり、その依存性が色により異なるので周囲温度が変化すると色合いが変化する問題もある。（４）の方法は、Ｐｎ接合の境界面に複数の層を挟み、それらの発光色を変えるというものであるが、Ｐｎ接合に印加する電圧により各層に注入されるキャリア数が変わるので、印加電圧により色が変化してしまう問題がある。また、印加電圧は波長の最も短い層に合わせて決定されるので、電圧損失が生じ、エネルギ効率が悪くなる問題がある。さらに、色合いを調整するのは各発光層の膜厚、組成、層数など多数のパラメータにより決定されるので、再現性を確保するのが困難である。

【００４２】

これに対し、本実施形態の発光装置では、このような問題を生じることなく白色を得ることができる。また、ウエハ面内の組成分布を大きくすれば色合いをさらに自然な色に近づけることが可能である。また、各ＬＥＤはそれぞれ最適な電圧で動作しているため、電圧損失も発生しない。

【００４３】

なお、（２）の方法に関しては、従来では青色ＬＥＤを用いて蛍光体を励起させ、青色と黄色を混合して白色を出しているが、本実施形態の発光装置では上述したように波長４７０ｎｍ～４９０ｎｍまでほぼフラットな強度を保ち、半値幅が約４６０ｎｍ～５１０ｎｍまでの５０ｎｍの青緑色の光を発光することができるため、これを一次光源として用いて（２）の方法を採用することで、色合いの調整が可能となる効果も奏する。すなわち、本実施形態の発光装置上にＹＡＧ系の蛍光体を載せ、発光装置からの青緑色の光によりＹＡＧ系蛍光体を励起させる。

【００４４】

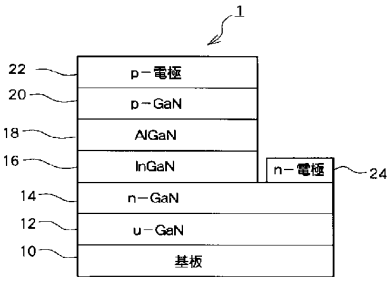
より具体的には、ＬＥＤチップを被覆する樹脂モールド中にＹＡＧ系蛍光体を含有させる。ＹＡＧ系蛍光体を用いた白色ＬＥＤは公知であり、例えば特開平１１－２４３２３２号公報に開示されている。光源として、青色ＬＥＤの代わりに本実施形態の発光装置を用いればよい。青緑色の一次光と蛍光体からの二次光との混合により従来にはない色合いを作成できる。

【００４５】

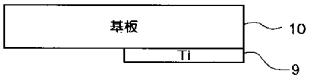
以上、本発明の実施形態について説明したが、本発明はこれに限定されるものではなく種々の変更が可能である。

【００４６】
例えば、本実施形態では発光層としてＩｎＧａＮを用いたが、ＡｌＩｎＧａＮを用いることもでき、一般式ではＡｌｙＩｎｘＧａ１－ｘ－ｙＮ（０≦Ｘ≦１、０≦Ｙ≦１）と表現できる。
【００４７】
また、本実施形態において、同一ウエハ内においてチップを切り出す位置によりそのチップ内に存在する各波長帯域のＬＥＤの個数に相違が生じているが、同一ウエハ内にモノリシックに複数のＬＥＤを形成する際に、より意図的に組成分布に対して不均一にＬＥＤを形成することも可能である。例えば、組成分布は図９に示されるように周期的に形成しつつ、ＬＥＤの形成密度（ＬＥＤ個数）をウエハ位置によって変化させる（ある位置では高密度に形成し、別の位置では低密度に形成する）、あるいはＬＥＤの面積をウエハ位置によって変化させる（ある位置では大面積で形成し、別の位置では小面積で形成する）。これによりチップを切り出すウエハ位置により発光スペクトルが変化する。ＬＥＤ密度（個数）や面積は、組成分布のピッチに応じて設定する。
【００４８】
【発明の効果】
以上説明したように、本発明によれば、発光スペクトルが広く、あるいは、発光スペクトルを所望の値に設定することができる発光装置を得ることができる。
【図面の簡単な説明】
【図１】ＬＥＤの基本構成図である。
【図２】温度分布形成説明図である。
【図３】ＬＥＤの平面図である。
【図４】図３の発光スペクトル説明図である。
【図５】他の温度分布形成説明図である。
【図６】さらに他の温度分布形成説明図である。
【図７】ＬＥＤの直列接続説明図である。
【図８】ＬＥＤアレイのピッチと組成分布との関係を示す説明図である。
【図９】溝の形成ピッチを示す説明図である。
【図１０】二次元ＬＥＤアレイの配置説明図である。
【図１１】図１０の回路図である。
【図１２】図１０の等価回路図である。
【図１３】ウエハ内の形成位置説明図である。
【符号の説明】
１０　基板（ウエハ）、１２　ｕ－ＧａＮ層、１４　ｎ型ＧａＮ層、１６　ＩｎＧａＮ発光層、１８　ＡｌＧａＮ層、２０　Ｐ－ＧａＮ層、２２　Ｐ－電極、２４　ｎ－電極。

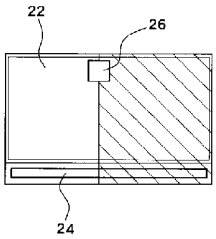
【図１】



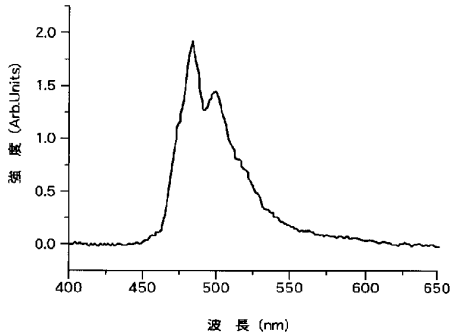
【図２】



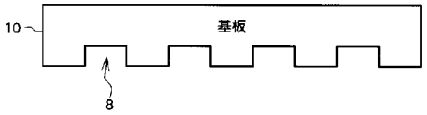
【図３】



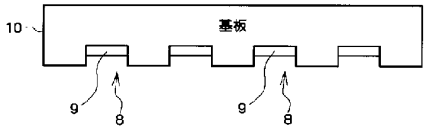
【図４】



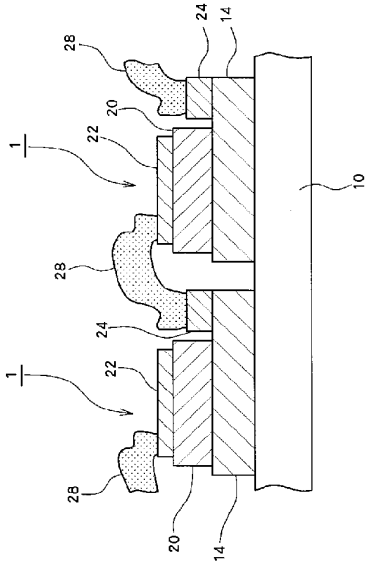
【図５】



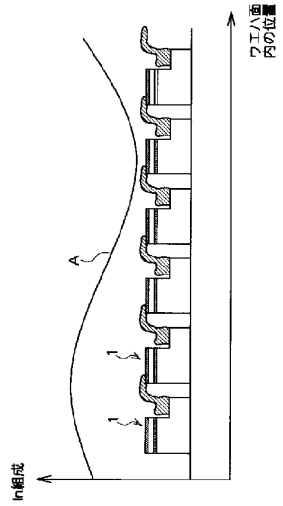
【図６】



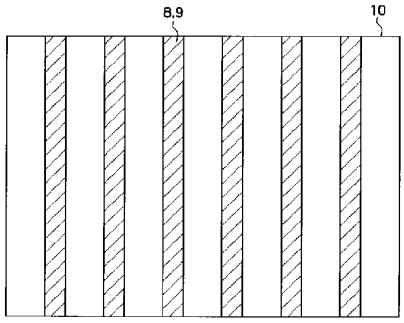
【図７】



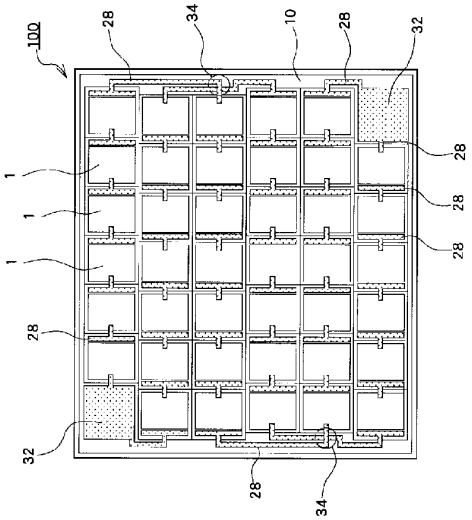
【図８】



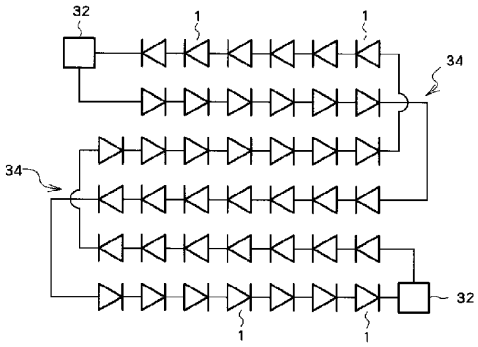
【図９】



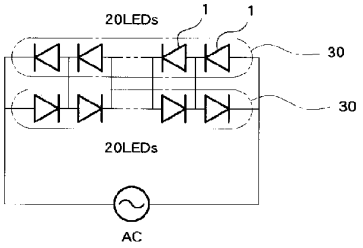
【図１０】



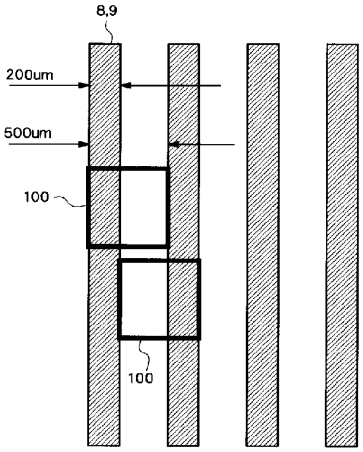
【図１１】



【図１２】



【図１３】



フロントページの続き

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(54) Semiconductor LED Device and method for manufacturing the same

Abstract

The present invention relates to an LED device. The LED device includes a pumping layer having a superior light emission efficiency due to hetero-junction multilayer, and an activation layer of homo-junction multilayer capable of converting a received light to a light having desirable wavelength due to smaller band gap. Accordingly, light is generated in the pumping layer of AlGaInN in which small amount of In is included, incident into the activation layer in which large amount of In is included, and then emitted, so that a blue shift caused by a current is reduced and efficiency is increased. Further, a single LED can emit lights having more than two wavelengths and therefore various lights can be obtained from a single device. Since the device can be manufactured by a single continuous growth process, reproducibility and productivity of the device are improved. In addition, phosphor material which reduces efficiency while generating white light is not employed so that efficiency can be increased. Since the device can be mounted using a bump, the mounting process is simplified.

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(54) 반도체 엘이디 소자 및 그 제조방법

요약

본 발명은 반도체 LED 소자에 관한 것으로서, 특히 이종 접합된 다층에 의해 발광효율이 우수한 펌핑층과 그보다 밴드갭이 적어 수광된 빛을 모두 원하는 파장의 빛으로 전환시킬 수 있는 동종접합의 다층으로된 활성층을 구비하였으므로, In 양이 적은 AlGaInN 재질의 펌핑층에서 광을 생성하고, 이를 얻고자하는 In 양이 많은 활성층에 입사시켜, 빛을 방출하게 하여 전류에 의한 단파장화(blue shift)를 감소시켜 효율을 향상시키고, 하나의 LED 소자에서 두 개 이상의 파장을 갖는 빛의 방출이 가능하여 다양한 파장의 빛을 하나의 소자에서 얻을 수 있으며, 연속되는 한번의 성장 공정으로 소자를 형성하므로 소자의 재현성이 우수하며 양산성이 향상되며, 백색광을 형성할 때 효율이 저하되는 형광물질을 사용하지 않아 효율이 증가되고, 범프를 이용한 실장이 가능하여 실장 공정이 간단하다.

대표도

도2

명세서

도면의 간단한 설명

도 1은 종래 기술에 따른 LED 소자의 단면도.

도 2는 본 발명에 따른 LED 소자의 단면도.

도 3a 내지 도 3e는 본 발명에 따른 LED 소자의 제조 공정도.

도 4는 도 2의 LED 소자의 실장 단면도.

< 도면의 주요 부분에 대한 부호의 설명 >

10,20,30 : 기판11,21,31 : 버퍼층

12,22,24,32 : n형 AlGaInN층13,23,33 : 활성층

14,26,36 : p형 AlGaInN층15 : 투명전극

16,29,39 : n형 전극17,27,37 : p형 전극

25,35 : 펌핑층28,43 : 절연막

41 : 하부배선42 : 실리콘 기판

44 : p형 배선45,47 : 범프

46 : n형 배선50 : 반도체 LED 소자

발명의 상세한 설명

발명의 목적

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발명이 속하는 기술분야 및 그 분야의 종래기술

본 발명은 반도체 엘이디(light emitting diode: 이하 LED라 칭함) 소자 및 그 제조방법에 관한 것으로서, 특히 AlGaInN계 LED로서 전류와 빛 변환 효율이 높은 펌핑(pumping)층을 이용하여, 원하는 파장의 빛을 방출하는 활성층에 빛을 펌핑(pumping) 하여 활성층에서 파장 변환을 하여 하나의 소자 내에서 파장 변환된 단색의 LED 소자를 구현할 수 있고, 펌핑층의 일부를 이용하여, 한 소자 내에서 두 파장을 혼합하여 백색광을 구현할 수 있는 반도체 LED 소자에 관한 것이다.

일반적으로 화합물 반도체소자는 금속-반도체 전계효과 트랜지스터(metal semiconductor field effect transistor) 및 고전자 이동도 트랜지스터(high electron mobility transistor; HEMT)등의 스위칭 소자와 반도체 레이저(LASER; light amplification by stimulated emission of radition) 및 광다이오드 등과 같은 광소자 및 PD가 사용되고 있다.

상기 레이저는 단일 파장으로서, 직진성이 뛰어나 정보통신을 위한 효과적인 송신 수단으로서 주목받고 있으며, 그중 반도체 레이저는 다른 레이저에 비해 구동 전류가 작고, 소형이며, 전류의 변화에 따라 빛의 세기 및 주파수를 직접 변조 할 수 있고, 레이저의 효율이 통상 70% 이상으로 매우 높으며, 광범위한 파장 영역을 갖는 등의 이점이 있어 레이저 프린터, 바코드 리더 등과 같은 사무용 기기나 광통신 기기 등에서 널리 사용되고 있다.

도 1은 종래 기술에 따른 LED 소자의 단면도로서, 절연기판을 사용하고, AlGaInN LED 소자에서 Al과 In이 포함되지 않은 경우의 예이다.

먼저, 절연성 투광 재질의 기판(10) 상에 버퍼층(11), n형 GaN층(12), GaN(또는 InGaN) 활성층(13), p형 GaN층(14) 및 투명전극(15)이 순차적으로 적층 되어 있으며, 상기 투명전극(15)의 일측 상부에는 금속재질의 p형 전극(17)이 형성되어있고, 기판(10) 타측의 투명전극(15)과 p형 GaN층(14), GaN 활성층(13) 및 n형 GaN층(12)의 일부 두께가 제거되고 노출된 n형 GaN층(12)의 상부에 금속재질의 n형 전극(16)이 형성되어있다.

상기와 같은 일반적인 화합물 반도체 광소자의 원리는 p형 금속전극을 통해 들어오는 정공과 n형 금속전극을 통해 들어오는 전자가 단층 또는 다층의 활성층에서 결합하여 활성층 물질 조성의 밴드갭(bandgap)에 해당하는 빛을 방출하는 구조이다. 이렇게 활성층에서 방출된 빛은 활성층의 윗면과 아랫면으로 대부분 방출되게 되는데, AlGaInN계 LED의 경우 활성층의 상층부는 투명 전극을, 하층부는 기판이 빛에 대하여 투명하기 때문에 이러한 동작이 가능하다.

일반적으로 LED의 출력과 파장등 중요한 특성은 활성층에서 결정되며 그만큼 활성층의 결정질 구조 조성이 매우 중요하게 된다.

종래의 AlGaInN계 LED 구조는 반도체 소자에서는 단 한 개 파장의 빛이 활성층으로부터 방출하므로, 여러 가지 색을 얻기 위해서는 형광 물질을 사용하거나 서로 다른 종류의 LED를 구비하여야하는 등의 문제점이 있다.

또한 전구나, 디스플레이의 백 라이트(back light) 광원 등을 대체할 수 있는 백색 LED는 다양한 용도로 사용이 가능하지만, 상기 백색광 LED는 LED 방사 파장의 보색광을 내는 형광체를 사용하는 패키지로 형성하여야하는데, 이러한 형광물질의 신뢰성이 LED 소자에 비해 떨어져 장시간 사용함에 따라 변색이 일어나거나, 발광 효율이 저하되는 다른 문제점이 있다.

발명이 이루고자 하는 기술적 과제

본 발명은 상기와 같은 문제점들을 해결하기 위하여 것으로서, 본 발명의 목적은 고출력이 가능한 펌핑층을 소자 내부에 구비시켜 펌핑층으로부터 발생한 빛을 활성층에 흡수시켜 이 흡수된 빛이 활성층에서 다시 재결합하여, 얻고자 하는 LED 파장의 빛을 효율적으로 얻을 수 있는 반도체 LED 소자를 제공함에 있다.

발명의 구성 및 작용

상기와 같은 목적을 달성하기 위한 본 발명에 따른 반도체 LED 소자의 특징은,

AlGaInN 계 LED 소자에 있어서,

절연성 투광재질의 기판상에 형성되어있는 제1도전형 $Al_{x1}Ga_{y1}In_{z1}N$층 (x1+y1+z1=1)과,

상기 제1도전형 $Al_{x1}Ga_{y1}In_{z1}N$층의 일측 상에 순차적으로 형성되어있는 활성층 패턴과 펌핑층 패턴과 제2도전형 AlGaInN층 패턴 및 제2도전형 전극을 구비하되, 상기 활성층은 1개 이상의 등종접합의 단층 또는 다층의 $Al_xGa_yIn_zN$ / $Al_{x1}Ga_{y1}In_{z1}N$ 재질이고, 상기 펌핑층은 이종접합의 단층 또는 다층의 $Al_xGa_yIn_zN$ / $Al_{x1}Ga_{y1}In_{z1}N$ 재질이며, 펌핑층을 활성층과 함께 적어도 하나씩 구비하여 수직으로 집적되어 LED 소자를 구성하되 활성층의 $Al_xGa_yIn_zN$ 의 밴드갭이 펌핑층의 $Al_aGa_bIn_cN$ 의 밴드갭 보다 적게 형성되어있고,

상기 제1도전형 $Al_{x1}Ga_{y1}In_{z1}N$층의 타측에 형성되있는 제1도전형 전극을 구비함에 있다.

또한 상기 기판이 알루미나, 사파이어 또는 석영으로 형성되며, 상기 활성층 패턴과 펌핑층 패턴과 제2도전형 AlGaInN층 패턴의 측벽이 10~80° 의 경사각을 가지도록 형성되어있어 측벽에서 반사된 광이 기판 쪽으로 반사되도록하는 것을 특징으로 한다.

또한 상기의 반도체 LED 소자를 실장하되, 실리콘 기판의 일측에 형성된 제2도전형 배선이 상기 LED 소자의 제2도전형 전극과 범프를 통하여 연결되고, 실리콘 기판의 타측에 절연막이 개재된 상태로 형성되어있

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는 제1도전형 배선은 LED 소자의 제1도전형 배선과 범프를 통하여 연결되어 있는 것을 특징으로 한다.

또한 본 발명에 따른 반도체 LED 소자 제조방법의 특징은,

절연성 투광재질의 기판상에 제1도전형 $Al_xGa_yIn_zN$층, 동일 도전형의 $AlGaInN$층 / $Al_xGa_yIn_zN$ 재질이 반복적층된 다층또는 단층의 활성층, 제1도전형 $AlGaInN$층, 이종접합의 $Al_aGa_bIn_cN$ / $Al_xGa_{b-1}In_cN$ 재질이 반복적층된 펌핑층, 제2도전형 $AlGaInN$층을 순차적으로 형성하는 공정과,

상기 제2도전형 $AlGaInN$층에서 활성층까지를 순차적으로 선택 식각하여 각 패턴들을 형성하고 제1도전형 $Al_xGa_yIn_zN$층의 일측을 노출시키는 공정과,

상기 제2도전형 $AlGaInN$층상에 제2도전형 전극을 형성하는 공정과,

상기 패턴들의 측면에 절연막을 형성하는 공정과,

상기 노출된 제1도전형 $Al_xGa_yIn_zN$층과 접촉되는 제1도전형 전극을 형성하는 공정을 구비함에 있다.

또한 상기 제1도전형 $Al_xGa_yIn_zN$층, 활성층, 펌핑층 및 제2도전형 $AlGaInN$층은 MOCVD, MBE 및 VPA 중 하나의 방법으로 형성되고, 상기 제2도전형 $AlGaInN$층에서 활성층까지의 식각 공정을 경사식각 공정으로 실시하여 측벽이 경사각을 갖도록하여 측벽에서 반사되는 광이 기판을 반사되도록하는 것을 특징으로 한다.

이하, 본 발명에 따른 반도체 LED 소자 및 그 제조방법에 관하여 첨부 도면들을 참조하여 상세히 설명한다.

본 발명의 기본 원리를 살펴보면 다음과 같다.

먼저, 일반적인 $AlGaInN$ 계 광소자는 활성층에 In 양이 많이 들어갈수록 효율이 감소하는 특성이 있다. 보통 InO| 약 35% 들어가는 $InGaN$ 활성층의 파장은 약 470nm인데 이 경우 출력은 소자의 구조에 따라 약 3~5mW이다. 반면 InO| 약 5% 들어가는 380nm 혹은 InO| 약 22% 들어가는 430nm 파장의 활성층의 경우에는 동일한 구조에서도 출력이 약 10mW를 쉽게 상회한다. 이것은 활성층의 In량이 증가할수록 결정의 질이 악화되며 효율이 급격히 저하되는 특성이 있기 때문이다. 또한 In 양이 증가하면, 이 활성층에 전류가 주입되어 빛으로 변환되는 과정에서 파장이 짧은 쪽으로 옮겨지는 (blue shift) 현상이 증가하며 효율이 더욱 악화된다.

본 발명의 새로운 구조는 In 조성이 적은 양질의 펌핑층의 장점과 In 조성 높은 활성층 특히 전류에 의한 재결합 방출이 아니라, 빛의 흡수를 그대로 빛으로 전환시키는 활성층의 장점을 이용하는 것이다. 따라서, 얻고자 하는 빛의 파장을 종래의 p-n 구조에서가 아니고, 동일 도전형(conductive type), 예를 들면 n-n 활성층으로부터 얻을 수 있다.

이 원리를 의해 효율이 좋은 단 파장, 예를 들면 380~430nm 파장의 빛을 발광하는 펌핑층을 이용하여 효율이 좋지 않은 470nm(청색), 525nm(녹색), 635nm(적색)의 빛으로 쉽게 변환할 수 있다.

또한 이 원리를 이용하면 한 개의 LED 소자에서 한 개 이상의 파장을 가지는 빛을 얻을 수 있고, 이런 두 개 이상 파장의 빛의 적절한 혼합으로 새로운 색 파장의 빛을 얻을 수 있다. 예를 들면 펌핑층에서 발생된 깊은 청색(~450 nm) 파장의 빛이 활성층에 흡수되어, 이 색과 보색 관계인 황색(590nm) 빛을 낼 때 활성층의 두께와 활성층의 적층수를 조절하여, 깊은 청색(~450nm) 파장 빛의 활성층에서의 흡수량과 투과량 등을 조절하여 흰색의 빛을 얻을 수가 있다.

또 다른 방법으로 펌핑층의 빛을 일부분 방출시키고, 활성층의 빛과 혼합하여도 2 개 파장의 빛을 얻을 수도 있다.

이와 같은 다파장 LED는 형광 물질을 사용하지 않아 소자의 신뢰성이 혁신적으로 향상되며, 또한 한번의 에피성장 과정에서 얻어진 에피웨이퍼를 기존의 청색 LED 공정을 그대로 적용하여 제작이 가능하여 공정이 간단해지고, 소자 특성의 균일성이 우수하여 양산성이 향상된다.

이러한 반도체 LED 소자는 LED의 파장과 출력을 결정하는 활성층과, 상기 활성층에 에너지를 공급하는 펌핑층을 수직으로 배치시켜 펌핑층에서 발생한 빛을 모두 활성층에서 흡수되도록한다.

도 2는 본 발명에 따른 반도체 LED 소자의 단면도로서, n-n형 등종 접합 활성층과 펌핑층이 수직으로 집적된 예이다.

먼저, 알루미나, 사파이어 또는 석영 등의 절연성 투광재질의 기판(20)상에 버퍼층(21)과 n형 $Al_xGa_yIn_z$ N층(22, x1+y1+z1=1)이 형성되어있고, 상기 n형 $Al_xGa_yIn_z$ N층(22) 상에 $AlGaIn$ N / $Al_xGa_{1-x}In_zN$ 재질이 반복적층된 다층의 활성층(23) 패턴과, n형 $AlGaInN$층(24) 패턴과, $Al_aGa_bIn_cN$ / $Al_xGa_{b-1}In_cN$ 재질이 반복적층된 다층의 펌핑층(25) 패턴과, p형 $AlGaInN$층(26) 패턴과, p형 전극(27) 패턴이 순차적으로 적층되어있다. 여기서 상기 활성층(23) 패턴과, n형 $AlGaInN$층(24) 패턴과, $Al_aGa_bIn_cN$ / $Al_xGa_{b-1}In_cN$ 재질이 반복적층된 다층의 펌핑층(25) 패턴과, p형 $AlGaInN$층(26) 패턴의 측벽은 10~89。의 경사각을 가지고 있어 측면으로 방출되는 빛이 식각된 측면에서 반사되어 용이하게 기판으로 향하게 경사식각되어 있으며, 상기 n형 $AlGaInN$층(24) 패턴을 필요에 따라 제거될 수도 있다.

또한 상기 활성층(23)에서 p형 전극(27) 패턴까지의 측벽에 측면 보호를 위하여 투명 절연막(28)이 형성되어있고, 상기 n형 $Al_xGa_yIn_zN$층(22)과 접촉되는 n형 전극(29)이 형성되어있다.

상기 p형 및 n형 전극(27,29)은 불투명한 금속재질로 형성하여 기판(20)으로 빛을 반사시킨다.

상기에서 활성층(23)과 펌핑층(25)은 밴드갭이 다른 서로 다른 조성을 가지는 두개의 층이 반복적층되어 있는 층들로서 도 2에서는 편의상 단일층으로 도시되어있으며, 상기 활성층(23)은 조성은 다르나 도전형

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이 같은 n-n 또는 p-p형의 $Al_xGa_yIn_zN$ / $Al_{x1}Ga_{y1}In_{z1}N$ 두층이 반복 적층되어있는 구조로서, x+y+z=1과 x1+y1+z1=1을 만족시키며, 활성층 역할의 $Al_xGa_yIn_zN$ 층의 밴드갭(Eg($Al_xGa_yIn_zN$))이 베리어층 $Al_{x1}Ga_{y1}In_{z1}N$의 밴드갭(Eg($Al_{x1}Ga_{y1}In_{z1}N$) 보다 작고, 또한 상기 펌핑층(25)은 p-n 구조의 $Al_xGa_yIn_zN$ / $Al_{x2}Ga_{y2}In_{z2}N$ 재질이 반복적층되어 있으며, 펌핑 역할을 하는 $Al_xGa_yIn_zN$ 층의 밴드갭(Eg($Al_xGa_yIn_zN$))이 활성층(23)의 밴드갭(Eg($Al_xGa_yIn_zN$)) 보다 크고, In량도 적다.

이와 같이 형성된 반도체 LED 소자의 동작 원리는, 우선 두 개의 전극으로부터 공급되는 전류에 의해 p형 AlGaInN층(26) 패턴을 통해 들어온 정공이 펌핑층(25)에 제한되고, n형 $Al_{x1}Ga_{y1}In_{z1}N$층(22)을 통해 들어온 전자도 펌핑층(25)에 제한되어 전자와 정공이 결합하면서 펌핑층(25)의 밴드갭(Eg(펌핑층))에 해당하는 에너지의 빛을 방출하며, 펌핑층(25)에서 하부로 방출된 빛은 그대로 활성층(23)에 흡수되고, 펌핑층(25)의 상부로 방출된 빛은 p형 전극(27)에서 반사되어 활성층(23)에 흡수된다.

그 다음 이렇게 흡수된 빛은 활성층(23)에서 전자와 정공으로 변환되고 활성층(23)의 베리어층에 의해 제한되어 있다가 활성층(23)에서 다시 결합하여 활성층(33)의 밴드갭(Eg(활성층))에 해당하는 빛을 방출하게 된다. 이런 빛은 LED 구조에서 에너지가 가장 작은 빛으로 더 이상 어느 층에도 흡수되지 않고 기판을 통해 전부 방출시킬 수 있다. 상기 n-p형은 서로 바꿀수도 있다.

도 3a 내지 도 3e는 본 발명에 따른 반도체 LED 소자의 제조공정도이다.

먼저, 알루미나, 사파이어 또는 석영 등의 절연성 투광재질의 기판(30)상에 버퍼층(31)과 n형 $Al_{x1}Ga_{y1}In_{z1}N$층(32), 동일 도전형의 $Al_xGa_yIn_zN$ / $Al_{x1}Ga_{y1}In_{z1}N$ 재질이 반복적층된 다층의 활성층(33), n형 AlGaInN층(34), 반대 도전형의 $Al_xGa_yIn_zN$ / $Al_{x2}Ga_{y2}In_{z2}N$ 재질이 반복적층된 펌핑층(35), p형 AlGaInN층(36)을 순차적으로 형성한다. 상기 층들은 유기금속화학기상증착(Metal-Organic Chemical Vapor Deposition; 이하 MOCVD라 칭함)나 분자빔에피택시(molecular beam epitaxy; 이하 MBE라 칭함)나 기상에피택시(vapor phase epitaxy; 이하 VPA라 칭함) 등의 방법을 사용할 수 있다. (도 3a 참조).

그 다음 패턴닝 마스크(도시되지 않음)를 사용하여 상기 p형 AlGaInN층(36)에서 활성층(33)까지를 순차적으로 선택 식각하여 패턴들을 형성한다. 이때 상기 n형 $Al_{x1}Ga_{y1}In_{z1}N$층(32)의 일부 두께가 식각된다. 이때 상기 p형 AlGaInN층(36)에서 활성층(33)까지의 식각을 경사식각으로하여 측벽이 경사각을 가지고 형성되도록하여 측벽에서 반사된 광이 기판쪽으로 반사되도록한다. (도 3b 참조).

그후, 상기 p형 AlGaInN층(36)상에 빛을 반사시키는 p형 전극(37)을 형성하고, (도 3c 참조), 상기 구조의 전표면에 패턴들의 측면 보호를 위한 절연막(38)을 형성한 후, 이를 패턴닝하여 n형 $Al_{x1}Ga_{y1}In_{z1}N$층(32)을 노출시킨다. 이때 후속 도전선 연결을 위하여 상기 p형 전극(37)도 노출시킨다. (도 3d 참조).

그 다음 상기 노출되어있는 n형 $Al_{x1}Ga_{y1}In_{z1}N$층(32)과 접촉되는 n형 전극(39)을 형성한다. (도 3e 참조).

상기에서 n-p형은 서로 바꿀수도 있다.

도 4는 도 2의 반도체 LED 소자가 실리콘 기판에 실장되어있는 상태의 단면도로서, 실리콘 기판(42)의 상부면에 절연막(43)이 형성되어있고, 상기 절연막(43)의 일측이 제거되어 노출된 실리콘기판(42)상에 옴믹 접촉되는 p형 배선(44)이 형성되어 있으며, 상기 절연막(43)의 타측 상부에는 n형 배선(45)이 형성되어있고, 상기 반도체 LED 소자(50)의 p형 전극과 n형 전극이 각각 범프(45, 47)를 통하여 배선들(44,46)과 연결되어있으며, 상기 실리콘기판(42)의 하부면에는 기판전압을 인가하는 옴믹 접촉된 하부 배선(41)이 형성되어있다. 상기의 실장 어레이는 n형 배선(44) 만이 와이어 본딩되고 하부 배선은 직접 전압과 연결되어 와이어 본딩 수를 줄일 수 있다.

발명의 효과

이상에서 설명한 바와 같이 본 발명에 따른 반도체 LED 소자는 이중 접합된 다층에 의해 발광효율이 우수한 펌핑층과 그보다 밴드갭이 작아 수광된 빛을 모두 원하는 파장의 빛으로 전환시킬 수 있는 동종접합의 다층으로된 활성층을 구비하였으므로, In 양이 적은 AlGaInN 재질의 펌핑층에서 광을 생성하고, 이를 얻고자하는 In 양이 많은 활성층에 입사시켜, 빛을 방출하게 하여 전류에 의한 단파장화(blue shift)를 감소시켜 효율을 향상시키고, 하나의 LED 소자에서 두 개 이상의 파장을 갖는 빛의 방출이 가능하며 다양한 파장의 빛을 하나의 소자에서 얻을 수 있으며, 연속되는 한번의 성장 공정으로 소자를 형성하므로 소자의 재현성이 우수하며 양산성이 향상되며, 백색광을 형성할 때 효율이 저하되는 형광물질을 사용하지 않아 효율이 증가되는 이점이 있다.

또한, 활성층에서의 흡수율을 활성층의 두께 및 수를 조절하여 높임으로써 펌핑층이 활성층의 파장으로 모두 변환된 단파장 단색 LED도 구현이 가능하며, 범프를 이용한 실장이 가능하며 실장 공정이 간단하다.

(57) 청구의 범위

청구항 1

AlGaInN 계 LED 소자에 있어서,

절연성 투광재질의 기판상에 형성되어있는 제1도전형 $Al_{x1}Ga_{y1}In_{z1}N$층 (x1+y1+z1=1)과,

상기 제1도전형 $Al_{x1}Ga_{y1}In_{z1}N$층의 일측 상에 순차적으로 형성되어있는 활성층 패턴과 펌핑층 패턴과 제2도전형 AlGaInN층 패턴 및 제2도전형 전극을 구비하되, 상기 활성층을 1개 이상의 동종접합의 단층 또는 다층의 $Al_xGa_yIn_zN$ / $Al_{x1}Ga_{y1}In_{z1}N$ 재질이고, 상기 펌핑층은 이종접합의 단층 또는 다층의 $Al_xGa_yIn_zN$ / $Al_{x2}Ga_{y2}In_{z2}N$ 재질이며, 펌핑층을 활성층과 함께 적어도 하나씩 구비하여 수직으로 적적되어 LED 소자를

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구성하되 활성층의 $Al_xGa_yIn_zN$ 의 밴드갭이 펌핑층의 $Al_aGa_bIn_cN$ 의 밴드갭 보다 적게 형성되어있고,

상기 제1도전형 $Al_xGa_yIn_zN$층의 타측에 형성되있는 제1도전형 전극을 구비하는 것을 특징으로하는 반도체 LED 소자.

청구항 2

제 1 항에 있어서,

상기 제1 및 제2도전형은 n 및 p형인 것을 특징으로하는 반도체 LED 소자.

청구항 3

제 1 항에 있어서,

상기 기판이 알루미나, 사파이어 및 석영으로 이루어지는 군에서 임의로 선택되는 하나의 재질인 것을 특징으로 하는 반도체 LED 소자.

청구항 4

제 1 항에 있어서,

상기 활성층 패턴과 펌핑층 패턴과 제2도전형 AlGaInN층 패턴의 측벽이 10~89。 의 경사각을 가지도록 형성되어있어 측벽에서 반사된 광이 기판쪽으로 반사되도록하는 것을 특징으로 하는 반도체 LED 소자.

청구항 5

제 1 항의 반도체 LED 소자를 실장하되, 실리콘 기판의 일측에 형성된 제2도전형 배선이 상기 LED 소자의 제2도전형 전극과 범프를 통하여 연결되고, 실리콘 기판의 타측에 절연막이 게제된 상태로 형성되어있는 제1도전형 배선은 LED 소자의 제1도전형 배선과 범프를 통하여 연결되어 있는 것을 특징으로 하는 반도체 LED 소자의 어레이.

청구항 6

절연성 투광재질의 기판상에 제1도전형 $Al_xGa_yIn_zN$층, 동일 도전형의 $Al_xGa_yIn_zN$ / $Al_xGa_yIn_zN$ 재질이 반복적층된 다층또는 단층의 활성층, 제1도전형 AlGaInN층, 이종접합의 $Al_aGa_bIn_cN$ / $Al_xGa_{1-x}In_yN$ 재질이 반복적층된 펌핑층, 제2도전형 AlGaInN층을 순차적으로 형성하는 공정과,

상기 제2도전형 AlGaInN층에서 활성층까지를 순차적으로 선택 식각하여 각 패턴들을 형성하고 제1도전형 $Al_xGa_yIn_zN$층의 일측을 노출시키는 공정과,

상기 제2도전형 AlGaInN층상에 제2도전형 전극을 형성하는 공정과,

상기 패턴들의 측면에 절연막을 형성하는 공정과,

상기 노출된 제1도전형 $Al_xGa_yIn_zN$층과 접촉되는 제1도전형 전극을 형성하는 공정을 구비하는 반도체 LED 소자의 제조방법.

청구항 7

제 6 항에 있어서,

상기 제1 및 제2 도전형은 각각 n및 p형인 것을 특징으로하는 반도체 LED 소자의 제조방법.

청구항 8

제 6 항에 있어서,

상기 제1도전형 $Al_xGa_yIn_zN$층, 활성층, 펌핑층 및 제2도전형 AlGaInN층은 MOCVD, MBE 및 VPA 중 하나의 방법으로 형성되는 것을 특징으로 하는 반도체 LED 소자의 제조방법.

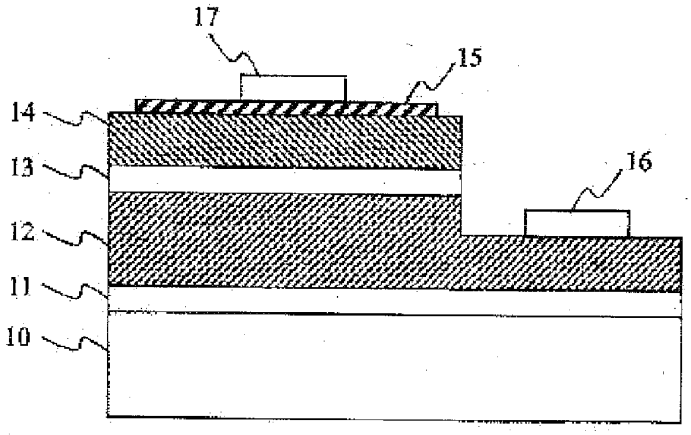
청구항 9

제 6 항에 있어서,

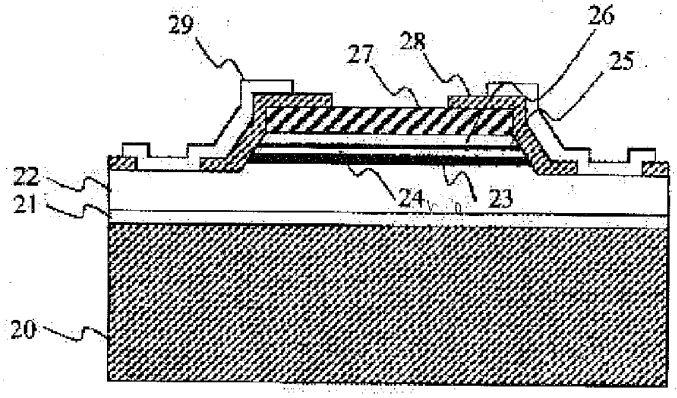
상기 제2도전형 AlGaInN층에서 활성층까지의 식각 공정을 경사식각 공정으로 실시하여 측벽이 경사각을 갖도록하여 측벽에서 반사되는 광이 기판을 반사되도록하는 것을 특징으로 하는 반도체 LED 소자의 제조방법.

도면

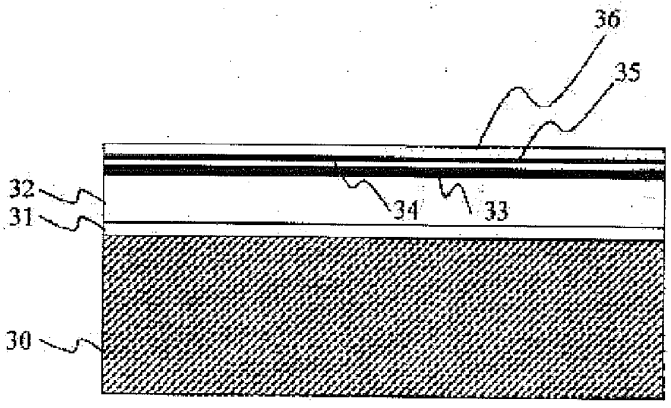
도면1


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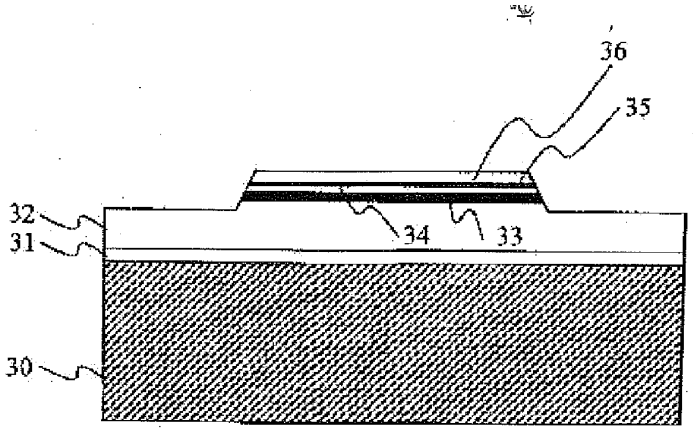
도면2


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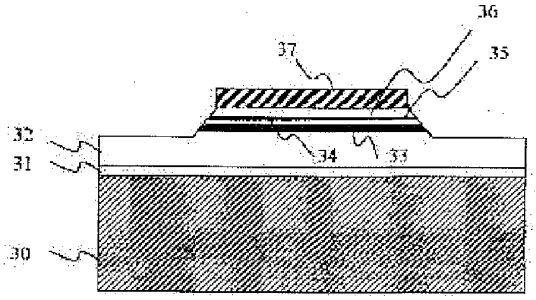
도면3a


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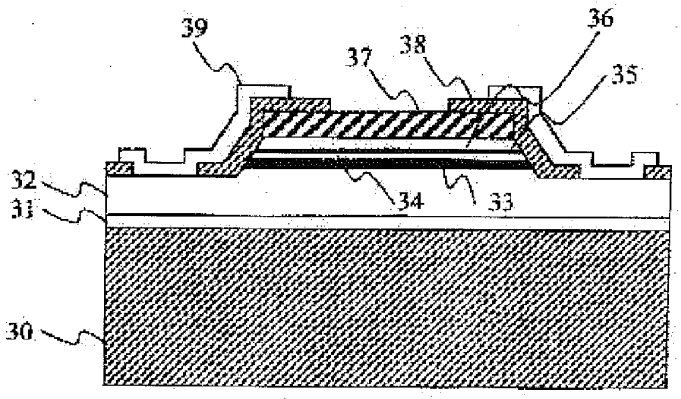
도면3b



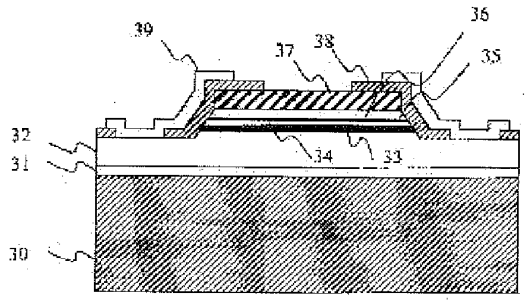
도면3c



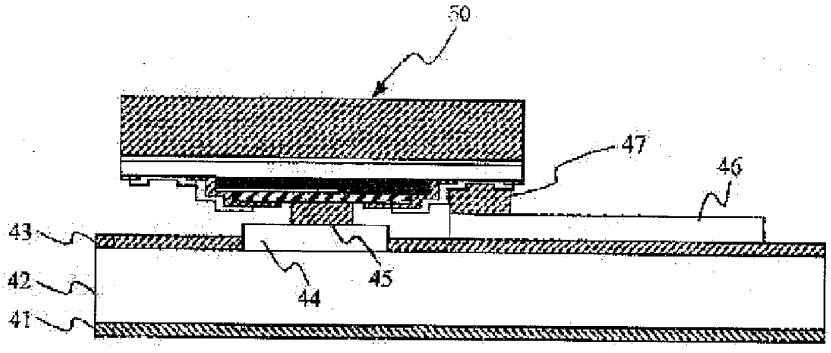
도면3d



도면3a



도면4



상세보기

마이폴더저장 마이폴더보기

(54) **LIGHT-EMITTING DEVICE HAVING LIGHT-EMITTING ELEMENTS**
DISPOSITIF ELECTROLUMINESCENT COMPRENANT DES ELEMENTS ELECTROLUMINESCENTS

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- (11) 특허번호 (Publication Number) : **WO04/023568** (2004.03.18)
- (13) 문헌종류 (Kind of Document) : A1 (PUBL.OF THE INT.APPL. WITH INT.SEARCH REPORT)
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- (75) 발명자 (Inventor) : SAKAI SHIRO
  AO JIN-PING
  ONO YASUO
- (73) 출원인 (Assignee) : SAKAI SHIRO
  NITRIDE SEMICONDUCTORS CO LTD
  AO JIN-PING
  ONO YASUO
- (57) 요약 (Abstract) :

A light-emitting device operating on a high drive voltage and a small (1) are two-dimensionally formed on an insulating substrate (10) monolithically and connected in series to form an LED array. Two s connected to electrodes (32) in inverse parallel. Air-bridge wiri between the LEDs (1) and between the LEDs (1) and electrodes (3 are arranged zigzag to form a plurality of LEDs (1) to produce a high small drive current. Two LED arrays are connected in inverse paralle AC power supply can be used as the power supply.$L'invention co électroluminescent fonctionnant avec une tension de commande courant de commande. Des DEL (1) sont formées de manière monolithiquement sur un substrat isolant (10), tel que du saphir, et c de sorte ?former un réseau de DEL. Deux de ces réseaux de DEL s électrodes (32) en parallèle inverse. Un câblage de pont aérien (28 DEL (1) et entre les DEL (1) et les électrodes (32). Les réseaux de D zigzag de manière ?former une pluralit?de DEL (1) permettant de p de commande élevée et un faible courant de commande. Deux ré connectés en parallèle inverse, une alimentation CA pouvant ê alimentation électrique.

- (51) 국제특허분류 (IPC) : H01L-033/00
- 유럽특허분류 (ECLA Code) : H01L-027/15B
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  KR 0697803 B1 (2007.03.14)
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- 법적상태 (Legal Status) :

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(54) 복수의 발광 소자를 갖는 발광 장치

요약

높은 구동전압 및 낮은 구동전류로 동작하는 발광 장치이다. 사파이어 기판 등의 절연기판(10)상에 복수의 LED(1)를 마차원적으로 모놀리식 형성하고, 복수의 LED(1)를 직렬 접속해서 LED 어레이로 한다. 2조의 LED 어레이를 서로 역극성으로 전극(32)에 접속한다. LED(1)의 사이 및 LED(1)와 전극(32) 사이에는 에어 브리지 배선(28)으로 한다. LED 어레이를 지그재그 형상으로 배치함으로서 다수의 LED(1)를 형성하고, 높은 구동전압과 낮은 구동전류를 얻는다. 2개의 LED 어레이는 역극성이기 때문에, 전원으로서 교류전원을 사용할 수 있다.

대표도

도6

색인어

발광 장치, 모놀리식, 높은 구동 전압, 역극성

명세서

기술분야

본 발명은, 기판 상에 복수의 발광 소자가 형성된 발광 장치에 관한 것이다.

배경기술

발광 소자(LED)등의 발광수단이 표시용도 등에 사용되는 경우에는, 그 사용조건이 구동전압 약 1~4V, 구동전류 약 20mA로 되어 있다. 그런데, 최근 GaN계 화합물 반도체를 이용한 단파장 LED가 개발되어, 풀 컬러나 백색 등의 고체 광원이 실용화됨에 따라, 점차 LED를 조명용도에도 응용하는 것이 검토되고 있다. LED를 조명용도에 응용하는 경우에, 상술한 구동전압 약 1~4V, 구동전류 약 20mA라고 하는 사용조건과는 다른 조건에서 사용되는 사태도 생긴다. 이 때문에, LED에 의해 대전류를 흐르게 하고, 발광출력을 크게 하는 연구가 이루어지고 있다. 대전류를 흐르게 하기 위해서는, LED의 pn접합 면적을 크게 하고, 전류밀도를 작게 억제할 필요가 있다.

LED를 조명용 광원으로 사용하는 경우에는, 전원으로서 교류를 사용하고, 100V 이상의 구동전압에서 사용할 수 있는 것이 편리하다. 또한, 같은 전력을 투입해서 같은 발광출력을 얻는다면, 낮은 전류값을 유지하면서 높은 전압을 인가하는 쪽이 전력손실을 작게 할 수 있다. 그러나, 종래의 LED에서는, 반드시 충분히 구동전압을 높게 할 수는 없었다.

발명의 상세한 설명

본 발명의 목적은, 높은 구동전압으로 동작할 수 있는 발광 장치를 제공하는 것에 있다.

본 발명은, 절연기판 상에 복수의 GaN계 발광 소자가 형성되고, 상기 복수의 발광 소자가 모놀리식으로 직렬 접속되는 것을 특징으로 한다.

여기서, 상기 복수의 발광 소자는 상기 기판 상에 이차원 배치되어 있는 것이 호적하다.

또한, 상기 복수의 발광 소자는 2조로 나뉘어, 2개의 전극에 서로 반대극성이 되도록 병렬 접속되어도 좋다.

상기 복수의 발광 소자 사이의 접속은 에어 브리지 배선으로 해도 좋다.

상기 복수의 발광 소자 사이의 전기적인 분리는, 상기 기판으로 사용되는 사파이어에 의해 행해져도 좋다.

또한, 상기 복수의 발광 소자는 동수(同數)씩 2조로 나뉘어, 각조의 발광 소자 어레이는 지그재그 형상으로 배치하고, 또한, 2조의 발광 소자 어레이는 2개의 전극에 서로 반대극성이 되도록 병렬 접속되어도 좋고, 상기 2조의 발광 소자 어레이는, 서로 다르게 배치해도 좋다.

또한, 상기 발광 소자 및 전극은, 평면형상이 거의 정방형 혹은 삼각형상으로 해도 좋다.

또한, 상기 복수의 발광 소자 및 전극은, 전체 형상이 거의 정방형이 되도록 배치해도 좋다.

본 발명에 있어서, 전극은 교류전원용 전극으로 할 수 있다.

또한, 상기 2조의 발광 소자 어레이는, 공통의 n전극을 가져도 좋다.

본 발명에서는 복수의 발광 소자를 모놀리식으로, 즉 동일 기판 상에 형성하고, 이들을 직렬 접속함으로서, 고(高)구동전압을 가능하게 한다. 복수의 발광 소자를 한쪽 방향으로 접속함으로서 직류구동이 가능하게 되지만, 복수의 발광 소자를 2조로 나누고, 각조의 발광 소자(발광 소자 어레이)를 서로 역극성이 되도록 전극에 접속함으로서 교류구동도 가능해진다. 각조의 개수는 동수(同數)라도 좋고, 혹은 달라도 좋다.

복수의 발광 소자를 이차원 배열하는 방법은 여러 가지 존재하지만, 기판 전유면적을 될 수 있는 한 작게 하는 것이 바람직하다. 예를 들면, 2조의 발광 소자 어레이를 각각 지그재그 형상으로, 즉 복수의 발광 소자를 절곡된 직선상에 배치하고, 각각의 발광 소자 어레이를 서로 다르게 배치함으로서, 기판 면적을 유효 활용해서 다수의 발광 소자를 접속할 수 있다. 2조의 발광 소자 어레이를 서로 다르게 배치함으로서, 배선의 교차부분이 생기는 경우도 있지만, 발광 소자 사이를 에어브리지 배선으로 접속함으로서 교차부분에서의 단락을 유효하게 방지할 수 있다. 발광 소자 및 전극 형상은 임의지만, 예를 들면 평면형상이 거의 정방형으로 되도록 형성함으로서 전체형상도 거의 정방형으로 되고, 표준적인 마운트 구조를 사용할 수 있다. 발광 소자 및 전극을 정방형 이외, 예를 들면, 삼각형으로 한 경우라도, 이들 삼각형상을 조합해서 전체로서 거의 정방형을 형성하면, 마찬가지로 표준적인 마운트 구조를 사용할 수 있게 된다.

도면의 간단한 설명

도 1은, 발광 소자(LED)의 기본구성도이다.

도 2는, 발광 장치의 등가회로도이다.

도 3은, 2개의 LED의 평면도이다.

도 4는, 도 3의 IV-IV 단면도이다.

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도 5는, 발광 장치의 다른 등가회로도이다.

도 6은, 40개의 LED를 이차원 배열한 설명도이다.

도 7은, 도 6의 회로도이다.

도 8은, 6개의 LED를 이차원 배열한 설명도이다.

도 9는, 도 8의 회로도이다.

도 10은, 14개의 LED를 이차원 배열한 설명도이다.

도 11은, 도 10의 회로도이다.

도 12는, 6개의 LED를 이차원 배열한 설명도이다.

도 13은, 도 12의 회로도이다.

도 14는, 16개의 LED를 이차원 배열한 설명도이다.

도 15는, 도 14의 회로도이다.

도 16은, 2개의 LED를 배열한 설명도이다.

도 17은, 도 16의 회로도이다.

도 18은, 4개의 LED를 이차원 배열한 설명도이다.

도 19는, 도 18의 회로도이다.

도 20은, 3개의 LED를 이차원 배열한 설명도이다.

도 21은, 도 20의 회로도이다.

도 22는, 6개의 LED를 이차원 배열한 설명도이다.

도 23은, 도 22의 회로도이다.

도 24는, 5개의 LED를 이차원 배열한 설명도이다.

도 25는, 도 24의 회로도이다.

도 26은, 다른 이차원 배치 설명도이다.

도 27은, 도 26의 회로도이다.

도 28은, 다른 이차원 배치 설명도이다.

도 29는, 도 28의 회로도이다.

도 30은, 다른 이차원 배치 설명도이다.

도 31은, 도 30의 회로도이다.

실시예

이하, 도면에 근거해서 본 발명의 실시예에 대해 설명한다.

도 1은, 본 실시예에 있어서 GaN계 화합물 반도체 발광 소자로서의 LED(1)의 기본구성이 나타나 있다. LED(1)은, 기판(10)상에 차례로 GaN층(12), Si-도핑 n형 GaN층(14), InGaN발광층(16), AlGaN층(18), p형 GaN층(20)이 적층되고, p형 GaN층(20)에 접해서 p전극(22), n형 GaN층(14)에 접해서 n전극(24)이 형성되는 구성이다.

도 1에 나타낸 LED는 이하의 프로세스에 의해 제작된다. 즉, 우선, MOCVD장치로 사파이어 c면 기판을 수소분위기중에서 1100℃, 10분간 열처리한다. 그리고, 온도를 500 ℃까지 강온(降溫)시키고, 실란가스와 암모니아가스를 100초간 공급해서 불연속적인 SiN막을 기판(10)상에 형성한다. 즉, 상기 프로세스는 디바이스층의 전위밀도를 저감시키기 위한 것이고, 도에서는 SiN막은 생략하고 있다. 다음으로, 동일 온도로 트리메틸갈륨 및 암모니아가스를 공급해서 GaN층을 20nm 두께 성장시킨다. 온도를 1050 ℃로 승온(昇溫)하고, 다시 트리메틸갈륨 및 암모니아가스를 공급해서 언도핑 GaN(u-GaN)층12 및 Si도핑 n형 GaN층(14)을 각 2㎛ 두께 성장시킨다. 그 뒤, 온도를 700 ℃ 정도까지 강온해서 InGaN발광층(16)을 2nm 두께 성장시킨다. 목표조성은 x=0.15, 즉 $In_{0.15}Ga_{0.85}N$ 이다. InGaN발광층(16) 성장 후, 온도를 1000 ℃까지 승온해서 AlGaN 정공(正孔)주입층(18)을 성장시키고, 나아가 p형 GaN층(20)을 성장시킨다.

p형 GaN층(20)을 성장시킨 후, 웨이퍼를 MOCVD 장치로부터 꺼내고, Ni10nm 두께, Au10nm 두께를 차례로 전공증착으로 성장층 표면에 형성한다. 5%의 산소를 포함하는 질소가스 분위기중에서 520 ℃ 열처리함으로서 금속막은 p형 투명전극(22)으로 된다. 투명전극 형성후, 전면에 포토레지스트를 도포하고, n형전극 형성을 위한 에칭을 포토레지스트를 마스크로서 행한다. 에칭 깊이는, 예를 들면, 600nm 정도이다. 에칭으로 노출된 n형 GaN층(14)상에 Ti 5nm 두께, Al 5nm 두께를 형성하고, 질소가스 분위기중에서 450 ℃, 30분간 열처리해서 n형전극(24)을 형성한다. 마지막으로, 기판(10)의 속면(裏面)을 100㎛까지 연마해서 칩을 잘라내고, 마운트함으로서 LED(1)이 얻어진다.

도 1에서는, 기판(10)상에 하나의 GaN계 LED(1)가 형성되어 있지만, 본 실시예에서는, 기판(10)

상에 LED(1)를 모놀리식으로, 또한 이차원 어레이 형상으로 복수 형성하고, 각 LED를 접속해서 발광 장치(칩)를 구성한다. 여기서, 「모놀리식」이란, 1개의 기판상에 모든 소자가 형성되어 있는 것을 의미한다.

도 2에는, 발광 장치의 등가회로도가 나타나 있다. 도 2에서, 2차원 어레이 형상으로 형성된 발광 소자군은 동수(도4에서는 4개)씩 2조로 나뉘어, 각 조의 LED(1)은 각각 직렬 접속되고, 2조의 LED배열은 전극(구동전극)에 대해서 역극성으로 되도록 병렬 접속된다. 이와 같이 LED배열이 직렬 접속됨으로서, 각각의 구동전압이 가산된 높은 전압에서 LED(1)를 구동할 수 있다. 또한, 각 LED배열은 그 극성이 서로 반대가 되도록 전극에 병렬 접속되어 있으므로, 전원으로서 교류전원을 사용한 경우에도, 전원의 각 주기 중에 반드시 어느 쪽인가의 LED열이 발광하고 있게 되므로, 효율이 좋은 발광을 행할 수 있다.

도 3에는, 기판(10)상에 모놀리식으로 형성된 복수의 LED의 부분적인 평면도가 나타나 있다. 또한, 도4는, 도3의 Ⅳ-Ⅳ 단면도가 나타나 있다. 도 3에 있어서, LED(1)의 상면에는, 도1에 나타낸 것과 같이 p전극(22) 및 n전극(24)이 형성되어 있다. 인접하는 LED(1)의 p전극(22)과 n전극(24)의 사이가 에어 브리지 배선(28)에 의해 접속되고, 복수의 LED(1)가 직렬 접속된다.

도 4에 있어서, 각 LED(1)는 설명의 편의상 간략하게 나타내고 있다. 즉, n형 GaN층(14), p형 GaN층(20), p전극(22), n전극(24)만이 나타나 있다. 실제로는 도1에 나타난 것과 같이 InGaN발광층(16) 등이 존재하는 것은 말할 필요도 없다. 에어 브리지 배선(28)은, p전극(22)에서부터 n전극(24)까지를 공중(空中)을 개재시켜 접속한다. 이에 따라, 소자표면에 절연막을 도포하고, 그 위에 전극을 형성해서 p전극(22)과 n전극(24)을 전기적으로 접속하는 방법에 비해서, 에칭홀을 따라 전극을 배치할 필요가 없게 되므로, 배선조각이나 절연막에서 n층, p층으로 절연재료를 구성하는 원소가 열확산해서 LED(1)를 열화 시키는 문제를 회피할 수 있다. 에어 브리지 배선(28)은 LED(1) 사이뿐만 아니라, LED(1)와 도시하지 않은 전극 사이의 접속에도 사용된다.

또한, 도 4에 나타낸 것과 같이, 각 LED(1)는 서로 독립하고, 전기적으로 절연될 필요가 있다. 이 때문에, 각 LED(1)는 사파이어 기판(10)상에서 분리된 구성으로 되어 있다. 사파이어는 그 자체가 절연체이므로, LED(1)를 각각 전기적으로 분리할 수 있다. 이와 같이, 사파이어 기판(10)을 LED의 전기적인 분리를 행하기 위한 저항체로서 사용함으로서, 용이하고 또한 확실하게 LED의 전기적인 분리를 행할 수 있다.

즉, 발광 소자로서는, pn접합을 갖는 LED 이외, MIS로 할 수도 있다.

도 5에는, 발광 장치의 다른 등가회로도가 나타나 있다. 도에서, 20개의 LED(1)가 직렬 접속되어 하나의 LED 어레이를 형성하고 있고, 두 개의 LED 어레이(합계 40개의 LED)가 전원에 병렬로 접속되어 있다. LED(1)의 구동전압은 5V로 설정되고, 각 LED 어레이의 구동전압은 100V로 되어 있다. 두 개의 LED 어레이는 도2와 마찬가지로 서로 반대극성으로 되도록 전원에 병렬 접속되어 있고, 전원의 극성이 모두 반드시 어느 쪽인가의 LED 어레이가 발광하게 된다.

도 6에는, 이차원 어레이가 구체적으로 나타나 있다. 도 2의 등가 회로도에 대응하는 것이다. 도에서, 사파이어 기판(10)상에 합계 40개의 LED(1)가 형성되어 있고, 각각 20개씩 2조로 나뉘어져, 에어 브리지 배선(28)에 의해 직렬 접속되어 두 개의 LED 어레이를 형성하고 있다. 보다 상세하게는, 각 LED(1)는 모두 동형(同形)인 정방형으로 동사이즈이고, 하나의 LED 어레이는 위에서부터 6개, 7개, 7개로 각각 직선상에 배치되고, 위에서부터 제1열째(6개)와 제2열째(7개)는 서로 역방향으로 형성되고, 제2열째와 제3열째도 서로 역방향으로 형성된다. 제1열째와 제2열째, 제2열째와 제3열째는 서로 이간(離間)되어 배치되어 있다. 이것은 후술하는 것과 같이, 다른 쪽의 LED 어레이 열에 교대로 삽입되기 때문이다. 제1열째의 우단(右端) LED(1)와 제2열째의 우단 LED(1)는 에어 브리지 배선(28)에 의해 접속된다. 제2열째의 좌단 LED(1)와 제3열째의 좌단(左端) LED(1)도 에어 브리지 배선(28)으로 접속되어 지그재그 배열로 된다. 제1열째의 좌단 LED(1)는 기판(10)의 좌상부에 형성된 전극(패드)(32)에 에어 브리지 배선(28)으로 접속되고, 제3열째의 우단 LED(1)는 기판(10)의 우하부에 형성된 전극(패드)(32)에 에어 브리지 배선(28)으로 접속된다. 두 개의 전극(패드)(32)도 LED(1)와 동형인 정방형이다. 다른 쪽 LED 어레이는 상술한 한쪽 LED 어레이의 간극에 서로 다르게 형성된다. 즉, 다른 쪽 LED 어레이는 위에서부터 7개, 7개, 6개로 각각 직선상에 배치되고, 위에서부터 제1열째는 한쪽 LED 어레이의 제1열째와 제2열째의 사이에 형성되고, 제2열째는 한쪽 LED 어레이의 제2열째와 제3열째의 사이에 형성되고, 제 3열째는 한쪽 LED 어레이의 제3열째의 아래에 형성된다. 다른 쪽 LED 어레이의 제1열째와 제2열째, 및 제2열째와 제3열째 도 서로 역방향으로 되도록 형성되고, 제1열째의 우단 LED(1)는 제2열째의 우단 LED(1)에 에어 브리지 배선(28)으로 접속되고, 제2열째의 좌단 LED(1)는 제3열의 좌단 LED(1)에 에어 브리지 배선(28)으로 접속되어 지그재그 형상으로 된다. 다른 쪽 LED 어레이의 제1열째의 좌단 LED는 기판(10)의 좌상부(左上部)에 형성된 전극(32)에 에어 브리지 배선(28)으로 접속되고, 제3열째의 우단 LED(1)는 기판(10)의 우하부(右下部)에 형성된 전극(32)에 에어 브리지 배선(28)으로 접속된다. 한쪽 LED 어레이와 다른 쪽 LED 어레이의 전극(32)에 대한 극성은 서로 반대이다. 발광 장치(칩)의 전체 형상은 장방형이다. 전원이 공급되는 두 개의 전극(32)은, 장방형의 대각선 위치에 이간해서 형성되는 점도 착안하고 싶다.

도 7에는, 도 6의 회로도가 나타나 있다. 각각의 LED 어레이는 지그재그 형상으로 굴곡하면서 직렬 접속되고, 2개의 LED 어레이는 지그재그 형상의 각 열이 서로의 열 사이에 형성되는 모습이 분명해질 것이다. 이와 같은 배치로 함으로서, 다수의 LED(1)를 작은 기판(10)상에 배치할 수 있다. 또한, 40개의 LED(1)에 대해서 전극(32)이 2개로도 되므로, 이점에서도 기판(10)의 사용 효율을 향상시킬 수 있다. 또한, 각 LED(1)를 분리하기 위해서 LED(1)를 개별로 형성하는 경우에는 웨이퍼를 잘라서 분리할 필요가 있는 것에 대해, 본 실시예에서는 각 LED(1)의 분리를 에칭으로 행할 수 있으므로, LED(1)의 간극을 좁게 할 수 있다. 이에 따라, 사파이어 기판(10)의 크기를 보다 작게 할 수 있다. LED(1)끼리의 분리는, 포토레지스트나 반응성 이온 에칭, 습식 에칭을 병용함으로서 LED(1) 이외의 영역을 기판(10)에 달할 때까지 에칭 제거함으로서 달성된다. 각 LED 어레이는 교대로 발광하므로, 발광효율을 향상할 수 있음과 동시에 방열 특성도 향상시킬 수 있다. 또한, 직렬 접속시키는 LED(1)의 수를 변경하면, 전체로서의 구동전압도 변경할 수 있다. 또한, LED(1)의 면적을 작게 하면, 하나의 LED당 구동전압을 높게 할 수도 있다. LED(1)를 20개 직렬로 접속한 경우, 상용전원(100V, 60Hz)으로 구동하면, 대략 150mW의 발광출력을 얻을 수

있다. 이 경우의 구동전류로서는 20mA 정도이다.

즉, 도 7로부터 알 수 있듯이, 2개의 LED 어레이를 지그재그 형상으로 교대로 배열할 경우, 에어 브리지 배선(28)에 교차부분(34)이 필연적으로 발생한다. 예를 들면, 다른 쪽 LED 어레이의 제1열째와 제2열째를 접속할 때, 한 쪽 LED 어레이의 제1열째와 제2열째를 접속하기 위한 배선부분과 교차한다. 그러나, 본 실시예의 에어 브리지 배선(28)은, 상술한 것과 같이 기판(10)에 접착되어 있지 않고, 기판(10)으로부터 떨어져 공중(空中)을 통과하므로, 교차부분(34)에 있어서 에어 브리지 배선(28)끼리 접촉하고, 단락하는 것을 쉽게 회피할 수 있다. 에어 브리지 배선(28)을 이용하는 이점의 하나이다. 에어 브리지 배선(28)은, 예를 들면, 다음과 같이 형성된다. 즉, 전면에 2㎛의 두께의 포토레지스트를 도포하고, 에어 브리지 배선(28)의 형상으로 구멍을 뚫은 후에 포스트 베이크 한다. 그 위에, 진공증착으로 Ti를 10nm, Au를 10nm, 상기 순서로 증착한다. 나아가, 그 위의 전면에 2㎛ 두께로 포토레지스트를 다시 도포하고, 에어 브리지 배선(28)을 형성하는 부분에만 구멍을 뚫는다. 이어서, Ti와 Au를 전극으로서 전해액속에서 이온 도금에 의해 전극 전면에 3~5㎛의 두께의 Au를 부착시킨다. 그 다음, 시료를 아세톤에 담그고, 초음파세정에 의해 포토레지스트를 용해제거해서 에어 브리지 배선(28)이 완성된다.

이와 같이, 복수의 LED(1)를 이차원 어레이 형상으로 배치함으로서, 기판면적을 유효하게 활용하면서 고(高)구동전압, 특히, 상용전원에서의 구동도 가능해지지만, 이차원 어레이의 패턴으로서는 이 외에도 다양한 패턴이 가능하다. 일반적으로, 이차원 어레이 패턴으로서는, 다음의 조건을 구비하는 것이 바람직하다.

(1) 각 LED에 균일하게 전류를 흐르게 하고, 균일한 발광을 얻기 위해서는 각 LED의 형상, 전극 위치가 동일한 것이 바람직하다.

(2) 웨이퍼를 잘라서 칩으로 하기 위해서는, 각 LED의 변(邊)은 직선인 것이 바람직하다.

(3) 광 취출 효율을 향상시키기 위해, 표준적인 마운트를 사용해서 주변으로부터의 반사를 이용하기 위해서는 LED는 평면형상이 정방형에 가까운 형상이 바람직하다.

(4) 2개의 전극(본딩 패드)의 크기는 100㎛각 정도로, 서로 떨어져 있는 것이 바람직하다.

(5) 웨이퍼 면적의 유효한 이용을 위해, 배선, 패드가 차지하는 비율은 작은 편이 바람직하다.

물론, 이들은 반드시 필요한 것은 아니고, 예를 들면, LED의 형상으로서는 평면형상 삼각형을 이용하는 것도 가능할 것이다. 각 LED의 형상이 삼각형이라도, 이들을 조합시킴으로서 전체 형상을 거의 정방형으로 할 수 있다. 이하, 이차원 어레이 패턴의 예를 몇 개 나타낸다.

도 8에는, 합계 6개의 LED(1)를 이차원으로 배치한 예가 나타나 있고, 도9에는 그 회로도가 나타나 있다. 도8의 배치는, 기본적으로 도6의 배치와 동일하고, 합계 6개의 LED 어레이는 동수(同數)씩 2조로 나뉘어, 각각 직렬 접속된 3개의 LED로부터 구성된다. 한 쪽 LED 어레이는 지그재그 형상으로 배열되고, 위에서부터 제1열째는 1개의 LED(1), 제2열째는 2개의 LED(1)가 형성된다. 제1열째의 LED와 제2열째의 우단 LED(1)는 에어 브리지 배선(28)으로 직렬 접속된다. 기판(10)의 좌상부와 좌하부에 전극(패드)32가 형성되고, 제1열째의 LED(1)는 좌상부의 전극(32)에 에어 브리지 배선(28)으로 접속되고, 제2열째의 좌단 LED(1)는 좌하부의 전극(32)에 접속된다. 다른 쪽 LED 어레이도 지그재그 형상으로 배열되고, 위에서부터 제1열째는 2개의 LED(1), 제2열째는 1개의 LED(1)가 형성된다. 다른 쪽 LED 어레이의 제1열째는 상기 한쪽 LED 어레이의 제1열째와 제2열째 사이에 형성되고, 다른 쪽 LED 어레이의 제2열째는 상기 한쪽 LED 어레이의 제2열째의 하방에 형성된다. 제1열째의 우단 LED(1)는 제2열째의 LED(1)에 에어 브리지 배선(28)으로 직렬 접속되고, 제1열째의 2개의 LED(1)끼리도 에어 브리지 배선(28)으로 직렬 접속된다. 제1열째의 좌단 LED(1)는 좌상부의 전극(32)에 에어 브리지 배선(28)으로 접속되고, 제2열째의 LED(1)는 좌하부의 전극(32)에 에어 브리지 배선(28)으로 접속된다. 도9로부터 알 수 있듯이, 이 예에서도 2개의 LED 어레이는 서로 병렬로 전극(32)에 접속되고, 또한, 서로 역극성으로 되도록 접속된다. 따라서, 교류전원을 공급한 경우, 2개의 LED 어레이는 교대로 발광하게 된다.

도 10에는, 합계 14개의 LED를 이차원으로 배치한 예가 나타나 있고, 도 11에는 그 회로도가 나타나 있다. 합계 14개의 LED 어레이는 2조로 나뉘어, 각각 직렬 접속된 7개의 LED로부터 구성된다. 한 쪽 LED 어레이는 지그재그 형상으로 배열되고, 위에서부터 제1열째는 3개의 LED(1), 제2열째는 4개의 LED(1)가 형성된다. 제1열째의 좌단 LED와 제2열째의 좌단 LED(1)는 에어 브리지 배선(28)으로 직렬 접속되고, 제1열째의 3개의 LED끼리, 및 제 2열째의 4개의 LED(1)끼리도 에어 브리지 배선(28)으로 직렬 접속된다. 기판(10)의 우상부와 우하부에 전극(패드)32가 형성되고, 제 1열째의 우단 LED(1)는 우상부의 전극(32)에 에어 브리지 배선(28)으로 접속되고, 제2열째의 우단 LED(1)는 우하부의 전극(32)에 접속된다. 다른 쪽 LED 어레이도 지그재그 형상으로 배열되고, 위에서부터 제1열째는 4개의 LED(1), 제2열째는 3개의 LED(1)가 형성된다. 다른 쪽 LED 어레이의 제1열째는 상기 한쪽 LED 어레이의 제1열째와 제2열째 사이에 형성되고, 다른 쪽 LED 어레이의 제2열째는 상기 한쪽 LED 어레이의 제2열째의 하방에 형성된다. 제1열째의 우단 LED(1)는 제2열째의 좌단 LED(1)에 에어 브리지 배선(28)으로 직렬 접속된다. 제1열째의 4개의 LED(1)끼리 및 제2열째의 3개인 LED(1)끼리도 직렬 접속된다. 제1열째의 우단 LED(1)는 우상부의 전극(32)에 에어 브리지 배선(28)으로 접속되고, 제2열째의 우단 LED(1)는 우하부의 전극(32)에 에어 브리지 배선(28)으로 접속된다. 도 11로부터 알 수 있듯이, 이 예에서도 2개의 LED 어레이는 서로 병렬로 전극(32)에 접속되고, 또한, 서로 역극성으로 되도록 접속된다. 따라서, 교류전원을 공급한 경우, 2개의 LED 어레이는 교대로 발광하게 된다.

도 6, 도 8, 도 10의 이차원 패턴에 공통하는 특징으로서는, 각 LED(1)가 거의 정방형의 동형(同形), 동사이즈인 것, 2개의 전극(패드)도 거의 정방형이고, 인접 형성되어 있지 않은(이간 형성되어 있는) 것, 2개의 LED 어레이의 조합인 것, 2개의 LED 어레이는 글곡하면서 첩상에 서로 교차하도록 형성되는 것, 2개의 LED 어레이는 서로 역극성이 되도록 전극에 접속되는 것, 등이다.

도 12에는, 평면형상이 삼각형인 LED를 이차원 배열한 경우의 예가 나타나 있고, 도 13에는 그 회로도가 나타나 있다. 도 12에 있어서, 합계 6개의 LED(1a, 1b, 1c, 1d, 1e, 1f)가 그 평면형상이 삼각

형상으로 되도록 형성되어 있다. LED(1a와 1e)가 삼각형의 일변에서 대향해서 2개로 거의 정방형이 되도록 배치되고, LED(1b와 1f)가 대향해서 2개로 거의 정방향으로 되도록 배치된다. 또한, LED(1d)와 전극(32)이 대향해서 접속하고, LED(1c)와 전극(32)이 대향해서 접속한다. 2개의 전극(32)도 LED와 마찬가지로 평면형상이 삼각형상이고, 마찬가지로 거의 정방형이 되도록 배치된다. LED끼리 대향하는 변은 n전극(24)을 구성하고, 즉, 대향하는 2개의 LED는 n전극(24)를 공유한다. LED와 전극(32)도 n전극 접속이다. 이 배치도, 상술한 예와 마찬가지로 합계 6개의 LED는 2조로 나눠진다. 한쪽 LED 어레이는, LED(1a, 1b, 1c)로 이루어지는 어레이 이고, LED(1a)의 p전극(22)은 전극(32)에 에어 브리지 배선(28)으로 접속되고, 그 n전극(24)은 LED(1b)의 p전극(22)과 에어 브리지 배선(28)으로 접속된다. LED(1b)의 n전극(24)은 LED(1c)의 p전극(22)과 에어 브리지 배선(28)으로 접속된다. LED(1c)의 n전극(24)은 전극(32)에 접속된다. 다른 쪽 LED 어레이는 LED(1d, 1e, 1f)로 구성되고, 전극(32)와 LED(1f)의 p전극(22)은 에어 브리지 배선(28)으로 접속되고, LED(1f)의 n전극(24)은 LED(1e)의 p전극(22)과 에어 브리지 배선(28)으로 접속되고, LED(1e)의 n전극(24)과 LED(1d)의 p전극(22)은 에어 브리지 배선(28)으로 접속되고, LED(1d)의 n전극(24)은 전극(32)에 접속된다.

도 13에 있어서, 한쪽 LED 어레이를 구성하는 LED(1a)와 다른쪽 LED 어레이를 구성하는 LED(1e)의 n전극(24)이 접속되어 있고, 한 쪽 LED 어레이를 구성하는 LED(1b)와 다른 쪽 LED 어레이를 구성하는 LED(1f)의 n전극(24)이 접속되어 있는 점에도 착안하고 싶다. 2조의 LED 어레이의 몇 개의 n전극(24)을 공유함으로서, 회로배선을 삭감할 수 있다. 또한, 이 예에서도, 2개의 LED 어레이는 병렬로 전극(32)에 접속되고, 또한, 서로 역극성이 되도록 접속된다. 또한, 각 LED는 동형, 동사이즈이고, 각 LED를 하나의 변으로 대향시킴과 동시에 전극(32)도 삼각형상으로 함으로서 LED 및 전극을 고밀도로 형성해서 필요한 가판면적을 작게 할 수 있다.

도 14에는, 평면형상이 삼각형인 LED를 이차원 배열한 다른 예가 나타나 있고, 도 15에는 그 회로도가 나타나 있다. 이 예에서는, 합계 16개의 LED(1a~1r)이 이차원 형성되어 있다. LED(1a) 와 LED(1j), LED(1b) 와 LED(1k), LED(1c) 와 LED(1m), LED(1d) 와 LED(1n), LED(1e) 와 LED(1p), LED(1f) 와 LED(1q), LED(1g) 와 LED(1r) 이 각각 삼각형의 하나의 변에 대향한다. 대향하는 변에는 n전극(24)이 공통 형성되어 있다. 또한, LED(1i)와 전극(32)이 대향하고, LED(1h)와 전극(32)이 대향한다. 한쪽 LED 어레이는 LED(1a, 1b, 1c, 1d, 1e, 1f, 1g, 1h)로 구성되고, 다른 쪽 LED 어레이는 LED(1r, 1q, 1p, 1n, 1m, 1k, 1j, 1i)로 구성된다. LED(1b)의 n전극(24)은 에어 브리지 배선(28)에 의해 LED(1c)의 p전극(22)에 접속되고, LED(1e)의 n전극(24)도 에어 브리지 배선(28)에 의해 LED(1f)의 p전극(22)에 접속된다. 또한, LED(1q)의 n전극(24)도 에어 브리지 배선(28)에 의해 LED(1p)의 p전극(22)에 접속되고, LED(1m)의 n전극(24)도 에어 브리지 배선(28)에 의해 LED(1k)의 p전극(22)에 접속된다. 도 14에 있어서도, 도 12와 마찬가지로 교차부분이 생기지만, 에어 브리지 배선(28)에 의해 단락을 회피할 수 있다. 또한, 이 예에서도 2조의 LED 어레이의 몇 개인가의 n전극(24)를 공유구조로 함으로서 필요한 배선을 삭감하고 있다. 또한, 이 예에서도 2개의 LED 어레이는 병렬로 서로 역극성으로 전극(32)에 접속되어 있고, 교류구동이 가능하다. 도 12에 있어서는, 합계 6개의 LED의 경우, 도 14에 있어서는, 합계 16개의 LED의 경우에 대해서 나타냈지만, 다른 개수의 LED라도 마찬가지로 이차원 배열할 수 있다. 본 출원인은, 38개의 LED를 이차원 배열한 발광 장치도 작성하고 있다.

이상, 교류구동의 경우에 대해서 설명했지만, 직류구동도 가능하다는 것은 말할 필요도 없다. 이 경우, LED 어레이를 서로 역극성으로 되도록 전극에 접속하는 것이 아니라, 직류전원의 극성 방향에 맞추어 LED 어레이를 순방향으로 접속하면 좋다. 복수의 LED를 직렬 접속함으로서, 고전압구동이 가능하다. 이하, 직류구동의 경우에 대해서 설명한다.

도 16에는, 2개의 LED를 직렬 접속한 예가 나타나 있고, 도 17에는 그 회로도가 나타나 있다. 각 LED(1)는 평면형상이 직사각형상이고, 2개의 LED 사이는 에어 브리지 배선(28)으로 접속된다. 전극(32)은 LED(1)의 근방에 형성되어 있고, 전극(32)과 LED(1)에서 장방형의 영역을 형성한다. 즉, 전극(32)은 장방형 영역의 일부를 점유하고, 장방형 영역의 다른 영역에 LED(1)가 형성되어 있다.

도 18에는, 합계 4개의 LED를 이차원 배열한 예가 나타나 있고, 도 19에는 그 회로도가 나타나 있다. 도 16의 LED(1)를 2개로 분할하고, 각각을 병렬로 접속한 것이다. 2개의 LED로 이루어진 LED 어레이를 2조 병렬로 순방향 접속했다고 말할 수도 있다. LED(1a)와 LED(1b)로 하나의 LED 어레이를 구성하고, LED(1c)와 LED(1d)로 하나 더 LED 어레이를 구성한다. LED(1a)와 LED(1c)는 p전극(22) 및 n전극(24)를 공유하고, LED(1b)와 LED(1d)도 p전극(22) 및 n전극(24)을 공유한다. 상기 구성에 의하면, 도 16에 비해 전류가 균일화되는 효과가 있다.

도 20은, 합계 3개의 LED를 이차원 배열한 예가 나타나 있고, 도 21에는 그 회로도가 나타나 있다. LED(1a, 1b, 1c)는 동형이 아니고, LED(1a)의 일부에 전극(32)이 형성되어 있다. LED(1a)의 n전극(24)과 LED(1b)의 p전극(22)은 LED(1b)의 위를 넘는 에어 브리지 배선(28)으로 접속된다. 각 LED의 형상 및 배치를 궁리한 끝에, 3개의 LED에서도 발광 장치(칩) 전체의 외관형상을 거의 정방형으로 할 수 있었다.

도 22에는, 합계 6개의 LED를 이차원 배열한 예가 나타나 있고, 도 23에는 그 회로도가 나타나 있다. 각 LED(1a~1f)는 동형, 동사이즈이다. LED(1a~1f)는 직렬 접속된다. LED(1a~1c)는 직선상에 배치되고, LED(1d~1f)는 다른 직선상에 배치된다. LED(1c)와 LED(1d)는 에어 브리지 배선(28)으로 접속된다. 이 예에서도, 칩 전체 형상을 거의 정방형으로 할 수 있다.

도 24에는, 합계 5개의 LED를 이차원 배열한 예가 나타나 있고, 도 25에는 그 회로도가 나타나 있다. LED(1a~1e) 는 동형(장방형), 동사이즈이다. 이 예에서도, 전체 형상을 거의 정방형으로 할 수 있다.

이상, 본 발명의 실시예에 대해서 설명했지만, 본 발명은 이에 한정되지 않고, 각종 변경이 가능하다. 특히, 복수의 발광 소자(LED 등)를 이차원 배치하는 경우의 패턴은 상술한 패턴 이외에도 가능하다. 이 경우, 인접하는 발광 소자 사이에서 전극을 공유해서 배선을 적게 하는 것, 전체 형상을 정방형 혹은 장방형으로 하는 것, 복수조의 발광 소자 어레이를 전극에 병렬 접속하는 것, 교류구동의 경우에

복수조의 발광 소자 어레이를 서로 역극성으로 하는 것, 복수조의 발광 소자 어레이를 각각 지그재그 형상으로 굴곡 시켜 조합하는 것, 등이 호적하다.

도 26~도 31에는, 이들의 변경 예의 몇 개인가를 예시하고 있다. 도 26은 교류구동의 경우의 이차원 배치이고, 합계 40개의 LED가 배치되어 있다. 도 27은 그 회로도이다. 도 6과 다른 점은, 2조의 LED 어레이의 몇 개인가가 n전극(24)을 공유하는 점이다(도 5참조). 예를 들면, 한 쪽 LED 어레이의 제1열의 우단으로부터 2번째에 위치하는 LED(도중 α로 표시한다)의 n전극(24)은, 다른 쪽 LED 어레이의 제1열의 우단에 위치하는 LED(도중 β로 표시한다)의 n전극(24)과 공유되어 있다. 즉, LED 어레이의 단부(도중 γ 부분)에 대한 에어 브리지 배선(28)은, 교차시키는 것 없이 공통 형성되어 있다.

도 28은, 교류 구동의 경우의 이차원 배치이고, 합계 14개의 LED가 배치되어 있다. 도 29는 그 회로도이다. 도 10과 다른 점은, 2조의 LED 어레이의 몇 개인가가 n전극(24)를 공유하는 점이다. 예를 들면, 한 쪽 LED 어레이의 제1열의 좌단 LED(도중 α로 표시한다)의 n전극(24)은, 다른 쪽 LED 어레이의 제1열의 우단으로부터 2번째에 위치하는 LED(도중 β로 표시한다)의 n전극(24)과 공유되여 있다. 또한, 단부(도중 γ 부분)에 대한 에어 브리지 배선(28)은, 공통 형성되어 있다.

도 30은, 교류 구동의 경우의 이차원 배치이고, 합계 6개의 LED가 배치되어 있다. 도 31은 그 회로도이다. 이 예에서도, 단부(γ 부)의 에어 브리지 배선(28)이 공통 형성되어 있다. 이 구성도, 한 쪽 LED 어레이에 대한 n전극(24)과 다른 쪽 LED 어레이에 대한 n전극(24)이 공유되여 있다고 말할 수 있다.

청구의 범위

청구항 1

절연기판 상에 복수의 GaN계 발광 소자가 형성되고, 상기 복수의 발광 소자가 모놀리식으로 직렬 접속되는 것을 특징으로 하는 발광 장치.

청구항 2

제 1 항에 있어서,

상기 복수의 발광 소자는 상기 기판 상에 이차원 배치되어 있는 것을 특징으로 하는 발광 장치.

청구항 3

제 1 항에 있어서,

상기 복수의 발광 소자는 2조로 나뉘어, 2개의 전극에 서로 반대극성이 되도록 병렬 접속되는 것을 특징으로 하는 발광 장치.

청구항 4

제 1 항에 있어서,

상기 복수의 발광 소자 사이의 접속은 에어 브리지 배선인 것을 특징으로 하는 발광 장치.

청구항 5

제 1 항에 있어서,

상기 복수의 발광 소자 사이의 전기적인 분리는, 상기 기판으로서 사용되는 사파이어에 의해 행해지는 것을 특징으로 하는 발광 장치.

청구항 6

제 2 항에 있어서,

상기 복수의 발광 소자는 동수(同數)씩 2조로 나뉘어, 각 조의 발광 소자 어레이는 지그재그 형상으로 배치되고, 또한, 2조의 발광 소자 어레이는 2개의 전극에 서로 반대 극성이 되도록 병렬 접속되는 것을 특징으로 하는 발광 장치.

청구항 7

제 6 항에 있어서,

상기 2조의 발광 소자 어레이는, 서로 다르게 배치되는 것을 특징으로 하는 발광 장치.

청구항 8

제 6 항에 있어서,

상기 발광 소자 및 전극은, 평면형상이 대략 정방형인 것을 특징으로 하는 발광 장치.

청구항 9

제 6 항에 있어서,

상기 발광 소자 및 전극은, 평면형상이 삼각형상인 것을 특징으로 하는 발광 장치.

청구항 10

제 2 항에 있어서,

상기 복수의 발광 소자 및 전극은, 전체형상이 대략 정방형이 되도록 배치되는 것을 특징으로 하는 발광 장치.

청구항 11

제 10 항에 있어서,

상기 복수의 발광 소자로 이루어진 발광 소자 어레이는 지그재그 형상으로 배치되는 것을 특징으로 하는 발광 장치.

청구항 12

제 6 항에 있어서,

상기 전극은 교류전원용 전극인 것을 특징으로 하는 발광 장치.

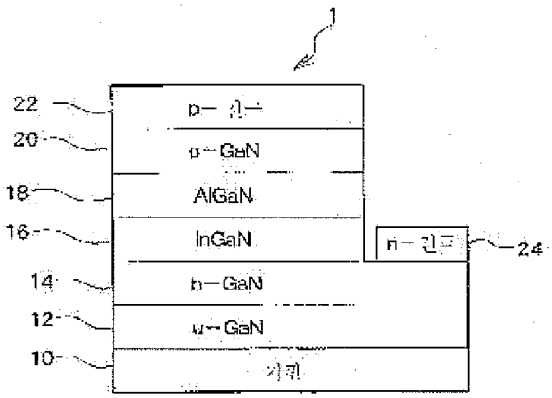
청구항 13

제 6 항에 있어서,

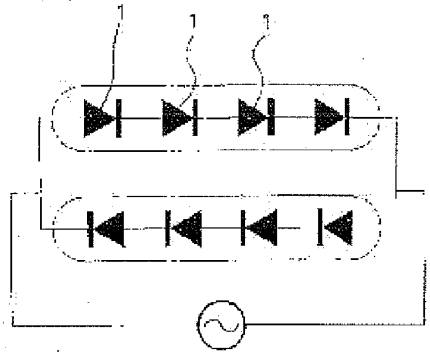
상기 2조의 발광 소자 어레이는, 공통의 n전극을 갖는 것을 특징으로 하는 발광 장치.

도면

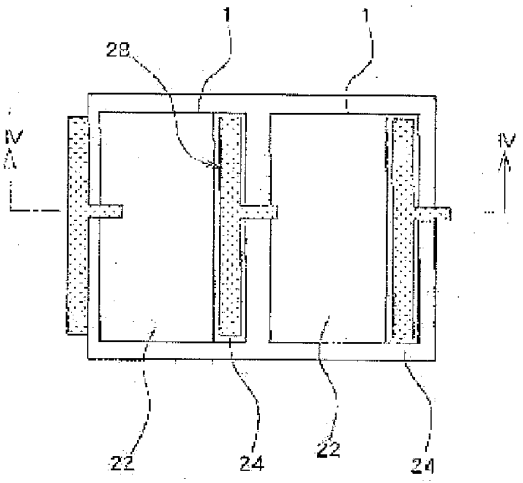
도면1



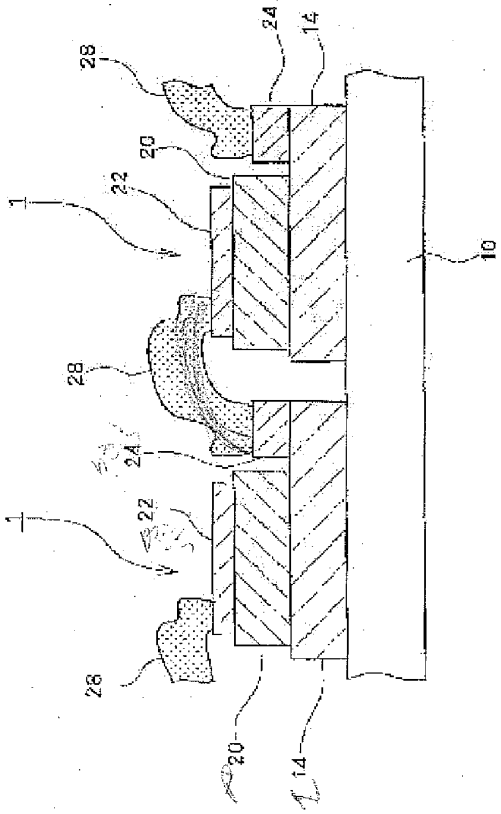
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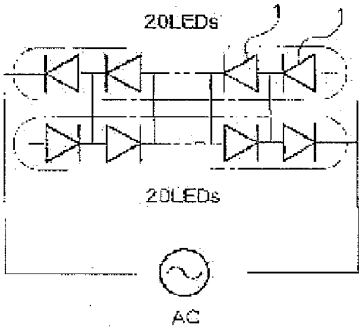
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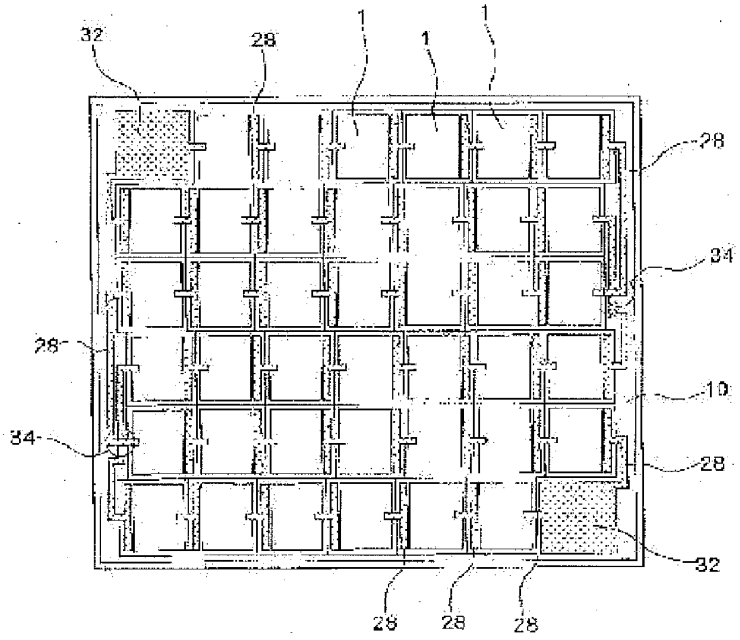
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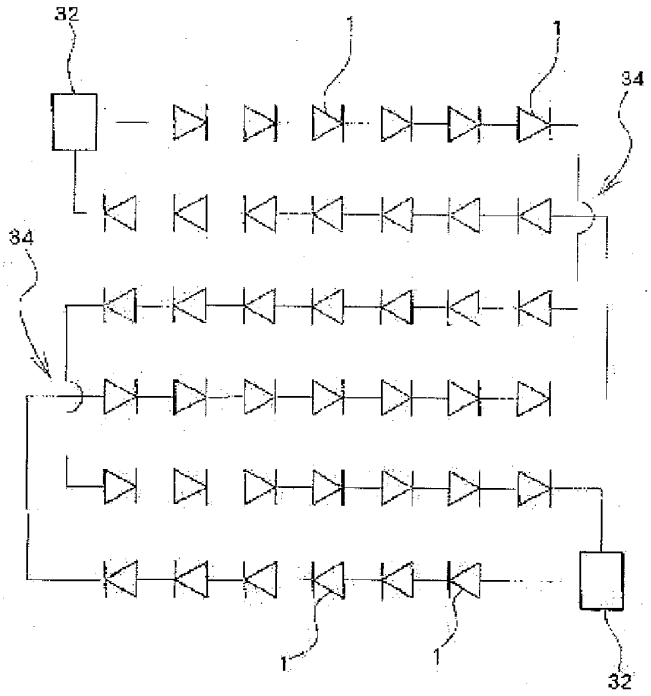
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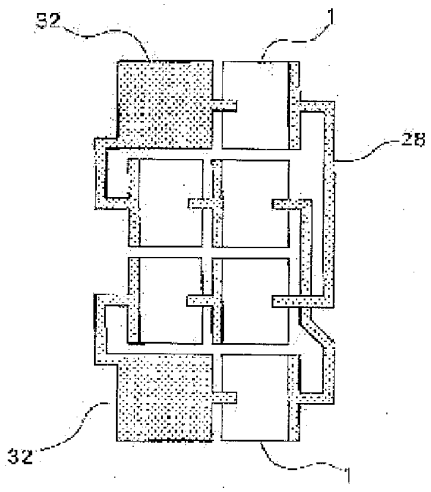
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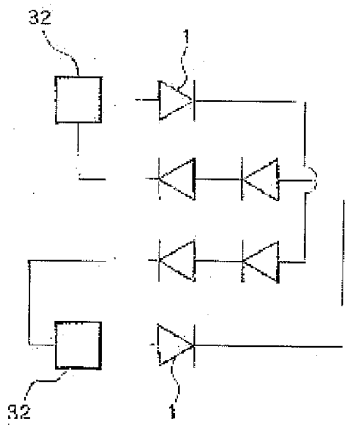
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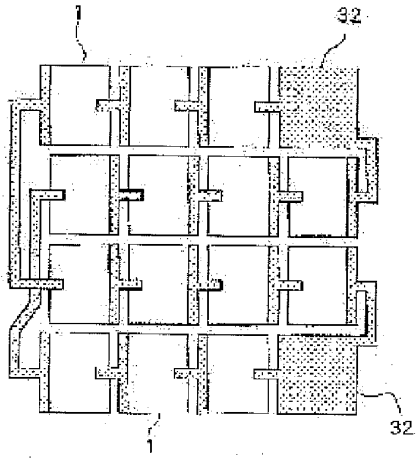
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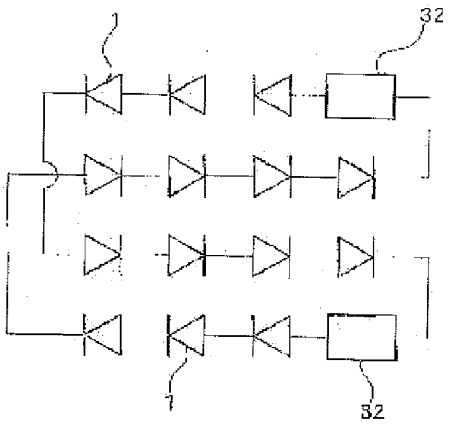
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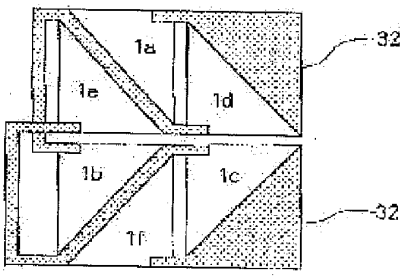
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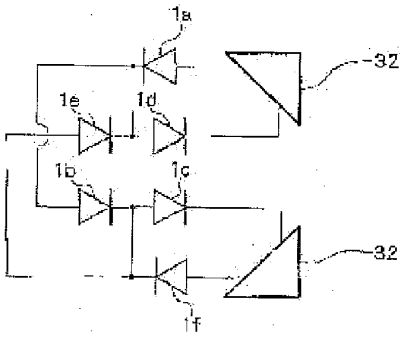
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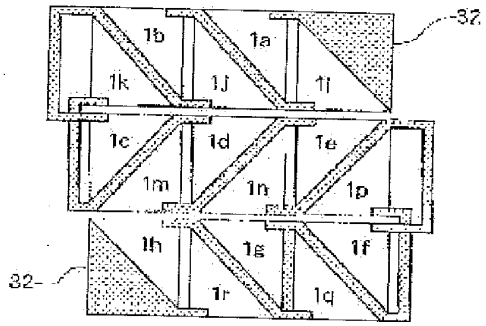
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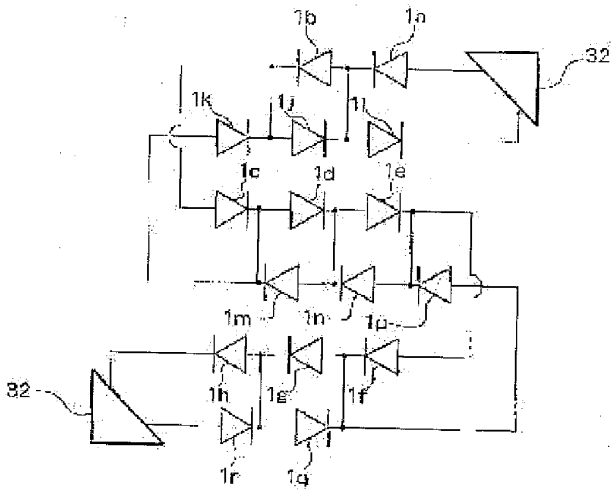
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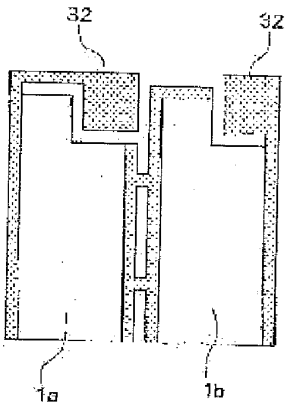
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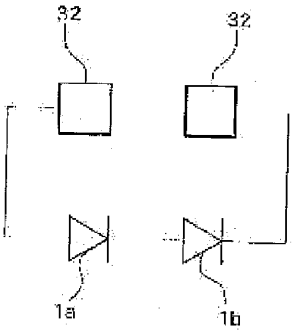
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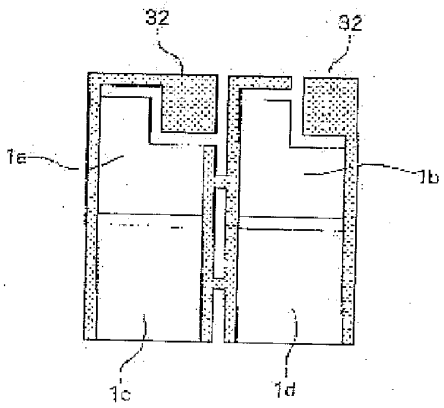
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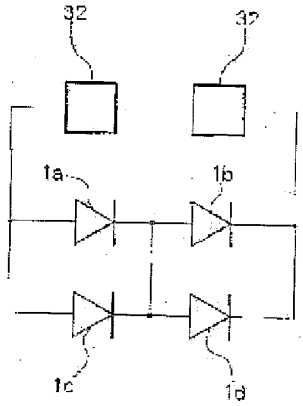
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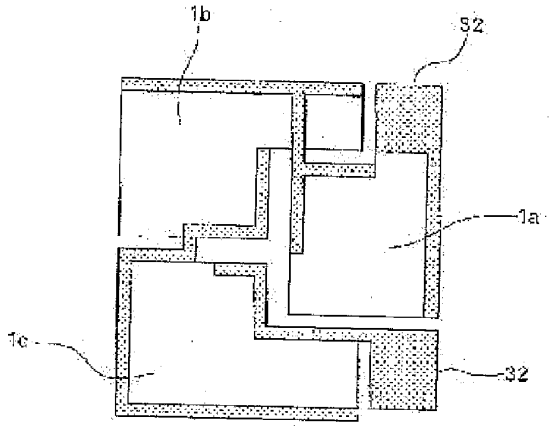
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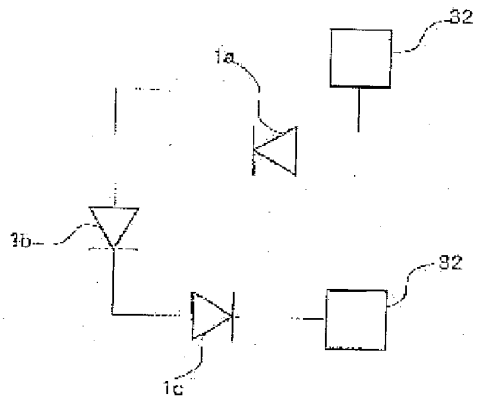
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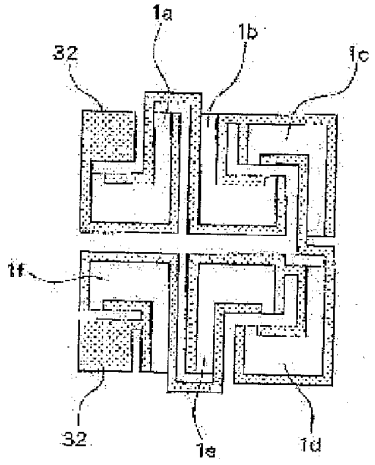
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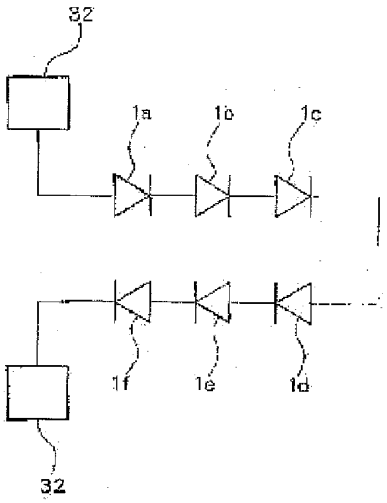
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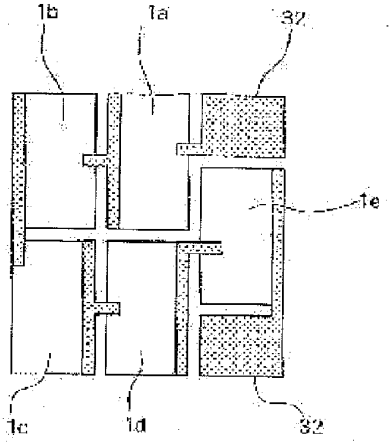
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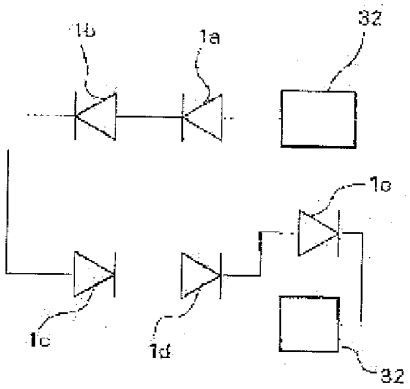
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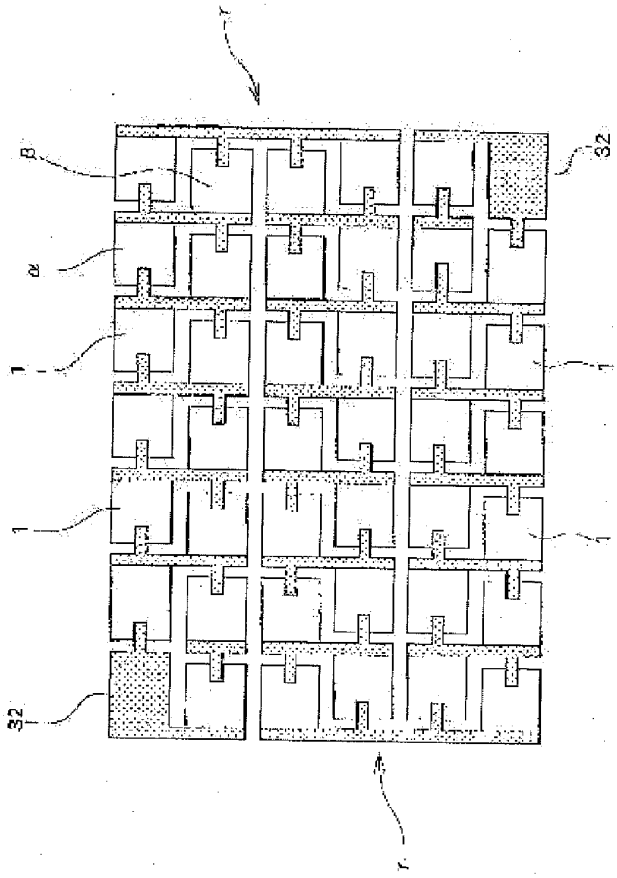
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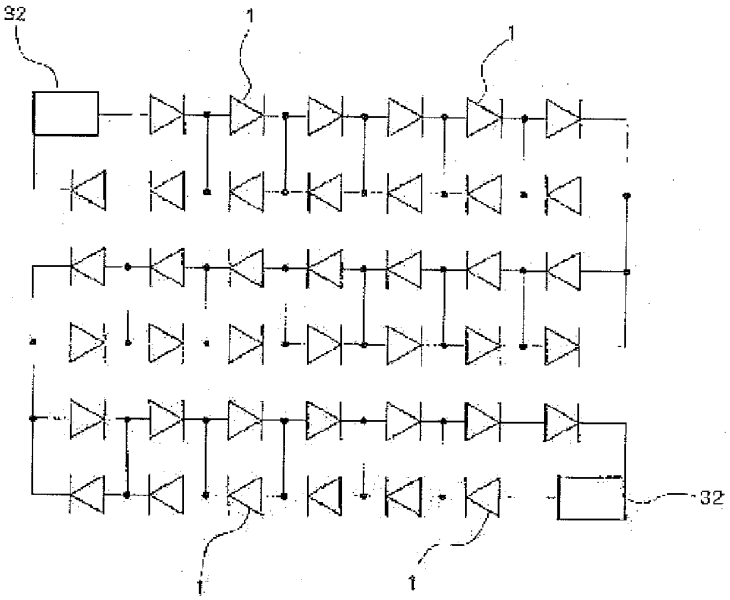
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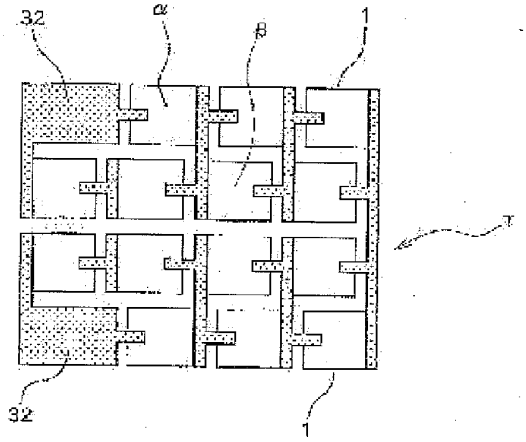
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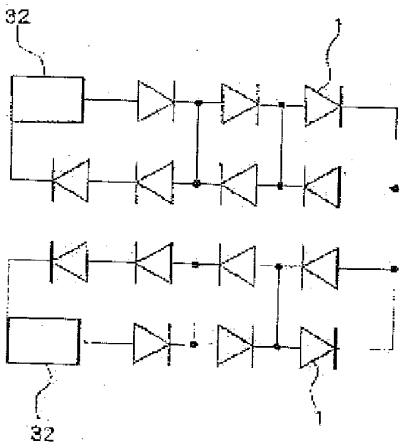
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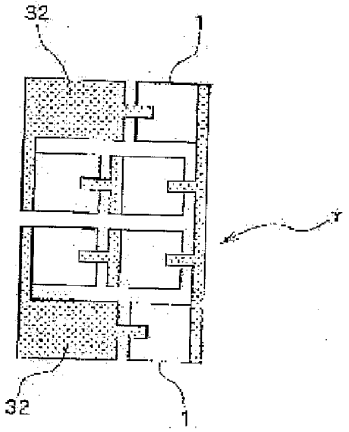
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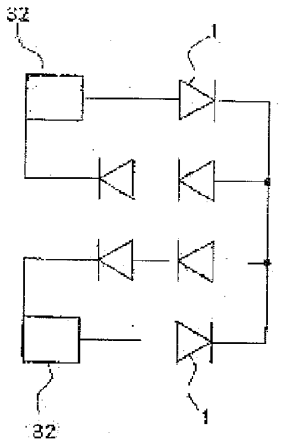
도면29



도면30



도면31



Electronic Acknowledgement Receipt

EFS ID:	3698749
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
Receipt Date:	30-JUL-2008
Filing Date:	26-DEC-2007
Time Stamp:	13:06:09
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed	US_IDS_Form_SB_08a.pdf	924804 4864beb2ddd7230ade39e13883630c40b70acdf2	no	4

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2	Foreign Reference	JP2004-079867.pdf	644961 145508d5e2da7b8f8e28d86c10d3de10d44e6f05	no	14
Warnings:					
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3	Foreign Reference	KR10-2003-0022940.pdf	534219 1ab38350b61bf9b799c106c834af091a84471751	no	9
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4	Foreign Reference	KR10-2005-0052474.pdf	817943 f3408bf67902a3b6997602076641db972ecc63fd	no	24
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(Not for submission under 37 CFR 1.99)

Application Number	11993965
Filing Date	2007-12-26
First Named Inventor	Jong Lam LEE
Art Unit	2811
Examiner Name	To be determined
Attorney Docket Number	P2317US00

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	1	20040075399		2004-04-22	David HALL	

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	1	1020060037589	KR		2006-05-03	Seoul Semiconductor Co Ltd		☐
	2	2002026378	JP		2002-01-25	Kyocera Corp		☐
	3	1020050066358	KR		2005-06-30	Samsung Electro-Mechanics Co Ltd		☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
	Art Unit	2811
	Examiner Name	To be determined
	Attorney Docket Number	P2317US00

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
	Art Unit	2811
	Examiner Name	To be determined
	Attorney Docket Number	P2317US00

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2008-08-29
Name/Print	Hae-Chan Park	Registration Number	50,114

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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(19) KOREAN INTELLECTUAL PROPERTY OFFICE

KOREAN PATENT ABSTRACTS

(11)Publication number: 1020050066358 A
(43)Date of publication of application: 30.06.2005

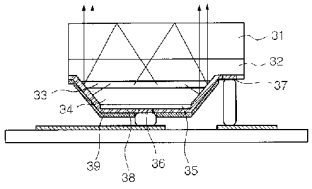
(21)Application number: 1020030097634
(22)Date of filing: 26.12.2003
(30)Priority: ..

(51)Int. Cl H01L 33/00

(71)Applicant: SAMSUNG ELECTRO-MECHANICS CO., LTD.
(72)Inventor: HAN, KYUNG TAEG
PARK, YOUNG HO

(54) NITRIDE SEMICONDUCTOR LIGHT EMITTING DEVICE FOR FLIP CHIP AND FABRICATING METHOD THEREOF TO IMPROVE LIGHT EMITTING EFFICIENCY OF NITRIDE LIGHT EMITTING DEVICE OF FLIP-CHIP STRUCTURE

(57) Abstract:



PURPOSE: A nitride semiconductor light emitting device for a flip chip is provided to improve light emitting efficiency of a nitride light emitting device of a flip-chip structure, by etching an active layer and p-type nitride semiconductor layer formed on the active layer to form a mesa-type ridge structure, by forming a separate ARC(anti-reflective coating) on the upper surface and the inclined surface of the ridge and by reflecting the light emitted from the lateral surface of the light emitting device toward a substrate. CONSTITUTION: A gallium nitride-based semiconductor material is grown on a substrate(31). An n-type nitride semiconductor layer(32) is formed on the substrate, and a mesa-type ridge structure is formed in a partial region on the upper surface of the n-type nitride semiconductor layer. An active layer(33) and a p-type nitride semiconductor layer(34) are sequentially formed on the mesa-type ridge structure of the n-type nitride semiconductor layer to form a mesa-type ridge structure extended from the mesa-type ridge structure of the n-type nitride semiconductor layer. An n electrode is formed on the n-type nitride semiconductor layer. A p bonding electrode(36) is formed on the ridge structure. An insulation layer(38) is formed on the n-type nitride semiconductor layer and the upper surface and inclined surface of the ridge structure to expose the n electrode and the p bonding electrode. An ARC(39) is formed on the insulation layer in a manner that the n electrode and the p bonding electrode are exposed.

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(54) 플립칩용 질화물 반도체 발광소자 및 그 제조방법

요약

본 발명은 플립칩 구조로 사용되는 질화물 반도체 발광소자 및 그 제조방법에 관한 것이다. 질화갈륨계 반도체 물질을 성장시키기 위한 기판과, 상기 기판 상에 형성되며, 그 상면 일부영역에 메사형 리지구조가 형성된 n형 질화물 반도체층과, 상기 n형 질화물 반도체층의 메사형 리지구조 상에, 상기 n형 질화물 반도체층의 메사형 리지구조가 연장되는 메사형 리지구조를 갖도록 순차적으로 형성된 활성층 및 p형 질화물 반도체층과, 상기 n형 질화물 반도체층 상에 형성되는 n측 전극과, 상기 리지구조 상에 형성되는 p측 본딩전극과, 상기 n측 전극 및 p측 본딩전극이 노출되도록 상기 n형 질화물 반도체층 및 상기 리지구조의 상면과 경사면 상에 형성되는 절연막 및 상기 절연막 상에, 상기 n측 전극 및 p측 본딩전극이 노출되도록 형성되는 반사막을 포함하는 플립칩용 질화물 반도체 발광소자를 제공한다. 본 발명에 따르면, 플립칩 구조로 사용되는 질화물 발광소자의 발광효율을 향상시킬 수 있는 효과가 있다.

대표도

도 2

색인어

플립칩, 질화물, 반도체, 발광소자, 반사막, 절연막, 메사형, 리지

명세서

도면의 간단한 설명

도 1은 종래의 플립칩용 질화물 반도체 발광소자의 단면도이다.

도 2는 본 발명에 따른 플립칩용 질화물 반도체 발광소자의 단면도이다.

도 3a-3h는 본 발명에 따른 플립칩용 질화물 반도체 소자의 제조방법을 도시한 공정사시도 및 공정단면도이다.

도면의 주요부분에 대한 부호의 설명

31, 41 : 기판 32, 42 : n형 질화물 반도체층

33, 43 : 활성층 34, 44 : p형 질화물 반도체층

35, 45 : 반사전극층 36, 46 : p측 본딩전극

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37, 47 : n측 본딩전극 38, 48 : 절연막

39, 49 : 반사막

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 질화물 반도체 발광소자 및 그 제조방법에 관한 것으로, 보다 상세하게는 플립칩으로 사용되는 질화물 반도체 발광소자에서, 활성층과 활성층 상부에 형성되는 p형 질화물 반도체층을 메사형 리지구조로 에칭하고, 상기 리지구조의 상면 및 경사면에 별도의 반사막을 형성하여, 발광소자의 측면으로 방출되는 빛을 반사시켜 기판 측으로 방출되게 함으로써 질화물 발광소자의 휘도를 향상시킬 수 있는 반사막을 구비한 플립칩용 질화물 반도체 발광소자 및 그 제조방법에 관한 것이다.

근래에 새로운 영상정보를 전달매체로 부각되고 있는 LED(발광소자) 전광판은 초기에는 단순 문자나 숫자정보로 시작하여 현재는 각종 CF 영상물, 그래픽, 비디오 화면 등 동화상을 제공하는 수준까지 이르게 되었다. 색상도 기존 단색의 조잡한 화면 구현에서 적색과 황록색 LED등으로 제한된 범위의 색상 구현을 했었고, 최근에는 질화물 반도체를 이용한 고휘도 청색 LED가 등장함에 따라 적색, 황록색, 청색을 이용한 총천연색 표시가 비로소 가능하게 되었다. 그러나 황록색 LED가 적색 LED, 청색 LED보다 휘도가 낮고 발광 파장이 565nm 정도로 빛의 삼원색에서 필요한 파장의 녹색이 아니기 때문에 자연스러운 총천연색 표현은 불가능하였으나, 이후, 자연스러운 총천연색 표시에 적합한 파장 525nm 고휘도 순수 녹색 질화물 반도체 LED를 생산함으로써 해결되었다.

이와 같이, 질화물 반도체 물질은 청색 또는 녹색 파장대의 광을 얻기 위한 발광소자에 사용되고 있으며, $Al_xIn_yGa_{(1-x-y)}N$ 조성식(여기서, $0\leq x\leq 1$, $0\leq y\leq 1$, $0\leq x+y\leq 1$임)을 갖는다.

현재, 상기 질화물 반도체 발광소자를 차세대 조명 장치로 사용하기 위해 고휘도 특성을 갖는 질화물 반도체 발광소자의 개발이 요구되고 있으며, 이러한 요구를 만족시키기 위한 종래의 기술로는 다음과 같은 기술이 제안되고 있다.

종래의 질화물 반도체 발광소자는, 기판 상에 순차적으로 형성된 n형 질화물 반도체층, 다중우물구조인 활성층 및 p형 질화물 반도체층을 포함하며, 상기 p형 질화물 반도체층과 활성층은 그 일부영역이 제거되어 n형 질화물 반도체층의 일부상면이 노출된 구조를 갖는다. 상기 노출된 n형 질화물 반도체층의 상면에 n측 전극이 형성되고, 상기 p형 질화물 반도체층 상에는 오믹 접촉을 형성하고 전류 주입 효율을 향상시키기 위한 p 메탈층을 형성한 후에, 상기 p 메탈층의 상면에 p측 본딩전극을 형성한다. 이와 같은 종래의 질화물 반도체 발광소자는 상기 활성층에서 생성되는 빛을 상기 p 메탈층 방향을 방출한다.

상기 p 메탈층은 투광성을 가지면서 접촉저항을 개선하여 전류 주입 효율을 향상시키기 위한 층으로서, 일반적으로 Ni/Au의 이중층을 사용한다. 상기 Ni/Au의 이중층은 빛의 투과율이 상대적으로 좋은 금속층으로서, 이를 100Å 이하로 얇게 증착시켜서 발광소자 내부에서 발생한 빛이 금속을 투과하여 외부로 방출된다. 이러한 Ni/Au의 이중층은 전류 주입 효율을 향상시키기 위해서는 가능한 두껍게 형성하는 것이 바람직하지만, 금속을 이용하여 투명전극을 형성하므로 원하는 투광성을 얻는데 문제가 될 수 있다. 비록, 열처리 과정을 통해 비교적 높은 투광성을 갖게 되더라도 그 투과율은 약 60%에 불과하므로, Ni/Au의 이중층의 두께가 증가할 경우에 휘도가 저하될 수 있다. 따라서, 이러한 Ni/Au의 이중층은 두께의 제약을 받을 수 밖에 없으며, 이로 인해 전류 주입 효율을 향상시키는데 한계가 있다.

상기와 같은 종래의 질화물 반도체 발광소자의 문제점을 해결하기 위해 도 1에 도시된 것과 같은 플립칩(flip-chip) 방식의 질화물 반도체 발광소자가 제안되었다. 이 플립칩 방식의 질화물 반도체 발광소자는 도 1에 도시된 바와 같이, 기판(11) 상에 순차적으로 형성된 n형 질화물 반도체층(12), 다중우물구조인 활성층(13) 및 p형 질화물 반도체층(14)을 포함하며, 상기 p형 질화물 반도체층(14)과 활성층(13)은 그 일부영역이 제거되어 n형 질화물 반도체층(12)의 일부상면이 노출된 구조를 갖는다. 상기 노출된 n형 질화물 반도체층(12)의 상면에 n측 전극(17)이 형성되고, 상기 p형 질화물 반도체층(14) 상에 반사율이 좋은 Al, Ag 등을 사용한 p 메탈층(15)을 형성한 후에, 상기 p 메탈층(15)의 상면에 p측 본딩전극(16)을 형성한다. 이와 같이 형성된 질화물 반도체 발광소자를 뒤집어서, 상기 n측 전극(17) 및 p측 본딩전극(16)을, 범프(23)를 사용하여 서브마운트(submount)(21) 상의 도전성 패턴(22)과 연결하여 사용한다. 상기 플립칩 방식의 질화물 반도체 발광소자는 상기 p 메탈층(25)으로 반사율이 좋은 금속을 채용하여 전극방향으로 향하는 빛을 반사시켜 투명한 기판 쪽으로 방출되도록 함으로써 휘도를 향상시킬 수 있으며, 전극을 통해 소자 내에서 발생한 열을 외부로 쉽게 방출할 수 있다.

그러나, 이와 같은 종래의 플립칩용 질화물 반도체 발광소자는, 발광소자의 측면으로 방출되는 빛(L)이 존재한다. 플립칩용 질화물 반도체 발광소자는 상기 활성층(13)에서 생성되는 빛이 기판(11)측으로 방출되는 것이 반도체 발광소자의 발광효율에 있어 가장 바람직하지만, 도 1에 도시된 것과 같이 발광소자의 측면으로 방출되는 빛(L)이 존재하기 때문에 종래의 질화물 발광소자는 발광효율이 저하되는 문제점이 발생한다.

따라서, 당 기술분야에서는, 플립칩용 질화물 반도체 발광소자의 측면으로 방출되는 빛을 기판 측으로 방출될 수 있게 하여 발광효율을 개선할 수 있는 새로운 플립칩용 질화물 반도체 발광소자의 개발이 요구되고 있는 실정이다.

발명이 이루고자 하는 기술적 과제

본 발명은 이러한 기술적 요구를 충족시키기 위해 안출된 것으로, 그 목적은, 플립칩으로 사용되는 질화물 반도체 발광소자에서, 활성층과 활성층 상부에 형성되는 p형 질화물 반도체층을 메사형 리지구조로 에칭하고, 상기 리지의 상면 및 경사면에 별도의 반사막을 형성하여, 발광소자의 측면으로 방출되는 빛을 반사시켜 기판 측으로 방출되게 함으로써 질화물 발광소자의 발광효율을 향상시킬 수 있는 반사막을 이용한 플립칩용 질화물 반도체 발광소자 및 그 제조방법을 제공하는 것이다.

발명의 구성 및 작용

상기 기술적 과제를 달성하기 위해 본 발명은,

질화갈륨계 반도체 물질을 성장시키기 위한 기판;

상기 기판 상에 형성되며, 그 상면 일부영역에 메사형 리지구조가 형성된 n형 질화물 반도체층;

상기 n형 질화물 반도체층의 메사형 리지구조 상에, 상기 n형 질화물 반도체층의 메사형 리지구조가 연장되는 메사형 리지구조를 갖도록 순차적으로 형성된 활성층 및 p형 질화물 반도체층;

상기 n형 질화물 반도체층 상에 형성되는 n측 전극;

상기 리지구조 상에 형성되는 p측 본딩전극;

상기 n측 전극 및 p측 본딩전극이 노출되도록 상기 n형 질화물 반도체층 및 상기 리지구조의 상면과 경사면 상에 형성되는 절연막; 및

상기 절연막 상에, 상기 n측 전극 및 p측 본딩전극이 노출되도록 형성되는 반사막을 포함하는 플립칩용 질화물 반도체 발광소자를 제공한다.

상기 반사막은 Rh, Al, Ag, Pt, Pd 및 Ti로 구성된 그룹으로부터 선택된 하나의 금속 또는 둘 이상 금속의 합금으로 이루어질 수 있다.

바람직하게, 상기 본 발명에 따른 플립칩용 질화물 반도체 발광소자는 상기 p형 질화물 반도체층 상에 형성되는 반사전극층을 더 포함할 수 있다.

또한, 본 발명은 상기 플립칩용 질화물 반도체 발광소자의 제조방법도 제공한다. 본 발명에 따른 방법은,

질화물 반도체 물질을 성장시키기 위한 기판을 마련하는 단계;

상기 기판 상에, n형 질화물 반도체층과, 활성층과, p형 질화물 반도체층을 순차적으로 형성하는 단계;

상기 n형 질화물 반도체층의 적어도 일부 영역이 노출되도록 상기 p형 질화물 반도체층, 상기 활성층 및 상기 n형 질화물 반도체층의 일부를 제거하여 메사형 리지구조를 형성하는 단계;

상기 리지구조 상에 p측 본딩전극을 형성하며, 상기 n형 질화물 반도체층의 노출된 영역에 n측 전극을 형성하는 단계;

상기 p측 본딩전극 및 n측 전극이 노출되도록 상기 n형 질화물 반도체층, 상기 반사전극층 및 상기 리지구조의 경사면 상에 절연막을 형성하는 단계; 및

상기 절연막 상에, 상기 n측 전극 및 p측 본딩전극이 노출되도록 반사막을 형성하는 단계를 포함한다.

바람직하게, 본 발명에 따른 플립칩용 질화물 반도체 발광소자는, 상기 p형 질화물 반도체층 상면에 반사전극층을 형성하는 단계를 더 포함할 수 있다.

상기 반사막을 형성하는 단계는, 상기 절연막 상에, Rh, Al, Ag, Pt, Pd 및 Ti로 구성된 그룹으로부터 선택된 하나의 금속 또는 둘 이상 금속의 합금을, 500Å 내지 5000Å의 두께로 증착시키는 단계인 것이 바람직하다.

이하, 첨부된 도면을 참조하여 본 발명의 일실시형태에 따른 플립칩용 질화물 반도체 소자 및 그 제조방법에 대해 보다 상세하게 설명하기로 한다.

도 2는 본 발명의 일실시형태에 따른 플립칩용 질화물 반도체 발광소자의 단면도이다. 도 2는 본 발명의 일실시형태에 따른 플립칩용 질화물 반도체 소자를 뒤집어서 서브마운트에 적용시킨 일례를 도시한 것으로, 이하에서는 발광소자를 서브마운트에 적용하기 이전의 상태, 즉 기판(31)이 최하부에 위치한 상태의 발광소자에 대해 설명하기로 한다.

도 2를 참조하면, 본 발명에 따른 플립칩용 질화물 반도체 발광소자는, 질화갈륨계 반도체 물질을 성장시키기 위한 기판(31)과, 상기 기판(31) 상에 형성되며, 그 상면 일부영역에 메사형 리지구조가 형성된 n형 질화물 반도체층(32)과, 상기 n

형 질화물 반도체층(32)의 메사형 리지구조 상에, 상기 n형 질화물 반도체층의 메사형 리지구조가 연장되는 메사형 리지구조를 갖도록 순차적으로 형성된 활성층(33) 및 p형 질화물 반도체층(34)과, 상기 p형 질화물 반도체층(34) 상에 형성된 반사전극층(35)과, 상기 n형 질화물 반도체층(32) 상에 형성되는 n측 전극(37)과, 상기 리지구조 상면에 형성되는 p측 본딩전극(36)과, 상기 n측 전극(37) 및 p측 본딩전극(36)이 노출되도록 상기 n형 질화물 반도체층 및 상기 리지구조의 상면과 경사면 상에 형성되는 절연막(38) 및 상기 절연막(38) 상에, 상기 n측 전극(37) 및 p측 본딩전극(36)이 노출되도록 형성되는 반사막(39)을 포함하여 구성된다.

상기 기판(31)은, 사파이어 기판이나 SiC 기판을 사용하며, 특히 사파이어 기판이 대표적으로 사용된다. 이는 상기 기판(31) 위에 성장되는 질화물 반도체 물질의 결정과, 결정구조가 동일하면서 격자정합을 이루는 상업적인 기판이 존재하지 않기 때문이다.

상기 n형 질화물 반도체층(32)은 $Al_xIn_yGa_{(1-x-y)}N$ 조성식(여기서, $0\leq x\leq 1$, $0\leq y\leq 1$, $0\leq x+y\leq 1$임)을 갖는 n 도핑된 반도체 물질로 이루어질 수 있으며, 특히 GaN가 널리 사용된다. n형 질화물 반도체층(32)은, 상기 반도체 물질을 MOCVD(Metal Organic Chemical Vapor Deposition)법 또는 MBE(Molecular Beam Epitaxy)법과 같은 공지의 증착공정을 사용하여 기판 상에 성장시킴으로써 형성된다. 상기 사파이어 기판 상에 질화물 반도체 물질을 성장시키는 경우, 격자부정합에 의한 스트레스(stress)로 양질의 결정성장을 기대하기 어렵기 때문에 버퍼층(buffer layer)이라고 하는 저온성장층을 먼저 기판 상에 형성할 수도 있다. 상기 버퍼층은 GaN 등과 같은 물질로 이루어질 수 있다. 상기 n형 질화물 반도체층(32)의 일부영역에는 그 상면이 비교적 넓고 높이가 낮은 메사형 리지구조가 형성된다. 상기 n형 질화물 반도체층(32)에 형성된 메사형 리지구조 상에 이후 활성층(33)과 p형 질화물 반도체층(34)이 순차적으로 형성된다. 이 때, 활성층(33)과 p형 질화물 반도체층(34)은 상기 n형 질화물 반도체층에 형성된 리지구조가 연장된 메사형 리지구조를 갖는다.

상기 활성층(33)은 양자우물구조를 가지며 GaN 또는 InGaN으로 이루어 질 수 있다.

상기 p형 질화물 반도체층(34)은 상기 n형 질화물 반도체층(32)과 마찬가지로, $Al_xIn_yGa_{(1-x-y)}N$ 조성식(여기서, $0\leq x\leq 1$, $0\leq y\leq 1$, $0\leq x+y\leq 1$임)을 갖는 질화물 반도체 물질로 이루어지며, 상기 질화물 반도체 물질은 p 도핑된다. 상기 n형 질화물 반도체층과 마찬가지로 p형 질화물 반도체층(34)은, 질화물 반도체 물질을 MOCVD법 또는 MBE법과 같은 공지의 증착공정을 사용하여 상기 활성층(33)의 상면에 성장된다.

본 발명에서는 상기 활성층(33)과 p형 질화물 반도체층(34)이 메사형 리지구조를 갖도록 형성되는 특징이 있다. 이는 이후에 리지구조의 경사면에 반사막(39)이 형성됨으로써 상기 반사막(39)에 의해 반사되는 빛이 발광소자의 기판측으로 방출될 수 있게 한다. 상기 리지구조의 경사면은 n형 질화물 반도체층의 일부까지 형성된다. 종래의 질화물 반도체 발광소자에서는 p형 질화물 반도체층을 형성한 이 후, p형 질화물 반도체층 및 활성층의 일부(특히 모서리부분)를 제거하여 n형 질화물 반도체층의 일부영역이 노출되게 한다. 본 발명에서는 상기 활성층(33)과 p형 질화물 반도체층(34)을 적층한 후 메사형 리지구조로 p형 질화물 반도체층, 활성층 및 n형 질화물 반도체층의 일부를 에칭하여 제거함으로써, n형 질화물 반도체층의 일부 영역이 노출될 수 있다.

상기 반사전극층(35)은 상기 p형 질화물 반도체층(34) 상에 형성된다. 상기 반사전극층(35)은 활성층(33)에서 생성된 빛을 기판(31)측으로 반사함과 동시에, p형 질화물 반도체층(34)과의 오믹 접촉을 형성하기 위한 것이다. 상기 반사전극층(35)의 재료로는 반사율이 우수한 금속인 Rh, Al, Ag, Pt, Pd 및 Ti로 구성된 그룹으로부터 선택된 하나의 금속 또는 둘 이상 금속의 합금이 채택될 수 있다.

상기 반사전극층(35)의 상면에는 p측 본딩전극(36)이 형성되며, 상기 활성층(33) 및 p형 질화물 반도체층(34)의 에칭을 통해 노출되는 n형 질화물 반도체층(32) 상에는 n측 전극(37)이 형성된다. 도 2와 같이, 상기 p측 본딩전극(36)과 n측 전극(37)은 범프를 이용하여 서브마운트 상의 도전 패턴과 연결되어 발광소자에 전원을 제공한다.

상기 절연막(38)은 상기 리지구조의 상면과 경사면 및 노출된 n형 질화물 반도체층 상에 형성된다. 이 때, n측 전극(37)과 p측 본딩전극(36)은 서브마운트와의 전기적 연결을 위해 노출된다. 상기 절연막(38)은 질화물 반도체 발광소자의 표면을 보호하고, 전기적 절연을 위해 형성되는 것으로 통상 SiO_2와 같은 절연물질로 이루어진다.

상기 반사막(39)은 상기 절연막(38)의 상에 형성된다. 즉, 리지구조의 상면과 경사면 및 노출된 n형 질화물 반도체층의 상부에 반사막이 형성된다. 종래의 플립칩용 반도체 발광소자는 반사전극층만 구비하므로, 활성층에서 생성된 빛이 반사전극층으로 거의 수직으로 입사하는 경우에만 기판측으로 빛을 반사할 수 있었다. 즉, 각도를 가지고 반사전극층으로 입사하는 빛은 기판측으로 방출되지 못하고, 발광소자의 측면으로 방출되어 빛의 손실이 발생하였다. 또한 발광층에서 발광소자의 측면으로 방출되는 빛은 반사하지 못하였다. 이에 비해, 본 발명에 따른 반사막(39)은 메사형 리지구조의 경사면까지 형성됨으로써, 리지의 경사면 측으로 방출되는 빛을 기판측으로 반사시킬 수 있어, 빛의 손실을 감소시킬 수 있다.

도 3a 내지 도 3h는 이상에서 설명한 본 발명의 일실시예에 따른 플립칩용 질화물 반도체 발광소자의 제조방법을 설명하기 위한 공정사시도 및 공정단면도이다.

본 발명의 일실시예에 따른 플립칩용 질화물 반도체 발광소자의 제조방법은, 먼저 도 1과 같이, 질화물 반도체 물질을 성장시키기 위한 기판(41)을 마련한 후, 상기 기판 상(41)에, n형 질화물 반도체층(42)과, 활성층(43)과, p형 질화물 반도체층(44)을 순차적으로 형성한다. 상기 기판(41)은 사파이어 기판일 수 있으며, 상기 n형 질화물 반도체층(42), 활성층(43) 및 p형 질화물 반도체층(44)은 MOCVD법 또는 MBE법과 같은 공지의 증착공정을 사용하여 성장될 수 있다.

이어, 도 3b와 같이, 에칭을 통해 n형 질화물 반도체층(42)의 일부 및 활성층(43)과 p형 질화물 반도체층(44)의 일부를 제거하여 메사형 리지구조를 형성하고 n형 질화물 반도체층(45)의 일부를 노출시키기 위해, p형 질화물 반도체층(44) 상면에 에칭이 이루어지지 않는 부분에 포토 레지스트(51)를 형성한다. 상기 포토 레지스트(51)가 형성된 부분은 이 후 에칭을 통해 형성되는 리지구조의 상면이 되는 부분이다.

이어, 도 3c와 같이 에칭을 통해 활성층(43)과 p형 질화물 반도체층(44) 및 n형 질화물 반도체층(42)의 일부를 제거하여 리지구조를 형성하고, n형 질화물 반도체층(42)의 일부영역을 노출시킨 후 상기 포토 레지스트(51)를 제거한다. 에칭은 드라이에칭 공정을 이용하는 것이 바람직하다. 상기 드라이에칭은 높은 분해능과 평탄화 기술에 필수 불가결한 에칭단면의 이방적 특성을 제공하는 것으로, 그 방법에는 플라즈마 에칭, 리액티브 이온 에칭, 리액티브 이온 빔 에칭 등이 있으며, 이들 대부분이 불활성 이온과 반응성 가스를 사용하여 에칭 단면의 이방적 특성을 제공한다.

다음으로, 도 3d와 같이 상기 메사형 리지구조 상면에 반사전극층(45)을 형성하고, 상기 반사전극층(45)의 상면에 p측 본딩전극(46)을 형성하며, 상기 노출된 n형 질화물 반도체층(42)의 상면에 n측 전극(47)을 형성한다. 상기 반사전극층(45), p측 본딩전극(46) 및 n측 전극(47)은, 전자빔 증착법과 같은 증착공정에 의해 형성될 수 있다.

본 발명의 보다 명확한 이해를 위해, 이후에 설명되는 공정은, 도 3e 내지 도 3h는 도 3d의 A-A'선을 따라 절개한 공정 단면도를 통해 설명된다.

다음으로, 도 3e와 같이, 상기 n형 질화물 반도체층, 상기 반사전극층 및 상기 리지구조의 경사면 상에 절연막(48)을 형성한다. 즉, 현재공정까지 제작된 발광소자 상면 전체에 절연막(48)을 형성한다. 상기 절연막(48)은, SiO_2와 같은 절연물질로 이루어지며, 발광소자의 표면보호와 전기적 절연을 위해 형성된다. 이 때, p측 본딩전극(46)과 n측 전극(47)은 소자에 전류를 공급하여야 하므로, p측 본딩전극(46)과 n측 전극(47)의 상면에 형성된 절연막은 제거되어야 한다. 따라서, p측 본딩전극(46)과 n측 전극(47)의 상면에 형성된 절연막 영역을 제외한 영역에 포토 레지스트(52)를 형성하고, 에칭 공정을 통해 p측 본딩전극(46)과 n측 전극(47)의 상면에 형성된 절연막을 제거한 후 포토 레지스트를 제거한다. p측 본딩전극(46)과 n측 전극(47)의 상면에 형성된 절연막이 제거된 상태가 도 3f에 도시되어 있다.

이어, 도 3g와 같이 p측 본딩전극(46)과 n측 전극(47)의 상면에 포토 레지스트(53)를 형성한 후, 전자빔 증착법과 같은 증착공정을 통해 반사막(49)을 형성한다. 상기 포토 레지스트(53)가 p측 본딩전극(46)과 n측 전극(47)의 상면에 형성되므로, p측 본딩전극(46)과 n측 전극(47)의 상면에는 상기 반사막(49)이 형성되지 않는다.

최종적으로, 도 3h와 같이 포토레지스트를 제거하면, p측 본딩전극(46)과 n측 전극(47)이 외부와의 연결을 위해 노출되고, 메사형 리지구조의 경사면까지 반사막(49)이 형성되어 발광소자의 측면으로 손실되는 빛을 기판(41)측으로 반사하여 발광효율을 높일 수 있는 플립칩용 질화물 반도체 발광소자가 완성된다.

이와 같이, 본 발명은 상술한 실시형태 및 첨부된 도면에 의해 한정되는 것이 아니고, 첨부된 청구범위에 의해 한정하고자 하며, 청구범위에 기재된 본 발명의 기술적 사상을 벗어나지 않는 범위 내에서 다양한 형태의 치환, 변형 및 변경이 가능하다는 것은 당 기술분야의 통상의 지식을 가진 자에게는 자명할 것이다.

발명의 효과

상술한 바와 같이, 본 발명에 따르면, 활성층과 활성층 상부에 형성되는 p형 질화물 반도체층을 메사형 리지구조로 에칭하고, 상기 리지의 상면 및 경사면에 별도의 반사막을 형성하여, 발광소자의 측면으로 방출되는 빛을 반사시켜 기판측으로 방출되게 함으로써 플립칩 구조로 사용되는 질화물 발광소자의 발광효율을 향상시킬 수 있는 우수한 효과가 있다.

(57) 청구의 범위

청구항 1.

질화갈륨계 반도체 물질을 성장시키기 위한 기판;

상기 기판 상에 형성되며, 그 상면 일부영역에 메사형 리지구조가 형성된 n형 질화물 반도체층;

상기 n형 질화물 반도체층의 메사형 리지구조 상에, 상기 n형 질화물 반도체층의 메사형 리지구조가 연장되는 메사형 리지구조를 갖도록 순차적으로 형성된 활성층 및 p형 질화물 반도체층;

상기 n형 질화물 반도체층 상에 형성되는 n측 전극;

상기 리지구조 상에 형성되는 p측 본딩전극;

상기 n측 전극 및 p측 본딩전극이 노출되도록 상기 n형 질화물 반도체층 및 상기 리지구조의 상면과 경사면 상에 형성되는 절연막; 및

상기 절연막 상에, 상기 n측 전극 및 p측 본딩전극이 노출되도록 형성되는 반사막을 포함하는 플립칩용 질화물 반도체 발광소자.

청구항 2.

제1항에 있어서,

상기 반사막은 Rh, Al, Ag, Pt, Pd 및 Ti로 구성된 그룹으로부터 선택된 하나의 금속 또는 둘 이상 금속의 합금으로 이루어지는 것을 특징으로 하는 질화물 반도체 발광소자.

청구항 3.

제1항에 있어서,

상기 p형 질화물 반도체층 상에 형성되는 반사전극층을 더 포함하는 것을 특징으로 하는 질화물 반도체 발광소자.

청구항 4.

질화물 반도체 물질을 성장시키기 위한 기판을 마련하는 단계;

상기 기판 상에, n형 질화물 반도체층과, 활성층과, p형 질화물 반도체층을 순차적으로 형성하는 단계;

상기 n형 질화물 반도체층의 적어도 일부 영역이 노출되도록 상기 p형 질화물 반도체층, 상기 활성층 및 상기 n형 질화물 반도체층의 일부를 제거하여 메사형 리지구조를 형성하는 단계;

상기 리지구조 상에 p측 본딩전극을 형성하며, 상기 n형 질화물 반도체층의 노출된 영역에 n측 전극을 형성하는 단계;

상기 p측 본딩전극 및 n측 전극이 노출되도록 상기 n형 질화물 반도체층, 상기 반사전극층 및 상기 리지구조의 경사면 상에 절연막을 형성하는 단계; 및

상기 절연막 상에, 상기 n측 전극 및 p측 본딩전극이 노출되도록 반사막을 형성하는 단계를 포함하는 플립칩용 질화물 반도체 발광소자의 제조방법.

청구항 5.

제4항에 있어서,

상기 p형 질화물 반도체층 상면에 반사전극층을 형성하는 단계를 더 포함하는 것을 특징으로 하는 플립칩용 질화물 반도체 발광소자의 제조방법.

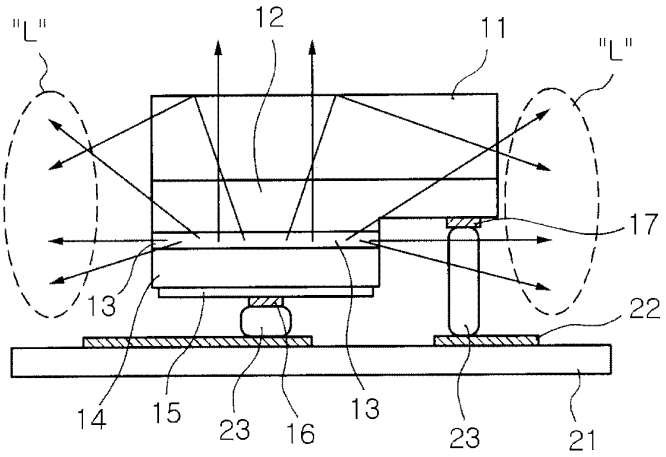
청구항 6.

제4항에 있어서,상기 반사막을 형성하는 단계는,

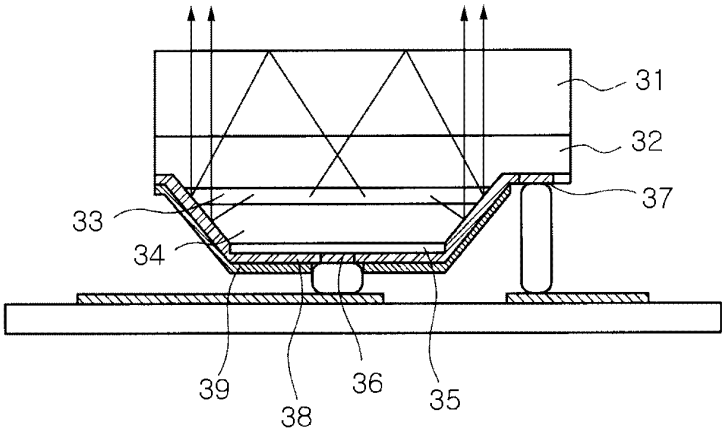
상기 절연막 상에, Rh, Al, Ag, Pt, Pd 및 Ti로 구성된 그룹으로부터 선택된 하나의 금속 또는 둘 이상 금속의 합금을 증착시키는 단계인 것을 특징으로 하는 플립칩용 질화물 반도체 발광소자.

도면

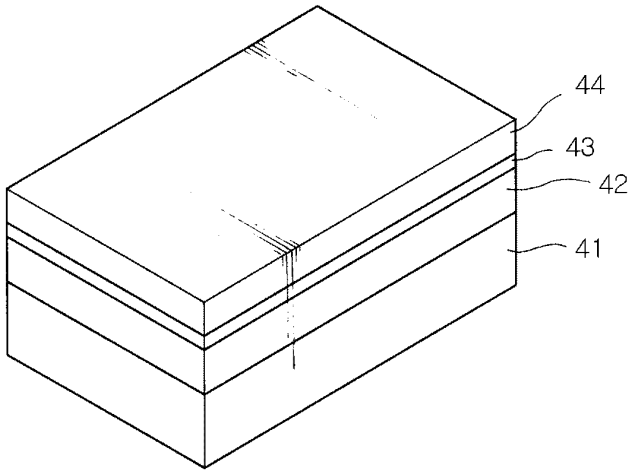
도면1


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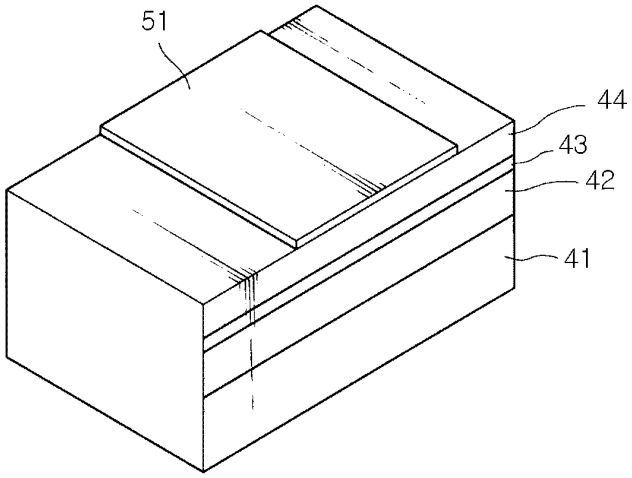
도면2


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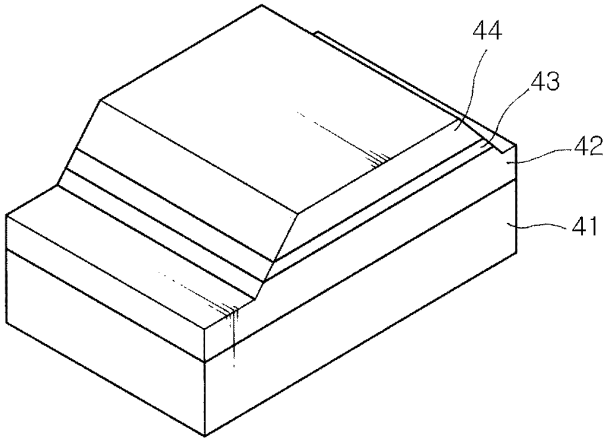
도면3a


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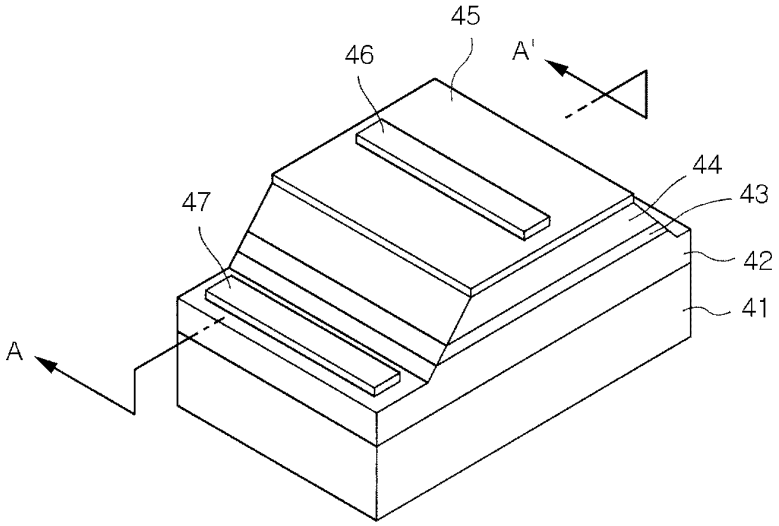
도면3b



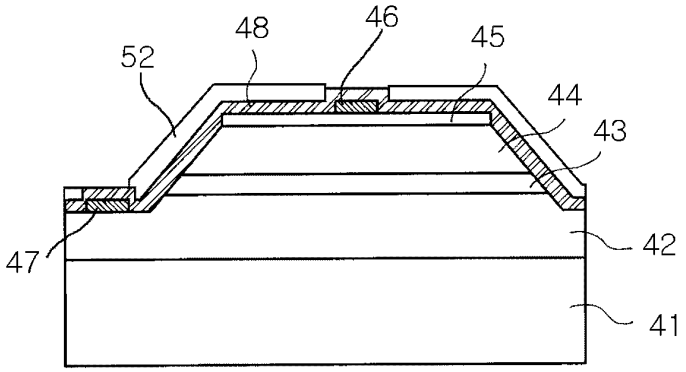
도면3c



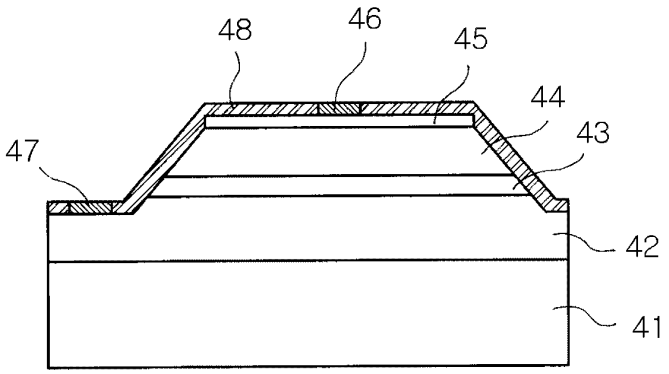
도면3d



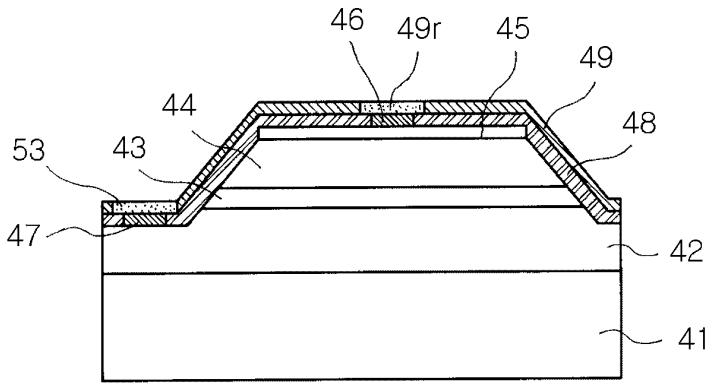
도면3e



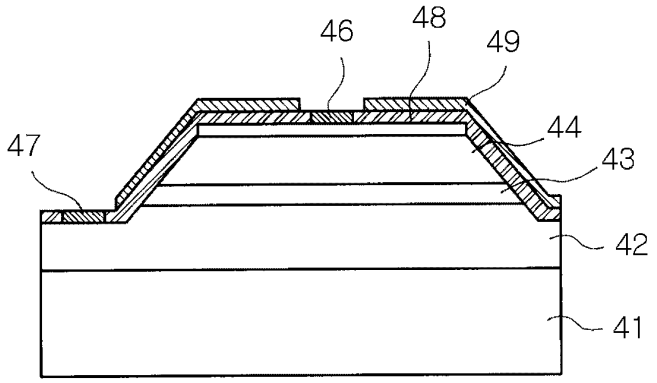
도면3f



도면3g



도면3h



PATENT ABSTRACTS OF JAPAN

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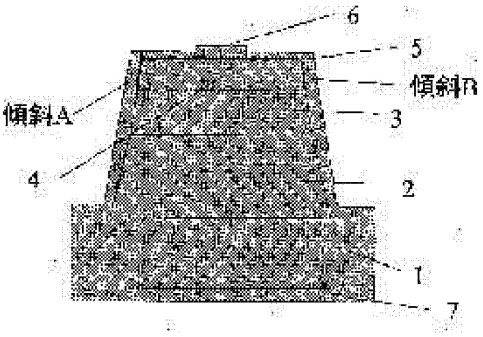
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(71)Applicant : KYOCERA CORP
(72)Inventor : KITADA KATSUNOBU
BITO YOSHIFUMI

(54) LIGHT EMITTING DIODE AND LED ARRAY HEAD

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a high performance light emitting diode by improving light emitting directivity in the light emitting body.
SOLUTION: A semiconductor buffer layer 2 is formed in a shape like an island on a single crystal substrate 1. A forward conductive semiconductor layer 3, a reverse conductive semiconductor layer 4, and an individual electrode 6 are sequentially formed on a semiconductor buffer layer 2 in the light emitting diode. The surrounding edge of the reverse conductive semiconductor layer 4 has an inclination with an inclination angle of 90 degrees or below to the single crystal substrate 1.



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(43)公開日　平成14年１月25日(2002.1.25)

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Ｈ０１Ｌ　33/00		Ｈ０１Ｌ　33/00	Ａ　５Ｆ０４１

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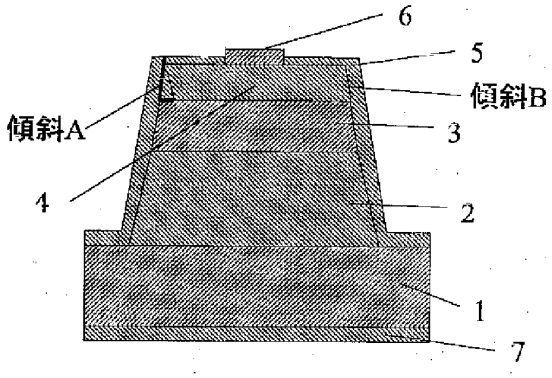
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最終頁に続く

(54)【発明の名称】　発光ダイオードおよびＬＥＤアレーヘッド

(57)【要約】
【課題】発光体内の発光の指向性を高め、高性能な発光ダイオードを提供する。
【解決手段】単結晶基板１上に半導体緩衝層２を島状に形成し、この半導体緩衝層２上に一導電型半導体層３と逆導電型半導体層４と個別電極６とを順次積層した発光ダイオードであって、逆導電型半導体層４の端面周囲に、単結晶基板１に対し９０°以下の傾斜角となるように勾配を設けた。



【特許請求の範囲】
【請求項１】単結晶基板上に半導体緩衝層を島状に形成し、この半導体緩衝層上に一導電型半導体層と逆導電型半導体層と電極とを順次積層した発光ダイオードであって、前記逆導電型半導体層の端面周囲に、単結晶基板に対し９０°以下の傾斜角となるように勾配を設けたことを特徴とする発光ダイオード。
【請求項２】請求項１の発光ダイオードに使用する単結晶基板がシリコンからなることを特徴とするＬＥＤアレーヘッド。
【請求項３】請求項１または請求項２の発光ダイオードを複数個にてアレイ状に配列してなるＬＥＤアレーヘッド。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明はメサ型構造を有する発光ダイオードに関し、特にページプリンタ用にて感光ドラムの露光用光源などに用いられる指向性が求められる発光ダイオードに関するものである。さらに、かかる発光ダイオードを複数個アレー状に配列してなるＬＥＤアレーヘッドに関する。
【０００２】
【従来の技術】従来の発光ダイオードを図１０と図１１に示す。図１０は発光ダイオードの平面図であり、図１１は図１０における切断面線Ｆ－Ｆ‘の断面図である。
【０００３】２１は単結晶基板であり、この単結晶基板２１の上に矩形状の半導体緩衝層２２を島状に形成し、この半導体緩衝層２２の上に矩形状の一導電型半導体層２３と矩形状の逆導電型半導体層２４とを順次積層し、さらに逆導電型半導体層２４の表面のほぼ中央部に一方の電極を、単結晶基板２１の裏面に他方の対向電極を形成する。
【０００４】この発光ダイオードがＬＥＤアレーヘッドなどに使用する場合には、一方の電極が個別電極２６となり、他方の対向電極が共通電極２７となる。
【０００５】さらに単結晶基板２１上、各層の端面周囲、および逆導電型半導体層２４における個別電極２６の非成膜面上に絶縁膜２５を設ける。
【０００６】上記構成の発光ダイオードによれば、個別電極２６と共通電極２７との間に電圧を印加し電流を流すことで発光し、その照射光が逆導電型半導体層２４を通して個別電極２６の非成膜面より指向性をもって出射する。
【０００７】
【発明が解決しようとする課題】上記のような従来の発光ダイオードによれば、矩形状の逆導電型半導体層２４の端面の単結晶基板２１の面に対する傾斜角度は、その端面によって異なるが、その理由は、結晶方位に依存するためである。
【０００８】図１０に示すように逆導電型半導体層２４の端面の傾斜角度が、対向する傾斜Ａ’－傾斜Ｂ’および傾斜Ｃ’－傾斜Ｄ’に二分した場合には、傾斜Ａ’―傾斜Ｂ’は単結晶基板２１に対して９０° を超える勾配がある。
【０００９】すなわち、傾斜Ｃ’－傾斜Ｄ’に対しては、個別電極２６の断線を防ぐ必要があることから、その勾配を緩やかにしているが、その半面、傾斜Ａ’－傾斜Ｂ’においては、単結晶基板２１に対し９０° を超えるような勾配になる。
【００１０】しかしながら、傾斜Ａ’－傾斜Ｂ’において、単結晶基板２１に対し９０° を超えるような勾配にしたことで、逆導電型半導体層２４で発光した光は、傾斜Ａ’、Ｂ’にて反射され、これにより、発光部内の発光が不均一となり、その結果、発光ダイオードの指向性を著しく低下していた。
【００１１】さらに発光ダイオードを複数個アレー状に配列してなるＬＥＤアレーヘッドににおいては、それをプリンターに用いるにしても、各発光ダイオードの間にて発光が不均一となり、そのために露光ビーム形が不均一となり、この結果、印画品質の低下を招いていた。
【００１２】その上、傾斜Ａ’－傾斜Ｂ’のように、単結晶基板２１に対し９０° を超えるような勾配に形成する場合には、その形状をコントロールするためには、エッチングをおこなう必要がある。
【００１３】しかしながら、単結晶基板２１と、その上の成膜との双方に対し、ガリウム砒素などを基本とした化合物半導体でもって構成した場合には、エッチングの選択性がなく、これによってエッチング液の自由度が小さくなるという課題がある。
【００１４】本発明は叙上に鑑みて完成されたものであり、その目的は発光体内の発光の指向性を高めた高性能な発光ダイオードを提供することにある。
【００１５】本発明の他の目的は所要とおりに形状にエッチングするために使用するエッチング液の選択自由度を高め、これによって、製造コストを下げるとともに、発光の指向性を高めた発光ダイオードを提供することにある。
【００１６】本発明のさらに他の目的は発光の不均一性を改善し、露光ビーム形の均一化を図って印画品質の向上させた高品質なＬＥＤアレーヘッドを提供することにある。
【００１７】
【課題を解決するための手段】本発明の発光ダイオードは、単結晶基板上に半導体緩衝層を島状に形成し、この半導体緩衝層上に一導電型半導体層と逆導電型半導体層と電極とを順次積層し、そして、この逆導電型半導体層の端面周囲に、単結晶基板に対し９０° 以下の傾斜角となるように勾配を設けたことを特徴とする。
【００１８】本発明の他の発光ダイオードは、上記のような本発明の発光ダイオードに使用する単結晶基板がシ

リコンからなることを特徴とする。

【００１９】本発明のＬＥＤアレーヘッドは、かかる本発明の発光ダイオードを複数個アレイ状に配列してなることを特徴とする。

【００２０】

【発明の実施の形態】以下、本発明を図面に基づき詳細に説明する。図１は本発明の発光ダイオードの一実施形態を示す平面図であり、図２は図１における切断面線Ｅ－Ｅ'による断面図である。

【００２１】１は単結晶基板であり、単結晶基板１の上に矩形状の半導体緩衝層２を島状に形成し、この半導体緩衝層２の上に矩形状の一導電型半導体層３と矩形状の逆導電型半導体層４とを順次積層する。さらに逆導電型半導体層４の表面のほぼ中央部に一方の電極を、単結晶基板１の裏面に他方の対向電極を形成する。

【００２２】この発光ダイオードがＬＥＤアレーヘッドなどに使用する場合には、一方の電極が個別電極６となり、他方の対向電極が共通電極７となる。

【００２３】さらに単結晶基板１上、各層の端面周囲、および逆導電型半導体層４における個別電極６の非成膜面上に絶縁膜５を設ける。

【００２４】単結晶基板１については、ＧａＡｓ基板やＳｉ基板が使用されるが、好適には（１００）面を＜０１１＞方向に２～７°オフさせたＳｉ基板がよい。

【００２５】半導体緩衝層２はシリコンなどの一導電型半導体不純物を1×10^{16}～10^{18}原子／cm^3含有するガリウム砒素（ＧａＡｓ）などにて構成し、２～４μｍ程度の厚みにて形成するとよい。

【００２６】そして、半導体緩衝層２は、単結晶基板１と半導体層との格子定数の不整合に基づくミスフィット転位を防止するために設ける。

【００２７】一導電型半導体層３はシリコン（Ｓｉ）などの一導電型半導体不純物を1×10^{16}～10^{19}原子／cm^3含有するアルミニウムガリウム砒素（ＡｌＧａＡｓ）などで構成し、０．２～１．０μｍ程度の厚みに形成するとよい。

【００２８】逆導電型半導体層４は亜鉛（Ｚｎ）などの逆導電型半導体不純物を1×10^{19}～10^{21}原子／cm^3程度含有するアルミニウムガリウム砒素（ＡｌＧａＡｓ）などで構成し、０．１～１．０μｍ程度の厚みに形成するとよい。

【００２９】かかる各層については、発光効率を高めるために、シングルヘテロ構造もしくはダブルヘテロ構造にするとよく、そのためにアルミニウムガリウム砒素の化合物の混晶比を違えた層にして形成してもよい。

【００３０】絶縁膜５は窒化シリコンなどから成り、たとえば厚み３０００Å程度に形成される。

【００３１】個別電極６は金／クロム（Ａｕ／Ｃｒ）の積層などにて構成し、共通電極７は金／アンチモン（Ａｕ／Ｓｂ）の積層などにて構成し、双方とも厚み１μｍ程度にて形成するとよい。

【００３２】本発明の発光ダイオードでは、図１に示すように、個別電極６と共通電極７との間に電圧を印加し、双方間に電流を流すことによって発光させることができる。

【００３３】また、図３は本発明のＬＥＤアレーヘッドであり、長尺状の単結晶基板１の上に半導体緩衝層２を複数個配列し、個々の半導体緩衝層２上に一導電型半導体層３と逆導電型半導体層４と個別電極６とを順次積層し、さらに単結晶基板１の裏面に共通電極７を形成した構造である。

【００３４】このように本発明の発光ダイオードをアレイ状にＮ個配列形成することで、ページプリンタ用感光ドラムの露光用光源となる。

【００３５】そして、本発明の発光ダイオードにおいては、図１および図２に示すように、逆導電型半導体層４の端面周囲に、単結晶基板１に対し９０°以下の傾斜角となるように勾配を設けることが特徴である。

【００３６】すなわち、矩形状の逆導電型半導体層４においては、端面周囲を単結晶基板１に対して勾配を設けるが、その際、対向した傾斜Ａと傾斜Ｂ、ならびに対向した傾斜Ｃと傾斜Ｄとは、いずれも単結晶基板１に対し９０°以下の傾斜角となるように勾配を設ける。

【００３７】半導体緩衝層２と一導電型半導体層３に関しては、双方とも図２に示すように単結晶基板１に対し９０°以下の傾斜角となるように勾配を設けてもよい。これによって、逆導電型半導体層４の下層である部分がなだらかな順メサ形状とすることができるために、素子の欠けが発生し難い構造を形成し易いという点で好適である。

【００３８】しかし、この形状に限定されるものではなく、少なくとも一端面において、単結晶基板１に対し９０°を超える傾斜角となるように勾配を設けてもよい上記構成の発光ダイオードによれば、図４に示すような光路になる。同図に示すように、逆導電型半導体層４の端面周囲を単結晶基板１に対して９０°以下の傾斜角となるように勾配を設けたことで、光の出射面が小さくなり、さらにその端面に至る光は逆導電型半導体層４の内部にて反射されながら、最後には、その小さい出射面が発光され、これにより、発光が絞られ、その結果、発光の指向性が顕著に向上する。

【００３９】図５は、本発明の発光ダイオードの発光強度分布を示す。横軸は切断面線Ｅ－Ｅ'に対応し、縦軸は光強度を示す。

【００４０】また、図６は本発明の発光ダイオードをアレー状に並べて、個々の発光ダイオードのビーム形状を測定したものである。なお、白部分は発光強度が大きく、黒部分は発光強度が小さくなっていることを示す。

【００４１】これに対し、従来の発光ダイオードは図７に示すような光路になる。

【００４２】同図に示すように、傾斜Ａ’、Ｂ’によって、逆導電型半導体層４の端面周囲を単結晶基板１に対して９０°を超える傾斜角となるように勾配を設けたことで、光の出射面が大きくなり、さらにその端面に至る光は外に反射され、これにより、発光が放散され、その結果、発光の指向性が劣る。

【００４３】図８は、従来の発光ダイオードの発光強度分布を示す。横軸は切断面線Ｆ－Ｆ’に対応し、縦軸は光強度を示す。また、図９は従来の発光ダイオードをアレー状に並べて、個々の発光ダイオードのビーム形状を測定したものである。

【００４４】以上の各図から明らかなとおり、本発明の発光ダイオードによれば、発光が絞られ、図５や図６に示されるように、発光の指向性が向上しているが、これに対する従来の発光ダイオードにおいては、図８と図９に示されるように発光の指向性が劣っていることがわかる。

【００４５】つぎに本発明の発光ダイオードおよびＬＥＤアレーヘッドの作製方法を述べる。

【００４６】大きな単結晶基板１の上に半導体緩衝層２と一導電型半導体層３と逆導電型半導体層４とを順次積層し、そして、周知のエッチング方法によって半導体緩衝層２と一導電型半導体層３と逆導電型半導体層４から成る島状半導体層を形成し、この逆導電型半導体層４の上に個別電極６を接続形成し、さらに単結晶基板１の裏面に共通電極７を接続形成する。

【００４７】上記のエッチングは硫酸過酸化水素系のエッチング液を用いたウェットエッチングやCCl_2F_2ガスを用いたドライエッチングなどがある。

【００４８】また、上記の半導体緩衝層２と一導電型半導体層３と逆導電型半導体層４から成る島状半導体層は、ＭＯＣＶＤ法などで順次積層して形成する。

【００４９】これら半導体緩衝層２と一導電型半導体層３と逆導電型半導体層４を形成するには、基板温度を４００～５００℃に設定し、アモルファス状のガリウム砒素膜を２００～２０００Åの厚みにて形成し、その後、基板温度を６００～９００℃にまで上げることで得られる。

【００５０】このＭＯＣＶＤ法を使用するには、原料ガスとしてはＴＭＧ（$(CH_3)_3Ga$）、ＴＥＧ（$(C_2H_5)_3Ga$）、アルシン（AsH_3）、ＴＭＡ（$(CH_3)_3Al$）、ＴＥＡ（$(C_2H_5)_3Al$）などが用いられる。

【００５１】導電型を制御するためのガスとしては、シラン（SiH_4）、セレン化水素（H_2Se）、ＴＭＺ（$(CH_3)_3Zn$）などが用いられ、キャリアガスとしては、H_2などがある。

【００５２】本発明では、少なくとも逆導電型半導体層４を単結晶基板１に対して勾配を９０°以下に形成することから、硫酸、過酸化水素の比率を変化させることで、所望の形状を制御する。あるいはドライエッチングでもって異方性エッチングしてもよい。

【００５３】このようなエッチングにおいては、単結晶基板１に対しＳｉ基板を用いるとよく、これにより、硫酸過酸化水素のウエットエッチングまたはドライエッチングでも、ガリウム砒素や、アルミニウムガリウム砒素との選択エッチング性が高くなり、その結果、半導体基板を不用にエッチングされることが防止され、高い精度でもって所要とおりの形状にできる。

【００５４】つぎにプラズマＣＶＤ法で、シランガス（SiH_4）とアンモニアガス（NH_3）を用いて窒化シリコンから成る絶縁膜５を被覆し、パターニングする。

【００５５】その後に、個別電極６と共通電極７は、Ａｕ、ＡｕＧｅなどを蒸着法やスパッタリング法で形成してパターニングする。

【００５６】しかる後に、各ＬＥＤ素子ごとにダイシング等の方法にて切断し、分離する。そして、各ＬＥＤ素子に対しダイボンディング、ワイヤーボンディング、エポエシ樹脂のコートをおこなう。

【００５７】なお、本発明は上記の実施形態例に限定されるものではなく、本発明の要旨を逸脱しない範囲内で種々の変更や改良等はなんら差し支えない。たとえば、半導体緩衝層２、一導電型半導体層３および逆導電型半導体層４を矩形状に形成したが、これに代えて、これら各層を六角形、八角形などの多角形にしてもよい。

【００５８】

【発明の効果】以上のとおり、本発明の発光ダイオードによれば、単結晶基板上に半導体緩衝層を島状に形成し、この半導体緩衝層上に一導電型半導体層と逆導電型半導体層と電極とを順次積層し、そして、この逆導電型半導体層の端面周囲に、単結晶基板に対し９０°以下の傾斜角となるように勾配を設けたことで、発光体内の発光の指向性を高め、これによって高性能な発光ダイオードが提供できた。

【００５９】また、本発明の発光ダイオードにおいては、上記の単結晶基板をシリコンにて構成したことで、所要とおりに形状にエッチングでき、これにより、エッチング液の選択自由度を高め、その結果、製造コストを下げるとともに、発光の指向性を高めた発光ダイオードが提供できた。

【００６０】さらに本発明によれば、かかる本発明の発光ダイオードを用いたことで、発光の不均一性を改善し、露光ビーム形の均一化を図って印画品質の向上させた高品質なＬＥＤアレーヘッドが提供できた。

【図面の簡単な説明】

【図１】本発明の発光ダイオードの平面図である。

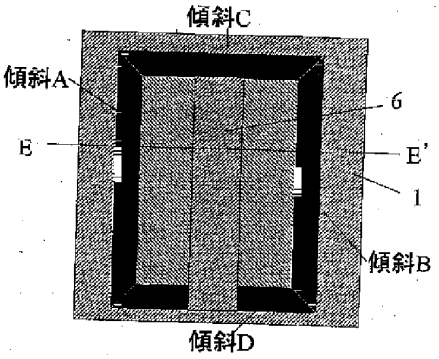
【図２】本発明の発光ダイオードの断面図である。

【図３】本発明のＬＥＤアレーヘッドの断面図である。

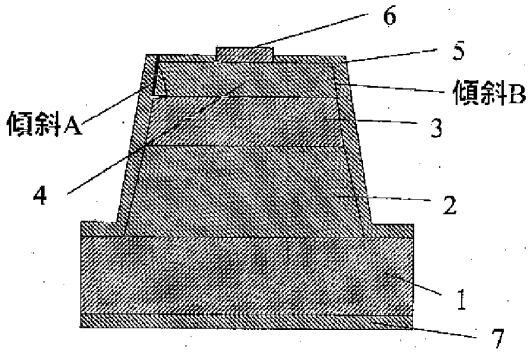
【図４】本発明の発光ダイオードにおける光路を示す断

面図である。
【図５】本発明の発光ダイオードの発光強度を示す図である。
【図６】本発明のＬＥＤアレーヘッドの発光ビーム形状を示す図である。
【図７】従来の発光ダイオードにおける光路を示す断面図である。
【図８】従来の発光ダイオードの発光強度を示す図である。
【図９】従来のＬＥＤアレーヘッドの発光ビーム形状を示す図である。
【図１０】従来の発光ダイオードの平面図である。
【図１１】従来の発光ダイオードの断面図である。
【符号の説明】
１・・・単結晶基板
２・・・半導体緩衝層
３・・・一導電型半導体層
４・・・逆導電型半導体層
５・・・絶縁膜
６・・・個別電極
７・・・共通電極

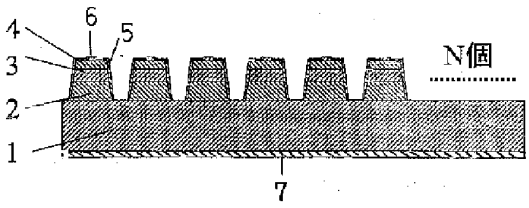
【図１】



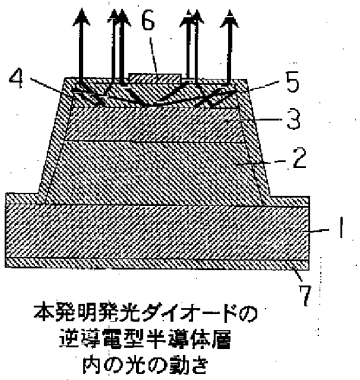
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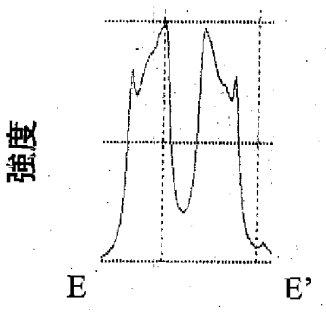
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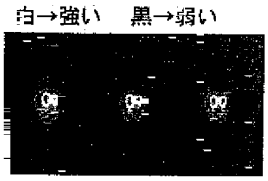
【図４】



【図５】

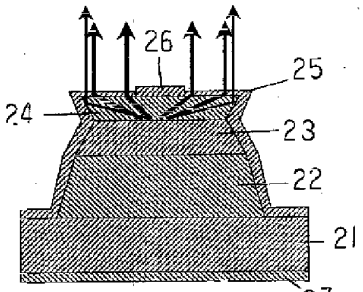


【図6】



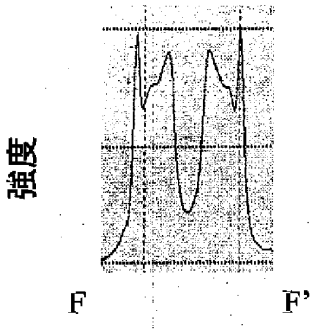
発光ダイオードをアレイ状にした時の指向性を示すビーム形状

【図7】

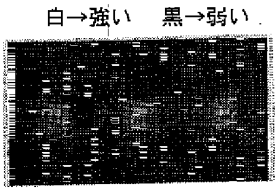


従来発光ダイオードの逆導電型半導体層内の光の動き

【図8】

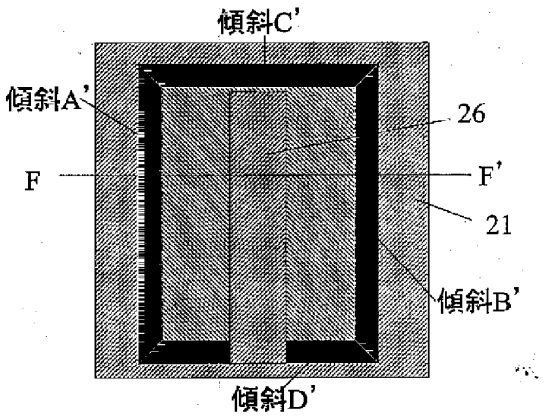


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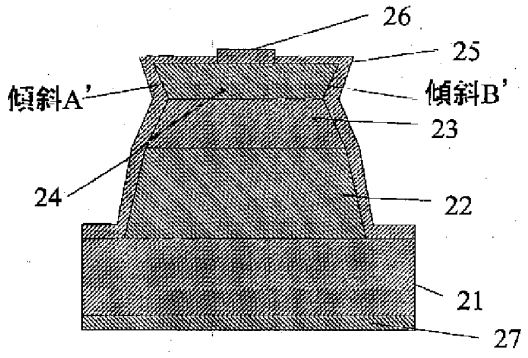


発光ダイオードをアレイ状にした時の指向性を示すビーム形状

【図10】



【図11】



フロントページの続き

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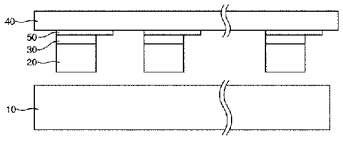
(51)Int. Cl H01L 33/00

(71)Applicant: SEOUL SEMICONDUCTOR CO., LTD.
(72)Inventor: LEE, CHUNG HOON
KIM, HONG SAN

(54) LIGHT EMITTING DEVICE TO WHICH PLURAL CELLS ARE COUPLED, FABRICATING METHOD THEREOF AND LIGHT EMITTING APPARATUS USING THE SAME TO SIMPLIFY PROCESS FOR FABRICATING LAMP

(57) Abstract:

PURPOSE: A light emitting device to which plural cells are coupled is provided to simplify a process for fabricating a lamp by electrically connecting a plurality of light emitting cells in a wafer level. CONSTITUTION: A plurality of vertical light emitting cells that the interconnection in series or parallel are formed on a host substrate(40). The host substrate is made of one of a conductor substrate, a non-conductor substrate or a semiconductor substrate. An electrode pattern layer(50) is formed between the non-conductor substrate and the plurality of light emitting cells.



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심사청구 : 없음

(54) 다수의 셀이 결합된 발광 소자 및 이의 제조 방법 및 이를이용한 발광 장치

요약

본 발명은 다수의 셀이 어레이된 발광 소자 및 이의 제조 방법 및 이를 이용한 조명용 발광장치에 관한 것으로, 전극과 발광 반도체층을 포함하는 수직형의 다수의 발광 셀 및 상기 발광 셀이 직렬 접속된 호스트 기판을 포함하는 발광 소자 및 이의 제조 방법을 제공한다. 이로써, 고전압 또는 가정용 교류 전원을 사용하는 조명용 발광 장치의 제작 공정을 단순화시킬 수 있고, 조명용 발광 장치의 제작시 발생하는 불량률을 줄일 수 있으며, 조명용 발광 장치를 대량 생산할 수 있다. 또한, 발광 소자 외부에 소정의 정류 회로를 둠으로 인해 교류 동작시 직류 구동 효율을 향상시킬 수 있는 이점이 있다.

대표도

도 3

색인어

발광 셀, 발광 소자, 직렬 접속, 금속배선, 정류 브리지, 조명용 발광 장치

명세서

도면의 간단한 설명

도 1은 종래의 발광 장치를 설명하기 위한 개념도이다.

도 2 및 도 3은 본 발명의 일 실시예에 따른 발광 소자의 제조 방법을 설명하기 위한 단면도이다.

도 4는 본 발명에 따른 다른 일 실시예에 따른 발광 소자의 제조 방법을 설명하기 위한 단면도이다.

도 5 내지 도 11은 각기 본 발명의 제 1 내지 제 7 실시예에 따른 발광 소자를 설명하기 위한 개념도들이다.

도 12는 본 발명에 따른 발광 장치를 설명하기 위한 개념도이다.

<도면의 주요 부분에 대한 부호의 설명>

1, 200 : 발광 소자 10 : 모체 기판

20 : 발광 반도체층 30, 50, 60 : 전극

40 : 호스트 기판 70 : 배선

100 : 발광 셀 150 : 정류 브리지부

210 내지 260 : 외부 단자 전극

310 내지 340 : 다이오드 블록

410, 420 : 전원패드 510 : 전원부

520 : 제어부

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 다수의 셀이 결합된 발광 소자 및 이의 제조 방법 및 이를 이용한 발광 장치에 관한 것으로, 특히, 단일 기판상에 다수의 발광용 셀이 배열된 단일의 발광 소자와 이의 제조 방법에 관한 것이고, 또한, 이를 이용하여 제조된 발광장치에 관한 것이다.

발광 다이오드는 반도체의 p-n 접합구조를 이용하여 주입된 소수캐리어(전자 또는 양공)를 만들어내고, 이들의 재결합에 의하여 소정의 빛을 발산하는 소자를 지칭한다. 이러한 발광 다이오드는 표시 소자 및 백라이트로 이용되고 있으며, 최근 일반 조명용도로 이를 적용하기 위해 활발한 연구가 진행중이다.

이는 발광 다이오드가 기존의 전구 또는 형광등에 비해 소모 전력이 작고 수명이 길기 때문이다. 즉, 발광 다이오드의 소모 전력이 기존의 조명 장치에 비해 수 내지 수 십분의 1에 불과하고, 수명이 수 내지 수십배에 이르러, 소모 전력의 절감과 내구성 측면에서 월등하기 때문이다.

일반적으로, 발광 다이오드를 조명용으로 사용하기 위해서는 별도의 패키징 공정을 통해 발광 소자를 형성하고, 다수의 개별 발광소자를 와이어 본딩을 통해 직렬 연결하고, 외부에서 보호 회로 및 교류/직류 변환기 등을 설치하여 램프의 형태로 제작하였다.

도 1은 종래의 발광 장치를 설명하기 위한 개념도이다.

도 1을 참조하면, 발광 칩이 실장된 다수의 발광 소자(1)를 직렬 접속시켜 일반 조명 용도의 발광 장치를 제작하였다. 이를 위해 다수의 발광 소자(1)를 직렬로 배열한 다음, 금속배선 공정을 통해 각기 다른 발광 소자(1)내부의 발광 칩을 전기적으로 직렬 연결하였다. 이러한, 제조 공정에 관해서는 미국 공개 특허 제 5,463,280호에 개시되어 있다. 하지만, 상술한 구조를 통한 종래의 기술로 조명 용도의 발광 장치를 제작하였을 경우, 많은 갯수의 소자에 일일이 금속 배선 공정을 수행하여야 하기 때문에 공정단계가 많아지고 복잡해지는 문제가 발생한다. 또한, 공정의 단계가 증가할수록 이에 따른 불량 발생

률 또한, 높아지게 되어 대량 생산에 걸림돌이 되고 있다. 또한, 소정의 충격에 의해 금속배선이 단락 되어 발광 소자의 동작이 종료되는 경우가 발생할 수 있다. 또한, 개개의 발광 소자를 직렬로 배열하여야 함으로 인해 차지하게 되는 공간이 커지게 되어 램프의 크기가 상당히 커지는 단점이 발생하였다.

또한, 앞서 설명한 소자 레벨의 발광 칩 어레이가 아닌 웨이퍼 레벨에서의 마이크로칩을 어레이함에 관해서는 한국 공개특허공보 제2004-9818호에 개시되어 있다. 이는, 표시 장치에 관한 것으로 각각의 화소에 발광을 유도하는 발광 다이오드가 배치 되도록 발광 셀을 매트릭스 형태로 배열한다. 하지만, 상술한 매트릭스 형태로 배열된 구조의 소자를 발광시키기 위해서는 세로 방향과 가로 방향으로 각기 서로 다른 전기적 신호를 인가하여야할 뿐만 아니라, 전기적 신호를 어드레스 방식으로 인가하여야 하기 때문에 이를 제어하기가 극히 어렵다. 또한, 매트릭스 형태의 배열로 인해 배선간의 단선이 우려되고, 배선간의 중첩영역에 많은 간섭이 발생하게 된다. 또한, 상술한 매트릭스 형태의 구조로는 고전압이 인가 되는 조명용 발광장치에 적용할 수 없는 문제점이 있었다.

발명이 이루고자 하는 기술적 과제

따라서, 본 발명은 상기의 문제점을 해결하기 위하여 다수의 발광 셀이 직렬 접속된 단일칩 형태로 발광 소자를 사용하여 발광 다이오드 램프를 제작할 수 있고, 웨이퍼 레벨에서 다수의 발광 셀을 전기적으로 연결하기 때문에 램프의 제작 공정을 단순화 할 수 있으며, 불량률을 감소시킬 수 있어 대량 생산에 유리한 다수의 셀이 어레이된 발광 소자 및 이의 제조 방법 및 이를 이용한 발광 장치를 제공함을 그 목적으로 한다.

발명의 구성 및 작용

본 발명에 따른 호스트기판 및 상기 호스트기판상에 직렬 또는 직병렬 연결된 다수의 수직형 발광셀을 포함하여 구성된 발광소자를 제공한다.

여기서, 상기 호스트기판은, 도체, 부도체, 및 반도체 기판중 어느 일측으로 구성되는 것을 특징으로 한다. 이때, 상기 부도체 호스트기판과 상기 다수의 발광셀 사이에는 전극패턴층이 형성되어 있는 것을 특징으로 하고, 상기 도체 또는 반도체 호스트기판과 상기 발광셀 사이에는, 상기 호스트기판측에 절연층이, 상기 다수의 발광셀측에 전극패턴층이 개재되어 있는 것을 특징으로 한다.

그리고 상기 다수의 수직형 발광셀은 각각 GaN계 반도체를 포함한다.

또한, 본 발명에 따른 모체기판에 화합물반도체를 성장시키는 단계와, 상기 화합물반도체를 다수의 수직형 발광셀로 형성한 후, 상기 각각의 수직형 발광셀의 상부에 제 1전극을 형성하는 단계와, 상기 수직형 발광셀의 상부에 호스트기판을 부착하는 단계와, 상기 모체기판을 제거한 후 상기 각 수직형 발광셀의 하부에 제 2전극을 형성하는 단계 및 상기 각 수직형 발광셀의 제 1전극들과 인접하는 수직형 발광셀의 제 2전극들을 직렬 또는 직병렬로 연결하는 단계를 포함하는 발광소자 제조방법을 제공한다.

여기서, 상기 호스트기판이 도체 또는 반도체기판인 경우, 상기 호스트기판과 상기 수직형 발광셀의 제 1전극 사이에 절연층을 형성하는 단계를 더 포함하는 것을 특징으로 한다.

또한, 본 발명에 따른 모체기판에 화합물반도체를 성장시키는 단계와, 상기 화합물반도체를 다수의 수직형 발광셀로 형성하는 단계와, 상기 다수의 수직형 발광셀의 상부에 호스트기판을 부착하는 단계 및 상기 각 수직형 발광셀을 인접하는 수직형 발광셀들과 직렬 또는 직병렬로 연결하는 단계를 포함하는 발광소자 제조방법을 제공한다.

이때, 상기 모체기판은 레이져를 이용한 리프트오프공정, 식각공정, 또는 CMP공정으로 제거되는 것을 특징으로 한다.

이하, 첨부된 도면을 참조하여 본 발명의 실시예를 더욱 상세히 설명하기로 한다. 그러나 본 발명은 이하에서 개시되는 실시예에 한정되는 것이 아니라 서로 다른 다양한 형태로 구현될 것이며, 단지 본 실시예들은 본 발명의 개시가 완전하도록 하며, 통상의 지식을 가진 자에게 발명의 범주를 완전하게 알려주기 위해 제공되는 것이다. 도면상에서 동일 부호는 동일한 요소를 지칭한다.

본 발명은 기판상에 각기 분리된 다수의 수직형 발광 셀이 형성된다. 이후, 다수의 수직형 발광 셀의 상부에 호스트 기판을 본딩한 다음, 하부의 모체 기판을 제거한다. 이후 다수의 수직형 발광 셀의 인접한 셀간의 서로 다른 전극간을 전기적으로 연결한다. 즉, 발광 셀간을 직렬 연결하여 발광 소자를 형성한다. 이러한 수직형 발광 셀의 구조를 간략히 살펴보면, 발광

반도체층과, 발광 반도체층 상하에 위치한 제 1 및 제 2 전극과, 제 1 전극과 접속된 전극 패턴을 포함하는 호스트 기판을 포함하고 있다. 물론 호스트 기판의 특성에 따라 전극 패턴과 호스트 기판 사이에 별도의 절연층을 더 포함할 수도 있다. 이러한 구조의 발광 셀들이 직렬 접속된 발광 소자를 제조하기 위해서는 다양한 제조 방법들이 제공될 수 있다.

이에 관한 구체적인 설명은 하기의 도면을 참조하여 설명한다.

도 2 및 도 4는 본 발명의 일 실시예에 따른 발광 소자의 제조 방법을 설명하기 위한 단면도이다.

도 2를 참조하면, 모체기판(10)상에 반도체층(20)과 제 1 전극(30)을 포함하는 복수개의 분리된 발광 셀(100)을 형성하고, 소정의 전극 패턴(50)이 형성된 호스트 기판(40)을 마련한다.

모체 기판(10)으로는 반도체 소자의 제조가 가능한 모든 기판이 사용될 수 있고, 본 실시예에서는 사파이어 기판 또는 실리콘 기판을 사용한다.

상기의 발광 반도체층(20)은 다수의 물질층으로 이루어진 구조를 갖는다. 즉, 본 실시예에서는 버퍼층(미도시), N형 반도체층(미도시), 활성층(미도시) 및 P형 반도체층(미도시)이 순차적으로 적층된 형태의 구조를 갖는다. 또한, 제 1 전극(30)은 소정의 도전성 패드를 지칭하는 것이며, 각각의 발광 반도체층(20)은 소정간격 이격되어 있다.

이를 위해, 모체 기판(10)상에 버퍼층, N형 반도체층, 활성층 및 P형 반도체층을 순차적으로 형성한다. 이때 버퍼층은 결정 성장시에 모체기판(10)과 후속층들의 격자 부정합을 줄위기 위한 층으로서, 반도체 재료인 GaN을 포함하여 이루어진다. 물론 이때, 버퍼층을 형성하지 않을 수도 있다. 또한, 상기의 N형 반도체층은 전자가 생성되는 층으로서, N형 화합물 반도체층과 N형 클래드층으로 형성된다. 이때, N형 화합물 반도체 층은 N형 불순물이 도핑되어 있는 GaN을 사용한다. 그리고, P형 반도체층은 전공이 생성되는 층으로서, P형 클래드층과 P형 화합물 반도체층으로 형성된다. 이때, P형 화합물 반도체층은 P형 불순물이 도핑되어 있는 AlGaN을 사용한다. 마지막으로 활성층은 소정의 밴드 갭과 양자 우물이 만들어져 전자 및 정공이 재결합되는 영역으로서, InGaN을 포함하여 이루어진다. 이때 활성층을 이루는 물질의 종류에 따라 전자 및 전공이 결합하여 발생하는 발광 파장이 변화된다. 따라서, 목표로 하는 파장에 따라 활성층에 포함되는 반도체 재료를 조절하는 것이 바람직하다.

이후 P형 반도체층 상에 소정의 전극막을 형성한 후, 소정의 마스크를 이용한 식각공정을 통해 전극막, P형 반도체층, 활성층, N형 반도체층 및 버퍼층을 식각하여 각기 분리된 제 1 전극(30) 및 발광 반도체층(20)을 형성한다.

한편, 표면에 소정의 전극 패턴(50)이 형성된 호스트 기판(40)은 호스트 기판(40)의 하부 면상에 도전성 물질막을 형성한 다음, 이를 소정의 마스크를 이용하여 제거함으로써 제작된다. 물론 이뿐만 아니라 호스트 기판(40)상에 소정의 시드 패턴을 형성한 다음, 금속도금 방법을 통해 형성할 수도 있다. 또한, 인쇄회로 방법을 이용하여 형성할 수도 있다.

도 3 및 도 4를 참조하면, 상기와 같이 전극 패턴(50)이 형성된 호스트 기판(40)의 전극 패턴(50)에 상기 제 1 전극(30)을 본딩한다. 이를 위해 호스트 기판(40)의 표면에 형성되는 전극패턴(50)은 하부의 제 1 전극(30)보다 더 크게 형성되고, 각각은 서로 인접한 전극패턴(50) 및 제 1 전극(30)과 물리적 및 전기적으로 분리되어 있게 된다. 또한, 호스트 기판(40) 표면의 전극 패턴(50)과 제 1 전극(30)간을 본딩하기 위해 별도의 도전성 페이스트를 이용하여 접착한다. 물론, 이외의 다양한 본딩방법을 이용하여 이둘간을 접착할 수 있다. 또한, 도 3에서보는 바와 같이 제 1 전극(30) 상부의 일측방향으로 전극패턴(50)의 일부가 돌출되도록 하여 후속 전극간의 연결을 좀더 양호하게 할 수 있다.

다음으로, 하부의 모체기판(10)을 제거하고 모체 기판(10)이 제거된 영역의 발광 반도체층(20)의 하부에 제 2 전극(60)을 형성하여 호스트 기판(40) 하부에 다수의 수직형 발광 셀(100)을 형성한다. 이때, 하부의 모체기판(10)의 제거는 레이져를 이용한 리프트 오프 공정을 통해 제거된다. 물론, 반도체 제조 공정에서 사용되는 식각공정 또는 CMP 공정을 통해 제거할 수도 있다. 모체 기판(10)이 제거됨으로 인해 모체 기판(10)상부의 발광 반도체층(20)이 노출된다. 이후 소정의 전극 패드 형성공정을 통해 모체기판(10)이 제거됨으로서 노출된 발광 반도체층(20) 상에 제 2 전극(60)을 형성하여 개개의 수직형 발광 셀(100)을 제조한다.

마지막으로, 인접한 개개의 수직형 발광 셀(100)의 서로 다른 전극간을 배선(70)을 이용하여 전기적으로 연결한다. 즉, 도 3에서와 같이 모체 기판(10)의 하부에 형성된 전극 패턴(50)과 이와 인접한 발광 셀(100)의 제 2 전극(60)간을 연결함으로써, 다수의 수직형 발광 셀(100)이 직렬 접속된 발광 소자를 형성한다. 이때, 양측 가장자리의 발광 셀(100) 각각의 전극 패턴(50)과 제 2 전극(60)은 별도의 외부 단자를 더 포함할 수 있다.

또한, 상술한 전극은 도전성의 물질막을 사용하되, 모든 전기 전도성을 갖는 물질을 사용할 수 있다.

상술한 본 발명의 일 실시예에서는 호스트 기판으로 전기 전도성이 없는 부도체물질일 경우에 관해 설명하였다. 하지만 이에 한정되지 않고 호스트 기판으로 전기 전도성을 갖는 도체 물질 또는 반도체 물질을 사용할 수도 있다. 또한, 제 1 전극을 형성하지 않고, 호스트 기판의 전극 패턴을 제 1 전극으로 사용할 수도 있고, 호스트 기판에 전극 패턴을 형성하지 않고, 제 1 전극이 형성된 발광 셀을 직접 호스트 기판에 실장할 수 있다. 이에 관해 하기에서 설명한다.

도 5a 내지 도 5c는 본 발명에 따른 다른 일 실시예들에 따른 발광 소자의 제조 방법을 설명하기 위한 단면도이다.

도 5a를 참조하면, 호스트 기판(40)으로 SiC, Si 또는 금속을 사용할 경우, 그 표면에 부도체의 절연물질로 이루어진 소정의 절연층(45)을 형성한 다음, 절연층(45) 상에 앞선 실시예에서 설명하였던 전극패턴(50)을 형성한다. 또한, 도 2에서 설명하였던 모체기판(도 2의 10번 참조)상에 형성된 발광 반도체층(20)과 제 1 전극(30)을 전극 패턴(50)에 본딩한다. 이후, 하부의 모체 기판을 제거한 다음 노출된 발광 반도체층(20) 하부에 제 2 전극(60)을 형성한다.

그런다음, 와이어 본딩 또는 금속배선공정을 통해 이웃하는 발광 셀간의 서로 다른 전극들을 연결한다. 이때 인접한 셀의 제 1 전극(30) 및 제 2 전극(60)은 호스트 기판(40)의 전극 패턴(50)과 별도의 배선(70)을 통해 전기적으로 직렬 연결한다.

도 5b를 참조하면, 소정의 전극 패턴(50)이 형성된 호스트 기판(40)을 마련하고, 도 2에서 설명한 모체기판(도 2의 10번 참조) 상에 발광 반도체층(20)만을 형성한다. 본 실시예에서는 제 1 전극(도 2의 30번 참조)을 형성하지 않는다. 다음으로, 호스트 기판(40)의 전극 패턴(50)에 발광 반도체층(20)을 본딩한다. 이때, 도전성 페이스트를 이용하여 본딩한다. 이후, 하부의 모체 기판을 제거한 다음 노출된 발광 반도체층(20) 하부에 제 2 전극(60)을 형성한다.

그 후에 와이어 본딩 또는 금속배선공정을 통해 이웃하는 발광 셀(100)의 전극 패턴(50)과 제 2 전극(60)을 별도의 배선(70)을 이용하여 전기적으로 직렬 연결한다.

도 5c를 참조하면, 호스트 기판(40)을 마련하고, 도 2에서 설명한 반도체층(20)과 제 1 전극(30)을 포함하는 복수개의 분리된 셀을 마련한다. 다음으로, 호스트 기판(40)에 제 1 전극(30)을 본딩한다. 이후, 하부의 모체 기판을 제거한 다음, 노출된 발광 반도체층(20)의 일부를 제거하여 제 1 전극(30)의 일부를 노출시킨다. 그후, 제 1 전극(30)의 반대편 발광 반도체층(20)에 제 2 전극(60)을 형성한다.

다음으로, 와이어 본딩 또는 금속배선공정을 통해 이웃하는 발광 셀(100)간의 서로 다른 전극들을 연결한다. 이때 인접한 셀의 제 1 전극(30)과 제 2 전극은 별도의 배선(70)을 통해 전기적으로 직렬 연결한다.

상술한 본 발명의 실시예는 각각의 실시예에 한정되지 않고 다양한 형태의 변형이 가능하다. 즉, 발광 반도체층(20)의 형성에 있어서도 다수의 반도체막들이 더 추가 될 수도 있고, 인접한 발광 셀(100)간을 연결하기 위해서 별도의 절연막을 형성하여 인접한 셀간을 전기적으로 고립시킨 다음, 각각의 전극을 노출하여 이들간을 소정의 배선(70)으로 연결할 수도 있다. 이뿐만 아니라 브리지(Bridge) 공정 또는 스탭 커버리지(Step Coverage) 등의 공정을 통해 각기 인접한 발광 셀(100)의 제 1 전극/전극패턴(30/50)과 제 2 전극(60)간을 전기적으로 연결하는 도전성 배선(70)을 형성한다.

상술한 브리지 공정은 에어브리지 공정이라고도 하며, 서로 연결할 칩 간에 포토 공정을 이용해 감광액을 도포하고 현상하여 감광막 패턴을 형성하고, 그 위에 금속 등의 물질을 진공 증착등의 방법으로 먼저 박막으로 형성하고, 다시 그 위에 도금 또는 금속증착등의 방법으로 금을 포함하는 도전성 물질을 일정 두께로 도포한다. 이후, 솔벤트등의 용액으로 감광막 패턴을 제거하면 도전성 물질의 하부는 다 제거되고 브리지 형태의 도전성 물질 만이 공간에 형성된다.

또한, 스텝커버리지 공정은 서로 연결할 칩 간에 포토공정을 이용해 감광액을 도포하고, 현상하여 서로 연결될 부분만을 남기고 다른 부분은 감광막 패턴으로 뒤덮고, 그 위에 도금 또는 금속증착 등의 방법으로 금을 포함하는 도전성 물질을 일정두께로 도포한다. 이어서, 솔벤트 등의 용액으로 감광막 패턴을 제거하면 도전성 물질이 덮인 이외의 부분은 다 제거되고 이 덮혀진 부분 만이 남아 연결할 칩 사이를 전기적으로 연결시키는 역할을 하게 된다. 또한, 상기의 배선으로는 금속뿐만 아니라 전도성을 갖는 모든 물질들을 사용할 수 있다.

본 발명의 발광 소자 일단부에 위치한 발광 셀(100)의 제 1 전극(30)과 접속해 있는 전극 패턴(50)과 제 2 전극(60) 각각에 별도의 패드(즉, 외부 단자 전극)를 형성하여 외부로 부터 소정의 전원을 입력받을 수 있도록 한다.

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그리고 본 발명의 발광 소자를 구성하는 수직형 발광 셀(100)의 개수는 교류 구동이 가능한 전압의 숫자 만큼 형성하는 것이 효과적이다. 즉, 본 발명에서는 단일 발광 셀(100)을 구동하기 위한 전압/전류와 조명용 발광소자에 인가되는 교류 구동전압에 따라 직렬 접속되는 발광 셀(100)의 개수가 매우 다양할 수 있다. 물론 바람직하게는 10 내지 1000개의 발광 셀을 직렬 접속한다. 더욱 바람직하게는 30 내지 70개의 셀을 직렬 접속하는 것이 효과적이다. 예를 들어, 가정용 220V 교류 구동에서는 일정 구동 전류에 3.3V 짜리 단위 발광 다이오드 셀을 66 내지 67개를 직렬로 연결하여 발광 소자를 제작한다. 또한, 110V 교류 구동에서는 일정 구동 전류에 3.3V 짜리 단위 발광 다이오드 셀을 33 내지 34개를 직렬로 연결하여 발광 소자를 제작한다.

또한, 상술한 발광 소자는 외부 교류전압을 정류하기 위한 정류용 제 1 내지 제 4 다이오드(미도시)가 형성될 수 있다. 제 1 내지 제 4 다이오드는 정류 브리지형태로 배열된다. 제 1 내지 제 4 다이오드간의 정류 노드들이 각기 발광 셀의 N형 패드와 P형 패드에 접속될 수 있다. 상기 제 1 내지 제 4 다이오드로 발광 셀을 사용할 수 있다. 이에 관해서는 후술하도록 한다.

이하 소정의 회로 개념도를 통해 본 발명의 발광 소자에 관해 설명한다.

도 6은 본 발명의 제 1 실시예에 따른 발광 소자를 설명하기 위한 개념도이다.

도 6을 참조하면, 본 실시예의 발광 소자(200)는 직렬 접속된 다수의 발광 셀(100) 블록이 외부와 전기적으로 연결된다. 도 2 내지 도 4에서 설명한 본 발명의 발광 소자(200)에 와이어 공정을 통해 N형 패드 및 P형 패드에 각기 외부 단자 전극(210 및 220)을 형성한다. 외부 단자 전극(210 및 220)은 애노드전극(210) 및 캐소드전극(220)을 지칭한다. 이로써, 다수의 발광 셀(100)이 직렬 접속된 단일의 발광소자(200)를 제조한다. 뿐만 아니라, 교류 구동시에도 동작할 수 있도록 별도의 제어부가 추가된 발광 소자를 제공할 수 있다.

도 7은 본 발명의 제 2 실시예에 따른 발광 소자를 설명하기 위한 개념도이다.

도 7을 참조하면, 본 실시예의 발광 소자(200)는 직렬 접속된 다수의 발광 셀(100)과, 발광 셀 블록과 접속되고 발광 셀(100)에 소정의 전류를 인가하기 위한 정류 브리지부(150)와 상기 정류 브리지부(150)와 접속된 외부 단자 전극들(210 및 220)을 포함한다.

본 실시예에서는 직렬 접속된 다수의 발광 셀(100)이 외부의 전원과 집적 접속되지 않고, 제 1 및 제 2 외부 단자 전극(210 및 220)에 접속된 정류 브리지부(150)를 통해 외부의 전원과 전기적으로 접속된다. 상기의 정류 브리지부(150)는 제 1 외부 단자 전극(210)과 발광 셀(100)의 에노드 단자에 접속된 제 1 다이오드(D1)와, 발광 셀(100)의 에노드단자와 제 2 외부 단자 전극(220)에 접속된 제 2 다이오드(D2)와, 제 2 외부 단자 전극(220)과 발광 셀(100)의 캐소드에 접속된 제 3 다이오드(D3)와, 발광 셀(100)의 캐소드와 제 1 외부 단자 전극(210)에 접속된 제 4 다이오드(D4)를 포함하여 이루어진다. 따라서, 정류 브리지부(150)는 교류 구동중 순방향 전압 인가시 순방향으로 정렬된 브리지 다이오드(D1 및 D3)에 의해 전류가 직렬 접속된 발광 셀(100)에 인가되고, 역방향 전압 인가시 역방향으로 정렬된 정류브리지 다이오드(D2 및 D4)에 의해 전류가 직렬 접속된 발광 셀(100)에 인가된다. 이로써, 교류전원에 상관없이 계속적으로 발광 소자(200)가 발광하게 된다.

또한, 외부의 전원이 정류 브리지와 직렬 접속된 발광 셀에 동시에 인가될 수도 있다.

도 8은 본 발명의 제 3 실시예에 따른 발광 소자를 설명하기 위한 개념도이다.

도 8을 참조하면, 본 실시예의 발광 소자(200)는 직렬 접속된 다수의 발광 셀(100)과, 직렬 접속된 발광 셀(100) 블록에 소정의 전류를 인가하기 위한 정류 브리지부(150)와, 상기 발광 셀(100)과 정류 브리지부(150)에 각기 접속된 외부 단자 전극들(210 내지 240)을 포함한다.

본 실시예에서는 직렬 접속된 다수의 발광 셀(100)이 제 2 및 제 4 외부 단자 전극(220 및 240)에 의해 외부의 전원과 직접 접속되고, 제 1 및 제 3 외부 단자 전극(210 및 230)에 접속된 정류 브리지부(15)에 의해 외부 전원과 전기적으로 접속되어 있다. 상기의 발광 셀(110)과 접속되는 전원과 정류 브리지부(150)와 접속되는 전원은 동일한 전원일 수도 있고, 각기 다른 전원일 수도 있다.

상기의 정류 브리지부(150)는 제 1 외부 단자 전극(210)과 제 2 외부 단자 전극(220)사이에 접속된 제 1 다이오드(D1)와, 제 2 외부 단자 전극(220)과 제 3 외부 단자 전극(230) 사이에 접속된 제 2 다이오드(D2)와, 제 3 외부 단자 전극(230)과 제 4 외부 단자 전극(240) 사이에 접속된 제 3 다이오드(D3)와, 제 4 외부 단자 전극(240)과 제 1 외부 단자 전극(210) 사이에 접속된 제 4 다이오드(D4)를 포함하여 구성하되, 제 2 외부 단자 전극(220) 및 제 4 외부 단자 전극(240)은 각기 발광 칩(100)의 에노드 및 캐소드에 접속된다.

본 실시예에서는 교류 전원은 정류 브리지부(150)를 통해 인가되고, 제 2 외부 단자 전극(220) 및 제 4 외부 단자 전극(240)은 외부로부터 RC필터를 연결하여 사용할 용도로 따로 마련된 것이다. 직류 전원은 발광 셀(100)에 직접 인가된다. 이로써, 본 발명의 발광 소자(200)의 전체 입출력 전극 단자수는 4개가된다. 이때, 2개는 교류 구동용 이고, 나미지 2개는 RC 필터를 병렬로 연결할 용도로 준비되어 있다. RC 필터의 역활은 전류 성분중 리플 요소(Ripple Factor)를 최소화 하기 위함이다.

도 9는 본 발명의 제 4 실시예에 따른 발광 소자를 설명하기 위한 개념도이다.

도 9를 참조하면, 본 실시예의 발광 소자(200)는 직렬 접속된 다수의 발광 셀(100)과, 발광 셀(100)에 소정의 전류를 인가하기 위한 정류 브리지부(150)와, 상기 정류 브리지부(150)에 접속된 외부 단자 전극들(210 및 220)과, 상기 정류 브리지부(150)에 접속되고, LED 어레이의 저항을 조절하기 위한 외부 연결용 음전극(250)과 상기 발광 셀(100)에 접속된 직류용 양전극(260)을 포함한다.

본 실시예에서는 직렬 접속된 다수의 발광 셀(100)의 양전극(260)과 외부 연결용 음전극(250) 사이에 저항체를 임으로 직렬 연결하여 과부하를 방지할 수 있다.

상기의 정류 브리지부(150)는 제 1 외부 단자 전극(210)과 외부 연결용 음전극(250)사이에 접속된 제 1 다이오드(D1)와, 외부 연결용 음전극(250)과 제 2 외부 단자 전극(220) 사이에 접속된 제 2 다이오드(D2)와, 제 2 외부 단자 전극(220)과 발광 셀(100)의 캐소드 사이에 접속된 제 3 다이오드(D3)와, 발광 셀(100)의 캐소드와 제 1 외부 단자 전극(210) 사이에 접속된 제 4 다이오드(D4)를 포함하여 구성된다.

도 10은 본 발명의 제 5 실시예에 따른 발광 소자를 설명하기 위한 개념도이다.

도 10을 참조하면, 본 실시예의 발광 소자(200)는 직렬 접속된 다수의 발광 셀(100)과, 발광 셀(100)에 소정의 전류를 인가하기 위한 정류 브리지부(150)와, 정류 브리지부(150)와 발광 셀(100)에 각기 접속된 외부 단자 전극들(210 내지 240)과, 상기 정류 브리지부(150)에 접속된 외부 연결용 음전극(250)을 포함한다.

본 실시예에서는 정류브리지부(150)의 두 외부 단자(210 및 230)가 교류 전원에 연결되고 직렬 접속된 다수의 발광 셀(100)이 연결된 제 2 및 제 4 외부 단자 전극(220 및 240)에는 병렬로 RC회로가 연결되어 교류 성분의 리플 요소를 최소화 하고, 외부 연결용 음전극(250)에는 직렬로 저항체를 연결하여 발광 셀(100)에 걸리는 과부하를 방지할 수 있는 특징이 있다.

상기의 정류 브리지부(150)는 제 1 외부 단자 전극(210)과 외부 연결용 음전극(250)사이에 접속된 제 1 다이오드(D1)와, 외부 연결용 음전극(250)과 제 3 외부 단자 전극(230) 사이에 접속된 제 2 다이오드(D2)와, 제 3 외부 단자 전극(230)과 제 4 외부 단자 전극(240) 사이에 접속된 제 3 다이오드(D3)와, 제 4 외부 단자 전극(240)과 제 1 외부 단자 전극(210) 사이에 접속된 제 4 다이오드(D4)를 포함하여 구성하되, 제 4 외부 단자 전극(240)은 발광 칩(100)의 캐소드에 접속된다.

본 실시예에서는 전체 입출력 전극 단자수는 5개가 되고, 교류 전원은 정류 브리지부(150)를 통해 인가되고, 나머지 전극들은 각각 외부 연결용 음전극(250), 병렬로 RC회로가 연결되는 두 외부 단자 전극(220 및 240)으로 구성된다.

상술한 바와 같이 브리지부(150)의 외부에 본 발명의 발광 칩(100)이 배치될 수도 있고, 브리지부(150) 내부에 발광 칩(100)이 배치될 수도 있다. 또한, 브리지부(150)를 사용하지 않고, 다수의 발광 칩(100)을 병렬 연결할 수도 있다.

이하 이에 관해 좀더 구체적으로 설명한다.

본 발명의 다른 일 실시예로 직렬 접속된 다수의 발광 셀로 이루어진 발광 셀 블록을 브리지부 내부 즉, 브리지부의 마주보는 접점(직렬 접점들) 사이에 접속시켜 발광 소자의 집적도를 높일 수 있고, 교류전압에서 발광 셀 블록을 구동하도록 하여 조명용 밝기를 갖는 발광 소자를 제공한다. 또한, 브리지부를 이용하지 않고, 적어도 2개 이상의 발광 셀 블록을 병렬 연결시켜 교류 전압에서 엇갈려가며 발광 셀 블록이 발광하도록 하여 조명용 밝기를 갖는 발광 소자를 제공한다.

먼저, 브리지부 내에 다수의 발광 셀이 직렬 접속된 발광 셀 블록이 형성된 발광 소자를 살펴보면 다음과 같다.

도 11은 본 발명의 제 6 실시예에 따른 발광 소자를 설명하기 위한 개념도이다.

도 11을 참조하면, 직렬 접속된 다수의 발광 셀(100)을 포함하는 발광 셀 블록(1000)과, 직렬 접점에 상기 발광 셀 블록(1000)이 접속된 브리지 회로를 포함한다.

브리지부는 4개의 다이오드 블록(310 내지 340)을 포함하고 있고, 제 1 및 제 2 다이오드 블록(310 및 320)은 제 1 직렬 노드(SN1)에 의해 직렬 접속되고, 제 3 및 제 4 다이오드 블록(330 및 340)은 제 2 직렬 노드(SN2)에 의해 직렬 접속된다. 또한, 각기 직렬 접속된 제 1 및 제 2 다이오드 블록(310 및 320)과 제 3 및 제 4 다이오드 블록(330 및 340)은 제 1 및 제 2 병렬 노드(PN1 및 PN2)에 의해 병렬 접속된다. 여기서, 제 1 및 제 2 병렬 노드(PN1 및 PN2)는 외부의 교류전원과 접속하기 위한 소정의 전원 패드(410 및 420)에 접속된다.

이때, 제 1 내지 제 4 다이오드 블록(310 내지 340) 각각은 적어도 한개 이상의 다이오드(311)를 포함하여 이루어진다. 도 4에서는 2개의 발광 다이오드를 하나의 다이오드 블록으로 구성하였다. 또한, 제 1 및 제 2 다이오드 블록(310 및 320) 각각은 직렬 노드에서 병렬 노드로 소정의 전류가 흐르게 하고, 제 3 및 제 4 다이오드 블록(330 및 340) 각각은 병렬 노드에서 직렬 노드로 소정의 전류가 흐르게 구성하는 것이 바람직하다. 물론 이에 한정되지 않고 다양한 실시예가 가능하다.

상술한 구성의 본 발명의 일 실시예에 따른 발광 소자는 소정의 전원부(미도시)를 포함하여 발광 장치로써 구동한다. 이러한 발광 장치의 구동을 상기 도 12의 회로도를 통해 설명하면, 먼저 외부의 전원패드(410 및 420)를 통해 교류 전압이 인가되면 브리지부의 제 1 및 제 2 병렬노드(PN1 및 PN2)에 소정의 교류 전압이 인가된다. 만일, 제 1 병렬 노드(PN1)에 + 전압이 인가되고, 제 2 병렬 노드(PN2)에 -전압이 인가될 경우, 전류가 제 1 병렬 노드(PN1), 제 3 다이오드 블록(330), 발광 셀 블록(1000), 제 2 다이오드 블록(320) 및 제 2 병렬 노드(PN2)를 통해 흐르게 되어 발광 셀 블록(1000)을 발광시킨다. 한편, 제 1 병렬 노드(PN1)에 -전압이, 제 2 병렬 노드(PN2)에 + 전압이 인가될 경우는, 전류가 제 2 병렬 노드(PN2), 제 4 다이오드 블록(340), 발광 셀 블록(1000), 제 1 다이오드 블록(310) 및 제 1 병렬 노드(PN1)를 통해 흐르게 되어 발광 셀 블록(1000)을 발광시킨다. 이와 같이 외부의 교류 전원의 전압 상태에 상관없이 본 실시예의 발광 소자는 외부 전원이 인가되면 계속적인 발광을 할 수 있다.

다음으로, 브리지부를 이용하지 않고, 적어도 2개 이상의 발광 셀 블록(다수의 발광 셀이 직렬 접속된)을 병렬 연결시켜 제작된 발광 소자를 살펴본다.

도 12는 본 발명의 제 7 실시예에 따른 발광 소자를 설명하기 위한 개념도이다.

도 12를 참조하면, 직렬 접속된 다수의 발광 셀(100)을 포함하는 적어도 2개 이상의 발광 셀 블록(1000a 및 1000b)이 병렬 접속된다.

상기의 도 12에서는 제 1 발광 셀 블록(1000a)과 제 2 발광 셀 블록(1000b)이 제 10 및 제 20 병렬 노드(PN10 및 PN20) 사이에 병렬 접속되어 있다. 제 10 및 제 20 병렬 노드(PN10 및 PN20) 각각은 제 1 및 제 2 전원 패드(410 및 420)에 접속된다. 이때, 제 1 발광 셀 블록(1000a)의 캐소드는 제 10 병렬 노드(PN10)에 접속되고, 애노드는 제 20 병렬 노드(PN20)에 접속되며, 제 2 발광 셀 블록(1000b)의 캐소드는 제 20 병렬 노드(PN20)에 접속되고, 애노드는 제 10 병렬 노드(PN10)에 접속된다. 이는 일 실시예일뿐, 2개 이상의 발광 셀 블록(1000)이 병렬 연결될 수도 있다. 또한, 병렬 연결된 두개의 발광 셀 블록(1000a 및 1000b) 각각은 도 3에서 언급한 전체 발광 셀 블록(1000)의 발광 셀(100) 개수의 절반 정도의 개수의 발광 셀(100)이 포함되어 구성될 수도 있다. 즉, 발광 소자에 포함된 발광 셀 블록(1000)내의 발광 셀이 40이면, 제 1 발광 셀 블록(1000a)내에 20개, 제 2 발광 셀 블록(1000b)내에 20개로 나누어질 수 있다. 물론 제 1 및 제 2 발광 셀 블록(1000a 및 1000b)내의 발광 셀(100)의 개수는 이와 같이 한정되지 않는다. 하지만, 발광소자의 밝기의 변화를 최소화하기 위해 제 1 및 제 2 발광 셀 블록(1000a 및 1000b) 내의 발광 셀(100)의 개수가 동일한 것이 바람직하다.

상술한 구성의 본 발명의 다른 일 실시예에 따른 발광 소자는 소정의 전원부(미도시)를 포함하여 발광 장치로써 구동한다.

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이러한 발광 장치의 구동을 상기 도 12의 회로도를 통해 설명하면, 먼저 외부의 전원패드(410 및 420)를 통해 교류 전압이 인가된다. 이경우 만일, 제 10 병렬 노드(PN10)에 + 전압이 인가되고, 제 20 병렬 노드(PN20)에 -전압이 인가될 경우, 제 2 발광 셀 블록(1000b)이 발광하게 된다. 또한, 제 10 병렬 노드(PN10)에 -전압이, 제 20 병렬 노드(PN20)에 + 전압이 인가될 경우, 제 1 발광 셀 블록(1000a)이 발광하게 된다. 즉, 외부의 교류 전원이 발광 소자에 인가되더라도 제 1 및 제 2 발광 셀 블록(1000a 및 1000b)이 번갈아 가면서 발광하기 때문에 교류전원에서도 충분히 사용이 가능하다. 또한 가정에서 사용되는 전원은 60Hz 이므로 두개의 발광 셀 블록(1000a 및 1000b)이 번갈아 가면서 발광하여도 아무런 문제가 없다.

이로써, 별도의 정류회로 없이도 교류에서 구동가능하고, 단일 셀만을 이용하기 때문에 공정을 간소화할 수 있다. 또한, 이와 같이 웨이퍼 레벨에서 다수의 발광 셀이 결합된 발광 소자를 이용하여 조명용 장치를 제조할 수 있다. 즉 본 발명의 발광 소자를 종래의 발광 장치에 사용할 수 있다. 예를 들어 본 발명의 발광 소자의 전원 패드에 소정의 전압을 인가하는 전원부 접속시켜 발광 장치를 형성할 수 있다. 상기 전원부로는 1V 내지 500V를 인가하는 장치가 가능하고, 통상적으로 가정에서 사용하는 전압 및 손전등과 같은 발광 장치에서 사용하는 전압을 발생하는 장치를 사용할 수 있다. 또한, 전원 패드와 전원부 사이에는 전압강하를 위한 소정의 전압 분배부를 더 포함할 수도 있다. 이와같이 본 발명의 발광 소자는 종래의 전구와 같은 조명소자를 대신할 수 있다.

상술한 제 1 내지 제 7 실시예에 따른 발광 소자는 다양한 형상의 어레이가 가능하다. 즉, 발광 소자는 다수의 발광 셀이 매트릭스 배열된 발광 셀 블록과, 발광 셀 블록의 양측면에 각기 형성된 브리지용 제 1 내지 제 4 다이오드 블록을 포함한다. 구체적으로, 제 1 및 제 3 다이오드 블록은 상기 발광 셀 블록의 일측면(좌측)에 형성되고, 제 2 및 제 4 다이오드 블록은 상기 발광 셀 블록의 다른 일 측면(우측)에 형성되었다. 이때, 만일 제 7 실시예와 같이 병렬 연결일 경우에는 전원패드(즉, 병렬노드)에 병렬 접속되고 각기 다수의 발광 셀을 포함하는 제 1 및 제 2 발광 셀 블록을 포함하되, 상기 제 1 및 제 2 발광 셀 블록내의 다수의 발광 셀들은 매트릭스 배열되어 있고, 각각의 발광 셀 블록 별로 직렬 접속되어 있다. 물론 이에 한정되지 않고, 전기적 연결의 편의를 위해 다양한 배치가 가능하다. 이때 제 1 내지 제 4 다이오드와 발광 셀 블록간은 도 7 내지 10에서 도시된 바와 같이 연결되기 위한 별도의 패드와 같은 연결부를 가질수 있다.

다음으로, 이러한 발광 소자를 이용한 발광 장치에 관해 설명하면 다음과 같다.

도 13은 본 발명에 따른 발광 장치를 설명하기 위한 개념도이다.

본 발명의 전원부와, 다수의 발광 셀이 직렬 접속된 발광 셀 블록을 포함하는 발광 소자와, 발광 소자에 인가되는 전압 및 전류의 파형을 조절하기 위한 제어부를 포함한다.

상기 도 13에서는 전원부(510)로 교류 전원이 인가되고, 제어부(520)에 구성된 병렬 RC회로와 직렬 저항체를 발광소자(200)부에 연결하는 형태로 구성된다.

제어부(520)는 발광 소자(200) 내부의 발광 셀(100)과 각기 병렬 접속된 커패시터(C1) 및 제 1 저항(R1)을 포함한다. 발광 셀(100)과 직렬 접속된 제 2 저항(R2)을 더 포함할 수도 있다.

이를 도 13을 참조하여 조명용 발광 장치의 구조 및 동작에 관해 구체적으로 설명한다.

발광 소자(200)의 정류 브리지부(150)는 제 1 및 제 2 외부 단자 단자를 통해 교류 전원과 접속된다. 제 1 및 제 2 외부 단자 단자가 접속되지 않는 정류 브리지부(150)의 두 노드 사이에 제 2 저항(R2)과 발광 셀(100)부가 직렬 접속된다. 또한, 제 1 및 제 2 외부 단자가 접속되지 않는 정류 브리지부(150)의 두 노드에 제 1 커패시터(C1)와 제 1 저항(R1)이 각기 병렬 접속된다. 즉, 직렬 접속된 제 2 저항(R2)과 발광 셀(100)부가 제 1 커패시터(C1) 및 제 1 저항(R1)과 각기 병렬 접속된다.

따라서, 본 발광 장치에 교류 전원을 인가시키면 발광 소자(200)내의 정류 브리지부(150)를 통해 양과 음으로 구분된 전류가 발광 셀(100)부의 양방향으로 인가되고, 이로써, 순차적으로 발광을 하게 된다. 또한, 각각 병렬로 접속된 커패시터(C1)와, 저항(R1 및 R2)으로 인해 전류의 파형이 조절된다.

발명의 효과

상술한 바와 같이, 본 발명은 수직 타입의 다수의 발광 셀이 직렬 접속된 발광 셀 블록을 포함하는 발광 소자를 통해 조명용으로 사용할 수 있는 발광 장치를 제작할 수 있다.

또한, 웨이퍼 레벨에서 다수의 발광 셀을 전기적으로 연결하기 때문에 고전원 또는 가정용 교류 전원에서 발광할 수 있는 발광 소자를 제작할 수 있다.

또한, 다수의 발광 셀이 기판상에서 전기적으로 연결된 발광 소자를 사용하기 때문에 조명용 발광 장치의 제작 공정을 단순화시킬 수 있고, 조명용 발광 장치이 제작시 발생하는 불량률을 줄일 수 있으면, 조명용 발광 장치를 대량 생산할 수 있다.

또한, 발광 소자 칩의 전극과 소정의 정류 회로를 연결하여 교류 동작시 리플 요소를 최소화 하여 발광 효율을 극대화하고 저하체의 설치를 통해 LED 어레이에 걸리는 부하를 조절하여 발광 소자 칩을 보호할 수 있다.

(57) 청구의 범위

청구항 1.

호스트기판; 및

상기 호스트기판상에 직렬 또는 직병렬 연결된 다수의 수직형 발광셀;을 포함하여 구성된 발광소자.

청구항 2.

제 1항에 있어서,

상기 호스트기판은, 도체, 부도체, 및 반도체 기판중 어느 일측으로 구성되는 것을 특징으로 하는 발광소자.

청구항 3.

제 2항에 있어서,

상기 부도체 호스트기판과 상기 다수의 발광셀 사이에는 전극패턴층이 형성되어 있는 것을 특징으로 하는 발광소자.

청구항 4.

제 2항에 있어서,

상기 도체 또는 반도체 호스트기판과 상기 발광셀 사이에는, 상기 호스트기판측에 절연층이, 상기 다수의 발광셀측에 전극패턴층이 개재되어 있는 것을 특징으로 하는 발광소자.

청구항 5.

제 1항 내지 제 4항 중 어느 한 항에 있어서,

상기 다수의 수직형 발광셀은 각각 GaN계 반도체를 포함하는 것을 특징으로 하는 발광소자.

청구항 6.

모체기판에 화합물반도체를 성장시키는 단계;

상기 화합물반도체를 다수의 수직형 발광셀로 형성한 후, 상기 각각의 수직형 발광셀의 상부에 제 1전극을 형성하는 단계;

상기 수직형 발광셀의 상부에 호스트기판을 부착하는 단계;

상기 모체기판을 제거한 후 상기 각 수직형 발광셀의 하부에 제 2전극을 형성하는 단계; 및

상기 각 수직형 발광셀의 제 1전극들과 인접하는 수직형 발광셀의 제 2전극들을 직렬 또는 직병렬로 연결하는 단계;를 포함하는 발광소자 제조방법.

청구항 7.

제 6항에 있어서, 상기 호스트기판이 도체 또는 반도체기판인 경우,

상기 호스트기판과 상기 수직형 발광셀의 제 1전극 사이에 절연층을 형성하는 단계를 더 포함하는 것을 특징으로 하는 발광소자 제조방법.

청구항 8.

모체기판에 화합물반도체를 성장시키는 단계;

상기 화합물반도체를 다수의 수직형 발광셀로 형성하는 단계;

상기 다수의 수직형 발광셀의 상부에 호스트기판을 부착하는 단계; 및

상기 각 수직형 발광셀을 인접하는 수직형 발광셀들과 직렬 또는 직병렬로 연결하는 단계;를 포함하는 발광소자 제조방법.

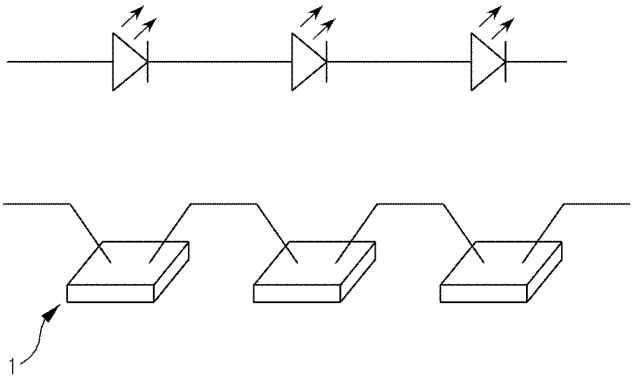
청구항 9.

제 6항 또는 제 8항에 있어서,

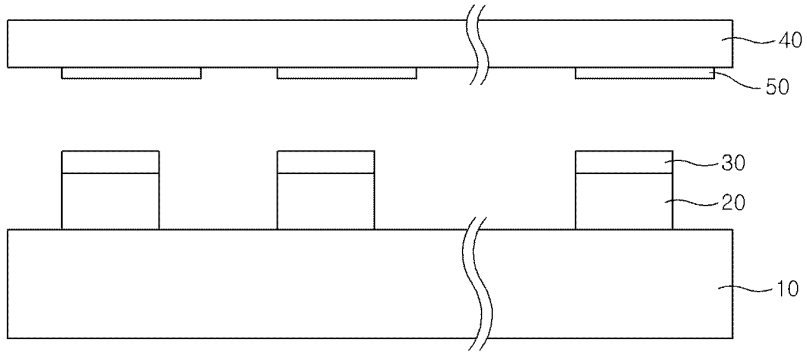
상기 모체기판은 레이저를 이용한 리프트오프공정, 식각공정, 또는 CMP공정으로 제거되는 것;을 특징으로 하는 발광소자 제조방법.

도면

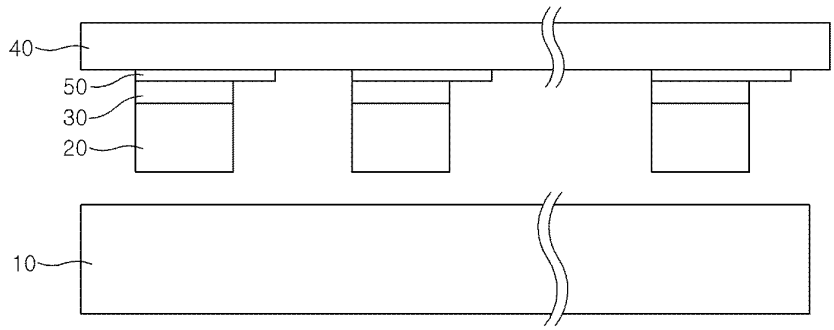
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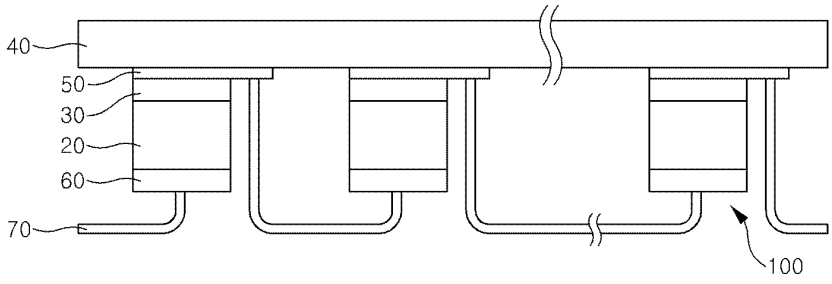
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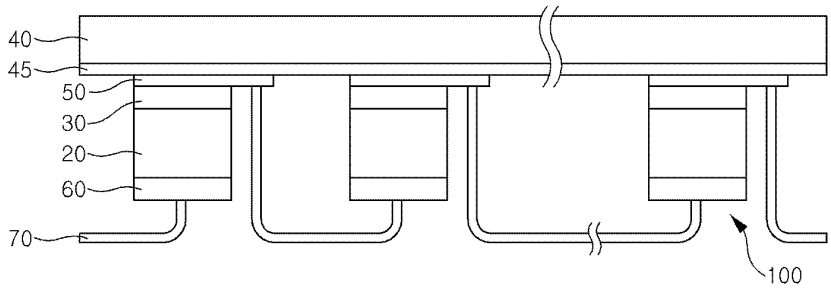
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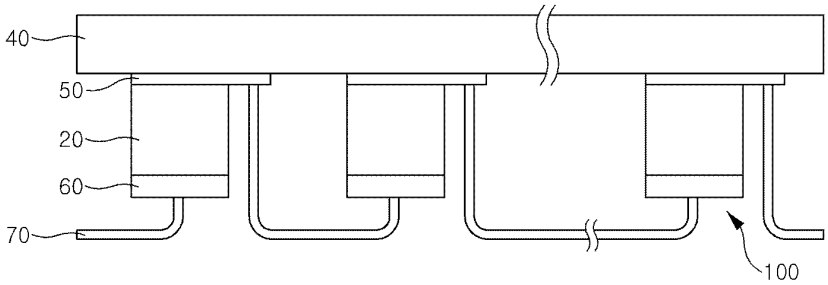
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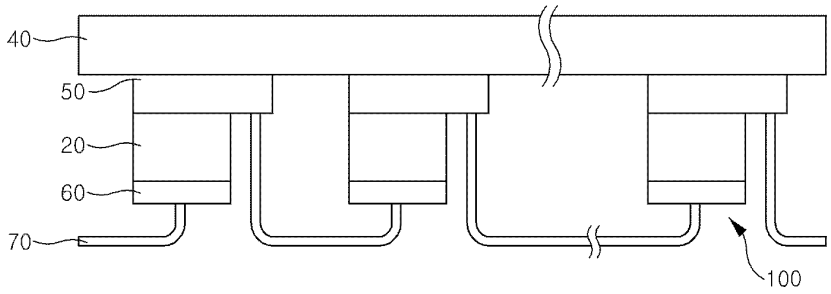
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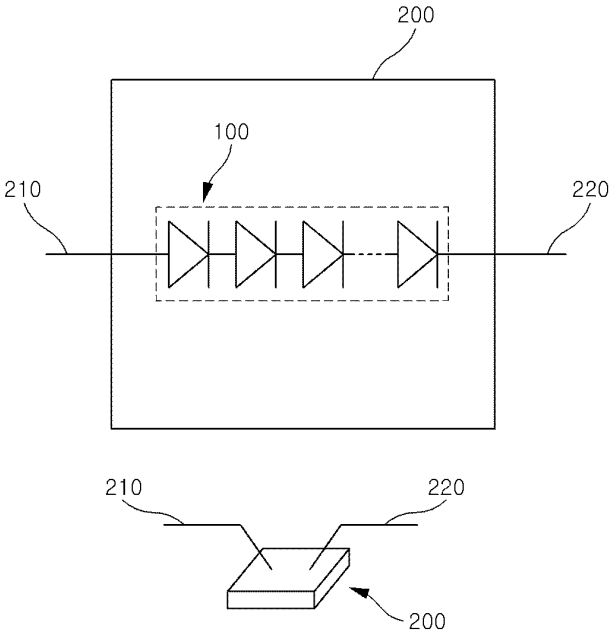
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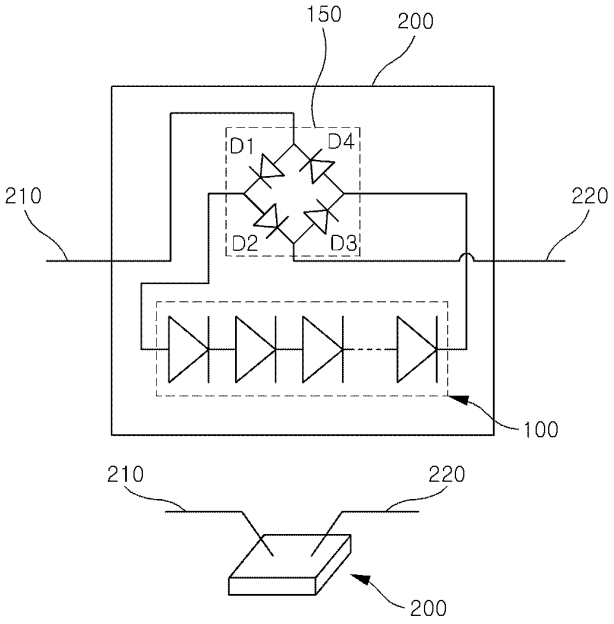
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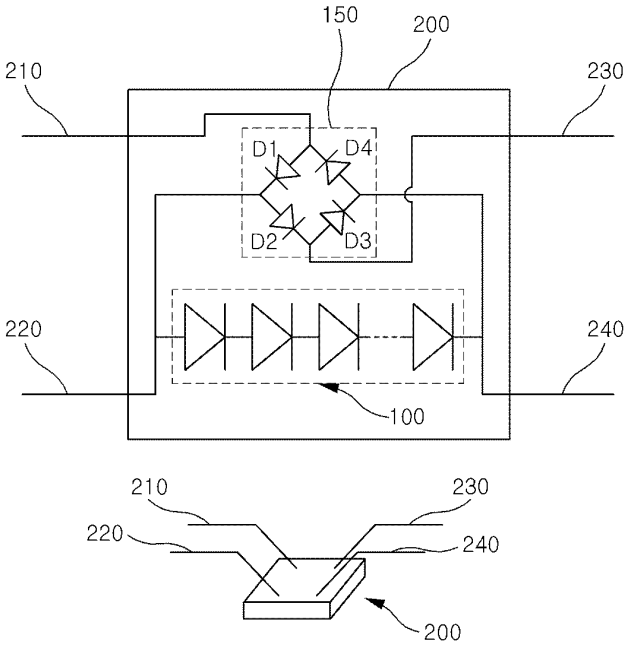
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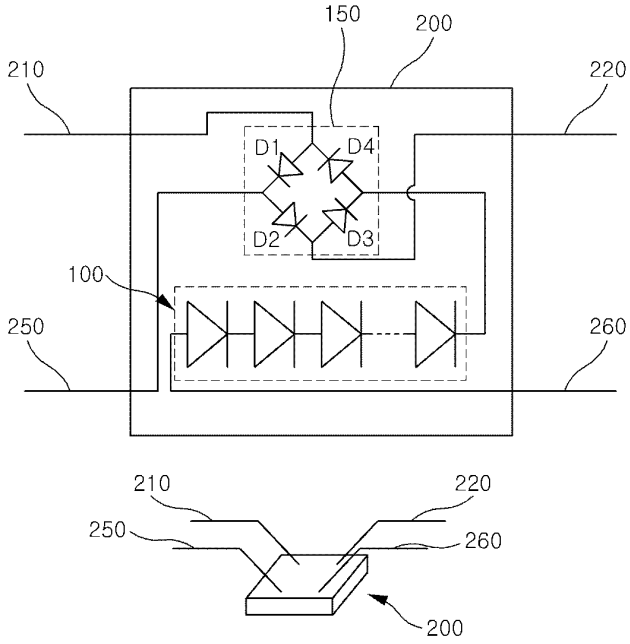
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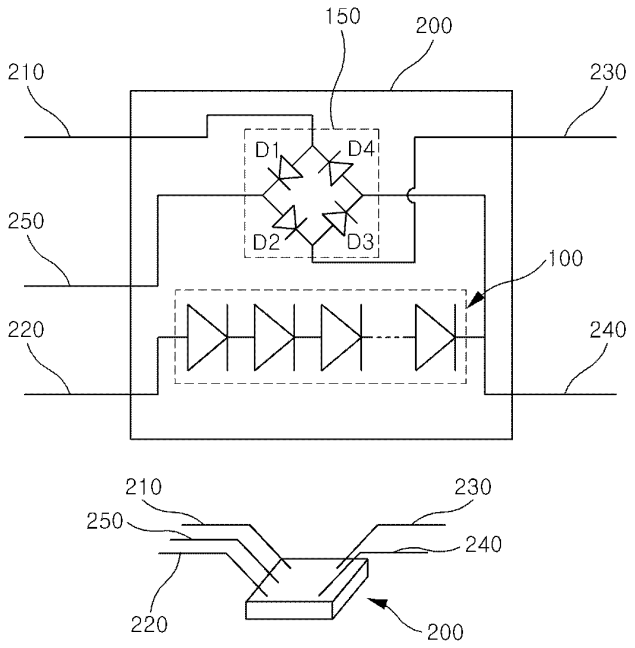
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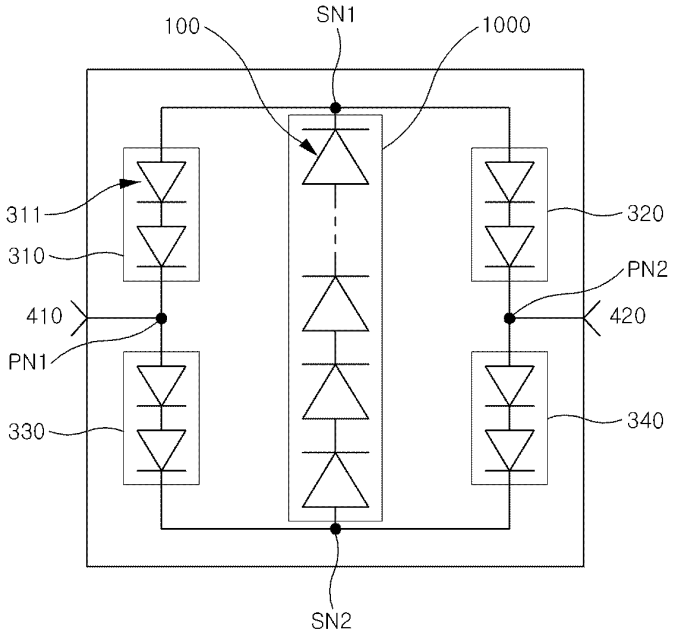
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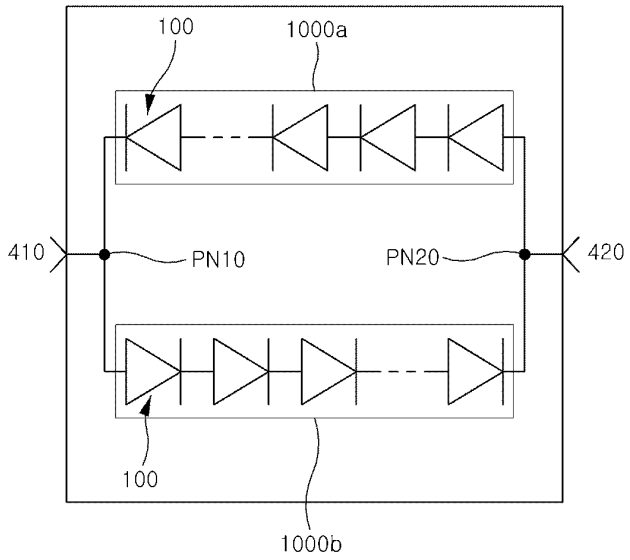
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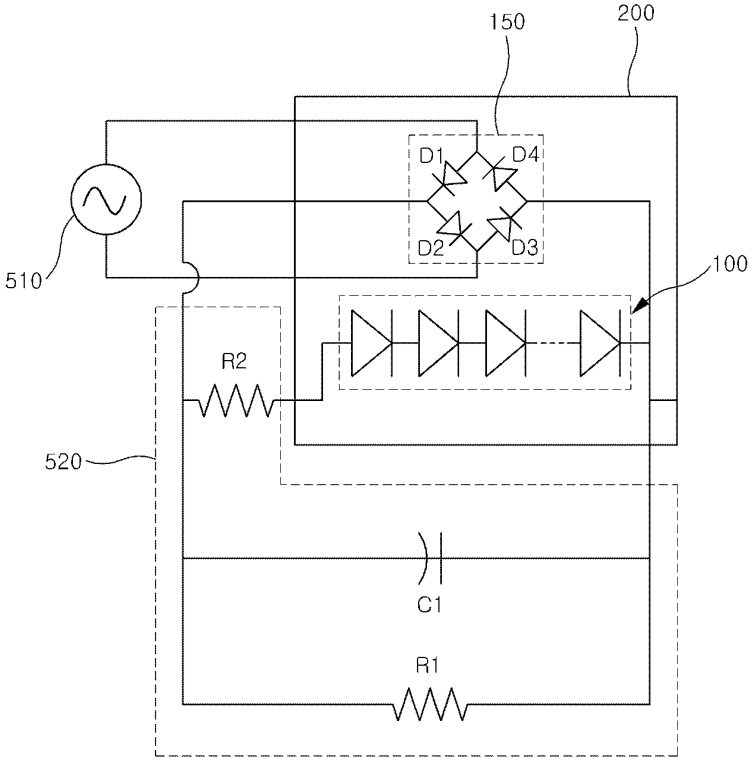
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도면13


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Electronic Acknowledgement Receipt

EFS ID:	3862532
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
Receipt Date:	29-AUG-2008
Filing Date:	26-DEC-2007
Time Stamp:	19:53:35
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	P2317US00-IDSTransmittal.pdf	771247 48670779f76d0a7e6e7f30bd87f6e48933e7f9ea	no	4

Warnings:	
Information:	

2	Foreign Reference	P2317US00-KR10-2005-66358.pdf	578876 05dfe614210c9b8ca390fec85aef43994c8f1c48	no	12
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3	Foreign Reference	P2317US00-JP2002-26378.pdf	565242 8e51009847ebe17eb4fc81641fa46ee63d864b9e	no	8
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			Total Files Size (in bytes):	2747903	

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If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/993,965	12/26/2007	Jong Lam Lee	P2317US00

CONFIRMATION NO. 2191

58027
H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

PUBLICATION NOTICE



Title: Light Emitting Device and Method of Manufacturing the Same

Publication No.US-2008-0251796-A1
Publication Date:10/16/2008

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PTO/SB/08a (01-09)
Approved for use through 02/28/2009. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(**Not for submission under 37 CFR 1.99)**

Application Number	11993965
Filing Date	2007-12-26
First Named Inventor	Jong Lam LEE
Art Unit	2811
Examiner Name	
Attorney Docket Number	P2317US00

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	04-023568	WO		2004-03-18	Nitride Semiconductors Co., Ltd.		☐
	2	04-013916	WO		2004-02-12	Nichia Corporation		☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
	Art Unit	2811
	Examiner Name	
	Attorney Docket Number	P2317US00

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		☐

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
	Art Unit	2811
	Examiner Name	
	Attorney Docket Number	P2317US00

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2009-02-09
Name/Print	Hae-Chan Park	Registration Number	50114

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

(12)特許協力条約に基づいて公開された国際出願

(19) 世界知的所有権機関
国際事務局

(43) 国際公開日
2004 年3 月18 日 (18.03.2004)

PCT

(10) 国際公開番号
WO 2004/023568 A1

(51) 国際特許分類[7]: H01L 33/00

(21) 国際出願番号: PCT/JP2003/010922

(22) 国際出願日: 2003 年8 月28 日 (28.08.2003)

(25) 国際出願の言語: 日本語

(26) 国際公開の言語: 日本語

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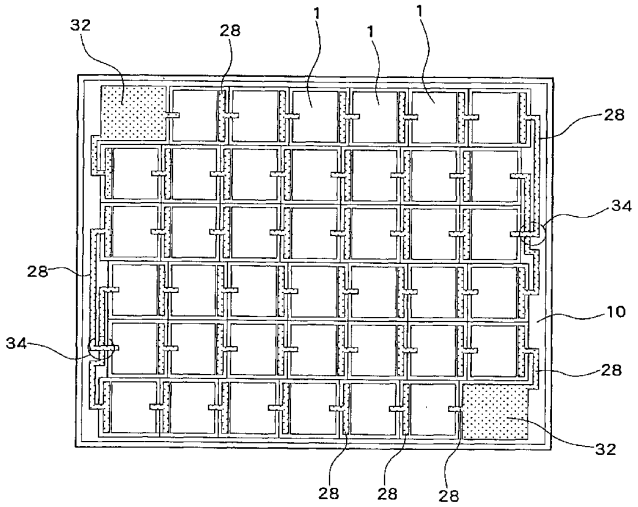
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[続葉有]

(54) Title: LIGHT-EMITTING DEVICE HAVING LIGHT-EMITTING ELEMENTS

(54) 発明の名称: 複数の発光素子を有する発光装置



(57) Abstract: A light-emitting device operating on a high drive voltage and a small drive current. LEDs (1) are two-dimensionally formed on an insulating substrate (10) of e.g., sapphire monolithically and connected in series to form an LED array. Two such LED arrays are connected to electrodes (32) in inverse parallel. Air-bridge wiring (28) is formed between the LEDs (1) and between the LEDs (1) and electrodes (32). The LED arrays are arranged zigzag to form a plurality of LEDs (1) to produce a high drive voltage and a small drive current. Two LED arrays are connected in inverse parallel, and therefore an AC power supply can be used as the power supply.

(57) 要約: 高い駆動電圧及び低い駆動電流で動作する発光装置。サファイア等の絶縁基板（１０）上に複数のＬＥＤ（１）を二次元的にモノリシック形成し、複数のＬＥＤ（１）を直列接続してＬＥ

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Ｄアレイとする。２組のＬＥＤアレイを互いに逆極性で電極（３２）に接続する。ＬＥＤ（１）の間及びＬＥＤ（１）と電極（３２）間はエアブリッジ配線（２８）とする。ＬＥＤアレイをシグザグ状に配置することで多数のＬＥＤ（１）を形成し、高い駆動電圧と低い駆動電流を得る。２つのＬＥＤアレイは逆極性であるため、電源として交流電源を使用できる。

明　細　書

複数の発光素子を有する発光装置

技術分野

本発明は、基板上に複数の発光素子が形成された発光装置に関する。

背景技術

発光素子（ＬＥＤ）等の発光手段が表示用途等に使用される場合には、その使用条件が駆動電圧約１～４Ｖ、駆動電流が約２０ｍＡとなっている。ところで、近年ＧａＮ系化合物半導体を用いた短波長ＬＥＤが開発され、フルカラーや白色等の固体光源が実用化されたことに伴い、次第にＬＥＤを照明用途にも応用することが検討されている。ＬＥＤを照明用途に応用する場合に、上述した駆動電圧１～４Ｖ、駆動電流２０ｍＡという使用条件とは異なる条件で使用される事態も生じる。このため、ＬＥＤにより大電流を流し、発光出力を大きくする工夫がなされている。大電流を流すためには、ＬＥＤのｐｎ接合面積を大きくし、電流密度を小さく抑える必要がある。

ＬＥＤを照明用光源として使用する場合には、電源として交流を使用し、１００Ｖ以上の駆動電圧で使用できることが便利である。また、同じ電力を投入して同じ発光出力を得るのであれば、低い電流値を保ちながら高い電圧を印加した方が電力損失を小さくすることができる。しかし、従来のＬＥＤでは、必ずしも十分に駆動電圧を高くすることはできなかった。

発明の開示

本発明の目的は、高い駆動電圧で動作できる発光装置を提供することにある。

本発明は、絶縁基板上に複数のＧａＮ系発光素子が形成され、前記複数の発光素子がモノリシックに直列接続されることを特徴とする。

ここで、前記複数の発光素子は、前記基板上に二次元配置されていることが好

適である。

また、前記複数の発光素子は２組に分けられ、２個の電極に互いに反対極性となるように並列接続されてもよい。

前記複数の発光素子間の接続はエアブリッジ配線としてもよい。

前記複数の発光素子間の電気的な分離は、前記基板として使用されるサファイアにより行われてもよい。

また、前記複数の発光素子は同数ずつ２組に分けられ、各組の発光素子アレイはジグザグ状に配置し、かつ、２組の発光素子アレイは２個の電極に互いに反対極性となるように並列接続されてもよく、前記２組の発光素子アレイは、互い違いに配置してもよい。

また、前記発光素子及び電極は、平面形状が略正方形あるいは三角形状としてもよい。

また、前記複数の発光素子及び電極は、全体形状が略正方形となるように配置してもよい。

本発明において、電極は、交流電源用電極とすることができる。

また、前記２組の発光素子アレイは、共通のｎ電極を有してもよい。

本発明では複数の発光素子をモノリシックに、すなわち同一基板上に形成し、これらを直列接続することで、高駆動電圧を可能とする。複数の発光素子を一方向に接続することで直流駆動が可能となるが、複数の発光素子を２組に分け、各組の発光素子（発光素子アレイ）を互いに逆極性となるように電極に接続することで交流駆動も可能となる。各組の個数は同数でもよく、あるいは異なっていてもよい。

複数の発光素子を二次元配列する方法は種々存在するが、基板専有面積をできるだけ小さくすることが望ましい。例えば、２組の発光素子アレイをそれぞれジグザグ状に、すなわち複数の発光素子を折れ曲がった直線上に配置し、それぞれの発光素子アレイを互い違いに配置することで、基板面積を有効活用して多数の発光素子を接続することができる。２組の発光素子アレイを互い違いに配置することで、配線の交叉部分が生じる場合もあるが、発光素子間をエアブリッジ配線で接続することにより交叉部分での短絡を有効に防止できる。発光素子及び電極

の形状は任意であるが、例えば平面形状が略正方形となるように形成することで全体形状も略正方形となり、標準的なマウント構造を使用できる。発光素子及び電極を正方形以外、例えば三角形とした場合でも、これらの三角形状を組み合わせることで全体として略正方形を形成すれば、同様に標準的なマウント構造を使用できるようになる。

図面の簡単な説明

図１は、発光素子（ＬＥＤ）の基本構成図である。

図２は、発光装置の等価回路図である。

図３は、２個のＬＥＤの平面図である。

図４は、図３のＩＶ－ＩＶ断面図である。

図５は、発光装置の他の等価回路図である。

図６は、４０個のＬＥＤを二次元配列した説明図である。

図７は、図６の回路図である。

図８は、６個のＬＥＤを二次元配列した説明図である。

図９は、図８の回路図である。

図１０は、１４個のＬＥＤを二次元配列した説明図である。

図１１は、図１０の回路図である。

図１２は、６個のＬＥＤを二次元配列した説明図である。

図１３は、図１２の回路図である。

図１４は、１６個のＬＥＤを二次元配列した説明図である。

図１５は、図１４の回路図である。

図１６は、２個のＬＥＤを配列した説明図である。

図１７は、図１６の回路図である。

図１８は、４個のＬＥＤを二次元配列した説明図である。

図１９は、図１８の回路図である。

図２０は、３個のＬＥＤを二次元配列した説明図である。

図２１は、図２０の回路図である。

図２２は、６個のＬＥＤを二次元配列した説明図である。

図２３は、図２２の回路図である。

図２４は、５個のＬＥＤを二次元配列した説明図である。

図２５は、図２４の回路図である。

図２６は、他の二次元配置説明図である。

図２７は、図２６の回路図である。

図２８は、他の二次元配置説明図である。

図２９は、図２８の回路図である。

図３０は、他の二次元配置説明図である。

図３１は、図３０の回路図である。

発明を実施するための最良の形態

以下、図面に基づき本発明の実施形態について説明する。

図１には、本実施形態においてＧａＮ系化合物半導体発光素子としてのＬＥＤ１の基本構成が示されている。ＬＥＤ１は、基板１０上に順次ＧａＮ層１２、Ｓｉドープのｎ型ＧａＮ層１４、ＩｎＧａＮ発光層１６、ＡｌＧａＮ層１８、ｐ型ＧａＮ層２０が積層され、ｐ型ＧａＮ層２０に接してｐ電極２２、ｎ型ＧａＮ層１４に接してｎ電極２４が形成される構成である。

図１に示されたＬＥＤは以下のプロセスにより作製される。すなわち、まず、ＭＯＣＶＤ装置にてサファイアｃ面基板を水素雰囲気中で１１００℃、１０分間熱処理する。そして、温度を５００℃まで降温させ、シランガスとアンモニアガスを１００秒間供給して不連続なＳｉＮ膜を基板１０上に形成する。なお、このプロセスはデバイス中の転位密度を低減させるためのものであり、図ではＳｉＮ膜は省略している。次に、同一温度でトリメチルガリウム及びアンモニアガスを供給してＧａＮ層を２０ｎｍ厚成長させる。温度を１０５０℃に昇温し、再びトリメチルガリウム及びアンモニアガスを供給してアンドープＧａＮ（ｕ－ＧａＮ）層１２及びＳｉドープのｎ型ＧａＮ層１４を各２μｍ厚成長させる。その後、温度を７００℃程度まで降温してＩｎＧａＮ発光層１６を２ｎｍ厚成長させる。目標組成はｘ＝０．１５、すなわち$In_{0.15}Ga_{0.85}N$である。発光層１６成長後、温度を１０００℃まで昇温してＡｌＧａＮ正孔注入層１８を成長させ、さら

にｐ型ＧａＮ層２０を成長させる。

ｐ型ＧａＮ層２０を成長させた後、ウエハをＭＯＣＶＤ装置から取り出し、Ｎｉ１０ｎｍ厚、Ａｕ１０ｎｍ厚を順次真空蒸着で成長層表面に形成する。５％の酸素を含む窒素ガス雰囲気中で５２０℃熱処理することで金属膜はｐ型透明電極２２となる。透明電極形成後、全面にフォトレジストを塗布し、ｎ型電極形成のためのエッチングをフォトレジストをマスクとして行う。エッチング深さは、例えば６００ｎｍ程度である。エッチングで露出したｎ型ＧａＮ層１４上にＴｉ５ｎｍ厚、Ａｌ５ｎｍ厚を形成し、窒素ガス雰囲気中で４５０℃、３０分間熱処理してｎ型電極２４を形成する。最後に、基板１０の裏面を１００μｍまで研磨してチップを切り出し、マウントすることでＬＥＤ１が得られる。

図１では、基板１０上に一つのＧａＮ系ＬＥＤ１が形成されているが、本実施形態では、基板１０上にＬＥＤ１をモノリシックに、かつ二次元アレイ状に複数形成し、各ＬＥＤを接続して発光装置（チップ）を構成する。ここで、モノリシック」とは、１個の基板上に全ての素子が形成されていることを意味する。

図２には、発光装置の等価回路図が示されている。図２において、２次元アレイ状に形成された発光素子群は同数（図では４個）ずつ２組に分けられ、各組のＬＥＤ１はそれぞれ直列接続され、２組のＬＥＤ列は電極（駆動電極）に対して逆極性となるように並列接続される。このようにＬＥＤ列が直列接続されることにより、各々の駆動電圧が加算された高い電圧でＬＥＤ１を駆動することができる。また、各ＬＥＤ列はその極性が互いに反対となるように電極に並列接続されているので、電源として交流電源を使用した場合にも、電源の各周期中に必ずどちらかのＬＥＤ列が発光していることになるので、効率のよい発光を行うことができる。

図３には、基板１０上にモノリシックに形成された複数のＬＥＤの部分的な平面図が示されている。また、図４は、図３のＩＶ－ＩＶ断面図が示されている。図３において、ＬＥＤ１の上面には、図１に示されるようにｐ電極２２及びｎ電極２４が形成されている。隣接するＬＥＤ１のｐ電極２２とｎ電極２４との間がエアブリッジ配線２８により接続され、複数のＬＥＤ１が直列接続される。

図４において、各ＬＥＤ１は説明の都合上簡略的に示されている。すなわち、

ｎ－ＧａＮ層１４、ｐ－ＧａＮ層２０、ｐ－電極２２、ｎ－電極２４のみが示されている。実際には図１に示されるようにＩｎＧａＮ発光層１６等が存在することは云うまでもない。エアブリッジ配線２８は、ｐ電極２２からｎ電極２４までを空中を介して接続する。これにより、素子表面に絶縁膜を塗布し、この上に電極を形成してｐ電極２２とｎ電極２４とを電気的に接続する方法に比べ、エッチング溝に沿って電極を配置する必要が無くなるので、配線切れや絶縁膜からｎ層、ｐ層へ絶縁材料を構成する元素が熱拡散してＬＥＤ１を劣化させるという問題を回避できる。エアブリッジ配線２８は、ＬＥＤ１間のみならずＬＥＤ１と図示しない電極との間の接続にも使用される。

また、図４に示されるように、各ＬＥＤ１は互いに独立し、電気的に絶縁される必要がある。このため、各ＬＥＤ１はサファイア基板１０上で分離された構成となっている。サファイアはそれ自身絶縁体であるので、ＬＥＤ１をそれぞれ電気的に分離することができる。このように、サファイア基板１０をＬＥＤの電気的な分離を行うための抵抗体として使用することにより、容易かつ確実にＬＥＤの電気的な分離を行うことができる。

なお、発光素子としては、ｐｎ接合を有するＬＥＤの他、ＭＩＳとすることもできる。

図５には、発光装置の他の等価回路図が示されている。図において、２０個のＬＥＤ１が直列接続されて１つのＬＥＤアレイを形成しており、２つのＬＥＤアレイ（合計４０個のＬＥＤ）が電源に並列に接続されている。ＬＥＤ１の駆動電圧は５Ｖに設定されており、各ＬＥＤアレイの駆動電圧は１００Ｖとなっている。２つのＬＥＤアレイは図２と同様に互いに反対極性となるように電源に並列接続されており、電源の極性がいずれであっても必ずどちらかのＬＥＤアレイが発光することになる。

図６には、二次元アレイが具体的に示されている。図２の等価回路図に対応するものである。図において、サファイア基板１０上に合計４０個のＬＥＤ１が形成されており、それぞれ２０個ずつ２組に分けられ、エアブリッジ配線２８により直列接続されて２つのＬＥＤアレイを形成している。より詳細には、各ＬＥＤ１は全て同形の正方形で同サイズであり、１つのＬＥＤアレイは上から６個、７

個、７個とそれぞれ直線上に配置され、上から第１列目（６個）と第２列目（７個）は互いに逆向きに形成され、第２列目と第３列目も互いに逆向きに形成される。第１列目と第２列目、第２列目と第３列目は互いに離間して配置されている。これは、後述するように他方のＬＥＤアレイの列が交互に挿入されるためである。第１列目の右端のＬＥＤ１と第２列目の右端のＬＥＤ１とはエアブリッジ配線２８により接続される。第２列目の左端のＬＥＤ１と第３列目の左端のＬＥＤ１もエアブリッジ配線２８で接続されてジグザグ配列となる。第１列目の左端のＬＥＤ１は基板１０の左上部に形成された電極（パッド）３２にエアブリッジ配線２８で接続され、第３列目の右端のＬＥＤ１は基板１０の右下部に形成された電極（パッド）３２にエアブリッジ配線２８で接続される。２つの電極（パッド）３２もＬＥＤ１と同形の正方形である。他方のＬＥＤアレイは上述した一方のＬＥＤアレイの間隙に互い違いとなるように形成される。すなわち、他方のＬＥＤアレイは上から７個、７個、６個とそれぞれ直線上に配置され、上から第１列目は一方のＬＥＤアレイの第１列目と第２列目の間に形成され、第２列目は一方のＬＥＤアレイの第２列目と第３列目の間に形成され、第３列目は一方のＬＥＤアレイの第３列目の下に形成される。他方のＬＥＤアレイの第１列目と第２列目、及び第２列目と第３列目も互いに逆方向となるように形成され、第１列目の右端のＬＥＤ１は第２列目の右端のＬＥＤ１にエアブリッジ配線２８で接続され、第２列目の左端のＬＥＤ１は第３列の左端のＬＥＤ１にエアブリッジ配線２８で接続されてジグザグ状となる。他方のＬＥＤアレイの第１列目の左端のＬＥＤは基板１０の左上部に形成された電極３２にエアブリッジ配線２８で接続され、第３列目の右端のＬＥＤ１は基板１０の右下部に形成された電極３２にエアブリッジ配線２８で接続される。一方のＬＥＤアレイと他方のＬＥＤアレイの電極３２に対する極性は互いに逆である。発光装置（チップ）の全体形状は長方形である。電源が供給される２つの電極３２は、長方形の対角位置に離間して形成される点も着目されたい。

図７には、図６の回路図が示されている。それぞれのＬＥＤアレイはジグザグ状に屈曲しつつ直列接続され、２つのＬＥＤアレイはジグザグ状の各列が互いの列の間に形成される様子が明らかとなろう。このような配置とすることで、多数

のＬＥＤ１を小さな基板１０上に配置することができる。また、４０個のＬＥＤ１に対して電極３２が２個でよいので、この点でも基板１０の使用効率を向上させることができる。また、各ＬＥＤ１を分離するためにＬＥＤ１を個別に形成する場合にはウエハをカットして分離する必要があるのに対し、本実施形態では各ＬＥＤ１の分離をエッチングで行うことができるので、ＬＥＤ１の間隔を狭くすることができる。これにより、サファイア基板１０の大きさをより小さくすることができる。ＬＥＤ１同士の分離は、フォトレジストや反応性イオンエッチング、ウエットエッチングを併用することでＬＥＤ１以外の領域を基板１０に達するまでエッチング除去することで達成される。各ＬＥＤアレイは交互に発光するので、発光効率を向上できるとともに放熱特性も向上させることができる。また、直列接続させるＬＥＤ１の数を変更すれば、全体としての駆動電圧も変更できる。また、ＬＥＤ１の面積を小さくすると、１つのＬＥＤ当たりの駆動電圧を高くすることもできる。ＬＥＤ１を２０個直列に接続した場合、商用電源（１００Ｖ、６０Ｈｚ）で駆動すると、およそ１５０mWの発光出力を得ることができる。この場合の駆動電流としては２０ｍＡ程度である。

なお、図７から分かるように、２つのＬＥＤアレイをジグザグ状に交互に配列する場合、エアブリッジ配線２８に交叉部分３４が必然的に発生する。例えば、他方のＬＥＤアレイの第１列目と第２列目を接続する際に、一方のＬＥＤアレイの第１列目と第２列目を接続するための配線部分と交叉する。しかし、本実施形態のエアブリッジ配線２８は、上述したように基板１０に接着しておらず、基板１０から離れて空中を通過するので、交叉部分３４においてエアブリッジ配線２８同士が接触し、短絡することを容易に回避することができる。エアブリッジ配線２８を用いる利点の一つである。エアブリッジ配線２８は、例えば以下のようにして形成される。すなわち、全面に２μmの厚さのフォトレジストを塗布し、エアブリッジ配線の形状に穴を開けた後にポストベークする。その上に、真空蒸着でＴｉを１０ｎｍ、Ａｕを１０ｎｍ、この順序で蒸着する。さらにその上の全面に２μm厚さでフォトレジストを再度塗布し、エアブリッジ配線を形成する部分のみに穴を開ける。次いで、ＴｉとＡｕを電極として電解液中でイオンプレーティング（メッキ）により電極全面に３～５μmの厚さのＡｕを付着させる。そ

の後、試料をアセトンに浸し、超音波洗浄によりフォトレジストを溶解除去してエアブリッジ配線２８が完成する。

このように、複数のＬＥＤ１を二次元アレイ状に配置することで、基板面積を有効に活用しつつ高駆動電圧、特に商用電源での駆動も可能となるが、二次元アレイのパターンとしてはこの他にも種々のパターンが可能である。一般に、二次元アレイパターンとしては、以下の条件を備えることが望ましい。

（１）各ＬＥＤに均一に電流を流し、均一な発光を得るためには各ＬＥＤの形状、電極位置が同一であることが望ましい。

（２）ウエハをカットしてチップにするためには、各ＬＥＤの辺は直線であることが望ましい。

（３）光取り出し効率を向上させるため、標準的なマウントを使用して周辺からの反射を利用するためにはＬＥＤは平面形状が正方形に近い形状が望ましい。

（４）２つの電極（ボンディングパット）の大きさは１００μｍ角程度で、互いに離れていることが望ましい。

（５）ウエハ面積の有効利用のため、配線、パッドの占める割合は小さい方が望ましい。

もちろん、これらは必須ではなく、例えば各ＬＥＤの形状としては平面形状三角形を用いることも可能であろう。各ＬＥＤの形状が三角形であっても、これらを組み合わせることで全体形状を略正方形とすることができる。以下、二次元アレイパターンの例をいくつか示す。

図８には、合計６個のＬＥＤ１を二次元に配置した例が示されており、図９にはその回路図が示されている。図８の配置は、基本的には図６の配置と同様であり、合計６個のＬＥＤアレイは同数ずつ２組に分けられ、それぞれ直列接続された３個のＬＥＤから構成される。一方のＬＥＤアレイはジグザグ状に配列され、上から第１列目は１個のＬＥＤ１、第２列目は２個のＬＥＤ１が形成される。第１列目のＬＥＤと第２列目の右端のＬＥＤ１はエアブリッジ配線２８で直列接続され、第２列目の２個のＬＥＤ１もエアブリッジ配線２８で直列接続される。基板１０の左上部と左下部に電極（パッド）３２が形成され、第１列目のＬＥＤ１は左上部の電極３２にエアブリッジ配線で接続され、第２列目の左端のＬＥＤ１

は左下部の電極３２に接続される。他方のＬＥＤアレイもジグザグ状に配列され、上から第１列目は２個のＬＥＤ１、第２列目は１個のＬＥＤ１が形成される。他方のＬＥＤアレイの第１列目は前記一方のＬＥＤアレイの第１列目と第２列目の間に形成され、他方のＬＥＤアレイの第２列目は前記一方のＬＥＤアレイの第２列目の下方に形成される。第１列目の右端のＬＥＤ１は第２列目のＬＥＤ１にエアブリッジ配線２８で直列接続され、第１列目の２個のＬＥＤ１同士もエアブリッジ配線２８で直列接続される。第１列目の左端のＬＥＤ１は左上部の電極３２にエアブリッジ配線２８で接続され、第２列目のＬＥＤ１は左下部の電極３２にエアブリッジ配線２８で接続される。図９から分かるように、この例でも２つのＬＥＤアレイは互いに並列に電極３２に接続され、かつ、互いに逆極性となるように接続される。したがって、交流電源を供給した場合、２つのＬＥＤアレイは交互に発光することになる。

図１０には、合計１４個のＬＥＤを二次元配置した例が示されており、図１１にはその回路図が示されている。合計１４個のＬＥＤアレイは２組に分けられ、それぞれ直列接続された７個のＬＥＤから構成される。一方のＬＥＤアレイはジグザグ状に配列され、上から第１列目は３個のＬＥＤ１、第２列目は４個のＬＥＤ１が形成される。第１列目の左端のＬＥＤと第２列目の左端のＬＥＤ１はエアブリッジ配線２８で直列接続され、第１列目の３個のＬＥＤ同士、及び第２列目の４個のＬＥＤ１同士もエアブリッジ配線２８で直列接続される。基板１０の右上部と右下部に電極（パッド）３２が形成され、第１列目の右端のＬＥＤ１は右上部の電極３２にエアブリッジ配線で接続され、第２列目の右端のＬＥＤ１は右下部の電極３２に接続される。他方のＬＥＤアレイもジグザグ状に配列され、上から第１列目は４個のＬＥＤ１、第２列目は３個のＬＥＤ１が形成される。他方のＬＥＤアレイの第１列目は前記一方のＬＥＤアレイの第１列目と第２列目の間に形成され、他方のＬＥＤアレイの第２列目は前記一方のＬＥＤアレイの第２列目の下方に形成される。第１列目の左端のＬＥＤ１は第２列目の左端のＬＥＤ１にエアブリッジ配線２８で直列接続される。第１列目の４個のＬＥＤ１同士、及び第２列目の３個のＬＥＤ１同士も直列接続される。第１列目の右端のＬＥＤ１は右上部の電極３２にエアブリッジ配線２８で接続され、第２列目の右端のＬＥ

Ｄ１は右下部の電極３２にエアブリッジ配線２８で接続される。図１１から分かるように、この例でも２つのＬＥＤアレイは互いに並列に電極３２に接続され、かつ、互いに逆極性となるように接続される。したがって、交流電源を供給した場合、２つのＬＥＤアレイは交互に発光することになる。

図６、図８、図１０の二次元パターンに共通する特徴としては、各ＬＥＤ１が略正方形の同形、同サイズであること、２つの電極（パッド）も略正方形であり、隣接形成されていない（離間形成されている）こと、２つのＬＥＤアレイの組み合わせであること、２つのＬＥＤアレイは屈曲しつつチップ上に互いに交錯するように形成されること、２つのＬＥＤアレイは互いに逆極性となるように電極に接続されること、等である。

図１２には、平面形状が三角形のＬＥＤを二次元配列した場合の例が示されており、図１３にはその回路図が示されている。図１２において、合計６個のＬＥＤ１ａ、１ｂ、１ｃ、１ｄ、１ｅ、１ｆがその平面形状が三角形状となるように形成されている。ＬＥＤ１ａとＬＥＤ１ｅが三角形の一辺で対向して２つで略正方形となるように配置され、ＬＥＤ１ｂと１ｆが対向して２つで略正方形となるように配置される。また、ＬＥＤ１ｄと電極３２が対向して接続し、ＬＥＤ１ｃと電極３２が対向して接続する。２つの電極３２もＬＥＤと同様に平面形状が三角形状であり、同様に略正方形となるように配置される。ＬＥＤ同士の対向する辺はｎ電極２４を構成し、すなわち、対向する２つのＬＥＤはｎ電極２４を共有する。ＬＥＤと電極３２もｎ電極接続である。この配置も、上述した例と同様に合計６個のＬＥＤは２組に分けられる。一方のＬＥＤアレイは、ＬＥＤ１ａ、ＬＥＤ１ｂ、ＬＥＤ１ｃからなるアレイであり、ＬＥＤ１ａのｐ電極２２は電極３２にエアブリッジ配線２８で接続され、そのｎ電極２４はＬＥＤ１ｂのｐ電極２２とエアブリッジ配線２８で接続される。ＬＥＤ１ｂのｎ電極２４はＬＥＤ１ｃのｐ電極２２とエアブリッジ配線２８で接続される。ＬＥＤ１ｃのｎ電極２４は電極３２に接続される。他方のＬＥＤアレイは、ＬＥＤ１ｄ、ＬＥＤ１ｅ、ＬＥＤ１ｆから構成され、電極３２とＬＥＤ１ｆのｐ電極２２はエアブリッジ配線２８で接続され、ＬＥＤ１ｆのｎ電極２４はＬＥＤ１ｅのｐ電極２２とエアブリッジ配線２８で接続され、ＬＥＤ１ｅのｎ電極２４とＬＥＤ１ｄのｐ電極２２はエ

アブリッジ配線２８で接続され、ＬＥＤ１ｄのｎ電極２４は電極３２に接続される。

図１３において、一方のＬＥＤアレイを構成するＬＥＤ１ａと他方のＬＥＤアレイを構成するＬＥＤ１ｅのｎ電極が接続されており、一方のＬＥＤアレイを構成するＬＥＤ１ｂと他方のＬＥＤアレイを構成するＬＥＤ１ｆのｎ電極が接続されている点にも着目されたい。２組のＬＥＤアレイのいくつかのｎ電極を共有することで、回路配線を削減することができる。また、この例においても、２つのＬＥＤアレイは並列に電極３２に接続され、かつ、互いに逆極性となるように接続される。また、各ＬＥＤは同形、同サイズであり、各ＬＥＤを一つの辺で対向させるとともに電極３２も三角形状とすることでＬＥＤ及び電極を高密度に形成して必要な基板面積を小さくすることができる。

図１４には、平面形状が三角形のＬＥＤを二次元配列した他の例が示されており、図１５にはその回路図が示されている。この例では、合計１６個のＬＥＤ１ａ～１ｒが二次元形成されている。ＬＥＤ１ａと１ｊ、１ｂと１ｋ、１ｃと１ｍ、１ｄと１ｎ、１ｅと１ｐ、１ｆと１ｑ、１ｇと１ｒがそれぞれ三角形の一つの辺で対向する。対向する辺にはｎ電極２４が共通形成されている。また、ＬＥＤ１ｉと電極３２が対向し、ＬＥＤ１ｈと電極３２が対向する。一方のＬＥＤアレイはＬＥＤ１ａ、１ｂ、１ｃ、１ｄ、１ｅ、１ｆ、１ｇ、１ｈから構成され、他方のＬＥＤアレイはＬＥＤ１ｒ、１ｑ、１ｐ、１ｎ、１ｍ、１ｋ、１ｊ、１ｉから構成される。ＬＥＤ１ｂのｎ電極２４はエアブリッジ配線２８によりＬＥＤ１ｃのｐ電極２２に接続され、ＬＥＤ１ｅのｎ電極２４もエアブリッジ配線２８によりＬＥＤ１ｆのｐ電極２２に接続される。また、ＬＥＤ１ｑのｎ電極２４もエアブリッジ配線２８によりＬＥＤ１ｐのｐ電極２２に接続され、ＬＥＤ１ｍのｎ電極２４もエアブリッジ配線２８によりＬＥＤ１ｋのｐ電極２２に接続される。図１４においても、図１２と同様に交叉部分が生じるが、エアブリッジ配線２８により短絡を回避できる。また、この例においても２組のＬＥＤアレイのいくつかのｎ電極２４を共有構造とすることで必要な配線を削減している。また、この例においても２つのＬＥＤアレイは並列で互いに逆極性で電極３２に接続されており、交流駆動が可能である。図１２においては合計６個のＬＥＤの場合、図１４

においては合計１６個のＬＥＤの場合について示したが、他の個数のＬＥＤでも同様に二次元配列できる。本願出願人は、３８個のＬＥＤを二次元配列した発光装置も作成している。

以上、交流駆動の場合について説明したが、直流駆動も可能であることは言うまでもない。この場合、ＬＥＤアレイを互いに逆極性となるように電極に接続するのではなく、直流電源の極性の向きに合わせてＬＥＤアレイを順方向に接続すればよい。複数のＬＥＤを直列接続することで、高電圧駆動が可能である。以下、直流駆動の場合についても説明する。

図１６には、２個のＬＥＤを直列接続した例が示されており、図１７にはその回路図が示されている。各ＬＥＤ１は平面形状が矩形状であり、２個のＬＥＤ間はエアブリッジ配線２８で接続される。電極３２は各ＬＥＤ１の近傍に形成されており、電極３２とＬＥＤ１とで長方形の領域を形成する。すなわち、電極３２は長方形領域の一部を占有し、長方形領域の他の領域にＬＥＤ１が形成されている。

図１８には、合計４個のＬＥＤを二次元配列した例が示されており、図１９にはその回路図が示されている。図１６のＬＥＤ１を２個に分割し、それぞれを並列に接続したものである。２個のＬＥＤからなるＬＥＤアレイを２組並列に順方向接続したと云うこともできる。ＬＥＤ１ａと１ｂで一つのＬＥＤアレイを構成し、ＬＥＤ１ｃと１ｄでもう一つのＬＥＤアレイを構成する。ＬＥＤ１ａとＬＥＤ１ｃはｐ電極２２及びｎ電極２４を共有し、ＬＥＤ１ｂとＬＥＤ１ｄもｐ電極２２及びｎ電極２４を共有する。この構成によれば、図１６に比べて電流が均一化する効果がある。

図２０は、合計３個のＬＥＤを二次元配列した例が示されており、図２１にはその回路図が示されている。ＬＥＤ１ａ、１ｂ、１ｃは同形ではなく、ＬＥＤ１ａの一部に電極３２が形成されている。ＬＥＤ１ａのｎ電極２４とＬＥＤ１ｂのｐ電極はＬＥＤ１ｂの上を跨ぐエアブリッジ配線２８で接続される。各ＬＥＤの形状及び配置を工夫することで、３個のＬＥＤであっても発光装置（チップ）全体の外観形状を略正方形とすることができる。

図２２には、合計６個のＬＥＤを二次元配列した例が示されており、図２３に

はその回路図が示されている。各ＬＥＤ１ａ～１ｆは同形、同サイズである。ＬＥＤ１ａ～１ｆは直列接続される。ＬＥＤ１ａ～１ｃは直線上に配置され、ＬＥＤ１ｄ～１ｆは他の直線上に配置される。ＬＥＤ１ｃとＬＥＤ１ｄはエアブリッジ配線２８で接続される。この例においても、チップの全体形状を略正方形とすることができる。

図２４には、合計５個のＬＥＤを二次元配列した例が示されており、図２５にはその回路図が示されている。ＬＥＤ１ａ～１ｅは同形（長方形）、同サイズである。この例においても、全体形状を略正方形とすることができる。

以上、本発明の実施形態について説明したが、本発明はこれに限定されるものではなく種々の変更が可能である。特に、複数の発光素子（ＬＥＤ等）を二次元配置する場合のパターンは上述したパターン以外にも可能である。この場合、隣接する発光素子間で電極を共有して配線を少なくすること、全体形状を正方形あるいは長方形とすること、複数組の発光素子アレイを電極に並列接続すること、交流駆動の場合に複数組の発光素子アレイを互い逆極性とすること、複数組の発光素子アレイをそれぞれジグザグ状に屈曲させて組み合わせること、等が好適である。

図２６～図３１には、これらの変更例のいくつかが例示されている。図２６は交流駆動の場合の二次元配置であり、合計４０個のＬＥＤが配置されている。図２７はその回路図である。図６と異なる点は、２組のＬＥＤアレイのいくつかがｎ電極２４を共有する点である（図５参照）。例えば、一方のＬＥＤアレイの第１列の右端から２番目に位置するＬＥＤ（図中αで示す）のｎ電極２４は、他方のＬＥＤアレイの第１列の右端に位置するＬＥＤ（図中βで示す）のｎ電極２４と共有されている。なお、ＬＥＤアレイの端部（図中γ部分）におけるエアブリッジ配線２８は、交叉させることなく共通形成されている。

図２８は、交流駆動の場合の二次元配置であり、合計１４個のＬＥＤが配置されている。図２９はその回路図である。図１０と異なる点は、２組のＬＥＤアレイのいくつかがｎ電極２４を共有する点である。例えば、一方のＬＥＤアレイの第１列の左端のＬＥＤ（図中αで示す）のｎ電極２４は、他方のＬＥＤアレイの第１列の右端から２番目に位置するＬＥＤ（図中βで示す）のｎ電極２４と共有

されている。また、端部（図中γ部分）におけるエアブリッジ配線２８は共通形成されている。

図３０は、交流駆動の場合の二次元配置であり、合計６個のＬＥＤが配置されている。図３１はその回路図である。この例においても、端部（γ部）のエアブリッジ配線２８が共通形成されている。この構成も、一方のＬＥＤアレイにおけるｎ電極２４と他方のＬＥＤアレイにおけるｎ電極２４が共有されていると云うことができる。

請 求 の 範 囲

１．絶縁基板上に複数のＧａＮ系発光素子が形成され、前記複数の発光素子がモノリシックに直列接続されることを特徴とする発光装置。

２．請求項１記載の装置において、
前記複数の発光素子は、前記基板上に二次元配置されていることを特徴とする発光装置。

３．請求項１記載の装置において、
前記複数の発光素子は２組に分けられ、２個の電極に互いに反対極性となるように並列接続されることを特徴とする発光装置。

４．請求項１記載の装置において、
前記複数の発光素子間の接続はエアブリッジ配線であることを特徴とする発光装置。

５．請求項１記載の装置において、
前記複数の発光素子間の電気的な分離は、前記基板として使用されるサファイアにより行われることを特徴とする発光装置。

６．請求項２記載の装置において、
前記複数の発光素子は同数ずつ２組に分けられ、各組の発光素子アレイはジグザグ状に配置され、かつ、２組の発光素子アレイは２個の電極に互いに反対極性となるように並列接続されることを特徴とする発光装置。

７．請求項６記載の装置において、
前記２組の発光素子アレイは、互い違いに配置されることを特徴とする発光装置。

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８．請求項６記載の装置において、

前記発光素子及び電極は、平面形状が略正方形であることを特徴とする発光装置。

９．請求項６記載の装置において、

前記発光素子及び電極は、平面形状が三角形状であることを特徴とする発光装置。

１０．請求項２記載の装置において、

前記複数の発光素子及び電極は、全体形状が略正方形となるように配置されることを特徴とする発光装置。

１１．請求項１０記載の装置において、

前記複数の発光素子からなる発光素子アレイはジグザグ状に配置されることを特徴とする発光装置。

１２．請求項６記載の装置において、

前記電極は、交流電源用電極であることを特徴とする発光装置。

１３．請求項６記載の装置において、

前記２組の発光素子アレイは、共通のｎ電極を有することを特徴とする発光装置。

図1

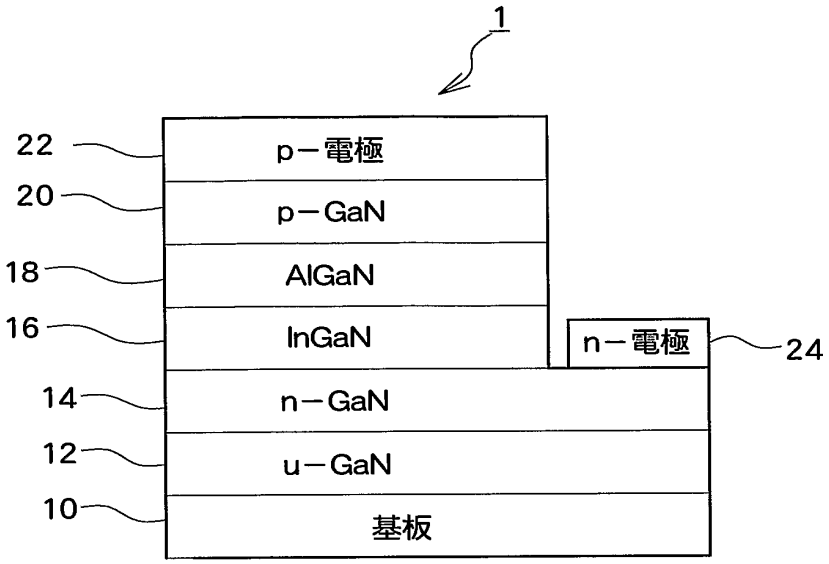

1
22
p－電極
20
p－GaN
18
AlGaN
16
InGaN
n－電極
24
14
n－GaN
12
u－GaN
10
基板

図2

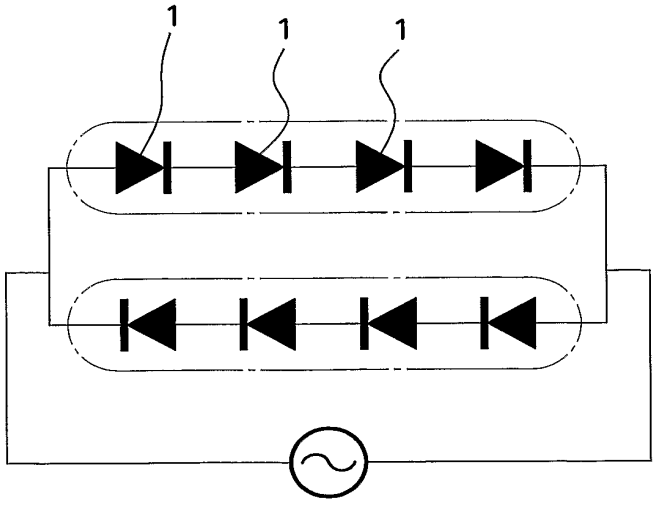

1
1
1

図 3

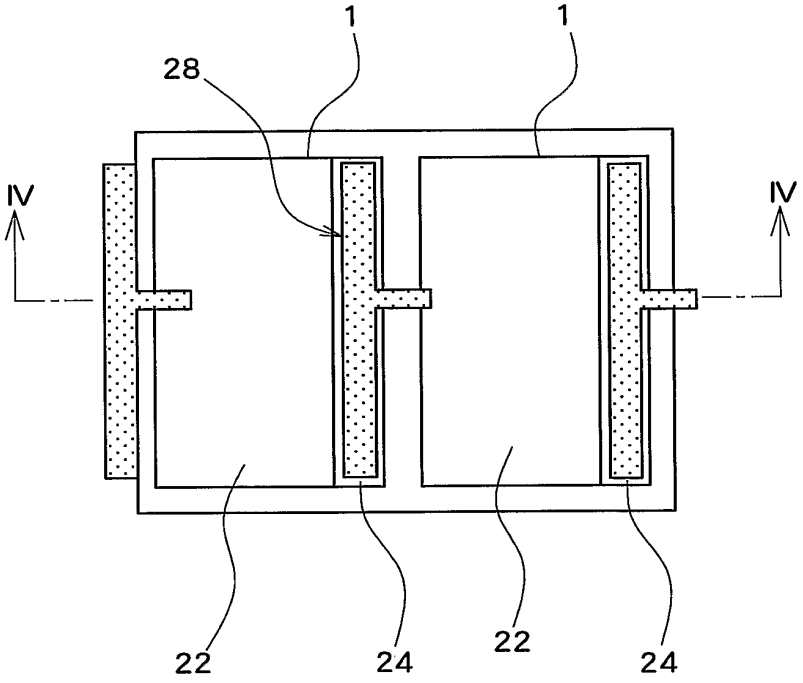


図 4

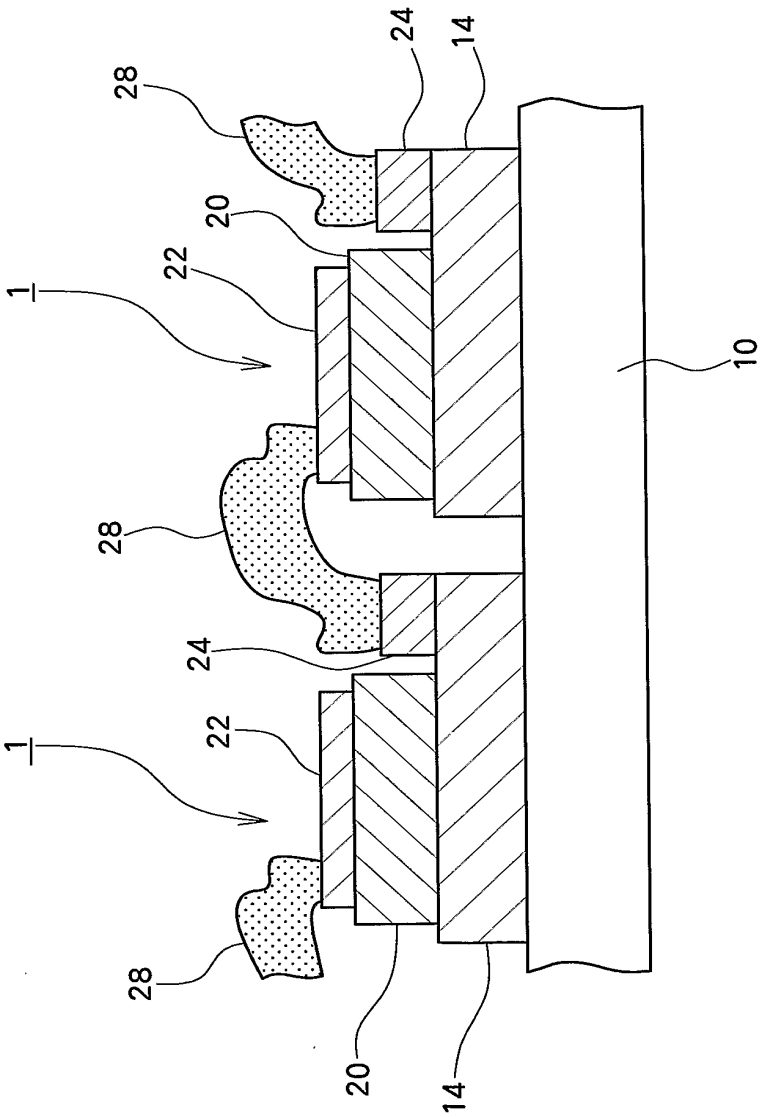


図 5

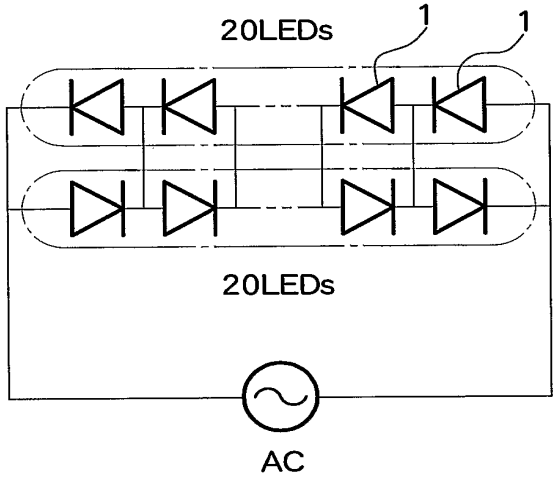


図 6

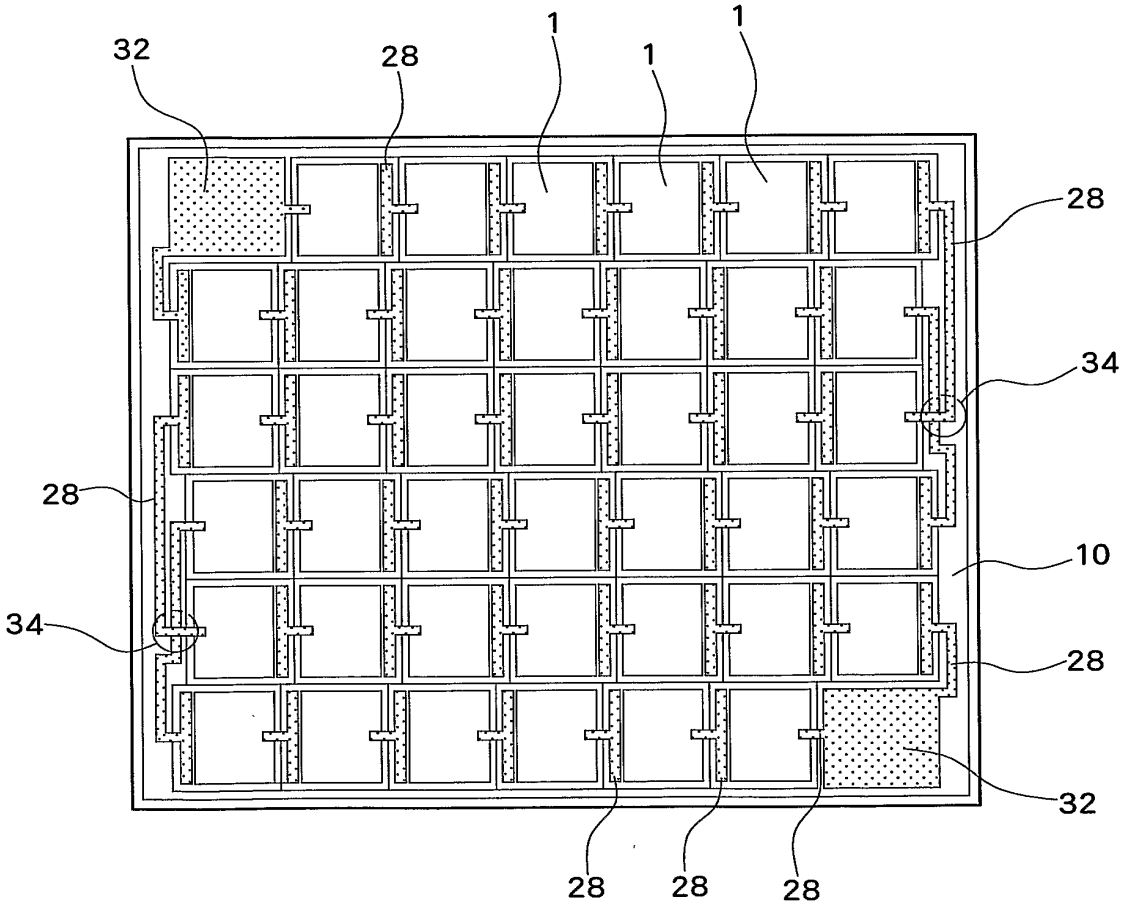


図 7

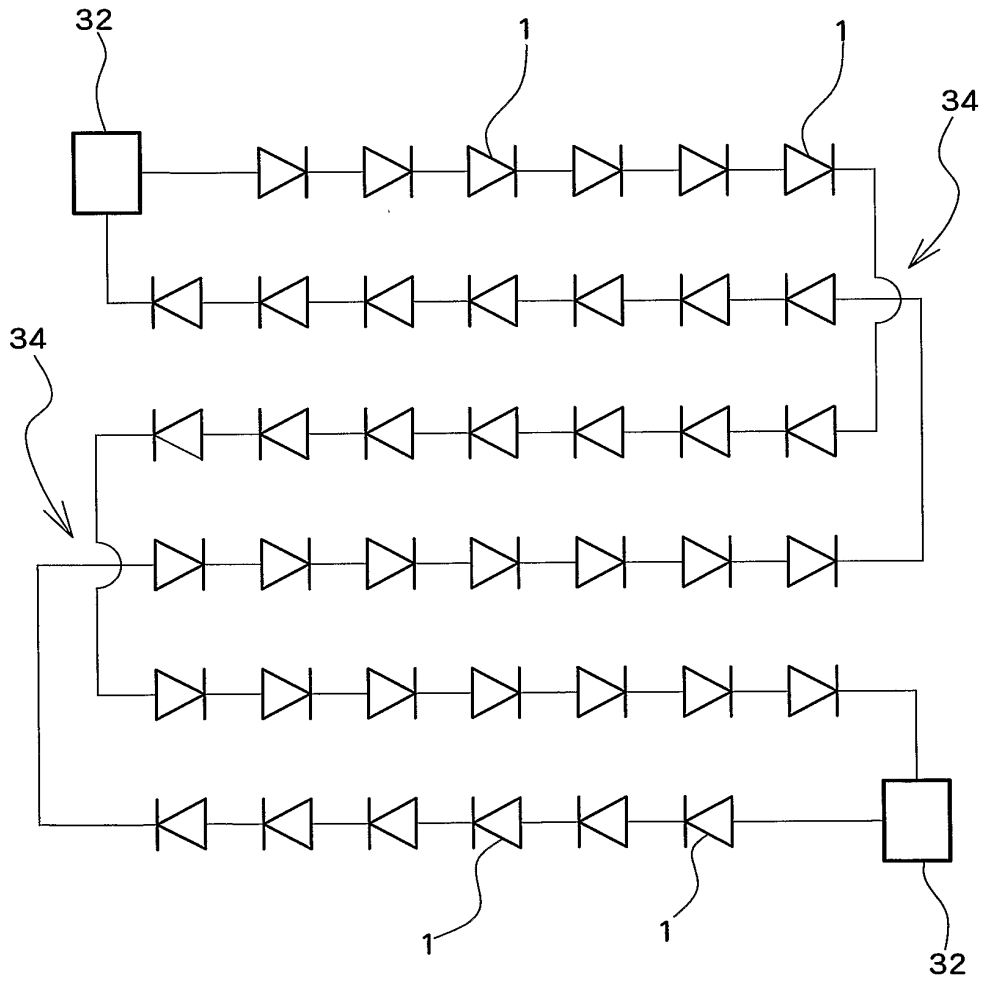


図 8

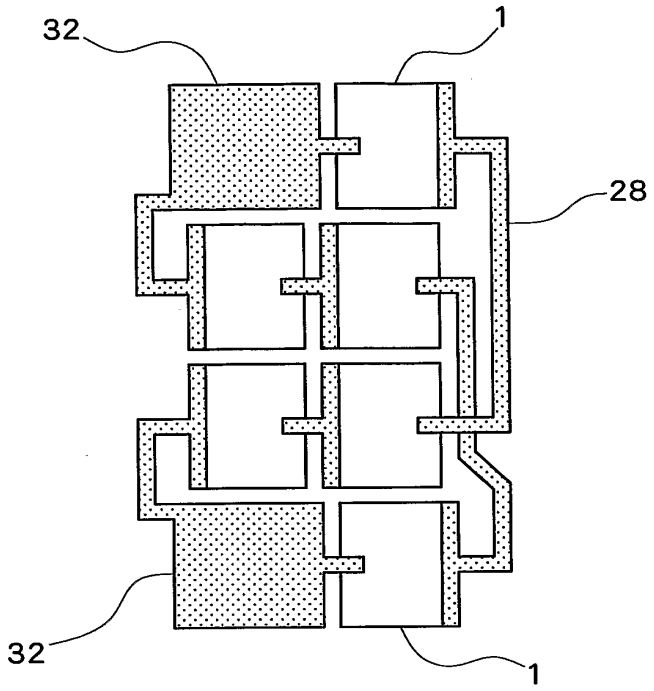


図 9

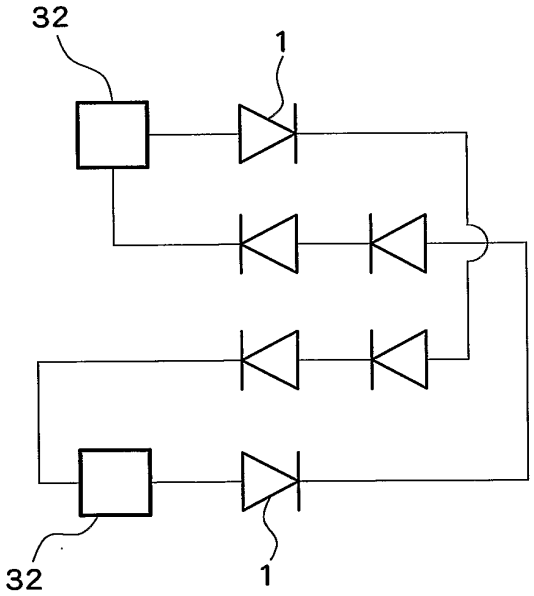


図 10

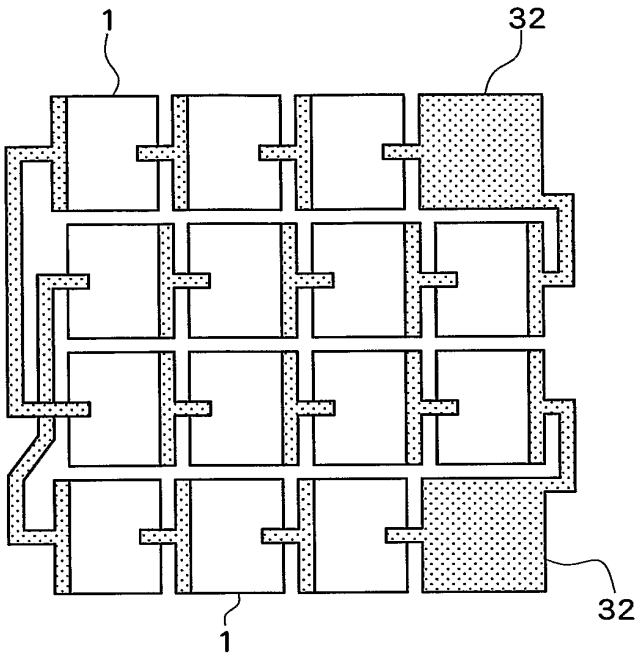


図 11

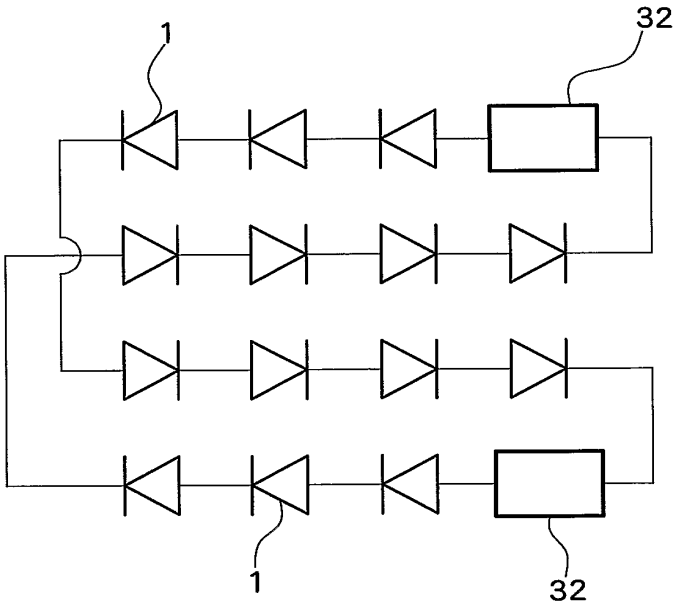


図 12

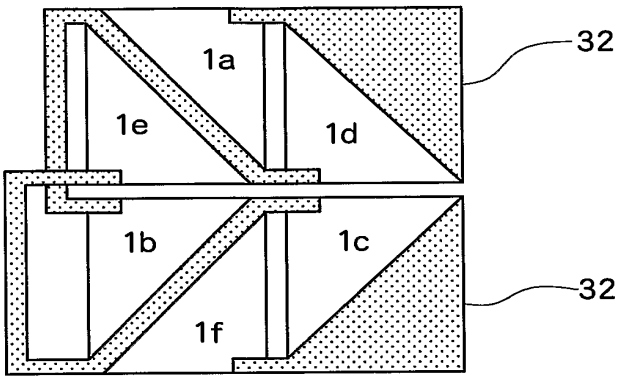


図 13

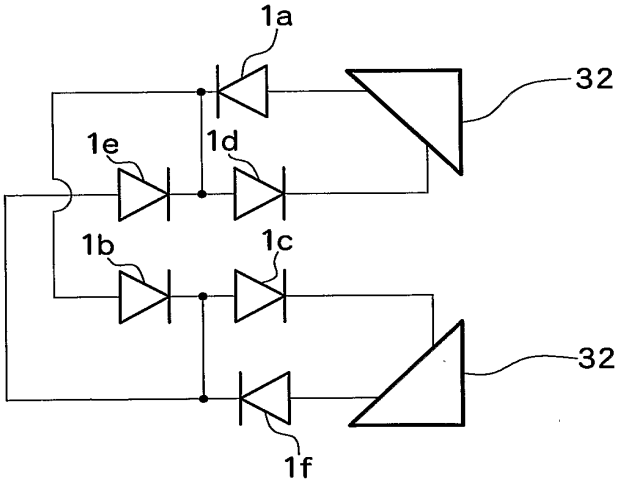


図 14

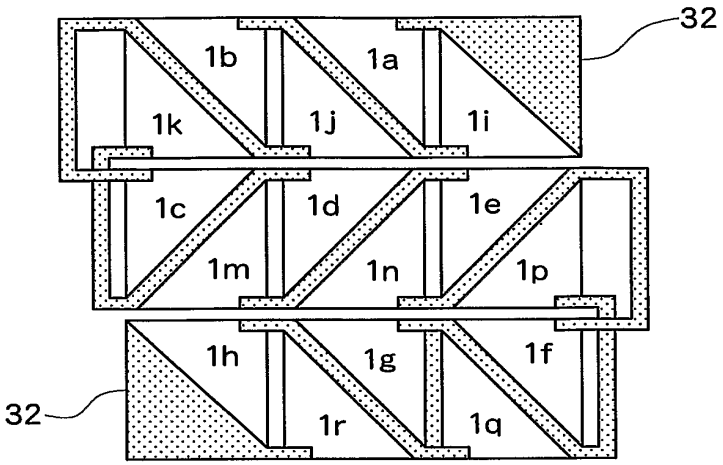

32
1b
1a
1k
1j
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1m
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1p
1h
1g
1f
32
1r
1q

図 15

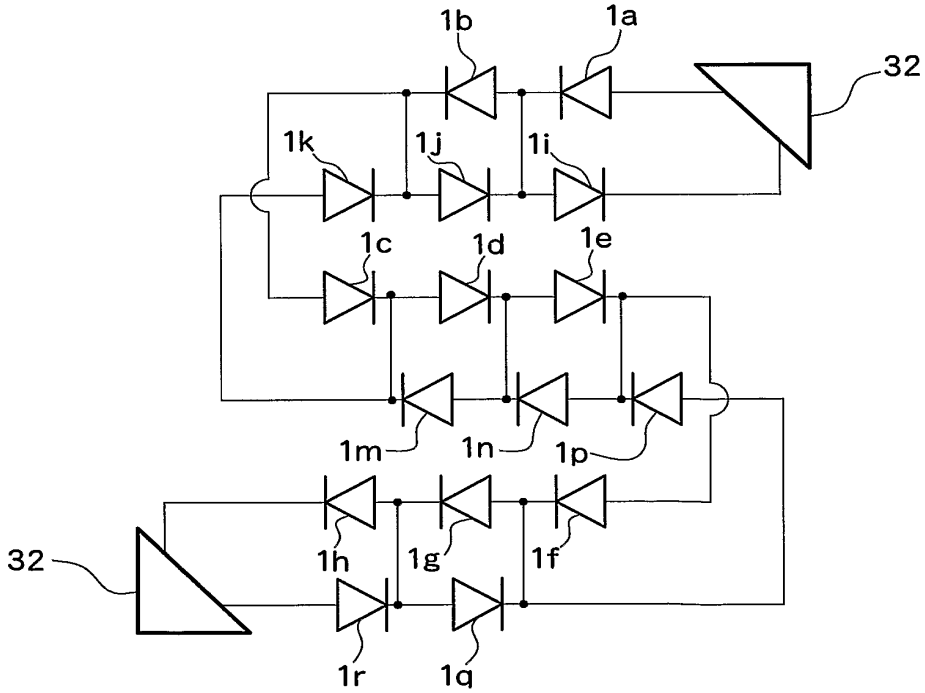

1b
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図 16

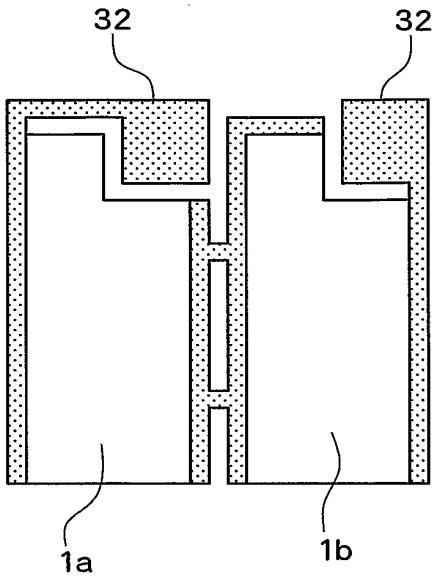


図 17

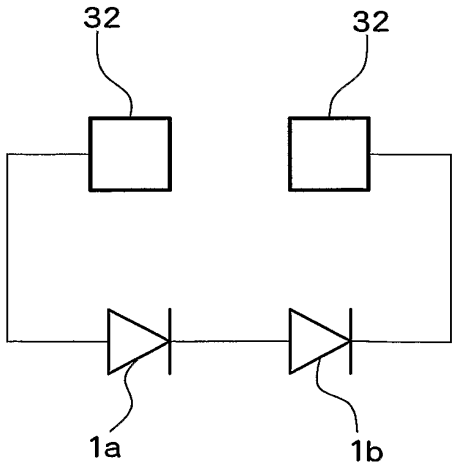


図 18

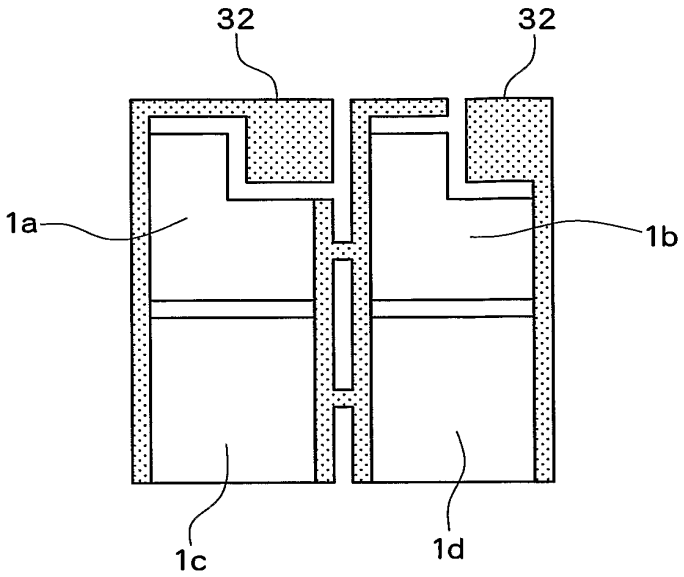


図 19

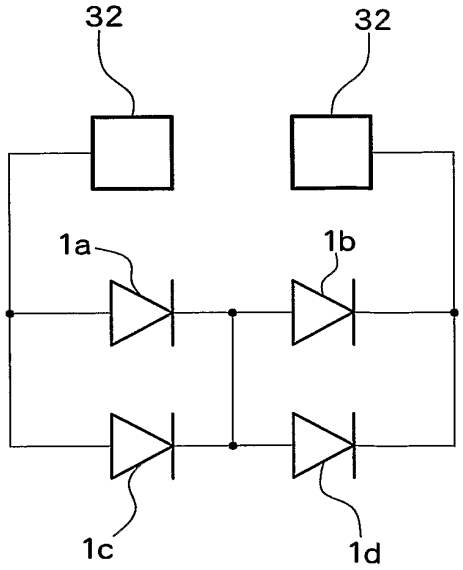


図 20

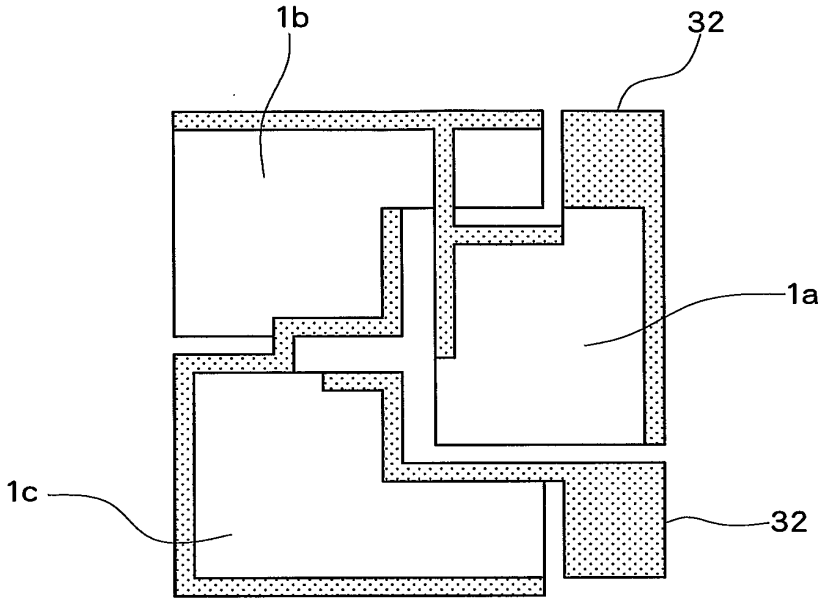


図 21

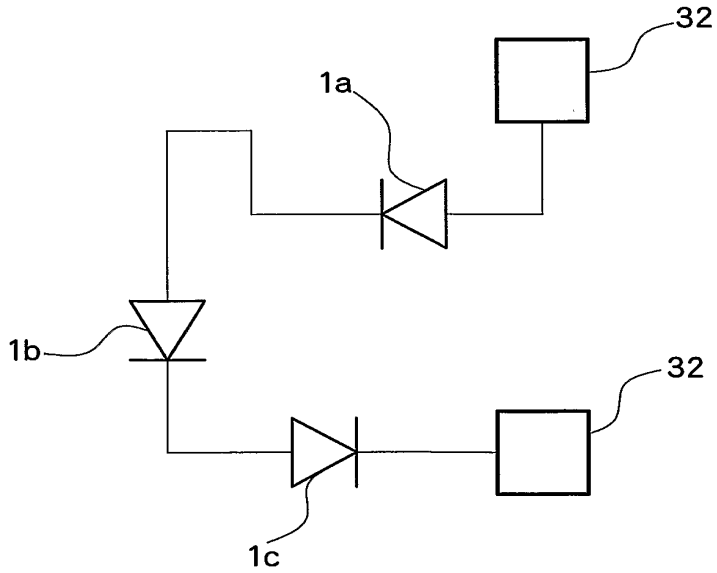


図 22

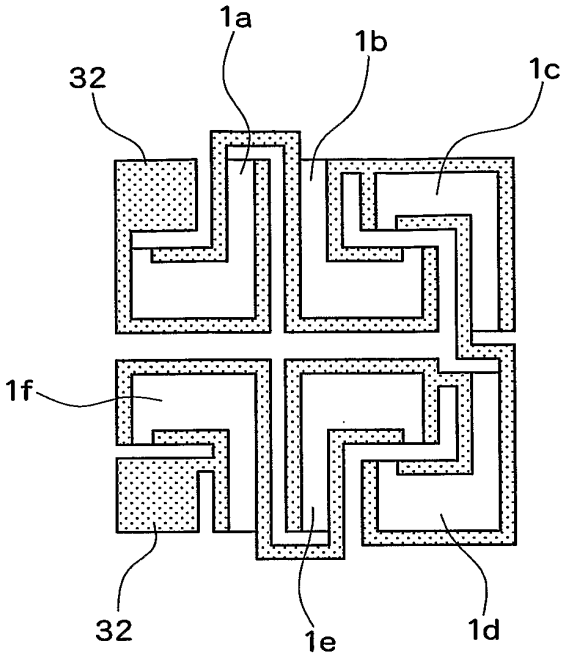


図 23

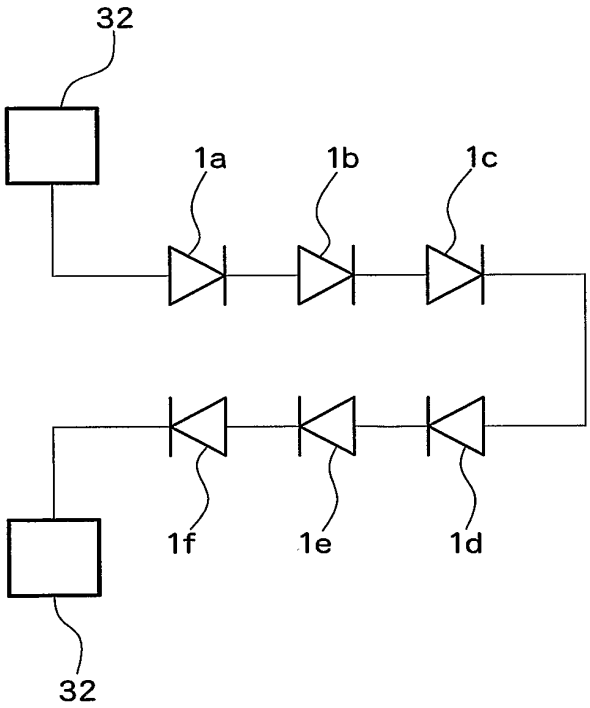


図 24

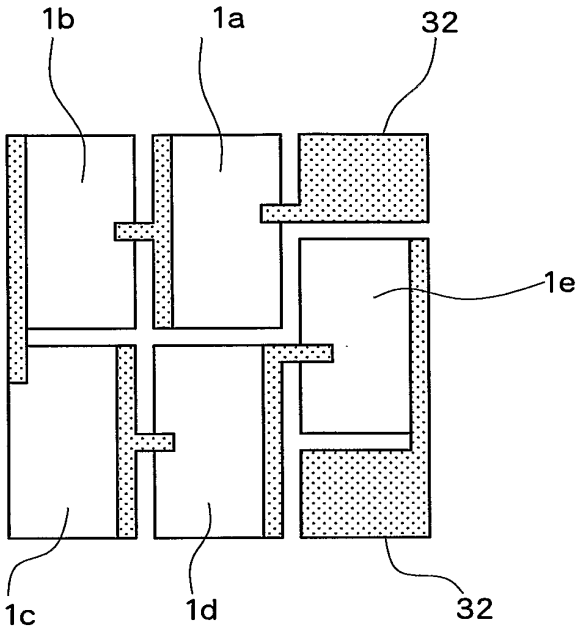


図 25

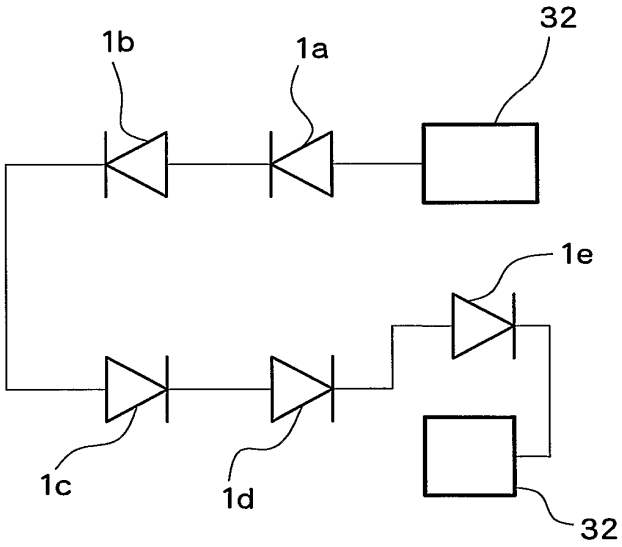


図 26

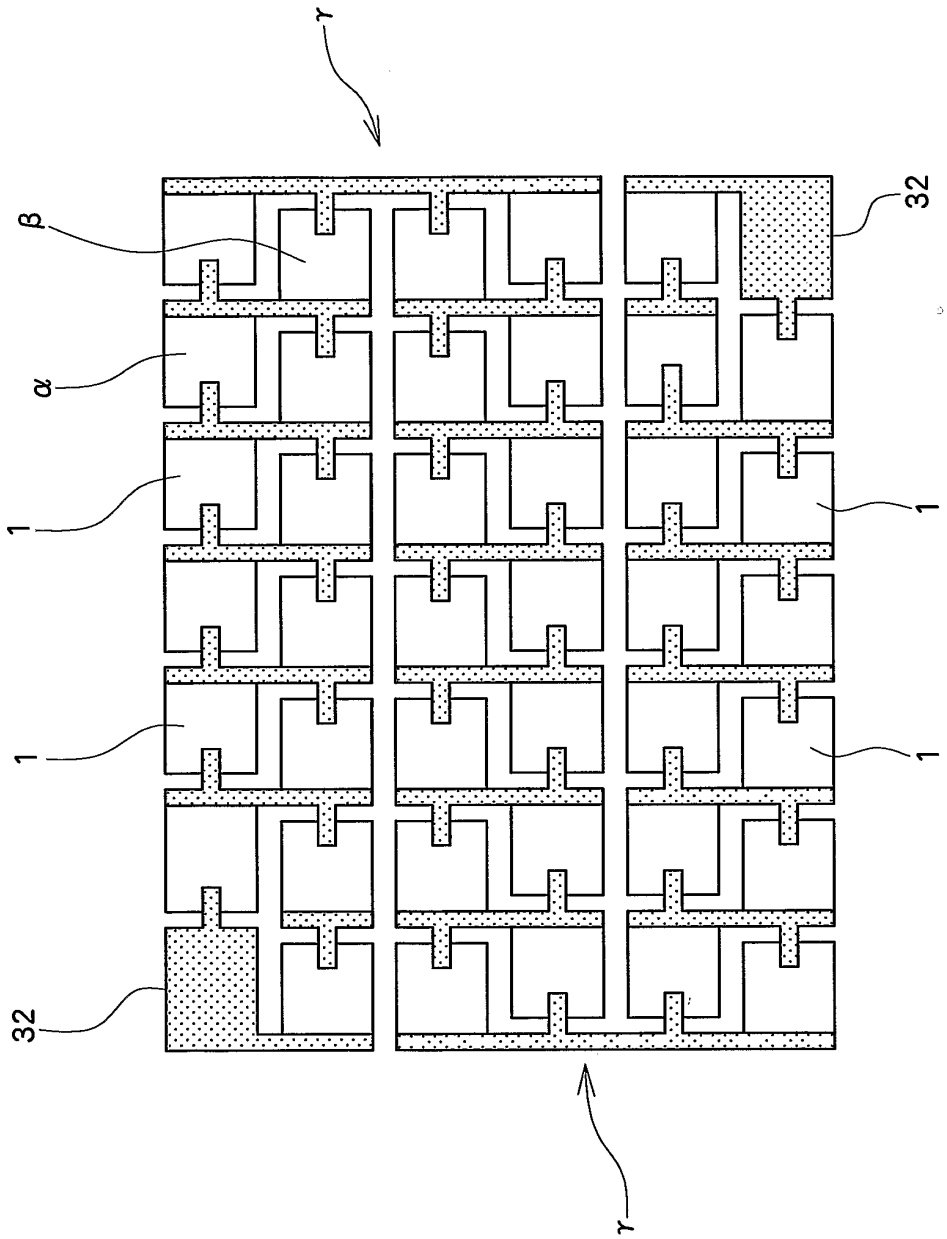


図 27

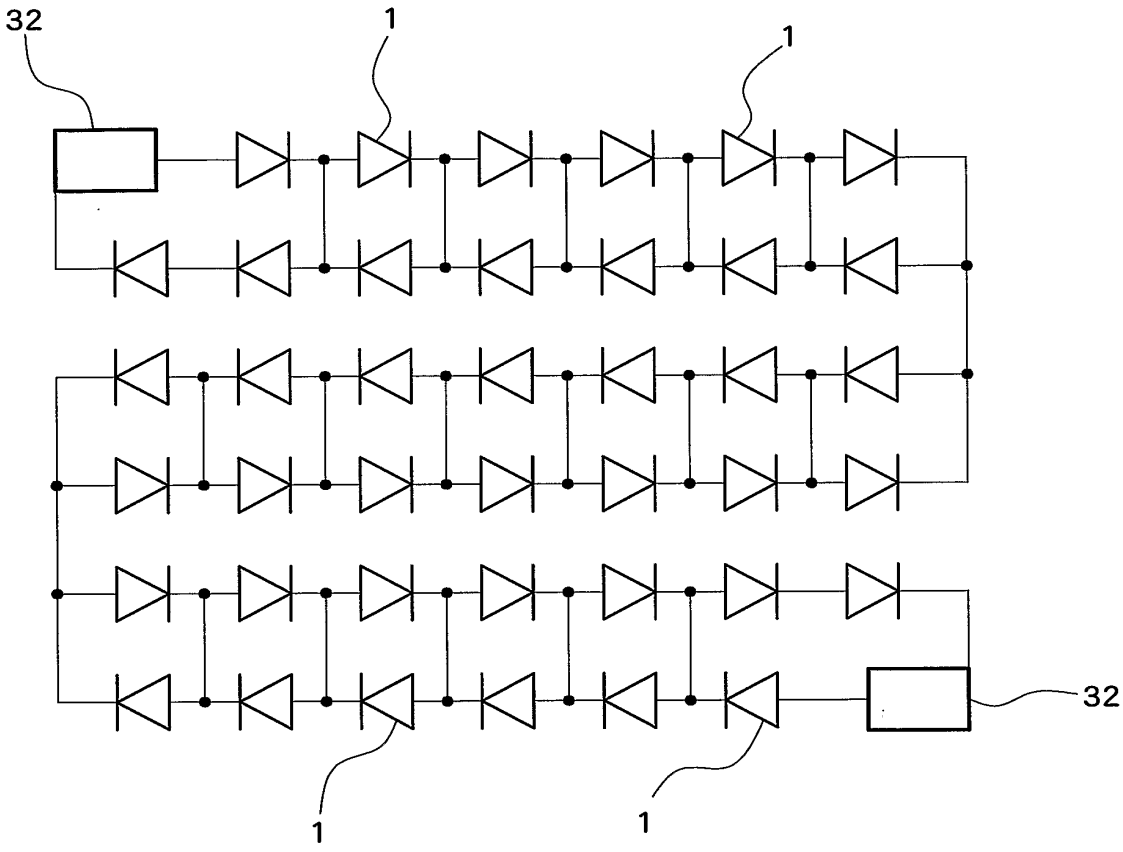


図 28

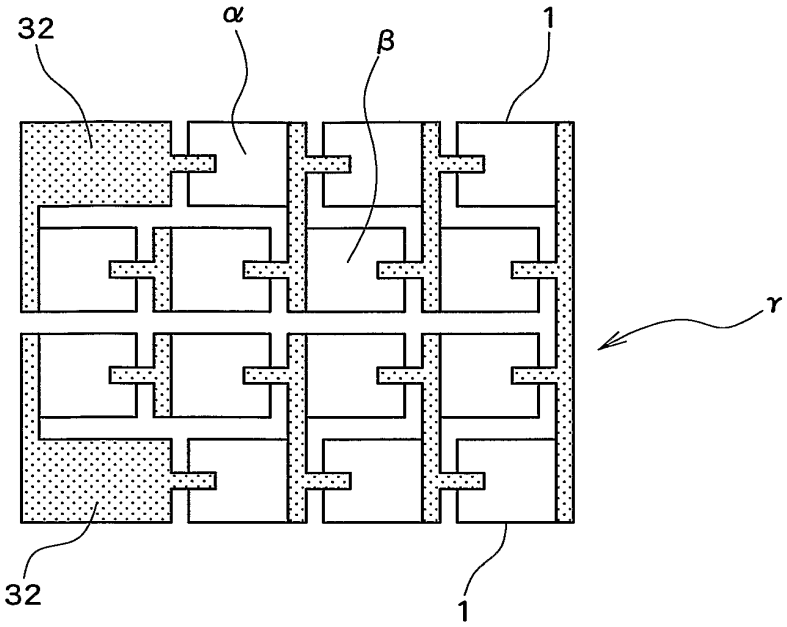


図 29

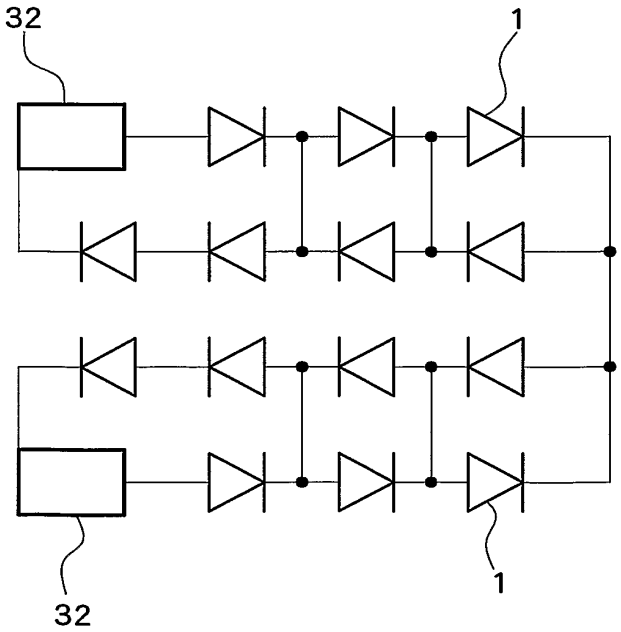


図 30

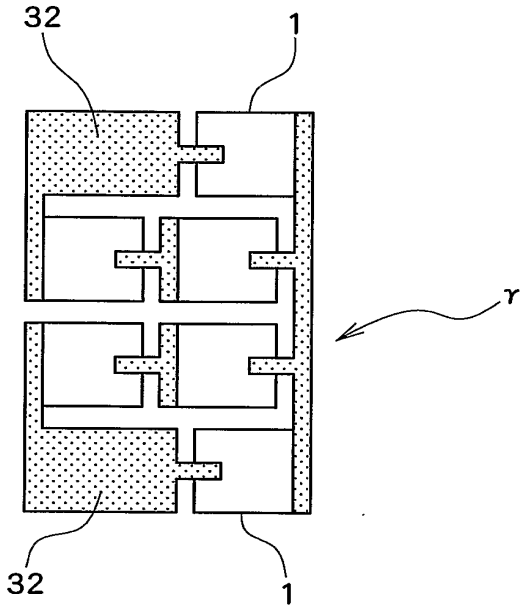
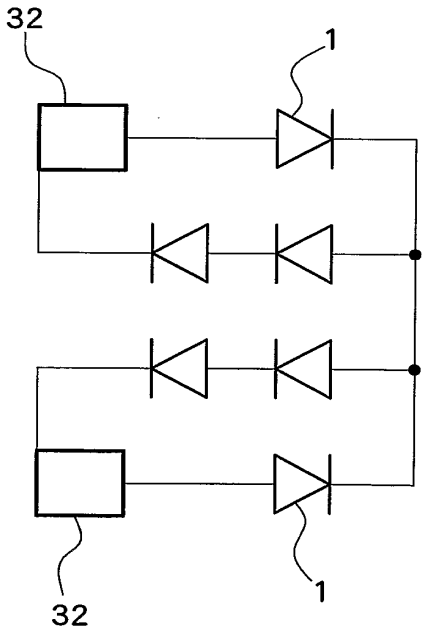


図 31



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP03/10922

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H01L33/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H01L33/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1922-1996	Toroku Jitsuyo Shinan Koho	1994-2003
Kokai Jitsuyo Shinan Koho	1971-2003	Jitsuyo Shinan Toroku Koho	1996-2003

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2001-156331 A (Nichia Chemical Industries, Ltd.), 08 June, 2001 (08.06.01), Full text; all drawings (Family: none)	1-2,4-5,10
X	JP 2001-307506 A (Hitachi, Ltd.), 02 November, 2001 (02.11.01), Full text; all drawings (Family: none)	1-3,5,10
X	JP 2000-068555 A (Hitachi, Ltd.), 03 March, 2000 (03.03.00), Full text; all drawings (Family: none)	1,2,5,10

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search 18 September, 2003 (18.09.03)	Date of mailing of the international search report 07 October, 2003 (07.10.03)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP03/10922

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2001-351789 A (Toshiba Lighting & Technology Corp.), 21 December, 2001 (21.12.01), Full text; all drawings (Family: none)	6
A	JP 59-206873 A (Toshiba Corp.), 22 November, 1984 (22.11.84), Full text; all drawings (Family: none)	6

Form PCT/ISA/210 (continuation of second sheet) (July 1998)

国際調査報告

国際出願番号　ＰＣＴ／ＪＰ０３／１０９２２

A.　発明の属する分野の分類（国際特許分類（ＩＰＣ））

Ｉｎｔ．Ｃｌ⁷　Ｈ０１Ｌ３３／００

B.　調査を行った分野

調査を行った最小限資料（国際特許分類（ＩＰＣ））

Ｉｎｔ．Ｃｌ⁷　Ｈ０１Ｌ３３／００

最小限資料以外の資料で調査を行った分野に含まれるもの

日本国実用新案公報	１９２２－１９９６年
日本国公開実用新案公報	１９７１－２００３年
日本国登録実用新案公報	１９９４－２００３年
日本国実用新案登録公報	１９９６－２００３年

国際調査で使用した電子データベース（データベースの名称、調査に使用した用語）

C.　関連すると認められる文献

引用文献のカテゴリー＊	引用文献名　及び一部の箇所が関連するときは、その関連する箇所の表示	関連する請求の範囲の番号
X	JP 2001-156331 A(日亜化学工業株式会社)2001.06.08 全文,全図（ファミリーなし）	1-2,4-5,10
X	JP 2001-307506 A(株式会社日立製作所)2001.11.02 全文,全図（ファミリーなし）	1-3,5,10
X	JP 2000-068555 A(株式会社日立製作所)2000.03.03 全文,全図（ファミリーなし）	1,2,5,10

☒ Ｃ欄の続きにも文献が列挙されている。　☐ パテントファミリーに関する別紙を参照。

＊　引用文献のカテゴリー
「Ａ」特に関連のある文献ではなく、一般的技術水準を示すもの
「Ｅ」国際出願日前の出願または特許であるが、国際出願日以後に公表されたもの
「Ｌ」優先権主張に疑義を提起する文献又は他の文献の発行日若しくは他の特別な理由を確立するために引用する文献（理由を付す）
「Ｏ」口頭による開示、使用、展示等に言及する文献
「Ｐ」国際出願日前で、かつ優先権の主張の基礎となる出願の日の後に公表された文献
「Ｔ」国際出願日又は優先日後に公表された文献であって出願と矛盾するものではなく、発明の原理又は理論の理解のために引用するもの
「Ｘ」特に関連のある文献であって、当該文献のみで発明の新規性又は進歩性がないと考えられるもの
「Ｙ」特に関連のある文献であって、当該文献と他の１以上の文献との、当業者にとって自明である組合せによって進歩性がないと考えられるもの
「＆」同一パテントファミリー文献

国際調査を完了した日 １８．０９．０３	国際調査報告の発送日 07.10.03
国際調査機関の名称及びあて先 日本国特許庁（ＩＳＡ／ＪＰ） 郵便番号１００－８９１５ 東京都千代田区霞が関三丁目４番３号	特許庁審査官（権限のある職員） 道祖土　新吾　２Ｋ　９８１４ 電話番号　０３－３５８１－１１０１　内線　３２５３

様式ＰＣＴ／ＩＳＡ／２１０（第２ページ）（１９９８年７月）

Ｃ（続き）．　関連すると認められる文献

引用文献のカテゴリー＊	引用文献名　及び一部の箇所が関連するときは、その関連する箇所の表示	関連する請求の範囲の番号
A	JP 2001-351789 A(東芝ライテック株式会社)2001.12.21 全文,全図（ファミリーなし）	6
A	JP 59-206873 A(株式会社東芝)1984.11.22 全文,全図（ファミリーなし）	6

(12)特許協力条約に基づいて公開された国際出願

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特願2002-225043 2002 年8 月1 日 (01.08.2002) JP
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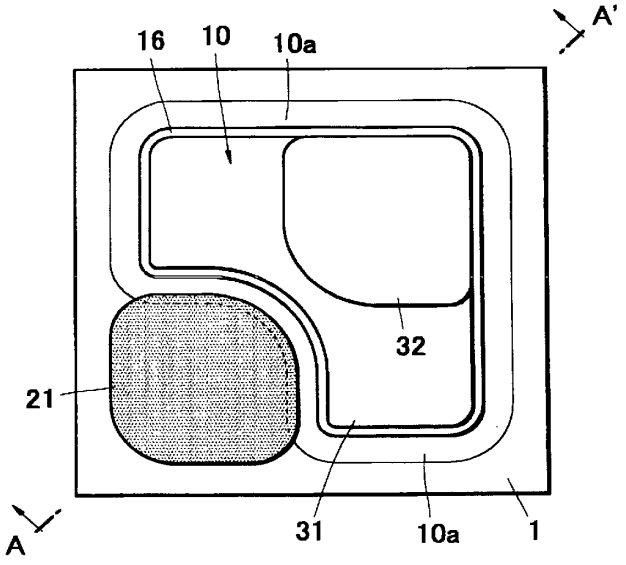
(81) 指定国 (国内): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, KE, KG, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) 指定国 (広域): ARIPO 特許 (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), ユーラシア特許 (AM,

[続葉有]

(54) Title: SEMICONDUCTOR LIGHT-EMITTING DEVICE, METHOD FOR MANUFACTURING SAME AND LIGHT-EMITTING APPARATUS USING SAME

(54) 発明の名称: 半導体発光素子及びその製造方法並びにそれを用いた発光装置



(57) Abstract: A nitride semiconductor light-emitting device comprising a multilayer portion deposited on a substrate and having an n-type semiconductor layer, an active layer and a p-type semiconductor layer, wherein the multilayer portion emits light. The lateral surface of the multilayer portion is a slope including the surface of the n-type semiconductor layer, and an n electrode is formed on the surface of the n-type semiconductor layer. With the above-described device structure, the luminous efficiency and light-output efficiency are increased.

[続葉有]

WO 2004/013916 A1

AZ, BY, KG, KZ, MD, RU, TJ, TM), ヨーロッパ特許 (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI 特許 (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

添付公開書類:
— 国際調査報告書
— 請求の範囲の補正の期限前の公開であり、補正書受領 の際には再公開される。

２文字コード及び他の略語については、定期発行される各*PCT*ガゼットの巻頭に掲載されている「コードと略語のガイダンスノート」を参照。

(57) 要約: 基板上に、ｎ型半導体層、活性層及びｐ型半導体層が積層されてなる積層部を有し、その積層部で発光する窒化物半導体発光素子において、積層部の側面は、ｎ型半導体層の表面を含む傾斜面であり、そのｎ型半導体層の表面にｎ電極が形成されている。こうした素子構造により、発光効率が高くかつ光の出射効率が高くなる。

明 細 書

半導体発光素子及びその製造方法並びにそれを用いた発光装置

技術分野

本発明は、半導体を用いた発光素子に係り、特に窒素を含む化合物半導体である窒化物半導体を用いた素子に係り、窒化物半導体の発光素子は、ＧａＮ、ＡｌＮ、もしくはＩｎＮ、又はこれらの混晶であるＩＩＩ－Ｖ族窒化物半導体（ＩｎｂＡｌｃＧａ１－ｂ－ｃＮ、０≦ｂ、０≦ｄ、ｂ＋ｄ＜１）を用いた発光素子で、発光装置、投光器、集合ランプ、イルミネーション、光結合装置、光検知装置、光通信装置、光ファイバモジュールの光源などに用いられる発光素子及びその発光素子の製造方法に関する。

背景技術

近年、窒化ガリウム系化合物半導体を用いた発光ダイオードが、紫外域、青色等の比較的短い波長域を中心に広く用いられるようになって来ている。この窒化ガリウム系化合物半導体は直接遷移であり発光効率が高いことからもその適用範囲が拡大している。

そのような発光素子には様々な素子構造、特に半導体の積層体の形状、電極構造・配置が提案されている。

発明の開示

（第１の発明）

本発明は半導体の積層体を有する発光素子において、その積層体、積層部の形状を発光素子の発光効率、特に、光取出し効率、放熱特性に優れ、高出力で高信頼性の発光素子を提供するものである。具体的な構造としては、半導体層の構造体、例えば、第１導電型層と第２導電型層に挟まれた発光層を有する構造体が、発光素子に含まれ、その積層構造体に、発光層、第１，２導電型層の接合部（ｐ－ｎ接合部）、基板、電極形成面などの面に傾斜した側面を有する

構造部を有して、その傾斜構造部底面が方形状、多角形状であって、その底面角部において、底面角部の丸み、面取りが大きくなるように上面に延びる傾斜側面を有している。これにより、底面よりも上面に近い発光部を備えた発光素子構造体において、その発光部において発生した光をその発生部近傍にあるその角部傾斜面でもって、光の散乱が促進され、効果的に光を素子外部に取り出せる構造となる。

その具体的な構成は下記の通りである。

第１導電型層２と第２導電型層３とに挟まれた発光層４を有する構造を備えた半導体発光素子１００００において、前記第１，２導電型層２，３、発光層４の少なくとも一部が含まれて、断面において構造部幅の大きい底面側１０ｇと小さい上面側１０ｆを備えて、対向する側面１０ｘ，１０ｙが互いに傾斜した構造部１０が設けられると共に、前記構造部１０側面１０ｘ，ｙが、底面側１０ｇよりも上面側１０ｆの幅が大きな第１側面１０ｘと、上面側よりも底面側の幅が大きな第２側面１０ｙと、を有することを特徴とする半導体発光素子である。具体的には、図５３Ａ，Ｃに示すように、素子の構造部１０において、底面側１０ｇよりも面積の小さい上面側１０ｆであって、図中の１点鎖線部１０ｘ－１、１０ｘ－２に挟まれた、区切られた側面について、各角部を構成する側面１０ｘが、上面側に向かって幅が大きくなるような側面として形成され、他方、上面側に向かって幅が小さくなるような側面１０ｙが設けられた構造を有することで、図５３Ｂに見るように、図中の矢印の発光素子からの光が、構造部の高さ方向に（上面側に近づくにつれて）、その幅が逆に変化する側面１０ｘ（大きくなる）、１０ｙ（小さくなる）ことで、その構造部内において、構造部高さにより、その高さの面（上面に平行な面若しくは高さ方向軸を法線とする面）における各側面により構成される各辺の長さの比が変化し、またその高さ面に上面側に設けられて被さる側面の占有面積比が変化することから、これら側面による底面側への光の反射が分散されて、光が偏る傾向にある発光素子において、均一性、光取り出しに優れた発光素子が得られる。

前記第１側面１０ｘが、底面１０ｇにおいて構成辺１０ｇ－１，－２に挟まれた角部１０ｇ－ｘに設けられていることを特徴とする半導体発光素子である。

その具体例として、図５３Ａの構造部１０、及びその部分拡大図５３Ｂ、別の形態を説明する図５３Ｃに見るように、方形状、多角形状の底面部１０ｇから上面に近づくにつれ断面幅が小さくなるような傾斜側面を備えた構造部１０で、その底面若しくは上面の角部が、切り子、若しくは隅切形を形成する第１側面１０ｘが設けられることで、上述したような発光素子内に伝搬する光を効果的に底面側方向に反射させる構造、若しくは上面側方向に取り出す構造とできる。

前記構造部が、その内部に前記発光層を備えることを特徴とする半導体発光素子である。図５３Ａ～Ｄの点線部４として示すように、発光素子において、発光源となる発光層が上記特有の形状を有する構造部内、上記上面と底面間に設けられることで、素子内部への無駄な伝搬を減らし、光源から近距離において、上記側面に依る反射、光取り出し効果が得られ、光取り出し効率に優れる発光素子が得られる。

前記構造部の底面側が方形状、多角形状であり、該形状の底面側構成辺に前記第２側面が設けられ、該形状の角部が前記第１側面が設けられていることを特徴とする半導体発光素子である。上述したように、角部１０ｘが上面側に近づく、高さが高くなるにつれて、幅広となる末広型の第１側面１０ｘが設けられ、他方底面側に近づくにつれて幅広となる末広型の第２側面１０ｙが、底面の構成辺１０ｇ－１，－２を形成することで、底面部を所望の形状として、その角部が高くなるに従い末広型の側面として形成されることとなり、様々な形状について上記本発明ができようできる。

前記構造部が錐体形状を有することを特徴とする発光素子である。後述する第２，３の発明と同様に、錐体形状であることで、面内集積度を高め、加工精度に優れた好適な発光素子が得られる。

前記第１側面が、構造部外側に向かって凸な湾曲面であることを特徴とする半導体発光素子である。図５３Ｂに示されるように、第１側面と第２側面とが互いに異なる曲面、曲率半径、若しくは第２側面が平面で形成されることで、光の反射、取り出し機能において、様々な方向への放散が可能となり、光の集中を軽減した発光素子が得られる。

前記構造部上面、底面における第１側面が丸みを帯びた構成辺を形成し、該

丸みの曲率半径が底面側より上面側が大きいことを特徴とする半導体発光素子である。図５３Ｂに見られるように、具体的な構成として、曲率が上面側ほど大きくなることで、上面の法線方向において、傾斜面（その前記法線方向への投影像が重なる領域）にとは、光伝搬性能が異なることになるが、図に見るように、上面の面内方向への光伝搬を促すことができる。また、後述するマスク形成において、上面側が曲率半径の大きな角部丸めが施されることで、マスクの形成精度が高まり、もって、傾斜面に電極、保護膜を形成する際の精度を高めて、精密なデバイス構造をとることができ、特性に優れた素子が得られる。

前記発光素子が、前記構造部を複数有して、各構造部がほぼ同時に発光されるように電極構造が形成されていることを特徴とする発光素子である。

前記発光素子が、構造部上面に同一面側に正負一対の電極を有することを特徴とする発光素子である。後述の第２の発明に同様な素子構造とできる。

前記発光素子の一方の電極は、前記構造部側面の一部を覆って形成されていることを特徴とする発光素子である。

前記構造部が基板上に互いに分離されて複数設けられ、各構造部がほぼ同時に発光できるように電極が設けられていることを特徴とする発光素子である。

前記発光素子が構造部上面側を実装面側として、実装基体に載置され、前記構造部に設けられた一方の電極は、基板面の上に設けられ、他方の電極は、互いに分離された複数構造部上面に接続するような配線が前記実装基体側に設けられていることを特徴とする発光素子である。図１６Ｂに見るように、一方を半導体層積層基板側、他方を実装面側に配線して接続することで、空間を有効に活用でき、構造部間の空間に様々デバイス機能、例えば反射膜、光取り出し膜、光変換部材を備えることができ、また、基板側に絶縁膜を介して正負電極及びその配線電極を立体交差させる際のリークの問題も解決される。

前記発光素子が、構造部上面、底面側に対向配置された一対の電極を有し、それぞれ第１，２導電型層表面に設けられていることを特徴とする発光素子である。後述の第３の発明のような対向配置電極構造の発光素子への応用が可能となる。

前記発光素子の構造部側面を覆う透光性絶縁膜を介して充填部材を有すること

を特徴とする発光素子である。上述したように、構造部側面は内部方向への光反射膜として機能させる際に、外部に出射した光もそれを被覆する透光性の膜、金属などの反射膜の構造部側各面により反射され、素子外部に幾重にも反射構造を備えた発光素子とでき、光制御性、発光効率に優れた発光素子が得られる。

前記発光素子が、複数の構造部を有し、該構造部間に凸状の充填部材を有することを特徴とする発光素子である。充填部材は、後述する第３の発明のように、金属部材７なども用いることができるが、これにより、素子の放熱性、光反射性、素子の強度に優れた素子が得られる。

前記発光素子の構造部が発光層を内部に有し、前記充填部材が前記発光層よりも構造部底面側に突出して形成されていることを特徴とする発光素子である。これにより、上述した放熱源、光源となる発光素子に隣接して、充填剤が設けられることになり、これらを改善した構造とできる。

（第２の発明）

窒化ガリウム系化合物半導体は通常、絶縁基板であるサファイア基板の上に成長されることに起因して、従来の窒化物半導体発光素子には以下のような課題があった。第１に、サファイア基板が絶縁体であるために、ｎ側の電極とｐ側の電極をいずれも、サファイア基板上の窒化ガリウム半導体の上に形成する必要があり、特にｎ側の電極部分は、非発光領域となり、発光領域から生じた光が、ＧａＮ層を横方向に伝播する際の多重反射により吸収され、取り出し効率を低下させるという問題点があった。第２に、発光した光は基板面に対して通常は垂直方向に取り出すように構成されるが、発光ダイオードの側面から出射される光の割合が比較的高く、発光した光を効果的に利用することができないという問題があった。

そこで、本発明は、ｎ側電極下部での多重反射をなくし、ｎ側の電極による吸収を低減し、取り出し効率の高い窒化物半導体発光素子を提供することを第１の目的とする。また、本発明は発光した光を効果的に利用することができる窒化物半導体発光素子を提供することを第２の目的とする。

以上の従来の問題点を解決するために、本発明（第２の発明）に係る窒化物半導体発光素子は、基板上に、ｎ型半導体層、活性層及びｐ型半導体層が積層さ

れてなる積層部を有し、その積層部で発光する窒化物半導体発光素子において、上記積層部の側面は、上記ｎ型半導体層の表面を含む傾斜面であり、そのｎ型半導体層の表面にｎ電極が形成されたことを特徴とする。以上のように構成された窒化物半導体発光素子は、光の出射効率を高くできる。

本発明に係る窒化物半導体発光素子では、上記ｎ電極は上記積層部を囲むように形成されていることが好ましい。これにより、少ない面積の電極接触面（半導体構造体への電流供給面）であっても効率的な素子構造体への電流注入が実現される。

また、本発明に係る窒化物半導体発光素子では、上記ｎ電極を上記基板の側面から上記基板の下面にも連続して形成することができる。このようにすると、ｐ側オーミック電極を透光性電極としてその透光性電極を介して光を出射させる場合に、上記基板の側面及び上記基板の下面で反射した光も透光性電極を介して出力できるので、光の取り出し効率を高くできる。

また、本発明に係る窒化物半導体発光素子では、上記発光領域となる積層部を複数形成することもでき、これにより、大面積でかつ発光効率の高い窒化物半導体発光素子を構成できる。

上記積層部を複数形成した窒化物半導体発光素子では、上記各積層部に形成されたｎ電極を互いに接続して共通電極として形成することができる。これにより、上記発光領域である積層部を容易に並列接続することが可能となる。

また、上記積層部を複数形成した窒化物半導体発光素子では、上記ｎ電極を互いに接続して共通電極として形成するとともに、上記各積層部において形成された上記ｐ型半導体層とオーミック接触するｐ側オーミック電極を互いに接続することもできる。これにより、上記発光領域である積層部が素子上で並列接続された窒化物半導体発光素子を提供できる。各積層部を電気的に接続する配線電極は、正負とも基板側に配線され設けられていても良く、一方（基板側の第１導電型層であるｎ型層）を基板側、例えば基板面上、第１導電型層の積層部から露出した露出面（電極形成面上など）に配線して、他方（第１導電型層よりも基板に遠い第２導電型層であるｐ型層）を発光素子を実装する実装基体、例えばヒートシンク、サブマウントなど、若しくは発光装置の素子実装部、実装側リード、側に発

光素子に設けられた複数の積層部上部側電極間を互いに接続可能なような配線を設けても良い。他方を発光素子外部の実装基体（実装素子）側、発光装置実装部側に配線すると、発光素子において凸状の積層部による素子上面の起伏、凹凸が大きい場合に精度良く配線困難な場合にも良好に複数の積層部を接続でき、また、他の構造物、例えば反射膜、絶縁膜、保護膜の形成が容易になり、より好適な素子構造が得られ好ましい。

また、本発明に係る窒化物半導体発光素子において、基板側から光を出力するように構成する場合には、光の出射効率を高くするために、上記積層部を覆うように反射層を形成することが好ましい。この場合、基板材料は、発光素子が発光する光・電磁波に対して透過性に優れ、自己吸収が少なく、透明な基板を選定すると良い。

また、上記窒化物半導体発光素子において、上記金属層は、上記積層部のｐ型半導体層にそれぞれ形成されたｐオーミック電極を接続する接続電極により構成することができる。

本発明に係る窒化物半導体発光素子において、上記反射層は上記積層部を覆うように絶縁膜を介して金属層を形成することにより形成してもよいし、誘電体多層膜により構成するようにしても良い。また、光・電磁波透過性の絶縁膜の屈折率と、発光積層部の半導体材料の屈折率を適宜調整することで、透過性絶縁膜も反射膜とでき、多層膜とする構成もでき、これら、分布ブラック反射膜（ＤＢＲ）の誘電体多層膜、光反射膜、絶縁膜を組み合わせて使用することもできる。

本発明に係る窒化物半導体発光素子において、上記傾斜側面は、外側に膨らんだ凸曲面とすることもできる。このように凸面、凸状の曲面、屈曲面、多面構造とすることで、前述の第１の発明における構造部の隅部、角部における凸状部との組み合わせにより、さらに効果的な光反射制御、光取り出し効率向上、光密度制御（特に発光部）が可能となり好ましい。

このような第２の発明の効果として、本発明に係る窒化物半導体発光素子は、傾斜した側面を持った積層部を有し、その積層部の側面のｎ型半導体層の表面にｎ電極を形成することによりｎ電極による光の吸収を抑制でき、光の出射効率を高くできる。特に、基板と積層部とが互いに屈折率が異なり、基板上に第１導電

型層の電極（ｎ電極）と、積層部の傾斜側面に設けられることで、発光積層部の光を傾斜面により、光学的に接続された基板に伝搬させ、また、電極が構造部側面と基板上に跨って形成されることで、素子に接触する電極面積を減少させることができる。

（第３の発明）

また、特開２００１－３１３４２２号公報（第６頁右欄８行～第７頁左欄４２行、図８，図９）に開示された方法は、個々の素子に分割した際に切断面（分割後の素子の側面）でｐ側の層とｎ側の層とが短絡しやすいという問題があったため、本発明の第２の課題（第１と２の発光素子）としては、側面における短絡を防止することができる窒化物半導体発光素子の構造及びその製造方法を提供することを目的とする。その他の従来例として、特開平８－３３０６２９号公報（図１～図３）がある。

この目的（第２の課題）を達成するために、本発明に係る第１の窒化物半導体発光素子は、ｎ型窒化物半導体層とｐ型窒化物半導体層の間に、窒化物半導体からなる発光層を有してなる窒化物半導体発光素子において、少なくとも上記ｐ型窒化物半導体層と上記発光層を含むように台形錐形状の積層体が形成され、該積層体は側面が絶縁されるように金属部材に埋め込まれたことを特徴とする。この充填部材となる金属部材により、凸状の積層体をウエハ上、１つの素子内に複数設けることにより、エピタキシャル層（成長層）の強度を補強し、また、充填部は、凸状積層体（発光構造部）間、若しくはその周囲に設けられる素子の凹部に埋め込まれることで、比較的素子動作部（発光部）に接近して充填部材が設けられることになり、各動作部（積層体）からの放熱を助け、素子の放熱性を高めて、高出力、大電流駆動に優れた発光素子が得られる。さらにこのような充填部材は、発光部近傍に設けられることで、反射膜、反射機能を有する構造物、若しくはその基礎、土台として機能させることもできる。

また、本発明（第３の発明）に係る第２の窒化物半導体発光素子は、ｎ型窒化物半導体層とｐ型窒化物半導体層の間に、窒化物半導体からなる発光層を有してなる窒化物半導体発光素子において、少なくとも上記ｐ型窒化物半導体層と上記発光層を含むように台形錐形状の積層体が形成されて、その積層体が該積層体の

表面に沿って対向するように設けられた金属部材により保持されたことを特徴とする。

以上のように構成された窒化物半導体発光素子において、上記積層体は側面が絶縁されるように金属部材に埋め込まれていて、切断時又は切断後に積層体の側面が損傷を受けることがないので、信頼性を向上させることができる。

また、本発明に係る窒化物半導体発光素子は、両側に電極を形成することができるので、一方の面に正負の電極を設けた従来の窒化物半導体発光素子に比較して発光領域を大きくとることができる。

本発明に係る第１と第２の窒化物半導体素子では、上記金属部材の上記積層体の反対側に位置する面が、平坦な面であることが好ましい。

このようにすると、素子を実装する際に、実装基板にその平坦な面を対向させて実装することにより容易に実装することが可能になる。

また、上記第１と第２の窒化物半導体素子では、上記ｎ型窒化物半導体層の対向する２つの面のうちの上記積層体の反対側に位置する面に透明電極を形成するようにして、該透明電極を介して光を出射するようにしてもよい。また、透明電極は、素子の光、電磁波を透過して、注入電流を素子面内に拡散させる透過性電流拡散導体として機能するものであり、透明導電膜の他、光、電磁波を通過させる開口部、窓部を有する金属膜、例えば格子状、枝状、放射状の電極を適用することもできる。

このようにすると発光層全体に均一に電流を注入することができ、均一な発光が可能になる。この場合、上記透明電極は透光性が高くかつ抵抗値を低くできるＩＴＯであることが好ましい。その他に酸化物導電膜、酸化物半導体膜、透明導電膜なども適用できる。

また、本発明の第１と第２の窒化物半導体発光素子において、上記ｐ型窒化物半導体層とオーミック接触するように上記積層体と上記金属部材の間に形成されるｐ型電極は、Ｒｈを含むことが好ましく、これにより電極の剥離を防止できる。このように、ｐ型窒化物半導体の電極として優れた材料、例えば貴金属、白金族元素、を用い、さらに反射性、密着性の点でＲｈが好ましい。

さらに、本発明の第１と第２の窒化物半導体発光素子において、上記積層体は

上記ｎ型窒化物半導体層の一部を含んで構成されていてもよいし、上記ｎ型窒化物半導体層の全てを含むように構成されていてもよい。

また、本発明の第１と第２の窒化物半導体発光素子において、より確実に発光領域の形状を保持するために、上記金属部材の厚さは５０μｍ以上であることが好ましい。

また、本発明の第１と第２の窒化物半導体発光素子においては、上記積層体を複数個備えていてもよく、複数の積層体を用いて発光素子を構成することにより、大面積の発光素子を構成できる。

さらに、上記積層体を複数個備えた発光素子では、上記複数の積層体は、共通のｎ型窒化物半導体層の上に設けられていてもよいし、各積層体ごとに分離されていてもよい。

このような第３の発明の効果として、本発明に係る窒化物半導体発光素子は、ｎ型窒化物半導体層とｐ型窒化物半導体層の間に、窒化物半導体からなる発光層を有してなる窒化物半導体発光素子において、上記ｐ型窒化物半導体層と上記発光層を含むように台形錐形状の積層体を形成し、該積層体を側面が絶縁されるように金属部材に埋め込んでいるので、切断時又は切断後に積層体の側面が損傷を受けることがない。したがって、本発明に係る窒化物半導体発光素子によれば、信頼性を向上させることができる。

（第４の発明）

本発明において、第４の発明としては、上記第１～３の発明における発光素子を用いた発光装置にかかるものであり、具体的な構成としては下記の通りである。

上記本発明の発光素子が載置される載置部を有する発光装置であって、前記載置部に、発光素子が支持基板上に実装されて、載置されていることを特徴とする発光装置である。

上記本発明の発光素子を用いた発光装置であって、発光装置には、発光素子から光の一部を、それとは異なる波長の光に変換する光変換部材を有することを特徴とする発光装置。

前記光変換部材が、Ａｌを含み、かつＹ、Ｌｕ、Ｓｃ、Ｌａ、Ｇｄ、Ｔｂ、Ｅｕ及びＳｍから選択された少なくとも一つの元素と、Ｇａ及びＩｎから選択さ

れた一つの元素とを含むアルミニウム・ガーネット系蛍光体であって、さらに希土類元素から選択された少なくとも一つの元素を含有するアルミニウム・ガーネット系蛍光体を有することを特徴とする発光装置である。

前記光変換部材が、$(Re_{1-x}R_x)_3(Al_{1-y}Ga_y)_5O_{12}$（$0<x<1$、$0\leqq y\leqq 1$、但し、Reは、Y，Gd,La，Lu，Tb，Smからなる群より選択される少なくとも一種の元素であり、RはCe又はCeとPrである）であらわされる蛍光体を有することを特徴とする発光装置である。

前記光変換部材が、Nを含み、かつBe、Mg、Ca、Sr、Ba、及びZnから選択された少なくとも一つの元素と、C、Si、Ge、Sn、Ti、Zr、及びHfから選択された少なくとも一つの元素とを含み、希土類元素から選択された少なくとも一つの元素で付活された窒化物系蛍光体を有する発光装置である。

前記窒化物系蛍光体が、一般式$L_XSi_YN_{(2/3X+4/3Y)}$：Eu若しくは$L_XSi_YO_ZN_{(2/3X+4/3Y-2/3Z)}$：Eu（Lは、Sr若しくはCa、又は、Sr及びCa、のいずれか。）で表されることを特徴とする発光装置である。

また、第１の発明は下記第２，３の発明を包含して、それぞれに適用することができる。例えば、第２の発明は、基板上の同一面側に、正負一対の電極、例えば、第１導電型層（ｐ型層）の電極（ｐ側電極）と第２導電型層（ｎ型層）の電極（ｎ側電極）、を有する第１の発明の一形態であり、第３の発明は、正負一対の電極、例えば、第１導電型層（ｐ型層）の電極（ｐ側電極）と第２導電型層（ｎ型層）の電極（ｎ側電極）、が発光素子の構造体を挟んで対向して配置された電極構造を有する第１の発明の一形態である。また、第２，３の発明では、第１の発明における発光素子として、窒化物半導体を用いた発光素子について説明するが本発明（１，２，３）はこれに限定されない。また、第２，３の発明では、第１導電型層をｎ型窒化物半導体層、第２導電型層をｐ型窒化物半導体層として、具体的に説明するが、逆でも良く、また、各導電型層（第１，２導電型層）に設けられる電極についても同様である。また、図面においては、その図中、本明細書中の符号の下二桁は、各発明、各実施形態、各実施例、及びその図における各構成要素についてを示すものであり、符号の下二桁が同じ構成要素は、互いに相当な関係にあり、また下二桁が「００」の場

合は上三桁若しくは下４桁移行の数字について上記下２桁と同様な関係にある。また、下２桁目は同様な構成の変形例を示す場合があり、具体的には、発光素子の積層構造１０は、その１０番台において具体的な層構成を示し、２０番台は第１導電型層（ｎ型層）の電極（ｎ電極）の各例を示し、３０番台は第２導電型層（ｐ型層）の電極（ｐ電極）の各例を示し、６０番台は接続電極（配線電極）の各例を示す。さらに各図面は模式的な図として示すものもあり、一部を誇張して示すものもある。

図面の簡単な説明

図１は、本発明に係る実施の形態１の発光素子の平面図である。

図２は、図１のＡ－Ａ’線についての断面図である。

図３は、本発明に係る実施の形態１の変形例の発光素子の平面図である。

図４は、図３のＢ－Ｂ’線についての断面図である。

図５は、本発明に係る実施の形態２の発光素子の平面図である。

図６は、本発明に係る実施の形態３の発光素子の平面図である。

図７は、図６のＣ－Ｃ’線についての断面図である。

図８は、実施の形態３の変形例に係る発光素子の断面図である。

図９は、本発明に係る実施の形態４の発光素子の平面図である。

図１０は、実施の形態４の変形例に係る発光素子の平面図である。

図１１は、本発明に係る実施の形態５の発光素子において、ｐ側の電極を省いて示す平面図である。

図１２は、本発明に係る実施の形態５の発光素子の平面図（ｐ側の電極を含む）である。

図１３は、図１２のＤ－Ｄ’線についての断面図である。

図１４は、実施の形態５の第１変形例に係る発光素子の平面図である。

図１５は、実施の形態５の第２変形例に係る発光素子の平面図である。

図１６Ａは実施の形態５の第３変形例に係る発光素子の平面図であり、図１６Ｂは図１６ＡのＧ－Ｇ‘線において発光素子を実装基体に実装した例を示す断面図である。

図１７は、本発明に係る実施の形態６の発光素子の平面図である。

図１８は、図１７の一部を拡大して示す平面図である。

図１９Ａは図１８のＥ－Ｅ’線についての断面図であり、図１９Ｂは図１８のＦ－Ｆ’線についての断面図である。

図２０Ａ～Ｃは、本発明の窒化物半導体発光素子において、傾斜側面を有する積層部の形成方法の一例を示す工程図である。

図２１は、従来例の発光素子の断面図である。

図２２は、本発明の窒化物半導体発光素子において、傾斜側面の好ましい傾斜角について説明するための模式図である。

図２３Ａ～Ｃは、本発明の窒化物半導体発光素子において、（ｐ側）電極７３１による光の吸収が積層部の形状とその配列により抑制できることを説明するための各図である。

図２４は、実施の形態５の第４変形例に係る発光素子の平面図である。

図２５は、本発明に係る実施の形態６において、取り出し効率の測定に用いた発光素子の平面図である。

図２６は、本発明に係る実施の形態６の比較例（その１）として、取り出し効率の測定に用いた発光素子の平面図である。

図２７は、本発明に係る実施の形態６の比較例（その２）として、取り出し効率の測定に用いた発光素子の平面図である。

図２８は、本発明に係る実施の形態６の取り出し効率の測定において、基準として用いた発光素子の平面図である。

図２９Ａ～Ｂは、本発明に係る実施の形態６において、比較例の基準として用いた発光素子の平面図である。

図３０は、本発明に係る実施の形態６の取り出し効率の測定方法の概要を示す模式図である。

図３１は、本発明に係る実施の形態７の発光素子の平面図である。

図３２は、実施の形態７の発光素子の一部を拡大して示す平面図である。

図３３Ａは本発明に係る実施の形態８の実装基体に実装された発光素子を説明する平面（素子構造透視図）図であり、図３３Ｂは図３３ＡのＨ方向からの

側面図である。

図３４は、本発明に係る実施の形態９の窒化物半導体発光素子の断面図である。

図３５は、本発明に係る実施の形態９の窒化物半導体発光素子の製造方法において、サファイア基板上に半導体層を形成した後の断面図である。

図３６は、実施の形態９の製造方法において、サファイア基板上に半導体層をエッチングして積層体を形成した後の断面図である。

図３７は、実施の形態９の製造方法において、各積層体の上に（ｐ側）電極を形成した後の断面図である。

図３８は、実施の形態９の製造方法において、絶縁層５を形成した後の断面図である。

図３９は、実施の形態９の製造方法において、反射層６を形成した後の断面図である。

図４０は、実施の形態９の製造方法において、金属部材７を形成した後の断面図である。

図４１は、実施の形態９の製造方法において、積層体１０成長用基板１を剥離した後の断面図である。

図４２は、実施の形態９の製造方法において、積層体１０成長用基板１を剥離した後にｎ型窒化物半導体層（第２導電型層）２の上に透明電極を形成した後の断面図である。

図４３は、実施の形態９の製造方法において、透明電極を形成した後にｎパッド電極と絶縁膜４を形成した後の断面図である。

図４４Ａ～Ｃは、実施の形態９の製造方法において、台形錐形状の積層体の形成方法を示す断面図である。

図４５は、実施の形態９の変形例の窒化物半導体素子の断面図である。

図４６は、実施の形態９の図４５とは別の変形例の窒化物半導体素子の断面図である。

図４７は、実施の形態１０の窒化物半導体素子の断面図である。

図４８は、実施の形態１０の変形例１の窒化物半導体素子の断面図である。

図４９は、実施の形態１０の変形例２の窒化物半導体素子の断面図である。

図５０は、実施の形態１０の窒化物半導体素子の平面図である。

図５１は、実施の形態１０の変形例３の窒化物半導体素子の平面図である。

図５２Ａ～Ｂは、第１の発明における構造部１０の形状例を説明する模式的斜視図である。

図５３Ａ，Ｃは第１の発明における構造部１０の形状例を説明する模式的斜視図であり、図５３Ｂは図５３Ａの一部（構造部側面１０ｘ，ｙ）を拡大した模式的斜視図であり、図５３Ｄは図５３Ａに第２電極（ｎ電極）２１を設けた状態における模式的上面図である。

図５４Ａは第４の発明（実施形態１０）における発光装置を説明する模式的断面図であり、図５４Ｂはその等価回路図である。

図５５は、第４の発明（実施形態１１）における発光装置を説明する模式断面図である。

図５６は、第４の発明における発光装置を説明する模式断面図である。

図５７Ａ～Ｄは、本発明の発光素子における凹凸面600について説明する模式断面図である。

図５８は、本発明の発光素子における素子構造を説明する模式断面図である。

図５９Ａ～Ｂは、本発明の発光素子における基板除去を説明する模式断面図である。

図６０Ａ～Ｅは、本発明の発光素子における素子構造と電極構造を説明する模式的斜視図である。

発明を実施するための最良の形態

（第１の発明）

本発明における第１の発明は、発光素子構造の少なくとも一部、好ましくは素子動作部（電流注入部内）に設けられる凸状の構造部であり、また、素子積層構造の非動作部（非電流注入部）、若しくは、その他、発光素子に用いられる透光性部材にも適用できる。具体的には、図５３Ａ～Ｄに本発明の構造部１０を模式的に説明する斜視図Ａ，Ｃ、とその図Ａの一部を拡大して示すものであり、上面図を示すものである。

一方、図５２Ａ～Ｂは、第１の発明について比較対照するための構造部１０の例である。図５２Ａから判るように底面１０ｇが四角形状の錐体状構造部において、図中の点線１０ｘ－１，２のように角を面取りして多角形状とすると、図５２Ｂに見られるように、底面側１０ｇから上面側に向かって幅が狭くなるような側面形状となり、また、構造部の高さにおける高さ方向軸を法線とする切断面において、それを側面と切断面が成す構成辺において、各辺の長さの比は、どの高さにおいても同じような比率となる。このような、凸状構造部では、例えば発光層４が内部に設けられる場合に、真横での側面反射が大きく、その他は、弱い光の反射となり、さらに上面平面部では、十分な光の反射制御が成されないことから、上面の法線方向における光強度は弱くなり、また、発光層４付近からの反射が他の側面領域における反射より強くなり、円環状に強い発光が偏った光となってしまう。

さらに製造上の問題として、後述の第２の発明に示すように側面において電極を設ける場合には、図５２Ｂの点線２１ｍとして示すように、その形状精度が悪くなる傾向にある。これは、凸状部１０上のマスクＭ１が形成される状態を図に示すように、上面側における面取り部の幅が小さいと、レジストなどのマスクの側面への回り込みが不十分となり、凸状部１０の狭い面取り部の肩において、マスク材が横方向に出っ張る傾向にあり、特に上面１０ｆの辺が短い場合に、突出傾向が顕著となり、電極形状２１ｍが不安定な形状として形成される。このような電極形状不安定性は、十分な電極形成面積が確保できない第２の発明のような場合には、深刻な問題となる傾向にある。

また、図５２Ａに示すように、上面部１０ｆにおいて電極形成され、電流注入されると、小さく狭まった領域、例えば、上面の角、短い構成辺周辺において、電流のムラが発生しやすい傾向にある。

本発明では、上記問題点を解決するものであり、具体的には図５２Ａに示すように、傾斜側面を備えた凸状部の構造部１０において、その側面の幅が、上面側に近づくにつれて広くなる、若しくは角部丸めにおいて、その曲率半径が大きくなるような第１側面１０ｘを備えるものであり、これにより、構造部高さにおける切断面の切断形状が、高さによって、例えば辺の長さの比が大きく変化し、す

なわち、高さにより、側面の囲み状態が多様性に富む形状を有することになり、従って、上述したように、側面反射・出射領域における光の指向性のムラが改善され、さらに、電流注入においては、上面側の角部が十分大きな領域が形成されており、電流のムラ発生を改善でき、さらに、上面側の構成辺が大きく、若しくは、湾曲された曲面で構成されることで、レジストはみ出しが改善されて、素子加工、電極などのデバイス加工に優れた構造部とでき、信頼性、量産性に優れた発光素子となる。

第１の発明の形成方法としては、図２０Ａ～Ｃ、図４４Ａ～Ｃなどに説明されるように、マスクＭ１の膜厚変化、形状の異なるマスクの多層構造など、マスク形状・膜厚を適宜選択することで、本発明の構造体を得ることができる。

本発明における側面構成辺については、底面１０ｇ側において、幅広で上面１０ｆ側に向かって幅が狭くなる第２側面１０ｙと、それとは逆の第１側面１０ｘを備えることが好ましく、このとき、上面側の形状に依っては、例えば図５３Ｃに見られるように、底面１０ｇ側における幅広側面１０ｙ（その構成辺１０ｇ－１）が形状変化して、両者の境界線である１０ｘ－１，２が途中で消滅する場合もあり、必ずしも第２側面が上面側に到達する必要はない。そのため、上面１０ｆと底面１０ｇが図５３Ｃの点線１０ｆ、ｇに示すように異なる平面形状となる場合もある。また、上面側に十分な曲面を設けることで、円形状となる場合にも本発明は適用される。また、上面１０ｆ、底面１０ｇは、構造部に対して、任意の高さ領域に設定でき、好ましくは、素子の積層構造に対応した突出全体を本発明の構造部の構成とすることが好ましい。さらに好ましくは、上記上面側に向かってその幅が末広型の第１側面においては、構造部１０の外側に向かって凸な曲面（凸面）を形成することが、上記光の反射、散乱作用、マスク形成精度に優れて好ましい。第１，２側面１０ｘ，ｙの上面側、底面側の構成辺の長さの関係は特に限定されないが、図５３Ａに見るように、上面、底面とも第１側面による辺が第２側面のそれより小さくすることで、好適な凸部形状が得られる。

また、それにより形成される電極形状としては、図５３Ｄの平面図においてハッチングを施して示すが（電極２１）、その上面側周縁が、構造部の角部（第１側面）の曲率半径、若しくは辺の長さより、図中点線（２１ｇ－ｘ）で示すよう

に、大きな形状で電極が形成され、例えば図５３Ｃなど、これにより、囲み電極の折れ曲がり部において構造部１０（角部１０ｆ－ｘの下方）より大きな形状で折れ曲がることから、その場所における電流集中傾向を軽減できる。

本発明（第１及びそれを用いた第２，３の発明）は、図５３Ａ～Ｄに示すように、好ましくは、発光層４をその構造部１０内部に備えることで、光の制御性に優れた素子とでき、さらに好ましくは、第１導電型層２の一部と第２の導電型層３とそれに挟まれた発光層４を備えることであり、さらに好ましくは、上面に第２電極（第２導電型層３の電極，ｐ型層のｐ電極）を設けることである。また、構造部の側面形状は、断面形状が図５３Ａ～Ｄに見られるような直線状のものだけでなく、湾曲したもの、図５８に示すような階段状、テラス部２ｓを有するものとでき、これら側面の突出部上面２ｓの表面とその下方側面に電極が延伸して形成することもできる。

（第２の発明）

以下、図面を参照しながら本発明（第１の発明）に係る実施の形態の窒化物半導体発光素子について説明する。

実施の形態１（第２の発明）．

本発明に係る実施の形態１の窒化物半導体発光素子は、図１及び図２に示すように、発光領域を構成する積層部１０の側面を内側に傾斜した傾斜面１０ａとし、その傾斜面１０ａに露出したｎ型コンタクト層１２とオーミック接触するようにｎ電極２１を形成することにより構成されている。

実施の形態１の窒化物半導体発光素子において、積層部１０は、図２に示すように、サファイア基板１上に、バッファ層１１、ｎ型コンタクト層１２、ｎ型クラッド層１３、発光層１４、ｐ型クラッド層１５及びｐ型コンタクト層１６を順次成長させて積層構造を形成し、図１に示す平面形状（略矩形形状において、１つの隅部が円弧状に切り欠かれた形状）になるようにエッチングすることにより形成される。

積層部１０を構成する各層は例えば次のようなもので形成する。

バッファ層１１：４００℃～６００℃の低温で成長されたＧａＮ又はＡｌＧａＮ層、

ｎ型コンタクト層１２：ＳｉドープのＧａＮ（例えば、厚さ６μｍ）、

ｎ型クラッド層１３：ｎ型ＡｌＧａＮ、

発光層１４：ノンドープのＩｎＧａＮ井戸層を含む（例えば、厚さ約３０Å）単一又は多重量子井戸構造、

ｐ型クラッド層１５：ｐ型ＡｌＧａＮ、

ｐ型コンタクト層１６：Ｍｇがドープされ　ＧａＮ（例えば、厚さ約１２００Å）。

また、本実施の形態１において、積層部１０を形成するためのエッチングは、サファイヤの表面が露出するまで行い、積層部１０が円弧状に切り欠かれた１つの隅部にｎ電極２１を形成するためにサファィヤ基板表面を露出させる。尚、本実施の形態１では、ｎ電極２１を形成するために露出されたサファイア基板の表面と連続して積層部１０の周りを取り囲むようにサファィヤ基板の表面が露出される。

本実施の形態１において、ｎ電極２１は、図１及び図２に示すように、積層部１０の１つの隅部に露出させたサファィヤ基板１の表面から積層部１０の傾斜面１０ａに亙って連続して形成し、傾斜面１０ａに露出したｎ型コンタクト層１２とオーミック接触する。

また、ｐ側の電極は全面電極３１とｐパッド電極３２とからなり、全面電極３１は積層部１０の最上層に位置するｐ型コンタクト層１６の表面のほぼ全面に形成され、ｐパッド電極３２は全面電極３１上のｎ側電極２１と対角をなす位置（他方の隅部）に形成される。

以上のように構成された実施の形態１の窒化物半導体発光素子は、ｎ電極２１による光の吸収を極めて少なくできるので、効率良く光を出力できる。

すなわち、図２１に示す従来の構造では、基板１とｎ電極５２１の間に存在するｎ型コンタクト層５１２に発光領域で発光した光が漏れ出して導波し、基板１の上面とｎ電極１２１の裏面により繰り返して反射される間に（図２１において、Ｙ１００の符号を付して模式的に示す）、大部分の光がｎ電極１２１によって吸収されて結局外部に取り出すことができないという問題があった。しかしながら、本発明では、傾斜側面１０ａに露出されたｎ型コンタクト層１２の表面でｎ電極

をオーミック接触させることにより、ｎ型コンタクト層１２において光が導波する部分を無くし（図２において、Ｙ１の符号を付して模式的に示す）、従来の問題点を解決している。

また、発光した光を基板側から出射させる場合に、積層部１０の傾斜側面１０ａで反射した光も基板を介して出力することができ、出射効率を向上させることができる。

また、発光した光を基板側から出射させる場合に、傾斜側面１０ａで効果的に反射させるためには、傾斜側面１０ａには通常SiO_2保護膜が形成されていることを考慮すると、傾斜側面１０ａの傾斜角αを６０度以下に設定することが好ましく、４５度以下に設定することがより好ましい。

この傾斜角αは本明細書では、図２２に示すように定義し、その好ましい範囲は、臨界角θｃが$\sin\theta c = n_S / n_G$（n_G：活性層の屈折率、n_S：ＳｉＯ２保護膜の屈折率）で与えられることから、求めることができる。

例えば、波長３８０ｎｍの光を発光する素子の場合、波長３８０ｎｍの光に対する$Al_xGa_{1-x}N$の屈折率は、ｘの値が１～０の範囲であるとすると２．１５～２．８０である。この時、臨界角θｃが最も小さくなるのは、屈折率が２．８０の場合であり、この時の臨界角θｃは約３０°である。

従って、臨界角θｃを３０°以上、すなわち、傾斜角αを６０°以下に設定すると、少なくとも半導体層に平行に伝播される最も強い光は全反射されることになる。

以上のように傾斜角αを６０°以下に設定すると半導体層と平行に伝播される最も強い光は全反射されて取り出し効率を向上させることができる。しかしながら、層内を伝播される光には半導体層に平行でない光もあり、それらも効果的に全反射させるためには、傾斜角αを４５度以下に設定することがさらに好ましい。

また、傾斜側面１０ａにｎ電極を形成することを考慮した場合における、傾斜側面１０ａの傾斜長Ｌの上から見た投影長Ｗは、１０μｍ以上であることが好ましい。

以上の説明では、１つの隅部において、ｎ電極２１とｎ型コンタクト層１２と

がオーミック接触するように形成した例について説明したが、本実施の形態１では、図３及び図４に示すように、ｎ電極２２は積層部１０を囲むように形成することが好ましい。このようにすると、発光領域全体に均一に電流を注入することができ、効率良く発光させることができる。

実施の形態２（第２の発明）．

本発明に係る実施の形態２の窒化物半導体発光素子は、図５に示すように、発光領域を構成する積層部１１０の形状を円形にしたものである。本実施の形態２の窒化物半導体発光素子において、ｎ電極２３が積層部１１０の内側に傾斜した側面である傾斜面１１０ａに露出したｎ型コンタクト層１２とオーミック接触するように形成されている点は、実施の形態１と同様である。

また、実施の形態２の窒化物半導体発光素子において、積層部１１０の積層構造（半導体層の構成）は実施の形態１の発光素子と同様であり、積層部１１０を形成するためのエッチングは、サファイヤの表面が露出するまで行う。

実施の形態２において、ｐ側の電極は全面電極３３とｐパッド電極３４とからなり、全面電極３３は積層部１１０の最上層に位置するｐ型コンタクト層１６の円形表面のほぼ全面に形成され、ｐパッド電極３４は全面電極３３中央部に形成される。

ここで、全面電極３３、ｐパッド電極３４及び円形の積層部１１０は中心が一致するように同心円状に形成される。

以上のように構成された実施の形態２の窒化物半導体発光素子は、実施の形態１の発光素子と同様の作用効果を有する。

すなわち、ｎ電極２３による光の吸収を極めて少なくでき、効率良く光を出力できるとともに、積層部１１０の傾斜側面１１０ａで反射した光も基板を介して出力することができ、出射効率を向上させることができる。

さらに、本実施の形態２では、図５から明らかなように、ｎ電極２３は積層部１１０を囲むように形成しているので、発光領域全体に均一に電流を注入することができ、効率良く発光させることができる。

実施の形態３（第２の発明）．

本発明に係る実施の形態３の窒化物半導体発光素子は、図６、図７に示すよう

に、発光領域を構成する積層部１１０の形状を円形にしたものであるが、本実施の形態２の窒化物半導体発光素子とは、以下の点が異なる。

すなわち、実施の形態３の窒化物半導体発光素子では、ｐ型コンタクト層の表面に透光性を有する透光性オーミック電極３３ａを形成し、その上にｐパッド電極３４を形成している。

また、実施の形態３の窒化物半導体発光素子では、図７に示すように、傾斜側面１１０ａでｎ型コンタクト層とオーミック接触するｎ電極２４を基板１の側面及び裏面に連続して形成している。

この実施の形態３において、透光性オーミック電極３３ａとｎ電極２４以外は、実施の形態２と同様に構成される。

以上のように構成された実施の形態３の窒化物半導体発光素子は、積層部１１０で発光した光を透光性オーミック電極３３ａを介して出力することができ、以下のような効果を有する。

すなわち、ｎ電極２４による光の吸収を極めて少なくでき、効率良く光を出力でき、基板の側面及び裏面に形成されたｎ電極２４により光を反射して透光性オーミック電極３３ａを介して出力できるので、出射効率を向上させることができる。

また、本実施の形態３では、図６から明らかなように、ｎ電極２４を積層部１１０を囲むように形成しているので、発光領域全体に均一に電流を注入することができ、効率良く発光させることができる。

以上の実施の形態３の窒化物半導体発光素子では、ｎ電極２４により基板全体が覆われるように構成したが、本発明はこれに限られるものではなく、図８に示すように、ｎ電極２５と基板１を覆う電極２６とを別の金属で構成してもよい。

以上のように構成しても実施の形態３と同様の作用効果が得られ、さらに以下のような効果がある。

すなわち、ｎ電極２５はｎ型コンタクト層と良好なオーミック接触が得られる金属から選択して構成し、基板１を覆う電極２６には、その機能に応じて適切な金属材料を選択して構成することができる。

具体的には、基板１の裏面をはんだ付けにより実装する場合には、電極２６の

材料としてはんだ耐熱性の優れた材料を選択したり、光の反射を重視する場合には反射率の高い金属を選択して用いることができる。

実施の形態４（第２の発明）.

本発明に係る実施の形態４の窒化物半導体発光素子は、図９に示すように、発光領域を構成する積層部１１１の形状を矩形にしたものである。

すなわち、実施の形態３の窒化物半導体発光素子では、ｐ型コンタクト層の表面に全面電極３５を形成し、その上にｐパッド電極３６を形成している。

また、図９に示すように、矩形の積層部１１１の傾斜側面１１１ａでｎ型コンタクト層とオーミック接触するｎ電極２７を基板の表面とｎ型コンタクト層（傾斜側面１１１ａに露出したもの）とに亙って形成している。

尚、実施の形態４において、積層部の積層構造は実施の形態１～３と同様に構成される。

以上のように構成された実施の形態４の窒化物半導体発光素子は、実施の形態１～３と同様の作用効果を有する。

また、図９の窒化物半導体発光素子では、ｎ電極２７は積層部１１１の一辺でｎコンタクト層に接触するように形成したが、本実施の形態４では、図１０に示すように、積層部１１１の外周全体でｎコンタクト層とオーミック接触するようにｎ電極２８を形成することもでき、これにより、発光領域全体に均一に電流を注入することができ、効率良く発光させることができる。

実施の形態５（第２の発明）.

実施の形態５の窒化物半導体発光素子は、図１１，図１２に示すように、複数（図１１，１２では１８個）の積層部２１０を備えた発光面積の大きい発光素子であって、素子全体の面積に占める発光領域の面積を大きくでき、発光領域全体を均一に発光させることができるという特徴を有する。

図１１は主としてｎ電極２２１の形態を示すために、ｐ側ボンディング電極２５１及びｐ側接続電極２６１を省いて示す平面図であり、図１２はｐ側ボンディング電極２５１及びｐ側接続電極２６１を省略せずに示す平面図である。また、図１３は、図１２のＤ－Ｄ’線についての断面図である。

このように、発光領域を複数の部分に分割して形成するのは、大面積の発光領

域を分割することなく１つの大きな領域として形成した場合に生じる、電極から離れた部分で電流が低下して発光効率が悪くなるという問題を解決するためである。しかしながら、発光領域を複数の部分に分割して形成した場合には、各発光領域間を接続する電極面積が大きくなり、いかにして発光領域の面積を確保するかが課題となる。また、図２１に示す構造の従来の素子を複数個並べた場合には、ｎ型コンタクト層を光が導波して反射を繰り返すうちにｎ電極により吸収される光により発光効率が低下する。しかしながら、本実施の形態５の窒化物半導体発光素子では、第１に各積層部の傾斜した側面にｎ型コンタクト層とオーミック接触するｎ電極を形成することにより、ｎ電極が必要とする面積を小さくして発光領域の面積を確保し、かつｎ電極による光の吸収を防止している。

また、本実施の形態５の窒化物半導体発光素子では、ｐ側の全面電極による吸収も従来例に比較して抑えることができる。

すなわち、大面積の発光領域を分割することなく１つの大きな領域として形成した従来例では、図２３Ｂに示すように、臨界角以上でｐ側の全面電極に入射された光は、ｐ側の全面電極７３１と、基板１と半導体層との間の境界の間で反射を繰り返すうちに、かなりの部分がｐ側の全面電極により吸収される。

また、発光領域を複数の部分に分割して形成した場合であっても、分割された発光領域が傾斜した側面を有していない場合には、図２３Ｃに示すように、臨界角以上でｐ側の全面電極７３１に入射された光が基板に略垂直な側面から出射されて隣接する発光領域に再入射される確率が高くなる。そのためにｐ側の全面電極により吸収される率が高くなる。

これに対して、本実施の形態５の窒化物半導体発光素子は、各発光領域が傾斜側面を有しているので、基板側から発光させる場合には、図２３ＢにおいてＡ２の符号を付して示す光のように、また、電極側から発光させる場合には、図２３ＢにおいてＡ３の符号を付して示す光のように、隣接する発光領域に再入射されることなく（隣接する発光領域に再入射される確率を低くできる）、外部に出射される。これにより、ｐ側の全面電極３１で吸収される率を低くできる。

また、実施の形態５の窒化物半導体発光素子では、発光領域を構成する積層部２１０の形状を六角形とし、その複数の積層部２１０は積層部間の面積が最も小

さくなるように配列される（図１１，１２）。本実施の形態５において、隣接する積層部２１０間は基板の表面までエッチングされており（図１３）、複数の積層部２１０はそれぞれ完全に分離されている。尚、隣接する積層部２１０間の間隔は、例えば、１０μｍに設定される。

また、実施の形態５において、各積層部２１０の側面は、実施の形態１等と同様に全て傾斜面２１０ａであり、その傾斜面２１０ａに露出されたｎ型コンタクト層にオーミック接触するようにｎ電極２２１が形成される。

実施の形態５において、ｎ電極２２１は図１１に示すように全ての積層部２１０を取り囲むように一体として形成される。

実施の形態５において、各積層部２１０のｐ型コンタクト層のほぼ全面に全面電極２３１が形成され、その中央部にｐパッド電極２３２が形成される。そして、ｐパッド電極２３２上に開口部を有する絶縁膜２７１が素子全体を覆うように形成され、その絶縁膜２７１上にｐパッド電極２３２を互いに接続する接続電極２６１（一端がｐ側ボンディング部に接続）が形成される。尚、絶縁膜２７１はｎ電極２２１のうちボンディング部２４１を開口させる開口部も有している。

以上のように構成された実施の形態５の窒化物半導体発光素子は、発光領域である積層部２１０の形状を六角形とし、その積層部２１０間の面積が最も小さくなるように配列し、かつ各積層部２１０の傾斜した傾斜側面にｎ電極を形成することにより、発光領域の面積が大きくなるように構成している。

これにより、発光領域を効果的に発光させることができる適切な大きさの複数の部分に分割し、かつｎ電極を形成するために必要となる面積を抑制することが可能となる。従って、発光領域の面積を低下させることなく、かつ各発光領域を効率よく発光させることができ、高い輝度を有する大面積の発光素子を構成できる。

実施の形態５の窒化物半導体発光素子は、基板側から光を出射するようにしても良いし、全面電極２３１を透明電極とすることにより半導体側から光を出射するようにしても良い。いずれの場合についても、発光層で発光した光は基板側とｐ型半導体側の両方に伝播されるので、出射側とは反対側に反射膜を形成することが好ましく、これにより出射効率を向上させることができる。

図１４は、本実施の形態５の窒化物半導体発光素子において、接続電極２６１間を更に接続する第２接続電極２６２を形成したものである。この第２接続電極２６２はｐ側ボンディング部２５１から離れた位置にある積層部２１０における電流注入量が低下するのを防止するために形成するものであり、各積層部の発光強度を均一化するものである。

しかしながら、半導体層側から光を出射させる場合には、この第２接続電極２６２が光を遮ることになるので、本構成は基板側から光を出射する場合に特に適している。

図１５は、半導体層側から光を出射させる場合に適した接続電極の例を示すものである。本例では、ｐ側ボンディング部２５１に接続された第１接続電極２６３を積層部２１０の間のｎ電極上に絶縁膜を介してｎ電極と導通しないようにして形成する。この第１接続電極２６３は積層部上には形成されないので、積層部で発光した光を遮ることはない。そして、各積層部２１０のｐパッド電極と第１接続電極２６３の間は第２接続電極２６４により接続される。ここで、１つのｐパッド電極２３２と第１接続電極２６３の間は、１つの第２接続電極２６４で接続されている。

図１６Ａ～Ｂは、基板側から光を出射する場合の電極構造のより好ましい例を示したものである。

すなわち、図１６Ａの窒化物半導体発光素子では、実施の形態５（図１２）の接続電極２６１（ｐ側ボンディング部を含む）に替えて、絶縁膜２７１の上から複数の積層部を全て覆う電極層２６５を形成している。

このようにすると、各積層部の上面、特に傾斜側面からの光の漏れを防止でき（各積層部の上面及び傾斜側面で反射させることができ）、基板側から効率良く光を出射できる。また、図１６Ｂに示すように、そのような接続電極２６５を実装面側、実装基体１０３００側に設けることで、基板側で、正負電極が立体交差することがなく、複数の構造部２１０（１０）を同時に発光させることができ、その構造部周辺に、保護膜、反射膜、透過膜、光変換部材などを配置して、空間の有効利用がはかれて、さらに配線の立体交差によるリークの問題も解決されて、信頼性に優れる発光素子が得られる。

以上の実施の形態５の窒化物半導体発光素子では、各積層部２１０を六角形に形成した例により示したが、四角形又は円形等の他の形状であってもよい。

図２４は、積層部４１０を四角形にした具体例を示す平面図である。本例では、ｐ側ボンディング部４５１を２つの隅部に形成された積層部４１０上にそれぞれ設け、そのｐ側ボンディング部４５１に接続された接続電極４６１により、積層部４１０のｐパッド電極間が接続される。尚、接続電極４６１は、積層部４１０の間のｎ電極上に絶縁膜を介してｎ電極と導通しないようにして形成される。

また、ｎ電極４２１は、全ての積層部４１０を取り囲むように一体として形成し、各積層部４１０の傾斜面４１０ａに露出されたｎ型コンタクト層とオーミック接触するように形成され、その一部にｎパッド電極４４１が形成される。

また、図２４の変形例として、図３３Ａ～Ｂに示すように、実装基体（保護素子）１０３００上に、電極形成面側を実装面側として、フリップチップボンディングした形状とすることもできる。ここで図３３Ａでは、本来実装面側で基板に隠れる部分も実線で示している。この図では、上述した第１の発明における構造部の第１，２側面が形成されており、具体的には、構造部底面の角部の丸みの曲率半径が、上面側（ｐ型層表面よりも）の角部の曲率半径よりも小さくなっており、また、ｎ電極の形成外形もその形成部における構造部の角部曲率より大きな角部曲線が形成されている。また、複数ある構造部７１０（１０）の内、７１０ｘは、図３３Ｂに見るように、ｎ電極７２１（２１）が上部まで被覆されて、ボンディング１１４００ａにおいて、ボンディング面を提供している構造となっている。これにより、他の構造部のｐ電極と高さをそろえて、実装基板などに実装できる。また、この構造部７１０ｘは、素子として動作しない非動作部の構造物となる。

実施の形態６（第２の発明）.

図１７は実施の形態６の窒化物半導体発光素子の全体構成を示す平面図であり、図１８は１つの積層部３１０を拡大して示す平面図である。また、図１９Ａは図１８のＥ－Ｅ’線についての断面図であり、図１９Ｂは図１８のＦ－Ｆ’線についての断面図である。

実施の形態６の窒化物半導体発光素子において、積層部３１０はそれぞれ円形

形状に形成され、その中心が縦横とも１つの直線上に位置するように基板上に配列される。また、各積層部３１０の積層構造は他の実施の形態と同様であり、その外周側面は内側に傾いた傾斜面（外周傾斜面３１０ａ）とされ、その断面形状は、図１９Ａ～Ｂに示すように、上面を上底とする台形である。

各積層部３１０において、ｎオーミック電極３２１ａは外周傾斜面３１０ａに露出されたｎ側コンタクト層とオーミック接触するように外周傾斜面３１０ａの全周に形成される。また、積層部３１０の間の基板上にはそれぞれｎ接続パッド３２１ｂが形成され、各積層部３１０に形成されたｎオーミック電極３２１ａは隣接する４つのｎ接続パッド３２１ｂと接続される。

すなわち、実施の形態６の窒化物半導体発光素子において、ｎ電極３２１はｎオーミック電極３２１ａとｎ接続パッド３２１ｂとからなる。

また、各積層部３１０の上面（ｐコンタクト層の上面）のほぼ全面に、全面電極３３１が形成され、その全面電極３３１の中央部に円形のｐパッド電極３３２が形成される。

以上のように、ｎオーミック電極３２１ａ、ｎ接続パッド電極３２１ｂ、全面電極３３１及びｐパッド電極３３２を形成した後、接続パッド電極３２１ｂとその周辺及びｐパッド電極３３２の上面を除いて素子全体を覆う絶縁膜３７１を形成して、各積層部３１０のｐパッド電極３３２を互いに接続するｐ側接続電極３６１を形成する。尚、ｐ側接続電極３６１は、ｐパッド電極３３２上に接続されたパッド接続部３６１ｂとそのパッド接続部３６１ｂ間を接続する接続部３６１とからなる。

以上のように構成された実施の形態６の窒化物半導体発光素子は、実施の形態１と同様、電極による吸収を防止でき、発光した光の取り出し効率を高くできる。

実施の形態６の窒化物半導体発光素子における光の取り出し効率を確認するために以下の比較検討を行った。

まず、本実施の形態６の窒化物半導体発光素子として、図２５の平面図に示す積層部３１０を９個（３×３個）形成した素子を作製し、積層部３１０が１つの場合の発光素子（図２８の平面図に示す）と取り出し効率の比較を行った。

取り出し効率の測定は、図３０に示すように、マイナス側端子と一体で構成さ

れたカップ内に発光素子をダイボンディングし、ｎパッド電極とマイナス側端子Ｔ２とをボンディングワイヤーＷ２１で接続し、ｐパッド電極とプラス側端子Ｔ１とをボンディングワイヤーＷ３２で接続して、発光光量に対する外部に取り出される光量を測定した。

その結果、９個の積層部３１０を形成した実施の形態６の素子（図２５）の取り出し効率は、積層部３１０が１つの場合の発光素子（図２８）の取り出し効率を１００とした場合、８６％であった。

これに対して、比較例として作製した図２６に示す発光素子（９個の積層部を形成した素子）の取り出し効率は、図２９Ａに示す１つの積層部を備えた発光素子の取り出し効率を１００とした場合、７１％であった。

尚、積層部３１０が１つの場合の発光素子（図２８）の取り出し効率と、図２９Ａに示す１つの積層部を備えた発光素子の取り出し効率とはほぼ等しいものであった。

ここで、比較例の発光素子において、各積層部は実施の形態６と同様の積層構造を有し、その平面形状は略矩形に形成されている。また、ｎ電極５２１は、各積層部の１つの隅部において、ｎ型コンタクト層の表面を露出させ、その露出させた表面に形成されている。さらに、ｐオーミック電極５３１はｐ型コンタクト層のほぼ全面に形成され、ｐオーミック電極５３１上のｎ電極５２１と対角をなす位置にｐパッド電極５３２が形成されている。尚、図２６に示す素子では、隣接する積層部の間はサファイア基板が露出されるまでエッチングされて、隣接する積層部の間は完全に分離されている。また、各積層部の側面は、サファイア基板の上面に対してほぼ垂直に形成されている。

以上のように、複数の積層部を備えた実施の形態６の窒化物半導体発光素子は、同じく集合状態の比較例の窒化物半導体発光素子に比較して、取り出し効率を高くできることが確認された。

また、図２７は異なる比較例として作製した素子であって、図２６に示す比較例の発光素子において、隣接する積層部間においてサファイア基板が露出するまでエッチングせずに、ｎ型コンタクト層を残すようにしたものである。この図２７の比較例の素子の取り出し効率は、図２９Ｂに示す１つの積層部を備えた発光

素子の取り出し効率を１００とした場合、６８％であった。

尚、図２９Ａの素子の取り出し効率と、図２９Ｂの素子の取り出し効率とはほぼ等しいものであった。

以上のように、複数の積層部を備えた比較例の発光素子は、いずれも実施の形態６の発光素子より取り出し効率が悪いものであった。

また、実施の形態６の窒化物半導体発光素子は、実施の形態５の発光素子と同様の作用効果を有し、さらに以下のような特徴を有する。

すなわち、ウエハ上に各積層部を形成した後に、要求に応じて必要な個数の積層部３１０を含む任意の大きさの素子に分割することができるので、同一のパターンにより任意の大きさの素子を作製することが可能となる。

尚、この場合、いずれかの位置にあるｎ接続パッド電極３２１ｂとパッド接続部３６１ｂとをボンディング電極として用いることができる。

以上の各実施の形態の窒化物半導体発光素子は、上述したように、基板側から光を出力するようにも構成できるし、また、半導体側から光を出力するようにも構成できる。いずれの場合についても、光を出射する方向の反対側の面には、反射層を形成することが好ましい。図７、図８及び図１６Ａ～Ｂに示す構造の場合にはそれぞれ、ｎ電極２４、電極２６又は電極２６５を反射層として機能させることができることは上述した通りであるが、他の構成の場合には、反射層を別途設けることが好ましい。この反射層は、反射率の高い金属を用いて構成することもできるし、誘電体多層膜を用いて構成することもできる。誘電体多層膜を用いる場合には、例えば、図１３の絶縁層２７１を誘電体多層膜により構成することにより、絶縁機能に加え、反射機能を持たせるようにしても良い。

実施の形態７（第2の発明）.

図３１は実施の形態７の窒化物半導体発光素子の全体構成を示す平面図である。実施の形態７の窒化物半導体発光素子において、積層部３１０はそれぞれ円形形状に形成され、その中心が単位格子が六角形の格子点に位置するように基板上に配置される。また、各積層部６１０の積層構造は他の実施の形態と同様であり、その外周側面は内側に傾いた傾斜面とされている。

各積層部６１０において、ｎオーミック電極６２１ａは外周傾斜面に露出され

たｎ側コンタクト層とオーミック接触するように外周傾斜面の全周に形成される。また、６つの積層部６１０に囲まれた各六角形格子の中心には、それぞれｎ接続パッド６２１ｂが形成され、各積層部６１０に形成されたｎオーミック電極６２１ａは隣接する３つのｎ接続パッド６２１ｂと接続される。

すなわち、実施の形態７の窒化物半導体発光素子において、ｎ電極はｎオーミック電極６２１ａとｎ接続パッド６２１ｂとからなる。

また、各積層部６１０の上面（ｐコンタクト層の上面）のほぼ全面に、全面電極が形成され、その全面電極の中央部に円形のｐパッド電極６３２が形成され、各積層部６１０のｐパッド電極６３２はｐ側接続電極３６１により互いに接続される。

尚、ｎオーミック電極６２１ａ、ｎ接続パッド電極６２１ｂ等のｎ側の電極と、全面電極６３１、ｐパッド電極６３２、ｐ側接続電極３６１等のｐ側の電極とは実施の形態６と同様にして絶縁される。

以上のように構成された実施の形態７の窒化物半導体発光素子では、１つのｎ接続パッド電極６２１ｂに対して２つの積層部が設けらており、１つのｎ接続パッド電極に対して１つの積層部が設けられた実施の形態６に比較して、発光素子全体としての発光領域の面積を大きくできる。

また、この実施の形態７のように積層部を配置した場合、外形形状が、三角形、六角形、ひし形、平行四辺形等になるように分割することができ、そのように分割する際、ＧａＮ結晶の結晶軸の方向とスクライブラインの方向を一致させることができるので、分割時の歩留まりを向上させることができる。

次に、上記各実施の形態の窒化物半導体発光素子において、傾斜側面を有する積層部の形成方法の一例を示す。

本方法では、まず、サファイア基板１の上に、バッファ層１１、ｎ型コンタクト層１２、ｎ型クラッド層１３、発光層１４、ｐ型クラッド層１５及びｐ型コンタクト層１６を順次成長させて積層構造を形成し、その上に、図２０Ａに示すように、断面が台形形状のマスクＭ１を形成する。

次に、反応性イオンエッチングにより、マスクＭ１の上から積層体をエッチングする。この時、積層体をエッチングすると同時にマスクそのものもエッチング

により少しづつ除去する。図２０Ｂにおいて、破線と実線の間のＲ１の符号を付した部分が除去された部分である。

このエッチングを積層部１０の周りの基板表面が露出されるまで続ける（図２０Ｃ）。

このようにすると、マスクＭ１の形状に対応した形状の、傾斜側面１０ａを有する積層部１０が形成される。

本方法では、マスク材料と窒化物半導体材料のＲＩＥによるエッチング率を考慮して、マスクＭ１形状を設定することにより、所望の傾斜側面を有する積層部が形成できる。

例えば、マスクＭ１の側面を外側に膨らんだ形状とすることにより、積層部の傾斜側面を外側に膨らんだ凸曲面とすることができる。

このように、傾斜側面を外側に膨らんだ凸曲面とすることにより、基板側から光を出力する場合に集光して光を出射できる。

以上の各実施の形態では、最も好ましい例として、積層部の周りを基板までエッチングした例を用いて説明したが、本発明においては積層部の周りに光が伝送されないようにすることが重要であり、光の伝送を抑制できる程度の厚さにｎ型半導体層が残っていても良い。

（第３の発明）

以下、図面を参照しながら本発明に係る実施の形態について説明する。

実施の形態８（第３の発明）.

本発明に係る実施の形態１の窒化物半導体発光素子は、図３４に示すように、発光領域を構成する窒化物半導体層の一部が金属部材７に埋め込まれるように設けられ、その金属部材７によって、発光素子全体の形状が保持されている。

本実施の形態８の窒化物半導体発光素子においては、ｎ型窒化物半導体層２とｐ型窒化物半導体層３の間に発光層４を設けることによりダブルヘテロ構造の発光領域が構成されており、そのｐ型窒化物半導体層と発光層とｎ型窒化物半導体層の一部は台形錐形状（裁頭錐体形状）に加工されている。すなわち、本発明は、少なくともｐ型窒化物半導体層と発光層が含まれるように台形錐形状の積層体が形成される。また、積層体１０において、ｐ型窒化物半導体層３上のほぼ全面に

はｐ型オーミック電極３６が形成され、ｐ型オーミック電極３６の周辺部と積層体１０の傾斜した側面１０ａ及びその側面１０ａに連続したｎ型窒化物半導体層２を覆うように絶縁層７２（５）が形成されている。

そして、以上のように構成された積層体１０が金属部材７に埋め込まれるようにして保持されている。尚、積層体１０の側面は、絶縁層７２を介して金属部材７に埋め込まれ、積層体１０のｐ型オーミック電極３６が形成された面はｐ型オーミック電極３６を介して金属部材７に対向している。また、ｎ型窒化物半導体層２の対向する２つの面のうちの積層体１０の反対側に位置する面には透明電極２１が形成され、その透明電極２１の一部にはｎパッド電極２９が形成されている。

以上のように構成された実施の形態８の窒化物半導体発光素子において、積層体１０の発光層４で発光された光は、金属部材７の反対側から透明電極２１を介して出射される。

次に、本実施の形態８の窒化物半導体発光素子の製造方法について説明する。

本製造方法ではまず、図３５に示すように、サファイア基板１の上に例えばバッファ層（図示せず）を介してｎ型窒化物半導体層２、発光層４及びｐ型窒化物半導体層３をその順番に成長させる。

次に、素子間において、ｎ型窒化物半導体層が露出するまでエッチングすることにより、台形錐形状の積層体１０を形成する（図３６）。

この台形錐形状の積層体１０は、例えば、マスクを所定の台形錐形状に形成しておいて、そのマスクを用いてエッチングすることによりそのマスクの形状に対応した台形錐形状に加工できる。

具体的には、まず、図４４Ａに示すように、ｐ型窒化物半導体層３上に、断面が台形形状のマスクＭ１を形成する。このマスクＭ１は反応性イオンエッチングにより一定のレートでエッチング可能な材料を用いて形成する。

次に、反応性イオンエッチングにより、マスクＭ１の上からサファイア基板１上に形成された半導体層（ｐ型窒化物半導体層３、発光層４及びｎ型窒化物半導体層２）エッチングする。このエッチング工程においては、半導体層とともにマスクＭ１そのものもエッチングにより少しづつ除去される。尚、図４４Ｂにおい

て、破線と実線の間のＲ１の符号を付した部分が除去された部分である。

このエッチングを積層部１０の周りにｎ型窒化物半導体層２の表面が露出されるまで続ける（図４４Ｃ）。

このようにすると、マスクＭ１の形状に対応した台形錐形状の積層部１０が形成される。

本方法では、マスク材料と窒化物半導体材料のＲＩＥによるエッチング率を考慮して、マスクＭ１形状を設定することにより、所望の台形錐形状の積層部１０を形成できる。

上述の方法により積層体１０を加工するエッチング手段としては、反応性イオンエッチングの他、反応性イオンビームエッチング、イオンミリング等のドライエッチングを用いることができる。

また、台形錐形状の積層部１０の加工は、例えばウェットエッチングなどの等方性エッチング手段を用いて、アンダーカッティング（サイドエッチング）現象を利用するようにしてもよい。このアンダーカッティングを利用すると、台形錐形状の加工を簡単にできるが、加工精度は上述したドライエッチングを使用した方法に比較して劣る。

また、積層体１０の傾斜した側面１０ａの傾斜角（サファイア基板１の主面との為す角度）は、ｎ型窒化物半導体層を介して出力される光の取り出し効率を高くするために、３０度～８０度の範囲に設定されることが好ましくより好ましくは４５度に設定する。

また、本発明において、裁頭錐体は、円錐台形錐体、角錐（四角錐、六角錐他）台形錐体等、種々の台形錐体が適用できる。

以上のようにして、台形錐形状の積層部１０を形成した後、積層部１０の上底面（ｐ型窒化物半導体層３の表面）のほぼ全面にｐ型オーミック電極３６を形成する。

ここで、本明細書において、上底面とは、台形錐形状における互いに平行に対向する２つの面のうちの小さい方の面のことを言い、積層体２の底面という場合は、対向する２つの面のうちの大きい方の面のことを言う。

ｐ型オーミック電極３６は、Ｎｉ／Ａｕ、Ｎｉ／Ｐｔ、Ｐｄ／Ｐｔからなる電

極を用いることもできるが、本発明では、Ｒｈ／Ａｕ、Ｒｈ／Ｐｔ等のように、Ｒｈ層をｐ型窒化物半導体層３に接する層として形成した電極を用いることが好ましい。このように、Ｒｈをｐ型窒化物半導体層３に接する第１層として形成すると、金属部材７を形成した後に、ｐ型オーミック電極３６がｐ型窒化物半導体層３から剥離するのを防止できる。

尚、（／）で表記した組み合わせは、（／）の前に記載した金属をｐ型窒化物半導体層３に接する第１層として形成し、その第１層の上に形成した第２層を（／）の後ろに記載した金属で形成したことを意味している。

各積層体１０のｐ型窒化物半導体層上にｐ型オーミック電極３６を形成した後、図３８に示すように、各ｐ型オーミック電極３６の中央部（周辺部を除いた部分をいう。）を除いて基板上全体を覆うように、絶縁膜７２（５）を形成する。

この絶縁膜７２，７３，５は、例えば、SiO_2、TiO_2、Al_2O_3、Si_3N_4、ZrO_2等の無機絶縁膜を用いて好適に形成することができるが、有機絶縁膜を用いて形成してもよい。

その後、必要に応じて複数の積層部１０の間を接続する配線電極６５を形成する（図３９）。

次に、反射層６５（６）を形成する。この反射層６はＡｇ、Ｐｔ、Ｒｈ、Ａｌ等の光反射性の高い材料を用いて形成される。尚、複数の積層部により１つの発光素子を構成する場合には、この反射層６が配線用の電極を兼ねるようにしても良い。特に、台形錐形状の積層体の側面が傾斜しており、これに対向するように反射層が設けられているので、光の利用効率が飛躍的に向上する。

尚、本発明では、絶縁膜５（７２，７３）が反射層を兼ねるようにしてもよい。

反射層として用いることができる絶縁膜５の具体的な材料としては、SiO_2、TiO_2、Al_2O_3、Ta_2O_5、ZrO_2、Nb_2O_5、Y_2O_3が挙げられ、より好ましくは、これらの材料のなかから、２つの屈折率の異なる材料を組み合わせて交互に形成することにより多層構造の反射層を兼ねた絶縁膜５を形成する。例えば、TiO_2／SiO_2、を組み合わせて１０～２０層積層することにより、多層構造の反射層を形成する。

次に、例えば、メッキ等により金属部材７を全面に形成する（図４０）。本発

明において、この金属部材７は、後の工程でサファイア基板１を除去した後に発光素子の形状を保持することを第一義的な目的とするものであり、そのために厚く（好ましくは、５０μｍ以上、より好ましくは、１００～２００μｍの範囲）形成する必要がある。

本発明において、金属部材７は、第１にこの目的を果たすことができればよく、そのためには、例えば、Ｔｉ、Ａｇ、Ａｌ、Ｎｉ、Ｐｔ、Ａｕ、Ｒｈ、Ｃｕ、Ｗ等の種々の金属を用いることができる。

また、本実施の形態８において、金属部材７は、反射膜６との密着性のよいことが要求される。また、反射膜６が形成されていない場合は、金属部材７は、絶縁膜５（７３）とｐ型オーミック電極３６、とりわけ絶縁膜５（７３）との密着性が良いことが要求される。その場合、上述した材料により構成される絶縁膜５（７３）との密着性の良い材料として、Ｔｉ、Ｗ、Ａｌ、Ｎｉが挙げられる。

また、金属部材７そのものを反射率の高い材料で形成することにより、反射層６を省略するようにしてもよい。そのような金属材料として、Ａｇ、Ａｌ、Ｐｔ、Ｒｈが挙げられる。

また、本発明では、発光素子の形状を保持するという第一義的な機能のほか、光反射機能等を果たすために、金属部材７は、それぞれの機能を有する複数の層を積層した多層構造としてもよい。例えば、下地層として、発光した光に対する反射率が高くかつ絶縁膜５、ｐ型オーミック電極３６などとの密着性が良い第１金属膜を形成し、その上に厚く形成することが可能な第２金属膜を形成するようにして、金属部材７を構成することができる。

また、本発明では、金属部材７は、比較的厚く形成する必要があるので、成膜速度の速い無電解メッキ、や電気メッキを用いて形成することが好ましい。

具体的には、Ｎｉ、Ｃｕ、Ａｌ、Ａｕ等の電気メッキ、Ｎｉ、Ｃｕ等の無電解メッキを用いることができる。

特に、無電解Ｎｉメッキは、Ａｕ、Ｃｕ、Ａｇに比較して強度が高いためにウエハの反りを小さくできかつ電気接点が不用な点で好ましく、さらにＮｉはメッキ層の均一性、析出速度、ハンダ濡れ性、バンプ強度、耐食性の点においても優れた材料である。

次に、図４１に示すように、基板１の側からレーザを照射することによりサファイア基板１を除去する。この段階では、比較的厚い金属部材７が形成されているので、基板１を除去する方法としては、レーザ照射の他、研磨やエッチング等の種々の方法を用いることができる。

そして、基板１が除去されて露出したｎ型窒化物半導体層２の表面に透明電極であるｎ型電極２１（８）を形成する（図４２）。このｎ型電極２１（８）はＷ／Ａｌ、Ｖ／Ａｌ、Ｗ／Ｐｔ／Ａｕ、ＺｎＯ、ＩＴＯ、Ｍｏ等により形成することができる。光の取り出し効率を高くするためには、ＺｎＯやＩＴＯを用いることが好ましく、安価で入手しやすい材料であるという点で、ＩＴＯを用いることがさらに好ましい。

このＩＴＯを用いて透明電極２１（８）を形成する場合、抵抗値を下げるため、熱処理を施すことが好ましく、その好ましい熱処理温度は、１００℃～５００℃であり、より好ましい熱処理温度は、２００℃～４００℃である。

次に、各積層体１０に対応してそれぞれｎパッド電極２９を形成し、そのｎパッド電極２９の周辺部と透明電極２１（８）とを覆う絶縁膜７２（５）を形成する。

そして、ウエハを積層部の間で分割することにより個々の発光素子とする。

ここで、本発明では、個々の素子に分割する際の分割位置は、少なくとも積層体１０の傾斜側面１０ａから離れた位置とし、その傾斜側面１０ａと分割後の素子の側面とが離れるようにする。

以上のように構成された本発明に係る実施の形態８の窒化物半導体発光素子は、素子に分割する際の分割位置が積層体１０の傾斜側面１０ａから離れているので、積層体１０の傾斜側面１０ａのＰＮ接合面が損傷を受けることがない。

また、素子に分割する際の分割位置が積層体１０の傾斜側面１０ａから離れているので、金属部材７を切断する際の切断屑によるＰＮ接合面の短絡を防止できる。

また、本発明に係る実施の形態８の窒化物半導体発光素子では、積層体１０の両側に電極を形成しているので、同一面側に電極を形成した素子のように一方の電極を形成するために発光層の一部を除去する必要はない。これにより、発光層

の面積を小さくすることなく発光領域を確保できるので、発光効率を向上させることができる。

また、本発明に係る実施の形態８の窒化物半導体発光素子では、積層体１０の両側に電極を形成しているので、容易に発光層全体に電流を均一に流すことができ、発光層全体を均一にかつ効率よく発光させることができる。

特に、複数の積層部により１つの発光素子を構成するようにした場合には、比較的広い面積において、発光面内における均一性に優れた発光素子を提供できる。

また、本実施の形態８の窒化物半導体発光素子においては、ｎ型窒化物半導体層のほぼ全面に透明電極２１（８）を形成しているので、発光層全体に均一に電流を他注入することができ、発光層全体を均一に発光させることができる。

しかしながら、本発明はこれに限られるものではなく、透明電極２１（８）に代えてｎ型窒化物半導体層のほぼ全面に網目状（格子状）のｎ型電極を形成し、その格子の間から光を出力するようにしても良いし、ｎ型窒化物半導体層の一部にｎ型電極を形成するようにしてもよい。

ｎ型窒化物半導体はｐ型窒化物半導体に比較して抵抗値を小さくできることからｎ型窒化物半導体層内を電流が拡散しやすく、格子状のｎ型電極を用いた場合であっても、格子（電極が形成されていない部分の面積）を大きくでき、電極により光をあまり遮ることなく出射できる。また、ｎ型窒化物半導体層の一部にｎ型電極を形成するようにした場合であっても、比較的広範囲の発光層に電流を注入することが可能である。

変形例（第３の発明：第８の実施形態変形例）．

以上の実施の形態８では、ｎ型窒化物半導体層２を厚さ方向に途中までエッチングすることにより、上記積層体を上記ｎ型窒化物半導体層の少なくとも一部を含むように構成した。しかしながら、本発明はこれに限られるものではなく、図４５に示すように、ｐ型窒化物半導体層３と発光層４のみをエッチングするようにして積層部８１０－１を形成するようにしても良いし、図４６に示すように、ｐ型窒化物半導体層３と発光層４をエッチングした後さらに連続してｎ型窒化物半導体層２をサファイア基板が露出するまでエッチングすることにより、ｐ型窒化物半導体層３、発光層４及びｎ型窒化物半導体層２により積層部８１０－２を

形成するようにしてもよい。

実施の形態９（第３の発明）.

本発明に係る実施の形態９の窒化物半導体発光素子は、図４７に示すように、１つ例に４つの積層体８１０－３を配列した発光素子である。

すなわち、本実施の形態９の窒化物半導体発光素子は、図５０に示すように、縦横４つずつ、合計１６個の四角錐台形状の積層体８１０－３（ｐ型窒化物半導体層と発光層により構成）をｎ型窒化物半導体層２の一方の面に配列して比較的大面積の発光素子を構成している。

また、本実施の形態９の窒化物半導体発光素子において、ｎ型窒化物半導体層２の他方の面の全面には、全ての積層体８１０に共通の透明電極２１（８）がｎ型オーミック電極として形成され、その中央部に１つのｎパッド電極２３が形成されている。

また、本実施の形態９の窒化物半導体発光素子は、１６個の積層体８１０で１つの発光素子を構成するように、かつ分割位置が少なくとも積層体１０（８１０）の傾斜側面１０ａから離れた位置となるように積層部の間において分割されている。

以上のように構成された実施の形態９の窒化物半導体発光素子は、素子に分割する際の分割位置が積層体１０の傾斜側面１０ａから離れているので、積層体１０の傾斜側面１０ａのＰＮ接合面が損傷を受けることがなく、かつ金属部材７を切断する際の切断屑によるＰＮ接合面の短絡も防止できる。

また、本発明に係る実施の形態９の窒化物半導体発光素子では、実施の形態８の窒化物半導体発光素子と同様の理由で、発光効率を向上させることができ、発光層全体を均一にかつ効率よく発光させることができる。

以上の実施の形態９の窒化物半導体発光素子では、ｎ型窒化物半導体層２を含まずに、ｐ型窒化物半導体層３と発光層４とが積層された積層体８１０を用いて発光素子を構成した。しかしながら、本発明はこれに限られるものではなく、図４８に示すように、ｎ型窒化物半導体層２とｐ型窒化物半導体層３と発光層４とが積層された積層体８１０－４を用いて構成してもよい。

以上の実施の形態９の窒化物半導体発光素子では、１つの発光素子内では積層

体ごとに分離することなく、発光素子間においてｎ型窒化物半導体層２が分離されるようにウエハ上に形成した後、ｎ型窒化物半導体層２が分離された部分で素子ごとに分割するようにしてもよい（図４９）。

また、実施の形態９の窒化物半導体発光素子は、四角錐台形状の積層体８１０を用いて構成したが、本発明はこれに限られるものではなく、円錐台形状の積層体８１０－４を用いて構成するようにしてもよい（図５１）。

（本発明におけるその他の構成）

（本発明の発光素子１００00）

以上説明した各実施形態において、その実施形態（発光素子１００00）の各構成について以下に詳しく、説明するが、本発明は上記実施形態及びその構成について組み合わせて適用することもできる。

（素子構造体１０１00）

本発明の発光素子１００00に用いられる素子構造体１０１00は、図５９Ａ～Ｂの断面図などに示すように、基板１上に、第１導電型層２、活性層（発光層４）、第２導電型層３が順に積層された積層構造体１０１00でもよく、第１，２導電型層２，３が横方向に接合されていてもよく、これらを組み合わせたもの、例えば断面が折れ線（連続直線）状、山形、谷形などの様々な面が複合された接合面、でもよい。

具体的には、本発明の発光素子１００00は、素子構造体１０１00として、図５９Ａ～Ｂに示すように、素子構造体１０１00は、基板１上に、第１導電型層２、発光層（活性層）３、第２導電型層３が順に積層された積層構造１０１00を有するものであり、このとき、電極形成面内において、発光構造部５１１０は、図に示すように積層方向に第１，２導電型層が発光層を挟む構造の他、上述したとおり、第１，２導電型層が横方向に接合されていてもよく、またこれらを組み合わせた縦、横の複雑な複合接合面を形成したものでもよい。また、発光素子構造として、ＭＩＳ構造、ｐ－ｎ接合構造、ホモ接合構造、ヘテロ接合構造（ダブルヘテロ構造）、ＰＩＮ構造などを用いることができ、またユニポーラ素子にも適用できるが、好ましくは、第１，２導電型層が互いに異なる導電型層となるｐ－ｎ接合構造などのｎ型、ｐ型層で活性層を挟む構造を用いることが好ましい。

素子構造体１００００を構成する積層構造の半導体材料は、ＩｎＡｌＧａＰ系材料、ＩｎＰ系材料、ＡｌＧａＡｓ系材料、これらの混晶材料でもよく、ＧａＮ系窒化物半導体材料でもよい。ＧａＮ系窒化物半導体材料として具体的には、ＧａＮ、ＡｌＮ、もしくはＩｎＮ、又はこれらの混晶であるＩＩＩ－Ｖ族窒化物半導体（$In_{\alpha}Al_{\beta}Ga_{1-\alpha-\beta}N$、$0 \leqq \alpha$、$0 \leqq \beta$、$\alpha+\beta \leqq 1$）で表され、またこれに加えて、ＩＩＩ族元素として一部若しくは全部にＢを用いたり、Ｖ族元素としてＮの一部をＰ、Ａｓ、Ｓｂで置換したりした混晶でもよい。以下、窒化物半導体を用いて説明するが、他の材料系にも適用される。

発光層としては、ＩｎＧａＮ系材料を用いることができ、ワイドバンドギャップの発光層により、緑色、青色の可視光域から紫色、それより短波長の紫外域に発光するものが得られる。

各実施形態では、第１，２導電型層２，３を、ｎ型層、ｐ型層としているが、この逆でも良い。また、半導体積層構造１０１００の成長方法として具体的にはＭＯＶＰＥ（有機金属気相成長法）、ＨＶＰＥ（ハライド気相成長法）、ＭＢＥ（分子線エピタキシー法）、ＭＯＣＶＤ（有機金属化学気相成長法）があり、好ましくはＭＯＣＶＤ，ＭＢＥである。

本発明の半導体積層構造１０１００の成長方法に用いる基板、特にエピタキシャル成長用の基板１としては、窒化物半導体と異なる材料の異種基板として、例えば、Ｃ面、Ｒ面、及びＡ面のいずれかを主面とするサファイア、スピネル（$MgAl_2O_4$）のような絶縁性基板、ＳｉＣ（６Ｈ、４Ｈ、３Ｃを含む）、ＺｎＳ、ＺｎＯ、ＧａＡｓ、Ｓｉ、及び窒化物半導体と格子整合する酸化物基板等、窒化物半導体を成長させることが可能で従来から知られており、窒化物半導体と異なる基板材料を用いることができ、好ましくはサファイア、スピネルであり、また異種基板以外として、ＧａＮ、ＡｌＮなどの窒化物半導体基板なども用いることができる。他の半導体材料においては従来知られた同じ材料系の基板、若しくはＳｉなどの異種基板を用いることができる。

（半導体積層構造１０１００）

発光素子１００００を形成する半導体積層構造１０１００としては、例えば図５７Ａ～Ｄ，図３９，図５９Ａ～Ｂに示すように、上記基板１上に下地層５００な

どを介して成長され、このとき、下地層５００を素子構造１０１００として動作部に含めても良いが、通常素子構造の成長用のみ形成されて素子として機能しない非動作部として設けられる。下地層は、特に異種基板を用いた場合、結晶核形成、核成長層として、低温成長バッファ層を用い、好適な条件は$Al_xGa_{1-x}N$（$0 \leqq x \leqq 1$）を低温（２００～９００℃）で成長させるものであり、続いて高温で層成長させて、膜厚５０Å～０．１μｍ程度（単結晶、高温成長層）で形成する。また、ＥＬＯ(Epitaxial Lateral Overgrowth)として知られるように、基板上、若しくは下地層上に、島状部（凸部、マスク開口部）などの成長部を他の領域に比べて優先的、若しくは選択的に成長させて、各選択成長部が横方向に成長して接合、会合することで層を形成するような成長層を下地層５００若しくは、素子積層構造１０１００に用いることもでき、これにより結晶性、特に結晶欠陥を低減させた素子構造とできる。

窒化物半導体に用いるドーパントとして、ｎ型不純物としては、Ｓｉ、Ｇｅ、Ｓｎ、Ｓ、Ｏ、Ｔｉ、Ｚｒ等のＩＶ族、若しくはＶＩ族元素を用いることができ、好ましくはＳｉ、Ｇｅ、Ｓｎを、さらに最も好ましくはＳｉを用いる。また、ｐ型不純物としては、特に限定されないが、Ｂｅ、Ｚｎ、Ｍｎ、Ｃｒ、Ｍｇ、Ｃａなどが挙げられ、好ましくはＭｇが用いられる。これら、アクセプター、ドナーの各ドーパントを添加することにより、各導電型の窒化物半導体層を形成し、後述する各導電型層を構成する。また、窒化物半導体は不純物をドープしない無添加層であってもｎ型層として用いることができ、さらにＡｌＧａＡｓなどの他の材料系にはそれに適したドーパント用いる。本発明における第１導電型層、第２導電型層には、部分的にアンドープの層、半絶縁性の層が積層されていても良く、電流阻止層のよう逆導電型の埋込層に、各導電型層内に部分的に寄生な素子部分を形成していても良い。

（第１導電型層２）

上記実施形態の素子構造で示すように、第１導電型層２として、各導電型のドーパントを含有させ、電極形成面内及び活性層へのキャリアの供給、拡散を実現するような層構造を形成すると良く、特に電極形成部５２００から発光構造部５１１０にキャリアを面内に拡散して供給する電流拡散導体８（コンタクト層）に

は、他の領域より高濃度にドープされることが好ましい。また、このような電荷供給・面内拡散層（コンタクト層及びその近傍層）の他に、上記実施形態で示すように、積層方向において発光層へ電荷を移動・供給させる介在層、若しくは第２導電型のキャリアを発光層に閉じこめるクラッド層などを、コンタクト層とは別に設けることが好ましい。このような発光層４と面内拡散層（領域）のコンタクト層との間に設ける層として、窒化物半導体素子の場合には、面内拡散層（領域）より低濃度ドーパント量若しくはアンドープの低不純物濃度層（アンドープ層）、及び／又は多層膜層を設けることが好ましい。これは、低不純物層でもって、高不純物層（面内拡散層）による結晶性悪化を回復させてその上に成長させるクラッド層、発光層の結晶性を良好にし、駆動時にあっては高濃度層に隣接して低濃度層が設けられることで面内拡散を促進させ、また、耐圧性も向上させることができる。多層膜層は、少なくとも２種の層を交互に積層させたような周期構造で形成すること、具体的には、Ｉｎを含む窒化物半導体層とそれとは異なる組成の層の周期構造、好ましくは$In_xGa_{1-x}N$／$In_yGa_{1-y}N$（$0 \leqq x < y < 1$）で構成することで、発光層、特にＩｎを含む窒化物半導体層、好ましくはそれを井戸層として複数用いた場合において、その結晶性を向上させることができる。このような多層膜としては、組成が異なる層による周期構造の他、組成傾斜構造、また、これらの構造において不純物濃度を変調させた構造、膜厚を変動させた構造なども採用でき、好ましくは、２０ｎｍ以下の膜厚の層を積層した構造、さらに好ましくは１０ｎｍ以下の膜厚の層を積層した構造で形成することが、上記結晶性に有利となる。

（発光層［活性層］３）

本発明の素子構造１０１００としては、第１，２導電型層との間に、発光層を設けて、発光層で発光させる素子構造とすることが好ましく、特に窒化物半導体においてはＩｎを含む窒化物半導体を発光層に用いたものが、紫外域から可視光（赤色光）の領域において好適な発光効率が得られ好ましく、特にＩｎＧａＮ層を用いること、特にＩｎの混晶比を変化させて所望の発光波長を得ることが好ましい。このほかの窒化物半導体材料として、ＧａＮ，ＡｌＧａＮなどのＩｎＧａ

Ｎよりも高バンドギャップの材料を用いて、紫外域において使用する発光素子としても良い。

さらに好ましい発光層としては、量子井戸構造の活性層を用いることであり、井戸層が１つの単一量子井戸構造、さらに好ましくは、複数の井戸層が障壁層を介して積層した構造の多重量子井戸構造を採用することが好ましい。井戸層については上記発光層と同様に、好ましくはＩｎＧａＮ層を用いることであり、障壁層として、井戸層よりバンドギャップエネルギーが大きくなるような層として、例えばＩｎＧａＮ、ＧａＮ、ＡｌＧａＮを設けることが好ましい。このとき、井戸層、障壁層の膜厚としては、３０ｎｍ以下、好ましくは２０ｎｍ以下、さらに井戸層において好ましくは１０ｎｍ以下とすることで、量子効率に優れた発光層が得られる。また、井戸層、障壁層に、各導電型層のドーパントがドープされていても良く、障壁層は、井戸層間に一層以上設けても良い。

（第２導電型層３）

第２導電型層３としては、キャリアを発光層に閉じこめるクラッド層、電極が形成されるコンタクト層を、設けることが好ましく、この時両層を別々に設けてコンタクト層をクラッド層よりも発光層より遠くに設け、高濃度にドーパントをドープすることが好ましい。窒化物半導体においては、クラッド層として好ましくはＡｌを含む窒化物半導体、さらに好ましくはＡｌＧａＮ層を用いることが好ましく、さらに発光層に近接して、好ましくは接して形成されることで発光層の効率を高めることができ好ましい。さらに、コンタクト層とクラッド層との間にそれらの層より低不純物濃度の層を介在させることで、耐圧性に優れた素子とでき、またコンタクト層を高濃度にドープしても結晶性を改善できるため好ましい。コンタクト層は、図５８に示すように、電極形成面内で発光部５１１０として設けられるため、その面内でキャリアを拡散させる層としても機能しうるが、本発明では、電極２０００を設けて、該面内の一部に延伸する上部電極２２００と、それよりも面積の大きな、断面幅広な層状の下部電極２１００により面内での電流拡散導層、拡散導体として機能させることで、窒化物半導体における低い移動度のｐ型キャリアの拡散を補助し、また、コンタクト層の膜厚を他の層（クラッド層、介在低濃度層）よりも小さくして、且つ他の層よりも高濃度に不純物ドープ

することで、高キャリア濃度の層を形成して、電極から良好な電荷注入を実現でき好ましい。

（電流拡散導体８，９）

このように本発明の積層構造１０００１００において、電流拡散導体８は、素子構造体内（第１導電型層内８）に設けられても、素子構造体上（の電極２１００）に設けられる形態でもよい。具体的には、図５８などに示すように、第１導電型層２においては、露出電極形成面５２００に第１の電極１０００が設けられ、該第１電極１０００が設けられた第１導電型層２内を横方向に電流拡散する拡散導体８として機能し、他方、第２導電型層３側には、接続電極（配線電極、配線部）に電気的に接合するオーミック接触用の電極２１００でもって、面内において、一部に設けられた配線電極から、電流を面内に広く拡散させる拡散導体として機能する。第２導電型層３内に拡散層を設けても良く、第１導電型層上に、外部（電極）の拡散導体を設けても良い。

（発光素子面内構造）

本発明の発光素子には、素子構造部５７００に発光構造部５１１０と電極形成部５２００が設けられた構造であり、素子構造部５７００は電流拡散導体８（第１導電型層２）上に形成され、１つの素子構造部５７００内で１つの発光構造部５１１０（図１～１０，３４，４５，４６）とする形態でも良く、１つの素子構造部５７００内で複数の発光構造部５１１０が形成されるような発光構造部５１１０の集積構造を形成しても良く、１つの素子構造５７００に対して少なくとも１対の発光構造部５１１０と電極形成部５２００が形成されれば良く、さらに、素子構造部５７００を複数集積して集積型の発光素子１００００とすることもできる。

各電極の配線形態としては、各電極は素子構造体内に電流供給できるように、オーミック接触されたオーミック接触部を有することが好ましく、該オーミック接触部に一致して電極（配線電極、台座部）が形成されていることが好ましい。他の形態としては、離間して配置されたオーミック接触部に対して、それらを導通するように、配線用として電極が設けられてもよい。また、このような配線用電極は、後述する素子実装基体側に設けられてもよい。

このように素子構造体の電極形成位置は、各導電型層に設けられた電極形成面

の上に設けられ、上記素子構造体の形状・形態に依存するため、図に示すような第２導電型層、発光層を一部除去して露出させた第１導電型層を電極形成面として、基板上において、発光層の上方、下方にそれぞれ第２電極、第１電極の形成面が設けられる形態がある。その他に同一面側に両方の電極を形成すれば、他の電極形成面の形態もとりうる。

（第１電極１０００）

また、第１電極１０００は、第１導電型層２の露出部２ｓの少なくとも一部に電極形成領域５２００として形成され、第２の発明では発光構造部５１１０と面内で分離されて設けられ、オーミック接触用として第１導電型層２内に電流注入する。第１導電型層２の露出部２ｓは、図に示すように、発光構造部５１１０を囲むように素子構造部１０１００の端部に設けられていても良く、図５８などに示すように基板１を素子端部で露出（露出部４ｓ）させて、第１導電型層２の側面６１１０ａを傾斜させて、光反射部、取出し部として機能させることができ、この場合、発光構造部５１１０の側面５１１０ａよりも、傾斜側面における電極形成面、基板面の法線方向に対する角度を、大きくすることで、第１導電型層２内を横方向に伝搬する光を効率的に取出すことができ好ましい。また、露出部２ｓは、素子動作部５７内において、発光構造部５１１０に対して、第１電極１０００から露出させて設けること（５１１０ａ）で、光取り出し溝として機能させることもでき、またそのような電極１０００から露出された領域において凸部、例えば、電流注入されない非発光構造部（電極形成部５２００など、又は素子非動作部５８００）として凸部を設けると、反射機能、光取り出し端部に寄与する。

第１電極１０００は発光構造部５１１０に電流拡散、注入する機能を有する。上記第１導電型層２内の面内拡散層（８，９）、第２導電型層３内及び第２電極２０００（下部電極層２１００）の面内拡散、具体的にはシート抵抗を適宜調整することで、第１電極、第２電極間隔を調整して、所望の拡散状態、発光構造部５１１０の幅の発光素子とできる。

第１電極１０００は、パッド部１１００、接続電極部１２００とも同じ電極構造としても良く、別々に、例えば、オーミック接触用の電極として電極１０００の形

状で形成して、パッド部１１００にのみパッド電極を形成する構造として、形成しても良い。

（第２電極２０００）

下部電極２１００は、上述したように、発光構造部５１１０内で第２導電型層３の露出部２ｓのほぼ全面に形成されることで、発光構造部５１１０において面内に電流拡散させる拡散層として機能させることができる。第２導電型層３内に電流拡散層を設ける場合には、面内に拡散させる電極２１００が不要となるが、素子構造として困難な場合が多いため、素子構造内の電流拡散層と電極拡散層の両方を用いることもできる。窒化物半導体においてはｐ型層における面内拡散が不十分となる場合が多いため、外部と接続させるパッド部２２００ｐと、そこから延伸させて発光構造部５１１０に電流を拡散させる第２電極２０００の上部電極２２００、配線電極２２００ａ（２２００ｂ）と、第２電極２０００を面内に拡散するように配線電極２２００ａ（２２００ｂ）それよりも広い電極形成面を有する下部電極２１００を設けることが良い。

下部電極２１００は、上述したように透光性電極として設けることが好ましく、図１６Ｂ，図３３Ｂ，図５４Ａ，図５５に示すように、基板１側を光り取り出し面とする場合には、透光性電極の上に、又は透光性の絶縁膜などを介して反射膜を設けたり、透光性電極層の上に反射性電極層を設けた電極構造としたり、反射性電極とすることができる。光取り出し面を基板１側、第２導電型層３とする場合のいずれでも、好ましくは第２電極２０００の下部電極層２１００に開口部を設けて透光性電極とすること、若しくは下部電極層２１００の形成部２１００ａも透光性電極であることが好ましい。

第１，２電極１０００，２０００の電極材料、特にｐ型窒化物半導体層用の下部電極２１００の材料としては、ニッケル（Ｎｉ）、白金（Ｐｔ）パラジウム（Ｐｄ）、ロジウム（Ｒｈ）、ルテニウム（Ｒｕ）、オスミウム（Ｏｓ）、イリジウム（Ｉｒ）、チタン（Ｔｉ）、ジルコニウム（Ｚｒ）、ハフニウム（Ｈｆ）、バナジウム（Ｖ）、ニオブ（Ｎｂ）、タンタル（Ｔａ）、コバルト（Ｃｏ）、鉄（Ｆｅ）、マンガン（Ｍｎ）、モリブデン（Ｍｏ）、クロム（Ｃｒ）、タングステン（Ｗ）、ランタン（Ｌａ）、銅（Ｃｕ）、銀（Ａｇ）、イットリウム（Ｙ）

よりなる群から選択された少なくとも一種を含む金属、合金、積層構造、さらには、それらの化合物、例えば、導電性の酸化物、窒化物などがあり、導電性の金属酸化物（酸化物半導体）も、錫をドーピングした厚さ５０Å～１０μｍの酸化インジウム（Ｉｎｄｉｕｍ　Ｔｉｎ　Ｏｘｉｄｅ；ＩＴＯ）、ＺｎＯ、In_2O_3、またはSnO_2が挙げられ、透光性に有利なことから好適に用いられる。酸化物半導体材料の場合には、各導電型層２，３とその電極１０００、２０００との中間的な機能を有する形態となり、導電型層２，３と金属酸化物の導電性を同じとしてもよく、異なる導電型の酸化物半導体層を電極とする場合には、素子構造１０１００との間に何らかの介在層（逆導電型層、酸化物半導体、金属層）を更に介して使用してもよく、また拡散導体２１００（９）として機能することからも、第１導電型層２側の拡散導体８として、このような半導体層、電極材料を用いても良い。下部電極２１００が、金属層の場合には、透光性が確保される薄膜で形成することができ、また、本発明の開口部２１００ｂを有する下部電極層２１００の場合には、下部電極２１００の反射性の大きい金属、例えばＡｌ，Ａｇ，Ｒｈ、を用いることができる。

ここで、図６０Ａ～Ｅは第２電極２０００とその下部電極２１００、上部電極２２００（配線部２２００ａ）の実施形態を説明するものであり、上述したとおり、パッド部２２００ｐを列状２２００ａ（点線部）に配列して接続電極部２２００ａとしてもよく（図５８）、素子構造部１０１００の開口部６００に対応させた電極開口部２１００ｂと、電極形成部２１００ａとで下部電極２１００を形成しても良く（図６０Ｂ）、図６０Ｄに示すように、下部電極２１００を一部開口２１００ｂさせて、開口部２１００ｂ（第２導電型層３表面）と電極２１００の表面上に跨る電極２２００αとして、配線部２２００ａ（台座部２２００ｐ）を形成することもでき、酸化物などの化合物電極の場合には、第２電極の接着性を向上させることができる。また、このような開口部２１００ｂを充填する第２電極２２００αの形態としては、図６０Ｅに示すように、第２導電型層３に凹部６００を設けて開口させて、下部電極開口部２１００ｂと共に、第２電極２０００を開口部２１００ｂと電極２１００上に跨って形成する電極２２００α（上部電極台座部２２００ｐ－１，－２）とすることもできる。

また、第２電極の電極２１００は、発光構造部５１１０に設けられるため、光取出し、反射が有効となるように、透光性、反射性を好適に機能するには、透光性（光透過率）の大きい電極（形成部２１００ａ）とするか（光吸収の小さい電極材料）若しくはその透過率（吸収率）を調整して、及び／又は透過性を決める開口部２１００ｂの面積比（開口部面積の総和／電極形成［５３００］面積）、開口率、分布状態を調整して、とすることがいずれの光取出し方向においても有用である。

また、図６０Ａに示すように電極形成部２ｓの光取り出し面を凹凸部６００とする方法、図６０Ｃ、Ｅに示すように、電極２３００開口部２０００ｂに対応して、第２導電型層３にも凹部６００ａを設けて、凸部上面６００ｃ（電極材料界面）と凹部底面６００ａ（保護膜、絶縁膜材料界面）とでもって、異なる材料間の界面で凹凸部６００が形成されて、好適な光取出し、反射に寄与し、また、側面６００ｂの傾斜角を大きくすることにより、側面での反射が強まり、光取出し効率が向上する。このような凹凸部６００は、素子構造１０１００の端面、側面、露出面、界面（層間、基板面、金属形成面、絶縁膜などの膜形成面）のいずれに形成しても良く、例えば図５７に示すように図中矢印に伝搬する光を散乱、方向制御して取出し効率を高める目的で、基板１に凹凸加工６００を施して、その上に素子構造１０１００を積層させることで、基板１と素子構造の半導体との間で凹凸界面を形成させること、除去部７００により基板１を除去して露出した下地層５００（第１導電型層２）の除去面に凹凸界面６００を形成することもできる。このような凹凸面６００を形成することが、本発明の発光素子において、光取出しが向上し、出力が向上し、好ましい。

ここで、凹凸部６００の形状、前記周期構造の下部電極２１００の開口部２１００ｂ（形成部２０００ａ）の形状としては、面内で、ドット状、格子状、ハニカム状、枝状、矩形状、多角形状、円形状など様々な形状の凸部（上面）若しくは開口部２０００ｂ及び、又は凹部（底面）若しくは形成部２１００ａとすることができ、その大きさとしては、少なくとも光に対して反射、散乱、取出しするように、λ／（４ｎ）｛ｎは凹凸部の界面を構成する材料の屈折率、λは発光層の発光波長｝以上の大きさとすることであり、具体的には開口部、凸部、凹部の間隔、１

辺の長さ（矩形状、多角形状）、直径（ドット状、円形状）を、１～１０μｍとすることであり、好ましくは２～５μｍの大きさとすることである。断面の形状としては特に限定されないが、ほぼ垂直な凹部側面としても、傾斜面（メサ状、逆メサ状）となっていても良い。また、本発明において反射膜は、反射機能を持たせる素子の端面、露出面、基板との界面に形成して、所望（例えば基板１側）の光取出しを実現させるものである。具体的には、凹凸部６００と同様に、素子の露出面である第１，２導電型層露出面１ｓ（５２００）、２ｓ（５３００）、電極開口部２０００ｂの他、各半導体層（第１，２導電型層、発光構造部５１１０）の側面５１１０ａなど、さらに基板面に設けることができ、側面などでは傾斜面として所望の方向への反射光を得ることができ、さらに上述したように、他の金属層（例えば電極）に反射性を持たせることもでき、さらに上記凹凸部６００の各面６００ａ～ｃにも用いることができる。また、反射膜の材料としては、金属膜、酸化物膜（絶縁膜）、多層膜反射膜（ＤＢＲ）などを用いることができ、可視光、特に発光層が$In_xGa_{1-x}N$（$0 \leqq x \leqq 1$）であるような場合にはＡｌ，Ａｇが高反射膜材料として機能し、その他、形成位置、形成部分（素子の端部）の材料、発光波長などにより、それに適した材料が選択される。

ここで、第１電極１０００と第２電極２０００、若しくは、第１電極１０００と、第２電極２０００及び上部電極２２００（台座部２２００ｐ、接続電極）とを同一構造、材料の電極として、同時に形成することもできる。具体的には、露出部２ｓ側から順に、Ｔｉ／Ａｕ、Ｔｉ／Ａｌなどのように、第１導電型層とのオーミック用と密着用としてのＴｉ層（第１層）とパッド用のパッド層（第２層）として金、Ａｌ、白金族の構成、また、オーミック用の第１層（例えば、Ｗ、Ｍｏ、Ｔｉが第１導電型層とのオーミック接触に好ましい）と、パッド用の第２層との間にバリア層として、高融点金属層（Ｗ、Ｍｏ、白金族）を設ける構造、例えばＷ／Ｐｔ／Ａｕ、Ｔｉ／Ｒｈ（第２層ａ）／Ｐｔ（第２層ｂ）／Ａｕ、が用いられ、特に第１電極（オーミック接触用）として好適に用いられる。特に、反射性、バリア性に優れるＲｈを第２層に用いると、光取出し効率が向上して好ましい。また、第２導電型層３のオーミック用の電極２３００としては、露出部２ｓ側から

順に、Ｎｉ／Ａｕ、Ｃｏ／Ａｕの他、ＩＴＯなどの導電性酸化物、白金族元素の金属、Ｒｈ／Ｉｒ、Ｐｔ／Ｐｄなどが好適に用いられる。

特に、下部電極２１00（形成部２１00ａ）として、好ましくは、Ｎｉ／Ａｕ（透光性電極材料）であり、Ｒｈ／Ｉｒ（反射性電極材料）である。

（第４の発明）

本発明における第４の発明は、上述した第１～３の発明で得られる発光素子を用いた発光装置の発明であり、特に、発光装置の充填部材、レンズなどに光り変換部材を用いて、発光素子の光の少なくとも一部を光り変換させる発光装置について説明するものである。

実施形態１０．

実施形態１０では、上記第１～３の発明、実施形態１～９などの発光素子１０００を、その電極形成面で積層基体１０４00に、実装、接合した素子積層体１０３00であって、その模式断面図を図５４Ａに示す。発光素子１００00を素子積層体１０３00として、他の形態として、上述したように素子側で分離された第１電極２１（パッド部２９）｛第１導電型層２の電極とパッド部｝を、図５４Ａに示すように基体１０４00側電極１１２00で互いに接続し、分離された第２電極３１（パッド部３２）｛第２導電型層３の電極とパッド部｝も同様に基体１０４00側で互いに電気的に接続されて、実装、接合されても良い。基体１０４00側電極１１２00は、発光素子１００00側電極２１（２９），３１（３２）に対応して、互いに絶縁膜１１１00などで絶縁分離されて設けられ、外部接続用の電極１１３00が設けられている。基体１０４00に素子部１１５00を設けても良く、ここでは、図５４Ｂの等価回路に示すように、電流、静電保護素子（素子構造部１１５00）として、ｐ型層（第１導電型層）１１５00ａ、ｎ型層（第２導電型層）１１５00ｂを設けている。ここでは、素子部１１５00を基体１０４00に１つだけ設けているが、２つ以上設けて外部（素子１００00、実装基体２０１00）の電極、基体１０４00側配線などで接続される形態などでも良く、また、保護素子は、基体１０４00上、発光装置２０００0内（載置部２２２00）に実装して、発光素子にワイヤー接続、配線接続されても良い。

発光素子１００００側電極２１，３１と、基体１０４００の電極１１２００とは接合層１１４００を介して接合しているが、素子１００００側電極の一部と、若しくは基体１０４００側電極１１２００の一部と、を接合層の一部としても良く、パッド部１１、２２ｐに代えて接合層を形成しても良い。

また、基体１０４００は、素子構造１１５００を有しない通常のサブマウントでも良い。基体１０４００と外部とは、接続用の電極１１３００でワイヤー接続されても良く、基体１０４００の素子構造部の電極、若しくは内部、外部を導通する電極層を、実装面側に形成して、電極１１３００、接合層１１４００として設けても良い。

（支持基板９００）

本発明の発光素子構造１００００において、素子積層構造１０１００の形成時に用いた成長用基板１を除去すること形態としても良く、具体的には、図５９Ｂに示すように、基板４００、若しくは基板４００と積層構造１０１００との間に設けられた介在層５００の一部若しくは全部、又はそれらに加えて、第１導電型層１の一部を除去領域７００として、除去することも可能であり、すなわち、素子積層構造部１０１００以外で不要な領域を除去することが可能である。具体的には、図１６Ｂに示すように、サブマウントなどの素子積層基体への接着・実装、図５９Ａ～Ｂに示すように、支持基板１７００に貼り合わせた状態で、研磨・研削除去、基板１上の一部積層部を、化学的な方法（エッチャント）による潮解、融解、レーザ照射（レーザアブレーション）による分解で、除去部７００と素子積層構造部１０１００とを分離させる方法、機械的な研磨・外力を加えて面内、素子構造内において基板１と素子積層構造部１０１００との間での応力、歪による層破壊などによる剥離などの方法、及び、それらの方法の組合せにより除去することができる。

好ましくは、支持基板９００に、接合層８００などを介して貼り合わせることによる転写でもって、基板１などの除去部７００として除去することが好ましい。このとき、支持基板７００の材料としては、その目的により種々の材料を用いることができ、素子の放熱性を高めるためには、放熱用の基板として、ＡｌＮ、ＢＮ、ＳｉＣ、ＧａＡｓ、Ｓｉ、Ｃ（ダイヤモンド）が好適に用いられる。その他

の材料としては、Ｓｉ、ＳｉＣ、ＧａＡｓ、ＧａＰ、ＩｎＰ、ＺｎＳｅ、ＺｎＳ、ＺｎＯ等の半導体から成る半導体基板、又は、金属単体基板、又は相互に非固溶あるいは固溶限界の小さい２種以上の金属の複合体から成る金属基板を用いることができ、金属材料として具体的にはＡｇ，Ｃｕ，Ａｕ，Ｐｔ等の高導電性金属から選択された１種以上の金属と、Ｗ，Ｍｏ，Ｃｒ，Ｎｉ等の高硬度の金属から選択された１種以上の金属と、から成るものを用いることができる。さらに、金属基板としては、Ｃｕ－ＷあるいはＣｕ－Ｍｏの複合体を用いることが好ましい。基板による発光素子の光の吸収・損失、素子構造１０１００との接着性（素子構造１０１００と基板９００若しくは実装部材２０３００との間の熱膨張係数差など）を考慮して、支持基板９００の材料、及び接着方法が選択され、基板９００側から光を取出す場合には、透光性材料を選択し、また銀ペーストなどの透光性の接着層８００若しくは接着層を介さない接着方法により、光損失が少なくなるような構造とし、また、除去部７００側を光り取出し方向とする場合には、接着層８００若しくは基板９００、又は積層構造１０１００の一部に、Ａｌ、Ａｇなどの反射膜を設けるなどして、外部取出し効率を高めると良い。また、図５９Ｂに示すように、半導体層積層順序が転写により逆転する場合に本発明は、図中矢印にて示すように第１，２導電型層２，３を逆転させて本発明における素子構造とすることはいうまでもない。

（接合層８００、接合層１１４００、接着部材２０４００）

支持基板９００と素子構造１０１００との接着、素子構造１０１００（１０００）と積層基体１０３００との接着、発光素子１０００、支持基板９００、積層基体１０３００と発光装置２０００の実装基体２０１００（収納部２０２００）との接着、接合において、接合層８００、（１１４００）、接着部材２０４００を用いることができる。その材料、構造としては、Ａｇペースト、カーボンペースト、ＩＴＯペーストのような混合、複合組成物（有機物）、半田材料の他、発光素子１０００からの放熱性を考慮して、耐熱性に優れた材料、構造として、Ａｕ、Ｓｎ、Ｐｄ、Ｉｎ等の金属若しくはその積層体並びに合金などが、本発明の大面積、大電流駆動で高発熱性の素子に効果的である。第１及び第２の共晶形成層の組合せは、Ａｕ－Ｓｎ、Ｓｎ－Ｐｄ、又はＩｎ－Ｐｄが好ましい。さらに好ましくは、第１の

共晶形成層にＳｎを、そして第２の共晶形成層にＡｕを用いる組合せである。そのほかに、金属バンプ、Ａｕ－Ａｕ接合などの金属金属接合なども用いることができる。

またこのような接合層は、下地側（基板４００、素子構造１０１００表面、支持基板９００、実装基体２０１００、積層基体１０１００）に、密着性の良い層のメタライジング層などを介したり、上記発光素子の光反射のために反射層などを介したりして、共晶膜、共晶多層膜、合金膜などの接着膜（接合層）を形成したり、その表面側に酸化防止の表面保護膜を設けても良く、また、接着側の実装側にもメタライジング層（密着性の層）、表面保護層、接着膜（接合層）を形成して、両者が接着・接合されても良い。

具体例としては、図５６に示すように、発光素子１００００の基板（サファイア）１０と実装部２０２００の底面（例えばＡｇメッキの表面被膜）に接合層２０４００としては、基板側から順に、Ａｌ（０．２μｍ、反射層）／Ｗ（０．２μｍ）／Ｐｔ（０．２μｍ）と、その上にＡｕ（０．３μｍ）／Ｓｎ（０．２μｍ）を７対とその表面にＡｕ（１０ｎｍ）層を形成して、実装部２０２００側にもＡｕ層を形成して、加熱して圧着して接着層２０４００により発光素子１００００を接着する。図５９Ｂにおいて、素子構造１０１００を支持基板１７００に貼り合わせる接合層８００の具体例として、第２導電型層（ｐ型層）のｐ側電極の上に、Ｎｉ－Ｐｔ－Ａｕ－Ｓｎ－Ａｕの多層膜を、膜厚０．２μｍ－０．３μｍ－０．３μｍ－３．０μｍ－０．１μｍ　膜厚が２００μｍで、Ｃｕ３０％とＷ７０％の複合体から成る金属基板１７００を用い、その金属基板の表面に、Ｔｉから成る密着層、Ｐｔから成るバリア層、そしてＡｕから成る第２の共晶形成層を、この順で、膜厚０．２μｍ－０．３μｍ－１．２μｍに形成して、加熱して圧着する。

（素子積層体１０３００）

本発明において、上記発光素子を発光装置２００００に実装する場合に、図１６Ｂ、図３３Ｂ、図５４Ａ，図５５に示すように、ヒートシンク、サブマウントなどの積層基体１０４００に、発光素子１００００を実装して、素子の実装積層体として、素子積層体１０３００を形成しても良い。このとき、発光素子１００００

を積層実装する基体１０４００の材料としては、上記支持基板と同様であり、その目的、例えば、放熱性、光取出し構造、を考慮して選択される。また、このような素子積層体１０３００は、発光素子１００００との接合面に対向する面側を実装側として、発光装置２０００００の実装部２０２００に接合される。

本発明の積層基体１０４００には、発光素子１００００の電極形成面側に対向して接合する場合には、発光素子１００００側の電極２１（２９），３１（３２）に対応して、基体１０４００側に電極構造１１２００ａ，ｂが設けられ、発光素子１００００の電極形成面と対向する面側（基板４００）に対向して基体１０４００に接合する場合には、基体１０４００側電極は不要であり、接合用の接着層などが設けられるが、発光素子１００００とワイヤー接続用の電極を設けても良い。基体１０４００側電極１１２００は、図に示すように、発光素子１００００との接合面側にのみ設けられていても良く、接合面に対向する実装面側にまで回り込む実装側電極、実装面側に設けられた基体素子１０４００の電極１１４００、基体１０４００に貫通孔、ビアホールを設けて発光素子１００００の接合面側から実装面側に連通、連結若しくは電気的に接合させた実装面側電極が設けられても良い。

また、図では１つの発光素子１０１００を１つの積層基体１０４００に実装しているが、発光素子１０１００を複数集積して１つの積層基体１０４００に、基体１０４００側配線電極により並列、直列、両者混合で接続させ、実装した積層体１０３００としても良く、１つの発光素子１０１００に対し複数の積層基体１０４００を、例えば異なる機能の素子を基体としても良く、またこれらの組合せでも良く、さらに、発光素子１０１００、積層基体（素子）１０３００を縦方向に、いずれかを複数積層した素子積層体１０３００を形成しても良い。

発光素子１００００は、図５５に示すように、被覆膜１０５００で覆われていても良く、その組成物としては、SiO_2、Al_2O_3、$MSiO_3$（なお、Mとしては、Ｚｎ、Ｃａ、Ｍｇ、Ｂａ、Ｓｒ、Ｚｒ、Ｙ、Ｓｎ、Ｐｂ、などが挙げられる。）などの透光性無機部材であり、蛍光体（光変換部材１０６００）を含有させたものも好適に用いられる。これらの透光性無機部材により蛍光体同士が結着され、さらに蛍光体は層状にＬＥＤ１００００や支持体１０４００上に堆積され結着される。このほかに被覆層としては、素子構造１００００を被覆する絶縁保護膜

の他、反射膜（Ａｌ、Ａｇなどの金属反射膜）を設けても良く、その他の反射膜材料としてはＤＢＲなどを形成しても良い。

（光変換部材１０６00，層２３１00）

光変換部材１０６00、若しくは発光装置２００00内の光変換層２３１00は、発光素子１００00の光を一部吸収して、異なる波長の光を発光するものであり、蛍光体を含有したものを用いることができる。このような光変換部材１０６00、光変換層２３１00は、上記のように発光素子１００00一部若しくは全体、又はそれに加えて積層基体１０４00の一部に被覆して、被覆膜１０５00として形成されてもよい。また、上記第１～３の発明において、構造部などを被覆する透光性保護膜などの他、発光素子からの光経路内、例えば透光性部材（レンズ、封止部材）、などに設けることができる。蛍光体のバインダーとしては、少なくともＳｉ、Ａｌ、Ｇａ、Ｔｉ、Ｇｅ、Ｐ、Ｂ、Ｚｒ、Ｙ、Ｓｎ、Ｐｂ、あるいはアルカリ土類金属の群から選択される１種以上の元素を含む酸化物及び水酸化物は、少なくともＳｉ、Ａｌ、Ｇａ、Ｔｉ、Ｇｅ、Ｐ、Ｂ、Ｚｒ、Ｙ、Ｓｎ、Ｐｂ、あるいはアルカリ土類金属の群から選択される１種以上の元素を含む有機金属化合物（好ましくはさらに酸素を含む）により生成される。ここで、有機金属化合物には、アルキル基，アリール基を含む化合物等が含まれる。このような有機金属化合物として、例えば金属アルコキシド、金属ジケトナート、金属ジケトナート錯体、カルボン酸金属塩等が挙げられる。

また、図５６に示すように、発光装置２００00の封止部材２３０00の一部として設けられても良く、図に示すように発光素子１００00に離間して、封止部材２３０00ａ上、若しくは２３０００ｂとの間に設けられた層２３１00として形成されても良く、封止部材２３０00内に分散して光変換部材を含有して、封止部材２３０00を光変換層２３１00としても良く、装置基体２２０00、実装基体２０１00、凹部収納部２０２00内に沈降層として設けられても良い。

本発明の光変換部材に用いられる蛍光体は、発光素子から放出された可視光や紫外光を他の発光波長に変換するためのものであり、素子構造１０１00の半導体発光層から発光された光で励起されて発光する蛍光体などで、蛍光体として紫

外光、可視光により励起されて所定の色の光を発生する蛍光体も用いることができる。

具体的な蛍光体としては、銅で付活された硫化カドミ亜鉛やセリウムで付活されたイットリウム・アルミニウム・ガーネット系蛍光体（以下、「ＹＡＧ系蛍光体」と呼ぶ。）が挙げられる。特に、高輝度且つ長時間の使用時においては（$Re_{1-x}Sm_x)_3(Al_{1-y}Ga_y)_5O_{12}$：Ｃｅ（$0 \leqq x < 1$、$0 \leqq y \leqq 1$、但し、Ｒｅは、Ｙ，Ｇｄ，Ｌａからなる群より選択される少なくとも一種の元素である。）などが好ましい。この蛍光体は、ガーネット構造のため、熱、光及び水分に強く、励起スペクトルのピークが４７０ｎｍ付近などにさせることができる。また、発光ピークも５３０ｎｍ付近にあり７２０ｎｍまで裾を引くブロードな発光スペクトルを持たせることができる。本発明において、蛍光体は、２種類以上の蛍光体を混合させてもよい。即ち、Ａｌ、Ｇａ、Ｙ、Ｌａ及びＧｄやＳｍの含有量が異なる２種類以上の$(Re_{1-x}Sm_x)_3(Al_{1-y}Ga_y)_5O_{12}$：Ｃｅ蛍光体を混合させてＲＧＢの波長成分を増やすことができる。半導体発光素子の発光波長には、バラツキが生ずるものがあるため２種類以上の蛍光体を混合調整させて所望の白色系の混色光などを得ることができる。具体的には、発光素子の発光波長に合わせて色度点の異なる蛍光体の量を調整し含有させることでその蛍光体間と発光素子で結ばれる色度図上の任意の点を発光させることができる。蛍光体は、発光装置の表面上において一層からなる被覆層１０５００、光変換部層２２１００、部材１０６００中に二種類以上存在してもよいし、二層からなるコーティング層中にそれぞれ一種類あるいは二種類以上存在してもよい。このようにすると、異なる蛍光体からの光の混色による白色光が得られる。この場合、各蛍光物質から発光される光をより良く混色しかつ色ムラを減少させるために、各蛍光体の平均粒径及び形状は類似していることが好ましい。ＹＡＧ系蛍光体に代表されるアルミニウム・ガーネット系蛍光体と、赤色系の光を発光可能な蛍光体、特に窒化物系蛍光体とを組み合わせたものを使用することもできる。これらのＹＡＧ系蛍光体および窒化物系蛍光体は、混合して被覆層中に含有させてもよいし、複数の層から構成される被覆層中に別々に含有させてもよい。以下、それぞれの蛍光体について詳細に説明していく。

本実施の形態に用いられるアルミニウム・ガーネット系蛍光体とは、Ａｌを含み、かつＹ、Ｌｕ、Ｓｃ、Ｌａ、Ｇｄ、Ｔｂ、Ｅｕ及びＳｍから選択された少なくとも一つの元素と、Ｇａ及びＩｎから選択された一つの元素とを含み、希土類元素から選択された少なくとも一つの元素で付活された蛍光体であり、ＬＥＤチップ１０１００から発光された可視光や紫外線で励起されて発光する蛍光体である。例えば、上述したＹＡＧ系蛍光体の他、$Tb_{2.95}Ce_{0.05}Al_5O_{12}$、$Y_{2.90}Ce_{0.05}Tb_{0.05}Al_5O_{12}$、$Y_{2.94}Ce_{0.05}Pr_{0.01}Al_5O_{12}$、$Y_{2.90}Ce_{0.05}Pr_{0.05}Al_5O_{12}$等が挙げられる。これらのうち、特に本実施の形態において、Ｙを含み、かつＣｅあるいはＰｒで付活され組成の異なる２種類以上のイットリウム・アルミニウム酸化物系蛍光体が利用される。

発光層に窒化物系化合物半導体を用いた発光素子から発光した青色系の光と、青色光を吸収させるためボディーカラーが黄色である蛍光体から発光する緑色系及び赤色系の光と、或いは、黄色系の光であってより緑色系及びより赤色系の光を混色表示させると所望の白色系発光色表示を行うことができる。発光装置はこの混色を起こさせるために蛍光体の粉体やバルクをエポキシ樹脂、アクリル樹脂或いはシリコーン樹脂などの各種樹脂や酸化珪素、酸化アルミニウムなどの透光性無機物中に含有させることもできる。このように蛍光体が含有されたものは、ＬＥＤチップからの光が透過する程度に薄く形成させたドット状のものや層状ものなど用途に応じて種々用いることができる。蛍光体と透光性無機物との比率や塗布、充填量を種々調整すること及び発光素子の発光波長を選択することにより白色を含め電球色など任意の色調を提供させることができる。

また、２種類以上の蛍光体をそれぞれ発光素子からの入射光に対して順に配置させることによって効率よく発光可能な発光装置とすることができる。即ち、反射部材を有する発光素子上には、長波長側に吸収波長があり長波長に発光可能な蛍光体が含有された色変換部材と、それよりも長波長側に吸収波長がありより長波長に発光可能な色変換部材とを積層などさせることで反射光を有効利用することができる。また、発光ピーク波長λpも５１０ｎｍ付近にあり７００ｎｍ付近まで裾を引くブロードな発光スペクトルを持つ。一方、セリウムで付活されたイットリウム・アルミニウム酸化物系蛍光体である赤色系が発光可能なＹＡＧ系蛍

光体でも、ガーネット構造であり熱、光及び水分に強く、励起吸収スペクトルのピーク波長が４２０ｎｍから４７０ｎｍ付近にさせることができる。また、発光ピーク波長λｐが６００ｎｍ付近にあり７５０ｎｍ付近まで裾を引くブロードな発光スペクトルを持つ。

ガーネット構造を持ったＹＡＧ系蛍光体の組成の内、Ａｌの一部をＧａで置換することで発光スペクトルが短波長側にシフトし、また組成のＹの一部をＧｄ及び／又はＬａで置換することで、発光スペクトルが長波長側へシフトする。このように組成を変化することで発光色を連続的に調節することが可能である。したがって、長波長側の強度がＧｄの組成比で連続的に変えられるなど窒化物半導体の青色系発光を利用して白色系発光に変換するための理想条件を備えている。

（窒化物系蛍光体）

本発明で使用される蛍光体は、Ｎを含み、かつＢｅ、Ｍｇ、Ｃａ、Ｓｒ、Ｂａ、及びＺｎから選択された少なくとも一つの元素と、Ｃ、Ｓｉ、Ｇｅ、Ｓｎ、Ｔｉ、Ｚｒ、及びＨｆから選択された少なくとも一つの元素とを含み、希土類元素から選択された少なくとも一つの元素で付活された窒化物系蛍光体も用いることができる。また、本実施の形態に用いられる窒化物系蛍光体としては、ＬＥＤチップ１０１００から発光された可視光、紫外線、及びＹＡＧ系蛍光体からの発光を吸収することによって励起され発光する蛍光体をいう。例えば、Ｃａ－Ｇｅ－Ｎ：Ｅｕ，Ｚ系、Ｓｒ－Ｇｅ－Ｎ：Ｅｕ，Ｚ系、Ｓｒ－Ｃａ－Ｇｅ－Ｎ：Ｅｕ，Ｚ系、Ｃａ－Ｇｅ－Ｏ－Ｎ：Ｅｕ，Ｚ系、Ｓｒ－Ｇｅ－Ｏ－Ｎ：Ｅｕ，Ｚ系、Ｓｒ－Ｃａ－Ｇｅ－Ｏ－Ｎ：Ｅｕ，Ｚ系、Ｂａ－Ｓｉ－Ｎ：Ｅｕ，Ｚ系、Ｓｒ－Ｂａ－Ｓｉ－Ｎ：Ｅｕ，Ｚ系、Ｂａ－Ｓｉ－Ｏ－Ｎ：Ｅｕ，Ｚ系、Ｓｒ－Ｂａ－Ｓｉ－Ｏ－Ｎ：Ｅｕ，Ｚ系、Ｃａ－Ｓｉ－Ｃ－Ｎ：Ｅｕ，Ｚ系、Ｓｒ－Ｓｉ－Ｃ－Ｎ：Ｅｕ，Ｚ系、Ｓｒ－Ｃａ－Ｓｉ－Ｃ－Ｎ：Ｅｕ，Ｚ系、Ｃａ－Ｓｉ－Ｃ－Ｏ－Ｎ：Ｅｕ，Ｚ系、Ｓｒ－Ｓｉ－Ｃ－Ｏ－Ｎ：Ｅｕ，Ｚ系、Ｓｒ－Ｃａ－Ｓｉ－Ｃ－Ｏ－Ｎ：Ｅｕ，Ｚ系、Ｍｇ－Ｓｉ－Ｎ：Ｅｕ，Ｚ系、Ｍｇ－Ｃａ－Ｓｒ－Ｓｉ－Ｎ：Ｅｕ，Ｚ系、Ｓｒ－Ｍｇ－Ｓｉ－Ｎ：Ｅｕ，Ｚ系、Ｍｇ－Ｓｉ－Ｏ－Ｎ：Ｅｕ，Ｚ系、Ｍｇ－Ｃａ－Ｓｒ－Ｓｉ－Ｏ－Ｎ：Ｅｕ，Ｚ系、Ｓｒ－Ｍｇ－Ｓｉ－Ｏ－Ｎ：Ｅｕ，Ｚ系、Ｃａ－Ｚｎ－Ｓｉ－Ｃ－Ｎ：Ｅｕ，Ｚ系、Ｓｒ－Ｚｎ－Ｓ

i－C－N：Eu，Z系、Sr－Ca－Zn－Si－C－N：Eu，Z系、Ca－Zn－Si－C－O－N：Eu，Z系、Sr－Zn－Si－C－O－N：Eu，Z系、Sr－Ca－Zn－Si－C－O－N：Eu，Z系、Mg－Zn－Si－N：Eu，Z系、Mg－Ca－Zn－Sr－Si－N：Eu，Z系、Sr－Zn－Mg－Si－N：Eu，Z系、Mg－Zn－Si－O－N：Eu，Z系、Mg－Ca－Zn－Sr－Si－O－N：Eu，Z系、Sr－Mg－Zn－Si－O－N：Eu，Z系、Ca－Zn－Si－Sn－C－N：Eu，Z系、Sr－Zn－Si－Sn－C－N：Eu，Z系、Sr－Ca－Zn－Si－Sn－C－N：Eu，Z系、Ca－Zn－Si－Sn－C－O－N：Eu，Z系、Sr－Zn－Si－Sn－C－O－N：Eu，Z系、Sr－Ca－Zn－Si－Sn－C－O－N：Eu，Z系、Mg－Zn－Si－Sn－N：Eu，Z系、Mg－Ca－Zn－Sr－Si－Sn－N：Eu，Z系、Sr－Zn－Mg－Si－Sn－N：Eu，Z系、Mg－Zn－Si－Sn－O－N：Eu，Z系、Mg－Ca－Zn－Sr－Si－Sn－O－N：Eu，Z系、Sr－Mg－Zn－Si－Sn－O－N：Eu，Z系など種々の組合せの蛍光体を製造することができる。希土類元素であるZは、Y、La、Ce、Pr、Nd、Gd、Tb、Dy、Ho、Er、Luのうち少なくとも１種以上が含有されていることが好ましいが、Sc、Sm、Tm、Ybが含有されていてもよい。これらの希土類元素は、単体の他、酸化物、イミド、アミド等の状態で原料中に混合する。希土類元素は、主に安定な３価の電子配置を有するが、Yb、Sm等は２価、Ce、Pr、Tb等は４価の電子配置を有する。酸化物の希土類元素を用いた場合、酸素の関与が蛍光体の発光特性に影響を及ぼす。つまり酸素を含有することにより発光輝度の低下を生じる場合もある。その反面、残光を短くするなどの利点もある。但し、Mnを用いた場合は、MnとOとのフラックス効果により粒径を大きくし、発光輝度の向上を図ることができる。本発明に係る蛍光体は、Mnが添加されたSr－Ca－Si－N：Eu、Ca－Si－N：Eu、Sr－Si－N：Eu、Sr－Ca－Si－O－N：Eu、Ca－Si－O－N：Eu、Sr－Si－O－N：Eu系シリコンナイトライドである。この蛍光体の基本構成元素は、一般式$L_XSi_YN_{(2/3X+4/3Y)}$：Eu若しくは$L_XSi_YO_ZN_{(2/3X+4/3Y-2/3Z)}$：Eu（Lは、Sr、

Ｃａ、ＳｒとＣａのいずれか。）で表される。一般式中、Ｘ及びＹは、Ｘ＝２、Ｙ＝５又は、Ｘ＝１、Ｙ＝７であることが好ましいが、任意のものも使用できる。具体的には、基本構成元素は、Ｍｎが添加された（Sr_XCa_{1-X}）$_2Si_5N_8$：Ｅｕ、$Sr_2Si_5N_8$：Ｅｕ、$Ca_2Si_5N_8$：Ｅｕ、$Sr_XCa_{1-X}Si_7N_{10}$：Ｅｕ、$SrSi_7N_{10}$：Ｅｕ、$CaSi_7N_{10}$：Ｅｕで表される蛍光体を使用することが好ましいが、この蛍光体の組成中には、Ｍｇ、Ｓｒ、Ｃａ、Ｂａ、Ｚｎ、Ｂ、Ａｌ、Ｃｕ、Ｍｎ、Ｃｒ及びＮｉからなる群より選ばれる少なくとも１種以上が含有されていてもよい。但し、本発明は、この実施の形態及び実施例に限定されない。

Ｌは、Ｓｒ、Ｃａ、ＳｒとＣａのいずれかである。ＳｒとＣａは、所望により配合比を変えることができる。

蛍光体の組成にＳｉを用いることにより安価で結晶性の良好な蛍光体を提供することができる。発光中心に希土類元素であるユウロピウムＥｕを用いる。ユウロピウムは、主に２価と３価のエネルギー準位を持つ。具体的な組成としては、$Sr_2Si_5N_8$：Ｅｕ，Ｐｒ、$Ba_2Si_5N_8$：Ｅｕ，Ｐｒ、$Mg_2Si_5N_8$：Ｅｕ，Ｐｒ、$Zn_2Si_5N_8$：Ｅｕ，Ｐｒ、$SrSi_7N_{10}$：Ｅｕ，Ｐｒ、$BaSi_7N_{10}$：Ｅｕ，Ｃｅ、$MgSi_7N_{10}$：Ｅｕ，Ｃｅ、$ZnSi_7N_{10}$：Ｅｕ，Ｃｅ、$Sr_2Ge_5N_8$：Ｅｕ，Ｃｅ、$Ba_2Ge_5N_8$：Ｅｕ，Ｐｒ、$Mg_2Ge_5N_8$：Ｅｕ，Ｐｒ、$Zn_2Ge_5N_8$：Ｅｕ，Ｐｒ、$SrGe_7N_{10}$：Ｅｕ，Ｃｅ、$BaGe_7N_{10}$：Ｅｕ，Ｐｒ、$MgGe_7N_{10}$：Ｅｕ，Ｐｒ、$ZnGe_7N_{10}$：Ｅｕ，Ｃｅ、$Sr_{1.8}Ca_{0.2}Si_5N_8$：Ｅｕ，Ｐｒ、$Ba_{1.8}Ca_{0.2}Si_5N_8$：Ｅｕ，Ｃｅ、$Mg_{1.8}Ca_{0.2}Si_5N_8$：Ｅｕ，Ｐｒ、$Zn_{1.8}Ca_{0.2}Si_5N_8$：Ｅｕ，Ｃｅ、$Sr_{0.8}Ca_{0.2}Si_7N_{10}$：Ｅｕ，Ｌａ、$Ba_{0.8}Ca_{0.2}Si_7N_{10}$：Ｅｕ，Ｌａ、$Mg_{0.8}Ca_{0.2}Si_7N_{10}$：Ｅｕ，Ｎｄ、$Zn_{0.8}Ca_{0.2}Si_7N_{10}$：Ｅｕ，Ｎｄ、$Sr_{0.8}Ca_{0.2}Ge_7N_{10}$：Ｅｕ，Ｔｂ、$Ba_{0.8}Ca_{0.2}Ge_7N_{10}$：Ｅｕ，Ｔｂ、$Mg_{0.8}Ca_{0.2}Ge_7N_{10}$：Ｅｕ，Ｐｒ、$Zn_{0.8}Ca_{0.2}Ge_7N_{10}$：Ｅｕ，Ｐｒ、$Sr_{0.8}Ca_{0.2}Si_6GeN_{10}$：Ｅｕ，Ｐｒ、$Ba_{0.8}Ca_{0.2}Si_6GeN_{10}$：Ｅｕ，Ｐｒ、$Mg_{0.8}Ca_{0.2}Si_6GeN_{10}$：Ｅｕ，Ｙ、$Zn_{0.8}Ca_{0.2}Si_6GeN_{10}$：Ｅｕ，Ｙ、$Sr_2Si$

$_5N_8$：Ｐｒ、$Ba_2Si_5N_8$：Ｐｒ、$Sr_2Si_5N_8$：Ｔｂ、$BaGe_7N_{10}$：Ｃｅなどが製造できるがこれに限定されない。

窒化物系蛍光体は、ＬＥＤチップ１００００によって発光された青色光の一部を吸収して黄から赤色領域の光を発光する。窒化物系蛍光体をＹＡＧ系蛍光体と共に上記の構成を有する発光装置２００００に使用して、ＬＥＤチップ１００００により発光された青色光と、窒化物系蛍光体による黄色から赤色光とが混色により暖色系の白色系の混色光を発光する発光装置を提供する。窒化物系蛍光体の他に加える蛍光体には、セリウムで付活されたイットリウム・アルミニウム酸化物蛍光物質が含有されていることが好ましい。前記イットリウム・アルミニウム酸化物蛍光物質を含有することにより、所望の色度に調節することができるからである。セリウムで付活されたイットリウム・アルミニウム酸化物蛍光物質は、ＬＥＤチップ１０１００により発光された青色光の一部を吸収して黄色領域の光を発光する。ここで、ＬＥＤチップ１００００により発光された青色光と、イットリウム・アルミニウム酸化物蛍光物質の黄色光とが混色により青白い白色に発光する。従って、このイットリウム・アルミニウム酸化物蛍光物質と赤色発光する蛍光体とを、透光性を有するコーティング部材１０５００中に一緒に混合し、ＬＥＤチップ１００００により発光された青色光とを組み合わせることにより白色系の混色光を発光する発光装置を提供することができる。特に好ましいのは、色度が色度図における黒体放射の軌跡上に位置する白色の発光装置である。但し、所望の色温度の発光装置を提供するため、イットリウム・アルミニウム酸化物蛍光物質の蛍光体量と、赤色発光の蛍光体量を適宜変更することもできる。この白色系の混色光を発光する発光装置は、特殊演色評価数Ｒ９の改善を図っている。従来の青色発光素子とセリウムで付活されたイットリウム・アルミニウム酸化物蛍光物質との組合せのみの白色系発光装置は、色温度Ｔｃｐ＝４６００Ｋ付近において特殊演色評価数Ｒ９がほぼ０に近く、赤み成分が不足していた。そのため特殊演色評価数Ｒ９を高めることが解決課題となっていたが、本発明において赤色発光の蛍光体をイットリウム・アルミニウム酸化物蛍光物質と共に用いることにより、色温度Ｔｃｐ＝４６００Ｋ付近において特殊演色評価数Ｒ９を４０付近まで高めることができる。

（発光装置２０００）

図５５は、本発明において、発光素子１０００及びその積層体１０３００を実装基体２０１００に実装した発光装置２０００であり、本発明の実施形態１１に係る。発光装置２０００は、装置基体２２０００により、リード部２１０００が固定され、リード部の一方をマウント・リード２１０００として、実装基体２０１００として機能し、その収納部（凹部）２０２００内に発光素子１０００（積層体１０４００）が接合層１１４００（接着層２０４００）を介して実装され、凹部（開口部２２５００）側面を反射部２０３００とし、且つ、基体２０１００は、放熱部２０５００として機能させて外部放熱器に接続しても良い。また、装置基体２０２００には、光取出し部２２３００に開口して（開口部２２５００）、テラス部２２２００が基体２０１００外部に設けられ、保護素子などの他の素子を実装しても良く、凹部２０２００、基体２２０００開口部には、透光性の封止部材２３０００で封止され、また凹部２０２００外部にも反射部２０３００が設けられている。また、リード電極２１０００は、基体２２０００内部の内部リード２１１００と、それを基体２２０００外部に延在させた外部リード２１２００により、外部と接続される。発光素子１０００（積層体１０３００）は、各リード２１０００に、ワイヤー２５０００接続、電気的接合２０４００により電気的に接続される。

実施形態１１として、図５５に示すように、リード２１０００と絶縁分離された実装基体２１０００に発光素子１０００を接着部材２０４００により実装した発光装置２０００であり、発光素子１０００の収納基体２０１００には反射部２０３００を備え、放熱部２０５００として外部放熱体に接続しても良く、発光素子１０００は各内部リード２１１００にワイヤー２５０００接続され、リード２１０００は外部に延在して外部に電気的に接続される。このように、実装基体２０１００とリード２１０００とを分離することで、熱設計に優れた発光装置とできる。また、発光装置には、光透過性の封止部材２３０００で凹部２０２００、基体２２０００の反射部２２１００、テラス部２２２００を封止して、形成され、該封止部材２３０００に光学的に光学レンズ部を接続して、若しくは光学レンズの形状に封止部材２３０００を成形して、所望の光学系（レンズ）を設けることで、所望の指向性の発光を得ることができる。

パッケージ２２０００の凹部内表面２２１００、２２２００は、エンボス加工させて接着面積を増やしたり、プラズマ処理してモールド部材２３０００との密着性を向上させたりすることもできる。また、パッケージ２２０００の凹部は、図に示すようにその側面が開口方向に向かって広くなる形状（テーパー形状）を有していることが好ましい。このようにすると、発光素子から出光した光は凹部の側面２２１００に反射してパッケージ正面に向かうため、光取出し効率が向上するなどの効果がある。パッケージ２２０００は、外部電極２１２００と一体的に形成させてもよく、パッケージ２２０００が複数に分かれ、はめ込みなどにより組み合わせて構成させてもよい。このようなパッケージ２２０００は、インサート成形などにより比較的簡単に形成することができる。パッケージ材料としてポリカーボネート樹脂、ポリフェニレンサルファイド（ＰＰＳ）、液晶ポリマー（ＬＣＰ）、ＡＢＳ樹脂、エポキシ樹脂、フェノール樹脂、アクリル樹脂、ＰＢＴ樹脂等の樹脂やセラミック、金属などを用いることができる。紫外線を含む光を発光するＬＥＤチップを用いた発光装置を高出力で使用する場合、樹脂が紫外線によって劣化し、樹脂の黄変などによる発光効率低下や、機械的強度の低下による発光装置の寿命の低下などが生じることが考えられる。そこで、パッケージ材料として金属を使用することは、紫外線を含む光を発光するＬＥＤチップを高出力で使用した場合でも樹脂のようにパッケージが劣化することがないためより好ましい。

また、パッケージ２２０００を暗色系に着色させる着色剤としては種々の染料や顔料が好適に用いられる。具体的には、Cr_2O_3、MnO_2、Fe_2O_3やカーボンブラックなどが好適に挙げられる。

ＬＥＤチップ１００００とパッケージ２２０００との接着は熱硬化性樹脂などによって行うこともできる。具体的には、エポキシ樹脂、アクリル樹脂やイミド樹脂などが挙げられる。　外部電極２１２００としては、銅やリン青銅板表面に銀、パラジュウム或いは金などの金属メッキや半田メッキなどを施したものが好適に用いられる。ガラスエポキシ樹脂やセラミックなどの装置基体２２０００上などに設けられた外部電極２１２００としては、銅箔やタングステン層を形成させることができる。

導電性ワイヤー２５００の直径は、好ましくは、Φ１０μｍ以上、Φ７０μｍ以下である。このような導電性ワイヤー２５００として具体的には、金、銅、白金、アルミニウム等の金属及びそれらの合金を用いた導電性ワイヤーが挙げられる。このような導電性ワイヤー２５００は、各ＬＥＤチップ１００００の電極と、インナー・リード及びマウント・リードなどと、をワイヤーボンディング機器によって容易に接続させることができる。

モールド部材２３０００は、発光装置の使用用途に応じてＬＥＤチップ１００００、導電性ワイヤー２５０００、蛍光体が含有されたコーティング層２２１００、１０５００などを外部から保護するため、あるいは光取出し効率を向上させるために設けることができる。モールド部材２３０００は、各種樹脂や硝子（ガラス）などを用いて形成させることができる。モールド部材２３０００の具体的材料としては、主としてエポキシ樹脂、ユリア樹脂、シリコーン樹脂、フッ素樹脂などの耐候性に優れた透明樹脂や硝子などが好適に用いられる。また、モールド部材に拡散剤を含有させることによってＬＥＤチップ１００００からの指向性を緩和させ視野角を増やすこともできる。このような、モールド部材２３０００は、コーティング層の結着剤、バインダーと同じ材料を用いても良いし異なる材料としても良い。

なお、金属パッケージを使用して、窒素ガスなどと共にＬＥＤチップ１００００を気密封止する場合は、モールド部材２３０００は本発明に必須の構成部材ではない。また、紫外線を発光するＬＥＤチップを使用して発光装置を形成する場合であっても、フッ素樹脂等のように紫外線に強い樹脂をモールド部材として使用することができる。

また、他の発光装置２００００として、金属製の基体２２０００に実装部２０１００（凹部２０２００）若しくはリードの一方にマウントリードを設けて発光素子１００００（積層体１０３００）を実装して、基体２２０００に絶縁分離したリード２１０００を設けて、窓部を備えたキャップとなる封止体（金属製など）で、窒素などの不活性ガス、酸素若しくはそれらの混合ガスで気密封止したもの、ＣＯＢのように、金属製などの基板上の１つ若しくは複数の凹部収納部２０２００に発光素子１００００を直接実装し、また各収納部にレンズなどの光学部材を設け

たものなどがある。

発光素子１００００（積層体１０３００）の実装形態として、１つの収納部２０２００（実装基体２０１００）に複数の素子１００００（１０３００）を集積実装したもの、発光素子１００００（１０３００）を実装した基体２０１００を複数設けて（基体２０１００に複数の収納部２０２００設けて）１つの装置基体２２０００で成形したもの、などを挙げることができ、所望の特性に応じて設計することができる。

産業上の利用の可能性

本発明により得られる半導体発光素子は、所望方向への光を積極的に、かつ効率的に取り出すことが可能となり、光取り出し効率向上、高出力化が可能な発光素子が得られる。また、その発光素子を用いた発光装置も出力などの特性に優れたものとなる。

請 求 の 範 囲

1． 基板上に、ｎ型半導体層、活性層及びｐ型半導体層が積層されてなる積層部を有し、その積層部で発光する窒化物半導体発光素子において、

上記積層部の側面は、上記ｎ型半導体層の表面を含む傾斜面であり、そのｎ型半導体層の表面にｎ電極が形成されたことを特徴とする窒化物半導体発光素子。

2． 上記ｎ電極は上記積層部を囲むように形成された請求項１記載の窒化物半導体発光素子。

3． 上記ｎ電極を上記基板の側面から上記基板の下面にも連続して形成した請求項１又は２記載の窒化物半導体発光素子。

4． 上記積層部を円形とした請求項１～３のうちのいずれか１つに記載の窒化物半導体発光素子。

5． 上記積層部を六角形とした請求項１～３のうちのいずれか１つに記載の窒化物半導体発光素子。

6． 上記発光領域となる積層部を複数形成した請求項１～５のうちのいずれか１つに記載の窒化物半導体発光素子。

7． 上記各積層部に形成されたｎ電極は、互いに接続された共通電極として形成された請求項６記載の窒化物半導体発光素子。

8． 上記各積層部において形成された上記ｐ型半導体層とオーミック接触するｐ側オーミック電極が互いに接続された請求項７記載の窒化物半導体発光素子。

9． 上記積層部を覆うように反射層を形成した請求項１，２，４～８のうちのいずれか１つに記載の窒化物半導体発光素子。

１０． 上記反射層は上記積層部を覆うように絶縁膜を介して金属層を形成することにより形成された請求項９記載の窒化物半導体発光素子。

１１． 上記金属層は、上記積層部のｐ型半導体層にそれぞれ形成されたｐオーミック電極を接続する接続電極である請求項１０記載の窒化物半導体発光素子。

１２． 上記反射層は誘電体多層膜からなる請求項９記載の窒化物半導体発光素子。

１３． 上記傾斜側面は、外側に膨らんだ凸曲面である請求項１～１２のうちの

いずれか１つに記載の窒化物半導体発光素子。

１４．　ｎ型窒化物半導体層とｐ型窒化物半導体層の間に、窒化物半導体からなる発光層を有してなる窒化物半導体発光素子において、

少なくとも上記ｐ型窒化物半導体層と上記発光層を含むように台形錐形状の積層体が形成され、該積層体は側面が絶縁されるように金属部材に埋め込まれたことを特徴とする窒化物半導体発光素子。

１５．　ｎ型窒化物半導体層とｐ型窒化物半導体層の間に、窒化物半導体からなる発光層を有してなる窒化物半導体発光素子において、

少なくとも上記ｐ型窒化物半導体層と上記発光層を含むように台形錐形状の積層体が形成されて、その積層体が該積層体の表面に沿って対向するように設けられた金属部材により保持されたことを特徴とする窒化物半導体発光素子。

１６．　上記金属部材の上記積層体の反対側に位置する面が、平坦な面である請求項１又は２記載の窒化物半導体発光素子。

１７．　上記ｎ型窒化物半導体層の対向する２つの面のうちの上記積層体の反対側に位置する面に透明電極が形成されている請求項１～３のうちのいずれか１つに記載の窒化物半導体発光素子。

１８．　上記透明電極はＩＴＯである請求項４記載の窒化物半導体発光素子。

１９．　上記ｐ型窒化物半導体層とオーミック接触するように上記積層体と上記金属部材の間に形成されたｐ型電極は、Ｒｈを含む請求項１～５のうちのいずれか１つに記載の窒化物半導体発光素子。

２０．　上記積層体は上記ｎ型窒化物半導体層の一部を含んで構成されている請求項１～６のうちのいずれか１つに記載の窒化物半導体発光素子。

２１．　上記積層体は上記ｎ型窒化物半導体層の全てを含むように構成されている請求項１～６のうちのいずれか１つに記載の窒化物半導体発光素子。

２２．　上記金属部材の厚さは５０μｍ以上である請求項１～８のうちのいずれか１つに記載の窒化物半導体発光素子。

２３．　上記積層体を複数個備えた請求項１～９のうちのいずれか１つに記載の窒化物半導体発光素子。

２４．　上記複数の積層体は、共通のｎ型窒化物半導体層の上に設けられている

請求項１０記載の窒化物半導体発光素子。

２５．　上記ｎ型窒化物半導体は、各積層体ごとに分離されている請求項１０記載の窒化物半導体発光素子。

２６．　上記金属部材は、Ｔｉ、Ａｇ、Ａｌ、Ｎｉ、Ｐｔ、Ａｕ、Ｒｈ、Ｃｕ、Ｗ等からなる群から選択された金属又はその金属を少なくとも含む合金からなる請求項１～１２のうちのいずれか１つに記載の窒化物半導体発光素子。

２７．　基板上にｎ型半導体層と発光層とｐ型半導体層を形成する第１工程と、

上記ｐ型半導体層と上記発光層とを含むように台形錐形状の発光領域を形成する第２工程と、

上記発光領域を覆うように金属部材を形成する第３工程と、

上記基板を除去する第４工程と、

上記発光領域の間で金属部材を切断することにより、発光素子ごとに分離する第５工程とを含むことを特徴とする発光素子の製造方法。

２８．　上記第３工程において、上記金属部材をメッキにより形成する請求項１４記載の発光素子の製造方法。

２９．　第１導電型層と第２導電型層とに挟まれた発光層を有する構造を備えた半導体発光素子において、

前記第１，２導電型層、発光層の少なくとも一部が含まれて、断面において構造部幅の大きい底面側と小さい上面側を備えて、対向する側面が互いに傾斜した構造部が設けられると共に、

前記構造部側面が、底面側よりも上面側の幅が大きな第１側面と、上面側よりも底面側の幅が大きな第２側面と、を有することを特徴とする半導体発光素子。

３０．　前記第１側面が、底面において構成辺に挟まれた角部に設けられていることを特徴とする請求項２９記載の半導体発光素子。

３１．　前記構造部が、その内部に前記発光層を備えることを特徴とする請求項２９記載の半導体発光素子。

３２．　前記構造部の底面側が方形状、多角形状であり、該形状の底面側構成辺に前記第２側面が設けられ、該形状の角部が前記第１側面が設けられている

ことを特徴とする請求項２９記載の半導体発光素子。

３３．　前記構造部が錐体形状を有することを特徴とする請求項２９記載の発光素子。

３４．　前記第１側面が、構造部外側に向かって凸な湾曲面であることを特徴とする請求項２９記載の半導体発光素子。

３５．　前記構造部上面、底面における第１側面が丸みを帯びた構成辺を形成し、該丸みの曲率半径が底面側より上面側が大きいことを特徴とする請求項２９記載の半導体発光素子。

３６．　前記発光素子が、前記構造部を複数有して、各構造部がほぼ同時に発光されるように電極構造が形成されていることを特徴とする請求項２９記載の発光素子。

３７．　前記発光素子が、構造部上面に同一面側に正負一対の電極を有することを特徴とする請求項２９記載の発光素子。

３８．　前記発光素子の一方の電極は、前記構造部側面の一部を覆って形成されていることを特徴とする請求項３７記載の発光素子。

３９．　前記構造部が基板上に互いに分離されて複数設けられ、各構造部がほぼ同時に発光できるように電極が設けられていることを特徴とする請求項２９記載の発光素子。

４０．　前記発光素子が構造部上面側を実装面側として、実装基体に載置され、前記構造部に設けられた一方の電極は、基板面の上に設けられ、他方の電極は、互いに分離された複数構造部上面に接続するような配線が前記実装基体側に設けられていることを特徴とする請求項３７記載の発光素子。

４１．　前記発光素子が、構造部上面、底面側に対向配置された一対の電極を有し、それぞれ第１，２導電型層表面に設けられていることを特徴とする請求項２９記載の発光素子。

４２．　前記発光素子の構造部側面を覆う透光性絶縁膜を介して充填部材を有することを特徴とする請求項４１記載の発光素子。

４３．　前記発光素子が、複数の構造部を有し、該構造部間に凸状の充填部材を有することを特徴とする請求項４１記載の発光素子。

４４．　前記発光素子の構造部が発光層を内部に有し、前記充填部材が前記発光層よりも構造部底面側に突出して形成されていることを特徴とする請求項４２記載の発光素子。

４５．　請求項２９乃至４４記載の発光素子が載置される載置部を有する発光装置であって、前記載置部に、発光素子が支持基板上に実装されて、載置されていることを特徴とする発光装置。

４６．　請求項２９乃至４４記載の発光素子を用いた発光装置であって、発光装置には、発光素子から光の一部を、それとは異なる波長の光に変換する光変換部材を有することを特徴とする発光装置。

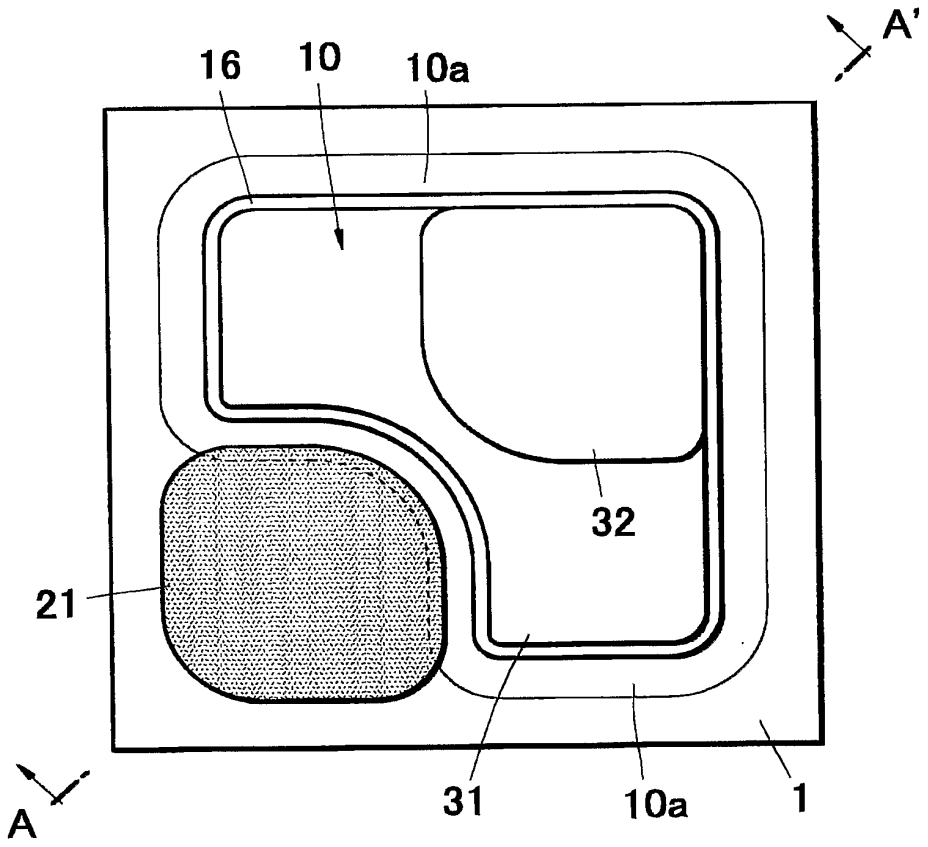
４７．　前記光変換部材が、Ａｌを含み、かつＹ、Ｌｕ、Ｓｃ、Ｌａ、Ｇｄ、Ｔｂ、Ｅｕ及びＳｍから選択された少なくとも一つの元素と、Ｇａ及びＩｎから選択された一つの元素とを含むアルミニウム・ガーネット系蛍光体であって、さらに希土類元素から選択された少なくとも一つの元素を含有するアルミニウム・ガーネット系蛍光体を有することを特徴とする請求項４５又は４６記載の発光装置。

４８．　前記光変換部材が、$(Re_{1-x}R_x)_3(Al_{1-y}Ga_y)_5O_{12}$（$0<x<1$、$0\leqq y\leqq 1$、但し、Ｒｅは、Ｙ，Ｇｄ,Ｌａ，Ｌｕ，Ｔｂ，Ｓｍからなる群より選択される少なくとも一種の元素であり、ＲはＣｅ又はＣｅとＰｒである）であらわされる蛍光体を有することを特徴とする請求項４５又は４６記載の発光装置。

４９．　前記光変換部材が、Ｎを含み、かつＢｅ、Ｍｇ、Ｃａ、Ｓｒ、Ｂａ、及びＺｎから選択された少なくとも一つの元素と、Ｃ、Ｓｉ、Ｇｅ、Ｓｎ、Ｔｉ、Ｚｒ、及びＨｆから選択された少なくとも一つの元素とを含み、希土類元素から選択された少なくとも一つの元素で付活された窒化物系蛍光体を有する請求項４５又は４６に記載の発光装置。

５０．　前記窒化物系蛍光体が、一般式$L_XSi_YN_{(2/3X+4/3Y)}$：Ｅｕ若しくは$L_XSi_YO_ZN_{(2/3X+4/3Y-2/3Z)}$：Ｅｕ（Ｌは、Ｓｒ若しくはＣａ、又は、Ｓｒ及びＣａ、のいずれか。）で表されることを特徴とする請求項４５又は４６に記載の発光装置。

図 1



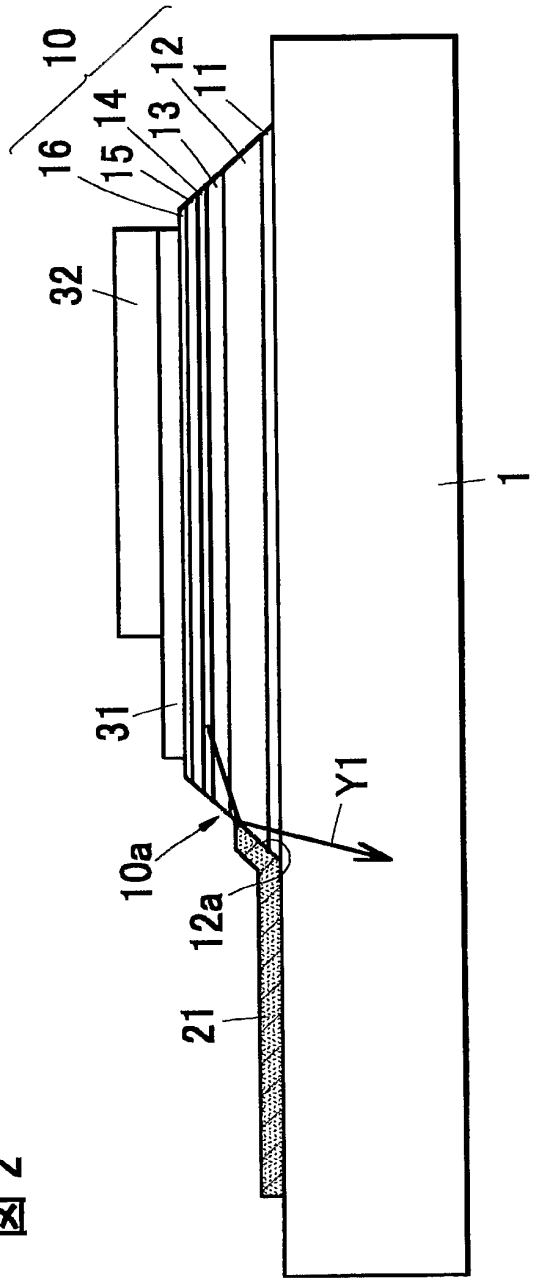
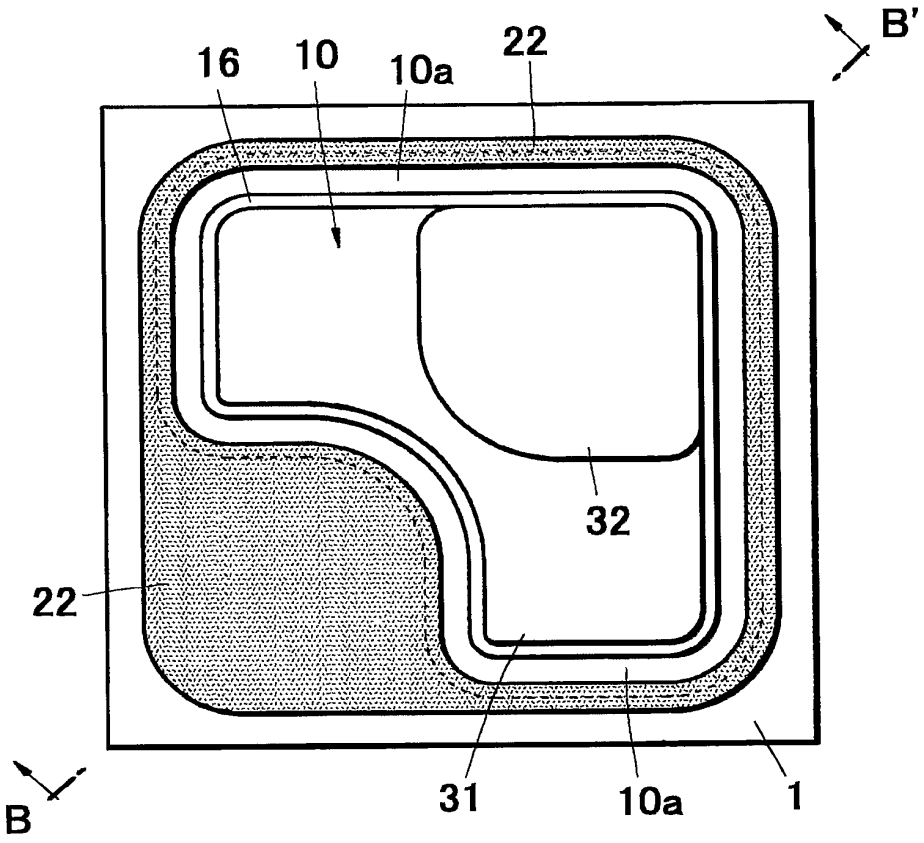


図 2

図 3



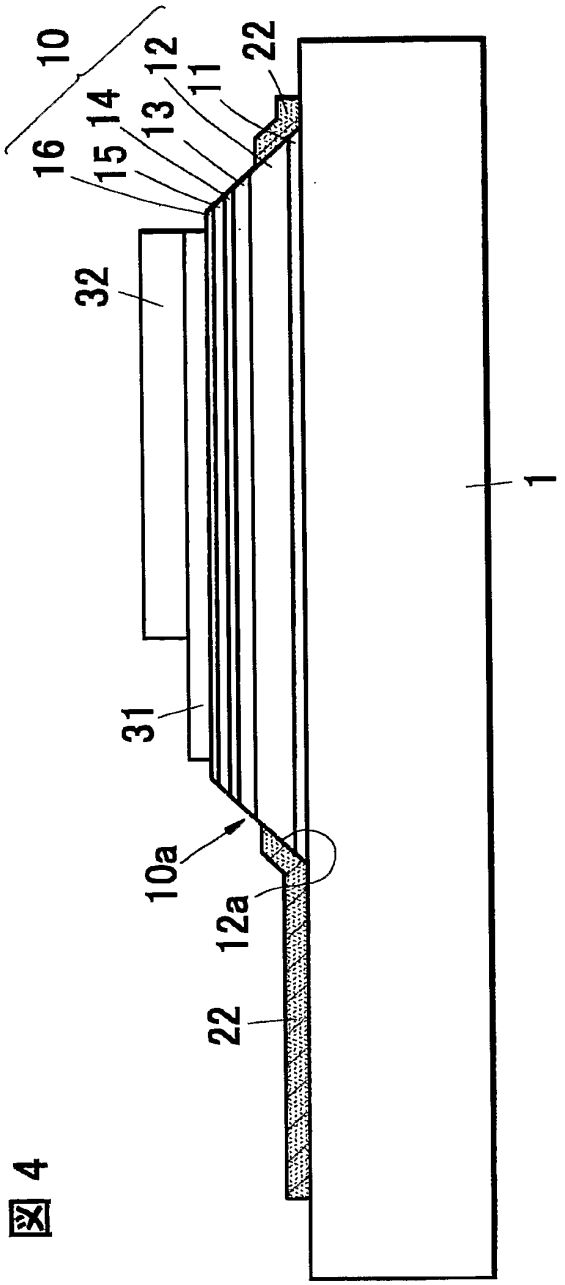


図 4

図 5

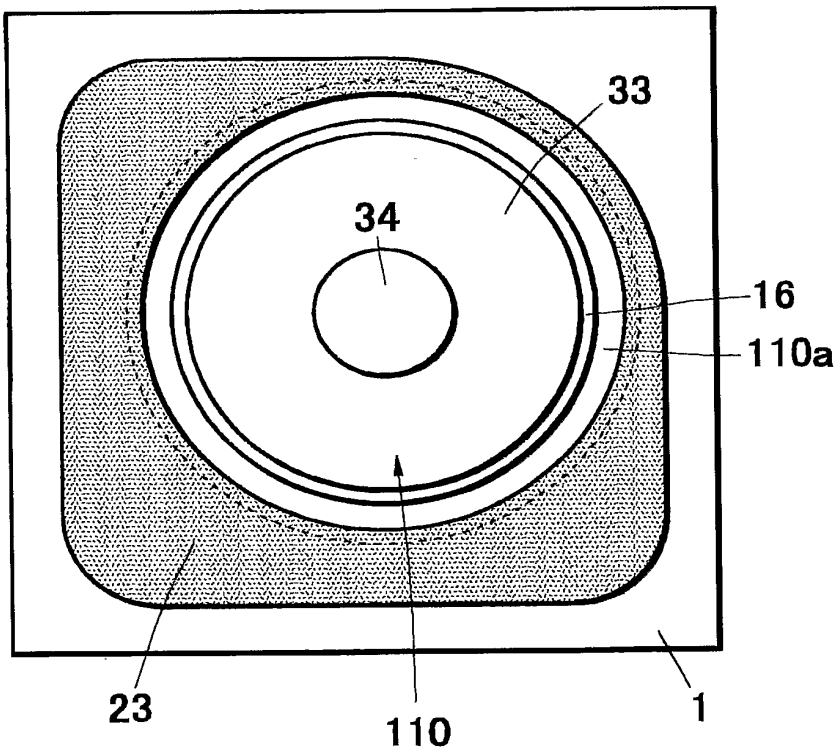


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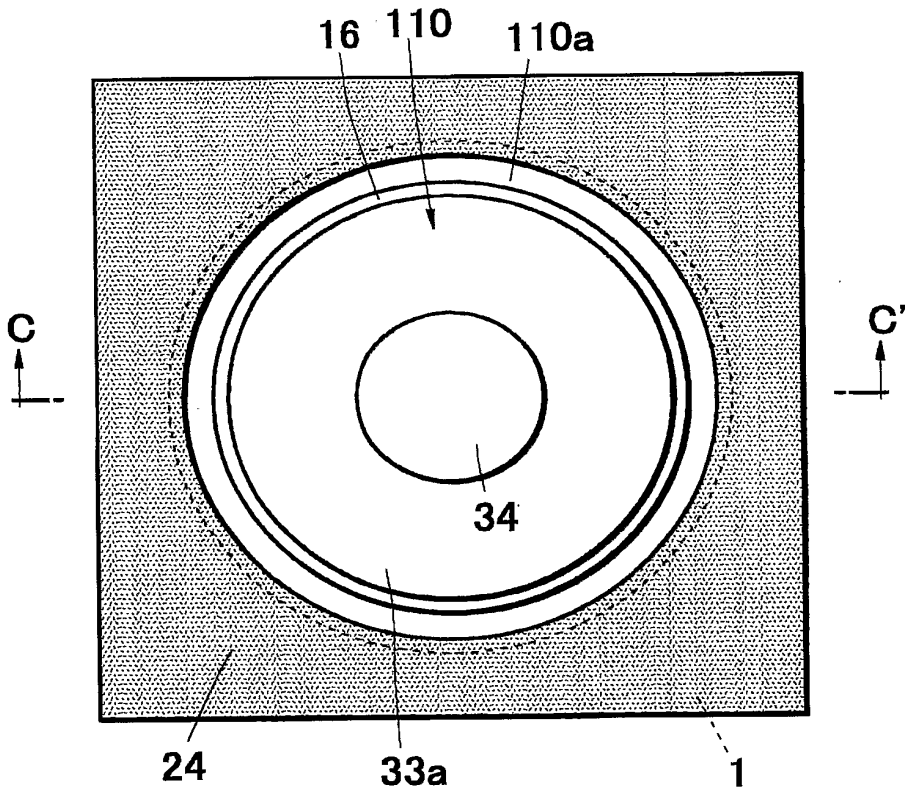


図 7

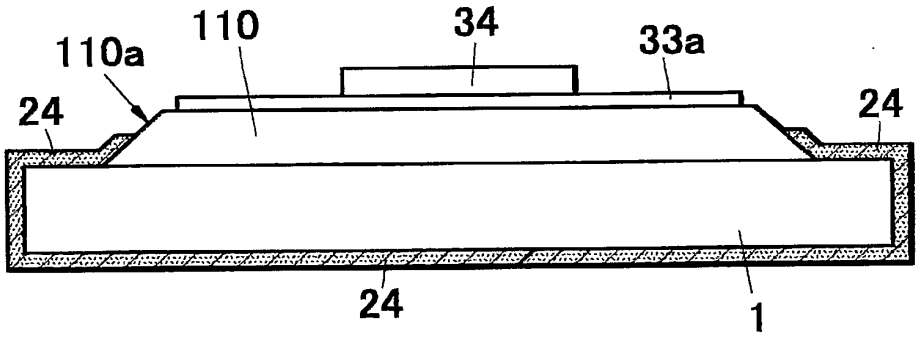


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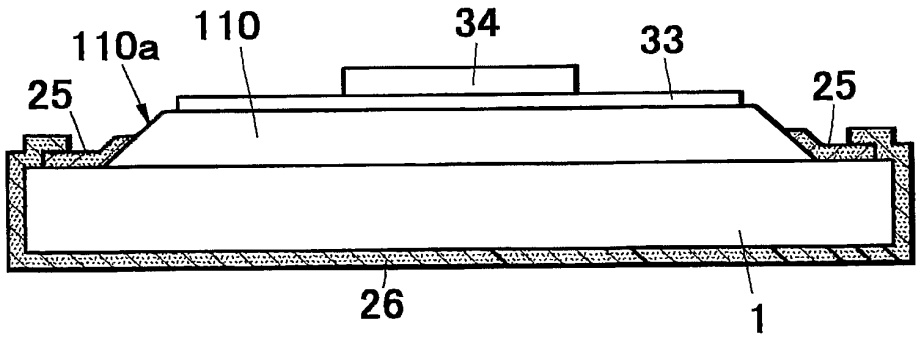


図 9

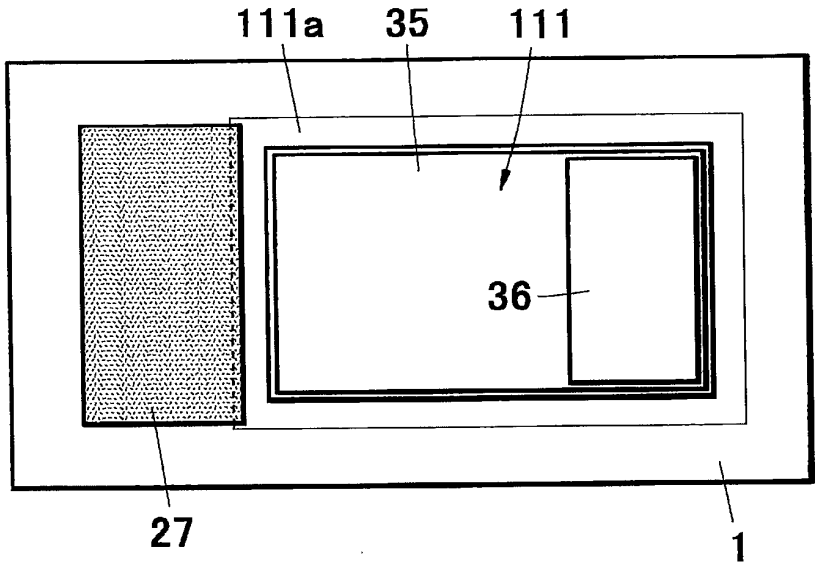


図 10

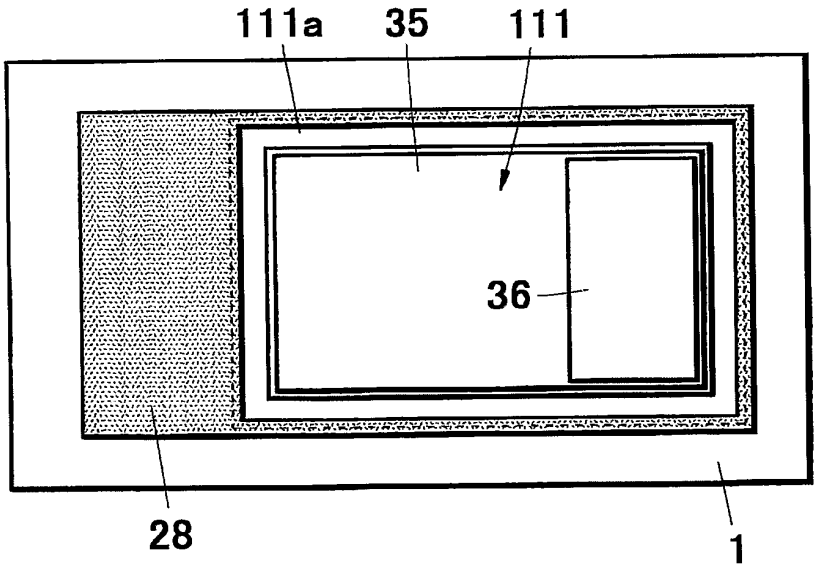


図 11

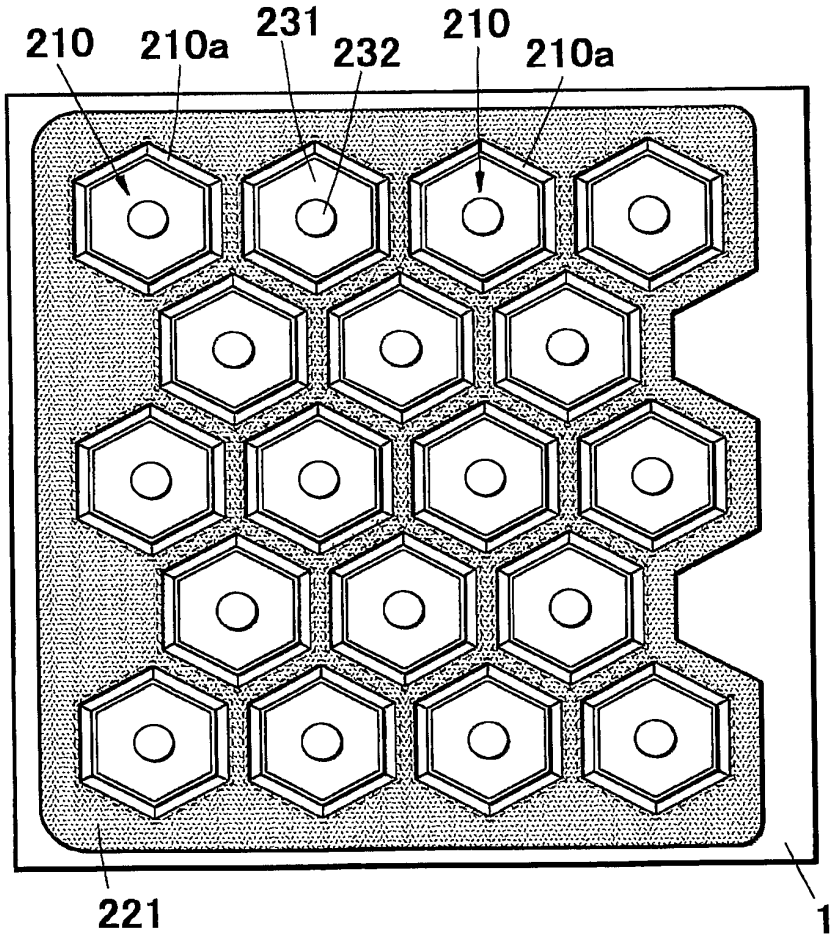
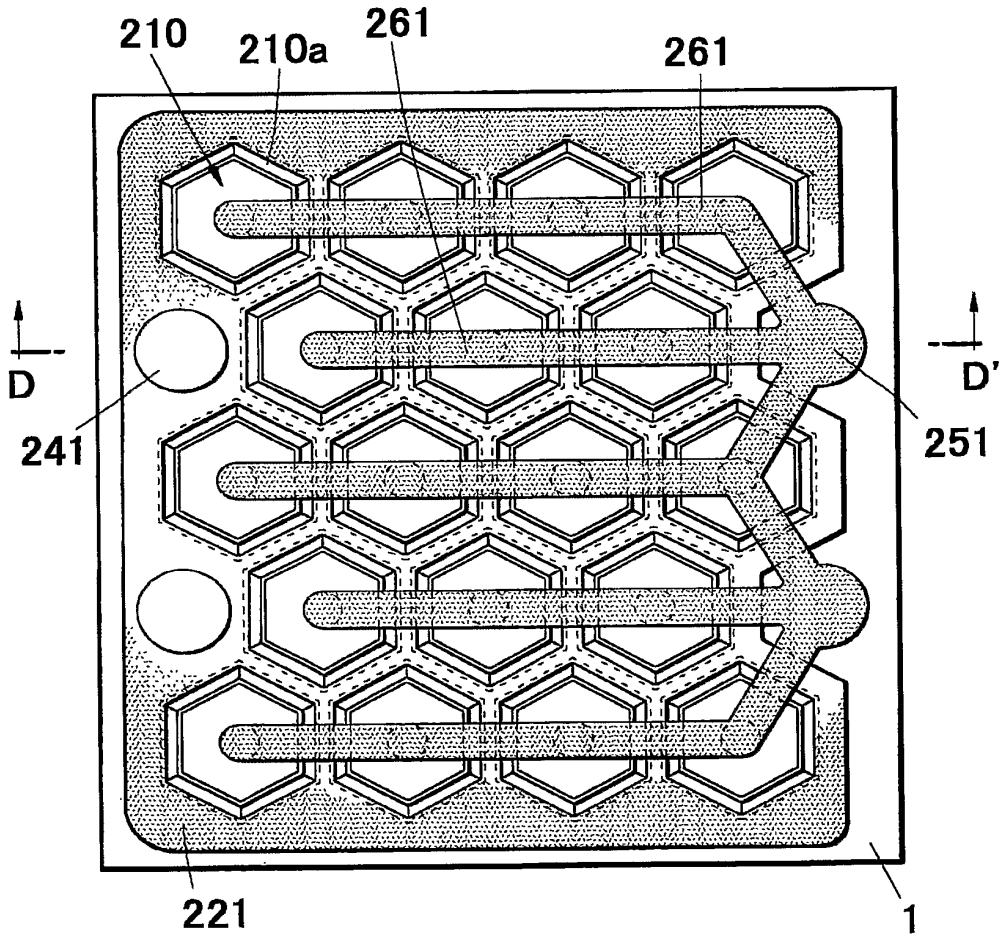


図 12



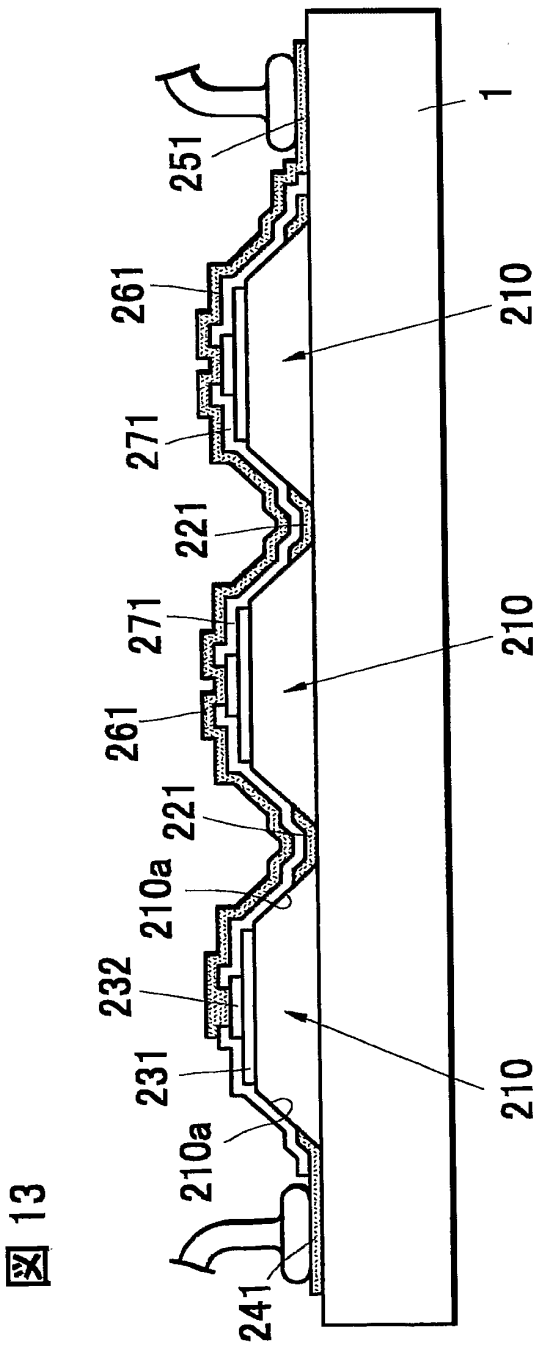


図 13

図 14

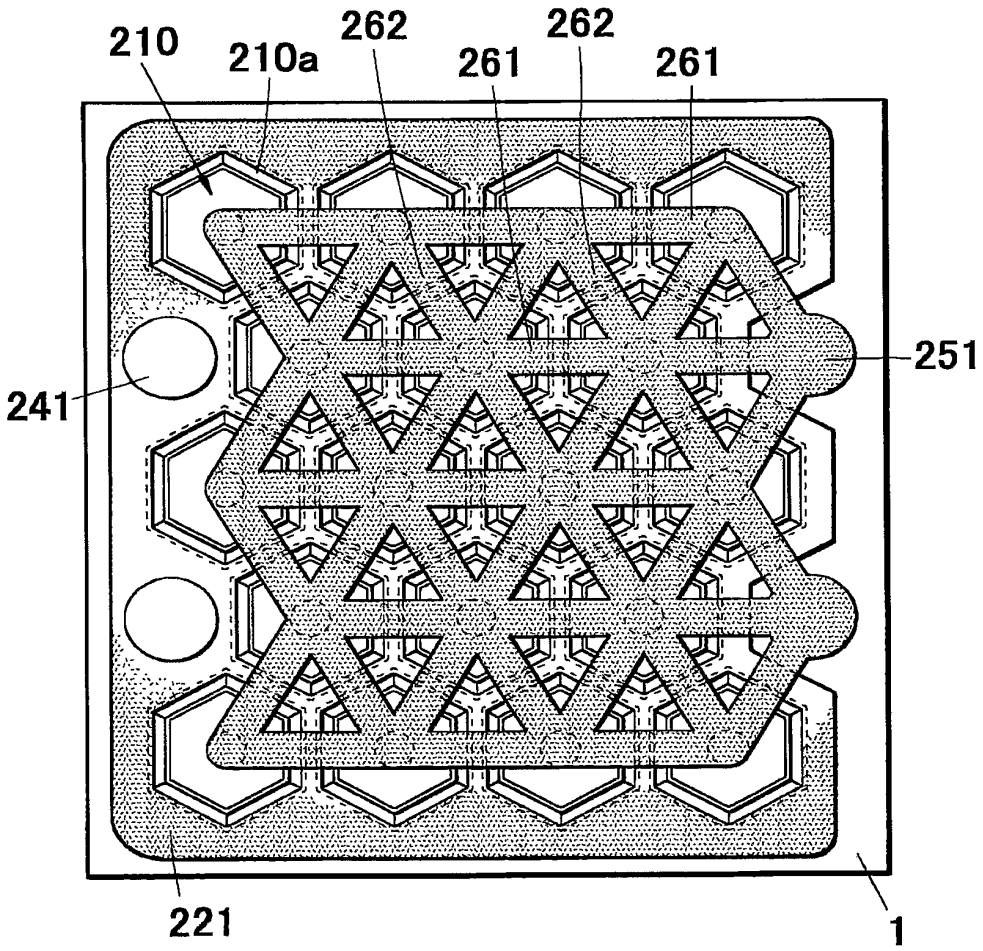


図 15

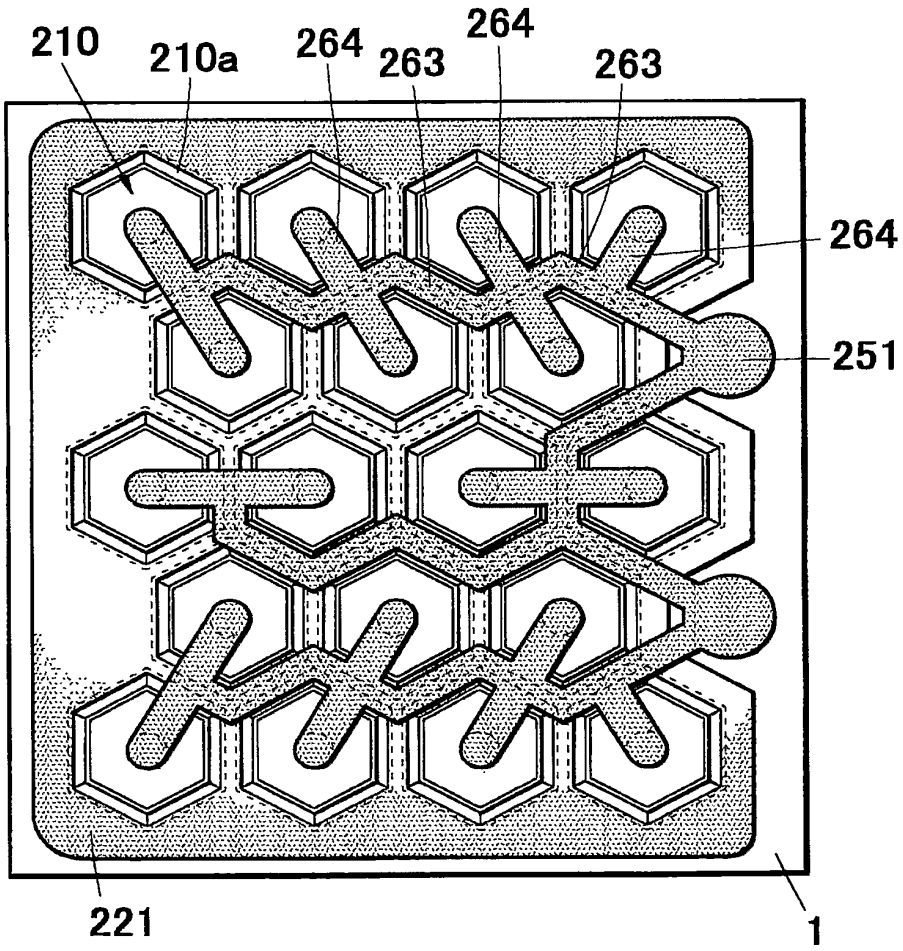


図16A

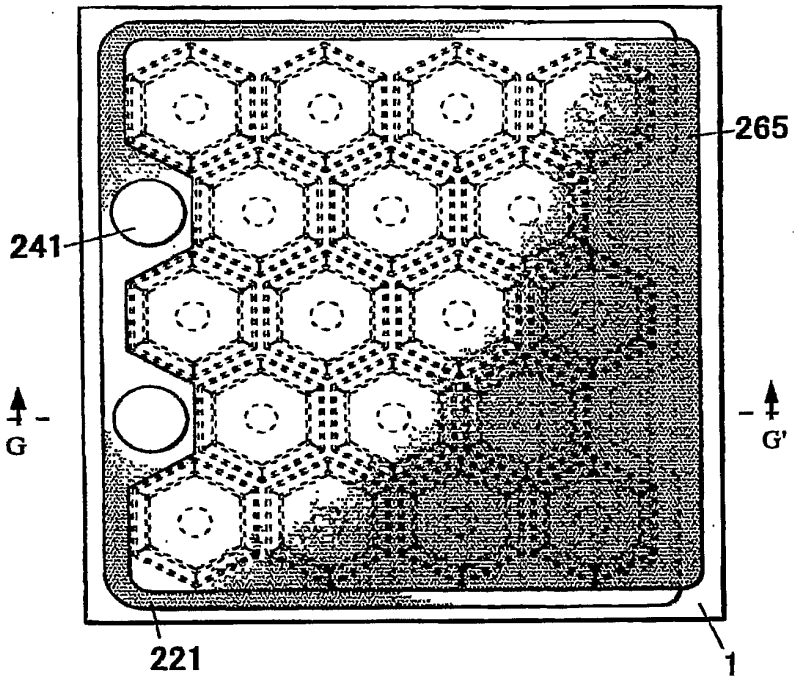

265
241
G
G'
221
1

図16B

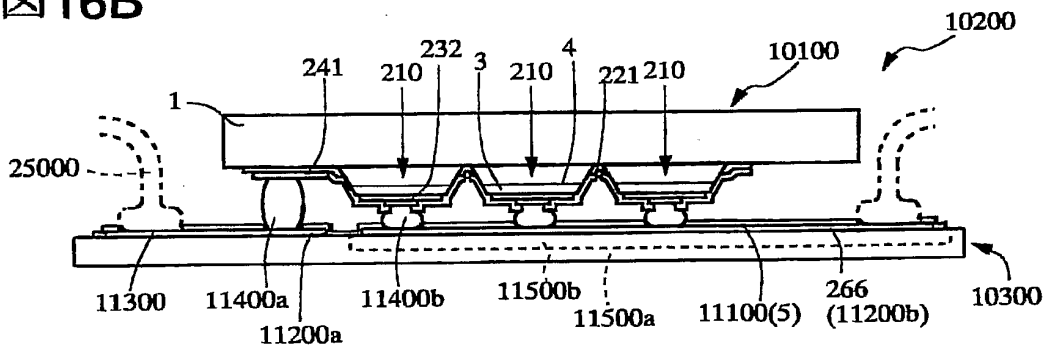

10200
10100
241
210
232
3
210
4
221
210
1
25000
11300
11400a
11200a
11400b
11500b
11500a
11100(5)
266
(11200b)
10300

図 17

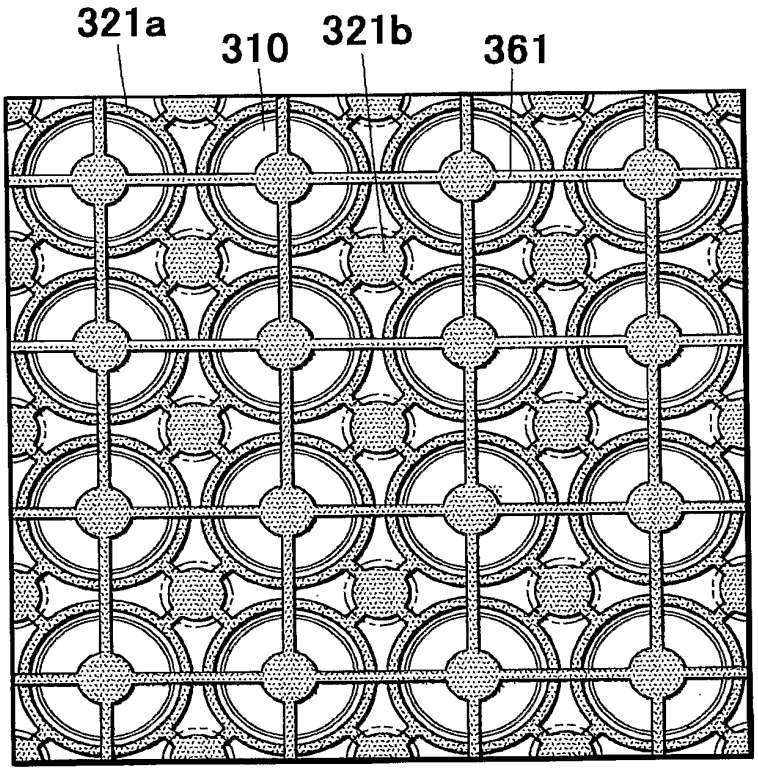


図 18

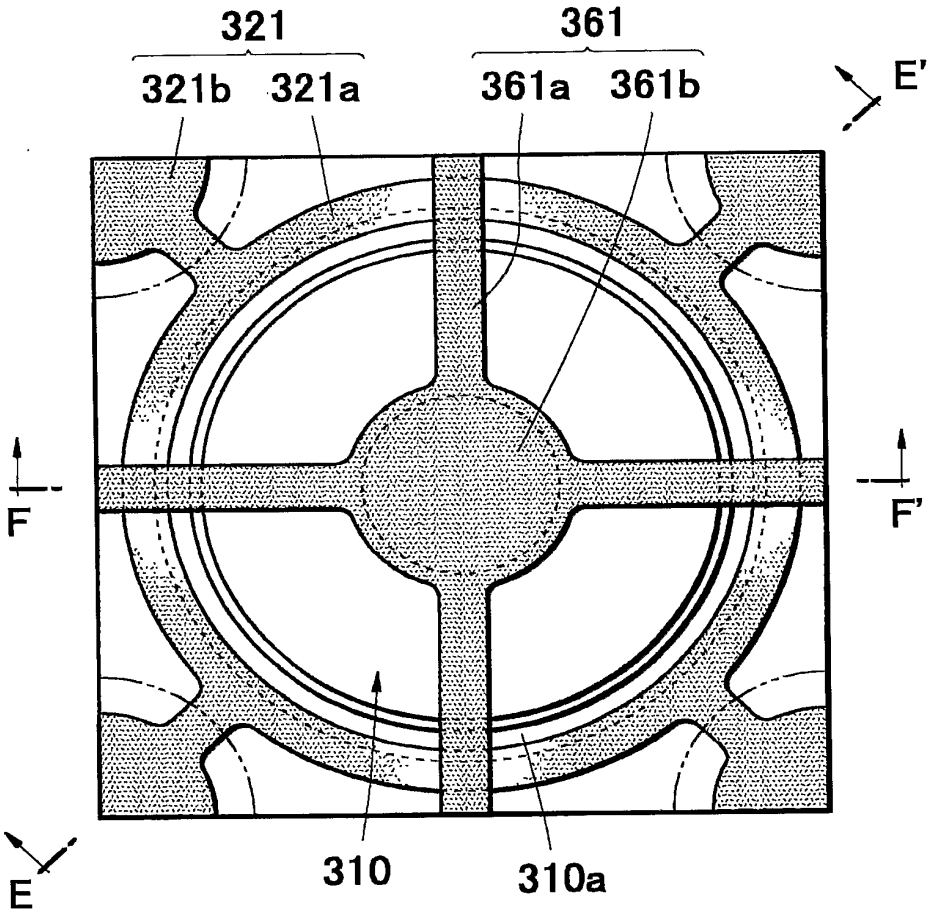


図 19 A

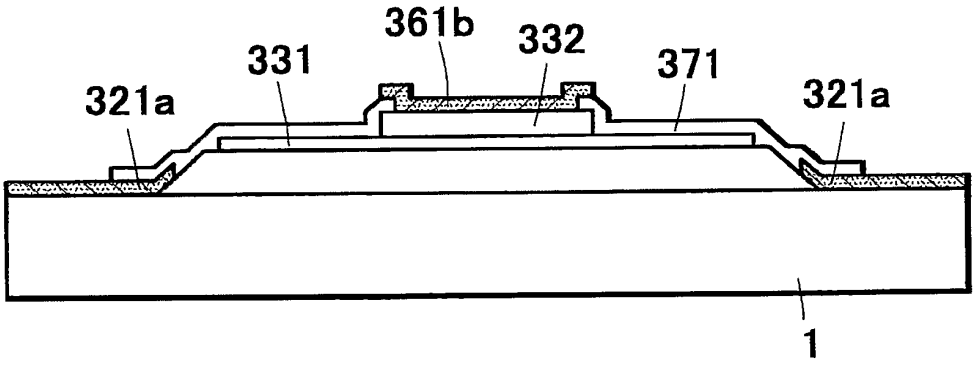

361b
332
331
371
321a
321a
1

図 19 B

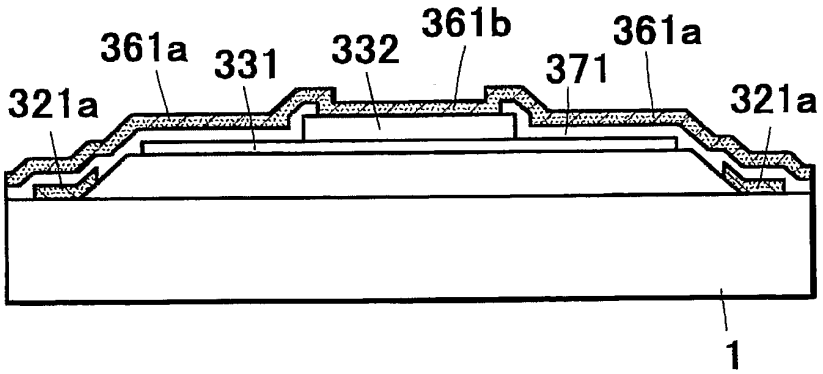

361b
361a
361a
331
332
371
321a
321a
1

図 20 A

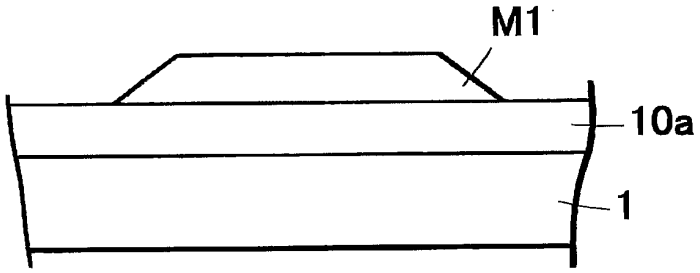


図 20 B

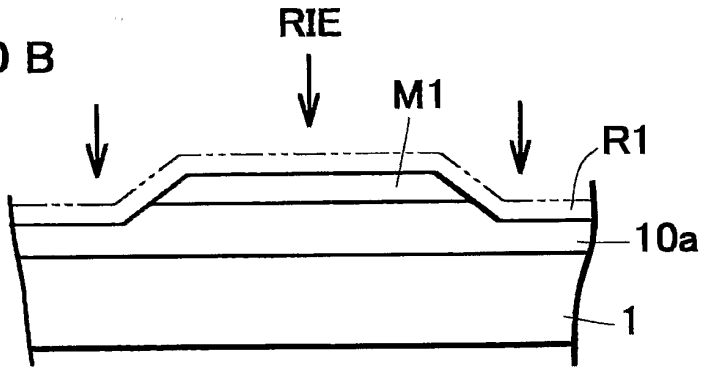
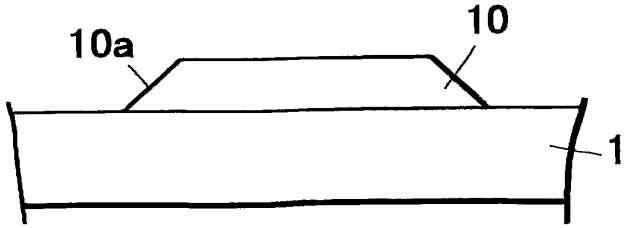


図 20 C



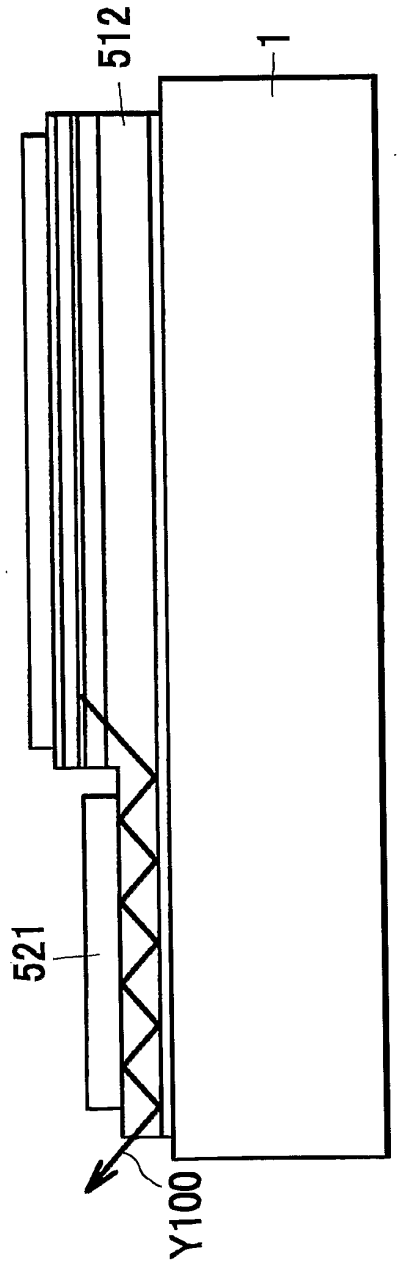


図 21

図 22

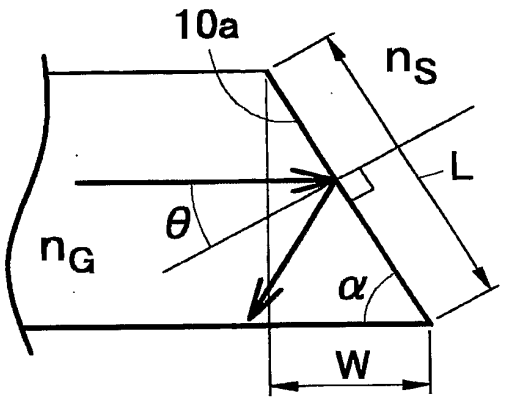


図 23 A

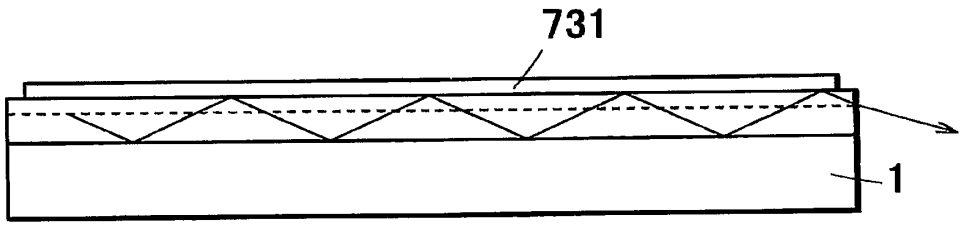


図 23 B

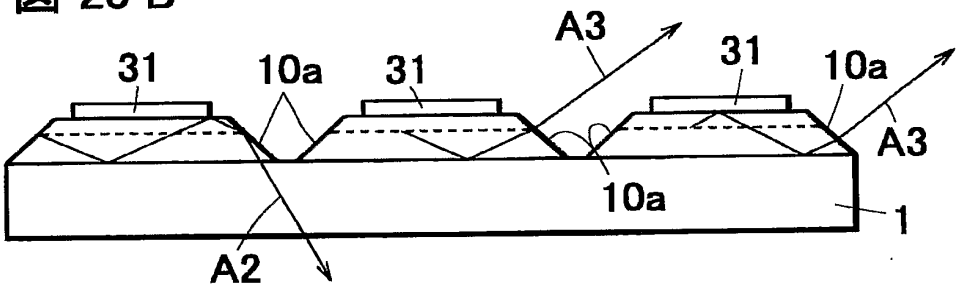


図 23 C

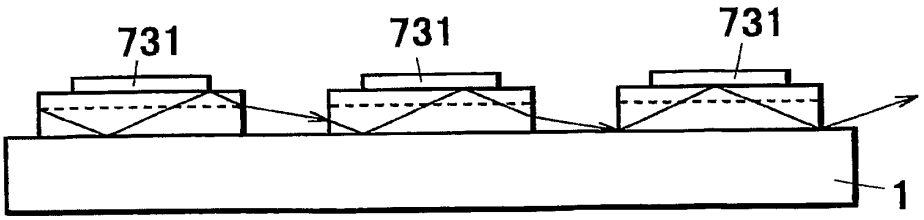


図 24

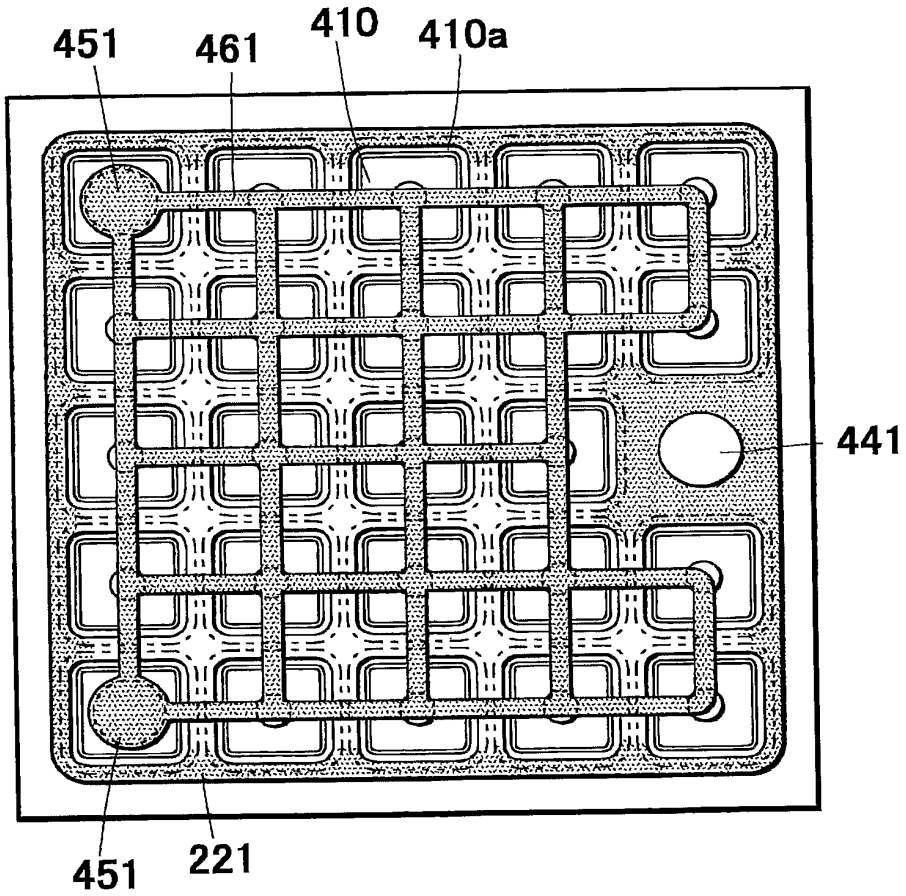


図 25

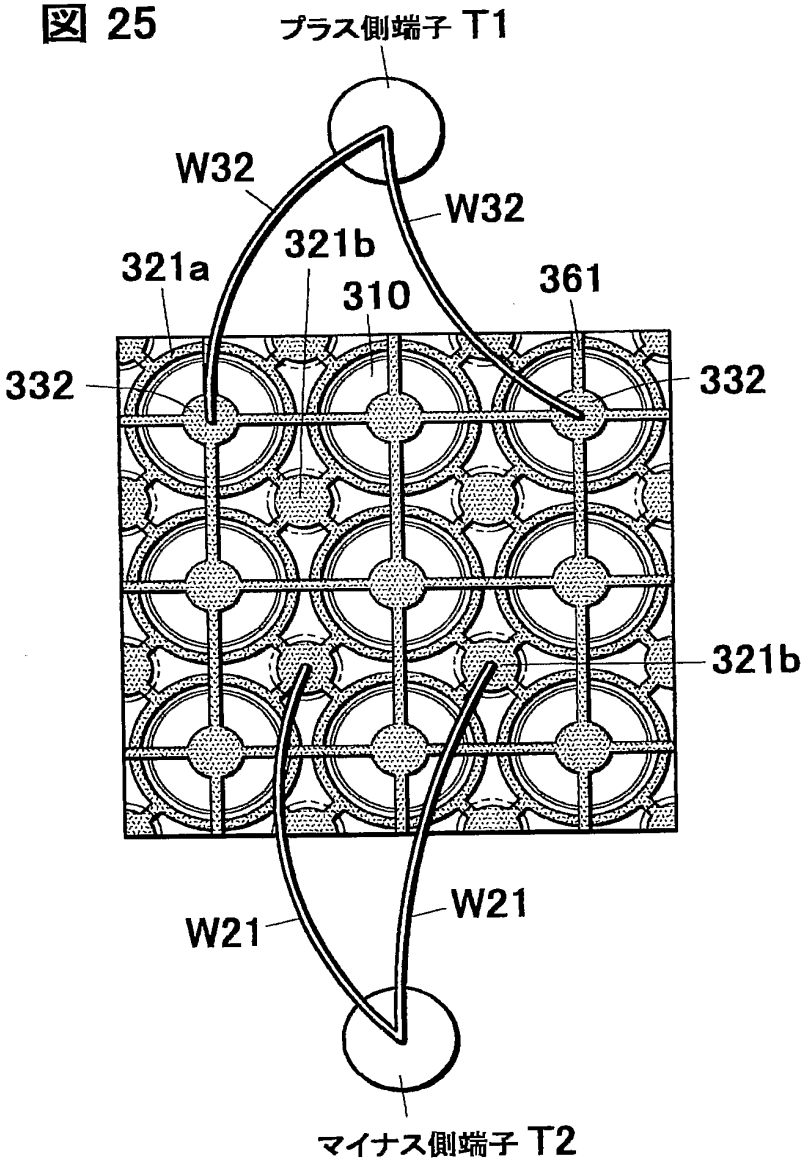

プラス側端子 T1
W32
W32
321a
321b
310
361
332
332
321b
W21
W21
マイナス側端子 T2

図 26

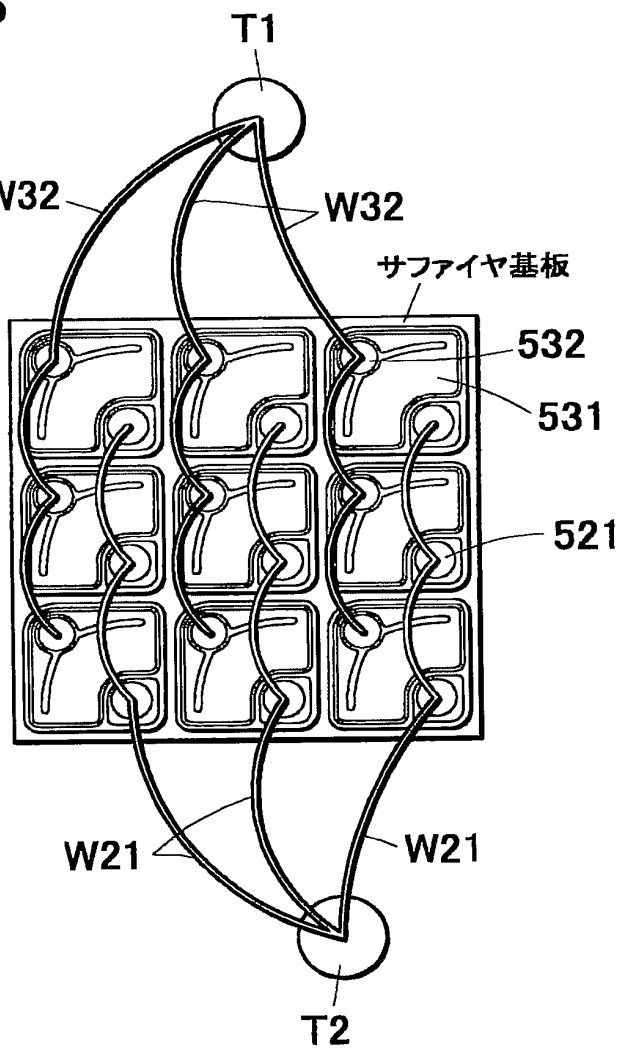
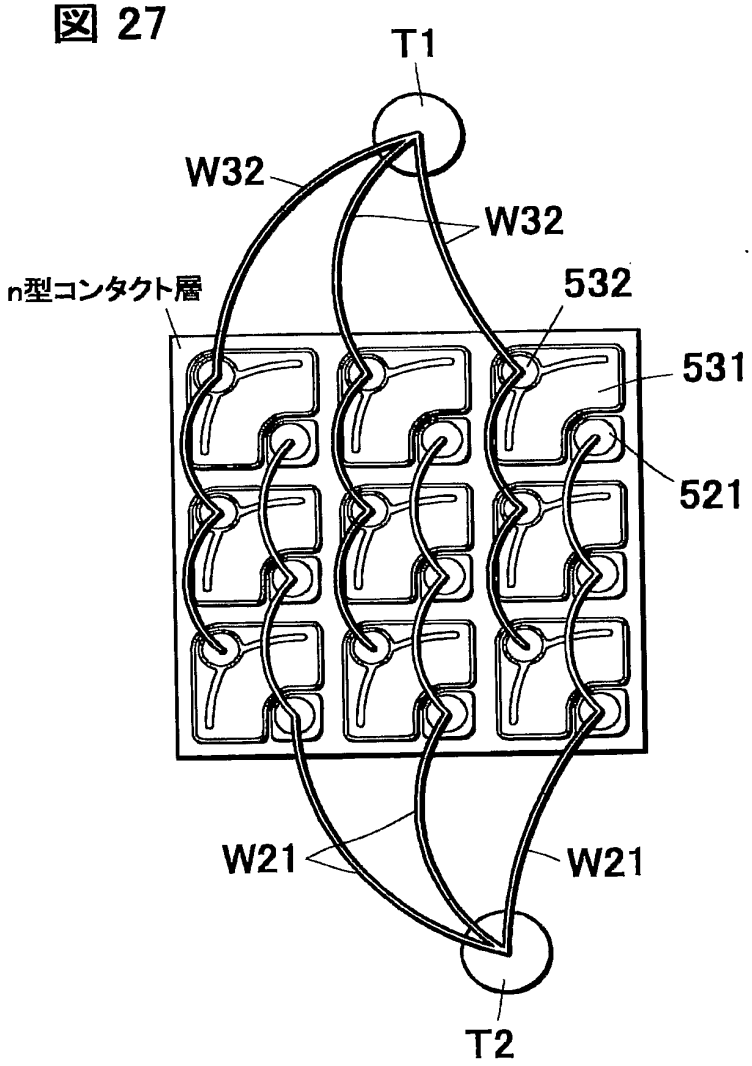


図 27



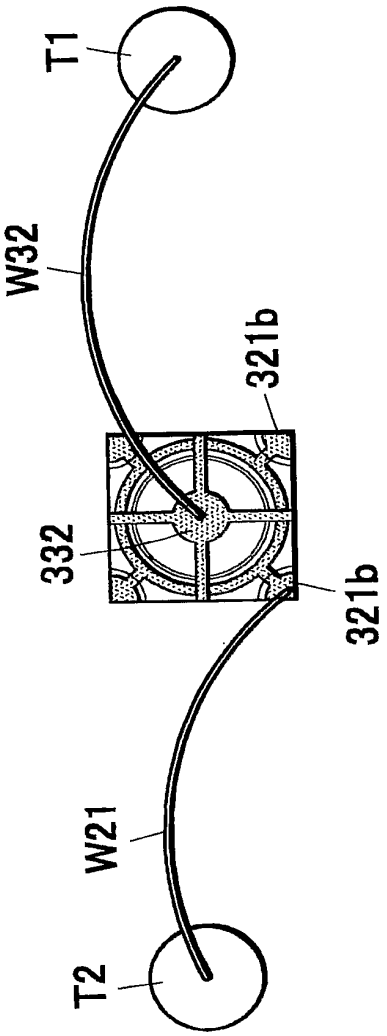


図 28

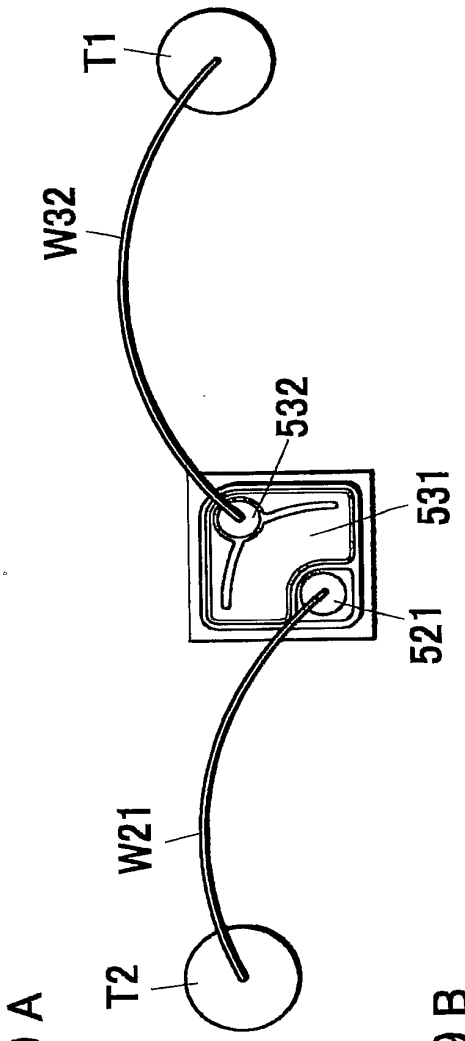


図 29 A

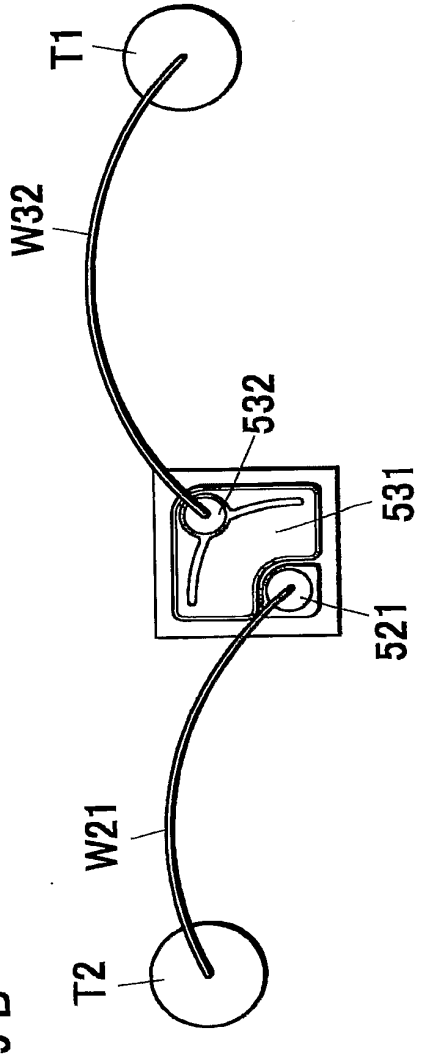


図 29 B

図 30

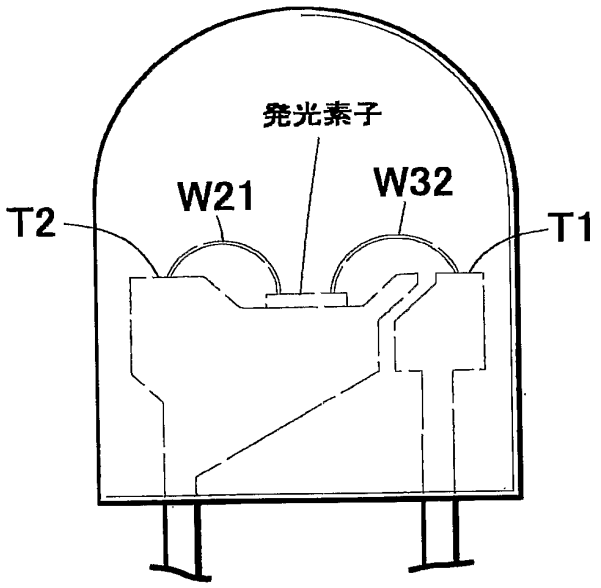


図 31

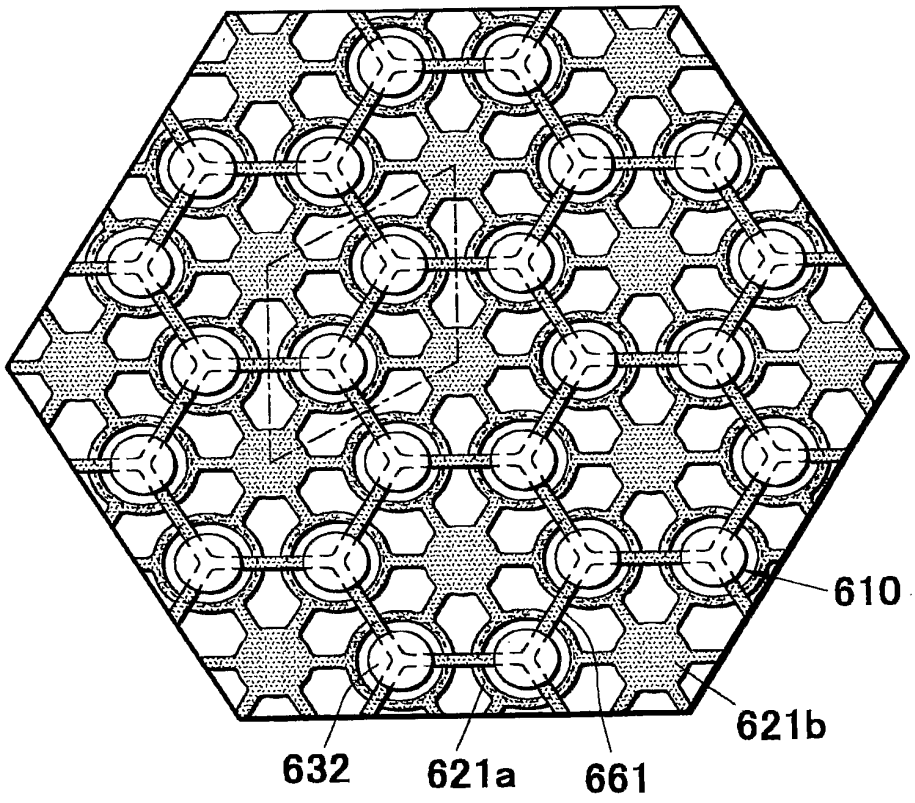


図 32

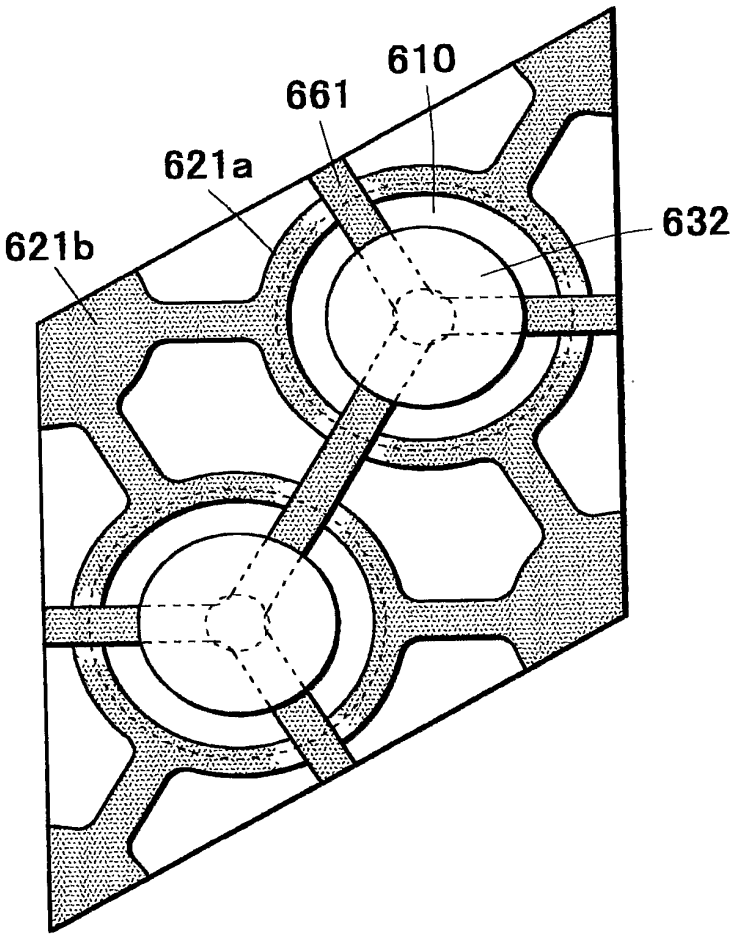


図33A

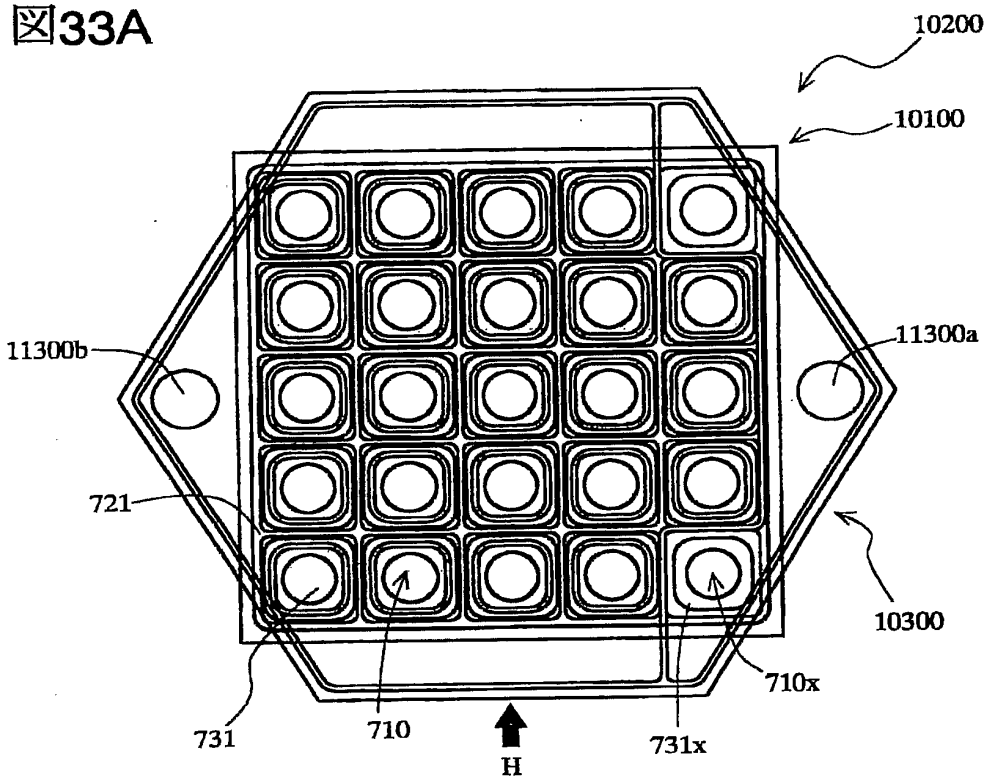

10200
10100
11300b
11300a
721
10300
710x
731
710
731x
H

図33B

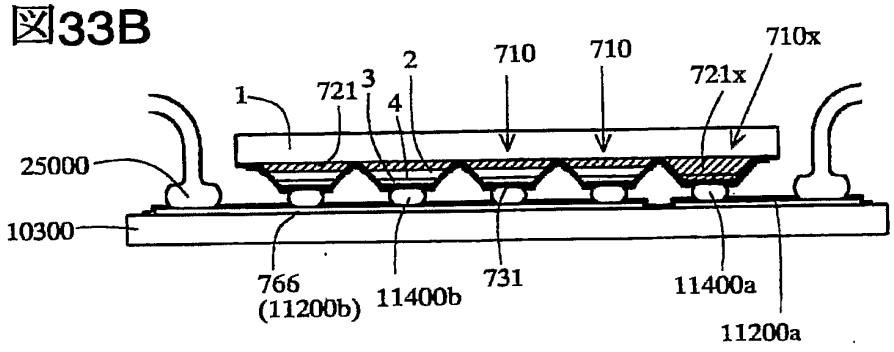

1
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3
2
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710x
25000
10300
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(11200b)
11400b
731
11400a
11200a

図 34

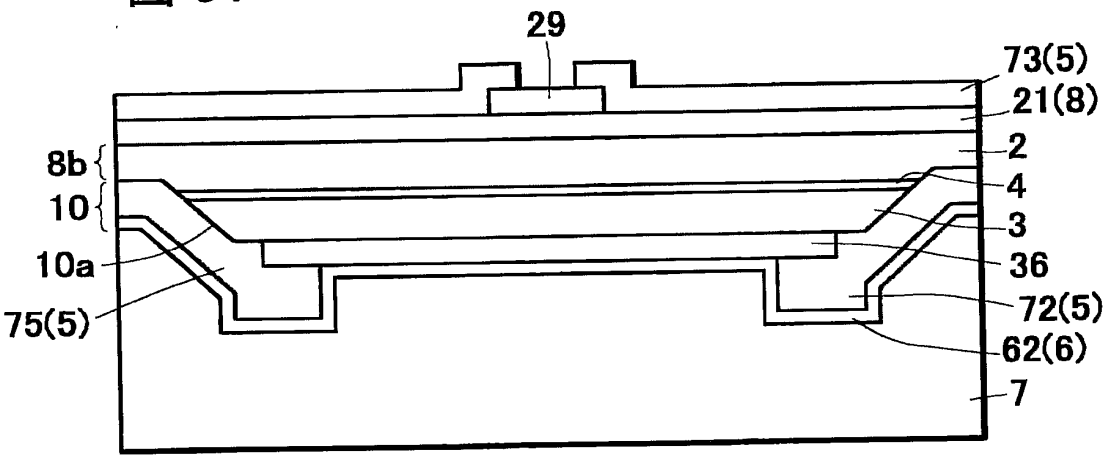


図 35

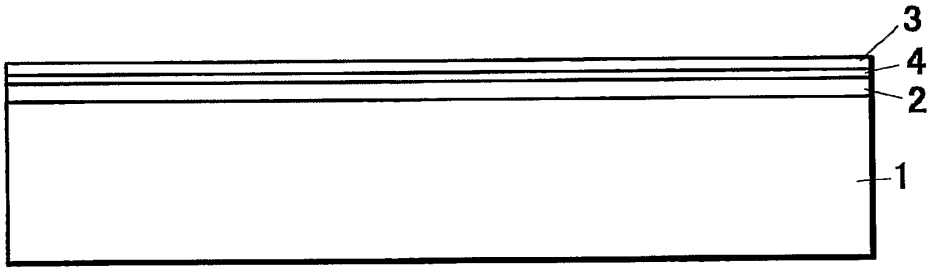


図 36

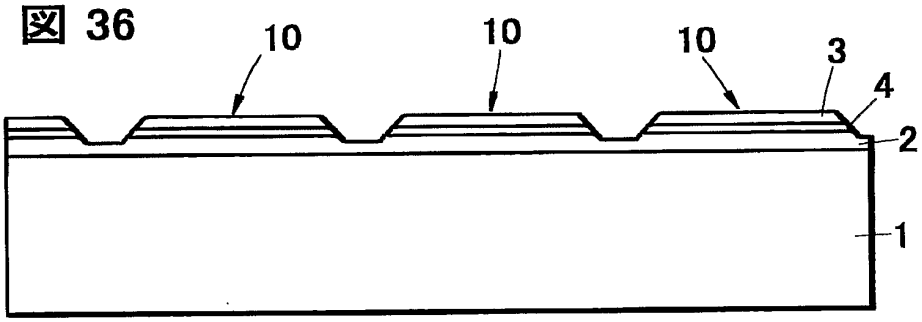


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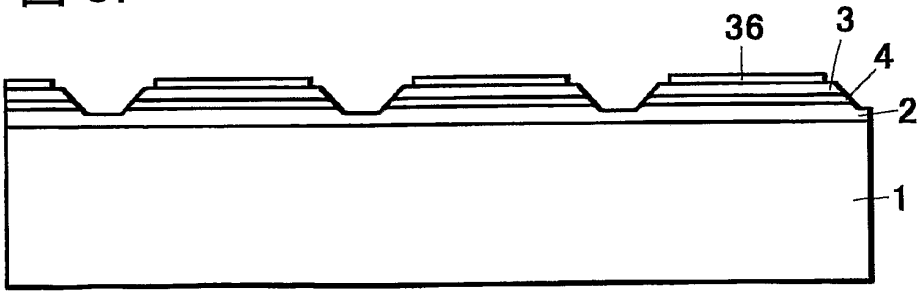


図 38

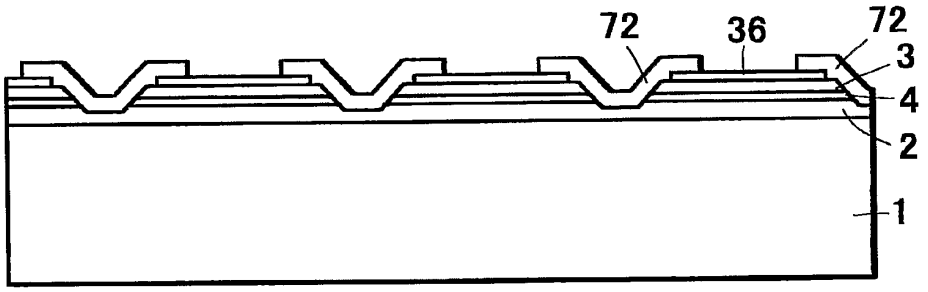


図 39

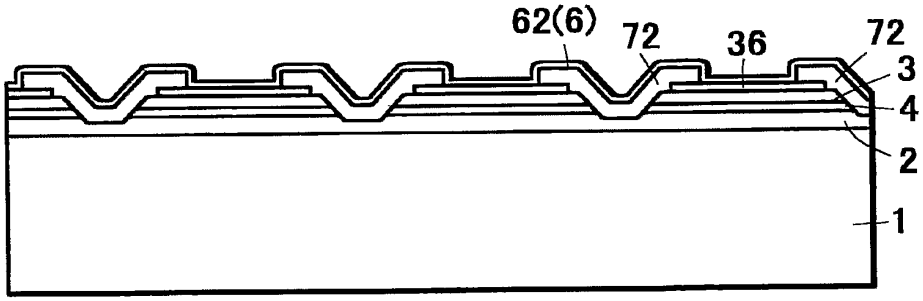


図 40

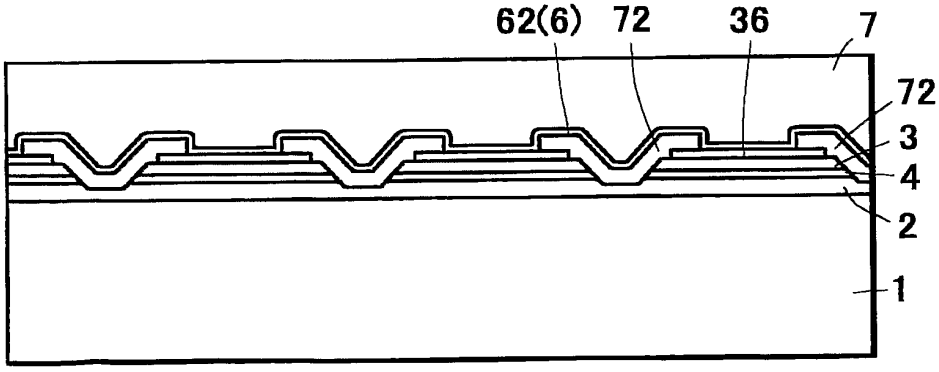


図 41

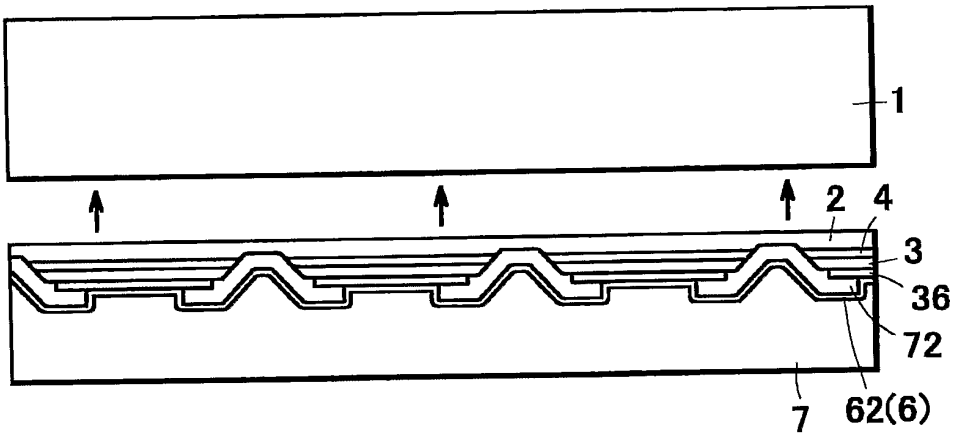


図 42

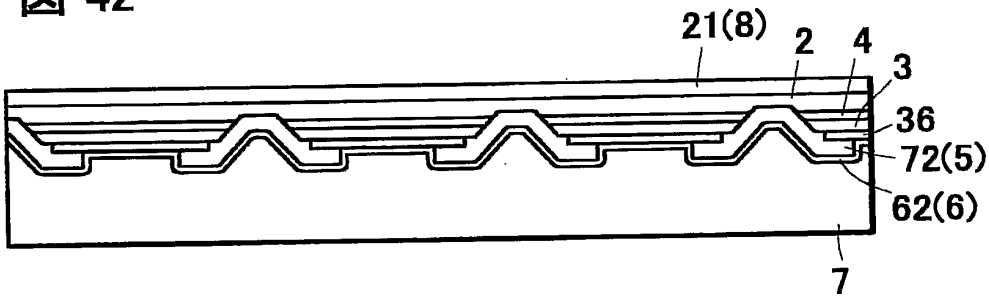


図 43

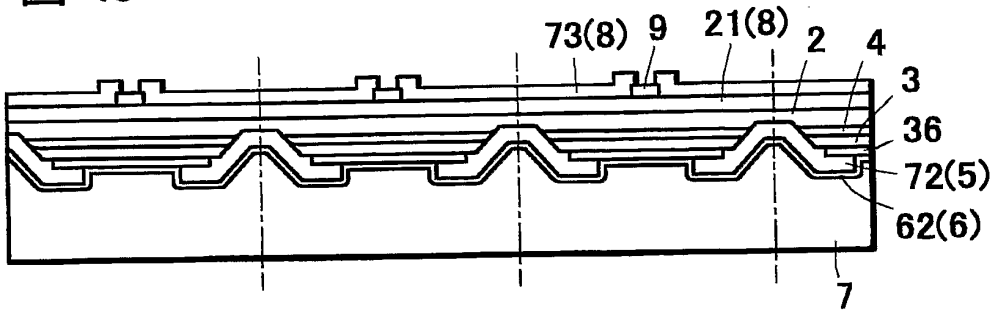


図 44 A

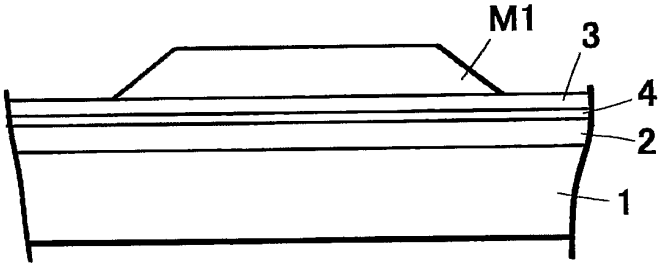


図 44 B

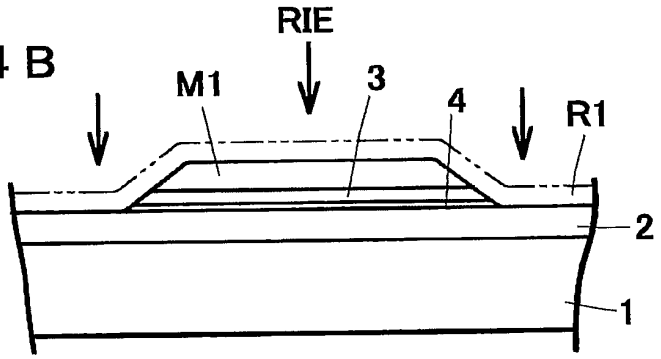


図 44 C

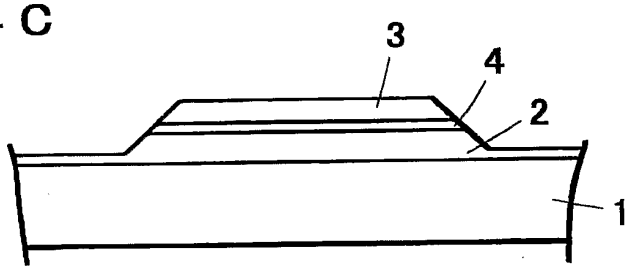


図 45

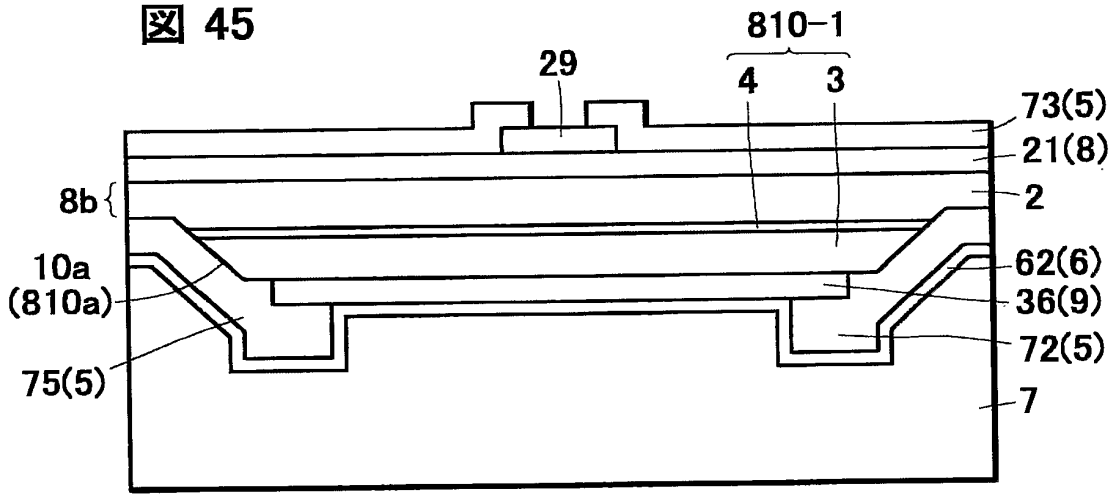

810-1
29
4
3
73(5)
21(8)
8b
2
10a
(810a)
62(6)
36(9)
72(5)
75(5)
7

図 46

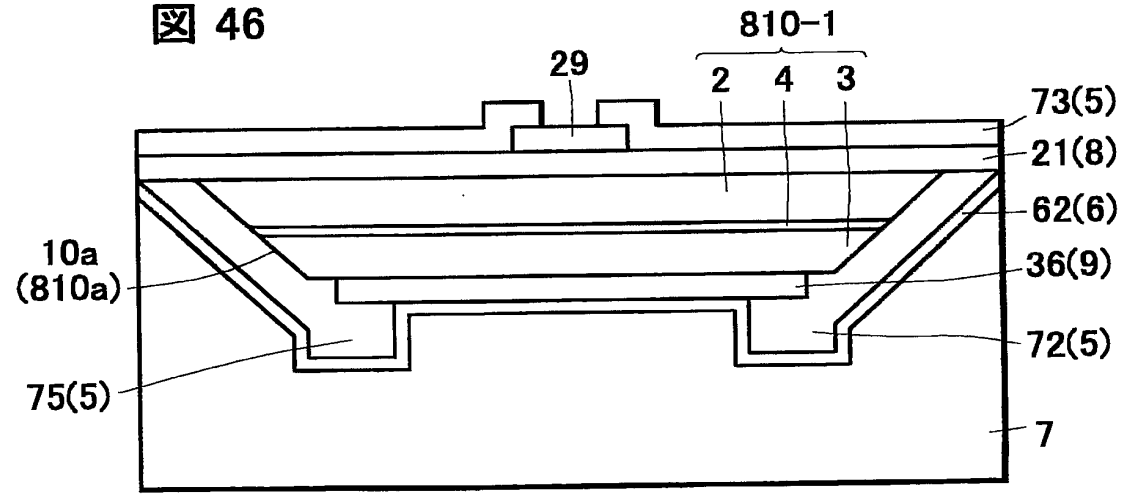

810-1
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2
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73(5)
21(8)
62(6)
10a
(810a)
36(9)
72(5)
75(5)
7

図 47

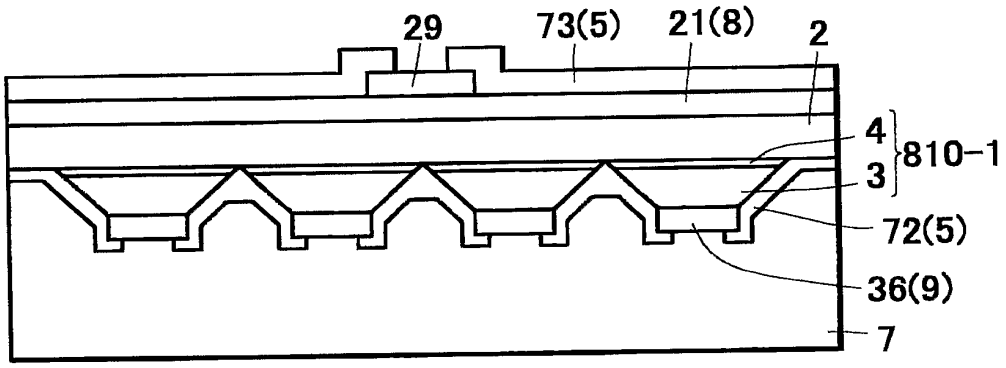

29
73(5)
21(8)
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3
810-1
72(5)
36(9)
7

図 48

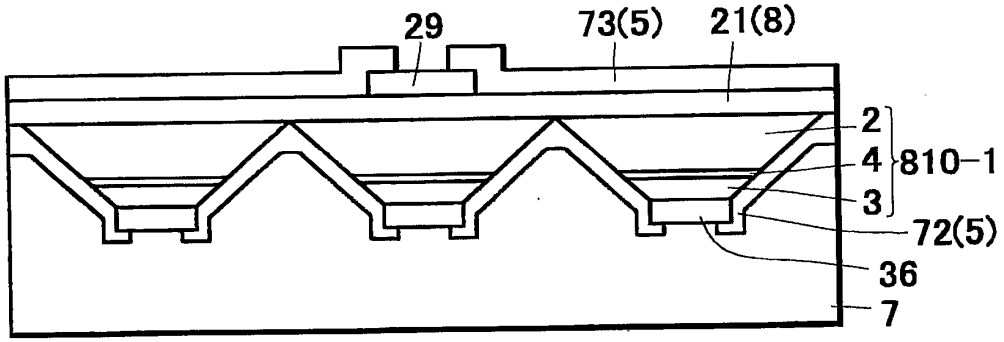

29
73(5)
21(8)
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4
3
810-1
72(5)
36
7

図 49

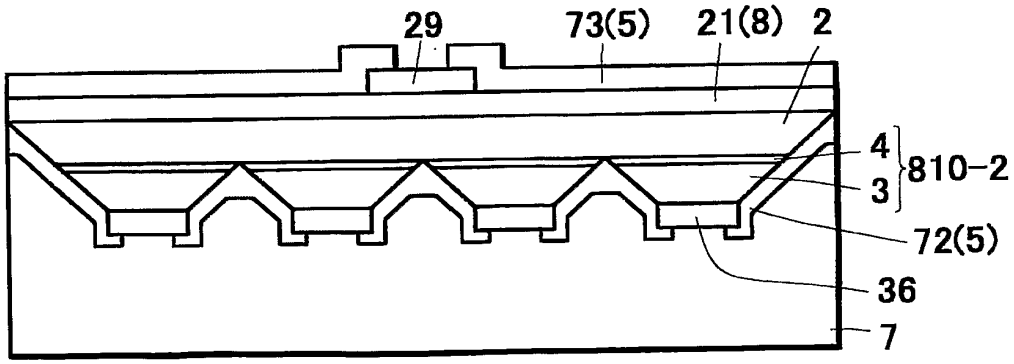

29
73(5)
21(8)
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810-2
72(5)
36
7

図 50

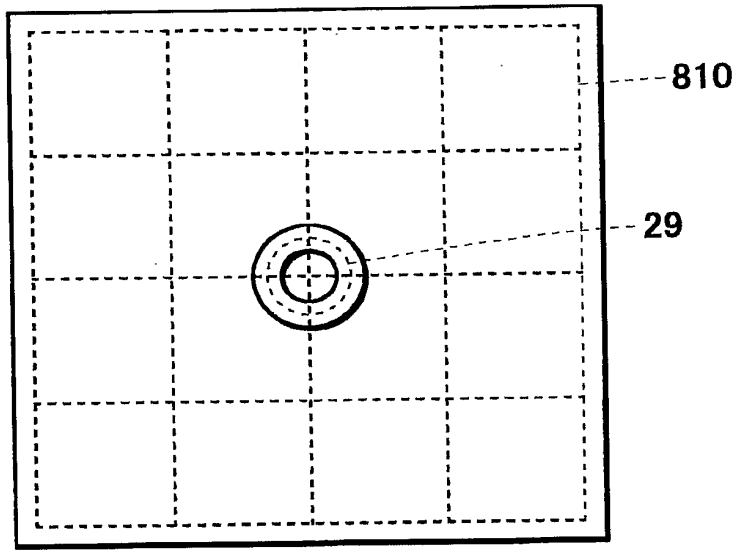


図 51

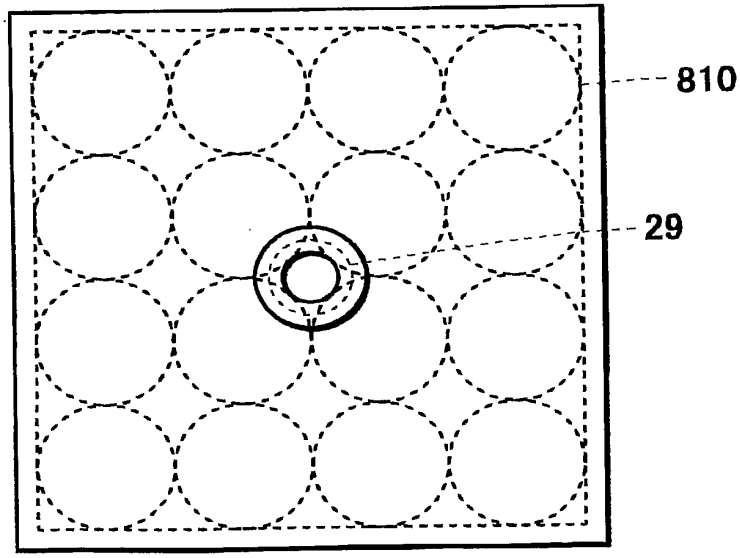


図52A

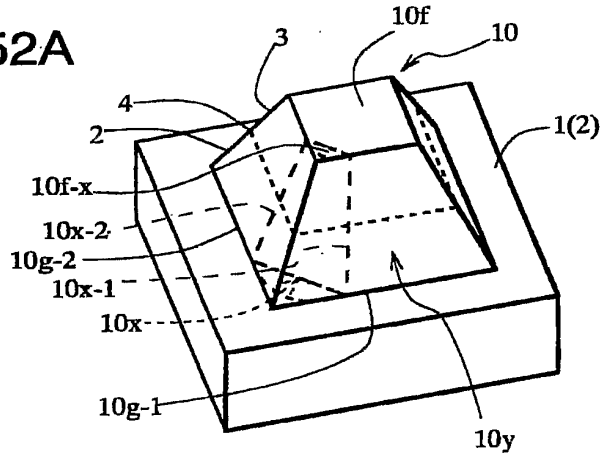


図52B

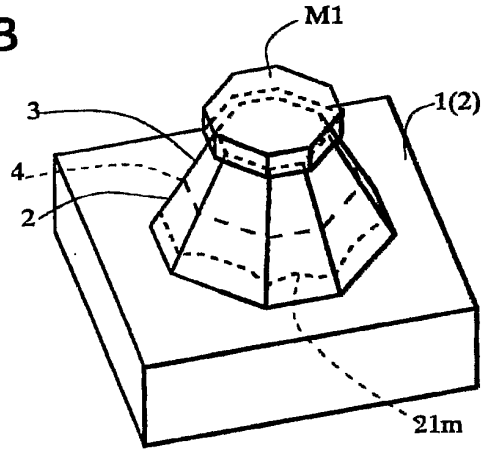


図53A

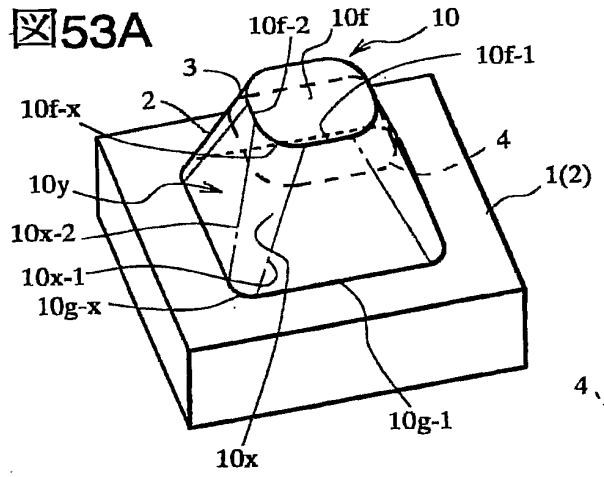


図53B

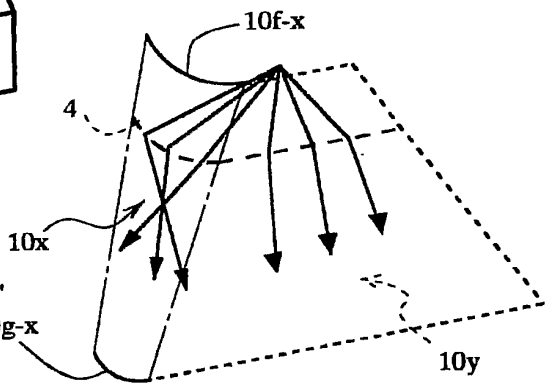


図53C

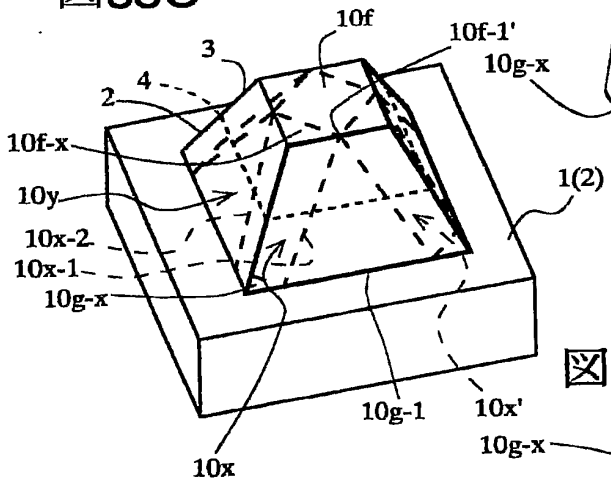


図53D

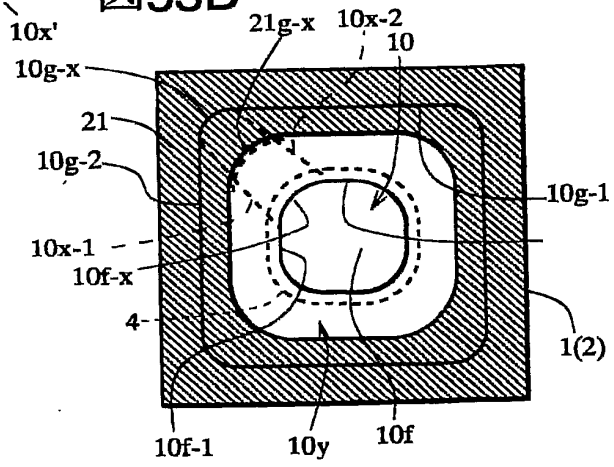


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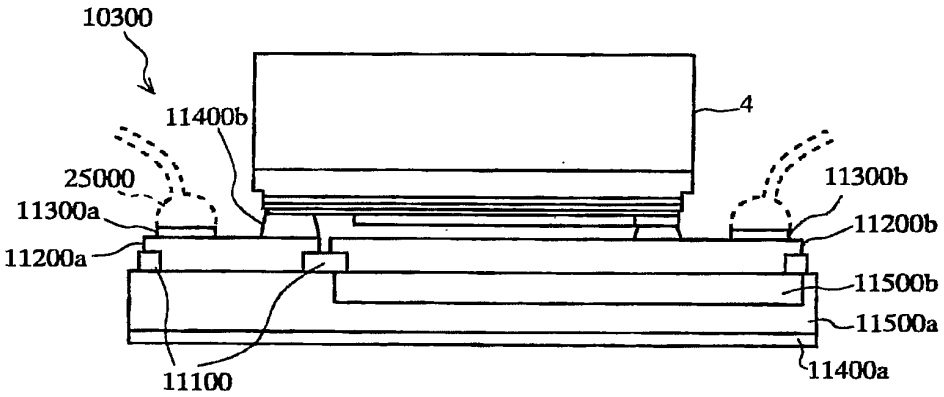


図54B

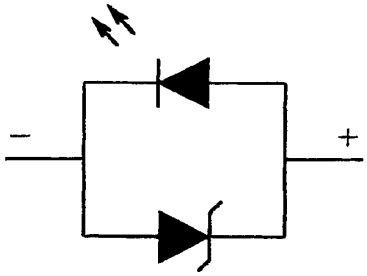


図55

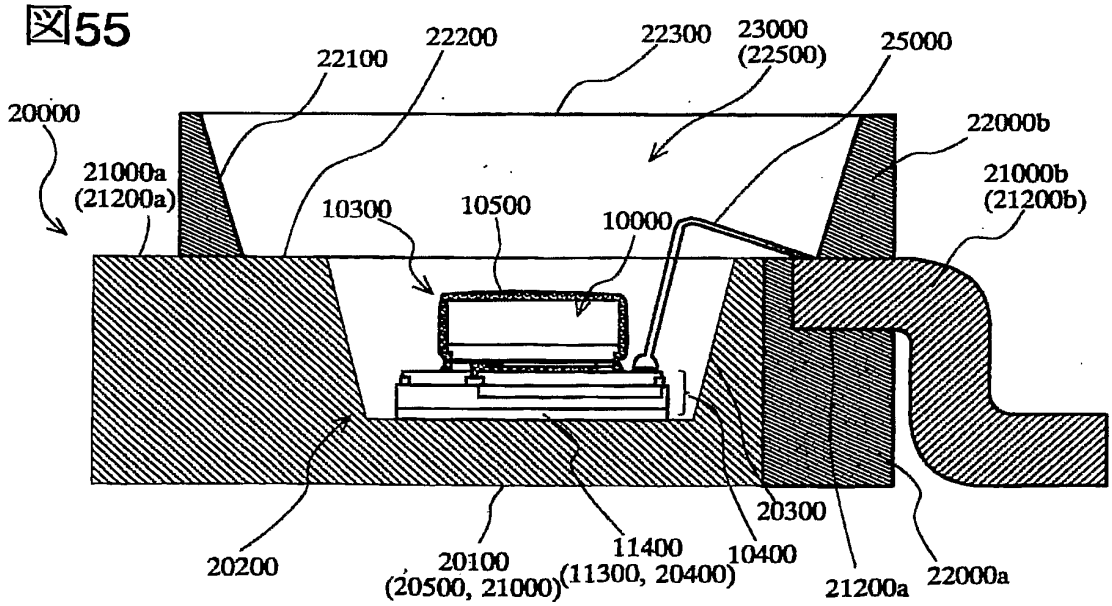


図56

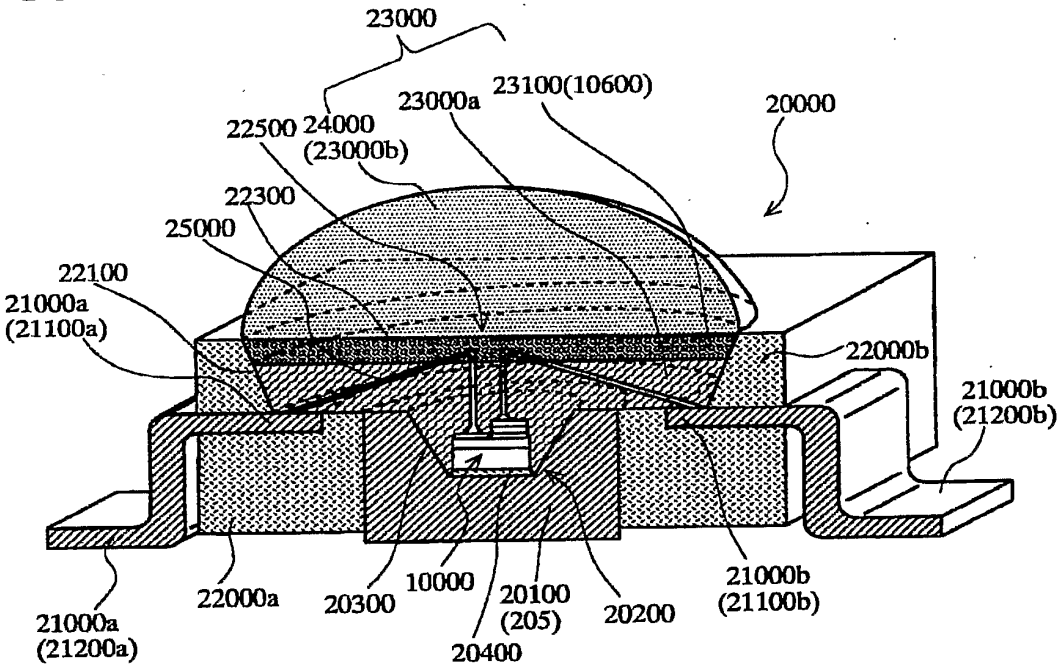


図57A

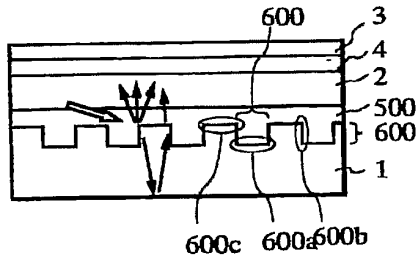


図57B

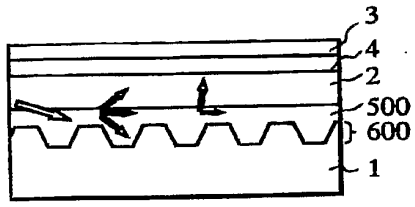


図57C

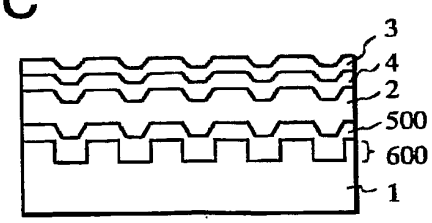


図57D

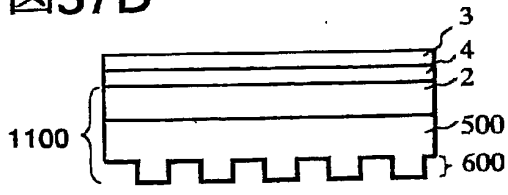


図58

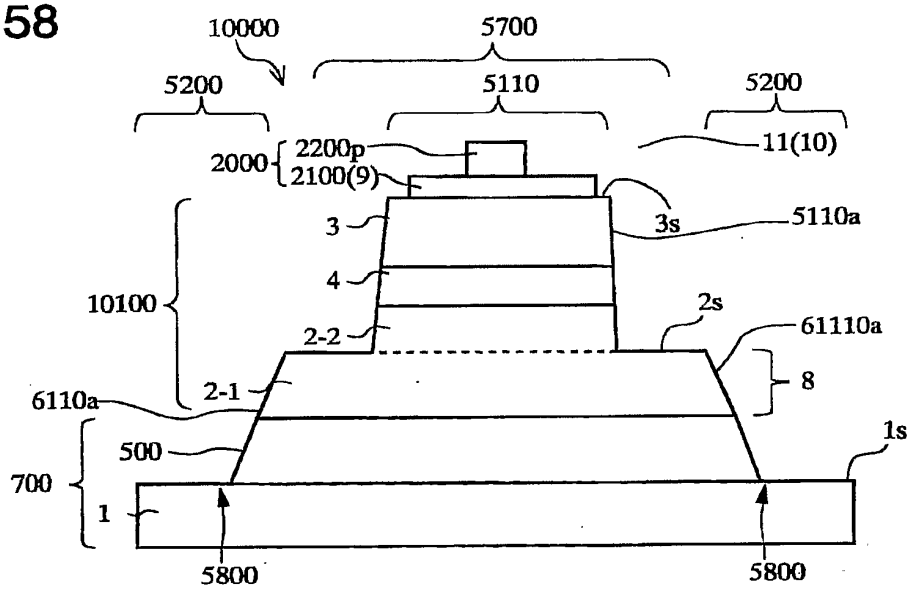


図59A

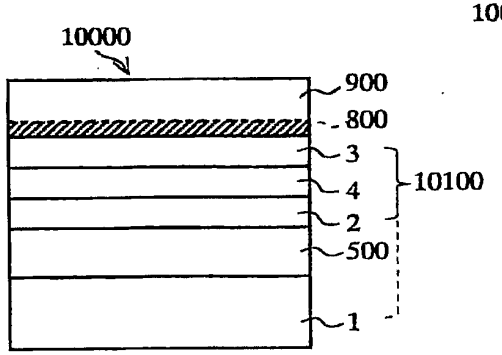


図59B

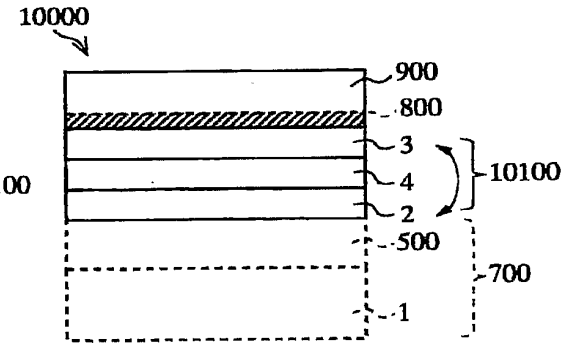


図60A

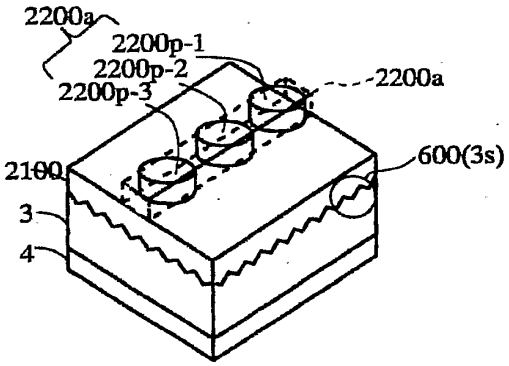


図60B

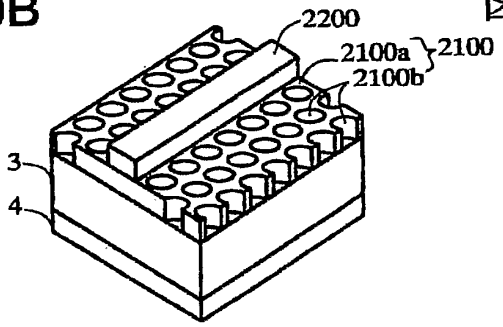


図60C

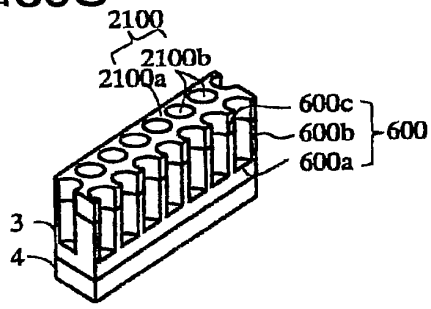


図 60D

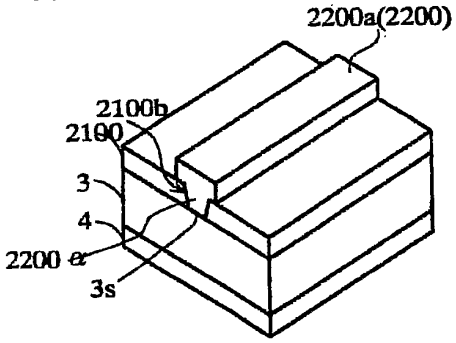
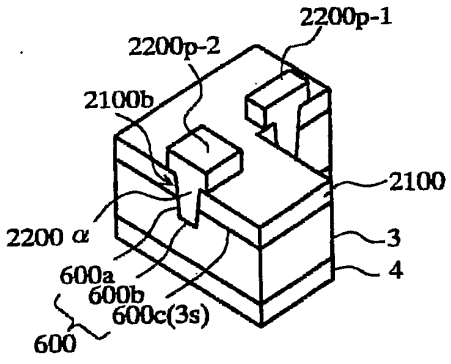


図 60E



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP03/09836

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H01L33/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H01L33/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1922-1996	Toroku Jitsuyo Shinan Koho	1994-2003
Kokai Jitsuyo Shinan Koho	1971-2003	Jitsuyo Shinan Toroku Koho	1996-2003

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 11-330559 A (Sanyo Electric Co., Ltd.), 30 November, 1999 (30.11.99), Full text; all drawings (Family: none)	1,2

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 November, 2003 (28.11.03)	09 December, 2003 (09.12.03)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP03/09836

Box I Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

The international search has revealed that the constitution of the invention of claim 1 was publicly known at the time of filing. Accordingly, the constitution of the invention of claim 1 is not a special technical feature within the meaning of PCT Rule 13.2, second sentence, since it makes no contribution over the prior art.

Since the inventions of claims 16, 18-22, and 24-26 are unclear, they are excluded from determination of technical features of claimed inventions.

(Continued to extra sheet)

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.: 1, 2

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP03/09836

Continuation of Box No. II of continuation of first sheet(1)

Claim 2: Electrode surrounds multilayer portion.
Claim 3: N electrode continues to lower surface of substrate.
Claim 4, 5: Circular or hexagonal multilayer portion
Claim 6-8, 23: Plural multilayer portions
Claim 9-12: Constitution of reflective layer
Claim 13: Shape of slope
Claim 14: Slope-embedding structure
Claim 15: Metal member holding structure
Claim 17: Use of transparent electrode
Claim 27, 28: Manufacturing method
Claim 29-50: Possession of first lateral surface

国際調査報告	国際出願番号　ＰＣＴ／ＪＰ０３／０９８３６

Ａ．　発明の属する分野の分類（国際特許分類（ＩＰＣ））

Ｉｎｔ．Ｃｌ⁷　Ｈ０１Ｌ　３３/００

Ｂ．　調査を行った分野

調査を行った最小限資料（国際特許分類（ＩＰＣ））

Ｉｎｔ．Ｃｌ⁷　Ｈ０１Ｌ　３３/００

最小限資料以外の資料で調査を行った分野に含まれるもの

日本国実用新案公報	１９２２－１９９６年
日本国公開実用新案公報	１９７１－２００３年
日本国登録実用新案公報	１９９４－２００３年
日本国実用新案登録公報	１９９６－２００３年

国際調査で使用した電子データベース（データベースの名称、調査に使用した用語）

Ｃ．　関連すると認められる文献

引用文献のカテゴリー＊	引用文献名　及び一部の箇所が関連するときは、その関連する箇所の表示	関連する請求の範囲の番号
X	JP 11-330559 A(三洋電機株式会社)1999.11.30 全文,全図（ファミリーなし）	1,2

☐ Ｃ欄の続きにも文献が列挙されている。　☐ パテントファミリーに関する別紙を参照。

＊　引用文献のカテゴリー
「Ａ」特に関連のある文献ではなく、一般的技術水準を示すもの
「Ｅ」国際出願日前の出願または特許であるが、国際出願日以後に公表されたもの
「Ｌ」優先権主張に疑義を提起する文献又は他の文献の発行日若しくは他の特別な理由を確立するために引用する文献（理由を付す）
「Ｏ」口頭による開示、使用、展示等に言及する文献
「Ｐ」国際出願日前で、かつ優先権の主張の基礎となる出願の日の後に公表された文献
「Ｔ」国際出願日又は優先日後に公表された文献であって出願と矛盾するものではなく、発明の原理又は理論の理解のために引用するもの
「Ｘ」特に関連のある文献であって、当該文献のみで発明の新規性又は進歩性がないと考えられるもの
「Ｙ」特に関連のある文献であって、当該文献と他の１以上の文献との、当業者にとって自明である組合せによって進歩性がないと考えられるもの
「＆」同一パテントファミリー文献

国際調査を完了した日	国際調査報告の発送日
２８．１１．０３	09.12.03

国際調査機関の名称及びあて先	特許庁審査官（権限のある職員）		
日本国特許庁（ＩＳＡ／ＪＰ） 郵便番号１００－８９１５ 東京都千代田区霞が関三丁目４番３号	道祖土　新吾	２Ｋ	９８１４
	電話番号　０３－３５８１－１１０１　内線　３２５３		

様式ＰＣＴ／ＩＳＡ／２１０（第２ページ）（１９９８年７月）

国際調査報告

国際出願番号　ＰＣＴ／ＪＰ０３／０９８３６

第Ⅰ欄　請求の範囲の一部の調査ができないときの意見（第１ページの２の続き）

法第８条第３項（ＰＣＴ１７条(2)(a)）の規定により、この国際調査報告は次の理由により請求の範囲の一部について作成しなかった。

1．☐ 請求の範囲 _____は、この国際調査機関が調査をすることを要しない対象に係るものである。
つまり、

2．☐ 請求の範囲 _____は、有意義な国際調査をすることができる程度まで所定の要件を満たしていない国際出願の部分に係るものである。つまり、

3．☐ 請求の範囲 _____は、従属請求の範囲であってＰＣＴ規則6.4(a)の第２文及び第３文の規定に従って記載されていない。

第Ⅱ欄　発明の単一性が欠如しているときの意見（第１ページの３の続き）

次に述べるようにこの国際出願に二以上の発明があるとこの国際調査機関は認めた。

請求の範囲１に記載される発明の構成は、調査の結果、出願当時公知であったことが判明した。従って、上記請求の範囲１に記載される発明の構成は、先行技術の域を出ないから、ＰＣＴ規則１３．２の第２文の意味において、特別な技術的特徴ではない。

なお、請求の範囲の判断において、請求の範囲１６、１８－２２、２４－２６は、その発明の内容が不明であるから、判断の対象外としている。

請求の範囲２：電極が積層部を取り囲む
請求の範囲３：ｎ電極が基板の下面まで連続
請求の範囲４、５：積層部が円形又は六角形
請求の範囲６－８、２３：複数の積層部
請求の範囲９－１２：反射層の構成
請求の範囲１３：傾斜面形状
請求の範囲１４：傾斜面埋め込み構造
請求の範囲１５：金属部材保持構造
請求の範囲１７：透明電極の利用
請求の範囲２７、２８：製法
請求の範囲２９－５０：第１側面を有する

1．☐ 出願人が必要な追加調査手数料をすべて期間内に納付したので、この国際調査報告は、すべての調査可能な請求の範囲について作成した。

2．☐ 追加調査手数料を要求するまでもなく、すべての調査可能な請求の範囲について調査することができたので、追加調査手数料の納付を求めなかった。

3．☐ 出願人が必要な追加調査手数料を一部のみしか期間内に納付しなかったので、この国際調査報告は、手数料の納付のあった次の請求の範囲のみについて作成した。

4．☒ 出願人が必要な追加調査手数料を期間内に納付しなかったので、この国際調査報告は、請求の範囲の最初に記載されている発明に係る次の請求の範囲について作成した。

請求の範囲１，２

追加調査手数料の異議の申立てに関する注意

☐ 追加調査手数料の納付と共に出願人から異議申立てがあった。

☐ 追加調査手数料の納付と共に出願人から異議申立てがなかった。

Electronic Acknowledgement Receipt

EFS ID:	4757434
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
Receipt Date:	09-FEB-2009
Filing Date:	26-DEC-2007
Time Stamp:	15:05:48
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	US_IDS_Form_SB_08a.pdf	34733 b967ad41ab47ac0a98eec1f810d4f24f96d3483c	no	4

Warnings:	
Information:	

This is not an USPTO supplied IDS fillable form					
2	Foreign Reference	WO04-023568.pdf	1409129 c447c01c6b0be2dfc8cecfc554a4e0a88434f2fb	no	42
Warnings:					
Information:					
3	Foreign Reference	WO04-013916.pdf	5840517 7a06e4cad77be34e32c73dffbc5784eea67b07d8	no	123
Warnings:					
Information:					
			Total Files Size (in bytes):	7284379	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/993,965	12/26/2007	Jong Lam Lee	P2317US00	2191

58027 7590 07/09/2009

H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

EXAMINER	
NGUYEN, THINH T	

ART UNIT	PAPER NUMBER
2818	

NOTIFICATION DATE	DELIVERY MODE
07/09/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATENT@PARK-LAW.COM

Office Action Summary	Application No.	Applicant(s)	
	11/993,965	LEE ET AL.	
	Examiner	Art Unit	
	THINH T. NGUYEN	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *1* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-16* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED OFFICE ACTION

Election/Restrictions

Claims 1-16 are pending in this application.

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

Group I. Claims 1-6 drawn to a semiconductor device, classified in class 257, subclass 088.

Group II. Claims 7-16 drawn to process of making a semiconductor device, classified in class 438, and subclass 28

2. The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of following can be shown: (1) that the process as claimed can be use to make other and materially different product or (2) that the product as claimed can be made by another and materially different process or by hand (MPEP § 806.05(f)). In the instance case unpatentabilities of the group I invention would not necessarily imply unpatentability of the group II invention, since the device of the group I invention could be made by the processes materially different from those of the group II invention, **for example, in the claim 7 a method for making the semiconductor device of claim 1, wherein this method can be used to fabricate a device wherein the side surface has a slope of 84 to 88 degree with the horizontal plane which is a materially different method from claim 1**

Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and examination burden if restriction were not required because one or more of the following reasons apply:

(a) the inventions have acquired a separate status in the art in view of their different classification;

(b) the inventions have acquired a separate status in the art due to their recognized divergent subject matter;

(c) the inventions require a different field of search (for example, searching different classes/subclasses or electronic resources, or employing different search queries);

(d) the prior art applicable to one invention would not likely be applicable to another invention;

(e) the inventions are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention.**

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected invention. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, the fields of search are not co-extensive. Therefore, separate examination would be required and restriction for examination purposes as indicated is proper.

4. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a diligently filed petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(h).

CONCLUSION

5. Any inquiry concerning this communication on earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on Monday-Friday from 9:30 AM to 6:30 PM. The examiner's supervisor, Steve Loke can be reached on 571-272-1657.The-fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thinh T Nguyen/
Patent Examiner
Art Unit 2818

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11993965	LEE ET AL.
	Examiner	**Art Unit**
	THINH T NGUYEN	2818

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/06/2009								
	1	÷								
	2	÷								
	3	÷								
	4	÷								
	5	÷								
	6	÷								
	7	÷								
	8	÷								
	9	÷								
	10	÷								
	11	÷								
	12	÷								
	13	÷								
	14	÷								
	15	÷								
	16	÷								

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Docket No.: P2317US00

Jong Lam LEE, *et al.*

Serial No.: 11/993,965 Group Art Unit: 2818

Confirmation No.: 2191

Filed: December 26, 2007 Examiner: NGUYEN, Thinh T.

For: **LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO ELECTION/RESTRICTION REQUIREMENT

Sir:

In reply to the July 9, 2009 Restriction Requirement, Applicants elect Group I, including claims 1-6, without traverse.

It is not believed that any extensions of time or fees are required. If extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned for under 37 C.F.R. §1.136(a) and associated fees may be charged to our Deposit Account No. 50-3698.

Respectfully submitted,

/hae-chan park/

Hae-Chan Park
Reg. No. 50,114

Dated: July 30, 2009

CUSTOMER NO.: 58027
H.C. Park & Associates, PLC

Electronic Acknowledgement Receipt

EFS ID:	5798088
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/Wayne Helge
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
Receipt Date:	30-JUL-2009
Filing Date:	26-DEC-2007
Time Stamp:	12:18:36
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	Response_to_Restriction_Requirement.pdf	68548 b833646f060a8df6e0510cf9dd7a7ffdea6c8048	no	1

Warnings:	
Information:	

Total Files Size (in bytes):	68548

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	Docket No.: P2317US00
Jong Lam LEE, *et al.*	
Serial No.: 11/993,965	Group Art Unit: 2818
Confirmation No.: 2191	
Filed: Dec. 27, 2007	Examiner: NGUYEN, Thinh T.

For: **LIGHT EMITTING DEVICE**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

Prior to examination on the merits, please amend the above-identified application as follows.

Amendments to the Specification begin on page 2.

Amendments to the Claims begin on page 3.

Remarks begin on page 7.

It is not believed that any extensions of time or fees for net addition of claims are required at this moment. However, if additional extension of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. §1.136(a), and any fees required therefor are hereby authorized to be charged to our Deposit Account No. 50-3698.

AMENDMENT TO THE SPECIFICATION

Please replace the specification with the attached substitute specification. A version with markings and a clean version are attached. The claims are not included with the substitute specification.

The substitute specification does not contain new matter.

AMENDMENT TO THE CLAIMS

Please **CANCEL** claims 5 and 6 without prejudice or disclaimer.

1. (Original) A light emitting device, comprising:

a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on a portion of the N-type semiconductor layer on a substrate, wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including the N-type or P-type semiconductor layer of the light emitting cell has a slope of 20 to 80° from a horizontal plane.

2. (Original) The light emitting device as claimed in claim 1, further comprising a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

3. (Previously presented) The light emitting device as claimed in claim 1, further comprising a transparent electrode layer on the P-type semiconductor layer.

4. (Previously presented) The light emitting device as claimed in claim 1, further comprising P-type and N-type ohmic metal layers containing Cr or Au on the P-type and N-type semiconductor layers, respectively.

5-6. (Canceled)

7. (Withdrawn) A method of manufacturing a light emitting device, comprising the steps

of:

sequentially forming N-type and P-type semiconductor layers on a substrate;

forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; and removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern.

8. (Withdrawn) The method as claimed in claim 7, further comprising the steps of:

removing a portion of the N-type semiconductor layer exposed through the removal of the P-type semiconductor layer to form a plurality of light emitting cells; and

connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire.

9. (Withdrawn) The method as claimed in claim 7, further comprising the step of flip-chip bonding the substrate onto an additional submount substrate after the step of removing the P-type semiconductor layer and the etching mask pattern.

10. (Withdrawn) The method as claimed in claim 9, further comprising the steps of:

removing a portion of the N-type semiconductor layer exposed due to the removal of the P-type semiconductor layer to form a plurality of light emitting cell; and

connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire, after the step of removing the P-type semiconductor layer and the etching mask pattern.

11. (Withdrawn) The method as claimed in claim 8, wherein the step of forming the plurality of light emitting cells comprises the steps of:

forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer;

removing the N-type and P-type semiconductor layers exposed through the etching mask pattern to form a plurality of light emitting cells; and

removing the etching mask pattern.

12. (Withdrawn) The method as claimed in claim 8, wherein the N type semiconductor layer of one light emitting cell and the P type semiconductor layer of another adjacent light emitting cell are connected with the conductive wire through a bridge or step coverage process.

13. (Withdrawn) The method as claimed in claim 7, wherein a photoresist with a thickness of 3 to 50μm is used in the step of forming the etching mask pattern.

14. (Withdrawn) The method as claimed in claim 13, wherein the step of forming the etching mask pattern comprises the steps of:

applying the photoresist onto the P-type semiconductor layer;

light exposing the photoresist in accordance with a predetermined mask pattern; and

developing the light-exposed photoresist without a baking process after the light exposure.

15. (Withdrawn) The method as claimed in claim 13, wherein the step of forming the etching mask pattern comprises the steps of:

applying the photoresist onto the P-type semiconductor layer;

light exposing the photoresist in accordance with a predetermined mask pattern;

hard baking the light-exposed photoresist at a temperature of 100 to 140¡É; and

developing the hard-baked photoresist.

16. (Withdrawn) The method as claimed in claim 7, further comprising the steps of:

after the step of removing the P-type semiconductor layer and the etching mask pattern, removing a rear surface of the substrate at a certain thickness; and

depositing Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof onto the rear surface of the substrate.

REMARKS

Claims 5 and 6 have been canceled without prejudice or disclaimer. The specification and drawings have been amended to include inadvertently omitted material from priority documents KR10-2005-0053797, KR10-2005-55179, and KR10-2006-0021801, which were incorporated by reference in their entirety per the Preliminary Amendment filed December 26, 2007.

Claims 7-16 have been previously withdrawn.

Accordingly, claims 1-4 are pending in this application, of which claim 1 is independent.

Applicants respectfully submit that the amendments do not add new matter to the application.

Amendments to the Specification

New paragraphs [0036], [0037], and [0128] through [0159] have been added to include material that was inadvertently omitted from the original specification. Support for new paragraphs [0036], [0037], and [0128] through [0159] is found respectively in paragraphs [0003], [0004], and [0031] through [0061] in priority document KR10-2006-0021801. A certified English translation of this Korean priority document is included herewith.

Paragraphs [0021], [0049] through [0053], [0062], [0063], [0073], [0099], [0100], [0114], and [0115] have been amended to include "μm" in the substitute specification. Support for these amendments is found in priority documents KR10-2005-0053797 and KR10-2005-0055179. Specifically, support for paragraphs [0021], [0049] through [0053], [0062], [0063], [0073] may be found respectively in paragraphs [0026], [0042] through [0046], [0056], [0057], and [0069] in priority document KR10-2005-0053797. Support for paragraphs [0099], [0100], [0114], and [0115] may respectively be found in paragraphs [0042], [0043], [0061], and [0062] in

priority document KR10-2005-0055179. Certified English translations of these Korean priority documents are included herewith.

Amendments to the Drawings

Please add new drawings 32 through 38 as shown in the attached New Drawing Sheets. New drawings 32 through 38, which were inadvertently omitted from the filed application, correspond to drawings 3 through 9 in the priority document KR10-2006-0021801.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,

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Attachments: (1) Substitute Specification, marked-up copy
(2) Substitute Specification, clean copy
(3) New Drawing Sheets (3)

LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

[0001] Field of Invention

[0002] The present invention relates to a light emitting device and a method of manufacturing the same. More particularly, the present invention relates to a nitride based semiconductor light emitting device with enhanced luminous efficiency and brightness and a method of manufacturing the light emitting device.

[0003] Description of the Related Art

[0004] A light emitting device refers to an element in which minority carriers (electrons or holes) injected using a p-n junction structure of a semiconductor are produced and certain light is emitted due to recombination of the carriers. A light emitting source is formed from any one or combination of compound semiconductor materials such as GaAs, AlGaAs, GaN, InGaN and AlGaInP, so that a variety of colors can be implemented. For example, a red light emitting device may be formed from GaAsP or the like; a green light emitting device may be formed from GaP, InGaN or the like; a blue light emitting device may be formed using an InGaN/GaN double hetero structure; and a UV light emitting device may be formed using an AlGaN/GaN or AlGaN/AlGaN structure.

[0005] In particular, GaN has a direct bandgap of 3.4eV at a normal temperature and a direct energy bandgap of 1.9eV (InN) to 3.4eV (GaN) or 6.2eV (AlN) by combining with a substance such as InN or AlN. Thus, GaN is a substance with great applicability to an optical element due to its broad wavelength range from visible light to ultraviolet light. Since the wavelength can be adjusted in such a manner, full-color implementation can be made by means of red, green and blue light emitting devices with a short wavelength range, so that the applicability to a general illumination market as well as a display device market is

expected to be greatly increased.

[0006] Light emitting devices have characteristics of lower power consumption, longer lifespan, better installation in a narrow space and stronger resistance against vibration as compared with existing bulbs or fluorescent lamps. Since the light emitting devices are used as display devices and backlights and have superior characteristics in view of the reduction in power consumption and the durability, many studies for applying the light emitting devices to a general illumination field have been recently conducted. In the future, their applicability is expected to extend to a backlight of a large-sized LCD-TV, a vehicle headlight and general illumination. To this end, it is necessary to improve luminous efficiency of light emitting devices, solve a heat dissipation problem, and achieve high brightness and output of the light emitting devices.

[0007] Many techniques for enhancing the performance of light emitting devices have been currently developed. There are various indexes indicating the performance of light emitting devices, such as luminous efficiency (lm/W), internal quantum efficiency (%), external quantum efficiency (%) and extraction efficiency (%). The extraction efficiency is determined as a ratio of electrons injected into the light emitting device to photons emitted to the outside of the light emitting device. That is, the light emitting device becomes bright as the extraction efficiency becomes high. Since the extraction efficiency of the light emitting device is much influenced by the shape and surface pattern of a chip, the structure of a chip and a packaging type, careful attention should be paid when designing the light emitting device.

[0008] Fig. 1 is a sectional view showing a conventional light emitting device with a horizontal structure.

[0009] Referring to Fig. 1, the light emitting device comprises a substrate 1, an N-type semiconductor layer 2 formed on the substrate 1, an active layer 3 formed on a portion

of the N-type semiconductor layer 2 and a P-type semiconductor layer 4. That is, after the N-type semiconductor layer 2, the active layer 3 and the P-type semiconductor layer 4 have been sequentially formed on the substrate 1, predetermined regions of the P-type semiconductor layer 4 and the active layer 3 are etched to expose a portion of the N-type semiconductor layer 2. Then, a predetermined voltage is applied to top surfaces of the exposed N-type semiconductor layer 2 and the P-type semiconductor layer 4.

[0010] Fig. 2 is a sectional view showing a conventional light emitting device with a flip chip structure.

[0011] Referring to Fig. 2, the light emitting device comprises an N-type semiconductor layer 2, an active layer 3 and a P-type semiconductor layer 4, which are sequentially formed on a base substrate 1. The light emitting device further comprises a submount substrate 5 onto which the base substrate 1 is flip-chip bonded using metal bumps 8 and 9. To this end, the N-type semiconductor layer 2, the active layer 3 and the P-type semiconductor layer 4 are sequentially formed on the predetermined substrate 1, and portions of the P-type semiconductor layer 4 and the active layer 3 are etched to expose the N-type semiconductor layer 2 such that a light emitting cell can be formed. Further, the additional submount substrate 5 is prepared to form first and second electrodes 6 and 7 thereon, and the P-type and N-type metal bumps 8 and 9 are then formed on the first and second electrodes 6 and 7, respectively. Thereafter, the light emitting cell is bonded with the submount substrate 5 such that P and N electrodes of the light emitting cell are bonded with the P-type and N-type metal bumps 8 and 9, respectively, to fabricate a light emitting device. Since such a conventional light emitting device with a flip chip structure has high heat dissipation efficiency and hardly has shield of light, there is an advantage in that its light efficiency is increased by 50% or more as compared with a conventional light emitting device. Further, since a gold wire for driving a light emitting device is not necessary, many applications to a

variety of small-sized packages can be considered.

[0012] Light produced from a light emitting layer of a light emitting device is emitted from all the surfaces of a chip, and light extraction efficiency is generally determined by a critical angle of light. However, when the conventional light emitting device is etched to expose an N-type semiconductor layer, side surfaces of the P-type semiconductor layer and the active layer are vertically processed such that a portion of light produced within the light emitting device is totally reflected on the etched surface that is processed vertically from a horizontal plane. Then, a considerable amount of light to be totally reflected is not emitted to the outside but dissipated within the light emitting device due to the internal reflection. That is, there is a problem in that luminous efficiency in which electric energy is converted into light energy and the light is then emitted to the outside of a light emitting device is low.

SUMMARY OF THE INVENTION

[0013] The present invention is conceived to solve the aforementioned problems. Accordingly, an object of the present invention is to provide a light emitting device for emitting light with high luminous intensity and brightness by enhancing characteristics of luminous efficiency, external quantum efficiency, extraction efficiency and the like and improving reliability, and a method of manufacturing the light emitting device.

[0014] According to an aspect of the present invention for achieving the objects, there is provided a light emitting device, comprising a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on a portion of the N-type semiconductor layer on a substrate. The N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell may be connected to each other, and a side surface including the N-type or P-type semiconductor layer of the light emitting cell has a slope of 20 to 80° from a horizontal

plane. The light emitting device may further comprise a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell, a transparent electrode layer on the P-type semiconductor layer, and P-type and N-type ohmic metal layers containing Cr or Au on the P-type and N-type semiconductor layers, respectively.

[0015] According to another aspect of the present invention, there is provided a light emitting device comprising a substrate formed with a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on the N-type semiconductor layer and a submount substrate flip-chip bonded onto the substrate. Preferably, the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including at least the P-type semiconductor layer of the light emitting cell has a slope of 20 to 80°from a horizontal plane. The light emitting device may further comprise a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

[0016] According to further aspect of the present invention, there is provided a method of manufacturing a light emitting device, comprising the steps of sequentially forming N-type and P-type semiconductor layers on a substrate; forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; and removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern.

[0017] According to still further aspect of the present invention, there is a method of manufacturing a light emitting device comprising the steps of removing a portion of the N-type semiconductor layer exposed due to the removal of the P-type semiconductor layer to form a plurality of light emitting cells; and connecting the N-type semiconductor layer of one

light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire.

[0018] According to still further aspect of the present invention, there is a method of manufacturing a light emitting device comprising the step of flip-chip bonding the substrate onto an additional submount substrate after the step of removing the P-type semiconductor layer and the etching mask pattern. The method of manufacturing a light emitting device may further comprise the steps of removing a portion of the N-type semiconductor layer exposed through the removal of the P-type semiconductor layer to form a plurality of light emitting cell; and connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire, after the step of removing the P-type semiconductor layer and the etching mask pattern.

[0019] The step of forming the plurality of light emitting cells may comprise the steps of forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; removing the N-type and P-type semiconductor layers exposed through the etching mask pattern to form a plurality of light emitting cells; and removing the etching mask pattern.

[0020] The N type semiconductor layer of one light emitting cell and the P type semiconductor layer of another adjacent light emitting cell may be connected with the conductive wire through a bridge or step coverage process.

[0021] A photoresist with a thickness of 3 to 50μm may be used in the step of forming the etching mask pattern. The step of forming the etching mask pattern may comprise the steps of: applying the photoresist onto the P-type semiconductor layer; light exposing the photoresist in accordance with a predetermined mask pattern; and developing the light-exposed photoresist without a baking process after the light exposure. The step of

forming the etching mask pattern may comprise the steps of: applying the photoresist onto the P-type semiconductor layer; light exposing the photoresist in accordance with a predetermined mask pattern; hard baking the light-exposed photoresist at a temperature of 100 to 140℃; and developing the hard-baked photoresist.

[0022] After the step of removing the P-type semiconductor layer and the etching mask pattern, the method of manufacturing a light emitting device may further comprise the steps of removing a rear surface of the substrate at a certain thickness; and depositing Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof onto the rear surface of the substrate.

[0023] In a light emitting device and a method of manufacturing the same according to the present invention, light produced from a side surface of a semiconductor layer, which is not perpendicular to but inclined at a predetermined slop from a horizontal plane, is not totally reflected but emitted to the outside of the light emitting device. Therefore, more enhanced characteristics of light extraction efficiency, external quantum efficiency, luminous efficiency or the like can be obtained. Further, a light emitting device of the present invention emits light with high luminous intensity and brightness and can be applied to a variety of products in which a superior light characteristic is necessary.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The above and other objects, features and advantages of the present invention will become apparent from the following description of preferred embodiments given in conjunction with the accompanying drawings, in which:

[0025] Figs. 1 and 2 are sectional views showing conventional light emitting devices, respectively;

[0026] Fig. 3 is a conceptual sectional view illustrating a light emitting device with a horizontal structure according to the present invention;

[0027] Figs. 4 and 5 are sectional views illustrating a process of manufacturing a light emitting device according to a first embodiment of the present invention;

[0028] Figs. 6 to 9 are sectional views illustrating a process of manufacturing a light emitting device according to a second embodiment of the present invention;

[0029] Figs. 10 to 13 are sectional views illustrating a process of manufacturing a light emitting device according to a third embodiment of the present invention;

[0030] Figs. 14 to 17 are sectional views illustrating a process of manufacturing a light emitting device according to a fourth embodiment of the present invention;

[0031] Fig. 18 is a conceptual sectional view illustrating a light emitting device with a flip chip structure according to the present invention;

[0032] Figs. 19 to 23 are sectional views illustrating a process of manufacturing a light emitting device according to a fifth embodiment of the present invention;

[0033] Figs. 24 to 28 are sectional views illustrating a process of manufacturing a light emitting device according to a sixth embodiment of the present invention;

[0034] Fig. 29 is a sectional view showing a seventh embodiment according to the present invention; and

[0035] Figs. 30 and 31 are conceptual sectional views illustrating a difference

between effects of the light emitting devices according to the prior art and the present invention;

[0036] Fig. 32 is a sectional view illustrating a light emitting diode for AC operation according to an eighth embodiment of the present invention; and

[0037] Figs. 33 to 38 are sectional views illustrating a process of manufacturing a light emitting diode according to the eighth embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0038] Hereinafter, a light emitting device and a manufacturing method thereof according to the present invention will be described in detail with reference to the accompanying drawings. However, the present invention is not limited to the embodiments set forth herein but can be implemented in different forms. Rather, the preferred embodiments are merely provided to allow the present invention to be completely described herein and to fully convey the scope of the invention to those skilled in the art.

[0039] Fig. 3 is a conceptual sectional view illustrating a light emitting device with a horizontal structure according to the present invention.

[0040] Referring to Fig. 3, the light emitting device comprises a substrate 10, and an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40, which are sequentially formed on the substrate 10. Each of side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 has a slope of 80 to 20° from a horizontal plane such that a critical angle of light can be changed by such surfaces and light can be easily extracted. Therefore, luminous efficiency of a light emitting device can be improved.

[0041] Figs. 4 and 5 are sectional views illustrating a process of manufacturing a light emitting device according to a first embodiment of the present invention.

[0042] Referring to Fig. 4, an N-type semiconductor layer 20, an active layer 30

and a P-type semiconductor layer 40 are sequentially formed on a substrate 10.

[0043] The substrate 10 refers to a general wafer used for fabricating a light emitting device and is made of at least any one of Al_2O_3, SiC, ZnO, Si, GaAs, GaP, $LiAl_2O_3$, BN, AlN and GaN. In this embodiment, a crystal growth substrate made of sapphire is used.

[0044] A buffer layer (not shown) may be further formed on the substrate 10 to reduce lattice mismatch between the substrate 10 and the subsequent layers upon growth of crystals. The buffer layer may contain GaN or AlN that is a semiconductor material.

[0045] The N-type semiconductor layer 20 is a layer in which electrons are produced and is preferably made from GaN doped with N-type impurities. However, the N-type semiconductor layer 20 is not limited thereto but may use a material layer having a variety of semiconductor properties. The N-type semiconductor layer 20 including N-type $Al_xGa_{1-x}N(0\leq x\leq 1)$ is formed in this embodiment. Further, the P-type semiconductor layer 40 is a layer in which holes are produced and is preferably made from GaN doped with P-type impurities. However, the P-type semiconductor layer 40 is not limited thereto but may use a material layer with a variety of semiconductor properties. The P-type semiconductor layer 40 including P-type $Al_xGa_{1-x}N(0\leq x\leq 1)$ is formed in this embodiment. Moreover, InGaN may be used as the semiconductor layer. Further, each of the N-type and P-type semiconductor layers 20 and 40 may be formed as a multiple layer.

[0046] The active layer 30 has a predetermined bandgap and is a region where a quantum well is formed so that electrons and holes are recombined. The active layer 30 may contain InGaN. The wavelength of light emitted through the combination of electrons and holes varies according to the kind of a material constituting the active layer 30. Therefore, it is preferred that a semiconductor material contained in the active layer 30 be controlled depending on a target wavelength.

[0047] The aforementioned material layers are formed through a variety of

deposition and growth methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like.

[0048] Thereafter, portions of the P-type semiconductor layer 40 and the active layer 30 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 20. An etching mask pattern is formed on the P-type semiconductor layer 40, and the P-type semiconductor layer 40 and the active layer 30 are then removed through a dry or wet etching process to expose the N-type semiconductor layer 20.

[0049] Generally, in order to perform the etching process, a photoresist has been applied onto a top surface of the P-type semiconductor layer 40 at a thickness of 1 to 2μm, and then soft-baked at a temperature of 80 to 90°C is performed. Next, an exposure process in which light in a UV range is irradiated through a predetermined photo mask to transfer a pattern formed on the mask to the applied photoresist is executed. Thereafter, the photoresist is hard-baked at a temperature of 100 to 120°C, and a developing process in which the photoresist at a portion with relatively weak combination through the exposure process is melted using a solvent is executed. A predetermined etching mask pattern is formed on the P-type semiconductor layer 40 through the above process.

[0050] However, in this embodiment, the photoresist is applied at a thickness of 3 to 50μm which is thicker as compared with the prior art when the etching mask pattern is formed, and the exposure process is performed after the soft-baking. Next, if the photoresist is directly developed without the hard-baking, a developed side surface of the remaining photoresist is formed into an inclined surface not perpendicular (90°) to but inclined at a predetermined slope from a horizontal plane. Subsequently, if exposed regions of the P-type semiconductor layer 40, the active layer 30 and the predetermined N-type semiconductor

layer 20 are etched using the etching mask pattern with such a slope of the side surface, the side surfaces of the etched P-type semiconductor layer 40, active layer 30 and N-type semiconductor layer 20 can be similarly formed into an inclined surface not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane.

[0051] That is, after the photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 40 of Fig. 4 and light-exposed, a developed etching mask pattern is immediately formed without the hard-baking. The P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer 20. A portion of the exposed N-type semiconductor layer 20 may be further removed. Thereafter, if the etching mask pattern is removed, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured as shown in Fig. 5.

[0052] Alternatively, after a photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 40 of Fig. 4 and light-exposed, hard-baking may be performed. In such a case, if the photoresist is hard-baked at a temperature of 100 to 140°C and then developed, the side surface of the developed photoresist may be etched to have a slope of 80 to 20° from a horizontal plane. For example, in a case where the hard-baking is performed at a temperature of 100°C, an etching mask pattern with a slope of about 80° from the horizontal plane can be obtained, and the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 can have a slope of about 80° from the horizontal plane using the etching mask pattern. Further, in a case where the hard-baking is performed at a temperature of 140°C, an etching mask pattern with a slope of about 20° from the horizontal plane can be obtained, and the side surfaces of the P-type

semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 can have a slope of about 20° from the horizontal plane using the etching mask pattern.

[0053] The etching mask pattern, which the photoresist with a thickness of 3 to 50μm has been light-exposed and hard-baked at a temperature of 100 to 140°C and then developed in such a manner, can be used such that the side surfaces of the etched the P-type semiconductor layer 40, active layer 30 and predetermined N-type semiconductor layer 20 have a slope of 80 to 20° from a horizontal plane similarly to the etching mask pattern. Then, light produced within a light emitting layer is not totally reflected on the etched side surface with a variety of slopes but emitted to the outside of a light emitting device.

[0054] A transparent electrode layer may be further formed on the P-type semiconductor layer 40 to reduce resistance of the P-type semiconductor layer 40 and enhancing transmittance of light, and an additional ohmic metal layer may be further formed on the P-type semiconductor layer 40 or the exposed N-type semiconductor layer 20 to facilitate current supply. The transparent electrode layer may be made of ITO (Indium Tin Oxide), ZnO or a transparent conductive metal, and the ohmic metal layer may be made of Cr or Au. Further, for the application of voltage, a P-type electrode may be further formed on the P-type semiconductor layer 40 and an N-type electrode may be further formed on the N-type semiconductor layer 20.

[0055] Further, in order to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10.

[0056] As can be seen from this figure, a plurality of light emitting devices may be fabricated on a single substrate 10, which is cut into the individual light emitting devices. At this time, portions A shown in Fig. 5 are cutting portions used for individually cutting the

plurality of light emitting devices.

[0057] Accordingly, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 is not perpendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured.

[0058] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto. Various processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes.

[0059] Figs. 6 to 7 are sectional views illustrating a process of manufacturing a light emitting device according to a second embodiment of the present invention.

[0060] The second embodiment of the present invention is almost the same as the first embodiment. In the second embodiment, however, there is provided a light emitting device in which a plurality of light emitting cells are connected in series, parallel or series-parallel in a wafer level to reduce the size of the device, and they can be driven at proper voltage and current to be used for illustration purpose and can also be driven even with an AC power source. Descriptions overlapping with the previous embodiment will be omitted herein.

[0061] Referring to Fig. 6, an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40 are sequentially formed on a substrate 10 through various deposition methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like. A buffer layer may be further formed on the substrate 10 to reduce lattice mismatch between the substrate 10 and the subsequent layers upon growth of crystals.

[0062] Thereafter, portions of the P-type semiconductor layer 40 and the active layer 30 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 20. That is, after the photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 40 of Fig. 6 and light-exposed, it is developed without hard-baking to form an etching mask pattern. The P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer 20. A portion of the exposed N-type semiconductor layer 20 may be further removed. Thereafter, if the etching mask pattern is removed, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured as shown in Fig. 7.

[0063] Alternatively, after a photoresist has been applied in a thickness of 3 to 50μm on the P-type semiconductor layer 40 of Fig. 6 and light-exposed, it is hard-baked at a temperature of 100 to 140° and developed such that an etching mask pattern can be formed. After the P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, have been etched, the etching mask pattern is removed such that the side surfaces of the etched P-type semiconductor layer 40 and active layer 30 can have a variety of slopes of 80 to 20°.

[0064] Next, in order to form a plurality of light emitting cells on the substrate 10, predetermined regions of the exposed N-type semiconductor layer 20 are removed such that a portion of the substrate 10 can be exposed. To this end, a predetermined mask pattern is formed on all the portions except the predetermined regions where the substrate 10 will be exposed, and regions of the N-type semiconductor layer 20 that are exposed through the mask pattern are then etched such that the plurality of light emitting cells can be electrically

isolated from one another as shown in Fig. 8. At this time, the mask pattern whose side surface is inclined through the aforementioned process is formed and then used to etch the exposed N-type semiconductor layer 20 such that the side surface of the N-type semiconductor layer 20 in which the plurality of light emitting cells are separated from one another is not perpendicular to but inclined at a predetermined slope from a horizontal plane.

[0065] Referring to Fig. 9, the N-type semiconductor layer 20 of a light emitting cell and the P-type semiconductor layer 40 of the adjacent light emitting cell are connected through a predetermined wiring process. That is, the exposed N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent light emitting cell are connected through a wire 60. At this time, the conductive wire 60 for electrically connecting the N-type and P-type semiconductor layers 20 and 40 are formed through a bridge process.

[0066] The aforementioned bridge process is also called an air-bridge process. In the air-bridge process, a photosensitive liquid is applied between chips to be connected with each other through a photo process and developed to form a photoresist pattern, a material such as metal is first formed into a thin film on the photoresist pattern through a vacuum vapor deposition method or the like, and a conductive material containing gold (Au) is applied at a predetermined thickness onto the thin film through an electroplating, electroless plating or metal vapor deposition method. Thereafter, if the photoresist pattern is removed with a solution of a solvent or the like, a lower portion of the conductive material is completely removed, and thus, only the bridge-shaped conductive material is formed in a space between the adjacent light emitting cells.

[0067] The wire 60 may be made of not only metal but also all kinds of conductive materials. It will be apparent that a silicone compound doped with impurities may be used.

[0068] Further, in order to apply an external voltage to the light emitting device, a

P-type bonding pad 50 is formed on the P-type semiconductor layer 40 of the light emitting cell positioned at one edge of the substrate 10 and an N-type bonding pad 55 is formed on the exposed N-type semiconductor layer 20 of the light emitting cell positioned at the other edge of the substrate 10.

[0069] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment but is not limited thereto. Various modifications can be made or various material films can be further added. For example, in order to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10.

[0070] Accordingly, a light emitting device in which the plurality of light emitting cells each of which side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at predetermined slope from a horizontal plane are connected with one another can be manufactured.

[0071] Figs. 10 to 13 are sectional views illustrating a process of manufacturing a light emitting device according to a third embodiment of the present invention.

[0072] The third embodiment is almost the same as the second embodiment. In the second embodiment, the N-type semiconductor layer 20 is first exposed and a portion of the exposed N-type semiconductor layer 20 is then removed to separate the light emitting cells from one another. In the third embodiment, however, a plurality of light emitting cells are first separated, and a portion of an N-type semiconductor layer 20 is then exposed. Descriptions overlapping with the previous embodiments will be omitted herein.

[0073] Referring to Fig. 10, portions of an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40, which are sequentially formed on a

substrate 10, are removed to form a plurality of light emitting cells. To this end, after a photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 40 and light-exposed, it is immediately developed without hard-baking such that an etching mask pattern can be formed. The portions of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor pattern 20, which are exposed through the etching mask pattern, and the etching mask pattern is removed to separate the light emitting cells from one another. Accordingly, a light emitting device in which entire side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at a predetermined slope can be obtained as shown in this figure. Further, the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are removed using the etching mask pattern in which a photoresist is applied at a thickness of 3 to 50μm on the P-type semiconductor layer 40 and light-exposed and hard-baked at a temperature of 100 to 140° and then developed. Accordingly, the entire side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 can be formed at various slopes of 80 to 20°.

[0074] Thereafter, as shown in Fig. 11, portions of the P-type semiconductor layer 40 and the active layer 30 are removed to expose a portion of the N-type semiconductor layer 20 through a predetermined etching process.

[0075] Referring to Fig. 12, the N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent light emitting cell are connected with each other through a bridge process.

[0076] Further, in order to apply an external voltage to the light emitting device, a P-type bonding pad 50 is formed on the P-type semiconductor layer 40 of the light emitting cell positioned at one edge of the substrate 10 and an N-type bonding pad 55 is formed on the exposed N-type semiconductor layer 20 of the light emitting cell positioned at the other edge

of the substrate 10.

[0077] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment but is not limited thereto. Various modifications can be made and various material films may be further added. For example, in order to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10.

[0078] Further, even in a case where the plurality of light emitting cells are separated by etching such that the side surfaces may have various slopes as shown in Fig. 10 and then etched to expose the N-type semiconductor layer 20, a light emitting device can be manufactured using the same etching process as described above. That is, as shown in Fig. 11, the side surfaces of the P-type semiconductor layer 40 and the active layer 30, which are etched to expose the N-type semiconductor layer 20, can be formed at various slopes.

[0079] Accordingly, a light emitting device in which the plurality of light emitting cells each of which side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at predetermined slope from a horizontal plane are connected with one another can be manufactured.

[0080] Figs. 14 to 17 are sectional views illustrating a process of manufacturing a light emitting device according to a fourth embodiment of the present invention.

[0081] The fourth embodiment is almost the same as the third embodiment. In the third embodiment, a conductive wire for electrically connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell is formed through a bridge process. In the fourth embodiment, however, the conductive wire is formed through a step coverage process. Descriptions overlapping with the

previous embodiments will be omitted herein.

[0082] Referring to Fig. 14, even in a case where a plurality of light emitting cells are separated by etching such that the side surfaces may have various slopes and then etched to expose an N-type semiconductor layer 20 through the aforementioned process, the side surfaces of P-type semiconductor layer 40 and active layer 30, which are etched to expose the N-type semiconductor layer 20, are formed with various slopes. Further, in order to reduce the resistance of the P-type semiconductor layer 40 and enhance the transmittance of light, a transparent electrode layer 85 may be further formed on a top surface of the P-type semiconductor layer 40. Further, an additional ohmic metal layer 87 for facilitating the supply of current may be further formed on a top surface of the P-type semiconductor layer 40 or the exposed N-type semiconductor layer 20. The transparent electrode layer 85 may be made of ITO (Indium Tin Oxide), ZnO or a conductive transparent metal, and the ohmic metal layer 87 may be made of Cr or Au.

[0083] Referring to Fig. 15, a continuous insulation layer 70 is formed on an entire surface of the substrate 10 with the plurality of light emitting cells formed thereon. The insulation layer 70 covers the side surfaces and top surfaces of the light emitting cells and the top surfaces of the substrate 10 between the adjacent light emitting cells. For example, the insulation layer 70 may be formed as a silicone oxide film using a CVD (Chemical Vapor Deposition) technique.

[0084] Since the side surfaces of the light emitting cells are inclined, the insulation layer 70 can easily cover the side surfaces of the light emitting cells. Since the total thickness of the N-type semiconductor layer 20 and active layer 30 is small and spaces between the adjacent P-type semiconductor layers 40 are broad, the side surfaces of the P-type semiconductor layers 40 adjacent to the exposed regions of the N-type semiconductor layers 20 can be easily covered with the insulation layer 70.

[0085] Referring to Fig. 16, an opening portion is formed on each of the exposed N-type and P-type semiconductor layers 20 and 40 of the light emitting cell by patterning the insulation layer 70 through a predetermined etching process. If the transparent electrode layer 85 and/or the ohmic metal layer 87 are formed as shown in this figure, the transparent electrode layer 85 and/or the ohmic metal layer 87 are exposed through the opening portion.

[0086] Referring to Fig. 17, a wire 80 is formed on the insulation layer 70 with the opening portion. The wire 80 connects the N-type and P-type semiconductor layers 20 and 40 through the opening portion thereof. That is, the N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent the light emitting cell are electrically connected with the wire.

[0087] The wire 80 may be formed using a plating technique. That is, after an etching mask pattern with an opening portion defining a region of the wire 80 has been formed on the insulation layer 70 and a metal layer has been plated within the opening portion, the etching mask pattern is removed and thus the wire 80 can be formed.

[0088] Further, the wire 80 may be formed using the CVD (Chemical Vapor Deposition) or PVD (Physical Vapor Deposition) technique. That is, a metal layer is formed using a vapor deposition technique such as electron beam deposition and then patterned using a photo and etching process, so that the wire 80 can be formed. Since the side surface of the light emitting cell is inclined, the metal layer is continuously formed on the upper side surface of the light emitting cell.

[0089] The light emitting device in which the wire 80 is formed as described above has an advantage in that it is possible to prevent the wire 80 from being disconnected or shorted due to external pressure and also prevent conductive materials such as metal, which remains while the wire 80 is formed, from shorting the light emitting cell.

[0090] Accordingly, a light emitting device in which the plurality of light emitting

cells each of which side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at predetermined slope from a horizontal plane are connected with one another can be manufactured.

[0091] As described above, the light emitting device according to the present invention is formed such that the side surfaces of the P-type semiconductor layer, the active layer and a portion of the N-type semiconductor layer are not perpendicular (90°) to but inclined at a predetermined slope from a horizontal plane. Therefore, luminous efficiency of the light emitting device of the present invention can be enhanced as compared with that of the conventional light emitting device. The reason is that a photon reflected on a flat surface in the prior art is not reflected on a surface with a different angle but emitted to the outside.

[0092] Fig. 18 is a conceptual sectional view illustrating a light emitting device with a flip chip structure according to the present invention.

[0093] Referring to Fig. 18, the light emitting device comprises a light emitting layer, i.e. an N-type semiconductor layer 120, an active layer 130 and a P-type semiconductor layer 140 sequentially formed on a base substrate 110. Further, the light emitting device comprises a submount substrate 200 onto which the base substrate 110 with the light emitting layer formed thereon is flip-chip bonded through metal bumps 150 and 155. A side surface of the light emitting layer comprising the P-type semiconductor layer 140, the active layer 130 and the N-type semiconductor layer 120 is inclined at a slope of 20 to 80°from the horizontal plane and a critical angle of light is changed due to the side surface such that the light can be easily extracted. Therefore, luminous efficiency of the light emitting device can be improved.

[0094] Figs. 19 to 23 are sectional views illustrating a process of manufacturing a light emitting device according to a fifth embodiment of the present invention.

[0095] Referring to Fig. 19, an N-type semiconductor layer 120, an active layer

130 and a P-type semiconductor layer 140 are sequentially formed on a base substrate 110.

[0096] The base substrate 110 refers to a general wafer used for fabricating a light emitting device is made of a transparent substrate such as Al_2O_3, ZnO and $LiAl_2O_3$. In this embodiment, a crystal growth substrate made of sapphire is used.

[0097] The N-type semiconductor layer 120, the active layer 130 and the P-type semiconductor layer 140 are sequentially formed on the substrate 110 through various deposition methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like. A buffer layer may be further formed on the substrate 110 to reduce lattice mismatch between the substrate 110 and the subsequent layers upon growth of crystals. The aforementioned components are the same as those in the previous embodiments, and thus, descriptions overlapping with the foregoing components will be omitted herein.

[0098] Thereafter, portions of the P-type semiconductor layer 140 and the active layer 130 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 120. This etching process is the same as that of the previous embodiments.

[0099] That is, after a photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 140 of Fig. 19 and light-exposed, it is immediately developed without hard-baking to form an etching mask pattern. The P-type semiconductor 140 and the active layer 130, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer 120. Thereafter, if the etching mask pattern is removed, side surfaces of the P-type semiconductor layer 140 and the active layer 130 which are not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane can be obtained as

shown in Fig. 20.

[0100] Alternatively, after a photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 140 of Fig. 19 and light-exposed, it is hard-baked at a temperature of 100 to 140°C and then developed such that an etching mask pattern can be formed. After the P-type semiconductor layer 140 and the active layer 130, which are exposed through the etching mask pattern, have been etched, the etching mask pattern is removed such that the side surfaces of the etched P-type semiconductor layer 140 and active layer 130 can have a variety of slopes of 80 to 20°.

[0101] A reflection layer for reflecting light may be further formed on a top surface of the P-type semiconductor layer 140, and an additional ohmic metal layer for facilitating the supply of current may be further formed on a top surface of the P-type semiconductor layer 140 or the exposed N-type semiconductor layer 120. The ohmic metal layer may be made of Cr or Au.

[0102] Further, P-type and N-type metal bumps 155 and 150 are formed on the P-type and N-type semiconductor layers 140 and 120, respectively, as shown in Fig. 21. Each of the P-type and N-type metal bumps 155 and 150 may be made of at least one material selected from the group consisting of Pb, Sn, Au, Ge, Cu, Bi, Cd, Zn, Ag, Ni, Ti and an alloy thereof. To this end, a photoresist is applied onto an entire structure and a photoresist pattern (not shown) through which portions of the P-type and N-type semiconductor layers 140 and 120 are exposed is formed through a photo-etching process using a predetermined mask. After a metal film has been deposited on the entire structure, metal film portions formed on regions other than regions on the P-type and N-type semiconductor layers 140 exposed through the photoresist pattern and the photoresist pattern are removed. Accordingly, the P-type and N-type metal bumps 155 and 150 are formed on the P-type and N-type semiconductor layers 140 and 120, respectively.

[0103] Next, referring to Fig. 22, an additional submount substrate 200 is prepared to form P-type and N-type bonding pads 215 and 210 connected to the P-type and N-type metal bumps 155 and 150, respectively.

[0104] At this time, various kinds of superior heat conductive substrates 200 are used as the submount substrate 200. That is, the submount substrate 200 may be made of SiC, Si, Ge, SiGe, AlN, metal or the like. In this embodiment, AlN with superior heat conductivity and insulation property is used. The present invention is not limited thereto, but a metallic material with superior heat and electric conductivity may be employed. In this case, an insulation or dielectric film is formed on the substrate 200 to sufficiently serve as an insulation. The dielectric film may be made of SiO2, MgO and SiN or an insulating material. Further, each of the P-type and N-type bonding pads 210 and 215 is made of a metal with superior electric conductivity. This is formed through a screen printing process or a deposition process using a predetermined mask pattern.

[0105] Thereafter, the submount substrate 200 is flip-chip bonded onto the base substrate 110 with the light emitting layer formed thereon.

[0106] Referring to Fig. 23, in the light emitting device of the present invention, the N-type and P-type metal bumps 150 and 155 formed on the top of the light emitting layer are bonded and connected with the N-type and P-type bonding pads 210 and 215 of the submount substrate 200, respectively. At this time, the bonding pads and metal bumps may be bonded using heat or ultrasonic waves or simultaneously using the heat and ultrasonic waves. The metal bumps 150 and 155 and the lower bonding pads 210 and 215 are connected through a variety of bonding methods.

[0107] Moreover, the N-type and P-type metal bumps 150 and 155 are not formed on the top of the light emitting layer but may be formed on the submount substrate 200.

[0108] As can be seen from this figure, a plurality of light emitting devices may be

fabricated on a single substrate 10, which is cut into the individual light emitting devices. At this time, portions A shown in Fig. 23 are cutting portions used for individually cutting the plurality of light emitting devices.

[0109] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto. Various processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes. For example, in the same process as the previous embodiments, the base substrate with the N-type semiconductor layer, the active layer and the P-type semiconductor layer sequentially formed thereon is prepared as shown in Fig. 19. Then, portions of the P-type semiconductor layer, the active layer and the N-type semiconductor layer are first removed to expose the substrate such that the plurality of light emitting devices can be individually isolated. At this time, the side surfaces of the P-type semiconductor layer, the active layer and the N-type semiconductor layer, which are etched through the aforementioned process, may be formed not to be perpendicular (90°) to but inclined at a predetermined slope.

[0110] Accordingly, a light emitting device with a flip chip structure, in which the side surfaces of the P-type semiconductor layer, the active layer and a portion of the N-type semiconductor layer are not perpendicular (90°) to but inclined at the predetermined slope from the horizontal plane, can be manufactured.

[0111] Figs. 24 to 28 are sectional views illustrating a process of manufacturing a light emitting device according to a sixth embodiment of the present invention.

[0112] The sixth embodiment is almost the same as the fifth embodiment. In the sixth embodiment, however, there is provided a light emitting device with a flip chip structure, in which a plurality of light emitting cells are connected in series, parallel or series-parallel in a wafer level to reduce the size of the device, and they can be driven at proper

voltage and current to be used for illumination purpose and can also be driven even with an AC power source. Descriptions overlapping with the previous embodiments will be omitted herein.

[0113] Referring to Fig. 24, an N-type semiconductor layer 120, an active layer 130 and a P-type semiconductor layer 140 are sequentially formed on a base substrate 110 through various deposition methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like. A buffer layer may be further formed on the substrate 110 to reduce lattice mismatch between the substrate 110 and the subsequent layers upon growth of crystals.

[0114] Thereafter, portions of the N-type semiconductor layer 120, the active layer 130 and the P-type semiconductor layer 140, which are sequentially formed on the base substrate 110, are removed to form a plurality of light emitting cells. To this end, after a photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 140 of Fig. 24 and light-exposed, it is immediately developed without hard-baking to form an etching mask pattern. The P-type semiconductor 140, the active layer 130 and the predetermined N-type semiconductor layer 120, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to separate the light emitting cells from one another. Next, if the etching mask pattern is removed, a light emitting device in which entire side surfaces of the etched P-type semiconductor layer 140, active layer 130 and N-type semiconductor layer 120 are not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane can be obtained as shown in Fig. 25.

[0115] Alternatively, after a photoresist has been applied at a thickness of 3 to 50μm on the P-type semiconductor layer 140 of Fig. 24 and light-exposed, it is hard-baked at

a temperature of 100 to 140°C and developed such that an etching mask pattern can be formed. After the P-type semiconductor layer 140, the active layer 130 and the N-type semiconductor layer 120, which are exposed through the etching mask pattern, have been etched, the etching mask pattern is removed such that the side surfaces of the etched P-type semiconductor layer 140 and active layer 130 can be inclined at various slopes of 80 to 20°.

[0116] Next, portions of the P-type semiconductor layer 140 and the active layer 130 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 120, as shown in Fig. 26. The exposed N-type semiconductor layer 120 of one light emitting cell and the P-type semiconductor layer 140 of another adjacent light emitting cell are connected with each other through a predetermined conductive wire. At this time, a bridge wire 160 is made of a conductive material, e.g. metal. It will be apparent that the bridge wire 160 may be made of a silicone compound doped with impurities. The bridge wire 160 is formed through a bridge process.

[0117] Further, a plurality of metal bumps are formed on the top of the light emitting cells, and P-type and N-type metal bumps 155 and 150 are further formed on the P-type semiconductor layer 140 of the light emitting cell positioned at one edge of the substrate 110 and the N-type semiconductor layer 120 of the light emitting cell positioned the other edge of the substrate, respectively.

[0118] Next, as shown in Fig. 27, an additional submount substrate 200 is prepared, on which a plurality of bonding layers 220, a P-type bonding pad 215 positioned at one edge of the submount substrate 200 and an N-type bonding pad 210 positioned at the other edge of the submount substrate are formed.

[0119] Thereafter, as can be shown in Fig. 28, the aforementioned base substrate 110 with the plurality of light emitting cells formed thereon is flip-chip bonded onto the submount substrate 200 to fabricate the light emitting device. The substrates are bonded

with each other through the metal bumps 150 and 155 formed on the top of the light emitting cell and the bonding layers 220 formed on the submount substrate 200, respectively. The P-type bonding pad 215 positioned at one edge of the submount substrate 200 is connected to the P-type metal bump 155 of the light emitting cell positioned at one edge of the base substrate 110, whereas the N-type bonding pad 210 positioned at the other edge of the submount substrate 200 is connected to the N-type metal bump 150 of the light emitting cell positioned at the other edge of the base substrate 110.

[0120] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto. Various processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes. For example, in this embodiment, the conductive wire for electrically connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell is formed through a bridge process, and the base substrate is then flip-chip bonded onto the submount substrate. However, the present invention is not limited thereto. That is, a conductive wire for electrically connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cells may be formed through a step coverage process which is the same as in the fourth embodiment. Further, an electrode layer may be formed on the submount substrate when the plurality of light emitting cells are flip-chip bonded onto the submount substrate such that the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are electrically connected through the metal bumps.

[0121] Accordingly, a light emitting device in which a plurality of flip chip light emitting cells each having a side surface of a light emitting layer, which is not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane, are arrayed on the

submount substrate can be manufactured. The light emitting cells may be connected in various ways, i.e. in series, parallel or series-parallel, depending on the desired purpose.

[0122] Fig. 29 is a sectional view showing a seventh embodiment according to the present invention.

[0123] The seventh embodiment is almost the same as the sixth embodiment. In this embodiment, even in a case where a plurality of light emitting cells are separated by etching such that the side surfaces may have slopes as shown in Fig. 25 and then etched to expose an N-type semiconductor layer, a light emitting device can be manufactured using the same etching process as the previous embodiment. That is, side surfaces of a P-type semiconductor layer 140 and an active layer 130 etched to expose an N-type semiconductor layer 120 are formed with various slopes, as shown in Fig. 29.

[0124] Accordingly, a light emitting device in which a plurality of flip chip light emitting cells each having an entire side surface of a light emitting layer, which is not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane, are arrayed on the submount substrate can be manufactured. The light emitting cells may be connected in various ways, i.e. in series, parallel or series-parallel, depending on the desired purpose.

[0125] As described above, the light emitting device with a flip chip structure according to the present invention is formed such that some side surfaces of a light emitting layer are not particular (90°) to but inclined at a predetermined slope from the horizontal plane. Therefore, luminous efficiency of the light emitting device of the present invention can be enhanced as compared with that of the conventional light emitting device. The reason is that a photon reflected on a flat surface in the prior art is not reflected on a surface with a different angle but emitted to the outside.

[0126] Figs. 30 and 31 are conceptual sectional views illustrating a difference

between effects of the light emitting devices according to the prior art and the present invention.

[0127] The light efficiency of a light emitting device may be expressed as internal quantum efficiency and external quantum efficiency, and the internal quantum efficiency is determined in accordance with the design and quality of an active layer. The external quantum efficiency is determined in accordance with a degree where a photon produced in an active layer is emitted to the outside of a light emitting device. Referring to Fig. 30 in which a conventional light emitting device is shown, a side surface of a semiconductor layer is formed perpendicular to a horizontal plane. In such a case, some portions of photons are not penetrated through the side surface of the semiconductor layer but reflected thereon, and totally reflected light is not emitted to the outside but dissipated within the light emitting device. However, referring to Fig. 31 in which a light emitting device according to the present invention is shown, a side surface of a semiconductor layer is not perpendicular to but inclined at a predetermined slope from a horizontal plane. In such a case, the inclined side surface makes a critical angle of light change to help the light to be more easily extracted. Therefore, light generated in an active layer is not totally reflected but emitted to the outside of the light emitting device such that external quantum efficiency can be markedly enhanced.

[0128] Fig. 32 is a sectional view illustrating a light emitting diode for AC operation according to the eighth embodiment of the present invention.

[0129] Referring to Fig. 32, a plurality of light emitting cells 56 are disposed to be spaced apart in a substrate 51. The substrate 51 may be insulating or conducting one, and may be, for example, a sapphire or a silicon carbide (SiC) substrate.

[0130] The light emitting cells 56 respectively include a lower semiconductor layer 55, an upper semiconductor layer 59 disposed in a region of the lower semiconductor layer, and an active layer 57 disposed between the lower semiconductor layer and the upper

semiconductor layer. The upper and the lower semiconductor layers may be N-type and P-type, respectively. Alternatively the upper and the lower semiconductor layers may be P-type and N-type, respectively.

[0131] The lower semiconductor layer 55, active layer 57 and upper semiconductor layer 59 may include a gallium nitride-based semiconducting material, for example, (B, Al, In, Ga)N. Elements and stoichiometry of the active layer 57 may be determined so that a light having a desired wavelength, for example, ultraviolet ray or blue light, can be emitted. The lower semiconductor layer 55 and upper semiconductor layer 59 are formed of a material having a greater bandgap compared with the active layer 57.

[0132] The lower semiconductor layer 55 and/or the upper semiconductor layer 59 may be, as illustrated, formed of a single layer or multiple layers. The active layer 57 may have a single-quantum-well structure or a multiple-quantum-well structure.

[0133] A buffer layer 53 may be disposed between the light emitting cells 56 and the substrate 51. The buffer layer 53 is employed to reduce a lattice mismatch between the substrate 51 and the lower semiconductor layer 55 formed thereon. The buffer layer 53 may be continuous as illustrated, but it is not limited thereto. The buffer layer 53 may be disposed under the lower semiconductor layers 55 to be discontinuous.

[0134] Side surfaces of the light emitting cells 56 are formed to be inclined with respect to an upper surface of the substrate 51 and get narrowed toward upside. The inclination of the side surfaces improves emission efficiency of a light produced in the active layer 57, and helps conformal deposition of other layers which will be formed on the light emitting cells 56. In the exemplary embodiment, the inclinations of the side surfaces of the respective lower semiconductor layers 55 of the light emitting cells 56 may be in a range of approximately 15 degrees to approximately 80 degrees.

[0135] An insulation layer 69 covers an entire surface of the light emitting cells 56.

The insulation layer 69 include opening portions on other regions of the lower semiconductor layers 55, for example, a region adjacent to a region on which the upper semiconductor layer 59 is formed, and include opening portions on the upper semiconductor layers 59. The opening portions are space apart from each other, and therefore, the side surfaces of the light emitting cells 56 are covered with the insulation layer 69. The insulation layer 69 may cover the substrate 51 in regions between the light emitting cells 56, or the buffer layer 53. The insulation layer 69 may include a silicon oxide (SiO2) layer.

[0136] Wires 71 are formed on the insulation layer 69. The wires 71 are electrically connected to the lower semiconductor layers 55 and the upper semiconductor layers 59 through the opening portions. In addition, the wires 71 respectively connect the lower semiconductor layers 55 and the upper semiconductor layers 59 of the adjacent light emitting cells 56 to form a series array of the light emitting cells 56. The array may be formed in plurality, and a plurality of arrays may be connected to be reverse parallel and connected to AC power to be driven. Further, a bridge rectifier (not shown) connected to the series array of the light emitting cells may be formed, and the light emitting cells may be driven with AC power by the bridge rectifier. The bridge rectifier may be formed by connecting light emitting cells having substantially the same structure as the light emitting cells using wires 71. The wires may be formed of a conductive material, for example, a doped semiconducting material such as polycrystalline silicon or a metal.

[0137] Meanwhile, electrode pads may be disposed between other regions of the lower semiconductors 55 and the insulation layer 69. The electrode pads 67 are exposed by the opening portions formed in other regions of the lower semiconductor layers 55. The electrode pads 67 have ohmic contacts to the lower semiconductor layers 55. The wires 71 are in contact with the electrode pads 67 exposed by the opening portions to be electrically connected to the lower semiconductor layers 55.

[0138] Transparent electrode layers 65 may be disposed between the upper semiconductor layers 59 and the insulation layers 69. The transparent electrode layers 65 are exposed by the opening portions formed on the upper semiconductor layers 59. The transparent electrode layers 65 transmit light produced in the active layer 57, and disperse and supply currents to the upper semiconductor layers 59. The wires 71 are in contact with the transparent electrode layers 65 exposed by the opening portions to be electrically connected to the upper semiconductor layers 55. Electrode pads (not shown) may be further formed on the transparent electrode layers 65 and the wires 71 may be in contact with the electrode pads.

[0139] A protecting insulation layer 73 may cover the wires 71 and the insulation layer 69. The protecting insulation layer 73 substantially reduces contamination of the wires 71 from moisture and so forth, and damage of the wires 71 from external pressure. The protecting insulation layer 73 may be formed of a light-transmitting material, for example, silicon oxide layer.

[0140] Figs. 33 to 38 are sectional views illustrating a process of manufacturing a light emitting diode according to the eighth embodiment of the present invention.

[0141] Referring to Fig. 33, a lower semiconductor layer 55, an active layer 57, and an upper semiconductor layer 59 are formed on a substrate 51. A buffer layer 53 may be formed on the substrate 51 before the lower semiconductor layer 55 is formed.

[0142] The substrate 51 may be sapphire (Al2O3), silicon carbide (SiC), zinc oxide (ZnO), silicon (Si), gallium arsenide (GaAs), gallium phosphate (GaP), lithium-alumina (LiAl2O3), boron nitride (BN), aluminum nitride (AlN) or gallium nitride (GaN). However, it is not limited thereto and may be variable according to a semiconducting material which is to be formed on the substrate 51.

[0143] The buffer layer 53 is formed to reduce lattice mismatch between the

substrate 51 and the semiconductor layer 55 which is to be formed thereon. The buffer layer 53 may include, for example, gallium nitride (GaN) or aluminum nitride (AlN). When the substrate 51 is a conductive substrate, the buffer layer 53 may be formed of an insulation layer or a semi-insulation layer, for example, AlN or semi-insulating GaN.

[0144] The lower semiconductor layer 55, active layer 57 and upper semiconductor layer 59 may include a gallium nitride-based semiconducting material, for example, (B, Al, In, Ga)N. The lower and upper semiconductor layers 55 and 59 and the active layer 57 may be formed continuously or discontinuously using, for example, metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy or hydride vapor phase epitaxy (HNPE) technology.

[0145] The upper and the lower semiconductor layers may be N-type and P-type, respectively. Alternatively the upper and the lower semiconductor layers may be P-type and N-type, respectively. In the gallium nitride-based compound semiconductor layer, N-type semiconductor layer may be doped with, for example, silicon (Si), and P-type semiconductor layer may be doped with, for example, magnesium (Mg).

[0146] Photoresist patterns 63 defining light emitting cell regions are formed on the upper semiconductor layer 59. The photoresist patterns are formed to cover the light emitting cell regions. Reflow of the photoresist patterns 63 is performed so that side surfaces can be inclined with respect to an upper surface of the substrate 51. The side surfaces of the photoresist patterns 63 may be formed to have an inclination angle in a range of approximately 15 degree to 80 degree with respect to the upper surface of the substrate 51.

[0147] Referring to Fig. 34, the upper semiconductor layer 59, the active layer 57 and the lower semiconductor layer 55 are sequentially etched using the photoresist patterns 63 as etching mask. Accordingly, the shape of the photoresist patterns 63 is reproduced in the semiconductor layers 59, 57 and 55 and the light emitting cells with inclined side surfaces

are separated. The buffer layer 53 may be exposed and the exposed buffer layer 53 may be removed by over-etching.

[0148] Thereafter, the photoresist patterns 63 are removed, and the upper semiconductor layer and the active layer are patterned again to expose the etched lower semiconductor layers 55. The exposed lower semiconductor layers may be partially etched by over-etching. Accordingly, light emitting cells 56 that are spaced apart are formed on the substrate 51. Each of the light emitting cells 56 includes the lower semiconductor layer 56 which is spaced apart by etching, the upper semiconductor layer 57 disposed on an upper side of a region of the lower semiconductor layer 56, and the active layer 57 disposed between the lower semiconductor layer 55 and the upper semiconductor layer 57. Other region of the lower semiconductor layer 56 is exposed. Further, most of the side surfaces of the light emitting cells 56 are formed to be inclined with respect to an upper surface of the substrate 51. Whereas, side surfaces of the upper semiconductor layers 59 adjacent to other regions of the lower semiconductor layers 55 may be formed to be inclined as illustrated, and alternatively, may be formed vertically.

[0149] Referring to Fig. 35, a transparent electrode layer 65 may be formed on the upper semiconductor layer 59 of the light emitting cell 56. The transparent electrode layer 65 includes a transparent metal such as indium tin oxide (ITO) layer or Ni/Au. Further, electrode pads 67 may be formed on other regions of the lower semiconductor layers 55. The electrode pads 67 have an ohmic contact with the lower semiconductor layers 55.

[0150] The transparent electrode layer 65 may be formed on the upper semiconductor layer 59 before the photoresist patterns are formed. The transparent electrode layer 65 is patterned together with the upper semiconductor layer

[0151] Referring to Fig. 36, a continuous insulation layer 69 is formed on an entire surface of the substrate 51 with the plurality of light emitting cells 56 formed thereon. The

insulation layer 69 covers the side surfaces and top surfaces of the light emitting cells 56, and the top surfaces of the substrate 51 between the adjacent light emitting cells 56. For example, the insulation layer 69 may be formed as a silicone oxide film using a CVD (Chemical Vapor Deposition) technique.

[0152] Since the side surfaces of the light emitting cells 56 are inclined, the insulation layer 69 can easily cover the side surfaces of the light emitting cells 56. Since the total thickness of the upper semiconductor layer 59 and active layer 57 is small and spaces between the upper semiconductor layers 59 are broad, the side surfaces of the upper semiconductor layers 59 adjacent to other regions of the lower semiconductor layers 55 can be easily covered with the insulation layer 69.

[0153] Referring to Fig. 37, an opening portions are formed on other regions of the lower semiconductor layers 55 and the upper semiconductor layers 59 by patterning the insulation layer 69. If the electrode pads 67 and the transparent electrode layers 65 are formed, the electrode pads 67 and the transparent electrode layers 65 are exposed through the opening portions.

[0154] The opening portions may be formed using a photo and etching process, and the electrode pads 67 substantially reduce damage of the lower semiconductor layers 55 while the insulation layer 69 is etched.

[0155] Referring to Fig. 38, wires 71 are formed on the insulation layer 69 with the opening portions. The wire 71 are electrically connected to the lower semiconductor layers 55 and the upper semiconductor layers 59 through the opening portions, and connect the lower semiconductor layers 55 and the upper semiconductor layers 59 of the adjacent light emitting cells 56 to form arrays connected in series.

[0156] The wires 71 may be formed using a plating technique. That is, the wires 71 may be formed by forming a photoresist pattern having opening portions defining wire

region on the insulation layer 69, plating a metal layer in the opening portions, and removing the photoresist pattern.

[0157] Alternatively, the wires 71 may be formed using CVD (Chemical Vapor Deposition) or PVD (Physical Vapor Deposition) technique. That is, a metal layer is formed using a vapor deposition technique such as electron beam deposition and then patterned using a photo and etching process, so that the wires 71 can be formed. Since the insulation layer 69 covers the side surfaces of the light emitting cells 56, short-circuiting of the light emitting cells 56 due to a remaining metallic material after patterning of metal layer may be prevented.

[0158] A protecting insulation layer 73 is formed on the substrate 51 with the wires 71 formed thereon. The protecting insulation layer 73 is formed of a light-transmitting material, for example, silicon oxide layer using chemical vapor deposition technique. In this way, a light emitting diode for AC operation.

[0159] According to the eighth embodiment, a reliable light emitting diode for AC operation can be provided by preventing disconnection or short circuit of wires by external pressure, and short circuit of a light emitting cell by a conductive material such as metal residue while the wires are formed may be prevented. Further, the wires may be formed to be supported by insulation layers, so that a reliable light emitting diode for AC operation can be manufactured.

[0160] Although the present invention has been described in detail in connection with the specific embodiments, it will be readily understood by those skilled in the art that various modifications and changes can be made thereto within the technical spirit and scope of the present invention. It is also apparent that the modifications and changes fall within the scope of the present invention defined by the appended claims.

LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

[0001] Field of Invention

[0002] The present invention relates to a light emitting device and a method of manufacturing the same. More particularly, the present invention relates to a nitride based semiconductor light emitting device with enhanced luminous efficiency and brightness and a method of manufacturing the light emitting device.

[0003] Description of the Related Art

[0004] A light emitting device refers to an element in which minority carriers (electrons or holes) injected using a p-n junction structure of a semiconductor are produced and certain light is emitted due to recombination of the carriers. A light emitting source is formed from any one or combination of compound semiconductor materials such as GaAs, AlGaAs, GaN, InGaN and AlGaInP, so that a variety of colors can be implemented. For example, a red light emitting device may be formed from GaAsP or the like; a green light emitting device may be formed from GaP, InGaN or the like; a blue light emitting device may be formed using an InGaN/GaN double hetero structure; and a UV light emitting device may be formed using an AlGaN/GaN or AlGaN/AlGaN structure.

[0005] In particular, GaN has a direct bandgap of 3.4eV at a normal temperature and a direct energy bandgap of 1.9eV (InN) to 3.4eV (GaN) or 6.2eV (AlN) by combining with a substance such as InN or AlN. Thus, GaN is a substance with great applicability to an optical element due to its broad wavelength range from visible light to ultraviolet light. Since the wavelength can be adjusted in such a manner, full-color implementation can be made by means of red, green and blue light emitting devices with a short wavelength range, so that the applicability to a general illumination market as well as a display device market is

expected to be greatly increased.

[0006] Light emitting devices have characteristics of lower power consumption, longer lifespan, better installation in a narrow space and stronger resistance against vibration as compared with existing bulbs or fluorescent lamps. Since the light emitting devices are used as display devices and backlights and have superior characteristics in view of the reduction in power consumption and the durability, many studies for applying the light emitting devices to a general illumination field have been recently conducted. In the future, their applicability is expected to extend to a backlight of a large-sized LCD-TV, a vehicle headlight and general illumination. To this end, it is necessary to improve luminous efficiency of light emitting devices, solve a heat dissipation problem, and achieve high brightness and output of the light emitting devices.

[0007] Many techniques for enhancing the performance of light emitting devices have been currently developed. There are various indexes indicating the performance of light emitting devices, such as luminous efficiency (lm/W), internal quantum efficiency (%), external quantum efficiency (%) and extraction efficiency (%). The extraction efficiency is determined as a ratio of electrons injected into the light emitting device to photons emitted to the outside of the light emitting device. That is, the light emitting device becomes bright as the extraction efficiency becomes high. Since the extraction efficiency of the light emitting device is much influenced by the shape and surface pattern of a chip, the structure of a chip and a packaging type, careful attention should be paid when designing the light emitting device.

[0008] Fig. 1 is a sectional view showing a conventional light emitting device with a horizontal structure.

[0009] Referring to Fig. 1, the light emitting device comprises a substrate 1, an N-type semiconductor layer 2 formed on the substrate 1, an active layer 3 formed on a portion

of the N-type semiconductor layer 2 and a P-type semiconductor layer 4. That is, after the N-type semiconductor layer 2, the active layer 3 and the P-type semiconductor layer 4 have been sequentially formed on the substrate 1, predetermined regions of the P-type semiconductor layer 4 and the active layer 3 are etched to expose a portion of the N-type semiconductor layer 2. Then, a predetermined voltage is applied to top surfaces of the exposed N-type semiconductor layer 2 and the P-type semiconductor layer 4.

[0010] Fig. 2 is a sectional view showing a conventional light emitting device with a flip chip structure.

[0011] Referring to Fig. 2, the light emitting device comprises an N-type semiconductor layer 2, an active layer 3 and a P-type semiconductor layer 4, which are sequentially formed on a base substrate 1. The light emitting device further comprises a submount substrate 5 onto which the base substrate 1 is flip-chip bonded using metal bumps 8 and 9. To this end, the N-type semiconductor layer 2, the active layer 3 and the P-type semiconductor layer 4 are sequentially formed on the predetermined substrate 1, and portions of the P-type semiconductor layer 4 and the active layer 3 are etched to expose the N-type semiconductor layer 2 such that a light emitting cell can be formed. Further, the additional submount substrate 5 is prepared to form first and second electrodes 6 and 7 thereon, and the P-type and N-type metal bumps 8 and 9 are then formed on the first and second electrodes 6 and 7, respectively. Thereafter, the light emitting cell is bonded with the submount substrate 5 such that P and N electrodes of the light emitting cell are bonded with the P-type and N-type metal bumps 8 and 9, respectively, to fabricate a light emitting device. Since such a conventional light emitting device with a flip chip structure has high heat dissipation efficiency and hardly has shield of light, there is an advantage in that its light efficiency is increased by 50% or more as compared with a conventional light emitting device. Further, since a gold wire for driving a light emitting device is not necessary, many applications to a

variety of small-sized packages can be considered.

[0012] Light produced from a light emitting layer of a light emitting device is emitted from all the surfaces of a chip, and light extraction efficiency is generally determined by a critical angle of light. However, when the conventional light emitting device is etched to expose an N-type semiconductor layer, side surfaces of the P-type semiconductor layer and the active layer are vertically processed such that a portion of light produced within the light emitting device is totally reflected on the etched surface that is processed vertically from a horizontal plane. Then, a considerable amount of light to be totally reflected is not emitted to the outside but dissipated within the light emitting device due to the internal reflection. That is, there is a problem in that luminous efficiency in which electric energy is converted into light energy and the light is then emitted to the outside of a light emitting device is low.

SUMMARY OF THE INVENTION

[0013] The present invention is conceived to solve the aforementioned problems. Accordingly, an object of the present invention is to provide a light emitting device for emitting light with high luminous intensity and brightness by enhancing characteristics of luminous efficiency, external quantum efficiency, extraction efficiency and the like and improving reliability, and a method of manufacturing the light emitting device.

[0014] According to an aspect of the present invention for achieving the objects, there is provided a light emitting device, comprising a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on a portion of the N-type semiconductor layer on a substrate. The N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell may be connected to each other, and a side surface including the N-type or P-type semiconductor layer of the light emitting cell has a slope of 20 to 80° from a horizontal

plane. The light emitting device may further comprise a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell, a transparent electrode layer on the P-type semiconductor layer, and P-type and N-type ohmic metal layers containing Cr or Au on the P-type and N-type semiconductor layers, respectively.

[0015] According to another aspect of the present invention, there is provided a light emitting device comprising a substrate formed with a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on the N-type semiconductor layer and a submount substrate flip-chip bonded onto the substrate. Preferably, the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including at least the P-type semiconductor layer of the light emitting cell has a slope of 20 to 80°from a horizontal plane. The light emitting device may further comprise a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

[0016] According to further aspect of the present invention, there is provided a method of manufacturing a light emitting device, comprising the steps of sequentially forming N-type and P-type semiconductor layers on a substrate; forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; and removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern.

[0017] According to still further aspect of the present invention, there is a method of manufacturing a light emitting device comprising the steps of removing a portion of the N-type semiconductor layer exposed due to the removal of the P-type semiconductor layer to form a plurality of light emitting cells; and connecting the N-type semiconductor layer of one

light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire.

[0018] According to still further aspect of the present invention, there is a method of manufacturing a light emitting device comprising the step of flip-chip bonding the substrate onto an additional submount substrate after the step of removing the P-type semiconductor layer and the etching mask pattern. The method of manufacturing a light emitting device may further comprise the steps of removing a portion of the N-type semiconductor layer exposed through the removal of the P-type semiconductor layer to form a plurality of light emitting cell; and connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a conductive wire, after the step of removing the P-type semiconductor layer and the etching mask pattern.

[0019] The step of forming the plurality of light emitting cells may comprise the steps of forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; removing the N-type and P-type semiconductor layers exposed through the etching mask pattern to form a plurality of light emitting cells; and removing the etching mask pattern.

[0020] The N type semiconductor layer of one light emitting cell and the P type semiconductor layer of another adjacent light emitting cell may be connected with the conductive wire through a bridge or step coverage process.

[0021] A photoresist with a thickness of 3 to 50[[□]]μm may be used in the step of forming the etching mask pattern. The step of forming the etching mask pattern may comprise the steps of: applying the photoresist onto the P-type semiconductor layer; light exposing the photoresist in accordance with a predetermined mask pattern; and developing the light-exposed photoresist without a baking process after the light exposure. The step of

forming the etching mask pattern may comprise the steps of: applying the photoresist onto the P-type semiconductor layer; light exposing the photoresist in accordance with a predetermined mask pattern; hard baking the light-exposed photoresist at a temperature of 100 to 140℃; and developing the hard-baked photoresist.

[0022] After the step of removing the P-type semiconductor layer and the etching mask pattern, the method of manufacturing a light emitting device may further comprise the steps of removing a rear surface of the substrate at a certain thickness; and depositing Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof onto the rear surface of the substrate.

[0023] In a light emitting device and a method of manufacturing the same according to the present invention, light produced from a side surface of a semiconductor layer, which is not perpendicular to but inclined at a predetermined slop from a horizontal plane, is not totally reflected but emitted to the outside of the light emitting device. Therefore, more enhanced characteristics of light extraction efficiency, external quantum efficiency, luminous efficiency or the like can be obtained. Further, a light emitting device of the present invention emits light with high luminous intensity and brightness and can be applied to a variety of products in which a superior light characteristic is necessary.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The above and other objects, features and advantages of the present invention will become apparent from the following description of preferred embodiments given in conjunction with the accompanying drawings, in which:

[0025] Figs. 1 and 2 are sectional views showing conventional light emitting devices, respectively;

[0026] Fig. 3 is a conceptual sectional view illustrating a light emitting device with a horizontal structure according to the present invention;

[0027] Figs. 4 and 5 are sectional views illustrating a process of manufacturing a light emitting device according to a first embodiment of the present invention;

[0028] Figs. 6 to 9 are sectional views illustrating a process of manufacturing a light emitting device according to a second embodiment of the present invention;

[0029] Figs. 10 to 13 are sectional views illustrating a process of manufacturing a light emitting device according to a third embodiment of the present invention;

[0030] Figs. 14 to 17 are sectional views illustrating a process of manufacturing a light emitting device according to a fourth embodiment of the present invention;

[0031] Fig. 18 is a conceptual sectional view illustrating a light emitting device with a flip chip structure according to the present invention;

[0032] Figs. 19 to 23 are sectional views illustrating a process of manufacturing a light emitting device according to a fifth embodiment of the present invention;

[0033] Figs. 24 to 28 are sectional views illustrating a process of manufacturing a light emitting device according to a sixth embodiment of the present invention;

[0034] Fig. 29 is a sectional view showing a seventh embodiment according to the present invention; and

[0035] Figs. 30 and 31 are conceptual sectional views illustrating a difference

between effects of the light emitting devices according to the prior art and the present invention;

[0036] Fig. 32 is a sectional view illustrating a light emitting diode for AC operation according to an eighth embodiment of the present invention; and

[0037] Figs. 33 to 38 are sectional views illustrating a process of manufacturing a light emitting diode according to the eighth embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0038] Hereinafter, a light emitting device and a manufacturing method thereof according to the present invention will be described in detail with reference to the accompanying drawings. However, the present invention is not limited to the embodiments set forth herein but can be implemented in different forms. Rather, the preferred embodiments are merely provided to allow the present invention to be completely described herein and to fully convey the scope of the invention to those skilled in the art.

[0039] Fig. 3 is a conceptual sectional view illustrating a light emitting device with a horizontal structure according to the present invention.

[0040] Referring to Fig. 3, the light emitting device comprises a substrate 10, and an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40, which are sequentially formed on the substrate 10. Each of side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 has a slope of 80 to 20° from a horizontal plane such that a critical angle of light can be changed by such surfaces and light can be easily extracted. Therefore, luminous efficiency of a light emitting device can be improved.

[0041] Figs. 4 and 5 are sectional views illustrating a process of manufacturing a light emitting device according to a first embodiment of the present invention.

[0042] Referring to Fig. 4, an N-type semiconductor layer 20, an active layer 30

and a P-type semiconductor layer 40 are sequentially formed on a substrate 10.

[0043] The substrate 10 refers to a general wafer used for fabricating a light emitting device and is made of at least any one of Al_2O_3, SiC, ZnO, Si, GaAs, GaP, $LiAl_2O_3$, BN, AlN and GaN. In this embodiment, a crystal growth substrate made of sapphire is used.

[0044] A buffer layer (not shown) may be further formed on the substrate 10 to reduce lattice mismatch between the substrate 10 and the subsequent layers upon growth of crystals. The buffer layer may contain GaN or AlN that is a semiconductor material.

[0045] The N-type semiconductor layer 20 is a layer in which electrons are produced and is preferably made from GaN doped with N-type impurities. However, the N-type semiconductor layer 20 is not limited thereto but may use a material layer having a variety of semiconductor properties. The N-type semiconductor layer 20 including N-type $Al_xGa_{1-x}N(0\leq x\leq 1)$ is formed in this embodiment. Further, the P-type semiconductor layer 40 is a layer in which holes are produced and is preferably made from GaN doped with P-type impurities. However, the P-type semiconductor layer 40 is not limited thereto but may use a material layer with a variety of semiconductor properties. The P-type semiconductor layer 40 including P-type $Al_xGa_{1-x}N(0\leq x\leq 1)$ is formed in this embodiment. Moreover, InGaN may be used as the semiconductor layer. Further, each of the N-type and P-type semiconductor layers 20 and 40 may be formed as a multiple layer.

[0046] The active layer 30 has a predetermined bandgap and is a region where a quantum well is formed so that electrons and holes are recombined. The active layer 30 may contain InGaN. The wavelength of light emitted through the combination of electrons and holes varies according to the kind of a material constituting the active layer 30. Therefore, it is preferred that a semiconductor material contained in the active layer 30 be controlled depending on a target wavelength.

[0047] The aforementioned material layers are formed through a variety of

deposition and growth methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like.

[0048] Thereafter, portions of the P-type semiconductor layer 40 and the active layer 30 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 20. An etching mask pattern is formed on the P-type semiconductor layer 40, and the P-type semiconductor layer 40 and the active layer 30 are then removed through a dry or wet etching process to expose the N-type semiconductor layer 20.

[0049] Generally, in order to perform the etching process, a photoresist has been applied onto a top surface of the P-type semiconductor layer 40 at a thickness of 1 to 2[[□]]μm, and then soft-baked at a temperature of 80 to 90°C is performed. Next, an exposure process in which light in a UV range is irradiated through a predetermined photo mask to transfer a pattern formed on the mask to the applied photoresist is executed. Thereafter, the photoresist is hard-baked at a temperature of 100 to 120°C, and a developing process in which the photoresist at a portion with relatively weak combination through the exposure process is melted using a solvent is executed. A predetermined etching mask pattern is formed on the P-type semiconductor layer 40 through the above process.

[0050] However, in this embodiment, the photoresist is applied at a thickness of 3 to 50[[□]]μm which is thicker as compared with the prior art when the etching mask pattern is formed, and the exposure process is performed after the soft-baking. Next, if the photoresist is directly developed without the hard-baking, a developed side surface of the remaining photoresist is formed into an inclined surface not perpendicular (90°) to but inclined at a predetermined slope from a horizontal plane. Subsequently, if exposed regions of the P-type semiconductor layer 40, the active layer 30 and the predetermined N-type

semiconductor layer 20 are etched using the etching mask pattern with such a slope of the side surface, the side surfaces of the etched P-type semiconductor layer 40, active layer 30 and N-type semiconductor layer 20 can be similarly formed into an inclined surface not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane.

[0051] That is, after the photoresist has been applied at a thickness of 3 to 50[[□]]μm on the P-type semiconductor layer 40 of Fig. 4 and light-exposed, a developed etching mask pattern is immediately formed without the hard-baking. The P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer 20. A portion of the exposed N-type semiconductor layer 20 may be further removed. Thereafter, if the etching mask pattern is removed, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured as shown in Fig. 5.

[0052] Alternatively, after a photoresist has been applied at a thickness of 3 to 50[[□]]μm on the P-type semiconductor layer 40 of Fig. 4 and light-exposed, hard-baking may be performed. In such a case, if the photoresist is hard-baked at a temperature of 100 to 140°C and then developed, the side surface of the developed photoresist may be etched to have a slope of 80 to 20° from a horizontal plane. For example, in a case where the hard-baking is performed at a temperature of 100°C, an etching mask pattern with a slope of about 80° from the horizontal plane can be obtained, and the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 can have a slope of about 80° from the horizontal plane using the etching mask pattern. Further, in a case where the hard-baking is performed at a temperature of 140°C, an etching

mask pattern with a slope of about 20° from the horizontal plane can be obtained, and the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 can have a slope of about 20° from the horizontal plane using the etching mask pattern.

[0053] The etching mask pattern, which the photoresist with a thickness of 3 to 50[[□]]μm has been light-exposed and hard-baked at a temperature of 100 to 140°C and then developed in such a manner, can be used such that the side surfaces of the etched the P-type semiconductor layer 40, active layer 30 and predetermined N-type semiconductor layer 20 have a slope of 80 to 20° from a horizontal plane similarly to the etching mask pattern. Then, light produced within a light emitting layer is not totally reflected on the etched side surface with a variety of slopes but emitted to the outside of a light emitting device.

[0054] A transparent electrode layer may be further formed on the P-type semiconductor layer 40 to reduce resistance of the P-type semiconductor layer 40 and enhancing transmittance of light, and an additional ohmic metal layer may be further formed on the P-type semiconductor layer 40 or the exposed N-type semiconductor layer 20 to facilitate current supply. The transparent electrode layer may be made of ITO (Indium Tin Oxide), ZnO or a transparent conductive metal, and the ohmic metal layer may be made of Cr or Au. Further, for the application of voltage, a P-type electrode may be further formed on the P-type semiconductor layer 40 and an N-type electrode may be further formed on the N-type semiconductor layer 20.

[0055] Further, in order to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10.

[0056] As can be seen from this figure, a plurality of light emitting devices may be

fabricated on a single substrate 10, which is cut into the individual light emitting devices. At this time, portions A shown in Fig. 5 are cutting portions used for individually cutting the plurality of light emitting devices.

[0057] Accordingly, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 is not perpendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured.

[0058] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto. Various processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes.

[0059] Figs. 6 to 7 are sectional views illustrating a process of manufacturing a light emitting device according to a second embodiment of the present invention.

[0060] The second embodiment of the present invention is almost the same as the first embodiment. In the second embodiment, however, there is provided a light emitting device in which a plurality of light emitting cells are connected in series, parallel or series-parallel in a wafer level to reduce the size of the device, and they can be driven at proper voltage and current to be used for illustration purpose and can also be driven even with an AC power source. Descriptions overlapping with the previous embodiment will be omitted herein.

[0061] Referring to Fig. 6, an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40 are sequentially formed on a substrate 10 through various deposition methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like. A

buffer layer may be further formed on the substrate 10 to reduce lattice mismatch between the substrate 10 and the subsequent layers upon growth of crystals.

[0062] Thereafter, portions of the P-type semiconductor layer 40 and the active layer 30 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 20. That is, after the photoresist has been applied at a thickness of 3 to 50[[□]]μm on the P-type semiconductor layer 40 of Fig. 6 and light-exposed, it is developed without hard-baking to form an etching mask pattern. The P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer 20. A portion of the exposed N-type semiconductor layer 20 may be further removed. Thereafter, if the etching mask pattern is removed, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured as shown in Fig. 7.

[0063] Alternatively, after a photoresist has been applied in a thickness of 3 to 50[[□]]μm on the P-type semiconductor layer 40 of Fig. 6 and light-exposed, it is hard-baked at a temperature of 100 to 140°C and developed such that an etching mask pattern can be formed. After the P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, have been etched, the etching mask pattern is removed such that the side surfaces of the etched P-type semiconductor layer 40 and active layer 30 can have a variety of slopes of 80 to 20°.

[0064] Next, in order to form a plurality of light emitting cells on the substrate 10, predetermined regions of the exposed N-type semiconductor layer 20 are removed such that a portion of the substrate 10 can be exposed. To this end, a predetermined mask pattern is formed on all the portions except the predetermined regions where the substrate 10 will be

exposed, and regions of the N-type semiconductor layer 20 that are exposed through the mask pattern are then etched such that the plurality of light emitting cells can be electrically isolated from one another as shown in Fig. 8. At this time, the mask pattern whose side surface is inclined through the aforementioned process is formed and then used to etch the exposed N-type semiconductor layer 20 such that the side surface of the N-type semiconductor layer 20 in which the plurality of light emitting cells are separated from one another is not perpendicular to but inclined at a predetermined slope from a horizontal plane.

[0065] Referring to Fig. 9, the N-type semiconductor layer 20 of a light emitting cell and the P-type semiconductor layer 40 of the adjacent light emitting cell are connected through a predetermined wiring process. That is, the exposed N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent light emitting cell are connected through a wire 60. At this time, the conductive wire 60 for electrically connecting the N-type and P-type semiconductor layers 20 and 40 are formed through a bridge process.

[0066] The aforementioned bridge process is also called an air-bridge process. In the air-bridge process, a photosensitive liquid is applied between chips to be connected with each other through a photo process and developed to form a photoresist pattern, a material such as metal is first formed into a thin film on the photoresist pattern through a vacuum vapor deposition method or the like, and a conductive material containing gold (Au) is applied at a predetermined thickness onto the thin film through an electroplating, electroless plating or metal vapor deposition method. Thereafter, if the photoresist pattern is removed with a solution of a solvent or the like, a lower portion of the conductive material is completely removed, and thus, only the bridge-shaped conductive material is formed in a space between the adjacent light emitting cells.

[0067] The wire 60 may be made of not only metal but also all kinds of conductive

materials. It will be apparent that a silicone compound doped with impurities may be used.

[0068] Further, in order to apply an external voltage to the light emitting device, a P-type bonding pad 50 is formed on the P-type semiconductor layer 40 of the light emitting cell positioned at one edge of the substrate 10 and an N-type bonding pad 55 is formed on the exposed N-type semiconductor layer 20 of the light emitting cell positioned at the other edge of the substrate 10.

[0069] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment but is not limited thereto. Various modifications can be made or various material films can be further added. For example, in order to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10.

[0070] Accordingly, a light emitting device in which the plurality of light emitting cells each of which side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at predetermined slope from a horizontal plane are connected with one another can be manufactured.

[0071] Figs. 10 to 13 are sectional views illustrating a process of manufacturing a light emitting device according to a third embodiment of the present invention.

[0072] The third embodiment is almost the same as the second embodiment. In the second embodiment, the N-type semiconductor layer 20 is first exposed and a portion of the exposed N-type semiconductor layer 20 is then removed to separate the light emitting cells from one another. In the third embodiment, however, a plurality of light emitting cells are first separated, and a portion of an N-type semiconductor layer 20 is then exposed. Descriptions overlapping with the previous embodiments will be omitted herein.

[0073] Referring to Fig. 10, portions of an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40, which are sequentially formed on a substrate 10, are removed to form a plurality of light emitting cells. To this end, after a photoresist has been applied at a thickness of 3 to 50[[□]]μm on the P-type semiconductor layer 40 and light-exposed, it is immediately developed without hard-baking such that an etching mask pattern can be formed. The portions of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor pattern 20, which are exposed through the etching mask pattern, and the etching mask pattern is removed to separate the light emitting cells from one another. Accordingly, a light emitting device in which entire side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at a predetermined slope can be obtained as shown in this figure. Further, the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are removed using the etching mask pattern in which a photoresist is applied at a thickness of 3 to 50[[□]]μm on the P-type semiconductor layer 40 and light-exposed and hard-baked at a temperature of 100 to 140°C and then developed. Accordingly, the entire side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 can be formed at various slopes of 80 to 20°.

[0074] Thereafter, as shown in Fig. 11, portions of the P-type semiconductor layer 40 and the active layer 30 are removed to expose a portion of the N-type semiconductor layer 20 through a predetermined etching process.

[0075] Referring to Fig. 12, the N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent light emitting cell are connected with each other through a bridge process.

[0076] Further, in order to apply an external voltage to the light emitting device, a P-type bonding pad 50 is formed on the P-type semiconductor layer 40 of the light emitting

cell positioned at one edge of the substrate 10 and an N-type bonding pad 55 is formed on the exposed N-type semiconductor layer 20 of the light emitting cell positioned at the other edge of the substrate 10.

[0077] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment but is not limited thereto. Various modifications can be made and various material films may be further added. For example, in order to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10.

[0078] Further, even in a case where the plurality of light emitting cells are separated by etching such that the side surfaces may have various slopes as shown in Fig. 10 and then etched to expose the N-type semiconductor layer 20, a light emitting device can be manufactured using the same etching process as described above. That is, as shown in Fig. 11, the side surfaces of the P-type semiconductor layer 40 and the active layer 30, which are etched to expose the N-type semiconductor layer 20, can be formed at various slopes.

[0079] Accordingly, a light emitting device in which the plurality of light emitting cells each of which side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at predetermined slope from a horizontal plane are connected with one another can be manufactured.

[0080] Figs. 14 to 17 are sectional views illustrating a process of manufacturing a light emitting device according to a fourth embodiment of the present invention.

[0081] The fourth embodiment is almost the same as the third embodiment. In the third embodiment, a conductive wire for electrically connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light

emitting cell is formed through a bridge process. In the fourth embodiment, however, the conductive wire is formed through a step coverage process. Descriptions overlapping with the previous embodiments will be omitted herein.

[0082] Referring to Fig. 14, even in a case where a plurality of light emitting cells are separated by etching such that the side surfaces may have various slopes and then etched to expose an N-type semiconductor layer 20 through the aforementioned process, the side surfaces of P-type semiconductor layer 40 and active layer 30, which are etched to expose the N-type semiconductor layer 20, are formed with various slopes. Further, in order to reduce the resistance of the P-type semiconductor layer 40 and enhance the transmittance of light, a transparent electrode layer 85 may be further formed on a top surface of the P-type semiconductor layer 40. Further, an additional ohmic metal layer 87 for facilitating the supply of current may be further formed on a top surface of the P-type semiconductor layer 40 or the exposed N-type semiconductor layer 20. The transparent electrode layer 85 may be made of ITO (Indium Tin Oxide), ZnO or a conductive transparent metal, and the ohmic metal layer 87 may be made of Cr or Au.

[0083] Referring to Fig. 15, a continuous insulation layer 70 is formed on an entire surface of the substrate 10 with the plurality of light emitting cells formed thereon. The insulation layer 70 covers the side surfaces and top surfaces of the light emitting cells and the top surfaces of the substrate 10 between the adjacent light emitting cells. For example, the insulation layer 70 may be formed as a silicone oxide film using a CVD (Chemical Vapor Deposition) technique.

[0084] Since the side surfaces of the light emitting cells are inclined, the insulation layer 70 can easily cover the side surfaces of the light emitting cells. Since the total thickness of the N-type semiconductor layer 20 and active layer 30 is small and spaces between the adjacent P-type semiconductor layers 40 are broad, the side surfaces of the P-type

semiconductor layers 40 adjacent to the exposed regions of the N-type semiconductor layers 20 can be easily covered with the insulation layer 70.

[0085] Referring to Fig. 16, an opening portion is formed on each of the exposed N-type and P-type semiconductor layers 20 and 40 of the light emitting cell by patterning the insulation layer 70 through a predetermined etching process. If the transparent electrode layer 85 and/or the ohmic metal layer 87 are formed as shown in this figure, the transparent electrode layer 85 and/or the ohmic metal layer 87 are exposed through the opening portion.

[0086] Referring to Fig. 17, a wire 80 is formed on the insulation layer 70 with the opening portion. The wire 80 connects the N-type and P-type semiconductor layers 20 and 40 through the opening portion thereof. That is, the N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent the light emitting cell are electrically connected with the wire.

[0087] The wire 80 may be formed using a plating technique. That is, after an etching mask pattern with an opening portion defining a region of the wire 80 has been formed on the insulation layer 70 and a metal layer has been plated within the opening portion, the etching mask pattern is removed and thus the wire 80 can be formed.

[0088] Further, the wire 80 may be formed using the CVD (Chemical Vapor Deposition) or PVD (Physical Vapor Deposition) technique. That is, a metal layer is formed using a vapor deposition technique such as electron beam deposition and then patterned using a photo and etching process, so that the wire 80 can be formed. Since the side surface of the light emitting cell is inclined, the metal layer is continuously formed on the upper side surface of the light emitting cell.

[0089] The light emitting device in which the wire 80 is formed as described above has an advantage in that it is possible to prevent the wire 80 from being disconnected or shorted due to external pressure and also prevent conductive materials such as metal, which

remains while the wire 80 is formed, from shorting the light emitting cell.

[0090] Accordingly, a light emitting device in which the plurality of light emitting cells each of which side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at predetermined slope from a horizontal plane are connected with one another can be manufactured.

[0091] As described above, the light emitting device according to the present invention is formed such that the side surfaces of the P-type semiconductor layer, the active layer and a portion of the N-type semiconductor layer are not perpendicular (90°) to but inclined at a predetermined slope from a horizontal plane. Therefore, luminous efficiency of the light emitting device of the present invention can be enhanced as compared with that of the conventional light emitting device. The reason is that a photon reflected on a flat surface in the prior art is not reflected on a surface with a different angle but emitted to the outside.

[0092] Fig. 18 is a conceptual sectional view illustrating a light emitting device with a flip chip structure according to the present invention.

[0093] Referring to Fig. 18, the light emitting device comprises a light emitting layer, i.e. an N-type semiconductor layer 120, an active layer 130 and a P-type semiconductor layer 140 sequentially formed on a base substrate 110. Further, the light emitting device comprises a submount substrate 200 onto which the base substrate 110 with the light emitting layer formed thereon is flip-chip bonded through metal bumps 150 and 155. A side surface of the light emitting layer comprising the P-type semiconductor layer 140, the active layer 130 and the N-type semiconductor layer 120 is inclined at a slope of 20 to 80°from the horizontal plane and a critical angle of light is changed due to the side surface such that the light can be easily extracted. Therefore, luminous efficiency of the light emitting device can be improved.

[0094] Figs. 19 to 23 are sectional views illustrating a process of manufacturing a

light emitting device according to a fifth embodiment of the present invention.

[0095] Referring to Fig. 19, an N-type semiconductor layer 120, an active layer 130 and a P-type semiconductor layer 140 are sequentially formed on a base substrate 110.

[0096] The base substrate 110 refers to a general wafer used for fabricating a light emitting device is made of a transparent substrate such as Al_2O_3, ZnO and $LiAl_2O_3$. In this embodiment, a crystal growth substrate made of sapphire is used.

[0097] The N-type semiconductor layer 120, the active layer 130 and the P-type semiconductor layer 140 are sequentially formed on the substrate 110 through various deposition methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like. A buffer layer may be further formed on the substrate 110 to reduce lattice mismatch between the substrate 110 and the subsequent layers upon growth of crystals. The aforementioned components are the same as those in the previous embodiments, and thus, descriptions overlapping with the foregoing components will be omitted herein.

[0098] Thereafter, portions of the P-type semiconductor layer 140 and the active layer 130 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 120. This etching process is the same as that of the previous embodiments.

[0099] That is, after a photoresist has been applied at a thickness of 3 to 50[[□]]μm on the P-type semiconductor layer 140 of Fig. 19 and light-exposed, it is immediately developed without hard-baking to form an etching mask pattern. The P-type semiconductor 140 and the active layer 130, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer 120. Thereafter, if the etching mask pattern is removed, side

surfaces of the P-type semiconductor layer 140 and the active layer 130 which are not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane can be obtained as shown in Fig. 20.

[0100] Alternatively, after a photoresist has been applied at a thickness of 3 to 50[[□]]μm on the P-type semiconductor layer 140 of Fig. 19 and light-exposed, it is hard-baked at a temperature of 100 to 140°C and then developed such that an etching mask pattern can be formed. After the P-type semiconductor layer 140 and the active layer 130, which are exposed through the etching mask pattern, have been etched, the etching mask pattern is removed such that the side surfaces of the etched P-type semiconductor layer 140 and active layer 130 can have a variety of slopes of 80 to 20°.

[0101] A reflection layer for reflecting light may be further formed on a top surface of the P-type semiconductor layer 140, and an additional ohmic metal layer for facilitating the supply of current may be further formed on a top surface of the P-type semiconductor layer 140 or the exposed N-type semiconductor layer 120. The ohmic metal layer may be made of Cr or Au.

[0102] Further, P-type and N-type metal bumps 155 and 150 are formed on the P-type and N-type semiconductor layers 140 and 120, respectively, as shown in Fig. 21. Each of the P-type and N-type metal bumps 155 and 150 may be made of at least one material selected from the group consisting of Pb, Sn, Au, Ge, Cu, Bi, Cd, Zn, Ag, Ni, Ti and an alloy thereof. To this end, a photoresist is applied onto an entire structure and a photoresist pattern (not shown) through which portions of the P-type and N-type semiconductor layers 140 and 120 are exposed is formed through a photo-etching process using a predetermined mask. After a metal film has been deposited on the entire structure, metal film portions formed on regions other than regions on the P-type and N-type semiconductor layers 140 exposed through the photoresist pattern and the photoresist pattern are removed. Accordingly, the P-

type and N-type metal bumps 155 and 150 are formed on the P-type and N-type semiconductor layers 140 and 120, respectively.

[0103] Next, referring to Fig. 22, an additional submount substrate 200 is prepared to form P-type and N-type bonding pads 215 and 210 connected to the P-type and N-type metal bumps 155 and 150, respectively.

[0104] At this time, various kinds of superior heat conductive substrates 200 are used as the submount substrate 200. That is, the submount substrate 200 may be made of SiC, Si, Ge, SiGe, AlN, metal or the like. In this embodiment, AlN with superior heat conductivity and insulation property is used. The present invention is not limited thereto, but a metallic material with superior heat and electric conductivity may be employed. In this case, an insulation or dielectric film is formed on the substrate 200 to sufficiently serve as an insulation. The dielectric film may be made of SiO2, MgO and SiN or an insulating material. Further, each of the P-type and N-type bonding pads 210 and 215 is made of a metal with superior electric conductivity. This is formed through a screen printing process or a deposition process using a predetermined mask pattern.

[0105] Thereafter, the submount substrate 200 is flip-chip bonded onto the base substrate 110 with the light emitting layer formed thereon.

[0106] Referring to Fig. 23, in the light emitting device of the present invention, the N-type and P-type metal bumps 150 and 155 formed on the top of the light emitting layer are bonded and connected with the N-type and P-type bonding pads 210 and 215 of the submount substrate 200, respectively. At this time, the bonding pads and metal bumps may be bonded using heat or ultrasonic waves or simultaneously using the heat and ultrasonic waves. The metal bumps 150 and 155 and the lower bonding pads 210 and 215 are connected through a variety of bonding methods.

[0107] Moreover, the N-type and P-type metal bumps 150 and 155 are not formed

on the top of the light emitting layer but may be formed on the submount substrate 200.

[0108] As can be seen from this figure, a plurality of light emitting devices may be fabricated on a single substrate 10, which is cut into the individual light emitting devices. At this time, portions A shown in Fig. 23 are cutting portions used for individually cutting the plurality of light emitting devices.

[0109] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto. Various processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes. For example, in the same process as the previous embodiments, the base substrate with the N-type semiconductor layer, the active layer and the P-type semiconductor layer sequentially formed thereon is prepared as shown in Fig. 19. Then, portions of the P-type semiconductor layer, the active layer and the N-type semiconductor layer are first removed to expose the substrate such that the plurality of light emitting devices can be individually isolated. At this time, the side surfaces of the P-type semiconductor layer, the active layer and the N-type semiconductor layer, which are etched through the aforementioned process, may be formed not to be perpendicular (90°) to but inclined at a predetermined slope.

[0110] Accordingly, a light emitting device with a flip chip structure, in which the side surfaces of the P-type semiconductor layer, the active layer and a portion of the N-type semiconductor layer are not perpendicular (90°) to but inclined at the predetermined slope from the horizontal plane, can be manufactured.

[0111] Figs. 24 to 28 are sectional views illustrating a process of manufacturing a light emitting device according to a sixth embodiment of the present invention.

[0112] The sixth embodiment is almost the same as the fifth embodiment. In the sixth embodiment, however, there is provided a light emitting device with a flip chip

structure, in which a plurality of light emitting cells are connected in series, parallel or series-parallel in a wafer level to reduce the size of the device, and they can be driven at proper voltage and current to be used for illumination purpose and can also be driven even with an AC power source. Descriptions overlapping with the previous embodiments will be omitted herein.

[0113] Referring to Fig. 24, an N-type semiconductor layer 120, an active layer 130 and a P-type semiconductor layer 140 are sequentially formed on a base substrate 110 through various deposition methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hybride Vapor Phase Epitaxy) and the like. A buffer layer may be further formed on the substrate 110 to reduce lattice mismatch between the substrate 110 and the subsequent layers upon growth of crystals.

[0114] Thereafter, portions of the N-type semiconductor layer 120, the active layer 130 and the P-type semiconductor layer 140, which are sequentially formed on the base substrate 110, are removed to form a plurality of light emitting cells. To this end, after a photoresist has been applied at a thickness of 3 to 50[[□]]μm on the P-type semiconductor layer 140 of Fig. 24 and light-exposed, it is immediately developed without hard-baking to form an etching mask pattern. The P-type semiconductor 140, the active layer 130 and the predetermined N-type semiconductor layer 120, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to separate the light emitting cells from one another. Next, if the etching mask pattern is removed, a light emitting device in which entire side surfaces of the etched P-type semiconductor layer 140, active layer 130 and N-type semiconductor layer 120 are not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane can be obtained as shown in Fig. 25.

[0115] Alternatively, after a photoresist has been applied at a thickness of 3 to 50[[□]]μm on the P-type semiconductor layer 140 of Fig. 24 and light-exposed, it is hard-baked at a temperature of 100 to 140°C and developed such that an etching mask pattern can be formed. After the P-type semiconductor layer 140, the active layer 130 and the N-type semiconductor layer 120, which are exposed through the etching mask pattern, have been etched, the etching mask pattern is removed such that the side surfaces of the etched P-type semiconductor layer 140 and active layer 130 can be inclined at various slopes of 80 to 20°.

[0116] Next, portions of the P-type semiconductor layer 140 and the active layer 130 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 120, as shown in Fig. 26. The exposed N-type semiconductor layer 120 of one light emitting cell and the P-type semiconductor layer 140 of another adjacent light emitting cell are connected with each other through a predetermined conductive wire. At this time, a bridge wire 160 is made of a conductive material, e.g. metal. It will be apparent that the bridge wire 160 may be made of a silicone compound doped with impurities. The bridge wire 160 is formed through a bridge process.

[0117] Further, a plurality of metal bumps are formed on the top of the light emitting cells, and P-type and N-type metal bumps 155 and 150 are further formed on the P-type semiconductor layer 140 of the light emitting cell positioned at one edge of the substrate 110 and the N-type semiconductor layer 120 of the light emitting cell positioned the other edge of the substrate, respectively.

[0118] Next, as shown in Fig. 27, an additional submount substrate 200 is prepared, on which a plurality of bonding layers 220, a P-type bonding pad 215 positioned at one edge of the submount substrate 200 and an N-type bonding pad 210 positioned at the other edge of the submount substrate are formed.

[0119] Thereafter, as can be shown in Fig. 28, the aforementioned base substrate

110 with the plurality of light emitting cells formed thereon is flip-chip bonded onto the submount substrate 200 to fabricate the light emitting device. The substrates are bonded with each other through the metal bumps 150 and 155 formed on the top of the light emitting cell and the bonding layers 220 formed on the submount substrate 200, respectively. The P-type bonding pad 215 positioned at one edge of the submount substrate 200 is connected to the P-type metal bump 155 of the light emitting cell positioned at one edge of the base substrate 110, whereas the N-type bonding pad 210 positioned at the other edge of the submount substrate 200 is connected to the N-type metal bump 150 of the light emitting cell positioned at the other edge of the base substrate 110.

[0120] The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto. Various processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes. For example, in this embodiment, the conductive wire for electrically connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell is formed through a bridge process, and the base substrate is then flip-chip bonded onto the submount substrate. However, the present invention is not limited thereto. That is, a conductive wire for electrically connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cells may be formed through a step coverage process which is the same as in the fourth embodiment. Further, an electrode layer may be formed on the submount substrate when the plurality of light emitting cells are flip-chip bonded onto the submount substrate such that the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are electrically connected through the metal bumps.

[0121] Accordingly, a light emitting device in which a plurality of flip chip light

emitting cells each having a side surface of a light emitting layer, which is not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane, are arrayed on the submount substrate can be manufactured. The light emitting cells may be connected in various ways, i.e. in series, parallel or series-parallel, depending on the desired purpose.

[0122] Fig. 29 is a sectional view showing a seventh embodiment according to the present invention.

[0123] The seventh embodiment is almost the same as the sixth embodiment. In this embodiment, even in a case where a plurality of light emitting cells are separated by etching such that the side surfaces may have slopes as shown in Fig. 25 and then etched to expose an N-type semiconductor layer, a light emitting device can be manufactured using the same etching process as the previous embodiment. That is, side surfaces of a P-type semiconductor layer 140 and an active layer 130 etched to expose an N-type semiconductor layer 120 are formed with various slopes, as shown in Fig. 29.

[0124] Accordingly, a light emitting device in which a plurality of flip chip light emitting cells each having an entire side surface of a light emitting layer, which is not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane, are arrayed on the submount substrate can be manufactured. The light emitting cells may be connected in various ways, i.e. in series, parallel or series-parallel, depending on the desired purpose.

[0125] As described above, the light emitting device with a flip chip structure according to the present invention is formed such that some side surfaces of a light emitting layer are not particular (90°) to but inclined at a predetermined slope from the horizontal plane. Therefore, luminous efficiency of the light emitting device of the present invention can be enhanced as compared with that of the conventional light emitting device. The reason is that a photon reflected on a flat surface in the prior art is not reflected on a surface with a

different angle but emitted to the outside.

[0126] Figs. 30 and 31 are conceptual sectional views illustrating a difference between effects of the light emitting devices according to the prior art and the present invention.

[0127] The light efficiency of a light emitting device may be expressed as internal quantum efficiency and external quantum efficiency, and the internal quantum efficiency is determined in accordance with the design and quality of an active layer. The external quantum efficiency is determined in accordance with a degree where a photon produced in an active layer is emitted to the outside of a light emitting device. Referring to Fig. 30 in which a conventional light emitting device is shown, a side surface of a semiconductor layer is formed perpendicular to a horizontal plane. In such a case, some portions of photons are not penetrated through the side surface of the semiconductor layer but reflected thereon, and totally reflected light is not emitted to the outside but dissipated within the light emitting device. However, referring to Fig. 31 in which a light emitting device according to the present invention is shown, a side surface of a semiconductor layer is not perpendicular to but inclined at a predetermined slope from a horizontal plane. In such a case, the inclined side surface makes a critical angle of light change to help the light to be more easily extracted. Therefore, light generated in an active layer is not totally reflected but emitted to the outside of the light emitting device such that external quantum efficiency can be markedly enhanced.

[0128] Fig. 32 is a sectional view illustrating a light emitting diode for AC operation according to the eighth embodiment of the present invention.

[0129] Referring to Fig. 32, a plurality of light emitting cells 56 are disposed to be spaced apart in a substrate 51. The substrate 51 may be insulating or conducting one, and may be, for example, a sapphire or a silicon carbide (SiC) substrate.

[0130] The light emitting cells 56 respectively include a lower semiconductor layer

55, an upper semiconductor layer 59 disposed in a region of the lower semiconductor layer, and an active layer 57 disposed between the lower semiconductor layer and the upper semiconductor layer. The upper and the lower semiconductor layers may be N-type and P-type, respectively. Alternatively the upper and the lower semiconductor layers may be P-type and N-type, respectively.

[0131] The lower semiconductor layer 55, active layer 57 and upper semiconductor layer 59 may include a gallium nitride-based semiconducting material, for example, (B, Al, In, Ga)N. Elements and stoichiometry of the active layer 57 may be determined so that a light having a desired wavelength, for example, ultraviolet ray or blue light, can be emitted. The lower semiconductor layer 55 and upper semiconductor layer 59 are formed of a material having a greater bandgap compared with the active layer 57.

[0132] The lower semiconductor layer 55 and/or the upper semiconductor layer 59 may be, as illustrated, formed of a single layer or multiple layers. The active layer 57 may have a single-quantum-well structure or a multiple-quantum-well structure.

[0133] A buffer layer 53 may be disposed between the light emitting cells 56 and the substrate 51. The buffer layer 53 is employed to reduce a lattice mismatch between the substrate 51 and the lower semiconductor layer 55 formed thereon. The buffer layer 53 may be continuous as illustrated, but it is not limited thereto. The buffer layer 53 may be disposed under the lower semiconductor layers 55 to be discontinuous.

[0134] Side surfaces of the light emitting cells 56 are formed to be inclined with respect to an upper surface of the substrate 51 and get narrowed toward upside. The inclination of the side surfaces improves emission efficiency of a light produced in the active layer 57, and helps conformal deposition of other layers which will be formed on the light emitting cells 56. In the exemplary embodiment, the inclinations of the side surfaces of the respective lower semiconductor layers 55 of the light emitting cells 56 may be in a range of

approximately 15 degrees to approximately 80 degrees.

[0135] An insulation layer 69 covers an entire surface of the light emitting cells 56. The insulation layer 69 include opening portions on other regions of the lower semiconductor layers 55, for example, a region adjacent to a region on which the upper semiconductor layer 59 is formed, and include opening portions on the upper semiconductor layers 59. The opening portions are space apart from each other, and therefore, the side surfaces of the light emitting cells 56 are covered with the insulation layer 69. The insulation layer 69 may cover the substrate 51 in regions between the light emitting cells 56, or the buffer layer 53. The insulation layer 69 may include a silicon oxide (SiO2) layer.

[0136] Wires 71 are formed on the insulation layer 69. The wires 71 are electrically connected to the lower semiconductor layers 55 and the upper semiconductor layers 59 through the opening portions. In addition, the wires 71 respectively connect the lower semiconductor layers 55 and the upper semiconductor layers 59 of the adjacent light emitting cells 56 to form a series array of the light emitting cells 56. The array may be formed in plurality, and a plurality of arrays may be connected to be reverse parallel and connected to AC power to be driven. Further, a bridge rectifier (not shown) connected to the series array of the light emitting cells may be formed, and the light emitting cells may be driven with AC power by the bridge rectifier. The bridge rectifier may be formed by connecting light emitting cells having substantially the same structure as the light emitting cells using wires 71. The wires may be formed of a conductive material, for example, a doped semiconducting material such as polycrystalline silicon or a metal.

[0137] Meanwhile, electrode pads may be disposed between other regions of the lower semiconductors 55 and the insulation layer 69. The electrode pads 67 are exposed by the opening portions formed in other regions of the lower semiconductor layers 55. The electrode pads 67 have ohmic contacts to the lower semiconductor layers 55. The wires 71

are in contact with the electrode pads 67 exposed by the opening portions to be electrically connected to the lower semiconductor layers 55.

[0138] Transparent electrode layers 65 may be disposed between the upper semiconductor layers 59 and the insulation layers 69. The transparent electrode layers 65 are exposed by the opening portions formed on the upper semiconductor layers 59. The transparent electrode layers 65 transmit light produced in the active layer 57, and disperse and supply currents to the upper semiconductor layers 59. The wires 71 are in contact with the transparent electrode layers 65 exposed by the opening portions to be electrically connected to the upper semiconductor layers 55. Electrode pads (not shown) may be further formed on the transparent electrode layers 65 and the wires 71 may be in contact with the electrode pads.

[0139] A protecting insulation layer 73 may cover the wires 71 and the insulation layer 69. The protecting insulation layer 73 substantially reduces contamination of the wires 71 from moisture and so forth, and damage of the wires 71 from external pressure. The protecting insulation layer 73 may be formed of a light-transmitting material, for example, silicon oxide layer.

[0140] Figs. 33 to 38 are sectional views illustrating a process of manufacturing a light emitting diode according to the eighth embodiment of the present invention.

[0141] Referring to Fig. 33, a lower semiconductor layer 55, an active layer 57, and an upper semiconductor layer 59 are formed on a substrate 51. A buffer layer 53 may be formed on the substrate 51 before the lower semiconductor layer 55 is formed.

[0142] The substrate 51 may be sapphire (Al2O3), silicon carbide (SiC), zinc oxide (ZnO), silicon (Si), gallium arsenide (GaAs), gallium phosphate (GaP), lithium-alumina (LiAl2O3), boron nitride (BN), aluminum nitride (AlN) or gallium nitride (GaN). However, it is not limited thereto and may be variable according to a semiconducting material which is

to be formed on the substrate 51.

[0143] The buffer layer 53 is formed to reduce lattice mismatch between the substrate 51 and the semiconductor layer 55 which is to be formed thereon. The buffer layer 53 may include, for example, gallium nitride (GaN) or aluminum nitride (AlN). When the substrate 51 is a conductive substrate, the buffer layer 53 may be formed of an insulation layer or a semi-insulation layer, for example, AlN or semi-insulating GaN.

[0144] The lower semiconductor layer 55, active layer 57 and upper semiconductor layer 59 may include a gallium nitride-based semiconducting material, for example, (B, Al, In, Ga)N. The lower and upper semiconductor layers 55 and 59 and the active layer 57 may be formed continuously or discontinuously using, for example, metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy or hydride vapor phase epitaxy (HNPE) technology.

[0145] The upper and the lower semiconductor layers may be N-type and P-type, respectively. Alternatively the upper and the lower semiconductor layers may be P-type and N-type, respectively. In the gallium nitride-based compound semiconductor layer, N-type semiconductor layer may be doped with, for example, silicon (Si), and P-type semiconductor layer may be doped with, for example, magnesium (Mg).

[0146] Photoresist patterns 63 defining light emitting cell regions are formed on the upper semiconductor layer 59. The photoresist patterns are formed to cover the light emitting cell regions. Reflow of the photoresist patterns 63 is performed so that side surfaces can be inclined with respect to an upper surface of the substrate 51. The side surfaces of the photoresist patterns 63 may be formed to have an inclination angle in a range of approximately 15 degree to 80 degree with respect to the upper surface of the substrate 51.

[0147] Referring to Fig. 34, the upper semiconductor layer 59, the active layer 57 and the lower semiconductor layer 55 are sequentially etched using the photoresist patterns

63 as etching mask. Accordingly, the shape of the photoresist patterns 63 is reproduced in the semiconductor layers 59, 57 and 55 and the light emitting cells with inclined side surfaces are separated. The buffer layer 53 may be exposed and the exposed buffer layer 53 may be removed by over-etching.

[0148] Thereafter, the photoresist patterns 63 are removed, and the upper semiconductor layer and the active layer are patterned again to expose the etched lower semiconductor layers 55. The exposed lower semiconductor layers may be partially etched by over-etching. Accordingly, light emitting cells 56 that are spaced apart are formed on the substrate 51. Each of the light emitting cells 56 includes the lower semiconductor layer 56 which is spaced apart by etching, the upper semiconductor layer 57 disposed on an upper side of a region of the lower semiconductor layer 56, and the active layer 57 disposed between the lower semiconductor layer 55 and the upper semiconductor layer 57. Other region of the lower semiconductor layer 56 is exposed. Further, most of the side surfaces of the light emitting cells 56 are formed to be inclined with respect to an upper surface of the substrate 51. Whereas, side surfaces of the upper semiconductor layers 59 adjacent to other regions of the lower semiconductor layers 55 may be formed to be inclined as illustrated, and alternatively, may be formed vertically.

[0149] Referring to Fig. 35, a transparent electrode layer 65 may be formed on the upper semiconductor layer 59 of the light emitting cell 56. The transparent electrode layer 65 includes a transparent metal such as indium tin oxide (ITO) layer or Ni/Au. Further, electrode pads 67 may be formed on other regions of the lower semiconductor layers 55. The electrode pads 67 have an ohmic contact with the lower semiconductor layers 55.

[0150] The transparent electrode layer 65 may be formed on the upper semiconductor layer 59 before the photoresist patterns are formed. The transparent electrode layer 65 is patterned together with the upper semiconductor layer

[0151] Referring to Fig. 36, a continuous insulation layer 69 is formed on an entire surface of the substrate 51 with the plurality of light emitting cells 56 formed thereon. The insulation layer 69 covers the side surfaces and top surfaces of the light emitting cells 56, and the top surfaces of the substrate 51 between the adjacent light emitting cells 56. For example, the insulation layer 69 may be formed as a silicone oxide film using a CVD (Chemical Vapor Deposition) technique.

[0152] Since the side surfaces of the light emitting cells 56 are inclined, the insulation layer 69 can easily cover the side surfaces of the light emitting cells 56. Since the total thickness of the upper semiconductor layer 59 and active layer 57 is small and spaces between the upper semiconductor layers 59 are broad, the side surfaces of the upper semiconductor layers 59 adjacent to other regions of the lower semiconductor layers 55 can be easily covered with the insulation layer 69.

[0153] Referring to Fig. 37, an opening portions are formed on other regions of the lower semiconductor layers 55 and the upper semiconductor layers 59 by patterning the insulation layer 69. If the electrode pads 67 and the transparent electrode layers 65 are formed, the electrode pads 67 and the transparent electrode layers 65 are exposed through the opening portions.

[0154] The opening portions may be formed using a photo and etching process, and the electrode pads 67 substantially reduce damage of the lower semiconductor layers 55 while the insulation layer 69 is etched.

[0155] Referring to Fig. 38, wires 71 are formed on the insulation layer 69 with the opening portions. The wire 71 are electrically connected to the lower semiconductor layers 55 and the upper semiconductor layers 59 through the opening portions, and connect the lower semiconductor layers 55 and the upper semiconductor layers 59 of the adjacent light emitting cells 56 to form arrays connected in series.

[0156] The wires 71 may be formed using a plating technique. That is, the wires 71 may be formed by forming a photoresist pattern having opening portions defining wire region on the insulation layer 69, plating a metal layer in the opening portions, and removing the photoresist pattern.

[0157] Alternatively, the wires 71 may be formed using CVD (Chemical Vapor Deposition) or PVD (Physical Vapor Deposition) technique. That is, a metal layer is formed using a vapor deposition technique such as electron beam deposition and then patterned using a photo and etching process, so that the wires 71 can be formed. Since the insulation layer 69 covers the side surfaces of the light emitting cells 56, short-circuiting of the light emitting cells 56 due to a remaining metallic material after patterning of metal layer may be prevented.

[0158] A protecting insulation layer 73 is formed on the substrate 51 with the wires 71 formed thereon. The protecting insulation layer 73 is formed of a light-transmitting material, for example, silicon oxide layer using chemical vapor deposition technique. In this way, a light emitting diode for AC operation.

[0159] According to the eighth embodiment, a reliable light emitting diode for AC operation can be provided by preventing disconnection or short circuit of wires by external pressure, and short circuit of a light emitting cell by a conductive material such as metal residue while the wires are formed may be prevented. Further, the wires may be formed to be supported by insulation layers, so that a reliable light emitting diode for AC operation can be manufactured.

[0160] Although the present invention has been described in detail in connection with the specific embodiments, it will be readily understood by those skilled in the art that various modifications and changes can be made thereto within the technical spirit and scope of the present invention. It is also apparent that the modifications and changes fall within the scope of the present invention defined by the appended claims.

Electronic Acknowledgement Receipt

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International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
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Time Stamp:	22:33:27
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Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	New or Additional Drawings	New_Drawing_Sheets.pdf	124070 135a64d15eb6e40cc47ff615822e17ff84223ce6	no	3

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2	Translation of Foreign Priority Documents	KR200553797_Verified_Translation_of_Priority_Document.pdf	923481 c3565548992d5dd16df2484a6e719c5c6613f02e	no	19
Warnings:					
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3	Translation of Foreign Priority Documents	KR200555179_Verified_Translation_of_Priority_Document.pdf	963219 45f6bece9c370c9a9f79bae199c88fb6666de55d	no	18
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4	Translation of Foreign Priority Documents	KR200621801_Verified_Translation_of_Priority_Document.pdf	788143 4868ea078a7534c9f7ee513bc3694f15511bc67a	no	14
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5		PrelimAmend.pdf	45131 5db941879e3c4c2b13b5f684beafcc93430e1b95	yes	8

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Preliminary Amendment	1	1
Specification	2	2
Claims	3	6
Applicant Arguments/Remarks Made in an Amendment	7	8

Warnings:					
Information:					
6	Specification	SSC.pdf	202202 d31e78d1fd259fd99f01f1676c7bb0113bc70657	no	38
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Information:					
7	Specification	SSM.pdf	205953 b5f0ce337f0019f3fe7e61f2a010cdc07a5419c3	no	38
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FIG. 32

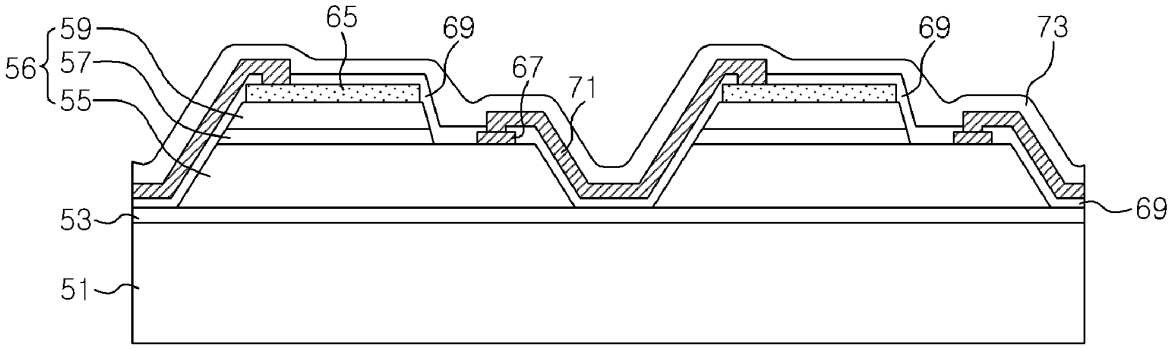


FIG. 33

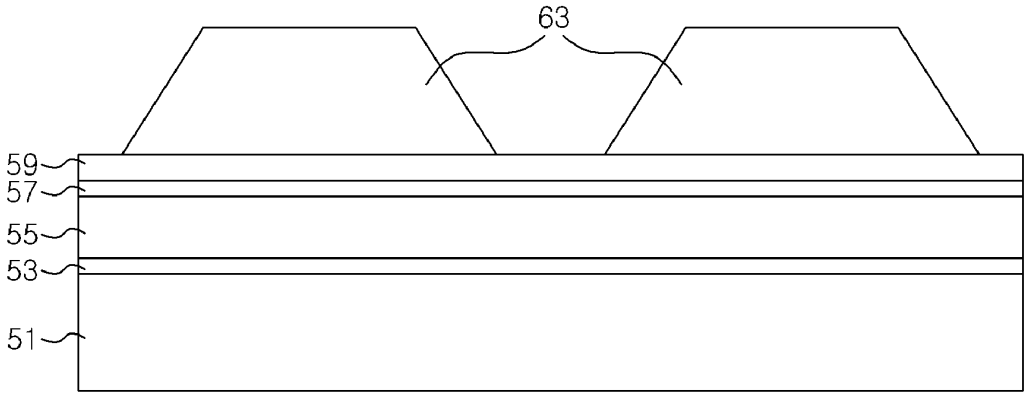


FIG. 34

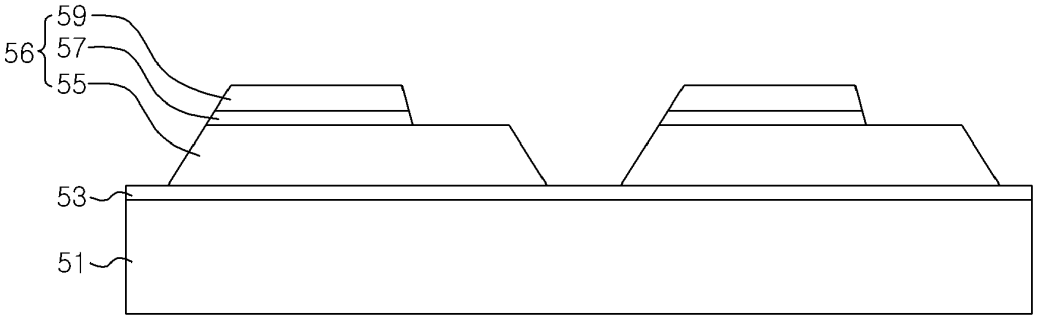


FIG. 35

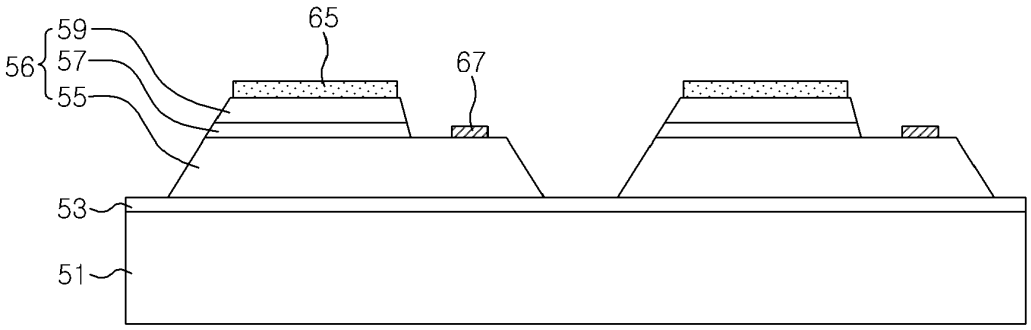


FIG. 36

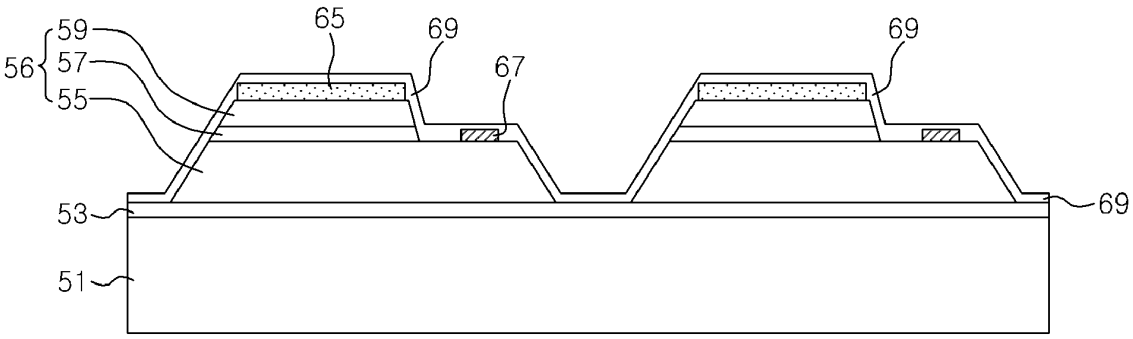


FIG. 37

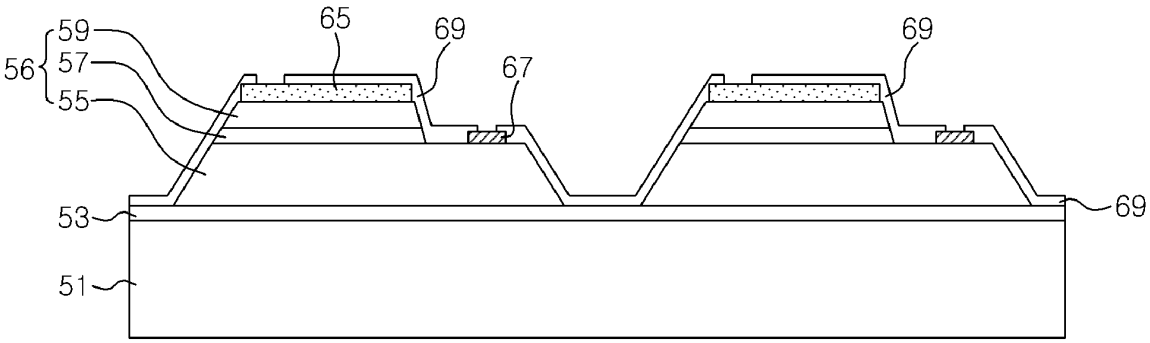
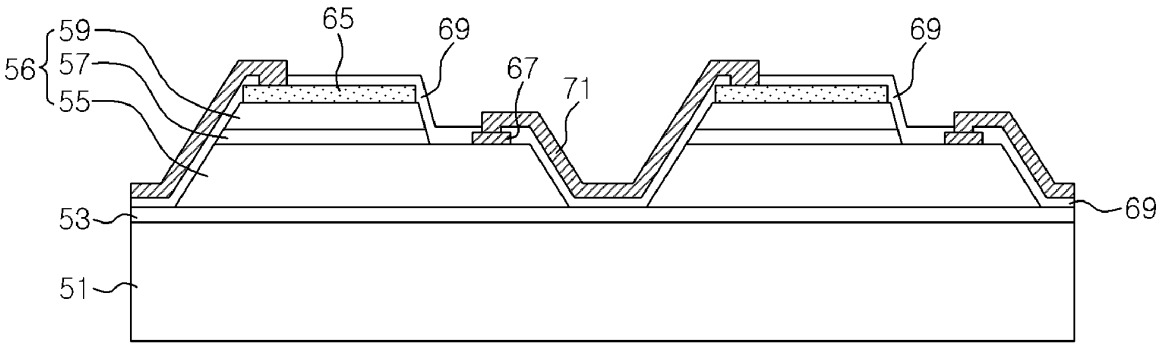


FIG. 38



VERIFICATION OF THE TRANSLATION

I, Seung-Hee NAM of Ein Patent Law Firm, 12F, Seojeon Bldg., 1330-9, Seocho-Dong, Seocho-Gu, Seoul, 137-858, Republic of Korea being fully conversant with both the English and the Korean language, declare the attached to be a true and accurate translation of the Korean Patent Application Nos. 10-2005-53797 filed on June 22, 2005, 10-2005-55179 filed on June 24, 2005, and 10-2006-21801 filed on March 8, 2006.

Signed by

Seung-Hee NAM

Dated this 1st day of September, 2009.

LIGHT-EMITTING DEVICE AND METHOD OF MANURACTURING THE SAME

BACKGROUND OF THE INVENTION

[Field of Invention]

<14> The present disclosure relates to a light emitting device and a method of manufacturing the same. More particularly, the present disclosure relates to a nitride based semiconductor light emitting device with enhanced luminous efficiency and brightness and a method of manufacturing the light emitting device.

[Description of the Related Art]

<15> A light emitting device refers to an element in which minority carriers (electrons or holes) injected using a p-n junction structure of a semiconductor are produced and certain light is emitted due to recombination of the carriers. A light emitting source is formed from any one or combination of compound semiconductor materials such as GaAs, AlGaAs, GaN, InGaN and AlGaInP, so that a variety of colors can be implemented. For example, a red light emitting device may be formed from GaAsP or the like; a green light emitting device may be formed from GaP, InGaN or the like; a blue light emitting device may be formed using an InGaN/GaN double hetero structure; and a UV light emitting device may be formed using an AlGaN/GaN or AlGaN/AlGaN structure. In particular, GaN has a direct bandgap of 3.4eV at a normal temperature and a direct energy bandgap of 1.9eV (InN) to 3.4eV (GaN) or 6.2eV (AlN) by combining with a substance such as InN or AlN. Thus, GaN is a substance with great applicability to an optical element due to its broad wavelength range from visible light to ultraviolet light. Since the wavelength can be adjusted in such a manner, full-color implementation can be made by means of red, green and blue light emitting devices with a short wavelength range, so that the applicability to a general illumination market as well as a display device market is expected to be greatly increased.

<16> Light emitting devices have characteristics of lower power consumption, longer lifespan, better installation in a narrow space and stronger resistance against vibration as compared with existing bulbs or fluorescent lamps. Since the light emitting devices are used as display devices and backlights and have superior characteristics in view of the reduction in power consumption and the durability, many studies for applying the light emitting devices to a general illumination field have been recently conducted. In the future, their applicability is expected to extend to a backlight of a large-sized LCD-TV, a vehicle headlight and general illumination. To this end, it is necessary to improve luminous efficiency of light emitting devices, solve a heat dissipation problem, and achieve high brightness and output of the light emitting devices.

<17> Many techniques for enhancing the performance of light emitting devices have been currently developed. There are various indexes indicating the performance of light emitting devices, such as luminous efficiency (lm/W), internal quantum efficiency (%), external quantum efficiency (%) and extraction efficiency (%). The extraction efficiency is determined as a ratio of electrons injected into the light emitting device to photons emitted to the outside of the light emitting device. That is, the light emitting device becomes bright as the extraction efficiency becomes

high. Since the extraction efficiency of the light emitting device is much influenced by the shape and surface pattern of a chip, the structure of a chip and a packaging type, careful attention should be paid when designing the light emitting device.

<18> Fig. 1 is a sectional view showing a light emitting device in a related art.

<19> Referring to the figure, the light emitting device comprises a substrate 1, an N-type semiconductor layer 2 formed on the substrate 1, an active layer 3 formed on a portion of the N-type semiconductor layer 2 and a P-type semiconductor layer 4. That is, after the N-type semiconductor layer 2, the active layer 3 and the P-type semiconductor layer 4 have been sequentially formed on the substrate 1, predetermined regions of the P-type semiconductor layer 4 and the active layer 3 are etched to expose a portion of the N-type semiconductor layer 2. Then, a predetermined voltage is applied to top surfaces of the exposed N-type semiconductor layer 2 and the P-type semiconductor layer 4.

<20> Light produced from a light emitting layer of a light emitting device is emitted from 6 surfaces of a chip, and light extraction efficiency is generally determined by a critical angle of light. However, when the conventional light emitting device is etched to expose an N-type semiconductor layer, side surfaces of the P-type semiconductor layer and the active layer are vertically processed such that a portion of light produced within the light emitting device is totally reflected on the etched surface that is processed vertically from a horizontal plane. Then, a considerable amount of light to be totally reflected is not emitted to the outside but dissipated within the light emitting device due to the internal reflection. That is, there is a problem in that luminous efficiency in which electric energy is converted into light energy and the light is then emitted to the outside of a light emitting device is low.

SUMMARY OF THE INVENTION

<21> The present disclosure is conceived to solve the aforementioned problems. Accordingly, an object of the present invention is to provide a light emitting device for emitting light with high luminous intensity and brightness by enhancing characteristics of luminous efficiency, external quantum efficiency, extraction efficiency and the like and improving reliability, and a method of manufacturing the light emitting device.

<22> According to an aspect of the present disclosure for achieving the objects, there is provided a light emitting device including: a substrate; an N-type semiconductor layer formed on the substrate; and a P-type semiconductor layer formed on the N-type semiconductor layer, wherein a side surface including the N-type semiconductor layer or the P-type semiconductor layer is inclined to have a slope in a range of 20 degrees to 80 degrees.

<23> There is also provided a light emitting device, comprising a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on a portion of the N-type semiconductor layer on a substrate. The N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell may be connected to each other, and a side surface including the N-type or P-type semiconductor layer of the light emitting cell has a slope of 20 to 80°from a horizontal plane. The light emitting device may further comprise a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light

emitting cell

<24> The light emitting device may further include a transparent electrode layer on the P-type semiconductor layer, and P-type and N-type ohmic metal layers containing Cr or Au on the P-type and N-type semiconductor layers, respectively.

<25> According to another aspect of the present invention, there is provided a method of manufacturing a light emitting device, comprising the steps of sequentially forming N-type and P-type semiconductor layers on a substrate; forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; and removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern.

<26> A photoresist with a thickness of 3 to 50㎛ may be used in the step of forming the etching mask pattern.

<27> The step of forming the etching mask pattern may comprise the steps of: applying the photoresist onto the P-type semiconductor layer; light exposing the photoresist in accordance with a predetermined mask pattern; and developing the light-exposed photoresist without a baking process after the light exposure.

<28> The step of forming the etching mask pattern may comprise the steps of: applying the photoresist onto the P-type semiconductor layer; light exposing the photoresist in accordance with a predetermined mask pattern; hard baking the light-exposed photoresist at a temperature of 100 to 140℃; and developing the hard-baked photoresist.

<29> The method of manufacturing a light emitting device may further comprise the steps of removing a portion of the N-type semiconductor layer exposed through the removal of the P-type semiconductor layer to form a plurality of light emitting cell, and connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a bridge wire. The bridge wire may connect the N type semiconductor layer of one light emitting cell and the P type semiconductor layer of another adjacent light emitting cell through a bridge or step coverage process

<30> After the step of removing the P-type semiconductor layer and the etching mask pattern, the method of manufacturing a light emitting device may further comprise the steps of removing a rear surface of the substrate at a certain thickness; and depositing Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof onto the rear surface of the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will become apparent from the following description of preferred embodiments given in conjunction with the accompanying drawings, in which:

<1> Fig. 1 is a plan view illustrating a light emitting device in a related art;

<2> Fig. 2 is a conceptual sectional view illustrating a light emitting device according to the present disclosure;

<3> Figs. 3a and 3b are sectional views illustrating a process of manufacturing a light emitting device according to a first exemplary embodiment of the present disclosure;

<4> Figs. 4a to 4d are sectional views illustrating a process of manufacturing a light emitting device according to a second exemplary embodiment of the present

disclosure;

<5> Figs. 5a to 5d are sectional views illustrating a process of manufacturing a light emitting device according to a third exemplary embodiment of the present disclosure; and

<6> Figs. 6a and 6b are conceptual sectional views illustrating a difference between effects of the light emitting devices according to the related art and the present disclosure.

<7> <Reference numerals selected>

<8>	1:	substrate	2:	N-type semiconductor layer
<9>	3:	active layer	4:	P-type semiconductor layer
<10>	10:	substrate	20:	N-type semiconductor layer
<11>	30:	active layer	40:	P-type semiconductor layer
<12>	50:	P-type bonding pad	55:	N-type bonding pad
<13>	60:	wire		

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

<31> Hereinafter, a light emitting device and a manufacturing method thereof according to the present disclosure will be described in detail with reference to the accompanying drawings. However, the present invention is not limited to the embodiments set forth herein but can be implemented in different forms. Rather, the exemplary embodiments are merely provided to allow the present invention to be completely described herein and to fully convey the scope of the invention to those skilled in the art.

<32> Fig. 2 is a conceptual sectional view illustrating a light emitting device with a horizontal structure according to the present invention.

<33> Referring to the figure, the light emitting device comprises a substrate 10, and an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40, which are sequentially formed on the substrate 10. Each of side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 has a slope of 80 to 20° from a horizontal plane such that a critical angle of light can be changed by such surfaces and light can be easily extracted. Therefore, luminous efficiency of a light emitting device can be improved.

<34> Figs. 3a and 3b are sectional views illustrating a process of manufacturing a light emitting device according to a first embodiment of the present invention.

<35> Referring to Fig. 3a, an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40 are sequentially formed on a substrate 10.

<36> The substrate 10 refers to a general wafer used for fabricating a light emitting device and is made of at least any one of Al_2O_3, SiC, ZnO, Si, GaAs, GaP, $LiAl_2O_3$, BN, AlN and GaN. In this embodiment, a crystal growth substrate made of sapphire is used.

<37> A buffer layer (not shown) may be further formed on the substrate 10 to reduce lattice mismatch between the substrate 10 and the subsequent layers upon growth of crystals. The buffer layer may contain GaN or AlN that is a semiconductor material.

<38> The N-type semiconductor layer 20 is a layer in which electrons are produced and is preferably made from GaN doped with N-type impurities.

However, the N-type semiconductor layer 20 is not limited thereto but may use a material layer having a variety of semiconductor properties. The N-type semiconductor layer 20 including N-type $Al_xGa_{1-x}N(0\leq x\leq 1)$ is formed in this embodiment. Further, the P-type semiconductor layer 40 is a layer in which holes are produced and is preferably made from GaN doped with P-type impurities. However, the P-type semiconductor layer 40 is not limited thereto but may use a material layer with a variety of semiconductor properties. The P-type semiconductor layer 40 including P-type $Al_xGa_{1-x}N(0\leq x\leq 1)$ is formed in this embodiment. Moreover, InGaN may be used as the semiconductor layer. Further, each of the N-type and P-type semiconductor layers 20 and 40 may be formed as a multiple layer.

<39> The active layer 30 has a predetermined bandgap and is a region where a quantum well is formed so that electrons and holes are recombined. The active layer 30 may contain InGaN. The wavelength of light emitted through the combination of electrons and holes varies according to the kind of a material constituting the active layer 30. Therefore, it is preferred that a semiconductor material contained in the active layer 30 be controlled depending on a target wavelength.

<40> The aforementioned material layers are formed through a variety of deposition and growth methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hydride Vapor Phase Epitaxy) and the like.

<41> Thereafter, portions of the P-type semiconductor layer 40 and the active layer 30 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 20. An etching mask pattern is formed on the P-type semiconductor layer 40, and the P-type semiconductor layer 40 and the active layer 30 are then removed through a dry or wet etching process to expose the N-type semiconductor layer 20.

<42> Generally, in order to perform the etching process, a photoresist has been applied onto a top surface of the P-type semiconductor layer 40 at a thickness of 1 to 2㎛, and then soft-baked at a temperature of 80 to 90℃ is performed. Next, an exposure process in which light in a UV range is irradiated through a predetermined photo mask to transfer a pattern formed on the mask to the applied photoresist is executed. Thereafter, the photoresist is hard-baked at a temperature of 100 to 120℃, and a developing process in which the photoresist at a portion with relatively weak combination through the exposure process is melted using a solvent is executed. A predetermined etching mask pattern is formed on the P-type semiconductor layer 40 through the above process.

<43> However, in this embodiment, the photoresist is applied at a thickness of 3 to 50㎛ which is thicker as compared with the prior art when the etching mask pattern is formed, and the exposure process is performed after the soft-baking. Next, if the photoresist is directly developed without the hard-baking, a developed side surface of the remaining photoresist is formed into an inclined surface not perpendicular (90°) to but inclined at a predetermined slope from a horizontal plane. Subsequently, if exposed regions of the P-type semiconductor layer 40, the active layer 30 and the predetermined N-type semiconductor layer 20 are etched using the etching mask pattern with such a slope of the side surface, the side surfaces of the etched P-type semiconductor layer 40, active layer 30 and N-type semiconductor

layer 20 can be similarly formed into an inclined surface not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane.

<44> That is, after the photoresist has been applied at a thickness of 3 to 50㎛ on the P-type semiconductor layer 40 of Fig. 3a and light-exposed, a developed etching mask pattern is immediately formed without the hard-baking. The P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer 20. A portion of the exposed N-type semiconductor layer 20 may be further removed. Thereafter, if the etching mask pattern is removed, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured as shown in Fig. 3b.

<45> Alternatively, after a photoresist has been applied at a thickness of 3 to 50㎛ on the P-type semiconductor layer 40 of Fig. 3a and light-exposed, hard-baking may be performed. In such a case, if the photoresist is hard-baked at a temperature of 100 to 140℃ and then developed, the side surface of the developed photoresist may be etched to have a slope of 80 to 20° from a horizontal plane. For example, in a case where the hard-baking is performed at a temperature of 100℃, an etching mask pattern with a slope of about 80° from the horizontal plane can be obtained, and the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 can have a slope of about 80° from the horizontal plane using the etching mask pattern. Further, in a case where the hard-baking is performed at a temperature of 140℃, an etching mask pattern with a slope of about 20° from the horizontal plane can be obtained, and the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 can have a slope of about 20° from the horizontal plane using the etching mask pattern.

<46> The etching mask pattern, which the photoresist with a thickness of 3 to 50㎛ has been light-exposed and hard-baked at a temperature of 100 to 140℃ and then developed in such a manner, can be used such that the side surfaces of the etched the P-type semiconductor layer 40, active layer 30 and predetermined N-type semiconductor layer 20 have a slope of 80 to 20° from a horizontal plane similarly to the etching mask pattern. Then, light produced within a light emitting layer is not totally reflected on the etched side surface with a variety of slopes but emitted to the outside of a light emitting device

<47> A transparent electrode layer may be further formed on the P-type semiconductor layer 40 to reduce resistance of the P-type semiconductor layer 40 and enhancing transmittance of light, and an additional ohmic metal layer may be further formed on the P-type semiconductor layer 40 or the exposed N-type semiconductor layer 20 to facilitate current supply. The transparent electrode layer may be made of ITO (Indium Tin Oxide), ZnO or a transparent conductive metal, and the ohmic metal layer may be made of Cr or Au. Further, for the application of voltage, a P-type electrode may be further formed on the P-type semiconductor layer 40 and an N-type electrode may be further formed on the N-type semiconductor layer 20.

<48> Further, in order to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be

deposited on the rear surface of the substrate 10.

<49> As can be seen from this figure, a plurality of light emitting devices may be fabricated on a single substrate 10, which is cut into the individual light emitting devices. At this time, portions A shown in Fig. 3b are cutting portions used for individually cutting the plurality of light emitting devices.

<50> Accordingly, a light emitting device in which a portion of side surface of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 is not perpendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured.

<51> The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto. Various processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes.

<52> As described above, a portion of the side surface of the P-type semiconductor layer, the active layer and the N-type semiconductor layer of the light emitting device of the present disclosure is formed to be not perpendicular but inclined at a predetermined slope with respect to a horizontal plane, so that luminous efficiency can be enhanced as compared with that of the light emitting device of the related art. The reason is that a photon reflected on a flat surface in the related art is not reflected on a surface with a various angles but emitted to the outside.

<53> Figs. 4a to 4d are sectional views illustrating a process of manufacturing a light emitting device according to a second embodiment of the present invention.

<54> The second embodiment of the present invention is almost the same as the first embodiment. In the second embodiment, however, there is provided a light emitting device in which a plurality of light emitting cells are connected in series, parallel or series-parallel in a wafer level to reduce the size of the device, and they can be driven at proper voltage and current to be used for illustration purpose and can also be driven even with an AC power source.

<55> Referring to Fig. 4a, an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40 are sequentially formed on a substrate 10 through various deposition methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hydride Vapor Phase Epitaxy) and the like. A buffer layer may be further formed on the substrate 10 to reduce lattice mismatch between the substrate 10 and the subsequent layers upon growth of crystals. This is almost the same as the Fig. 3a, and descriptions overlapping with the previous embodiment will be omitted herein.

<56> Thereafter, portions of the P-type semiconductor layer 40 and the active layer 30 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 20. That is, after the photoresist has been applied at a thickness of 3 to 50㎛ on the P-type semiconductor layer 40 of Fig. 6 and light-exposed, it is developed without hard-baking to form an etching mask pattern. The P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer 20. A portion of the exposed N-type semiconductor layer 20 may be further removed. Thereafter, if the etching mask pattern is removed, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured as shown in Fig. 7.

<57> Alternatively, after a photoresist has been applied in a thickness of 3 to 50㎛ on the P-type semiconductor layer 40 of Fig. 6 and light-exposed, it is hard-baked at a temperature of 100 to 140℃ and developed such that an etching mask pattern can be formed. After the P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, have been etched, the etching mask pattern is removed such that the side surfaces of the etched P-type semiconductor layer 40 and active layer 30 can have a variety of slopes of 80 to 20°.

<58> Next, in order to form a plurality of light emitting cells on the substrate 10, predetermined regions of the exposed N-type semiconductor layer 20 are removed such that a portion of the substrate 10 can be exposed. To this end, a predetermined mask pattern is formed on all the portions except the predetermined regions where the substrate 10 will be exposed, and regions of the N-type semiconductor layer 20 that are exposed through the mask pattern are then etched such that the plurality of light emitting cells can be electrically isolated from one another as shown in Fig. 4c. At this time, the mask pattern whose side surface is inclined through the aforementioned process is formed and then used to etch the exposed N-type semiconductor layer 20 such that the side surface of the N-type semiconductor layer 20 in which the plurality of light emitting cells are separated from one another is not perpendicular to but inclined at a predetermined slope from a horizontal plane.

<59> A transparent electrode layer such as ITO may be further formed on the P-type semiconductor layer 40 to reduce resistance of the P-type semiconductor layer 40 and enhance transmittance of light, and an additional ohmic metal layer may be further formed using Cr, Au on the P-type semiconductor layer 40 or the exposed N-type semiconductor layer 20 to facilitate current supply.

<60> Referring to Fig. 4d, the N-type semiconductor layer 20 of a light emitting cell and the P-type semiconductor layer 40 of the adjacent light emitting cell are connected through a predetermined wiring process. That is, the exposed N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent light emitting cell are connected through a wire 60. At this time, the conductive wire 60 for electrically connecting the N-type and P-type semiconductor layers 20 and 40 are formed through a bridge process.

<61> The aforementioned bridge process is also called an air-bridge process. In the air-bridge process, a photosensitive liquid is applied between chips to be connected with each other through a photo process and developed to form a photoresist pattern, a material such as metal is first formed into a thin film on the photoresist pattern through a vacuum vapor deposition method or the like, and a conductive material containing gold (Au) is applied at a predetermined thickness onto the thin film through an electroplating, electroless plating or metal vapor deposition method. Thereafter, if the photoresist pattern is removed with a solution of a solvent or the like, a lower portion of the conductive material is completely removed, and thus, only the bridge-shaped conductive material is formed in a space between the adjacent light emitting cells.

<62> A step coverage process includes: applying a photosensitive liquid between chips to be connected with each other through a photo process; developing it to cover regions that are not assigned to the connection between the chips with a photoresist pattern; applying a conductive material including gold to have a predetermined thickness through an electroplating, electroless plating or metal vapor deposition method. Thereafter, if the photoresist pattern is removed with a solution of a solvent or the like, regions that are not covered with the conductive material are completely removed, and regions that are covered with the conductive material

remain to electrically connect the chips.

<63> The wire may be made of not only metal but also all kinds of conductive materials.

<64> Further, in order to apply an external voltage to the light emitting device, a P-type bonding pad 50 is formed on the P-type semiconductor layer 40 of the light emitting cell positioned at one edge of the substrate 10 and an N-type bonding pad 55 is formed on the exposed N-type semiconductor layer 20 of the light emitting cell positioned at the other edge of the substrate 10.

<65> Accordingly, a light emitting device in which the plurality of light emitting cells in each of which a portion of the side surface of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 is not perpendicular (90°) to but inclined at predetermined slope from a horizontal plane are connected with one another can be manufactured.

<66> The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment but is not limited thereto. Various modifications can be made or various material films can be further added. For example, in order to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10.

<67> Figs. 5a to 5d are sectional views illustrating a process of manufacturing a light emitting device according to a third embodiment of the present invention.

<68> The third embodiment is almost the same as the second embodiment. In the second embodiment, the N-type semiconductor layer 20 is first exposed and a portion of the exposed N-type semiconductor layer 20 is then removed to separate the light emitting cells from one another. In the third embodiment, however, a plurality of light emitting cells are first separated, and a portion of an N-type semiconductor layer 20 is then exposed. Descriptions overlapping with the previous embodiments will be omitted herein.

<69> Referring to Fig. 5a, portions of an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40, which are sequentially formed on a substrate 10, are removed to form a plurality of light emitting cells. To this end, after a photoresist has been applied at a thickness of 3 to 50㎛ on the P-type semiconductor layer 40 and light-exposed, it is immediately developed without hard-baking such that an etching mask pattern can be formed. The portions of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor pattern 20, which are exposed through the etching mask pattern, and the etching mask pattern is removed to separate the light emitting cells from one another. Accordingly, a light emitting device in which entire side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at a predetermined slope can be obtained as shown in this figure. Further, the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are removed using the etching mask pattern in which a photoresist is applied at a thickness of 3 to 50㎛ on the P-type semiconductor layer 40 and light-exposed and hard-baked at a temperature of 100 to 140℃ and then developed. Accordingly, the entire side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 can be formed at various slopes of 80 to 20°.

<70> Thereafter, as shown in Fig. 5b, portions of the P-type semiconductor

layer 40 and the active layer 30 are removed to expose a portion of the N-type semiconductor layer 20 through a predetermined etching process.

<71> A transparent electrode layer may be further formed on the P-type semiconductor layer 40 to reduce resistance of the P-type semiconductor layer 40 and enhance transmittance of light, and an additional ohmic metal layer may be further formed on the P-type semiconductor layer 40 or the exposed N-type semiconductor layer 20 to facilitate current supply. The transparent electrode layer may be made of ITO (Indium Tin Oxide), ZnO or a transparent conductive metal, and the ohmic metal layer may be made of Cr or Au

<72> Referring to Fig. 5c, the N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent light emitting cell are connected with each other through a bridge process.

<73> Further, in order to apply an external voltage to the light emitting device, a P-type bonding pad 50 is formed on the P-type semiconductor layer 40 of the light emitting cell positioned at one edge of the substrate 10 and an N-type bonding pad 55 is formed on the exposed N-type semiconductor layer 20 of the light emitting cell positioned at the other edge of the substrate 10.

<74> The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment but is not limited thereto. Various modifications can be made and various material films may be further added. For example, in order to enhance the heat dissipation characteristic of a light emitting device, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10.

<75> Further, even in a case where the plurality of light emitting cells are separated by etching such that the side surfaces may have various slopes as shown in Fig. 5a and then etched to expose the N-type semiconductor layer 20, a light emitting device can be manufactured using the same etching process as described above. That is, as shown in Fig. 5d, the side surfaces of the P-type semiconductor layer 40 and the active layer 30, which are etched to expose the N-type semiconductor layer 20, can be formed at various slopes.

<76> Accordingly, a light emitting device in which the plurality of light emitting cells each of which side surfaces of the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at predetermined slope from a horizontal plane are connected with one another can be manufactured.

<77> Figs. 6a and 6b are conceptual sectional views illustrating a difference between effects of the light emitting devices according to the prior art and the present invention.

<78> The light efficiency of a light emitting device may be expressed as internal quantum efficiency and external quantum efficiency, and the internal quantum efficiency is determined in accordance with the design and quality of an active layer. The external quantum efficiency is determined in accordance with a degree where a photon produced in an active layer is emitted to the outside of a light emitting device. Referring to Fig. 6a in which a conventional light emitting device is shown, a side surface of a semiconductor layer is formed perpendicular to a horizontal plane. In such a case, some portions of photons are not penetrated through the side surface of the semiconductor layer but reflected thereon, and totally reflected light is not emitted to the outside but dissipated within the light emitting device. However, referring to Fig. 6b in which a light emitting device according to

the present invention is shown, a side surface of a semiconductor layer is not perpendicular to but inclined at a predetermined slope from a horizontal plane. In such a case, the inclined side surface makes a critical angle of light change to help the light to be more easily extracted. Therefore, light generated in an active layer is not totally reflected but emitted to the outside of the light emitting device such that external quantum efficiency can be markedly enhanced.

[Advantageous Effects]

<79> Exemplary embodiments of the present disclosure provide a light emitting device and a method of manufacturing the same in which light produced from a side surface of a semiconductor layer, that is not perpendicular but inclined at a predetermined slope with respect to a horizontal plane, is not totally reflected but emitted to the outside of the light emitting device. Therefore, more enhanced characteristics of light extraction efficiency, external quantum efficiency, luminous efficiency or the like can be obtained. Further, a light emitting device provided in the present disclosure emits light with high luminous intensity and brightness and can be applied to a variety of products in which a superior light characteristic is necessary.

What is claimed is;

1. A light emitting device, comprising:

a substrate;

an N-type semiconductor layer formed on the substrate; and

a P-type semiconductor layer formed on the N-type semiconductor layer,

wherein a side surface including the N-type semiconductor layer and the P-type semiconductor layer has a slope of 20 to 80° from a horizontal plane.

2. A light emitting device, comprising:

a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on a portion of the N-type semiconductor layer on a substrate,

wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including the N-type or P-type semiconductor layer of the light emitting cell has a slope of 20 to 80° from a horizontal plane.

3. The light emitting device as claimed in claim 2, further comprising a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

4. The light emitting device as claimed in any one of claims 1 to 3, further comprising a transparent electrode layer on the P-type semiconductor layer.

5. The light emitting device as claimed in any one of claims 1 to 3, further comprising P-type and N-type ohmic metal layers containing Cr or Au on the P-type and N-type semiconductor layers, respectively.

6. A method of manufacturing a light emitting device, comprising:

sequentially forming N-type and P-type semiconductor layers on a substrate;

forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; and

removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern.

7. The method as claimed in claim 6, wherein a photoresist with a thickness of 3 to 50㎛ is used in the step of forming the etching mask pattern.

8. The method as claimed in claim 7, wherein the step of forming the etching mask pattern comprises the steps of:

applying the photoresist onto the P-type semiconductor layer;

light exposing the photoresist in accordance with a predetermined mask pattern; and

developing the light-exposed photoresist without a baking process after the light exposure.

9. The method as claimed in claim 7, wherein the step of forming the etching mask pattern comprises the steps of:

applying the photoresist onto the P-type semiconductor layer;

light exposing the photoresist in accordance with a predetermined mask pattern;

hard baking the light-exposed photoresist at a temperature of 100 to 140℃; and

developing the hard-baked photoresist.

10. The method as claimed in any one of claims 6 to 9, further comprising:

removing a portion of the N-type semiconductor layer exposed due to the removal of the P-type semiconductor layer to form a plurality of light emitting cell; and

connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a bridge wire.

11. The method as claimed in claim 10, wherein the bridge wire connects the N-type semiconductor layer of the one light emitting cell and the P-type semiconductor layer of the another adjacent light emitting cell through a bridge process or a step coverage process.

12. The method as claimed in any one of claims 6 to 9, further comprising:

removing a rear surface of the substrate at a certain thickness; and

depositing Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof onto the rear surface of the substrate,

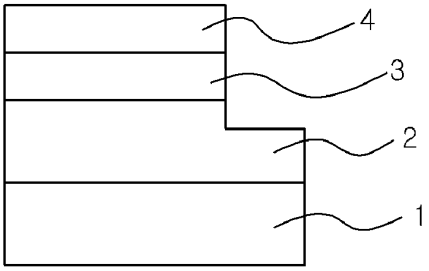
after removing the P-type semiconductor layer and the etching mask pattern.

ABSTRACT

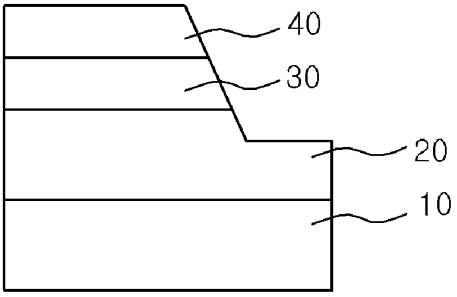
A light emitting device and a method of manufacturing the same are provided. The light emitting device includes a substrate, an N-type semiconductor layer formed on the substrate, and a P-type semiconductor layer formed on the N-type semiconductor layer, wherein a side surface including the N-type or P-type semiconductor layer has a slope of 20 to 80° from a horizontal plane. There is an advantage in that the characteristics of a light emitting device such as luminous efficiency, external quantum efficiency and extraction efficiency are enhanced and the reliability is secured such that light with high luminous intensity and brightness can be emitted.

DRAWINGS

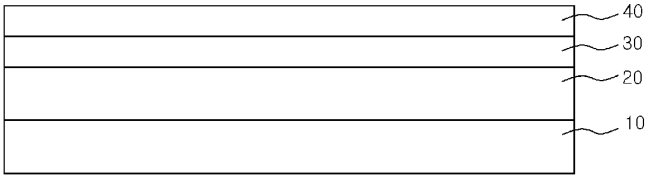
[Figure 1]



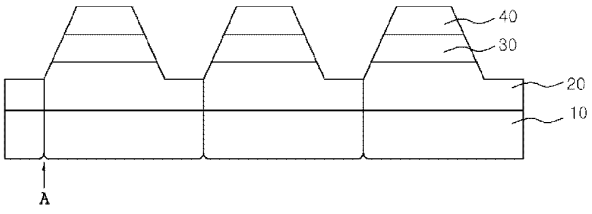
[Figure 2]



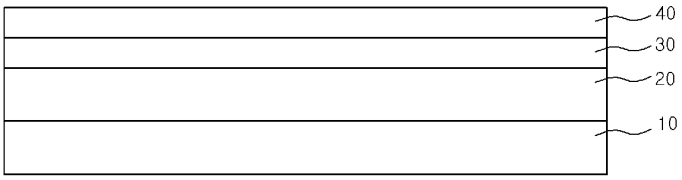
[Figure 3a]



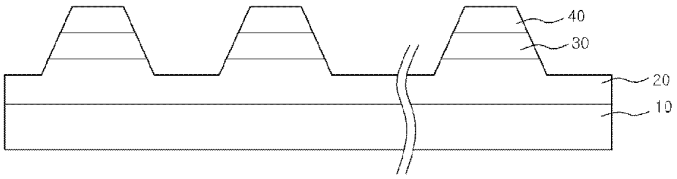
[Figure 3b]



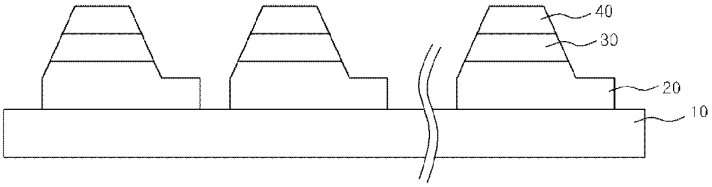
[Figure 4a]



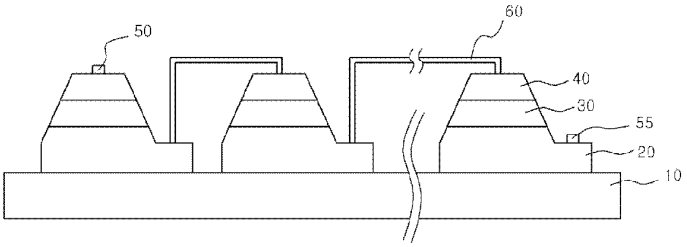
[Figure 4b]



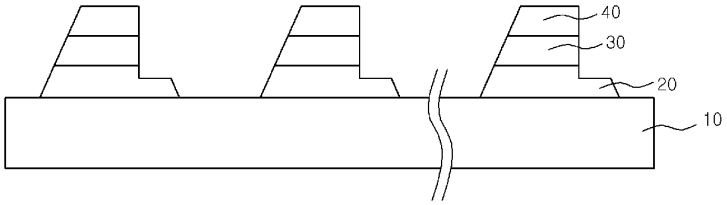
[Figure 4c]



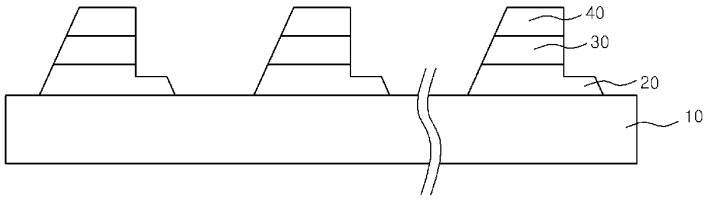
[Figure 4d]



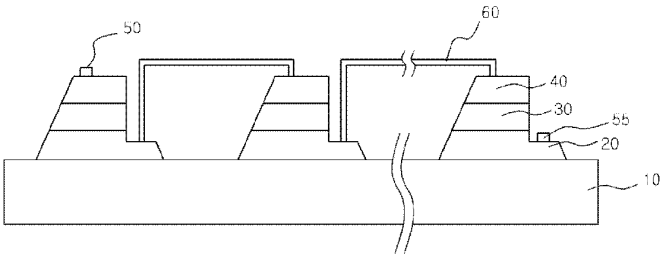
[Figure 5a]



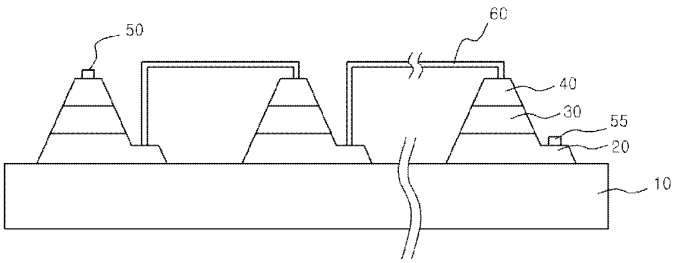
[Figure 5b]



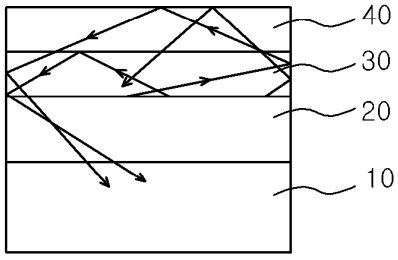
[Figure 5c]



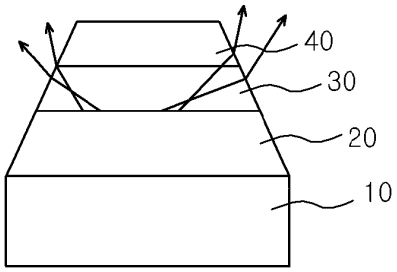
[Figure 5d]



[Figure 6a]



[Figure 6b]



VERIFICATION OF THE TRANSLATION

I, Seung-Hee NAM of Ein Patent Law Firm, 12F, Seojeon Bldg., 1330-9, Seocho-Dong, Seocho-Gu, Seoul, 137-858, Republic of Korea being fully conversant with both the English and the Korean language, declare the attached to be a true and accurate translation of the Korean Patent Application Nos. 10-2005-53797 filed on June 22, 2005, 10-2005-55179 filed on June 24, 2005, and 10-2006-21801 filed on March 8, 2006.

Signed by

Seung-Hee NAM

Dated this 1st day of September, 2009.

LIGHT-EMITTING DEVICE HAVING ARRAYED CELLS AND METHOD OF MANURACTURING THE SAME

BACKGROUND OF THE INVENTION

[Field of Invention]

<13> The present disclosure relates to a light emitting device having arrayed cells and a method of manufacturing the same. More specifically, the present disclosure relates to a light emitting device having a flip-chip structure, which is a light emitting device having arrayed cells with enhanced luminous efficiency and brightness and a method of manufacturing the same.

[Description of the Related Art]

<14> A light emitting device refers to an element in which minority carriers (electrons or holes) injected using a p-n junction structure of a semiconductor are produced and certain light is emitted due to recombination of the carriers. A light emitting source is formed from any one or combination of compound semiconductor materials such as GaAs, AlGaAs, GaN, InGaN and AlGaInP, so that a variety of colors can be implemented. For example, a red light emitting device may be formed from GaAsP or the like; a green light emitting device may be formed from GaP, InGaN or the like; a blue light emitting device may be formed using an InGaN/GaN double hetero structure; and a UV light emitting device may be formed using an AlGaN/GaN or AlGaN/AlGaN structure. In particular, GaN has a direct bandgap of 3.4eV at a normal temperature and a direct energy bandgap of 1.9eV (InN) to 3.4eV (GaN) or 6.2eV (AlN) by combining with a substance such as InN or AlN. Thus, GaN is a substance with great applicability to an optical element due to its broad wavelength range from visible light to ultraviolet light. Since the wavelength can be adjusted in such a manner, full-color implementation can be made by means of red, green and blue light emitting devices with a short wavelength range, so that the applicability to a general illumination market as well as a display device market is expected to be greatly increased.

<15> In particular, GaN has a direct bandgap of 3.4eV at a normal temperature and a direct energy bandgap of 1.9eV (InN) to 3.4eV (GaN) or 6.2eV (AlN) by combining with a substance such as InN or AlN. Thus, GaN is a substance with great applicability to an optical element due to its broad wavelength range from visible light to ultraviolet light. Since the wavelength can be adjusted in such a manner, full-color implementation can be made by means of red, green and blue light emitting devices with a short wavelength range, so that the applicability to a general illumination market as well as a display device market is expected to be greatly increased.

<16> Light emitting devices have characteristics of lower power consumption, longer lifespan, better installation in a narrow space and stronger resistance against vibration as compared with existing bulbs or fluorescent lamps. Since the light emitting devices are used as display devices and backlights and have superior characteristics in view of the reduction in power consumption and the durability, many studies for applying the light emitting devices to a general illumination field have been recently conducted. In the future, their applicability is expected to extend to a backlight of a large-sized LCD-TV, a vehicle headlight and general illumination.

To this end, it is necessary to improve luminous efficiency of light emitting devices, solve a heat dissipation problem, and achieve high brightness and output of the light emitting devices.

<17> As a solution to reduce such drawbacks, presently, a light emitting device having a flip-chip structure is being focused.

<18> Fig. 1 is a sectional view showing a light emitting device having a flip-chip structure in a related art.

<19> Referring to Fig. 1, the light emitting device includes an N-type semiconductor layer 5, an active layer 6 and a P-type semiconductor layer 7, which are sequentially formed on a base substrate 1. Portions of the P-type semiconductor layer 7 and the active layer 6 are etched to expose the N-type semiconductor layer 5 such that a light emitting cell can be formed. Further, an additional submount substrate 2 is prepared to form first and second electrodes 3 and 4 thereon, and a P-type solder 8 is formed on the first electrode 3 and an N-type solder 9 is formed on the second electrode 4. Thereafter, the light emitting cell is bonded to the submount substrate 2 such that P electrode of the light emitting cell is bonded with the P-type solder 8 and N electrode of the light emitting cell is bonded with the N-type solder 9. Molding portion (not shown) for sealing the substrate to which the light emitting cell is bonded is formed to fabricate a light emitting device.

<20> Since such a conventional light emitting device with a flip chip structure has high heat dissipation efficiency and substantially reduced shield of light, there is an advantage in that its light efficiency is increased by 50% or more as compared with a conventional light emitting device. Further, since a gold wire for driving a light emitting device is not necessary, many applications to a variety of small-sized packages can be considered.

<21> Light produced from a light emitting layer of a light emitting device is emitted from all the surfaces of a chip, and light extraction efficiency is generally determined by a critical angle of light. There are various indexes indicating the performance of light emitting devices, such as luminous efficiency (lm/W), internal quantum efficiency (%), external quantum efficiency (%) and extraction efficiency (%). The extraction efficiency is determined as a ratio of electrons injected into the light emitting device to photons emitted to the outside of the light emitting device. That is, the light emitting device becomes bright as the extraction efficiency becomes high. However, when the conventional light emitting device is etched to expose an N-type semiconductor layer, side surfaces of the P-type semiconductor layer and the active layer are vertically processed such that a portion of light produced within the light emitting device is totally reflected on the etched surface that is processed vertically from a horizontal plane. Then, a considerable amount of light to be totally reflected is not emitted to the outside but dissipated within the light emitting device due to the internal reflection. That is, there is a problem in that luminous efficiency in which electric energy is converted into light energy and the light is then emitted to the outside of a light emitting device is low.

SUMMARY OF THE INVENTION

<22> The present disclosure is conceived to solve the aforementioned problems. Accordingly, an object of the present invention is to provide a light emitting device having a flip-chip structure, which is a light emitting device with arrayed cells for emitting light with high luminous intensity and brightness by enhancing

characteristics of luminous efficiency, external quantum efficiency, extraction efficiency and the like and improving reliability, and a method of manufacturing the light emitting device.

<23> According to an aspect of the present disclosure for achieving the objects, there is provided a light emitting device comprising a substrate formed with a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on the N-type semiconductor layer, and a submount substrate flip-chip bonded onto the substrate. The N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including at least the P-type semiconductor layer of the light emitting cell has a predetermined slope other than a perpendicular angle with respect to a horizontal plane. The light emitting device may further comprise a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell. The predetermined slope may be 20 degrees to 80 degrees.

<24> According to another aspect of the present disclosure, there is provided a method of manufacturing a light emitting device including: sequentially forming N-type and P-type semiconductor layers on a substrate to form a light emitting cell on the substrate; forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; and removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern.

<25> Forming the light emitting cell on the substrate may include forming a plurality of light emitting cells by removing portions of the N-type semiconductor layer and P-type semiconductor layer. Forming the light emitting cell on the substrate may include connecting an N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a bridge wire, after removing the P-type semiconductor layer and the etching mask pattern. Forming the plurality of light emitting cells may include forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer; removing the N-type and P-type semiconductor layers exposed through the etching mask pattern to form a plurality of light emitting cells; and removing the etching mask pattern. The bridge wire may connect the N type semiconductor layer of one light emitting cell and the P type semiconductor layer of another adjacent light emitting cell through a bridge process or step coverage process.

<26> A photoresist with a thickness of 3 to 50㎛ may be used during forming the etching mask pattern.

<27> Forming the etching mask pattern may comprise the steps of: applying the photoresist onto the P-type semiconductor layer; light exposing the photoresist in accordance with a predetermined mask pattern; and developing the light-exposed photoresist without a baking process after the light exposure.

<28> Forming the etching mask pattern may comprise the steps of: applying the photoresist onto the P-type semiconductor layer; light exposing the photoresist in accordance with a predetermined mask pattern; hard baking the light-exposed photoresist at a temperature of 100 to 140℃; and developing the hard-baked photoresist.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will become apparent from the following description of preferred embodiments given in conjunction with the accompanying drawings, in which:

<1> Fig. 1 is a sectional view illustrating a light emitting device having a flip-chip structure in a related art;

<2> Fig. 2 is a conceptual sectional view illustrating a light emitting device according to the present disclosure;

<3> Figs. 3a to 3e are sectional views illustrating process of manufacturing a light emitting device according to a first exemplary embodiment of the present disclosure;

<4> Figs. 4a to 4d are sectional views illustrating a process of manufacturing a light emitting device according to a second exemplary embodiment of the present disclosure; and

<5> Fig. 5 is a sectional view illustrating a third exemplary embodiment of the present disclosure.

<6> <Reference numerals selected>

<7>	10:	substrate	20:	N-type semiconductor layer
<8>	30:	active layer	40:	P-type semiconductor layer
<9>	50:	N-type metal bump	55:	P-type metal bump
<10>	60:	wire	100:	submount substrate
<11>	110:	N-type bonding pad	115:	P-type bonding pad
<12>	120:	bonding layer		

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

<29> Hereinafter, a light emitting device and a manufacturing method thereof according to the present disclosure will be described in detail with reference to the accompanying drawings. However, the present invention is not limited to the embodiments set forth herein but can be implemented in different forms. Rather, the exemplary embodiments are merely provided to allow the present invention to be completely described herein and to fully convey the scope of the invention to those skilled in the art.

<30> Fig. 2 is a conceptual sectional view illustrating a light emitting device according to a present disclosure.

<31> Referring to the figure, the light emitting device comprises a light emitting layer, i.e. an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40 sequentially formed on a base substrate 10. Further, the light emitting device comprises a submount substrate 100 onto which the base substrate 10 with the light emitting layer formed thereon is flip-chip bonded through metal bumps 50 and 55. A side surface of the light emitting layer comprising the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20 is inclined at a slope of 20 to 80° from the horizontal plane and a critical angle of light is changed due to the side surface such that the light can be easily extracted. Therefore, luminous efficiency of the light emitting device can be improved.

<32> Figs. 3a to 3e are sectional views illustrating a process of manufacturing a light emitting device according to a first exemplary embodiment of the present

invention.

<33> Referring to Fig. 3a, an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40 are sequentially formed on a base substrate 10.

<34> The base substrate 10 refers to a general wafer used for fabricating a light emitting device is made of a transparent substrate such as Al_2O_3, ZnO and $LiAl_2O_3$. In this embodiment, a crystal growth substrate made of sapphire is used.

<35> Buffer layer (not shown) may be further formed on the substrate 10 to reduce lattice mismatch between the substrate 10 and the subsequent layers upon growth of crystals. The buffer layer may contain GaN or AlN that is a semiconductor material.

<36> The N-type semiconductor layer 20 is a layer in which electrons are produced and is preferably made from GaN doped with N-type impurities. However, the N-type semiconductor layer 20 is not limited thereto but may use a material layer having a variety of semiconductor properties. The N-type semiconductor layer 20 including N-type $Al_xGa_{1-x}N(0 \leq x \leq 1)$ is formed in this embodiment. Further, the P-type semiconductor layer 40 is a layer in which holes are produced and is preferably made from GaN doped with P-type impurities. However, the P-type semiconductor layer 40 is not limited thereto but may use a material layer with a variety of semiconductor properties. The P-type semiconductor layer 40 including P-type $Al_xGa_{1-x}N(0 \leq x \leq 1)$ is formed in this embodiment. Moreover, InGaN may be used as the semiconductor layer. Further, each of the N-type and P-type semiconductor layers 20 and 40 may be formed as a multiple layer.

<37> The active layer 30 has a predetermined bandgap and is a region where a quantum well is formed so that electrons and holes are recombined. The active layer 30 may contain InGaN. The wavelength of light emitted through the combination of electrons and holes varies according to the kind of a material constituting the active layer 30. Therefore, it is preferred that a semiconductor material contained in the active layer 30 be controlled depending on a target wavelength.

<38> The aforementioned material layers are formed through a variety of deposition and growth methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hydride Vapor Phase Epitaxy) and the like.

<39> Thereafter, portions of the P-type semiconductor layer 40 and the active layer 30 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 20. An etching mask pattern is formed on the P-type semiconductor layer 40, and the P-type semiconductor layer 40 and the active layer 30 are then removed through a dry or wet etching process to expose the N-type semiconductor layer 20.

<40> Generally, in order to perform the etching process, a photoresist has been applied onto a top surface of the P-type semiconductor layer 40 at a thickness of 1 to 2㎛, and then soft-baked at a temperature of 80 to 90℃ is performed. Next, an exposure process in which light in a UV range is irradiated through a predetermined photo mask to transfer a pattern formed on the mask to the applied photoresist is executed. Thereafter, the photoresist is hard-baked at a temperature of 100 to 120℃, and a developing process in which the photoresist at a portion with relatively weak combination through the exposure process is melted using a solvent is executed. A predetermined etching mask pattern is formed on the P-type semiconductor layer

40 through the above process.

<41> However, in this embodiment, the photoresist is applied at a thickness of 3 to 50㎛ which is thicker as compared with the prior art when the etching mask pattern is formed, and the exposure process is performed after the soft-baking. Next, if the photoresist is directly developed without the hard-baking, a developed side surface of the remaining photoresist is formed into an inclined surface not perpendicular (90°) to but inclined at a predetermined slope from a horizontal plane. Subsequently, if exposed regions of the P-type semiconductor layer 40, the active layer 30 and the predetermined N-type semiconductor layer 20 are etched using the etching mask pattern with such a slope of the side surface, the side surfaces of the etched P-type semiconductor layer 40, active layer 30 and N-type semiconductor layer 20 can be similarly formed into an inclined surface not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane.

<42> That is, after the photoresist has been applied at a thickness of 3 to 50㎛ on the P-type semiconductor layer 40 of Fig. 3a and light-exposed, a developed etching mask pattern is immediately formed without the hard-baking. The P-type semiconductor layer 40 and the active layer 30, which are exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to expose the N-type semiconductor layer 20. A portion of the exposed N-type semiconductor layer 20 may be further removed. Thereafter, if the etching mask pattern is removed, a light emitting device in which the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at the predetermined slope from a horizontal plane can be manufactured as shown in Fig. 5.

<43> Alternatively, after a photoresist has been applied at a thickness of 3 to 50㎛ on the P-type semiconductor layer 40 of Fig. 3a and light-exposed, hard-baking may be performed. In such a case, if the photoresist is hard-baked at a temperature of 100 to 140℃ and then developed, the side surface of the developed photoresist may be etched to have a slope of 80 to 20° from a horizontal plane. For example, in a case where the hard-baking is performed at a temperature of 100℃, an etching mask pattern with a slope of about 80° from the horizontal plane can be obtained, and the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 can have a slope of about 80° from the horizontal plane using the etching mask pattern. Further, in a case where the hard-baking is performed at a temperature of 140℃, an etching mask pattern with a slope of about 20° from the horizontal plane can be obtained, and the side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 can have a slope of about 20° from the horizontal plane using the etching mask pattern.

<44> The etching mask pattern, which the photoresist with a thickness of 3 to 50㎛ has been light-exposed and hard-baked at a temperature of 100 to 140℃ and then developed in such a manner, can be used such that the side surfaces of the etched the P-type semiconductor layer 40, active layer 30 and predetermined N-type semiconductor layer 20 have a slope of 80 to 20° from a horizontal plane similarly to the etching mask pattern. Then, light produced within a light emitting layer is not totally reflected on the etched side surface with a variety of slopes but emitted to the outside of a light emitting device.

<45> A reflection layer for reflecting light may be further formed on a top

surface of the P-type semiconductor layer 140, and an additional ohmic metal layer for facilitating the supply of current may be further formed on a top surface of the P-type semiconductor layer 140 or the exposed N-type semiconductor layer 120. The ohmic metal layer may be made of Cr or Au.

<46> Further, P-type and N-type metal bumps 55 and 50 are formed on the P-type and N-type semiconductor layers 40 and 20, respectively, as shown in Fig. 3c. Each of the P-type and N-type metal bumps 55 and 50 may be made of at least one material selected from the group consisting of Pb, Sn, Au, Ge, Cu, Bi, Cd, Zn, Ag, Ni, Ti and an alloy thereof. To this end, a photoresist is applied onto an entire structure and a photoresist pattern (not shown) through which portions of the P-type and N-type semiconductor layers 40 and 20 are exposed is formed through a photo-etching process using a predetermined mask. After a metal film has been deposited on the entire structure, metal film portions formed on regions other than regions on the P-type and N-type semiconductor layers 40 exposed through the photoresist pattern and the photoresist pattern are removed. Accordingly, the P-type and N-type metal bumps 55 and 50 are formed on the P-type and N-type semiconductor layers 40 and 20, respectively.

<47> Next, referring to Fig. 3d, an additional submount substrate 100 is prepared to form P-type and N-type bonding pads 115 and 110 connected to the P-type and N-type metal bumps 55 and 50, respectively.

<48> At this time, various kinds of superior heat conductive substrates 100 are used as the submount substrate 100. That is, the submount substrate 100 may be made of SiC, Si, Ge, SiGe, AlN, metal or the like. In this embodiment, AlN with superior heat conductivity and insulation property is used. The present invention is not limited thereto, but a metallic material with superior heat and electric conductivity may be employed. In this case, an insulation or dielectric film is formed on the substrate 100 to sufficiently serve as an insulation. The dielectric film may be made of SiO2, MgO and SiN or an insulating material. Further, each of the P-type and N-type bonding pads 110 and 115 is made of a metal with superior electric conductivity. This is formed through a screen printing process or a deposition process using a predetermined mask pattern.

<49> Thereafter, the submount substrate 100 is flip-chip bonded onto the base substrate 10 with the light emitting layer formed thereon.

<50> Referring to Fig. 3e, in the light emitting device of the present invention, the N-type and P-type metal bumps 50 and 55 formed on the top of the light emitting layer are bonded and connected with the N-type and P-type bonding pads 110 and 115 of the submount substrate 100, respectively.

<51> At this time, the bonding pads and metal bumps may be bonded using heat or ultrasonic waves or simultaneously using the heat and ultrasonic waves. The metal bumps 50 and 55 and the lower bonding pads 110 and 115 are connected through a variety of bonding methods.

<52> Moreover, the N-type and P-type metal bumps 50 and 55 are not formed on the top of the light emitting layer but may be formed on the submount substrate 100.

<53> As can be seen from this figure, a plurality of light emitting devices may be fabricated on a single substrate 10, which is cut into the individual light emitting devices. At this time, portions A shown in Fig. 3e are cutting portions used for individually cutting the plurality of light emitting devices.

<54> Accordingly, a light emitting device with a flip chip structure, in which the side surfaces of the P-type semiconductor layer, the active layer and a portion of

the N-type semiconductor layer are not perpendicular (90°) to but inclined at the predetermined slope from the horizontal plane, can be manufactured.

<55> The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto. Various processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes.

<56> For example, in the same process as the previous exemplary embodiments, the base substrate with the N-type semiconductor layer, the active layer and the P-type semiconductor layer sequentially formed thereon is prepared as shown in Fig. 3a. Then, portions of the P-type semiconductor layer, the active layer and the N-type semiconductor layer are first removed to expose the substrate such that the plurality of light emitting devices can be individually isolated. At this time, the side surfaces of the P-type semiconductor layer, the active layer and the N-type semiconductor layer, which are etched through the aforementioned process, may be formed not to be perpendicular (90°) to but inclined at a predetermined slope.

<57> As described above, in a light emitting device having a flip-chip structure, a side surface of a light emitting layer may be formed to be not perpendicular but inclined at a predetermined slope with respect to a horizontal plane, so that light emitting efficiency can be improved compared with a conventional light emitting device. Light produced from a side surface of a semiconductor layer, which is not perpendicular to but inclined at a predetermined slop from a horizontal plane, is not totally reflected but emitted to the outside of the light emitting device. The reason is that a photon reflected on a flat surface in the related art is not reflected on a surface with various angles but emitted to the outside.

<58> Figs. 4a to 4b are sectional views illustrating a process of manufacturing a light emitting device according to a second exemplary embodiment of the present invention.

<59> The second exemplary embodiment is almost the same as the first exemplary embodiment. In the second exemplary embodiment, however, there is provided a light emitting device with a flip chip structure, in which a plurality of light emitting cells are connected in series, parallel or series-parallel in a wafer level to reduce the size of the device, and they can be driven at proper voltage and current to be used for illumination purpose and can also be driven even with an AC power source. Descriptions overlapping with the previous exemplary embodiments will be omitted herein.

<60> Referring to Fig. 4a, an N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor layer 40 are sequentially formed on a base substrate 10 through various deposition methods including MOCVD (Metal Organic Chemical Vapor Deposition), CVD (Chemical Vapor Deposition), PCVD (Plasma-enhanced Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), HVPE (Hydride Vapor Phase Epitaxy) and the like. A buffer layer may be further formed on the substrate 10 to reduce lattice mismatch between the substrate 10 and the subsequent layers upon growth of crystals.

<61> Thereafter, portions of the N-type semiconductor layer 20, the active layer 30 and the P-type semiconductor layer 40, which are sequentially formed on the base substrate 10, are removed to form a plurality of light emitting cells. To this end, after a photoresist has been applied at a thickness of 3 to 50㎛ on the P-type semiconductor layer 40 and light-exposed, it is immediately developed without hard-baking to form an etching mask pattern. The P-type semiconductor 40, the active layer 30 and the predetermined N-type semiconductor layer 20, which are

exposed through the etching mask pattern, are removed through an ICP (Inductive Coupled Plasma) or dry etching process to separate the light emitting cells from one another. Next, if the etching mask pattern is removed, a light emitting device in which entire side surfaces of the etched P-type semiconductor layer 40, active layer 30 and N-type semiconductor layer 20 are not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane can be obtained.

<62> Alternatively, after a photoresist has been applied at a thickness of 3 to 50㎛ on the P-type semiconductor layer 40 and light-exposed, it is hard-baked at a temperature of 100 to 140℃ and developed such that an etching mask pattern can be formed. After the P-type semiconductor layer 40, the active layer 30 and the N-type semiconductor layer 20, which are exposed through the etching mask pattern, have been etched, the etching mask pattern is removed such that the side surfaces of the etched P-type semiconductor layer 40 and active layer 30 can be inclined at various slopes of 80 to 20°.

<63> Next, portions of the P-type semiconductor layer 40 and the active layer 30 are removed through a predetermined etching process to expose a portion of the N-type semiconductor layer 20, as shown in Fig. 4c. The exposed N-type semiconductor layer 20 of one light emitting cell and the P-type semiconductor layer 40 of another adjacent light emitting cell are connected with each other through a predetermined conductive wire. At this time, a bridge wire 60 is made of a conductive material, e.g. metal. It will be apparent that the bridge wire 60 may be made of a silicone compound doped with impurities. The bridge wire 60 is formed through a bridge process or a step coverage process.

<64> The aforementioned bridge process is also called an air-bridge process. In the air-bridge process, a photosensitive liquid is applied between chips to be connected with each other through a photo process and developed to form a photoresist pattern, a material such as metal is first formed into a thin film on the photoresist pattern through a vacuum vapor deposition method or the like, and a conductive material containing gold (Au) is applied at a predetermined thickness onto the thin film through an electroplating, electroless plating or metal vapor deposition method. Thereafter, if the photoresist pattern is removed with a solution of a solvent or the like, a lower portion of the conductive material is completely removed, and thus, only the bridge-shaped conductive material is formed in a space between the adjacent light emitting cells.

<65> A step coverage process includes: applying a photosensitive liquid between chips to be connected with each other through a photo process; developing it to cover regions that are not assigned to the connection between the chips with a photoresist pattern; applying a conductive material including gold to have a predetermined thickness through an electroplating, electroless plating or metal vapor deposition method. Thereafter, if the photoresist pattern is removed with a solution of a solvent or the like, regions that are not covered with the conductive material are completely removed, and regions that are covered with the conductive material remain to electrically connect the chips.

<66> Further, a plurality of metal bumps are formed on the top of the light emitting cells, and P-type and N-type metal bumps 55 and 50 are further formed on the P-type semiconductor layer 40 of the light emitting cell positioned at one edge of the substrate 10 and the N-type semiconductor layer 20 of the light emitting cell positioned the other edge of the substrate, respectively.

<67> Next, as shown in Fig. 4d, an additional submount substrate 100 is prepared, on which a plurality of bonding layers 120, a P-type bonding pad 115

positioned at one edge of the submount substrate 100 and an N-type bonding pad 110 positioned at the other edge of the submount substrate are formed.

<68> Thereafter, as can be shown in Fig. 4e, the aforementioned base substrate 10 with the plurality of light emitting cells formed thereon is flip-chip bonded onto the submount substrate 100 to fabricate the light emitting device. The substrates are bonded with each other through the metal bumps 50 and 55 formed on the top of the light emitting cell and the bonding layers 120 formed on the submount substrate 100, respectively. The P-type bonding pad 115 positioned at one edge of the submount substrate 100 is connected to the P-type metal bump 55 of the light emitting cell positioned at one edge of the base substrate 10, whereas the N-type bonding pad 110 positioned at the other edge of the submount substrate 100 is connected to the N-type metal bump 50 of the light emitting cell positioned at the other edge of the base substrate 10.

<69> The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment, but is not limited thereto. Various processes and manufacturing methods may be modified or added depending on the characteristics of devices and the convenience of processes.

<70> For example, in this exemplary embodiment, the bridge wire for electrically connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell is formed through a bridge process or a step coverage process, and the base substrate is then flip-chip bonded onto the submount substrate. However, the present invention is not limited thereto. That is, an electrode layer may be formed on the submount substrate when the plurality of light emitting cells are flip-chip bonded onto the submount substrate such that the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are electrically connected through the metal bumps.

<71> Accordingly, a light emitting device in which a plurality of flip chip light emitting cells each having a side surface of a light emitting layer, which is not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane, are arrayed on the submount substrate can be manufactured. The light emitting cells may be connected in various ways, i.e. in series, parallel or series-parallel, depending on the desired purpose.

<72> Fig. 5 is a sectional view showing a third exemplary embodiment according to the present invention.

<73> The third exemplary embodiment is almost the same as the second exemplary embodiment. In this embodiment, even in a case where a plurality of light emitting cells are separated by etching such that the side surfaces may have slopes as shown in Fig. 4b and then etched to expose an N-type semiconductor layer, a light emitting device can be manufactured using the same etching process as the previous embodiment. That is, side surfaces of a P-type semiconductor layer 40 and an active layer 30 etched to expose an N-type semiconductor layer 20 are formed with various slopes, as shown in Fig. 5. In such a light emitting device, light emitting efficiency can be improved because photon reflected on a flat surface in the related art is not reflected on a surface with various angles but emitted to the outside.

<74> Accordingly, a light emitting device in which a plurality of flip chip light emitting cells each having an entire side surface of a light emitting layer, which is not perpendicular (90°) to but inclined at a predetermined slope from the horizontal plane, are arrayed on the submount substrate can be manufactured. The light emitting cells may be connected in various ways, i.e. in series, parallel or

series-parallel, depending on the desired purpose.

<75> The light efficiency of a light emitting device may be expressed as internal quantum efficiency and external quantum efficiency, and the internal quantum efficiency is determined in accordance with the design and quality of an active layer. The external quantum efficiency is determined in accordance with a degree where a photon produced in an active layer is emitted to the outside of a light emitting device. Referring to Fig. 30 in which a conventional light emitting device is shown, a side surface of a semiconductor layer is formed perpendicular to a horizontal plane. In such a case, some portions of photons are not penetrated through the side surface of the semiconductor layer but reflected thereon, and totally reflected light is not emitted to the outside but dissipated within the light emitting device. However, referring to Fig. 31 in which a light emitting device according to the present invention is shown, a side surface of a semiconductor layer is not perpendicular to but inclined at a predetermined slope from a horizontal plane. In such a case, the inclined side surface makes a critical angle of light change to help the light to be more easily extracted. Therefore, light generated in an active layer is not totally reflected but emitted to the outside of the light emitting device such that external quantum efficiency can be markedly enhanced.

[Advantageous Effects]

<76> Exemplary embodiments of the present disclosure provide a light emitting device having arrayed cells and a method of manufacturing the same in which light produced in an active layer is not totally reflected at an inclined surface having a predetermined slope but emitted to the outside of the light emitting device to achieve enhanced light extraction efficiency. Further, exemplary embodiments of the present disclosure provide a light emitting device having arrayed cells and a method of manufacturing the same having improved heat dissipation efficiency and substantially low shield of light, so that light efficiency can be increased.

<77> A light emitting device having arrayed cells and a method of manufacturing the same according to the present disclosure can emit light having high luminous intensity and high brightness by enhancing characteristics of luminous efficiency, external quantum efficiency and the like and improving reliability.

What is claimed is:

1. A light emitting device, comprising:

a substrate formed with a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on the N-type semiconductor layer; and

a submount substrate flip-chip bonded onto the substrate,

wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including at least the P-type semiconductor layer of the light emitting cell has a slope other than perpendicular angle with respect to a horizontal plane.

2. The light emitting device as claimed in claim 1, further comprising a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

3. The light emitting device as claimed in claim 1 or 2, wherein the slope is in a range of 20 degrees to 80 degrees.

4. A method of manufacturing a light emitting device, comprising the steps of:

sequentially forming N-type and P-type semiconductor layers on a substrate to form a light emitting cell on the substrate;

forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a slope with respect to a horizontal plane, on the P-type semiconductor layer;

removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern; and

flip-chip bonding the substrate onto an additional submount substrate.

5. The light emitting device as claimed in claim 4, wherein forming the light emitting cells on the substrate comprises: forming a plurality of light emitting cells by removing portions of the N-type semiconductor layer and the P-type semiconductor layer; and

connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell through a bridge wire, after removing the P-type semiconductor layer and the etching mask pattern.

6. The method as claimed in claim 5, wherein forming the plurality of light emitting cells comprises:

forming an etching mask pattern, of which side surface is not perpendicular to but inclined at a predetermined slope from a horizontal plane, on the P-type semiconductor layer;

removing the N-type and P-type semiconductor layers exposed through the etching mask pattern to form a plurality of light emitting cells; and

removing the etching mask pattern.

7. The method as claimed in claim 5, wherein the bridge wire connects the N type semiconductor layer of one light emitting cell and the P type semiconductor layer of another adjacent light emitting cell through a bridge or step coverage process.

8. The method as claimed in any one of claims 4 to 7, wherein a photoresist with a thickness of 3 to 50㎛ is used durin forming the etching mask pattern.

9. The method as claimed in claim 8, wherein forming the etching mask pattern comprises:

applying the photoresist onto the P-type semiconductor layer;

light exposing the photoresist in accordance with a predetermined mask pattern; and

developing the light-exposed photoresist without a baking process after the light exposure.

10. The method as claimed in claim 8, wherein forming the etching mask pattern comprises:

applying the photoresist onto the P-type semiconductor layer;

light exposing the photoresist in accordance with a predetermined mask pattern;

hard baking the light-exposed photoresist at a temperature of 100 to 140℃; and

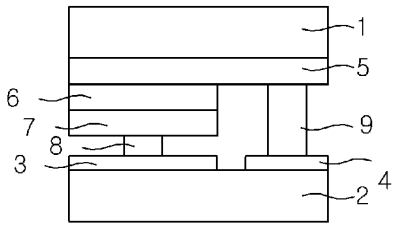
developing the hard-baked photoresist.

ABSTRACT

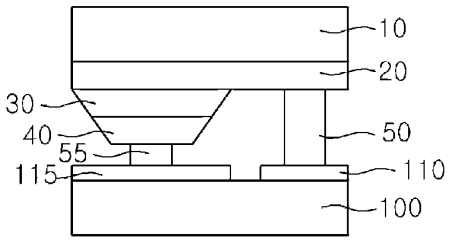
A light emitting device having arrayed cells and method of manufacturing the same are provided. The light emitting device includes: a substrate formed with a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on the N-type semiconductor layer; and a submount substrate flip-chip bonded onto the substrate. The N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including at least the P-type semiconductor layer of the light emitting cell has a slope other than perpendicular angle with respect to a horizontal plane. There is an advantage in that the characteristics of a light emitting device such as luminous efficiency, external quantum efficiency and extraction efficiency are enhanced and the reliability is secured such that light with high luminous intensity and brightness can be emitted.

DRAWINGS

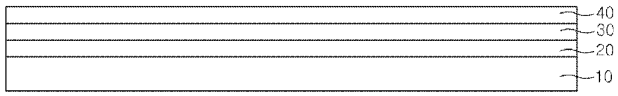
[Figure 1]



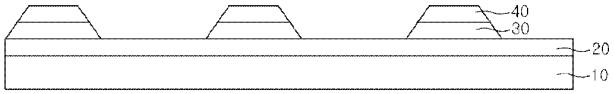
[Figure 2]



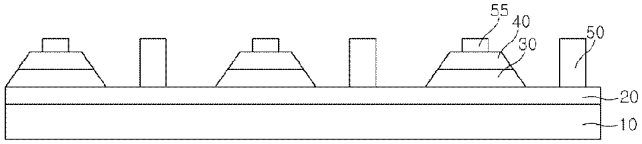
[Figure 3a]



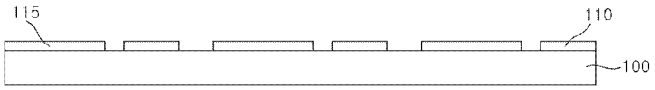
[Figure 3b]



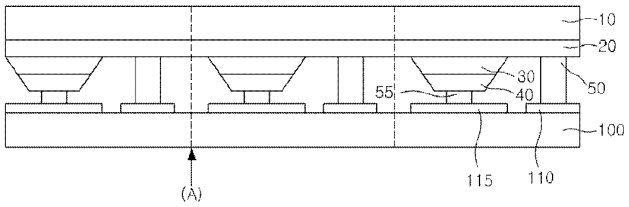
[Figure 3c]



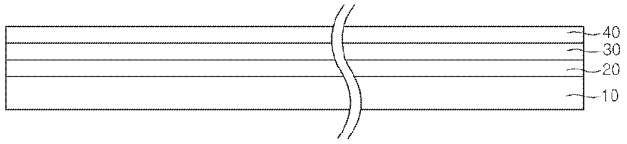
[Figure 3d]



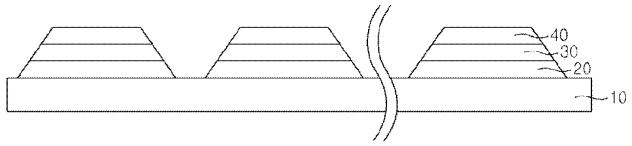
[Figure 3e]



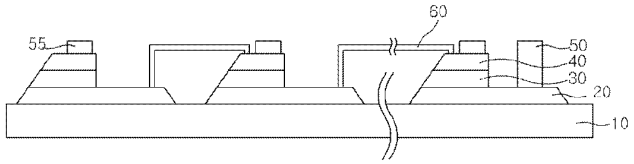
[Figure 4a]



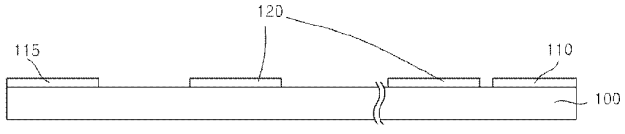
[Figure 4b]



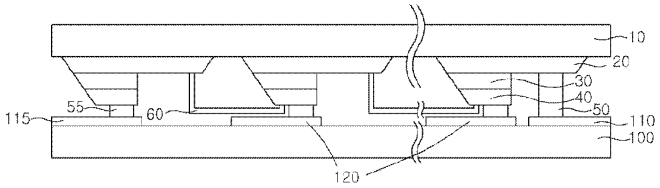
[Figure 4c]



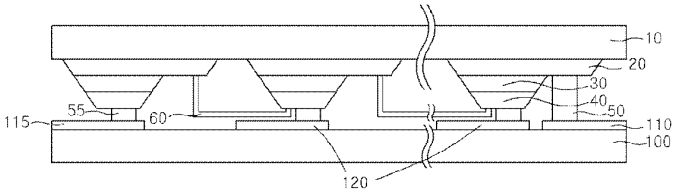
[Figure 4d]



[Figure 4e]



[Figure 5]



VERIFICATION OF THE TRANSLATION

I, Seung-Hee NAM of Ein Patent Law Firm, 12F, Seojeon Bldg., 1330-9, Seocho-Dong, Seocho-Gu, Seoul, 137-858, Republic of Korea being fully conversant with both the English and the Korean language, declare the attached to be a true and accurate translation of the Korean Patent Application Nos. 10-2005-53797 filed on June 22, 2005, 10-2005-55179 filed on June 24, 2005, and 10-2006-21801 filed on March 8, 2006.

Signed by

Seunghee Nam

Seung-Hee NAM

Dated this 1st day of September, 2009.

LIGHT EMITTING DIODE FOR AC OPERATION WITH WIRES AND METHOD OF FABRICATING THE SAME

BACKGROUND OF THE INVENTION

[Field of Invention]

<5> The present disclosure relates to a light emitting diode for AC operation and a method of manufacturing the same, and more specifically, to a light emitting diode for AC operation capable of preventing disconnection of wires and/or short circuit by wires and a method of manufacturing the same.

[Description of the Related Art]

<6> A gallium nitride based light emitting diode has been employed and developed for about ten years. LED technologies have been changed a lot due to GaN based LEDs, and presently, are used in various applications such as color LED display devices, LED traffic lights, white LEDs and so forth. In particular, efficiency of white LEDs is getting closer to that of commercial fluorescent lamp.

<7> In general, a light emitting diode emits light by forward bias current and requires supply of direct current. When a light emitting diode is directly connected to AC power supply, it repeatedly turns on/off according to a direction of current. That is a light emitting diode directly connected to AC power supply is not able to continuously emit light and easily damaged by reverse bias current.

<8> A light emitting diode which can be directly connected to high voltage AC power supply by reducing the above described drawbacks is disclosed in International Publication No. WO 2004/023568 (A1) entitled "LIGHT-EMITTING DEVICE HAVING LIGHT-EMITTING ELEMENTS" BY SAKAI et. Al.

<9> Fig. 1 is a partial plan view illustrating a light emitting diode for AC operation according to the WO 2004/023568 (A1), and Fig. 2 is a sectional view along line IV-IV of Fig. 1

<10> Referring to Figs. 1 and 2, a plurality of light emitting cells 1 are formed on a substrate 10. Further, a p-electrode 22 and an n-electrode 24 are formed on the light emitting cells 1. Air-bridge wires 28 electrically connect the p-electrodes 22 and n-electrodes 24 of adjacent light emitting cells, so that the plurality of light emitting cells can be connected in series.

<11> Each light emitting cell includes an n-GaN layer 14 and a p-GaN layer 20. Although not shown, an InGaN active layer may be disposed between the n-GaN layer 14 and the p-GaN layer 20. The p-electrode 22 is formed on the p-GaN layer 20, and the n-electrode 24 is formed on the n-GaN layer 14. The air-bridge wires 28 electrically connect the n-electrode 24 and the p-electrode 22.

<12> According to the WO 2004/023568 (A1), LEDs (light emitting cells) are connected in series on an insulating substrate such as sapphire substrate to form an LED array. Two LED arrays are connected in reverse parallel on the sapphire substrate. As such, a single chip light emitting device which can operate by AC power supply may be provided.

<13> However, the p-electrode 22 and the n-electrode 24 are connected by the air-bridge wire 28 as shown in Fig. 2, in which a part of the wire other than contact portions hangs in the air. In such a configuration, the air-bridge wire 28 may be easily disconnected by external pressure, and may cause a short circuit due to a deformation by external pressure.

SUMMARY OF THE INVENTION

<14> The present disclosure provides a light emitting diode for AC operation capable of preventing disconnection or short circuit of wires by external pressure.

<15> The present disclosure provides a light emitting diode for AC operation capable of preventing short circuit of light emitting cells by remaining metallic materials after the wires are formed.

<16> The present disclosure provides a method of fabricating a light emitting diode for AC operation capable of preventing disconnection and/or short circuit of wires.

<17> An aspect of the present disclosure provides a light emitting diode for AC operation comprising having robust wires. The light emitting diode may include light emitting cells spaced apart from each other on a substrate. Each of the light emitting cells may include a lower semiconductor layer, an upper semiconductor layer disposed on a region of the lower semiconductor layer, and an active layer disposed between the lower semiconductor layer and the upper semiconductor layer. Side surfaces of the light emitting cells may be formed to be inclined with respect to an upper surface of the substrate and get narrowed toward upside. An insulation layer may cover entire surface of the light emitting cells. The insulation layer may include opening portions respectively formed on another regions of the lower semiconductor layers and on the upper semiconductor layers. Wires may be formed on the insulation layer and electrically connected to the lower semiconductor layers and the upper semiconductor layers through the opening portions. The wires electrically connect the lower semiconductor layers and the upper semiconductor layers of adjacent light emitting cells. Since the wires are formed on the insulation layer, disconnection and short circuit of the wires may be prevented, so that a reliable light emitting diode for AC operation can be provided.

<18> Inclination angles of the side surfaces of the lower semiconductor layers of the respective light emitting cells may be in a range of 15 degrees to 80 degrees. Accordingly, the wires can be formed by deposition and patterning of a metal layer, so that a robust wires can be easily formed.

<19> Electrode pads may be disposed between the another regions of the lower semiconductor regions and the insulation layer. The electrode pads may be exposed through the opening portions formed on the another portions of the lower semiconductor layers. Accordingly, the wires are in contact with the electrode pads to be electrically connected to the lower semiconductor layer.

<20> Transparent electrode layers may be disposed between the upper semiconductor layers and the insulation layer. The transparent electrode layers may be exposed through the opening portions formed on the upper semiconductor layers. Accordingly, the wires are in contact with the transparent electrodes to be electrically connected to the upper semiconductor layer. The transparent electrodes disperse current in the upper semiconductor layers, and transmit light produced in the active layer.

<21> A protecting insulation layer may cover the wires and the insulation layer. The protecting insulation layer may prevent deformation of the wires by external pressure and contamination of the wires by moisture and so forth.

<22> Another aspect of the present disclosure provides a method of manufacturing a light emitting diode for AC operation having a robust wires. The

method may include forming light emitting cells spaced apart from each other on a substrate. The light emitting cells may include a lower semiconductor layer, an upper semiconductor layer disposed on a region of the lower semiconductor layer, and an active layer disposed between the lower semiconductor layer and the upper semiconductor layer, and side surfaces of the light emitting cells are formed to be inclined with respect to an upper surface of the substrate and get narrowed toward upside. A continuous (conformal) insulation layer may be formed on the substrate on which the light emitting cells are formed. Thereafter, the insulation layer may be patterned and opening portions may be formed on another regions of the lower semiconductor layers and on the upper semiconductor layers. Then, wires may be formed on the insulation layer. The wires may be electrically connected to the lower semiconductor layers and the upper semiconductor layers through the opening portions, and electrically connect the lower semiconductor layers and the upper semiconductor layers of adjacent light emitting cells. According to the aspect of the present disclosure, it is easy to continuously form the insulation layer because the side surfaces of the light emitting cells are formed to be inclined. Further, as the insulation layer can be formed continuously (conformal insulation layer), the insulation layer may prevent short circuit of the light emitting cells. In addition, the wires may be formed to be supported by the insulation layer, a reliable light emitting diode for AC operation can be fabricated.

<23> Meanwhile, electrode pads may be formed on the another regions of the lower semiconductor layers of the light emitting cells before forming the insulation layer. The electrode pads are exposed by the opening portions formed on the another regions of the lower semiconductor layers. That is, the electrode pads are exposed while the opening portions are formed on the insulation layer to prevent the lower semiconductor layers from being exposed. Accordingly, damage of the lower semiconductor layers may be reduced while the opening portions are formed.

<24> Transparent electrode layers may be formed on the upper semiconductor layers of the light emitting cells before forming the insulation layer. The transparent electrode layers are exposed by the opening portions formed on the upper semiconductor layers. As the transparent electrode layers are formed on the upper semiconductor layers, the wires are in contact with the transparent electrode layers. Accordingly, materials of the wires may be chosen from more options.

<25> Forming the light emitting cells may include forming a lower semiconductor layer, an active layer and an upper semiconductor layer on an entire surface of the substrate. Photoresist patterns defining light emitting cell regions may be formed on the upper semiconductor layer. Then, reflow of the photoresist patterns may be performed so that side surfaces of the photoresist patterns can be inclined with respect to an upper surface of the substrate. Thereafter, the upper semiconductor layer, active layer and lower semiconductor layer may be sequentially etched using the photoresist patterns as an etching mask. Accordingly, the light emitting cell regions are separated to have inclined side surfaces.

<26> Reflow of the photoresist patterns may be performed so that inclination angles of the side surfaces of the photoresist patterns with respect to the upper surface of the substrate are in a range of 15 degrees to 80 degrees. Inclination angle of 80 degrees or less is required to form continuous insulation layer and wires, and inclination angle of 15 degrees or more is required to ensure a sufficient light emitting regions.

<27> Further, the upper semiconductor layer, the active layer and the lower semiconductor layer may be sequentially etched and then the upper semiconductor

layer and the active layer may be patterned again to expose the lower semiconductor layer. Alternatively, the upper semiconducting layer and the active layer may be patterned and then the upper semiconductor layer, the active layer and the lower semiconductor layer may be sequentially etched to expose the lower semiconductor layer.

<28> Forming the wires may include forming photoresist pattern including opening portions defining wire regions on the insulation layer. Then, a metal layer may be plated in the opening portions. Thereafter, the photoresist patterns may be removed to form the wires.

<29> Alternatively, forming the wires may include depositing a metal layer on the substrate on which the insulation layer is formed. Then the metal layer may be patterned to form the wires. As the side surfaces of the light emitting cells are inclined, the metal layer is continuously formed on the insulation layer. Accordingly, depositing the metal layer and forming the wires by patterning the metal layer may be easily performed. Further, the insulation layer covers the side surfaces of the light emitting cells, short circuit of the light emitting cells by the metal layer material may be prevented.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will become apparent from the following description of preferred embodiments given in conjunction with the accompanying drawings, in which:

<1> Fig. 1 is a plan view illustrating a light emitting diode for AC operation in a related art;

<2> Fig. 2 is a sectional view along line IV-IV of Fig. 1;

<3> Fig. 3 is a sectional view illustrating a light emitting diode for AC operation according to an exemplary embodiment of the present invention; and

<4> Figs. 4 to 9 are sectional views illustrating a process of manufacturing a light emitting diode according to the exemplary embodiment of the present invention.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

<30> Hereinafter, a light emitting diode for AC operation and a method of fabricating the same will be described in detail with reference to the accompanying drawings. However, the present disclosure is not limited to the exemplary embodiments set forth herein but can be implemented in different forms. Rather, the exemplary embodiments are merely provided to allow the present invention to be completely described herein and to fully convey the scope of the invention to those skilled in the art.

<31> Fig. 3 is a sectional view illustrating a light emitting diode for AC operation according to an exemplary embodiment of the present invention.

<32> Referring to Fig. 3, a plurality of light emitting cells 56 are disposed to be spaced apart in a substrate 51. The substrate 51 may be insulating or conducting one, and may be, for example, a sapphire or a silicon carbide (SiC) substrate.

<33> The light emitting cells 56 respectively include a lower semiconductor layer 55, an upper semiconductor layer 59 disposed on a region of the lower

semiconductor layer, and an active layer 57 disposed between the lower semiconductor layer and the upper semiconductor layer. The upper and the lower semiconductor layers may be n-type and p-type, respectively. Alternatively the upper and the lower semiconductor layers may be p-type and n-type, respectively.

<34> The lower semiconductor layer 55, active layer 57 and upper semiconductor layer 59 may include a gallium nitride-based semiconducting material, for example, (B, Al, In, Ga)N. Elements and stoichiometry of the active layer 57 may be determined so that a light having a desired wavelength, for example, ultraviolet ray or blue light, can be emitted. The lower semiconductor layer 55 and upper semiconductor layer 59 are formed of a material having a greater bandgap compared with the active layer 57.

<35> The lower semiconductor layer 55 and/or the upper semiconductor layer 59 may be, as illustrated, formed of a single layer or multiple layers. The active layer 57 may have a single-quantum-well structure or a multiple-quantum-well structure.

<36> A buffer layer 53 may be disposed between the light emitting cells 56 and the substrate 51. The buffer layer 53 is employed to reduce a lattice mismatch between the substrate 51 and the lower semiconductor layer 55 formed thereon. The buffer layer 53 may be continuous as illustrated, but it is not limited thereto. The buffer layer 53 may be disposed under the lower semiconductor layers 55 to be discontinuous.

<37> Side surfaces of the light emitting cells 56 are formed to be inclined with respect to an upper surface of the substrate 51 and get narrowed toward upside. The inclination of the side surfaces improves emission efficiency of a light produced in the active layer 57, and helps conformal deposition of other layers which will be formed on the light emitting cells 56. In the exemplary embodiment, the inclination angles of the side surfaces of the lower semiconductor layers 55 of the respective light emitting cells 56 may be in a range of 15 degrees to 80 degrees.

<38> An insulation layer 69 covers an entire surface of the light emitting cells 56. The insulation layer 69 include opening portions on another regions of the lower semiconductor layers 55, for example, a region adjacent to a region on which the upper semiconductor layer 59 is formed, and include opening portions on the upper semiconductor layers 59. The opening portions are space apart from each other, and therefore, the side surfaces of the light emitting cells 56 are covered with the insulation layer 69. The insulation layer 69 may cover the substrate 51 in regions between the light emitting cells 56, or the buffer layer 53. The insulation layer 69 may include a silicon oxide (SiO2) layer.

<39> Wires 71 are formed on the insulation layer 69. The wires 71 are electrically connected to the lower semiconductor layers 55 and the upper semiconductor layers 59 through the opening portions. In addition, the wires 71 respectively connect the lower semiconductor layers 55 and the upper semiconductor layers 59 of the adjacent light emitting cells 56 to form a series array of the light emitting cells 56. The array may be formed in plurality, and a plurality of arrays may be connected to be reverse parallel and connected to AC power to be driven. Further, a bridge rectifier (not shown) connected to the series array of the light emitting cells may be formed, and the light emitting cells may be driven with AC power by the bridge rectifier. The bridge rectifier may be formed by connecting light emitting cells having substantially the same structure as the light emitting cells using wires 71. The wires may be formed of a conductive material, for example, a doped semiconducting material such as polycrystalline silicon or a metal.

<40> Meanwhile, electrode pads may be disposed between the another regions of the lower semiconductors 55 and the insulation layer 69. The electrode pads 67 are exposed by the opening portions formed in the another regions of the lower semiconductor layers 55. The electrode pads 67 have ohmic contacts to the lower semiconductor layers 55. The wires 71 are in contact with the electrode pads 67 exposed by the opening portions to be electrically connected to the lower semiconductor layers 55.

<41> Transparent electrode layers 65 may be disposed between the upper semiconductor layers 59 and the insulation layers 69. The transparent electrode layers 65 are exposed by the opening portions formed on the upper semiconductor layers 59. The transparent electrode layers 65 transmit light produced in the active layer 57, and disperse and supply currents to the upper semiconductor layers 59. The wires 71 are in contact with the transparent electrode layers 65 exposed by the opening portions to be electrically connected to the upper semiconductor layers 55. Electrode pads (not shown) may be further formed on the transparent electrode layers 65 and the wires 71 may be in contact with the electrode pads.

<42> A protecting insulation layer 73 may cover the wires 71 and the insulation layer 69. The protecting insulation layer 73 substantially reduces contamination of the wires 71 from moisture and so forth, and damage of the wires 71 from external pressure. The protecting insulation layer 73 may be formed of a light-transmitting material, for example, silicon oxide layer.

<43> Figs. 4 to 9 are sectional views illustrating a process of manufacturing a light emitting diode according to the exemplary embodiment of the present invention.

<44> Referring to Fig. 4, a lower semiconductor layer 55, an active layer 57, and an upper semiconductor layer 59 are formed on a substrate 51. A buffer layer 53 may be formed on the substrate 51 before the lower semiconductor layer 55 is formed.

<45> The substrate 51 may be sapphire (Al2O3), silicon carbide (SiC), zinc oxide (ZnO), silicon (Si), gallium arsenide (GaAs), gallium phosphate (GaP), lithium-alumina (LiAl2O3), boron nitride (BN), aluminum nitride (AlN) or gallium nitride (GaN). However, it is not limited thereto and may be variable according to a semiconducting material which is to be formed on the substrate 51.

<46> The buffer layer 53 is formed to reduce lattice mismatch between the substrate 51 and the semiconductor layer 55 which is to be formed thereon. The buffer layer 53 may include, for example, gallium nitride (GaN) or aluminum nitride (AlN). When the substrate 51 is a conductive substrate, the buffer layer 53 may be formed of an insulation layer or a semi-insulation layer, for example, AlN or semi-insulating GaN.

<47> The lower semiconductor layer 55, active layer 57 and upper semiconductor layer 59 may include a gallium nitride-based semiconducting material, for example, (B, Al, In, Ga)N. The lower and upper semiconductor layers 55 and 59 and the active layer 57 may be formed continuously or discontinuously using, for example, metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy or hydride vapor phase epitaxy (HNPE) technology.

<48> The upper and the lower semiconductor layers may be n-type and p-type, respectively. Alternatively the upper and the lower semiconductor layers may be p-type and n-type, respectively. In the gallium nitride-based compound semiconductor layer, n-type semiconductor layer may be doped with, for example, silicon (Si), and p-type semiconductor layer may be doped with, for example, magnesium (Mg).

<49> Photoresist patterns 63 defining light emitting cell regions are formed on the upper semiconductor layer 59. The photoresist patterns are formed to cover the light emitting cell regions. Reflow of the photoresist patterns 63 is performed so that side surfaces can be inclined with respect to an upper surface of the substrate 51. The side surfaces of the photoresist patterns 63 may be formed to have an inclination angle in a range of 15 degree to 80 degree with respect to the upper surface of the substrate 51.

<50> Referring to Fig. 5, the upper semiconductor layer 59, the active layer 57 and the lower semiconductor layer 55 are sequentially etched using the photoresist patterns 63 as etching mask. Accordingly, the shape of the photoresist patterns 63 is reproduced in the semiconductor layers 59, 57 and 55 and the light emitting cells with inclined side surfaces are separated. The buffer layer 53 may be exposed and the exposed buffer layer 53 may be removed by over-etching.

<51> Thereafter, the photoresist patterns 63 are removed, and the upper semiconductor layer and the active layer are patterned again to expose the etched lower semiconductor layers 55. The exposed lower semiconductor layers may be partially etched by over-etching. Accordingly, light emitting cells 56 that are spaced apart are formed on the substrate 51. Each of the light emitting cells 56 includes the lower semiconductor layer 56 which is spaced apart by etching, the upper semiconductor layer 57 disposed on an upper side of a region of the lower semiconductor layer 56, and the active layer 57 disposed between the lower semiconductor layer 55 and the upper semiconductor layer 57. Another region of the lower semiconductor layer 56 is exposed. Further, most of the side surfaces of the light emitting cells 56 are formed to be inclined with respect to an upper surface of the substrate 51. Whereas, side surfaces of the upper semiconductor layers 59 adjacent to another regions of the lower semiconductor layers 55 may be formed to be inclined as illustrated, and alternatively, may be formed vertically.

<52> Referring to Fig. 6, a transparent electrode layer 65 may be formed on the upper semiconductor layer 59 of the light emitting cell 56. The transparent electrode layer 65 includes a transparent metal such as indium tin oxide (ITO) layer or Ni/Au. Further, electrode pads 67 may be formed on another regions of the lower semiconductor layers 55. The electrode pads 67 have an ohmic contact with the lower semiconductor layers 55.

<53> The transparent electrode layer 65 may be formed on the upper semiconductor layer 59 before the photoresist patterns are formed. The transparent electrode layer 65 is patterned together with the upper semiconductor layer.

<54> Referring to Fig. 7, a continuous insulation layer 69 is formed on an entire surface of the substrate 51 with the plurality of light emitting cells 56 formed thereon. The insulation layer 69 covers the side surfaces and top surfaces of the light emitting cells 56, and the top surfaces of the substrate 51 between the adjacent light emitting cells 56. For example, the insulation layer 69 may be formed as a silicone oxide film using a CVD (Chemical Vapor Deposition) technique.

<55> Since the side surfaces of the light emitting cells 56 are inclined, the insulation layer 69 can easily cover the side surfaces of the light emitting cells 56. Since the total thickness of the upper semiconductor layer 59 and active layer 57 is small and spaces between the upper semiconductor layers 59 are broad, the side surfaces of the upper semiconductor layers 59 adjacent to another regions of the lower semiconductor layers 55 can be easily covered with the insulation layer 69.

<56> Referring to Fig. 8, an opening portions are formed on another regions of the lower semiconductor layers 55 and the upper semiconductor layers 59 by

patterning the insulation layer 69. If the electrode pads 67 and the transparent electrode layers 65 are formed, the electrode pads 67 and the transparent electrode layers 65 are exposed through the opening portions.

<57> The opening portions may be formed using a photo and etching process, and the electrode pads 67 substantially reduce damage of the lower semiconductor layers 55 while the insulation layer 69 is etched.

<58> Referring to Fig. 9, wires 71 are formed on the insulation layer 69 with the opening portions. The wire 71 are electrically connected to the lower semiconductor layers 55 and the upper semiconductor layers 59 through the opening portions, and connect the lower semiconductor layers 55 and the upper semiconductor layers 59 of the adjacent light emitting cells 56 to form arrays connected in series.

<59> The wires 71 may be formed using a plating technique. That is, the wires 71 may be formed by forming a photoresist pattern having opening portions defining wire region on the insulation layer 69, plating a metal layer in the opening portions, and removing the photoresist pattern.

<60> Alternatively, the wires 71 may be formed using CVD (Chemical Vapor Deposition) or PVD (Physical Vapor Deposition) technique. That is, a metal layer is formed using a vapor deposition technique such as electron beam deposition and then patterned using a photo and etching process, so that the wires 71 can be formed. Since the insulation layer 69 covers the side surfaces of the light emitting cells 56, short-circuiting of the light emitting cells 56 due to a remaining metallic material after patterning of metal layer may be prevented.

<61> A protecting insulation layer 73 is formed on the substrate 51 with the wires 71 formed thereon. The protecting insulation layer 73 is formed of a light-transmitting material, for example, silicon oxide layer using chemical vapor deposition technique. In this way, a light emitting diode for AC operation shown in Fig. 1 is manufactured.

[Advantageous Effects]

<62> According to the exemplary embodiments, a reliable light emitting diode for AC operation can be provided by preventing disconnection or short circuit of wires by external pressure, and short circuit of a light emitting cell by a conductive material such as remaining metals while the wires are formed may be prevented. Further, the wires may be formed to be supported by insulation layers, so that a reliable light emitting diode for AC operation can be manufactured.

What is claimed is;

1. A light emitting diode for AC operation comprising:

light emitting cells spaced apart from each other on a substrate, each of which comprising a lower semiconductor layer, an upper semiconductor layer disposed on a region of the lower semiconductor layer, and an active layer disposed between the lower semiconductor layer and the upper semiconductor layer, wherein side surfaces are formed to be inclined with respect to an upper surface of the substrate and get narrowed toward upside;

an insulation layer which covers entire surface of the light emitting cells and includes opening portions respectively formed on another regions of the lower semiconductor layers and on the upper semiconductor layers; and

wires that are formed on the insulation layer, electrically connected to the lower semiconductor layers and the upper semiconductor layers through the opening portions, and electrically connect the lower semiconductor layers and the upper semiconductor layers of adjacent light emitting cells.

2. The light emitting diode for AC operation of claim 1, wherein the inclination angles of the side surfaces of the lower semiconductor layers of the respective light emitting cells are in a range of 15 degrees to 80 degrees.

3. The light emitting diode for AC operation of claim 1, further comprising electrode pads disposed between the another regions of the lower semiconductor regions and the insulation layer, wherein the electrode pads are exposed through the opening portions formed on the another portions of the lower semiconductor layers.

4. The light emitting diode for AC operation of claim 3, further comprising transparent electrode layers disposed between the upper semiconductor layers and the insulation layer, wherein the transparent electrode layers are exposed through the opening portions formed on the upper semiconductor layers.

5. The light emitting diode for AC operation of claim 1, further comprising a protecting insulation layer covering the wires and the insulation layer.

6. A method of manufacturing a light emitting diode for AC operation, comprising:

forming light emitting cells spaced apart from each other on a substrate, wherein the light emitting cells comprises a lower semiconductor layer, an upper semiconductor layer disposed on a region of the lower semiconductor layer, and an active layer disposed between the lower semiconductor layer and the upper semiconductor layer, and wherein side surfaces are formed to be inclined with respect to an upper surface of the substrate and get narrowed toward upside;

forming a continuous insulation layer on the substrate on which the light emitting cells are formed;

patterning the insulation layer and forming opening portions on another regions of the lower semiconductor layers and on the upper semiconductor layers; and

forming wires on the insulation layer, wherein the wires are electrically connected to the lower semiconductor layers and the upper semiconductor layers through the opening portions, and electrically connect the lower semiconductor layers and the upper semiconductor layers of adjacent light emitting cells.

7. The method of manufacturing a light emitting diode for AC operation of claim 6,

further comprising forming electrode pads on the another regions of the lower semiconductor layers of the light emitting cells before forming the insulation layer, wherein the electrode pads are exposed by the opening portions formed on the another regions of the lower semiconductor layers.

8. The method of manufacturing a light emitting diode for AC operation of claim 7, further comprising forming transparent electrode layers on the upper semiconductor layers of the light emitting cells before forming the insulation layer, wherein the transparent electrode layers are exposed by the opening portions formed on the upper semiconductor layers.

9. The method of manufacturing a light emitting diode for AC operation of claim 6, wherein forming the light emitting cells comprises:

forming the lower semiconductor layer, active layer and upper semiconductor layer on the entire surface of the substrate;

forming photoresist patterns defining the light emitting cell regions on the upper semiconductor layer;

performing reflow of the photoresist patterns so that side surfaces of the photoresist patterns can be inclined with respect to an upper surface of the substrate; and

sequentially etching the upper semiconductor layer, active layer and lower semiconductor layer using the photoresist patterns as an etching mask.

10. The method of manufacturing a light emitting diode for AC operation of claim 9, wherein the reflow of the photoresist patterns is performed so that inclination angles of the side surfaces of the photoresist patterns with respect to the upper surface of the substrate are in a range of 15 degrees to 80 degrees.

11. The method of manufacturing a light emitting diode for AC operation of claim 9, further comprising patterning again the upper semiconducting layer and the active layer to expose the lower semiconductor layer after sequentially etching the upper semiconductor layer, active layer and lower semiconductor layer.

12. The method of manufacturing a light emitting diode for AC operation of claim 6, wherein forming the wires comprises:

forming photoresist pattern including opening portions defining wire regions on the insulation layer;

plating a metal layer in the opening portions; and

removing the photoresist patterns.

13. The method of manufacturing a light emitting diode for AC operation of claim 6, wherein forming the wires comprises:

depositing a metal layer on the substrate on which the insulation layer is formed; and

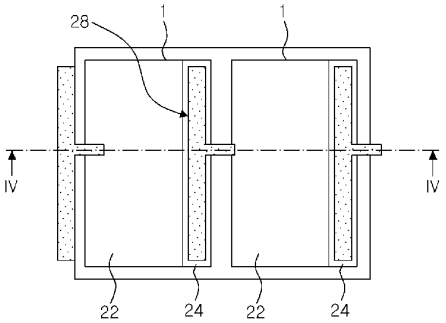
patterning the metal layer.

ABSTRACT

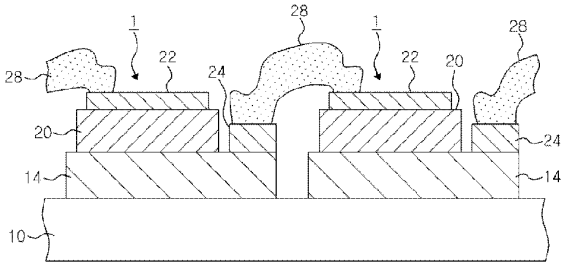
A light emitting diode for AC operation with wires and a method of fabricating the same are provided. The light emitting diode includes light emitting cells spaced apart from each other on a substrate. Each of the light emitting cells includes a lower semiconductor layer, an upper semiconductor layer disposed on a region of the lower semiconductor layer, and an active layer disposed between the lower semiconductor layer and the upper semiconductor layer. Further, side surfaces of the light emitting cells are formed to be inclined with respect to an upper surface of the substrate and get narrowed toward upside. An insulation layer covers entire surface of the light emitting cells. The insulation layer includes opening portions respectively formed on another regions of the lower semiconductor layers and on the upper semiconductor layers. Wires are formed on the insulation layer and electrically connected to the lower semiconductor layers and the upper semiconductor layers through the opening portions. The wires electrically connect the lower semiconductor layers and the upper semiconductor layers of adjacent light emitting cells. Accordingly, the wires are formed on the insulation layer and disconnection and short circuit of the wires may be prevented, so that a reliable light emitting diode for AC operation can be provided.

DRAWINGS

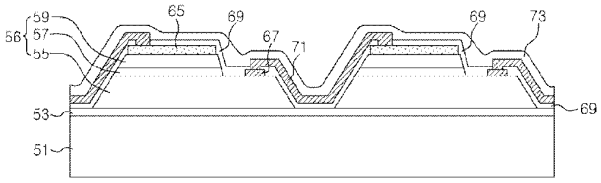
[Figure 1]



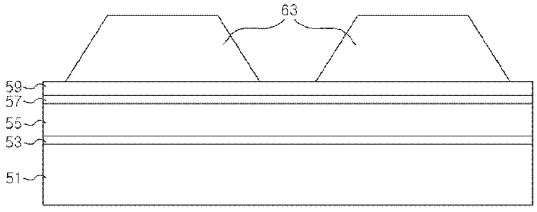
[Figure 2]



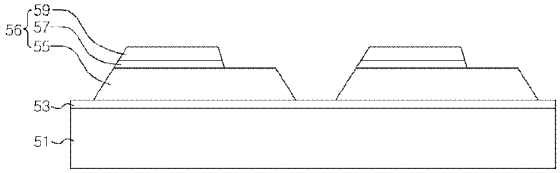
[Figure 3]



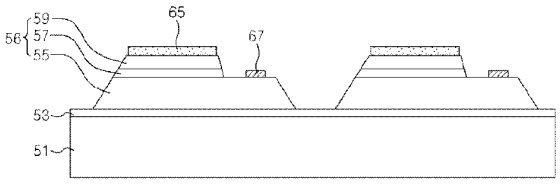
[Figure 4]



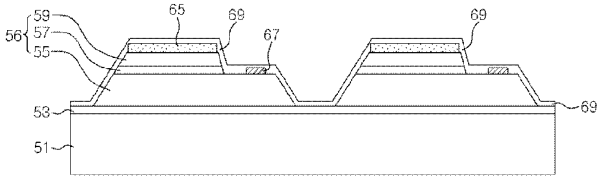
[Figure 5]



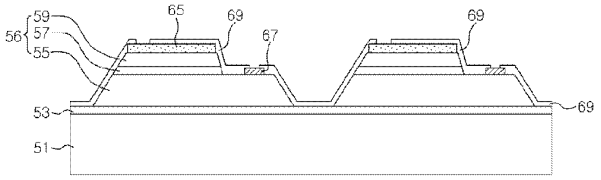
[Figure 6]



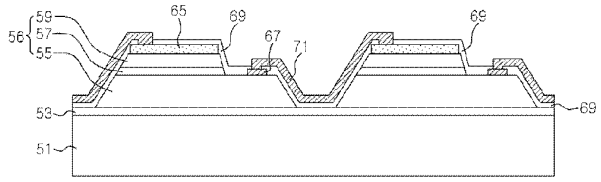
[Figure 7]



[Figure 8]



[Figure 9]



REMARKS

Claims 5 and 6 have been canceled without prejudice or disclaimer. The specification and drawings have been amended to include inadvertently omitted material from priority documents KR10-2005-0053797, KR10-2005-55179, and KR10-2006-0021801, which were incorporated by reference in their entirety per the Preliminary Amendment filed December 26, 2007.

Claims 7-16 have been previously withdrawn.

Accordingly, claims 1-4 are pending in this application, of which claim 1 is independent.

Applicants respectfully submit that the amendments do not add new matter to the application.

Amendments to the Specification

New paragraphs [0036], [0037], and [0128] through [0159] have been added to include material that was inadvertently omitted from the original specification. Support for new paragraphs [0036], [0037], and [0128] through [0159] is found respectively in paragraphs [0003], [0004], and [0031] through [0061] in priority document KR10-2006-0021801. A certified English translation of this Korean priority document is included herewith.

Paragraphs [0021], [0049] through [0053], [0062], [0063], [0073], [0099], [0100], [0114], and [0115] have been amended to include "μm" in the substitute specification. Support for these amendments is found in priority documents KR10-2005-0053797 and KR10-2005-0055179. Specifically, support for paragraphs [0021], [0049] through [0053], [0062], [0063], [0073] may be found respectively in paragraphs [0026], [0042] through [0046], [0056], [0057], and [0069] in priority document KR10-2005-0053797. Support for paragraphs [0099], [0100], [0114], and [0115] may respectively be found in paragraphs [0042], [0043], [0061], and [0062] in

priority document KR10-2005-0055179. Certified English translations of these Korean priority documents are included herewith.

Amendments to the Drawings

Please add new drawings 32 through 38 as shown in the attached New Drawing Sheets. New drawings 32 through 38, which were inadvertently omitted from the filed application, correspond to drawings 3 through 9 in the priority document KR10-2006-0021801.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,

/hae-chan park/

Hae-Chan Park
Reg. No. 50,114

Date: September 18, 2009

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Facsimile: 703-288-5139
HCP/BCR/kbs

Attachments: (1) Substitute Specification, marked-up copy
(2) Substitute Specification, clean copy
(3) New Drawing Sheets (3)

PTO/SB/06 (07-06)
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Application or Docket Number	Filing Date	☐ To be Mailed
11/993,965	12/26/2007	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	09/18/2009	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 14	Minus	** 20	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

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Legal Instrument Examiner:
/PEGGY YARBOROUGH/

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Application Number	11993965
Filing Date	2007-12-26
First Named Inventor	Jong Lam LEE
Art Unit	2818
Examiner Name	NGUYEN, Thinh T.
Attorney Docket Number	P2317US00

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	2	7474681		2009-01-06	Lin, et al.	
	3	7271421		2007-09-18	Yukimoto, et al.	
	4	7034340		2006-04-25	Yukimoto	
	5	7525248		2009-04-28	Fan	
	6	6635902		2003-10-21	Lin	
	7	7511311		2009-03-31	Kususe, et al.	
	8	7213942		2007-05-08	Jiang, et al.	

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	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, Thinh T.
	Attorney Docket Number	P2317US00

	9	7221044		2007-05-22	Fan, et al.	
	10	7210819		2007-05-01	Jiang, et al.	
	11	6957899		2005-10-25	Jiang, et al.	
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	2	20050224973		2005-10-13	Bernier, et al.	
	3	20050199885		2005-09-15	Hata, et al.	
	4	20060169993		2006-08-03	Fan, et al.	
	5	20050225973		2005-10-13	Eliashevich, et al.	

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	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, Thinh T.
	Attorney Docket Number	P2317US00

	6	20080230765		2008-09-25	Yoon, et al.	
	7	20060043433		2003-03-02	Matsushita	

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	1	11-150303	JP		1999-06-02	Takeuchi		☐

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	Art Unit	2818
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Name/Print	Hae-Chan Park	Registration Number	50114

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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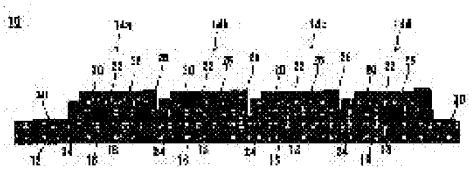
(11)Publication number : **11-150303**
(43)Date of publication of application : **02.06.1999**

(51)Int.Cl. H01L 33/00
H01S 3/18

(21)Application number : **09-331083**
(22)Date of filing : **14.11.1997**

(71)Applicant : **SANYO ELECTRIC CO LTD**
(72)Inventor : **TAKEUCHI KUNIO**

(54) **LIGHT EMITTING PARTS**



(57)Abstract:
PROBLEM TO BE SOLVED: To obtain light emitting parts which are formed as single parts and can be used suitably as a surface light source having a high luminous intensity.
SOLUTION: An n-type GaN layer 16, a light emitting layer 18, and a p-type GaN contact layer 20 are successively formed on an insulating substrate 12 in this order correspondingly to GaN light emitting diodes 14a-14d. A light transmissive electrode 22 which is a p-type side electrode is formed on the contact layer 20 in a planar form, and an n-type side electrode 24 is formed on the GaN layer 16 in such a state that the electrode 24 is extended in the widthwise direction from the vicinity of one edge of the layer 16. The members on the substrate 12 are covered with a protective film 26 and the light transmissive electrode 22 of each light emitting diode is connected in series with the p-type side electrodes 24 of its adjacent electrodes through internal wiring 28 having a width. Then pad electrodes 30 which are respectively connected to external parts are connected to the light transmissive electrode 22 of the diode at one end and the p-type side electrode 24 of the diode at the other end. Thus the light emitting parts in which the GaN light emitting diodes 14a-14d are connected in series on one insulating substrate 12 is obtained.

* NOTICES *

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1]A light-emitting component provided with two or more 3 fellows nitride semiconductor light emitting elements which are formed on a substrate and said substrate, respectively, and are connected.
[Claim 2]The light-emitting component according to claim 1 to which said two or more 3 fellows nitride semiconductor light emitting elements are connected in series.
[Claim 3]A semiconductor layer of the 1st conductivity type with which said three fellows each nitride semiconductor light emitting element is formed on said substrate, The 1st conductivity-type lateral electrode formed [crosswise near the one end rim] on a semiconductor layer of said 1st conductivity type by extending, The 2nd conductivity-type lateral electrode formed at surface state on a semiconductor layer of the 2nd conductivity type formed on said semiconductor layer of the 1st conductivity and a semiconductor layer of said 2nd conductivity type is included, The light-emitting component according to claim 1 or 2 to which said 1st conductivity-type lateral electrode of one light emitting device of said 3 fellows nitride semiconductor light emitting element which said three fellows each nitride semiconductor light emitting element is arranged by linear shape, and adjoins mutually, and said 2nd conductivity-type lateral electrode of a light emitting device of another side are connected by internal wiring which has width.
[Claim 4]The light-emitting component according to claim 3 which will be set as R1**R2 in resistance of a semiconductor layer of said 1st conductivity type if resistance of R1 and said 2nd conductivity-type lateral electrode is set to R2.
[Claim 5]The light-emitting component according to claim 3 or 4 in which said 2nd conductivity-type lateral electrode contains a translucency electrode.
[Claim 6]The light-emitting component according to any one of claims 1 to 5 in which the number of said 3 fellows nitride semiconductor light emitting elements is determined according to driver voltage.
[Claim 7]The light-emitting component according to any one of claims 1 to 6 in which said 3 fellows nitride semiconductor light emitting element contains a GaN system light emitting device.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]Especially this invention relates to the light-emitting component for example, using 3 fellows nitride semiconductor light emitting element about a light-emitting component.
[0002]
[Description of the Prior Art]As shown in drawing 9, as the conventional GaN system light emitting device 1, That is [on the one insulating substrate 2, the pad electrode for the bonding of the couple which consists of the one translucency electrode 3, and the anode electrode 4 and the cathode terminal 5 was formed], the light emitting diode which has one light-emitting part to one chip has been used widely.
[0003]
[Problem(s) to be Solved by the Invention]since the conventional GaN system light emitting device 1 has a light-emitting part only in one place -- it -- if independent, as the surface light source, it was not suitable.
[0004]Since only one element is formed on the one insulating substrate 2 in the GaN system light emitting device 1, Since two or more GaN system light emitting devices 1 needed to be arranged on the base and it needed to connect mutually when it was going to acquire the surface light source of the large area, the interval of the GaN system light emitting device 1 which adjoins mutually had a limit, and there was a problem that the surface light source which has big luminescence intensity could not be acquired.
[0005]So, the main purpose of this invention is to provide the light-emitting component which is suitable as the surface light source which is formed as single parts and has big luminescence intensity.
[0006]
[Means for Solving the Problem]To achieve the above objects, the light-emitting component according to claim 1 is provided with two or more 3 fellows nitride semiconductor light emitting elements which are formed on a substrate and a substrate, respectively, and are connected.
[0007]As for two or more 3 fellows nitride semiconductor light emitting elements, the light-emitting component according to claim 2 is connected in series in the light-emitting component according to claim 1.
[0008]In the light-emitting component according to claim 1 or 2, the light-emitting component according to claim 3 a three fellows each nitride semiconductor light emitting

element, The 1st conductivity-type lateral electrode formed [crosswise near the one end rim] on a semiconductor layer of the 1st conductivity type formed on a substrate, and a semiconductor layer of the 1st conductivity type by extending, The 2nd conductivity-type lateral electrode formed at surface state on a semiconductor layer of the 2nd conductivity type formed on a semiconductor layer of the 1st conductivity and a semiconductor layer of the 2nd conductivity type is included, The 1st conductivity-type lateral electrode of one light emitting device of 3 fellows nitride semiconductor light emitting element which a three fellows each nitride semiconductor light emitting element is arranged by linear shape, and adjoins mutually, and the 2nd conductivity-type lateral electrode of a light emitting device of another side are connected by internal wiring which has width.

[0009]In the light-emitting component according to claim 3, resistance of a semiconductor layer of the 1st conductivity type will be set as R1**R2, if the light-emitting component according to claim 4 sets resistance of R1 and the 2nd conductivity-type lateral electrode to R2.

[0010]In the light-emitting component according to claim 3 or 4, as for the light-emitting component according to claim 5, the 2nd conductivity-type lateral electrode contains a translucency electrode.

[0011]As for the light-emitting component according to claim 6, in the light-emitting component according to any one of claims 1 to 5, the number of 3 fellows nitride semiconductor light emitting elements is determined according to driver voltage.

[0012]In the light-emitting component according to any one of claims 1 to 6, as for the light-emitting component according to claim 7, 3 fellows nitride semiconductor light emitting element contains a GaN system light emitting device.

[0013]In the light-emitting component according to claim 1, since two or more 3 fellows nitride semiconductor light emitting elements are formed and connected on one substrate using general IC manufacturing process, an interval of 3 fellows nitride semiconductor light emitting element which adjoins mutually can be made narrower than before. Therefore, it is formed as single parts and the surface light source with large luminescence intensity is acquired.

[0014]If two or more 3 fellows nitride semiconductor light emitting elements are connected in series so that it may indicate to claim 2, light quantity from a three fellows each nitride semiconductor light emitting element will be made equal.

[0015]A three fellows each nitride semiconductor light emitting element is arranged by linear shape so that it may indicate to claim 3, And connection of the 1st conductivity-type lateral electrode of one light emitting device of 3 fellows nitride semiconductor light emitting element which adjoins mutually, and the 2nd conductivity-type lateral electrode of a light emitting device of another side of internal wiring which has width will equalize more luminous intensity distributions in each 3 fellows nitride semiconductor light emitting element. If set as ** (resistance R1 of a semiconductor layer of the 1st conductivity type) (resistance R2 of the 2nd conductivity-type lateral electrode) indicate to claim 4, luminous intensity distributions in each 3 fellows nitride semiconductor light emitting element will be abbreviated-equalized.

[0016]If the number of 3 fellows nitride semiconductor light emitting elements is set up suit driver voltage of a device with which a light-emitting component is used so that it may indicate to claim 6, a light-emitting component applicable to various driver voltages will be obtained. The 2nd conductivity-type lateral electrode is formed of a translucency

electrode, and as a 3 fellows nitride semiconductor light emitting element, for example, a GaN system light emitting device is used so that it may indicate to claim 7, so that it may indicate to claim 5.
[0017]
[Embodiment of the Invention]Hereafter, this embodiment of the invention is described with reference to drawings.
[0018]With reference to drawing 1 and drawing 2, as for the light-emitting component 10 of this embodiment of the invention, the four GaN (semiconductor which contains Ga and N at least) system light emitting diodes 14a-14d are formed on the insulating substrate 12, for example including the insulating substrates 12, such as silicon-on-sapphire Hitoshi.
[0019]Namely, on the insulating substrate 12, it corresponds to each GaN system light emitting diodes 14a-14d, The n type GaN layer (Si dope) 16 used as the electrode installation layer of 3.0 micrometers of thickness, the luminous layer 18 of 0.1 micrometer of thickness, and the p type GaN contact layer (Mg dope) 20 of 0.5 micrometer of thickness are formed in this order.
[0020]On each p type GaN contact layer 20, the translucency electrode 22 which is a p type lateral electrode is formed at surface state, and, [crosswise near the one end rim] on each n type GaN layer 16, the n type lateral electrode 24 is formed. The translucency electrode 22 and the n type lateral electrode 24 are formed in parallel so that drawing 1 may show well.
[0021]And each member on the insulating substrate 12 is covered with the protective film 26, and the series connection of the translucency electrode 22 and the n type lateral electrode 24 between adjoining GaN system light emitting diodes is carried out with the internal wiring 28 which has the predetermined width W1. At this time, the end of the internal wiring 28 is extended and formed [crosswise near the one end rim] on the translucency electrode 22. Therefore, concerning one GaN system light emitting diode, in the connected part of the internal wiring 28 and the translucency electrode 22, the formation point of the n type lateral electrode 24 becomes near the edge of an opposite hand. The size of the width W1 of the internal wiring 28 is set up become for it to be a little smaller than the width W2 of the translucency electrode 22, and a little larger than length L of the n type lateral electrode 24 for example, so that drawing 1 may show.
[0022]The pad electrode 30 for connecting with external parts, respectively is connected to the translucency electrode 22 and the n type lateral electrode 24 of both ends. The pad electrode 30 as well as the internal electrode 28 is formed.
[0023]Thus, the light-emitting component 10 which carried out the series connection of the four GaN system light emitting diodes 14a-14d is obtained by connecting the translucency electrode 22 and the n type lateral electrode 24 via the internal wiring 28. The equivalent circuit of the light-emitting component 10 is shown in drawing 3.
[0024]An example of such a manufacturing method of the light-emitting component 10 is explained with reference to drawing 4.
[0025]First, as shown in drawing 4 (a), the n type GaN layer 16, the luminous layer 18, and the p type GaN contact layer 20 are grown epitaxially in this order by MOCVD (organometal chemistry vapor phase growth) on the insulating substrate 12, The p type GaN contact layer 20 of 3.0 micrometers of thickness, the n type GaN layer 16 of $N_D=10^{18}cm^{-3}$, the luminous layer 18 of 0.1 micrometer of thickness and 0.5 micrometer of thickness, and $N_A=10^{17}cm^{-3}$ is formed.

[0026]As shown in drawing 4 (b), by subsequently, the dry etching method which supplies photo lithography and gaseous chlorine with nickel mask by the pressure of 0.5 Pa. Etching removal of the p type GaN contact layer 20, the luminous layer 18, and the n type GaN layer 16 on the insulating substrate 12 is carried out, and the mesa 21 is formed. The depth of etching at this time is 0.8 micrometer.
[0027]As shown in drawing 4 (c), by the dry etching method which supplies photo lithography and gaseous chlorine with nickel mask by the pressure of 0.5 Pa, etching removal of the n type GaN layer 16 on the insulating substrate 12 is carried out, and the crevice 32 is formed so that the insulating substrate 12 may be exposed. The depth of etching is set to 3.6 micrometers and the layer which constitutes the GaN system light emitting diodes 14a-14d is separated by this, respectively.
[0028]As it continues and is shown in drawing 4 (d), by the electron beam evaporation by the pressure of $2x10^{-6}$torr. The Ni film of 2 nm of thickness and the Au membrane of 4 nm of thickness are formed in this order at the whole p type GaN contact layer 20 upper surface, and the translucency electrode 22 of surface state is formed of photo lithography. By the electron beam evaporation by the pressure of $2x10^{-6}$torr. On the n type GaN layer 16, the Ti film of 30 nm of thickness and the Al film of 500 nm of thickness are formed in this order, and the n type lateral electrode 24 prolonged by photo lithography [crosswise near the one end rim] on the n type GaN layer 16 is formed. The n type lateral electrode 24 is equivalent to the cathode terminal of a GaN system light emitting diode.
[0029]Then, as shown in drawing 4 (e), the protective film 26 which becomes the whole upper surface of the chip formed by drawing 4 (d) from SiO_2 of 300 nm of thickness is formed of electron beam evaporation.
[0030]Then, etching removal of the protective film 26 is carried out by photo lithography, and an opening is carried out so that a part of each upper surface of the translucency electrode 22 and the n type lateral electrode 24 may be exposed. Concerning one GaN system light emitting diode at this time, the opening on the translucency electrode 22 is extended and formed [of an opposite hand / crosswise near the edge] with the formation point of the n type lateral electrode 24. The opening of the n type lateral electrode 24 is also prolonged crosswise, and is formed.
[0031]And as shown in drawing 4 (f), the Ni film of 100 nm of thickness and the Au membrane of 700 nm of thickness are formed in this order by the electron beam evaporation by the pressure of $2x10^{-6}$torr at the whole upper surface of the protective film 26, and the internal wiring 28 is formed of photo lithography. Therefore, concerning one GaN system light emitting diode, the internal wiring 28 connected to the internal wiring 28 and the n type lateral electrode 24 which are connected to the translucency electrode 22 will be pulled out by the counter direction from the both ends of a GaN system light emitting diode, respectively. Although not illustrated to drawing 4 (f), the pad electrode 30 is formed simultaneously similarly. The end part connected with the translucency electrode 22 among the internal wiring 28 and the pad electrode 30 is equivalent to the anode electrode of a GaN system light emitting diode.
[0032]Thus, the light-emitting component 10 in which the series connection of the four GaN system light emitting diodes 14a-14d was carried out is formed.
[0033]Since two or more GaN system light emitting diodes 14a-14d are formed and connected on the insulating substrate 12 of one sheet using general IC manufacturing

process according to the luminescence intensity 10, the interval of the GaN system light emitting diode which adjoins mutually can be made narrower than before. Therefore, the light-emitting component 10 which is formed as single parts and is suitable as the surface light source with large luminescence intensity is obtained.
[0034]Since according to the light-emitting component 10 the GaN system light emitting diodes 14a-14d can be formed on the insulating substrate 12 at linear shape as shown in drawing 5 (a), luminescence of a large area is obtained so that drawing 5 (b) may show.
[0035]Since the GaN system light emitting diodes 14a-14d can be formed on the same insulating substrate 12, the insulated separation for GaN system light emitting diode 14a-14d and integration become easy.
[0036]Each GaN system light emitting diodes [14a-14d] luminous intensity distributions come to be shown in drawing 6. Setting resistance of Rt and the n type GaN layer 16 to Rn for resistance of the translucency electrode 22, Rp shows a part for resistance of the p type GaN contact layer 20, the contact resistance of the translucency electrode 22 and the p type GaN contact layer 20, and p-n junction phase-voltages this resistance, and each resistance presupposes it that it is thought in a field that it is fixed.
[0037]Since the n type lateral electrode 24 of one light emitting diode of the GaN system light emitting diode which each GaN system light emitting diodes 14a-14d are arranged by linear shape, and adjoins mutually, and the translucency electrode 22 of the light emitting diode of another side are connected by the internal wiring 28 which has the width W1, When resistance per unit area of the translucency electrode 22 is small (Rt**Rn), as shown in drawing 6 (a), current flows into the n type GaN layer 16 from the translucency electrode 22 whole surface, and the current which passes the luminous layer 18 becomes uniform irrespective of the position in the luminous layer 18. Therefore, as shown in drawing 6 (b) and (c), luminescence from the translucency electrode 22 becomes abbreviated homogeneity irrespective of a luminescence part, and bigger luminescence intensity is obtained.
[0038]Incidentally, when resistance per unit area of the translucency electrode 22 is strong (Rt>Rn), as shown in drawing 6 (d), the current which passes the luminous layer 18 is concentrated on the internal wiring 28, i.e., anode electrode vicinity. In this case, although the luminescence intensity in the X-X section shown in drawing 6 (e) becomes uneven, Since the n type lateral electrode 24 of one light emitting diode of the GaN system light emitting diode which each GaN system light emitting diodes 14a-14d are arranged by linear shape, and adjoins mutually, and the translucency electrode 22 of the light emitting diode of another side are connected by the internal wiring 28 which has the width W1, The luminescence intensity in the Y-Y section shown in drawing 6 (f) becomes abbreviated homogeneity. Therefore, from the case where resistance per unit area of the translucency electrode 22 mentioned above is small, luminescence intensity is equalized from unevenness and the conventional technology shown in drawing 9 at least, and luminescence intensity becomes large, although it becomes small.
[0039]As shown in drawing 7 (a) - (c), the GaN system light emitting diodes 14a-14d may be formed on the insulating substrate 12a, a series connection may be carried out to a U shape, and the light-emitting component which it is formed as single parts also in this case, and big luminescence intensity is obtained, and is suitable as the surface light source is obtained.
[0040]That is, the light-emitting component which it is formed as single parts, and big

luminescence intensity is obtained, and can be applied to the surface light source is obtained by forming and carrying out the series connection of two or more GaN system light emitting diodes on an insulating substrate so that drawing 5 and drawing 7 may show.

[0041]In order to drive a GaN system light emitting diode, it is [more than 3V] required, and circuit operation is performed using 5V power supply in many cases. When 4V grade needs per GaN system light emitting diode (for example, when sending 20-mA current), and driver voltage is 24V, six GaN system light emitting diodes should just use the light-emitting component by which the series connection was carried out. Thus, by using the GaN system light emitting diode of the number of series elements according to driver voltage, luminescence of a large area is attained, and restriction of driver voltage also decreases, and the application covered in many fields can be expected.

[0042]As shown in drawing 8, current control elements, such as resistance (drawing 8 (a)) and FET (drawing 8 (b)), may be formed on the same insulating substrate with the GaN system light emitting diodes 14a-14n, In this case, the GaN system light emitting diodes 14a-14n and a current control element can be formed on the same insulating substrate at a monolithic.

[0043]Thus, since an external element becomes unnecessary, the small and lightweight light-emitting component 10 is obtained and not only the GaN system light emitting diodes 14a-14d but a current control element can be formed with a wide gap band material, The strong light-emitting component 10 is obtained to generation of heat, and integration becomes easy. Since an element is constituted only in the one side principal surface of an insulating substrate, general IC manufacturing process also in this case is applicable. Restriction of driver voltage decreases further by it not only adjusting the number of GaN system light emitting diodes, but adding a current control element. The surge current at the time of an assembly and use can be controlled by adding resistance to the GaN system light emitting diodes 14a-14n.

[0044]Although the embodiment of drawing 1 described the case where the series connection of the four GaN system light emitting diodes 14a-14d was carried out, it cannot be overemphasized that the number of GaN system light emitting diodes is not limited to this.

[0045]In an above-mentioned embodiment, although the light emitting diode was explained to the example as a light emitting device, it may not be limited to this but may be laser.

[0046]As a 3 fellows nitride semiconductor light emitting element of the light-emitting component 10, if it is a light emitting device which consists of a 3 fellows nitride semiconductor which contains AlN, InN, BN, or InGaN, for example, arbitrary 3 fellows nitride semiconductor light emitting elements can be used.

[0047]

[Effect of the Invention]According to this invention, two or more light-emitting parts can be formed on one substrate, and the light-emitting component which it is formed as single parts, and big luminescence intensity is obtained, and is suitable as the surface light source is obtained.

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TECHNICAL FIELD

[Field of the Invention]Especially this invention relates to the light-emitting component for example, using 3 fellows nitride semiconductor light emitting element about a light-emitting component.

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PRIOR ART

[Description of the Prior Art]As shown in drawing 9, as the conventional GaN system light emitting device 1, That is [on the one insulating substrate 2, the pad electrode for the bonding of the couple which consists of the one translucency electrode 3, and the anode electrode 4 and the cathode terminal 5 was formed], the light emitting diode which has one light-emitting part to one chip has been used widely.

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EFFECT OF THE INVENTION

[Effect of the Invention]According to this invention, two or more light-emitting parts can be formed on one substrate, and the light-emitting component which it is formed as single parts, and big luminescence intensity is obtained, and is suitable as the surface light source is obtained.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]since the conventional GaN system light emitting device 1 has a light-emitting part only in one place -- it -- if independent, as the surface light source, it was not suitable.
[0004]Since only one element is formed on the one insulating substrate 2 in the GaN system light emitting device 1, Since two or more GaN system light emitting devices 1 needed to be arranged on the base and it needed to connect mutually when it was going to acquire the surface light source of the large area, the interval of the GaN system light emitting device 1 which adjoins mutually had a limit, and there was a problem that the surface light source which has big luminescence intensity could not be acquired.
[0005]So, the main purpose of this invention is to provide the light-emitting component which is suitable as the surface light source which is formed as single parts and has big luminescence intensity.

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MEANS

[Means for Solving the Problem]To achieve the above objects, the light-emitting component according to claim 1 is provided with two or more 3 fellows nitride semiconductor light emitting elements which are formed on a substrate and a substrate, respectively, and are connected.
[0007]As for two or more 3 fellows nitride semiconductor light emitting elements, the light-emitting component according to claim 2 is connected in series in the light-emitting component according to claim 1.
[0008]In the light-emitting component according to claim 1 or 2, the light-emitting component according to claim 3 a three fellows each nitride semiconductor light emitting element, The 1st conductivity-type lateral electrode formed [crosswise near the one end rim] on a semiconductor layer of the 1st conductivity type formed on a substrate, and a semiconductor layer of the 1st conductivity type by extending, The 2nd conductivity-type lateral electrode formed at surface state on a semiconductor layer of the 2nd conductivity type formed on a semiconductor layer of the 1st conductivity and a semiconductor layer of the 2nd conductivity type is included, The 1st conductivity-type lateral electrode of one light emitting device of 3 fellows nitride semiconductor light emitting element which a three fellows each nitride semiconductor light emitting element is arranged by linear shape, and adjoins mutually, and the 2nd conductivity-type lateral electrode of a light emitting device of another side are connected by internal wiring which has width.
[0009]In the light-emitting component according to claim 3, resistance of a semiconductor layer of the 1st conductivity type will be set as R1**R2, if the light-emitting component according to claim 4 sets resistance of R1 and the 2nd conductivity-type lateral electrode to R2.
[0010]In the light-emitting component according to claim 3 or 4, as for the light-emitting component according to claim 5, the 2nd conductivity-type lateral electrode contains a translucency electrode.
[0011]As for the light-emitting component according to claim 6, in the light-emitting component according to any one of claims 1 to 5, the number of 3 fellows nitride semiconductor light emitting elements is determined according to driver voltage.
[0012]In the light-emitting component according to any one of claims 1 to 6, as for the light-emitting component according to claim 7, 3 fellows nitride semiconductor light emitting element contains a GaN system light emitting device.
[0013]In the light-emitting component according to claim 1, since two or more 3 fellows nitride semiconductor light emitting elements are formed and connected on one substrate

using general IC manufacturing process, an interval of 3 fellows nitride semiconductor light emitting element which adjoins mutually can be made narrower than before. Therefore, it is formed as single parts and the surface light source with large luminescence intensity is acquired.
[0014]If two or more 3 fellows nitride semiconductor light emitting elements are connected in series so that it may indicate to claim 2, light quantity from a three fellows each nitride semiconductor light emitting element will be made equal.
[0015]A three fellows each nitride semiconductor light emitting element is arranged by linear shape so that it may indicate to claim 3, And connection of the 1st conductivity-type lateral electrode of one light emitting device of 3 fellows nitride semiconductor light emitting element which adjoins mutually, and the 2nd conductivity-type lateral electrode of a light emitting device of another side of internal wiring which has width will equalize more luminous intensity distributions in each 3 fellows nitride semiconductor light emitting element. If set as ** (resistance R1 of a semiconductor layer of the 1st conductivity type) (resistance R2 of the 2nd conductivity-type lateral electrode) indicate to claim 4, luminous intensity distributions in each 3 fellows nitride semiconductor light emitting element will be abbreviated-equalized.
[0016]If the number of 3 fellows nitride semiconductor light emitting elements is set up suit driver voltage of a device with which a light-emitting component is used so that it may indicate to claim 6, a light-emitting component applicable to various driver voltages will be obtained. The 2nd conductivity-type lateral electrode is formed of a translucency electrode, and as a 3 fellows nitride semiconductor light emitting element, for example, a GaN system light emitting device is used so that it may indicate to claim 7, so that it may indicate to claim 5.
[0017]
[Embodiment of the Invention]Hereafter, this embodiment of the invention is described with reference to drawings.
[0018]With reference to drawing 1 and drawing 2, as for the light-emitting component 10 of this embodiment of the invention, the four GaN (semiconductor which contains Ga and N at least) system light emitting diodes 14a-14d are formed on the insulating substrate 12, for example including the insulating substrates 12, such as silicon-on-sapphire Hitoshi.
[0019]Namely, on the insulating substrate 12, it corresponds to each GaN system light emitting diodes 14a-14d, The n type GaN layer (Si dope) 16 used as the electrode installation layer of 3.0 micrometers of thickness, the luminous layer 18 of 0.1 micrometer of thickness, and the p type GaN contact layer (Mg dope) 20 of 0.5 micrometer of thickness are formed in this order.
[0020]On each p type GaN contact layer 20, the translucency electrode 22 which is a p type lateral electrode is formed at surface state, and, [crosswise near the one end rim] on each n type GaN layer 16, the n type lateral electrode 24 is formed. The translucency electrode 22 and the n type lateral electrode 24 are formed in parallel so that drawing 1 may show well.
[0021]And each member on the insulating substrate 12 is covered with the protective film 26, and the series connection of the translucency electrode 22 and the n type lateral electrode 24 between adjoining GaN system light emitting diodes is carried out with the internal wiring 28 which has the predetermined width W1. At this time, the end of the internal wiring 28 is extended and formed [crosswise near the one end rim] on the

translucency electrode 22. Therefore, concerning one GaN system light emitting diode, in the connected part of the internal wiring 28 and the translucency electrode 22, the formation point of the n type lateral electrode 24 becomes near the edge of an opposite hand. The size of the width W1 of the internal wiring 28 is set up become for it to be a little smaller than the width W2 of the translucency electrode 22, and a little larger than length L of the n type lateral electrode 24 for example, so that drawing 1 may show.
[0022]The pad electrode 30 for connecting with external parts, respectively is connected to the translucency electrode 22 and the n type lateral electrode 24 of both ends. The pad electrode 30 as well as the internal electrode 28 is formed.
[0023]Thus, the light-emitting component 10 which carried out the series connection of the four GaN system light emitting diodes 14a-14d is obtained by connecting the translucency electrode 22 and the n type lateral electrode 24 via the internal wiring 28. The equivalent circuit of the light-emitting component 10 is shown in drawing 3.
[0024]An example of such a manufacturing method of the light-emitting component 10 is explained with reference to drawing 4.
[0025]First, as shown in drawing 4 (a), the n type GaN layer 16, the luminous layer 18, and the p type GaN contact layer 20 are grown epitaxially in this order by MOCVD (organometal chemistry vapor phase growth) on the insulating substrate 12, The p type GaN contact layer 20 of 3.0 micrometers of thickness, the n type GaN layer 16 of $N_D=10^{18}cm^{-3}$, the luminous layer 18 of 0.1 micrometer of thickness and 0.5 micrometer of thickness, and $N_A=10^{17}cm^{-3}$ is formed.
[0026]As shown in drawing 4 (b), by subsequently, the dry etching method which supplies photo lithography and gaseous chlorine with nickel mask by the pressure of 0.5 Pa. Etching removal of the p type GaN contact layer 20, the luminous layer 18, and the n type GaN layer 16 on the insulating substrate 12 is carried out, and the mesa 21 is formed. The depth of etching at this time is 0.8 micrometer.
[0027]As shown in drawing 4 (c), by the dry etching method which supplies photo lithography and gaseous chlorine with nickel mask by the pressure of 0.5 Pa, etching removal of the n type GaN layer 16 on the insulating substrate 12 is carried out, and the crevice 32 is formed so that the insulating substrate 12 may be exposed. The depth of etching is set to 3.6 micrometers and the layer which constitutes the GaN system light emitting diodes 14a-14d is separated by this, respectively.
[0028]As it continues and is shown in drawing 4 (d), by the electron beam evaporation by the pressure of $2x10^{-6}$torr. The Ni film of 2 nm of thickness and the Au membrane of 4 nm of thickness are formed in this order at the whole p type GaN contact layer 20 upper surface, and the translucency electrode 22 of surface state is formed of photo lithography. By the electron beam evaporation by the pressure of $2x10^{-6}$torr. On the n type GaN layer 16, the Ti film of 30 nm of thickness and the Al film of 500 nm of thickness are formed in this order, and the n type lateral electrode 24 prolonged by photo lithography [crosswise near the one end rim] on the n type GaN layer 16 is formed. The n type lateral electrode 24 is equivalent to the cathode terminal of a GaN system light emitting diode.
[0029]Then, as shown in drawing 4 (e), the protective film 26 which becomes the whole upper surface of the chip formed by drawing 4 (d) from SiO_2 of 300 nm of thickness is formed of electron beam evaporation.
[0030]Then, etching removal of the protective film 26 is carried out by photo lithography,

and an opening is carried out so that a part of each upper surface of the translucency electrode 22 and the n type lateral electrode 24 may be exposed. Concerning one GaN system light emitting diode at this time, the opening on the translucency electrode 22 is extended and formed [of an opposite hand / crosswise near the edge] with the formation point of the n type lateral electrode 24. The opening of the n type lateral electrode 24 is also prolonged crosswise, and is formed.

[0031]And as shown in drawing 4 (f), the Ni film of 100 nm of thickness and the Au membrane of 700 nm of thickness are formed in this order by the electron beam evaporation by the pressure of $2x10^{-6}$torr at the whole upper surface of the protective film 26, and the internal wiring 28 is formed of photo lithography. Therefore, concerning one GaN system light emitting diode, the internal wiring 28 connected to the internal wiring 28 and the n type lateral electrode 24 which are connected to the translucency electrode 22 will be pulled out by the counter direction from the both ends of a GaN system light emitting diode, respectively. Although not illustrated to drawing 4 (f), the pad electrode 30 is formed simultaneously similarly. The end part connected with the translucency electrode 22 among the internal wiring 28 and the pad electrode 30 is equivalent to the anode electrode of a GaN system light emitting diode.

[0032]Thus, the light-emitting component 10 in which the series connection of the four GaN system light emitting diodes 14a-14d was carried out is formed.

[0033]Since two or more GaN system light emitting diodes 14a-14d are formed and connected on the insulating substrate 12 of one sheet using general IC manufacturing process according to the luminescence intensity 10, the interval of the GaN system light emitting diode which adjoins mutually can be made narrower than before. Therefore, the light-emitting component 10 which is formed as single parts and is suitable as the surface light source with large luminescence intensity is obtained.

[0034]Since according to the light-emitting component 10 the GaN system light emitting diodes 14a-14d can be formed on the insulating substrate 12 at linear shape as shown in drawing 5 (a), luminescence of a large area is obtained so that drawing 5 (b) may show.

[0035]Since the GaN system light emitting diodes 14a-14d can be formed on the same insulating substrate 12, the insulated separation for GaN system light emitting diode 14a-14d and integration become easy.

[0036]Each GaN system light emitting diodes [14a-14d] luminous intensity distributions come to be shown in drawing 6. Setting resistance of Rt and the n type GaN layer 16 to Rn for resistance of the translucency electrode 22, Rp shows a part for resistance of the p type GaN contact layer 20, the contact resistance of the translucency electrode 22 and the p type GaN contact layer 20, and p-n junction phase-voltages this resistance, and each resistance presupposes it that it is thought in a field that it is fixed.

[0037]Since the n type lateral electrode 24 of one light emitting diode of the GaN system light emitting diode which each GaN system light emitting diodes 14a-14d are arranged by linear shape, and adjoins mutually, and the translucency electrode 22 of the light emitting diode of another side are connected by the internal wiring 28 which has the width W1, When resistance per unit area of the translucency electrode 22 is small (Rt**Rn), as shown in drawing 6 (a), current flows into the n type GaN layer 16 from the translucency electrode 22 whole surface, and the current which passes the luminous layer 18 becomes uniform irrespective of the position in the luminous layer 18. Therefore, as shown in drawing 6 (b) and (c), luminescence from the translucency electrode 22

becomes abbreviated homogeneity irrespective of a luminescence part, and bigger luminescence intensity is obtained.

[0038]Incidentally, when resistance per unit area of the translucency electrode 22 is strong (Rt>Rn), as shown in drawing 6 (d), the current which passes the luminous layer 18 is concentrated on the internal wiring 28, i.e., anode electrode vicinity. In this case, although the luminescence intensity in the X-X section shown in drawing 6 (e) becomes uneven, Since the n type lateral electrode 24 of one light emitting diode of the GaN system light emitting diode which each GaN system light emitting diodes 14a-14d are arranged by linear shape, and adjoins mutually, and the translucency electrode 22 of the light emitting diode of another side are connected by the internal wiring 28 which has the width W1, The luminescence intensity in the Y-Y section shown in drawing 6 (f) becomes abbreviated homogeneity. Therefore, from the case where resistance per unit area of the translucency electrode 22 mentioned above is small, luminescence intensity is equalized from unevenness and the conventional technology shown in drawing 9 at least, and luminescence intensity becomes large, although it becomes small.

[0039]As shown in drawing 7 (a) - (c), the GaN system light emitting diodes 14a-14d may be formed on the insulating substrate 12a, a series connection may be carried out to a U shape, and the light-emitting component which it is formed as single parts also in this case, and big luminescence intensity is obtained, and is suitable as the surface light source is obtained.

[0040]That is, the light-emitting component which it is formed as single parts, and big luminescence intensity is obtained, and can be applied to the surface light source is obtained by forming and carrying out the series connection of two or more GaN system light emitting diodes on an insulating substrate so that drawing 5 and drawing 7 may show.

[0041]In order to drive a GaN system light emitting diode, it is [more than 3V] required, and circuit operation is performed using 5V power supply in many cases. When 4V grade needs per GaN system light emitting diode (for example, when sending 20-mA current), and driver voltage is 24V, six GaN system light emitting diodes should just use the light-emitting component by which the series connection was carried out. Thus, by using the GaN system light emitting diode of the number of series elements according to driver voltage, luminescence of a large area is attained, and restriction of driver voltage also decreases, and the application covered in many fields can be expected.

[0042]As shown in drawing 8, current control elements, such as resistance (drawing 8 (a)) and FET (drawing 8 (b)), may be formed on the same insulating substrate with the GaN system light emitting diodes 14a-14n, In this case, the GaN system light emitting diodes 14a-14n and a current control element can be formed on the same insulating substrate at a monolithic.

[0043]Thus, since an external element becomes unnecessary, the small and lightweight light-emitting component 10 is obtained and not only the GaN system light emitting diodes 14a-14d but a current control element can be formed with a wide gap band material, The strong light-emitting component 10 is obtained to generation of heat, and integration becomes easy. Since an element is constituted only in the one side principal surface of an insulating substrate, general IC manufacturing process also in this case is applicable. Restriction of driver voltage decreases further by it not only adjusting the number of GaN system light emitting diodes, but adding a current control element. The

surge current at the time of an assembly and use can be controlled by adding resistance to the GaN system light emitting diodes 14a-14n.
[0044]Although the embodiment of drawing 1 described the case where the series connection of the four GaN system light emitting diodes 14a-14d was carried out, it cannot be overemphasized that the number of GaN system light emitting diodes is not limited to this.
[0045]In an above-mentioned embodiment, although the light emitting diode was explained to the example as a light emitting device, it may not be limited to this but may be laser.
[0046]As a 3 fellows nitride semiconductor light emitting element of the light-emitting component 10, if it is a light emitting device which consists of a 3 fellows nitride semiconductor which contains AlN, InN, BN, or InGaN, for example, arbitrary 3 fellows nitride semiconductor light emitting elements can be used.

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3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a top view showing the principal part of one embodiment of this invention.
[Drawing 2]It is a sectional view showing the embodiment of drawing 1.
[Drawing 3]It is a representative circuit schematic showing the embodiment of drawing 1.
[Drawing 4]It is process drawing showing the manufacturing process of the embodiment of drawing 1.
[Drawing 5](a) is a top view showing typically the arrangement state of the GaN system light emitting diode in the embodiment of drawing 1, and (b) is a side view showing the luminescent state typically.
[Drawing 6]It is an illustration figure showing the flow of the current of a GaN system light emitting diode, and the outline of luminous intensity distributions, and as for (d) - (f), (a) - (c) shows the case where resistance of a translucency electrode is strong, respectively, when resistance of a translucency electrode is small.
[Drawing 7](a) is a representative circuit schematic showing other embodiments of this invention, (b) is a top view showing typically the arrangement state of the GaN system light emitting diode in that embodiment, and (c) is a side view showing that luminescent state typically.
[Drawing 8]It is a representative circuit schematic showing the embodiment of others of this invention, and that by which (a) added resistance to the GaN system light emitting diode, and (b) show, respectively what added FET to the GaN system light emitting diode.
[Drawing 9](a) is a top view showing conventional technology, and (b) is the end elevation.
[Description of Notations]
10 Light-emitting component
12 12a Insulating substrate
14a-14d, 14n GaN system light emitting diode
16 N type GaN buffer layer
18 Luminous layer
20 P type GaN contact layer
22 Translucency electrode
24 N type lateral electrode
26 Protective film
28 Internal wiring
30 Pad electrode
W1 Width of internal wiring

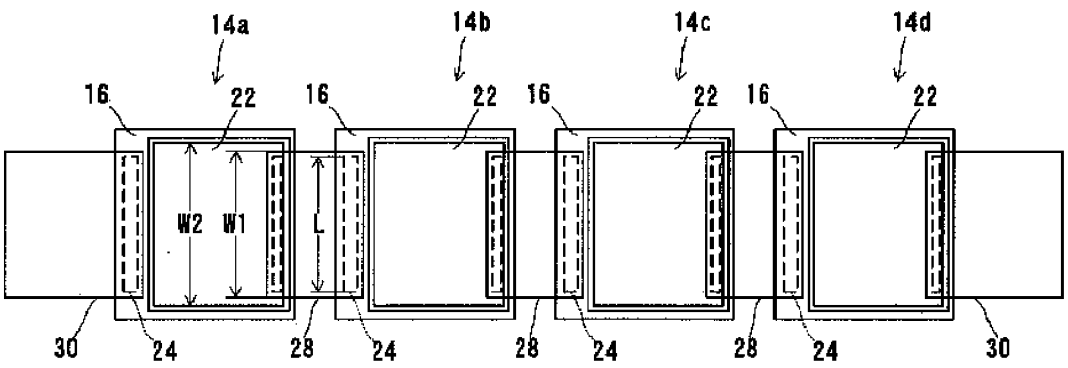
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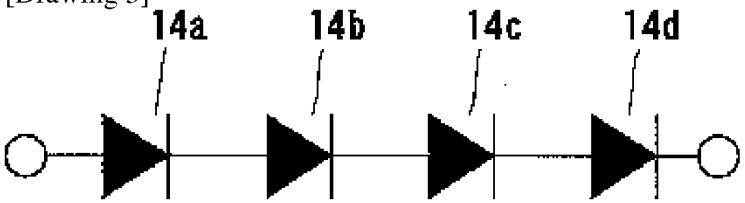
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DRAWINGS

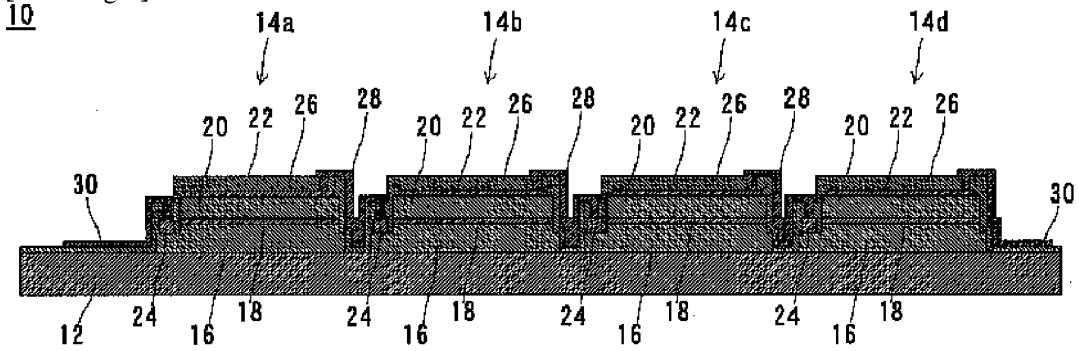
[Drawing 1]



[Drawing 3]

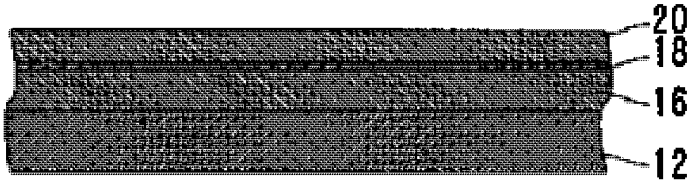


[Drawing 2]

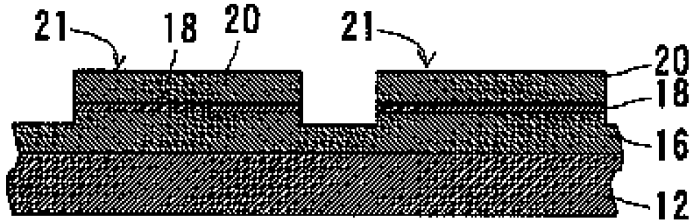


[Drawing 4]

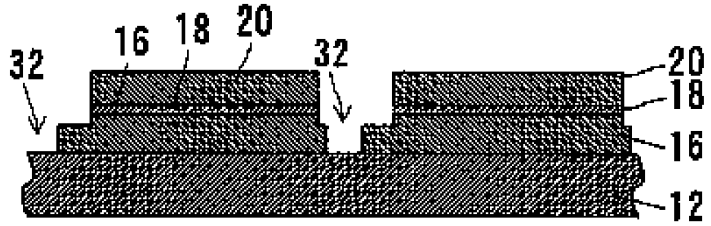
(a)


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16
12

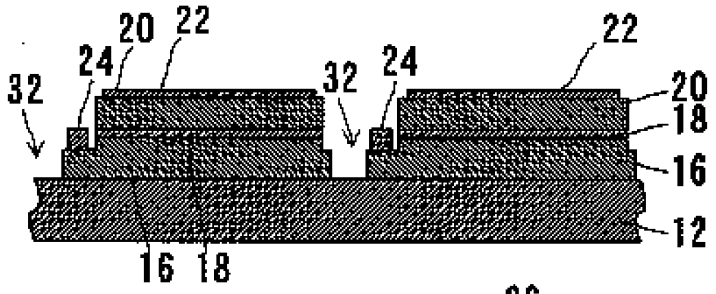
(b)


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21
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12

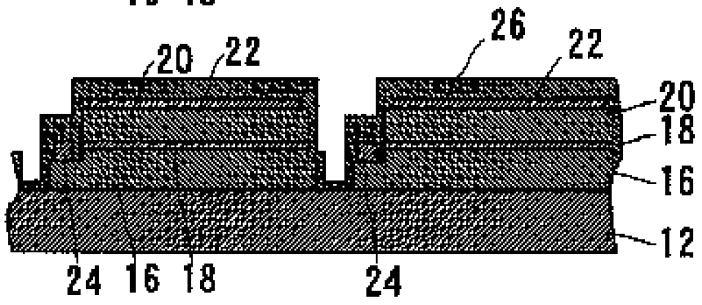
(c)


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12

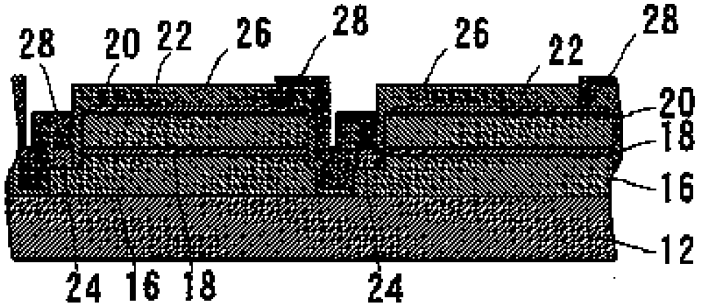
(d)


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22
24
32
24
22
32
20
18
16
12
16
18

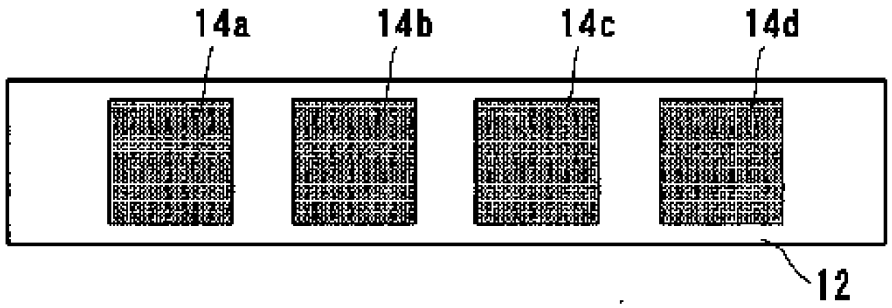
(e)


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24

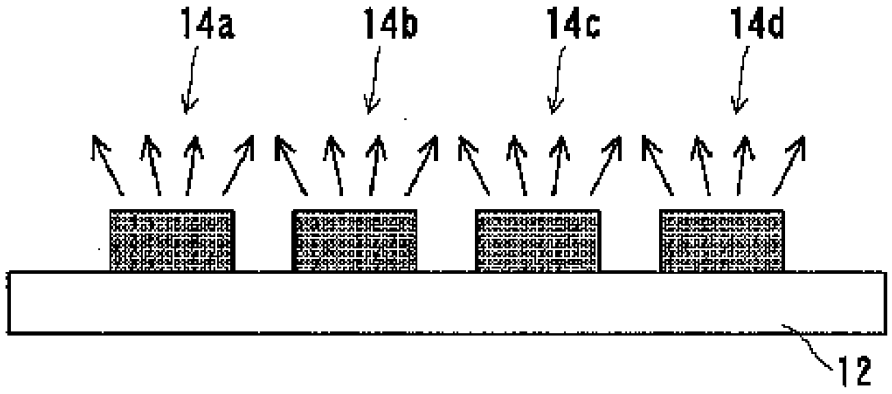
(f)


28
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16
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24

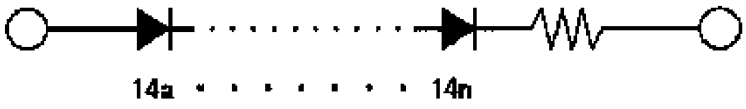
[Drawing 5]
(a)



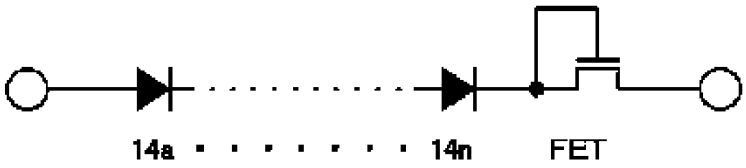
(b)



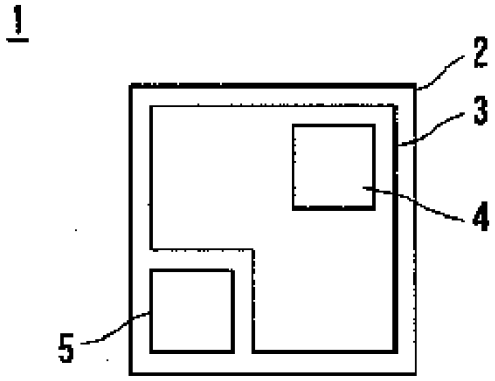
[Drawing 8]
(a)



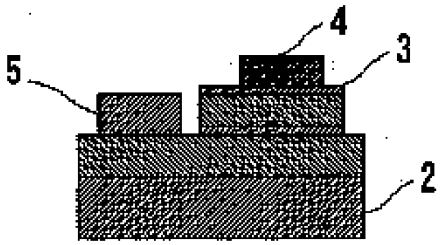
(b)



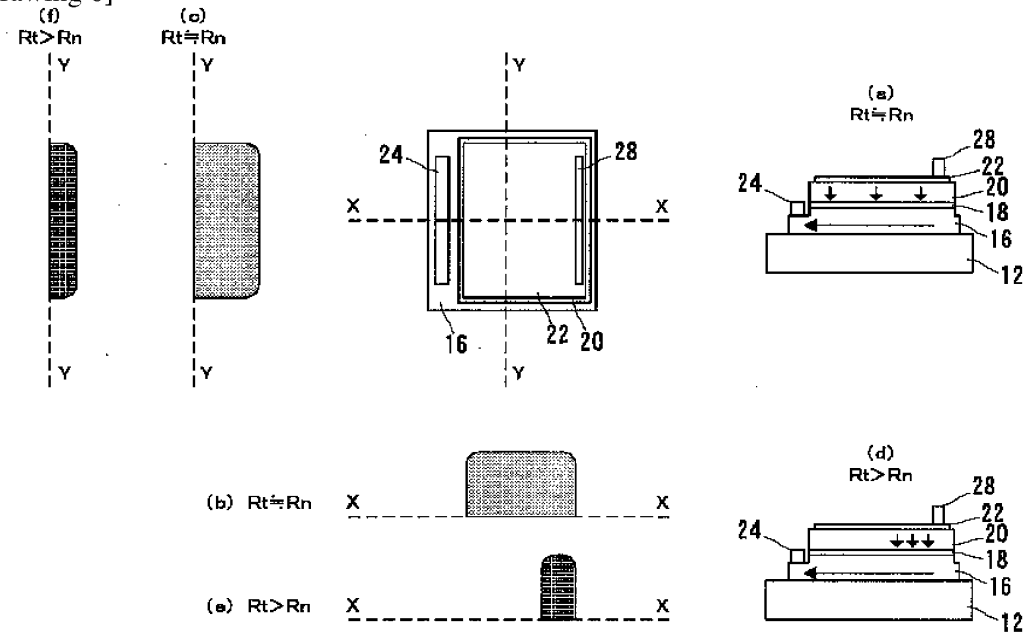
[Drawing 9]
(a)



(b)

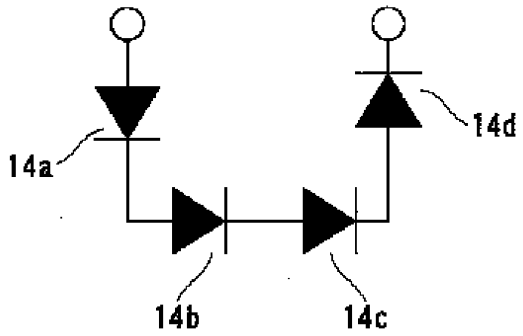


[Drawing 6]

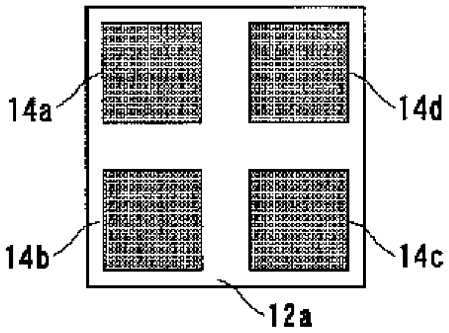

(f)
Rt>Rn
(c)
Rt≒Rn
Y
Y
Y
Y
Y
24
28
X
X
16
22
20
(a)
Rt≒Rn
28
22
20
18
16
12
24
(b) Rt≒Rn
X
X
(e) Rt>Rn
X
X
(d)
Rt>Rn
28
22
20
18
16
12
24

[Drawing 7]

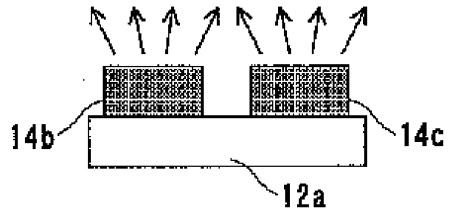
(a)



(b)



(c)



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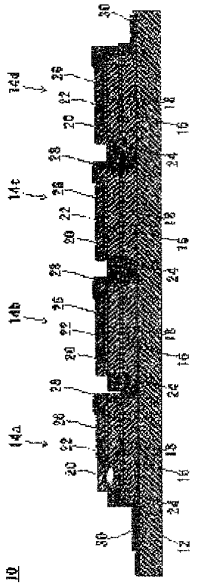
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(54)【発明の名称】　発光部品

(57)【要約】

【課題】　単一の部品として形成されかつ大きな発光強度を有する面光源として適する発光部品を得る。

【解決手段】　絶縁性基板１２上に、各ＧａＮ系発光ダイオード１４ａ～１４ｄに対応して、ｎ型ＧａＮ層１６、発光層１８およびｐ型ＧａＮコンタクト層２０を、この順序で形成する。ｐ型ＧａＮコンタクト層２０上にはｐ型側電極である透光性電極２２を面状に形成し、ｎ型ＧａＮ層１６上の一端縁近傍かつ幅方向に延びてｎ型側電極２４を形成する。絶縁性基板１２上の各部材を保護膜２６で覆い、隣接するＧａＮ系発光ダイオード間の透光性電極２２とｎ型側電極２４とを幅を有する内部配線２８で直列接続し、両端の透光性電極２２およびｎ型側電極２４には、それぞれ外部の部品と接続するためのパッド電極３０を接続する。このようにして、１枚の絶縁性基板１２上に複数のＧａＮ系発光ダイオード１４ａ～１４ｄを直列接続した発光部品１０を得る。



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【特許請求の範囲】

【請求項１】　基板、および前記基板上にそれぞれ形成されかつ接続される複数の３族窒化物半導体発光素子を備える、発光部品。

【請求項２】　前記複数の３族窒化物半導体発光素子は直列に接続される、請求項１に記載の発光部品。

【請求項３】　前記各３族窒化物半導体発光素子は、前記基板上に形成される第１導電型の半導体層、前記第１導電型の半導体層上の一端縁近傍かつ幅方向に延びて形成される第１導電型側電極、前記第１導電性の半導体層上に形成される第２導電型の半導体層、および前記第２導電型の半導体層上に面状に形成される第２導電型側電極を含み、

前記各３族窒化物半導体発光素子は直線状に配列され、かつ相互に隣接する前記３族窒化物半導体発光素子の一方の発光素子の前記第１導電型側電極と他方の発光素子の前記第２導電型側電極とは幅を有する内部配線によって接続される、請求項１または２に記載の発光部品。

【請求項４】　前記第１導電型の半導体層の抵抗をＲ１、前記第２導電型側電極の抵抗をＲ２とすると、Ｒ１≒Ｒ２に設定される、請求項３に記載の発光部品。

【請求項５】　前記第２導電型側電極は透光性電極を含む、請求項３または４に記載の発光部品。

【請求項６】　前記３族窒化物半導体発光素子の数は駆動電圧に応じて決定される、請求項１ないし５のいずれかに記載の発光部品。

【請求項７】　前記３族窒化物半導体発光素子はＧａＮ系発光素子を含む、請求項１ないし６のいずれかに記載の発光部品。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】この発明は発光部品に関し、特にたとえば３族窒化物半導体発光素子を用いる発光部品に関する。

【０００２】

【従来の技術】図９に示すように、従来のＧａＮ系発光素子１としては、１つの絶縁性基板２上に、１つの透光性電極３、およびアノード電極４とカソード電極５とからなる一対のボンディング用のパッド電極が形成された、すなわち１つのチップに対して１ヶ所の発光部を有する、発光ダイオードが広く用いられてきた。

【０００３】

【発明が解決しようとする課題】従来のＧａＮ系発光素子１は発光部を１ヶ所しか有さないので、それ単独では面光源としては適さなかった。

【０００４】また、ＧａＮ系発光素子１では１つの絶縁性基板２上に１つの素子しか形成されないため、大面積の面光源を得ようとすると、複数のＧａＮ系発光素子１を基体上に配列して互いに接続する必要があるので相互に隣接するＧａＮ系発光素子１の間隔に限界があり、大きな発光強度を有する面光源を得られないという問題点があった。

2

【０００５】それゆえにこの発明の主たる目的は、単一の部品として形成されかつ大きな発光強度を有する面光源として適する、発光部品を提供することである。

【０００６】

【課題を解決するための手段】上記目的を達成するために、請求項１に記載の発光部品は、基板、および基板上にそれぞれ形成されかつ接続される複数の３族窒化物半導体発光素子を備える。

【０００７】請求項２に記載の発光部品は、請求項１に記載の発光部品において、複数の３族窒化物半導体発光素子は直列に接続されるものである。

【０００８】請求項３に記載の発光部品は、請求項１または２に記載の発光部品において、各３族窒化物半導体発光素子は、基板上に形成される第１導電型の半導体層、第１導電型の半導体層上の一端縁近傍かつ幅方向に延びて形成される第１導電型側電極、第１導電性の半導体層上に形成される第２導電型の半導体層、および第２導電型の半導体層上に面状に形成される第２導電型側電極を含み、各３族窒化物半導体発光素子は直線状に配列され、かつ相互に隣接する３族窒化物半導体発光素子の一方の発光素子の第１導電型側電極と他方の発光素子の第２導電型側電極とは幅を有する内部配線によって接続されるものである。

【０００９】請求項４に記載の発光部品は、請求項３に記載の発光部品において、第１導電型の半導体層の抵抗をＲ１、第２導電型側電極の抵抗をＲ２とすると、Ｒ１≒Ｒ２に設定されるものである。

【００１０】請求項５に記載の発光部品は、請求項３または４に記載の発光部品において、第２導電型側電極は透光性電極を含むものである。

【００１１】請求項６に記載の発光部品は、請求項１ないし５のいずれかに記載の発光部品において、３族窒化物半導体発光素子の数は駆動電圧に応じて決定されるものである。

【００１２】請求項７に記載の発光部品は、請求項１ないし６のいずれかに記載の発光部品において、３族窒化物半導体発光素子はＧａＮ系発光素子を含むものである。

【００１３】請求項１に記載の発光部品では、一般のＩＣ製造プロセスを用いて１枚の基板上に複数の３族窒化物半導体発光素子が形成されかつ接続されるので、相互に隣接する３族窒化物半導体発光素子の間隔を従来よりも狭くできる。したがって、単一の部品として形成されかつ発光強度が大きい面光源が得られる。

【００１４】請求項２に記載するように、複数の３族窒化物半導体発光素子が直列に接続されると、各３族窒化物半導体発光素子からの発光量が等しくされる。

【００１５】請求項３に記載するように、各３族窒化物

半導体発光素子は直線状に配列され，かつ相互に隣接する３族窒化物半導体発光素子の一方の発光素子の第１導電型側電極と他方の発光素子の第２導電型側電極とが幅を有する内部配線によって接続されると、個々の３族窒化物半導体発光素子における発光強度分布はより均一化される。請求項４に記載するように，（第１導電型の半導体層の抵抗Ｒ１）≒（第２導電型側電極の抵抗Ｒ２）に設定されると，個々の３族窒化物半導体発光素子における発光強度分布は略均一化される。

【００１６】また，請求項６に記載するように，３族窒化物半導体発光素子の数が，発光部品が用いられる装置の駆動電圧に適合するように設定されると、さまざまな駆動電圧に適用可能な発光部品が得られる。なお，請求項５に記載するように，第２導電型側電極は透光性電極によって形成され，請求項７に記載するように，３族窒化物半導体発光素子としてはたとえばＧａＮ系発光素子が用いられる。

【００１７】

【発明の実施の形態】以下，この発明の実施の形態について，図面を参照して説明する。

【００１８】図１および図２を参照して，この発明の実施の形態の発光部品１０は，たとえばサファイア基板等などの絶縁性基板１２を含み，絶縁性基板１２上に４個のＧａＮ（少なくともＧａ，Ｎを含む半導体）系発光ダイオード１４ａ～１４ｄが形成されるものである。

【００１９】すなわち、絶縁性基板１２上には，各ＧａＮ系発光ダイオード１４ａ～１４ｄに対応して，層厚３．０μｍの電極設置層となるｎ型ＧａＮ層（Ｓｉドープ）１６，層厚０．１μｍの発光層１８，および層厚０．５μｍのｐ型ＧａＮコンタクト層（Ｍｇドープ）２０が，この順序で形成される。

【００２０】また，各ｐ型ＧａＮコンタクト層２０上にはｐ型側電極である透光性電極２２が面状に形成され，各ｎ型ＧａＮ層１６上の一端縁近傍かつ幅方向にはｎ型側電極２４が形成される。図１からよくわかるように，透光性電極２２とｎ型側電極２４とは平行に形成される。

【００２１】そして，絶縁性基板１２上の各部材は保護膜２６によって覆われ，隣接するＧａＮ系発光ダイオード間の透光性電極２２とｎ型側電極２４とは所定の幅Ｗ１を有する内部配線２８によって直列接続される。このとき，内部配線２８の一端は透光性電極２２上の一端縁近傍かつ幅方向に延びて形成される。したがって，１つのＧａＮ系発光ダイオードに関していえば、内部配線２８と透光性電極２２との接続箇所は，ｎ型側電極２４の形成箇所とは反対側の端縁近傍となる。なお，図１からわかるように，内部配線２８の幅Ｗ１の寸法は，たとえば，透光性電極２２の幅Ｗ２よりやや小さくかつｎ型側電極２４の長さＬよりやや大きくなるように設定される。

【００２２】さらに，両端の透光性電極２２およびｎ型側電極２４には，それぞれ外部の部品と接続するためのパッド電極３０が接続される。パッド電極３０も内部電極２８と同様に形成される。

【００２３】このように，内部配線２８を介して透光性電極２２とｎ型側電極２４とを接続することによって、４個のＧａＮ系発光ダイオード１４ａ～１４ｄを直列接続した発光部品１０が得られる。発光部品１０の等価回路が図３に示される。

【００２４】このような発光部品１０の製造方法の一例を，図４を参照して説明する。

【００２５】まず，図４（ａ）に示すように，絶縁性基板１２上に，ｎ型ＧａＮ層１６，発光層１８およびｐ型ＧａＮコンタクト層２０をＭＯＣＶＤ（有機金属化学気相成長法）によってこの順序でエピタキシャル成長させ，膜厚３．０μｍ，$N_D = 10^{18}cm^{-3}$のｎ型ＧａＮ層１６，膜厚０．１μｍの発光層１８，および膜厚０．５μｍ，$N_A = 10^{18}cm^{-3}$のｐ型ＧａＮコンタクト層２０が形成される。

【００２６】ついで，図４（ｂ）に示すように，N_2マスクによるフォトリソグラフィーおよび塩素ガスを０．５Ｐａの圧力で供給するドライエッチング法によって，絶縁性基板１２上のｐ型ＧａＮコンタクト層２０，発光層１８およびｎ型ＧａＮ層１６がエッチング除去され，メサ２１が形成される。このときのエッチングの深さは０．８μｍである。

【００２７】さらに，図４（ｃ）に示すように，N_2マスクによるフォトリソグラフィーおよび塩素ガスを０．５Ｐａの圧力で供給するドライエッチング法によって，絶縁性基板１２上のｎ型ＧａＮ層１６がエッチング除去され，絶縁性基板１２が露出するように凹部３２が形成される。これによって、エッチングの深さは３．６μｍとなり，ＧａＮ系発光ダイオード１４ａ～１４ｄを構成する層がそれぞれ分離される。

【００２８】つづいて，図４（ｄ）に示すように，2×10^{-6}ｔｏｒｒの圧力による電子ビーム蒸着によって，ｐ型ＧａＮコンタクト層２０上面全体に，膜厚２ｎｍのＮｉ膜および膜厚４ｎｍのＡｕ膜がこの順序で成膜され，フォトリソグラフィーによって面状の透光性電極２２が形成される。また，2×10^{-6}ｔｏｒｒの圧力による電子ビーム蒸着によって，ｎ型ＧａＮ層１６上に，膜厚３０ｎｍのＴｉ膜および膜厚５００ｎｍのＡｌ膜がこの順序で成膜され，フォトリソグラフィーによってｎ型ＧａＮ層１６上の一端縁近傍かつ幅方向に延びたｎ型側電極２４が形成される。ｎ型側電極２４はＧａＮ系発光ダイオードのカソード電極に相当する。

【００２９】その後，図４（ｅ）に示すように，図４（ｄ）で形成されたチップの上面全体に膜厚３００ｎｍのSiO_2からなる保護膜２６が電子ビーム蒸着によって形成される。

【００３０】その後、透光性電極２２およびｎ型側電極２４のそれぞれの上面の一部が露出するように、フォトリソグラフィーによって保護膜２６がエッチング除去されて開口される。このとき、１つのＧａＮ系発光ダイオードに関していえば、透光性電極２２上の開口はｎ型側電極２４の形成箇所とは反対側の端縁近傍かつ幅方向に延びて形成される。また、ｎ型側電極２４の開口も幅方向に延びて形成される。

【００３１】そして、図４（ｆ）に示すように、２×１０⁻⁶ｔｏｒｒの圧力による電子ビーム蒸着によって、保護膜２６の上面全体に膜厚１００ｎｍのＮｉ膜および膜厚７００ｎｍのＡｕ膜がこの順序で成膜され、フォトリソグラフィーによって内部配線２８が形成される。したがって、１つのＧａＮ系発光ダイオードに関していえば、透光性電極２２に接続される内部配線２８およびｎ型側電極２４に接続される内部配線２８は、ＧａＮ系発光ダイオードの両端からそれぞれ反対方向に引き出されることになる。なお、図４（ｆ）には図示しないが、パッド電極３０も同様にして同時に形成される。内部配線２８およびパッド電極３０のうち、透光性電極２２と接続される一端部が、ＧａＮ系発光ダイオードのアノード電極に相当する。

【００３２】このようにして、４個のＧａＮ系発光ダイオード１４ａ～１４ｄが直列接続された発光部品１０が形成される。

【００３３】発光強度１０によれば、一般のＩＣ製造プロセスを用いて１枚の絶縁性基板１２上に複数のＧａＮ系発光ダイオード１４ａ～１４ｄが形成されかつ接続されるので、相互に隣接するＧａＮ系発光ダイオードの間隔を従来よりも狭くできる。したがって、単一の部品として形成されかつ発光強度が大きい面光源として適する発光部品１０が得られる。

【００３４】また、発光部品１０によれば、図５（ａ）にも示すように、絶縁性基板１２上にＧａＮ系発光ダイオード１４ａ～１４ｄを直線状に形成することができるので、図５（ｂ）からわかるように、大面積の発光が得られる。

【００３５】また、同一の絶縁性基板１２上にＧａＮ系発光ダイオード１４ａ～１４ｄを形成できるので、ＧａＮ系発光ダイオード１４ａ～１４ｄ間の絶縁分離、集積化が容易になる。

【００３６】各ＧａＮ系発光ダイオード１４ａ～１４ｄの発光強度分布は図６に示すようになる。透光性電極２２の抵抗をＲｔ、ｎ型ＧａＮ層１６の抵抗をＲｎとし、Ｒｐは、ｐ型ＧａＮコンタクト層２０の抵抗、透光性電極２２とｐ型ＧａＮコンタクト層２０との接触抵抗およびｐ－ｎ接合電圧相当抵抗分を示し、各抵抗は面内において一定と考えるとする。

【００３７】各ＧａＮ系発光ダイオード１４ａ～１４ｄは直線状に配列され、かつ相互に隣接するＧａＮ系発光ダイオードの一方の発光ダイオードのｎ型側電極２４と他方の発光ダイオードの透光性電極２２とが幅Ｗ１を有する内部配線２８によって接続されているので、透光性電極２２の単位面積当たりの抵抗が小さい場合（Ｒｔ≒Ｒｎ）には、図６（ａ）に示すように、透光性電極２２全面からｎ型ＧａＮ層１６に電流が流れ、発光層１８を通過する電流は発光層１８内の位置に拘わらず均一になる。したがって、図６（ｂ）および（ｃ）に示すように、透光性電極２２からの発光は発光箇所に拘わらず略均一になり、かつより大きな発光強度が得られる。

【００３８】因みに、透光性電極２２の単位面積当たりの抵抗が大きい場合（Ｒｔ＞Ｒｎ）には、図６（ｄ）に示すように、発光層１８を通過する電流は内部配線２８すなわちアノード電極近傍に集中する。この場合、図６（ｅ）に示すＸ－Ｘ断面における発光強度は不均一になるが、各ＧａＮ系発光ダイオード１４ａ～１４ｄは直線状に配列され、かつ相互に隣接するＧａＮ系発光ダイオードの一方の発光ダイオードのｎ型側電極２４と他方の発光ダイオードの透光性電極２２とが幅Ｗ１を有する内部配線２８によって接続されているので、図６（ｆ）に示すＹ－Ｙ断面における発光強度は略均一になる。したがって、上述した透光性電極２２の単位面積当たりの抵抗が小さい場合より発光強度は不均一かつ小さくなるが、少なくとも図９に示す従来技術より発光強度は均一化されかつ大きくなる。

【００３９】さらに、図７（ａ）～（ｃ）に示すように、絶縁性基板１２ａ上にＧａＮ系発光ダイオード１４ａ～１４ｄを形成しコ字状に直列接続してもよく、この場合にも、単一の部品として形成されかつ大きな発光強度が得られ面光源として適する発光部品が得られる。

【００４０】すなわち、図５および図７からわかるように、絶縁性基板上に複数個のＧａＮ系発光ダイオードを形成し直列接続することによって、単一の部品として形成されかつ大きな発光強度が得られ面光源に応用できる発光部品が得られる。

【００４１】なお、ＧａＮ系発光ダイオードを駆動するには、３Ｖ以上必要であり、５Ｖ電源を用いて回路動作を行うことが多い。１つのＧａＮ系発光ダイオードあたり４Ｖ（たとえば２０ｍＡの電流を流す場合）程度必要とすると、駆動電圧が２４Ｖの場合には６つのＧａＮ系発光ダイオードが直列接続された発光部品を用いればよい。このように、駆動電圧に応じた直列素子数のＧａＮ系発光ダイオードを用いることによって、大面積の発光が可能となり、かつ駆動電圧の制限も少なくなり、多方面にわたる応用が期待できる。

【００４２】また、図８に示すように、ＧａＮ系発光ダイオード１４ａ～１４ｎとともに抵抗（図８（ａ））やＦＥＴ（図８（ｂ））などの電流制御素子が同一絶縁性基板上に形成されてもよく、この場合、ＧａＮ系発光ダイオード１４ａ～１４ｎと電流制御素子とを同一の絶縁

性基板上にモノリシックに形成できる。

【００４３】このように外付け素子が不要になるため、小型かつ軽量の発光部品１０が得られ、また、ＧａＮ系発光ダイオード１４ａ～１４ｄだけではなく電流制御素子をもワイドギャップバンド材料によって形成できるので、発熱に対して強い発光部品１０が得られ、集積化が容易となる。さらに、絶縁性基板の一方主面にのみ素子を構成するので、この場合にも一般的なＩＣ製造プロセスを適用できる。また、ＧａＮ系発光ダイオードの数を調整するだけではなく電流制御素子を付加することにより、駆動電圧の制限がさらに少なくなる。さらに、ＧａＮ系発光ダイオード１４ａ～１４ｎに抵抗を付加することによって、組立時や使用時におけるサージ電流を抑制することができる。

【００４４】図１の実施の形態では、４個のＧａＮ系発光ダイオード１４ａ～１４ｄを直列接続する場合について述べたが、ＧａＮ系発光ダイオードの数はこれに限定されないことはいうまでもない。

【００４５】また、上述の実施の形態では、発光素子として発光ダイオードを例に説明したが、これに限定されず、レーザであってもよい。

【００４６】さらに、発光部品１０の３族窒化物半導体発光素子としては、たとえばＡｌＮ、ＩｎＮ、ＢＮまたはＩｎＧａＮなどを含む３族窒化物半導体からなる発光素子であれば、任意の３族窒化物半導体発光素子を用いることができる。

【００４７】

【発明の効果】この発明によれば、１つの基板上に発光部を複数形成でき、単一の部品として形成されかつ大きな発光強度が得られ面光源として適する発光部品が得られる。

【図面の簡単な説明】

【図１】この発明の一実施形態の主要部を示す平面図である。

【図２】図１の実施形態を示す断面図である。

＊【図３】図１の実施形態を示す等価回路図である。

【図４】図１の実施形態の製造プロセスを示す工程図である。

【図５】（ａ）は図１の実施形態におけるＧａＮ系発光ダイオードの配置状態を模式的に示す平面図であり、（ｂ）はその発光状態を模式的に示す側面図である。

【図６】ＧａＮ系発光ダイオードの電流の流れおよび発光強度分布の概略を示す図解図であり、（ａ）～（ｃ）は透光性電極の抵抗が小さい場合、（ｄ）～（ｆ）は透光性電極の抵抗が大きい場合をそれぞれ示す。

【図７】（ａ）はこの発明の他の実施の形態を示す等価回路図であり、（ｂ）はその実施の形態におけるＧａＮ系発光ダイオードの配置状態を模式的に示す平面図であり、（ｃ）はその発光状態を模式的に示す側面図である。

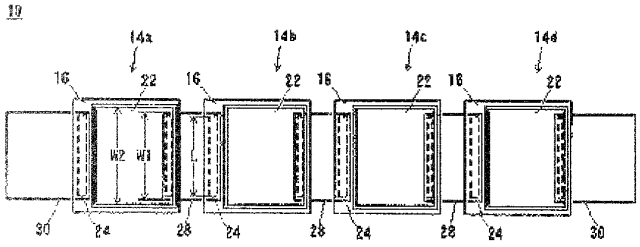
【図８】この発明のその他の実施の形態を示す等価回路図であり、（ａ）はＧａＮ系発光ダイオードに抵抗を付加したもの、（ｂ）はＧａＮ系発光ダイオードにＦＥＴを付加したものをそれぞれ示す。

【図９】（ａ）は従来技術を示す平面図であり、（ｂ）はその端面図である。

【符号の説明】

１０	発光部品
１２．１２ａ	絶縁性基板
１４ａ～１４ｄ．１４ｎ	ＧａＮ系発光ダイオード
１６	ｎ型ＧａＮバッファ層
１８	発光層
２０	ｐ型ＧａＮコンタクト層
２２	透光性電極
２４	ｎ型側電極
２６	保護膜
２８	内部配線
３０	パッド電極
Ｗ１	内部配線の幅

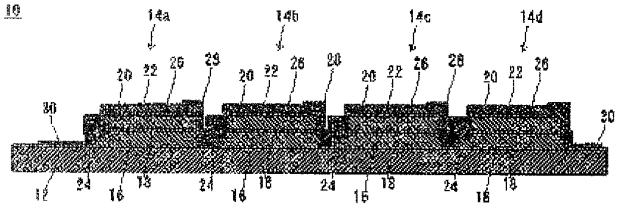
【図１】



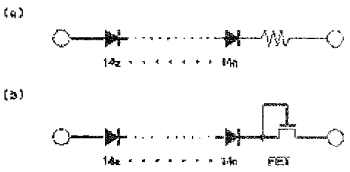
【図３】



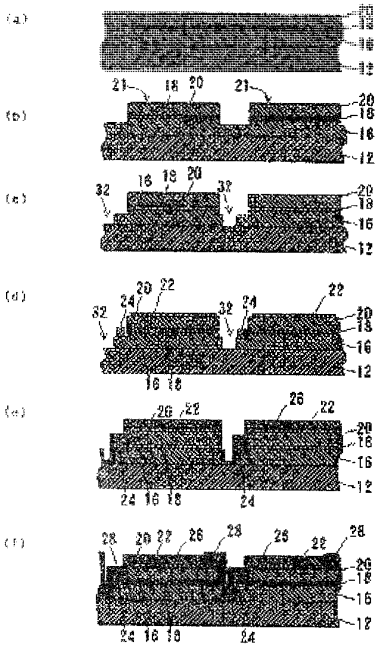
【図2】



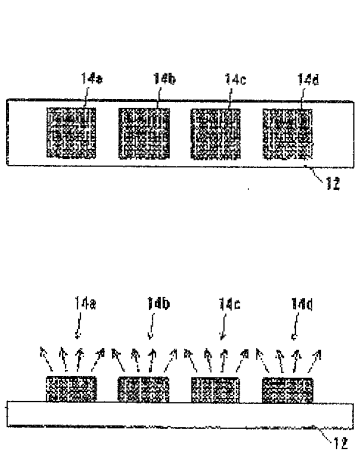
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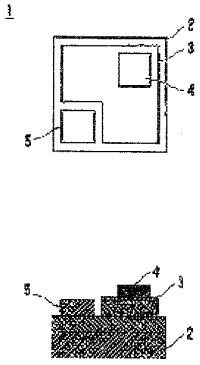
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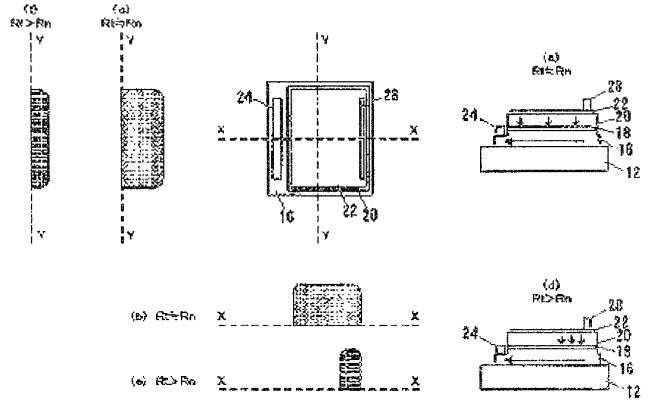
【図5】



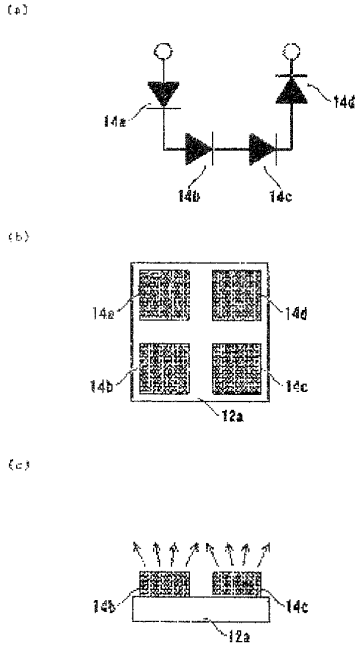
【図9】



【図６】



【図７】



Electronic Acknowledgement Receipt

EFS ID:	6400117
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
Receipt Date:	05-NOV-2009
Filing Date:	26-DEC-2007
Time Stamp:	16:51:30
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	US_IDS_Form_SB_08a.pdf	1419076 7c63c8deb47f9bb7c3d018c9e7cd9d66e17c5b90	no	5

Warnings:	
Information:	

2	Foreign Reference	JP11-150303.pdf	1954573 999af3f1e09a0d18d42904a4ce5d4359793a7a5e	no	33

Warnings:	
Information:	
Total Files Size (in bytes):	3373649

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	Docket No.: P2317US00
Jong Lam LEE, *et al.*	
Serial No.: 11/993,965	Group Art Unit: 2818
Confirmation No.: 2191	
Filed: Dec. 27, 2007	Examiner: NGUYEN, Thinh T.

For: **LIGHT EMITTING DEVICE**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

Prior to examination on the merits, please amend the above-identified application as follows.

Amendments to the Claims begin on page 2.

Remarks begin on page 5.

It is not believed that any extensions of time or fees for net addition of claims are required at this moment. However, if additional extension of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. §1.136(a), and any fees required therefor are hereby authorized to be charged to our Deposit Account No. 50-3698.

AMENDMENTS TO THE CLAIMS

Please **CANCEL** claims 7-16 without prejudice or disclaimer.

Please **ADD** claims 17-31.

1. (Original) A light emitting device, comprising:

a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer formed on a portion of the N-type semiconductor layer on a substrate, wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface including the N-type or P-type semiconductor layer of the light emitting cell has a slope of 20 to 80° from a horizontal plane.

2. (Original) The light emitting device as claimed in claim 1, further comprising a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

3. (Previously presented) The light emitting device as claimed in claim 1, further comprising a transparent electrode layer on the P-type semiconductor layer.

4. (Previously presented) The light emitting device as claimed in claim 1, further comprising P-type and N-type ohmic metal layers containing Cr or Au on the P-type and N-type semiconductor layers, respectively.

5-16. (Canceled)

17. (New) A light emitting device comprising:

a substrate; and

a plurality of light emitting cells disposed on the substrate to be spaced apart from each other,

wherein the light emitting cell comprises a first-type semiconductor layer and a second-type semiconductor layer,

at least one of the light emitting cells has at least one side surface that is not perpendicular to a horizontal plane, and

the first-type semiconductor layer of at least one of the light emitting cells is electrically connected to the second-type semiconductor layer of an adjacent another light emitting cell.

18. (New) The light emitting device as claimed in claim 17, wherein the side surface that is not perpendicular is inclined at a slope with respect to the horizontal plane.

19. (New) The light emitting device as claimed in claim 18, wherein the slope is approximately 20˚ to approximately 80˚ with respect to the horizontal plane.

20. (New) The light emitting device as claimed in claim 18, wherein the inclined surface of the light emitting cell comprises at least a side surface of the first-type semiconductor layer.

21. (New) The light emitting device as claimed in claim 20, wherein the first-type semiconductor layer is an N-type semiconductor layer.

22. (New) The light emitting device as claimed in claim 20, wherein the inclined surface of the light emitting cell is formed continuously up to the second-type semiconductor layer.

23. (New) The light emitting device as claimed in claim 22, wherein the second-type semiconductor layer is a P-type semiconductor layer.

24. (New) The light emitting device as claimed in claim 22, wherein the second-type semiconductor layer of the light emitting cell comprises at least one surface that is not inclined.

25. (New) The light emitting device as claimed in claim 20, wherein at least one of the light emitting cells further comprises a first-type bonding pad and a second-type bonding pad that are disposed respectively on the first-type semiconductor layer and the second-type semiconductor layer.

26. (New) The light emitting device as claimed in claim 25, wherein the electrical connection is configured to electrically connect the first-type bonding pad disposed on the first-type semiconductor layer of at least one of the light emitting cells to the second-type bonding pad disposed on the second-type semiconductor layer of the adjacent another light emitting cell.

27. (New) The light emitting device as claimed in claim 26, wherein the electrical connection between the bonding pads is formed through the same process.

28. (New) The light emitting device as claimed in claim 27, wherein the same process comprises at least one of plating method, chemical vapor deposition (CVD), physical vapor deposition (PVD), and electron beam deposition.

29. (New) The light emitting device as claimed in claim 26, wherein the electrical connection is formed by an electrical conductor disposed on the inclined surface of the light emitting cell.

30. (New) The light emitting device as claimed in claim 29, wherein an insulation layer is disposed between the light emitting cell and the electrical conductor.

31. (New) The light emitting device as claimed in claim 20, further comprising Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof disposed on a rear surface of the substrate on which the light emitting cell is formed.

REMARKS

By this Amendment, claims 7-16 have been canceled without prejudice or disclaimer, and claims 17-31 have been added. Claims 5-6 have been previously canceled. Accordingly, claims 1-4 and 17-31 are pending in this application, of which claims 1 and 17 are independent.

Applicants respectfully submit that the amendments do not add new matter to the application and are fully supported by the specification. Support for the added claims may be found at least in: Figures 1-17 and 32; paragraphs [0039]-[0091] and [0135].

Added Claims

Added claims 17-31 are directed to additional features of the invention, which are not disclosed or suggested in the art of record.

CONCLUSION

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,

/hae-chan park/

Hae-Chan Park
Reg. No. 50,114

Date: November 5, 2009

CUSTOMER NUMBER: 58027
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Vienna, VA 22182
Telephone: 703-288-5105
Facsimile: 703-288-5139
HCP/BCR

Electronic Acknowledgement Receipt

EFS ID:	6401578
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
Receipt Date:	05-NOV-2009
Filing Date:	26-DEC-2007
Time Stamp:	17:09:47
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Preliminary_Amendment.pdf	31647 384e242531d492b194fda6fcc7862008aa136877	yes	5

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Claims	2	4
	Applicant Arguments/Remarks Made in an Amendment	5	5
Warnings:			
Information:			
	Total Files Size (in bytes):	31647	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/993,965	12/26/2007	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	11/05/2009	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 19	Minus	** 20	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/DONNA L. PRICE/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/993,965	12/26/2007	Jong Lam Lee	P2317US00	2191

58027 7590 11/06/2009

H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

EXAMINER	
NGUYEN, THINH T	

ART UNIT	PAPER NUMBER
2818	

NOTIFICATION DATE	DELIVERY MODE
11/06/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATENT@PARK-LAW.COM

Office Action Summary	Application No.	Applicant(s)	
	11/993,965	LEE ET AL.	
	Examiner	Art Unit	
	THINH T. NGUYEN	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *1* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *7-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-6* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 are pending in the application

Election/ Restriction

2. Applicant election of claims 1-6 pertains to group I in the communication with the Office on July /30th /2009 is acknowledged.

3 Claims 1-6 directed to semiconductor devices are restricted as follows:

This application contains claims directed to more than one species of the generic invention. These species are deemed to lack unity of invention because they are not so linked as to form a single general inventive concept under PCT Rule 13.1.

The species are as follows:

I/ Species I: Embodiment I. Described in claims 1-4

II/Species II: Embodiment II. Described in claims 5-6

The species listed above do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, the species lack the same or corresponding special technical features because species I does not have the technical features of a submount substrate that species II possess.

Applicant is required, in reply to this action, to elect a single species to which the claims shall be restricted if no generic claim is finally held to be allowable. The reply must also identify

the claims readable on the elected species, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered non-responsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

This application contains claims directed to the patentably distinct species **as set forth above.** The species are independent or distinct because claims to the different species recite the mutually exclusive characteristics of such species. In addition, these species are not obvious variants of each other based on the current record.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable.

There is an examination and search burden for these patentably distinct species due to their mutually exclusive characteristics. The species require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search queries); and/or the prior art applicable to one species would not likely be applicable to another species; and/or the species are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species to be examined even though the requirement may be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected species, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election. The election of the species may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the election of species requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected species. (MPEP § 809.02(a).)

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the species unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other species.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141.

4. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a diligently filed petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(h).

CONCLUSION

5 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on 9.30 AM 6.30 PM Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Loke can be reached on (571) 272-1657. The fax phone numbers for the organization where this application or proceeding is assigned are 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/**Thinh T Nguyen**/

Patent Examiner
Art Unit 2818

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11993965	LEE ET AL.
	Examiner	Art Unit
	THINH T NGUYEN	2818

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/06/2009	10/30/2009							
	1	÷	÷							
	2	÷	÷							
	3	÷	÷							
	4	÷	÷							
	5	÷	÷							
	6	÷	÷							
	7	÷	N							
	8	÷	N							
	9	÷	N							
	10	÷	N							
	11	÷	N							
	12	÷	N							
	13	÷	N							
	14	÷	N							
	15	÷	N							
	16	÷	N							

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Docket No.: P2317US00

Jong Lam LEE, *et al.*

Serial No.: 11/993,965 Group Art Unit: 2818

Confirmation No.: 2191

Filed: December 26, 2007 Examiner: NGUYEN, Thinh T.

For: **LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO ELECTION/RESTRICTION REQUIREMENT

Sir:

In reply to the November 6, 2009 Restriction Requirement, Applicants respectfully request that the Restriction Requirement be withdrawn. Since the Preliminary Amendment filed on September 18, 2009 canceled claims 5-6, which were indicated as Species II, the Restriction Requirement is moot.

It is not believed that any extensions of time or fees are required. If extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned for under 37 C.F.R. §1.136(a) and associated fees may be charged to our Deposit Account No. 50-3698.

Respectfully submitted,

/hae-chan park/

Hae-Chan Park
Reg. No. 50,114

Dated: December 7, 2009

CUSTOMER NO.: 58027
H.C. Park & Associates, PLC

Electronic Acknowledgement Receipt

EFS ID:	6584222
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
Receipt Date:	07-DEC-2009
Filing Date:	26-DEC-2007
Time Stamp:	16:01:53
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	P2317US00_Response_to_Restriction_Requirement.pdf	14246 fc44154a3565a1c2dd1280e93c8e0b54778901ed	no	1

Warnings:	
Information:	

Total Files Size (in bytes):	14246

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/08a (06-09)
Approved for use through 07/31/2009. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(**Not for submission under 37 CFR 1.99)**

Application Number	11993965
Filing Date	2007-12-26
First Named Inventor	Jong Lam Lee
Art Unit	2818
Examiner Name	NGUYEN, THINH T
Attorney Docket Number	P2317US00

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2004-071644	JP		2004-03-04	NICHIA CHEM IND LTD		☐
	2	2004-273746	JP		2004-09-30	HITACHI CABLE LTD		☐
	3	2005-136130	JP		2005-05-26	KYOCERA CORP		☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T
	Attorney Docket Number	P2317US00

	4	2001-156331	JP		2001-06-08	NICHIA CHEM IND LTD		☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		☒

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T
	Attorney Docket Number	P2317US00

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2010-01-27
Name/Print	Hae-Chan Park	Registration Number	50114

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2004-071644
(43)Date of publication of application : 04.03.2004

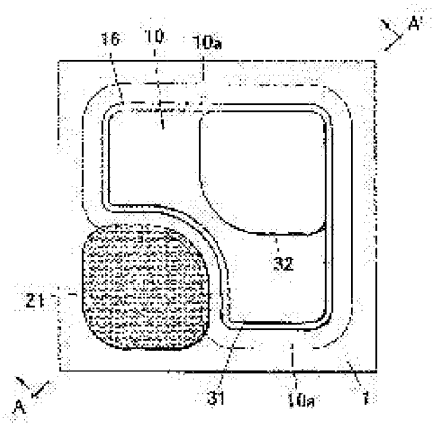
(51)Int.Cl. H01L 33/00

(21)Application number : 2002-225043
(22)Date of filing : 01.08.2002

(71)Applicant : NICHIA CHEM IND LTD
(72)Inventor : KUSUSE TAKESHI
SAKAMOTO TAKAHIKO

(54) NITRIDE SEMICONDUCTOR LIGHT EMITTING DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a nitride semiconductor light emitting device which ensures higher light emission efficiency and higher light emission efficiency.
SOLUTION: A nitride semiconductor light emitting device includes a laminated portion formed of an n-type semiconductor layer, an active layer, and a p-type semiconductor layer laminated on a substrate in order to emit the light. The side surface of the laminated portion is formed as a slope including the surface of the n-type semiconductor layer, and an n-type electrode is formed on the surface of the n-type semiconductor layer.



(19)日本国特許庁(JP)　(12)公開特許公報(A)　(11)特許出願公開番号
特開2004-71644
(P2004-71644A)
(43)公開日　平成16年3月4日(2004.3.4)

(51)Int.Cl.[7]	F I		テーマコード（参考）
H01L 33/00	H01L 33/00	E	5F041
	H01L 33/00	C	

審査請求 未請求　請求項の数 13　OL　（全 20 頁）

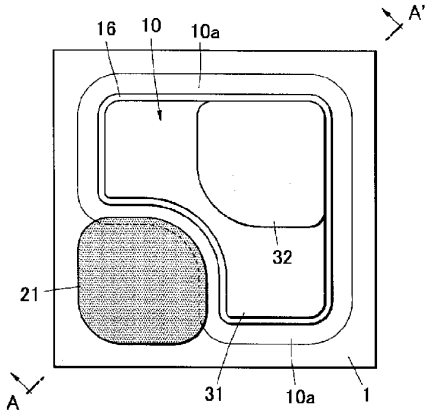
(21)出願番号　特願2002-225043(P2002-225043)
(22)出願日　平成14年8月1日(2002.8.1)

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日亜化学工業株式会社内

Fターム(参考)　5F041 AA03　CA40　CA93　CA99　CB05
CB15

(54)【発明の名称】窒化物半導体発光素子

(57)【要約】
【課題】発光効率が高くかつ光の出射効率が高い窒化物半導体発光素子を提供する。
【解決手段】基板上に、n型半導体層、活性層及びP型半導体層が積層されてなる積層部を有し、その積層部で発光する窒化物半導体発光素子において、積層部の側面は、n型半導体層の表面を含む傾斜面であり、そのn型半導体層の表面にn電極が形成されている。
【選択図】　図1



【特許請求の範囲】
【請求項１】
基板上に、ｎ型半導体層、活性層及びＰ型半導体層が積層されてなる積層部を有し、その積層部で発光する窒化物半導体発光素子において、
上記積層部の側面は、上記ｎ型半導体層の表面を含む傾斜面であり、そのｎ型半導体層の表面にｎ電極が形成されたことを特徴とする窒化物半導体発光素子。
【請求項２】
上記ｎ電極は上記積層部を囲むように形成された請求項１記載の窒化物半導体発光素子。
【請求項３】
上記ｎ電極を上記基板の側面から上記基板の下面にも連続して形成した請求項１又は２記載の窒化物半導体発光素子。
【請求項４】
上記積層部を円形とした請求項１～３のうちのいずれか１つに記載の窒化物半導体発光素子。
【請求項５】
上記積層部を六角形とした請求項１～３のうちのいずれか１つに記載の窒化物半導体発光素子。
【請求項６】
上記発光領域となる積層部を複数形成した請求項１～５のうちのいずれか１つに記載の窒化物半導体発光素子。
【請求項７】
上記各積層部に形成されたｎ電極は、互いに接続された共通電極として形成された請求項６記載の窒化物半導体発光素子。
【請求項８】
上記各積層部において形成された上記Ｐ型半導体層とオーミック接触するＰ側オーミック電極が互いに接続された請求項７記載の窒化物半導体発光素子。
【請求項９】
上記積層部を覆うように反射層を形成した請求項１，２，４～８のうちのいずれか１つに記載の窒化物半導体発光素子。
【請求項１０】
上記反射層は上記積層部を覆うように絶縁膜を介して金属層を形成することにより形成された請求項９記載の窒化物半導体発光素子。
【請求項１１】
上記金属層は、上記積層部のＰ型半導体層にそれぞれ形成されたＰオーミック電極を接続する接続電極である請求項１０記載の窒化物半導体発光素子。
【請求項１２】
上記反射層は誘電体多層膜からなる請求項９記載の窒化物半導体発光素子。
【請求項１３】
上記傾斜側面は、外側に膨らんだ凸曲面である請求項１～１２のうちのいずれか１つに記載の窒化物半導体発光素子。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】
本発明は、発光素子、特に窒化物半導体発光素子に関する。
【０００２】
【従来の技術】
近年、窒化ガリウム系化合物半導体を用いた発光ダイオードが、紫外域、青色等の比較的短い波長域を中心に広く用いられるようになって来ている。この窒化ガリウム系化合物半導体は直接遷移であり発光効率が高いことからもその適用範囲が拡大している。
【０００３】

【発明が解決しようとする課題】
しかしながら、窒化ガリウム系化合物半導体は通常、絶縁基板であるサファイア基板の上に成長されることに起因して、従来の窒化物半導体発光素子には以下のような課題があった。
第１に、サファイア基板が絶縁体であるために、ｎ側の電極とＰ側の電極をいずれも、サファイア基板上の窒化ガリウム半導体の上に形成する必要があり、特にｎ側の電極部分は、非発光領域となり、発光領域から生じた光が、ＧａＮ層を横方向に伝播する際の多重反射により吸収され、取り出し効率を低下させるという問題点があった。
第２に、発光した光は基板面に対して通常は垂直方向に取り出すように構成されるが、発光ダイオードの側面から出射される光の割合が比較的高く、発光した光を効果的に利用することができないという問題があった。
【０００４】
そこで、本発明は、ｎ側電極下部での多重反射をなくし、ｎ側の電極による吸収を低減し、取り出し効率の高い窒化物半導体発光素子を提供することを第１の目的とする。
また、本発明は発光した光を効果的に利用することができる窒化物半導体発光素子を提供することを第２の目的とする。
【０００５】
【課題を解決するための手段】
以上の従来の問題点を解決するために、本発明に係る窒化物半導体発光素子は、基板上に、ｎ型半導体層、活性層及びＰ型半導体層が積層されてなる積層部を有し、その積層部で発光する窒化物半導体発光素子において、
上記積層部の側面は、上記ｎ型半導体層の表面を含む傾斜面であり、そのｎ型半導体層の表面にｎ電極が形成されたことを特徴とする。
以上のように構成された窒化物半導体発光素子は、光の出射効率を高くできる。
【０００６】
本発明に係る窒化物半導体発光素子では、上記ｎ電極は上記積層部を囲むように形成されていることが好ましい。
【０００７】
また、本発明に係る窒化物半導体発光素子では、上記ｎ電極を上記基板の側面から上記基板の下面にも連続して形成することができる。このようにすると、Ｐ側オーミック電極を透光性電極としてその透光性電極を介して光を出射させる場合に、上記基板の側面及び上記基板の下面で反射した光も透光性電極を介して出力できるので、光の取り出し効率を高くできる。
【０００８】
また、本発明に係る窒化物半導体発光素子では、上記発光領域となる積層部を複数形成することもでき、これにより、大面積でかつ発光効率の高い窒化物半導体発光素子を構成できる。
【０００９】
上記積層部を複数形成した窒化物半導体発光素子では、上記各積層部に形成されたｎ電極を互いに接続して共通電極として形成することができる。
これにより、上記発光領域である積層部を容易に並列接続することが可能となる。
また、上記積層部を複数形成した窒化物半導体発光素子では、上記ｎ電極を互いに接続して共通電極として形成するとともに、上記各積層部において形成された上記Ｐ型半導体層とオーミック接触するＰ側オーミック電極を互いに接続することもできる。
これにより、上記発光領域である積層部が素子上で並列接続された窒化物半導体発光素子を提供できる。
【００１０】
また、本発明に係る窒化物半導体発光素子において、基板側から光を出力するように構成する場合には、光の出射効率を高くするために、上記積層部を覆うように反射層を形成することが好ましい。

【００１１】
また、上記窒化物半導体発光素子において、上記金属層は、上記積層部のＰ型半導体層にそれぞれ形成されたＰオーミック電極を接続する接続電極により構成することができる。
【００１２】
本発明に係る窒化物半導体発光素子において、上記反射層は上記積層部を覆うように絶縁膜を介して金属層を形成することにより形成してもよいし、誘電体多層膜により構成するようにしても良い。
【００１３】
本発明に係る窒化物半導体発光素子において、上記傾斜側面は、外側に膨らんだ凸曲面とすることもできる。
【００１４】
【発明の実施の形態】
以下、図面を参照しながら本発明に係る実施の形態の窒化物半導体発光素子について説明する。
実施の形態１．
本発明に係る実施の形態１の窒化物半導体発光素子は、図１及び図２に示すように、発光領域を構成する積層部１０の側面を内側に傾斜した傾斜面１０αとし、その傾斜面１０αに露出したｎ型コンタクト層１２とオーミック接触するようにｎ電極２１を形成することにより構成されている。
【００１５】
実施の形態１の窒化物半導体発光素子において、積層部１０は、図２に示すように、サファイア基板１上に、バッファ層１１、ｎ型コンタクト層１２、ｎ型クラッド層１３、発光層１４、Ｐ型クラッド層１５及びＰ型コンタクト層１６を順次成長させて積層構造を形成し、図１に示す平面形状（略矩形形状において、１つの隅部が円弧状に切り欠かれた形状）になるようにエッチングすることにより形成される。
【００１６】
積層部１０を構成する各層は例えば次のようなもので形成する。
バッファ層１１：４００℃～６００℃の低温で成長されたＧａＮ又はＡｌＧａＮ層、
ｎ型コンタクト層１２：Ｓｉドープのガ（例えば、厚さ６μｍ）、
ｎ型クラッド層１３：ｎ型ＡｌＧａＮ、
発光層１４：ノンドープのＩｎＧａＮ井戸層を含む（例えば、厚さ約３０Å）単一又は多重量子井戸構造、
Ｐ型クラッド層１５：Ｐ型ＡｌＧａＮ、
Ｐ型コンタクト層１６：Ｍｇがドープされたガ（例えば、厚さ約１２００Å）。
【００１７】
また、本実施の形態１において、積層部１０を形成するためのエッチングは、サファイヤの表面が露出するまで行い、積層部１０が円弧状に切り欠かれた１つの隅部にｎ電極２１を形成するためにサファィヤ基板表面を露出させる。尚、本実施の形態１では、ｎ電極２１を形成するために露出されたサファイア基板の表面と連続して積層部１０の周りを取り囲むようにサファィヤ基板の表面が露出される。
【００１８】
本実施の形態１において、ｎ電極２１は、図１及び図２に示すように、積層部１０の１つの隅部に露出させたサファィヤ基板１の表面から積層部１０の傾斜面１０αに亙って連続して形成し、傾斜面１０αに露出したｎ型コンタクト層１２とオーミック接触する。
また、Ｐ側の電極は全面電極３１とＰパッド電極３２とからなり、全面電極３１は積層部１０の最上層に位置するＰ型コンタクト層１６の表面のほぼ全面に形成され、Ｐパッド電極３２は全面電極３１上のｎ側電極２１と対角をなす位置（他方の隅部）に形成される。
【００１９】
以上のように構成された実施の形態１の窒化物半導体発光素子は、ｎ電極２１による光の吸収を極めて少なくできるので、効率良く光を出力できる。

すなわち、図２１に示す従来の構造では、基板１とｎ電極５２１の間に存在するｎ型コンタクト層５１２に発光領域で発光した光が漏れ出して導波し、基板１の上面とｎ電極１２１の裏面により繰り返して反射される間に（図２１において、Ｙ１００の符号を付して模式的に示す）、大部分の光がｎ電極１２１によって吸収されて結局外部に取り出すことができないという問題があった。しかしながら、本発明では、傾斜側面１０αに露出されたｎ型コンタクト層１２の表面でｎ電極をオーミック接触させることにより、ｎ型コンタクト層１２において光が導波する部分を無くし（図２において、Ｙ１の符号を付して模式的に示す）、従来の問題点を解決している。

また、発光した光を基板側から出射させる場合に、積層部１０の傾斜側面１０αで反射した光も基板を介して出力することができ、出射効率を向上させることができる。

【００２０】

また、発光した光を基板側から出射させる場合に、傾斜側面１０αで効果的に反射させるためには、傾斜側面１０αには通常ＳｉＯ２保護膜が形成されていることを考慮すると、傾斜側面１０αの傾斜角αを６０度以下に設定することが好ましく、４５度以下に設定することがより好ましい。

この傾斜角αは本明細書では、図２２に示すように定義し、その好ましい範囲は、臨界角θｃが$\mathrm{Sin}\theta c = n_S / n_G$（$n_G$：活性層の屈折率、$n_S$：ＳｉＯ２保護膜の屈折率）で与えられることから、求めることができる。

例えば、波長３８０ｎｍの光を発光する素子の場合、波長３８０ｎｍの光に対する$Al_xGa_{1-x}N$の屈折率は、×の値が１～０の範囲であるとすると２．１５～２．８０である。この時、臨界角θｃが最も小さくなるのは、屈折率が２．８０の場合であり、この時の臨界角θｃは約３０°である。

従って、臨界角θｃを３０°以上、すなわち、傾斜角αを６０°以下に設定すると、少なくとも半導体層に平行に伝播される最も強い光は全反射されることになる。

以上のように傾斜角αを６０°以下に設定すると半導体層と平行に伝播される最も強い光は全反射されて取り出し効率を向上させることができる。しかしながら、層内を伝播される光には半導体層に平行でない光もあり、それらも効果的に全反射させるためには、傾斜角αを４５度以下に設定することがさらに好ましい。

また、傾斜側面１０αにｎ電極を形成することを考慮した場合における、傾斜側面１０αの傾斜長Ｌの上から見た投影長Ｗは、１０μｍ以上であることが好ましい。

【００２１】

以上の説明では、１つの隅部において、ｎ電極２１とｎ型コンタクト層１２とがオーミック接触するように形成した例について説明したが、本実施の形態１では、図３及び図４に示すように、ｎ電極２２は積層部１０を囲むように形成することが好ましい。このようにすると、発光領域全体に均一に電流を注入することができ、効率良く発光させることができる。

【００２２】

実施の形態２．

本発明に係る実施の形態２の窒化物半導体発光素子は、図５に示すように、発光領域を構成する積層部１１０の形状を円形にしたものである。本実施の形態２の窒化物半導体発光素子において、ｎ電極２３が積層部１１０の内側に傾斜した側面である傾斜面１１０αに露出したｎ型コンタクト層１２とオーミック接触するように形成されている点は、実施の形態１と同様である。

【００２３】

また、実施の形態２の窒化物半導体発光素子において、積層部１１０の積層構造（半導体層の構成）は実施の形態１の発光素子と同様であり、積層部１１０を形成するためのエッチングは、サファイヤの表面が露出するまで行う。

実施の形態２において、Ｐ側の電極は全面電極３３とＰパッド電極３４とからなり、全面電極３３は積層部１１０の最上層に位置するＰ型コンタクト層１６の円形表面のほぼ全面に形成され、Ｐパッド電極３４は全面電極３３中央部に形成される。

ここで、全面電極３３、Ｐパッド電極３４及び円形の積層部１１０は中心が一致するように同心円状に形成される。

【００２４】

以上のように構成された実施の形態２の窒化物半導体発光素子は、実施の形態１の発光素子と同様の作用効果を有する。

すなわち、ｎ電極２３による光の吸収を極めて少なくでき、効率良く光を出力できるとともに、積層部１１０の傾斜側面１１０ａで反射した光も基板を介して出力することができ、出射効率を向上させることができる。

さらに、本実施の形態２では、図５から明らかなように、ｎ電極２３は積層部１１０を囲むように形成しているので、発光領域全体に均一に電流を注入することができ、効率良く発光させることができる。

【００２５】

実施の形態３.

本発明に係る実施の形態３の窒化物半導体発光素子は、図６、図７に示すように、発光領域を構成する積層部１１０の形状を円形にしたものであるが、本実施の形態２の窒化物半導体発光素子とは、以下の点が異なる。

すなわち、実施の形態３の窒化物半導体発光素子では、Ｐ型コンタクト層の表面に透光性を有する透光性オーミック電極３３ａを形成し、その上にＰパッド電極３４を形成している。

また、実施の形態３の窒化物半導体発光素子では、図７に示すように、傾斜側面１１０ａでｎ型コンタクト層とオーミック接触するｎ電極２４を基板１の側面及び裏面に連続して形成している。

この実施の形態３において、透光性オーミック電極３３ａとｎ電極２４以外は、実施の形態２と同様に構成される。

【００２６】

以上のように構成された実施の形態３の窒化物半導体発光素子は、積層部１１０で発光した光を透光性オーミック電極３３ａを介して出力することができ、以下のような効果を有する。

すなわち、ｎ電極２４による光の吸収を極めて少なくでき、効率良く光を出力でき、基板の側面及び裏面に形成されたｎ電極２４により光を反射して透光性オーミック電極３３ａを介して出力できるので、出射効率を向上させることができる。

また、本実施の形態３では、図６から明らかなように、ｎ電極２４を積層部１１０を囲むように形成しているので、発光領域全体に均一に電流を注入することができ、効率良く発光させることができる。

【００２７】

以上の実施の形態３の窒化物半導体発光素子では、ｎ電極２４により基板全体が覆われるように構成したが、本発明はこれに限られるものではなく、図８に示すように、ｎ電極２５と基板１を覆う電極２６とを別の金属で構成してもよい。

以上のように構成しても実施の形態３と同様の作用効果が得られ、さらに以下のような効果がある。

すなわち、ｎ電極２５はｎ型コンタクト層と良好なオーミック接触が得られる金属から選択して構成し、基板１を覆う電極２６には、その機能に応じて適切な金属材料を選択して構成することができる。

具体的には、基板１の裏面をはんだ付けにより実装する場合には、電極２６の材料としてはんだ耐熱性の優れた材料を選択したり、光の反射を重視する場合には反射率の高い金属を選択して用いることができる。

【００２８】

実施の形態４.

本発明に係る実施の形態４の窒化物半導体発光素子は、図９に示すように、発光領域を構成する積層部１１１の形状を矩形にしたものである。

すなわち、実施の形態３の窒化物半導体発光素子では、Ｐ型コンタクト層の表面に全面電極３５を形成し、その上にＰパッド電極３６を形成している。
また、図９に示すように、矩形の積層部１１１の傾斜側面１１１ａでｎ型コンタクト層とオーミック接触するｎ電極２７を基板の表面とｎ型コンタクト層（傾斜側面１１１ａに露出したもの）とに亙って形成している。
尚、実施の形態４において、積層部の積層構造は実施の形態１～３と同様に構成される。
【００２９】
以上のように構成された実施の形態４の窒化物半導体発光素子は、実施の形態１～３と同様の作用効果を有する。
また、図９の窒化物半導体発光素子では、ｎ電極２７は積層部１１１の一辺でｎコンタクト層に接触するように形成したが、本実施の形態４では、図１０に示すように、積層部１１１の外周全体でｎコンタクト層とオーミック接触するようにｎ電極２８を形成することもでき、これにより、発光領域全体に均一に電流を注入することができ、効率良く発光させることができる。
【００３０】
実施の形態５．
実施の形態５の窒化物半導体発光素子は、図１１，図１２に示すように、複数（図１１，１２では１８個）の積層部２１０を備えた発光面積の大きい発光素子であって、素子全体の面積に占める発光領域の面積を大きくでき、発光領域全体を均一に発光させることができるという特徴を有する。
図１１は主としてｎ電極２２１の形態を示すために、Ｐ側ボンディング電極２５１及びＰ側接続電極２６１を省いて示す平面図であり、図１２はＰ側ボンディング電極２５１及びＰ側接続電極２６１を省略せずに示す平面図である。また、図１３は、図１２のＤ－Ｄ’線についての断面図である。
【００３１】
このように、発光領域を複数の部分に分割して形成するのは、大面積の発光領域を分割することなく１つの大きな領域として形成した場合に生じる、電極から離れた部分で電流が低下して発光効率が悪くなるという問題を解決するためである。しかしながら、発光領域を複数の部分に分割して形成した場合には、各発光領域間を接続する電極面積が大きくなり、いかにして発光領域の面積を確保するかが課題となる。また、図２１に示す構造の従来の素子を複数個並べた場合には、ｎ型コンタクト層を光が導波して反射を繰り返すうちにｎ電極により吸収される光により発光効率が低下する。しかしながら、本実施の形態５の窒化物半導体発光素子では、第１に各積層部の傾斜した側面にｎ型コンタクト層とオーミック接触するｎ電極を形成することにより、ｎ電極が必要とする面積を小さくして発光領域の面積を確保し、かつｎ電極による光の吸収を防止している。
【００３２】
また、本実施の形態５の窒化物半導体発光素子では、Ｐ側の全面電極による吸収も従来例に比較して抑えることができる。
すなわち、大面積の発光領域を分割することなく１つの大きな領域として形成した従来例では、図２３（ｂ）に示すように、臨界角以上でＰ側の全面電極に入射された光は、Ｐ側の全面電極７３１と、基板１と半導体層との間の境界の間で反射を繰り返すうちに、かなりの部分がＰ側の全面電極により吸収される。
また、発光領域を複数の部分に分割して形成した場合であっても、分割された発光領域が傾斜した側面を有していない場合には、図２３（ｃ）に示すように、臨界角以上でＰ側の全面電極７３１に入射された光が基板に略垂直な側面から出射されて隣接する発光領域に再入射される確率が高くなる。そのためにＰ側の全面電極により吸収される率が高くなる。
これに対して、本実施の形態５の窒化物半導体発光素子は、各発光領域が傾斜側面を有しているので、基板側から発光させる場合には、図２３（ａ）においてＡ２の符号を付して示す光のように、また、電極側から発光させる場合には、図２３（ａ）においてＡ３の符

号を付して示す光のように、隣接する発光領域に再入射されることなく（隣接する発光領域に再入射される確率を低くできる）、外部に出射される。これにより、Ｐ側の全面電極３１で吸収される率を低くできる。

【００８３】

また、実施の形態５の窒化物半導体発光素子では、発光領域を構成する積層部２１０の形状を六角形とし、その複数の積層部２１０は積層部間の面積が最も小さくなるように配列される（図１１，１２）。本実施の形態５において、隣接する積層部２１０間は基板の表面までエッチングされており（図１３）、複数の積層部２１０はそれぞれ完全に分離されている。尚、隣接する積層部２１０間の間隔は、例えば、１０μｍに設定される。

また、実施の形態５において、各積層部２１０の側面は、実施の形態１等と同様に全て傾斜面２１０αであり、その傾斜面２１０αに露出されたｎ型コンタクト層にオーミック接触するようにｎ電極２２１が形成される。

実施の形態５において、ｎ電極２２１は図１１に示すように全ての積層部２１０を取り囲むように一体として形成される。

【００８４】

実施の形態５において、各積層部２１０のＰ型コンタクト層のほぼ全面に全面電極２３１が形成され、その中央部にＰパッド電極２３２が形成される。そして、Ｐパッド電極２３２上に開口部を有する絶縁膜２７１が素子全体を覆うように形成され、その絶縁膜２７１上にＰパッド電極２３２を互いに接続する接続電極２６１（一端がＰ側ボンディング部に接続）が形成される。尚、絶縁膜２７１はｎ電極２２１のうちボンディング部２４１を開口させる開口部も有している。

【００８５】

以上のように構成された実施の形態５の窒化物半導体発光素子は、発光領域である積層部２１０の形状を六角形とし、その積層部２１０間の面積が最も小さくなるように配列し、かつ各積層部２１０の傾斜した傾斜側面にｎ電極を形成することにより、発光領域の面積が大きくなるように構成している。

これにより、発光領域を効果的に発光させることができる適切な大きさの複数の部分に分割し、かつｎ電極を形成するために必要となる面積を抑制することが可能となる。従って、発光領域の面積を低下させることなく、かつ各発光領域を効率よく発光させることができ、高い輝度を有する大面積の発光素子を構成できる。

【００８６】

実施の形態５の窒化物半導体発光素子は、基板側から光を出射するようにしても良いし、全面電極２３１を透明電極とすることにより半導体側から光を出射するようにしても良い。いずれの場合についても、発光層で発光した光は基板側とＰ型半導体側の両方に伝播されるので、出射側とは反対側に反射膜を形成することが好ましく、これにより出射効率を向上させることができる。

【００８７】

図１４は、本実施の形態５の窒化物半導体発光素子において、接続電極２６１間を更に接続する第２接続電極２６２を形成したものである。この第２接続電極２６２はＰ側ボンディング部２５１から離れた位置にある積層部２１０における電流注入量が低下するのを防止するために形成するものであり、各積層部の発光強度を均一化するものである。

しかしながら、半導体層側から光を出射させる場合には、この第２接続電極２６２が光を遮ることになるので、本構成は基板側から光を出射する場合に特に適している。

【００８８】

図１５は、半導体層側から光を出射させる場合に適した接続電極の例を示すものである。本例では、Ｐ側ボンディング部２５１に接続された第１接続電極２６３を積層部２１０の間のｎ電極上に絶縁膜を介してｎ電極と導通しないようにして形成する。この第１接続電極２６３は積層部上には形成されないので、積層部で発光した光を遮ることはない。そして、各積層部２１０のＰパッド電極と第１接続電極２６３の間は第２接続電極２６４により接続される。ここで、１つのＰパッド電極２３２と第１接続電極２６３の間は、１つの

第２接続電極２６４で接続されている。

【００３９】

図１６は、基板側から光を出射する場合の電極構造のより好ましい例を示したものである。

すなわち、図１６の窒化物半導体発光素子では、実施の形態５（図１２）の接続電極２６１（Ｐ側ボンディング部を含む）に替えて、絶縁膜２７１の上から複数の積層部を全て覆う電極層２６５を形成している。

このようにすると、各積層部の上面、特に傾斜側面からの光の漏れを防止でき（各積層部の上面及び傾斜側面で反射させることができ）、基板側から効率良く光を出射できる。

【００４０】

以上の実施の形態５の窒化物半導体発光素子では、各積層部２１０を六角形に形成した例により示したが、四角形又は円形等の他の形状であってもよい。

図２４は、積層部４１０を四角形にした具体例を示す平面図である。本例では、Ｐ側ボンディング部４５１を２つの隅部に形成された積層部４１０上にそれぞれ設け、そのＰ側ボンディング部４５１に接続された接続電極４６１により、積層部４１０のＰパッド電極間が接続される。尚、接続電極４６１は、積層部４１０の間のｎ電極上に絶縁膜を介してｎ電極と導通しないようにして形成される。

また、ｎ電極４２１は、全ての積層部４１０を取り囲むように一体として形成し、各積層部４１０の傾斜面４１０ａに露出されたｎ型コンタクト層とオーミック接触するように形成され、その一部にｎパッド電極４４１が形成される。

【００４１】

実施の形態６．

図１７は実施の形態６の窒化物半導体発光素子の全体構成を示す平面図であり、図１８は１つの積層部３１０を拡大して示す平面図である。また、図１９（ａ）は図１８のＥ－Ｅ’線についての断面図であり、図１９（ｂ）は図１８のＦ－Ｆ’線についての断面図である。

実施の形態６の窒化物半導体発光素子において、積層部３１０はそれぞれ円形形状に形成され、その中心が縦横とも１つの直線上に位置するように基板上に配列される。また、各積層部３１０の積層構造は他の実施の形態と同様であり、その外周側面は内側に傾いた傾斜面（外周傾斜面３１０ａ）とされ、その断面形状は、図１９（ａ）（ｂ）に示すように、上面を上底とする台形である。

【００４２】

各積層部３１０において、ｎオーミック電極３２１ａは外周傾斜面３１０ａに露出されたｎ側コンタクト層とオーミック接触するように外周傾斜面３１０ａの全周に形成される。また、積層部３１０の間の基板上にはそれぞれｎ接続パッド３２１ｂが形成され、各積層部３１０に形成されたｎオーミック電極３２１ａは隣接する４つのｎ接続パッド３２１ｂと接続される。

すなわち、実施の形態６の窒化物半導体発光素子において、ｎ電極３２１はｎオーミック電極３２１ａとｎ接続パッド３２１ｂとからなる。

また、各積層部３１０の上面（Ｐコンタクト層の上面）のほぼ全面に、全面電極３３１が形成され、その全面電極３３１の中央部に円形のＰパッド電極３３２が形成される。

【００４３】

以上のように、ｎオーミック電極３２１ａ、ｎ接続パッド電極３２１ｂ、全面電極３３１及びＰパッド電極３３２を形成した後、接続パッド電極３２１ｂとその周辺及びＰパッド電極３３２の上面を除いて素子全体を覆う絶縁膜３７１を形成して、各積層部３１０のＰパッド電極３３２を互いに接続するＰ側接続電極３６１を形成する。尚、Ｐ側接続電極３６１は、Ｐパッド電極３３２上に接続されたパッド接続部３６１ｂとそのパッド接続部３６１ｂ間を接続する接続部３６１とからなる。

【００４４】

以上のように構成された実施の形態６の窒化物半導体発光素子は、実施の形態１と同様、

電極による吸収を防止でき、発光した光の取り出し効率を高くできる。
実施の形態６の窒化物半導体発光素子における光の取り出し効率を確認するために以下の比較検討を行った。
【００４５】
まず、本実施の形態６の窒化物半導体発光素子として、図２５の平面図に示す積層部３１０を９個（３×３個）形成した素子を作製し、積層部３１０が１つの場合の発光素子（図２８の平面図に示す）と取り出し効率の比較を行った。
取り出し効率の測定は、図３０に示すように、マイナス側端子と一体で構成されたカップ内に発光素子をダイボンディングし、ｎパッド電極とマイナス側端子Ｔ２とをボンディングワイヤーＷ２１で接続し、Ｐパッド電極とプラス側端子Ｔ１とをボンディングワイヤーＷ３２で接続して、発光光量に対する外部に取り出される光量を測定した。
【００４６】
その結果、９個の積層部３１０を形成した実施の形態６の素子（図２５）の取り出し効率は、積層部３１０が１つの場合の発光素子（図２８）の取り出し効率を１００とした場合、８６％であった。
これに対して、比較例として作製した図２６に示す発光素子（９個の積層部を形成した素子）の取り出し効率は、図２９（ａ）に示す１つの積層部を備えた発光素子の取り出し効率を１００とした場合、７１％であった。
尚、積層部３１０が１つの場合の発光素子（図２８）の取り出し効率と、図２９（ａ）に示す１つの積層部を備えた発光素子の取り出し効率とはほぼ等しいものであった。
【００４７】
ここで、比較例の発光素子において、各積層部は実施の形態６と同様の積層構造を有し、その平面形状は略矩形に形成されている。また、ｎ電極５２１は、各積層部の１つの隅部において、ｎ型コンタクト層の表面を露出させ、その露出させた表面に形成されている。さらに、Ｐオーミック電極５３１はＰ型コンタクト層のほぼ全面に形成され、Ｐオーミック電極５３１上のｎ電極５２１と対角をなす位置にＰパッド電極５３２が形成されている。尚、図２６に示す素子では、隣接する積層部の間はサファイア基板が露出されるまでエッチングされて、隣接する積層部の間は完全に分離されている。また、各積層部の側面は、サファイア基板の上面に対してほぼ垂直に形成されている。
【００４８】
以上のように、複数の積層部を備えた実施の形態６の窒化物半導体発光素子は、同じく集合状態の比較例の窒化物半導体発光素子に比較して、取り出し効率を高くできることが確認された。
【００４９】
また、図２７は異なる比較例として作製した素子であって、図２６に示す比較例の発光素子において、隣接する積層部間においてサファイア基板が露出するまでエッチングせずに、ｎ型コンタクト層を残すようにしたものである。この図２７の比較例の素子の取り出し効率は、図２９（ｂ）に示す１つの積層部を備えた発光素子の取り出し効率を１００とした場合、６８％であった。
尚、図２９（ａ）の素子の取り出し効率と、図２９（ｂ）の素子の取り出し効率とはほぼ等しいものであった。
以上のように、複数の積層部を備えた比較例の発光素子は、いずれも実施の形態６の発光素子より取り出し効率が悪いものであった。
【００５０】
また、実施の形態６の窒化物半導体発光素子は、実施の形態５の発光素子と同様の作用効果を有し、さらに以下のような特徴を有する。
すなわち、ウエハ上に各積層部を形成した後に、要求に応じて必要な個数の積層部３１０を含む任意の大きさの素子に分割することができるので、同一のパターンにより任意の大きさの素子を作製することが可能となる。
尚、この場合、いずれかの位置にあるｎ接続パッド電極３２１ｂとパッド接続部３６１ｂ

とをボンディング電極として用いることができる。

【００５１】

以上の各実施の形態の窒化物半導体発光素子は、上述したように、基板側から光を出力するようにも構成できるし、また、半導体側から光を出力するようにも構成できる。いずれの場合についても、光を出射する方向の反対側の面には、反射層を形成することが好ましい。図７、図８及び図１６に示す構造の場合にはそれぞれ、ｎ電極２４、電極２６又は電極２６５を反射層として機能させることができることは上述した通りであるが、他の構成の場合には、反射層を別途設けることが好ましい。この反射層は、反射率の高い金属を用いて構成することもできるし、誘電体多層膜を用いて構成することもできる。誘電体多層膜を用いる場合には、例えば、図１８の絶縁層２７１を誘電体多層膜により構成することにより、絶縁機能に加え、反射機能を持たせるようにしても良い。

【００５２】

実施の形態７．

図３１は実施の形態７の窒化物半導体発光素子の全体構成を示す平面図である。実施の形態７の窒化物半導体発光素子において、積層部３１０はそれぞれ円形形状に形成され、その中心が単位格子が六角形の格子点に位置するように基板上に配置される。また、各積層部６１０の積層構造は他の実施の形態と同様であり、その外周側面は内側に傾いた傾斜面とされている。

【００５３】

各積層部６１０において、ｎオーミック電極６２１ａは外周傾斜面に露出されたｎ側コンタクト層とオーミック接触するように外周傾斜面の全周に形成される。また、６つの積層部６１０に囲まれた各六角形格子の中心には、それぞれｎ接続パッド６２１ｂが形成され、各積層部６１０に形成されたｎオーミック電極６２１ａは隣接する３つのｎ接続パッド６２１ｂと接続される。

すなわち、実施の形態７の窒化物半導体発光素子において、ｎ電極はｎオーミック電極６２１ａとｎ接続パッド６２１ｂとからなる。

また、各積層部６１０の上面（Ｐコンタクト層の上面）のほぼ全面に、全面電極が形成され、その全面電極の中央部に円形のＰパッド電極６３２が形成され、各積層部６１０のＰパッド電極６３２はＰ側接続電極３６１により互いに接続される。

【００５４】

尚、ｎオーミック電極６２１ａ、ｎ接続パッド電極６２１ｂ等のｎ側の電極と、全面電極６３１、Ｐパッド電極６３２、Ｐ側接続電極３６１等のＰ側の電極とは実施の形態６と同様にして絶縁される。

以上のように構成された実施の形態７の窒化物半導体発光素子では、１つのｎ接続パッド電極６２１ｂに対して２つの積層部が設けられており、１つのｎ接続パッド電極に対して１つの積層部が設けられた実施の形態６に比較して、発光素子全体としての発光領域の面積を大きくできる。

また、この実施の形態７のように積層部を配置した場合、外形形状が、三角形、六角形、ひし形、平行四辺形等になるように分割することができ、そのように分割する際、ＧａＮ結晶の結晶軸の方向とスクライブラインの方向を一致させることができるので、分割時の歩留まりを向上させることができる。

【００５５】

次に、上記各実施の形態の窒化物半導体発光素子において、傾斜側面を有する積層部の形成方法の一例を示す。

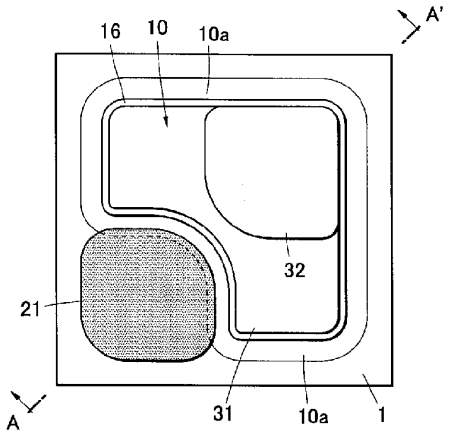
本方法では、まず、サファイア基板１の上に、バッファ層１１、ｎ型コンタクト層１２、ｎ型クラッド層１３、発光層１４、Ｐ型クラッド層１５及びＰ型コンタクト層１６を順次成長させて積層構造を形成し、その上に、図２０（ａ）に示すように、断面が台形形状のマスクＭ１を形成する。

次に、反応性イオンエッチングにより、マスクＭ１の上から積層体をエッチングする。この時、積層体をエッチングすると同時にマスクそのものもエッチングにより少しづつ除去

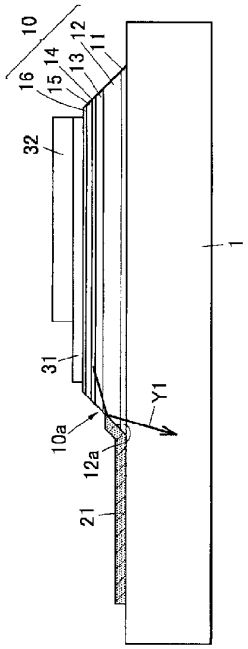
する。図２０（ｂ）において、破線と実線の間のＲ１の符号を付した部分が除去された部分である。
この工ッチングを積層部１０の周りの基板表面が露出されるまで続ける（図２０（ｃ））。
このようにすると、マスクＭ１の形状に対応した形状の、傾斜側面１０αを有する積層部１０が形成される。
本方法では、マスク材料と窒化物半導体材料のＲＩＥによる工ッチング率を考慮して、マスクＭ１形状を設定することにより、所望の傾斜側面を有する積層部が形成できる。
【００５６】
例えば、マスクＭ１の側面を外側に膨らんだ形状とすることにより、積層部の傾斜側面を外側に膨らんだ凸曲面とすることができる。
このように、傾斜側面を外側に膨らんだ凸曲面とすることにより、基板側から光を出力する場合に集光して光を出射できる。
【００５７】
以上の各実施の形態では、最も好ましい例として、積層部の周りを基板まで工ッチングした例を用いて説明したが、本発明においては積層部の周りに光が伝送されないようにすることが重要であり、光の伝送を抑制できる程度の厚さにｎ型半導体層が残っていても良い。
【００５８】
【発明の効果】
以上詳細に説明したように、本発明に係る窒化物半導体発光素子は、傾斜した側面を持った積層部を有し、その積層部の側面のｎ型半導体層の表面にｎ電極を形成することによりｎ電極による光の吸収を抑制でき、光の出射効率を高くできる。
【図面の簡単な説明】
【図１】本発明に係る実施の形態１の発光素子の平面図である。
【図２】図１のＡ－Ａ’線についての断面図である。
【図３】本発明に係る実施の形態１の変形例の発光素子の平面図である。
【図４】図３のＢ－Ｂ’線についての断面図である。
【図５】本発明に係る実施の形態２の発光素子の平面図である。
【図６】本発明に係る実施の形態３の発光素子の平面図である。
【図７】図６のＣ－Ｃ’線についての断面図である。
【図８】実施の形態３の変形例に係る発光素子の断面図である。
【図９】本発明に係る実施の形態４の発光素子の平面図である。
【図１０】実施の形態４の変形例に係る発光素子の平面図である。
【図１１】本発明に係る実施の形態５の発光素子において、Ｐ側の電極を省いて示す平面図である。
【図１２】本発明に係る実施の形態５の発光素子の平面図（Ｐ側の電極を含む）である。
【図１３】図１２のＤ－Ｄ’線についての断面図である。
【図１４】実施の形態５の第１変形例に係る発光素子の平面図である。
【図１５】実施の形態５の第２変形例に係る発光素子の平面図である。
【図１６】実施の形態５の第３変形例に係る発光素子の平面図である。
【図１７】本発明に係る実施の形態６の発光素子の平面図である。
【図１８】図１７の一部を拡大して示す平面図である。
【図１９】（ａ）は図１８のＥ－Ｅ’線についての断面図であり、（ｂ）は図１８のＦ－Ｆ’線についての断面図である。
【図２０】本発明の窒化物半導体発光素子において、傾斜側面を有する積層部の形成方法の一例を示す工程図である。
【図２１】従来例の発光素子の断面図である。
【図２２】本発明の窒化物半導体発光素子において、傾斜側面の好ましい傾斜角について説明するための模式図である。

【図２３】本発明の窒化物半導体発光素子において、Ｐ電極による光の吸収が抑制できることを説明するための図である。
【図２４】実施の形態５の第４変形例に係る発光素子の平面図である。
【図２５】本発明に係る実施の形態６において、取り出し効率の測定に用いた発光素子の平面図である。
【図２６】本発明に係る実施の形態６の比較例（その１）として、取り出し効率の測定に用いた発光素子の平面図である。
【図２７】本発明に係る実施の形態６の比較例（その２）として、取り出し効率の測定に用いた発光素子の平面図である。
【図２８】本発明に係る実施の形態６の取り出し効率の測定において、基準として用いた発光素子の平面図である。
【図２９】本発明に係る実施の形態６において、比較例の基準として用いた発光素子の平面図である。
【図３０】本発明に係る実施の形態６の取り出し効率の測定方法の概要を示す模式図である。
【図３１】本発明に係る実施の形態７の発光素子の平面図である。
【図３２】実施の形態７の発光素子の一部を拡大して示す平面図である。
【符号の説明】
１　サファイア基板、
１０，１１０，１１１，２１０，３１０　積層部、
１０ａ，１１０ａ，１１１ａ，２１０ａ，３１０ａ　傾斜面（傾斜側面）、
１１　バッファ層、
１２　ｎ型コンタクト層、
１３　ｎ型クラッド層、
１４　発光層、
１５　Ｐ型クラッド層、
１６　Ｐ型コンタクト層、
２１，２２，２３，２４，２５，２７，２８，２２１，３２１　ｎ電極、
３１，３３，３５　全面電極、
３２，３４，３６　Ｐパッド電極、
３３ａ　透光性オーミック電極。

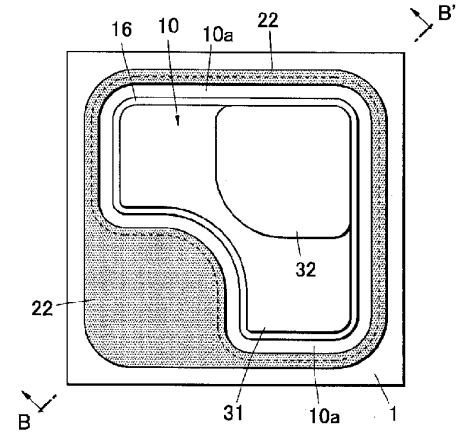
【図１】


16
10
10a
A'
32
21
A
31
10a
1

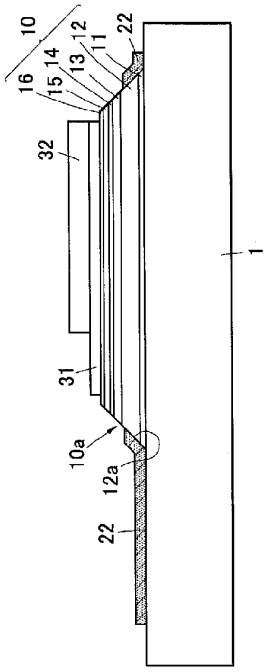
【図２】


10
12
11
14
13
16
15
32
1
31
Y1
10a
12a
21

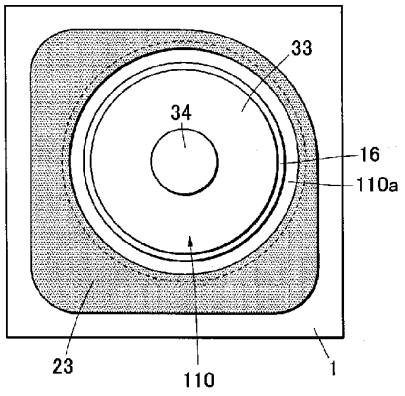
【図３】


16
10
10a
22
B'
32
22
B
31
10a
1

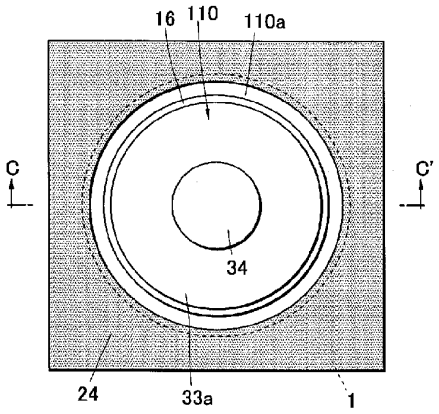
【図４】


10
12
11
22
14
13
16
15
32
1
31
10a
12a
22

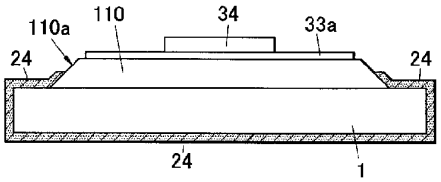
【図５】



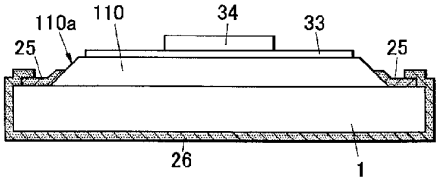
【図６】



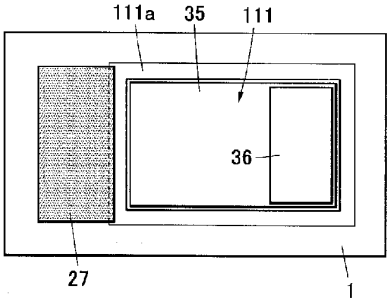
【図７】



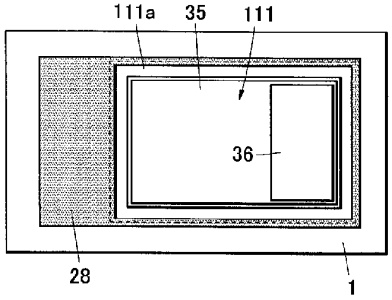
【図８】



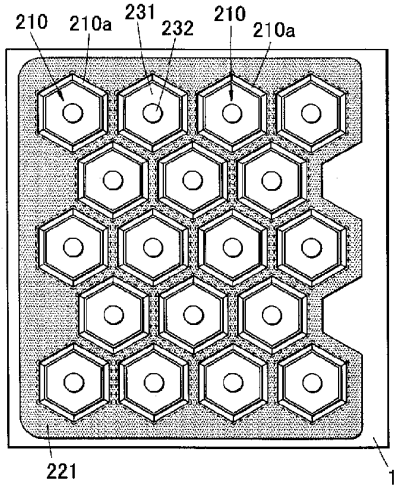
【図９】



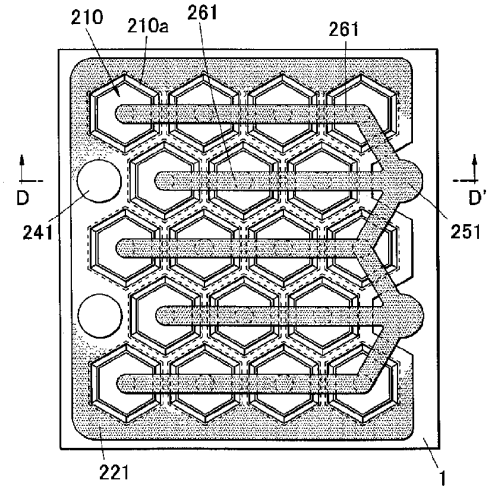
【図１０】



【図１１】

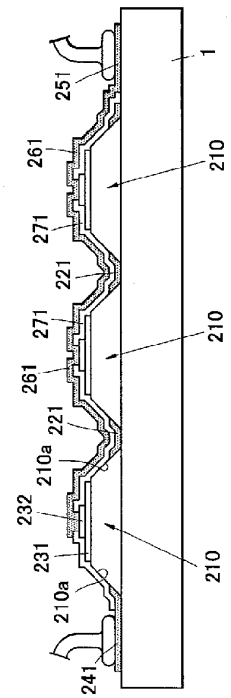


【図１２】

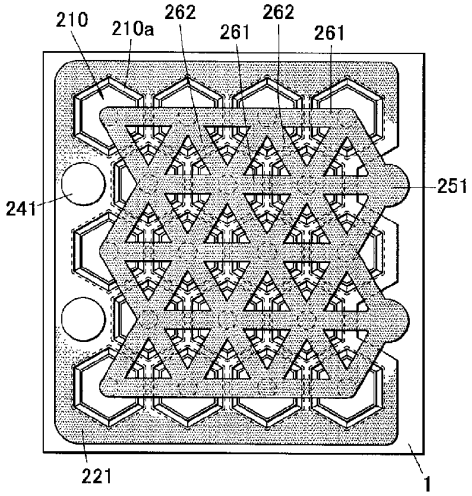


素子間接続Pパターン

【図１３】

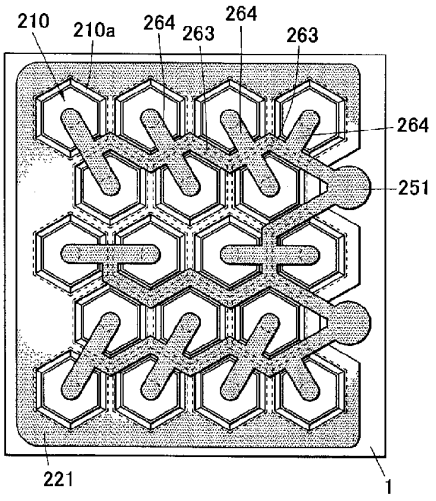


【図１４】



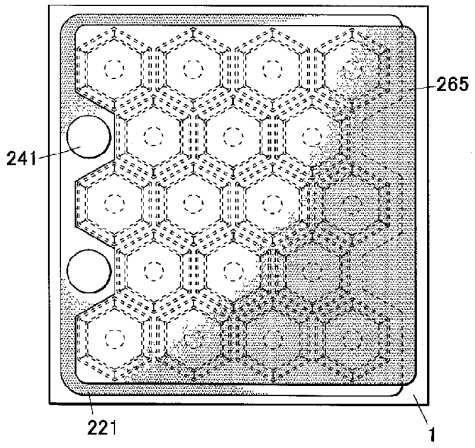
p配線例その２

【図１５】



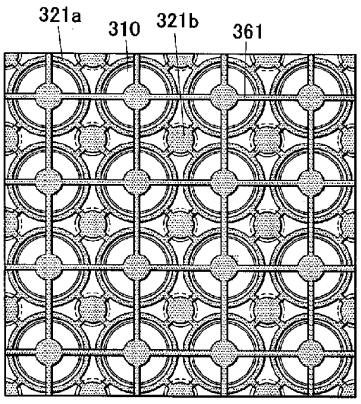
配線例4

【図１６】

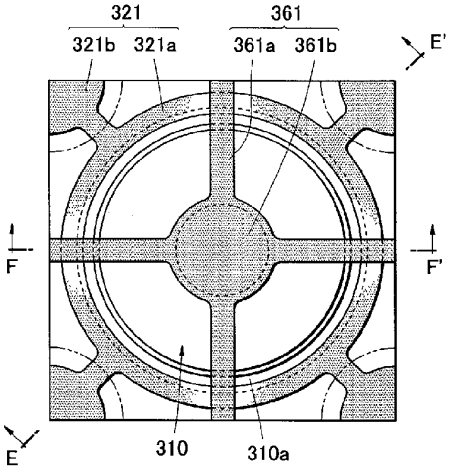


P配線例その3(FD対応型)

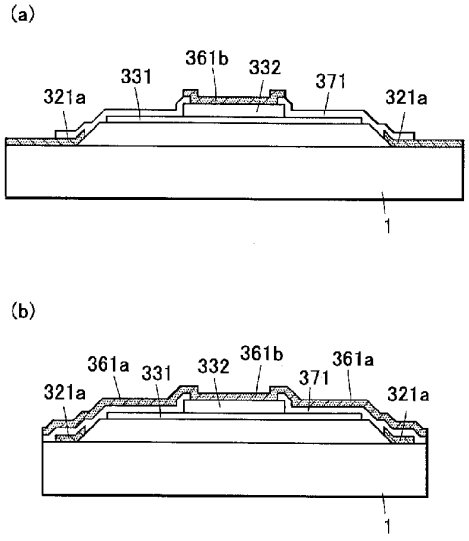
【図１７】



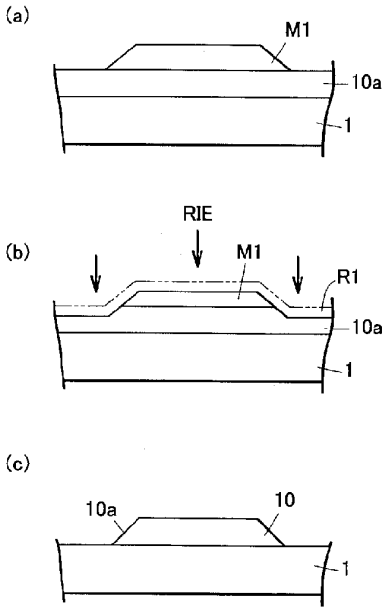
【図１８】



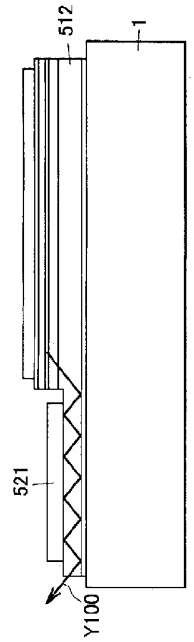
【図１９】



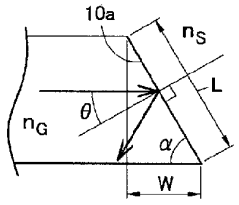
【図２０】



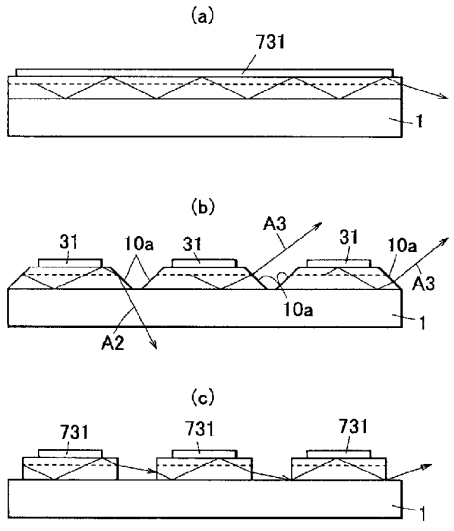
【図２１】



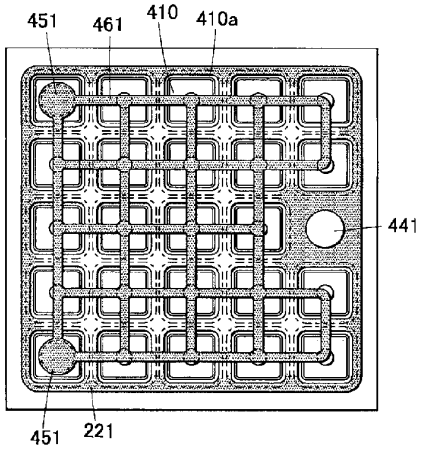
【図２２】



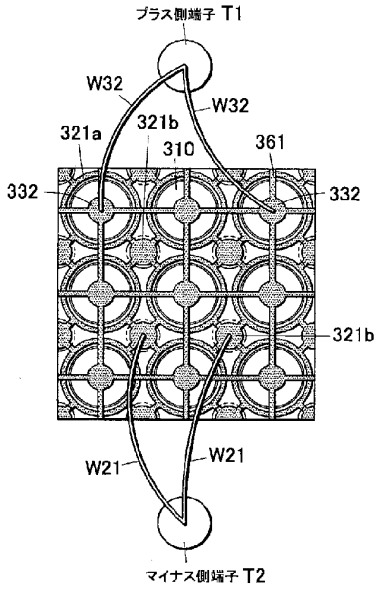
【図２３】



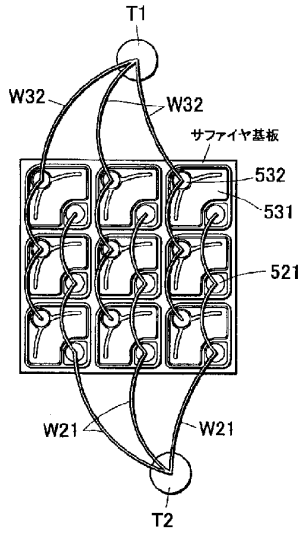
【図２４】



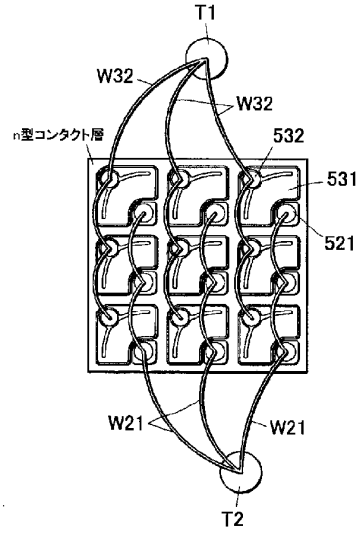
【図２５】



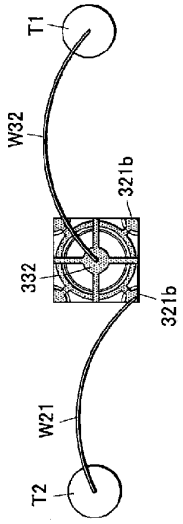
【図２６】



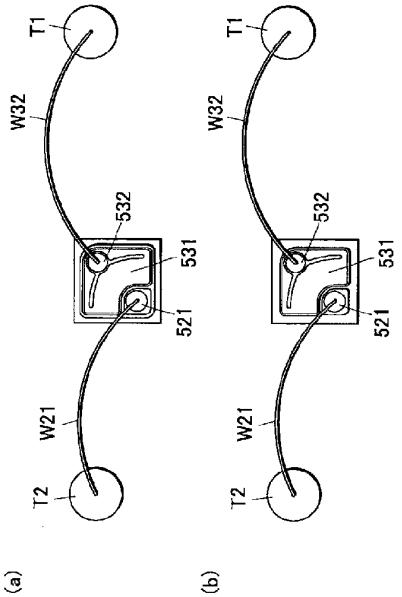
【図２７】



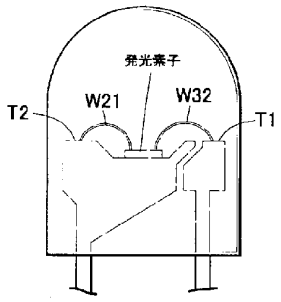
【図２８】



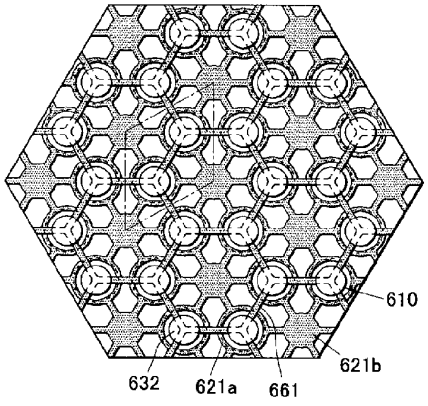
【図２９】



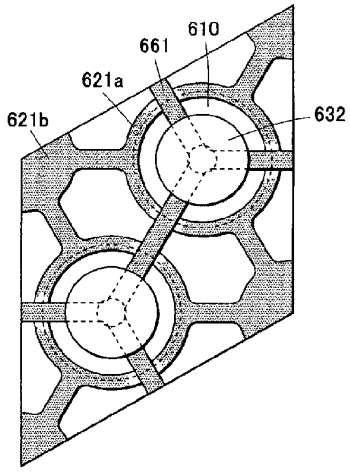
【図３０】



【図３１】



【図３２】



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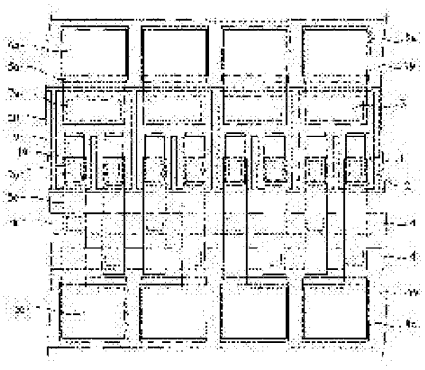
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(54) LIGHT-EMITTING DIODE ARRAY

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a light emitting diode array capable of preventing the short-circuit of a wiring due to the residue of Au of working which is generated on the slanted surface of a level difference of mesa etching, and easy in the size control of a light emitting part while high in an yield and excellent in manufacturability.
SOLUTION: The light emitting diode array is provided with a conductive layer formed on a substrate, individually independent light emitting units formed on the conductive layer, first electrodes formed at least on one part of the upper surface of respective light emitting units and second electrodes formed on the conductive layer adjacent to the light emitting units. In such a light emitting diode array, the first electrodes are provided with a matrix common electrode for switching while the second electrodes are provided with a common electrode partitioned for every blocks. At least one of bonding pads extended from the first common electrode and the second common electrode is provided on a bonding unit formed on the conductive layer like an island, whereby respective bonding pads are formed independently.



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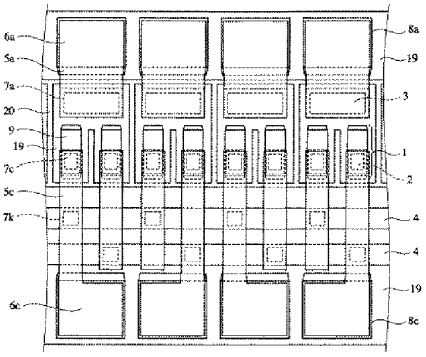
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最終頁に続く

(54)【発明の名称】発光ダイオードアレイ

(57)【要約】
【課題】メサエッチング段差の斜面部分に発生するＡｕの加工残りによる配線短絡を防止するとともに発光部の寸法制御が容易で、高歩留、かつ量産性に優れた発光ダイオードアレイを提供する。
【解決手段】基板上に形成された導電層と、前記導電層上に形成された個々独立の発光部と、各発光部の上面の少なくとも一部に形成された第一の電極と、前記発光部に近接して前記導電層上に形成された第二の電極とを有する発光ダイオードアレイにおいて、前記第一の電極はスイッチ用のマトリクス共通電極を有し、前記第二の電極はブロック毎に分割された共通電極を有する発光ダイオードアレイであって、前記第一の共通電極及び前記第二の共通電極に延在するボンディングパッドの少なくとも一方は、前記導電層上に島状に形成されたボンディング部上に設けられており、もって前記ボンディングパッドは個々独立に形成されていることを特徴とする。
【選択図】　図１



【特許請求の範囲】
【請求項1】
基板上に形成された導電層と、前記導電層上に形成された個々独立の発光部と、各発光部の上面の少なくとも一部に形成された第一の電極と、前記発光部に近接して前記導電層上に形成された第二の電極とを有する発光ダイオードアレイにおいて、前記第一の電極はスイッチ用のマトリクス共通電極を有し、前記第二の電極はブロック毎に分割された共通電極を有する発光ダイオードアレイであって、前記第一の共通電極及び前記第二の共通電極に延在するボンディングパッドの少なくとも一方は、前記導電層上に島状に形成されたボンディング部上に設けられており、もって前記ボンディングパッドは個々独立に形成されていることを特徴とする発光ダイオードアレイ。
【請求項2】
請求項１に記載の発光ダイオードアレイにおいて、前記第一電極側及び前記第二電極側のボンディングパッドのどちらか一方は、メサエッチング溝部に設けられた絶縁膜上に形成されていることを特徴とする発光ダイオードアレイ。
【請求項3】
請求項１又は２に記載の発光ダイオードアレイにおいて、前記マトリクス共通電極はメサエッチング溝部に設けられた絶縁膜上に形成されていることを特徴とする発光ダイオードアレイ。

【発明の詳細な説明】
【０００１】
【発明の属する技術分野】
本発明は発光出力の大きい発光ダイオードアレイに関し、特に電子写真方式のプリンタ光源に好適な発光ダイオードアレイに関する。
【０００２】
【従来の技術】
電子写真方式のプリンタは、画像信号に応じた光により感光ドラム上に静電潜像を形成し、トナーを選択的に付着させて現像した後、紙に転写して画像を得る。潜像を形成するための光源としてはレーザ方式と発光ダイオードアレイ方式が広く用いられている。特に発光ダイオードアレイ方式の光源は、レーザ方式のように光路長を長くとる必要がないため、小型のプリンタや大サイズの印刷に適している。近年は印刷の高速・高画質化やプリンタの更なる小型化にともない、より高精細で高出力、かつ低コストの発光ダイオードアレイが求められている。
【０００３】
一般に、低コストを実現するためには、個々独立に発光ダイオードを駆動させるＩＣを備える方法（スタティック駆動方式）ではなく、２のｎ乗個の発光ダイオードを１つのブロックとし、スイッチ用のマトリクス配線を用いて時間分割駆動させ、駆動ＩＣやボンディング本数を削減する方法（ダイナミック駆動方式）が用いられている。このような発光ダイオードアレイを製造するプロセスにおいて、配線材料としてはＴｉ／ＡｕやＭｏ／Ａｕが広く用いられている。この配線を形成する方法としては、リフトオフ法（フォトレジストでパターンニング後、電子線蒸着し、不要部分をレジストと共に除去する方法）と、スパッタ～イオンミリング加工法（スパッタでウェーハ全体にＴｉ／ＡｕやＭｏ／Ａｕを沈着させた後、パターンニングされたフォトレジストやSiO_2等の絶縁膜からなるマスク材を物理的に削る方法）が用いられる。リフトオフ法ではステップカバレジが悪いのでメサエッチング段差が大きいＬＥＤでは配線層が段切れし易い。また、スパッタ～イオンミリング加工法の場合、ステップカバレジが良好で段切れが起き難い反面、メサエッチング段差部にＡｕ加工残りが発生し易いという欠点がある。特に共通電極を有するダイナミック駆動式のＬＥＤでは、このＡｕの加工残りによって、配線が短絡し、所望しないＬＥＤが発光してしまうという問題があった。
【０００４】
図４は、従来の２分割ダイナミック駆動方式の発光ダイオードアレイを示す上面図であり

、図５（ａ）は図４のうちのひとつのブロックを示す上面図である。図５（ｂ）は図５（ａ）のＡ－Ａ断面図であり、図５（ｃ）は図５（ａ）のＢ－Ｂ断面図である。ｎ型ＧａＡｓ基板１０上に形成されたｐ型ＧａＡｓ導電層１１の上に所定間隔で複数の発光部１が配置されている。各発光部１は、ｐ型ＧａＡｓ導電層１１の上に順次積層されたｐ型ＡｌＧａＡｓエッチングストッパ層１２、ｐ型ＡｌＧａＡｓクラッド層１３、ｐ型ＡｌＧａＡｓ活性層１４、ｎ型ＡｌＧａＡｓクラッド層１５及びｎ型ＧａＡｓキャップ層１６からなる。発光部１の発光領域は、ｐ型ＡｌＧａＡｓクラッド層１３、ｐ型ＡｌＧａＡｓ活性層１４及びｎ型ＡｌＧａＡｓクラッド層１５からなるダブルヘテロ構造を有する。

【０００５】

各発光部１はエピタキシャル層をメサエッチングにより除去することにより形成されている。メサエッチング溝は、発光部１とボンディング部８とを分離する第一のメサエッチング溝部１９と各ブロックを分割する役割を有する第二のメサエッチング溝部２０とからなる。

【０００６】

各発光部１の上面の一部にカソード電極２が形成されている。発光部１に近接してｐ型ＧａＡｓ導電層１１上に各ブロック毎に設けられているアノード電極３はｐ型ＧａＡｓ導電層１１の上にそれぞれ金属を蒸着・合金化することにより形成される。カソード電極２及びアノード電極３の各々のコンタクト孔７ｃ、７ａを除いて、発光部１及び露出した導電層１１の表面はＰＳＧ（リンガラス）等からなる第一絶縁膜１７により覆われている。共通電極４はカソード側のボンディング部（メサ頂面）８ｃを覆う第一絶縁膜１７上に設けられ、更に第二絶縁膜を被覆した後、この第二絶縁膜により覆われていないカソード電極２に一端部が接続するようにＡｕ配線層５ｃが形成されており、Ａｕ配線層５ｃはボンディング部８ｃの表面まで延在して共通電極４の所望部分と接続し、その他端部にはボンディングパッド６ｃが形成されている。一方、アノード電極３に一端部が接続するようにＡｕ配線層５ａが形成されており、Ａｕ配線層５ａはボンディング部（メサ頂面）８ａの表面まで延在し、Ａｕ配線層５ａの他端部にはボンディングパッド６ａが形成されている。

【０００７】

このような構造の発光ダイオードアレイは、Ａｕ配線層５を形成する方法にスパッタ～イオンミリング法を用いたとき、第一のメサエッチング溝の斜面２１にはイオンミリングによるＡｕ残りが発生し易く、Ａｕ配線の短絡を防止するうえで満足できるものではない（例えば、特許文献１参照。）。この問題は、発光部１を除く全てを第一メサエッチング溝として除去し、メサエッチング溝部の底面に配線層、共通電極及びボンディングパッドを形成すれば解決できるが、その場合には異なる問題が発生する。すなわち、発光部１を残して全てをエッチングすると、エッチング面積の大きい部分と各発光部間のエッチング面積の小さい部分の差が広がる。エッチングプロセスにおいてエッチング速度には面積依存性があるため（ローディング効果）、性能に影響する発光部の寸法制御が極めて困難になる。

【０００８】

特許文献２には半導体基板の一部に凹部を設け、この凹部内に共通電極を形成した発光ダイオードアレイが開示されている。しかしながら、この方式では共通電極部分のみが凹部内に形成されているため、メサエッチング溝の斜面に発生したＡｕ残りにより短絡が発生しやすい。

【０００９】

【特許文献１】

特開２０００－３２３７５０号公報

【特許文献２】

特開平１０－１５７１９３号公報

【００１０】

【発明が解決しようとする課題】

従って本発明の目的は、メサエッチング段差の斜面部分に発生するＡｕの加工残りによる

配線短絡を防止するとともに発光部の寸法制御が容易で、高歩留、かつ量産性に優れた発光ダイオードアレイ及びその製造プロセスを提供することである。

【００１１】

【課題を解決するための手段】

上記目的に鑑み鋭意研究の結果、本発明者らは、ボンディングパッドをメサエッチング溝によって独立したボンディング部（メサ頂面）上に形成することにより、Ａｕの加工残りによる配線短絡を防止できることを発見し、本発明に想到した。

【００１２】

すなわち、本発明の発光ダイオードアレイは、基板上に形成された導電層と、前記導電層上に形成された個々独立の発光部と、各発光部の上面の少なくとも一部に形成された第一の電極と、前記発光部に近接して前記導電層上に形成された第二の電極とを有し、前記第一の電極はスイッチ用のマトリクス共通電極を有し、前記第二の電極はブロック毎に分割された共通電極を有する発光ダイオードアレイであって、前記第一の共通電極及び前記第二の共通電極に延在するボンディングパッドの少なくとも一方は、前記導電層上に島状に形成されたボンディング部上に設けられており、もって前記ボンディングパッドは個々独立に形成されていることを特徴とする。

【００１３】

前記第一電極側及び前記第二電極側のボンディングパッドのどちらか一方は、メサエッチング溝部に設けられた絶縁膜上に形成されていてもよい。また、前記マトリクス共通電極はメサエッチング溝部に設けられた絶縁膜上に形成されているのが好ましい。

【００１４】

本発明の発光ダイオードアレイにおいて、発光部及びボンディング部は導電層上に形成されたエピタキシャル層をメサエッチング溝により個々独立・分割してなるのが好ましい。好ましい実施例による発光ダイオードアレイでは、ボンディングパッドは個々独立のボンディング部上に形成されているために、メサエッチング溝の斜面にＡｕ配線を残してもボンディングパッド間で短絡することがない。また、ボンディング部は第一のメサエッチング溝により残されたエピタキシャル層上に形成されているので、エッチング面積を増大させることがない。これによりローディング効果を避けることができ、同じく第一のメサエッチング溝により残されたエピタキシャル層である発光部の寸法制御が容易となる

【００１５】

【発明の実施の形態】

［１］　発光ダイオードアレイの構造

図１及び図２に示すように、本発明の発光ダイオードアレイは、基板１０、基板１０上に形成された複数の発光部１、各発光部１の上面に部分的に形成された第一の電極２、及び発光部１に近接する位置で導電層１１上に形成された第二の電極３を有する。図示の実施例では、各発光部１は基板１０上に均一に形成されたエピタキシャル層にメサエッチング溝部１９、２０を設け、個々独立のエピタキシャル層部としたものである。

【００１６】

（１）　基板

基板１０は、発光ダイオード用に使用し得るものであれば特に限定されず、発光部と電気的に絶縁できる構造であればよい。ｎ型基板でもｐ型基板でも用いることができ、半絶縁性ＧａＡｓ基板等の半絶縁性基板または絶縁性基板を用いてもよい。基板１０と導電層１１との間にアンドープＧａＡｓ層等の高抵抗層を設けて絶縁することもでき、また導電層１１に対して逆の極性を有する半導体層を設けて絶縁することもできる。

【００１７】

（２）　発光部

基板１０の導電層１１上に積層する化合物半導体の種類や結晶層の厚さは、所望の発光波長及び発光出力により適宜選択する。化合物半導体としては、例えばＡｌＧａＡｓ、ＡｌＧａＩｎＰ等を用いることができる。発光部１は第一導電型のクラッド層、活性層及び第二導電型のクラッド層からなるダブルヘテロ構造を有するのが好ましく、導電層上に形成

したエピタキシャル層を第一のメサエッチング溝により分割してなるのが好ましい。さらに、第二のメサエッチング溝２０は各ブロック間を分離するために導電層１１を分断している。

【００１８】

図示の実施例では、発光ダイオードアレイの発光部１は、ｎ型ＧａＡｓ基板１０の上にｐ型ＧａＡｓ導電層１１を介して順次形成されたｐ型ＡｌＧａＡｓエッチングストッパ層１２、ｐ型ＡｌＧａＡｓクラッド層１３、ｐ型ＡｌＧａＡｓ活性層１４、ｎ型ＡｌＧａＡｓクラッド層１５及びｎ型ＧａＡｓキャップ層１６からなる。ｎ型ＧａＡｓキャップ層１６は、光取り出し部９の領域ではエッチングにより除去されている。Ａｕ配線層５との短絡防止のため、第一及び第二絶縁膜１７、１８がカソード電極２を除いて発光部２の表面全体を覆っている。

【００１９】

上記発光部１のうち発光に直接関与する領域は、発光波長に対応するエネルギーバンドギャップを有するｐ型ＡｌＧａＡｓ活性層１４を、それよりもエネルギーバンドギャップの大きいｐ型ＡｌＧａＡｓクラッド層１３（第一導電型のクラッド層）及びｎ型ＡｌＧａＡｓクラッド層１５（第二導電型のクラッド層）で挟んだ、いわゆるダブルヘテロ構造を有する。

【００２０】

（３）　電極及び配線層

第一及び第二電極の一方がカソード電極で、他方がアノード電極であればよく、例えば第一の電極はカソード電極でもアノード電極でもよい。各電極はボンディング特性、下層とのオーミック接続特性が要求される。例えばアノード電極にＡｕＺｎ／Ｎｉ／Ａｕの積層電極を使用し、カソード電極にＡｕＧｅ／Ｎｉ／Ａｕ等の積層電極を使用する。

【００２１】

共通電極及びＡｕ配線層はボンディング特性、上層・下層との密着性が良好であることが要求されるため複数の金属層で構成されるのが好ましい。最上層及び最下層にはボンディング特性及び絶縁膜の接着性が良いＴｉ，Ｍｏ等の金属層を有するのが好ましい。例えば、共通電極としてＴｉ／Ａｕ／Ｔｉ、Ｍｏ／Ａｕ／Ｍｏ、ＴｉＷ／Ａｕ／ＴｉＷ等の積層電極を使用することができる。

【００２２】

各電極の金属層は抵抗加熱蒸着法、電子線加熱蒸着法、スパッタ法等で形成することができ、酸化物層は各種公知の成膜方法で形成することができる。カソード及びアノード金属層には、オーミック性を付与するため熱処理（合金化）をさらに施すのが好ましい。

【００２３】

図１及び図２に示す実施例では、各発光部１のメサ頂面にカソード電極２が形成されており、各発光部１側面及びカソード電極２周辺部は第一絶縁膜１７で覆われている。各発光部１上のカソード電極２は、コンタクト孔７によりＡｕ配線層５ｃを経由して２本の共通電極４のうち何れか一本と接続しており、個々独立したボンディング部８ｃ上にボンディングパッド６ｃを形成している。一方、各発光部１に近接する位置にアノード電極３がｐ型ＧａＡｓ導電層１１上に形成され、オーム接触している。アノード電極３は、Ａｕ配線層５ａを経由して、ボンディング部８ａのメサ頂面のボンディングパッド６ａに接続している。

【００２４】

（４）　メサエッチング溝

個々独立の発光部１及びボンディング部８を形成するため第一のメサエッチング溝部１９は、発光部１とボンディング部８とを電気的に分離するため導電層１１又はエッチングストッパ層１２まで達する第一のメサエッチング溝部１９と、発光部１の各ブロックを分断する目的で導電層１１を除去する第二のメサエッチング溝部２０とからなる。本発光ダイオードアレイの特徴的な要素である第一のメサエッチング溝部１９は発光部１を形成するほかに、個々独立のボンディング部８を形成している。

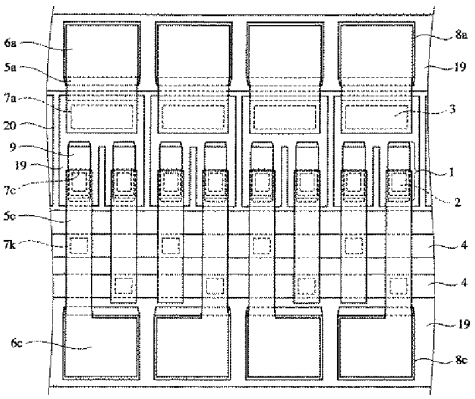
【００２５】
［２］　発光ダイオードアレイの製造方法
本発明の発光ダイオードアレイは、第一のメサエッチング溝部１９により個々独立のボンディング部８を形成する以外、従来と同じ方法により製造することができる。好ましい製造例としては、まず有機金属気相成長法（ＭＯＶＰＥ法）によりｎ型ＧａＡｓ基板１０の上面に、ｐ型ＧａＡｓ導電層１１（キャリア濃度：４×１０^{19}ｃｍ$^{-3}$、厚さ：１μｍ）、ｐ型ＡｌＧａＡｓエッチングストッパ層１２（キャリア濃度：３×１０^{19}ｃｍ$^{-3}$、厚さ：０．１μｍ）、ｐ型ＡｌＧａＡｓクラッド層１３（キャリア濃度：１×１０^{18}ｃｍ$^{-3}$、厚さ：１μｍ）、ｐ型ＡｌＧａＡｓ活性層１４（キャリア濃度：１×１０^{18}ｃｍ$^{-3}$、厚さ：１μｍ）、ｎ型ＡｌＧａＡｓクラッド層１５（キャリア濃度：２×１０^{18}ｃｍ$^{-3}$、厚さ：３μｍ）、及びｎ型ＧａＡｓキャップ層１６（キャリア濃度：１×１０^{18}ｃｍ$^{-3}$、厚さ：０．５μｍ）を順次成長させる。
【００２６】
形成した結晶層にウェットエッチングを選択的に施す。まずカソード電極２と接触する部分を残して発光部１のｎ型ＧａＡｓキャップ層１６を除去する。次に、ｐ型ＡｌＧａＡｓエッチングストッパ層１２が露出する深さにメサエッチング溝１９を設けて、ｐ型ＧａＡｓ導電層１１上のエピタキシャル層を複数の発光部１に分割するとともに、発光部１と個々独立したボンディング部８とを形成する。このとき、ローディング効果を回避できるのであれば、図３に示すようにどちらか一方のボンディング部は除去してしまっても良い。さらに第二のメサエッチング溝部２０によりｐ型ＧａＡｓ導電層１１を除去し、発光部１の各ブロックを電気的に分離する。このときのｎ型ＧａＡｓ基板１０も僅かにエッチングされるように第二のメサエッチング溝部２０の深さを設定すれば、エッチング誤差があっても導電層１１が残留することはない。
【００２７】
次いで、カソード電極２（ＡｕＧｅ／Ｎｉ／Ａｕ）及びアノード電極３（ＡｕＺｎ／Ｎｉ／Ａｕ）をそれぞれ蒸着～リフトオフ法により形成する。次に発光ダイオードアレイの上面全体を覆うように化学気相成長法（ＣＶＤ法）により第一絶縁膜１７を成長させた後、共通電極４（Ｔｉ／Ａｕ／Ｔｉ）を蒸着～リフトオフ法で形成する。さらにＣＶＤ法により第二絶縁膜１８を成長させた後、カソード電極２、アノード電極３と２本の共通電極のうち所望の一方にコンタクト孔をエッチングにより設け、Ｔｉ／Ａｕをスパッタ～イオンミリングにより、各々のボンディング部８まで延在するＡｕ配線層５を形成する。
【００２８】
ここでは共通電極を２本とした２×２構造の例を述べたが、４つの発光部を１ブロックとして４本の共通電極を持つ４×４構造でも、８×８、１６×１６…の構造でも同様である。
【００２９】
【発明の効果】
以上詳述したように、本発明の発光ダイオードアレイではボンディング部がメサエッチング溝により個々独立に形成されるので、メサエッチング溝の斜面にＡｕ配線層が残っても、或いは意図的にメサエッチング斜面をＡｕ配線層で被覆するような設計にしても配線が短絡することがなく、かつ発光部の寸法制御が容易で、高歩留の量産プロセスを提供することができる。
【図面の簡単な説明】
【図１】本発明の一実施例による発光ダイオードアレイを示す上面図である。
【図２】図１の発光ダイオードアレイを構成する単一セルを示し、（ａ）は上面図であり、（ｂ）は（ａ）のＡ－Ａ断面図であり、（ｃ）は（ａ）のＢ－Ｂ断面図である。
【図３】本発明の別の実施例による発光ダイオードアレイを構成する単一セルを示し、（ａ）は上面図であり、（ｂ）は（ａ）のＡ－Ａ断面図である。
【図４】従来の発光ダイオードアレイを示す上面図である。
【図５】図４の発光ダイオードアレイを構成する単一セルを示し、（ａ）は上面図であり

、（ｂ）は（ａ）のＡ－Ａ断面図であり、（ｃ）は（ａ）のＢ－Ｂ断面図である。

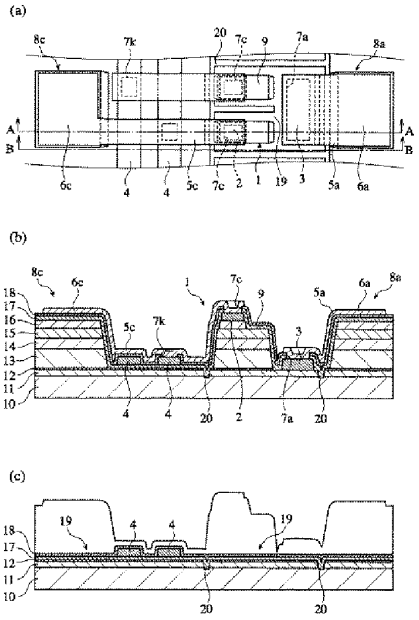
【符号の説明】

１・・・発光部
２・・・カソード電極
３・・・アノード電極
４・・・共通電極
５・・・Ａｕ配線層
５ａ・・・アノード側
５ｃ・・・カソード側
６・・・ボンディングパッド
６ａ・・・アノード側
６ｃ・・・カソード側
７・・・コンタクト孔
７ａ・・・アノード側
７ｃ・・・カソード側
７ｋ・・・共通電極上コンタクト孔
８・・・ボンディング部
８ａ・・・アノード側
８ｃ・・・カソード側
９・・・光取り出し部
１０・・・（ｎ型ＧａＡｓ）基板
１１・・・（ｐ型ＧａＡｓ）導電層
１２・・・ｐ型ＡｌＧａＡｓエッチングストッパ層
１３・・・ｐ型ＡｌＧａＡｓクラッド層
１４・・・ｐ型ＡｌＧａＡｓ活性層
１５・・・ｎ型ＡｌＧａＡｓクラッド層
１６・・・ｎ型ＧａＡｓキャップ層
１７・・・第一絶縁膜
１８・・・第二絶縁膜
１９・・・第一のメサエッチング溝部
２０・・・第二のメサエッチング溝部
２１・・・第一のメサエッチング溝の斜面

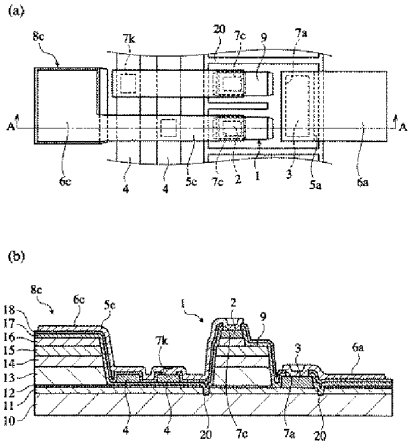
【図1】


6a
5a
7a
20
9
19
7c
5c
7k
6c
8a
19
3
1
2
4
4
19
8c

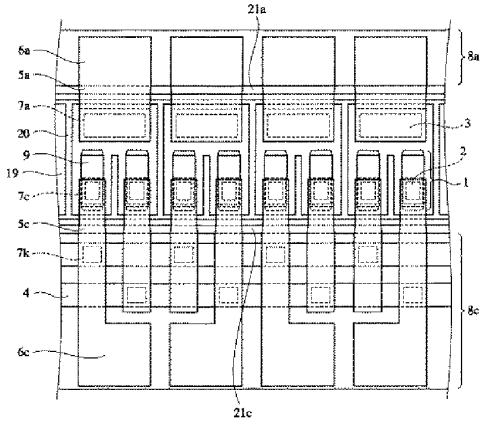
【図2】


(a)
8c
7k
20
7c
9
7a
8a
A
B
6c
4
4
5c
7c
2
1
19
3
5a
6a
(b)
8c
6c
1
7c
9
5a
6a
8a
18
17
16
15
14
13
12
11
10
5c
7k
3
4
4
20
2
7a
20
(c)
19
4
4
19
18
17
12
11
10
20
20

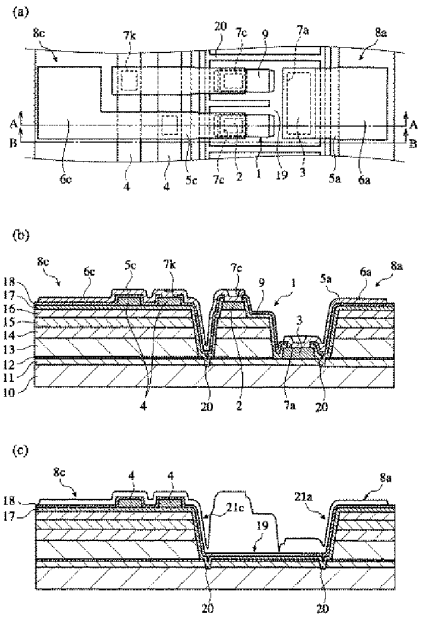
【図3】


(a)
8c
7k
20
7c
9
7a
A
A
6c
4
4
5c
7c
2
1
3
5a
6a
(b)
8c
6c
5c
1
2
9
18
17
16
15
14
13
12
11
10
7k
3
6a
4
4
20
7c
7a
20

【図4】


21a
6a
5a
7a
20
9
19
7c
5c
7k
4
6c
21c
8a
3
2
1
8c

【図5】


(a)
8c
7k
20
7c
9
7a
8a
A
B
6c
4
4
5c
7c
2
1
19
3
5a
6a
(b)
8c
6c
5c
7k
7c
9
1
5a
6a
8a
18
17
16
15
14
13
12
11
10
4
20
2
7a
20
3
(c)
8c
4
4
8a
18
17
21c
19
21a
20
20

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CB11　CB25　DB07　FF13

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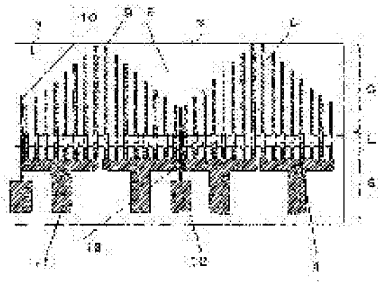
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B41J 2/45
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(22)Date of filing : 30.10.2003

(71)Applicant : KYOCERA CORP
(72)Inventor : KITADA KATSUNOBU

(54) LIGHT EMITTING DIODE ARRAY DEVICE AND LIGHT EMITTING DIODE PRINTER USING IT

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a light emitting diode array device that can reduce the variation of the resistances of electrodes and is improved in the connection reliability of common electrodes, and to provide an LED printer.
SOLUTION: In the light emitting diode array device, a plurality of light emitting diodes 10 are arranged on a high resistance substrate 1. The device is composed of individual electrodes 4 which are commonly connected to light emitting diodes in the same group composed of N pieces of light emitting diodes, and common electrodes 50 which are connected to prescribed light emitting diodes of different groups. Of M groups of light emitting elements, the light emitting diodes 10 of the m-th group are successively connected to N pieces of common electrodes 50 from the first common electrode 5a nearest to a light emitting diode array to the first common electrode 5h farthest from the array. The light emitting diodes 10 of a group adjoining the m-th group are successively connected to the N pieces of common electrodes 50 from the first common electrode 5h farthest from the light emitting diode array to the first common electrode 5a nearest to the array.



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B41J 2/455			

審査請求 未請求　請求項の数 3　OL　（全 20 頁）

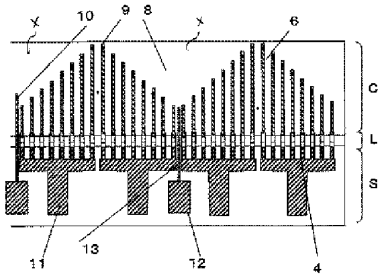
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Fターム(参考)　2C162 AH22 AH30 AH40 AH84 FA04 FA17 FA23
5F041 AA14 AA21 CA02 CA35 CA36 CA65 CA82 CA92 CB22 FF13

(54)【発明の名称】発光ダイオードアレイ装置及びそれを用いた発光ダイオードプリンタ

(57)【要約】
【課題】　電極抵抗のバラツキを小さくするとともに、共通電極の高い接続信頼性の発光ダイオードアレイ装置及びＬＥＤプリンタを提供することにある。
【解決手段】
本発明は、高抵抗基板１上に発光ダイオード１０を複数個配列するとともに、Ｎ個の発光ダイオードを発光素子群として、同一の発光素子群内の発光ダイオードに共通に接続する個別電極４と、異なる群に属する所定の発光ダイオードに接続する共通電極５０とからなる発光ダイオードアレイ装置である。そして、M群の発光素子群のうち、m番目の発光素子群の各発光ダイオード１０は、Ｎ個の共通電極のうち発光ダイオードアレイに最も近い側の第１の共通電極５ａから遠い側の第１の共通電極５ｈに順次に接続し、m番目の発光素子群に隣接する発光素子群の各発光ダイオード１０は、Ｎ個の共通電極のうち発光ダイオードアレイに最も遠い側の第１の共通電極５ｈから近い側の第１の共通電極５ａに順次接続する。
【選択図】図３



【特許請求の範囲】
【請求項1】
高抵抗基板上に複数の一導電型半導体層と逆導電型半導体層を設け、且つ該一導電型半導体層に共通電極を、逆導電型半導体層に個別電極を接続した発光ダイオードを複数個配列するとともに、前記複数の配列された発光ダイオードのうち、Ｎ個の発光ダイオードを発光素子群として、Ｍ群から構成される発光ダイオードアレイと、同一の発光素子群内の発光ダイオードの逆導電型半導体層に共通に接続する個別電極と、異なる群に属する所定の発光ダイオードの一導電型半導体層に接続する共通電極とからなる発光ダイオードアレイ装置において、
　共通電極は、発光ダイオードの配列方向に概略平行に延びるＮ個の第１の共通電極と、いずれか１つの第１の共通電極と同一の発光素子群のいずれか１つの発光ダイオードとを接続する第２の共通電極とから構成されるとともに
　Ｍ群の発光素子群のうち、ｍ番目の発光素子群の各発光ダイオードは、Ｎ個の共通電極のうち発光ダイオードアレイに最も近い側の第１の共通電極から遠い側の第１の共通電極に順次に第２の共通電極を介して接続するとともに、
　前記ｍ番目の発光素子群に隣接する発光素子群の各発光ダイオードは、Ｎ個の共通電極のうち発光ダイオードアレイに最も遠い側の第１の共通電極から近い側の第１の共通電極に順次に第２の共通電極を介して接続されていることを特徴とする発光ダイオードアレイ装置。
【請求項2】
前記第１の共通電極上には、第１の共通電極と第２の共通電極とを接続するコンタクトホールが形成された絶縁膜によって被覆され、且つ該絶縁基板上に第１の共通電極から共通電極側接続パッドとを接続する引出し配線が形成されているとともに、該引出し配線と第１の共通電極配線は、記前記隣接しあう発光素子群から延びる第２の共通電極の境界部分の絶縁膜に形成した第２のコンタクトホールを介して接続されていることを特徴とする請求項１記載の発光ダイオードアレイ装置。
【請求項3】
前記請求項１乃至２に記載された発光ダイオードアレイ装置と、該発光ダイオードアレイ装置の駆動を制御する駆動回路と、ページプリンタ用感光ドラムとを少なくとも有し、前記駆動回路によって発光動作する発光ダイオードアレイ装置の光を、前記ページプリンタ用感光ドラムの露光用光源に用いて、該ドラム表面に画像を形成する発光ダイオードプリンタ。

【発明の詳細な説明】
【技術分野】
【0001】
　本発明は、本発明は発光ダイオードアレイ装置、及びページプリンタ用感光ドラムの露光用光源などに用いられる発光ダイオードプリンタ（以下、単に、ＬＥＤプリンタという）に関するものである。
【背景技術】
【0002】
　通常、発光ダイオードアレイ装置の発光ダイオードの構造として、高抵抗基板の内部に一導電型半導体層、逆導電型導体層を形成すべく、ドープ材料を拡散処理して形成する構造（例えば特開平１１－４０８４２号）と、高抵抗基板上に、一導電型半導体層、逆導電型導体層をそれぞれ成膜して形成する構造（メサ型）が知られている。
【0003】
　例えば、このメサ型構造の発光ダイオードアレイ装置に関して、特開２００１－３２００８８号（特許文献１）が提案されている。その構造を図１１～図１３に示す。
【0004】
　図１１は、発光ダイオードの部分断面図、図１２は高抵抗基板上での電極配線の状況、特に下部側の電極配線の状況を示す概略平面図であり、図１３は電極配線の状況、特に上

部側の電極配線の状況を示す概略平面図である。

【0005】

図１１において、１２１は高抵抗基板であり、例えば半導体基板である。１２２は一導電型半導体層、１２３は逆導電型半導体層、１２４は個別電極、１２５は共通電極である。

【0006】

例えば、一導電型半導体層１２２は、バッファ層１２２ａ、オーミックコンタクト層１２２ｂ、電子注入層１２２ｃで構成される。また、逆導電型半導体層１２３は、発光層１２３ａ、クラッド層１２３ｂおよびオーミックコンタクト層１２３ｃで構成される。

【0007】

高抵抗基板１２１上に、一導電型半導体層１２２と逆導電型半導体層１２３とから成る発光ダイオードを設けるに当たり、一導電型半導体層１２２よりも逆導電型半導体層１２３を小面積と成すとともに、この一導電型半導体層１２２の露出部（オーミックコンタクト層１２２ｂ）に共通電極１２５が接続されている。また、逆導電型半導体層２３のオーミックコンタクト層１２３ｃに個別電極124が接続されている。なお、符号126は、窒化シリコン膜、ポリイミドなどから成る絶縁膜である。

【0008】

また、図１２に示すように発光ダイオードは、その配列方向にそって複数配列形成、平面視上、複数の発光ダイオードがアレイ状に配置されている。図では説明を簡略化のため、左端の３２の発光ダイオード素子が配列されている状態を例示している。そして、各発光ダイオードの駆動にあたっては、1つの発光素子群の構成する素子数Nを例えば８として取り扱っている。すなわち、図１２では、左側から１番目から８番目の発光ダイオード素子を群１に、９番目から１６番目の発光ダイオード素子を群２、・・・・とし、全体として群１～群M（図では、M=４までの一部を図示している）を有して構成される。

【0009】

また、各発光ダイオードの一導電型半導体層１２２には、共通電極１２５が接続されている。この共通電極125は、高抵抗基板１２１上に形成した絶縁膜１２６上に形成され逆導電型半導体層１２３には、個別電極１２４が接続されている。この個別電極１２４は、高抵抗基板１２１上においては、共通電極１２５と同様に絶縁膜１２６を介して形成されている。

【0010】

この共通電極１２５は、図１２に示すように、絶縁膜１２６上に概略コ字状形状の下地側に位置する第１の共通電極１２５ａ、１２５ｂ、１２５ｃ、１２５d、１２５ｅ、１２５ｆ、１２５ｇ、１２５hと、図１３に示すように、第１の共通電極１２５ａ、１２５ｂ、１２５ｃ、１２５d、１２５ｅ、１２５ｆ、１２５ｇ、１２５ｈを被覆された第２の絶縁膜１２７上にアレイ状の配列方向と平行に断続的に形成された上側の第２の共通電極１２８ａ、１２８ｂ、１２８ｃ、１２８ｄ、１２８ｅ、１２８ｆ、１２８ｇ、１２８ｈとで構成されている。

【0011】

ここで、共通電極１２５のうち、コ字状の下地側の第１の共通電極は、隣接する１２つの群の所定発光素子どうしを接続するように形成されている。たとえば、この第１の共通電極１２５ａ、１２５ｂ、１２５ｃ、１２５ｄ、１２５ｅ、１２５ｆ、１２５ｇ、１２５ｈどうしが交差していように配慮されており、最外周に位置する電極１２５ａは、群１（群３）の第１の番目の発光ダイオードと群２（群４）の第８番目の発光ダイオードとを接続するように概略コ字状に形成され、外周より２番目に位置する電極１２５ｂは、群１（群３）の第２の番目の発光ダイオードと群２（群４）の第７番目の発光ダイオードとを接続するように概略コ字状に形成され、外周より３番目に位置する電極１２５ｃは、群１（群３）の第３の番目の発光ダイオードと群２（群４）の第６番目の発光ダイオードとを接続するように概略コ字状に形成され、外周より４番目に位置する電極１２５ｄは、群１（群３）の第４の番目の発光ダイオードと群２（群４）の第５番目の発光ダイオードとを接

続するように概略コ字状に形成され、外周より５番目に位置する電極１２５ｅは、群１（群３）の第５の番目の発光ダイオードと群２（群４）の第４番目の発光ダイオードとを接続するように概略コ字状に形成され、
外周より６番目に位置する電極１２５ｆは、群１（群３）の第６の番目の発光ダイオードと群２（群４）の第３番目の発光ダイオードとを接続するように概略コ字状に形成され、
外周より７番目に位置する電極１２５ｇは、群１（群３）の第７の番目の発光ダイオードと群２（群４）の第１２番目の発光ダイオードとを接続するように概略コ字状に形成され、
最内周に位置する電極１２５ｈは、群１（群３）の第８の番目の発光ダイオードと群２（群４）の第１番目の発光ダイオードとを接続するように概略コ字状に形成されている。すなわち、１２ｎ－１番目の群に属する所定の発光ダイオードは、１２×ｎ番目（ｎ＝１・・・Ｎ／１２）の群に属する所定の発光ダイオードに接続している。

【0012】

これに対して、個別電極１２４は、同一群に属する発光素子の逆導電型半導体層１２３に共通的に接続している。また、この個別電極１２４には、それぞれ下地側の接続パッド１２４ａを有している。

【0013】

図１３は、図１２に示す発光ダイオードアレイ部分を除く領域上に、絶縁層１２７を被着形成し、該絶縁層１２７上に形成された電極を示している。この絶縁層１２７上に共通電極１２５を構成する複数の第２の共通電極１２８ａ、１２８ｂ、１２８ｃ、１２８ｄ、１２８ｅ、１２８ｆ、１２８ｇ、１２８ｈが形成されている。この第２の共通電極１２８ａ、１２８ｂ、１２８ｃ、１２８ｄ、１２８ｅ、１２８ｆ、１２８ｇは、１群目からＮ番目の群を互いに接続するために作用する。

【0014】

すなわち、最も外側に形成される直線状の複数の第２の共通電極１２８ａは、各群に跨がって最外周側に形成された複数の第１の共通電極１２５ａどうしを接続するものである。また、さらに内側に形成される直線状の第２の共通電極１２８ｂは、各群に跨がって形成された第１の共通電極１２５ｂどうしを接続するものであり、さらに内側に形成される直線状の第２の共通電極１２８ｃは、各群に跨がって形成された第１の共通電極１２５ｃどうしを接続するものであり、さらに内側に形成される直線状の第２の共通電極１２８ｄは、各群に跨がって形成された第１の共通電極１２５ｄどうしを接続するものであり、さらに内側に形成される直線状の第２の共通電極１２８ｅは、各群に跨がって形成された第１の共通電極１２５ｅどうしを接続するものであり、さらに内側に形成される直線状の第２の共通電極１２８ｆは、各群に跨がって形成された第１の共通電極１２５ｆどうしを接続するものであり、さらに内側に形成される直線状の第１２の共通電極１２８ｇは、各群に跨がって形成された第１の共通電極１２５ｇどうしを接続するものである。

【0015】

また、最も内側に形成される直線状の第１２の共通電極１２８ｈは、各群に跨がって形成された第１の共通電極１２５ｈどうしを接続するものである。

【0016】

そして、各第２の共通電極１２８ａ～１２８ｈの長さは、それぞれ相違しており，この相違によって形成された空白領域には、共通電極１２５の接続パッドが形成されている。図１３では、第２の共通電極１２８ａ及び第２の共通電極１２８ｂに接続する２つの外部接続パッド１２９が形成されているものの、図１３には現れない右側の領域に第２の共通電極１２８ｃ～１２８ｈに接続する接続パッド１２９が形成されている。

【0017】

また、個別電極１２４側には、上述の下地側接続パッド１２４ａに接続する個別側接続パッド１２４ｂが形成されている。

【0018】

この第１の共通電極１２５ａ～１２５ｈ及び第２の共通電極１２８ａ～１２８ｈの電気

的な接続及び個別電極１２４の下地側接続パッドと上側接続パッドとの接続は、絶縁層１２７の形成にあたり、絶縁層１２７の厚み方向に形成した開口を介して接続される。具体的には、第２の共通電極１２８ａ～１２８ｈの両端部が位置する領域に、開口が形成されている。

【特許文献1】特開２００１－３２００８８号

【発明の開示】

【発明が解決しようとする課題】

【0019】

しかしながら、発光ダイオードの動作においては、この所定の共通電極１２５と個別電極１２４とに所定電流を供給して行われる。発光ダイオードアレイにおいては、共通電極１２５そのものの構造が非常に複雑となってしまう。そして、共通電極１２５側の接続部が多いため接続部分での抵抗のバラツキが大きく、その結果発光バラツキを誘発する問題があった。例えば、図１３において、第２の共通電極１２８ａに接続する外部接続パッドから、群１～群４の所定共通電極１２５には、少なくとも１個所の接続部分を介して接続されるが、群５、群６の所定共通電極１２５に接続するまでには、３個所の接続部を経ることになり、群７、群８の所定共通電極１２５には、５個所の接続部が必要になる。

【0020】

このため、所定接続パッド１２９から、それに接続する所定発光ダイオードの共通電極１２５までの接続部分の個数が、各発光素子群によって相違するため、発光バラツキの原因となっていた。

【0021】

また、共通電極１２５の形成時に金属－半導体との接触性（オーミック性）を考慮して形成しているため、共通電極１２５の厚みサイズによる抵抗値とを両立させる必要があることから、金属材料の制約が大きく、材料が限られると言う問題もあった。

【0022】

また、共通電極１２５の形状や厚みについては、コスト増やチップサイズが増大などの問題があるが、さらに、共通電極１２５の材料については、低抵抗低材料の他に、金属－半導体の接触性を両立させる必要がある。

【0023】

第２の共通電極１２８は、その下部に、複雑な構造、例えば共通電極１２５の存在などにより、その表面に凹凸が形成されやすく、非常に平坦性の高い表面にこの電極を形成することが非常に困難となる。これによって、第２の共通電極１２８の電極形成が不安定となり、電極の抵抗バラツキが発生してしまう。

【0024】

接続パッド１２９は、所定第２の共通電極１２８が延長されて接続している。即ち、隣接しあう発光素子群の第２の共通電極１２８との間の非常に狭いスペースに、所定第２の共通電極１２８の延長部、接続パッド１２９を形成する必要があり、第２の共通電極が他の導体と接続してしまうなど接続信頼性が非常に低かった。

【0025】

本発明は上述の問題点に鑑みて案出されたものであり、その目的は、共通電極の構造及び接続構造を改良し、同時に接続パッドから発光ダイオードまで接続部分の個数を極小化させて各共通電極における電極抵抗のバラツキを小さくして発光バラツキを改善するとともに、共通電極の接続信頼性を向上した発光ダイオードアレイ装置を提供するものである。

【0026】

別の目的は、発光バラツキの少ない発光ダイオードアレイ装置を用いて、高品位な画像を形成できるＬＥＤプリンタを提供することにある。

【課題を解決するための手段】

【0027】

本発明の発光ダイオードアレイ装置は、高抵抗基板上に複数の一導電型半導体層と逆導電型半導体層を設け、且つ該一導電型半導体層に共通電極を、逆導電型半導体層に個別電

極を接続した発光ダイオードを複数個配列するとともに、前記複数の配列された発光ダイオードのうち、Ｎ個の発光ダイオードを発光素子群として、Ｍ群から構成される発光ダイオードアレイと、同一の発光素子群内の発光ダイオードの逆導電型半導体層に共通に接続する個別電極と、異なる群に属する所定の発光ダイオードの一導電型半導体層に接続する共通電極とからなる発光ダイオードアレイ装置において、

共通電極は、発光ダイオードの配列方向に概略平行に延びるＮ個の第１の共通電極と、いずれか１つの第１の共通電極と同一の発光素子群のいずれか１つの発光ダイオードとを接続する第２の共通電極とから構成されるとともに

Ｍ群の発光素子群のうち、ｍ番目の発光素子群の各発光ダイオードは、Ｎ個の共通電極のうち発光ダイオードアレイに最も近い側の第１の共通電極から遠い側の第１の共通電極に順次に第２の共通電極を介して接続するとともに、

前記ｍ番目の発光素子群に隣接する発光素子群の各発光ダイオードは、Ｎ個の共通電極のうち発光ダイオードアレイに最も遠い側の第１の共通電極から近い側の第１の共通電極に順次に第２の共通電極を介して接続されていることを特徴とする発光ダイオードアレイ装置である。

【0028】

また、第１の共通電極上には、第１の共通電極と第２の共通電極とを接続するコンタクトホールが形成された絶縁膜によって被覆され、且つ該絶縁基板上に第１の共通電極から共通電極側接続パッドとを接続する引出し配線が形成されているとともに、該引出し配線と第１の共通電極配線は、記前記隣接しあう発光素子群から延びる第２の共通電極の境界部分の絶縁膜に形成した第２のコンタクトホールを介して接続されていることを特徴とする発光ダイオードアレイ装置である。

【0029】

また、上述した発光ダイオードアレイ装置と、該発光ダイオードアレイ装置の駆動を制御する駆動回路と、ページプリンタ用感光ドラムとを少なくとも有し、前記駆動回路によって発光動作する発光ダイオードアレイ装置の光を、前記ページプリンタ用感光ドラムの露光用光源に用いて、該ドラム表面に画像を形成する発光ダイオードプリンタである。

【発明の効果】

【0030】

本発明では、複数の配列された発光ダイオードのうち、所定数の発光ダイオードを一群として、複数群から構成される発光ダイオードアレイと、同一の群内の発光ダイオードの一導電型半導体層に個別電極を接続し、異なる群に属する所定番目に配置された発光ダイオードの逆導電型半導体層に共通電極に接続した発光ダイオードアレイ装置である。

【0031】

共通電極は、発光ダイオードの配列方向に概略平行に延びる第１の共通電極及び該第１の共通電極の一部から各異なる群に属する同一番目に配置された発光ダイオードの逆導電型半導体層に接続する第２の共通電極とから構成されている。そして、Ｍ群の発光素子群のうち、ｍ番目の発光素子群の各発光ダイオードは、Ｎ個の共通電極のうち発光ダイオードアレイに最も近い側の第１の共通電極から遠い側の第１の共通電極に順次に第２の共通電極を介して接続するとともに、

Ｍ群の発光素子群のうち、ｍ番目の発光素子群に隣接する発光素子群の各発光ダイオードは、Ｎ個の共通電極のうち発光ダイオードアレイに最も遠い側の第１の共通電極から近い側の第１の共通電極に順次に第２の共通電極を介して接続されている。このため、ｍ番目の発光素子群に隣接する２つの発光素子群のうち、１つの発光素子群との間には、実質的に三角形状のスペースを有している。

【0032】

この第１の共通電極についていえば、発光ダイオードに直接接続することがなく、金属－半導体のオーミック接触性を全く考慮することなく、その材料を配線抵抗のみを考慮して選択することができる。また、この第1の共通電極は、複数の発光ダイオードアレイの配列方向に略平行に延び、しかも、実質的には発光ダイオードの配列されている略幅に渡

って形成されている。しかも、この第１の共通電極は、高抵抗基板の表面に形成された第１の絶縁膜を介して形成されることになり、非常に導体長が長い電極であっても，その形成を平坦な表面に形成するができ、第１の共通電極を安定、均一に形成することができる。

【0033】

このため、第１の共通電極は材料からしても、また、構造からしても、複数の第１の共通電極をすべて同じ状態で形成できるため、安定した導体膜であり、且つ電極抵抗も大きくなることがない。これにより、第１の共通電極の抵抗バラツキを有効に抑えることができ、発光ダイオードの安定した発光動作を行うことができる。

【0034】

しかし、発光ダイオードから第１の共通電極への接続は、各群のいずれの発光ダイオードについても、第２の共通電極から第１の共通電極へは１個所の接続部（コンタクトホール）のみ行われるため、全体として接続部を数も減少させることができる。しかも、所定の第１の共通電極から共通電極側接続パッドへも１個所の接続部（コンタクトホール）のみ行われるため、全体として共通電極側接続パッドから発光ダイオードへの接続部を数が大きく減少できる。

【0035】

従って、各共通電極における電極抵抗のバラツキを小さくでき、発光ダイオードでの発光バラツキを改善できる。また、共通電極を電極が要求される抵抗特性と、半導体と接続する金属－半導体のオーミック接触性とを両立させることができ、また、導体長さの長い第１の共通電極を低抵抗とすることも容易となり、これによっても、発光ダイオードでの発光バラツキを改善できる。

【0036】

しかも、第１の共通電極から共通電極側接続パッドへの接続部（コンタクトホール）は、上述のm番目の発光素子群に隣接する発光素子群のうち、１つの発光素子群との間に形成される実質的に三角形状のスペースに形成されている。このため、第１の共通電極と共通電極側接続パッド（または共通電極側接続パッドに接続する引出し電極）との接続部が、第１の共通電極と第２の共通電極との接続部から距離的に離して形成できる。このため、第１の共通電極と共通電極側接続パッド（または共通電極側接続パッドに接続する引出し電極）との接続部の接続信頼性が向上する。

【0037】

これにより、外部の駆動回路との接続、例えばボンディングワイヤの融着接合が、高抵抗基板の一方端部側である個別電極形成領域のみで行われるため、その接合作業が非常に簡単となり、発光ダイオードアレイ装置と駆動回路との接合が安定する。

【0038】

これは、ボンィングワイヤに限らず、例えば接続パッドに銀粉末を含有する導電性ペーストを塗布して、この銀バンプと外部の駆動回路とを接続する場合においても、上述の導電性ペーストの塗布が高抵抗基板の一方端部側である個別電極形成領域のみで行われるので、その接合作業が非常に簡単となる。

【0039】

また、このような発光ダイオードアレイ装置を安定した接合状態で駆動回路に接続して、発光制御して発光動作させることにより、ページプリンタ用感光ドラムにバラツキの少ない露光用光源となり、その結果、該ドラム表面に安定した画像を形成することができ、高い品位の印字が可能となる。

【発明を実施するための最良の形態】

【0040】

以下、本発明の発光ダイオードアレイ装置を図面に基づき詳細に説明する。

【0041】

図１～図３は本発明に係る発光ダイオードアレイ装置の一実施形態を示し、図１は本発明の横断面図であり、図２は、発光ダイオード（発光素子部）の要部拡大の断面図であり、

図３は発光ダイオードアレイ装置の平面である。なお、図４は第１の共通電極と第２の共通電極との関係を明瞭にした平面図である。

【0042】

図において、１は高抵抗基板であり、１０は発光ダイオード素子であり、２は発光ダイオード１０を構成する一導電型半導体層であり、３は発光ダイオード１０を構成する逆導電型半導体層であり、４は個別電極であり、５０は共通電極であり、５は第１の共通電極であり、６は第２の共通電極であり、７は高抵抗基板１の表面に形成された第１の絶縁膜であり、８は第１の共通電極５上に被着された第２の絶縁膜であり、本発明でいう絶縁膜とはこの第２の絶縁膜８を指す。

【0043】

高抵抗基板１は、たとえばシリコン（Ｓｉ）やガリウム砒素（ＧａＡｓ）などの単結晶半導体基板やサファイア（Al_2O_3）などの単結晶絶縁基板である。例えば、単結晶半導体基板の場合においては、（１００）面を＜０１１＞方向に２～７°オフさせた基板などが好適に用いられる。サファイアの場合においては、Ｃ面基板が好適である。

【0044】

この高抵抗基板１上の表面中央部領域に、複数の発光ダイオード１０が１列に複数配列されて形成されている。また、基板１上には、この発光ダイオード１０が配列された領域Ｌを挟んで、主に個別電極が形成される個別電極形成領域Ｓと、主に共通電極が形成される共通電極形成領域Ｃを有している。

【0045】

この発光ダイオードの主要部分の構成は、一導電型半導体層２及び逆導電型半導体層３から構成されている。

【0046】

一導電型半導体層２は、バッファ層２ａ、オーミックコンタクト層２ｂ、電子の注入層２ｃで構成される。バッファ層２ａは２～４μｍ程度の厚みに形成され、オーミックコンタクト層２ｂは０．１～１．０μｍ程度の厚みに形成され、電子の注入層２ｃは０．２～０．４μｍ程度の厚みに形成される。バッファ層２ａとオーミックコンタクト層２ｂはガリウム砒素などで形成され、電子の注入層２ｃはアルミニウムガリウム砒素などで形成される。また、オーミックコンタクト層２ｂはシリコンなどの一導電型半導体不純物を１×１０^{16}～１０^{19}ａｔｏｍｓ／ｃｍ^3 程度含有し、電子の注入層２ｃはシリコンなどの一導電型半導体不純物を１×１０^{16}～１０^{19}ａｔｏｍｓ／ｃｍ^3 程度含有する。

【0047】

バッファ層２ａは高抵抗基板１と半導体層との格子定数の不整合に基づくミスフィット転位を防止するために設けるものであり、半導体不純物を含有させる必要はない。

【0048】

この一導電型半導体層２のオーミックコンタクト層２ｂには、共通電極５０が接続される。

【0049】

また、逆導電型半導体層３は、発光層３ａ、第２のクラッド層３ｂおよび第２のオーミックコンタクト層３ｃで構成される。

【0050】

発光層３ａと第２のクラッド層３ｂは０．２～０．４μｍ程度の厚みに形成され、オーミックコンタクト層３ｃは膜厚ｄ＞（０．１５μｍ－オーミックコンタクト層膜厚）程度の厚みに形成される。発光層３ａと第２のクラッド層３ｂはアルミニウムガリウム砒素などから成り、第２のオーミックコンタクト層３ｃはガリウム砒素などから成る。発光層３ａと第２のクラッド層３ｂは、電子の閉じ込め効果と光の取り出し効果を考慮してアルミニウム砒素（ＡｌＡｓ）とガリウム砒素（ＧａＡｓ）との混晶比を異ならしめる。発光層３ａと第２のクラッド層３ｂは亜鉛（Ｚｎ）などの逆導電型半導体不純物を１×１０^{16}～１０^{21}ａｔｏｍｓ／ｃｍ^3 程度含有し、第２のオーミックコンタクト層３ｃは亜鉛などの逆導電型半導体不純物を１×１０^{19}～１０^{21}ａｔｏｍｓ／ｃｍ^3 程度含有する。

【0051】
この逆導電型半導体層３の第２のオーミックコンタクト層３ｃには、個別電極４が接続される。
【0052】
また、高抵抗基板１の共通電極形成領域Ｃ及び個別電極形成領域Ｓの大部分の領域には、第１の絶縁膜７が形成されている。
【0053】
第１の絶縁膜７は、酸化シリコンや窒化シリコンなどが例示できる。基板材料がシリコンである場合、基板表面の熱酸化処理により形成できる。また、その他の基板材料の場合に、シランガス（SiH_4）や必要に応じてアンモニアガス（NH_3）を用いてプラズマＣＶＤ法などによって被着形成する。
【0054】
共通電極５０を構成する第１の共通電極５は、高抵抗基板１の共通電極側領域Ｃの第１の絶縁膜７上に形成される。この第１の共通電極５は、発光ダイオード１０の配列方向に略平行に形成され、その長さは、実質的には、発光ダイオード１０の配列の幅と同等の長さを有している。また、この第１の共通電極は、発光ダイオード１０の駆動の単位である発光素子群を構成する発光ダイオードの構成数（Ｎ）と同一の数だけ形成される。
【0055】
第１の共通電極５は、高抵抗基板１上に形成した平坦な面を有する第１の絶縁膜７上に、例えば、下地導体膜としてＣｒを１５０Å以上形成した後、アルミニウム／金などの順次積層た多層構成などが例示できる。その厚みが例えば１μｍである。なお、下地導体膜を省略して金／クロム（Ａｕ／Ｃｒ）、アルミニウム／クロム（Ａｌ／Ｃｒ）の多層層構造であってもよい。
【0056】
この第１の共通電極５は、発光ダイオード１０の配列幅にわたり、比較的長く形成されているものの、その下面には、平坦な高抵抗基板１の表面に形成された第１の絶縁膜に形成される。即ち、基板の複雑な構造や導体膜がない状態でないため、第１の絶縁膜７の表面が非常に平坦化された表面となり、この平坦な表面に第１の共通電極５を形成されるため、複数の第１の共通電極５において構造的に均一化を図ることができる。また、材料も金を含む非常に良好な導電材料を用いているため、その抵抗のバラツキも抑えることができる。
【0057】
第２の絶縁膜８は、共通電極形成領域Ｃ、個別電極形成領域Ｓの一部、さらには、発光ダイオードの一部に形成されるものであり、例えば透明な材料で構成される。具体的には、ポリイミド合成樹脂、感光性樹脂、窒化シリコン、酸化シリコン、ポリイミドシリコンなどから成る材料などが例示できる。この第2の絶縁膜8の厚みは２０００～２００００Å程度に形成する。
【0058】
この第２の絶縁膜８は、発光ダイオード１０において、少なくともオーミックコンタクト層２ｂ、３ｃを露出するように形成され、さらに、共通電極形成領域Ｃには、２種類の開口（コンタクトホール９、１０）が形成されている。
【0059】
コンタクトホール９は、発光ダイオードのオーミックコンタクト層２ｂと第１の共通電極５を接続する第２の共通電極６が、安定して所定第１の共通電極５に接続するように形成されるものであり、例えば、所定第１の共通電極５の一部を露出するように形成されている。
【0060】
また，コンタクホール１０は、共通電極側接続パッド１２と所定第１の共通電極５を接続する引出し電極１３が、安定して所定第１の共通電極５に接続するように形成されるものである。

【0061】
このような第２の絶縁膜８は、例えば高抵抗基板１の上面に、第２の絶縁膜８となるポリイミド合成樹脂、感光性樹脂、窒化シリコン、酸化シリコン、ポリイミドシリコンなどを被着形成し、その後フォトグラフィ技術を利用して、コンタクトホール９、１０や一導電型半導体層２のオーミックコンタクト層２ｂ、逆導電型半導体層３のオーミックコンタクト層３ｃが露出すようにエッチング処理されて形成されるものである。
【0062】
ここで、コンタクトホール９は、１つの発光素子群の幅に対応する領域に、Ｎ個の第１の共通電極５を順次露出するように形成されている。図３においては、最も右側（右側から奇数番目）の発光素子群に対応するＮ個のコンタクトホール９は、右肩下がりに配列されて形成され、右から２番目（右から偶数番目）の発光素子群に対応するＮ個のコンタクトホール９は、右肩上がりに配列されて形成されている。その結果、第２番目の発光素子群と、第３番目の発光素子群と範囲に対応する共通電極形成領域Ｃには、比較的広い第２の絶縁膜の領域が形成されることになる。
【0063】
コンタクトホール１０は、Ｍ群の発光素子群の幅（アレイの全幅）に対応する領域に、Ｎ個の第１の共通電極５のいずれかを露出するように形成されている。図３においては、右側から１番目の発光素子群と右側から２番目の発光素子群との間に、右側から２数番目の発光素子群と右側から３番目の発光素子群との間に、・・・にそれぞれ形成されている。
【0064】
また、高抵抗基板１の個別電極形成領域Ｓには、複数の個別電極４が形成されている１つの個別電極４は、１つの発光素子群を成す例えば８つ個の発光素子に共通的に接続するように、例えば櫛形状に形成される。即ち、個別電極４は、発光素子群の数Ｍに対応する数だけ形成されている。この個別電極４は、第２の絶縁膜８上に形成され、発光ダイオード１０の逆導電型半導体層３ｃに接続される。
【0065】
また、各個別電極４は、個別電極側接続パッド１１を有している。また、個別電極側接続パッド１１も第２の絶縁膜８に形成されている。なお、個別電極側接続パッド１１と外部駆動回路との接続手法によっては、第２の絶縁膜８が除外されて第１の絶縁膜７上に形成してもよい。
【0066】
高抵抗基板１の共通電極形成領域Ｃには、複数の第２の共通電極６が形成されている。１つの第２の共通電極６は、１つの発光ダイオードの一導電型半導体層２のオーミックコンタクト層２ｂから所定のコンタクホール９から露出する第１の共通電極５を接続するために形成されている。即ち、第１の共通電極５は、発光ダイオード１０の配列方向に平行に延びているが、第２の共通電極６は、それと直交する方向に形成されている。
【0067】
これより、発光素子群を構成するＮ個の発光ダイオード１０は、それぞれ異なる第１の共通電極５に接続することになる。
【0068】
また、各第１の共通電極５には、それぞれ１つの共通電極側接続パッド１２に接続されている。この共通電極側接続パッド１２は、例えば個別電極形成領域Ｓ側に形成されている。そして、この共通電極側接続パッド１２と所定の第１の共通電極５は、引出し電極１３によってコンタクトホール１０を介して接続されている。なお、共通電極側接続パッド１２も第２の絶縁膜８に形成されているが、虚通電極側接続パッド１２と外部の駆動回路との接続手法によっては、第２の絶縁膜８が除外されて第１の絶縁膜７上に形成してもよい。
【0069】
また、この引出し電極１３は、各発光素子群との境界部分の間隙に、第２の絶縁膜８

上に形成されている。これにより、共通電極形成領域Ｃに形成されたコンタクトホール１０と個別電極形成領域Ｓに形成された共通電極側接続パッド１２とが引出し電極１３が接続されている。

【0070】

この第２の共通電極６や個別電極４は、オーミックコンタクト層２ｂ、３ｃに接触する電極である。このため、金／金・ゲルマニウム／クロム（Ａｕ／ＡｕＧｅ／Ｃｒ）などのから成る多層構造となっており、その厚み１μｍ程度以下に形成される。なお、この多層構造の材料を熱処理を加えて、Geを半導体層に拡散処理している。

【0071】

なお、引出し電極１３は、第２の共通電極６、個別電極４と同一工程で形成することが望ましいが、金属－半導体オーミック接触性を考慮することなく、良導電体材料を用いて構わない。また、接続パッド１１、１２の上面にも、引出し電極１３と同一の良導電体材料を被着形成してもよい。

【0072】

以上の構成した発光ダイオードアレイ装置では、高抵抗基板１の共通電極形成領域Ｃでは、高抵抗基板１上に第１の絶縁膜７が形成され、さらに、第１の共通電極５が形成され、さらに、第１の共通電極５上には第２の絶縁膜８が形成されおり、第２の絶縁膜８を介して第２の共通電極６または引出し電極１３が形成ささている構造である。

【0073】

また、高抵抗基板１の個別電極形成領域Ｓでは、高抵抗基板１上に第１の絶縁膜７、第２の絶縁膜８が形成されており、この第２の絶縁膜８上に個別電極４、個別電極側接続パッド１１、共通電極側接続パッド１２、引出し電極１３が形成されている。なお、個別電極側接続パッド１１、共通電極側接続パッド１２の直下においては、第２の絶縁膜８を省略してもよい。

【0074】

次に、図３、図４を用いて、発光ダイオードアレイ装置の電極及び接続パッド構造を詳細に説明する。

【0075】

上述の構成の発光ダイオードは、複数アレイ状に配置され、例えば、隣接するＮ個（図３、図４では８個）の発光ダイオード（素子）が１つの群として取り扱われる。図３、図４では、右側からは第１の群から第４群までの３２（８素子×４群）素子が示されているが、全体としては、Ｍ群の発光素子群を有している。

【0076】

図３、図４に示す高抵抗基板１の図の下側領域である個別電極形成領域Ｓには、１つの発光素子群を成す８つ個の発光素子に共通的に接続するように、例えば櫛形状の個別電極４が形成されている。そして、この櫛状の個別電極４には個別電極側接続パッド１１が１つ形成さている。なお、隣接する群も個別電極４の構成は同様となっている。

【0077】

つぎに、共通電極５０について言えば、第１の共通電極５と第２の共通電極６とか構成されているが、図４に示すように、第１の共通電極５は、発光ダイオードの配列方向と平行に延びるように形成されている。第１の共通電極５は、例えば発光素子群の群数Ｍに係わらず、１つの発光素子群を構成する発光ダイオード１０の数Ｎ（図ではＮ＝８）に相当する数だけ形成されている。この例では第１の共通電極５は８つの電極で構成されている。また、第２の共通電極６は、各発光ダイオードと第１の共通電極５とを接続するものであり、各発光ダイオードから第１の共通電極５のいずれかに接続するように発光ダイオードの配列方向と直交する方向に延びて形成されている。そして、第２の共通電極６の一端は１つの発光タダイオードの一導電型半導体層２のオーミックコンタクト層２ｂに重畳接続し、他端はコンタクトホール９を介して所定第１の共通電極５の一部に重畳接続する。即ち、第２の共通電極６は発光素子群１つから素子数Ｎ（例ではＮ＝８）だけ延びており、全体として、Ｎ素子×Ｍ群だけ形成されている。

【0078】
ここで、第１の共通電極５に関しては、例えば８つの第１の共通電極を区別するためには、発光ダイオードアレイに近い側から符号５ａ、５ｂ、５ｃ・・５ｈ（例では１発光素子群が８素子で構成されているためＮ＝８、最終符号は５ｈとなる）で示す。また、第２の共通電極６に関しては、例えば最も右側の発光素子群を構成する発光ダイオードで、第１の共通電極５ａに接続する第２の共通電極を符号６１ａ、そのコンタンクトホール９１ａ、第１の共通電極５ｂに接続する第２の共通電極を符号６１ｂ、そのコンタンクトホール９１ｂ、・・・・・第１の共通電極５ｈに接続する第２の共通電極を符号６１ｈ、そのコンタンクトホール９１ｈと示し、右側から２番目の発光素子群を構成する発光ダイオード１０で第１の共通電極５ａに接続する第２の共通電極を符号６２ａ、そのコンタンクトホール９２ａ、第１の共通電極５ｂに接続する第２の共通電極を符号６２ｂ、そのコンタンクトホール９２ｂ、・・・・・第１の共通電極５ｈに接続する第２の共通電極を符号６２ｈ、そのコンタンクトホール９２ｈと示す。
【0079】
この図３、図４で、右側から第１番目、３番目、５番目・・・（奇数番目）の発光素子群の発光ダイオードで、第２の共通電極を介して第１の共通電極５ａに接続する発光ダイオードは、発光素子群中最も右側に形成されものであり、第１の共通電極５ｈに接続する発光ダイオードは、発光素子群中最も左側に形成されものであり、右側から第２番目、４番目、６番目・・・（偶数番目）発光素子群の発光ダイオードで、第２の共通電極を介して第１の共通電極５ａに接続する発光ダイオードは、発光素子群中最も左側に形成されものであり、第１の共通電極５ｈに接続する発光ダイオードは、発光素子群中最も右側に形成されものであり、奇数番目の発光素子群と偶数番目の発光素子群と対象に配置されている。
【0080】
これにより、Ｍ群の発光素子群のうち、ｍ番目の発光素子群の各発光ダイオードは、Ｎ個の共通電極のうち発光ダイオードアレイに最も近い側の第１の共通電極５ａから遠い側の第１の共通電極５ｈに順次に第２の共通電極６を介して接続するとともに、Ｍ群の発光素子群のうち、ｍ番目の発光素子群に隣接する発光素子群の各発光ダイオードは、Ｎ個の共通電極のうち発光ダイオードアレイに最も遠い側の第１の共通電極５ｈから近い側の第１の共通電極５ａに順次に第２の共通電極６を介して接続されている。このため、ｍ番目の発光素子群に隣接する２つの発光素子群のうち、１つのは発光素子群との間には、実質的に三角形状のスペースＸが形成される。
【0081】
また、第１の共通電極５ａの一部は、共通電極側接続パッド１２ａに接続されており、第１の共通電極５ｂの一部は共通電極側接続パッド１２ｂに接続されており、・・・第１の共通電極５ｈの一部は共通電極側接続パッド１２ｈに接続されている。
【0082】
具体的には、図３、図4では第１の共通電極５ａに接続する共通電極側接続パッド１２ａは、第１番目の発光素子群と第２番目の発光素子群との境界部分を介して、個別電極形成領域Ｓ側に延び、個別電極側接続パッド１１に並設されている。また、第１の共通電極５ｂに接続する共通電極側接続パッド１２ｂは、第２番目の発光素子群と第３番目の発光素子群との境界部分を介して、個別電極形成領域Ｓ側に延び、個別電極側接続パッド１１に並設されている。このとき、第１の共通電極５ａと共通電極側接続パッド１２ａとは、コンタンクホール１０ａ、引出し電極１３を介して行われる。同様に、第１の共通電極５ｂ～５ｈと共通電極側接続パッド１２ｂ～１２ｈとは、コンタンクホール１０ｂ～１０ｈ、引出し電極１３を介して行われる。
【0083】
尚、図では省略しているが、共通電極側接続パッド１２を、上述のコンタクトホール１０ａ～１０ｈの形成領域を含む領域、即ち、上述の三角形状のスペースＸに形成してもよい。このときには、１つの三角形状のスペースＸに１つの第１の共通電極５に接続する１

つの共通電極側接続パッド１２を形成する。しかも、この共通電極側接続パッド１２の形成領域の直下にコンタクトホール１０ａ～１０ｈを位置させれば、引出し電極が省略できる。

【0084】

このような接続構造において、各発光素子群に係わらず、各発光タイオードの共通電極５０側においては、第２の共通電極６、コンタンクホール９を介して、所定の第１の共通極５ａ～５ｈのいずれかに接続し、さらに各第１の共通電極５ａ～５ｈから１つのコンタンクホール１０ａ～１０ｈを介して共通電極側接続パッド１２ａ～１２ｈに接続している。

【0085】

このような発光ダイオードアレイ装置は、外部の駆動回路によって、個別電極４と共通電極５０とが同時にと選択された発光ダイオード１０に電圧が印加され、その結果、それに対応する発光ダイオードが発光することになる。

【0086】

例えば、第１の共通電極５ａに相当する共通電極を選択することにより、発光し得る発光ダイオードは、各発光素子群内で１つの発光ダイオードだけとなる。即ち、図３、図４においては、右側から奇数番目の発光素子群の最も右側の発光ダイオードと、同じく偶数番目の発光素子群の最も左側の発光ダイオードに限られる。

【0087】

この時、発光素子群に共通的に接続される個別電極４で、どの発光素子群に選択するかによって、選択された発光素子群の上述の発光ダイオード１０に発光に必要な電圧が印加されて発光することになる。

【0088】

このように、第１の共通電極５ａ～５ｈに相当する共通電極５０のうち、どれの共通電極５０を選択し、個別電極４側でどの発光素子群を選択するかによって、アレイ状に配置された発光ダイオードのうち、どの発光ダイオードを発光させるかを制御できる。

【0089】

このように、個別電極４で、発光させるべき対象の発光ダイオードを含む発光素子群を選択し、共通電極５０側の第１の共通電極５ａ～５ｈを順次選択切り替えてすべての発光ダイオードを独立に制御することができる。

【0090】

しかも、発光ダイオードの配列数、即ち、発光されるビット数が６４ｂｉｔ（Ｎ＝８、Ｍ＝８）であっても、１９２ｂｉｔ（Ｎ＝８、Ｍ＝２４）であっても、８つの第１の共通電極で簡単に駆動制御が可能である。この第２の共通電極５の数は、発光素子群を構成する発光ダイオードの数に相当する数で、簡単に発光ダイオードの発光制御が可能である。

【0091】

なお、この構造は、１系統の駆動回路で発光制御することを前提として説明しているものであり、２系統の駆動回路で制御する場合には、この発光ダイオードアレイ装置を、１つの高抵抗基板１上に並設するようにしても構わない。

【0092】

このように、本発明の発光ダイオードアレイ装置によれば、複数の発光ダイオードの発生を制御するための個別電極４、共通電極５０の第１の共通電極５、第２の共通電極６とが全く別の構造で形成されており、且つ第１の共通電極５の導体材料と第２の共通電極６とを全く別の材料で構成することができる。例えば第１の共通電極５を、配線抵抗（電極抵抗）を小さくするための構造、材料を容易に選択でき、また、第２の共通電極６を、半導体－金属の接触性を考慮して、また、第１の共通電極５との接続性を考慮して、それぞれの特性が良好にするための構造、材料を選択できる。

【0093】

しかも、各発光ダイオード１０から共通電極側接続パッド１２までの接続点、例えばコンタクトホール９、１０の数を、各発光ダイオード１０で均一化することができる。

【0094】
これにより、従来例に示した発光ダイオードアレイ装置に比較して、共通電極側における発光ダイオードから共通電極側接続パッドまでの接続点の数を減少でき、また、目的に応じて導体材料の選択の容易となり、その結果、各発光ダイオードにおける共通電極５の電極抵抗のバラツキが極小化でき、発光バラツキを小さくすることができる。
【0095】
また、第１の共通電極５は、発光ダイオードアレイの配列方向に平行に形成され、第２の共通電極６は、各発光ダイオーと第１の共通電極５とを接続するように形成されている。即ち、第２の共通電極６の幅を、実質的に発光ダイオードの幅よりも小さく設計することで、発光ダイオードアレイの配列方向の寸法を極小化することができる。
【0096】
さらに、共通電極側接続パッド１２は、発光ダイオード１０の配列領域Ｌを挟んで設けられる個別共通電極形成領域Ｓに形成されている。即ち、共通電極が形成された共通電極形成領域Ｃから個別電極形成領域Ｓに、発光素子群との境界部分に形成された引出し電極１３によって接続され、この個別電極形成領域Ｓには個別電極側接続パッド１１、共通電極側接続パッド１２とが並設されている。
【0097】
これにより、外部の駆動回路との接続、例えばボンディングワイヤの融着接合が、高抵抗基板の一方端部側である個別電極形成領域のみで行われるため、その接合作業が非常に簡単となり、発光ダイオードアレイ装置と外部の駆動回路との接合が安定する。
【0098】
これは、ボンィングワイヤに限らず、例えば接続パッドに銀粉末を含有する導電性ペーストを塗布して、この銀バンプと外部の駆動回路とを接続する場合においても、上述の導電性ペーストの塗布が高抵抗基板の一方端部側である個別電極形成領域のみで行われるので、その接合作業が非常に簡単となる。
【0099】
しかも、第１の共通電極５から共通電極側接続パッド１２への接続部（コンタクトホール１０）は、上述のｍ番目の発光素子群に隣接する発光素子群のうち、１つの発光素子群との間に形成される実質的に三角形状のスペースＸに形成されている。このため、第１の共通電極５と共通電極側接続パッド１２（または共通電極側接続パッド１２に接続する引出し電極１３）との接続部（コンタクトホール１０）が、第１の共通電極５と第２の共通電極６との接続部（コンタクトホール９）から距離的に離して形成できる。このため、第１の共通電極と共通電極側接続パッド（または共通電極側接続パッドに接続する引出し電極１３）との接続部の接続信頼性が向上する。
【0100】
また、共通電極を電極が要求される抵抗特性と、半導体と接続する金属－半導体のオーミック接触性とを両立させることができ、また、導体長さの長い第１の共通電極を低抵抗とすることも容易となり、これによっても、発光ダイオードでの発光バラツキを改善できる。
【0101】
このよう発光ダイオードアレイ装置は、ＬＥＤプリンタの露光用光源として用いられる。即ち、ＬＥＤプリンタは、その主要部分の構成は、ページプリンタ用感光ドラム、この感光体ドラム上に画像を形成するための露光光源手段である発光ダイオードアレイ装置、このプリントすべき画像情報、感光体ドラムの回転測度に応じて、発光させるべき発光ダイオードの駆動を制御する駆動回路と、ドラムに電荷を印加または除去する手段、トナーを供給する手段、ドラム上に付着するトナーを記録媒体に転写する転写手段、記録媒体に転写したトナーを定着する定着手段、記録媒体を搬送する搬送手段、ドラム上の不要なトナーを除去するクリーニング手段とから構成されている。
【0102】
このようなＬＥＤプリンタにおいて、露光光源である発光ダイオードアレイ装置の発光

バラツキがすくないため、非常に安定した画像を感光体ドラムに形成することができ、よって、記録媒体に印刷される画像が非常に高品位とすることができる。

【0103】

また、このような発光ダイオードアレイ装置を安定した接合状態で駆動回路に接続して、発光制御して発光動作させることにより、その結果、該ドラム表面に安定した画像を形成することができ、高い品位の印字が可能となる。

【0104】

次に、図５～図１０及び図３、図４を用いて発光ダイオードアレイ装置の製造方法を説明する。

【0105】

まず、図５において、単結晶材料からなる高抵抗基板１を用意するとともに、その全面に第１の絶縁膜７となる絶縁膜７１を形成する。絶縁膜７１は、酸化シリコンや窒化シリコンなどが例示で、基板材料よっては、基板表面を熱酸化処理に形成したり、また、プラズマＣＶＤ法で、シランガス（SiH_4）や必要に応じてアンモニアガス（NH_3）を用いて被着形成する。

【0106】

つぎに、図６に示すに、発光ダイオード１０が形成される領域Ｌのみを、配列方向に沿って絶縁膜７１をエッチング処理して、共通電極形成領域Ｃ、個別電極形成領域にＳに第１の絶縁膜７を形成する。

【0107】

つぎに、図７、図８に示すように、高抵抗基板１が露出する配列領域Ｌに、一導電型半導体層２及び逆導電型半導体層３をＭＯＣＶＤ法などで順次積層して発光ダイオード１０の主要部分を形成する。これより、図２に示すように一導電型半導体層２は、バッファ層２ａ、オーミックコンタクト層２ｂ、電子の注入層２ｃからなり、逆導電型半導体層３は、発光層３ａ、第２のクラッド層３ｂおよび第２のオーミックコンタクト層３ｃからなる発光ダイオードの主要部分が形成される。なお、一導電型半導体層２、逆導電型半導体層３を形成する場合、高抵抗基板１を４００～５００℃に設定して２００～２０００Åの厚みにアモルファス状のガリウム砒素膜を形成した後、基板温度を７００～９００℃に上げて所望厚みの半導体層２、３を形成する。この場合、原料ガスとしてはＴＭＧ（$(CH_3)_3Ga$）、ＴＥＧ（$(C_2H_5)_3Ga$）、アルシン（AsH_3）、ＴＭＡ（$(CH_3)_3Al$）、ＴＥＡ（$(C_2H_5)_3Al$）などが用いられ、導電型を制御するためのガスとしては、シラン（SiH_4）、セレン化水素（H_2Se）、ＴＭＺ（$(CH_3)_3Zn$）などが用いられ、キャリアガスとしては、H_2などが用いられる。

【0108】

そして、隣接する発光ダイオード１０どうしが電気的に分離されるように、一導電型半導体層２、逆導電型半導体層が島状にパターニングされる。このエッチングは、硫酸過酸化水素系のエッチング液を用いたウェットエッチングやCCl_2F_2ガスを用いたドライエッチングなどで行われる。

【0109】

その後、一導電型半導体層２の一端部側の一部が露出し、且つこの一導電型半導体層２の隣接する領域部分が露出するように逆導電型半導体層３が一導電型半導体層２よりも幅狭に形成されるように逆導電型半導体層３をエッチングする。このエッチングも硫酸過酸化水素系のエッチング液を用いたウェットエッチングやCCl_2F_2ガスを用いたドライエッチングなどでおこなわれる。

【0110】

次に、図９に示すように高抵抗基板１の共通電極形成領域Ｃの絶縁膜７上に第１の共通電極５ａ～５ｈを形成する。具体的にはクロムと金を順次蒸着法やスパッタリング法で多層化された金属膜を形成しパターン化する。この形成にあたっては、パターン化の際にエッチング液が発光ダイオードの主要部分に及ぼす影響を考慮して、リフトオフ法によって形成する。

【0111】
つぎに、図１０に示すように第２の絶縁膜８を形成する。この絶縁膜８の形成において、同時に、複数のコンタクトホール９、１０が形成される。具体的には、全体にポリイミド合成樹脂、感光性樹脂、窒化シリコン、酸化シリコン、ポリイミドシリコンなどから成る材料で絶縁膜を厚み２０００～２００００Å程度に形成する。その後、フォトグラフィ技術を利用して、少なくともコンタクトホール９、１０、一導電型半導体層２のオーミックコンタクト層２ｂ、逆導電型半導体層３のオーミックコンタクト層３ｃが露出すようにエッチング処理しその後レジスト膜を剥離する。
【0112】
最後に、図４に示すように、高抵抗基板１の第２の絶縁膜８上に、個別電極４、第２の共通電極６、個別電極側接続パッド１１、共通電極側接続パッド１２を被着形成する。
【0113】
このうち、第２の共通電極６は、高抵抗基板１の中央付近に配列された発光ダイオードの配列ラインを挟み、一方側、例えば図面の上部側の第２の絶縁膜８に形成され、個別電極４、第２の共通電極６、接続パッド１１、１２は、他方側、例えば図面の下部側の第２の絶縁膜８に形成される。即ち、第２の共通電極６は、発光ダイオードの一導電型半導体層２のオーミックコンタクト層２ｃと、所定の第１の共通電極５が露出するコンタクトホール９に跨がるように形成される。また、第１の共通電極５とこの共通電極５と接続する接続パッド１１とは、コンタンクホール１０から発光素子群で区分される境界部分の間を介して延びる引出し電極１３によって、共通電極側接続パッド１２に接続されている。
【0114】
これらの第２の共通電極６、個別電極４とは、半導体－金属接触性を考慮した材料を用いる必要があり、接続パッド１１、１２は半導体－金属接触性を考慮する必要はない。従って、この第２の共通電極６、個別電極４、個別電極側接続パッド１１、共通電極側接続パッド１２とを同一工程で形成してもよいし、例えば、第２の共通電極６、個別電極４を半導体－金属接触性の良好な材料、良好な層構成で形成し、その後、個別電極側接続パッド１１、共通電極側接続パッド１２のみを良導電性の材料で形成しても構わない。
【0115】
たとえば、個別電極４、第２の共通電極6、個別電極側接続パッド１１、共通電極側接続パッド１２を同時に形成する場合に半導体－金属接触性を考慮して、クロムと金ゲルマニウムと金を蒸着法やスパッタリング法で順次積層して、Cr／AuGe／Auの層構成とすればよい。
【0116】
以上のようにして製造された発光ダイオードアレイ装置は、高抵抗基板１上に複数の一導電型半導体層２と逆導電型半導体層３を被着形成し、且つ該一導電型半導体層２に共通電極５０を、逆導電型半導体層３に個別電極４を接続した発光ダイオード１０を複数個配列するとともに、前記複数の配列された発光ダイオード１０のうち、所定数の発光ダイオード１０を一つの発光素子群として、複数発光素子群から構成される発光ダイオードアレイと、同一の群内の発光ダイオード１０の逆電型半導体層３に個別電極４を接続し、異なる群に属する所定番目に配置された発光ダイオードの一導電型半導体層２に共通電極５０に接続した発光ダイオードアレイ装置である。そして、共通電極５０は、発光ダイオード１０の配列方向に概略平行に延びる第１の共通電極５及び該第１の共通電極５の一部から各異なる群に属する所定の発光ダイオード１０の一導電型半導体層２に接続する第２の共通電極６とから構成される。
【0117】
なお、第１の共通電極５は、高抵抗基板１上に形成した第１の絶縁膜７上に形成され、前記第２の共通電極６と第１の共通電極５との間には、第２の絶縁膜８が介在され、第２の共通電極６の一部が、コンタンクトホール９を介して第１の共通電極５に重畳して接続されている。
【0118】

これにより、第１の共通電極５を、発光素子群を構成する発光ダイオード１０の数に相当する数だけ形成され、各発光ダイオード１０は、第２の共通電極６を介して、所定の第１の共通電極５に接続されている。この第２の共通電極６は、どの発光素子群に属する発光ダイオード１０でありながら、その接続構造は、実質的に同一構造となる。即ち、どの発光ダイオード１０であっても、接続部であるコンタクホール９は１個所のみとなる。これにより、発光ダイオード１０に接続する共通電極５０の構造が非常に簡素化し、接続条件が均一となるため、電極における抵抗のバラツキが小さく、これにより、発光ダイオードの発光バラツキを小さくすることができる。

【0119】

また、第１の共通電極５と第２の共通電極６、個別電極側接続パッド１１、共通電極側接続パッド１２をそれぞれ別の導体材料で構成できるため、第２の共通電極６、個別電極４では、安定した金属－半導体接触性を考慮した材料を、第１の共通電極５では、良好な導電性を考慮した材料を選択できるため、これによっても、電極抵抗のバラツキが小さくなり、これにより、発光ダイオードの発光バラツキを小さくすることができる。

【0120】

また、第１の共通電極５が高抵抗基板１に形成した第１の絶縁膜７上に形成されている。この絶縁膜７の下部には、基板の凹凸の構造物、他の導体膜の凹凸が一切ない、この絶縁膜７の表面が非常に平坦化することになる。このため、第１の共通電極５を非常に安定した形成できる。これより、第１の共通電極５は構造的にバラツキが少ないものとなる。

【0121】

また、個別電極側接続パッド１１、共通電極側接続パッド１２は、発光ダイオードの配列領域を中心に個別電極形成領域Ｓに集中されており、共通電極５０（第１の共通電極５及び第２の共通電極６の接続構造）は、発光ダイオード１０の共通電極形成領域Ｃに集中されている。

【0122】

これにより、外部の駆動回路との接続が一方側の領域のみで行われるため、駆動回路の接続が容易となる。

【0123】

また、個別電極側接続パッド１１、共通電極側接続パッド１２の下部領域には、従来のように共通電極などが全く配置されていない。従って、この接続パッド１１、１２と駆動回路が形成された回路基板とを接続するにあたり、個別電極側接続パッド１１、共通電極側接続パッド１２に半田バンプなどのように半田接合やボンディングワイヤによる接合をおこなっても、熱衝撃や機械的衝撃が個別電極側接続パッド１１、共通電極側接続パッド１２接続パッド１１、１２に印加されても、共通電極や個別電極の接続構造に悪影響を与えることが一切なく、安定した発光動作が可能となる。

【図面の簡単な説明】

【0124】

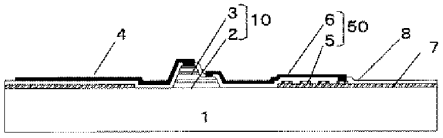
【図1】本発明に係る発光ダイオードアレイ装置の概略断面図である。
【図2】本発明に係る発光ダイオードの主要部分の断面図である。
【図3】本発明に係る発光ダイオードアレイ装置の平面図である。
【図4】本発明に係る発光ダイオードアレイ装置の電極構造を示す平面図である。
【図5】本発明に係る発光ダイオードアレイ装置の製造方法の一工程の平面図である。
【図6】本発明に係る発光ダイオードアレイ装置の製造方法の一工程の平面図である。
【図7】本発明に係る発光ダイオードアレイ装置の製造方法の一工程の平面図である。
【図8】本発明に係る発光ダイオードアレイ装置の製造方法の一工程の平面図である。
【図9】本発明に係る発光ダイオードアレイ装置の製造方法の一工程の平面図である。
【図10】本発明に係る発光ダイオードアレイ装置の製造方法の一工程の平面図である。
【図11】従来の発光ダイオードアレイ装置の主要部分の断面図である。
【図12】従来の発光ダイオードアレイ装置の下部側電極を説明する平面図である。
【図13】従来の発光ダイオードアレイ装置の上部側電極を説明する平面図である。

【符号の説明】

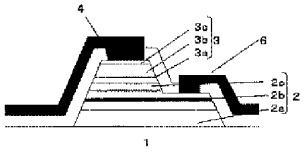
【0125】

１・・高抵抗基板
１０・・発光ダイオード
２・・・一導電型半導体層
　２ａ・・・バッファ層
２ｂ・・オーミックコンタクト層・・・第２の共通電極
２ｃ・・電子の注入層
３・・・逆導電型半導体層
　　３ａ・・・発光層
　　３ｂ・・・第２のクラッド層
　　３ｃ・・・第２のオーミックコンタクト層３・・・個別電極
４・・個別電極
５０・・・共通電極
　５・・・第１の共通電極
　６・・・第２の共通電極
７・・・第１の絶縁膜
８・・・第２の絶縁膜
９・・・コンタクトホール
１０・・コンタクトホール
１１・・個別電極側接続パッド
１２・・共通電極側接続パッド
１３・・引出し電極

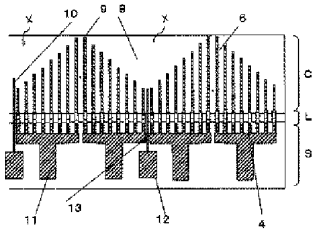
【図1】



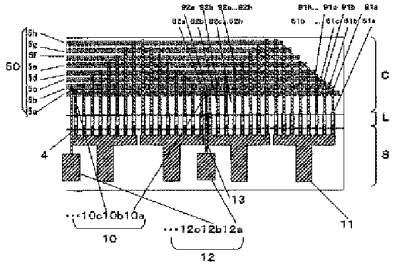
【図2】



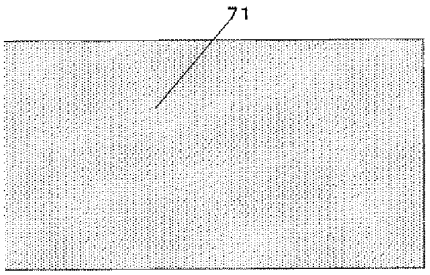
【図3】



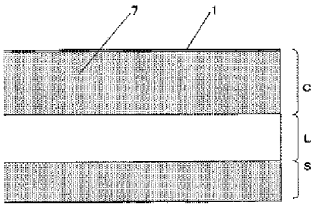
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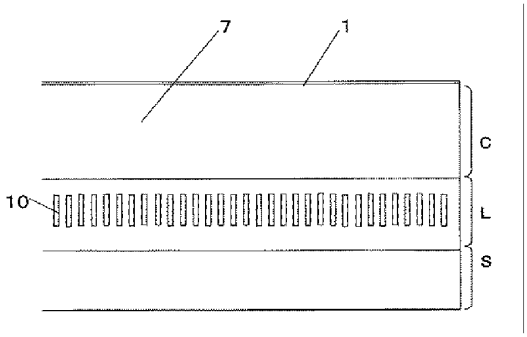
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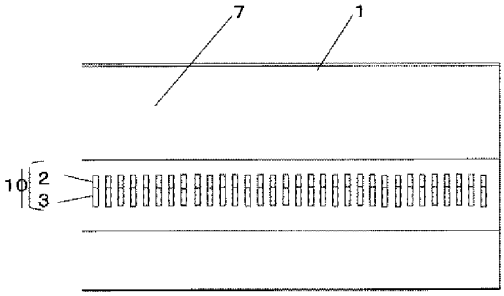
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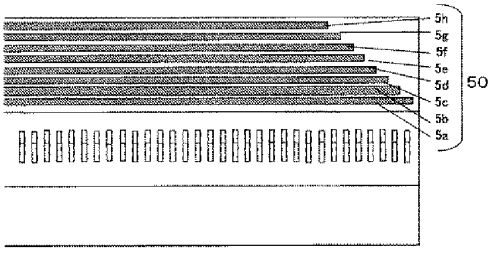
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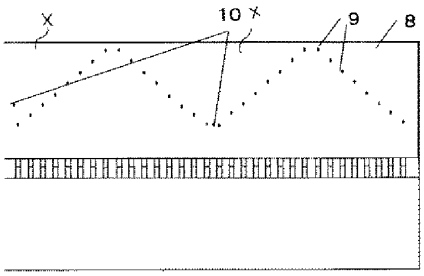
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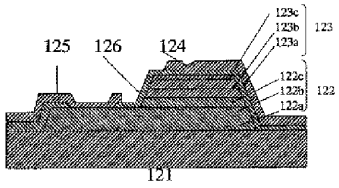
【図9】



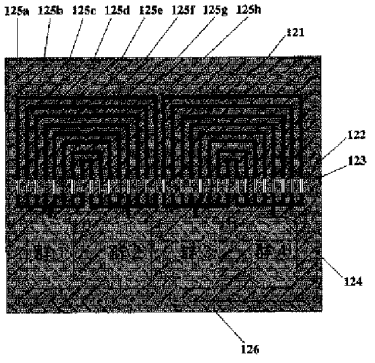
【図10】



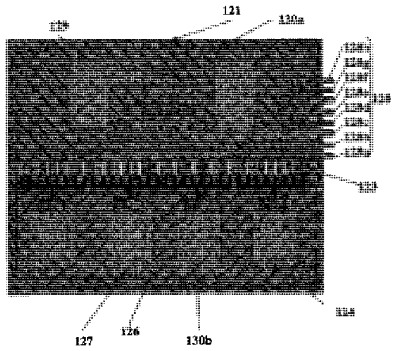
【図11】



【図12】



【図13】



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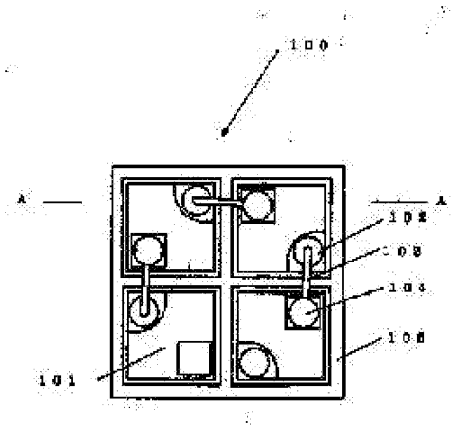
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(71)Applicant : NICHIA CHEM IND LTD
(72)Inventor : KOMAKI TOSHIO
KITANO AKIYUKI

(54) NITRIDE SEMICONDUCTOR LIGHT EMITTING ELEMENT

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a nitride semiconductor light emitting element which utilizes a nitride semiconductor and can emit high-luminance light at a high luminous efficiency.
SOLUTION: The light emitting element is constituted by laminating nitride semiconductors containing at least Ga upon a substrate in p- and n-type. Particularly, a plurality of nitride semiconductor layers is formed on the same film- forming substrate in a state where the layers are electrically separated from each other and each nitride semiconductor layer is electrically connected with a conductive wire.



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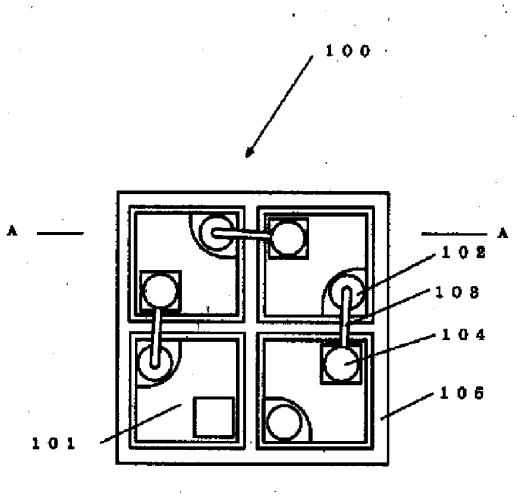
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Ｆターム(参考)　5F041 AA03 CA34 CA40 CA74 CB25
DA07

(54)【発明の名称】　窒化物半導体発光素子

(57)【要約】
【課題】窒化物半導体を利用した発光素子に関わり、特に発光効率を高めより高輝度に発光可能な窒化物半導体発光素子を提供するものである。
【解決手段】少なくともＧａを含む窒化物半導体が基板上にｐ型及びｎ型に積層された有する発光素子である。特に、窒化物半導体層は同一成膜基板上で電気的に複数分離してなり、それぞれの窒化物半導体層が導電性ワイヤで電気的に接続されている窒化物半導体発光素子である。



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【特許請求の範囲】

【請求項１】　基板上にｐ型及びｎ型に積層された少なくともＧａを含む窒化物半導体を有する発光素子であって．前記ｐ型及びｎ型に積層された少なくともＧａを含む窒化物半導体層は同一成膜基板上で電気的に複数分離してなり、それぞれ分離された個々の窒化物半導体層の電極を導電性ワイヤで電気的に直列及び／又は並列に接続されていることを特徴とする窒化物半導体発光素子。

【請求項２】　前記導電性ワイヤは．それぞれ電気的に分離された個々の窒化物半導体層の電極をボールボンディングを用いて順次結線されてなる請求項１に記載の窒化物半導体発光素子。

【請求項３】　前記窒化物半導体層の少なくとも一部の電極は、ステッチボンディングされたワイヤ上に．ボールボンディングされ隣接する窒化物半導体層の電極と電気的に接続されている請求項１に記載の窒化物半導体発光素子。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は窒化物半導体を利用した発光素子に関わり、特に発光効率を高めより高輝度に発光可能な窒化物半導体発光素子を提供するものである。

【０００２】

【従来技術】今日、窒化物半導体を利用した発光素子はそのバンドギャップによって紫外域から赤色領域までが効率よく発光可能な発光素子として注目されている。このような窒化物半導体を用いた発光素子４００の一例を図４に示す。図４にはサファイア基板上にＧａＮのバッファ層を介してｎ型ＧａＮを利用したｎ型コンタクト層．多重量子井戸構造とされるＧａＮ層とＩｎＧａＮ層とを複数層積層させた発光層、ｐ型ＡｌＧａＮのクラッド層．ｐ型ＧａＮのｐ型コンタクト層及びｐ型コンタクト層からなる窒化物半導体層４０１が形成されＬＥＤチップである発光ダイオードを構成している。ｎ型コンタクト層の一部は露出されｎ型電極４０２が又透光性電極４０３上にはｐ型電極４０４が積層されている。ｎ型及びｐ型電極に電流を流すことにより．ＬＥＤチップから所望の発光スペクトルを効率よく放出させることができる。

【０００３】しかしながら．窒化物半導体を利用した発光素子の利用分野が広がるにつれて．より発光輝度が高く．且つ消費電力の低い発光効率の優れた発光素子が要望されている。特に、窒化物半導体を利用した発光素子はその半導体特性が十分解明されていないことから、発光素子の効率向上が極めて難しい。

【０００４】

【発明が解決しようとする課題】したがって、上記発光素子の構成では十分ではなく、本発明は更なる発光効率向上が可能な窒化物半導体を利用した発光素子を提供することにある。

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【０００５】

【課題を解決するための手段】本発明は、基板上にｐ型及びｎ型に積層された少なくともＧａを含む窒化物半導体を有する発光素子である。特に、ｐ型及びｎ型に積層された少なくともＧａを含む窒化物半導体層は同一成膜基板上で電気的に複数分離してなり．それぞれ分離された個々の窒化物半導体層の電極を導電性ワイヤで電気的に直列及び／又は並列に接続されている窒化物半導体発光素子である。これによって、より発光輝度が高く、且つ消費電力の低い発光効率の優れた発光素子とすることができる。

【０００６】本発明の請求項２に記載の窒化物半導体発光素子は、導電性ワイヤがそれぞれ電気的に分離された個々の窒化物半導体層の電極をボールボンディングを用いて順次結線されてなる窒化物半導体発光素子である。これによって．ウエッジボンダーを用いて結線されたものと比べステッチボンドと同等の結線を行うことができる。したがって．成膜基板上に形成された各窒化物半導体の配置や方向性に関係なくボンディングすることが可能となる。これにより異種混合されたパターンでのボンディング可能化・ボンディング時間の短縮・電極接合強度の向上を図ることができる。

【０００７】本発明の請求項３に記載の窒化物半導体発光素子は、窒化物半導体層の少なくとも一部の電極は、ステッチボンディングされたワイヤ上に、ボールボンディングされ隣接する窒化物半導体層の電極と電気的に接続されてなる窒化物半導体発光素子である。これによって．ステッチボンディング上にボールボンディングをする場合においても、同一成膜基板上であるため信頼性よく比較的強固に密着することができる。また、小型化時においても量産性よく窒化物半導体を形成させることができる。これによって、より発光効率を高めた窒化物半導体発光素子とすることができる。

【０００８】

【発明の実施の形態】本発明は種々の実験の結果．窒化物半導体発光素子から放出される光は同一電圧を印可したときに発光する発光強度はその面積の大きさに比例しないことを見出し本発明をなすに至った。さらに．このような発光素子における結線がで量産性や信頼性が大きく変わることを見出し本発明を成すにいたった。

【０００９】すなわち、窒化物半導体発光素子においては同一電流を流した場合．発光素子を大きくすればするほど．その発光面積の増大に伴って発光輝度が高くなるものではない。むしろ発光効率が低下する傾向にある。そのため、本発明は複数の窒化物半導体を直列接続させた発光素子とすることにより、同一発光面積の単一発光素子よりも発光効率の優れた発光素子としうるものである。なお、本発明による発光効率向上は不明であるが窒化物半導体自体の抵抗が高く、欠陥が多いことに起因し

ていると考えられる。次に、発光効率を向上させるために、同一成膜基板上を複数の窒化物半導体を積層させ、それぞれの電極を導電性ワイヤを用いて電気的に接続させた場合、直並列接続の組合せによっては極めて狭い箇所に方向性なく強固にワイヤを密着させる必要がある。このような場合、ボールボンディングを利用し、ステッチボンディング上には再びボールを形成させることで安定性よく密着性を向上させることができる。特に、本発明のごときく極めて狭い空間でもワイヤボンディングさせる場合は、同一成膜基板にステッチボンド及びボールボンドを続けて行っても安定して密着性よく形成することができる。

【００１０】以下、本発明の窒化物半導体発光素子について図1を用いて説明する。図１は本発明の窒化物半導体発光素子を示した模式的平面図であり、図２は図１のＡＡ断面図である。略矩形状のサファイア基板１０５上に複数の島状に分離した窒化物半導体層１０１が形成されている。島状に分離した窒化物半導体層１０１はそれぞれがサファイア基板１０５上に、ＧａＮを用いたバッファ層２０１、ｎ型コンタクト層となるＧａＮ２０２、ＩｎＧａＮとＧａＮとを複数組積層させた量子井戸構造とされる発光層２０３、ｐ型クラッド層となるＡｌＧａＮ２０４、ｐ型コンタクト層となるＧａＮ２０５が順次積層されている。ｐ型コンタクト層上にはほぼ全面に透光性電極２０６及びその上にｐ型台座電極２０７が設けられている。他方、エッチングにより矩形状窒化物半導体の一部を部分的に除去してｎ型コンタクト層を露出させてある。なお、ｎ型コンタクト層の露出とサファイア基板上に各窒化物半導体を島状に分離させることをエッチングにより同時に行うこともできる。ｎ型コンタクト層上にはｎ型の台座電極が形成されており、平面状から見てｐ型台座電極とｎ型台座電極とが矩形形状の対向する隅部に配置されている。また、島状に分離された各ｐ型及びｎ型の台座電極は、サファイア基板の外周状に沿って隣り合う島状の窒化物半導体と近接して配置されている。少なくとも一箇所のｐ型及びｎ型台座電極間は金線を利用してダイボンド接続され直列接続されている。台座電極間が近接して配置されているために、金線の使用量が極めて少なくてすむ。また、対向する隅部に各ｐ型及びｎ型の台座電極が設けられていることにより、島状に分離した窒化物半導体層から均一に発光することができる。さらに、サファイア基板の外周に沿ってｐ型及びｎ型の台座電極が設けられていることにより、窒化物半導体発光素子の中心光度を向上させることができる。そのため、このような発光素子をレンズ効果のあるモールド部材で被覆させるときには光学設計を極めて簡単に行うことができる。なお、各島状の窒化物半導体層を電気的に絶縁するために絶縁性保護膜２０８を形成してもよい。

【００１１】図中では４個の島状に分離させたｐ型及びｎ型がそれぞれ積層された窒化物半導体を金線で３箇所直列に接続させてある。金線にて接続させていない隣接する窒化物半導体層上のｐ型及びｎ型の台座電極は、窒化物半導体発光素子のｐ電極及びｎ電極として機能することとなる。各ワイヤー１０３は、窒化物半導体層の一方の電極上でボールボンディングし第一のボール部１０２を形成した後、隣接する窒化物半導体層の電極とステッチボンディングする。このステッチボンディング部にはこの上から更にボールボンディングを行い第二のボール部１０４を形成させる。以下、本発明の窒化物半導体発光素子の具体的形成方法について説明するがこれのみに限られないことはいうまでもない。

【００１２】

【実施例】あらかじめ、酸で表面を洗浄させた２インチのサファイア基板（α－アルミナ基板）をＭＯＣＶＤ法を利用する反応装置内に配置させる。真空排気後、１０００℃にまで上げクリーニングを行う。続いて、水素ガスを流しながら大気圧とさせる。次に、成膜温度を５３０℃に下げ反応装置内に、原料ガスとしてＴＭＧ（トリメチルガリウム）、窒素ガスをキャリアガスとして水素ガスと共に流し、厚さ約２００ÅのＧａＮ層を成膜させる。なお、バッファ層は窒化物半導体と基板との格子不整合を緩和させるために設けられるものであり、ＧａＮの他、ＡｌＮ、ＧａＡｌＮなどを好適に利用することができる。また、基板はサファイアの他、スピネル、ルビーなど種々のものを利用することができる。

【００１３】次に、一旦キャリアガスのみとした後に成膜温度を１０５０℃に上げる。成膜温度が一定となった後に原料ガスとしてＴＭＧガス、窒素ガス、ドーパントガスとしてシランガス、キャリアガスとして水素ガスを流しｎ型ＧａＮであるコンタクト層兼クラッド層を成膜させる。なお、窒化物半導体は静電耐圧が他の半導体に比べて低いため、ｎ型コンタクト層をアンドープのＧａＮなどでサンドイッチさせ結晶性と耐電圧を向上させ得るように構成しても良い。

【００１４】次に、活性層としてＧａＮとＩｎＧａＮの多層膜を形成させる。成膜温度を１０５０℃に維持したまま、原料ガスとしてＴＭＧガス、窒素ガス及びキャリアガスとして水素ガスを流してＧａＮ層を形成する。続いて、一旦キャリアガスのみとして、成膜温度を８００℃にまで低下させる。温度が一定となった後に、原料ガスとしてＴＭＧガス、ＴＭＩ（トリメチルインジウム）ガス、窒素ガスを流し、ＩｎＧａＮ層を形成させる。これを３回繰り返した後、最後に上述のアンドープＧａＮと同様の成膜条件にてＧａＮ層を成膜させる。これにより、多重量子井戸構造とされる活性層を成膜させる。発光素子の発光スペクトルは井戸層のバンドギャップに左右されるためＩｎＧａＮの他、ＡｌＧａＩｎＮやＡｌＧａＮなどとすることができる。同様に、Ｓｉなどのｎ型不純物やＭｇなどのｐ型不純物を含有させることもでき

る。

【００１５】活性層成膜後、成膜温度を１０５０℃に保持して、原料ガスをＴＭＡ（トリメチルアルミニウム）ガス、ＴＭＧガス、窒素ガス、ドーパントガスとしてCp_2Mgガス及びキャリアガスとして水素ガスを流し、ｐ型クラッド層となるＡｌＧａＮ層を成膜させる。ｐ型クラッド層は結晶性を向上させためにＧａＮとＡｌＧａＮの超格子構造とさせることもできる。

【００１６】成膜温度を維持したまま、原料ガスをＴＭＧガス、窒素ガス、ドーピングガスとしてCp_2Mgガス及びキャリアガスとして水素ガスを流し、ｐ型コンタクト層となるＧａＮ層を成膜させることができる。

【００１７】こうして成膜させた窒化物半導体ウエハにマスクをかけた後、エッチングにより本発明のごとく、同一成膜基板上に電気的に分離され且つ、ｐｎ接合などを持った複数の島状半導体の窒化物半導体を個々に形成する。ｎ型電極を形成させるｎ型コンタクト層の一部及び窒化物半導体を島状に分離させマスクを除去後、再び電極形成用のマスクを形成させてスパッタリング法によりｐ型透光性電極としてＡｕを成膜させる。

【００１８】ｐ型台座電極としてＮｉ／Ａｕ及びｎ型台座電極としてＷ／Ａｌを、あらかじめ図１のごとく配置できるようにマスクを形成してある。電極形成後、電極表面を残して、SiO_2により保護膜を形成させる。

【００１９】続いて島状に分離した４個の窒化物半導体をひとまとめにして、ダイサー及びスクライバーにより分離した溝に沿ってサファイア基板を切断する。

【００２０】次に、島状の窒化物半導体のｎ型台座電極と、隣り合う島状の窒化物半導体のｐ型台座電極とをワイヤボンディングにより電気的に直列接続させる。より具体的には、あらかじめ金線にボールを形成させた後、島状窒化物半導体のｎ型台座電極或いはｐ型台座電極にボールボンディングさせる。ボールボンディングさせた金線を延ばしつつ、隣り合う島状窒化物半導体のｐ型台座電極或いはｎ型台座電極にステッチボンディングさせ隣り合う島状窒化物半導体を直列接続させる。続いて、成膜基板上に形成された窒化物半導体を固定させるワークを回転させることなく、一度ステッチボンディングさせたワイヤ上に再びボールボンディングを行う。続いて、ステッチボンディング上にボールボンディングさせた金線を延ばしつつ、次に隣り合う隣り合う島状窒化物半導体のｐ型台座電極或いはｎ型台座電極にステッチボンディングさせ隣り合う島状窒化物半導体を電気的に直列接続させる。なお、窒化物半導体の大きさが極めて小さい場合、ボールボンディングをｎ型及びｐ型台座電極に直接押しつけることによって一度に直列接続させることもできる。

【００２１】同一の発光面積を持った単一窒化物半導体発光素子に比べて、同一成膜基板上に形成させた複数の窒化物半導体からなる窒化物半導体発光素子の方が発光効率が高い。そのために直列接続のみに限らず、並列接続或いは直並列接続した本発明の窒化物半導体発光素子とさせることもできる。また、各島状窒化物半導体を集中して配置させることもできるし、図３のごとく、直線上に配置させることもできる。サファイア基板３０５上に形成させた島状の窒化物半導体素子３０１を図３（Ａ）に示すようにワイヤー３０３で直列接続させる場合、各島状窒化物半導体に抵抗を少なく電流を流す必要があることからボワイヤボンディングにより直列接続させることが好ましい。特に、ボールボンディングさせた第一のボール部３０２の他方に形成されるステッチボンディング上には再びボールとして第二のボール部３０４を形成することが好ましい。同様に図３（Ｂ）に示すごとく並列接続させることもできる。

【００２２】島状窒化物半導体の個々の大きさが約１５０μｍ角として上述の窒化物半導体発光素子を形成させる。また、本発明と比較のために発光面積がほぼ同様とさせ、一つの窒化物半導体を積層させた以外は同様にして約６００μｍ角の窒化物半導体発光素子を形成させる。本発明の窒化物半導体発光素子の発光強度を１００として比較したところ、比較のための発光素子は８２％にしかすぎなかった。本発明の窒化物半導体は一つの窒化物半導体に比較して発光効率が優れていることが分かったが、島状窒化物半導体の個々の大きさがそれぞれ約８０μｍより大きく、約３００μｍ未満において、より量産性を満たしつつ効率を向上させることができる。したがって、より発光面積の大きい窒化物半導体を高輝度に発光させるためには、個々に分割させた窒化物半導体を直列に接続させた窒化物半導体とすることが好ましい。なお、図においては、正方形の窒化物半導体素子のみを示したが、サファイア基板の分離しやすさのために菱形やフリップチップ実装を考慮した長方形としたものにも応用できる。

【００２３】

【発明の効果】本発明の窒化物半導体発光素子とすることによって、大面積においても効率よく発光可能な窒化物半導体発光素子とすることができる。また、ウエッジボンダーでのステッチボンドではできなかった方向性なくボンディングすることが可能となる。したがって、異種混合されたパターンでのボンディグ可能化・ボンディグ時間の短縮・電極接合強度の向上を図ることが可能となる。

【図面の簡単な説明】

【図１】　本発明の窒化物半導体発光素子の模式的平面図である。

【図２】　図１のＡＡ断面における模式的断面図である。

【図３】　図３（Ａ）は直列接続させた本発明の別の窒化物半導体発光素子の模式的平面図であり、図３（Ｂ）は、並列接続させた本発明の窒化物半導体発光素子の模

式的平面図である。

【図４】　本発明と比較のために示す窒化物半導体発光素子の模式的平面図である。

【符号の説明】

１００…本発明の窒化物半導体発光素子

１０１…同一成膜基板上に形成された個々の島状窒化物半導体

１０２…第一のボール部

１０３…ワイヤー

１０４…スッテチボンディグ上に形成された第二のボール部

１０５…サファイア基板

２０１…バッファ層

２０２…ｎ型コンタクト層

２０３…多重量子井戸構造とされる活性層

２０４…ｐ型クラッド層

２０５…ｐ型コンタクト層

２０６…透光性電極

２０７…ｐ型台座電極

２０８…絶縁性保護膜

３００…直列接続された本発明の窒化物半導体発光素子

３01…同一成膜基板上に形成された個々の島状窒化物半導体

３０２…ワイヤーのボール

３０３…ワイヤー

３０４…スッテチボンディグ上に形成されたボール

３０５…サファイア基板

３０１…並列接続された本発明の窒化物半導体発光素子

４００…本発明と比較のために示された窒化物半導体発光素子

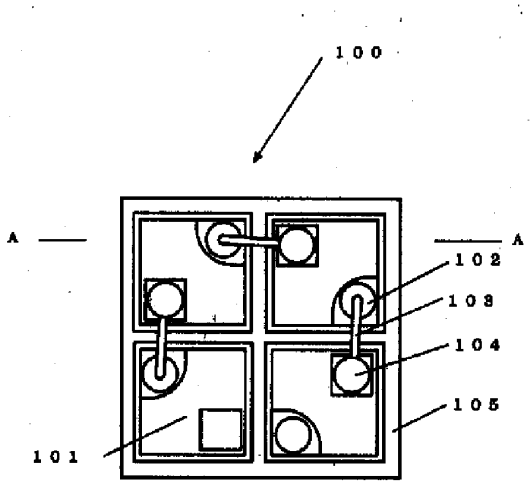
４０１…窒化物半導体層

４０２…ｎ型電極

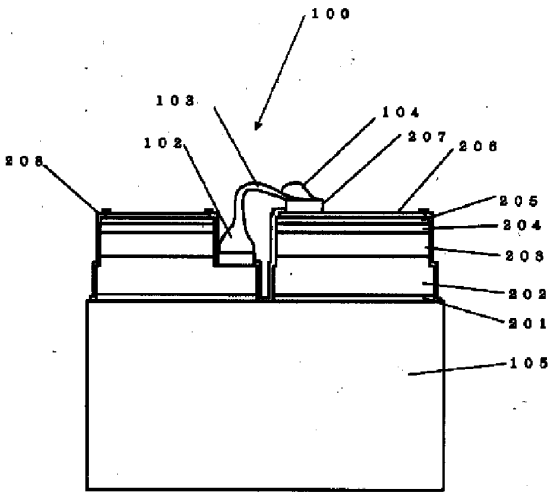
４０３…透光性電極

４０４…ｐ型電極

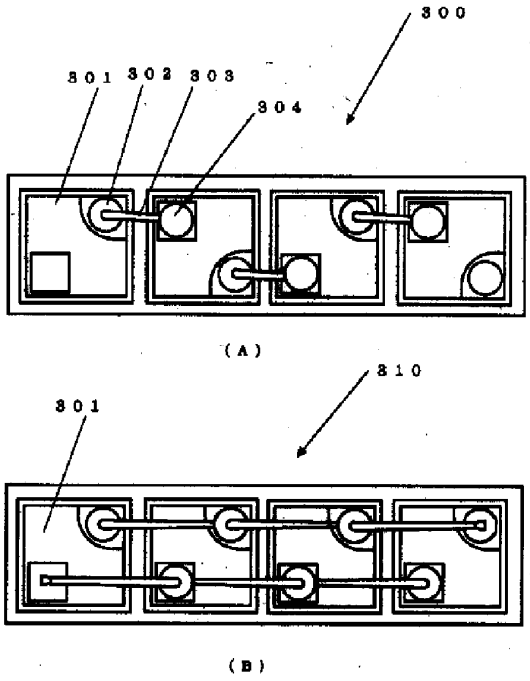
【図１】



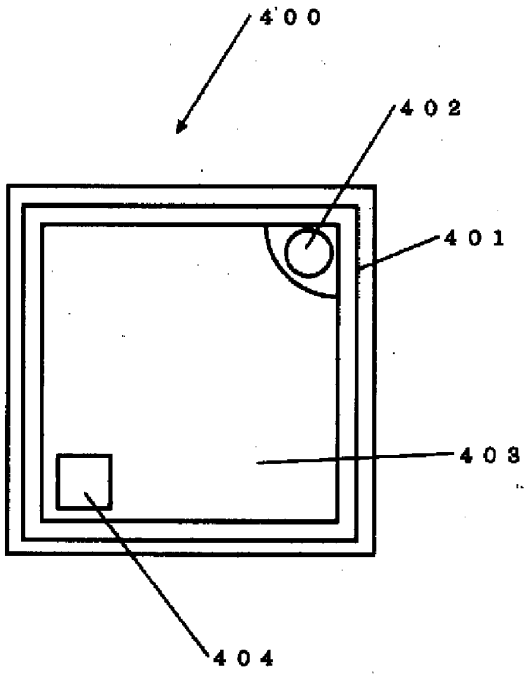
【図２】



【図3】



【図4】



Electronic Acknowledgement Receipt

EFS ID:	6887381
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	P2317US00_IDS_TRANSMITTAL.pdf	32363 9156f5fcff9228daaafe079406e7cecfd6536116	no	4

Warnings:	
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2	Foreign Reference	P2317US00_1_JP_2004071644.pdf	1295688 61b5f3e219b34413a55616b2da723c5b0fca5635	no	21
Warnings:					
Information:					
3	Foreign Reference	P2317US00_2_JP_2004273746.pdf	452760 6a6c30e4d8e4dc04402e85af8dab10c09e5e61eb	no	11
Warnings:					
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4	Foreign Reference	P2317US00_3_JP_2005136130.pdf	1131293 7061ae42e77f9d228e16312ad66e9f1831f85f60	no	22
Warnings:					
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5	Foreign Reference	P2317US00_4_JP_2001-156331.pdf	327701 037fb1598d7654195bbe73f54b420695dd83de4c	no	7
Warnings:					
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			Total Files Size (in bytes):	3239805	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/993,965	12/26/2007	Jong Lam Lee	P2317US00	2191

58027 7590 02/05/2010

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EXAMINER	
NGUYEN, THINH T	
ART UNIT	**PAPER NUMBER**
2818	

NOTIFICATION DATE	DELIVERY MODE
02/05/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATENT@PARK-LAW.COM

Office Action Summary	Application No.	Applicant(s)	
	11/993,965	LEE ET AL.	
	Examiner	Art Unit	
	THINH T. NGUYEN	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 17-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 17-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :12/26/07,7/30/08,8/29/08,2/9/09,11/5/09,1/27/10.

DETAILED OFFICE ACTION

1. Claims 1-4,17-31 are pending in the Application.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, -- "AI, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof disposed on a rear surface of the substrate on which the light emitting cell is formed. "-- in claim 31 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 31 is objected to because it lacks enablement that can make the claim not in compliance with 35 USC 112 first paragraph because Applicant fails to show what kind of structure of embodiment the , -- "AI, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof disposed on a rear surface of the substrate on which the light emitting cell is formed. "-- in claim 31 can take.

Correction is required.

4. The Examiner note that some pending claims of this Application has a product by process limitation. Please note that in a product-by-process claim, it is the patentability of the claimed product and not of the recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. The Patent Office is not equipped to manufacture products by a myriad of processes put before it and then obtain prior art product and make physical comparisons therewith. In re Brown, 173 USPQ 685 (CCPA 1972). Also, a product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ I S at 17 (footnote 3). See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al., 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a " product by process" claim, and not the

patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 3,4,25-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regard to claim 3, Claim 3 is indefinite because the limitation – "transparent electrode layer"-- lacks antecedent basis.

With regard to claim 4, Claim 3 is indefinite because the limitation – "ohmic metal layers"-- lacks antecedent basis..

With regard to claim 25, Claim 25 is indefinite because the limitations – "first type bonding pad "-- , – "second type bonding pad "-- lacks antecedent basis..

With regard to claim 26-30, these claims are indefinite because they depend on an indefinite base claim; furthermore the limitation – " same process" – in claims 27,28 lacks antecedent basis.

With regard to claim 31 Claim 31 is indefinite because the limitation – "an alloy thereof disposed on a rear surface of the substrate "-- lacks antecedent basis. More over claim 31 is unclear because the embodiment of the – " AI, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof disposed on a rear surface of the substrate on which the light emitting cell is formed. "-- is not shown on the drawing therefore it is not possible to determine the metes and bound that the Applicant seeks patent protection.

7. To Expedite the prosecution of the Application , the Examiner assume that the Applicant will correct the deficiencies of the drawings and the claims to make them in compliance with the rule and 35 USC 112 first and second paragraph and will examines the claims as best as the examiner can understand them

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible

harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 1-4,17-21 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1-14 of copending Application No. 12/568,630. Although the conflicting claims are not identical, they are not patentably distinct from each other.

A person skilled in the art at the time the invention was made would have been able to use the disclosures by claim 1-14 of Application No. 12/568,630 and make routine modification or optimization using his knowledge at the time the invention was made in order to arrive at the inventions of claims 1-4, 17-21 of the current Application. It would have been obvious to one of ordinary skill in the art at the time the invention was made to select known available materials and technologically feasible size and shapes as recited in claims1-4,17-21

This is a **provisional** obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that forms the basis for the rejections under this section made in this office action.

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
>
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

11. Claim 1-2, 4,17-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Fan et al. (U.S. Patent 7,535,028.).thereafter Fan 028

With regard to claim 1, Fan 028 discloses (fig 2,fig 3) a light emitting device, comprising: a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer (elements 20,16,fig 2, ,column 3 lines 24,50) formed on a portion of the N-type semiconductor layer on a substrate (fig 2 ,element 12) , wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, (fig 2,fig 3) and a side surface including the N-type or P-type semiconductor layer of the light emitting cell has a slope of 20 to 80 o from a horizontal plane (column 4 lines 5-20).

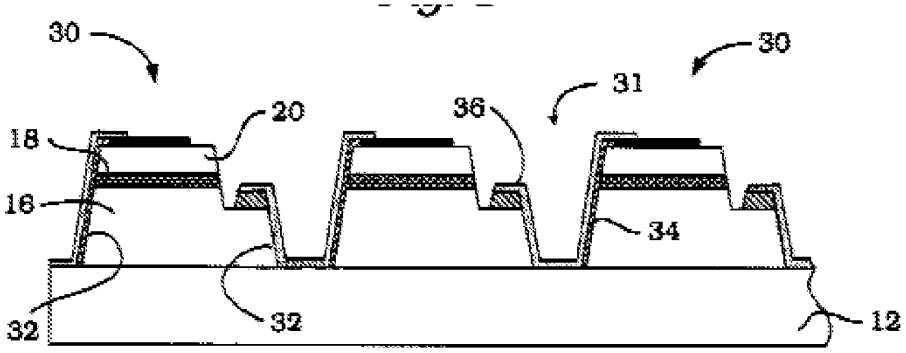


Fig. 2

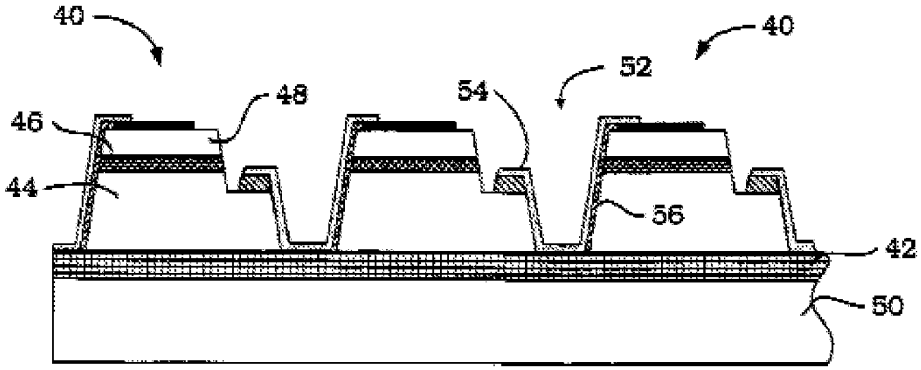


Fig. 3

FAN 028 DISCLOSURES.

With regard to claim 2, Fan 028 discloses (fig 2,fig 3) a light emitting device, comprising a wire for connecting the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

With regard to claim 4, Fan 028 discloses (fig 2,fig 3) a light emitting device,

With regard to claim 17-23 , Fan 028 discloses (fig 2,fig 3) a light emitting device comprising: a substrate; and a plurality of light emitting cells disposed on the substrate to be spaced apart from each other, wherein the light emitting cell comprises a first-type

semiconductor layer and a second-type semiconductor layer, (column 3 lines 24-50) at least one of the light emitting cells has at least one side surface that is not perpendicular to a horizontal plane, and the first-type semiconductor layer of at least one of the light emitting cells is electrically connected to the second-type semiconductor layer of an adjacent another light emitting cell.(column 4 lines 6-34); or wherein the side surface that is not perpendicular is inclined at a slope with respect to the horizontal plane or wherein the slope is approximately 20° to approximately 80° with respect to the horizontal plane 9 column 4 lines 5-20) ;or .wherein the inclined surface of the light emitting cell comprises at least a side surface of the first-type semiconductor layer ; or wherein the first-type semiconductor layer is an N-type semiconductor layer ; or wherein the inclined surface of the light emitting cell is formed continuously up to the second-type semiconductor layer ; or wherein the second-type semiconductor layer is a P-type semiconductor layer

Claim Rejections - 35 USC § 103

12. The following is a quotation of U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 3,25-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fan et al. (U.S. Patent 7,535,028.).thereafter Fan 028

With regard to claim 3, as set forth in the rejection of claim 1, Fan 028 discloses all the invention except for the use of transparent electrode on the P-side. This limitation however, is considered obvious because the use of transparent electrode is a features known in the art at the time the invention was made (see US patent 6,608,330 by Yamada fig 1 layer 112) when the light is emitted in the vertical direction of the LED.

With regard to claim 24, as set forth in the rejection of claim 22 Fan 028 discloses all the invention except for the use the use of vertical of a vertical sidewall for the LED , this limitation , however, is considered obvious because the use of vertical sidewall for LED is known in the art at the time the invention was made.

With regard to claim 25,26 as set forth in the rejection of claim 20 and 25, Fan 028 discloses all the invention except for the use of bond pads. this limitation , however, is considered obvious because the use of bond pad used for wire bonding for LED is known in the art at the time the invention was made.(see US patent 5,652,434) note that a person skilled in the art at the time the invention was made would have been motivated to provide the Fan 028 device with bond pad for an extra option for wire bonding or other kind of electrical connection.

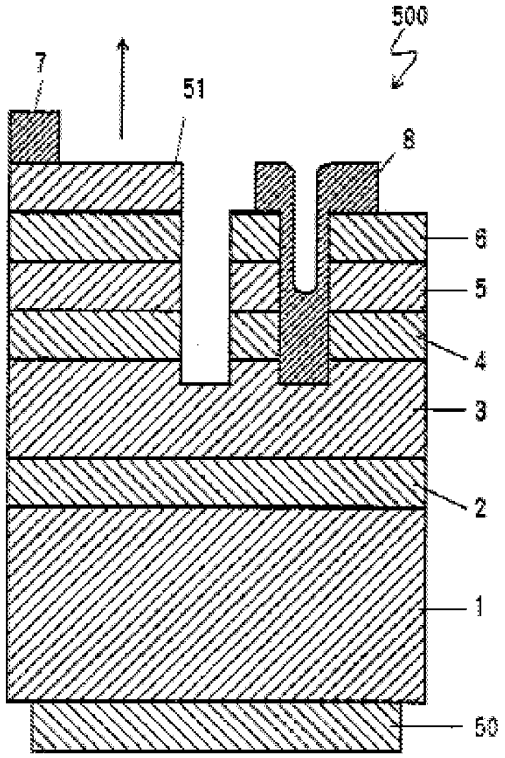
With regard to claim 27,28 , for the rationale set forth in paragraph 4 of this Office Action claim 27,28 are rendering obvious by the disclosure of Fan 028.

With regard to claim 29, Fan 028 discloses (fig 2,fig 3) a light emitting device, wherein the electrical connection is formed by an electrical conductor disposed on the inclined surface of the light emitting cell (fig 2 element 36, column 4 lines 25-35) .

With regard to claim 30, Fan 028 discloses (fig 2,fig 3) a light emitting device, The light emitting device wherein an insulation layer (fig 2 element 34) is disposed between the light emitting cell and the electrical conductor.

With regard to claim 31, as set forth in the rejection of claim 12, Fan 028 discloses all the invention except for AI, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof disposed on a rear surface of the substrate on which the light emitting cell is formed . this limitation , however, is considered obvious because the use of a metal layer to reflect light to increase the light output efficiency of an LED device is known in the art at the time the invention was made (see US 5,862,167 fig 5 layer 50).

F I G. 5



14. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

15. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

16. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d) which papers have been placed of record in the file.

CONCLUSION

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on Monday-Friday 9:30am-6: 30pm.If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached at 571-272-1657.The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/**Thinh T. Nguyen**/

Patent Examiner
Art Unit 2818

Notice of References Cited	Application/Control No. 11/993,965	Applicant(s)/Patent Under Reexamination LEE ET AL.	
	Examiner THINH T. NGUYEN	Art Unit 2818	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2010/0006870	01-2010	Lee et al.	257/88
*	B	US-7,535,028	05-2009	Fan et al.	257/88
*	C	US-6,608,330	08-2003	Yamada, Motokazu	257/90
*	D	US-5,652,434	07-1997	Nakamura et al.	257/13
*	E	US-5,862,167	01-1999	Sassa et al.	372/45.01
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11993965	LEE ET AL.
	Examiner	Art Unit
	THINH T NGUYEN	2818

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/06/2009	10/30/2009	01/30/2010						
	1	÷	÷	✓						
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	31			✓						

EAST Search History

EAST Search History (Prior Art)

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L22	30873	trapezoidal near shape	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/01/30 20:37
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EAST Search History

EAST Search History (Prior Art)

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L8	7	"7213942"	US-PGPUB; USPAT; USOCR	OR	OFF	2010/01/30 22:31
L9	7	"7213942"	US-PGPUB; USPAT; USOCR	OR	OFF	2010/01/30 22:34
L10	7	"7221044"	US-PGPUB; USPAT; USOCR	OR	OFF	2010/01/30 22:37

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
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L2	2	"20080251796"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/01/31 09:50
L3	10	"6635902"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/01/31 10:32
L4	0	3 and ITO	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/01/31 10:59
L5	8	"7221044"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/01/31 11:00
L6	2	"7535028"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/01/31 11:00
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L11	106031	transparent same electrode	US-PGPUB; USPAT; USOCR	OR	ON	2010/01/31 11:03
L12	350405	11 ITO	US-PGPUB; USPAT; USOCR	OR	ON	2010/01/31 11:03
L13	20	9 and 12	US-PGPUB; USPAT; USOCR	OR	ON	2010/01/31 11:04
L14	17	11 and 13	US-PGPUB; USPAT; USOCR	OR	ON	2010/01/31 11:04
L15	61453	transparent near2 electrode	US-PGPUB; USPAT; USOCR	OR	ON	2010/01/31 11:07

L16	69506	transparent near3 electrode	US-PGPUB; USPAT; USOCR	OR	ON	2010/01/31 11:07
L17	869	nichia.as.	US-PGPUB; USPAT; USOCR	OR	ON	2010/01/31 11:08
L18	58	15 and 17	US-PGPUB; USPAT; USOCR	OR	ON	2010/01/31 11:08
L19	224903	(reflecting metal) near layer	US-PGPUB; USPAT; USOCR	OR	ON	2010/01/31 12:36
L20	55270	substrate same (backside back adj side lower adj side)	US-PGPUB; USPAT; USOCR	OR	ON	2010/01/31 12:39
L21	2543	19 same 20	US-PGPUB; USPAT; USOCR	OR	ON	2010/01/31 12:40
L22	770935	LED	US-PGPUB; USPAT; USOCR	OR	ON	2010/01/31 12:41
L23	385	lumileds.as.	US-PGPUB; USPAT; USOCR	OR	ON	2010/01/31 12:41
L24	385	lumiled.as.	US-PGPUB; USPAT; USOCR	OR	ON	2010/01/31 12:41
L25	1	21 and 24	US-PGPUB; USPAT; USOCR	OR	ON	2010/01/31 12:42
L26	319	21 and 22	US-PGPUB; USPAT; USOCR	OR	ON	2010/01/31 12:44

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11993965	LEE ET AL.
	Examiner	Art Unit
	THINH T NGUYEN	2818

SEARCHED			
Class	Subclass	Date	Examiner
257	100, 266	9/16/09	ttn

SEARCH NOTES		
Search Notes	Date	Examiner
east	9/16/09	ttn
east	1/30/10	TTN

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed
PTO/SB/08a (06-09)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T
	Attorney Docket Number	P2317US00

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	1	2004-071644	JP		2004-03-04	NICHIA CHEM IND LTD		☐
	2	2004-273746	JP		2004-09-30	HITACHI CABLE LTD		☐
	3	2005-136130	JP		2005-05-26	KYOCERA CORP		☐

Receipt date: 01/27/2010	Application Number	11993965 11993965 - GAU: 2818
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T
	Attorney Docket Number	P2317US00

	4	2001-156331	JP		2001-06-08	NICHIA CHEM IND LTD		☐

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Receipt date: 01/27/2010	Application Number	11993965 11993965 - GAU: 2818
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T
	Attorney Docket Number	P2317US00

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2010-01-27
Name/Print	Hae-Chan Park	Registration Number	50114

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
	Art Unit	2811
	Examiner Name	
	Attorney Docket Number	P2317US00

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	1	04-023568	WO		2004-03-18	Nitride Semiconductors Co., Ltd.		☐
	2	04-013916	WO		2004-02-12	Nichia Corporation		☐
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Receipt date: 02/09/2009	Application Number	11993965 11993965 - GAU: 2818
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
	Art Unit	2811
	Examiner Name	
	Attorney Docket Number	P2317US00

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	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
	Art Unit	2811
	Examiner Name	
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	1	2004-079867	JP		2004-03-11	Sakai SHIRO Nitride Semiconductor Co., Ltd.		☐
	2	10-2003-0022940	KR		2003-03-19	Epivalley Co., Ltd.		☐
	3	10-2005-0052474	KR		2005-06-02	Sakai SHIRO et al.		☐

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Receipt date: 07/30/2008	Application Number	11993965 11993965 - GAU: 2818
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
	Art Unit	2811
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	Attorney Docket Number	P2317US00

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
	Art Unit	2811
	Examiner Name	To be determined
	Attorney Docket Number	P2317US00

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	1	20040075399		2004-04-22	David HALL	

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	1	1020060037589	KR		2006-05-03	Seoul Semiconductor Co Ltd		☐
	2	2002026378	JP		2002-01-25	Kyocera Corp		☐
	3	1020050066358	KR		2005-06-30	Samsung Electro-Mechanics Co Ltd		☐

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Receipt date: 08/29/2008	Application Number	11993965 11993965 - GAU: 2818
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
	Art Unit	2811
	Examiner Name	To be determined
	Attorney Docket Number	P2317US00

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	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, Thinh T.
	Attorney Docket Number	P2317US00

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6547249		2003-04-15	Collins, et al.	
	2	7474681		2009-01-06	Lin, et al.	
	3	7271421		2007-09-18	Yukimoto, et al.	
	4	7034340		2006-04-25	Yukimoto	
	5	7525248		2009-04-28	Fan	
	6	6635902		2003-10-21	Lin	
	7	7511311		2009-03-31	Kususe, et al.	
	8	7213942		2007-05-08	Jiang, et al.	

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Receipt date: 11/05/2009	Application Number	11993965	11993965 - GAU: 2818
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2007-12-26	
	First Named Inventor	Jong Lam LEE	
	Art Unit	2818	
	Examiner Name	NGUYEN, Thinh T.	
	Attorney Docket Number	P2317US00	

	9	7221044		2007-05-22	Fan, et al.	
	10	7210819		2007-05-01	Jiang, et al.	
	11	6957899		2005-10-25	Jiang, et al.	
	12	6472718		2002-10-29	Lell	

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	1	20060044864		2006-03-02	Lin, et al.	
	2	20050224973		2005-10-13	Bernier, et al.	
	3	20050199885		2005-09-15	Hata, et al.	
	4	20060169993		2006-08-03	Fan, et al.	
	5	20050225973		2005-10-13	Eliashevich, et al.	

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	First Named Inventor	Jong Lam LEE	
	Art Unit	2818	
	Examiner Name	NGUYEN, Thinh T.	
	Attorney Docket Number	P2317US00	

	6	20080230765		2008-09-25	Yoon, et al.	
	7	20060043433		2003-03-02	Matsushita	

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	1	11-150303	JP		1999-06-02	Takeuchi		☐

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	First Named Inventor	Jong-Lam Lee
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	1	6255129		2001-07-03	Lin	

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	1	20040012958		2004-01-22	Hashimoto, et al.	

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	1	1020030052499	KR		2003-06-27	Bae		☐
	2	1020040005098	KR		2004-01-16	Kang		☐

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Art Unit	2818
Examiner Name	NGUYEN, Thinh T.
Attorney Docket Number	P2317US00

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	1	7504772		2009-03-17	Yukimoto et al.	
	2	5940683		1999-08-17	Holm et al.	

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	1	20030010989		2003-01-16	Yukimoto	
	2	20020109147		2002-08-15	Shirai et al.	
	3	20070114542		2007-05-24	Yamazaki et al.	
	4	20050121679		2005-06-09	Nagahama et al.	

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	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, Thinh T.
	Attorney Docket Number	P2317US00

	5	20050082966		2005-04-21	Yamazaki et al.		
	6	20050254243		2005-11-17	Jiang et al.		

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	1	2004-311677	JP		2004-11-04	Matsushita Electric Works Ltd.		☐
	2	2005-142278	JP		2005-06-02	Sharp Corp.		☐
	3	2005-117020	JP		2005-04-28	Stanley Electric Co., Ltd.		☐
	4	2003-017740	JP		2003-01-17	Lumileds Lighting US LLC		☐
	5	2001-185755	JP		2001-07-06	Rohm Co., Ltd.		☐
	6	07-153993	JP		1995-06-16	Daido Steel Co., Ltd.		☐
	7	06-244458	JP		1994-09-02	Nichia Chem Ind Ltd.		☐

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	Application Number	11993965
	Filing Date	2007-12-26
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	Art Unit	2818
	Examiner Name	NGUYEN, Thinh T.
	Attorney Docket Number	P2317US00

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	1	Office Action dated February 1, 2010 for co-pending application no. 12/568,630	☐

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	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, Thinh T.
	Attorney Docket Number	P2317US00

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ See attached certification statement.

☒ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2010-02-24
Name/Print	Hae-Chan Park	Registration Number	50114

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PATENT ABSTRACTS OF JAPAN

(11)Publication number : 06-244458
(43)Date of publication of application : 02.09.1994

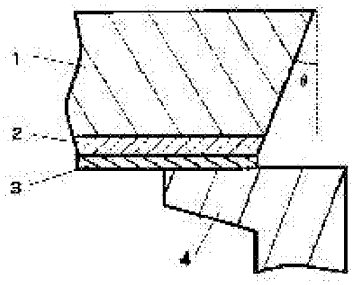
(51)Int.Cl. H01L 33/00

(21)Application number : 05-055074
(22)Date of filing : 19.02.1993

(71)Applicant : NICHIA CHEM IND LTD
(72)Inventor : TANAKA MASANOBU
NAKAMURA SHUJI

(54) BLUE-COLOR-LIGHT EMITTING DIODE

(57)Abstract:
PURPOSE: To improve the light emitting efficiency of a blue-color LED without a reflecting plate such as a cup by effectively utilizing the light emitted from the side surface of a light emitting element utilizing a gallium-nitride-based compound semiconductor, and taking out the light to the side of the observing surface.
CONSTITUTION: A light emitting element comprises at least a light transmitting substrate 1 and a gallium-nitride-based compound semiconductor 2, which is formed on the light transmitting substrate. With the light transmitting substrate 1 of the light emitting element up, the element is mounted on a lead frame 4. The entire light emitting element is sealed with a resin mold 5. In this blue- color-light emitting diode, the side surface of the light emitting element is cut at an acute angle θ downward from the upper surface of the light transmitting substrate.



(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号

特開平6－244458

(43)公開日　平成６年(1994)９月２日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０１Ｌ　33/00	Ａ	7376－4M		
	Ｎ	7376－4M		

審査請求　未請求　請求項の数２　ＦＤ　（全　４　頁）

(21)出願番号　特願平5－55074

(22)出願日　平成５年(1993)２月19日

(71)出願人　000226057
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徳島県阿南市上中町岡491番地100

(72)発明者　田中　政信
徳島県阿南市上中町岡491番地100　日亜化学工業株式会社内

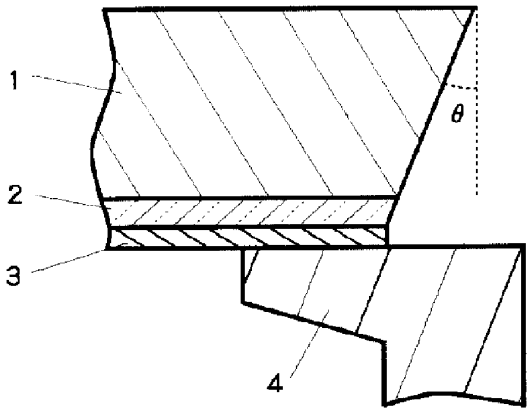
(72)発明者　中村　修二
徳島県阿南市上中町岡491番地100　日亜化学工業株式会社内

(54)【発明の名称】　青色発光ダイオード

(57)【要約】　（修正有）

【目的】　カップ等の反射板を必要とせず、窒化ガリウム系化合物半導体を利用した発光素子の側面から出る光を有効利用して、観測面側に取り出し、青色ＬＥＤの発光効率を向上させる。

【構成】　発光素子が少なくとも透光性基板１と該透光性基板に積層された窒化ガリウム系化合物半導体２とからなり、さらに該発光素子の透光性基板１を上面としてリードフレーム４上に載置し、発光素子全体を樹脂モールド５で封止してなる青色発光ダイオードにおいて、前記発光素子の側面が、透光性基板上面から鉛直方向に向かって、鋭角θで切断されていることを特徴とする。



【特許請求の範囲】
【請求項１】　発光素子が少なくとも透光性基板と該透光性基板に積層された窒化ガリウム系化合物半導体とからなり、さらに該発光素子の透光性基板を上面としてリードフレーム上に載置し、発光素子全体を樹脂モールドで封止してなる青色発光ダイオードにおいて、
前記発光素子の側面が、透光性基板上面の鉛直方向より、鋭角θで切断されていることを特徴とする青色発光ダイオード。
【請求項２】　前記鋭角θは、前記透光性基板の屈折率をｎ1、前記樹脂モールドの屈折率をｎ2とすると、$\theta \geqq \sin^{-1}(n2/n1)$の関係にあることを特徴とする請求項１に記載の青色発光ダイオード。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、透光性基板上に窒化ガリウム系化合物半導体が積層された発光素子を有する青色発光ダイオード（以下、青色ＬＥＤという。）に係り、特に該発光素子の細部の構造に関する。
【０００２】
【従来の技術】一般に、青色ＬＥＤの発光素子の材料として、ＧａＮ、ＩｎＧａＮ、ＧａＡｌＮ、ＩｎＡｌＧａＮ等の窒化ガリウム系化合物半導体が知られている。これら窒化ガリウム系化合物半導体を用いた発光素子を有する従来の青色ＬＥＤの構造を図２に示す。１は透光性基板、２は透光性基板１上に積層された窒化ガリウム系化合物半導体（以下、本明細書においては、１と２とを合わせて発光素子という。）３は窒化ガリウム系化合物半導体２上の適切な位置に設けられた電極、４は発光素子を載置するリードフレーム、５は発光素子全体を封止し、窒化ガリウム系化合物半導体２からの発光を集光する樹脂モールドである。透光性基板１の材料にはサファイア、酸化亜鉛、酸化マグネシウム等の酸化物系単結晶を使用することができ、一般的にはサファイアが用いられている。また樹脂モールド５には、エポキシ樹脂、ユリア樹脂等、耐候性に優れた透明樹脂が用いられる。この図に示すように、従来の青色ＬＥＤはそのほとんどが、発光素子の端面が垂直になるようにチップ状にカットされ、透光性基板１側が上面、即ち発光観測面となるようにしてリードフレームに載置された構造を有している。
【０００３】
【発明が解決しようとする課題】この構造の発光素子において、例えば透光性基板１をサファイアとした場合、サファイア基板１の厚さは通常数百μｍある。これに対し、窒化ガリウム系化合物半導体の厚さはせいぜい数μｍにしか過ぎず、窒化ガリウム系化合物半導体より放射される全青色発光のうち、サファイア基板１の側面に達する光は、全体の約１０～４０％である。しかも、封止樹脂をエポキシ樹脂とした場合、サファイアの屈折率を約３とし、エポキシの屈折率を約１．５とすると、サファイアとエポキシ樹脂との境界での臨界角は約３０°となり、側面に入射する３０°以下の光は、全てサファイア基板の側面から出て行ってしまい、有効利用されていない。
【０００４】ところで、リードフレームの形状をカップ状として、そのカップの底に発光素子を載置して、側面から出ていく光を、カップ側面で上部に反射させる方法もあるが、リードフレームをカップ形状にすると、透光性基板を上にして電極を下にするような構造の窒化ガリウム系化合物半導体発光素子、つまり透光性基板を利用した発光素子では、アッセンブリが生産技術上不可能である。そのため、従来の青色ＬＥＤは、そのほとんどが図２のような構造であり、この構造のＬＥＤはチップ側面より出ていく光を有効利用できず、高い順方向電圧のわりに、発光効率が低く、十分な輝度が得られないという問題があった。
【０００５】したがって本発明はこのような事情を鑑みて成されたものであり、カップ等の反射板を必要とせず、窒化ガリウム系化合物半導体を利用した発光素子の側面から出る光を有効利用して、観測面側に取り出し、青色ＬＥＤの発光効率を向上させることを目的とする。
【０００６】
【課題を解決するための手段】本発明の青色ＬＥＤは、発光素子が少なくとも透光性基板と該透光性基板に積層された窒化ガリウム系化合物半導体とからなり、さらに該発光素子の透光性基板を上面としてリードフレーム上に載置し、発光素子全体を樹脂モールドで封止してなる青色発光ダイオードにおいて、前記発光素子の側面が、透光性基板上面の鉛直方向より、鋭角θで切断されていることを特徴とするものである。
【０００７】鋭角θの角度は特に限定するものではないが、透光性基板の屈折率、樹脂モールドの屈折率によって適宜変更することができる。窒化ガリウム系化合物半導体の発光を全て透光性基板側（発光観測面側）に全反射させるためには、鋭角θは、透光性基板の屈折率をｎ1、前記樹脂モールドの屈折率をｎ2とした場合、$\sin^{-1}(n2/n1)$以上の角度、即ち臨界角以上の角度で切断されていることが好ましい。なお、この式により、全ての青色発光を発光素子側面で全反射させる場合、樹脂モールドの材料の屈折率が基板の屈折率よりも小さいものを選択することはいうまでもない。
【０００８】また、発光素子の側面を斜めにカットするには、例えばダイシングを用いることができ、刃先が所望の角度に調整されているブレードを使用することによって切断可能である。
【０００９】
【作用】図４は、本発明の一実施例に係る青色ＬＥＤにおいて、側面が鋭角θで切断された発光素子の構造を示す図である。また図３は、側面が垂直に切断された従来

の発光素子の構造を示す図である。なおこれらの図は電極、リードフレームを省略して示している。図４に示すように、発光素子の側面を、透光性基板１の上面から、鋭角θで切断することにより、窒化ガリウム系化合物半導体より発する青色発光、特に発光素子側面近傍の青色発光を、透光性基板１で反射させて発光観測面に取り出し、有効利用することが可能となる。一方、前にも説明したように、図３に示す従来の発光素子は、透光性基板１内で全反射したり、発光素子の側面から出て行ってしまう光が圧倒的に多い。なお、この図４はθを臨界角以上としていないため、一部側面から出ていく光もあるが、θを前述の式に基づいて臨界角以上で切断することにより、全て観測面側に反射させることができるのは当然である。

【００１０】このように、発光素子の側面を鋭角に切断することにより、青色発光を多く観測面に反射させることができるため、青色発光ダイオードの発光出力を向上させることができる。また、窒化ガリウム系化合物半導体を有する発光素子は、他のＧａＡｓ、ＧａＰ、ＡｌＩｎＧａＰ等の材料を用いた発光素子と異なり、材料自体にへき開性を有していないため、斜めに切断しやすいという利点を有している。このため、窒化ガリウム系化合物半導体の発光素子の側面を斜めに切断して、その側面で青色発光を反射させることは非常に重要である。

【００１１】

【実施例】予めサファイア基板の上にｎ型ＧａＮとｐ型ＧａＮとを順に積層した２インチφのウエハーを用意し、ｐ型ＧａＮ層の一部をエッチングして、ｎ型ＧａＮ層を一部露出させる。次に、露出させたｎ型ＧａＮ層と、ｐ型ＧａＮとに所定の形状で電極を蒸着した後、サファイア基板に粘着テープを張り付ける。

【００１２】一方、ウエハーを斜めにカットするため、図５に示すように刃先の中心線に向かってそれぞれ両側に３０°の傾斜を設けたブレードを用意してダイシングソーにセットする。次に、前述のウエハーをテーブルに貼付し、ダイシングでｐ型ＧａＮ層側からＸ軸をカットした後、テーブルを９０°回転させ、今度はＹ軸をカットする。

【００１３】最後にウエハーをテーブルから剥し取り、チップ状に分離した後、チップをサファイア基板面が発光観測面になるようにして、リードフレームに取り付け、電極とリードフレームとを電気的に接続した後、エポキシ樹脂でレンズ状にモールドすることにより、本発明の青色ＬＥＤを得る。

【００１４】このようにして得た青色ＬＥＤは、順方向電圧５Ｖで、発光出力２０μＷを示した。一方、側面を垂直にカットしたチップよりなる従来の青色ＬＥＤは発光出力は１０μＷとほぼ半分しかなかった。

【００１５】

【発明の効果】以上説明したように、本発明の青色ＬＥＤはその発光素子の側面を斜めにカットしているために、窒化ガリウム系化合物半導体の発光を、その側面で反射させて透光性基板から有効に取り出すことができる。しかも従来のようにカップ状のリードフレームも必要とせず、生産性にも非常に優れている。

【図面の簡単な説明】

【図１】　本発明の青色ＬＥＤに係る発光素子の側面の構造を一部拡大して示す断面図。

【図２】　従来の青色ＬＥＤの構造を示す断面図。

【図３】　従来の発光素子の構造を示す断面図。

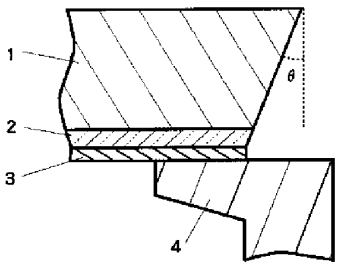
【図４】　本発明の一実施例に係る発光素子の構造を示す断面図。

【図５】　ダイシングソーのブレードの刃先角を示す断面図。

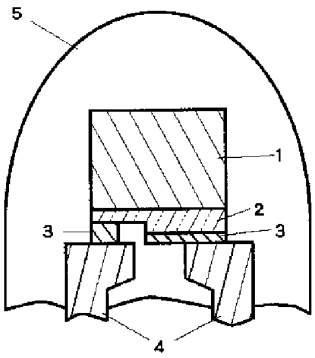
【符号の説明】

１・・・・・・透光性基板
２・・・・・・窒化ガリウム系化合物半導体
３・・・・・・電極
４・・・・・・リードフレーム
５・・・・・・樹脂モールド

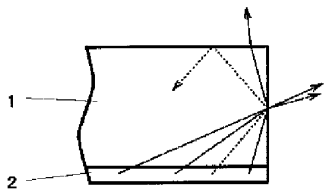
【図１】



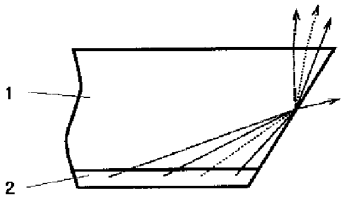
【図２】



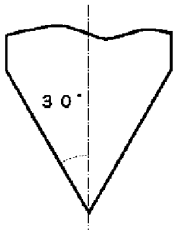
【図３】



【図４】



【図５】



PATENT ABSTRACTS OF JAPAN

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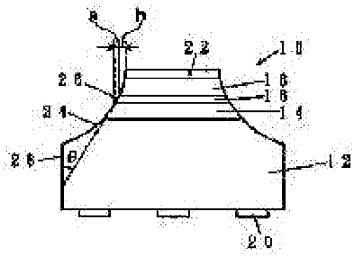
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(54) LIGHT-EMITTING DIODE

(57)Abstract:
PURPOSE: To obtain high light-emitting efficiency by forming an inwardly curved slope spreading from a second clad layer toward a substrate and exposing the periphery of an active layer to the slant face.
CONSTITUTION: A second clad layer 18 is smaller in area than a substrate 12, and a slope 24 including the edge of a first clad layer 14 on the substrate 12 and the upper edge of the second clad layer 18 is inwardly curved. The slope exposes an end face 26 of an active layer 16 and the periphery including the end face 26 forms a prescribed angle θ to an end face 28 of the substrate 12. Thereby, current density becomes high so as to obtain higher light-emitting efficiency.



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特開平7－153993

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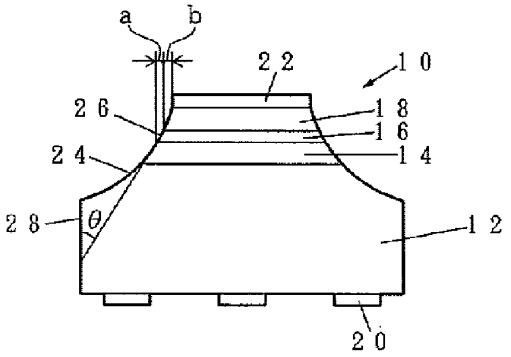
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最終頁に続く

(54)【発明の名称】　発光ダイオード

(57)【要約】
【目的】　高い発光効率が得られる発光ダイオードを提供する。
【構成】　ＬＥＤ（発光ダイオード）１０は、全体が略角柱状を成しているが、基板１２側よりも第２クラッド層１８側の方の面積が小さくされており、基板１２の第１クラッド層１４側の端部と、第２クラッド層１８上面の端部とを結ぶ側面２４は湾曲した斜面とされている。そのため、第１クラッド層１４、活性層１６および第２クラッド層１８は、基板１２側から先細りとなるように積層されて略四角錐台状を成し、活性層１６の端面２６を含む周縁は、基板１２の端面２８に対して所定の角θを成す斜面とされている。



【特許請求の範囲】
【請求項１】　基板上に第１クラッド層、活性層および第２クラッド層が順次積層され、該基板と該第２クラッド層との間に動作電流が通電されることによって該活性層内で発生した光を、該第２クラッド層側から取り出す面発光型発光ダイオードであって、
前記第２クラッド層から前記基板に向かうに従って外周側に向かう斜面が形成され、該斜面に前記活性層の周縁が露出させられていることを特徴とする発光ダイオード。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、発光ダイオードの発光効率を高める技術に関する。
【０００２】
【従来の技術】基板上に第１クラッド層、活性層および第２クラッド層が順次積層され、その基板と第２クラッド層との間に動作電流が通電されることによって上記活性層内で発生した光を、その第２クラッド層側から取り出す面発光型発光ダイオード（以下ＬＥＤという）が知られている。一般に、このような構造のＬＥＤでは、上記活性層内で発生した光が、光取り出し面である第２クラッド層表面に到達するまでに減衰したり反射され、或いは第２クラッド層表面以外の所からも放射されると共に、基板側に向かって放射され、その底面で反射されて側面に向かう光は、その側面への入射角が比較的大きくなるため反射されて内部で吸収されるため、第２クラッド層側から取り出されるのは発生した光の一部のみとなって、高い発光効率が得られない。そこで、発光効率を高めるために、例えばＬＥＤのアッセンブリに際して、開口部側に面する凹面内にＬＥＤを固定し、その端面から放射された光をその凹面で反射させ、第２クラッド層側から取り出される光と同じ方向に取り出すこと等が行われる。
【０００３】
【発明が解決すべき課題】しかしながら、上記のようなアッセンブリによっても発光効率の改善は未だ不充分であった。上記アッセンブリ構造では、ＬＥＤの端面から放射された光が取り出し可能となるのみであり、また、テーパ面での反射効率を十分に高くするには高精度の加工を要して多大なコスト増となるため、反射効率も低いものであったのである。
【０００４】本発明は、以上の事情を背景として為されたものであって、その目的は、高い発光効率が得られる発光ダイオードを提供することにある。
【０００５】
【課題を解決するための手段】斯かる目的を達成するために、本発明の要旨とするところは、基板上に第１クラッド層、活性層および第２クラッド層が順次積層され、その基板と第２クラッド層との間に動作電流が通電されることによって上記活性層内で発生した光を、その第２クラッド層側から取り出す面発光型発光ダイオードであって、前記第２クラッド層から前記基板に向かうに従って外周側に向かう斜面が形成され、該斜面に前記活性層の周縁が露出させられていることにある。
【０００６】
【作用および発明の効果】このようにすれば、第２クラッド層と基板との間に斜面が形成されて、活性層の周縁がその斜面に露出させられると共に、第２クラッド層は基板よりも小さい面積とされるので、その斜面は第２クラッド層側から取り出される光と同じ方向、すなわち光の取り出し方向に向かわせられる。このため、活性層の端面側から放射された光の一部は、直接光の取り出し方向に放射されることになる。また、斜面が光の取り出し方向に向かわせられているため、活性層は第２クラッド層よりも大きな面積を有することになり、第２クラッド層の表面よりも外側に位置する部分で発生して、活性層から第２クラッド層側に向かう光は、第２クラッド層表面に到達する前に取り出される。そのため、この光は、ＬＥＤ内で殆ど減衰或いは反射されることなく取り出される。また、活性層から基板側へ放射され、基板底面で反射されて側面に向かう光は、その側面が斜面とされているため反射光の入射角が小さくなり、その斜面を通って外部に取り出される。したがって、ＬＥＤの側面から放射される光が比較的多く取り出されると共に、発生した光の減衰や反射が減じられ、また、基板側に向かう光も効率良く取り出されて、高い発光効率が得られる。更に、上記のように斜面が形成された結果、活性層が基板よりも小さい面積とされているため、その面積が等しくされている場合に比較して電流密度が高くなり、一層高い発光効率が得られる。
【０００７】
【実施例】図１は、本発明の一実施例であるＬＥＤ（発光ダイオード）１０の構成を示す図である。このＬＥＤ１０は、基板１２上に、例えば有機金属化学気相成長（ＭＯＣＶＤ：Metal Organic Chemical Vapor Deposition ）法や分子線エピタキシー（ＭＢＥ：Molecular Beam Epitaxy）法、或いは気相エピタキシー（ＶＰＥ：Vapor Phase Epitaxy ）法等によって、第１クラッド層１４、活性層１６および第２クラッド層１８が順次結晶成長させられた後、基板１２の下面および第２クラッド層１８の上面に、下部電極２０および上部電極２２がそれぞれ蒸着されて構成されている。
【０００８】上記基板１２は例えば３５０μｍ程度の厚さのｎ－$Al_{0.4}Ga_{0.6}As$単結晶から成る化合物半導体、第１クラッド層１４は例えば４μｍ程度の厚さを備えた、上記基板と同じｎ－$Al_{0.4}Ga_{0.6}As$単結晶から成る化合物半導体、活性層１６は例えば１μｍ程度の厚さのｐ－ＧａＡｓ単結晶から成る化合物半導体、第２クラッド層１８は例えば４μｍ程度の厚さのｐ－Ａ

$l_{0.4}$ $Ga_{0.6}$ Ａｓ単結晶から成る化合物半導体である。また、下部電極２０は、基板１２側から順にＡｕ－Ｇｅ合金、ＮｉおよびＡｕが積層形成されており、上部電極２２は第２クラッド層１８側にＡｕ－Ｚｎ合金が、その上にＡｕが積層形成されている。これらの下部電極２０および上部電極２２はそれぞれオーミック電極である。

【０００９】上記ＬＥＤ１０は、全体が略角柱状を成しているが、基板１２側よりも第２クラッド層１８側の方の面積が小さくされており、基板１２の第１クラッド層１４側の端部と、第２クラッド層１８上面の端部とを結ぶ側面２４は、図に示すように湾曲した斜面とされている。すなわち、第２クラッド層１８から基盤１２に向かうに従って外周側に向かう斜面が形成されている。そのため、第１クラッド層１４、活性層１６および第２クラッド層１８は、基板１２側から先細りとなるように積層されて略四角錐台状を成し、活性層１６の端面２６を含む周縁は、基板１２の端面２８に対して所定の角θ（例えば６０°程度）を成す斜面とされている。なお、図において基板１２、各層１４，１６，１８および電極２０，２２等の大きさは、必ずしも正確な比率で示されていない。

【００１０】以上のように構成されたＬＥＤ１０は、下部電極２０と上部電極２２とに動作電圧が印加され、第１クラッド層１４および第２クラッド層１８間に動作電流が通電されることによって、活性層１６内で光が発生し、第２クラッド層１８の上面側からその光が取り出される。

【００１１】ここで、本実施例においては、ＬＥＤ１０の上記側面２４が斜面を成しているため、活性層１６の端部は、その厚さに $\tan\theta$ を乗じた大きさ（幅ａ）で、光取り出し方向である図の上方向に向けられている。そのため、活性層１６の端面２６から放射された光の一部は、直接光の取り出し方向に放射されることになる。また、第２クラッド層１８の上面の面積は、活性層１６の上面の面積よりも小さくされており、図の幅ｂ内で発生した光は第２クラッド層１８の上面に達する以前に第２クラッド層１８の端面から取り出されることになる。このため、この光はＬＥＤ１０内で殆ど減衰或いは反射されることなく取り出される。また、活性層１６から基板１２側へ放射され、基板１２底面で反射されて側面２４に向かう光は、その側面２４が斜面とされているため入射角が小さくなり、従来入射角が大き過ぎるために反射されて内部で吸収されていた光が、その斜面を通って外部に取り出される。したがって、側面２４から放射される光が比較的多く取り出されると共に、発生した光の減衰や反射が減じられ、また、基板１２側に向かう光も効率良く取り出されて、高い発光効率が得られる。更に、活性層１６が基板１２よりも小さい面積とされているため、その面積が等しくされている場合に比較して電流密度が高くなり、一層高い発光効率が得られる。

【００１２】上記ＬＥＤ１０は、例えば図２の（ａ）～（ｈ）の工程に従って製造される。（ａ）の工程において、多数のＬＥＤ１０を製造するための基板１２上に第１クラッド層１４、活性層１６および第２クラッド層１８を順次結晶成長させて、エピタキシャル層３０を作製する。なお、図２においては、エピタキシャル層３０の各層の境界を省略している。次いで（ｂ）の工程において、エピタキシャル層３０上にフォトリソグラフィによって所定のパターンの上部電極２２を形成し、（ｃ）の工程において、その上にフォトレジスト膜３２を形成して、フォトリソグラフィによって、ＬＥＤ１０となる個々の素子３４毎にパターニングを行う。このとき、（ｃ）に示されるように、上部電極２２はフォトレジスト膜３２に覆われた状態にされている。次いで（ｄ）の工程において、例えば燐酸および過酸化水素水を混合したエッチング液によって、エピタキシャル層３０の上面側からエッチングを行う。このエッチング液はフォトレジスト膜３２を溶解せず、エピタキシャル層３０および基板１２のみを溶解するものが好適に用いられる。このとき、エピタキシャル層３０の各層および基板１２の溶解性が略等しいため、その表面上の点Ｐを中心とした略円弧上の凹部３６が形成されるように溶解され、エッチング液の組成、濃度、処理温度および処理時間を適宜設定することにより、エピタキシャル層３０の上面が上部電極２２よりもやや小さくされる。次いで、（ｅ）の工程において、フォトレジスト膜３２を除去し、（ｆ）の工程において、個々の素子３４毎にダイシングによって分離する。このとき、前記のエッチング処理によってエピタキシャル層３０の上面からはみ出した上部電極２２の周縁部が水流或いは超音波によって除去される。次いで（ｇ）の工程において下部電極２０を形成して、図１に示されるＬＥＤ１０が製造される。このＬＥＤ１０は、（ｈ）の工程において、テーパ状の内壁面３８を備えたケース４０の底面に、下部電極２０が図示しないリードに導通がとられるように固定されると共に、上部電極２２にリード４２がボンディングされ、図示しない工程において樹脂モールド内に封入して用いられる。

【００１３】上記の製造工程においては、上記凹部３６がダイシングの切り代の幅よりも極めて大きくされていると共に、凹部３６は基板１２の上部の一部までの範囲で形成されているため、（ｆ）の工程で素子３４がダイシングによって分離されると、基板１２の下部の端面はその底面と直角になるが、エピタキシャル層３０および基板１２の一部の端面はやや湾曲した斜面を成す。したがって、エピタキシャル層３０および基板１２の一部が略四角錐台状とされた、すなわち、図１に示した、基板１２と第２クラッド層１８の上面とを結ぶ側面２４が斜面とされたＬＥＤ１０が容易に得られるのである。

【００１４】なお、本実施例では、凹部３６が形成され

た後にダイシングが行われるため、ダイシングの際に活性層１６にカッタが触れない。したがって、活性層１６等にダイシングに起因する欠けが発生せず、電流のリークが発生し難い利点がある。また、テーパ状の内壁面３８を備えたケース４０内にＬＥＤ１０が固定されているため、活性層１６の側面から第２クラッド層１８の表面と平行な方向に放射される光も、その内壁面３８によって反射されて光の取り出し方向に向かわされ、一層高い発光効率が得られる。

【００１５】図3は、前述の製造工程の（ｄ）の工程において、エッチング時間を変えた場合の光出力すなわち発光効率を表したグラフである。前述の工程においては、例えば４０乃至５０分間処理することによって、エッチング処理をしないＬＥＤに比較して約１．８倍程度の高い光出力のＬＥＤ１０が得られている。なお、最適なエッチング時間は、エッチング液の種類や濃度および処理時間や処理温度等の条件によって変動するが、短か過ぎる場合にはエピタキシャル層３０の面積が十分に小さくならないため電流密度が上がらず、また、側面の傾斜部が形成されないために、高い光出力が得られない。また、必要以上に長時間のエッチング処理をしても、電流密度は高くなるものの活性層１６すなわち発光面積が小さくなるため、ある一定値以上の光出力は得られないのである。

【００１６】図4は、上記ＬＥＤ１０において、動作電流を５０ｍＡとしたときの電流密度と光出力の関係を表したグラフである。このグラフにおいては、従来用いられていた電流密度５４ｍＡ／ｃｍ^2 程度のＬＥＤの光出力を１として、相対的な光出力を示している。図より明らかなように電流密度が高くなると相対光出力が高くなる。本実施例のＬＥＤ１０においては、前述のような構成とされた結果、電流密度が約１２８ｍＡ／ｃｍ^2 程度と高くなり、上述のように従来の１．８倍程度の高い光出力が得られるのである。なお、本図は、前述の構造のＬＥＤ１０による測定結果であるため、前述のように側面２４が斜面とされたことによる効果が含まれた光出力であり、必ずしも電流密度と相対光出力との厳密な関係を表すものではない。

【００１７】図5は、他の製造方法によったＬＥＤ４４の例である。本実施例においては、基板１２と第２クラッド層１８の上面とを結ぶ側面４６は、湾曲しない真直な斜面とされている。このような構造としても、前述の実施例と同様に、活性層１６の端面２６が斜面とされてその端面２６から放出される光が光の取り出し方向に向かわされ、また、側面４６が斜面とされて活性層１６の端部側で発生した光の減衰や反射が低減させられ、また、基板１２側へ放射されてその底面で反射された光が斜面から取り出され、更に、活性層１６が基板１２よりも小さい面積とされて電流密度が高くされているため、高い発光効率が得られるのである。更に、本実施例においては、側面４６が湾曲していないため、第２クラッド層１８上面と基板１２底面との面積比を等しくした場合には、前述のＬＥＤ１０よりも幅ａが大きくなり、一層高い発光効率が得られる。このＬＥＤ４４は、例えば、前述の図２の工程において、このようなプロファイルが得られるエッチング液を使用するか、或いはエッチング処理に代えて幅広且つ先端がテーパ状とされたダイヤモンドカッタ等で溝切り加工をし、その後図２（ｆ）の工程と同様にダイシングを行うことによって得られる。

【００１８】なお、前述のＬＥＤ１０およびＬＥＤ４４においては、第２クラッド層１８上に直接上部電極２２を形成したが、例えば、図6に示すように、第２クラッド層１８の上に第２クラッド層１８とは導電型が異なる電流ブロック層４８を設け、その上に上部電極２２を形成して、ＬＥＤ５０のような構造としても良い。前述の実施例においては、上部電極２２は例えば図７に示されるように形成されており、リード４２がボンディングされる部分すなわち上部電極２２の中央部５２は、通電されて光が発生しても上部電極２２に遮蔽されてその光が取り出し得ない。これに対して、ＬＥＤ５０では、中央部５２は電流ブロック層４８が存在するために通電され得ず、発光させられない。すなわち、上部電極２２に遮蔽されないで光が取り出される部分のみが発光させられるため、発生した光の取り出し効率が一層高くなり、高い光出力が得られる。なお、上記電流ブロック層４８は、例えばフォトリソグラフィ等によって任意の形状に形成されるものである。

【００１９】以上、本発明の一実施例を図面を参照して詳細に説明したが、本発明は更に別の態様でも実施される。

【００２０】例えば、前述の実施例においては、ＧａＡｓ／Ａｌ$_x$ＧａＡｓダブルヘテロ構造の面発光型ＬＥＤ１０等について説明したが、そのＡｌとＧａとの組成比は適宜設定されると共に、ＧａＰ，ＩｎＰ，ＩｎＧａＡｓＰ等から成るダブルヘテロ構造のＬＥＤや、単なるｐｎ接合から成るＬＥＤにも本発明は同様に適用され得る。また、基板１２には、例えばＧａＡｓ等の他の半導体が用いられても良い。

【００２１】また、前述の実施例においては、基板１２側にｎ型半導体が、第２クラッド層１８側にｐ型半導体が用いられ、上部電極２２から下部電極２０に向かって動作電流が流れるようにされていたが、ｐ型，ｎ型を反対にして動作電流の流れる方向を反対にしても良い。

【００２２】例えば、前述の実施例においては、活性層１６の端面２６の傾斜の角度θは６０°程度とされていたが、この角度θは、１０～８０°の範囲の値を取り得るものである。

【００２３】また、前述の実施例において第１クラッド層１４が比較的厚く（例えば５０μｍ程度）されている場合は、第１クラッド層１４までが傾斜させられていて

も良い。

【００２４】また、前述の実施例においては、ＬＥＤ１０，４４，５０は全体が略角柱状に形成され、エピタキシャル層３０（すなわち第１クラッド層１４乃至第２クラッド層１８）および基板１２の一部は四角錐台状に形成されていたが、ＬＥＤ１０等の全体の形状は例えば多角柱状とされていても良く、エピタキシャル層３０および基板１２の一部は、三角錐台を含む多角錐台状或いは円錐台状とされていても良い。本発明においては、活性層１６が基板１２よりも小さい面積とされ、その端面２６を含む周縁が斜面に露出させられていれば、その効果が得られるのである。なお、ＬＥＤ１０等の形状は、例えば、図２の工程において上部電極２２およびフォトレジスト膜３２を多角形或いは円形等に形成してエッチング処理を行うことで容易に変更できる。

【００２５】その他、一々例示はしないが、本発明はその主旨を逸脱しない範囲で種々変更を加え得るものである。

【図面の簡単な説明】

【図１】本発明の一実施例である発光ダイオードの構成を示す図であり、図２の製造方法によって得られたものである。

【図２】本発明の一実施例である発光ダイオードの製造方法を示す図である。

【図３】図２の工程におけるエッチングの時間と光出力との関係を示すグラフである。

【図４】図２の工程において得られた発光ダイオードの電流密度と光出力との関係を示すグラフである。

【図５】本発明の他の実施例を示す図である。

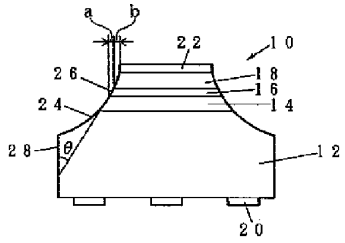
【図６】本発明の更に他の実施例を示す図である。

【図７】図１の発光ダイオードの電極の構成を示す図である。

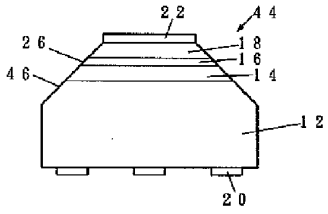
【符号の説明】

１０：ＬＥＤ（発光ダイオード）
１２：基板
１４：第１クラッド層
１６：活性層
１８：第２クラッド層
２２：上部電極
２４：側面
２６：活性層の端面（周縁）

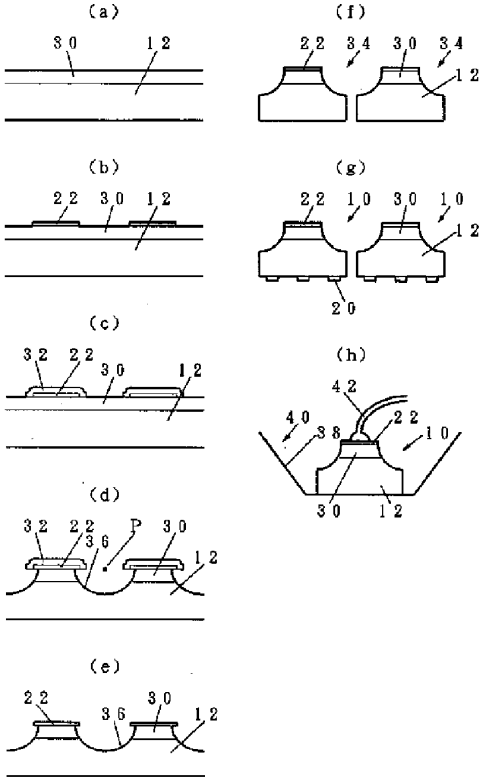
【図１】



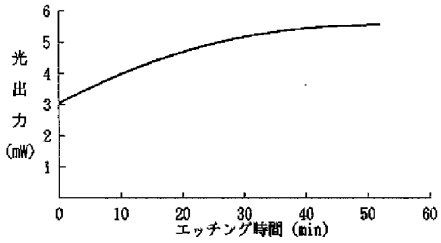
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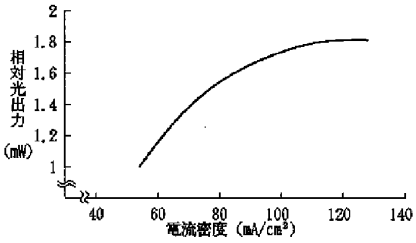
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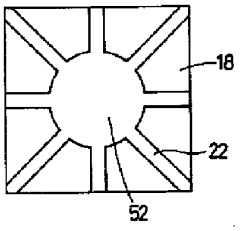
【図３】



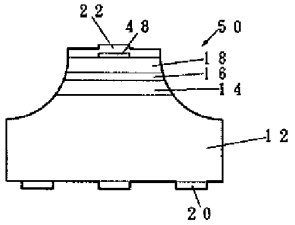
【図４】



【図７】



【図６】



フロントページの続き

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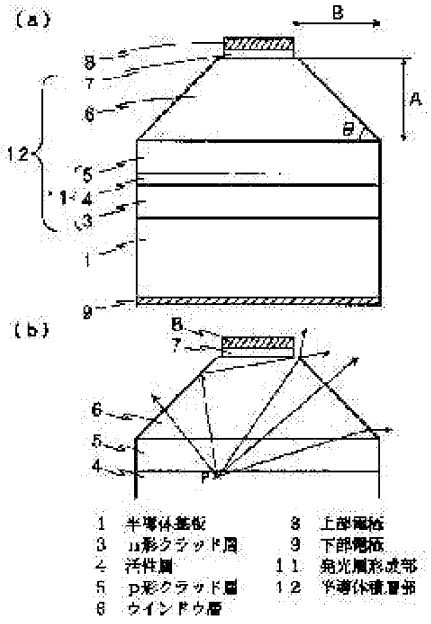
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(54) SEMICONDUCTOR LIGHT EMITTING ELEMENT

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a semiconductor light emitting element which has a structure permitting lights emitted from a light emitting layer to be taken out possibly much outside a chip to improve the outside differential quantum efficiency.
SOLUTION: A semiconductor laminate 12 having a light emitting layer forming part 11 having an active layer 4 sandwiched between at least an n-type layer 3 and a p-type layer 5 is provided on a semiconductor substrate 1, an upper (p-side) electrode 8 is provided on the front surface of the semiconductor laminate 12, a lower (n-side) electrode 9 is provided on the back surface of the semiconductor substrate 1, and a slope narrower at the upper electrode 8 and broader at the active layer 4 is formed on the side of an upper layer of the semiconductor laminate 12 than its active layer 4.



(19)日本国特許庁（ＪＰ）　(12) **公開特許公報**（Ａ）　(11)特許出願公開番号
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(21)出願番号　特願平11－367726

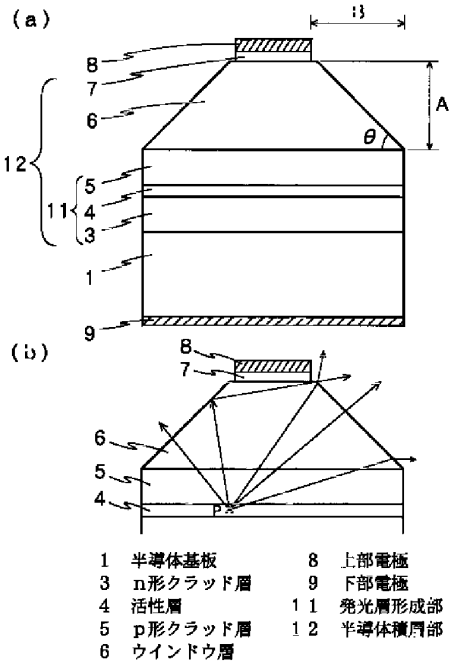
(22)出願日　平成11年12月24日(1999.12.24)

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Ｆターム(参考)　5F041 AA03 AA07 CA35 CA36 CA93 FF11

(54)【発明の名称】　半導体発光素子

(57)【要約】
【課題】　発光層で発光した光をチップの外側にできるだけ取り出せる構造とし、外部微分量子効率を向上させることができる半導体発光素子を提供する。
【解決手段】　半導体基板１の上に、少なくともｎ形層３およびｐ形層５により活性層４を挟持する発光層形成部１１を有する半導体積層部１２が設けられている。また、半導体積層部１２の表面側に上部電極（ｐ側電極）８が設けられ、半導体基板１の裏面側に下部電極（ｎ側電極）９が設けられている。そして、半導体積層部１２の活性層４より上層部に上部電極８側の幅が狭く、活性層４側で幅が広くなるように側面に傾斜面が形成されている。



1　半導体基板　　8　上部電極
3　n形クラッド層　　9　下部電極
4　活性層　　11　発光層形成部
5　p形クラッド層　　12　半導体積層部
6　ウインドウ層

【特許請求の範囲】
【請求項１】　半導体基板と、該半導体基板の上に設けられ、少なくともｎ形層およびｐ形層により活性層を挟持する発光層形成部を有する半導体積層部と、該半導体積層部の表面側に設けられる上部電極と、前記半導体基板の裏面側に設けられる下部電極とからなり、前記半導体積層部の前記活性層より上層部に前記上部電極側の幅が狭く、前記活性層側で幅が広くなるように側面に傾斜面が形成されてなる半導体発光素子。
【請求項２】　前記傾斜面が、外側が凸面となる傾斜面である請求項１記載の半導体発光素子。
【請求項３】　前記半導体積層部の表面側が、ＡｌＧａＡｓ系化合物半導体層からなり、表面側ほどＡｌの混晶比が小さくなるように組成が変化する層である請求項１または２記載の半導体発光素子。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、半導体層が積層されて発光層を形成する発光層形成部の表面側に光を取り出す構造の半導体発光素子に関する。さらに詳しくは、側面方向に光を取り出しやすくし、全体として発光する光の外部への取出し効率（外部微分量子効率）を向上させ得る構造の半導体発光素子に関する。
【０００２】
【従来の技術】従来の可視光半導体発光素子は、たとえば図５に示されるような構造になっている。すなわち、図５において、ｎ形ＧａＡｓからなる半導体基板２１上に、たとえばｎ形のＩｎＧａＡｌＰ系の半導体材料からなるｎ形クラッド層２２、クラッド層よりバンドギャップエネルギーが小さくなる組成のＩｎＧａＡｌＰ系の半導体材料からなる活性層２３、ｎ形クラッド層と同じ組成でｐ形のＩｎＧａＡｌＰ系の半導体材料からなるｐ形クラッド層２４がそれぞれエピタキシャル成長され、ダブルヘテロ構造の発光層形成部２９が形成されている。さらにその表面にＡｌＧａＡｓ系化合物半導体からなるｐ形のウインドウ層（電流拡散層）２５が設けられている。そして、その表面の中央部にＧａＡｓからなるコンタクト層２６を介して上部（ｐ側）電極２７および半導体基板の裏面に下部（ｎ側）電極２８が形成されている。
【０００３】この構造の半導体発光素子で、たとえば活性層２３のＰ点で発光した光は、四方に放射（半導体基板側にも進むが、半導体基板２１のＧａＡｓは光を吸収して表面側に取り出すことが困難であるため図示してない）され、電極以外の表面およびウインドウ層２５の側面から外部に取り出される。しかし、半導体層の屈折率は３．５程度であり、空気の屈折率は１、ランプ型にする場合など周囲を透明樹脂で被覆する場合でも、樹脂の屈折率は１．５程度であり、界面での入射角が小さくないと図５に示されるように、全反射をしてＬＥＤチップの内部を全反射しながら吸収などにより減衰してしまう。
【０００４】
【発明が解決しようとする課題】前述のように、半導体層とその外周の空気または透明樹脂などとの屈折率の差により、発光層で発光した光がチップの上面または側面で全反射する割合が高い。一方、クラッド層や活性層などは完全な透明体ではなく、発光層で発光した光を吸収し、また、半導体基板やコンタクト層などに用いられるＧａＡｓは、発光層で発光する光を吸収する材料であるため、全反射を繰り返すうちに吸収されて減衰する。そのため、外部に取り出すことができる光の割合が小さくなり、外部微分量子効率が向上しないという問題がある。
【０００５】本発明は、このような問題を解決するためになされたもので、発光層で発光した光をチップの外側にできるだけ取り出せる構造とし、外部微分量子効率を向上させることができる半導体発光素子を提供することを目的とする。
【０００６】
【課題を解決するための手段】本発明者らは、発光した光を外に有効に取り出すことができない原因を鋭意検討を重ねて調べた結果、発光層（活性層）で発光する光は四方に均一に放射されるが、とくに電流が集中して流れ電流密度が大きいチップの中心部で発光する光は、真上に行く光が上部電極で遮られ、コンタクト層で吸収されたり、反射しても再度半導体基板側に反射して吸収されてしまい、斜め方向に進む光は、上面または側面に大きな入射角で入射して全反射し、有効に取り出せないことに原因があることを見出した。そして、上面から側面にかけての界面（チップの外壁）を傾斜面とすることにより、斜め方向に進んできた光に対して入射角を小さくし、全反射させないで外に取り出すことができることを見出した。
【０００７】本発明による半導体発光素子は、半導体基板と、該半導体基板の上に設けられ、少なくともｎ形層およびｐ形層により活性層を挟持する発光層形成部を有する半導体積層部と、該半導体積層部の表面側に設けられる上部電極と、前記半導体基板の裏面側に設けられる下部電極とからなり、前記半導体積層部の前記活性層より上層部に前記上部電極側の幅が狭く、前記活性層側で幅が広くなるように側面に傾斜面が形成されている。
【０００８】この構造にすることにより、半導体積層部の上部電極が設けられた部分以外の上表面および側面が傾斜面となるため、斜めに表面側に向かってきた光も全反射することなく外側に出やすい。また、ウインドウ層（半導体積層部の上層部）の側面側に向かった光も、側面が内側に傾斜しているため、チップの外部との境界面では、その入射角が小さくなり、全反射しないで外部にでやすくなる。その結果、外部への光の取り出し効率が

向上し、外部微分量子効率を向上させることができる。

【0009】前記傾斜面が、外側が凸面となる傾斜面であれば、より一層チップ内部での入射角が小さくなり、外側へ光を取り出しやすくなる。

【0010】前記半導体積層部の表面側が、AlGaAs系化合物半導体層からなり、表面側ほどAlの混晶比が小さくなるように組成が変化する層であれば、Gaをエッチングしやすいエッチャントを用いることにより、Alの混晶比の小さい上層部はエッチングされやすく、Alの混晶比の大きい下層はエッチングされにくいため、容易に傾斜面を作りやすい。この場合、Alの組成比の変化を直線的に変化させることもできるが、上部を凸とする放物線状に変化させれば、エッチングのみで外側が凸面となる傾斜面とすることができる。

【0011】

【発明の実施の形態】つぎに、本発明による半導体発光素子について、図面を参照しながら説明をする。本発明による半導体発光素子は、図1にその一実施形態の断面説明図が示されるように、半導体基板1の上に、少なくともn形層3およびp形層5により活性層4を挟持する発光層形成部11を有する半導体積層部12が設けられている。また、半導体積層部12の表面側に上部電極（p側電極）8が設けられ、半導体基板1の裏面側に下部電極（n側電極）9が設けられている。そして、半導体積層部12の活性層4より上層部に上部電極8側の幅が狭く、活性層4側で幅が広くなるように側面に傾斜面が形成されていることに特徴がある。

【0012】発光層形成部11は、たとえば$In_{0.49}(Ga_{1-x}Al_x)_{0.51}P$（$0.6 \leqq x \leqq 0.8$、たとえばx＝0.67）からなるn形クラッド層3が0.1～2μm程度、たとえば587nm程度の発光波長とする$In_{0.49}(Ga_{1-y}Al_y)_{0.51}P$（$0.2 \leqq y \leqq 0.3$、たとえばy＝0.26）からなる活性層4が0.1～2μm程度、$In_{0.49}(Ga_{1-x}Al_x)_{0.51}P$（$0.6 \leqq x \leqq 0.8$、たとえばx＝0.67）からなるp形クラッド層5が0.1～2μm程度それぞれ成長されて形成されている。なお、発光層形成部を構成する半導体層は、InGaAlP系化合物半導体に限らず、AlGaAs系化合物半導体など、他の発光色の半導体層を用いることができる。

【0013】この発光層形成部11の表面に、$Al_zGa_{1-z}As$（$0.5 \leqq z \leqq 0.8$）からなるウインドウ層6が1～10μm程度設けられている。また、ウインドウ層6の表面には、上部電極8の下側のみにGaAsなどからなるコンタクト層7が設けられ、これらにより半導体積層部12が形成されている。

【0014】本発明の半導体発光素子においては、この半導体積層部12の活性層4より上層、たとえばウインドウ層6の側面が、半導体基板1の面に対して垂直方向ではなく、上部電極8側で幅が狭く、活性層4側で幅が広くなるように傾斜面に形成されている。図1に示される例では、たとえばピラミッド形状の4角錐の上部が上部電極8部分で底面に平行に切り取られた形状になっており、たとえばウインドウ層6の厚さAが6μm程度で、上部電極8からチップ側面までの距離Bが約50μm程度（チップの一辺が200μm程度で、上部電極8の一辺が100μm程度）であり、傾斜角θは、約7°程度になる。しかし、ウインドウ層をもっと厚くすれば傾斜角も大きくすることができ、60°以下程度であれば、外部への光の取り出し効率を向上することができた。

【0015】このような傾斜面を形成するには、たとえば半導体積層部12を形成し、その上に上部電極8を形成してコンタクト層7をパターニングした後に、ウェハの状態で、図2に示されるように、チップの境界部に開口部16aを形成したホトレジスト膜16を設け、その開口部16aから露出するウインドウ層6を、たとえば昭和電工（株）商品名ショウポリッシュによりエッチングすることにより、表面側がオーバーエッチングされて図2に示されるように凹部17が形成される。この凹部17の中心部でダイシングすることにより、チップの側面に傾斜面が形成されたLEDチップが得られる。この傾斜面の形成法としては、このようなエッチングによらなくても、機械的研磨などの方法によっても形成することができる。

【0016】また、エッチングにより形成するにしても、とくに前述のエッチャントは、Gaをよくエッチングするため、ウインドウ層として、前述の$Al_zGa_{1-z}As$を使用し、Alの組成を表面側にいくにしたがって減らすことにより、表面側ほどよくエッチングされ、傾斜面を形成しやすい。このウインドウ層6のAlの組成を順次減らすには、図3（a）に示されるように、ウインドウ層の下面から上面に直線状にまたは階段状（図示せず）に減らすこともできるし、図3（b）に示されるように、放物線状に減らすこともできる。この組成を変化させるには、後述するMOCVD法により行う場合、導入ガスの流量を変化させることにより、容易に変化させることができる。

【0017】このような放物線状にAlの組成を減らすことにより、エッチングスピードが放物線状に変化し、図4にウインドウ層6部の断面説明図が示されるように、側面の傾斜面が外側に凸の形状となる。このような外側に凸の形状になるように傾斜面を形成すると、活性層4で発光して斜め上方に向かう光はチップの境界面では凹面をなす界面に入射するため、より一層入射角が小さくなり、全反射することなく光が透過しやすくなる。その結果、より一層光の取り出し効率が向上して好ましい。

【0018】上部（p側）電極8は、たとえばAu-Be／Ni／Ti／Auなどを全面に設けた後にパターニ

ングすることにより形成されてもよいし、電極が設けられる部分以外にマスクを設けて、全面に電極材料を被膜してからマスクを除去するリフトオフ法により形成されてもよい。また、GaAsからなる半導体基板1の裏面には、全面にAu-Ge／Ni／Auなどが0.2～0.4μm程度の厚さに設けられ、n側電極9が形成されている。

【0019】本発明の半導体発光素子によれば、ウインドウ層の上面および側面が繋がった傾斜面になっているため、たとえば図1（b）に一部の発光経路が示されるように、活性層4の発光部Pで発光し、斜め方向に進んだ光は、上面や側面に大きな入射角で入射しないで、傾斜面に直接小さな入射角で入射する。すなわち、半導体層の屈折率は、3.3～3.7程度で、その外部に透明なエポキシ樹脂が設けらる場合、その屈折率は1.5～1.55程度であり、臨界角は30°程度になる。すなわち、入射角が30°程度以下であれば全反射することなくウインドウ層の界面から光が外に取り出されるが、それより大きな入射角で入射すると全反射をする。しかし、本発明によれば、斜め方向に向かう光に対して、傾斜面が対向するため、入射角が小さくなり、光が外に出やすくなる。

【0020】さらに、本発明では、上部電極を挟んで両外側に傾斜面が形成されているため、傾斜面が互いに近づくか遠ざかる方向で対向し、平行に向き合わない構造になる。そのため、たとえ全反射をしても対向する傾斜面では光が出やすくなる。その結果、チップ内部で何回も全反射を繰り返して中で減衰しないで、効率よく外に取り出すことができる。

【0021】また、前述のように傾斜面が外側に凸になるように形成されることにより、より一層傾斜面に対する入射角が小さくなり、光の取り出し効率が向上する。このような傾斜面を簡単に形成するのに、たとえばAlGaAs系化合物半導体のAl組成など、その組成を変化させることにより、選択的にエッチングをすることができ、組成の変化に応じた形状の傾斜面を形成することができる。また、前述のAlGaAs系化合物半導体のAl比率を表面側で少なくすることにより、腐食しやすいAlの露出が少なくなり、保護層の機能も果たし、より一層効果が大きい。とくに放物線状にAlの比率が小さくなることにより、Alの比率が小さくなると発光する光を吸収しやすくなるが、その層が非常に薄いため、吸収の影響も殆どなくなる。

【0022】この半導体発光素子を製造するには、たとえばn形GaAs基板1をMOCVD（有機金属化学気相成長）装置内に入れ、反応ガスのトリエチルガリウム（TEG）またはトリメチルガリウム（TMG）、アルシン（AsH_3）、トリメチルアルミニウム（TMA）、トリメチルインジウム（TMIn）、n形ドーパントとしてのH_2Se、p形層形成の場合はp形ドーパントとしてのジメチル亜鉛（DMZn）の必要なガスをそれぞれ導入し、図1（a）に示されるように、$In_{0.49}(Ga_{0.3}Al_{0.7})_{0.51}P$からなるn形クラッド層3を0.1～2μm程度、ノンドープの$In_{0.49}(Ga_{0.75}Al_{0.25})_{0.51}P$からなる活性層4を0.1～2μm程度、$In_{0.49}(Ga_{0.3}Al_{0.7})_{0.51}P$からなるp形クラッド層5を0.1～2μm程度、たとえば$Al_{0.7}Ga_{0.3}As$からなるp形ウインドウ層6を1～10μm程度、GaAsからなるコンタクト層7を0.2～1μm程度それぞれ連続的に成長する。

【0023】その後、Au-Be／Ni／Ti／Auなどをリフトオフ法、マスク蒸着、または全面に成膜した後にホトリソグラフィ法によるパターニングにより、上部（p側）電極8を形成し、さらに半導体基板1の裏面にAu-Ge／Ni／Auなどを全面に設けて下部（n側）電極9を形成する。その後、半導体積層部12の表面に上部電極8部を覆ってレジスト膜を設け、チップ境界面に開口部を設ける。この開口部の大きさは、たとえば前述のウインドウ層6の厚さAが6μm程度で、横の長さが50μm程度、ウインドウ層6の$Al_zGa_{1-z}As$のzを下面から上面まで、たとえば0.7から0.5程度に変化させる場合、幅が30μm程度の開口部を設けると良好な傾斜面が得られる。その後、エッチングによる凹部の底面でチップ化することにより図1（a）に示されるLEDチップが得られる。

【0024】

【発明の効果】本発明の半導体発光素子によれば、発光部から斜め方向に進む光に対して、チップの壁面（半導体積層部上層のたとえばウインドウ層の壁面）が傾斜面により対向しているため、斜め方向に進んできた光をそのまま外に取り出すことができ、結果的に非常に外部微分量子効率が向上する。しかも、斜め方向に進んできた光を殆どそのまま透過させるため、チップから外に出た光も四方に進みやすく、横方向の輝度が向上し、広い面積を照射する用途に適し、たとえば液晶表示装置のバックライトのように面全体を照射する光源に適する。その結果、明るい液晶表示装置用のバックライトが得られる。

【図面の簡単な説明】

【図1】本発明の一実施形態であるLEDチップの断面説明図である。

【図2】図1のLEDチップの傾斜面を形成する工程の断面説明図である。

【図3】図1のLEDチップの傾斜面を作るのに適したウインドウ層の組成の変化の例を示す図である。

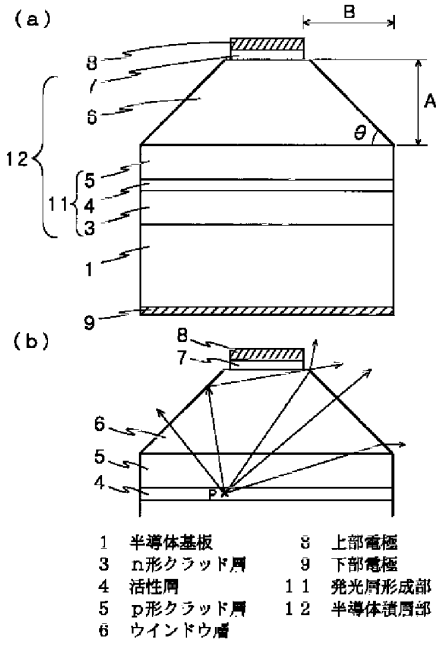
【図4】本発明による半導体発光素子における傾斜面の他の構造例を示す図である。

【図5】従来のLEDチップの構造例を示す断面説明図である。

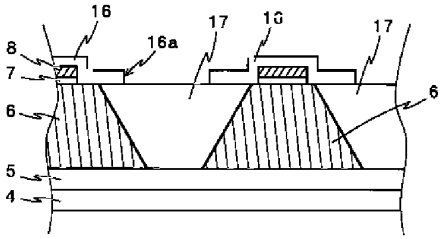
【符号の説明】

1　半導体基板
3　n形クラッド層
4　活性層
5　p形クラッド層
6　ウインドウ層
8　上部電極
9　下部電極
11　発光層形成部
12　半導体積層部

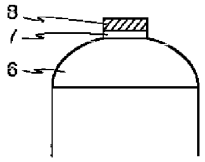
【図1】



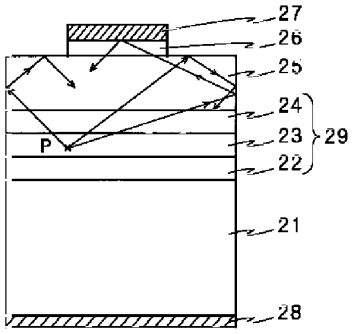
【図2】



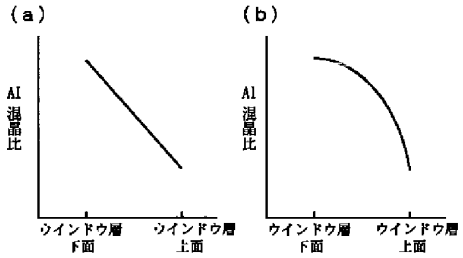
【図4】



【図5】



【図3】



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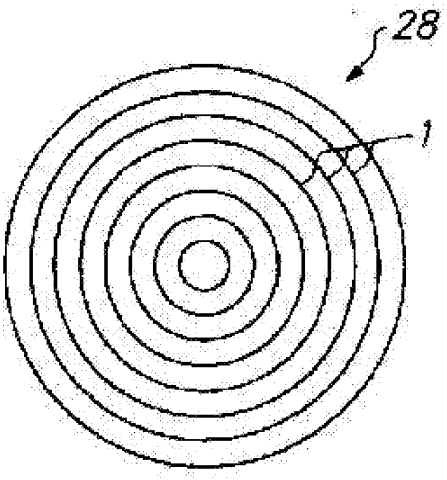
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(54) FORMATION OF OPTICAL ELEMENT OF LIGHT EMITTING DEVICE FOR IMPROVING LIGHT EMITTING RATE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a light emitting device containing either one or both of a Fresnel lens and a holographic diffuser formed on the surface of a semiconductor light emitting element for improving the light emitting rate of the element, and to provide a method of forming the device.
SOLUTION: An optical element formed on the surface of the semiconductor light emitting element improves the light emitting efficiency of the element by reducing the reflection losses and total-reflection losses. The Fresnel lens and holographic diffuser can be formed on the surface of the light emitting element by using a chemical wet etching technique or dry etching technique together with a lithographic technique. The lens and diffuser can also be formed by shaving the surface of the element. Even when a stamping process which is another method of forming the optical element is used, the lens and diffuser can be formed on the surface of the element. The stamping process includes a step of pressing a shape obtained by inverting a desired optical element and a patterned stamping block against the surface of a light emitting diode.



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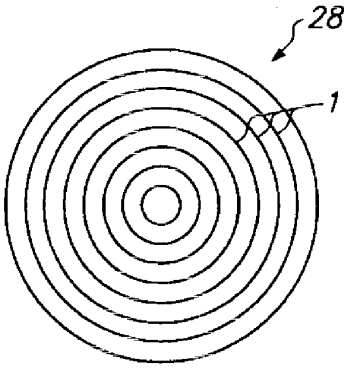
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最終頁に続く

(54)【発明の名称】　光取出率を改善するための発光デバイスにおける光学エレメントの形成

(57)【要約】
【課題】　光の取出率を改善するために半導体発光素子の面に形成されたフレネルレンズ及びホログラフィックディフューザの一方又は両方を含む発光デバイス、このような発光デバイスを形成するための方法を提供する。
【解決手段】　半導体発光素子の面に形成された光学エレメントは、反射損失及び全反射による損失を低減して、光の取出効率を改善する。フレネルレンズ、ホログラフィックディフューザは、化学的ウェットエッチング又はドライエッチング技術をリソグラフィー技術と共に用いて面上に形成できる。フレネルレンズ、ホログラフィックディフューザの形成は、表面に削り加工等を行ってもできる。光学エレメントを形成する別の方法であるスタンピング工程を用いても、半導体発光素子の面にフレネルレンズやホログラフィックディフューザを形成できる。スタンピングは、所望の光学エレメントを逆にした形状及びパターンスタンピングブロックを発光ダイオードの面に対してプレスする工程を含む。



【特許請求の範囲】
【請求項１】　半導体発光素子によって放射される光に作用を及ぼすよう、前記半導体発光素子の少なくとも一つの面にフレネルレンズ及びホログラフィックディフューザのうちの少なくとも一つを形成する工程を含む、発光デバイスを形成する方法。
【請求項２】　前記半導体発光素子は光を取り出すことを意図した少なくとも一つの光取出面を有し、前記形成工程を、前記半導体発光素子の少なくとも一つの光取出面において行うものである請求項１に記載の方法。
【請求項３】　前記形成工程は、スタンピングブロックを、前記半導体発光素子の少なくとも一つの面にプレスする工程を含んでいる請求項１に記載の方法。
【請求項４】　前記形成工程は、ウェハーボンディングプロセスと同時に実行され、前記ウェハーボンディングプロセスは、
前記半導体発光素子の第一のサブストレートを取り除く工程と、
第二のサブストレートを前記半導体発光素子にボンディングする工程とを含んでいる、請求項１に記載の方法。
【請求項５】　前記形成工程は、エッチング加工、削り加工、アブレーション加工、機械加工、スクライビング加工、放電加工、及びスタンピング加工から選択した少なくとも一つの方法を含んでいる請求項１に記載の方法。
【請求項６】　前記半導体発光素子の一又は二以上の側面を傾斜させる工程を含んでいる請求項１に記載の方法。
【請求項７】　請求項１に記載の方法において、前記半導体発光素子は発光層を有しており、前記方法は、さらに、前記発光層の予め選択された部分に光放射を制限することを含んでいる方法。
【請求項８】　前記制限することには、ホロニアクプロセスの適用、選択領域成長の使用、選択領域ボンディングの使用、ディフィージョンの使用、そしてイオン注入の使用の中から選択された少なくとも一つの方法が含まれている、請求項７に記載の方法。
【請求項９】　請求項１に記載の方法において、さらに、前記半導体発光素子の一又は二以上の面に反射材をコーティングする工程を含んでいる方法。
【請求項１０】　請求項１に記載の方法において、さらに、前記フレネルレンズ又は前記ホログラフィックディフューザに反射材をコーティングする工程を含んでいる方法。
【請求項１１】　請求項２に記載の方法において、さらに、前記取出面とは反対側の面に光学エレメントを形成する工程を含んでいる方法。
【請求項１２】　半導体発光素子と、
前記半導体発光素子の少なくとも一つの表面を形成する第一の光学エレメントと、を有し、前記第一の光学エレメントはフレネルレンズ及びホログラフィックディフューザのうちの一方を含んでいる発光デバイス。
【請求項１３】　請求項１２に記載のデバイスにおいて、さらに、前記デバイスの少なくもと一つの面をコーティングする反射材を含んでいるデバイス。
【請求項１４】　前記半導体発光素子の発光層が、主に前記第一の光学エレメントの予め決められた部分に向かって光子を放射するように作られた、請求項１２に記載のデバイス。
【請求項１５】　発光デバイスの少なくとも一つの面は傾斜されている、請求項１２に記載のデバイス。
【請求項１６】　前記半導体発光素子は、制限放射スポット発光ダイオードである、請求項１２に記載のデバイス。
【請求項１７】　前記半導体発光素子及び前記第一の光学エレメントは、
$(Al_xGa_{1-x})_yIn_{1-y}P$（$0 \leqq x \leqq 1$、$0 \leqq y \leqq 1$）
を含んでいる請求項１２に記載のデバイス。
【請求項１８】　前記発光ダイオードは、III-窒化物半導体化合物を含んでおり、前記第一の光学エレメントは、シリコンカーバイド及びサファイアのうちの一方を含んでいる、請求項１２に記載のデバイス。
【請求項１９】　前記半導体発光素子及び前記第一の光学エレメントは、アルミニウム・ガリウム・砒素半導体化合物を含んでいる請求項１２に記載のデバイス。
【請求項２０】　前記半導体発光素子は、フリップチップ構造を含んでいる請求項１２に記載のデバイス。
【請求項２１】　前記半導体発光素子は、前記半導体発光素子の発光層は前記フレネルレンズに対して実質的に垂直である、請求項１２に記載のデバイス。
【請求項２２】　請求項１２に記載のデバイスにおいて、前記デバイスの放射パターンは、前記第一の光学エレメントと前記半導体発光素子の発光層との距離に対する前記第一の光学エレメントの焦点距離の比によって制御されるデバイス。
【請求項２３】　前記第一の光学エレメントは、光をフォーカスする作用、光をコリメートする作用、光を発散する作用のうちの一つを達成するよう設計されたものである請求項１２に記載のデバイス。
【請求項２４】　前記第一の光学エレメントは、光を予め選択した方向に導くよう設計されたものである請求項１２に記載のデバイス。
【請求項２５】　請求項１２に記載のデバイスにおいて、さらに、前記半導体発光素子の前記第一の光学エレメントを有する面とは反対の面に第二の光学エレメントを有するデバイス。
【請求項２６】　前記第一のフレネルレンズ及び第二のフレネルレンズのうちの一方が光をフォーカスするよう設計されたものである請求項２５に記載のデバイス。

【請求項２７】　半導体発光素子によって放射される光に作用を及ぼすよう、前記半導体発光素子の少なくとも一つの面にスタンピングを行う工程を含んでいる、発光デバイスを形成するための方法。
【請求項２８】　請求項２７に記載の方法において、さらに、前記発光デバイスの面に反射層をコーティングする工程を含んでいる方法。
【請求項２９】　前記スタンピングを、前記半導体発光素子の半導体層及びサブストレート層のうちの少なくとも一方に対して行う、請求項２７に記載の方法。
【請求項３０】　前記半導体層は、アルミニウムを含む透明な化合物を含んでいる請求項２９に記載の方法。
【請求項３１】　前記プレスする工程は、室温よりも高い温度において実行される、請求項２７に記載の方法。
【請求項３２】　請求項３１に記載の方法において、さらに、前記プレス工程の後に前記半導体発光素子から前記スタンピングブロックを引き離すのを容易にするために、前記高い温度を低くする工程を含んでいる方法。
【請求項３３】　前記高い温度は、前記フレネルレンズを形成する前記少なくとも一つの面を構成する材料の延性遷移温度よりも高いものである請求項３２に記載の方法。
【請求項３４】　半導体発光素子と、
半導体発光素子の少なくとも一つの面にスタンピングされた少なくもと一つの光学エレメントとを含み、
前記光学エレメントは第一の光学エレメントである発光デバイス。
【請求項３５】　前記半導体発光素子の発光層は、主に前記第一の光学エレメントの予め選択した方向に光子を放射するよう設計されたものである請求項３４に記載のデバイス。
【請求項３６】　前記発光層及び前記第一の光学エレメントは、
$(Al_xGa_{1-x})_yIn_{1-y}P$（$0 \leqq x \leqq 1$、$0 \leqq y \leqq 1$）
を含んでいる請求項３４に記載のデバイス。
【請求項３７】　前記半導体発光素子は、III-窒化物半導体化合物を含んでおり、前記第一の光学エレメントは、シリコンカーバイド及びサファイアのうちの一方を含んでいる、請求項３４に記載のデバイス。
【請求項３８】　前記半導体発光素子及び前記第一の光学エレメントは、アルミニウム・ガリウム・砒素半導体化合物を含んでいる請求項３４に記載のデバイス。
【請求項３９】　前記発光ダイオードは、フリップチップ構造を有している請求項３４に記載のデバイス。
【請求項４０】　前記発光ダイオードは、前記発光ダイオードの発光層が前記フレネルレンズに対して実質的に垂直な構造を有している請求項３４に記載のデバイス。
【請求項４１】　複数の発光デバイスを含んでいる発光ダイオードアレーであって、
半導体発光素子と、
前記半導体発光素子の面に形成されたフレネルレンズ及びホログラフィックディフューザのうちの一つと、
を含んでいる発光ダイオードアレー。
【請求項４２】　複数の発光デバイスを含んでいる発光アレーであって、
半導体発光素子と、
前記半導体発光素子の面にスタンピングされた光学エレメントと、
を含んでいる発光アレー。
【請求項４３】　少なくとも一つの青色発光デバイス、少なくとも一つの緑色発光デバイス、少なくとも一つの赤色発光デバイスを含んだディスプレーデバイスであって、前記青色発光デバイス、緑色発光デバイス、赤色発光デバイスのうちの少なくとも一つは、
半導体発光素子と、
前記半導体発光素子の面に形成されたフレネルレンズ及びホログラフィックディフューザのうちの一つと、
を含んでいるディスプレーデバイス。
【請求項４４】　少なくとも一つの青色発光デバイス、少なくとも一つの緑色発光デバイス、少なくとも一つの赤色発光デバイスを含んだディスプレーデバイスであって、前記青色発光デバイス、緑色発光デバイス、赤色発光デバイスのうちの少なくとも一つは、
半導体発光素子と、
前記半導体発光素子の面にスタンピングされた一つの光学エレメントと、
を含んでいるディスプレーデバイス。
【請求項４５】　発光デバイスから放射される光に対して透明な材料に光学エレメントをスタンピングする工程と、
前記光学エレメントを半導体発光素子にボンディングする工程と、を含む、発光デバイスを形成する方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、発光デバイス一般に、より詳しくは、光取出率が改善された発光デバイスに関する。
【０００２】
【従来の技術】図１は、従来からの半導体発光素子１００であり、基板２０、多層構造２６、最上層２４から構成されている。半導体発光素子１００としては、例えば発光ダイオード（ＬＥＤ）又は半導体レーザーが考えられる。ＬＥＤは、電気エネルギーの入力流を電磁放射の出力流に変換するよう設計されたｐｎ接合デバイスである。ＬＥＤは、電磁スペクトルの紫外領域、可視領域、赤外領域の電磁放射を発することができる。可視ＬＥＤは通常、照明及びディスプレーに用いられ、また、電子機器とそのユーザーとの間の情報リンクとしての応用もある。赤外ＬＥＤは、オプトアイソレータ及び光ファイ

バー通信において有用である。半導体レーザーは、ＬＥＤと同様の方法で作製される。

【０００３】多層構造２６は、ここでは下部封止層（confining layer）２１、上部封止層２３、光子が発せられる活性層２２を含んでいるが、この構造に限られるものではない。上部封止層２３は、最上層２４を含んでいてもよい。半導体発光素子１００が分離した最上層２４を有していない場合は、上部封止層２３が最上層となる。

【０００４】多層構造２６の封止層２１，２３及び活性層２２は、通常、III-V半導体、III-窒化物半導体、II-VI半導体から形成される。最上層２４は、上部封止層２３上にエピタキシャル成長させることができるが、これもまた普通はIII-V半導体、III-窒化物半導体、II-VI半導体、あるいはこれらの化合物である。しかしながら、最上層２４は、封止層２１又は封止層２３を形成する材料とは異なる半導体化合物とすることもできる。最上層２４は、活性層２２によって発せられた光に対して透明となるよう、活性層２２よりも大きなバンドギャップを有する材料とすることが望ましい。ここでは「透明」という用語は、特定の半導体発光素子の放射波長において、吸収又は散乱による単光路損失が約５０％より少ない、より望ましくは約１０％より少ない状態で、光学エレメントが光を透過することを意味する。最上層２４は、上部封止層２３にウェハ・ボンディングされた透明なサブストレート（スーパーストレート）とすることができる。最上層２４はまた、その上にエピタキシャル層を成長させたサブストレートとしてもよい。

【０００５】下部封止層２１及び上部封止層２３は、活性層２２に、そしてコンタクト３１及びコンタクト３２に電気的に接続されている。通常、一方の封止層にはドナーがドープされてｎ型の封止層とされ、他方の封止層にはアクセプタがドープされてｐ型の封止層とされる。したがって、コンタクト３１と３２との間に適当な電圧を印加すると、ｎ型封止層からの電子とｐ型封止層からのホールが活性層２２内で結合して、等方的に光を発する。ＬＥＤとしての半導体発光素子１００についてのより詳細な説明については、Michael R. Kramesらに付与された「AlGaInN-based LED Having Thick Epitaxial Layer for Improved Light Extraction」と題された米国特許第６，１３３，５８９号、Fred A. Kish, Jr.らに付与された、いずれも「Transparent Substrate Light Emitting Diode with Directed Light Output」と題された米国特許第５，７９３，０６２号及び第６，０１５，７１９号を参照することができる。これらすべての特許を、参考としてここに援用する。

【０００６】半導体発光素子１００をＬＥＤ１００とすることができる。ＬＥＤについての問題は、光の取出効率が低いことである。この光の取出効率が低い原因は、ＬＥＤ１００から出ようとする光が、活性層２２によって発せられた光エネルギーのうちのわずかのみ（例えば透明基板を有するAlGaAsＬＥＤの場合、大体３０％程度）だということである。光の取出効率が低い結果、消費される電気的な入力のうちのわずかの部分だけが、外部から観測できる光に寄与する。光の取出効率は、ＬＥＤにおいて生成される光子の数に対する、ＬＥＤから出てくる光子の数の比として定義される。

【０００７】図１の経路３は、活性層２２の点光源２７から放射される光子の方向を示している。経路３によって示されるように、コンタクト３１，３２の吸収特性が、低い光の取出率に寄与する。経路３に沿って進む光子は、ＬＥＤ１００の内側面で反射されコンタクト３１によって吸収される。コンタクト３１及び３２は、金、ニッケル、アルミニウム、チタン、クロム、パラジウム、そしてこれらの合金又は化合物などの金属から形成することができる。

【０００８】低い光の取出効率を生じさせる損失の機構には、半導体発光素子内における吸収、光が一つの材料から屈折率の異なる別の材料へ入るときの反射損失、発光デバイス内で吸収されることになる全反射が含まれる。しかしながら、全反射は、活性層２２によって発せられた光子が発光デバイス１００とその周囲の材料との境界に臨界角（θc）よりも大きい角度で到達したときのみ、光子が半導体発光素子１００から出ることを妨げる。本実施例に関連する臨界角（図１にθcで示す）は、

$\theta c = arcsine(n_{surrounding} / n_{LED})$

によって定義される。ここで、$n_{surrounding}$及びn_{LED}はそれぞれ、発光デバイスの周囲の材料と発光デバイスの屈折率を示している。ＬＥＤはしばしばエポキシ内に封入されるが、その屈折率（n_{epoxy}）は大体１．５程度である。前述のIII-V半導体材料の一つで作られたＬＥＤでは、その屈折率は約２．４から約４．１までの範囲である。平均的な屈折率（n_{LED}）を約３．５とすると、θcの典型的な値は約２５°である。したがって、活性層２２内の点光源２７から発せられる光子のうち半角が２５°の「取出円錐」内の任意の表面を通るものは、ＬＥＤから外部へ放射される。ＬＥＤ１００と取出円錐の外側の材料との間の境界面に当たる光子は、全反射を繰り返し受け、例えば半導体層（活性層２２を含む）又はコンタクト３１及び３２によって吸収されることになる。すなわち、表面に垂直な軸に対して２５°よりも大きい角度で表面に当たる多くの光子は、最初の段階でＬＥＤから外部へは放射されない。発せられた光子のうちのより多くの部分が取り出される高い光の取出効率を有するＬＥＤが必要とされている。

【０００９】

【課題を解決するための手段】本発明は、半導体発光素子の光取出率を改善するとともに、所望の放射パターンを得るために光を導き、フォーカスし、そして散乱させ

るのに用いられる。本発明には、例えばフレネルレンズ、ホログラフィックディフューザなどの一又は二以上の光学エレメントに適合するようにされた半導体発光素子、そして半導体発光素子の表面をスタンピング（stamping）して光学エレメントに形成する方法が含まれる。半導体発光素子１００の一又は二以上の表面を、フレネルレンズ又はホログラフィックディフューザに形成することができる。フレネルレンズは、活性層２２から発せられたより多くの光子が垂直に近い入射角で半導体発光素子１００の表面に当たるようにし、全反射による光の損失を最小限に抑えることができるので、表面をフレネルレンズにすることは望ましい。さらに、フレネルレンズに形成された半導体発光素子の表面は、半導体発光素子を構成する材料とは異なる屈折率を有するレンズの材料によって通常引き起こされる光の反射損失を低減する。フレネルレンズ及びホログラフィックディフューザの一方又は両方を、フォトリソグラフィー、電子ビームリソグラフィー、イオンビームリソグラフィー、Ｘ線リソグラフィー、ホログラフィックリソグラフィーなどを含む（ただし、これらに限定されるものではない）リソグラフィー技術に関連したエッチングによって形成することができる。プラズマエッチング、反応性イオンエッチング（ＲＩＥ）、及び化学的手段を援用したイオンビームエッチング（ＣＡＩＢＥ）などの化学的ウェットエッチング又はドライエッチング技術を用いることができる。あるいは、イオンビーム削り加工（ion beam milling）又はフォーカスされたイオンビーム削り加工（ＦＩＢ）を用いてフレネルレンズを表面に刻印し、走査させた電子又はレーザービームを用いて表面にフレネルレンズをアブレーション加工し、または削り加工やスクライビング加工を行って機械的に半導体発光素子１００の表面にフレネルレンズを形成することもできる。

【００１０】スタンピングは、発光デバイスの表面上に光学エレメントを形成する別の方法である。スタンピングプロセスは、スタンピングを行うとする半導体材料の延性遷移点（ductile transition point）よりも高い温度で実行される。一つの実施例では、スタンピングは、ウェハ・ボンディングプロセスと統合される。ウェハ・ボンディングプロセスは通常６００℃近傍又はこれよりも高温で行われるので、ウェハ・ボンディングプロセスを容易にウェハ・ボンディングプロセスと統合することができ、これによって生産効率を向上させることができる。ウェハ・ボンディングプロセスでは、所望の品質のエピタキシャル層を成長させるためのテンプレートとして用いられた最初の吸収性のサブストレートを除去すること、そして光の取出率を改善するためにこれを透明なサブストレートと置き換えることを伴う。オプションとして、透明なサブストレートを半導体発光素子１００の第一の表面にボンディングする時点において、所望の光学エレメントの形状又はパターンの逆の形状又はパターンを有するスタンピングブロックを、半導体発光素子１００の第二の表面、透明サブストレートの表面、又はこれらの両方に対してプレスしてもよい。圧力を開放したときに、所望の光学エレメントに形作られた表面を有する発光デバイスが形成される。スタンピングに用いられるスタンピングブロックは、通常、光学エレメントの形成時に適用されるプロセス温度よりも高い融点を有する。スタンピングブロックに適する材料としてモリブデン合金、グラファイト、シリコンカーバイド、そしてサファイアなどがあるが、これらに限定されるものではない。半導体発光素子の一又は二以上の表面上に、光学エレメントを形成することができる。スタンピングプロセスは独立したプロセスであるが、ウェハ・ボンディングプロセスの前、後、あるいは同時に行うことも可能である。あるいはまた、スタンピングプロセスを、後に半導体発光素子１００に対してボンディングされる材料をスタンピングするのに用いてもよい。

【００１１】本発明は、容易に、別の応用に合うよう適合させることができる。例えば、照明用に光をコリメートするように光学エレメントを作ったり、あるいは光ファイバーに光をフォーカスするように作ることもできる。さらに、ＬＥＤの任意の表面を一又は二以上の光学エレメントに形作ったり、二以上の表面を一又は二以上のフレネルレンズに形作ったりもできる。コリメートされた光又はフォーカスされた光を所望の方向に導くために、反射コーティングを用いることもできる。半導体発光素子１００上に多数の光学エレメントを形成することによって作られるダイオードアレーを、高出力の応用目的に用いることもできる。

【００１２】光学エレメントの予め決められた部分に向かって放射される光子の割合を増大させることによって、本発明の有用性はさらに高まる。例えば、フレネルレンズが存在してもその縁部に到達する光子は有益性が小さいので、放射されたより多くの割合の光子がフレネルレンズの中心に向かって放射されるような制限放射スポット（confined-emission spot）ＬＥＤを作ることができる。光子の放射を活性層の選択した領域へ閉じ込める方法には、イオンの注入又は拡散、酸化物不活性化（oxide passivation）、選択領域成長（selective area growth）、選択領域ボンディング（selective area bonding）が含まれる。あるいは、半導体発光素子１００又は活性層２２の外側の縁部を、エッチングで取り除いてもよい。外側の縁部をエッチングで取り除くことによって、傾斜した側面を有する発光デバイスを作ることができる。

【００１３】

【発明の実施の形態】本明細書で参照する図面は、縮尺通りには描かれていない。

【００１４】本明細書において「取出面」とは、光出力面となるよう意図した発光デバイスの面を指す。発光デ

バイスは、二以上の取出面を備えることもできる。図示を簡単にするために、図では取出面を一番上の面としている。発光デバイスはＬＥＤとすることができる。ここで説明するＬＥＤの光を生成する部分は、ＬＥＤの通常の活性層である。ここで用いている「発光デバイス」は、少なくとも一つの半導体発光素子１００を有するデバイスを含んでいる。本発明は、発光デバイスの表面をスタンピングして光学素子にすることと、発光デバイスの表面にスタンピングを含む任意の方法を用いてフレネルレンズ又はホログラフィックディフューザを形成することの両方を含んでいる。本発明はまた発光デバイスの表面上に形成されたホログラフィックディフューザを含んでいるが、この例及び説明では、分かり易い例示とするために、主としてフレネルレンズを参照する。同じく分かり易い例示のために、半導体発光素子１００を発光ダイオード１００として説明する。異なる図で同じ符号を有する要素は、同じものである。

【００１５】図２Ａ、図２Ｂ、図３Ａ、図３Ｂ、図４Ａ、図４Ｂ、図５Ａ、図５Ｂに示したように、フレネルレンズ２８は、収束レンズの単一の曲面とは対照的に、表面上に一連の同心のグルーブが形成されて構成されている。グルーブ１は、屈折面として作用する湾曲した、あるいは角度をつけた面を有している。グルーブ１は、図２Ａ及び図３Ａに示すように、一定間隔とすることができる。図２Ｂ及び３Ｂに示すように、フレネルレンズ２８のグルーブが一定間隔のときは、フレネルレンズ２８を希望の焦点距離とするようにグルーブの高さを変えることができる。グルーブの形状は、例えば光線を集束させるために図２Ｂのように、または光線を発散させるために図３Ｂに示すように変えることができる。あるいは、フレネルレンズ２８のグルーブが図４Ｂ、図５Ｂに示すように同じ高さのときは、グルーブ１間の間隔を調整して、希望の焦点距離のフレネルレンズ２８とすることができる。図４Ａ及び図５Ａに示すフレネルレンズ２８は、レンズの縁に近づくにつれてグルーブの間隔が狭くなる。図４Ｂ及び図５Ｂは、光を希望する通りに導くためにグルーブ１の形状を調整できることを示している。図４Ｂのフレネルレンズは光線を集束させ、図５Ｂのフレネルレンズは光線を発散させる。フレネルレンズ２８のグルーブ１は、レンズ中心の周囲に同心的に配置することは必要ではない。例えば図６には、同心でないグルーブ１を有するフレネルレンズ２８が示してある。フレネルレンズは、非球面に基づくものとすることも、球面に基づくものとすることもできる。さらに、フレネルレンズが形成される表面は平面である必要もない。フレネルレンズを任意の形状のＬＥＤ上、例えば長方形のＬＥＤ上、楕円形のＬＥＤ上、ピラミッド型のＬＥＤ上、そして円柱形のＬＥＤ上に形成することもできる。フレネルレンズ２８を半導体発光デバイス上に形成するときは、オプションとして、図２Ｂ、図３Ｂのフレネルレンズ２８の縁の近傍の高いグルーブ、および図４Ｂ、図５Ｂのフレネルレンズ２８の縁の近傍の間隔の狭いグルーブを省くことができる。

【００１６】図２Ｂ、図３Ｂ、図４Ｂ、図５Ｂは、通常の収束又は発散レンズ２の厚さを、フレネルレンズ２８と比較している。図示のように、フレネルレンズ２８は、ほぼ同じ焦点距離を有する通常のレンズ２よりも薄くなっている。レンズ材料（すわち半導体材料）は本来的にいくぶんかの光を吸収するので、ＬＥＤへの応用目的では、厚い普通のレンズよりも薄いフレネルレンズ２８は好ましい。

【００１７】図７Ａは、フレネルレンズ２８として示した、表面上に形成された光学エレメント２８を有する発光デバイスを例示している。半導体発光素子１００の取出面に形成されたフレネルレンズ２８は半導体発光素子１００からの光の取り出しを助けるが、これは、取出面が平坦でなくグルーブ１を有している場合には、放射されたより多くの光子が垂直に近い入射角で取出面に当たるからである。垂直に近い入射角で表面に当たる光子は全反射を受けず、したがってより取り出しやすくなる。反射材４０で底面をコーティングすると、底面における反射損失又は吸収損失による光の損失を軽減するのを助ける。経路５に沿って進む光子も、減衰及び最終的な吸収を受ける。後述のように、経路５に沿って進む光子を取り出すために、底面に設けたフレネルレンズを用いることもできる。

【００１８】図７Ａ、図７Ｂ、図７Ｃは、フレネルレンズ２８の高さ、グルーブの間隔、焦点距離と同様に、距離δによって、どのように発光デバイスの放射パターンを操作するかを例示している。距離δは、活性層２２とフレネルレンズ２８の距離を示している。距離δ、フレネルレンズ２８の水平位置、そしてフレネルレンズ２８の焦点距離は、発光デバイスの発光パターンに影響する。光源を実質的に収束レンズの焦点距離近くに置いたときは、図７Ａに示すように、出て行く光線は実質的に並行になる。距離δを変えることによって、光線を実質的に図７Ｂに示すように収束させたり、図７Ｃに示すように発散させることができる。図７Ｂに示すような光を収束させるような実施例は、光ファイバーへの応用に用いることができる。

【００１９】フレネルレンズ又はホログラフィックディフューザを表面に形成する方法は数多くある。「彫刻法」は、まず、例えば多層構造２６上に最上層２４を形成し、そしてプラズマエッチング、反応性イオンエッチング、化学的手段を援用したイオンビームエッチング（ＣＡＩＢＥ）などの化学的ウェットエッチング又はドライエッチング技術によって、最上層２４に希望のパターンを形作ることが必要となる。オプションとして、エッチング技術については、リソグラフィー技術を用いることもできる。リソグラフィー技術には、フォトリソグ

ラフィー、電子ビームリソグラフィー、イオンビームリソグラフィー、Ｘ線リソグラフィー、ホログラフィックリソグラフィーが含まれる（ただし、これらに限定されるものではない）。さらに、イオンビーム削り加工又はフォーカスされたイオンビーム削り加工を用いて表面に刻印し、走査させた電子又はレーザービームを用いて表面をアブレーション加工し、放電加工（ＥＤＭ）によって表面に加工し、または削り加工やスクライビング加工を行って、機械的に半導体発光素子１００の表面に、希望の光学エレメントを形成することができる。

【００２０】フレネルレンズ又はホログラフィックディフューザを、ボンディング法を用いて形成することもできる。ボンディング法には、多層構造２６に、通常ボンディング材料を用いて光学エレメントをボンディングする必要がある。ボンディング材料は、スピニング、スパッタリング、蒸着、化学気相成長、金属・有機化学気相成長、気相エピタキシャル、液相エピタキシャル、分子ビームエピタキシャルなどの一般的な堆積技術を用いて堆積させることができる。図７Ａに示した実施例ではボンディング材料を示していないが、ボンディング材料は、光学エレメント２８と上部導電層２３の間の境界２５ａにある。しかし、発光デバイスが最上層２４を含んでいる場合には、ボンディング材料は、光学エレメント２８と最上層２４の間にあってもよい。

【００２１】ボンディング法を用いるときは、境界２５ａ又は２５ｂにおける反射光損失を最小限に抑えるために、ボンディング材料がn_{LED}又はn_{lens}（n_{LED}とn_{lens}が異なる場合）に非常に近い屈折率（$n_{bonding}$）を有することが望ましい（図７Ａ）。デバイスが温度変化を受けたときのひずみを最小限に抑えるために、半導体発光素子とフレネルレンズ２８の両方と同等の熱膨張係数を持つボンディング材料とすることができる。さらに、ボンディング材料を、活性層２２によって発せられる光の波長に対して透明にすることもできる。例えば、レンズとボンディング材料を、以下に列挙するもののうちの一つとすることができる（ただしこれらに限定されるものではない）：屈折率の大きい光学ガラス、ＧａＰ（６００ｎｍで、ｎ～３．３）ＩｎＧａＰ（６００ｎｍで、ｎ～３．７）、ＧａＡｓ（５００ｎｍで、ｎ～３．４）、ＧａＮ（５００ｎｍで、ｎ～２．４）などのIII-V半導体、ＺｎＳ（５００ｎｍで、ｎ～２．４）、ＺｎＳｅ（５００ｎｍで、ｎ～２．６）、ＣｄＳ（５００ｎｍで、ｎ～２．６）、ＣｄＴｅ（５００ｎｍで、ｎ～２．７）、ＺｎＴｅ（５００ｎｍで、ｎ～３．１）などのII-VI半導体、IV族の半導体、そしてＳｉ（５００ｎｍで、ｎ～３．５）及びＧｅ（５００ｎｍで、ｎ～４．１）などの化合物、屈折率の大きい有機半導体、屈折率の大きい有機化合物、そしてこれらの混合物又は合金。$n_{bonding}$がn_{LED}及びn_{lens}と異なる場合には、半導体発光素子とボンディング材料の境界、そしてボンディング材料とフレネルレンズ２８の境界の両方において反射光損失が生じる。

【００２２】レンズ材料は、ボンディング材料なしで、高温環境でレンズと多層構造とをプレスすることで接着されるものを選択するのがよい。ボンディング材料を使わなければ、ボンディング材料の屈折率がn_{LED}と異なることによって増える光の損失を低減させることができる。接着については、「LED with Improved Light Extraction Efficiency」と題された米国特許出願第０９／６６０，３１７号においてさらに詳しく説明されており、その内容は、参考としてここに援用する。

【００２３】本発明に用いることができるさらに別の方法は、スタンピング法である。図８Ａは、半導体発光素子１００を含む発光デバイスと、光学エレメント２８が形成された表面を示している。図８Ｂは、図８Ａの光学エレメント２８として用いることのできるホログラフィックディフューザの概略図を示す。ホログラフィックディフューザの表面には、ランダムで非周期的な多数の小型レンズ（microlenslet）が含まれている。ホログラフィックディフューザは光を発散させ、ノイズ及び色回折（color diffraction）を取り除く。図８Ｂはホログラフィックディフューザとして光学エレメント２８を示しているが、光学エレメント２８は、通常のレンズ、フレネルレンズ、あるいは反射部なと、他の任意の光学エレメントであってもよい。

【００２４】図９に例示した典型的なプロセスでは、光学エレメント２８のパターンとは逆のパターンを有するスタンピングブロック７０によって、最上層２４がスタンピングされる。図９は、光学エレメント２８としてフレネルレンズ２８を示している。このスタンピング法は、半導体発光素子１００の任意の表面に光学レンズ２８を形成するのに用いることができる。図９は、スタンピングと同時に実行されるウェハーボンディングプロセスを示しているが、スタンピングはウェハーボンディングの前又は後、あるいは完全に別な独立したプロセスとして実行することも可能であることが理解されるだろう。例えば、ウェハーボンディングされていない半導体発光素子１００上に、光学エレメントをスタンピングしてもよい。あるいはまた、最初に材料の上で光学エレメントをスタンピングし、後に材料を半導体発光素子１００に接着することもできる。

【００２５】スタンピング法では、フレネルレンズ２８が形成されるのがＬＥＤの最上層２４であることから、フレネルレンズ２８の屈折率とＬＥＤの最上層２４の屈折率が同じくなる蓋然性は高い。スタンピングプロセスでは、半導体発光素子１００を少なくとも最上層２４の延性遷移点（ductile transition point）まで加熱し、そしてスタンピングブロック７０をプレスする。必要であれば、スタンピングを容易にするために、１００ｐｓｉ又はそれ以上の圧力を加えてもよい（正確な圧力は、

使用する材料及びプロセス温度に依存する）。半導体発光素子１００の最上層２４にスタンピングしたあとは、スタンピングブロック７０を得られた発光デバイスから離し易くするために、圧力を開放し温度を下げることができる。半導体発光素子１００上に正確なフレネルレンズのパターンをスタンピングするためには、スタンピングブロックの材料は、加えられる温度及び圧力に耐えられるものでなければならない。このため、スタンピングブロックの材料は、表面にスタンピングがなされる材料（例えば半導体材料）の延性遷移点よりも高い延性遷移点を有していることが適当である。スタンピングブロックとして適当な材料の例には、ＴＺＭ（モリブデン、チタン、ジルコン、そしてカーボンの化合物）などのモリブデン合金、グラファイト、シリコンカーバイド、そしてサファイア、ステンレススチール、Hastalloy（商標）、Kovar（商標）、Nichrome（商標）、タングステン及びタングステン合金、タンタル、ニオブ、チタン合金などが含まれる。

【００２６】製造プロセスにおいて通常は別個のステップであるボンディングプロセスと異なり、スタンピングは、ウェハーボンディングと同時に実行することも（図９参照）、あるいはウェハーボンディングプロセスとは別にその前又は後に行うことも可能である。ウェハーボンディングプロセスの目的は、まず通常は光を吸収する第一のサブストレート２０．１を取り除き、そしてこれを、より多くの光が外部へ到達できる新しいサブストレート２０．２と置き換えることによって、光の取出率を改善することである。第一のサブストレート２０．１は、所望の機械的特性を持った半導体発光層を製造するのに適合する材料である。例えば、高品質のエピタキシャル成長を達成し、確実な格子整合を得るために、標準的な吸収性のサブストレート材料を利用することができる。これらの吸収性の成長サブストレートは通常、半導体発光素子の放射エネルギーより小さいか又は同等のバンドギャップを有している。多層構造２６を成長させた後、第一のサブストレート２０．１を取り除く。第一のサブストレート２０．１は、化学エッチング及びラップ仕上げ／研磨を含む方法（たたし、これらには限定されない）によって取り除くことができる。

【００２７】第一のサブストレート２０．１を取り除いたら、続いて、光学的には透明な第２のサブストレート２０．２を半導体発光素子１００に接着する。接着の手順には、新たなサブストレート２０．２を、その組成に依存して２５℃と１０００℃の間の温度に加熱することが含まれる。ウェハーボンディングプロセスについては、Fred A. Kishらに付与された「Wafer Bonding of Light Emitting Diode Layers」と題された米国特許第５，５０２，３１６号においてさらに詳しく説明されており、その内容はここに援用するものとする。新たなサブストレート２０．２とスタンピングブロック７０の両方を半導体発光素子１００に同時にプレスすることによって、スタンピングプロセスをウェハーボンディングプロセスに組み込むことができる。スタンピングブロック７０は、新たなサブストレート２０．２、最上層２４、あるいはこれらの両方に対してフレネルレンズ２８をプレスすることができる。図９では分かり易さと簡単のためにただ一つの光学エレメントを示しているが、スタンピングブロック７０には、二以上の光学エレメントのパターンを含ませることもできる。

【００２８】図１０は、側面を傾斜させた半導体発光素子１００を示している。側面を傾斜させると、経路３及び経路４の違いとして示すように、光子が反射する角度にすることによって光の取出率が向上する。側面が傾斜しているときは、活性層２２によって放射された光子は、経路３ではなく経路４（実線）に沿って進むことができる。経路３は、側面が傾斜していない半導体発光素子における経路である（図７Ａ参照）。図１０に点線で示した経路３は、側面が傾斜していないときに、活性層２２の点２７から放射される光子が側面で反射されコンタクト３１によって吸収されることを示している。しかしながら、図１０に実線で示した経路４は、傾斜させた発光デバイス内で光源２７から同じ方向に放射された光子がフレネルレンズ２８の方向へ反射され、発光デバイスから取り出されることを示している。このように側面を傾斜させると、傾斜させない場合に発光デバイスからは取り出せない光子のいくらかを取出面へ向けることによって、光の取出効率が改善される。さらに吸収を少なくするために傾斜させた側面を金属（例えば銀）又は誘電体などの反射材４０でコーティングすれば、光の取出率はさらに改善される。

【００２９】図１１は、活性層２２の断面領域がフレネルレンズ２８の断面領域よりも小さい半導体発光素子１００を含む発光デバイスを示している。ここで断面領域は、半導体発光素子１００の異なる層の境界に平行な面内にある。活性層の縁部からの電流を遮断するために、開口部又は保護リングを用いることができる。あるいは、活性層２２の縁部からの電流を遮断し又は縁部から離れるように電流を流すために、イオンの注入又は拡散を用いることができる。パターン化ウェハボンディング及びパターン化エピタキシャル成長とも呼ばれる選択領域成長（selective area growth）及び選択領域ボンディング（selective area bonding）は、光放射を閉じ込めるための二つのさらに別の方法である。選択領域成長及び選択領域ボンディングについては、米国特許第５，７９３，０６２号において議論されており、その内容は参考としてここに援用する。さらに、活性層２２の縁部に酸化物を形成して不活性化することによって、制限放射スポット（confined-emission spot）ＬＥＤを作ることができる。その一つを図１１に示した制限放射スポットＬＥＤは、ホロニアクプロセス（Holonyak process）

を用いて作ることができる。ホロニアクプロセスでは、ＬＥＤを３時間まで３７５℃と５５０℃の間の温度にすることによって、メサ（mesa）３３を形成する必要がある。ホロニアクプロセスは不要なアルミニウム酸化物の形成を防ぐために実行されるが、このプロセスにおいて制限層２３の上部には電気的絶縁性の天然の酸化物３４が形成される。ホロニアクプロセスの詳細及びその応用については、Nick Holonyak, Jr.らに付与された「AlGaAs Native Oxide」と題する米国特許第５，２６２，３６０号及びNick Holonyak, Jr.らに付与された「Semiconductor Devices Fabricated with Passivated High-Aluminum III-V Material」と題された米国特許第５，５１７，０３９号を参照することができる。これらの両特許の内容は、参考としてここに援用する。

【００３０】図１１に示した制限放射スポットＬＥＤにおいて、最上層２４は、アルミニウムを含んだｐ型の導電層とすることができる（ただしこれには限定されない）。メサ３３は、アルミニウムを含んだ透明なｐ型層とすることができる。最上層２４の体積酸化速度、あるいは特定のＬＥＤ１００が別個の最上層２４を持たない場合には上部制限層２３の体積酸化速度よりも、導電層の横方向の酸化速度の方が速くなるように、導電層（これは、例えば高アルミニウム濃度のIII-V半導体からなる）の組成として高いモル比を有するものを選択する。図１１は、アルミニウムを含む層を露出させたＬＥＤデバイスを示している。アルミニウムを含む層の異方性酸化は、メサ３３及び天然の酸化物３４を形成させる。天然の酸化物３４の絶縁特性は、電流をこれらの領域に制限し、これによって制限放射スポットＬＥＤが得られる。この例におけるアルミニウムを含むｐ型導電層である最上層２４及びメサ３３は、酸化速度においてそれぞれに適切な異方性を有する、アルミニウムを含む任意の透明な化合物から形成することができる。

【００３１】図１２及び図１３は、二つの光学エレメント２８，２９を含む本発明の実施例を示しており、二つの光学エレメントのうちの一方には反射材４０がコーティングされて反射部を形成している。図１２は、フレネルレンズ２８を有する表面とは反対の側に設けられた反射部２９としての光学エレメント２９を示している。フレネルレンズ２８と反射部２９の両方のグルーブは、入射光線をコリメートするようになパターンとされている。したがって、光源２７から放射された光子が破線で示した経路に沿って進んで反射部２９に当たると、反射部２９は、光子をコリメートして反射して上のフレネルレンズ２８の方向へ戻す。反射部２９がないと、点光源２７から放射された光子は、図７Ａに示した経路５に沿って進み、発光デバイスからは出られない。経路５に沿った光子は内部で何度も反射され、吸収され、減衰され、あるいは取出面ではない面から取り出される。

【００３２】図１３は、図１２と同様に、発光デバイスの一つの表面上のフレネルレンズ２８と、反対側の表面の反射部２９を示している。しかし、図１３の反射部２９のグルーブは、図１２のように入射した光子をコリメートするのではなく、代わりに点光源２７上にフォーカスする。図１３の発光デバイスは、図１２では経路６に沿って進んだであろう光子を、図１３の経路７に沿って進ませることによって、軸に沿って取り出される光の強度を高める。図１３の反射部２９は、距離δ、反射部２９の水平位置、グルーブのパターンのうちの一又は二以上を調整することによって、入射した光子をフレネルレンズ２８に向かって戻るようコリメートし、フォーカスし、発散させ、あるいは導くように作ることができる。同様に、光子を、ＬＥＤ内の吸収領域、例えば活性層２２、コンタクト３１及び３２から離れるように導くことができる。この分野の当業者であれば、フレネルレンズを設計し、所望の放射パターンを特定の応用目的に適合するように仕立てることができるだろう。例えば、図１３の実施例は、軸に沿った高い強度を必要とする応用目的については、図１２の実施例よりも好ましい。

【００３３】図１４及び図１５に示した例では、本発明は、取出面に光学エレメントを必要としない。点光源２７から放射された光子は、図１４ではフォーカスされ、図１５では発散される。いずれの場合も、光子は取出面に向かって上向きに反射される。図１４の実施例は図１３の実施例のように軸に沿った強度が高くなり、例えば光ファイバーへの応用といった軸に沿った高い強度を必要とする応用目的に有用である。

【００３４】図１６は、フリップチップ構造を用いた発光デバイスを示している。フリップチップ構造では、コンタクト３１と３２を同じ側、この場合の例では底面側に配置することができる。コンタクト３１及び３２はしばしば光を吸収するものであり、また光取出面の一部を占めることになるので、これらを光取出面から無くすことによって、より多くの光を取出面を通してＬＥＤデバイスから取り出すことができる。

【００３５】図１７は、封止層２１，２３及び活性層２２の向きが、取出面に対して実質的に垂直である発光デバイスを示している。図１７に示した発光デバイスは、図１の半導体発光素子１００を９０度回転させて光が半導体発光素子１００の側面から取り出されるようにしたものである。フリップチップ構造と同様に、図１７に示した構造は、取出面にコンタクトがないという点が有利である。

【００３６】本発明のＬＥＤを多数一緒にして、高出力の応用に用いることができる。例えば図１８は、図１３に示したタイプの発光デバイス三つをアレー状に配置して、高い光出力を発するようにしたものである。ＬＥＤチップ上又はウェハー上に形成することができるこれらのダイオードアレーは、通常、単一の半導体発光素子のチップに比べてより大きい面積を有する。また、本発明

のＬＥＤデバイスは、赤、緑、青のＬＥＤをピクセルエレメントとして用いるカラーディスプレーパネルに適している。このようなディスプレーは周知であり、この例を図１９に示した。ディスプレーパネル５０は、赤（５２）、緑（５４）、青（５６）のＬＥＤをそれぞれ含み、これらを周知の回路によって選択的に光らせることによって画像を表示させる発光デバイスのアレーを有している。図１９では簡単のために三つのピクセルだけを示している。一つの実施例として、発光デバイスをカラム状に配置した。他の実施例として、発光デバイスを別のパターン、例えば三角形などに配置することもできる。高い光取出率を有する発光デバイスを、ＬＣＤディスプレーのバックライト用に使用することもできる。

【００３７】本発明について、特定の実施例を挙げて例示したが、本発明の範囲を、例示したこれらの特定のあるいは好適な実施例に限定することを意図するものではない。例えば、光検出器や太陽電池などのデバイスについて、ここに開示した実施例は有益なものとなろう。

【図面の簡単な説明】

【図１】従来からの半導体発光素子の概略図である。

【図２Ａ】光を収束するよう設計された、高さの異なるグルーブを一様な間隔で設けたフレネルレンズの平面図である。

【図２Ｂ】収束レンズと図２Ａのフレネルレンズの断面を示した図である。

【図３Ａ】光を発散するよう設計された、高さの異なるグルーブを一様な間隔で設けたフレネルレンズの平面図である。

【図３Ｂ】発散レンズと図３Ａのフレネルレンズの断面を示した図である。

【図４Ａ】一様な高さのグルーブを有し、グルーブ間の間隔をレンズ中心からの距離の関数とした、収束フレネルレンズの平面図である。

【図４Ｂ】収束レンズと図４Ａのフレネルレンズの断面を示した図である。

【図５Ａ】一様な高さのグルーブを有し、グルーブ間の間隔をレンズ中心からの距離の関数とした、発散フレネルレンズの平面図である。

【図５Ｂ】発散レンズと図５Ａのフレネルレンズの断面を示した図である。

【図６】レンズ中心について同心でないグルーブを有するフレネルレンズの平面図である。

【図７Ａ】本発明に基づいて一つの取出面上に光をコリメートするフレネルレンズが形成された発光デバイスの概略図である。

【図７Ｂ】本発明に基づいて取出面上に光をフォーカスするフレネルレンズが形成された発光デバイスの概略図である。

【図７Ｃ】本発明に基づいて取出面上に光を発散するフレネルレンズが形成された発光デバイスの概略図である。

【図８Ａ】表面が光学エレメントに形作られた発光デバイスの概略図である。

【図８Ｂ】本発明で用いることができるホログラフィックディフューザの面の平面図である。

【図９】スタンピングプロセス及びウェハーボンディングプロセスを統合する典型的な例を示した概略図である。

【図１０】表面にフレネルレンズを形成した、傾斜した側面を有するＬＥＤの概略図である。

【図１１】異方性を持つ天然の酸化物を形成した制限放射スポットＬＥＤ上に形成されたフレネルレンズの概略図である。

【図１２】半導体発光素子の対向する二つの面に光をコリメートするフレネルレンズを形成し、一方を反射材でコーティングした発光デバイスの概略図である。

【図１３】半導体発光素子の対向する二つの面にフレネルレンズを形成し、反射材をコーティングしたレンズが光を活性層にフォーカスするようにした発光デバイスの概略図である。

【図１４】軸に沿った強度を高めるために、半導体発光素子の取出面ではない面に形成された、光をフォーカスするフレネルレンズの概略図である。

【図１５】半導体発光素子の取出面ではない面に形成され、反射材でコーティングされた、光を発散するフレネルレンズの概略図である。

【図１６】フリップチップ構造の発光デバイスの概略図である。

【図１７】実質的にフレネルレンズに垂直な活性層を有する発光デバイスの概略図である。

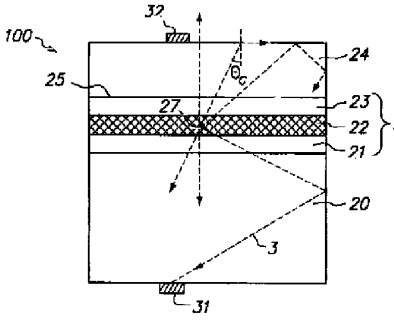
【図１８】単一のサブストレート上のダイオードアレーの概略図である。

【図１９】本発明に基づいた、発光デバイスが組み込まれたディスプレーデバイスの概略図である。

【符号の説明】

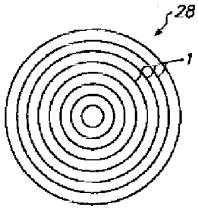
２０…サブストレート、２１…下部封止層、２２…活性層、２３…上部封止層、２４…最上層、２６…多層構造、２７…光源、２８…フレネルレンズ、３１，３２…コンタクト、３３…メサ、３４…酸化物、４０…反射材、７０…スタンピングブロック、１００…半導体発光素子、５０…ディスプレーパネル、５２…赤色ＬＥＤ、５４…緑色ＬＥＤ、５６…青色ＬＥＤ

【図1】

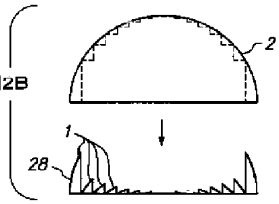


（従来技術）

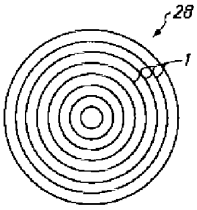
【図2A】



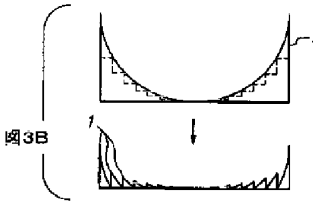
【図2B】



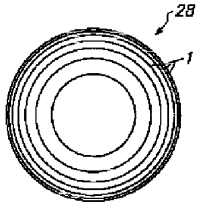
【図3A】



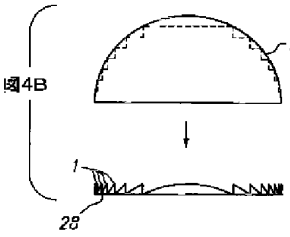
【図3B】



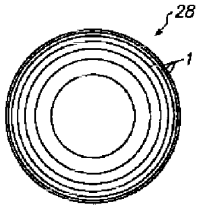
【図4A】



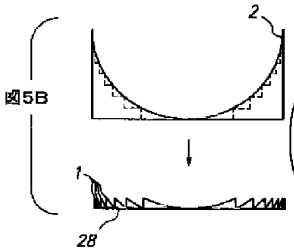
【図4B】



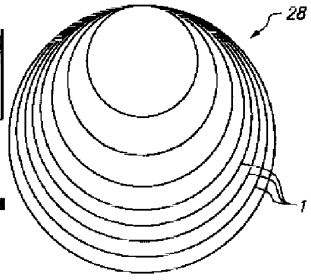
【図5A】



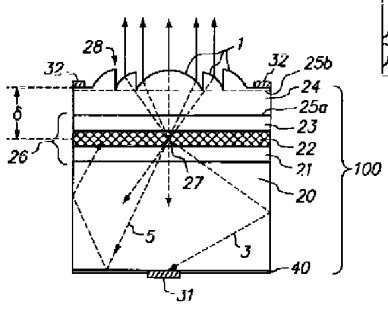
【図5B】



【図6】



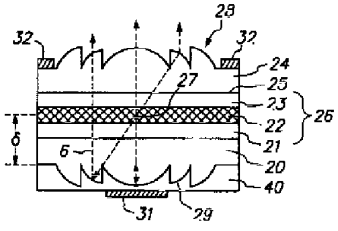
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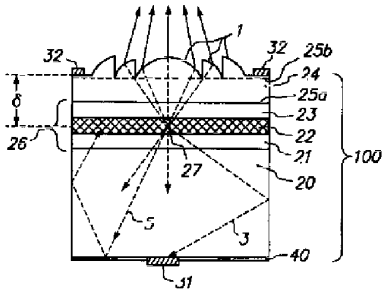
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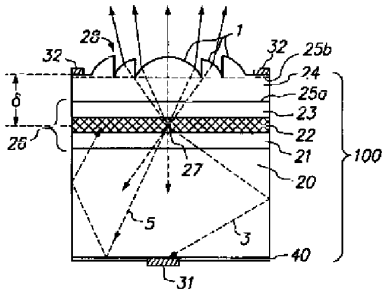
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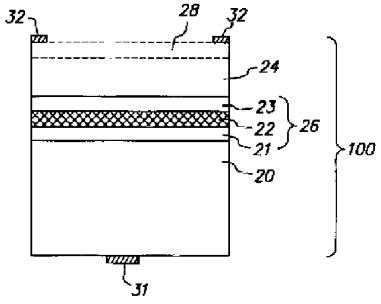
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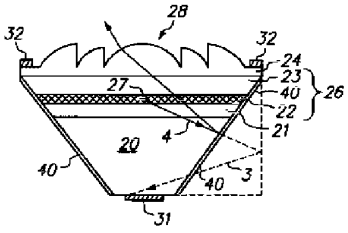
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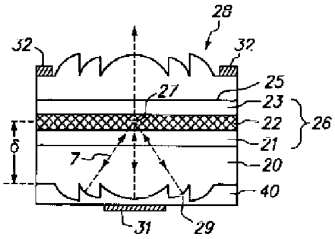
【図8A】



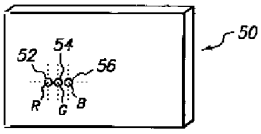
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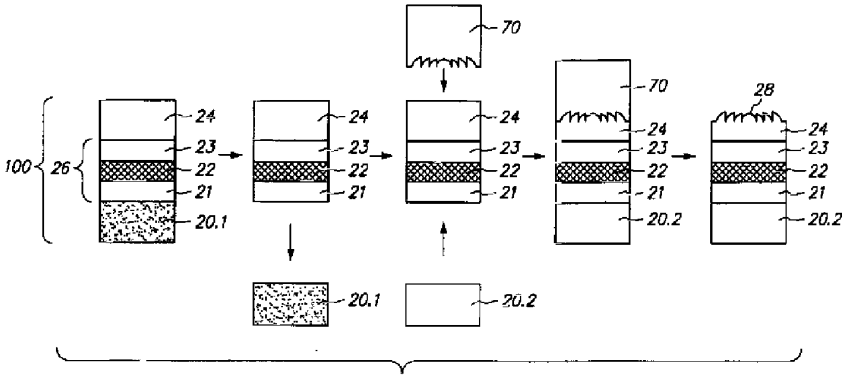
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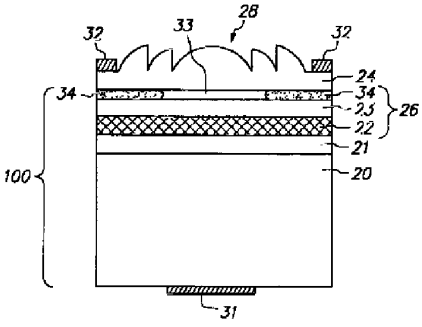
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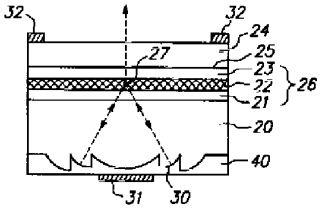
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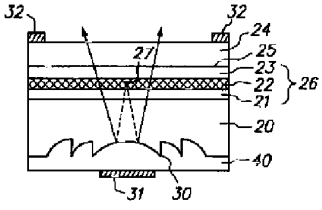
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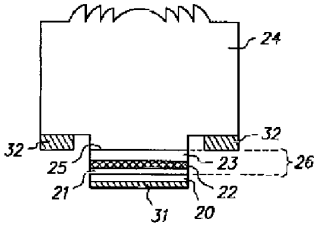
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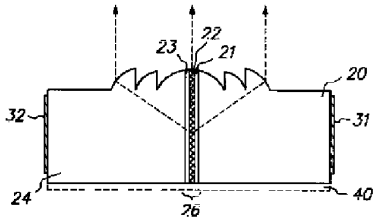
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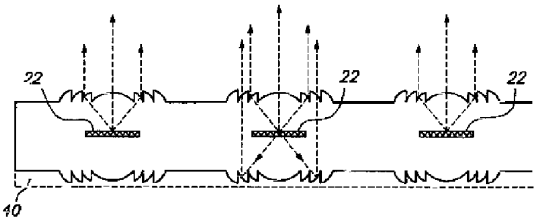
【図16】



【図１７】



【図１８】



フロントページの続き

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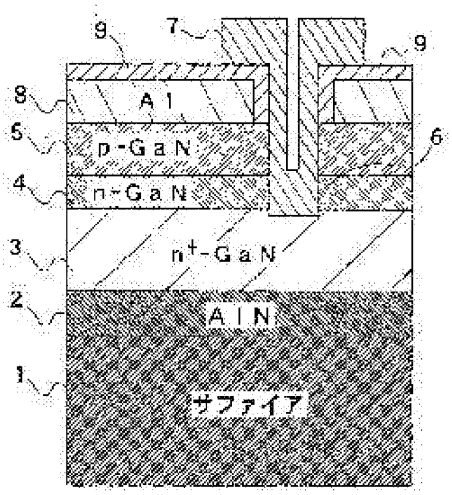
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(54) SEMICONDUCTOR LIGHT EMITTING DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a semiconductor light emitting device which can be improved in emission efficiency per unit power.
SOLUTION: The semiconductor light emitting device comprises a support substrate 1, a semiconductor layer 3 of a first conductivity type, an active layer 4 which is a light emitting layer, and a semiconductor layer 5 of a second conductivity type, all of which are stacked in this order. In the semiconductor light emitting device, a trench 6 is formed which is extended from the semiconductor layer 5 of the second conductivity type through the active layer 4 and reaches the semiconductor layer 3 of the first conductivity type. A first electrode 7 is formed in the trench 6 while a second electrode 8 is formed on the semiconductor layer 5 of the second conductivity type. At least, on a facing surface of the first electrode 7 and the second electrode 8, an insulation section 9 is formed.



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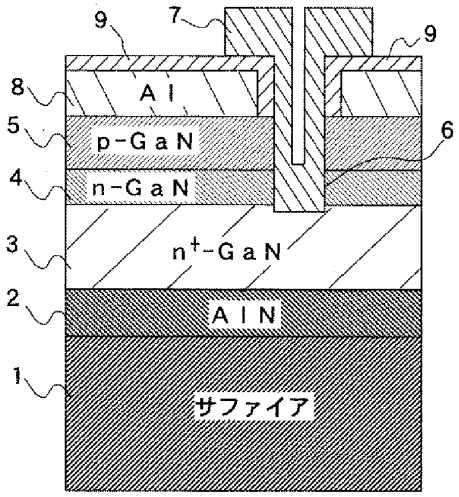
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最終頁に続く

(54)【発明の名称】半導体発光素子

(57)【要約】
【課題】単位電力あたりの発光効率が向上するような半導体発光素子を提供する。
【解決手段】本発明に係る半導体発光素子は、支持基板１と、第１導電型半導体層３と、発光層である活性層４と、第２導電型半導体層５とを順次積層して備えた半導体発光素子であって、第２導電型半導体層５より活性層４を貫通し第１導電型半導体層３に至る溝部６を備え、溝部６に第１電極７を設け、第２導電型半導体層５に第２電極８を設けるとともに、少なくとも、第１電極７と第２電極８との対向面に絶縁部９を備える。
【選択図】　図１



【特許請求の範囲】
【請求項1】
支持基板と、第１導電型半導体層と、発光層である活性層と、第２導電型半導体層とを順次積層して備えた半導体発光素子であって、
前記第２導電型半導体層より前記活性層を貫通し前記第１導電型半導体層に至る溝部を備え、
該溝部に第１電極を設け、前記第２導電型半導体層に第２電極を設けるとともに、
少なくとも、前記第１電極と前記第２電極との対向面に絶縁部を設けたことを特徴とする半導体発光素子。
【請求項2】
前記絶縁部を、少なくとも前記溝部の側面を覆うように設けた請求項１記載の半導体発光素子。
【請求項3】
前記溝部が、平面視においてクシ歯状である請求項１又は請求項２に記載の半導体発光素子。
【請求項4】
前記第１電極及び前記第２電極を構成する材料が、透光性を有する請求項１乃至請求項３のいずれかに記載の半導体発光素子。
【請求項5】
前記絶縁部は、表面に凹凸部を備えた請求項４に記載の半導体発光素子。

【発明の詳細な説明】
【０００１】
【発明の属する技術分野】
本発明は、半導体発光素子に関し、特に発光層に電圧印加するための電極をそれぞれ支持基板の同一面側において形成した構造を有する半導体発光素子に関するものである。
【０００２】
【従来の技術】
従来の半導体発光素子としては、例えば、図５に示すように、支持基板１であるサファイア基板の上に、バッファ層２であるＡｌＮと、ｎ型窒化ガリウム系化合物半導体からなるｎ層３と、発光層であり活性層である低キャリア濃度ｎ層４であるｎ－ＧａＮと、ｐ型窒化ガリウム系化合物半導体からなるｐ層５と、ｐ層５の上面からｎ層３に至るまで形成された溝５０と、ｐ層５の上面からｎ層３に至るまで形成された孔６０と、孔６０にｎ層３と接合しｐ層５の上面にまで形成された第１電極７と、ｐ層５の上面に溝５０によって第１電極７と電気的に絶縁分離されるように形成された第２電極８とを備えたものを挙げることができる（特許文献１参照。）。
【０００３】
上述の半導体発光素子は、溝５０により第１電極７と第２電極８との電気的な絶縁分離を実現しているので、半導体発光素子を順方向バイアスにする、つまり、第２電極８をプラス電圧にし第１電極７をマイナス電圧に印加することにより、第２電極８から第１電極７に向かって電流が流れ、ｐ層５とｎ層３の界面に位置する低キャリア濃度ｎ層４にてホールと電子が結合し発光する。
【０００４】
【特許文献１】
特許第２６９６０９５号公報
【０００５】
【発明が解決しようとする課題】
上述のような半導体発光素子においては、前述の溝により第１電極と第２電極との間の電気的な絶縁分離を実現されているため、溝を形成する分だけ、半導体発光素子全体に占める活性層の面積が制約を受けてしまい、単位電力あたりの発光効率が低下するという問題点があった。

【０００６】
本発明は上記問題点を改善するためになされたものであり、単位電力あたりの発光効率が向上するような半導体発光素子を提供することを目的とするものである。
【０００７】
【課題を解決するための手段】
上述の目的を達成するために、本発明の請求項１に係る半導体発光素子は、支持基板と、第１導電型半導体層と、発光層である活性層と、第２導電型半導体層とを順次積層して備えた半導体発光素子であって、前記第２導電型半導体層より前記活性層を貫通し前記第１導電型半導体層に至る溝部を備え、該溝部に第１電極を設け、前記第２導電型半導体層に第２電極を設けるとともに、少なくとも、前記第１電極と前記第２電極との対向面に絶縁部を設けている。
【０００８】
このような構成の半導体発光素子は、少なくとも前記第１電極と前記第２電極との対向面に前記絶縁部を設けることで、半導体発光素子全体に占める前記活性層の面積割合を大きくすることができ、単位電力あたりの発光効率が向上する。
【０００９】
また、本発明の請求項２に係る半導体発光素子は、請求項１に記載の半導体発光素子において、少なくとも前記溝部の側面を覆うように設けている。
【００１０】
このような構成の半導体発光素子は、少なくとも前記溝部の側面を覆うことで、前記第２電極から前記第１電極に向けて流れる漏れ電流の経路となりうる前記溝部の側面、つまり、前記溝部の前記活性層側及び前記第２導電型半導体層側に対して少なくとも前記絶縁部を形成して、漏れ電流の影響を取り除くことで、更に単位電力あたりの発光効率が向上する。
【００１１】
また、本発明の請求項３に係る半導体発光素子は、請求項１又は請求項２に記載の半導体発光素子において、前記溝部が平面視においてクシ歯状である。
【００１２】
このような構成の半導体発光素子は、溝部が平面視においてクシ歯状に形成することで、発光に寄与する活性層を流れる電流の均一化がされるので、更に単位電力あたりの発光効率が向上する。
【００１３】
また、本発明の請求項４に係る半導体発光素子は、請求項１乃至請求項３のいずれかに記載の半導体発光素子において、前記第１電極及び前記第２電極を構成する材料が透光性を有する。
【００１４】
このような構成の半導体発光素子は、第１電極及び第２電極を構成する材料が透光性を有することで、活性層より生じる光を半導体発光素子表面（上面）からも取り出せるようになるので、更に単位電力あたりの発光効率が向上する。
【００１５】
また、本発明の請求項５に係る半導体発光素子は、請求項４に記載の半導体発光素子において、前記絶縁部は、表面に凹凸部を備えている。
【００１６】
このような構成の半導体発光素子は、絶縁部が表面に凹凸部を備えることで、絶縁部の表面で全反射する光量が低減できるため、半導体発光素子表面（上面）からの光の取り出し効率が更に向上する。
【００１７】
【発明の実施の形態】
本発明の第１実施形態を図１、図２に基づいて説明する。図１は、本発明の第１実施形態に係る半導体発光素子を示す概略断面図であり、図２は、第１実施形態に係る半導体発光

素子の変形例を示す概略断面図である。

【００１８】

第１実施形態においては、半導体発光素子は、図１に示すように、支持基板１と、バッファ層２と、第１導電型半導体である第１導電型クラッド層３と、第１導電型クラッド層３と後述の第２導電型クラッド層５とに挟まれた発光半導体層であり低キャリア濃度ｎ層である活性層４と、第２導電型半導体である第２導電型クラッド層５とが順次積層された構成であり、第２導電型クラッド層５より活性層４を貫通し第１導電型クラッド層３に至る溝部６と、Ａｌで形成された第１電極７と、Ａｌで形成された第２電極８と、絶縁部９とを備えた構成である。

【００１９】

なお、半導体発光素子の上下方向は、実際の使用状態での方位性に依存するため一義的に規定できないが、第１実施形態の記述では説明の便宜上、図１、図２に示すように、支持基板１の配置側を下（下面）側、第２導電型クラッド層５の配置側を上（上面）側というように上下方向を規定するものとする。

【００２０】

ここで、第２電極８は、第２導電型クラッド層５の上面に接続されるように形成され、第２電極８の上面及び第２電極８の溝部６側の側面には、絶縁部９を備えている。つまり、第１実施形態においては、絶縁部９は、第１電極７と第２電極８とが直接的に面する対向面に形成されている。

【００２１】

また、第１電極７は、溝部６に対して、第１導電型クラッド層３の表面が露出した露出領域に接続され、この露出領域から第２電極８の側面に設けた絶縁部９、第２電極８の上面の一部にわたり形成されている。なお、絶縁部９は、第１電極７と第２電極８との間の電気的な絶縁分離を行うために、第１電極７と第２電極８との間に少なくとも設けられていればよい。

【００２２】

ここで、支持基板１は、例えば絶縁性のサファイア基板であり、第１導電型クラッド層３は、例えばｎ型ＡｌＧａＮのようなｎ型ＧａＮよりなる高キャリア濃度ｎ＋層であり、活性層４は、例えばｎ型ＩｎＧａＮのような３族窒化物半導体を用いて形成されたものである。また、第２導電型クラッド層５は、例えばｐ型ＡｌＧａＮのようなｐ型ＧａＮよりなる高キャリア濃度ｎ＋層であり、絶縁部９は、例えば絶縁膜であり、その材料は例えば、透明性を有しているSiO_2を用いる。なお、絶縁部９は、絶縁性を備えており、更に好ましくは透明性を有するものがであればよい。

【００２３】

また、バッファ層２は支持基板１と第１導電型クラッド層３との格子不整合を緩和するために設けられるもので、例えばＡｌＮ、ＧａＮ、ＡｌＧａＮにより形成される。なお、活性層４をｎ型ＩｎＧａＮで形成する場合には、活性層４の発光色は、Ｉｎの組成比を適宜調整したり、あるいはＳｉ、Ｇｅ、Ｓ等のｎ型不純物やＺｎ、Ｍｇ等のｐ型不純物を適宜ドープすることにより、紫外～赤色の範囲で所望の色に調節可能である。

【００２４】

なお、第１導電型クラッド層３の露出領域は、例えば第１導電型クラッド層３の全面に活性層４及び第２導電型クラッド層５を積層形成した後、活性層４及び第２導電型クラッド層５のうち露出領域相当箇所上部に積層されている部分を第１導電型クラッド層３が露出するまでエッチング除去することで形成することができる。なお、溝部６は、この第１導電型クラッド層３の露出領域を含み、活性層４、第２導電型クラッド層５のエッチング除去された箇所で構成されている。

【００２５】

第２電極８は、第２導電型クラッド層５の上に、後に第２電極８の側面に設ける絶縁部９相当箇所を考慮し、溝部６を取り囲むように形成される。そして、第２電極８の上面及び第２電極８の溝部６側の側面には、絶縁部９が形成される。

【００２６】
その後、第１導電型クラッド層３の露出領域から活性層４、第２導電型クラッド層５、第２電極８の溝部６側の側面に設けた絶縁部９、第２電極８の上面に設けた絶縁部９の一部にわたって、第１導電型クラッド層３に接続した第１電極７が形成される。
【００２７】
第１電極７及び第２電極８は、例えば所定のマスクを用いて形成することができるもので、両電極の材料としてはＡｌの他に、例えばＮｉ、Ａｕ、Ｔｉ等の金属を使用することができる。
【００２８】
なお、第１実施形態においても、半導体発光素子は、順方向バイアス、すなわちｐ型である第２導電型クラッド層５に形成した第２電極８にプラス電圧にし、第１電極７をマイナス電圧に印加することにより、活性層４にてホールと電子が結合し発光する。
【００２９】
かかる半導体発光素子においては、少なくとも、第１電極７と第２電極８との対向面に絶縁部９を設けることで、従来のように、第１電極７と第２電極８とを電気的に絶縁分離するための溝を形成する必要はなくなるので、半導体発光素子全体に占める活性層４の面積割合を大きくすることができ、単位電力あたりの発光効率が向上する。
【００３０】
ここで、第１実施形態における変形例として、第１電極７及び第２電極８の材料として、透光性を有する透明電極を用いてもよい。透明電極の材料としては、例えば、In_2O_3とSnO_2の複合化合物であるＩＴＯや、Cd_2SnO_4を用いることができる。
【００３１】
この場合、第１の電極７及び第２電極８に透明電極を用いることで、活性層４より生じる光を半導体発光素子表面（上面）からも取り出せるようにすることで、更に単位電力あたりの発光効率が向上する。また、半導体発光素子の両面、つまり、表面（上面）と裏面（下面）から光の取り出しが可能なフリップチップ実装との組み合わせにおいては、単位電力あたりの発光効率が向上する。
【００３２】
また、第１電極７及び第２電極８の材料として、透光性を有する透明電極を用いた場合に、図２に示すように、半導体発光素子の絶縁部９の表面に凹凸部９１設けた構成であってもよい。なお、凹凸部９１は、例えば、サンドブラスト法で形成することができる。なお、図２において、光の取り出しの様子は矢印で示している。
【００３３】
この場合、絶縁部９の表面に凹凸部９１設けることで、絶縁部９表面での全反射が抑制されるので、半導体発光素子表面（上面）からの光の取り出し効率が更に向上する。
【００３４】
なお、第１実施形態及びその変形例においては、漏れ電流の経路となる可能性がある活性層４及び第２導電型クラッド層５は、例えば数μｍレベルと非常に薄く、ハイインピーダンス状態となるため、第２電極８から第１電極７に向けて漏れ電流は、活性層４を流れる電流に比べ、ほとんどの場合において、無視できるレベルに制限される。
【００３５】
次に、第１実施形態における絶縁部９の形成箇所の変形例を示した実施形態を、本発明の第２実施形態として図３に基づいて説明する。図３は、本発明の第２実施形態に係る半導体発光素子を示す概略断面図である。なお、第１実施形態との同一箇所には同一符号を付して、共通部分の説明は省略する。
【００３６】
第２実施形態においては、半導体発光素子は、図３に示すように、絶縁部９が溝部６にける第１導電型クラッド層３の露出領域の一部まで拡大された構成であり、この点が、第１電極７と第２電極８とが直接的に面する対向面に絶縁部９を形成した第１実施形態の構成と異なる点である。

【００３７】
第２実施形態においては、絶縁部９は、溝部６の側面及び第１導電型クラッド層３の露出領域の一部まで形成されているが、少なくとも溝部６の側面を覆うように形成されていればよい。
【００３８】
かかる半導体発光素子においては、第２電極８から第１電極７に向けて流れる漏れ電流の経路となりうる溝部６の側面、つまり、溝部６の活性層４側及び第２導電型クラッド層５側に対して、少なくとも絶縁部９を形成して漏れ電流の影響を取り除くことで、単位電力あたりの発光効率が向上する。
【００３９】
次に、第１実施形態における溝部６をクシ歯状に形成した実施形態を、本発明の第３実施形態として図４に基づいて説明する。図４は、本発明の第３実施形態に係る半導体発光素子を示す平面図及び概略断面図である（図４（ａ）は、平面図であり、図４（ｂ）は、図４（ａ）のＸ－Ｘ断面における概略断面図であり、図４（ａ）においては、平面視における絶縁部９の段差部の図示は省略している）。なお、第１実施形態との同一箇所には同一符号を付して、共通部分の説明は省略する。
【００４０】
第３実施形態においては、半導体発光素子は、図４に示すように、平面視において例えば５つのクシ歯状になるように各溝部６を備え、その各溝部６に第１電極７を設けた構成である。なお、各第１電極７は、第１電極７と一体形成されたＡｌからなるクシ芯部７１により各々電気的に接続されている。
【００４１】
かかる半導体発光素子においては、溝部６を平面視においてクシ歯状に形成したすることにより、発光に寄与する活性層４を流れる電流が均一化されるため、更に単位電力あたりの発光効率が向上する。
【００４２】
ここで、第２実施形態における溝部６をクシ歯状に形成しても勿論よい。この場合も、同様に、活性層４を流れる電流が均一化されるため、更に単位電力あたりの発光効率が向上する。また、第２実施形態及び第３実施形態において、第１実施形態における変形例に示したように、第１電極７及び第２電極８の材料として、透光性を有する透明電極を用いてもよいし、更に絶縁部９の表面に凹凸部を設けた構成であってもよい。
【００４３】
【発明の効果】
以上説明したように、本発明の請求項１に係る半導体発光素子は、第２導電型半導体層より活性層を貫通し第１導電型半導体層に至る溝部に第１電極を設け、第２導電型半導体層に第２電極を設けるとともに、少なくとも、第１電極と第２電極との対向面に絶縁部を設けることで、半導体発光素子全体に占める活性層の面積割合を大きくすることができ、単位電力あたりの発光効率が向上する。
【００４４】
また、本発明の請求項２に係る半導体発光素子は、請求項１に記載の半導体発光素子の効果に加えて、第２電極から第１電極に向けて流れる漏れ電流の経路となりうる溝部の側面、つまり、溝部の活性層側及び第２導電型半導体層側に対して少なくとも絶縁部を形成して、漏れ電流の影響を取り除くことで、更に単位電力あたりの発光効率が向上する。
【００４５】
また、本発明の請求項３に係る半導体発光素子は、請求項１又は請求項２に記載の半導体発光素子の効果に加えて、溝部が平面視においてクシ歯状であることで、発光に寄与する活性層を流れる電流の均一化がされるので、更に単位電力あたりの発光効率が向上する。
【００４６】
また、本発明の請求項４に係る半導体発光素子は、請求項１乃至請求項３のいずれかに記載の半導体発光素子の効果に加えて、第１電極及び第２電極を構成する材料が透光性を有

することで、活性層より生じる光を半導体発光素子表面（上面）からも取り出せるようになるので、更に単位電力あたりの発光効率が向上する。また、半導体発光素子の両面、つまり、表面（上面）と裏面（下面）から光の取り出しが可能なフリップチップ実装との組み合わせにおいては、単位電力あたりの発光効率が向上する。

【００４７】

また、本発明の請求項５に係る半導体発光素子は、請求項４に記載の半導体発光素子の効果に加えて、絶縁部は、表面に凹凸部を備えることで、絶縁部の表面で全反射する光量が低減できるため、半導体発光素子表面（上面）からの光の取り出し効率が更に向上する。

【図面の簡単な説明】

【図１】本発明の第１実施形態に係る半導体発光素子を示す概略断面図である。

【図２】本発明の第１実施形態に係る半導体発光素子の変形例を示す概略断面図である。

【図３】本発明の第２実施形態に係る半導体発光素子を示す概略断面図である。

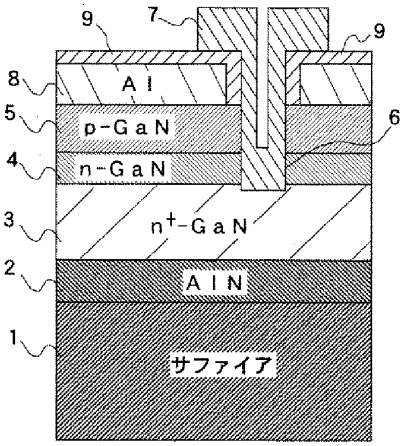
【図４】本発明の第３実施形態に係る半導体発光素子を示す平面図及び概略断面図である。

【図５】従来例に係る半導体発光素子を示す概略断面図である。

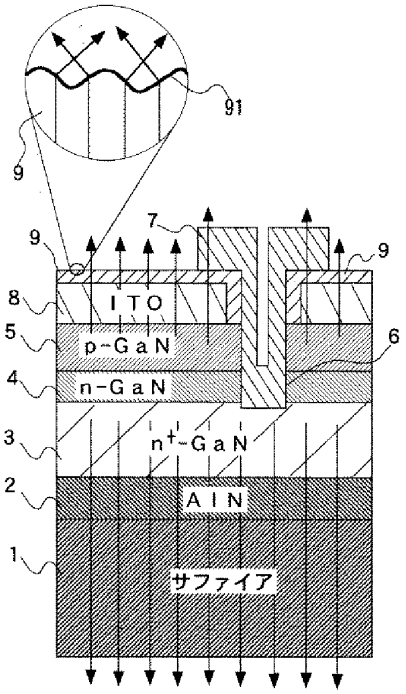
【符号の説明】

１　支持基板
２　バッファ層
３　第１導電型クラッド層
４　活性層
５　第２導電型クラッド層
６　溝部
７　第１電極
８　第２電極
９　絶縁部
９１　凹凸部

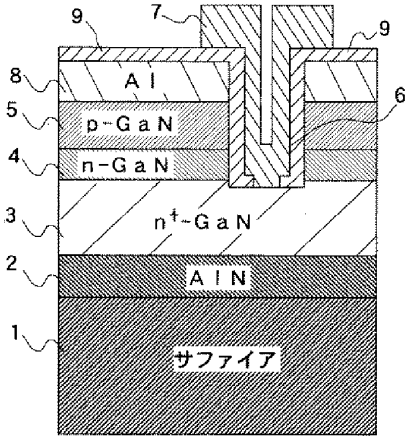
【図1】


9
7
9
8
Al
5
p-GaN
6
4
n-GaN
3
n+-GaN
2
AlN
1
サファイア

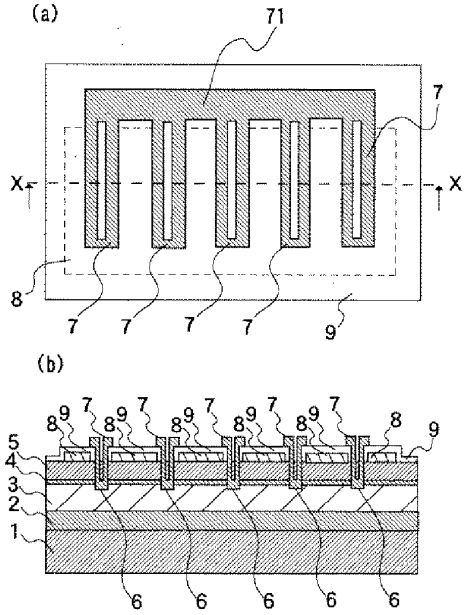
【図2】


91
9
7
9
9
8
ITO
5
p-GaN
6
4
n-GaN
3
n+-GaN
2
AlN
1
サファイア

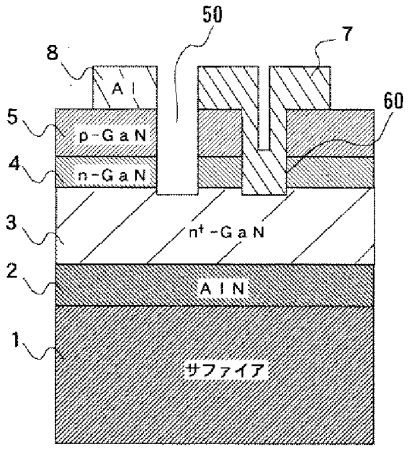
【図3】


9
7
9
8
Al
6
5
p-GaN
4
n-GaN
3
n+-GaN
2
AlN
1
サファイア

【図4】


(a)
71
7
X
X
8
7
7
7
7
9
(b)
8
9
7
5
4
3
2
1
6
6
6
6
6

【図5】



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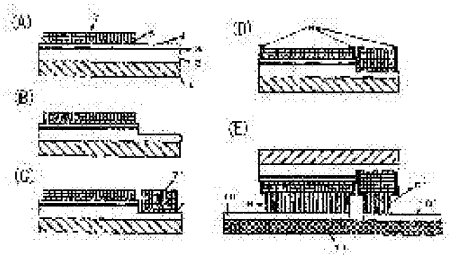
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(54) GALLIUM NITRIDE BASED COMPOUND SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a gallium nitride based compound semiconductor device capable of performing free process designing and having an optimum device property, and a manufacturing method of the device.
SOLUTION: As suitable materials, a Pt/Rh layer, a Pt/Ir layer or an Rh layer is used as an electrode for a p-type gallium nitride based compound semiconductor, and an Al/Rh layer, an Al/Ir layer, an Al/Pd layer or an Al/Pt layer is used as an electrode for an n-type gallium nitride based compound semiconductor. For this reason, different from any material in a conventional technology, ohmic contact can be obtained without performing annealing, and a good gallium nitride based device can be formed. Thereby, it becomes possible to perform this device process by using low heat-resistant materials. Furthermore, there can be obtained such useful effects as to avoid the deterioration of the device property caused by a thermal hysteresis of high temperature treatment and to reduce the number of processes.



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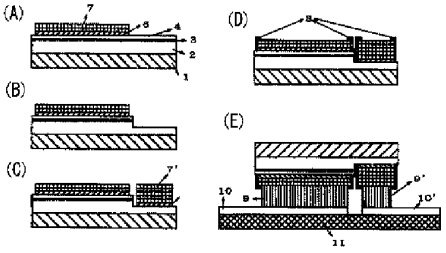
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(54)【発明の名称】窒化ガリウム系化合物半導体素子とその製造方法

(57)【要約】
【課題】　従来技術において、窒化ガリウム系化合物半導体上にオーミック電極を形成するためには４００℃以上のアニール処理が必須であったため、この処理によるデバイス特性の悪化やプロセス上の制約が生じていた。
【解決手段】　好適な材料としてｐ型窒化ガリウム系化合物半導体用電極としてＰｔ／Ｒｈ層，Ｐｔ／Ｉｒ層，又はＲｈ層を用い、ｎ型窒化ガリウム系化合物半導体用電極としてＡｌ／Ｒｈ層、Ａｌ／Ｉｒ層、Ａｌ／Ｐｄ層、又はＡｌ／Ｐｔ層を用いることで、従来技術にある如何なる材料とも異なり、アニール処理を行なうことなくオーミック接触を得ることができ、良好な窒化ガリウム系デバイスを形成することができる。これにより、低耐熱材料を使用して本デバイスプロセスを行なうことが可能となる。また高温処理の熱履歴によるデバイス特性の悪化の回避、工程数の削減、等有用な効果が得られる。
【選択図】　図１



【特許請求の範囲】
【請求項1】
窒化ガリウム系化合物半導体と、該窒化ガリウム系化合物半導体と接するように形成されかつオーミック接触する電極とを備えた窒化ガリウム系化合物半導体発光素子の製造方法であって、
基板上に窒化ガリウム系化合物半導体層を積層する工程と、
該窒化ガリウム系化合物半導体層の表面を露出させる工程と、
該窒化ガリウム系化合物半導体の露出表面を表面処理する工程と、
該処理表面上に窒化ガリウム系化合物半導体用電極を形成する工程を順に備え、
前記電極形成工程終了から窒化ガリウム系化合物半導体発光素子を当該素子搭載基板上に搭載する工程を行うまでの間において、オーミック接触を得るためのアニール処理を行わないことを特徴とする窒化ガリウム系化合物半導体発光素子の製造方法。
【請求項2】
前記窒化ガリウム系化合物半導体が、ｎ型窒化ガリウム系化合物半導体であることを特徴とする請求項１記載の窒化ガリウム系化合物半導体発光素子の製造方法。
【請求項3】
前記電極形成工程が、ｎ型窒化ガリウム系化合物半導体層上に厚さ１ｎｍ～１０ｎｍのＡｌ層を蒸着するサブ工程と、前記Ａｌ層上に形成されるＲｈ、Ｉｒ、Ｐｔ、Ｐｄからなる群から選択されるいずれかの金属層を蒸着するサブ工程を有し、前記オーミック接触を得るためのアニール処理を必要としないことを特徴とする請求項２に記載の窒化ガリウム系化合物半導体発光素子の製造方法。
【請求項4】
前記電極形成工程が、ｎ型窒化ガリウム系化合物半導体層上に形成される島状構造または網目状構造を有する厚さ１ｎｍ～１０ｎｍのＡｌ層を蒸着するサブ工程と、Ｒｈ、Ｉｒ、Ｐｔ、Ｐｄからなる群から選択されるいずれかの金属層を蒸着するサブ工程とを含み、サブ工程は同時にまたはＡｌ蒸着サブ工程に続いて金属蒸着サブ工程行う、前記オーミック接触を得るためのアニール処理を必要としないことを特徴とする請求項２に記載の窒化ガリウム系化合物半導体発光素子の製造方法。
【請求項5】
前記窒化ガリウム系化合物半導体が、ｐ型窒化ガリウム系化合物半導体であることを特徴とする請求項１記載の窒化ガリウム系化合物半導体発光素子の製造方法。
【請求項6】
ｐ型窒化ガリウム系化合物半導体層にオーミック接触するｐ型窒化ガリウム系化合物半導体用電極が、Ｐｄ、Ｐｔ、Ｒｈ、Ｐｔ／Ｒｈ、Ｐｔ／Ａｇ、Ｒｈ／Ａｇ、Ｐｄ／Ｒｈ、Ｐｄ／Ａｇ層からなる群から選択されるいずれかの層で構成されるとともに、前記オーミック接触を得るためのアニール処理を必要としないことを特徴とする請求項５に記載の窒化ガリウム系化合物半導体発光素子の製造方法。
【請求項7】
前記ｐ型窒化ガリウム系化合物半導体用電極がＰｔ／Ｒｈ、Ｐｔ／Ａｇのいずれかの層の場合において、前記Ｐｔ層の膜厚が０．３ｎｍ～１００ｎｍであり、及び／又は前記ＲｈもしくはＡｇ層の膜厚が５０ｎｍ～３００ｎｍであることを特徴とする請求項６に記載の窒化ガリウム系化合物半導体発光素子の製造方法。
【請求項8】
前記ｐ型窒化ガリウム系化合物半導体用電極がＰｄ，ＰｔまたはＲｈのいずれかの層の場合において、前記Ｐｄ、Ｐｔ、又はＲｈ層の膜厚が０．３ｎｍ～２００ｎｍであることを特徴とする請求項６に記載の窒化ガリウム系化合物半導体発光素子の製造方法。
【請求項9】
ｎ型窒化ガリウム系化合物半導体層およびｐ型窒化ガリウム系化合物半導体層を含むＩＩＩ族窒化物系化合物半導体積層構造と、ｎ型窒化ガリウム系化合物半導体層上に形成され

たｎ電極と、ｐ型窒化ガリウム系化合物半導体上に形成されたｐ電極とを備えたＩＩＩ族窒化物系化合物半導体発光素子であって、
　前記ｎ電極が、ｎ型窒化ガリウム系化合物半導体層と接する厚さ１ｎｍ～１０ｎｍのＡｌ層と、前記Ａｌ層上に形成されるＲｈ、Ｉｒ、Ｐｔ、Ｐｄからなる群から選択されるいずれかの金属層とからなり、アニール処理を施すことなくオーミック接触していることを特徴とするＩＩＩ族窒化物系化合物半導体発光素子。
【請求項10】
前記ｐ電極が、ｐ型窒化ガリウム系化合物半導体層と接するＰｄ、Ｐｔ、Ｒｈ、Ｐｔ／Ｒｈ、Ｐｔ／Ａｇ、Ｒｈ／Ａｇ、Ｐｄ／Ｒｈ、Ｐｄ／Ａｇ層からなる群から選択されるいずれかの層で構成され、厚みが２００ｎｍ以下であるとともに、アニール処理を施すことなくオーミック接触していることを特徴とする請求項９に記載のＩＩＩ族窒化物系化合物半導体発光素子。
【請求項11】
前記ｎ型またはｐ型窒化ガリウム系化合物半導体用電極上に、更に、共晶制限層および共晶材料層を積層してなる金属積層構造が形成されたことを特徴とする請求項９または１０に記載のＩＩＩ族窒化物系化合物半導体発光素子。
【請求項12】
前記共晶制限層は実質的にＡｇ又はＰｔで構成されており、且つ、前記共晶材料層はＡｕ，Ｓｎ，Ｉｎからなる群から選択される金属、またはこれらのうち少なくとも一つを含む合金で構成されていることを特徴とする請求項１１に記載のＩＩＩ族窒化物系化合物半導体発光素子。
【請求項13】
請求項９に記載のＩＩＩ族窒化物系化合物半導体発光素子であって、前記半導体層の側面が、前記基板の垂直方向に対して傾斜しているとともに、
　前記電極が、前記傾斜した側面に延在して形成されていることを特徴とする窒化ガリウム系化合物半導体デバイス。
【発明の詳細な説明】
【技術分野】
【0001】
　本発明は窒化ガリウム系化合物半導体を用いた素子に関する。より具体的には、窒化ガリウム系化合物半導体に最適な電極を有する素子および当該素子の製造方法（デバイスプロセス）に関する。
【背景技術】
【0002】
　従来の窒化ガリウム系化合物半導体発光素子を図６に示す。この発光素子はフリップチップ方式にて図示しない給電電極上に搭載する構成であり、電極面を下側として示している。この発光素子はサファイア基板１上にｎ型窒化ガリウム系化合物半導体層２（以後、ｎ型ＧａＮ層と記載）、活性層３、ｐ型窒化ガリウム系化合物半導体層４（以後、ｐ型ＧａＮ層と記載）がこの順で形成され、これらに対してｎ型窒化ガリウム系化合物半導体用電極５（以後、ｎ型ＧａＮ用電極と記載）と、ｐ型窒化ガリウム系化合物半導体用電極６（以後、ｐ型ＧａＮ用電極と記載）とを通じて電流を印可することで所定の波長の光を発することが可能である。ここで例示されている基板は、サファイア基板であるが、これに限定されず、ＳｉＣ基板やＳｉ基板に置き換えることができることは周知である。この基板上に、ＭＯＣＶＤ法等周知の技術により、窒化ガリウム系化合物半導体（ＡｌｘＩｎｙＧａ（１－ｘ－ｙ）Ｎ、０≦ｘ，ｙ≦１）薄膜を成膜することができる。
【0003】
　ここで、ｎ型ＧａＮ用電極５は一般にはＴｉ／Ａｌ、Ｖ／Ａｌ等の金属薄膜によって構成される。また、ｐ型ＧａＮ用電極６はＰｔ，またはＮｉ／Ａｕ等の金属薄膜によって構成されることが多い。以後、本明細書において「Ａ／Ｂ層」と表現した場合、より左に記載した材料Ａが半導体層側、より右に記載した材料Ｂが半導体層から離れた層側とする。また、フリップチップ方式で搭載する場合の光取り出し効率向上のために、ｎ型ＧａＮ用

電極５として反射率の高いＲｈ／Ａｌ層を用いてサファイア基板側において素子の発光を反射する技術や、同様にｐ型ＧａＮ用電極６として反射率の高いＲｈ／Ａｌ、Ａｇ等を用いる技術が知られている。なお図面において符号７、７で示すのは共晶電極である。

これらの従来の窒化ガリウム系化合物半導体発光素子とその製造方法については、特許文献１、特許文献２、特許文献３、特許文献４、特許文献５、特許文献６、特許文献７などが挙げられる。

【0004】

【特許文献1】特開平５－２１１３４７

【特許文献2】特開平１１－２２０１６８

【特許文献3】特開２００３－１１０１４０

【特許文献4】特開２００３－１１０１３８

【特許文献5】特開平５－２９１６２１

【特許文献6】特開２０００－３６６１９

【特許文献7】特開２０００－１８３４００

【発明の開示】

【発明が解決しようとする課題】

【0005】

特許文献１にはｉ層の窒化ガリウム系化合物半導体に接合する層をＮｉとした電極が開示されている。特許文献２にはフリップチップ型の窒化ガリウム系化合物半導体素子においてｐ型層と厚膜反射性電極層の間に薄膜金属層を設けることが開示される。特許文献３は窒化物半導体発光素子の光の取り出し効率を向上するために電極の所定の領域を高い反射率とすることを開示する。特許文献４は窒化物半導体発光ダイオードの外部量子効率を向上させるために透光性ｐ電極のシート抵抗と光の透過率との調和を図る旨を開示する。特許文献５にはｐ型不純物をドープした窒化ガリウム系化合物半導体とオーミック接触を得る材料としてＡｕ，Ｐｔ，Ａｇ，Ｎｉを使用すること、及びｎ型不純物をドープした窒化ガリウム系化合物半導体とオーミック接触を得る材料としてＡｌ，Ｃｒ，Ｔｉ，Ｉｎを使用することが開示されている。特許文献６はフリップチップ型の窒化ガリウム系化合物半導体素子においてｐ型層に接続される厚膜電極層をＡｇ，Ｒｈ，Ｒｕ，Ｐｔ，Ｐｄを用いて高反射率とすることが開示する。特許文献７にも同じくフリップチップ型の窒化ガリウム系化合物半導体素子においてｐ型層に接続される厚膜電極層を高反射率とすることが開示されている。

しかしながら、上に挙げた、従来のＧａＮ用電極は、半導体層とオーミック接触を得るために積極的なアニール処理を施さないことに関する知見は一切開示されていない。なぜならば窒化ガリウム系化合物半導体とオーミック接触を得るためにはいずれも４００℃以上のアニール処理を必要とするからである。このことは、以下のような幾つかの問題を引起す。

【0006】

（１）第１の問題点として、アニール炉における表面汚染と酸化が避けられないことが挙げられる。

【0007】

ＧａＮデバイスプロセスにおけるアニール処理の工程としてウェハに対してｉ）ｎ型ＧａＮ用電極形成－＞ アニール－＞ｐ型ＧａＮ用電極形成 －＞ アニールを順に行う工程（または、当該工程においてｐ型ＧａＮ用電極の形成とｎ型ＧａＮ用電極の形成順を逆にする）、あるいは、ｉｉ）ｎ型ＧａＮ用電極形成
－＞ ｐ型ＧａＮ用電極形成－＞アニールを順に行う工程（または、当該工程においてｐ型ＧａＮ用電極の形成とｎ型ＧａＮ用電極の形成順を逆にする）のいずれかが一般的である。

【0008】

ｉ）の工程の場合、ｎ型ＧａＮ用電極を先に形成して、オーミック接触を取るためにアニールを行うので、アニール時にはｐ型ＧａＮ用電極を形成するためのウェハ表面部分は

炉の雰囲気に直に曝されることになる。このため、この表面の炉内不純物による汚染や表面酸化が避けられず、その上にｐ型
ＧａＮ用電極を形成しても電気的特性は悪くなる。汚染や表面酸化を避けるために電極を形成するための表面を洗浄するとしても、既にｎ型ＧａＮ用電極が形成されているため、この材料が侵されるような洗浄プロセスを使うことはできず、洗浄は不完全にならざるを得ない。また、ｐ型ＧａＮ用電極を形成後にもやはりアニール処理が存在するため、ｎ型ＧａＮ用電極に余計な熱履歴を与えてしまい、結果として２回のアニール処理により電気特性が悪くなる。ｐ型ＧａＮ用電極形成を先にしてもやはり同様の問題がある。

【0009】

ｉｉ）の工程の場合、ｉ）の工程と違いアニール処理を１度で済ませるためｉ）の工程のような問題は存在しない。しかしながら、ｎ型ＧａＮ用電極またはｐ型ＧａＮ用電極のうち、温度、雰囲気、時間等のアニール条件がより過酷な条件を電極形成後のアニール処理条件として適用しなければならない。このため、より穏やかな条件で最適なオーミック特性が得られるはずの他方の電極の特性は、悪化せざるを得ない。

【0010】

ｎ型ＧａＮ用，ｐ型ＧａＮ用両電極を共通の材料と共通の条件でアニールできれば一度に蒸着とアニールとを行うことができるが、現在のところそのような材料は見つかっていない。

【0011】

例えば、ｎ型ＧａＮ用電極５が４００℃前後のアニール処理を必要とし、ｐ型ＧａＮ用電極６が７００℃前後のアニール処理を必要とする場合には、ｐ型ＧａＮ用電極６を先に形成しなければならない。なぜならｎ型ＧａＮ用電極５を先に形成した場合、同一ウェハに後から形成されたｐ型ＧａＮ用電極６のオーミック特性を得るために７００℃のアニール処理を経なければならないため、ｎ型ＧａＮ用電極５が過剰な熱を受け、電気特性が低下してしまうからである。

【0012】

（２）第２の問題点として、デバイスプロセスが制約されることが挙げられる。

【0013】

図６に示す共晶電極７、７は、Ｔｉ／Ａｕ／(Ｐｔ／Ａｕ）ｎ層やＮｉ／Ａｕ／(Ｐｔ／Ａｕ)ｎ層等の金属積層構造よりなる。共晶電極７、７'の最表面層に共晶材料層としてＡｕ層、その下に共晶制限層としてＰｔ層を用いている。これらを下にしてサブマウントや配線の側に積層したＡｕ／Ｓｎ共晶部に接続してフリップチップ接続する。接続の際には、共晶電極７、７'の最表面のＡｕ層とサブマウントの共晶部最表面のＡｕ層を接触させて３００℃程度の熱をかけることによってＡｕ／Ｓｎの共晶状態を作り出し、接合する。従って、上記のｎ型ＧａＮ用電極５を形成後に電極金属のオーミック接続を取るため４００℃以上のアニール処理を行う際に、もし成膜工程を続けて共晶電極７、７'まで成膜してしまうと、共晶用金属が融解して電極７、７'が機能しなくなってしまうことがある。故に、ｎ型ＧａＮ用，ｐ型ＧａＮ用両電極５，６を形成しアニールした後に、別工程で共晶電極７を形成しなければならない。なお、本明細書において、「（Ａ／Ｂ）ｎ層」といった表現は、材料Ａと材料Ｂとを繰り返してｎ回積層することを意味するものとする。

【0014】

一般にｎ型ＧａＮ用，ｐ型ＧａＮ用両電極とも過剰な温度によってアニールされると、半導体層側の金属層表面が荒れて反射率やオーミック特性が落ちるため好ましくない。特に、Ｐｔ，Ｒｈ，Ｐｄ等をＧａＮ系ＬＥＤ用ｐ型電極として用いた場合、熱処理によって立上り電圧（Ｖｆ）が０．０５～０．２Ｖ上昇してしまう。よって、余計なアニール処理は無い方が良い。

【0015】

このように、ウェハにかけるアニール処理の温度の高低によってデバイスプロセスの順番が決定されてしまう。あるいは、アニール処理の温度の最適化ができない。このことから必然的に、自由なデバイスプロセス設計ができない、デバイス特性を最適なものにでき

ないという問題が生じる。

本発明は、上に挙げた問題点に鑑み、自由なプロセス設計が可能であるとともに最適なデバイス特性を有する窒化ガリウム系化合物半導体素子、及びその製造方法を提供することを目的とする。

【課題を解決するための手段】

【0016】

上述の目的を達成するため、本発明は、ＧａＮ系化合物半導体デバイスプロセスにおいて、所定の積層構造電極を半導体用電極に用いることによりｎ型ＧａＮ用電極形成、ｐ型 ＧａＮ用電極形成、共晶電極形成のいずれのプロセスにおいても積極的にアニール処理を施すことを必要としないデバイスを形成する。

本発明は、窒化ガリウム系化合物半導体と、該窒化ガリウム系化合物半導体と接するように形成されかつオーミック接触する電極とを備えた窒化ガリウム系化合物半導体発光素子の製造方法を提供するものであって、

基板上に窒化ガリウム系化合物半導体層を積層する工程と、

該窒化ガリウム系化合物半導体層の表面を露出させる工程と、

該窒化ガリウム系化合物半導体の露出表面を表面処理する工程と、

該処理表面上に窒化ガリウム系化合物半導体用電極を形成する工程を順に備え、

前記電極形成工程終了から窒化ガリウム系化合物半導体発光素子を当該素子搭載基板上に搭載する工程を行うまでの間において、オーミック接触を得るためのアニール処理を行わないことを特徴とする窒化ガリウム系化合物半導体発光素子の製造方法である（請求項１）。

ここで、窒化ガリウム系化合物半導体は、ｎ型窒化ガリウム系化合物半導体及びｐ型窒化ガリウム系化合物半導体のいずれかであることが好ましい（請求項２，５）。

ｎ型ＧａＮ半導体の場合、前記電極形成工程が、ｎ型窒化ガリウム系化合物半導体層上に厚さ１ｎｍ～１０ｎｍのＡｌ層を蒸着するサブ工程と、前記Ａｌ層上に形成されるＲｈ、Ｉｒ、Ｐｔ、Ｐｄからなる群から選択されるいずれかの金属層を蒸着するサブ工程を有することが好ましい（請求項３）。あるいは前記電極形成工程が、ｎ型窒化ガリウム系化合物半導体層上に形成される島状構造または網目状構造を有する厚さ１ｎｍ～１０ｎｍのＡｌ層を蒸着するサブ工程と、Ｒｈ、Ｉｒ、Ｐｔ、Ｐｄからなる群から選択されるいずれかの金属層を蒸着するサブ工程とを含み、サブ工程は同時にまたはＡｌ蒸着サブ工程に続いて金属蒸着サブ工程行うことが好ましい（請求項４）。

【0017】

より具体的には、好適な材料としてｐ型ＧａＮ用電極としてＰｔ／Ｒｈ層またはＰｔ／Ａｇ層を用い、ｎ型ＧａＮ用電極としてＡｌ／Ｒｈ層、Ａｌ／Ｉｒ層、Ａｌ／Ｐｄ層、又はＡｌ／Ｐｔ層を用いる。これによりアニールを行わずにＧａＮデバイスを形成することができる。これらの材料は従来技術にある如何なる材料とも違って、アニールを行わずに良好なオーミック特性を達成し得るのである。

【0018】

従来、Ａｌ単体でｎ型ＧａＮ用電極を形成できることは知られていたが、オーミック特性が悪く、また、アニール処理を経なければオーミック接触にならなかった。また、Ｒｈ，Ｐｄ，Ｉｒ，Ｐｔなどの金属ではｎ型窒化ガリウム系化合物半導体に対してオーミック接触が得られなかった。しかし、本発明者等の研究の結果、これらの材料の組合せによってアニール処理を行わずにｎ型窒化ガリウム系化合物半導体に対して良好なオーミック特性が得られることが判った。

図３はＡｌ／Ｉｒ層電極およびＡｌ／Ｐｄ層電極の接触抵抗値のアニール温度依存性を示す。なお、Ａｌ層の膜厚は３ｎｍ、Ｉｒ層またはＰｄ層の膜厚は１００ｎｍとし、真空蒸着法にてキャリア密度１×１０１８台のｎ型ＧａＮ層上に形成した。膜厚は水晶振動子を用いて蒸着厚をモニターして厚みを制御した。このようにして作製したｎ型ＧａＮ用電極を窒素雰囲気とした所定温度の電気炉内において２０秒間のアニール処理を実施した。接触抵抗率は４探針法（Transmission line model）により測定した。また、Ａｌ／Ｐｄ

の代わりにＡｌ／Ｒｈを同一条件で作成した場合Ａｌ／Ｐｄとほぼ同一であった。

ｎ型ＧａＮ層のドーピング濃度がさほど高いウェハを用いてはいないが、それでも常温において１０－６ｃｍ２台のオーミック特性が得られることが分かる。オーミック特性を得られる理由の詳細は不明であるが、本発明者等の研究により次のように考え得る。

【0019】

Ｒｈ，Ｐｄ，Ｉｒ，Ｐｔは周期律表においてＶＩＩＩ族第５，６周期の元素であって、且つその結晶はｆｃｃ構造をとることが知られている。また、格子定数の値はそれぞれＲｈは３８０．３ｐｍ，Ｐｄは３８９．０ｐｍ，Ｉｒは３８３．９４ｐｍ，Ｐｔは３９２．３ｐｍである。ここで、Ａｌはやはりｆｃｃ構造を取り、しかもその格子定数はａ＝４０４．９６ｐｍであって前記４種の金属と５％前後大きいだけである。従って、ＡｌとＲｈ等を積層した場合、相互に格子間に原子が入り込んで金属間化合物のようなものを形成し、何らかの原子間相互作用が起こるものと思われる。

また、１層目の電極材料であるＡｌと２層目の電極材料である金属元素とは原子半径が異なる。１層目の材料に２層目の電極材料に比べて原子半径の小さなＡｌを用いることで、密着性が向上しているものと推定される。

【0020】

上記のような相互作用がｎ型ＧａＮ層表面から深さ１０ｎｍ以内の領域で起こることで、半導体層／電極金属間のオーミック特性に好ましい影響を与えているものと思われる。このことは、本発明者等の実験によって確認することができた。

Ａｌ／Ｒｈ層においてＲｈ層の厚みを１００ｎｍと一定にし、Ａｌ薄膜の厚みを変えて評価した結果、Ａｌ薄膜が１０ｎｍ未満においては良好なオーミック特性が得られた。なお、この検討の際にアニール処理は実施していない。

Ａｌ薄膜の膜厚が２０ｎｍを超えるとＡｌ単層の厚膜（１００ｎｍ）をｎ型ＧａＮ層上に形成し、且つアニール処理を施した場合のオーミック特性とほぼ同等であった。即ち、Ａｌ／Ｒｈ、Ａｌ／Ｉｒ等の金属層によってｎ型ＧａＮ層とオーミック接触を得る場合、半導体層上に直接に形成する層であるＡｌ薄膜の膜厚が１０ｎｍより大きくなるとオーミック特性が急激に悪化する。本発明においてＡｌ薄膜の膜厚の望ましい範囲は１ｎｍ～１０ｎｍであり、薄膜形成時の膜厚制御性を考えるとより望ましくは１ｎｍ～５ｎｍであり、更に望ましくは２ｎｍ～４ｎｍである。また、１ｎｍより薄くなっても良好なオーミック特性が得にくくなる。

【0021】

Ａｌ層の構造については「薄膜」と定義したが、島状構造や網目構造なども同様の効果を奏するため、この「薄膜」にはこれらの構造も含む。また、ＡｌとＲｈ等の同時蒸着等何らかの手法によりＡｌ－Ｒｈ等の合金層を電極として形成した場合も同じようにアニール処理なしでオーミック接触が得られる。本発明の要点は、ＡｌとＲｈ等金属の相互作用がｎ型ＧａＮ層表面近傍で得られることによってオーミック接触が達成される点にあり、本要点を変更しない範囲で様々な応用が考えられる。

Ａｌ　３ｎｍ／Ｒｈ　１００ｎｍのＮ電極を用いて、アニール処理を行わないものと、同じ電極で５００℃のアニール処理を施したものについて取出し効率を測定したところ、アニール処理を施すことにより反射率が約２～３％低下した。また、表面反射率も低下していた。この原因はＡｌとＲｈの粒界が大きくなること、およびＡｌとｎ型ＧａＮ層の界面において拡散することが主な原因と考えられる。

なお、特許文献２には窒化ガリウム系化合物半導体とオーミック接触を得る電極材料としてＡｌも例示されている。しかしながら、Ｃｒ電極に比べるとオーミック特性が悪いことを開示するものの、積極的にアニール処理を施さない旨の記載はない。さらに、好適な厚みとしてｐ電極であるＮｉとして０．０１～０．５ミクロンとすることおよびＡｌ電極単独であることは開示するものの、半導体層と接するＡｌ層の膜厚を１０ｎｍ以下とすると積極的なアニール処理を施すことなくＡｌ単層膜に比べてオーミック特性が優れることについては一切記載されていない。

【0022】

ｐ型ＧａＮ用電極についても、ｐ型ＧａＮ層表面にＲｈまたはＰｄ，Ｐｔ，Ｐｔ／Ｒｈ，Ｐｔ／Ａｇ，Ｒｈ／Ａｇ，Ｐｄ／Ｒｈ，Ｐｄ／Ａｇ層を形成することによって、アニール処理なしでオーミック接触をなす電極が得られる（請求項６）。この時、Ｐｔ層の膜厚が０．３ｎｍ～１００ｎｍであり、及び／又は前記ＲｈもしくはＡｇ層の膜厚が５０ｎｍ～３００ｎｍであることが好ましい（請求項７）あるいは、前記Ｐｄ、Ｐｔ、又はＲｈ層の膜厚が０．３ｎｍ～２００ｎｍであることであることが好ましい（請求項８）。

これら電極の接触抵抗値のアニール温度依存性について図４に示す。

図４はＲｈ単層電極およびＰｔ／Ｒｈ層電極の接触抵抗値のアニール温度依存性を示す。なお、Ｒｈ層の膜厚は１００ｎｍ、Ｐｔ層の膜厚は１ｎｍとし、ｐ型ＧａＮ層上に真空蒸着法で形成した。膜厚は水晶振動子を用いて蒸着厚をモニターして厚みを制御した。このようにして作製したｐ型ＧａＮ用電極を窒素雰囲気とした所定温度の電気炉内において２０秒間のアニール処理を実施した。接触抵抗率は４探針法（Transmission line model）により測定した。

常温において１０－４ｃｍ２台のオーミック特性が得られることが分かる。

【0023】

これらの電極材料は、従来、アニール処理無しではオーミック接触を形成しないか、著しく抵抗が高いと思われていた。しかし、本発明者等の研究によって、アニール処理無しで実用的なほど低抵抗のｐ型ＧａＮ用電極を得ることができることが明らかになった。この場合、表面処理、特に、特開２０００－１０１１３４号公報にある脱酸素作用を有する液体、例えば王水による表面処理をｐ型ＧａＮ層表面に、電極層形成直前に行うことにより、アニール処理無しで極めて接触抵抗の低い、且つ密着性に優れたｐ型ＧａＮ用電極を得ることができた。ｐ型電極としてＰｄ、ＰｔまたはＲｈのいずれかの層を形成する場合には０．３～２００ｎｍが好適である。これより薄いと反射率が低下し、厚いと応力の問題が顕在化してくるからである。また、Ｐｔ／ＲｈまたはＰｔ／Ａｇの場合にも同様の理由によりＰｔ層の膜厚を０．３～１００ｎｍおよび／またはＡｇ層の膜厚を５０～３００ｎｍとすると良い。

【0024】

サファイア基板側を光取出し面とするフリップチップ型の実装方式を採る場合、ｐ型ＧａＮ用電極の発光波長に対する反射率はより高いほうが望ましい。しかし、アニール処理を経ることによって一般的には電極金属の反射率は低下する。熱を受けたことによって、半導体層／電極金属界面が荒れるからである。そこで、本発明の製造方法を用いれば、アニール処理を行わないため、電極金属の高い反射率をそのまま活かすことができ、光取り出し効率の上昇に大きく寄与する。

また本発明は、ｎ型窒化ガリウム系化合物半導体層およびｐ型窒化ガリウム系化合物半導体層を含むＩＩＩ族窒化物系化合物半導体積層構造と、ｎ型窒化ガリウム系化合物半導体層上に形成されたｎ電極と、ｐ型窒化ガリウム系化合物半導体上に形成されたｐ電極とを備えたＩＩＩ族窒化物系化合物半導体発光素子を提供するものであって、

前記ｎ電極が、ｎ型窒化ガリウム系化合物半導体層と接する厚さ１ｎｍ～１０ｎｍのＡｌ層と、前記Ａｌ層上に形成されるＲｈ、Ｉｒ、Ｐｔ、Ｐｄからなる群から選択されるいずれかの金属層とからなり、アニール処理を施すことなくオーミック接触していることを特徴とするＩＩＩ族窒化物系化合物半導体発光素子である（請求項９）。

この場合に、前記ｐ電極が、ｐ型窒化ガリウム系化合物半導体層と接するＰｄ、Ｐｔ、Ｒｈ、Ｐｔ／Ｒｈ、Ｐｔ／Ａｇ、Ｒｈ／Ａｇ、Ｐｄ／Ｒｈ、Ｐｄ／Ａｇ層からなる群から選択されるいずれかの層で構成され、厚みが２００ｎｍ以下であるとともに、アニール処理を施すことなくオーミック接触していることが好ましい（請求項１０）。

また、前記ｎ型またはｐ型窒化ガリウム系化合物半導体用電極上に、更に、共晶制限層および共晶材料層を積層してなる金属積層構造が形成されたることが好ましい（請求項１１）。

この場合、前記共晶制限層は実質的にＡｇ又はＰｔで構成されており、且つ、前記共晶材料層はＡｕ，Ｓｎ，Ｉｎからなる群から選択される金属、またはこれらのうち少なくと

も一つを含む合金で構成されていることが好ましい（請求項１２）。
　また本発明は、前記ＩＩＩ族窒化物系化合物半導体発光素子であって、前記半導体層の側面が、前記基板の垂直方向に対して傾斜しているとともに、
　前記電極が、前記傾斜した側面に延在して形成されていることを特徴とする窒化ガリウム系化合物半導体デバイスを提供する（請求項１３）。
【発明の効果】
【0025】
　本発明により、ＧａＮ系デバイスの電極を形成するにあたってアニール処理が不要となる。そのため、ウェハに不要な熱履歴が蓄積せず、電極のオーミック特性や反射率がプロセスにおいて劣化しないという効果がある。また、ｎ型又はｐ型ＧａＮ用電極の形成後、蒸着用真空装置から出さずに続けてＡｕ／Ｓｎ積層構造等の共晶電極を積層できるため、デバイスプロセスに要する総合的な時間を著しく短縮できる。また、蒸着真空装置から取り出すことがないためｐ型もしくはｎ型ＧａＮ用電極の汚染や表面酸化を防止することができる。また、蒸着回数が少なくて済む。さらに、プロセス設計にあたって熱に弱い有機材料が使用し得るなどの自由度が大きくなるという利点がある。
　また、アニール処理を行うと、ＧａＮ層と電極材料間の熱膨張係数の相違による応力がかかるが、本発明においては電極材料に与える熱履歴が少なくなるので応力の蓄積が著しく小さくなるため、電極の剥離が抑制され信頼性が向上する。
　特にボンディングパッド部を除く電極層の総厚みを２００ｎｍ以下とすると、剥離が殆ど発生せずに好適である。
　従って、本発明はＧａＮ系デバイス製造にあたって非常に優れた工業的価値を持つことが明らかである。なお、ＧａＮ層にて説明したが、ＡｌＧａＩｎＮ、ＡｌＧａＮ、ＩｎＧａＮ層などの窒化ガリウム系化合物半導体の場合も同様であろう。
【発明を実施するための最良の形態】
【0026】
　以下に本発明の２つの実施例を示す。両実施例ともフリップチップ方式の実装方法を前提としているが、半導体面側を光取出し面とするフェイスアップ方式であっても本発明は当然適用可能である。本実施例は発明者らが本発明の効果を確認するために行った実験のうちの幾例かを挙げたに過ぎず、本発明は実施例に限定して解釈されるべきではない。
【実施例】
【0027】
　ＭＯＣＶＤ法によってサファイア基板１上にバッファ層を介してシリコン（Ｓｉ）ドープのｎ型ＧａＮ層２、窒化ガリウムアルミインジウム系化合物からなる活性層３、マグネシウム（Ｍｇ）をドープしたｐ型ＧａＮ層４を含むデバイスウェハを得た。次いで、このウェハを以下に示すプロセスで加工した。この工程について図１を参照して説明する。
【0028】
　（１）ウェハを液温２０℃の王水（体積比で濃硝酸１：濃塩酸３）中に５分間浸漬洗浄、超純水リンスを施す表面処理工程を行ないｐ型ＧａＮ層４表面を清浄化した。その後、その表面に電子線加熱蒸着法によりｐ型ＧａＮ用電極６としてＰｔ１ｎｍ／Ｒｈ １００ｎｍを形成し、連続して共晶電極７としてＴｉ１００ｎｍ／(Ｐｔ １００ｎｍ／Ａｕ２００ｎｍ)２を形成し、その一部を除去した。（図１（Ａ）参照）
【0029】
　（２）ｐ型ＧａＮ層４の一部を周知の技術である反応性イオンエッチング法によってエッチングして、ｎ型ＧａＮ層２を部分的に露出させた。（図１（Ｂ）参照）
【0030】
　（３）露出したｎ型ＧａＮ層２表面の一部に、フォトリソグラフィと電子線加熱蒸着法とによりｎ型ＧａＮ用電極５としてＡｌ
３ｎｍ／Ｒｈ １００ｎｍを形成し、連続して共晶電極７'としてＴｉ １００ｎｍ／Ｐｔ １００ｎｍ／Ａｕ１００ｎｍ～１０００ｎｍ／Ｐｔ １００ｎｍ／Ａｕ２００ｎｍ（下層側のＡｕ層厚は設計上可変）を形成した。（図１（Ｃ）参照）

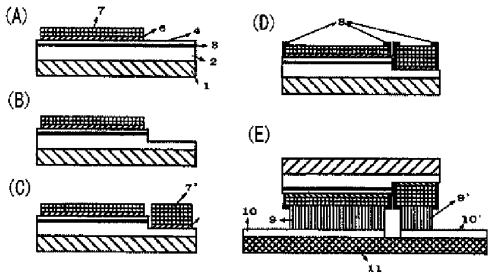
【0031】
（４）周知の技術によって、共晶電極部分を除くウェハ表面をＳｉＯ２膜８で被覆し、また、デバイス毎にウェハをカットした。（図１（Ｄ）参照）
【0032】
（５）デバイスの共晶電極部分７，７’と、別に構成したサブマウント１１の共晶部９，９’と合わせ、３００℃程度の熱圧着によってサブマウント１１にデバイスを接合した。（図１（Ｅ）参照）
【0033】
従来技術において、デバイスプロセスはｎ型ＧａＮ用電極、ｎ型ＧａＮ用電極上部共晶電極、ｐ型ＧａＮ用電極、ｐ型ＧａＮ用電極上部共晶電極の電極等を表面に形成するために、フォトリソグラフィによるパターニングと電子線加熱蒸着法による電極材料の積層工程を、４回繰り返す必要があった。しかし、本発明においては、ｎ型ＧａＮ用電極とｎ型ＧａＮ用電極上部共晶電極を続けて１回の工程で形成することができ、またｐ型ＧａＮ用電極とｐ型ＧａＮ用電極上部共晶電極を続けて１回の工程で形成することができる。すなわち、合計として２回の工程で済ませることができ、大変経済性がよい。また、デバイスの熱履歴は最高で３００℃であり、これによりデバイスの熱による劣化を抑えることができる。
【実施例】
【0034】
図２及び以下に示すデバイスプロセスにおいて、実施例１と同じウェハに対してｎ型ＧａＮ用電極を先に形成した。
【0035】
（１）ｐ型ＧａＮ層４の一部を周知の技術である反応性イオンエッチングによってエッチングして、ｎ型ＧａＮ層２を部分的に露出させた。この際、ＧａＮ層２，３，４の側面をウェハ底面となす角が４５°前後になるように傾斜させた。（図２（Ａ）参照）
【0036】
（２）露出したｎ型ＧａＮ層２表面および傾斜した側面に、フォトリソグラフィと電子線加熱蒸着法とによりｎ型ＧａＮ用電極５としてＡｌ３ｎｍ／Ｉｒ １００ｎｍを形成し、連続して共晶電極’としてＮｉ １００ｎｍ／Ｐｔ １００ｎｍ／Ａｕ １００ｎｍ／(Ｐｔ１００ｎｍ／Ａｕ ２００ｎｍ)２（下層側のＡｕ層厚は設計上可変）を形成した。（図２（Ｂ）参照）
【0037】
（３）ｐ型ＧａＮ層４表面の一部にフォトリソグラフィと電子線加熱蒸着法とによりｐ型ＧａＮ用電極６としてＰｔ１ｎｍ／Ａｇ １００ｎｍを形成し、連続して共晶電極７としてＮｉ１００ｎｍ／Ｐｔ １００ｎｍ／Ａｕ １００～１０００ｎｍ／Ｐｔ １００ｎｍ／Ａｕ２００ｎｍを形成した。（図２（Ｃ）参照）
【0038】
（４）周知の技術によって、共晶電極部分を除くウェハ表面をＳｉＯ２膜８で被覆し、また、デバイス毎にウェハをカットした。（図２（Ｄ）参照）
【0039】
（５）デバイスの共晶電極部分７，７’と、別に構成したサブマウント１１の共晶反応部分９，９’と合わせ、３００℃程度の熱圧着によってサブマウント１１にデバイスを接合した。（図２（Ｅ）参照）
【0040】
ＧａＮ層の側面を傾斜させ、その側面に延在させてｐ型および／又はｎ型ＧａＮ用電極を形成することは、層内を伝播する光を傾斜端面において透光性基板側に反射するので各層に対してほぼ垂直な端面を有する場合に比べて光取り出し効率が向上する。よって光の取り出し効率の観点から、特にフリップチップ方式を用いて実装する場合に有効な方法である。また、本発明によるこのような構成としたことで、電極形成工程において副次的に次のような効果がある。

【0041】
傾斜した側面に電極を形成し、従来の方法のようにアニールを行うと、図５の１２に示すように電極金属がだれることがある。電極層が厚くなれば大きくだれてしまい、これにより電極の短絡などの問題になりかねない。しかし、本発明においては電極に対してアニールを行なわないため、このような電極だれの問題は発生しなくなり、デバイス製造時の信頼性向上に著しい効果がある。
【0042】
なお、実施例１ではｎ型ＧａＮ用電極としてＡｌ
３ｎｍ／Ｒｈ　１００ｎｍ、ｐ型ＧａＮ用電極としてＰｔ
１ｎｍ／Ｒｈ　１００ｎｍを用い、実施例２ではｎ型ＧａＮ用電極としてＡｌ
３ｎｍ／Ｉｒ　１００ｎｍ、ｐ型ＧａＮ用電極としてＰｔ
１ｎｍ／Ａｇ　１００ｎｍを用いた。しかし、ｎ型ＧａＮ用電極としてはＡｌ／Ｒｈ，Ａｌ／Ｉｒ以外にもＡｌ／Ｐｄ，Ａｌ／Ｐｔを使用することが可能であり、また、ｐ型ＧａＮ用電極としてＰｔ／Ｒｈ，Ｐｔ／Ａｇ以外にもＲｈを使用することができることは言うまでもない。
【0043】
実施例においては、共晶電極接着のため共晶電極としてＡｕを用いた場合には３００℃程度以下の加熱で接合することができるので、３００℃より高い温度がかかることはない。これに対し、従来技術における電極のアニール処理では少なくとも４００℃以上の温度で加熱が複数回行なわれ、その温度差は少なくとも１００℃以上ある。熱がデバイスに及ぼす悪影響は、温度に対して指数関数的に大きくなる性質があるから、この１００℃の差のアニール処理が複数回行なわれるによってデバイスの性能は本発明によるデバイス性能と相当に違ってくる。共晶電極の材料を最適に選択することで、本発明のデバイスに対する最終的な熱履歴は更に減らすことができる。特に、上記したフリップチップ型の実装方式を採用する場合において、共晶電極層／共晶制限層からなる共晶電極を窒化ガリウム用電極上に形成し、共晶電極層として、Ａｕ，Ｓｎ，Ｉｎからなる群れから選択される金属、またはこれらのうちの少なくとも一つを含む合金、特にＡｕもしくはＡｕを含む合金で構成した場合には、共晶接続を行う際の熱の影響を小さくすることができ好適である。また、共晶制限層としてＡｇまたはＰｔを用いた場合には積極的なアニール処理を施さない電極を用い且つ共晶電極層としてＡｕ、Ｓｎ，Ｉｎを用いた場合において、共晶電極層材料の窒化ガリウム層もしくは該層用電極への拡散を効果的に抑止することができる。共晶電極層／共晶制限層を複数回積層した場合にはより効果的となる。各層の膜厚は好ましくは５０ｎｍ～２０００ｎｍであり、前記ｎ型またはｐ型窒化ガリウム系化合物半導体用電極と前記共晶電極との間にＴｉ層またはＮｉ層が挿入すると、より拡散を抑止することができ得る。
また、フェイスアップ方式の実装方法で、共晶電極を全く使用しないならば、実装に至るまで事実上全く熱処理工程を含まないデバイスプロセスが本発明によって実現可能である。
【図面の簡単な説明】
【0044】
【図1】（A）から（E）は本発明による窒化ガリウム系化合物半導体ウェハプロセスの一実施態様である。
【図2】（A）から（E）は本発明による窒化ガリウム系化合物半導体ウェハプロセスの他の実施態様である。
【図3】本発明によるｎ型窒化ガリウム系化合物半導体用電極の接触抵抗値のアニール温度依存性を示す図である。
【図4】本発明によるｐ型窒化ガリウム系化合物半導体用電極の接触抵抗値のアニール温度依存性を示す図である。
【図5】従来技術によるアニール処理において起こる電極のだれについて示した図である。

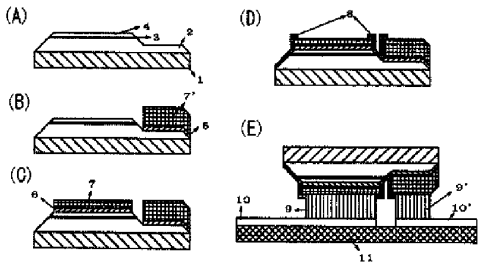
【図6】従来技術による窒化ガリウム系化合物半導体デバイスについて示した図である。
【符号の説明】
【0045】

１	サファイア基板
２	ｎ型窒化ガリウム系化合物半導体層
３	活性層
４	ｐ型窒化ガリウム系化合物半導体層
５	ｎ型窒化ガリウム系化合物半導体用電極
６	ｐ型窒化ガリウム系化合物半導体用電極
７，７’	共晶電極
８	ＳｉＯ２膜
９，９’	サブマウント側共晶部
１０，１０’	サブマウント側配線部
１１	サブマウント基板
１２	電極だれ

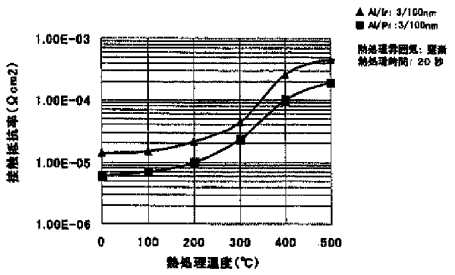
【図1】



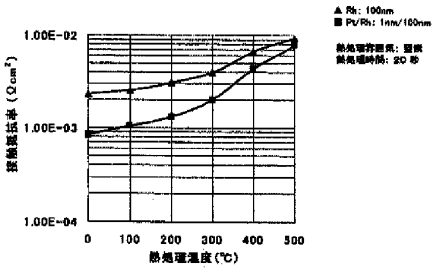
【図2】



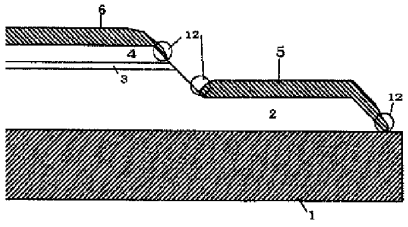
【図3】



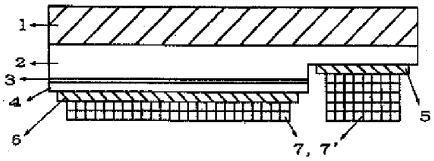
【図4】



【図5】



【図6】



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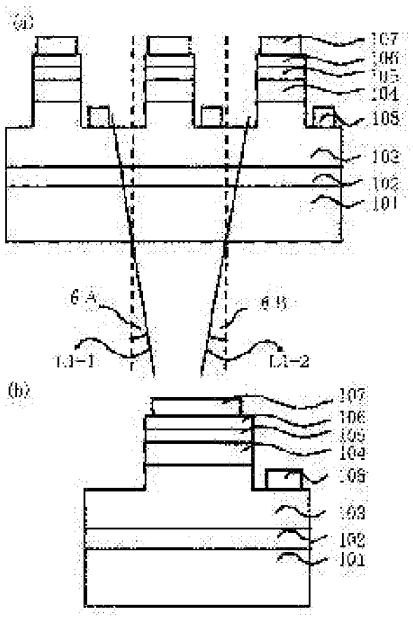
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(54) NITRIDE SEMICONDUCTOR LIGHT-EMITTING DIODE CHIP AND ITS MANUFACTURING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a nitride semiconductor light-emitting diode chip with the light extraction efficiency is improved.
SOLUTION: The nitride-semiconductor light-emitting diode chip includes a light-transmitting substrate (101) and a nitride-semiconductor laminated structure (102 to 106) formed on the top face of the substrate (101). The nitride-semiconductor laminated structure includes a light-emitting layer (104) and a plurality of other semiconductor layers. The substrate (101) does not depend on the face azimuth and has a thickness of 120 μm or larger. Consequently, the extraction efficiency of a light from the chip is improved. At least one of the parting faces of the chip is inclined to a surface orthogonal with respect to a substrate surface, and the underside of the substrate also has an area smaller than that of the upper-side region of the nitride-semiconductor laminated structure, thus improving the extraction efficiency of the light from the chip.



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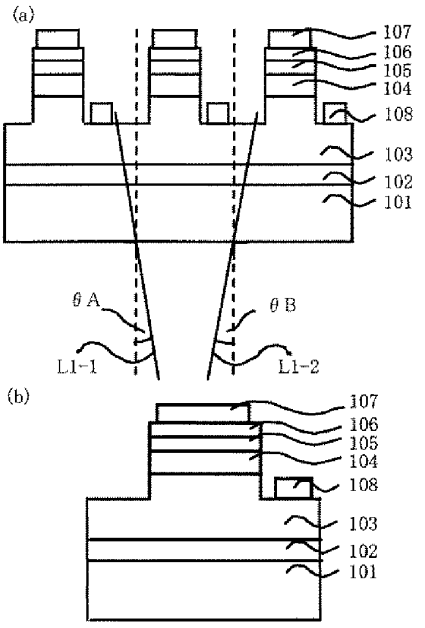
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最終頁に続く

(54)【発明の名称】窒化物半導体発光ダイオードチップとその作製法

(57)【要約】
【課題】　光取り出し効率の改善された窒化物半導体発光ダイオードチップを提供する。
【解決手段】　窒化物半導体発光ダイオードチップは、透光性基板（１０１）と、その基板の上面上に形成された窒化物半導体積層構造（１０２－１０６）とを含み、その窒化物半導体積層構造は発光層（１０４）と他の複数の半導体層とを含み、基板（１０１）は面方位によらずかつ１２０μm以上の厚さを有しており、これによってチップからの光の取り出し効率が改善されている。なお、チップの分割面の少なくとも一つは基板面に直交する面に対して傾斜させられ、かつ基板の下面は窒化物半導体積層構造の上側領域より小さい面積を有することによっても、チップからの光の取り出し効率が改善され得る。
【選択図】　図1



【特許請求の範囲】
【請求項1】
窒化物半導体発光ダイオードチップであって、透光性基板と、前記基板の上面上に形成された窒化物半導体積層構造とを含み、前記窒化物半導体積層構造は発光層とその他の複数の半導体層とを含み、前記基板は面方位によらずかつ１２０μｍ以上の厚さを有しており、これによって前記チップからの光の取り出し効率が改善されていることを特徴とする窒化物半導体発光ダイオードチップ。
【請求項2】
窒化物半導体発光ダイオードチップであって、透光性基板と、前記基板の上面上に形成された窒化物半導体積層構造とを含み、前記窒化物半導体積層構造は発光層とその他の複数の半導体層とを含み、前記基板は面方位によらないものであって、前記チップの分割面の少なくとも一つは前記基板の上面に直交する面に対して傾斜させられており、かつ前記基板の下面は前記窒化物半導体積層構造の上側領域より小さい面積を有しており、これによって前記チップからの光の取り出し効率が改善されていることを特徴とする窒化物半導体発光ダイオードチップ。
【請求項3】
前記チップの分割面の少なくとも一つは前記基板の上面に直交する面に対して傾斜させられており、かつ前記基板の下面は前記窒化物半導体積層構造の上側領域より小さい面積を有していることを特徴とする請求項１に記載の窒化物半導体発光ダイオードチップ。
【請求項4】
前記基板として絶縁性基板が用いられていることを特徴とする請求項１から３のいずれかに記載の窒化物半導体発光ダイオードチップ。
【請求項5】
前記基板としてサファイア基板または炭化珪素基板が用いられていることを特徴とする請求項１から４のいずれかに記載の窒化物半導体発光ダイオードチップ。
【請求項6】
請求項１から５のいずれかに記載された窒化物半導体発光ダイオードチップを作製するための方法であって、基板の上面上において発光層を含む複数の窒化物半導体層を結晶成長させたエピタキシャルウエハを形成する工程と、レーザ光を利用して前記ウエハから前記チップを分割する工程とを含み、これによってチップ歩留まりが改善されることを特徴とする作製法。
【請求項7】
前記レーザ光の光源として固体レーザ装置が利用されることを特徴とする請求項６に記載の作製法。

【発明の詳細な説明】
【技術分野】
【0001】
本発明はＩＩＩ－Ｖ族化合物半導体発光素子に関し、特に透光性基板上に積層された複数の窒化物系半導体層を含む発光ダイオードチップにおける光取り出し効率の改善に関するものである。
【背景技術】
【0002】
一般に、窒化物半導体発光ダイオードチップの作製においては、基板上に発光層を含む複数の窒化物半導体層が堆積されたエピタキシャルウエハが形成され、そのウエハを分割することによって複数のチップが得られる。従来の窒化ガリウム（ＧａＮ）系半導体発光ダイオードチップでは、主にサファイア等の基板が使用されており、現在ではそのようなチップを含む発光ダイオード装置が商品化されている。
【0003】
ところで、サファイア基板を用いた発光ダイオード装置では、その基板が絶縁性であるので、基板の上下両面側にｐ側電極とｎ側電極をそれぞれ設けた構造にすることが困難で

あり、透光性の電極を介して発光ダイオードチップから光を取り出す必要がある。さらに、サファイア基板の硬度が高いことから、基板を薄膜状に加工した後に、ウエハからチップに分割する必要がある。

【0004】

従来の代表的な窒化物半導体発光素子として、サファイア基板上にＧａＮ系半導体積層構造を形成して、その基板を１００μｍ程度の厚みにした後にチップ化されたものが商用化されている。例えば特開２００２－２７０９６２号公報に開示されているように、サファイア基板上に作製したＧａＮ系半導体発光素子層を分割する際に、基板厚さを８０μｍの薄さに加工している。さらに、特開２０００－６８５５６号公報では、サファイア基板上に堆積した複数の窒化物半導体層を含むエピタキシャルウエハを歩留まりよくチップ化する方法が検討されており、その方法によって８０μｍの厚みを有するウエハをチップ分割している。

【特許文献1】特開２００２－２７０９６２号公報

【特許文献2】特開２０００－６８５５６号公報

【発明の開示】

【発明が解決しようとする課題】

【0005】

上述のように、従来の窒化物半導体発光ダイオードチップにおいては、それに含まれる半導体積層構造の表面に、透光性の電極（通常はｐ側電極下）とｐ側およびｎ側の両電極とを形成する必要がある。そして、基板の裏面は支持台上に接合される。したがって、チップから外部への光の取出し効率に関して、ｐ側およびｎ側の両電極で光が遮られることによる損失が生じる。

【0006】

また、サファイア基板を含むエピタキシャルウエハから複数の発光ダイオードチップを歩留まりよく分割する場合、サファイア基板の硬度が高くてダイシングやスクライブが困難である。したがって、エピタキシャルウエハの形成後に、基板を研削するなどして１００μｍ以下の薄さにする必要がある。しかし、基板を薄くするれば、基板の側面から外部への光の取り出し効率が低下する。これらの事情から、従来のサファイア基板を含む窒化物半導体発光ダイオードチップにおいて、チップから外部へ光の取り出しを行う際の光損失が大きい。

【0007】

以上のような従来技術の状況に鑑み、本発明は、光取り出し効率の改善された窒化物半導体発光ダイオードチップを歩留まりよく提供することを主要な目的としている。

【課題を解決するための手段】

【0008】

本発明の一つの態様によれば、窒化物半導体発光ダイオードチップは、透光性基板と、その基板の上面上に形成された窒化物半導体積層構造とを含み、その窒化物半導体積層構造は発光層と他の複数の半導体層とを含み、基板は面方位によらずかつ１２０μｍ以上の厚さを有しており、これによってチップからの光の取り出し効率が改善されていることを特徴としている。

【0009】

本発明の他の態様によれば、窒化物半導体発光ダイオードチップは、透光性基板と、その基板の上面上に形成された窒化物半導体積層構造とを含み、その窒化物半導体積層構造は発光層とその他の複数の半導体層とを含み、基板は面方位によらないものであって、チップの分割面の少なくとも一つは基板面に直交する面に対して傾斜させられており、かつ基板の下面は窒化物半導体積層構造の上側領域より小さい面積を有しており、これによってチップからの光の取り出し効率が改善されていることを特徴としている。

【0010】

なお、基板としては、絶縁性基板が用いられ得る。また、絶縁性基板として、サファイア基板、炭化珪素基板、またはスピネル基板が用いられ得る。

【0011】
上述のような窒化物半導体発光ダイオードチップを作製するための方法として、基板の上面上において発光層を含む複数の窒化物半導体層を結晶成長させたエピタキシャルウエハを形成する工程と、レーザ光を利用してウエハからチップを分割する工程とを含むことができ、これによってチップ歩留まりが改善され得る。なお、レーザ光の光源として、固体レーザ装置が好ましく利用され得る。
【発明の効果】
【0012】
本発明の一つの態様によれば、窒化物半導体発光ダイオードチップに含まれる透光性基板が従来に比べて大きな１２０μｍ以上の厚さを有している。したがって、大きな厚さの基板の側面からの光放射量が増大して、発光ダイオードチップからの光の取り出し効率が改善され得る。本発明の他の態様によれば、窒化物半導体発光ダイオードチップの分割面の少なくとも一つが基板の上面に直交する面に対して傾斜させられており、かつ基板の下面は窒化物半導体積層構造の上側領域より小さい面積を有している。したがって、その基板の傾斜側面による反射や屈折の影響によって、基板の側面からの光放射量が増大し、発光ダイオードチップからの光の取り出し効率が改善され得る。
【発明を実施するための最良の形態】
【0013】
（実施例１）
図１において、本発明の実施例１によるＧａＮ系化合物半導体発光ダイオードに関するチップ分割法が模式的な断面図で図解されている。すなわち、図１（ａ）は複数の発光ダイオード構造を含むエピタキシャルウエハを表し、図１（ｂ）はそのウエハから分割された発光ダイオードチップを表している。なお、本願の図面において、種々の層の厚さや幅などの寸法関係は図面の明瞭化と簡略化のために適宜に変更されており、実際の寸法関係を表してはいない。
【0014】
図１（ａ）のウエハにおいて、厚さ４３０μｍで、Ｃ面（０００１）の面方位をもったサファイア基板１０１上に、ＧａＮバッファ層１０２、ｎ型ＧａＮコンタクト層１０３、$In_{0.08}Ga_{0.92}N$量子井戸層とＧａＮ障壁層の４ペアーからなるＭＱＷ（多重量子井戸）活性層１０４、ｐ型ＡｌＧａＮ層１０５、ｐ型ＧａＮコンタクト層１０６が順次積層されている。そして、ｐ型ＧａＮコンタクト層１０６上にｐ側コンタクト電極として透光性Ｐｄ電極１０７が形成され、ｎ型ＧａＮコンタクト層１０３上にｎ側コンタクト電極としてＴｉとＡｌを用いたｎ側電極１０８が形成されている。
【0015】
図１（ａ）のウエハの作製においては、ＭＯＣＶＤ（有機金属気相成長）法を用いて、サファイア基板１０１上に複数のＧａＮ系半導体層がエピタキシャル成長させられた。まず、サファイア基板１０１を反応室内のサセプター上に装着後、NH_3とN_2とH_2を混合した雰囲気にて１２００℃でその基板のベーキングを行った。
【0016】
その後、すみやかに基板温度を４５０℃に降温し、H_2のキャリアガスとともにトリメチルガリウム（ＴＭＧ）とアンモニア（NH_3）を用いて、厚さ３０ｎｍのＧａＮバッファ層１０２を基板上に堆積した。続いて、すみやかに基板温度を１１００℃に昇温し、トリメチルガリウム（ＴＭＧ）とNH_3およびドーパントのモノシラン（SiH_4）を用いて、バッファ層１０２上に厚さ５μｍのｎ型ＧａＮコンタクト層１０３を成長させた。
【0017】
次に、７５０℃の基板温度にて、トリメチルインジウム（ＴＭＩ）、ＴＭＧ、およびNH_3を利用して、ｎ型コンタクト層１０３上において、厚さ３ｎｍの$In_{0.08}Ga_{0.92}N$井戸層と厚さ９０ｎｍのＧａＮ障壁層の４ペアーからなるＭＱＷ活性層１０４を形成した。
【0018】

さらに、基板温度１１００℃にて、トリメチルアルミニウム（ＴＭＡ）、ＴＭＧ、NH_3、およびドーパントのシクロペンタジエニルマグネシウム（Cp_2Mg）を用いて、ＭＱＷ活性層１０４上に、Ｍｇドープのｐ型$Al_{0.08}Ga_{0.92}N$クラッド層１０５を厚さ３０ｎｍに成長させた。続いて、同じ基板温度にて、ＴＭＧ、NH_3、およびCp_2Mgを用いて、ｐ型クラッド層１０５上に厚さ１２０ｎｍのＭｇドープｐ型ＧａＮコンタクト層１０６を堆積し、基板温度を常温まで冷却した後にエピタキシャルウエハを大気中に取り出した。

【0019】

その後、エピタキシャルウエハ中のｐ型ドーパントを活性化するために、熱処理炉を用いてN_2雰囲気中で８００℃にて１５分間の熱処理を行った。次に、ウエハの上面にレジストを塗布してフォトリソグラフィを行った後、ｐ型ＧａＮ層１０６上にｐ側コンタクト電極として透光性Ｐｄ電極１０７を形成した。

【0020】

次に、有機洗浄を行ってレジストを除去した後にウエハ上面に再度レジストを塗布してフォトリソグラフィを行ない、続いて反応性イオンエッチング（ＲＩＥ）を利用して、ウエハのｐ型ＧａＮ層１０６からｎ型ＧａＮ層１０３に達するまで選択的にエッチングを行った。さらに、有機洗浄を行ってレジストを除去した後にウエハ上面に再度レジストを塗布してフォトリソグラフィを行ない、ｎ型ＧａＮ層１０３上にｎ側コンタクト電極としてＴｉとＡｌからなるｎ側電極１０８を形成した。

【0021】

続いて、有機洗浄を行ってレジストを除去した後にウエハ上面に再度レジストを塗布してフォトリソグラフィを行ない、電極部を除いてウエハ上面がSiO_2膜（図示せず）で覆われた。

【0022】

その後、ウエハをシートに貼り付けて冶具に固定し、ウエハから複数の発光ダイオードチップの分割が固体レーザ装置を用いて行われた。より具体的には、固体レーザ装置としてＹＡＧレーザ装置が利用され、２６６ｎｍまたは３５５ｎｍの高調波レーザ光が用いられた。レーザ光のエネルギに関しては、１０μＪ／ｃｍ^2～１００ｍＪ／ｃｍ^{2}程度の範囲内のパルス状または連続な状態のレーザ光を使用することができる。なお、レーザ装置としてはＹＡＧレーザ装置に限られず、２６６ｎｎから３５５ｎｍ程度の波長範囲内のレーザ光を放射し得るレーザ装置を用いて、サファイア基板の局所的な昇華または熱膨張を利用してスクライブできればよい。

【0023】

具体的には、レーザ光がサファイア基板に進入する角度を冶具によって制御して、レーザスクライブラインＬ１－１とＬ１－２に沿って、ウエハから複数の発光ダイオードチップが分割された。本実施例１においては、図１（ａ）に示されているように、スクライブラインＬ１－１とＬ１－２は、基板面に直交する破線に対して時計回りを正にして$\theta A=0°$および$\theta B=0°$の角度をなすように設定され、その状態でスクライブを行った。その結果、図１（ｂ）に示されているように、一辺が３５０μｍの正方形状平面を有するＧａＮ系発光ダイオードチップが得られた。そのような発光ダイオードチップはその基板底面が支持台上に接合され、電気的配線と樹脂モールドを介して発光ダイオード装置として完成させられる。

【0024】

従来法によれば、ダイオードチップ作製において、サファイア基板を研削研磨し、裏面よりダイアモンド製のカッターによって分割した。しかし、この方法では、サファイア面に対して、分割する角度を制御して歩留まりよくチップ分割をすることは難しかったが、本実施例の方法によれば、歩留まりよく、なおかつ分割角度の制御がよくダイオードチップの作製が可能になった。

【0025】

図１（ｂ）に示された本実施例１のＧａＮ系発光ダイオードチップの出力特性は、従来

のＧａＮ系発光ダイオードチップの出力特性と比較された。その従来の発光ダイオードチップの作製においては、図１（ａ）と同様のエピタキシャルウエハが作製された。しかし、そのウエハから複数の発光ダイオードチップを分割する際に、従来方法に従ってウエハの厚さを１００μｍ程度まで基板裏面を研削して研磨し、その後に機械的スクライブとブレーキングによってチップ分割された。こうして得られた従来の発光ダイオードチップにおいて、順方向注入電流（Ｉｆ）＝２０ｍＡのときに、光出力（Ｐｏ）＝３．０ｍＷであった。他方、本実施例１によって作製された図１（ｂ）の発光ダイオードチップにおいては、Ｉｆ＝２０ｍＡのときにＰｏ＝５．０ｍＷであった。

【0026】

すなわち、本実施例１におけるチップ分割による発光ダイオードチップは、従来に比べて光出力が顕著に改善されていることがわかる。この理由としては、従来の機械的スクライブ法では研削と研磨によってサファイア基板１０１を１００μｍ程度に薄くしなければチップ化することが困難であったが、本実施例１のようにレーザスクライブを利用する方法では基板が４３０μｍのように厚くてもチップ分割が可能であることから、発光層から放射されて基板裏面で反射された光が、基板側面から外部へ取り出されやすくなったために、光取り出し効率が向上したと考えられる。

【0027】

さらなる検討の結果では、本実施例においてサファイア基板１０１の厚さが２５０μｍである場合には、Ｉｆ＝２０ｍＡのときにＰｏ＝３．８ｍＷであることがわかった。また、サファイア基板１０１の厚さが１２０μｍ以上の場合に、従来に比べて発光ダイオードチップの光出力が向上することがわかった。

【0028】

（実施例２）

図２において、本発明の実施例２によるＧａＮ系化合物半導体発光ダイオードに関するチップ分割法が模式的な断面図で図解されている。この図２における複数層２０１～２０８の作製法は実施例１における複数層１０１～１０８の作製法と同様であるので、その説明は繰り返されない。なお、本実施例２においても、サファイア基板２０１として、実施例１と同様に４３０μｍの厚さものが使用された。また、本実施例２においても、実施例１と同様にレーザスクライブを利用して、エピタキシャルウエハから発光ダイオードチップが分割された。

【0029】

本実施例２においては、レーザ光が基板へ入射する角度を冶具で制御することによって、図２の基板面に垂直な破線方向に対するレーザスクライブラインＬ２－１およびＬ２－２の傾斜角θＣおよびθＤが制御された。このとき、図２において、光を放射する半導体層の上面領域で一辺の長さｄを３５０μｍに設定し、θＣとθＤを調整することによって基板裏面側の一辺の長さｅが２００μｍになるように設定した。ただし、図２に示されているように、スクライブラインＬ２－１とＬ２－２は、それぞれ基板面に直交する破線に対して時計回りを正にしてθＣ＜０°およびθＤ＞０°の角度をなすように設定された。

【0030】

こうして得られた本実施例２の発光ダイオードチップにおいて、Ｉｆ＝２０ｍＡの入力電流のもとで、光出力はＰｏ＝５．２ｍＷであった。すなわち、本実施例２の発光ダイオードチップにおける外部への光取り出し効率は、実施例１と比較しても向上したことがわかる。この理由としては、基板面に垂直な面に対して発光ダイオードチップの側面を傾斜させることによって、その傾斜側面による反射や屈折の影響によって、発光層からの光が基板側面から放射されやすくなったものと考えられる。

【0031】

さらなる検討の結果、ｄ＝３５０μｍに固定してｅ＝１００μｍになるように発光ダイオードチップを作製したところ、Ｉｆ＝２０ｍＡの入力電流のもとでPo＝５．４ｍＷの光出力が得られた。しかしながら、さらなる検討の結果では、基板底面の長さｅが１００μｍより小さな発光ダイオードチップを作製したところ、Ｉｆ＝２０ｍＡの入力電流のも

とで光出力がＰｏ＝４．０ｍＷになった。これは、発光層から放射されて基板裏面で反射された光が、基板側面から外部へ取り出されにくくなり、光取り出し効率が悪化したためと考えられる。

【0032】

（実施例３）

図３と図４において、本発明の実施例３によるＧａＮ系化合物半導体発光ダイオードに関するチップ分割法が模式的な断面図で図解されている。この図３と図４における複数層３０１～３０８の作製法も実施例１における複数層１０１～１０８の作製法と同様であるので、その説明は繰り返されない。なお、本実施例３においても、サファイア基板３０１として、実施例１と同様に４３０μｍの厚さのものが使用された。また、本実施例３においても、実施例１と同様にレーザスクライブを利用して、エピタキシャルウエハから発光ダイオードチップが分割された。

【0033】

本実施例３に係る図３と図４においても、実施例２の場合と同様に、レーザ光が基板へ入射する角度を冶具で制御することによって、基板面に垂直な破線方向に対するレーザスクライブラインＬ３－１およびＬ３－２の傾斜角θＥおよびθＦが制御された。そして、光を放射する半導体層の上面領域で一辺の長さｆを３５０μｍに設定し、θＥとθＦを調整することによって基板裏面側の一辺の長さｅが２００μｍになるように設定した。ただし、スクライブラインＬ３－１とＬ３－２は、基板面に直交する破線に対して時計回りを正にして、図３においてはθＥ＜０°およびθＦ＝０°の角度をなすようにそれぞれ設定され、図４においてはθＥ＜０°およびθＦ＜０°の角度をなすようにそれぞれ設定された。

【0034】

こうして得られた図３と図４のいずれの発光ダイオードチップにおいても、Ｉｆ＝２０ｍＡの入力電流のもとで、光出力はＰｏ＝５．２ｍＷであった。すなわち、本実施例３の発光ダイオードチップにおける外部への光取り出し効率も、実施例２の場合と同様に実施例１と比較しても向上したことがわかる。この理由は、実施例２の場合と同様と考えられる。

【0035】

なお、上述のいずれの実施例においても基板としてＣ面（０００１）の面方位を持ったサファイア基板を用いたが、この面方位によらずにＡ（１１－２０）面、Ｍ（１１００）面、またはR面（１１０２）の面方位を持ったサファイア基板を用いても、それらの面方位から変位させられたオフ面方位のサファイア基板であっても、同様の効果が得られる。また、基板として、ＧａＮ基板、スピネル基板、またはＳｉＣ基板を用いることもできる。さらに、上述の実施例において、サファイア基板に対するレーザ光の入射角度が基板を固定する冶具によって制御されたが、レーザ光をミラー等で制御してサファイア基板に対する入射角度を制御してもよい。

【産業上の利用可能性】

【0036】

以上のように、本発明によれば、光取り出し効率の改善された窒化物半導体発光ダイオードチップを歩留まりよく提供することができる。

【図面の簡単な説明】

【0037】

【図1】本発明の実施例１によるエピタキシャルウエハから複数のＧａＮ系化合物半導体発光ダイオードチップを分割する方法を図解する模式的断面図である。

【図2】本発明の実施例２によるエピタキシャルウエハから複数のＧａＮ系化合物半導体発光ダイオードチップを分割する方法を図解する模式的断面図である。

【図3】本発明の実施例３によるエピタキシャルウエハから複数のＧａＮ系化合物半導体発光ダイオードチップを分割する一態様を図解する模式的断面図である。

【図4】本発明の実施例３によるエピタキシャルウエハから複数のＧａＮ系化合物半導体

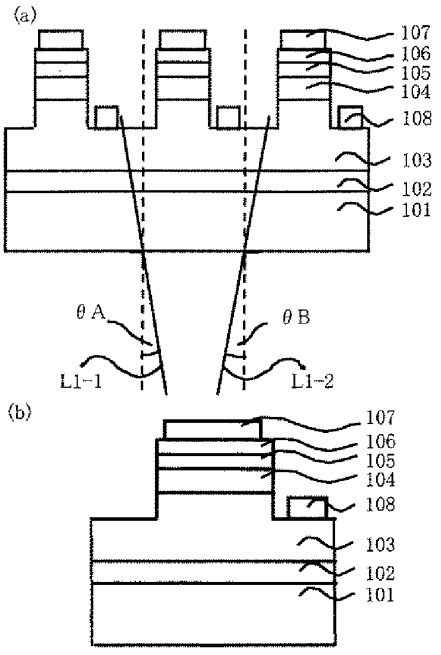
発光ダイオードチップを分割する他の態様を図解する模式的断面図である。

【符号の説明】

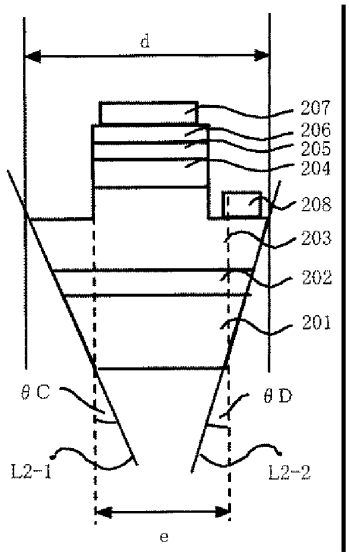
【0038】

１０１、２０１、３０１　サファイア基板、１０２、２０２、３０２　ＧａＮバッファ層、１０３、２０３、３０３　ｎ型ＧａＮコンタクト層、１０４、２０４、３０４　ＭＱＷ活性層、１０５、２０５、３０５　ｐ型ＡｌＧａＮ層、１０６、２０６、３０６　ｐ型ＧａＮコンタクト層、１０７、２０７、３０７　透光性Ｐｄ電極、１０８、２０８、３０８　ｎ側電極、Ｌ１－１、Ｌ１－２、Ｌ２－１、Ｌ２－２、Ｌ３－１、Ｌ３－２　レーザスクライブライン、θＡ、θＢ、θＣ、θＤ、θＥ、θＦ　基板面に垂直な方向に対するレーザ光の進入角度、ｄ、ｆ　半導体積層構造の光放射面側で一辺の長さ、ｅ、ｇ　基板裏面側の一辺の長さ。

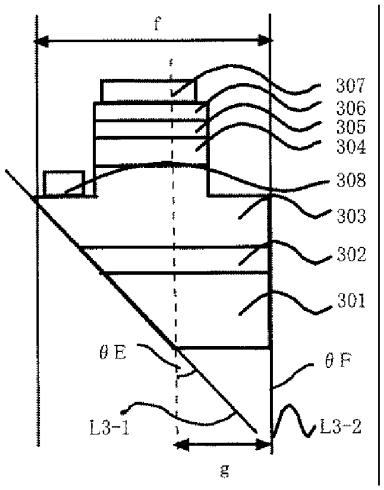
【図1】



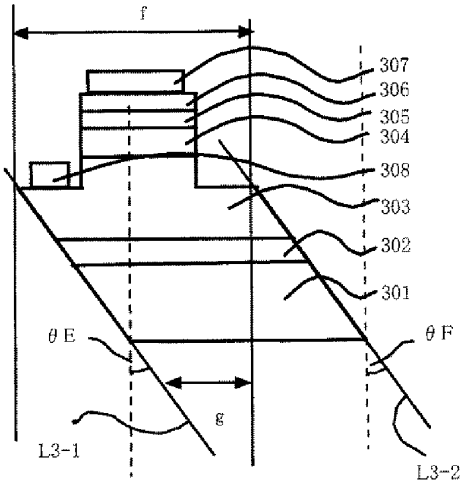
【図2】



【図3】


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【図4】


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θF
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L3-1
L3-2

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Ｆターム(参考) 5F041 AA04　AA41　CA04　CA05　CA40　CA65　CA74　CA76　CA83　CA87

Electronic Patent Application Fee Transmittal

Application Number:	11993965
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Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Filer:	Hae-Chan Park/karim sosa
Attorney Docket Number:	P2317US00

Filed as Large Entity

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt

EFS ID:	7078112
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
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First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
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RAM confirmation Number	2909
Deposit Account	
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Information Disclosure Statement (IDS) Filed (SB/08)	IDS_Transmittal.pdf	886284 1620cadcc3c1ec1b39c2277ecefbe527fe5c38f0	no	5
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Information:					
2	NPL Documents	2010-02-01_Office_Action.pdf	649569 acae82a7f2e18257fd3ec313ceeab57926540bae	no	18
Warnings:					
Information:					
3	Foreign Reference	JP06-244458.pdf	224920 3be0a9f137d93f40fdbd1b2fd453250dca309a6e	no	5
Warnings:					
Information:					
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10	Fee Worksheet (PTO-875)	fee-info.pdf	29941 b5a85481cb589943649e2fb95513c5d73565c9a7	no	2
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PTO/SB/08a (07-09)
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(**Not for submission under 37 CFR 1.99)**

Application Number	11993965
Filing Date	2007-12-26
First Named Inventor	Jong Lam LEE
Art Unit	2818
Examiner Name	NGUYEN, Thinh T
Attorney Docket Number	P2317US00

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5252434		1993-10-12	Blonder	

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U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050023537		2005-02-03	Salam	

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	1	2005008791	WO		2005-01-27	Matsushita Electric Industrial Co., Ltd.		☐
	2	1469529	EP		2004-10-20	Lumileds Lighting US, LLC		☐
	3	2004006582	JP		2004-01-08	Nitride Semiconductor Co Ltd		☐

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	Examiner Name	NGUYEN, Thinh T
	Attorney Docket Number	P2317US00

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	1	European Search Report issued February 10, 2010 by the European Patent Office in European Patent Application No. 06769008.1	☐

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	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, Thinh T
	Attorney Docket Number	P2317US00

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☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2010-03-01
Name/Print	Hae-Chan Park	Registration Number	50114

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(54) Alternating current light emitting device

(57) A plurality of semiconductor light emitting diodes formed on a single substrate are connected in series for use with an alternating current source. In one embodiment, the series array of light emitting diodes is directly connected to an alternating current source. In other embodiments, the series array of semiconductor light emitting diodes is mounted on a submount with integrated rectifying and filtering circuitry. The submount may be, for example, a silicon integrated circuit. In some embodiments a wavelength converting material is provided over the semiconductor light emitting diodes such that light emitted by the light emitting diodes and light emitted by the wavelength converting material mix to produce while light.

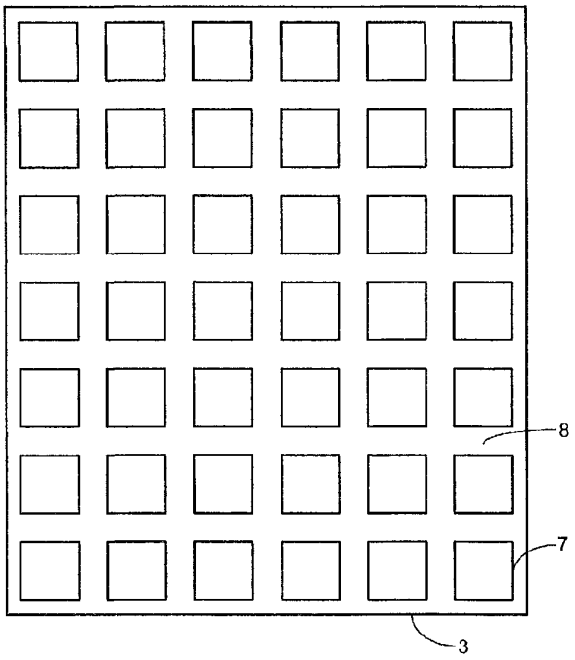


Fig. 1A

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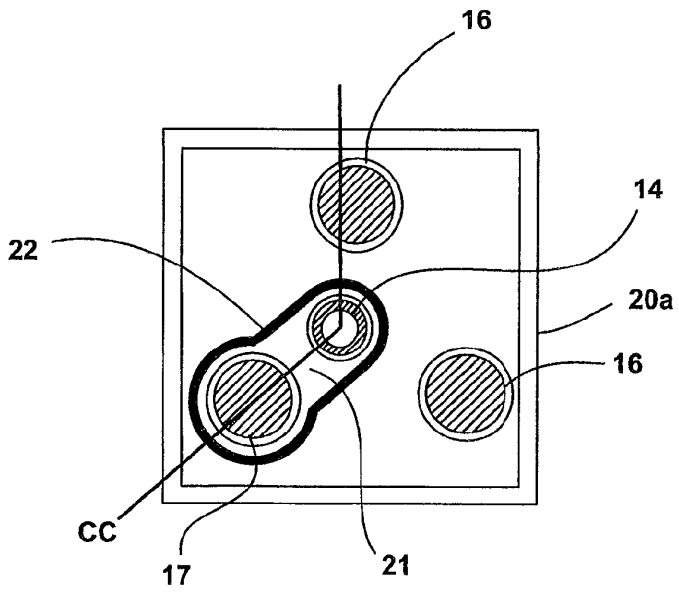


Fig. 1B

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Description

[0001] The present invention relates to monolithic arrays of semiconductor light emitting devices powered by alternating current sources.

[0002] Wojnarowski et al., U.S. Patent 6,412,971, teach an array of separate, individual semiconductor light emitting diodes (LEDs) mounted on a conventional light bulb base for insertion into a residential 120 volt alternating current socket. Wojnarowski et al.'s devices include a rectifier and filter to provide direct current. Direct current provides a constant voltage and current to the array of LEDs, thus the LEDs are constantly on when the array is connected to the alternating current source, eliminating any visible flickering that may have occurred had unfiltered alternating current been used to power the array. Wojnarowski et al.'s devices are bulky and difficult to build and package due to the large number of separate LEDs used and due to the external filtering and rectifying circuitry. The filtering and rectifying circuitry also use power, create heat, and add cost.

[0003] In accordance with embodiments of the invention, a plurality of LEDs formed on a single substrate are connected in series for use with an alternating current source. In one embodiment, the plurality of LEDs are directly connected to an unfiltered and unrectified alternating current source. In other embodiments, the LEDs are mounted on a submount with integrated rectifying and filtering circuitry. The submount may be, for example, a silicon integrated circuit. In some embodiments a wavelength converting material is provided over the LEDs such that light emitted by the LEDs and light emitted by the wavelength converting material mix to produce light with a wavelength distribution different from that emitted by the LEDs.

[0004] Devices without external LED electrical drivers (or with rectifying and filtering circuitry integrated in the submount) offer the advantages of being small and simple to build and package. Such devices may also have reliability and cost advantages.

BRIEF DESCRIPTION OF THE DRAWINGS:

[0005]

Fig. 1A is a plan view of a monolithic array of electrically isolated LEDs.

Fig. 1B is a plan view of a single LED in the array shown in Fig. 1A.

Fig. 2 is a cross-sectional view of the device illustrated in Fig. 1B.

Fig. 3 illustrates a monolithic array of LEDs mounted on a submount.

Figs. 4 and 5 are circuit diagrams of different embodiments of the device of Fig. 3.

Fig. 6 illustrates an embodiment of the invention incorporating a zener diode.

Fig. 7 is an exploded view of a packaged light emitting device.

Fig. 8 is a cross section of a portion of a monolithic array of LEDs mounted on a submount.

Figs. 9 and 10 illustrate packaged devices.

[0006] In accordance with embodiments of the present invention, semiconductor light emitting devices such as light emitting diodes are arranged in monolithic arrays suitable for use with high voltage power sources include those using alternating current. "High voltage" refers to a voltage greater than 10 times the forward voltage of a single LED. For example, some current III-nitride devices operate at a forward voltage of about 3.5 V at a current density of about 50 A/cm^2. Such devices usually fail at current densities greater than 150 A/cm^2. If a single such device were connected to a 120 RMS V alternating current circuit, the peak voltage of about 180 V would far exceed the maximum operating current density. Accordingly, in some embodiments, multiple LEDs are connected in series in order to achieve an appropriate voltage drop and current density for each device when connected to a high voltage power source.

[0007] Fig. 1A is a plan view of a monolithic array of LEDs for use in an alternating current device. An array of individual LEDs 7 are formed on a single substrate 3. The individual LEDs in the array are electrically isolated from each other by, for example, trenches 8 etched between the devices down to substrate 3 or to an insulating layer such as an undoped semiconductor layer.

[0008] Fig. 1B is a plan view of an example of a single small junction III-nitride LED 7 (i.e., an area less than approximately one square millimeter) formed in the monolithic device illustrated in Fig. 1A. In one embodiment, the device in Fig. 1B has an area greater than 300 microns by 300 microns. Fig. 2 is a cross section of the device shown in Fig. 1B, taken along axis CC. As illustrated in Fig. 2, the device includes an n-type region 11, an active region 12, and a p-type region 13 formed over a substrate 15. Each of the n-type region 11, the active region 12, and the p-type region 13 may be, for example, III-nitride semiconductor layers, and each region may contain multiple layers with the same or different characteristics. The substrate may be, for example, sapphire, GaP, Si, or SiC.

[0009] The device shown in Figs. 1B and 2 has a single via 14 etched down to n-type layer 11. An n-contact 21 is deposited in via 14. N-via 14 is located at the center of the device to provide uniformity of current and light emission. A highly reflective p-contact 20 is deposited on p-type layer 13. A thick p-metal layer 20a is deposited over reflective p-contact 20. N-contact 21 is separated from the p-metal layers 20, and 20a by one or more dielectric layers 22. A p-submount connection 16 connects to p-metal layer 20a, and an n-submount connection 17 connects to n-metal layer 21, for connecting the device to a submount. Interconnects 16 and 17 may be, for example, solder bumps.

[0010] As illustrated in Fig. 1B, the device is connect-

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ed to a submount by p-submount connections 16 and n-submount connection 17. N-submount connection 17 may be located anywhere within n-contact region 21 (surrounded by insulating layer 22) and need not be located directly over via 14. Similarly, p-submount connections 16 may be located anywhere on p-metal layer 20a. As a result, the connection of the device to a submount is not limited by the shape or placement of p-contact 20a and n-contact 21.

[0011] Fig. 3 illustrates the monolithic array of Fig. 1A mounted on a submount. Fig. 8 illustrates a cross section of a portion monolithic array mounted on a submount. Array 3 is flipped over and mounted with the contacts closest to submount 2. The dashed lines illustrate the location of each of the individual LEDs 7. The individual LEDs 7 may be separated by a trench 87 as illustrated in Fig. 8. LED array 3 is mounted on submount 2 by electrically and physically connecting interconnects (such as solder bumps 81-84 of Fig. 8) of each LED 7 to submount 2. LED array 3 is therefore mounted in flip chip configuration, such that light is extracted from each of LEDs 7 through the substrate 15 (Fig. 2). In one embodiment, each of the LEDs are connected to each other in series by interconnects within or on the surface of submount 2. Interconnect 86 of Fig. 8, formed on the surface of submount 2, connects solder bumps 82 and 83 of the two LEDs pictured in Fig. 8. Interconnect 85, formed within submount 2, connects solder bump 81 to another LED or other circuitry (not shown). Alternatively, the individual LEDs can be connected by interconnects formed on array 3. Such interconnects are described in more detail in U.S. Patent No. 6,547,249, issued April 15, 2003, titled "Monolithic Series/Parallel LED Arrays Formed On Highly Resistive Substrates," and incorporated herein by reference. In some embodiments, the individual LEDs in array 3 may be interconnected by a combination of interconnects formed on array 3 and interconnects formed on or within submount 2. In embodiments where all or a portion of the interconnects are formed on array 3, only a portion of the LEDs in array 3 may be electrically and physically connected to submount 3.

[0012] Series interconnection reduces the voltage drop across each LED to a level that does not exceed the maximum forward voltage of each LED. Excessive forward voltage can damage the LEDs irreversibly. Bonding pads 4 and 5 are electrically connected to the positive and negative terminals of the array of LEDs and are used to electrically and physically connect the submount to a package. An example of a package is described below in reference to Fig. 7.

[0013] Fig. 3 illustrates a 6 x 7 monolithic array of LEDs mounted on submount 2. The number of LEDs in the monolithic array may be selected to achieve a particular voltage drop across each device. The voltage across each of the individual LEDs in the array is the line voltage divided by the number of LEDs in series. The number of LEDs is chosen such that the maximum voltage across each individual LED during the peak in the alternating current cycle is low enough so as to not damage the LEDs. At 120 RMS volts, the peak voltage will be about 180V. If the individual LEDs illustrated in Figs. 1B and 2 can tolerate a maximum forward voltage of 4.5V, at least 38 LEDs connected in series are required to prevent the voltage across each LED from exceeding the maximum tolerable voltage at the peak of the alternating current cycle. Sources with 240 RMS volts would require twice as many LEDs connected in series, while 60 RMS volt sources would require half as many LEDs connected in series. In some embodiments, the number of LEDs is selected to accommodate common alternating current sources, such as 100V in Japan, 120V in the United States, and 240V in Europe and parts of Asia. For example, for a 120 V alternating current circuit, the peak voltage may be about 180 V. If each of the LEDs in the 6 x 7 array of LEDs illustrated in Fig. 3 has a forward voltage of 3.5 V, each device will achieve the desired current density of 50 A/cm^2 at 3.5 x 42 = 147 V, without exceeding the maximum current density of 150 A/cm^2 at the peak voltage of 180 V. In the embodiment illustrated in Fig. 3, a single monolithic array is mounted on a single submount. In some embodiments, more than one monolithic array may be mounted on one or more submounts, in order to achieve the desired maximum voltage drop across each LED in the arrays.

[0014] Figs. 4 and 5 illustrate two examples of circuits that may be implemented in the device illustrated in Fig. 3. Fig. 4 illustrates a device with an LED array connected in series with an alternating current source, without any rectifying and filtering circuitry for converting the alternating voltage to a direct voltage. The LEDs are only on during that portion of the positive voltage half of each cycle of the alternating current where there is enough voltage to turn on the LEDs. Thus, at 60 Hz, the LEDs turn on 60 times per second.

[0015] Fig. 5 illustrates an LED array and a full wave bridge rectifier for rectifying the alternating current source. The full wave bridge rectifier can be an external component or integrated into the submount, as described below. An optional capacitor filters the rectified voltage to provide nearly direct current to the LED array. Driving the LEDs with a near-direct current source is common and an efficient drive waveform. When the line voltage drops below the turn-on voltage for the LEDs during the alternating current cycle, current is supplied from the capacitor rather than from the line. When the line voltage rises above the turn-on voltage of the LEDs, the capacitor charges. In some embodiments of the invention, rectifying and filtering circuitry, such as the capacitor and full wave bridge rectifier illustrated in Fig. 5, is formed in submount 2 shown in Fig. 3. Submount 2 may be, for example, a silicon chip. The circuitry other than the LED array illustrated in Fig. 5 can be formed on and/or in submount 2 using conventional integrated circuit fabrication techniques.

[0016] In some embodiments of the devices illustrat-

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ed in Figs. 4 and 5, one or more Zener diodes may be included in series with the LED array to control the voltage drop across the LED array, as illustrated in Fig. 6. The Zener diodes may be formed in submount 2. In addition, submount 2 may contain additional circuitry such as electrostatic discharge protection circuitry.

[0017] Fig. 7 is an exploded view of a packaged light emitting device. A heat-sinking slug 100 is placed into a leadframe 105. The leadframe 105 may be, for example, a filled plastic material molded around a metal frame that provides an electrical path. Slug 100 may include an optional reflector cup 102. The light emitting device array and submount 104, which may be any of the devices described herein, is mounted on slug 100. Bonding pads 4 and 5 on submount 2 (Fig. 3) are electrically connected to leads 106 by, for example wire bonding. An optical lens 108 may be added.

[0018] In some embodiments, one or more wavelength converting layers are formed over the LEDs to create white light. For example, blue LEDs may be used with a yellow wavelength converting layer, or with a red wavelength converting layer and a green wavelength converting layer, in order to create white light. Similarly, UV LEDs may be used with red, blue, and green wavelength converting layers to create white light. The wavelength converting layers may be, for example, any suitable phosphors, and may be deposited over each of LEDs 7 in array 3 (Fig. 3) by screen printing or electrophoretic deposition, or suspended in an encapsulant and injected into the space between device 104 and lens 108 in Fig. 7. Individual LEDs in the monolithic array may be covered with different wavelength converting materials.

[0019] Fig. 9 illustrates a monolithic LED array in a package such as an Edison base, designed to be screwed into a conventional light bulb socket. Submount 2 is connected by wire bonds 92 to the contacts in base 91. Base 91 can be screwed into a conventional light bulb socket. A glass bulb 90 may be positioned over base 91. Fig. 10 illustrates a monolithic LED array in a bi-pin base such as an MR16 base, designed to be plugged into a conventional wall socket. Submount 2 is connected by wire bonds 92 to contacts connected to the two prongs of plug 93. In the devices illustrated in Figs. 9 and 10, any necessary circuitry additional to array 3, such as electrostatic discharge protection circuitry, or rectifying and filtering circuitry, may be formed within submount 2.

[0020] Monolithic arrays of LEDs capable of operating with an alternating current source may offer several advantages. First, the use of a single monolithic array on a single submount simplifies building and packaging the device since it is only necessary to align, mount, and connect a single chip to the submount, rather than separate, individual devices. In addition, the lack of rectifying or filtering circuitry (or the integration of rectifying and filtering circuitry into the submount) makes the devices small in size and simple to package, since external driver circuitry is not required. In addition, devices without rectifying and filtering circuitry in particular are simple and inexpensive to fabricate due to the lack of additional circuitry beyond the LED array.

[0021] Having described the invention in detail, those skilled in the art will appreciate that, given the present disclosure, modifications may be made to the invention without departing from the spirit of the inventive concept described herein. For example, though some examples describe III-nitride devices, devices made from other materials systems, such as III-phosphide, III-arsenide, or II-VI materials may be used. Therefore, it is not intended that the scope of the invention be limited to the specific embodiments illustrated and described.

Claims

1. A device comprising:

   a submount; and
   a plurality of light emitting diodes formed on a single substrate, the plurality of light emitting diodes being mounted on the submount and connected in series;

   wherein the plurality of light emitting diodes are directly connected to an alternating current source.

2. The device of claim 1 wherein the plurality of light emitting diodes are connected in series by interconnects formed on a surface of the plurality of light emitting diodes.

3. The device of claim 1 wherein the plurality of light emitting diodes are connected in series by interconnects formed on or in the submount.

4. The device of claim 1 wherein the submount comprises a silicon integrated circuit.

5. The device of claim 1 wherein at least one of the light emitting diodes is a III-nitride light emitting diode.

6. The device of claim 5 wherein the III-nitride light emitting diode comprises a portion of the substrate and a plurality of semiconductor device layers, and wherein the III-nitride light emitting diode is mounted on the submount such that the plurality of semiconductor device layers are closer to the submount than the portion of the substrate.

7. The device of claim 1 further comprising at least one wavelength converting material overlying at least one of the light emitting diodes.

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8. The device of claim 7 wherein light emitted from the light emitting diodes mixed with light emitted from the at least one wavelength converting material appears white.

9. The device of claim 1 further comprising:

a plurality of leads electrically connected to the submount; and a lens overlying the plurality of light emitting devices;

wherein the alternating current source is connected to the plurality of leads.

10. The device of claim 1, wherein alternating current source has a peak voltage of at least 100 volts.

11. The device of claim 1, wherein the alternating current source has an rms voltage of at least 120 volts.

12. The device of claim 1, wherein the submount is connected to a base capable of being connected to a light bulb socket.

13. The device of claim 12, wherein the base is an Edison base.

14. The device of claim 1, wherein the submount is connected to a base capable of being connected to an alternating current outlet socket.

15. The device of claim 14, wherein the base is an MR16 base.

16. A device comprising:

a submount; and
a plurality of light emitting diodes formed on a single substrate, the plurality of light emitting diodes being mounted on the submount and connected in series;
a rectifying and filtering circuit formed in the submount and connected to the plurality of light emitting diodes.

17. The device of claim 16 wherein at least one of the light emitting diodes is a III-nitride light emitting diode.

18. The device of claim 17 wherein the III-nitride light emitting diode comprises a portion of the substrate and a plurality of semiconductor device layers, and wherein the III-nitride light emitting diode is mounted on the submount such that the plurality of semiconductor device layers are closer to the submount than the portion of the substrate.

19. The device of claim 16 further comprising at least one wavelength converting material overlying at least one of the light emitting diodes.

20. The device of claim 19 wherein light emitted from the light emitting diodes mixed with light emitted from the at least one wavelength converting material appears white.

21. The device of claim 16 wherein the rectifying and filtering circuit comprises a capacitor.

22. The device of claim 16 wherein the rectifying and filtering circuit comprises a full wave bridge rectifier.

23. A method of operating a light emitting device, the method comprising:

providing a plurality of semiconductor light emitting diodes formed on a single substrate and connected in series; and
supplying an alternating current source to the plurality of semiconductor light emitting diodes.

24. The method of claim 23 wherein the plurality of semiconductor light emitting diodes are physically mounted on and electrically connected to a submount, and supplying an alternating current source to the plurality of semiconductor light emitting diodes comprises supplying an alternating current source to the submount.

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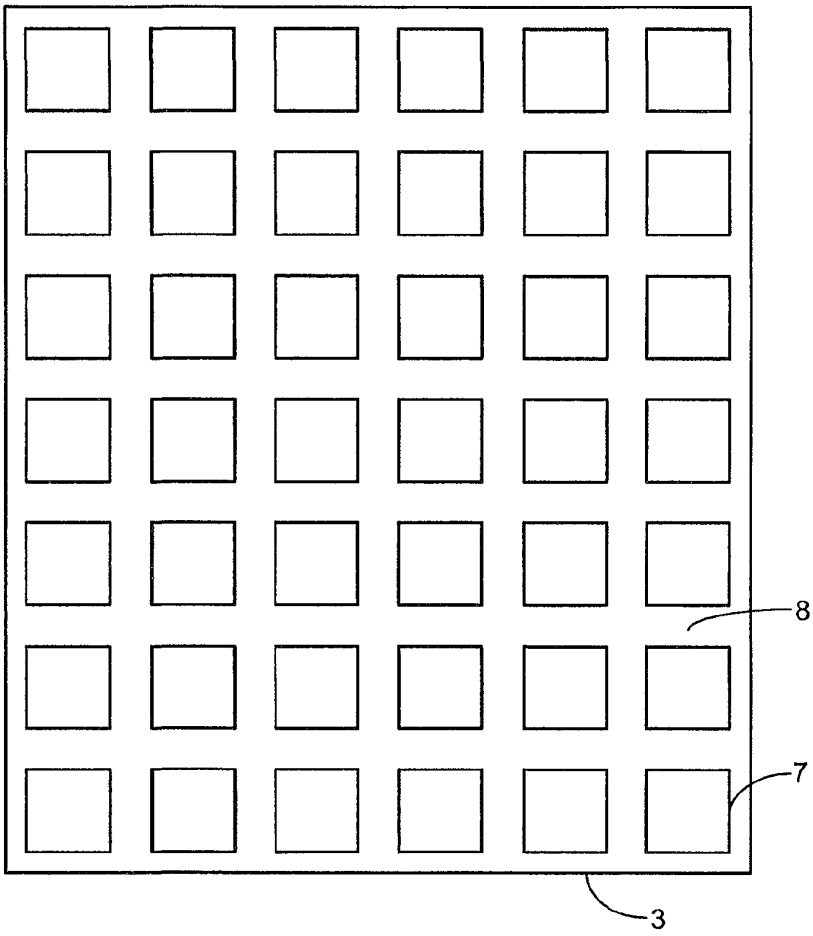


Fig. 1A

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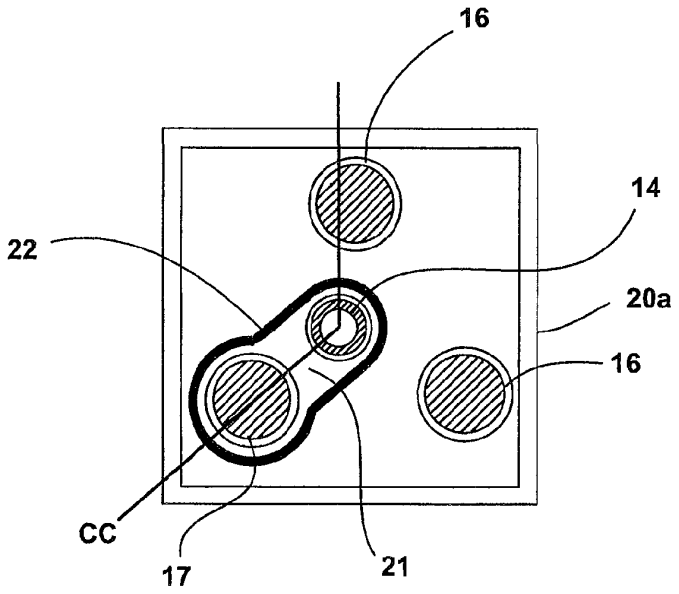


Fig. 1B

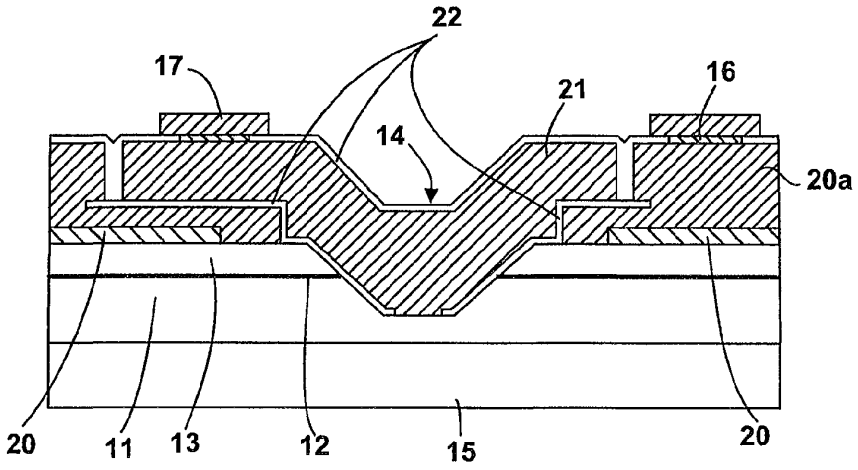


Fig. 2

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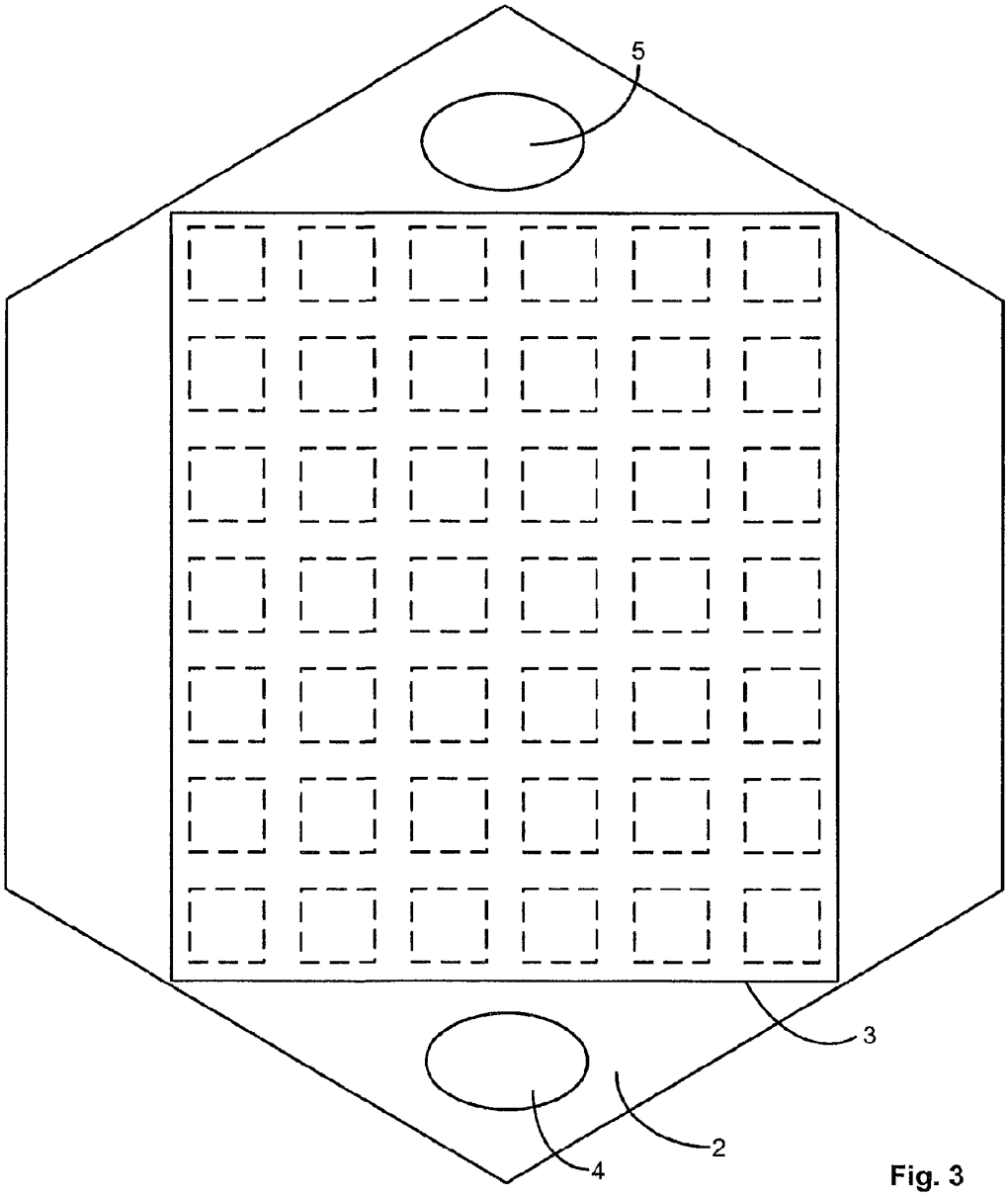


Fig. 3

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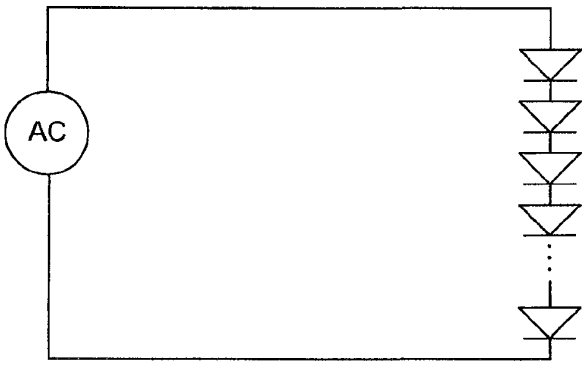


Fig. 4

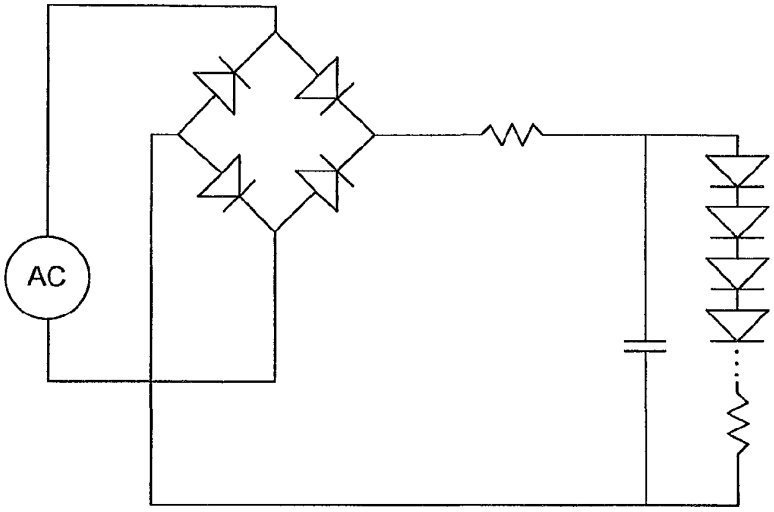


Fig. 5

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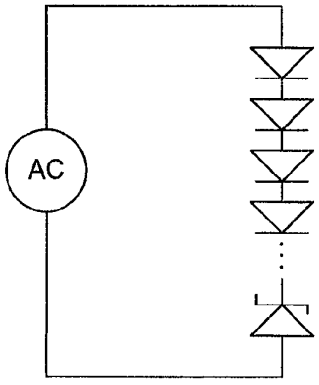


Fig. 6

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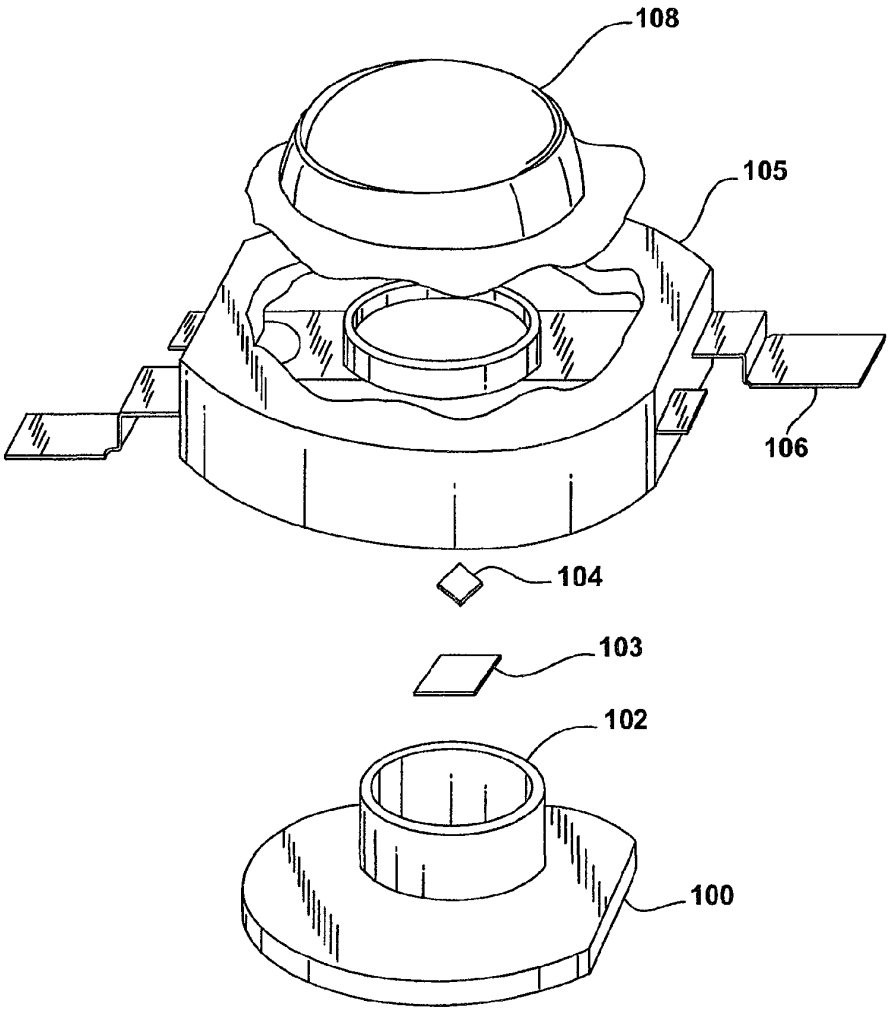


Fig. 7

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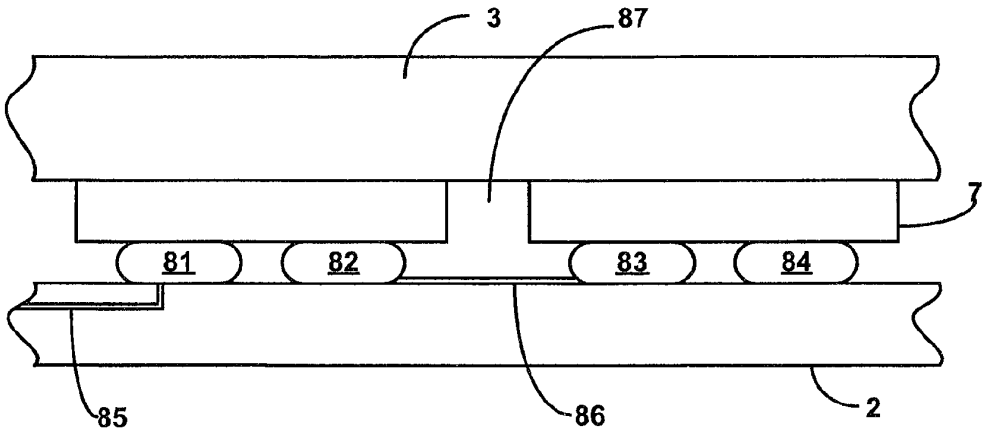


Fig. 8

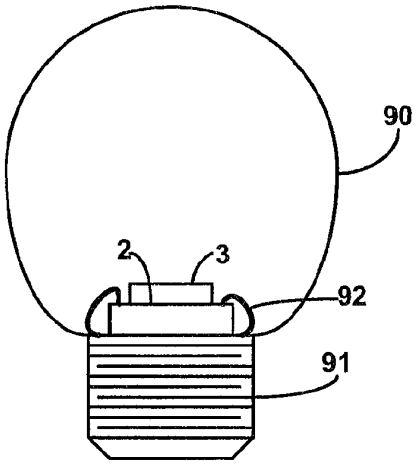


Fig. 9

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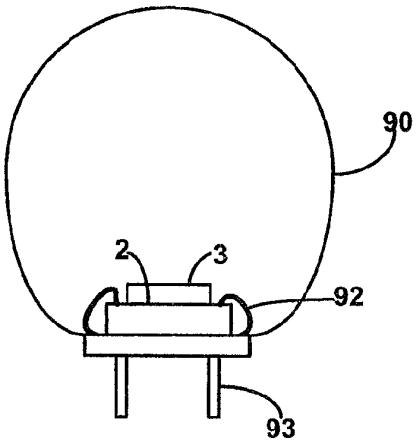


Fig. 10

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Patent Abstracts of Japan

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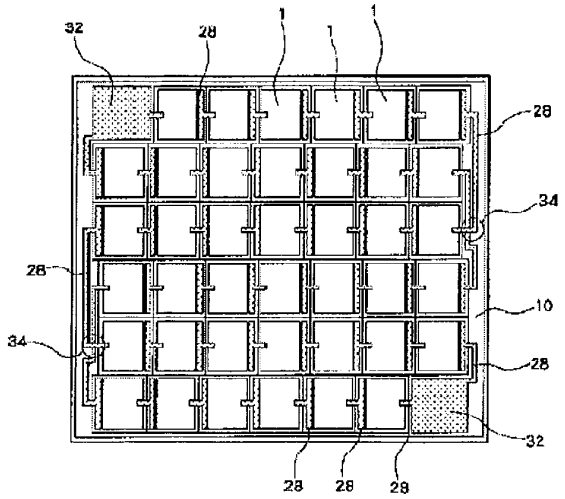
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APPLICATION NUMBER : 2002249957

APPLICANT : NITRIDE SEMICONDUCTOR CO LTD;

INVENTOR : ONO YASUO;

INT.CL. : H01L 33/00

TITLE : LIGHT EMITTING DEVICE



ABSTRACT : PROBLEM TO BE SOLVED: To provide a light emitting device which can be operated with a higher drive voltage and a lower drive current.

SOLUTION: A plurality of LEDs 1 are formed in two dimensions on an insulated substrate 10 such as sapphire with the monolithic formation process and these LEDs are connected in series to form an LED array. Two sets of LED arrays are connected in the reverse polarities to the electrode 32. An air bridge wiring 28 is formed between the LEDs 1 and between the LED 1 and electrode 32. Many LEDs 1 are formed by allocating LED arrays in zig-zag in order to obtain a higher drive voltage and a lower drive current. Since two LED arrays are connected in the reverse polarities, an AC power supply may be used as the power source.

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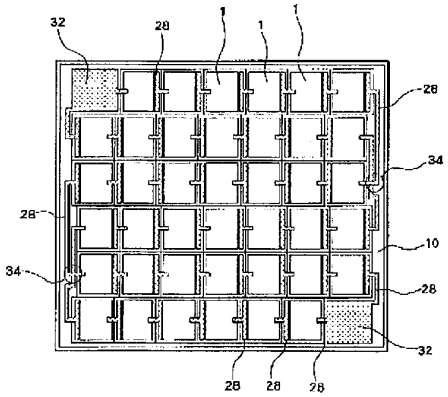
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(54)【発明の名称】発光装置

(57)【要約】
【課題】高い駆動電圧、低い駆動電流で動作できる発光装置を提供する。
【解決手段】サファイア等の絶縁基板１０上に複数のＬＥＤ１を二次元的にモノリシック形成し、複数のＬＥＤを直列接続してＬＥＤアレイとする。２組のＬＥＤアレイを互いに逆極性で電極３２に接続する。ＬＥＤ１の間及びＬＥＤ１と電極３２間はエアブリッジ配線２８とする。ＬＥＤアレイをシグザグ状に配置することで多数のＬＥＤ１を形成し、高い駆動電圧と低い駆動電流を得る。２つのＬＥＤアレイは逆極性であるため、電源として交流電源を使用できる。
【選択図】　図６



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【特許請求の範囲】
【請求項1】
絶縁基板上に複数の発光素子が形成され、前記複数の発光素子がモノリシックに直列接続されることを特徴とする発光装置。
【請求項2】
請求項１記載の装置において、
前記複数の発光素子は、前記基板上に二次元配置されていることを特徴とする発光装置。
【請求項3】
請求項１、２のいずれかに記載の装置において、
前記複数の発光素子は２組に分けられ、２個の電極に互いに反対極性となるように並列接続されることを特徴とする発光装置。
【請求項4】
請求項１～３のいずれかに記載の装置において、
前記複数の発光素子間の接続はエアブリッジ配線であることを特徴とする発光装置。
【請求項5】
請求項１～４のいずれかに記載の装置において、
前記複数の発光素子間の電気的な分離は、前記基板として使用されるサファイアにより行われることを特徴とする発光装置。
【請求項6】
請求項２記載の装置において、
前記複数の発光素子は同数ずつ２組に分けられ、各組の発光素子アレイはジグザグ状に配置され、かつ、２組の発光素子アレイは２個の電極に互いに反対極性となるように並列接続されることを特徴とする発光装置。
【請求項7】
請求項６記載の装置において、
前記２組の発光素子アレイは、互い違いに配置されることを特徴とする発光装置。
【請求項8】
請求項６、７のいずれかに記載の装置において、
前記発光素子及び電極は、平面形状が略正方形であることを特徴とする発光装置。
【請求項9】
請求項６、７のいずれかに記載の装置において、
前記発光素子及び電極は、平面形状が三角形状であることを特徴とする発光装置。
【請求項10】
請求項２記載の装置において、
前記複数の発光素子及び電極は、全体形状が略正方形となるように配置されることを特徴とする発光装置。
【請求項11】
請求項１０記載の装置において、
前記複数の発光素子からなる発光素子アレイはジグザグ状に配置されることを特徴とする発光装置。
【請求項12】
請求項６～９のいずれかに記載の装置において、
前記電極は、交流電源用電極であることを特徴とする発光装置。
【請求項13】
請求項６～９のいずれかに記載の装置において、
前記２組の発光素子アレイは、共通のｎ電極を有することを特徴とする発光装置。

【発明の詳細な説明】
【０００１】
【発明の属する技術分野】
本発明は、基板上に複数の発光素子が形成された発光装置に関する。

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【０００２】
【従来の技術】
発光素子（ＬＥＤ）等の発光手段が表示用途等に使用される場合には、その使用条件が駆動電圧約１～４Ｖ、駆動電流が約２０ｍＡとなっている。ところで、近年ＧａＮ系化合物半導体を用いた短波長ＬＥＤが開発され、フルカラーや白色等の固体光源が実用化されたことに伴い、次第にＬＥＤを照明用途にも応用することが検討されている。ＬＥＤを照明用途に応用する場合に、上述した駆動電圧１～４Ｖ、駆動電流２０ｍＡという使用条件とは異なる条件で使用される事態も生じる。このため、ＬＥＤにより大電流を流し、発光出力を大きくする工夫がなされている。大電流を流すためには、ＬＥＤのｐｎ接合面積を大きくし、電流密度を小さく抑える必要がある。
【０００３】
【発明が解決しようとする課題】
ＬＥＤを照明用光源として使用する場合には、電源として交流を使用し、１００Ｖ以上の駆動電圧で使用できることが便利である。また、同じ電力を投入して同じ発光出力を得るのであれば、低い電流値を保ちながら高い電圧を印加した方が電力損失を小さくすることができる。しかし、従来のＬＥＤでは、必ずしも十分に駆動電圧を高くすることはできなかった。
【０００４】
本発明は、上記従来技術の有する課題に鑑みなされたものであり、その目的は、高い駆動電圧で動作できる発光装置を提供することにある。
【０００５】
【課題を解決するための手段】
上記目的を達成するために、本発明は、絶縁基板上に複数の発光素子が形成され、前記複数の発光素子がモノリシックに直列接続されることを特徴とする。
【０００６】
ここで、前記複数の発光素子は、前記基板上に二次元配置されていることが好適である。
【０００７】
また、前記複数の発光素子は２組に分けられ、２個の電極に互いに反対極性となるように並列接続されることが好適である。
【０００８】
前記複数の発光素子間の接続はエアブリッジ配線とすることが好適である。
【０００９】
前記複数の発光素子間の電気的な分離は、前記基板として使用されるサファイアにより行われることが好適である。
【００１０】
また、前記複数の発光素子は同数ずつ２組に分けられ、各組の発光素子アレイはジグザグ状に配置し、かつ、２組の発光素子アレイは２個の電極に互いに反対極性となるように並列接続されることも好適であり、前記２組の発光素子アレイは、互い違いに配置することができる。
【００１１】
また、前記発光素子及び電極は、平面形状が略正方形あるいは三角形状とすることが好適である。
【００１２】
また、前記複数の発光素子及び電極は、全体形状が略正方形となるように配置されることが好適である。
【００１３】
本発明において、電極は、交流電源用電極とすることができる。
【００１４】
また、前記２組の発光素子アレイは、共通のｎ電極を有することが好適である。
【００１５】

このように、本発明では複数の発光素子をモノリシックに、すなわち同一基板上に形成し、これらを直列接続することで、高駆動電圧を可能とする。複数の発光素子を一方向に接続することで直流駆動が可能となるが、複数の発光素子を２組に分け、各組の発光素子（発光素子アレイ）を互いに逆極性となるように電極に接続することで交流駆動も可能となる。各組の個数は同数でもよく、あるいは異なっていてもよい。

【００１６】

複数の発光素子を二次元配列する方法は種々存在するが、基板専有面積をできるだけ小さくすることが望ましい。例えば、２組の発光素子アレイをそれぞれジグザグ状に、すなわち複数の発光素子を折れ曲がった直線上に配置し、それぞれの発光素子アレイを互い違いに配置することで、基板面積を有効活用して多数の発光素子を接続することができる。２組の発光素子アレイを互い違いに配置することで、配線の交叉部分が生じる場合もあるが、発光素子間をエアブリッジ配線で接続することにより交叉部分での短絡を有効に防止できる。発光素子及び電極の形状は任意であるが、例えば平面形状が略正方形となるように形成することで全体形状も略正方形となり、標準的なマウント構造を使用できる。発光素子及び電極を正方形以外、例えば三角形とした場合でも、これらの三角形状を組み合わせることで全体として略正方形を形成すれば、同様に標準的なマウント構造を使用できるようになる。

【００１７】

【発明の実施の形態】

以下、図面に基づき本発明の実施形態について説明する。

【００１８】

図１には、本実施形態においてＧａＮ系化合物半導体発光素子としてのＬＥＤ１の基本構成が示されている。ＬＥＤ１は、基板１０上に順次ＧａＮ層１２、Ｓｉドープのｎ型ＧａＮ層１４、ＩｎＧａＮ発光層１６、ＡｌＧａＮ層１８、ｐ型ＧａＮ層２０が積層され、ｐ型ＧａＮ層２０に接してｐ電極２２、ｎ型ＧａＮ層１４に接してｎ電極２４が形成される構成である。

【００１９】

図１に示されたＬＥＤは以下のプロセスにより作製される。すなわち、まず、ＭＯＣＶＤ装置にてサファイアｃ面基板を水素雰囲気中で１１００℃、１０分間熱処理する。そして、温度を５００℃まで降温させ、シランガスとアンモニアガスを１００秒間供給して不連続なＳｉＮ膜を基板１０上に形成する。なお、このプロセスはデバイス中の転位密度を低減させるためのものであり、図ではＳｉＮ膜は省略している。次に、同一温度でトリメチルガリウム及びアンモニアガスを供給してＧａＮ層を２０ｎｍ厚成長させる。温度を１０５０℃に昇温し、再びトリメチルガリウム及びアンモニアガスを供給してアンドープＧａＮ（ｕ－ＧａＮ）層１２及びＳｉドープのｎ型ＧａＮ層１４を各２μｍ厚成長させる。その後、温度を７００℃程度まで降温してＩｎＧａＮ発光層１６を２ｎｍ厚成長させる。目標組成はｘ＝０．１５、すなわち$In_{0.15}Ga_{0.85}N$である。発光層１６成長後、温度を１０００℃まで昇温してＡｌＧａＮ正孔注入層１８を成長させ、さらにｐ型ＧａＮ層２０を成長させる。

【００２０】

ｐ型ＧａＮ層２０を成長させた後、ウエハをＭＯＣＶＤ装置から取り出し、Ｎｉ１０ｎｍ厚、Ａｕ１０ｎｍ厚を順次真空蒸着で成長層表面に形成する。５％の酸素を含む窒素ガス雰囲気中で５２０℃熱処理することで金属膜はｐ型透明電極２２となる。透明電極形成後、全面にフォトレジストを塗布し、ｎ型電極形成のためのエッチングをフォトレジストをマスクとして行う。エッチング深さは、例えば６００ｎｍ程度である。エッチングで露出したｎ型ＧａＮ層１４上にＴｉ１５ｎｍ厚、Ａｌ１５ｎｍ厚を形成し、窒素ガス雰囲気中で４５０℃、３０分間熱処理してｎ型電極２４を形成する。最後に、基板１０の裏面を１００μｍまで研磨してチップを切り出し、マウントすることでＬＥＤ１が得られる。

【００２１】

図１では、基板１０上に一つのＬＥＤ１が形成されているが、本実施形態では、基板１０

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上にＬＥＤ１をモノリシックに、かつ二次元アレイ状に複数形成し、各ＬＥＤを接続して発光装置（チップ）を構成する。

【００２２】

図２には、発光装置の等価回路図が示されている。図２において、２次元アレイ状に形成された発光素子群は同数（図では４個）ずつ２組に分けられ、各組のＬＥＤ１はそれぞれ直列接続され、２組のＬＥＤ列は電極（駆動電極）に対して逆極性となるように並列接続される。このようにＬＥＤ列が直列接続されることにより、各々の駆動電圧が加算された高い電圧でＬＥＤ１を駆動することができる。また、各ＬＥＤ列はその極性が互いに反対となるように電極に並列接続されているので、電源として交流電源を使用した場合にも、電源の各周期中に必ずどちらかのＬＥＤ列が発光していることになるので、効率のよい発光を行うことができる。

【００２３】

図３には、基板１０上にモノリシックに形成された複数のＬＥＤの部分的な平面図が示されている。また、図４は、図３のＩＶ－ＩＶ断面図が示されている。図３において、ＬＥＤ１の上面には、図１に示されるようにｐ電極２２及びｎ電極２４が形成されている。隣接するＬＥＤ１のｐ電極２２とｎ電極２４との間がエアブリッジ配線２８により接続され、複数のＬＥＤ１が直列接続される。

【００２４】

図４において、各ＬＥＤ１は説明の都合上簡略的に示されている。すなわち、ｎ－ＧａＮ層１４、ｐ－ＧａＮ層２０、ｐ－電極２２、ｎ－電極２４のみが示されている。実際には図１に示されるようにＩｎＧａＮ発光層１６等が存在することは云うまでもない。エアブリッジ配線２８は、ｐ電極２２からｎ電極２４までを空中を介して接続する。これにより、素子表面に絶縁膜を塗布し、この上に電極を形成してｐ電極２２とｎ電極２４とを電気的に接続する方法に比べ、エッチング溝に沿って電極を配置する必要が無くなるので、配線切れや絶縁膜からｎ層、ｐ層へ絶縁材料を構成する元素が熱拡散してＬＥＤ１を劣化させるという問題を回避できる。エアブリッジ配線２８は、ＬＥＤ１間のみならずＬＥＤ１と図示しない電極との間の接続にも使用される。

【００２５】

また、図４に示されるように、各ＬＥＤ１は互いに独立し、電気的に絶縁される必要がある。このため、各ＬＥＤ１はサファイア基板１０上で分離された構成となっている。サファイアはそれ自身絶縁体であるので、ＬＥＤ１をそれぞれ電気的に分離することができる。このように、サファイア基板１０をＬＥＤの電気的な分離を行うための抵抗体として使用することにより、容易かつ確実にＬＥＤの電気的な分離を行うことができる。

【００２６】

なお、発光素子としては、ｐｎ接合を有するＬＥＤの他、ＭＩＳとすることもできる。

【００２７】

図５には、発光装置の他の等価回路図が示されている。図において、２０個のＬＥＤ１が直列接続されて１つのＬＥＤアレイを形成しており、２つのＬＥＤアレイ（合計４０個のＬＥＤ）が電源に並列に接続されている。ＬＥＤ１の駆動電圧は５Ｖに設定されており、各ＬＥＤアレイの駆動電圧は１００Ｖとなっている。２つのＬＥＤアレイは図２と同様に互いに反対極性となるように電源に並列接続されており、電源の極性がいずれであっても必ずどちらかのＬＥＤアレイが発光することになる。

【００２８】

図６には、二次元アレイが具体的に示されている。図２の等価回路図に対応するものである。図において、サファイア基板１０上に合計４０個のＬＥＤ１が形成されており、それぞれ２０個ずつ２組に分けられ、エアブリッジ配線２８により直列接続されて２つのＬＥＤアレイを形成している。より詳細には、各ＬＥＤ１は全て同形の正方形で同サイズであり、１つのＬＥＤアレイは上から６個、７個、７個とそれぞれ直線上に配置され、上から第１列目（６個）と第２列目（７個）は互いに逆向きに形成され、第２列目と第３列目も互いに逆向きに形成される。第１列目と第２列目、第２列目と第３列目は互いに離間して

配置されている。これは、後述するように他方のＬＥＤアレイの列が交互に挿入されるためである。第１列目の右端のＬＥＤ１と第２列目の右端のＬＥＤ１とはエアブリッジ配線２８により接続される。第２列目の左端のＬＥＤ１と第３列目の左端のＬＥＤ１もエアブリッジ配線２８で接続されてジグザグ配列となる。第１列目の左端のＬＥＤ１は基板１０の左上部に形成された電極（パッド）３２にエアブリッジ配線２８で接続され、第３列目の右端のＬＥＤ１は基板１０の右下部に形成された電極（パッド）３２にエアブリッジ配線２８で接続される。２つの電極（パッド）３２もＬＥＤ１と同形の正方形である。他方のＬＥＤアレイは上述した一方のＬＥＤアレイの間隙に互い違いとなるように形成される。すなわち、他方のＬＥＤアレイは上から７個、７個、６個とそれぞれ直線上に配置され、上から第１列目は一方のＬＥＤアレイの第１列目と第２列目の間に形成され、第２列目は一方のＬＥＤアレイの第２列目と第３列目の間に形成され、第３列目は一方のＬＥＤアレイの第３列目の下に形成される。他方のＬＥＤアレイの第１列目と第２列目、及び第２列目と第３列目も互いに逆方向となるように形成され、第１列目の右端のＬＥＤ１は第２列目の右端のＬＥＤ１にエアブリッジ配線２８で接続され、第２列目の左端のＬＥＤ１は第３列の左端のＬＥＤ１にエアブリッジ配線２８で接続されてジグザグ状となる。他方のＬＥＤアレイの第１列目の左端のＬＥＤは基板１０の左上部に形成された電極３２にエアブリッジ配線２８で接続され、第３列目の右端のＬＥＤ１は基板１０の右下部に形成された電極３２にエアブリッジ配線２８で接続される。一方のＬＥＤアレイと他方のＬＥＤアレイの電極３２に対する極性は互いに逆である。発光装置（チップ）の全体形状は長方形である。電源が供給される２つの電極３２は、長方形の対角位置に離間して形成される点も着目されたい。

【００２９】

図７には、図６の回路図が示されている。それぞれのＬＥＤアレイはジグザグ状に屈曲しつつ直列接続され、２つのＬＥＤアレイはジグザグ状の各列が互いの列の間に形成される様子が明らかとなろう。このような配置とすることで、多数のＬＥＤ１を小さな基板１０上に配置することができる。また、４０個のＬＥＤ１に対して電極３２が２個でよいので、この点でも基板１０の使用効率を向上させることができる。また、各ＬＥＤ１を分離するためにＬＥＤ１を個別に形成する場合にはウエハをカットして分離する必要があるのに対し、本実施形態では各ＬＥＤ１の分離をエッチングで行うことができるので、ＬＥＤ１の間隔を狭くすることができる。これにより、サファイア基板１０の大きさをより小さくすることができる。ＬＥＤ１同士の分離は、フォトレジストや反応性イオンエッチング、ウエットエッチングを併用することでＬＥＤ１以外の領域を基板１０に達するまでエッチング除去することで達成される。各ＬＥＤアレイは交互に発光するので、発光効率を向上できるとともに放熱特性も向上させることができる。また、直列接続させるＬＥＤ１の数を変更すれば、全体としての駆動電圧も変更できる。また、ＬＥＤ１の面積を小さくすると、１つのＬＥＤ当たりの駆動電圧を高くすることもできる。ＬＥＤ１を２０個直列に接続した場合、商用電源（１００Ｖ、６０Ｈｚ）で駆動すると、およそ１５０ｍＷの発光出力を得ることができる。この場合の駆動電流としては２０ｍＡ程度である。

【００３０】

なお、図７から分かるように、２つのＬＥＤアレイをジグザグ状に交互に配列する場合、エアブリッジ配線２８に交叉部分３４が必然的に発生する。例えば、他方のＬＥＤアレイの第１列目と第２列目を接続する際に、一方のＬＥＤアレイの第１列目と第２列目を接続するための配線部分と交叉する。しかし、本実施形態のエアブリッジ配線２８は、上述したように基板１０に接着しておらず、基板１０から離れて空中を通過するので、交叉部分３４においてエアブリッジ配線２８同士が接触し、短絡することを容易に回避することができる。エアブリッジ配線２８を用いる利点の一つである。エアブリッジ配線２８は、例えば以下のようにして形成される。すなわち、全面に２μｍの厚さのフォトレジストを塗布し、エアブリッジ配線の形状に穴を開けた後にポストベークする。その上に、真空蒸着でＴｉを１０ｎｍ、Ａｕを１０ｎｍ、この順序で蒸着する。さらにその上の全面に２μｍ厚さでフォトレジストを再度塗布し、エアブリッジ配線を形成する部分のみに穴を開ける

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。次いで、ＴｉとＡｕを電極として電解液中でイオンプレーティング（メッキ）により電極全面に３～５μｍの厚さのＡｕを付着させる。その後、試料をアセトンに浸し、超音波洗浄によりフォトレジストを溶解除去してエアブリッジ配線２８が完成する。

【００３１】

このように、複数のＬＥＤ１を二次元アレイ状に配置することで、基板面積を有効に活用しつつ高駆動電圧、特に商用電源での駆動も可能となるが、二次元アレイのパターンとしてはこの他にも種々のパターンが可能である。一般に、二次元アレイパターンとしては、以下の条件を備えることが望ましい。

【００３２】

（１）各ＬＥＤに均一に電流を流し、均一な発光を得るためには各ＬＥＤの形状、電極位置が同一であることが望ましい。

【００３３】

（２）ウエハをカットしてチップにするためには、各ＬＥＤの辺は直線であることが望ましい。

【００３４】

（３）光取り出し効率を向上させるため、標準的なマウントを使用して周辺からの反射を利用するためにはＬＥＤは平面形状が正方形に近い形状が望ましい。

【００３５】

（４）２つの電極（ボンディングパット）の大きさは１００μｍ角程度で、互いに離れていることが望ましい。

【００３６】

（５）ウエハ面積の有効利用のため、配線、パッドの占める割合は小さい方が望ましい。

【００３７】

もちろん、これらは必須ではなく、例えば各ＬＥＤの形状としては平面形状三角形を用いることも可能であろう。各ＬＥＤの形状が三角形であっても、これらを組み合わせることで全体形状を略正方形とすることができる。以下、二次元アレイパターンの例をいくつか示す。

【００３８】

図８には、合計６個のＬＥＤ１を二次元に配置した例が示されており、図９にはその回路図が示されている。図８の配置は、基本的には図６の配置と同様であり、合計６個のＬＥＤアレイは同数ずつ２組に分けられ、それぞれ直列接続された３個のＬＥＤから構成される。一方のＬＥＤアレイはジグザグ状に配列され、上から第１列目は１個のＬＥＤ１、第２列目は２個のＬＥＤ１が形成される。第１列目のＬＥＤと第２列目の右端のＬＥＤ１はエアブリッジ配線２８で直列接続され、第２列目の２個のＬＥＤ１もエアブリッジ配線２８で直列接続される。基板１０の左上部と左下部に電極（パッド）３２が形成され、第１列目のＬＥＤ１は左上部の電極３２にエアブリッジ配線で接続され、第２列目の左端のＬＥＤ１は左下部の電極３２に接続される。他方のＬＥＤアレイもジグザグ状に配列され、上から第１列目は２個のＬＥＤ１、第２列目は１個のＬＥＤ１が形成される。他方のＬＥＤアレイの第１列目は前記一方のＬＥＤアレイの第１列目と第２列目の間に形成され、他方のＬＥＤアレイの第２列目は前記一方のＬＥＤアレイの第２列目の下方に形成される。第１列目の右端のＬＥＤ１は第２列目のＬＥＤ１にエアブリッジ配線２８で直列接続され、第１列目の２個のＬＥＤ１同士もエアブリッジ配線２８で直列接続される。第１列目の左端のＬＥＤ１は左上部の電極３２にエアブリッジ配線２８で接続され、第２列目のＬＥＤ１は左下部の電極３２にエアブリッジ配線２８で接続される。図９から分かるように、この例でも２つのＬＥＤアレイは互いに並列に電極３２に接続され、かつ、互いに逆極性となるように接続される。したがって、交流電源を供給した場合、２つのＬＥＤアレイは交互に発光することになる。

【００３９】

図１０には、合計１４個のＬＥＤを二次元配置した例が示されており、図１１にはその回路図が示されている。合計１４個のＬＥＤアレイは２組に分けられ、それぞれ直列接続さ

れた７個のＬＥＤから構成される。一方のＬＥＤアレイはジグザグ状に配列され、上から第１列目は３個のＬＥＤ１、第２列目は４個のＬＥＤ１が形成される。第１列目の左端のＬＥＤと第２列目の左端のＬＥＤ１はエアブリッジ配線２８で直列接続され、第１列目の３個のＬＥＤ同士、及び第２列目の４個のＬＥＤ１同士もエアブリッジ配線２８で直列接続される。基板１０の右上部と右下部に電極（パッド）３２が形成され、第１列目の右端のＬＥＤ１は右上部の電極３２にエアブリッジ配線で接続され、第２列目の右端のＬＥＤ１は右下部の電極３２に接続される。他方のＬＥＤアレイもジグザグ状に配列され、上から第１列目は４個のＬＥＤ１、第２列目は３個のＬＥＤ１が形成される。他方のＬＥＤアレイの第１列目は前記一方のＬＥＤアレイの第１列目と第２列目の間に形成され、他方のＬＥＤアレイの第２列目は前記一方のＬＥＤアレイの第２列目の下方に形成される。第１列目の左端のＬＥＤ１は第２列目の左端のＬＥＤ１にエアブリッジ配線２８で直列接続される。第１列目の４個のＬＥＤ１同士、及び第２列目の３個のＬＥＤ１同士も直列接続される。第１列目の右端のＬＥＤ１は右上部の電極３２にエアブリッジ配線２８で接続され、第２列目の右端のＬＥＤ１は右下部の電極３２にエアブリッジ配線２８で接続される。図１１から分かるように、この例でも２つのＬＥＤアレイは互いに並列に電極３２に接続され、かつ、互いに逆極性となるように接続される。したがって、交流電源を供給した場合、２つのＬＥＤアレイは交互に発光することになる。

【００４０】

図６、図８、図１０の二次元パターンに共通する特徴としては、各ＬＥＤ１が略正方形の同形、同サイズであること、２つの電極（パッド）も略正方形であり、隣接形成されていない（離間形成されている）こと、２つのＬＥＤアレイの組み合わせであること、２つのＬＥＤアレイは屈曲しつつチップ上に互いに交錯するように形成されること、２つのＬＥＤアレイは互いに逆極性となるように電極に接続されること、等である。

【００４１】

図１２には、平面形状が三角形のＬＥＤを二次元配列した場合の例が示されており、図１３にはその回路図が示されている。図１２において、合計６個のＬＥＤ１ａ、１ｂ、１ｃ、１ｄ、１ｅ、１ｆがその平面形状が三角形状となるように形成されている。ＬＥＤ１ａとＬＥＤ１ｅが三角形の一辺で対向して２つで略正方形となるように配置され、ＬＥＤ１ｂと１ｆが対向して２つで略正方形となるように配置される。また、ＬＥＤ１ｄと電極３２が対向して接続し、ＬＥＤ１ｃと電極３２が対向して接続する。２つの電極３２もＬＥＤと同様に平面形状が三角形状であり、同様に略正方形となるように配置される。ＬＥＤ同士の対向する辺はｎ電極２４を構成し、すなわち、対向する２つのＬＥＤはｎ電極２４を共有する。ＬＥＤと電極３２もｎ電極接続である。この配置も、上述した例と同様に合計６個のＬＥＤは２組に分けられる。一方のＬＥＤアレイは、ＬＥＤ１ａ、ＬＥＤ１ｂ、ＬＥＤ１ｃからなるアレイであり、ＬＥＤ１ａのｐ電極２２は電極３２にエアブリッジ配線２８で接続され、そのｎ電極２４はＬＥＤ１ｂのｐ電極２２とエアブリッジ配線２８で接続される。ＬＥＤ１ｂのｎ電極２４はＬＥＤ１ｃのｐ電極２２とエアブリッジ配線２８で接続される。ＬＥＤ１ｃのｎ電極２４は電極３２に接続される。他方のＬＥＤアレイは、ＬＥＤ１ｄ、ＬＥＤ１ｅ、ＬＥＤ１ｆから構成され、電極３２とＬＥＤ１ｆのｐ電極２２はエアブリッジ配線２８で接続され、ＬＥＤ１ｆのｎ電極２４はＬＥＤ１ｅのｐ電極２２とエアブリッジ配線２８で接続され、ＬＥＤ１ｅのｎ電極２４とＬＥＤ１ｄのｐ電極２２はエアブリッジ配線２８で接続され、ＬＥＤ１ｄのｎ電極２４は電極３２に接続される。

【００４２】

図１３において、一方のＬＥＤアレイを構成するＬＥＤ１ａと他方のＬＥＤアレイを構成するＬＥＤ１ｅのｎ電極が接続されており、一方のＬＥＤアレイを構成するＬＥＤ１ｂと他方のＬＥＤアレイを構成するＬＥＤ１ｆのｎ電極が接続されている点にも着目されたい。２組のＬＥＤアレイのいくつかのｎ電極を共有することで、回路配線を削減することができる。また、この例においても、２つのＬＥＤアレイは並列に電極３２に接続され、かつ、互いに逆極性となるように接続される。また、各ＬＥＤは同形、同サイズであり、各

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ＬＥＤを一つの辺で対向させるとともに電極３２も三角形状とすることでＬＥＤ及び電極を高密度に形成して必要な基板面積を小さくすることができる。

【００４３】

図１４には、平面形状が三角形のＬＥＤを二次元配列した他の例が示されており、図１５にはその回路図が示されている。この例では、合計１６個のＬＥＤ１ａ～１ｒが二次元形成されている。ＬＥＤ１ａと１ｊ、１ｂと１ｋ、１ｃと１ｍ、１ｄと１ｎ、１ｅと１ｐ、１ｆと１ｑ、１ｇと１ｒがそれぞれ三角形の一つの辺で対向する。対向する辺にはｎ電極２４が共通形成されている。また、ＬＥＤ１ｉと電極３２が対向し、ＬＥＤ１ｈと電極３２が対向する。一方のＬＥＤアレイはＬＥＤ１ａ、１ｂ、１ｃ、１ｄ、１ｅ、１ｆ、１ｇ、１ｈから構成され、他方のＬＥＤアレイはＬＥＤ１ｒ、１ｑ、１ｐ、１ｎ、１ｍ、１ｋ、１ｊ、１ｉから構成される。ＬＥＤ１ｂのｎ電極２４はエアブリッジ配線２８によりＬＥＤ１ｃのｐ電極２２に接続され、ＬＥＤ１ｅのｎ電極２４もエアブリッジ配線２８によりＬＥＤ１ｆのｐ電極２２に接続される。また、ＬＥＤ１ｑのｎ電極２４もエアブリッジ配線２８によりＬＥＤ１ｐのｐ電極２２に接続され、ＬＥＤ１ｍのｎ電極２４もエアブリッジ配線２８によりＬＥＤ１ｋのｐ電極２２に接続される。図１４においても、図１２と同様に交叉部分が生じるが、エアブリッジ配線２８により短絡を回避できる。また、この例においても２組のＬＥＤアレイのいくつかのｎ電極２４を共有構造とすることで必要な配線を削減している。また、この例においても２つのＬＥＤアレイは並列で互いに逆極性で電極３２に接続されており、交流駆動が可能である。図１２においては合計６個のＬＥＤの場合、図１４においては合計１６個のＬＥＤの場合について示したが、他の個数のＬＥＤでも同様に二次元配列できる。本願出願人は、３８個のＬＥＤを二次元配列した発光装置も作成している。

【００４４】

以上、交流駆動の場合について説明したが、直流駆動も可能であることは言うまでもない。この場合、ＬＥＤアレイを互いに逆極性となるように電極に接続するのではなく、直流電源の極性の向きに合わせてＬＥＤアレイを順方向に接続すればよい。複数のＬＥＤを直列接続することで、高電圧駆動が可能である。以下、直流駆動の場合についても説明する。

【００４５】

図１６には、２個のＬＥＤを直列接続した例が示されており、図１７にはその回路図が示されている。各ＬＥＤ１は平面形状が矩形状であり、２個のＬＥＤ間はエアブリッジ配線２８で接続される。電極３２は各ＬＥＤ１の近傍に形成されており、電極３２とＬＥＤ１とで長方形の領域を形成する。すなわち、電極３２は長方形領域の一部を占有し、長方形領域の他の領域にＬＥＤ１が形成されている。

【００４６】

図１８には、合計４個のＬＥＤを二次元配列した例が示されており、図１９にはその回路図が示されている。図１６のＬＥＤ１を２個に分割し、それぞれを並列に接続したものである。２個のＬＥＤからなるＬＥＤアレイを２組並列に順方向接続したと云うこともできる。ＬＥＤ１ａと１ｂで一つのＬＥＤアレイを構成し、ＬＥＤ１ｃと１ｄでもう一つのＬＥＤアレイを構成する。ＬＥＤ１ａとＬＥＤ１ｃはｐ電極２２及びｎ電極２４を共有し、ＬＥＤ１ｂとＬＥＤ１ｄもｐ電極２２及びｎ電極２４を共有する。この構成によれば、図１６に比べて電流が均一化する効果がある。

【００４７】

図２０は、合計３個のＬＥＤを二次元配列した例が示されており、図２１にはその回路図が示されている。ＬＥＤ１ａ、１ｂ、１ｃは同形ではなく、ＬＥＤ１ａの一部に電極３２が形成されている。ＬＥＤ１ａのｎ電極２４とＬＥＤ１ｂのｐ電極はＬＥＤ１ｂの上を跨ぐエアブリッジ配線２８で接続される。各ＬＥＤの形状及び配置を工夫することで、３個のＬＥＤであっても発光装置（チップ）全体の外観形状を略正方形とすることができる。

【００４８】

図２２には、合計６個のＬＥＤを二次元配列した例が示されており、図２３にはその回路

図が示されている。各ＬＥＤ１ａ～１ｆは同形、同サイズである。ＬＥＤ１ａ～１ｆは直列接続される。ＬＥＤ１ａ～１ｃは直線上に配置され、ＬＥＤ１ｄ～１ｆは他の直線上に配置される。ＬＥＤ１ｃとＬＥＤ１ｄはエアブリッジ配線２８で接続される。この例においても、チップの全体形状を略正方形とすることができる。

【００４９】

図２４には、合計５個のＬＥＤを二次元配列した例が示されており、図２５にはその回路図が示されている。ＬＥＤ１ａ～１ｅは同形（長方形）、同サイズである。この例においても、全体形状を略正方形とすることができる。

【００５０】

以上、本発明の実施形態について説明したが、本発明はこれに限定されるものではなく種々の変更が可能である。特に、複数の発光素子（ＬＥＤ等）を二次元配置する場合のパターンは上述したパターン以外にも可能である。この場合、隣接する発光素子間で電極を共有して配線を少なくすること、全体形状を正方形あるいは長方形とすること、複数組の発光素子アレイを電極に並列接続すること、交流駆動の場合に複数組の発光素子アレイを互い逆極性とすること、複数組の発光素子アレイをそれぞれジグザグ状に屈曲させて組み合わせること、等が好適である。

【００５１】

図２６～図３１には、これらの変更例のいくつかが例示されている。図２６は交流駆動の場合の二次元配置であり、合計４０個のＬＥＤが配置されている。図２７はその回路図である。図６と異なる点は、２組のＬＥＤアレイのいくつかがｎ電極２４を共有する点である（図５参照）。例えば、一方のＬＥＤアレイの第１列の右端から２番目に位置するＬＥＤ（図中αで示す）のｎ電極２４は、他方のＬＥＤアレイの第１列の右端に位置するＬＥＤ（図中βで示す）のｎ電極２４と共有されている。なお、ＬＥＤアレイの端部（図中γ部分）におけるエアブリッジ配線２８は、交叉させることなく共通形成されている。

【００５２】

図２８は、交流駆動の場合の二次元配置であり、合計１４個のＬＥＤが配置されている。図２９はその回路図である。図１０と異なる点は、２組のＬＥＤアレイのいくつかがｎ電極２４を共有する点である。例えば、一方のＬＥＤアレイの第１列の左端のＬＥＤ（図中αで示す）のｎ電極２４は、他方のＬＥＤアレイの第１列の右端から２番目に位置するＬＥＤ（図中βで示す）のｎ電極２４と共有されている。また、端部（図中γ部分）におけるエアブリッジ配線２８は共通形成されている。

【００５３】

図３０は、交流駆動の場合の二次元配置であり、合計６個のＬＥＤが配置されている。図３１はその回路図である。この例においても、端部（γ部）のエアブリッジ配線２８が共通形成されている。この構成も、一方のＬＥＤアレイにおけるｎ電極２４と他方のＬＥＤアレイにおけるｎ電極２４が共有されていると云うことができる。

【００５４】

【発明の効果】

以上説明したように、本発明によれば、高い駆動電圧で駆動し発光させることができる。

【図面の簡単な説明】

【図１】発光素子（ＬＥＤ）の基本構成図である。

【図２】発光装置の等価回路図である。

【図３】２個のＬＥＤの平面図である。

【図４】図３のＩＶ－ＩＶ断面図である。

【図５】発光装置の他の等価回路図である。

【図６】４０個のＬＥＤを二次元配列した説明図である。

【図７】図６の回路図である。

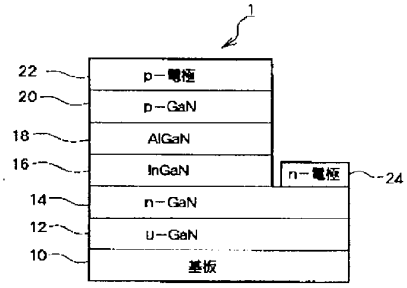
【図８】６個のＬＥＤを二次元配列した説明図である。

【図９】図８の回路図である。

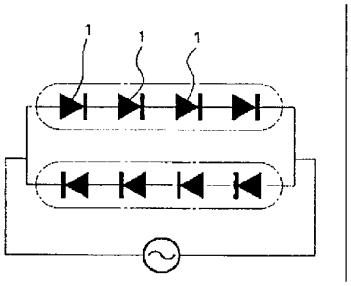
【図１０】１４個のＬＥＤを二次元配列した説明図である。

【図１１】図１０の回路図である。
【図１２】６個のＬＥＤを二次元配列した説明図である。
【図１３】図１２の回路図である。
【図１４】１６個のＬＥＤを二次元配列した説明図である。
【図１５】図１４の回路図である。
【図１６】２個のＬＥＤを配列した説明図である。
【図１７】図１６の回路図である。
【図１８】４個のＬＥＤを二次元配列した説明図である。
【図１９】図１８の回路図である。
【図２０】３個のＬＥＤを二次元配列した説明図である。
【図２１】図２０の回路図である。
【図２２】６個のＬＥＤを二次元配列した説明図である。
【図２３】図２２の回路図である。
【図２４】５個のＬＥＤを二次元配列した説明図である。
【図２５】図２４の回路図である。
【図２６】他の二次元配置説明図である。
【図２７】図２６の回路図である。
【図２８】他の二次元配置説明図である。
【図２９】図２８の回路図である。
【図３０】他の二次元配置説明図である。
【図３１】図３０の回路図である。
【符号の説明】
１０　基板（ウエハ）、１２　ｕ－ＧａＮ層、１４　ｎ型ＧａＮ層、１６　ＩｎＧａＮ発光層、１８　ＡｌＧａＮ層、２０　ｐ－ＧａＮ層、２２　ｐ－電極、２４　ｎ－電極。

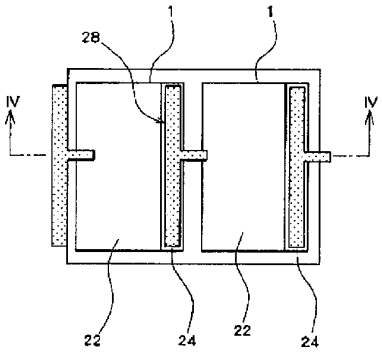
【図1】



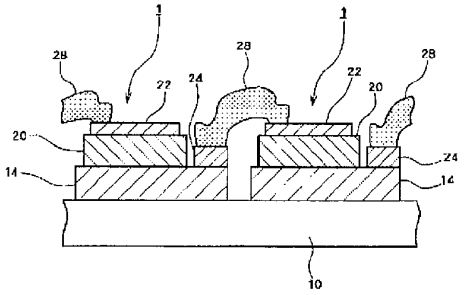
【図2】



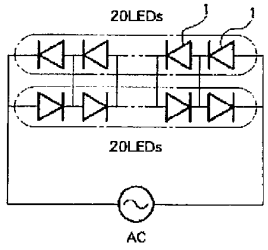
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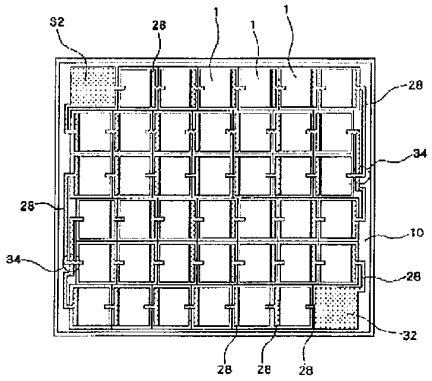
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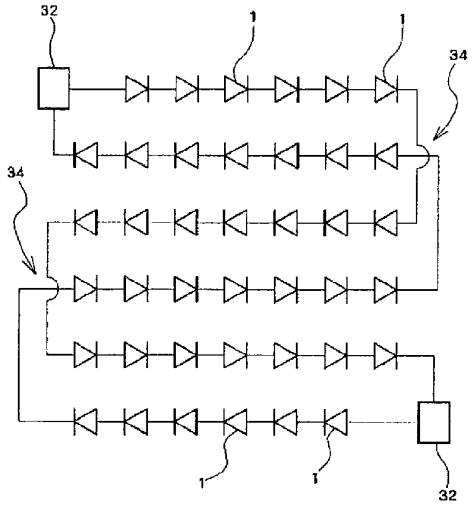
【図5】



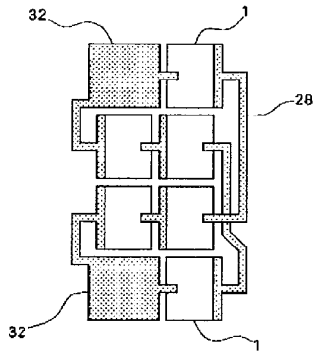
【図6】



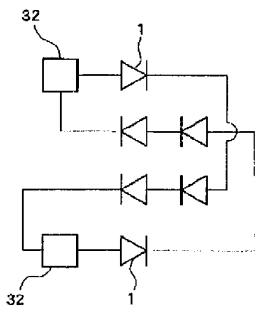
【図7】



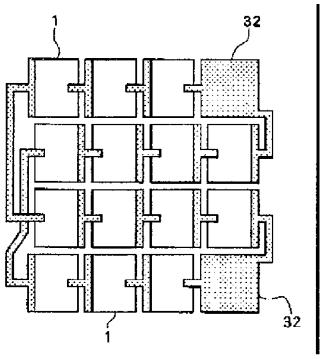
【図8】



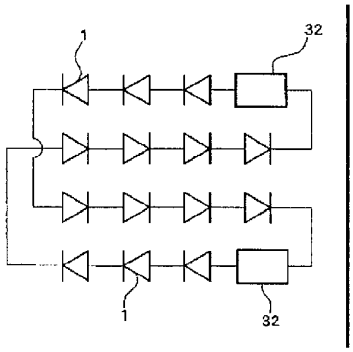
【図9】



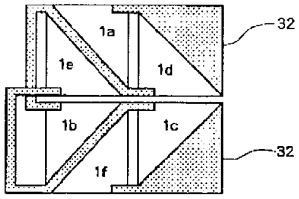
【図10】



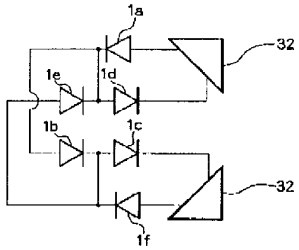
【図11】



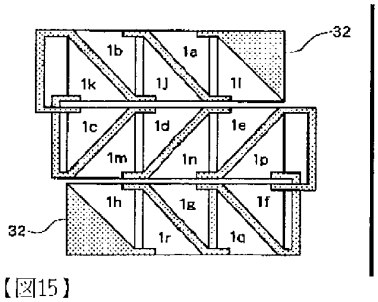
【図12】



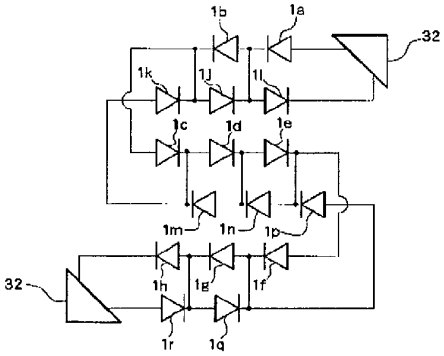
【図13】



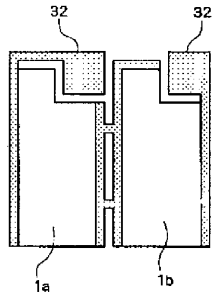
【図14】



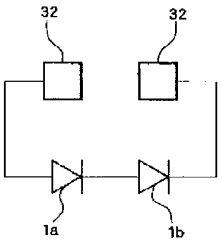
【図15】



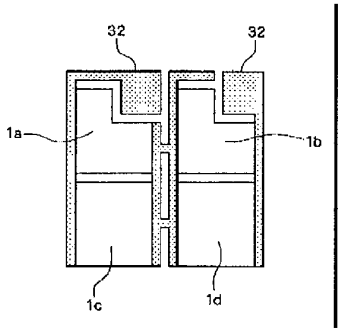
【図16】



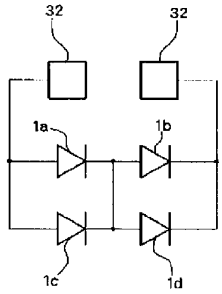
【図17】



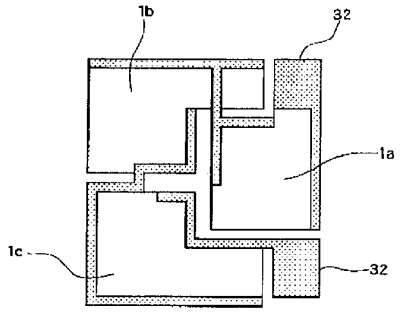
【図18】



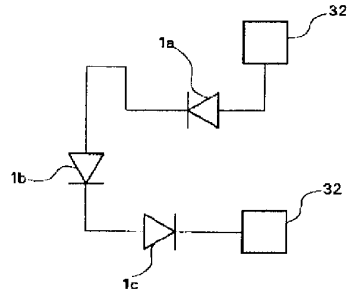
【図19】



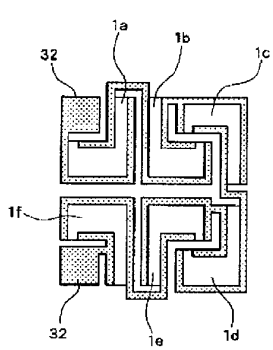
【図20】



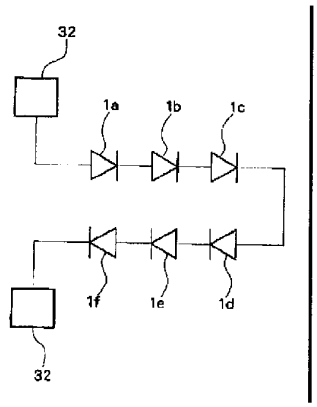
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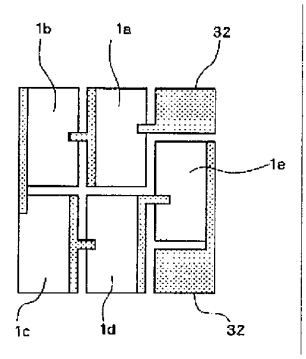
【図22】



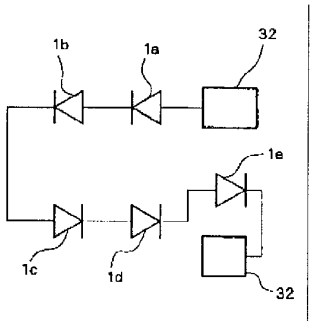
【図23】



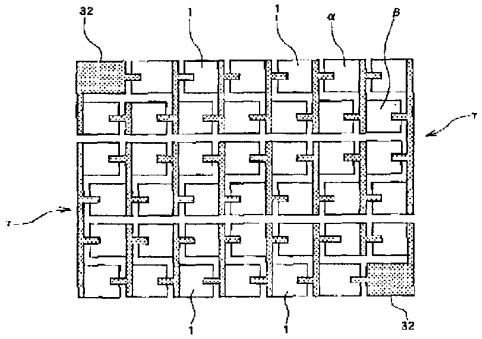
【図24】



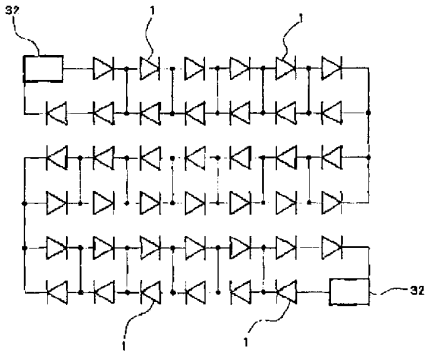
【図25】



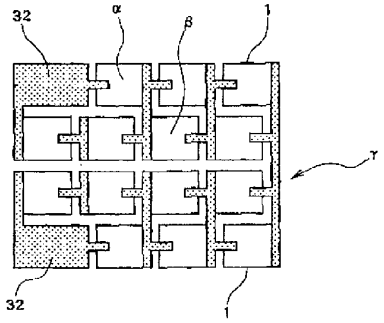
【図26】



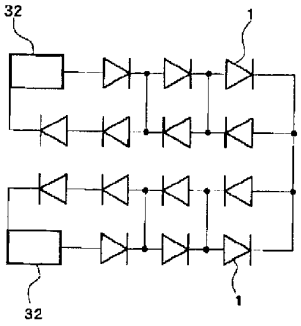
【図27】



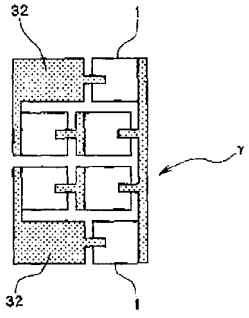
【図28】



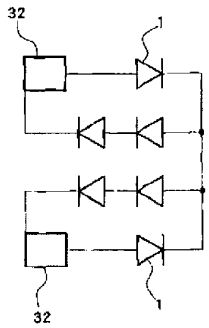
【図29】



【図30】



【図31】



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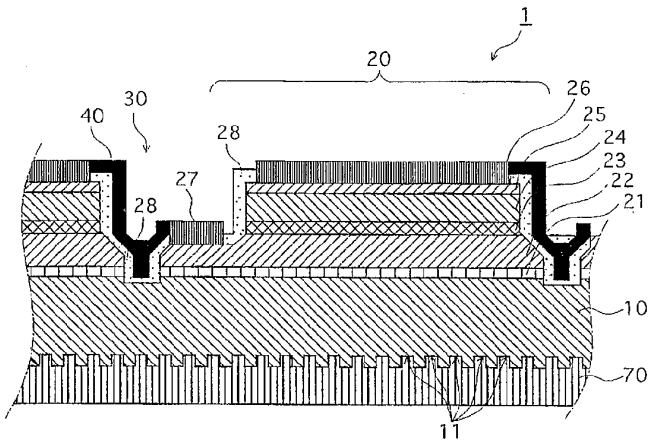
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(54) Title: SEMICONDUCTOR LIGHT EMITTING DEVICE, METHOD OF MANUFACTURING THE SAME, AND LIGHTING APPARATUS AND DISPLAY APPARATUS USING THE SAME



(57) Abstract: The present invention aims to provide a semiconductor light emitting device that may be firmly attached to a substrate with maintaining excellent light emitting efficiency, and a manufacturing method of the same, and a lighting apparatus and a display apparatus using the same. In order to achieve the above object, the semiconductor light emitting device according to the present invention includes a luminous layer, a light transmission layer disposed over a main surface of the luminous layer, and having depressions on a surface facing away from the luminous layer, and a transmission membrane disposed on the light transmission layer so as to follow contours of the depressions, and light from the luminous layer is irradiated so as to pass through the light transmission layer and the transmission membrane.

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DESCRIPTION

SEMICONDUCTOR LIGHT EMITTING DEVICE, METHOD OF MANUFACTURING THE SAME, AND LIGHTING APPARATUS AND DISPLAY APPARATUS USING THE SAME

Technical Field

The present invention relates to a semiconductor light emitting device and a method of manufacturing the same, as well as a lighting apparatus and a display apparatus using the same.

Background Art

Lighting apparatuses with light emitting diodes (LEDs) have been gaining attention as a new light source because of excellent properties in terms of light emitting efficiency and longevity in comparison with incandescent lamps or halogen lamps. In order to improve light output of this kind of lighting apparatus, a quick solution is to mount LEDs in high density. However, this solution is not very realistic due to current issues regarding production cost and heat dissipation in driving when LEDs are mounted in high density. A more realistic solution in order to enhance the light output is to make luminous efficiency of an LED as high as possible. Various attempts have been made to this end, and two key parameters in making such attempts are Internal Quantum Efficiency (IQE) and External Quantum Efficiency (EQE).

The IQE is a parameter indicating the amount of light generated in a luminous layer of an LED to the amount of electric

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power that is supplied to the LED. The IQE is affected by the crystallinity of a semiconductor and the structure of the luminous layer that constitute the LED.

On the other hand, the EQE is a parameter indicating an amount of light emitted outside the LED to the amount of supplied electric power, and expressed by a product of the IQE and light extraction efficiency (a proportion of the amount of light emitted outside the LED in the amount of light generated in the LED). The light extraction efficiency is affected by the shape of a bare chip, the material that covers the bare chip, and the shape of the material. In order to improve the light extraction efficiency, it is common to cover a bare chip with resin so as to minimize the refractive index difference at a boundary between the bare chip and outside of the bare chip as much as possible.

Moreover, in a case of lighting apparatuses using LEDs, it is common for a light extracting surface of a bare chip to have depressions so that an incident angle of light on the light extracting surface is not fixed to one angle, thus improving the light extraction efficiency (Japanese Patent No. 2836687, and *Compound Semiconductor*, Vol.8, No.1, pp.39-42, 2002).

As a method of mounting a bare chip on a mounting substrate, flip-chip bonding as shown in FIG.20 is commonly employed. In the flip-chip bonding as illustrated in FIG.20, a vacuum collet 1300 sticks to a light extracting surface of a bare chip 1100, and the bare chip 1100 is joined with a wiring layer 1210 of a mounting substrate 1200 using ultrasonic bonding. By mounting the bare chip 1100 in this way, the distance between

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a light emitting layer of the bare chip 1100 and the mounting substrate 1200 is shortened, thus making it possible to effectively dissipate the heat generated in the light emitting layer. In other words, the flip-chip bonding is very effective for a lighting apparatus that requires LEDs in high density, in order to ensure a high heat dissipation capacity.

However, mounting bare chips having depressions on the light extracting surface using the flip-chip bonding often causes problems such as decreases in positioning accuracy and bonding strength, and destruction of the depressions. Specifically, as shown in an enlarged view in the circle in FIG.20, depressions 1111 make it difficult for the vacuum collet 1300 to stick to the bare chip 1100 without fail, and for ultrasonic waves to propagate from the vacuum collet 1300 to the bare chips 1100 sufficiently for bonding. The same kind of problems also occur in display apparatuses having bare chips.

Disclosure of the Invention

In order to solve the above noted problems, the present invention aims to provide a semiconductor light emitting device that may be firmly attached to a substrate with maintaining excellent light emitting efficiency, and a manufacturing method of the same, and a lighting apparatus and a display apparatus using the same.

In order to achieve the above object, a semiconductor light emitting device having a luminous layer according to the present invention comprises a light transmission layer disposed over a main surface of the luminous layer, and having

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depressions on a surface facing away from the luminous layer, and a transmission membrane disposed on the light transmission layer so as to follow contours of the depressions, and light from the luminous layer is irradiated so as to pass through the light transmission layer and the transmission membrane.

The above semiconductor light emitting device has the depressions on a surface of the light transmission layer facing away from the luminous layer. Accordingly, the light emitted from the luminous layer is scattered by the depressions or transmitted efficiently, and thus high light extraction efficiency is maintained, as well as high light emission efficiency. Further, the depressions of the semiconductor light emitting device according to the present invention are filled and covered by the membrane, and therefore it is possible to suppress destruction of the depressions by ultrasonic waves applied when the bare chip is mounted to a mounting substrate. Because of this, with the semiconductor light emitting device according to the present invention, it is possible to obtain high light emission efficiency.

Moreover, with the semiconductor light emitting device according to the present invention, a loss of ultrasonic energy is not large because of the above membrane, even when the chip is mounted to the mounting substrate.

Accordingly, the semiconductor light emitting device according to the present invention has an advantage to be able to firmly attach to the mounting substrate while maintaining a high emission efficiency.

Note that it is possible to mount the chip to the mounting substrate using flip-chip bonding.

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The membrane covers the surface so as to follow the contours of the depressions, without including air or gap. Further, by saying the light transmission layer is disposed over the main surface of the luminous layer, it indicates that the light transmission layer may be disposed either directly on the main surface of the luminous layer, or indirectly above the main surface of the luminous layer.

Further, a semiconductor light emitting device usually has a structure that plural layers are formed on the substrate. The above depressions do not necessarily have to be on a surface of a layer out of the plural layers. For example, the depressions may be formed on one of the main surface of the substrate in a case of the semiconductor light emitting device that irradiate light from the luminous layer through the substrate.

When formed irregularly, the depressions serve a function of light diffusion. When the depressions are at a regular interval, a structure of such depressions is called a photonic crystal (PC) or a photonic band gap (PBG) structure, depending on how the depressions are formed. The PC and PBG structures, in general, are a cyclic structure in which depressions and projections appear cyclically at a micoron to $\lambda/4$ (λ is a wavelength in the medium) order on a surface, and have a characteristic that light having a specific wavelength is selectively reflected and transmitted. Therefore, when the semiconductor light emitting device according to the present invention has the light transmission layer having the depression in either the PC or PBG structure, it is possible to realize a function of allowing the light

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to be transmitted easily in the light transmission layer.

The above semiconductor light emitting device may be such that the membrane is formed so as to follow the contours of the depressions on the surface of the light transmission layer. However, it is more desirable that the surface of the membrane facing away from the light transmission layer is substantially flat. Specifically, when mounting the above semiconductor light emitting device to a mounting substrate, the vacuum collet sticks to a surface, from which the light is irradiated, of the device, as described above. If the surface to which the vacuum collet sticks is substantially flat, it is possible that the vacuum collet sticks more firmly. Therefore, it is possible to mount the above semiconductor light emitting device to the mounting substrate more accurately.

A main component of the membrane in the above semiconductor light emitting device may be one of polyimide, epoxy, silicone, and glass. When the glass is used as a material of the membrane, it is possible to use glass by the sol-gel method or low-melting glass. Specific examples of the glass material include (1) a glass material using metal alkoxide (such as tetramethoxysilane and tetraethoxysilane) as starting material, (2) a glass material made from polymer ceramic precursor such as perhydropolysilazane, and (3) a glass material made from such as phosphorus oxide and boronic oxide.

With any of the above listed glass materials, it is possible to form a glass layer (membrane) whose upper surface is substantially flat and filling the depressions, by applying the glass material on the depressions using such as potting

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and spin-coating, drying the glass material, and baking the glass material at a temperature of several hundred degrees centigrade.

It is also desirable that the membrane contains a luminous substance that is excited by the light from the luminous layer. It is especially desirable for a lighting apparatus using the semiconductor light emitting device according to the present invention, if the luminous substance contained in the membrane is a material that is able to convert the light from the luminous layer into the white light (such as a phosphor material).

In order to maintain high light extracting efficiency for the above semiconductor light emitting device, it is also desirable that the depressions on the surface of the light transmission layer are at an interval equal to or greater than $\lambda/4$, λ being a wavelength of the light from the luminous layer.

The luminous layer of the semiconductor light emitting device is generally disposed over a transmission substrate in a state being sandwiched between plural layers such as clad layers, contact layers, and buffer layers. The present invention may also be such that the light transmission substrate as a part or all of the light transmission layer has the depressions on one of main surfaces. It is desirable that the light transmission substrate is made of a material having a refractive index that is substantially equal to a refractive index of the luminous layer, because it is effective to maintain high light extraction efficiency. Specifically, the material for the light transmission substrate may be selected from a group of GaN, SiC, and AlN.

The above structure that is characteristics to the

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present invention may be applied to a light emitting diode device, as well as a Vertical Cavity Surface Emitting Laser device, a Resonant Cavity Light Emitting Diode device, and a Surface Mount Device.

Further, a method of manufacturing the semiconductor light emitting device according to the present invention comprises steps of forming a light transmission layer over a multi-layered body in which the luminous layer is sandwiched between a plurality of layers, the light transmission layer having depressions on a surface facing away from the luminous layer, and forming a transmission membrane on the light transmission layer so as to follow contours of the depressions.

With the above method of manufacturing the semiconductor light emitting device according to the present invention, it is possible to obtain a semiconductor light emitting device having high light extraction efficiency, because the depressions is formed on the surface of the light transmission layer facing away from the luminous layer. Further, the transmission membrane is formed on the light transmission layer so as to fill the depressions, and therefore it is possible to mount the chip firmly with protecting the depressions from destruction when the chip is mounted to the mounting substrate. Specifically, with the above manufacturing method, it is possible to increase the accuracy in mounting when the vacuum collet sticks to the chip, and to reduce a loss of ultrasonic energy in the depressions when the ultrasonic waves are applied.

Accordingly, with the above described method of manufacturing the semiconductor light emitting device

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according to the present invention, a semiconductor light emitting device that has high light emitting efficiency and may be attached to the substrate firmly may be obtained.

As described in the above, the depressions may serve different functions according to a state of the depressions. When formed irregularly, the depressions serve a function of light diffusion. When the depressions are formed regularly at a fixed interval, a structure of such depressions is called a photonic crystal (PC) or a photonic band gap (PBG) structure.

In the method of manufacturing the semiconductor light emitting device according to the present invention, it is also desirable that the membrane contains a luminous substance that is excited by the light from the luminous layer. It is especially desirable that the membrane is polished to a preferred thickness so that the device may irradiate the white light having a desirable wavelength.

Further, a lighting apparatus according to the present invention is such that the semiconductor light emitting device according to the present invention is mounted to the mounting substrate.

The above lighting apparatus has the semiconductor light emitting device including the light transmission layer having the depressions on the surface and the membrane that covers the light transmission layer, and therefore it is possible to maintain high light emitting efficiency and to firmly attach the semiconductor light emitting device to the mounting substrate.

Therefore, the lighting apparatus according to the present invention has high light emitting efficiency and stable

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quality.

As described above, the semiconductor light emitting device according to the present invention has the light transmission layer having a surface with the depressions is disposed over the luminous layer. Thus, it is possible to maintain high light extracting efficiency as well as high light emitting efficiency. Further, because the membrane is disposed over the surface so as to fill the depressions, it is possible to realize firm attachment without destroying the depressions when the semiconductor light emitting device is mounted to the mounting substrate.

Further, with the method of manufacturing the semiconductor light emitting device according to the present invention, the light transmission layer having a surface with depressions is formed over the luminous layer on a side that the device irradiate the light, and then the membrane is formed so as to follow the contours of the depressions. Therefore, it is possible to manufacture the semiconductor light emitting device having the above described advantages easily.

In addition, the lighting apparatus according to the present invention has high light emitting efficiency and stable quality, because the above explained semiconductor light emitting device is mounted to the mounting substrate.

A main component of the membrane in the above semiconductor light emitting device membrane may be one of polyimide, epoxy, silicone, glass by the sol-gel method, and low-melting glass. Specific examples of the glass material include (1) a glass material using metal alkoxide (such as tetramethoxysilane and tetraethoxysilane) as starting

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material, (2) a glass material made from polymer ceramic precursor such as perhydropolysilazane, and (3) a glass material made from such as phosphorus oxide and boronic oxide.

With any of the above listed glass materials, it is possible to form a glass layer (membrane) whose upper surface is substantially flat and filling the depressions, by applying the glass material on the depressions using such as potting and spin-coating, drying the glass material, and baking the glass material at a temperature of several hundred degrees centigrade.

Brief Description Of The Drawings

FIG.1 is a perspective view of a LED chip 1, according to a first embodiment of the present invention.

FIG.2A is a partial sectional view of the LED chip 1.

FIG.2B is a circuit wiring diagram of the LED chip 1.

FIG.3 is a process drawing illustrating a manufacturing process of the LED chip 1.

FIG.4 is a process drawing illustrating a manufacturing process of the LED chip 1.

FIG.5A is a perspective view of a LED module 100 viewed from outside.

FIG.5B is a partial sectional view of the LED module 100.

FIG.6 is a schematic view illustrating a step of flip-chip bonding of the LED chip 1 to a mounting substrate 110.

FIG.7A is a front view of the mounting substrate 110.

FIG.7B is a layout drawing of pads on a LED chip mount unit 1a.

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FIG.8A is a partial sectional view of a lighting apparatus 200 according to the first embodiment, and FIG.8B is a bottom view of the same.

FIG.9 illustrates a process drawing illustrating an attachment process of a LED module 100 to a socket 210 of the lighting apparatus 200.

FIG.10 shows emission spectrum of the lighting apparatus 200.

FIG.11A illustrates a partial sectional view of an LED chip 3 according to the second embodiment.

FIG.11B illustrates configuration of a depression 326a of the bare chip 3.

FIG.12 illustrates manufacturing steps of an LED chip 3.

FIG.13A illustrates a partial sectional view of a mounting substrate 410 on which an LED module 3 is mounted, and FIG.13B

FIG.14 shows an emission spectrum of a lighting apparatus having the LED chip 3.

FIG.15A is a perspective view of an LED display apparatus according to a third embodiment of the present invention, and FIG.15B is a sectional view to illustrate a part indicated by B in FIG.15A.

FIG.16A is a perspective view of a Vertical Cavity Surface Emitting Laser (VCSEL) device 7 according to a fourth embodiment according to the present invention, and FIG.16B is a partial sectional view of the VCSEL device 7.

FIG.17 illustrates manufacturing steps of the VCSEL device 7.

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FIG.18 also illustrates manufacturing steps of the VCSEL device 7.

FIG.19 is a sectional view illustrating a Surface Mount Device as a modified example.

FIG.20 is a schematic view showing steps in mounting a conventional LED chip 1100 to a mounting substrate 1210.

Best Mode for Carrying Out the Invention

The following describes preferred embodiments of the present invention with reference to the drawings.

[First Embodiment]

In a first embodiment, an LED bare chip (hereinafter referred to as the LED chip) 1 is used as an example of semiconductor light emitting devices.

[Structure of LED Chip 1]

The LED chip 1 is explained with reference to FIGs.1 and 2. FIG.1 shows a perspective view. FIG.2A shows a partial sectional view, and FIG.2B shows a circuit wiring diagram, of the LED chip 1.

As shown by FIG.1, the LED chip 1 is such that plural light-emitting elements 20 are formed on a non-doped GaN substrate 10. The light emitting elements 20 are disposed on the substrate 10 in a matrix of 7 × 5 in x and y directions respectively to form total 35 regions on the substrate. A size of one light emitting element 20 is 285 μm in x direction, and 400 μm in y direction. A size of the LED chip 1 is 2 mm × 2 mm, for example.

Each of the light emitting elements 20 on the LED chip 1 constitutes a diode structure, and is separated from other

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light emitting elements 20 by separation grooves 30, and a bridge wiring 40 electrically connects the 35 diode structures in series.

As shown in FIG.1, a cathode electrode 50 and an anode electrode 60 on each of a pair of opposing corners of the LED chip 1. These electrodes 50 and 60 are an n-electrode and a p-electrode, respectively, of the light emitting elements 20 that is positioned at the both edges of the 35 light emitting elements 20 serially connected by the bridge wiring 40.

Further, as shown in an enlarged part in FIG.1, a lower surface of the non-doped GaN substrate 10 has depressions 11, and a membrane 70 covers the depressions. There is no gap between the membrane 70 and the non-doped GaN substrate 10, even at bottoms of the depressions 11. In other words, a surface having depressions of the non-doped GaN substrate 10 is densely covered with the membrane 70.

A negative direction along a z-axis in FIG.1 (downside of the drawing) is a direction in which light from the LED chip 1 is irradiated. The depressions 11 on the substrate 10 are formed in order that the irradiated light is easily diffused or transmitted and to virtually lower the refractive index difference at the boundary (a irradiation surface). Details regarding this are described in the patent and non-patent references cited in the above, and further explanation is not given here.

As shown in FIG.2A, when the LED chip 1 is viewed in section, a GaN buffer layer 21 (30 nm thick), an n-GaN clad layer 22 (Si doped 3×10^{18} cm^{-3}, 2 μm thick), a (InGaN/GaN) ×6 luminous layer 23 (InGaN is 2 nm thick, and GaN is 8 nm),

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a p-GaN clad layer 24 (Mg doped 3×10^{19} cm^{-3}, 200 nm thick), and then a p-GaN contact layer 25 (Mg doped 3×10^{19} cm^{-3}, 50 nm thick) are layered on the non-doped GaN substrate 10 in a stated order, and finally p-electrodes 26 made of Rh/Pt/Au are formed on a top of the layers.

The (InGaN/GaN)×6 luminous layer 23 indicates a multiplex quantum well structure luminous layer at 6 periods of InGaN/GaN, and irradiates blue light having a wavelength of 460 nm in driving the LED chip 1.

A refractive index of the non-doped GaN substrate 10 is around 2.5, which is substantially the same as a refractive index of the (InGaN/GaN) × 6 luminous layer 23. Therefore, the non-doped GaN substrate 10 is more effective to improve the light extraction efficiency in comparison with a conventional LED chip that utilizes a sapphire (refractive index = 1.7).

The separation grooves 30 are made so as to reach the non-doped GaN substrate 10, and a Si_3N_4 membrane 28 as an insulating film covers a surface of the separation grooves 30. On the shelf shaped n-GaN clad layer 22, n-electrodes 27 made of Ti/Au are formed at the boundary between the light emitting element 20 and the separation grooves 30. The bridge wiring 40 made of Ti/Pt/Au connects the n-electrodes 27 to the n-electrodes 26 on the light emitting element 20 that is next to the n-electrodes 27, in one-to-one relation.

On the other hand, the non-doped GaN substrate 10 has the minute depressions 11 having a square-shaped cross-section (the depressions are at an interval of 1 μm, for example) on all over the lower surface. By having the depressions 11 on

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the surface of the non-doped GaN substrate 10, the irradiated light from the (InGaN/GaN) × 6 luminous layer 23 is easily diffused or transmitted. Further, as described above, the membrane 70 is formed on the surface of the non-doped GaN substrate 10 so as to fill the depressions 11. The membrane 70 is mainly made of polyimide resin that transmits light, and contains yellow phosphor material such as $(Sr, Ba)_2SiO_4:Eu^{2+}$ and ultrafine particles such as SiO_2 dispersed in the membrane. The membrane 70 is formed so as that a surface of the membrane 70 facing away from the luminous layer becomes substantially flat and a thickness is 80 μm at a thinnest part where there is no depression.

A structure of the depressions 11 is called a photonic crystal (PC) or a photonic band gap (PBG) structure, depending on how the depressions are formed, and depressions of such a structure serve a different function other than the light diffusion, i.e. such a structure allows the depressions to transmit light easily.

The thickness of the membrane 70 is set to 80 μm in order that the LED chip 1 as a whole emits white light, by mixing blue exciting light, having a peak wavelength ranged from 400 to 500 nm, from the (InGaN/GaN) × 6 luminous layer 23 and yellow light, having a peak wavelength ranged from 550 to 600 nm, generated from the membrane 70 excited by a part of the blue exciting light.

The depressions 11 of the non-doped GaN substrate 10 are square in the present embodiment, as explained above. However, a shape and size of the depressions are not restricted to the above example as long as the shape and size are set

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in a range that improves the light extraction efficiency. Round or honey-comb depressions, or straight-line grooves may be employed, for example. Note that it is desirable that the depressions 11 are formed at an interval of $\lambda/4$ or greater, when the wavelength of the light from the (InGaN/GaN) × 6 luminous layer 23 is λ.

As shown in FIG.2B, the LED chip 1 is such that the 35 light emitting elements 20 are connected in series by the bridge wiring 40 connecting the light emitting elements 20. When supplying the LED chip 1 with a power of 50 mA via the cathode electrode 50 and anode electrode 60, an operational voltage becomes 120 V. When supplying power to the LED chip 1, it is desirable to secure a path to disperse heat generated at the LED chip 1 by connecting to a mounting substrate and such.

Note that, although the LED chip 1 according to the present embodiment has a structure including the plural light emitting elements 20, it is also possible that one LED chip includes only one light emitting element.

[Method of Manufacturing LED Chip 1]

Next, a method of manufacturing the LED chip 1 is explained with reference to FIGs.3 and 4.

As shown in FIG.3A, the GaN buffer layer 21, n-GaN clad layer 22、(InGaN/GaN) × 6 luminous layer 23, p-GaN clad layer 24, and p-GaN contact layer 25 are layered in a stated order on the non-doped GaN substrate 10, which is φ5 cm and 300 μm thick, using Metal Organic Chemical Vapor Deposition (MOCVD).

Next, as shown in FIG.3B, grooves 31 are formed by etching at areas where the separation grooves 30 and n-electrodes 27 are formed. The grooves 31 are as deep as to reach the n-GaN

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clad layer 22. In forming the grooves 31, although not shown by the drawings, etching is performed after masking the rest of the areas, and the mask is removed after the grooves 31 are formed.

As shown in FIG.3C, a part of a bottom surface of each of the grooves 31 is further etched. Grooves 32 are thus formed and penetrate the n-GaN buffer layer 21 to reach the non-doped GaN substrate 10. The separation grooves 30 are formed based on the grooves 32. In order to form the grooves 32, it is possible to use a laser instead of etching.

As shown in FIG.3D, the Si_3N_4 membrane 28 is formed so as to cover an entire surface including wall surfaces of the grooves 32. The Si_3N_4 membrane 28 is formed using such as spattering, in order to achieve insulation and surface protection. By covering the surfaces of the grooves 32, the grooves 33 are formed. The grooves 32 make only low cuts in the substrate 10, and very superficial, and therefore the grooves 32 will not break the substrate 10.

Next, as shown in FIG.4E, parts of the Si_3N_4 membrane 28 where the p-electrodes 26 are to be formed are removed by etching, and then films of Rh/Pt/Au are formed by evaporation. Thus, the p-electrodes 26 are formed.

Then, as shown in FIG.4F, parts of the Si_3N_4 membrane 28 where the n-electrodes 27 are to be formed on the shelf part next to each of the separation grooves 30 are removed by etching, and then films of Ti/Au are formed by evaporation. Thus, the n-electrodes 27 are formed. Similarly, the bridge wiring 40 made of Ti/Pt/Au is formed so as to connect each p-electrode 26 and n-electrode 27 of two light emitting

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elements 20 that are next to each other.

Manufacturing steps from here are the most characteristic part in the present embodiment.

As shown in FIG.4G, a back surface of the non-doped GaN substrate 10 (downside of the drawing) is polished until thickness becomes 150 μm using lap polish. Then, as shown in an enlarged part of FIG.4G, the depressions 11 are etched on the back surface of the non-doped GaN substrate 10. The depressions 11, as described above, are formed at an interval of 1 μm, and an opening of each depression is rectangular.

As shown in FIG.4H, the polyimide acid solution, containing particles of yellow phosphor material such as $(Sr, Ba)_2SiO_4:Eu^{2+}$, and SiO_2 in a dispersed state, is applied to the back surface of the non-doped GaN substrate 10 on which the depressions 11 are formed. The solution is filled in the depressions 11 so that no air bubble is caused inside. And, after heating and hardening at a temperature of 350 °C, the membrane is formed.

The formed membrane is polished so that the LED chip 1 irradiates white light generated by the light from the (InGaN/GaN) × 6 luminous layer 23 mixed with the light excited by the phosphor material in the membrane. For polishing, lap polishing is performed until the thickness of the membrane becomes 80 μm, for example. By this, the membrane 70 is finished.

As a main component of the membrane 70, it is also possible to use such as an epoxy resin or a hard silicone resin, in addition to the above-mentioned polyimide. In this case, it is possible to harden the membrane by heating at a temperature

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150 °C. Further, the thickness of the membrane 70 varies according to a relation between the blue light from the (InGaN/GaN) × 6 luminous layer 23 and a proportion of the yellow phosphor contained in the membrane 70. Therefore, in the polishing step, the membrane 70 is polished to a thickness with which a specific color temperature is obtained without fail.

Finally, although not shown in the drawing, the LED chip 1 is finished by dicing the membrane into individual LED chips 1.

In the present embodiment, the non-doped GaN substrate 10 was used as a substrate. However, it is also possible to use a low cost substrate such that a high resistant layer such as an AlGaN layer is formed on an n-GaN substrate. In this case, it is necessary to form the separation grooves so that the high resistant layer is not removed.

[Structure of LED Module 100]

A LED module 100 having the above LED chip 1 is explained with reference to FIG.5.

As shown in FIG.5A, the LED module 100 comprises a disk shaped composite substrate 110 with a diameter of φ5 cm and three light emitting units 120 provided on the composite substrate 110. The composite substrate 110 includes a notch 110a used when the LED module is attached to the lighting apparatus 200, and terminals 130 and 140 with which power is supplied from the lighting apparatus 200. Although not shown in the drawing, the guiding hole is formed on a substantial center of the composite substrate 110 in order to improve operationality when attached to the lighting apparatus 200.

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The three light emitting units 120 on the composite substrate 110 each include the LED chip 1 mounted thereon. Details are explained with reference to a partial sectional view in FIG.5B.

As shown in FIG.5B, the LED chip 1 is mounted at a bottom surface of a depression 111 of the composite substrate 110. The LED chip 1 is mounted to the composite substrate 110 using flip-chip bonding, and has an excellent heat dispersion property. A reflective mirror 150 made of aluminum is formed so as to surround the depression 111 in which the LED chip 1 is mounted. The depression 111 surrounded by the reflective mirror 150 is filled with a resin layer 16, and thereby the LED chip 1 is sealed. Examples of material for the resin layer 160 include a silicon resin and a epoxy resin.

An entire part of the reflective mirror 150 and the resin layer 160 that covers the LED chip 1 are further covered by a lens layer 170. Such as a resin material that can be formed in one-piece by molding and a glass material may be used for the lens layer 170. An internal structure of the LED module 100 is explained using FIG.5B illustrating a sectional view taken at line A-A of FIG.5A.

As shown in an enlarged part of FIG.5B, the p-electrodes 26 and n-electrodes 27 of the LED chip 1 are connected to the wiring layer 114 of the composite substrate 110. In addition to an Au coating applied to a surface of the wiring layer 114, Au layers 180 are inserted between each of the electrodes 26 and 27 and the wiring layer 114. These Au layers are Au bumps that have been disposed on the wiring layer 114 when the LED chip 1 is mounted on the composite substrate 110 by flip-chip

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bonding.

Also as shown in an enlarged part of FIG.5B, the composite substrate 110 includes an aluminum layer 112 with 1 mm in thickness, an alumina composite insulating layer 113, and the wiring layer 114 made of copper layered in a stated order. Moreover, although not shown in FIG.5, an alumina composite insulating layer 115 is layered on the wiring layer (See FIG.6).

Thickness of the alumina composite insulating layers 113 and 115 is 100 μm, and thickness of the wiring layer 114 is 25 μm.

The p-electrodes 26 and n-electrodes 27 on the LED chip 1 are mounted on the wiring layer 114 in flip-chip bonding. In FIG.1, predetermined pads on the wiring layer 114 to which the cathode electrode 50 and anode electrode 60 are connected are electrically connected to the terminals 130 and 140, respectively. By this, when driving the LED module 100, power is supplied to the LED chip 1 via the wiring layer 114.

The LED module 100 according to the embodiment of the present invention includes three light emitting units 120, each of which has a structure described above.

While the p-electrodes 26 and n-electrodes 27 on the light emitting elements 20 that are next to each other are connected by the bridge wiring 40 as explained above, the p-electrodes 26 and n-electrodes 27 are connected by being mounted on the composite substrate 110, in order to ensure the connection within the LED chip 1 and to disperse the heat generated in the LED chip 1 to the composite substrate 110 without fail, when driving to emit light.

[Mounting LED Chip 1 to Composite Substrate 110]

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Next, a method of mounting the LED chip 1 to the composite substrate 110 with reference to FIG.6 and FIG.7.

As shown in FIG.6, the alumina composite insulating layer 115, which is a top layer of the composite substrate 110, is partially removed at an area where the LED chip 1 is mounted. The composite substrate 110 has areas on which three LED chips 1a, 1b, and 1c are mounted, respectively, as shown in FIG.7A, and the wiring layer 114 connects the positive and negative electrodes of each chip to the terminals 130 and 140, respectively.

As shown in FIG.7B, the wiring layer 114 is, at the areas where LED chips 1a, 1b, and 1c are mounted, patterned to a cathode pad 1151, an anode pad 1152, and island pads 1153 each correspond to each of 35 light emitting elements 20 of the LED chip 1. Among the pads, the cathode pad 1151 and anode pad 1152 are connected to the terminals 130 and 140, respectively, as described above. In addition, Au bumps 180 are formed on each of the pads 1151-1153.

The island pads 1153 have a function to improve the connectivity between the p-electrodes 26 and n-electrodes 27 each on the light emitting elements 20 that are next to each other, as well as a function to transmit the heat generated in the LED chip 1 to the composite substrate 110 at high efficiency. The heat transmitted to the composite substrate 110 is dispersed from the aluminum layer 112 via the wiring layer 114 and alumina composite insulating layer 113. Each of the island pads 1153 is formed independently, and has the above explained important functions.

Back to FIG.6, when the LED chip 1 is mounted to the

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composite substrate 110 by flip-chip bonding, a vacuum collet 500 sticks to a surface of the LED chip 1 on which the membrane 70 is formed and then moves down the LED chip 1 till the electrode 26 and 27 come into contact with the Au bumps 180 on the wiring layer 114 of the composite substrate 110. Next, while the electrode 26 and 27 are pressed against the Au bumps 180, ultrasonic waves are applied from the vacuum collet 500. The Au bumps 180 becomes soft by the ultrasonic waves applied to the bumps, and the bonding is finished when application of the ultrasonic waves stops.

As shown in an enlarged part of FIG.6, the membrane 70 is formed on the surface of the LED chip 1 that the vacuum collet 500 sticks to. Because the surface of the membrane 70 that the vacuum collet 500 sticks to is substantially flat as shown in the drawing, it is possible that the vacuum collet 500 sticks to the surface without fail. In addition, the surface that is substantially flat reduces loss of energy in applying the ultrasonic waves from the vacuum collet 500 via the surface.

Further, the membrane 70 also has a function to protect the depressions 11 of the non-doped GaN substrate 10 from being destroyed while the ultrasonic bonding.

[Lighting Apparatus 200 having LED module 100]

A lighting apparatus 200 having a LED module 100 is explained next with reference to FIGs.8 and 9. FIG.8 illustrates a perspective view and a bottom view of the lighting apparatus 200. FIG.9 illustrates an explosion view relating to attachment of the LED module 100.

As shown in FIG.8A, the lighting apparatus 200 comprises

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a horn-shaped member 210 and the LED module 100 that is attached inside the horn-shaped member 210. The horn-shaped member 210 includes a power conversion circuit (not shown in the drawings) for converting commercially supplied AC power (100 V and 50/60 Hz, for example) into DC power that is necessary to drive the LED module 100 to emit light.

As shown in FIG.8B, the LED module 100 is disposed so that the aluminum layer 112 of the composite substrate 110 is closely attached to an attaching surface inside the horn-shaped member 210 of the lighting apparatus 200.

Next, as shown in FIG.9, a round depression 211 that corresponds to a shape of the composite substrate 110 of the LED module 100 is formed on the attaching surface of the horn-shaped member 210 to which the LED module 100 is attached. The bottom of the depression 211 is substantially flat, and a female screw (not shown in the drawings) is disposed at a part closer to an opening of the depression 211 on an inside wall. A guide 212 and flexible terminals 213 and 214 are disposed on the inside wall between the female screw and the bottom surface. Positions of the guide 212 and the flexible terminals 213 and 214 correspond, respectively, to positions of the notch 110a and terminals 130 and 140 of the LED module 100. In addition, a guide pin 215 is disposed at a center of the bottom surface of the depression 211 of the horn-shaped member 210.

The flexible terminals 213 and 214 are flexible and not attached to the bottom surface of the depression 211 of the horn-shaped member 210. When inserting the LED module 100 into the depression 211, both the flexible terminals 213 and

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214 are flexed along the inside wall of the depression 211 in advance, before inserting the LED module 100.

In order to attach the LED module 100 to the horn-shaped member 210 having the above structure, the guide 212 is inserted into a guiding hole of the LED module 10, and the LED module 100 is set into the bottom surface of the horn-shaped member 210 by fitting the notch 110a along the guide pin 215. Then, when the LED module 100 is placed on the bottom surface of the depression 211 of the horn-shaped member 210, the flexible terminals 213 and 214 that have been flexed along the inside all of the depression 211 are cranked so as to be connected to the terminals 130 and 140 of the LED module 100, respectively. After that, an O-shaped ring 220 is placed at a circumference of the LED module 100, and a ring-shaped screw 230 is screwed into the female screw disposed on the inside wall of the depression 211. When the ring-shaped screw 230 and female screw are fully screwed together, the attachment of the LED module 100 to the horn-shaped member 210 is completed.

In the lighting apparatus 200 according to the present embodiment, silicone grease is applied between a back side of the LED module 100 and the bottom surface of the depression 211 of the horn-shaped member 210 in order to improve the heat dispersion efficiency. In addition, a high reflection finish is applied to an inside wall of a lampshade part of the horn-shaped member 210 in order to extract light from the LED module 100 at a high light extraction efficiency.

In the lighting apparatus 200 having the above structure, a current 150 mA is supplied to the LED module 100 via the terminals 130 and 140 after converting the commercially

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supplied AC power into the DC power at the power conversion circuit in the horn-shaped member. In the LED module 100 to which the current is supplied, the three light emitting units 120 emit the white light. At this time, the heat generated in the LED chip 1 is dispersed to the horn-shaped member 210 via the aluminum layer 112 of the composite substrate 110. Therefore, with the lighting apparatus 200, it is possible to suppress deterioration of the LED chip 1 and to maintain high luminous efficiency, even when the LED chip 1 is driven to emit light for an extended length of time.

Further, by high reflection finishing applied the lampshade part of the horn-shaped member 210, more than 90 % of the white light from the LED module 100 is extracted from the lighting apparatus 200.

A spectral distribution of the white light irradiated by the lighting apparatus 200 according to the present embodiment is illustrated in FIG.10. As shown in FIG.10, the lighting apparatus 200 according to the present embodiment irradiates the white light having a color temperature of 5400 K and an average color rendering index (CRI) of 70. A relative intensity of an emission spectrum becomes its peak in vicinity of wavelengths 460 nm and 560 nm, and especially sharp in vicinity of wavelengths 460 nm. A total luminous flux is 1000 lm, and an on-axis luminous intensity is 2000 cd.

With the lighting apparatus 200 according to the present embodiment, the white light is obtained by mixing blue light from the (InGaN/GaN) × 6 luminous layer 23 and yellow light that the membrane 70 emits when excited, and accordingly, the CRI is around 70. However, by having the membrane 70 contain

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such as Ca-Al-Si-O-N oxynitride phosphor glass that irradiates red light, it is possible to improve the CRI.

[Advantages of LED Chip 1, LED Module 100 Using LED Chip 1, and Lighting Apparatus 200 Using LED Chip 1]

As described above, the LED chip 1 according to the present embodiment is such that the depressions 11 are disposed on the surface of the non-doped GaN substrate 10 facing away from the luminous layer, and the membrane 70 is formed so as to cover the depressions 11. Accordingly, as in FIG.6, when the LED chip 1 is mounted by flip-chip bonding to the composite substrate 110, the depressions 11 on the non-doped GaN substrate 10 are protected. Further, misalignment of the position when mounting is suppressed, because the vacuum collet 500 sticks to the LED chip 1 firmly in flip-chip bonding. Moreover, when the vacuum collet 500 applies the ultrasonic waves, the membrane 70 prevents the ultrasonic energy from weakening in transmission between the vacuum collet 500 and the LED chip 1, and thus mounting is performed without fail.

With the LED module 100 having the LED chip 1 and the lighting apparatus 200 having the LED chip 1, it is possible to obtain high light extraction efficiency, because the depressions 11 of the non-doped GaN substrate 10 of the LED chip 1 are protected. In addition, the LED module 100 having the LED chip 1 and the lighting apparatus 200 having the LED chip 1 have high light emission efficiency, because the attachment is done firmly when mounting.

Note that the LED chip 1 according to the present embodiment also has an advantage such that there is no obstacle such as an electrode which blocks the light on a side which

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light from the luminous layer is irradiated, and therefore a shadow on an irradiated surface will not appear.

[Second Embodiment]

In a second embodiment, a LED chip 3 as an example of the semiconductor light emitting device is explained.

[Structure of LED chip 3]

The LED chip 3 according to the present embodiment has a similar appearance with the LED chip 1 shown in FIG.1. Specifically, light emitting elements 320 each having a size of 285 μm × 400 μm are disposed in a matrix of 7 × 5, and a size of the LED chip 3 is 2 × 2 mm. Below, a structure of the LED chip 3 is explained focusing on differences from the LED chip 1, with reference to FIG.11. FIG.11A illustrates a partial sectional view of the LED chip 3, and FIG.11B illustrates a top view of the LED chip 3 without a membrane 370, which will be explained later.

As shown in FIG.11A, the LED chip 3 is formed in a manner that an AlGaN buffer layer 321 (30 nm thick), an n-$Al_{0.1}Ga_{0.9}N$ clad layer 322 (Si doped 3 × 10^{18} cm^{-3}, 1.5 μm thick), an $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N$ × 5 luminous layer 323 ($In_{0.03}Ga_{0.97}N$ is 3 nm thick, and $Al_{0.05}Ga_{0.95}N$ is 5 nm thick), a p-$Al_{0.1}Ga_{0.9}N$ clad layer 324 (Mg doped 3 × 10^{19} cm^{-3}, 200 nm thick), and a p-GaN contact layer 325 (Mg doped 3 × 10^{19} cm^{-3}, 500 nm thick) are layered on the a non-doped 4H-SiC substrate 310 in a stated order. The $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N$ × 5 luminous layer 323 indicates a multiplex quantum well structure luminous layer with 5 periods of $In_{0.03}Ga_{0.97}N/Al_{0.06}Ga_{0.95}N$, and irradiates near-ultraviolet light having a wavelength of 380 nm in driving the LED chip 3.

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A refractive index of the non-doped 4H-SiC substrate 310 is around 2.3, which is substantially the same as a refractive index of the $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N$ × 5 luminous layer 323.

Structures of a separation groove 330, n-electrode 327, an Si_3N_4 membrane328, and a bridge wiring 340 are the same as in the LED chip 1, and not explained here.

As shown in FIG.11B, depressions are not formed on a back surface of the non-doped 4H-SiC substrate 310 of the LED chip 3, and an Ni/Al/Pt/Au layer 380 is formed. Further, a p-electrode 326 made of Ni/Au is formed on the p-GaN contact layer 325, and a plurality of depressions 326a are formed so as to penetrate from a surface of the p-GaN contact layer 325 to the p-electrode 326. Details about these depressions are explained with reference to FIG.11B.

As shown in FIG.11A, the depressions 326a are in a round shape formed at a period of 1 μm, and as described above, the depressions have a function to make light irradiated from the $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N$ × 5 luminous layer 323 is easily dispersed or transmitted. The depressions 326a are formed over an entire area of the p-electrode 326 that irradiates the near-ultraviolet light from the $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N$ × 5 luminous layer 323.

Back to FIG.11A, an upper surface of the LED chip 3 where electrodes 326 and 327 are formed is entirely covered by the transmission membrane 370. Although not shown in the drawing, the membrane 370 is not formed on parts corresponding to a cathode electrode 50 and an anode electrode 60 in FIG.1.

The membrane 370 is 50 μm thick, mainly composed of a

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hard silicon resin having light transmissivity, and is formed so as to fill the depressions 326a completely and so that an external surface is substantially flat. Moreover, the membrane 370 contains, in a dispersed state, a phosphor material that is excited to emit light by the near-ultraviolet light from the $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N \times 5$ luminous layer 323, and fine particles of SiO_2. The phosphor material to be selected may be any phosphor material that is excited by the near-ultraviolet light so that the white light is irradiated from the LED chip 3 as a result. Examples of such a phosphor material that may be applied are in the following.

Example 1: A combination of blue phosphor material, green phosphor material, and red phosphor material, emitting blue light, green light, and red light, respectively when excited by the near-ultraviolet light.

Example 2: A combination of the phosphor material in the Example 1, and yellow phosphor material emitting yellow light when excited by the near-ultraviolet light.

Example 3: A combination of blue phosphor material and yellow phosphor material, emitting blue light and yellow light, respectively, when excited by the near-ultraviolet light.

Example 4: A combination of the phosphor material in the Example 3, and red phosphor material emitting red light when excited by the near-ultraviolet light.

Example 5: A combination of blue phosphor material emitting blue light when excited by the near-ultraviolet light, and green phosphor material and red phosphor material, emitting green light and red light, respectively, when excited by the blue light emitted from the blue phosphor material.

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Example 6: A combination of blue phosphor material emitting blue light when excited by the near-ultraviolet light, green phosphor material emitting green light when excited by the blue light emitted from the blue phosphor material, and red phosphor material emitting red light when excited by the green light emitted from the green phosphor material.

The above examples are just examples, and do not restrict the present invention. Any other combination with which the white light is obtained from the LED chip 3 may be employed.

In addition, in the above examples, the blue light indicates light having a peak wavelength of light emission falls in a range of 400 nm to 500 nm, the green light indicates light having a peak wavelength of light emission falls in a range of 500 nm to 550 nm, the red light indicates light having a peak wavelength of light emission falls in a range of 600 nm to 680 nm, and the yellow light indicates light having a peak wavelength of light emission falls in a range of 550 nm to 600 nm.

Specifically, the following phosphor materials may be utilized.

Blue Phosphor Material:

$(Ba, Sr)MgAl_{10}O_{17}:Eu^{2+}$

$(Ba, Sr, Ca)_{10}Mg(PO_4)_6Cl_2:Eu^{2+}$

Green Phosphor Material:

$BaMgAl_{10}O_{17}:Eu^{2+}, Mn^{2+}$

$(Ba, Sr)_2SiO_4:Eu^{2+}$

$Y_3(Al, Ga)_5O_{12}:Ce^{3+}$

Yellow Phosphor Material:

$(Y, Gd)_3Al_5O_{12}:Ce^{3+}$

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$(Sr, Ba)_2SiO_4:Eu^{2+}$

Red Phosphor Material:

$La_2O_2S:Eu^{3+}$

$CaS:Eu^{2+}$

Moreover, among the substances contained in the membrane 370, SiO_2 is ultrafine particles having a diameter ranged from a couple 10 nm to a couple 100 nm. The following may be used as fine particles contained in the membrane 370, other than SiO_2 as described above: Al_2O_3, ZnO, Y_2O_3, TiO_2, ZrO_2, HfO_2, SnO_2, Ta_2O_3, Nb_2O_3, $BaSO_4$, ZnS, V_2O_5, and a mixture of any of the above substances.

A circuit configuration of the LED chip 3 of the above structure is such that the 35 light emitting elements 320 are connected in series as FIG.2B, and the near-ultraviolet light from the $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N \times 5$ luminous layer 323 is converted into the white light at the membrane 370 and irradiated from the upper surface shown in FIG.11A. Driving voltage of the LED chip 3 is 120 V, when the heat dispersion is ensured and a current of 50 mA is supplied.

[Method of Manufacturing LED Chip 3]

Next, a method of manufacturing the LED chip 3 is explained with reference to FIG.12. In manufacturing the LED chip 3, steps after the step shown in FIG.4F are explained, because the steps from the beginning to FIG.4F are the same as the method of manufacturing the LED chip 1, although material used is not the same.

FIG.12A shows a step at which formation of the p-electrode 326 and n-electrode 327 is completed.

Next, as shown in FIG.12B, the lower surface of the

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non-doped 4H-SiC substrate 310 is polished till a thickness of the substrate becomes 150 μm. After the polishing, the Ni/Al/Pt/Au layer 380 is formed on the polished surface using evaporation.

As shown in FIG.12C, the depressions 326a in a pattern shown in FIG.11B are etched to an area where the p-electrode 326 is to be formed. Etching is performed in a manner that a surface of the p-GaN contact layer 325 becomes bottom surfaces of the depressions 326a. The depressions 326a are formed at a period of 1 μm and a shape of openings of the depressions 326a is round.

Then silicon resin containing phosphor material is applied to an entire upper surface of the chip, and the membrane 370 is formed after heating the silicon resin at a temperature of 150 °C and hardening. When applying the silicon resin, a special care needs to be taken so that the depressions 326a does not include air inside. In addition, parts corresponding to the cathode electrode and anode electrode are masked so that the silicon resin is not applied.

Finally, after lap polishing is performed until the thickness of the membrane becomes 50 μm, the manufacturing of the LED chip 3 is completed by dicing the membrane into LED chips.

[Structure of LED module]

A LED module having the above LED chip 3 is explained with reference to FIG.13. FIG.13A illustrates a partial sectional view of the LED module, and FIG.13B illustrates a connection between the LED chip 3 and a wiring layer 414.

As shown in FIG.13A, main components of the LED module

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include a ceramics substrate 410 having a depression 411 whose opening has a diameter of φ3 mm, and the LED chip 3 that is connected to a bottom surface of the depression 411. A reflective mirror 450 made of aluminum (thickness: 0.5 mm, diameter of an upper part of an opening: 4 mm) is attached over the ceramics substrate 410 so as to surround the depression 411. A resin layer 460 is filled in the depression 411 surrounded by the reflective mirror 450, so as to firmly fix the LED chip 3. An upper surface of the resin layer 460 is substantially even with an upper surface of the reflective mirror 450, and a lens layer 470 is formed to cover the upper surfaces.

As shown in FIG.13A, the ceramics substrate 410 is a substrate with a diameter of φ5 cm and having a laminated structure. The ceramics substrate 410 is structured such that an AlN layer 412 with 0.5 mm in thickness, the wiring layer 414 that is 25 μm in thickness and made of copper or tungsten with, and a ceramics layer 415 are layered in a stated order on the ceramics substrate 410. At a part where the depression 411 is formed, the ceramics layer 415 as a top layer is removed, and the wiring layer 414 is patterned into two parts, a cathode electrode side and an anode electrode side. Further, an Au coating is applied to a surface of a part (pad) where the wiring layer 414 is exposed because the ceramics layer 415 is removed by the depression 411. Although not shown in the drawing, a lower surface of the ceramics substrate 410 is applied with an Au coating in order to improve the heat dispersion property.

It is possible to use a layer made of Al_2O_3, BN, MgO, ZnO, or SiC for the ceramics substrate 410, instead of the

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AlN layer 412.

The LED chip 3 is disposed on the bottom surface of the depression 411 of the ceramics substrate 410, and Au layers 480 are inserted between the Ni/Al/Pt/Au layer 380 and the wiring layer 414 of the ceramics substrate 410. The Au layers are the Au bumps that are placed on the wiring layer 414 when the chip is mounted, as explained already. As shown in FIG.13B, the LED chip 3 is connected onto a cathode pad 414a, which is a larger one of two pads (the cathode pad 414a and anode pad 414b) that are extending from facing sides of the inside wall of the depression 411. The cathode electrode 350 and anode electrode 360 of the LED chip 3 are connected to the cathode pad 414a and anode pad 414b via bonding wires 481 and 482, respectively.

In the present embodiment, the LED chip 3 and the pads 414a and 414b on the ceramics substrate 410 are connected by wire bonding. However, it is also possible, instead of connecting electrically by wire bonding, that the LED chip 3 and the pads are connected using bumps or by soldering, by a metal piece disposed in a penetrating hole in the LED chip 3 so as to dispose an electrode on a back surface of the LED chip 3.

Structures of the reflective mirror 450, the resin layer 460, and the lens layer 470 are the same as in the LED chip 1, and therefore not explained in detail.

Although not shown in the drawing, the LED module according to the present embodiment has substantially the same structure as the LED module in FIG.5, other than the structure of and connection to the LED chip 3. A lighting apparatus

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having the LED module may be the same structure as shown in FIG.8, or may have a different structure.

The lighting apparatus having the LED chip 3 according to the present embodiment irradiates white light having a color temperature of 4600 K and an average CRI of 90 by supplying a DC electricity of 150 mA to the LED module. A total luminous flux of this lighting apparatus is 1000 lm, and on-axis luminous intensity is 2000 cd. A spectral distribution of the white light irradiated by the lighting apparatus according to the present embodiment is illustrated in FIG.14.

As shown in FIG.14, a relative intensity of an emission spectrum shows a sharp peak in vicinity of wavelengths 620 nm, and is relatively high in vicinity of wavelengths between 450 nm and 620 nm.

[Advantages of LED Chip 3, LED Module Using LED Chip 3, and Lighting Apparatus Using LED Chip 3]

As described above, the LED chip 3 according to the present embodiment is such that the depressions 326a are on a side of the p-electrode 326 which the near-ultraviolet light from the $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N \times 5$ luminous layer 323 passes through, and the membrane 370 is formed so as to cover the depressions 326a. When the LED chip 3 is mounted to the ceramics substrate 410, a vacuum collet sticks to the surface of the membrane 370, then the ultrasonic waves are applied after the LED chip 3 is pressed to the ceramics substrate 410. By forming the membrane 370, it is possible to mount the LED chip 3 without fail, because the vacuum collet firmly sticks to the LED chip 3, and the ultrasonic energy is not lost in the depressions 326a of the p-electrode 326. Further, because

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the loss of the ultrasonic energy in the depressions 326a is small and the surface of the depressions 326a is protected by the membrane 370, the depressions 326a are not destroyed by application of the ultrasonic waves when the chip is mounted. Such advantages are the same as the case of the first embodiment.

Because of the above advantages that the LED chip 3 has, it is possible that the LED module and the lighting apparatus having the LED chip 3 obtains, as in the case of the first embodiment, high light extraction efficiency and excellent heat dispersion property because the LED chip 3 is firmly attached when mounting. Thus, the LED module and the lighting apparatus having the LED chip 3 have such advantages that high light-emission efficiency and longevity.

Further, as in the LED chip 3 according to the present embodiment, when the p-electrode 326 and n-electrode 327 are disposed on one side, it is necessary, in general, to remove the luminous layer at the part where the n-electrode 327 is disposed, and therefore it is unavoidable that a luminous area becomes smaller. However, in the LED chip 3 according to the present embodiment, the light emitting elements are connected using the bridge wiring 380 in the LED chip 3, and it is possible to make the n-electrode 327 smaller in comparison with a case in which the light emitting elements are connected using bonding wires or bumps (For example, the n-electrode 327 can be 10 μm square, when it is 100 μm square when using bonding wires or bumps). Thus, by using the LED chip 3, the luminous area becomes wider, because it is possible to make an area of the p-electrode 326 under which the luminous layer is formed wider according to an area that the n-electrode 327 is made

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smaller.

For example, when a size of each light emitting element of the LED chip is 285 μm × 400 μm, and an overlapping margin for attachment is 25 μm wide from an edge, an effective area becomes 82250 μm^2. Further, the luminous area per light emitting element of the LED chip 3, in which the area of the n-electrode accounts for 10 × 10 μm^2, according to the present embodiment becomes 82250 - 10 × 10 = 82150 μm^2. Calculating in the same way, a luminous area per light emitting element of a conventional LED chip, in which the area of the n-electrode accounts for 100 × 100 μm^2, becomes 72250 μm^2. In comparison, it is clear that the luminous area of the LED chip 3 according to the present embodiment is 1.13 times as large as that of the conventional LED chip.

Moreover, by making the luminous area wider, the current density may be reduced when the same current is supplied as the case in which the luminous area is smaller, and thus it is possible either to suppress the heat, or to increase quantity of light by supplying more current till the level of current density becomes the same as the case of the smaller luminous area.

As described above, the LED chip 3 according to the present embodiment has an advantage that, when the light emitting elements are connected using bridge wiring on the chip, it is possible to increase the luminous area even when the total chip area is the same, in comparison with the case in which the LED chip made of one light emitting element is connected by wire bonding or bumps.

Although the non-doped 4H-SiC substrate 310 is used as

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a substrate in the LED chip 3 according to the present embodiment, it is also possible to use a substrate of an n-SiC substrate on which a layer having a high resistance such as an AlGaN layer is formed. In this case, it is necessary that a separating groove does not completely remove the layer having high resistance.

Moreover, if the cathode electrode is connected to the n-SiC substrate in the LED chip 3, it is not necessary to use a bonding wire between the cathode pad and the cathode electrode.

As explained above, when the n-SiC substrate is used in place of the non-doped 4H-SiC substrate, it is possible to disperse the generated heat to the mounting substrate even when the luminous layer comes upper side, because the n-SiC substrate has as high heat conductance as metal.

It is also possible to use sapphire, AlN, and Si for the substrate, even though heat conductance of those material is not as good.

[Third Embodiment]

Next, a structure of an LED display apparatus 6 according to a third embodiment of the present invention is explained with reference to FIG.15.

As shown in FIG.15A, the LED display apparatus 6 according to the present embodiment is such that a reflective mirror 62 and a lens 63 are layered, in a stated order, in an area on a main surface of a composite substrate 61, and 256 light emitting units 66 are formed in 16 × 16 in this area. Connecting terminals 64 and 65 that connect between the LED display apparatus 6 and a driving circuit to drive the LED display

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apparatus 6 are formed in the other areas on the main surface of a composite substrate 61. The connecting terminals 64 and 65, respectively, are connected to the LED chip 67 that constitutes each of the light emitting units 66 via wiring layers 615 and 616 formed as a part of the composite substrate 61 (See FIG.15B).

As shown in FIG.15B, the light emitting units 66 of the LED display apparatus 6 has such a structure that the LED chip 67 is attached to a conductive land 617 that is disposed on the main surface of the composite substrate 61, i.e. the LED chip 67 is mounted to the composite substrate 61 by flip-chip bonding. Then, the reflective mirror 62 is disposed so as to surround the LED chip 67, and the lens 63 is formed so as to cover the LED chip 67 and the reflective mirror 62.

The composite substrate 61 is formed by a metal layer 611 and three insulating layers 612-614, and wiring layers 615 and 616 are formed, respectively, between the insulating layer 613 and 614 and between the insulating layers 612 and 613. The conductive land 617 and each of the wiring layers 615 and 616 are connected by a via hole.

As shown in FIG.15B, the LED chip 67 has the same structure as the light emitting element 20 in the LED chip 1 shown in FIG.2. Further, as shown in an enlarged part of FIG.15B, minute depressions 6711 having a square shaped opening are formed on an entire surface of a non-doped GaN substrate 671 on a side that the light is irradiated (upper side in the drawing). The depressions 6711 are formed at an interval of 1 μm, for example.

A membrane 672 is formed on the non-doped GaN substrate

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671 so as to fill the depressions 6711. As in the first embodiment, the membrane 672 is mainly made of a polyimide resin having transmissivity, and contains a yellow phosphor material such as $(Sr, Ba)_2SiO_4:Eu^{2+}$, and ultrafine particles such as SiO_2 in a dispersed state. The membrane 672 is formed so as to be 80 μm thick at the thinnest part (parts that do not have the depression 6711), and so that a surface is substantially flat. A structure of the membrane 672 is the same as in a case of the first embodiment.

With the LED display apparatus 6 according to the third embodiment, as in the first embodiment, it is possible to protect the depression 6711 and suppress displacement of the LED chip 67 when the LED chip 67 is mounted to the composite substrate 61 by flip-chip bonding. Further, by having the membrane 672, the ultrasonic energy applied does not become weakened between the vacuum collet and LED chip when the vacuum collet applies the ultrasonic waves.

With the LED display apparatus 6 having the above structure, the depressions 6711 on the non-doped GaN substrate 671 of the LED chip 67 are protected, and thus it is possible to obtain high light extraction efficiency, as well as high light emitting efficiency due to a firm attachment in mounting.

The LED display apparatus 6 according to the present embodiment illustrates an example of the present invention, and the present invention is not restricted by this embodiment. For example, it is possible to use TFT substrate instead of the composite substrate 61.

[Fourth Embodiment]

A structure of a fourth embodiment is explained below,

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with reference to FIG.16. In the present embodiment, a Vertical Cavity Surface Emitting Laser (hereinafter referred to as VCSEL) device is taken as an example.

As shown in FIG.16A, a VCSEL device 7 according to the present embodiment is such that a cathode electrode 72 is disposed on one of main surfaces of a SiC substrate 71 (lower surface in FIG.16A), a phosphor layer 74 is formed on a part of the other side of main surfaces (upper surface in FIG.16A), and an anode electrode 75 is disposed on the rest of the same side of main surfaces. A total number of 36 VCSEL cells 73 are formed in the area of the SiC substrate 71 that is covered by the phosphor layer 74. As shown in the drawing by a partial cutout part, an anode electrode 738 (See FIG.16B) of each of the VCSEL cells 73 and the anode electrode 75 disposed on the main surface of the SiC substrate 71 are connected by an Al bridge wiring 76.

As shown by a sectional view of FIG.16B taken at a plane indicated by C-C, there are 6 VCSEL cells 73 at the section of the VCSEL device 7. As shown in an enlarged view of FIG.16B, the VCSEL cell 73 is formed the SiC substrate 71, the cathode electrode 72 that is formed on one of the main surfaces of the SiC substrate 71, and layers that are layered on the other side of the main surfaces on which the phosphor layer 74 is formed. The layers that are layered on the other side of the main surfaces are formed on the SiC substrate 71 such that a semiconductor DBR layer 731, an n-clad layer 732, an active layer having a multiplex quantum well structure (hereinafter referred to as MQW layer) 733, and a p-clad layer 734 are layered in a stated order, and an SiN passivation layer 735 and an

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anode electrode 736 are formed so as to enclose a layered part of the above layers. Further, an ITO layer 737 and a dielectric DBR layer are layered in a stated order on a part of a surface of the p-clad layer 734 that is enclosed by the anode electrode 736.

As explained above, each of the VCSEL cells 73 of the VCSEL device 7 is structured by the SiC substrate 71, the cathode electrode 72, and the above-described more than one components 731-738. Further, a characteristics of the above VCSEL device 7 according to the present embodiment is in that the phosphor layer 74 covers an entire part where the VCSEL cells 73 are formed. Specifically, as in the first to third embodiments, covering an entire VCSEL cells 73 by the phosphor layer 74 protects the anode electrode 736 and such of each of the VCSEL cells 73 from being damaged when mounting the VCSEL device 7, and also ensures an accurate mounting. In addition, it is possible to obtain the same effect as in the first and second embodiments.

Next, a method of manufacturing the VCSEL device 7 according to the present embodiment is explained with reference to FIGs.17 and 18. Both FIGs.17 and 18 illustrate the same one of the VCSEL cells 73, for convenience.

As shown in FIG.17A, the semiconductor DBR layer 731, the n-clad layer 732, the MQW layer 733, and the p-clad layer 734 are layered, in a stated order, on one of the main surfaces of the SiC substrate 71.

As shown in FIG.17B, a mask (not shown in the drawing) is formed at an area of a surface of the p-clad layer 734, specifically, an area where the VCSEL cells 73 are formed,

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and etching is performed with the n-clad layer 732 as a stopper layer. By this etching, the MQW layer 733 and p-clad layer 734 remain in projections on an area on the surface of the n-clad layer 732.

As shown in FIG.17C, the semiconductor DBR layer 731 and n-clad layer 732 are etched so as to be slightly larger in section than the MQW layer 732 and p-clad layer 734. After this, as shown in FIG.17D, the Al bridge wiring 76 is formed so as to reach the surface of the SiC substrate 71 and a part of the surface of the n-clad layer 734.

As shown in FIG.18E, the SiN passivation layer 735 is formed so as to cover a surface that the Al bridge wiring 76 and n-clad layer 732 remain and the area of the surface the p-clad layer 734.

Next, as shown in FIG.18F, the anode electrode 736 is formed on an area of a surface of the SiN passivation layer 735 and the area of the p-clad layer 734.

As shown in FIG.18G, an ITO layer 737 and a dielectric DBR layer 738 are layered in a stated order at the area of the surface of the p-clad layer 734 surrounded by the anode electrode 736. In addition, as shown in FIG.18H, the cathode electrode 72 is formed on an entire surface of the other main surface of the SiC substrate 71.

Although not shown in the drawing, after a step shown in FIG.18H, the phosphor layer 74 is formed, where necessary, on the surface of the SiC substrate 71 where the above elements 731-738 are formed. Finally, the VCSEL cells 73 of the VCSEL device 7 is completed after the SiC substrate 71 is cut into units as shown in FIG.16.

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As described above, in manufacturing the VCSEL device 7, the phosphor layer 74 is formed so as to form an entire area where the VCSEL cells 73 to be formed. The phosphor layer 74 is formed so as that its surface becomes substantially flat. Therefore, an advantageous effect may be obtained because it is possible to mount the VCSEL device 7 to the substrate using the surface of the phosphor layer 74.

Although the present embodiment is explained by taking the VCSEL device as an example, the same effect may be obtained when applied to a Resonant Cavity Light Emitting Diode (RC-LED) that has substantially the same structure as the VCSEL device.

[Other Matters]

The first to fourth embodiments are examples to explain the characteristics of the structures and effects of the present invention, and the present invention is not restricted by these embodiments. For example, in the first and second embodiments, the white light irradiated from each of the light emitting units 120 is generated by the light from the luminous layer mixing with light generated by the luminous substance being excited by the light from the luminous layer. However, it is also possible that either the white light or mono color light is generated using mono-color LED modules, or mixing mono-color LED lights.

Moreover, although the membranes 70 and 370 in the LED chips 1 and 3 contain the phosphor material and such, the phosphor material and such do not necessarily have to be contained. Basically, these membranes are formed in order to allow the vacuum collet to stick to the LED chips 1 and 3 more firmly when the LED chips are mounted, as well as to

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reduce the loss in the ultrasonic energy. Thus, whether or not the phosphor material is contained is not an essential part of the present invention.

In addition, the examples of the material to form the membrane 70 listed in the first embodiment are organic resins such as polyimide, epoxy, and silicone. However, it is also possible to use glass by the sol-gel method or low-melting glass for the membrane 70. Specific examples of the glass material include (1) a glass material using metal alkoxide (such as tetramethoxysilane and tetraethoxysilane) as starting material, (2) a glass material made from polymer ceramic precursor such as perhydropolysilazane, and (3) a glass material made from such as phosphorus oxide and boronic oxide.

With any of the above listed glass materials, it is possible to form a glass layer (membrane) whose upper surface is substantially flat and filling the depressions, by applying the glass material on the depressions using such as potting and spin-coating, drying the glass material, and baking the glass material at a temperature of several hundred degrees centigrade.

Further, with the above semiconductor light emitting devices explained in the first to fourth embodiments, the advantages that the vacuum collet firmly sticks to the LED chip may be obtained even without applying the ultrasonic waves when the LED chip is mounted.

It is also possible to modify the structures of the display device 6 and VCSEL device 7 explained in the third and fourth embodiments, respectively, within a scope in which the effects of the present invention may be obtained.

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Moreover, the present invention may be applied to a Surface Mount Device (SMD) illustrated in FIG.19. As shown in FIG.19, an SMD 8 to which the present invention is applied is structured so that a pair of external electrodes 82a and 82b are disposed on a mounting substrate 81, and a LED chip 82 is mounted to the electrodes 82a and 82b by flip-chip bonding with bumps therebetween, and the LED chip 82 and electrodes 82a and 82b over the mounting substrate 81 are covered by a resin package 85.

As shown in an enlarged part in FIG.19, the LED chip 82 of the SMD 8, like the LED chip 67 in the second embodiment described above, has a surface with depressions 8311, and a membrane 8322 covers the LED chip 67 so as to fill the depressions. With the SDM 8 having the above structure, it is possible to obtain the same effects as the above first to fourth embodiments, because damages to the depressions in mounting the LED chip 82 to the mounting substrate 81 may be reduced.

Industrial Applicability

The present invention is effective to realize a high power semiconductor light emitting device having high light output, and a lighting apparatus and a display device using such a semiconductor light emitting device.

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CLAIMS

1. A semiconductor light emitting device having a luminous layer, comprising:

a light transmission layer disposed over a main surface of the luminous layer, and having depressions on a surface facing away from the luminous layer; and

a transmission membrane disposed on the light transmission layer so as to follow contours of the depressions, wherein

light from the luminous layer is irradiated so as to pass through the light transmission layer and the transmission membrane.

2. A semiconductor light emitting device according to Claim 1, wherein a surface of the membrane facing away from the light transmission layer is substantially flat.

3. A semiconductor light emitting device according to Claim 1, wherein a main component of the membrane is one of polyimide, epoxy, and silicone.

4. A semiconductor light emitting device according to Claim 1, wherein a main component of the membrane is glass.

5. A semiconductor light emitting device according to Claim 1, wherein the membrane contains a luminous substance that

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is excitable by the light from the luminous layer.

6. A semiconductor light emitting device according to Claim 5, wherein the light from the luminous layer is converted into white light by passing through the membrane.

7. A semiconductor light emitting device according to Claim 5, irradiating white light generated by light from the luminous substance being excited mixing with the light from the luminous layer.

8. A semiconductor light emitting device according to Claim 1, wherein the depressions are at an interval equal to or greater than $\lambda/4$, λ being a wavelength of the light from the luminous layer.

9. A semiconductor light emitting device according to Claim 1, wherein

the light transmission layer is formed from at least a light transmission substrate, and

the luminous layer is sandwiched between a plurality of layers and is disposed over the light transmission substrate.

10. A semiconductor light emitting device according to Claim 9, wherein the depressions are on a main surface of the light transmission substrate facing away from the luminous layer.

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11. A semiconductor light emitting device according to Claim 9, wherein the light transmission substrate is made of a material having a refractive index that is substantially equal to a refractive index of the luminous layer.

12. A semiconductor light emitting device according to Claim 11, wherein the material for the light transmission substrate is selected from a group of GaN, SiC, and AlN.

13. A semiconductor light emitting device according to Claim 9, wherein a reflective film is disposed on a surface of the luminous layer facing away from the light transmission layer.

14. A semiconductor light emitting device according to Claim 1, being a light emitting diode device.

15. A semiconductor light emitting device according to Claim 1, being a Vertical Cavity Surface Emitting Laser device.

16. A semiconductor light emitting device according to Claim 1, being a Resonant Cavity Light Emitting Diode device.

17. A semiconductor light emitting device according to Claim 1, being a Surface Mount Device.

18. A lighting apparatus comprising a mounting substrate, and a semiconductor light emitting device mounted on a pad

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on a surface of the mounting substrate, wherein:

the semiconductor light emitting device includes;

a luminous layer;

a light transmission layer disposed over a main surface of the luminous layer, and having depressions on a surface facing away from the luminous layer; and

a transmission membrane disposed on the light transmission layer so as to follow contours of the depressions, and

light from the luminous layer is irradiated so as to pass through the light transmission layer and the transmission membrane.

19. A lighting apparatus according to Claim 18, wherein a surface of the membrane facing away from the light transmission layer is substantially flat.

20. A lighting apparatus according to Claim 18, wherein a main component of the membrane is glass.

21. A display apparatus comprising a mounting substrate, and a plurality of semiconductor light emitting devices each mounted on a pad on a surface of the mounting substrate, wherein

each of the semiconductor light emitting devices includes:

a luminous layer;

a light transmission layer disposed over a main surface

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of the luminous layer, and having depressions on a surface facing away from the luminous layer; and

a transmission membrane disposed on the light transmission layer so as to follow contours of the depressions, and

light from the luminous layer is irradiated so as to pass through the light transmission layer and the transmission membrane.

22. A display apparatus according to Claim 21, wherein a surface of the membrane facing away from the light transmission layer is substantially flat.

23. A display apparatus according to Claim 21, wherein a main component of the membrane is glass.

24. A method of manufacturing a semiconductor light emitting device, comprising steps of:

forming a light transmission layer over a multi-layered body in which the luminous layer is sandwiched between a plurality of layers, the light transmission layer having depressions on a surface facing away from the luminous layer; and

forming a transmission membrane on the light transmission layer so as to follow contours of the depressions.

25. A method of manufacturing a semiconductor light emitting

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device according to Claim 24, wherein a material that forms the membrane contains a luminous substance that is excitable by the light from the luminous layer.

26. A method of manufacturing a semiconductor light emitting device according to Claim 25, further comprising a step of:

polishing the membrane after forming the membrane, till a thickness of the membrane becomes such that irradiated light is desirable white light.

27. A method of manufacturing a semiconductor light emitting device according to Claim 24, wherein a material that forms the membrane contains one of polyimide, epoxy, and silicone.

28. A method of manufacturing a semiconductor light emitting device according to Claim 24, wherein a material that forms the membrane contains glass.

29. A method of manufacturing a semiconductor light emitting device according to Claim 24, wherein

the light transmission layer includes at least a light transmission substrate, and

the depressions are on a main surface of the light transmission substrate facing away from the luminous layer.

30. A method of manufacturing a semiconductor light emitting device according to Claim 29, wherein the light transmission

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substrate is formed by a material selected from a group of GaN, SiC, and AlN.

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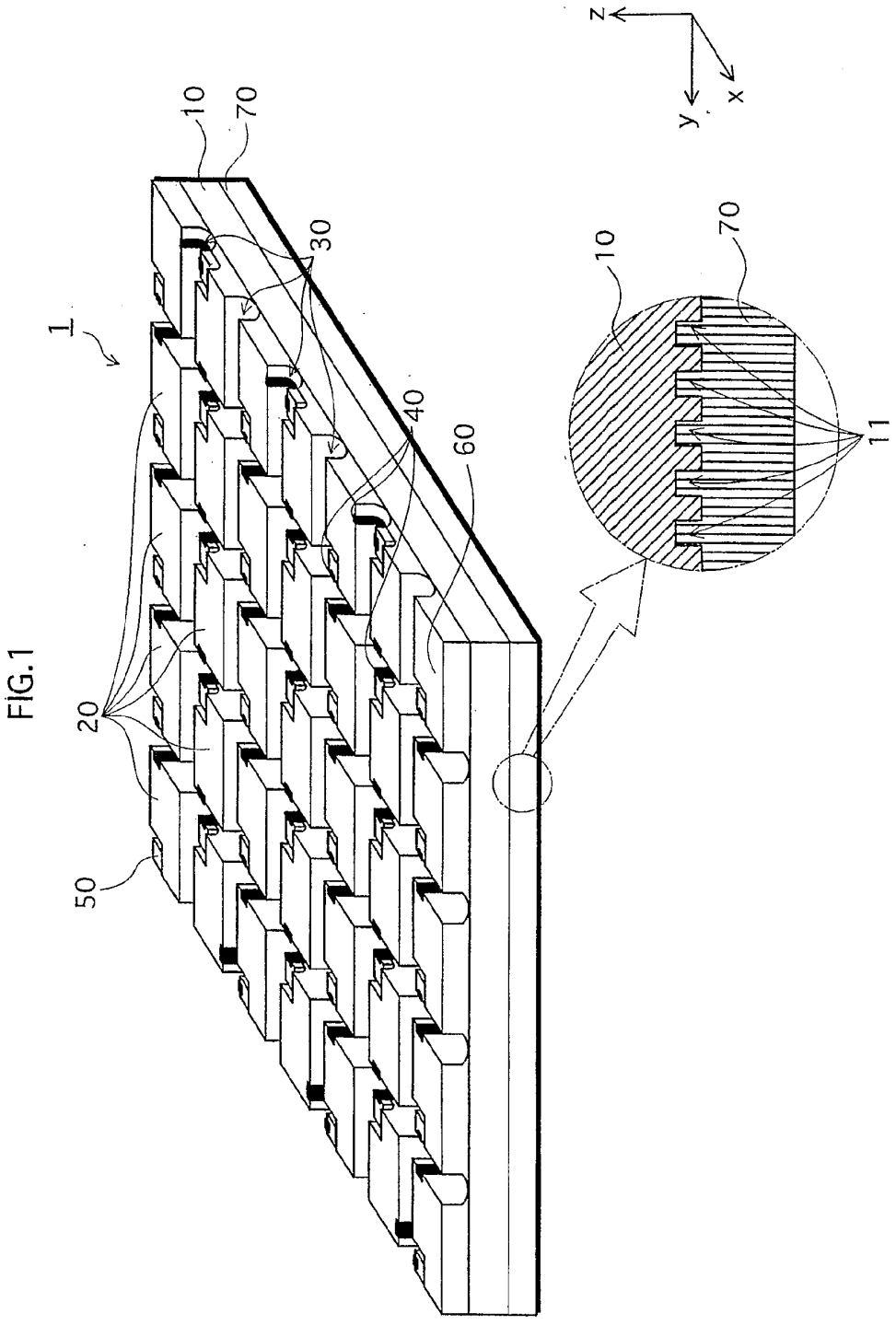


FIG.1

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FIG.2A

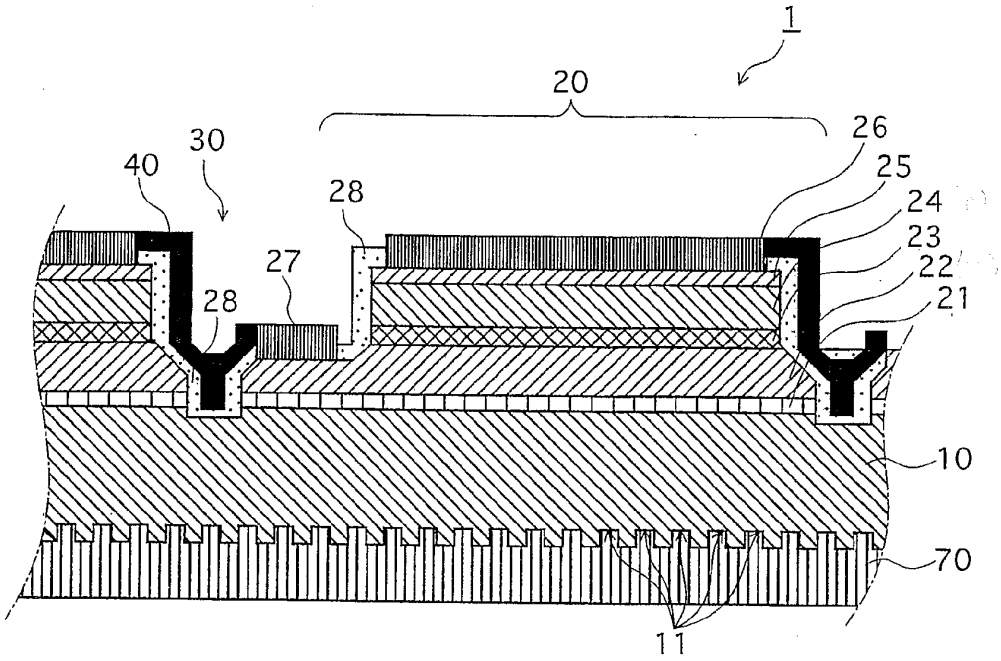
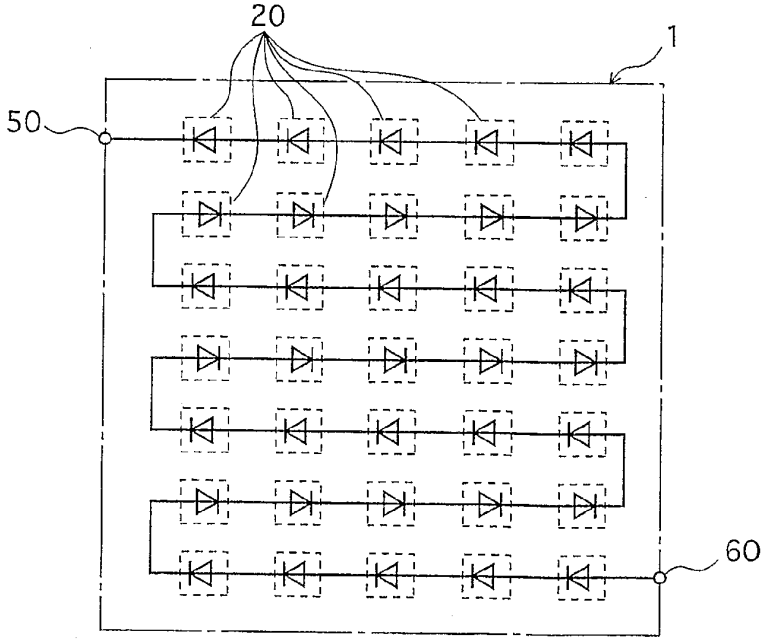


FIG.2B



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FIG.3A

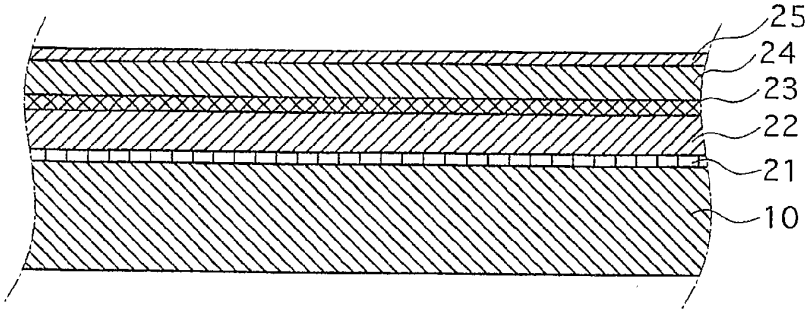


FIG.3B

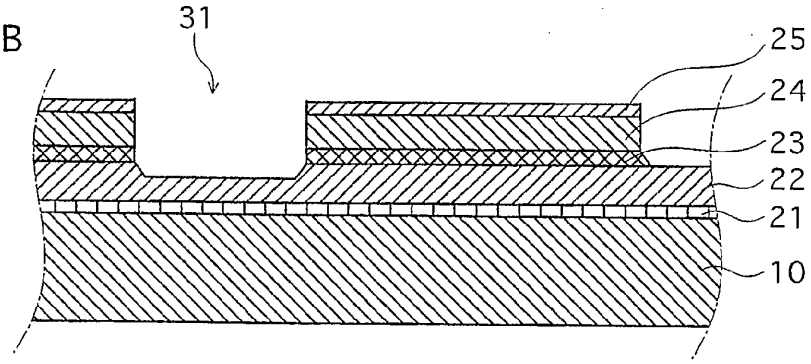


FIG.3C

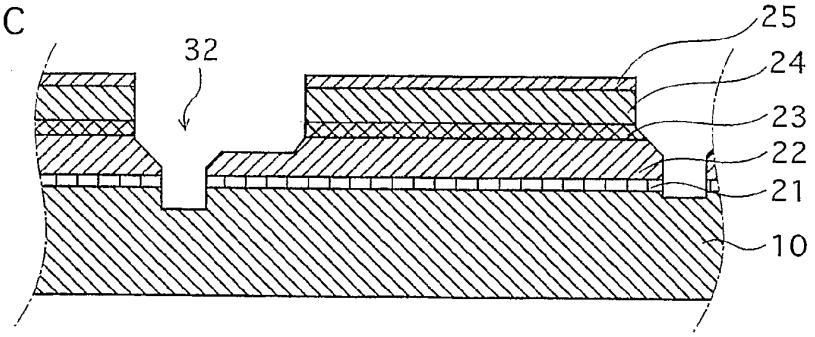
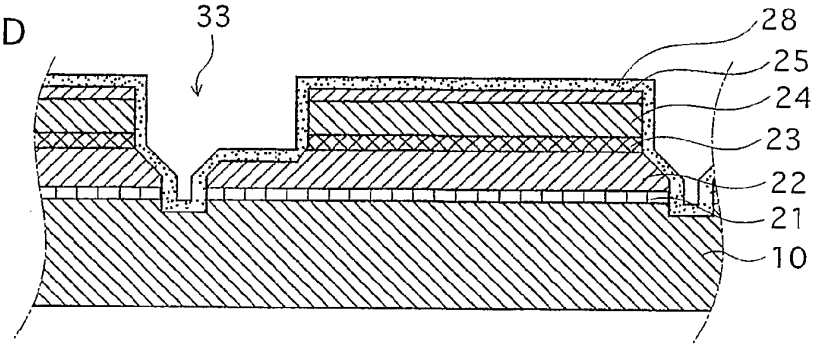


FIG.3D



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FIG.4E

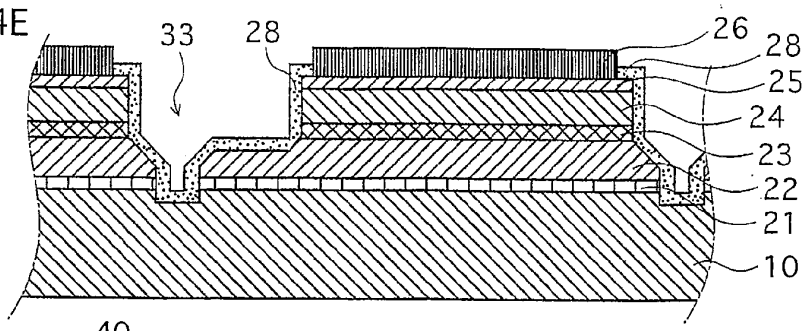


FIG.4F

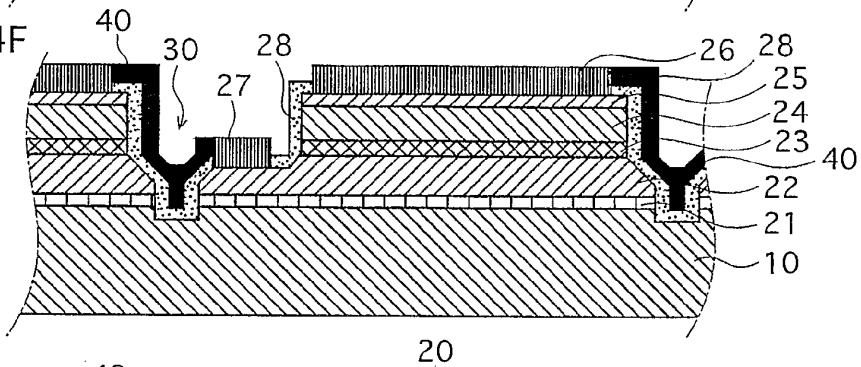


FIG.4G

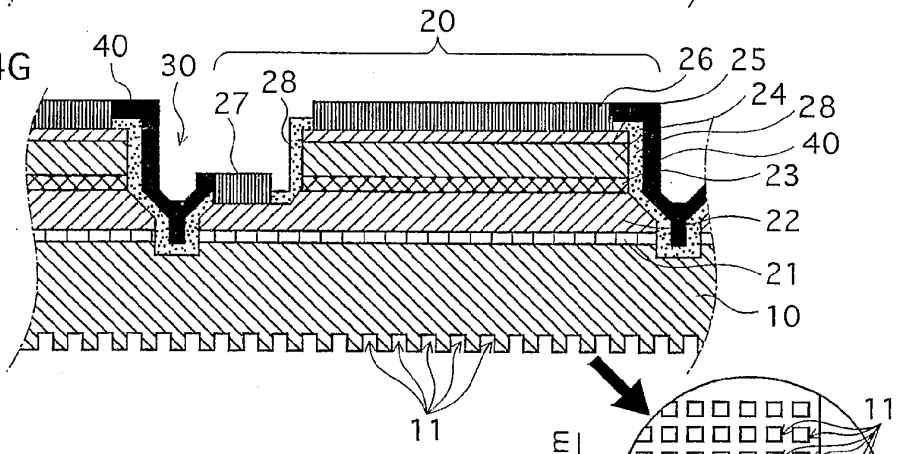
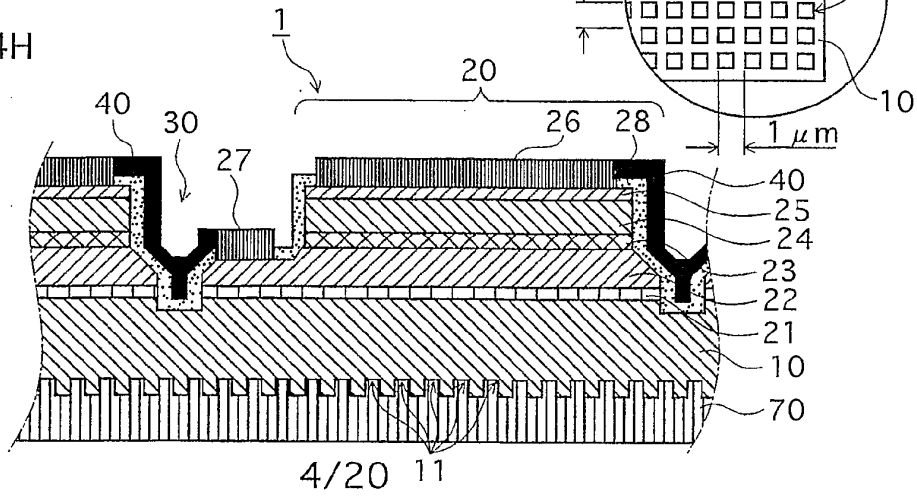


FIG.4H



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FIG.5A

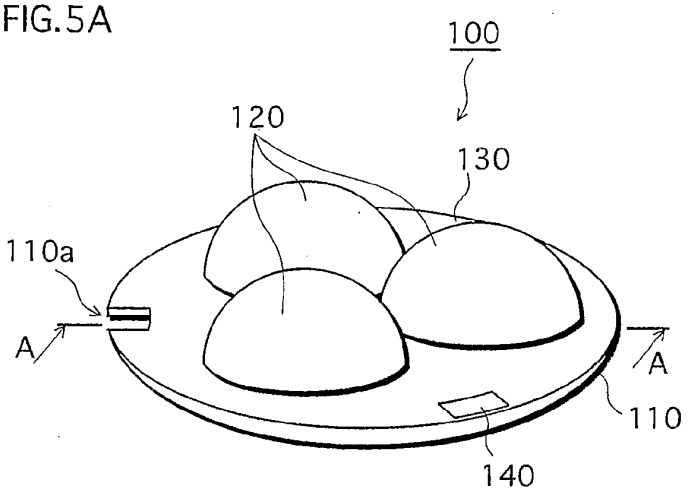
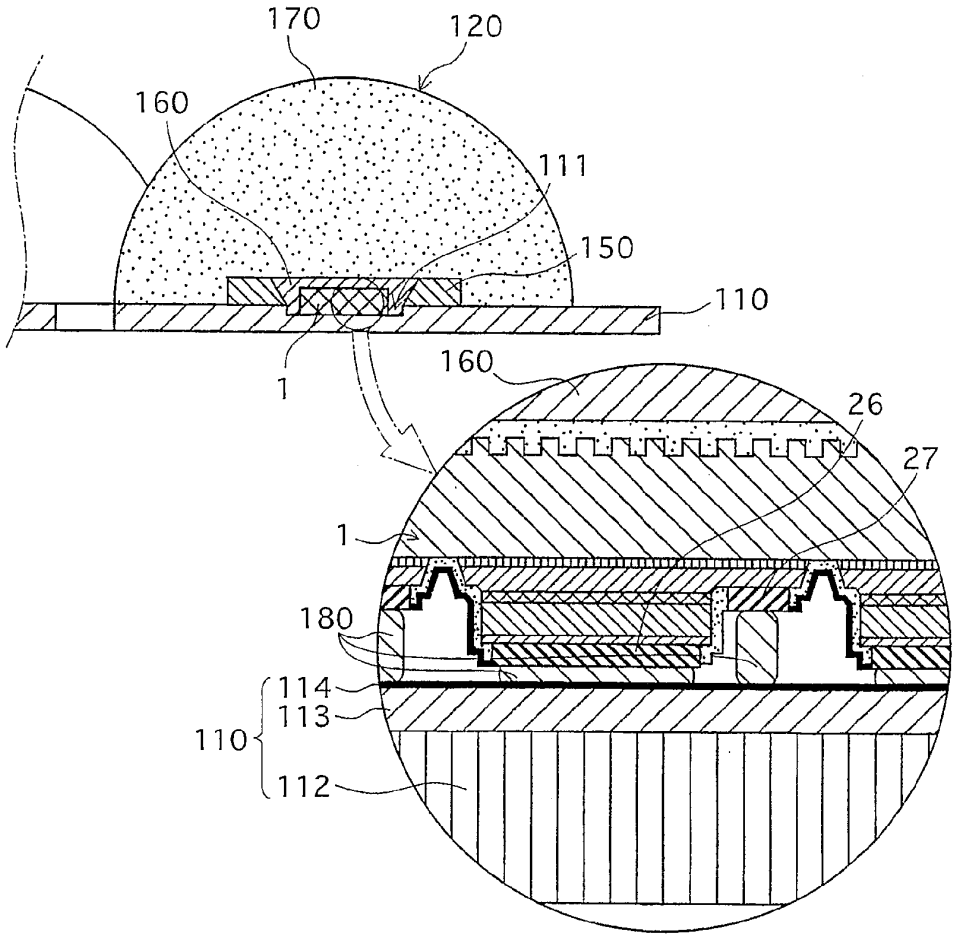
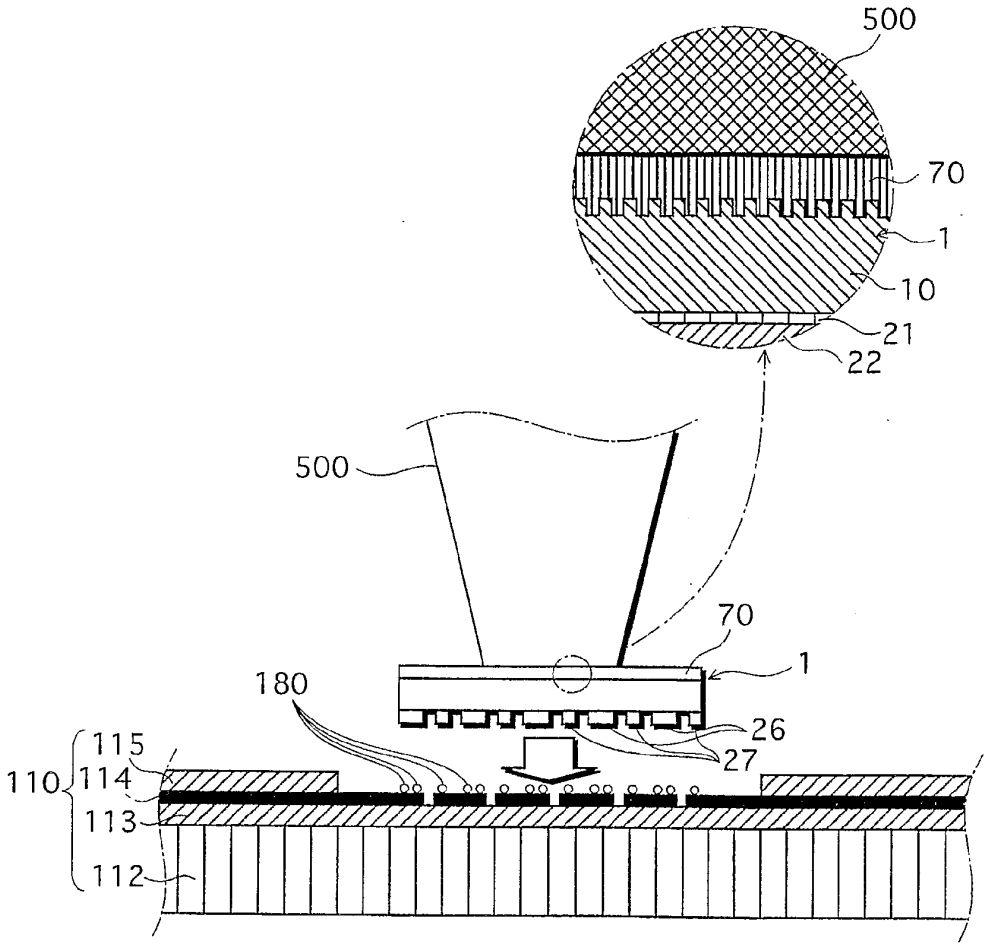


FIG.5B



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FIG.6



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FIG.7A

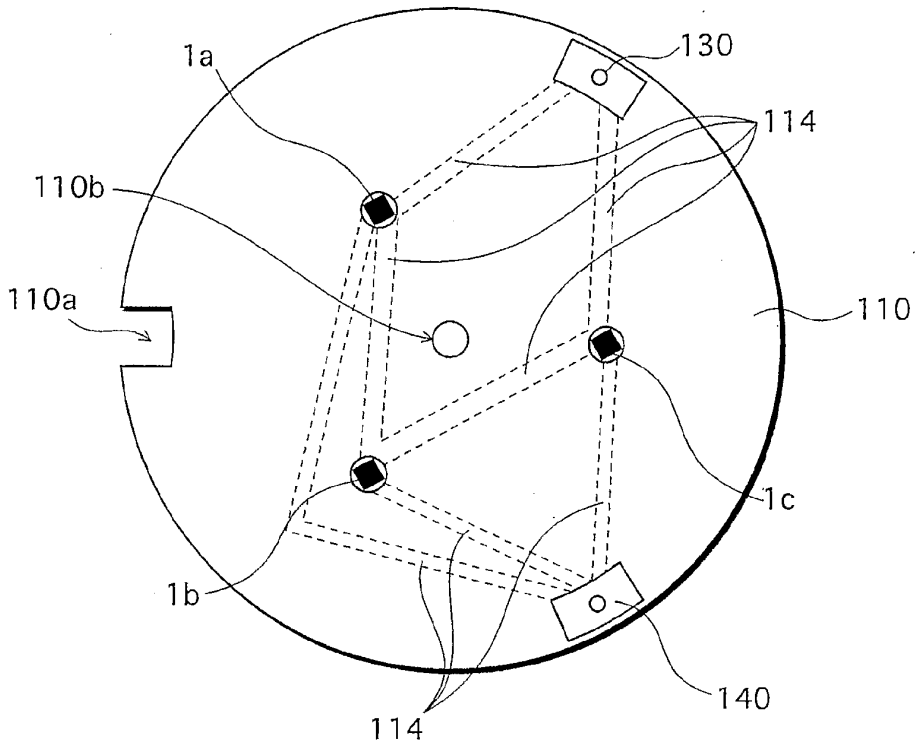
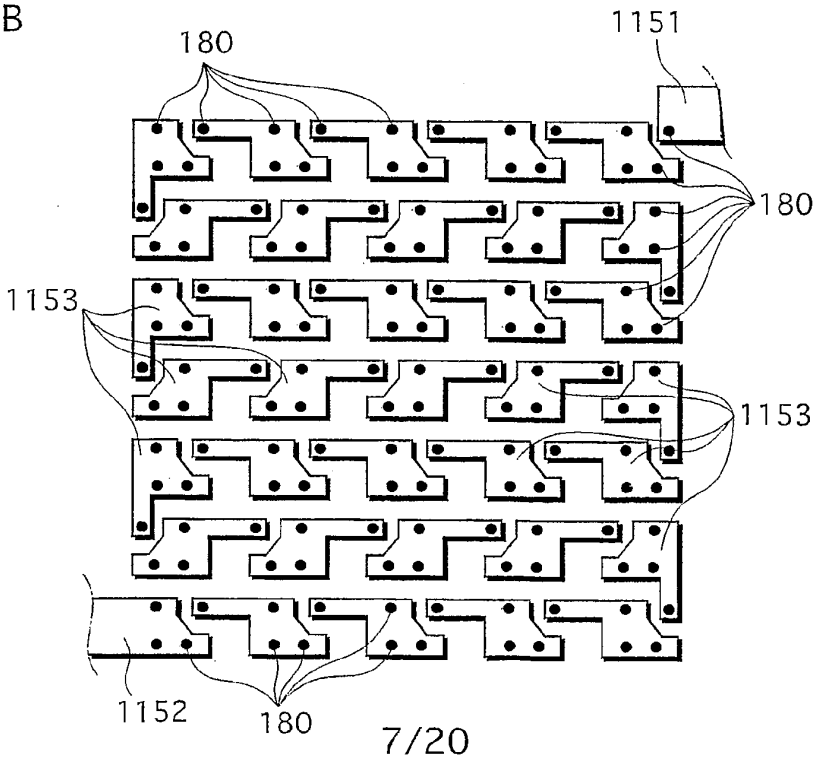


FIG.7B



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FIG.8A

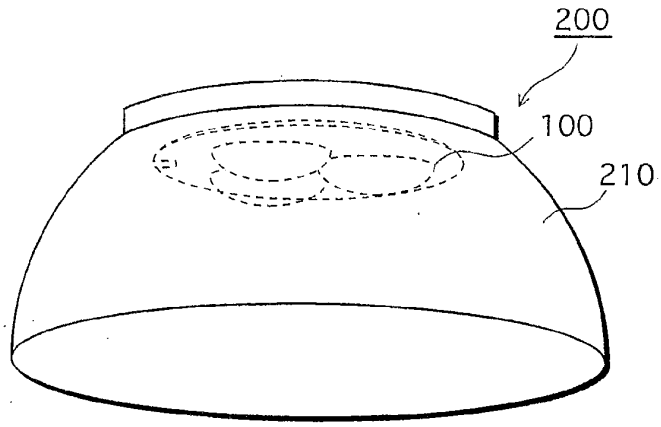
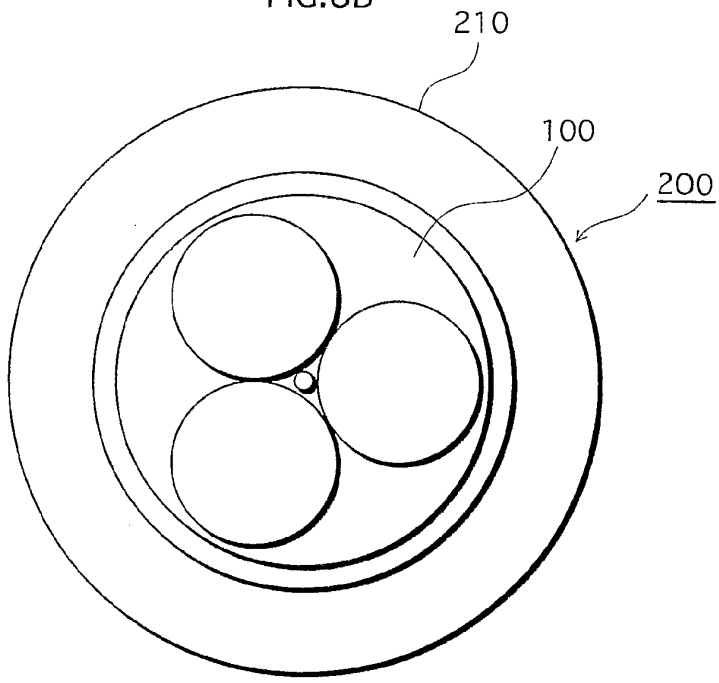
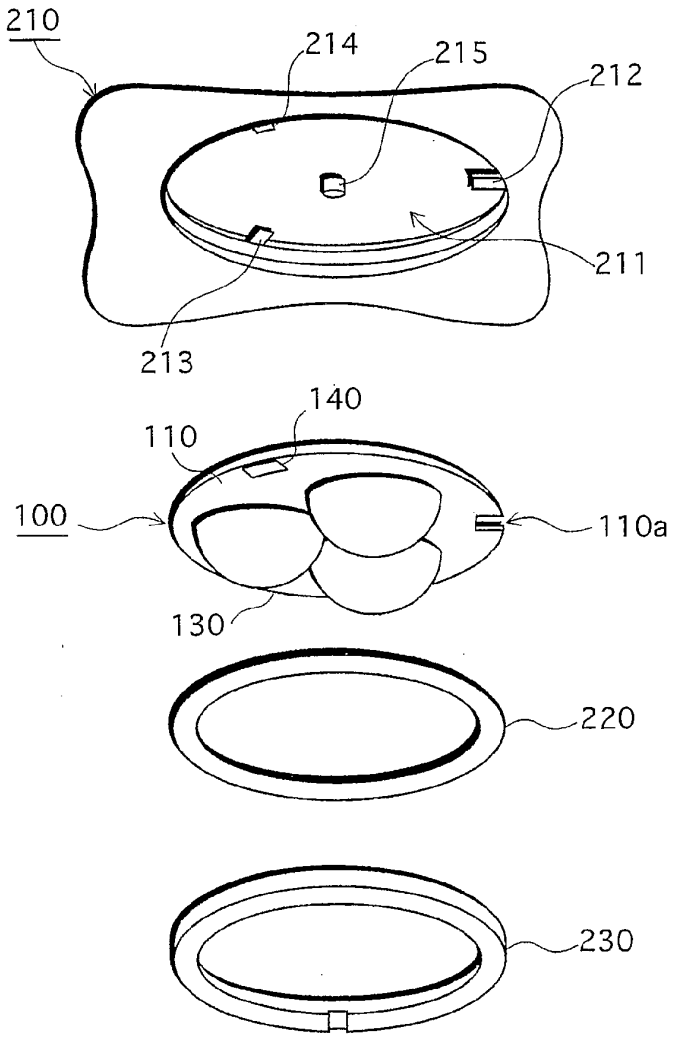


FIG.8B



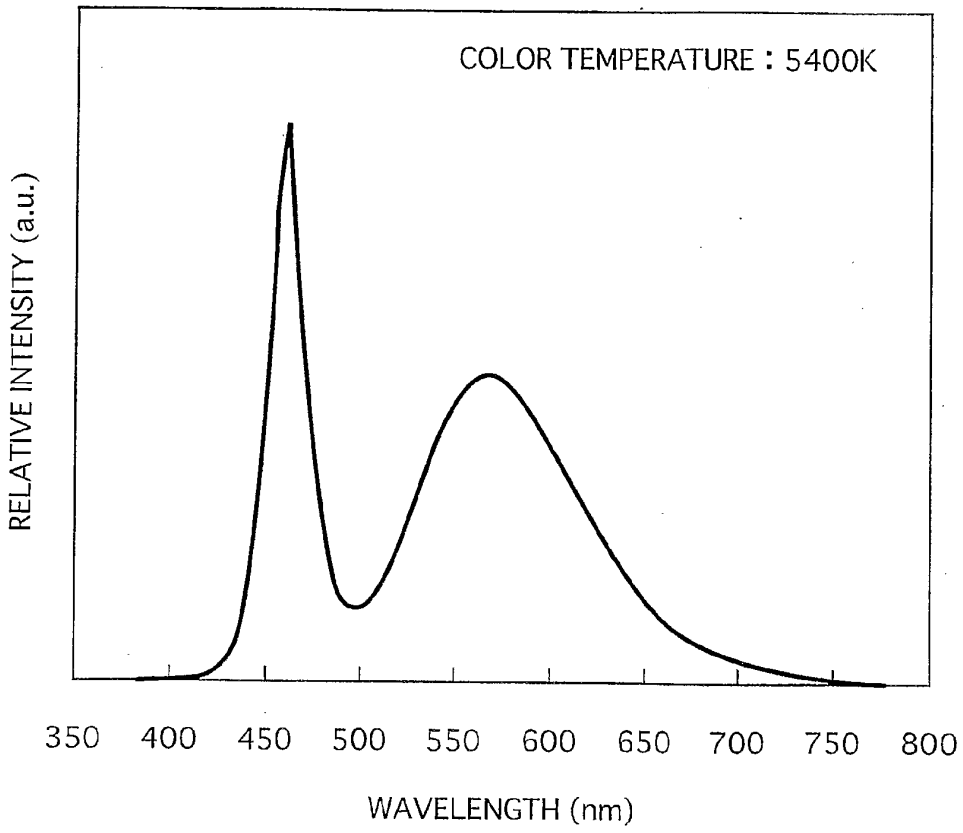
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FIG.9



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FIG.10



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FIG.11A

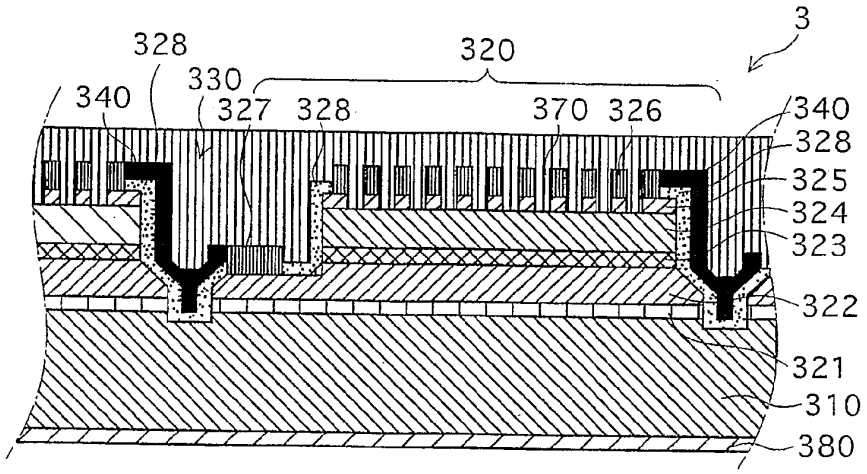
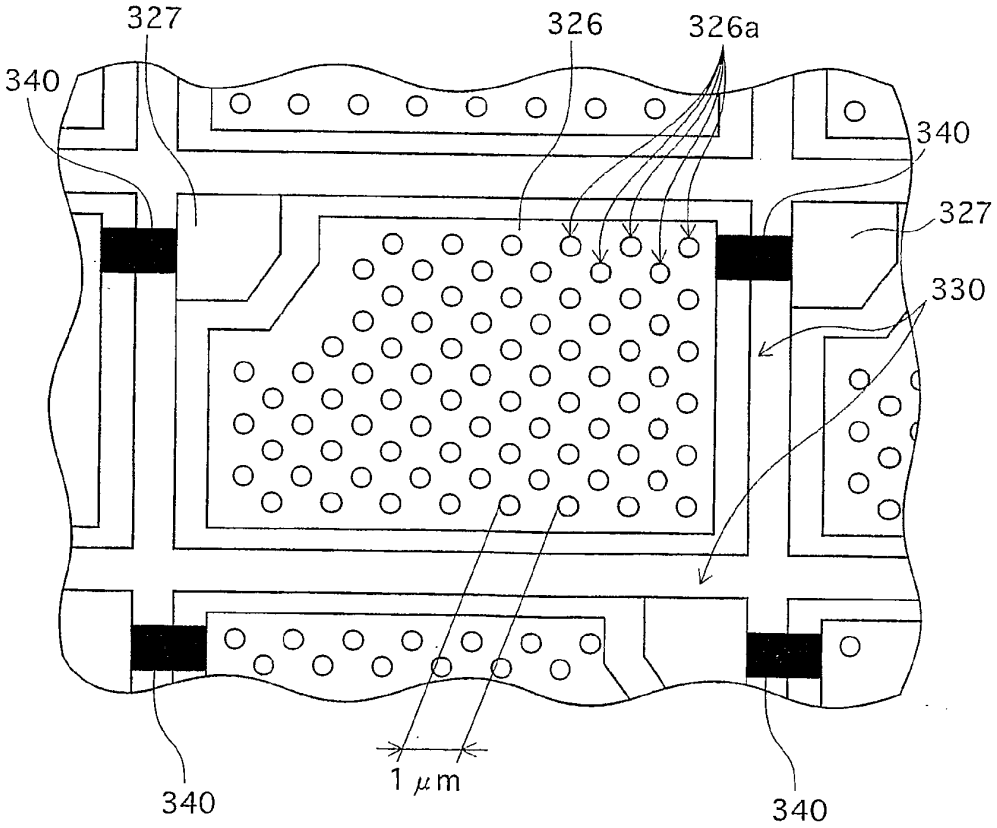


FIG.11B



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FIG.12A

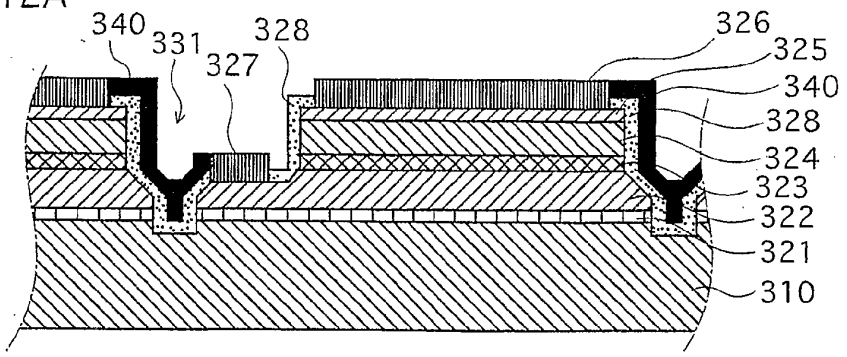


FIG.12B

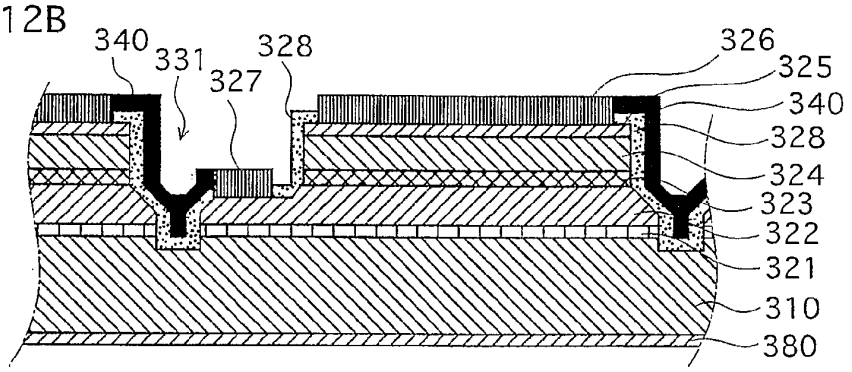


FIG.12C

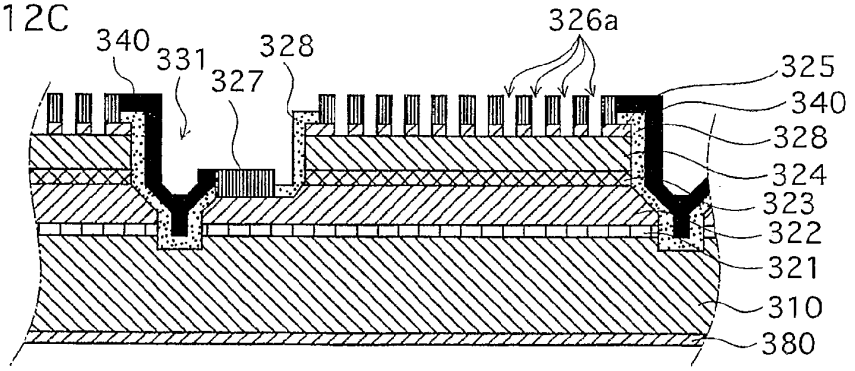
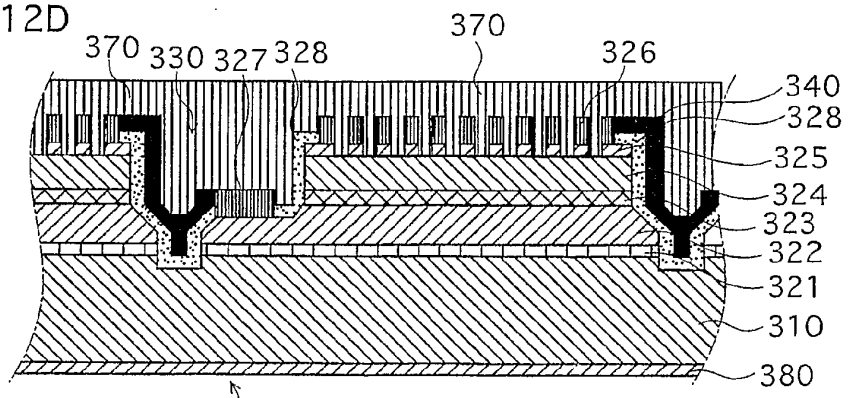


FIG.12D



3

SDOCID: <WO_____2005008791A2_I_>

FIG.13A

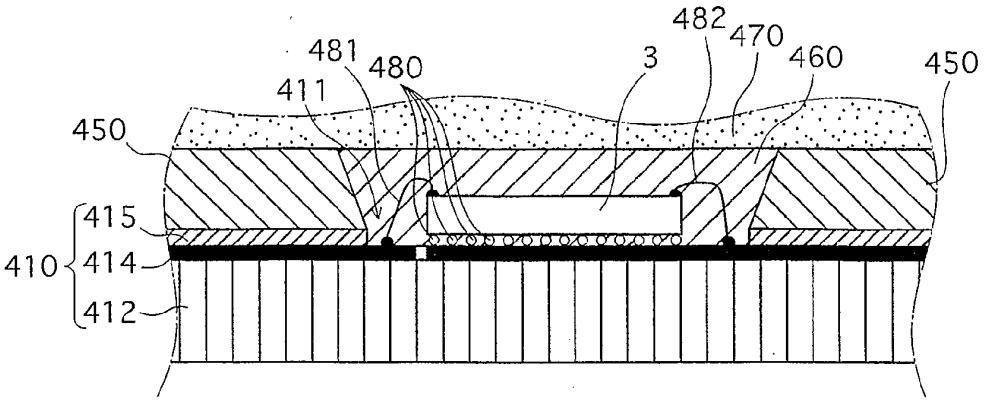
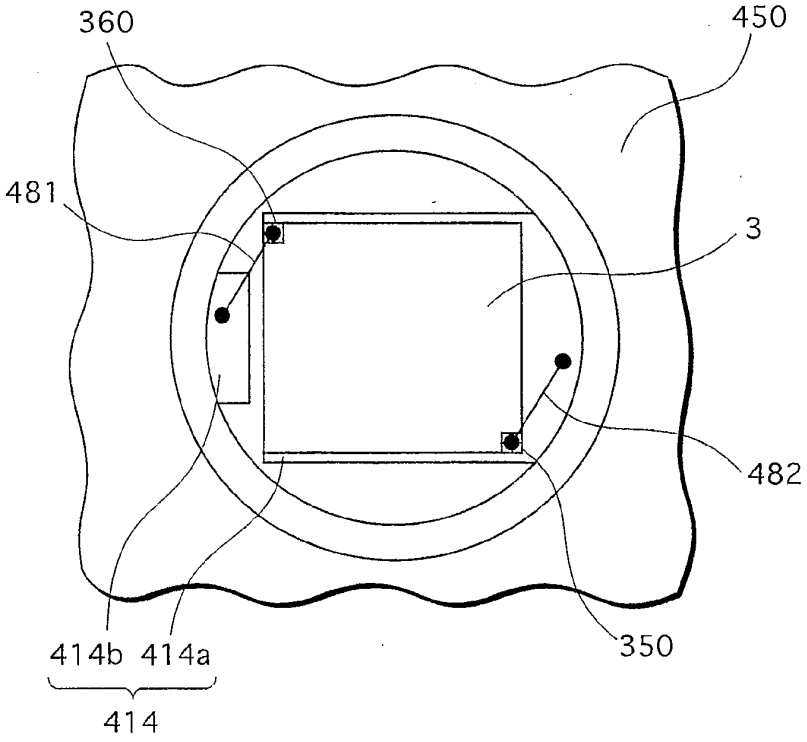
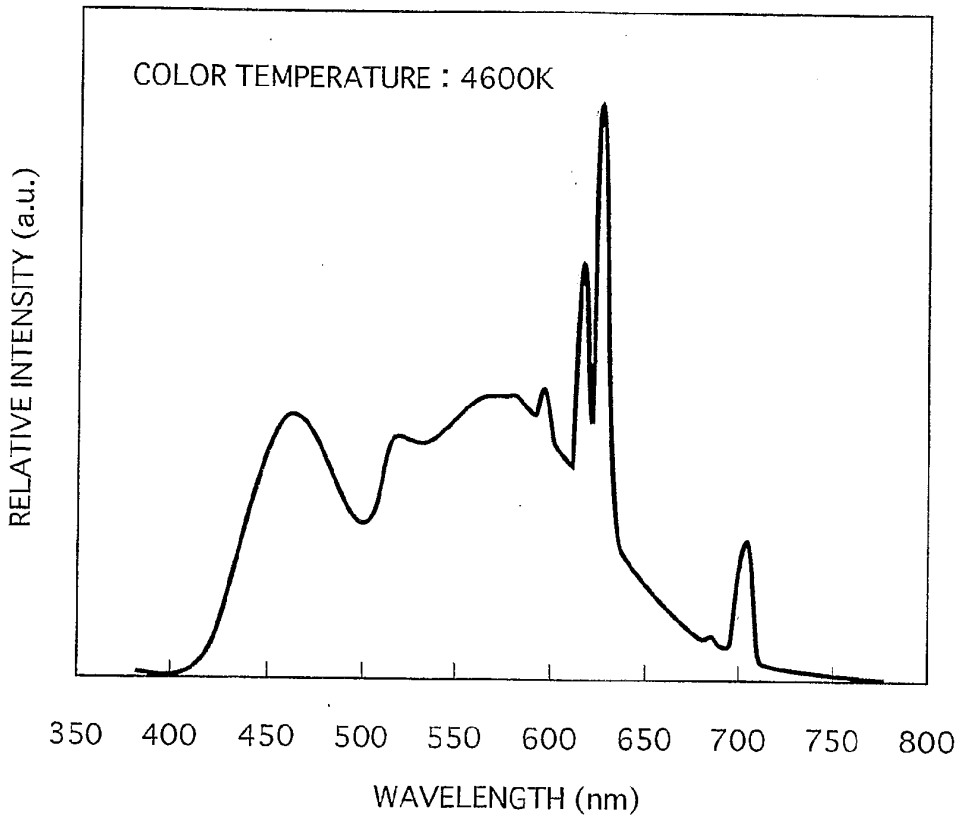


FIG.13B



BNSDOCID: <WO_____2005008791A2_I_>

FIG.14



ISDOCID: <WO_____2005008791A2_I_>

FIG.15A

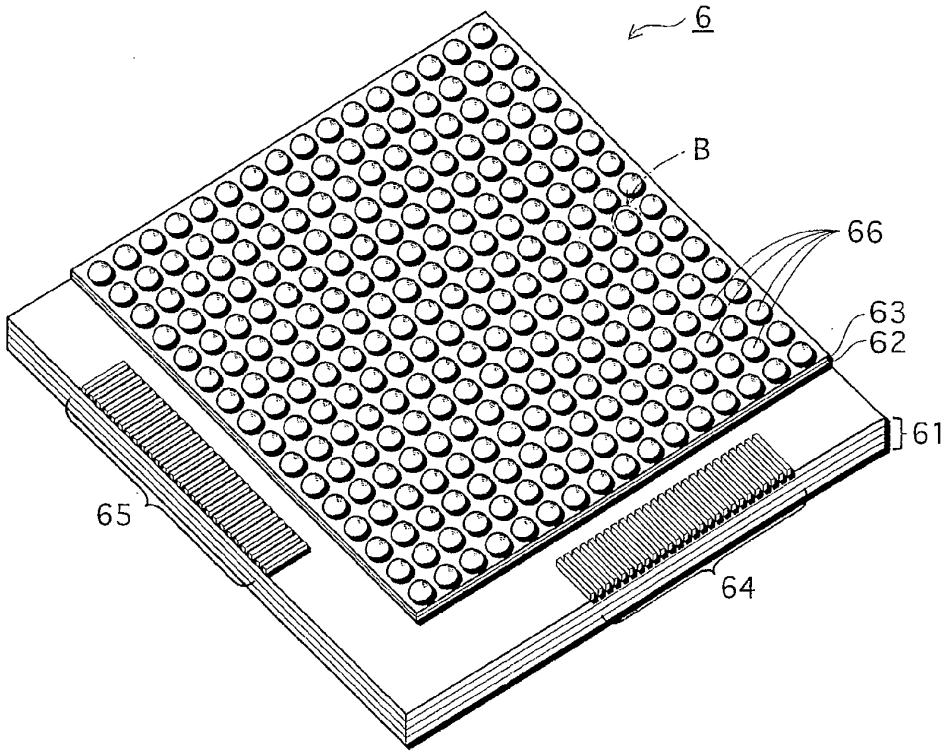
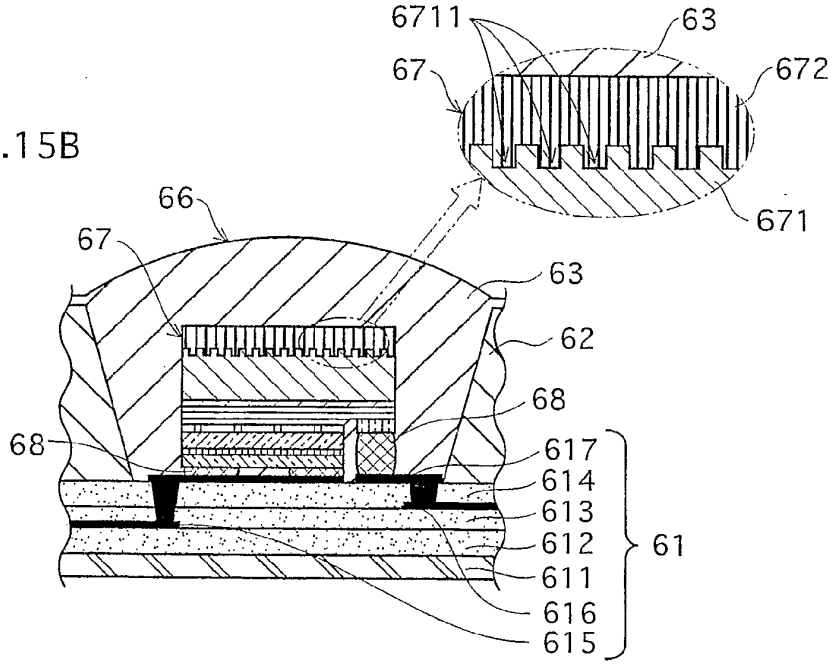


FIG.15B



BNSDOCID: <WO 2005008791A2_I_>

FIG.16A

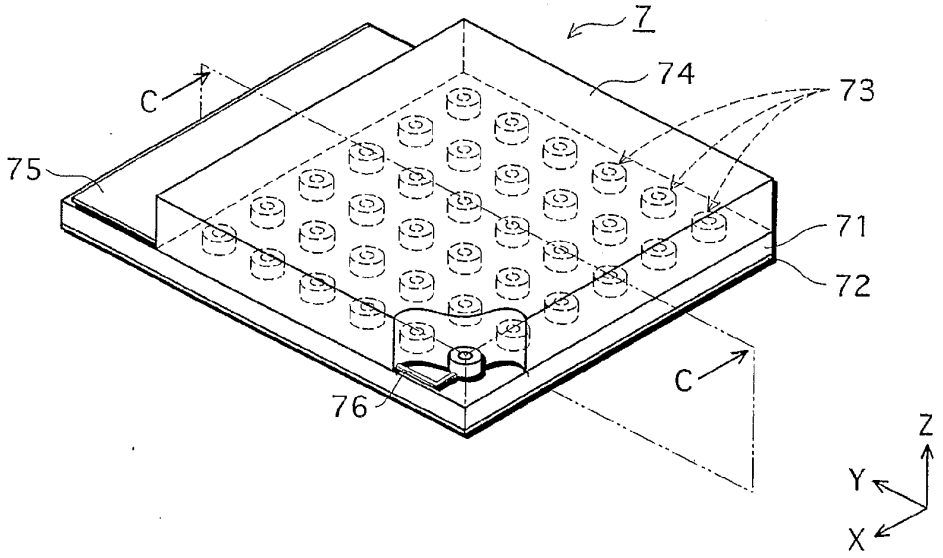
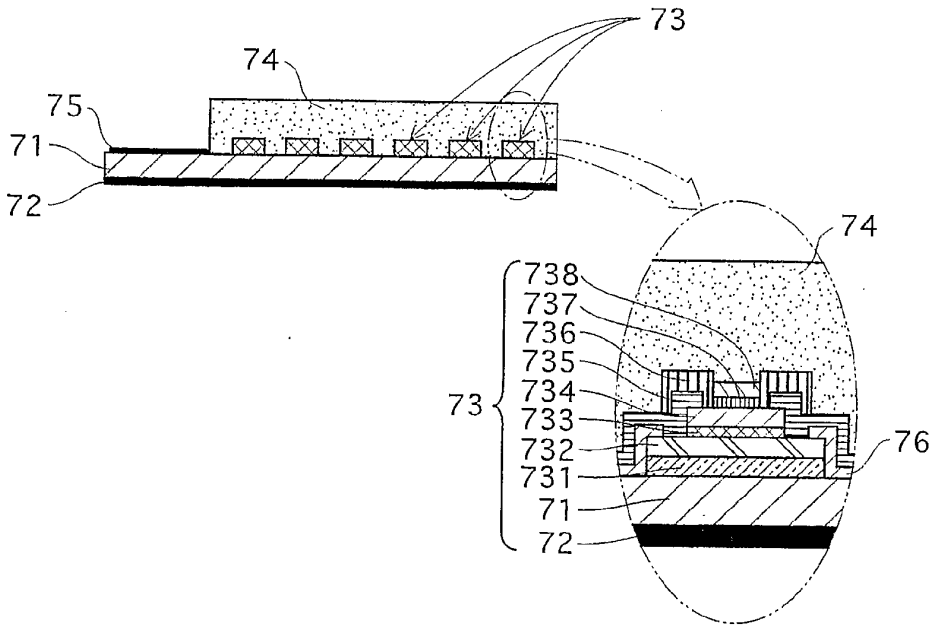


FIG.16B



ISDOCID: <WO_____2005008791A2_I_>

FIG.17A

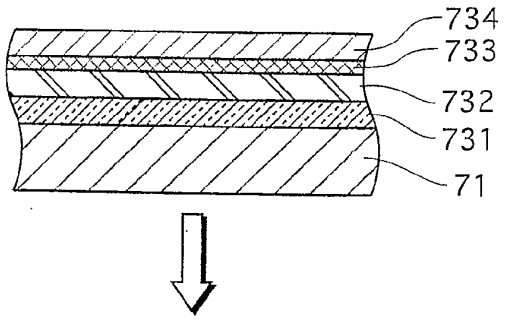


FIG.17B

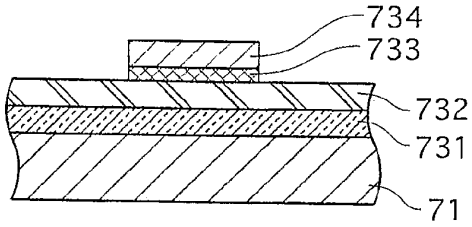


FIG.17C

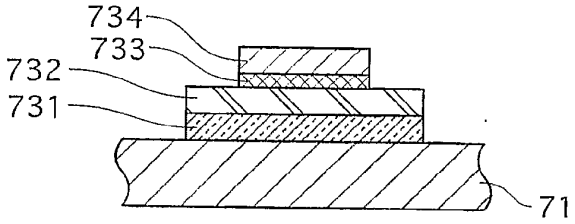
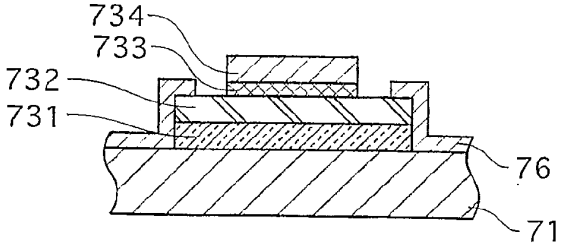


FIG.17D



BNSDOCID: <WO_ 2005008791A2_I_>

FIG.18E

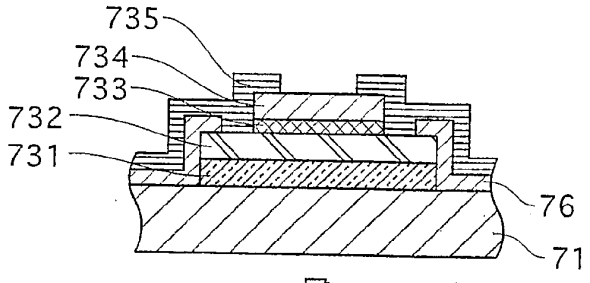


FIG.18F

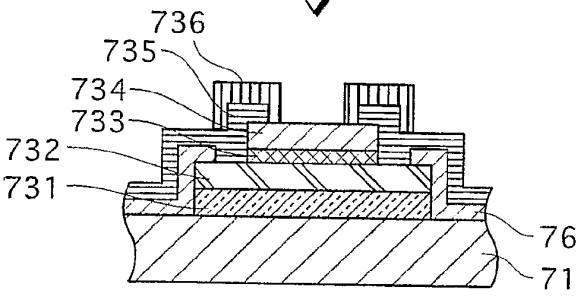


FIG.18G

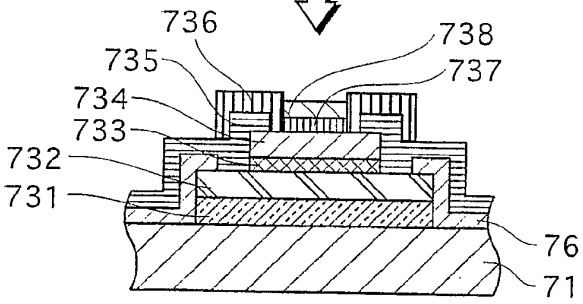
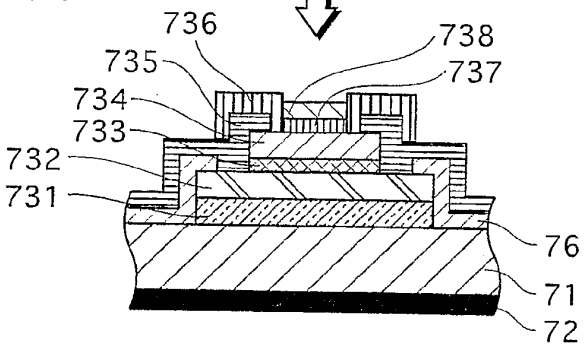
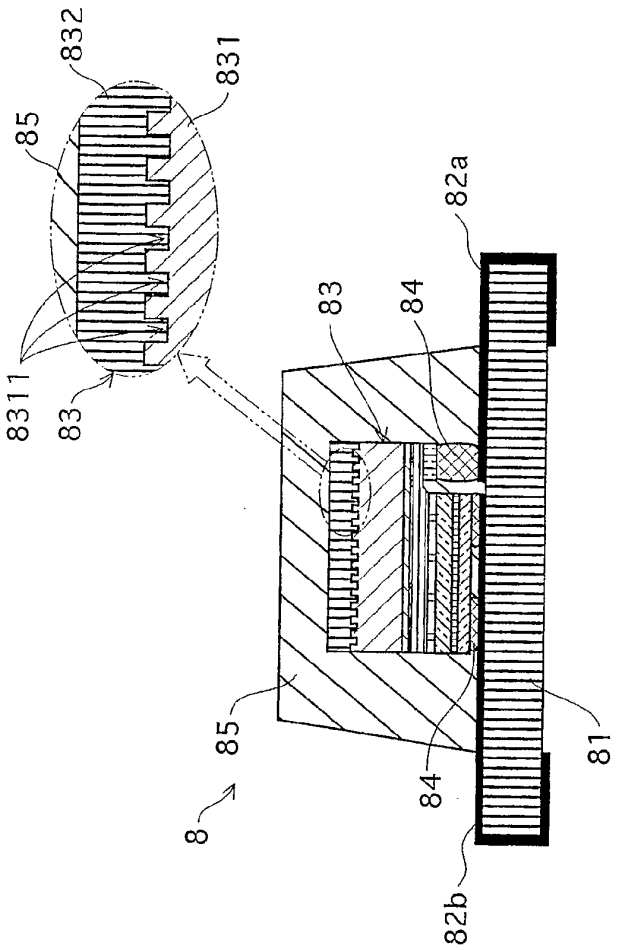


FIG.18H



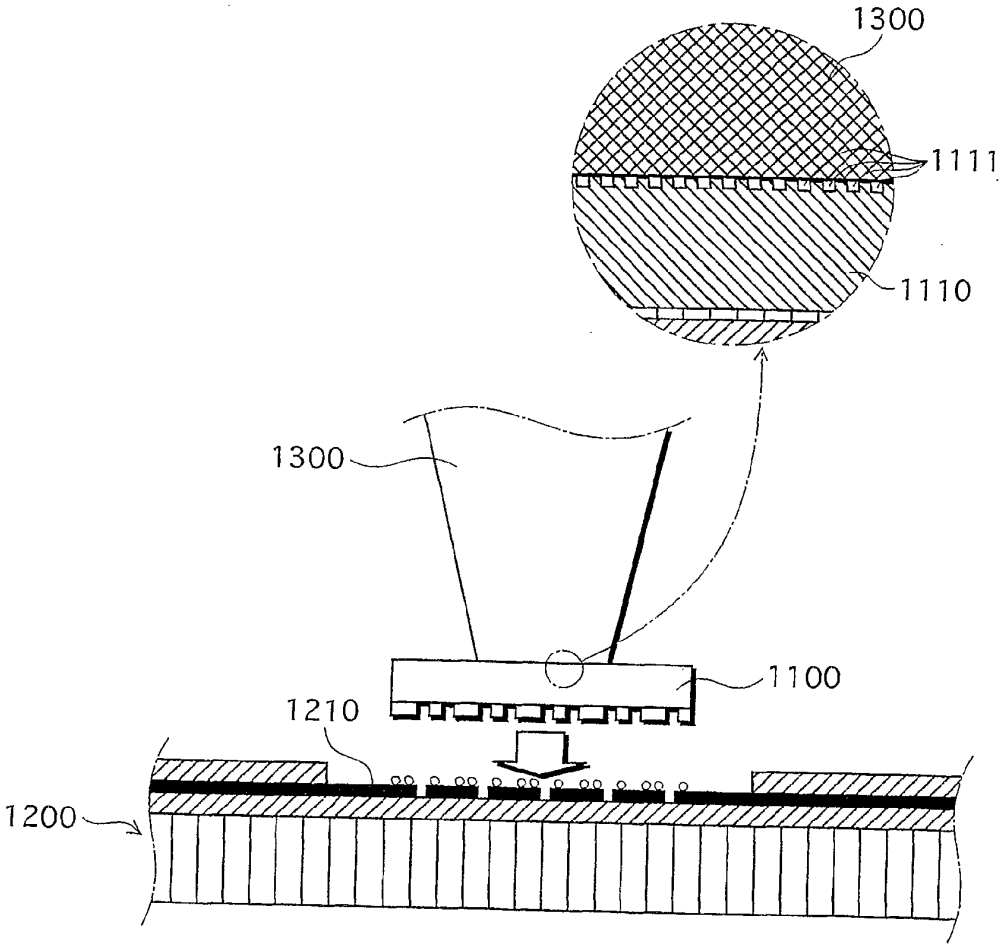
SDOCID: <WO_____2005008791A2_I_>

FIG.19



BNSDOCID: <WO_____2005008791A2_I_>

FIG.20



SDOCID: <WO____2005008791A2_I_>

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(71) Applicant *(for all designated States except US)*: MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. [JP/JP]; 1006, Oazakadoma, Kadoma-shi, Osaka 5718501 (JP).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: NAGAI, Hideo.

(74) Agent: NAKAJIMA, Shiro; 6F, Yodogawa 5-Bankan, 2-1 Toyosaki 3-chome, Kita-ku, Osaka-shi, Osaka 5310072 (JP).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

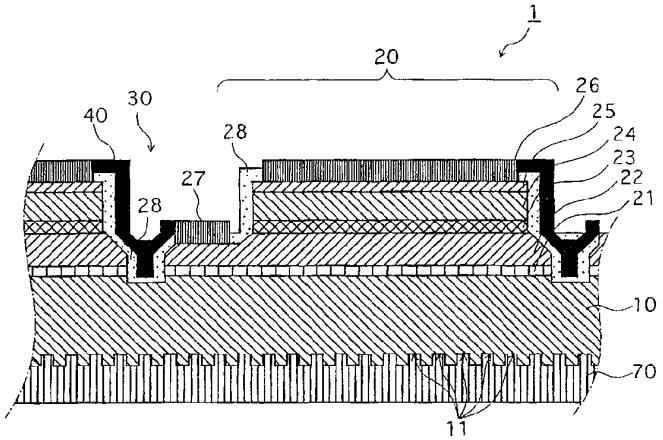
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
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[Continued on next page]

(54) Title: SEMICONDUCTOR LIGHT EMITTING DEVICE, METHOD OF MANUFACTURING THE SAME, AND LIGHTING APPARATUS AND DISPLAY APPARATUS USING THE SAME



(57) Abstract: The present invention aims to provide a semiconductor light emitting device (1) that may be firmly attached to a substrate with maintaining excellent light emitting efficiency, and a manufacturing method of the same, and a lighting apparatus and a display apparatus using the same. In order to achieve the above object, the semiconductor light emitting device (1) according to the present invention includes a luminous layer (23), a light transmission layer (10) disposed over a main surface of the luminous layer(23), and having depressions (11) on a surface facing away from the luminous layer (23), and a transmission membrane (70) disposed on the light transmission layer (10) so as to follow contours of the depressions, and light from the luminous layer (23) is irradiated so as to pass through the light transmission layer (10) and the transmission membrane (70).

WO 2005/008791 A3

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

PCT/JP2004/010244

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L33/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2001/010449 A1 (CHIU CHIEN-CHIA ET AL) 2 August 2001 (2001-08-02)	1,2,5-7, 11, 13-19, 21,22, 24,25,29
Y	paragraph '0040! - paragraph '0048!; figures 6,7	9,10,12, 20,23, 26-28,30
A		3,4,8
X	US 6 410 348 B1 (CHEN TZER-PERNG ET AL) 25 June 2002 (2002-06-25)	1-4,11, 14-19, 21,22,24
Y		8-10,20, 23,27,28
A	column 3, line 19 - column 4, line 65; figures 3-6	5-7,12, 13,25, 26,29,30

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 February 2005	07/03/2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Krause, J

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 162 878 A (SASAGAWA ET AL) 10 November 1992 (1992-11-10)	1,2, 14-17,24
A	column 4, line 61 - column 8, line 48; figures 4-7	3-13, 18-23, 25-30
X	EP 0 404 565 A (MITSUBISHI KASEI POLYTEC CO; MITSUBISHI KASEI CORP; MITSUBISHI KASEI C) 27 December 1990 (1990-12-27)	1,2,14, 24
A	page 3, line 16 - line 54; figure 1	3-13, 15-23, 25-30
X	US 6 495 862 B1 (OKAZAKI HARUHIKO ET AL) 17 December 2002 (2002-12-17)	1,14,24
A	column 4, line 1 - column 8, line 49; figures 1-3,6	2-13, 15-23, 25-30
Y	EP 0 361 602 A (PHILIPS ELECTRONICS UK LIMITED; N.V. PHILIPS' GLOEILAMPENFABRIEKEN; PH) 4 April 1990 (1990-04-04)	8
A	column 3, line 25 - line 49; figure 1	1,24
Y	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 06, 22 September 2000 (2000-09-22) -& JP 2000 077713 A (SANYO ELECTRIC CO LTD; TOTTORI SANYO ELECTRIC CO LTD), 14 March 2000 (2000-03-14) abstract	12,30
Y	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 23, 10 February 2001 (2001-02-10) -& JP 2001 177158 A (MATSUSHITA ELECTRONICS INDUSTRY CORP), 29 June 2001 (2001-06-29)	26
A	abstract	1,2,5-7, 14,18, 19,21, 22,25

INTERNATIONAL SEARCH REPORT

Information on patent family members

PCT/JP2004/010244

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2001010449 A1	02-08-2001	TW 465123 B	21-11-2001
		JP 2001217467 A	10-08-2001
US 6410348 B1	25-06-2002	TW 445507 B	11-07-2001
		US 2002134985 A1	26-09-2002
US 5162878 A	10-11-1992	JP 4264781 A	21-09-1992
EP 0404565 A	27-12-1990	JP 2953468 B2	27-09-1999
		JP 3024771 A	01-02-1991
		DE 69008931 D1	23-06-1994
		DE 69008931 T2	08-12-1994
		EP 0404565 A1	27-12-1990
		KR 179952 B1	20-03-1999
		US 5040044 A	13-08-1991
US 6495862 B1	17-12-2002	JP 3469484 B2	25-11-2003
		JP 2000196152 A	14-07-2000
		US 2003062530 A1	03-04-2003
EP 0361602 A	04-04-1990	GB 2223352 A	04-04-1990
		EP 0361602 A2	04-04-1990
		JP 2123784 A	11-05-1990
JP 2000077713 A	14-03-2000	NONE	
JP 2001177158 A	29-06-2001	NONE	

Electronic Acknowledgement Receipt

EFS ID:	7113336
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
Receipt Date:	01-MAR-2010
Filing Date:	26-DEC-2007
Time Stamp:	17:23:06
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	2010-03-01_P2317US00_IDS.pdf	33432 429cdb8a3bd69898236e862ee1a54376430eda0b	no	4
Warnings:					
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2	Foreign Reference	2010-03-01_P2317US_IDSRefEP1469529.pdf	474700 409bca7e4a01fed115c271c8deaa21a5e1da3ede	no	14
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3	NPL Documents	2010-03-01_P2317US_IDSRefEPSearchReport.pdf	365255 a0ade83f77732a7bbc171880c1bf5f94d6d95e17	no	9
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4	Foreign Reference	2010-03-01_P2317US_IDSRefJP2004006582.pdf	831282 97c084267aaa94e0a826a3bfe4377bc4ed4cdff9	no	17
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5	Foreign Reference	2010-03-01_P2317US_IDSRefWO2005008791.pdf	3289914 93de5f4bb95cb120f6d69c0ccafb056db9474b1b	no	82
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	Docket No.: P2317US00
Jong Lam LEE, *et al.*	
Serial No.: 11/993,965	Group Art Unit: 2818
Confirmation No.: 2191	
Filed: December 26, 2007	Examiner: NGUYEN, Thinh T.

For: **LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME**

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY UNDER 37 C.F.R. § 1.111

Sir:

In response to the Non-Final Office Action dated February 5, 2010 ("Office Action"), Applicants respectfully request reconsideration of the application in view of the following Amendments and Remarks.

Amendments to the Specification begin on page 2.

Amendments to the Claims begin on page 4.

Remarks begin on page 9.

Applicants believe that no extensions of time are required at this time. If extensions of time are necessary to prevent abandonment of this application, then they are hereby petitioned for under 37 C.F.R. § 1.136(a). Applicants submit a fee in the amount of $104 for the addition of two dependent claims. Any fees required for further extensions of time and any fees for the net addition of claims are hereby authorized to be charged to our Deposit Account No. 50-3698.

AMENDMENTS TO THE SPECIFICATION

On page 1, prior to "BACKGROUND OF THE INVENTION" please insert the following section heading and paragraph:

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a U.S. national phase application of PCT International Application No. PCT/KR2006/002427, filed June 22, 2006, which claims priority of Korean Patent Application No. 10-2005-0053797, filed June 22, 2005, Korean Patent Application No. 10-2005-0055179, filed June 24, 2005 and Korean Patent Application No. 10-2006-0021801, filed March 8, 2006 the contents of which are incorporated herein by reference in their entirety.

Please replace paragraph [0064] with the following:

[0064] Next, in order to form a plurality of light emitting cells on the substrate 10, predetermined regions of the exposed N-type semiconductor layer 20 are removed such that a portion of the substrate 10 can be exposed. To this end, a predetermined mask pattern is formed on all the portions except the predetermined regions where the substrate 10 will be exposed, and regions of the N-type semiconductor layer 20 that are exposed through the mask pattern are then etched such that the plurality of light emitting cells can be electrically isolated from one another as shown in Fig. 8. At this time, the mask pattern whose side surface is inclined through the aforementioned process is formed and then used to etch the exposed N-type semiconductor layer 20 such that the side surfaces of the [[N]] P-type semiconductor layer 20 and the active layer 30 ~~in which the plurality of light emitting cells are separated from one another is~~ are not perpendicular to but inclined at a predetermined slope from a horizontal plane.

Please replace paragraph [0078] with the following:

[0078] Further, even in a case where the plurality of light emitting cells are separated by etching such that the side surfaces may have various slopes as shown in Fig. 10 and then etched to expose the N-type semiconductor layer 20, a light emitting device can be manufactured using

the same etching process as described above. That is, as shown in Fig. [[11]] 13, the side surfaces of the P-type semiconductor layer 40 and the active layer 30, which are etched to expose the N-type semiconductor layer 20, can be formed at various slopes.

AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 1, 2, 4, and 17-31as shown below.

Please **CANCEL** claim 3 without prejudice or disclaimer.

Please **ADD** claims 32-35.

This claim list replaces all prior claim lists in the application.

1. (Currently Amended) A light emitting device, comprising:

a plurality of light emitting cells each ~~including~~ comprising an N-type semiconductor layer and a P-type semiconductor layer formed on a portion of the N-type semiconductor layer on a substrate,

wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface ~~including~~ comprising the N-type or P-type semiconductor layer of the light emitting cell has a slope of approximately 20° to approximately 80° from a horizontal plane based on the substrate, wherein a transparent electrode layer is disposed on the P-type semiconductor layer to dissipate heat away from the P-type semiconductor layer.

2. (Currently Amended) The light emitting device as claimed in claim 1, further comprising:

a wire ~~for connecting~~ to couple the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

3. (Canceled)

4. (Currently Amended) The light emitting device as claimed in claim 1, further comprising:

P-type and N-type ohmic metal layers ~~containing~~ comprising Cr or Au on the P-type and N-type semiconductor layers, respectively.

5-16. (Canceled)

17. (Currently Amended) A light emitting device comprising:

a substrate; and

a plurality of light emitting cells disposed on the substrate ~~to be~~ being spaced apart from each other,

wherein the light emitting cell comprises a first[[-type]] semiconductor layer and a second[[-type]] semiconductor layer,

at least one of the light emitting cells has at least one side surface that is not perpendicular to a horizontal plane based on the substrate, and

the first[[-type]] semiconductor layer of at least one of the light emitting cells is ~~electrically connected~~ coupled to the second[[-type]] semiconductor layer of an another adjacent ~~another~~ light emitting cell, wherein a transparent electrode layer is disposed on the second semiconductor layer to dissipate heat away from the second semiconductor layer.

18. (Currently Amended) The light emitting device as claimed in claim 17, wherein the at least one side surface ~~that is not perpendicular is inclined~~ has an inclination angle ~~at a slope~~ with respect to the horizontal plane.

19. (Currently Amended) The light emitting device as claimed in claim 18, wherein the ~~slope~~ inclination angle is approximately 20˚ to approximately 80˚ with respect to the horizontal plane.

20. (Currently Amended) The light emitting device as claimed in claim 18, wherein the inclined surface of the light emitting cell comprises at least a side surface of the first[[-type]] semiconductor layer.

21. (Currently Amended) The light emitting device as claimed in claim 20, wherein the first[[-type]] semiconductor layer is an N[[-type]] semiconductor layer.

22. (Currently Amended) The light emitting device as claimed in claim 20, wherein the inclined surface of the light emitting cell is formed continuously up to the second[[-type]] semiconductor layer.

23. (Currently Amended) The light emitting device as claimed in claim 22, wherein the second[[-type]] semiconductor layer is a P[[-type]] semiconductor layer.

24. (Currently Amended) The light emitting device as claimed in claim 22, wherein the second[[-type]] semiconductor layer of the light emitting cell comprises at least one surface not being inclined ~~that is not inclined~~.

25. (Currently Amended) The light emitting device as claimed in claim 20, wherein at least one of the light emitting cells further comprises:

a first[[-type]] bonding pad and a second[[-type]] bonding pad ~~that are~~ disposed respectively on the first[[-type]] semiconductor layer and the second[[-type]] semiconductor layer.

26. (Currently Amended) The light emitting device as claimed in claim 25, wherein ~~the electrical connection is configured to electrically connect~~ the first[[-type]] bonding pad is disposed on the first[[-type]] semiconductor layer of ~~at least~~ one of the light emitting cells to couple the second[[-type]] bonding pad disposed on the second[[-type]] semiconductor layer of the ~~adjacent~~ another adjacent light emitting cell.

27. (Currently Amended) The light emitting device as claimed in claim 26, wherein ~~the~~

~~electrical~~ connections between the light emitting cells are provided using the bonding pads ~~is formed through the same process~~ .

28. (Currently Amended) The light emitting device as claimed in claim 27, wherein providing the ~~same process comprises~~ bonding pads comprises utilizing at least one of plating method, chemical vapor deposition (CVD), physical vapor deposition (PVD), ~~and~~ or electron beam deposition.

29. (Currently Amended) The light emitting device as claimed in claim 26, wherein the ~~electrical~~ connection is ~~formed~~ provided by an electrical conductor disposed on the inclined surface of the light emitting cell.

30. (Currently Amended) The light emitting device as claimed in claim 29, wherein an insulation layer is disposed to continuously cover a surface of the substrate, ~~between~~ a top and the inclined surface of the light emitting cell and the electrical conductor.

31. (Currently Amended) The light emitting device as claimed in claim 20, further comprising:

Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof disposed on a rear surface of the substrate on which the light emitting cell is formed to enhance the heat dissipation.

32. (New) The light emitting device as claimed claim 1, wherein the substrate comprises a front surface and a rear surface, wherein the light emitting cells are disposed on the front surface and Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof is disposed on the rear surface to enhance the heat dissipation.

33. (New) The light emitting device as claimed claim 1, wherein an insulation layer is disposed continuously to cover a surface of the substrate, a top and the inclined surface of the

light emitting cells.

34. (New) The light emitting device as claimed in claim 1, wherein the transparent electrode layer is selected from ITO (Indium Tin Oxide), ZnO (Zinc Oxide) or a conductive transparent metal.

35. (New) The light emitting device as claimed in claim 17, wherein the transparent electrode layer is selected from ITO (Indium Tin Oxide), ZnO (Zinc Oxide) or a conductive transparent metal.

REMARKS

Claims 1, 2, 4, and 17-31 have been amended, claim 3 has been canceled without prejudice or disclaimer, and new claims 32-35 have been added. Accordingly, claims 1, 2, 4 and 17-35 are currently pending in the application, of which claims 1 and 17 are independent.

Care has been exercised to avoid the introduction of new matter. Adequate descriptive support for the present Amendment is apparent throughout the originally filed disclosure noting, for example, paragraphs [0069], [0077], [0082], [0138], [0151] and [0152] of Substitute Specification, as well as various figures, e.g., FIG. 13-17.

In view of the above amendments, and the following Remarks, Applicants respectfully request reconsideration and timely withdrawal of the pending objections and rejections for the reasons discussed below.

Objections to the Drawings

Objection has been made to the drawings under 37 C.F.R. 1.83(a) for lacking illustration of "Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof disposed on a rear surface of the substrate on which the light emitting cell is formed." (Office Action, page 2) Reconsideration of the requirement for additional drawing content is respectfully solicited. 37 C.F.R. 1.83(a) merely requires that the drawings in an application show every feature of the invention specified in the claims. It seems that the Examiner misconstrues "every feature of the invention." The rule specifies content of drawings, for example, "detailed illustration is not essential for a proper understanding of the invention." Furthermore, the rule clearly guides not to include "sequence listings" and "tables" that are included in the Specification. A purpose for this rule prohibits unnecessary complexity attributed to the listings and tables. This rationale is captured by the 35 USC 113, which states "The applicant shall furnish a drawing **where necessary for the**

understanding of the subject matter sought to be patented." In fact, the claimed "Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof" is included in the paragraphs [0055], [0069] and [0077]. Since every features of the invention, in fact, is illustrated in the drawings– see, e.g., FIGs. 4-17, figure item No. 10, and the claimed "Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof" are included in the Specification, therefore, the requirements of 37 C.F.R. 1.83(a) are met. It is submitted, therefore, that withdrawal of the objection is warranted.

Claim Objection

Claim 31 was objected to for lack of enablement that can make the claim not in compliance with 35 U.S.C. § 112 first paragraph because Applicant fails to show what kind of structure of embodiment the, -- "Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof disposed on a rear surface of the substrate on which the light emitting cell is formed." – in claim 31 can take. (Office Action, page 3)

With respect to the rejection to claim 31 under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement, Applicants respectfully disagree. For example, the Specification, paragraph [0037], discloses following (Emphasis added.):

> **[0037]** The aforementioned process of manufacturing a light emitting device according to the present invention is merely a specific embodiment but is not limited thereto. Various modifications can be made or various material films can be further added. For example, in order to enhance the heat dissipation characteristic of a light emitting device, **after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10**.

From the above passage, it is clear that one of ordinary skill in the art can make and use the claimed invention without undue experimentation. Namely, according to the above example, an artisan can deposit the above chemical element listing on the rear surface of the substrate according to the disclosure.

In order to make a rejection, the Examiner has the initial burden to establish a reasonable basis to question the enablement provided for the claimed invention. *In re Wright,* 999 F.2d 1557,1562, 27 USPQ2d 1510, 1513 (Fed. Cir. 1993). (examiner must provide a reasonable explanation as to why the scope of protection provided by a claim is not adequately enabled by the disclosure). A conclusive and a vague statement – "fails to show what kind of structure of embodiment [sic of] the . . . light emitting cell is formed" is not a reasonable explanation. Further, MPEP §2164.03 states that "[t]he more that is known in the prior art about the nature of the invention, how to make, and how to use the invention, and the more predictable the art is, the less information needs to be explicitly stated in the specification."

Moreover, it is incumbent upon the Patent Office, whenever a rejection on this basis is made, to explain why it doubts the truth or accuracy of any statement in a supporting disclosure and to back up assertions of its own with acceptable evidence or reasoning which is inconsistent with the contested statement. Otherwise, there would be no need for the applicant to go to the trouble and expense of supporting his presumptively accurate disclosure. *In re Mazrocchi*, 439 F.2d 224, 169 USPQ 370 (CCPA 1971). Here, the Examiner merely arrives to a conclusion without providing any reasoning as to why, much less reasoning showing why the Specification lacks enabling description.

Based on the foregoing, Applicants submit that the Examiner has not met his burden with respect to the enablement requirement, thus, a *prima facie* case of lack of enablement cannot be established, and respectfully urge the withdrawal of the enablement rejection.

Further, the Office Action, page 3 item number 4, only provides a vague statement informing the rejection by stating "[t]he Examiner note [sic] that some pending claims of this application has [sic] a product by process claim."

Applicants submit that the lack of adequate reasoning put forth by the Office Action for the rejection of 'some pending claims' contravenes 35 U.S.C. § 132, which requires the Director to "notify the applicant thereof, stating the reasons for such rejection." This section is violated if the rejection "is so uninformative that it prevents the applicant from recognizing and seeking to counter the grounds for rejection." *Chester v. Miller*, 15 USPQ2d 1333 (Fed. Cir. 1990). This policy is captured in the Manual of Patent Examining Procedure. For example, MPEP § 706 states that "[t]he goal of examination is to clearly articulate any rejection early in the prosecution process so that applicant has the opportunity to provide evidence of patentability and otherwise respond completely at the earliest opportunity." Furthermore, MPEP § 706.02(j) indicates that: "[i]t is important for an examiner to properly communicate the basis for a rejection so that the issues can be identified early and the applicant can be given fair opportunity to respond."

Unfortunately, in this case, the Examiner's only discussion about case laws and decisions without referring to relevant claims (merely stating "some pending claims" page 3) are vague references to a seemingly irrelevant passage. By not addressing factual evidences, Applicants are left to rely on conjecture for the Office Action's reasoning.

Rejections Under 35 U.S.C. § 112, second paragraph

Claims 3, 4, 25-31 stand rejected under 35 U.S.C. § 112, second paragraph as being indefinite. Applicants respectfully traverse this rejection for at least the following reasons.

In view of the amendments to claims 27 and 28, these claims have been amended to delete problematic passages, the rejection of claims 27 and 28 under 35 U.S.C. § 112, second paragraph, is believed to be overcome.

With respect to the indefiniteness rejection over the claims 3, 4, 25-26, 29-31, Applicants note that the claimed feature of "further comprising" indeed requires no antecedent basis. Thus, for example, claim 4 is a proper dependent claim– "further comprising: P-type and N-type ohmic metal layers . . . ." The other claims 25-26 and 29-31 are clear and do not render the claims vague and indefinite. A new element can be preceded by a transitional phrase "further comprising." MPEP 2173.02 states that "[e]xaminers are encouraged to suggest claim language to applicants to improve the clarity or precision of the language used, but should not reject claims or insist on their own preferences if other modes of expression selected by applicants satisfy the statutory requirement." Applicants traverse this rejection as there is no reasonable basis for making the rejection.

Accordingly, withdrawal of the rejection of claims 3, 4, 25-31 under 35 U.S.C. § 112, second paragraph, is respectfully requested.

Rejection of Claims under Double Patenting

Claims 1-4 and 17-21 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of copending Application No. 12/568,630, U.S. Patent Application Publication No. 2010/0006870 applied for by Lee, *et al.* ("Lee").

Applicants respectfully traverse this rejection for at least the following reasons.

Clearly, the claims of the '630 copending Application do not mention to "N-type semiconductor layer and a P-type semiconductor layer formed on a portion of the N-type

semiconductor layer on a substrate," much less "wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other." Further, the claim 2 through 4 further distinguish over the claims of the '630 Application.

The Examiner fails to show why the subject matter of each of instant claims 1-4 over claims 1-14 of copending Application ('630) would have been obvious. The Examiner's rationale for the obviousness-type double patenting rejection, as it appears in the Office Action, on page 6, reads, *in toto,* as follows: "[a]lthough the conflicting claims are not identical, they are not patentably distinct from each other," which is not correct because there is no requirement of "first insulation layer" and "second insulation layer" not to mention "an electrically conductive material disposed on the first insulation layer to couple two of the light emitting cells; and a second insulation layer disposed on the electrically conductive material, wherein the second insulation layer corresponds to a contour of each light emitting cell" in the instant invention. (Emphasis added.) This is clearly different from instant claims 1 and 17, which do not require this feature. For at least these reasons, the claims of the present application are patentability distinct over claim 1-14 of the copending Application No. 12/568,630. The Examiner has failed to present a *prima facie* case regarding the obviousness of the instant claimed subject matter.

MPEP 804 further supports the argument that the examiner did not establish a *prima facie* case.

> Since the analysis employed in an obviousness-type double patenting determination parallels the guidelines for a 35 U.S.C. 103(a) rejection, the factual inquiries set forth in *Graham v. John Deere Co.,* 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103 are employed when making an obvious-type double patenting analysis. These factual inquiries are summarized as follows:

> (A) Determine the scope and content of a patent claim relative to a claim in the application at issue;
>
> (B) Determine the differences between the scope and content of the patent claim as determined in (A) and the claim in the application at issue;
>
> (C) Determine the level of ordinary skill in the pertinent art; and
>
> (D) Evaluate any objective indicia of nonobviousness.
>
> The conclusion of obviousness-type double patenting is made in light of these factual determinations.
>
> Any obviousness-type double patenting rejection should make clear:
>
> (A) The differences between the inventions defined by the conflicting claims - a claim in the patent compared to a claim in the application; and
>
> (B) The reasons why a person of ordinary skill in the art would conclude that the invention defined in the claim at issue >is anticipated by, or< would have been an obvious variation of >,< the invention defined in a claim in the patent.

Applicants, therefore, respectfully submit that the imposed provisional rejection of claims 1 through 4 and 17 through 21 on the ground of double patenting of the obviousness type over claims 1 through 14 of the '630 Application is not legally viable and, hence, solicits withdrawal thereof.

Rejections Under 35 U.S.C. §§ 102 and 103

Claims 1-2, 4 and 17-23 stand rejected under 35 U.S.C. § 102(e) as being allegedly anticipated by U.S. Patent No. 7,535,028 issued to Fan, *et al.* ("Fan"). Claims 3 and 25-31 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Fan.

Applicants wish to point out an apparent omission in the Office Action on page 9 regarding to citing references at item 13. However, this statement is inconsistent with the subsequent paragraph, page 10, which states, "see US patent 6,608,330 by Yamada fig 1 layer 112" and "see US patent 5,652,434 and US 5,862,167 fig 5 layer 50." Also, claim 24 seems inadvertently being omitted at item 13 but appear in body of the rejection on page 10. Therefore, Applicants' present response assumes the rejections over claims 3, 24-31 are based on the combination of Fan *et al.,* Yamada, Nakamura *et al.* and Sassa *et al.*

Applicants respectfully traverse the rejections under 35 U.S.C §§ 102 and 103 as the applied art, Fan *et al.* Yamada, Nakamura *et al.* and Sassa *et al.* applied individually or in combination, fails to anticipate or make obvious the many features of the pending claims, particularly as amended.

In the interest of advancing prosecution, Applicants have amended independent claims 1 and 17. As amended, claim 1 recites "wherein a transparent electrode layer is disposed on the P-type semiconductor layer to dissipate heat away from the P-type semiconductor layer." Amended claim 17 recites "wherein a transparent electrode layer is disposed on the second semiconductor layer to dissipate heat away from the second semiconductor layer."

The Office Action appears to acquiesce in the fact that Fen et al. does not teach the above features and rejects claim 3 as being obvious based on Fen et al. in view of Yamada (U.S. Patent No. 6,608,330), rather than as being anticipated by Fen et al. (Office Action on Page 10)

Applicants respectfully submit that the recitations in amended independent claims 1 and 17 are not disclosed in Yamada since the above amended features define a functional feature i.e., "to dissipate heat" that provides advantages (e.g., heat dissipation by distributing current via "transparent electrode layer," which is notably distinct form that taught in Yamada which focuses on facilitating bonding of p-electrode pad 113) over the conventional structure including layer

112 disclosed in FIG. 1 of Yamada. It is noted that paragraph [0082] of Applicants' substitute Specification describes the capabilities of the "transparent electrode layer," recites here "[f]urther in order **to reduce the resistance** of the P-type semiconductor layer 40 and **enhance the transmittance of light**, a transparent electrode layer 85 may be further formed on a top surface of the P-type semiconductor layer." (Emphasis added) Applicants would like to point out that the present invention, as described in the Specification (e.g., [0002], [0005] through [0007]) concerns "enhanced luminous efficiency" and "brightness" accessing applications to improve luminous efficiency of light emitting device while solving heat dissipation problem in the same manner, thus, the invention is required to address somewhat incompatible factors.

Specifically, at paragraphs, for example, [0069], [0082], [0138] in explaining the present invention and improvement over the prior art, it is revealed that the invention is an approach for providing "to enhance the heat dissipation characteristic of a light emitting deice, after a rear surface of the substrate 10 has been removed at a predetermined thickness, Al, Ti, Ag, W, Ni, Ta, Ru or an alloy thereof may be deposited on the rear surface of the substrate 10." [0069] Paragraph [0138] also states "[t]he transparent electrode layers 65 transmit light produced in the active layer 57, and disperse and supply currents to the upper semiconductor layers 59.

In contradistinction to the above combined structure (*viz.*, transparent electrode layer + Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof disposed on a rear surface of the substrate) to enhance luminous efficiency and the heat problem, Yamada structure merely controls an efficiency of luminance and temperature by first and second well layers and some of relevant passages are introduced as follows:

> Col. 5: 20-26
> As it is clearly understood by the persons skilled in the art that such degree of asperity of the **first and second well layers** can be adjusted by controlling the growth condition such as the growth speed and the growth temperature. The degree of asperity may be controlled by any other growth condition than the above-mentioned.

Col. 11: 37-51
A forward current of 20 mA is applied to the LED lamp (Vf=3.5V), then white light with spectrum which has a coordinate in the CIE chromaticity diagram as (X, Y)=(0.333, 0.314) as shown in FIG. 3 and its color temperature of 6000K. Light emitted by the **first and second well layers** are observed to have principal wavelength of about 470 nm and about 575 nm, respectively. The spectrum distribution of light emitted by the **second well layer** 109 has broader half-width than that by the **first well layer** 108, which contributes the lamp in improving the color rendering property. It is noted that more than two kinds of **well layers** (the first and second well layers) that emit different wavelength light can be also utilized so that the spectrum of the LED lamp is much broader to further improve the color rendering property.

Col. 11, line 65 – Col. 12, line 16
An another light emitting device 200 of this Example 2 is formed as the same way of Example 1 except that an another **first well layer** is added, that is, the device 200 has four first well layers instead of three. Such formed light emitting device 200 emits light having the color temperature higher than that of the device of Example 1 and bluish white color. Similarly an another light emitting device is formed as the same way of Example 1 except two another **first well layers** are added, that is, the device has five first well layers. Such formed light emitting device emits light having more bluish white color. FIG. 3 shows the coordinates in the CIE chromaticity diagram of light emitted by the light emitting device 100 (including **three first well layers** and **one second well layer**) of Example 1, and by the light emitting device 200 (including **four first well layers and one second well layer**) of Example 2. Thus the ratio of the growth numbers of the **first and second well layers** can be adjusted to obtain the mixed light having the desired coordinate in the CIE chromaticity diagram and the color temperature.

Col. 13: 40-53
When the growth temperature is a little increased and the **second well layer** 108 is formed, the **second well layer** 109 is obtained such that its degree R of asperity is 0.2. In other words, an another light emitting device of this Example 6 is formed as the same way of Example 1 except that the **second well layer** 109 is formed such

> that its degree R of asperity is 0.2. The light emitting device of Example 6 has a luminous ratio of the blue light emitted by the **first well layer** 108 over the yellow light emitted by the **second well layer** 109, which is a little greater than that of Example 1. And the luminous efficiency of the light emitting device 100 is almost same as one of Example 1.

Thus, it is clear that, unlike the prior art (Yamada) luminance and heat control schemes related to "first and second well layers," the claimed invention is directed to control enhanced luminous efficiency and brightness with "a transparent electrode layer disposed on the P-type semiconductor layer **to dissipate heat away** from the P-type semiconductor layer," and "Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof disposed on a rear surface of the substrate on which the light emitting cell is formed to **enhance the heat dissipation**," which are positively recited in amended claims 1, 17, 31 and new claim 32."

Office Action, page 11, introduces Sassa et al. (U.S. Patent No. 5,862,167) for a supposed teaching of "Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof disposed on a rear surface of the substrate" – particularly FIG. 5, metal reflecting layer 50. Applicants submit that the cited layer 50 bears no relevance to claimed features i.e., "to enhance the heat dissipation." The following related passages with respect to the metal reflecting layer 50 reinforces Applicant's position: "[s]ince the sapphire substrate 1 is transparent to the light emitted from the LED 500, the light reflected by the metal reflecting layer 50 beneath the **sapphire substrate 1 is transmitted to the emission plane with little attenuation** when the light passes through the sapphire substrate 1." (Col. 5: 16-24) This passage would suggest to one of ordinary skill in the art that the metal reflecting layer 50 acts facilitating transmission of LED light reflecting by the layer 50. Hence, there is no technical support from Sassa *et al.* to teach or suggest "to enhance the heat dissipation."

Accordingly, the above mentioned paragraphs [0069], [0082], [0138] of the Specification

demonstrate the advantages and distinctive structural characteristics of Applicant's light emitting device associated with heat dissipation including claimed "transparent electrode layer" along with "Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof disposed on a rear surface of the substrate," thereby, the nonobviousness of Applicants' light emitting device of claims 1, 17, 31, and 32. *See, e.g.*, *In re Thorpe*, 777 F.2d 695, 697-98 (Fed. Cir. 1985); *In re Garnero*, 412 F.2d at 279.

With respect to amended dependent features of claims 30 and newly added claim 33 for proper dependency of claim 1, the cited insulation layer- FIG. 2, element 34 (page 11) of Fan *et al.* fails to teach or suggest the amended features recite "insulation layer is disposed continuously to cover a surface of the substrate, a top and the inclined surface of the light emitting cell and the electrical conductor." Thus, any purported combination of Fan *et al*. with Yamada, Nakamura et al. or Sassa *et al*. would fail to teach. Not surprisingly, the only insulated portion of Fan et al. by insulation layer 34 is covered from the semiconductor sidewalls 32 to the metal wire 36, which clearly shows that the insulation layer 34 Fan *et al*. (Fig. 2) does not cover "a surface of the substrate, a top and the inclined surface of the light emitting cell" not to mention "continuously cover."

Moreover, even if the transparent electrode disclosed by Yamada were capable of being modified as suggested by the Examiner, the reference would still fail to teach the presently claimed invention, specifically as amended. Consequently, a *prima facie* case of obviousness has not been established. *See, e.g.*, *Uniroyal, Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044 (Fed. Cir. 1988). Applicants, therefore, respectfully request the withdrawal of the 35 U.S.C. § 103(a) rejections to claims 24-31.

Based on the foregoing arguments, and given that anticipation under 35 U.S.C. § 102 requires the **identical** disclosure in a single reference of **each element** of a claimed invention, such that the **identically claimed invention** is placed into the recognized possession of one having ordinary skill in the art, it is clear that Fan et al. does not anticipate the claims 1-2, 4, 17-

23. *See, e.g.*, *Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368-69 (Fed. Cir. 2003); *Crown Operations Int'l, Ltd. v. Solutia Inc.*, 289 F.3d 1367, 1375 (Fed. Cir. 2002).

Turning now to new claims 34 and 35, dependent claims 34 and 35 are drawn to material for "transparent electrode layer" to support current spreading recites "transparent electrode layer is selected from ITO (Indium Tin Oxide), ZnO (Zinc Oxide) or a conductive transparent metal." This feature is captured from Specification [0082] and Applicants respectfully submit that none the references taken alone, or in combination, teaches or suggests recited material.

Based on the foregoing Applicants submit that the imposed rejections under 35 U.S.C. § 102 as being anticipated by Fan *et al.* and under 35 U.S.C. § 103(a) for obviousness predicated upon Fan et al. in view of Yamada and Nakamura et al. and further in view of Sassa *et al*. is not factually or legally viable, and hence, solicit withdrawal thereof.

CONCLUSION

A full and complete response has been made to the pending Office Action, and all of the stated objections and grounds for rejection have been overcome or rendered moot. Accordingly, all pending claims are allowable, and the application is in condition for allowance.

The Examiner is invited to contact Applicants' undersigned representative at the number below if it would expedite prosecution. Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully submitted,

/hae-chan park/

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Date: April 12, 2010

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Electronic Patent Application Fee Transmittal

Application Number:	11993965
Filing Date:	26-Dec-2007
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Filer:	Hae-Chan Park/ethan song
Attorney Docket Number:	P2317US00

Filed as Large Entity

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Claims in excess of 20	1615	2	52	104
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**104**

Electronic Acknowledgement Receipt

EFS ID:	7393306
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
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Receipt Date:	12-APR-2010
Filing Date:	26-DEC-2007
Time Stamp:	14:22:51
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$104
RAM confirmation Number	573
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1		P2317US00_Reply.pdf	122308 fbca5c8039567a51e1674a279f4b6bc1341bee3f	yes	22

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Specification	2	3
	Claims	4	8
	Applicant Arguments/Remarks Made in an Amendment	9	22

Warnings:

Information:

2	Fee Worksheet (PTO-875)	fee-info.pdf	29741 feea800001775ecf568bede74366806d203ddfd3	no	2

Warnings:

Information:

Total Files Size (in bytes):	152049

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<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/993,965	12/26/2007	Jong Lam Lee	P2317US00	2191

58027 7590 06/29/2010

H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

EXAMINER	
NGUYEN, THINH T	

ART UNIT	PAPER NUMBER
2818	

NOTIFICATION DATE	DELIVERY MODE
06/29/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATENT@PARK-LAW.COM

Office Action Summary	Application No.	Applicant(s)	
	11/993,965	LEE ET AL.	
	Examiner	Art Unit	
	THINH T. NGUYEN	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4 and 17-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,17- 35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/24/10,3/1/10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED OFFICE ACTION

1. Claims 1-2, 4, 17-35 are pending in the Application.

2. The Examiner note that some pending claims of this Application has a product by process limitation. Please note that in a product-by-process claim, it is the patentability of the claimed product and not of the recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. The Patent Office is not equipped to manufacture products by a myriad of processes put before it and then obtain prior art product and make physical comparisons therewith. In re Brown, 173 USPQ 685 (CCPA 1972). Also, a product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ I S at 17 (footnote 3). See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al., 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a " product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In

re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear.

3. The Examiner also note that some pending claims has the intended use of a structure for example claim 1 recites -- " **to dissipate heat away from** the P-type semiconductor"-- . Please note that it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus (explicitly disclosed or not) satisfying the claimed structural limitations. *Ex Parte Masham*, 2 USPQ F.2d 1647 (1987).

Claim Rejections - 35 USC § 103

4. The following is a quotation of U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 4, 17-29, 31-32,34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fan et al. (U.S. Patent 7,535,028.) thereafter Fan 028 in view of Yamada (US patent 6,608,330) thereafter Yamada 330

With regard to claim 1, Fan 028 discloses (fig 1, fig 2,fig 3) a light emitting device, comprising: a plurality of light emitting cells each including an N-type semiconductor layer and a P-type semiconductor layer (elements 20,16,fig 2, ,column 3 lines 24,50) formed on a portion of the N-type semiconductor layer on a substrate (fig 2 ,element 12) , wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, (fig 2,fig 3) and a side surface including the N-type or P-type semiconductor layer of the light emitting cell has a slope of approximately 20 degree approximately 80 degree from a horizontal plane (column 4 lines 5-20).based on the substrate and an electrode layer (fig 1 element # 22 or no name element on top of layer #20 in fig 2) is disposed on the P-type semiconductor layer (fig 1,fig 2 element # 20) to dissipate heat away from the P-type semiconductor layer. Note that because Fan 028 can be a stack of metal layer formed by depositing different metal on each other and anneal them (Nickel or gold or Titanium or Aluminum , see Fan 028 disclosure column 3 lines 39-50) Fan 028 disclosed electrode structure inherently dissipate heat away from the p-type semiconductor type

Not Specific in Fan 028 is the limitation that this electrode layer is transparent, this limitation, however, is considered obvious because Yamada 330 in his invention of a light emitting device discloses that the p electrode (fig 1 element #112) disposed on a p-semiconductor layer (fig 1 element # 111) made with the same metal of the Fan 028 invention (

Nickel and gold, Yamada 330 column 40-55) can be transparent (Yamada 330 column 10 lines 40-55)

It would have been obvious to one of ordinary skill in the art the time the invention was made to incorporate this features, as taught by Yamada 330 into the Fan 028 device and come up with the invention of claim 1.

The rationale is as the following:

A person skilled in the art at the time the invention was made would have been motivated to have this feature in order to provide the Fan 028 device with more option (i.e. transmit light in the vertical direction for example) and make it a commercial success.

Moreover, please note that the transparent limitation is considered obvious because it has been held that

The selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll co V. Interchemical Corp., 325 U.S. 327, 85 USPQ 297 (1945)

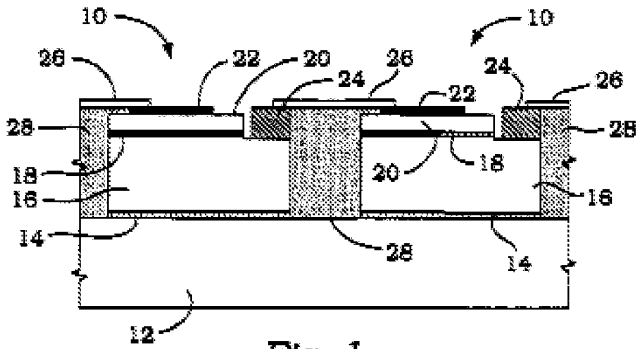


Fig. 1

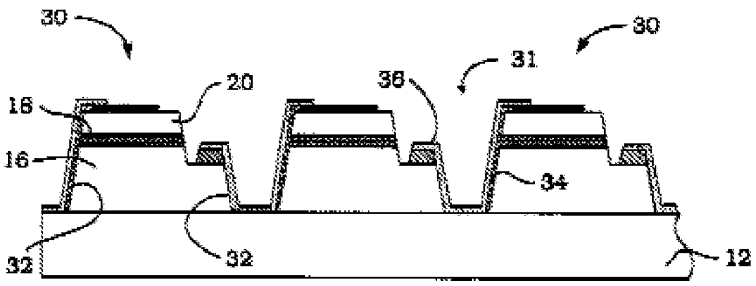


Fig. 2

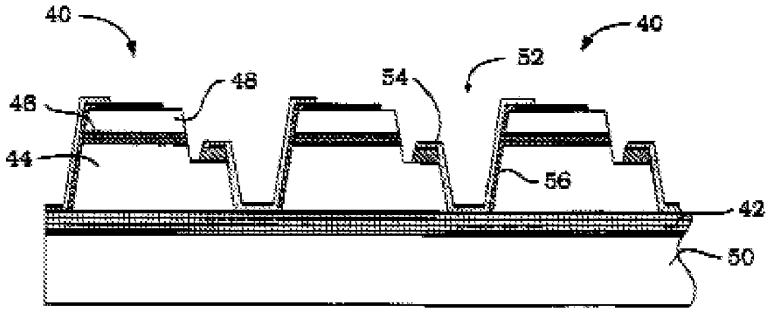
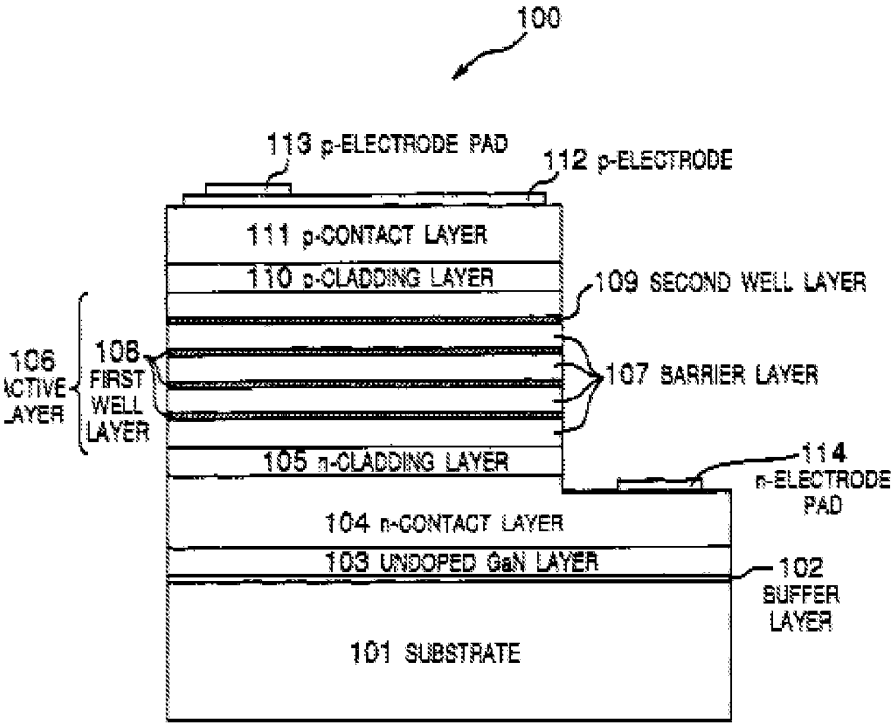


Fig. 3

FAN 028 DISCLOSURES.

Fig.1



YAMADA 330 DISCLOSURES

With regard to claim 2, Fan 028 discloses (fig 1, fig 2,fig 3) a light emitting device, comprising a wire to couple the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

With regard to claim 4, Fan 028 discloses (fig 2, fig 2,fig 3) a light emitting device, , further comprising P-type and N-type ohmic metal layers Cr or Au on the P-type and N-type semiconductor layers, respectively. (column 3 lines 35-50)

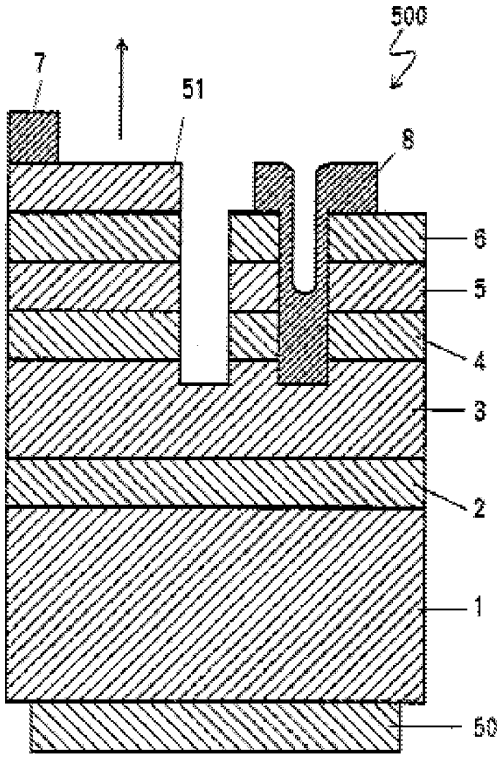
With regard to claim 17-23 , the combined Fan 028 in view of Yamada 330 disclosure will disclose (fig 2,fig 3 of Fan 028) a light emitting device comprising: a substrate; and a plurality of light emitting cells disposed on the substrate being spaced apart from each other, wherein the light emitting cell comprises a first-type semiconductor layer and a second-type semiconductor layer, (column 3 lines 24-50) at least one of the light emitting cells has at least one side surface that is not perpendicular to a horizontal plane based on the substrate , and the first-type semiconductor layer of at least one of the light emitting cells is electrically connected to the second-type semiconductor layer of an adjacent another light emitting cell.(column 4 lines 6-34); wherein a transparent electrode layer is disposed on the second semiconductor layer to dissipate heat away from the second semiconductor layer or wherein at least one side surface has an inclination angle with respect to the horizontal plane or wherein the inclination angle is approximately 20° to approximately 80° with respect to the horizontal plane (Fan 028 column 4 lines 5-20) ;or .wherein the inclined surface of the light emitting cell comprises at least a side surface of the first- semiconductor layer ; or wherein the first-type semiconductor layer is an N-type semiconductor layer ; or wherein the inclined surface of the light emitting cell is formed continuously up to the second-type semiconductor layer ; or wherein the second-type semiconductor layer is a P- semiconductor layer

With regard to claim 24, Fan discloses an embodiment (fig 1) , wherein the second semiconductor layer of the light emitting cell comprises at least one surface not being inclined

With regard to claim 25, Yamada discloses a bonding pad on each of the p-side and n-side electrode

With regard to claim 31,32 as set forth in the rejection of claim 20 and 1,, the combined Fan 028 in view of Yamada device discloses all the invention except for AI, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof disposed on a rear surface of the substrate on which the light emitting cell is formed to enhance heat dissipation . this limitation , however, is considered obvious because the use of a metal layer to reflect light to increase the light output efficiency of an LED device is known in the art at the time the invention was made (see US 5,862,167 fig 5 layer 50).

FIG. 5



With regard to claims 34, 35 these claims are obvious over the disclosures of Fan 028 in view of Yamada 330 for the following rationale

The selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll co V. Interchemical Corp., 325 U.S. 327, 85 USPQ 297 (1945)

With regard to claim 26,27 the combined Fan 028 in view of Yamada 330 disclosure will disclose (fig 2,fig 3 of Fan 028) a light emitting device wherein the first bonding pad is disposed on the first semiconductor layer of one of the light emitting cells to couple the second bonding pad disposed on the second semiconductor layer of the another adjacent light emitting cell or connection between the light emitting cells are provided using the bonding pads (Fan 028 fig 2,fig 3, Yamada Fig 1)

With regard to claim 28, Yamada 330 discloses the use of bond pads (note that for claim 28 the product by process limitations are not considered because of the rationale set forth in paragraph 2 of this office Action.

With regard to claim 29, Fan 028 discloses a light emitting device (fig 2,fig 3, element # 36) wherein the-connection is provided by an electrical conductor disposed on the inclined surface of the light emitting cell.

6. Claims 30,33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fan et al. (U.S. Patent 7,535,028.) thereafter Fan 028 in view of Yamada (US patent 6,608,330) thereafter Yamada 330 in further view of Jiang et al. (US patent 7,213,942) thereafter Jiang 942

With regard to claim 30,33 , as set forth in the rejection of claim 29 and claim 1, the combined Fan 028 in view of Yamada 330 device discloses all the invention except for the

limitation wherein an insulation layer is disposed to continuously cover a surface of the substrate, between a top and the inclined surface of the light emitting cell and the electrical conductor or wherein an insulation layer is disposed continuously to cover a surface of the substrate, a top and the inclined surface of the light emitting cells.

Jiang 028, however, discloses a light emitting device array wherein an insulation layer is disposed to continuously cover a surface of the substrate, between a top and the inclined surface of the light emitting cell and the electrical conductor or wherein an insulation layer is disposed continuously to cover a surface of the substrate, a top and the inclined surface of the light emitting cells.(Jiang 942 fig 4 element # 54, column 5 lines 4-22)

It would have been obvious to one of ordinary skill in the art the time the invention was made to incorporate this features, as taught by Jiang 942 into the combined Fan 028 in view of Yamada 330 device and come up with the invention of claim 30,33

The rationale is as the following:

A person skilled in the art at the time the invention was made would have been motivated to have this feature in order to provide the Fan 028 in view Yamada 330 device with extra protection in order to increase its reliability

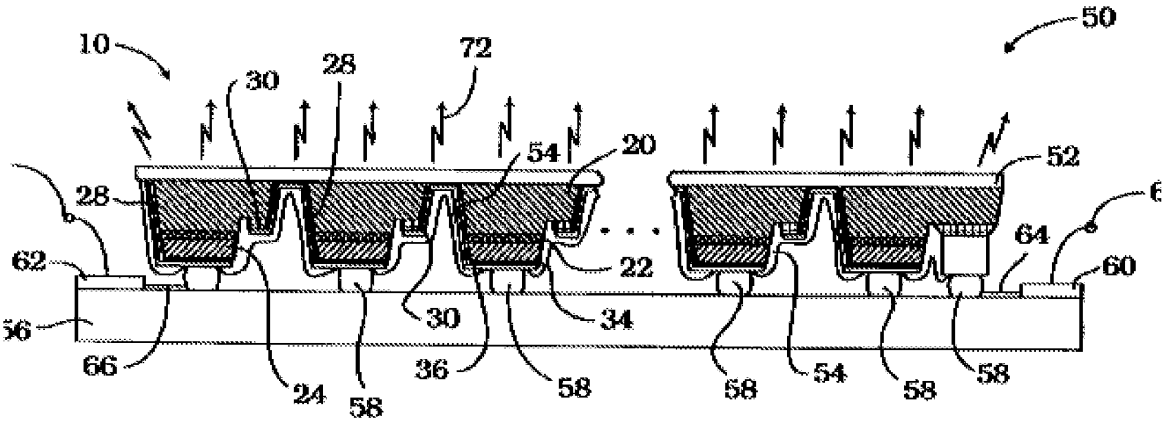


Fig. 4

JIANG 942 DISCLOSURES

CONCLUSION

7. THIS ACTION IS MADE FINAL. Applicant's amendments necessitated new grounds of rejection of the claims and therefore this Action is made Final (See MPEP § 706.07(a)) . Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on 9:30 am - 6:30 pm Monday to Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, STEVEN LOKE can be reached on 571-272-1657. The fax phone numbers for the organization where this application or proceeding is assigned is 571-273-8300

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thinh T Nguyen/

Primary Examiner

Art Unit 2818

Notice of References Cited	Application/Control No. 11/993,965	Applicant(s)/Patent Under Reexamination LEE ET AL.	
	Examiner THINH T. NGUYEN	Art Unit 2818	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,535,028	05-2009	Fan et al.	257/88
*	B	US-6,608,330	08-2003	Yamada, Motokazu	257/90
*	C	US-7,213,942	05-2007	Jiang et al.	362/231
*	D	US-5,862,167	01-1999	Sassa et al.	372/45.01
	E	US-			
	F	US-			
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	H	US-			
	I	US-			
	J	US-			
	K	US-			
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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
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*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11993965	LEE ET AL.
	Examiner	Art Unit
	THINH T NGUYEN	2818

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/06/2009	10/30/2009	01/30/2010	06/21/2010					
	1	÷	÷	✓	✓					
	2	÷	÷	✓	✓					
	3	÷	÷	✓	-					
	4	÷	÷	✓	✓					
	5	÷	÷	-	-					
	6	÷	÷	-	-					
	7	÷	N	-	-					
	8	÷	N	-	-					
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	31			✓	✓					
	32				✓					
	33				✓					
	34				✓					
	35				✓					

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11993965	LEE ET AL.
	Examiner	Art Unit
	THINH T NGUYEN	2818

SEARCHED			
Class	Subclass	Date	Examiner
257	100, 266	9/16/09	ttn

SEARCH NOTES		
Search Notes	Date	Examiner
east	9/16/09	ttn
east	1/30/10	TTN
east	6/20/10	TTN

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, Thinh T.
	Attorney Docket Number	P2317US00

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7504772		2009-03-17	Yukimoto et al.	
	2	5940683		1999-08-17	Holm et al.	
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	1	20030010989		2003-01-16	Yukimoto	
	2	20020109147		2002-08-15	Shirai et al.	
	3	20070114542		2007-05-24	Yamazaki et al.	
	4	20050121679		2005-06-09	Nagahama et al.	

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /T.N./

Receipt date: 02/24/2010	Application Number	11993965 11993965 - GAU: 2818
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, Thinh T.
	Attorney Docket Number	P2317US00

	5	20050082966		2005-04-21	Yamazaki et al.	
	6	20050254243		2005-11-17	Jiang et al.	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2004-311677	JP		2004-11-04	Matsushita Electric Works Ltd.		☐
	2	2005-142278	JP		2005-06-02	Sharp Corp.		☐
	3	2005-117020	JP		2005-04-28	Stanley Electric Co., Ltd.		☐
	4	2003-017740	JP		2003-01-17	Lumileds Lighting US LLC		☐
	5	2001-185755	JP		2001-07-06	Rohm Co., Ltd.		☐
	6	07-153993	JP		1995-06-16	Daido Steel Co., Ltd.		☐
	7	06-244458	JP		1994-09-02	Nichia Chem Ind Ltd.		☐

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Receipt date: 02/24/2010	Application Number	11993965 11993965 - GAU: 2818
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, Thinh T.
	Attorney Docket Number	P2317US00

NON-PATENT LITERATURE DOCUMENTS Remove			
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Office Action dated February 1, 2010 for co-pending application no. 12/568,630	☐

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EXAMINER SIGNATURE			
Examiner Signature	/Thinh Nguyen/	Date Considered	06/20/2010

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	7973	(AC alternating near2 current) with lighting	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/21 15:20
L2	415049	Light adj emitting adj (diode device element)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/21 15:21
L3	1717	1 and 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/21 15:29
L4	103130	passivation	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/21 15:29
L5	16	3 and 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/21 15:29
L6	3	"7683377"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/21 15:49
L7	14	"7213942"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/21 17:31
L8	57	"5862167"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/21 18:27

EAST Search History (Interference)

<This search history is empty>

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (07-09)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(**Not for submission under 37 CFR 1.99)**

Application Number	11993965
Filing Date	2007-12-26
First Named Inventor	Jong Lam LEE
Art Unit	2818
Examiner Name	NGUYEN, Thinh T
Attorney Docket Number	P2317US00

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5252434		1993-10-12	Blonder	

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U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050023537		2005-02-03	Salam	

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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2005008791	WO		2005-01-27	Matsushita Electric Industrial Co., Ltd.		☐
	2	1469529	EP		2004-10-20	Lumileds Lighting US, LLC		☐
	3	2004006582	JP		2004-01-08	Nitride Semiconductor Co Ltd		☐

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Receipt date: 03/01/2010	Application Number	11993965 11993965 - GAU: 2818
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, Thinh T
	Attorney Docket Number	P2317US00

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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	European Search Report issued February 10, 2010 by the European Patent Office in European Patent Application No. 06769008.1	☐

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EXAMINER SIGNATURE

Examiner Signature	/Thinh Nguyen/	Date Considered	06/20/2010

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
GROUP ART UNIT 2818

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	Docket No.: P2317US00
Jong Lam LEE, *et. al.*	
Serial No.: 11/993,965	Group Art Unit: 2818
Confirmation No.: 2191	
Filed: December 26, 2007	Examiner: NGUYEN, Thinh T.

For: **LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME**

Mail Stop: AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY AND AMENDMENT UNDER 37 C.F.R. § 1.116

Sir:

In response to the Final Office Action dated June 29, 2010 ("Office Action"), Applicants respectfully request reconsideration of the application in view of the following Amendments and Remarks.

Amendments to the Claims begin on page 2.

Remarks begin on page 7.

Applicants believe that no extensions of time are required at this time. If extensions of time are necessary to prevent abandonment of this application, then they are hereby petitioned for under 37 C.F.R. § 1.136(a). Applicants believe that no further fees for net addition of claims are required at this time. Any fees required for further extensions of time and any fees for the net addition of claims are hereby authorized to be charged to our Deposit Account No. 50-3698.

AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 1, 17, 31 and 32 as shown below.

This claim list replaces all prior claim lists in the application.

1. (Currently Amended) A light emitting device, comprising:

a plurality of light emitting cells each comprising an N-type semiconductor layer and a P-type semiconductor layer formed on a portion of the N-type semiconductor layer on a substrate, wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface comprising the N-type or P-type semiconductor layer of the light emitting cell has a slope of approximately 20° to approximately 80° from a horizontal plane based on the substrate, wherein a P-type electrode and a N-type electrode are disposed on the respective P-type semiconductor layer and the N-type semiconductor layer and a transparent ~~electrode~~ layer is disposed on the P-type semiconductor layer to dissipate heat away from the P-type semiconductor layer, and wherein an ohmic layer is disposed on the transparent layer or the N-type semiconductor layer, respectively.

2. (Previously Presented) The light emitting device as claimed in claim 1, further comprising:

a wire to couple the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

3. (Canceled)

4. (Previously Presented) The light emitting device as claimed in claim 1, further comprising:

P-type and N-type ohmic metal layers comprising Cr or Au on the P-type and N-type semiconductor layers, respectively.

5-16. (Canceled)

17. (Currently Amended) A light emitting device comprising:

a substrate; and

a plurality of light emitting cells disposed on the substrate being spaced apart from each other,

wherein the light emitting cell comprises a first semiconductor layer and a second semiconductor layer,

at least one of the light emitting cells has at least one side surface that is not perpendicular to a horizontal plane based on the substrate, and

the first semiconductor layer of at least one of the light emitting cells is coupled to the second semiconductor layer of an another adjacent light emitting cell, wherein an electrode of the first semiconductor and an electrode of the second semiconductor are disposed on the respective first semiconductor and the second semiconductor and a transparent ~~electrode~~ layer is disposed on the second semiconductor layer to dissipate heat away from the second semiconductor layer, and wherein an ohmic layer is disposed on the transparent layer or the first semiconductor.

18. (Previously Presented) The light emitting device as claimed in claim 17, wherein the at least one side surface has an inclination angle with respect to the horizontal plane.

19. (Previously Presented) The light emitting device as claimed in claim 18, wherein the

inclination angle is approximately 20˚ to approximately 80˚ with respect to the horizontal plane.

20. (Previously Presented) The light emitting device as claimed in claim 18, wherein the inclined surface of the light emitting cell comprises at least a side surface of the first semiconductor layer.

21. (Previously Presented) The light emitting device as claimed in claim 20, wherein the first semiconductor layer is an N semiconductor layer.

22. (Previously Presented) The light emitting device as claimed in claim 20, wherein the inclined surface of the light emitting cell is formed continuously up to the second semiconductor layer.

23. (Previously Presented) The light emitting device as claimed in claim 22, wherein the second semiconductor layer is a P semiconductor layer.

24. (Previously Presented) The light emitting device as claimed in claim 22, wherein the second semiconductor layer of the light emitting cell comprises at least one surface not being inclined.

25. (Previously Presented) The light emitting device as claimed in claim 20, wherein at least one of the light emitting cells further comprises:

a first bonding pad and a second bonding pad disposed respectively on the first semiconductor layer and the second semiconductor layer.

26. (Previously Presented) The light emitting device as claimed in claim 25, wherein the first bonding pad is disposed on the first semiconductor layer of one of the light emitting cells to couple the second bonding pad disposed on the second semiconductor layer of the another adjacent light emitting cell.

27. (Previously Presented) The light emitting device as claimed in claim 26, wherein connections between the light emitting cells are provided using the bonding pads.

28. (Previously Presented) The light emitting device as claimed in claim 27, wherein providing the bonding pads comprises utilizing at least one of plating method, chemical vapor deposition (CVD), physical vapor deposition (PVD), or electron beam deposition.

29. (Previously Presented) The light emitting device as claimed in claim 26, wherein the connection is provided by an electrical conductor disposed on the inclined surface of the light emitting cell.

30. (Previously Presented) The light emitting device as claimed in claim 29, wherein an insulation layer is disposed to continuously cover a surface of the substrate, a top and the inclined surface of the light emitting cell and the electrical conductor.

31. (Currently Amended) The light emitting device as claimed in claim ~~20~~ 17, ~~further comprising:~~

wherein a portion of the rear surface of the substrate is removed and Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof is disposed on [[a]] the rear surface of the substrate on which the light emitting cell is formed to enhance the heat dissipation.

32. (Currently Amended) The light emitting device as claimed claim 1, wherein the substrate comprises a front surface and a rear surface, wherein the light emitting cells are disposed on the front surface and a portion of the rear surface is removed and Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof is disposed on the rear surface to enhance the heat dissipation.

33. (Previously Presented) The light emitting device as claimed claim 1, wherein an

insulation layer is disposed continuously to cover a surface of the substrate, a top and the inclined surface of the light emitting cells.

34. (Previously Presented) The light emitting device as claimed in claim 1, wherein the transparent electrode layer is selected from ITO (Indium Tin Oxide), ZnO (Zinc Oxide) or a conductive transparent metal.

35. (Previously Presented) The light emitting device as claimed in claim 17, wherein the transparent electrode layer is selected from ITO (Indium Tin Oxide), ZnO (Zinc Oxide) or a conductive transparent metal.

REMARKS

Claims 1, 17, 31 and 32 have been amended.

Accordingly, claims 1, 2, 4 and 17-35 are currently pending in the application, of which claims 1 and 17 are independent.

Applicants respectfully submit that the above amendments do not add new matter to the application and are fully supported by the specification. Adequate descriptive support for the amendments is apparent throughout the originally filed disclosure, for example, paragraph [0054] and paragraph [0082] of substitute specification, and accompanying figures 13-17.

Entry of the Amendment is proper under 37 C.F.R. §1.116 because it does not raise new issues requiring further search and/or consideration by the Examiner because similar subject matter was previously considered by the Examiner and thus further consideration and/or search by the Examiner is not warranted. For at least these reasons, entry of the present Amendment is therefore respectfully requested. Accordingly, Applicants request reconsideration and timely withdrawal of the pending rejections for the reasons discussed below.

Rejections Under 35 U.S.C. § 103

Claims 1, 2, 4, 17-29, 31, 32, 34 and 35 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over U.S. Patent No. 7,535,028 issued to Fan, *et al.* ("Fan") in view of U.S. Patent No. 6,608,330 issued to Yamada ("Yamada"). Claims 30 and 33 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Fan in view of Yamada in further view of U.S. Patent No. 7,213,942 issued to Jiang, *et al.* ("Jiang") Applicants respectfully traverse this rejection for at least the following reasons.

Applicants have, in order to reduce issues for potential appeal, clarified the meaning and structural feature of "transparent layer," particularly with respect to claimed "P-type electrode" and 'p-electrode 112' of Yamada (FIG. 1) on which Examiner is relied to supposed teaching of

the "transparent layer." Also, Applicants incorporate the arguments previously advanced in the Reply dated April 12, 2010 in traversing the imposed rejections under 35 U.S.C. §§ 102 and 103 based on Fan and Yamada over the independent claims 1 and 17 noting the references neither discloses nor suggests not only claimed combined structure (*viz.*, transparent layer + a portion of the rear surface of the substrate is removed and Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof is disposed on the rear surface of the substrate) but claimed functional advantages attributed to the claimed novel layered structure— to enhance luminous efficiency and resolve a chronic heat problem.

Applicants respectfully submit that the Examiner misapplies decisions of *Ex Parte Masham*, 2 USPQ F.2d 1647 (1987) in an attempt to engaging in a factually erroneous interpretation of the facts of the cited case law by omitting key condition of the decision— "if the prior art apparatus teaches all the structural limitations of the claim," consequently, a misapplication of the case law. Namely, none of the references taken alone, or in combination teaches or suggests claimed features.

For example, claim 1, as amended, recites "wherein, **a P-type electrode and a N-type electrode** are disposed on the respective P-type semiconductor layer and the N-type semiconductor layer and **a transparent layer** is disposed on the **P-type semiconductor layer to dissipate heat** away from the P-type semiconductor layer, and wherein an **ohmic layer** is disposed **on the transparent layer or the N-type semiconductor layer, respectively**." Amended claim 17 recites "the first semiconductor layer of at least one of the light emitting cells is coupled to the second semiconductor layer of an another adjacent light emitting cell, wherein **an electrode** of the first semiconductor and **an electrode** of the second semiconductor are disposed on the respective first semiconductor and the second semiconductor and **a transparent layer** is disposed on the **the second semiconductor layer to dissipate heat** away from the second semiconductor layer, and wherein **an ohmic layer** is disposed **on the**

transparent layer or the first semiconductor."

By amending claims 1 and 17, Applicants have clarified structural differences between the claimed "transparent layer" and 'p-electrode 112' of Yamada. And this distinction is viable although the 'p-electrode 112' is a transparent electrode. (Office Action, page 5) Moreover, applied art does not teach or suggest "an **ohmic layer** is disposed **on the transparent layer or the N-type semiconductor layer, respectively**" and "**an ohmic layer** is disposed **on the transparent layer or the first semiconductor**," as positively recited in claims 1 and 17, respectively.

To the extent the Examiner is relying on the theory of inherency to cure the Examiner's reasoning (Office Action, page 4, states "Fan 028 disclosed electrode structure inherently dissipate heat away from the p-type semiconductor,") Applicants reminds the Examiner of the provisions of MPEP §2112, which states that the "fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result, or characteristic." *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993). Also, inherency may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. *In re Roberstson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). In the case at hand, the cited passages (column 3, lines 39-50) even do not touch heat problem, thus the Examiner cannot simply surmise that the layered structure of Fan can perform the features of the claims 1 and 17.

Given the novel structural features of claims 1 and 17 along with their dependent claims 31 and 32 (i.e., transparent layer + a portion of the rear surface of the substrate is removed and Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof is disposed on the rear surface of the substrate) the features that the Examiner states as to "dissipate heat away" from the reference are not the

features that the Examiner avers to be "inherently" disclosed from the Fan. Applicants contend that Fan even does not consider heat problem.

Therefore, Applicants respectfully submit that the Examiner has not established a *prima facie* case that Fan inherently describes "dissipate heat away" not to mention the art is devoid of claimed structural features.

Not surprisingly, in the statement of the rejections with respect to dependent claims 31 and 32, the Examiner (page 9) asserts that "this limitation [enhance heat dissipation], however, is considered obvious because the use of a metal layer to reflect light to increase the light output efficiently of an LED device is known in the art at the time the invention made." This rejection is traversed.

The fact remains Sassa (US 5,862,167, Office Action, page 9) never addresses nor teaches about "heat" other than "little attenuation," which means not gradual loss in intensity of light emitted from LED 500, therefore cannot be encompassed by features recited in the dependent claims 31 and 32 because "little attenuation" inevitably gains intensity of flux of light that is directly opposite teaching to the problem addressed by the claimed invention. Further, the deficiencies of Fan, Yamada and Sassa cannot be remedied by Examiner's mere conjecture, design choice, routine skill, or optimization, especially when the record does not support such conclusions. *See generally In re Zurko*, 258 F.3d 1379 (Fed. Cir. 2001).

> The metal reflecting layer 50 is useful. Since the sapphire substrate 1 is transparent to the light emitted from the LED 500, the light reflected by the **metal reflecting layer 50** beneath the **sapphire substrate 1** is transmitted to the emission plane with **little attenuation** when the light passes through the sapphire substrate 1. Further, the fabrication of the layer 50 is straight forward, because it is formed at the backside of the sapphire substrate 1. (Sassa, FIG. 5, item50 and accompanying passages, Office Action, page 9)

With respect to rejections over claims 30 and 33, the Office Action correctly

acknowledges the primary references (Fan and Yamada) do not disclose features of "wherein an insulation layer is disposed to continuously cover a surface of the substrate, a top and the inclined surface of the light emitting cell and the electrical conductor." Consequently, the Office Acton is forced to rely on Jiang for supposed teachings of the above features.

Even assuming the 'passivation layer 54' of Jiang were equated to claimed "insulation layer," and assuming the modifications proposed in the Office Action were justified by additional teachings or suggestions found in the references, even the combination does not render the claimed invention obvious. Specifically, according to the cited FIG. 4, item 54, and accompanying passages col. 5: 4-22, the 'passivation layer 54' cannot be interpreted "to **continuously cover** a surface of the substrate because of a cut portion due to a bonding bump 58 (suggested meaning of continuous is destroyed by the boding bump 58), thereby not supporting "continuously cover," let alone "insulation layer is disposed to continuously cover a surface of the substrate, a top and the inclined surface of the light emitting cell and the electrical conductor."

Accordingly, Applicants respectfully urge the indication that independent claims 1 and 17 and dependent claims 2, 4, and 18-36 are allowable.

To establish an obviousness rejection under 35 U.S.C. § 103(a), four factual inquiries must be examined. The four factual inquiries include (a) determining the scope and contents of the prior art; (b) ascertaining the differences between the prior art and the claims in issue; (c) resolving the level of ordinary skill in the pertinent art; and (d) evaluating evidence of secondary consideration. *Graham v. John Deere*, 383 U.S. 1, 17-18 (1966).

In view of these four factors, the analysis supporting a rejection under 35 U.S.C. 103(a) should be made explicit, and should "identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the [prior art] elements" in the manner claimed. *KSR Int'l. Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 82 USPQ2d 1385, 1396 (2007). The

Federal Circuit requires that "rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006).

Finally, even if the prior art may be combined, there must be a reasonable expectation of success, and the reference or references, when combined, must disclose or suggest every claimed feature. *See in re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

CONCLUSION

A full and complete response has been made to the pending Office Action, and all of the stated objections and grounds for rejection have been overcome or rendered moot. Accordingly, all pending claims are allowable, and the application is in condition for allowance.

The Examiner is invited to contact Applicants' undersigned representative at the number below if it would expedite prosecution. Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully submitted,

/hae-chan park/

Hae-Chan Park
Reg. No. 50,114

Date: August 3, 2010

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Electronic Acknowledgement Receipt

EFS ID:	8145197
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
Receipt Date:	03-AUG-2010
Filing Date:	26-DEC-2007
Time Stamp:	16:40:08
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P2317US00_Reply.pdf	73569 0acf6ebf0698c6909ac4d0bc869a3b3db1a62391	yes	13

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment After Final	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	13
Warnings:			
Information:			
	Total Files Size (in bytes):	73569	

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/993,965	12/26/2007	Jong Lam Lee	P2317US00	2191

58027 7590 08/16/2010

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EXAMINER	
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ART UNIT	PAPER NUMBER
2818	

NOTIFICATION DATE	DELIVERY MODE
08/16/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATENT@PARK-LAW.COM

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 11/993,965	**Applicant(s)** LEE ET AL.	
	Examiner THINH T. NGUYEN	**Art Unit** 2818	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 03 August 2010 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1,2,4 and 17-35*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Thinh T Nguyen /
Primary Examiner
Art Unit: 2818

Continuation of 11. does NOT place the application in condition for allowance because: Amendments to claim 1,17,31,32 raised new issues for claims 1,2,4,17-35; more searches are required.

/TTN/

Patent Examiner

Art Unit 2818

DO NOT ENTER: /T.N./

/Thinh Nguyen/ 08/11/2010

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
GROUP ART UNIT 2818

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	Docket No.: P2317US00
Jong Lam LEE, *et. al.*	
Serial No.: 11/993,965	Group Art Unit: 2818
Confirmation No.: 2191	
Filed: December 26, 2007	Examiner: NGUYEN, Thinh T.

For: **LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME**

Mail Stop: AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY AND AMENDMENT UNDER 37 C.F.R. § 1.116

Sir:

In response to the Final Office Action dated June 29, 2010 ("Office Action"), Applicants respectfully request reconsideration of the application in view of the following Amendments and Remarks.

Amendments to the Claims begin on page 2.

Remarks begin on page 7.

Applicants believe that no extensions of time are required at this time. If extensions of time are necessary to prevent abandonment of this application, then they are hereby petitioned for under 37 C.F.R. § 1.136(a). Applicants believe that no further fees for net addition of claims are required at this time. Any fees required for further extensions of time and any fees for the net addition of claims are hereby authorized to be charged to our Deposit Account No. 50-3698.

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	11/993,965	Filing Date	2007-12-26	Docket Number (if applicable)	P2317US00	Art Unit	2818
First Named Inventor	Jong Lam Lee			Examiner Name	NGUYEN, THINH T.		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☒ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☐ Enclosed

- ☐ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 503698

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/hae-chan park/	Date (YYYY-MM-DD)	2010-08-23
Name	Hae-Chan Park	Registration Number	50114

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal	
Application Number:	11993965
Filing Date:	26-Dec-2007
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Filer:	Hae-Chan Park/eun jo
Attorney Docket Number:	P2317US00
Filed as Large Entity	

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	810	810
		Total in USD ($)		**810**

Electronic Acknowledgement Receipt

EFS ID:	8267017
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
Receipt Date:	23-AUG-2010
Filing Date:	26-DEC-2007
Time Stamp:	19:52:17
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$810
RAM confirmation Number	6685
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Request for Continued Examination (RCE)	P2317US00_RCE.pdf	768779 ddf5d9c72c665490a77af3101bf5fcb2169589b3	no	3
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	30176 df4d1052f714330de7df06e92ea5fed32b462056	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	798955		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/993,965	12/26/2007	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	08/23/2010	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 22	Minus	** 22	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/AMANDA FORD/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	11993965
Filing Date	2007-12-26
First Named Inventor	Jong Lam Lee
Art Unit	2818
Examiner Name	NGUYEN, THINH T.
Attorney Docket Number	P2317US00

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317US00

	1	Non-Final Office Action of U.S Patent Application No. 12/630,370 issued on December 09, 2010.	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317US00

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2010-12-09
Name/Print	Hae-Chan Park	Registration Number	50114

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	9000535
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
Receipt Date:	09-DEC-2010
Filing Date:	26-DEC-2007
Time Stamp:	14:29:42
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	P2317US_IDS.pdf	990517 b5fa967c5f97d67d15ab740a4aed0a4c4080f43e	no	4

Warnings:
Information:

A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.

2	NPL Documents	P2317USC2_OA12_09_2010.pdf	887882 717a749d7f571468bf359d2ff607644598a68527	no	26

Warnings:

Information:

Total Files Size (in bytes):	1878399

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317US00

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7598149		2009-10-06	Dawson et al.	
	2	7057208		2006-06-06	Akimoto et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317US00

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Non-Final Office Action of U.S Patent Application No. 12/613,275 issued on December 23, 2010.	☐

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317US00

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2010-12-29
Name/Print	Hae-Chan Park	Registration Number	50114

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

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Electronic Acknowledgement Receipt

EFS ID:	9132322
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/Charles Greene
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
Receipt Date:	29-DEC-2010
Filing Date:	26-DEC-2007
Time Stamp:	18:07:32
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	P2317US00_IDS.pdf	999145 237efcaf8dc0bbd3fcdcb4fad6a7b92a0d8e9106	no	4

Warnings:	
Information:	

2	NPL Documents	P2317USD1_NFOA.pdf	973342 6baddc50ea917bcf723bcd04a9251461a3b60da6	no	29

Warnings:	
Information:	
Total Files Size (in bytes):	1972487

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New Applications Under 35 U.S.C. 111
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National Stage of an International Application under 35 U.S.C. 371
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New International Application Filed with the USPTO as a Receiving Office
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PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	11993965
Filing Date	2007-12-26
First Named Inventor	Jong Lam Lee
Art Unit	2818
Examiner Name	NGUYEN, THINH T.
Attorney Docket Number	P2317US00

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317US00

	1	Notice of allowance of US Patent Application No. 12/613,275 issued on March 25, 2011.	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317US00

CERTIFICATION STATEMENT

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☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2011-03-30
Name/Print	Hae-Chan Park	Registration Number	50114

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronic Acknowledgement Receipt	
EFS ID:	9771801
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
Receipt Date:	30-MAR-2011
Filing Date:	26-DEC-2007
Time Stamp:	16:09:21
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	P2317US00_IDS.pdf	990323 5954f0b3dc30c5d709682a6033f3047e6d938194	no	4
Warnings:					
Information:					

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2	NPL Documents	P2317USD1_NOA.pdf	397048 4df7505bd84b405e80fd9ccfec5e4174d27b7b9a	no	8

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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317US00

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317US00

	1	Notice of Allowance of US Patent Application No. 12/630,370 issued on May 6, 2011.	☐

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	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317US00

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☒ A certification statement is not submitted herewith.

SIGNATURE

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Signature	/hae-chan park/	Date (YYYY-MM-DD)	2011-05-11
Name/Print	Hae-Chan Park	Registration Number	50114

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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Electronic Acknowledgement Receipt

EFS ID:	10065868
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
Receipt Date:	11-MAY-2011
Filing Date:	26-DEC-2007
Time Stamp:	14:34:41
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	P2317US00_IDS.pdf	990308 a166594429be86883cd4b7de14a0bee5bd3879b6	no	4

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2	NPL Documents	P2317USC2_NOA_5_6_2011.pdf	561268 5a5011919ee677a4051a4264b06f212552ba88d0	no	13

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	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, Thinh T.
	Attorney Docket Number	P2317US00

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	1	2002-043633	JP		2002-02-08	STANLEY ELECTRIC CO LTD		☐
	2	10-2004-0005098	KR		2004-01-16	VICHEL INC.		☐
	3	2005/008791	WO		2005-01-27	MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.		☐

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	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, Thinh T.
	Attorney Docket Number	P2317US00

	4	2005-019874	JP		2005-01-20	MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.		☐
	5	2005/050748	WO		2005-06-02	NICHIA CORPORATION		☐
	6	2002-237646	JP		2002-08-23	NICHIA CHEM IND LTD		☐

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Signature	/hae-chan park/	Date (YYYY-MM-DD)	2011-09-15
Name/Print	Hae-Chan Park	Registration Number	50114

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PATENT ABSTRACTS OF JAPAN

(11)Publication number : **2002-043633**
(43)Date of publication of application : **08.02.2002**

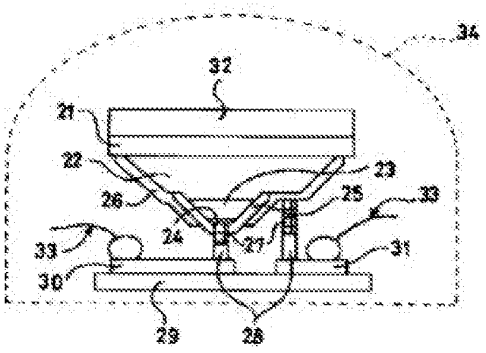
(51)Int.Cl. **H01L 33/00**

(21)Application number : **2000-223513**
(22)Date of filing : **25.07.2000**

(71)Applicant : **STANLEY ELECTRIC CO LTD**
(72)Inventor : **KATO MUNEHIRO**
SANO MICHIHIRO
SATO HIROYUKI
MORIKAWA KENICHI

(54) WHITE LIGHT EMITTING DIODE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a white light emitting diode having excellent color rendering properties required for liquid crystal backlight in which emission lifetime characteristics are enhanced by reducing deterioration of mold resin.
SOLUTION: In the white light emitting diode where UV rays emitted from a pumping element having an n-type semiconductor layer 22 and a p-type semiconductor layer 23 is converted through a wavelength conversion element 32 into white light and irradiated through a mold resin 34, the wavelength conversion element 32 is arranged on one side of the pumping element and an insulation film 25 is arranged on the other side thereof through a p-type ohmic electrode 24. Furthermore, side face of the pumping element is covered with an n-type ohmic electrode 26 exhibiting high reflectivity in UV wavelength.



(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号
特開2002－43633
（P2002－43633A）
(43)公開日　平成14年２月８日(2002.2.8)

(51)Int.Cl.[7]	識別記号	ＦＩ	テーマコード*(参考)
Ｈ０１Ｌ　33/00		Ｈ０１Ｌ　33/00	Ｎ　５Ｆ０４１ Ａ Ｃ

審査請求　有　　請求項の数２　ＯＬ　（全　６　頁）

(21)出願番号　特願2000－223513(P2000－223513)

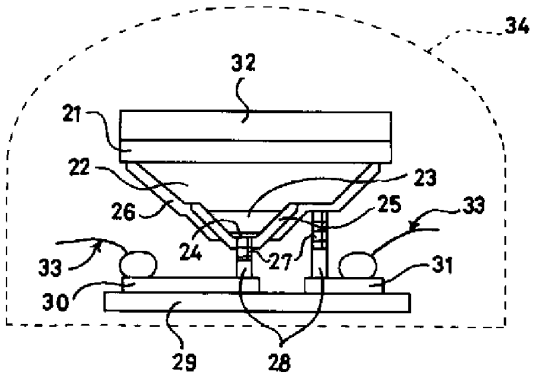
(22)出願日　平成12年７月25日(2000.7.25)

(71)出願人　000002303
スタンレー電気株式会社
東京都目黒区中目黒２丁目９番13号
(72)発明者　加藤　宗弘
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(74)代理人　100076196
弁理士　小池　寛治

最終頁に続く

(54)【発明の名称】　白色発光ダイオード

(57)【要約】
【課題】　液晶用バックライトなどとして演色性に優れた構成とし、かつ、モールド樹脂の劣化を少なくして発光寿命特性を改善した白色発光ダイオードを提供すること。
【解決手段】　ｎ型半導体層２２とＰ型半導体層２３からなる励起素子が発光する紫外線光を波長変換素子３２によって白色光に変換し、白色光をモールド樹脂３４を通して照射する白色発光ダイオードにおいて、励起素子の一面側に波長変換素子３２を、その他面側にＰ型オーミック電極２４を介在させて絶縁膜２５を各々配設し、さらに、励起素子の側面を紫外線波長において高反射率のｎ型オーミック電極２６によって覆う構成としてある。



1

【特許請求の範囲】

【請求項１】　Ｐ型半導体とｎ型半導体とによって紫外線光を発光する励起素子と、この励起素子の発光を蛍光体によって白色波長光に変換する波長変換素子と、これら励起素子及び波長変換素子を覆う透明なモールド樹脂とからなる白色発光ダイオードにおいて、

Ｐ型半導体とｎ型半導体の接合部分に平行する励起素子の一面側に波長変換素子を配設すると共に、紫外線波長とその近傍の波長において透明な絶縁膜を上記接合部分が位置する励起素子側面に設け、

さらに、紫外線波長とその近傍の波長において高反射率のＰ型オーミック電極とｎ型オーミック電極とで励起素子の一面以外の他面を覆うようにこれらオーミック電極を設けて構成したことを特徴とする白色発光ダイオード。

【請求項２】　請求項1に記載した白色発光ダイオードにおいて、

一面側を広く、その対向側を狭くするように励起素子側面を９０°以下の角度で傾斜形成させたことを特徴とする白色発光ダイオード。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】この発明は、照明器具、インジケータ、ディスプレイ、表示器のバックライトなどとして使用する白色発光ダイオードに関する。

【０００２】

【従来の技術】図５は現在実用化されている白色発光ダイオードを示す断面図である。この発光ダイオードは、サファィア基板上にｎ型半導体（ｎ型ＧａＮ）とＰ型半導体（Ｐ型ＧａＮ）とを成長させたＧａＮ系の青色励起素子１１がメタルステム１２にダイボンディングされている。

【０００３】そして、青色励起素子１１はそのｎ型層がメタルステム１２に、そのＰ型層がメタルステム１３に各々金線１４、１５によって電気接続され、また、青色励起素子１１には蛍光体１６が所定の厚みで塗布形成されている。

【０００４】このように構成した青色励起素子１１、金線１４、１５、蛍光体１６、メタルステム１２、１３の一部が透明なエポキシ系樹脂材のモールド樹脂１７によって包囲され、白色発光ダイオードとして構成されている。

【０００５】上記の白色発光ダイオードは、青色励起素子１１が青色光源として青色光を発光し、この青色光が蛍光体１６によって波長変換されて白色光を照射する。

【０００６】

【発明が解決しようとする課題】図６は上記した白色発光ダイオードの発光スパクトルを示す。この発光スパクトルから分かるように、上記の白色発光ダイオードは、青色励起素子１１の発光（波長４５０ｎｍ近傍）と、蛍

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光体１６の発光（波長５８０ｎｍ近傍）とによって生成される白色光となる。

【０００７】したがって、この白色発光ダイオードは、光の三原色である青色（波長４５０ｎｍ）、緑色（波長５２５ｎｍ）、赤色（波長６６０ｎｍ）から白色光を形成するものではないため、室内灯や液晶画面のバックライトなどとして使われている蛍光灯の代替発光ダイオードとしては演色性などの点で問題となっている。

【０００８】この問題を解決する１つの有効な手段として、ＺｎＯ系或いはＧａＮ系の紫外励起素子の紫外線光を蛍光体を用いて波長変換し、白色光を照射させる構成とした白色発光ダイオードが提案されている。

【０００９】しかし、紫外励起素子を光源とするこのような白色発光ダイオードは、励起素子の紫外線光によってモールドされたエポキシ系樹脂が劣化し、モールド樹脂の透過率が経時的に低下するため、白色発光出力が低下してしまうと言う問題がある。

【００１０】本発明は上記した実情にかんがみ、液晶用バックライトなどとして演色性に優れた構成とし、かつ、モールド樹脂の劣化を少なくして発光出力寿命を改善した紫外励起素子を励起光源とする白色発光ダイオードを提供することを目的とする。

【００１１】

【課題を解決するための手段】上記した目的を達成するため、本発明では、Ｐ型半導体とｎ型半導体とによって紫外線光を発光する励起素子と、この励起素子の発光を蛍光体によって白色波長光に変換する波長変換素子と、これら励起素子及び波長変換素子を覆う透明なモールド樹脂とからなる白色発光ダイオードにおいて、Ｐ型半導体とｎ型半導体の接合部分に平行する励起素子の一面側に波長変換素子を配設すると共に、紫外線波長とその近傍の波長において透明な絶縁膜を上記接合部分が位置する励起素子側面に設け、さらに、紫外線波長とその近傍の波長において高反射率のＰ型オーミック電極とｎ型オーミック電極とで励起素子の一面以外の他面を覆うようにこれらオーミック電極を設けて構成したことを特徴とする白色発光ダイオードを提案する。

【００１２】このように構成した白色発光ダイオードは、励起素子が光源となって紫外線光を発光する。そして、励起素子の一面側に向かって射出する紫外線光が波長変換素子によって白色光に波長変換され、白色光がモールド樹脂を通って外方に照射される。

【００１３】また、励起素子の一面側以外の他の側面に向かって射出する紫外線光は、高反射率のＰ型オーミック電極とｎ型オーミック電極によって反射されるため、モールド樹脂には入射しない。

【００１４】この結果、紫外線光が波長変換素子の蛍光体によって白色光に変換されるので、演色性に優れた白色発光ダイオードとなる。また、紫外線光がモールド樹脂に入射しないことから、モールド樹脂の劣化が極めて

少なく、長期間使用によっても発光出力がほとんど低下しない白色発光ダイオードとなる。

【００１５】また、上記した白色発光ダイオードは、一面側を広く、その対向面側を狭くするように励起素子側面を傾斜形成することによって、発光出力を増大させることができる。

【００１６】すなわち、励起素子側面には紫外線波長において高反射率のオーミック電極が設けてあるから、励起素子側面を傾斜形成することによって、オーミック電極が波長変換素子に向かって紫外線光を反射させる。この結果、波長変換素子によって白色光に波長変換される紫外線光が増加することから、白色発光出力が増大する。

【００１７】

【発明の実施の形態】次に、本発明の実施形態について図面に沿って説明する。図１は本発明の一実施形態を示す白色発光ダイオードの構成図である。

【００１８】この図において、２１は基板、２２はｎ型半導体層、２３はＰ型半導体層、２４はＰ型オーミック電極、２５は絶縁膜、２６はｎ型オーミック電極、２７はマウント用ボンディングパッド、２８は共晶電極、２９は絶縁性基板、３０はアノード引き出し電極、３１はカソード引き出し電極、３２は波長変換素子、３３は金線、３４はモールド樹脂を示す。

【００１９】この白色発光ダイオードは、紫外線光を透過するサファィアなどの基板２１の面上にｎ型半導体層２２（ｎ型ＧａＮまたはｎ型ＺｎＯ）を形成した後、その上にＰ型半導体層２３（Ｐ型ＧａＮまたはＰ型ＺｎＯ）を形成してデバイスウエハを構成する。

【００２０】なお、ＧａＮ半導体層は一般的なＭＯＣＶＤ（有機金属化学気相成長）法によって代表される成膜法によって形成し、また、ＺｎＯ半導体層はレーザーアブレーション法やＭＢＥ（分子線エピタキシー）法などの成膜法によって形成することができる。

【００２１】また、ｎ型半導体層２２とＰ型半導体層２３については、Ｐ型半導体層２３を基板２１側に膜形成し、その上にｎ型半導体層２２を形成するようにしてもよい。

【００２２】このように構成したデバイスウエハは液晶エッチングまたは気相エッチングによってｎ型半導体層２２を露出させ、その後、Ｐ型半導体層２３上にＮｉ、Ａｕ、Ｐｔ、Ｐｈなどの金属で形成したＰ型オーミック電極２４を設ける。

【００２３】このＰ型オーミック電極２４は紫外線光の波長領域における反射率が高い材料を使うことが好ましく、このＰ型オーミック電極２４とマウント用ボンディングパッド２７とで励起素子外部に紫外線光を放出させない電極構造とする。

【００２４】Ｐ型オーミック電極２４を形成した後に、ＳｉｘＮｙ、ＳｉＯ2、ＡＩ２０３などの紫外線領域で透明な絶縁膜２５を形成する。

【００２５】この絶縁膜２５は、デバイスウエハとＰ型オーミック電極２４との全体を電子線加熱蒸着法やスパッタ法、化学気相成膜法などを用いて形成することができる。そして、励起素子の電気的接触を得るために、Ｐ型オーミック電極２４の一部とｎ型半導体層２２の一部については絶縁膜を形成しないか、または、絶縁膜を形成した後に電気的接触部分を除去する構造とする。

【００２６】本実施形態における絶縁膜２５は、Ｐ型半導体層２３の側面と、ｎ型半導体層２２とＰ型半導体層２３の接合部分が位置する側面とを覆うように形成して電気的短絡を防止するように設けてある。

【００２７】絶縁膜２５を形成した後に、紫外線波長において高い反射率のＴｉ、Ａｇ、Ａｌなどで形成したｎ型オーミック電極２６をデバイスウエハ側面の全体を覆うように形成する。

【００２８】Ｐ型オーミック電極２４とｎ型オーミック電極２６を形成した後に、マウント用ボンディングパッド２７をＴｉ、Ｎｉ、Ａｕなどの金属材で形成し、次に、Ａｕ－Ｓｕなどで共晶電極２８を順次形成する。

【００２９】これらマウント用ボンディングパッド２７と共晶電極２８は別々に形成しても、一括に形成してもよく、また、Ｐ型オーミック電極２４とｎ型オーミック電極２６と一括形成してもよい。

【００３０】なお、一般的には、Ｐ型オーミック電極２４又はｎ型オーミック電極２６を形成した後、または、すべての電極を形成した後に、各半導体層と電極との電気的、機械的接触特性を改善するために加熱処理する。

【００３１】全ての電極を形成した後に、ダイシング法またはスクライブ法によって個々のＬＥＤチップ（起動素子）に分離し、このＬＥＤチップをサブマウント基板にダイボンディングする。

【００３２】つまり、絶縁性基板２９上にアノード引き出し電極３０とカソード引き出し電極３１を形成したサブマウント基板を設け、Ｐ型半導体層２３をサブマウント側になるようにしてＬＥＤチップをこのサブマウント基板にダイボンディングする。そして、ＬＥＤチップをダイボンディングしたサブマウント基板はＬＥＤフレームなどにマウントし、電極３０、３１を金線３３によって電気接続する。

【００３３】さらに、基板２１の面上に蛍光体と多層光学薄膜と前記２点を保持する基板（ガラス、サファイア等：図示せず）からなる波長変換素子３２をマウントする。この波長変換素子３２に含まれる多層光学薄膜により、励起光である紫外線光は蛍光体側に反射し、モールド樹脂３４に入射しない。

【００３４】モールド樹脂３４は、ＬＥＤチップとサブマウント基板を覆うように設けた透明なエポキシ系樹脂材によって形成する。

【００３５】上記のように構成した白色発光ダイオード

は、励起素子が紫外線光を発光し、この紫外線光が波長変換素子３２によって白色光に波長変換され、白色光がモールド樹脂３４を透過して照射される。

【００３６】また、本実施形態では、図示するように、波長変換素子３２側を広く、Ｐ型オーミック電極２４側を狭くするように励起素子側面を傾斜形成し、この傾斜面にｎ型オーミック電極２６を設けたので、紫外線光がこのオーミック電極２６によって反射され、モールド樹脂３４には入射しない。

【００３７】その上、ｎ型オーミック電極２６が紫外線領域において高い反射率のものとなっているので、この電極２６によって反射された紫外線光が波長変換素子３２に導光される。この結果、波長変換素子３２によって波長変換される紫外線光が増加し、出力される白色光が増大する。

【００３８】一方、励起素子の側面を上記のように傾斜させることにより、絶縁膜２５の形成が容易となり、ｎ型半導体層２２とＰ型半導体層２３との間の電気絶縁の信頼性が向上し、結果として励起素子の歩留りを改善することができる。

【００３９】したがつて、励起素子側面の傾斜は、励起素子の歩留りを改善するなら基板２１に対して９０°以下とすればよいが、ｎ型オーミック電極２６で反射した紫外線光を波長変換素子３２に供給する構成とする場合は励起素子側面は基板２１に対して４５°程度に傾斜させることが好ましい。

【００４０】他方、本実施形態の改善案としては、ｎ型オーミック電極２６をＰ型半導体層２３の側面に直接に形成してもよい。ただし、この場合には、ｎ型オーミック電極２６とＰ型オーミック電極２４とを電気的に絶縁する必要がある。

【００４１】また、Ｐ型オーミック電極２４によって励起素子側面を覆う構成とすることができる。この場合、ｎ型オーミック電極２６はマウント用ボンディングパッド２７と合せて紫外線光を外部に放射させない電極構造とし、また、ｎ型半導体層２２の側面と、ｎ型半導体層２２とＰ型半導体層２３との接合部分が位置する側面には絶縁膜２５を設ける必要がある。

【００４２】図２は実際に実施した白色発光ダイオードの実施例を示す断面図である。この実施例の白色発光ダイオードは図１に示す白色発光ダイオードと同じ工程で構成してあるから、同じ部材と部所については同じ参照符号が付してある。

【００４３】この実施例の励起素子としては、サファィア基板２１上に紫外線光を発光させるＧａＮ系半導体層をＭＯＣＶＤ法により形成し、デバイスウエハを構成した。

【００４４】そして、このデバイスウエハは、塩素系ガスを用いた反応性イオンエッチング（ＲＩＥ）法により、Ｐ型ＧａＮ層と活性層部分をエッチング（表面から約４０００Ａ程度）し、ｎ型ＧａＮ層を露出させた。

【００４５】Ｐ型オーミック電極２４、絶縁膜２５、ｎ型オーミック電極２６の各々には、Ｎｉ（１０Ａ）／Ｐｈ（３０００Ａ）、ＳｉＯ２（４０００Ａ）、Ｔｉ（２５０Ａ）／Ａｌ（１５０００Ａ）を使用した。

【００４６】その後ランプ加熱を利用したラピッドサーマルアニーリング法を用いてデバイスウエハを加熱処理した。そのときの加熱条件は、５００℃、２０Ｓｅｃであり、雰囲気は窒素雰囲気によって行なった。

【００４７】この加熱処理後に、マウント用ボンディングパッド２７（Ｔｉ（４００Ａ）／Ａｕ（１００００Ａ））と共晶電極２８（Ａｕ－Ｓｕ）を順次形成した。なお、全ての電極と絶縁膜は電子線加熱蒸着法によって成膜し、パターニングはリフトオフ法によって行なった。

【００４８】全ての電極を形成したデバイスウエハはスクライブ法によってＬＥＤチップ分離し、このＬＥＤチップをサブマウントにダイボンディングした。そして、サファィア基板２１上に波長変換素子３２を設置し、また、モールド樹脂を設けて白色発光ダイオードを構成した。

【００４９】なお、特性比較のために、活性層側面部分（ｎ型半導体層２２とＰ型半導体層２３の接合部分が位置するデバイスウエハの側面部分）に反射作用のｎ型オーミック電極２６を設けない紫外ＬＥＤチップを用いた白色発光ダイオード（便宜上、従来タイプの白色発光ダイオードという）を上記同様にして構成した。図３はこのように構成した従来タイプの白色発光ダイオードのＬＥＤチップを示す断面図である。

【００５０】図４は図２に示したＬＥＤチップを使用した本発明の白色発光ダイオードと、図３に示したＬＥＤチップを使用した従来タイプの白色発光ダイオードとの発光出力比の寿命特性を示す。

【００５１】なお、この図において、曲線Ａは本発明の白色発光ダイオードの寿命特性を、曲線Ｂは従来タイプの白色発光ダイオードの寿命特性を各々示す。

【００５２】曲線Ａより分かるように、本発明の白色発光ダイオードは、１１５０時間後に測定した発光出力が寿命試験開始直後に測定した発光出力に比べて約９８％となることが確認された。

【００５３】また、曲線Ｂの通り、従来タイプの白色発光ダイオードは、１１５０時間後の発光出力が寿命試験開始直後に測定した発光出力に比べて約８８％となることが確認された。

【００５４】この結果、本発明の白色発光ダイオードによれば、発光寿命特性が１１５０時間の連続点灯で約１０％改善されることが判明した。

【００５５】

【発明の効果】上記した通り、本発明の白色発光ダイオードは、波長変換素子を配設する励起素子の一面側以外

の他面を高反射率のオーミック電極で覆う構成としたことから、励起素子が発光する紫外線光がモールド樹脂に入射しない。

【００５６】したがって、モールド樹脂が経時的にも劣化しないから、波長変換素子で波長変換された白色光がモールド樹脂を透過して効果的に出力され、発光寿命特性の優れた白色発光ダイオードとなる。

【００５７】また、本発明の白色発光ダイオードは、励起素子側面を傾斜させオーミック電極によって反射される紫外線光を波長変換素子に導光するようにすれば、励起素子が発光する紫外線光が効率よく白色光に変換されるから、発光出力を増大させることができる。

【００５８】さらに、家庭用蛍光灯などに使われている蛍光体と同様に、紫外線光によって励起される蛍光体を使用して白色発光ダイオードを構成することができるので、青、緑、赤の三原色の発光成分となる蛍光体を個々に調整することができ、幅広い領域の色調を得ることができる白色発光ダイオードとなる。

【図面の簡単な説明】

【図１】本発明の一実施形態として示した白色発光ダイオードの断面図である。

＊【図２】本発明の白色発光ダイオードに使用するＬＥＤチップを示す断面図である。

【図３】従来タイプの白色発光ダイオードのＬＥＤチップを示す断面図である。

【図４】本発明の白色発光ダイオードと従来タイプの白色発光ダイオードの発光寿命特性を示す図である。

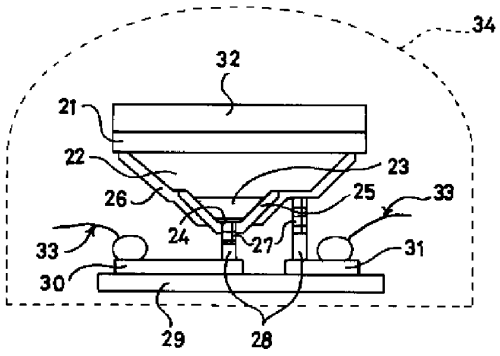
【図５】従来例とした示した白色発光ダイオードの断面図である。

【図６】従来例として示した白色発光ダイオードの発光スペクトルを示す図である。

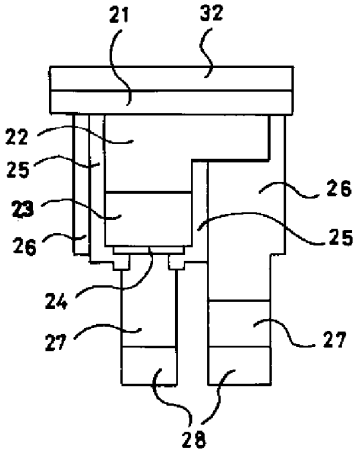
【符号の説明】

２１　基板
２２　ｎ型半導体層
２３　Ｐ型半導体層
２４　Ｐ型オーミック電極
２５　絶縁膜
２６　ｎ型オーミック電極
２７　マウント用ボンディングパッド
２８　共晶電極
３２　波長変換素子
３４　モールド樹脂

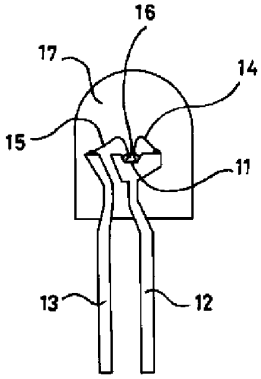
【図１】



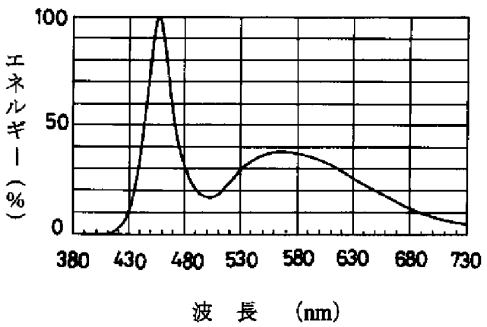
【図２】



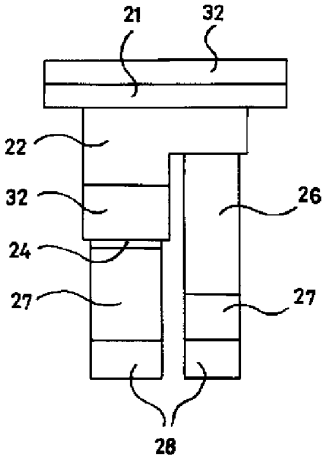
【図５】



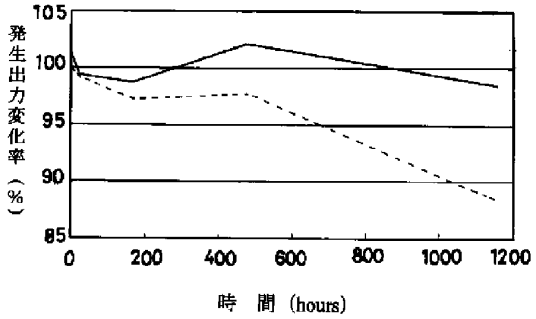
【図６】



【図３】



【図４】



フロントページの続き

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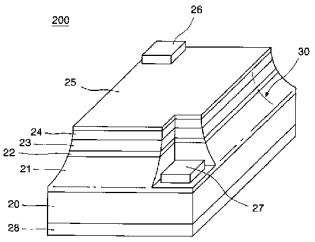
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(71)Applicant: VICHEL INC.
(72)Inventor: KANG, SANG GYU

(54) NITRIDE SEMICONDUCTOR LED AND FABRICATING METHOD THEREFOR

(57) Abstract:



PURPOSE: A nitride semiconductor LED and a fabricating method therefor are provided to reduce the consumption of chips due to a cutting process by using a scribing process and a cleaving process including a laser process. CONSTITUTION: A nitride semiconductor LED includes an active layer(22) and a p-type and n-type doping layers(24,21). The active layer(22) is formed by depositing a nitride semiconductor on a substrate(20). The p-type and n-type doping layers(24,21) are formed on an upper surface and a bottom surface of the active layer(22). An inclined portion(30) is formed on one outer side of an upper portion of the substrate(20) including the active layer(22) and the p-type and n-type doping layers (24,21). The inclined portion(30) is formed by using a scribing method including a laser process.

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1	1-1-2002-0217145-06	2002.07.08	Patent Application (특허출원서)	Acceptance (수리)
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6	9-5-2004-0267877-29	2004.06.30	Decision to Refuse a Patent (거절결정서)	Dispatched (발송처리완료)
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(54) 질화물계 반도체 발광 소자 및 그 제조방법

요약

본 발명은 질화물계 반도체 발광 소자의 칩 생산수율과 그 자체의 광 이용효율을 극대화시킨 질화물계 반도체 발광 소자 및 그 제조방법을 제공하기 위한 것으로, 본 발명에 의하면 기판(20)상에 질화물계 반도체로 된 활성층(22)과, 이 활성층(22)의 상부 및 하부에 각각 형성된 질화물계 반도체로 된 p형 및 n형 도핑층(24, 21)을 구비하여 이루어진 질화물계 반도체 발광 소자(200; 300; 400; 500; 600)에 있어서, 상기 소자의 기판(20) 외측면 또는 활성층(22)과 상기 도핑층(21, 24)을 둘러싸는 외측면에는 레이저 가공을 통한 흠집내기(Scribing) 공정 및 절개 공정에 의해 경사지게 절개된 경사부(30; 40)가 형성되는 것을 특징으로 하는 질화물계 반도체 발광 소자가 제공된다.

대표도

도 3

색인어

질화물계, 반도체, 발광 소자, 결정 구조, 전반사, 경사부

명세서

도면의 간단한 설명

도 1은 일반적인 질화물계 발광 다이오드의 구조를 개략적으로 나타낸 도면,

도 2는 종래의 직육면체 구조의 질화물계 발광 다이오드의 수평 단면을 통해서 임의의 점광원에서 발생한 빛의 순환적인 전반사 과정을 설명하기 위한 도면,

도 3은 본 발명의 제1 실시예에 따른 질화물계 반도체 발광 소자의 구조를 개략적으로 나타낸 사시도,

도 4는 본 발명의 실시예에 따른 질화물계 반도체 발광 소자의 제조 공정에서 흠집내기 공정을 설명하기 위한 도면,

도 5는 본 발명의 실시예에 따른 질화물계 반도체 발광 소자의 제조 공정에서 흠집내기 공정의 또다른 예를 설명하기 위한 도면,

도 6은 본 발명의 제2 실시예에 따른 질화물계 반도체 발광 소자의 일예를 개략적으로 나타낸 사시도,

도 7a는 본 발명의 제2 실시예에 따른 질화물계 반도체 발광 소자의 다른 예를 개략적으로 나타낸 사시도,

도 7b는 도 7a의 평면도,

도 8은 질화물계 반도체가 가지는 정육각형 기둥 모양의 단위 결정 구조를 나타낸 도면,

도 9는 도 8의 단위 결정 구조들이 주기적으로 배열된 질화물계 반도체의 결정 구조를 (0001)면에서 바라본 것을 단순화시켜 나타낸 도면,

도 10a 내지 도 10c는 본 발명의 제2 실시예에 따른 정삼각형, 평행사변형, 사다리꼴 모양의 수평 단면을 갖는 질화물계 반도체 발광 소자의 제조 공정을 설명하기 위한 도면,

도 11a는 본 발명의 제3 실시예에 따른 질화물계 반도체 발광 소자를 설명하기 위한 도면,

도 11b는 도 11a의 평면도,

도 12는 본 발명의 실시예에 따른 질화물계 반도체 발광 소자의 제조 공정에서 흠집내기 공정의 또다른 예를 설명하기 위한 도면,

도 13a는 본 발명의 제4 실시예에 따른 질화물계 반도체 발광 소자를 설명하기 위한 도면,

도 13b는 도 13a의 평면도,

도 14는 전자 소자의 인쇄회로기판에 실장되는 본 발명의 제4 실시예에 따른 질화물계 반도체 발광 소자의 일예를 설명하기 위한 도면,

도 15는 도 14에서 인쇄회로기판 위에 플립칩 본딩되는 발광 소자의 배치를 설명하기 위한 도면.

* 도면의 주요 부분에 대한 부호의 설명 *

20 : 기판 21, 24 : 도핑층

22 : 활성층 23 : 클래드층

26, 27 : 전극 30, 40 : 경사부

72a, 72b : 전극 패턴 74a, 74b : 솔더 범프

200, 300, 400, 500, 600 : 발광 소자

700 : 인쇄회로기판

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 질화물계 반도체 발광 소자와 그 제조방법 및 이를 이용한 전자 소자에 관한 것으로, 특히 칩 생산수율(yiel

d)과 소비전력 대비 광 이용효율(quantum efficiency)을 극대화한 질화물계 반도체 발광 소자 및 그 제조방법에 관한 것이다.

일반적으로 질화물계 반도체 발광 다이오드(Nitride Semiconductor LED, 100)는 도 1에 도시된 바와 같이 기판(20) 상에 실제로 빛을 발생시키기 위한 InGaN 등의 활성층(22)과, 이 활성층(22)의 상부 및 하부에 각각 형성되어 활성층(22)에 전류를 공급할 수 있도록 다이오드 구조를 만드는 GaN 등의 n형 및 p형 도핑층(21, 24)을 구비하고 있다. 또한, 전하를 띤 캐리어들의 누적 효율을 증가시키기 위해 보다 큰 에너지 밴드갭을 갖는 AlGaN 등의 p형 클래드층(23)을 활성층(22)과 p형 도핑층(24) 사이에 추가적으로 구비하기도 한다. 도 1에서 25, 26, 27 및 28은 각각 p형 투명전극, p형 전극, n형 전극 및 반사용 금속층을 나타낸다.

한편, 종래의 질화물계 반도체 발광 다이오드는 대체로 직육면체, 즉 사각기둥의 구조를 취하고 있으며, 이러한 직육면체 구조의 질화물계 반도체 발광 다이오드를 제작하기 위해서는 일반적으로 다이아몬드 등의 절삭 공구를 이용하여 절삭을 행한다.

그러나 직육면체 구조의 발광 다이오드는 전반사 현상으로 인해 낮은 광 이용효율을 갖는다. 이는 발광 다이오드의 패키징 공정에서 칩 몰딩시 사용되는 에폭시의 굴절율이 칩의 굴절율보다 낮아서 칩 내부의 활성 영역에서 발생한 빛이 칩으로부터 에폭시쪽으로 빠져나올 때, 그 경계면에 어떤 임계각 이상으로 입사하는 모든 빛들은 빠져 나오지 못하기 때문이다.

도 2는 종래의 직육면체 구조의 질화물계 발광 다이오드의 수평 단면을 통해서 임의의 점광원에서 발생한 빛의 순환적인 전반사 과정을 설명하기 위한 도면이다. 여기서 사방으로 임계각의 원뿔 영역(빗금친 부분에 해당함)을 제외한 영역으로 경계면에 입사한 빛들은 계속해서 모든 경계면에서 전반사 영역에 머물게 되어 영원히 바깥으로 빠져나올 수 없게 된다. 도 2에서 어느 점광원에서 발생된 빛이 전반사각에 해당하는 θ_1 로 경계면에 입사하게 되면, 다음 경계면에서는 $\theta_2 = \theta_{10}$ 로 입사하게 되므로 결국 순환적인 전반사가 일어나게 된다. 직사각형 형태의 대칭성으로 인해

수학식 1

$$\theta_1+\theta_2=\theta_1+\theta_{10}=\pi/2$$

가 되므로, $\theta_c<\pi/4$ 이고 $\theta_c<\theta_1<\pi/2-\theta_c$ 인 경우에는 입사각 θ_1 에 대하여 순환적인 전반사가 일어남을 다음과 같이 쉽게 입증할 수 있다.

수학식 2

$$\theta_c<\theta_2(=\theta_{10}=\pi/2-\theta_1)<\pi/2-\theta_c$$

직육면체의 경우, 실제로는 3차원이므로 임의의 광원이 접하는 면은 모두 6개가 된다. 따라서 경계면내 임의의 한 점을 생각해 볼 때, 그 점을 꼭지점으로 하여 임계각과 같은 각도로 형성된 원뿔내로 입사하는 광자들만 바깥으로 빠져나올 수 있다.

실제로, 에폭시의 굴절율은 대개 약 1.5이고 질화갈륨(GaN)의 굴절율은 약 2.5이므로, 이를 전반사 임계각에 관한 수학식 3에 넣어서 계산해 보면, 발광 다이오드 칩의 전반사 임계각 θ_c 는 약 36.9° 가 된다.

수학식 3

$$\theta_c=\arcsin(n_{epoxy}/n_{GaN})$$

결국 경계면의 수직면에 36.9° 이상 53.1° ($\pi/2-\theta_c$) 이하의 각으로 입사한 빛들은 모두 반사되어 바깥으로 빠져나올 수 없다. 다른 요소들을 고려하지 않고 이상적인 직육면체 모양의 발광 다이오드 칩을 고려하여 광 이용효율을 계산해 보면,

수학식 4

$$\eta_{trans}=3[1-\{1-(n_{epoxy}/n_{GaN})^2\}^{1/2}]$$

을 통해서 광 이용효율 $\eta_{trans}=0.6$ 의 값을 얻을 수 있다.

위의 예는 실제의 발광 다이오드와는 다른 이상적인 예이지만, 전반사 현상으로 인하여 발생된 모든 빛을 이용할 수 없다는 사실은 자명하다. 실제 발광 다이오드는 전극을 통해 넣어준 전류가 발광 다이오드의 활성 영역에서 빛으로 전환되어 상하의 p형 및 n형 도핑층을 지나서 바깥으로 나오게 되므로, 이 과정에서 전기에너지의 빛에너지로의 전환 효율과 발광 다이오드내 결정층에서의 흡수, 굴절율과 다른 경계면에서 일어나는 일정량의 반사 등의 요소들을 모두 고려해 주어야만 정확한 광 이용효율을 구할 수가 있다. 더구나 대개의 발광 다이오드의 구조는 앞서 설명한 도 1에서와 같이 그 하측에 금속면을 증착하여 'n'형 전극으로 이용하거나 질화물계 반도체 발광 다이오드에서 사파이어(Al_2O_3) 등의 부도체 기판을 사용하는 경우에도 이 기판이 반사면으로 작용하기 때문에 아래쪽으로 진행하는 빛은 모두 다시 반사되어 활성 영역으로 되돌아온다. 따라서 관련된 모든 요소들을 고려해 볼 때, 일반적으로 실제 발광 다이오드는 입력된 전류량의 약 20% 미만의 광 이용효율을 가진다.

또한 질화물계 반도체는 기본적으로 정육각형(Hexagonal) 기둥 모양의 결정 구조(Crystal Structure)를 갖고 있기 때문에, 상기와 같이 다이아몬드 등의 절삭 공구를 이용하여 절삭을 행할 경우 절삭 공구가 갖는 두께와 그 두께만큼의 추가적인 웨이퍼의 손실을 가져온다. 따라서 질화물계가 아닌 다른 화합물로 된 반도체 발광 다이오드의 칩 제작시와 비교할 때, 최소 약 35% 이상의 칩 손실을 가져오게 된다.

예를 들어, 현재 보편적으로 사용되고 있는 다이아몬드 절삭 공구의 날 두께는 50㎛인데, 이를 사용하여 300㎛×300㎛ 크기의 정사각형 모양의 수평 단면 구조를 갖는 직육면체의 발광 다이오드의 칩을 만든다고 가정하자. 이 경우 절삭날이 기판을 지나가면서 절삭날 두께의 약 2배에 해당하는 100㎛ 이상의 폭에 해당하는 영역이 소실된다. 더욱이 이런 방식의 칩 제작과정에서는 절삭에 의해 생산된 칩마저 가장자리에 충격이 가해져 손상되기가 쉬우므로 실제로 이용가능한 칩의 수는 더욱 줄어든다.

한편, 이러한 광 이용효율을 고려한 기술이 대한민국 공개특허공보 제1998-83823호에 개시되어 있다. 동 공보에는 적은 소비전력으로 높은 휘도의 광을 발생시키기 위한 것으로, 발광 다이오드의 몸체의 적어도 어느 일부분의 수평 단면을 삼각형 또는 예각을 갖는 사변형으로 하고 수직 영역의 단면적이 수직 방향으로 점차적으로 증가 또는 감소하는 형태로 하는 것이 제안되어 있다.

그러나 상기한 기술은 광 이용효율의 측면에서는 종래에 비해 다소 개선된 것이라 할 수 있으나, 본 발명의 관심사 중의 하나인 칩 생산수율의 관점에서 보면 오히려 종래의 직육면체 형태의 반도체 발광 다이오드에 비해 칩 생산수율이 더욱 저하될 수밖에 없다는 문제점을 가지고 있다. 뿐만 아니라, 상기한 공보의 어느 곳에서도 기본적으로 정육각형 기둥 모양의 단위 결정 구조를 갖는 질화물계 반도체의 특성을 고려한 점을 찾아볼 수 없으며, 따라서 상기 기술이 본 발명에서와 같은 질화물계 반도체 발광 소자에 그대로 적용될 경우 다이아몬드 절삭 공구의 과도한 사용으로 인한 칩 생산수율의 현저한 감소를 초래할 수밖에 없다는 치명적인 문제점을 내포하고 있는 것이다.

발명이 이루고자 하는 기술적 과제

본 발명은 상기한 종래 기술의 문제점을 해결하기 위하여 안출된 것으로, 본 발명의 목적은 질화물계 반도체 발광 소자 자체의 광 이용효율을 크게 향상시킨 질화물계 반도체 발광 소자를 제공하는 데 있다.

본 발명의 또다른 목적은 질화물계 반도체 발광 소자의 제작시 절삭 공구의 사용으로 인한 불필요한 칩의 손실을 없앰으로써 칩 생산수율을 종래에 비해 현저히 개선한 질화물계 반도체 발광 소자의 제조방법을 제공하는 데 있다.

본 발명의 또다른 목적은 질화물계 반도체 발광 소자의 결정구조를 고려하여 레이저 가공을 이용한 흠집내기 공정을 이용함으로써 칩 생산수율을 종래에 비해 더욱 현저히 개선하고 동시에 질화물계 반도체 발광 소자 자체의 광 이용효율을 더욱 크게 향상시킨 질화물계 반도체 발광 소자 및 그 제조방법을 제공하는 데 있다.

발명의 구성 및 작용

상기한 목적을 달성하기 위한 본 발명은 기판상에 질화물계 반도체로 된 활성층과, 이 활성층의 상부 및 하부에 각각 형성된 질화물계 반도체로 된 p형 및 n형 도핑층을 구비하여 이루어진 질화물계 반도체 발광 소자에 있어서, 상기 소자의 활성층과 도핑층을 둘러싸는 외측면 중 적어도 어느 하나의 외측면은, 레이저 가공을 이용한 흠집내기(Scribing) 공정에 의해 경사지게 절개되어, 상기 기판의 상부측 방향으로 갈수록 단면적이 감소하는 모양으로 이루어진 경사부를 포함하는 것을 특징으로 하는 질화물계 반도체 발광 소자를 제공한다.

본 발명은 또한 기판상에 질화물계 반도체로 된 활성층과, 이 활성층의 상부 및 하부에 각각 형성된 질화물계 반도체로 된 p형 및 n형 도핑층을 구비하여 이루어진 질화물계 반도체 발광 소자에 있어서, 상기 기판의 적어도 어느 하나의 외측면은, 레이저 가공을 이용한 흠집내기(Scribing) 공정에 의해 경사지게 절개되어, 상기 활성층과 상기 도핑층이 형성되어 있는 방향의 반대쪽 방향으로 갈수록 단면적이 감소하는 모양으로 이루어진 경사부를 포함하는 것을 특징으로 하는 질화물계 반도체 발광 소자를 제공한다.

본 발명에 있어서, 상기 레이저 가공은 펨토세컨드 레이저(Femtosecond Laser)를 이용하는 것이 바람직하다.

본 발명에 있어서, 상기 레이저 가공은 진공 분위기 하에서 행해지는 것이 바람직하다.

본 발명에 있어서, 질화물계 반도체 발광 소자는 질화물계 반도체의 결정 구조에 따른 정삼각형을 기본으로 하여, 이들의 조합으로 이루어진 정삼각형, 평행사변형, 사다리꼴 중 어느 하나의 수평 단면 구조를 갖는 것이 더욱 바람직하다.

본 발명은 또한 기판상에 질화물계 반도체로 된 활성층과, 이 활성층의 상부 및 하부에 각각 형성된 질화물계 반도체로 된 p형 및 n형 도핑층을 포함하여 이루어진 질화물계 반도체 발광 소자의 제조방법에 있어서, 상기 질화물계 반도체 발광 소자가 다수 형성되어 있는 웨이퍼를 개개의 칩으로 자르는 과정에서, 상기 활성층과 상기 도핑층의 외측면에 경사부가 형성되도록 레이저 가공을 이용하여 상기 웨이퍼에 흠집내기(Scribing)를 행하는 흠집내기 공정; 및 상기 흠집내기 공정에 의해 형성된 직선들을 따라 절개(Cleaving)를 행하는 절개 공정을 포함하는 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법을 제공한다.

본 발명은 또한 기판상에 질화물계 반도체로 된 활성층과, 이 활성층의 상부 및 하부에 각각 형성된 질화물계 반도체로 된 p형 및 n형 도핑층을 포함하여 이루어진 질화물계 반도체 발광 소자의 제조방법에 있어서, 상기 질화물계 반도체 발광 소자가 다수 형성되어 있는 웨이퍼를 업사이드 다운(upside-down) 방식으로 개개의 칩으로 자르는 과정에서, 상기 기판의 외측면에 경사부가 형성되도록 레이저 가공을 이용하여 상기 웨이퍼에 흠집내기(Scribing)를 행하는 흠집내기 공정; 및 상기 흠집내기 공정에 의해 형성된 직선들을 따라 절개(Cleaving)를 행하는 절개 공정을 포함하는 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법을 제공한다.

본 발명에 있어서, 상기 레이저 가공은 펨토세컨드 레이저(Femtosecond Laser)를 이용하는 것이 바람직하다.

본 발명에 있어서, 상기 레이저 가공은 진공 분위기 하에서 행해지는 것이 바람직하다. 한편, 상기 레이저 가공이 대기중에서 행해지는 경우, 레이저 가공은 생성되는 부산물을 제거하기 위해 압축 공기 분사 또는 화학 물질 주입 과정과 함께 행해지는 것이 더욱 바람직하다.

본 발명에 있어서, 상기 흠집내기 공정은, 상기 질화물계 반도체의 결정 구조를 따라 제1의 간격을 두고 제1 방향으로 다수의 흠집내기를 행하는 제1 흠집내기 공정과; 상기 질화물계 반도체의 결정 구조를 따라 제2의 간격을 두고 상기 제1 방향과 60° 의 각도를 이루는 제2 방향으로 다수의 흠집내기를 행하는 제2 흠집내기 공정; 및 상기 질화물계 반도체의 결정 구조를 따라 제3의 간격을 두고 상기 제1 방향 및 제2 방향과 각각 60° 의 각도를 이루는 제3 방향으로 다수의 흠집내기를 행하는 제3 흠집내기 공정을 포함하고, 상기 절개 공정은 상기 제1, 제2 및 제3 흠집내기 공정에 의해 형성된 직선들을 따라 절개를 행하는 것이 바람직하다.

본 발명에 있어서, 상기 제1의 간격과 제2의 간격 및 제3의 간격은 모두 동일하게 조정되는 것이 바람직하다.

본 발명에 있어서, 상기 제1의 간격과 제2의 간격은 서로 동일하며, 상기 제3의 간격은 상기 제1의 간격 및 제2의 간격의 1/2로 조정되는 것도 바람직하다.

본 발명에 있어서, 상기 흠집내기 공정은, 상기 질화물계 반도체의 결정 구조를 따라 제1의 간격을 두고 제1 방향으로 다수의 흠집내기를 행하는 제1 흠집내기 공정과; 상기 질화물계 반도체의 결정 구조를 따라 제2의 간격을 두고 상기 제1 방향과 60° 의 각도를 이루는 제2 방향으로 다수의 흠집내기를 행하는 제2 흠집내 기 공정을 포함하고, 상기 절개 공정은 상기 제1 및 제2 흠집내기 공정에 의해 형성된 직선들을 따라 절개를 행하는 절개 공정을 포함하며, 상기 제1의 간격과 상기 제2의 간격은 m:n(m, n은 양의 정수)의 비율을 가질 수 있다.

이하, 본 발명의 바람직한 실시예를 도면을 참조하여 구체적으로 설명하기로 한다.

실시예

이하에서 설명되는 본 발명은 기본적으로 네 가지 측면에서 강조된다. 첫 번째 측면에서는 질화물계 반도체 발광 소자의 기판 상부측 측면- 활성층과 도핑층을 둘러싸는 외측면- 에 경사부가 형성되도록 레이저 가공을 이용한 흠집내기 공정을 웨이퍼 상에 행한 후에 절개하여 소자의 측면 대칭성을 깨뜨림으로써 소자 내부에서 발생되는 광의 순환적인 전반사를 제거하여 광 이용효율을 극대화시킨다.

두 번째 측면에서는 질화물계 반도체 발광 소자가 질화물계 반도체의 결정 구조에 따른 수평 단면 구조를 갖고 그것의 기판 상부측 측면- 활성층과 도핑층을 둘러싸는 외측면- 에 경사부를 구비하도록 레이저 가공을 이용한 흠집내기 공정을 웨이퍼 상에 행한 후에 절개하여 소자의 평면 및 측면 대칭성을 깨뜨림으로써 소자 내부에서 발생되는 광의 순환적인 전반사를 제거하고 광 이용효율을 극대화시킬 뿐만 아니라 소자(칩)의 수율을 종래에 비해 현저히 개선한다.

세 번째 측면에서는 질화물계 반도체 발광 소자의 기판 측면에 경사부가 형성되도록 레이저 가공을 이용한 흠집내기 공정을 업사이드 다운 방식으로 웨이퍼 상에 행한 후에 절개하여 소자의 측면 대칭성을 깨뜨림으로써 소자 내부에서 발생되는 광의 순환적인 전반사를 제거하고 동시에 광 이용효율을 극대화시킨다.

네 번째 측면에서는 질화물계 반도체 발광 소자가 질화물계 반도체의 결정 구조에 따른 수평 단면 구조를 갖고 그의 기판 측면에 경사부가 형성되도록 레이저 가공을 이용한 흠집내기 공정을 업사이드 다운 방식으로 웨이퍼 상에 행한 후에 절개하여 소자의 평면 및 측면 대칭성을 깨뜨림으로써 소자 내부에서 발생되는 광의 순환적인 전반사를 제거하고 광 이용효율을 극대화시킬 뿐만 아니라 소자(칩)의 수율을 종래에 비해 현저히 개선한다.

<실시예 1>

도 3은 본 발명의 제1 실시예에 따른 질화물계 반도체 발광 소자의 구조를 개략적으로 나타낸 사시도이다.

도 3에 도시된 바와 같이, 본 발명의 제1 실시예에 따른 질화물계 반도체 발광 소자(200)는, 사파이어(Al_2O_3) 기판(20) 상에 InGaN 등의 질화물계 반도체로 된 활성층(22)과, 이 활성층(22)의 상부 및 하부에 각각 형성된 GaN 등의 질화물계 반도체로 된 p형 및 n형 도핑층(24, 21)을 구비하여 이루어진다. 또한 전하를 띤 캐리어들의 누적 효율을 증가시키기 위해 보다 에너지 밴드갭을 갖는 AlGaN 등의 클래드층(23)을 활성층(22)과 p형 도핑층(24) 사이에 추가적으로 구비할 수 있다. 그리고 상기한 p형 도핑층(24)의 상부에 형성되는 p형 투명전극(25)과, 이 p형 투명 전극(25) 위에 부분적으로 형성되는 p형 전극(26)과, 상기한 n형 도핑층(21)에 접하여 형성되는 n형 전극(27), 및 기판(20)의 제2 주면(도면에서 아래쪽 면) 상에 형성되는 반사용 금속층(28)이 적절한 형태와 크기로 소정 위치에 구비된다.

특히 본 발명의 제1 실시예에 따른 질화물계 발광 소자(200)는 그 측면- 예를 들면 상기한 활성층(22)과 도핑층(21, 24)을 둘러싸는 외측면 - 에 형성된 경사부(30)를 포함한다. 이러한 경사부(30)는 일관가공(Fabrication) 과정에서 가공된 웨이퍼 상에 오목한 모양으로 흠집(32)을 내는 레이저 가공을 이용한 흠집내기 공정에 의해 형성된다. 이러한 흠집내기 공정에는 예를 들어 펨토세컨드 레이저(Femtosecond Laser) 등의 극초단 레이저가 이용되는 것이 바람직하다. 도 4는 본 발명의 레이저 가공을 이용한 흠집내기 공정을 설명하기 위한 도면이다. 도 4에 도시된 바와 같이, 펨토세컨드 레이저로 질화물계 물질을 가공하면, 그 가공면의 프로파일(profile)은 대략 반원형 또는 반타원형 모양이 된다.

극초단 레이저 가공은 먼저 아주 짧은 펄스 길이 때문에 매우 높은 파워(충격량)를 만들어 낼 수 있으며, 가공 물질로 에너지를 아주 빨리 효과적으로 전달할 수 있어 열 전달 및 확산(thermal diffusion) 현상에 의한 에너지 손실을 극소화할 수 있을 뿐만 아니라 가공중에 물질에 가해질 수 있는 열적 충격이나 변형을 극소화 할 수 있다. 또한 아주 급격한 레이저 가공 문턱선속(very abrupt threshold laser fluence) 특성은 가공 물질의 위치나 결함밀도(defect density) 등에 구애받지 않고 물질을 가공할 수 있게 함으로써 특히 투명물질의 가공시 뛰어난 가공 정확도와 미세도를 확

보할 수 있게 해준다.

예를 들어, 극초단 레이저 가공은 진공 분위기 하에서 강도를 1.6×10 ^{2} mJ/㎠로 하고 스캔 속도를 0.5㎜/sec로 한 펨토세컨드 레이저 선속(laser fluence)을 이용하여 반도체 소자용 질화물계 물질을 가공했을 때, 질화물계 물질에 대략 깊이 13㎛, 폭 20~30㎛의 홈이 얻어지도록 행해질 수 있다. 특히 레이저 가공은 대기중에서 행하는 경우 레이저 가공을 행한 후에 홈의 내부와 주위에 재증착되는 산화 물질이 생성되기 때문에 진공 분위기 하에서 행해질 수 있다.

한편, 위의 예에서와 같이 진공 분위기 하에서 레이저 가공을 실시하지 않고 대기중에서 행하는 경우에는, 압축 공기를 분사하여 산화 부산물을 제거하거나 화학 물질을 주입하여 산화 부산물을 처리할 수 있다.

이와 같이 본 발명에서는 극초단 레이저 가공을 적절하게 행하여 질화물계 반도체 발광 소자(200)의 기판 상부측 측면에 형성된 경사부(30)의 곡선의 기울기를 이 곡선에 접하는 접선의 기울기로 보았을 때 0° 를 초과해서 90° 미만의 범위 내에 있도록 적절하게 조정할 수 있다.

한편, 본 발명의 제1 실시예에 따른 질화물계 반도체 발광 소자는 상술한 구성으로 한정되지 않는다. 예를 들면 도 5에 도시된 바와 같이 가공된 웨이퍼의 홈집내기 공정에서 기판(20)의 소정 부분에까지 홈집(30a)을 형성할 수 있다. 이러한 경우, 홈집(30a)은 사파이어 기판(20)에서는 'V'자 형상으로 형성되고, 기판(20) 상의 질화물계 박막 형성부에서는 반원형 또는 반타원형 모양으로 형성된다. 즉 본 발명은 기판(20)의 소정 부분까지 경사부가 형성된 질화물계 반도체 발광 소자를 포함할 수 있다.

<실시예 2>

도 6은 본 발명의 제2 실시예에 따른 질화물계 반도체 발광 소자의 일예를 개략적으로 나타낸 사시도이고, 도 7a는 본 발명의 제2 실시예에 따른 질화물계 반도체 발광 소자의 다른 예를 개략적으로 나타낸 사시도이며, 도 7b는 도 7a의 평면도이다.

도 6과 도 7a 및 도 7b에 도시된 바와 같이, 본 발명의 제2 실시예에 따른 질화물계 반도체 발광 소자(300, 400)는, 본 발명의 제1 실시예에 따른 질화물계 반도체 발광 소자(200)와 유사하게, 사파이어(Al_2O_3) 기판(20) 상에 InGaN 등의 질화물계 반도체로 된 활성층(22)과, 이 활성층(22)의 상부 및 하부에 각각 형성된 GaN 등의 질화물계 반도체로 된 p형 및 n형 도핑층(24, 21)을 구비하여 이루어진다. 또한 전하를 띤 캐리어들의 누적 효율을 증가시키기 위해 보다 에너지 밴드갭을 갖는 AlGaN 등의 클래드층(23)을 활성층(22)과 p형 도핑층(24) 사이에 추가적으로 구비할 수 있다. 그리고 상기한 p형 도핑층(24)의 상부에 형성되는 p형 투명전극(25)과, 이 p형 투명전극(25) 위에 부분적으로 형성되는 p형 전극(26)과, 상기한 n형 도핑층(21)에 접하여 형성되는 n형 전극(27), 및 기판(20)의 제2 주면(도면에서 아래쪽 면) 상에 형성되는 반사용 금속층(28)이 적절한 형태와 크기로 소정 위치에 구비된다.

또한 본 발명의 제2 실시예에 따른 질화물계 반도체 발광 소자(300, 400)는 상기한 본 발명의 제1 실시예에 따른 질화물계 반도체 발광 소자(200)와 유사하게 기판(20)의 상부측 측면에 형성된 경사부(30)를 구비한다. 이러한 경사부(30)는 제1 실시예의 경우와 유사하게 일관가공 과정에서 웨이퍼 상에 홈집을 내는 레이저 가공을 이용한 홈집내기 공정에 의해 형성된다.

게다가, 본 발명의 제2 실시예에 따른 질화물계 반도체 발광 소자(300, 400)는 상기한 경사부(30)를 구비하는 것 이외에 질화물계 반도체의 결정 구조에 따른 수평 단면 구조를 갖는다. 다시 말해서, 사파이어 기판(20)과 이 기판(20)의 주면 상에 형성된 다수의 질화물계 박막층(21, 22, 23, 24)은 동일한 정육각형 기둥 모양의 결정 구조를 갖는다. 이러한 정육각형 기둥 모양의 결정 구조는 그 수평 단면 구조가 정삼각형 또는 정삼각형이 조합된 형상을 포함한다. 따라서 본 발명의 제2 실시예는 가공된 웨이퍼를 개개의 칩으로 자를 때, 상기한 결정 구조에 따라 정삼각형 또는 정삼각형이 조합된 형상- 평행사변형 또는 마름모꼴 형상- 으로 잘려진 칩(소자)에 의해 달성된다. 물론 본 발명의 제2 실시예에 따른 질화물계 반도체 발광 소자(300, 400)가 다수 가공되어 있는 웨이퍼를 결정 구조에 따라 자를 때에는 각 발광 소자의 기판 상부측 측면에 경사부(30)가 구비되도록 레이저 가공을 이용한 홈집내기 공정을 행해야 한다.

참고로 도 6은 수평 단면 구조가 정삼각형인 경우를 나타내고, 도 7a 및 도 7b는 수평 단면 구조가 평행사변형인 경우를 나타낸다. 또한, 도 6과 도 7a 및 도 7b에 도시된 제2 실시예에 따른 질화물계 반도체 발광 소자의 수평 단면 구조에 있 어서, 예각 꼭지점은 모두 60° 가 되고 둔각 꼭지점은 모두 120° 가 된다.

다음은 본 발명의 제2 실시예에 따른 질화물계 반도체 소자(300, 400)의 상기한 수평 단면 구조에 대한 이론적 근거를 보다 구체적으로 설명한다.

질화갈륨(GaN)을 비롯한 모든 질화물계 반도체는 상기한 바와 같이 기본적으로 정육각형(Hexagonal) 기둥 모양의 결정 구조를 갖는다. 이 기둥의 수평 단면은 정삼각형 여섯개가 모인 구조로 볼 수 있다. 도 8과 도 9는 이를 설명하기

위한 것으로, 도 8은 질화물계 반도체가 가지는 정육각형 기둥 모양의 단위 결정 구조를 나타낸 도면이고, 도 9는 도 8의 단위 결정 구조들이 주기적으로 배열된 질화물계 반도체의 결정 구조를 (0001)면에서 바라본 것을 단순화시켜 나타낸 도면이다. 도 8에서, 각각의 단위벡터에 표시된 숫자들은 결정학에서 일반적으로 사용되는 표시를 따른 것이다.

반면 갈륨비소(GaAs)를 비롯한 다른 대부분의 화합물 반도체들은 정육면체(Cubic) 결정 구조를 가지고 있는데, 이런 정육면체 결정 구조를 가진 화합물 반도체들을 이용하여 발광 다이오드를 만들 때에는 직사각형 모양의 수평 단면을 갖는 직육면체 구조의 발광 다이오드를 제조함에 있어 절삭 공구를 사용하지 않고도 그 정육면체 결정 구조의 특성을 살려서, 칩 제작시 통상적으로 사용되는 흠집내기(Scribing)와 절개(Cleaving)를 통하여 발광 다이오드 칩을 만들기 때문에 기판의 손실이 거의 없다.

그러나 질화물계 반도체를 이용하여 발광 다이오드를 제조할 경우에는 이들의 결정 구조가 정삼각형을 기본으로 하는 정육각형 기둥(Hexagonal System)의 형 태로 되어 있기 때문에 수평 단면의 모양을 직사각형의 형태로 만들기 위해서는 어쩔 수 없이 절삭용 공구를 사용해야만 한다.

본 발명의 특징 중의 하나는 이와 같은 질화물계 반도체의 결정 구조의 특성을 고려한 것으로, 정삼각형을 기본으로 하는 정육각형 기둥의 구조를 가진 반도체들은 정삼각형을 기본으로 하는 수평 단면을 지닌 모양의 발광 다이오드 칩을 만들기 위해서 절삭용 공구를 사용하지 않고도 통상적인 칩 제조방법인 흠집내기(Scribing)와 절개(Cleaving)를 통하여 발광 다이오드를 생산할 수 있다는 것이다.

도 9는 이에 대한 기하학적인 설명으로 여기서 실선들은 결정면들을 수평 단면으로 나타낸 것으로 절개가 쉽게 이루어지는 선들이다. 반면에, 점선들은 직사각형 모양의 수평 단면을 갖는 직육면체 질화물계 반도체 발광 다이오드를 만들기 위해 절삭이 불가피한 선을 나타낸다. 이런 점선들은 절개가 쉽게 이루어지지 않기 때문에 결국 절삭용 공구를 사용하여 절단(cutting)해야만 하는 것이다.

질화물계 반도체 결정 구조를 이용하여 만들 수 있는 발광 다이오드의 수평 단면 구조들의 구체적인 예들이 도 10a 내지 도 10c에 각각 도시되어 있으며, 이에 대하여는 이하에서 보다 구체적으로 나누어 설명하기로 한다.

도 9로부터 알 수 있는 바와 같이, 질화물계 반도체의 결정 구조는 정삼각형을 기본으로 하기 때문에 정삼각형을 이루는 방향으로 절개가 잘 이루어진다. 즉 [2-1-10], [-12-10], [-1-120]의 방향들이 절개가 쉽게 이루어지는 방향들이다. 따라서 이런 정삼각형을 기본으로 하는 형태의 발광 다이오드를 만드는 것이 기판을 불필요하게 소모하지 않고 모두 칩으로 제작해낼 수 있는 가장 효율적인 방법이다.

도 10a는 본 발명의 제2 실시예에 따른 정삼각형 모양의 수평 단면을 갖는 질화물계 반도체 발광 소자의 제조 공정을 설명하기 위한 도면이다.

즉 본 실시예에서는 질화물계 반도체 발광 다이오드를 제조함에 있어, 질화물계 반도체의 결정 구조를 따라 소정의 간격을 두고 [2-1-10]의 방향으로 다수의 흠집내기를 행하고, 역시 질화물계 반도체의 결정 구조를 따라 상기 소정의 간격과 동일한 간격을 두고 상기 [2-1-10]의 방향과 60° 의 각도를 이루는 [-1-120]의 방향으로 다수의 흠집내기를 행하고, 다음에 질화물계 반도체의 결정 구조를 따라 위와 동일한 간격을 두고 상기 [2-1-10]의 방향 및 [-1-120]의 방향과 각각 60° 의 각도를 이루는 [-12-10]의 방향(도면상에서 수평 방향)으로 다수의 흠집내기를 행하는 공정들을 거친 후, 이들 공정에 의해 형성된 직선들을 따라 절개를 행하였다. 얻어진 개개의 정삼형 칩의 측면에는 흠집내기 공정에서 이미 형성된 경사부(30)가 구비되어 있었다.

이와 같은 공정들에 의해 원하는 정삼각형 모양의 수평 단면을 갖고 기판(20)의 상부의 측면이 경사지게 절개된 질화물계 반도체 발광 다이오드 칩들을 얻었다. 또한 여기서 정삼각형 모양의 수평 단면을 갖는 발광 다이오드 칩의 크기는 상기한 흠집내기 간격을 조절함으로써 얼마든지 조절이 가능하다.

도 10b는 본 발명의 제2 실시예에 따른 평행사변형 모양의 수평 단면을 갖는 질화물계 반도체 발광 소자의 제조 공정을 설명하기 위한 도면이다.

즉 본 실시예에서는 질화물계 반도체 발광 다이오드를 제조함에 있어, 질화 물계 반도체의 결정 구조를 따라 소정의 간격을 두고 [2-1-10]의 방향으로 다수의 흠집내기를 행하고, 다음에 질화물계 반도체의 결정 구조를 따라 상기 소정의 간격과 동일한 간격을 두고 상기 [2-1-10]의 방향과 60° 의 각도를 이루는 [-12-10]의 방향(도면상에서 수평 방향)으로 다수의 흠집내기를 행하는 공정들을 거친 후, 이들 공정에 의해 형성된 직선들을 따라 절개를 행하였다.

이와 같은 공정들에 의해 원하는 평행사변형 모양의 수평 단면을 갖고 기판(20)의 상부의 측면이 경사지게 절개된 질화물계 반도체 발광 다이오드 칩들을 얻었다. 또한, 여기서도 평행사변형 모양의 수평 단면을 갖는 발광 다이오드 칩

의 크기는 상기한 흠집내기 간격을 조절함으로써 얼마든지 조절이 가능하다. 한편, 본 실시예에서는 흠집내기 공정에 있어 흠집내기 간격을 동일하게 하였으나, 흠집내기 간격을 m:n(m, n은 양의 정수)의 비율을 갖도록 함으로써 다양한 크기뿐만 아니라 다양한 모양의 평행사변형 모양의 수평 단면을 갖는 발광 다이오드 칩을 제조하는 것도 가능하다.

도 10c는 본 발명의 제2 실시예에 따른 사다리꼴 모양의 수평 단면을 갖는 질화물계 반도체 발광 소자의 제조 공정을 설명하기 위한 도면이다.

본 실시예에서는 상기한 제2 실시예의 삼각형 모양의 수평 단면을 갖는 질화물계 반도체 발광 소자의 제조 공정의 경우와 동일한 공정들에 의해 질화물계 반도체 발광 다이오드를 제조하였다. 다만, 본 실시예에서는 흠집내기 공정에 있어 [2-1-10]의 방향과 [-1-120]의 방향에 대한 흠집내기 간격은 서로 동일하게 하는 반면, [-12-10]의 방향에 대한 흠집내기 간격은 그 절반으로 설정하였다.

이와 같은 공정들에 의해 원하는 사다리꼴 모양의 수평 단면을 갖고 기판(20)의 상부의 측면이 경사지게 절개된 질화물계 반도체 발광 다이오드 칩들을 얻었으며, 이 사다리꼴 면적의 1/3에 해당하는 면적을 가진 정삼각형 모양의 수평 단면 구조를 갖고 기판(20)의 상부의 측면이 경사지게 절개된 칩들도 똑같은 개수로 얻었다. 또한, 여기서도 사다리꼴 및 정삼각형 모양의 수평 단면을 갖고 기판(20) 상부의 측면이 경사지게 절개된 발광 다이오드 칩의 크기는 상기한 흠집내기 간격을 조절함으로써 얼마든지 조절이 가능하다.

이상과 같은 본 발명의 실시예상의 형태들을 기본으로 질화물계 반도체 발광 다이오드를 제조하게 되면 광 이용효율을 극대화시키면서 동시에 웨이퍼의 수율을 극대화시킬 수 있다. 광 이용효율을 극대화시키는 것에 대해서는 이하에서 보다 구체적으로 살펴보기로 한다.

본 발명의 제2 실시예에서와 같은 정삼각형, 평행사변형 또는 사다리꼴 모양의 수평 단면을 갖는 발광 소자-예를 들면 발광 다이오드-의 경우 먼저 활성 영역의 임의의 점광원에서 발생한 빛 중 칩의 수직 경계면을 향해 임계각을 벗어난 전반사 영역으로 입사한 빛들은 일단 모두 반사된다. 그러나 정삼각형, 평행사변형 또는 사다리꼴의 특성상 대칭성이 깨져서 직사각형 수평 단면의 경우에서처럼 영구적인 전반사는 일어나지 않는다. 즉 곧바로 2차, 3차 경계면에서 임계각보다 작은 입사각으로 입사하게 되기 때문에 처음에 전반사되었던 빛이라 하더라도 결국 바깥으로 빠져나오게 된다.

<실시예 3>

도 11a는 본 발명의 제3 실시예에 따른 질화물계 반도체 발광 소자의 정면도이고, 도 11b는 도 11a의 평면도이며, 도 12는 본 발명의 실시예에 따른 질화물계 반도체 발광 소자의 제조 공정에서 흠집내기 공정의 또다른 예를 설명하기 위한 도면이다.

도 11a에 도시된 바와 같이, 본 발명의 제3 실시예에 따른 질화물계 반도체 발광 소자(500)는, 사파이어(Al_2O_3) 기판(20) 상에 InGaN 등의 질화물계 반도체로 된 활성층(22)과, 이 활성층(22)의 상부 및 하부에 각각 형성된 GaN 등의 질화물계 반도체로 된 p형 및 n형 도핑층(24, 21)을 구비하여 이루어진다. 또한 본 실시예에도 제1 및 제2 실시예의 경우와 유사하게 전하를 띤 캐리어들의 누적 효율을 증가시키기 위해 보다 에너지 밴드갭을 갖는 AlGaN 등의 클래드층(미도시)을 활성층(22)과 p형 도핑층(24) 사이에 추가적으로 구비할 수 있다. 그리고 상기한 p형 도핑층(24)의 상부에 부분적으로 형성되는 p형 전극(26)과 상기한 n형 도핑층(21)에 접하여 형성되는 n형 전극(27)이 적절한 위치에 적절한 형태와 크기로 구비된다.

특히 본 발명의 제3 실시예에 따른 질화물계 반도체 발광 소자(500)는 기판(20)의 측면에 형성된 경사부(40)를 포함한다. 이러한 경사부(40)는 상기한 활성층(22)과 도핑층(21, 24)이 형성되어 있는 방향의 반대쪽 방향-도면에서 위쪽 방향-으로 갈수록 단면적이 감소되는 모양으로 이루어진다. 즉, 도 11a 및 도 11b에 도시된 것과 같이, 경사부(40)는 기판(20)이 대략 직사각형 단면 구조를 갖기 때문에 각 측면의 상단부가 중심으로 모여진 모양 또는 동축상에서 단면적이 감소하는 모양으로 형성된다. 또 11b에서 참조부호 12a는 기판(20)의 가장 위쪽 주면을 나타낸다.

또한 경사부(40)는 일관가공 과정에서 가공된 웨이퍼를 업사이드 다운방식으로 놓고 흠집을 내는 레이저를 이용한 흠집내기 공정에 의해 형성된다. 흠집내기 공정은 사파이어 기판에 'V'자 모양의 홈이 형성되도록 펨토세컨드 레이저에 의해 이루어진다. 도 12는 사파이어 기판에 레이저 가공을 이용하여 흠집내기 공정을 행한 예를 나타낸 예시도이고, 여기에서 참조부호 40은 경사부를 나타낸다. 이러한 경사부(40)는 수직 측면을 기준으로 하여 그 기울기가 0° 를 초과해서 90° 미만의 범위 내에 있도록 적절하게 조정된다.

예를 들어, 경사부(40)는 진공 분위기 하에서, 강도를 2.1×10^{4} mJ/㎠로 하고 스캔 속도를 0.025㎜/sec로 한 펨토세컨드 레이저 선속(laser fluence)을 이용하여 사파이어 기판을 가공했을 때, 사파이어 기판에 형성된 깊이 60㎛, 폭 78 ~ 86㎛의 'V'자 모양의 홈에 의해 소정 기울기로 형성된다. 한편, 본 실시예에서는 제1 실시예나 제2 실시예와는 달

리 사파이어 기판을 레이저 가공하기 때문에 부산물로서의 산화물질이 거의 발생되지 않는다. 따라서 레이저 가공을 대기중에서 행해도 크게 문제가 되지 않는다. 게다가, 레이저 가공을 대기중에서 행하는 경우에는 발생된 적은 부산물을 압축 공기나 화학 처리 등을 이용하여 용이하게 제거할 수도 있다.

<실시예 4>

도 13a는 본 발명의 제4 실시예에 따른 질화물계 반도체 발광 소자의 정면도이다.

도 13a에 도시된 바와 같이, 본 발명의 제4 실시예에 따른 질화물계 반도체 발광 소자(600)는, 사파이어(Al_2O_3) 기판(20) 상에 InGaN 등의 질화물계 반도체로 된 활성층(22)과, 이 활성층(22)의 상부 및 하부에 각각 형성된 GaN 등의 질화물계 반도체로 된 p형 및 n형 도핑층(24, 21)을 구비하여 이루어진다. 또한 본 실시예에도 제1, 제2 및 제3 실시예의 경우와 유사하게 전하를 띤 캐리어들의 누적 효율을 증가시키기 위해 보다 에너지 밴드갭을 갖는 AlGaN 등의 클래드층(미도시)을 활성층(22)과 p형 도핑층(24) 사이에 추가적으로 구비할 수 있다. 그리고 상기한 p형 도핑층(24)의 상부에 부분적으로 형성되는 p형 전극(26)과 상기한 n형 도핑층(21)에 접하여 형성되는 n형 전극(27)이 적절한 형태와 크기로 소정 위치에 구비된다.

특히 본 발명의 제4 실시예에 따른 질화물계 반도체 발광 소자(600)는 기판(20)의 측면에 형성된 경사부(40)를 포함한다. 이러한 기판(20)의 측면에 형성된 경사부(40)는 활성층(22)과 도핑층(21, 24)이 형성되어 있는 방향의 반대쪽 방향- 도면에서 위쪽 방향- 으로 갈수록 단면적이 감소되는 모양으로 이루어진다. 도 13b는 도 13a의 평면도이고, 여기에서 참조부호 20a는 기판(20)의 최상부측 표면을 나타낸다. 또한 경사부(40)는 일관가공 과정에서 가공된 웨이퍼를 업사이드 다운방 식으로 놓고 흡집내기를 행하는 레이저 가공을 이용한 흡집내기 공정에 의해 형성된다. 흡집내기 공정에는 제1, 제2 및 제3 실시예에서와 같이 펨토세컨드 레이저를 이용하는 것이 바람직하다.

게다가, 본 실시예에 따른 발광소자(600)는 상기한 경사부(40)를 구비하는 것에 더하여 본 발명의 제2 실시예의 경우와 유사하게 발광 소자(600)가 질화물계 반도체의 결정구조에 따른 수평단면구조를 갖는 것을 특징으로 한다. 도 13b에 도시된 바와 같이 본 발명의 제4 실시예에 따른 발광 소자는 정삼각형 또는 정삼각형이 조합된 모양- 예를 들면 평행사변형, 사다리꼴 모양- 을 갖는다. 도 13b에서 소자의 예각 꼭지점은 모두 60° 가 되고 둔각 꼭지점은 모두 120° 가 된다. 이에 대한 구체적인 설명은 제2 실시예의 수평단면구조에 대한 설명과 중복되므로 생략한다.

다음은 제4 실시예에 따른 질화물계 반도체 발광 소자를 인쇄회로기판에 실장하는 예를 설명한다.

도 14는 본 발명의 실시예에 따른 질화물계 반도체 발광 소자를 전자 소자의 인쇄회로기판 상에 플립칩 본딩 방식으로 실장하는 예를 설명하기 위한 도면이고, 도 15는 도 14에서 전자 소자의 인쇄회로기판 위에 플립칩 본딩되는 발광 소자의 배치를 설명하기 위한 도면이다. 한편, 본 실시예에서는 제4 실시예에 따른 질화물계 반도체 발광 소자(600)가 실장된 경우에 대하여 언급하지만 본 발명은 그러한 구성으로 한정되지 않고, 앞서 언급한 본 발명의 제3 실시예에 따른 질화물계 반도체 발광 소자(500)가 실장되는 경우에도 동일하게 적용된다.

도 14에 도시된 바와 같이, 본 발명의 제4 실시예에 따른 질화물계 반도체 발광 소자(600)가 실장된 전자 소자는 발광 소자(600)와 인쇄회로기판(700) 및 이것들을 전기적으로 연결하는 솔더 범프(74a, 74b) 등의 결합수단을 포함한다. 솔더 범프(74a, 74b)는 발광 소자(600)의 p형 및 n형 전극(26, 27)과 인쇄회로기판(700)의 p형 및 n형 전극 패턴(72a, 72b)과의 사이에 배치된다. 도 15에서와 같이, 인쇄회로기판(700)의 p형 및 n형 전극 패턴(72a, 72b)은 금(Au) 등의 도전성 재료에 의해 소정 형상으로 인쇄회로기판의 주면상에 도포되어 형성된다. 도 15에서 참조부호 27a는 n형 전극 패드 영역을 나타내고, 참조부호 74c와 74d는 더미 솔더 범프(dummy solder bump)를 나타내며, 참조부호 600a는 발광 소자(600)가 놓여지는 위치를 나타낸다. 한편 도면에는 도시하지 않았지만, p형 및 n형 전극 패턴(72a, 72b)은 금(Au) 등의 도전성 재료를 이용한 와이어 본딩에 의해 주변 회로 또는 외부 회로와 전기적으로 연결될 수 있다.

이러한 구성에 의하면, 발광 소자 내에서 생성된 빛은 소자 내부에서 순환적으로 전반사되지 않고 대부분 소자 내의 활성영역을 통해 활성화되어 기판(20)의 상부면(20a)을 통해 방출된다(도 13b 참조). 다시 말하면, 통상의 발광소자에서 사파이어 기판의 두께는 질화물계 물질의 활성영역층의 두께보다 두껍기 때문에 경사부의 각도를 확보하기 상대적으로 쉽다. 또한 사파이어 기판의 굴절률이 질화물계 물질의 굴절률보다 낮기 때문에 빛의 전반사 횟수가 적다. 따라서 제1 실시예나 제2 실시예에서는 질화물계 물질의 활성영역층 내에서 빛이 여러차례 전반사되고 그 가운데 일부가 활성층에 흡수되는 반면, 본 실시예에서와 같이 발광 소자를 업사이드 다운 방식으로 인쇄회로기판 상에 실장하는 경우에는 활성층에 의해 흡수되는 빛이 상대적으로 적기 때문에 광효율이 매우 높아진다. 이같이 본 발명에 의하면 발광 소자에서 생성된 빛을 최대한 바깥으로 뽑아내어 이용하는 것이 가능하다.

이와 같이 본 발명의 제4 실시예에 따른 질화물계 반도체 발광 소자(600)는 소정 모양의 전극 패턴(72a, 72b)이 형성된 인쇄회로기판(700) 상에 솔더 범프(solder bump; 74a, 74b) 등을 통해 플립칩 본딩(Filp- chip bonding) 되는 것

이 바람직하다. 더욱 바람직하게는 위의 제4 실시예에서 언급한 바와 같이 플립칩 본딩되는 발광 소자가 질화물계 반도체의 결정구조에 따른 수평 단면 구조- 정삼각형 또는 정삼각형이 조합된 모양- 를 갖고 동시에 레이저 가공에 의해 경사부를 갖도록 이루어진다.

이상의 실시예에서는 질화물계 반도체 발광 다이오드에 대하여 설명하였으나, 본 발명은 정육각기둥 형태를 가진 질화물계 반도체를 이용하여 제조되는 모든 소자들에 적용될 수 있으므로, 단지 발광 다이오드(LED) 뿐만 아니라 레이저 다이오드(LD) 등의 모든 질화물계 반도체 발광 소자와 전자 소자들의 제작시 칩 생산수율을 최대로 높여줄 수 있는 것이다.

발명의 효과

상기한 바와 같이 본 발명에 의하면, 반도체를 이용한 모든 발광 소자 및 전자 소자들의 칩 제작시, 절삭 공구를 사용하지 않고 레이저 가공을 통한 홈집내기(Scribing)와 절개(Cleaving) 방법을 이용하여 칩을 만들기 때문에 절삭과정을 통해 소모되는 칩의 양을 거의 없게 할 수 있다. 따라서 종래의 기술에 비해 칩 생산수율을 크게 증가시킬 수 있다는 이점이 있다.

뿐만 아니라 발광 소자, 특히 발광 다이오드를 그 측면에 경사부가 구비된 구조로 제조할 경우, 영구적인 전반사 현상을 제거하여 발생한 빛의 양을 최대한 바깥으로 뽑아내어 이용할 수 있게 함으로써 광 이용효율의 극대화를 이룰 수 있으며, 나아가 전력대비 광 이용효율이 증가함에 따라 투입 전류량을 줄여서 발광 소자 자체의 수명을 연장할 수도 있다.

더욱이 질화물계 반도체 발광 소자를 이용하는 경우, 질화물계 반도체의 정육각형(Hexagonal) 기둥 형태의 결정 구조에 따라 소자의 수평 단면 구조가 형성되도록 제조하면서 동시에 레이저 가공을 통한 홈집내기를 한 후 절개하는 과정을 통해 그 측면에 경사부를 형성함으로써, 소자 내부의 순환적인 전반사 현상을 제거하여 광 이용효율을 더욱 극대화시키고 동시에 칩 생산수율을 더욱 크게 증가시킬 수 있다는 이점이 있다.

본 명세서에서 기술된 실시예들은 단지 설명의 목적으로 기재된 것이며, 따라서 당업자들에 의한 이들의 다양한 변형 내지는 사소한 변경은 본 발명의 기술적 사상의 범주에 포함되며 나아가 본 특허청구범위에 속하는 것으로 이해되어야 할 것이다.

(57) 청구의 범위

청구항 1.
기판(20)상에 질화물계 반도체로 된 활성층(22)과, 이 활성층(22)의 상부 및 하부에 각각 형성된 질화물계 반도체로 된 p형 및 n형 도핑층(24, 21)을 구비하여 이루어진 질화물계 반도체 발광 소자(200; 300; 400)에 있어서,

상기 활성층(22)과 상기 도핑층(21, 24)이 형성되어 있는 기판(20)의 상부측 외측면 중 적어도 어느 하나의 외측면은, 레이저 가공을 이용한 홈집내기(Scribing) 공정에 의해 경사지게 잘려지고 상기 기판(20)의 상부측 방향으로 갈수록 단면적이 감소하는 모양으로 이루어진 경사부(30)를 포함하는 것을 특징으로 하는 질화물계 반도체 발광 소자.

청구항 2.
기판(20)상에 질화물계 반도체로 된 활성층(22)과, 이 활성층(22)의 상부 및 하부에 각각 형성된 질화물계 반도체로 된 p형 및 n형 도핑층(24, 21)을 구비하여 이루어진 질화물계 반도체 발광 소자(500; 600)에 있어서,

상기 기판(20)의 적어도 어느 하나의 외측면은, 레이저 가공을 이용한 홈집내기(Scribing) 공정에 의해 경사지게 잘려지고 상기 활성층(22)과 상기 도핑층(21, 24)이 형성되어 있는 방향의 반대쪽 방향으로 갈수록 단면적이 감소하는 모양으로 이루어진 경사부(40)를 포함하는 것을 특징으로 하는 질화물계 반도체 발광 소자.

청구항 3.
제1항 또는 제2항에 있어서,

상기 레이저 가공은 펨토세컨드 레이저(Femtosecond Laser)를 이용하는 것을 특징으로 하는 질화물계 반도체 발광 소자.

청구항 4.
제3항에 있어서,

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상기 레이저 가공은 진공 분위기 하에서 행해지는 것을 특징으로 하는 질화물계 반도체 발광 소자.

청구항 5.
제1항 또는 제2항에 있어서,

질화물계 반도체의 결정 구조에 따른 정삼각형을 기본으로 하여, 이들의 조합으로 이루어진 정삼각형, 평행사변형, 사다리꼴 중 어느 하나의 수평 단면 구조를 갖는 것을 특징으로 하는 질화물계 반도체 발광 소자.

청구항 6.
기판(20)상에 질화물계 반도체로 된 활성층(22)과, 이 활성층(22)의 상부 및 하부에 각각 형성된 질화물계 반도체로 된 p형 및 n형 도핑층(24, 21)을 포함하여 이루어진 질화물계 반도체 발광 소자(200; 300; 400)의 제조방법에 있어서,

상기 질화물계 반도체 발광 소자(200; 300; 400)가 다수 형성되어 있는 웨이퍼를 개개의 칩으로 자르는 과정에서, 상기 활성층(22)과 상기 도핑층(21, 24)의 외측면에 경사부(30)가 형성되도록 레이저 가공을 이용하여 상기 웨이퍼에 흠집내기(Scribing)를 행하는 흠집내기 공정; 및

상기 흠집내기 공정에 의해 형성된 직선들을 따라 절개(Cleaving)를 행하는 절개 공정을 포함하는 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법.

청구항 7.
기판(20)상에 질화물계 반도체로 된 활성층(22)과, 이 활성층(22)의 상부 및 하부에 각각 형성된 질화물계 반도체로 된 p형 및 n형 도핑층(24, 21)을 포함하여 이루어진 질화물계 반도체 발광 소자(500; 600)의 제조방법에 있어서,

상기 질화물계 반도체 발광 소자(500; 600)가 다수 형성되어 있는 웨이퍼를 업사이드 다운(upside-down) 방식으로 개개의 칩으로 자르는 과정에서, 상기 기판(20)의 외측면에 경사부(40)가 형성되도록 레이저 가공을 이용하여 상기 웨이퍼에 흠집내기(Scribing)를 행하는 흠집내기 공정; 및

상기 흠집내기 공정에 의해 형성된 직선들을 따라 절개(Cleaving)를 행하는 절개 공정을 포함하는 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법.

청구항 8.
제6항 또는 제7항에 있어서,

상기 레이저 가공은 펨토세컨드 레이저(Femtosecond Laser)를 이용하는 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법.

청구항 9.
제8항에 있어서,

상기 레이저 가공은 진공 분위기 하에서 행해지는 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법.

청구항 10.
제8항에 있어서,

상기 레이저 가공은 레이저 가공시 생성되는 부산물을 제거하기 위한 압축 공기 분사 또는 화학 물질 주입 과정과 함께 행해지는 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법.

청구항 11.
제6항 또는 제7항에 있어서,

상기 흠집내기 공정은, 상기 질화물계 반도체의 결정 구조를 따라 제1의 간격을 두고 제1 방향으로 다수의 흠집내기(Scribing)를 행하는 제1 흠집내기 공정과; 상기 질화물계 반도체의 결정 구조를 따라 제2의 간격을 두고 상기 제1 방향과 60° 의 각도를 이루는 제2 방향으로 다수의 흠집내기를 행하는 제2 흠집내기 공정; 및 상기 질화물계 반도체의 결정 구조를 따라 제3의 간격을 두고 상기 제1 방향 및 제2 방향과 각각 60° 의 각도를 이루는 제3 방향으로 다수의 흠집내기를 행하는 제3 흠집내기 공정을 포함하고,

상기 절개 공정은 상기 제1, 제2 및 제3 흠집내기 공정에 의해 형성된 직선들을 따라 절개(Cleaving)를 행하는 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법.

청구항 12.
제11항에 있어서,

상기 제1의 간격과 제2의 간격 및 제3의 간격은 모두 동일한 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법.

청구항 13.
제11항에 있어서,

상기 제1의 간격과 제2의 간격은 서로 동일하며, 상기 제3의 간격은 상기 제1의 간격 및 제2의 간격의 1/2인 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법.

청구항 14.
제6항 또는 제7항에 있어서,

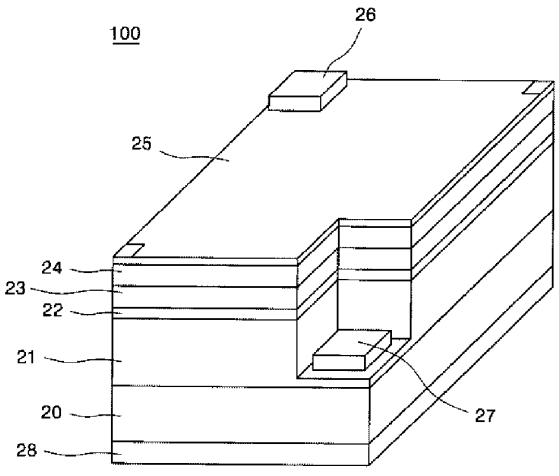
상기 흠집내기 공정은, 상기 질화물계 반도체의 결정 구조를 따라 제1의 간격을 두고 제1 방향으로 다수의 흠집내기(Scribing)를 행하는 제1 흠집내기 공정과; 상기 질화물계 반도체의 결정 구조를 따라 제2의 간격을 두고 상기 제1 방향과 60° 의 각도를 이루는 제2 방향으로 다수의 흠집내기를 행하는 제2 흠집내기 공정을 포함하고,

상기 절개 공정은 상기 제1 및 제2 흠집내기 공정에 의해 형성된 직선들을 따라 절개(Cleaving)를 행하는 절개 공정을 포함하며,

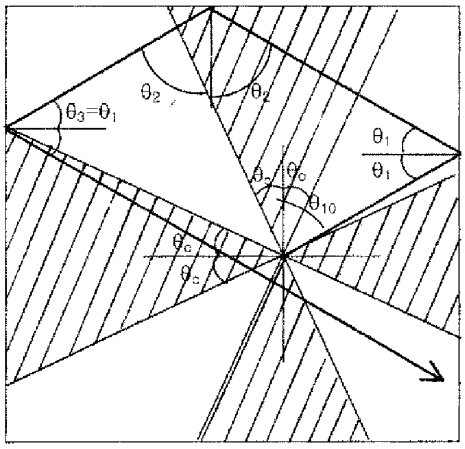
상기 제1의 간격과 상기 제2의 간격은 m:n(m, n은 양의 정수)의 비율을 갖는 것을 특징으로 하는 질화물계 반도체 발광 소자의 제조방법.

도면

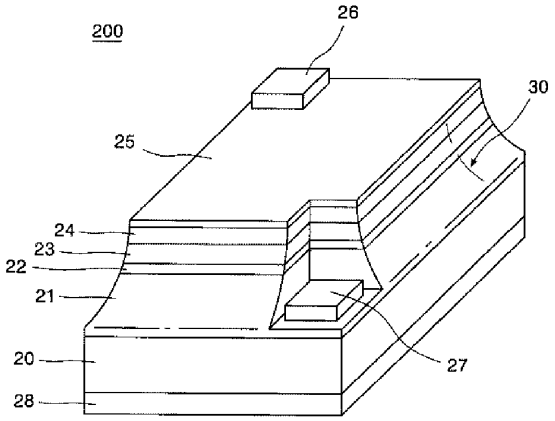
도면1



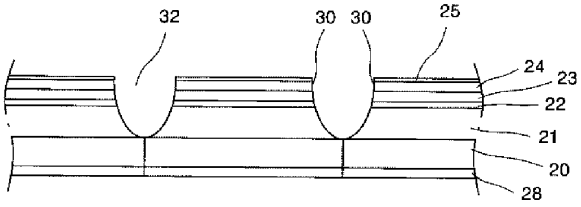
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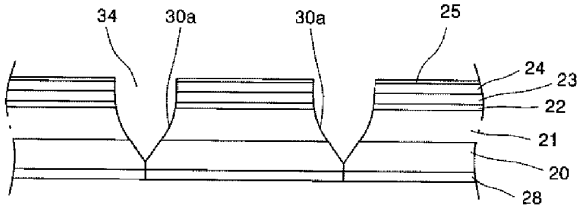
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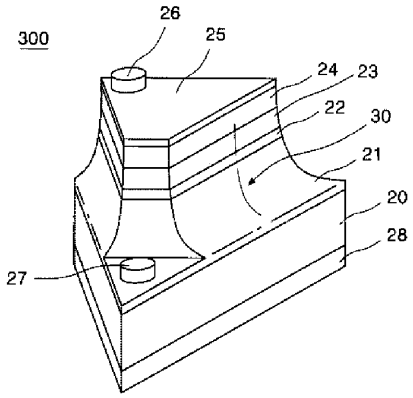
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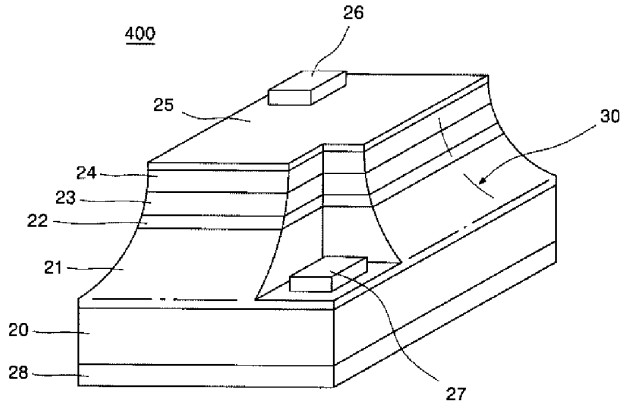
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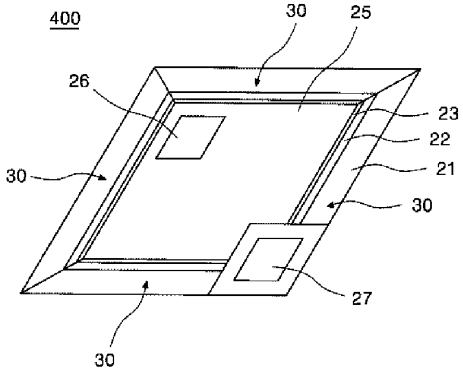
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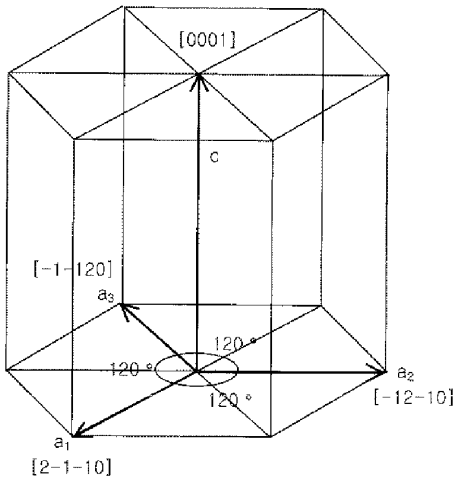
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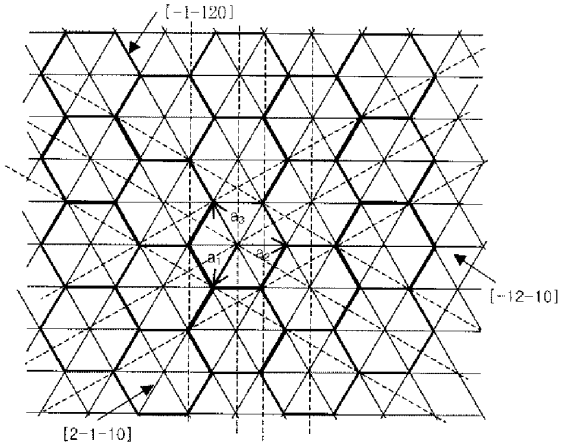
도면7b



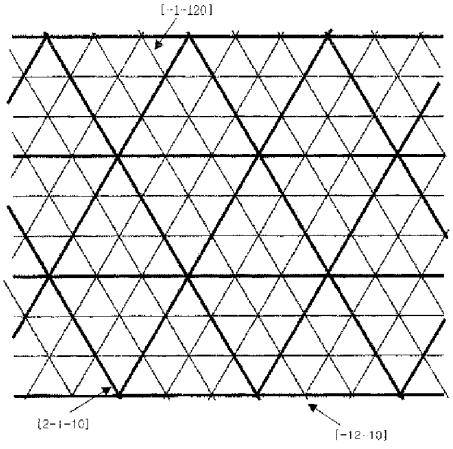
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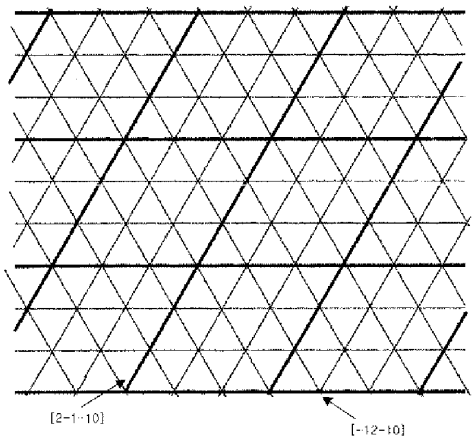
도면9



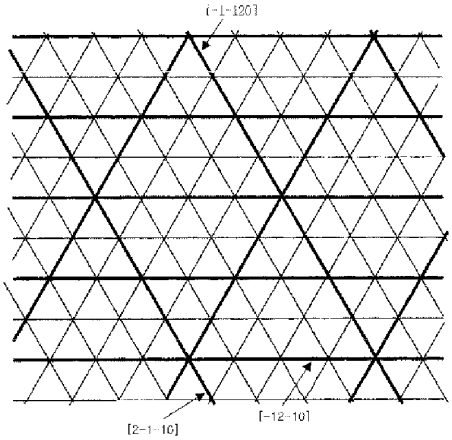
도면10a



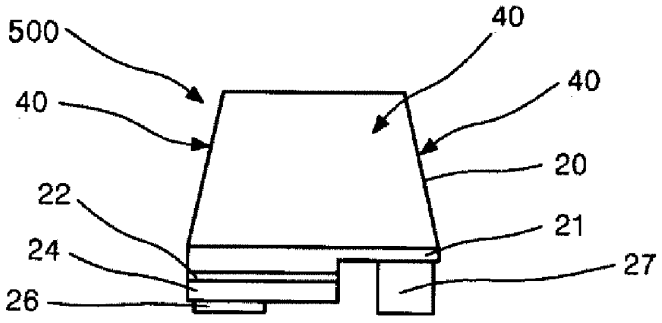
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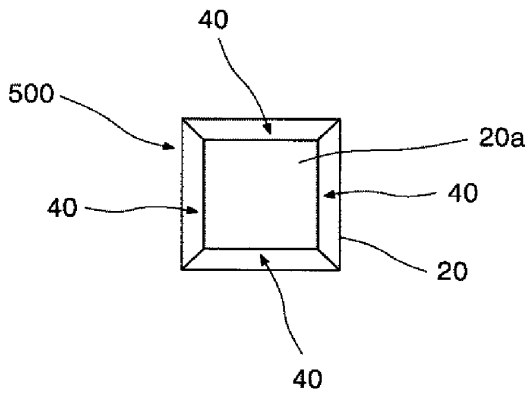
도면10c



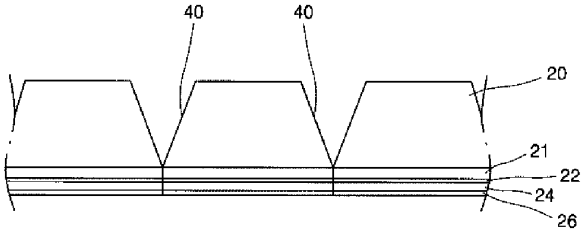
도면11a



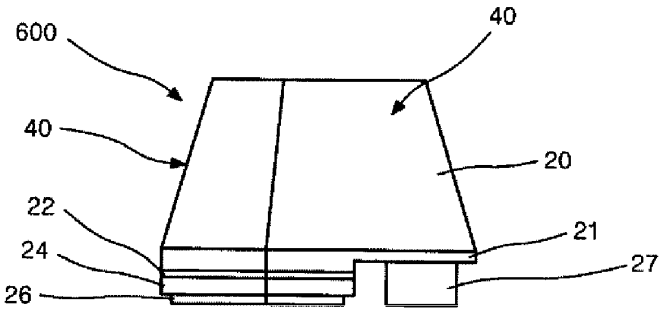
도면11b



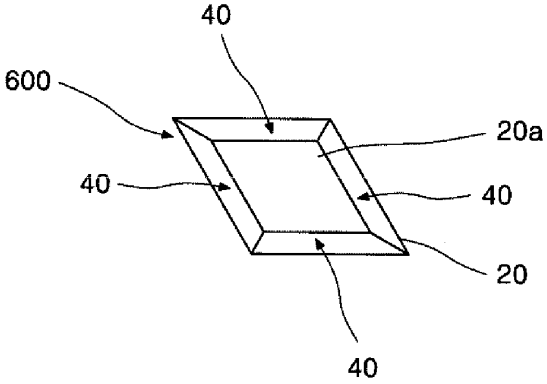
도면12



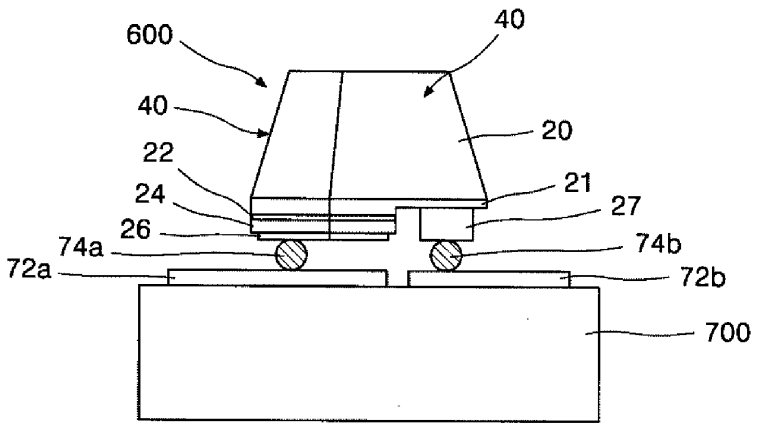
도면13a



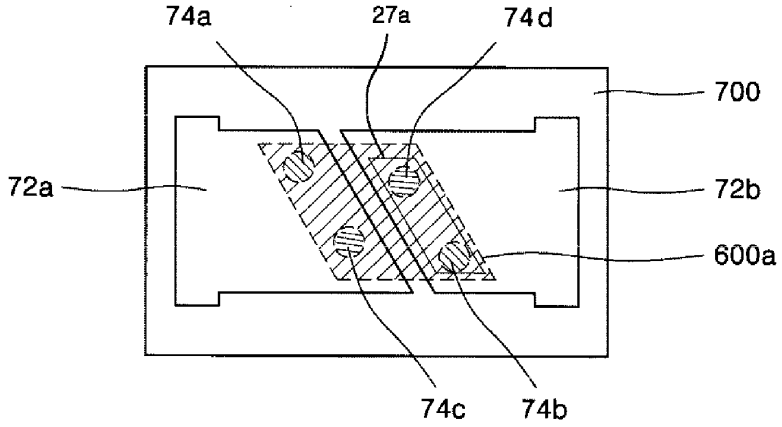
도면13b



도면14


600
40
40
20
22
21
24
27
26
74a
74b
72a
72b
700

도면15


74a
27a
74d
700
72a
72b
600a
74c
74b

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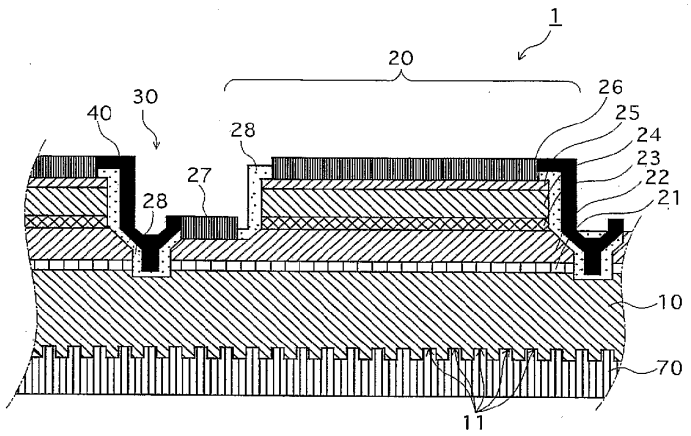
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(54) **Title:** SEMICONDUCTOR LIGHT EMITTING DEVICE, METHOD OF MANUFACTURING THE SAME, AND LIGHTING APPARATUS AND DISPLAY APPARATUS USING THE SAME



(57) **Abstract:** The present invention aims to provide a semiconductor light emitting device that may be firmly attached to a substrate with maintaining excellent light emitting efficiency, and a manufacturing method of the same, and a lighting apparatus and a display apparatus using the same. In order to achieve the above object, the semiconductor light emitting device according to the present invention includes a luminous layer, a light transmission layer disposed over a main surface of the luminous layer, and having depressions on a surface facing away from the luminous layer, and a transmission membrane disposed on the light transmission layer so as to follow contours of the depressions, and light from the luminous layer is irradiated so as to pass through the light transmission layer and the transmission membrane.

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DESCRIPTION

SEMICONDUCTOR LIGHT EMITTING DEVICE, METHOD OF MANUFACTURING THE SAME, AND LIGHTING APPARATUS AND DISPLAY APPARATUS USING THE SAME

Technical Field

The present invention relates to a semiconductor light emitting device and a method of manufacturing the same, as well as a lighting apparatus and a display apparatus using the same.

Background Art

Lighting apparatuses with light emitting diodes (LEDs) have been gaining attention as a new light source because of excellent properties in terms of light emitting efficiency and longevity in comparison with incandescent lamps or halogen lamps. In order to improve light output of this kind of lighting apparatus, a quick solution is to mount LEDs in high density. However, this solution is not very realistic due to current issues regarding production cost and heat dissipation in driving when LEDs are mounted in high density. A more realistic solution in order to enhance the light output is to make luminous efficiency of an LED as high as possible. Various attempts have been made to this end, and two key parameters in making such attempts are Internal Quantum Efficiency (IQE) and External Quantum Efficiency (EQE).

The IQE is a parameter indicating the amount of light generated in a luminous layer of an LED to the amount of electric

power that is supplied to the LED. The IQE is affected by the crystallinity of a semiconductor and the structure of the luminous layer that constitute the LED.

On the other hand, the EQE is a parameter indicating an amount of light emitted outside the LED to the amount of supplied electric power, and expressed by a product of the IQE and light extraction efficiency (a proportion of the amount of light emitted outside the LED in the amount of light generated in the LED). The light extraction efficiency is affected by the shape of a bare chip, the material that covers the bare chip, and the shape of the material. In order to improve the light extraction efficiency, it is common to cover a bare chip with resin so as to minimize the refractive index difference at a boundary between the bare chip and outside of the bare chip as much as possible.

Moreover, in a case of lighting apparatuses using LEDs, it is common for a light extracting surface of a bare chip to have depressions so that an incident angle of light on the light extracting surface is not fixed to one angle, thus improving the light extraction efficiency (Japanese Patent No. 2836687, and *Compound Semiconductor*, Vol.8, No.1, pp.39-42, 2002).

As a method of mounting a bare chip on a mounting substrate, flip-chip bonding as shown in FIG.20 is commonly employed. In the flip-chip bonding as illustrated in FIG.20, a vacuum collet 1300 sticks to a light extracting surface of a bare chip 1100, and the bare chip 1100 is joined with a wiring layer 1210 of a mounting substrate 1200 using ultrasonic bonding. By mounting the bare chip 1100 in this way, the distance between

a light emitting layer of the bare chip 1100 and the mounting substrate 1200 is shortened, thus making it possible to effectively dissipate the heat generated in the light emitting layer. In other words, the flip-chip bonding is very effective for a lighting apparatus that requires LEDs in high density, in order to ensure a high heat dissipation capacity.

However, mounting bare chips having depressions on the light extracting surface using the flip-chip bonding often causes problems such as decreases in positioning accuracy and bonding strength, and destruction of the depressions. Specifically, as shown in an enlarged view in the circle in FIG.20, depressions 1111 make it difficult for the vacuum collet 1300 to stick to the bare chip 1100 without fail, and for ultrasonic waves to propagate from the vacuum collet 1300 to the bare chips 1100 sufficiently for bonding. The same kind of problems also occur in display apparatuses having bare chips.

Disclosure of the Invention

In order to solve the above noted problems, the present invention aims to provide a semiconductor light emitting device that may be firmly attached to a substrate with maintaining excellent light emitting efficiency, and a manufacturing method of the same, and a lighting apparatus and a display apparatus using the same.

In order to achieve the above object, a semiconductor light emitting device having a luminous layer according to the present invention comprises a light transmission layer disposed over a main surface of the luminous layer, and having

depressions on a surface facing away from the luminous layer, and a transmission membrane disposed on the light transmission layer so as to follow contours of the depressions, and light from the luminous layer is irradiated so as to pass through the light transmission layer and the transmission membrane.

The above semiconductor light emitting device has the depressions on a surface of the light transmission layer facing away from the luminous layer. Accordingly, the light emitted from the luminous layer is scattered by the depressions or transmitted efficiently, and thus high light extraction efficiency is maintained, as well as high light emission efficiency. Further, the depressions of the semiconductor light emitting device according to the present invention are filled and covered by the membrane, and therefore it is possible to suppress destruction of the depressions by ultrasonic waves applied when the bare chip is mounted to a mounting substrate. Because of this, with the semiconductor light emitting device according to the present invention, it is possible to obtain high light emission efficiency.

Moreover, with the semiconductor light emitting device according to the present invention, a loss of ultrasonic energy is not large because of the above membrane, even when the chip is mounted to the mounting substrate.

Accordingly, the semiconductor light emitting device according to the present invention has an advantage to be able to firmly attach to the mounting substrate while maintaining a high emission efficiency.

Note that it is possible to mount the chip to the mounting substrate using flip-chip bonding.

The membrane covers the surface so as to follow the contours of the depressions, without including air or gap. Further, by saying the light transmission layer is disposed over the main surface of the luminous layer, it indicates that the light transmission layer may be disposed either directly on the main surface of the luminous layer, or indirectly above the main surface of the luminous layer.

Further, a semiconductor light emitting device usually has a structure that plural layers are formed on the substrate. The above depressions do not necessarily have to be on a surface of a layer out of the plural layers. For example, the depressions may be formed on one of the main surface of the substrate in a case of the semiconductor light emitting device that irradiate light from the luminous layer through the substrate.

When formed irregularly, the depressions serve a function of light diffusion. When the depressions are at a regular interval, a structure of such depressions is called a photonic crystal (PC) or a photonic band gap (PBG) structure, depending on how the depressions are formed. The PC and PBG structures, in general, are a cyclic structure in which depressions and projections appear cyclically at a micoron to $\lambda/4$ (λ is a wavelength in the medium) order on a surface, and have a characteristic that light having a specific wavelength is selectively reflected and transmitted. Therefore, when the semiconductor light emitting device according to the present invention has the light transmission layer having the depression in either the PC or PBG structure, it is possible to realize a function of allowing the light

to be transmitted easily in the light transmission layer.

The above semiconductor light emitting device may be such that the membrane is formed so as to follow the contours of the depressions on the surface of the light transmission layer. However, it is more desirable that the surface of the membrane facing away from the light transmission layer is substantially flat. Specifically, when mounting the above semiconductor light emitting device to a mounting substrate, the vacuum collet sticks to a surface, from which the light is irradiated, of the device, as described above. If the surface to which the vacuum collet sticks is substantially flat, it is possible that the vacuum collet sticks more firmly. Therefore, it is possible to mount the above semiconductor light emitting device to the mounting substrate more accurately.

A main component of the membrane in the above semiconductor light emitting device may be one of polyimide, epoxy, silicone, and glass. When the glass is used as a material of the membrane, it is possible to use glass by the sol-gel method or low-melting glass. Specific examples of the glass material include (1) a glass material using metal alkoxide (such as tetramethoxysilane and tetraethoxysilane) as starting material, (2) a glass material made from polymer ceramic precursor such as perhydropolysilazane, and (3) a glass material made from such as phosphorus oxide and boronic oxide.

With any of the above listed glass materials, it is possible to form a glass layer (membrane) whose upper surface is substantially flat and filling the depressions, by applying the glass material on the depressions using such as potting

and spin-coating, drying the glass material, and baking the glass material at a temperature of several hundred degrees centigrade.

It is also desirable that the membrane contains a luminous substance that is excited by the light from the luminous layer. It is especially desirable for a lighting apparatus using the semiconductor light emitting device according to the present invention, if the luminous substance contained in the membrane is a material that is able to convert the light from the luminous layer into the white light (such as a phosphor material).

In order to maintain high light extracting efficiency for the above semiconductor light emitting device, it is also desirable that the depressions on the surface of the light transmission layer are at an interval equal to or greater than $\lambda/4$, λ being a wavelength of the light from the luminous layer.

The luminous layer of the semiconductor light emitting device is generally disposed over a transmission substrate in a state being sandwiched between plural layers such as clad layers, contact layers, and buffer layers. The present invention may also be such that the light transmission substrate as a part or all of the light transmission layer has the depressions on one of main surfaces. It is desirable that the light transmission substrate is made of a material having a refractive index that is substantially equal to a refractive index of the luminous layer, because it is effective to maintain high light extraction efficiency. Specifically, the material for the light transmission substrate may be selected from a group of GaN, SiC, and AlN.

The above structure that is characteristics to the

present invention may be applied to a light emitting diode device, as well as a Vertical Cavity Surface Emitting Laser device, a Resonant Cavity Light Emitting Diode device, and a Surface Mount Device.

Further, a method of manufacturing the semiconductor light emitting device according to the present invention comprises steps of forming a light transmission layer over a multi-layered body in which the luminous layer is sandwiched between a plurality of layers, the light transmission layer having depressions on a surface facing away from the luminous layer, and forming a transmission membrane on the light transmission layer so as to follow contours of the depressions.

With the above method of manufacturing the semiconductor light emitting device according to the present invention, it is possible to obtain a semiconductor light emitting device having high light extraction efficiency, because the depressions is formed on the surface of the light transmission layer facing away from the luminous layer. Further, the transmission membrane is formed on the light transmission layer so as to fill the depressions, and therefore it is possible to mount the chip firmly with protecting the depressions from destruction when the chip is mounted to the mounting substrate. Specifically, with the above manufacturing method, it is possible to increase the accuracy in mounting when the vacuum collet sticks to the chip, and to reduce a loss of ultrasonic energy in the depressions when the ultrasonic waves are applied.

Accordingly, with the above described method of manufacturing the semiconductor light emitting device

according to the present invention, a semiconductor light emitting device that has high light emitting efficiency and may be attached to the substrate firmly may be obtained.

As described in the above, the depressions may serve different functions according to a state of the depressions. When formed irregularly, the depressions serve a function of light diffusion. When the depressions are formed regularly at a fixed interval, a structure of such depressions is called a photonic crystal (PC) or a photonic band gap (PBG) structure.

In the method of manufacturing the semiconductor light emitting device according to the present invention, it is also desirable that the membrane contains a luminous substance that is excited by the light from the luminous layer. It is especially desirable that the membrane is polished to a preferred thickness so that the device may irradiate the white light having a desirable wavelength.

Further, a lighting apparatus according to the present invention is such that the semiconductor light emitting device according to the present invention is mounted to the mounting substrate.

The above lighting apparatus has the semiconductor light emitting device including the light transmission layer having the depressions on the surface and the membrane that covers the light transmission layer, and therefore it is possible to maintain high light emitting efficiency and to firmly attach the semiconductor light emitting device to the mounting substrate.

Therefore, the lighting apparatus according to the present invention has high light emitting efficiency and stable

quality.

As described above, the semiconductor light emitting device according to the present invention has the light transmission layer having a surface with the depressions is disposed over the luminous layer. Thus, it is possible to maintain high light extracting efficiency as well as high light emitting efficiency. Further, because the membrane is disposed over the surface so as to fill the depressions, it is possible to realize firm attachment without destroying the depressions when the semiconductor light emitting device is mounted to the mounting substrate.

Further, with the method of manufacturing the semiconductor light emitting device according to the present invention, the light transmission layer having a surface with depressions is formed over the luminous layer on a side that the device irradiate the light, and then the membrane is formed so as to follow the contours of the depressions. Therefore, it is possible to manufacture the semiconductor light emitting device having the above described advantages easily.

In addition, the lighting apparatus according to the present invention has high light emitting efficiency and stable quality, because the above explained semiconductor light emitting device is mounted to the mounting substrate.

A main component of the membrane in the above semiconductor light emitting device membrane may be one of polyimide, epoxy, silicone, glass by the sol-gel method, and low-melting glass. Specific examples of the glass material include (1) a glass material using metal alkoxide (such as tetramethoxysilane and tetraethoxysilane) as starting

material, (2) a glass material made from polymer ceramic precursor such as perhydropolysilazane, and (3) a glass material made from such as phosphorus oxide and boronic oxide.

With any of the above listed glass materials, it is possible to form a glass layer (membrane) whose upper surface is substantially flat and filling the depressions, by applying the glass material on the depressions using such as potting and spin-coating, drying the glass material, and baking the glass material at a temperature of several hundred degrees centigrade.

Brief Description Of The Drawings

FIG.1 is a perspective view of a LED chip 1, according to a first embodiment of the present invention.

FIG.2A is a partial sectional view of the LED chip 1.

FIG.2B is a circuit wiring diagram of the LED chip 1.

FIG.3 is a process drawing illustrating a manufacturing process of the LED chip 1.

FIG.4 is a process drawing illustrating a manufacturing process of the LED chip 1.

FIG.5A is a perspective view of a LED module 100 viewed from outside.

FIG.5B is a partial sectional view of the LED module 100.

FIG.6 is a schematic view illustrating a step of flip-chip bonding of the LED chip 1 to a mounting substrate 110.

FIG.7A is a front view of the mounting substrate 110.

FIG.7B is a layout drawing of pads on a LED chip mount unit 1a.

FIG.8A is a partial sectional view of a lighting apparatus 200 according to the first embodiment, and FIG.8B is a bottom view of the same.

FIG.9 illustrates a process drawing illustrating an attachment process of a LED module 100 to a socket 210 of the lighting apparatus 200.

FIG.10 shows emission spectrum of the lighting apparatus 200.

FIG.11A illustrates a partial sectional view of an LED chip 3 according to the second embodiment.

FIG.11B illustrates configuration of a depression 326a of the bare chip 3.

FIG.12 illustrates manufacturing steps of an LED chip 3.

FIG.13A illustrates a partial sectional view of a mounting substrate 410 on which an LED module 3 is mounted, and FIG.13B

FIG.14 shows an emission spectrum of a lighting apparatus having the LED chip 3.

FIG.15A is a perspective view of an LED display apparatus according to a third embodiment of the present invention, and FIG.15B is a sectional view to illustrate a part indicated by B in FIG.15A.

FIG.16A is a perspective view of a Vertical Cavity Surface Emitting Laser (VCSEL) device 7 according to a fourth embodiment according to the present invention, and FIG.16B is a partial sectional view of the VCSEL device 7.

FIG.17 illustrates manufacturing steps of the VCSEL device 7.

FIG.18 also illustrates manufacturing steps of the VCSEL device 7.

FIG.19 is a sectional view illustrating a Surface Mount Device as a modified example.

FIG.20 is a schematic view showing steps in mounting a conventional LED chip 1100 to a mounting substrate 1210.

Best Mode for Carrying Out the Invention

The following describes preferred embodiments of the present invention with reference to the drawings.

[First Embodiment]

In a first embodiment, an LED bare chip (hereinafter referred to as the LED chip) 1 is used as an example of semiconductor light emitting devices.

[Structure of LED Chip 1]

The LED chip 1 is explained with reference to FIGs.1 and 2. FIG.1 shows a perspective view. FIG.2A shows a partial sectional view, and FIG.2B shows a circuit wiring diagram, of the LED chip 1.

As shown by FIG.1, the LED chip 1 is such that plural light-emitting elements 20 are formed on a non-doped GaN substrate 10. The light emitting elements 20 are disposed on the substrate 10 in a matrix of 7 × 5 in x and y directions respectively to form total 35 regions on the substrate. A size of one light emitting element 20 is 285 μm in x direction, and 400 μm in y direction. A size of the LED chip 1 is 2 mm × 2 mm, for example.

Each of the light emitting elements 20 on the LED chip 1 constitutes a diode structure, and is separated from other

light emitting elements 20 by separation grooves 30, and a bridge wiring 40 electrically connects the 35 diode structures in series.

As shown in FIG.1, a cathode electrode 50 and an anode electrode 60 on each of a pair of opposing corners of the LED chip 1. These electrodes 50 and 60 are an n-electrode and a p-electrode, respectively, of the light emitting elements 20 that is positioned at the both edges of the 35 light emitting elements 20 serially connected by the bridge wiring 40.

Further, as shown in an enlarged part in FIG.1, a lower surface of the non-doped GaN substrate 10 has depressions 11, and a membrane 70 covers the depressions. There is no gap between the membrane 70 and the non-doped GaN substrate 10, even at bottoms of the depressions 11. In other words, a surface having depressions of the non-doped GaN substrate 10 is densely covered with the membrane 70.

A negative direction along a z-axis in FIG.1 (downside of the drawing) is a direction in which light from the LED chip 1 is irradiated. The depressions 11 on the substrate 10 are formed in order that the irradiated light is easily diffused or transmitted and to virtually lower the refractive index difference at the boundary (a irradiation surface). Details regarding this are described in the patent and non-patent references cited in the above, and further explanation is not given here.

As shown in FIG.2A, when the LED chip 1 is viewed in section, a GaN buffer layer 21 (30 nm thick), an n-GaN clad layer 22 (Si doped 3×10^{18} cm^{-3}, 2 μm thick), a (InGaN/GaN) ×6 luminous layer 23 (InGaN is 2 nm thick, and GaN is 8 nm),

a p-GaN clad layer 24 (Mg doped 3×10^{19} cm^{-3}, 200 nm thick), and then a p-GaN contact layer 25 (Mg doped 3×10^{19} cm^{-3}, 50 nm thick) are layered on the non-doped GaN substrate 10 in a stated order, and finally p-electrodes 26 made of Rh/Pt/Au are formed on a top of the layers.

The (InGaN/GaN)×6 luminous layer 23 indicates a multiplex quantum well structure luminous layer at 6 periods of InGaN/GaN, and irradiates blue light having a wavelength of 460 nm in driving the LED chip 1.

A refractive index of the non-doped GaN substrate 10 is around 2.5, which is substantially the same as a refractive index of the (InGaN/GaN) × 6 luminous layer 23. Therefore, the non-doped GaN substrate 10 is more effective to improve the light extraction efficiency in comparison with a conventional LED chip that utilizes a sapphire (refractive index = 1.7).

The separation grooves 30 are made so as to reach the non-doped GaN substrate 10, and a Si_3N_4 membrane 28 as an insulating film covers a surface of the separation grooves 30. On the shelf shaped n-GaN clad layer 22, n-electrodes 27 made of Ti/Au are formed at the boundary between the light emitting element 20 and the separation grooves 30. The bridge wiring 40 made of Ti/Pt/Au connects the n-electrodes 27 to the n-electrodes 26 on the light emitting element 20 that is next to the n-electrodes 27, in one-to-one relation.

On the other hand, the non-doped GaN substrate 10 has the minute depressions 11 having a square-shaped cross-section (the depressions are at an interval of 1 μm, for example) on all over the lower surface. By having the depressions 11 on

the surface of the non-doped GaN substrate 10, the irradiated light from the (InGaN/GaN) × 6 luminous layer 23 is easily diffused or transmitted. Further, as described above, the membrane 70 is formed on the surface of the non-doped GaN substrate 10 so as to fill the depressions 11. The membrane 70 is mainly made of polyimide resin that transmits light, and contains yellow phosphor material such as $(Sr, Ba)_2SiO_4:Eu^{2+}$ and ultrafine particles such as SiO_2 dispersed in the membrane. The membrane 70 is formed so as that a surface of the membrane 70 facing away from the luminous layer becomes substantially flat and a thickness is 80 μm at a thinnest part where there is no depression.

A structure of the depressions 11 is called a photonic crystal (PC) or a photonic band gap (PBG) structure, depending on how the depressions are formed, and depressions of such a structure serve a different function other than the light diffusion, i.e. such a structure allows the depressions to transmit light easily.

The thickness of the membrane 70 is set to 80 μm in order that the LED chip 1 as a whole emits white light, by mixing blue exciting light, having a peak wavelength ranged from 400 to 500 nm, from the (InGaN/GaN) × 6 luminous layer 23 and yellow light, having a peak wavelength ranged from 550 to 600 nm, generated from the membrane 70 excited by a part of the blue exciting light.

The depressions 11 of the non-doped GaN substrate 10 are square in the present embodiment, as explained above. However, a shape and size of the depressions are not restricted to the above example as long as the shape and size are set

in a range that improves the light extraction efficiency. Round or honey-comb depressions, or straight-line grooves may be employed, for example. Note that it is desirable that the depressions 11 are formed at an interval of $\lambda/4$ or greater, when the wavelength of the light from the (InGaN/GaN) × 6 luminous layer 23 is λ.

As shown in FIG.2B, the LED chip 1 is such that the 35 light emitting elements 20 are connected in series by the bridge wiring 40 connecting the light emitting elements 20. When supplying the LED chip 1 with a power of 50 mA via the cathode electrode 50 and anode electrode 60, an operational voltage becomes 120 V. When supplying power to the LED chip 1, it is desirable to secure a path to disperse heat generated at the LED chip 1 by connecting to a mounting substrate and such.

Note that, although the LED chip 1 according to the present embodiment has a structure including the plural light emitting elements 20, it is also possible that one LED chip includes only one light emitting element.

[Method of Manufacturing LED Chip 1]

Next, a method of manufacturing the LED chip 1 is explained with reference to FIGs.3 and 4.

As shown in FIG.3A, the GaN buffer layer 21, n-GaN clad layer 22、(InGaN/GaN) × 6 luminous layer 23, p-GaN clad layer 24, and p-GaN contact layer 25 are layered in a stated order on the non-doped GaN substrate 10, which is φ5 cm and 300 μm thick, using Metal Organic Chemical Vapor Deposition (MOCVD).

Next, as shown in FIG.3B, grooves 31 are formed by etching at areas where the separation grooves 30 and n-electrodes 27 are formed. The grooves 31 are as deep as to reach the n-GaN

clad layer 22. In forming the grooves 31, although not shown by the drawings, etching is performed after masking the rest of the areas, and the mask is removed after the grooves 31 are formed.

As shown in FIG.3C, a part of a bottom surface of each of the grooves 31 is further etched. Grooves 32 are thus formed and penetrate the n-GaN buffer layer 21 to reach the non-doped GaN substrate 10. The separation grooves 30 are formed based on the grooves 32. In order to form the grooves 32, it is possible to use a laser instead of etching.

As shown in FIG.3D, the Si_3N_4 membrane 28 is formed so as to cover an entire surface including wall surfaces of the grooves 32. The Si_3N_4 membrane 28 is formed using such as spattering, in order to achieve insulation and surface protection. By covering the surfaces of the grooves 32, the grooves 33 are formed. The grooves 32 make only low cuts in the substrate 10, and very superficial, and therefore the grooves 32 will not break the substrate 10.

Next, as shown in FIG.4E, parts of the Si_3N_4 membrane 28 where the p-electrodes 26 are to be formed are removed by etching, and then films of Rh/Pt/Au are formed by evaporation. Thus, the p-electrodes 26 are formed.

Then, as shown in FIG.4F, parts of the Si_3N_4 membrane 28 where the n-electrodes 27 are to be formed on the shelf part next to each of the separation grooves 30 are removed by etching, and then films of Ti/Au are formed by evaporation. Thus, the n-electrodes 27 are formed. Similarly, the bridge wiring 40 made of Ti/Pt/Au is formed so as to connect each p-electrode 26 and n-electrode 27 of two light emitting

elements 20 that are next to each other.

Manufacturing steps from here are the most characteristic part in the present embodiment.

As shown in FIG.4G, a back surface of the non-doped GaN substrate 10 (downside of the drawing) is polished until thickness becomes 150 μm using lap polish. Then, as shown in an enlarged part of FIG.4G, the depressions 11 are etched on the back surface of the non-doped GaN substrate 10. The depressions 11, as described above, are formed at an interval of 1 μm, and an opening of each depression is rectangular.

As shown in FIG.4H, the polyimide acid solution, containing particles of yellow phosphor material such as $(Sr, Ba)_2SiO_4:Eu^{2+}$, and SiO_2 in a dispersed state, is applied to the back surface of the non-doped GaN substrate 10 on which the depressions 11 are formed. The solution is filled in the depressions 11 so that no air bubble is caused inside. And, after heating and hardening at a temperature of 350 °C, the membrane is formed.

The formed membrane is polished so that the LED chip 1 irradiates white light generated by the light from the (InGaN/GaN) × 6 luminous layer 23 mixed with the light excited by the phosphor material in the membrane. For polishing, lap polishing is performed until the thickness of the membrane becomes 80 μm, for example. By this, the membrane 70 is finished.

As a main component of the membrane 70, it is also possible to use such as an epoxy resin or a hard silicone resin, in addition to the above-mentioned polyimide. In this case, it is possible to harden the membrane by heating at a temperature

150 °C. Further, the thickness of the membrane 70 varies according to a relation between the blue light from the (InGaN/GaN) × 6 luminous layer 23 and a proportion of the yellow phosphor contained in the membrane 70. Therefore, in the polishing step, the membrane 70 is polished to a thickness with which a specific color temperature is obtained without fail.

Finally, although not shown in the drawing, the LED chip 1 is finished by dicing the membrane into individual LED chips 1.

In the present embodiment, the non-doped GaN substrate 10 was used as a substrate. However, it is also possible to use a low cost substrate such that a high resistant layer such as an AlGaN layer is formed on an n-GaN substrate. In this case, it is necessary to form the separation grooves so that the high resistant layer is not removed.

[Structure of LED Module 100]

A LED module 100 having the above LED chip 1 is explained with reference to FIG.5.

As shown in FIG.5A, the LED module 100 comprises a disk shaped composite substrate 110 with a diameter of φ5 cm and three light emitting units 120 provided on the composite substrate 110. The composite substrate 110 includes a notch 110a used when the LED module is attached to the lighting apparatus 200, and terminals 130 and 140 with which power is supplied from the lighting apparatus 200. Although not shown in the drawing, the guiding hole is formed on a substantial center of the composite substrate 110 in order to improve operationality when attached to the lighting apparatus 200.

The three light emitting units 120 on the composite substrate 110 each include the LED chip 1 mounted thereon. Details are explained with reference to a partial sectional view in FIG.5B.

As shown in FIG.5B, the LED chip 1 is mounted at a bottom surface of a depression 111 of the composite substrate 110. The LED chip 1 is mounted to the composite substrate 110 using flip-chip bonding, and has an excellent heat dispersion property. A reflective mirror 150 made of aluminum is formed so as to surround the depression 111 in which the LED chip 1 is mounted. The depression 111 surrounded by the reflective mirror 150 is filled with a resin layer 16, and thereby the LED chip 1 is sealed. Examples of material for the resin layer 160 include a silicon resin and a epoxy resin.

An entire part of the reflective mirror 150 and the resin layer 160 that covers the LED chip 1 are further covered by a lens layer 170. Such as a resin material that can be formed in one-piece by molding and a glass material may be used for the lens layer 170. An internal structure of the LED module 100 is explained using FIG.5B illustrating a sectional view taken at line A-A of FIG.5A.

As shown in an enlarged part of FIG.5B, the p-electrodes 26 and n-electrodes 27 of the LED chip 1 are connected to the wiring layer 114 of the composite substrate 110. In addition to an Au coating applied to a surface of the wiring layer 114, Au layers 180 are inserted between each of the electrodes 26 and 27 and the wiring layer 114. These Au layers are Au bumps that have been disposed on the wiring layer 114 when the LED chip 1 is mounted on the composite substrate 110 by flip-chip

bonding.

Also as shown in an enlarged part of FIG.5B, the composite substrate 110 includes an aluminum layer 112 with 1 mm in thickness, an alumina composite insulating layer 113, and the wiring layer 114 made of copper layered in a stated order. Moreover, although not shown in FIG.5, an alumina composite insulating layer 115 is layered on the wiring layer (See FIG.6).

Thickness of the alumina composite insulating layers 113 and 115 is 100 μm, and thickness of the wiring layer 114 is 25 μm.

The p-electrodes 26 and n-electrodes 27 on the LED chip 1 are mounted on the wiring layer 114 in flip-chip bonding. In FIG.1, predetermined pads on the wiring layer 114 to which the cathode electrode 50 and anode electrode 60 are connected are electrically connected to the terminals 130 and 140, respectively. By this, when driving the LED module 100, power is supplied to the LED chip 1 via the wiring layer 114.

The LED module 100 according to the embodiment of the present invention includes three light emitting units 120, each of which has a structure described above.

While the p-electrodes 26 and n-electrodes 27 on the light emitting elements 20 that are next to each other are connected by the bridge wiring 40 as explained above, the p-electrodes 26 and n-electrodes 27 are connected by being mounted on the composite substrate 110, in order to ensure the connection within the LED chip 1 and to disperse the heat generated in the LED chip 1 to the composite substrate 110 without fail, when driving to emit light.

[Mounting LED Chip 1 to Composite Substrate 110]

Next, a method of mounting the LED chip 1 to the composite substrate 110 with reference to FIG.6 and FIG.7.

As shown in FIG.6, the alumina composite insulating layer 115, which is a top layer of the composite substrate 110, is partially removed at an area where the LED chip 1 is mounted. The composite substrate 110 has areas on which three LED chips 1a, 1b, and 1c are mounted, respectively, as shown in FIG.7A, and the wiring layer 114 connects the positive and negative electrodes of each chip to the terminals 130 and 140, respectively.

As shown in FIG.7B, the wiring layer 114 is, at the areas where LED chips 1a, 1b, and 1c are mounted, patterned to a cathode pad 1151, an anode pad 1152, and island pads 1153 each correspond to each of 35 light emitting elements 20 of the LED chip 1. Among the pads, the cathode pad 1151 and anode pad 1152 are connected to the terminals 130 and 140, respectively, as described above. In addition, Au bumps 180 are formed on each of the pads 1151-1153.

The island pads 1153 have a function to improve the connectivity between the p-electrodes 26 and n-electrodes 27 each on the light emitting elements 20 that are next to each other, as well as a function to transmit the heat generated in the LED chip 1 to the composite substrate 110 at high efficiency. The heat transmitted to the composite substrate 110 is dispersed from the aluminum layer 112 via the wiring layer 114 and alumina composite insulating layer 113. Each of the island pads 1153 is formed independently, and has the above explained important functions.

Back to FIG.6, when the LED chip 1 is mounted to the

composite substrate 110 by flip-chip bonding, a vacuum collet 500 sticks to a surface of the LED chip 1 on which the membrane 70 is formed and then moves down the LED chip 1 till the electrode 26 and 27 come into contact with the Au bumps 180 on the wiring layer 114 of the composite substrate 110. Next, while the electrode 26 and 27 are pressed against the Au bumps 180, ultrasonic waves are applied from the vacuum collet 500. The Au bumps 180 becomes soft by the ultrasonic waves applied to the bumps, and the bonding is finished when application of the ultrasonic waves stops.

As shown in an enlarged part of FIG.6, the membrane 70 is formed on the surface of the LED chip 1 that the vacuum collet 500 sticks to. Because the surface of the membrane 70 that the vacuum collet 500 sticks to is substantially flat as shown in the drawing, it is possible that the vacuum collet 500 sticks to the surface without fail. In addition, the surface that is substantially flat reduces loss of energy in applying the ultrasonic waves from the vacuum collet 500 via the surface.

Further, the membrane 70 also has a function to protect the depressions 11 of the non-doped GaN substrate 10 from being destroyed while the ultrasonic bonding.

[Lighting Apparatus 200 having LED module 100]

A lighting apparatus 200 having a LED module 100 is explained next with reference to FIGs.8 and 9. FIG.8 illustrates a perspective view and a bottom view of the lighting apparatus 200. FIG.9 illustrates an explosion view relating to attachment of the LED module 100.

As shown in FIG.8A, the lighting apparatus 200 comprises

a horn-shaped member 210 and the LED module 100 that is attached inside the horn-shaped member 210. The horn-shaped member 210 includes a power conversion circuit (not shown in the drawings) for converting commercially supplied AC power (100 V and 50/60 Hz, for example) into DC power that is necessary to drive the LED module 100 to emit light.

As shown in FIG.8B, the LED module 100 is disposed so that the aluminum layer 112 of the composite substrate 110 is closely attached to an attaching surface inside the horn-shaped member 210 of the lighting apparatus 200.

Next, as shown in FIG.9, a round depression 211 that corresponds to a shape of the composite substrate 110 of the LED module 100 is formed on the attaching surface of the horn-shaped member 210 to which the LED module 100 is attached. The bottom of the depression 211 is substantially flat, and a female screw (not shown in the drawings) is disposed at a part closer to an opening of the depression 211 on an inside wall. A guide 212 and flexible terminals 213 and 214 are disposed on the inside wall between the female screw and the bottom surface. Positions of the guide 212 and the flexible terminals 213 and 214 correspond, respectively, to positions of the notch 110a and terminals 130 and 140 of the LED module 100. In addition, a guide pin 215 is disposed at a center of the bottom surface of the depression 211 of the horn-shaped member 210.

The flexible terminals 213 and 214 are flexible and not attached to the bottom surface of the depression 211 of the horn-shaped member 210. When inserting the LED module 100 into the depression 211, both the flexible terminals 213 and

214 are flexed along the inside wall of the depression 211 in advance, before inserting the LED module 100.

In order to attach the LED module 100 to the horn-shaped member 210 having the above structure, the guide 212 is inserted into a guiding hole of the LED module 10, and the LED module 100 is set into the bottom surface of the horn-shaped member 210 by fitting the notch 110a along the guide pin 215. Then, when the LED module 100 is placed on the bottom surface of the depression 211 of the horn-shaped member 210, the flexible terminals 213 and 214 that have been flexed along the inside all of the depression 211 are cranked so as to be connected to the terminals 130 and 140 of the LED module 100, respectively. After that, an O-shaped ring 220 is placed at a circumference of the LED module 100, and a ring-shaped screw 230 is screwed into the female screw disposed on the inside wall of the depression 211. When the ring-shaped screw 230 and female screw are fully screwed together, the attachment of the LED module 100 to the horn-shaped member 210 is completed.

In the lighting apparatus 200 according to the present embodiment, silicone grease is applied between a back side of the LED module 100 and the bottom surface of the depression 211 of the horn-shaped member 210 in order to improve the heat dispersion efficiency. In addition, a high reflection finish is applied to an inside wall of a lampshade part of the horn-shaped member 210 in order to extract light from the LED module 100 at a high light extraction efficiency.

In the lighting apparatus 200 having the above structure, a current 150 mA is supplied to the LED module 100 via the terminals 130 and 140 after converting the commercially

supplied AC power into the DC power at the power conversion circuit in the horn-shaped member. In the LED module 100 to which the current is supplied, the three light emitting units 120 emit the white light. At this time, the heat generated in the LED chip 1 is dispersed to the horn-shaped member 210 via the aluminum layer 112 of the composite substrate 110. Therefore, with the lighting apparatus 200, it is possible to suppress deterioration of the LED chip 1 and to maintain high luminous efficiency, even when the LED chip 1 is driven to emit light for an extended length of time.

Further, by high reflection finishing applied the lampshade part of the horn-shaped member 210, more than 90 % of the white light from the LED module 100 is extracted from the lighting apparatus 200.

A spectral distribution of the white light irradiated by the lighting apparatus 200 according to the present embodiment is illustrated in FIG.10. As shown in FIG.10, the lighting apparatus 200 according to the present embodiment irradiates the white light having a color temperature of 5400 K and an average color rendering index (CRI) of 70. A relative intensity of an emission spectrum becomes its peak in vicinity of wavelengths 460 nm and 560 nm, and especially sharp in vicinity of wavelengths 460 nm. A total luminous flux is 1000 lm, and an on-axis luminous intensity is 2000 cd.

With the lighting apparatus 200 according to the present embodiment, the white light is obtained by mixing blue light from the (InGaN/GaN) × 6 luminous layer 23 and yellow light that the membrane 70 emits when excited, and accordingly, the CRI is around 70. However, by having the membrane 70 contain

such as Ca-Al-Si-O-N oxynitride phosphor glass that irradiates red light, it is possible to improve the CRI.

[Advantages of LED Chip 1, LED Module 100 Using LED Chip 1, and Lighting Apparatus 200 Using LED Chip 1]

As described above, the LED chip 1 according to the present embodiment is such that the depressions 11 are disposed on the surface of the non-doped GaN substrate 10 facing away from the luminous layer, and the membrane 70 is formed so as to cover the depressions 11. Accordingly, as in FIG.6, when the LED chip 1 is mounted by flip-chip bonding to the composite substrate 110, the depressions 11 on the non-doped GaN substrate 10 are protected. Further, misalignment of the position when mounting is suppressed, because the vacuum collet 500 sticks to the LED chip 1 firmly in flip-chip bonding. Moreover, when the vacuum collet 500 applies the ultrasonic waves, the membrane 70 prevents the ultrasonic energy from weakening in transmission between the vacuum collet 500 and the LED chip 1, and thus mounting is performed without fail.

With the LED module 100 having the LED chip 1 and the lighting apparatus 200 having the LED chip 1, it is possible to obtain high light extraction efficiency, because the depressions 11 of the non-doped GaN substrate 10 of the LED chip 1 are protected. In addition, the LED module 100 having the LED chip 1 and the lighting apparatus 200 having the LED chip 1 have high light emission efficiency, because the attachment is done firmly when mounting.

Note that the LED chip 1 according to the present embodiment also has an advantage such that there is no obstacle such as an electrode which blocks the light on a side which

light from the luminous layer is irradiated, and therefore a shadow on an irradiated surface will not appear.

[Second Embodiment]

In a second embodiment, a LED chip 3 as an example of the semiconductor light emitting device is explained.

[Structure of LED chip 3]

The LED chip 3 according to the present embodiment has a similar appearance with the LED chip 1 shown in FIG.1. Specifically, light emitting elements 320 each having a size of 285 μm × 400 μm are disposed in a matrix of 7 × 5, and a size of the LED chip 3 is 2 × 2 mm. Below, a structure of the LED chip 3 is explained focusing on differences from the LED chip 1, with reference to FIG.11. FIG.11A illustrates a partial sectional view of the LED chip 3, and FIG.11B illustrates a top view of the LED chip 3 without a membrane 370, which will be explained later.

As shown in FIG.11A, the LED chip 3 is formed in a manner that an AlGaN buffer layer 321 (30 nm thick), an n-$Al_{0.1}Ga_{0.9}N$ clad layer 322 (Si doped 3 × 10^{18} cm^{-3}, 1.5 μm thick), an $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N$ × 5 luminous layer 323 ($In_{0.03}Ga_{0.97}N$ is 3 nm thick, and $Al_{0.05}Ga_{0.95}N$ is 5 nm thick), a p-$Al_{0.1}Ga_{0.9}N$ clad layer 324 (Mg doped 3 × 10^{19} cm^{-3}, 200 nm thick), and a p-GaN contact layer 325 (Mg doped 3 × 10^{19} cm^{-3}, 500 nm thick) are layered on the a non-doped 4H-SiC substrate 310 in a stated order. The $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N$ × 5 luminous layer 323 indicates a multiplex quantum well structure luminous layer with 5 periods of $In_{0.03}Ga_{0.97}N/Al_{0.06}Ga_{0.95}N$, and irradiates near-ultraviolet light having a wavelength of 380 nm in driving the LED chip 3.

A refractive index of the non-doped 4H-SiC substrate 310 is around 2.3, which is substantially the same as a refractive index of the $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N$ × 5 luminous layer 323.

Structures of a separation groove 330, n-electrode 327, an Si_3N_4 membrane328, and a bridge wiring 340 are the same as in the LED chip 1, and not explained here.

As shown in FIG.11B, depressions are not formed on a back surface of the non-doped 4H-SiC substrate 310 of the LED chip 3, and an Ni/Al/Pt/Au layer 380 is formed. Further, a p-electrode 326 made of Ni/Au is formed on the p-GaN contact layer 325, and a plurality of depressions 326a are formed so as to penetrate from a surface of the p-GaN contact layer 325 to the p-electrode 326. Details about these depressions are explained with reference to FIG.11B.

As shown in FIG.11A, the depressions 326a are in a round shape formed at a period of 1 μm, and as described above, the depressions have a function to make light irradiated from the $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N$ × 5 luminous layer 323 is easily dispersed or transmitted. The depressions 326a are formed over an entire area of the p-electrode 326 that irradiates the near-ultraviolet light from the $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N$ × 5 luminous layer 323.

Back to FIG.11A, an upper surface of the LED chip 3 where electrodes 326 and 327 are formed is entirely covered by the transmission membrane 370. Although not shown in the drawing, the membrane 370 is not formed on parts corresponding to a cathode electrode 50 and an anode electrode 60 in FIG.1.

The membrane 370 is 50 μm thick, mainly composed of a

hard silicon resin having light transmissivity, and is formed so as to fill the depressions 326a completely and so that an external surface is substantially flat. Moreover, the membrane 370 contains, in a dispersed state, a phosphor material that is excited to emit light by the near-ultraviolet light from the $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N \times 5$ luminous layer 323, and fine particles of SiO_2. The phosphor material to be selected may be any phosphor material that is excited by the near-ultraviolet light so that the white light is irradiated from the LED chip 3 as a result. Examples of such a phosphor material that may be applied are in the following.

Example 1: A combination of blue phosphor material, green phosphor material, and red phosphor material, emitting blue light, green light, and red light, respectively when excited by the near-ultraviolet light.

Example 2: A combination of the phosphor material in the Example 1, and yellow phosphor material emitting yellow light when excited by the near-ultraviolet light.

Example 3: A combination of blue phosphor material and yellow phosphor material, emitting blue light and yellow light, respectively, when excited by the near-ultraviolet light.

Example 4: A combination of the phosphor material in the Example 3, and red phosphor material emitting red light when excited by the near-ultraviolet light.

Example 5: A combination of blue phosphor material emitting blue light when excited by the near-ultraviolet light, and green phosphor material and red phosphor material, emitting green light and red light, respectively, when excited by the blue light emitted from the blue phosphor material.

Example 6: A combination of blue phosphor material emitting blue light when excited by the near-ultraviolet light, green phosphor material emitting green light when excited by the blue light emitted from the blue phosphor material, and red phosphor material emitting red light when excited by the green light emitted from the green phosphor material.

The above examples are just examples, and do not restrict the present invention. Any other combination with which the white light is obtained from the LED chip 3 may be employed.

In addition, in the above examples, the blue light indicates light having a peak wavelength of light emission falls in a range of 400 nm to 500 nm, the green light indicates light having a peak wavelength of light emission falls in a range of 500 nm to 550 nm, the red light indicates light having a peak wavelength of light emission falls in a range of 600 nm to 680 nm, and the yellow light indicates light having a peak wavelength of light emission falls in a range of 550 nm to 600 nm.

Specifically, the following phosphor materials may be utilized.

Blue Phosphor Material:

$(Ba, Sr)MgAl_{10}O_{17}:Eu^{2+}$

$(Ba, Sr, Ca)_{10}Mg(PO_4)_6Cl_2:Eu^{2+}$

Green Phosphor Material:

$BaMgAl_{10}O_{17}:Eu^{2+}, Mn^{2+}$

$(Ba, Sr)_2SiO_4:Eu^{2+}$

$Y_3(Al, Ga)_5O_{12}:Ce^{3+}$

Yellow Phosphor Material:

$(Y, Gd)_3Al_5O_{12}:Ce^{3+}$

$(Sr, Ba)_2SiO_4:Eu^{2+}$

Red Phosphor Material:

$La_2O_2S:Eu^{3+}$

$CaS:Eu^{2+}$

Moreover, among the substances contained in the membrane 370, SiO_2 is ultrafine particles having a diameter ranged from a couple 10 nm to a couple 100 nm. The following may be used as fine particles contained in the membrane 370, other than SiO_2 as described above: Al_2O_3, ZnO, Y_2O_3, TiO_2, ZrO_2, HfO_2, SnO_2, Ta_2O_3, Nb_2O_3, $BaSO_4$, ZnS, V_2O_5, and a mixture of any of the above substances.

A circuit configuration of the LED chip 3 of the above structure is such that the 35 light emitting elements 320 are connected in series as FIG.2B, and the near-ultraviolet light from the $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N \times 5$ luminous layer 323 is converted into the white light at the membrane 370 and irradiated from the upper surface shown in FIG.11A. Driving voltage of the LED chip 3 is 120 V, when the heat dispersion is ensured and a current of 50 mA is supplied.

[Method of Manufacturing LED Chip 3]

Next, a method of manufacturing the LED chip 3 is explained with reference to FIG.12. In manufacturing the LED chip 3, steps after the step shown in FIG.4F are explained, because the steps from the beginning to FIG.4F are the same as the method of manufacturing the LED chip 1, although material used is not the same.

FIG.12A shows a step at which formation of the p-electrode 326 and n-electrode 327 is completed.

Next, as shown in FIG.12B, the lower surface of the

non-doped 4H-SiC substrate 310 is polished till a thickness of the substrate becomes 150 μm. After the polishing, the Ni/Al/Pt/Au layer 380 is formed on the polished surface using evaporation.

As shown in FIG.12C, the depressions 326a in a pattern shown in FIG.11B are etched to an area where the p-electrode 326 is to be formed. Etching is performed in a manner that a surface of the p-GaN contact layer 325 becomes bottom surfaces of the depressions 326a. The depressions 326a are formed at a period of 1 μm and a shape of openings of the depressions 326a is round.

Then silicon resin containing phosphor material is applied to an entire upper surface of the chip, and the membrane 370 is formed after heating the silicon resin at a temperature of 150 °C and hardening. When applying the silicon resin, a special care needs to be taken so that the depressions 326a does not include air inside. In addition, parts corresponding to the cathode electrode and anode electrode are masked so that the silicon resin is not applied.

Finally, after lap polishing is performed until the thickness of the membrane becomes 50 μm, the manufacturing of the LED chip 3 is completed by dicing the membrane into LED chips.

[Structure of LED module]

A LED module having the above LED chip 3 is explained with reference to FIG.13. FIG.13A illustrates a partial sectional view of the LED module, and FIG.13B illustrates a connection between the LED chip 3 and a wiring layer 414.

As shown in FIG.13A, main components of the LED module

include a ceramics substrate 410 having a depression 411 whose opening has a diameter of φ3 mm, and the LED chip 3 that is connected to a bottom surface of the depression 411. A reflective mirror 450 made of aluminum (thickness: 0.5 mm, diameter of an upper part of an opening: 4 mm) is attached over the ceramics substrate 410 so as to surround the depression 411. A resin layer 460 is filled in the depression 411 surrounded by the reflective mirror 450, so as to firmly fix the LED chip 3. An upper surface of the resin layer 460 is substantially even with an upper surface of the reflective mirror 450, and a lens layer 470 is formed to cover the upper surfaces.

As shown in FIG.13A, the ceramics substrate 410 is a substrate with a diameter of φ5 cm and having a laminated structure. The ceramics substrate 410 is structured such that an AlN layer 412 with 0.5 mm in thickness, the wiring layer 414 that is 25 μm in thickness and made of copper or tungsten with, and a ceramics layer 415 are layered in a stated order on the ceramics substrate 410. At a part where the depression 411 is formed, the ceramics layer 415 as a top layer is removed, and the wiring layer 414 is patterned into two parts, a cathode electrode side and an anode electrode side. Further, an Au coating is applied to a surface of a part (pad) where the wiring layer 414 is exposed because the ceramics layer 415 is removed by the depression 411. Although not shown in the drawing, a lower surface of the ceramics substrate 410 is applied with an Au coating in order to improve the heat dispersion property.

It is possible to use a layer made of Al_2O_3, BN, MgO, ZnO, or SiC for the ceramics substrate 410, instead of the

AlN layer 412.

The LED chip 3 is disposed on the bottom surface of the depression 411 of the ceramics substrate 410, and Au layers 480 are inserted between the Ni/Al/Pt/Au layer 380 and the wiring layer 414 of the ceramics substrate 410. The Au layers are the Au bumps that are placed on the wiring layer 414 when the chip is mounted, as explained already. As shown in FIG.13B, the LED chip 3 is connected onto a cathode pad 414a, which is a larger one of two pads (the cathode pad 414a and anode pad 414b) that are extending from facing sides of the inside wall of the depression 411. The cathode electrode 350 and anode electrode 360 of the LED chip 3 are connected to the cathode pad 414a and anode pad 414b via bonding wires 481 and 482, respectively.

In the present embodiment, the LED chip 3 and the pads 414a and 414b on the ceramics substrate 410 are connected by wire bonding. However, it is also possible, instead of connecting electrically by wire bonding, that the LED chip 3 and the pads are connected using bumps or by soldering, by a metal piece disposed in a penetrating hole in the LED chip 3 so as to dispose an electrode on a back surface of the LED chip 3.

Structures of the reflective mirror 450, the resin layer 460, and the lens layer 470 are the same as in the LED chip 1, and therefore not explained in detail.

Although not shown in the drawing, the LED module according to the present embodiment has substantially the same structure as the LED module in FIG.5, other than the structure of and connection to the LED chip 3. A lighting apparatus

having the LED module may be the same structure as shown in FIG.8, or may have a different structure.

The lighting apparatus having the LED chip 3 according to the present embodiment irradiates white light having a color temperature of 4600 K and an average CRI of 90 by supplying a DC electricity of 150 mA to the LED module. A total luminous flux of this lighting apparatus is 1000 lm, and on-axis luminous intensity is 2000 cd. A spectral distribution of the white light irradiated by the lighting apparatus according to the present embodiment is illustrated in FIG.14.

As shown in FIG.14, a relative intensity of an emission spectrum shows a sharp peak in vicinity of wavelengths 620 nm, and is relatively high in vicinity of wavelengths between 450 nm and 620 nm.

[Advantages of LED Chip 3, LED Module Using LED Chip 3, and Lighting Apparatus Using LED Chip 3]

As described above, the LED chip 3 according to the present embodiment is such that the depressions 326a are on a side of the p-electrode 326 which the near-ultraviolet light from the $In_{0.03}Ga_{0.97}N/Al_{0.05}Ga_{0.95}N \times 5$ luminous layer 323 passes through, and the membrane 370 is formed so as to cover the depressions 326a. When the LED chip 3 is mounted to the ceramics substrate 410, a vacuum collet sticks to the surface of the membrane 370, then the ultrasonic waves are applied after the LED chip 3 is pressed to the ceramics substrate 410. By forming the membrane 370, it is possible to mount the LED chip 3 without fail, because the vacuum collet firmly sticks to the LED chip 3, and the ultrasonic energy is not lost in the depressions 326a of the p-electrode 326. Further, because

the loss of the ultrasonic energy in the depressions 326a is small and the surface of the depressions 326a is protected by the membrane 370, the depressions 326a are not destroyed by application of the ultrasonic waves when the chip is mounted. Such advantages are the same as the case of the first embodiment.

Because of the above advantages that the LED chip 3 has, it is possible that the LED module and the lighting apparatus having the LED chip 3 obtains, as in the case of the first embodiment, high light extraction efficiency and excellent heat dispersion property because the LED chip 3 is firmly attached when mounting. Thus, the LED module and the lighting apparatus having the LED chip 3 have such advantages that high light-emission efficiency and longevity.

Further, as in the LED chip 3 according to the present embodiment, when the p-electrode 326 and n-electrode 327 are disposed on one side, it is necessary, in general, to remove the luminous layer at the part where the n-electrode 327 is disposed, and therefore it is unavoidable that a luminous area becomes smaller. However, in the LED chip 3 according to the present embodiment, the light emitting elements are connected using the bridge wiring 380 in the LED chip 3, and it is possible to make the n-electrode 327 smaller in comparison with a case in which the light emitting elements are connected using bonding wires or bumps (For example, the n-electrode 327 can be 10 μm square, when it is 100 μm square when using bonding wires or bumps). Thus, by using the LED chip 3, the luminous area becomes wider, because it is possible to make an area of the p-electrode 326 under which the luminous layer is formed wider according to an area that the n-electrode 327 is made

smaller.

For example, when a size of each light emitting element of the LED chip is 285 μm × 400 μm, and an overlapping margin for attachment is 25 μm wide from an edge, an effective area becomes 82250 μm^2. Further, the luminous area per light emitting element of the LED chip 3, in which the area of the n-electrode accounts for 10 × 10 μm^2, according to the present embodiment becomes 82250 - 10 × 10 = 82150 μm^2. Calculating in the same way, a luminous area per light emitting element of a conventional LED chip, in which the area of the n-electrode accounts for 100 × 100 μm^2, becomes 72250 μm^2. In comparison, it is clear that the luminous area of the LED chip 3 according to the present embodiment is 1.13 times as large as that of the conventional LED chip.

Moreover, by making the luminous area wider, the current density may be reduced when the same current is supplied as the case in which the luminous area is smaller, and thus it is possible either to suppress the heat, or to increase quantity of light by supplying more current till the level of current density becomes the same as the case of the smaller luminous area.

As described above, the LED chip 3 according to the present embodiment has an advantage that, when the light emitting elements are connected using bridge wiring on the chip, it is possible to increase the luminous area even when the total chip area is the same, in comparison with the case in which the LED chip made of one light emitting element is connected by wire bonding or bumps.

Although the non-doped 4H-SiC substrate 310 is used as

a substrate in the LED chip 3 according to the present embodiment, it is also possible to use a substrate of an n-SiC substrate on which a layer having a high resistance such as an AlGaN layer is formed. In this case, it is necessary that a separating groove does not completely remove the layer having high resistance.

Moreover, if the cathode electrode is connected to the n-SiC substrate in the LED chip 3, it is not necessary to use a bonding wire between the cathode pad and the cathode electrode.

As explained above, when the n-SiC substrate is used in place of the non-doped 4H-SiC substrate, it is possible to disperse the generated heat to the mounting substrate even when the luminous layer comes upper side, because the n-SiC substrate has as high heat conductance as metal.

It is also possible to use sapphire, AlN, and Si for the substrate, even though heat conductance of those material is not as good.

[Third Embodiment]

Next, a structure of an LED display apparatus 6 according to a third embodiment of the present invention is explained with reference to FIG.15.

As shown in FIG.15A, the LED display apparatus 6 according to the present embodiment is such that a reflective mirror 62 and a lens 63 are layered, in a stated order, in an area on a main surface of a composite substrate 61, and 256 light emitting units 66 are formed in 16 × 16 in this area. Connecting terminals 64 and 65 that connect between the LED display apparatus 6 and a driving circuit to drive the LED display

apparatus 6 are formed in the other areas on the main surface of a composite substrate 61. The connecting terminals 64 and 65, respectively, are connected to the LED chip 67 that constitutes each of the light emitting units 66 via wiring layers 615 and 616 formed as a part of the composite substrate 61 (See FIG.15B).

As shown in FIG.15B, the light emitting units 66 of the LED display apparatus 6 has such a structure that the LED chip 67 is attached to a conductive land 617 that is disposed on the main surface of the composite substrate 61, i.e. the LED chip 67 is mounted to the composite substrate 61 by flip-chip bonding. Then, the reflective mirror 62 is disposed so as to surround the LED chip 67, and the lens 63 is formed so as to cover the LED chip 67 and the reflective mirror 62.

The composite substrate 61 is formed by a metal layer 611 and three insulating layers 612-614, and wiring layers 615 and 616 are formed, respectively, between the insulating layer 613 and 614 and between the insulating layers 612 and 613. The conductive land 617 and each of the wiring layers 615 and 616 are connected by a via hole.

As shown in FIG.15B, the LED chip 67 has the same structure as the light emitting element 20 in the LED chip 1 shown in FIG.2. Further, as shown in an enlarged part of FIG.15B, minute depressions 6711 having a square shaped opening are formed on an entire surface of a non-doped GaN substrate 671 on a side that the light is irradiated (upper side in the drawing). The depressions 6711 are formed at an interval of 1 μm, for example.

A membrane 672 is formed on the non-doped GaN substrate

671 so as to fill the depressions 6711. As in the first embodiment, the membrane 672 is mainly made of a polyimide resin having transmissivity, and contains a yellow phosphor material such as $(Sr, Ba)_2SiO_4:Eu^{2+}$, and ultrafine particles such as SiO_2 in a dispersed state. The membrane 672 is formed so as to be 80 μm thick at the thinnest part (parts that do not have the depression 6711), and so that a surface is substantially flat. A structure of the membrane 672 is the same as in a case of the first embodiment.

With the LED display apparatus 6 according to the third embodiment, as in the first embodiment, it is possible to protect the depression 6711 and suppress displacement of the LED chip 67 when the LED chip 67 is mounted to the composite substrate 61 by flip-chip bonding. Further, by having the membrane 672, the ultrasonic energy applied does not become weakened between the vacuum collet and LED chip when the vacuum collet applies the ultrasonic waves.

With the LED display apparatus 6 having the above structure, the depressions 6711 on the non-doped GaN substrate 671 of the LED chip 67 are protected, and thus it is possible to obtain high light extraction efficiency, as well as high light emitting efficiency due to a firm attachment in mounting.

The LED display apparatus 6 according to the present embodiment illustrates an example of the present invention, and the present invention is not restricted by this embodiment. For example, it is possible to use TFT substrate instead of the composite substrate 61.

[Fourth Embodiment]

A structure of a fourth embodiment is explained below,

with reference to FIG.16. In the present embodiment, a Vertical Cavity Surface Emitting Laser (hereinafter referred to as VCSEL) device is taken as an example.

As shown in FIG.16A, a VCSEL device 7 according to the present embodiment is such that a cathode electrode 72 is disposed on one of main surfaces of a SiC substrate 71 (lower surface in FIG.16A), a phosphor layer 74 is formed on a part of the other side of main surfaces (upper surface in FIG.16A), and an anode electrode 75 is disposed on the rest of the same side of main surfaces. A total number of 36 VCSEL cells 73 are formed in the area of the SiC substrate 71 that is covered by the phosphor layer 74. As shown in the drawing by a partial cutout part, an anode electrode 738 (See FIG.16B) of each of the VCSEL cells 73 and the anode electrode 75 disposed on the main surface of the SiC substrate 71 are connected by an Al bridge wiring 76.

As shown by a sectional view of FIG.16B taken at a plane indicated by C-C, there are 6 VCSEL cells 73 at the section of the VCSEL device 7. As shown in an enlarged view of FIG.16B, the VCSEL cell 73 is formed the SiC substrate 71, the cathode electrode 72 that is formed on one of the main surfaces of the SiC substrate 71, and layers that are layered on the other side of the main surfaces on which the phosphor layer 74 is formed. The layers that are layered on the other side of the main surfaces are formed on the SiC substrate 71 such that a semiconductor DBR layer 731, an n-clad layer 732, an active layer having a multiplex quantum well structure (hereinafter referred to as MQW layer) 733, and a p-clad layer 734 are layered in a stated order, and an SiN passivation layer 735 and an

anode electrode 736 are formed so as to enclose a layered part of the above layers. Further, an ITO layer 737 and a dielectric DBR layer are layered in a stated order on a part of a surface of the p-clad layer 734 that is enclosed by the anode electrode 736.

As explained above, each of the VCSEL cells 73 of the VCSEL device 7 is structured by the SiC substrate 71, the cathode electrode 72, and the above-described more than one components 731-738. Further, a characteristics of the above VCSEL device 7 according to the present embodiment is in that the phosphor layer 74 covers an entire part where the VCSEL cells 73 are formed. Specifically, as in the first to third embodiments, covering an entire VCSEL cells 73 by the phosphor layer 74 protects the anode electrode 736 and such of each of the VCSEL cells 73 from being damaged when mounting the VCSEL device 7, and also ensures an accurate mounting. In addition, it is possible to obtain the same effect as in the first and second embodiments.

Next, a method of manufacturing the VCSEL device 7 according to the present embodiment is explained with reference to FIGs.17 and 18. Both FIGs.17 and 18 illustrate the same one of the VCSEL cells 73, for convenience.

As shown in FIG.17A, the semiconductor DBR layer 731, the n-clad layer 732, the MQW layer 733, and the p-clad layer 734 are layered, in a stated order, on one of the main surfaces of the SiC substrate 71.

As shown in FIG.17B, a mask (not shown in the drawing) is formed at an area of a surface of the p-clad layer 734, specifically, an area where the VCSEL cells 73 are formed,

and etching is performed with the n-clad layer 732 as a stopper layer. By this etching, the MQW layer 733 and p-clad layer 734 remain in projections on an area on the surface of the n-clad layer 732.

As shown in FIG.17C, the semiconductor DBR layer 731 and n-clad layer 732 are etched so as to be slightly larger in section than the MQW layer 732 and p-clad layer 734. After this, as shown in FIG.17D, the Al bridge wiring 76 is formed so as to reach the surface of the SiC substrate 71 and a part of the surface of the n-clad layer 734.

As shown in FIG.18E, the SiN passivation layer 735 is formed so as to cover a surface that the Al bridge wiring 76 and n-clad layer 732 remain and the area of the surface the p-clad layer 734.

Next, as shown in FIG.18F, the anode electrode 736 is formed on an area of a surface of the SiN passivation layer 735 and the area of the p-clad layer 734.

As shown in FIG.18G, an ITO layer 737 and a dielectric DBR layer 738 are layered in a stated order at the area of the surface of the p-clad layer 734 surrounded by the anode electrode 736. In addition, as shown in FIG.18H, the cathode electrode 72 is formed on an entire surface of the other main surface of the SiC substrate 71.

Although not shown in the drawing, after a step shown in FIG.18H, the phosphor layer 74 is formed, where necessary, on the surface of the SiC substrate 71 where the above elements 731-738 are formed. Finally, the VCSEL cells 73 of the VCSEL device 7 is completed after the SiC substrate 71 is cut into units as shown in FIG.16.

As described above, in manufacturing the VCSEL device 7, the phosphor layer 74 is formed so as to form an entire area where the VCSEL cells 73 to be formed. The phosphor layer 74 is formed so as that its surface becomes substantially flat. Therefore, an advantageous effect may be obtained because it is possible to mount the VCSEL device 7 to the substrate using the surface of the phosphor layer 74.

Although the present embodiment is explained by taking the VCSEL device as an example, the same effect may be obtained when applied to a Resonant Cavity Light Emitting Diode (RC-LED) that has substantially the same structure as the VCSEL device.

[Other Matters]

The first to fourth embodiments are examples to explain the characteristics of the structures and effects of the present invention, and the present invention is not restricted by these embodiments. For example, in the first and second embodiments, the white light irradiated from each of the light emitting units 120 is generated by the light from the luminous layer mixing with light generated by the luminous substance being excited by the light from the luminous layer. However, it is also possible that either the white light or mono color light is generated using mono-color LED modules, or mixing mono-color LED lights.

Moreover, although the membranes 70 and 370 in the LED chips 1 and 3 contain the phosphor material and such, the phosphor material and such do not necessarily have to be contained. Basically, these membranes are formed in order to allow the vacuum collet to stick to the LED chips 1 and 3 more firmly when the LED chips are mounted, as well as to

reduce the loss in the ultrasonic energy. Thus, whether or not the phosphor material is contained is not an essential part of the present invention.

In addition, the examples of the material to form the membrane 70 listed in the first embodiment are organic resins such as polyimide, epoxy, and silicone. However, it is also possible to use glass by the sol-gel method or low-melting glass for the membrane 70. Specific examples of the glass material include (1) a glass material using metal alkoxide (such as tetramethoxysilane and tetraethoxysilane) as starting material, (2) a glass material made from polymer ceramic precursor such as perhydropolysilazane, and (3) a glass material made from such as phosphorus oxide and boronic oxide.

With any of the above listed glass materials, it is possible to form a glass layer (membrane) whose upper surface is substantially flat and filling the depressions, by applying the glass material on the depressions using such as potting and spin-coating, drying the glass material, and baking the glass material at a temperature of several hundred degrees centigrade.

Further, with the above semiconductor light emitting devices explained in the first to fourth embodiments, the advantages that the vacuum collet firmly sticks to the LED chip may be obtained even without applying the ultrasonic waves when the LED chip is mounted.

It is also possible to modify the structures of the display device 6 and VCSEL device 7 explained in the third and fourth embodiments, respectively, within a scope in which the effects of the present invention may be obtained.

Moreover, the present invention may be applied to a Surface Mount Device (SMD) illustrated in FIG.19. As shown in FIG.19, an SMD 8 to which the present invention is applied is structured so that a pair of external electrodes 82a and 82b are disposed on a mounting substrate 81, and a LED chip 82 is mounted to the electrodes 82a and 82b by flip-chip bonding with bumps therebetween, and the LED chip 82 and electrodes 82a and 82b over the mounting substrate 81 are covered by a resin package 85.

As shown in an enlarged part in FIG.19, the LED chip 82 of the SMD 8, like the LED chip 67 in the second embodiment described above, has a surface with depressions 8311, and a membrane 8322 covers the LED chip 67 so as to fill the depressions. With the SDM 8 having the above structure, it is possible to obtain the same effects as the above first to fourth embodiments, because damages to the depressions in mounting the LED chip 82 to the mounting substrate 81 may be reduced.

Industrial Applicability

The present invention is effective to realize a high power semiconductor light emitting device having high light output, and a lighting apparatus and a display device using such a semiconductor light emitting device.

CLAIMS

1. A semiconductor light emitting device having a luminous layer, comprising:

a light transmission layer disposed over a main surface of the luminous layer, and having depressions on a surface facing away from the luminous layer; and

a transmission membrane disposed on the light transmission layer so as to follow contours of the depressions, wherein

light from the luminous layer is irradiated so as to pass through the light transmission layer and the transmission membrane.

2. A semiconductor light emitting device according to Claim 1, wherein a surface of the membrane facing away from the light transmission layer is substantially flat.

3. A semiconductor light emitting device according to Claim 1, wherein a main component of the membrane is one of polyimide, epoxy, and silicone.

4. A semiconductor light emitting device according to Claim 1, wherein a main component of the membrane is glass.

5. A semiconductor light emitting device according to Claim 1, wherein the membrane contains a luminous substance that

is excitable by the light from the luminous layer.

6. A semiconductor light emitting device according to Claim 5, wherein the light from the luminous layer is converted into white light by passing through the membrane.

7. A semiconductor light emitting device according to Claim 5, irradiating white light generated by light from the luminous substance being excited mixing with the light from the luminous layer.

8. A semiconductor light emitting device according to Claim 1, wherein the depressions are at an interval equal to or greater than $\lambda/4$, λ being a wavelength of the light from the luminous layer.

9. A semiconductor light emitting device according to Claim 1, wherein

the light transmission layer is formed from at least a light transmission substrate, and

the luminous layer is sandwiched between a plurality of layers and is disposed over the light transmission substrate.

10. A semiconductor light emitting device according to Claim 9, wherein the depressions are on a main surface of the light transmission substrate facing away from the luminous layer.

11. A semiconductor light emitting device according to Claim 9, wherein the light transmission substrate is made of a material having a refractive index that is substantially equal to a refractive index of the luminous layer.

12. A semiconductor light emitting device according to Claim 11, wherein the material for the light transmission substrate is selected from a group of GaN, SiC, and AlN.

13. A semiconductor light emitting device according to Claim 9, wherein a reflective film is disposed on a surface of the luminous layer facing away from the light transmission layer.

14. A semiconductor light emitting device according to Claim 1, being a light emitting diode device.

15. A semiconductor light emitting device according to Claim 1, being a Vertical Cavity Surface Emitting Laser device.

16. A semiconductor light emitting device according to Claim 1, being a Resonant Cavity Light Emitting Diode device.

17. A semiconductor light emitting device according to Claim 1, being a Surface Mount Device.

18. A lighting apparatus comprising a mounting substrate, and a semiconductor light emitting device mounted on a pad

on a surface of the mounting substrate, wherein:

the semiconductor light emitting device includes;

a luminous layer;

a light transmission layer disposed over a main surface of the luminous layer, and having depressions on a surface facing away from the luminous layer; and

a transmission membrane disposed on the light transmission layer so as to follow contours of the depressions, and

light from the luminous layer is irradiated so as to pass through the light transmission layer and the transmission membrane.

19. A lighting apparatus according to Claim 18, wherein a surface of the membrane facing away from the light transmission layer is substantially flat.

20. A lighting apparatus according to Claim 18, wherein a main component of the membrane is glass.

21. A display apparatus comprising a mounting substrate, and a plurality of semiconductor light emitting devices each mounted on a pad on a surface of the mounting substrate, wherein

each of the semiconductor light emitting devices includes:

a luminous layer;

a light transmission layer disposed over a main surface

of the luminous layer, and having depressions on a surface facing away from the luminous layer; and

a transmission membrane disposed on the light transmission layer so as to follow contours of the depressions, and

light from the luminous layer is irradiated so as to pass through the light transmission layer and the transmission membrane.

22. A display apparatus according to Claim 21, wherein a surface of the membrane facing away from the light transmission layer is substantially flat.

23. A display apparatus according to Claim 21, wherein a main component of the membrane is glass.

24. A method of manufacturing a semiconductor light emitting device, comprising steps of:

forming a light transmission layer over a multi-layered body in which the luminous layer is sandwiched between a plurality of layers, the light transmission layer having depressions on a surface facing away from the luminous layer; and

forming a transmission membrane on the light transmission layer so as to follow contours of the depressions.

25. A method of manufacturing a semiconductor light emitting

device according to Claim 24, wherein a material that forms the membrane contains a luminous substance that is excitable by the light from the luminous layer.

26. A method of manufacturing a semiconductor light emitting device according to Claim 25, further comprising a step of:

polishing the membrane after forming the membrane, till a thickness of the membrane becomes such that irradiated light is desirable white light.

27. A method of manufacturing a semiconductor light emitting device according to Claim 24, wherein a material that forms the membrane contains one of polyimide, epoxy, and silicone.

28. A method of manufacturing a semiconductor light emitting device according to Claim 24, wherein a material that forms the membrane contains glass.

29. A method of manufacturing a semiconductor light emitting device according to Claim 24, wherein

the light transmission layer includes at least a light transmission substrate, and

the depressions are on a main surface of the light transmission substrate facing away from the luminous layer.

30. A method of manufacturing a semiconductor light emitting device according to Claim 29, wherein the light transmission

substrate is formed by a material selected from a group of GaN, SiC, and AlN.

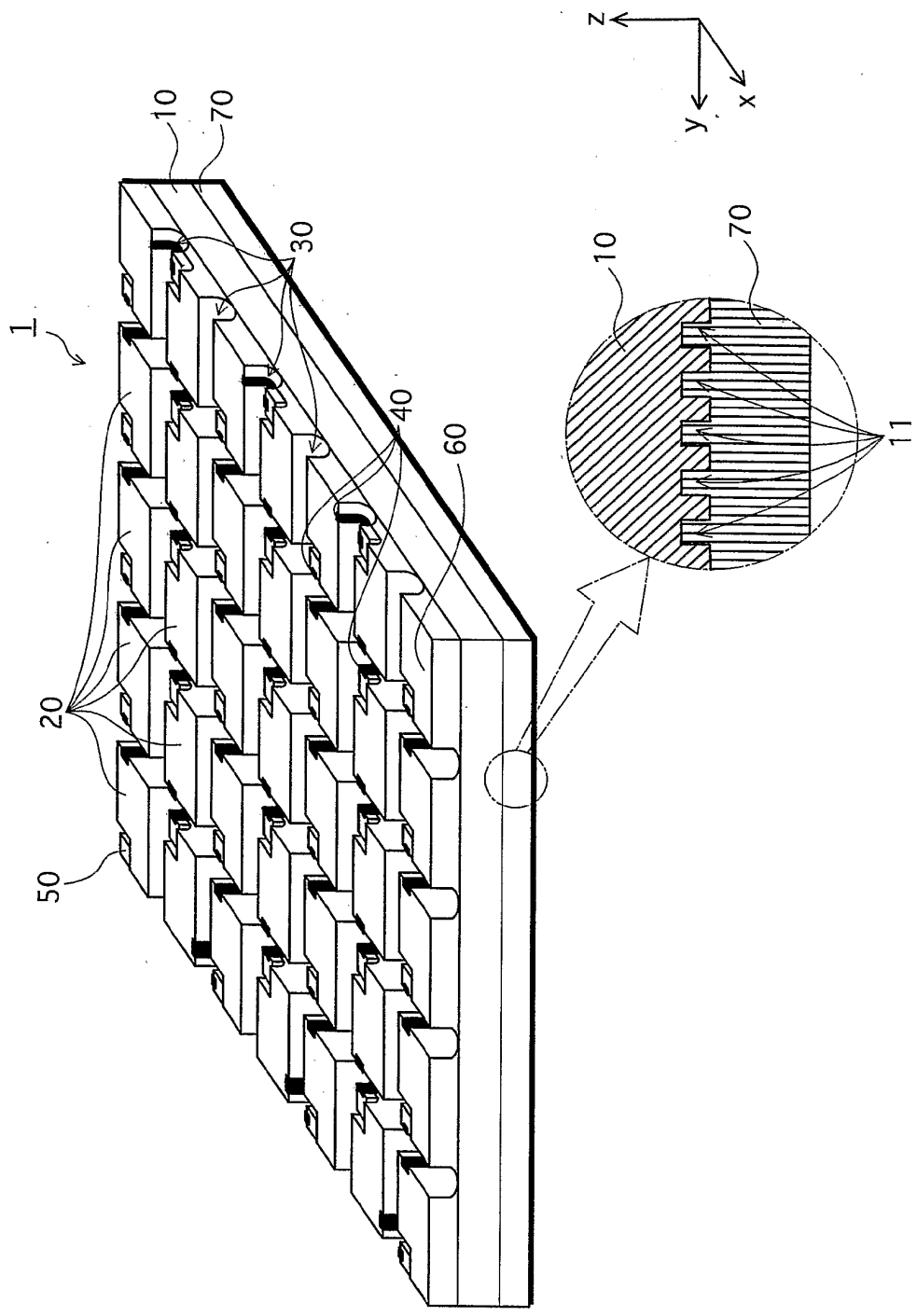


FIG.1

FIG.2A

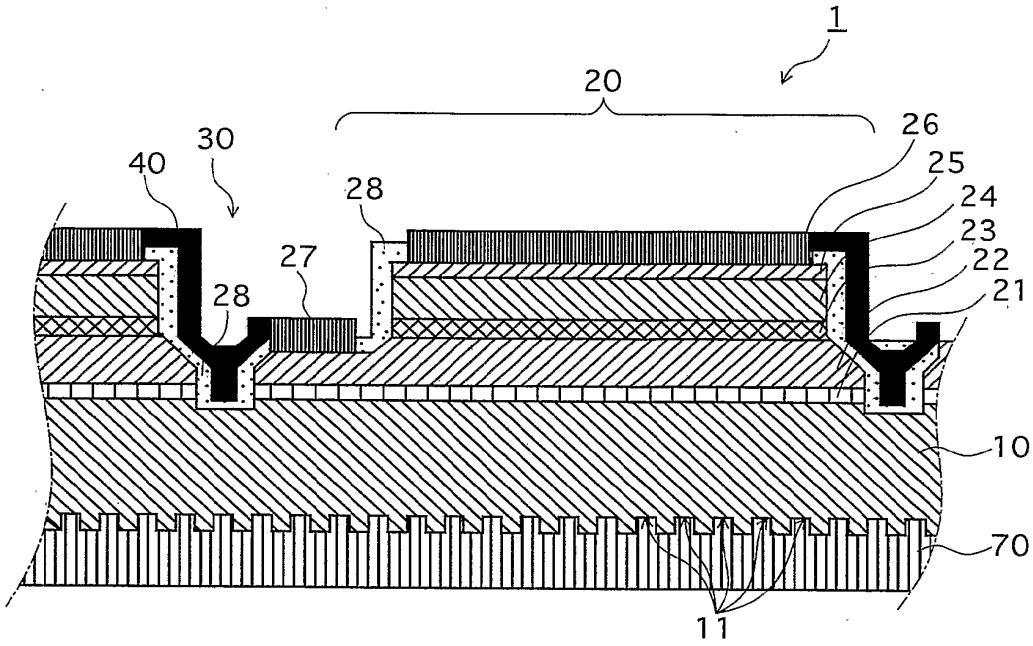


FIG.2B

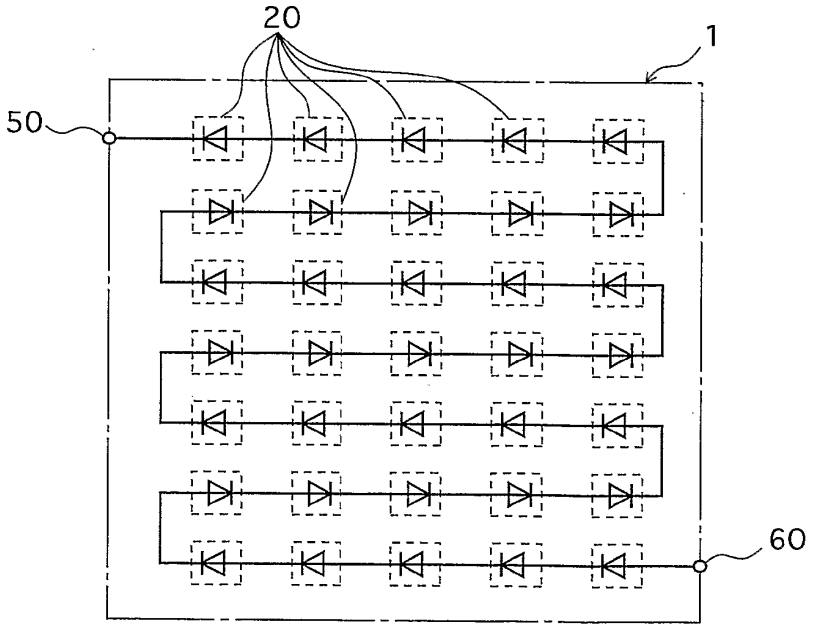


FIG.3A

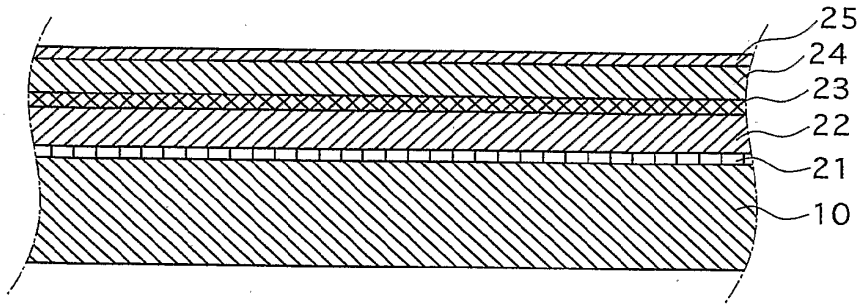


FIG.3B

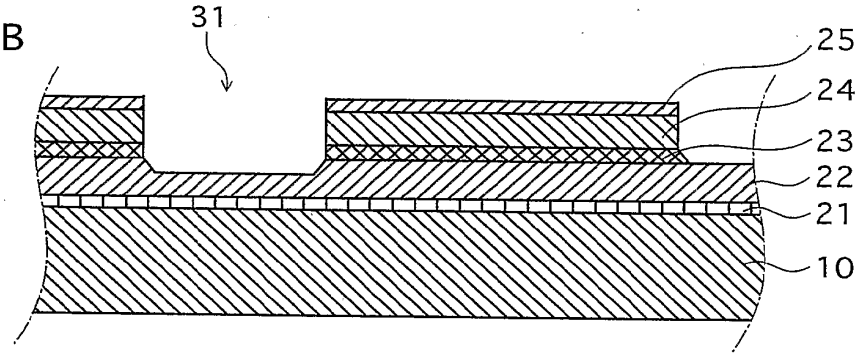


FIG.3C

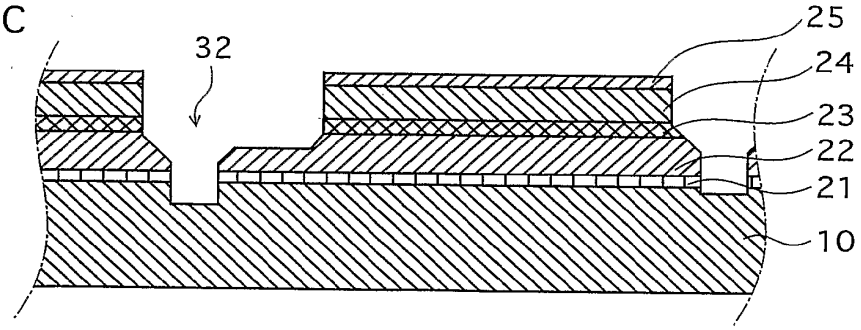


FIG.3D

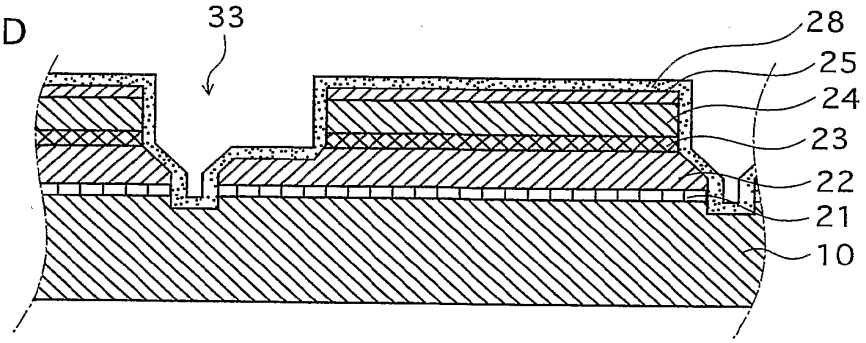


FIG.4E

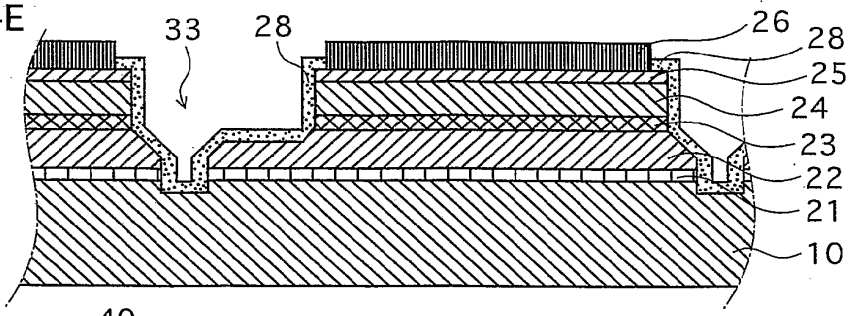


FIG.4F

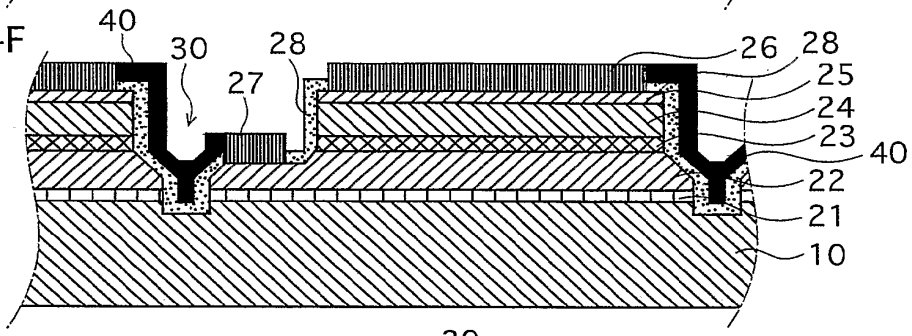


FIG.4G

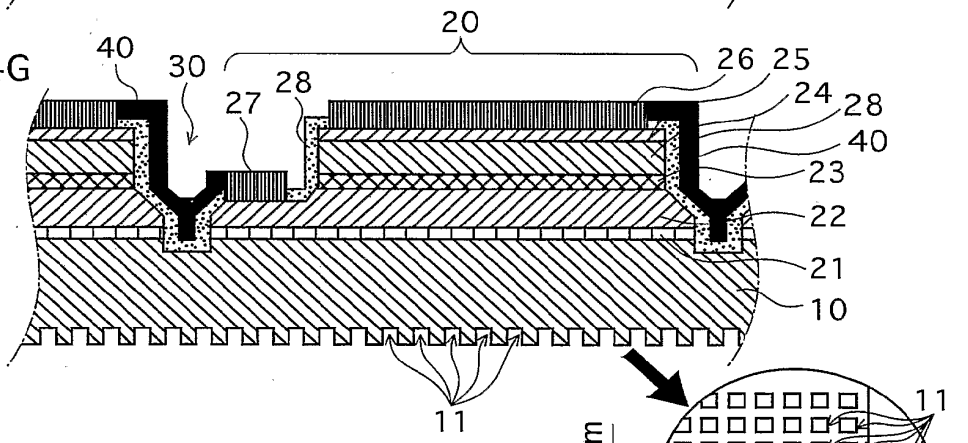


FIG.4H

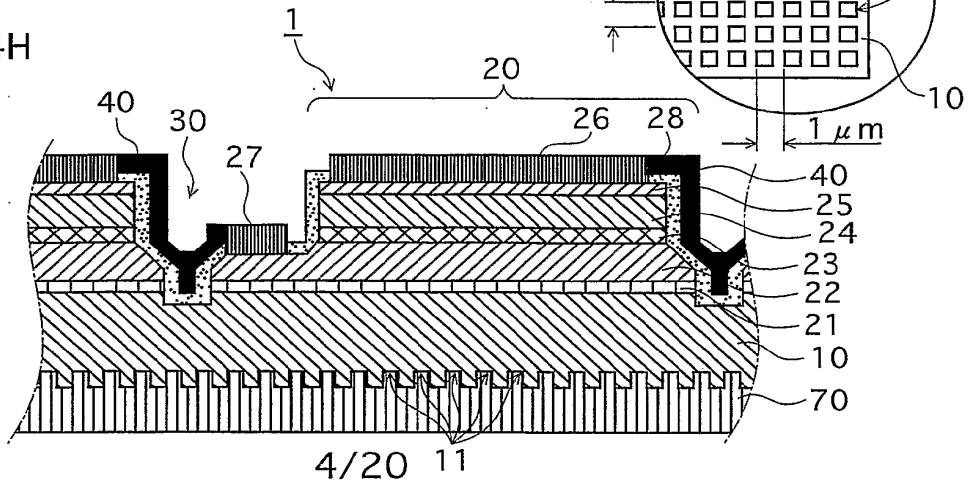


FIG.5A

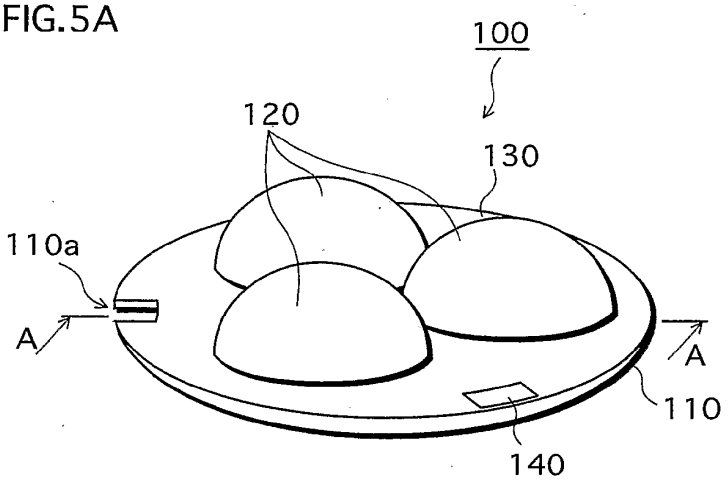

100
120
130
110a
A
A
110
140

FIG.5B

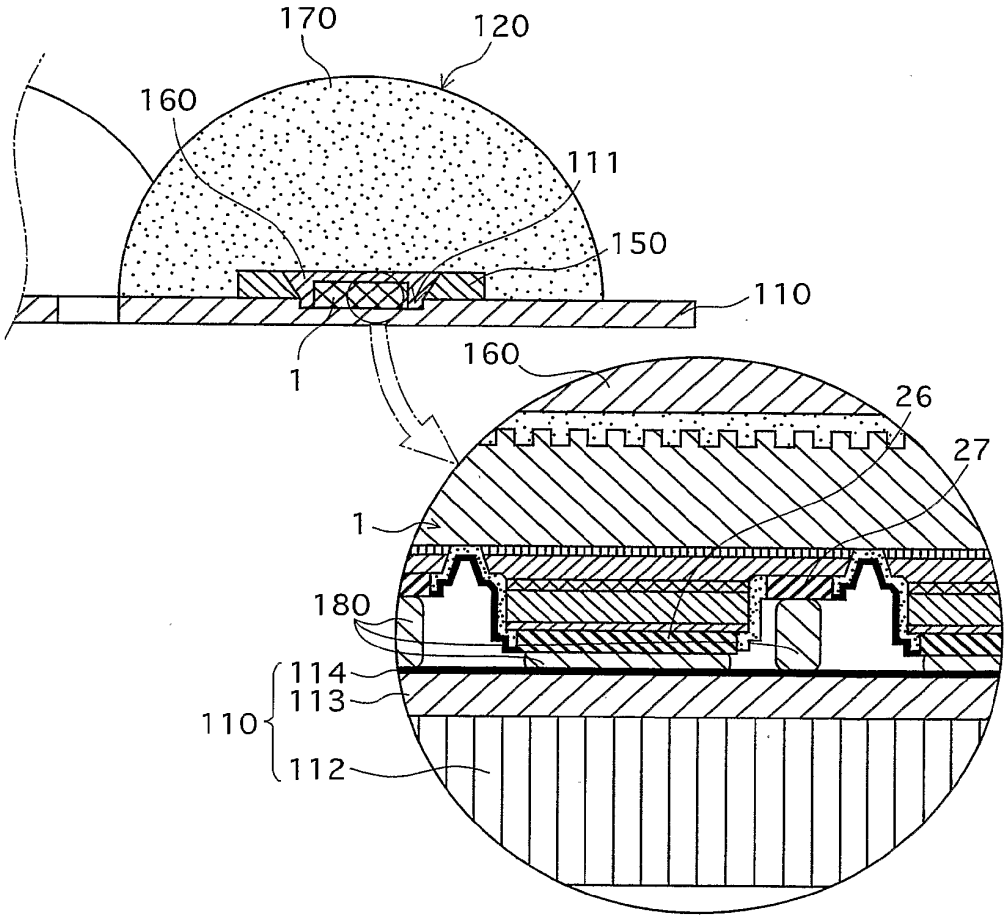

170
120
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111
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110
1
160
26
27
1
180
114
113
110
112

FIG.6

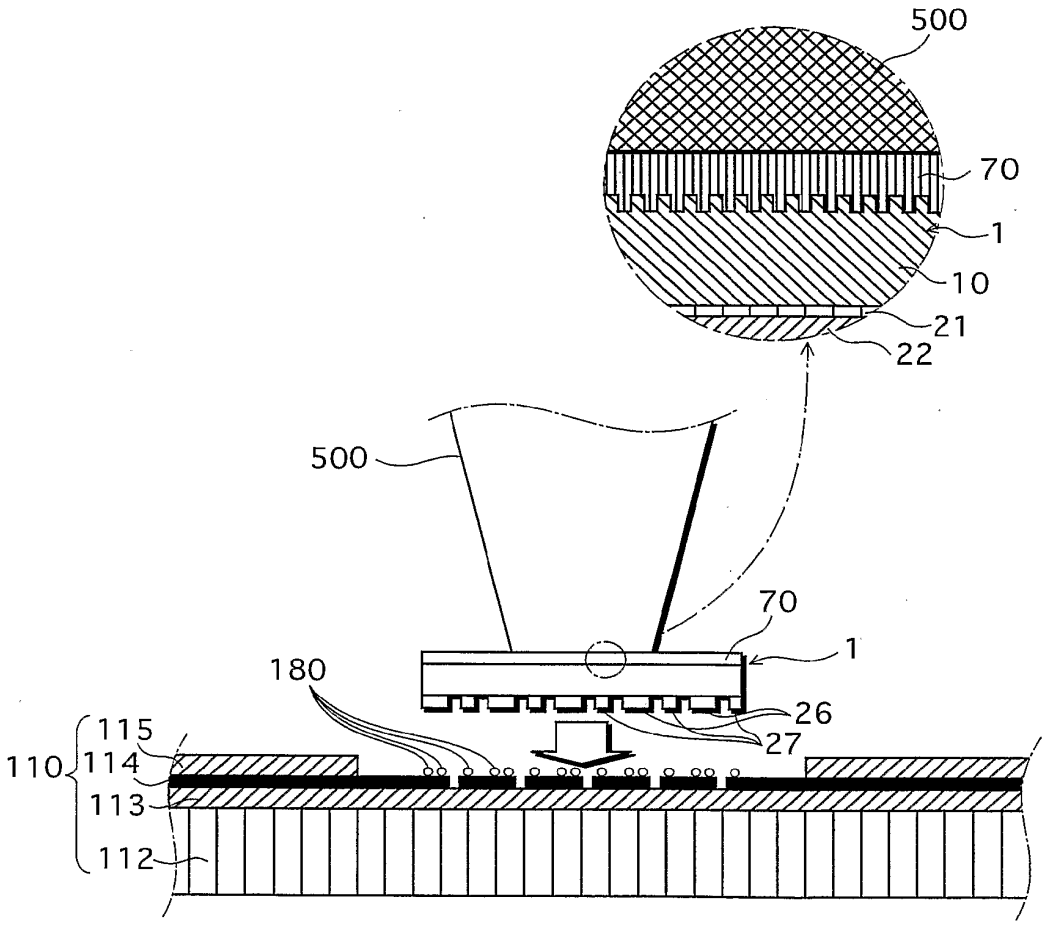


FIG.7A

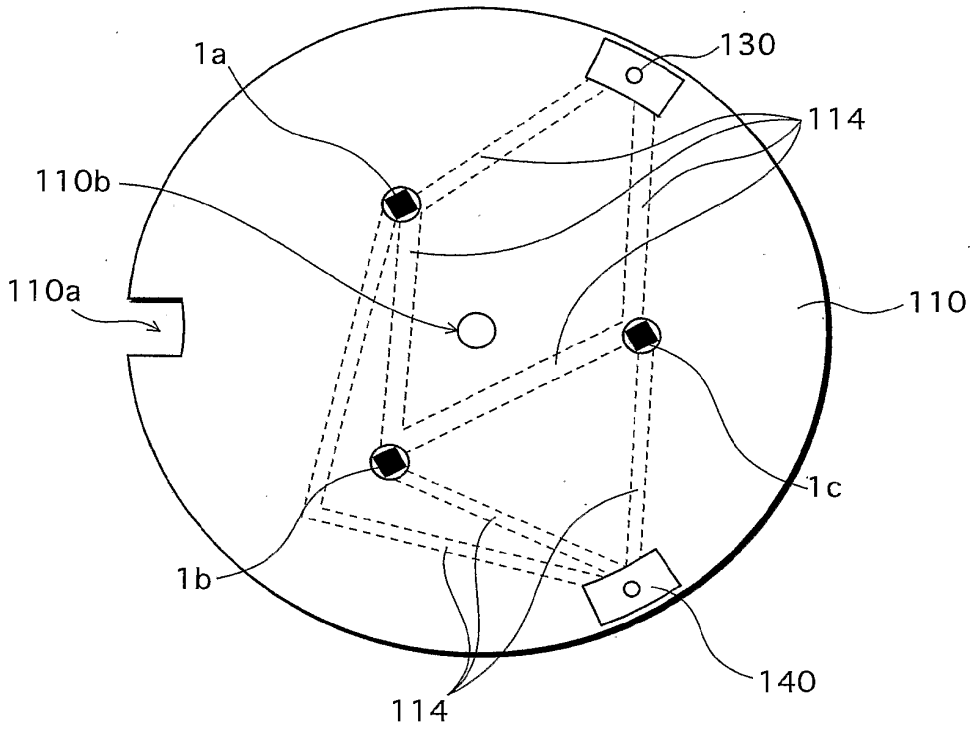

1a
130
114
110b
110a
110
1c
1b
140
114

FIG.7B

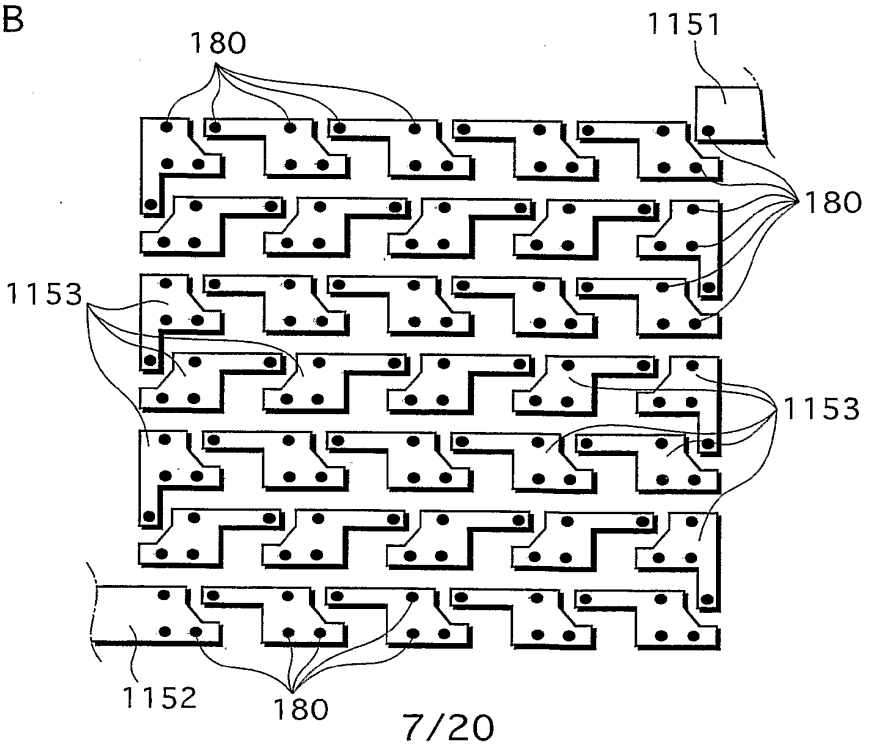

180
1151
180
1153
1153
1152
180

FIG.8A

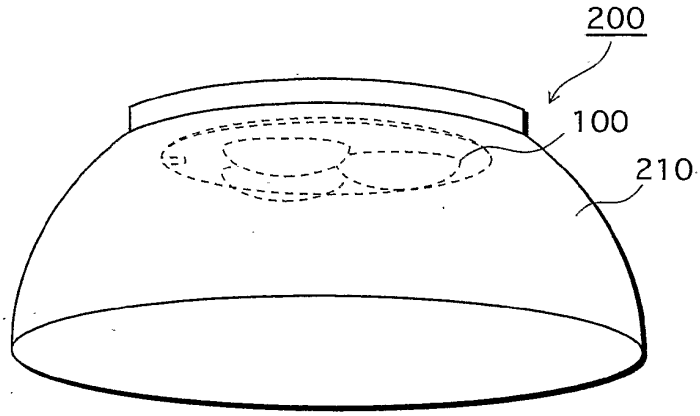


FIG.8B

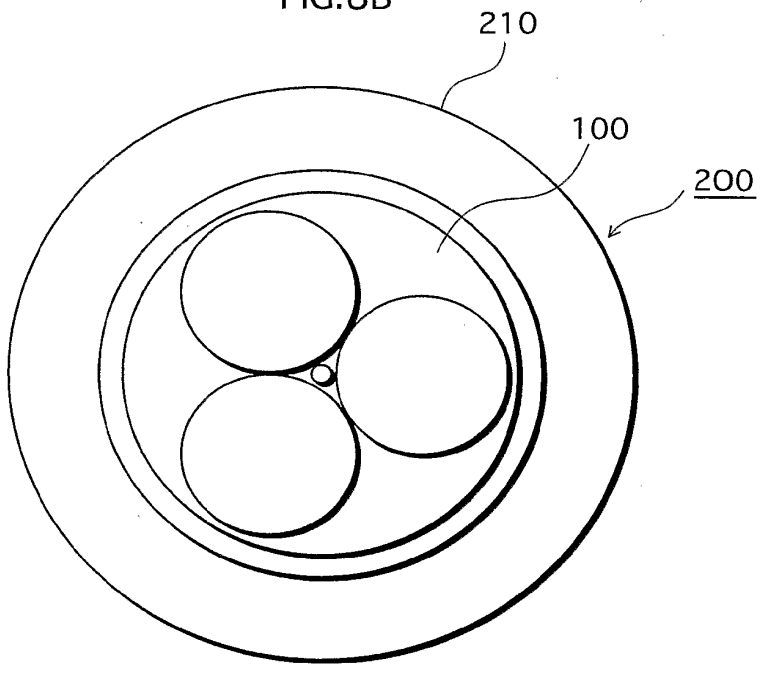


FIG.9

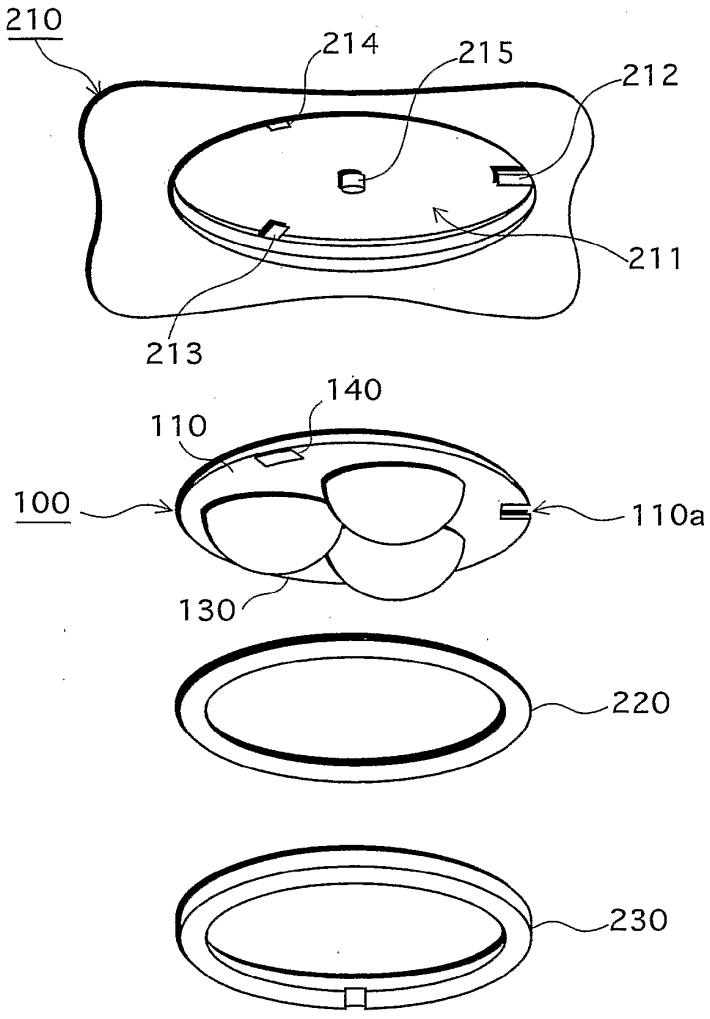


FIG.10

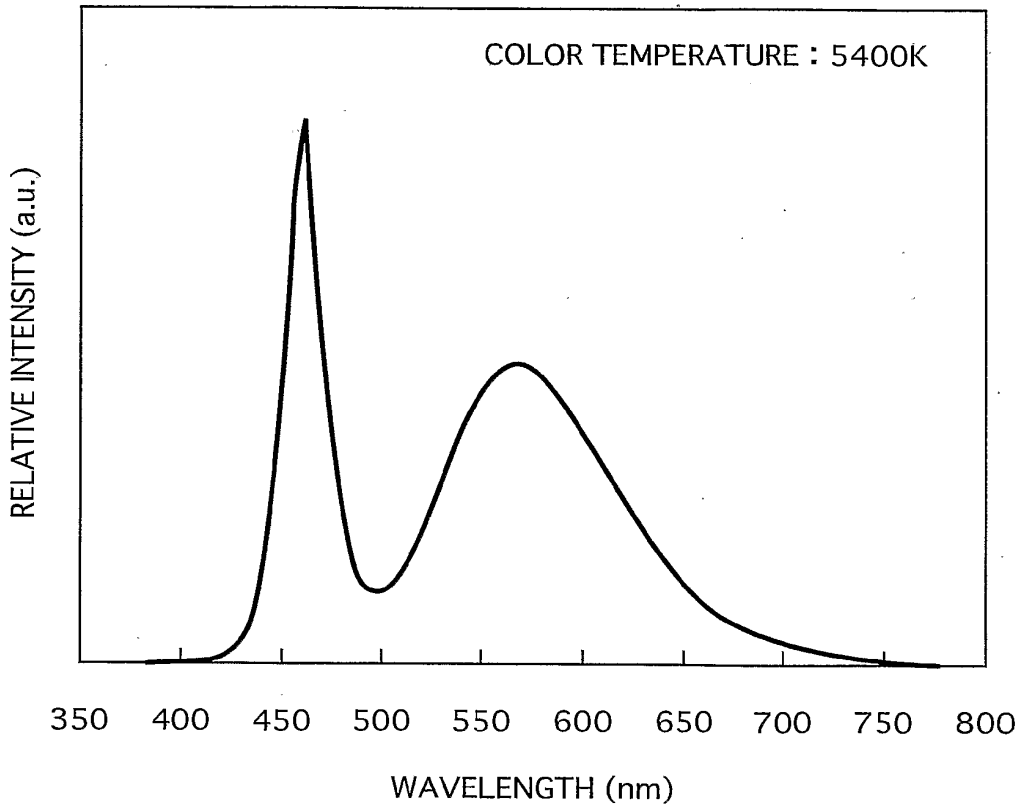

COLOR TEMPERATURE : 5400K
RELATIVE INTENSITY (a.u.)
350
400
450
500
550
600
650
700
750
800
WAVELENGTH (nm)

FIG.11A

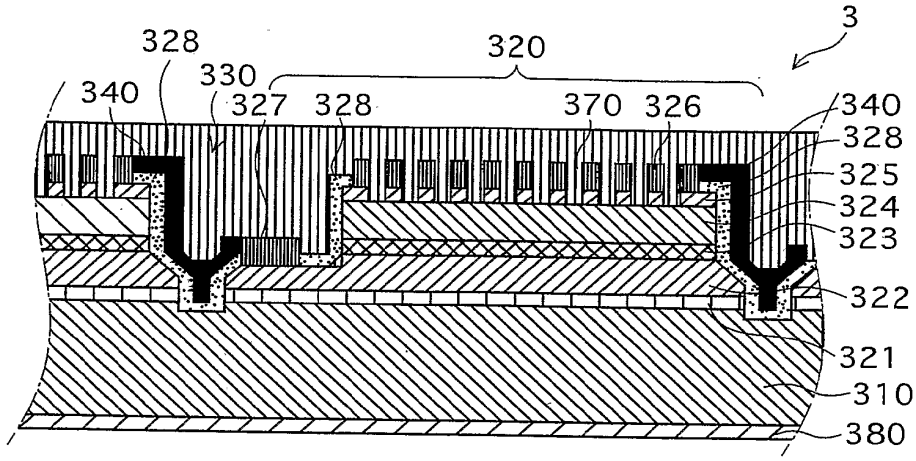


FIG.11B

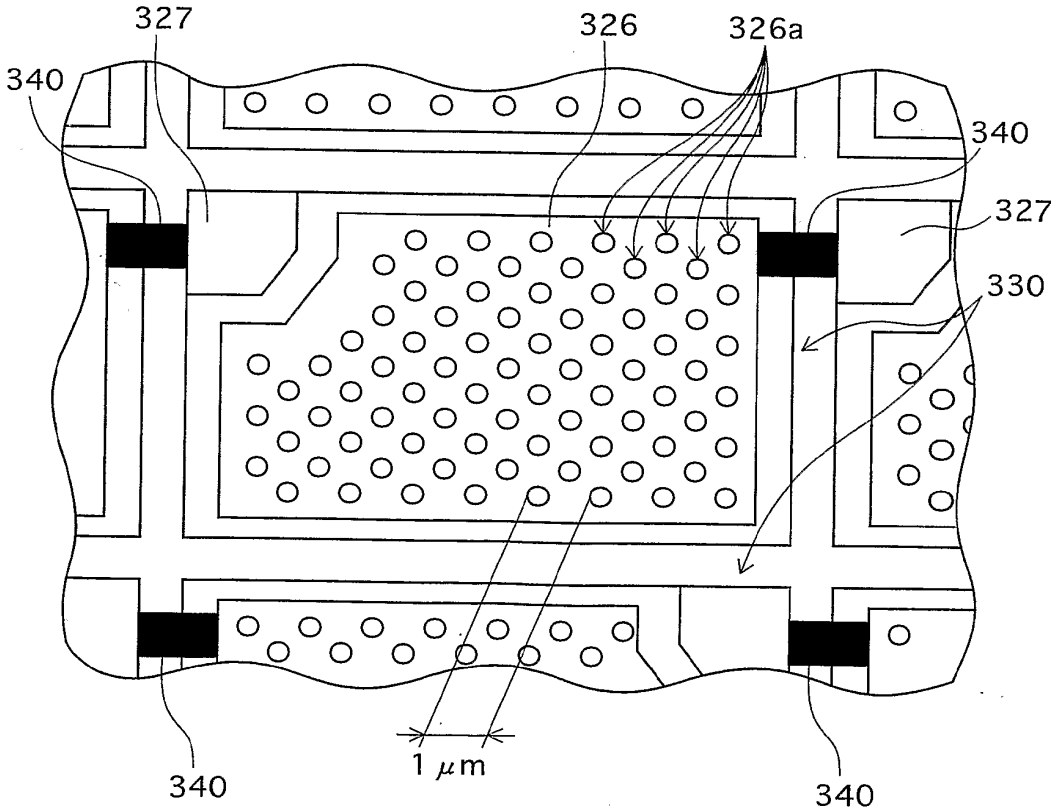


FIG.12A

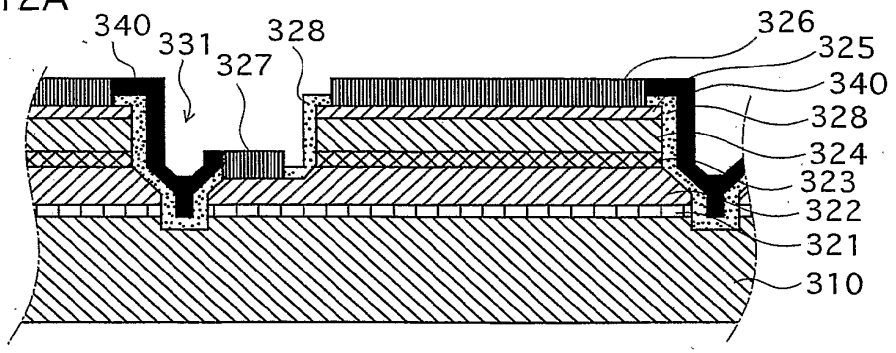


FIG.12B

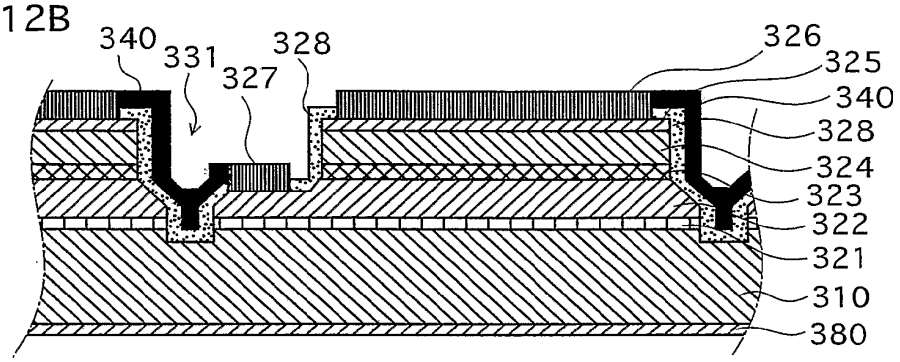


FIG.12C

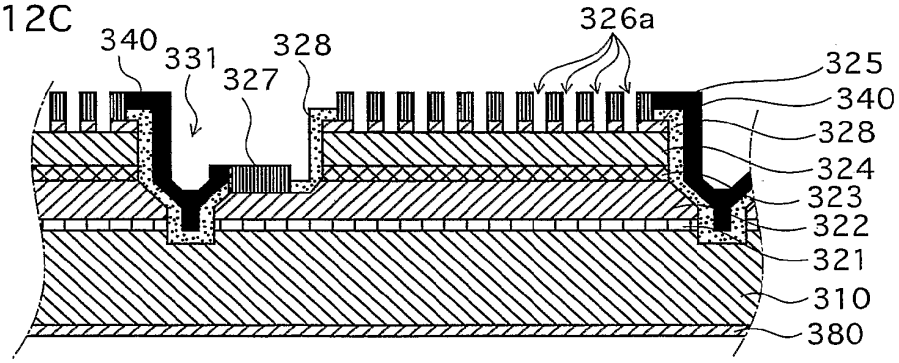


FIG.12D

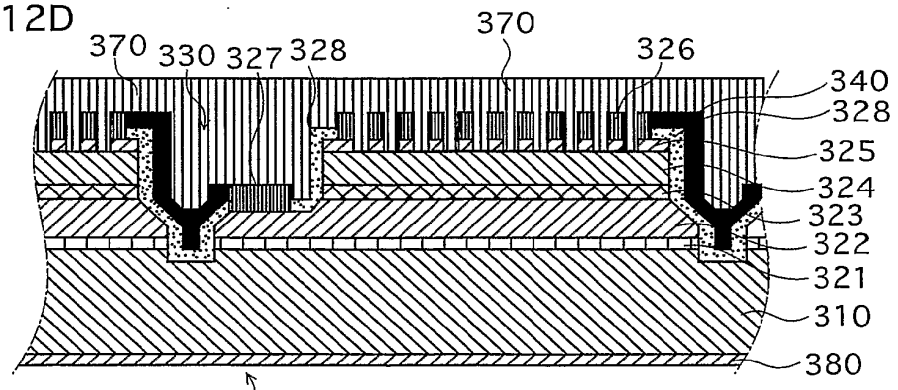


FIG.13A

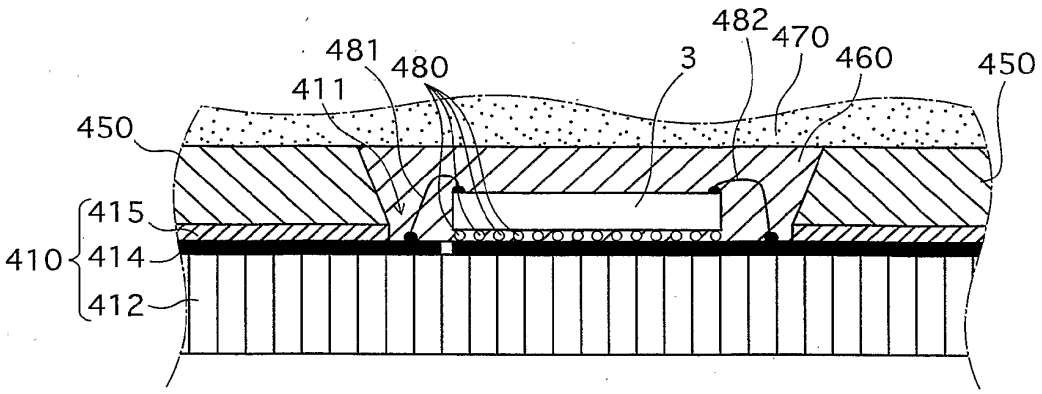


FIG.13B

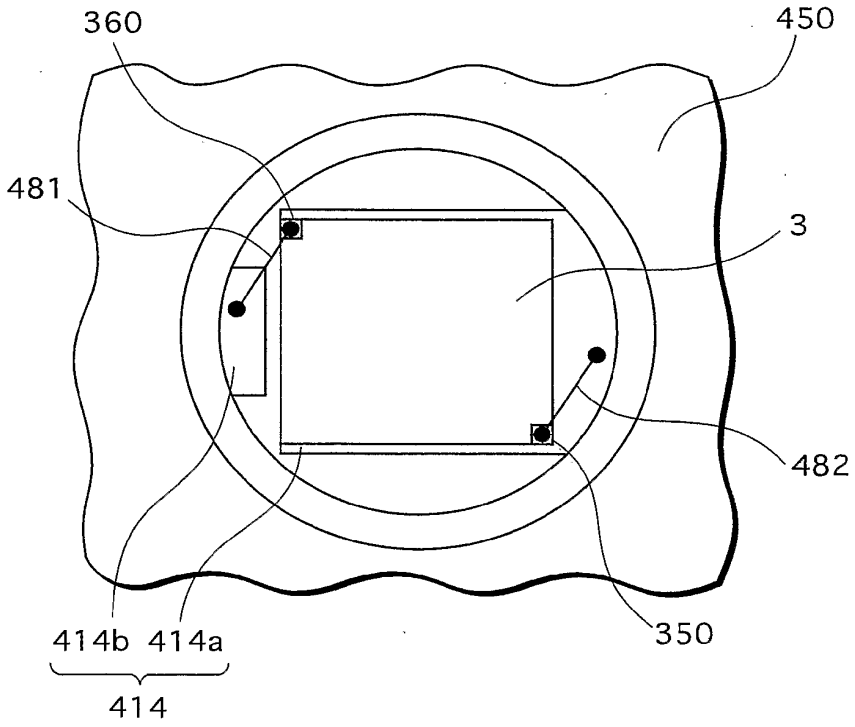


FIG.14

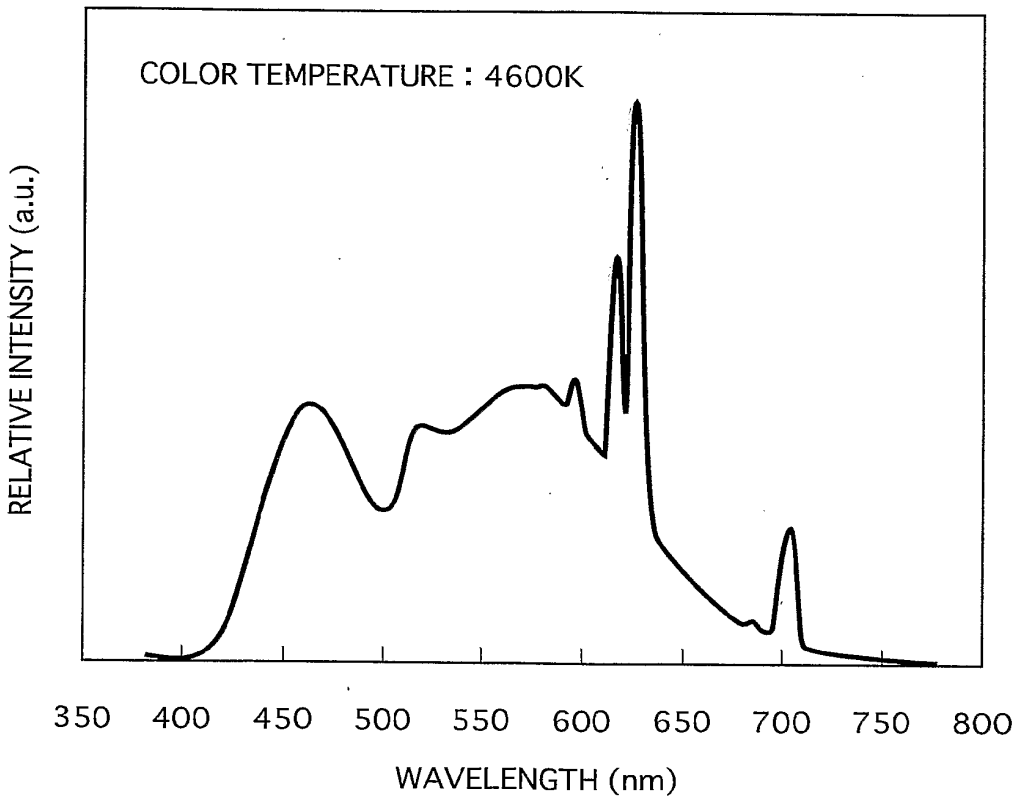

COLOR TEMPERATURE : 4600K
RELATIVE INTENSITY (a.u.)
350
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550
600
650
700
750
800
WAVELENGTH (nm)

FIG.15A

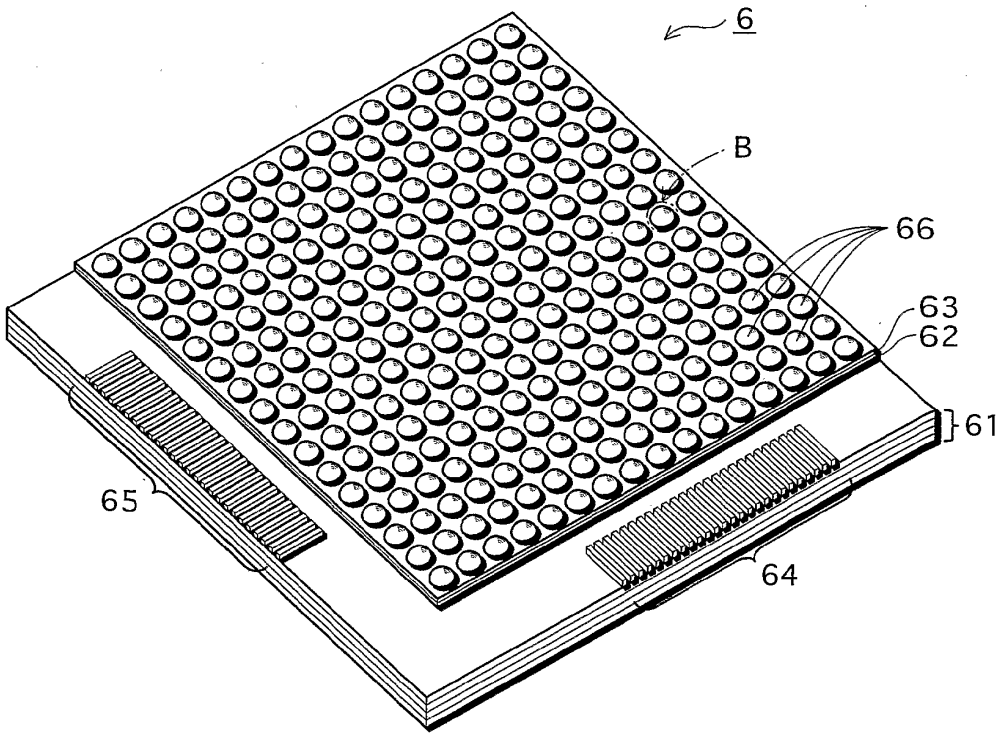


FIG.15B

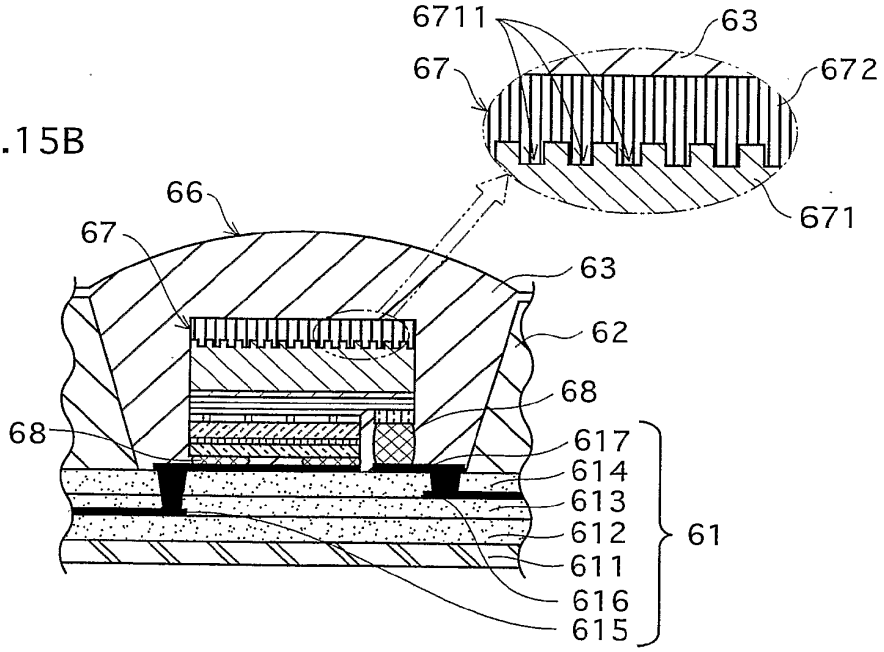


FIG.16A

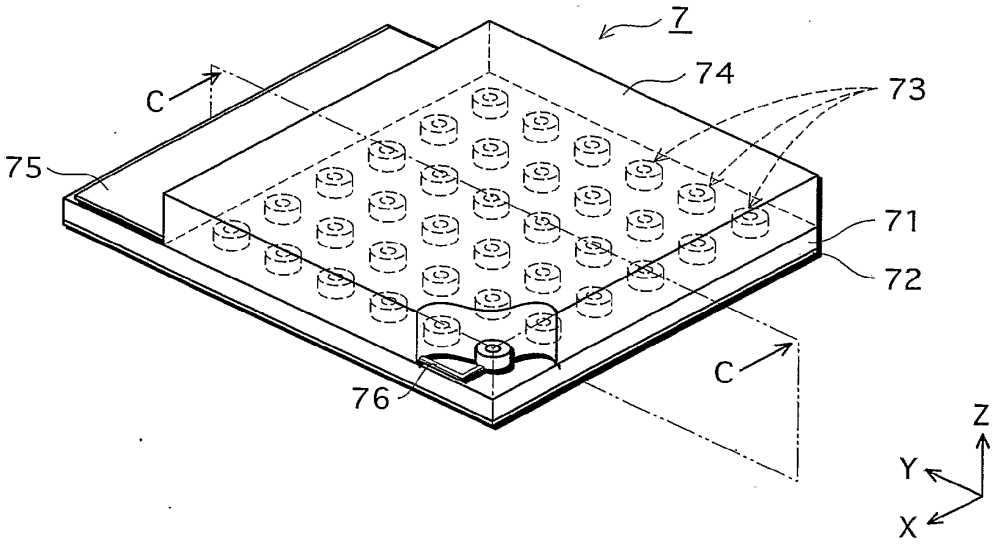


FIG.16B

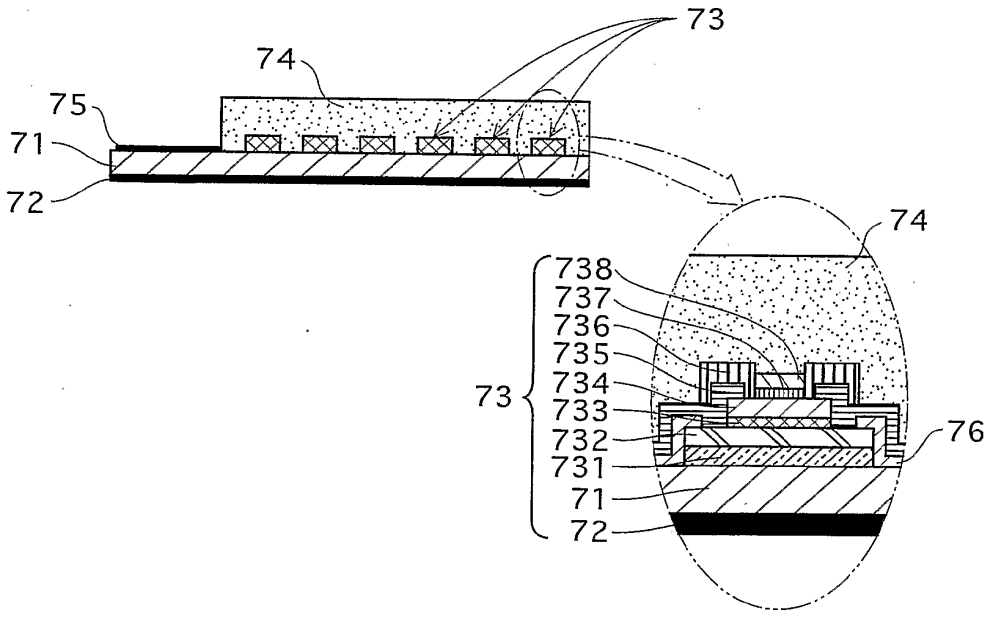


FIG.17A

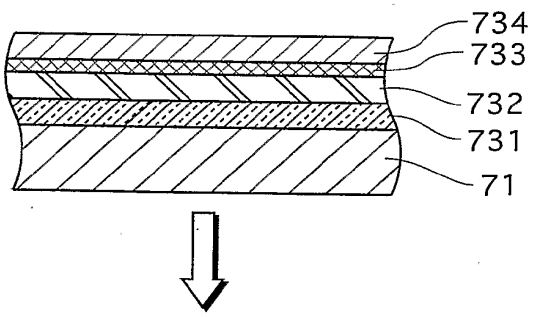


FIG.17B

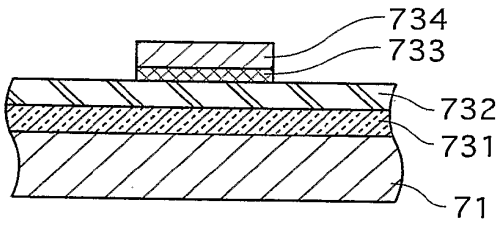


FIG.17C

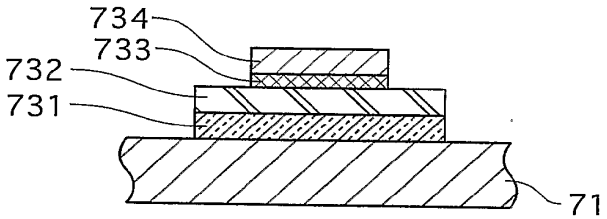


FIG.17D

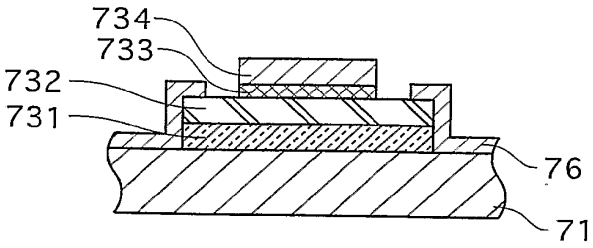


FIG.18E

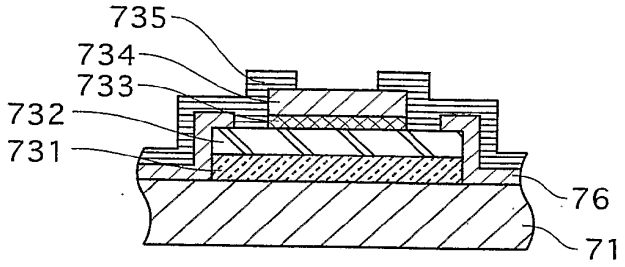


FIG.18F

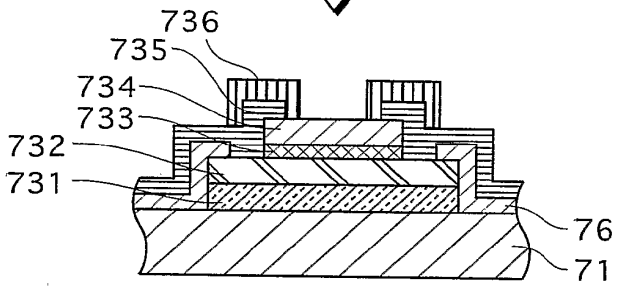


FIG.18G

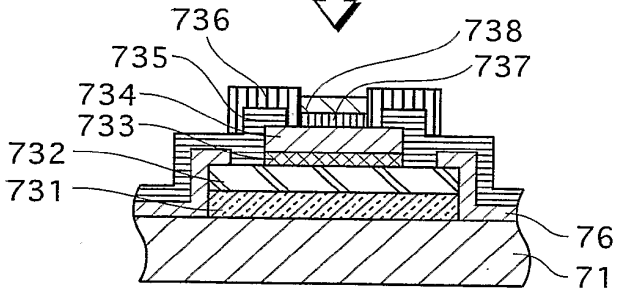


FIG.18H

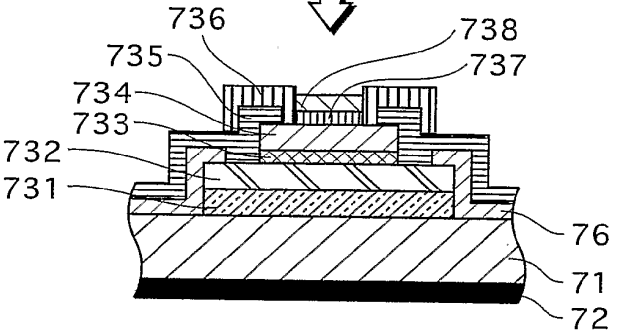


FIG.19

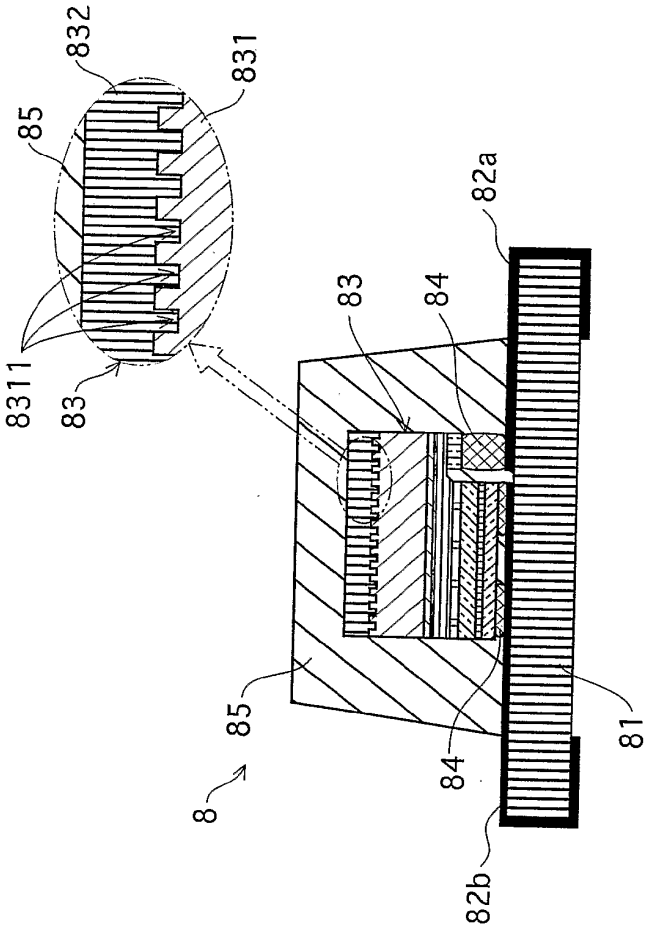
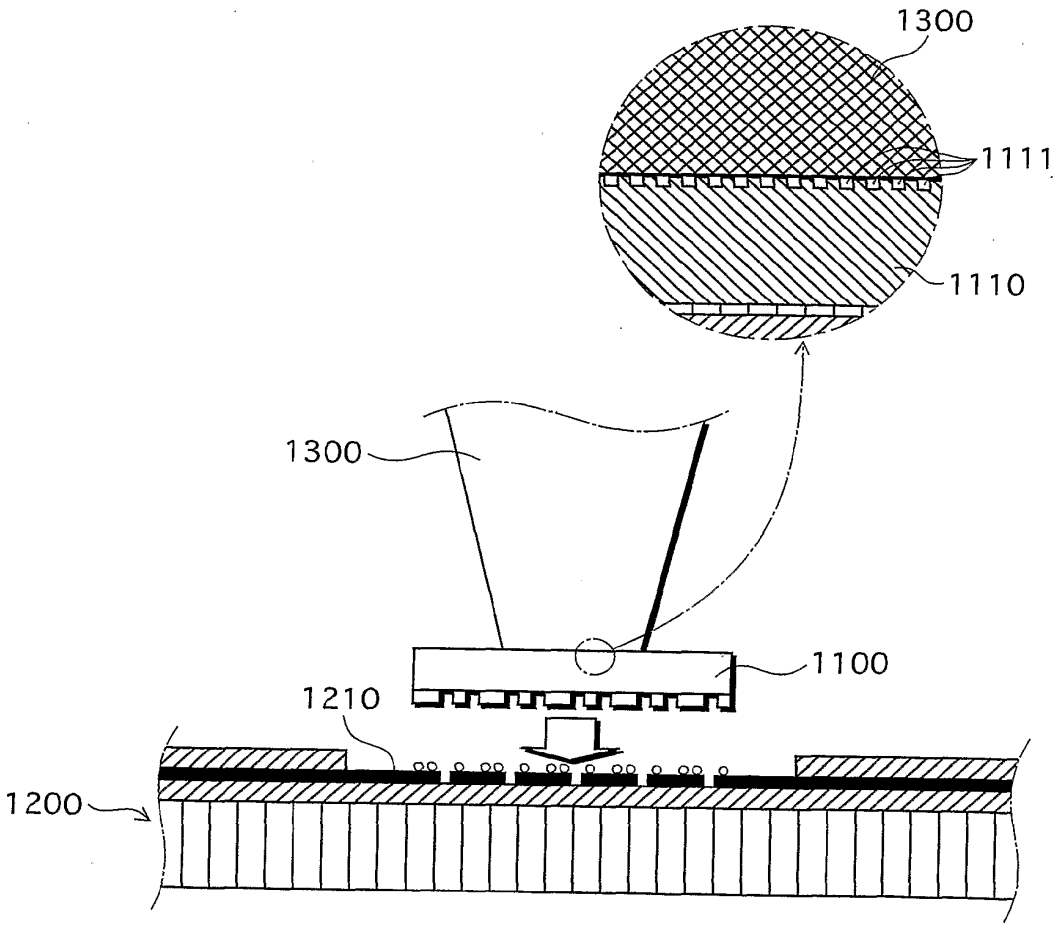


FIG.20



(12)特許協力条約に基づいて公開された国際出願

(19) 世界知的所有権機関
国際事務局

(43) 国際公開日
2005 年6 月2 日 (02.06.2005)

PCT

(10) 国際公開番号
WO 2005/050748 A1

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(21) 国際出願番号: PCT/JP2004/016957

(22) 国際出願日: 2004 年11 月15 日 (15.11.2004)

(25) 国際出願の言語: 日本語

(26) 国際公開の言語: 日本語

(30) 優先権データ:
特願 2003-388894
2003 年11 月19 日 (19.11.2003) JP

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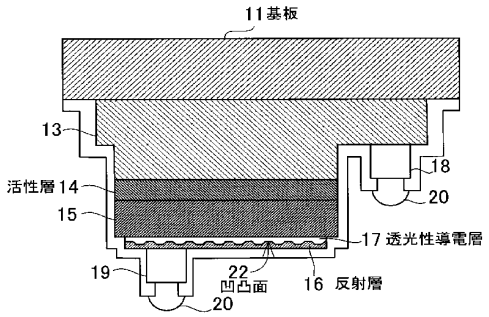
(72) 発明者; および

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[続葉有]

(54) Title: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SAME

(54) 発明の名称: 半導体素子及びその製造方法



11...SUBSTRATE
14...ACTIVE LAYER
17...TRANSPARENT CONDUCTIVE LAYER
22...INDENTED SURFACE
16...REFLECTIVE LAYER

(57) Abstract: A nitride semiconductor light-emitting device comprises a substrate (11) having a pair of major surfaces opposite to each other, a first conductivity type nitride semiconductor layer formed on one major surface of the substrate (11), a second conductivity type nitride semiconductor layer formed on the first conductivity type nitride semiconductor layer, an active layer (14) formed between the first conductivity type nitride semiconductor layer and the second conductivity type nitride semiconductor layer, and a reflective layer (16) formed on the second conductivity type nitride semiconductor layer for reflecting light traveling from the active layer (14) to the second conductivity type nitride semiconductor layer. This nitride semiconductor light-emitting device can be mounted on a wiring board in such a manner that the other major surface of the substrate (11) serves as a major light taking-out surface. Further, a transparent conductive layer (17) is formed between the reflective layer (16) and the second conductivity type nitride semiconductor layer, and an indented surface (22) is formed at the interface between the transparent conductive layer (17) and the reflective layer (16).

(57) 要約: 窒化物半導体発光素子は、対向する一対の主面を有する基板１１と、基板１１の一方の主面上に積層される第１の伝導型窒化物半導体層と、第１の伝導型窒化物半導体層上に積層される第２の伝導型窒化物半導体層と、第１の伝導型窒化物半導体層と第２の伝導型窒化物半導体層との間に形成される活性層１４と、第２の伝導型窒化物半導体層上に形成され、活性層１４から第２の伝導型窒化物半導体層に向かう光を反

[続葉有]

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射させるための反射層１６とを備える。この窒化物半導体発光素子は、上記基板１１の他方の主面を主光取出し面として配線基板に実装可能である。さらに、反射層１６と第２の伝導型窒化物半導体層との間に透光性導電層１７が形成されており、透光性導電層１７と反射層１６との界面に凹凸面２２が形成されている。

明 細 書

半導体素子及びその製造方法

技術分野

[0001] 本発明は、$Al_xIn_yGa_{1-x-y}N$（0≦x、0≦y、0≦x＋y＜1）からなる窒化物半導体を積層した半導体層を用いて形成した窒化物半導体素子及びその製造方法に関し、特に光取り出し効率を改善した発光ダイオード（LED）やレーザ等の半導体発光素子及びその製造方法に関する。

背景技術

[0002] 窒化ガリウム等の窒化物系半導体を用いた発光素子は、紫外光、青色光、緑色光等の発光が可能であり、高効率で低消費電力である上、小型化可能で機械的な振動等にも強く、長寿命で信頼性が高い等の利点を有することから、各方面での利用が進んでいる。特に発光素子は大型ディスプレイや信号機、携帯電話のバックライト光源等への普及が顕著である。

[0003] 窒化物系半導体を用いた発光素子においては、活性層で発生される光を外部に取り出して有効利用できるように、光の取り出し効率を高めることが重要となる。このような観点から透光性を有する導電膜が電極として要求されており、例えばITO（InとSnの複合酸化物）やSnO_2、ZnO等が利用されている。中でもITOは酸化物インジウムにスズを含有する酸化物導電性材料であり、低抵抗、高透明度を備えているので、透明電極等に好適である。

[0004] このような透明電極を利用したLEDの一例を図1に示す。LEDはサファイア基板1の上にバッファ層を介してn型GaN層2、InGaN発光層3、p型GaN層4が順次エピタキシャル成長された構成を有する。また、InGaN発光層3及びp型GaN層4の一部が選択的にエッチング除去されて、n型GaN層2が露出されている。p型GaN層3上にはp側透明電極5としてITO層が形成され、さらにp側電極7のボンディングパッドが積層されている。また、n型GaN層2の上にはn側電極8が形成されている。これらの電極は、Al、Au、In等の金属を蒸着によって形成している。このような構造においては、p側電極7を介して注入された電流は、導電性の良いp側透明電極5であるITO

層で均一に拡散され、p型GaN層3からn型GaN層2に電流が注入されて発光する。またその発光はp側電極7に遮られず、ITO層を透過してチップ外に取り出される。

[0005] しかしながら、このような窒化物系半導体発光素子は、電極部の接触抵抗が高いという問題を有していた。それは、GaNのバンドギャップは3．4eVと広いために、電極とオーミック接触をさせることが難しいからである。その結果、電極部の接触抵抗が高くなり、素子の動作電圧が高くなって消費電力、発熱量も大きくなるという問題が生ずる。

[0006] また一方で、光の取り出し効率も良くない。それは、GaNの屈折率は約2．67と大きいために、臨界角が21．9度と極めて小さいからである。つまり、主光取出し面の法線からみて、この臨界角よりも大きい角度で入射した光は、LEDチップの外に取り出せず閉じ込められてしまう。このために、外部量子効率を改善してより大きな発光パワーを得ることが困難であった。

[0007] ここで、主光取出し面であるp型GaN層の表面を凹凸形状に加工すれば、この問題を改善することができる。しかし、凹凸形状を形成するためにはp型GaN層はある程度の厚さが必要となる。そして、電極との接触抵抗を少しでも低減するために高濃度の不純物をドーピングしつつ、厚いp型GaN層を形成しようとすると、結晶表面の面荒れが発生するという新たな問題が生じていた。

[0008] このような問題を解消するものとして、主光取出し面に凹凸を設けて光取り出し効率を改善したLED発光素子が特許文献1に開示される。特許文献1に開示されるLEDは、透明電極であるITO層とp型半導体層であるp型GaN層との界面を凹凸にして、この面で反射される光を外部に取り出しし易い構成として取り出し効率を改善したものである。具体的には、p型GaN層の表面を凹凸に加工して、この上に透明金属電極や透明電極を設けている。

[0009] しかしながら、GaN層の表面を凹凸に加工すると、エピタキシャル成長層がダメージを受けてこの部分が発光しなくなるという問題がある。またp型GaN層は薄いため、凹凸加工の際に活性層、n型GaN層に達してしまうことがあり、これを回避するにはGaN層を厚膜にしなければならなかった。一方、p型GaN層の表面を平面としてp側透明電極の表面を凹凸に加工する方法もあるが、凹凸面が主光取出し面に近くなるた

め、この凹凸パターンが外部から視認され易くなって外観上の見栄えが悪くなるという問題があった。

[0010] また主光取出し面にp型電極を設けたいわゆるフェイスアップ構造では、n型電極を設ける必要があり主光取出し面が狭くなる上、p型電極にパッド電極を設けるため、この部分で光が遮られてしまい、光の取り出しができなくなって光取り出し効率が悪くなるという問題もあった。

[0011] また透光性導電層として、ITOが代表として挙げられる導電性酸化物膜を用いる構造では、透光性を良好にする必要があり、さらに導電性酸化物膜を半導体層に接して設ける構造では、オーミック特性も良好にする必要がある。しかしながら、透光性とオーミック特性とを同時に良好にすることは困難であり、導電性酸化物膜のさらなる特性の向上が必要であった。

特許文献1:特開2000−196152号公報

発明の開示

発明が解決しようとする課題

[0012] 本発明は、このような問題点を解決するためになされたものである。本発明の主な目的は、反射効率の高い半導体発光素子及びその製造方法であって、特に光取り出し効率の優れた半導体発光素子及びその製造方法を提供することにある。

課題を解決するための手段

[0013] 以上の目的を達成するために本発明に係る半導体素子は、対向する一対の主面を有する基板11と、前記基板11の一方の主面上に第1の伝導型半導体層と、前記第1の伝導型半導体層上に第2の伝導型半導体層と、前記第1の伝導型半導体層と第2の伝導型半導体層との間に形成される活性層14と、前記第2の伝導型半導体層上に形成され、前記活性層14から前記第2の伝導型半導体層に向かう光を反射させるための反射層16とを備える。

この半導体素子は、発光素子として、上記基板11の他方の主面を主光取出し面として配線基板に実装可能である。さらに、前記反射層16と第2の伝導型半導体層との間に透光性導電層17が形成されており、前記透光性導電層17と前記反射層16との界面に凹凸面22が形成されている。この構成によって、活性層14から第2の伝導型

半導体層に照射される光を凹凸面22で反射、散乱させて、外部への光の取り出し効率を高めることができる。特に、透光性導電層17と前記反射層16との界面で凹凸を形成しているため、第2の伝導型半導体層の特性を悪化させずに表面を加工することが困難な問題を解消している。

[0014] また半導体発光素子は、前記透光性導電層17と前記第2の伝導型半導体層との界面が略平滑面とすることができる。この構成によって、第2の伝導型半導体層の表面には加工を行うことなく、透光性導電層17と前記反射層16との界面で凹凸を形成して光の取り出し効率を改善できる。

[0015] さらに半導体素子は、半導体発光素子として、前記凹凸面22が傾斜面を備えており、該傾斜面の傾斜角度が主光取出し面の法線に対して60° 以下とすることができる。この構成によって、光を臨界角以下の角度に反射させる確率を高くでき、光の取り出し効率を改善することができる。

[0016] さらに半導体素子は、半導体発光素子として、前記凹凸面22が連続したシリンドリカルレンズ状とすることができる。この構成によって、界面に平行な面を少なくし、光を臨界角以下の角度に反射させる確率を高くして光の取り出し効率を改善することができる。

[0017] さらにまた、半導体素子は、半導体発光素子として、前記透光性導電層17がZn、In、Sn、Mgよりなる群から選択された少なくとも1種の元素Cを含む酸化物からなる層を用いることができる。また、前記酸化物膜は元素Cに加えて、微量元素Dを含む層を用いることができる。また、微量元素Dは、スズ、亜鉛、ガリウム、アルミニウムから選択される少なくとも一種の元素とすることができる。好ましくは元素Cとしてインジウム、微量元素Dとしてスズを用いたITOからなるよう構成することができる。この構成によって、微細パターンが形成し易いITOを透光性導電層17として表面を凹凸面22に加工でき、光の取り出し効率を高めることができる。またITOは窒化物半導体層とのオーミック接続にも優れているため、窒化物半導体発光素子として、第2の伝導型窒化物半導体層との界面での接触抵抗を小さくして順方向電圧Vfが低い実用的な窒化物半導体発光素子を実現できる。

[0018] また、元素Cと微量元素Dを含む酸化物膜を、半導体層との界面近傍における微

量元素Dが、酸化物膜の他の部分の膜中微量元素Dの濃度よりも高い半導体素子とすることができる。また元素Cと微量元素Dを含む酸化物膜を、半導体層との界面近傍における微量元素Dが、界面に対向する面近傍の微量元素Dの濃度よりも高い半導体素子とすることができる。この構成によって、例えばITOでは、微量元素Dを酸化物膜中において一定に含むものよりも、半導体層側においてキャリアを多く配置することができ、ショットキー障壁を小さく、また半導体層側のシート抵抗を小さくすることができ、光取り出し効率の改善とシート抵抗の低減を両立させた高品質の半導体発光素子を実現できる。また前記酸化物膜は元素Cに対して20%以下の元素Dを含むことが好ましい。

[0019] さらにまた、窒化物半導体発光素子は、前記反射層16をアルミニウム、チタン、白金、ロジウム、銀、パラジウム、イリジウム、ケイ素、亜鉛から選択される少なくとも一種の元素を含む層とすることができる。なかでも本発明の窒化物半導体発光素子に用いる高反射が実現できる層として、アルミニウム(Al)、ロジウム(Rh)、銀(Ag)を含む層とすることが好ましい。アルミニウム、ロジウム、銀は高反射率であるため、透光性導電層17との界面で効率よく反射させて光取り出し効率を高くできる。

[0020] さらにまた、窒化物半導体発光素子は、前記反射層16がSi、Zn、Ti、Zr、Hf、Nb、Ta、Al、Mgの少なくともいずれかを含む誘電体としてもよい。さらに好ましくはSiO_2、TiO_2、ZrO_2、HfO_2、Nb_2O_3、Al_2O_3等、組み合わせて低屈折率と高屈折率の関係を満たし、その屈折率差が大きくなるように2種の誘電体を多層化した誘電体多層膜、又はSiO_2、MgO、MgF、Al_2O_3、SiN、SiON等を用いることが好ましい。この構成によって、反射層16と透光性導電層17との接着性を高めることができる。特に透光性導電層17にITOを使用する場合、反射層16をAl等の金属よりも誘電体の方が界面の接着性が高く、信頼性を高めることができる。

[0021] さらにまた、窒化物半導体発光素子は、前記透光性導電層17の膜厚を、前記活性層14から放出される光の波長λに対してλ／4のおよそ整数倍としてもよい。

[0022] さらにまた、窒化物半導体発光素子は前記透光性導電層17の膜厚を2μm以下とすることができる。

[0023] さらに窒化物半導体発光素子は、前記反射層16を、基板11の主面と交差する面

にも形成してもよい。この構造によって、横方向に放射される光も上面に反射させて、より多くの光を取り出すことが可能となる。

[0024] さらにまた、窒化物半導体発光素子は、前記窒化物半導体層の、前記基板11の主面と交差する面の少なくとも一部を傾斜させている。この構成によって、横方向に放射される光を上方向に反射させて、光の取り出し効率をさらに改善できる。

[0025] また、本発明の窒化物半導体発光素子の製造方法は、対向する一対の主面を有する基板11と、前記基板11の一方の主面上に第1の伝導型半導体層と、前記第1の伝導型半導体層上に第2の伝導型半導体層と、前記第1の伝導型半導体層と第2の伝導型半導体層との間に形成される活性層14と、前記第2の伝導型半導体層上に形成され、前記活性層14から前記第2の伝導型半導体層に向かう光を反射させるための反射層16と、を備え、上記基板11の他方の主面を主光取出し面として配線基板に実装可能な半導体素子の製造方法である。この方法は、基板11上に、第1の伝導型半導体層と、活性層14と、第2の伝導型半導体層を積層するステップと、前記第2の伝導型半導体層上に透光性導電層17を形成するステップと、前記透光性導電層17に凹凸面22を形成するステップと、前記凹凸面22の形成された透光性導電層17上に反射層16を形成するステップとを備える。これによって、活性層14から第2の伝導型半導体層に照射される光を凹凸面22で反射、散乱させて、外部への光の取り出し効率を高めることができる。特に、透光性導電層17と前記反射層16との界面で凹凸を形成しているため、第2の伝導型半導体層の特性を悪化させずに表面を加工することが困難な問題を解消している。

発明の効果

[0026] 本発明の半導体素子及びその製造方法は、特性を低下させることなく加工することが困難な窒化物半導体への損傷を与えることなく、外部への光取り出し効率を大きく改善することができる。それは、本発明が凹凸面を有する透光性導電層上に反射膜を成型することにより、この界面を凹凸を備える反射面として、反射部と対向する主光取出し面に対し、反射光の多くを臨界角以下の角度で入射させて外部への光取り出しを大幅に増加させているからである。また透光性導電層を第2の伝導型窒化物半導体層と反射層との間に介在させることで、上記凹凸面の加工が容易なことに加えて

、オーミック接触を得やすいという利点もある。特に窒化物半導体と金属はオーミック接触を得ることが困難であるが、ITOや誘電体等の透光性導電層を介在させることでオーミック接触を取りやすくなり、この接触抵抗を小さくして動作電圧を下げ、消費電力や発熱量を抑えた窒化物半導体発光素子を実現できるという利点もある。

[0027] また透光性導電膜として用いる導電性酸化物膜を本発明の構造とすることにより、半導体素子、特に半導体発光素子として、光取り出し効率の改善とシート抵抗の低減を両立させた高品質の半導体発光素子を実現できる。

図面の簡単な説明

[0028] [図1]従来の透明電極を利用したLEDの一例を示す概略断面図である。

[図2]本発明の一実施の形態に係る窒化物半導体発光素子を実装したLEDを示す概略断面図である。

[図3]本発明の第1の実施の形態に係る窒化物半導体発光素子を示す概略断面図である。

[図4]発光素子において反射面で反射した光を主光取り出し面から取り出す様子を示す説明図である。

[図5]本発明の第1の実施の形態の変形例1に係る窒化物半導体発光素子を示す概略断面図である。

[図6]本発明の第1の実施の形態の変形例2に係る窒化物半導体発光素子を示す概略断面図である。

[図7]本発明の第1の実施の形態の変形例3に係る窒化物半導体発光素子を示す概略断面図である。

[図8]窒化物半導体層と金属膜の反射層との間に透光性導電層を介在させることによる光吸収の変化を示す説明図である。

[図9]本発明の第1の実施の形態の変形例4に係る窒化物半導体発光素子を示す概略断面図である。

[図10]ITO膜中のスズのデプスプロファイルを示すグラフである。

[図11]本発明の実施の形態2に係る窒化物半導体発光素子を示す概略断面図である。

[図12]本発明の他の実施の形態に係る窒化物半導体発光素子として透光性導電層の表面を示す概略図である。

[図13]本発明の他の実施の形態に係る窒化物半導体発光素子として、電極形状を示す概略図である。

符号の説明

[0029] 1…サファイア基板;2…n型GaN層;3…InGaN発光層;4…p型GaN層
5…p側透明電極;7…p側電極;8…n側電極;9…LEDチップ;10…サブマウント
11…基板;12…バッファ層
13…n型窒化物半導体層;14…活性層;15…p型窒化物半導体層
16…反射層;17…透光性導電層
18…n側パッド電極;19…p側パッド電極
20…バンプ;21…ワイヤー
22、22B、22C、22D…凹凸面
23…窒化物半導体層;24…金属膜
25…窒化物半導体層と金属膜との界面;26…窒化物半導体層と透光性導電層との界面
27…透光性導電層と金属膜との界面;28…傾斜面
29…誘電体反射層;30…補助電極

発明を実施するための最良の形態

[0030] 以下、本発明の実施の形態を図面に基づいて説明する。ただし、以下に示す実施の形態は、本発明の技術思想を具体化するための半導体素子及びその製造方法を例示するものであって、本発明は半導体素子及びその製造方法を以下のものに特定しない。

[0031] また、本明細書は特許請求の範囲に示される部材を、実施の形態の部材に特定するものでは決してない。特に実施の形態に記載されている構成部品の寸法、材質、形状、その相対的配置等は特に特定的な記載がない限りは、本発明の範囲をそれのみに限定する趣旨ではなく、単なる説明例にすぎない。なお、各図面が示す部材の大きさや位置関係等は、説明を明確にするため誇張していることがある。さらに以

下の説明において、同一の名称、符号については同一もしくは同質の部材を示しており、詳細説明を適宜省略する。さらに、本発明を構成する各要素は、複数の要素を同一の部材で構成して一の部材で複数の要素を兼用する態様としてもよいし、逆に一の部材の機能を複数の部材で分担して実現することもできる。

(実施の形態1)

[0032] 本発明の一実施の形態に係る窒化物半導体発光素子を実装した例を図2の概略断面図に示す。この図では、窒化物半導体発光素子であるLEDチップ9を配線基板の一であるサブマウント10上にフリップチップ実装している。フリップチップは、窒化物半導体層の電極形成面を主光取出し面とするフェイスアップ実装と異なり、電極形成面と対向する基板11側を主光取出し面とする実装方式であり、フェイスダウン実装等とも呼ばれる。

[0033] 図2のLEDチップ9は、基板11上にバッファ層12、n型窒化物半導体層13、活性層14、p型窒化物半導体層15を順にエピタキシャル成長し、さらに透光性導電層17と反射層16を積層している。結晶成長方法としては、例えば、有機金属気相成長法(MOCVD:metal-organic chemical vapor deposition)、ハイドライド気相成長法(HVPE)、ハイドライドCVD法、MBE(molecularbeam epitaxy)等の方法が利用できる。また、半導体層の積層構造としては、MIS接合、PIN接合やPN接合を有したホモ構造、ヘテロ構造あるいはダブルヘテロ構成のものが挙げられる。また、各層を超格子構造としたり、活性層14を量子効果が生ずる薄膜に形成させた単一量子井戸構造や多重量子井戸構造とすることもできる。

[0034] また図2においては詳細に図示しないが、活性層14及びp型窒化物半導体層15の一部を選択的にエッチング除去して、n型窒化物半導体層15の一部を露出させて、n側パッド電極18を形成している。またn側電極と同一面側で、p型窒化物半導体層15にはp側パッド電極19が形成される。パッド電極の上には、外部電極等と接続させるためのメタライズ層(バンプ20)を形成する。メタライズ層は、Ag、Au、Sn、In、Bi、Cu、Zn等の材料から成る。これらLEDチップ9の電極形成面側をサブマウント10上に設けられた正負一対の外部電極と対向させ、バンプ20にて各々の電極を接合する。さらにサブマウント10に対してワイヤー21等が配線される。一方、フェイスダウ

ンで実装されたLEDチップ9の基板11の主面側を、主光取出し面としている。

[0035] なお本明細書において、層上等でいう「上」とは、必ずしも上面に接触して形成される場合に限られず、離間して上方に形成される場合も含んでおり、層と層の間に介在層が存在する場合も包含する意味で使用する。

[0036] 図3に、本発明の第1の実施の形態に係る窒化物半導体発光素子をより詳細に示す。図に示す窒化物半導体発光素子はフリップチップ実装であることを示すため、上下逆に表示している。実際の製造工程では基板11上に各層を形成し、得られた窒化物半導体発光素子を上下逆にして図2のように実装する。

[0037] [基板11]

基板11は、窒化物半導体をエピタキシャル成長させることができる透光性基板で、基板の大きさや厚さ等は特に限定されない。この基板としては、C面、R面、及びA面のいずれかを主面とするサファイアやスピネル($MgAl_2O_4$)のような絶縁性基板、また炭化珪素(6H、4H、3C)、シリコン、ZnS、ZnO、Si、GaAs、ダイヤモンド、及び窒化物半導体と格子接合するニオブ酸リチウム、ガリウム酸ネオジウム等の酸化物基板が挙げられる。また、デバイス加工が出来る程度の厚膜(数十μm以上)であればGaNやAlN等の窒化物半導体基板を用いることもできる。異種基板はオフアングルしていてもよく、サファイアC面を用いる場合には、0.01°ー3.0°、好ましくは0.05°ー0.5°の範囲とする。またさらに基板としてサファイア等の窒化物半導体と異なる材料を用いるとき、基板に凹凸を形成した上に窒化物半導体をエピタキシャル成長させてもよい。これにより、窒化物半導体層と異種基板との界面で反射する光を減らすことができ、また界面で反射した光も工程に基板側から出されるようになるので、好ましい。この凹凸の段差としては、少なくとも発光層からの光の波長よりも大きくかつ、発光層を成長する際に平坦な面が得られる程度の段差を設ければよい。

[0038] [窒化物半導体層]

窒化物半導体としては、一般式が$In_xAl_yGa_{1-x-y}N$($0 \leqq x$、$0 \leqq y$、$x+y \leqq 1$)であって、BやP、Asを混晶してもよい。また、n型窒化物半導体層13、p型窒化物半導体層15は、単層、多層を特に限定しない。また、窒化物半導体層にはn型不純物、p型不純物を適宜含有させる。n型不純物としては、Si、Ge、Sn、S、O、Ti、Zr等のIV

族、若しくはVI族元素を用いることができ、好ましくはSi、Ge、Snを、最も好ましくはSiを用いる。また、p型不純物としては、特に限定されないが、Be、Zn、Mn、Cr、Mg、Ca等が挙げられ、好ましくはMgが用いられる。これにより、各導電型の窒化物半導体を形成することができる。前記窒化物半導体層には活性層14を有し、該活性層14は単一（SQW）又は多重量子井戸構造（MQW）とする。以下に窒化物半導体の詳細を示す。

[0039] 基板11上に成長させる窒化物半導体はバッファ層（図3に図示せず）を介して成長する。バッファ層としては、一般式$Al_aGa_{1-a}N$（$0 \leqq a \leqq 0.8$）で表される窒化物半導体、より好ましくは、$Al_aGa_{1-a}N$（$0 \leqq a \leqq 0.5$）で示される窒化物半導体を用いる。バッファ層の膜厚は、好ましくは0.002ー0.5μm、より好ましくは0.005ー0.2μm、さらに好ましくは0.01ー0.02μmとする。バッファ層の成長温度は、好ましくは200ー900℃、より好ましくは400ー800℃である。これにより、窒化物半導体層上の転位やピットを低減させることができる。さらに、上述した異種基板上にELO（Epitaxial Lateral Overgrowth）法により$Al_xGa_{1-x}N$（$0 \leqq X \leqq 1$）層を成長させてもよい。ELO（Epitaxial Lateral Overgrowth）法とは、窒化物半導体を横方向成長させることで貫通転位を曲げて収束させることにより、転位を低減させるものである。バッファ層は多層構成としてもよく、低温成長バッファ層と、その上に高温成長層を形成してもよい。高温成長層としては、アンドープのGaN又はn型不純物をドープしたGaNを用いることができる。高温成長層の膜厚は、1μm以上、より好ましくは3μm以上である。また、高温成長層の成長温度は900ー1100℃、好ましくは1050℃以上でとする。

[0040] 次に、n型窒化物半導体層13を成長させる。まずn型コンタクト層（図示せず）を成長させる。n型コンタクト層としては、活性層14のバンドギャップエネルギーより大きくなる組成であり、$Al_jGa_{1-j}N$（$0 < j < 0.3$）が好ましい。n型コンタクト層の膜厚は特に限定されるものではないが、好ましくは1μm以上、より好ましくは3μm以上である。次に、n型クラッド層を成長させる。n型クラッド層はAlを含有しており、n型不純物濃度は特に限定されるものではないが、好ましくは1×10^{17}ー1×10^{20}／cm^3、より好ましくは1×10^{18}ー1×10^{19}／cm^3である。また、n型不純物濃度に傾斜をつけても良い。また、Alの組成傾斜をつけることで、キャリアの閉じ込めのためのクラッド層としても

機能する。

[0041] 活性層14は発光層として機能し、少なくとも$Al_aIn_bGa_{1-a-b}N$（$0 \leqq a \leqq 1$、$0 \leqq b \leqq 1$、$a+b \leqq 1$）から成る井戸層と、$Al_cIn_dGa_{1-c-d}N$（$0 \leqq c \leqq 1$、$0 \leqq d \leqq 1$、$c+d \leqq 1$）から成る障壁層とを含む量子井戸構造を有する。活性層14に用いられる窒化物半導体は、ノンドープ、n型不純物ドープ、p型不純物ドープのいずれでも良い。好ましくは、ノンドープもしくは、又はn型不純物ドープの窒化物半導体を用いることにより、発光素子を高出力化することができる。さらに好ましくは、井戸層をアンドープとし、障壁層をn型不純物ドープとすることで、発光素子の出力と発光効率を高めることができる。また発光素子に用いる井戸層にAlを含ませることで、従来のInGaNの井戸層では困難な波長域、具体的には、GaNのバンドギャップエネルギーである波長365nm付近、もしくはそれより短い波長を得ることができる。活性層14から放出する光の波長は、発光素子の目的、用途等に応じて360nmー650nm付近、好ましくは380nmー560nmの波長とする。

[0042] 井戸層の膜厚は、好ましくは1nm以上30nm以下、より好ましくは2nm以上20nm以下、さらに好ましくは3．5nm以上20nm以下である。1nmより小さいと井戸層として良好に機能せず、30nmより大きいとInAlGaNの4元混晶の結晶性が低下し素子特性が低下するからである。また、2nm以上では膜厚に大きなむらがなく比較的均一な膜質の層が得られ、20nm以下では結晶欠陥の発生を抑制して結晶成長が可能となる。さらに膜厚を3．5nm以上とすることで出力を向上させることができる。これは井戸層の膜厚を大きくすることで、大電流で駆動させるLDのように多数のキャリア注入に対して、高い発光効率及び内部量子効率により発光再結合がなされるものであり、特に多重量子井戸構造において効果を有する。また、単一量子井戸構造では膜厚を5nm以上とすることで上記と同様に出力を向上させる効果が得られる。また、井戸層の数は特に限定されないが、4以上の場合には井戸層の膜厚を10nm以下として活性層14の膜厚を低く抑えることが好ましい。活性層14を構成する各層の膜厚が厚くなると、活性層14全体の膜厚が厚くなりV_fの上昇を招くからである。多重量子井戸構造の場合、複数の井戸の内、好ましくは上記の10nm以下の範囲にある膜厚の井戸層を少なくとも1つ有すること、より好ましくは全ての井戸層を上記の10nm以

下とすることである。

[0043] また障壁層は、井戸層の場合と同様に、好ましくはp型不純物又はn型不純物がドープされているか又はアンドープとする。より好ましくは、n型不純物がドープされているか又はアンドープとする。例えば、障壁層中にn型不純物をドープする場合、その濃度は少なくとも5×10^{16}／cm^3以上が必要である。例えばLEDでは、5×10^{16}／cm^3以上2×10^{18}／cm^3以下が好ましい。また、高出力のLEDやLDでは、5×10^{17}／cm^3以上1×10^{20}／cm^3以下、より好ましくは1×10^{18}／cm^3以上5×10^{19}／cm^3以下とする。この場合、井戸層はn型不純物を実質的に含有しないか、あるいはアンドープで成長させることが好ましい。また、障壁層にn型不純物をドープする場合、活性層内のすべての障壁層にドープしても良く、あるいは、一部をドープとし一部をアンドープとすることもできる。ここで、一部の障壁層にn型不純物をドープする場合、活性層内でn型層側に配置された障壁層にドープすることが好ましい。例えば、n型層側から数えてn番面の障壁層B_n（nは正の整数）にドープすることで、電子が効率的に活性層内に注入され、優れた発光効率と内部量子効率を有する発光素子が得られる。また、井戸層についても、n型層側から数えてm番目の井戸層W_m（mは正の整数）にドープすることにより上記の障壁層の場合と同様の効果が得られる。また、障壁層と井戸層の両方にドープしても同様の効果が得られる。

[0044] 次に、活性層14上にp型窒化物半導体層15として以下の複数層（図示せず）を形成する。まずp型クラッド層としては、活性層14のバンドギャップエネルギーより大きくなる組成であり、活性層14へのキャリアの閉じ込めができるものであれば特に限定されない。例えば$Al_kGa_{1-k}N$（$0\leqq k<1$）が用いられ、特に$Al_kGa_{1-k}N$（$0<k<0.4$）が好ましい。p型クラッド層の膜厚は特に限定されないが、好ましくは0．01ー0．3μm、より好ましくは0．04ー0．2μmとする。p型クラッド層のp型不純物濃度は、1×10^{18}ー1×10^{21}／cm^3、好ましくは1×10^{19}ー$5\times10^{20}cm^3$とする。p型不純物濃度が上記の範囲にあると、結晶性を低下させることなくバルク抵抗を低下させることができる。p型クラッド層は、単一層でも多層膜層（超格子構造）でも良い。多層膜層の場合、上記の$Al_kGa_{1-k}N$と、それよりバンドギャップエネルギーの小さい窒化物半導体層とからなる多層膜層であれば良い。例えばバンドギャップエネルギーの小さい層として

は、n型クラッド層の場合と同様に、$In_lGa_{1-l}N$（$0 \leqq l < 1$）、$Al_mGa_{1-m}N$（$0 \leqq m < 1$、$m > l$）が挙げられる。多層膜層を形成する各層の膜厚は、超格子構造の場合は、一層の膜厚が好ましくは100Å以下、より好ましくは70Å以下、さらに好ましくは10ー40Åとすることができる。また、p型クラッド層がバンドギャップエネルギーの大きい層と、バンドギャップエネルギーの小さい層からなる多層膜層である場合、バンドギャップエネルギーの大きい層及び小さい層の少なくともいずれか一方にp型不純物をドープさせても良い。また、バンドギャップエネルギーの大きい層及び小さい層の両方にドープする場合は、ドープ量は同一でも異なっても良い。

[0045] 次にp型クラッド層上にp型コンタクト層を形成する。p型コンタクト層は、$Al_fGa_{1-f}N$（$0 \leqq f < 1$）が用いられ、特に、$Al_fGa_{1-f}N$（$0 \leqq f < 0.3$）で構成することにより、オーミック電極であるp電極と良好なオーミックコンタクトが可能となる。p型不純物濃度は1×10^{17}／cm^3以上が好ましい。また、p型コンタクト層は、導電性基板側でp型不純物濃度が高く、かつAlの混晶比が小さくなる組成勾配を有することが好ましい。この場合、組成勾配は、連続的に組成を変化させても、あるいは、不連続に段階的に組成を変化させても良い。例えば、p型コンタクト層を、オーミック電極と接し、p型不純物濃度が高くAl組成比の低い第1のp型コンタクト層と、p型不純物濃度が低くAl組成比の高い第2のp型コンタクト層とで構成することもできる。第1のp型コンタクト層により良好なオーミック接触が得られ、第2のp型コンタクト層により自己吸収を防止することが可能となる。

[0046] 以上のように窒化物半導体を基板11上に成長させた後、ウェハーを反応装置から取り出し、その後、酸素及び／又は窒素を含む雰囲気中で450℃以上で熱処理をする。これによりp型層に結合している水素が取り除かれ、p型の伝導性を示すp型窒化物半導体層15を形成する。

[0047] 窒化物半導体層の積層構造としては、例えば、次の（1）ー（5）に示すものが挙げられる。

（1）GaNよりなるバッファ層（膜厚：200Å）、Siドープn型GaNよりなるn型コンタクト層（4μm）、アンドープ$In_{0.2}Ga_{0.8}N$よりなる単一量子井戸構造の発光層（30Å）、Mgドープp型$Al_{0.1}Ga_{0.9}N$よりなるp型クラッド層（0．2μm）、Mgドープp型GaNよりな

るp型コンタクト層（0．5μm）。

[0048] （2）AlGaNからなるバッファ層（膜厚：約100Å）、アンドープGaN層（1μm）、Siを4．5×10^{18}／cm^3含むGaNからなるn側コンタクト層（5μm）、アンドープGaNからなる下層（3000Å）と、Siを4．5×10^{18}／cm^3含むGaNからなる中間層（300Å）と、アンドープGaNからなる上層（50Å）との3層からなるn側第1多層膜層（総膜厚：3350Å）、アンドープGaN（40Å）とアンドープ$In_{0.1}Ga_{0.9}N$（20Å）とが繰り返し交互に10層ずつ積層されてさらにアンドープGaN（40Å）が積層された超格子構造のn側第2多層膜層（総膜厚：640Å）、アンドープGaNからなる障壁層（250Å）と$In_{0.3}Ga_{0.7}N$からなる井戸層（30Å）とが繰り返し交互に6層ずつ積層されてさらにアンドープGaNからなる障壁層（250Å）が積層された多重量子井戸構造の発光層（総膜厚：1930Å）、Mgを5×10^{19}／cm^3含む$Al_{0.15}Ga_{0.85}N$（40Å）とMgを5×10^{19}／cm^3含む$In_{0.03}Ga_{0.97}N$（25Å）とが繰り返し5層ずつ交互に積層されてさらにMgを5×10^{19}／cm^3含む$Al_{0.15}Ga_{0.85}N$（40Å）が積層された超格子構造のp側多層膜層（総膜厚：365Å）、Mgを1×10^{20}／cm^3含むGaNからなるp側コンタクト層（1200Å）。

[0049] （3）AlGaNからなるバッファ層（膜厚：約100Å）アンドープGaN層（1μm）、Siを4．5×10^{18}／cm^3含むGaNからなるn側コンタクト層（5μm）、アンドープGaNからなる下層（3000Å）と、Siを4．5×10^{18}／cm^3含むGaNからなる中間層（300Å）と、アンドープGaNからなる上層（50Å）との3層からなるn側第1多層膜層（総膜厚：3350Å）、アンドープGaN（40Å）とアンドープ$In_{0.1}Ga_{0.9}N$（20Å）とが繰り返し交互に10層ずつ積層されてさらにアンドープGaN（40Å）が積層された超格子構造のn側第2多層膜層（総膜厚：640Å）、アンドープGaNからなる障壁層（250Å）と$In_{0.3}Ga_{0.7}N$からなる井戸層（30Å）と$In_{0.02}Ga_{0.98}N$からなる第1の障壁層（100Å）とアンドープGaNからなる第2の障壁層（150Å）が繰り返し交互に6層ずつ積層されて形成された多重量子井戸構造の発光層（総膜厚：1930Å）（繰り返し交互に積層する層は3層ー6層の範囲が好ましい）、Mgを5×10^{19}／cm^3含む$Al_{0.15}Ga_{0.85}N$（40Å）とMgを5×10^{19}／cm^3含む$In_{0.03}Ga_{0.97}N$（25Å）とが繰り返し5層ずつ交互に積層されてさらにMgを5×10^{19}／cm^3含む$Al_{0.15}Ga_{0.85}N$（40Å）が積層された超格子構造のp側多層膜層（総膜厚：365Å）、Mgを1×10^{20}／cm^3含むGaNからなるp側コンタクト

層（1200Å）。

[0050] なお、このうち、n側に設けるアンドープGaNからなる下層（3000Å）を、下からアンドープGaNからなる第1の層（1500Å）、Siを5×10^{17}／cm^3含むGaNからなる第2の層（100Å）及びアンドープGaNからなる第3の層（1500Å）からなる3層構造の下層とすることで、発光素子の駆動時間経過に伴うVfの変動を抑えることが可能となる。

[0051] さらに、p側多層膜層とp側コンタクト層との間に、GaN又はAlGaN（2000Å）を形成してもよい。この層は、アンドープで形成され、隣接する層からのMgの拡散によりp型を示す。この層を設けることで、発光素子の静電耐圧が向上する。この層は、静電保護機能を別途設けた発光装置に用いる場合にはなくてもよいが、発光素子外部に静電保護素子等、静電保護手段を設けない場合には、静電耐圧を向上させることができるので、設けることが好ましい。

[0052] （4）バッファ層、アンドープGaN層、Siを6.0×10^{18}／cm^3含むGaNからなるn側コンタクト層、アンドープGaN層（以上が総膜厚6nmのn型窒化物半導体層）、Siを2.0×10^{18}／cm^3含むGaN障壁層とInGaN井戸層とを繰り返し5層ずつ交互に積層された多重量子井戸の発光層（総膜厚：1000Å）、Mgを5.0×10^{18}／cm^3含むGaNからなるp型窒化物半導体層（膜厚：1300Å）。

[0053] さらに、p型窒化物半導体層の上にInGaN層（30ー100Å、好ましくは50Å）を有してもよい。これにより、このInGaN層が電極と接するp側コンタクト層となる。

[0054] （5）バッファ層、アンドープGaN層、Siを1.3×10^{19}／cm^3含むGaNからなるn側コンタクト層、アンドープGaN層（以上が総膜厚6nmのn型窒化物半導体層）、Siを3.0×10^{18}／cm^3含むGaN障壁層とInGaN井戸層とを繰り返し7層ずつ交互に積層された多重量子井戸の発光層（総膜厚：800Å）、Mgを2.5×10^{20}／cm^3含むGaNからなるp型窒化物半導体層。このp型窒化物半導体層の上には、p側コンタクト層として、InGaN層（30ー100Å、好ましくは50Å）を形成してもよい。

[0055] ［透光性導電層17］

このようにして成長されたp型窒化物半導体層15上に、透光性導電層17を形成する。なお透光性とは、発光素子の発光波長を透過できるという意味であって、必ずし

も無色透明を意味するものではない。透光性導電層17は、オーミック接触を得るために、好ましくは酸素を含むものとする。酸素を含む透光性導電層17には数々の種類があるが、特に好ましくは亜鉛(Zn)、インジウム(In)、スズ(Sn)よりなる群から選択された少なくとも一種の元素を含む酸化物とする。具体的には、ITO、ZnO、In_2O_3、SnO_2等、Zn、In、Snの酸化物を含む透光性導電層17を形成することが望ましく、好ましくはITOを使用する。またさらに、Ni等の金属を透光性を有するように薄膜で形成後、ITOを形成した透光性導電層17としてもよい。

[0056] 透光性導電層17の中に酸素原子を含ませるには、酸素原子を含有させる層を形成した後、酸素を含む雰囲気にて熱処理すればよい。あるいは、反応性スパッタリング、イオンビームアシスト蒸着等により、それぞれの層に酸素原子を含有させることもできる。

[0057] 窒化物半導体層に金属膜等の反射層16を接触させず、透光性導電層17を介在させることで窒化物半導体層との界面でオーミック接触を取ることができる。特にp型窒化物半導体層15は抵抗が高い傾向にあるため、この界面との接触抵抗を低減することは重要となる。さらに、透光性導電層17に凹凸面22を設けることによって、窒化物半導体に直接凹凸を設ける必要をなくし、これによって電気特性を悪化させる原因となる困難な加工を回避しつつ凹凸面22を形成できる。

[0058] [凹凸面22]

透光性導電層17の表面に、凹凸面22を形成する。凹凸面22の形成は、レジストパターンの上からRIE(reactiveion etching)やイオンミリング(ion milling)等の方法によりエッチング等で行う。図3の例では、等脚台形状の傾斜面を備えるメサ型のディンプルを複数設けたパターンの凹凸面22としている。このような凹凸パターンの形成によって、光の取り出し効率が改善される様子を図4に基づいて説明する。図4(a)、(b)は、上面を主光取り出し面、下面を反射面、すなわち下方に向かう光を上側から取り出すために光を反射させる面とする発光素子を示している。図4(a)に示すように、発光部を備える発光素子の反射面が平坦の場合は、反射面で反射される光は入射角と出射角が等しくなるので、主光取出し面の法線に対して臨界角よりも大きい角度で入射した光は、全反射するため発光素子の上面から取り出せなくなる。

[0059] これに対して、図4(b)に示すように反射面を凹凸面22とすることによって、反射角が変更されるので光の散乱のような効果が生じ、光が反射を続けるうち出射角が臨界角以下となった時点で外部に放出される。この結果、反射光の多くを臨界角以下の角度にして外部に放出させ、光取り出し効率を大幅に改善することができる。

[0060] 凹凸の傾斜面の傾斜角度は、主光取出し面の法線とのなす角度Xを0° ＜X＜65° とすると、光を臨界角以下の角度に反射させる確率を高くでき、光の取り出し効率を改善することができ好ましい。

[0061] 凹凸面22のパターンは、図3や図4のような等脚台形状の他、光の散乱効果が得られる任意の形状が採用できる。例えば、第1の実施の形態の変形例1として、図5に示すような断面を半円状とするシリンドリカルレンズ状の凹凸面22Bを形成しても良い。シリンドリカル形状によって、より効率よく上方向への光が外部に取り出しできる。また第1の実施の形態の変形例2として、図6に示すような三角波状に凹凸面22Cを形成することもできる。これら図5、図6の構成は、図3と異なり透光性導電層17と反射層との界面に平行な平坦面がないので、全反射の生じる領域を極減して、外部取り出し効率をより高めることができる。さらに第1の実施の形態の変形例3として図7に示すような矩形波状の凹凸面22Dとすることもできる。また図示しないが、図5のシリンドリカルレンズ状のパターンを隣接するディンプル同士で離間させて設けたり、断面を円形に変えて楕円形状としてもよい。あるいはディンプルのパターンをストライプ状とする例に限られず、円柱状、三角円錐状、あるいはプリズム状、角柱状等の多角柱状等とすることもできる。あるいはまた、単一のドーム状の凸部、あるいは凹部とすることもできる。以上のようなパターンとすることでも、光取り出し効率を改善することができる。なお本明細書において凹凸とは、必ずしも凹部と凸部を備える場合に限られず、凹部のみあるいは凸部のみの場合も包含することはいうまでもない。

[0062] 更に、これら凹凸面のパターンは、全体で均一なパターンとする必要はなく、必要に応じて複数のパターンを組み合わせたり、あるいは分布密度を変更することができる。例えば、活性層の二次元的な光出力の分布密度に応じて、光強度の強い領域は凹凸面のパターンを密として、より多くの光を外部に取り出せるようにしてもよい。あるいは、3次元的な光の照射パターンに応じて、反射層への光の入射角が主光取り

出し面の法線方向に対して大きい領域においては、例えば図4(b)の傾斜面を急峻にしたり、ディンプルの密度を増す等して、光を臨界角以下の角度で出射できる確率を増すことができる。

[0063] この透光性導電層17の厚さは、凹凸面が形成できる程度の厚さとし、好ましくは1μm以下、さらに好ましくは100Åから5000Åとする。膜厚を1000Åでオーミック性が確認され、厚くするとアニール温度が上昇する傾向にある。また、活性層14から放出される光の波長λに対してλ／4のおよそ整数倍とすることが好ましい。なぜなら、透光性導電層内での光の干渉により、強い光が透光性導電層から放出されるからである。

[0064] 透光性導電層17の表面には凹凸が形成されている。凹凸の形状は特に限定されるものではなく、光の取り出し効率を考慮して適宜調整することができる。例えば、周期的又は不規則な格子状のパターン、円形、多角形、多角形の角が若干の丸みを帯びた略多角形の周期的又は不規則な配列パターンが挙げられる。中でも、凹凸が密に配置することができる三角形、四角形、六角形等の凸形状が好ましい。なお、これらのパターンはその形成方法によって、パターン表面と底面とで異なる形状、つまりパターン表面に近づくにつれて幅が細くなる形状、角が丸みを帯びた形状等であってもよい。周期的なパターンの場合、そのピッチは、例えば1μm程度以下、700nm程度以下、500nm程度以下、300nm程度以下等であることが適当である。凹凸の高さは、特に限定されるものではなく、例えば2μm程度以下、500nm程度以下、好ましくは10ー500nm程度が挙げられる。このような凹凸パターンは、例えば凹部の深さをdとし、パターンの上面の幅をWとするとき、d≦Wの関係を満たすように設定することが好ましい。これにより、光の反射を制御することができ、光の取り出し効率を向上させることができる。

[0065] [反射層16]

以上のようにして凹凸面22が形成された透光性導電層17上に、反射層16を形成する。反射層16は、例えば金属膜で形成できる。金属膜は、酸素を含有する透光性導電層17との接続を良好に行うため、一部が酸化されていることが好ましい。このように金属膜の反射層を透光性導電層17を介して窒化物半導体層と接続することにより

、透光性導電層17は半導体層と良好なオーミック接続を行うことができる。

[0066] また金属膜と窒化物半導体と直接接合をさせると、金属膜から不純物が窒化物半導体層に拡散して汚染される問題や、界面での接合性が悪く剥離等の問題が生じて歩留まりが低下することがある。間に酸化膜を介在させると、酸化膜が保護膜となって拡散が阻止される。加えて、酸化物と金属膜との接着性は一般に悪いが、凹凸面22とすることで接触面積を増やして接着強度を向上できる。

[0067] また界面での光の吸収によって光の取り出し効率が悪化するという問題もある。図8(a)に示すように、透光性導電層17を介することなく直接GaN等の窒化物半導体層23と金属膜24の反射層とを接合させると、金属膜との界面25で光の吸収が生じてしまい、有効に取り出せる光が失われる。吸収率は材質によって異なるが、AlとGaNの場合で約10%となる。これに対して、図8(b)に示すようにITO等の透光性導電層17を介在させることで、窒化物半導体との界面26で光の吸収を抑え、また金属膜24の反射層との界面27での光の吸収も抑制でき、有効に利用できる光を増やして光取り出し効率、外部量子効率を改善して発光出力を高めることができる。これに加えて、上述した界面を凹凸面22とすることで、より多くの光を外部に取り出すことができるようになり、さらに出力が改善される。

[0068] 金属膜の膜厚は、好ましくは200オングストローム以上、さらに好ましくは500オングストローム以上とすることで、十分に光が反射される。特に限定するものではないが、上限としては1μm以下とすればよい。

[0069] 金属膜は、p型窒化物半導体の電極となり、かつ反射率の高い薄膜を形成できる材料を使用する。特にアルミニウム(Al)、銀(Ag)、亜鉛(Zn)、ニッケル(Ni)、白金(Pt)、パラジウム(Pd)、ロジウム(Rh)、ルテニウム(Ru)、オスミウム(Os)、イリジウム(Ir)、チタン(Ti)、ジルコニウム(Zr)、ハフニウム(Hf)、バナジウム(V)、ニオブ(Nb)、タンタル(Ta)、コバルト(Co)、鉄(Fe)、マンガン(Mn)、モリブデン(Mo)、クロム(Cr)、タングステン(W)、ランタン(La)、銅(Cu)、イットリウム(Y)よりなる群から選択された少なくとも一種の元素を含む金属又は合金であって、その単一の層もしくは多層が好ましい。これらの金属又は合金は、窒化物半導体と好ましいオーミック接続が得られ、さらに発光素子の順方向電圧を低下させる上で有用である。特にAl、Ti、Pt、R

h、Ag、Pd、Irよりなる群から選ばれた少なくとも1種を含む層とすることが好ましく、さらに好ましくは高反射が実現できる層として、アルミニウム、ロジウム、銀を含む層とする。特にアルミニウム、ロジウム、銀を本発明の構成に用いると、凹凸面での反射率は70%以上とでき、これによって窒化物半導体よりなる発光素子の360nmー650nm付近、望ましくは380nmー560nmの波長の吸収が少なく、さらに好ましいオーミック接触を得ることができる。また、金属膜の層を上記で列挙した金属の積層構造としてもよい。また後に電極を熱的アニールで処理して、電極材料が金属膜の中で渾然一体となって合金化した状態としてもよい。

[0070] これら透光性導電層17や反射層16は、多層構造としても良い。例えば、多層構造で半導体層側に位置する第二の層の屈折率を、第一の層の屈折率より段階的に小さくすることにより、発光素子からの光の取り出しを向上させることができる。

[0071] [誘電体]

また反射層16を誘電体で構成することもできる。誘電体は、好ましくは酸化物の積層構造とする。酸化物は金属よりも化学的に安定しているので、金属膜の反射層に比べてより信頼性高く使用することができる。また反射率を98%以上、100%に近い値とでき、反射層での光の吸収による損失を極減できる。

[0072] 誘電体で反射膜を構成する場合は、多層構造が採用できる。好ましくは、Si、Zn、Ti、Zr、Hf、Nb、Taの少なくともいずれかを含む誘電体とする。

[0073] さらにまた、誘電体を利用すると、表面へのコーティングが容易となるので、発光素子の実装面のみならず、基板11の主面と交差する面、すなわち図3において発光素子の側面にも誘電体の反射層を設けて、横方向の光を効率よく反射させて取り出すことが可能となる。これにより、半導体の側面に設けられた反射層で横方向からの光を漏れを抑制し、上方への光の取り出し向上に寄与し得る。

[0074] さらに、第1の実施の形態の変形例4として図9に示すように、発光素子の半導体層の側面を傾斜させた傾斜面28とすることで、側面方向に向かう光を上方向に反射して、さらに光取り出し効率を改善できる。この構造は、傾斜面28をドーム状にすることで、出射光を上方向に効果的に反射し、極めて高い光取り出し効率を得ることができる。この傾斜面28はフラットに形成する他、曲面とすることもできる。曲面とする方が、

さらに反射効率を高めることができる。傾斜面28上に誘電体反射層29を形成することで、横方向の光も確実に反射させて有効に出力し、効率を改善する。また、この構成は図示しないが反射層を側面に設けない構成にも適用できる。

[0075] またこれらの層を形成するには、蒸着、スパッタ等の手法により、通常の気相成膜装置を用いて形成できる。また、有機金属気相成長法（MOCVD）、蒸着法、スパッタリング法等、それぞれ異なる成膜方法を使い分けて、各々の層を形成することもできる。またさらにはゾルゲル法により形成することも可能である。例えばある層は蒸着法によって成膜し、他の層はスパッタリング法によって成膜を行ってもよい。特に、金属膜を介することなく窒化物半導体層に直接透光性導電層17を成膜するときには、蒸着法によることが好ましい。このように、成膜方法を使い分けることにより、膜質が向上し透光性電極と窒化物半導体とのオーミック接続が良好となり、更に接触抵抗を下げることができる。また、透光性導電層17と反射層16との界面をパターニングするには、ウェットエッチング、ドライエッチング又はリフトオフ等のパターニング方法を使い分けることにより行うことができる。

[0076] なお、本実施の形態における窒化物半導体発光素子は、p型層に対して透光性導電層17及び反射層16を設けているが、他の形態においてn型層に対して透光性導電層17等を設けてもよいことはいうまでもない。例えば、n型層の側から主に光を取り出す構成とし、n層のパッド電極に凹凸面22を形成し、反射膜を設けてもよい。

[0077] ［パッド電極］

本実施の形態において、パッド電極は、反射層の表面に設けてもよいし、設けなくてもよい。また反射層として機能する層を含めて設けてもよく、p型窒化物半導体層15側及びn型窒化物半導体層13側のうち、一方の窒化物半導体層側に設けられた透光性導電層17及び他方の窒化物半導体層に対して形成される。また本発明に係る他の実施の形態におけるパッド電極の一部は、透光性導電層17に設けた貫通孔内に延在させて窒化物半導体層に直接設けたり、あるいは透光性導電層17の外縁にて窒化物半導体層に直接設けてもよい。このように、パッド電極の一部が窒化物半導体層に直接設けられることによってパッド電極の剥離を防止することができる。

[0078] パッド電極表面にAuバンプのような導電部材を配置し、導電部材を介して対向さ

れた発光素子の電極と外部電極との電気的接続を図ることができる。

[0079] また、p型窒化物半導体層15側及びn型窒化物半導体層13側に形成されるパッド電極は、用いる金属の種類や膜厚が同じ構成とすることが好ましい。このように同じ構成とすることによって、p型窒化物半導体層15側及びn型窒化物半導体層13側とで同時にパッド電極を形成することができるため、p型窒化物半導体層15側及びn型窒化物半導体層13側とを別々に形成する場合と比較して、パッド電極の形成の工程を簡略化することができる。本実施の形態におけるパッド電極として、例えば、p型窒化物半導体層15あるいはn型窒化物半導体層13側からTi、Rh、Pt、Auのそれぞれをスパッタリングにより順に積層させたTi／Rh／Pt／Au電極やW、Pt、Auのそれぞれをスパッタリングにより順に積層させたW／Pt／Au電極（その膜厚として、例えばそれぞれ20nm／200nm／500nm）が挙げられる。パッド電極の最上層をAuとすることによって、パッド電極は、Auを主成分とする導電性ワイヤと良好な接続ができる。また、RhとAuの間にPtを積層させることによって、AuあるいはRhの拡散を防止することができる。また、Rhは、光反射性及びバリア性に優れ、光取り出し効率が向上するため好適に用いることができる。

[0080] 発光素子としてLEDやレーザを作成する場合、一般的には特定の基板上に各半導体層を成長させて形成されるが、その際、基板としてサファイア等の絶縁性基板を用いその絶縁性基板を最終的に取り除かない場合、通常、p電極及びn電極はいずれも半導体層上の同一面側に形成される。これによって、絶縁性基板側を視認側に配置し発光された光を基板側から取り出すフリップチップ実装が実現される。もちろん、最終的に基板を除去した上で、フリップチップ実装することもできる。このように、光の取り出し効率を良くし、外部量子効率を改善してより大きな発光パワーを得ることができる。

（実施の形態2）

[0081] 本発明の別の実施の形態に係る半導体素子は、対向する一対の主面を有する基板11と、前記基板11の一方の主面上に第1の伝導型半導体層と、前記第1の伝導型半導体層上に第2の伝導型半導体層と、前記第1の伝導型半導体層と第2の伝導型半導体層との間に形成される活性層14と、前記第2の伝導型半導体層上に形成

され、前記活性層14から前記第2の伝導型半導体層に向かう光を反射させるための反射層16とを備える。

[0082] この半導体素子は、発光素子として、上記基板11の他方の主面を主光取出し面として配線基板に実装可能である。さらに、前記反射層16と第2の伝導型半導体層との間に透光性導電層17が形成されており、透光性導電層17は、少なくとも亜鉛、インジウム、スズ及びマグネシウムよりなる群から選択された少なくとも一種の元素Cと、微量元素Dを含む。この構成により、半導体層中の活性層から出た光が透光性導電層を通過し、好適に反射層で反射し、外部に光が取り出される。特に、酸化物膜からなる透光性導電層を、半導体層との界面近傍における微量元素Dが、酸化物膜の他の部分の膜中微量元素Dの濃度よりも高くすることで、半導体層の界面近傍において、キャリアを多く有することになる。この微量元素Dは、膜厚方向において、特有の濃度分布を持つことで、結晶性及び導電性に優れた導電性酸化物膜とすることができる。詳しくは、微量元素Dが多すぎると導電性は良くなる傾向にあるが、結晶性が悪くなり、透光性の電極として好ましくない。すなわち、微量元素Dは膜厚方向において、濃度の高い領域と低い領域とが共存することが好ましい。特に、半導体層との界面近傍における膜中微量元素Dの濃度が、導電性酸化物膜の他の部分の膜中微量元素Dの濃度よりも高いことがさらに好ましい。例えば、導電性酸化物膜がITOの場合、微量元素Dはスズとなる。ITOは、酸素欠損量が多いことで高いキャリア濃度が得られると共に、スズのドープ量が多いことでも高いキャリア濃度が得られる。ただし、スズのドープ量が多すぎるとキャリアは高くなるが、結晶性が悪くなり、一般に透光性の電極としては好ましくない。しかし本発明の実施の形態では、半導体層との界面近傍においてスズのドープ量が多いことで、導電性酸化物膜と半導体層との間において良好なオーミックコンタクトが得られると共に、他の領域でではスズのドープ量が少ないことで、良好な結晶性の膜となるので好ましい。この様子をAES（オージェ電子分光）分析装置により測定すると、図10のような傾向になる。図10は、ITO膜中のスズのデプスプロファイルを示すグラフである。デプスプロファイルとは、物質の表面から物質内部に向かっての元素濃度の変化、深さ方向の濃度分布の事をいう。図10（a）は、連続的にスズ濃度の濃度勾配がある場合、（b）は総括したスズ濃度の傾向を示す図

である。またスズのドープ量を、移動度の高い状態を維持した範囲で、つまり導電性が最も良い状態のドープ量のスズを半導体層との界面近傍に設けることで、導電性酸化物膜に投入された電流を膜全体に拡散させ、さらに半導体層に均一に拡散させることができる膜となり、好ましい。

[0083] また、半導体層との界面近傍における膜中微量元素Dの濃度が、その界面に対向する面近傍の微量元素Dの濃度よりも高いことがさらに好ましい。導電性酸化物膜は、半導体層との界面に対向する面には、反射膜を有し、その反射膜が接してなることで半導体層中の活性層から出た光が導電性酸化物膜を通過し、好適に反射層で反射する。特に反射層が、アルミニウム、チタン、白金、ロジウム、銀、パラジウム、イリジウム、ケイ素、亜鉛から選択される少なくとも一種の元素を含む場合、これらの反射層は、半導体層と比べて導電性がよく、キャリアが多く存在するために、導電性酸化物膜とのショットキー障壁は小さく、オーミックコンタクトも比較的得られやすい。そのような界面においてはスズのドープ量を抑え、結晶性を良好にすることで、反射層としての機能を十分に発揮することができる。これは導電性酸化物膜の表面状態を考慮してもいえることで、元素Cを含む酸化物からなる導電性酸化物膜に微量元素Dを有する場合、微量元素Dを多く有すると荒れた表面状態となる。この表面状態は、微量元素Dによる荒れ状態となるため、このような荒れた表面に反射層を形成すると、反射層としての金属の結晶方位が不安定になるか、良好な界面が形成されにくくなり、良好な反射特性を得るには好ましくない。つまり、金属元素を含む反射層との界面は、キャリアを抑えて結晶性を良好にすることが好ましく、導電性酸化物膜は、半導体層との界面において微量元素Dを多く、反対に金属との界面においては微量元素Dを少なく有することで、オーミック特性に優れ、かつ反射特性つまりは光取り出しの良好な半導体発光素子を得ることができる。

[0084] これら、微量元素Dを含む構成としては、例えばIn_2O_3にドープされたスズ、ZnOにドープされたアルミニウム等がこのような特有の濃度分布の導電性酸化物膜が得られるので好ましい。本発明において、微量元素Dを含む導電性酸化物膜とは、具体的には元素Cに対して、およそ20％以下の元素Dを含むことを意味する。

[0085] また微量元素Dはドープ量を用いて説明したが、半導体素子として微量元素がどの

程度の量を有しているかを示すもので、導電性酸化物膜を成膜する際にその導電性酸化物がどの程度の量の微量元素Dが存在するかではなく、その膜状態においてどの程度の量の微量元素Dが存在するかを示すものであり、熱拡散等による微量元素Dの移動後の状態も含むものである。

[0086] その他、導電性酸化物膜について、元素Cや微量元素Dの好ましい材料については、実施の形態1と同様のものが好ましい。さらに、導電性酸化物膜（透光性導電層17）の中に酸素原子を含ませるには、酸素原子を含有させる層を形成した後、酸素を含む雰囲気にて熱処理すればよい。あるいは、反応性スパッタリング、イオンビームアシスト蒸着等により、酸素原子を含有させることもできる。

[0087] また導電性酸化物膜以外の層構成については、上記実施の形態1と同様の構成が好適に利用できる。図11に、実施の形態2に係る窒化物半導体発光素子の概略断面図を示す。この図に示す窒化物半導体発光素子は、フリップチップ実装であることを示すため、上下逆に表示している。実際の製造工程では、基板11上に各層を形成し、得られた窒化物半導体発光素子を上下逆にして図2のように実装する。実施の形態1と同様の構成、部材等については、同じ符号を付して詳細説明を省略する。

[0088] またさらに加えて、実施の形態1に示した導電性酸化物膜に凹凸を形成することで、微量元素Dが、膜厚方向において、特有の濃度分布を持つ実施の形態2の半導体素子の特性をさらに良好にすることができる。具体的には、凹部となる面と凸部となる面、さらには凹部と凸部とに接する傾斜面とのそれぞれにおいて、微量元素Dの濃度が異なることが好ましい。具体的な例として、微量元素Dが半導体層との界面に対向する面近傍の微量元素Dが、半導体層から離れるにつれて、微量元素Dの濃度が低くなるような導電性酸化物膜とすると、凸部となる面に対して、凹部となる面での微量元素Dの濃度が高くなる。つまり、凸部の面では微量元素Dの濃度が低く、結晶性の良好な面が形成でき、好適な反射特性が得られると共に、凸部となる面では、微量元素Dの濃度が高く、キャリアが多く、反射層と導電性酸化物膜とが良好なオーミックコンタクトとなる。また、傾斜面では、これらの特性が共存され、外部への光取り出し向上と動作電圧の低減の点において最も好ましい。

[0089] 以上、2つの実施の形態を示したが、いずれも半導体素子を窒化物半導体からなる

発光素子として詳説した。また好ましい形態として、第1の伝導型半導体層をn型、第2の伝導型半導体層をp型で示したが、これらに限るものではなく、本発明の特徴部を備えていれば本発明に含まれることは言うまでもない。

実施例 1

[0090] 以下、本発明に係る実施例について詳述する。ここでは実施例1として、図3に示す構成の半導体発光素子としてLEDを作成した。まず、MOVPE反応装置を用い、2インチφのサファイア基板11の上にGaNよりなるバッファ層を200オングストローム、Siドープn型GaNよりなるn型コンタクト層を4μm、ノンドープ$In_{0.2}Ga_{0.8}N$よりなる単一量子井戸構造の活性層14を30オングストローム、Mgドープp型$Al_{0.1}Ga_{0.9}N$よりなるp型クラッド層を0．2μm、Mgドープp型GaNよりなるp型コンタクト層を0．5μmの膜厚で順に成長させた。

[0091] さらにウエハーを反応容器内において、窒素雰囲気とし温度600℃でアニーリングして、p型窒化物半導体層15をさらに低抵抗化した。アニーリング後、ウエハーを反応容器から取り出し、最上層のp型GaNの表面に所定の形状のマスクを形成し、エッチング装置でマスクの上からエッチングを行い、図3に示すようにn型コンタクト層の一部を露出させた。

[0092] 次に、p型窒化物半導体層15の上のマスクを除去し、最上層のp型GaNのほぼ全面に透光性導電層17としてITOを4000Åの膜厚でスパッタした。スパッタ後の透光性導電層17は明らかに透明性となっており、サファイア基板11まで透けて観察できた。このように、露出したp型窒化物半導体層15のほぼ全面に透光性導電層17が形成されることにより、電流をp型窒化物半導体層15全体に均一に広げることができる。しかも透光性導電層17は透光性であるので、電極側を主光取出し面とすることもできる。ITOからなる透光性導電層17を形成後、RIE（反応性イオンエッチング）によりITOに凹凸を形成した。凹凸形成後、さらにスパッタにより反射層16としてRhを1000Åの膜厚で成膜した。ここで、透光性導電層17（ITO）、反射層16（Rh）共に100Wの低出力で、Ar雰囲気中で成膜を行った。透光性導電層17を形成した時点では、ITOの酸素が十分でないため、透過率は低い。また、透光性導電層17（ITO）と反射層16（Rh）のパターニングは、ウェットエッチングで行った。このようにウェットエッチン

グで行うことにより、界面の接触抵抗を低く抑えることができた。

[0093] ここでITOはスパッタ成膜中に300℃程度に加熱した状態で成膜してもよいし、スパッタ成膜中は室温で成膜し、成膜後に加熱処理を行ってもよいし、これらを組み合わせて用いてもよい。加熱処理後のコンタクト特性は良好なオーミック特性を示した。また従来技術と比較してシート抵抗の低いITO膜を含む透光性導電層17が得られた。以上の工程により、シート抵抗が6．5Ω／□、透過率90％程度の高透過率、低抵抗の透光性導電層17を得ることができた。

[0094] 反射層16の形成後、反射層16の表面全面にPt／Auを含むパッド電極を7000Åの膜厚で形成した。なお、このパッド電極は透光性ではない。

[0095] パッド電極を形成した後、露出したn型窒化物半導体層13にTi／Rh／Pt／Auを含むn電極を7000Åの膜厚で形成した。

[0096] 以上のようにして、n型コンタクト層とp型コンタクト層とに電極を形成したウエハーを、320μm角のチップ状に切断し、図2のようにサブマウント10上にフリップチップ実装した。

実施例 2

[0097] 実施例5として、上記実施例1において、反射層16を誘電体とする他は同様にしてLEDを作成した。反射層16は、透光性導電層17上にTiO_2／SiO_2からなる4．5ペアの9層を積層した。膜厚は、発光層から発光される光のピーク波長λをもとに、λ／4の整数倍の値を用いるとよく、ここではλ／4(nm)を用いた。反射層16は、光の入射側、すなわち透光性導電層17に近い側に屈折率の大きい層を配置することで、全反射を生じ易くして反射率を向上できる。このように誘電体の多層膜として、屈折率の大きい層と屈折率の小さい層のペアを繰り返すことで、表面の臨界角を大きくでき、これによって反射する光を増やすことができる。この誘電体を積層した反射層16を使用して、実施例1よりも反射率は140％向上した。

実施例 3

[0098] 実施例3として、上記実施例2において透光性導電層17と反射層16との間に、図12に示すような、n電極と対抗する隅部からLEDチップの隣接した外縁へ向かって円弧状に延伸する補助電極30を形成した。このような補助電極30は、半導体発光素

子に投入された電流を透光性電極全体に拡散させる。補助電極30の材料としては、Rh／Pt／Auをそれぞれの膜厚を1000オングストローム／2000オングストローム／5000オングストロームとして形成した。反射層としても機能する金属（Rh）を形成しているので、反射効率もほとんど低下せず、好ましい補助電極30として用いることができる。その他は実施例2と同様にして半導体発光素子を作成することで、実施例2よりもV_fがさらに低い素子を得ることができた。

実施例 4

[0099] 実施例4として、上記実施例2において反射層として用いる誘電体の材料を、ZrO_2／SiO_2からなる9．5ペアの19層を積層した。膜厚は、発光層から発光される光のピーク波長λをもとに、λ／4（nm）とした。ZrO_2とSiO_2との組み合わせによる多層膜は、TiO_2とSiO_2との組み合わせによる多層膜より屈折率差が小さいために、積層数を増やしている。その他は実施例2と同様にして半導体発光素子を作成したところ、実施例2と同等の特性の素子が得られた。

実施例 5

[0100] 実施例5として、上記実施例1においてTi／Rh／Pt／Auを含むn電極を、ITO／Rh／Pt／Auとし、p型層上に形成されるp電極（透光性導電層／反射層／パッド電極）と同様の構成とし、p電極と同時にn電極も形成した。この構成によって電極形成工程が簡略化されると共に、半導体発光素子の内部を伝播し、n電極に当たった発光層からの光も好適に反射させることができ、光取り出し効率が実施例1よりも向上する。

実施例 6

[0101] 実施例6として、上記実施例4においてTi／Rh／Pt／Auを含むn電極を、ITO／（ZrO_2／SiO_2からなる9．5ペアの19層）／Pt／Auとし、p型層上に形成されるp電極（透光性導電層／反射層／パッド電極）と同様の構成とし、p電極と同時にn電極も形成した。この構成によって電極形成工程が簡略化されるとともに、半導体発光素子の内部を伝播し、n電極に当たった発光層からの光も好適に反射させることができ、光取り出し効率が実施例4よりも向上する。

実施例 7

[0102] 次に実施例7について詳述する。図3に示す構成の半導体発光素子としてLEDを作成した。まず、MOVPE反応装置を用い、2インチφのサファイア基板11の上にAlGaNからなるバッファ層（膜厚：約100Å）、アンドープGaN層（1μm）、Siを4．5×10^{18}／cm^3含むGaNからなるn電極を形成するn型コンタクト層（5μm）、アンドープGaNからなる下層（3000Å）と、Siを4．5×10^{18}／cm^3含むGaNからなる中間層（300Å）と、アンドープGaNからなる上層（50Å）との3層からなるn側第1多層膜層（総膜厚：3350Å）、アンドープGaN（40Å）とアンドープ$In_{0.1}Ga_{0.9}N$（20Å）とが繰り返し交互に10層ずつ積層されてさらにアンドープGaN（40Å）が積層された超格子構造のn側第2多層膜層（総膜厚：640Å）、アンドープGaNからなる障壁層（250Å）と$In_{0.3}Ga_{0.7}N$からなる井戸層（30Å）と$In_{0.02}Ga_{0.98}N$からなる第1の障壁層（100Å）とアンドープGaNからなる第2の障壁層（150Å）が繰り返し交互に6層ずつ積層されて形成された多重量子井戸構造の発光層（総膜厚：1930Å）、Mgを5×10^{19}／cm^3含む$Al_{0.15}Ga_{0.85}N$（40Å）とMgを5×10^{19}／cm^3含む$In_{0.03}Ga_{0.97}N$（25Å）とが繰り返し5層ずつ交互に積層されてさらにMgを5×10^{19}／cm^3含む$Al_{0.15}Ga_{0.85}N$（40Å）が積層された超格子構造のp側多層膜層（総膜厚：365Å）、Mgを1×10^{20}／cm^3含むGaNからなる表面にp電極を形成するp型コンタクト層（1200Å）を順に成長させた。ここではアンドープGaNからなる下層（3000Å）を、下からアンドープGaNからなる第1の層（1500Å）、Siを5×10^{17}／cm^3含むGaNからなる第2の層（100Å）及びアンドープGaNからなる第3の層（1500Å）からなる3層構造の下層とし、さらに、p側多層膜層とp側コンタクト層との間に、GaN（2000Å）を、アンドープで形成後、隣接する層からのMgの拡散によりp型を示すp型半導体層を形成する。

[0103] さらにウエハーを反応容器内において、窒素雰囲気とし温度600℃でアニーリングして、p型窒化物半導体層15をさらに低抵抗化した。アニーリング後、ウエハーを反応容器から取り出し、最上層のp型GaNの表面に所定の形状のマスクを形成し、エッチング装置でマスクの上からエッチングを行い、図3に示すようにn型コンタクト層の一部を露出させた。

[0104] 次に、p型窒化物半導体層15の上のマスクを除去し、最上層のp型GaNのほぼ全

面に透光性導電層17としてITOを4000Åの膜厚でスパッタした。スパッタ後の透光性導電層17は明らかに透明性となっており、サファイア基板11まで透けて観察できた。このように、露出したp型窒化物半導体層15のほぼ全面に透光性導電層17が形成されることにより、電流をp型窒化物半導体層15全体に均一に広げることができる。しかも透光性導電層17は透光性であるので、電極側を主光取出し面とすることもできる。ITOからなる透光性導電層17を形成後、スパッタにより反射層16としてRhを1000Åの膜厚で成膜した。ここで、透光性導電層17(ITO)、反射層16(Rh)共に100Wの低出力で、Ar雰囲気中で成膜を行った。また、透光性導電層17(ITO)と反射層16(Rh)のパターニングは、ウェットエッチングで行った。このようにウェットエッチングで行うことにより、界面の接触抵抗を低く抑えることができた。

[0105] ここでITOはスパッタ成膜中に300℃程度に加熱した状態で成膜してもよいし、スパッタ成膜中は室温で成膜し、成膜後に加熱処理を行ってもよいが、本実施例では、加熱処理において、ITOのスズがp型コンタクト層との界面近傍において、ITOの他の部分のスズの濃度よりも高くなるように処理した。ITOのスズについてAES分析装置で膜厚方向に測定した結果、図10(a)に示すように、半導体層との界面近傍において、スズの濃度が高くなっていることが確認された。以上の工程により、高透過率、低抵抗の透光性導電層17を得ることができた。

[0106] 反射層16の形成後、反射層16の表面全面と、露出したn型窒化物半導体層13にTi/Rh/Pt/Auを7000Åの膜厚で形成した。

[0107] 以上のようにして、n型コンタクト層とp型コンタクト層とに電極を形成したウエハーを、320μm角のチップ状に切断し、図2のようにサブマウント10上にフリップチップ実装した。従来のITOを用いた場合と比べて、外部への光取り出し効率が向上し、動作電圧の低減した素子が得られる。

実施例 8

[0108] 次に実施例8について、電極形成面側の平面図を示した図13に基づいて説明する。実施例8に係る半導体素子は、図13に示すように、p型窒化物半導体層の間にn型窒化物半導体層がエッチングによりストライプ状に露出されている。露出されたn型窒化物半導体層は、素子の内側において、細くなる形状を有しており、この露出され

たn型半導体層上にn電極8が形成されている。なお、p側の透光性導電層（ITO）17と反射層（Rh）16は、ストライプ形状であり、発光素子中央部分において、露出されたn型窒化物半導体層の幅より広い形状を有している。p側の透光性導電層は、実施例7と同様のITOにより形成されている。p側の透光性導電層17及び反射層16のストライプ列数は、n型窒化物半導体層状のn電極（Ti／Rh／Pt／Au）8の列数より多い。その他は実施例7と同様にして半導体発光素子を得る。なお、図13では、透光性導電層17の上に反射層16が形成されているので、平面図では反射層16のみが見えるようになる。

[0109] このように、n電極がくびれた形状を有することによりp側の透光性導電層と反射層の領域面積を大きくすることができ、単位時間当たりに発光素子に投入される電流量を増大させることができる。さらに発光面において、発光素子の発光に寄与しないn型窒化物半導体層の面積を減らし、p型窒化物半導体層の面積を相対的に増やすことで発光素子の光取り出し効率を向上させることができる。したがって、この発光素子では、高輝度を実現することができる。また透光性導電層をこのように設けることにより、発光素子に投入される電流を均一に発光素子全面に拡散させることができ、発光素子の発光面からの発光を均一とすることができる。

[0110] なお、p側の反射層上に形成されるパッド電極及びn電極は、バンプに含有される材料の少なくとも一種を含有することが好ましい。例えば、バンプがAuを材料とするときには、p側のパッド電極及びn電極の材料、特にバンプと直接に接する接合面の材料は、Au又はAuを含む合金とすることが好ましい。また、Ag、Al、Rh、Rh／Irの単層又は多層膜でもよい。

実施例 9

[0111] さらに実施例9に係る半導体発光素子は、上記実施例7で得られる発光素子の透光性導電層の表面に、実施例1で示したように凹凸を形成し、その凹凸上に反射層を形成した他は、実施例7と同様にして半導体発光素子を得た。これによって得られた半導体発光素子は、さらに外部への光取り出し効率が向上し、動作電圧の低減した素子が得られた。

実施例 10

[0112] さらに実施例10に係る半導体素子を説明する。この半導体素子も、図13に示す電極形成面側の平面図で示したように、p型窒化物半導体層の間にn型窒化物半導体層がエッチングによりストライプ状に露出されている。露出されたn型窒化物半導体層は、素子の内側において、細くなる形状を有しており、この露出されたn型半導体層上にn電極が形成されている。なお、p側の透光性導電層（ITO）と反射層（Rh）は、ストライプ形状であり、発光素子中央部分において、露出されたn型窒化物半導体層の幅より広い形状を有している。p側の透光性導電層は、上記実施例7と同様のITOにより形成されている。p側の透光性導電層及び反射層のストライプ列数は、n型窒化物半導体層状のn電極（Ti／Rh／Pt／Au）の列数より多い。その他は上記実施例9と同様にして半導体発光素子を得た。

[0113] このように、n電極がくびれた形状を有することによりp側の透光性導電層と反射層の領域面積を大きくすることができ、単位時間当たりに発光素子に投入される電流量を増大させることができる。さらに発光面において、発光素子の発光に寄与しないn型窒化物半導体層の面積を減らし、p型窒化物半導体層の面積を相対的に増やすことで発光素子の光取り出し効率を向上させることができる。したがって、この発光素子では、高輝度を実現することができる。また透光性導電層をこのように設けることにより、発光素子に投入される電流を均一に発光素子全面に拡散させることができ、発光素子の発光面からの発光を均一とすることができる。

[0114] なお、p側の反射層上に形成されるパッド電極及びn電極は、バンプに含有される材料の少なくとも一種を含有することが好ましい。例えば、バンプがAuを材料とするときには、p側のパッド電極及びn電極の材料、特にバンプと直接に接する接合面の材料は、Au又はAuを含む合金とすることが好ましい。また、Ag、Al、Rh、Rh／Irの単層又は多層膜でもよい。

[0115] 以上、実施例1から示したすべての実施例のように、窒化物半導体発光素子をフリップチップでマウント基板上に形成することによって、複数の窒化物半導体発光素子を等電位で実装でき、フェイスアップで実装するよりも、窒化物半導体発光装置の小型化が図れる。特にフェイスアップ実装にすると、パッド電極が光遮光部となってしまい、発光面積が減ってしまうが、フリップチップ実装では基板11の裏面側全面を発光

面とでき、広い面積で発光できる。また接合に共晶合金を用いることで、小型化にしても比較的発光面積を大きく取ることができる。また、透光性導電層17や反射層16の膜厚を調節することで、素子の発光面を水平としたり、水平から傾斜して設けたりすることが容易にできる。

産業上の利用可能性

[0116] 本発明の半導体素子は、発光素子のみならず受光素子等にも適用でき、例えば発光ダイオード(LED)やレーザダイオード(LD)等としてフルカラーLEDディスプレイ、LED信号機、道路情報表示板等のLEDデバイス、あるいは太陽電池、光センサー等の受光素子としてイメージスキャナー等に適用したり、あるいはまた電子デバイス(FET等のトランジスタやパワーデバイス)や、これらを用いた光ディスク用光源等大容量の情報を記憶するDVD等のメディアや通信用の光源、印刷機器、照明用光源等に好適に利用できる。

請求の範囲

[1] 対向する一対の主面を有する基板(11)と、

前記基板(11)の一方の主面上に第1の伝導型半導体層と、

前記第1の伝導型半導体層上に第2の伝導型半導体層と、

前記第1の伝導型半導体層と第2の伝導型半導体層との間に形成される活性層(14)と、

前記第2の伝導型半導体層上に形成され、前記活性層(14)から前記第2の伝導型半導体層に向かう光を反射させるための反射層(16)と、

を備え、上記基板(11)の他方の主面を主光取出し面とする半導体素子であって、

前記反射層(16)と第2の伝導型半導体層との間に透光性導電層(17)が形成されており、前記透光性導電層(17)と前記反射層(16)との界面に凹凸面(22)が形成されてなることを特徴とする半導体素子。

[2] 請求項1に記載の半導体素子であって、

前記透光性導電層(17)と前記第2の伝導型半導体層との界面が略平滑面であることを特徴とする半導体素子。

[3] 請求項1又は2に記載の半導体素子であって、

前記凹凸面(22)が傾斜面を備えており、該傾斜面の傾斜角度が主光取出し面の法線に対して60° 以下であることを特徴とする半導体素子。

[4] 請求項1から3のいずれかに記載の半導体素子であって、

前記凹凸面(22)が連続したシリンドリカルレンズ状であることを特徴とする半導体素子。

[5] 請求項1から4のいずれかに記載の半導体素子であって、

前記透光性導電層(17)は、少なくとも亜鉛、インジウム、スズ及びマグネシウムよりなる群から選択された少なくとも一種の元素Cを含む酸化物膜であることを特徴とする半導体素子。

[6] 請求項5に記載の半導体素子であって、前記酸化物膜は元素Cに加えて、微量元素Dを含むことを特徴とする半導体素子。

[7] 請求項6に記載の半導体素子であって、前記微量元素Dは、スズ、亜鉛、ガリウム、

アルミニウムから選択される少なくとも一種の元素であることを特徴とする半導体素子。

[8] 請求項7に記載の半導体素子であって、前記酸化物膜は、前記半導体層との界面近傍における前記微量元素Dが、前記酸化物膜の他の部分の膜中微量元素Dの濃度よりも高いことを特徴とする半導体素子。

[9] 請求項7又は8に記載の半導体素子であって、前記酸化物膜は、前記半導体層との界面近傍における前記微量元素Dが、前記界面に対向する面近傍の微量元素Dの濃度よりも高いことを特徴とする半導体素子。

[10] 請求項6から9のいずれかに記載の半導体素子であって、前記酸化物膜は元素Cに対して20%以下の元素Dを含むことを特徴とする半導体素子。

[11] 請求項1から10のいずれかに記載の半導体素子であって、
前記透光性導電層(17)はITOからなることを特徴とする半導体素子。

[12] 請求項1から11のいずれかに記載の半導体素子であって、
前記反射層(16)が、アルミニウム、チタン、白金、ロジウム、銀、パラジウム、イリジウム、ケイ素、亜鉛から選択される少なくとも一種の元素を含むことを特徴とする半導体素子。

[13] 請求項1から12のいずれかに記載の半導体素子であって、
前記反射層(16)が、アルミニウムを含む金属膜であることを特徴とする半導体素子。

[14] 請求項1から12のいずれかに記載の半導体素子であって、
前記反射層(16)がSi、Zn、又はTiの少なくともいずれかを含む誘電体であることを特徴とする半導体素子。

[15] 請求項1から14のいずれかに記載の半導体素子であって、
前記透光性導電層(17)の膜厚が、前記活性層(14)から放出される光の波長λに対してλ／4のおよそ整数倍であることを特徴とする半導体素子。

[16] 請求項1から15のいずれかに記載の半導体素子であって、
前記透光性導電層(17)の膜厚が1μm以下であることを特徴とする半導体素子。

[17] 請求項1から16のいずれかに記載の半導体素子であって、
前記反射層(16)を、前記基板(11)の主面と交差する面にも形成してなることを特徴と

する半導体素子。

[18] 請求項1から17のいずれかに記載の半導体素子であって、

前記半導体層の、前記基板(11)の主面と交差する面の少なくとも一部を傾斜させてなることを特徴とする半導体素子。

[19] 請求項1から18のいずれかに記載の半導体素子であって、

前記第1伝導型半導体層はn型半導体層であり、第2伝導型半導体層はp型半導体層であることを特徴とする半導体素子。

[20] 請求項1から19のいずれかに記載の半導体素子であって、

前記第1伝導型半導体層及び第2伝導型半導体層は、窒化物半導体層であることを特徴とする半導体素子。

[21] 対向する一対の主面を有する基板(11)と、

前記基板(11)の一方の主面上に積層される第1の伝導型半導体層と、

前記第1の伝導型半導体層上に積層される第2の伝導型半導体層と、

前記第1の伝導型半導体層と第2の伝導型半導体層との間に形成される活性層(14)と、

前記第2の伝導型半導体層上に形成され、前記活性層(14)から前記第2の伝導型半導体層に向かう光を反射させるための反射層(16)と、

を備え、上記基板(11)の他方の主面を主光取出し面として配線基板に実装可能な半導体素子の製造方法であって、

基板(11)上に、第1の伝導型半導体層と、活性層(14)と、第2の伝導型半導体層を積層するステップと、

前記第2の伝導型半導体層上に透光性導電層(17)を形成するステップと、

前記透光性導電層(17)に凹凸面(22)を形成するステップと、

前記凹凸面(22)の形成された透光性導電層(17)上に反射層(16)を形成するステップと、

を備えることを特徴とする半導体素子の製造方法。

[22] 請求項21に記載の半導体素子の製造方法であって、

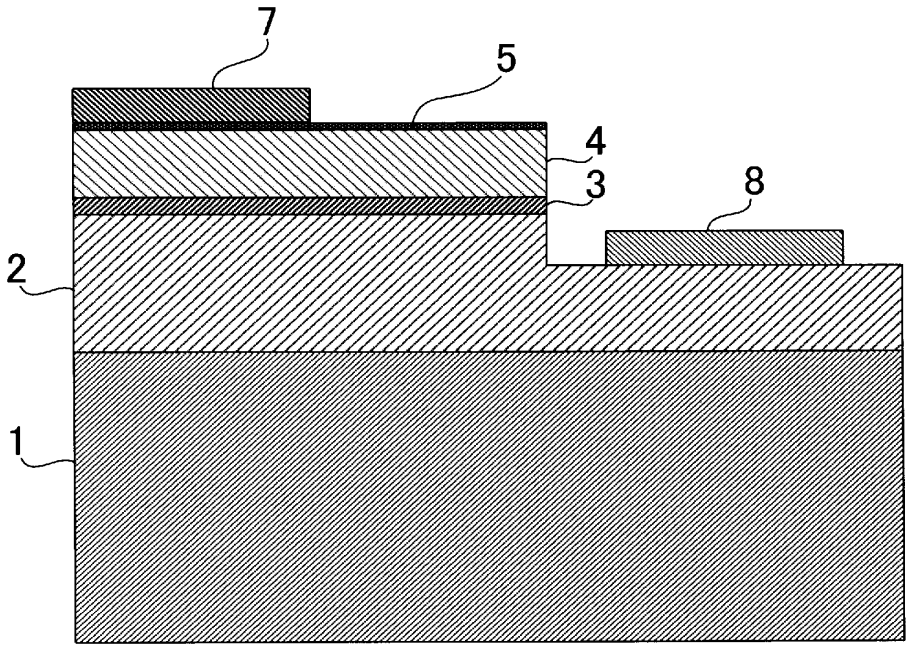
前記透光性導電層(17)は、少なくとも亜鉛、インジウム、スズ及びマグネシウムよりな

る群から選択された少なくとも一種の元素Cと、微量元素Dは、スズ、亜鉛、ガリウム、アルミニウムから選択される少なくとも一種の元素とを含む酸化物膜であることを特徴とする半導体素子の製造方法。

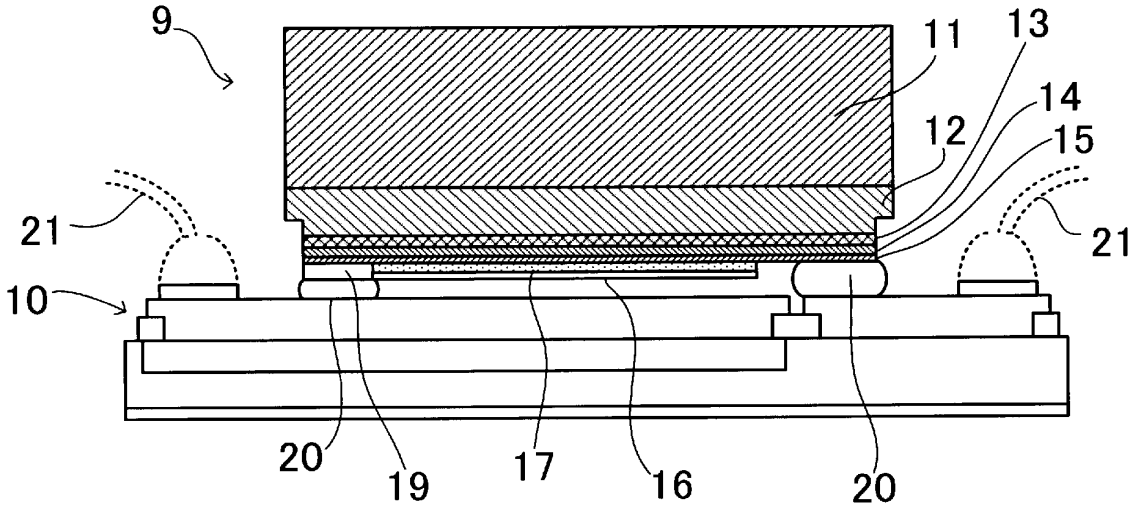
[23] 請求項22に記載の半導体素子の製造方法であって、前記酸化物膜は、前記半導体層との界面近傍における前記微量元素Dが、前記酸化物膜の他の部分の膜中微量元素Dの濃度よりも高いことを特徴とする半導体素子の製造方法。

[24] 請求項22又は23に記載の半導体素子の製造方法であって、前記酸化物膜は、前記半導体層との界面近傍における前記微量元素Dが、前記界面に対向する面近傍の微量元素Dの濃度よりも高いことを特徴とする半導体素子の製造方法。

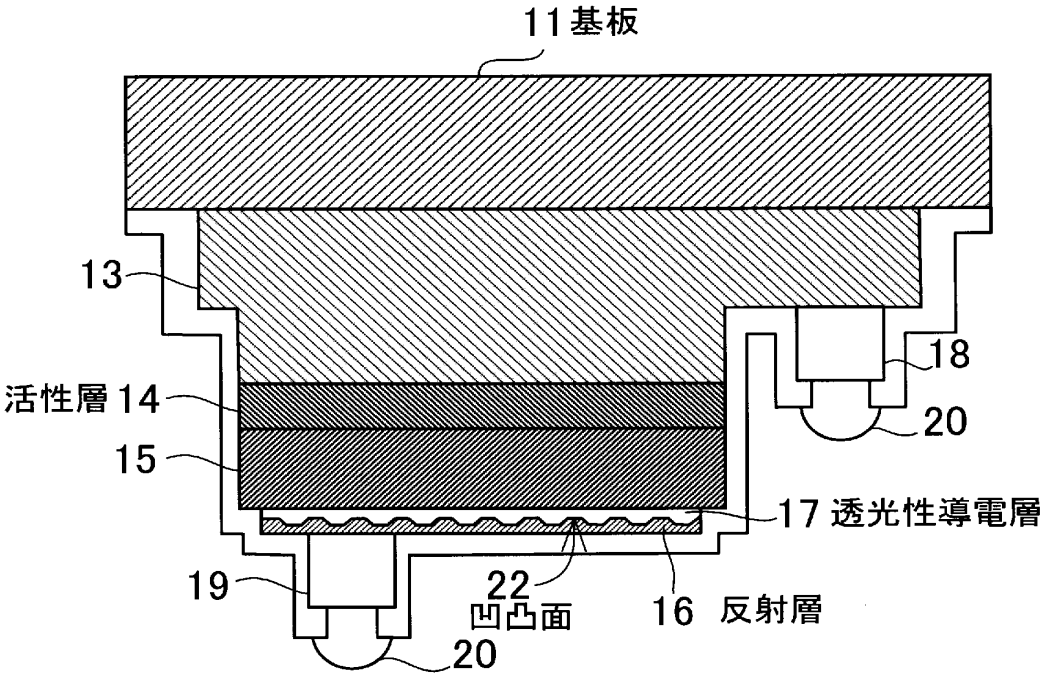
[図1]



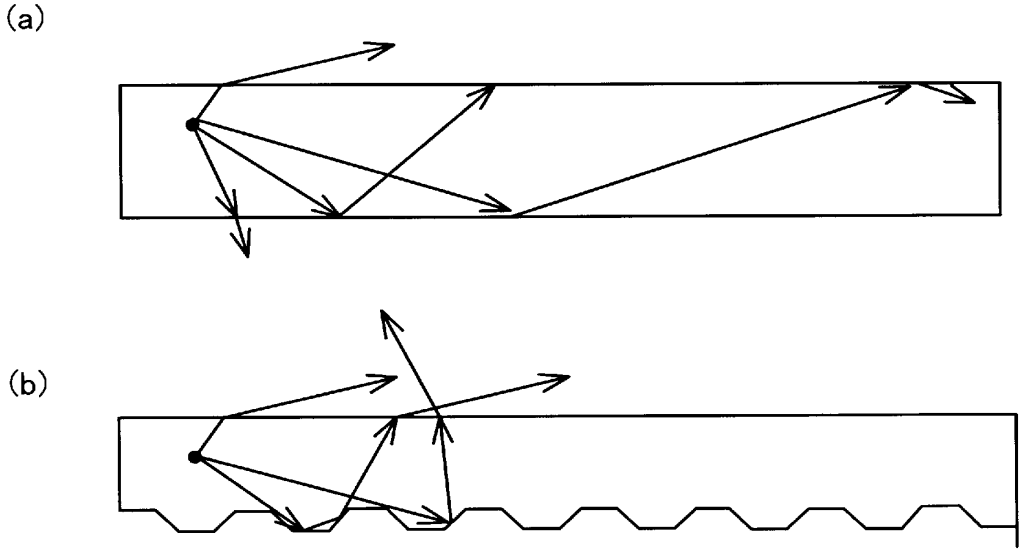
[図2]



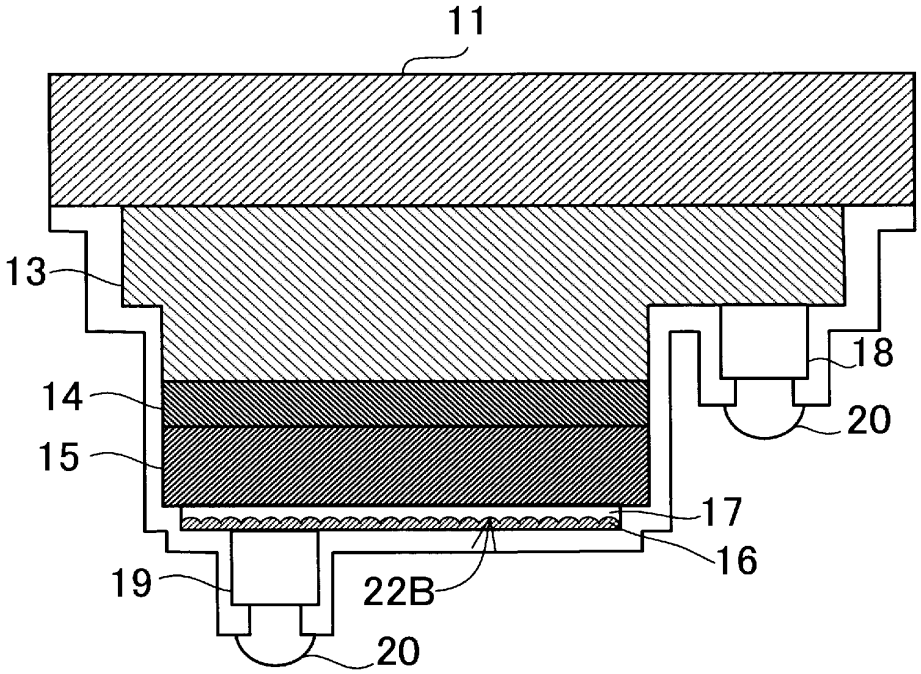
[図3]



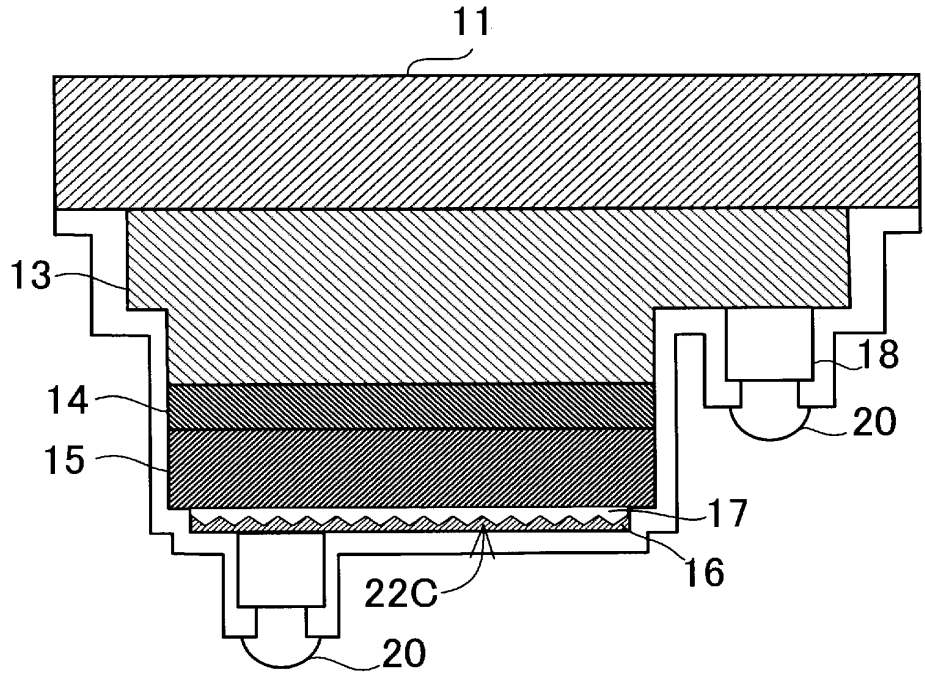
[図4]



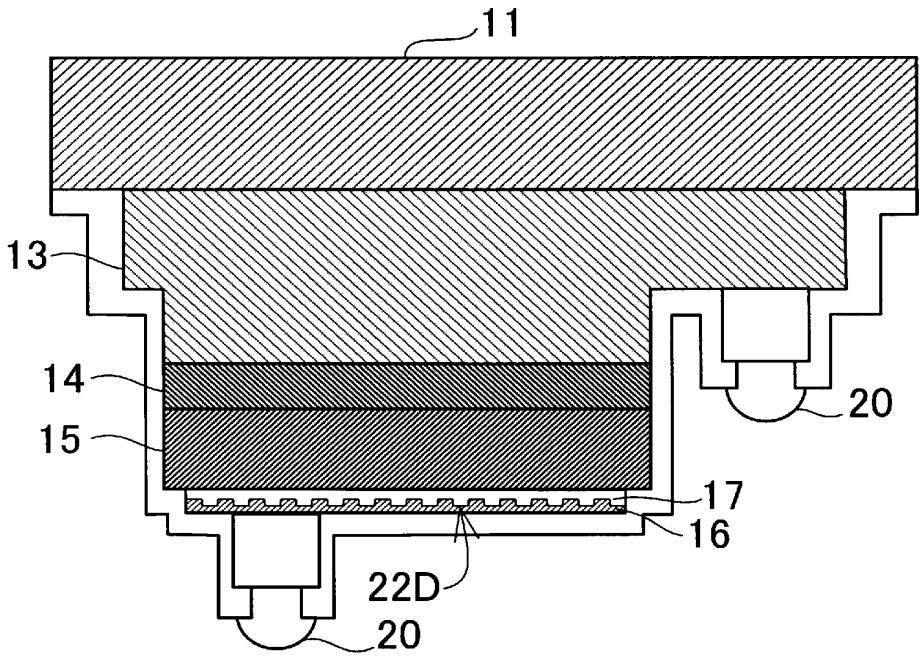
[図5]



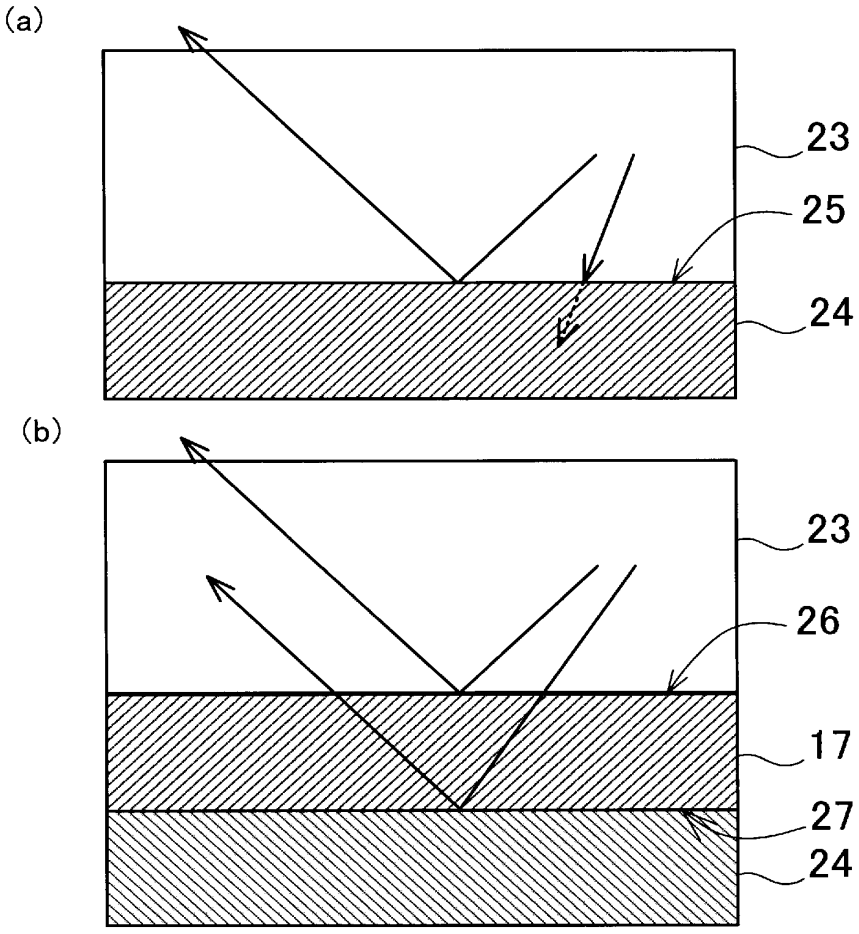
[図6]



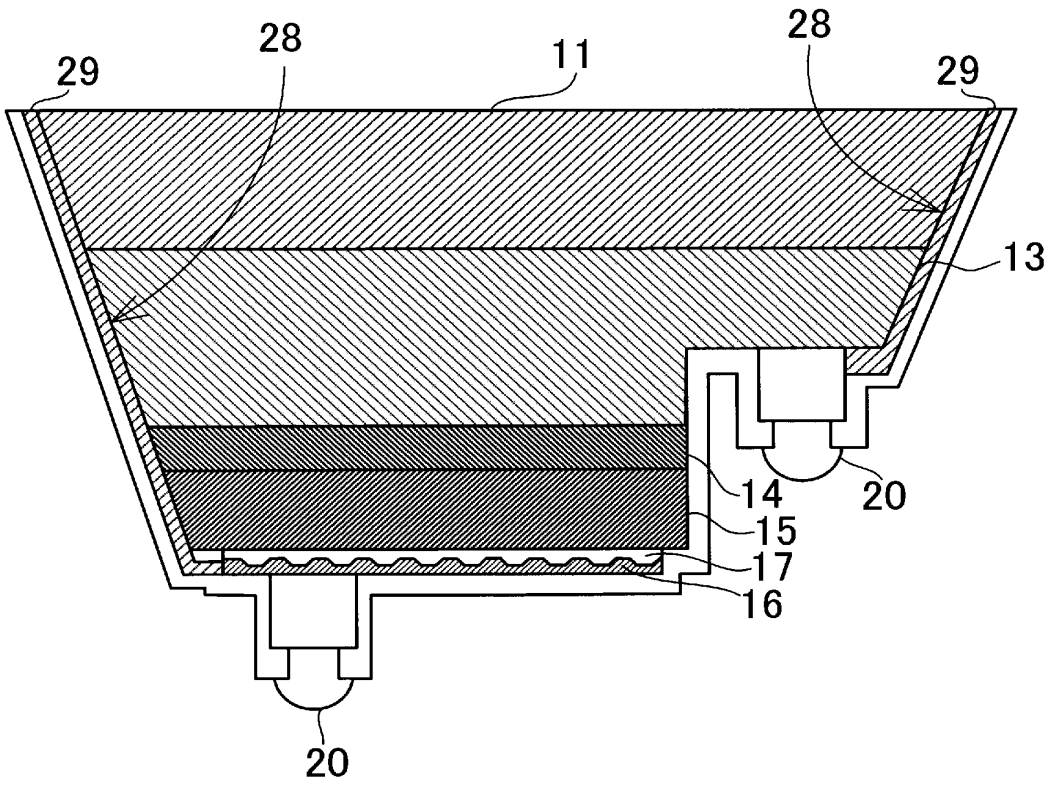
[図7]



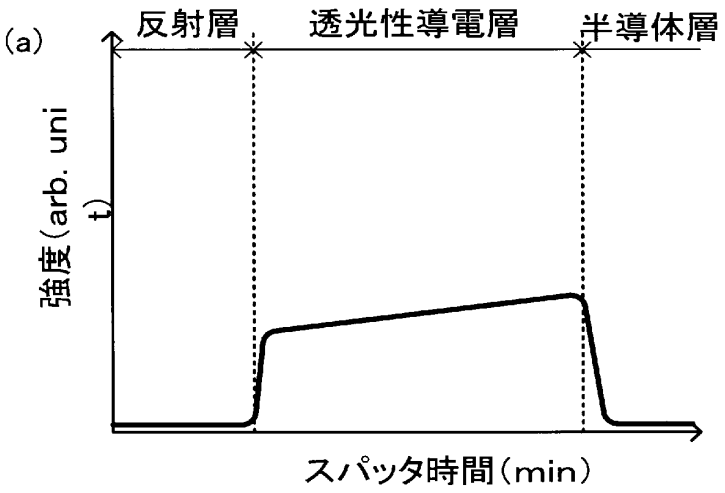
[図8]

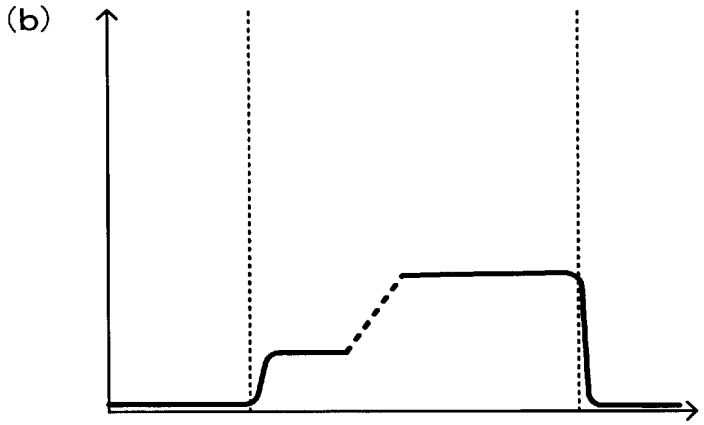


[図9]

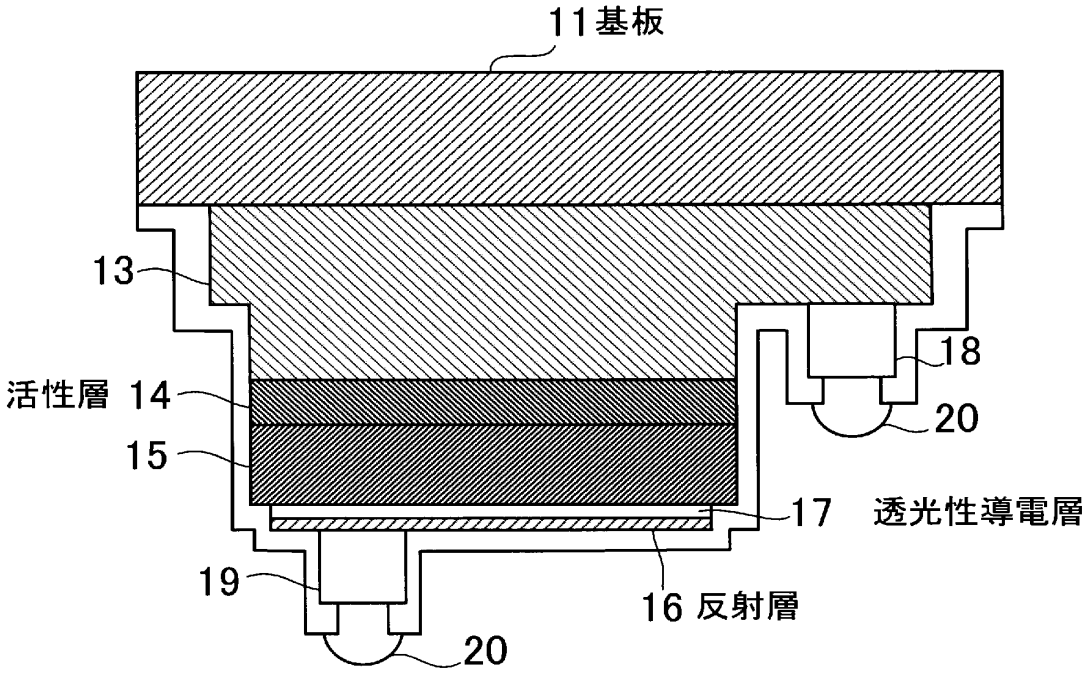


[図10]

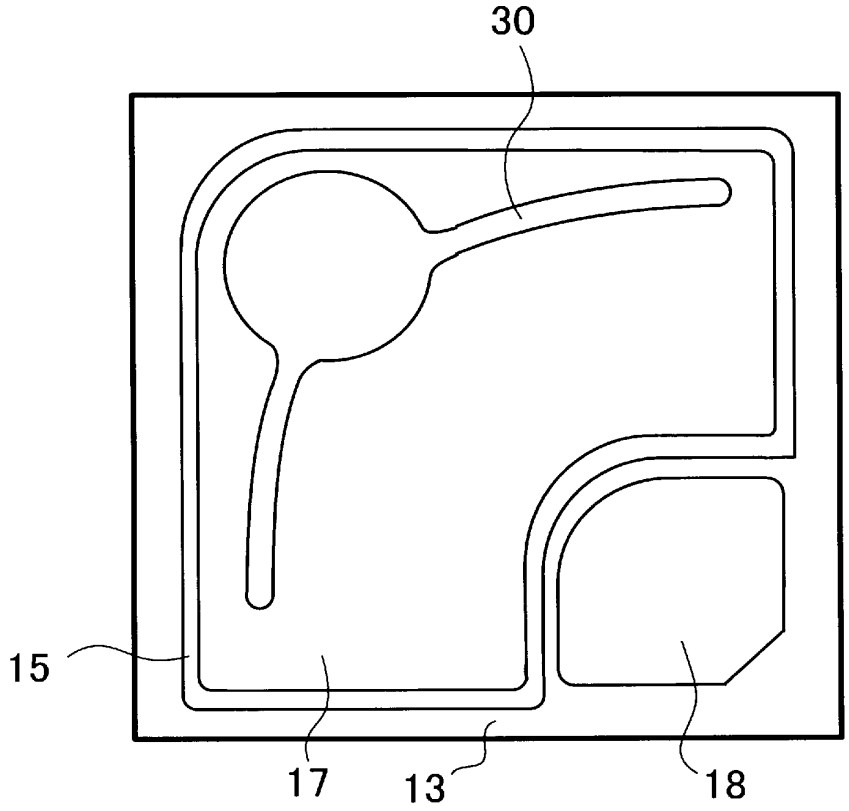




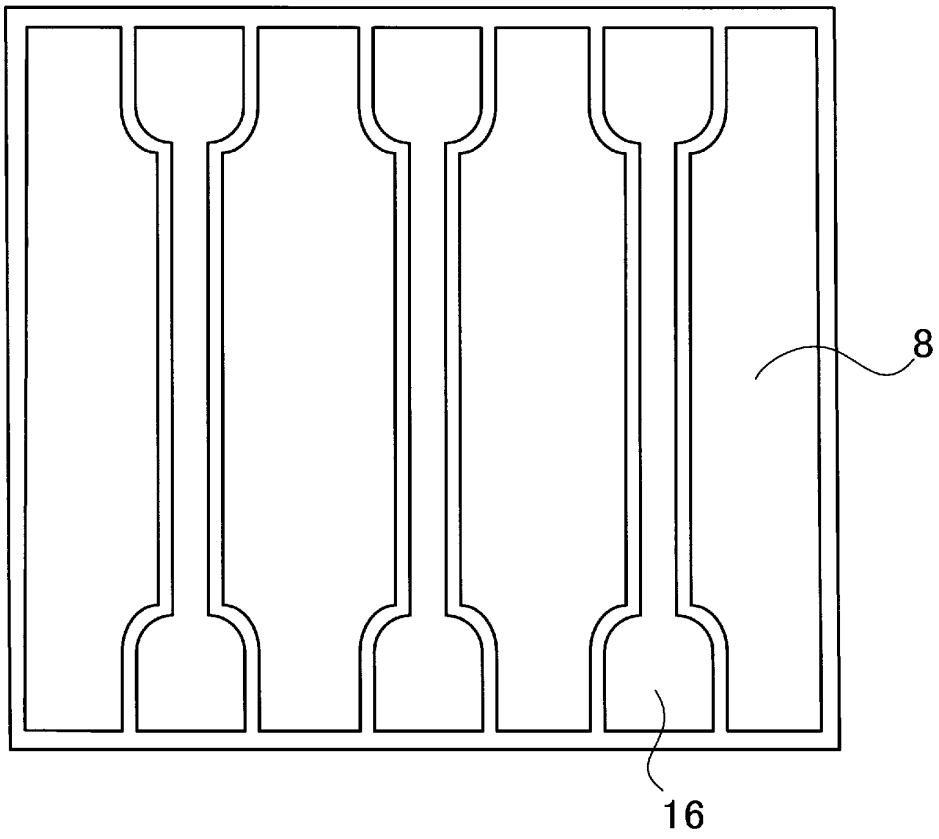
[図11]



[図12]



[図13]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2004/016957

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H01L33/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H01L33/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1922-1996	Toroku Jitsuyo Shinan Koho	1994-2004
Kokai Jitsuyo Shinan Koho	1971-2004	Jitsuyo Shinan Toroku Koho	1996-2004

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2000-196152 A (Toshiba Corp.), 14 July, 2000 (14.07.00), Par. Nos. [0064] to [0072]; Fig. 8 & US 2003/0062530 A1	1-24
A	JP 10-270754 A (Sanyo Electric Co., Ltd.), 09 October, 1998 (09.10.98), Full text; all drawings (Family: none)	1-24
A	JP 3-138893 A (Tokyo Electric Co., Ltd.), 13 June, 1991 (13.06.91), Full text; all drawings (Family: none)	1-24

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
02 February, 2005 (02.02.05)	15 February, 2005 (15.02.05)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (January 2004)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2004/016957

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2002-246648 A (Stanley Electric Co., Ltd.), 30 August, 2002 (30.08.02), Full text; all drawings (Family: none)	1-24

Form PCT/ISA/210 (continuation of second sheet) (January 2004)

国際調査報告	国際出願番号　ＰＣＴ／ＪＰ２００４／０１６９５７

A.　発明の属する分野の分類（国際特許分類（ＩＰＣ））

Ｉｎｔ．Ｃｌ⁷　Ｈ０１Ｌ３３／００

B.　調査を行った分野

調査を行った最小限資料（国際特許分類（ＩＰＣ））

Ｉｎｔ．Ｃｌ⁷　Ｈ０１Ｌ３３／００

最小限資料以外の資料で調査を行った分野に含まれるもの

日本国実用新案公報	１９２２－１９９６年
日本国公開実用新案公報	１９７１－２００４年
日本国登録実用新案公報	１９９４－２００４年
日本国実用新案登録公報	１９９６－２００４年

国際調査で使用した電子データベース（データベースの名称、調査に使用した用語）

C.　関連すると認められる文献

引用文献のカテゴリー＊	引用文献名　及び一部の箇所が関連するときは、その関連する箇所の表示	関連する請求の範囲の番号
Ａ	ＪＰ　２０００－１９６１５２　Ａ（株式会社東芝）２０００．０７．１４，【００６４】－【００７２】欄，図８　＆　ＵＳ　２００３／００６２５３０　Ａ１	１－２４
Ａ	ＪＰ　１０－２７０７５４　Ａ（三洋電機株式会社）１９９８．１０．０９，全文，全図（ファミリーなし）	１－２４
Ａ	ＪＰ　３－１３８８９３　Ａ（東京電気株式会社）１９９１．０６．１３，全文，全図（ファミリーなし）	１－２４

☒ Ｃ欄の続きにも文献が列挙されている。　　☐ パテントファミリーに関する別紙を参照。

＊　引用文献のカテゴリー
「Ａ」特に関連のある文献ではなく、一般的技術水準を示すもの
「Ｅ」国際出願日前の出願または特許であるが、国際出願日以後に公表されたもの
「Ｌ」優先権主張に疑義を提起する文献又は他の文献の発行日若しくは他の特別な理由を確立するために引用する文献（理由を付す）
「Ｏ」口頭による開示、使用、展示等に言及する文献
「Ｐ」国際出願日前で、かつ優先権の主張の基礎となる出願の日の後に公表された文献
「Ｔ」国際出願日又は優先日後に公表された文献であって出願と矛盾するものではなく、発明の原理又は理論の理解のために引用するもの
「Ｘ」特に関連のある文献であって、当該文献のみで発明の新規性又は進歩性がないと考えられるもの
「Ｙ」特に関連のある文献であって、当該文献と他の１以上の文献との、当業者にとって自明である組合せによって進歩性がないと考えられるもの
「＆」同一パテントファミリー文献

国際調査を完了した日	国際調査報告の発送日
０２．０２．２００５	15. 2. 2005

国際調査機関の名称及びあて先	特許庁審査官（権限のある職員）	
日本国特許庁（ＩＳＡ／ＪＰ） 郵便番号１００－８９１５ 東京都千代田区霞が関三丁目４番３号	土屋　知久	２Ｋ　８８２６
	電話番号　０３－３５８１－１１０１　内線　３２５３	

様式ＰＣＴ／ＩＳＡ／２１０（第２ページ）（２００４年１月）

Ｃ（続き）．　関連すると認められる文献

引用文献のカテゴリー＊	引用文献名　及び一部の箇所が関連するときは、その関連する箇所の表示	関連する請求の範囲の番号
Ａ	ＪＰ　２００２－２４６６４８　Ａ（スタンレー電気株式会社）２００２．０８．３０，全文，全図（ファミリーなし）	１－２４

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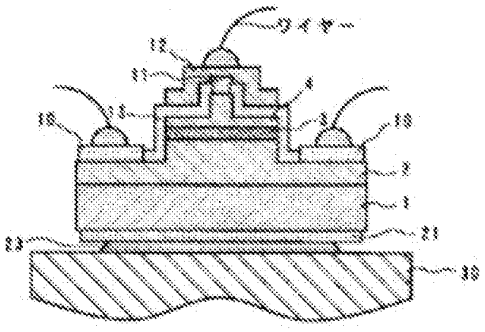
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(54) NITRIDE SEMICONDUCTOR LIGHT-EMITTING ELEMENT

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a light-emitting element wherein adherence of a chip is large and heat dissipating property is high.
SOLUTION: In the light-emitting chip, nitride semiconductor is grown on a first main surface side of an oxide substrate having a first main surface and a second main surface, and a first heat dissipating thin film, including at least one kind of metal selected from among a group composed of Al, Ti, Zr, Cr, I, Mo, W, Ge, Si, Sn, Zn, Cu, Mn, V and Nb, is formed on a second main surface side. The light-emitting chip is die-bonded on a retainer via adhesive agent, having thermal conductivity and electric conductivity in a state with the first heat dissipating thin film facing the surface of the retainer, so that the light-emitting chip is bonded rigidly. In a part between the adhesive agent and the first heat-dissipating thin film, a second heat-dissipating thin film is formed, which contains at least one kind of metal selected from a group composed of Pt, Ti and Ni and whose thickness is nearly equal to or greater that that of the first heat-dissipating thin film.



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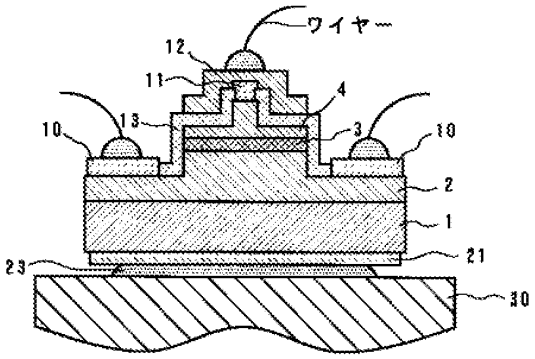
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最終頁に続く

(54)【発明の名称】　窒化物半導体発光素子

(57)【要約】
【課題】　チップの接着性が大きく、かつ放熱性の高い発光素子を提供する。
【解決手段】　第１の主面と第２の主面とを有する酸化物基板の第１の主面側に窒化物半導体が成長され、第２の主面側にＡｌ、Ｔｉ、Ｚｒ、Ｃｒ、Ｎｉ、Ｍｏ、Ｗ、Ｇｅ、Ｓｉ、Ｓｎ、Ｚｎ、Ｃｕ、Ｍｎ、Ｖ、Ｎｂよりなる群から選択された少なくとも一種の金属を含む第１の放熱薄膜が形成された発光チップが、第１の放熱薄膜と支持体表面とが対向した状態で、熱伝導性および導電性を有する接着剤を介して、支持体にダイボンディングされていることにより、発光チップが強固に接着されている。接着剤と第１の放熱薄膜との間には、Ｐｔ、Ｔｉ、Ｎｉよりなる群から選択された少なくとも一種の金属を含み、第１の放熱薄膜の膜厚とほぼ同じか厚い膜厚の第２の放熱薄膜が形成されている。



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【特許請求の範囲】

【請求項１】　第１の主面と第２の主面とを有する酸化物基板の第１の主面側に窒化物半導体が成長され、第２の主面側にＡｌ、Ｔｉ、Ｚｒ、Ｃｒ、Ｎｉ、Ｍｏ、Ｗ、Ｇｅ、Ｓｉ、Ｓｎ、Ｚｎ、Ｃｕ、Ｍｎ、Ｖ、Ｎｂよりなる群から選択された少なくとも一種の金属を含む第１の放熱薄膜が形成された発光チップが、第１の放熱薄膜と支持体表面とが対向した状態で、熱伝導性および導電性を有する接着剤を介して、支持体にダイボンディングされてなる窒化物半導体発光素子であって、

前記熱伝導性および導電性を有する接着剤と、前記第１の放熱薄膜との間にＰｔ、Ｔｉ、Ｎｉよりなる群から選択された少なくとも一種の金属を含み、前記第１の放熱薄膜の膜厚とほぼ同じか、もしくはそれよりも厚い膜厚である第２の放熱薄膜が形成されていることを特徴とする窒化物半導体発光素子。

【請求項２】　前記第１の放熱薄膜の膜厚が、５０オングストローム～１０μｍであることを特徴とする請求項１記載の窒化物半導体発光素子。

【請求項３】　前記第１の放熱薄膜が、Ｔｉ、Ｃｒ、Ｎｉ、Ｚｒよりなる群から選択された少なくとも一種の金属を含むことを特徴とする請求項１又は２に記載の窒化物半導体発光素子。

【請求項４】　前記第１の放熱薄膜がＴｉを含む金属であり、前記第２の放熱膜がＰｔであることを特徴とする請求項１から３のいずれかに記載の窒化物半導体発光素子。

【請求項５】　前記熱伝導性および導電性を有する接着剤はＳｉ、Ｇｅ、Ｓｎよりなる群から選択された少なくとも一種の金属と、Ａｕとを含むことを特徴とする請求項１から４のいずれかに記載の窒化物半導体発光素子。

【請求項６】　前記熱伝導性および導電性を有する接着剤はＳｉとＡｕとを含むことを特徴とする請求項１から５のいずれかに記載の窒化物半導体発光素子。

【請求項７】　前記窒化物半導体発光素子が窒化物半導体発光素子素子であり、前記支持体がヒートシンクであることを特徴とする請求項１から６のいずれかに記載の窒化物半導体発光素子。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明はＬＥＤ、ＬＤ等の発光デバイスに使用される窒化物半導体（$In_XAl_YGa_{1-X-Y}N$、０≦Ｘ、０≦Ｙ、Ｘ＋Ｙ≦１）よりなる発光素子に関する。

【０００２】

【従来の技術】窒化物半導体よりなる光度１ｃｄ以上の高輝度な青色、純緑色ＬＥＤは、最近実用化され、現在本出願人により、製造、販売されて公知となっている。それらのＬＥＤは単一量子井戸構造のＩｎＧａＮよりなる活性層をＡｌＧａＮ及び／又はＧａＮで挟んだｐ－ｎ

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接合を有するダブルヘテロ構造を有し、窒化物半導体はサファイア基板上に成長されている。サファイア基板に成長された窒化物半導体発光チップはフェースアップ（基板と支持体とが対向した状態）で、リードフレームのような支持体にダイボンディングされている。ダイボンディング時の接着剤としては、例えば特開平７－８６６４０号公報に記載されているように、有機物を含む透明な絶縁性の接着剤が使用されている。

【０００３】一方、窒化物半導体よりなるＬＤ（レーザダイオード）については、また本出願人が世界で初めて、４１０ｎｍの室温でのパルス発振を報告した。（例えば、日経エレクトロニクス 1996.1.15 (No.653) p13～p15）。このレーザ素子もサファイア基板の上にＩｎＧａＮを含む多重量子井戸構造よりなる活性層をＡｌＧａＮ、ＧａＮ等で挟んだダブルヘテロ構造を有している。

【０００４】

【発明が解決しようとする課題】透明な絶縁性の接着剤でダイボンディングされたＬＥＤは、接着剤自身が発光を透過するために、ＬＥＤの外部量子効率を向上させる上で非常に効果的である。しかし、有機物を含んでいるため、短波長による有機物の劣化と、長時間の使用により接着剤が変色して外部量子効率を低下させる恐れがある。また、基板と支持体との接着性が不十分であると、ワイヤーボンディング時にチップが支持体から剥がれたり、ずれたりする恐れがある。

【０００５】一方、ＬＤの場合はパルス発振には成功したが、発光チップがヒートシンクのような支持体にダイボンディングされた完成体は未だ開発されていない。ＬＤの場合、ＬＥＤと異なり、チップの発熱量が桁違いに大きい。そのため、発光チップをダイボンディングするには熱伝導性に優れた接着剤を選択する必要がある。さらに、ワイヤーボンディング時に発光チップが支持体から一部剥がれたり、ずれたりすると、接着剤と基板、若しくは接着剤と支持体との間に空隙が存在し、密着性が悪くなる。密着性が悪くなると、発光チップの発熱が十分にヒートシンクに伝わらなくなるので、発振閾値が上昇したり、発光チップの寿命を極端に短くする。

【０００６】従って本発明の目的とするところは、酸化物基板の上に成長された窒化物半導体よりなる発光チップが、ヒートシンク、リードフレームのような支持体にフェースアップでダイボンディングされた発光素子を実現するに際し、チップの接着性が大きく、かつ放熱性の高い発光素子を提供することにある。

【０００７】

【課題を解決するための手段】我々は窒化物半導体よりなる発光チップの基板側に数々の金属薄膜を形成して、ダイボンディングすると接着強度が増大することを発見し、さらに接着強度が強い金属のみを列挙してみたところ、ある特定の金属元素に接着強度を増大させる傾向が

あることを見いだし、本発明をなすに至った。即ち、本発明の窒化物半導体発光素子は、第１の主面と第２の主面とを有する酸化物基板の第１の主面側に窒化物半導体が成長され、第２の主面側にＡｌ、Ｔｉ、Ｚｒ、Ｃｒ、Ｎｉ、Ｍｏ、Ｗ、Ｇｅ、Ｓｉ、Ｓｎ、Ｚｎ、Ｃｕ、Ｍｎ、Ｖ、Ｎｂよりなる群から選択された少なくとも一種の金属を含む第１の放熱薄膜が形成された発光チップが、第１の放熱薄膜と支持体表面とが対向した状態で、熱伝導性および導電性を有する接着剤を介して、支持体にダイボンディングされてなる窒化物半導体発光素子であって、前記熱伝導性および導電性を有する接着剤と、前記第１の放熱薄膜との間にＰｔ、Ｔｉ、Ｎｉよりなる群から選択された少なくとも一種の金属を含み、前記第１の放熱薄膜の膜厚とほぼ同じか、もしくはそれよりも厚い膜厚である第２の放熱薄膜が形成されていることを特徴とする。

【０００８】また、本発明の他の窒化物半導体発光素子は、前記第１の放熱薄膜の膜厚が、５０オングストローム～１０μｍであることを特徴とする。

【０００９】さらに、本発明の他の窒化物半導体発光素子は、前記第１の放熱薄膜が、Ｔｉ、Ｃｒ、Ｎｉ、Ｚｒよりなる群から選択された少なくとも一種の金属を含むことを特徴とする。

【００１０】さらにまた、本発明の他の窒化物半導体発光素子は、前記第１の放熱薄膜がＴｉを含む金属であり、前記第２の放熱膜がＰｔであることを特徴とする。さらにまた、本発明の他の窒化物半導体発光素子は、前記熱伝導性および導電性を有する接着剤はＳｉ、Ｇｅ、Ｓｎよりなる群から選択された少なくとも一種の金属と、Ａｕとを含むことを特徴とする。さらにまた、本発明の他の窒化物半導体発光素子は、前記熱伝導性および導電性を有する接着剤はＳｉとＡｕとを含むことを特徴とする。さらにまた、本発明の他の窒化物半導体発光素子は、前記窒化物半導体発光素子素子であり、前記支持体がヒートシンクであることを特徴とする。

【００１１】

【発明の実施の形態】図１は本発明に係る発光素子の一構造を示す模式的な断面図であり、具体的には、レーザ光の共振方向に垂直な方向で切断したレーザ素子の構造を示している。発光チップの基本的な構造としては、酸化物基板１の第１の主面上にｎ型層２、活性層３、ｐ型層４が順に積層されたダブルヘテロ構造を有しており、さらにｐ型層から上をリッジ形状として、発光がｐ電極１１の下に相当する活性層３に集中するようにされている。発光チップはフェースアップの状態で支持体３０であるヒートシンク若しくはサブマウントに、導電性接着剤２３を介してダイボンディングされており、酸化物基板１の第２の主面側には導電性接着剤２３との接着性を高める目的で、特定の金属よりなる第１の薄膜２１が形成されている。なおｎ電極１０と、ｐ電極１１に電気的に接続されたパッド電極１２とは、それぞれ金線（図ではワイヤーと記載する。）でワイヤーボンディングされている。

【００１２】また基板１が酸化物基板であるので、基板裏面（第２の主面）側にｎ電極を形成することができない。従って第１の主面側にある窒化物半導体層をエッチングして、同一面側にｎ電極１０と、ｐ電極１１とを取り出した構造としている。同一面側にｎ電極１０、ｐ電極１１が形成された窒化物半導体レーザ素子では、この図に示すように、レーザ光の共振方向に対して、ほぼ左右対称にエッチングを行い、そのエッチング面にｎ電極１０を左右対称に２ヶ所設けることにより、閾値電流が低下する傾向にある。さらに、エッチングされて露出したｎ型層２のほぼ全面にｎ電極１０を設けると閾値電圧も低下する傾向にある。

【００１３】さらに、ｐ電極１１に電気的に接続し、ｐ電極よりも表面積が大きいワイヤーボンディング用のパッド電極１２を形成している。パッド電極１２はエッチングにより露出された窒化物半導体層の表面に形成された絶縁膜１３を介して形成する。ｐ電極１１はその表面積がワイヤーボンドできるほど大きくない。従って、ｐ電極１１と電気的に接続したパッド電極１２を設けることにより、ｐ電極にワイヤーボンディングできるようにしている。なお、ｐ電極１１は最上層のｐ型層４にオーミック接触する必要があるため、その材料が限定されるが、パッド電極１２はｐ電極１１と強固に接着できて、導電性の良好な材料であればどのような材料でもよい。また、絶縁膜１３は例えばSiO_2、TiO_2、Al_2O_3、ポリイミドのような絶縁性の材料で形成することができ、例えば１００オングストローム～５μｍ以下の膜厚で、ｎ電極１０、ｐ電極１１を形成すべき窒化物半導体層の表面を除いたほぼ全面に形成する。絶縁膜１３はパッド電極１２がｎ型層２に接触してショートするのを防止すると共に、発光チップ表面に傷が入って素子をダメにするのを防止する作用がある。

【００１４】次に本発明の重要な点である酸化物基板と、第１の薄膜との関係について述べる。本発明の発光素子では基板に酸化物が用いられる。酸化物基板にはサファイア（Al_2O_3）、スピネル（$MgAl_2O_4$）、酸化亜鉛（ＺｎＯ）、マグネシア（ＭｇＯ）等の単結晶を用いることができるが、一般的にはサファイア若しくはスピネルを用いる。

【００１５】次に酸化物基板の第２の主面側に形成する第１の薄膜２１は、電気陰性度が２．０未満の金属で、空気中で安定な金属であればよく、例えばＡｌ＝１．５、Ｔｉ＝１．５、Ｚｒ＝１．４、Ｃｒ＝１．６、Ｎｉ＝１．８、Ｍｏ＝１．８、Ｗ＝１．７、Ｇｅ＝１．８、Ｓｉ＝１．８、Ｓｎ＝１．８、Ｚｎ＝１．６、Ｃｕ＝１．９、Ｍｎ＝１．５、Ｖ＝１．６、Ｎｂ＝１．６のよ

うに、アルカリ金属を除く金属で、融点が２００℃以上の金属を使用することができ、その中でも最も好ましくはＴｉ、Ｃｒ、Ｎｉ、Ｚｒ、Ｍｏよりなる群から選択された少なくとも一種の金属を第１の薄膜２１とする。第１の薄膜２１は、蒸着、スパッタ等の通常のＣＶＤ装置を用いて、通常５０オングストローム～１０μｍの膜厚で形成できる。この第１の薄膜を形成することにより、酸化物基板１と導電性接着剤２３との接着性が良くなり、さらに熱伝導性も向上する。なお電気陰性度はポーリング（L.Pauling）の値による。

【００１６】さらに、第１の薄膜２１と支持体３０とを接続する導電性接着剤２３は金属を含んだ熱伝導性に優れた接着剤を使用でき、例えば銀ペースト、Ｉｎペースト、Ｐｔペースト、Ｐｂ－Ｓｎ半田、その他金属系接着剤があるが、その中でも特にＳｉ、Ｇｅ、Ｓｎよりなる群から選択された少なくとも一種の金属と、Ａｕとを含む導電性接着剤、具体的にはＡｕ－Ｓｉ、Ａｕ－Ｇｅ、Ａｕ－Ｓｎ等を用いる。これら具体的接着剤の各金属の組成比は特に規定しないが、通常はＳｉ、Ｇｅ、ＳｎよりもＡｕを多く含む方が、より強い接着力と高い熱伝導性が得られる。なお、導電性接着剤２３は発光チップをダイボンディングする際に、５０オングストローム～１０μｍ程度の薄膜の状態で、予め第１の薄膜２１の表面に形成することもできるし、また支持体側に形成することもできる。

【００１７】図２は本発明のレーザ素子に係る他の態様を示す模式的な断面図であり、図１と同様に、レーザ素子をレーザ光の共振方向に垂直な方向で切断した際の断面を示しており、図１と同一符号は同一部材を示している。この素子が図１の素子と異なる点は、第１の薄膜の上に、Ａｕよりも高融点を有する金属よりなる第２の薄膜２２を形成していることにある。この第２の薄膜２２の作用は、ダイボンディング時の加熱により、導電性接着剤２３が第１の薄膜２１に混入してきて合金化し、第１の薄膜を変質させるのを防止する作用がある。つまり、第２の薄膜２２は第１の薄膜２１と導電性接着剤２３との間のバリア層として作用し、接着力が低下するのを防止する作用がある。第２の薄膜の材料としては例えばＰｔ、Ｔｉ、Ｎｉ等を好ましく用いることができる。また第２の薄膜の膜厚も特に限定するものではなく、第１の薄膜とほぼ同じ膜厚か、それよりも厚くすることが望ましい。

【００１８】本発明の発光素子において、酸化物基板の第２の主面にＡｌ、Ｔｉ、Ｚｒ、Ｃｒ、Ｎｉ、Ｍｏ、Ｗ、Ｇｅ、Ｓｉ、Ｓｎ、Ｚｎ、Ｃｕ、Ｍｎ、Ｖ、Ｎｂ等の電気陰性度が２．０未満の金属薄膜を形成すると接着力が向上するのかは定かではないが、他の２．０以上の金属薄膜を形成した場合と明らかに差がある。この原因は次のようなことが考えられる。発光チップをダイボンディングする際に導電性接着剤が数百℃に加熱される。加熱時、熱は発光チップに形成された第１の薄膜、第２の薄膜に伝わって、導電性接着剤に含まれる金属と、第１の薄膜、第２の薄膜に含まれる金属とが一部、合金化、若しくは共晶化する。この際に、酸化物基板の材料と、第１の薄膜と、導電性接着剤との金属材料の組み合わせで、何らかの物理的接着力、あるいは化学的接着力が強まるのではないかと推察される。

【００１９】

【実施例】［実施例１］２インチφのサファイア基板Ｃ面（０００１）の上に、ｎ型ＧａＮよりなるｎ型コンタクト層と、ｎ型ＡｌＧａＮよりなるｎ型光閉じこめ層と、ｎ型ＡｌＧａＮよりなる光ガイド層と、ＩｎＧａＮよりなる活性層と、ｐ型ＡｌＧａＮよりなる光ガイド層と、ｐ型ＡｌＧａＮよりなるｐ型光閉じこめ層と、ｐ型ＧａＮよりなるｐ型コンタクト層とが積層されたレーザウェーハを用意する。窒化物半導体の積層構造は単にレーザ発振するための一例を示したものであって、この構造に限定されるものではない。

【００２０】次に、このウェーハの窒化物半導体の最上層に、所定の形状のマスクを形成した後、$SiCl_4$ ガス、Cl_2 ガスを用いてＲＩＥ（反応性イオンエッチング）を行い、図１に示すような形状でｎ電極を形成すべきｎ型コンタクト層を露出させる。ｎ型コンタクト層露出後、マスクを形成し、再度エッチングを行い。ｐ型コンタクト層、ｐ型クラッド層の一部をエッチングし、図１に示すように、ｐ型クラッド層から上をリッジ形状とする。これらのエッチングにより、図１に示すように、リッジ形状のストライプに対して左右対称なｎ型コンタクト層が露出される。

【００２１】ｎ型コンタクト層露出後、最上層のｐ型コンタクト層と、ｎ電極を形成すべきｎ型コンタクト層の表面を除く、窒化物半導体層の表面にSiO_2 よりなる絶縁膜をＣＶＤ法を用いて１μｍの膜厚で形成する。絶縁膜形成後、最上層のｐ型コンタクト層のほぼ全面に２μｍのストライプ状のＮｉ－Ａｕよりなるｐ電極を形成し、ｎ型コンタクト層のほぼ全面にストライプ状のＴｉ－Ａｌよりなるｎ電極を形成する。そして、ｐ電極の上には同じくＮｉ－Ａｕよりなるパッド電極を図１に示すように絶縁膜を介して形成する。

【００２２】電極形成後、サファイア基板を８０μｍの厚さまでラッピングと、ポリシングして研磨した後、そのポリシング面にＣＶＤ法を用いて、Ｔｉよりなる第１の薄膜を０．１μｍの膜厚で形成する。

【００２３】続いてＴｉよりなる第１の薄膜の上に、Ａｕ－Ｓｎ（７０％－３０％）よりなる導電性接着剤層を０．５μｍの膜厚で形成する。

【００２４】導電性接着剤層形成後、基板を強制的に劈開して、窒化物半導体の

【外１】

（１１００）

面に相当する面に共振面を作成し、バー状のレーザチップを作製する。なお外１面とは窒化物半導体を六方晶系で近似した際に表される六角柱の側面（四角形の面、Ｍ面）に相当する面である。

【００２５】次にバー状のレーザチップの共振面側に、プラズマＣＶＤ装置を用いて、SiO_2 とTiO_2 よりなる誘電体多層膜を形成して反射鏡を形成し、バー状のレーザチップを今度はｎ電極に平行な位置でスクライブにより分割して、３５０×５００μｍ角の矩形のレーザチップを得る。

【００２６】以上のようにして得られたレーザチップを、４００℃に加熱したヒートシンクにフェースアップの状態でダイボンダーを用いてダイボンドする。ヒートシンクにダイボンドされたレーザ素子を数千個作製し、その中から１０００個をランダムに抜き取り、さらにｎ電極とｐ電極とをそれぞれ金線でワイヤーボンディングする。ワイヤーボンディング工程中、若しくはワイヤーボンディング後にレーザチップがヒートシンクから剥がれたり、浮いたりしたものを取り除いたところ、歩留は９９％以上あり、非常に強固にレーザ素子がダイボンドされていることが判明した。さらに、このレーザ素子を直流電流で発振させたところ、４１０ｎｍのレーザ発振を示し、１時間以上の寿命であった。

【００２７】［実施例２］実施例１において、Ｔｉよりなる第１の薄膜の上に、Ｐｔよりなる第２の薄膜を０．２μｍの膜厚で形成し、その第２の薄膜の上にＡｕ－Ｓｉよりなる導電性接着剤層を同様に形成する。その他は実施例１と同様にしてレーザチップをダイボンドした後、電極をワイヤーボンドしたところ、歩留は９９．５％以上であり、レーザチップがヒートシンクから剥がれたものは発見されなかった。さらにレーザ素子の寿命も実施例１とほぼ同等の寿命であった。

【００２８】［実施例３］実施例１において、基板にスピネル基板を用い、スピネル基板の第１の主面に窒化物半導体を成長させ、成長後、研磨したスピネル基板の第２の主面側にＣｒよりなる第１の薄膜を０．１μｍの膜厚で形成し、そのＣｒよりなる第１の薄膜の上にＡｕ－Ｇｅ（７０％－３０％）よりなる導電性接着剤層を同じく０．５μｍの膜厚で形成する他は同様にしてレーザチップを得て、ワイヤーボンディングを行ったところ、同じく歩留は９９％以上であり、レーザ素子の寿命も実施例１のものとほぼ同等であった。

【００２９】［実施例４］実施例３において、Ｃｒよりなる第１の薄膜の上に、Ｗよりなる第２の薄膜を０．２μｍの膜厚で形成し、その第２の薄膜の上にＡｕ－Ｓｉよりなる導電性接着剤層を同様に形成する。その他は実施例１と同様にしてレーザチップをダイボンドした後、電極をワイヤーボンドしたところ、歩留は９９．５％以上であり、レーザチップがヒートシンクから剥がれたものは発見されなかった。さらにレーザ素子の寿命も実施例１とほぼ同等の寿命であった。

【００３０】［実施例５］実施例１において、基板にスピネル基板を用い、スピネル基板の第１の主面に窒化物半導体を成長させ、成長後、研磨したスピネル基板の第２の主面側にＮｉよりなる第１の薄膜を０．１μｍの膜厚で形成し、そのＮｉよりなる第１の薄膜の上にＡｕ－Ｓｉ（７０％－３０％）よりなる導電性接着剤層を同じく０．５μｍの膜厚で形成する他は同様にしてレーザチップを得て、ワイヤーボンディングを行ったところ、同じく歩留は９９％以上であり、レーザ素子の寿命も実施例１のものとほぼ同等であった。

【００３１】［実施例６］実施例１において、研磨したサファイア基板の第２の主面側にＺｒよりなる第１の薄膜を０．１μｍの膜厚で形成し、そのＺｒよりなる第１の薄膜の上にＡｕ－Ｓｎ（７０％－３０％）よりなる導電性接着剤層を同じく０．５μｍの膜厚で形成する他は同様にしてレーザチップを得て、ワイヤーボンディングを行ったところ、同じく歩留は９９％以上であり、レーザ素子の寿命も実施例１のものとほぼ同等であった。

【００３２】［実施例７］実施例１において、研磨したサファイア基板の第２の主面側にＭｏよりなる第１の薄膜を０．１μｍの膜厚で形成し、Ｍｏよりなる第１の薄膜の上にＡｕ－Ｓｎ（７０％－３０％）よりなる導電性接着剤層を同じく０．５μｍの膜厚で形成する他は同様にしてレーザチップを得て、ワイヤーボンディングを行ったところ、同じく歩留は９９％以上であり、レーザ素子の寿命も実施例１のものとほぼ同等であった。

【００３３】［実施例８～１６］実施例１において、研磨したサファイア基板の第２の主面側に、それぞれＡｌ（例８）、Ｗ（例９）、Ｓｉ（例１０）、Ｓｎ（例１１）、Ｚｎ（例１２）、Ｃｕ（例１３）、Ｍｎ（例１４）、Ｖ（例１５）、Ｎｂ（例１６）よりなる第１の薄膜を０．１μｍの膜厚で形成し、その第１の薄膜の上にＡｕ－Ｓｎ（７０％－３０％）よりなる導電性接着剤層を同じく０．５μｍの膜厚で形成する他は同様にしてレーザチップを得て、ワイヤーボンディングを行ったところ、それぞれ歩留は実施例１に比較して９３～９５％以上とやや低下したが、レーザ素子の寿命は実施例１のものとほぼ同等であった。

【００３４】［比較例１］実施例１において、研磨したサファイア基板の第２の主面側にＰｄ（電気陰性度＝２．２よりなる第１の薄膜を０．１μｍの膜厚で形成し、その第１の薄膜の上にＡｕ－Ｓｎ（７０％－３０％）よりなる導電性接着剤層を同じく０．５μｍの膜厚で形成する他は同様にしてレーザチップを得て、ワイヤーボンディングを行ったところ、同じく歩留は８５％に低下した。

【００３５】［比較例２］実施例１において、研磨した

サファイア基板の第２の主面側にＰｔ（電気陰性度＝２．２よりなる第１の薄膜を０．１μｍの膜厚で形成し、その第１の薄膜の上に銀ペーストよりなる導電性接着剤層を同じく０．５μｍの膜厚で形成する他は同様にしてレーザチップを得て、ワイヤーボンディングを行ったところ、歩留は６０％に低下した。

【００３６】［比較例３］実施例１において、研磨したサファイア基板の第２の主面側にＡｕ（電気陰性度＝２．４）よりなる第１の薄膜を０．１μｍの膜厚で形成し、その第１の薄膜の上にＡｕ－Ｇｅよりなる導電性接着剤層を同じく０．５μｍの膜厚で形成する他は同様にしてレーザチップを得て、ワイヤーボンディングを行ったところ、歩留は８８％に低下した。

【００３７】

【発明の効果】以上説明したように、本発明の窒化物半導体素子では、窒化物半導体層を形成していない基板側に、特定の金属よりなる薄膜を形成し、この特定の金属を形成した状態で、支持体に加熱しながらＡｕ－Ｓｎ等の導電性接着剤を介してボンディングすることにより、発光チップの接着性が向上する。さらに、第１の薄膜の上に高融点金属よりなる第２の薄膜を形成すると、バリア効果が高まりさらに接着性が向上する。さらにまた、本発明の発光素子ではボンディング材料がすべて金属を含む熱伝導性のよい材料を使用しているために、特にレ＊ーザ素子のような放熱性を要求される発光デバイスに使用すると、素子の寿命を向上させる上でも非常に都合がよい。以上、本発明の発光素子ではレーザ素子について説明したが、本発明はレーザ素子だけではなく、ＬＥＤ素子にも適用することも可能である。

【図面の簡単な説明】

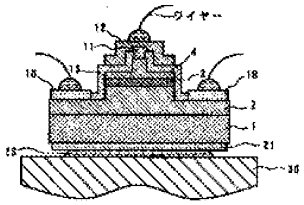
【図１】　本発明の発光素子に係る一構造を示す模式断面図。

【図２】　本発明の発光素子に係る他の構造を示す模式断面図。

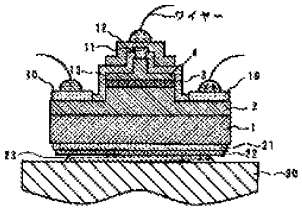
【符号の説明】

１・・・・酸化物基板
２・・・・ｎ型層
３・・・・活性層
４・・・・ｐ型層
１０・・・・ｎ電極
１１・・・・ｐ電極
１２・・・・パッド電極
１３・・・・絶縁膜
２１・・・・第１の薄膜
２２・・・・第２の薄膜
２３・・・・導電性接着剤
３０・・・・支持体

【図１】



【図２】



フロントページの続き

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(54) LED, LED CHIP, LED MODULE, AND LIGHTING SYSTEM

(57)Abstract:
PROBLEM TO BE SOLVED: To provide an LED, or the like which increases an accuracy without involving an increase of a mounting surface area.
SOLUTION: The LED is obtained by laminating diode structure layers 24, 26, 28 with contact layers 30, 32 disposed therebetween. Each of the diode structure layers includes a p-Al0.1Ga0.9N cladding layer (doped with 3 × 1019cm-3 of Mg), an n-Al0.1Ga0.9N cladding layer (doped with 2 × 1018cm-3 of Si), and a 5-period multiple quantum well light emitting layer of an In0.03Ga0.97N (3nm-thick)/Al0.05Ga0.95N (3nm-thick) dispos

Electronic Acknowledgement Receipt

EFS ID:	10954656
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
Receipt Date:	15-SEP-2011
Filing Date:	26-DEC-2007
Time Stamp:	18:08:13
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	P2317US00_IDS_Transmittal.pdf	805874 6aefe8bc53aeb6b87ea42d2c52cafb91839714e2	no	4

Warnings:	
Information:	

A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
2	Foreign Reference	JP_2002-043633.pdf	181245 f2d75f032a9549cb4183783273c59d7982f91919	no	7
Warnings:					
Information:					
3	Foreign Reference	KR_10-2004-0005098.pdf	1043528 e9b8e82f25d129a3dad06c15bc6aaec44a6240e2	no	21
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Information:					
4	Foreign Reference	WO_2005-008791.pdf	3127727 3e8e36d97d336a5ab6c6bd3ecb3774e09f0f6edf	no	76
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5	Foreign Reference	WO_2005-050748.pdf	2930713 793db499817bae1a895bf0180711b7d610d36246	no	53
Warnings:					
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6	Foreign Reference	JP_2002-237646.pdf	3373991 b7a4b1c3a176c3b4df2b329360bf8421a4715b67	no	7
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7	Foreign Reference	JP_2005-019874.pdf	198345 1a2206e1e26c25ecd0a228e903e16fc0c2b70de8	no	1
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			Total Files Size (in bytes):	11661423	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/993,965	12/26/2007	Jong Lam Lee	P2317US00	2191

58027 7590 06/14/2012

H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

EXAMINER	
NGUYEN, THINH T	

ART UNIT	PAPER NUMBER
2897	

NOTIFICATION DATE	DELIVERY MODE
06/14/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATENT@PARK-LAW.COM

Office Action Summary	Application No.	Applicant(s)	
	11/993,965	LEE ET AL.	
	Examiner	Art Unit	
	THINH T. NGUYEN	2897	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1,2,4 and 17-35* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1,2,4 and 17-35* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/09/10,12/29/10,03/30/11,05/11/11,9/15/11*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED OFFICE ACTION

1. This is in response to Applicant filing of a Request for Continuation Examination on August 23rd 2010

2. Claims 1-2, 4, 17-35 are pending in the Application.

3. The Examiner note that some pending claims of this Application has a product by process limitation. Please note that in a product-by-process claim, it is the patentability of the claimed product and not of the recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. The Patent Office is not equipped to manufacture products by a myriad of processes put before it and then obtain prior art product and make physical comparisons therewith. In re Brown, 173 USPQ 685 (CCPA 1972). Also, a product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ I S at 17 (footnote 3). See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al., 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a " product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process"

claims or not.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

4. The Examiner also note that some pending claims has the intended use of a structure for example claim 1 recites -- " **to dissipate heat away from** the P-type semiconductor"-- . Please note that it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus (explicitly disclosed or not) satisfying the claimed structural limitations. *Ex Parte Masham*, 2 USPQ F.2d 1647 (1987).

Claim Rejections - 35 USC § 112

5 The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

Claim 1 is rejected under 35 U.S.C. 112, first paragraph, because it introduces new matter by reciting:

--"a transparent layer is disposed on the P-type semiconductor layer to **dissipate heat away** from the P-type semiconductor layer, "--

there is no support for this limitation in the original specification of the present Application.

7. Claim 17 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

Claim 17 is rejected under 35 U.S.C. 112, first paragraph, because it introduces new matter by reciting

--"a transparent layer is disposed on the second semiconductor layer to **dissipate heat away** from the second semiconductor layer"--

There is no support for this limitation in the original specification of the present Application.,

8. Claims 2, 4, 18-35 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement because they are dependent of a rejected base claim

9. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

10. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

11. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d) which papers have been placed of record in the file.

CONCLUSION

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on 9:30 am - 6:30 pm Monday to Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fernando Toledo can be reached on 571-272-1867. The fax phone numbers for the organization where this application or proceeding is assigned is 571-273-8300

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thinh T Nguyen/

Primary Examiner

Art Unit 2897

Notice of References Cited	Application/Control No. 11/993,965	Applicant(s)/Patent Under Reexamination LEE ET AL.	
	Examiner THINH T. NGUYEN	Art Unit 2897	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2004/0080941	04-2004	Jiang et al.	362/252
*	B	US-6,583,442	06-2003	Ito, Shigetoshi	257/79
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	11993965
Filing Date	2007-12-26
First Named Inventor	Jong Lam Lee
Art Unit	2818
Examiner Name	NGUYEN, THINH T.
Attorney Docket Number	P2317US00

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7598149		2009-10-06	Dawson et al.	
	2	7057208		2006-06-06	Akimoto et al.	

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Receipt date: 12/29/2010	Application Number	11993965 11993965 - GAU: 2897
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317US00

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Non-Final Office Action of U.S Patent Application No. 12/613,275 issued on December 23, 2010.	☐

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EXAMINER SIGNATURE

Examiner Signature	/Thinh Nguyen/	Date Considered	05/07/2012

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /T.N./

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	7	11/993965	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/02/27 23:03
L2	8	"7535028"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/02/27 23:26
L3	33946	AC.as. near3 LED.as. lighting.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/02/27 23:32
L4	12	AC.as. near3 LED.as. near3 lighting.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/02/27 23:32
L5	70	"5862167"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/02/27 23:35
L6	39	"6608330"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/02/27 23:36

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EAST Search History

EAST Search History (Prior Art)

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L7	9	3 and 6	US-PGPUB; USPAT; USOCR	OR	OFF	2012/05/27 23:02
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L9	875477	LED	US-PGPUB; USPAT; USOCR	OR	OFF	2012/05/27 23:21
L10	406	8 and 9	US-PGPUB; USPAT;	OR	OFF	2012/05/27 23:22

			USOCR			
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L12	615	(transparent transpare$4) near9 (n$1) near9 (layer film)near9 nitride	US-PGPUB; USPAT; USOCR	OR	OFF	2012/05/27 23:44

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EAST Search History

EAST Search History (Prior Art)

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L2	9	"7535028"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/27 22:41
L3	41	("20020006040" | "20020043943" | "20030160258" | "20040080941" | "20040129946" | "20040206970" | "20040223342" | "20050127816" | "20050253151" | "20050254243" | "20060044864" | "20060180818" | "20060208264" | "3900863" | "5278432" | "5317170" | "5563422" | "5652434" | "5699073" | "5767581" | "5773130" | "5877558" | "5929466" | "5952680" | "5955748" | "5966393" | "6054724" | "6093965" | "6410940" | "6410942" | "6455878" | "6461019" | "6547249" | "6635902" | "6740960" | "6936855" | "6957899" | "7045965" | "7210819" | "7213942" | "7221044").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/05/27 22:46
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L7	9	3 and 6	US-PGPUB; USPAT; USOCR	OR	OFF	2012/05/27 23:02
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L9	875477	LED	US-PGPUB; USPAT; USOCR	OR	OFF	2012/05/27 23:21
L10	406	8 and 9	US-PGPUB; USPAT;	OR	OFF	2012/05/27 23:22

			USOCR			
L11	29107	(transparent transpare$4) near9 (n$1) near9 (layer film)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/05/27 23:44
L12	615	(transparent transpare$4) near9 (n$1) near9 (layer film)near9 nitride	US-PGPUB; USPAT; USOCR	OR	OFF	2012/05/27 23:44

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
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S5	8	"7535028"	US-PGPUB; USPAT; USOCR	OR	OFF	2012/05/27 23:01
S6	91323	(transparent transpare$4) near9 (electrode)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/05/27 23:02
S7	9	S3 and S6	US-PGPUB; USPAT; USOCR	OR	OFF	2012/05/27 23:02
S8	803	(transparent transpare$4) near9(electrode)near9 (nickel ni) near9 (Gold Au)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/05/27 23:20
S9	875477	LED	US-PGPUB; USPAT; USOCR	OR	OFF	2012/05/27 23:21
S10	406	S8 and S9	US-PGPUB; USPAT;	OR	OFF	2012/05/27 23:22

			USOCR			
S11	29107	(transparent transpare$4) near9 (n$1) near9 (layer film)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/05/27 23:44
S12	615	(transparent transpare$4) near9 (n$1) near9 (layer film)near9 nitride	US-PGPUB; USPAT; USOCR	OR	OFF	2012/05/27 23:44
S13	9	"7535028"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/28 23:45
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S15	29	S14 and transparent	US-PGPUB; USPAT; USOCR	OR	OFF	2012/05/28 23:47

EAST Search History (Interference)

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5/29/2012 8:07:33 AM
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317US00

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Receipt date: 03/30/2011	Application Number	11993965 11993965 - GAU: 2897
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317US00

	1	Notice of allowance of US Patent Application No. 12/613,275 issued on March 25, 2011.	☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317US00

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Receipt date: 05/11/2011	Application Number	11993965 11993965 - GAU: 2897
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317US00

	1	Notice of Allowance of US Patent Application No. 12/630,370 issued on May 6, 2011.	☐

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Examiner Signature	/Thinh Nguyen/	Date Considered	05/07/2012

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11993965	LEE ET AL.
	Examiner	**Art Unit**
	THINH T NGUYEN	2818

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/06/2009	10/30/2009	01/30/2010	06/21/2010	05/29/2012				
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	32				✓	✓				
	33				✓	✓				
	34				✓	✓				
	35				✓	✓				

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317US00

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Receipt date: 12/09/2010	Application Number	11993965 11993965 - GAU: 2818
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2818
	Examiner Name	NGUYEN, THINH T.
	Attorney Docket Number	P2317US00

	1	Non-Final Office Action of U.S Patent Application No. 12/630,370 issued on December 09, 2010.	☐

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EXAMINER SIGNATURE

Examiner Signature	/Thinh Nguyen/	Date Considered	02/28/2012

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11993965	LEE ET AL.
	Examiner	Art Unit
	THINH T NGUYEN	2818

SEARCHED			
Class	Subclass	Date	Examiner
257	100, 266,88,90,e33.064	9/16/09	ttn
362	231	5/27/12	TTN

SEARCH NOTES		
Search Notes	Date	Examiner
east	9/16/09	ttn
east	1/30/10	TTN
east	6/20/10	TTN
east	5/27/12	TTN

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

EAST Search History

EAST Search History (Prior Art)

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S2	9	"7535028"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/27 22:41
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S7	9	S3 and S6	US-PGPUB; USPAT; USOCR	OR	OFF	2012/05/27 23:02
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		semiconductor semi adj conductor)) same ((dissipating dissipate) near9 heat near9 away)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			22:17
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EAST Search History (Interference)

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S24	1	"20040251796"	USPAT; UPAD	OR	ON	2012/05/28 22:20

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam LEE
	Art Unit	2818
	Examiner Name	NGUYEN, Thinh T.
	Attorney Docket Number	P2317US00

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	1	2002-043633	JP		2002-02-08	STANLEY ELECTRIC CO LTD		☐
	2	10-2004-0005098	KR		2004-01-16	VICHEL INC.		☐
	3	2005/008791	WO		2005-01-27	MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.		☐

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Receipt date: 09/15/2011	Application Number	11993965	11993965 - GAU: 2897
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	2007-12-26	
(Not for submission under 37 CFR 1.99)	First Named Inventor	Jong Lam LEE	
	Art Unit	2818	
	Examiner Name	NGUYEN, Thinh T.	
	Attorney Docket Number	P2317US00	

	4	2005-019874	JP		2005-01-20	MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.		☐
	5	2005/050748	WO		2005-06-02	NICHIA CORPORATION		☐
	6	2002-237646	JP		2002-08-23	NICHIA CHEM IND LTD		☐

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Receipt date: 09/15/2011	Application Number	11993965	11993965 - GAU: 2897
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2007-12-26	
	First Named Inventor	Jong Lam LEE	
	Art Unit	2818	
	Examiner Name	NGUYEN, Thinh T.	
	Attorney Docket Number	P2317US00	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

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Signature	/hae-chan park/	Date (YYYY-MM-DD)	2011-09-15
Name/Print	Hae-Chan Park	Registration Number	50114

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2897
	Examiner Name	NGUYEN, THINH T
	Attorney Docket Number	P2317US00

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050110033		2005-05-26	Heremans, et al.	
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2897
	Examiner Name	NGUYEN, THINH T
	Attorney Docket Number	P2317US00

	1	European Patent Office Action dated April 11, 2012 for Application No. 09 014 468.4 - 2222	☐
	2	European Patent Office Action dated April 17, 2012 for Application No. 06 769 008.1 - 2222	☐

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	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2897
	Examiner Name	NGUYEN, THINH T
	Attorney Docket Number	P2317US00

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☐ See attached certification statement.

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Signature	/hae-chan park/	Date (YYYY-MM-DD)	2012-08-10
Name/Print	Hae-Chan Park	Registration Number	50114

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Electronic Patent Application Fee Transmittal

Application Number:	11993965
Filing Date:	26-Dec-2007
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Filer:	Hae-Chan Park/Sharon Price
Attorney Docket Number:	P2317US00

Filed as Large Entity

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

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EFS ID:	13466659
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/JungAh Kim
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
Receipt Date:	10-AUG-2012
Filing Date:	26-DEC-2007
Time Stamp:	17:01:40
Application Type:	U.S. National Stage under 35 USC 371

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4	Fee Worksheet (SB06)	fee-info.pdf	29942 1dcd1228fd209088b5964bacf1a0943f152bbea9	no	2
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	Docket No.: P2317US00
Jong Lam LEE, *et al.*	
Serial No.: 11/993,965	Group Art Unit: 2897
Confirmation No.: 2191	
Filed: December 26, 2007	Examiner: NGUYEN, Thinh T.

For: **LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME**

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY UNDER 37 C.F.R. § 1.111

Sir:

In response to the Non-Final Office Action mailed June 14, 2012 ("Office Action"), Applicants respectfully request reconsideration of the application in view of the following Amendments and Remarks.

Amendments to the Claims begin on page 2.

Remarks begin on page 7.

Applicants believe that no extensions of time are required at this time. If extensions of time are necessary to prevent abandonment of this application, then they are hereby petitioned for under 37 C.F.R. § 1.136(a). Applicants believe that no further fees for net addition of claims are required at this time. Any fees required for further extensions of time and any fees for the net addition of claims are hereby authorized to be charged to our Deposit Account No. 50-3698.

AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 1 and 17 as shown below.

This claim list replaces all prior claim lists in the application.

1. (Currently Amended) A light emitting device, comprising:

a plurality of light emitting cells each comprising an N-type semiconductor layer and a P-type semiconductor layer formed on a portion of the N-type semiconductor layer on a substrate, wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface comprising the N-type or P-type semiconductor layer of the light emitting cell has a slope of approximately 20° to approximately 80° from a horizontal plane based on the substrate, wherein a P-type electrode and a N-type electrode are disposed on the respective P-type semiconductor layer and the N-type semiconductor layer and a transparent layer is disposed on the P-type semiconductor layer ~~to dissipate heat away from the P-type semiconductor layer~~, and wherein an ohmic layer is disposed on the transparent layer or the N-type semiconductor layer, respectively.

2. (Previously Presented) The light emitting device as claimed in claim 1, further comprising:

a wire to couple the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

3. (Canceled)

4. (Previously Presented) The light emitting device as claimed in claim 1, further comprising:

P-type and N-type ohmic metal layers comprising Cr or Au on the P-type and N-type semiconductor layers, respectively.

5-16. (Canceled)

17. (Currently Amended) A light emitting device comprising:

a substrate; and

a plurality of light emitting cells disposed on the substrate being spaced apart from each other,

wherein the light emitting cell comprises a first semiconductor layer and a second semiconductor layer,

at least one of the light emitting cells has at least one side surface that is not perpendicular to a horizontal plane based on the substrate, and

the first semiconductor layer of at least one of the light emitting cells is coupled to the second semiconductor layer of an another adjacent light emitting cell, wherein an electrode of the first semiconductor and an electrode of the second semiconductor are disposed on the respective first semiconductor and the second semiconductor and a transparent layer is disposed on the second semiconductor layer ~~to dissipate heat away from the second semiconductor layer~~, and wherein an ohmic layer is disposed on the transparent layer or the first semiconductor.

18. (Previously Presented) The light emitting device as claimed in claim 17, wherein

the at least one side surface has an inclination angle with respect to the horizontal plane.

19. (Previously Presented) The light emitting device as claimed in claim 18, wherein the inclination angle is approximately 20˚ to approximately 80˚ with respect to the horizontal plane.

20. (Previously Presented) The light emitting device as claimed in claim 18, wherein the inclined surface of the light emitting cell comprises at least a side surface of the first semiconductor layer.

21. (Previously Presented) The light emitting device as claimed in claim 20, wherein the first semiconductor layer is an N semiconductor layer.

22. (Previously Presented) The light emitting device as claimed in claim 20, wherein the inclined surface of the light emitting cell is formed continuously up to the second semiconductor layer.

23. (Previously Presented) The light emitting device as claimed in claim 22, wherein the second semiconductor layer is a P semiconductor layer.

24. (Previously Presented) The light emitting device as claimed in claim 22, wherein the second semiconductor layer of the light emitting cell comprises at least one surface not being inclined.

25. (Previously Presented) The light emitting device as claimed in claim 20, wherein

at least one of the light emitting cells further comprises:

a first bonding pad and a second bonding pad disposed respectively on the first semiconductor layer and the second semiconductor layer.

26. (Previously Presented) The light emitting device as claimed in claim 25, wherein the first bonding pad is disposed on the first semiconductor layer of one of the light emitting cells to couple the second bonding pad disposed on the second semiconductor layer of the another adjacent light emitting cell.

27. (Previously Presented) The light emitting device as claimed in claim 26, wherein connections between the light emitting cells are provided using the bonding pads.

28. (Previously Presented) The light emitting device as claimed in claim 27, wherein providing the bonding pads comprises utilizing at least one of plating method, chemical vapor deposition (CVD), physical vapor deposition (PVD), or electron beam deposition.

29. (Previously Presented) The light emitting device as claimed in claim 26, wherein the connection is provided by an electrical conductor disposed on the inclined surface of the light emitting cell.

30. (Previously Presented) The light emitting device as claimed in claim 29, wherein an insulation layer is disposed to continuously cover a surface of the substrate, a top and the inclined surface of the light emitting cell and the electrical conductor.

31. (Previously Presented) The light emitting device as claimed in claim 17,

wherein a portion of the rear surface of the substrate is removed and Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof is disposed on the rear surface of the substrate on which the light emitting cell is formed to enhance the heat dissipation.

32. (Previously Presented) The light emitting device as claimed claim 1, wherein the substrate comprises a front surface and a rear surface, wherein the light emitting cells are disposed on the front surface and a portion of the rear surface is removed and Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof is disposed on the rear surface to enhance the heat dissipation.

33. (Previously Presented) The light emitting device as claimed claim 1, wherein an insulation layer is disposed continuously to cover a surface of the substrate, a top and the inclined surface of the light emitting cells.

34. (Previously Presented) The light emitting device as claimed in claim 1, wherein the transparent electrode layer is selected from ITO (Indium Tin Oxide), ZnO (Zinc Oxide) or a conductive transparent metal.

35. (Previously Presented) The light emitting device as claimed in claim 17, wherein the transparent electrode layer is selected from ITO (Indium Tin Oxide), ZnO (Zinc Oxide) or a conductive transparent metal.

REMARKS

Claims 1 and 17 have been amended.

Accordingly, claims 1, 2, 4 and 17-35 are currently pending in the application, of which claims 1 and 17 are independent.

In view of the above amendments and the following Remarks, Applicants respectfully request reconsideration and timely withdrawal of the pending objections and rejections for the reasons discussed below.

Product-by-Process Claim Limitation

Applicants submit that a burden has not been discharged because the Examiner does not specify which claims supposed to be product-by process claims (See, Office Action, page 2, "some pending claims"). In addition, the Office Action even does not provide a rationale which claims support the conclusion that the claimed product appears to be the same or similar to that of the prior art. The Examiner does not cite any prior art to establish an unobvious difference between the claimed product and the prior art product. See, MPEP 2113 and *In re Marosi*, 218 USPQ 289, 292 (Fed. Cir. 1983)

Rejections Under 35 U.S.C. § 112, first paragraph

Claim 1 stands rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement. Claim 17 stands rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement. Claims 2, 4, and 18-35 stands rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement because they are dependent of a rejected base claim.

In view of canceling features of "to dissipate heat away from the P-type semiconductor layer" from claims 1 and 17, rejections under 35 U.S.C. § 112, first paragraph over claims 1, 17, and 2, 4, and 18-35 are rendered moot.

Therefore, Applicants respectfully urge the withdrawal of the rejections under 35 U.S.C. § 112, first paragraph, and requests the indication that claims 1 and 17 are allowable, along with their corresponding dependent claims 2, 4, and 18-35.

CONCLUSION

A full and complete response has been made to the pending Office Action, and all of the stated objections and grounds for rejection have been overcome or rendered moot. Accordingly, all pending claims are allowable, and the application is in condition for allowance.

The Examiner is invited to contact Applicants' undersigned representative at the number below if it would expedite prosecution. Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully submitted,

/hae-chan park/

Hae-Chan Park
Reg. No. 50,114

Date: September 7, 2012

CUSTOMER NUMBER: 58027
H.C. Park & Associates, PLC
8500 Leesburg Pike
Suite 7500
Vienna, VA 22182
Tel: 703-288-5105
Fax: 703-288-5139
HCP/SSK/eyj

Electronic Acknowledgement Receipt

EFS ID:	13681805
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/JungAh Kim
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
Receipt Date:	07-SEP-2012
Filing Date:	26-DEC-2007
Time Stamp:	17:02:32
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P2317US00-Reply.pdf	45106 c6f152873f0e2e7716de5b9079edfa8b72d4d121	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	8
Warnings:			
Information:			
	Total Files Size (in bytes):	45106	

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/993,965	12/26/2007	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	09/07/2012	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 22	Minus	** 22	= 0	X $ =		OR	X $60=	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $ =		OR	X $250=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	**0**

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/SUSAN FORD/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/993,965	12/26/2007	Jong Lam Lee	P2317US00	2191

58027 7590 12/21/2012

H.C. PARK & ASSOCIATES, PLC
1894 PRESTON WHITE DRIVE
RESTON, VA 20191

EXAMINER	
NGUYEN, THINH T	
ART UNIT	**PAPER NUMBER**
2897	

NOTIFICATION DATE	DELIVERY MODE
12/21/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATENT@PARK-LAW.COM

Office Action Summary	Application No.	Applicant(s)	
	11/993,965	LEE ET AL.	
	Examiner	Art Unit	
	THINH T. NGUYEN	2897	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2012*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1,2,4 and 17-35* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1,2,4 and 17-35* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/10/12*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED OFFICE ACTION

1. Claims 1-2, 4, 17-35 are pending in the Application.

2. The Examiner note that some pending claims of this Application has a product by process limitation. For Example claim 28 recites:

--" wherein providing the bonding pads comprises utilizing at least one of plating method, chemical vapor deposition (CVD), physical vapor deposition (PVD), or electron beam deposition.

Please note that in a product-by-process claim, it is the patentability of the claimed product and not of the recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. The Patent Office is not equipped to manufacture products by a myriad of processes put before it and then obtain prior art product and make physical comparisons therewith. In re Brown, 173 USPQ 685 (CCPA 1972). Also, a product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ I S at 17 (footnote 3). See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al., 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a " product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear.

3. Applicant's amendments to independent claims 1 and 17 have necessitated new grounds of rejection for claims 1-2, 4, 17-35. See MPEP § 706.07(a).

Claim Rejections - 35 USC § 103

4. The following is a quotation of U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 4, 17-29, 31-32,34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fan et al. (U.S. Patent 7,535,028.) thereafter Fan 028 in view of Yamada (US patent 6,608,330) thereafter Yamada 330

With regard to claim 1, Fan 028 discloses (fig 1, fig 2,fig 3)a light emitting device, comprising: a plurality of light emitting cells each comprising an N-type semiconductor layer and a P- type semiconductor layer (elements 20,16,fig 2, ,column 3 lines 24-50) formed on a portion of the N-type semiconductor layer on a substrate, (fig 2 ,element 12) wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, (fig 2,fig 3) and a side surface comprising the N-type or P-type semiconductor layer of the light emitting cell has a slope of approximately 20 degree to approximately 80 degree from a horizontal plane (column 4 lines 5-20).based on the substrate, wherein a P-type electrode (fig 1,fig 2,fig 3, electrode 22 ,also an ohmic layer electrode column 3 lines 24-48) and a N-type electrode (fig 1, fig 2, fig 3 , electrode 24, also an ohmic layer electrode column 3 lines 24-48) are disposed on the respective P-type semiconductor layer and the N-type semiconductor layer

Not Specific in Fan 028 is the limitation wherein a transparent layer is disposed on the P-type semiconductor layer and wherein an ohmic layer is disposed on the transparent layer or the N-type semiconductor layer, respectively (i.e. a transparent layer between the ohmic P-type or N-type electrodes)

Yamada 330, however, discloses a transparent layer is wherein this transparent layer (fig 1 transparent layer 112,column 10 lines 40-55) is disposed on the P-type semiconductor layer (

fig 1 layer 111 is p-type) and wherein an ohmic layer is disposed (fig 1 , ohmic layer 113, column 10 lines 40-55) on the transparent layer or the N-type semiconductor layer, respectively

It would have been obvious to one of ordinary skill in the art the time the invention was made to incorporate this features, as taught by Yamada 330 into the Fan 028 device and come up with the invention of claim 1.

The rationale is as the following:

A person skilled in the art at the time the invention was made would have been motivated to have this feature in order to improve the light intensity and directional performance of the Fan 028 light emitting device (i.e. transmit light in the vertical direction for example) and make it a commercial success.

Moreover, please note that the transparent limitation is considered obvious because it has been held that

The selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll co V. Interchemical Corp., 325 U.S. 327, 85 USPQ 297 (1945)

With regard to claim 2, Fan 028 discloses (fig 1, fig 2,fig 3) a light emitting device, comprising a wire to couple the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell.

With regard to claim 4, Fan 028 discloses (fig 2, fig 2,fig 3) a light emitting device further comprising P-type and N-type ohmic metal layers Cr or Au on the P-type and N-type semiconductor layers, respectively. (column 3 lines 35-50)

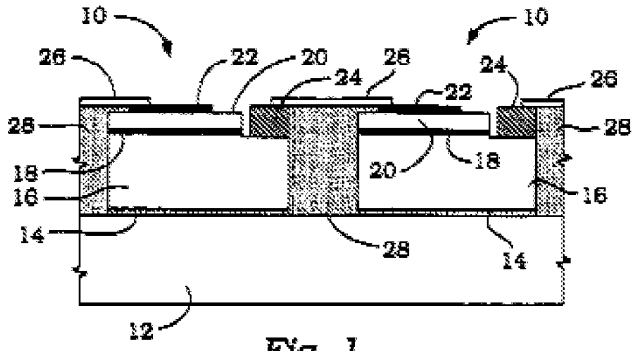


Fig. 1

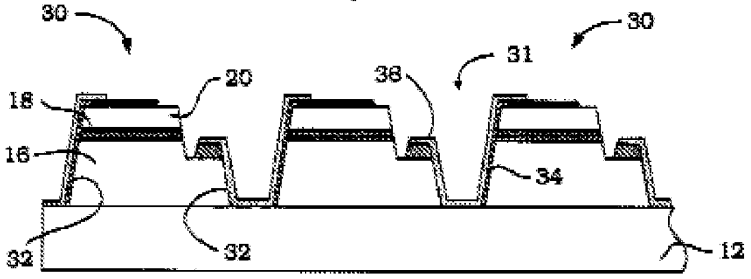


Fig. 2

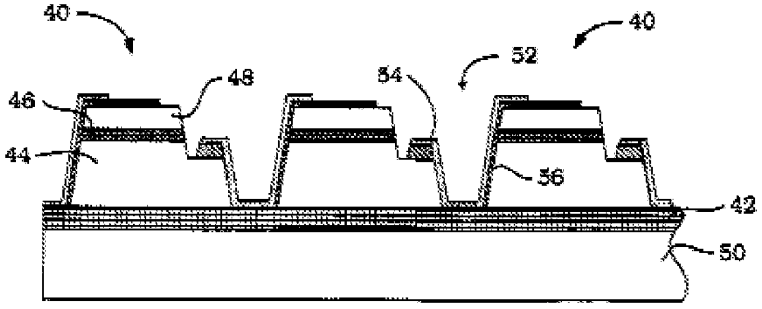
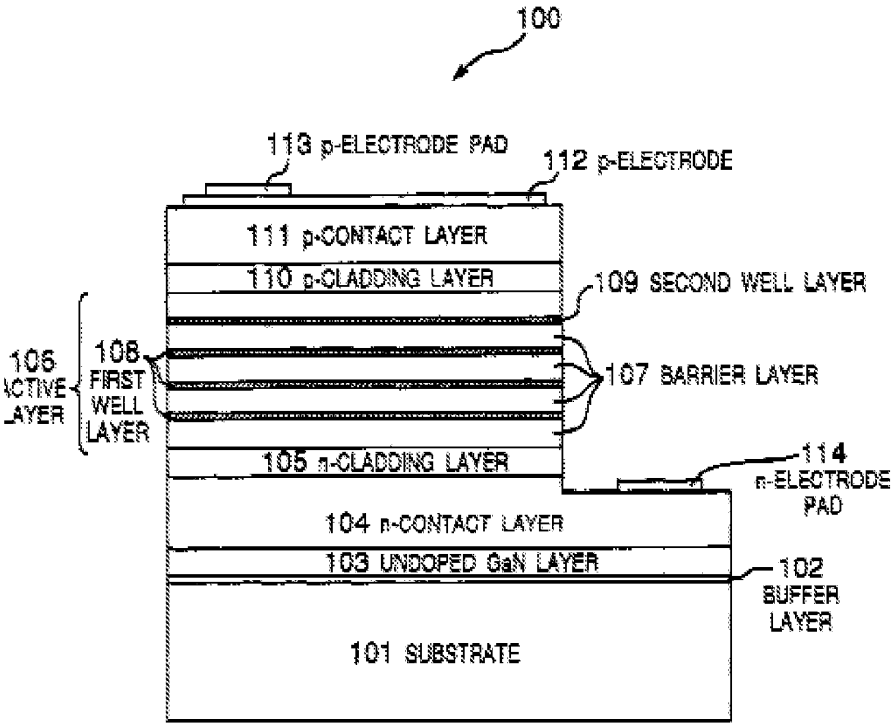


Fig. 3

FAN 028 DISCLOSURES

Fig.1



YAMADA 330 DISCLOSURES

With regard to claim 17-23 , the combined Fan 028 in view of Yamada 330 device will disclose (fig 2,fig 3 of Fan 028) a light emitting device comprising: a substrate; and a plurality of light emitting cells (fig 2,fig 3 of Fan 028) disposed on the substrate being spaced apart from each other, wherein the light emitting cell comprises a first semiconductor layer and a second semiconductor layer, (Fan 028 , column 3 lines 24-50) at least one of the light emitting cells has

at least one side surface that is not perpendicular to a horizontal plane based on the substrate, and the first semiconductor layer of at least one of the light emitting cells is coupled to the second semiconductor layer of an another adjacent light emitting cell, (inherently shown in Fan 028 Fig 2, fig 3) wherein an electrode of the first semiconductor and an electrode of the second semiconductor are disposed on the respective first semiconductor and the second semiconductor (Fan 028, fig 1, fig 2, fig 3 , ohmic electrode 22 on p-type semiconductor , and 24 on n-type semiconductor (fan 028, column 3 lines 24-40) and a transparent layer (Yamada 330 fig 1, transparent layer 112, column 10 lines 40-55 is disposed on the second semiconductor layer (Yamada Fig 1, second semiconductor layer 111, column 10 lines 40-55) and wherein an ohmic layer is disposed on the transparent layer or the first semiconductor.(Yamada 330 ohmic layer 113, fig 1, column 10 lines 40-55)

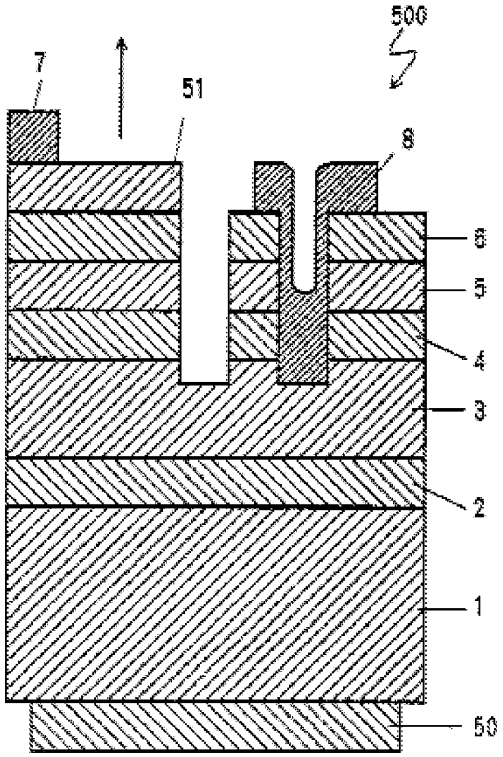
or wherein at least one side surface has an inclination angle with respect to the horizontal plane or wherein the inclination angle is approximately 20° to approximately 80° with respect to the horizontal plane (Fan 028 column 4 lines 5-20) ;or .wherein the inclined surface of the light emitting cell comprises at least a side surface of the first- semiconductor layer ; or wherein the first-type semiconductor layer is an N-type semiconductor layer ; or wherein the inclined surface of the light emitting cell is formed continuously up to the second-type semiconductor layer ; or wherein the second-type semiconductor layer is a P- semiconductor layer

With regard to claim 24, Fan 028 discloses an embodiment (fig 1), wherein the second semiconductor layer of the light emitting cell comprises at least one surface not being inclined

With regard to claim 25, Yamada discloses a bonding pad on each of the p-side and n-side electrode

With regard to claim 31, 32 as set forth in the rejection of claim 20 and 1,, the combined Fan 028 in view of Yamada device discloses all the invention except for AI, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof disposed on a rear surface of the substrate on which the light emitting cell is formed to enhance heat dissipation. this limitation , however, is considered obvious because the use of a metal layer to reflect light to increase the light output efficiency of an LED device is known in the art at the time the invention was made (see US 5,862,167 fig 5 layer 50).

FIG. 5



With regard to claims 34, 35 these claims are obvious over the disclosures of Fan 028 in view of Yamada 330 for the following rationale

The selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll co V. Interchemical Corp., 325 U.S. 327, 85 USPQ 297 (1945)

With regard to claim 26,27 the combined Fan 028 in view of Yamada 330 disclosure will disclose (fig 2,fig 3 of Fan 028) a light emitting device wherein the first bonding pad is disposed on the first semiconductor layer of one of the light emitting cells to couple the second bonding pad disposed on the second semiconductor layer of the another adjacent light emitting cell or connection between the light emitting cells are provided using the bonding pads (Fan 028 fig 2,fig 3, Yamada Fig 1)

With regard to claim 28, Yamada 330 discloses the use of bond pads (note that for claim 28 the product by process limitations are not considered because of the rationale set forth in paragraph 2 of this office Action.

With regard to claim 29, Fan 028 discloses a light emitting device (fig 2,fig 3, element # 36) wherein the-connection is provided by an electrical conductor disposed on the inclined surface of the light emitting cell.

5. Claims 30,33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fan et al. (U.S. Patent 7,535,028.) thereafter Fan 028 in view of Yamada (US patent 6,608,330) thereafter Yamada 330 in further view of Jiang et al. (US patent 7,213,942) thereafter Jiang 942

With regard to claim 30,33 , as set forth in the rejection of claim 29 and claim 1, the combined Fan 028 in view of Yamada 330 device discloses all the invention except for the limitation wherein an insulation layer is disposed to continuously cover a surface of the substrate, between a top and the inclined surface of the light emitting cell and the electrical conductor or wherein an insulation layer is disposed continuously to cover a surface of the substrate, a top and the inclined surface of the light emitting cells.

Jiang 028, however, discloses a light emitting device array wherein an insulation layer is disposed to continuously cover a surface of the substrate, between a top and the inclined surface of the light emitting cell and the electrical conductor or wherein an insulation layer is disposed continuously to cover a surface of the substrate, a top and the inclined surface of the light emitting cells.(Jiang 942 fig 4 element # 54, column 5 lines 4-22)

It would have been obvious to one of ordinary skill in the art the time the invention was made to incorporate this features, as taught by Jiang 942 into the combined Fan 028 in view of Yamada 330 device and come up with the invention of claim 30,33

The rationale is as the following:

A person skilled in the art at the time the invention was made would have been motivated to have this feature in order to provide the Fan 028 in view Yamada 330 device with extra protection in order to increase its reliability

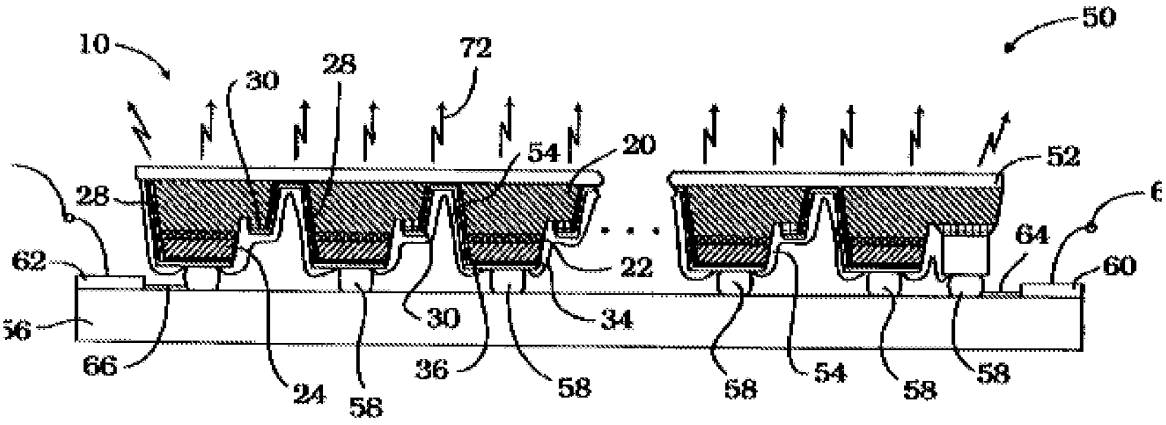


Fig. 4

JIANG 942 DISCLOSURES

6. Applicant arguments in the communications with the Office on September 7th 2012 have been fully considered and the rejections under 35 USC first paragraph have been withdrawn. However, Claims 1,2,4, 17-35 are still rejected as being unpatentable over prior art as discussed in this Office Action.

CONCLUSION

7. THIS ACTION IS MADE FINAL. Applicant's amendments to independent claims 1 and 17 have necessitated new grounds of rejection for claims 1-2, 4, 17-35 and therefore

this Action is made Final (See MPEP § 706.07(a) . Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on 9:30 am - 6:30 pm Monday to Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fernando Toledo can be reached on 571-272-1867. The fax phone numbers for the organization where this application or proceeding is assigned is 571-273-8300

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thinh T Nguyen/

Primary Examiner

Art Unit 2897

Notice of References Cited	Application/Control No. 11/993,965	Applicant(s)/Patent Under Reexamination LEE ET AL.	
	Examiner THINH T. NGUYEN	Art Unit 2897	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,535,028	05-2009	Fan et al.	257/88
*	B	US-6,608,330	08-2003	Yamada, Motokazu	257/90
*	C	US-7,213,942	05-2007	Jiang et al.	362/231
*	D	US-5,862,167	01-1999	Sassa et al.	372/45.01
	E	US-			
	F	US-			
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	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
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	O					
	P					
	Q					
	R					
	S					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	11993965
	Filing Date	2007-12-26
	First Named Inventor	Jong Lam Lee
	Art Unit	2897
	Examiner Name	NGUYEN, THINH T
	Attorney Docket Number	P2317US00

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050110033		2005-05-26	Heremans, et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /T.N./

Receipt date: 08/10/2012	Application Number	11993965	11993965 - GAU: 2897
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2007-12-26	
	First Named Inventor	Jong Lam Lee	
	Art Unit	2897	
	Examiner Name	NGUYEN, THINH T	
	Attorney Docket Number	P2317US00	

	1	European Patent Office Action dated April 11, 2012 for Application No. 09 014 468.4 - 2222	☐
	2	European Patent Office Action dated April 17, 2012 for Application No. 06 769 008.1 - 2222	☐

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EXAMINER SIGNATURE

Examiner Signature	/Thinh Nguyen/	Date Considered	12/14/2012

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /T.N./

Receipt date: 08/10/2012	Application Number	11993965	11993965 - GAU: 2897
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2007-12-26	
	First Named Inventor	Jong Lam Lee	
	Art Unit	2897	
	Examiner Name	NGUYEN, THINH T	
	Attorney Docket Number	P2317US00	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2012-08-10
Name/Print	Hae-Chan Park	Registration Number	50114

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /T.N./

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /T.N./

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11993965	LEE ET AL.
	Examiner	**Art Unit**
	THINH T NGUYEN	2818

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/06/2009	10/30/2009	01/30/2010	06/21/2010	05/29/2012				
	1	÷	÷	✓	✓	✓				
	2	÷	÷	✓	✓	✓				
	3	÷	÷	✓	-	-				
	4	÷	÷	✓	✓	✓				
	5	÷	÷	-	-	-				
	6	÷	÷	-	-	-				
	7	÷	N	-	-	-				
	8	÷	N	-	-	-				
	9	÷	N	-	-	-				
	10	÷	N	-	-	-				
	11	÷	N	-	-	-				
	12	÷	N	-	-	-				
	13	÷	N	-	-	-				
	14	÷	N	-	-	-				
	15	÷	N	-	-	-				
	16	÷	N	-	-	-				
	17			✓	✓	✓				
	18			✓	✓	✓				
	19			✓	✓	✓				
	20			✓	✓	✓				
	21			✓	✓	✓				
	22			✓	✓	✓				
	23			✓	✓	✓				
	24			✓	✓	✓				
	25			✓	✓	✓				
	26			✓	✓	✓				
	27			✓	✓	✓				
	28			✓	✓	✓				
	29			✓	✓	✓				
	30			✓	✓	✓				
	31			✓	✓	✓				
	32				✓	✓				
	33				✓	✓				
	34				✓	✓				
	35				✓	✓				

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	9	lumiled.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/12/17 06:52
L2	6295	Nichia.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/12/17 06:54
L3	0	Nagal.inv. near3 Hideo.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/12/17 06:55
L4	604	Nagai.inv. near3 Hideo.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/12/17 06:55
L5	1386	lumileds.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/17 06:57
L6	965840	mat-sushita.as. matsushita.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/12/17 06:58
L7	217	4 and 6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/12/17 06:58
L8	26921	semiconductor near3 light near3 emitting near3 device	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/12/17 06:59
L9	35371	semiconductor near3 light near3 emitting near3 (diode device)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/12/17 06:59
L10	32	7 and 8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/12/17 07:00
L11	33	7 and 9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/12/17 07:00
L12	9	"7535028"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/12/17 07:35
L13	45	"6608330"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/12/17 07:41
L14	2	"20080251796"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2012/12/17 07:47

EAST Search History (Interference)

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12/17/2012 9:18:22 AM

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11993965	LEE ET AL.
	Examiner	Art Unit
	THINH T NGUYEN	2818

SEARCHED			
Class	Subclass	Date	Examiner
257	100, 266,88,90,e33.064,98,99,103	9/16/09	ttn
362	231	5/27/12	TTN

SEARCH NOTES		
Search Notes	Date	Examiner
east	9/16/09	ttn
east	1/30/10	TTN
east	6/20/10	TTN
east	5/27/12	TTN
EAST	12/17/12	TTN

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE
GROUP ART UNIT 2897

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	Docket No.: P2317US00
Jong Lam LEE, *et. al.*	
Serial No.: 11/993,965	Group Art Unit: 2897
Confirmation No.: 2191	
Filed: December 26, 2007	Examiner: NGUYEN, Thinh T.

For: **LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME**

Mail Stop: AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY AND AMENDMENT UNDER 37 C.F.R. § 1.116

Sir:

In response to the Final Office Action mailed December 21, 2012 ("Office Action"), Applicants respectfully request reconsideration of the application in view of the following Amendments and Remarks.

Amendments to the Claims begin on page 2.

Remarks begin on page 7.

Applicants believe that no extensions of time are required at this time. If extensions of time are necessary to prevent abandonment of this application, then they are hereby petitioned for under 37 C.F.R. § 1.136(a). Applicants believe that no further fees for net addition of claims are required at this time. Any fees required for further extensions of time and any fees for the net addition of claims are hereby authorized to be charged to our Deposit Account No. 50-3698.

AMENDMENTS TO THE CLAIMS

.Please **AMEND** claims 1 and 17 as shown below.

.Please **CANCEL** claims 30-32 as shown below.

This claim list replaces all prior claim lists in the application.

1. (Currently Amended) A light emitting device, comprising:

a plurality of light emitting cells each comprising an N-type semiconductor layer and a P-type semiconductor layer formed on a portion of the N-type semiconductor layer on a substrate, wherein the N-type semiconductor layer of one light emitting cell and the P-type semiconductor layer of another adjacent light emitting cell are connected to each other, and a side surface comprising the N-type or P-type semiconductor layer of the light emitting cell has a slope of approximately 20° to approximately 80° from a horizontal plane based on the substrate, wherein a P-type electrode and a N-type electrode are disposed on the respective P-type semiconductor layer and the N-type semiconductor layer and a transparent layer is disposed on the P-type semiconductor layer, and ~~wherein~~ an ohmic layer is disposed on the transparent layer or the N-type semiconductor layer, respectively, and a portion of the rear surface of the substrate is removed and Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof is deposited on the removed portion of the rear surface to enhance a heat dissipation, and wherein an insulation layer is disposed to continuously cover a surface of the substrate, a top and the inclined surface of the light emitting cell.

2. (Previously Presented) The light emitting device as claimed in claim 1, further comprising:

a wire to couple the N-type semiconductor layer of one light emitting cell and the P-type

semiconductor layer of another adjacent light emitting cell.

3. (Canceled)

4. (Previously Presented) The light emitting device as claimed in claim 1, further comprising:

P-type and N-type ohmic metal layers comprising Cr or Au on the P-type and N-type semiconductor layers, respectively.

5-16. (Canceled)

17. (Currently Amended) A light emitting device comprising:

a substrate; and

a plurality of light emitting cells disposed on the substrate being spaced apart from each other,

wherein the light emitting cell comprises a first semiconductor layer and a second semiconductor layer,

at least one of the light emitting cells has at least one side surface that is not perpendicular to a horizontal plane based on the substrate, and

the first semiconductor layer of at least one of the light emitting cells is coupled to the second semiconductor layer of an another adjacent light emitting cell, wherein an electrode of the first semiconductor and an electrode of the second semiconductor are disposed on the respective first semiconductor and the second semiconductor and a transparent layer is disposed on the second semiconductor layer, and ~~wherein~~ an ohmic layer is disposed on the transparent layer or the first semiconductor, and a portion of the rear surface of the substrate is

removed and Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof is deposited on the removed portion of the rear surface to enhance a heat dissipation, and wherein an insulation layer is disposed to continuously cover a surface of the substrate, a top and the inclined surface of the light emitting cell.

18. (Previously Presented) The light emitting device as claimed in claim 17, wherein the at least one side surface has an inclination angle with respect to the horizontal plane.

19. (Previously Presented) The light emitting device as claimed in claim 18, wherein the inclination angle is approximately 20˚ to approximately 80˚ with respect to the horizontal plane.

20. (Previously Presented) The light emitting device as claimed in claim 18, wherein the inclined surface of the light emitting cell comprises at least a side surface of the first semiconductor layer.

21. (Previously Presented) The light emitting device as claimed in claim 20, wherein the first semiconductor layer is an N semiconductor layer.

22. (Previously Presented) The light emitting device as claimed in claim 20, wherein the inclined surface of the light emitting cell is formed continuously up to the second semiconductor layer.

23. (Previously Presented) The light emitting device as claimed in claim 22, wherein the second semiconductor layer is a P semiconductor layer.

24. (Previously Presented) The light emitting device as claimed in claim 22, wherein the second semiconductor layer of the light emitting cell comprises at least one surface not being inclined.

25. (Previously Presented) The light emitting device as claimed in claim 20, wherein at least one of the light emitting cells further comprises:

a first bonding pad and a second bonding pad disposed respectively on the first semiconductor layer and the second semiconductor layer.

26. (Previously Presented) The light emitting device as claimed in claim 25, wherein the first bonding pad is disposed on the first semiconductor layer of one of the light emitting cells to couple the second bonding pad disposed on the second semiconductor layer of the another adjacent light emitting cell.

27. (Previously Presented) The light emitting device as claimed in claim 26, wherein connections between the light emitting cells are provided using the bonding pads.

28. (Previously Presented) The light emitting device as claimed in claim 27, wherein providing the bonding pads comprises utilizing at least one of plating method, chemical vapor deposition (CVD), physical vapor deposition (PVD), or electron beam deposition.

29. (Previously Presented) The light emitting device as claimed in claim 26, wherein the connection is provided by an electrical conductor disposed on the inclined surface of the light emitting cell.

30-32. (Canceled)

33. (Previously Presented) The light emitting device as claimed claim 1, wherein an insulation layer is disposed continuously to cover a surface of the substrate, a top and the inclined surface of the light emitting cells.

34. (Previously Presented) The light emitting device as claimed in claim 1, wherein the transparent electrode layer is selected from ITO (Indium Tin Oxide), ZnO (Zinc Oxide) or a conductive transparent metal.

35. (Previously Presented) The light emitting device as claimed in claim 17, wherein the transparent electrode layer is selected from ITO (Indium Tin Oxide), ZnO (Zinc Oxide) or a conductive transparent metal.

REMARKS

Claims 1 and 17 have been amended. Claims 30-32 have been canceled without prejudice or disclaimer.

Accordingly, claims 1, 2, 4, 17-29, and 33-35 are currently pending in the application, of which claims 1 and 17 are independent.

Applicants respectfully submit that the above amendments do not add new matter to the application. The amendments have been made merely to incorporate dependent claims 30-32 into claims 1 and 17, respectively.

Entry of the Amendment is proper under 37 C.F.R. §1.116 because it places the application in *prima facie* condition for allowance for at least the reasons discussed herein; it does not raise new issues requiring further search and/or consideration by the Examiner because similar subject matter was previously considered by the Examiner, and thus, further consideration and/or search by the Examiner is not warranted; it places the application in better form for appeal, should an appeal be necessary.

For at least these reasons, entry of the present Amendment is, therefore, respectfully requested. Accordingly, Applicants request reconsideration and timely withdrawal of the pending rejections for at least the reasons discussed below.

Request for Withdrawal of Premature Final Rejection

Withdrawal of the prematurely imposed final rejection is respectfully requested. The Manual of Patent Examining Procedure (MPEP) § 706.07(a) sets forth the United States Patent and Trademark Office's policy for final rejections as follows:

> Under present practice, second or any subsequent actions on the merits shall be final, **except** where the examiner introduces a **new ground of rejection** that is neither **necessitated by applicant's amendment** of the claims nor based on information submitted in

> an information disclosure statement filed during the period set forth in 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p).
> ….
> A second or any subsequent action on the merits in any application or patent involved in reexamination proceedings **should not be made final** if it includes **a rejection**, **on prior art not of record**, **of any claim amended to include limitations which should reasonably have been expected to be claimed**. See MPEP § 904 *et seq.* For example, one would reasonably expect that a rejection under 35 U.S.C. § 112 for the reason of incompleteness would be replied to by an amendment supplying the omitted element.

In the present application, claims 12-24 were originally rejected in the non-final Office Action of June 14, 2012, under 35 U.S.C. § 112, ¶ 1 as failing to comply with the written description requirement. In response, features of "to dissipate heat away from the P-type semiconductor layer" were canceled. The present Office Action now imposes a new ground of rejection based on Fan, Yamada, Jiang and Sassa, allegedly because the Applicant's amendment necessitated the new ground of rejection. However, the mere canceling a portion of the claimed features do not necessitate the § 103 rejection, and in any event, amendments to supply a missing element or statutory basis should reasonably have been expected.

Because the amendment did not necessitate the new ground of rejection, the imposition of the finality of the Office Action is premature, and its withdrawal is respectfully requested.

Rejections Under 35 U.S.C. § 103

Claims 1, 2, 4, 17-29, 31, 32, 34, and 35 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over U.S. Patent No. 7,535,028, issued to Fan, *et al.* ("Fan") in view of U.S. Patent No. 6,608,330, issued to Yamada ("Yamada"). Claims 30 and 33 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Fan in view of Yamada, and further in view of U.S. Patent No. 7,213,942, issued to Jiang, *et al.* ("Jiang").

Applicants have amended independent claims 1 and 17 to reduce issues for possible appeal and place the application in better form for the appeal. The amendments merely incorporate features previously recited in dependent claims 30-32 into respective claims 1 and 17. Entry of the Amendment is proper under 37 C.F.R. § 1.116 because the amendments not raise new issues requiring further search and/or consideration by the Examiner because similar subject matter was previously considered by the Examiner, and thus, further consideration and/or search by the Examiner may not warranted.

The Examiner bears the initial burden of establishing a prima facie basis to deny patentability to a claimed invention under any statutory provision. In rejecting a claim under 35 U.S.C. § 103(a), the Examiner is required to provide a factual basis to support the obviousness conclusion. *In re Warner*, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967); *In re Lunsford*, 357 F.2d 385, 148 USPQ 721 (CCPA 1966); *In re Freed*, 425 F.2d 785, 165 USPQ 570 (CCPA 1970).

Further in rejecting a claim under 35 U.S.C. § 103(a) it is incumbent upon the Examiner to establish the requisite motivation. As maintained by the Supreme Court of the United States in *KSR Intern. Co. v. Teleflex Inc.*, 127 S.Ct. 1727 at 1741, an obviousness "analysis should be made explicit." *See In re Kahn*, 441 F.3d 977, 988 (C.A. Fed, 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusions of obviousness"). Indeed, the Examiner is required to make specific factual findings, not generalizations, *See* M.P.E.P. § 2144.08 II.A.5. The initial burden required by procedural due process of law has not been discharged.

Applicants respectfully traverse the imposed rejections under 35 U.S.C. § 103 based on Sassa and Yamada (Office Action, page 9) over independent claims 1 and 17, noting that the references neither disclose nor suggest not only the claimed two-tier structure (*viz.*, transparent

layer + **a portion** of the rear surface of the substrate is **removed and** Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof is **deposited on the removed portion** of the rear surface **to enhance a heat dissipation**), but also the claimed functional advantages attributed to the claimed novel layered structure, i.e., to enhance luminous efficiency and resolve **a chronic heat problem**. (*See* paragraphs [0004] [0009], [0051], [0065], and [0073]).

The fact remains, Sassa (US 5,862,167, Office Action, page 9) never addresses nor teaches about "heat" other than "little attenuation," which means not gradual loss in intensity of light emitted from LED 500, and therefore, cannot be encompassed by features recited in the dependent claims 31 and 32 because "little attenuation" inevitably gains intensity of flux of light that is directly opposite to the teachings of the problem addressed by the claimed invention. Further, the deficiencies of Fan, Yamada and Sassa cannot be remedied by Examiner's mere conjecture, design choice, routine skill, or optimization, especially when the record does not support such conclusions. *See generally In re Zurko*, 258 F.3d 1379 (Fed. Cir. 2001).

Further, the Office Action states the following:

> The metal reflecting layer 50 is useful. Since the sapphire substrate 1 is transparent to the light emitted from the LED 500, the light reflected by the **metal reflecting layer 50** beneath the **sapphire substrate 1** is transmitted to the emission plane with **little attenuation** when the light passes through the sapphire substrate 1. Further, the fabrication of the layer 50 is straight forward, because it is formed at the backside of the sapphire substrate 1. (Sassa, FIG. 5, item50 and accompanying passages, Office Action, page 9)

The Office Action has engaged in impermissible hindsight reconstruction of Applicants' claimed invention; this time, the Office Action has additionally delved into employing non-analogous art to contrive a structure to satisfy the features of the claims. It means Sassa is not "reasonably pertinent" reference. "A reference is reasonably pertinent if it, as a result of its subject matter, 'logically would have commended itself to an inventor's attention in considering his problem.'" Slip Op. at 15, quoting *Innovention Toys, LLC v. MGA Entm't, Inc.*, 637 F.3d

1314, 1321 (Fed. Cir. 2011). In this case, a person having ordinary skill in the art would not have consulted Sassa's metal layer, because merely adding a metal layer on rear surface of the substrate does not relieve heating problems.

The claimed features provide novel two tier layers to dissipate heat by using "transparent layer" and "**a portion** of the rear surface of the substrate is **removed and** Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof is **deposited on the removed portion** of the rear surface **to enhance a heat dissipation**." The Examiner is not allowed to ignore qualified terms such as "**a portion** of the rear surface of the substrate is **removed**" and "Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof is **deposited on the removed portion** of the rear surface" much less "**to enhance a heat dissipation**."

Applicants respectfully request that the Examiner either provide such evidence supposedly teaching the above-noted features or withdraw the rejection.

Although the invention may have been technologically simple and readily apparent once the problem is defined, the invention may not be common sense if the problem itself is not obvious. Often the inventive contribution lies in defining the problem in a new revelatory way.

It is well settled that the **problem** addressed and solved by a claimed invention **must be given consideration** in resolving the ultimate legal conclusion of obviousness under 35 U.S.C. § 103. *North American Vaccine, Inc. v. American Cyanamid Co.*, 7 F.3d 1571, 28 USPQ 1333 (Feb. Cir. 1993); *In re Dillon, 919 F.2d 688, 16 USPQ2d 1897* (Fed. Cir. 1990); *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 15 USPQ 1321 (Fed. Cir. 1990); *Jones v. Hardy*, 727 F.2d 1524, 220 USPQ 1021 (Fed. Cir. 1984).

Although claimed features evince the unobvious structural differences between Applicants' claimed invention and the cited references, the Examiner is reconstructing the claims based on hindsight. It is well settled that it is impermissible simply to engage in hindsight reconstruction of the claimed invention, using Appellant's structure as a template and selecting

elements from the references to fill in the gaps. *In re Gorman*, 933 F.2d982, 18 USPQ2d 1885 (Fed. Cir. 1991).

Furthermore, simplicity and hindsight are not proper criteria for resolving obviousness. *In re Warner*, 397 F.2d 1011, 154 USPQ 173 (CCPA 1967).

With respect to the second prong of claim 1, i.e., "an insulation layer is disposed to continuously cover a surface of the substrate, a top and the inclined surface of the light emitting cell," the Examiner, however, on page 9, has engaged in impermissible hindsight by reconstructing the claimed invention using Appellant's "insulation layer" as a template and selecting element from Jiang to fill the gap.

In other words, given the following factual evidences from Jiang (FIG. 4 and col. 5: 32-35) and bonding bump 58, it cannot be reasonably read on claimed "an insulation layer is disposed to **continuously cover a surface of the substrate, a top and the inclined surface** of the light emitting cell."

> The passivation layer 54 is **removed from the conductive layer 36** and the chip 10 is flipped to be bonded to submount 56, and light is extracted from the top transparent substrate side

It is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983) The requisite motivation to establish a prima facie case of obviousness cannot be established by undercutting the expressed objectives of an applied reference. See *In re Fritch*, 972 F.2d 1260, 23 USPQ2d 1780 (Fed. Cir. 1992); *In re Gordon*, 733F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984); *In re Schulpen*, 390 F.2d 1009, 157 USPQ 52 (CCPA 1968).

A *prima facie* of obviousness, thus, has not been established. To establish *prima facie* obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). All words in a claim

must be considered in judging the patentability of that claim against the prior art. *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Therefore, Applicants respectfully request to withdraw outstanding obviousness rejections, and urge to indicate claims 1 and 17 be allowable and dependent claims thereof.

CONCLUSION

A full and complete response has been made to the pending Office Action, and all of the stated grounds for rejection have been overcome or rendered moot. Accordingly, all pending claims are allowable, and the application is in condition for allowance.

The Examiner is invited to contact Applicants' undersigned representative at the number below if it would expedite prosecution. Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully submitted,

/sangwon kim/

Sangwon Kim
Reg. No. 54,221

Date: January 23, 2013

CUSTOMER NUMBER: 58027
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1894 Preston White Drive
Reston, VA 20191
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Electronic Acknowledgement Receipt

EFS ID:	14767518
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/JungAh Kim
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
Receipt Date:	23-JAN-2013
Filing Date:	26-DEC-2007
Time Stamp:	15:47:57
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Reply.pdf	73963 04203658282eb7840e28f09f93225e8eb5bf2b00	yes	13

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment After Final	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	13
Warnings:			
Information:			
	Total Files Size (in bytes):	73963	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/993,965	12/26/2007	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	01/23/2013	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 19	Minus	** 22	= 0	X $ =		OR	X $62=	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $ =		OR	X $250=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	**0**

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/DORIS ISAAC/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/993,965	12/26/2007	Jong Lam Lee	P2317US00	2191

58027 7590 01/31/2013

H.C. PARK & ASSOCIATES, PLC
1894 PRESTON WHITE DRIVE
RESTON, VA 20191

EXAMINER	
NGUYEN, THINH T	
ART UNIT	**PAPER NUMBER**
2897	

NOTIFICATION DATE	DELIVERY MODE
01/31/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATENT@PARK-LAW.COM

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 11/993,965	**Applicant(s)** LEE ET AL.
	Examiner THINH T. NGUYEN	**Art Unit** 2897

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 23 January 2013 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

NO NOTICE OF APPEAL FILED

1. ☒ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
   c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection. The current period for reply expires months from the mailing date of *the prior Advisory Action* or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.
   Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANT'S FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   b) ☐ They raise the issue of new matter (see NOTE below);
   c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): (a) ☐ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: See Continuation Sheet.

STATUS OF CLAIMS

14. The status of the claim(s) is (or will be) as follows:
    Claim(s) allowed: .
    Claim(s) objected to: .
    Claim(s) rejected: 1,2,4 and 17-35.
    Claim(s) withdrawn from consideration: .

/Thinh T Nguyen/ Primary Examiner Art Unit 2897	

Continuation of 13. Other: The amendments to independent claim 1 and 17 raise new issues for claims 1,2,4 and 17-35 more searches are required

Examiner
Thinh T Nguyen
/TTN/

.

DO NOT ENTER: /T.N./

/Thinh Nguyen/ 01/25/2013

RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE
GROUP ART UNIT 2897

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	Docket No.: P2317US00
Jong Lam LEE, *et. al.*	
Serial No.: 11/993,965	Group Art Unit: 2897
Confirmation No.: 2191	
Filed: December 26, 2007	Examiner: NGUYEN, Thinh T.

For: **LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME**

Mail Stop: AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY AND AMENDMENT UNDER 37 C.F.R. § 1.116

Sir:

In response to the Final Office Action mailed December 21, 2012 ("Office Action"), Applicants respectfully request reconsideration of the application in view of the following Amendments and Remarks.

Amendments to the Claims begin on page 2.

Remarks begin on page 7.

Applicants believe that no extensions of time are required at this time. If extensions of time are necessary to prevent abandonment of this application, then they are hereby petitioned for under 37 C.F.R. § 1.136(a). Applicants believe that no further fees for net addition of claims are required at this time. Any fees required for further extensions of time and any fees for the net addition of claims are hereby authorized to be charged to our Deposit Account No. 50-3698.

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	11/993,965	Filing Date	2007-12-26	Docket Number (if applicable)	P2317US00	Art Unit	2897
First Named Inventor	Jong Lam Lee			Examiner Name	NGUYEN, THINH T		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☒ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☐ Enclosed

☐ Amendment/Reply

☐ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 503698

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/sangwon kim/	Date (YYYY-MM-DD)	2013-02-26
Name	Sangwon Kim	Registration Number	54221

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	11993965
Filing Date:	26-Dec-2007
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Filer:	Hae-Chan Park/eun jo
Attorney Docket Number:	P2317US00

Filed as Large Entity

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	930	930
		Total in USD ($)		**930**

Electronic Acknowledgement Receipt

EFS ID:	15049516
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	Light Emitting Device and Method of Manufacturing the Same
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/Sangwon Kim
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
Receipt Date:	26-FEB-2013
Filing Date:	26-DEC-2007
Time Stamp:	13:45:40
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$930
RAM confirmation Number	10
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Request for Continued Examination (RCE)	P2317US00-RCE.pdf	76681 93f9fba9aac880f9c903a0f33212a01d505512f1	no	3
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30160 b6daa57ddf737d0cef6a9c644ac1944443f9100c	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	106841	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/993,965	12/26/2007	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	02/26/2013	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 19	Minus	** 22	= 0	X $ =		OR	X $62=	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $ =		OR	X $250=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/AMANDA FORD/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

58027 7590 03/06/2013

H.C. PARK & ASSOCIATES, PLC
1894 PRESTON WHITE DRIVE
RESTON, VA 20191

EXAMINER	
NGUYEN, THINH T	
ART UNIT	PAPER NUMBER
2897	

DATE MAILED: 03/06/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/993,965	12/26/2007	Jong Lam Lee	P2317US00	2191

TITLE OF INVENTION: LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1770	$300	$0	$2070	06/06/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

58027 7590 03/06/2013
H.C. PARK & ASSOCIATES, PLC
1894 PRESTON WHITE DRIVE
RESTON, VA 20191

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/993,965	12/26/2007	Jong Lam Lee	P2317US00	2191

TITLE OF INVENTION: LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1770	$300	$0	$2070	06/06/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, THINH T	2897	257-088000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee
❑ Publication Fee (No small entity discount permitted)
❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

❑ A check is enclosed.
❑ Payment by credit card. Form PTO-2038 is attached.
❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/993,965	12/26/2007	Jong Lam Lee	P2317US00	2191

58027 7590 03/06/2013

H.C. PARK & ASSOCIATES, PLC
1894 PRESTON WHITE DRIVE
RESTON, VA 20191

EXAMINER	
NGUYEN, THINH T	
ART UNIT	PAPER NUMBER
2897	

DATE MAILED: 03/06/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 233 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 233 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	11/993,965	LEE ET AL.	
	Examiner	Art Unit	
	THINH T. NGUYEN	2897	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *02/26/2013*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *1-2,4,17-29,33-35*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/Thinh T Nguyen/
Primary Examiner
Art Unit 2897

DETAILED ACTION

1. This is in response to Applicant filing a Request for Continuing Examination (RCE) on February 26th 2013 with claims 1-2,4,17-35 pending in the Application.

Reason for allowance

2. Claims 1-2, 4,17-29,33-35 are allowed.

The following is an examiner's statement of reason for allowance:

Group I: claims 1-2,4,33-34 :

None of the references of record teaches or suggests the claimed LIGHT EMITTING DEVICE having the limitations:

--" a side surface comprising the N-type or P-type semiconductor layer of the light emitting cell has a slope of approximately 20 degree to approximately 80 degree from a horizontal plane based on the substrate, wherein a P-type electrode and a N-type electrode are disposed on the respective P-type semiconductor layer and the N-type semiconductor layer and a transparent layer is disposed on the P-type semiconductor layer, and wherein an ohmic layer is disposed on the transparent layer or the N- type semiconductor layer, respectively, and a portion of the rear surface of the substrate is removed and Al, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof is deposited on the removed portion of the rear surface to enhance a heat dissipation, and wherein an insulation layer is disposed to continuously cover a surface of the substrate, a top and the inclined surface of the light emitting cell."--

In combination with all other limitations as recited in claim 1

Group II: claims 17-29,35 :

None of the references of record teaches or suggests the claimed LIGHT EMITTING DEVICE having the limitations:

--" the first semiconductor layer of at least one of the light emitting cells is coupled to the second semiconductor layer of an another adjacent light emitting cell, wherein an electrode of the first semiconductor and an electrode of the second semiconductor are disposed on the respective first semiconductor and the second semiconductor and a transparent layer is disposed on the second semiconductor layer, and wherein an ohmic layer is disposed on the transparent layer or the first semiconductor, and a portion of the rear surface of the substrate is removed and AI, Ti, Ag, W, Ta, Ni, Ru or an alloy thereof is deposited on the removed portion of the rear surface to enhance a heat dissipation, and wherein an insulation layer is disposed to continuously cover a surface of the substrate, a top and the inclined surface of the light emitting cell."--

In combination with all other limitations as recited in claim 17

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

CONCLUSION

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The

examiner can normally be reached on Monday-Friday 9:30am-6:30pm.If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fernando Toledo can be reached at 571-272-1867.The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thinh T Nguyen/

Primary Examiner

Art unit 2897

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	7	11/993965	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 20:31
L2	623983	(transparent clear transpare$3) near9 (layer film)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 20:49
L3	84872	(p-type (p near3 (type dop$4))) near9 (semiconductor semi-conductor) near9 (layer film)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 20:51
L4	5473	2 same 3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 20:51
L5	545	4 same disposed	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 20:52
L6	131836	(plurality plural$4) with(LED light near9 emitting near9 (diode element device))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 20:54
L7	134	5 and 6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 20:55
L8	23418	(portion part) near9 (rear bottom) near9 surface near9 substrate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 20:56
L9	3488	8 same remov$4	US-PGPUB; USPAT;	OR	ON	2013/03/03 20:57

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L10	0	9 same substrate same (metal$4 alloy) same deposit$4 same ((heat thermal) near9 dissipation)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 20:59
L11	0	1 and 7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 20:59
L12	7	4 and 1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 21:00
L13	0	5 and 1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 21:00
L19	43	"18" same substrate same (metal$4 alloy) same deposit$4 same ((heat thermal) near9 dissipation)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 21:07
L22	6383	(257/100,266,88,90,e33.064).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/03/03 21:12
L23	482	(257/e33.064).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/03/03 21:12
L24	18778	(257/98,99,103,81,82,86).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/03/03 21:13
L25	2453	(362/231).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/03/03 21:13
L26	0	("12and22").PN.	US-PGPUB; USPAT;	OR	OFF	2013/03/03 21:13

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L27	6	12 and 22	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 21:14
L28	0	22 and 10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 21:14
L29	0	24 and 10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 21:14
L30	51	24 and 25	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 21:14
L31	0	25 and 12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 21:15
L32	6687	(438/22,24,46,47).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/03/03 21:52
L33	2	12 and 32	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 21:53
L34	0	32 and 28	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 21:54

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L14	186957	(transparent clear transpare$3) near9 (layer film)	USPAT; UPAD	OR	ON	2013/03/03 21:05
L15	28228	(p-type (p near3 (type dop$4))) near9	USPAT;	OR	ON	2013/03/03

		(semiconductor semi-conductor) near9 (layer film)	UPAD			21:05
L16	1694	14 same 15	USPAT; UPAD	OR	ON	2013/03/03 21:06
L17	184	16 same disposed	USPAT; UPAD	OR	ON	2013/03/03 21:06
L18	8839	(portion part) near9 (rear bottom) near9 surface near9 substrate	USPAT; UPAD	OR	ON	2013/03/03 21:07
L20	2	18 same substrate same (metal$4 alloy) same deposit$4 same ((heat thermal) near9 dissipation)	USPAT; UPAD	OR	ON	2013/03/03 21:08
L21	0	17 and 20	USPAT; UPAD	OR	ON	2013/03/03 21:10

3/ 3/ 2013 9:54:49 PM
C:\ Users\ tnguyen31\ Documents\ EAST\ Workspaces\ east new.wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11993965	LEE ET AL.
	Examiner	Art Unit
	THINH T NGUYEN	2818

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	100, 266,88,90,e33.064,98,99,103,81,82,85	9/16/09	ttn
362	231	5/27/12	TTN
438	22,24,46,47	3/3/13	TTN

SEARCH NOTES		
Search Notes	Date	Examiner
east	9/16/09	ttn
east	1/30/10	TTN
east	6/20/10	TTN
east	5/27/12	TTN
EAST	12/17/12	TTN
east	3/3/13	TTN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
257	88,81,98	3/3/13	TTN
east	text	3/3/13	TTN

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CONFIRMATION NO. 2191

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/993,965	12/26/2007	257	2897	P2317US00

APPLICANTS

Jong Lam Lee, Pohang, KOREA, REPUBLIC OF;
Jae Ho Lee, Yongin, KOREA, REPUBLIC OF;
Yeo Jin Yoon, Ansan, KOREA, REPUBLIC OF;
Eu Jin Hwang, Siheung, KOREA, REPUBLIC OF;
Dae Won Kim, Seoul, KOREA, REPUBLIC OF;

**** CONTINUING DATA ***************************

This application is a 371 of PCT/KR2006/002427 06/22/2006

**** FOREIGN APPLICATIONS ***************************

REPUBLIC OF KOREA 1020050053797 06/22/2005
REPUBLIC OF KOREA 1020050055179 06/24/2005
REPUBLIC OF KOREA 1020060021801 03/08/2006

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

05/08/2008

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /THINH T NGUYEN/ Examiner's Signature	☑ Met after Allowance /TTN/ Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		KOREA, REPUBLIC OF	11	16	3

ADDRESS

H.C. PARK & ASSOCIATES, PLC
1894 PRESTON WHITE DRIVE
RESTON, VA 20191
UNITED STATES

TITLE

Light Emitting Device and Method of Manufacturing the Same

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BIB (Rev. 05/07).

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11993965	LEE ET AL.
	Examiner	**Art Unit**
	THINH T NGUYEN	2897

CPC		
Symbol	**Type**	**Version**

CPC Combination Sets				
Symbol	**Type**	**Set**	**Ranking**	**Version**

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION									
CLASS	**SUBCLASS**	**CLAIMED**					**NON-CLAIMED**				
257	88	H	0	1	L	33 / 00 (2010.01.01)					
CROSS REFERENCE(S)											
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**										
257	88	85	98	E33.064							
438	22	24	46	47							

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	19	
/THINH T NGUYEN/ Primary Examiner.Art Unit 2897	03/03/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	FIG 29

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11993965	LEE ET AL.
	Examiner	**Art Unit**
	THINH T NGUYEN	2897

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	19	
/THINH T NGUYEN/ Primary Examiner.Art Unit 2897	03/03/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	FIG 29

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Part of Paper No. 20130303

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11993965	LEE ET AL.
	Examiner	**Art Unit**
	THINH T NGUYEN	2897

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	33												
2	2	18	34												
3	4	19	35												
4	17														
5	18														
6	19														
7	20														
8	21														
9	22														
10	23														
11	24														
12	25														
13	26														
14	27														
15	28														
16	29														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	19	
/THINH T NGUYEN/ Primary Examiner.Art Unit 2897	03/03/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	FIG 29

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	7	11/993965	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 20:31
L2	623983	(transparent clear transpare$3) near9 (layer film)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 20:49
L3	84872	(p-type (p near3 (type dop$4))) near9 (semiconductor semi-conductor) near9 (layer film)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 20:51
L4	5473	2 same 3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 20:51
L5	545	4 same disposed	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 20:52
L6	131836	(plurality plural$4) with(LED light near9 emitting near9 (diode element device))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 20:54
L7	134	5 and 6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 20:55
L8	23418	(portion part) near9 (rear bottom) near9 surface near9 substrate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 20:56
L9	3488	8 same remov$4	US-PGPUB; USPAT;	OR	ON	2013/03/03 20:57

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L10	0	9 same substrate same (metal$4 alloy) same deposit$4 same ((heat thermal) near9 dissipation)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 20:59
L11	0	1 and 7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 20:59
L12	7	4 and 1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 21:00
L13	0	5 and 1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 21:00
L19	43	"18" same substrate same (metal$4 alloy) same deposit$4 same ((heat thermal) near9 dissipation)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 21:07
L22	6383	(257/100,266,88,90,e33.064).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/03/03 21:12
L23	482	(257/e33.064).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/03/03 21:12
L24	18778	(257/98,99,103,81,82,86).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/03/03 21:13
L25	2453	(362/231).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/03/03 21:13
L26	0	("12and22").PN.	US-PGPUB; USPAT;	OR	OFF	2013/03/03 21:13

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L27	6	12 and 22	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 21:14
L28	0	22 and 10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 21:14
L29	0	24 and 10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 21:14
L30	51	24 and 25	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 21:14
L31	0	25 and 12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/03/03 21:15

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L14	186957	(transparent clear transpare$3) near9 (layer film)	USPAT; UPAD	OR	ON	2013/03/03 21:05
L15	28228	(p-type (p near3 (type dop$4))) near9 (semiconductor semi-conductor) near9 (layer film)	USPAT; UPAD	OR	ON	2013/03/03 21:05
L16	1694	14 same 15	USPAT; UPAD	OR	ON	2013/03/03 21:06
L17	184	16 same disposed	USPAT; UPAD	OR	ON	2013/03/03 21:06
L18	8839	(portion part) near9 (rear bottom) near9 surface near9 substrate	USPAT; UPAD	OR	ON	2013/03/03 21:07
L20	2	18 same substrate same (metal$4 alloy) same deposit$4 same ((heat thermal) near9 dissipation)	USPAT; UPAD	OR	ON	2013/03/03 21:08
L21	0	17 and 20	USPAT; UPAD	OR	ON	2013/03/03 21:10

3/3/2013 9:16:16 PM
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PTO/SB/08a (08-09)
Approved for use through 07/31/2009. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	11993965
Filing Date	2007-12-26
First Named Inventor	Jong Lam Lee
Art Unit	2818
Examiner Name	NGUYEN, THINH T
Attorney Docket Number	P2317US00

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2004-071644	JP		2004-03-04	NICHIA CHEM IND LTD		☐
	2	2004-273746	JP		2004-09-30	HITACHI CABLE LTD		☐
	3	2005-136130	JP		2005-05-26	KYOCERA CORP		☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH
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Receipt date: 01/27/2010	Application Number	11993965	11993965 - GAU: 2818
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	2007-12-26	
(Not for submission under 37 CFR 1.99)	First Named Inventor	Jong Lam Lee	
	Art Unit	2818	
	Examiner Name	NGUYEN, THINH T	
	Attorney Docket Number	P2317US00	

	4	2001-156331	JP		2001-06-08	NICHIA CHEM IND LTD		☐

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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
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EXAMINER SIGNATURE

Examiner Signature	/Thinh Nguyen/	Date Considered	01/30/2010

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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Receipt date: 01/27/2010	Application Number	11993965	11993965 - GAU: 2818
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)	Filing Date	2007-12-26	
	First Named Inventor	Jong Lam Lee	
	Art Unit	2818	
	Examiner Name	NGUYEN, THINH T	
	Attorney Docket Number	P2317US00	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2010-01-27
Name/Print	Hae-Chan Park	Registration Number	50114

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Examiner /Thinh T. Nguyen/ Date: 3/28/13

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Examiner /Thuan T. Nguyen/ Date: 3/28/13

ALL REFERENCES CONSIDERED EXCEPT WHERE LINE THROUGH /TTN/

EFS Web 2.1.15

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/993,965	12/26/2007	Jong Lam Lee	P2317US00	2191

58027 7590 04/05/2013

H.C. PARK & ASSOCIATES, PLC
1894 PRESTON WHITE DRIVE
RESTON, VA 20191

EXAMINER	
NGUYEN, THINH T	
ART UNIT	**PAPER NUMBER**
2897	

NOTIFICATION DATE	DELIVERY MODE
04/05/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATENT@PARK-LAW.COM

UNITED STATES DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office
Address : COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
11/993,965	26 December, 2007	LEE ET AL.	P2317US00

		EXAMINER	
H.C. PARK & ASSOCIATES, PLC 1894 PRESTON WHITE DRIVE RESTON, VA 20191		THINH T. NGUYEN	
		ART UNIT	PAPER
		2897	20130329

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

Attached is considered IDS on February 5th 2010

/Thinh T Nguyen/
Primary Examiner
Art Unit 2897

PTO-90C (Rev.04-03)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

H.C. PARK & ASSOCIATES, PLC
1894 Preston White Dr.
Reston, VA 20191

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/993,965	12/26/2007	Jong Lam Lee	P2317US00	2191

TITLE OF INVENTION:

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1780	$300	$0	$2080	06/06/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 H.C. PARK & ASSOCIATES, PLC
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Seoul Opto Device Co., Ltd.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Ansan-si, Republic of Korea

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☑ Issue Fee
☑ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.
☑ Payment by credit card.
☑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-3698 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Sangwon S. Kim/ Date June 4, 2013

Typed or printed name Sangwon S. Kim Registration No. 54,221

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The **Privacy Act of 1974** (**P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	Docket No.: P2317US00
Jong Lam LEE, *et al.*	
Serial No.: 11/993,965	Group Art Unit: 2897
Confirmation No.: 2191	
Filed: December 26, 2007	Examiner: NGUYEN, Thinh T.

For: **LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME**

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Sir:

Applicants appreciate the indication in the Notice of Allowance mailed March 6, 2013 that claims 1, 2, 4, 17-29, and 33-35 are allowed. While Applicants agree these claims are patentable over the cited references, Applicants do not agree that patentability resides in each feature exactly as expressed in the claims, nor that each feature is required for patentability of each claim.

Respectfully Submitted,

/Sangwon S. Kim/

Sangwon S. Kim
Reg. No. 54,221

Date: June 4, 2013

CUSTOMER NUMBER: 58027
HCP/SSK/eyj

Electronic Patent Application Fee Transmittal

Application Number:	11993965
Filing Date:	26-Dec-2007
Title of Invention:	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jong Lam Lee
Filer:	Hae-Chan Park/eun Jo
Attorney Docket Number:	P2317US00

Filed as Large Entity

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	1780	1780
Publ. Fee- Early, Voluntary, or Normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**2080**

Electronic Acknowledgement Receipt

EFS ID:	15940243
Application Number:	11993965
International Application Number:	
Confirmation Number:	2191
Title of Invention:	LIGHT EMITTING DEVICE AND METHOD OF MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jong Lam Lee
Customer Number:	58027
Filer:	Hae-Chan Park/Sangwon Kim
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P2317US00
Receipt Date:	04-JUN-2013
Filing Date:	26-DEC-2007
Time Stamp:	16:36:56
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$2080
RAM confirmation Number	3967
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Issue Fee Payment (PTO-85B)	P2317US00-IssueFee.pdf	110254 797ef3118f7503b84b49ad327b3684df33790dd3	no	2
Warnings:					
Information:					
2	Post Allowance Communication - Incoming	P2317US00-RFAComments.pdf	13932 20ea0681b603e414818c092139ff04720decbff0	no	1
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	32102 0fe2c9397fb5ca1308fefb7dcd4859dec3578b2c	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	156288		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/993,965	07/02/2013	8476648	P2317US00	2191

58027 7590 06/12/2013

H.C. PARK & ASSOCIATES, PLC
1894 PRESTON WHITE DRIVE
RESTON, VA 20191

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 233 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Jong Lam Lee, Pohang, KOREA, REPUBLIC OF;
Jae Ho Lee, Yongin, KOREA, REPUBLIC OF;
Yeo Jin Yoon, Ansan, KOREA, REPUBLIC OF;
Eu Jin Hwang, Siheung, KOREA, REPUBLIC OF;
Dae Won Kim, Seoul, KOREA, REPUBLIC OF;

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