

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. AND
SAMSUNG ELECTRONICS AMERICA, INC.
Petitioner

v.

SINOTECHNIX LLC
Patent Owner

Case IPR2025-00332

PETITION FOR *INTER PARTES* REVIEW OF

U.S. PATENT NO. 7,951,626

CHALLENGING CLAIMS 1, 3, 7, 9, 13, AND 15
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104

TABLE OF CONTENTS

	<u>Page</u>
I. Introduction.....	1
II. Mandatory Notices.....	2
A. Real Parties-In-Interest.....	2
B. Related Matters.....	2
C. Counsel	3
D. Service Information	3
III. Fees	4
IV. Certification Of Grounds For Standing	4
V. Identification Of Challenge And Relief Requested.....	4
A. Identification Of Prior Art.....	4
B. Grounds for Challenge	5
VI. Technology Background.....	6
A. Light Emitting Diodes	6
B. Photolithography	8
VII. Overview Of The '626 Patent.....	10
A. Alleged Problem.....	10
B. Purported Invention.....	10
C. Prosecution History	12
VIII. Level Of Ordinary Skill In The Art.....	14
IX. Claim Construction.....	15

X.	Specific Grounds Of Invalidity.....	16
A.	Ground I: Eliashevich In Combination With Rabinzohn Renders Obvious Claims 1 and 3.	16
1.	Eliashevich (EX1003).....	16
2.	Rabinzohn (EX1004)	21
3.	Eliashevich In Combination With Rabinzohn ("Eliashevich-Rabinzohn").....	23
1.	Claim 1	30
2.	Claim 3	40
B.	Ground II: Eliashevich In Combination With Rabinzohn And Yoo Renders Obvious Claim 7.....	42
1.	Claim 7	42
C.	Ground III: Eliashevich In Combination With Rabinzohn and Huang Renders Obvious Claims 9 and 15.	47
1.	Huang (EX1006).....	47
2.	Eliashevich In Combination With Rabinzohn And Huang ("Eliashevich-Rabinzohn-Huang").....	48
3.	Claim 9.....	53
4.	Claim 15	59
D.	Ground IV: Eliashevich In Combination With Rabinzohn, Huang, And Yoo Renders Obvious Claim 13.....	59
1.	Claim 13	59
E.	Ground V: Horio Anticipates Claims 9, 13, And 15.....	63
1.	Horio (EX1007)	63

2.	Claim 9	68
3.	Claim 13	85
4.	Claim 15	85
XI.	Discretionary Factors Favor Institution	86
A.	<i>Advanced Bionics</i> Factors Favor Institution.	86
B.	Discretionary Denial Under <i>Fintiv</i> Is Not Appropriate.	86
1.	No Evidence Regarding A Stay	87
2.	Parallel Proceeding Trial Date	87
3.	Investment In Parallel Proceeding	88
4.	Overlapping Issues With Parallel Proceeding	88
5.	Identity Of Parties	89
6.	Other Circumstances, Including The Merits.....	89
C.	<i>General Plastic</i> Factors Favor Institution	89
XII.	Conclusion	90

TABLE OF AUTHORITIES

Page

Cases

<i>Advanced Bionics LLC v. MED-EL Elektromedizinische Geräte GmbH</i> , IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020)	86
<i>Apple Inc. v. Fintiv, Inc.</i> , IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020)	87
<i>In re Genentech, Inc.</i> , 566 F.3d 1338 (Fed. Cir. 2009)	88
<i>Koninklijke Philips N.V. v. Quectel Wireless Sols. Co.</i> , No. 2023-1221, 2024 WL 3042238 (Fed. Cir. June 18, 2024)	53, 77
<i>Mformation Techs., Inc. v. Rsch. in Motion Ltd.</i> , 764 F.3d 1392 (Fed. Cir. 2014)	53
<i>Nidec Motor Corp. v. Zhongshan Broad Ocean Motor, Co.</i> , 868 F.3d 1013 (Fed. Cir. 2017)	16
<i>PEAG LLC v. Varta Microbattery GmbH</i> , IPR2020-01214, Paper 8, 17 (Jan. 6, 2021)	88
<i>Phillips v. AWH Corp.</i> , 415 F.3d 1303 (Fed. Cir. 2005)	15
<i>Sand Revolution II LLC v. Continental Intermodal Group – Trucking LLC</i> , IPR2019-01393, Paper 24 (June 16, 2020)	88
<i>UCB, Inc. v. Actavis Lab’s UT</i> , 65 F.4th 679 (Fed. Cir. 2023)	54

Statutes

35 U.S.C. § 314(a)	6
35 U.S.C. §102	4, 5, 6

Petition for *Inter Partes* Review of U.S. Patent No. 7,951,626
Claims 1, 3, 7, 9, 13, 15

35 U.S.C. §103.....4

35 U.S.C. §112.....6

Rules

37 C.F.R. § 42.100(b) 15

PETITIONER’S EXHIBIT LIST

Petitioner Exhibit No.	DESCRIPTION
1001	U.S. Patent No. 7,951,626 (“’626 Patent”)
1002	Declaration of Dr. Ioannis Kymissis
1003	PCT Application Publication No. WO2002/059983 (“Eliashevich”)
1004	U.S. Patent No. 5,378,309 (“Rabinzohn”)
1005	U.S. Patent Application Publication No. 2003/0189212 (“Yoo”)
1006	U.S. Patent No. 6,444,410 (“Huang”)
1007	U.S. Patent Application Publication No. 2005/0281303 (“Horio”)
1008	U.S. Patent Application Publication No. 2006/0169993 (“Fan”)
1009	U.S. Patent No. 7,053,419 (“Camras”)
1010	U.S. Patent No. 6,229,160 (“Krames”)
1011	H. Xiao, “Introduction to Semiconductor Manufacturing Technology,” “Chapter 6,” Prentice Hall, 2001
1012	File History of U.S. Patent No. 7,951,626
1013	File History of U.S. Application No. 11/993,965
1014	L.F. Thompson, “Introduction to Microlithography,” “Chapter 1. Introduction to Photolithography,” <i>ACS Symposium Series</i> Vol. 219, 1983 (“Thompson”) ¹
1015	D. J. Kim, “Characterization and Modeling of Positive Photoresist,” Memorandum No. UCB/ERL M84/65, 1984 (“Kim”)
1016	S. L. Morton et al., “Ultrasonic Sensor for Photoresist Process Monitoring,” <i>IEEE Transactions on Semiconductor Manufacturing</i> , Vol. 12, No. 3, August 1999 (“Morton”)
1017	E. J. Jewell et al., “The New Oxford American Dictionary,” Oxford University Press, p. 1286, 2001
1018	Docket Control Order in <i>Sinotechnix LLC v. Samsung Electronics et al.</i> , 2:24-cv-544-JRG-RSP
1019	Judicial Caseload For Eastern District of Texas
1020	Judge Gilstrap’s Case Schedule (May 4, 2026)
1021	T. Nakazawa et al., “Compact and monolithic coarse wavelength-division multiplexer-demultiplexer fabricated by use of a high-spatial-frequency transmission grating buried in a slab waveguide,”

¹ Available at <https://pubs.acs.org/doi/10.1021/bk-1983-0219.ch001>

Petition for *Inter Partes* Review of U.S. Patent No. 7,951,626
Claims 1, 3, 7, 9, 13, 15

Petitioner Exhibit No.	DESCRIPTION
	Vol. 29, Issue 11, pp. 1188-1190, 2004 (“Nakazawa”) ²
1022	U.S. Patent Application No. 2006/0231852 (“Kususe”)
1023	H. Jansen et al., “A survey on the reactive ion etching of silicon in microtechnology,” Micromechanics Europe 1995 Technical Digest, 1995 (“Jansen”)

² Available at <https://opg.optica.org/ol/abstract.cfm?uri=ol-29-11-1188>.

LISTING OF CHALLENGED CLAIMS

Claim 1

[1Pre] A method of manufacturing a light emitting device, comprising:

[1A] sequentially forming an N-type semiconductor layer, active layer, and P-type semiconductor layer on a substrate;

[1B] forming an etching mask pattern, of which a side surface is not perpendicular to but inclined at a slope from a horizontal plane, on the P-type semiconductor layer; and

[1C] removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern,

[1D-1] wherein forming the etching mask pattern comprises: forming a photoresist on the P-type semiconductor layer;

[1D-2] wherein forming the etching mask pattern comprises: ... exposing the photoresist to light; and

[1D-3] wherein forming the etching mask pattern comprises: ... developing the light-exposed photoresist without a baking process after the light exposure.

Claim 3

[3] The method as claimed in claim 1, further comprising the step of flip-chip bonding the substrate onto an additional submount substrate after the step of removing the P-type semiconductor layer and the etching mask pattern.

Claim 7

[7] The method as claimed in claim 1, wherein the photoresist with a thickness of 3 to 50 μm is used in the forming the etching mask pattern.

Claim 9

[9Pre] A method of manufacturing a light emitting device, comprising:

[9A] sequentially forming an N-type semiconductor layer, active layer, and P-type semiconductor layer on a substrate;

[9B] forming an etching mask pattern, of which a side surface is not perpendicular to but inclined at a slope from a horizontal plane, on the P-type semiconductor layer; and

[9C] removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern,

[9D-1] wherein forming the etching mask pattern comprises: forming a photoresist on the P-type semiconductor layer;

[9D-2] wherein forming the etching mask pattern comprises: ... exposing the photoresist to light;

[9D-3] wherein forming the etching mask pattern comprises: ... hard-baking and developing the photoresist; and

[9D-4] wherein forming the etching mask pattern comprises: ... etching a side surface of the developed photoresist to have the slope from the horizontal plane.

Claim 13

[13] The method as claimed in claim 9, wherein the photoresist with a thickness of 3 to 50 μm is used in the forming the etching mask pattern.

Claim 15

[15] The method as claimed in claim 9, wherein the hard-baking is performed at a temperature of 100 to 140°C.

I. Introduction

U.S. Patent No. 7,951,626 (“’626 Patent”) describes methods of manufacturing a light emitting device with a sloped side surface that purportedly improves light extraction efficiency. All claimed methods require, in part, (1) “forming an etching mask pattern” with a sloped side surface on a P-type semiconductor layer and (2) removing the etching mask pattern and the underlying P-type layer exposed through the etching mask pattern. Two independent claims of the ’626 Patent recite different ways of forming the etching mask pattern with a sloped side surface: claim 1 recites “exposing the photoresist to light; and developing the light-exposed photoresist *without a baking process after the light exposure*”; and claim 9 recites “*hard-baking* and developing the photoresist; and *etching a side surface of the developed photoresist* to have the slope from the horizontal plane.”

The claimed subject matter, however, was well known in the prior art, and the prior art references identified herein anticipate and/or render obvious the challenged claims. For example, Eliashevich (EX1003) discloses a method of manufacturing a light emitting device by forming a sloped etching mask pattern and using the sloped etching mask pattern to etch the underlying P-type layer, just like the ’626 Patent. Eliashevich in combination with Rabinzohn (EX1004)—which teaches forming an etching mask pattern with sloped side surfaces by “preetching” the etching mask

pattern without any mention of a baking process—would have rendered obvious claim 1, as detailed in Ground I. Similarly, Eliashevich in combination with Rabinzohn and Huang (EX1005)—which additionally teaches hard-baking the photoresist—would have rendered obvious claim 9, as detailed in Ground III. Likewise, Horio (EX1007) discloses a method of manufacturing a light emitting device by using a sloped etching mask pattern, where the sloped etching mask pattern is formed by hard-baking and etching the photoresist, thereby anticipating claim 9 as explained in Ground V.

Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively “Petitioner”) respectfully requests cancellation of Claims 1, 3, 7, 9, 13, and 15 of ’626 Patent.

II. Mandatory Notices

A. Real Parties-In-Interest

Petitioner identifies itself as a real party-in-interest (“RPI”).

B. Related Matters

The ’626 Patent is currently asserted against Petitioner by Sinotechnix LLC (“Patent Owner”) in *Sinotechnix LLC v. Samsung Electronics Co., Ltd. et al.*, No. 2:24-cv-00544 (EDTX) (“Litigation”). Petitioner has filed petitions for *inter partes* review of U.S. Patent Nos. 8,132,952 (IPR2025-00335), 7,748,873 (IPR2025-00333), 7,901,113 (IPR2025-00336), and 7,618,162 (IPR2025-00331), and plans to

Petition for *Inter Partes* Review of U.S. Patent No. 7,951,626
Claims 1, 3, 7, 9, 13, 15

file a petition for *inter partes* review of U.S. Patent No. 9,412,913, each of which is being asserted against Petitioner in the Litigation.

C. Counsel

Petitioner is filing a Power of Attorney appointing the practitioners associated with Customer Number 132,593. Petitioner designates the following lead and back-up counsel:

Lead Counsel	First Back-up Counsel
Taeg Sang Cho (Reg. No. 69,618) Desmarais LLP 230 Park Ave New York, NY 10169 Telephone: (212) 351-3400 Email: tcho@desmaraisllp.com	YuKai Bao (Reg. No. 79,686) Desmarais LLP 101 California St San Francisco, CA, 94111 Telephone: (415) 573-1822 Email: ybao@desmaraisllp.com
	Back-up Counsel
	Yung-Hoon Ha (Reg. No. 56,368) Desmarais LLP 230 Park Ave New York, NY 10169 Telephone: (212) 351-3400 Email: yha@desmaraisllp.com

D. Service Information

Post and hand delivery: Desmarais LLP

230 Park Ave, New York, NY 10169

Telephone: 212-351-3400

Fax: 212-351-3401

Email: Samsung-Sinotechnix-IPR@desmaraisllp.com

Please address all correspondence to counsel identified above. Petitioner consents to electronic service by email at:

Samsung-Sinotechnix-IPR@desmaraisllp.com

III. Fees

Petitioner submits herewith the required fees for this Petition. The Board is authorized to charge Desmarais LLP's deposit account, No. 50-6822, for any fee deficiency.

IV. Certification Of Grounds For Standing

Petitioner certifies that the '626 Patent is available for *inter partes* review and that Petitioner is not estopped or barred from requesting this *inter partes* review.

V. Identification Of Challenge And Relief Requested

Petitioner requests *inter partes* review and cancellation of claims 1, 3, 7, 9, 13, and 15 of the '626 Patent.

A. Identification Of Prior Art

The '626 Patent was filed on November 5, 2009, and claims priority to Korean Patent Application Nos. 10-2005-0053797, 10-2005-0055179, and 10-2006-0021801, filed June 22, 2005, June 24, 2005, and March 8, 2006, respectively. EX1001, Cover. Accordingly, this Petition applies pre-AIA provisions of 35 U.S.C. §§ 102 and 103.

The following references are pertinent to the grounds of unpatentability

presented below:

1. PCT Application Publication No. WO2002/059983 (“Eliashevich”) (EX1003³), filed November 16, 2001 and published August 1, 2002, is prior art under at least 35 U.S.C. § 102(b).

2. U.S. Patent No. 5,378,309 (“Rabinzohn”) (EX1004), filed August 5, 1992 and issued January 3, 1995, is prior art under at least 35 U.S.C. § 102(b).

3. U.S. Patent Application Publication No. 2003/0189212 (“Yoo”) (EX1005), filed April 9, 2002 and published October 9, 2003, is prior art under at least 35 U.S.C. § 102(b).

4. U.S. Patent No. 6,444,410 (“Huang”) (EX1006), filed October 14, 2000 and issued September 3, 2002, is prior art under at least 35 U.S.C. § 102(b).

5. U.S. Patent Application Publication No. 2005/0281303 (“Horio”) (EX1007), filed June 17, 2005 and published December 22, 2005, is prior art under at least 35 U.S.C. § 102(e).

None of the presented prior art references were considered during the prosecution of the ’626 Patent.

B. Grounds for Challenge

Petitioner requests cancellation of claims 1, 3, 7, 9, 13, and 15 of the ’626

³ Petitioner has added line numbers to EX1003 to aid with citations.

Patent under 35 U.S.C. §§ 102 and 103⁴ based on the following Grounds.

Ground	35 U.S.C.	Claims	Prior Art Reference(s)
I	§103	1, 3	Eliashevich, Rabinzohn
II	§103	7	Eliashevich, Rabinzohn, Yoo
III	§103	9, 15	Eliashevich, Rabinzohn, Huang
IV	§103	13	Eliashevich, Rabinzohn, Huang, Yoo
V	§102	9, 13, 15	Horio

This Petition, supported by the declaration of Dr. Kymissis (EX1002), demonstrates that there is a reasonable likelihood that Petitioner would prevail with respect to at least one challenged claim. 35 U.S.C. § 314(a). Petitioner respectfully requests institution.

VI. Technology Background

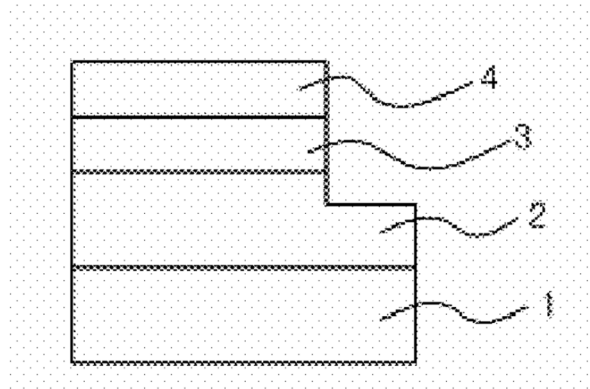
A. Light Emitting Diodes

A light emitting diode (“LED”) is a semiconductor device that emits light when current flows through it. As shown below, an LED typically includes an N-type semiconductor layer 2, an active layer 3 formed on the N-type semiconductor layer 2, and a P-type semiconductor layer 4 formed on the active layer 3. EX1001, 2:13-26 (background). Generally, the active layer 3—which provides a junction between the N-type layer 2 and the P-type layer 4—generates light when a voltage

⁴ Petitioner reserves the right to challenge the patentability of the claims under 35 U.S.C. §112 in other proceedings.

is applied across the N-type layer 2 and the P-type layer 4. EX1001, 1:28-31 (background).

[Figure 1]

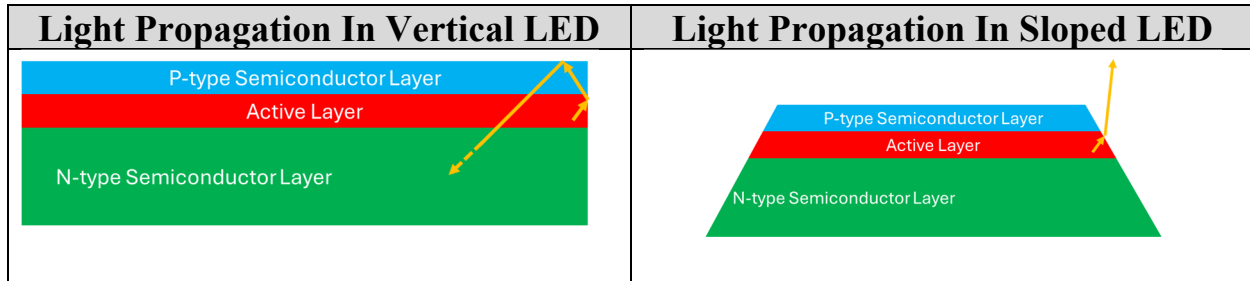


EX1001, Figure 1 (background). EX1002, ¶31.

One well-known issue with LEDs is that some of the generated light is trapped inside the LEDs. For example, the active layer typically generates light rays in all directions, and depending on the angle at which the generated light ray hits the physical interface between the LED and its surrounding material (*e.g.*, air), the light ray either escapes the LED through refraction (and becomes visible to outside observers) or is trapped inside the LED because it is totally reflected internally. EX1009, 1:20-23; EX1003, 5:7-25. The unintended light trapping reduces the LED's efficiency. EX1003, 5:26-30. EX1002, ¶32.

It was well known that the amount of trapped light can be reduced by sloping the LED's side surface. EX1010, 3:6-9. When the LED's side surface is sloped, the light escapes the LED with a higher likelihood because the light is more likely to

impinge on the interface at a shallower angle, as illustrated below. EX1008, [0020],
Figure 2.



EX1002, ¶33.

B. Photolithography

Semiconductor devices like LEDs typically include multiple layers that are patterned through a process called photolithography. Photolithography for semiconductors typically includes the following steps:

1. **Step 1:** Depositing a “thin film” of a semiconductor material;
2. **Step 2:** Applying a photoresist layer on the semiconductor layer;
3. **Step 3:** Exposing the photoresist layer to light through a photomask;
4. **Step 4:** Developing the exposed photoresist layer to form an etching mask pattern;
5. **Step 5:** Etching the exposed portions of the semiconductor layer;
6. **Step 6:** Removing the remaining photoresist.

EX1014, 1-4, 7-9.

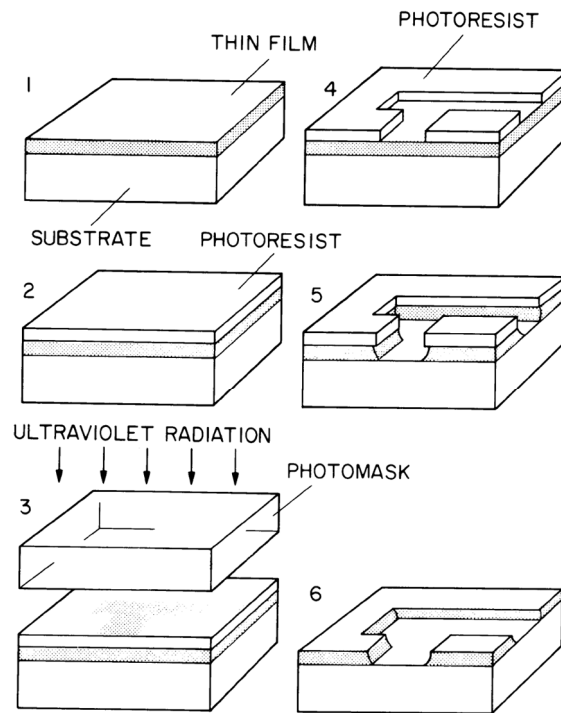
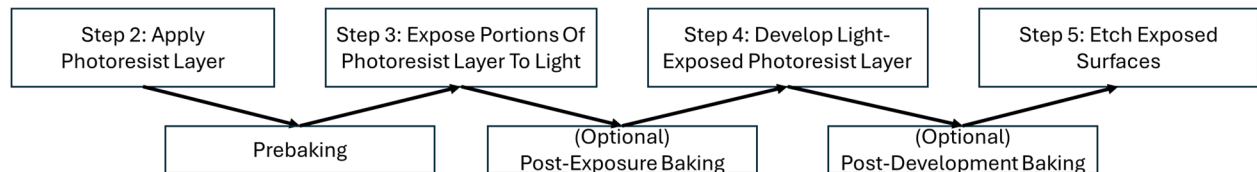


Figure 5. A typical photolithography process

EX1014, Figure 5. EX1002, ¶34.

Although not shown in the above illustration, photolithography commonly involves baking the photoresist layer at various stages, as illustrated in the bottom row of the figure below. EX1013, 22-23, 31-32, 35-36.



EX1002, ¶35.

For example, in step 2, the photoresist in its viscous form is applied on the underlying material layer using, for instance, a spin coater. EX1013, 13-16. Then

before step 3, the photoresist undergoes a “prebaking” or “soft bake” step that evaporates the solvent from the photoresist. EX1016, 1; EX1013, 13-14, 22-23. EX1002, ¶36.

Once the soft-baked photoresist is selectively exposed to light in step 3 but before it is developed in step 4, it is optionally subject to a post-exposure baking (“PEB”) step to make the exposure pattern more uniform. EX1016, 1; EX1013, 31-32. Subsequently, “[a]fter the development [in step 4,] the resist is *often baked again at higher temperature* for better adhesion” between the photoresist layer and the underlying material. EX1015, 11; EX1013, 35-36. EX1002, ¶¶37-38.

VII. Overview Of The ’626 Patent

A. Alleged Problem

The ’626 Patent relates to a method of manufacturing a “light emitting device.” EX1001, 1:21-26. The ’626 Patent states that conventional LEDs have vertical side surfaces, and the vertical side surfaces limit the LEDs’ efficiency because “a portion of light produced within the light emitting is device is totally reflected on the etched surface that is processed vertically from a horizontal plane.” EX1001, 2:56-67. EX1002, ¶39.

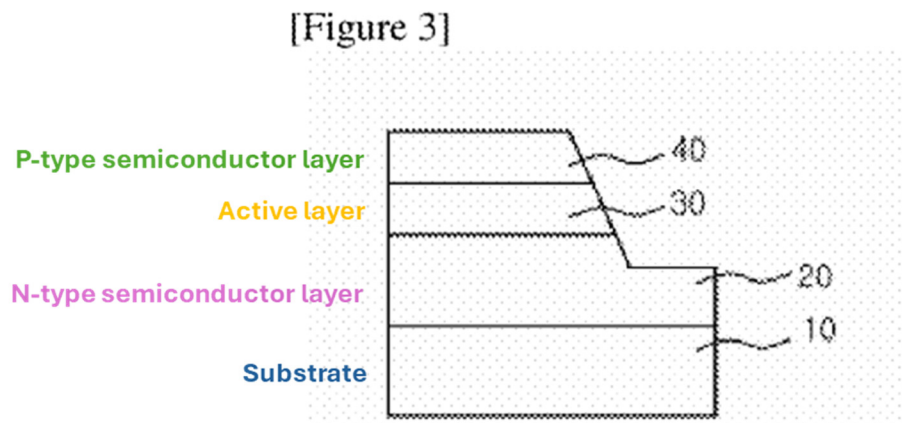
B. Purported Invention

The ’626 Patent purports to address the conventional LEDs’ limited efficiency by providing an LED with a sloped side surface, as shown in Figure 3 (see below).

The LED includes a substrate 10, an N-type semiconductor layer 20, an active layer 30, and a P-type semiconductor layer 40. EX1001, 5:47-56. According to the '626 Patent:

Each of side surfaces of the P-type semiconductor layer 40, the active layer 30 and a portion of the N-type semiconductor layer 20 has *a slope of 80 to 20° from a horizontal plane* such that a critical angle of light can be changed by such surfaces and *light can be easily extracted*. Therefore, luminous efficiency of a light emitting device can be improved.

EX1001, 5:50-56.



EX1001, Figure 3⁵. EX1002, ¶40.

To form the layers 20, 30, 40 with a sloped side surface, the '626 Patent discloses etching the layers “using the etching mask pattern [e.g., made using a

⁵ All annotations are added unless noted otherwise.

photoresist] with such a slope of the side surface.” EX1001, 6:60-7:5. *See also* EX1001, 7:27-40. EX1002, ¶41.

The ’626 Patent states that the etching mask pattern with a sloped side surface can be formed by: (1) providing a layer of photoresist; (2) soft-baking the photoresist layer at a temperature of 80 to 90 °C; (3) exposing the photoresist layer to light; and (4) developing the exposed photoresist layer without any baking after the light exposure so that a “developed side surface of the remaining photoresist is formed into an inclined surface not perpendicular (90°) to but inclined at a predetermined slope ... from a horizontal plane.” EX1001, 6:57-64, 7:6-9. EX1002, ¶42.

The ’626 Patent also states that the etching mask pattern with a sloped side surface can also be formed by: performing (1)-(3) as above; (4) hard-baking the exposed photoresist layer at a temperature of 100 to 140 °C; (5) developing the hard-baked photoresist layer; and (6) etching the side surface of the developed photoresist “to have a slope of 80 to 20° from a horizontal plane.” EX1001, 7:21-40 (“[I]f the photoresist is hard-baked at a temperature of 100 to 140° C. and then developed, the side surface of the developed photoresist may be etched to have a slope of 80 to 20° from a horizontal plane.”). EX1002, ¶43.

C. Prosecution History

The ’626 Patent originated from U.S. Patent Application No. 12/613,275 (“’275 Application”), filed November 5, 2009. The ’275 Application is a divisional

Petition for *Inter Partes* Review of U.S. Patent No. 7,951,626
Claims 1, 3, 7, 9, 13, 15

of U.S. Patent Application No. 11/993,965 (“’965 Application”), filed December 26, 2007, which is a national entry application of PCT Application No. PCT/KR2006/002427, filed June 22, 2006. The PCT application claims priority to Korean Patent Application No. 10-2005-0053797, filed June 22, 2005, Korean Patent Application No. 10-2005-0055179, filed June 24, 2005, and Korean Patent Application No. 10-2006-0021801, filed March 8, 2006. EX1012 [FH of the ’275 Appl.], 43-44; EX1013 [FH of the ’965 Appl.]. EX1002, ¶45.

The ’275 Application originally included claims 1-10. EX1012, 104-107. The sole independent claim 1 was directed to a method of manufacturing an LED using an etching mask pattern with a sloped side surface. EX1012, 104. In response to a restriction requirement, Applicant elected claims 1-2, and 5-10. EX1012, 496, 503. EX1002, ¶¶46-47.

In an Office Action dated December 23, 2010, the Examiner rejected claims 1-2, 5-7, and 10 for being obvious over U.S. Patent No. 7,213,942 (“Jiang ’942”) in view of U.S. Patent Publication No. 2005/0023537 (“Salam”) or U.S. Patent No. 7,598,149 (“Dawson”) or U.S. Patent No. 7,057,208 (“Akimoto”). EX1012, 516-520. And claim 9 was rejected for being indefinite. EX1012, 515. But the Examiner indicated that claim 8 would be allowable if written in an independent form. EX1012, 520. EX1002, ¶48.

In response to the Office Action, Applicant: (1) cancelled claims 8 and 9; (2)

amended claim 1 to include the allowable subject matter of the then-cancelled claim 8; (3) added new independent claim 11 directed to the subject matter of the then-cancelled claim 9; (4) added new dependent claims 12-17 that depend from claim 11; and (5) sought rejoinder of claims 3 and 4. EX1012, 552-562. EX1002, ¶49.

Subsequently, the Examiner allowed the pending claims 1-7, and 10-17, and the allowed claims issued as claims 1-15. EX1012, 566-573, 583. EX1002, ¶50.

VIII. Level Of Ordinary Skill In The Art

“Factors that may be considered in determining level of ordinary skill in the art include: (1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field.” *Env’t Designs, Ltd. v. Union Oil Co. of California*, 713 F.2d 693, 696 (Fed. Cir. 1983). However, “[n]ot all such factors may be present in every case, and one or more of these or other factors may predominate.” *Id.*

The ’626 Patent is directed to a method of manufacturing a semiconductor light emitting device. EX1001, Title, Abstract. As explained in Section VI.A, the field of light emitting devices and their manufacturing was well established by the

earliest claimed priority date of the '626 Patent—June 22, 2005⁶. The types of problems encountered in the art, such as the limited efficiency due to internal reflection, and solutions to those problems, such as providing a sloped side surface on the light emitting diode, were all well known in the art, as shown by prior art of record in the '626 Patent. *See, e.g.*, EX1008, [0020], Figure 2. EX1002, ¶51.

Accordingly, a person of ordinary skill in the relevant field or art (“POSITA”) as of the earliest claimed priority date of the '626 Patent would have had a Bachelor’s degree in Electrical Engineering, Material Science, Physics, or an equivalent field, and approximately two years of experience in the field of semiconductor manufacturing. Lack of professional experience can be substituted by additional education, and vice versa. EX1002, ¶52.

IX. Claim Construction

The claims should be construed “in accordance with the ordinary and customary meaning of such claims as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b); *see also Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). Moreover, the Board “need[s] only construe terms ‘that are in controversy, and only to the

⁶ Petitioner reserves all rights to challenge the claimed priority date of the '626 Patent in other forums.

extent necessary to resolve the controversy.’” *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor, Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Petitioner submits no terms require express construction for the purposes of this IPR.⁷ EX1002, ¶¶54-55.

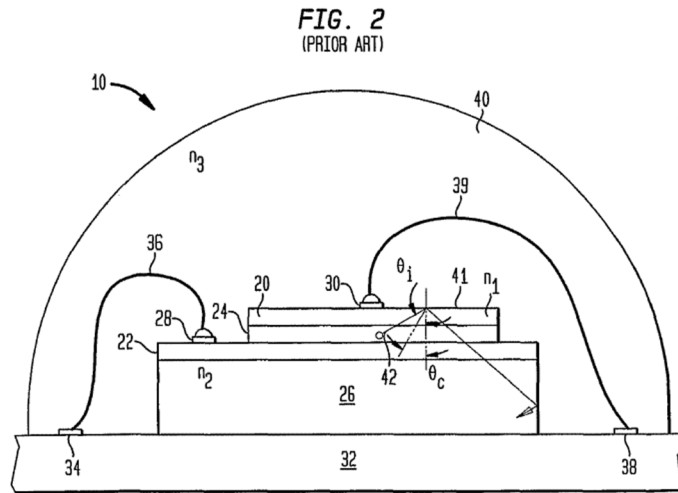
X. Specific Grounds Of Invalidity

A. Ground I: Eliashevich In Combination With Rabinzohn Renders Obvious Claims 1 and 3.

1. Eliashevich (EX1003)

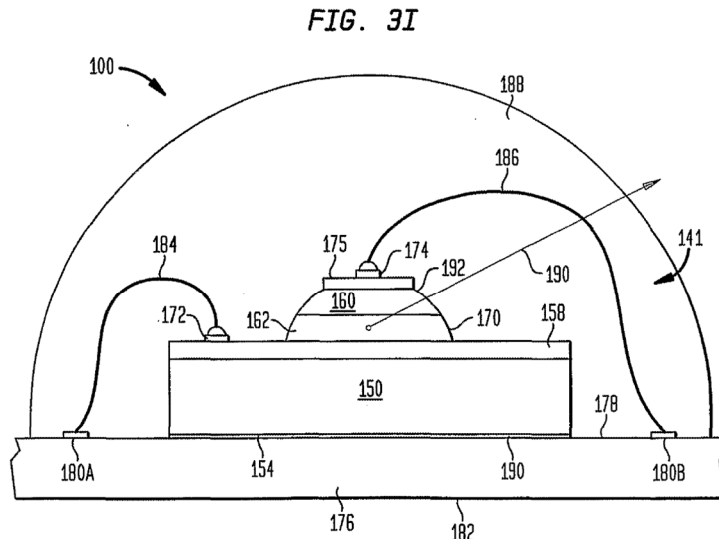
Eliashevich is directed to “methods of making light emitting diodes.... having optimized light extraction characteristics.” EX1003, 1:4-6. Eliashevich teaches that LEDs include “thin layers of semiconductor material of two opposite conductivity types, referred to as p-type and n-type” (EX1003, 1:8-11), and that light is generated at a junction layer sandwiched between the p-type and n-type layers (EX1003, 1:15-19). Eliashevich explains that in a conventional LED (shown below in Figure 2), “many of the light rays generated at the junction layer are never emitted from the package, but are totally internally reflected within the package” (EX1003, 5:26-28), which reduces efficiency. EX1003, 5:7-25, FIG. 2.

⁷ Petitioner reserves all rights to raise claim construction arguments in other forums.



EX1003, Figure 2. EX1002, ¶¶57-59.

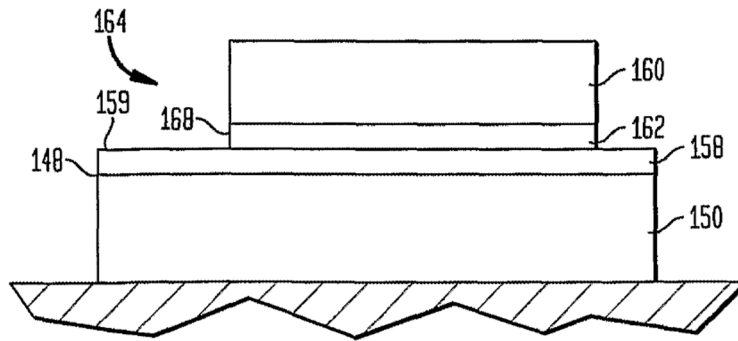
To improve the efficiency, Eliashevich teaches an LED with a non-vertical side surface that reduces internal reflection. EX1003, 6:10-19. Eliashevich's LED, shown in Figure 3I (below), has a p-type layer 160, n-type layer 158, and a junction layer 162 (EX1003, 14:33-15:13), and the p-type layer 160, the junction layer 162, and optionally a portion of the n-type layer 158 form a "mesa" (EX1003, 16:33-17:8). Eliashevich teaches that the side surface of the mesa—identified using the numeral 170—is made non-vertical such that the light generated by the junction layer 162 is extracted more easily. EX1003, 6:11-18, 19:17-26.



EX1003, Figure 3I. EX1002, ¶60.

Eliashevich explains the process of manufacturing an LED with a non-vertical side surface in connection with Figures 3A-3I. EX1003, 14:12-14. First, as shown in Figures 3A-3B, Eliashevich provides a substrate 150 (EX1003, 14:14-17) and forms a “stacked structure 110” that includes “a junction [layer] 162 between the n-type layers 158 and p-type layers 160.” EX1003, 14:33-15:13. Then, as shown in Figure 3C (below), “[t]he semiconductor structure 110 ... is preferably etched to form an upwardly projecting mesa 164 and a lower surface 159.” EX1003, 17:2-8.

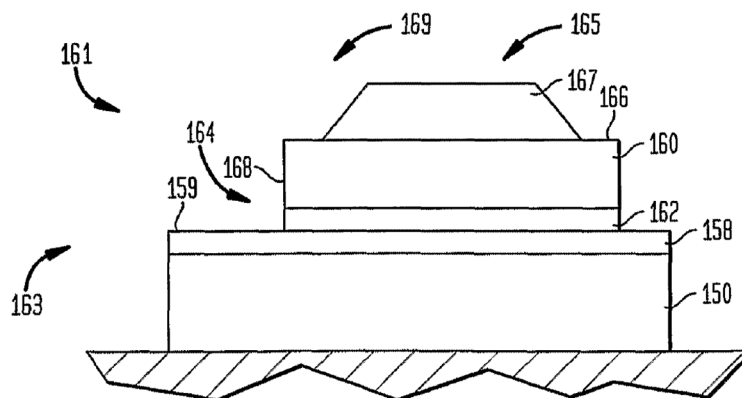
FIG. 3C



EX1003, Figure 3C. EX1002, ¶¶61-62.

Subsequently, Eliashevich deposits “[a] photoresist material 167 ... on the top surface 166 of mesa 164 and is exposed and developed to form a mask 165 having openings 169,” as shown in Figure 3E (below). EX1003, 18:19-21. Eliashevich explains that “[t]he *mask may be given a tapered shape*, as shown in FIG. 3D, utilizing *controlled processing* ... of the photoresist....” EX1003, 18:26-31. While silent on the additional details of such controlled processing, Eliashevich states that “[t]hese techniques are known in the art.” EX1003, 18:34-19:1.

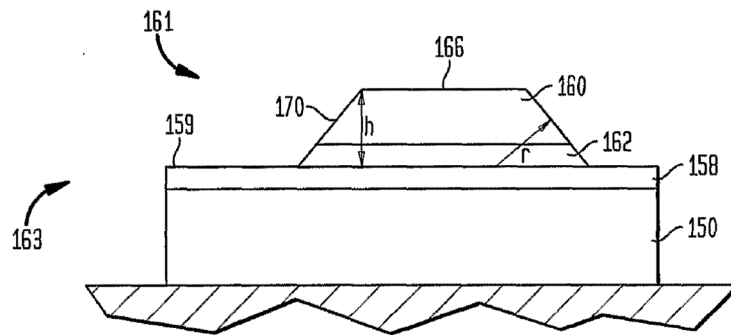
FIG. 3E



EX1003, Figure 3E. EX1002, ¶63.

Then, the subsequent dry-etching step (e.g., reactive-ion etching, or RIE) “removes the mask at an outside portion of the mesa first and then begins to remove semiconductor material from the p-type layers 160” to “form[] one or more radial surfaces 170 extending between top surface 166 and n-type layers 158 as shown in FIG. 3F,” shown below. EX1003, 18:31-19:10. “The radial surface 170 optimizes the amount of light that may be extracted ...” EX1003, 19:14-16.

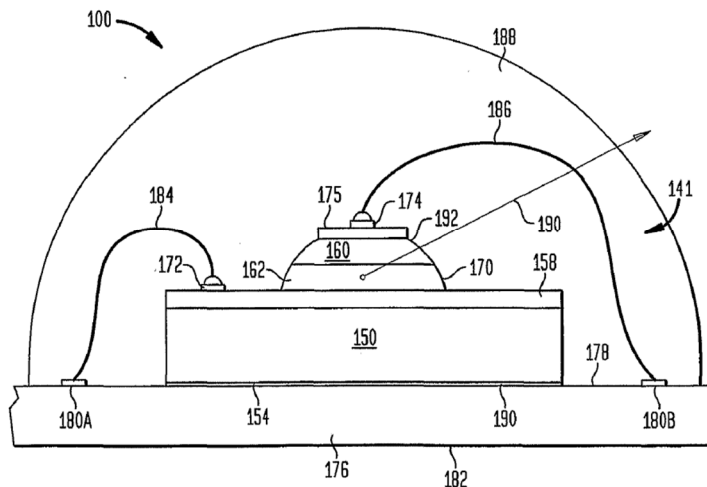
FIG. 3F



EX1003, Figure 3F. EX1002, ¶64.

Eliashevich then provides electrical connections to the p-type layer 160 and the n-type layer 158, and packages the LED as shown in Figure 3I (below). EX1003, 22:11-22.

FIG. 3I



EX1003, Figure 3I.⁸ EX1002, ¶¶65-66.

2. Rabinzohn (EX1004)

Rabinzohn teaches a “[m]ethod for controlling the etching profile of a layer of an integrated circuit” by transferring the side surface slope of a photoresist layer to the underlying layer. EX1004, Title, 3:35-43, 4:1-13. EX1002, ¶67.

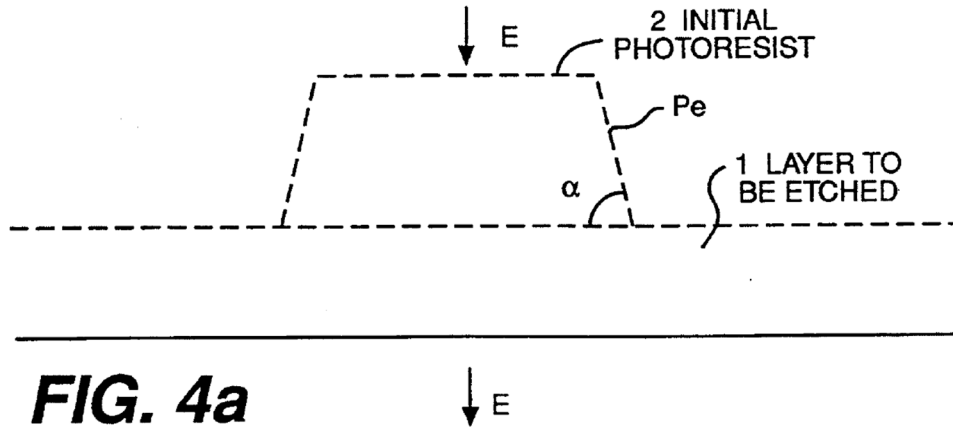
For example, Rabinzohn teaches providing a patterned photoresist layer 2 on the layer 1 that is to be etched. EX1004, 3:31-34. The patterned photoresist layer 2 has side surfaces that are “inclined at an angle α ” with respect to the underlying layer 1. EX1004, 7:21-38, Figure 4a. Rabinzohn explains that the sloped side surfaces

⁸ The side surface 170 in Figure 3I is curved, whereas the side surface 170 in Figure 3F is linear. That difference is immaterial to the challenged claims.

EX1002, ¶66.

on the patterned photoresist layer 2 are formed by “preeching” the photoresist layer

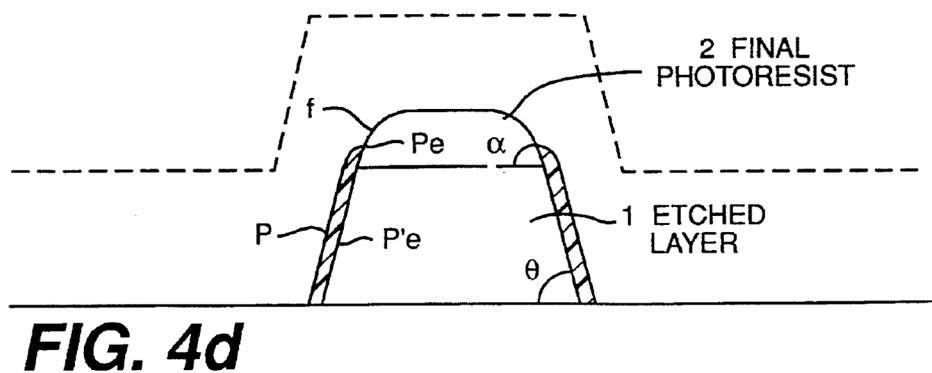
2. EX1004, 7:21-33, Figure 4a.



EX1004, Figure 4a. EX1002, ¶¶68-69.

Subsequently, Rabinzohn teaches performing a dry-etching called “reactive ionic etching” to transfer the shape of the photoresist layer 2 to the underlying layer

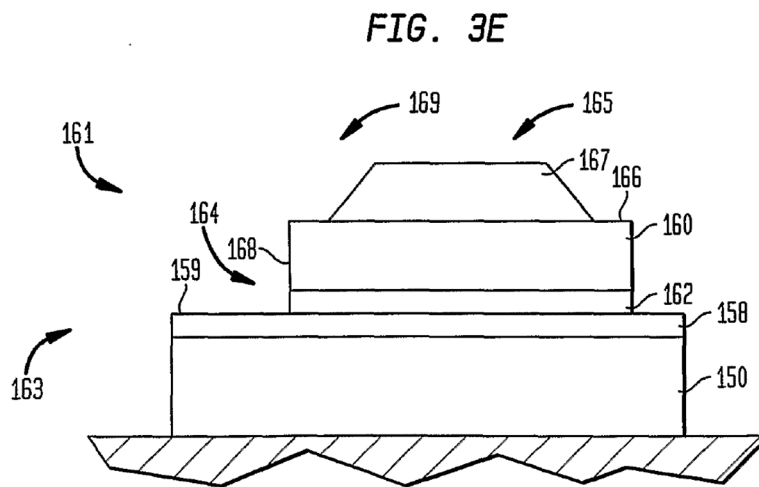
1. EX1004, 4:1-23, 7:38-47, Figure 4d.



EX1004, Figure 4d. EX1002, ¶70.

3. Eliashevich In Combination With Rabinzohn (“Eliashevich-Rabinzohn”)

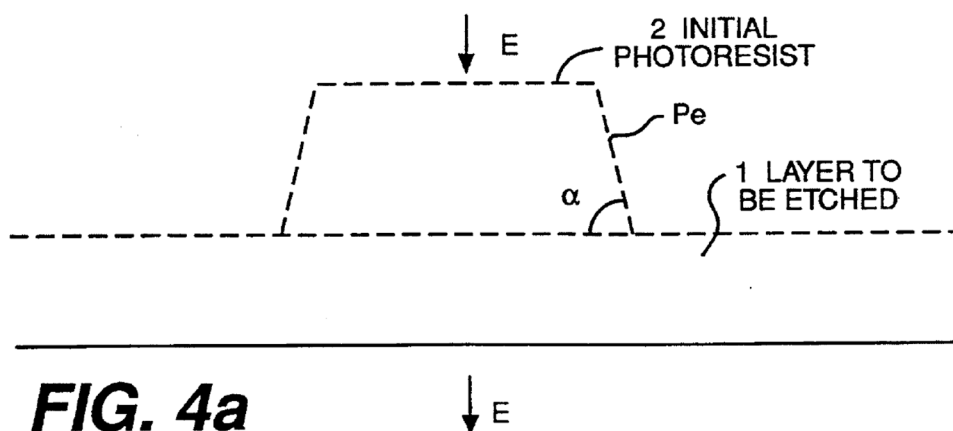
As explained in Section X.A.1 [Eliashevich], Eliashevich forms an LED with a non-vertical surface 170 by etching the LED’s mesa 164 using a photoresist layer 167 with a tapered side surface, as shown in Figure 3E. Eliashevich explains that the tapered photoresist layer 167 is formed “utilizing controlled processing ... of the photoresist,” but does not provide details on the “controlled processing ... of the photoresist.” EX1003, 18:26-29. Instead, Eliashevich states that “[t]hese techniques are known in the art.” EX1003, 18:34-19:1. Thus, a POSITA would have naturally looked to other prior art references for details on the “controlled processing ... of the photoresist.”



EX1003, Figure 3E. EX1002, ¶¶71-72.

Making a photoresist mask with a tapered side surface through “controlled processing ... of the photoresist” was well “known in the art.” EX1003, 18:26-19:1.

For example, as explained in Section X.A.2 [Rabinzohn], Rabinzohn teaches providing a photoresist mask with sloped side surfaces (referred to as “flanks”) by performing “preetching.” Specifically, Rabinzohn teaches that “in the case of FIG. 4, the initial masking photoresist layer 2, previously to the actual etching process, has been subjected to a *preetching stage*, the effect of which is to *generate etching flanks of slope Pe* inclined in relation to the free surface of the layer 1 to be etched, assumed to be horizontal, the etching flanks of the initial masking photoresist layer 2 being thus *inclined at an angle α* in relation to the abovementioned free surface.” EX1004, 7:21-30.

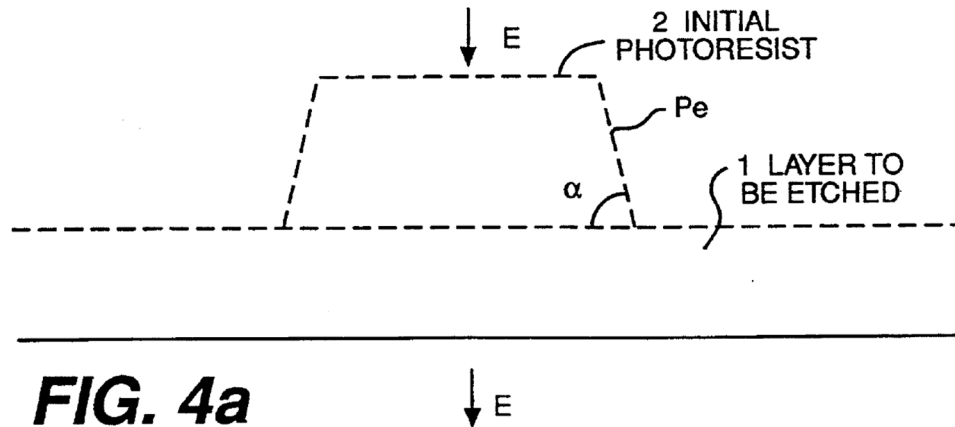


EX1004, Figure 4a. EX1002, ¶73.

Rabinzohn explains that the “preetching” process is separate from, and occurs before, the “actual etching process” (i.e., the reactive-ion etching process) that etches the underlying layer 1. EX1004, 7:21-27, 7:38-47, Figures 4b-4d. Rabinzohn also explains that unlike the “actual etching process,” the “preetching” process is “mild”

such that it selectively etches the photoresist layer 2 but not the underlying layer 1.

EX1004, 7:30-33 (“It will be noted that the *preetching process may consist of a mild etching*, which has the property of selectively attacking the initial masking photoresist layer 2, excluding an attack alternatively layer 1 to be etched.”).

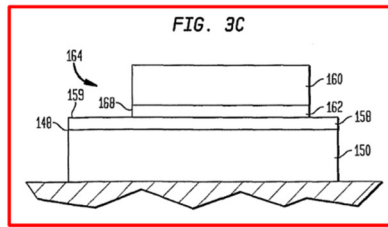


EX1004, Figure 4a. EX1002, ¶74.

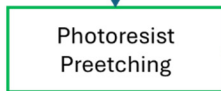
A POSITA would have found it obvious to combine Eliashevich with Rabinzohn so that Eliashevich’s photoresist with a tapered side surface is made using Rabinzohn’s preetching process. The combined process is illustrated below:

Eliashevich In Combination With Rabinzohn

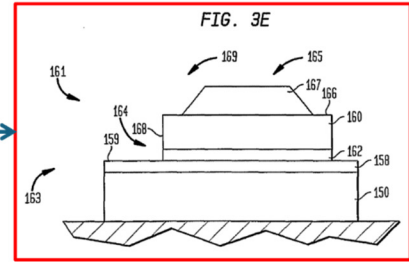
EX1003 [Eliashevich], Figure 3C



EX1003 [Eliashevich], 18:19-21



EX1004 [Rabinzohn], 7:21-37



EX1003 [Eliashevich], Figure 3E

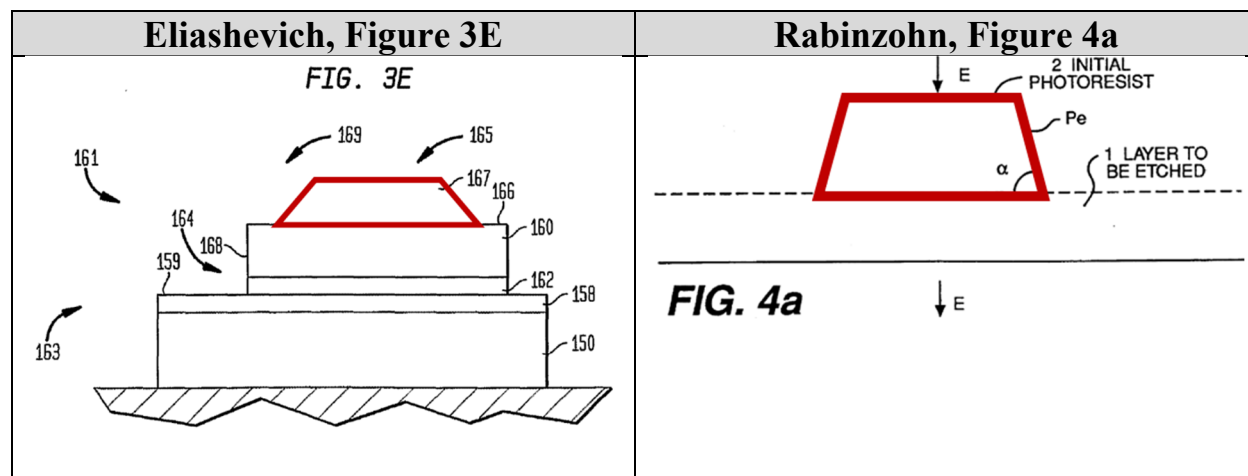
EX1002, ¶75.

**i. Reasons To Combine Eliashevich With Rabinzohn
With A Reasonable Expectation Of Success**

A POSITA would have been motivated to combine Eliashevich with Rabinzohn as described above for at least two reasons. **First**, Eliashevich specifically teaches that a patterned photoresist with a tapered side surface can be formed through “controlled processing ... of the photoresist” and suggests that a prior art method would be readily applicable. EX1003, 18:26-29, 18:34-19:1. And as Eliashevich suggested, Rabinzohn teaches such “controlled processing,” *i.e.*, Rabinzohn’s “preetching,” for tapering the side surfaces of the patterned photoresist. EX1004, 7:21-30, Figure 4a. Accordingly, the combination would have merely amounted to carrying out Eliashevich’s manufacturing method in accordance with the details disclosed by Rabinzohn based on Eliashevich’s express suggestion that

the patterned photoresist with a tapered side surface would be formed using the “controlled processing” of photoresist. EX1003, 18:26-29, 18:34-19:1, Figure 3E. EX1002, ¶¶76-78.

Second, a POSITA would have been motivated to use Rabinzohn’s preetching process to form Eliashevich’s photoresist having “tapered” side surfaces because Rabinzohn’s photoresist has nearly identical “sloped” side surfaces. For example, Eliashevich uses a patterned photoresist with a “tapered” side surface (outlined below in Figure 3E) to etch the underlying semiconductor layer so that the underlying layer forms a non-vertical side surface. *See, e.g.*, EX1003, 18:14-35, Figure 3F. Likewise, Rabinzohn uses a patterned photoresist with a “sloped” side surface (outlined below in Figure 4a) to etch the underlying semiconductor layer so that the underlying layer forms a non-vertical side surface. *See, e.g.*, EX1004, 3:35-43, 4:1-13, 7:38-8:2, 8:62-68, Figures 4a, 4d. As shown below, the trapezoidal shape of Rabinzohn’s “sloped” photoresist is nearly identical to the trapezoidal shape of Eliashevich’s “tapered” photoresist. Accordingly, a POSITA would have readily understood that Rabinzohn’s preetching method for making a “sloped” photoresist is readily applicable in Eliashevich’s fabrication process in making “tapered” photoresist.



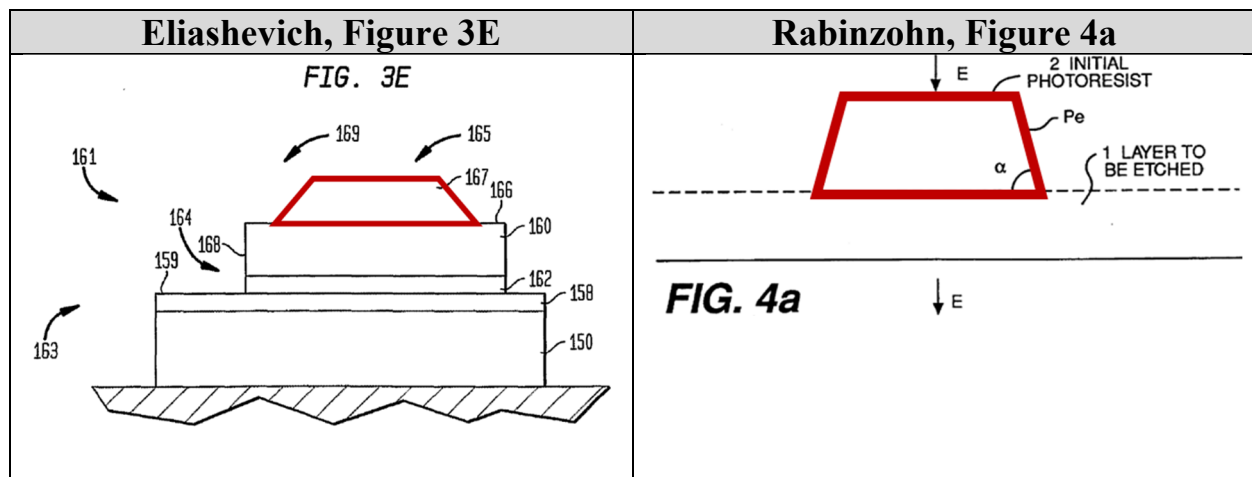
EX1002, ¶¶79-80.

A POSITA would have had a reasonable expectation of success in using Rabinzohn's preetching method to make Eliashevich's photoresist with a tapered side surface. ***First***, Eliashevich's method is compatible with Rabinzohn's preetching method. Both Eliashevich and Rabinzohn disclose using the tapered/sloped photoresist to etch the underlying semiconductor layer so that the underlying layer forms a non-vertical side surface. EX1003, 18:14-35; EX1004, 3:35-43, 4:1-13, 7:38-8:2, 10:62-68, Figure 4d. Accordingly, a POSITA would have understood that Rabinzohn's preetching process is compatible with, and readily applicable to, Eliashevich's method of manufacturing sloped photoresist. EX1002, ¶81.

Second, a POSITA would have understood that the particulars of the process of forming the tapered photoresist do not impact the subsequent dry-etching process that etches the underlying layer. In other words, the process of forming the tapered photoresist is substantially independent of the subsequent dry-etching process; a

POSITA would have understood that what matters is the shape of the photoresist, not the particular method of forming that shape. Accordingly, a POSITA would have had a reasonable expectation of success in using Rabinzohn's preetching process in Eliashevich's process of manufacturing sloped LEDs. EX1002, ¶82.

Third, the combination would have merely amounted to a simple application of Rabinzohn's preetching process for forming a sloped photoresist to yield predictable results of forming the tapered/sloped photoresist etching mask pattern taught in Eliashevich for use in etching underlying semiconductor layers. Indeed, both Eliashevich's process and Rabinzohn's process form a photoresist etching mask pattern with substantially similar sloped side surfaces. Compare EX1003, Figure 3E with EX1004, Figure 4a.



EX1002, ¶83.

At a minimum, it would have been obvious to try to manufacture Eliashevich's tapered photoresist 167 using Rabinzohn's preetching method.

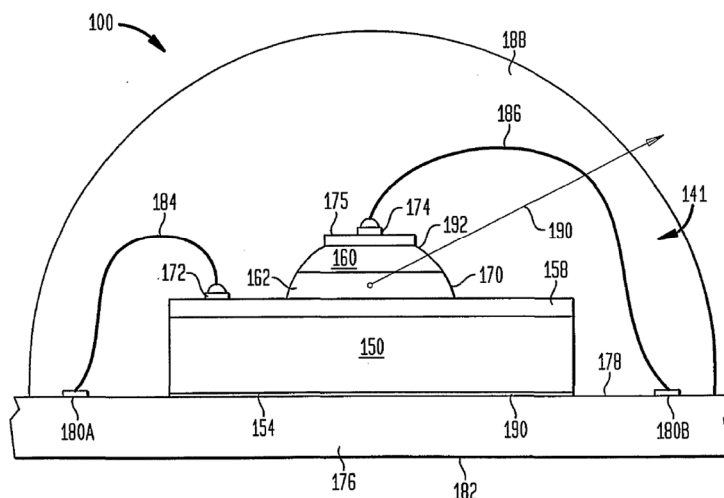
Eliashevich teaches that a tapered photoresist mask can be formed using a controlled processing of photoresist, but Eliashevich does not teach the specific details of that controlled process. Thus, there was a design need to understand how the controlled processing of photoresist would form a tapered photoresist. And a POSITA would have readily understood that Rabinzohn's preetching is one of such "controlled processes" that would provide a tapered photoresist mask. Accordingly, it would have been common sense for a POSITA to at least try Rabinzohn's method to form Eliashevich's tapered photoresist layer, and a POSITA would have had a reasonable expectation of success in doing so. EX1002, ¶84.

1. Claim 1

i. [1Pre] A method of manufacturing a light emitting device, comprising:

Eliashevich discloses preamble [1Pre]. Eliashevich discloses "*methods of making light emitting diodes and light-emitting diode packages* having optimized light extraction characteristics, and methods of making the foregoing." EX1003, 1:2-7. *See also* EX1003, Figures 3A-3I.

FIG. 3I

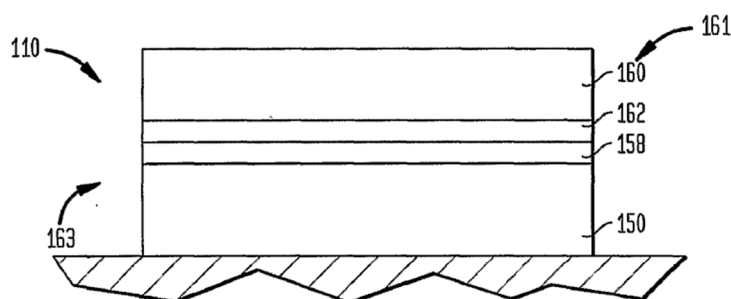


EX1003, Figure 3I. EX1002, ¶¶85-86.

- ii. [1A] sequentially forming an N-type semiconductor layer, active layer, and P-type semiconductor layer on a substrate;

Eliashevich discloses [1A]. Eliashevich's LED manufacturing process first provides a "substrate 150." EX1003, 14:14-15, Figure 3A. Then "one or more n-type layers 158 are deposited on the first surface 152 of substrate 150." EX1003, 14:25-26. Subsequently, "[o]ne or more p-type layers 160 having a top surface 166 are deposited over the n-type layers 158. A junction is also formed between the n-type layers 158 and p-type layers 160." EX1003, 14:29-32.

FIG. 3B



EX1003, Figure 3B. EX1002, ¶87.

“The junction is shown schematically in FIG. 3B as a *discrete layer* interposed between the layers 158 and 160. In practice, the *junction* may comprise ... *one* or more *intermediate layers*.” EX1003, 15:2-6. See also EX1003, 15:7-13. Accordingly, a POSITA would have understood that the *n-type layer* 158, the *junction layer* 162, and the *p-type layer* 160 are deposited sequentially in that order on a substrate 150, as shown in Figure 3B. EX1002, ¶88.

The *n-type layer* and *p-type layer* in Eliashevich are the claimed “*N-type semiconductor layer*” and “*P-type semiconductor layer*,” respectively, because both the *n-type layer* and *p-type layer* comprise semiconductor materials in a “semiconductor structure.” EX1003, 14:21-30 (“*A semiconductor structure 110* comprising a stacked structure of semiconductor layers is formed on the substrate 150. A *semiconductor material having a first conductivity type* is deposited on the first surface 152 of the substrate 150. For example, *one or more n-type layers* 158

are deposited on the first surface 152 of substrate 150. *A semiconductor material having a second conductivity type* is deposited over the semiconductor material of the first conductivity type.”). EX1002, ¶89.

In addition, the **junction layer** in Eliashevich is the claimed “**active layer**” because: (1) the **junction layer** is sandwiched between an **n-type layer** and a **p-type layer**, just like the **active layer** of the ’626 Patent (EX1003, 4:3-5, 14:29-32, Figure 3B; EX1001, 6:39-43, 8:32-39, Figures 3, 6); (2) the **junction layer** generates light, just like the **active layer** of the ’626 Patent (EX1003, 5:26-27, 23:18-21; EX1001, 6:24-27); and (3) the **junction layer** may be a quantum well, just like the **active layer** of the ’626 Patent (EX1003, 5:10-13; EX1001, 6:22-24). EX1002, ¶90.

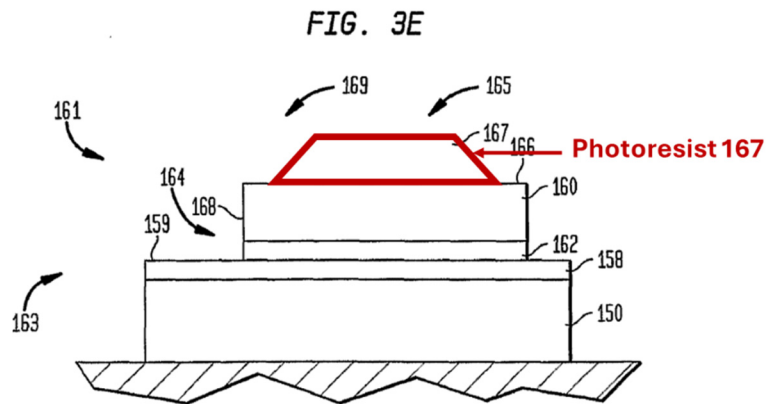
- iii. [1B] forming an **etching mask pattern**, of which a side surface is not perpendicular to but inclined at a slope from a horizontal plane, on the **P-type semiconductor layer**; and
[1D-1] wherein forming the **etching mask pattern** comprises: forming a **photoresist** on the **P-type semiconductor layer**;
[1D-2] exposing the **photoresist** to light; and
[1D-3] developing the light-exposed photoresist without a baking process after the light exposure.

Eliashevich-Rabinzohn teaches [1B], [1D-1] through [1D-3]. EX1002, ¶91.

a. [1B] “forming an **etching mask pattern**”

Eliashevich-Rabinzohn renders obvious “forming an **etching mask pattern**.” For example, Eliashevich discloses forming a **patterned photoresist 167** with a

“tapered shape,” as shown in Figure 3E. EX1003, 18:14-16, 18:26-31. The **patterned photoresist 167** is an “**etching mask pattern**” because it is subsequently used to mask the p-type semiconductor layer from dry-etching. EX1003, 18:14-24, 18:31-35, Figures 3D, 3F. *See also* Section X.A.1.iv [Ground I, 1C].

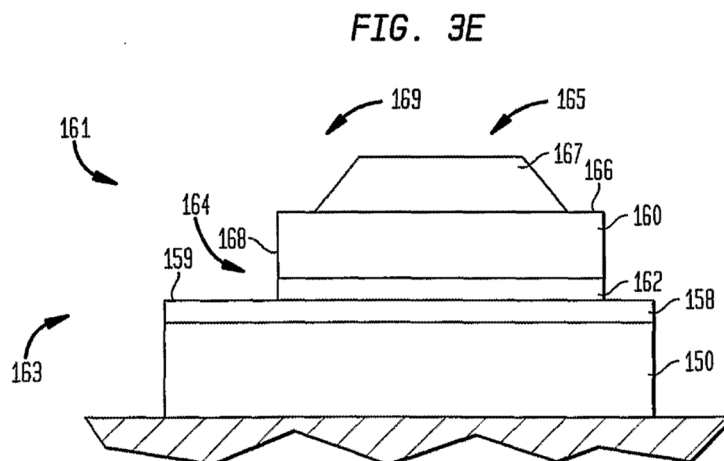


EX1003, Figure 3E. EX1002, ¶¶92-93.

Eliashevich in combination with Rabinzohn further renders obvious all details recited in [1D-1] through [1D-3], as explained below. EX1002, ¶94.

(a) [1D-1] “forming a photoresist on the P-type semiconductor layer”

Eliashevich discloses depositing “[a] photoresist material 167 ... on the top surface 166 of mesa 164.” EX1003, 18:19-20. As explained in Section X.A.1.ii [Ground I, 1A], the top layer of mesa 164 is a “p-type layer 160.” EX1003, 14:29-32, Figure 3B. Indeed, Figure 3E shows that the photoresist material 167 is on the p-type layer 160. Thus, Eliashevich teaches depositing (claimed “forming”) a photoresist material 167 (claimed “photoresist”) on the p-type layer 160.



EX1003, Figure 3E. EX1002, ¶95.

(b) [1D-2] “exposing the photoresist to light;”

Eliashevich teaches that “[a] *photoresist material 167* is deposited on the top surface 166 of mesa 164 and is *exposed* and developed to form a mask 165 having openings 169.” EX1003, 18:19-21. A POSITA would have understood Eliashevich to teach that the *photoresist material 167* is exposed to light because it was well known that a *photoresist material*—where the prefix “photo” means “light” (EX1017, 3)—is selectively patterned by exposing it to *light*. See Section VI.B [Photolithography]; EX1014, 1-4, 7-9. EX1002, ¶¶96-97.

(c) [1D-3] “developing the light-exposed photoresist without a baking process after the light exposure.”

First, Eliashevich discloses “*developing the light-exposed photoresist.*” As explained in Section X.A.1.iii.a(b) [Ground I, 1D-2], Eliashevich’s photoresist is “light-exposed.” Eliashevich also teaches that “[a] *photoresist material 167* ... is

exposed and developed to form a mask 165 having openings 169.” EX1003, 18:19-21. EX1002, ¶98.

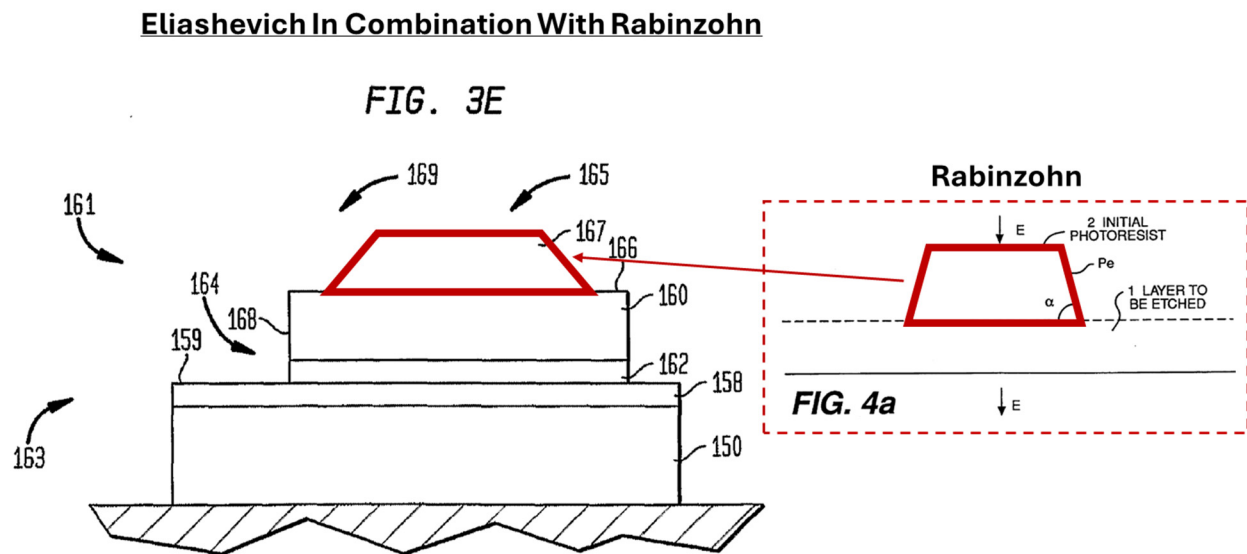
Second, Eliashevich in combination with Rabinzohn renders obvious that the light-exposed photoresist is developed “without a baking process after the light exposure.” Neither Eliashevich nor Rabinzohn teaches baking the photoresist after the light exposure. For example, Eliashevich teaches developing the light-exposed photoresist without any mention of baking after the light exposure: it simply states that “[a] photoresist material 167 ... is *exposed and developed*.” EX1003, 18:19-21. *See also* EX1003, 18:14-19:16. Similarly, Rabinzohn teaches developing the exposed photoresist without any mention of baking after the light exposure. *See generally* EX1004, 7:21-37. Indeed, the Eliashevich-Rabinzohn combination does not rely on baking to form the inclined photoresist layer; rather, the combination relies on Eliashevich’s “controlled processing” that is implemented as Rabinzohn’s “preetching” process. *See* Section X.A.3 [Eliashevich-Rabinzohn]. EX1002, ¶¶99-100.

(d) “forming an etching mask pattern, of which a side surface is not perpendicular to but inclined at a slope from a horizontal plane, on the P-type semiconductor layer”

Eliashevich-Rabinzohn renders obvious forming the patterned photoresist 167 (the claimed “etching mask pattern”) on a p-type layer 160 as shown in Figure 3E.

EX1003, 18:26-31, Figure 3E. *See also* Section X.A.1.ii [Ground I, 1A]; EX1003, 14:21-30. EX1002, ¶101.

Eliashevich-Rabinzohn also renders obvious that the side surface of the **patterned photoresist 167** is not perpendicular to but inclined at a slope from a horizontal plane, as shown by the sloped side surface of the **patterned photoresist 167** shown in Eliashevich's Figure 3E and taught by the preetching process and Figure 4a in Rabinzohn. EX1003, 18:26-31, Figure 3E; EX1004, 7:21-37, Figure 4a.



EX1003, Figure 3E; EX1004, Figure 4a. EX1002, ¶102.

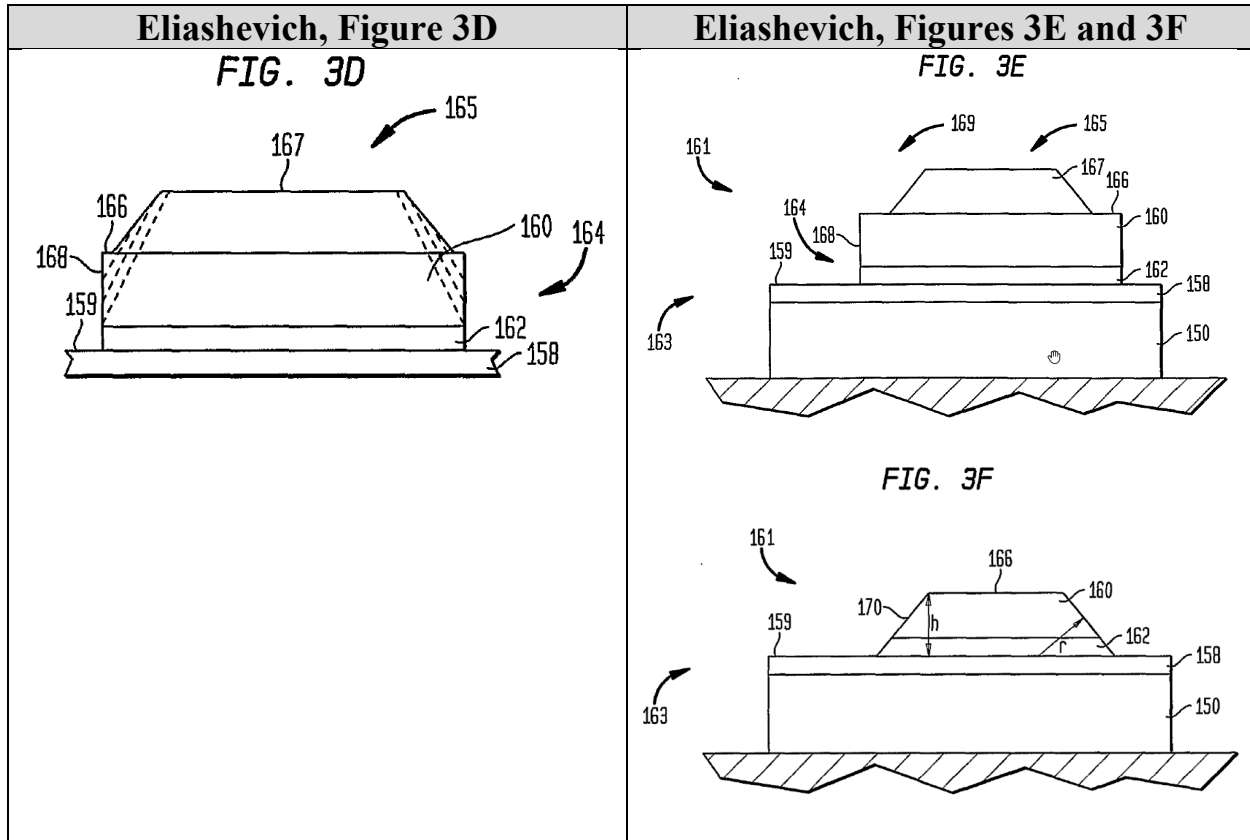
- iv. [1C] removing the **etching mask pattern** and the **P-type semiconductor layer** exposed through the **etching mask pattern**;

Eliashevich discloses [9C]. EX1002, ¶103.

First, Eliashevich teaches “removing the **etching mask pattern**.” Eliashevich teaches that “[o]ne preferred etching process includes a reactive ion etching (RIE) process” and “[t]he *RIE etching removes the mask*” formed by the **patterned photoresist 167**. EX1003, 18:16-17, 18:31-34 (“The RIE etching removes the mask at an outside portion of the mesa first and then begins to remove semiconductor material from the p-type layers 160, as represented by the dashed lines in FIG. 3D.”), Figures 3E and 3F (showing absence of photoresist 167). EX1002, ¶104.

Second, Eliashevich also teaches “removing ... the **P-type semiconductor layer** exposed through the **etching mask pattern**.” Eliashevich teaches that “mesa 164 is subjected to an *etching process* which *removes* some of the semiconductor material from the **p-type layers 160**.” EX1003, 18:14-31. Specifically, “[t]he *RIE etching* removes the mask at an outside portion of the mesa first and *then begins to remove semiconductor material from the p-type layers 160*, as represented by the dashed lines in FIG. 3D.” EX1003, 18:31-34. The **p-type layer 160** removed by the etching process is the portion “exposed through the **etching mask pattern**.” Eliashevich explains that the **photoresist material 167** is developed to “form a mask 165 having *openings 169*,” as shown in Figure 3E. And the etching process “removes the mask at an outside portion of the mesa first and then begins to *remove semiconductor material from the p-type layers 160, as represented by the dashed lines in FIG. 3D*,” which is the material exposed through the etching mask pattern.

EX1003, 18:31-34. The RIE etching process thus removes the portion of “p-type layer 160” that is exposed through the photoresist mask 167. See also EX1003, 19:8-10.



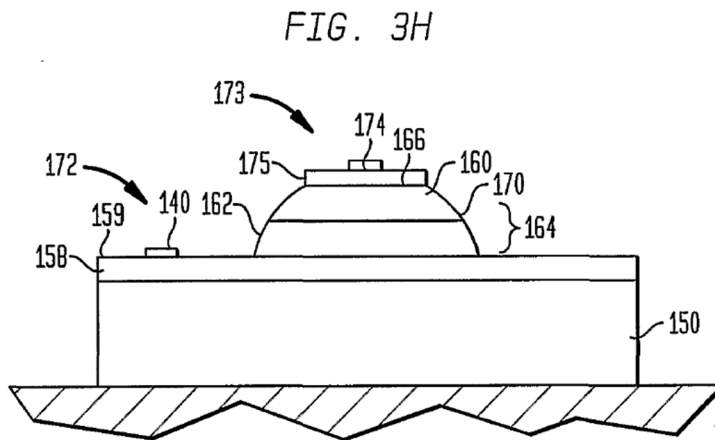
EX1002, ¶105.

2. Claim 3

- i. [3] The method as claimed in claim 1, further comprising the step of flip-chip bonding the substrate onto an additional submount substrate after the step of removing the P-type semiconductor layer and the etching mask pattern.

Eliashevich-Rabinzohn renders obvious [3]. Eliashevich teaches that the LED chip manufactured using the process described in Figures 3A-3H can be flipped and mounted on another substrate to form an LED device. EX1002, ¶106.

For example, after etching the mesa to form a non-vertical surface 170 shown in Figure 3F, Eliashevich deposits electrodes 172 and 173 to make the LED chip shown in Figure 3H. EX1003, 19:26-33.

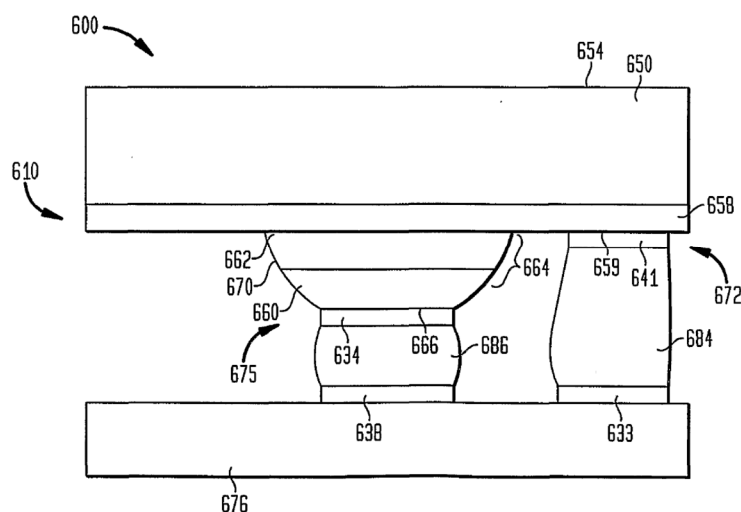


EX1003, Figure 3H. EX1002, ¶107.

Eliashevich teaches that the LED of Figure 3H is then flipped and bonded on another substrate, as shown in Figure 8 (below). EX1003, 28:12-30. Eliashevich shows in Figure 8 “a semiconductor structure [610] comprising a stacked structure

of p-type, n-type and other semiconductor materials for generating light” (EX1003, 28:16-19) and “a sapphire substrate 650” (EX1003, 28:15-16). The “[s]tructure 610 [including the sapphire substrate 650] is ***bonded*** to the contacts of ***second substrate 676*** by, for example, disposing masses 686 and 684 of bonding material between each of the pads and contacts” identified by 633, 634, 638, and 641 in Figure 8. EX1003, 28:26-29:1, Figure 8. *See also* EX1003, 34:10-12. As shown in Figure 8, bonding the structure 610 to the underlying substrate 676 would have required flipping the structure 610 before bonding. A POSITA would have understood that one example of the semiconductor structure 610 is the LED of Figure 3H because the components in the semiconductor structure 610 are substantially the same as the components in the LED in Figure 3H. *See also* EX1003, 33:35-34:7 (claiming a device package that includes an “optoelectronic device of claim 1” directed to Figure 3H and “a second substrate” shown in Figure 8).

FIG. 8



EX1003, Figure 8. EX1002, ¶¶108-112.

Accordingly, at the time the semiconductor structure 610 is flipped and bonded to the second substrate 676, “the step of removing the P-type semiconductor layer and the etching mask pattern” pursuant to Figures 3D-3F would already have been performed. *See* Section X.A.1.iv [Ground I, 1C]. EX1002, ¶113.

Thus, Eliashevich-Rabinzohn teaches “the step of flip-chip bonding the substrate [sapphire substrate 650 of structure 610, corresponding to substrate 150 in Figure 3H] onto an additional submount substrate [second substrate 676] after the step of removing the P-type semiconductor layer and the etching mask pattern” as described in Figures 3D-3F. EX1002, ¶114.

B. Ground II: Eliashevich In Combination With Rabinzohn And Yoo Renders Obvious Claim 7.

1. Claim 7

- i. [7] The method as claimed in claim 1, wherein the **photoresist** with a thickness of 3 to 50 μm is used in the forming the **etching mask pattern**.

Eliashevich in combination with Rabinzohn and Yoo (“Eliashevich-Rabinzohn-Yoo”) renders obvious [7]. EX1002, ¶115.

Eliashevich teaches forming the **patterned photoresist layer** (the claimed **etching mask pattern**) by depositing “[a] **photoresist material 167** ... on the top surface 166 of mesa 164.” EX1003, 18:19-21. Although Eliashevich does not specify the thickness for the **photoresist material 167**, Eliashevich suggests that the

deposited photoresist is preferably thick, because (1) Eliashevich teaches that the photoresist material 167 is used to protect the top surface 166 of the mesa 164 during etching and (2) “[p]referably, a portion of the top surface [of the mesa] *remains* after etching, to be used for an upper electrode-pad unit.” EX1003, 18:21-26. A POSITA would have understood that the photoresist layer is preferably thick because otherwise, the etching step would have completely removed the photoresist layer and, hence, the top surface 166 of the mesa 164. EX1002, ¶116.

Using a thick photoresist layer in LED manufacturing was common. For example, Yoo discloses using a 10-micron thick photoresist in LED manufacturing. EX1005, [0036]. More specifically, Yoo is directed to a method of manufacturing LEDs by selectively etching LEDs’ layers using dry-etching—specifically reactive ion etching (RIE). EX1005, Abstract, [0032], [0035]. To protect the LED structure against RIE’s intense plasma, Yoo teaches using a thick photoresist that is “beneficially ... 10 microns” thick. EX1005, [0036] (“In the illustrated example, the photo-resist is beneficially spin coated to a thickness of about *10 microns*.”), [0035]. EX1002, ¶117.

A POSITA would have found it obvious to combine Eliashevich-Rabinzohn with Yoo to make Eliashevich’s photoresist 167 to be *10 microns thick* as taught by Yoo. **First**, as described above, Eliashevich itself motivates using a thick photoresist, like the 10-micron thick photoresist taught by Yoo. *See* EX1003, 18:24-

26. Indeed, using a **thick photoresist** (such as a **10-micron thick photoresist**) for LED manufacturing was common, and using such **thick photoresist** specifically to form a **photoresist layer** with a sloped side surface—as in Eliashevich-Rabinzohn—was also common. *See* EX1007, Title (“Semiconductor ***Light Emitting Device*** And Manufacturing Method Thereof”); [0085] (“As to the **resist layer 130** having a thickness of ***approximately 10μm, it is possible to form the inclined resist layer 130 without problem.***”). EX1002, ¶118.

Second, a POSITA would have understood that Yoo’s teachings are readily applicable to the Eliashevich-Rabinzohn combination because Eliashevich-Rabinzohn and Yoo are both directed to semiconductor manufacturing, and the dimensions of the structures in Eliashevich-Rabinzohn are commensurate with the dimensions of the structures in Yoo. EX1003, 18:4-5 (“Typically, the entire stack including mesa 164 is on the order of five microns thick.”); EX1005, [0033] (“The vertical topology GaN-based LED layer structure 120 is beneficially less than 5 microns thick.”). EX1002, ¶119.

Third, Eliashevich-Rabinzohn and Yoo both use a RIE technique (EX1003, 18:16-19; EX1005, [0035]), and Yoo teaches that a manufacturing process based on RIE would benefit from a **thick photoresist**—such as a **10-micron thick photoresist**—to protect the underlying structure from intense plasma (EX1005, [0035]). EX1002, ¶120.

Fourth, a POSITA would have understood that the combination merely amounts to applying a known technique (*i.e.*, using a 10-micron thick photoresist layer per Yoo) to a known method (*i.e.*, a semiconductor manufacturing method per Eliashevich-Rabinzohn) ready for improvement (preventing inadvertent etching of underlying structures) to yield predictable results of manufacturing an LED according to the design specifications. EX1002, ¶121.

And finally, a POSITA would have understood that the combination amounts to a simple substitution of one known element (a photoresist layer in Eliashevich-Rabinzohn) for another (a 10-micron thick photoresist layer per Yoo) to obtain predictable results of preventing inadvertent etching of underlying structures according to the design specifications. EX1002, ¶122.

A POSITA would have had a reasonable expectation of success in using Yoo's 10-micron thick photoresist in Eliashevich-Rabinzohn's manufacturing process. For example, Yoo specifically discloses that a 10-micron thick photoresist was successfully used in LED manufacturing. EX1005, [0036]. Indeed, it was common to use such a thick photoresist in semiconductor manufacturing, specifically to form a photoresist layer with an inclined side surface. *See* EX1007, Title ("Semiconductor ***Light Emitting Device*** And Manufacturing Method Thereof"); [0085] ("As to the resist layer 130 having a thickness of ***approximately 10um***, ***it is possible to form the inclined resist layer 130 without problem.***"). Thus, a POSITA

would have had a reasonable expectation that a 10-micron thick photoresist would also work well in Eliashevich-Rabinzohn's manufacturing process, as suggested by Eliashevich. *See* EX1003, 18:24-26. EX1002, ¶123.

In addition, a POSITA would have had a reasonable expectation of success in forming and using a 10-micron thick photoresist layer in semiconductor manufacturing processes like Eliashevich-Rabinzohn's manufacturing process. It was well known that the thickness of a photoresist layer is easily controlled by controlling the parameter associated with the photoresist application technique. *See* EX1011, 17 (When the photoresist is applied to a wafer using a spin coater, "[t]he PR [photoresist] thickness is related to both PR viscosity and the wafer spin rate, ... The higher the spin rate, the thinner the PR layer, ..."). And indeed, Yoo itself is shows that a 10-micron thick photoresist layer is compatible with, and readily used in, LED manufacturing. EX1005, [0036]. *See also* EX1007, [0082], [0086]. EX1002, ¶¶124-125.

Furthermore, selecting the thickness of the photoresist would have merely amounted to a routine optimization of a design parameter—the thickness—and such routine optimization was well within the ordinary skill. EX1002, ¶126.

At a minimum, it would have been obvious to try to use Yoo's 10-micron thick photoresist layer in the manufacturing process of Eliashevich-Rabinzohn. As taught in Yoo, forming a 10-micron thick photoresist layer was feasible, and it was

desirable to use a thick-enough photoresist to provide sufficient protection of the underlying semiconductor layers, as suggested by Eliashevich. *See* EX1003, 18:24-26. So, it would have been common sense to try a 10-micron thick photoresist layer, as taught by Yoo, in Eliashevich-Rabinzohn. EX1002, ¶127.

C. Ground III: Eliashevich In Combination With Rabinzohn and Huang Renders Obvious Claims 9 and 15.

1. Huang (EX1006)

Huang is directed to a “method of improving a photoresist profile for a semiconductor manufacturing.” EX1006, 3:54-55, 1:12-16. Huang explains in conjunction with Figure 3, the steps of photoresist coating (Step 301), soft bake (Step 302), exposure (Step 303), post-exposure bake (PEB) at “about 100-120°C” (Step 304), development (Step 305) and a hard bake (Steps 306 at “about 135-145 °C” or 307a at “about 110 °C”). *See* EX1006, 2:53-3:32.

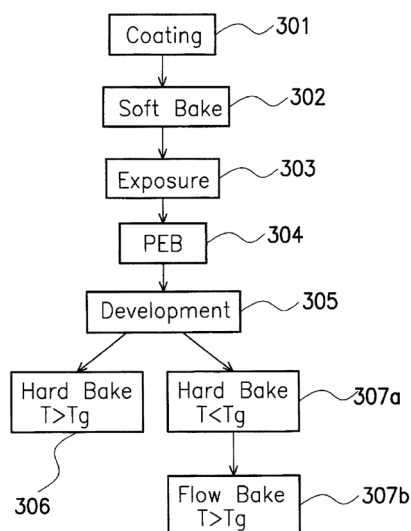


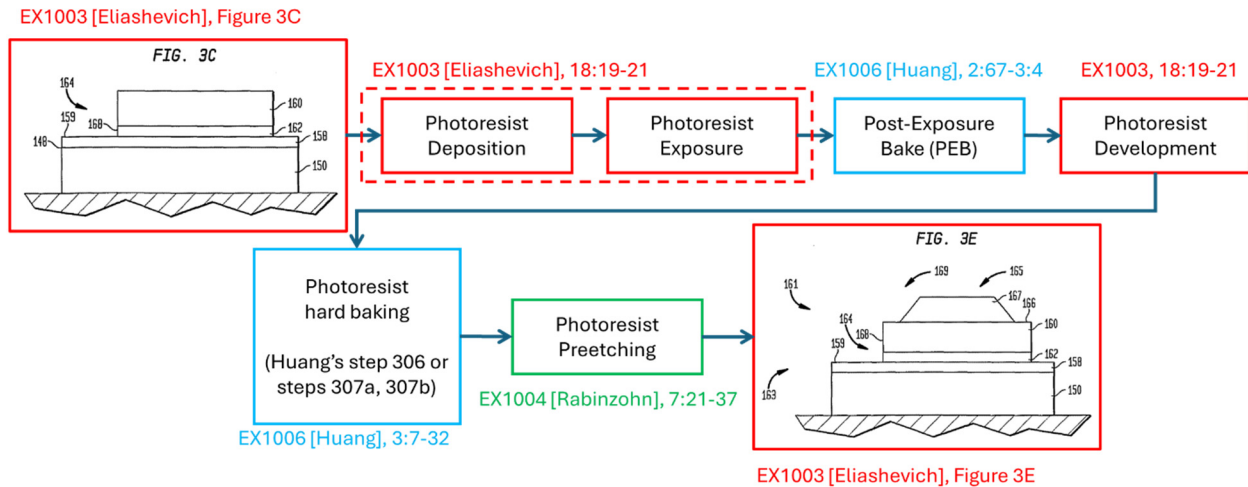
FIG. 3

EX1006, Figure 3. EX1002, ¶128.

**2. Eliashevich In Combination With Rabinzohn And Huang
 (“Eliashevich-Rabinzohn-Huang”)**

A POSITA would have found it obvious to combine Eliashevich-Rabinzohn—described in Section X.A.3 [Eliashevich-Rabinzohn]—with Huang’s photoresist baking steps to improve the photoresist processing in Eliashevich-Rabinzohn. As shown in Figure 3 of Huang, Huang teaches that the photoresist is conventionally subject to PEB before photoresist development, and the photoresist is also subject to a hard bake after development. Accordingly, consistent with Huang’s Figure 3, a POSITA would have found it obvious to modify the manufacturing process in Eliashevich-Rabinzohn to add: (1) a PEB step of baking the exposed photoresist at “about 100-120°C” between the exposure and development steps; and (2) a hard baking step (e.g., step 306 at “about 135-145 °C” or step 307a at “about 110 °C”) after developing the photoresist as illustrated below.

Eliashevich In Combination With Rabinzohn And Huang



EX1002, ¶¶129-130.

i. Reasons To Combine Eliashevich-Rabinzohn with Huang

A POSITA would have been motivated to combine Eliashevich-Rabinzohn with Huang as described above. Huang expressly states that the PEB and hard bake steps are part of a “conventional method to patterning photoresist layer.” EX1006, 1:22-27. Indeed, even an elementary textbook called “Introduction to Semiconductor Manufacturing Technology” published 5 years before the earliest priority date of the ’626 Patent discloses the PEB and hard bake steps. *See* EX1011, 31-32, 35-36. Thus, it would have been common sense to use such conventional method to augment the manufacturing processes of Eliashevich-Rabinzohn. EX1002, ¶131.

Indeed, a POSITA would have been motivated to augment the manufacturing processes of Eliashevich-Rabinzohn with the PEB and hard bake steps of Huang because of known benefits of PEB and hard bake steps in semiconductor manufacturing. For example, it was well known that PEB steps generally help with smoothing the side surface of the developed photoresist layer. “When the exposure light reflects from the photoresist-substrate interface, it can interfere with incoming exposure light and cause the standing wave effect due to the constructive and destructive interference at the different depth.” EX1011, 31. “The standing wave effect causes striations ... through the photoresist” (EX1011, 31), which is known to cause imprecision in the subsequent etching processes. It was common knowledge that the standing wave effect would be reduced when the photoresist is subject to a “*post-exposure bake (PEB)* between the exposure and develop processes.” EX1011, 31-32. *See also* EX1016, 1. EX1002, ¶¶132-133.

Similarly, it was well known that hard bake steps generally help with subsequent photoresist processing. For example, Huang itself explains that a hard bake step is useful for “evaporat[ing] the remaining solvent contained in the photoresist layer”; improving “the adhesion of the photoresist layer” to the underlying structure; and “solidify[ing] the photoresist and [] form[ing] the profile of the photoresist layer.” EX1006, 1:28-35, 1:42-43. *See also* EX1011, 35 (“After development, the wafer is put through a *hard bake* process. Hard bake drives out

the remaining solvents in the photoresist, strengthens the PR [photoresist], and improves the PR etch and implantation resistance via further polymerization, and also improves its adhesion to the wafer due to further thermal dehydration.”). EX1002, ¶¶134-135.

A POSITA would have had a reasonable expectation of success in adding the PEB and hard bake steps to the process flow of Eliashevich-Rabinzohn because they are part of a “*conventional* method to patterning [a] photoresist layer” (EX1006, 1:22-27) and Huang specifically teaches that the PEB and hard bake steps can be conventionally used in the specific order presented in the combination. *See* EX1006, Figure 3. Indeed, PEB and hard bake steps were well known in the art (*see* EX1011, 31-32, 35-36), and they merely involve heating up the wafer, for example, by placing it on a “hot plate.” EX1006, 1:38-39. EX1002, ¶136.

Accordingly, the combination would have merely involved using known techniques (PEB and hard bake steps per Huang) to improve a similar manufacturing technique (the process of Eliashevich-Rabinzohn) in the same way (performing the PEB step before the photoresist development and the hard bake step after the photoresist development, per Huang) to achieve the expected result of reducing the standing wave effect (due to PEB) (EX1011, 31-32), “evaporat[ing] the remaining solvent contained in the photoresist layer,” “improving “the adhesion of the photoresist layer” to the underlying structure, “solidify[ing] the photoresist and []

form[ing] the profile of the photoresist layer,” and improving the surface profile of the photoresist layer (due to hard bake). EX1006, 1:28-35, 1:42-43, 3:7-12; 3:30-32; EX1015, 11; EX1011, 35. EX1002, ¶137.

Similarly, the combination would have merely involved applying known techniques (PEB and hard bake steps per Huang) to a known method (the LED manufacturing process per Eliashevich-Rabinzohn) ready for improvement to yield predictable results of reducing the standing wave effect, evaporating remaining solvent contained in the photoresist layer, and improving adhesion of the photoresist layer to the underlying structure, as explained above. EX1002, ¶138.

At a minimum, it would have been common sense and obvious to try the PEB and hard bake steps taught by Huang because they are known to be “conventional” in semiconductor manufacturing processes—like the LED manufacturing process in Eliashevich-Rabinzohn—and they provide specific benefits to Eliashevich-Rabinzohn’s manufacturing process with a reasonable expectation of success, as explained above. EX1002, ¶139.

3. Claim 9

- i. [9Pre] A method of manufacturing a light emitting device, comprising:
[9A] sequentially forming an N-type semiconductor layer, active layer, and P-type semiconductor layer on a substrate;
[9B] forming an etching mask pattern, of which a side surface is not perpendicular to but inclined at a slope from a horizontal plane, on the P-type semiconductor layer; and
[9C] removing the etching mask pattern and the P-type semiconductor layer exposed through the etching mask pattern;
[9D-1] wherein forming the etching mask pattern comprises: forming a photoresist on the P-type semiconductor layer;
[9D-2] exposing the photoresist to light;

[9Pre]-[9D-2] are identical to [1Pre]-[1D-2]. See Listing of Challenged Claims. Eliashevich-Rabinzohn renders obvious [9Pre]-[9D-2] for the reasons provided above for [1Pre]-[1D-2]. EX1002, ¶140.

- ii. [9D-3] hard-baking and developing the photoresist; and

Eliashevich-Rabinzohn-Huang renders obvious [9D-3]. EX1002, ¶141.

First, Huang teaches “hard-baking ... the photoresist.” As an initial matter, [9D-3] does not restrict the order of the claimed “hard-baking” step and “develop[ment]” step. *Koninklijke Philips N.V. v. Quectel Wireless Sols. Co.*, No. 2023-1221, 2024 WL 3042238, at *4 (Fed. Cir. June 18, 2024) (“We have held that ‘as a general rule, unless the steps of a method claim actually recite an order, the steps are not ordinarily construed to require one,’ ...”) (quoting *Mformation Techs.*,

Inc. v. Rsch. in Motion Ltd., 764 F.3d 1392, 1398 (Fed. Cir. 2014)). Accordingly, for the reasons provided below, the claimed “hard-baking” limitation is met by the hard bake step 306 or the hard bake step 307a in Huang. EX1002, ¶142.

As shown in the Eliashevich-Rabinzohn-Huang combination, Huang teaches that “a step of hard bake is performed.” EX1006, 3:4-7. “When a single flow step 306 is used,” “the temperature for performing hard bake step ... is about 135-145° C.” EX1006, 3:7-20. “When a multiple flow step [307] is used, ... the hard bake 307a is performed at about 110° C.” EX1006, 3:21-30. The “hard bake 306” step or the “hard bake 307a” independently satisfies the claimed “hard-baking” because both the “hard bake 306” step and the “hard bake 307a” step “hard-bak[es] ... the photoresist.” EX1002, ¶143.

At a minimum, the hard bake step 306 performed at “about 135-145° C” (EX1006, 3:7-20) renders obvious the claimed hard-baking because it overlaps the temperature range of hard baking required by claim 15: “performed at a temperature of 100 to 140°C.” EX1001, claim 15. See *UCB, Inc. v. Actavis Lab’s UT, Nc.*, 65 F.4th 679, 689 (Fed. Cir. 2023) (“A presumption of obviousness applies where a claimed range overlaps with a range disclosed in the prior art.”) (quotation marks omitted). Nothing in the record suggests that the “prior art teaches away from the [required] range [of 100 to 140°C], ... the [required] range produces new and unexpected results,” or the required temperature range is non-obviousness. *Id.*

Also, the **hard bake 307a** step performed at “about **110° C.**” (EX1006, 3:21-30) discloses the claimed **hard-baking** because it falls within the temperature range of **hard baking** required by claim 15. EX1002, ¶¶144-145.

To the extent the claimed “hard baking” step must occur before the claimed “developing” step, the Eliashevich-Rabinzohn-Huang combination still teaches the claimed “hard baking” because it includes the **post-exposure bake (PEB) 304** step. For example, Huang teaches that “an exposure step 303 is performed on the **photoresist layer 20**, followed by performing the steps of **post-exposure bake (PEB) 304**” EX1006, 2:66-3:2, Figure 3. “The temperature for performing the **post-exposure bake 304** is about **100-120° C.**, ...” EX1006, 3:2-4. The PEB step 304 satisfies the claimed “**hard-baking**” limitation because, as claim 15 claims, the “**hard-baking** is performed at a temperature of 100 to 140°C” (EX1001, claim 15), and the temperature of Huang’s **PEB step 304** falls within that temperature range (EX1006, 3:2-4 (**PEB** occurring at “100-120°C”)).

Eliashevich In Combination With Rabinzohn And Huang

EX1003 [Eliashevich], Figure 3C

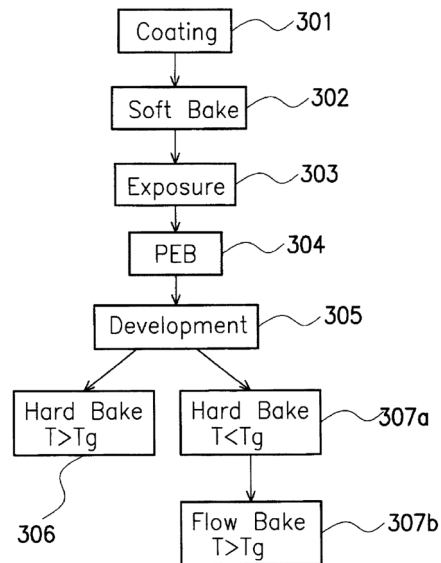
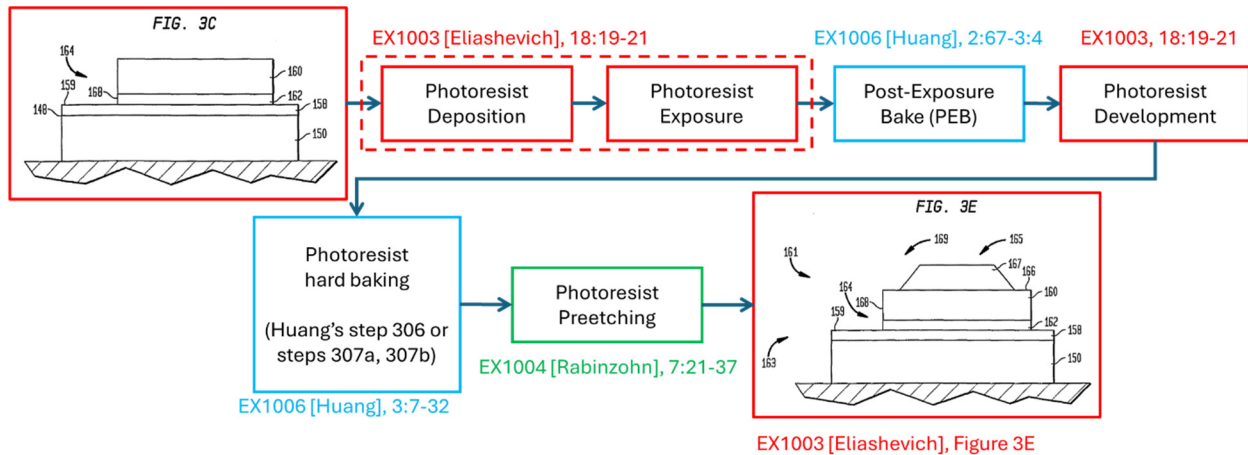
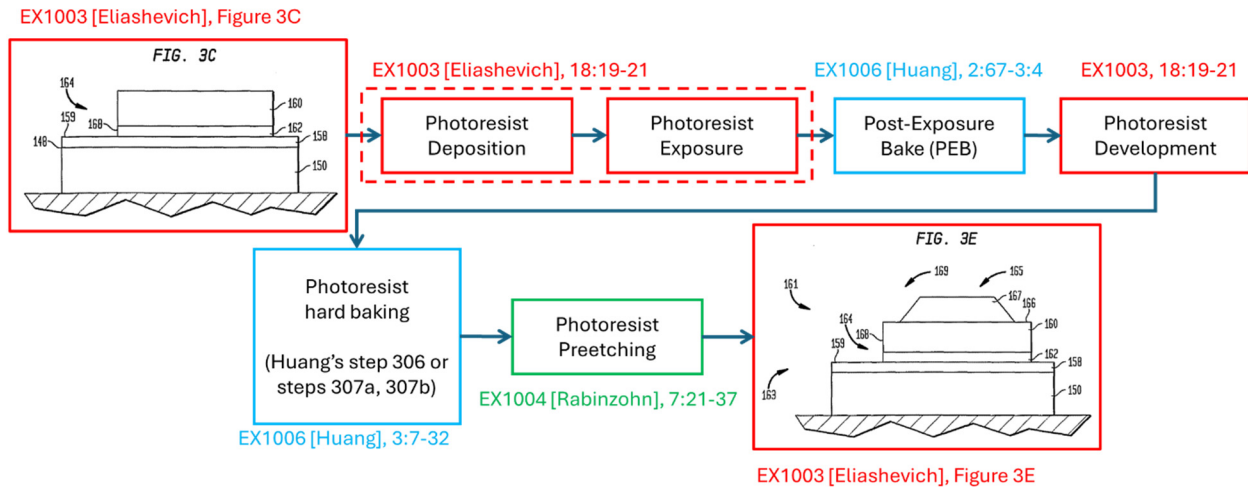


FIG. 3

EX1006, Figure 3. EX1002, ¶146.

Second, Eliashevich discloses “developing the photoresist.” Eliashevich teaches that to form the mask 165, “[a] photoresist material 167 is deposited on the top surface 166 of mesa 164 and is exposed and developed to form a mask 165 having openings 169.” EX1003, 18:19-21.

Eliashevich In Combination With Rabinzohn And Huang



EX1002, ¶147.

iii. [9D-4] **etching** a side surface of the developed **photoresist** to have the **slope from the horizontal plane**.

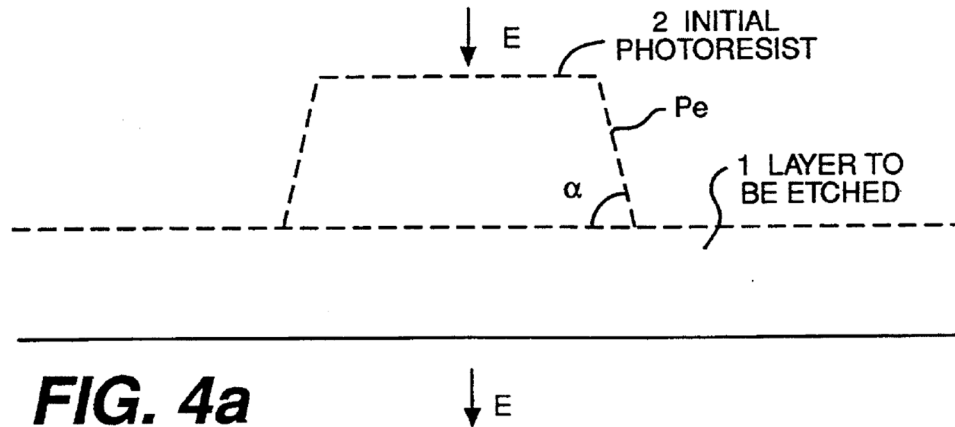
Eliashevich-Rabinzohn-Huang renders obvious [9D-4]. EX1002, ¶148.

As explained in Section X.A.2 [Rabinzohn] and Section X.A.3 [Eliashevich-Rabinzohn], Rabinzohn teaches performing “**preetching**” on the **photoresist layer 2** to provide sloped side surfaces, as shown in Figure 4a (below). For example, Rabinzohn states:

Alternatively, in the case of FIG. 4, the initial masking photoresist layer 2, previously to the actual etching process, has been subjected to a **preetching stage**, the effect of which is to generate **etching flanks of slope pe** inclined in relation to the free surface of the layer 1 to be etched, assumed to be horizontal, the **etching flanks of the initial masking photoresist layer 2 being**

thus inclined at an angle α in relation to the abovementioned
free surface.

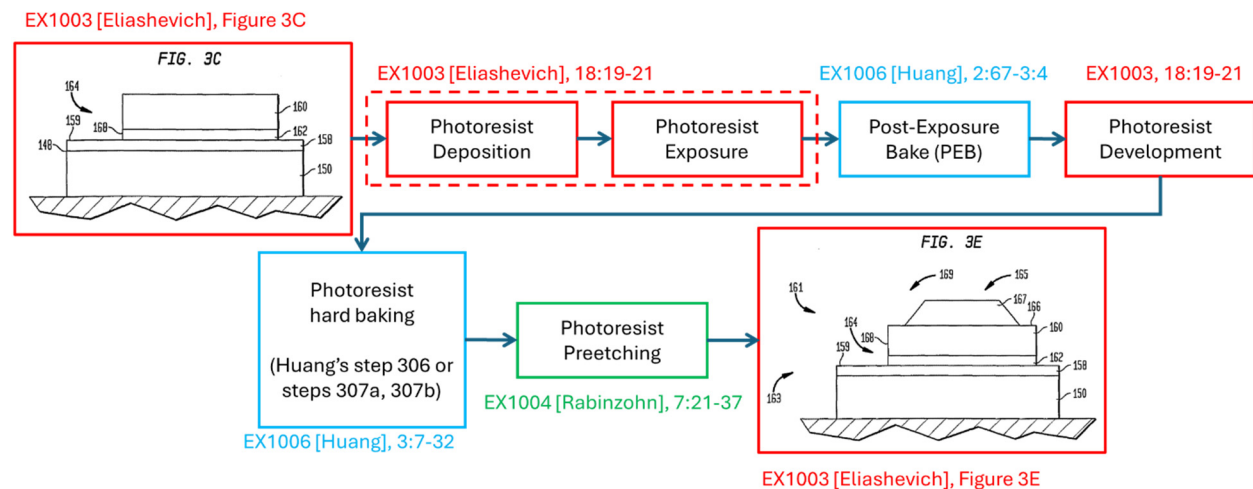
EX1004, 7:21-30.



EX1004, Figure 4a. EX1002, ¶149.

And in the Eliashevich-Rabinzohn-Huang combination, Rabinzohn's **preetching step** is applied to Eliashevich's **photoresist** that has already undergone the development step, as shown below.

Eliashevich In Combination With Rabinzohn And Huang



EX1002, ¶150.

Accordingly, Eliashevich-Rabinzohn-Huang renders obvious **preetching** (the claimed “**etching**”) the sidewalls (the claimed “side surface”) of the developed **photoresist layer 2** (the claimed “developed **photoresist**”) to have an angle α in relation to the horizontal plane, free surface of the layer 1 (the claimed “**slope from the horizontal plane**”). EX1002, ¶151.

4. Claim 15

- i. **[15] The method as claimed in claim 9, wherein the **hard-baking** is performed at a temperature of 100 to 140°C.**

Eliashevich-Rabinzohn-Huang teaches the additional limitation of Claim 15. For the reasons provided in Section X.C.3.ii [Ground III, limitation 9D-3], Eliashevich-Rabinzohn-Huang renders obvious that “the **hard-baking** is performed at a temperature of 100 to 140°C.” See EX1006, 3:2-4 (**PEB** occurring at “**100-120°C**”); 3:7-20 (**hard bake 306** occurring at “about **135-145° C**”); 3:21-30 (**hard bake 307a** occurring at “about **110° C**”). EX1002, ¶152.

D. Ground IV: Eliashevich In Combination With Rabinzohn, Huang, And Yoo Renders Obvious Claim 13.

1. Claim 13

- i. **[13] The method as claimed in claim 9, wherein the **photoresist** with a thickness of 3 to 50 μm is used in the forming the etching mask pattern.**

As explained in Section X.B.1.i [Ground II, Claim 7], a POSITA would have found it obvious to combine Eliashevich-Rabinzohn with Yoo to make Eliashevich’s

photoresist 167 to be **10 microns thick** as disclosed by Yoo. For substantially similar reasons, a POSITA would have found it obvious to combine Eliashevich-Rabinzohn-Huang—as articulated in Section X.C.2—with Yoo to make Eliashevich’s photoresist 167 to be **10 microns thick** as disclosed by Yoo. *See* Section X.B.1.i [Ground II, Claim 7]. EX1002, ¶153.

For example, a POSITA would have been motivated to combine Eliashevich-Rabinzohn-Huang with Yoo because Eliashevich itself motivates using a thick photoresist, like the 10-micron thick photoresist in Yoo, in forming the etching mask pattern. *See* EX1003, 18:24-26. Also, Eliashevich-Rabinzohn-Huang and Yoo are all directed to semiconductor manufacturing, and the dimensions of the structures in Eliashevich-Rabinzohn-Huang are commensurate with the dimensions of the structures in Yoo. EX1003, 18:4-5; EX1005, [0033]. Indeed, using a 10-micron thick photoresist for semiconductor manufacturing was common, and using such thick photoresist specifically to form a photoresist layer with an inclined surface was also common. *See* EX1007, Title, [0085]. EX1002, ¶154.

Also, Eliashevich-Rabinzohn-Huang and Yoo both use RIE (EX1003, 18:16-19; EX1005, [0035]), and Yoo teaches that a manufacturing process based on RIE would benefit from a thick photoresist to protect the underlying structure against intense plasma (EX1005, [0035]). EX1002, ¶155.

A POSITA would have understood that the combination merely amounts to applying a known technique (i.e., using a 10-micron thick photoresist layer per Yoo) to a known method (i.e., a semiconductor manufacturing method per Eliashevich-Rabinzohn-Huang) ready for improvement (preventing inadvertent etching of underlying structures) to yield predictable results of manufacturing semiconductor structures according to the desired design specifications. EX1002, ¶156.

Similarly, a POSITA would have understood that the combination amounts to a simple substitution of one known element (a photoresist layer in Eliashevich-Rabinzohn-Huang) for another (a 10-micron thick photoresist layer per Yoo) to obtain predictable results of preventing inadvertent etching of underlying structures during semiconductor manufacturing. EX1002, ¶157.

A POSITA would have had a reasonable expectation of success in using Yoo's 10-micron thick photoresist in Eliashevich-Rabinzohn-Huang's manufacturing process. For example, Yoo specifically discloses that a 10-micron thick photoresist was successfully used in semiconductor manufacturing. EX1005, [0036]. Indeed, it was common to use such a thick photoresist in semiconductor manufacturing, specifically to form a photoresist layer with an inclined side surface. See EX1007, Title; [0085] ("As to the resist layer 130 having a thickness of *approximately 10um*, *it is possible to form the inclined resist layer 130 without problem.*"). Thus, a POSITA would have had a reasonable expectation that a 10-micron thick photoresist

would also work well in Eliashevich-Rabinzohn-Huang's semiconductor manufacturing process, as suggested by Eliashevich. *See* EX1003, 18:24-26. EX1002, ¶158.

In addition, a POSITA would have had a reasonable expectation of success in forming and using a 10-micron thick photoresist layer in semiconductor manufacturing processes like Eliashevich-Rabinzohn-Huang's semiconductor manufacturing process. It was well known that the thickness of a photoresist layer is easily controlled by controlling the parameter associated with the photoresist application technique. *See* EX1011, 17. And indeed, Yoo itself is an example showing that a 10-micron thick photoresist layer is compatible with, and is readily used in, semiconductor manufacturing. EX1005, [0036]. *See also* EX1007, [0082], [0086]. EX1002, ¶159.

Furthermore, selecting the thickness of the photoresist would have merely amounted to a routine optimization of a design parameter—the thickness—and such routine optimization was well within the ordinary skill. EX1002, ¶160.

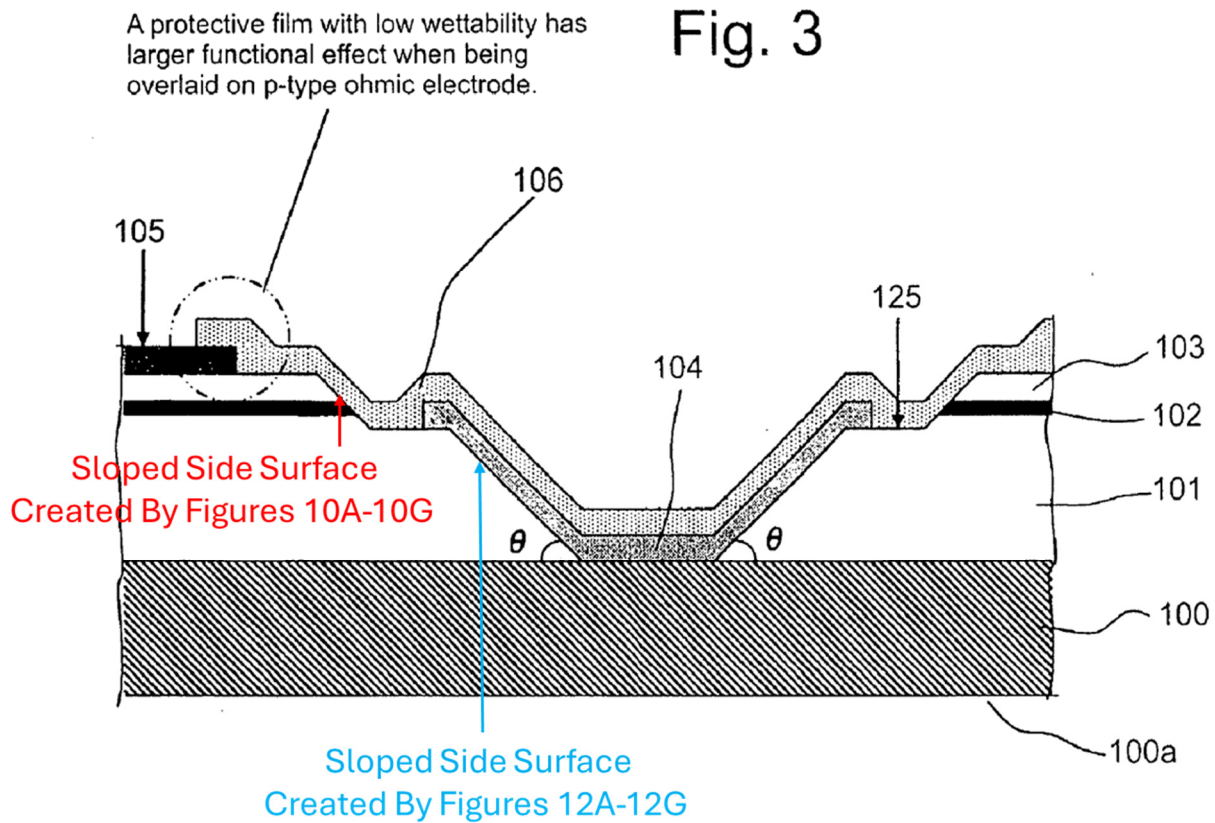
At a minimum, it would have been obvious to try to use Yoo's 10-micron thick photoresist layer in the manufacturing process of Eliashevich-Rabinzohn-Huang. As taught in Yoo, forming a 10-micron thick photoresist layer was feasible, and it was desirable to use a thick-enough photoresist to provide sufficient protection of the underlying semiconductor layers, as suggested by Eliashevich. So it would

have been common sense to try a 10-micron thick photoresist layer, as taught by Yoo, in Eliashevich-Rabinzohn. EX1002, ¶161.

E. Ground V: Horio Anticipates Claims 9, 13, And 15.

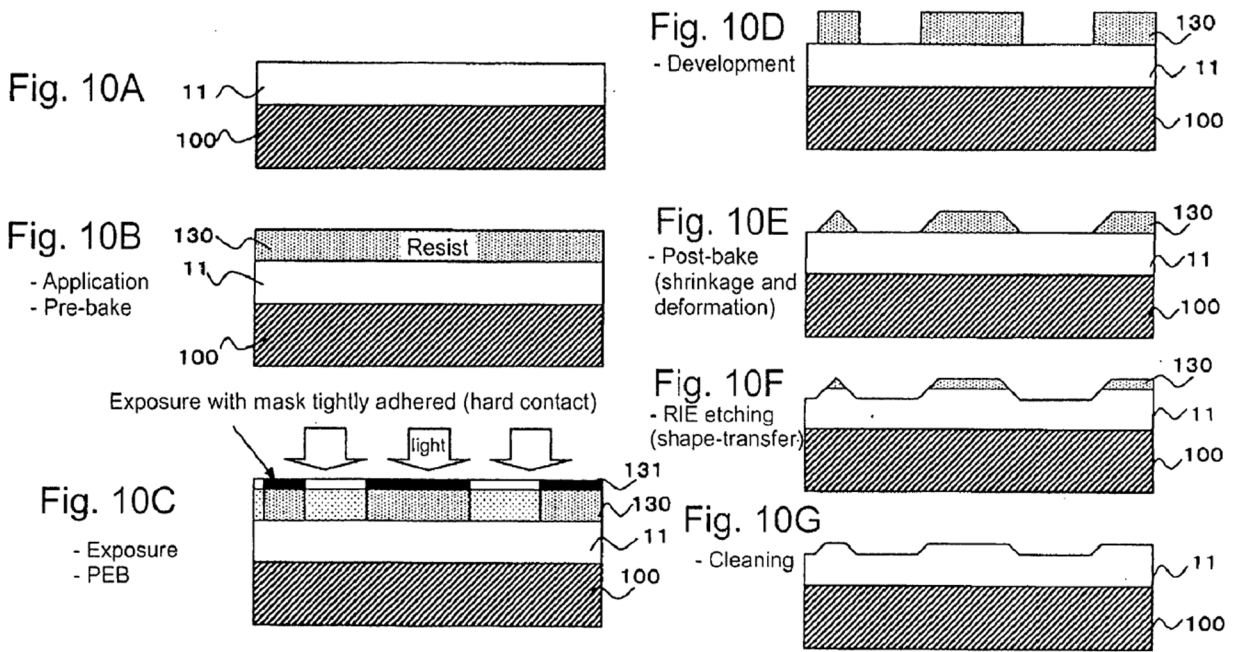
1. Horio (EX1007)

Horio is directed to a method of manufacturing an LED with a sloped side surface. Horio's LED includes a transparent substrate 100, a nitride layer that "includes at least an n-type nitride semiconductor layer 101, a luminescent layer 102, and a p-type nitride semiconductor layer 103," and electrodes 104, 105. EX1007, [0053]-[0054], Figures 2B, 3. Horio's manufacturing method includes two specific photolithography steps: one for forming a sloped side surface on the stack of the p-type layer 103, the luminescence layer 102, and a portion of the n-type layer 101 (e.g., Figures 10A-10G); and another for forming a sloped side surface on the remaining, bottom portion of the n-type layer 101 (e.g., Figure 12A-12G).



EX1007, Figure 3. EX1002, ¶¶162-163.

With respect to Figures 10A-10G, Horio teaches: (1) forming a photoresist layer with an inclined side surface on the p-type layer of the nitride layer 11 (EX1007, Figures 10B-10E); and (2) dry-etching the exposed nitride layer 11 to transfer the side surface profile of the photoresist layer onto the underlying LED layer (EX1007, Figure 10F). EX1007, [0078].



EX1007, Figures 10A-10G. EX1002, ¶164.

Specifically, in Figure 10A, Horio first provides on a substrate 100 a nitride semiconductor layer 11 that includes “at least an n-type nitride semiconductor layer 101, a luminescent layer 102, and a p-type nitride semiconductor layer 103.” EX1007, [0054], [0079]. Then in Figure 10B, Horio forms a resist layer 130 through spin-coating and pre-baking. EX1007, [0079]. Subsequently in Figures 10C-10D, Horio exposes portions of the resist layer 130 to light, and develops the resist layer 130. EX1007, [0080]. EX1002, ¶165.

In Figure 10E—after the development—Horio performs a “post bake.” EX1007, [0080]-[0081]. Horio explains that:

By adjusting temperature and time in this *post bake process*, the whole resist layer 130 shrinks. Thus, *it is possible to incline the end portions of the resist at an angle in accordance with a bake condition*. To be more specific, the end portions of the resist layer 130 incline at an inclination angle of 55 degrees on a post bake condition of *110 degrees centigrade* and 120 seconds. The inclination angle becomes 45 degrees on a post bake condition of *115 degrees centigrade* and 120 seconds, and the inclination angle becomes 35 degrees on a post bake condition of *120 degrees centigrade* and 120 seconds.

EX1007, [0081]. EX1002, ¶166.

Subsequently in Figure 10F, Horio etches the “nitride semiconductor layer 11 up to a predetermined depth by dry etching using a chlorine gas (FIG. 10F).” EX1007, [0082]. Through this dry etching step, “the *end faces of the nitride semiconductor layer 11 are formed into an inclination angle which is determined by the inclination angle of the resist layer 130 and the selection ratio.*”⁹ EX1007, [0082]. Then in Figure 10G, Horio removes the remaining photoresist from the top surface. EX1007, Figure 10G, [0083].

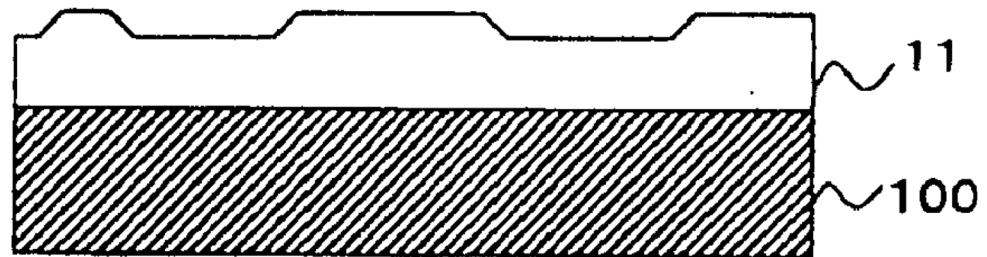
⁹ The “selection ratio” is the ratio of rates at which the etchant etches the photoresist layer 130 and the semiconductor layer 110. EX1007, [0086].

EX1002, ¶168.

This process creates a stack of p-type layer 103, luminescence layer 102, and n-type layer 101 with an inclined (or sloped) side surface, as shown in Figure 10G.

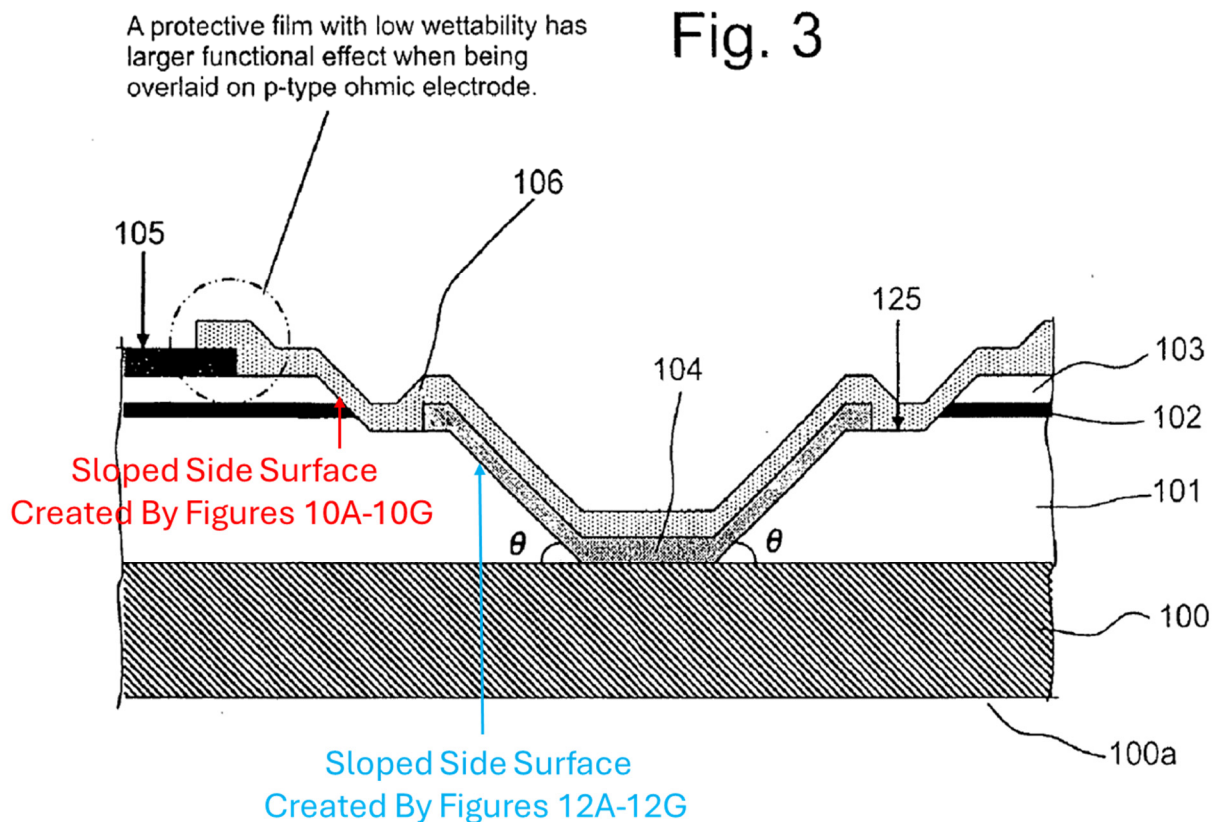
Fig. 10G

- Cleaning



EX1007, Figure 10G. EX1002, ¶¶167-169.

To form the rest of the structures shown in Figure 3, Horio performs another lithography process described in Figures 12A-12G that also forms an inclined surface at the bottom portion of the n-type layer 101. Like the process in Figures 10A-10G, the process in Figures 12A-12G uses an inclined photoresist layer to create a sloped side surface on the bottom portion of the n-type layer 101. *See* EX1007, [0090]. The processes in Figures 10A-10G and Figures 12A-12G both provide inclined side surfaces at a “predetermined angle θ .” EX1007, [0074], Figure 3.



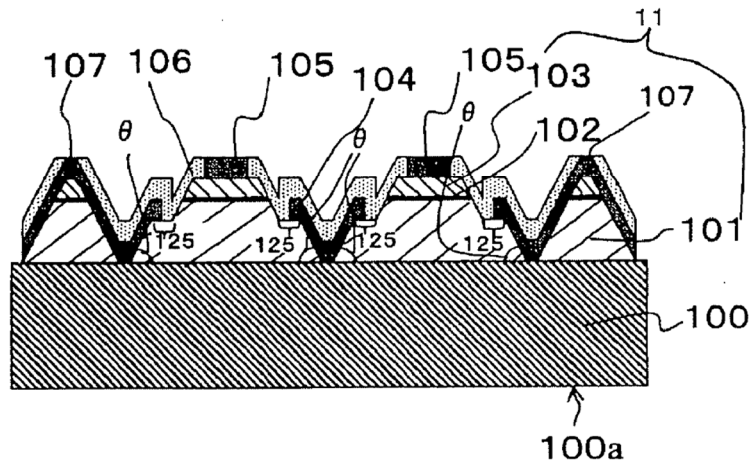
EX1007, Figure 3. EX1002, ¶170.

2. Claim 9

- i. [9Pre] A method of manufacturing a light emitting device, comprising:

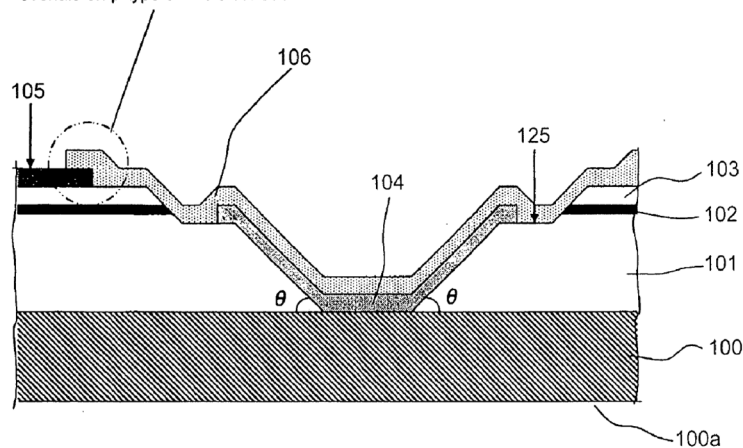
Horio discloses [9Pre]. Horio is titled “Semiconductor *Light Emitting Device* and *Manufacturing Method* Thereof,” and teaches “[a] method for *manufacturing the light emitting device*” shown in Figures 2B and 3. EX1007, Title, [0088]-[0090] (describing manufacturing process of LED in Figure 2B); [0034] (“FIG. 3 is an enlarged view of a portion of FIG. 2B.”). *See also* EX1007, Claim 29, [0029], [0077].

Fig. 2B



A protective film with low wettability has larger functional effect when being overlaid on p-type ohmic electrode.

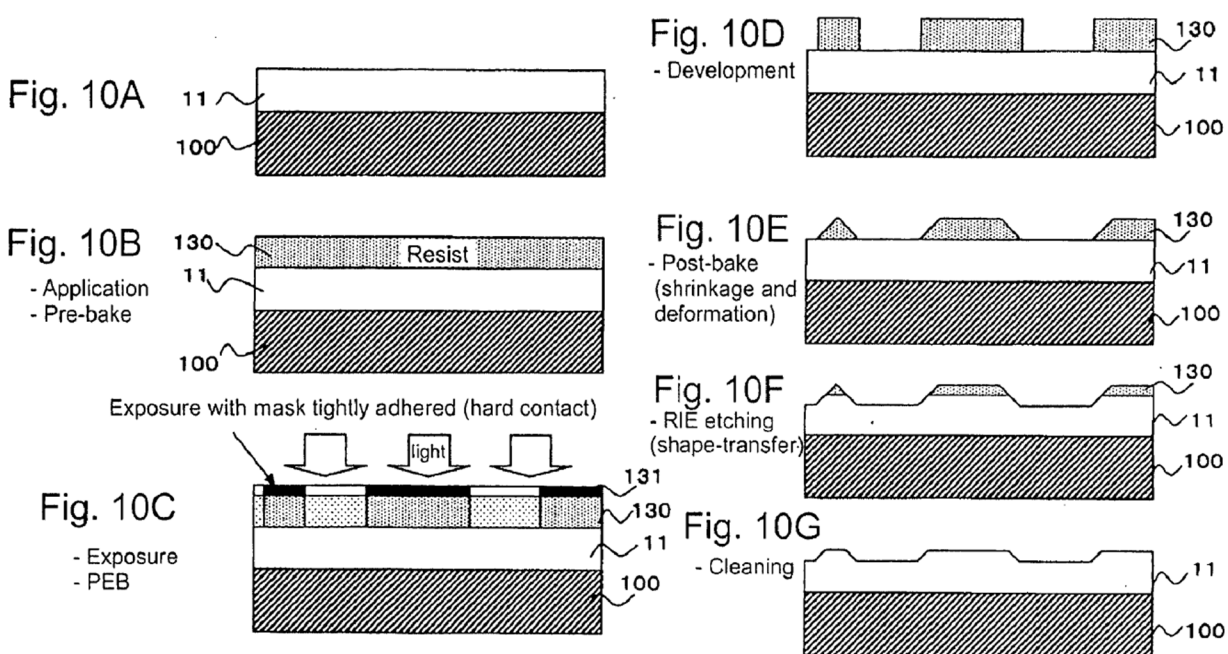
Fig. 3



EX1007, Figures 2B, 3. EX1002, ¶171.

Horio's method of manufacturing the LED in Figure 3 includes the lithography processes for forming an inclined side surface of an LED, illustrated in Figures 10A-10G and 12A-12G. EX1007, [0088]-[0090] (describing use of the

processes in Figures 10A-10G and 12A-12G to make the device in Figure 3), [0034],
 Figures 10A-10G, 12A-12G. *See generally* EX1007, [0077]-[0087].

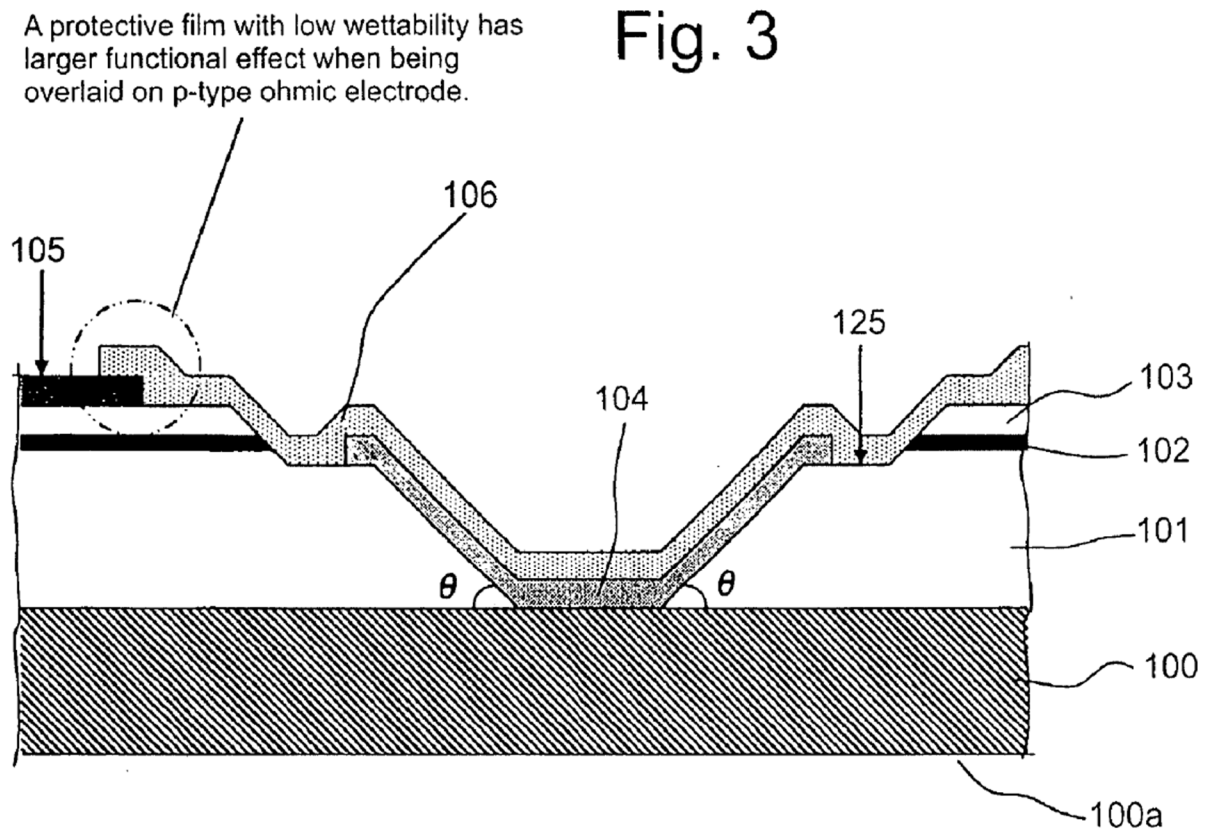


EX1007, Figures 10A-10G. EX1002, ¶172.

- ii. [9A] sequentially forming an N-type semiconductor layer, active layer, and P-type semiconductor layer on a substrate;

Horio discloses [9A]. Horio teaches forming a “*nitride semiconductor layer 11* [that] includes at least an n-type nitride semiconductor layer 101, a luminescent layer 102, and a p-type nitride semiconductor layer 103 which can be laminated *in this order* on the sapphire substrate 100.” EX1007, [0054], [0079], [0088]. Indeed, Figure 3 below shows that the n-type nitride semiconductor layer 101, the

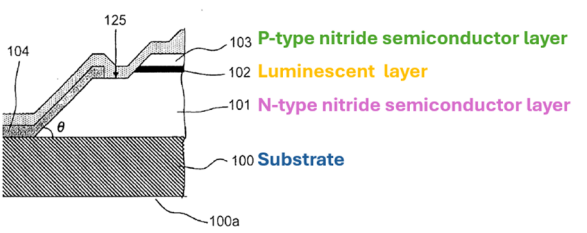
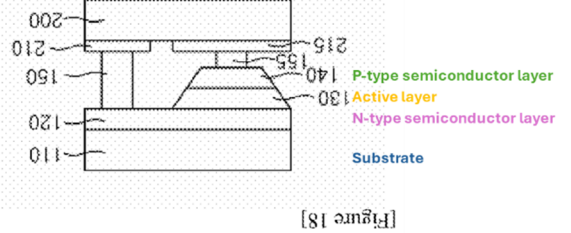
luminescent layer 102, and the p-type nitride semiconductor layer 103 are sequentially formed on the substrate 100.



EX1007, Figure 3. EX1002, ¶173.

Horio's luminescent layer 102 teaches the claimed "active layer" because the luminescent layer 102, sandwiched between N-type and P-type semiconductor layers, generates light. EX1007, [0008] ("light is emitted from a luminescent layer"); [0054] ("Light from the luminescent layer 102 is emitted from the rear face (emission surface) 100 a of the sapphire substrate 100."). Indeed, the luminescent layer 102 is nearly identical to the "active layer" of the '626 Patent. EX1001, 12:51-

54 (“Referring to FIG. 18, the light emitting device comprises a light emitting layer, i.e. an N-type semiconductor layer 120, an active layer 130 and a P-type semiconductor layer 140 sequentially formed on a base substrate 110.”); 6:22-27 (“The active layer 30 has a predetermined bandgap and is a region where a quantum well is formed so that electrons and holes are recombined. ... The wavelength of light emitted through the combination of electrons and holes varies according to the kind of a material constituting the active layer 30.”).

Horio, Figure 3 (portion)	'626 Patent, Figure 18 (flipped)
Fig. 3  104 125 103 P-type nitride semiconductor layer 102 Luminescent layer 101 N-type nitride semiconductor layer 100 Substrate 100a	 200 210 215 155 140 130 120 110 115 110a P-type semiconductor layer Active layer N-type semiconductor layer Substrate [Figure 18]

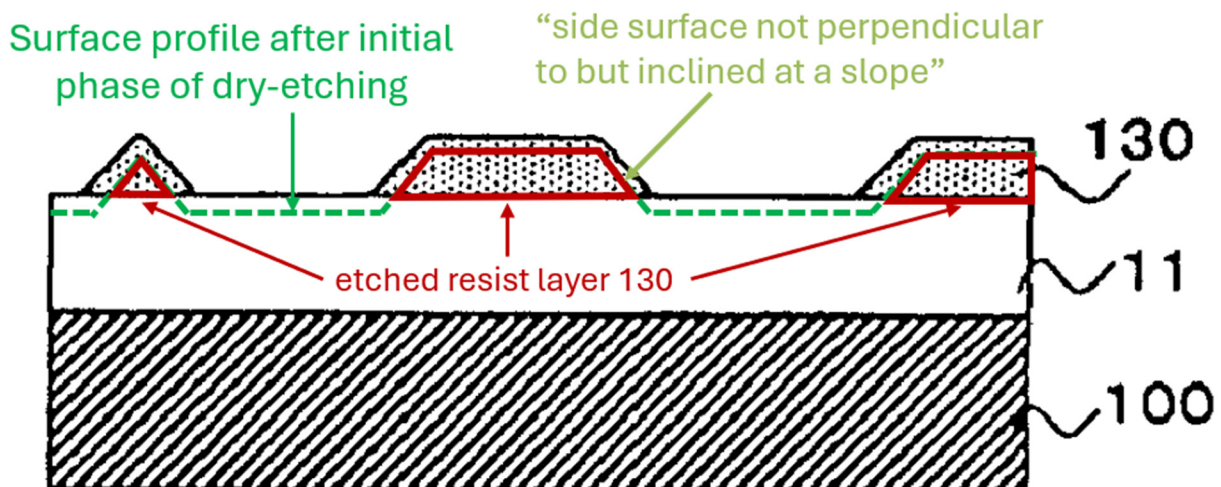
EX1007, Figure 3; EX1001, Figure 18. EX1002, ¶¶174-175.

- iii. [9B] forming an **etching mask pattern**, of which a side surface is not perpendicular to but inclined at a **slope from a horizontal plane**, on the **P-type semiconductor layer**;
[9D-1] wherein forming the **etching mask pattern** comprises: forming a **photoresist** on the **P-type semiconductor layer**;
[9D-2] exposing the **photoresist** to light;
[9D-3] **hard-baking** and **developing** the **photoresist**; and
[9D-4] **etching** a side surface of the developed **photoresist** to have the **slope from the horizontal plane**.
[9C] removing the **etching mask pattern** and the **P-type semiconductor layer** exposed through the **etching mask pattern**

Horio discloses [9B], [9D-1]-[9D-4], and [9C]. EX1002, ¶176.

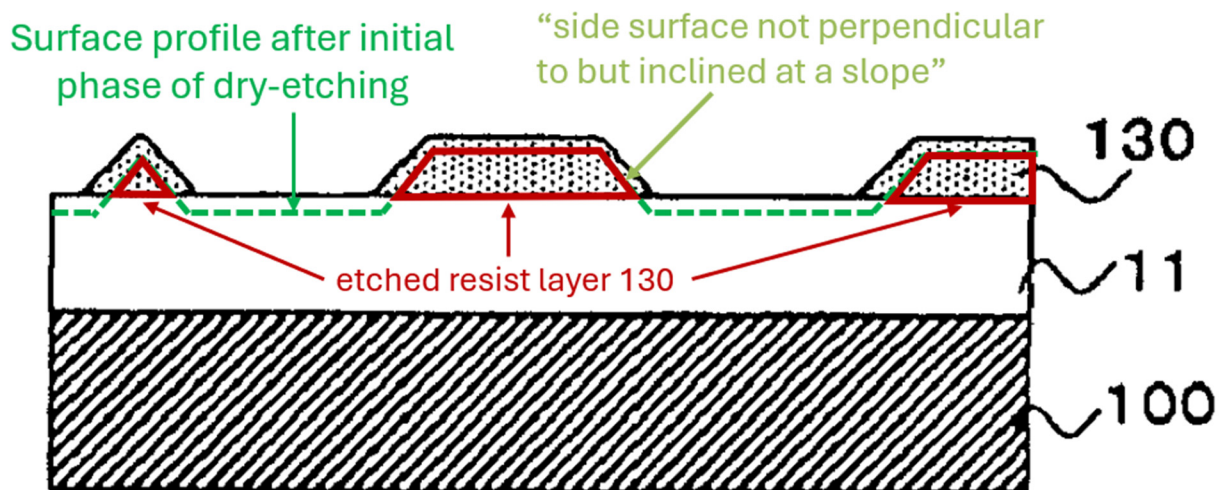
- a. [9B] forming an **etching mask pattern**, of which a side surface is not perpendicular to but inclined at a **slope from a horizontal plane**, on the **P-type semiconductor layer**

As explained in more detail below in Section X.E.2.iii.b, Horio discloses forming an **etched resist layer 130** (the claimed “**etching mask pattern**”), including all of the details recited in limitations [9D-1]-[9D-4].



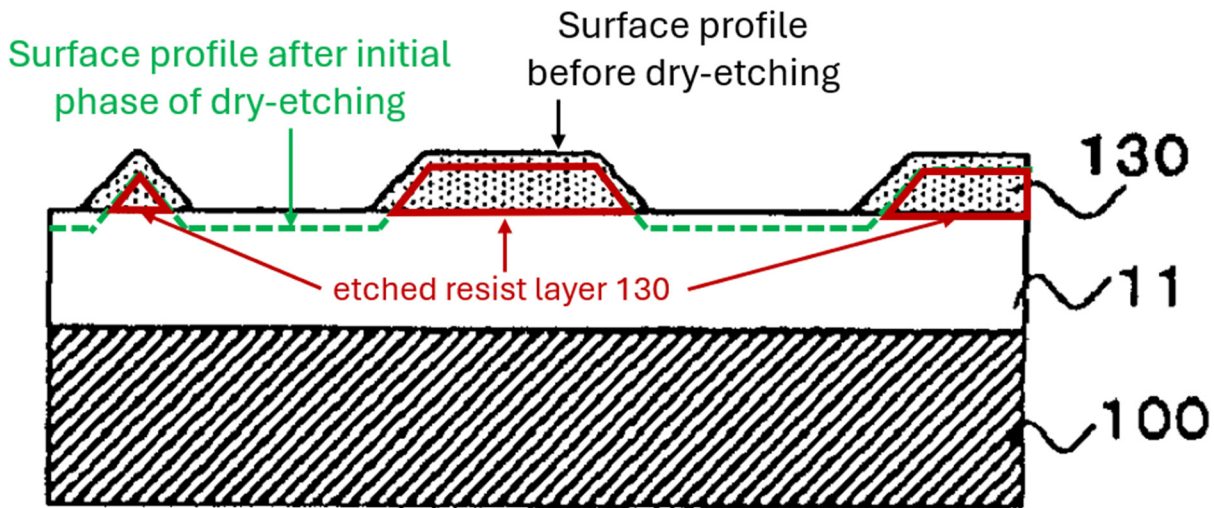
EX1007, Figure 10E (modified). EX1002, ¶177.

Horio also teaches that the **etched resist layer 130** (the claimed “**etching mask pattern**”) has “a side surface [that] is not perpendicular to but inclined at **a slope from a horizontal plane**.” For example, as explained below in Section X.E.2.iii.b(d) [Ground V, 9D-4], the initial phase of Horio’s dry-etching step (the claimed “**etching**” step) maintains the **slope** on the side surfaces of the **etched resist layer 130** with respect to a horizontal plane formed by the top surface of the semiconductor layer 11.



EX1007, Figure 10E (modified). EX1002, ¶178.

Horio further discloses forming the **etched resist layer 130** “on the **P-type semiconductor layer**.” As seen below, the **etched resist layer 130** is formed on top of the semiconductor layer 11 which, as described in Section X.E.2.ii [Ground V, 9A], includes the **p-type semiconductor layer 103** as the top layer. EX1007, [0077]-[0079].



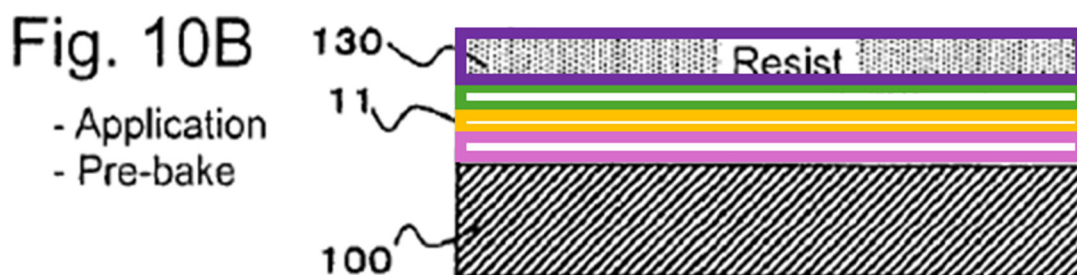
EX1007, Figure 10E (modified). EX1002, ¶179.

b. “forming an etching mask pattern” Pursuant To [9D-1]-[9D-4]

Horio discloses “forming an etching mask pattern,” including all of the details recited in limitations [9D-1]-[9D-4]. EX1002, ¶180.

(a) [9D-1] “forming a photoresist on the P-type semiconductor layer;”

Horio teaches forming a resist layer 130 on a nitride semiconductor layer 11. EX1007, Figure 10B, [0079] (“To be more specific, a resist is evenly applied to the wafer-shaped substrate 100 in which the nitride semiconductor layer 11 is formed in advance by use of a spin coater. After a resist coating layer is formed, a resist layer 130 is formed by pre-baking (FIGS. 10A and 10B).”). As explained in Section X.E.2.ii [Ground V, 9A], the top-most layer of the semiconductor layer 11 is a p-type semiconductor layer. EX1007, [0054], [0079], [0088].

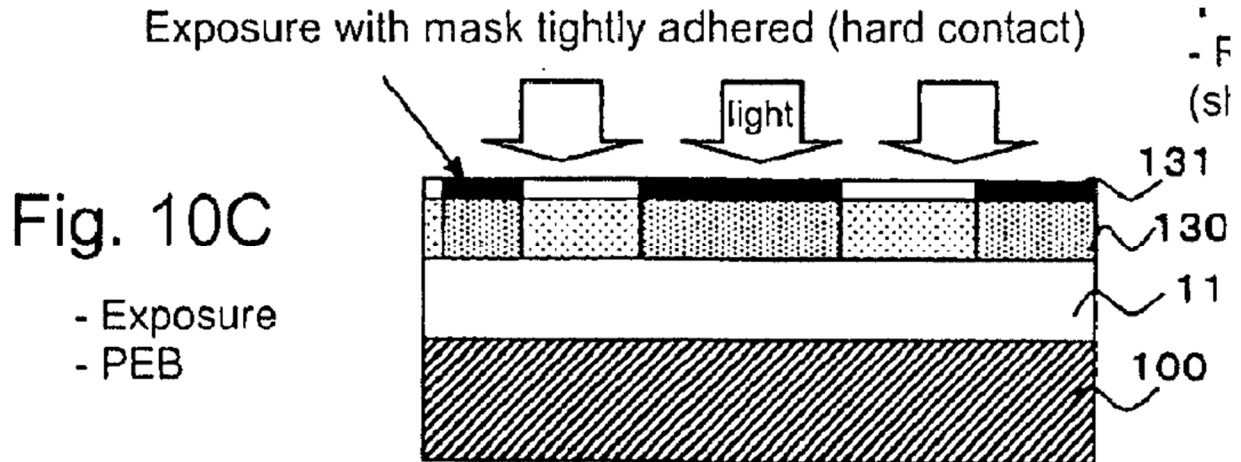


EX1007, Figure 10B. EX1002, ¶181.

Horio explains that one example of **resist layer 130** is “a **heat-resistant g-line positive resist** (trade name: **AZ6130**, made by Clariant (Japan)K.K.).” EX1007, [0079]. It was well recognized that **AZ6130** from Clariant is a **photoresist**. EX1021, 2 (“patterning of the **photoresist (AZ6130, Clariant)**”). EX1002, ¶182.

(b) [9D-2] “exposing the **photoresist** to light;”

Horio discloses selectively exposing the **resist layer 130** to light through a photomask. EX1007, [0080] (“Then, a photomask for transferring a pattern and the substrate 100 with the **resist layer 130** as shown in FIG. 10B are set on the mask aligner, to carry out contact **exposure** (hard contact) (FIG. 10C).”). Figure 10C expressly shows that the **resist layer 130** is exposed to “light.”

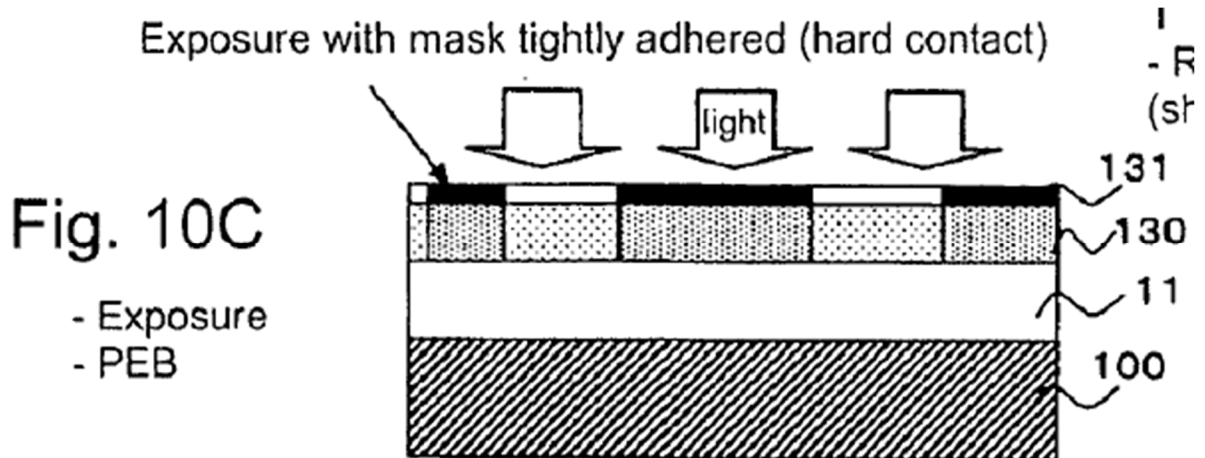


EX1007, Figure 10C. EX1002, ¶183.

(c) [9D-3] “hard-baking and developing the photoresist; and”

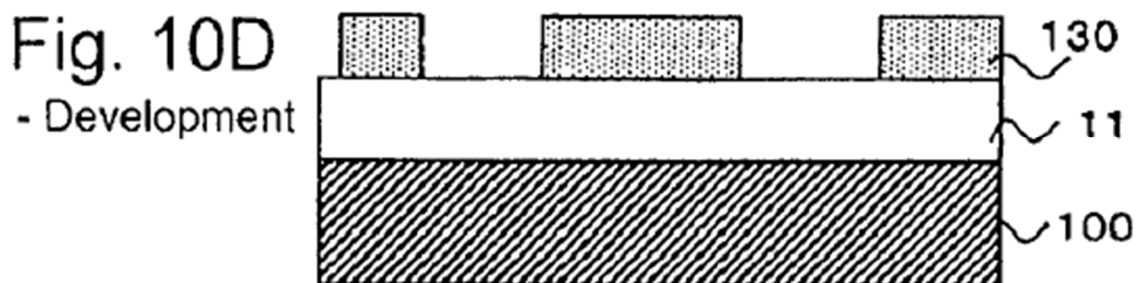
As explained below, Horio teaches developing the photoresist. Horio also teaches baking the photoresist before *and* after that development step, either or both of which satisfies the claimed “hard-baking” because [9D-3] does not impose any temporal limitation on the “hard-baking” step and the “develop[ment]” step. *Koninklijke Philips*, 2024 WL 3042238, at *4. EX1002, ¶184.

More specifically, Horio explains that after exposure to light, the resist layer 130 is subject to a “post exposed bake (hereinafter abbreviated as PEB)” that “is carried out on a condition of *110 degrees centigrade* and 120 seconds.” EX1007, [0080], Figure 10C.



EX1007, Figure 10C. EX1002, ¶185.

After the **post exposure bake (PEB)**, Horio “**develop[s]** the **photoresist.**” EX1007, [0080] (“**[D]evelopment** is carried out by use of a developing solution (trade name: AZ300MIF, made by Clariant(Japan)K.K.), and the **resist layer 130 in exposed portions are removed** (FIG. 10D).”).



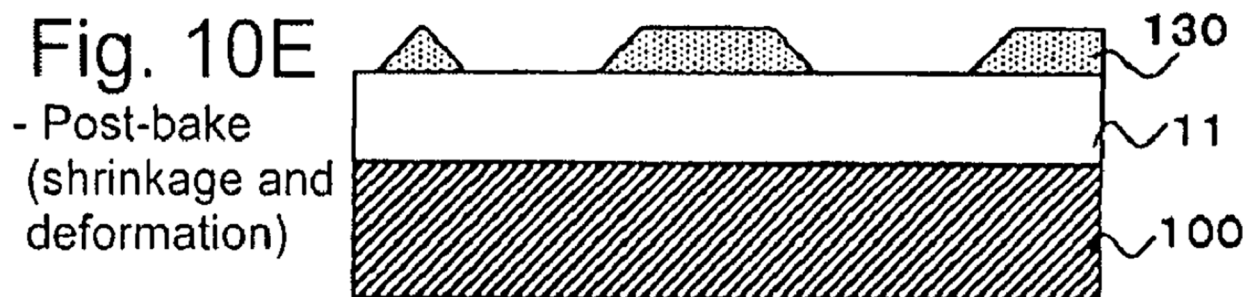
EX1007, Figure 10D. EX1002, ¶186.

Subsequently, Horio carries out another **bake** on the developed **resist layer 130**, which Horio calls a “**post bake**,” as shown in Figure 10E. EX1007, [0080]-

[0081]. Horio teaches that the *post bake is carried out at a temperature of 110 to 120° C* depending on the desired side surface slope of the resist layer 130:

To be more specific, the end portions of the resist layer 130 incline at an inclination angle of 55 degrees on a *post bake* condition of *110 degrees centigrade* and 120 seconds. The inclination angle becomes 45 degrees on a *post bake* condition of *115 degrees centigrade* and 120 seconds, and the inclination angle becomes 35 degrees on a *post bake* condition of *120 degrees centigrade* and 120 seconds.

EX1007, [0081].



EX1007, Figure 10E. EX1002, ¶187.

The *PEB* step and the *post bake* step both satisfy the claimed “hard baking” limitation because the temperature ranges of the *PEB* and *post bake* each overlap with the temperature range of *hard baking* required by claim 15: “performed at a temperature of 100 to 140°C.” EX1001, claim 15. EX1007, [0080] (*PEB* occurring at “110°C”); [0081] (*post bake* occurring at “110°C”, “115°C”, or “120°C”). EX1002, ¶188.

(d) [9D-4] “etching a side surface of the developed photoresist to have the slope from the horizontal plane.”

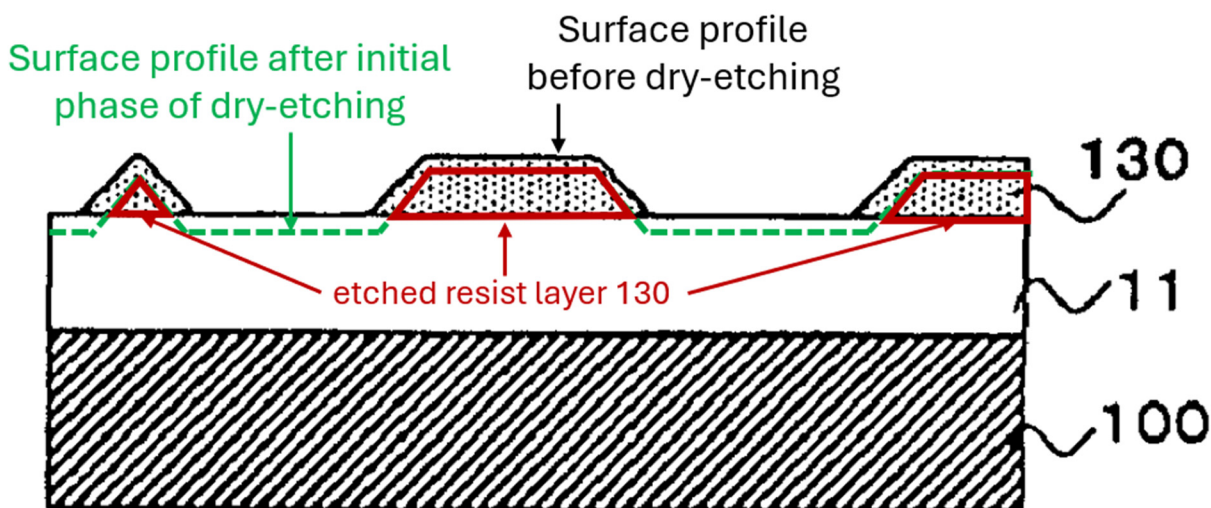
As an initial matter, the '626 Patent states that “if the photoresist is hard-baked at a temperature of 100 to 140° C. and then developed, the side surface of the developed photoresist may be etched to have a slope of 80 to 20° from a horizontal plane.” EX1001, 7:24-27. To the extent the quoted embodiment discloses a single etching step that performs both the “etching” step of [9D-4] and the “removing” step of [9C], Horio discloses [9D-4] (and as explained below, [9C]). EX1002, ¶189.

More specifically, like the '626 Patent, Horio discloses dry-etching both the developed resist layer 130 and the underlying semiconductor layer simultaneously. For example, after developing the resist layer 130, “the *substrate with the resist layer 130* that has end faces which are inclined as shown in FIG. 10E is *set on an RIE (reactive ion etching)* device.” EX1007, [0082].¹⁰ Horio’s RIE dry-etching step etches both the developed resist layer 130 and the exposed portion of the semiconductor layer 11 simultaneously because the “selection ratio [between the resist layer 130 and the semiconductor layer 11] of this dry etching is approximately

¹⁰ RIE is a type of anisotropic dry-etching that etches an exposed surface by bombarding accelerated reactive ions onto the exposed surface. EX1023, 2, 4. EX1002, ¶190.

1.” EX1007, [0082]. In other words, Horio’s RIE dry-etching step etches both the developed resist layer 130 and the exposed nitride semiconductor layer 11 at the same time. EX1007, [0086]. Further, because the RIE dry-etching etches all exposed surfaces—including the side surface of the developed resist layer 130. EX1002, ¶¶190-192.

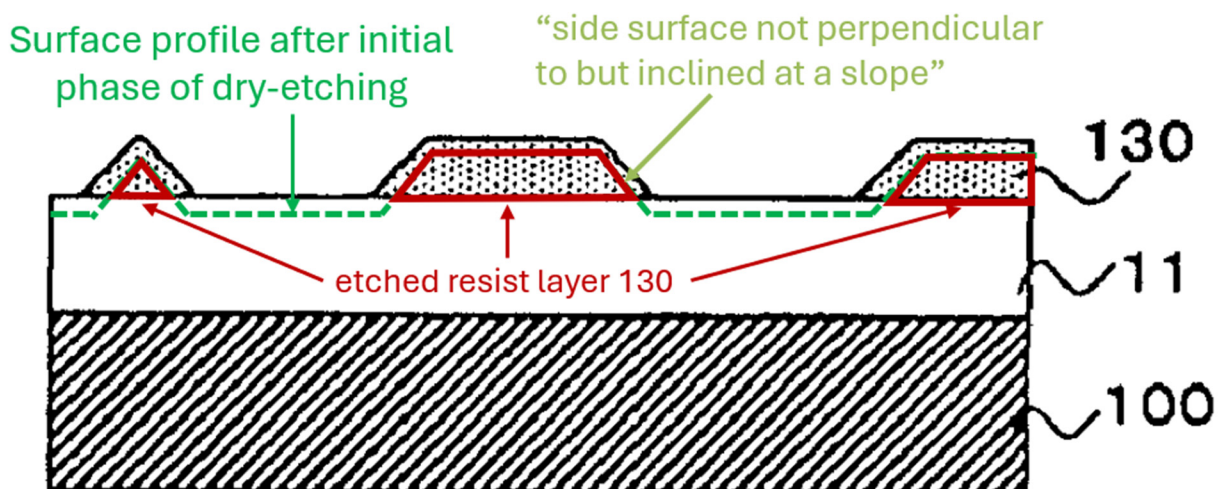
During the *initial phase* of dry-etching specifically, the top exposed portions of the developed resist layer 130 are etched away predominantly in the vertical direction. EX1022, [0227]-[0234], Figures 20A-20B. The resulting structure is shown below.



EX1007, Figure 10E (modified). EX1002, ¶193.

Horio also discloses that during the *initial phase* of Horio’s dry-etching, the side surface of the developed resist layer 130 is etched “to have the slope from the horizontal plane.” As explained above in Section X.E.2.iii.b(c) [Ground V, 9D-3]

and as shown in Figure 10E, the developed resist layer 130 has sloped side surfaces. EX1007, [0081], [0084] (“[I]t is possible to *incline the end portions of the resist layer 130* with high reproducibility at an angle corresponding to the post bake condition ... ”); [0085]. Because the initial phase of *dry-etching* etches the exposed surfaces of the resist layer 130 predominantly in the vertical direction, the initial phase of *dry-etching* etches the developed resist layer 130 “to have the *slope* from the horizontal plane.” See EX1022, [0227]-[0234], Figures 20A-20B.



EX1007, Figure 10E (modified). EX1002, ¶194.

* * *

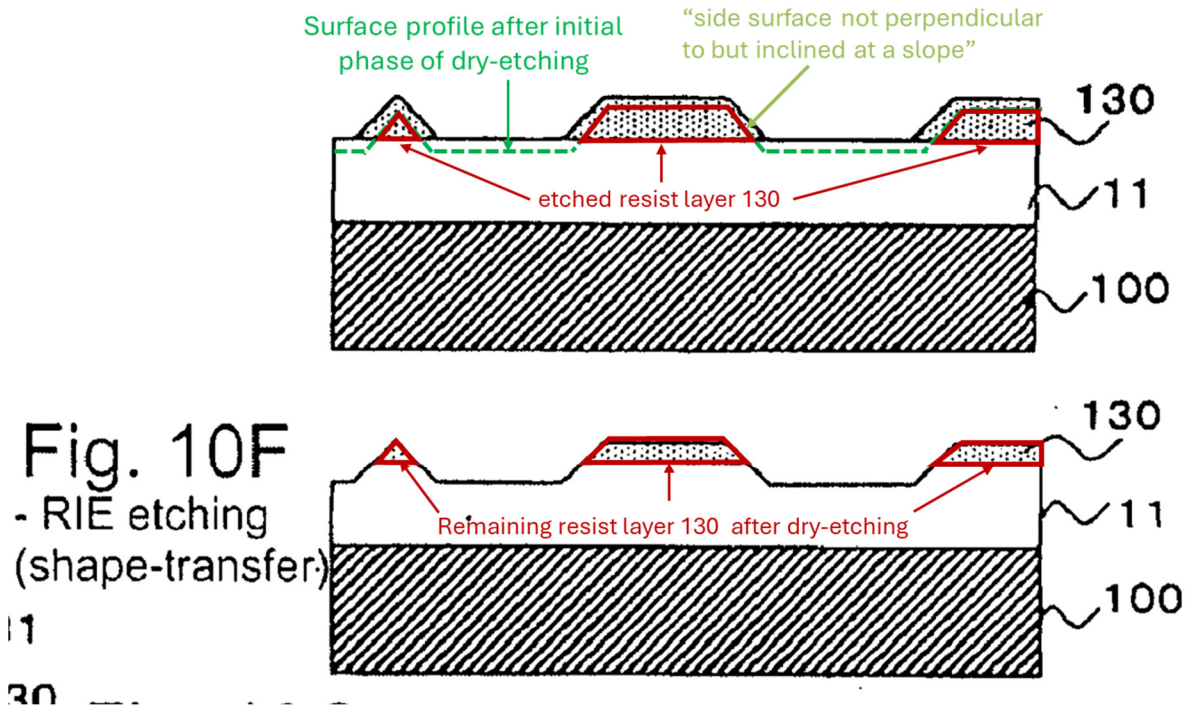
The resulting product—the developed resist layer 130 that has undergone an initial phase of *dry-etching*, herein referred to as the “*etched resist layer 130*”—is an “*etching mask pattern*” as claimed because the *etched resist layer 130* is further used to mask the underlying p-type layer from the remaining dry-etching. EX1007, [0082], Figure 10F. See also Section X.E.2.iii.c [Ground V, 9C]. EX1002, ¶195.

c. [9C] removing the **etching mask pattern** and the **P-type semiconductor layer** exposed through the **etching mask pattern**;

Horio discloses [9C]. After the initial phase of the dry-etching step corresponding to the “etching” step of [9D-4], Horio’s dry-etching continues to remove the **etched resist layer 130** and the **P-type semiconductor layer** exposed through the **etched resist layer 130**. EX1002, ¶196.

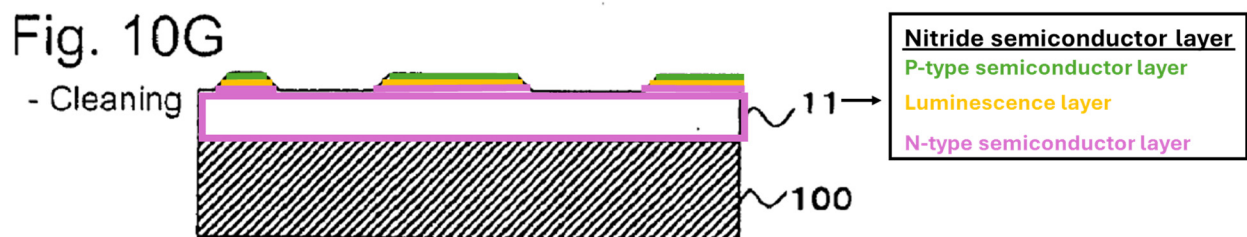
Specifically, Horio teaches that after forming the **etched resist layer 130**, “the *nitride semiconductor layer 11 in the open portions* [including the **p-type layer 103** exposed through the **etched resist layer 130**] is etched to a predetermined depth of the terrace 125 by use of a dry etching technology. Thus, the **p-type nitride semiconductor layer 103**, the luminescent layer 102, and a part of the n-type nitride semiconductor layer 101 are **removed** (FIG. 10F).” EX1007, [0089]; [0082], Figure 10E. EX1002, ¶197.

And for the reasons provided in Section X.E.2.iii.b(d) [Ground V, 9D-4], the dry-etching step continues to etch the **etched resist layer 130**. EX1007, [0082], [0086]. That way, “the inclined shape of the **resist layer 130** is transferred to the nitride semiconductor layer 11.” EX1007, [0082]. Thus, the remaining dry-etching step also removes at least some portions of the **etched resist layer 130**.



EX1007, Figures 10E(modified)-10F. EX1002, ¶198.

Once the dry-etching is completed, “[t]he **resist layer 130** is [completely] removed by dissolving, and cleaned lastly,” as shown in Figure 10G. EX1007, [0083]; [0089].



EX1007, Figure 10G. EX1002, ¶199.

Accordingly, the remaining dry-etching step alone, or the remaining dry-etching step and the resist cleaning step collectively, discloses removing the **etched**

resist layer 130 (the claimed “etching mask pattern”) and the p-type nitride semiconductor layer 103 (the claimed “P-type semiconductor layer”) exposed through the etched resist layer 130. EX1002, ¶200.

3. Claim 13

- i. [13] The method as claimed in claim 9, wherein the photoresist with a thickness of 3 to 50 μm is used in the forming the etching mask pattern.

Horio discloses [13]. Horio discloses that the resist layer 130 with a thickness of “*approximately 10 μm* ” is used to form the resist layer 130 in Figure 10B, and the resist layer 130 is then used to form the etched resist layer 130 (the claimed etching mask pattern). EX1007, [0085], Figures 10B-F. *See also* Section X.E.2.iii.b(d) [Ground V, 9D-4]. EX1002, ¶201.

4. Claim 15

- i. [15] The method as claimed in claim 9, wherein the hard-baking is performed at a temperature of 100 to 140° C.

Horio discloses [15]. As explained in Section X.E.2.iii.b(c) [Ground V, 9D-3], Horio discloses hard-baking the resist layer 130 (the claimed photoresist) at a temperature of 100 to 140° C. For example, Horio explains that a “post exposed bake” is performed at a temperature of 110° C (EX1007, [0080], Figure 10C), and a “*post bake*” is performed at a temperature of 110°C, 115°C, or 120°C (EX1007, [0080]-[0081], Figure 10E). Accordingly, the post exposed bake step and/or the post

bake step teaches hard-baking the resist layer 130, and the hard-baking is performed at a temperature of 100 to 140° C. EX1002, ¶202.

XI. Discretionary Factors Favor Institution

The discretionary factors the Board employs for its institution decisions favor institution.

A. Advanced Bionics Factors Favor Institution.

This Petition presents five prior art references—Eliashevich, Rabinzohn, Yoo, Huang, and Horio. The Patent Office has never considered the prior art references presented, and these prior art references are noncumulative over the references previously considered. Thus, the presented prior art references do not satisfy the first prong of *Advanced Bionics*, and discretionary denial under *Advanced Bionics* is not warranted. *See Advanced Bionics LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 (precedential).

B. Discretionary Denial Under *Fintiv* Is Not Appropriate.

At the outset, Petitioner filed a motion to transfer the pending case from the Eastern District of Texas to the District of New Jersey, where Samsung Electronics America Inc. resides. *See Sinotechnix LLC v. Samsung Electronics Co. Ltd et al.*, Case No. 2:24-cv-00544, Dkt. No. 53 (EDTX). While Petitioner will inform the Board of the latest developments related to the *Fintiv* factors as they become

available, the following analysis is based on the *current* venue in the Eastern District of Texas for the parallel district court litigation.

Based on the current facts, the six *Fintiv* factors guide against discretionary denial. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (precedential).

1. No Evidence Regarding A Stay

Factor 1 is neutral because no motion to stay has been filed.

2. Parallel Proceeding Trial Date

Factor 2 is neutral. Trial in co-pending litigation is scheduled for May 4, 2026. EX1018 [Docket Control Order]. The expected trial date based on the court’s median time-to-trial date statistics is also approximately May 2026. *See* EX1019 (showing the median time-to-trial date is approximately 21.9 months from the filing of the case (*i.e.*, July 17, 2024)). Both of these dates are close to the expected final written decision date, which is around August 2026.

However, there is significant uncertainty over the trial date. Judge Gilstrap has scheduled trials for eleven other cases for May 4, 2026. EX1020 [Judge Gilstrap Trial List]. It is at the very least uncertain that the ’626 Patent will be tried on May 4, 2026. Hence, this factor is neutral.

As the interim guideline notes, “when other relevant factors weigh against exercising discretion to deny institution or are neutral, the proximity to trial should not alone outweigh all of those other factors.” Memorandum Regarding Interim

Procedure for Discretionary Denials¹¹, 8 (*citing In re Genentech, Inc.*, 566 F.3d 1338, 1347 (Fed. Cir. 2009)).

3. Investment In Parallel Proceeding

Factor 3 favors institution. The co-pending litigation is in its early stages, and the investment in it has been minimal. *See* EX1018. The parties have not exchanged preliminary positions on claim construction, and discovery opened only recently on December 17, 2024. *See PEAG LLC v. Varta Microbattery GmbH*, IPR2020-01214, Paper 8, 17 (Jan. 6, 2021). Invalidity contentions have not been served. *See* EX1018, 5. Markman hearing is not scheduled until November 7, 2025, and expert discovery is scheduled for completion on January 20, 2026—both of which are after the expected institution decision date of August 2025 for this instant IPR. EX1018, 3-4. Hence, this factor favors institution.

4. Overlapping Issues With Parallel Proceeding

Factor 4 favors institution. Petitioner stipulates that if the IPR is instituted, Petitioner will not pursue the same grounds in the district court litigation. *Sand Revolution II LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-

¹¹ Available online at

https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf

01393, Paper 24 at 7 (June 16, 2020) (informative). As such, the Grounds presented in the instant IPR will be materially different from the grounds that will be presented in the district court. Petitioner may further update the stipulation in this instant proceeding after invalidity contentions have been exchanged with Patent Owner on February 14, 2025 in the co-pending district court litigation.

5. Identity Of Parties

Petitioner is the defendant in the co-pending litigation. This factor should not be a basis for denying institution.

6. Other Circumstances, Including The Merits

Factor 6 guides against discretionary denial. “[W]here the PTAB determines that the information presented at the institution stage presents a compelling unpatentability challenge, that determination alone demonstrates that the PTAB should not discretionarily deny institution under *Fintiv*.” Memo, 4-5. Here, the evidence of unpatentability is compelling, as evidenced by Grounds laid out above. This factor also guides against discretionary denial.

Accordingly, *Fintiv* factors guide against discretionary denial.

C. General Plastic Factors Favor Institution

The ’626 patent has not been challenged in any prior IPR petition, so none of the *General Plastic* factors apply to this Petition and the *General Plastic* Factors favor institution.

XII. Conclusion

Petitioner respectfully requests that the Board institute *inter partes* review, hold the challenged claims unpatentable, and cancel the challenged claims.

Dated: February 13, 2025

Respectfully submitted,

/Taeg Sang Cho/

Taeg Sang Cho (Reg. No. 69,618)

DESMARAIS LLP

230 Park Avenue

New York, NY 10169

Telephone: 212-351-3400

Facsimile: 212-351-3401

Counsel for Petitioner

Samsung Electronics Co., Ltd.

Samsung Electronics America, Inc.

Petition for *Inter Partes* Review of U.S. Patent No. 7,951,626
Claims 1, 3, 7, 9, 13, 15

CERTIFICATION UNDER 37 C.F.R. § 42.24(d)

I hereby certify that this Petition for *Inter Partes* Review of U.S. Patent No. 7,951,626 has, excluding the portions exempted under 37 C.F.R. § 42.24(a), 13,595 words as counted by the word-processing system used to prepare this document, in compliance with 37 C.F.R. § 42.24(d).

Dated: February 13, 2025

Respectfully submitted,

/Taeg Sang Cho/

Taeg Sang Cho (Reg. No. 69,618)

DESMARAIS LLP

230 Park Avenue

New York, NY 10169

Telephone: 212-351-3400

Facsimile: 212-351-3401

Counsel for Petitioner

Samsung Electronics Co., Ltd.

Samsung Electronics America, Inc.

CERTIFICATE OF SERVICE

Under 37 C.F.R. §§ 42.6(e) and 42.126, the undersigned certifies that on February 13, 2025, complete copies of the foregoing and any accompanying exhibits were caused to be served by sending them via Federal Express Priority Overnight shipping, which is at least as fast and reliable as U.S. Priority Mail Express, to the correspondence address of record for U.S. Patent No. 7,951,626 as indicated in Patent Center:

H.C. Park & Associates, PLC
1894 Preston White Drive, Reston, VA

Petitioner is also serving courtesy copies to the counsel of record in the Litigation via Federal Express Priority Overnight shipping at:

Nelson Bumgardner Conroy PC
2727 North Harwood Street Suite #250
Dallas, TX 75201

Dated: February 13, 2025

Respectfully submitted,

/Taeg Sang Cho/
Taeg Sang Cho (Reg. No. 69,618)
DESMARAIS LLP
230 Park Avenue
New York, NY 10169
Telephone: 212-351-3400
Facsimile: 212-351-3401

Counsel for Petitioner
Samsung Electronics Co., Ltd.
Samsung Electronics America, Inc.