PTO-1390 (Rev. 09-08)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A SUBMISSION UNDER 35 U.S.C. 371

		ATTORNEY'S DOCKET NUMBER: P3962US00
		U.S. APPLICATION NO. (If known, see 37 CFR 1.5):
INTERNATIONAL APPLICATION NO.: PCT/KR2008/006777	INTERNATIONAL FILING DATE: November 18, 2008	PRIORITY DATE CLAIMED: December 3, 2007

TITLE OF INVENTION: SLIM LED PACKAGE

APPLICANT(S) FOR DO/EO/US: Eun Jung SEO

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☑ This is a **FIRST** submission of items concerning a submission under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a submission under 35 U.S.C. 371.
3. ☑ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☑ The US has been elected (Article 31).
5. ☑ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☑ is attached hereto (required only if not communicated by the International Bureau).
   b. ☐ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☑ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☑ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☑ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☑ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☑ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. ☑ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☑ A preliminary amendment.
14. ☑ An Application Data Sheet under 37 CFR 1.76.
15. ☑ A substitute specification.
16. ☑ A power of attorney and/or change of address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13*ter*.3 and 37 CFR 1.821- 1.825.
18. ☐ A second copy of the published International Application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).

This collection of information is required by 37 CFR 1.414 and 1.491-1.492. The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 15 minutes to complete, including gathering information, preparing, and submitting the completed form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop PCT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

IPR2025-00334
Samsung Electronics Co., Ltd. v. Sinotechnix, LLC.
Samsung's Exhibit 1012
EX1012, Page 1

U.S. APPLICATION NO. (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
	PCT/KR2008/006777	P3962US00

20. Other items or information:

PCT/RO/105, PCT/IB/301, PCT/IB/306, PCT/IB/308, PCT/ISA/220, PCT/ISA/237, PCT/ISA/210

The following fees have been submitted	CALCULATIONS	PTO USE ONLY
21. ☑ Basic national fee (37 CFR 1.492(a)) **$330**	$ 330	
22. ☑ Examination fee (37 CFR 1.492(c)) If the written opinion prepared by ISA/US or the international preliminary examination report prepared by IPEA/US indicates all claims satisfy provisions of PCT Article 33(1)-(4)..... **$0** All other situations..... **$220**	$ 220	
23. ☑ Search fee (37 CFR 1.492(b)) If the written opinion of the ISA/US or the International preliminary examination report prepared by IPEA/US indicates all claims satisfy provisions of PCT Article 33(1)-(4)..... **$0** Search fee (37 CFR 1.445(a)(2)) has been paid on the international application to the USPTO as an International Searching Authority..... **$100** International Search Report prepared by an ISA other than the US and provided to the Office or previously communicated to the US by the IB..... **$430** All other situations..... $**540**	$ 540	
TOTAL OF 21, 22 and 23 =	1090	
☐ Additional fee for specification and drawings filed in paper over 100 sheets (excluding sequence listing in compliance with 37 CFR 1.821(c) or (e) in an electronic medium or computer program listing in an electronic medium) (37 CFR 1.492(j)). The fee is **$270** for each additional 50 sheets of paper or fraction thereof.		
Total Sheets: - 100 = / Extra Sheets: /50 = / Number of each additional 50 or fraction thereof (round **up** to a whole number): / RATE: x $**270**	$	
Surcharge of **$130.00** for furnishing any of the search fee, examination fee, or the oath or declaration after the date of commencement of the national stage (37 CFR 1.492(h)).	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	$	
Total claims	16 - 20 =		x $ **52**	$	
Independent claims	1 - 3 =		x **$220**	$	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$390**	$	
			TOTAL OF ABOVE CALCULATIONS =	$	
☐ Applicant claims small entity status. See 37 CFR 1.27. Fees above are reduced by ½.					
			SUBTOTAL =	$ 1090	
Processing fee of **$130.00** for furnishing the English translation later than 30 months from the earliest claimed priority date (37 CFR 1.492(i)). +				$	
			TOTAL NATIONAL FEE =	$ 1090	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$	
			TOTAL FEES ENCLOSED =	$ 1090	
			Amount to be refunded:	$	
			Amount to be charged	$	

a. ☐ A check in the amount of $ _____ to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $ _____ to cover the above fees.

c. ☑ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 503681.

d. ☑ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038. The PTO-2038 should only be mailed or faxed to the USPTO. However, when paying the basic national fee, the PTO-2038 may NOT be faxed to the USPTO.

ADVISORY: If filing by EFS-Web, do **NOT** attach the PTO-2038 form as a PDF along with your EFS-Web submission. Please be advised that this is **not** recommended and by doing so your **credit card information may be displayed via PAIR**. To protect your information, it is recommended paying fees online by using the electronic payment method.

NOTE: Where an appropriate time limit under 37 CFR 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the International Application to pending status.

SEND ALL CORRESPONDENCE TO:

H.C. Park & Associates, PLC
8500 Leesburg Pike
Suite 7500
Vienna, VA 22182

/hae-chan park/
SIGNATURE

Hae-Chan PARK
NAME

50114
REGISTRATION NUMBER

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
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SEND ALL CORRESPONDENCE TO:

H.C. Park & Associates, PLC
8500 Leesburg Pike
Suite 7500
Vienna, VA 22182

/hae-chan park/
SIGNATURE

Hae-Chan PARK
NAME

50114
REGISTRATION NUMBER

Privacy Act Statement

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PCT REQUEST

Print Out (Original in Electronic Form)

0	**For receiving Office use only**	
0-1	International Application No.	
0-2	International Filing Date	
0-3	Name of receiving Office and "PCT International Application"	

0-4	**Form PCT/RO/101 PCT Request**	
0-4-1	Prepared Using	PCT-SAFE Version 3.51.036.211 MT/FOP 20090101/0.20.5.15
0-5	**Petition** The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty	
0-6	**Receiving Office (specified by the applicant)**	Korean Intellectual Property Office (RO/KR)
0-7	**Applicant's or agent's file reference**	P08-5018
I	**Title of Invention**	SLIM LED PACKAGE
II	**Applicant**	
II-1	This person is	applicant only
II-2	Applicant for	all designated States except US
II-4	Name	SEOUL SEMICONDUCTOR CO., LTD.
II-5	Address	148-29, Gasan-dong, Geumcheon-gu, Seoul, 153-801 Republic of Korea
II-6	State of nationality	KR
II-7	State of residence	KR
II-8	Telephone No.	82-2-2106-7388
II-9	Facsimile No.	82-2-857-5430
II-11	Applicant's registration No. with the Office	1-1998-099837-1

PCT REQUEST

Print Out (Original in Electronic Form)

III-1	**Applicant and/or inventor**	
III-1-1	This person is	applicant and inventor
III-1-2	Applicant for	US only
III-1-4	Name (LAST, First)	SEO, Eun Jung
III-1-5	Address	1B-35, 727-5, Wonsi-dong, Danwon-gu, Ansan-si, Gyeonggi-do, 425-851 Republic of Korea
III-1-6	State of nationality	KR
III-1-7	State of residence	KR
IV-1	**Agent or common representative; or address for correspondence**	
	The person identified below is hereby/ has been appointed to act on behalf of the applicant(s) before the competent International Authorities as:	agent
IV-1-1	Name (LAST, First)	LEE, Soo Wan
IV-1-2	Address	1901-ho, Keungil Tower 19F, 677-25, Yeoksam-dong, Gangnam-gu, Seoul, 135-914 Republic of Korea
IV-1-3	Telephone No.	82-2-3543-2626
IV-1-4	Facsimile No.	82-2-3453-9339
IV-1-5	e-mail	aip@aiplaw.com
IV-1-5(a)	E-mail authorization The receiving Office, the International Searching Authority, the International Bureau and the International Preliminary Examining Authority are authorized to use this e-mail address to send, if the Office or Authority so wishes, advance copies of notifications in respect of this international application.	Yes
IV-1-6	Agent's registration No.	9-1998-000352-8
IV-2	**Additional agent(s)**	additional agent(s) with same address as first named agent
IV-2-1	Name(s)	CHO,Jin Tae(9-2003-000088-1); YUN,Jong Seop(9-2003-000089-8); LEE,Seong Kyu(9-2003-000083-0); LEE,Jae Woong(9-2007-000061-1)

PCT REQUEST

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V	DESIGNATIONS	
V-1	**The filing of this request constitutes under Rule 4.9(a), the designation of all Contracting States bound by the PCT on the international filing date, for the grant of every kind of protection available and, where applicable, for the grant of both regional and national patents.**	
V-2	**Item V-2 may only be used to exclude (irrevocably) the designations concerned if, at the time of filing or subsequently under Rule 26bis.1, the international application contains in Box No. VI a priority claim to an earlier national application filed in the particular State concerned, in order to avoid the ceasing of the effect, under the national law, of this earlier national application.**	KR
VI-1	**Priority claim of earlier national application**	
VI-1-1	Filing date	03 December 2007 (03.12.2007)
VI-1-2	Number	10-2007-0124469
VI-1-3	Country	KR
VI-2	**Priority document request** The receiving Office is requested to prepare and transmit to the International Bureau a certified copy of the earlier application(s) identified above as item(s):	VI-1
VI-3	**Incorporation by reference :** where an element of the international application referred to in Article 11(1)(iii)(d) or (e) or a part of the description, claims or drawings referred to in Rule 20.5(a) is not otherwise contained in this international application but is completely contained in an earlier application whose priority is claimed on the date on which one or more elements referred to in Article 11(1)(iii) were first received by the receiving Office, that element or part is, subject to confirmation under Rule 20.6, incorporated by reference in this international application for the purposes of Rule 20.6.	
VII-1	**International Searching Authority Chosen**	Korean Intellectual Property Office (ISA/KR)

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VIII	Declarations	Number of declarations	
VIII-1	Declaration as to the identity of the inventor	-	
VIII-2	Declaration as to the applicant's entitlement, as at the international filing date, to apply for and be granted a patent	-	
VIII-3	Declaration as to the applicant's entitlement, as at the international filing date, to claim the priority of the earlier application	-	
VIII-4	Declaration of inventorship (only for the purposes of the designation of the United States of America)	-	
VIII-5	Declaration as to non-prejudicial disclosures or exceptions to lack of novelty	-	
IX	**Check list**	number of sheets	electronic file(s) attached
IX-1	Request (including declaration sheets)	5	✓
IX-2	Description	7	✓
IX-3	Claims	2	✓
IX-4	Abstract	1	✓
IX-5	Drawings	4	✓
IX-7	TOTAL	19	
	Accompanying Items	paper document(s) attached	electronic file(s) attached
IX-8	Fee calculation sheet	-	✓
IX-9	Original separate power of attorney	-	✓
IX-18	PCT-SAFE physical media	-	-
IX-20	**Figure of the drawings which should accompany the abstract**	1	
IX-21	**Language of filing of the international application**	Korean	
X-1	**Signature of applicant, agent or common representative**	(PKCS7 Digital Signature)	
X-1-1	Name (LAST, First)	LEE, Soo Wan	
X-1-2	Name of signatory		
X-1-3	Capacity		

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10-1	**Date of actual receipt of the purported international application**	
10-2	**Drawings:**	
10-2-1	Received	
10-2-2	Not received	
10-3	**Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application**	
10-4	**Date of timely receipt of the required corrections under PCT Article 11(2)**	
10-5	**International Searching Authority**	ISA/KR
10-6	**Transmittal of search copy delayed until search fee is paid**	

FOR INTERNATIONAL BUREAU USE ONLY

11-1	**Date of receipt of the record copy by the International Bureau**	

PCT (ANNEX - FEE CALCULATION SHEET)

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(This sheet is not part of and does not count as a sheet of the international application)

0	**For receiving Office use only**	
0-1	International Application No.	
0-2	Date stamp of the receiving Office	

0-4	**Form PCT/RO/101 (Annex)** **PCT Fee Calculation Sheet**				
0-4-1	Prepared Using		PCT-SAFE Version 3.51.036.211 MT/FOP 20090101/0.20.5.15		
0-9	**Applicant's or agent's file reference**		P08-5018		
2	**Applicant**		SEOUL SEMICONDUCTOR CO., LTD.		
12	**Calculation of prescribed fees**		fee amount/multiplier	Total amounts (KRW)	
12-1	Transmittal fee	**T**	➪	45000	
12-2-1	Search fee	**S**	➪	225000	
12-2-2	International search to be carried out by		KR		
12-3	International filing fee (first 30 sheets)	**i1**	1327000		
12-4	Remaining sheets		0		
12-5	Additional amount	**(X)**	0		
12-6	Total additional amount	**i2**	0		
12-7	i1 + i2 =	**i**	1327000		
12-12	Electronic Filing reduction (Full)	**R**	-299000		
12-13	Total International filing fee (i-R)	**I**	➪	1028000	
12-14	Fee for priority document Number of priority documents requested		1		
12-15	Fee per document	**(X)**	0		
12-16	Total priority document fee:	**P**	➪		
12-17	Fee for restoration of priority rights Number of requests for restoration of priority rights	**RP**	0		
	Total amount of fees for restoration of priority rights				
12-19	**TOTAL FEES PAYABLE (T+S+I+P+RP)**		➪	1298000	
12-21	**Mode of payment**		cash		

PCT POWER OF ATTORNEY

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(This sheet is not part of and does not count as a sheet of the international application)

0-1	**PCT Power of Attorney (for an international application filed under the Patent Cooperation Treaty) (PCT Rule 90.4)**	
0-1-1	Prepared Using	PCT-SAFE Version 3.51.036.211 MT/FOP 20090101/0.20.5.15

PCT POWER OF ATTORNEY

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(This sheet is not part of and does not count as a sheet of the international application)

1	The undersigned applicant(s)	SEO, Eun Jung
1-1-1	hereby appoints (appoint) the following person	LEE, Soo Wan 1901-ho, Keungil Tower 19F, 677-25, Yeoksam-dong, Gangnam-gu, Seoul, 135-914 Republic of Korea
1-1-2	hereby appoints (appoint) the following person	CHO, Jin Tae 1901-ho, Keungil Tower 19F, 677-25, Yeoksam-dong, Gangnam-gu, Seoul, 135-914 Republic of Korea
1-1-3	hereby appoints (appoint) the following person	YUN, Jong Seop 1901-ho, Keungil Tower 19F, 677-25, Yeoksam-dong, Gangnam-gu, Seoul, 135-914 Republic of Korea
1-1-4	hereby appoints (appoint) the following person	LEE, Seong Kyu 1901-ho, Keungil Tower 19F, 677-25, Yeoksam-dong, Gangnam-gu, Seoul, 135-914 Republic of Korea
1-1-5	hereby appoints (appoint) the following person	LEE, Jae Woong 1901-ho, Keungil Tower 19F, 677-25, Yeoksam-dong, Gangnam-gu, Seoul, 135-914 Republic of Korea
1-2	as	agent
1-3	to represent the undersigned before	all the competent International Authorities
1-4	in connection with the international application identified below:	
1-4-1	Title of Invention	SLIM LED PACKAGE
1-4-2	Applicant's or agent's file reference	P08-5018
1-4-3	International application number (if already available)	
1-4-4	filed with the following Office as receiving Office	Korean Intellectual Property Office (RO/KR)
1-5	and to make or receive payments on behalf of the undersigned	

PCT POWER OF ATTORNEY

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(This sheet is not part of and does not count as a sheet of the international application)

2-1	**Signature of applicant, agent or common representative**	
2-1-1	Name (LAST, First)	SEO, Eun Jung
2-1-2	Name of signatory	
2-1-3	Capacity	
3	**Date**	17 November 2008 (17.11.2008)

명세서

슬림형 ＬＥＤ 패키지{SLIM LED PACKAGE}

기술분야

[1] 본 발명은 LED 패키지에 관한 것으로서, 더욱 상세하게는, 발광효율의 실질적인 저하 없이, 더 나아가서는, 발광 효율을 상승시키면서도, 두께는 크게 감소된 슬림형 LED 패키지에 관한 것이다.

배경기술

[2] 발광다이오드(LED; Light Emitting Diode)는 전류 인가에 의해 전자와 정공이 만나 빛을 발하는 것이다. LED 패키지는 발광다이오드 칩, 즉, LED칩이 내장된 패키지 구조물을 의미한다. 많은 종류의 LED 패키지가 알려져 있는데, 그 중에서도, 리드프레임 타입의 LED 패키지와 PCB 타입의 LED 패키지가 많이 알려져 있다. 리드프레임 타입의 LED 패키지는, 리드프레임을 지지하는 하우징의 캐비티 내에 LED칩이 위치되고, 그 하우징의 캐비티가 봉지재에 의해 충전된 구조를 포함한다. PCB 타입의 LED 패키지는, PCB 상에 LED칩이 직접 실장되고, 그 LED칩을 덮는 봉지재가 PCB 상에 형성된 구조를 포함한다.

[3] 리드프레임 타입 LED 패키지의 경우, 리드프레임을 지지하는 하우징의 두께가 너무 커서, 얇은 두께로 제작하는 것이 힘들다. 상대적으로, PCB 타입의 LED 패키지는, 하우징의 생략으로 인해, 리드프레임 타입의 LED 패키지에 비해서는 두께를 얇게 제작하는 것이 비교적 용이하다.

[4] 하지만, PCB 타입의 LED 패키지도 두께를 줄이는데 있어서 많은 제한적인 요소들을 갖고 있다. 즉, PCB 타입의 LED 패키지는, 봉지재를 고려하지 않고라도, 크기 감소에 큰 제한이 있는, PCB의 두께, LED칩의 두께 및 본딩와이어의 루프 높이(loop height)에 의해 두께가 정해지므로, 전체적으로 총 두께의 감소 및 그에 의한 슬림화가 어렵다.

[5] 또한, LED 패키지는 LED칩의 발광 동작시 발생한 에너지에 의해 그것을 덮는 봉지재에 황변 현상이 초래된다. 이러한 황변 현상은 LED 패키지의 발광 성능 및 수명을 저하시키는 주요 원인이 된다. 이러한 이유로 방열 구조를 채택한 LED 패키지가 개발되었는 바, 리드프레임 타입의 LED 패키지는 추가적인 부품인 방열슬러그를 하우징 내측에 삽입하여 몰딩하는 구조를 채택한다. 이는 부품 추가 및 복잡한 제조 공정을 요하므로 경제성이 떨어진다. PCB 타입의 LED 패키지는 LED칩이 실장되는 B-T 수지가 방열 성능이 떨어지는 재질이며, 더 나아가, 방열 구조를 추가하는 것도 어려웠다.

발명의 상세한 설명

기술적 과제

[6] 따라서, 본 발명의 기술적 과제는, 하우징 없이 투광성 봉지재가 리드프레임을 직접 지지하도록 하고, 리드프레임의 칩 실장 영역의 두께를 줄여, 전체적으로

두께가 감소된 슬림형이며, 더 나아가, 방열 성능도 좋은 슬림형의 LED 패키지를 제공하는 것이다.

기술적 해결방법

[7] 본 발명의 일 측면에 따라, 서로 이격된 제 1 및 제 2 리드프레임과, 상기 제 1 리드프레임의 상면 일 영역에서 상기 제 1 리드프레임의 두께가 타 영역에 비해 감소되어 형성된 칩 실장홈과, 상기 칩 실장홈의 바닥면에 실장된 채, 본딩와이어에 의해 상기 제 2 리드프레임과 연결되는 LED칩과, 상기 제 1 및 제 2 리드프레임을 지지하도록 그리고 상기 LED칩을 보호하도록 형성된 투광성 봉지재를 포함하는 슬림형 LED 패키지가 제공된다. 이때, 상기 LED칩의 높이는 상기 칩 실장홈의 깊이 이하인 것이 바람직하다.

[8] 바람직하게는, 상기 칩 실장홈은 상기 제 1 리드프레임의 상면 일 영역을 두께 식각하여 형성된다. 본 명세서에서, 용어 '두께 식각'은 재료, 즉, 리드프레임의 일 영역의 두께를 줄이는 목적으로 행해지는 식각을 의미하는 것이다.

[9] 바람직하게는, 상기 제 2 리드프레임의 상면 일 영역에서 상기 제 2 리드프레임의 두께가 타 영역에 비해 감소되어 형성된 본딩홈을 더 포함하며, 상기 본딩홈 내로 상기 본딩와이어의 일단부가 본딩된다. 상기 본딩홈은 상기 제 2 리드프레임의 상면 일 영역을 두께 식각하여 형성될 수 있다.

[10] 상기 제 1 리드프레임 또는 상기 제 2 리드프레임의 상면 또는 저면에 형성되어 상기 제 1 및 제 2 리드프레임과 상기 봉지재와의 접합력을 크게 하는 구멍 또는 홈들을 더 포함할 수 있다. 대안적으로, 상기 구멍 또는 홈들 대신에 상기 제 1 및 제 2 리드프레임의 상면 또는 저면에 형성된 스크래치(scratch)들이 리드프레임과 봉지재의 접합력을 증가시키는데 기여할 수 있다. 또한, 상기 LED칩의 높이는 상기 칩 실장홈의 깊이 이하인 것이 바람직하다. 상기 제 1 및 제 2 리드프레임은 서로 마주하는 대향 측면들을 갖되, 상기 대향 측면들은 서로 경사진 상태로 마주하는 직선 또는 곡선형의 경사부들을 포함하는 것이 바람직하다. 상기 대향 측면들 중 적어도 하나의 대향 측면에는 상기 제 1 리드프레임과 상기 제 2 리드프레임의 이격 거리를 넓히는 오목부가 형성된 것이 바람직하다.

[11] 또한, 상기 봉지재의 내측에는 형광체가 제공되는 것이 바람직하다. 또한, 상기 봉지재 내측에서 상기 칩 실장홈 내에 형성된 근접 수지부를 더 포함하며, 상기 형광체는 상기 근접 수지부 내에 개재된 것이 바람직하다. 대안적으로, 상기 형광체는 상기 봉지재를 구성하는 수지 내에 개재되거나, 상기 LED칩 상에 컨포멀 코팅에 의해 형성될 수도 있다.

[12] 상기 봉지재는 고상의 수지, 특히, 고상의 EMC를 이용한 트랜스퍼 몰딩에 의해 형성되는 것이 바람직하지만, 액상 수지를 이용한 인젝션 몰딩에 의해서도 형성될 수 있다.

유리한 효과

[13] 본 발명에 따르면, 두께를 감소시켜 형성된 리드프레임의 칩 실장홈에 LED칩을 실장하는 방식으로, LED칩의 두께와 리드프레임의 두께 일부가 중첩되게 하여, LED 패키지의 전체 두께를 크게 줄일 수 있고, 이에 의해, 초박형으로 슬림화된 LED 패키지를 얻을 수 있다. 또한, LED칩이 실장되는 리드프레임과 본딩와이어가 연결되는 리드프레임이 하우징 없이 바닥으로 노출되는 면적이 크게 증가되어 방열 성능이 크게 향상된 LED 패키지를 얻을 수 있다. 또한, 본딩와이어가 연결되는 리드프레임에도 두께를 감소시켜 형성된 본딩홈을 형성하고, 그 본딩홈 내에 본딩와이어가 연결되는 와이어볼을 마련하는 구조에 의해, LED 패키지의 두께 증가 원인을 더 줄이며, 이에 의하면, 보다 더 슬림화된 LED 패키지를 얻을 수 있다. 또한, 본 발명의 실시예에 따르면, 리드프레임에 형성된 구멍 또는 홈에 의해 리드프레임과 봉지재와의 접합력을 크게 해줄 수 있으며, 이는 봉지재와 리드프레임 사이에서 일어날 수 있는 계면 박리 현상을 막아준다. 또한, 상기 칩 실장홈의 내측면은 LED칩으로부터 나온 광을 상측으로 반사시키는 기존 PCB 타입의 LED 패키지에 비해 발광효율을 향상시키는데 기여한다.

도면의 간단한 설명

[14] 도 1은 본 발명의 일 실시예에 따른 슬림형 LED 패키지의 평면도.

[15] 도 2는 도 1의 I-I를 따라 취해진 단면도.

[16] 도 3 내지 도 5는 본 발명의 다양한 다른 실시예들을 설명하는 단면도들.

[17] 도 6은 본 발명의 또 다른 실시예에 따른 슬림형 LED 패키지의 평면도.

[18] 도 7은 도 6의 II-II를 따라 취해진 단면도.

발명의 실시를 위한 최선의 형태

[19] 이하, 첨부한 도면들을 참조하여 본 발명의 실시예들을 상세히 설명하기로 한다. 다음에 소개되는 실시예들은 당업자에게 본 발명의 사상이 충분히 전달될 수 있도록 하기 위해 예로서 제공되는 것이다. 따라서, 본 발명은 이하 설명되는 실시예들에 한정되지 않고 다른 형태로 구체화될 수도 있다. 그리고, 도면들에 있어서, 구성요소의 폭, 길이, 두께 등은 편의를 위하여 과장되어 표현될 수 있다. 명세서 전체에 걸쳐서 동일한 참조번호들은 동일한 구성요소들을 나타낸다.

[20] 도 1은 본 발명의 일 실시예에 따른 슬림형 LED 패키지를 도시한 평면도이며, 도 2는 도 1의 I-I를 따라 취해진 단면도이다.

[21] 도 1 및 도 2에 도시된 바와 같이, 본 실시예에 따른 슬림형 LED 패키지(1)는, 서로 이격된 제 1 및 제 2 리드프레임(12, 14)을 포함한다. 상기 제 1 리드프레임(12)에는 LED칩(2)이 실장되며, 상기 제 2 리드프레임(14)은 본딩와이어(W)에 의해 상기 LED칩(2)과 전기적으로 연결된다. 상기 본딩와이어(W)는 도시되지 않은 와이어볼(또는, 솔더링볼)에 의해 상기 제 2 리드프레임(14)에 연결된다.

[22] 상기 제 1 및 제 2 리드프레임(12, 14)은 투광성 봉지재(20)에 의해 지지된다.

상기 투광성 봉지재(20)는, 몰딩 성형에 의해 형성되는 것으로, LED칩(2)과 본딩와이어(W)를 전체적으로 덮어, 그것들을 보호하는 역할을 한다. 상기 투광성 봉지재(20)는 고상의 에폭시 수지재인 EMC(Epoxy Molding Compound)를 이용한 트랜스퍼 몰딩(transfer molding)에 의해 형성될 수 있다. 예컨대, 트랜스퍼 몰딩은 파우더형 EMC 재료를 적절한 압력으로 가압하여 태블릿(tablet) 형태로 만들고, 그 태블릿 형태의 EMC를 고온, 고압 조건으로 봉지재(20)의 형태를 한정하는 금형에 주입하는 방식으로 이루어진다.

[23] 상기 봉지재(20)는 트랜스퍼 몰딩에 의해 형성되는 것이 바람직하지만, 이에 반드시 한정되는 것은 아니며, 상기 봉지재는 액상 수지를 금형에 주입하여 봉지재를 형성하는 인젝션 몰딩에 의해 형성될 수도 있다. 상기 봉지재(20)의 재질로는 EMC 외에 에폭시 계열 또는 실리콘 계열의 수지 등 다른 종류의 투광성 수지가 이용될 수 있다.

[24] 상기 제 1 리드프레임(12)의 상면에는 칩 실장홈(121)이 형성되며, 상기 LED칩(2)은 상기 칩 실장홈(121)의 바닥면에 다이 어태칭 방식으로 실장된다. 상기 칩 실장홈(121)은, 기존 리드프레임의 반사컵 형성을 위해 이용되는 절곡 방식으로 형성되는 홈이 아니며, 제 1 리드프레임(12)의 상면 일 영역에서 타 영역에 비해 두께를 감소시켜 형성되는 홈이다. 따라서, 상기 LED칩(2)이 실장되는 부분에 국한하여 상기 제 1 리드프레임(12)의 두께가 감소되며, 이는 LED칩(2)의 실장 높이를 줄여 LED 패키지(1)의 전체 두께를 줄이는 슬림화에 기여한다. 또한, 상기 칩 실장홈(121)의 내측면은 광을 반사시키는 리플렉터(reflector)로서의 기능을 하여 LED 패키지(1)의 발광 효율 향상에도 기여할 수 있다.

[25] 바람직하게는, 상기 칩 실장홈(121)은 리드프레임의 두께를 줄일 목적으로 수행되는 두께 식각에 의해 형성된다. 이때, 상기 식각은 LED칩(2)의 실장 영역을 제외한 제 1 리드프레임(12)의 상면을 마스크로 가린 후 수행될 수 있다. 또한, 상기 칩 실장홈(121)의 깊이는 상기 제 1 리드프레임(12) 두께의 대략 1/2인 것이 바람직하나 이는 본 발명을 한정하는 것은 아니다.

[26] 또한, 상기 LED칩(2)의 높이가 상기 LED 패키지(1)의 두께 증가에 어떠한 영향도 미치지 않도록, 상기 LED칩(2)은 상기 칩 실장홈(121)의 깊이 이하의 높이를 갖는 것이 바람직하다. 달리 말하면, 상기 칩 실장홈(121)의 깊이가 상기 LED칩(2)의 높이 이상으로 정해지는 것이 바람직하다.

[27] 도 2에 잘 도시된 바와 같이, 상기 제 1 및 제 2 리드프레임(12, 14)의 저면 각각에는 홈들(122, 142)이 형성되며, 그 홈들(122, 142)에는 몰딩 성형 중에 상기 봉지재(20)의 일부가 메워진다. 이는 상기 홈(122, 142)과 상기 봉지재(20)의 일부가 맞물리는 효과 및 리드프레임(12, 14)과 봉지재(20) 사이의 접합 면적을 증가시키는 효과를 제공하여, 리드프레임에 대한 봉지재(20)의 접합력을 증가시키는데 기여한다. 상기 홈들(122, 142) 또한 상기 제 1 및 제 2 리드프레임(12, 14)의 저면 일부 영역의 두께를 감소시키는 방식으로 형성되며,

가장 바람직하게는, 전술한 것과 같은 두께 식각에 의해 형성될 수 있다. 또한, 상기 구멍 또는 홈들 대신에 상기 제 1 및 제 2 리드프레임의 상면 또는 저면에 형성된 스크래치(scratch)들이 리드프레임과 봉지재의 접합력을 증가시키는데 기여할 수 있다.

[28] 도 2를 더 참조하면, 상기 봉지재(20) 내에는 특정 파장의 광에 의해 여기되어 다른 파장의 광을 발하는 형광체(202)가 개재된다. 상기 형광체(202)는 LED칩(2)으로부터 나온 광의 파장을 변화시켜, 파장 변화를 통해 백색광을 만들어내는데 기여한다. 본 실시예에서, 상기 형광체(202)는 몰딩 재료인 수지와 혼합된 후 그 몰딩 재료에 의한 몰딩 성형 공정에 의해 상기 봉지재(20) 내에 개재될 수 있다. 예컨대, 트랜스퍼 몰딩에 의한 봉지재(20)의 형성의 경우, EMC와 형광체(202)가 미리 혼합되며, 그 혼합된 재료가 트랜스퍼 몰딩의 재료로 이용된다.

발명의 실시를 위한 형태

[29] 이하에서는, 본 발명의 여러가지 다른 실시예들에 대한 설명이 이루어진다. 그러한 실시예들을 설명함에 있어서, 앞에서 설명된 내용은 중복을 피하기 위해 생략되며, 앞선 실시예와 동일한 부재번호는 동일한 또는 유사한 구성요소를 나타낸다.

[30] 도 3을 참조하여 본 발명의 다른 한 실시예를 설명하면, 제 2 리드프레임(14)의 상면 일 영역에서 상기 제 2 리드프레임(14)의 두께를 타 영역에 비해 감소시켜 형성된 본딩홈(141)을 볼 수 있다. 상기 본딩홈(141)도 앞선 실시예의 칩 실장홈(121)과 마찬가지로 두께 식각에 의해 형성될 수 있다. 이때, 본딩와이어(W)의 일단부는 상기 본딩홈(141) 내에서 상기 제 2 리드프레임(14)과 연결된다.

[31] 도시하지는 않았지만, 상기 본딩와이어(W)가 본딩되는 일단부에는 와이어볼이 존재하는데, 상기 본딩홈(141)은 와이어볼의 높이에 따른 LED 패키지의 두께 증가를 막아준다. 또한, 와이어볼의 크기가 클수록 본딩와이어(W)가 견고하게 제 1 리드프레임(14)에 고정될 수 있는데, 상기 본딩홈(141)의 형성으로 인해, 상기 와이어볼의 크기를 증가시키는데 있어서의 제한이 감소될 수 있다.

[32] 도 4를 참조하여 본 발명의 다른 한 실시예를 설명하면, 형광체(202)가 포함된 수지(21)가 칩 실장홈(121) 내에 한정적으로 형성되어 상기 LED칩(2)을 근접 거리에서 덮고 있다. 본 명세서에서, 칩 실장홈(121) 내에 채워진 수지를 '근접 수지부'라 정의한다. 상기 근접 수지부(21)는 형광체(202)가 상기 봉지재(20) 내에서 산재하지 않고, LED칩(21) 주변에만 한정적으로 위치할 수 있도록 해준다. 이는 형광체(202)에 의한 색 변환 효율을 높여주며, 패키지 외측에서 볼 때 균일하게 색 혼합된 광을 얻을 수 있도록 해준다.

[33] 덧붙여, 상기 근접 수지부(21)는 상기 형광체가 포함되지 않은 것도 고려될 수

있다. 예컨대, 에폭시와 같은 봉지재 재질은, 열에 취약하므로, LED칩(2) 주변에서 열변 또는 황변 현상을 일으킬 수 있다. 이때, 상기 칩 실장홈(121) 내에 형성된 근접 수지부(21)를 열에 상대적으로 강한 실리콘 수지로 하면, 전술한 열변 또는 황변 현상에 의한 LED 패키지의 성능 또는 수명 저하를 크게 줄여줄 수 있다. 열변 또는 황변 현상을 방지할 목적으로, 실리콘을 근접 수지부(21)의 재료로 이용하는 경우, 형광체(202)가 포함될 수도 있지만, 그것을 생략하더라도, 열변 또는 황변의 방지 측면에서, 충분한 효과를 제공한다.

[34] 대안적으로, 상기 형광체(202)를 예를 들면, 전기 영동법에 의한 컨포멀 코팅(conformal coating) 방식으로, 상기 LED칩(2) 표면에 형성하는 것도 고려될 수 있으며, 이러한 사항을 포함하는 LED 패키지(1)의 구조는 도 5에 도시하였다.

[35] 도 6은 본 발명의 또 다른 실시예에 따른 슬림형 LED 패키지의 평면도이고, 도 7은 도 6의 II-II를 따라 취해진 단면도이다.

[36] 도 6 및 도 7을 참조하면, 봉지재(20)와 리드프레임(12, 14) 사이의 접합력을 크게 하기 위해, 상기 제 1 및 제 2 리드프레임(12, 14)은, 앞선 실시예의 홈(122, 142; 도 2 참조)들 대신에, 상기 제 1 및 제 2 리드프레임(12, 14)을 상하로 관통하는 구멍(123, 143)들을 구비한다. 상기 구멍(123, 143)들은, 프레스 가공에 의해 형성될 수 있으며, 또한, 리드프레임의 전체 두께에 대한 식각 가공에 의해 형성될 수도 있다.

[37] 도 6에 잘 도시된 바와 같이, 상기 제 1 및 제 2 리드프레임(12, 14)은, 서로 마주하는 대향 측면들에서, 서로 경사진 상태로 마주하고 있는 제 1 및 제 2 경사부(125, 145)를 포함한다. 상기 제 1 경사부(125)는 제 1 리드프레임(12)의 대향 측면에서 좌우 양측으로 벌어진 채 경사진 구조로 형성되어 있다. 또한, 상기 제 2 경사부(145)는 제 2 리드프레임(14)의 대향 측면에서 좌우 양측으로 벌어진 채 경사진 구조로 형성되어 있다. 또한 상기 제 1 및 제 2 경사부(125, 145)는 직선형이거나 곡선형일 수 있다.

[38] 상기 제 1 및 제 2 리드프레임(12, 14)의 대향 측면들 사이에는 봉지재(20)의 일부가 개재되는데, 그 개재된 봉지재(20)와 상기 대향 측면들 상에는 힘이 작용한다. 이때, 상기 경사부(125, 145)들은 힘을 경사지게 분산시켜 상기 봉지재(20)가 대향 측면상에서 파손될 위험성이 있다. 더 더욱이, 제 1 리드프레임(12)의 경사부(125)는, 그와 인접하는 봉지재(20) 일부를 감싸는 형상이므로 보다 견고하게 봉지재(20)를 잡아주는 역할을 할 수 있다. 상기 대향 측면들 사이에서의 봉지재(20) 파손은 숏트(short) 등의 위험을 야기한다는 것에 주목한다.

[39] 또한, 상기 제 1 리드프레임(12)의 대향 측면 중앙에는 상기 제 1 리드프레임(12)과 상기 제 2 리드프레임(14)의 이격 거리를 넓히는 효과를 제공하는 오목부(126)가 형성된다. 상기 오목부(126)는 본딩와이어(W)가 상기 제 1 리드프레임(12)과 상기 제 2 리드프레임(14)을 연결하는 경로 바로 아래쪽에 위치한다. 상기 오목부(126)는 본딩와이어(W)가 리드프레임(12, 14)들에 의해

잘못 접촉되는 것과, 그 잘못된 접촉에 의해 야기될 수 있는 본딩와이어(W)의 숏트를 막아준다.

[40] 전술한 슬림형 LED 패키지(1)는 하나의 큰 금속박판을 다수의 제 1 및 제 2 리드프레임(12, 14)을 갖는 형상으로 패턴 가공하고, 그 패턴 가공된 금속박판 상에 다수의 봉지재를 형성하는 몰딩 성형을 하고, 다음, 제 1 및 제 2 리드프레임(12, 14)을 지지하는 봉지재 단위로, 리드프레임들을 절단(sawing)하는 것에 의해, 다수의 개수로 제작될 수 있다. 이때, 상기 절단시 생긴 버(burr)를 제거하는 공정이 포함될 수 있다.

청구범위

[1] 서로 이격된 제 1 및 제 2 리드프레임;
상기 제 1 리드프레임의 상면 일 영역에서 상기 제 1 리드프레임의 두께가 타 영역에 비해 감소되어 형성된 칩 실장홈;
상기 칩 실장홈의 바닥면에 실장된 채, 본딩와이어에 의해 상기 제 2 리드프레임과 연결되는 LED칩; 및
상기 제 1 및 제 2 리드프레임을 지지하도록 그리고 상기 LED칩을 보호하도록 형성된 투광성 봉지재를 포함하는 슬림형 LED 패키지.

[2] 청구항 1에 있어서, 상기 칩 실장홈은 상기 제 1 리드프레임의 상면 일 영역을 두께 식각하여 형성된 것을 특징으로 하는 슬림형 LED 패키지.

[3] 청구항 1에 있어서, 상기 제 2 리드프레임의 상면 일 영역에서 상기 제 2 리드프레임의 두께가 타 영역에 비해 감소되어 형성된 본딩홈을 더 포함하며, 상기 본딩홈 내로 상기 본딩와이어의 일단부가 본딩되는 것을 특징으로 하는 슬림형 LED 패키지.

[4] 청구항 3에 있어서, 상기 본딩홈은 상기 제 2 리드프레임의 상면 일 영역을 두께 식각하여 형성된 것을 특징으로 하는 슬림형 LED 패키지.

[5] 청구항 1에 있어서, 상기 제 1 리드프레임 또는 상기 제 2 리드프레임의 상면 또는 저면에 형성되어, 상기 제 1 및 제 2 리드프레임과 상기 봉지재와의 접합력을 크게 하는 구멍 또는 홈들을 더 포함하는 것을 특징으로 하는 슬림형 LED 패키지.

[6] 청구항 1에 있어서, 상기 LED칩의 높이는 상기 칩 실장홈의 깊이 이하인 것을 특징으로 하는 슬림형 LED 패키지.

[7] 청구항 1에 있어서, 상기 제 1 및 제 2 리드프레임은 서로 마주하는 대향 측면들을 갖되, 상기 대향 측면들은 서로 경사진 상태로 마주하는 직선 또는 곡선형의 경사부들을 포함하는 것을 특징으로 하는 슬림형 LED 패키지.

[8] 청구항 7에 있어서, 상기 대향 측면들 중 적어도 하나의 대향 측면에는 상기 제 1 리드프레임과 상기 제 2 리드프레임의 이격 거리를 넓히는 오목부가 형성된 것을 특징으로 하는 슬림형 LED 패키지.

[9] 청구항 1에 있어서, 상기 봉지재의 내측에는 형광체가 제공된 것을 특징으로 하는 슬림형 LED 패키지.

[10] 청구항 9에 있어서, 상기 봉지재 내측에서 상기 칩 실장홈 내에 형성된 근접 수지부를 더 포함하며, 상기 형광체는 상기 근접 수지부 내에 개재된 것을 특징으로 하는 슬림형 LED 패키지.

[11] 청구항 9에 있어서, 상기 형광체는 상기 봉지재를 구성하는 수지 내에 개재된 것을 특징으로 하는 슬림형 LED 패키지.

[12] 청구항 9에 있어서, 상기 형광체는 상기 LED칩 상에 컨포멀 코팅에 의해

형성된 것을 특징으로 하는 슬림형 LED 패키지.

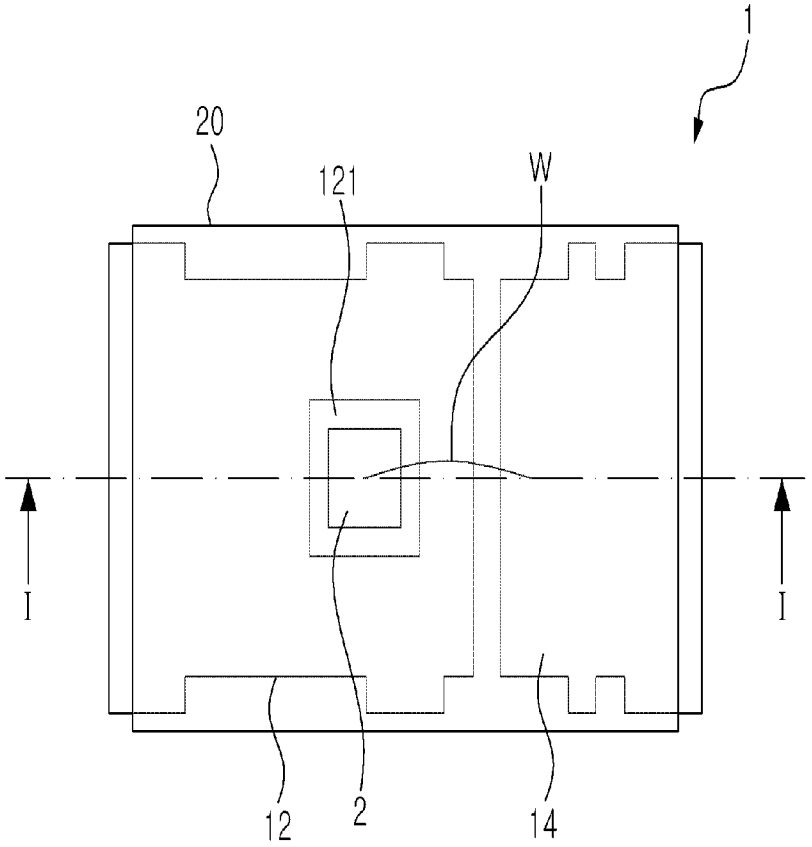
[13] 청구항 1에 있어서, 상기 봉지재는 트랜스퍼 몰딩에 의해 형성된 것을 특징으로 하는 슬림형 LED 패키지.

[14] 청구항 1에 있어서, 상기 제 1 리드프레임 또는 상기 제 2 리드프레임의 상면 또는 저면에 형성되어, 상기 제 1 및 제 2 리드프레임과 상기 봉지재와의 접합력을 크게 하는 스크래치를 더 포함하는 것을 특징으로 하는 슬림형 LED 패키지.

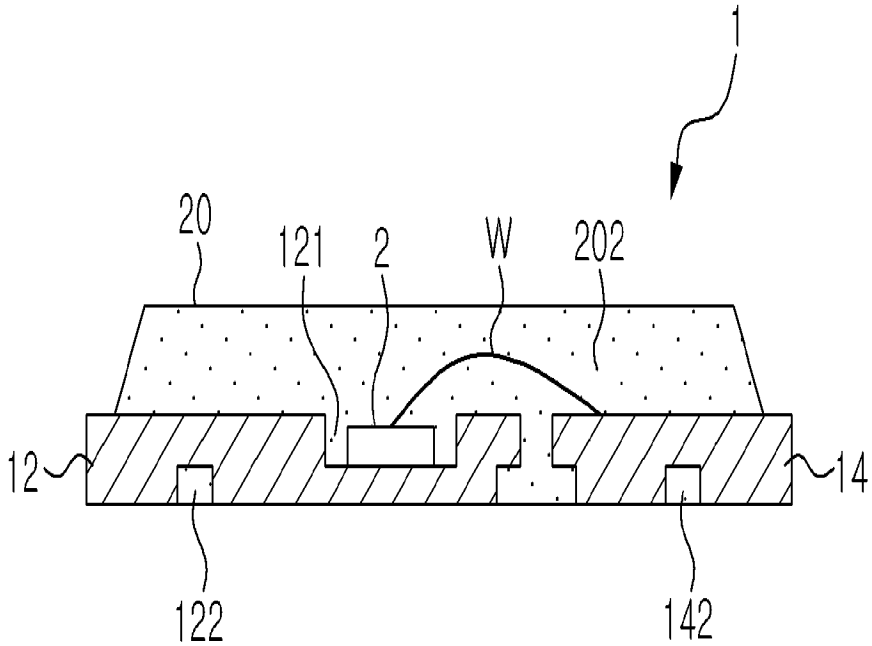
요약서

여기에서는 슬림형 LED 패키지가 개시된다. 개시된 LED 패키지는, 서로 이격된 제 1 및 제 2 리드프레임과, 상기 제 1 리드프레임의 상면 일 영역에서 상기 제 1 리드프레임의 두께가 타 영역에 비해 감소되어 형성된 칩 실장홈과, 상기 칩 실장홈의 바닥면에 실장된 채, 본딩와이어에 의해 상기 제 2 리드프레임과 연결되는 LED칩과, 상기 제 1 및 제 2 리드프레임을 지지하도록 그리고 상기 LED칩을 보호하도록 형성된 투광성 봉지재를 포함한다.

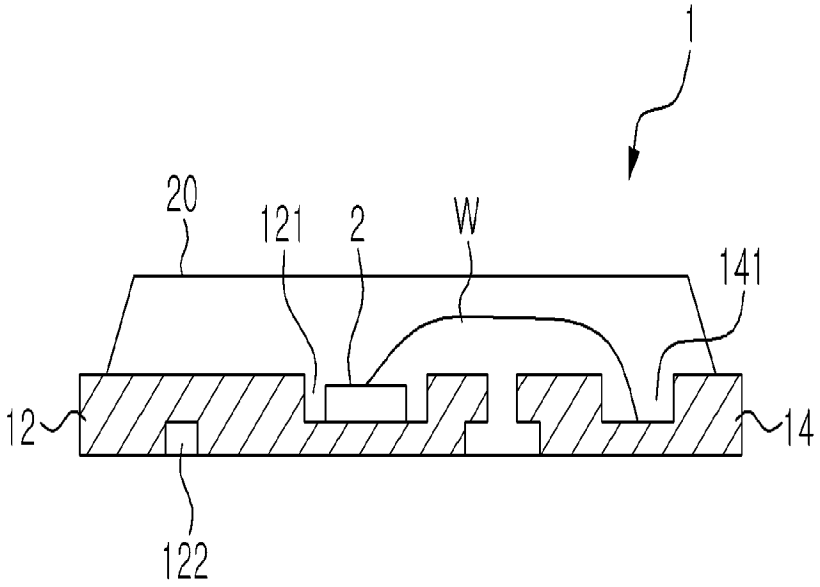
[Fig. 1]



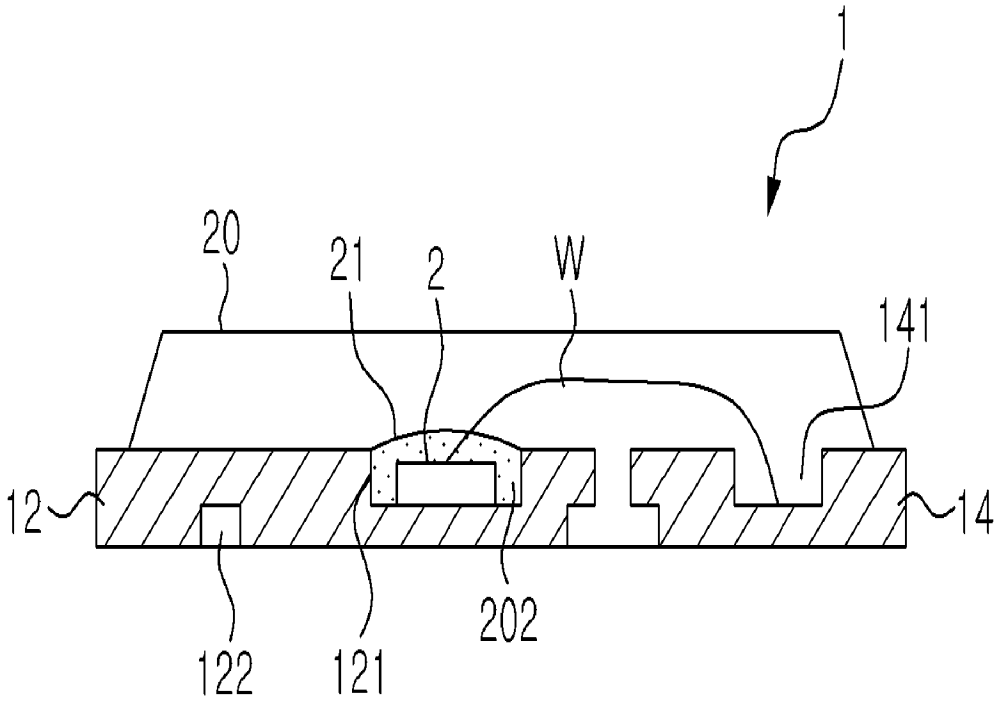
[Fig. 2]



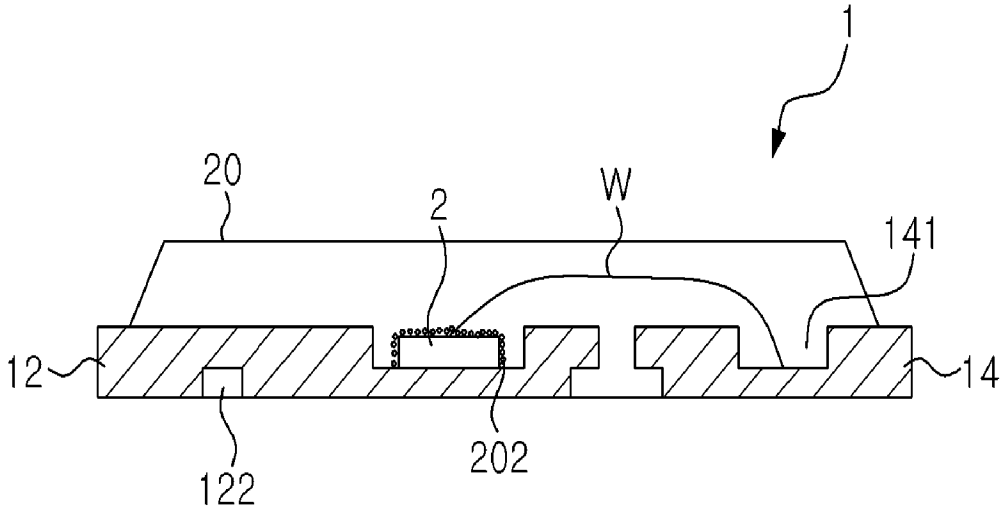
[Fig. 3]



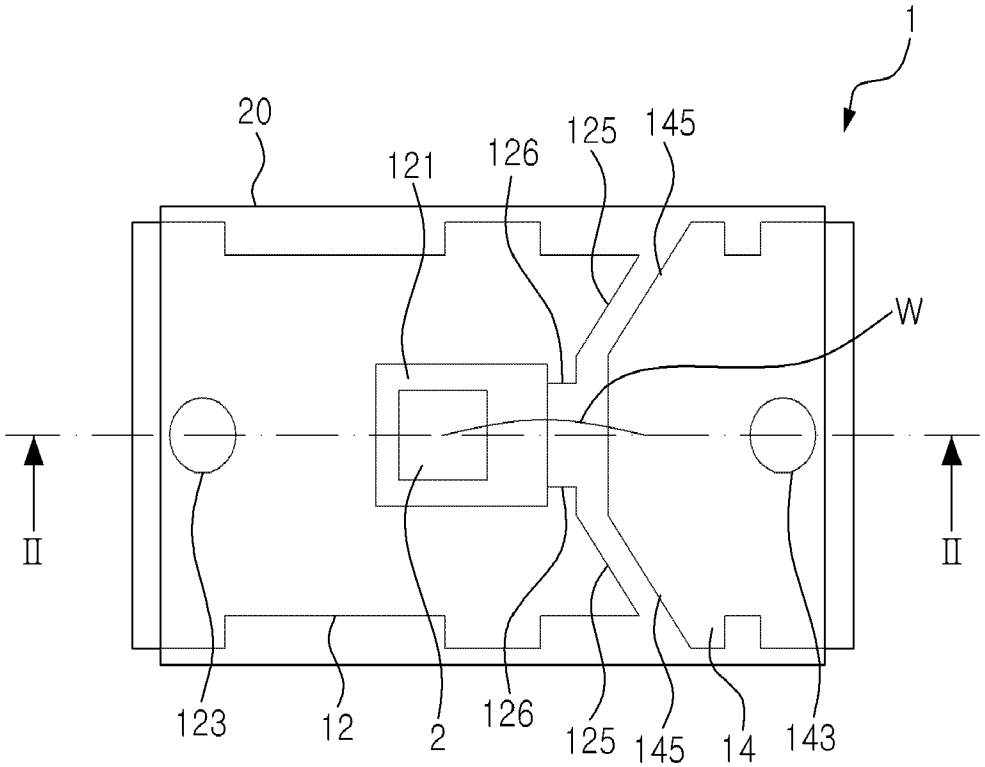
[Fig. 4]



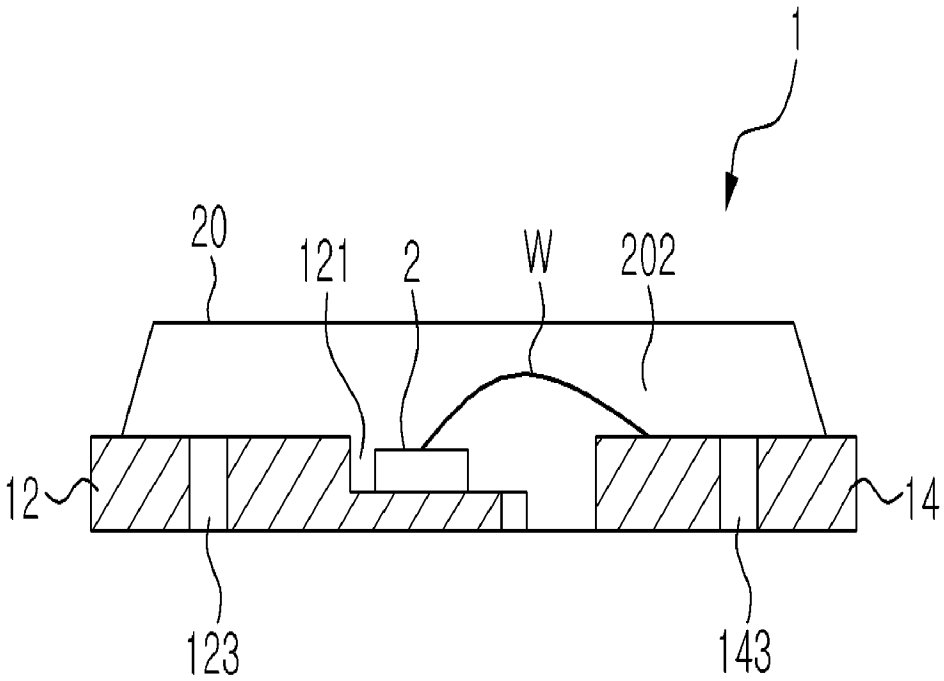
[Fig. 5]


1
20
2
W
141
12
14
122
202

[Fig. 6]


1
20
121
126
125
145
W
II
II
123
12
2
126
125
145
14
143

[Fig. 7]



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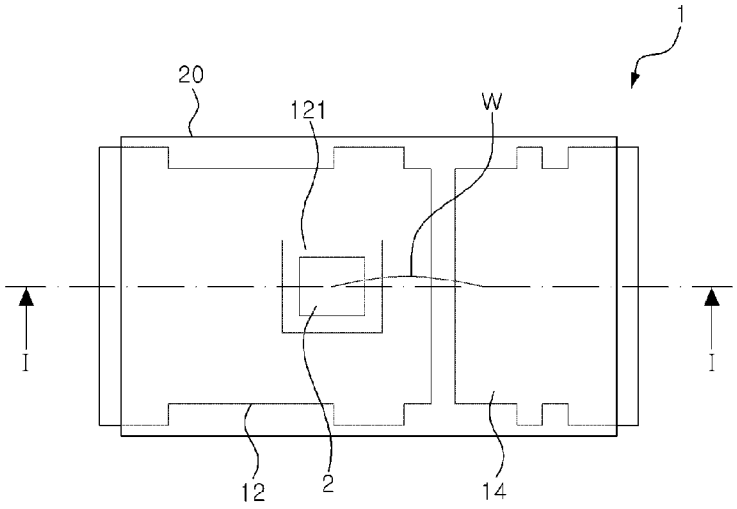
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(54) **Title:** SLIM LED PACKAGE

[Fig. 1]



(57) **Abstract:** Disclosed herein is a slim LED package. The slim LED package includes first and second lead frames separated from each other, a chip mounting recess formed on one upper surface region of the first lead frame by reducing a thickness of the one upper surface region below other upper surface regions of the first lead frame, an LED chip mounted on a bottom surface of the chip mounting recess and connected with the second lead frame via a bonding wire, and a transparent encapsulation material protecting the LED chip while supporting the first and second lead frames.

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Description

SLIM LED PACKAGE

Technical Field

[1] The present invention relates to a light emitting diode (LED) package and, more particularly, to a slim LED package that is significantly reduced in thickness without substantially reducing luminescence efficiency or while improving the luminescence efficiency.

Background Art

[2] An LED emits light through recombination of electrons and holes by application of an electric current. An LED package means a package structure in which a light emitting diode chip, that is, an LED chip, is received. Many kinds of LED packages, particularly, a lead frame type LED package and a printed circuit board (PCB) type LED package, are well known in the art. The lead frame type LED package has a structure wherein a cavity of a housing for supporting a lead frame is filled with an encapsulation material, with the LED chip positioned in the cavity of the housing. The PCB type LED package has a structure wherein the LED chip is directly mounted on a PCB and covered with the encapsulation material.

[3] For the lead frame type LED package, the housing supporting the lead frame has an excessive thickness, which makes it difficult to fabricate a thin lead frame type LED package. On the other hand, since the PCB type LED package does not include a housing, it can be more easily fabricated to have a thin structure than the lead frame type LED package.

[4] However, there are many restrictions in thickness reduction of the PCB type LED package. In other words, since the thickness of the PCB type LED package is determined by thicknesses of the PCB and LED chips, and a loop height of a bonding wire even without considering the encapsulation material, it is difficult to achieve an overall thickness reduction and slimness of the PCB type LED package.

[5] Further, the encapsulation material of the LED package, which covers the LED chip, undergoes a yellowing phenomenon by energy generated from the LED chip emitting light. Such a yellowing phenomenon is a main cause of decreased luminescence performance and lifetime of the LED package. To overcome such problems, new LED packages have been developed to have a heat sink structure. In detail, the lead frame type LED package further includes a heat dissipation slug inserted into the housing by molding. Such a structure of the lead frame type LED package requires addition of components and a complicated manufacturing process, thereby decreasing economic feasibility. For the PCB type LED package, B-T resin on which the LED chip is

mounted has a low heat dissipation performance, and it is difficult to have the heat sink structure.

Disclosure of Invention

Technical Problem

[6] Therefore, an aspect of the present invention is to provide a slim LED package that is configured to allow a transparent encapsulation material to directly support a lead frame without a housing, that has a reduced overall thickness by reducing the thickness of a chip mounting region of the lead frame, and that exhibits good heat dissipation performance.

Technical Solution

[7] In accordance with an aspect of the present invention, a slim LED package includes: first and second lead frames separated from each other; a chip mounting recess formed on one upper surface region of the first lead frame by reducing a thickness of the one upper surface region below other upper surface regions of the first lead frame; an LED chip mounted on a bottom surface of the chip mounting recess and connected with the second lead frame via a bonding wire; and a transparent encapsulation material protecting the LED chip while supporting the first and second lead frames. The LED chip may have a thickness lower than or equal to a depth of the chip mounting recess.

[8] The chip mounting recess may be formed by thickness-etching the one upper surface region of the first lead frame. Herein, the term thickness-etching refers to etching performed to reduce the thickness of a material, that is, the thickness of the one upper surface region of the lead frame.

[9] The slim LED package may further include a bonding recess formed on one upper surface region of the second lead frame by reducing a thickness of the one upper surface region of the second lead frame below other upper surface regions of the second lead frame, one end of the bonding wire being bonded into the bonding recess. The bonding recess may be formed by thickness-etching the one upper surface region of the second lead frame.

[10] The slim LED package may further include openings or grooves formed on an upper or lower surface of the first or second lead frame to increase a bonding force between the first and second lead frames and the encapsulation material. Alternatively, the slim LED package may further include scratches formed on an upper or lower surface of the first or second lead frame to increase the bonding force between the first and second lead frames and the encapsulation material. Further, the LED chip may have a lower height than the depth of the chip mounting recess. The first and second lead frames may have opposite sides facing each other and including linear or rounded slant parts facing each other in a slanted state. At least one of the opposite sides may have a

depressed part formed thereon to widen a separation between the first lead frame and the second lead frame.

[11] The slim LED package may further include a phosphor in the encapsulation material. The slim LED package may further include an adjacent resin part formed in the chip mounting recess inside the encapsulation material, and the phosphor may be disposed in the adjacent resin part. Alternatively, the phosphor may be disposed in a resin constituting the encapsulation material or may be coated on the LED chip by conformal coating.

[12] The encapsulation material may be formed by transfer molding with a solid resin, particularly, a solid EMC. Alternatively, the encapsulation material may be formed by injection molding with a liquid resin.

Advantageous Effects

[13] According to one embodiment of the present invention, the LED package is configured to mount an LED chip on a chip mounting recess, which is formed on a predetermined region of a lead frame by reducing the thickness of the predetermined region, such that the thickness of the LED chip partially overlaps the thickness of the lead frame, whereby the LED package can be significantly reduced in overall thickness, achieving an ultrathin slimness. Further, the lead frame on which the LED chip is mounted and the lead frame with which a bonding wire is connected have a significantly increased area exposed to the bottom, so that the LED package has greatly improved thermal dissipation efficiency. Additionally, a bonding recess is formed on the lead frame by reducing the thickness of a part of the lead frame with which the bonding wire is connected, and is provided therein with a wire ball to be connected with the bonding wire. As a result, a factor causing an increase in thickness of the LED package can be eliminated, so that the LED package is further slimed. Further, according to one embodiment of the present invention, openings or grooves are formed on the lead frames to increase a bonding force between the lead frames and an encapsulation material, thereby preventing separation of an interfacial surface between the encapsulation material and the lead frames. Moreover, an inside surface of the chip mounting recess serves to improve luminescence efficiency, as compared to a conventional PCB type LED package that is configured to reflect light emitted from the LED chip to an upper side.

Brief Description of Drawings

[14] The above and other aspects, features and advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

[15] Fig. 1 is a plan view of a slim LED package according to one embodiment of the

present invention;

[16] Fig. 2 is a cross-sectional view taken line I-I of Fig. 1;

[17] Figs. 3 to 5 are cross-sectional views of slim LED packages according to various embodiments of the present invention;

[18] Fig. 6 is a cross-sectional view of a slim LED package according to yet another embodiment of the present invention; and

[19] Fig. 7 is a cross-sectional view taken along line II-II of Fig. 6.

Best Mode for Carrying out the Invention

[20] Exemplary embodiments of the present invention will be described in detail with reference to the accompanying drawings. The embodiments are given by way of illustration for complete understanding of the present invention by those skilled in the art. Hence, the present invention is not limited to these embodiments and can be realized in various forms. Further, for convenience of description, width, length, and thickness of components are not drawn to scale in the drawings. Like components are indicated by like reference numerals throughout the specification.

[21] Fig. 1 is a plan view of a slim LED package according to one embodiment of the invention, and Fig. 2 is a cross-sectional view taken line I-I of Fig. 1.

[22] Referring to Figs. 1 and 2, a slim LED package 1 of this embodiment includes first and second lead frames 12, 14 separated from each other. The first lead frame 12 has an LED chip 2 mounted thereon, and the second lead frame 14 is electrically connected with the LED chip 2 via a bonding wire W. The bonding wire W is connected with the second lead frame 14 via a wire ball or soldering ball (not shown).

[23] The first and second lead frames 12, 14 are supported by a transparent encapsulation material 20. The transparent encapsulation material 20 is formed to entirely cover and protect the LED chip 2 and bonding wire W by molding. The encapsulation material 20 may be formed by transfer molding with an epoxy molding compound that is a solid epoxy resin. For example, the transfer molding is performed by compressing epoxy molding compound (EMC) powder at a proper pressure into a tablet-shape, followed by positioning and molding the tablet-shaped EMC in a mould at high temperature and pressure conditions to form the encapsulation material 20.

[24] In this embodiment, the encapsulation material 20 is formed by transfer molding, but the present invention is not limited thereto. Alternatively, the encapsulation material 20 can be formed by injection molding, in which a liquid resin is injected into a mould. The encapsulation material 20 may be formed of other kinds of transparent resins such as epoxy-based or silicone-based resins, as well as the EMC.

[25] The first lead frame 12 is formed on an upper surface thereof with a chip mounting recess 121, which has the LED chip 2 mounted on a bottom surface thereof in a die-

attachment manner. The chip mounting recess 121 is formed by reducing the thickness of one upper surface region of the first lead frame 12 below other regions of the first lead frame 12, instead of bending the lead frame to form a reflection cup as in the prior art. Accordingly, the first lead frame 12 has a decreased thickness only in the region of the first lead frame 12 where the LED chip 2 is mounted, whereby a mounting height of the LED chip 2 is lowered to contribute to slimness of the LED package 1 through an overall thickness reduction of the LED package 1. Further, an inside surface of the chip mounting groove 121 serves as a reflector for reflecting light, thereby enhancing luminescence efficiency of the LED package 1.

[26] The chip mounting recess 121 may be formed by thickness-etching, which is performed for the purpose of reducing the thickness of the lead frame. At this time, etching can be performed, with the upper surface of the first lead frame 12 except for the chip mounting region covered with a mask. Further, the chip mounting recess 121 may have a thickness of about half of the thickness of the first lead frame 12. However, it should be noted that the present invention is not limited thereto.

[27] Further, the LED chip 22 may have a thickness less than or equal to the depth of the chip mounting recess 121 to prevent the height of the LED chip 2 from affecting a thickness increase of the LED package 1. In other words, it is desirable that the depth of the chip mounting recess 121 be set greater than or equal to the height of the LED chip 2.

[28] As clearly shown in Fig. 2, the first and second lead frames 12, 14 are respectively formed on lower surfaces thereof with grooves 122, 142, which are filled with a portion of the encapsulation material 20 during the molding process. As a result, the portion of the encapsulation material 20 engages with the grooves 122, 142, and a contact area between the lead frames 12, 14 and the encapsulation material 20 increases, thereby increasing a bonding force between the encapsulation material 20 and the lead frames. The grooves 122, 142 are also formed by reducing the thickness of predetermined regions of the lower surfaces of the first and second lead frames 12, 14, and preferably by thickness-etching as described above. Alternatively, instead of forming the openings or grooves, scratches may be formed on the upper or lower surfaces of the first and second lead frames to increase the bonding force between the lead frames and the encapsulation material.

[29] Referring again to Fig. 2, the encapsulation material 20 contains a phosphor 202 that is excited by light of a predetermined wavelength and emits light of a different wavelength. The phosphor 202 contributes to generation of white light through wavelength conversion by converting light emitted from the LED chip 2. In this embodiment, the phosphor 202 is mixed with a resin prepared as a molding material and is disposed in the encapsulation material 20 by the molding process using the

molding material. For example, when forming the encapsulation material 20 by transfer molding, a mixture of EMC and the phosphor 202 is prepared and used as the material for the transfer molding.

Mode for the Invention

[30] Next, various other embodiments of the present invention will be described. In description of the embodiments, a repetitious description will be omitted, and, the same or similar elements will be denoted by the same reference numerals as those of the above description.

[31] In Fig. 3, a bonding recess 141 is shown, which is formed by reducing the thickness of one upper surface region of a second lead frame 14 below the thickness of other regions thereof. The bonding recess 141 can also be formed by the thickness-etching as in the formation of the chip mounting recess 121 of the aforementioned embodiment. At this time, one end of a bonding wire W is connected with the second lead frame 14 within the bonding recess 141.

[32] Although not shown in the drawings, a wire ball is located in the bonding recess 141 such that the one end of the bonding wire W is connected with the wire ball in the bonding recess 141, thereby preventing a thickness increase of the LED package due to the height of the wire ball. A size increase of the wire ball ensures that the bonding wire W can be more rigidly secured to the first lead frame 14. Here, the formation of the bonding wire 141 enables more freedom to increase the size of the wire ball.

[33] Referring to Fig. 4, in another embodiment of the present invention, a resin 21 containing a phosphor 202 is restrictively provided in the chip mounting recess 121 to cover the LED chip 2 in an adjacent distance. Herein, the resin filling in the chip mounting recess 121 will be defined as an adjacent resin part. The adjacent resin part 21 prevents the phosphor 202 from being scattered within the encapsulation material 20, and allows the phosphor 202 to be located around the LED chip 21. This configuration can improve color conversion efficiency by the phosphor, and can provide light consisting of uniformly mixed colors when viewed outside the package.

[34] Alternatively, the adjacent resin part 21 may not contain the phosphors. For example, the encapsulation material such as epoxy is vulnerable to heat, and can cause thermal deformation or a yellowing phenomenon around the LED chip 2. Here, when the adjacent resin part 21 formed in the chip mounting recess 121 is made of a silicone resin, which is essentially invulnerable to heat, it is possible to efficiently prevent deterioration in performance or lifetime of the LED package caused by the yellowing phenomenon. When using the silicone as a material for the adjacent resin part 21 to prevent thermal deformation or the yellowing phenomenon, the phosphors 202 can be included in the adjacent resin part 21 or omitted therefrom without any influence on

the effect of preventing thermal deformation or the yellowing phenomenon.

[35] Alternatively, the phosphors 202 can be coated on the surface of the LED chip 2 by, for example, conformal coating via electrophoresis. In this case, the LED package 1 has a configuration as illustrated in Fig. 5.

[36] Fig. 6 is a cross-sectional view of a slim LED package according to yet another embodiment of the present invention, and Fig. 7 is a cross-sectional view taken along line II-II of Fig. 6.

[37] Referring to Figs. 6 and 7, instead of the grooves 122, 142 (see Fig. 2) of the above embodiment, first and second lead frames 12, 14 of this embodiment are formed with openings 123, 143, which penetrate the first and second lead frames 12, 14 in the vertical direction, to increase the bonding force between an encapsulation material 20 and the lead frames 12, 14. The openings 123, 143 can be formed by pressing or by etching the lead frames in the thickness direction.

[38] As clearly shown in Fig. 6, the first and second lead frames 12, 14 include first and second slant parts 125, 145, which are formed on opposite sides of the lead frames facing each other in an inclined state. That is, the first slant part 125 is formed on one side of the first lead frame 12 facing the other side of the second lead frame 14 to be inclined towards right and left sides of the first lead frame 12. Further, the second slant part 145 is formed on the other side of the second lead frame 14 facing the one side of the first lead frame 12 to be inclined towards right and left sides of the second lead frame 14. The first and second slant parts 125, 145 may have a linear or curved shape.

[39] A portion of the encapsulation material 20 is interposed between the opposite sides of the first and second lead frames 12, 14 facing each other, and a force is applied to the interposed portion of the encapsulation material 20 and the opposite sides of the first and second lead frames. At this time, the slant parts 125, 145 disperse the force diagonally, thereby preventing the encapsulation material 20 from being broken on the opposite sides of the lead frames. Furthermore, since the slant part 125 of the first lead frame 12 has a shape surrounding the portion of the encapsulation material 20 adjacent thereto, it serves to more rigidly hold the encapsulation material 20. It should be noted that the breakage of the encapsulation material 20 between the opposite sides of the lead frames causes electric short or the like.

[40] Additionally, a depressed part 126 is formed at the center of the one side of the first lead frame 12 facing the other side of the second lead frame to increase a separation between the first lead frame 12 and the second lead frame 14. The depressed part 126 is located directly below a path of the bonding wire W which connects the first lead frame 12 with the second lead frame 14. The depressed part 126 prevents the bonding wire W from being erroneously brought into contact with the lead frames 12, 14, and electric short of the bonding wire W caused by the erroneous contact.

[41] To fabricate the LED packages 1 as described above, a single metal sheet is processed to have a pattern of first and second lead frames 12, 14, followed by molding an encapsulation material on the patterned metal sheet. Then, the lead frames are sawed per each encapsulation material supporting a pair of first and second lead frames 12, 14, thereby providing a plurality of LED packages. At this time, a process of removing burrs formed during sawing may be further included.

[42] Although the present invention has been described with reference to the embodiments and the accompanying drawings, the present invention is not limited to these embodiments and the drawings. It should be understood that various modifications, additions and substitutions can be made by a person having ordinary knowledge in the art without departing from the scope and spirit of the invention, as defined only by the accompanying claims.

Claims

[1] A slim LED package comprising:
first and second lead frames separated from each other;
a chip mounting recess formed on one upper surface region of the first lead frame by reducing a thickness of the one upper surface region below other upper surface regions of the first lead frame;
an LED chip mounted on a bottom surface of the chip mounting recess and connected with the second lead frame via a bonding wire; and
a transparent encapsulation material protecting the LED chip while supporting the first and second lead frames.

[2] The slim LED package according to claim 1, wherein the chip mounting recess is formed by thickness-etching the one upper surface region of the first lead frame.

[3] The slim LED package according to claim 1, further comprising:
a bonding recess formed on one upper surface region of the second lead frame by reducing a thickness of the one upper surface region of the second lead frame below other upper surface regions of the second lead frame, one end of the bonding wire being bonded into the bonding recess.

[4] The slim LED package according to claim 3, wherein the bonding recess is formed by thickness-etching the one upper surface region of the second lead frame.

[5] The slim LED package according to claim 1, further comprising:
openings or recesses formed on an upper or lower surface of the first or second lead frame to increase a bonding force between the first and second lead frames and the encapsulation material.

[6] The slim LED package according to claim 1, wherein the LED chip has a lower height than a depth of the chip mounting recess.

[7] The slim LED package according to claim 1, wherein the first and second lead frames have opposite sides facing each other and comprising linear or rounded slant parts facing each other in a slanted state.

[8] The slim LED package according to claim 7, wherein at least one of the opposite sides has a depressed part formed thereon to widen a separation between the first lead frame and the second lead frame.

[9] The slim LED package according to claim 1, further comprising:
a phosphor in the encapsulation material.

[10] The slim LED package according to claim 9, further comprising:
an adjacent resin part formed in the chip mounting recess inside the encapsulation material, and the phosphor is disposed in the adjacent resin part .

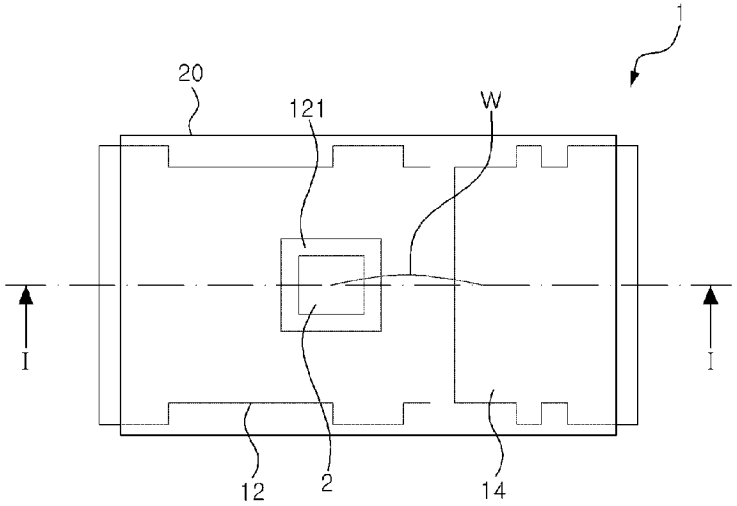
[11] The slim LED package according to claim 9, wherein the phosphor is disposed in a resin constituting the encapsulation material.

[12] The slim LED package according to claim 9, wherein the phosphor is coated on the LED chip by conformal coating.

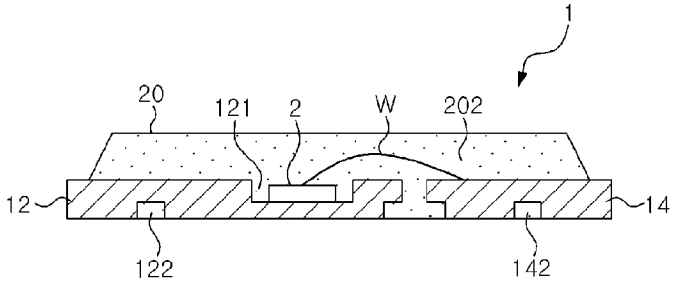
[13] The slim LED package according to claim 1, wherein the encapsulation material is formed by transfer molding.

[14] The slim LED package according to claim 1, further comprising:
scratches formed on an upper or lower surface of the first or second lead frame to increase a bonding force between the first and second lead frames and the encapsulation material.

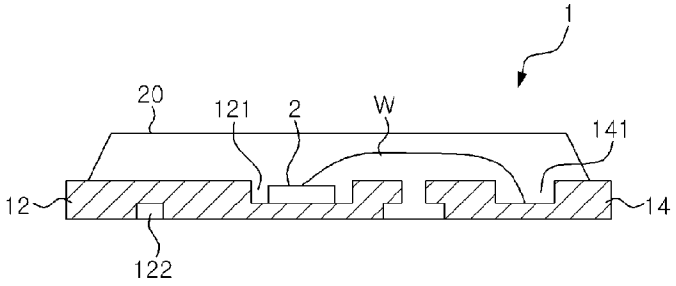
[Fig. 1]



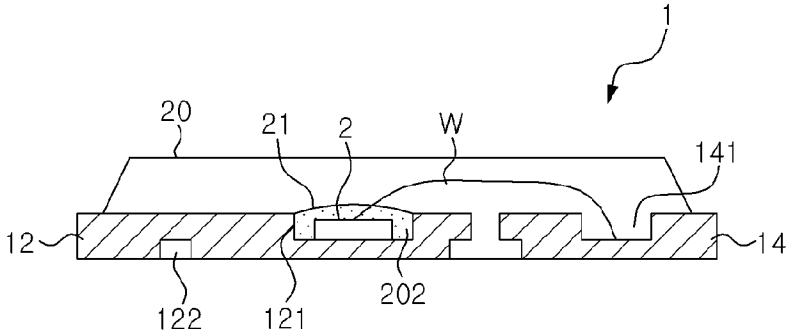
[Fig. 2]



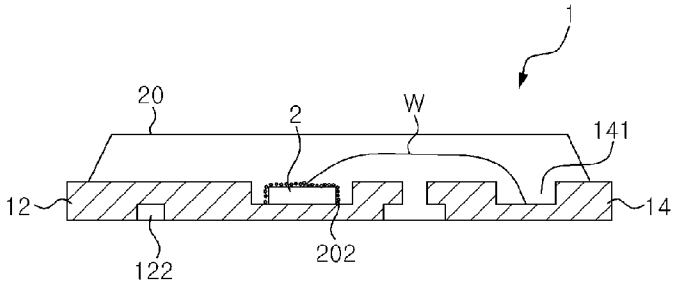
[Fig. 3]



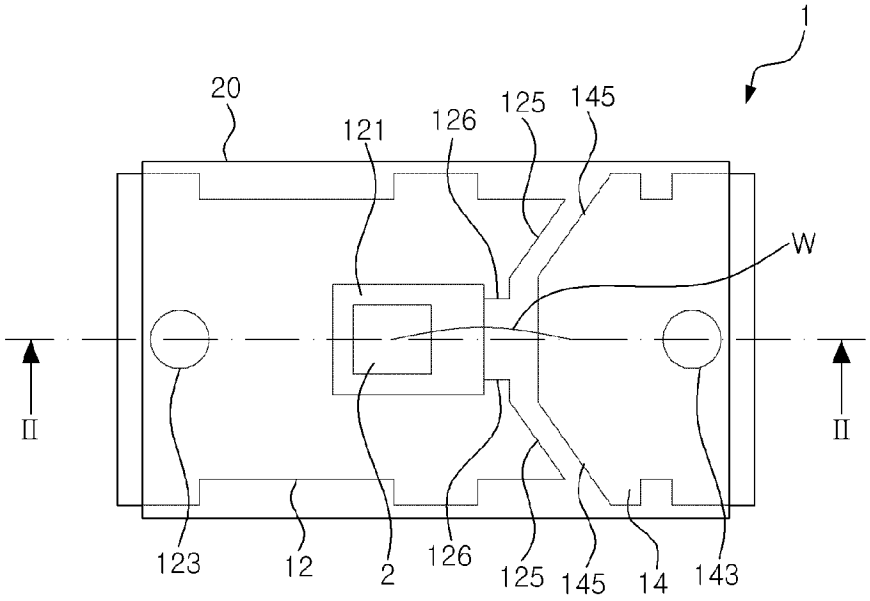
[Fig. 4]



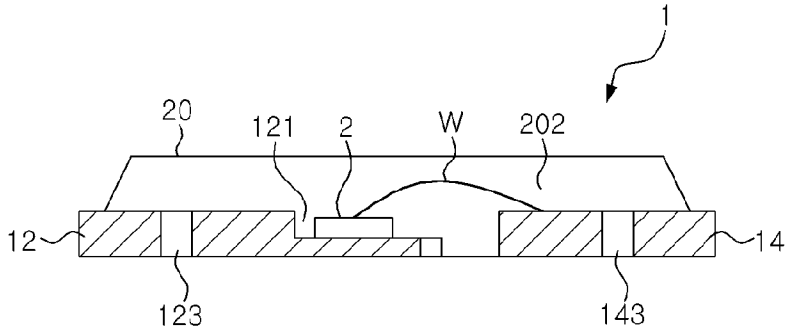
[Fig. 5]



[Fig. 6]



[Fig. 7]



특 허 협 력 조 약
(PATENT COOPERATION TREATY)

발신:수리관청

수신:
LEE Soo Wan

1901-ho, Keungil Tower 19F, 677-25, Yeoksam-dong,
Gangnam-gu, Seoul, 135-914 Republic of Korea

PCT

국제출원번호 및 국제출원일 통지서

(PCT 규칙 20.2(c))

발송일 *(일/월/년)*	2008년 12월 04일 (04.12.2008)
출원인 또는 대리인의 서류참조기호 P08-5018	중요통지사항

국제출원번호	국제출원일 *(일/월/년)*	우선일 *(일/월/년)*
PCT/KR2008/006777	**2008년 11월 18일 (18.11.2008)**	2007년 12월 03일 (03.12.2007)

출원인
SEOUL SEMICONDUCTOR CO., LTD. et al

발명의 명칭
SLIM LED PACKAGE

1. 이 국제출원은 위에 기재된 바와 같이 국제출원번호와 국제출원일이 부여되었습니다.

2. 이 국제출원의 기록원본은:

☐ _____ 자로 국제사무국에 송부되었습니다.

☐ 아래의 사유로 인하여 아직 국제사무국에 송부되지 않았으며,이 통지서의 사본은 국제사무국에 송부되었습니다*:

☐ 국가안전보장에 필요한 허가를 얻지 못했음

☐ 기타 *(이유를 상술)*:

RECEIVED
2008. 12. 10
AIP Patent & Law
No. 44467

* 국제사무국은 수리관청에 의한 기록원본의 송달을 감시하고 그 접수사실을 출원인에게 통지합니다. (서식 PCT/IB/301). 국제사무국은 우선일부터 14월이 경과할 때까지 기록원본을 수령하지 않은 때에는 출원인에게 이를 통지합니다. (규칙 22.1(c)).

수리관청명칭 및 우편주소
대한민국 특허청
(302-701) 대전광역시 서구 선사로 139,
정부대전청사
팩스번호: 82-42-472-7140

특허청장
전화번호: 82-42-481-5281

서식 PCT/RO/105 (2008년 7월)

File Copy

PATENT COOPERATION TREATY

ADVANCE E-MAIL

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF RECEIPT OF RECORD COPY

(PCT Rule 24.2(a))

To:

LEE, Soo Wan
1901-ho, Keungil Tower 19F, 677-25, Yeoksam-dong
Gangnam-gu
Seoul, 135-914
RÉPUBLIQUE DE CORÉE

Date of mailing *(day/month/year)*	**IMPORTANT NOTIFICATION**
10 December 2008 (10.12.2008)	
Applicant's or agent's file reference	International application No.
P08-5018	PCT/KR2008/006777

The applicant is hereby **notified** that the International Bureau has received the record copy of the international application as detailed below.

Name(s) of the applicant(s) and State(s) for which they are applicants:

SEOUL SEMICONDUCTOR CO., LTD. (for all designated States except US)
SEO, Eun Jung (for US)

International filing date: 18 November 2008 (18.11.2008)

Priority date(s) claimed: 03 December 2007 (03.12.2007)

Date of receipt of the record copy by the International Bureau: 08 December 2008 (08.12.2008)

List of designated Offices:

AP: BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW
EA: AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
EP: AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR
OA: BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG
National: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW

ATTENTION: The applicant should carefully check the data appearing in this notification. In case of any discrepancy between these data and the indications in the international application, the applicant should immediately inform the International Bureau. **In addition, the applicant's attention is drawn to the information contained in the Annex**, relating to:

- time limits for entry into the national phase - **see updated important information (as of April 2002)**
- requirements regarding priority documents (if applicable)

A copy of this notification is being sent to the receiving Office and to the International Searching Authority.

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. +41 22 338 70 90

Authorized officer
Lee Sun
e-mail pt12.pct@wipo.int
Telephone No. +41 22 338 74 12

INFORMATION ON ENTERING THE NATIONAL PHASE

The applicant is reminded that the **"national phase" must be entered** before each of the designated Offices indicated on the cover sheet of this notification by paying national fees and furnishing translations, as prescribed by Articles 22 and 39 and the applicable national laws. In addition, the applicant may also have to comply with **other special requirements** applicable in certain Offices. It is the **applicant's responsibility** to ensure that the necessary steps to enter the national phase are taken in a timely fashion. Most Offices do not issue reminders to applicants in connection with the entry into the national phase.

The **applicable time limit** for entering the national phase will, **subject to what is said in the following paragraph**, be **30 MONTHS** from the priority date, not only in respect of any elected Office if a demand for international preliminary examination is filed before the expiration of 19 months from the priority date (see Article 39(1)), but also in respect of any designated Office, in the absence of filing of such demand, where Article 22(1) as modified with effect from 1 April 2002 applies in respect of that designated Office. For further details, see *PCT Gazette* No. 44/2001 of 1 November 2001, pages 19926, 19932 and 19934, as well as the *PCT Newsletter*, October and November 2001 and February 2002 issues.

In practice, **time limits other than the 30-month time limit will continue to apply, for various periods of time**, in respect of certain designated or elected Offices. For **regular updates on the applicable time limits (20, 21, 30 or 31 months, or other time limit)**, Office by Office, refer to the *PCT Gazette* ("Section IV" part published on a weekly basis), to the *PCT Newsletter* (on a monthly basis) and to the relevant National Chapters in Volume II of the *PCT Applicant's Guide* (the paper version of which is updated usually twice a year and the Internet version of which is updated usually on a weekly basis). Finally, a cumulative table of all applicable time limits for entering the national phase is available from WIPO's Internet site, via links from various pages of the site, including those of the *Gazette*, *Newsletter* and *Guide*, at http://www.wipo.int/pct/en/index.html.

Information about the requirements for **filing a demand for international preliminary examination** is set out in the *PCT Applicant's Guide*, Volume I/A, Chapter IX. Note that only an applicant who is a national or resident of a PCT Contracting State which is bound by Chapter II has the right to file a demand for international preliminary examination (at present, all PCT Contracting States are bound by Chapter II).

REQUIREMENTS REGARDING PRIORITY DOCUMENTS

For applicants who have not yet complied with the requirements regarding priority documents, the following is recalled.

Where the priority of an earlier national, regional or international application is claimed, the applicant must submit a copy of the said earlier application, certified by the authority with which it was filed ("the priority document") to the receiving Office (which will transmit it to the International Bureau) or directly to the International Bureau, before the expiration of 16 months from the priority date, provided that any such priority document may still be submitted to the International Bureau before the date of international publication of the international application, in which case that document will be considered to have been received by the International Bureau on the last day of the 16-month time limit (Rule 17.1(a)).

Where the priority document is issued by the receiving Office, the applicant may, instead of submitting the priority document, request the receiving Office to prepare and transmit the priority document to the International Bureau. Such request must be made before the expiration of the 16-month time limit and may be subjected by the receiving Office to the payment of a fee (Rule 17.1(b)).

If the priority document concerned is not submitted to the International Bureau and if the request to the receiving Office to prepare and transmit the priority document has not been made (and the corresponding fee, if any, paid) within the applicable time limit indicated under the preceding paragraphs, any designated State may disregard the priority claim, provided that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances (Rule 17.1(c)).

Where several priorities are claimed, the priority date to be considered for the purposes of computing the 16-month time limit (and all other PCT time limits) is the filing date of the earliest application whose priority is claimed (Article 2(xi)(b)).

PATENT COOPERATION TREATY

ADVANCE E-MAIL

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF THE RECORDING OF A CHANGE

(PCT Rule 92*bis*.1 and Administrative Instructions, Section 422)

To:

LEE, Soo Wan
Shin-Won Building 8F
823-14 Yeoksam-dong
Gangnam-gu
Seoul 135-933
RÉPUBLIQUE DE CORÉE

Date of mailing *(day/month/year)*
17 April 2009 (17.04.2009)

Applicant's or agent's file reference
P08-5018

IMPORTANT NOTIFICATION

International application No.
PCT/KR2008/006777

International filing date *(day/month/year)*
18 November 2008 (18.11.2008)

1. The following indications appeared on record concerning:

☐ the applicant ☐ the inventor ☒ the agent ☐ the common representative

Name and Address
LEE, Soo Wan
1901-ho, Keungil Tower 19F, 677-25
Yeoksam-dong, Gangnam-gu
Seoul 135-914
Republic of Korea

State of Nationality

State of Residence

Telephone No.
82-2-3453-2626

Facsimile No.
82-2-3453-9339

E-mail address

2. The International Bureau hereby notifies the applicant that the following change has been recorded concerning:

☐ the person ☐ the name ☒ the address ☐ the nationality ☐ the residence

Name and Address
LEE, Soo Wan
Shin-Won Building 8F
823-14 Yeoksam-dong
Gangnam-gu
Seoul 135-933
Republic of Korea

State of Nationality

State of Residence

Telephone No.
82-2-3453-2626

Facsimile No.
82-2-3453-9339

E-mail address
aip@aiplaw.com
☐ Notifications by e-mail authorized

3. Further observations, if necessary:

4. A copy of this notification has been sent to:

☒ the receiving Office
☒ the International Searching Authority
☐ the Authority(ies) specified for supplementary search
☐ the International Preliminary Examining Authority
☐ the designated Offices concerned
☐ the elected Offices concerned
☐ other:

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. +41 22 338 70 90

Authorized officer
Lee Sun
e-mail pt12.pct@wipo.int
Telephone No. +41 22 338 74 12

Form PCT/IB/306 (January 2009) 1/D00UHHZA37

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION CONCERNING
AVAILABILITY OF THE PUBLICATION
OF THE INTERNATIONAL APPLICATION

To:

LEE, Soo Wan
AIP Patent & Law Offices
Shin-Won Building 8F
823-14 Yeoksam-dong
Gangnam-gu
Seoul 135-933
RÉPUBLIQUE DE CORÉE

Date of mailing *(day/month/year)* 11 June 2009 (11.06.2009)		
Applicant's or agent's file reference P08-5018	**IMPORTANT NOTICE**	
International application No. PCT/KR2008/006777	International filing date *(day/month/year)* 18 November 2008 (18.11.2008)	Priority date *(day/month/year)* 03 December 2007 (03.12.2007)
Applicant SEOUL SEMICONDUCTOR CO., LTD. et al		

The applicant is hereby **notified** that the International Bureau:

☑ has **published** the above-indicated international application on 11 June 2009 (11.06.2009) under No. WO 2009/072757

☐ has **republished** the above-indicated international application on under No. WO
For an explanation as to the reason for this republication of the international application, reference is made to INID codes (15), (48) or (88) (*as the case may be*) on the front page of the published international application.

A copy of the international application is available for viewing and downloading on WIPO's website at the following address: www.wipo.int/pctdb (in the appropriate field of the structured search, enter the PCT or WO number).

The applicant may also obtain a paper copy of the published international application from the International Bureau by sending an e-mail to patentscope@wipo.int or by submitting a written request to the contact details provided below.

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. +41 22 338 82 70

Authorized officer
Philippe Becamel

e-mail: pt12.pct@wipo.int

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

FIRST NOTICE INFORMING THE APPLICANT OF THE COMMUNICATION OF THE INTERNATIONAL APPLICATION (TO DESIGNATED OFFICES WHICH DO NOT APPLY THE 30 MONTH TIME LIMIT UNDER ARTICLE 22(1))

(PCT Rule 47.1(c))

To:

LEE, Soo Wan
AIP Patent & Law Offices
Shin-Won Building 8F
823-14 Yeoksam-dong
Gangnam-gu
Seoul 135-933
RÉPUBLIQUE DE CORÉE

Date of mailing *(day/month/year)* 09 July 2009 (09.07.2009)	
Applicant's or agent's file reference P08-5018	**IMPORTANT NOTICE**

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/KR2008/006777	18 November 2008 (18.11.2008)	03 December 2007 (03.12.2007)

Applicant
SEOUL SEMICONDUCTOR CO., LTD. et al

1. **ATTENTION**: For any designated Office(s), for which the time limit under Article 22(1), as in force from 1 April 2002 (30 months from the priority date), **does apply**, please see Form PCT/IB/308(Second and Supplementary Notice) (to be issued promptly after the expiration of 28 months from the priority date).

2. Notice is hereby given that the following designated Office(s), for which the time limit under Article 22(1), as in force from 1 April 2002, **does not apply**, has/have requested that the communication of the international application, as provided for in Article 20, be effected under Rule 93*bis*.1. The International Bureau has effected that communication on the date indicated below:
11 June 2009 (11.06.2009)

   None

   In accordance with Rule 47.1(c-*bis*)(i), those Offices will accept the present notice as conclusive evidence that the communication of the international application has duly taken place on the date of mailing indicated above and no copy of the international application is required to be furnished by the applicant to the designated Office(s).

3. The following designated Offices, for which the time limit under Article 22(1), as in force from 1 April 2002, **does not apply**, have not requested, as at the time of mailing of the present notice, that the communication of the international application be effected under Rule 93*bis*.1 :

   LU, TZ, UG

   In accordance with Rule 47.1(c-*bis*)(ii), those Offices accept the present notice as conclusive evidence that the Contracting State for which that Office acts as a designated Office does not require the furnishing, under Article 22, by the applicant of a copy of the international application.

4. **TIME LIMITS for entry into the national phase**

   For the designated Office(s) listed above, and unless a demand for international preliminary examination has been filed before the expiration of **19 months** from the priority date (see Article 39(1)), the applicable time limit for entering the national phase will, **subject to what is said in the following paragraph,** be **20 MONTHS** from the priority date.

   In practice, **time limits other than the 20-month time limit** will continue to apply, for various periods of time, in respect of certain of the designated Offices listed above. For **regular updates on the applicable time limits** (20 or 21 months, or other time limit), Office by Office, refer to the *PCT Gazette*, the *PCT Newsletter* and the *PCT Applicant's Guide*, Volume II, National Chapters, all available from WIPO's Internet site, at http://www.wipo.int/pct/en/index.html.

   It is the applicant's **sole responsibility** to monitor all these time limits.

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. +41 22 338 82 70

Authorized officer
Philippe Becamel

e-mail: pt12.pct@wipo.int

PATENT COOPERATION TREATY

ADVANCE E-MAIL

PCT

From the INTERNATIONAL BUREAU

SECOND AND SUPPLEMENTARY NOTICE INFORMING THE APPLICANT OF THE COMMUNICATION OF THE INTERNATIONAL APPLICATION (TO DESIGNATED OFFICES WHICH APPLY THE 30 MONTH TIME LIMIT UNDER ARTICLE 22(1))

(PCT Rule 47.1(c))

To:

LEE, Soo Wan
AIP Patent & Law Offices
Shin-Won Building 8F
823-14 Yeoksam-dong
Gangnam-gu
Seoul 135-933
RÉPUBLIQUE DE CORÉE

Date of mailing *(day/month/year)*
08 April 2010 (08.04.2010)

Applicant's or agent's file reference
P08-5018

IMPORTANT NOTICE

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/KR2008/006777	18 November 2008 (18.11.2008)	03 December 2007 (03.12.2007)

Applicant
SEOUL SEMICONDUCTOR CO., LTD. et al

1. **ATTENTION**: For any designated Office(s), for which the time limit under Article 22(1), as in force from 1 April 2002 (30 months from the priority date), **does not apply**, please see Form PCT/IB/308(First Notice) issued previously.

2. Notice is hereby given that the following designated Office(s), for which the time limit under Article 22(1), as in force from 1 April 2002, **does apply**, has/have requested that the communication of the international application, as provided for in Article 20, be effected under Rule 93*bis*.1. The International Bureau has effected that communication on the date indicated below:
11 June 2009 (11.06.2009)

   AU, AZ, BY, CN, CO, DZ, EP, HU, KG, KP, MD, MK, MY, MZ, NA, NG, PG, RU, SY, TM, US

   In accordance with Rule 47.1(c-*bis*)(i), those Offices will accept the present notice as conclusive evidence that the communication of the international application has duly taken place on the date of mailing indicated above and no copy of the international application is required to be furnished by the applicant to the designated Office(s).

3. The following designated Offices, for which the time limit under Article 22(1), as in force from 1 April 2002, **does apply**, have not requested, as at the time of mailing of the present notice, that the communication of the international application be effected under Rule 93*bis*.1 :

   AE, AG, AL, AM, AO, AP, AT, BA, BB, BG, BH, BR, BW, BZ, CA, CH, CR, CU, CZ, DE, DK, DM, DO, EA, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, ID, IL, IN, IS, JP, KE, KM, KN, KZ, LA, LC, LK, LR, LS, LT, LY, MA, ME, MG, MN, MW, MX, NI, NO, NZ, OA, OM, PH, PL, PT, RO, RS, SC, SD, SE, SG, SK, SL, SM, ST, SV, TJ, TN, TR, TT, UA, UZ, VC, VN, ZA, ZM, ZW

   In accordance with Rule 47.1(c-*bis*)(ii), those Offices accept the present notice as conclusive evidence that the Contracting State for which that Office acts as a designated Office does not require the furnishing, under Article 22, by the applicant of a copy of the international application.

4. **TIME LIMITS for entry into the national phase**

   For the designated or elected Office(s) listed above, the applicable time limit for entering the national phase will, **subject to what is said in the following paragraph,** be **30 MONTHS** from the priority date.

   In practice, **time limits other than the 30-month time limit** will continue to apply, for various periods of time, in respect of certain of the designated or elected Office(s) listed above. For **regular updates on the applicable time limits** (30 or 31 months, or other time limit), Office by Office, refer to the *PCT Gazette*, the *PCT Newsletter* and the *PCT Applicant's Guide*, Volume II, National Chapters, all available from WIPO's Internet site, at http://www.wipo.int/pct/en/index.html.

   It is the applicant's **sole responsibility** to monitor all these time limits.

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

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Authorized officer
Philippe Becamel

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특 허 협 력 조 약
(PATENT COOPERATION TREATY)

발신 : 국제조사기관

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PCT

국제조사보고서 및 국제조사기관의 견해서,
또는 국제조사보고서
부작성 선언서 송부 통지서
(PCT 규칙 44.1)

발송일 (일/월/년)	2009년 06월 24일 (24.06.2009)
출원인 또는 대리인 서류참조기호 P08-5018	이후의 절차에 대하여는 아래 1. 및 4. 참조
국제출원번호 **PCT/KR2008/006777**	국제출원일 (일/월/년) **2008년 11월 18일 (18.11.2008)**
출원인 **SEOUL SEMICONDUCTOR CO., LTD. et al**	

1. ☒ 국제보고서 및 국제조사기관의 견해서가 작성되어 이를 송부함을 출원인에게 통지합니다.
조약 제19조의 규정에 의한 보정서 및 설명서의 제출:
희망하는 경우 출원인은 국제출원의 청구의 범위를 보정할 수 있습니다.(조약규칙 46):
기간 보정서 제출기간은 통상 국제조사보고서 송부일부터 2월.

제출처 International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland
Faxcimile No. : +41 22 338 82 70

보다 자세한 지침에 대하여는 첨부되는 용지에 기재된 설명을 참조.

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No. 2071

2. ☐ 국제조사보고서가 작성되지 아니할 것이며 조약 제17조(2)(a)의 규정에 의한 선언서 및 국제조사기관의 견해서가 송부됨을 출원인에게 통지합니다.

3. ☐ 조약규칙 40.2의 규정에 의한 추가수수료 납부에 대한 이의신청과 관련하여 아래 사항을 출원인에게 통지합니다.
☐ 이의신청 및 이의신청에 대한 결정 통지서를 출원인이 제출한 이의신청 및 이의신청에 대한 결정 통지서의 지정관청에의 송부 신청서와 함께 국제사무국에 송부하였습니다.
☐ 이의신청에 대한 결정이 아직 이루어지지 않았습니다; 결정이 이루어지는 대로 출원인에게 통지할 것입니다.

4. **주의사항**
우선일부터 **18월** 만료직후 국제사무국은 국제출원을 공개합니다. 공개를 하지 않거나 또는 연기할 것을 희망하는 경우에는 출원인은 국제공개의 기술적 준비가 완료되기 전에 각각의 경우에 따라 조약 규칙 90bis.1 및 90bis.3의 규정에 의한 국제출원 취하서 또는 우선권주장 취하서를 국제사무국에 제출하여야 합니다.

출원인은 비공식적으로 국제조사기관의 견해서에 대한 의견서를 국제사무국에 제출할 수 있다. 국제사무국은 국제예비심사보고서가 작성되지 아니했거나 작성되지 아니할 예정인 경우 당해 의견서의 사본을 모든 지정관청에 송부할것이다. 당해 의견서는 공중에 이용가능하게 될 것이나, 우선일부터 30월 만료 전에는 그러하지 아니하다.

일부 지정관청에 대하여는 출원인이 우선일부터 30월까지 (일부관청에 대하여는 더 늦을수도 있음) 국내단계의 개시를 연기하고자 하는 경우에는 우선일부터 **19월**이내에 국제예비심사를 청구하여야 합니다; 그렇지 않은 경우 출원인은 우선일부터 20월 이내에 당해 지정관청에 대한 국내단계의 개시를 위한 규정된 절차를 밟아야 합니다.

다른 지정관청에 대하여는, 우선일부터 19월 이내에 국제예비심사를 청구하지 않더라도 30월(또는 더 늦을 수도 있음)의 기간이 적용될 것입니다.

서식 PCT/IB/301의 부속서류를 참조하기 바라며, 각 특허청마다의 적용기간에 대한 구체적인 사항은 PCT출원인 안내 제2권 국내단계 및 WIPO 인터넷 사이트를 참조하시기 바랍니다.

ISA/KR의 명칭 및 우편주소 대한민국 특허청 (302-701) 대전광역시 서구 선사로 139, 정부대전청사	특허청장
팩스 번호 82-42-472-7140	전화번호 82-42-481-5209

서식 PCT/ISA/220 (2005년 10월)

서식 PCT/ISA/220에 대한 설명(NOTE)

이 설명은 조약 제19조의 규정에 의한 보정에 관한 기본적인 안내입니다. 이는 특허협력조약, 조약규칙 및 조약시행세칙에 의한 요건에 기초하고 있습니다. 이 설명과 앞서 언급된 요건 사이에 상이점이 있는 경우에는 후자가 적용됩니다. 보다 자세한 정보에 대하여는 WIPO 발행 PCT 출원인 안내를 참조.

이 설명에서 "조약", "조약규칙" 및 "조약시행세칙"이라 함은 각각 특허협력조약, 특허협력조약에 의한 시행규칙 및 특허협력조약에 의한 시행세칙을 말합니다.

조약 제19조의 규정에 의한 보정에 관한 안내

국제조사보고서 및 국제조사기관의 견해서를 수령한 후 출원인은 1회에 한하여 국제출원의 청구의 범위를 보정할 기회를 가집니다. 국제출원의 모든 부분(청구의 범위, 명세서 및 도면)은 국제예비심사 절차 동안에 보정이 가능하므로, 예를 들어 출원인이 가보호(provisional protection)를 위하여 조약 제19조의 규정에 의한 보정이 공개 될 것을 희망하는 경우 또는 국제공개전에 청구의 범위를 보정할 다른 이유가 있는 경우를 제외하고는 통상 조약 제19조의 규정에 의한 보정을 할 필요는 없습니다. 또한 가보호는 일부국가에서만 가능함을 명심해야 합니다(*PCT 출원인안내*, 부록 B1 및 B2 참조).

조약 17(2)조의 규정에 의하여 국제조사기관이 국제조사보고서가 작성되지 않을것을 선언할 경우, 조약 19조에 근거한 청구범위의 보정을 할 수 없음을 주의하시기 바랍니다.(*PCT 출원인안내*, 296절)

국제출원의 어느 부분을 보정할 수 있는가?

조약 제19조의 규정에 의하여 청구의 범위만을 보정할 수 있습니다.

국제단계 중에는 조약 제34조의 규정에 의하여 국제예비심사기관에 대하여 청구의 범위를 보정(추가 보정도 가능)할 수 있습니다. 명세서 및 도면은 조약 제34조의 규정에 의하여 국제예비심사기관에 대하여만 보정(추가 보정도 가능)할 수 있습니다.

국내단계를 개시할 때 국제출원의 모든 부분은 조약 제28조 또는 제41조(해당하는 경우)의 규정에 의하여 보정할 수 있습니다.

기간은? 국제조사보고서 송부일부터 2월 또는 우선일부터 16월중 늦게 만료하는 날. 다만, 기간 만료후 국제공개의 기술적 준비가 완료되기 전에 국제사무국에 보정서가 수리된 경우에는, 기간내에 수리된 것으로 봅니다(조약규칙 46.1).

보정서를 제출하지 않아야 할 곳은?

보정서는 수리관청 또는 국제조사기관이 아니라 국제사무국에 제출하여야 합니다(조약규칙 46.2).

국제예비심사청구서가 제출된 경우에는 아래 참조.

방법은? 1 또는 2이상의 청구항 전부의 삭제, 1 또는 2이상의 새로운 청구항의 추가 또는 1또는 2이상의 출원시 청구항의 변경을 통하여 이루어짐.

보정에 의하여 최초 출원서의 용지와 달라지는 청구항의 각 용지에 대하여는 대체용지를 제출하여야 합니다.

대체용지상의 모든 청구항은 아라비아 숫자로 번호를 부여하여야 합니다. 청구항이 삭제된 경우에는 타 청구항에 대하여 번호를 다시 부여할 필요는 없습니다 . 번호를 다시 부여한 경우에는 항상 연속된 번호를 부여해야 합니다(조약시행세칙 205(b)).

보정은 당해 국제출원의 공개언어로 하여야 합니다.

보정서에 수반되는/수반되어야 하는 서류는?

서한(조약시행세칙 205(b)):

보정서는 서한과 함께 제출하여야 합니다.

서한은 국제출원 및 보정된 청구의 범위와 함께 공개되지 않습니다. 서한은 "조약 제19조(1)의 규정에 의한 설명서"와 혼동해서는 안됩니다(아래 "조약 제19조(1)의 규정에 의한 설명서"참조).

서한은 출원인의 선택에 따라 영어 또는 불어로 작성하여야 합니다. 다만, 국제출원언어가 영어인 경우에는 영어로, 국제출원언어가 불어인 경우에는 불어로 작성하여야 합니다.

서한에는 출원시의 청구의 범위 및 보정된 청구의 범위 사이의 상이점에 대하여 기재하여야 합니다. 특히,

(i) 청구항이 변경되었는지
(ii) 청구항이 삭제되었는지
(iii) 청구항이 새로운 것인지
(iv) 청구항이 출원시의 1 또는 2이상의 청구항을 대체하는지
(v) 청구항이 출원시의 청구항의 분할인지

여부를 국제출원의 각 청구항과 연관하여 (몇몇의 청구항에 관한 동일한 기재는 묶어서 할 수 있습니다) 기재하여야 합니다.

다음의 예는 서한에서 보정을 설명하는 방식을 나타냅니다.

1. [최초에 48개의 청구항이 있었으나 일부 청구항을 보정하여 51개의 청구항이 있는 경우]:
"Claims 1 to 29, 31, 32, 34, 35, 37 to 48 replaced by amended claims bearing the same numbers; claims 30, 33, and 36 unchanged; new claims 49 to 51 added."
2. [최초에 15개의 청구항이 있었으나 모든 청구항을 보정하여 11개의 청구항이 있는 경우];
"Claims 1 to 15 replaced by amended claims 1 to 11."
3. [최초에 14개의 청구항이 있었으나 일부 청구항을 삭제하고 새로운 청구항을 추가하는 경우];
"Claims 1 to 6 and 14 unchanged; claims 7 to 13 cancelled; new claims 15, 16 and 17 added." 또는
"Claims 7 to 13 cancelled; new claims 15, 16 and 17 added; all other claims unchanged."
4. [다양한 보정이 있는 경우]:
"Claims 1-10 unchanged; claims 11 to 13, 18 and 19 cancelled; claims 14,15 and 16 replaced by amended claim 14; claim 17 subdivided into amended claims 15, 16 and 17; new claims 20 and 21 added."

"조약 제19조(1)의 규정에 의한 설명서"(조약규칙 46.4)

보정서에는 보정내용을 설명하고 당해 보정이 명세서 및 도면(조약 제19조(1)의 규정에 의하여는 보정이 불가)에 미치는 영향을 기재한 설명서를 첨부할 수 있습니다.
설명서는 국제출원 및 보정된 청구의 범위와 함께 공개됩니다.
설명서는 당해 국제출원의 공개언어로 작성하여야 합니다.
설명서는 짧게 작성하여야 하며 영어 또는 영어로 번역한 경우 500단어를 넘지 않아야 합니다.
설명서는 최초 출원시의 청구의 범위와 보정된 청구의 범위 사이의 차이점에 대하여 기재한 서한과 혼동하여서는 아니되며 또한 설명서가 당해 서한을 대체하지도 않습니다.설명서는 별도의 용지로 제출하여야 하며, 제목을 기재하여 구별하되 그 제목은 "조약 제19조(1)의 규정에 의한 설명서"로 기재하는 것이 좋습니다.
설명서에는 국제조사보고서 또는 당해 보고서에 포함된 인용문헌의 관련성에 대하여 비방하는 의견을 기재하여서는 안됩니다. 어떤 청구항에 관련된 것으로서 국제조사보고서에 포함되어 있는 인용문헌에 대해서는 당해 청구항의 보정과 관련해서만 언급할 수 있습니다.

국제예비심사청구서가 이미 제출된 경우의 결과

조약 제19조 규정에 의한 보정서 및 설명서의 제출시에 이미 국제예비심사청구서가 제출되어 있는 경우에는 가능하면 출원인은 국제사무국에 보정서 (및 설명서)를 제출함과 동시에 국제예비심사기관에도 당해 보정서의 사본 (및 설명서의 사본) 및 해당하는 경우에는 당해 기관에서의 절차를 위한 보정서의 번역문을 제출하여야 합니다(조약규칙 55.3(a) 및 62.2 첫 번째 문장 참조). 추가적인 정보는 demand form(PCT/IPEA/401)에 대한 설명을 참조.

국제예비심사가 청구되면, 국제예비심사기관이 국제조사기관으로서의 역할을 하지 않았고 당해 예비심사기관이 국제사무국에 조약규칙 66.1bis(b)의 규정에 의한 통지를 한 경우를 제외하고, 국제조사기관의 견해서는 국제예비심사기관의 견해서로 간주된다. 국제예비심사청구가 이루어진 경우 출원인은 국제예비심사기관에 보정서(해당하는 경우)와 함께 견해서에 대한 답변을 제출할 수 있다. 견해서에 대한 답변 제출기간은 서식 PCT/ISA/220의 발송일부터 3월 또는 우선일부터 22월 중 늦게 만료하는 날 전까지이다 (조약규칙 43bis.1(c)).

국내단계 개시를 위한 국제출원의 번역문에 관한 결과

출원인은 국내단계를 개시하는 경우 조약 제19조의 규정에 의하여 보정된 청구의 범위의 번역문을 최초의 청구의 범위의 번역문과 함께 또는 당해 번역문을 대신하여 지정/선택관청에 제출하여야 하는 경우가 있다는 사실을 기억해야 합니다.

각 지정/선택관청의 요건에 관한 보다 자세한 사항은 *PCT 출원인 안내*, 제2권 참조.

* 참고사항

국제조사보고서에 인용된 문헌의 사본은 아래 특허청 영문홈페이지를 통해 국제조사보고서 발송일부터 3개월간 다운로드 할 수 있습니다.

http://www.kipo.go.kr/en/ => Patent Search => PCT-Service

ID : PCT 국제출원번호 (예: PCT/KR2008/012345)
PW : **I2QFCIB0**

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
LEE Soo Wan

AIP Patent & Law Offices Shin-Won Builduing 8F 823-14 Yeoksam-dong Gangnam-gu Seoul 135-914 Republic of Korea

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing *(day/month/year)*	**24 JUNE 2009 (24.06.2009)**
Applicant's or agent's file reference P08-5018	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/KR2008/006777	**18 NOVEMBER 2008 (18.11.2008)**	03 DECEMBER 2007 (03.12.2007)

International Patent Classification (IPC) or both national classification and IPC

H01L 33/00(2006.01)i

Applicant

SEOUL SEMICONDUCTOR CO., LTD. et al

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/KR	Date of completion of this opinion	Authorized officer
Korean Intellectual Property Office Government Complex-Daejeon, 139 Seonsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	23 JUNE 2009 (23.06.2009)	Lee, Kyu Jae Telephone No.82-42-481-8512

Form PCT/ISA/237 (cover sheet) (April 2007)

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/KR2008/006777

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of :

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into _____ , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. type of material
   - ☐ a sequence listing
   - ☐ table(s) related to the sequence listing

   b. format of material
   - ☐ on paper
   - ☐ in electronic form

   c. time of filing/furnishing
   - ☐ contained in the international application as filed.
   - ☐ filed together with the international application in electronic form.
   - ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additioanl copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/KR2008/006777

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-14	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	3-5	YES
	Claims	1-2, 6-14	NO
Industrial applicability (IA)	Claims	1-14	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: KR 2006-59575 A
D2: KR 2002-65729 A
D3: US 6603148 B1

1. Novelty and Inventive Step
1) Claims having no inventive step
(1) Concerning Independent Claim 1;

D1, which is considered to be the closest prior art to the subject matter of claim 1, discloses a semiconductor package comprising a lead frame having a chip-mount surface on which a semiconductor chip ismounted, another lead frames interconnected with the lead frame by a bonding wire, and a resin molding part covering the resultant structure, wherein the chip-mount surface is a recess surface formed by half-etch process against the lead frame. Furthermore, D2 and D3 disclose semiconductor package structures similar to that of D1. Claim 1 differs from D1-D3 in that claim 1 refers to the function of a transparent encapsulation material as to protect the LED chip while supporting the first and second lead frames. However, this is obvious to a skilled man in the art after his reviewing documents of D1-D3. Therefore, claim 1 lacks an inventive step under PCT Article 33(3).

(2)Concerning Dependent Claims 2, 6-14;

The chip mounting recess formed by thickness-etching claim 2 corresponds to a chip-mount surface formed by half-etching process of D1 and D2.
A LED chip height lower than a depth of the chip mounting recess of claim 6 is identical to features of fig.8 of D3 and is easily changed by the skilled man in the art from D1-D2.
The first and second lead frames have opposite sides facing each other of claim 7 and at least one of the opposite sides having a depressed part formed thereon of claim 8 substantially correspond to features of the representative figures of D1-D3.
A phosphor in the encapsulation material of claims 9, 11-12 is obvious to the skilled man in the art.

(Continued on the Supplemental Box)

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of :

BOX V

An adjacent resin part formed in the chip mounting recess of claim 10 corresponds to adhesives of D1 and D2 or covering material of D3.
The encapsulation material formed by transfer molding of claim 13 is obvious to the skilled man in the art.
Scratches formed on an upper or lower surface of the first or second lead frame of claim 14 substantially corresponds to small projections on the chip-mount surface of D1.
Therefore, claims 2, 6-14 lack an inventive step under PCT Article 33(3).

2) Claims 3-5 having novelty and an inventive step

The additional subject matters of claims 3-5 differ from these prior art documents in that the claims comprise a bonding recess formed on one upper surface region of the second lead frame, or openings or recesses formed on an upper or lower surface of the first or second lead frame, and they are not obvious to a person skilled in the art by the documents, taken alone or in combination. Therefore, claims 3-5 meet the requirements of PCT Article 33(2) and (3) with respect to novelty and an inventive step.

2. Industrial Applicability

Claims 1-14 are industrially applicable under PCT Article 33(4).

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
P08-5018		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/KR2008/006777	**18 NOVEMBER 2008 (18.11.2008)**	03 DECEMBER 2007 (03.12.2007)

Applicant

SEOUL SEMICONDUCTOR CO., LTD. et al

This International search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of :
      ☒ the international application in the language in which it was filed
      ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.
2. ☐ **Certain claims were found unsearchable** (See Box No. II)
3. ☐ **Unity of invention is lacking** (See Box No. III)
4. With regard to the **title,**
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:
5. With regard to the **abstract,**
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.
6. With regard to the drawings,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 1
      ☒ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figure is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2008/006777

A. CLASSIFICATION OF SUBJECT MATTER

H01L 33/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC H01L 33/00, H01L 23/12, H01L 23/04, H01L 23/48

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Utility models and applications for Utility models since 1975

Japanese Utility models and applications for Utility models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKIPASS(KIPO internal) "LED", "lead frame", "recess", "trench", "half etching", "resin"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	KR 2006-59575 A (SAMSUNG ELECTRONICS CO., LTD.) 02 June 2006	1-2, 6-14
A	See the whole document	3-5
X	KR 2002-65729 A (CHIPPAC KOREA CO., LTD.) 14 August 2002	1-2, 6-13
A	See the whole document	3-5, 14
X	US 6603148 B1 (MASASHI SANO et al.) 05 August 2003	1, 6-13
A	See the whole document	2-5, 14
A	JP 2006-179541 A (ENOMOTO CO LTD) 06 July 2006 See the whole document	1-14

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 JUNE 2009 (23.06.2009)	**24 JUNE 2009 (24.06.2009)**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office Government Complex-Daejeon, 139 Seonsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea	Lee, Kyu Jae
Facsimile No. 82-42-472-7140	Telephone No. 82-42-481-8512

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR2008/006777

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR 2006-59575 A	02.06.2006	NONE	-
KR 2002-65729 A	14.08.2002	NONE	-
US 6603148 B1	05.08.2003	CN 1233039 C	21.12.2005
		CN 1303520 A	11.07.2001
		EP 1081761 A1	07.03.2001
		JP 11-345912 A	14.12.1999
		JP 11-346006 A	14.12.1999
		JP 11-346008 A	14.12.1999
		JP 3808627 B2	16.08.2006
		JP 3908383 B2	25.04.2007
		JP 3967459 B2	29.08.2007
		KR 2001-0071309 A	28.07.2001
		TW 414924 A	11.12.2000
		US 6603148 B1	05.08.2003
		WO 99-63594 A1	09.12.1999
JP 2006-179541 A	06.07.2006	CN 1815767 A	09.08.2006
		KR 2006-71312 A	26.06.2006

【DESCRIPTION】

【Invention Title】

SLIM LED PACKAGE

【Technical Field】

The present invention relates to a light emitting diode (LED) package and, more particularly, to a slim LED package that is significantly reduced in thickness without substantially reducing luminescence efficiency or while improving the luminescence efficiency.

【Background Art】

An LED emits light through recombination of electrons and holes by application of an electric current. An LED package means a package structure in which a light emitting diode chip, that is, an LED chip, is received. Many kinds of LED packages, particularly, a lead frame type LED package and a printed circuit board (PCB) type LED package, are well known in the art. The lead frame type LED package has a structure wherein a cavity of a housing for supporting a lead frame is filled with an encapsulation material, with the LED chip positioned in the cavity of the housing. The PCB type LED package has a structure wherein the LED chip is directly mounted on a PCB and covered with the encapsulation material.

For the lead frame type LED package, the housing supporting the lead frame has an excessive thickness, which makes it difficult to fabricate a thin lead frame type LED package.

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On the other hand, since the PCB type LED package does not include a housing, it can be more easily fabricated to have a thin structure than the lead frame type LED package.

However, there are many restrictions in thickness reduction of the PCB type LED package. In other words, since the thickness of the PCB type LED package is determined by thicknesses of the PCB and LED chips, and a loop height of a bonding wire even without considering the encapsulation material, it is difficult to achieve an overall thickness reduction and slimness of the PCB type LED package.

Further, the encapsulation material of the LED package, which covers the LED chip, undergoes a yellowing phenomenon by energy generated from the LED chip emitting light. Such a yellowing phenomenon is a main cause of decreased luminescence performance and lifetime of the LED package. To overcome such problems, new LED packages have been developed to have a heat sink structure. In detail, the lead frame type LED package further includes a heat dissipation slug inserted into the housing by molding. Such a structure of the lead frame type LED package requires addition of components and a complicated manufacturing process, thereby decreasing economic feasibility. For the PCB type LED package, B-T resin on which the LED chip is mounted has a low heat dissipation performance, and it is difficult to have the heat sink structure.

【Disclosure】

【Technical Problem】

Therefore, an aspect of the present invention is to provide a slim LED package that is configured to allow a transparent encapsulation material to directly support a lead frame without

EX1012, Page 64

a housing, that has a reduced overall thickness by reducing the thickness of a chip mounting region of the lead frame, and that exhibits good heat dissipation performance.

【Technical Solution】

In accordance with an aspect of the present invention, a slim LED package includes: first and second lead frames separated from each other; a chip mounting recess formed on one upper surface region of the first lead frame by reducing a thickness of the one upper surface region below other upper surface regions of the first lead frame; an LED chip mounted on a bottom surface of the chip mounting recess and connected with the second lead frame via a bonding wire; and a transparent encapsulation material protecting the LED chip while supporting the first and second lead frames. The LED chip may have a thickness lower than or equal to a depth of the chip mounting recess.

The chip mounting recess may be formed by thickness-etching the one upper surface region of the first lead frame. Herein, the term "thickness-etching" refers to etching performed to reduce the thickness of a material, that is, the thickness of the one upper surface region of the lead frame.

The slim LED package may further include a bonding recess formed on one upper surface region of the second lead frame by reducing a thickness of the one upper surface region of the second lead frame below other upper surface regions of the second lead frame, one end of the bonding wire being bonded into the bonding recess. The bonding recess may be formed by thickness-etching the one upper surface region of the second lead frame.

The slim LED package may further include openings or grooves formed on an upper or

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lower surface of the first or second lead frame to increase a bonding force between the first and second lead frames and the encapsulation material. Alternatively, the slim LED package may further include scratches formed on an upper or lower surface of the first or second lead frame to increase the bonding force between the first and second lead frames and the encapsulation material. Further, the LED chip may have a lower height than the depth of the chip mounting recess. The first and second lead frames may have opposite sides facing each other and including linear or rounded slant parts facing each other in a slanted state. At least one of the opposite sides may have a depressed part formed thereon to widen a separation between the first lead frame and the second lead frame.

The slim LED package may further include a phosphor in the encapsulation material. The slim LED package may further include an adjacent resin part formed in the chip mounting recess inside the encapsulation material, and the phosphor may be disposed in the adjacent resin part. Alternatively, the phosphor may be disposed in a resin constituting the encapsulation material or may be coated on the LED chip by conformal coating.

The encapsulation material may be formed by transfer molding with a solid resin, particularly, a solid EMC. Alternatively, the encapsulation material may be formed by injection molding with a liquid resin.

【Advantageous Effects】

According to one embodiment of the present invention, the LED package is configured to mount an LED chip on a chip mounting recess, which is formed on a predetermined region of a lead frame by reducing the thickness of the predetermined region, such that the thickness of the

LED chip partially overlaps the thickness of the lead frame, whereby the LED package can be significantly reduced in overall thickness, achieving an ultrathin slimness. Further, the lead frame on which the LED chip is mounted and the lead frame with which a bonding wire is connected have a significantly increased area exposed to the bottom, so that the LED package has greatly improved thermal dissipation efficiency. Additionally, a bonding recess is formed on the lead frame by reducing the thickness of a part of the lead frame with which the bonding wire is connected, and is provided therein with a wire ball to be connected with the bonding wire. As a result, a factor causing an increase in thickness of the LED package can be eliminated, so that the LED package is further slimed. Further, according to one embodiment of the present invention, openings or grooves are formed on the lead frames to increase a bonding force between the lead frames and an encapsulation material, thereby preventing separation of an interfacial surface between the encapsulation material and the lead frames. Moreover, an inside surface of the chip mounting recess serves to improve luminescence efficiency, as compared to a conventional PCB type LED package that is configured to reflect light emitted from the LED chip to an upper side.

【Description of Drawings】

The above and other aspects, features and advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a plan view of a slim LED package according to one embodiment of the present invention;

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Fig. 2 is a cross-sectional view taken line I - I of Fig. 1;

Figs. 3 to 5 are cross-sectional views of slim LED packages according to various embodiments of the present invention;

Fig. 6 is a cross-sectional view of a slim LED package according to yet another embodiment of the present invention; and

Fig. 7 is a cross-sectional view taken along line II - II of Fig. 6.

【Best Mode】

Exemplary embodiments of the present invention will be described in detail with reference to the accompanying drawings. The embodiments are given by way of illustration for complete understanding of the present invention by those skilled in the art. Hence, the present invention is not limited to these embodiments and can be realized in various forms. Further, for convenience of description, width, length, and thickness of components are not drawn to scale in the drawings. Like components are indicated by like reference numerals throughout the specification.

Fig. 1 is a plan view of a slim LED package according to one embodiment of the invention, and Fig. 2 is a cross-sectional view taken line I - I of Fig. 1.

Referring to Figs. 1 and 2, a slim LED package 1 of this embodiment includes first and second lead frames 12, 14 separated from each other. The first lead frame 12 has an LED chip 2 mounted thereon, and the second lead frame 14 is electrically connected with the LED chip 2 via a bonding wire W. The bonding wire W is connected with the second lead frame 14 via a wire ball or soldering ball (not shown).

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The first and second lead frames 12, 14 are supported by a transparent encapsulation material 20. The transparent encapsulation material 20 is formed to entirely cover and protect the LED chip 2 and bonding wire W by molding. The encapsulation material 20 may be formed by transfer molding with an epoxy molding compound that is a solid epoxy resin. For example, the transfer molding is performed by compressing epoxy molding compound (EMC) powder at a proper pressure into a tablet-shape, followed by positioning and molding the tablet-shaped EMC in a mould at high temperature and pressure conditions to form the encapsulation material 20.

In this embodiment, the encapsulation material 20 is formed by transfer molding, but the present invention is not limited thereto. Alternatively, the encapsulation material 20 can be formed by injection molding, in which a liquid resin is injected into a mould. The encapsulation material 20 may be formed of other kinds of transparent resins such as epoxy-based or silicone-based resins, as well as the EMC.

The first lead frame 12 is formed on an upper surface thereof with a chip mounting recess 121, which has the LED chip 2 mounted on a bottom surface thereof in a die-attachment manner. The chip mounting recess 121 is formed by reducing the thickness of one upper surface region of the first lead frame 12 below other regions of the first lead frame 12, instead of bending the lead frame to form a reflection cup as in the prior art. Accordingly, the first lead frame 12 has a decreased thickness only in the region of the first lead frame 12 where the LED chip 2 is mounted, whereby a mounting height of the LED chip 2 is lowered to contribute to slimness of the LED package 1 through an overall thickness reduction of the LED package 1. Further, an inside surface of the chip mounting groove 121 serves as a reflector for reflecting light, thereby enhancing luminescence efficiency of the LED package 1.

The chip mounting recess 121 may be formed by thickness-etching, which is performed for the purpose of reducing the thickness of the lead frame. At this time, etching can be performed, with the upper surface of the first lead frame 12 except for the chip mounting region covered with a mask. Further, the chip mounting recess 121 may have a thickness of about half of the thickness of the first lead frame 12. However, it should be noted that the present invention is not limited thereto.

Further, the LED chip 22 may have a thickness less than or equal to the depth of the chip mounting recess 121 to prevent the height of the LED chip 2 from affecting a thickness increase of the LED package 1. In other words, it is desirable that the depth of the chip mounting recess 121 be set greater than or equal to the height of the LED chip 2.

As clearly shown in Fig. 2, the first and second lead frames 12, 14 are respectively formed on lower surfaces thereof with grooves 122, 142, which are filled with a portion of the encapsulation material 20 during the molding process. As a result, the portion of the encapsulation material 20 engages with the grooves 122, 142, and a contact area between the lead frames 12, 14 and the encapsulation material 20 increases, thereby increasing a bonding force between the encapsulation material 20 and the lead frames. The grooves 122, 142 are also formed by reducing the thickness of predetermined regions of the lower surfaces of the first and second lead frames 12, 14, and preferably by thickness-etching as described above. Alternatively, instead of forming the openings or grooves, scratches may be formed on the upper or lower surfaces of the first and second lead frames to increase the bonding force between the lead frames and the encapsulation material.

Referring again to Fig. 2, the encapsulation material 20 contains a phosphor 202 that is excited by light of a predetermined wavelength and emits light of a different wavelength. The

phosphor 202 contributes to generation of white light through wavelength conversion by converting light emitted from the LED chip 2. In this embodiment, the phosphor 202 is mixed with a resin prepared as a molding material and is disposed in the encapsulation material 20 by the molding process using the molding material. For example, when forming the encapsulation material 20 by transfer molding, a mixture of EMC and the phosphor 202 is prepared and used as the material for the transfer molding.

【Mode for Invention】

Next, various other embodiments of the present invention will be described. In description of the embodiments, a repetitious description will be omitted, and, the same or similar elements will be denoted by the same reference numerals as those of the above description.

In Fig. 3, a bonding recess 141 is shown, which is formed by reducing the thickness of one upper surface region of a second lead frame 14 below the thickness of other regions thereof. The bonding recess 141 can also be formed by the thickness-etching as in the formation of the chip mounting recess 121 of the aforementioned embodiment. At this time, one end of a bonding wire W is connected with the second lead frame 14 within the bonding recess 141.

Although not shown in the drawings, a wire ball is located in the bonding recess 141 such that the one end of the bonding wire W is connected with the wire ball in the bonding recess 141, thereby preventing a thickness increase of the LED package due to the height of the wire ball. A size increase of the wire ball ensures that the bonding wire W can be more rigidly secured to the first lead frame 14. Here, the formation of the bonding wire 141 enables more

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freedom to increase the size of the wire ball.

Referring to Fig. 4, in another embodiment of the present invention, a resin 21 containing a phosphor 202 is restrictively provided in the chip mounting recess 121 to cover the LED chip 2 in an adjacent distance. Herein, the resin filling in the chip mounting recess 121 will be defined as an "adjacent resin part." The adjacent resin part 21 prevents the phosphor 202 from being scattered within the encapsulation material 20, and allows the phosphor 202 to be located around the LED chip 21. This configuration can improve color conversion efficiency by the phosphor, and can provide light consisting of uniformly mixed colors when viewed outside the package.

Alternatively, the adjacent resin part 21 may not contain the phosphors. For example, the encapsulation material such as epoxy is vulnerable to heat, and can cause thermal deformation or a yellowing phenomenon around the LED chip 2. Here, when the adjacent resin part 21 formed in the chip mounting recess 121 is made of a silicone resin, which is essentially invulnerable to heat, it is possible to efficiently prevent deterioration in performance or lifetime of the LED package caused by the yellowing phenomenon. When using the silicone as a material for the adjacent resin part 21 to prevent thermal deformation or the yellowing phenomenon, the phosphors 202 can be included in the adjacent resin part 21 or omitted therefrom without any influence on the effect of preventing thermal deformation or the yellowing phenomenon.

Alternatively, the phosphors 202 can be coated on the surface of the LED chip 2 by, for example, conformal coating via electrophoresis. In this case, the LED package 1 has a configuration as illustrated in Fig. 5.

Fig. 6 is a cross-sectional view of a slim LED package according to yet another

embodiment of the present invention, and Fig. 7 is a cross-sectional view taken along line II - II of Fig. 6.

Referring to Figs. 6 and 7, instead of the grooves 122, 142 (see Fig. 2) of the above embodiment, first and second lead frames 12, 14 of this embodiment are formed with openings 123, 143, which penetrate the first and second lead frames 12, 14 in the vertical direction, to increase the bonding force between an encapsulation material 20 and the lead frames 12, 14. The openings 123, 143 can be formed by pressing or by etching the lead frames in the thickness direction.

As clearly shown in Fig. 6, the first and second lead frames 12, 14 include first and second slant parts 125, 145, which are formed on opposite sides of the lead frames facing each other in an inclined state. That is, the first slant part 125 is formed on one side of the first lead frame 12 facing the other side of the second lead frame 14 to be inclined towards right and left sides of the first lead frame 12. Further, the second slant part 145 is formed on the other side of the second lead frame 14 facing the one side of the first lead frame 12 to be inclined towards right and left sides of the second lead frame 14. The first and second slant parts 125, 145 may have a linear or curved shape.

A portion of the encapsulation material 20 is interposed between the opposite sides of the first and second lead frames 12, 14 facing each other, and a force is applied to the interposed portion of the encapsulation material 20 and the opposite sides of the first and second lead frames. At this time, the slant parts 125, 145 disperse the force diagonally, thereby preventing the encapsulation material 20 from being broken on the opposite sides of the lead frames. Furthermore, since the slant part 125 of the first lead frame 12 has a shape surrounding the portion of the encapsulation material 20 adjacent thereto, it serves to more rigidly hold the

encapsulation material 20. It should be noted that the breakage of the encapsulation material 20 between the opposite sides of the lead frames causes electric short or the like.

Additionally, a depressed part 126 is formed at the center of the one side of the first lead frame 12 facing the other side of the second lead frame to increase a separation between the first lead frame 12 and the second lead frame 14. The depressed part 126 is located directly below a path of the bonding wire W which connects the first lead frame 12 with the second lead frame 14. The depressed part 126 prevents the bonding wire W from being erroneously brought into contact with the lead frames 12, 14, and electric short of the bonding wire W caused by the erroneous contact.

To fabricate the LED packages 1 as described above, a single metal sheet is processed to have a pattern of first and second lead frames 12, 14, followed by molding an encapsulation material on the patterned metal sheet. Then, the lead frames are sawed per each encapsulation material supporting a pair of first and second lead frames 12, 14, thereby providing a plurality of LED packages. At this time, a process of removing burrs formed during sawing may be further included.

Although the present invention has been described with reference to the embodiments and the accompanying drawings, the present invention is not limited to these embodiments and the drawings. It should be understood that various modifications, additions and substitutions can be made by a person having ordinary knowledge in the art without departing from the scope and spirit of the invention, as defined only by the accompanying claims.

【CLAIMS】

【Claim 1】

A slim LED package comprising:

first and second lead frames separated from each other;

a chip mounting recess formed on one upper surface region of the first lead frame by reducing a thickness of the one upper surface region below other upper surface regions of the first lead frame;

an LED chip mounted on a bottom surface of the chip mounting recess and connected with the second lead frame via a bonding wire; and

a transparent encapsulation material protecting the LED chip while supporting the first and second lead frames.

【Claim 2】

The slim LED package according to claim 1, wherein the chip mounting recess is formed by thickness-etching the one upper surface region of the first lead frame.

【Claim 3】

The slim LED package according to claim 1, further comprising:

a bonding recess formed on one upper surface region of the second lead frame by

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reducing a thickness of the one upper surface region of the second lead frame below other upper surface regions of the second lead frame, one end of the bonding wire being bonded into the bonding recess.

【Claim 4】

The slim LED package according to claim 3, wherein the bonding recess is formed by thickness-etching the one upper surface region of the second lead frame.

【Claim 5】

The slim LED package according to claim 1, further comprising:

openings or recesses formed on an upper or lower surface of the first or second lead frame to increase a bonding force between the first and second lead frames and the encapsulation material.

【Claim 6】

The slim LED package according to claim 1, wherein the LED chip has a lower height than a depth of the chip mounting recess.

【Claim 7】

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The slim LED package according to claim 1, wherein the first and second lead frames have opposite sides facing each other and comprising linear or rounded slant parts facing each other in a slanted state.

【Claim 8】

The slim LED package according to claim 7, wherein at least one of the opposite sides has a depressed part formed thereon to widen a separation between the first lead frame and the second lead frame.

【Claim 9】

The slim LED package according to claim 1, further comprising:

a phosphor in the encapsulation material.

【Claim 10】

The slim LED package according to claim 9, further comprising:

an adjacent resin part formed in the chip mounting recess inside the encapsulation material, and the phosphor is disposed in the adjacent resin part .

【Claim 11】

The slim LED package according to claim 9, wherein the phosphor is disposed in a resin constituting the encapsulation material.

【Claim 12】

The slim LED package according to claim 9, wherein the phosphor is coated on the LED chip by conformal coating.

【Claim 13】

The slim LED package according to claim 1, wherein the encapsulation material is formed by transfer molding.

【Claim 14】

The slim LED package according to claim 1, further comprising:

scratches formed on an upper or lower surface of the first or second lead frame to increase a bonding force between the first and second lead frames and the encapsulation material.

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【ABSTRACT】

Disclosed herein is a slim LED package. The slim LED package includes first and second lead frames separated from each other, a chip mounting recess formed on one upper surface region of the first lead frame by reducing a thickness of the one upper surface region below other upper surface regions of the first lead frame, an LED chip mounted on a bottom surface of the chip mounting recess and connected with the second lead frame via a bonding wire, and a transparent encapsulation material protecting the LED chip while supporting the first and second lead frames.

PTO/SB/14 (11-08)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P3962US00
	Application Number	
Title of Invention	SLIM LED PACKAGE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
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All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	58027		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	SLIM LED PACKAGE		
Attorney Docket Number	P3962US00	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	5	Suggested Figure for Publication (if any)	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P3962US00
	Application Number	
Title of Invention	SLIM LED PACKAGE	

Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐	**Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
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Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	58027		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	a 371 of international	PCT/KR2008/006777	2008-11-18

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

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This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

			Remove
Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
10-2007-0124469	KR	2007-12-03	◉ Yes ○ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1

PTO/SB/14 (11-08)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P3962US00
	Application Number	
Title of Invention	SLIM LED PACKAGE	

If the Assignee is an Organization check here. ☒			
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Email Address			
Additional Assignee Data may be generated within this form by selecting the **Add** button.			

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.					
Signature	/hae-chan park/			Date (YYYY-MM-DD)	2010-06-02
First Name	Hae-Chan	Last Name	Park	Registration Number	50114

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	Docket No.: P3962US00
Eun Jung SEO	
Serial No.: To be Assigned	Group Art Unit: To be Assigned
Confirmation No.: To be Assigned	
Filed: Concurrently Herewith	Examiner: To be Assigned

For: **SLIM LED PACKAGE**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

Prior to examination on the merits, please amend the above-identified application as follows.

Amendments to the Specification begin on page 2.

Amendments to the Claims begin on page 3.

Remarks begin on page 7.

It is not believed that any extensions of time or fees for net addition of claims are required at this moment. However, if additional extension of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. §1.136(a), and any fees required therefor are hereby authorized to be charged to our Deposit Account No. 50-3698.

AMENDMENTS TO THE SPECIFICATION

Please replace the specification with the attached substitute specification. A version with markings and a clean version are attached. The claims are not included with the substitute specification.

The substitute specification does not contain new matter.

AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 1-14 as shown below.

Please **ADD** claims 15 and 16 as shown below.

1. (Currently amended) A [[slim]] light emitting diode (LED) package, comprising:

a first lead frame and a second lead frame[[s]] separated from each other;

a chip mounting recess formed ~~on one~~ in a first upper surface region of the first lead frame ~~by reducing a thickness of the one upper surface region below other upper surface regions of the first lead frame~~;

an LED chip ~~mounted~~ disposed on a bottom surface of the chip mounting recess and connected to [[with]] the second lead frame via a bonding wire; and

a transparent encapsulation material arranged on ~~protecting~~ the LED chip ~~while supporting the first and second lead frames~~,

wherein a thickness of the first lead frame in the first upper surface region is less than the thickness of the first lead frame in the other upper surface regions.

2. (Currently amended) The [[slim]] LED package ~~according to~~ of claim 1, wherein the chip mounting recess ~~is formed by thickness-etching the one upper surface region of the first lead frame~~ comprises an etched surface.

3. (Currently amended) The [[slim]] LED package ~~according to~~ of claim 1, further comprising:

a bonding recess formed ~~on one~~ in a first upper surface region of the second lead frame

~~by reducing a thickness of the one upper surface region of the second lead frame below other upper surface regions of the second lead frame~~, wherein a thickness of the second lead frame in the first upper surface region is less than the thickness of the second lead frame in the other upper surface regions, and one end of the bonding wire ~~being bonded into~~ is connected with the second lead frame in the bonding recess.

4. (Currently amended) The [[slim]] LED package ~~according to~~ of claim 3, wherein the bonding recess ~~is formed by thickness-etching the one upper surface region of the second lead frame~~ comprises an etched surface.

5. (Currently amended) The [[slim]] LED package ~~according to~~ of claim 1, further comprising:

an opening[[s]] or recess[[es]] formed [[on]] in at least one [[an]] upper surface or lower surface of the first lead frame or second lead frame ~~to increase a bonding force between the first and second lead frames and the encapsulation material~~, wherein the transparent encapsulation material is arranged in the opening or recess.

6. (Currently amended) The [[slim]] LED package ~~according to~~ of claim 1, wherein the LED chip ~~has a lower height~~ is thinner than a depth of the chip mounting recess.

7. (Currently amended) The [[slim]] LED package ~~according to~~ of claim 1, wherein the first lead frame and the second lead frame[[s]] have opposite sides facing each other, and the opposite sides each comprise ~~comprising linear or rounded~~ a slanted part~~s facing each other in a slanted state~~.

8. (Currently amended) The [[slim]] LED package ~~according to~~ of claim 7, wherein at

least one of the opposite sides comprises [[has]] a depressed part formed therein ~~thereon to~~ that widens a separation between the first lead frame and the second lead frame.

9. (Currently amended) The [[slim]] LED package ~~according to~~ of claim 1, further comprising:

a phosphor disposed in the transparent encapsulation material.

10. (Currently amended) The [[slim]] LED package ~~according to~~ of claim [[9]]1, further comprising:

a ~~an adjacent~~ resin part disposed ~~formed~~ in the chip mounting recess ~~inside the encapsulation material, and the phosphor is disposed in the adjacent resin part~~.

11. (Currently amended) The [[slim]] LED package ~~according to~~ of claim [[9]]10, wherein the phosphor is disposed in ~~a resin constituting~~ the ~~encapsulation material~~resin part.

12. (Currently amended) The [[slim]] LED package ~~according to~~ of claim 9, wherein the phosphor is ~~coated~~ disposed directly on the LED chip ~~by conformal coating~~.

13. (Currently amended) The [[slim]] LED package ~~according to~~ of claim 1, wherein the transparent encapsulation material is formed by transfer molding.

14. (Currently amended) The [[slim]] LED package ~~according to~~ of claim 1, further comprising:

a plurality of scratches formed on an upper surface or a lower surface of the first lead frame or the second lead frame to increase a bonding force between the first lead frame [[and]] or the second lead frame[[s]] and the transparent encapsulation material.

15. (New) The LED package of claim 7, wherein the first lead frame comprises a depressed part formed therein that widens a separation between the first lead frame and the second lead frame, and wherein the bonding wire is disposed directly above the depressed part.

16. (New) The LED package of claim 10, wherein the phosphor is disposed in the transparent encapsulation material.

REMARKS

Claims 1-14 have been amended, and claims 15 and 16 have been added. Claims 1-16 are now pending in this application, of which claim 1 is independent. The specification has been amended to correct informalities, as well as to add new paragraph [0022] and revise paragraph [0031] to address new Figures 8(a) and 8(b).

Applicants respectfully submit that the amendments do not add new matter to the application. Support for new paragraph [0022] and new Figures 8(a) and 8(b) may be found at least at paragraphs [0012] and [0031] of the specification. Support for new claims 15 and 16 may be found at least at in Figures 2 and 6-7 and paragraphs [0032], [0037], and [0040]-[0043].

Amendments to the Drawings

Attached is a New Drawing Sheet including new Figures 8(a) and 8(b). Support for new Figures 8(a) and 8(b) may be found at least at paragraphs [0022] and [0031] of the specification. Applicants respectfully submit that these Figures do not add new matter to the application.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,

/hae-chan park/

Hae-Chan Park
Reg. No. 50,114

Date: June 2, 2010

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Attachments: (1) Substitute Specification, marked-up copy
(2) Substitute Specification, clean copy
(3) New Drawing Sheet

~~【DESCRIPTION】~~

~~【Invention Title】~~

SLIM LED PACKAGE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is the National Stage of International Application No. PCT/KR2008/006777, filed November 18, 2008, and claims priority from and the benefit of Korean Patent Application No. 10-2007-0124469, filed on December 3, 2007, which are both hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] ~~【Technical Field】~~ FIELD OF THE INVENTION

The present invention relates to a light emitting diode (LED) package and, more particularly, to a slim LED package that is significantly reduced in thickness without substantially reducing luminescence efficiency or while improving the luminescence efficiency.

[0003] ~~【Background Art】~~ DISCUSSION OF THE BACKGROUND

[0004] An LED emits light through recombination of electrons and holes by application of an electric current. An LED package means a package structure in which a light emitting diode chip, that is, an LED chip, is received. Many kinds of LED packages, particularly, a lead frame type LED package and a printed circuit board (PCB) type LED package, are well known in the art. The lead frame type LED package has a structure wherein a cavity of a housing for supporting a lead frame is filled with an encapsulation material, with the LED chip positioned in the cavity of the housing. The PCB type LED package has a structure wherein the LED chip is

directly mounted on a PCB and covered with the encapsulation material.

[0005] For the lead frame type LED package, the housing supporting the lead frame has an excessive thickness, which makes it difficult to fabricate a thin lead frame type LED package. On the other hand, since the PCB type LED package does not include a housing, it can be more easily fabricated to have a thin structure than the lead frame type LED package.

[0006] However, there are many restrictions in thickness reduction of the PCB type LED package. In other words, since the thickness of the PCB type LED package is determined by thicknesses of the PCB and LED chips, and a loop height of a bonding wire even without considering the encapsulation material, it is difficult to achieve an overall thickness reduction and slimness of the PCB type LED package.

[0007] Further, the encapsulation material of the LED package, which covers the LED chip, undergoes a yellowing phenomenon by energy generated from the LED chip emitting light. Such a yellowing phenomenon is a main cause of decreased luminescence performance and lifetime of the LED package. To overcome such problems, new LED packages have been developed to have a heat sink structure. In detail, the lead frame type LED package further includes a heat dissipation slug inserted into the housing by molding. Such a structure of the lead frame type LED package requires addition of components and a complicated manufacturing process, thereby decreasing economic feasibility. For the PCB type LED package, B-T resin on which the LED chip is mounted has a low heat dissipation performance, and it is difficult to have the heat sink structure.

~~【Disclosure】~~

~~【Technical Problem】~~

SUMMARY OF THE INVENTION

[0008] Therefore, an aspect of the present invention is to provide a slim LED package that is configured to allow a transparent encapsulation material to directly support a lead frame without a housing, that has a reduced overall thickness by reducing the thickness of a chip mounting region of the lead frame, and that exhibits good heat dissipation performance.

~~【Technical Solution】~~

[0009] In accordance with an aspect of the present invention, a slim LED package includes: first and second lead frames separated from each other; a chip mounting recess formed on one upper surface region of the first lead frame by reducing a thickness of the one upper surface region below other upper surface regions of the first lead frame; an LED chip mounted on a bottom surface of the chip mounting recess and connected with the second lead frame via a bonding wire; and a transparent encapsulation material protecting the LED chip while supporting the first and second lead frames. The LED chip may have a thickness lower than or equal to a depth of the chip mounting recess.

[0010] The chip mounting recess may be formed by thickness-etching the one upper surface region of the first lead frame. Herein, the term "thickness-etching" refers to etching performed to reduce the thickness of a material, that is, the thickness of the one upper surface region of the lead frame.

[0011] The slim LED package may further include a bonding recess formed on one upper surface region of the second lead frame by reducing a thickness of the one upper surface region of the second lead frame below other upper surface regions of the second lead frame, one end of the bonding wire being bonded into the bonding recess. The bonding recess may be formed by

thickness-etching the one upper surface region of the second lead frame.

[0012] The slim LED package may further include openings or grooves formed on an upper or lower surface of the first or second lead frame to increase a bonding force between the first and second lead frames and the encapsulation material. Alternatively, the slim LED package may further include scratches formed on an upper or lower surface of the first or second lead frame to increase the bonding force between the first and second lead frames and the encapsulation material. Further, the LED chip may have a lower height than the depth of the chip mounting recess. The first and second lead frames may have opposite sides facing each other and including linear or rounded slant parts facing each other in a slanted state. At least one of the opposite sides may have a depressed part formed thereon to widen a separation between the first lead frame and the second lead frame.

[0013] The slim LED package may further include a phosphor in the encapsulation material. The slim LED package may further include an adjacent resin part formed in the chip mounting recess inside the encapsulation material, and the phosphor may be disposed in the adjacent resin part. Alternatively, the phosphor may be disposed in a resin constituting the encapsulation material or may be coated on the LED chip by conformal coating.

[0014] The encapsulation material may be formed by transfer molding with a solid resin, particularly, a solid EMC. Alternatively, the encapsulation material may be formed by injection molding with a liquid resin.

~~【Advantageous Effects】~~

[0015] According to one embodiment of the present invention, the LED package is configured to mount an LED chip on a chip mounting recess, which is formed on a predetermined region of a lead frame by reducing the thickness of the predetermined region,

such that the thickness of the LED chip partially overlaps the thickness of the lead frame, whereby the LED package can be significantly reduced in overall thickness, achieving an ultrathin slimness. Further, the lead frame on which the LED chip is mounted and the lead frame with which a bonding wire is connected have a significantly increased area exposed to the bottom, so that the LED package has greatly improved thermal dissipation efficiency. Additionally, a bonding recess is formed on the lead frame by reducing the thickness of a part of the lead frame with which the bonding wire is connected, and is provided therein with a wire ball to be connected with the bonding wire. As a result, a factor causing an increase in thickness of the LED package can be eliminated, so that the LED package is further ~~slimed~~ slimmed. Further, according to one embodiment of the present invention, openings or grooves are formed on the lead frames to increase a bonding force between the lead frames and an encapsulation material, thereby preventing separation of an interfacial surface between the encapsulation material and the lead frames. Moreover, an inside surface of the chip mounting recess serves to improve luminescence efficiency, as compared to a conventional PCB type LED package that is configured to reflect light emitted from the LED chip to an upper side.

BRIEF DESCRIPTION OF THE DRAWINGS ~~【Description of Drawings】~~

[0016] The above and other aspects, features and advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

[0017] Fig. 1 is a plan view of a slim LED package according to one embodiment of the present invention;

[0018] Fig. 2 is a cross-sectional view taken along line I - I of Fig. 1;

[0019] Figs. 3 to 5 are cross-sectional views of slim LED packages according to various embodiments of the present invention;

[0020] Fig. 6 is a cross-sectional view of a slim LED package according to yet another embodiment of the present invention; and

[0021] Fig. 7 is a cross-sectional view taken along line II - II of Fig. 6[[.]]; and

[0022] Figs. 8(a) and 8(b) are cross-sectional views of a slim LED package according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS ~~[Best Mode]~~

[0023] Exemplary embodiments of the present invention will be described in detail with reference to the accompanying drawings. The embodiments are given by way of illustration for complete understanding of the present invention by those skilled in the art. Hence, the present invention is not limited to these embodiments and can be realized in various forms. Further, for convenience of description, width, length, and thickness of components are not drawn to scale in the drawings. Like components are indicated by like reference numerals throughout the specification.

[0024] Fig. 1 is a plan view of a slim LED package 1 according to one embodiment of the invention, and Fig. 2 is a cross-sectional view taken line I - I of Fig. 1.

[0025] Referring to Figs. 1 and 2, a slim LED package 1 of this embodiment includes first and second lead frames 12, 14 separated from each other. The first lead frame 12 has an LED chip 2 mounted thereon, and the second lead frame 14 is electrically connected with the LED chip 2 via a bonding wire W. The bonding wire W is connected with the second lead frame 14 via a wire ball or soldering ball (not shown).

[0026] The first and second lead frames 12, 14 are supported by a transparent encapsulation material 20. The transparent encapsulation material 20 is formed to entirely cover and protect the LED chip 2 and bonding wire W by molding. The encapsulation material 20 may be formed by transfer molding with an epoxy molding compound that is a solid epoxy resin. For example, the transfer molding is performed by compressing epoxy molding compound (EMC) powder at a proper pressure into a tablet-shape, followed by positioning and molding the tablet-shaped EMC in a ~~mould~~ mold at high temperature and pressure conditions to form the encapsulation material 20.

[0027] In this embodiment, the encapsulation material 20 is formed by transfer molding, but the present invention is not limited thereto. Alternatively, the encapsulation material 20 can be formed by injection molding, in which a liquid resin is injected into a ~~mould~~ mold. The encapsulation material 20 may be formed of other kinds of transparent resins such as epoxy-based or silicone-based resins, as well as the EMC.

[0028] The first lead frame 12 is formed ~~on an upper surface thereof~~ with a chip mounting recess 121 on its upper surface, ~~which~~ and the chip mounting recess 121 has the LED chip 2 mounted on a bottom surface thereof in a die-attachment manner. The chip mounting recess 121 is formed by reducing the thickness of one upper surface region of the first lead frame 12 below other regions of the first lead frame 12, instead of bending the lead frame to form a reflection cup as in the prior art. Accordingly, the first lead frame 12 has a decreased thickness only in the region of the first lead frame 12 where the LED chip 2 is mounted, whereby a mounting height of the LED chip 2 is lowered to contribute to slimness of the LED package 1 through an overall thickness reduction of the LED package 1. Further, an inside surface of the chip mounting groove 121 serves as a reflector for reflecting light, thereby enhancing

luminescence efficiency of the LED package 1.

[0029] The chip mounting recess 121 may be formed by thickness-etching, which is performed for the purpose of reducing the thickness of the lead frame. At this time, etching can be performed, with the upper surface of the first lead frame 12 except for the chip mounting region covered with a mask. Further, the chip mounting recess 121 may have a thickness of about half of the thickness of the first lead frame 12. However, it should be noted that the present invention is not limited thereto.

[0030] Further, the LED chip [[22]] 2 may have a thickness less than or equal to the depth of the chip mounting recess 121 to prevent the height of the LED chip 2 from affecting a thickness increase of the LED package 1. In other words, it is desirable that the depth of the chip mounting recess 121 be set greater than or equal to the height of the LED chip 2.

[0031] As clearly shown in Fig. 2, the first and second lead frames 12, 14 are respectively formed on lower surfaces thereof with grooves 122, 142, which are filled with a portion of the encapsulation material 20 during the molding process. As a result, the portion of the encapsulation material 20 engages with the grooves 122, 142, and a contact area between the lead frames 12, 14 and the encapsulation material 20 increases, thereby increasing a bonding force between the encapsulation material 20 and the lead frames 12, 14. The grooves 122, 142 are also formed by reducing the thickness of predetermined regions of the lower surfaces of the first and second lead frames 12, 14, and preferably by thickness-etching as described above. Alternatively, instead of forming the openings or grooves, as shown in Fig. 8(a) and Fig. 8(b), scratches 122' and 142' may be formed on the upper or lower surfaces of the first and second lead frames 12, 14, respectively, to increase the bonding force between the lead frames 12, 14 and the encapsulation material 20.

[0032] Referring again to Fig. 2, the encapsulation material 20 contains a phosphor 202 that is excited by light of a predetermined wavelength and emits light of a different wavelength. The phosphor 202 contributes to generation of white light through wavelength conversion by converting light emitted from the LED chip 2. In this embodiment, the phosphor 202 is mixed with a resin prepared as a molding material and is disposed in the encapsulation material 20 by the molding process using the molding material. For example, when forming the encapsulation material 20 by transfer molding, a mixture of EMC and the phosphor 202 is prepared and used as the material for the transfer molding.

~~【Mode for Invention】~~

[0033] Next, various other embodiments of the present invention will be described. In description of the embodiments, a repetitious description will be omitted, and, the same or similar elements will be denoted by the same reference numerals as those of the above description.

[0034] In Fig. 3, a bonding recess 141 is shown, which is formed by reducing the thickness of one upper surface region of a second lead frame 14 below the thickness of other regions thereof. The bonding recess 141 can also be formed by the thickness-etching as in the formation of the chip mounting recess 121 of the aforementioned embodiment. At this time, one end of a bonding wire W is connected with the second lead frame 14 within the bonding recess 141.

[0035] Although not shown in the drawings, a wire ball is located in the bonding recess 141 such that the one end of the bonding wire W is connected with the wire ball in the bonding recess 141, thereby preventing a thickness increase of the LED package due to the height of the wire ball. A size increase of the wire ball ensures that the bonding wire W can be more rigidly

secured to the ~~first~~ second lead frame 14. Here, the formation of the bonding ~~wire~~ recess 141 enables more freedom to increase the size of the wire ball.

[0036] Referring to Fig. 4, in another embodiment of the present invention, a resin 21 containing a phosphor 202 is restrictively provided in the chip mounting recess 121 to cover the LED chip 2 in an adjacent distance. Herein, the resin 21 filling in the chip mounting recess 121 will be defined as an "adjacent resin part." The adjacent resin part 21 prevents the phosphor 202 from being scattered within the encapsulation material 20, and allows the phosphor 202 to be located around the LED chip [[21]] 2. This configuration can improve color conversion efficiency by the phosphor 202, and can provide light consisting of uniformly mixed colors when viewed outside the LED package 1.

[0037] Alternatively, the adjacent resin part 21 may not contain the phosphor[[s]] 202. For example, the encapsulation material such as epoxy is vulnerable to heat, and can cause thermal deformation or a yellowing phenomenon around the LED chip 2. Here, when the adjacent resin part 21 formed in the chip mounting recess 121 is made of a silicone resin, which is essentially invulnerable to heat, it is possible to efficiently prevent deterioration in performance or lifetime of the LED package 1 caused by the yellowing phenomenon. When using the silicone as a material for the adjacent resin part 21 to prevent thermal deformation or the yellowing phenomenon, the phosphor[[s]] 202 can be included in the adjacent resin part 21 or omitted therefrom without any influence on the effect of preventing thermal deformation or the yellowing phenomenon.

[0038] Alternatively, the phosphor[[s]] 202 can be coated on the surface of the LED chip 2 by, for example, conformal coating via electrophoresis. In this case, the LED package 1 has a configuration as illustrated in Fig. 5.

[0039] Fig. 6 is a cross-sectional view of a slim LED package 1 according to yet another embodiment of the present invention, and Fig. 7 is a cross-sectional view taken along line II - II of Fig. 6.

[0040] Referring to Figs. 6 and 7, instead of the grooves 122, 142 (see Fig. 2) of the above embodiment, first and second lead frames 12, 14 of this embodiment are formed with openings 123, 143, which penetrate the first and second lead frames 12, 14 in the vertical direction, to increase the bonding force between an encapsulation material 20 and the lead frames 12, 14. The openings 123, 143 can be formed by pressing or by etching the lead frames 12, 14 in the thickness direction.

[0041] As clearly shown in Fig. 6, the first and second lead frames 12, 14 include first and second slant parts 125, 145, which are formed on opposite sides of the lead frames 12, 14 facing each other in an inclined state. That is, the first slant part 125 is formed on one side of the first lead frame 12 facing the other side of the second lead frame 14 to be inclined towards right and left sides of the first lead frame 12. Further, the second slant part 145 is formed on the other side of the second lead frame 14 facing the one side of the first lead frame 12 to be inclined towards right and left sides of the second lead frame 14. The first and second slant parts 125, 145 may have a linear or curved shape.

[0042] A portion of the encapsulation material 20 is interposed between the opposite sides of the first and second lead frames 12, 14 facing each other, and a force is applied to the interposed portion of the encapsulation material 20 and the opposite sides of the first and second lead frames 12, 14. At this time, the slant parts 125, 145 disperse the force diagonally, thereby preventing the encapsulation material 20 from being broken on the opposite sides of the lead frames 12, 14. Furthermore, since the slant part 125 of the first lead frame 12 has a shape

surrounding the portion of the encapsulation material 20 adjacent thereto, it serves to more rigidly hold the encapsulation material 20. It should be noted that the breakage of the encapsulation material 20 between the opposite sides of the lead frames 12, 14 may cause[[s]] electric shorts or the like.

[0043] Additionally, a depressed part 126 is formed at the center of the one side of the first lead frame 12 facing the other side of the second lead frame 14 to increase a separation between the first lead frame 12 and the second lead frame 14. The depressed part 126 is located directly below a path of the bonding wire W which connects the first lead frame 12 with the second lead frame 14. The depressed part 126 prevents the bonding wire W from being erroneously brought into contact with the lead frames 12, 14, and an electric short of the bonding wire W caused by the erroneous contact.

[0044] To fabricate the LED packages 1 as described above, a single metal sheet is processed to have a pattern of first and second lead frames 12, 14, followed by molding an encapsulation material 20 on the patterned metal sheet. Then, the lead frames 12, 14 are ~~sawed~~ sawn per each encapsulation material 20 supporting a pair of first and second lead frames 12, 14, thereby providing a plurality of LED packages 1. At this time, a process of removing burrs formed during sawing may be further included.

[0045] Although the present invention has been described with reference to the embodiments and the accompanying drawings, the present invention is not limited to these embodiments and the drawings. It should be understood that various modifications, additions and substitutions can be made by a person having ordinary knowledge in the art without departing from the scope and spirit of the invention, as defined only by the accompanying claims.

SLIM LED PACKAGE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is the National Stage of International Application No. PCT/KR2008/006777, filed November 18, 2008, and claims priority from and the benefit of Korean Patent Application No. 10-2007-0124469, filed on December 3, 2007, which are both hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] FIELD OF THE INVENTION

The present invention relates to a light emitting diode (LED) package and, more particularly, to a slim LED package that is significantly reduced in thickness without substantially reducing luminescence efficiency or while improving the luminescence efficiency.

[0003] DISCUSSION OF THE BACKGROUND

[0004] An LED emits light through recombination of electrons and holes by application of an electric current. An LED package means a package structure in which a light emitting diode chip, that is, an LED chip, is received. Many kinds of LED packages, particularly, a lead frame type LED package and a printed circuit board (PCB) type LED package, are well known in the art. The lead frame type LED package has a structure wherein a cavity of a housing for supporting a lead frame is filled with an encapsulation material, with the LED chip positioned in the cavity of the housing. The PCB type LED package has a structure wherein the LED chip is directly mounted on a PCB and covered with the encapsulation material.

[0005] For the lead frame type LED package, the housing supporting the lead frame has

an excessive thickness, which makes it difficult to fabricate a thin lead frame type LED package. On the other hand, since the PCB type LED package does not include a housing, it can be more easily fabricated to have a thin structure than the lead frame type LED package.

[0006] However, there are many restrictions in thickness reduction of the PCB type LED package. In other words, since the thickness of the PCB type LED package is determined by thicknesses of the PCB and LED chips, and a loop height of a bonding wire even without considering the encapsulation material, it is difficult to achieve an overall thickness reduction and slimness of the PCB type LED package.

[0007] Further, the encapsulation material of the LED package, which covers the LED chip, undergoes a yellowing phenomenon by energy generated from the LED chip emitting light. Such a yellowing phenomenon is a main cause of decreased luminescence performance and lifetime of the LED package. To overcome such problems, new LED packages have been developed to have a heat sink structure. In detail, the lead frame type LED package further includes a heat dissipation slug inserted into the housing by molding. Such a structure of the lead frame type LED package requires addition of components and a complicated manufacturing process, thereby decreasing economic feasibility. For the PCB type LED package, B-T resin on which the LED chip is mounted has a low heat dissipation performance, and it is difficult to have the heat sink structure.

SUMMARY OF THE INVENTION

[0008] Therefore, an aspect of the present invention is to provide a slim LED package that is configured to allow a transparent encapsulation material to directly support a lead frame without a housing, that has a reduced overall thickness by reducing the thickness of a chip

mounting region of the lead frame, and that exhibits good heat dissipation performance.

[0009] In accordance with an aspect of the present invention, a slim LED package includes: first and second lead frames separated from each other; a chip mounting recess formed on one upper surface region of the first lead frame by reducing a thickness of the one upper surface region below other upper surface regions of the first lead frame; an LED chip mounted on a bottom surface of the chip mounting recess and connected with the second lead frame via a bonding wire; and a transparent encapsulation material protecting the LED chip while supporting the first and second lead frames. The LED chip may have a thickness lower than or equal to a depth of the chip mounting recess.

[0010] The chip mounting recess may be formed by thickness-etching the one upper surface region of the first lead frame. Herein, the term "thickness-etching" refers to etching performed to reduce the thickness of a material, that is, the thickness of the one upper surface region of the lead frame.

[0011] The slim LED package may further include a bonding recess formed on one upper surface region of the second lead frame by reducing a thickness of the one upper surface region of the second lead frame below other upper surface regions of the second lead frame, one end of the bonding wire being bonded into the bonding recess. The bonding recess may be formed by thickness-etching the one upper surface region of the second lead frame.

[0012] The slim LED package may further include openings or grooves formed on an upper or lower surface of the first or second lead frame to increase a bonding force between the first and second lead frames and the encapsulation material. Alternatively, the slim LED package may further include scratches formed on an upper or lower surface of the first or second lead frame to increase the bonding force between the first and second lead frames and the

encapsulation material. Further, the LED chip may have a lower height than the depth of the chip mounting recess. The first and second lead frames may have opposite sides facing each other and including linear or rounded slant parts facing each other in a slanted state. At least one of the opposite sides may have a depressed part formed thereon to widen a separation between the first lead frame and the second lead frame.

[0013] The slim LED package may further include a phosphor in the encapsulation material. The slim LED package may further include an adjacent resin part formed in the chip mounting recess inside the encapsulation material, and the phosphor may be disposed in the adjacent resin part. Alternatively, the phosphor may be disposed in a resin constituting the encapsulation material or may be coated on the LED chip by conformal coating.

[0014] The encapsulation material may be formed by transfer molding with a solid resin, particularly, a solid EMC. Alternatively, the encapsulation material may be formed by injection molding with a liquid resin.

[0015] According to one embodiment of the present invention, the LED package is configured to mount an LED chip on a chip mounting recess, which is formed on a predetermined region of a lead frame by reducing the thickness of the predetermined region, such that the thickness of the LED chip partially overlaps the thickness of the lead frame, whereby the LED package can be significantly reduced in overall thickness, achieving an ultrathin slimness. Further, the lead frame on which the LED chip is mounted and the lead frame with which a bonding wire is connected have a significantly increased area exposed to the bottom, so that the LED package has greatly improved thermal dissipation efficiency. Additionally, a bonding recess is formed on the lead frame by reducing the thickness of a part of the lead frame with which the bonding wire is connected, and is provided therein with a wire ball

to be connected with the bonding wire. As a result, a factor causing an increase in thickness of the LED package can be eliminated, so that the LED package is further slimmed. Further, according to one embodiment of the present invention, openings or grooves are formed on the lead frames to increase a bonding force between the lead frames and an encapsulation material, thereby preventing separation of an interfacial surface between the encapsulation material and the lead frames. Moreover, an inside surface of the chip mounting recess serves to improve luminescence efficiency, as compared to a conventional PCB type LED package that is configured to reflect light emitted from the LED chip to an upper side.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The above and other aspects, features and advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

[0017] Fig. 1 is a plan view of a slim LED package according to one embodiment of the present invention;

[0018] Fig. 2 is a cross-sectional view taken along line I - I of Fig. 1;

[0019] Figs. 3 to 5 are cross-sectional views of slim LED packages according to various embodiments of the present invention;

[0020] Fig. 6 is a cross-sectional view of a slim LED package according to yet another embodiment of the present invention; and

[0021] Fig. 7 is a cross-sectional view taken along line II - II of Fig. 6; and

[0022] Figs. 8(a) and 8(b) are cross-sectional views of a slim LED package according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0023] Exemplary embodiments of the present invention will be described in detail with reference to the accompanying drawings. The embodiments are given by way of illustration for complete understanding of the present invention by those skilled in the art. Hence, the present invention is not limited to these embodiments and can be realized in various forms. Further, for convenience of description, width, length, and thickness of components are not drawn to scale in the drawings. Like components are indicated by like reference numerals throughout the specification.

[0024] Fig. 1 is a plan view of a slim LED package 1 according to one embodiment of the invention, and Fig. 2 is a cross-sectional view taken line I - I of Fig. 1.

[0025] Referring to Figs. 1 and 2, a slim LED package 1 of this embodiment includes first and second lead frames 12, 14 separated from each other. The first lead frame 12 has an LED chip 2 mounted thereon, and the second lead frame 14 is electrically connected with the LED chip 2 via a bonding wire W. The bonding wire W is connected with the second lead frame 14 via a wire ball or soldering ball (not shown).

[0026] The first and second lead frames 12, 14 are supported by a transparent encapsulation material 20. The transparent encapsulation material 20 is formed to entirely cover and protect the LED chip 2 and bonding wire W by molding. The encapsulation material 20 may be formed by transfer molding with an epoxy molding compound that is a solid epoxy resin. For example, the transfer molding is performed by compressing epoxy molding compound (EMC) powder at a proper pressure into a tablet-shape, followed by positioning and molding the tablet-shaped EMC in a mold at high temperature and pressure conditions to form

the encapsulation material 20.

[0027] In this embodiment, the encapsulation material 20 is formed by transfer molding, but the present invention is not limited thereto. Alternatively, the encapsulation material 20 can be formed by injection molding, in which a liquid resin is injected into a mold. The encapsulation material 20 may be formed of other kinds of transparent resins such as epoxy-based or silicone-based resins, as well as the EMC.

[0028] The first lead frame 12 is formed with a chip mounting recess 121 on its upper surface, and the chip mounting recess 121 has the LED chip 2 mounted on a bottom surface thereof in a die-attachment manner. The chip mounting recess 121 is formed by reducing the thickness of one upper surface region of the first lead frame 12 below other regions of the first lead frame 12, instead of bending the lead frame to form a reflection cup as in the prior art. Accordingly, the first lead frame 12 has a decreased thickness only in the region of the first lead frame 12 where the LED chip 2 is mounted, whereby a mounting height of the LED chip 2 is lowered to contribute to slimness of the LED package 1 through an overall thickness reduction of the LED package 1. Further, an inside surface of the chip mounting groove 121 serves as a reflector for reflecting light, thereby enhancing luminescence efficiency of the LED package 1.

[0029] The chip mounting recess 121 may be formed by thickness-etching, which is performed for the purpose of reducing the thickness of the lead frame. At this time, etching can be performed, with the upper surface of the first lead frame 12 except for the chip mounting region covered with a mask. Further, the chip mounting recess 121 may have a thickness of about half of the thickness of the first lead frame 12. However, it should be noted that the present invention is not limited thereto.

[0030] Further, the LED chip 2 may have a thickness less than or equal to the depth of

the chip mounting recess 121 to prevent the height of the LED chip 2 from affecting a thickness increase of the LED package 1. In other words, it is desirable that the depth of the chip mounting recess 121 be set greater than or equal to the height of the LED chip 2.

[0031] As clearly shown in Fig. 2, the first and second lead frames 12, 14 are respectively formed on lower surfaces thereof with grooves 122, 142, which are filled with a portion of the encapsulation material 20 during the molding process. As a result, the portion of the encapsulation material 20 engages with the grooves 122, 142, and a contact area between the lead frames 12, 14 and the encapsulation material 20 increases, thereby increasing a bonding force between the encapsulation material 20 and the lead frames 12, 14. The grooves 122, 142 are also formed by reducing the thickness of predetermined regions of the lower surfaces of the first and second lead frames 12, 14, and preferably by thickness-etching as described above. Alternatively, instead of forming the openings or grooves, as shown in Fig. 8(a) and Fig. 8(b), scratches 122' and 142' may be formed on the upper or lower surfaces of the first and second lead frames 12, 14, respectively, to increase the bonding force between the lead frames 12, 14 and the encapsulation material 20.

[0032] Referring again to Fig. 2, the encapsulation material 20 contains a phosphor 202 that is excited by light of a predetermined wavelength and emits light of a different wavelength. The phosphor 202 contributes to generation of white light through wavelength conversion by converting light emitted from the LED chip 2. In this embodiment, the phosphor 202 is mixed with a resin prepared as a molding material and is disposed in the encapsulation material 20 by the molding process using the molding material. For example, when forming the encapsulation material 20 by transfer molding, a mixture of EMC and the phosphor 202 is prepared and used as the material for the transfer molding.

[0033] Next, various other embodiments of the present invention will be described. In description of the embodiments, a repetitious description will be omitted, and, the same or similar elements will be denoted by the same reference numerals as those of the above description.

[0034] In Fig. 3, a bonding recess 141 is shown, which is formed by reducing the thickness of one upper surface region of a second lead frame 14 below the thickness of other regions thereof. The bonding recess 141 can also be formed by the thickness-etching as in the formation of the chip mounting recess 121 of the aforementioned embodiment. At this time, one end of a bonding wire W is connected with the second lead frame 14 within the bonding recess 141.

[0035] Although not shown in the drawings, a wire ball is located in the bonding recess 141 such that the one end of the bonding wire W is connected with the wire ball in the bonding recess 141, thereby preventing a thickness increase of the LED package due to the height of the wire ball. A size increase of the wire ball ensures that the bonding wire W can be more rigidly secured to the second lead frame 14. Here, the formation of the bonding recess 141 enables more freedom to increase the size of the wire ball.

[0036] Referring to Fig. 4, in another embodiment of the present invention, a resin 21 containing a phosphor 202 is restrictively provided in the chip mounting recess 121 to cover the LED chip 2 in an adjacent distance. Herein, the resin 21 filling in the chip mounting recess 121 will be defined as an "adjacent resin part." The adjacent resin part 21 prevents the phosphor 202 from being scattered within the encapsulation material 20, and allows the phosphor 202 to be located around the LED chip 2. This configuration can improve color conversion efficiency by the phosphor 202, and can provide light consisting of uniformly mixed colors when viewed

outside the LED package 1.

[0037] Alternatively, the adjacent resin part 21 may not contain the phosphor 202. For example, the encapsulation material such as epoxy is vulnerable to heat, and can cause thermal deformation or a yellowing phenomenon around the LED chip 2. Here, when the adjacent resin part 21 formed in the chip mounting recess 121 is made of a silicone resin, which is essentially invulnerable to heat, it is possible to efficiently prevent deterioration in performance or lifetime of the LED package 1 caused by the yellowing phenomenon. When using the silicone as a material for the adjacent resin part 21 to prevent thermal deformation or the yellowing phenomenon, the phosphor 202 can be included in the adjacent resin part 21 or omitted therefrom without any influence on the effect of preventing thermal deformation or the yellowing phenomenon.

[0038] Alternatively, the phosphor 202 can be coated on the surface of the LED chip 2 by, for example, conformal coating via electrophoresis. In this case, the LED package 1 has a configuration as illustrated in Fig. 5.

[0039] Fig. 6 is a cross-sectional view of a slim LED package 1 according to yet another embodiment of the present invention, and Fig. 7 is a cross-sectional view taken along line II - II of Fig. 6.

[0040] Referring to Figs. 6 and 7, instead of the grooves 122, 142 (see Fig. 2) of the above embodiment, first and second lead frames 12, 14 of this embodiment are formed with openings 123, 143, which penetrate the first and second lead frames 12, 14 in the vertical direction, to increase the bonding force between an encapsulation material 20 and the lead frames 12, 14. The openings 123, 143 can be formed by pressing or by etching the lead frames 12, 14 in the thickness direction.

[0041] As clearly shown in Fig. 6, the first and second lead frames 12, 14 include first and second slant parts 125, 145, which are formed on opposite sides of the lead frames 12, 14 facing each other in an inclined state. That is, the first slant part 125 is formed on one side of the first lead frame 12 facing the other side of the second lead frame 14 to be inclined towards right and left sides of the first lead frame 12. Further, the second slant part 145 is formed on the other side of the second lead frame 14 facing the one side of the first lead frame 12 to be inclined towards right and left sides of the second lead frame 14. The first and second slant parts 125, 145 may have a linear or curved shape.

[0042] A portion of the encapsulation material 20 is interposed between the opposite sides of the first and second lead frames 12, 14 facing each other, and a force is applied to the interposed portion of the encapsulation material 20 and the opposite sides of the first and second lead frames 12, 14. At this time, the slant parts 125, 145 disperse the force diagonally, thereby preventing the encapsulation material 20 from being broken on the opposite sides of the lead frames 12, 14. Furthermore, since the slant part 125 of the first lead frame 12 has a shape surrounding the portion of the encapsulation material 20 adjacent thereto, it serves to more rigidly hold the encapsulation material 20. It should be noted that the breakage of the encapsulation material 20 between the opposite sides of the lead frames 12, 14 may cause electric shorts or the like.

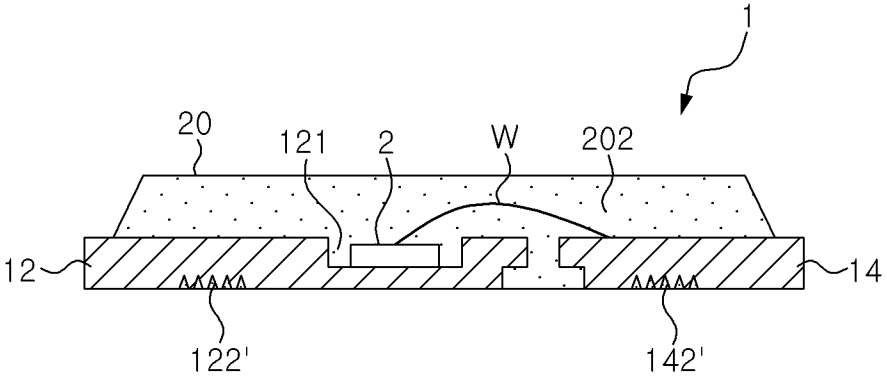
[0043] Additionally, a depressed part 126 is formed at the center of the one side of the first lead frame 12 facing the other side of the second lead frame 14 to increase a separation between the first lead frame 12 and the second lead frame 14. The depressed part 126 is located directly below a path of the bonding wire W which connects the first lead frame 12 with the second lead frame 14. The depressed part 126 prevents the bonding wire W from being

erroneously brought into contact with the lead frames 12, 14, and an electric short of the bonding wire W caused by the erroneous contact.

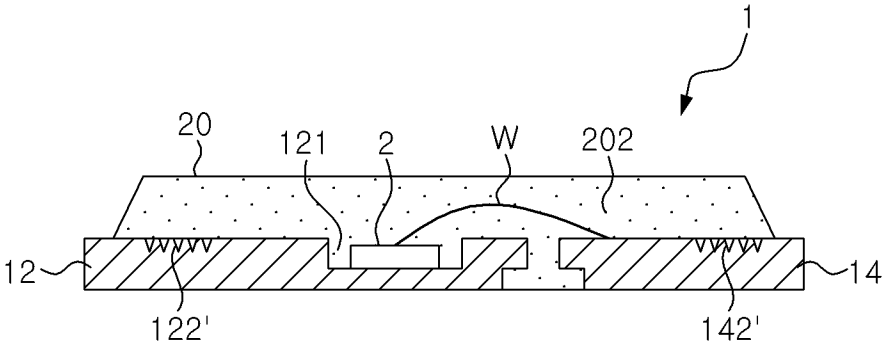
[0044] To fabricate the LED packages 1 as described above, a single metal sheet is processed to have a pattern of first and second lead frames 12, 14, followed by molding an encapsulation material 20 on the patterned metal sheet. Then, the lead frames 12, 14 are sawn per each encapsulation material 20 supporting a pair of first and second lead frames 12, 14, thereby providing a plurality of LED packages 1. At this time, a process of removing burrs formed during sawing may be further included.

[0045] Although the present invention has been described with reference to the embodiments and the accompanying drawings, the present invention is not limited to these embodiments and the drawings. It should be understood that various modifications, additions and substitutions can be made by a person having ordinary knowledge in the art without departing from the scope and spirit of the invention, as defined only by the accompanying claims.

Fig. 8



(a)



(b)

PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	2010-06-02
First Named Inventor	Eun Jung SEO
Art Unit	
Examiner Name	
Attorney Docket Number	P3962US00

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6603148		2003-08-05	Sano et al.	

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2006-179541	JP		2006-07-06	Enomoto Co Ltd		☐
	2	1020020065729	KR		2002-08-14	Chippac Korea Co., Ltd.		☐
	3	1020060059575	KR		2006-06-02	Samsung Electronics Co., Ltd.		☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	
	Filing Date	2010-06-02
	First Named Inventor	Eun Jung SEO
	Art Unit	
	Examiner Name	
	Attorney Docket Number	P3962US00

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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		☐

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	
	Filing Date	2010-06-02
	First Named Inventor	Eun Jung SEO
	Art Unit	
	Examiner Name	
	Attorney Docket Number	P3962US00

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2010-06-02
Name/Print	Hae-Chan Park	Registration Number	50114

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT ABSTRACTS OF JAPAN

(11)Publication number : **2006-179541**
(43)Date of publication of application : **06.07.2006**

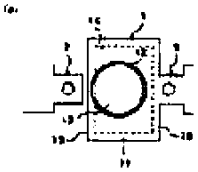
(51)Int.Cl. *H01L 33/00 (2006.01)*
H01L 23/48 (2006.01)

(21)Application number : **2004-368650**
(22)Date of filing : **21.12.2004**

(71)Applicant : **ENOMOTO CO LTD**
(72)Inventor : **OGAWA HIDEO**
UMEYA KAZUYOSHI

(54) LEAD FRAME FOR POWER LED AND ITS MANUFACTURING PROCESS

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a lead frame for power LED in which assembling work of components is not required, the occurrence rate of defective products is lower and manufacturing cost is relatively low, and to provide a manufacturing process of a lead frame for power LED in which assembling work of components is not required, the occurrence rate of defective products is low, manufacturing cost is relatively low and processing speed is high.
SOLUTION: A lead frame for power LED in which a heat sink portion 1 and a lead portion 3 at least on one side are made integrally of the same metal material.





(19)日本国特許庁(JP)　(12)公開特許公報(A)　(11)特許出願公開番号
特開2006-179541
(P2006-179541A)
(43)公開日　平成18年7月6日(2006.7.6)

(51)Int.Cl.		F I			テーマコード（参考）
H01L 33/00	***(2006.01)***	H01L	33/00	N	5F041
H01L 23/48	***(2006.01)***	H01L	23/48	F	

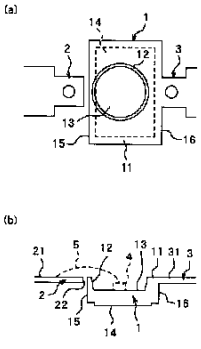
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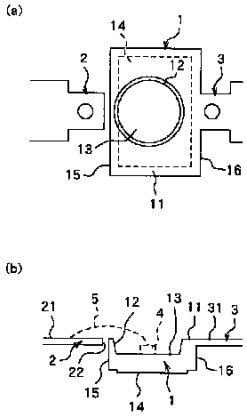
(21)出願番号　特願2004-368650 (P2004-368650)
(22)出願日　平成16年12月21日 (2004.12.21)

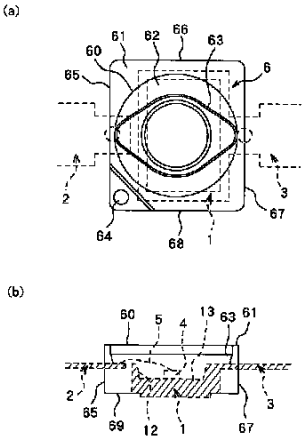
(71)出願人　390032528
株式会社エノモト
山梨県上野原市上野原８１５４－１９
(74)代理人　100097319
弁理士　狩野　彰
(72)発明者　小川　秀雄
山梨県北都留郡上野原町上野原８１５４－１９　株式会社エノモト内
(72)発明者　梅屋　一芳
山梨県北都留郡上野原町上野原８１５４－１９　株式会社エノモト内

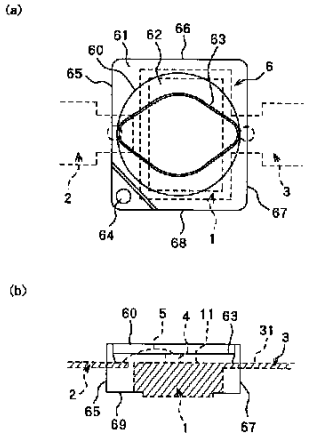
Fターム(参考)　5F041 AA33　AA41　AA42　DA17　DA22　DA25　DA43

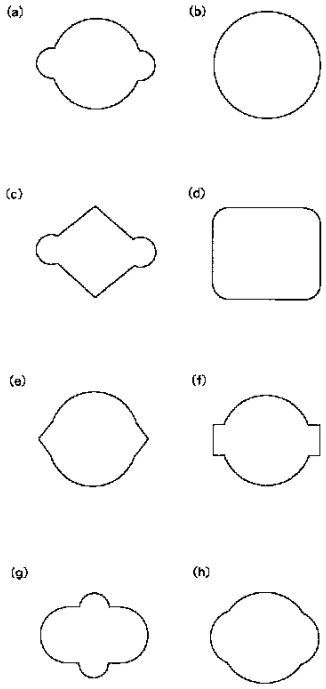
(54)【発明の名称】パワーＬＥＤ用リードフレーム及びその製造方法

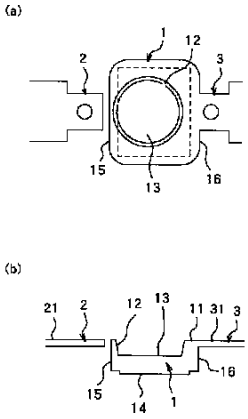


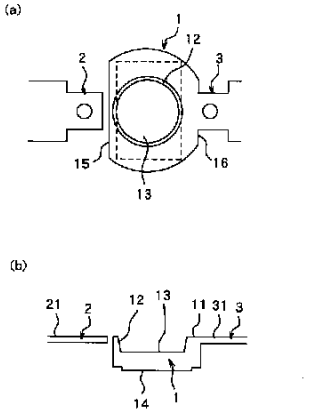

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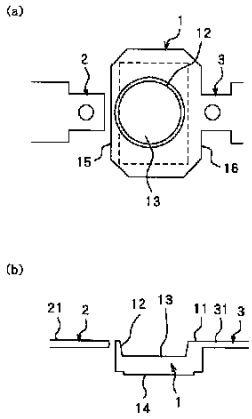

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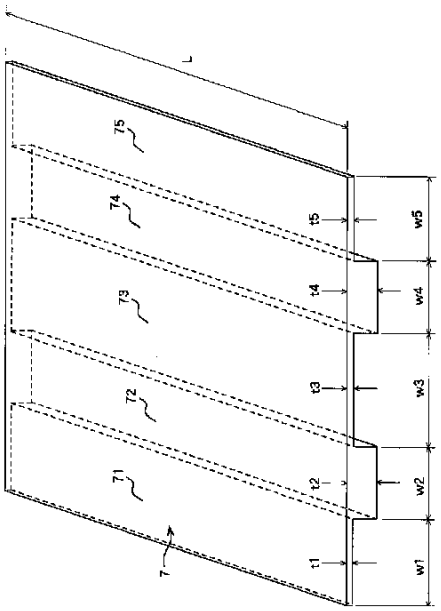

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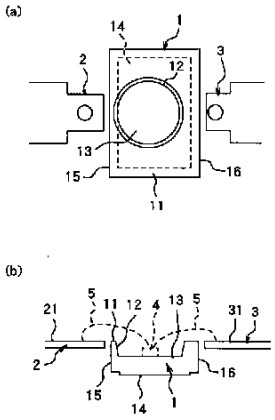

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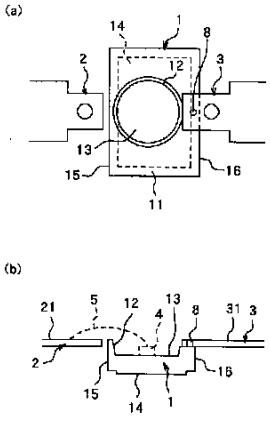

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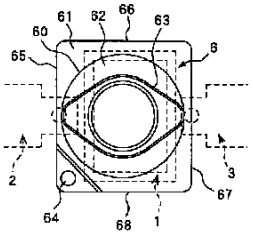

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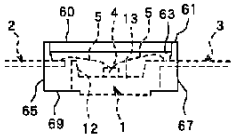

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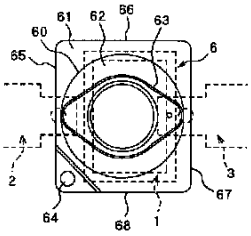
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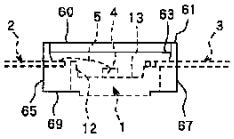
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(19) KOREAN INTELLECTUAL PROPERTY OFFICE

KOREAN PATENT ABSTRACTS

(11)Publication number: 1020020065729 A
(43)Date of publication of application: 14.08.2002

(21)Application number: 1020010005902
(22)Date of filing: 07.02.2001
(30)Priority:

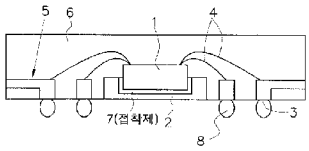
(51)Int. Cl H01L 23/04

(71)Applicant: CHIPPAC KOREA CO., LTD.
(72)Inventor: KIM, YEONG SIL

(54) SEMICONDUCTOR PACKAGE

(57) Abstract:

PURPOSE: A semiconductor package is provided to reduce fabricating cost and improve a heat radiating capacity, by using conventional materials which are inexpensive and reliable. CONSTITUTION: A semiconductor chip attach region of a die pad(2) is half-etched. A semiconductor chip(1) is attached to the half-etched region of the die pad. A lead(5) is composed of a half-etching region and a ball land region, separately positioned near the die pad. A conductive connecting member(4) electrically connects a bonding pad of the semiconductor chip with the lead. A mold body(6) surrounds the entire structure except only the ball land region of the lead.



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Legal Status
Date of request for an examination (20010503)
Notification date of refusal decision ( )
Final disposal of an application (rejection)
Date of final disposal of an application (20041117)
Patent registration number ( )
Date of registration ( )
Number of opposition against the grant of a patent ( )
Date of opposition against the grant of a patent ( )
Number of trial against decision to refuse (2004101004120)
Date of requesting trial against decision to refuse (20040913)
Date of extinction of right ( )

(19) 대한민국특허청(KR)
(12) 공개특허공보(A)

(51) 。Int. Cl. [7]
H01L 23/04

(11) 공개번호 특2002-0065729
(43) 공개일자 2002년08월14일

(21) 출원번호 10-2001-0005902
(22) 출원일자 2001년02월07일

(71) 출원인 주식회사 칩팩코리아
경기 이천시 부발읍 아미리 산136-1

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요약

본 발명은 기존의 반도체 패키지가 갖는 장점을 최대한 살리면서 단점은 해소한 새로운 타입의 반도체 패키지를 제공하기 위한 것으로서, 값싸고 신뢰성 높은 기존의 부자재(附資材)를 이용하므로써 제조 비용 측면에서는 저비용으로 제조 가능하고 구조적 측면에서는 경박단소하며 방열성능이 뛰어난 신뢰성 높은 반도체 패키지 및 그 제조방법을 제공하기 위한 것이다.

이를 위해, 본 발명은 반도체칩(1) 부착영역이 하프에칭된 다이패드(2)와, 상기 다이패드(2)의 하프에칭된 영역에 부착되는 반도체칩(1)과, 상기 다이패드(2) 주위에 이격되어 위치하며 하프에칭 영역 및 볼랜드(3) 영역으로 이루어진 리드(5)와, 상기 반도체칩(1)의 본딩패드와 상기 리드(5)를 전기적으로 연결하는 전도성 연결부재(4)와, 상기 리드(5)의 볼랜드(3) 영역만이 노출되도록 하고 이를 제외한 나머지 전체 구조를 감싸는 몰드바디(6)를 포함하여서 된 반도체 패키지가 제공된다.

대표도
도 1

명세서

도면의 간단한 설명

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도 1은 본 발명의 제1실시예에 따른 반도체 패키지를 나타낸 종단면도

도 2는 본 발명의 제2실시예에 반도체 패키지를 나타낸 종단면도

도 3은 본 발명의 제3실시예에 따른 반도체 패키지를 나타낸 종단면도

도 4는 본 발명의 제4실시예에 따른 반도체 패키지를 나타낸 종단면도

* 도면의 주요부분에 대한 부호의 설명 *

1:반도체 칩2:다이패드

3:볼랜드4:전도성 연결부재

5:리드6:몰드바디

7:어드헤시브8:솔더볼

9:랜드

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 반도체 패키지에 관한 것으로서, 더욱 상세하게는 기존의 부자재인 리드프레임을 이용하면서도 경박단소화되며 열방출 성능이 향상된 새로운 구조의 반도체 패키지를 제공하기 위한 것이다.

일반적으로, 반도체 산업에서 집적회로에 대한 패키징 기술은 소형화에 대한 요구 및 실장 신뢰성을 만족시키기 위해 지금까지 계속 발전해오고 있다.

즉, 소형화에 대한 요구는 칩 스케일에 근접한 패키지에 대한 개발을 가속화시키고 있으며, 실장 신뢰성에 대한 요구는 실장작업의 효율성 및 실장후의 기계적· 전기적 신뢰성을 향상시킬 수 있는 패키지 제조 기술에 대한 중요성을 부각시키고 있다.

한편, 일반적으로 반도체소자는 집적회로가 형성된 웨이퍼 상태에서 낱개의 칩으로 각각 분리된 후, 이것을 플라스틱 패키지나 세라믹 패키지에 탑재하여 기판에의 실장이 용이하도록 조립하는 패키징 공정을 거치게 된다.

이와 같이 행해지는 반도체소자에 대한 패키징 공정의 주목적은 기판이나 소켓에 실장하기 위한 형상의 확보와 기능보호에 있다고 할 수 있다.

또한, 최근에는 집적회로의 고집적화에 따라 다핀화, 미세조립기술, 또 실장형태의 다양화에 따른 패키지의 다종류화 등, 조립공정과 관련된 기술도 각각 세분된 분야에 따라 크게 변화하고 있다.

반도체 조립공정의 개요에 대해 현재 가장 많이 사용되고 있는 플라스틱 타입의 반도체소자를 예로 들어 설명하면 다음과 같다.

먼저, 전기적 회로가 형성된 웨이퍼를 각각의 단일 칩으로 분리하는데, 이때 Si(실리콘)는 모스경도 7로서 딱딱하고 깨지기 쉬운 성질을 갖고 있으므로 웨이퍼의 제조시 미리 분리할 라인에 절단하기 위한 물질을 넣어두고 이 분리라인을 따라 브레이크 응력을 가해 파괴, 분리시키는 방법을 취하는 경우가 많다.

또한, 분리된 각각의 반도체 칩은 리드프레임의 다이패드에 본딩되고, 이때의 접합방법은 Au-Si 공정(共晶)법, 납땜법, 수지접착법 등이 있으며 용도에 따라 알맞은 방법이 선택되어 사용된다.

한편, 전술한 바와 같이 반도체 칩을 리드프레임의 다이패드에 접착하는 목적은 조립이 완료된 후 기판에 실장시키기 위해서 뿐만 아니라, 전기적 입출력단자나 어스(earth)를 겸하는 일도 있으며 소자의 동작시 발생하는 열의 방열통로로서도 필요로 하는 경우가 있기 때문이다.

상기와 같이 반도체 칩을 본딩한 후에는 칩의 본딩패드와 리드프레임의 인너리드를 와이어로 본딩하므로써 연결하게 되며, 와이어 본딩의 방법으로 플라스틱 봉함 패키지에서는 일반적으로 골드 와이어를 사용한 열압착법 또는 열압착법과 초음파법을 혼용한 방법이 주로 이용되고 있다.

또한, 와이어 본딩에 의해 반도체 칩과 인너리드가 전기적으로 연결된 후에는 칩을 고순도의 에폭시 수지를 사용하여 성형 봉합하므로써 몰드바디를 형성시키는 몰딩공정이 수행되는데, 이때 사용되는 에폭시 수지는 집적회로의 신뢰성을 좌우하는 중요한 요소이며, 수지의 고순도화와 몰딩시 집적회로에 주어지는 응력을 저감시키기 위한 저응력화 등의 개선이 추진되고 있다.

그리고, 상기한 공정이 완료된 후에는 IC 패키지를 소켓이나 기판에 실장하기 위해 아웃터리드(outer lead)를 소정의 형상으로 절단하고 성형하는 공정이 행해지며, 아웃터리드에는 실장접합성(납땜성)을 향상시키기 위해 도금이나 납딥(dip)이 처리된다.

한편, 반도체 패키지는 실장형태 및 리드형태에 따라 여러 가지 유형으로 나뉘는데, 패키지의 대표적인 예로서는 전술한 DIP(Dual Inline Package)외에 QFP(Quad Flat Package), TSOP(Thin Small Outline Package), BGA 패키지(Ball Grid Array package), BLP(Bottom Leaded Package) 등이 있으며, 계속 다핀(多-pin)화 또는 경박단소(輕薄短小)화 되고 있다.

상기한 패키지 타입중, BGA 패키지(Ball Grid Array package)는 반도체 칩이 부착된 기판의 이면에 구형의 솔더볼을 소정의 상태로 배열(Array)하여 아웃터리드(outer lead) 대신으로 사용하게 되며, 상기 BGA 패키지는 패키지 몸체(Package Body) 면적을 QFP(Quad Flat Package) 타입보다 작게 할 수 있으며, QFP와는 달리 리드의 변형이 없는 장점이 있다.

발명이 이루고자 하는 기술적 과제

그러나, 상기 BGA 패키지는 기존의 리드프레임에 비해 값이 비싼 회로기판을 사용하므로 제조원가가 높아지고, 반도체 칩 및 골드 와이어의 보호를 위해 봉지공정 수행시 상형 및 하형에 의해 회로기판이 눌러져 솔더마스크에 크랙이 발생할 우려가 높아지는 등의 단점이 있다.

한편, BLP(Bottom Leaded Package)는 패키지 몸체의 바텀면을 통해 노출된 리드를 이용하여 기판에 실장하므로, 패키지 몸체의 두께를 아웃터리드를 갖는 DIP나 QFP 타입에 비해 작게 할 수 있다.

상기한 반도체 패키지들은 실장면적, 입출력 단자수, 전기적 신뢰성, 제조공정의 유연성, 제조비용등에 있어 제각기 장점 및 단점을 갖고 있다.

따라서, 상기한 각 패키지들의 장점을 살리면서 단점을 해소한 새로운 타입의 반도체 패키지가 지속적으로 연구 개발되고 있는 실정이다.

본 발명은 상기한 바와 같이 기존의 반도체 패키지가 갖는 장점을 최대한 살리면서 단점은 해소한 새로운 타입의 반도체 패키지를 제공하기 위한 것으로서, 값싸고 신뢰성 높은 기존의 부자재(附資材)를 이용하므로써 제조 비용 측면에서는 저비용으로 제조가능하고 구조적 측면에서는 경박단소하며 방열성능이 뛰어난 신뢰성 높은 반도체 패키지 및 그 제조방법을 제공하는데 그 목적이 있다.

발명의 구성 및 작용

상기한 목적을 달성하기 위해, 본 발명은 반도체칩 부착영역이 하프에칭된 다이패드와, 상기 다이패드의 하프에칭된 영역에 부착되는 반도체칩과, 상기 다이패드 주위에 이격되어 위치하며 하프에칭 영역 및 볼랜드 영역으로 이루어진 리드와, 상기 반도체칩의 본딩패드와 상기 리드를 전기적으로 연결하는 전도성 연결부재와, 상기 리드의 볼랜드 영역만이 노출되도록 하고 이를 제외한 나머지 전체 구조를 감싸는 몰드바디를 포함하여서 된 반도체 패키지가 제공된다.

이하, 본 발명의 실시예들을 도 1 내지 도 4를 참조하여 상세히 설명하면 다음과 같다.

먼저, 본 발명의 제1실시예를 설명하면 다음과 같다.

도 1은 본 발명의 제1실시예에 따른 반도체 패키지를 나타낸 종단면도로서, 본 발명의 제1실시예에 따른 반도체 패키지는, 반도체칩(1) 부착영역이 하프에칭된 다이패드(2)와, 상기 다이패드(2)의 하프에칭된 영역에 부착되는 반도체칩(1)과, 상기 다이패드(2) 주위에 이격되어 위치하며 하프에칭 영역 및 볼랜드(3) 영역으로 이루어진 리드(5)와, 상기 반도체칩(1)의 본딩패드와 상기 리드(5)를 전기적으로 연결하는 전도성 연결부재(4)와, 상기 리드(5)의 볼랜드(3) 영역만이 노출되도록 하고 이를 제외한 나머지 전체 구조를 감싸는 몰드바디(6)와, 상기 몰드바디(6) 하부로 노출된 리드(5)의 볼랜드(3)에 부착되는 솔더볼(8)을 포함하여 구성된다.

이 때, 상기 전도성 연결부재(4)는 골드, 알루미늄, 또는 구리중의 어느 하나이거나 이들을 포함한 합금으로 이루어진다.

또한, 상기 다이패드(2)와 반도체칩(1) 사이에는 에폭시 또는 양면 접착테이프 등의 어드헤시브(7)가 개재(介在)된다.

이와 같이 구성된 본 발명의 제1실시예에 따른 반도체 패키지의 제조과정은 다음과 같다.

먼저, 다이패드(2)의 하프에칭된 반도체칩(1) 부착영역에 반도체칩(1)을 부착한다.

이 때, 상기 다이패드(2)와 반도체칩(1) 사이에는 에폭시 또는 양면 접착테이프등의 어드헤시브(7)가 개재(介在)됨은 물론이다

그 후, 상기 반도체칩(1)의 본딩패드와 상기 리드(5)를 골드와이어 등의 전도성 연결부재(4)를 이용하여 전기적으로 연결한다.

이어, 상기 봉지제를 이용하여 리드(5)의 볼랜드(3) 영역만이 노출되도록 봉지하여 몰드바디(6)를 형성한다.

이에 따라, 반도체 칩과 전도성 연결부재(4)는 외부의 영향으로부터 보호된다.

그리고, 상기한 바와 같이 몰드바디(6)가 형성된 후에는 몰드바디(6) 하부로 노출된 볼랜드(3)에 솔더페이스트를 도포한 다음 솔더볼(8)을 부착하여 패키지를 완성하게 된다.

한편, 도 2는 본 발명의 제2실시예에 따른 반도체 패키지를 나타낸 종단면도로서, 이 경우는 다이패드(2) 상면의 반도체칩(1) 부착영역만이 하프에칭되는 것이 아니라, 다이패드 전면이 하프에칭되는 경우로서, 나머지 구성은 제1실시예에서 동일하므로 그 설명은 생략한다.

이하에서는, 본 발명의 제3실시예에 대해 설명하고자 한다.

도 3은 본 발명의 제3실시예에 따른 반도체 패키지를 나타낸 종단면도로서,제3실시예에 따른 반도체 패키지는 반도체

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칩(1) 부착영역이 하프에칭된 다이패드(2)와, 상기 다이패드(2)의 하프에칭된 영역에 부착되는 반도체칩(1)과, 상기 다이패드(2) 주위에 이격되어 위치하며 하프에칭 영역 및 랜드(9) 영역으로 이루어진 리드(5)와, 상기 반도체칩(1)의 본딩패드와 상기 리드(5)를 전기적으로 연결하는 전도성 연결부재(4)와, 상기 리드(5)의 랜드(9) 영역만이 노출되도록 하고 이를 제외한 나머지 전체 구조를 감싸는 몰드바디(6)를 포함하여서 구성된다.

이 때, 상기 전도성 연결부재(4)는 골드, 알루미늄, 또는 구리중의 어느 하나이거나 이들을 포함한 합금으로 이루어진다.

또한, 상기 다이패드(2)와 반도체칩(1) 사이에는 에폭시 또는 양면접착테이프등의 어드헤시브(7)가 개재(介在)된다.

이와 같이 구성된 본 발명의 제3실시예에 따른 반도체 패키지의 제조 과정은 제1 및 제2실시예의 패키지 제조과정과 동일한 원리로 진행되며, 다만 솔더볼(8) 부착공정이 생략되는 점만이 다르므로 제조과정의 설명은 생략한다.

한편, 상기한 제3실시예의 경우에는 랜드(9) 영역에 솔더페이스트가 도포되어 마더보드에 그대로 실장되므로 패키지의 실장 높이를 한층 더 낮출수 있게 된다.

도 4는 본 발명의 제4실시예에 따른 반도체 패키지를 나타낸 종단면도로서, 이 경우에는 다이패드(2) 상면의 반도체칩(1) 부착영역만이 하프에칭되는 것이 아니라, 다이패드(2) 전면이 하프에칭되는 경우로서, 나머지 구성은 제3실시예에서 동일하므로 그 설명은 생략한다.

한편, 상기한 제1내지 제4실시예에 따른 반도체 패키지는 볼 그리드 타입 또는 랜드 그리드 타입으로 제조 가능함은 물론이다.

발명의 효과

이상에서와 같이, 본 발명은 기존의 반도체 패키지가 갖는 장점을 최대한 살리면서 단점은 해소한 새로운 타입의 반도체 패키지를 제공하기 위한 것이다.

즉, 본 발명은 값싸고 신뢰성 높은 기존의 부자재(附資材)를 이용하므로써 제조 비용 측면에서는 저비용으로 제조가능하고 구조적 측면에서는 경박단소하며 방열성능이 뛰어난 신뢰성 높은 반도체 패키지의 제조가 가능하다.

(57) 청구의 범위

청구항 1.

반도체칩 부착영역이 하프에칭된 다이패드와,

상기 다이패드의 하프에칭된 영역에 부착되는 반도체칩과,

상기 다이패드 주위에 이격되어 위치하며 하프에칭 영역 및 볼랜드 영역으로 이루어진 리드와,

상기 반도체칩의 본딩패드와 상기 리드를 전기적으로 연결하는 전도성 연결부재와,

상기 리드의 볼랜드 영역만이 노출되도록 하고 이를 제외한 나머지 전체 구조를 감싸는 몰드바디를 포함하여서 된 반도체 패키지.

청구항 2.

제 1 항에 있어서,

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상기 리드의 볼랜드 영역에 솔더볼이 부착됨을 특징으로 하는 반도체 패키지.

청구항 3.

제 1 항에 있어서,

상기 전도성 연결부재는 골드, 알루미늄, 또는 구리중의 어느 하나이거나 이들을 포함한 합금으로 이루어짐을 특징으로 하는 반도체 패키지.

청구항 4.

제 1 항에 있어서,

상기 다이패드와 반도체칩 사이에는 에폭시 또는 양면 접착테이프 등의 어드헤시브가 개재(介在)됨을 특징으로 하는 반도체 패키지.

청구항 5.

반도체칩 부착영역이 하프에칭된 다이패드와,

상기 다이패드의 하프에칭된 영역에 부착되는 반도체칩과,

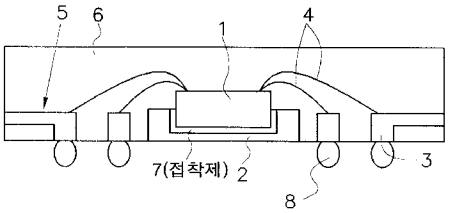
상기 다이패드 주위에 이격되어 위치하며 하프에칭 영역 및 랜드 영역으로 이루어진 리드와,

상기 반도체칩의 본딩패드와 상기 리드를 전기적으로 연결하는 전도성 연결부재와,

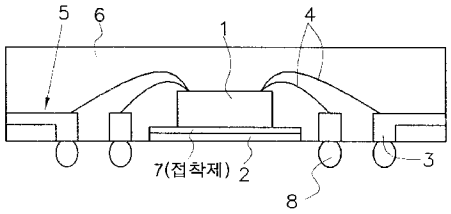
상기 리드의 랜드 영역만이 노출되도록 하고 이를 제외한 나머지 전체 구조를 감싸는 몰드바디를 포함하여서 됨을 특징으로 하는 반도체 패키지.

도면

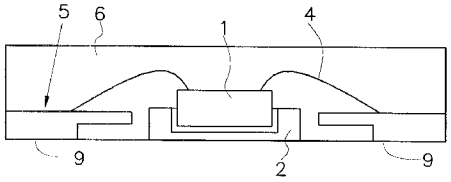
도면 1



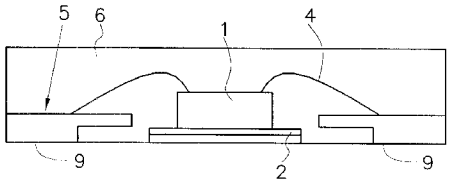
도면 2



도면 3



도면 4



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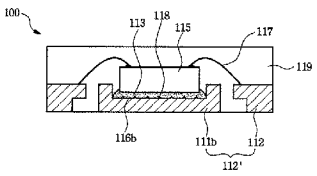
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SHIM, BO KEUN

(54) SEMICONDUCTOR PACKAGE USING FINE PROTRUSIONS OF DIE PAD FOR INCREASING CONTACT SURFACE BETWEEN SEMICONDUCTOR CHIP AND DIE PAD

(57) Abstract:



PURPOSE: A semiconductor package is provided to intensify the adhesiveness between a semiconductor chip and a die pad by increasing a contact surface between the semiconductor chip and the die pad using fine protrusions. CONSTITUTION: A semiconductor package comprises a lead frame, a semiconductor chip, a connection par, and a resin molding part. The lead frame(112) includes a die pad. A plurality of fine protrusions are formed on a chip mounting surface of the die pad. The semiconductor chip(115) is attached on the die pad via a liquid type adhesive. The connection part is used for connecting electrically the semiconductor chip with the lead frame. The resin molding part(119) is used for molding selectively the resultant structure.

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심사청구 : 없음

(54) 다이패드에 미세 돌기가 형성된 반도체 패키지

요약

본 발명은 다이패드에 미세 돌기가 형성된 반도체 패키지에 관한 것으로, 다이패드의 반도체 칩 실장면에 미세 돌기가 형성된 리드프레임; 상기 다이패드 위에 액상형 접착제에 의해 부착되는 반도체 칩; 상기 반도체 칩과 상기 리드프레임을 전기적으로 연결하는 연결수단; 및 상기 반도체 칩, 리드프레임 및 연결수단을 봉지하는 수지 봉지부를 포함하며, 상기 미세 돌기에 의해 반도체 칩과 다이패드 사이의 접착면적이 넓어지는 것을 특징으로 한다. 본 발명에 따른 다이패드에 미세 돌기가 형성된 반도체 패키지에 의하면 반도체 칩과 다이패드간의 접착면적이 증가하여 반도체 칩과 다이패드의 접착력을 증가시킬 수 있고, 칩 실장면의 거칠기(roughness)에 의하여 액상형 접착제의 치우침에 의한 에폭시 보이드의 발생을 감소시킬 수 있어 반도체 패키지의 신뢰성을 향상시킬 수 있다.

대표도

도 5

색인어

미세 돌기, 리드프레임, 하프에칭, ELP, 반도체 패키지

명세서

도면의 간단한 설명

도1a는 종래 ELP(Exposed Leaded Package)를 나타내는 단면도이다.

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도1b은 종래 DDP(Dual Die Package)를 나타내는 단면도이다.

도2는 하프에칭 리드프레임의 다이패드 제조공정의 단면도이다.

도3a는 종래 하프에칭 리드프레임의 다이패드를 나타내는 단면도이다.

도3b는 본 발명에 따른 반도체 패키지에 이용하는 칩 실장 영역에 미세 돌기가 형성된 다이패드를 나타내는 단면도이다.

도4a는 종래 하프에칭 리드프레임을 나타내는 SEM(Scanning Electron Micro-scope) 사진이다.

도4b는 본 발명에 따른 반도체 패키지에 이용하는 다이패드 미세 돌기가 형성된 하프에칭 리드프레임을 나타내는 SEM사진이다.

도5는 본 발명에 따른 다이패드에 미세 돌기가 형성된 반도체 패키지의 일실시예를 나타내는 단면도이다.

<도면의 주요부분에 대한 간단한 설명>

11, 21, 111; 다이패드 12, 22, 112; 리드

12', 22', 112'; 리드프레임 13, 23, 113; 액상형 접착제

114; 포켓 15, 25, 115; 반도체 칩

116; 칩 실장면 17, 27, 117; 본딩 와이어

118; 미세 돌기 19, 29, 119; 수지 봉지부

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 반도체 패키지에 관한 것으로서, 보다 구체적으로는 반도체 칩과 다이패드간의 접착력을 증가시키고 액상형 접착제의 치우침에 의한 에폭시 보이드를 감소시킬 수 있는 다이패드에 미세 돌기가 형성된 반도체 패키지에 관한 것이다.

최근 전자기기 및 휴대기기의 고성능화 및 소형화, 경량화로 인하여 패키지 내에 실장되는 반도체 칩의 수는 증가하는 한편 패키지 자체는 경박단소화가 요구되고 있다. 이러한 요구에 부응하기 위한 다양한 패키지 구조가 개발되고 있으며, 특히 리드프레임을 이용한 반도체 패키지에서는 하프에칭이라는 구조를 통하여 리드프레임의 두께를 감소시켜 패키지의 경박 단소화 및 고집적화를 추구하고 있다.

도1a 및 도1b는 이러한 하프에칭 리드프레임을 이용한 반도체 패키지의 실시예를 나타내는 단면도이다. 도1a는 ELP(Exposed Leaded Package) 구조를 나타내며, 도 2a는 DDP(Dual Die Package) 구조를 나타낸다.

도1a를 참조하면, ELP(10)는 칩 실장 영역이 가장자리에 대하여 오목하게 형성된 다이패드(11)에 액상형 접착제(13)에 의하여 반도체 칩(15)이 부착된다. 본딩 와이어에 의하여 반도체 칩(15)과 리드(12)가 전기적으로 연결되며, 반도체 칩(15) 및 본딩 와이어(17)의 보호를 위하여 리드프레임(12'), 반도체 칩915) 및 본딩 와이어(17)를 봉지한 수지 봉지부(19)가 형성된 구조를 갖는다. 수지 봉지부(19)는 다이 패드(11) 및 리드(12)의 하면이 외부로 노출되도록 형성된다. 이러한 구조에 의하면 다이패드(11)의 하프에칭 깊이 만큼 패키지의 두께를 감소시킬 수 있어 패키지 박형화시킬 수 있다.

도1b를 참조하면, DDP(20)는 도1a와 같이 형성된 다이패드(21)의 상면과 하면에 모두 반도체 칩(25)이 부착된 구조를 갖는다. 각 반도체 칩(25)과 리드(22)는 본딩 와이어(17)에 의하여 전기적으로 연결되며, 반도체 칩(25), 본딩 와이어(27)를

보호하기 위하여 리드프레임(22'), 반도체 칩(25) 및 본딩 와이어(27)를 봉지한 수지 봉지부(19)가 형성된다. 이러한 구조에 의하면 다이패드(21)의 하프에칭 깊이만큼 패키지의 두께를 감소시킬 수 있으며,하나의 패키지(20) 안에 두개의 반도체 칩(25)을 실장할 수 있어 패키지의 고집적화가 가능해진다.

그러나 종래 하프에칭 리드 프레임을 이용한 반도체 패키지(10, 20)에서 칩 실장면(16, 26)은 평평하게 형성되는 것이 일반적이다. 따라서 반도체 칩 부착공정, 봉지 공정 및 신뢰성 시험 등 고온을 수반하는 공정에서 액상형 접착제(13, 23)의 유동성이 증가하게 되고 이러한 액상형 접착제(13, 23)가 평평한 칩 실장면(16, 26) 위를 흘러 접착제가 한쪽으로 치우지는 현상이 발생한다. 이러한 접착제의 치우침 현상은 에폭시 보이드 및 반도체 칩(15, 25)과 다이패드(11, 21)간의 접착력을 약화시키는 문제를 가져온다.

발명이 이루고자 하는 기술적 과제

본 발명의 제 1목적은 액상형 접착제를 사용하는 경우 발생하는 접착제의 치우침 현상에 의한 에폭시 보이드를 감소시키는데 있다.

본 발명의 제 2목적은 반도체 칩과 리드프레임간 접착성을 증대하여 반도체 패키지의 신뢰성을 향상시키는데 있다.

발명의 구성 및 작용

이와 같은 목적 달성을 위하여 본 발명은 다이패드의 반도체 칩 실장면에 미세 돌기가 형성된 리드프레임; 상기 다이패드 위에 액상형 접착제에 의해 부착되는 반도체 칩; 상기 반도체 칩과 상기 리드프레임을 전기적으로 연결하는 연결수단; 및 상기 반도체 칩, 리드프레임 및 연결수단을 봉지하는 수지 봉지부를 포함하며, 상기 미세 돌기에 의해 반도체 칩과 다이패드 사이의 접착면적이 넓어지는 것을 특징으로 하는 다이패드에 미세 돌기가 형성된 반도체 패키지를 제공한다.

본 발명에 따른 다이패드에 미세 돌기가 형성된 반도체 패키지의 반도체 칩 실장면은 하프에칭(Half-etching)에 의해 다이패드의 가장자리 부분에 대해서 아래로 오목하게 형성된 포켓의 바닥면인 것을 특징으로 한다.

또한 본 발명에 따른 다이패드에 미세 돌기가 형성된 반도체 패키지의 미세돌기는 칩 실장면의 가장 낮은 곳에 대하여 2~3μm 돌출된 것을 특징으로 한다.

이하 본 발명에 따른 다이패드에 미세 돌기가 형성된 반도체 패키지의 실시예를 도면을 참조하여 상세히 설명하기로 한다.

도2는 일반적인 하프에칭 리드프레임 제작시 다이패드의 제작 공정을 나태내는 단면도이다. 도2를 참조하면, 다이 패드(111)는 에칭 영역을 제외한 영역에 레지스터(120)가 도포되고, 에칭 영역을 포함하는 면이 아래를 향하도록 고정된다. 다이패드(111) 아래에 위치한 분사기(130)로 에칭용액을 분사하는 것에 의하여 에칭면이 형성되며, 에칭 용액으로는 일반적으로 염화철 용액이 사용된다.

도3a 및 3b는 도2와 같은 공정에 의하여 형성된 다이패드의 단면도이다. 도 3a는 종래 하프에칭 리드프레임에 사용하던 다이패드의 단면도이며, 도3b는 본 발명에 따른 반도체 패키지에 사용하는 칩 실장 영역에 미세 돌기가 형성된 다이패드의 단면도이다. 도3a 및 3b를 참조하면, 하프에칭 공정에 의해 다이패드(111a, 111b)는 칩 실장 영역이 가장자리에 대하여 오목하게 포켓(114)으로 형성되고, 포켓(114)의 바닥면이 칩 실장면(116a, 116b)이 된다.

도3a의 다이패드(111a)는 다이패드 제작공정(도2)에서 에칭용액(염화철 용액)의 비중을 약 1.45로 설정한 경우이다. 1.45는 종래 다이패드 에칭시 일반적으로 사용되던 염화철 용액의 비중이며, 이경우 비교적 평탄한 영역의 칩 실장면(116a)이 형성된다. 도3b의 다이패드(111b)는 도3a의 다이패드(111a) 형성시보다 에칭용액의 비중을 높게 한 경우이다. 염화철 용액의 비중이 1.45보다 높을 경우 칩 실장면(116b)에 일정 높이의 미세 돌기(118)가 형성되며, 미세 돌기(118)의 높이(D)는 비중이 높을수록 커진다. 미세 돌기(118)의 높이(D)는 2~3μm정도가 바람직하며, 염화철 용액의 비중이 1.47인 경우 이정도 높이의 미세돌기(118)가 형성된다.

도 4a 및 4b는 도3a 및 3b의 칩 실장면(116a,116b)을 촬영한 SEM 사진이다.도 4a 및 4b를 참조하면, 에칭용액의 비중에 따라 칩 실장면(116a, 116b)의 거칠기가 달라짐을 알 수 있으며, 도 4b의 경우 다이패드(111b)의 칩 실장면(116b)에 미세 돌기(118)가 형성된 것을 관찰할 수 있다.

EX1012, Page 143

도5는 본 발명에 따른 다이패드에 미세 돌기가 형성된 반도체 패키지의 일실시예를 나타내는 단면도이다. 본 발명에 따른 반도체 패키지(100)는 미세 돌기(118)가 형성된 다이패드(111b)에 액상형 접착제(113)에 의하여 반도체 칩(115)이 부착되는 구조를 갖는다.

다이 패드(111b)는 도3b에 도시되어 있는 바와 같이 칩 실장면(116b)에 미세 돌기(118)가 형성되어 있다. 칩 실장면(116b)에 미세 돌기(118)를 형성함으로써 액상형 접착제(113)를 사용하여 반도체 칩(115)을 부착하는 경우 종래에 비하여 액상형 접착제(113)의 퍼짐 접합면(칩 실장면;116b)이 넓어지는 것을 알 수 있다. 또한 미세 돌기(118)에 의해 칩 실장면(116b)이 거칠어지기 때문에 액상형 접착제(113)의 흐름을 막을 수 있고, 따라서 고온 공정에서 액상형 접착제(113)의 유동성에 의한 치우침 현상을 감소시킬 수 있다.

반도체 칩(115)는 다이패드(111b)의 하프에칭 부위에 액상형 접착제(113)에 의하여 부착되며, 본딩 와이어(117)가 반도체 칩(115)과 리드(112)를 전기적으로 연결한다. 반도체 칩(115)와 본딩 와이어(117)의 보호를 위하여 다이패드(111b)의 하면과 리드(112)의 하면이 노출되도록 리드프레임(112'), 반도체 칩(115), 본딩 와이어(117)를 봉지한 수지 봉지부(119)가 형성된다.

본 발명의 실시예에서는 다이패드에 미세 돌기가 형성된 ELP만를 개시하였으나, 에칭면을 갖는 다이패드를 사용한 반도체 패키지라면 본 발명을 적용할 수 있다. 예를 들어, 종래 DDP에서도 칩 실장 면에 미세 돌기를 형성함으로써 본 발명의 적용이 가능하다.

발명의 효과

이상에서 살펴본 바와 같이 본 발명에 따른 다이패드에 미세 돌기가 형성된 반도체 패키지는 반도체 칩이 부착되는 칩 실장 영역에 미세 돌기를 형성함으로써, 반도체 칩과 다이패드간의 접착면적을 증가하여 반도체 칩과 다이패드간 접착력을 증가시킬 수 있다. 뿐만 아니라, 미세 돌기에 의하여 칩 실장 영역의 거칠기가 증가하여 액상형 접착제의 치우침에 의한 에폭시 보이드가 감소시킬 수 있으며 따라서 패키지의 신뢰성을 향상시킬 수 있다.

(57) 청구의 범위

청구항 1.

다이패드의 반도체 칩 실장면에 미세 돌기가 형성된 리드프레임;

상기 다이패드 위에 액상형 접착제에 의해 부착되는 반도체 칩;

상기 반도체 칩과 상기 리드프레임을 전기적으로 연결하는 연결수단; 및

상기 반도체 칩, 리드프레임 및 연결수단을 봉지하는 수지 봉지부를 포함하며,

상기 미세 돌기에 의해 반도체 칩과 다이패드 사이의 접착면적이 넓어지는 것을 특징으로 하는 다이패드에 미세 돌기가 형성된 반도체 패키지.

청구항 2.

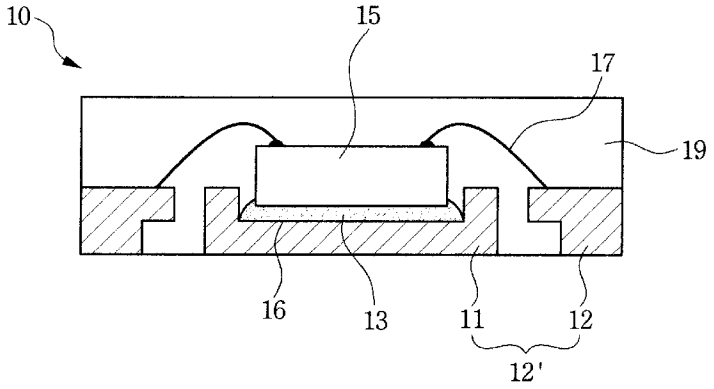
제1항에 있어서, 상기 반도체 칩 실장면은 하프에칭(Half-etching)에 의해 상기 다이패드의 가장자리 부분에 대해서 아래로 오목하게 형성된 포켓의 바닥면인 것을 특징으로 하는 다이패드에 미세 돌기가 형성된 반도체 패키지.

청구항 3.

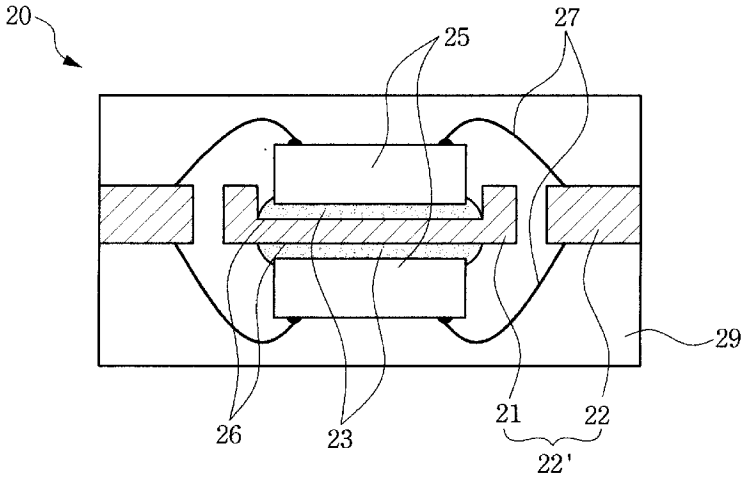
제 2항에 있어서, 상기 미세돌기는 반도체 칩 실장면의 가장 낮은 곳에 대하여 2~3μm 돌출된 것을 특징으로 하는 다이패드에 미세 돌기가 형성된 반도체 패키지.

도면

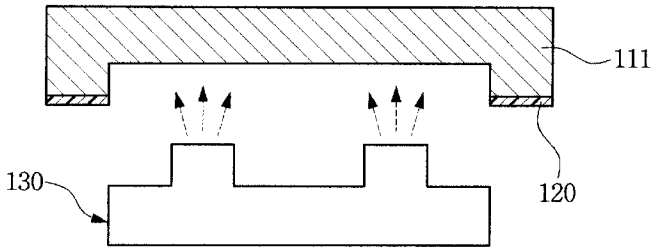
도면1a



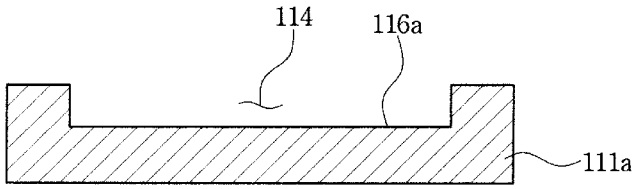
도면1b



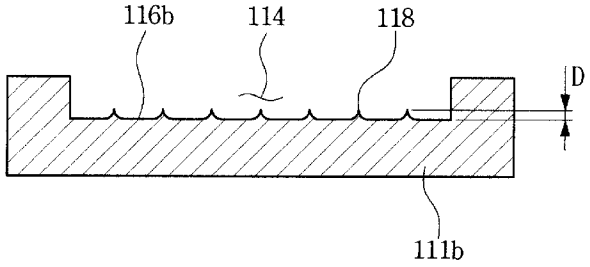
도면2



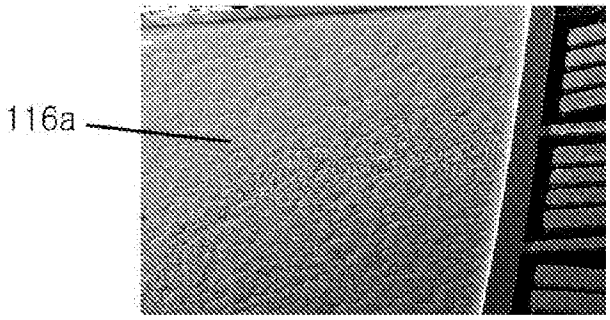
도면3a



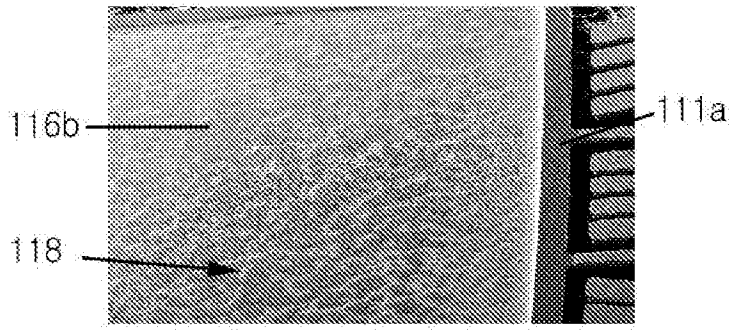
도면3b



도면4a



도면4b



도면5

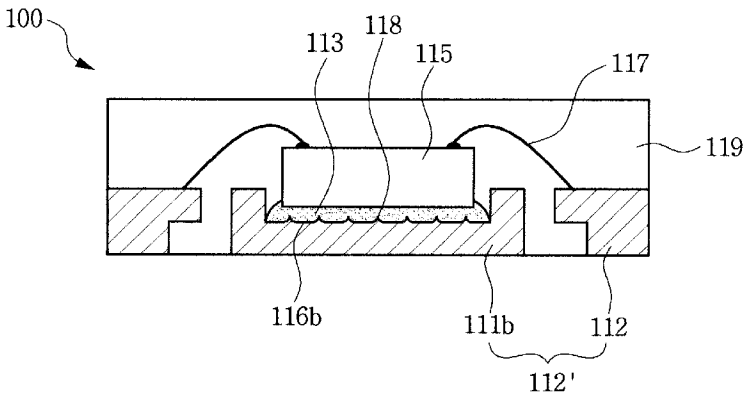


Fig.1

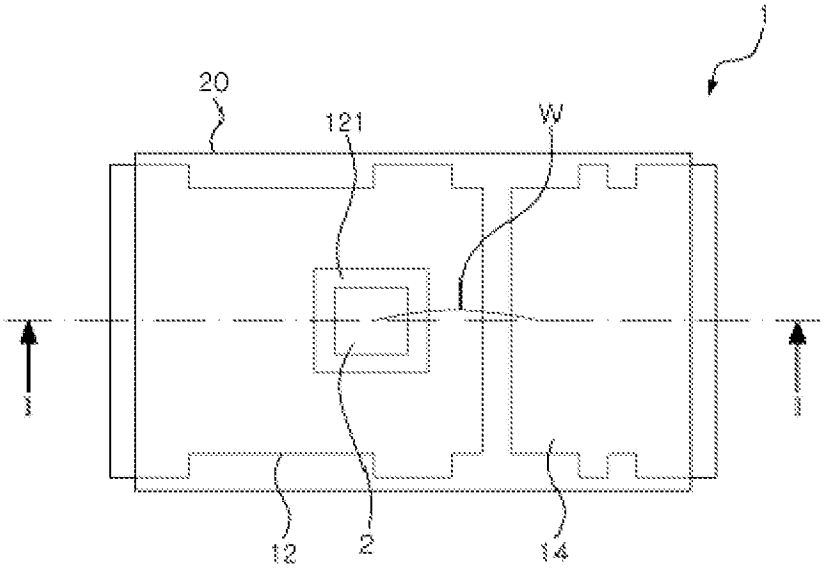


Fig.2

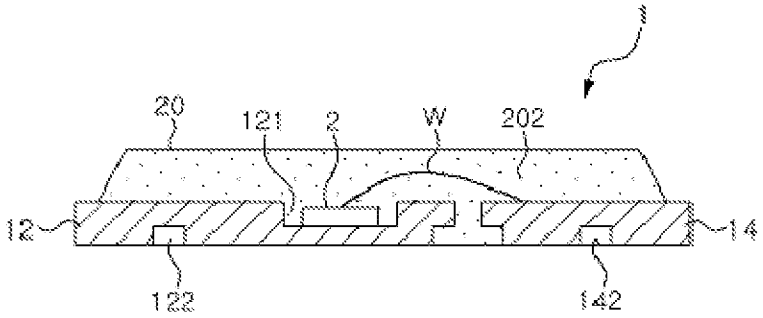


Fig.3

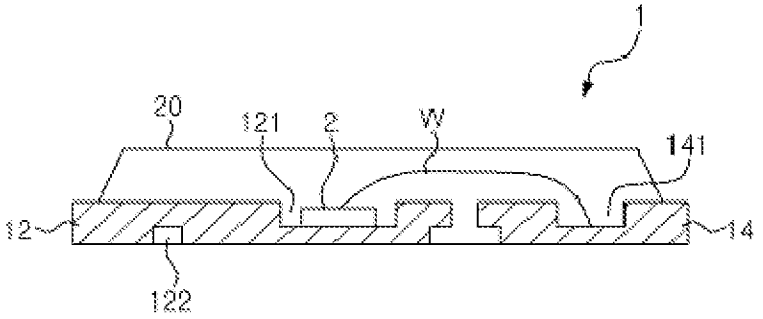


Fig.4

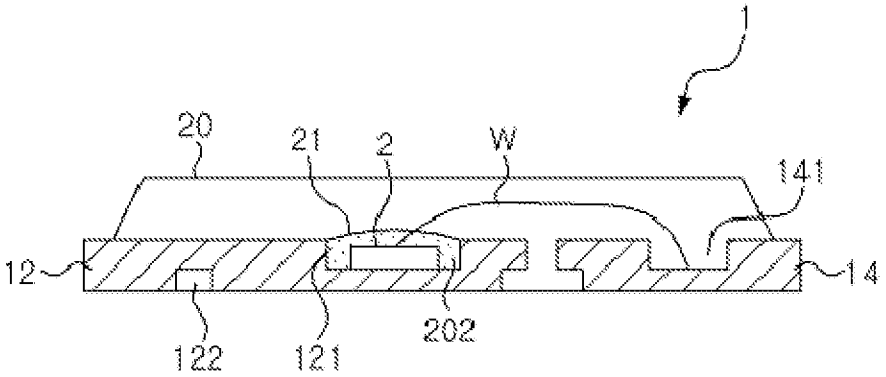


Fig.5

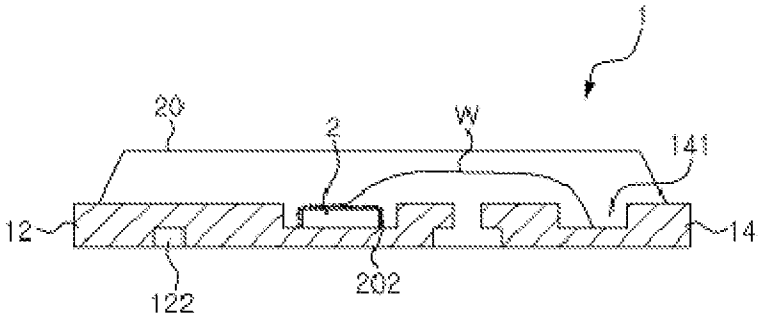

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202

Fig.6

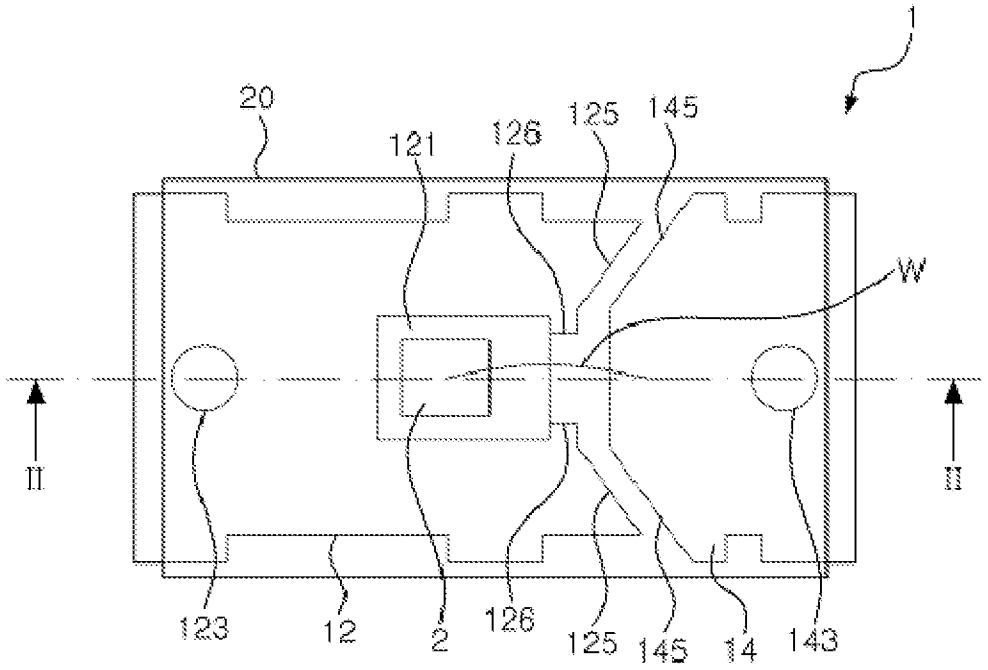
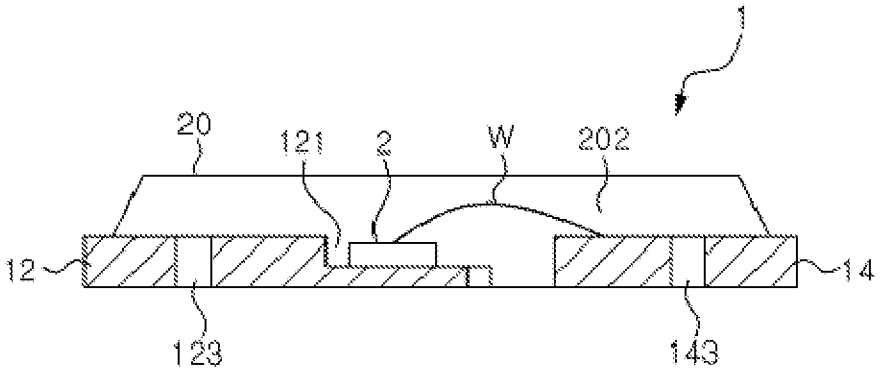

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Fig. 7



Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	SLIM LED PACKAGE
First Named Inventor/Applicant Name:	Eun Jung SEO
Filer:	Hae-Chan Park/Richard Schachner
Attorney Docket Number:	P3962US00

Filed as Large Entity

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
National Stage Fee	1631	1	330	330
National Stage Search - all other cases	1632	1	540	540
National Stage Exam - all other cases	1633	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1090**

Electronic Acknowledgement Receipt

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Application Number:	12745878
International Application Number:	PCT/KR08/06777
Confirmation Number:	4953
Title of Invention:	SLIM LED PACKAGE
First Named Inventor/Applicant Name:	Eun Jung SEO
Customer Number:	58027
Filer:	Hae-Chan Park/Richard Schachner
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P3962US00
Receipt Date:	02-JUN-2010
Filing Date:	
Time Stamp:	18:05:11
Application Type:	U.S. National Stage under 35 USC 371

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Payment Type	Credit Card
Payment was successfully received in RAM	$1090
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

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3	Transmittal of New Application	2010-06-02_P3962US00_PTO-1390.pdf	74291 bf130e1e0cc90c8ccd68a67ca03910e2be512d21	no	4
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4	Documents submitted with 371 Applications	2010-06-01_P3962US00_PCTApplicationasFiledinKorean.pdf	286732 61e04f2ca705aa594f1848f86e8090239d1c46b5	no	23
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Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	12
Claims	13	16
Abstract	17	17

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Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
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Assignee Name and Address

Seoul Semiconductor Co. Ltd,
148-29 Gasan-dong, Geumcheon gu,
Seoul, Republic of Korea

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SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	YCM YEASIN	Date	Aug 12, 2008
Name	YEASIN, YCM	Telephone	+82-10-4178-2184
Title	Director of IP & Legal Group		

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STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Eun Jung SEO

Application No./Patent No.: To be assigned Filed/Issue Date: June 2, 2010

Titled: SLIM LED PACKAGE

Seoul Semiconductor Co., Ltd. , a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;

2. ☐ an assignee of less than the entire right, title, and interest in (The extent (by percentage) of its ownership interest is _____ %); or

3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

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OR

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[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/hae-chan park/ June 2, 2010

Signature Date

Hae-Chan Park Attorney

Printed or Typed Name Title

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Attorney's Docket No.: P3952US00

ASSIGNMENT

Whereas, Assignor has invented certain new and useful processes, machines, articles of manufacture, compositions of matter, and/or improvements thereof ("Invention") disclosed in

☒ an application for United States Letters Patent entitled **SLIM LED PACKAGE** ("Application");

☐ upon which United States Letters Patent, Patent Number _____, has issued ("Patent");

Whereas, Assignor desires to convey all rights, titles, and interests in and to the same to:

Seoul Semiconductor Co., Ltd.
148-29, Gasan-dong, Geumcheon-gu
Seoul 158-801
Republic of Korea

Seoul Semiconductor Co., Ltd. herein further referred to as ("Assignee").

Now, for valuable consideration by Assignee to Assignor, the receipt of which is hereby acknowledged, and for other good and valuable consideration, Assignee and Assignor hereby agree as follows:

Assignor hereby conveys, assigns, sells and transfers to Assignee all rights, title and interests in and to the Invention disclosed in said application and in and to any Letters Patent of the United States (US), any continuation, division, renewal, or substitute thereof, and hereby grant to Assignee the right to apply in its own name for patents or Inventor's certificates and related rights heretofore or hereafter filed for the Invention in any and all countries, including (without limitation) all rights to claim priority based thereon, all patents granted thereon and all reissues, extensions and renewals thereof.

Assignor hereby covenants that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this Assignment.

Assignor further covenants that Assignee will, upon Assignee's request, be provided promptly with all pertinent facts and documents relating to the Invention, Patent, Application and any patents granted thereon, as may be known and accessible to Assignor, and Assignor will testify as to the same in any interference, litigation or proceeding related thereto and will promptly execute and deliver to Assignee or Assignee's legal representative any and all papers, instruments or affidavits required to apply for, protect, obtain, maintain, issue, defend and enforce the Application, Patent, Invention, whether in the US or any and all foreign countries and any patents granted thereon and/or for obtaining any reissue or reissues of any patent which may be granted for the invention and perform such further acts which may be necessary or desirable to

carry out the intent of this agreement as the Assignee thereof shall hereafter require and prepare at assignee's expense.

IN WITNESS WHEREOF, Assignor has hereunto set hand and seal.

First Inventor's Name: Eun Jung SEO

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Gyeonggi-do 425-851
Republic of Korea

First Inventor's Signature: 서 은 정

Date: 2010. 5. 21

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	SLIM LED PACKAGE

As the below named inventor(s), I/we declare that:

This declaration is directed to:

☒ The attached application having attorney docket number P3962US00, or

☐ Application No. _____ filed on _____

☐ As amended on _____ (if applicable);

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought;

I/we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

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All statements made herein of my/our own knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF INVENTOR(S)

Inventor one: Eun Jung SEO Date: 2010. 5. 27

Signature: _____ Citizen of: Republic of Korea

☐ Additional inventors or a legal representative are being name on ____ additional form(s) attached hereto.

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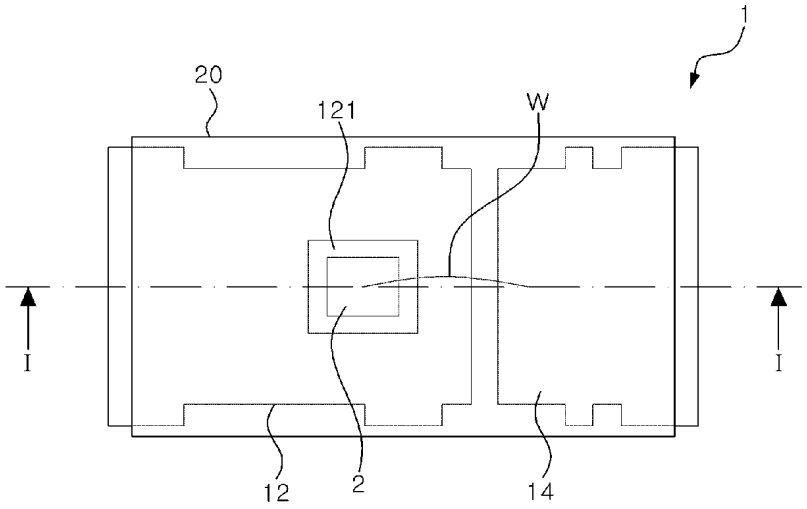
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(54) **Title:** SLIM LED PACKAGE

[Fig. 1]



(57) **Abstract:** Disclosed herein is a slim LED package. The slim LED package includes first and second lead frames separated from each other, a chip mounting recess formed on one upper surface region of the first lead frame by reducing a thickness of the one upper surface region below other upper surface regions of the first lead frame, an LED chip mounted on a bottom surface of the chip mounting recess and connected with the second lead frame via a bonding wire, and a transparent encapsulation material protecting the LED chip while supporting the first and second lead frames.

WO 2009/072757 A2

Description

SLIM LED PACKAGE

Technical Field

[1] The present invention relates to a light emitting diode (LED) package and, more particularly, to a slim LED package that is significantly reduced in thickness without substantially reducing luminescence efficiency or while improving the luminescence efficiency.

Background Art

[2] An LED emits light through recombination of electrons and holes by application of an electric current. An LED package means a package structure in which a light emitting diode chip, that is, an LED chip, is received. Many kinds of LED packages, particularly, a lead frame type LED package and a printed circuit board (PCB) type LED package, are well known in the art. The lead frame type LED package has a structure wherein a cavity of a housing for supporting a lead frame is filled with an encapsulation material, with the LED chip positioned in the cavity of the housing. The PCB type LED package has a structure wherein the LED chip is directly mounted on a PCB and covered with the encapsulation material.

[3] For the lead frame type LED package, the housing supporting the lead frame has an excessive thickness, which makes it difficult to fabricate a thin lead frame type LED package. On the other hand, since the PCB type LED package does not include a housing, it can be more easily fabricated to have a thin structure than the lead frame type LED package.

[4] However, there are many restrictions in thickness reduction of the PCB type LED package. In other words, since the thickness of the PCB type LED package is determined by thicknesses of the PCB and LED chips, and a loop height of a bonding wire even without considering the encapsulation material, it is difficult to achieve an overall thickness reduction and slimness of the PCB type LED package.

[5] Further, the encapsulation material of the LED package, which covers the LED chip, undergoes a yellowing phenomenon by energy generated from the LED chip emitting light. Such a yellowing phenomenon is a main cause of decreased luminescence performance and lifetime of the LED package. To overcome such problems, new LED packages have been developed to have a heat sink structure. In detail, the lead frame type LED package further includes a heat dissipation slug inserted into the housing by molding. Such a structure of the lead frame type LED package requires addition of components and a complicated manufacturing process, thereby decreasing economic feasibility. For the PCB type LED package, B-T resin on which the LED chip is

mounted has a low heat dissipation performance, and it is difficult to have the heat sink structure.

Disclosure of Invention

Technical Problem

[6] Therefore, an aspect of the present invention is to provide a slim LED package that is configured to allow a transparent encapsulation material to directly support a lead frame without a housing, that has a reduced overall thickness by reducing the thickness of a chip mounting region of the lead frame, and that exhibits good heat dissipation performance.

Technical Solution

[7] In accordance with an aspect of the present invention, a slim LED package includes: first and second lead frames separated from each other; a chip mounting recess formed on one upper surface region of the first lead frame by reducing a thickness of the one upper surface region below other upper surface regions of the first lead frame; an LED chip mounted on a bottom surface of the chip mounting recess and connected with the second lead frame via a bonding wire; and a transparent encapsulation material protecting the LED chip while supporting the first and second lead frames. The LED chip may have a thickness lower than or equal to a depth of the chip mounting recess.

[8] The chip mounting recess may be formed by thickness-etching the one upper surface region of the first lead frame. Herein, the term thickness-etching refers to etching performed to reduce the thickness of a material, that is, the thickness of the one upper surface region of the lead frame.

[9] The slim LED package may further include a bonding recess formed on one upper surface region of the second lead frame by reducing a thickness of the one upper surface region of the second lead frame below other upper surface regions of the second lead frame, one end of the bonding wire being bonded into the bonding recess. The bonding recess may be formed by thickness-etching the one upper surface region of the second lead frame.

[10] The slim LED package may further include openings or grooves formed on an upper or lower surface of the first or second lead frame to increase a bonding force between the first and second lead frames and the encapsulation material. Alternatively, the slim LED package may further include scratches formed on an upper or lower surface of the first or second lead frame to increase the bonding force between the first and second lead frames and the encapsulation material. Further, the LED chip may have a lower height than the depth of the chip mounting recess. The first and second lead frames may have opposite sides facing each other and including linear or rounded slant parts facing each other in a slanted state. At least one of the opposite sides may have a

depressed part formed thereon to widen a separation between the first lead frame and the second lead frame.

[11] The slim LED package may further include a phosphor in the encapsulation material. The slim LED package may further include an adjacent resin part formed in the chip mounting recess inside the encapsulation material, and the phosphor may be disposed in the adjacent resin part. Alternatively, the phosphor may be disposed in a resin constituting the encapsulation material or may be coated on the LED chip by conformal coating.

[12] The encapsulation material may be formed by transfer molding with a solid resin, particularly, a solid EMC. Alternatively, the encapsulation material may be formed by injection molding with a liquid resin.

Advantageous Effects

[13] According to one embodiment of the present invention, the LED package is configured to mount an LED chip on a chip mounting recess, which is formed on a predetermined region of a lead frame by reducing the thickness of the predetermined region, such that the thickness of the LED chip partially overlaps the thickness of the lead frame, whereby the LED package can be significantly reduced in overall thickness, achieving an ultrathin slimness. Further, the lead frame on which the LED chip is mounted and the lead frame with which a bonding wire is connected have a significantly increased area exposed to the bottom, so that the LED package has greatly improved thermal dissipation efficiency. Additionally, a bonding recess is formed on the lead frame by reducing the thickness of a part of the lead frame with which the bonding wire is connected, and is provided therein with a wire ball to be connected with the bonding wire. As a result, a factor causing an increase in thickness of the LED package can be eliminated, so that the LED package is further slimed. Further, according to one embodiment of the present invention, openings or grooves are formed on the lead frames to increase a bonding force between the lead frames and an encapsulation material, thereby preventing separation of an interfacial surface between the encapsulation material and the lead frames. Moreover, an inside surface of the chip mounting recess serves to improve luminescence efficiency, as compared to a conventional PCB type LED package that is configured to reflect light emitted from the LED chip to an upper side.

Brief Description of Drawings

[14] The above and other aspects, features and advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

[15] Fig. 1 is a plan view of a slim LED package according to one embodiment of the

present invention;

[16] Fig. 2 is a cross-sectional view taken line I-I of Fig. 1;

[17] Figs. 3 to 5 are cross-sectional views of slim LED packages according to various embodiments of the present invention;

[18] Fig. 6 is a cross-sectional view of a slim LED package according to yet another embodiment of the present invention; and

[19] Fig. 7 is a cross-sectional view taken along line II-II of Fig. 6.

Best Mode for Carrying out the Invention

[20] Exemplary embodiments of the present invention will be described in detail with reference to the accompanying drawings. The embodiments are given by way of illustration for complete understanding of the present invention by those skilled in the art. Hence, the present invention is not limited to these embodiments and can be realized in various forms. Further, for convenience of description, width, length, and thickness of components are not drawn to scale in the drawings. Like components are indicated by like reference numerals throughout the specification.

[21] Fig. 1 is a plan view of a slim LED package according to one embodiment of the invention, and Fig. 2 is a cross-sectional view taken line I-I of Fig. 1.

[22] Referring to Figs. 1 and 2, a slim LED package 1 of this embodiment includes first and second lead frames 12, 14 separated from each other. The first lead frame 12 has an LED chip 2 mounted thereon, and the second lead frame 14 is electrically connected with the LED chip 2 via a bonding wire W. The bonding wire W is connected with the second lead frame 14 via a wire ball or soldering ball (not shown).

[23] The first and second lead frames 12, 14 are supported by a transparent encapsulation material 20. The transparent encapsulation material 20 is formed to entirely cover and protect the LED chip 2 and bonding wire W by molding. The encapsulation material 20 may be formed by transfer molding with an epoxy molding compound that is a solid epoxy resin. For example, the transfer molding is performed by compressing epoxy molding compound (EMC) powder at a proper pressure into a tablet-shape, followed by positioning and molding the tablet-shaped EMC in a mould at high temperature and pressure conditions to form the encapsulation material 20.

[24] In this embodiment, the encapsulation material 20 is formed by transfer molding, but the present invention is not limited thereto. Alternatively, the encapsulation material 20 can be formed by injection molding, in which a liquid resin is injected into a mould. The encapsulation material 20 may be formed of other kinds of transparent resins such as epoxy-based or silicone-based resins, as well as the EMC.

[25] The first lead frame 12 is formed on an upper surface thereof with a chip mounting recess 121, which has the LED chip 2 mounted on a bottom surface thereof in a die-

attachment manner. The chip mounting recess 121 is formed by reducing the thickness of one upper surface region of the first lead frame 12 below other regions of the first lead frame 12, instead of bending the lead frame to form a reflection cup as in the prior art. Accordingly, the first lead frame 12 has a decreased thickness only in the region of the first lead frame 12 where the LED chip 2 is mounted, whereby a mounting height of the LED chip 2 is lowered to contribute to slimness of the LED package 1 through an overall thickness reduction of the LED package 1. Further, an inside surface of the chip mounting groove 121 serves as a reflector for reflecting light, thereby enhancing luminescence efficiency of the LED package 1.

[26] The chip mounting recess 121 may be formed by thickness-etching, which is performed for the purpose of reducing the thickness of the lead frame. At this time, etching can be performed, with the upper surface of the first lead frame 12 except for the chip mounting region covered with a mask. Further, the chip mounting recess 121 may have a thickness of about half of the thickness of the first lead frame 12. However, it should be noted that the present invention is not limited thereto.

[27] Further, the LED chip 22 may have a thickness less than or equal to the depth of the chip mounting recess 121 to prevent the height of the LED chip 2 from affecting a thickness increase of the LED package 1. In other words, it is desirable that the depth of the chip mounting recess 121 be set greater than or equal to the height of the LED chip 2.

[28] As clearly shown in Fig. 2, the first and second lead frames 12, 14 are respectively formed on lower surfaces thereof with grooves 122, 142, which are filled with a portion of the encapsulation material 20 during the molding process. As a result, the portion of the encapsulation material 20 engages with the grooves 122, 142, and a contact area between the lead frames 12, 14 and the encapsulation material 20 increases, thereby increasing a bonding force between the encapsulation material 20 and the lead frames. The grooves 122, 142 are also formed by reducing the thickness of predetermined regions of the lower surfaces of the first and second lead frames 12, 14, and preferably by thickness-etching as described above. Alternatively, instead of forming the openings or grooves, scratches may be formed on the upper or lower surfaces of the first and second lead frames to increase the bonding force between the lead frames and the encapsulation material.

[29] Referring again to Fig. 2, the encapsulation material 20 contains a phosphor 202 that is excited by light of a predetermined wavelength and emits light of a different wavelength. The phosphor 202 contributes to generation of white light through wavelength conversion by converting light emitted from the LED chip 2. In this embodiment, the phosphor 202 is mixed with a resin prepared as a molding material and is disposed in the encapsulation material 20 by the molding process using the

molding material. For example, when forming the encapsulation material 20 by transfer molding, a mixture of EMC and the phosphor 202 is prepared and used as the material for the transfer molding.

Mode for the Invention

[30] Next, various other embodiments of the present invention will be described. In description of the embodiments, a repetitious description will be omitted, and, the same or similar elements will be denoted by the same reference numerals as those of the above description.

[31] In Fig. 3, a bonding recess 141 is shown, which is formed by reducing the thickness of one upper surface region of a second lead frame 14 below the thickness of other regions thereof. The bonding recess 141 can also be formed by the thickness-etching as in the formation of the chip mounting recess 121 of the aforementioned embodiment. At this time, one end of a bonding wire W is connected with the second lead frame 14 within the bonding recess 141.

[32] Although not shown in the drawings, a wire ball is located in the bonding recess 141 such that the one end of the bonding wire W is connected with the wire ball in the bonding recess 141, thereby preventing a thickness increase of the LED package due to the height of the wire ball. A size increase of the wire ball ensures that the bonding wire W can be more rigidly secured to the first lead frame 14. Here, the formation of the bonding wire 141 enables more freedom to increase the size of the wire ball.

[33] Referring to Fig. 4, in another embodiment of the present invention, a resin 21 containing a phosphor 202 is restrictively provided in the chip mounting recess 121 to cover the LED chip 2 in an adjacent distance. Herein, the resin filling in the chip mounting recess 121 will be defined as an adjacent resin part. The adjacent resin part 21 prevents the phosphor 202 from being scattered within the encapsulation material 20, and allows the phosphor 202 to be located around the LED chip 21. This configuration can improve color conversion efficiency by the phosphor, and can provide light consisting of uniformly mixed colors when viewed outside the package.

[34] Alternatively, the adjacent resin part 21 may not contain the phosphors. For example, the encapsulation material such as epoxy is vulnerable to heat, and can cause thermal deformation or a yellowing phenomenon around the LED chip 2. Here, when the adjacent resin part 21 formed in the chip mounting recess 121 is made of a silicone resin, which is essentially invulnerable to heat, it is possible to efficiently prevent deterioration in performance or lifetime of the LED package caused by the yellowing phenomenon. When using the silicone as a material for the adjacent resin part 21 to prevent thermal deformation or the yellowing phenomenon, the phosphors 202 can be included in the adjacent resin part 21 or omitted therefrom without any influence on

the effect of preventing thermal deformation or the yellowing phenomenon.

[35] Alternatively, the phosphors 202 can be coated on the surface of the LED chip 2 by, for example, conformal coating via electrophoresis. In this case, the LED package 1 has a configuration as illustrated in Fig. 5.

[36] Fig. 6 is a cross-sectional view of a slim LED package according to yet another embodiment of the present invention, and Fig. 7 is a cross-sectional view taken along line II-II of Fig. 6.

[37] Referring to Figs. 6 and 7, instead of the grooves 122, 142 (see Fig. 2) of the above embodiment, first and second lead frames 12, 14 of this embodiment are formed with openings 123, 143, which penetrate the first and second lead frames 12, 14 in the vertical direction, to increase the bonding force between an encapsulation material 20 and the lead frames 12, 14. The openings 123, 143 can be formed by pressing or by etching the lead frames in the thickness direction.

[38] As clearly shown in Fig. 6, the first and second lead frames 12, 14 include first and second slant parts 125, 145, which are formed on opposite sides of the lead frames facing each other in an inclined state. That is, the first slant part 125 is formed on one side of the first lead frame 12 facing the other side of the second lead frame 14 to be inclined towards right and left sides of the first lead frame 12. Further, the second slant part 145 is formed on the other side of the second lead frame 14 facing the one side of the first lead frame 12 to be inclined towards right and left sides of the second lead frame 14. The first and second slant parts 125, 145 may have a linear or curved shape.

[39] A portion of the encapsulation material 20 is interposed between the opposite sides of the first and second lead frames 12, 14 facing each other, and a force is applied to the interposed portion of the encapsulation material 20 and the opposite sides of the first and second lead frames. At this time, the slant parts 125, 145 disperse the force diagonally, thereby preventing the encapsulation material 20 from being broken on the opposite sides of the lead frames. Furthermore, since the slant part 125 of the first lead frame 12 has a shape surrounding the portion of the encapsulation material 20 adjacent thereto, it serves to more rigidly hold the encapsulation material 20. It should be noted that the breakage of the encapsulation material 20 between the opposite sides of the lead frames causes electric short or the like.

[40] Additionally, a depressed part 126 is formed at the center of the one side of the first lead frame 12 facing the other side of the second lead frame to increase a separation between the first lead frame 12 and the second lead frame 14. The depressed part 126 is located directly below a path of the bonding wire W which connects the first lead frame 12 with the second lead frame 14. The depressed part 126 prevents the bonding wire W from being erroneously brought into contact with the lead frames 12, 14, and electric short of the bonding wire W caused by the erroneous contact.

[41] To fabricate the LED packages 1 as described above, a single metal sheet is processed to have a pattern of first and second lead frames 12, 14, followed by molding an encapsulation material on the patterned metal sheet. Then, the lead frames are sawed per each encapsulation material supporting a pair of first and second lead frames 12, 14, thereby providing a plurality of LED packages. At this time, a process of removing burrs formed during sawing may be further included.

[42] Although the present invention has been described with reference to the embodiments and the accompanying drawings, the present invention is not limited to these embodiments and the drawings. It should be understood that various modifications, additions and substitutions can be made by a person having ordinary knowledge in the art without departing from the scope and spirit of the invention, as defined only by the accompanying claims.

Claims

[1] A slim LED package comprising:
first and second lead frames separated from each other;
a chip mounting recess formed on one upper surface region of the first lead frame by reducing a thickness of the one upper surface region below other upper surface regions of the first lead frame;
an LED chip mounted on a bottom surface of the chip mounting recess and connected with the second lead frame via a bonding wire; and
a transparent encapsulation material protecting the LED chip while supporting the first and second lead frames.

[2] The slim LED package according to claim 1, wherein the chip mounting recess is formed by thickness-etching the one upper surface region of the first lead frame.

[3] The slim LED package according to claim 1, further comprising:
a bonding recess formed on one upper surface region of the second lead frame by reducing a thickness of the one upper surface region of the second lead frame below other upper surface regions of the second lead frame, one end of the bonding wire being bonded into the bonding recess.

[4] The slim LED package according to claim 3, wherein the bonding recess is formed by thickness-etching the one upper surface region of the second lead frame.

[5] The slim LED package according to claim 1, further comprising:
openings or recesses formed on an upper or lower surface of the first or second lead frame to increase a bonding force between the first and second lead frames and the encapsulation material.

[6] The slim LED package according to claim 1, wherein the LED chip has a lower height than a depth of the chip mounting recess.

[7] The slim LED package according to claim 1, wherein the first and second lead frames have opposite sides facing each other and comprising linear or rounded slant parts facing each other in a slanted state.

[8] The slim LED package according to claim 7, wherein at least one of the opposite sides has a depressed part formed thereon to widen a separation between the first lead frame and the second lead frame.

[9] The slim LED package according to claim 1, further comprising:
a phosphor in the encapsulation material.

[10] The slim LED package according to claim 9, further comprising:
an adjacent resin part formed in the chip mounting recess inside the encapsulation material, and the phosphor is disposed in the adjacent resin part .

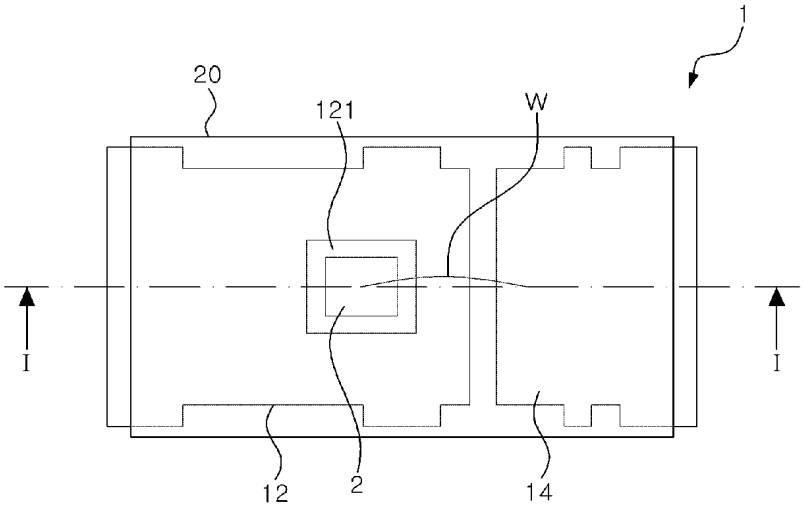
[11] The slim LED package according to claim 9, wherein the phosphor is disposed in a resin constituting the encapsulation material.

[12] The slim LED package according to claim 9, wherein the phosphor is coated on the LED chip by conformal coating.

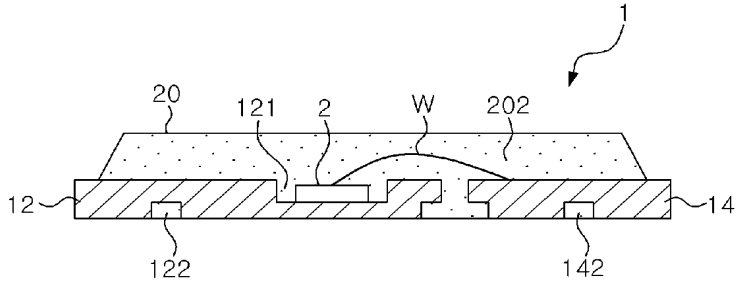
[13] The slim LED package according to claim 1, wherein the encapsulation material is formed by transfer molding.

[14] The slim LED package according to claim 1, further comprising:
scratches formed on an upper or lower surface of the first or second lead frame to increase a bonding force between the first and second lead frames and the encapsulation material.

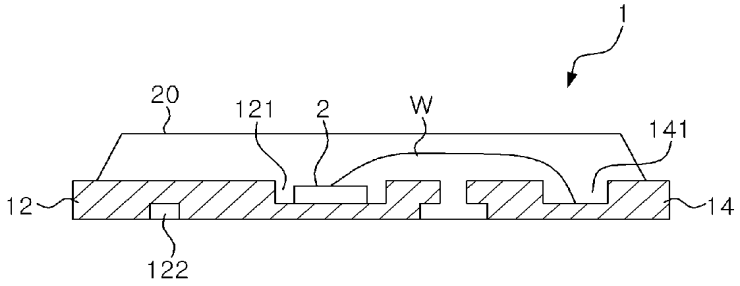
[Fig. 1]



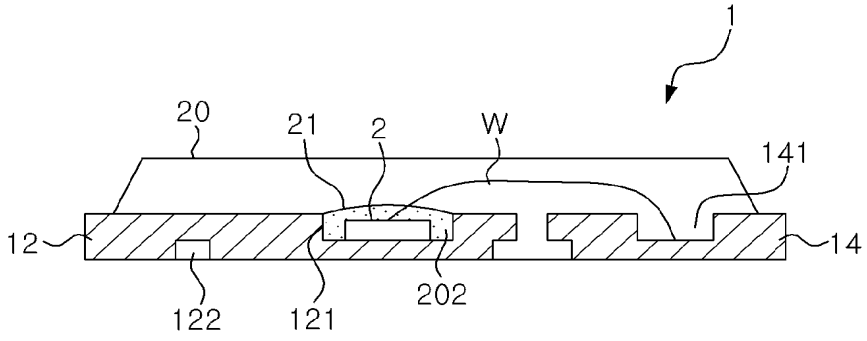
[Fig. 2]



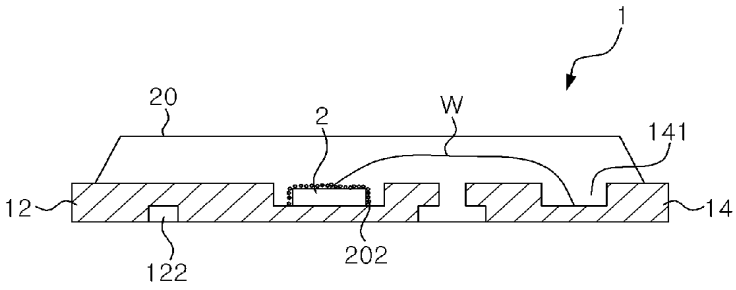
[Fig. 3]



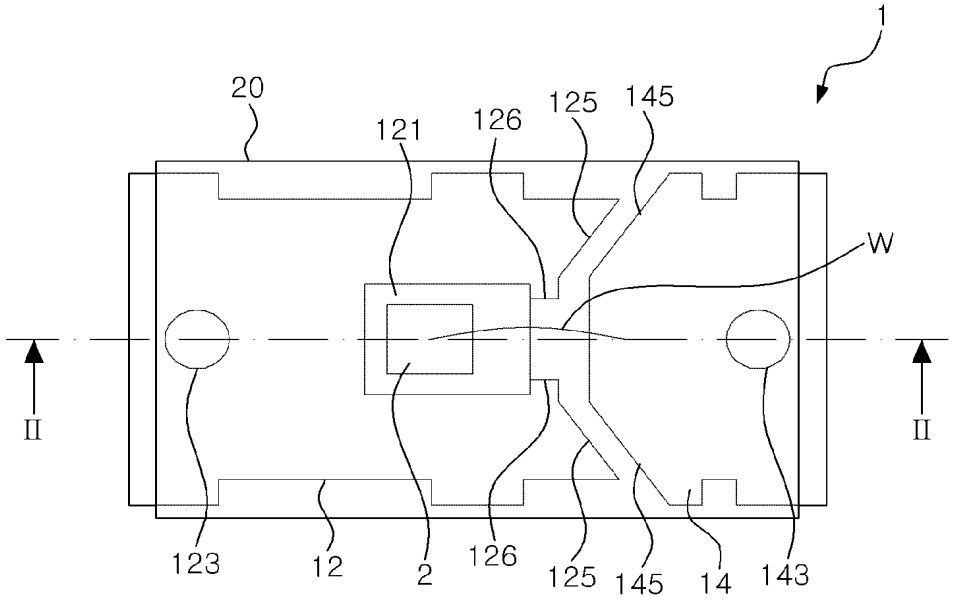
[Fig. 4]



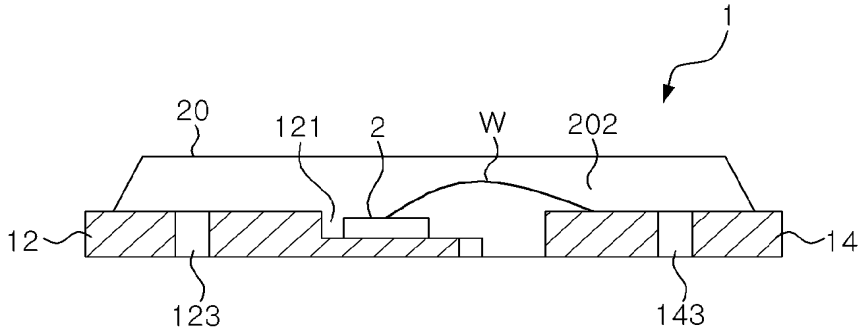
[Fig. 5]



[Fig. 6]



[Fig. 7]



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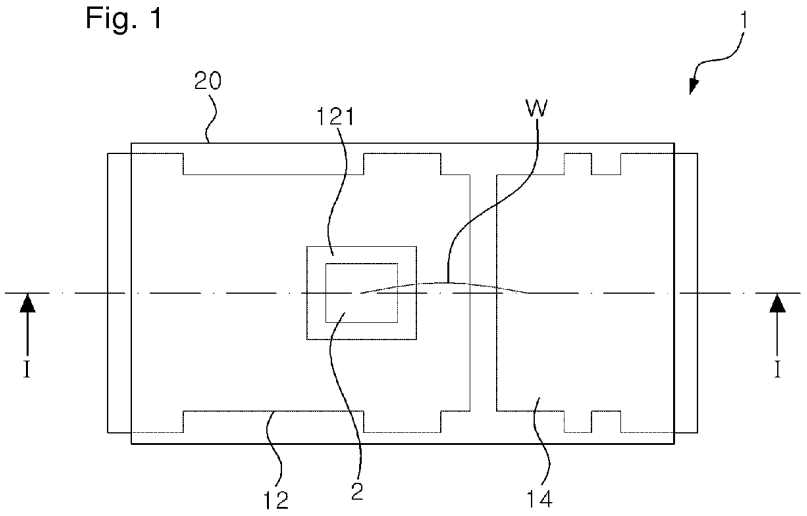
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Fig. 1



(57) Abstract: Disclosed herein is a slim LED package. The slim LED package includes first and second lead frames separated from each other, a chip mounting recess formed on one upper surface region of the first lead frame by reducing a thickness of the one upper surface region below other upper surface regions of the first lead frame, an LED chip mounted on a bottom surface of the chip mounting recess and connected with the second lead frame via a bonding wire, and a transparent encapsulation material protecting the LED chip while supporting the first and second lead frames.

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Applicant(s) SEOUL SEMICONDUCTOR CO.,LTD

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【발명의 영문명칭】 SLIM LED PACKAGE

2007-12-03

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【가산출원료】	19	면	0 원
【우선권주장료】	0	건	0 원
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【합계】 38,000 원

【요약서】

【요약】

여기에서는 슬림형 LED 패키지가 개시된다. 개시된 LED 패키지는, 서로 이격된 제 1 및 제 2 리드프레임과, 상기 제 1 리드프레임의 상면 일 영역에서 상기 제 1 리드프레임의 두께가 타 영역에 비해 감소되어 형성된 칩 실장홈과, 상기 칩 실장홈의 바닥면에 실장된 채, 본딩와이어에 의해 상기 제 2 리드프레임과 연결되는 LED칩과, 상기 제 1 및 제 2 리드프레임을 지지하도록 그리고 상기 LED칩을 보호하도록 형성된 투광성 봉지재를 포함한다.

【대표도】

도 1

【색인어】

리드프레임, 슬림, LED, 패키지, 칩 실장홈, 본딩와이어, 두께, 식각

【명세서】

【발명의 명칭】

슬림형 L E D 패키지{SLIM LED PACKAGE}

【발명의 상세한 설명】

【기술분야】

<1> 본 발명은 LED 패키지에 관한 것으로서, 더욱 상세하게는, 발광효율의 실질적인 저하 없이, 더 나아가서는, 발광 효율을 상승시키면서, 두께를 극소화한 슬림형 LED 패키지에 관한 것이다.

【배경기술】

<2> 발광다이오드(LED; Light Emitting Diode)는 전류 인가에 의해 p-n 반도체 접합(p-n junction)에서 전자와 정공이 만나 빛을 발하는 소자로서, 통상, LED칩이 탑재된 패키지의 구조로 제작된다. 기존의 LED 패키지로는, 리드프레임을 지지하는 하우징의 캐비티 내에 LED칩을 위치시키고, 그 하우징의 캐비티를 봉지재로 충전한 구조의 리드프레임 타임의 LED 패키지와, PCB 상에 직접 LED칩을 실장한 후, LED칩을 덮는 봉지재를 PCB 상에 형성한 PCB 타입의 LED 패키지가 알려져 있다.

<3> 리드프레임 타입 LED 패키지의 경우, 리드프레임을 지지하는 하우징의 두께가 상대적으로 너무 커서, 두께가 얇은 슬림형으로의 제작이 원천적으로 힘든 구조이다. 상대적으로, PCB 타입의 LED 패키지는, 하우징의 생략으로 인해, 기존 리드프레임 타입의 LED 패키지에 비해서는 두께를 얇게 하여 제작하는 것이 상대적으로 용이하다.

<4> 하지만, PCB 타입의 LED 패키지도 두께를 줄이는데 있어서 많은 제한적인 요소들을 갖고 있다. 즉, PCB 타입의 LED 패키지는, 봉지재를 고려하지 않고라도, 크기 감소에 큰 제한이 있는, PCB의 두께, LED칩의 두께 및 본딩와이어의 루프 높이(loop height)에 의해 두께가 정해지므로, 전체적으로 총 두께의 감소 및 그에 의한 슬림화가 어렵다.

<5> 또한, LED 패키지는 LED칩 동작시 발생한 에너지에 의해 그것을 덮는 봉지재에 열변 현상이 초래된다. 이러한 열변 현상은 LED 패키지의 발광 성능 및 수명을 저하시키는 주요 원인이 된다. 이러한 이유로 방열 구조를 채택한 LED 패키지가 개발되었는 바, 리드프레임 타입의 LED 패키지는 추가적인 부품인 방열슬러그를 하우징 내측에 삽입하여 몰딩하는 구조를 채택한다. 이는 부품 추가 및 복잡한 제조 공정을 요하므로 경제성이 떨어진다. PCB 타입의 LED 패키지는 LED칩이 실장되는 B-T 수지가 방열 성능이 떨어지는 재질이며, 더 나아가, 방열 구조를 추가하는 것도 어려웠다.

【발명의 내용】

【해결하고자 하는 과제】

<6> 따라서, 본 발명의 기술적 과제는, 하우징 없이 투광성 봉지재가 리드프레임을 직접 지지하도록 하고, 리드프레임의 칩 실장 영역의 두께를 줄여, 전체적으로 두께가 감소된 슬림형이며, 더 나아가, 방열 성능도 좋은 슬림형의 LED 패키지를 제공하는 것이다.

【과제 해결 수단】

<7> 본 발명의 일 측면에 따라, 서로 이격된 제 1 및 제 2 리드프레임과, 상기 제 1 리드프레임의 상면 일 영역에서 상기 제 1 리드프레임의 두께가 타 영역에 비해 감소되어 형성된 칩 실장홈과, 상기 칩 실장홈의 바닥면에 실장된 채, 본딩와이어에 의해 상기 제 2 리드프레임과 연결되는 LED칩과, 상기 제 1 및 제 2 리드프레임을 지지하도록 그리고 상기 LED칩을 보호하도록 형성된 투광성 봉지재를 포함하는 슬림형 LED 패키지가 제공된다. 이때, 상기 LED칩의 높이는 상기 칩 실장홈의 깊이 이하인 것이 바람직하다.

<8> 바람직하게는, 상기 칩 실장홈은 상기 제 1 리드프레임의 상면 일 영역을 두께 식각하여 형성된다. 본 명세서에서, 용어 '두께 식각'은 재료, 즉, 리드프레임의 일 영역의 두께를 줄이는 목적으로 행해지는 식각을 의미하는 것이다.

<9> 바람직하게는, 상기 제 2 리드프레임의 상면 일 영역에서 상기 제 2 리드프레임의 두께가 타 영역에 비해 감소되어 형성된 본딩홈을 더 포함하며, 상기 본딩홈 내로 상기 본딩와이어의 일단부가 본딩된다. 상기 본딩홈은 상기 제 2 리드프레임의 상면 일 영역을 두께 식각하여 형성될 수 있다.

<10> 상기 제 1 리드프레임 또는 상기 제 2 리드프레임의 상면 또는 저면에 형성되어 상기 제 1 및 제 2 리드프레임과 상기 봉지재와의 접합력을 크게 하는 구멍 또는 홈들을 더 포함할 수 있다. 대안적으로, 상기 구멍 또는 홈들 대신에 상기 제 1 및 제 2 리드프레임의 상면 또는 저면에 형성된 스크래치(scratch)들이 리드프레임과 봉지재의 접합력을 증가시키는데 기여할 수 있다. 또한, 상기 LED칩의 높이는 상기 칩 실장홈의 깊이 이하인 것이 바람직하다. 상기 제 1 및 제 2 리드프레임은

서로 마주하는 대향 측면들을 갖되, 상기 대향 측면들은 서로 경사진 상태로 마주하는 직선 또는 곡선형의 경사부들을 포함하는 것이 바람직하다. 상기 대향 측면들 중 적어도 하나의 대향 측면에는 상기 제 1 리드프레임과 상기 제 2 리드프레임의 이격 거리를 넓히는 오목부가 형성된 것이 바람직하다.

<11> 또한, 상기 봉지재의 내측에는 형광체가 제공되는 것이 바람직하다. 또한, 상기 봉지재 내측에서 상기 칩 실장홈 내에 형성된 근접 수지부를 더 포함하며, 상기 형광체는 상기 근접 수지부 내에 개재된 것이 바람직하다. 대안적으로, 상기 형광체는 상기 봉지재를 구성하는 수지 내에 개재되거나, 상기 LED칩 상에 컨포멀 코팅에 의해 형성될 수도 있다.

<12> 상기 봉지재는 고상의 수지, 특히, 고상의 EMC를 이용한 트랜스퍼 몰딩에 의해 형성되는 것이 바람직하지만, 액상 수지를 이용한 인젝션 몰딩에 의해서도 형성될 수 있다.

【효과】

<13> 본 발명에 따르면, 두께를 감소시켜 형성된 리드프레임의 칩 실장홈에 LED칩을 실장하는 방식으로, LED칩의 두께와 리드프레임의 두께 일부가 중첩되게 하여, LED 패키지의 전체 두께를 크게 줄일 수 있고, 이에 의해, 초박형으로 슬림화된 LED 패키지를 얻을 수 있다. 또한, LED칩이 실장되는 리드프레임과 본딩와이어가 연결되는 리드프레임이 하우징 없이 바닥으로 노출되는 면적이 크게 증가되어 방열성능이 크게 향상된 LED 패키지를 얻을 수 있다. 또한, 본딩와이어가 연결되는 리드프레임에도 두께를 감소시켜 형성된 본딩홈을 형성하고, 그 본딩홈 내에 본딩와

이어가 연결되는 와이어볼을 마련하는 구조에 의해, LED 패키지의 두께 증가 원인을 더 줄이며, 이에 의하면, 보다 더 슬림화된 LED 패키지를 얻을 수 있다. 또한, 본 발명의 실시예에 따르면, 리드프레임에 형성된 구멍 또는 홈에 의해 리드프레임과 봉지재와의 접합력을 크게 해줄 수 있으며, 이는 봉지재와 리드프레임 사이에서 일어날 수 있는 계면 박리 현상을 막아준다. 또한, 상기 칩 실장홈의 내측면은 LED 칩으로부터 나온 광을 상측으로 반사시키는 기존 PCB 타입의 LED 패키지에 비해 발광효율을 향상시키는데 기여한다.

【발명의 실시를 위한 구체적인 내용】

<14> 이하, 첨부한 도면들을 참조하여 본 발명의 실시예들을 상세히 설명하기로 한다. 다음에 소개되는 실시예들은 당업자에게 본 발명의 사상이 충분히 전달될 수 있도록 하기 위해 예로서 제공되는 것이다. 따라서, 본 발명은 이하 설명되는 실시예들에 한정되지 않고 다른 형태로 구체화될 수도 있다. 그리고, 도면들에 있어서, 구성요소의 폭, 길이, 두께 등은 편의를 위하여 과장되어 표현될 수 있다. 명세서 전체에 걸쳐서 동일한 참조번호들은 동일한 구성요소들을 나타낸다.

<15> 도 1은 본 발명의 일 실시예에 따른 슬림형 LED 패키지를 도시한 평면도이며, 도 2는 도 1의 I-I를 따라 취해진 단면도이다.

<16> 도 1 및 도 2에 도시된 바와 같이, 본 실시예에 따른 슬림형 LED 패키지(1)는, 서로 이격된 제 1 및 제 2 리드프레임(12, 14)을 포함한다. 상기 제 1 리드프레임(12)에는 LED칩(2)이 실장되며, 상기 제 2 리드프레임(14)은 본딩와이어(W)에

의해 상기 LED칩(2)과 전기적으로 연결된다. 상기 본딩와이어(W)는 도시되지 않은 와이어볼(또는, 솔더링볼)에 의해 상기 제 2 리드프레임(14)에 연결된다.

<17> 상기 제 1 및 제 2 리드프레임(12, 14)은 투광성 봉지재(20)에 의해 지지된다. 상기 투광성 봉지재(20)는, 몰딩 성형에 의해 형성되는 것으로, LED칩(2)과 본딩와이어(W)를 전체적으로 덮어, 그것들을 보호하는 역할을 한다. 상기 투광성 봉지재(20)는 고상의 에폭시 수지재인 EMC(Epoxy Molding Compound)를 이용한 트랜스퍼 몰딩(transfer molding)에 의해 형성될 수 있다. 예컨대, 트랜스퍼 몰딩은 파우더형 EMC 재료를 적절한 압력으로 가압하여 태블릿(tablet) 형태로 만들고, 그 태블릿 형태의 EMC를 고온, 고압 조건으로 봉지재(20)의 형태를 한정하는 금형에 주입하는 방식으로 이루어진다.

<18> 그러나, 상기 봉지재(20)는 트랜스퍼 몰딩에 의해 형성되는 것이 바람직하지만, 이에 반드시 한정되는 것은 아니며, 액상 수지를 금형에 주입하여 봉지재를 형성하는 인젝션 몰딩이 이용될 수도 있다. 또한, 상기 봉지재(20)의 재질로는 에폭시 수지 외에 실리콘 수지 등의 다른 투광성 수지가 이용될 수 있다.

<19> 상기 제 1 리드프레임(12)의 상면에는 칩 실장홈(121)이 형성되며, 상기 LED칩(2)은 상기 칩 실장홈(121)의 바닥면에 다이 어태칭 방식으로 실장된다. 상기 칩 실장홈(121)은, 기존 리드프레임의 반사컵 형성을 위해 이용되는 절곡 방식으로 형성되는 홈이 아니며, 제 1 리드프레임(12)의 상면 일 영역에서 타 영역에 비해 두께를 감소시켜 형성되는 홈이다. 따라서, 상기 LED칩(2)이 실장되는 부분에 국한하여 상기 제 1 리드프레임(12)의 두께가 감소되며, 이는 LED칩(2)의 실장 높이를 줄

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여 LED 패키지(1)의 전체 두께를 줄이는 슬림화에 기여한다. 또한, 상기 칩 실장홈(121)의 내측면은 광을 반사시키는 리플렉터(reflector)로서의 기능을 하여 LED 패키지(1)의 발광 효율 향상에도 기여할 수 있다.

<20> 바람직하게는, 상기 칩 실장홈(121)은 리드프레임의 두께를 줄일 목적으로 수행되는 두께 식각에 의해 형성된다. 이때, 상기 식각은 LED칩(2)의 실장 영역을 제외한 제 1 리드프레임(12)의 상면을 마스크로 가린 후 수행될 수 있다. 또한, 상기 칩 실장홈(121)의 깊이는 상기 제 1 리드프레임(12) 두께의 대략 1/2인 것이 바람직하나 이는 본 발명을 한정하는 것은 아니다.

<21> 또한, 상기 LED칩(2)의 높이가 상기 LED 패키지(1)의 두께 증가에 어떠한 영향도 미치지 않도록, 상기 LED칩(2)은 상기 칩 실장홈(121)의 깊이 이하로 그 높이가 정해지는 것이 바람직하다. 달리 말하면, 상기 칩 실장홈(121)의 깊이가 상기 LED칩(2) 이상으로 정해지는 것이 바람직하다.

<22> 도 2에 잘 도시된 바와 같이, 상기 제 1 및 제 2 리드프레임(12, 14)의 저면 각각에는 홈들(122, 142)이 형성되며, 그 홈들(122, 142)에는 몰딩 성형 중에 상기 봉지재(20)의 일부가 메워진다. 이는 상기 홈(122, 142)과 상기 봉지재(20)의 일부가 맞물리는 효과 및 리드프레임(12, 14)과 봉지재(20) 사이의 접합 면적을 증가시키는 효과를 제공하여, 리드프레임에 대한 봉지재(20)의 접합력을 증가시키는데 기여한다. 상기 홈들(122, 142) 또한 상기 제 1 및 제 2 리드프레임(12, 14)의 저면 일부 영역의 두께를 감소시키는 방식으로 형성되며, 가장 바람직하게는, 전술한 것과 같은 두께 식각에 의해 형성될 수 있다. 또한, 상기 구멍 또는 홈들 대신에 상

기 제 1 및 제 2 리드프레임의 상면 또는 저면에 형성된 스크래치(scratch)들이 리드프레임과 봉지재의 접합력을 증가시키는데 기여할 수 있다.

<23> 도 2를 더 참조하면, 상기 봉지재(20) 내에는 특정 파장의 광에 의해 여기되어 다른 파장의 광을 발하는 형광체(202)가 개재된다. 상기 형광체(202)는 LED칩(2)으로부터 나온 광의 색 변환 및 그 색 변환을 통해 백색광을 만들어내는데 참여한다. 본 실시예에서, 상기 형광체(202)는 몰딩 재료인 수지와 혼합된 후 그 몰딩 재료에 의한 몰딩 성형 공정에 의해 상기 봉지재(20) 내에 개재될 수 있다. 예컨대, 트랜스퍼 몰딩에 의한 봉지재(20)의 형성의 경우, EMC와 형광체(202)가 미리 혼합되며, 그 혼합된 재료가 트랜스퍼 몰딩의 재료로 이용된다.

<24> 이하에서는, 본 발명의 여러가지 다른 실시예들에 대한 설명이 이루어진다. 그러한 실시예들을 설명함에 있어서, 앞에서 설명된 내용은 중복을 피하기 위해 생략되며, 앞선 실시예와 동일한 부재번호는 동일한 또는 유사한 구성요소를 나타낸다.

<25> 도 3을 참조하여 본 발명의 다른 한 실시예를 설명하면, 제 2 리드프레임(14)의 상면 일 영역에서 상기 제 2 리드프레임(14)의 두께를 타 영역에 비해 감소시켜 형성된 본딩홈(141)을 볼 수 있다. 상기 본딩홈(141)도 앞선 실시예의 칩 실장홈(121)과 마찬가지로 두께 식각에 의해 형성될 수 있다. 이때, 본딩와이어(W)의 일단부는 상기 본딩홈(141) 내에서 상기 제 2 리드프레임(14)과 연결된다.

<26> 도시하지는 않았지만, 상기 본딩와이어(W)가 본딩되는 일단부에는 와이어볼이 존재하는데, 상기 본딩홈(141)은 와이어볼의 높이에 따른 LED 패키지의 두께 증가를 막아준다. 또한, 와이어볼의 크기가 클수록 본딩와이어(W)가 견고하게 제 1 리드프레임(14)에 고정될 수 있는데, 상기 본딩홈(141)의 형성으로 인해, 상기 와이어볼의 크기를 증가시키는데 있어서의 제한이 감소될 수 있다.

<27> 도 4를 참조하여 본 발명의 다른 한 실시예를 설명하면, 형광체(202)가 포함된 수지(21)가 칩 실장홈(121) 내에 한정적으로 형성되어 상기 LED칩(2)을 근접 거리에서 덮고 있다. 본 명세서에서, 칩 실장홈(121) 내에 채워진 수지를 '근접 수지부'라 정의한다. 상기 근접 수지부(21)는 형광체(202)가 상기 봉지재(20) 내에서 산재하지 않고, LED칩(21) 주변에만 한정적으로 위치할 수 있도록 해준다. 이는 형광체(202)에 의한 색 변환 효율을 높여주며, 패키지 외측에서 볼 때 균일하게 색 혼합된 광을 얻을 수 있도록 해준다.

<28> 덧붙여, 상기 근접 수지부(21)는 상기 형광체가 포함되지 않은 것도 고려될 수 있다. 예컨대, 에폭시와 같은 봉지재 재질은, 열에 취약하므로, LED칩(2) 주변에서 열변 또는 황변 현상을 일으킬 수 있다. 이때, 상기 칩 실장홈(121) 내에 형성된 근접 수지부(21)를 열에 상대적으로 강한 실리콘 수지로 하면, 전술한 열변 또는 황변 현상에 의한 LED 패키지의 성능 또는 수명 저하를 크게 줄여줄 수 있다. 열변 또는 황변 현상을 방지할 목적으로, 실리콘을 근접 수지부(21)의 재료로 이용하는 경우, 형광체(202)가 포함될 수도 있지만, 그것을 생략하더라도, 열변 또는

황변의 방지 측면에서, 충분한 효과를 제공한다.

<29> 대안적으로, 상기 형광체(202)를 예를 들면, 전기 영동법에 의한 컨포멀 코팅(conformal coating) 방식으로, 상기 LED칩(2) 표면에 형성하는 것도 고려될 수 있으며, 이러한 사항을 포함하는 LED 패키지(1)의 구조는 도 5에 도시하였다.

<30> 도 6은 본 발명의 또 다른 실시예에 따른 슬림형 LED 패키지의 평면도이고, 도 7은 도 6의 II-II를 따라 취해진 단면도이다.

<31> 도 6 및 도 7을 참조하면, 봉지재(20)와 리드프레임(12, 14) 사이의 접합력을 크게 하기 위해, 상기 제 1 및 제 2 리드프레임(12, 14)은, 앞선 실시예의 홈(122, 142; 도 2 참조)들 대신에, 상기 제 1 및 제 2 리드프레임(12, 14)을 상하로 관통하는 구멍(123, 143)들을 구비한다. 상기 구멍(123, 143)들은, 프레스 가공에 의해 형성될 수 있으며, 또한, 리드프레임의 전체 두께에 대한 식각 가공에 의해 형성될 수도 있다.

<32> 도 6에 잘 도시된 바와 같이, 상기 제 1 및 제 2 리드프레임(12, 14)은, 서로 마주하는 대향 측면들에서, 서로 경사진 상태로 마주하고 있는 제 1 및 제 2 경사부(125, 145)를 포함한다. 상기 제 1 경사부(125)는 제 1 리드프레임(12)의 대향 측면에서 좌우 양측으로 벌어진 채 경사진 구조로 형성되어 있다. 또한, 상기 제 2 경사부(145)는 제 2 리드프레임(14)의 대향 측면에서 좌우 양측으로 벌어진 채 경사진 구조로 형성되어 있다. 또한 상기 제 1 및 제 2 경사부(125, 145)는 직선형이거나 곡선형일 수 있다.

<33> 상기 제 1 및 제 2 리드프레임(12, 14)의 대향 측면들 사이에는 봉지재(20)의 일부가 개재되는데, 그 개재된 봉지재(20)와 상기 대향 측면들 상에는 힘이 작용한다. 이때, 상기 경사부(125, 145)들은 힘을 경사지게 분산시켜 상기 봉지재(20)가 대향 측면상에서 파손될 위험성이 있다. 더 더욱이, 제 1 리드프레임(12)의 경사부(125)는, 그와 인접하는 봉지재(20) 일부를 감싸는 형상이므로 보다 견고하게 봉지재(20)를 잡아주는 역할을 할 수 있다. 상기 대향 측면들 사이에서의 봉지재(20) 파손은 숏트(short) 등의 위험을 야기한다는 것에 주목한다.

<34> 또한, 상기 제 1 리드프레임(12)의 대향 측면 중앙에는 상기 제 1 리드프레임(12)과 상기 제 2 리드프레임(14)의 이격 거리를 넓히는 효과를 제공하는 오목부(126)가 형성된다. 상기 오목부(126)는 본딩와이어(W)가 상기 제 1 리드프레임(12)과 상기 제 2 리드프레임(14)을 연결하는 경로 바로 아래쪽에 위치한다. 상기 오목부(126)는 본딩와이어(W)가 리드프레임(12, 14)들에 의해 잘못 접촉되는 것과, 그 잘못된 접촉에 의해 야기될 수 있는 본딩와이어(W)의 숏트를 막아준다.

<35> 전술한 슬림형 LED 패키지(1)는 하나의 큰 금속박판을 다수의 제 1 및 제 2 리드프레임(12, 14)을 갖는 형상으로 패턴 가공하고, 그 패턴 가공된 금속박판 상에 다수의 봉지재를 형성하는 몰딩 성형을 하고, 다음, 제 1 및 제 2 리드프레임(12, 14)을 지지하는 봉지재 단위로, 리드프레임들을 절단(sawing)하는 것에 의해, 다수의 개수로 제작될 수 있다. 이때, 상기 절단시 생긴 버(burr)를 제거하는 공정이 포함될 수 있다.

【특허청구범위】

【청구항 1】

서로 이격된 제 1 및 제 2 리드프레임;

상기 제 1 리드프레임의 상면 일 영역에서 상기 제 1 리드프레임의 두께가 타 영역에 비해 감소되어 형성된 칩 실장홈;

상기 칩 실장홈의 바닥면에 실장된 채, 본딩와이어에 의해 상기 제 2 리드프레임과 연결되는 LED칩; 및

상기 제 1 및 제 2 리드프레임을 지지하도록 그리고 상기 LED칩을 보호하도록 형성된 투광성 봉지재를 포함하는 슬림형 LED 패키지.

【청구항 2】

청구항 1에 있어서, 상기 칩 실장홈은 상기 제 1 리드프레임의 상면 일 영역을 두께 식각하여 형성된 것을 특징으로 하는 슬림형 LED 패키지.

【청구항 3】

청구항 1에 있어서, 상기 제 2 리드프레임의 상면 일 영역에서 상기 제 2 리드프레임의 두께가 타 영역에 비해 감소되어 형성된 본딩홈을 더 포함하며, 상기 본딩홈 내로 상기 본딩와이어의 일단부가 본딩되는 것을 특징으로 하는 슬림형 LED 패키지.

【청구항 4】

청구항 3에 있어서, 상기 본딩홈은 상기 제 2 리드프레임의 상면 일 영역을

두께 식각하여 형성된 것을 특징으로 하는 슬림형 LED 패키지.

【청구항 5】

청구항 1에 있어서, 상기 제 1 리드프레임 또는 상기 제 2 리드프레임의 상면 또는 저면에 형성되어, 상기 제 1 및 제 2 리드프레임과 상기 봉지재와의 접합력을 크게 하는 구멍 또는 홈들을 더 포함하는 것을 특징으로 하는 슬림형 LED 패키지.

【청구항 6】

청구항 1에 있어서, 상기 LED칩의 높이는 상기 칩 실장홈의 깊이 이하인 것을 특징으로 하는 슬림형 LED 패키지.

【청구항 7】

청구항 1에 있어서, 상기 제 1 및 제 2 리드프레임은 서로 마주하는 대향 측면들을 갖되, 상기 대향 측면들은 서로 경사진 상태로 마주하는 직선 또는 곡선형의 경사부들을 포함하는 것을 특징으로 하는 슬림형 LED 패키지.

【청구항 8】

청구항 7에 있어서, 상기 대향 측면들 중 적어도 하나의 대향 측면에는 상기 제 1 리드프레임과 상기 제 2 리드프레임의 이격 거리를 넓히는 오목부가 형성된 것을 특징으로 하는 슬림형 LED 패키지.

【청구항 9】

청구항 1에 있어서, 상기 봉지재의 내측에는 형광체가 제공된 것을 특징으로 하는 슬림형 LED 패키지.

【청구항 10】

청구항 9에 있어서, 상기 봉지재 내측에서 상기 칩 실장홈 내에 형성된 근접 수지부를 더 포함하며, 상기 형광체는 상기 근접 수지부 내에 개재된 것을 특징으로 하는 슬림형 LED 패키지.

【청구항 11】

청구항 9에 있어서, 상기 형광체는 상기 봉지재를 구성하는 수지 내에 개재된 것을 특징으로 하는 슬림형 LED 패키지.

【청구항 12】

청구항 9에 있어서, 상기 형광체는 상기 LED칩 상에 컨포멀 코팅에 의해 형성된 것을 특징으로 하는 슬림형 LED 패키지.

【청구항 13】

청구항 1에 있어서, 상기 봉지재는 트랜스퍼 몰딩에 의해 형성된 것을 특징으로 하는 슬림형 LED 패키지.

【청구항 14】

청구항 1에 있어서, 상기 제 1 리드프레임 또는 상기 제 2 리드프레임의 상면 또는 저면에 형성되어, 상기 제 1 및 제 2 리드프레임과 상기 봉지재와의 접합력을 크게 하는 스크래치를 더 포함하는 것을 특징으로 하는 슬림형 LED 패키지.

【도면의 간단한 설명】

<36> 도 1은 본 발명의 일 실시예에 따른 슬림형 LED 패키지의 평면도.

<37> 도 2는 도 1의 I-I를 따라 취해진 단면도.

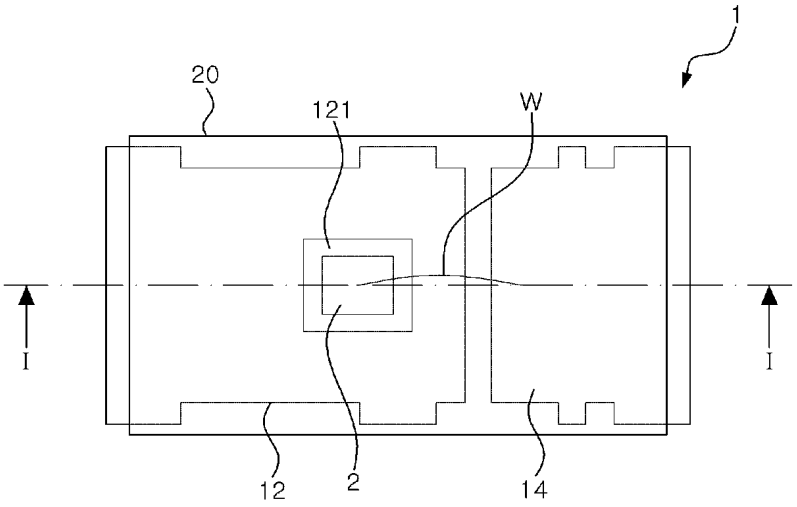
<38> 도 3 내지 도 5는 본 발명의 다양한 다른 실시예들을 설명하는 단면도들.

<39> 도 6은 본 발명의 또 다른 실시예에 따른 슬림형 LED 패키지의 평면도.

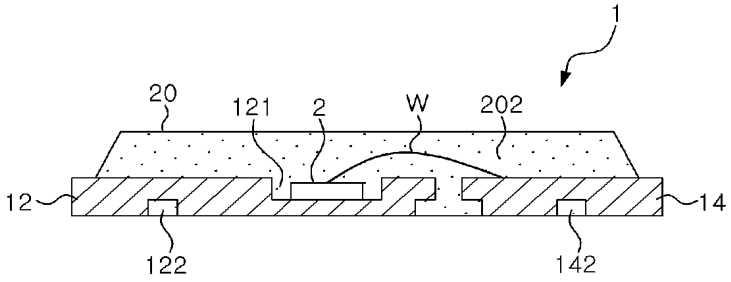
<40> 도 7은 도 6의 II-II를 따라 취해진 단면도.

【도면】

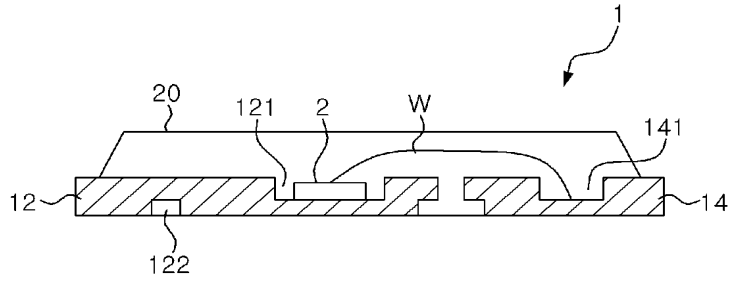
【도 1】



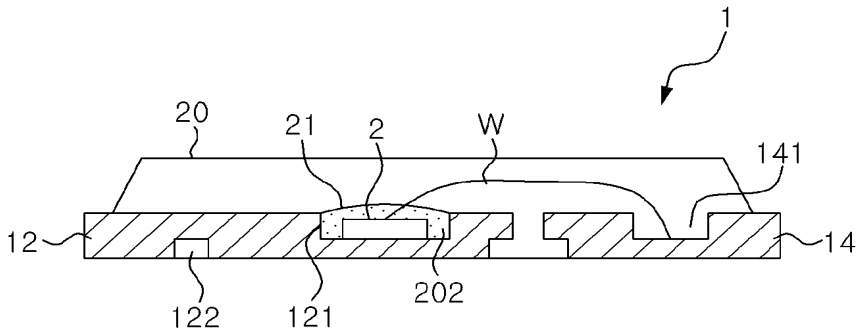
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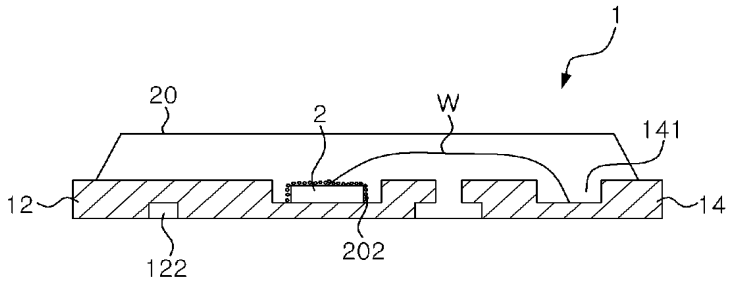
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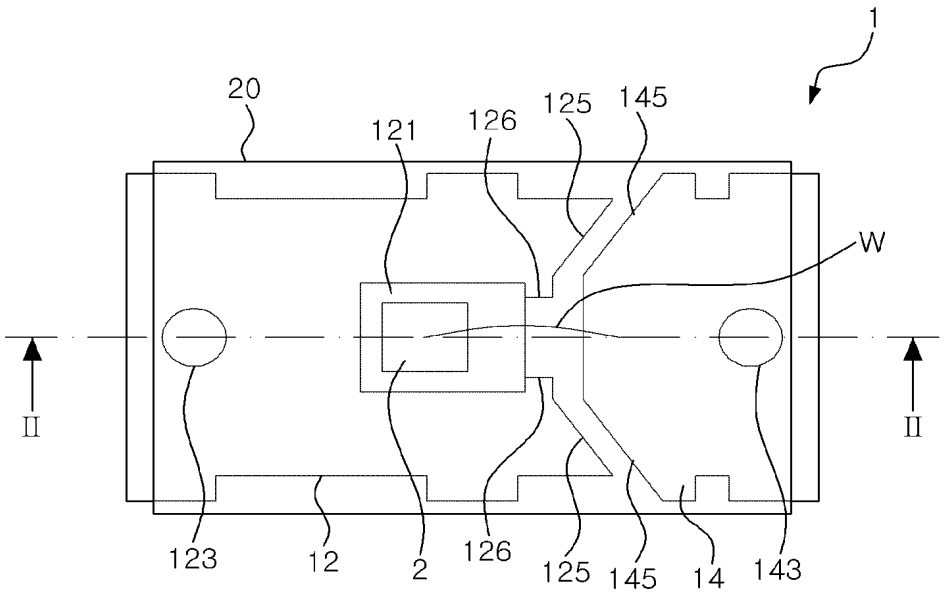
【도 4】


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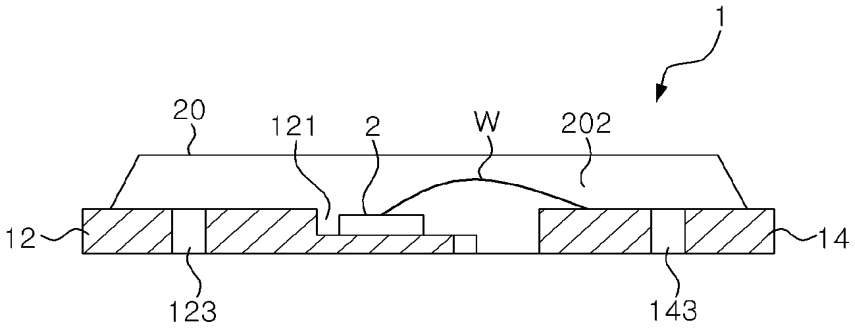
【도 5】


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【도 6】


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【도 7】


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Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 07/19/2010

CBURT1 SALE #00000008 Mailroom Dt: 06/02/2010 12745878
01 FC : 1642 430.00 OP

Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 07/19/2010

CBURT1 ADJ #00000008 Mailroom Dt: 06/02/2010
Seq No: 5218 Sales Acctg Dt: 06/03/2010 12745878
02 FC : 1632 -540.00 OP

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/745,878	06/02/2010	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	06/02/2010	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 16	Minus	** 20	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/LYNN NELSON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 02, 2008

Application or Docket Number: 12/745878

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)	SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
U.S. NATIONAL STAGE FEES			RATE	FEE		RATE	FEE
BASIC FEE	SMALL ENT. = $ 150	LARGE ENT. = $ 300	BASIC FEE	$165	OR	BASIC FEE	$330
EXAMINATION FEE	Satisfies PCT Article 33(1)-(4) = $ 50 / $ 100	All other situations = $ 110 / $ 220	EXAM. FEE	$110		EXAM. FEE	$220
SEARCH FEE	U.S. is ISA = $ 50 / $ 100 ALL other countries = $ 200 / $ 400	ALL other situations = $ 270 / $ 540	SEARCH FEE	$215		SEARCH FEE	$430
FEE FOR EXTRA SPEC. PGS.	minus 100 =	/ 50 =	X $ 135 =			X $ 270 =	
TOTAL CHARGEABLE CLAIMS	16 minus 20 =	*	X $ 26 =		OR	X $ 52 =	
INDEPENDENT CLAIMS	1 minus 3 =	*	X $ 110 =		OR	X $ 220 =	
MULTIPLE DEPENDENT CLAIM PRESENT			+ $ 195 =		OR	+ $ 390 =	
			TOTAL		OR	TOTAL	480

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

SMALL ENTITY RATE	ADDI-TIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDI-TIONAL FEE
X $ 26 =		OR	X $ 52 =	
X $ 110 =		OR	X $ 220 =	
+ $ 195 =		OR	+ $ 390 =	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

RATE	ADDI-TIONAL FEE	OR	RATE	ADDI-TIONAL FEE
X $ 26 =		OR	X $ 52 =	
X $ 110 =		OR	X $ 220 =	
+ $ 195 =		OR	+ $ 390 =	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than '20', enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than '3', enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

MULTIPLE DEPENDENT CLAIM CALCULATION SHEET (FOR USE WITH FORM PTO-875)	SERIAL NO.	FILING DATE
	12/745878	

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
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TOTAL IND.			1			
TOTAL DEP.			15			
TOTAL CLAIMS			16			

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
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Document code: WFEE

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U.S. APPLICATION NUMBER NO.	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
12/745,878	Eun Jung Seo	P3962US00

58027
H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

INTERNATIONAL APPLICATION NO.	
PCT/KR2008/006777	
I.A. FILING DATE	PRIORITY DATE
11/18/2008	12/03/2007

CONFIRMATION NO. 4953
371 ACCEPTANCE LETTER

OC000000042632529

Date Mailed: 07/21/2010

NOTICE OF ACCEPTANCE OF APPLICATION UNDER 35 U.S.C 371 AND 37 CFR 1.495

The applicant is hereby advised that the United States Patent and Trademark Office in its capacity as a Designated / Elected Office (37 CFR 1.495), has determined that the above identified international application has met the requirements of 35 U.S.C. 371, and is ACCEPTED for national patentability examination in the United States Patent and Trademark Office.

The United States Application Number assigned to the application is shown above and the relevant dates are:

06/02/2010	06/02/2010
DATE OF RECEIPT OF 35 U.S.C. 371(c)(1), (c)(2) and (c)(4) REQUIREMENTS	DATE OF COMPLETION OF ALL 35 U.S.C. 371 REQUIREMENTS

A Filing Receipt (PTO-103X) will be issued for the present application in due course. **THE DATE APPEARING ON THE FILING RECEIPT AS THE " FILING DATE" IS THE DATE ON WHICH THE LAST OF THE 35 U.S.C. 371 (c)(1), (c)(2) and (c)(4) REQUIREMENTS HAS BEEN RECEIVED IN THE OFFICE. THIS DATE IS SHOWN ABOVE.** *The filing date of the above identified application is the international filing date of the international application (Article 11(3) and 35 U.S.C. 363).* Once the Filing Receipt has been received, send all correspondence to the Group Art Unit designated thereon.

The following items have been received:

- Copy of the International Application filed on 06/02/2010
- Copy of the International Search Report filed on 06/02/2010
- Copy of IPE Report filed on 06/02/2010
- Preliminary Amendments filed on 06/02/2010
- Information Disclosure Statements filed on 06/02/2010
- Oath or Declaration filed on 06/02/2010
- Request for Immediate Examination filed on 06/02/2010
- U.S. Basic National Fees filed on 06/02/2010
- Substitute Specification filed on 06/02/2010
- Priority Documents filed on 06/02/2010
- Power of Attorney filed on 06/02/2010

FORM PCT/DO/EO/903 (371 Acceptance Notice)

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

CHARITTA A SHELTON

Telephone: (703) 756-1471

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/745,878	06/02/2010		980	P3962US00	16	1

CONFIRMATION NO. 4953

58027
H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

FILING RECEIPT

OC000000042632528

Date Mailed: 07/21/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Eun Jung Seo, Ansan-si, KOREA, REPUBLIC OF;

Assignment For Published Patent Application

Seoul Semiconductor Co., Ltd., Seoul, KOREA, REPUBLIC OF

Power of Attorney: The patent practitioners associated with Customer Number 58027

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/KR2008/006777 11/18/2008

Foreign Applications

REPUBLIC OF KOREA 10-2007-0124469 12/03/2007

If Required, Foreign Filing License Granted: 07/17/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/745,878**

Projected Publication Date: 10/28/2010

Non-Publication Request: No

Early Publication Request: No

Title

SLIM LED PACKAGE

Preliminary Class

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

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license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

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NOT GRANTED

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/745,878	06/02/2010	Eun Jung Seo	P3962US00

CONFIRMATION NO. 4953

58027
H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

PUBLICATION NOTICE



Title:SLIM LED PACKAGE

Publication No.US-2010-0270571-A1
Publication Date:10/28/2010

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	12745878
Filing Date	2010-06-02
First Named Inventor	Eun Jung Seo
Art Unit	2815
Examiner Name	WILSON, ALLAN R
Attorney Docket Number	P3962US00

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050151149		2005-07-14	Chia et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12745878
	Filing Date	2010-06-02
	First Named Inventor	Eun Jung Seo
	Art Unit	2815
	Examiner Name	WILSON, ALLAN R
	Attorney Docket Number	P3962US00

	1		☐

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	12745878
Filing Date	2010-06-02
First Named Inventor	Eun Jung Seo
Art Unit	2815
Examiner Name	WILSON, ALLAN R
Attorney Docket Number	P3962US00

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2012-01-13
Name/Print	Hae-Chan Park	Registration Number	50114

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	11832141
Application Number:	12745878
International Application Number:	
Confirmation Number:	4953
Title of Invention:	SLIM LED PACKAGE
First Named Inventor/Applicant Name:	Eun Jung Seo
Customer Number:	58027
Filer:	Hae-Chan Park/JungAh Kim
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P3962US00
Receipt Date:	13-JAN-2012
Filing Date:	02-JUN-2010
Time Stamp:	17:23:56
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	P3962US00_IDS.pdf	851274 2e6aa617582526894b711a76735b62fb5ec9687a	no	4

Warnings:	
Information:	

Total Files Size (in bytes):	851274

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/745,878	06/02/2010	Eun Jung Seo	P3962US00	4953

58027 7590 02/23/2012

H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

EXAMINER	
WILSON, ALLAN R	

ART UNIT	PAPER NUMBER
2815	

NOTIFICATION DATE	DELIVERY MODE
02/23/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATENT@PARK-LAW.COM

Office Action Summary	Application No.	Applicant(s)	
	12/745,878	SEO, EUN JUNG	
	Examiner	Art Unit	
	ALLAN R. WILSON	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *1* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2012*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-14* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☐ Claim(s) _____ is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☒ Claim(s) *1-14* are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Election/Restrictions

This application contains claims directed to the following patentably distinct species:

Species I. Figures 1 and 2.

Species II. Figure 3.

Species III. Figure 4.

Species IV. Figure 5.

Species V. Figures 6 and 7.

Species VI. Figure 8.

The species are independent or distinct because:

Species I. Illustrates phosphor is disposed in a resin constituting the encapsulation material, which appears to be claims 5, 9 and 11.

Species II. Illustrates no phosphor and a bonding recess, which appears to be claims 3 and 4.

Species III. Illustrates phosphor is disposed in the adjacent resin part and a bonding recess, which appears to be claims 3, 4, 5, 9 and 10.

Species IV. Illustrates phosphor is coated on the LED chip by conformal coating and a bonding recess, which appears to be claims 3, 4, 5 and 12.

Species V. Illustrates a slant part, which appears to be claims 5, 7 and 8.

Species VI. Illustrates scratches formed on an upper or lower surface of the first or second lead frame, which appears to be claim 14.

In addition, these species are not obvious variants of each other based on the current record.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species, or a single grouping of patentably indistinct species, for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, claims 1, 2, 6 and 13 are generic.

There is a search and/or examination burden for the patentably distinct species as set forth above because at least the following reason(s) apply:

--the species or groupings of patentably indistinct species have acquired a separate status in the art in view of their different classification;

--the species or groupings of patentably indistinct species have acquired a separate status in the art due to their recognized divergent subject matter;

--the species or groupings of patentably indistinct species require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search strategies or search queries).

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species or a grouping of patentably indistinct species to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected species or grouping of**

patentably indistinct species, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

The election may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the election of species requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected species or grouping of patentably indistinct species.

Should applicant traverse on the ground that the species, or groupings of patentably indistinct species from which election is required, are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing them to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the species unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other species.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141.

Conclusion

A shortened statutory period for reply to this Office Action is set to expire **ONE MONTH** from the mailing date of this Office Action. Applicant is reminded of the extension of time policy as set forth in 37 CFR § 1.136(a).

Any inquiry concerning this communication or earlier communications from an examiner should be directed to Primary Examiner Allan Wilson whose telephone number is 571-272-1738. Examiner Wilson can normally be reached 7:00-4:00 Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Allan R. Wilson/
Primary Examiner, Art Unit 2815

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Docket No.: P3962US00

Eun Jung SEO

Serial No.: 12/745,878 Group Art Unit: 2815

Confirmation No.: 4953

Filed: June 2, 2010 Examiner: WILSON, ALLAN R

For: **SLIM LED PACKAGE**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO ELECTION/RESTRICTION REQUIREMENT

Sir:

In reply to the February 23, 2012 Restriction Requirement, Applicant elects Species I, relating to Figures 1 and 2, and claims 1, 2, 5, 6, 9, and 13, without traverse.

It is not believed that any extensions of time or fees are required. If extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned for under 37 C.F.R. §1.136(a) and associated fees may be charged to our Deposit Account No. 50-3698.

Respectfully submitted,

/hae-chan park/

Hae-Chan Park
Reg. No. 50,114

Dated: March 19, 2012

CUSTOMER NO.: 58027
H.C. Park & Associates, PLC

Electronic Acknowledgement Receipt

EFS ID:	12335781
Application Number:	12745878
International Application Number:	
Confirmation Number:	4953
Title of Invention:	SLIM LED PACKAGE
First Named Inventor/Applicant Name:	Eun Jung Seo
Customer Number:	58027
Filer:	Hae-Chan Park/JungAh Kim
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P3962US00
Receipt Date:	19-MAR-2012
Filing Date:	02-JUN-2010
Time Stamp:	18:25:57
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	P3962US00-Reply.pdf	13791 a6e4a99677911e43d4b7209c74035fe147a71d4f	no	1

Warnings:	
Information:	

Total Files Size (in bytes):	13791

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/745,878	06/02/2010	Eun Jung Seo	P3962US00	4953

58027 7590 03/28/2012

H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

EXAMINER	
WILSON, ALLAN R	
ART UNIT	**PAPER NUMBER**
2815	

NOTIFICATION DATE	DELIVERY MODE
03/28/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATENT@PARK-LAW.COM

Office Action Summary	Application No.	Applicant(s)	
	12/745,878	SEO, EUN JUNG	
	Examiner	Art Unit	
	ALLAN R. WILSON	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2012*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-16* is/are pending in the application.

5a) Of the above claim(s) *3,4,7,8,10-12 and 14-16* is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1,2,5,6,9 and 13* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/2/10, 1/13/12*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Application Publication No. 2005/0151149 of record to Chia et al. (hereafter "Chia").

Regarding claim 1, Chia illustrates in at least figures 2 and 3 with associated text:

A light emitting diode (LED) package, comprising:

a first lead frame 215 and a second lead frame 220 separated from each other;

a chip mounting recess 235 formed in a first upper surface region of the first lead frame;

an LED chip disposed on a bottom surface of the chip mounting recess and connected to the second lead frame via a bonding wire 210; and a transparent encapsulation material 225 arranged on the LED chip,

wherein a thickness of the first lead frame in the first upper surface region is less than the thickness of the first lead frame in the other upper surface regions.

Regarding claim 2, the examiner had to assume what the product would be by the process claimed. For example, in claim 2 it was assumed that the product was the chip mounting recess. The claim that it was "an etched surface" was not considered to have full patentable weight. A "product by process" claim is directed to the product per se, no matter how actually made, MPEP 2113 "Product-by-Process Claims," In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90; In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claim 5, Chia illustrates in figures 2 and 3 an opening or recess 240, 245, 250, 260 formed in at least one upper surface or lower surface of the first lead frame or second lead frame wherein the transparent encapsulation material 225 is arranged in the opening or recess.

Regarding claim 13, it was assumed that the product was the transparent encapsulation material. The "product by process" claim that it was "formed by transfer molding" was not considered to have full patentable weight. See claim 2 above.

Claims 1, 6 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Application Publication No. 2005/0280017 of record to Oshio et al. (hereafter "Oshio").

Regarding claim 1, Oshio illustrates in at least figures 1-3 with associated text:

A light emitting diode (LED) package, comprising:

a first lead frame 20 and a second lead frame 30 separated from each other;

a chip mounting recess 20C formed in a first upper surface region of the first lead frame;

an LED chip 10 disposed on a bottom surface of the chip mounting recess and connected to the second lead frame via a bonding wire 60; and a transparent encapsulation material 50 arranged on the LED chip,

wherein a thickness T2 of the first lead frame in the first upper surface region is less than the thickness T1 of the first lead frame in the other upper surface regions.

Regarding claim 6, Oshio illustrates in figure 1 the LED chip 10 is thinner than a depth of the chip mounting recess.

Regarding claim 9, Oshio discloses in paragraph [0068] a phosphor disposed in the transparent encapsulation material 50.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: See the Information Disclosure Statement.

Any inquiry concerning this communication or earlier communications from an examiner should be directed to Primary Examiner Allan Wilson whose telephone

number is (571) 272-1738. Examiner Wilson can normally be reached 7:00-4:00 Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Allan R. Wilson/
Primary Examiner, Art Unit 2815

Notice of References Cited	Application/Control No. 12/745,878	Applicant(s)/Patent Under Reexamination SEO, EUN JUNG	
	Examiner ALLAN R. WILSON	Art Unit 2815	Page 1 of 1

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*	B	US-2004/0104391 A1	06-2004	Maeda et al.	257/079
*	C	US-2005/0280017 A1	12-2005	Oshio et al.	257/099
*	D	US-7,291,866 B2	11-2007	Oshio et al.	257/99
*	E	US-7,301,176	11-2007	Abe et al.	257/98
*	F	US-2008/0023714 A1	01-2008	Chae et al.	257/98
*	G	US-2008/0121921 A1	05-2008	Loh et al.	257/99
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*	I	US-7,682,848 B2	03-2010	Shimizu et al.	438/21
	J	US-			
	K	US-			
	L	US-			
	M	US-			

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	N	JP 63200550 A	08-1988	Japan	HASEGAWA, HIROMASA	
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　昭63－200550

⑤Int.Cl.⁴	識別記号	庁内整理番号	㊸公開　昭和63年(1988)8月18日
H 01 L 23/48		F－7735－5F	
33/00		N－7733－5F	

審査請求　未請求　発明の数 1　(全3頁)

㊹発明の名称　リードフレーム

㉑特　願　昭62－33862

㉒出　願　昭62(1987)2月17日

㉒発明者　長谷川　弘正　大阪府門真市大字門真1006番地　松下電子工業株式会社内

㉑出願人　松下電子工業株式会社　大阪府門真市大字門真1006番地

㉔代理人　弁理士　中尾　敏男　外1名

明　細　書

1、発明の名称

リードフレーム

2、特許請求の範囲

半導体素子載置部，内部リード部および外部リード部を有するリードパターンが複数個、一つの導体平板に反復して形成され、前記半導体素子載置部に凹部を設けたことを特徴とするリードフレーム。

3、発明の詳細な説明

産業上の利用分野

本発明は、半導体素子載置部が内部リード，外部リードと概して同一平面に設けられた半導体素子を搭載する半導体リードフレームに関するもので、半導体素子載置部の材料の厚さを大きくすることにより、凹部を設けるなど加工を容易にし、且つ加工による組立工程などへの影響を除去するものである。

従来の技術

従来のリードフレームの半導体素子載置部に凹部を設けた場合の平面図および断面図が第3図a，bである。半導体素子載置部1は材料の厚さが小さいため凹部4を設ける加工により、反対面には凸部8が形成されている。かかるリードフレームに半導体素子を搭載し、封止用樹脂で被覆して使用されている。

発明が解決しようとする問題点

従来の内部リード，外部リードと概して同一平面に半導体素子載置部を有するリードフレームは、材料の厚さが小さいため、半導体素子載置部の一面に凹部を設ける加工をすると他の面に、凸部が形成されるため、素子を搭載する、素子と内部リード部2を金線5で接続するなどいわゆる組立工程において、装置表面からリードフレームが浮き上るため、組立の作業性を著しく阻害するという欠点がある。これを避ける一方法として、装置側表面に溝を設ける手段が用いられるが、半導体素子載置部の寸法が異なるごとに、溝寸法も変更の必要があり実用的でない。本発明はこのような問題を解決するもので、容易に凹部加工ができ

て、且つ、組立作業の容易性を確保することを目的とする。

問題点を解決するための手段

上記問題を解決するために、本発明は半導体素子部の厚さを大きくしたものである。その厚さは、凹部の必要な深さが材料の厚さの６０％以下になるようにする。即ち深さが０．３㎜必要な場合には、材料の厚さは０．５㎜になる。

作用

半導体素子載置部の材料の厚さを、必要な凹部の深さが６０％以下となるよう選定することにより、凹部加工の反対面に凸部が形成されることなく平面の状態が保てる。

実施例

第１図ａは、本発明のリードフレームの平面図、ｂは断面図を示した一実施例である。半導体素子載置部１，内部リード部２，外部リード部３が複数個、一つの導体平板に反復形成されている。半導体素子載置部１には凹部４が形成されている。第２図ａ，ｂは、半導体素子載置部１に深

さ０．３㎜の凹部４を設けたＦｅ－Ｎｉ(４２％)を材料とする厚さ０．５㎜の半導体用リードフレームに封止用樹脂６を被覆した一実施例のそれぞれ平面図と断面図である。半導体素子７として０．４㎜□，厚さ０．２５㎜の発光ダイオードを導電性ペーストで接着，配設している。凹部４の上部開口径１．２㎜φ，下部底面径０．６φ、封止用樹脂６はエポキシ系透明樹脂を用いている。凹部の加工には金型によるプレス工法を用いた。凹部周辺にはワイヤボンドに影響のない程度の凸部が形成されるが反対側の面には５μｍ程度の凸部が形成されるだけで、いわゆる組立工程に関係なく、凹部加工をしていない場合と同様に使用できる。凹部の深さが０．３㎜より大きくなると反対面の凸部が目立ち初め、平坦な面とは見なし難く、又凹部周辺の凸部も高くなる。上記材料，寸法は一例であるが、凹部深さが材料厚さの６０％を越えると裏面の凸部が大きくなると同時に凹部周辺の凸部も大きくなり組立工程への影響は避け難い。

発明の効果

以上のように、本発明によるリードフレームを用いることで凹部加工をしても従来の組立装置を利用して容易に組立を実施できた。

４、図面の簡単な説明

第１図ａ，ｂは本発明の一実施例によるリードフレームの平面図，断面図、第２図ａ，ｂは本発明実施例のリードフレームを用いて組立を行い、樹脂封止により成型した半導体装置の平面透視図，断面図、第３図ａ，ｂは従来例リードフレームの平面図，断面図である。

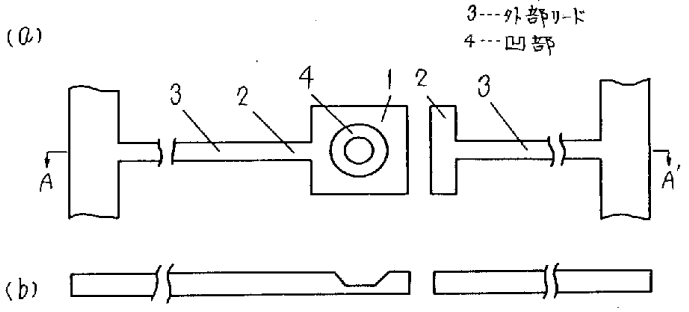
１……半導体素子載置部、２……内部リード、３……外部リード、４……凹部、５……金線、６……封止用樹脂、７……半導体素子、８……凸部。

代理人の氏名　弁理士　中尾敏男　ほか１名

EX1012, Page 236

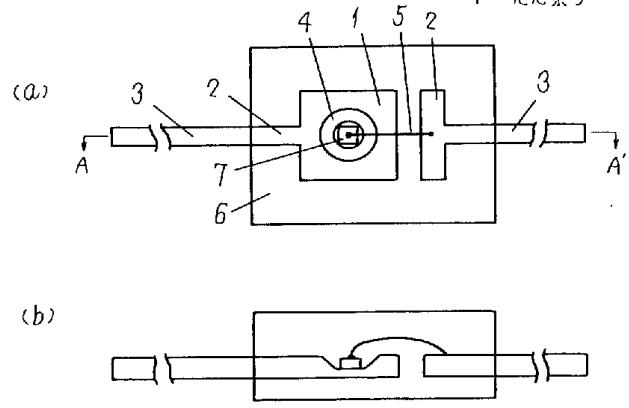
第 1 図

1---半導体素子載置部
2---内部リード
3---外部リード
4---凹部



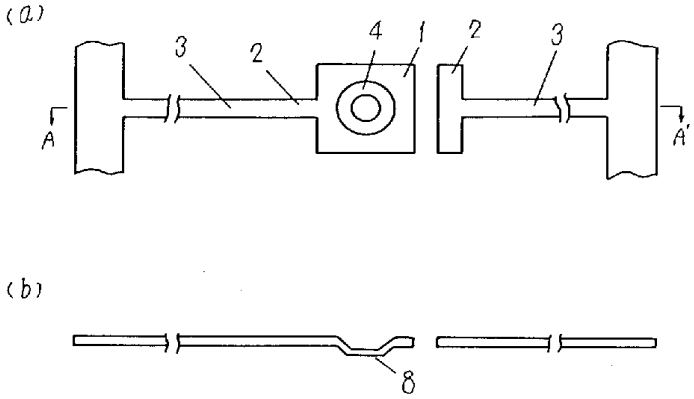
第 2 図

5---金線
6---封止用樹脂
7---発光素子



第 3 図

1---半導体素子載置部
2---内部リード
3---外部リード
4---凹部
8---凸部



PAT-NO: JP363200550A
DOCUMENT-IDENTIFIER: JP 63200550 A
TITLE: LEAD FRAME
PUBN-DATE: August 18, 1988

INVENTOR-INFORMATION:

NAME	COUNTRY
HASEGAWA, HIROMASA	

ASSIGNEE-INFORMATION:

NAME	COUNTRY
MATSUSHITA ELECTRONICS CORP	N/A

APPL-NO: JP62033862
APPL-DATE: February 17, 1987

INT-CL (IPC): H01L023/48 , H01L033/00

US-CL-CURRENT: 257/676

ABSTRACT:

PURPOSE: To prevent a lead frame from rising off the surface of a semiconductor device and facilitate assembly work of the semiconductor device by selecting the thickness of the lead frame material so as to make the depth of a necessary recess less than 60% of the thickness.

CONSTITUTION: A lead frame unit for a semiconductor device is composed of a semiconductor element mounting part 1, a plurality of inner lead parts 2 and a plurality of outer lead parts 3 and the lead frame units are repeatedly formed in one plane to constitute a lead

frame. A recess 4 with a depth of 0.3 mm is formed in the element mounting part 1 and the lead frame is covered with sealing resin 6 composed of Fe-Ni with a thickness of 0.5 mm. A light emitting diode is employed as the semiconductor element 7 placed and bonded in the recess 4 with conductive paste. The recess 4 is formed by a stamping process to reduce the influence upon the other parts, prevent the lead frame from rising off the surface of the semiconductor device and facilitate assembly of the device.

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BIB DATA SHEET

CONFIRMATION NO. 4953

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/745,878	06/02/2010	257	2815	P3962US00

APPLICANTS
Eun Jung Seo, Ansan-si, KOREA, REPUBLIC OF;

**** CONTINUING DATA ***************************
This application is a 371 of PCT/KR2008/006777 11/18/2008

**** FOREIGN APPLICATIONS **************************
REPUBLIC OF KOREA 10-2007-0124469 12/03/2007

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
07/17/2010

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /ALLAN R WILSON/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		KOREA, REPUBLIC OF	2	16	1

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SUITE 7500
VIENNA, VA 22182
UNITED STATES

TITLE
SLIM LED PACKAGE

FILING FEE RECEIVED		
980	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"20050151149".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/03/22 07:35
L2	14950	((257/98-100,E33.059,E33.061,E33.066) or (438/26)).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/03/22 07:57
L3	6108	((257/676) or (438/123)).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/03/22 07:58
L4	468	3 and (LED or (light emitting diode))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/03/22 08:00
L5	95	3 and (LED or (light emitting diode)) same (thickness or height)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/03/22 08:01
L6	2578	2 and lead frame	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/03/22 08:37
L7	975	6 and (LED or (light emitting diode)) same (thickness or height)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/03/22 08:37
L8	673	6 and (LED or (light emitting diode)) with (thickness or height)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	ADJ	ON	2012/03/22 08:37

			DERWENT; IBM_TDB			
L9	276	2 and second adj2 lead frame	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/03/22 08:38
L10	94	9 and (LED or (light emitting diode)) same (thickness or height)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/03/22 08:39
L11	1	"20110186902".pn. and "18"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/03/22 08:43
L12	12	(US-20100270571-$ or US-20050151149-$ or US-20080121921-$ or US-20110186902-$ or US-20110186901-$ or US-20110133237-$).did. or (US-6603148-$ or US-7488622-$ or US-6943433-$ or US-7282785-$ or US-7301176-$).did. or (JP-63200550-$).did.	US-PGPUB; USPAT; JPO	ADJ	ON	2012/03/22 08:52
L13	6	12 and phosphor$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/03/22 08:52
L14	73	9 and phosphor$2 not 10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/03/22 08:55
L15	483	7 and phosphor$2 not (10 or 14)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/03/22 09:00
L16	338	8 and phosphor$2 not (10 or 14)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/03/22 09:00
L17	329	8 and phosphor not (10 or 14)	US-PGPUB; USPAT;	ADJ	ON	2012/03/22 09:07

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L18	241	17 not (@ad>"20081118" or @rlad>"20081118" or @pt1d>"20081118")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/03/22 09:09
L19	2	"20050280017".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/03/22 09:41

3/22/2012 11:25:01 AM
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PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
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(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	2010-06-02
First Named Inventor	Eun Jung SEO
Art Unit	
Examiner Name	
Attorney Docket Number	P3962US00

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/A.W./	1	6603148		2003-08-05	Sano et al.	

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/A.W./	1	2006-179541	JP		2006-07-06	Enomoto Co Ltd		☐
/A.W./	2	1020020065729	KR		2002-08-14	Chippac Korea Co., Ltd.		☐
/A.W./	3	1020060059575	KR		2006-06-02	Samsung Electronics Co., Ltd.		☐

Receipt date: 06/02/2010	Application Number	12745878 - GAU: 2815
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2010-06-02
	First Named Inventor	Eun Jung SEO
	Art Unit	
	Examiner Name	
	Attorney Docket Number	P3962US00

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		☐

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Examiner Signature	/Allan Wilson/	Date Considered	03/21/2012

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	12745878
Filing Date	2010-06-02
First Named Inventor	Eun Jung Seo
Art Unit	2815
Examiner Name	WILSON, ALLAN R
Attorney Docket Number	P3962US00

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/A.W./	1	20050151149		2005-07-14	Chia et al.	

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Receipt date: 01/13/2012		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Application Number	12745878
	Filing Date	2010-06-02
	First Named Inventor	Eun Jung Seo
	Art Unit	2815
	Examiner Name	WILSON, ALLAN R
	Attorney Docket Number	P3962US00

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EXAMINER SIGNATURE

Examiner Signature	/Allan Wilson/	Date Considered	03/22/2012

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

Receipt date: 01/13/2012

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	12745878
Filing Date	2010-06-02
First Named Inventor	Eun Jung Seo
Art Unit	2815
Examiner Name	WILSON, ALLAN R
Attorney Docket Number	P3962US00

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2012-01-13
Name/Print	Hae-Chan Park	Registration Number	50114

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12745878	SEO, EUN JUNG
	Examiner	Art Unit
	ALLAN R WILSON	2815

SEARCHED

Class	Subclass	Date	Examiner
257	98-100, 676, E33.059, E33.061, E33.066	3/22/12	AW
438	26, 123	3/22/12	AW

SEARCH NOTES

Search Notes	Date	Examiner
See Examiner's search strategy and results – EAST Search History	3/22/12	AW

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner

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Courtesy Reminder for
Application Serial No: 12/745,878

Attorney Docket No: P3962US00
Customer Number: 58027
Date of Electronic Notification: 03/28/2012

This is a courtesy reminder that new correspondence is available for this application. The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	Docket No.: P3962US00
Eun Jung SEO	
Serial No.: 12/745,878	Group Art Unit: 2815
Confirmation No.: 4953	
Filed: June 2, 2010	Examiner: WILSON, ALLAN R

For: **SLIM LED PACKAGE**

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY UNDER 37 C.F.R. § 1.111

Sir:

In response to the Non-Final Office Action mailed March 28, 2012 ("Office Action"), Applicant respectfully requests reconsideration of the application in view of the following Amendments and Remarks.

Amendments to the Claims begin on page 2.

Remarks begin on page 6.

No extensions of time are required at this time. If extension(s) of time are necessary to prevent abandonment of this application, then they are petitioned for under 37 C.F.R. § 1.136(a). No fees for net addition of claims are required at this time. Any fees required for extension(s) of time or for the net addition of claims may be charged to our Deposit Account No. 50-3698.

AMENDMENTS TO THE CLAIMS

Please **AMEND** claim 1 as shown below.

Please **CANCEL** claim 6 as shown below.

Please **ADD** new claims 17 and 18 as shown below.

This claim list replaces all prior claim lists in the application.

1. (Currently Amended) A light emitting diode (LED) package, comprising:

a first lead frame and a second lead frame separated from each other;

a chip mounting recess formed in the ~~a first~~ upper surface ~~region~~ of the first lead frame;

an LED chip disposed within ~~on a bottom surface of~~ the chip mounting recess and connected to the second lead frame via a bonding wire;

a groove formed in the lower surface of the first lead frame and extending along an edge of the first lead frame that faces the second lead frame; and

a transparent encapsulation material arranged on the LED chip and in the groove,

wherein the chip mounting recess and the groove are disposed in different regions of the first lead frame ~~a thickness of the first lead frame in the first upper surface region is less than the thickness of the first lead frame in the other upper surface regions~~.

2. (Previously Presented) The LED package of claim 1, wherein the chip mounting recess comprises an etched surface.

3. (Withdrawn) The LED package of claim 1, further comprising:

a bonding recess formed in a first upper surface region of the second lead frame,

wherein a thickness of the second lead frame in the first upper surface region is less than the thickness of the second lead frame in the other upper surface regions, and one end of the bonding wire is connected with the second lead frame in the bonding recess.

4. (Withdrawn) The LED package of claim 3, wherein the bonding recess comprises an etched surface.

5. (Previously Presented) The LED package of claim 1, further comprising:

an opening or recess formed in at least one upper surface or lower surface of the first lead frame or second lead frame, wherein the transparent encapsulation material is arranged in the opening or recess.

6. (Canceled)

7. (Withdrawn) The LED package of claim 1, wherein the first lead frame and the second lead frame have opposite sides facing each other, and the opposite sides each comprise a slanted part.

8. (Withdrawn) The LED package of claim 7, wherein at least one of the opposite sides comprises a depressed part formed therein that widens a separation between the first lead frame and the second lead frame.

9. (Previously Presented) The LED package of claim 1, further comprising:

a phosphor disposed in the transparent encapsulation material.

10. (Withdrawn) The LED package of claim 1, further comprising:

a resin part disposed in the chip mounting recess.

11. (Withdrawn) The LED package of claim 10, wherein the phosphor is disposed in the resin part.

12. (Withdrawn) The LED package of claim 9, wherein the phosphor is disposed directly on the LED chip.

13. (Previously Presented) The LED package of claim 1, wherein the transparent encapsulation material is formed by transfer molding.

14. (Withdrawn) The LED package of claim 1, further comprising:

a plurality of scratches formed on an upper surface or a lower surface of the first lead frame or the second lead frame to increase a bonding force between the first lead frame or the second lead frame and the transparent encapsulation material.

15. (Withdrawn) The LED package of claim 7, wherein the first lead frame comprises a depressed part formed therein that widens a separation between the first lead frame and the second lead frame, and wherein the bonding wire is disposed directly above the depressed part.

16. (Withdrawn) The LED package of claim 10, wherein the phosphor is disposed in the transparent encapsulation material.

17. (New) The light emitting diode (LED) package of claim 1, wherein the LED chip

disposed completely within the chip mounting recess.

18. (New) The LED package of claim 1, wherein the chip mounting recess is not disposed directly above the groove.

REMARKS

Claim 1 has been amended, claim 6 has been canceled without prejudice or disclaimer, claims 3, 4, 7, 8, 10-12, and 14-16 have been withdrawn, and new claims 17 and 18 have been added. Accordingly, claims 1, 2, 5, 9, 13, 17 and 18 are currently pending and under consideration, of which claim 1 is independent. No new matter has been added.

In view of the above amendments and the following Remarks, Applicants respectfully request reconsideration and timely withdrawal of the pending objections and rejections for the reasons discussed below.

Amendments to the Drawings

Please replace the sheet including Figs. 2-4 with the attached replacement sheet including Figs. 2-4. Fig. 2 has been amended to identify grooves with reference numbers 122 and 142, as discussed in paragraph [0031] of the present specification. No new matter was added by this amendment.

Rejections Under 35 U.S.C. § 102

Claims 1, 2, 5, and 13 stand rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by U.S. Patent Publication No.2005/0151149, applied for by Chia, *et al*. ("Chia"). Applicant respectfully traverses this rejection for at least the following reasons.

In order for a rejection under 35 U.S.C. § 102(b) to be proper, a single reference must disclose every claimed feature. To be patentable, a claim need only recite a single novel feature that is not disclosed in the cited reference. Thus, the failure of a cited reference to disclose one or more claimed features renders the 35 U.S.C. § 102(b) rejection improper.

In order to even more particularly point out the aspects of the present invention, claim 1 has been amended to recite:

a chip mounting recess formed in the upper surface of the first lead frame;
an LED chip disposed within the chip mounting recess and connected to the second lead frame via a bonding wire;
a groove formed in the lower surface of the first lead frame and extending along an edge of the first lead frame that faces the second lead frame; and
a transparent encapsulation material arranged on the LED chip and in the groove,
wherein the chip mounting recess and the groove are disposed in different regions of the first lead frame.

Support for this amendment can be found in at least original claim 6, Fig. 2, and paragraph [0031] of the present specification.

As shown in FIG. 2, Chia fails to teach or disclose such features. In addition, Chia fails to teach or disclose all aspects of claims 2, 5, and 13, for at least their dependency upon amended claim 1. Therefore, reconsideration and withdrawal are respectfully requested.

Claims 1, 6, and 9 stand rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by U.S. Patent Publication No.2005/0280017, applied for by Oshio, *et al*. ("Oshio"). Applicant respectfully traverses this rejection for at least the following reasons.

In order for a rejection under 35 U.S.C. § 102(b) to be proper, a single reference must disclose every claimed feature. To be patentable, a claim need only recite a single novel feature that is not disclosed in the cited reference. Thus, the failure of a cited reference to disclose one or more claimed features renders the 35 U.S.C. § 102(b) rejection improper.

As recited above, amended claim 1 recites that the groove and the chip mounting recess are formed in different regions of the first lead frame. Accordingly, the presently claimed invention provides a slim LED package, since the depth of the chip mounting recess is not limited by the depth of the groove.

In contrast, as shown in FIGS. 1-3, Oshio relates to a first lead frame 20 that includes a chip mounting recess 20C formed on the upper surface thereof, and a groove formed in the lower surface thereof (unlabeled groove filled with resin 40). However, the groove is formed directly below one side of the recess 20, and thus is formed in the same region.

As such, the first lead frame 20 must be relatively thick, to insure that the edge portion of the first lead frame 20, which is disposed between the groove and the recess 20C, has a thickness sufficient to provide structural integrity. In other words, if the thickness of the first lead frame 20 was reduced, the distance between the recess 20C and the groove would be reduced, thereby reducing the thickness of the edge portion to the point that breakage could easily occur. Thus, Oshio fails to provide the thickness reduction benefits of the presently claimed invention.

Accordingly, Oshio fails to teach or disclose all aspects of the present claims. Therefore, reconsideration and withdrawal are respectfully requested.

Added Claims

New claim 17 recites that the LED chip is disposed entirely within the chip mounting recess, and new claim 18 recites that the chip mounting recess is not disposed directly above the groove. Support for these claims can be found in at least present FIG. 2.

As shown in FIGS. 1, 2, 5A, 6A, 7, and 8, Chia relates to light emission devices that include LED chips that are not disposed entirely within a chip mounting recess of a first lead frame. As such, Chia fails to teach or disclose an LED chip disposed entirely within a chip mounting recess, as recited in new claim 17.

With regard to claim 18, as shown in FIG. 2, the device of Chia includes a first lead frame 215 having an anchor recess 255 (groove) formed at an edge thereof that faces a second lead frame 220. The groove 255 is shown to be disposed directly under a chip mounting recess 235 formed in the upper surface of the first lead frame 215. As such, Chia fails to teach or

disclose a chip mounting recess that is not disposed directly above a groove, as recited in claim 18. In addition, Chia fails to provide the thickness reduction benefits of the presently claimed invention. As such, new claims 17 and 18 recite additional aspects not taught in the cited art.

CONCLUSION

A full and complete response has been made to the pending Office Action, and all of the stated objections and grounds for rejection have been overcome or rendered moot. Accordingly, all pending claims are allowable, and the application is in condition for allowance.

The Examiner is invited to contact Applicant's undersigned representative at the number below if it would expedite prosecution. Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully submitted,

/hae-chan park/

Hae-Chan Park
Reg. No. 50,114

Date: June 11, 2012

CUSTOMER NUMBER: 58027
H.C. Park & Associates, PLC
8500 Leesburg Pike
Suite 7500
Vienna, VA 22182
Tel: 703-288-5105
Fax: 703-288-5139
HCP/MTG/dea

Fig.2

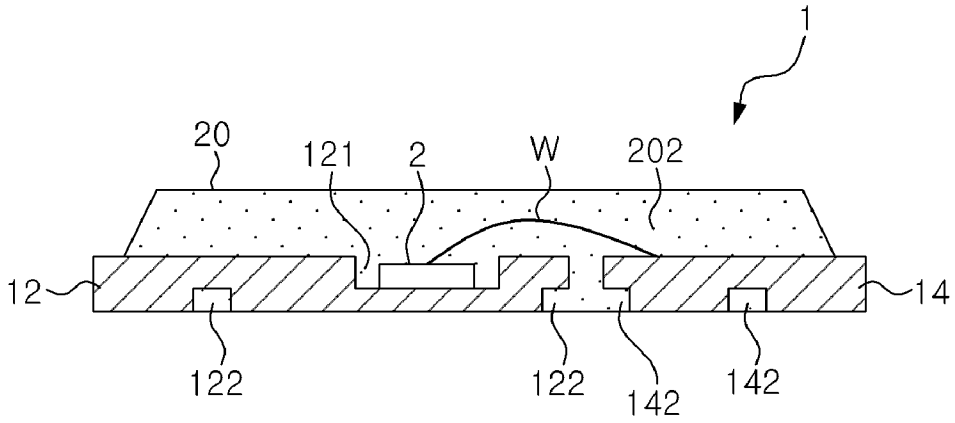


Fig.3

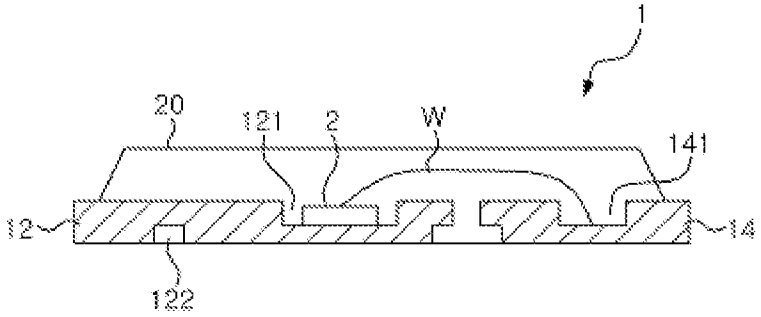
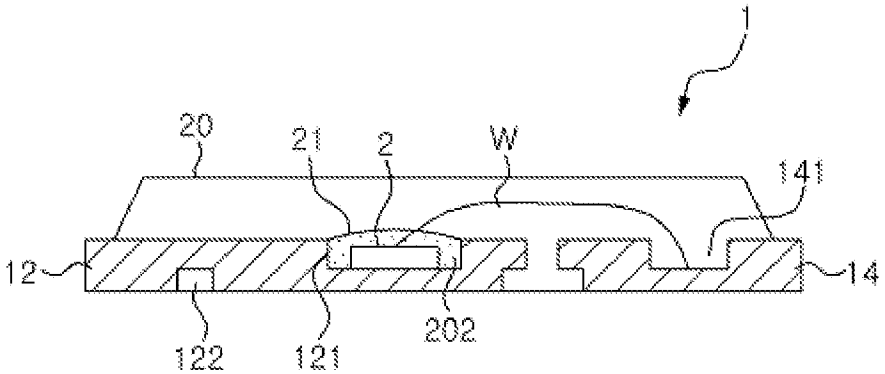


Fig.4



Electronic Acknowledgement Receipt

EFS ID:	12982872
Application Number:	12745878
International Application Number:	
Confirmation Number:	4953
Title of Invention:	SLIM LED PACKAGE
First Named Inventor/Applicant Name:	Eun Jung Seo
Customer Number:	58027
Filer:	Hae-Chan Park/JungAh Kim
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P3962US00
Receipt Date:	11-JUN-2012
Filing Date:	02-JUN-2010
Time Stamp:	17:18:22
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P3962US00-Reply.pdf	47610 ac8ca52b1effac7d296fd04906f3fbdb26d14ccf	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	9

Warnings:					
Information:					
2	Drawings-only black and white line drawings	P3962US00-ReplacementDrawings.pdf	33359 d18d502c008c495bf23adf47e75c427763831541	no	1
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Information:					
		Total Files Size (in bytes):	80969		

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/745,878	06/02/2010	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 06/11/2012	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 17	Minus	** 20	= 0	X $ =		OR	X $60=	0
Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $ =		OR	X $250=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/KAREN VESTAL/

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	12745878
Filing Date	2010-06-02
First Named Inventor	Eun Jung SEO
Art Unit	2897
Examiner Name	WILSON, ALLAN R
Attorney Docket Number	P3962US00

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	1	20060220048		2006-10-05	Matsumoto et al.	
	2	20030107316		2003-06-12	Murakami et al.	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	12745878
Filing Date	2010-06-02
First Named Inventor	Eun Jung SEO
Art Unit	2897
Examiner Name	WILSON, ALLAN R
Attorney Docket Number	P3962US00

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	the Extended European Search Report of EP Application No. 08 85 6932.2 dated March 7, 2012.	☐

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2012-06-13
Name/Print	Hae-Chan Park	Registration Number	50114

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	12745878
Filing Date:	02-Jun-2010
Title of Invention:	SLIM LED PACKAGE
First Named Inventor/Applicant Name:	Eun Jung Seo
Filer:	Hae-Chan Park/eun jo
Attorney Docket Number:	P3962US00

Filed as Large Entity

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt

EFS ID:	12999392
Application Number:	12745878
International Application Number:	
Confirmation Number:	4953
Title of Invention:	SLIM LED PACKAGE
First Named Inventor/Applicant Name:	Eun Jung Seo
Customer Number:	58027
Filer:	Hae-Chan Park/JungAh Kim
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P3962US00
Receipt Date:	13-JUN-2012
Filing Date:	02-JUN-2010
Time Stamp:	15:04:16
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$180
RAM confirmation Number	13039
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Information Disclosure Statement (IDS) Form (SB08)	P3962US00_IDS.pdf	851501 b26625d64dcf7e65eafadf77728b26c794d3338f	no	4
Warnings:					
Information:					
2	Non Patent Literature	P3962US00-EPSearchReport.pdf	505009 ef0bbc9218944e79ca3bfe323b59585eb8e16b6c	no	10
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30209 a1dcb721733994e35d0204b85275c84fe6089306	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	1386719	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20040047151		2004-03-11	Bogner, et al.	Corresponds to TW501276

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	I246780	TW		2006-01-01	Toyoda Gosei Co., Ltd.; Sumita Optical Glass Inc.	English Abstract can be found on page 4	☐
	2	501276	TW		2002-09-01	Osram Opto Semiconductors GmbH	Corresponds to US20040047151	☐
	3	200636049	TW		2006-10-16	Koninklijke Philips Electronics N.V		☐

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	Attorney Docket Number	P3962US00

	4	200522396	TW		2005-07-01	Lumileds Lighting U.S. LLCUS		☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Taiwanese Office Action dated June 1, 2012, corresponding to U.S. Application No. 12/745,878	☒

If you wish to add additional non-patent literature document citation information please click the Add button

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Signature	/hae-chan park/	Date (YYYY-MM-DD)	2012-07-16
Name/Print	/Hae-Chan Park/	Registration Number	50114

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

本案已向：

德國 國（地區） 申請專利，申請日期： 案號： ，☑有 □無主張優先權

2000 年 08 月 23 日申請案號 10041328.5

有關微生物已寄存於： ，寄存日期： ，寄存號碼：

五、發明說明(1)

本發明是有關於具有半導體晶片光電(光學電子)構件,尤其是一種可表面安裝之光電構件用於安裝於印刷電路板之洞孔(break-through)中。此外,它是有關一種方法用於製造多個此種光電構件,具有多個此種光電構件之模組(module)、顯示裝置、以及具有此種模具之照明裝置或背景照明裝置。

光電構件像是發光二極體構件典型地是所謂的放射式結構形狀,其以插入式安裝固定於印刷電路板上,或者以表面可安裝的結構形狀提供。人們例如可以比較刊載於 Simens Components 29(1991)第 4 冊第 147 至 149 頁由 F.Möllmer,G.Waitt 所著之"SIMENS SMT-TOPLED für die Oberflächenmontage。此兩個結構形狀型式使得只有以可觀的技術費用而配置於電路板之凹口或洞孔中。

本發明的目的尤其是發展用於光電構件之結構形狀,使得可以以小的結構高度,本身尤其以簡單的方式定位於電路板凹口或洞孔中。

此目的是藉由具有申請專利範圍第 1 項特徵之光電構件而達成。在申請專利範圍第 6 項中說明具有多個根據本發明光電構件之較佳模組。一個具有此種模組之較佳光學顯示裝置,以及具有此種模組之照明或背景照明裝置,是申請專利範圍第 9 或 10 項之標的。一較佳之方法用於製造多個根據本發明之構件是申請專利範圍第 13 項之標的。

五、發明說明(2)

藉由在撓性晶片載體上形成導軌此撓性晶片載體本身是構件之元件,其較佳可以被考慮同時用於構件之封裝。

較佳此種構件在裝備機器中不是由撓性載體(例如是封裝帶)拿起,而是此撓性晶片載體相對應於撓性晶片載體之劃分而切割成構件,並且將此如此獲得之構件設置在印刷電路板上。個別的封裝帶是在根據本發明之結構形式中有利地不須要。

在較佳的實施形式中,此撓性晶片載體是塑料箔。因此產生特別扁平的構件。

在一較佳的實施形式中,此半導體晶片是發光二極體晶片,其配置於形成於撓性晶片載體之殼體框之中央之中。因此產生較結構高度之光源,其尤其是用於無線電行動裝置中之導軌穿孔,例如用於特有之鍵盤或顯示器之背景照明。

此在申請專利範圍第 1,6,9,10 與 13 項中所提及之標的之有利的其他發展與實施形式,是在此等申請專利範圍上直接或間接依附之申請專利範圍附屬項中說明。

本發明之其他有利之配置與優點,是在以下與第 1 至 6 圖有關而說明的實施例中產生。

圖式之簡單說明

第 1 圖爲根據本發明在發光二極體構件上之俯視圖之概要圖式說明,

第 2 圖爲第 1 圖之發光二極體構件之橫截面之概要

五、發明說明(3)

圖式說明。

第 3 圖爲根據本發明之發光二極體構件之另一個實施例之俯視圖之概要圖式說明。

第 4 圖爲第 3 圖之發光二極體構件之橫截面之概要圖式說明。

第 5 圖爲具有多個根據本發明之構件之模組之概要截面圖式。

第 6 圖爲具有背景照明裝置(其具有多個根據本發明之構件)之液晶顯示器之概要截面圖式。

在不同的實施例中相同或相同作用的組成成份各設有相同的參考號碼。

此在第 1 與 2 圖中所說明的構件例如是發光二極體構件,並且具有發光半導體晶片 1,其包括發光活性層 2。以其底面此半導體晶片 1 與第 1 接觸層 3 導電連接。此半導體晶片 1 之表面經由連接線 4 而與第二接觸層 5 連接。此第一接觸層 3 與第二接觸層 5 例如是由金屬箔所製成,其膠合在撓性晶片載體箔 6 之上。

在另一個半導體晶片 1 中,此兩個電性連接表面具有在表面上此兩個連接表面例如借助於連接線(bond wire)而與接觸 3 與 5 連接。此半導體晶片因此可以同樣地固定在接觸表面 3 與 5 之一上,或是在兩個接觸表面 3 與 5 之間。

此半導體晶片 1 是在具有所形成漏斗形內側 8 之環形反射器框架 7 的中央之中,其較佳形成反射式。因此

五、發明說明(4)

此反射器框架 7 是在此位置,一個由半導體晶片 1 至其面所發射之光線掉頭至發射方向 9。

此由反射器框架 7 包圍之內呈是以透明之填充物質 10 填滿,在其中可埋入發光材料色素,其至少將一部份由半導體晶片 1 所發出的光線吸收,並且以與吸收光線不同波長的光線重新發射。

在第 3 與 4 圖中是說明與第 1 與 2 圖有關之變化實施例其描述發光二極體構件。在此實施例中此半導體晶片 1 是在側表面上傾斜,而固定在第一接觸層 3 與第二接觸層 5 上。在此情況中,活性層 2 是位於對晶片載體箔 6 的直角中。此配置具有優點,其不須要連接線以便用於將半導體晶片 1 固定於接觸層上。誠然其缺點爲,此活性層 2 的一面由晶片載體箔 6 取下。此外,此半導體晶片 1 之正面與底面至少部份地以材料覆蓋,其被使用於將半導體晶 1 固定在第一接觸層 3 與第二接觸層 5 上。相較於此在第 1 與 2 圖中所說明之實施例,因此在此根據第 3 與 4 圖之發光二極體中之光線產量(yield)較小。

作爲用於晶片載體箔 6 之材料首先考慮溫度固定並且可金屬化之塑料一箔。此晶片載體箔 6 例如可以是以環氧樹脂爲主之晶片載體箔,或是由聚亞胺或聚酯例如由聚一乙基一萘所製成。作爲用於反射器框架 7 的材料尤其適用溫度穩定並且能光學反射之材料,像是聚-酞醯胺(PPA)、液晶聚合物(LCP)、以及聚一乙醚一

五、發明說明(5)

乙醚一酮(PEEK)。除此之外還可以考慮其他的熱塑性塑料,只要它對溫度穩定並且是光學反射式。此種熱塑性塑料可以藉由埋入色素(像是例如 TiO_2)而具有非常高的反射性。

須選擇材料,使得反射器框架 7 可以附著在晶片載體箔 6 上。爲了改善在反射器框架 7 與晶片載體箔 6 之間連接之牢固性,在晶片載體箔中至少設有穿孔及凹口,其中嚙合反射器框架 7 之支撐榫頭 11。

作爲用於填充物質 10 之材料可以考慮用於製造光電半導體構件通常所使用的反應性樹脂,像是例如環氧樹脂,矽樹脂或丙烯類似物之化合物。

作爲發光材料例如適用一種以銪摻雜爲主之釔鋁顆粒色素,像是例如 $(Y_{1-x-y}Gd_xTb_y)_3aL_5O_{12}:Ce$,而 $0 \leqq x \leqq 1, 0 \leqq y \leqq 1$ 以及 $x+y \leqq 1$。

除了發光材料外在此填滿塊 10 還有一種擴散材料如二氧化鈦、鋇氧化物、二氧化鋯、或雙一三氧化鋁。此擴散材料有利地有助於所發射光線之均勻之外表形狀。應該沒有實施光線轉換,而是只有此所發射光線之擴散,因此在此填充物質 10 中可以只包含擴散材料並且不包括發光材料。

爲了製造發光二極體較佳首先在晶片載體箔帶上膠合金屬箔,並且然後塗以光阻層。此光阻層被塗層並且然後此光阻層與金屬箔藉由一個本身所熟知的蝕刻方法而結構化,因此產生多個接觸層對 3 與 5。然後此光

五、發明說明(6)

阻層之殘餘部份被去除,並且將反射器框架 7 例如借助於射出擠壓或射出成形而塗佈在晶片載體箔帶上。爲了將反射器框架 7 固定在晶片載體箔 6 上,而在此箔中形成洞孔,此反射器框架 7 可以嚙合於榫 11 中。

對於反射器框架之射出成形或射出壓擠之另一種方式,可以想像將預先製成的反射器框架 7 簡單容易地插在及/或黏在晶片載體箔 6 上。

然後將各半導體晶片 1 置放在晶片載體箔帶上。在將半導體晶片 1 各自接線之後,以及在晶片 1 之表面接觸與接觸層 5 之間之佈線連接製成之後,將屬於反射器框架 7 內室以填充物質 10 填滿。此晶片載體箔 6 然後被折疊或捲起,因此產生用於發光二極體之可使用之封裝單元。

對以上所說明方式不同之另一種方式,各反射器框架 7 只有在安裝了所屬之半導體晶片 1 後,才可塗佈在晶片載體箔 6 之上。

此在第 1 至 4 圖中所說明之實施例中形成帶狀之晶片載體箔 6,其中半導體晶片 1 成串排列在晶片載體箔 6 上。此外,晶片載體箔 6 還須要選擇爲寬,使得多列之發光二極體晶片可以找到彼此相鄰的位置。

此外可以將多個半導體晶片 1 配置在僅有的反射器 7 中,並且此外以此方式獲得發光二極體組件,其在不同的顏色中發光或是發出混合顏色的光。

此外,在根據本發明之結構形式中,可以以簡單的方

五、發明說明(7)

式在晶片載體箔 6 之反面尤其是整個表面設有金屬化層或金屬化結構,其在高頻使用時可用於屏蔽干擾波。

在此所說明之結構形狀藉由其比較小的位置須求而突顯其特色,藉由此可能產生幾乎完全深埋在印刷電路板洞孔中。此外,此撓性之晶片載體箔 6 可以沒有困難地適應不同的空間之實際情況。此外由於通常此晶片載體箔 6 形成得薄,此發光二極體通常具有較小的結構高度。因此產生特別扁平的構件。

另一個優點是,此晶片載體箔 6 與反射器框架 7 可由此種材料構成,其具有相同或至少非常接近之熱膨脹係數。因此,此發光二極體之可靠度在溫度循環中非常的高。

其最後還有優點,此藉助於晶片載體箔 6 所製成之發光二極體構件不再須要另外特別之封裝帶用於封裝與運輸。此撓性晶片載體箔可以有利地完全擔任封裝帶之角色,如同其在lead frame 技術中所須要者。

此晶片載體箔帶較佳是在將此組件安裝於所想要的各個構件或構件組(其由多個構件形成)中之前,才迅速地切開。

如果如此製成之發光二極體構件例如使用於行動式無線電裝置之鍵盤背景照明,此晶片載體箔可以在用於行動式無線電裝置之生產線上被分開,並且此所設之發光二極體之組一起使用於行動式無線電裝置中。在此種應用中是適合將此用於驅動發光二極體晶片所須之

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五、發明說明(8)

電路形成於晶片載體箔 6 上。

此方法在以上根據發光二極體說明。然而它還可以將其他的半導體晶片,以此說明之方法與方式封裝,並且使得可以使用。

在第 5 圖中顯示模組(module),其具有多個根據本發明之構件。在載體元件 19(例如是印刷電路板)中形成多個洞孔 20。此外,此載體元件 19 具有發射面 21。

在此載體元件 19 之面對發射面 21 之面上,將多個根據本發明之光線發射構件固定,其中光線發射構件各殼體框架 7 突入洞孔 20 中,並且發射方向 24 穿過洞孔 20 而延伸。

此晶片載體 6 與此等構件之電性導軌 3 與 5 是設置於此載體元件 19 之面對發射面 21 的表面上。爲了固定構件可以使用粘貼式連接或焊接式連接。由於形成較佳平坦晶片載體 6 之原因,其水平與垂直位置的須求明顯地小於在根據習知技術中所製之構件者。本發明尤其使得此等構件至少可以作部份埋入式的安裝。

由於所形成撓性晶片載體 6 之故,此構件是足夠的撓性,以便將壓力或變形以撓性或許也許塑性的方式支撐,而沒有將有害之壓力傳送至殼體或位於其中之發光晶片。此種安裝配置尤其適合用於緊密封裝之扁平顯示模組。

較佳此載體或至少此光線發射表面能夠吸收光線,例如使得變黑,因此可以將各個發光構件相對於其周圍的

五、發明說明(9)

對比提高。這尤其有利地設置於作爲顯示裝置的配置中。

在第 6 圖中顯示根據本發明構件之另一個配置。不同於先前所說明的配置,此在第 6 圖中所顯示之配置尤其適合作爲例如用於液晶顯示器之背景照明。

在載體 19 上如同在上一個實施例中根據本發明將光線發射構件埋入式安裝。在光線發射側將載體或構件額外配置擴散板 22。此外,此載體 19 或至少載體 19 之光線發射側表面較佳實施均勻地擴散反射,例如是白色。因此使得在非常扁平的結構中可以有相當均勻的背景照明。此擴散板被額外配置於待照明之液晶顯示器(LCD)23。

此載體 19 可以不但如以上所說明是僵硬而且可以是撓性,例如成塑料成陶瓷箔之形式,因此此背景照明或顯示模組以簡單的方式適應不同的形狀,並且甚至可以有利地安裝於本身變化的表面上。

本發明之根據此等所顯示之實施例之說明顯然不能被理解爲作爲本發明之限制,例如晶片可以直接地安裝(例如粘貼)於晶片載體之晶片安裝表面上,並且此晶片僅僅藉助於佈線連接而與導軌電性連接。此晶片同樣可以在各別的熱接合中安裝,其埋入於此晶片載體中,並且再度借助於電性佈線連接而與導軌連接。所有這些實施形式均不能偏離本發明之基本思想。

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五、發明說明(10)

符號說明

1...半導體晶片

2...活性層

3...接觸層

4...連接線

5...接觸層

6...晶片載體箔

7...反射器框架

8...內側

9...發射方向

10...填充材料

19...載體元件

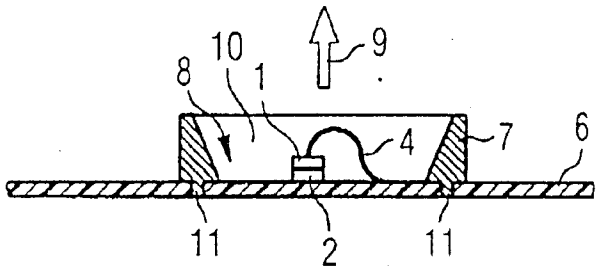
20...洞孔

21...發射面

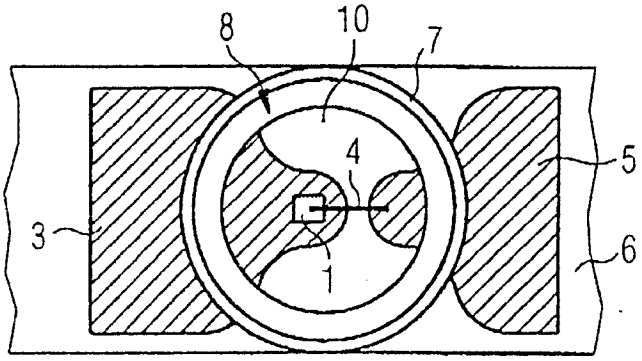
22...擴散板

24...發射方向

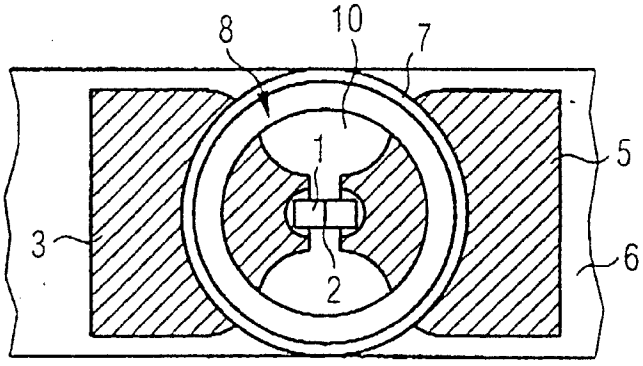
第2圖



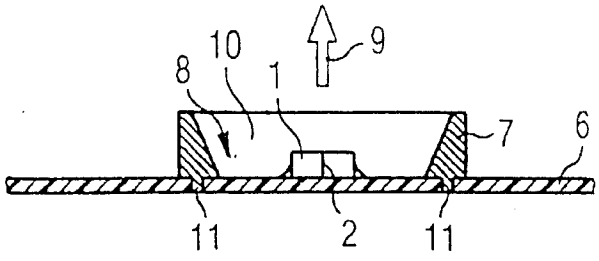
第1圖



第3圖

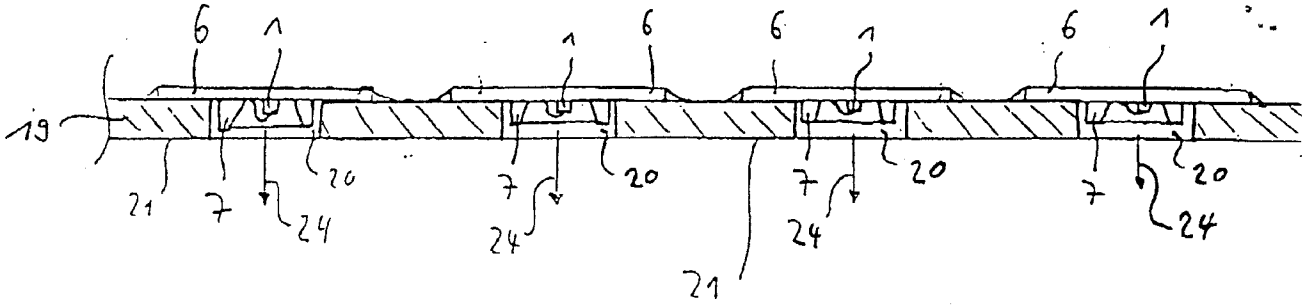


第4圖

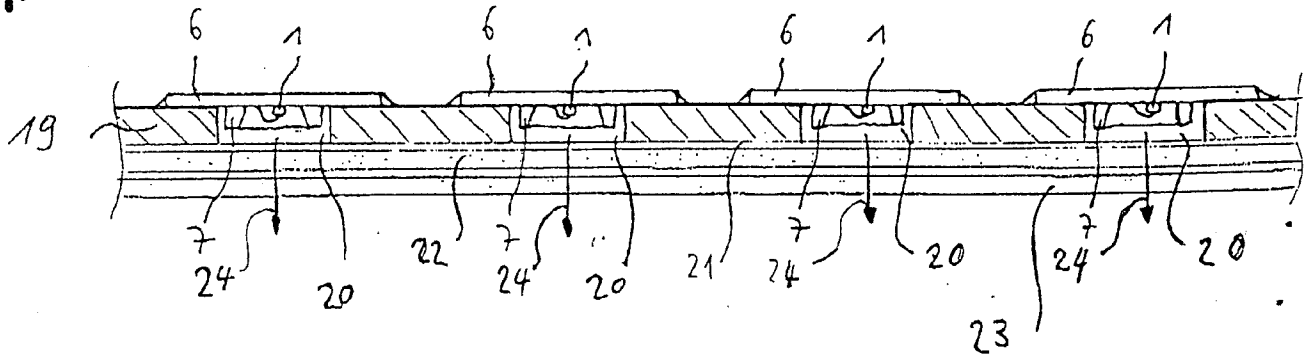


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第5圖



第6圖



91.3.1 公告本

申請日期	90.8.23
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類別	H01L27/14 H01L33/00

(以上各欄由本局填註)

501276

發明 新型 專利說明書(91年3月修正)

一、發明新型名稱	中文	具有半導體晶片之光電構件、具有多個構件之模組、光學顯示裝置、照明或背景照明裝置、液晶顯示器、製造與封裝多個構件之方法
	英文	Opto-electronic element with a semiconductor chip, Module with a semiconductor chip, Module with a plurality of elements, optical display device, illumination or background illumination device, liquid crystal display, and method to manufacture and package a plurality of elements
二、發明創作人	姓名	1.喬治伯格納(Georg BOGNER) 2.荷伯特布朗尼(Herbert BRUNNER) 3.沃夫甘雷克斯(Wolfgang LEX) 4.甘特懷特(Guenter WAITL)
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	住、居所(事務所)	德國 D-93049 理斯堡華能街 2 號
	代表人姓名	1.R.穆勒(Dr. Müller) 2.R.威特根(Wittgen)

頃請修正本國民91年3月1日所提之修正本，無變更原內容是否准予修正。

91.3.1

A5
B5

四、中文發明摘要（發明之名稱：　　）

具有半導體晶片之光電構件、具有多個構件之模組、光學顯示裝置、照明或背景照明裝置、液晶顯示器、製造與封裝多個構件之方法

本發明是有關於具有半導體晶片(1)之光電構件，其安裝於撓性晶片載體(6)上，其中在第一主要表面上形成導軌(3,5)用於電性連接半導體晶片(1)，並且在其上配置殼體框架(7)，其以一種光線透過介質尤其以一種填充材料填滿。此外，提供一種顯示裝置，一種照明與背景照明裝置，以及製造根據本發明構件之方法。

第 1 圖

英文發明摘要（發明之名稱：　　）

Opto-electronic element with a semiconductor chip, Module with a semiconductor chip, Module with a plurality of elements, optical display device, illumination or background illumination device, liquid crystal display, and method to manufacture and package a plurality of elements

The present invention relates to an opto-electronic member containing semiconductor-chip (1), which is mounted on a flexible chip carrier (6), wherein on the first main surface is formed the conductive tracks (3, 5) to electrically connect the semiconductor chips (1), and on that is arranged a housing frame (7), which is filled with a light-transmitting medium, especially with a filling-material. Besides, it is provided with a displaying device, an illumination – or background illumination device, and a method to manufacture the members according to this invention.

(Figure 1)

（請先閱讀背面之注意事項再填寫本頁各欄）

裝　訂　線

經濟部智慧財產局員工消費合作社印製

本紙張尺度適用中國國家標準（CNS）A4規格（210×297公釐）

91 3 1

六、申請專利範圍

第 90120710 號「具有半導體晶片之光電構件、具有多個構件之模組、光學顯示裝置、照明或背景照明裝置、液晶顯示器、製造與封裝多個構件之方法」專利案　　(91 年 2 月修正)

六申請專利範圍

1. 一種具有半導體晶片(1)之光電構件,其安裝於撓性晶片載體(6)上,其特徵爲

其中在第一主要表面上形成導軌(3,5)用於電性連接性此等半導體晶片(1),並且在此表面上配置殼體框架(7),其以可透光介質,尤其以填充材料填滿。

2. 如申請專利範圍第 1 項之構件,其中

此半導體晶片是發光二極體晶片(1)。

3. 如申請專利範圍第 2 項之構件,其中

此殼體框架(7)之內部表面形成作爲反射器,其將由半導體晶片(1)側面對發射方向(9)所發射之電磁射線反轉方向,及/或將一個由在構件外部所產生由半導體晶片(1)可接收之電磁射線對此反轉方向。

4. 如申請專利範圍第 1 至 3 項中任一項之構件,其中

在此晶片載體(6)之面對第一主要表面之第二主要表面上形成屏蔽層用以屏蔽干擾波。

5. 如申請專利範圍第 1 或 2 項之構件,其中

此填充材料包括發光材料及/或擴散材料。

6. 一種模組,其具有多個如申請專利範圍第 2 至 5 項中任一項之構件,其特徵爲:

其中載軌構件(19)設有多個洞孔(20),並且此等構件各

六、申請專利範圍

與晶片載體(6)須固定於載體元件(19)之構件面,使得此等載體框架(7)各突出進入或突出穿過各此等洞孔(20)中。

7. 如申請專利範圍第 6 項之模組,其中

此載體元件(19)形成撓性。

8. 如申請專利範圍第 6 或 7 項之模組,其中

在載體(19)上形成電性線路結構,用於電性連接此等構件。

9. 一種光學顯示裝置,具有如申請專利範圍第 6 至 8 項中任一項之模組,其特徵爲:

此等載體元件(19)之光線發射表面會吸收光線(尤其會變黑)。

10. 一種照明或背景照明裝置,其具有如申請專利範圍第 6 至 8 項中任一項之模組,其特徵爲:

此等載體元件(19)之光線發射表面擴散式地反射尤其成爲白色光。

11. 如申請專利範圍第 10 項之照明或背景照明裝置,其中此載體元件(19)之光線發射側額外地配置擴散板(22)。

12. 一種液晶顯示器,其特徵爲:

它是配置於如申請專利範圍第 10 或 11 項之裝置之背向觀看面之面上。

13. 一種製造與封裝多個如申請專利範圍第 1 至 5 項中任一項之構件所用之方法,其特徵爲具有以下步驟:

a)提供一些晶片載體箔帶;

b)製造多個導軌對(3,5),用於在晶片載體箔帶上之各半導

煩請委員明示 年 月 日所提之修正本有無變更實質內容是否准予修正。

六、申請專利範圍

體晶片(1),

c)在晶片載體箔帶之各位置上形成各殼體框架(7),在其上(尤其借助於射出成形射出壓擠方法)設置各個構件之半導體晶片(1)或半導體晶片配置,

d)在此晶片載體箔帶上安裝多個半導體晶片(1),以及

e)將此由殼體框架(7)所形成之發射窗口,至少以填充材料(10)部份地填滿。

14.如申請專利範圍第 13 項之方法,其中

此具有安裝與封裝之半導體晶片之晶片載體箔帶被發展成具有多個可表面安裝構件之封裝單元。

Patent/Publication Number	200522396
Title	Light emitting devices with enhanced luminous efficiency
Issued/Publication Date	2005/07/01
Application Date	2004/10/28
Application Number	093132834 Espacenet
IPC	H01L-033/00
Inventor	STEIGERWALD, DANIEL A. US; COLLINS, WILLIAN DAVID US; FLETCHER, ROBERT M. US; LUDOWISE, MICHAEL JOSEPH US; POSSELT, JASON L. US
Applicant	LUMILEDS LIGHTING U.S. LLCUS
Priority Number	20031031 US 20030699433
Abstract	A structure includes semiconductor light emitting device and a wavelength-converting layer. The wavelength-converting layer converts a portion of the light emitted from the semiconductor light-emitting device. The dominant wavelength of the combined light from the semiconductor light emitting device and the wavelength-converting layer is essentially the same as the wavelength of light emitted from the device. The wavelength-converting layer may emit light having a spectral luminous efficacy greater than the spectral luminous efficiency of the light emitted from the device. Thus, the structure has a higher luminous efficiency than a device without a wavelength-converting layer.
Individual	F

發明專利說明書

200636049

（本說明書格式、順序及粗體字，請勿任意更動，※記號部分請勿填寫）

※ 申請案號：

※ 申請日期：　　※IPC 分類：C09K 11/77
H01L 33/00

一、發明名稱：（中文/英文）

包含一輻射源及螢光材料之照明系統

ILLUMINATION SYSTEM COMPRISING A RADIATION SOURCE AND A FLUORESCENT MATERIAL

二、申 請 人：（共 1 人）

姓名或名稱：（中文/英文）

荷蘭商皇家飛利浦電子股份有限公司

KONINKLIJKE PHILIPS ELECTRONICS N.V.

代表人：（中文/英文）

J L 凡 德 渥

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荷蘭　THE NETHERLANDS

三、發明人：（共 4 人）

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4. 漢斯迪爾特　包森
   BAUSEN, HANS-DIETER

國　籍：（中文/英文）

1. 德國　GERMANY
2. 德國　GERMANY
3. 德國　GERMANY
4. 德國　GERMANY

四、聲明事項：

☐ 主張專利法第二十二條第二項☐第一款或☐第二款規定之事實，其事實發生日期為：　年　月　日。

☑ 申請前已向下列國家（地區）申請專利：

【格式請依：受理國家（地區）、申請日、申請案號　順序註記】

☑ 有主張專利法第二十七條第一項國際優先權：

1. 歐洲專利機構；2005年03月09日；05101834.9

2.

☐ 無主張專利法第二十七條第一項國際優先權：

1.

2.

☐ 主張專利法第二十九條第一項國內優先權：

【格式請依：申請日、申請案號　順序註記】

☐ 主張專利法第三十條生物材料：

☐ 須寄存生物材料者：

國內生物材料　【格式請依：寄存機構、日期、號碼　順序註記】

國外生物材料　【格式請依：寄存國家、機構、日期、號碼　順序註記】

☐ 不須寄存生物材料者：

所屬技術領域中具有通常知識者易於獲得時，不須寄存。

五、中文發明摘要：

本發明係關於一種用於產生彩色光的照明系統，特別是產生琥珀或紅色光，該照明系統包含一輻射源及一螢光材料，該螢光材料包含至少一磷光體，能夠吸收由該輻射源所發射之一部分光且發射波長與被吸收光不同的光；其中該至少一磷光體為一通式為$(Ca_{1-x-y-z}Sr_xBa_yMg_z)_{1-n}(Al_{1-a+b}B_a)Si_{1-b}N_{3-b}O_b:RE_n$的發射琥珀至紅色光之稀土金屬活化氧基次氮基鋁矽酸鹽，其中$0\leq x\leq 1$、$0\leq y\leq 1$、$0\leq z\leq 1$、$0\leq a\leq 1$、$0<b\leq 1$及$0.002\leq n\leq 0.2$，且RE係選自銪(II)及銪(III)。

本發明亦關於一種一通式為$(Ca_{1-x-y-z}Sr_xBa_yMg_z)_{1-n}(Al_{1-a+b}B_a)Si_{1-b}N_{3-b}O_b:RE_n$的發射琥珀或紅色光之稀土金屬活化氧基次氮基鋁矽酸鹽，其中$0\leq x\leq 1$、$0\leq y\leq 1$、$0\leq z\leq 1$、$0\leq a\leq 1$、$0<b\leq 1$其$0.002\leq n\leq 0.2$，且RE係選自銪(II)及銪(III)。

六、英文發明摘要：

ABSTRACT:

The invention concerns an illumination system for generation of colored, especially amber or red light, comprising a radiation source and a fluorescent material comprising at least one phosphor capable of absorbing a part of light emitted by the radiation source and emitting light of wavelength different from that of the absorbed light; wherein said at least one phosphor is a amber to red emitting a rare earth metal-activated oxonitridoalumosilicate of general formula $(Ca_{1-x-y-z}Sr_xBa_yMg_z)_{1-n}(Al_{1-a+b}B_a)Si_{1-b}N_{3-b}O_b:RE_n$, wherein $0 \le x \le 1$, $0 \le y \le 1$, $0 \le z \le 1$, $0 \le a \le 1$, $0 < b \le 1$ and $0.002 \le n \le 0.2$ and RE is selected from europium(II) and cerium(III).

The invention is also concerned with a amber or red-emitting a rare earth metal-activated oxonitridoalumosilicate of general formula $(Ca_{1-x-y-z}Sr_xBa_yMg_z)_{1-n}(Al_{1-a+b}B_a)Si_{1-b}N_{3-b}O_b:RE_n$, wherein $0 \le x \le 1$, $0 \le y \le 1$, $0 \le z \le 1$, $0 \le a \le 1$, $0 < b \le 1$ and $0.002 \le n \le 0.2$ and RE is selected from europium(II) and cerium(III).

Fig. 4

案號：109207	國外相應案：☑見申請書 ☐其他：		
申說份數：1	☐改中文 Title	☐細則§17 但書	字數：
☑原文說明書檔名：p:\Foreign Spec\ -filing			待檢人：
送者：	容稿者：	代表圖：	化學式：

七、指定代表圖：

(一)本案指定代表圖為：第（4）圖。

(二)本代表圖之元件符號簡單說明：

(無元件符號說明)

八、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

(無)

九、發明說明：

【發明所屬之技術領域】

本發明大體上係關於一種照明系統，其包括一輻射源及一含有琥珀至紅色磷光體的螢光材料。本發明亦關於一種用於此類照明系統之琥珀至紅色的磷光體。

更特定言之，本發明係關於一種照明系統，其包括一場致發光半導體裝置，用於作為輻射源，及包括一含有一磷光體之螢光材料，用於產生特定的白光或彩色光，包括黃色、琥珀及紅色光。

【先前技術】

此照明系統中，係基於一紫外光或藍色主要輻射，藉由發光下轉換加上色彩混合，來產生白光或特定的彩色光。

此類照明系統特別有利於交通工具及發信號的應用。

交通工具中，包括許多不同的組件和裝配件具有照明器或附屬的信號燈。使用冷光二極體裝置，例如固態發光二極體(Light Emitting Diode；LED)，作為照明器及信號指示器受到很大的注意，因為與其它傳統的低電壓光源相比，這些裝置提供許多潛在的優點。其它光源的缺點包括：它們效率相當差，例如傳統鎢白熱燈；其需要以高電壓操作，例如螢光及氣體放電燈；或容易損壞，例如白熱燈。

因此，對於只能提供有限電力或低電壓的交通工具，或因為安全的理由而不能使用高壓的應用，或會遭遇嚴重衝擊或振動的應用等方面而言，這些替代性光源並非最佳選

擇。另一方面，LED具有極高的衝擊耐受能力，因此與受到機械或熱衝擊時會爆裂的白熱或螢光燈泡相比，它佔有很大的優勢。與白熱燈典型的1,000到2,000小時或螢光燈的5,000到10,000小時相比，LED亦擁有200,000到1,000,000小時的操作使用期限。

現有的黃、琥珀或紅色交通號誌及交通工具燈光中包含冷光半導體裝置，其依靠直接激勵鋁鎵銦磷化物(AlGaInP) LED晶片來產生黃、琥珀或紅等彩色光。

AlInGaP LED的缺點是會隨溫度升高而發生發光淬火。當溫度從室溫上升到100℃時，它們的發光量降低40%以上。同時，其頻譜發生偏移，例如從617 nm偏移到623 nm，此進一步降低照明效率。因此，汽車工業殷切需要光輸出及發射頻譜較不會被溫度影響的黃至紅色LED。

目前用來產生黃、琥珀或紅光的解決方案中，有一種做法是應用白色LED及適當的彩色濾鏡，這是因為AlInGaN晶片應用於白光LED中發生熱淬火的情況較少。此外，由於其使用了YAG:Ce磷光體，因此白光LED隨溫度而發生頻譜偏移的情形較不嚴重。然而，這種概念的主要缺點是低效率，因為目前的白光LED只發射少量的橙至紅色光，且大部分的白光LED頻譜都被截斷。

另一種方法為美國6,649,946號專利所揭露，其中使用一發射黃至紅光的磷光體來產生黃至紅光之光源。該磷光體具有一氮化矽酸鹽類式$M_XSi_yN_Z$:Eu的主晶格，其中M為至少一選自Ca、Sr、Ba、Zn所組成群組之稀土金屬，且其中

$z=2/3x+4/3y$。此磷光體可用來產生穩定性很高的發射紅色或橙色或黃色LED，其可以基於發射峰值為380至480 nm之主要光源(較佳係InGaN晶片)，該主要光源之光由一該發明型式之摻雜Eu的稀土金屬-活化氮化物磷光體加以完全轉換。與眾所熟知之直接激勵黃至紅光的市售LED相比，這些LED展現更高的效率及改良的穩定性。

然而，近來針對交通號誌所作的色品需求評估，交通工具之紅色範圍及交通號誌必須包括較長的波長截斷，以確保彩色視力不良的駕駛能夠偵測到號誌。

因此有必要提供一種照明系統，其包含可以被接近UV至藍光範圍之輻射源激勵且發射可見琥珀至深紅色範圍的磷光體。

因此本發明提供一種照明系統，其包含一輻射源及一螢光材料，該螢光材料包含至少一磷光體，能夠吸收由該輻射源所發射之一部分光，且發射波長與該被吸收光不同的光；其中該至少一磷光體為一通式為$(Ca_{1-x-y-z}Sr_xBa_yMg_z)_{1-n}(Al_{1-a+b}B_a)Si_{1-b}N_{3-b}O_b:RE_n$的稀有稀土金屬活化氧基次氮基鋁矽酸鹽，其中$0\leq x\leq 1$、$0\leq y\leq 1$、$0\leq z\leq 1$、$0\leq a\leq 1$、$0<b\leq 1$及$0.002\leq n\leq 0.2$，且RE係選自銪(II)及銪(III)。

依據本發明之照明系統可提供一複合的彩色輸出光，特別是同時具備高溫耐受性、色點穩定性及高效率之琥珀或紅色光。

尤其是，相較於傳統的燈光，該複合輸出光在深紅色範圍的發射量更大，且擴大可呈現的色彩範圍。此特徵使裝

置能夠理想地用於例如黃色、琥珀及紅色的交通照明、樓梯/安全門燈照明、裝飾照明及交通工具訊號照明等應用上。

依據本發明之照明系統亦可提供複合白輸出光，其在顏色方面已經過良好地平衡。尤其是，相較於傳統的燈光，此複合白輸出光在紅色範圍的發射量更大。此特徵使裝置可理想地用於需要呈現真實色彩的應用上。本發明在這些方面的應用包括，特別是，交通照明、街道照明、安全照明，以及自動化工廠的照明。

尤其預期要用來作為該輻射源者，係固態發光二極體。

【發明內容】

本發明之一第一方面提供一照明系統，其包含一藍色發光二極體及一螢光材料，該藍色發光二極體具有420到495 nm之峰值發射波長作為輻射源，該螢光材料包含至少一磷光體，其為一通式為$(Ca_{1-x-y-z}Sr_xBa_yMg_z)_{1-n}(Al_{1-a+b}B_a)Si_{1-b}N_{3-b}O_b:RE_n$之稀土金屬活化氧基次氮基鋁矽酸鹽，其中$0\leq x\leq 1$，$0\leq y\leq 1$，$0\leq z\leq 1$，$0\leq a\leq 1$，$0<b\leq 1$及$0.002\leq n\leq 0.2$，且RE係選自銪(II)及銪(III)。

此照明系統在操作時將提供白光或彩色光，尤其是琥珀或紅色光。由LED所發射的藍光激勵該磷光體，使其發射琥珀或紅色光。由LED所發射的藍光透射穿過該磷光體，並與該磷光體所發射的琥珀或紅色光混合。混合後之該藍色和琥珀色光之混合物被觀察者感知為白光或彩色光，視該螢光材料中所出現磷光體的量而定。

本發明之一具體實施例提供一發射一白光或彩色光，尤其是琥珀或紅色光之照明系統，該照明系統包含一藍色發光二極體及一螢光材料，該藍色發光二極體該具有420到495 nm之峰值發射波長作為輻射源，該螢光材料包含一通式為$(Ca_{1-x-y-z}Sr_xBa_yMg_z)_{1-n}(Al_{1-a+b}B_a)Si_{1-b}N_{3-b}O_b:RE_n$之稀土金屬活化氧基次氮基鋁矽酸鹽，其中$0\leq x\leq 1$，$0\leq y\leq 1$，$0\leq z\leq 1$，$0\leq a\leq 1$，$0<b\leq 1$及$0.002\leq n\leq 0.2$，且RE係選自銪(II)及銪(III)。

當該螢光材料包含一磷光體其係由一稀土金屬活化氧基次氮基鋁矽酸鹽類之磷光體與至少一第二磷光體所混合而成時，可進一步改進依據本發明之白光或彩色光照明系統之色彩還原。

特定言之，該螢光材料可為一磷光體混合物，其包含一通式為$(Ca_{1-x-y-z}Sr_xBa_yMg_z)_{1-n}(Al_{1-a+b}B_a)Si_{1-b}N_{3-b}O_b:RE_n$之稀土金屬活化氧基次氮基鋁矽酸鹽(其中$0\leq x\leq 1$，$0\leq y\leq 1$，$0\leq z\leq 1$，$0\leq a\leq 1$，$0<b\leq 1$及$0.002\leq n\leq 0.2$，且RE係選自銪(II)及銪(III))及一紅色磷光體。該紅色磷光體可選自由$Ca_{1-x-y}Sr_xS:Eu_y$(其中$0\leq x\leq 1$及$0<y\leq 0.2$)及$(Sr_{1-x-y}Ba_xCa_y)_2Si_5N_8:Eu_z$(其中≤x≤1，$0\leq y\leq 1$及$0<z\leq 0.2$)所組成的群組。

或者，該螢光材料可為一磷光體混合物，其包含一通式為$(Ca_{1-x-y-z}Sr_xBa_yMg_z)_{1-n}(Al_{1-a+b}B_a)Si_{1-b}N_{3-b}O_b:RE_n$之稀有稀土金屬活化氧基次氮基鋁矽酸鹽(其中$0\leq x\leq 1$，$0\leq y\leq 1$，$0\leq z\leq 1$，$0\leq a\leq 1$，$0<b\leq 1$及$0.002\leq n\leq 0.2$，且RE係選自銪(II)及銪(III))及一黃至綠色磷光體。該黃至綠色磷光體可選自

由 $(Ca_xSr_{1-x-y})_2SiO_4:Eu_y$(其中 $0\leq x\leq$ 及 $0<y\leq 0.2$)、$(Sr_xBa_{1-x-y})_2SiO_4:Eu_y$(其中 $0\leq x\leq 1$ 及 $0<y\leq 0.2$)、$(Sr_{1-x-y}Ba_x)Ga_2S_4:Eu_y$(其中 $0\leq x\leq 1$ 及 $0<y\leq 0.2$)、$(Y_{1-x-y-z}Gd_xLu_z)_3(Al_{1-a}Ga_a)_5O_{12}:Ce_y$,(其中 $0\leq x\leq 1$ 及 $0<y\leq 0.2$,$0\leq z\leq 1$,$0\leq a\leq 0.5$)、ZnS:Cu、CaS:Ce,Cl及$SrSi_2N_2O_2$:Eu所組成的群組。

此一包括額外磷光體的螢光材料之發射光譜具有適當的波長,可連同LED之藍光與依據本發明之稀土金屬活化氧基次氮基鋁矽酸鹽類磷光體之琥珀至紅色光,得到在需要之色溫下具有良好色彩還原的高品質彩色光。

本發明之另一方面提供一白光或彩色光特別是琥珀或紅色光的照明系統,其中輻射源係選自具有峰值發射波長在200至400 nm之UV-範圍的發光二極體,且其螢光材料包含至少一磷光體,其為一通式為$(Ca_{1-x-y-z}Sr_xBa_yMg_z)_{1-n}(Al_{1-a+b}B_a)Si_{1-b}N_{3-b}O_b:RE_n$之稀有稀土金屬活化氧基次氮基鋁矽酸鹽及一黃至綠色磷光體,其中 $0\leq x\leq 1$,$0\leq y\leq 1$,$0\leq z\leq 1$,$0\leq a\leq 1$,$0<b\leq 1$ 及 $0.002\leq n\leq 0.2$,且RE係選自銪(II)及銪(III)。

依據本發明之一具體實施例提供一白光照明系統,其包含一藍色發光二極體及一螢光材料,該藍色發光二極體具有200到420 nm之峰值發射波長作為輻射源,該螢光材料包含一通式為$(Ca_{1-x-y-z}Sr_xBa_yMg_z)_{1-n}(Al_{1-a+b}B_a)Si_{1-b}N_{3-b}O_b:RE_n$之稀土金屬活化氧基次氮基鋁矽酸鹽(其中 $0\leq x\leq 1$,$0\leq y\leq 1$,$0\leq z\leq 1$,$0\leq a\leq 1$,$0<b\leq 1$ 及 $0.002\leq n\leq 0.2$,且RE係選自銪(II)及銪(III))及至少一第二磷光體。

特定言之，該螢光材料可為一磷光體混合物，其包含一通式為$(Ca_{1-x-y-z}Sr_xBa_yMg_z)_{1-n}(Al_{1-a+b}B_a)Si_{1-b}N_{3-b}O_b:RE_n$之稀有稀土金屬活化氧基次氮基鋁矽酸鹽(其中$0\leq x\leq 1$，$0\leq y\leq 1$，$0\leq z\leq 1$，$0\leq a\leq 1$，$0<b\leq 1$及$0.002\leq n\leq 0.2$，且RE係選自銪(II)及銪(III))及一藍色磷光體。該藍色磷光體可選自包含$BaMgAl_{10}O_{17}$：Eu、$Ba_5SiO_4(Cl, Br)_6$：Eu, $CaLa_2S_4$:Ce以及$(Sr,Ba,Ca)_5(PO_4)_3Cl$：Eu所組成的群組。

此一包含額外磷光體之螢光材料之發射光譜具有適當的波長，能夠連同LED的藍色光與依據本發明之稀有稀土金屬-活化氧基次氮基鋁矽酸鹽類磷光體的琥珀至紅色光，得到在需要的色溫下具有良好的色彩還原的高品質彩色光。

本發明另一方面提供一磷光體，其能夠吸收由輻射源所發射之一部分光且發射波長與該被吸收光不同的光；其中該磷光體係一通式為$(Ca_{1-x-y-z}Sr_xBa_yMg_z)_{1-n}(Al_{1-a+b}B_a)Si_{1-b}N_{3-b}O_b:RE_n$的稀有稀土金屬活化氧基次氮基鋁矽酸鹽，其中$0\leq x\leq 1$、$0\leq y\leq 1$、$0\leq z\leq 1$、$0\leq a\leq 1$、$0<b\leq 1$及$0.002\leq n\leq 0.2$，且RE係選自銪(II)及銪(III)。

藉由改變該磷光體的化學組成，可將該磷光體的顏色從琥珀色偏移至深紅色。發射光譜擴大到相當不易達到的頻譜範圍，包括深紅色及接近紫外光的區域。

該螢光材料可由波長從300 nm至400 nm之此類UV-A射線所激勵，但亦能有效地以藍色發光二極體所發射之波長在大約400到495 nm的藍色光加以激勵。因此該螢光材料

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具有能夠將氮化物半導體的藍發光成分轉換為白光或彩色光的理想特性。

這些磷光體為寬頻帶發射器，其中可見部分的發射相當寬，以致於可見發射之主要所在位置不存在80 nm的波長範圍。總轉換效率可高達98 %。

此種稀土金屬活化氧基次氮基鋁矽酸鹽類磷光體之額外重要特徵包括1)在典型裝置操作溫度(例如80℃)下能夠耐受發光之熱淬火；2)不會干擾與裝置製造中所使用封裝樹脂的反應；3)合適的吸收性輪廓，可最小化可見頻譜範圍內的靜止吸收；4)裝置的使用期限內恆常穩定的發光輸出；以及5)可控制組成以調整磷光體的激勵與發射特性。

這些稀有稀土金屬-活化氧基次氮基鋁矽酸鹽類磷光體亦可可包括鐿、鐠、釤及其它陽離子，包括作為共活化劑的陽離子混合物。

該等磷光體可具有一選自由元素鋁、銃、釔、鑥、釓及鎦之氟化物及正磷酸鹽與鋁、釔、矽及鑥之氧化物以及鋁之氮化物所組成群組的塗層。

【實施方式】

稀土金屬-活化氧基次氮基鋁矽酸鹽磷光體

本發明著重於在一任何組態之一輻射源的照明系統中，一稀土金屬活化氧基次氮基鋁矽酸鹽作為磷光體，該輻射源包括，但不限於，放電燈、螢光燈、LED、LD以及X-射線管。本說明書中，術語「輻射」涵蓋UV、IR及電磁光譜中可見範圍內的輻射。

雖然本發明之磷光體預期可應用於廣泛的照明陣列，但本發明係特別參考轉換磷光體之發光二極體及其特定應用作說明，該發光二極體包含特別是UV和藍色發光二極體作為輻射源的發光二極體。

該磷光體符合通式$(Ca_{1-x-y-z}Sr_xBa_yMg_z)_{1-n}(Al_{1-a+b}B_a)Si_{1-b}N_{3-b}O_b:R_{En}$，其中$0\leq x\leq 1$，$0\leq y\leq 1$，$0\leq z\leq 1$，$0\leq a\leq 1$，$0<b\leq 1$及$0.002\leq n\leq 0.2$，且RE係選自銪(II)及銪(III)。

此種磷光材料之類別係基於以鋁取代氧代氮化矽酸鹽之稀土金屬活化發光。該磷光體包含一主晶格，其中主要組成為矽、鋁、氮及氧。該主晶格亦可包含硼。

主要層具有包含$[(Al,Si)_2N_{6/3}(N,O)_{2/2}]$堆疊層的結構，其中矽和鋁的四面被氧和氮所包圍，請參見圖2。若鋁/矽的比同時變化以維持離子平衡，則連接兩個矽或鋁原子的氮原子可以由氧取代。因此可製備$MAlSiN_3MA_{12}N_2O$系統內的固溶體。

由先驅物材料或燃燒大氣所造成磷光體中的氧缺陷可藉由改變先驅混合物中Al/Si的比而予以補償。螢光材料中較低的缺陷密度導致效率較高且較好的光化學穩定性。

各層中，例如稀土金屬以及銪(II)、鈰(III)等金屬陽離子最終會與一共活化劑結合。其主要由連接2個鋁的N原子或矽原子或由替代的氧原子加以配位結合。該等稀土金屬較佳地選自鎂、鈣、鍶及鋇。

稀土金屬中的比例n較佳地在$0.002\leq n\leq 0.2$的範圍。當比例n較低時，亮度會下降，這是因為稀有稀土金屬陽離子

減少，使得光致發光發射中心被激勵的數目減少，當n大於0.2時，則會發生濃度淬滅。濃度淬滅指的是，為了提高螢光材料光度而添加的催化劑之濃度增加至超出最佳位準時，所發生的發射強度降低的現象。

用於製造本發明之微晶磷光體粉末之方法並無特別限制，可以使用任何提供依據本發明之磷光體的方法。可製造出一系列通式為$(Ca_{1-x-y-z}Sr_xBa_yMg_z)_{1-n}(Al_{1-a+b}B_a)Si_{1-b}N_{3-b}O_b:RE_n$之組成物通式，其中$0\leq x\leq 1$，$0\leq y\leq 1$，$0\leq z\leq 1$，$0\leq a\leq 1$，$0<b\leq 1$及$0.002\leq n\leq 0.2$，且RE係選自銪(II)及銪(III)。

一種製造依據本發明之磷光體的較佳程序為固態法。此程序中，將磷光體先驅物材料在固態下混合並予以加熱，使該先驅物反應而形成磷光體材料粉末。

以預定的比例將鹼土金屬氮化物與無結晶氮化矽(Si_3N_4)、氮化鋁(AlN)粉末、銪及/或鈰的氟化物混合，最後並加以熔融。

將混合物置於一高純度鉬坩堝中。把坩堝送進管爐以流動的氮氣/氫氣淨化數小時。爐子參數為，以10℃/分鐘升溫至1450℃，然後在1450℃維持4小時，之後使爐子緩慢冷卻到室溫。

再次把樣品磨成細粉，然後以1400℃進行第二次退火步驟。

可以用稍低的溫度，於流動的氫氣中透過額外的第三次退火，以改善光度輸出。

燃燒之後，以粉末的X-射線繞射(Cu，Kα-線)定出該粉末之特徵，其顯示需要的相已然形成。

如此得到琥珀至紅色的粉末，其在UV及藍光的激勵下有效率地發光。

依據本發明之稀土金屬活化氧基次氮基鋁矽酸鹽類磷光體可較佳地塗布一選自元素鋁、銃、釔、鑭、釓及鎦之氟化物及正磷酸鹽及鋁、釔、矽及鑭之氧化物以及鋁之氮化物等所組成群組之一或多種化合物之薄而均勻的保護層。

此保護層的厚度一般是在0.001至0.2 μm的範圍，已薄到可以讓輻射源之輻射穿透而實質上並不會損失能量。可藉由例如氣相或濕式塗布程序將這些材料塗層塗布於該磷光體粒子上。

依據本發明之磷光體，由於其氧基次氮基鋁矽酸鹽結構，因此能夠耐熱、光及濕。

這些稀土金屬活化氧基次氮基鋁矽酸鹽磷光體在被UVA輻射或電磁光譜藍光範圍激勵時係產生寬頻帶發射，其峰值波長在琥珀至深紅色的範圍，尾端發射達到紅外線的範圍。

較佳地，使用銪(II)作為活化劑。

表1為某些以銪 (II)活化之磷光體的頻譜資料。

表1：

組成物	Em,max	QE450	RQ450	x	y	LE
$CaAlSi(N,O)_3$:Eu(2%)	652 nm	86,1	35,2	0.657	0.342	125,3
$Ca_{0.95}Sr_{0.05}AlSi(N,O)_3$:Eu(2%)	657 nm	86.8	17.3	0.68	0.318	82
$Ca_{0.9}5Ba_{0.05}AlSi(N,O)_3$:Eu(2%)	658 nm	883.5	17.5	0.676	0.323	93.2
$CaAl_{0.98}B_{0.02}Si(N,O)_3$:Eu(2%)	650 nm	81.6	19.4	0.667	0.332	108.1
$CaAl_{0.95}B_{0.05}Si(N,O)_3$:Eu(2%)	654 nm	84.1	20.2	0.663	0.336	113
$Ca_{0.95}Mg_{0.05}AlSi(N,O)_3$:Eu(2%)	652 nm	86.1	35.2	0.657	0.342	125.3
$Ca_{0.9}Mg_{0.1}AlSi(N,O)_3$:Eu(2%)	645 nm	78.3	24.9	0.63	0.368	155.5
$Ca_{0.5}Mg_{0.5}AlSi(N,O)_3$:Eu(2%)	633 nm	70.8	36.3	0.578	0.418	222.4

將一以銪活化氧基次氮基鋁矽酸鹽中之一些或全部的銪以鈰取代產生如下的效果：鈰產生集中在黃色至琥珀色區域之可見頻譜的次要發射，而非從以銪(II)活化氧基次氮基鋁矽酸鹽磷光體一般集中在深紅區域之可見光頻譜的典型寬頻帶次要發射。

亦可使用例如鐿、鐠、釤、鈥、鉺、鏑、釩及鋱等共活化劑。可將鹼金屬之類的單價陽離子以匹配於或低於所含Ce(III)的量之數量納入到主晶格中，予以電荷補償。

表2為某些以鈰(III)活化之化合物的頻譜資料。

表2：

樣本	組成物	Em, max	QE_{450}	RQ_{450}	x	y	LE
WM7804	$CaAlSiN_3$:Ce (2%)	610 nm	75.2	45.2	0.502	0.48	340
WM8204	$CaAlSiN_3$:Ce,Eu (2%, 0.1%)	631 nm	78.2	49.6	0.55	0.438	271.5
WM8304	$CaAlSiN_3$:Ce,Na (2%, 0.1%)	564 nm	76.9	54.5	0.471	0.505	383.3
WM9004	$CaAlSiN_3$:Ce (2%)	571 nm	82.5	43.4	0.47	0.51	400.6
WM9004A	$CaAlSiN_3$:Ce (2%)	569 nm	81.8	39.9	0.472	0.508	399.5

WM9304	$CaAlSiN_3$:Ce (4%)	583 nm	74.5	26.9	0.501	0.487	366.4
WM9404	$CaAlSiN_3$:Ce,Pr (2%, 0.5%)	568 nm	74.5	36.5	0.477	0.503	390.1
WM9504B	$CaAlSiN_3$:Ce (2%) 及SiO_2塗層	571 nm	69.9	30.1	0.476	0.505	391.5

照明系統

本發明亦關於一包含一輻射源及一螢光材料之照明系統，該螢光材料包含至少一通式為$(Ca_{1-x-y-z}Sr_xBa_yMg_z)_{1-n}(Al_{1-a+b}B_a)Si_{1-b}N_{3-b}O_b:RE_n$的稀土金屬氧基次氮基鋁矽酸鹽，其中$0\leq x\leq 1$，$0\leq y\leq 1$，$0\leq z\leq 1$，$0\leq a\leq 1$，$0<b\leq 1$及$0.002\leq n\leq 0.2$，且RE係選自銪(II)及銪(III)。

輻射源包括半導體光學輻射發射器及其它回應電激勵發射光學輻射的裝置。半導體光學輻射發射器包括發光二極體LED晶片，發光聚合物(Light Emitting Polymer；LEP)、有機發光裝置(Organic Light Emitting Device；OLED)、聚合物發光裝置(Polymer Light Emitting Device；PLED)等。

此外，例如用於放電燈及螢光燈(例如水銀低及高壓放電燈、硫磺放電燈以及基於分子輻射體的放電燈)的發光組件亦預期將連同本發明之磷光體組成物一起使用來作為輻射源。

在本發明之一較佳具體實施例中，該輻射源為一固態發光二極體。

包括一固態LED及一稀土金屬活化氧基次氮基鋁矽酸鹽磷光組成物的照明系統之任一組態，都視為在本發明的範

圍內，較佳係加入其它眾所熟知的磷光體，其組合之後，在受到如前述由一LED所發射的主要UV或藍輻射照射時，可獲得一特定顏色的琥珀、紅色光或白光。

以下說明圖1所示之包含一輻射源及一螢光材料之此照明系統之一具體實施例的詳細構造。

圖1顯示一包含該螢光材料之塗層的晶片型發光二極體的示意圖。該裝置包含一作為輻射源的晶片型發光二極體(LED)1。該發光二極體晶粒被定位於一反射器杯導線架2中。晶粒1經由一焊線7連接至一第一端子6，以及直接連接至一第二電性端子6。該反射器杯的凹處填充依據本發明之含有螢光材料4、5的塗層材料，形成一內嵌於該反射器杯的塗層。該等磷光體係個別或以混合物的形式塗布。

塗層材料通常包含一聚合物3，用以封裝磷光體或磷光體混合物。這些具體實施例中，該等磷光體或磷光體混合物應具備能夠耐受該封裝物之高度穩定性的性質。較佳係，該聚合物具光學清晰的特性，以避免嚴重的光散射。在LED工業中，已知有許多不同的聚合物可用來製造LED燈。

在一具體實施例中，該聚合物係選自環氧樹脂及矽樹脂所組成的群組。將磷光體混合物加入到一聚合物先驅物液體中可以完成封裝。例如，該磷光體混合物可為一粒狀粉末。將該等磷光體粒子引入到聚合物先驅物液體中，會形成淤漿(即粒子懸浮)。聚合之後，磷光體混合物便被封裝於固定位置。在一具體實施例中，該螢光材料及LED晶粒

都被封裝在聚合物中。

透明塗層材料可有利地包含光擴散粒子(所謂散光體)。此類散光體的範例包括礦物填料，特定言之，CaF_2、TiO_2、SiO_2、$CaCO_3$或$BaSO_4$或其它有機顏料。這些材料可以用簡單的方式加入到前述的樹脂中。

操作時，施加電力於晶粒以啟動該晶粒。晶粒啟動時會發射主要光，例如藍光。該已發射之主要光的一部分完全或部分被該塗層中的螢光材料所吸收。該螢光材料接著回應該主要光之吸收而發射次要光，亦即，轉換後的光線具有較長的峰值波長，主要是頻帶夠寬的琥珀至紅色光 (明確言之，深紅色光占很大的比例)。該已發射之主要光的其餘未被吸收部分與該次要光一起透射穿過該螢光層。該封裝將一般方向上未被吸收之主要光及次要光引導成為一輸出光。因此，該輸出光為從晶粒發射的主要光及從螢光層發射的次要光所組成的複合光。

依據本發明之照明系統之輸出光的色溫或色點會視該次要光相較於該主要光的光譜分佈與強度而改變。

首先，藉由適當地選擇發光二極體，可以改變該主要光的色溫或色點。

其次，藉由適當地選擇螢光材料中的磷光體、磷光體顆粒大小及施加磷光體的數量，可改變該次要光的色溫或色點。此外，這些配置有利地提供在該螢光材料中使用磷光體混合物的可能性，因此有助於甚至更精確地設定所需色調。

白磷光體轉換的發光裝置

依據本發明之一方面，該照明系統的輸出光可具有一顯現為「白」光的頻譜分佈。最普遍的白光LED由塗布一磷光體的藍色發光LED晶片所組成，該磷光體將一部分藍輻射轉換成互補的顏色，例如黃色至琥珀色的發射。該藍色及黃色一起發射產生白光。

尚有白色LED是採用一UV發射晶片及設計用於將UV輻射轉換成可見光的磷光體。一般而言，需要兩種或更多的磷光體發射頻帶。

藍色/磷光體白光LED

(使用藍色發光二極體之二色白光磷光體轉換的發光裝置)

在一第一具體實施例中，藉由選擇螢光材料，使得由藍色發光二極體所發射之一藍色輻射轉換為互補的波長範圍，以形成二色白光，可有利地產生依據本發明之一發射白光的照明系統。

此例中，琥珀至紅色光係藉由包含一稀土金屬活化氧基次氮基鋁矽酸鹽磷光體的螢光材料產生。此外，還可再使用一第二螢光材料，以改進此照明系統之色彩還原。

採用最大發射在400至490 nm的藍色LED可達到尤佳結果。對於稀土金屬活化氧基次氮基鋁矽酸鹽的激勵光譜而言，已發現440 nm可得最佳結果。

與先前技術之LED所產生的白輸出光的光譜分佈比較，光譜分佈的明顯差異為，在可見光譜紅光區域內之峰值波長的偏移。因此，與先前技術之LED所產生的輸出光比

較，由該照明系統所產生的白輸出光多出大量的紅色。

(使用藍色發光二極體之多色白光磷光體轉換的發光裝置)

在一第二具體實施例中，藉由選擇螢光材料，使得由藍色發光二極體所發射之一藍色輻射轉換為互補的波長範圍，以形成多色白光，可有利地產生依據本發明之一發射白光的照明系統。此例中，琥珀至紅色光係利用包含一稀土金屬活化氧基次氮基鋁矽酸鹽磷光體及一第二磷光體之磷光體混合物的螢光材料產生。

藉由使用涵蓋全部光譜範圍之額外的紅與綠寬頻帶發射器磷光體，連同一發射藍光的LED及一發射琥珀至紅色光的稀土金屬活化氧基次氮基鋁矽酸鹽磷光體，有可能產生具有甚高色彩還原之白光發射。

下表3摘要列出常用的第二磷光體及其光學特性。

表3：

組成物	λ_{max}[nm]	色點x、y
$(Ba_{1-x}Sr_x)_2SiO_4$：Eu	523	0.272, 0.640
$SrGa_2S_4$：Eu	535	0.270, 0.686
$SrSi_2N_2O_2$：Eu	541	0.356, 0.606
$Y_3Al_5O_{12}$:Ce	550	0.447, 0.535
SrS：Eu	610	0.627, 0.372
$(Sr_{1-x-y}Ca_xBa_y)_2Si_5N_8$:Eu	615	0.615, 0.384
$(Sr_{1-x-y}Ca_xBa_y)_2Si_{5-a}Al_aN_{8-a}$:Eu	615-650	0.633, 0.366
CaS：Eu	655	0.700, 0.303
$(Sr_{1-x}Ca_x)S$：Eu	610-655	*

該螢光材料可為兩種磷光體的混合物，其一為琥珀至紅色的稀土金屬活化氧代氮化鋁酸鹽磷光體，另一為選自

$(Ca_{1-x}Sr_x)S:Eu$(其中$0\leq x\leq 1$)及$(Sr_{1-x-y}Ba_xCa_y)_2Si_{5-a}Al_aN_{8-a}O_a:Eu$(其中$0\leq a\leq 5$，$0\leq x\leq 1$及$0\leq y\leq 1$)所組成群組之紅色磷光體。

該螢光材料可為兩種磷光體的混合物，例如，其一為琥珀至紅色的稀土金屬活化氧代氮化鋁酸鹽磷光體，另一為選自$(Ba_{1-x}Sr_x)_2SiO_4:Eu$，(其中$0\leq x\leq 1$)、$SrGa_2S_4:Eu$及$SrSi_2N_2O_2:Eu$所組成群組之綠色磷光體。

此情況中，藉由根據混合物與濃度來適當地選擇磷光體，可以改變所產生的白光的色調(CIE色度圖中的色點)。

UV/磷光體白光LED

(使用UV發光之二色白光磷光體轉換的發光裝置)

在另一具體實施例中，藉由選擇螢光材料，使得由UV發光二極體所發射之一UV輻射轉換為互補的波長範圍，以形成二色白光，可有利地產生依據本發明之一發射白光的照明系統。此例中，琥珀及藍色光係藉由螢光材料產生。琥珀色光係藉由包含一稀土金屬-活化氧基次氮基鋁矽酸鹽磷光體的螢光材料產生。藍色光係藉由包含一選自$BaMgAl_{10}O_{17}:Eu$、$Ba_5SiO_4(Cl、Br)_6:Eu$、$CaLn_2S_4:Ce$與$(Sr、Ba、Ca)_5(PO_4)_3Cl:Eu$所組成群組之藍色磷光體的螢光材料而產生。

結合一最大發射在200至400 nm之UVA發光二極體，可達到尤佳結果。對於稀土金屬活化氧基次氮基鋁矽酸鹽的激勵光譜而言，已發現365 nm可得最佳結果。

使用UV發射LED之多色白光磷光體轉換的發光裝置

在另一具體實施例中，藉由選擇螢光材料，使得由UV發光二極體所發射之一UV輻射轉換為互補的波長範圍，以形成多色白光(藉由添加例如藍、綠及紅色之三色組)，可有利地產生依據本發明之一發射白光的照明系統。

此例中，琥珀至紅色、綠色及藍色光係藉由螢光材料產生。

此外，還可再使用一第二紅色螢光材料，以改進此照明系統之色彩還原。

藉由使用涵蓋全部光譜範圍之藍與綠寬頻帶發射器磷光體，連同一發射UV光的LED及一發射琥珀至紅色光的稀土金屬活化氧基次氮基鋁矽酸鹽磷光體，有可能產生具有甚高色彩還原之白光發射。

此情況中，藉由根據混合物與濃度來適當地選擇磷光體，可以改變所產生的白光的色調(CIE色度圖中的色點)。

琥珀至紅色磷光體轉換的發光裝

依據本發明之一較佳方面，提供一發射一頻譜分佈係顯示為琥珀至紅色光的輸出光之照明系統。

依據本發明之包含稀土金屬活化氧基次氮基鋁矽酸鹽作為磷光體的螢光材料特別適合由例如發射UVA的LED或發射藍光的LED等之一主要UVA或藍色輻射源加以激勵，而成為一琥珀或紅色成分。

因此有可能實施發射係在電磁光譜中的琥珀到紅色光區域的照明系統。

在一第一具體實施例中，藉由選擇發光材料，使得由藍色發光二極體所發射之一藍色輻射轉換為琥珀至紅色光，可有利地產生依據本發明之一發射琥珀至紅色光的照明系統。

此例中，該彩色光係藉由依據本發明包含一稀土金屬活化氧基次氮基鋁矽酸鹽磷光體的螢光材料產生。

採用最大發射為400至495 nm之藍色LED可達到尤佳結果。對於氧基次氮基鋁矽酸鹽磷光體的激勵光譜而言，已發現445至465 nm可得最佳結果。

LED磷光體系統的色彩輸出對磷光體層之厚度很敏感。若磷光體層較厚並且包含過多的發射琥珀或紅色光的稀土金屬活化氧基次氮基鋁矽酸鹽磷光體，則穿過該厚磷光體層的藍色LED的光量會較少。於是經組合的LED磷光體系統將顯現琥珀至紅色光，因為結果是由該磷光體之琥珀至紅色的次要光所支配。因此，該磷光體層的厚度是影響系統之顏色輸出的一個關鍵變數。

此情況中，藉由根據混合物與濃度來適當地選擇磷光體，可以改變所產生的琥珀至紅色光的色調(CIE色度圖中的色點)。

依據此一具體實施例之照明系統的色點是落在Commission internationale de I'eclairage(「CIE」)色度圖中琥珀至紅色光譜的範圍。

藉由將過多的$(Ca_{0.95}Sr_{0.05})_{0.98}Al_{1.04}Si_{0.96}N_{2.96}O_{0.04}:Eu_{0.02}$螢光材料與一用於產生發光轉換封裝或轉換層的矽樹脂混

合，可特佳實現一依據本發明之發射紅光的照明系統。由一462 nm之InGaN發光二極體所發射的大部分藍色輻射被該$(Ca_{0.95}Sr_{0.05})_{0.98}Al_{1.04}Si_{0.96}N_{2.96}O_{0.04}:Eu_{0.02}$無機螢光材料偏移入紅色光譜範圍中。個人觀察者將該剩餘之藍色主要光與該磷光體所發射的過多次要光的組合感知為紅光。

若能依據通式$(Ca_{1-x-y-z}Sr_xBa_yMg_z)_{1-n}(Al_{1-a+b}B_a)Si_{1-b}N_{3-b}O_b:RE_n$選擇適當的組合成分，則可藉由此單一磷光體二色概念，實現色點落在連接x=0.58，y=0.42及x=0.69，y=0.31的直線上的琥珀至紅色LED，如圖3所示。

在一第二具體實施例中，藉由選擇螢光材料，使得由藍色發光二極體所發射之一藍色輻射轉換為互補的波長範圍，以形成多色琥珀或紅色光，可有利地產生依據本發明之一發射彩色光的照明系統。在此例中，該彩色光係利用包含稀土金屬活化氧基次氮基鋁矽酸鹽磷光體及一第二磷光體之磷光體混合物的螢光材料產生。

以下表2摘要列出常用的第二磷光體及其光學特性。

組成物	λ_{max}[nm]	色點x、y
$(Ba_{1-x}Sr_x)_2SiO_4$：Eu	523	0.272, 0.640
$SrGa_2S_4$：Eu	535	0.270, 0.686
$SrSi_2N_2O_2$：Eu	541	0.356, 0.606
$Y_3Al_5O_{12}$:Ce	550	0.447, 0.535
SrS：Eu	610	0.627, 0.372
$(Sr_{1-x-y}Ca_xBa_y)_2Si_5N_8$:Eu	615	0.615, 0.384
$(Sr_{1-x-y}Ca_xBa_y)_2Si_{5-x}Al_xN_{8-x}Ox$:Eu	615 - 650	0.633, 0,366*
CaS：Eu	655	0.700, 0.303
$(Sr_{1-x}Ca_x)S$：Eu	610 – 655	*

本發明之另一方面，藉由選擇螢光材料，使得由發射

UV的二極體所發射之一UV輻射全部轉換為琥珀至紅色的單色光，可有利地產生依據本發明之一發射琥珀至紅色光的照明系統。在此情況下，該琥珀至紅色光係由該螢光材料產生。

在一第一具體實施例中，藉由選擇螢光材料，使得由發射UV的二極體所發射之一藍輻射轉換為互補波長的範圍，以形成二色光，特別是琥珀至紅色光，可有利地產生依據本發明之一發射琥珀至紅色光的照明系統。

在此例中，該彩色光係藉由包含一稀土金屬活化氧基次氮基鋁矽酸鹽磷光體的螢光材料產生。

採用最大發射接近UV之370至430 nm的UV-LED，可達到尤佳結果。

包含一UV-LED作為一輻射源之照明系統的色彩輸出對磷光體層的厚度不是非常敏感。因此，磷光體層的厚度並非影響系統顏色輸出的關鍵變數，可加以減薄。

此情況中，藉由根據混合物與濃度來適當地選擇磷光體，可以改變所產生的琥珀至紅色光的色調(CIE色度圖中的色點)。

依據此具體實施例之照明系統的色點是落在Commission internationale de l'eclairage(「CIE」)色度圖中琥珀至紅色光譜的範圍。

【圖式簡單說明】

圖1顯示包含本發明之一磷光體之二色白光LED燈的示意圖，其定位在藉由LED結構所發射之光路徑上。

圖2顯示$(Ca,RE)Al_{1-x+y}B_xSi_{1-y}N_{3-y}O_y$之一部分結晶結構的示意圖。

圖3顯示一C.I.E色度圖，其依據本發明之螢光材料的色點及螢光材料之色點。

圖4顯示$(Ca_{0.95}Sr_{0.05})_{0.98}Al_{1.04}Si_{0.96}N_{2.96}O_{0.04}:Eu_{0.02}$的激勵、發射及反射光譜。

【主要元件符號說明】

1	晶片型發光二極體(LED)
2	反射器杯導線架
3	聚合物
4、5	螢光材料
6	第一端子、第二端子
7	焊線

十、申請專利範圍：

1. 一種照明系統，其包含一輻射源及一螢光材料，該螢光材料包含至少一磷光體，能夠吸收由該輻射源所發射之一部分光且發射波長與被吸收光不同的光；其中該至少一磷光體為一通式為$(Ca_{1-x-y-z}Sr_xBa_yMg_z)_{1-n}(Al_{1-a+b}B_a)Si_{1-b}N_{3-b}O_b:RE_n$的稀土金屬活化氧基次氮基鋁矽酸鹽，其中$0\leq x\leq 1$、$0\leq y\leq 1$、$0\leq z\leq 1$、$0\leq a\leq 1$、$0<b\leq 1$及$0.002\leq n\leq 0.2$，且RE係選自銪(II)及銪(III)。

2. 如請求項1之照明系統，其中該輻射源係一固態發光二極體。

3. 如請求項1之照明系統，其中該輻射源係選自具有峰值發射波長在400至495 nm範圍之發光二極體。

4. 如請求項3之照明系統，其中該螢光材料包含一第二磷光體。

5. 如請求項4之照明系統，其中該第二磷光體為一紅色磷光體，其係選自由$Ca_{1-x-y}Sr_xS:Eu_y$（其中$0\leq x\leq 1$及$0<y\leq 0.2$）及$(Sr_{1-x-y}Ba_xCa_y)_2Si_5N_8:Eu_z$（其中$\leq x\leq 1$及$0\leq y\leq 1$及$0<z\leq 0.2$）所組成的群組。

6. 如請求項4之照明系統，其中該第二磷光體為一黃至綠色磷光體，其係選自由包含$(Ca_xSr_{1-x-y})_2SiO_4:Eu_y$（其中$0\leq x\leq$及$0<y\leq 0.2$）、$(Sr_xBa_{1-x-y})_2SiO_4:Eu_y$（其中$0\leq x\leq 1$及$0<y\leq 0.2$）、$(Sr_{1-x-y}Ba_x)Ga_2S_4:Eu_y$（其中$0\leq x\leq 1$及$0<y\leq 0.2$）、$(Y_{1-x-y-z}Gd_xLu_z)_3(Al_{1-a}Ga_a)_5O_{12}:Ce_y$，（其中$0\leq x\leq 1$及$0<y\leq 0.2$、$0\leq z\leq 1$、$0\leq a\leq 0.5$）、ZnS:Cu、CaS:Ce,Cl及

$SrSi_2N_2O_2$:Eu所組成的群組。

7. 如請求項1之照明系統，其中該輻射源係選自具有峰值發射波長在200至420 nm之UV範圍的發光二極體。

8. 如請求項7之照明系統，其中該螢光材料包含一第二磷光體。

9. 如請求項8之照明系統，其中該第二磷光體為一藍色磷光體，其係選自由 $BaMgAl_{10}O_{17}$：Eu、$Ba_5SiO_4(Cl,Br)_6$：Eu, $CaLa_2S_4$:Ce以及 $(Sr,Ba,Ca)_5(PO_4)_3Cl$：Eu及 $LaSi_3N_5$:Ce所組成的群組。

10. 一種磷光體，其能夠吸收由輻射源所發射之一部分光且發射波長與該被吸收光不同的光；其中該磷光體為一通式為 $(Ca_{1-x-y-z}Sr_xBa_yMg_z)_{1-n}(Al_{1-a+b}B_a)Si_{1-b}N_{3-b}O_b:RE_n$ 的稀土金屬活化氧基次氮基鋁矽酸鹽，其中 $0\leq x\leq 1$、$0\leq y\leq 1$、$0\leq z\leq 1$、$0\leq a\leq 1$、$0<b\leq 1$ 及 $0.002\leq n\leq 0.2$，且RE係選自銪(II)及銪(III)。

11. 如請求項10之磷光體，其中該磷光體額外包含一選自由鐿、鐠及鈐所組成的群組之共活化劑。

12. 如請求項10之磷光體，其中該磷光體具有一選自由元素鋁、鈧、釔、鑭、釓及鎘之氟化物及正磷酸鹽與鋁、釔、矽及鑭之氧化物以及鋁之氮化物所組成的群組之塗層。

十一、圖式：

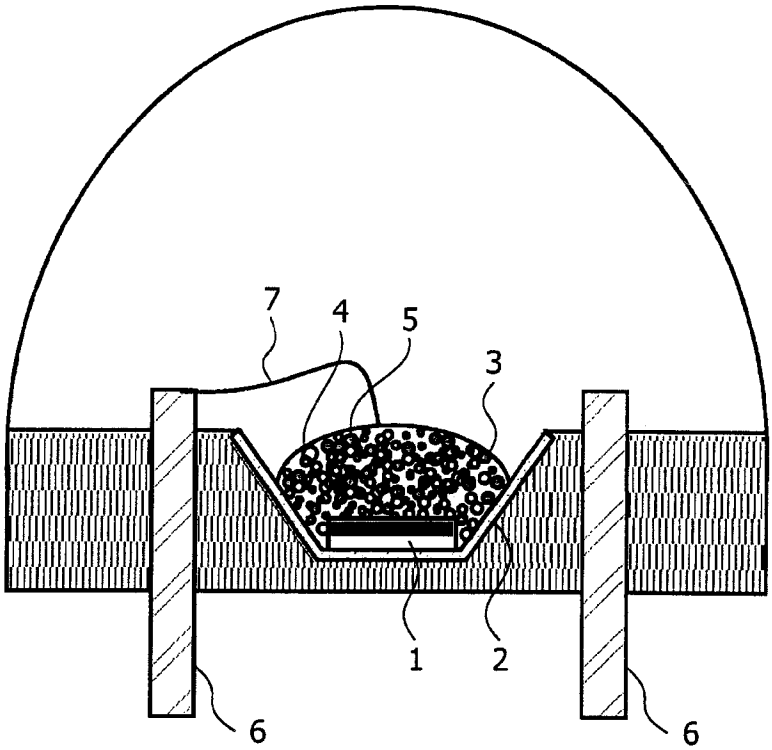


圖 1

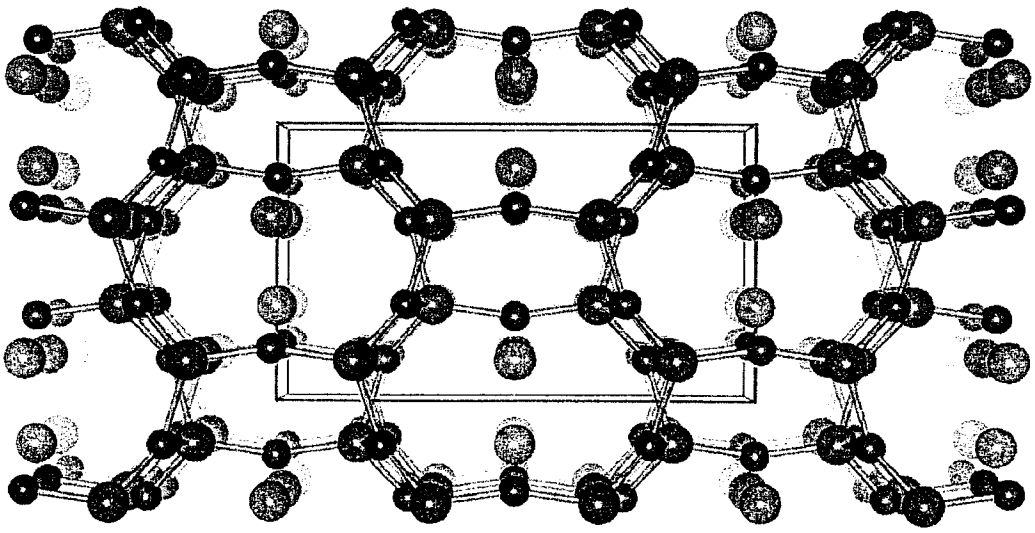


圖 2

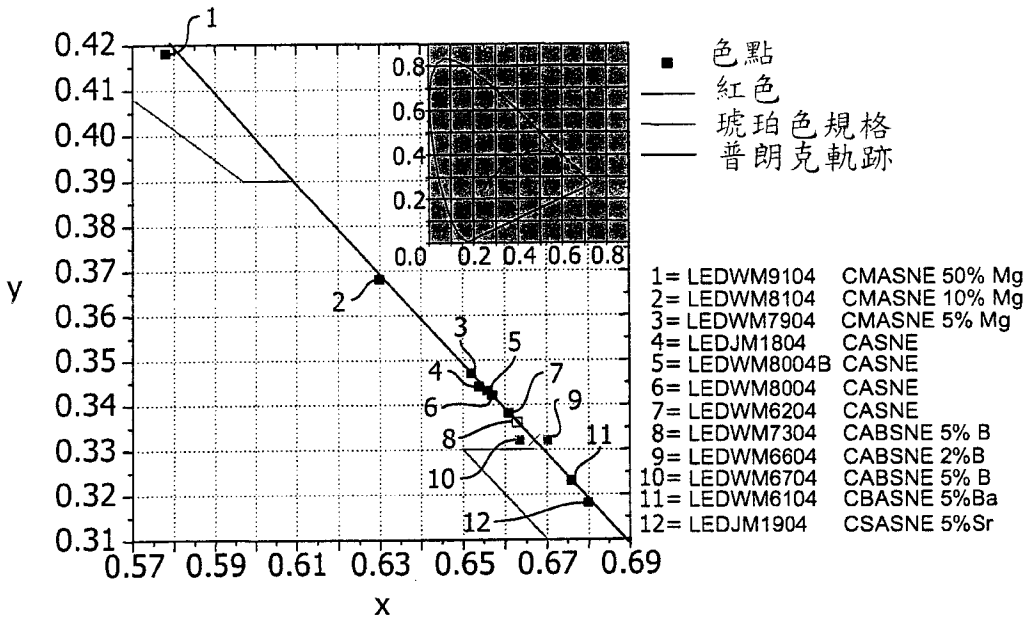

色點
紅色
琥珀色規格
普朗克軌跡
1= LEDWM9104 CMASNE 50% Mg
2= LEDWM8104 CMASNE 10% Mg
3= LEDWM7904 CMASNE 5% Mg
4= LEDJM1804 CASNE
5= LEDWM8004B CASNE
6= LEDWM8004 CASNE
7= LEDWM6204 CASNE
8= LEDWM7304 CABSNE 5% B
9= LEDWM6604 CABSNE 2%B
10= LEDWM6704 CABSNE 5% B
11= LEDWM6104 CBASNE 5%Ba
12= LEDJM1904 CSASNE 5%Sr
y
x

圖 3

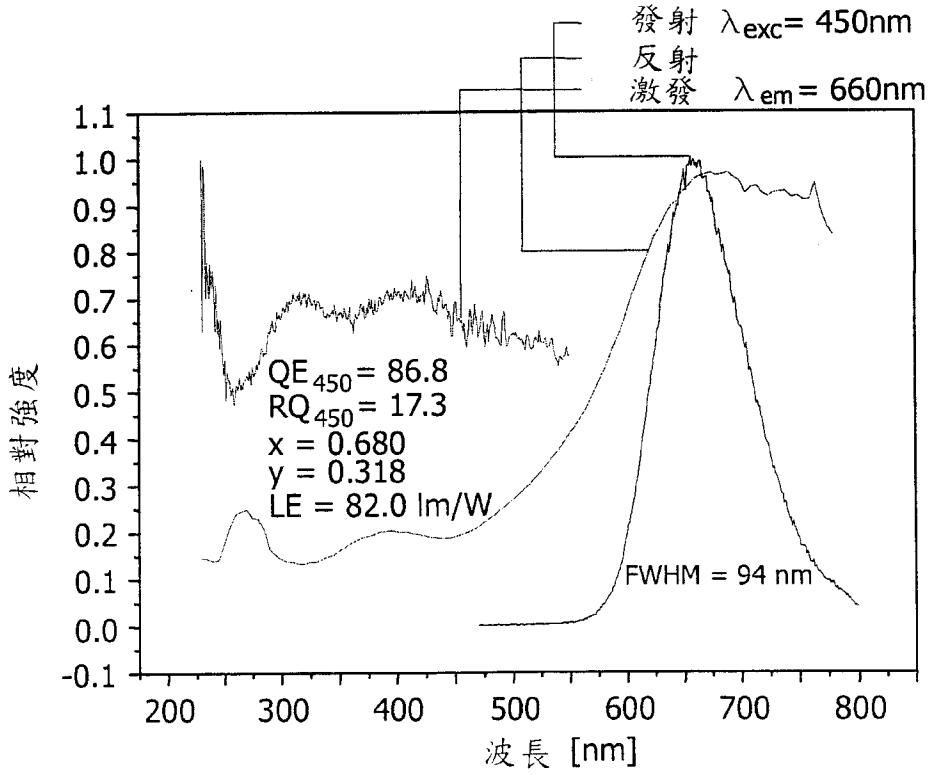

發射 λexc= 450nm
反射
激發 λem= 660nm
QE450= 86.8
RQ450= 17.3
x = 0.680
y = 0.318
LE = 82.0 lm/W
FWHM = 94 nm
相對強度
波長 [nm]

圖 4

公告本

發明專利說明書

（本說明書格式、順序及粗體字，請勿任意更動，※記號部分請勿填寫）

※申請案號：92106393

※申請日期：92.3.19　　※IPC 分類：H01L 33/00

一、發明名稱：（中文/英文）

固體元件裝置及其製造方法

SOLID-STATE COMPONENT DEVICE AND MANUFACTURING METHOD THEREOF

二、申請人：（共 2 人）

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7. 太田 光一/ OTA, KOICHI
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國　籍：(中文/英文)

1.~12. 日本/JP

四、聲明事項：

☐ 主張專利法第二十二條第二項☐第一款或☐第二款規定之事實，其事實發生日期為：　年　月　日。

☑ 申請前已向下列國家（地區）申請專利：

【格式請依：受理國家（地區）、申請日、申請案號　順序註記】

☑ 有主張專利法第二十七條第一項國際優先權：

受理國家（地區）：1.日本 JP　2.日本 JP　3.日本 JP　4.日本 JP
5.日本 JP　6.日本 JP　7.日本 JP

申請日：1. 2003/03/10　2.2003/06/05　3.2003/07/07　4.2003/06/05
5.2004/01/19　6.2003/09/30　7.2003/09/30

申請案號：1.特願 2003-063015　2.特願 2003-160855　3.特願 2003-193182
4.特願 2003-160867　5.特願 2004-010385　6.特願 2003-342705
7.特願 2003-342706

☐ 無主張專利法第二十七條第一項國際優先權：

☐ 主張專利法第二十九條第一項國內優先權：

【格式請依：申請日、申請案號　順序註記】

☐ 主張專利法第三十條生物材料：

☐ 須寄存生物材料者：

國內生物材料　【格式請依：寄存機構、日期、號碼　順序註記】

國外生物材料　【格式請依：寄存國家、機構、日期、號碼　順序註記】

☐ 不須寄存生物材料者：

所屬技術領域中具有通常知識者易於獲得時，不須寄存。

五、中文發明摘要：

一種固體元件裝置，其可於低溫下具體實現玻璃密封加工，並具有高可靠度之密封構造之固體元件裝置。

將 P_2O_5-ZnO 系玻璃以平行於搭載有 GaN 系 LED 元件 2 之含有玻璃成分之 Al_2O_3 基板 3 之方式放置，之後於氮氣中以 60kgf 之壓力、415℃之溫度進行熱壓加工。該條件下之低融點玻璃之黏度為 10^9 泊，低融點玻璃藉由形成於含有玻璃成分之 Al_2O_3 基板 3 上之氧化物被接著。

六、英文發明摘要：

The present invention provides a solid-state component device that can realize a glass sealing process at low temperature and has a sealing structure with high reliability.

A P_2O_5-ZnO-based glass with low melting point is set parallel to a glass-containing Al_2O_3 substrate 3 on which a GaN-based LED component 2 is carried, and then a hot-press process is performed in a N2 atmosphere where the pressure is 60 kgf and the temperature is higher than 415℃. Under this processing condition, the low melting point glass has a viscosity of 10^9 poise and is bonded to the surface of the glass-containing Al_2O_3 substrate 3 by the oxide formed thereon.

七、指定代表圖：

(一)本案指定代表圖為：第（1(a)）圖。

(二)本代表圖之元件符號簡單說明：

1 發光裝置

2 GaN 系 LED 元件

3 含有玻璃成分之 Al_2O_3 基板

3A 通孔

4 電路圖案

5 金凸塊

6 P_2O_5-Na_2-ZnO 系玻璃密封部

6A 頂面

6B 側面

八、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

（無）

九、發明說明：

一、【發明所屬之技術領域】

本申請案之提出以下列日本專利申請案號碼(2003-063015、2003-160855、2003-160867、2003-193182、2003-342705、2003-342706、2004-010385)為依據，此等日本專利申請案之全部內容均導入本申請案中供作參考。

本發明係有關利用玻璃材料將光學元件進行密封之固體元件裝置，特別是關於使用低融點玻璃材料做為玻璃材料之固體元件裝置。

二、【先前技術】

以往有利用環氧樹脂等透光性樹脂材料將發光二極體等固體元件進行密封之固體元件裝置，該固體元件裝置中，透光性樹脂會對強光產生反應，導致變黃等劣化情形。特別是使用會放出短波長光之三族氮化物系列化合物半導體發光元件時，該元件所放出之高能量光與元件本身之發熱會造成元件附近之透光樹脂變黃，導致取光效率有相當程度之降低。

為防止該密封構件之劣化，特開平 8-102553 號公報及特開平 11-177129 號公報特提案以低融點玻璃做為密封構件之發光裝置。

特開平 8-102553 號公報所記載之發光裝置係利用透明之低融點玻璃所形成之密封體 7 將 LED 元件、導線接合部(Wire Bonding)、及引線部上方之周圍進行覆蓋之方式所構成。低融點玻璃使用的是加入硒、鉈、砷、硫磺等，且融點約在攝氏 130~350 度之玻璃。此時，最好是使用融點在攝氏 200 度以下(150 度以下更佳)之低融點玻璃。

藉由特開平 8-102553 號公報之發光裝置，可避免環氧樹脂等所具有問題：亦即由紫外線所引發之不良或脆弱特性，致使密封體在經過一段時間後逐漸變黃之狀況。

另外，藉由特開平 11-177129 號公報之發光裝置中，覆蓋 LED 發光元件之密封體使用的是接近折射率為 2.3 左右之氮化鎵(GaN)

系列發光元件之折射率為 2 左右之低融點玻璃。

藉由特開平 11-177129 號公報之發光裝置，運用接近氮化鉀系列 LED 發光元件之折射率之低融點玻璃進行 LED 發光元件之密封時，於 LED 發光元件表面產生完全反射後折回內部之光量會變少，但從 LED 發光元件放出、然後射入低融點玻璃之光量會增加；其結果是，與本發明有關之晶片型 LED 等之發光效率將較利用環氧樹脂進行 LED 發光元件密封之以往之 LED 在發光效率上較高。

但往常之以低融點玻璃做為密封構件之固體元件裝置有以下問題；雖然是低融點玻璃，但必須進行高溫加工，且由於是硬質材料，若僅是樹脂密封加工之延伸，實際上並不能成功製作樣品。

因此，本發明之目的在提供一固體元件裝置及其製造方法，以抽出、並解決具體實現無機材料加工時之課題，進而以玻璃密封之方式實際達到預期之效果。

三、【發明內容】

為達成上述目的，本發明提供一具備下列特徵之固體元件裝置：(1)以覆晶方式安裝之固體元件、(2)接受固體元件之電力、供給電力至該固體元件之電力接受供給部、(3)對該固體元件進行密封之無機密封構件。

另外，為達成上述目的，本發明亦提供一固體元件裝置，其特徵為具備以下部分：(1)固體元件、(2)接受固體元件之電力、供給電力至該固體元件之電力接受供給部、(3)將該固體元件之電連接部與該電力接受供給部覆蓋之耐熱構件、(4)將包含該耐熱構件之該固體元件進行密封之無機密封構件。

另外，為達成上述目的，本發明亦提供一具備下列特徵之固體元件裝置：(1)固體元件、(2)接受固體元件之電力、供給電力至該固體元件之電力接受供給部、(3)玻璃密封部：密封該固體元件所使用之低融點玻璃係由 SiO_2-Nb_2O_5 系、B_2O_3-F 系、P_2O_5-F 系、P_2O_5-ZnO 系、SiO_2-B_2O_3-La_2O_3 系、SiO_2-B_2O_3 系中選擇。

另外，為達成上述目的，本發明亦提供一固體元件裝置，其

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特徵為具備下列部分：(1)固體元件、(2)接受固體元件之電力、供給電力至該固體元件之金屬製引線部、(3)密封該固體元件之無機密封材料。

另外，為達成上述目的，本發明亦提供一固體元件裝置，其特徵為具備下列部分：(1)固體元件、(2)接受固體元件之電力、供給電力至該固體元件之電力接受供給部、(3)無機密封構件：將該固體元件及該電力接受供給部之一部分進行密封，與該無機材料基板有相同熱膨脹係數之無機密封材料。

另外，為達成上述目的，本發明亦提供一固體元件裝置，其特徵為具備下列部分：(1)將固體元件安裝至電力接受供給部之安裝步驟、(2)密封步驟：利用氧氣斷絕環境及高於無機密封材料之降伏點之溫度，對無機密封材料加壓、進行密封加工。

四、【實施方式】

以下以參照圖示之方式說明與本發明之第 1 實施型態有關之發光裝置進行詳細說明。

圖 1 是與本發明第 1 實施型態有關之發光裝置，(a)是發光裝置之縱剖面圖，(b)是光源之 GaN 系 LED 元件之側面圖。該發光裝置 1 具有以下部分：(1)如圖 1(a)所示之覆晶型 GaN 系 LED 元件 2，(2)搭載有 GaN 系 LED 元件 2 之含有玻璃成分之 Al_2O_3 基板 3，(3)於由鎢(W)、鎳(Ni)、金(Au)構成、於含有玻璃成分之 Al_2O_3 基板 3 上形成之電路圖案 4，(4)將 GaN 系 LED 元件 2 與電路圖案 4 進行電連接之金凸塊(Au stud bump)5，(5)將 GaN 系 LED 元件 2 進行密封，並與含有玻璃成分之 Al_2O_3 基板 3 連接之 P_2O_5-ZnO 系列玻璃密封部 6。

如圖 1(b)所示，GaN 系 LED 元件 2 之形成方式是於藍寶石(Al_2O_3)之基板 20 表面依序形成緩衝(Buffer)層 21、n 型層 22、包含發光層之層 23、p 型層 24，並包含有(1)設置於 p 型層 24 表面之 p 電極 25，(2)將 p 型層 24 至 n 型層 22 之部分範圍以蝕刻之方

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式去除後所外露之n型層22上所形成之n電極26。該GaN系LED元件2係以超過700℃之溫度長成磊晶(Epitaxial)，且耐熱溫度達到600℃以上，於下文會說明之使用低融點玻璃進行密封加工時之溫度下可保持穩定。

另外p電極25具有將包含發光層之層23所發出之光朝基板20之方向反射之下方反射鏡之功能。

含有玻璃成分之Al_2O_3基板3之熱膨脹係數為12.3×10^{-6}/℃，並含有通孔3A；該通孔3A利用由金屬化之W之電路圖案4將基板表面及背面進行導通。

玻璃密封部6由P_2O_5-ZnO系列低融點玻璃(熱膨脹係數：11.4×10^{-6}/℃、降伏點：415℃、折射率：1.59、內部透過率：99%(470nm))所形成，藉由利用模具所進行之熱壓(Hot Press)加工使之與含有玻璃成分之Al_2O_3基板3結合後，再以切割機切割成具有頂面6A及側面6B之矩形。

低融點玻璃是於較一般樹脂中被稱之為高黏度的等級還要再黏很多之條件下加工，而玻璃之降伏點即使超出數十℃，粘度也不致於較一般之樹脂密封之程度還低。又，若想達到一般之樹脂成形時之黏度，則須要較LED元件之結晶成長溫度還高之溫度，且可能附著於模具上，導致密封及成形加工變的較困難。為此，最好是以10^6泊(Poise:黏度單位)以上進行加工。

以下針對此發光裝置1之製造方法進行說明。

首先，準備具有通孔3A之之含有玻璃成分之Al_2O_3基板3，並依據含有玻璃成分之Al_2O_3基板3上之電路圖案進行鎢膠(Paste)網板印刷；其次，將印刷有鎢膠之含有玻璃成分之Al_2O_3基板3以1000多℃進行熱處理，將鎢膠燒印至基板3上，再於W上鍍上鎳(Ni)及金(Au)，形成電路圖案4。其次，利用金凸塊5將GaN系LED元件2與含有玻璃成分之Al_2O_3基板3之電路圖案4(表面側)進行電性的結合。其次，將板狀之P_2O_2-ZnO系列之低融點玻璃與搭載有GaN系LED元件2之含有玻璃成分之Al_2O_3基板3平

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行地放置，之後於氮氣中以 60kgf 之壓力、465℃之溫度進行熱壓加工。該條件下之低融點玻璃之黏度為 10^8~10^9 泊，低融點玻璃與含有玻璃成分之 Al_2O_3 基板 3 間係透過其含有之氧化物接著在一起。其次，將與低融點玻璃一體化之含有玻璃成分之 Al_2O_3 基板 3 放置於切割機中進行切割，將矩形狀之發光裝置分離。

藉由該第 1 實施型態可獲得以下效果。

(1)於高黏度狀態下使用低融點玻璃進行熱壓加工時，可於遠低於結晶成長溫度下進行加工。

(2)透過氧化物將含有玻璃成分之 Al_2O_3 基板 3 與玻璃密封部 6 以化學結合之方式接著時，可獲得更強固之封著強度。因此，即使是接合面積小之小型封裝，亦可達成目的。

(3)密封玻璃與含有玻璃成分之 Al_2O_3 基板 3 之熱膨脹係數相同，因此於高溫進行接著後，之後即使是在常溫或低溫狀態下，亦不容易發生剝離、碎裂等情形。且玻璃不容易因為拉伸應力而碎裂，壓縮應力亦不容易使其碎裂，而密封玻璃使用的是較含有玻璃成分之 Al_2O_3 基板 3 之熱膨脹係數小之材料。經發明者確認之結果，於 −40℃← → 100℃之液相冷熱衝擊測試 1000 循環，亦無發生剝離及碎裂。另外，為確認 5 mm×5 mm 大小之玻璃片與陶瓷基板之接合基礎，將玻璃、陶瓷基板以各種熱膨脹係數之組合進行實驗之結果，熱膨脹係數較低之材料與較高之材料之熱膨脹係數之相對比率在 0.85 以上時，可實現不會碎裂之接合。以上結果與材料之剛性、大小或第 8 實施型態之應力吸收層雖有依存的關係，所謂的熱膨脹係數相同即是上述程度之範圍。

(4)藉由覆晶接合時，由於不需要連線(Wire)，即使於高黏度狀態下進行加工，電極亦不會產生不良。密封加工時之低融點玻璃之黏度在 10^8 至 10^9 泊左右之硬度，與熱硬化處理前之環氧樹脂之 5 泊左右之液體狀態比較，兩者物性相差極大，針對以連線將元件表面之電極與引線等供電材料進行電連接之朝上型 LED 元件進行密封時，於玻璃密封加工時連線會被壓壞、變形，此發明則可防止

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此情況。另外，針對透過金等凸塊將元件表面之電極與引線等供電材料做覆晶接合之覆晶型 LED 元件進行密封時，玻璃之黏度會對 LED 施加一朝向供電材料方向之壓力，此壓力會造成凸塊之崩毀或凸塊間短路等，但藉由本發明則可防止上述不良。

(5)將低融點玻璃與含有玻璃成分之 Al_2O_3 基板 3 平行地放置，於高黏度狀態下進行熱壓加工，低融點玻璃會平行移動至含有玻璃成分之 Al_2O_3 基板 3 之表面、並與之密合，且由於將 GaN 系 LED 元件 2 進行密封，因此不會產生空隙(Void)。

(6)含有玻璃成分之 Al_2O_3 基板 3 之配線用電路圖案 4 於通孔 3A 處被拉出至背面，因此不需針對其進入不需要玻璃之處、或電端子被覆蓋等情況採取特別對策，只需針對板狀之低融點玻璃、多個裝置同時進行密封加工，即可輕易地利用切割機量產多個發光裝置 1。另外，由於低融點玻璃係於高黏度狀態下被加工，因此不需像使用樹脂時般需特別採取對策，即使不依靠通孔，只要外部端子被拉出至背面即可對應大量生產。

(7)將 GaN 系 LED 元件 2 進行覆晶安裝時，不僅可克服於實現玻璃密封時之問題點，亦有可具體實現 0.5 mm×0.5 mm之超小型發光裝置 1 之效果；因為不需要連線之接合(Bonding)空間，且玻璃密封部 6 與含有玻璃成分之 Al_2O_3 基板 3 可選擇具相同熱膨脹係數之材料，利用以化學結合之強固結合方式，即使是微小接觸面積之接著亦不會產生界面剝離之情形。

圖 2 是與第 1 實施型態有關之發光裝置之第 1 變形例，其中(a)是發光裝置之剖面圖，(b)是光源之 GaN 系 LED 元件之側面圖。以下利用同一引用數字針對共通之構成部分進行說明。

該發光裝置 1 與第 1 實施型態不同之處在以下之構成方式：(1)將朝上型 GaN 系 LED 元件 2 以覆晶方式結合在電路圖案 4，(2)設置有保護 GaN 系 LED 元件 2 之電極和金凸塊 5 之白色系填膠 7。

填膠 7 可使用例如氮化硼(BN:Boron Nitride)等光反射性良好之填充材，將 GaN 系 LED 元件 2 接合之前，預先將之灌注至含有

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玻璃成分之 Al_2O_3 基板 3 上，再於其上方以覆晶方式將 GaN 系 LED 元件 2 接合。

如圖 2(b)所示般，GaN 系 LED 元件 2 具有(1)設置於 p 型層 24 表面之 ITO(Indium Tin Oxide)等透光性電極 27，(2)設置於透光性電極 27 表面之 p 電極 25。

藉由該第 1 變形例，即使是朝上型 GaN 系 LED 元件 2，亦可利用封膠 7 將反射擴散光由 GaN 系 LED 元件 2 之基板 20 處放射出來，提高光之取出率。另外，第 2 實施型態中選擇了白色系封膠 7 以提高光之取出效率，但若不重視光取出效率時，亦可使用白色系列以外之顏色之封膠 7。

第 2 變形部分，可於玻璃密封部 6 之表面使用提高耐濕性、耐酸鹼性之表面處理方式，而此時有效之處理方式有 MgF_2、SiO_2、SiN；另外，亦可藉由防止反射之多層膜進行減少介面反射之處理，此時以 TiO_2+SiO_2 多層鍍膜較有效。

圖 3 之第 3 變形例是使用其他封膠之發光裝置之縱剖面圖。第 3 變形例之發光裝置 1 使用熱傳導性良好之鑽石做為保護 GaN 系 LED 元件 2 之電極及金凸塊 5 之封膠 7。另外，亦可使用其他熱傳導性良好之封膠 7：例如 BN、氮化鋁(AlN)、碳化矽(SiC)；以上材料以平均粒徑為數微米之填充物(Filler)之型態混入耐熱性陶瓷鍍膜材料中。

圖 4 之第 4 變形例是設置有由樹脂材料所構成之模具成形部之發光裝置之縱剖面圖。該發光裝置 1 將第 1 實施型態中說明之發光裝置 1 與導線架 8 接合，並設置整體由環氧樹脂所構成之模具成形部。

模具成形部 9 具有一半球狀之光學形狀面 9A，以轉注成型(Transfer Molding)法所形成。

藉由以上構成，不僅可於玻璃密封型裝置上輕易形成光學部分，含有玻璃成分之 Al_2O_3 基板 3 及玻璃密封部 6 更因為被模具成形部 9 包圍，而提高耐濕性。另外，除了環氧樹脂外，模具成形

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部 9 亦可由矽樹脂形成；而除了轉注成型法之外，亦可利用灌入模具成形法等成形方法；之外，亦可利用壓克力、聚碳酸乙酯(Poly Carbonate)等樹脂材料、以注入(Injection)法形成，此時可提高生產性。

另外，模具成形部亦可含有螢光體，螢光體可使用 YAG 螢光粉、珪酸鹽螢光體，或將上述螢光體以特定比例進行混合亦可。

圖 5 是與第 2 實施型態有關之發光裝置之縱剖面圖，該發光裝置與第 1 實施型態之發光裝置不同之處在：(1)設置 SiO_2-Nb_2O_5 系玻璃密封部 6 以取代第 1 實施型態中之玻璃材料之構成，(2)於含有玻璃成分之 Al_2O_3 基板 3 上設置 Ag 系列電路圖案 4 之構成。

SiO_2-Nb_2O_5 系列玻璃密封部 6 是由 SiO_2-Nb_2O_5 系低融點玻璃(熱膨脹係數：12.1×10^{-6}/℃、降伏點：507℃、折射率：1.69、內部透過率：98%(470nm))所形成，藉由熱壓加工使之與含有玻璃成分之 Al_2O_3 基板 3 結合後，再以切割機形成具有頂面 6A 及側面 6B 之矩形。

含有玻璃成分之 Al_2O_3 基板 3 之熱膨脹係數為 12.3×10^{-6}/℃，並具有通孔 3A；該通孔 3A 將基板表面及背面之電解電鍍形成之 Ag 電路圖案 4 進行導通。

藉由該第 2 實施型態，當使用 SiO_2-Nb_2O_5 系列之低融點玻璃時，可降低透濕性、並提高光之取出率；另外，使用透濕性小之低融點玻璃時，有以下好處：

例如將 GaN 系 LED 元件以覆晶方式進行安裝時之電路圖案般，當施加電壓、圖案間隔為數 10 微米時，即使是採取樹脂密封時會有移行(Migration)之問題、應用上有困難之處，亦可使用高反射率材料之 Ag。

圖 6 是與本發明之第 3 實施型態有關之發光裝置之縱剖面圖，該發光裝置 1 具有以下部分：(1)朝上型 GaN 系 LED 元件 2，(2)搭載有 GaN 系 LED 元件 2 之含有玻璃成分之 Al_2O_3 基板 3，(3)由 W 構成之形成於含有玻璃成分之 Al_2O_3 基板 3 上之電路圖案 4，

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(5)將 GaN 系 LED 元件 2 與電路圖案 4 以電連接之金凸塊 5，(6)將 GaN 系 LED 元件 2 與電路圖案 4 以電連接之由 Au 形成之連線 10，(7)將 GaN 系 LED 元件 2、連線 10 及電路圖案 4 等包圍並鍍膜之耐熱無機材鍍膜 11，(8)將 GaN 系 LED 元件 2 與電路圖案 4 接著之無機白色接着劑 12，(9)密封並將含有玻璃成分之 Al_2O_3 基板 3 接著之 P_2O_5-ZnO 系列玻璃密封部 6。

耐熱無機材料鍍膜 11 是一具有透光性、多孔性質之 SiO_2 系列硬化處理鍍膜(Hard Coat)，可防止連線 10 於 P_2O_5-ZnO 系列玻璃於密封加工時產生變形之情形。

無機白色接著劑 12 將由 GaN 系 LED 元件 2 放射至基板側之光進行反射，再由電極形成面使其放射。

以下說明該發光裝置 1 之製造方法。

首先，準備具有通孔 3 之含有玻璃成分之 Al_2O_3 基板 3，並依據含有玻璃成分之 Al_2O_3 基板 3 上之電路圖案將 W(鎢)膠(Paste)進行網板印刷；其次，將印刷有鎢膠之含有玻璃成分之 Al_2O_3 基板 3 以 1500 多℃進行熱處理，將鎢膠燒印至基板 3 上，再於 W 上鍍上鎳(Ni)及金(Au)，形成電路圖案 4。其次，利用無機白色接著劑將 GaN 系 LED 元件 2 與含有玻璃成分之 Al_2O_3 基板 3 上之電路圖案 4(表面側)進行接著。其次，利用連線 10 將 GaN 系 LED 元件 2 之 p 電極、n 電極與電路圖案 4 進行電性接合；其次，以將 GaN 系 LED 元件 2 與連線 10 包圍之方式，將 SiO_2 系鍍膜材料灌注(Potting)。其次，對其施行 150℃之熱處理，形成多孔性質之耐熱無機材料鍍膜 11。其次，將 P_2O_5-ZnO 系列之低融點玻璃與搭載有 GaN 系 LED 元件 2 之含有玻璃成分之 Al_2O_3 基板 3 平行地放置，再以 60kgf 之壓力、415℃之溫度進行熱壓(Hot Press)加工。其次，將與低融點玻璃一體化之含有玻璃成分之 Al_2O_3 基板 3 放置於切割機(Dicer)中進行切割(Dicing)，將矩形狀之發光裝置 1 分離。

藉由該第 3 實施型態，以具有透光性之耐熱無機材鍍膜 11 對連線 10 進行鍍膜時，可針對接合有連線之 GaN 系 LED 元件 2，

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以高良率進行P_2O_5-ZnO系列低融點玻璃進行玻璃密封加工，具體實踐玻璃密封型發光裝置1。

另外，雖然不設置耐熱無機材料鍍膜11，仍可實現玻璃密封加工，但無法避免連線10產生變形之情形，易產生電性短路，使良率降低；另外，除了GaN系LED元件2上之金線10之球狀接合部毀損、容易產生電性短路之外，亦容易發生膜狀之Au覆蓋元件表面，妨礙光之取出等問題。

圖7是與第3實施型態有關之發光裝置之變形例之縱剖面圖，該發光裝置1於使用元件上下具有電極之AlInGaP系列LED元件2之構成部分與第3實施型態有不同。

AlInGaP系列LED元件2中，頂面之電極藉由連線10與電路圖案4電連接，而底面電極則藉由銀膠(Ag Paste)與電路圖案4有電連接。

針對該頂面與底面配置有電極之LED元件，施行耐熱無機材料鍍膜，並利用P_2O_5-ZnO系低融點玻璃進行玻璃密封加工之條件下，可以高良率實踐玻璃密封型發光裝置1。

圖8是與第4實施型態有關之發光裝置之縱剖面圖，該發光裝置1使用的是將第1實施型態所使用之GaN系LED元件2進行分斷(Scribe)加工後所形成之元件。分斷加工所形成之LED元件2於切斷部之側面具有凹凸構造，利用元件鍍膜材14將該側面覆蓋。

元件鍍膜材14可以使用例如SiO_2系列之鍍膜材料，鍍上SiO_2系鍍膜材料以覆蓋GaN系LED元件2之側面，再以150℃之熱處理使之硬化。

藉由該第4實施型態可達到以下效果：分斷(Scribe)加工容易造成GaN系LED元件2上之尖形凹凸處產生碎裂或空隙(void)；但利用元件鍍膜材14將凹凸處覆蓋、使之較平滑後，不僅可防止碎裂，同時還可抑制空隙之發生。

圖9是與第4實施型態有關之發光裝置之第1變形例之縱剖面圖，該發光裝置1中，由SiO_2系列鍍膜材料所構成之元件鍍膜

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材料 14 將 GaN 系 LED 元件 2 之周圍全體包覆之構成是其與第 4 實施型態不同之處。

元件鍍膜材料 14 之熱膨脹係數介於 GaN 系 LED 元件 2 之熱膨脹係數與 P_2O_5-ZnO 系列低熔點玻璃之熱膨脹係數中間，因此即使使用熱膨脹係數大之玻璃或大尺寸 LED 元件時，可防止碎裂之情形。

藉由該第 1 變形例，不僅可抑制 GaN 系 LED 元件 2 表面形狀所導致之碎裂或空隙，亦可防止 GaN 系 LED 元件 2 與低熔點玻璃之熱膨脹係數差所導致之碎裂之發生。另外，從 GaN 系 LED 元件 2 中之取光性之觀點來看，元件鍍膜材料 14 愈薄愈好。

圖 10 是與第 4 實施型態有關之發光裝置之第 2 變形例之縱剖面圖，該發光裝置 1 中，以含有螢光體之螢光體層 15 將 GaN 系 LED 元件 2 之周圍全體包覆之構成是其與第 4 實施型態不同之處。

螢光體層 15 之構成是：於第 1 變形例中所使用之由 SiO_2 系鍍膜材料所構成之元件鍍膜材料 14 加上做為螢光體之 YAG 螢光體；此時螢光體可以是一種類或是多種類螢光體之混合。另外，亦可使用珪酸鹽螢光體，甚至可於螢光體層中混合 YAG 型螢光體與珪酸鹽螢光體。

藉由該第 2 變形例，除了有第 1 變形例之良好效果外，由於玻璃密封將外部濕氣阻擋於螢光體外，因此可防止螢光體之劣化，可長期獲得安定之波長變換性。

圖 11 是與第 5 實施型態有關之發光裝置，其中(a)是發光裝置之俯視圖，(b)是發光裝置之側面圖，(c)是發光裝置之底視圖。該發光裝置 1 具備以下部分：(1)覆晶型之多個 GaN 系 LED 元件 2，(2)正方形狀之搭載有 GaN 系 LED 元件 2 之多層構造之含有玻璃成分之 Al_2O_3 基板 3，(3)於含有玻璃成分之 Al_2O_3 基板 3 之表面及層內由鎢(W)所形成之電路圖案 4(基板表面之圖案更鍍有鎳、金)，(4)將 GaN 系 LED 元件 2 與電路圖案 4 進行電連接之金凸塊 5，(5)將 GaN 系 LED 元件 2 進行密封，並與含有玻璃成分之 Al_2O_3

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基板 3 連接之 P_2O_5-ZnO 系列玻璃密封部 6，(6)於含有玻璃成分之 Al_2O_3 基板 3 之四角中，從內層之中間層中露出之底面電路圖案 16A(陽極)、16C(陰極)，(7)將 GaN 系元件 2 之發熱向外部發散之由銅箔構成之放熱圖案 17；透過金凸塊 5 將 3 乘 3 之共 9 個 GaN 系 LED 元件 2 配置在於基板表面所形成圓形狀之電路圖案 4 上。

含有玻璃成分之 Al_2O_3 基板 3 具有由鎢所構成之內層配線之多層構造，並將圖 11(b)所示之列方向之 3 個 GaN 系 LED 元件 2 串聯、形成元件群，將元件群之陽極與底面電路圖案 16A 之一連接，並將元件群之陰極與底面電路圖案 16C 連接。另外，陰極亦與另外 2 列上所形成之元件群之陰極連接。

藉由該第 5 實施型態，即使是使用多個 GaN 系 LED 元件 2 之情形，在使用陶瓷多層基板之情況下，可輕易形成串並聯電路，並能輕易完成電解電鍍時之配線理線。另外，將外部電連接端子由中間層中取出、於底面設置放熱用金屬圖案時，可迅速將被緊密安裝上去之 9 個 GaN 系 LED 元件 2 在發光時產生之熱，由放熱用金屬圖案傳導致散熱槽(HEAT SINK)。

圖 12 是與第 5 實施型態有關之發光裝置之第 1 變形例之縱剖面圖，該發光裝置 1 於 P_2O_5-ZnO 系玻璃密封部 6 之表面設置螢光體層 15 做為波長變換型發光裝置，此點是與第 5 實施型態不同之處。

藉由該第 1 變形例，由於 P_2O_5-ZnO 系玻璃密封部 6 具備將 GaN 系 LED 元件 2 之全體包圍之螢光體層 15，因此可實現具高光輸出之白色發光裝置 1。另外，多元件型發光裝置 1 中，各元件之特性即使有不同，但差異不顯著，因此可實現有均一發光特性之發光裝置 1。

圖 13 是與第 5 實施型態有關之發光裝置之第 2 變形例之縱剖面圖，該發光裝置 1 與第 5 變形例不同之處是：發出藍光或綠光之覆晶型 GaN 系 LED 元件 2 與發出紅光之上下電極型 AlInGaP 系 LED 元件 2 二元件混合存在，並以 P_2O_5-ZnO 系玻璃密封部 6

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進行密封。AlInGaP 系 LED 元件 2 連同連線 10 一起被耐熱無機材料鍍膜 11 所包圍。

藉由該第 2 變形例，即使覆晶型與上下電極型 LED 元件混合存在，亦可利用 P_2O_5-ZnO 系低融點玻璃進行密封加工，並可任意設定 LED 元件 2 之發光顏色之組合。

圖 14 是與第 6 實施型態有關之發光裝置之剖面圖，該發光裝置 1 具有以下部分：(1)於元件上下方具有電極之 AlInGaP 系 LED 元件 2，(2)搭載有 AlInGaP 系 LED 元件 2 之含有玻璃成分之 Al_2O_3 基板 3，(3)由鎢構成、形成於含有玻璃成分之 Al_2O_3 基板 3 上之電路圖案 4，(4)與 AlInGaP 系 LED 元件 2 之電極及電路圖案 4 有電連接之由金所形成之連線 10，(5)包圍 AlInGaP 系 LED 元件 2、連線 10、電路圖案 4 並鍍膜之由 TiO_2(折射率 2.4)構成之高折射率材料鍍膜 11A，(6)將 AlInGaP 系 LED 元件 2 與電路圖案 4 接著並進行電連接之銀膠 13，(7)將被高折射率材料鍍膜 11A 包圍之 AlInGaP 系 LED 元件 2 密封、並與含有玻璃成分之 Al_2O_3 基板 3 接著之 SiO_2-Nb_2O_5 系玻璃密封部 6。

SiO_2-Nb_2O_5 系玻璃密封部 6 由 SiO_2-Nb_2O_5 系低融點玻璃(熱膨脹係數：10.2×10^{-6}/℃、降伏點：543℃、折射率：1.92、內部透過率：81%(470nm)或 91%(厚度 10 mm處))所形成，其具有半球面狀之光學形狀面 6D；其將由 AlInGap 系 LED 元件 2 所發出之光透過高折射率材料鍍膜 11A，略垂直地射入玻璃界面，將界面反射極力縮小後向外放射。另外，當由 AlInGaP 系 LED 元件 2 發出之光以其與玻璃密封部 6 之界面間小於臨界角之角度射入時，光學形狀面 6D 亦可以是半球狀以外之形狀，具體來說，可以是六面體或八面體。

藉由該第 6 實施型態，由於 AlInGaP 系 LED 元件 2 被折射率 2.4 之 TiO_2 之高折射率材料鍍膜 11A 所包圍，並以折射率為 1.92 之 SiO_2-Nb_2O_5 系玻璃密封部 6 進行密封，因此可抑制高折射率材料 11A 與 SiO_2-Nb_2O_5 系玻璃密封部 6 之界面處之界面反射損失，

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提高高折射率媒體之 LED 元件之光取出效率。

另外，由於 SiO_2-Nb_2O_5 系玻璃密封部 6 係被形成為凸面狀，並從 AlInGaP 系 LED 元件 2 以垂直入射角度射入玻璃密封部 6 與空氣之界面，而可以獲得較高之外部放射效率。

圖 15 是與第 6 實施型態有關之發光裝置之第 1 變形例，其中(a)是發光裝置之縱剖面圖，(b)是光源之 GaN 系 LED 元件之側面圖；該發光裝置 1 之構成是以具有 SiC 基板 29 之 GaN 系 LED 元件 2 取代 AlInGaP 系 LED 元件 2，且 SiO_2-Nb_2O_5 系玻璃密封部 6 之表面具有光學形狀面 6D，該光學形狀面 6D 配置有 1/4 波長厚度之 SiO_2 膜 6E，以上是其與第 6 實施型態不同之處。

SiC 基板 29 於底面具有 n 電極 26，透過銀膠 13 與電路圖案 4 有電連接。

藉由該第 1 變形例，由於光學形狀面 6D 配置有 1/4 波長厚度之 SiO_2 膜 6E，SiO_2 膜會干涉被導引至光學形狀面 6D 之光，因此可降低反射。

圖 16 是與第 6 實施型態有關之發光裝置之第 2 變形例，其中(a)是發光裝置之縱剖面圖，(b)是光源之 GaN 系 LED 元件之側面圖。該發光裝置 1 與第 6 實施型態不同之處在，使用具有 GaN 基板 30 之覆晶型 GaN 系 LED 元件 2 取代 AlInGaP 系 LED 元件 2。

藉由該第 2 變形例，由於是使用具有 GaN 基板 30 之 GaN 系 LED 元件 2，LED 元件內部不會產生界面反射，因此可將光很有效率地導引至基板表面；而被導引至基板表面之光透過 SiO_2-Nb_2O_5 系玻璃密封部 6，從光學球狀面 6D 放射至外部，因此可獲得較高之外部放射效率。

圖 17 是與第 7 實施型態有關之發光裝置，其中(a)是發光裝置之縱剖面圖，(b)是光源之 GaN 系 LED 元件之側面圖。該發光裝置 1 利用 Al_2O_3 取代含有玻璃成分之 Al_2O_3 做為基板，並使用與 Al_2O_3 相當之熱膨脹係數之密封玻璃材料，以上是與至第 6 為止之實施型態不同之處。圖 17 中同時顯示被切斷為一個個裝置前之狀

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態，如圖 17(a)所示，各個發光裝置 1 具有以下部分：(1)覆晶型 GaN 系 LED 元件 2，(2)搭載有 GaN 系 LED 元件 2 之 Al_2O_3 基板 3，(3)形成於 Al_2O_3 基板 3 上之電路圖案 4，(5)將 GaN 系 LED 元件 2 與電路圖案 4 進行電連接之金凸塊 5，(6)將 Gan 系 LED 元件 2 進行密封、並與含有玻璃成分之 Al_2O_3 基板 3 連接之 B_2O_3-F 系列玻璃密封部 6。

如(b)所示，為防止 GaN 系 B_2O_3-F 系列玻璃之密封加工時發生之金凸塊 5 之損傷或電路間短路，GaN 系 LED 元件 2 會於其與 Al_2O_3 基板 3 間加入填膠(填膠 I)7。

Al_2O_3 基板 3 具有通孔 3，並透過此通孔 3 與表面及背面之電路圖案 4 間有電連接，且以一定之間隔形成基板切斷位置之溝槽 3B。

電路圖案 4 於搭載有 GaN 系 LED 元件 2 之表面具有提高其與 B_2O_3-F 系列玻璃密封部 6 之接著強度用之接著用圖案 4A、4B，接著用圖案 4B 亦是被取出至 Al_2O_3 基板 3 背面之電路圖案 4 之一部分。

B_2O_3-F 系玻璃密封部 6 由 B_2O_3-F 系低融點玻璃(熱膨脹係數：6.9×10^{-5}/℃、降伏點：539℃、折射率：1.75、內部透過率：98%(470nm))所形成，並針對預成形玻璃(Preform glass)進行熱壓加工(該預成形玻璃設置有以預先加工方式、預先設置有光學形狀面 6D 及薄肉部 6B)，使其與 Al_2O_3 基板 3 之表面接著。較薄處 6B 之厚度是以針對分斷(Scribe)加工處施加重力進行切割時，鄰接之發光裝置 1 不會產生碎裂等損壞之厚度為標準所形成。

發光裝置 1 在安裝上 GaN 系 LED 元件 2，並以 B_2O_3-F 系玻璃密封部進行密封後，將 Al_2O_3 基板 3 之溝槽 3B 做為分割位置、並施加重量後，Al_2O_3 基板 3 因為應力集中而斷開，同時，較薄處 6B 之 B_2O_3-F 系玻璃密封部 6 會被切斷。

藉由該第 7 實施型態，使用一般常用之 Al_2O_3 基板 3 時，白色光吸收較、可提高光之取出效率；不僅容易取得，同時亦很廉

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價。另外，由於是針對分斷加工部分施加重力、切割成各個發光裝置1，因此量產性很好。以切割方式形成各個發光裝置1時，以切割機切割後會於玻璃殘留歪斜應力，熱衝擊(HEAT SHOCK)時B_2O_3-F系玻璃密封部會有裂痕之情形；但是以分斷方式進行切割之發光裝置1之殘留歪斜應力較小，較不易發生裂痕等不良。

另外，B_2O_3-F系以外之低融點玻璃亦可使用SiO_2-B_2O_3-La_2O_3系低融點玻璃(熱膨脹係數：8.3×10^{-6}/℃、降伏點：559℃、折射率：1.81、內部透過率：99%(470nm))。

另外，分斷以外之其他分割方法中，亦可使用雷射光進行分割。

圖18是與第7實施型態有關之發光裝置之第1變形例之縱剖面圖，該發光裝置1與第7實施型態不同之處在：藉由B_2O_3-F系低融點玻璃形成B_2O_3-F系玻璃密封部6。

B_2O_3-F系SiO_2-B_2O_3玻璃密封部6與於Al_2O_3基板3上形成之溝槽3B之相對位置處具有畫線部6C，當施加重力時，畫線部6C與溝槽3B產生連動、應力集中，將B_2O_3-F系玻璃密封部6及Al_2O_3基板3分割。

藉由該第1變形例，由於不需要將B_2O_3-F系玻璃密封部6預成型，因此可簡化製程，利於生產。

另外，亦可使用SiO_2-B_2O_3-F系低融點玻璃做為玻璃密封部6之低融點玻璃。

圖19是與第8實施型態有關之發光裝置，其中(a)是發光裝置之縱剖面圖，(b)是光源之GaN系LED元件之側面圖；此實施型態與第7實施型態不同之處在該發光裝置1具有以下部分：(1)GaN系LED元件2下方具有熱傳導性佳之BN之填膠7，(2)搭載有GaN系LED元件2之AlN基板3，(3)將GaN系LED元件2密封，並與AlN基板3接著之與AlN有相同熱膨脹係數之SiO_2-B_2O_3-F系玻璃密封部6。

SiO_2-B_2O_3-F系玻璃密封部6係由SiO_2-B_2O_3系低融點玻璃(熱

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膨脹係數：4.9×10^{-6}/℃、降伏點：558℃、折射率：1.61、內部透過率：96%(380nm))所形成，其熱膨脹係數與 GaN 系 LED 元件 2 之熱膨脹係數：5×10^{-6}/℃相當。

藉由該第 8 實施型態，GaN 系 LED 元件 2 發光所產生之熱會透過熱傳導性佳之填膠 7 及金凸塊 5 傳導致高放熱材料之 AlN 基板 3，並有效率地被釋放至外部。另外，由於 GaN 系 LED 元件 2、AlN 基板 3、SiO_2-B_2O_3-F 系玻璃密封部 6 之主要材料之熱膨脹係數幾乎相等，因此不會發生熱膨脹係數不同所導致之剝離或密封性降低等情形。

例如，即使主要材料間之熱膨脹係數有不同，藉由設置有緩和應力效果之構成，可以吸收內部應力，防止密封性之降低或剝離等情形。

圖 20 是與第 8 實施型態有關之發光裝置之變形例之縱剖面圖，該發光裝置 1 與第 7 實施型態不同之處在：於安裝有 GaN 系 LED 元件 2 之電路圖案 4 之表面配置有以吸收內部應力為目的之軟金屬層。

圖 21 之(a)至(e)是於 AlN 基板上形成電路圖案之形成步驟，首先，如圖(a)所示，預先於形成有通孔 3A 之 AlN 基板 3 之兩面，根據電路圖案網板印刷上含有鎢之膠；其次，以超過 1500℃之溫度燒烤 AlN 基板 3，將鎢(W)燒印上去。藉此，鎢與 AlN 基板 3 會強固地結合，而該鎢亦可以使用濺鍍(SPUTTERING)的方式形成。另外，亦可使用 Mo 等高融點金屬取代鎢。其次，如(b)所示，AlN 基板 3 表面之電路圖案 4 上以電鍍法配置了鎳(Ni)層。其次，如(c)所示，以 700℃將 AlN 基板 3 加熱，使鎳與鎢產生反應；藉此使電路圖案 4 強固地接合在 AlN 基板 3 上。其次，如(d)所示，以電解電鍍法將金(Au)層 4C 形成於電路圖案 4 之表面。其次，如(e)所示，利用金凸塊 5 將 GaN 系 LED 元件 2 裝載(Mount)至規定之位置。

如此，針對於電路圖案 4 上安裝有 GaN 系 LED 元件 2 之 AlN

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基板 3，將 SiO_2-B_2O_3 系低融點玻璃進行熱壓加工，再將之分割為各個發光裝置 1。

藉由該變形例，可將強固之電路圖案 4 與 AlN 基板 3 進行接合，且藉由設置(1)金圖案(Ag Pattern)4C：透過金凸塊將 GaN 系 LED 元件 2 裝載於電路圖案 4 上，(2)鎳圖案 4A：與低融點玻璃接合為目的之兩者，可實現導電凸塊裝載，又可緩和應力。另外，玻璃是透過氧化物進行接合，其與金之間雖不能接著，但與鎳之間則透過鎳表面之鎳氧化膜進行接合。另外，亦與玻璃及 AlN 之間有良好接合。AlN 基板具高度熱傳導度，使 GaN 系 LED 元件 2 點燈後容易與玻璃間產生溫度差，但即使是此種情況下，金層 4C 之彈性變形會緩和應力，而可獲得安定之玻璃密封性。

圖 22 是與第 9 實施形態有關之發光裝置之縱剖面圖，該發光裝置 1 具有以下部分：(1)覆晶型 GaN 系 LED 元件 2，(2)搭載有 GaN 系 LED 元件 2 之 AlN 次裝載基台 18，(3)由鎢構成、形成於 AlN 次裝載基台之電路圖案 4，(4)具有搭載 AlN 次裝載基台之梯級部 19A 之由銅合金構成之引線 19，(5)將 GaN 系 LED 元件 2 與電路圖案 4 進行電連接之金凸塊 5，(6)將 GaN 系 LED 元件 2 及引線 19 包圍、將整體密封之 P_2O_5-F 系玻璃密封部 6。

AlN 次裝載基台 18 具有金屬化之電路圖案。

P_2O_5-F 系玻璃密封部 6 由 P_2O_5-F 系低融點玻璃(熱膨脹係數：16.9×10^{-6}/℃、降伏點：363℃、折射率：1.54、內部透過率：99%(470nm))所形成，並利用熱壓加工形成光學形狀面 6D，該光學形狀面 6D 為半球面狀，並將光放射至所希望之放射範圍。

熱壓加工之方式為：將 2 片 P_2O_5-F 系低融點玻璃以夾住形成於導線架之引線 19 之方式平行放置，於氮氣中以 10kgf 之壓力、140℃以上之條件進行，該條件時之低融點玻璃之黏度為 10^8 至 10^9 泊。

圖 23 是針對導線架以熱壓加工進行密封時之狀態，該圖亦同時顯示一對引線 311 往一方向被拉出之由板狀銅合金所構成之導

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線架 31 之狀態。該導線架 31 具有以下部分：(1)固定 AlN 次裝載基台 18 之引線 311，(2)設置於該引線 311 之支持側之開口 312，(3)吸收導線架之熱變形之小孔 313，(4)將導線架 31 之傳送位置進行定位之定位孔 314；引線 311 周圍於將板狀之銅合金打洞時，被當做開口 310 除去。

以下針對發光裝置 1 之製造方法進行說明。

首先，形成具有引線 19 之導線架 31，該導線架 31 上形成有搭載 AlN 次搭載基台 18 之梯級部 19A；其次，將導線架 31 與形成有電路圖案 4 之 AlN 次裝載基台 18 結合。其次，透過金凸塊 5 將設置於 AlN 次裝載基台 18 表面之電路圖案 4 與 GaN 系 LED 元件 2 進行覆晶接合。其次，將 P_2O_5-F 系低融點玻璃平行放置於導線架 31 之上下方。其次，使用圖示未顯示出來之模具，針對 P_2O_5-F 系低融點玻璃進行熱壓加工。以 P_2O_5-F 系低融點玻璃分別形成(1)以熱壓加工形成之較薄處 6B，(2)P_2O_5-F 系玻璃密封部 6。其次，切割引線 311，使其從導線架 31 分離，成為一個個發光裝置。

藉由該第 9 實施型態可獲得以下效果。

(1)由於是使用 P_2O_5-F 系低融點玻璃，於高黏度狀態進行熱壓加工，因此可以低於結晶成長溫度之條件進行玻璃密封加工。

(2)由於是於氮氣中進行熱壓加工，因此各材料不容易氧化。

(3)由於是以夾住引線之方式放置 2 片玻璃，因此可以在高黏度狀態進行封著。

(4)P_2O_5-F 系低融點玻璃與銅合金引線具有相同之熱膨脹係數，因此不易發生剝離、碎裂等接合不良。另外，即使熱膨脹係數有不同，內部應力會被軟金屬之銅之塑性所吸收。第 1 至第 8 實施型態中是使用形成有電路圖案之陶瓷基板做為電力供給之手段，但一般可取得之陶瓷基板之熱膨脹係數較低融點玻璃還低。雖然不一定有直接關聯，分子間結合較弱之材料有低融點且熱膨脹係數較大之特性。相對於此，使用金屬引線做為供電手段時，即使是熱膨脹係數大於 15×10^{-6}/℃ 以上之更低融點之玻璃亦可具體實現

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發光裝置1。另外，選擇熱膨脹係數較大之低融點玻璃時，由於其與GaN系LED元件間之熱膨脹係數差變大之故，最好同時採取對應該差異之對策。

(5)由於採取覆晶安裝，因此電極部分不易受損。

(6)具有一不易因材料間熱膨脹係數不同而產生碎裂之構造。亦即，於引線上形成對應AlN次裝載基台形狀之段差，AlN次裝載基台之長度方向之應力之緩和可藉由軟金屬之引線之塑性而達成。另外，拉伸應力容易使玻璃產生碎裂，但壓縮應力則不易產生碎裂。熱膨脹係數小之GaN系LED元件包圍的是中央部份，相對於此，高膨脹係數之引線、P_2O_5-F系低融點玻璃則是包圍周圍之構成，因此應力會針對GaN系LED元件之各面於垂直方向產生作用導致玻璃產生壓縮應力。藉此，相對於LED元件或次裝載基台，即使低融點玻璃之熱膨脹係數較大，亦可具體實踐。

(7)GaN系LED元件所發出之熱會透過AlN次裝載基台及引線迅速被釋放至外部，且玻璃之熱傳導係數優於樹脂密封構件達10倍左右，由玻璃釋放出之熱為不可忽視之程度。

(8)另外，針對導線架進行熱壓加工，之後除了針對引線個別進行玻璃密封之外，亦對導線架進行切割作業(Tie Bar Cut)，因此可一次進行多量生產，量產性佳。

(9)另外，構成次裝載基台之材料不限定是AlN，亦可使用藍寶石(Al_2O_3)。使用Al_2O_3時，由於其與玻璃材料之熱膨脹係數差較小之故，因此可控制碎裂、剝離之發生。

另外，如圖24所示，亦可利用n層18B及p層18C將GaN系LED元件2搭載至做為齊納二極體(Zener Diode)之矽次裝載基台18，此時可保護GaN系LED元件不受到靜電之破壞。另外，由於可利用上文所說明之耐熱無機材鍍膜11等保護材料，針對將矽次裝載基台18之p層18C與引線19進行電連接之連線進行保護，因此可避免伴隨玻璃密封加工而發生之損傷。

另外，夾住引線之2片玻璃方面，下方之玻璃亦可使用白色

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之玻璃。此時，其會反射被放射至下方之光，可將之放射至光學形狀形成側。

另外，夾住引線之2片玻璃可具有不同之黏度，具體來說，上方玻璃使用 P_2O_5-F 系低融點(熱膨脹係數：17.3×10^{-6}/℃、降伏點：310℃、折射率：1.51、內部透過率：99%(470nm))，下方使用 P_2O_5-F 系低融點玻璃(熱膨脹係數：16.9×10^{-6}/℃、降伏點：363℃、折射率：1.54、內部透過率：99%(470nm))；此時，熱壓加工時，上方為高黏度、下方則為低黏度，因此較易成形。

圖25是與第10實施型態有關之發光裝置，其中(a)是俯視圖，(b)是(a)中 A-A 部分之剖面圖，(c)是下方玻璃之立體圖。該發光裝置具有以下部分：(1)朝上型 GaN 系 LED 元件2，(2)具備搭載有 GaN 系 LED 元件2之引線罩杯部 19B 之引線19，(3)將 GaN 系 LED 元件與引線19進行電連接之連線10，(4)包覆 GaN 系 LED 元件2及連線10、進行保護之矽鍍膜35，(5)藉由經過預成形之上方玻璃60A及下方玻璃60B，將引線19進行整體密封之 P_2O_5-F 系玻璃密封部6。

引線罩杯部19因為傾斜面190及底面191而形成擂鉢狀，並被收納至(c)所示之下方玻璃60B之引線收納溝槽60C處，而引線收納溝槽60C是於利用模具製作下方玻璃60之預型體(Preform)時所形成。

以下說明發光裝置1之製造方法。

首先，準備圖示未顯示之導線架，該導線架配置有以銅為材料、表面經過鍍銀處理之一對引線19；其次，將 GaN 系 LED 元件2搭載於引線19之引線罩杯部19B上。GaN 系 LED 元件2藉由無機透明接著劑與引線罩杯部19B之底部191接著。其次，利用連線10將一對引線19與 GaN 系 LED 元件2之電極間進行電連接；然後於一對引線19與 GaN 系 LED 元件2之電極間有電連接之狀態下，將之收納於預成型之下方玻璃60B之引線收納溝槽60C中。其次，以覆蓋一對引線19與 GaN 系 LED 元件2之方式，將

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矽樹脂鍍膜灌入。其次，準備上方玻璃 60A，利用熱壓加工使之與下方玻璃 60B 成為一體，之後將發光裝置 1 從導線架上切割開。

藉由該第 10 實施形態，可獲得以下效果。

矽樹脂在 400℃以上之溫度下，分子結合因熱而被破壞、並產生氣體，但由於可在不會使矽樹脂鍍膜 35 產生熱分解之 360℃下進行加工之故，矽樹脂會吸收玻璃密封加工時之熱、緩和應力。另外，使用收納引線罩杯 19B 之預成型之下方玻璃 60B 時，一對引線 19 之密封狀態會較安定。另外，針對導線架進行熱壓加工，於各別針對引線進行玻璃密封之同時，亦進行從導線架上將發光裝置切割(TIBAR CUT)之作業，可同時進行大量之生產，量產性佳。

圖 26 是與第 10 實施形態有關之發光裝置之第 1 變形例之剖面圖，該發光裝置 1 具有(1)覆晶型 GaN 系 LED 元件 2(0.3mm×0.3mm)，(2)搭載有 GaN 系 LED 元件 2 之 AlN 次裝載基台 18，(3)具有收納 AlN 次裝載基台 18 之梯級部 19A 之一對導線架 19，以上是與第 10 實施形態不同之處。

一對導線架 19 於梯級部 19A 上方具有傾斜面 19D，由 GaN 系 LED 元件 2 放射出之光經由傾斜面 19D 反射、放射至外部。

AlN 次裝載基台 18 具有將設置於表面及背面之電路圖案 4 進行電連接之通孔 18A。

以下說明發光裝置 1 之製造方法。

首先，準備圖示未顯示之設置有一對引線 19 之導線架，其次，將 AlN 次裝載基台 18 放置於引線 19 之梯級部 19A，並利用銀膠將之進行電連接。其次，透過金凸塊 5 將 GaN 系 LED 元件 2 與 AlN 次裝載基台 18 接合。其次，於一對引線 19 與 GaN 系 LED 元件 2 之電極間有電連接之狀態下，將之收納於預成型之下方玻璃 60B 之引線收納溝槽 60C 中。其次，以覆蓋一對引線 19 與 GaN 系 LED 元件 2 之方式，灌入矽樹脂鍍膜。其次，準備上方玻璃 60A，利用熱壓加工使之與下方玻璃 60B 成為一體，之後將發光裝置 1

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從導線架上切割開。

藉由該第 1 變形例，使用覆晶型 GaN 系 LED 元件 2 時，可由基板中有效率地取出光。

圖 27 是與第 10 實施型態有關之發光裝置之第 2 變形例之剖面圖，該發光裝置 1 具有(1)覆晶型 GaN 系 LED 元件(大尺寸)2，(2)搭載有 GaN 系 LED 元件 2 之 AlN 次裝載基台 18，(3)具有收納 AlN 次裝載機台 18 之梯級部 19A 之導線架 19，以上是與第 10 實施型態不同之處。而大尺寸之 GaN 系 LED 元件 2 之大小是 1 mm× 1 mm。

第 2 變形例之說明是以使用大尺寸晶粒(Chip)做說明，而晶粒變大時，P_2O_5-F 系玻璃 AlN 次裝載基台 18 及 P_2O_5-F 系玻璃密封部 6 之熱膨脹係數差會變大；但即使是上述情形，亦可獲得良好密封性。

圖 28 是與第 11 實施型態有關之發光裝置，其中(a)是側面圖，(b)是玻璃密封狀態之立體圖。如圖 28(a)所示，該發光裝置 1 之密封方式是，針對由 P_2O_5-F 系玻璃所構成之筒狀體 60D 進行加熱，再將 GaN 系 LED 元件 2、連線 10 及一對引線 19 進行玻璃密封。

如圖 28(b)所示，筒狀體 60D 是由部分被切除之筒狀玻璃所構成，利用圖示未顯示之加熱器(Burner)等加熱裝置將筒狀體 60D 進行加熱、使玻璃溶解，再將 GaN 系 LED 元件 2、連線 10 及一對引線 19 進行玻璃密封。

藉由該第 11 實施形態，可依據溶解之玻璃之表面張力，針對 GaN 系 LED 元件 2、連線 10 及一對引線 19 進行玻璃密封。另外，本實施形態是讓溶融之玻璃附著之方式進行玻璃密封，但亦可於玻璃溶融之狀態下實施熱壓加工。

圖 29 是與第 12 實施形態有關之發光裝置之縱剖面圖，該發光裝置 1 於第 9 實施形態所說明之發光裝置 1 上配置有由環氧樹脂所構成之模具成形部。

模具成形部 9 具有半球狀之光學形狀面 9A，利用轉注成型法

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所形成。

該構成不僅能輕易地於玻璃密封型裝置上形成光學系統，且由於模具成形部9將玻璃密封部9包圍，因此可提高耐濕性。另外，引線拉出部並未由玻璃直接露出，有可防止引線彎曲時之應力所造成之玻璃之碎裂發生之效果。另外，模具成形部9除了環氧樹脂以外，亦可使用矽樹脂等樹脂材料形成；而轉注成型成形法之外，亦適用模具灌入成形法等手法。另外，亦可使用壓克力、碳酸乙酯等樹脂材料，以注入(Injection)法形成，此時可提高生產性。

以下詳細說明圖30至圖55所示之實施形態。

(光學元件)

光學元件包含發光二極體、雷射二極體及其他發光元件及受光元件。光學元件之受發光波長不侷限於特定波長，亦可使用於紫外光至綠光之範圍間有效之三族氮化合物半導體元件，或對紅光有效之GaAs系半導體元件。

密封構件之問題於放出短波長之三族氮化物系化合物半導體之發光元件上會特別突顯，三族氮化物系化合物半導體一般以AlxGaYIn1-X-YN(0＜X≦1、0≦Y≦1、0≦X＋Y≦1)來表示。其中含有Al的有2元系之AlN，3元系之AlxGa1-xN及AlxIn1-xN(其中，0＜X＜1)。三族氮化物系化合物半導體及GaN中，三族元素中至少有一部分可以被置換為硼(B)、鉈(Tl)等。另外，氮(N)之一部分亦可置換為磷(P)、砷(As)、銻(Sb)、鉍(Bi)等。

另外，三族氮化物系化合物半導體可以含有任何之摻雜物(Dopant)，n型不純物中可使用矽(Si)、鍺(Ge)、硒(Se)、碲(Te)、碳(C)等。而p型不純物則可使用鎂(Mg)、鋅(Zn)、鈹(Be)、鈣(Ca)、鍶(Sr)、鋇(Ba)等。另外，摻雜p型不純物後，不一定需要將三族氮化物系化合物半導體以電子線照射、電漿照射或以鍋爐等進行加熱。

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三族氮化物系化合物半導體層由MOCVD(有機金屬氣相磊晶成長)法所形成，但沒有必要將構成元件之所有半導體層以MOCVD法形成，亦可併用分子線結晶成長法(MBE法)、氫化物氣相磊晶法(HVPE法)、濺鍍(Sputter)法、離子電鍍(Ion Plating)法等。

發光元件之構成可使用以下幾種構造：具有MIS接合、PIN接合或pn接合之同質構造，異質(hetero)構造或雙異質(double-hetero)構造等。發光層可採用量子井構造(單一量子井構造或多重量子井構造)。該三族氮化物系化合物半導體之發光元件可利用以下兩種方式：(1)朝上(Face UP)方式：將光之主要受發光方向朝光裝置之光軸方向，(2)覆晶方式：將光之主要受發光方向朝向與光裝置之光軸方向相反方向，利用反射光。

三族氮化物系化合物半導體元件之耐熱溫度為600℃，而GaAs系半導體元件之耐熱溫度亦為600℃，兩者於低融點玻璃成型時均很安定。

(電力受送機構)

光裝置中含有電力受送機構，該電力受送機構是一將電力供給至發光元件、或將受光後於受光元件中之電力取出之電性零件；該電力受送機構包含(1)將光裝置與外部之電線進行連接之引線，(2)將該引線與光學元件進行配線之接合線(Bonding wire)，而接合線以金線或金合金線較多。該接合線本身、以及將接合線與引線或光學元件接合時之耐熱溫度為600℃以上，於低融點玻璃成形時均很安定。

(第1密封構件)

第1密封構件至少將光學元件與電力受送系統之一部分包覆，該第1密封構件於本發明中選擇的是：SiO_2-Nb_2O_5系、B_2O_3-F系、P_2O_5-F系、P_2O_5-ZnO系、SiO_2-B_2O_3-La_2O_3或SiO_2-B_2O_3系玻璃。

上述低融點玻璃均可於350~600℃間施壓成型，本發明第1

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密封構件可藉由自然溶著來形成。

亦可將螢光材料散佈於第 1 密封構件中，該螢光材料使用無機系螢光粉，可將之混合於低融點玻璃中。另外，亦將希土類離子摻雜於低融點玻璃中，使其產生螢光。將發光元件與螢光材料適當組合後，可獲得白光等任意顏色之光。

於第 1 密封構件與光學元件組合中，最好之條件如下：第 1 密封構件之阿貝數(Abbe Nmuber)在 40 以下，折射率 1.6 以上，光學元件之受發光波長在 546.1nm(Na 之 e 線之波長)以下。亦即，於高折射率材料內發光之光之外部量子效率，在對於發光波長之密封構件之折射率較高時較有利。光學材料之折射率是由 Na 之 d 線來定義，但一般波長愈短時，折射率愈高，折射率對光之波長之變化程度以阿貝數來表示。本發明不僅可防止以往於樹脂密封時會發生問題之短波長發光之發光元件中，因為選擇了 Na 之 d 線中具高折射率、且對波長之折射率之變化大之材料，導致樹脂變黃、使光輸出降低之問題；且實現了利用對短波長光有高折射率之材料進行密封、並獲得高外部量子效率。

具有該光學特性之低融點玻璃可以是 SiO_2-Nb_2O_5 系玻璃，其中又以 SiO_2-Nb_2O_2-Na_2O 玻璃較佳。

第 1 密封構件最好是至少將之配置於發光元件之光受、發方向上，並將之包覆之形態較佳，因為可確實防止該方向之變色。

第 1 密封構件之形狀並不做特別之限定，可針對光裝置所被要求之光學特性進行適當之設計。配置於發光元件之光放出方向之第 1 密封構件最好是凸透鏡型。

(第 2 密封構件)

本發明之光學元件亦有以包括以上說明之第 1 密封構件在內之多種密封構件進行密封之情形，此時第 2 密封構件是從主受發光方向及其反方向將光學元件包覆。

第 2 密封構件亦與第 1 密封構件相同，其低融點玻璃可由 SiO_2-Nb_2O_5 系、B_2O_3-F 系、P_2O_5-F 系、P_2O_5-ZnO 系、SiO_2-B_2O_3-La_2O_3

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及 SiO_2-B_2O_3 系中選擇；而第 2 密封構件可以是與第 1 密封構件是相同或不同之材料。當兩者是不同材料時，第 1 密封構件(存在於光學元件之主要受發光方向)之折射率最好是高於第 2 密封構件之折射率；藉此，當使用發光元件做為光學元件時，發光元件與密封構件之界面之臨界角會變大，能提高光效率。

與第 1 密封構件同樣，由低融點玻璃構成之第 2 密封構件可藉加壓模具(Press Mold)成形或以自然溶著之方式形成。

另外，與第 1 密封構件同樣，可將螢光材料散佈至由低融點玻璃構成之第 2 密封構件中。

第 2 密封構件亦可以利用非透明材料形成，該第 2 密封構件除了低融點玻璃外，亦可以是金屬板、陶瓷板等；此時，第 2 密封構件最好是能有效率地將光進行反射之材料所製成。以低融點玻璃以外之材料形成第 2 密封構件時，第 1 密封構件之線膨脹係數值最好是介於該第 2 密封構件之線膨脹係數與光學元件之線膨脹係數之間；藉此，即使當光學裝置於回銲(Reflow)爐等當中進行熱處理時，亦可減輕因為不同材料之線膨脹係數不同所導致之光裝置之內部應力。

以下說明本發明之實施例。

(第 1 實施例)

此實施例之光學元件使用的是圖 30 所示之朝上(Face Up)型三族氮化物系化合物半導體發光元件 1010，此發光元件釋放出藍色系之光。

發光元件 1010 各層之規格如下：

層別	組成
p 型層 1015	p-GaN：Mg
包含發光層之層 1014	包含 InGaN 層
n 型層 1013	n-GaN：Si
緩衝層 1012	AlN
基板 1011	藍寶石

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將摻雜 n 型不純物之矽(Si)之由 GaN 所構成之 n 型層 1013 透過緩衝層 1012 形成於基板 1011 上，此時基板 1011 使用的是藍寶石，但不限於此，除了藍寶石外，亦可使用尖晶石、碳化矽、氧化鋅、氧化鎂、氧化錳、硼化鋯、三族氮化物系化合物半導體單結晶等。其次，緩衝層是使用 AlN 以 MOCVD 法所形成，但不限於此，亦可使用 GaN、InN、AlGaN、InGaN 及 AlInGaN 為材料，可使用之方法有分子線結晶成長法(MBE 法)、氫化物氣相磊晶法(HVPE 法)、濺鍍(Sputter)法、離子電鍍(Ion Plating)法等。將三族氮化物系化合物半導體做為基板時，可省略該緩衝層。

半導體元件形成後，可視必要將基板及緩衝層除去。

此時之 n 型層 1013 是由 GaN 所形成，但亦可使用 AlGaN、InGaN 或 AlInGaN。

另外，n 型層 1013 摻雜有 n 型不純物-矽，但亦可摻雜 Ge、Se、Te、C 等做為 n 型不純物。

包含發光層之層 1014 亦可以包含量子井構造(多重量子井構造或單一量子井構造)，而發光元件之構造可以是單異質(Single-Hetero)型、雙異質(Double-Hetero)型及同質接合等。

包含發光層之層 1014 於 p 型層 1015 側可包含摻雜有 Mg 等、能隙(Band Gap)較寬之三族氮化物系化合物半導體層，因為可有效地防止被注入包含發光層之層 1014 中之電子擴散至 p 型層 1015 中。

包含發光層之層 1014 上形成有 p 型層，該 p 型層由摻雜有做為 p 型不純物-Mg 之 GaN 所構成，該 p 型層 1015 可以是 AlGaN、InGaN 或 InAlGaN，而 p 型不純物亦可使用 Zn、Be、Ca、Sr、Ba。導入 p 型不純物後，可使用電子線照射、鍋爐加熱或電漿照射等眾知之方法來降低電阻。上述構成之發光元件中，各三族氮化物系化合物半導體可利用 MOCVD、以一般條件形成，亦可利用分子線結晶成長法(MBE 法)、氫化物氣相磊晶法(HVPE 法)、濺鍍(Sputter)法、離子電鍍(Ion Plating)法等。

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n 電極 1018 是由 Al 與 V 之 2 層所構成，是於 p 型層 1015 形成後，是於將 p 型層 1015、包含發光層之層 1014 及 n 型層之一部分利用蝕刻去除後露出表面之 n 型層 1013 上以蒸著方式所形成。

透光性電極 1016 是包含金之薄膜，層積於 p 型層 1015 上。p 電極 1017 亦是由含金之材料所構成，藉由蒸著方式形成於透光性電極 1016 上。藉上述步驟將各層、各電極形成之後，接下來是各晶粒(Chip)之切割步驟。

如圖 31 所示，該發光元件 1010 之構造是：將發光元件固定於做為電力受送機構之裝載引線(Mount Lead)1021 上，並由發光元件 1010 上之電極處分別將接合線 1023、1024 懸架至裝載引線 1021 與其他電力受送機構之次引線 1022 處。為使從發光元件 1010 發出之光能有效率地反射，裝載引線 1021 之表面有鍍銀；另外，為確保光之反射效率，亦可使用無機系白色接著劑將發光元件 1010 固定至裝載引線 1021 處。再者，亦可使用接近純銅之銅合金等具有高散熱性之材料，而接合線使用的是金線。

圖 30 所示之組裝體 1020 被當做中心，以如圖 32 所示之方式被配置至壓著用模具 1025。先將低融點玻璃分別配置至該壓著用膜 1025 之凹部 1026、1027，藉由封閉該模具 1025，形成圖 33 所示之密封構件 1028(第 1 密封構件)。本實施例中，低融點玻璃選擇的是 P_2O_5-F 系玻璃(株式會社住田光學玻璃：商品名 K-PG325)，形成溫度為 430℃。結果如圖 33 所示，發光元件 1010 之全部、引線 1021 及 1022 之一部分被半球型之密封構件 1028 所包覆；該密封構件 1028 之形狀可因應光裝置 1022 所被要求之光學特性進行適當之設計，亦可採用砲彈型等。

(第 2 實施例)

如圖 34 所示之光裝置 1003 是於如圖 33 之光裝置 1001 中，將螢光材料加入低融點玻璃中所形成。另外，與圖 33 有相同要素之部分則加上同一符號、並省略說明。本實施例中之密封構件 1038 是摻雜有做為螢光材料之希土類元素之低融點玻璃所形成。

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藉由將任意之螢光材料加入低融點玻璃中之方式，可控制光裝置 1003 之發光顏色。

(第 3 實施例)

圖 35 所示之光裝置 1004 是於圖 4 之光裝置 1002 中以砲彈型蓋子(Cover)1048 將密封構件 1028 包覆，此蓋子 1048 由環氧樹脂及其他透光性樹脂所形成，再由模具成型。配置該蓋子可獲得大尺寸之光裝置。藉此，製作標準形狀之玻璃密封體，之後以模具型設備或作業更容易之樹脂即可獲得多樣之光學系統。此時，由發光元件所發出之光之密度高，且溫度上升之發光元件旁是玻璃材料，可將光輸出之劣化降低之可忽略之程度。另外，亦可以蓋子 1048 將圖 34 所示之密封構件 1038 包覆；另外，亦可利用該蓋子 1048 將下文會說明之圖 36、圖 38、圖 39 所示之各密封構件 1058、1068、1069 及 1079 包覆。該蓋子 1048 中亦可含有螢光材料。

(第 4 實施例)

圖 36 所示之光裝置 1005 具有以自然溶著方式所形成之密封構件 1058，與圖 33 相同要素之部分則加上同一符號、並省略說明。

密封構件 1058 是由以下之方式所形成。如圖 37 所示，先準備由低融點玻璃所構成之筒狀體 1058a，將之套至發光元件 1010 與引線 1021、1022 之組合體上，之後將之放入爐體中、軟化筒狀體 1058a。結果是，筒狀體 1058a 因為材料之表面張力而將組合體 1020 以凸透鏡之方式包覆。

本實施例不需要壓著用模具，可提供一廉價之光裝置。

(第 5 實施例)

圖 38 所示之光裝置 1006 是使用異種低融點玻璃將發光元件 1010 及引線 1021、1022 包覆。另外，圖 38 中，與圖 33 相同要素之部分則加上同一符號、並省略說明。

圖 38 之例子中，發光元件與上述實施例相同，使用藍光之發光元件，發光元件 1010 上方(主要之光放出方向)利用由

SiO_2-Nb_2O_5系玻璃所構成之第1密封構件6108(折射率1.8、阿貝數25)進行密封，而發光元件1010之下方(與主要之光放出方向相反之方向)則利用由P_2O_5-F系玻璃所構成之第2密封構件1069進行密封。從提高光取出效率之觀點，第1密封構件1068選擇高折射率材料；另外，上述方式所衍生之製造上之問題則藉由第2密封構件緩和，並可進行實際製作。結果是，第1密封構件1068之折射率較第2密封構件1069之折射率大。另外，第1密封構件1068選擇阿貝數較小之材料，對藍光發光元件之實際折射率變大。

圖38所示之光裝置1006可以是以將填充於圖35之模具1025之凹部1026、1027中之材料使用不同材料之方式形成。

另外，使用紅色系做為發光元件時，使用折射率高、阿貝數大之材料做為第1密封構件1068之情形下，可選擇實際折射率大之材料；例如，折射率1.8、阿貝數45之SiO_2-B_2O_3-La_2O_3系玻璃。(第6實施例)

圖39所示之光裝置1007使用金屬薄板做為第2密封構件1079。與圖38相同要素之部分則加上同一符號、並省略說明。使用金屬材料做為第2密封構件時，可將發光元件1010發出之光做有效率之反射。第2密封構件1079是專門用來發揮其反射板之目的，而除了金屬薄板之外，亦可使用其他樹脂板。

此發光裝置1007之製造方式如下：如圖40所示，發光元件1010與引線1021、1022之組合體1020之背面貼有金屬薄板1079，並以此為中心設置模具1025；此時，低融點玻璃僅被填充於壓著模具1025上方之凹部1026，之後封閉模具，獲得圖39之發光裝置1007。

如本實施例般，第1密封構件1068與第2密封構件1079由不同材料形成時，第1密封構件之線膨脹係數值最好是介於第2密封構件之線膨脹係數與發光元件之線膨脹係數之中間較佳。(第7實施例)

本實施例使用覆晶型發光元件1100，如圖41所示，覆晶型發

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光元件之構成方式是：於圖 30 之發光元件中，取代透光性電極 1016 與 p 電極 1017，而於 p 型層 1015 之整面層積厚膜之 p 電極。另外，與圖 30 相同之要素之部分則加上同一符號、並省略說明。

將該覆晶型發光元件 1100 透過次裝載基台 1110 裝載至裝載引線 1021 處，次裝載基台 1110 與次引線 1022 間利用接合線 1124 連接、形成組合體 1120。該次裝載基台 1110 上形成有電路圖案，發光元件 1100 之各電極 1018、1101 直接、或透過接合線 1124 與引線 1021、1022 間有電連接。將該組合體 1120 做為中心，與第 1 實施例一樣，形成密封材料 1028，最後獲得如圖 42 之光裝置 1008。於具備覆晶型發光元件之發光裝置中，密封步驟中非常纖細之接合線僅有一條，因此步驟管理非常容易，且可提升製造良率。另外，接合線並不靠近發光元件之發光面，因此並不影響外部放射效率。

另外，與第 1 實施例相同之要素則附加同一符號、並將說明簡略化。

圖 41 所示之覆晶型發光元件 1100 之組合體 1120 亦適用第 2 至第 6 實施例中所說明之密封構件，如圖 42 至圖 45 之說明。另外，由於簡化了說明，與既說明之要素相同之部分則使用同一符號、並省略說明。

(第 8 實施例)

本實施例中，如圖 47 所示，於由 AlN 等所構成之無機材料基板 1200 表面形成做為電力受送機構之電路圖案 1201、1202。覆晶型發光元件 1100 透過凸塊 1205、1206 被裝載至該電路圖案 1201、1202 處。另外，基盤 1200 藉由共晶材料被安裝至引線 1021、1022 處。與第 1 實施形態相同，將該組合體 1220 做為中心形成密封構件 1028，之後獲得如圖 48 所示之光裝置 1009。

另外，與第 1 實施例相同之要素則附加同一符號、並將說明簡略化。

圖 47 所示之組合體 1220 亦適用第 2 至第 6 實施例所說明之

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密封構件，如圖 49~51 所示。另外，由於簡化了說明，與既說明之要素相同之部分則使用同一符號、並省略說明。

上述實例是以密封構件將組合體 1220 整體包覆，但如圖 52 所示，亦可將發光元件 1100 與電路圖案 1201、1202 之一部分利用密封構件 1228 進行包覆。圖 53 所示之構成之光裝置可當做晶粒型 LED 運用。

本實施例之光裝置並不存在對熱、機械脆弱之接合線，且裝置內不含有機材料，因此可在高溫下壓著形成一低融點玻璃。另外，對回銲爐等之熱處理亦很安定。因此，相當容易製造，適用之低融點玻璃之選擇變多，可提供一廉價之光裝置。

不限於以上之共晶材料，亦可利用金凸塊進行光學元件之裝載，藉此可形成無線、僅有無機材料之安定之裝置。

(第 9 實施例)

本實施例之光裝置之剖面圖如圖 54、俯視圖則如圖 55 所示。

該發光裝置 1230 具備覆晶型發光元件 1100、AlN 基板 1231、金屬圖案 1236 及密封構件 1238。

本實施例中基板 1231 由 AlN 所構成，但亦可使用至少發光元件 1100 之安裝面是由 AlN 等絕緣材料形成之東西，例如使用以鋁板形成基板之基部、表面層積 AlN 之基板；AlN 之外，絕緣材料可使用 Al_2O_3 等。

基板 1231 上形成有通孔(Through Hole)1231、1232。

基板 1231 之安裝面之幾乎整面被金屬圖案 1235、1236 所包覆，本實施例利用金屬化法形成金屬圖案 1235、1236。因此，金屬圖案 1235、1236 與基板 1231 之結合力很強，且與基板 1231 之接觸面積變大之故，可提高兩者之結合力。實施例中之金屬圖案 1235、1236 是於鎢(W)上鍍鎳，並於發光元件裝載部及金屬圖案露出部(未被低融點玻璃密封處)鍍金。該金屬材料可與基板安裝面之絕緣材料及由低融點玻璃所構成之密封構件強力結合。另外，玻璃與金屬材料之熱膨脹係數略為相同(約在 $10\sim20\times10^{-6}$(1/℃))，

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不容易產生熱收縮應力；另外，金屬圖案之形狀及形成材料可因應基板安裝面與密封構件之材料進行適當之選擇。

金屬圖案 1235、1236 是針對發光元件 1100 進行電力受送之機構，另外，形成與該電力受送機構分開之金屬圖案，可確保基板與密封構件間之結合力。

覆晶型發光元件 1100 之電極面(圖示之下側)鍍有共晶材料；發光元件 1100 在通過一般之回銲爐後，被銲接在金屬圖案 1235、1236 上。

此處，發光元件 1100 之電極表面上廣泛、但薄薄地鍍有共晶材料，因此具有優良之將熱導引至基板側之性能。另外，如覆晶型發光元件般，p 電極與 n 電極間之間隔即使很窄，亦不會短路。

密封構件 1238 是由對於發光元件 1100 之波長為透明之低融點玻璃所構成，該低融點玻璃可以由以下低融點玻璃中選擇：SiO_2-Nb_2O_5 系、B_2O_3-F 系、P_2O_5-F 系、P_2O_5-ZnO 系、SiO_2-B_2O_3-La_2O_3 或 SiO_2-B_2O_3 系。

密封構件 1238 於減壓之氮氣中以模具成型。

藉由該光裝置 1230，形成密封構件 1238 之低融點玻璃與形成金屬圖案 1235、1236 之金屬間之接著性提高，且可確保該金屬與 AlN 基板 1231 間之高度接著性。因此，密封構件 1238 可強固地與基板 1231 接合，幾乎不會發生界面剝離之情形。另外，此光裝置並不存在對熱、機械脆弱之接合線，且裝置內不含有機材料，因此可在高溫下壓著形成一低融點玻璃。另外，對回銲爐等之熱處理亦很安定。因此，相當容易製造，適用之低融點玻璃之選擇變多。

以下詳細說明圖 56 至 64 所示之實施形態。

(光學元件)

光學元件包含發光二極體、雷射二極體及其他發光元件及受光元件。光學元件之受發光波長不侷限於特定波長，亦可使用對紫外光至綠光有效之三族氮化合物半導體元件，或對紅光有效之

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GaAs 系半導體元件。其他，亦可使用 SiC、AlInGaP 等形成之光學元件。

密封構件之問題於放出短波長之三族氮化物系化合物半導體之發光元件會特別突顯。三族氮化物系化合物半導體一般以 AlxGayIn1-X-yN(0＜X≦1、0≦Y≦1、0≦X＋Y≦1)來表示。其中含有 Al 的有 2 元系之 AlN，3 元系之 AlxGa1-xN 及 AlxIn1-xN(其中，0＜X＜1)。三族氮化物系化合物半導體及 GaN 中，三族元素中至少有部分可以置換為硼(B)、鉈(Tl)等。另外，氮(N)之一部分亦可置換為磷(P)、砷(As)、銻(Sb)、鉍(Bi)等。

另外，三族氮化物系化合物半導體可以含有任何之摻雜物，n 型不純物中可使用矽(Si)、鍺(Ge)、硒(Se)、碲(Te)、碳(C)等。而 p 型不純物則可使用鎂(Mg)、鋅(Zn)、鈹(Be)、鈣(Ca)、鍶(Sr)、鋇(Ba)等。另外，摻雜 p 型不純物後，不一定需要將三族氮化物系化合物半導體以電子線照射、電漿照射或以鍋爐等進行加熱。

三族氮化物系化合物半導體層由 MOCVD(有機金屬氣相磊晶成長)法所形成，但沒有必要將構成元件之所有半導體層以 MOCVD 法形成，亦可併用分子線結晶成長法(MBE 法)、氯化物氣相磊晶法(HVPE 法)、濺鍍(Sputter)法、離子電鍍(Ion Plating)法等。

發光元件之構成可使用以下幾種構造：具有 MIS 接合、PIN 接合或 pn 接合之同質構造，異質(hetero)構造或雙異質(double-hetero)構造等。發光層可採用量子井構造(單一量子井構造或多重量子井構造)。該三族氮化物系化合物半導體之發光元件可利用以下兩種方式：(1)朝上(Face UP)方式：將光之主要受發光方向朝光裝置之光軸方向，(2)覆晶方式：將光之主要受發光方向朝向與光裝置之光軸方向相反方向，利用反射光。

三族氮化物系化合物半導體元件之磊晶(EPI)成長溫度約在 1050℃，而 GaAs 系半導體元件之 EPI 成長溫度之耐熱溫度則在 600℃以上，兩者均因使用低融點玻璃，而可實現一不受熱所造成

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之不良影響之加工。

(無機材料基板)

本發明之光裝置之前述說明中之光學元件係被裝載於無機材料基板上，而無機材料基板之基礎材料及形狀可因應光裝置之用途而進行適當之選擇，亦可使用例如 AlN、Al_2O_3、含有玻璃成分之 Al_2O_3 等矩形板狀之材料。

基板中至少其表面是由上述基礎材料所形成即可，例如可使用中心部份以 Al 或 Al 合金所形成、表面則以 AlN 包圍之方式所形成之基板。

(金屬圖案)

無機材料基板上形成有金屬圖案，將光學元件之各電極與外部電路做電性結合，針對光學元件傳送、接收電力；亦即，當光學元件為發光元件時，即由外部電路對光學元件施加電力，而當光學元件為受光元件時，則將光學元件所發生之電力向外部電路送出。

本發明之金屬圖案除了上述電力之受送功能外，並具有將無機系密封構件安定地與無機材料基板進行接合之接著層之功能。密封構件是以將光學元件包圍之方式被配置，該金屬圖案亦是以一區域之方式將光學元件包圍，因此可將介於密封構件與無機材料基板間之金屬圖案之面積極大化。另外，包圍光學元件之金屬圖案並不限定為連續體，亦可以是一非連續體。該非連續體之金屬圖案中並不需要是所有部分均須具備電力受送功能。

金屬圖案具有將光進行反射之功能，以此將光學元件包圍，可在不漏失光學元件之光之情況下進行反射，提高光之取出效率。例如，由黑色 AlN 構成之基板會吸收光學元件發出之光，而由 Al_2O_3 構成之基板又會讓光學元件發出之光透過，因此利用金屬圖案將光學元件包圍之方式可讓光學元件發出之光有效率地向外部反射。

金屬圖案之形成材料可因應密封構件之材質及無機材料基板

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之材料，適當選擇與該等結合性佳之材料，且金屬材料亦可以是該等之多層構造。例如可採用以下材料做為金屬圖案之形成材料：W、W\Ni(於 W 上層積 Ni)、W\Ni\Ag(於 W 上順次層積 Ni 與 Ag)、銅箔等。

此時，W 層因加熱之故，會以楔型狀進入密封構件或基板之無機材料中，然後於兩者間形成一強固之結合。於 W 層上形成 Ni 層時，Ni 層與密封構件間因加熱而產生化學結合，使兩者獲得強固之結合。

Ag 層是將金屬圖案之光反射效率提高之高反射率層，在光學元件之週邊部位部分地形成之較佳；另外，裝載光學元件之部分可形成 Au 層做為結合機構，該 Au 層可將光學元件與金屬圖案接著。

可使用金凸塊做為結合機構，而除了金凸塊外，亦可使用銲錫凸塊或鍍上銲錫之共晶材料做為裝載結合機構。

從縮小基板之熱變形量之觀點看，基板之光學元件裝載面(表面)之實質上之全面最好形成有該金屬圖案。

於基板背面亦形成金屬圖案時，若基板上形成有通孔(Through Hole)，並將金屬圖案之材料通過通孔時，則基板表面與圖案及基板背面之圖案可進行連結。由於電端子從裝載有光學元件之面被拉出至背面，因此並不需要在基板之裝載有光學元件之面，為了電端子而特別設置沒有被光學元件之密封構件覆蓋之地方，因此量產性佳。此時基板若無貫通孔，則裝載有光學元件之面之光學元件之密封構件並不會被拉出至背面。

金屬圖案之形成方式並未有特定限制，實施例中是於無機材料基板上實施鎢膠之網板印刷，之後燒烤，將 W 之金屬圖案形成於無機材料基板上。其次於 W 層上鍍金，形成由 W\Ni 所構成之金屬圖案，之後加熱處理；W\Ni\Ag 則是於鍍金之 Ni 層上再鍍銀。

上述金屬層是以濺鍍或其他眾所皆知之方法形成。

(密封構件)

無機系密封構件對光學元件之受發光波長呈現透明，雖然只要是保護光學元件之材料的話，即不做特別的限制，但考慮到光學元件之耐熱溫度為600℃，最好是採用具有較其還低之融點(軟化點)之低融點玻璃較佳。

該低融點玻璃除了鉛玻璃或硫族元素(Chalcogen)化物玻璃外，亦可使用 SiO_2-Nb_2O_5 系、B_2O_3-F 系、P_2O_5-F 系、P_2O_5-ZnO 系、SiO_2-B_2O_3-La_2O_3 或 SiO_2-B_2O_3 系。上述低融點玻璃均可於350~600℃中熱壓成形。

亦可將螢光材料散佈於密封構件中，該螢光材料使用無機系螢光粉，可將之混合於低融點玻璃中。另外，亦可將希土類離子摻雜於低融點玻璃中，使其產生螢光。將發光元件與螢光材料適當組合後，可獲得白光等任意顏色之光。

此密封構件與光學元件之組合中，密封構件之阿貝數在40以下、折射率在1.6以上、且光學元件之受發光波長在546.1nm(Na之e線之波長)以下之條件較佳；亦即，以在高屈折材料內發光之光之外部量子效率來說，相對於發光波長之密封材料之折射率愈高愈好。光學材料之折射率由Na之d線來定義，一般波長愈短，其折射率愈高，而相對於光波長之折射率之變化程度則由阿貝數來表示。特別是，本發明除了可防止以往在樹脂密封時會成為問題之短波長發光之發光元件中，因為選擇了Na之d線中高折射率、相對於波長之折射率變化大之材料，使樹脂變黃、導致光輸出降低之問題外，在實質上還可達成以相對於短波長有高折射率之材料進行密封，獲得較高之外部量子效率。

具有該光學特性之低融點玻璃可以是 SiO_2-Nb_2O_5 系玻璃，其中又以 SiO_2-Nb_2O_5-Na_2O 玻璃較佳。

將板狀之低融點玻璃之密封構件重疊於光學元件上，並將之加熱、使其軟化，之後即可利用密封構件將發光元件元件圍繞。為使密封構件與光學元件間不會有空氣混入，該加熱最好是於減壓環境下進行。藉由該加熱，低融點玻璃與金屬圖案之界面間會

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產生化學反應，使兩者能強固地接著。

以下以實施例說明本發明。

(第 10 實施例)

此實施例之光學元件使用的是圖 56 所示之覆晶型三族氮化物系化合物半導體發光元件 2010，此發光元件釋放出藍色系之光。

發光元件 2010 各層之規格如下：

層別	組成
p 型層 2015	p-GaN：Mg
包含發光層之層 2014	包含 InGaN 層
n 型層 2013	n-GaN：Si
緩衝層 2012	AlN
基板 2011	藍寶石

將摻雜 n 型不純物之矽(Si)之由 GaN 所構成之 n 型層 2013 透過緩衝層 2012 形成於基板 2011 上。此時，基板 2011 使用的是藍寶石，但不限於此，可使用的有藍寶石、尖晶石(spinel)、碳化矽、氧化鋅、氧化鎂、氧化錳、硼化鋯、三族氮化物系化合物半導體單結晶等。其次，緩衝層是使用 AlN 以 MOCVD 法所形成，但不限於此，亦可使用 GaN、InN、AlGaN、InGaN 及 AlInGaN 為材料，方法則有分子線結晶成長法(MBE 法)、氫化物氣相磊晶法(HVPE 法)、濺鍍(Sputter)法、離子電鍍(Ion Plating)法等。將三族氮化物系化合物半導體做為基板時，可省略該緩衝層。

其次，半導體元件形成後，可視必要性將基板及緩衝層除去。

此時之 n 型層 2013 是由 GaN 所形成，但亦可使用 AlGaN、InGaN 或 AlInGaN。

另外，n 型層 2013 摻雜有 n 型不純物-矽，但亦可摻雜 Ge、Se、Te、C 等做為 n 型不純物。

包含發光層之層 2014 亦可以包含量子井構造(多重量子井構造或單一量子井構造)，而發光元件之構造可以是單異質(Single-Hetero)型、雙異質(Double-Hetero)型及同質接合等。

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包含發光層之層 2014 之部分，其 p 型層 2015 側可包含摻雜有 Mg 等之能隙(Band Gap)較寬之三族氮化物系化合物半導體層。

包含發光層之層 2014 上形成有 p 型層 2015，該 p 型層 2015 由摻雜有做為 p 型不純物-Mg 之 GaN 所構成，該 p 型層 2015 可以是 AlGaN、InGaN 或 InAlGaN，而 p 型不純物亦可使用 Zn、Be、Ca、Sr、Ba。導入 p 型不純物後，可使用電子線照射、鍋爐加熱、電漿照射等眾知之方法來降低電阻。上述構成之發光元件中，各三族氮化物系化合物半導體可利用 MOCVD、以一般條件形成，亦可利用分子線結晶成長法(MBE 法)、氫化物氣相磊晶法(HVPE 法)、濺鍍(Sputter)法、離子電鍍(Ion Plating)法等。

n 電極 2018 是由 Al 與 V 之 2 層所構成，是於 p 型層 2015 形成後，於將 p 型層 2015、包含發光層之層 2014 及 n 型層 2013 之部分利用蝕刻去除後露出表面之 n 型層 2013 上以蒸著方式所形成。p 電極 2016 以蒸著之方式層積於 p 型層 2015 上。藉上述步驟將各層、各電極形成之後，接下來是各晶粒(Chip)之切割步驟。

其次，準備裝載該發光元件 2010 之無機材料基板。

針對由 AlN 構成之燒烤前之無機材料基板 2021 之兩面進行含有鎢膠之網板印刷，成為如圖 57 所示之圖案 2023、2024。如圖 57(b)所示，基板 2021 上形成有通孔(Through Hole)2025，裝載面(表面)之圖案 2023 透過該通孔 2025 與背面之圖案 2024 有電性結合。然後以超過 1500℃之溫度燒烤 AlN，並將鎢膠燒印至基板 2021 上，藉此，W 與基板可強固地結合。該 W 亦可利用濺鍍法形成，且除了 W 之外，亦可使用 Mo 等高融點金屬。

其次，利用電鍍法對基板 2021 表面之 W 圖案 2023 上之 Ni 層以 700℃加熱，使 Ni 與 W 產生反應。藉此，AlN 基板 2021 上之金屬圖案會被強固地接合。其次，如圖 58 所示，藉由金凸塊 2027、2028，發光元件 2010 會被裝載於規定之位置；而凸塊 2027 會與發光元件 2010 之 n 電極 2018 連結，凸塊 2028 則與發光元件 2010 之 p 電極 2016 連結。發光元件 2010 會在如圖 58(a)所示之狀

態下被金屬圖案 2023 所包圍。

其次，如圖 59 所示，將密封構件所構成之板狀低融點玻璃重疊於基板 2021 之表面，然後於減壓環境中進行加熱、融著，針對發光元件進行密封。藉此，金屬表面之 Ni 會透過 Ni 表面之氧化物與低融點玻璃 2029 產生化學性之強固結合，並可以防止密封時會有殘留氣泡之發生。

另外，採用覆晶型做為發光元件時，因為可省略接合線(Bonding Wire)，所以機械性很穩定，使該構成之光裝置很適合量產步驟。最後，將基板 2021 於分割線 D 處進行分割，而後獲得實施例之光裝置。

(第 11 實施例)

圖 60 至圖 63 是其他實施例之光裝置。

圖 60 是光裝置之俯視圖，該光裝置之基板表面(裝載面)之圖案分為第 1 部分(環狀部分)2103，與第 2 部分(結合部分)2104、2105；第 1 部分 2103 上形成有多個孔穴 2107，且形成有延伸至基板周圍之導電部 2108，目的是電鍍時施加電力。

與第 10 實施例之方式相同，第 1 部分 2103 是 W 層與 Ni 層之層積體，再於其上方貼上無機系密封構件；此時，基板 2110、第 1 部分 2103 與密封構件 2140 間會有強固的結合。以電鍍方式形成、由 Cu 所構成之第 2 部分 2104、2105 會貫通第 1 基板 2111。

本實施例之基板 2110 之基本材料為 Al_2O_3，是由第 1 基板 2111 與第 2 基板 2112 兩者貼合構成。各基板之基本材料可使用 AlN、含有玻璃成分之 Al_2O_3 等其他無機材料，且第 1 基板 2111 之基礎材料與基板 2112 之基礎材料可以不同。

第 1 基板 2111 之基礎材料上形成有貫通孔 2107，該孔 2107 周圍亦層積有做為金屬圖案之第 1 部分 2103 之金屬層。

第 2 基板 2112 之表面形成有圖 62 所示之金屬圖案 2120、2121、2122；有切角之環狀金屬圖案 2120 與第 1 基板 2111 之孔穴為相對之方向；該金屬圖案 2120 與第 1 金屬圖案之第 1 部分

2103 相同，由 W 層與 Ni 層之層積體所構成。藉由上述方式構成之金屬圖案 2120，可使其與深入至孔穴 2107 底部之密封構件之無機系材料(低融點玻璃等)之間有充分之結合力。

形成於第 2 基板 2112 中央之金屬圖案 2121、2122 分別被形成於相對於第 1 基板 2111 中央之金屬圖案之第 2 部分 2104、2105 之位置處。將第 1 基板 2111 與第 2 基板 2112 貼合時，金屬圖案 2121、2122 分別與第 2 部分 2104、2105 間有電性結合。該金屬圖案 2121、2122 是於 W 層與 Ni 層之層積體上再層積 Au 所得。設置有 Au 層時，金屬圖案 2121、2122 與第 2 部分 2104、2105 間之結合性會提高。

第 2 基板 2112 上形成有貫通孔 2125、2126，且第 2 基板 2112 之背面形成有大面積之金屬圖案 2131、2132。第 2 基板 2112 之表面之金屬圖案 2121 透過填充於貫通孔 2125 內之導電性金屬材料與背面之金屬圖案 2131 間有電性結合。藉此，電力會透過第一基板 2111 之表面之金屬圖案 2104，從金屬圖案 2131 處傳送至元件 2010 之其中一方之電極。相同的，第 2 基板 2112 之表面之金屬圖案 2122 透過填充於貫通孔 2126 內之導電性金屬材料與背面之金屬圖案 2132 間有電性結合。藉此，電力會透過第一基板 2111 之表面之金屬圖案 2105，從金屬圖案 2132 處傳送至元件 2010 之另一方之電極。

形成於第 2 基板 2112 背面之金屬圖案 2131、2132 上分別形成有導電部 2135、2136，該導電部 2135、2136 之使用時機是以電鍍形成金屬圖案 2131、2132 時。

第 2 基板 2112 背面之金屬圖案 2131、2132 是於 W 層與 Ni 層之層積體上再層積 Au 所得。設置有 Au 層時，金屬圖案 2131、2132 與外部電極間之結合性會提高。貫通孔 2125 及 2126 內之金屬材料是於形成該金屬圖案 2131、2132 及表面之金屬圖案 2121、2122 時一併形成。

本實施例中，分別準備第 1 基板 2111 與第 2 基板 2112，再將

兩者結合，形成無機材料基板 2110；第 1 基板 2111 與第 2 基板 2112 之結合方法並無限定，亦可使用接著劑。

分割基板 2110 時，可於分割面形成金屬圖案，提高電路設計之自由度；另外，孔穴 2107 貫通基板 2110，密封構件之材料狀態有可能使其與支撐基板 2110 之下方模型接著，導致脫膜不佳之情形。若如同本實施例般，孔穴 2107 有底層時，即可將密封構件材料與下方模型之接觸做事前防範。另外，孔穴 2107 為貫通時，不容易將以抽出密封構件與基板表面間空氣為目的之負壓分布至基板全面；另外，孔穴 2107 有底層時，密封構件與基板間之空氣即使有殘存，空氣會進入該孔穴，可防止密封構件與基板間有氣泡之產生。以第 2 基板 2112 將形成於第 1 基板 2111 之貫通孔之其一開口部堵住以形成有底層之孔穴 2107 時，與在一片板狀之基板上穿設有底層之孔穴之情形比較，前者之量產性較佳。

由無機系透光材料所構成之密封構件 2140 被基板 2110 之表面所覆蓋，密封構件 2140 之材料不僅與基板 2110 之表面金屬圖案 2103 有強固的結合，本實施例中，密封材料 2140 之材料會進入孔穴 2107 中，使該密封構件 2140 之材料與基板 2110 間有物理性的結合；藉此密封構件 2140 與基板 2110 間即使有極大之熱膨脹係數之差異，仍可物理性地抑制兩者之變形，可確實防止密封構件 2140 從基板 2110 處剝離。

如此，於覆蓋有密封構件之基板面設置凹凸構造，可使密封構件與基板有物理性之結合，可確實防止密封構件從基板剝離。該凹凸除了本實施例之有底層之孔穴外，亦可使用溝槽或貫通孔；再者，對基板面施行粗糙(Ra=0.5um)處理時，可使兩者有物理性之結合。

將基板之基礎材料表面做粗糙處理時，即使於其上方形成金屬圖案，該粗糙亦反映至該金屬圖案表面。另外，僅於金屬圖案 2103 設置孔穴時，例如將金屬圖案 2103 形成格子狀時，亦可形成上述之凹凸構造。該凹凸構造之作用於以下情況下亦有效：在不

透過金屬圖案，將由無機系透光性材料所形成之密封構件覆蓋於無機材料基板之基礎材料之情況。

圖 64 之例子是於第 10 實施例之光學元件之基板設置有底層之孔穴 2257 之情況，如該圖 64 及圖 60 所示，孔穴、亦即凹凸最好是均勻分配於基板面，目的在確保基板全面之密封材料與凹凸構造間之結合，防止兩者產生剝離。

以下詳細說明圖 65 至圖 74 所示之實施形態。

(光學元件)

光學元件包含發光二極體、雷射二極體及其他發光元件及受光元件。光學元件之受發光波長不侷限於特定波長，亦可使用於紫外光至綠光之範圍間有效之三族氮化物系化合物半導體元件，或於紅光有效之 GaAs 系半導體元件。此外，亦可使用 SiC、AlInGaP 等所形成之光學元件。

密封構件之問題於放出短波長之三族氮化物系化合物半導體之發光元件會特別突顯。三族氮化物系化合物半導體一般以 AlXGaYIn1-X-YN(0＜X≦1、0≦Y≦1、0≦X＋Y≦1)來表示。其中含有 Al 的有 2 元系之 AlN，3 元系之 AlxGa1-xN 及 AlxIn1-xN(其中，0＜X＜1)。三族氮化物系化合物半導體及 GaN 中，三族元素中至少有一部分可以被置換為硼(B)、鉈(Tl)等。另外，氮(N)之一部分亦可置換為磷(P)、砷(As)、銻(Sb)、鉍(Bi)等。

另外，三族氮化物系化合物半導體可以含有任何之摻雜物(Dopant)，n 型不純物中可使用矽(Si)、鍺(Ge)、硒(Se)、碲(Te)、碳(C)等。而 p 型不純物則可使用鎂(Mg)、鋅(Zn)、鈹(Be)、鈣(Ca)、鍶(Sr)、鋇(Ba)等。另外，摻雜 p 型不純物後，不一定需要將三族氮化物系化合物半導體以電子線照射、電漿照射或以鍋爐等進行加熱。

三族氮化物系化合物半導體層由 MOCVD(有機金屬氣相磊晶成長)法所形成，但沒有必要將構成元件之所有半導體層以 MOCVD 法形成，亦可併用分子線結晶成長法(MBE 法)、氫化物

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氣相磊晶法(HVPE 法)、濺鍍(Sputter)法、離子電鍍(Ion Plating)法等。

發光元件之構成可使用以下幾種構造：具有 MIS 接合、PIN 接合或 pn 接合之同質構造，異質(hetero)構造或雙異質(double-hetero)構造等。發光層可採用量子井構造(單一量子井構造或多重量子井構造)。該三族氮化物系化合物半導體之發光元件可利用以下兩種方式：(1)朝上(Face UP)方式：將光之主要受發光方向(電極方向)朝光裝置之光軸方向，(2)覆晶方式：將光之主要受發光方向朝向與光裝置之光軸方向相反方向，利用反射光。

三族氮化物系化合物半導體元件之磊晶成長溫度為 1050℃左右，而 GaAs 系半導體元件之磊晶成長溫度之耐熱溫度為 600℃以上，兩者均因為使用低融點剝離而可以在不受熱之不良影響之狀況下進行加工。

(無機材料基板)

本發明之光裝置之前述說明中之光學元件係被裝載於無機材料基板上，而無機材料基板之基礎材料及形狀可因應光裝置之用途而進行適當之選擇，亦可使用例如 AlN、Al_2O_3、含有玻璃成分之 Al_2O_3 等矩形板狀之材料。

基板中至少其表面是由上述基礎材料所形成即可，例如可使用中心部份以 Al 或 Al 合金所形成、表面則以 AlN 包圍之方式所形成之基板。

(金屬圖案)

無機材料基板上形成有第 1 金屬圖案及第 2 金屬圖案。第 1 金屬圖案是將光學元件之各電極與外部電路進行電性結合，對光學元件進行電力之傳送；亦即，光學元件為發光元件時，外部電路會將電力施加至光學元件，而光學元件為受光元件時，光學電子所產生之電力會被取出至外部電路。

第 2 金屬圖案具有將無機系之密封構件安定地接著至無機材料機板上之接著層之功能；密封構件是以將光學元件包圍之形態

被配置，當第 2 金屬圖案亦以將裝載有光學元件之第 1 金屬圖案包圍之形態被配置時，可將介於密封構件與無機材料基板間之第 2 金屬材料之面積極大化，且第 2 金屬圖案不限定於是連續體，亦可以是非連續體。

第 1 金屬圖案與第 2 金屬圖案可以是連續之形態，若第 1 金屬圖案與第 2 金屬圖案為絕緣，藉由獨立地施加電壓，可對各自功能最適當之材料進行電場電鍍。

金屬層具有將光進行反射之功能，以第 1 金屬圖案及第 2 金屬圖案將光學元件包圍時，可在不漏失光學元件之光之情況下進行反射，提高光之取出效率。例如，由黑色 AlN 構成之基板會吸收光學元件發出之光，而由 Al_2O_3 構成之基板又會讓光學元件發出之光透過，因此利用金屬圖案將光學元件包圍之方式可讓光學元件發出之光有效率地向外部反射。

為提高光之反射效率，在儘可能地靠近光學元件處所形成之第 1 金屬圖案之表面最好是 Ag 等高反射率之金屬層。

第 1 金屬圖案之形成材料方面，其表面層必須與將圖案與光學元件結合之結合材料能夠合適，例如使用金凸塊做為結合材料時，第 1 金屬圖案之表面層以 Au 或 Ag 來形成；從提高該表面層之外之層之生產性之觀點來看，以與第 2 金屬圖案共通之材料來形成較佳。

將光學元件與基板結合之結合材料除了上述之金凸塊，亦可使用銲錫凸塊或銲錫電鍍等共晶材料。

Ag 層具有高度之光反射率，在光學元件之週邊部位部分地形成較佳。

第 2 金屬圖案之形成材料可因應密封構件之材質及無機材料基板之材料，適當選擇與該等結合性佳之材料，且金屬材料亦可以是該等之多層構造。例如可採用以下材料做為金屬圖案之形成材料：W、W\Ni(於 W 上層積 Ni)、W\Ni\Ag(於 W 上順次層積 Ni 與 Ag)、銅箔(與含有玻璃成分之 Al_2O_3 基板間透過氧化物而獲得

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接著強度，該基板之熱膨脹係數接近 13×10^{-6}(1/℃)之無機系密封構件)等。

此時，W 層因加熱之故，會以楔型狀進入密封構件或基板之無機材料中，然後於兩者間形成一強固之結合。於 W 層上形成 Ni 層時，Ni 層與密封構件間因加熱而產生化學結合，使兩者獲得強固之結合。

第 2 金屬圖案之表面最好是與軟化狀態之密封構件間有不錯之結合性之材料，該材料可以是 Ni、Cr、Ti、Cu，或者是這些金屬之合金。

將基板表面與密封構件接合之第 2 金屬圖案最好是儘可能大面積地被形成於基板表面上。

於基板表面佔有大面積之第 2 金屬圖案之形成材料方面，其熱膨脹係數最好是介於密封構件(熱膨脹係數：小)及無機材料機板(熱膨脹係數：大)之熱膨脹係數之中間。藉此，可緩和密封構件與無機材料基板之各熱膨脹係數差異；從利用密封構件將光學元件包覆時之高溫狀態冷卻至常溫時，密封構件與無機材料基板會依據各自之熱膨脹係數進行收縮，當兩者之熱膨脹係數差異過大時，基板會變形，或者密封構件會由基板剝離。而當兩者間存在有熱膨脹係數居於兩者之熱膨脹係數中間之第 2 金屬圖案時，可緩和兩者間熱膨脹係數差異所導致之應力。

當密封構件為低融點玻璃，基板為 AlN 時之兩者之熱膨脹係數分別是，低融點玻璃：17.3×10^{-6}/℃，AlN：4.5×10^{-6}/℃。此時，Ni 之熱膨脹係數為 12.8×10^{-6}/℃，居於兩者之間，很適合做為該金屬圖案之形成材料。

從縮小基板之熱變形量之觀點看，基板之光學元件裝載面(表面)之實質上之全面最好形成有該第 2 金屬圖案；再者，基板背面若廣範圍地形成由相同或同種材料所形成之金屬圖案時，可更進一步控制基板之熱變形量，效果更好。

將基板表面之金屬圖案延伸至基板背面時，若基板上形成有

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通孔(Through Hole)，並將金屬圖案之材料通過通孔時，則可連結基板表面之圖案及基板背面之圖案。由於電端子從裝載有光學元件之面被拉出至背面，因此並不需要在基板之裝載有光學元件之面，特別設置一沒有被為了電端子之光學元件之密封構件所覆蓋之地方，因此可選擇量產性佳之材料。此時基板若無貫通孔，則裝載有光學元件之面之光學元件之密封構件並不會露出至背面。另外，於光學元件之裝載位置形成該通孔時，光學元件之熱會透過通孔內之金屬圖案材料釋放至外部，因此放熱效率會提高，特別適合發熱量高之三族氮化物系化合物半導體發光元件。

第 1 及第 2 金屬圖案之形成方式並未有特定限制，實施例中是於無機材料基板上實施鎢膠之網板印刷，之後燒烤，將 W 之金屬圖案形成於無機材料基板上。其次於 W 層上 Ni，形成由 W\Ni 所構成之金屬圖案，之後加熱處理；W\Ni\Ag 則是於 Ni 層上再鍍銀。

上述金屬層是以濺鍍或其他眾所皆知之方法形成。

至於不甚要求複雜、正確之圖案形狀之基板背面，亦可使用銅箔般之金屬薄膜。

(密封構件)

無機系密封構件對光學元件之受發光波長呈現透明，雖然只要是保護光學元件之材料的話，即不做特別的限制，但考慮到光學元件之耐熱溫度為 600℃，最好是採用具有較其還低之融點(軟化點)之低融點玻璃較佳。

該低融點玻璃除了鉛玻璃或硫族元素(Chalcogen)化物玻璃外，亦可使用 SiO_2-Nb_2O_5 系、B_2O_3-F 系、P_2O_5-F 系、P_2O_5-ZnO 系、SiO_2-B_2O_3-La_2O_3 或 SiO_2-B_2O_3 系。上述低融點玻璃均可於 350~600℃ 中熱壓成形。

亦可將螢光材料散佈於第 1 密封構件中，該螢光材料使用無機系螢光粉，可將之混合於低融點玻璃中。另外，亦可將希土類離子摻雜於低融點玻璃中，使其產生螢光。將發光元件與螢光材

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料適當組合後，可獲得白光等任意顏色之光。

此密封構件與光學元件之組合中，密封構件之阿貝數在 40 以下、折射率在 1.6 以上、且光學元件之受發光波長在 546.1nm(Na 之 e 線之波長)之條件較佳；亦即，以在高屈折材料內發光之光之外部量子效率來說，相對於發光波長之密封材料之折射率愈高愈好。光學材料之折射率由 Na 之 d 線來定義，一般波長愈短，其折射率愈高，而相對於波長之折射率之變化程度則由阿貝數來表示。特別是，本發明除了可防止以往在樹脂密封時會成為問題之短波長發光之發光元件中，因為選擇了 Na 之 d 線中高折射率、相對於波長之折射率變化大之材料，使樹脂變黃、導致光輸出降低之問題外，在實質上還可達成以相對於短波長有高折射率之材料進行密封，獲得較高之外部量子效率。

具有該光學特性之低融點玻璃可以是 SiO_2-Nb_2O_5 系玻璃，其中又以 SiO_2-Nb_2O_5-Na_2O 玻璃較佳。

將板狀之低融點玻璃所構成之密封構件重疊於光學元件上，並將之加熱、使其軟化，之後即可利用密封構件將發光元件元件圍繞。為使密封構件與光學元件間不會有空氣混入，該加熱最好是於減壓環境下進行。藉由該加熱，低融點玻璃與金屬圖案之界面間會產生化學反應，使兩者能強固地接著。

可在重疊於光學元件上之軟化狀態之密封構件上形成凹凸構造，例如沿著無機材料基板之分割線，於密封構件上設置凹部(較薄部)時，較容易進行分割作業；另外，密封構件上，對應晶粒之凸部與沿著分割線之凹部處被形成細格子狀，藉此，熱變形不會相當於形成凹凸構造前之板狀大小，而會相當於細格子狀之大小，因此可降低密封構件之熱變形；即使密封構件與基板間有較大之熱膨脹係數差異，基板與密封構件間亦不容易發生剝離之情形，可緩和基板彎曲之問題。

將密封構件之凸部做成凸透鏡狀時，可將發光元件發出之光朝光軸方向集中，並可將外部之光朝受光元件處集中；此時，密

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封構件之材料最好是使用高折射率之材料。

將軟化狀態之密封構件與光學元件貼合時，最好是於減壓狀態下進行，因為可防止空氣被封閉於密封構件內；密封構件之凹凸構造可以在將密封構件與光學元件貼合後，密封構件在維持軟化狀態下，或再加熱、使密封構件軟化後之時機，以熱壓方式形成。

以下說明本發明之實施例。

(第 12 實施例)

此實施例之光學元件使用的是圖 65 所示之覆晶型三族氮化物系化合物半導體發光元件 3010，此發光元件釋放出藍色系之光。

發光元件 3010 各層之規格如下：

層別	組成
p 型層 3015	p-GaN：Mg
包含發光層之層 3014	包含 InGaN 層
n 型層 3013	n-GaN：Si
緩衝層 3012	AlN
基板 3011	藍寶石

將摻雜 n 型不純物之矽(Si)之由 GaN 所構成之 n 型層 3013 透過緩衝層 3012，形成於基板 3011 上。此時，基板 3011 使用的是藍寶石，但不限於此，亦可使用藍寶石，尖晶石、碳化矽、氧化鋅、氧化鎂、氧化錳、硼化鋯、三族氮化物系化合物半導體單結晶等。再者，緩衝層是使用 AlN 以 MOCVD 法所形成，但不限於此，亦可使用 GaN、InN、AlGaN、InGaN 及 AlInGaN 為材料，以及分子線結晶成長法(MBE 法)、氫化物氣相磊晶法(HVPE 法)、濺鍍(Sputter)法、離子電鍍(Ion Plating)法等。將三族氮化物系化合物半導體做為基板時，亦可省略該緩衝層。

半導體元件形成後，可視必要將基板及緩衝層除去。

此時之 n 型層 3013 是由 GaN 所形成，但亦可使用 AlGaN、

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InGaN 或 AlInGaN。

另外，n 型層 3013 摻雜有 n 型不純物-矽，但亦可摻雜 Ge、Sc、Te、C 等做為 n 型不純物。

包含發光層之層 3014 亦可以包含量子井構造(多重量子井構造或單一量子井構造)，而發光元件之構造可以是單異質(Single-Hetero)型、雙異質(Double-Hetero)型及同質接合等。

包含發光層之層 3014 之部分，其 p 型層 3015 側可包含摻雜有 Mg 等之能隙(Band Gap)較寬之三族氮化物系化合物半導體層，這是因為其可有效地防止被注入至包含發光層之層 3014 中之電子擴散至 p 型層之情形。

包含發光層之層 3014 上形成有 p 型層 3015，該 p 型層 3015 由摻雜有做為 p 型不純物-Mg 之 GaN 所構成，該 p 型層 1015 可以是 AlGaN、InGaN 或 InAlGaN，而 p 型不純物亦可使用 Zn、Be、Ca、Sr、Ba。導入 p 型不純物後，可使用電子線照射、以鍋爐加熱或電漿照射等眾知之方法來降低電阻。上述構成之發光元件中，各三族氮化物系化合物半導體可利用 MOCVD、以一般條件形成，亦可利用分子線結晶成長法(MBE 法)、氫化物氣相磊晶法(HVPE 法)、濺鍍(Sputter)法、離子電鍍(Ion Plating)法等。

n 電極 3018 是由 Al 與 V 之 2 層所構成，是於 p 型層 3015 形成後，於將 p 型層 3015、包含發光層之層 3014 及 n 型層之部分利用蝕刻去除後露出表面之 n 型層 3013 上以蒸著方式所形成。

p 電極 3016 以蒸著方式層積於 p 型層 3015 上。藉上述步驟將各層、各電極形成之後，接下來是各晶粒(Chip)之切割步驟。

其次，準備裝載有該發光元件 3010 之無機材料基板。

實施例之無機材料基板 3021 之基礎材料為 AlN，其上底面則形成有金屬圖案 3023、3024；其中，如圖 66 所示，上方圖案 3023 由第 1 金屬圖案 3025n、3025p 及第 2 金屬圖案 3026 所構成；第 1 金屬圖案 3025n 透過金凸塊 3027 與光學元件 3010 之 n 電極 3018 連結，第 1 金屬圖案 3025p 則透過金凸塊 3028 與光學元件之 p 電

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極 3016 連結。如圖 67 所示，第 1 金屬圖案 3025n 透過設置於無機材料基板 3021 之基礎材料之通孔 3031，與基板背面之金屬圖案 3024n 有電性之結合；同樣的，第 1 金屬圖案 3025p 透過通孔 3032，與基板背面之金屬圖案 3024p 有電性之結合。如圖 68(圖 67 之重要部位放大圖)，各通孔 3031、3032 中將銅(Cu)利用電鍍法填充進去。

第 2 金屬圖案 3026 以遠離、並環繞第 1 金屬圖案 3025n、3025p 之領域處被形成。

如圖 69 所示，背面側之金屬圖案 3024n 及 3024p 儘可能形成大面積較佳，如此，將熱膨脹係數在密封構件與基板中間之金屬材料所構成之大面積圖案與基板 3021 背面結合時，可將經過熱處理之基板 3021 之變形量儘量拉近密封構件 3029 之變形量；如此，可確實防止基板 3021 之彎曲、或密封構件與基板間之剝離等。

各金屬圖案之形成方式如下：首先，於以網板印刷方式在形成有貫通孔之燒烤前之無機材料基板 3021 之兩面、及形成有通孔之貫通孔處塗布鎢膠，之後以超過 1500℃之溫度燒烤 AlN 基板，將鎢膠燒印至基板 3021；藉此，鎢與 AlN 基板會強固地結合，而該鎢亦可以使用濺鍍(SPUTTERING)的方式形成。另外，亦可使用 Mo 等高融點金屬取代鎢。

其次，於 W 圖案上將 Ni 電鍍上去，再以 700℃加熱，使 Ni 與 W 產生反應，藉此使金屬圖案強固地接合在 AlN 基板 3021 上。

Ni 與由無機系透過性材料所構成之密封構件產生極強之化學結合，且軟化狀態之密封構件之無機系材料與 Ni 有良好之結合性，該密封構件之材料與第 2 電極圖案有全面性接觸，可防止氣泡之產生，且兩者間有高度之結合力。

第 1 金屬圖案 3025n、3025p 上，最好是可藉由 Ni 層上之金凸塊進行良好的接合，且形成有高反射率之 Ag 層；另外，若要於發光元件之底面形成反射面時，僅需考慮金凸塊之接合性，例如於藍光之發光元件中，亦可於 Ni 層上形成 Au 層。

第 1 金屬圖案 3025n、3025p 之正下方形成通孔 3031、3032，因此可將光學元件 10 之熱有效率地透過該通孔內之金屬材料向外部(金屬圖案 3021 之背面)釋放。

其次，如圖 67 所示，發光元件 3010 藉由金凸塊 3027、3028 被裝載於規定之位置；另外，凸塊 3027 與發光元件 3010 之 n 電極 3018 有連結，而凸塊 3028 則與發光元件 3010 之 p 電極 3016 有連結。如圖 66 之狀態，發光元件 3010 被第 1 金屬圖案 3025n 及 3025p 所包圍。

其次，如圖 67 所示，將密封構件之板狀低融點玻璃重疊於基板 3021 之表面，然後於減壓環境中進行加熱、融著，針對發光元件 3010 進行密封。藉此，金屬圖案表面之 Ni 會透過 Ni 表面之氧化物與低融點玻璃 3039 產生化學性之強固結合，並可防止密封時殘留氣泡之發生。

板狀之低融點玻璃在軟化狀態時，最好進行熱壓加工、形成凹凸構造；密封構件 3039 之凹部與基板 3021 之分割線 3037(Notch)一致時，基板之分割作業較容易進行；密封構件 3039 之凹部為透鏡(Lens)形狀時，可提高光之取出效率。

上述一連串之製造步驟中，發光元件 3010 與第 1 金屬圖案 3025n、3025p 間經由加工時之溫度，兩者透過高融點金凸塊 3027、3028 進行連結，而金凸塊並不因密封溫度而軟化。因此，密封作業中，即使發光元件受力，發光元件 3010 亦不會從規定之位置處偏移；另外，採用覆晶型發光元件 3010 時，由於可省略接合線，因此機械性上較安定，可以說相當適合該構成之光裝置之量產步驟。

再者，佔據金屬圖案之膜厚之大部分之 Ni 層之熱膨脹係數為 $12.8\times10^{-6}/℃$，為 AlN 之熱膨脹係數($4.5\times10^{-6}/℃$)與低融點玻璃 303039 之熱膨脹係數($17.3\times10^{-6}/℃$)的中間值。

無機系密封構件 3039 與無機材料基板 3021 間存在有金屬圖案時，密封構件 3039 與基板 3021 間不僅可強固地結合，亦可緩

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和起因於密封構件 3039 與基板 3021 之熱膨脹係數不同所導致之應力，因此可確實防止基板 3021 發生彎曲或碎裂，或密封構件 3039 與基板 3021 間發生剝離之情形。最後，沿著分割線 3037 將基板 3021 進行分割，而獲得實施例之光裝置。

圖 70 至圖 73 是本實施例之變形例之狀態，圖 70 至圖 73 當中，與圖 22 相同要素之部分則附加相同之符號、省略說明。

圖 69 之光裝置中，第 2 金屬圖案 3041 為矩行之環狀。

圖 70 之光裝置中，第 2 金屬圖案 43 為非連續體。

圖 72 之例子中，覆晶型發光元件之基板是以 GaN 基板 3011a 或 SiC 基板取代藍寶石基板；該元件用基板較藍寶石基板有較高之折射率，將之與高折射率之密封構件(低融點玻璃)組合時，可提高光之取出效率。

將 GaN 基板 3011a 之周圍部份進行研磨時，可更加提高光學元件 3010 之光取出效率。

另外，如圖 72 所示，無機材料基板 3051 之基礎材料採用的是較 AlN 之熱膨脹係數大、價廉之 Al_2O_3(熱膨脹係數：6.7×10^{-6}/℃)。

如圖 73 之例子當中，無機材料基板 3061 之基礎材料使用的是含有玻璃成分之 Al_2O_3，並將銅箔接著於基板 3061 全面，以電鍍法將銅填充於貫通孔 3031 及 3032 內。以 1000℃將該無機材料基板 3061 進行加熱時，Cu 與 Al_2O_3 會產生化學結合；於含有玻璃成分之 Al_2O_3 基板之背面廣範圍地形成與玻璃有相同熱膨脹係數之 Cu 層時，可防止基板之彎曲或密封構件與基板間之剝離之問題發生。

第 1 金屬圖案與第 2 金屬圖案為同一基礎材料(銅箔)，並僅在裝載有發光元件之區域-3025n、3025p 處鍍上 Ag 或 Au；此作業僅需將第 2 金屬圖案之區域罩(Masking)起來，即可容易地形成。

另外，亦可於基礎材料-銅箔上鍍鎳，將之當做藍光發光元件之第 2 金屬圖案之反射層。如此，第 1 金屬圖案 3025n、3025p 與第 2 金屬圖案 3026 間即使不是分離之狀態亦沒有問題。

(第 13 實施形態)

圖 74 是本實施例之光裝置，本實施例中之發光元件 3100 是於上下方具有電極之形態，因此需要接合線 3101。

由 AlN 所構成之無機材料基板 3110 上形成有通孔 3111，並利用電鍍法將 Cu 填充於該通孔 3111 中。基板 3110 之兩面形成有大面積之由 W/Ni 所形成之金屬圖案，該金屬圖案之形成方法與實施例 12 相同。

為提高熱之釋出效率，於通孔 3111 之第 1 金屬圖案 3113a 上裝載發光元件 3100 之其中之一之電極，並由另一電極處將接合線 3101 拉出，然後將之接合在第 2 金屬圖案 3113 上。

另外，準備由低融點玻璃所構成之板狀之間隔片 (Spacer)3120，該間隔片 3120 上形成有讓發光元件 3100 及接合線 3101 通過之孔穴，並可不受到發光元件及連線之干擾地將間隔片 3120 重疊於基板 3110 上(如圖 74 之狀態)，並於該狀態下，安裝由低融點玻璃所構成之密封構件 3130；接合線 3101 雖有可能因為該密封構件之材質而發生變形之可能，但該變形可被間隔片 3120 所控制，因此可防止接合線 3101 之斷線或短路於未然。另外，為保護接合線 3101，最好將間隔片 3120 繞至接合線 3101 之下方。

以下詳細說明圖 75 至圖 83 所示之實施形態。

(發光元件)

發光元件包含發光二極體、雷射二極體及其他發光元件及受光元件。發光元件之受發光波長不侷限於特定波長，亦可使用於紫外光至綠光之範圍間有效之三族氮化合物半導體元件，或於紅光有效之 GaAs 系半導體元件。此外，亦可使用 SiC、AlInGaP 等所形成之發光元件。

上文已提及具有絕緣性基板之三族氮化物系化合物半導體發光元件會有散熱之問題一事，將該發光元件做為白色光源時則更加要求高輸出。

三族氮化物系化合物半導體一般以 AlxGaYIn1-X-YN(0<

X≦1、0≦Y≦1、0≦X+Y≦1)來表示。其中含有 Al 的有 2 元系之 AlN，3 元系之 AlxGa1-xN 及 AlxIn1-xN(其中，0<X<1)。三族氮化物系化合物半導體及 GaN 中，三族元素中至少有一部分可以被置換為硼(B)、鉈(Tl)等。另外，氮(N)之一部分亦可置換為磷(P)、砷(As)、銻(Sb)、鉍(Bi)等。

另外，三族氮化物系化合物半導體可以含有任何之摻雜物(Dopant)，n 型不純物中可使用矽(Si)、鍺(Ge)、硒(Se)、碲(Te)、碳(C)等。而 p 型不純物則可使用鎂(Mg)、鋅(Zn)、鈹(Be)、鈣(Ca)、鍶(Sr)、鋇(Ba)等。另外，摻雜 p 型不純物後，不一定需要將三族氮化物系化合物半導體以電子線照射、電漿照射或以鍋爐等進行加熱。

三族氮化物系化合物半導體層由 MOCVD(有機金屬氣相磊晶成長)法所形成，但沒有必要將構成元件之所有半導體層以 MOCVD 法形成，亦可併用分子線結晶成長法(MBE 法)、氫化物氣相磊晶法(HVPE 法)、濺鍍(Sputter)法、離子電鍍(Ion Plating)法等。

發光元件之構成可使用以下幾種構造：具有 MIS 接合、PIN 接合或 pn 接合之同質構造，異質(hetero)構造或雙異質(double-hetero)構造等。發光層可採用量子井構造(單一量子井構造或多重量子井構造)。該三族氮化物系化合物半導體之發光元件可利用以下兩種方式：(1)朝上(Face UP)方式：將光之主要受發光方向朝光裝置之光軸方向，(2)覆晶方式：將光之主要受發光方向朝向與光裝置之光軸方向相反方向，利用反射光。

(次裝載基台：Sub Mount)

次裝載基台之基礎材料若為熱傳導性高之材料，則可因應發光裝置之用途進行適當之選擇，例如 AlN、Al_2O_3、SiC、Si_3N_4、Si 等無機材料。

形成次裝載基台之無機材料之熱膨脹係數介於發光元件之半導體材料與導線架之金屬材料之間，因此即使於發光裝置之製程

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中經過高熱(例如將次裝載基台銲接於第 1 及第 2 導線架時)，亦可緩和發光元件與導線架間之熱膨脹係數差所產生之應力。

次裝載基台之形狀方面，主要是能將其一端設置於形成於第 1 導線架之第 1 凹部、另一端能設置於形成於第 2 導線架之第 2 凹部之形狀即可。

採用覆晶型發光元件時，由於可省略連線，因此可將大電流施加至發光元件處，不僅能使發光元件產生高亮度，亦可將熱有效率地釋出。另外，由於可省略連線，因此可提高發光裝置之耐衝擊性。

取代連線，本實施例於次裝載基台上形成有通孔或側面金屬(SIDE METAL)等配線圖案，藉由該配線圖案，裝載於次裝載基台上之發光元件之各電極與第 1 導線架及第 2 導線架間有電性結合。金屬圖案之形成材料於選擇時，必須注意其表面層必須適合於將圖案與光學元件結合之結合材料；例如，使用金凸塊做為結合材料時，金屬圖案之表面層以 Au 或 Ag 來形成。將發光元件與次裝載基台之配線圖案結合之結合材料除了上述之金凸塊之外，亦可使用銲錫凸塊或電鍍銲錫等共晶材料。

(第 1 導線架、第 2 導線架)

第 1 導線架之其中一端形成有地第 1 凹部，第 2 導線架之其中一端形成有第 2 凹部；第 1 凹部及第 2 凹部可利用以下方式形成：分別針對第 1 及第 2 導線架之厚度方向，以切削溝槽或蝕刻之方式形成；另外，亦可針對第 1 及第 2 導線架之材料進行熱壓，以分別形成第 1 及第 2 凹部；另外，亦可於第 1 及第 2 導線架之表面設置凸部，將被該凸部包圍之部分做為凹部。

該凹部為次裝載基台之承座，其形狀及深度可因應次裝載基台而進行適當之設計。

將次裝載基台之一端安裝至該第 1 凹部中，再將另一端安裝至第 2 凹部，之後再以金屬之共晶材料所形成之銲錫(例如：Pb-Sn、Au-Sn)或銀膠將次裝載基台及第 1 與第 2 導線架進行機械

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性之固定。

將次裝載基台及第 1 及第 2 凹部周壁間之空隙(Margin)縮小，例如該次裝載基台及第 1 及第 2 凹部之間實質上處於結合狀態時，次裝載基台之安裝位置會很穩定，並可防止發光元件之位置偏移的情形發生；所以，利用凸透鏡狀之密封構件將發光元件進行密封時之配光特性將很穩定。

另外，在被安裝至第 1 凹部與第 2 凹部之狀態下，當次裝載基台與第 1 及第 2 導線架實質上為同一高度時，能比較輕易地控制從發光元件朝側面所放出之光，可提高光之取出效率。

再者，當次裝載基台與第 1 及第 2 導線架實質上為同一高度，且次裝載基台與第 1 及第 2 導線架間之空隙縮小(緊密結合之狀態)時，亦即兩者實質上處於同一平面時，導線架之反射率會提高。

以下說明本發明之實施例。

發光元件 10 是三族氮化物系化合物半導體發光元件，圖 75 是其構成之剖面圖；如圖 75 所示，發光元件 4010 是於藍寶石基板上，將多層三族氮化物系化合物半導體層積上去所構成。發光元件 4010 各層之規格如下：

層別	組成
p 型層 4015	p-GaN：Mg
包含發光層之層 4014	包含 InGaN 層
n 型層 4013	n-GaN：Si
緩衝層 4012	AlN
基板 11	藍寶石

將摻雜 n 型不純物之矽(Si)之由 GaN 所構成之 n 型層 4013 透過緩衝層 4012，形成於基板 4011 上。此時，基板 4011 使用的是藍寶石，但不限於此，亦可使用藍寶石，尖晶石、碳化矽、氧化鋅、氧化鎂、氧化錳、硼化鋯、三族氮化物系化合物半導體單結晶等。再者，緩衝層是使用 AlN 以 MOCVD 法所形成，但不限於此，亦可使用 GaN、InN、AlGaN、InGaN 及 AlInGaN 為材料，以

及分子線結晶成長法(MBE 法)、氫化物氣相磊晶法(HVPE 法)、濺鍍(Sputter)法、離子電鍍(Ion Plating)法、電子浴(Electronic Shower)法等。將三族氮化物系化合物半導體做為基板時，亦可省略該緩衝層。

半導體元件形成後，可視必要將基板及緩衝層除去。

此時之 n 型層 4013 是由 GaN 所形成，但亦可使用 AlGaN、InGaN 或 AlInGaN。

另外，n 型層 4013 摻雜有 n 型不純物-矽，但亦可摻雜 Ge、Se、Te、C 等做為 n 型不純物。

N 型半導體層 4013 可以是由(1)包含發光層之層 4014 之低電子濃度 n 層，及(2)緩衝層 12 之高電子濃度 n+層所構成之兩層構造。

包含發光層之層 4014 亦可以包含量子井構造(多重量子井構造或單一量子井構造)，而發光元件之構造可以是單異質(Single-Hetero)型、雙異質(Double-Hetero)型及同質接合等。

包含發光層之層 4014 之部分，其 p 型層 4015 側可包含摻雜有 Mg 等能隙(Band Gap)較寬之三族氮化物系化合物半導體層，這是因為其可有效地防止被注入至包含發光層之層 4014 中之電子擴散至 p 型層 4015 之情形。

包含發光層之層 4014 上形成有 p 型層 4015，該 p 型層 4015 由摻雜有做為 p 型不純物-Mg 之 GaN 所構成，該 p 型層 4015 可以是 AlGaN、InGaN 或 InAlGaN，而 p 型不純物亦可使用 Zn、Be、Ca、Sr、Ba。

再者，p 型半導體層 4015 可以是由(1)包含發光層之層 4014 之低電洞濃度 p－層，及(2)電極側之高電洞濃度 p+層所構成之兩層構造。

上述構成之發光二極體中，各三族氮化物系化合物半導體可利用 MOCVD、以一般條件形成，亦可利用分子線結晶成長法(MBE 法)、氫化物氣相磊晶法(HVPE 法)、濺鍍(Sputter)法、離子

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電鍍(Ion Plating)法、電子浴法等。

n 電極 4018 是由 Al 與 V 之 2 層所構成，是於 p 型半導體層 4015 形成後，於將 p 型層 4015、包含發光層之層 4014 及 n 型半導體層 4013 之一部分利用蝕刻法去除後，露出表面之 n 型層 4013 上以蒸著方式所形成。

P 電極 4016 是包含金之膜狀電極，以蒸著之方式層積於 p 型半導體層 4015 上。

藉上述步驟將各半導體層、各電極形成之後，接下來是各晶粒(Chip)之切割步驟。

如圖 76A 所示，次裝載基台 4020 是由 AlN 所構成之絕緣性之板狀構件，其上方表面形成有表面電極 4021、4022，背面則形成有背面電極 4023、4024。該等電極 4021、4022、4023、4024 是依鉭、鎳及金之順序層積而成，並利用通孔 4025(填充有導電性金屬)進行導通。

本實施例之次裝載基台 4020 是藉由通孔將表面電極 4021、4022 及背面電極 4023、4024 導通；亦可於次裝載基台 4020 側面形成金屬層(側面金屬層)，將兩者進行導通。

發光元件 4010 之 n 電極是透過金凸塊 4031 與表面電極 4021 間有電連接，而 p 電極是透過金凸塊 4032 與表面電極 4022 有電性之連接，亦可用銲錫球(Solder Ball)取代凸塊。

第 1 導線架 4041 與第 2 導線架 4042 之端緣處分別有以切削方式所形成之溝槽 4043、4044；各溝槽 4043、4044 之形狀係次裝載基台 4020 以兩端以幾乎沒有空隙的形態被嵌入；藉此，次裝載基台 4020 之位置會被固定；第 1 導線架 4041 及第 2 導線架 4042 與次裝載基台 4020 間是以銲錫(Sn-Ag 系之錫膏)4035 進行固定。

本實施例中，為使第 1 及第 2 導線架 4041、4042 之表面能與次裝載基台 4020 之表面處於同一高度，而調整溝槽 4043 及溝槽 4044 之深度；藉此能比較輕易地控制從發光元件 4010 所放出之光(特別是釋放至側邊之光)。

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另外，亦可採用將溝槽深度加深，利用溝槽側壁將發光元件4010所放出之光進行反射之構造。

之後，如圖77所示，以密封構件4051將發光元件4010包覆，形成實施例之發光裝置4050；利用將螢光材料混合於密封構件4051中之方式，可獲得白色等任意之發光顏色。密封構件4051可由能讓發光元件發出之光透過之材料中，因應發光裝置之用途進行適當之選擇；例如，亦可利用環氧樹脂、聚醯亞胺(Poly 亞胺)、彈性體(Elastomer)等有機材料及低熔點玻璃等無機材料來形成。本實施例是利用能承受回銲爐製程之亞胺系樹脂形成密封樹脂4051，之後將第1及第2導線架4041、4042焊接至次裝載基台。

圖78顯示的是其他型態之密封構件4053，該例子中，第1及第2導線架4041、4042之邊緣及次裝載基台4020亦被密封樹脂所包覆。該密封構件4053在將次裝載基台4020往第1及第2導線架4041、4042處固定後，藉由模具成形之方式形成，成形材料可使用環氧樹脂。

藉由以上述方式構成之本實施例之發光裝置4050，發光元件4010所產生之熱可透過次裝載基台4020，幾乎是均等地傳達至第1及第2導線架4041、4042；因此，可充分地確保熱傳達路徑，提高放熱效率。

另外，次裝載基台4020之位置、亦即發光元件4010之位置係藉由溝槽4043及溝槽4044所規定，因此發光裝置之配光特性會穩定。

以下說明上述實施例之各要素之變形型態。

與圖77至78所示之要素為相同要素時則賦予相同符號、並省略說明。

圖80之例子是將第1導線架4041之溝槽4045縮短，並於第2導線架4042處加長溝槽4046；藉此，第2導線架之4042之構件(溝槽4046之周壁)將位於發光元件4010之正下方；因此，發光元件4010至導線架間之距離會最短，可將發光元件4010所發出

之熱更有效率地發散。

圖 80 之例子中，溝槽 4047 及溝槽 4048 延伸至各導線架 4041、4042 之側面，藉此，可較容易地將次裝載基台 4020 安裝至溝槽 4047 及溝槽 4048 處。

圖 81 之例子中，第 1 導線架 4041 之側面形成有溝槽 4049；誠如此實施例，導線架之溝槽之形成方向及形成位置可任意設置，可因應發光裝置之用途適當地進行選擇。

圖 82 之例子係針對第 1 及第 2 導線架 4041、4042 之前端進行熱壓加工，以形成左側開口之凹部 4061、4062；並可如同圖 76 所示，將次裝載基台安裝至該凹部 4061、4062。

圖 83 之例子係針對第 1 及第 2 導線架 4041、4042 之前端進行熱壓加工，形成左邊開口形狀之凸部 4071、4072；被該凸部 4071、4072 包圍之部分則為凹部 4073、4074；並可如同圖 76 所示，將次裝載基台安裝至該凹部 4073、4074。

圖 84 之是與第 13 實施型態有關之發光裝置之構成之剖面圖，該發光裝置 5010 係由以下部分所構成：(1)做為供電構件之基板 5011，(2)搭載於該基板 5011 上之 LED 元件 5012，(3)以將基板上之 LED 元件 5012 包覆之方式被密封之緩衝層 5013，(4)以將該緩衝層 5013 及基板 5011 上方包覆之方式所形成之密封構件 5014。

基板 5011 具備以下部分：(1)高膨脹係數之陶瓷基板 5011a(絕緣性基板)，(2)於陶瓷基板 5011a 上，以規定之圖案所形成之配線層 5011b、5011c、5011d、5011e，(3)於陶瓷基板 5011a 下方，以規定之圖案所形成之配線層 5011f、5011g，(4)被包覆於配線層 5011c 表面之鍍金膜 5011h，(5)被包覆於配線層 5011d 表面之鍍金膜 5011i，(6)被包覆於配線層 5011f 表面之鍍金膜 5011j，(7)被包覆於配線層 5011g 表面之鍍金膜 5011k，(8)連接配線層 5011b 及配線層 5011f 之通孔 5011lm，(9) 連接配線層 5011d 及配線層 5011g 之通孔 5011m。

陶瓷基板 5011a 可使用例如含有玻璃成分之 Al_2O_3(熱膨脹係

數 13.2×10^{-6}/℃)；配線層 5011b、5011d、5011j、5011g 之功能是可供給電源之電極。另外，配置鍍金膜 5011h、5011i、5011j、5011k 之目的在提高連接性、導電性、耐腐蝕性等；另外，基板 5011 在搭載 LED 元件 5012 之前，需預先於陶瓷基板 5011a 上形成鍍金膜 5011h、5011i、5011j、5011k 以及通孔 5011l、5011m。

LED 元件 12 是以 GaN、AlInGaP 等半導體所構成，其晶粒大小有 0.3x0.3mm(標準尺寸)、1x1mm(大尺寸)等。緩衝層 5013 使用的是矽樹脂，而密封構件可使用好比住田光學玻璃製之「K-PSK100」(熱膨脹係數 11.4×10^{-6}/℃)。

密封構件 5014 使用的是具有透光性、低融點特性之玻璃材料；LED 元件 5012 下方具有電源用之電極 5012a、5012b，該電極 5012a、5012b 被銲接於基板 5011 之規定之配線層上。

以下說明發光裝置 10 之組裝方式。

首先，將電極 5012a、5012b 配置於基板 5011 之配線層 5011c、5011d 上，將 LED 元件 5012 定位，並分別將配線層 5011c 與電極 5012a、配線層 5011d 與電極 5012b 進行銲接。

其次，將液體狀之矽樹脂材料從 LED 元件 5012 中心之正上方滴下，將 LED 元件 5012 之頂面、側面之全面進行層狀之鍍膜，形成緩衝層 5013。

其次，於形成有緩衝層 5013 之狀態下，將基板 5011 及 LED 元件 5002 放置於 150℃左右之環境中，使緩衝層 5013 進行第一次硬化。

其次，利用玻璃材料之密封構件 5014 將緩衝層 5013 之表面及基板 5011 之表面進行密封；密封構件 5014 之密封是使用模具，於規定之溫度環境及加壓之方式，形成如圖 84 般之半圓形；發光裝置 5010 是藉由上述方式所完成。在矽樹脂進行玻璃密封加工之際，會因熱而使得化學結合中斷、SiO_2 化，但不會黑化、不會成為光吸收之要素。

上述構成之發光裝置 5010 中，當配線層 5011f 為 LED 元件

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5012 之陽極(Anode)時，配線層 5011f 會與直流電源(圖示未顯示)之正極(Plus)連接，配線層 5011g 則會與負極(Minus)連接。透過與表滅電極 5108 及 n 型電極 5109 有電連接之凸塊 2，針對 LED 元件施加順向電壓時，LED 元件 5012 內之發光層之電洞(Hole)與電子之載子(Carrier)會再次結合、發光，而光之輸出會透過藍寶石基板 5101，放出至 LED 元件 5012 之外部。幾乎所有的光會穿透密封構件 5014 內部、被釋放至密封構件 5014 外，部分的光會在內部反射後，放出至密封構件 5014 外。

藉由該第 13 實施形態，可獲得以下效果。

(1)以玻璃之密封構件 5014 將整體進行密封時，可減少樹脂密封時成為問題之因變黃、著色導致光之衰減等問題。

(2)於 LED 元件 5012 周圍設置緩衝層 5013 時，可緩和以密封構件 5014 進行密封時所產生之應力，該應力透過高黏度之玻璃材料被賦予至 LED 元件 5012。亦即，因為緩衝層 5013 居於中間，因此 LED 元件 5012 與密封構件 5014 不會直接接觸，可藉緩衝層 5013 吸收熱膨脹、熱收縮所產生之應力。

(3)透過緩衝層 5013 將 LED 元件 5012 進行玻璃密封時，可防止 LED 元件 5012 附近產生碎裂之情形。該緩衝層 5013 之構成對與密封構件 5014 間之接觸面積較大之大尺寸(1mm×1mm)LED 元件 5012 來說特別有效。

(4)以緩衝層 5013 將 LED 元件 5012 包圍時，可防止凸塊 5002 受壓損壞所導致之電極間短路；另外，緩衝層 5013 在控制凸塊形狀崩潰時，可防止玻璃密封時，LED 元件 5012 之光軸傾斜問題之發生。

(5)以分斷晶圓之方式形成 LED 元件 5012 時，被分斷之 LED 元件 5012 之側面會產生細小凹凸，該凹凸對玻璃封裝型發光裝置 5010 來說，其會於 LED 元件 5012 與密封構件 5014 之界面形成應力不均衡之部分，甚至是導致細微碎裂(Micro Crack)之成因。針對此問題，於成為 LED 元件 5012 分斷面之側面設置緩衝層 5021 時，可

防止密封構件 5014 之熱收縮時所發生之細微碎裂。

圖 85 是與第 13 實施形態有關之發光裝置之變形例之剖面圖，該發光裝置 5020 僅於 LED 側面設置緩衝層 5021 是其不同之處。該構成緩和以下兩問題：(1)凸塊 5002 受壓損壞所導致之電極間短路，(2)密封構件 5014 之熱收縮時產生之應力。另外，於 LED 元件 5012 之基板側不設置緩衝層時，於取出 LED 元件 5012 所發出之光時不會受到阻礙。

圖 86 是與第 14 實施形態有關之發光裝置之剖面圖，圖 86 之發光裝置 5030 是朝上型，具備以下部分：(1)做為供電構件之基板 5031，(2)搭載於基板 5031 上之 LED 元件 5032，(3)將 LED 元件 5035 整體包覆、密封之緩衝層 5033，(4)以將該緩衝層 5033 及基板 5031 頂面整體包覆之方式形成之密封構件 5034，(5)將 LED 元件 5032 之電極與基板 5031 上之配線層進行連接之導線 5035a、5035b。

基板 5031 具備以下部分：(1)使用與圖 84 之基板 5011 相同材料之絕緣性基板之陶瓷基板 5031a，(2)於陶瓷基板 5031a 上，以規定之圖案所形成之配線層 5031b、5031c，(3)於陶瓷基板 5031a 下方，與規定之圖案所形成之配線層 5031d、5031e，(4)連接配線層 5031b 及配線層 5031d 之通孔 5031f，(5)連接配線層 5031c 及配線層 5031e 之通孔 5031g。另外，配線層 5031b~5031e 之表面設置有鍍金膜，本圖將該部分省略。

陶瓷基板 5031a 可使用例如含有玻璃成分之 Al_2O_3；配線層 5031b~5031e 之功能是可供給電源之電極。另外，基板 5031 在搭載 LED 元件 5032 之前，需預先於陶瓷基板 5031a 上形成配線層 5031b~5031e 以及通孔 5031f、5031g。密封構件 5034 使用的是具透光性、低融點之特性之玻璃材料。

LED 元件 5032 是利用接著劑等被固定至配線層 5031c 上，LED 元件 5032 上之其中之一之電極(圖示未顯示)與配線層 5031b 間是以導線 5035a 進行連接，LED 元件 5032 上之另一電極(圖示

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未顯示)與配線層 5031c 是以連線 5035b 進行連接。

緩衝層 5033 將 LED 元件 5032 之露出部分及連線 5035a、5035b 包覆。密封構件 5034 將緩衝層 5033 之表面、露出於基板 5031 上之配線層或基板 5031 之露出之一部分包覆、形成半球狀。

以下說明發光裝置 5030 之組裝方式。

首先準備一陶瓷基板 5031a 上已經形成有配線層 5031b~5031e 及通孔 5031f、5031g 之基板 5031，並將 LED 元件 5032 搭載於配線層 5031c 上之規定之位置。

其次，利用連線 5035a、5035b 將 LED 元件 5032 與配線層 5031b、5031c 間接合。

其次，滴下液體狀之矽材料至規定之厚度，將 LED 之露出面及連線 5035a、5035b 包覆。

其次，將 LED 元件 5032 及連線 5035a、5035b 置於 150℃溫度之環境中，使緩衝層 5033 初步硬化，之後於緩衝層 5033 周邊形成以玻璃材料成形之密封構件 5034；至此，發光裝置 5030 即告完成。

該發光裝置 5030 中，當配線層 5031d 為 LED 元件 5032 之陽極(Anode)時，配線層 5031d 會與直流電源(圖示未顯示)之正極(Plus)連接，配線層 5031c 則會與負極(Minus)連接。藉由上述方式通電時，LED 會發光，該光線會從圖示之 LED 元件 5032 之上方射出，而幾乎所有的光會穿透密封構件 5034 內部、被釋放至外部，其餘部分的光會在密封構件 5034 內部反射後，放出至密封構件 5034 外。

第 14 實施形態中，由於在以朝上型方式搭載有 LED 元件 5032 之發光裝置 5030 之 LED 元件 5032 周邊設置有緩衝層 5033，因此不僅可防止於玻璃密封時會發生之連線 5035a、5035b 之變形、壓毀所導致之電極間短路之情形，亦可如同第 1 實施形態般，可防止因密封構件 5034 之高熱膨脹所導致之 LED 元件 5012 附近所發生之碎裂之情形。

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當未設置緩衝層 5033，且玻璃密封加工後之溫度設置較高時，會對 LED 造成損壞，而對溫度有限制；且玻璃密封加工是在玻璃為高黏度之狀態下進行，因此無法避免有外力施加至連線 5035a、5035b，維持連線 5035a、5035b 於所希望之狀態是很困難的事。例如，當連線 5035a 因為玻璃材料之加壓而毀壞時，會產生配線層 5031b 與 5031c 之短路之問題。此時，不僅不會發光，亦會對圖示未顯示之電源造成影響；另外一提，樹脂材料的話則不會產生上述問題。

朝上型之 LED 元件中，其上方金屬構件之連線本身即是一緩衝材，但其一旦被壓毀後，會產生電性短路之問題；因此，即使沒有緩衝材的要素，藉由防止崩潰之產生以預防電性短路之要素即非常重要。

圖 87 是與本發明第 15 實施形態有關之發光裝置之剖面圖，該發光裝置 5040 將次裝載基台 5043 搭載於引線部 5044a、5044b 處，而該次裝載基台搭載有 LED 元件 5041；另外，圖 87 顯示的次裝載基台為非剖面之狀態。

該發光裝置 5040 具備以下部分：(1)於安裝面設置有凸塊 5042 之 LED 元件 5041，(2)搭載有 LED 元件 5041 之次裝載基台 5043，(3)將做為搭載有次裝載基台 5043 之供電構件之引線部 5044a、5044b 及 LED 元件 5041 露出部分等包覆之緩衝層 5045，(4)將緩衝層 5045 及其周圍進行密封之透光性玻璃所形成之密封構件 5046。

次裝載基台 5043 可使用例如高熱傳導之 AlN(氮化鋁)，LED 元件 5041 之安裝面形成有與凸塊 5042 連接之電極 5043a，相反側(導線架側)則形成有以與引線部 5044a、5044b 連接為目的之電極 5043b。為將電極 5043a 與電極 5043b 連接，而於次裝載基台 5043 內設置有通孔 5043c。

引線部 5044a、5044b 是以做為導線架之一部分，從導線架兩側之帶狀部分與內側間保持規定之間隙、且兩引線部為相對方向

之狀態所形成，而 1 個 LED 元件分配有一對引線部。引線部 5044a、5044b 之前端之一部分是以有薄層斷差之方式製作，該斷差部分會裝載次裝載基台 5043。

緩衝層 5045 是以與前述之其他實施形態之緩衝層 5013、5021 及 5033 相同材料及加工方式所形成。

密封構件 5046 與前述其他實施形態相同，使用具有透光性、低融點特性之玻璃材料。

該發光裝置 5040 中，引線部 5044a 為正(+)電源供給端子時，被供給至引線部 5044a 之電流會經過引線部 5044a、電極 5043b 之其中一方、通孔 5043c 之其中一方、電極 5043a 之其中一方及凸塊 5042 之其中一方，流至 LED 元件 5041 之陽極；而由 LED 元件 5041 之陰極流出之電流則經過凸塊之另一方、電極 5043a 之另一方、通孔 5043c 之另一方以及電極 5043b 之另一方，流至引線部 5044b，此時 LED 元件 5041 會發光。

以下說明發光裝置 5040 之組裝方式。

首先準備一預先形成有電極 5043a、5043b 以及通孔 5043c 之次裝載基台 5043，再透過凸塊 5042 將 LED 元件 5041 搭載至次裝載基台之 5043 上之規定位置，如此會與 LED 元件 5041 間有電連接，並達成機械性之固定。

其次，將搭載於次裝載基台 5043 上之 LED 元件 5041 以配合通電方向之方式配置於引線部 5044a、5044b 前端之窪槽中。

其次，滴下液體狀之矽材料至規定之厚度，將 LED5041 之周圍包覆。

其次，將 LED 元件 5032、次裝載基台 5043 及引線部 5044a、5044b 置於 150℃溫度之環境中、使之初步硬化；之後於 LED 元件 5032 周圍形成緩衝層 5045。

將形成密封構件 5045 所需之玻璃片(Glass Sheet)配置於 LED 元件 5041 之上、下方，並於 LED 元件 5041 之上、下方分別配置模具。

其次，於規定之溫度環境中，利用模具進行加壓，使玻璃片成為規定之形狀；至此，發光裝置 5040 算完成。最後，各個發光裝置 5040 會從導線架上、由引線部 5044a、5044b 之另一端被一個一個分割下來。

藉由該第 15 實施形態，在針對搭載於高熱傳導性之次裝載基台 5043 上之 LED 元件 5041 進行玻璃密封時，可藉由緩衝層 5041，防止因熱膨脹係數差所導致之 LED 元件 5041 或次裝載基台 5043 周圍發生碎裂、剝離等情形。

另外，發光裝置 5040 中，亦可將螢光體混合於緩衝層 5045 中；此時，由被 LED 元件 5041 之光所激勵之螢光體所發出之勵起光與 LED 元件 5041 之放射光兩者混合後會產生波常之變換；螢光體可使用例如被 LED 元件 5041 發出之藍光所激勵、而放出黃光之 Ce：Yttrium Aluminum Garnet (釔鋁紅榴石)。

圖 88 是與本發明之第 16 實施形態有關之發光裝置之剖面圖，該發光裝置 5050 之構成是圖 87 之發光裝置 5040 上安裝有放熱構件；其特徵是：於 AlN 等構成之次裝載基台 5052 下方安裝放熱構件 5051，該放熱構件 5051 使用的是銅等具有優良熱傳導性之金屬材料。

發光裝置具有以下部分：(1)做為放熱器之放熱構件 5051，(2)搭載於放熱構件 5051 上之次裝載基台 5052，(3)前端被裝置於次裝載基台 5052 兩端之段差部分之引線部 5053a、5053b，(4)下方具有一對電源供給用之凸塊 5042、被搭載於次裝載基台 5052 上之 LED 元件 5041，(5)將 LED 元件 5041 露出部分包覆之緩衝層 5054，(6)將緩衝層 5054 及周圍密封之由低融點玻璃構成之密封構件 5055。

次裝載基台 5052 兩端之規定範圍經過厚度削薄之加工、以製造段差，該削薄部分載置有引線部 5053a、5053b 之前端部分，該前端部分與配線 5052a、5052b 之側面藉由銲接等方式進行連接。再者，次裝載基台 5052 從頂面至側面處設置有與一對凸塊 5042

接觸之配線圖案 5052a、5052b。

緩衝層 5054 是於 Si 系烷氧基(alkosidc)中混合有螢光體、燒烤後呈多孔質狀態之含有螢光體之 SiO_2，除了能緩衝應力外，亦有變換波長之功能。

誠如第 15 實施形態之說明，螢光體可使用 Ce：Yttrium Aluminum Garnet (鈰鋁紅榴石)。

第 16 實施形態之發光裝置之組裝方式依據第 15 實施形態，此處省略重複之說明；可先完成圖 88 之次裝載基台 5052 上方之部分，之後再以將放熱構件 5051 接著於其下方之方式進行安裝即可。

藉由該 16 實施形態可獲得以下效果。

(1)於次裝載基台 5052 下方設置促進放熱之放熱構件 5051，可將伴隨 LED 元件 5041 點燈所發出之熱，有效率地朝外部發散，可抑制由玻璃材質所形成之密封構件 5055 等之溫度上昇所導致之熱膨脹、熱收縮等之發生，以防止碎裂等情形。

(2)緩衝層 5054 內混合有螢光體，不僅可進行波長之變換，亦可提高光之取出效率。

另外，上述各實施形態中，亦可於基板 5011、5031 或引線部 5044a、5044b、5053a、5053b 之表面形成反射面，提高光之取出效率。

另外，可在密封構件 5014、5034 內之 LED 元件 5012、5032 上方之部分混合部分螢光體，或於緩衝層 5013、5033 內混合波長變換用之螢光體。

另外，使用 TiO_2 系陶瓷材料為緩衝層 5054 之材料時，其折射率具有 2.4 之相當高之數值，因此可提高由 LED 元件 5041 所發出之光之取出效率。

再者，上述各實施形態中，1 個密封構件內配設之 LED 元件數為 1 個，但亦可配設 2 個以上之發光型多晶型之發光裝置。搭載之複數 LED 元件可以是設置多個不同發光色之 LED 元件，亦

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可以是設置多個相同發光色之 LED 發光元件之構成。再者，LED 之驅動形態方面，可以是將多個 LED 元件全部以並聯連接、或以群組為單位之並聯連接，而複數單位之串聯連接或全數串聯之連接亦可。

另外，密封構件 5014 於上述說明中使用的是住田光學玻璃製之「K-PSK100」，但是不限於此，只要是不會對發光元件產生熱之影響，且會在可進行加工密封之溫度下軟化之玻璃即可。

另外，密封構件 5014、5034、5046、5055 之形狀於說明中為半球狀之構成，但本發明並不限定於圖示之形狀，可以是沒有凸透鏡之形狀、多角形、圓柱形等任意之形狀。

再者，密封構件 5014、5034、5046、5055 於成形之際，並不限定於使用玻璃片之加壓成形方式，亦可使用例如將溶融玻璃供給至 LED 元件附近，再以模具加熱成形等其他密封方法。

另外，緩衝層 5054 不限於多孔質，可吸收應力、熱膨脹係數介於 LED 元件與密封玻璃中間等，具有緩衝效果且具有絕緣性、耐熱性之材質亦可。

圖 89 是與本發明第 17 實施形態有關之發光裝置之構成之剖面圖，該發光裝置 6010 之構成具有以下部分：(1)做為供電構件之基板 6011，(2)電源供給用、具備至少一對由金所構成之凸塊 6012a、6012b 之被搭載於基板 6011 上之 LED 元件 6012，(3)被填充於 LED 元件 6012 下方與基板 6011 間之絕緣層 6013，(4)以覆蓋 LED 元件 6012 及基板 6011 上方之方式所形成之密封構件 6014。

基板 6011 具備以下部分：(1)陶瓷基板 6011a，(2)於陶瓷基板 6011a 上，以規定之圖案所形成之配線層 6011b、6011c、6011d、6011e，(3)於陶瓷基板 6011a 下方，以規定之圖案所形成之配線層 6011f、6011g，(4)被包覆於配線層 6011c 表面之鍍金膜 6011h，(5)被包覆於配線層 6011d 表面之鍍金膜 6011i，(6)被包覆於配線層 6011f 表面之鍍金膜 6011j，(7)被包覆於配線層 6011g 表面之鍍金膜 6011k，(8)連接配線層 6011b 及配線層 6011f 之通孔 6011l，(9)

連接配線層 6011d 及配線層 6011g 之通孔 6011m。

陶瓷基板 6011a 可使用例如含有玻璃成分之 Al_2O_3(熱膨脹係數 13.2×10^{-6}/℃)；配線層 6011c、6011d、6011f、6011g 之功能是可供給電源之電極。另外，配置鍍金膜 6011h、6011i、6011j、6011k 之目的在提高連接性、導電性、耐腐蝕性等；另外，基板 6011 在搭載 LED 元件 6012 之前，需預先於陶瓷基板 6011a 上形成配線層 6011b~6011g，鍍金膜 6011h、6011i、6011j、6011k 以及通孔 6011l、6011m。

LED 元件 6012 是以 GaN、AlInGaP 等半導體所構成，其晶粒大小有 0.3x0.3mm(標準尺寸)、1x1mm(大尺寸)等。LED 元件 6012 下方具有電源用之電極 6012a、6012b，該電極 6012a、6012b 被銲接於基板 6011 之規定之配線層上。

絕緣層 6013 是由矽材料、或鑽石、BN、SiC、或含有 AlN 之粉末之絕緣材所形成。使用矽樹脂為矽材料時，伴隨密封構件 6014 之密封所產生高溫，將使化學結合中斷、成為 SiO_2，發揮具有耐熱性之絕緣體之功能。另外，亦可使用以 Si 系或 Ti 系等烷氧基(alkoside)所形成之陶瓷材料取代以矽樹脂所形成之 SiO_2。另外，鑽石具有高度之熱傳導性，而 BN、SiC、AlN 與鑽石比較，雖然於熱傳導性上較遜色，但是較便宜。另外，鑽石、BN、SiC 為透明或白色，具有光吸收較少之特徵。

密封構件 6014 使用的是具有透光性、低融點特性之玻璃材料，例如可使用住田光學玻璃製之「K-PSK100」(熱膨脹係數 11.4×10^{-6}/℃)。另外，發明者們的實驗中，為獲得陶瓷與玻璃間之良好接合性，陶瓷基板 6011a 與密封構件 6014 需控制成略為相同之熱膨脹係數(熱膨脹係數差在 15%)，本例中之熱膨脹係數比為 0.86。

以下說明發光裝置 6010 之組裝方式。

首先，將金凸塊 6012a、6012b 定位、使其位於配線層 6011c、6011d 上，將 LED 元件 6012 配置於基板 6011 後，以滴下、填充等方式形成絕緣層 6013。

其次，利用玻璃材料之密封構件 6014 將 LED 元件 6012、絕緣層 6013 之露出面及基板 6011 之露出面進行密封；密封構件 6014 之密封是使用模具，於規定之溫度環境中加壓之方式，形成如圖 89 般之半圓形；做為絕緣層 6013 之矽材料會 SiO_2 化，LED 元件 6012 下方及凸塊 6012a、6012b 會被固定，因此可迴避凸塊 6012a、6012b 之變形、凸塊間之短路等。至此，發光裝置 6010 即告完成。

上述構成之發光裝置 6010 中，當配線層 6011f 為 LED 元件 6012 之陽極(Anode)時，配線層 6011f 會與直流電源(圖示未顯示)之正極(Plus)連接，配線層 6011g 則會與負極(Minus)連接。透過與 p 型電極及 n 型電極有電連接之凸塊 6002，針對 LED 元件 6012 施加順向電壓時，LED 元件 6012 內之活性層之電洞與電子之載子會再次結合、發光，而光之輸出會放出至 LED 元件 6012 之外部。幾乎所有的光會穿透密封構件 6014 內部、被釋放至密封構件 6014 外，部分的光會在內部反射後，放出至密封構件 6014 外。

藉由該第 17 實施形態，可獲得以下效果。

(1)以玻璃材質形成之密封構件 6014 將整體進行密封時，可減少樹脂密封時會成為問題之因變黃、著色所導致光之衰減等問題。

(2)於 LED 元件 6012 下方設置具有耐熱性之絕緣層 6013 後，以密封構件 6014 進行密封時，可防止以密封構件 6014 針對凸塊 6012a、6012b 以高熱加壓時，對 LED 元件 6012 產生不良影響之情形。亦即，本發明可防止導因於密封構件 6014 之高熱及高壓而使凸塊 6012a、6012b 產生變形、破損，造成凸塊間短路之問題。

(3)使用鑽石、BN、SiC 或含有 AlN 粉末之絕緣材時，LED 元件 6012 發出之熱可被有效率地釋放，因此可提高放熱性。

圖 90 是與第 18 實施形態有關之發光裝置之構成之剖面圖，該發光裝置 6020 是使用次裝載基台 6022、被搭載於導線架上之金屬引線型態之裝置，其具備以下部分：(1)於安裝面設置有凸塊 6021a、6021b 之 LED 元件 6021，(2)搭載有此 LED 元件 6021 之次裝載基台 6022，(3)搭載有該次裝載基台 6022、做為供電構件之

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引線部 6023a、6023b，(4)填充於引線部 6023a、6023b 及 LED 元件 6021 下方之間之絕緣層 6024，(5)以將絕緣層 6024 之邊緣及包含 LED 元件 6021 表面之引線部 6023a、6023b 之前端進行密封為目的之由透光性玻璃所構成之密封構件 6025。

次裝載基台 6022 可使用例如具高度熱傳導之 AlN(氮化鋁)；與凸塊 6021a 之其中一方連接之配線層 6022a 於其頂面、側面、底面之區域形成一左邊開口之形態，而相反側則有與凸塊 6021b 相連接之配線層 6022b 於其頂面、側面、底面之區域形成一左邊開口之形態。

另外，可視需要，將齊納二極體等電路內藏於次裝載基台 6022 中；又，亦可利用(1)設於其上底面之電極、(2)連通該上下電極之通孔兩者之組合所形成之配線機構取代配線層 6022a、6022b。

引線部 6023a、6023b 由銅或鐵系金屬所構成，是做為圖示未顯示之導線架之一部分，以導線架兩側之帶狀部分與內側間保持規定之間隙、且兩引線部面對面之方式所形成，而 1 個 LED 元件分配有一對引線部。引線部 6023a、6023b 之前端之一部分是以有薄層斷差之方式製作，該斷差部分會配置次裝載基台 6022。

與第 17 實施形態之絕緣層 6013 相同，絕緣層 6024 可以使用矽材料、鑽石或含有 AlN 粉末之絕緣材料；密封構件 6025 於密封進行時會發生化學結合中斷、矽材料成為 SiO_2 之形成過程、及使用鑽石、BN、SiC 或含有 AlN 粉末之絕緣材料時等兩種情況下，其放熱效果與絕緣層 6013 之情況時相同。

與上述實施形態相同，密封構件 6025 使用具透光性、低融點特性之玻璃材料。

該發光裝置 6020 中，引線部 6023a 為正(+)電源供給端子時，被供給至引線部 6023a 之電流會經過引線部 6023a、配線層 6022a、凸塊 6021a，流至 LED 元件 6021 之陽極；而由 LED 元件 6021 之陰極流出之電流則經過凸塊 6021b、配線層 6022b，流至引線部 6023b，此時 LED 元件 6021 會發光。

以下說明發光裝置 6020 之組裝方式。

首先準備一預先形成有配線層 6022a、6022b 之次裝載基台 6022，該次裝載基台 6022 上之規定位置處形成有凸塊 6021a、6021b，並將 LED 元件 6021 搭載至該凸塊上；如此，凸塊 6021a 與配線層 6022a、凸塊 6021b 與配線層 6022b 會有電連接，並達成機械性之固定。

其次，將搭載於次裝載基台 6022 上之 LED 元件 6021 以配合通電方向之方式配置於引線部 6023a、6023b 前端之窪槽中。另外，亦可以是將 LED 元件 6021 搭載至次裝載基台 6022 後，再將次裝載基台 6022 搭載至引線部 6023a、6023b 之順序。

其次，將做為絕緣層 6024 之矽材料填充於 LED 元件 6021 之下方及次裝載基台 6022 之頂面(該填充作業亦可在將次裝載基台 6022 搭載至引線部 6023a、6023b 作業之前)。於該狀態下將之搬入模具中，並將以形成密封構件 6025 為目的之玻璃片(圖示未顯示)配置於 LED 元件 6021 之上方及下方，再以規定之溫度以加壓方式形成半球狀；於密封進行時，矽材會 SiO_2 化、成為絕緣層 6024，並將 LED 元件 6021 下方、凸塊 6012a、6012b 固定，因此可迴避凸塊 6012a、6012b 之變形或凸塊間之短路；至此，發光裝置 6020 即告完成。最後，一個一個發光裝置 6020 會從圖示未顯示之導線架上，由引線部 6023a、6023b 之另一端處分離。

該第 18 實施形態中，使用了與玻璃材料有優良密著性之引線部 6023a、6023b、並於 LED 元件下方設置有絕緣層 6024，因此以密封構件 6025 進行密封時，密封構件 6025 並不會對 LED 元件 6021 造成不良影響，並可防止凸塊 6021a、6021b 之變形、移動及短路等情形之發生。再者，以玻璃材料所構成之密封構件 6025 將整體密封時，可防止密封構件為樹脂時會發生之變黃、著色等所導致之光放率衰減之問題之發生。

圖 91 是與第 19 實施形態有關之發光裝置之剖面圖，與第 18 實施形態相同，該發光裝置 6030 是使用次裝載基台將之搭載於導

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線架上之金屬引線形態之裝置；與圖 90 相同，此處僅顯示主要部分之構成，且次裝載基台 6032 顯示的並非剖面之狀態。本實施形態與第 18 實施形態相異之處在次裝載基台之構造，絕緣層之構成及形成範圍等。

該發光裝置 6030 具有以下部分：(1)於安裝面設置有凸塊 6031a、6031b 之 LED 元件 6031，(2)搭載有 LED 元件 6031 之次裝載基台 6032，(3)將前端部分搭載次裝載基台 6032 之做為供電構件之引線部 6032a、6032b(4)混合有螢光體 6034a 且將 LED 元件整體包圍之以滴下或填充方式形成之絕緣層 6034，(5)將包含 LED 元件 6031 上方在內之引線部 6033a、6033b 之前端部分進行密封之由具有透光性玻璃所形成之密封構件 6035。

次裝載基台 6032 可使用例如具高度熱傳導之 AlN(氮化鋁)，LED 元件 6031 之安裝面形成有與凸塊 6031a、6031b 連接之電極 6032a、6032b；相反側(導線架側)則形成有以與引線部 6033a、6033b 連接為目的之電極 6032c、6032d。為將電極 6032a 與電極 6032c、電極 6032c 與電極 6032d 連接，而於次裝載基台 6032 內設置有通孔 6032e、6032f。

引線部 6033a、6033b 由銅或鐵系金屬所構成，是做為圖示未顯示之導線架之一部分，以導線架兩側之帶狀部分與內側間保持規定之間隙、且兩引線部面對面之方式所形成，而 1 個 LED 元件分配有一對線部。引線部 6033a、6033b 之前端之一部分是以有薄層斷差之方式製作，該斷差部分會裝載次裝載基台 6032。

絕緣層 6034 以矽材料為主體，並混合有螢光體 6034a；另外，在密封構件 6025 於密封進行時發生化學結合中斷、成為 SiO_2 之形成過程、及使用鑽石或含有 AlN 粉末之絕緣材料時等兩種情況下，其放熱效果與絕緣層 6013 之情況時相同。

螢光體 6034a 之部分，當 LED 元件 6021 為藍光發光時，可使用具有被該藍光所激勵、而放出黃光特性之 Ce：Yttrium Aluminum Garnet (釔鋁紅榴石)。

與上述實施形態相同，密封構件 6035 使用具透光性、低融點特性之玻璃材料。

該發光裝置 6030 中，引線部 6033a 為正(+)電源供給端子時，被供給至引線部 6033a 之電流會經過引線部 6033a、電極 6032c、通孔 6032e、電極 6032a、凸塊 6031a，流至 LED 元件 6031 之陽極；而由 LED 元件 6031 之陰極流出之電流則經過凸塊 6031b、電極 6032b、通孔 6032f、電極 6032d，流至引線部 6033b，此時 LED 元件 6031 會發光。

以下說明發光裝置 6030 之組裝方式。

首先準備一形成有電極 6032a~6032d 及通孔 6032e、6032f 之次裝載基台 6032，該次裝載基台 6032 上之規定位置處形成有凸塊 6031a、6031b，並將 LED 元件 6031 搭載於該凸塊上；如此，LED 元件 6031 會透過凸塊 6031a、6031b 與電極 6032a、6032b 有電連接，並達成機械性之固定。

其次，將搭載於次裝載基台 6032 上之 LED 元件 6031 以配合通電方向之方式配置於引線部 6033a、6033b 前端之窪槽中。另外，亦可以是將次裝載基台 6032 搭載至引線部 6033a、6033b 上之後，再將 LED 元件 6031 搭載至次裝載基台 6032 之順序。

其次，將混合有螢光體 6034a 之絕緣層 6034 以滴下或填充之方式使其到達次裝載基台 6032 之頂面、側面及底面。

其次，將之搬入模具中，並將以形成密封構件 6035 為目的之玻璃片(圖示未顯示)配置於 LED 元件 6031 之上方及下方，再以規定之溫度以加壓方式形成半球狀，完成發光裝置 6030。於密封進行時，矽材會 SiO_2 化、成為絕緣層 6034，並將 LED 元件 6031 下方、凸塊 6031a、6031b 固定，因此可迴避凸塊 6031a、6031b 之變形或凸塊間之短路。最後，一個一個發光裝置 6030 會從導線架上，由引線部 6033a、6033b 之另一端分離。

藉由該第 19 實施形態，可獲得以下效果。

(1)由於設置有絕緣層 6034，因此利用密封構件 6035 進行密封時，

密封構件不會對 LED 元件 6031 造成不良影響，可以防止凸塊 6031a、6031b 發生變形、移動及短路等情形。

(2)絕緣層 6034 中混合有螢光體 6034a，因此可降低引線部上之電極(或次裝載基台上之配線層)將光吸收之情形。通常，電極或配線層上會鍍金，藍或紫光之吸收率較高，藉由設置混入有螢光體之絕緣層 6034，可將 LED 元件側面所放出之光進行波長之變換，可防止鍍金面之光吸收。

(3)亦可針對由 LED 元件 6031 上方所發出之光進行波長之變換。

另外，利用玻璃材料所構成之密封構件 6035 將整體進行密封，可防止密封構件為樹脂時會發生之變黃、著色所導致之光之衰減之問題。

另外，次裝載基台 6032 亦可使用如圖 90 所示之，具有左邊為開口形狀

之配線層 6022a、6022b 之次裝載基台 6022。相反的，亦可使用圖 91 所示之次裝載基台 6032 取代圖 90 之次裝載基台 6022。

圖 92 是標準尺寸之 LED 元件之凸塊形成面之俯視圖。該 LED 元件 6031 為長寬為 0.3mm 之 LED 元件，配置有(1)搭載有與 n 電極連接之凸塊 6041 之小圖案 6042，(2)與 p 電極連接之大圖案 6043，(3)搭載於該大圖案 6043 上之凸塊 6044a、6044b。LED 元件 6031 為高輸出型時，其電流愈大。因此，將 p 電極之凸塊數形成複數個，以對應大電流容量。

圖 93 是大尺寸之 LED 元件之凸塊形成面之俯視圖。該 LED 元件 6031 為長寬為 1mm 之 LED 元件，配置有(1)搭載有凸塊 6052a、6052b 之配線圖案 6054，(2)設置有凸塊 6053a、6053b 之配線圖案 6055。該大尺寸 LED 元件之發光面積較標準尺寸之發光面積大之故，會有更大之電流流通。因此，為使發光面有均一之發光，而對應配線圖案 6054、6055 之形狀 面積，將電極接點之各個凸塊形成複數個。

如圖 92 及圖 93 所示，透過凸塊進行電連接之 LED 元件容易

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因為玻璃密封時之溫度及壓力，導致凸塊之崩潰；特別是如圖 93 所示，具有複數凸塊 6053a~6053p 時，由於各凸塊間之距離較接近，當凸塊變形時，相當容易發生短路之情形。針對這種 LED 元件 6031，絕緣層 6034 不僅將凸塊覆蓋、確保凸塊間之絕緣，並可對抗玻璃密封時之壓力，因此可控制凸塊 6053a~6053p 間之變形，使利用玻璃材料形成密封構件 6035 成為可能。

另外，上述各實施形態中，是以由金所形成之凸塊 6012a、6012b 進行說明，但不限定於金，亦可以利用銲錫形成之凸塊。另外，不限定於凸塊，亦可是於電極上形成之銲錫電鍍層。使用住田光學玻璃製之「K-PSK100」時，由於在超過 400℃之溫度下進行密封加工、且加工時之玻璃黏度較高之故，即使是金凸塊亦會有崩毀之情形發生；另一方面，無機有機混合之綜合型(Hybrid)低融點玻璃雖然可於更低的溫度下進行密封加工，但如銲錫凸塊般、融點較加工溫度還低時，即使是微弱之壓力亦可造成電極間之短路；本發明針對以上現象有其效用。

另外，以上各實施形態中，亦可於密封構件 6014、6025、6035 中之 LED 元件 6012、6032 上方形成以變換波長為目的之螢光體層。

再者，上述各實施形態中，1 個密封構件內配設之 LED 元件數為 1 個，但亦可配設 2 個以上之多晶發光型之發光裝置。搭載之複數 LED 元件可以是設置多個不同發光色之 LED 元件，亦可以是設置多個相同發光色之 LED 發光元件之構成。再者，LED 之驅動形態方面，可以是將多個 LED 元件全部以並聯連接、或以群組單位之並聯連接，而複數單位之串聯連接或全數串聯之連接亦可。

另外，密封構件 6014、6025、6035 於說明中為圓頂狀之構成，但本發明並不限定於圖示之形狀，可以是沒有凸透鏡之形狀、多角形、圓柱形等任意之形狀。

再者，密封構件 6014、6025、6035 於成形之際，並不限定於

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使用玻璃片之加壓成形方式，亦可使用其他密封方法。

圖 94 是與本發明第 20 實施形態有關之發光裝置之構成之剖面圖，通常導線架兩側設置有與各引線部之外側連結之帶狀部，此處則於圖示中將之省略。另外，導線架上通常安裝有多個 LED 元件，次例則僅顯示其中之一。再者，圖 94 中，次裝載基台顯示的非剖面之狀態。

發光裝置 7010 是金屬引線安裝型，由以下部分所構成：(1)透過凸塊 7002，以覆晶型方式接合於安裝面之 GaN 系 LED 元件 7001(熱膨脹係數 4.5~6x10^{-6}/℃)，(2)搭載有 LED 元件 7001 之次裝載基台 7003，(3)搭載有次裝載基台 3 之做為供電構件之由銅所構成之引線部(熱膨脹係數 15~17x10^{-6}/℃、熱傳導係數 400W・m^{-1}・k^{-1})7004A、7004B，(4)以 LED 元件 7001 為中心、將其周圍進行密封之透明玻璃製之密封構件 7005。

次裝載基台 7003 可以使用例如 AlN(氮化鋁：熱膨脹係數 5x10^{-6}/℃、熱傳導係數 180W・m^{-1}・k^{-1})，而 LED 元件 7001 之安裝面形成有與凸塊 7002 連接之電極 7031A、7031B，相對側(導線架側)則形成有與一對引線部 7004A、7004B 連接之電極 7032A、7032B。引線部 7004A、7004B 上方之 LED 元件 7001 之搭載面經過加工後呈現低於其他部分之形態，該窪槽部分內配置有次裝載基台 7003。為將電極 7031A、7031B 與電極 7032A、7032B 連接，而於次裝載基台 7003 內設置通孔 7033。

密封構件 7005 之說明：將具有透明、低融點，且熱膨脹係數接近引線部 7004A、7004B(或在規定之熱膨脹係數差之範圍內)之特色之片狀玻璃進行熱融著，以形成一以將 LED 元件 7001、次裝載基台 7003 及引線部 7004A、7004B 之一部分進行密封之透光性玻璃。

引線部 7004A 為正(+)電源供給端子時，被供給至引線部 7004A 之電流會經過引線部 7004A、電極 7032A、7032B 之其中一方、通孔 7033 之其中一方、電極 7031A、7031B 之其中一方及凸

塊 7002 之其中一方，流至 LED 元件 7001 之陽極；而由 LED 元件 7001 之陰極流出之電流則經過凸塊 7002 之另一方、電極 7031A、7031B 之另一方、通孔 7033 之另一方以及電極 7032A、7032B 之另一方，流至引線部 7004B，此時 LED 元件 7001 會發光。

圖 95 是於導線架上搭載有次裝載基台之狀態之俯視圖，次裝載基台 7003 之中央搭載有 LED 元件 7001。引線部 7004A、7004B 是以做為導線架之一部分，從導線架兩側之帶狀部分與內側間保持規定之間隙、且兩引線部面對面之方式所形成，而 1 個 LED 元件分配有一對線部。

圖 96 是使用模具進行玻璃密封之前一刻之狀態之圖示，該圖顯示的是將圖 95A-A 部分切斷之狀態。以下參照圖 94 至圖 96，說明發光裝置 7010 之製造方法。

首先，將設置有凸塊 7002 之 LED 元件 7001 定位於次裝載基台 7003 上，進行回銲(Reflow)，使凸塊 7002 與電極 7031 間產生電連接，並將之機械性固定。

其次，將搭載於次裝載基台 7003 上之 LED 元件 7001 以配合通電方向之方式配置於引線部 7004A、7004B 前端之窪槽中。另外，次裝載基台 7003 使用的是預先形成有電極 7031A、7031B 及電極 7032A、7032B 與通孔 7033 之基台。

其次，將導線架 7006 搬入模具中，並於 LED 元件 7001 上方極下方配置玻璃片 7007、7008；玻璃片 7007、7008 之目的在形成密封構件 7005，其大小為可以同時密封多個 LED 元件 7001。

其次，以將玻璃片 7007 覆蓋之形態配置上方模具 7011，再以覆蓋玻璃片 7008 之形態配置下方模具 7012。其次，於真空環境中將玻璃片 7007、7008 加熱至 450℃、使其軟化之狀態下，將上方模具 7011 及下方模具 7012 朝圖 95 之箭頭方向移動，針對玻璃片 7007、7008 施壓，使玻璃片 7007、7008 沿著上方模具 7011 之凹部及下方模具 7012 之凹部，形成如圖 94 所示之密封構件般之圓頂形狀。

其次，將導線架 7004 之帶狀部等不要部份除去後，一個個發光裝置 7010 會由導線架 7004 上分離出來。

發光裝置 7010 之發光結構是：透過與衰減電極 7108 及 n 型電極有電連接之凸塊施加順向電壓實，LED 元件 7001 之活性層內之電洞(Hole)與電子之載子(Carrier)會再次結合、發光，而發出之光會透過藍寶石基板 7101 朝 LED 元件 7001 之外部放射；該輸出之光會透過密封構件 7005 朝外部放射。

藉由該第 20 實施形態，可獲得以下效果。

(1)熱膨脹係數大之玻璃材料之密封構件 7005 會將熱膨脹係數小之 LED 元件整體包圍、密封之故，因此熱膨脹係數差所導致之內部應力會被調整至朝向 LED 元件 7001 中心；亦即，玻璃加工後即便發生了因為玻璃材料之熱收縮所導致之內部應力，該內部應力成為朝向 LED 元件中心方向之壓縮力，因此不會對具有可承受壓縮力之強度之玻璃材料造成破壞，可實現玻璃密封構造。

(2)將熱膨脹係數小之 LED 元件搭載於熱膨脹係數小之次裝載基台 7003，再將之搭載於熱膨脹係數大之引線部 7004A、7004B 上之故，形成密封構件 7005 之玻璃材料被要求能與熱膨脹係數小之 LED 元件 7001、熱膨脹係數大之引線部 7004A、7004B 兩者有良好接著性，但最好選擇熱膨脹係數接近 LED 元件 7001 之材料進行密封較好。由銅等軟金屬所形成之引線部 7004A、7004B 與玻璃材料相比較富彈性，假使與 LED 元件 7001 與次裝載基台 7003 之熱膨脹係數差在 150%~400%之範圍內，則不僅可維持其與玻璃材料間之良好接著性，亦可以將熱收縮差所導致之應力結構性地吸收。由以上原因，以玻璃材料將引線部 7004A、7004B 夾住、密封實，亦不會發生碎裂等不良。

(3)當投入大量電力至 LED 元件 7001 之、產生高熱時，LED 元件亦可將發熱向外部放熱，可有效果地防止發光效率之降低；特別是，次裝載基台 7003 以及引線部 7004A、7004B 之熱傳導係數在 $100W \cdot m^{-1} \cdot k^{-1}$ 時可實現上述效果。

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(4)由於是使用低融點玻璃片 7007、7008 形成密封構件 7005，因此可縮短加熱所需之時間，使用簡易之加熱裝置，使玻璃密封加工變得容易。

(5)由於加工時不易發生碎裂等不良，可長期、安定地維持以玻璃材質進行之高度密封性，即使於水中、高濕條件下，發光條件亦不會降低，可長期發揮優良之耐久性。

另外，第 1 實施形態中，LED 元件 7001 是以 GaN 系 LED 元件 7001 之構成為例做說明，但 LED 元件不限定於 GaN 系，亦可使用其他 LED 元件。

另外，該實施形態中，係以由銅所構成之引線部 7004A、7004B 上搭載次裝載基台 7003 為例做說明，但例如由黃銅構成之引線部(熱傳導係數在 106W・m^{-1}・k^{-1})上搭載由矽所構成之次裝載基台 7003(熱傳導係數在 170W・m^{-1}・k^{-1})之構成亦可。

另外，密封構件 7005 方面，不限定於使用片狀玻璃、將多個 LED 元件 7001 及次裝載基台 7003 一次全部密封之形成方式，亦可以是將溶融玻璃材料供給至 LED 元件 7001 及次裝載基台 7003 之周圍，然後以上方模具 7011 及下方模具 7012 進行熱壓之形成方式。另外，所使用之玻璃材料只要是具有光透光性的話，並不做特別之限定，有著色之材料亦可。

另外，密封構件 7005 可依照規格等形成各種形狀，例如圓形、橢圓形、四角形等，亦可以是有凸透鏡、無凸透鏡之形狀。

該第 20 實施形態中是以將金屬引線供電構件之覆晶型發光裝置做說明，但亦可適用於其他形態之發光裝置。例如，使用連線接合之朝上(Face Up)型發光裝置亦可適用。

圖 97 是與第 20 實施形態有關之發光裝置之變形例之剖面圖，該發光裝置 7010 中是以將次裝載基台 7003 之角部去除，設置傾斜部 7003A 之構成，防止密封構件 7005 之熱膨脹、熱收縮所導致之碎裂。使用該次裝載基台 7003 時，除了第 20 實施形態之優良效果外，亦可時先不易發生碎裂情形之玻璃密封型發光裝置

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7010。

圖 98 是與第 21 實施形態相關之朝上型發光裝置之剖面圖，該發光裝置 7040 具有以下部分：(1)前端設有間隔、配置於水平方向及一直線上之做為供電構件之引線部 7004A、7004B，(2)透過接著劑等被搭載於引線部 7004A 前端上方之 GaN 系 LED 元件 7041，(3)將 LED 元件 7041 兩個電極(圖示未顯示)及引線部 7004A、7004B 連接之連線 7042，(4)將 LED 元件 7041 及引線部 7004A、7004B 之前端進行密封之由玻璃材料所構成之密封構件 7005。

密封構件 7005 使用的是透明、低融點、具有規定範圍內之熱膨脹係數之玻璃材料；特別是朝上型且使用連線之情形，於進行密封加工時，因加熱而軟化之連線 7042 及連線連接部 7042A 受壓力而較易毀損，容易產生短路等情形。因此，最好是使用越低之溶點之玻璃越好。

以下說明發光裝置 7040 之組裝方式。

首先，於導線架分離前之狀態下，將 LED 元件 7041 搭載至引線部 7004A 之前端頂面；其次利用連線 7042 將 LED 元件 7041 頂面之其中一方之電極 7004A 與引線部 7004A 頂面進行連接，再以連線 7042 將 LED 元件 7041 頂面之另一電極與引線部 7004B 頂面進行連接。其次，如第 20 實施形態所說明般，利用模具進行玻璃材料之成形，並形成規定形狀之密封構件 7005。最後，將導線架 7004 不要的部分除去，使各個發光裝置 7040 由導線架 7004 上分離。

圖示 98 中，例如當引線部 7004A 為 LED 元件 6012 之陽極(Anode)時，引線部 7004A 會與直流電源(圖示未顯示)之正極(Plus)連接，而引線部 7004B 則會與負極(Minus)連接。透過該通電過程 LED 元件 7041 會發光，光會由 LED 元件 7041 頂面射出，且幾乎所有的光會穿透密封構件 7005 內部、被釋放至外部，部分的光會在內部反射後，放出至密封構件 7005 外。

藉由該第 21 實施形態，除了可獲得第 20 形態之良好效果外，在考慮到引線部 7004A、7004B 與密封構件 7005 間之熱膨脹係數之數值，而使用低融點玻璃材質時，即使是朝上型(Face Up)型發光裝置 7040，亦可防止剝離或碎裂之情形發生。

另外，上述各實施形態中，亦可於引線部 7004A、7004B 表面形成反射面，提高光之射出效率。

另外，LED 元件 7001、7042 上方之密封構件 7005 中，亦可設置以特定波長之光激勵螢光體之波長變換部。

再者，上述各實施形態中，個密封構件內配設之 LED 元件數為 1 個，但亦可配設 2 個以上之發光型多晶型之發光裝置；此時，圖 94 所示之覆晶接合型之構成很適合該發光裝置形態。而搭載之複數 LED 元件可以是設置多個不同發光色之 LED 元件，亦可以是設置多個相同發光色之 LED 發光元件之構成。

再者，LED 之驅動形態方面，可以是將多個 LED 元件全部以並聯連接、或以群組單位之並聯連接，而複數單位之串聯連接或全數串聯之連接亦可。另外，說明當中之密封構件 7005 之形狀是頂部形成有凸透鏡之半球狀之構成，但密封構件 7005 並不限定於圖示之形狀，亦可以是沒有凸透鏡之形狀、多角形、圓柱形等任意之形狀。

再者，密封構件 7005 於成形之際，使用的是玻璃片，但並不限定於使用玻璃片方式，亦可使用其他密封方法。

圖 99 是與本發明第 22 實施形態有關之覆晶型發光裝置，(a)是剖面圖，(b)是由(a)之右側觀看之側面圖；另外，與第 20 實施形態相同之構成之部分則加上共通之數字表示。如圖 99(a)所示，該發光裝置 7010 之構成是將次裝載基台元件 7003 搭載至由銅所構成之放熱部 7050，並以密封構件 7005 將之密封成一體，而密封構件 7005 則形成有凸透鏡 7005A。

次裝載基台元件 7003 被收納於設置於放熱部 7050 之溝槽部 7051，而設置於其表面之配線圖案 7053 藉由凸塊 7002 與 LED 元

件 7001 之電極有電性之連接、構成供電部之一部分。配線圖案 7053 與 LED 元件 7001 接合後，再與由軟金屬之銅所構成之引線部 7004A、7004B 以銲錫接合。如圖 99(b)所示，引線部 7004B 在與放熱部 7050 為絕緣之狀態下，利用長方形剖面、透過棒狀玻璃材料 7052 將密封構件 7005 加熱加壓至溝槽部 7051。此時，引線部 7004A 以相同於引線部 7004B 之方式被處理。引線部 7004A、7004B 藉由以加熱加壓方式溶融之玻璃材料 7052 及密封構件 7005，在與放熱部 7050 間為絕緣之狀態下成為一體。

藉由第 22 實施形態，搭載次裝載基台元件 7003 之放熱部 7005 與由玻璃材料所構成之密封構件 7005 會經由密封而一體化，如此除了可獲得第 1 實施形態之良好效果之外，上可提高由次裝載基台元件 7003 所傳出之熱之放熱性，如此不僅於玻璃密封加工時，即使是在例如因為大電流化而導致 LED 元件 7001 之發熱量增大時，亦可獲得一具有良好之放熱性、且不容易因為熱膨脹係數差而發生 PACKAGE 碎裂之發光裝置 7001。

該第 22 實施型態之說明中是使用由銅(Cu)所構成之放熱部 7050，但亦可使用例如由銅合金或鋁等熱傳導性良好、與密封構件 7005 間之熱膨脹係數差較小之材料。當放熱部 7050 是鋁所構成時，其與 LED 元件 7001 及次裝載基台 7003 之熱膨脹係數之差為 500%。

圖 100 是與本發明第 23 實施型態有關之朝上型發光裝置，(a)是剖面圖，(b)是由(a)之右側觀看之側面圖。另外，與第 20 實施形態相同之構成之部分則加上共通之數字表示。如圖 100(a)所示，發光裝置 70040 之構成是：將 LED 元件 7040 接合至由銅所構成之放熱部 7050 之中央，利用連線 7042 將供電至 LED 元件 7040 之引線部 7004A、7004B 與 LED 元件 7040 之電極進行電連接。另外，LED 元件 7040、連線 7042、引線部 7004A、7004B 被由具有耐熱性之矽樹脂所構成之矽膜 7060 所覆蓋，密封構件 7005 將矽膜 7060 覆蓋之同時，亦與放熱部 7050 成為一體；另外，密封構

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件 7005 上形成有凸透鏡 7005A。

藉由第 23 實施型態，即使是朝上型發光裝置 7040，由於藉由附有耐熱性及彈性之矽膜 7060 將 LED 元件 7041 周圍覆蓋，除了可防止加工密封時之壓力所導致之 LED 元件 7041 之電極或連線 7042 之變形，更可進行玻璃密封，除了可獲得第 21 實施型態之良好效果外，還可達到 LED 元件 7041 之良好安裝性，該優點不僅於玻璃密封時，例如在通上大電流、導致 LED 元件 7041 之發熱量增大時，可獲得良好之發熱性；同時，亦可獲得一不因熱膨脹係數差而導致 PACKAGE CRACK 之發光裝置 7001。另外，矽膜 7060 亦可含有螢光體。

另外，該第 23 實施型態之構成是：由一對引線部 7004A、7004B 針對搭載於放熱部 7050 之 LED 元件 7041 進行供電之構成，但亦可以是以下構成：例如將放熱部 7050 與其中一方引線部一體化，再利用玻璃材料 7052 使另一方引線部與放熱部 7050 絕緣化。

另外，鍍膜材料除了使用矽樹脂之外，亦可使用陶瓷鍍膜材料等其他據有耐熱性之材料；該鍍膜實施之對象不限定於朝上型 LED 元件，亦適用於覆晶型 LED 元件。

另外，LED 類型之發光元件中，當發光元件之折射率為 2 以上時，若使用折射率為 1.5 以上之密封材料進行元件之密封時，可將元件之光取出效率提高約 2 倍以上；此時，密封材料必須是透光性。受光元件不具有該效果，以透光性材料直接將元件密著密封時，僅具在不同媒質之介面時可減少反射之效果；若非光學元件則不需具有透光性。

另外，說明中之芳止材料為玻璃材質，但只要是玻璃加工後成結晶化之材料即可，亦可以是以高度化學安定性之無機材料。

五、【圖式簡單說明】

圖 1 係與本發明之第 1 實施型態有關之發光裝置，其中(a)是發光裝置之剖面圖，(b)是光源之 GaN 系 LED 元件之側面圖。

圖 2 係與本發明之第 1 實施型態有關之發光裝置之第 1 變形例，其中(a)是發光裝置之縱剖面圖，(b)是光源之 Gan 系 LED 元件之側面圖。

圖 3 是第 3 變形例，顯示一使用其他填膠之發光裝置之縱剖面圖。

圖 4 是第 4 變形例，顯示的是設置有由樹脂材料所構成之模具成形部之發光裝置。

圖 5 顯示的是與第 2 實施型態有關之發光裝置之縱剖面圖。

圖 6 是與本發明第 3 實施型態有關之發光裝置之縱剖面圖。

圖 7 顯示的是與第 3 實施型態有關之發光裝置之變形例之縱剖面圖。

圖 8 顯示的是與第 4 實施型態有關之發光裝置之縱剖面圖。

圖 9 顯示的是與第 4 實施型態有關之發光裝置之第 1 變形例之縱剖面圖。

圖 10 顯示的是與第 4 實施型態有關之發光裝置之第 2 變形例之縱剖面圖。

圖 11 顯示的是與第 5 實施型態有關之發光裝置，其中(a)是發光裝置之俯視圖，(b)是發光裝置之側面圖，(c)是發光裝置之底視圖。

圖 12 顯示的是與第 5 實施型態有關之發光裝置之第 1 變形例之縱剖面圖。

圖 13 顯示的是與第 5 實施型態有關之發光裝置之第 2 變形例之縱剖面圖。

圖 14 顯示的是與第 6 實施型態有關之發光裝置之剖面圖。

圖 15 顯示的是與第 6 實施型態有關之發光裝置之第 1 變形例，其中(a)是發光裝置之縱剖面圖，(b)是光源之 GaN 系 LED 元件之側面圖。

圖 16 顯示的是與第 6 實施型態有關之發光裝置之第 2 變形例，其

中(a)是發光裝置之縱剖面圖，(b)是光源之 GaN 系 LED 元件之側面圖。

圖 17 顯示的是與第 7 實施型態有關之發光裝置，其中(a)是發光裝置之縱剖面圖，(b)是光源之 GaN 系 LED 元件之側面圖。

圖 18 顯示的是與第 7 實施型態有關之發光裝置之第 1 變形例之縱剖面圖。

圖 19 顯示的是與第 8 實施型態有關之發光裝置，其中(a)是發光裝置之縱剖面圖，(b)是光源之 GaN 系 LED 元件之側面圖。

圖 20 顯示的是與第 8 實施型態有關之發光裝置之縱剖面圖。

圖 21(a)至(f)顯示的是電路圖案之形成步驟：形成一於 AlN 基板上具有 Au 層之電路圖案。

圖 22 顯示的是與第 9 實施型態有關之發光裝置之縱剖面圖。

圖 23 顯示的是針對導線架進行以熱壓加工為基礎的玻璃密封之狀態。

圖 24 顯示的是將 GaN 系 LED 元件 2 搭載於做為齊納二極體之矽次裝載基台(Submount)上之狀態。

圖 25 顯示的是與第 10 實施型態有關之發光裝置，其中(a)是俯視圖，(b)是(a)A-A 之剖面圖，(c)是下方玻璃之立體圖。

圖 26 顯示的是與第 10 實施型態有關之發光裝置之第 1 變形例之縱剖面圖。

圖 27 顯示的是與第 10 實施型態有關之發光裝置之第 2 變形例之縱剖面圖。

圖 28 顯示的是與第 11 實施型態有關之發光裝置，(a)是側面圖，(b)是玻璃密封時之立體圖。

圖 29 顯示的是與第 12 實施型態有關之發光裝置之縱剖面圖。

圖 30 顯示的是本發明實施例所使用之朝上型態之發光元件之構成之剖面圖。

圖 31 顯示的是發光元件與引線之組合體之立體圖。

圖 32 顯示的是光裝置之製造方法之剖面圖。

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圖 33 顯示的是實施例之光裝置之剖面圖。
圖 34 顯示的是其他實施例之光裝置之剖面圖。
圖 35 顯示的是其他實施例之光裝置之剖面圖。
圖 36 顯示的是其他實施例之光裝置之剖面圖。
圖 37 顯示的是光裝置之製造方法之立體圖。
圖 38 顯示的是其他實施例之光裝置之剖面圖。
圖 39 顯示的是其他實施例之光裝置之剖面圖。
圖 40 顯示的是光裝置之製造方法之剖面圖。
圖 41 顯示的是覆晶型態發光元件之構成之剖面圖。
圖 42 顯示的是使用發光元件之光裝置之實施例之剖面圖。
圖 43 顯示的是其他實施例之光裝置之剖面圖。
圖 44 顯示的是其他實施例之光裝置之剖面圖。
圖 45 顯示的是其他實施例之光裝置之剖面圖。
圖 46 顯示的是其他實施例之光裝置之剖面圖。
圖 47 顯示的是覆晶型態之發光元件與電力接受傳送裝置之組合體之其他型態之俯視圖。
圖 48 顯示的是具備組合體之光裝置之剖面圖。
圖 49 顯示的是其他實施例之光裝置之剖面圖。
圖 50 顯示的是其他實施例之光裝置之剖面圖。
圖 51 顯示的是其他實施例之光裝置之剖面圖。
圖 52 顯示的是其他實施例之光裝置之剖面圖。
圖 53 顯示的是其他實施例之光裝置之剖面圖。
圖 54 顯示的是其他實施例之光裝置之剖面圖。
圖 55 顯示的是其他實施例之光裝置之剖面圖。
圖 56 顯示的是光學元件之構造之剖面圖。
圖 57(a)至(b)顯示的是第 10 實施例之光學裝置之製造方法。
圖 58(a)至(b)顯示的是將光學元件裝載至基板之狀態。
圖 59 顯示的是第 10 實施例之光裝置之構成之狀態。
圖 60 顯示的是其他實施例之光裝置之構成之俯視圖。

圖 61 顯示的是圖 60 中線條 B-B 部分之剖面圖。
圖 62 顯示的是圖 61 中箭頭線條 C-C 部分之剖面圖。
圖 63 是底視圖。
圖 64 顯示的是其他實施例之光裝置之俯視圖。
圖 65 顯示的是實施例之光學元件之構造之剖面圖。
圖 66 顯示的是第 12 實施例之光裝置之俯視圖。
圖 67 是圖 66 中線條 III-III 線之剖面圖。
圖 68 是圖 67 中主要部分之放大圖。
圖 69 是實施例之光裝置之底視圖。
圖 70 顯示的是其他實施例之光裝置之構成。
圖 71 顯示的是其他實施例之光裝置之構成。
圖 72 顯示的是其他實施例之光裝置之構成。
圖 73 顯示的是其他實施例之光裝置之構成。
圖 74 顯示的是其他實施例之光裝置之構成。
圖 75 是發光元件之構成之剖面圖。
圖 76 是實施例之發光裝置之構成，其中(A)是剖面圖，(B)是俯視圖。
圖 77 是具備密封構件之實施例之發光裝置之構成之剖面圖。
圖 78 是具備其他型態密封構件之實施例之發光裝置之構成之剖面圖。
圖 79 是其他型態之導線架之剖面圖。
圖 80 是其他型態之導線架之俯視圖。
圖 81 是其他型態之導線架之俯視圖。
圖 82 是其他型態之導線架之立體圖。
圖 83 是其他型態之導線架之立體圖。
圖 84 是與第 13 實施型態有關之發光裝置之構成之剖面圖。
圖 85 是與第 13 實施型態有關之發光裝置之變形例之剖面圖。
圖 86 是與第 14 實施型態有關之發光裝置之構成之剖面圖。
圖 87 是與第 15 實施型態有關之發光裝置之構成之剖面圖。

圖 88 是與第 16 實施型態有關之發光裝置之構成之剖面圖。
圖 89 是與第 17 實施型態有關之發光裝置之構成之剖面圖。
圖 90 是與第 18 實施型態有關之發光裝置之構成之剖面圖。
圖 91 是與第 19 實施型態有關之發光裝置之構成之剖面圖。
圖 92 是標準尺寸之 LED 元件之凸塊(凸塊)形成面之俯視圖。
圖 93 是大尺寸之 LED 元件之凸塊形成面之俯視圖。
圖 94 是與第 20 實施型態有關之發光裝置之構成之剖面圖。
圖 95 是於導線架上搭載次裝載基台(SUBMOUNT)之狀態之俯視圖。
圖 96 是使用模具進行玻璃密封前之狀態。
圖 97(a)至(c)是與第 20 實施型態有關之發光裝置之變形例之剖面圖。
圖 98 是與本發明第 21 實施型態有關之朝上(Face Up)型發光裝置之剖面圖。
圖 99 是與第 22 實施型態有關之覆晶型發光裝置，其中(a)是剖面圖，(b)是由(a)之右側面所見之側面圖。
圖 100 是與第 22 實施型態有關之朝上型發光裝置，其中(a)是剖面圖，(b)是由(a)之右側面所見之側面圖。

【元件符號之說明】

1 發光裝置
2 元件
3 基板
4 電路圖案(Pattern)
5 金凸塊(AU Stud 凸塊)
6 玻璃密封部
7 填膠
8 導線架
9 模具成形部

10、5035　連線
11　耐熱無機材鍍膜
12　無機白色接著劑
13　銀膠(Ag Paste)
14　元件鍍膜材
15　螢光體層
17　放熱圖案
18　裝載機台
19、7004B　引線部
23　含有發光層之層
27　透光性電極
29　SiC 基板
30　GaN 基板
31　導線架
35　矽鍍膜
40　鎢(W)層
41　鎳(Ni)層
3A　通孔(Via Hole)
3B　溝槽
4A、4B　接著用圖案
4C　金層
5A　導電凸塊
6A　頂面
6B　側面
6C　畫線部
9A　光學形狀面
16A　底面電路圖案(陽極)
16C　底面電路圖案(陰極)
18B　n 層

18C　P層
19A　梯級部
19B　引線罩杯部
19D、190　傾斜面
60A　上方玻璃
60B　下方玻璃
60C　引線收納溝槽
60D　管狀體
191　底面
310、312　開口
311　引線
313　小型孔
314　定位孔
5010、5020、5030、5040、5050、6010、6020、6030、7010發光裝置
5012、5034、5041、6012、6021、6031、7001、7041　LED元件
18A、5011l、5011m、5031f、5031g、5043c、6011m、6011l、6032e、7033　通孔
20、1011、2011、3011、4011　基板
21、1012、2012、3012、4012、5013、5021、5033、5045、5054緩衝層
22、1013、2013、3013、4013　n型層
24、1015、2015、3015、4015　p型層
25、28、1017、2016、3016、4016　p電極
26、1018、4018　n電極
1014、2014、3014、4014　包含發光層之層
1016、1101　透光性電極
5011、5031、6011　基板部
5011a、5031a、11a　陶瓷基板
5011b、5011c、5011d、5011e、5011f、5011g、5031b、5031c、5031d、5031e、6011c、6011d、6011e、6011f、6011g、6022a、6022b　配線層

5011h、5011i、5011j、5011k、6011b、6011h、6011i、6011k、6011j 鍍金膜

5012a、5043a、5043b、6032a 、 6032b、6032c、6032d 、7031A、7031B、7032A、 7032B 電極

5014、5046、5055、6014、6025、6035、7005 密封構件

5042、6012a、6021a、 6021b、6031a、6031b、6041、6044a、6044b、6052a、6052b、6053a、7002 凸塊

5043、5052、6022、6032、7003 次裝載基台

5044a、5044b、5053b、5053a、6023a、6023b、6033a、6033b、6032f、7004A、5052a 、5052b、6054、6055、7053 配線圖案

5051 放熱構件

5054a、6034a 螢光體

6010、7010、7040 發光裝置

6013、6024、6034 絕緣層

6042 小圖案

6043 大圖案

7003A 傾斜部

7004 導線架

7005A 凸透鏡

7007、7008 玻璃片

7011 上方模具

7012 下方模具

7011A、7012A 凹部

7042 接合線

7050 放熱部

7051 溝槽

7052 玻璃材料

7060 矽鍍膜部

十、申請專利範圍：

1.一種固體元件裝置，其特徵為包含：

固體元件，以覆晶型態安裝；

電力接受供給部，對於該固體元件施行電力之接受及供給；及

無機密封材料，將該固體元件予以密封。

2.一種固體元件裝置，其特徵為包含：

固體元件；

電力接受供給部，對於該固體元件施行電力之接受及供給；

耐熱構件，將該固體元件之電連接部與該電力接受供給部之一部分覆蓋；及

無機密封材料，將包含該耐熱構件之該固體元件予以密封。

3.一種固體元件裝置，其特徵為包含：

固體元件；

電力接受供給部，對於該固體元件施行電力之接受及供給；及

玻璃密封部，採用用以密封該固體元件之低融點玻璃，該低融點玻璃係選自於由 SiO_2-Nb_2O_5 系、B_2O_3-F 系、P_2O_5-F 系、P_2O_5-ZnO 系、SiO_2-B_2O_3-La_2O_3 系、SiO_2-B_2O_3 系所構成之族群。

4.一種固體元件裝置，其特徵為包含：

固體元件；

金屬製引線部，對於該固體元件施行電力之接受及供給；及

無機密封材料，將該固體元件予以密封。

5.如申請專利範圍第 4 項之固體元件裝置，其中該引線部由軟金屬構成。

6.如申請專利範圍第 4 項之固體元件裝置，其中該引線部具有次裝載基台，以及對應該次裝載基台之凹部。

7.如申請專利範圍第 4 項之固體元件裝置，其中該固體元件被具有較該固體元件之熱膨脹係數還高的熱膨脹係數之構件所包覆。

8.一種固體元件裝置，其特徵為包含：

固體元件；

電力接受供給部，由無機材料基板構成，對於該固體元件施行電力之接受及供給；及

無機密封材料，用以密封該固體元件，且與該無機材料有相等之熱膨脹係數。

9.如申請專利範圍第 1 項、第 2 項、第 4 項至第 8 項中任一項之固體元件裝置，其中該無機密封材料為無機密封玻璃材料。

10.如申請專利範圍第 9 項之固體元件裝置，其中該無機密封玻璃材料係選自於由 SiO_2-Nb_2O_5 系列、B_2O_3-F 系列、P_2O_5-F 系列、P_2O_5-ZnO 系列、SiO_2-B_2O_3-La_2O_3 系列、SiO_2-B_2O_3 系列所構成的族群中之低融點玻璃。

11.如申請專利範圍中第 1 項至第 3 項中任一項之固體元件裝置，其中該電力接受供給部是由金屬引線所構成。

12.如申請專利範圍第 11 項之固體元件裝置，其中該金屬引線是由軟金屬所構成。。

13.如申請專利範圍第 1 項至第 3 項、第 8 項中任一項之固體元件裝置，其中該電力接受供給部是由形成有導電圖案之無機材料基板所構成，而該無機材料基板之熱膨脹係數與該無機密封材料之熱膨脹係數相等。

14.如申請專利範圍第 13 項之固體元件裝置，其中該無機密封材料之熱膨脹係數較該無機材料基板之熱膨脹係數為小。

15.如申請專利範圍第 13 項之固體元件裝置，其中該無機材料基板是藉由與該無機密封材料之化學反應接合，而將該固體元件密封。

16.如申請專利範圍第 13 項之固體元件裝置，其中該無機密封材料之熱膨脹係數在 $15\times10^{-6}/℃$ 以下。

17.如申請專利範圍第 1 項至第 3 項、及第 8 項中任一項之固體元件裝置，其中該無機材料基板具有金屬層，而該無機材料基板與該無機密封材料係藉由該金屬層之氧化物進行接合。

18.如申請專利範圍第 13 項之固體元件裝置，其中形成於該無機材料基板之導電圖案具有以下種類：(1)裝載該固體元件之側之圖

案、(2)其背側之圖案、(3)將該兩側電連接之圖案。

19.如申請專利範圍第 13 項之固體元件裝置，其中該無機材料基板之表面形成有分割裝置用之溝槽。

20.如申請專利範圍第 13 項之固體元件裝置，其中該無機材料基板由含有玻璃成分之 Al_2O_3 或 AlN 所構成。

21.如申請專利範圍第 1 項至第 8 項中任一項之固體元件裝置，其中該無機密封材料之表面施行有耐濕、耐酸及鹼之鍍膜處理。

22.如申請專利範圍第 1 項至第 8 項中任一項之固體元件裝置，其中該固體元件為光學元件，且該無機密封材料為透光性材料。

23.如申請專利範圍第 22 項之固體元件裝置，其中該光學元件為發光元件。

24.如申請專利範圍第 23 項之固體元件裝置，其中該光學元件係由折射率在 1.7 以上之該無機密封材料所密封。

25.如申請專利範圍第 22 項之固體元件裝置，其中該光學元件為受光元件。

26.如申請專利範圍第 22 項之固體元件裝置，其中該無機密封材料之表面施加有以減輕無機密封材料與空氣間之界面反射為目的之鍍膜處理。

27.如申請專利範圍第 1 項至第 8 項中任一項之固體元件裝置，其中該無機密封材料表面藉由樹脂施以包覆成形(OVER MOLD)。

28.一種固體元件裝置之製造方法，包含以下步驟：

安裝步驟，將固體元件安裝至電力接受供給部；及

密封步驟，於氧氣斷絕環境，以超過無機密封材料之降伏點以上之溫度對該固體元件之無機密封材料加壓之方式，而將該固體元件進行密封。

29.如申請專利範圍第 28 項之固體元件裝置之製造方法，其中該安裝步驟是覆晶安裝。

30.如申請專利範圍第 28 項之固體元件裝置之製造方法，其中該安裝步驟包含以下步驟：施行導線之接合，利用耐熱構件將固體元

EX1012, Page 431

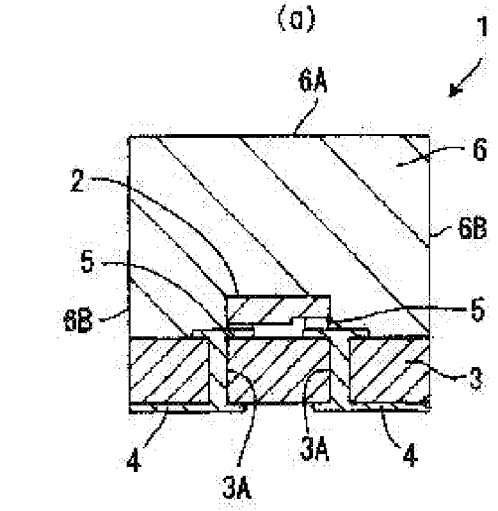
件之連線接合部覆蓋之步驟。

31.如申請專利範圍第 29 項之固體元件裝置之製造方法，其中該密封步驟將無機密封材料在高黏度狀態下進行加工。

32.如申請專利範圍第 31 項之固體元件裝置之製造方法，其中該密封步驟是將該無機密封材料在 10^6 泊以上之高黏度條件下進行加工。

33.如申請專利範圍第 28 項之固體元件裝置之製造方法，其中該電力接受供給部是一安裝有該固體元件且電極被拉出至背面之無機材料基板，將多個固體元件安裝至該無機材料基板，藉由將無機密封材料封接之方式而密封加工，密封後再將之分離。

34.如申請專利範圍第 33 項之固體元件裝置之製造方法，其中該無機密封材料使用的是預成型之玻璃。



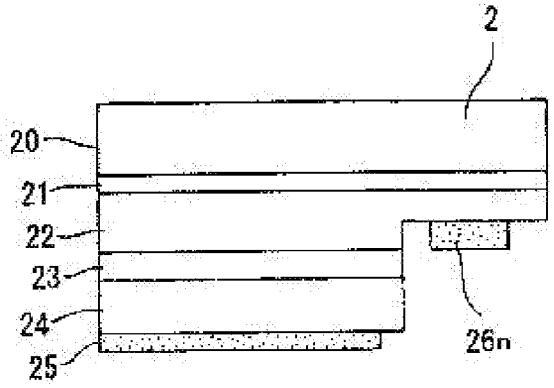


圖 1

圖式

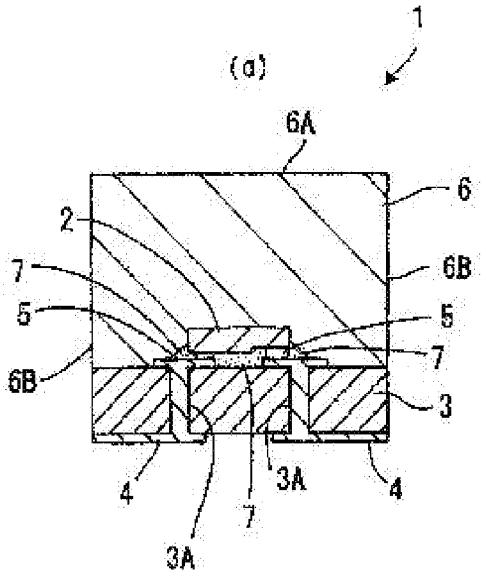


圖 2

圖式

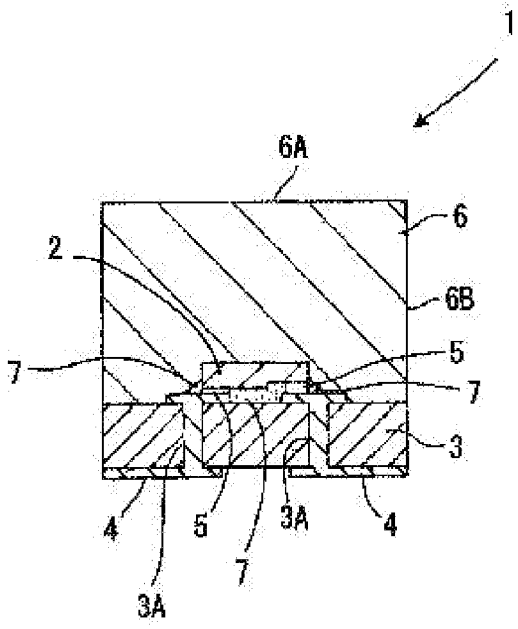


圖 3

圖式

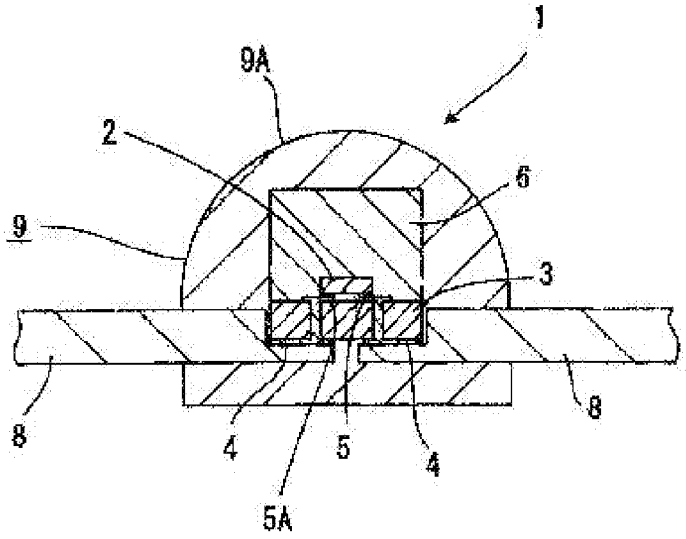


圖 4

圖式

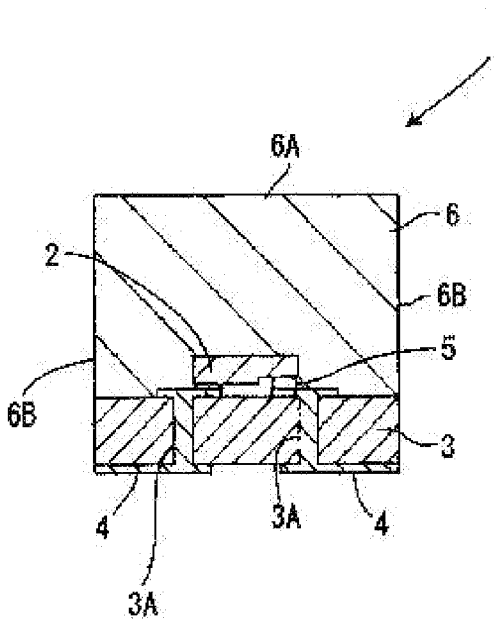


圖 5

圖式

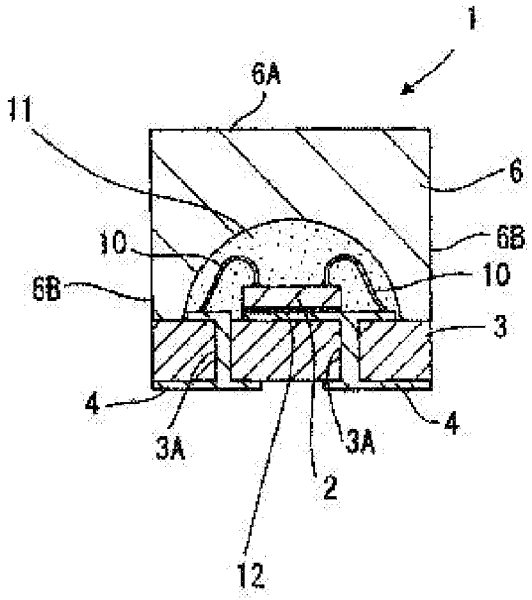


圖 6

圖式

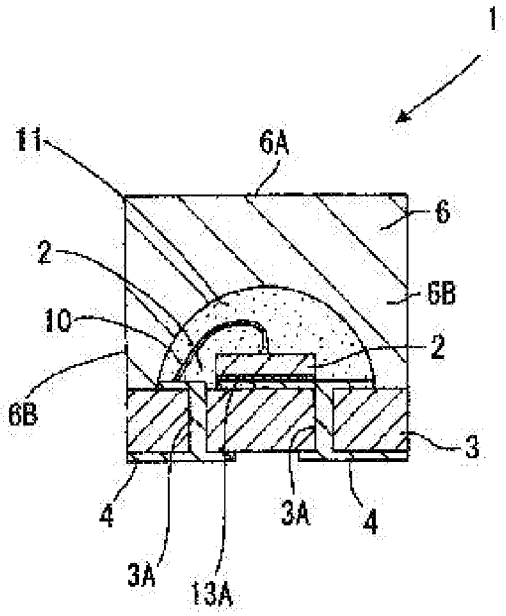


圖 7

圖式

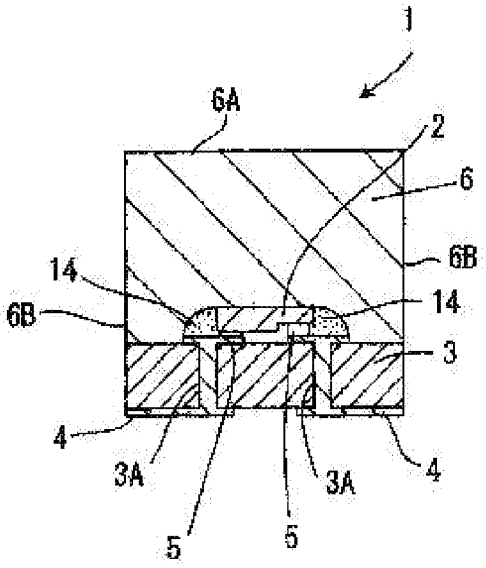


圖 8

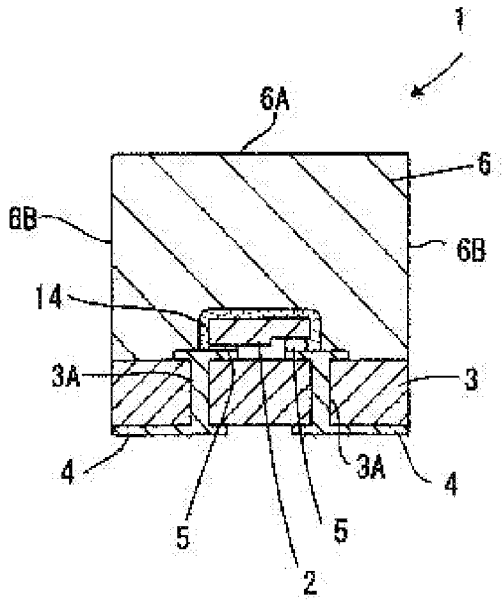


圖 9

圖式

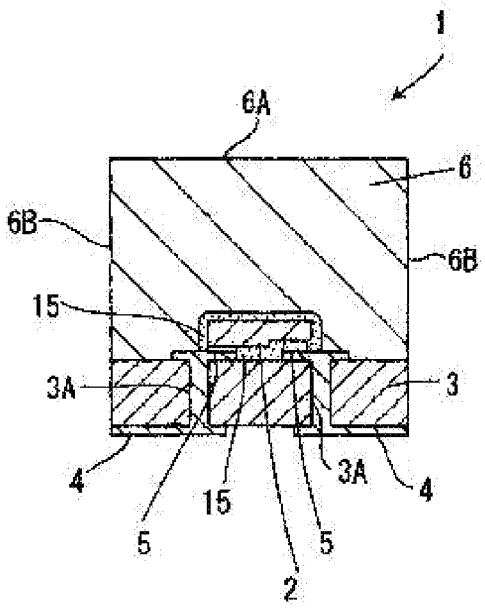


圖 10

圖式

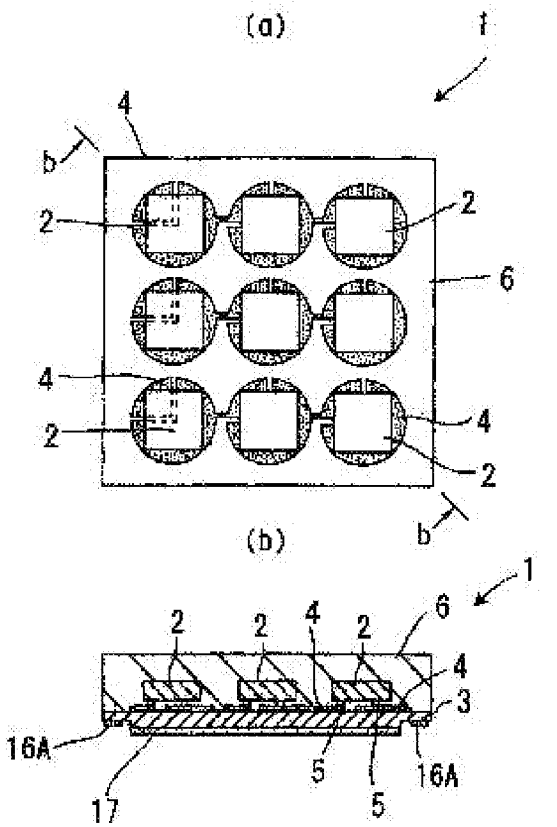


圖 11

圖式

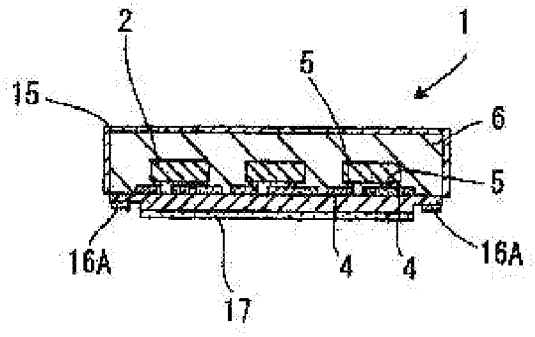


圖 12

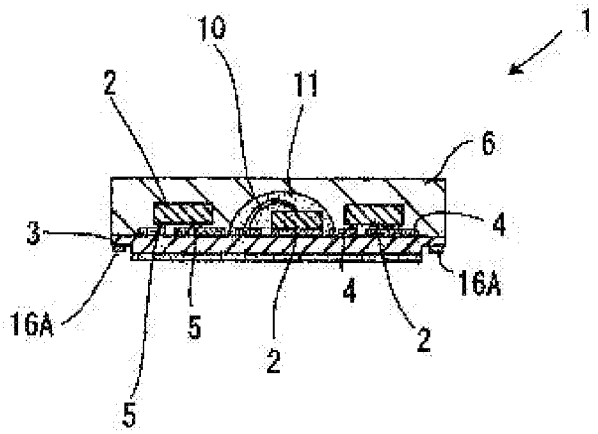


圖 13

圖式

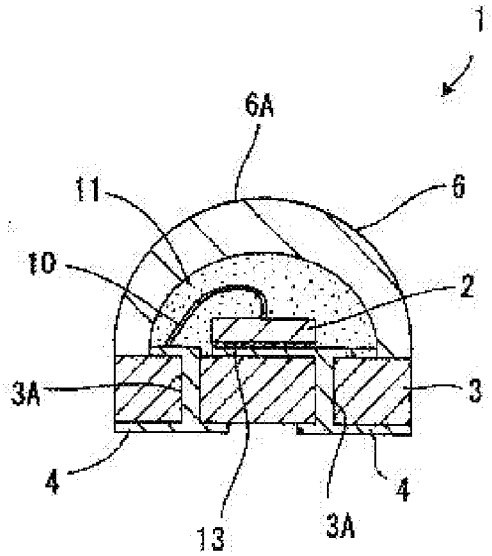
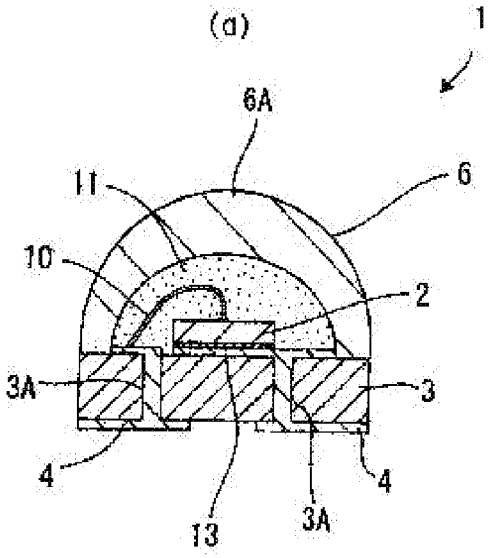


圖 14

圖式



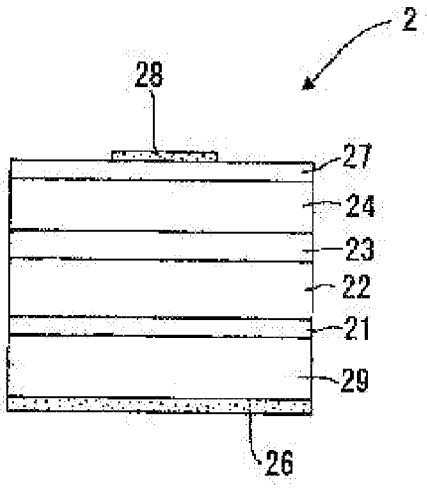
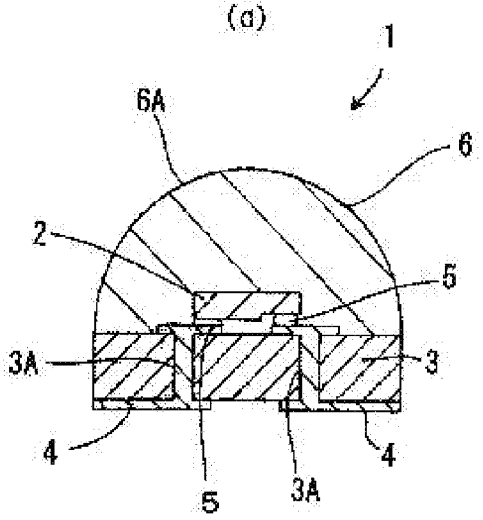


圖 15

圖式

(a)



(b)

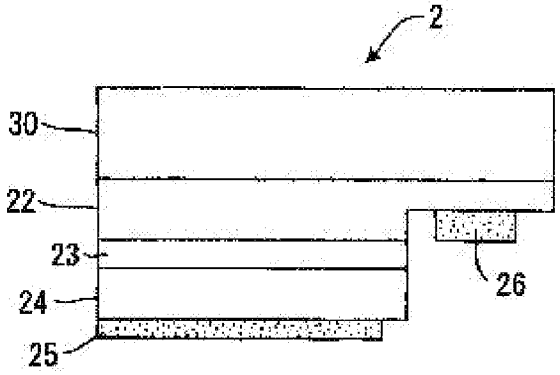
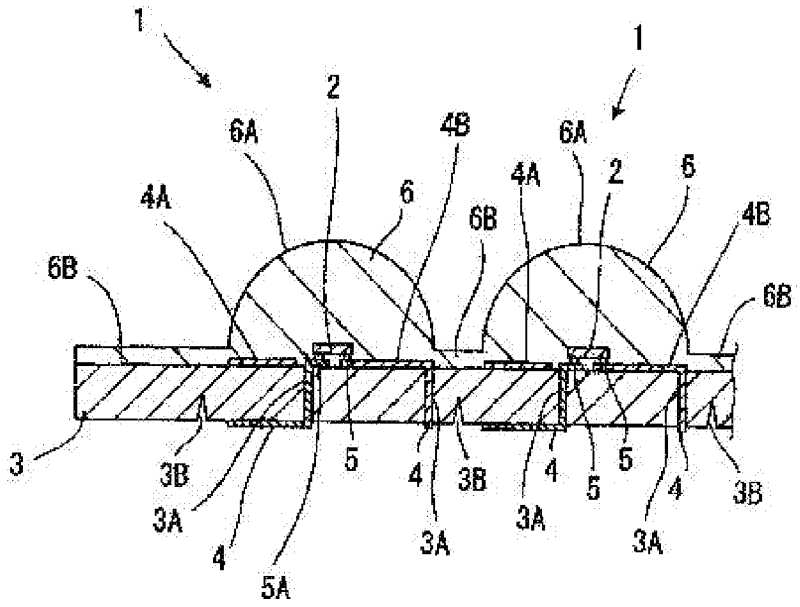


圖 16

圖式

(a)


1
1
2
6A
4B
6A
4A
6
6B
4A
2
6
4B
6B
6B
3
3B
3A
4
5A
5
4
3B
3A
5
4
3A
3A
5
4
3B

(b)

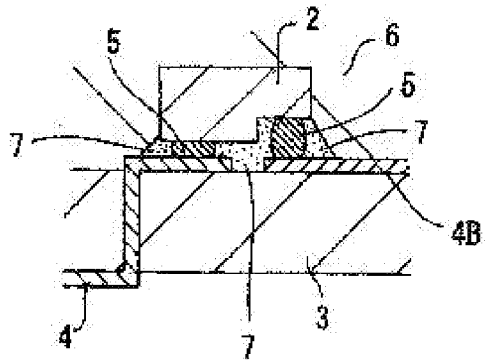

5
2
6
5
7
7
4B
4
7
3

圖 17

圖式

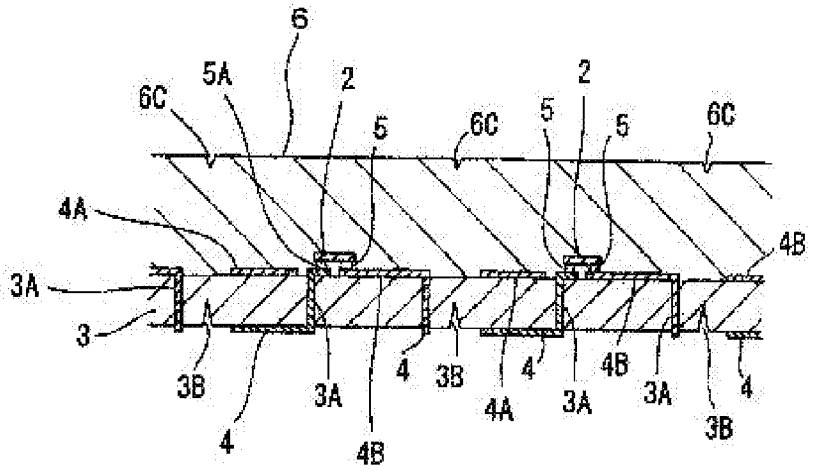
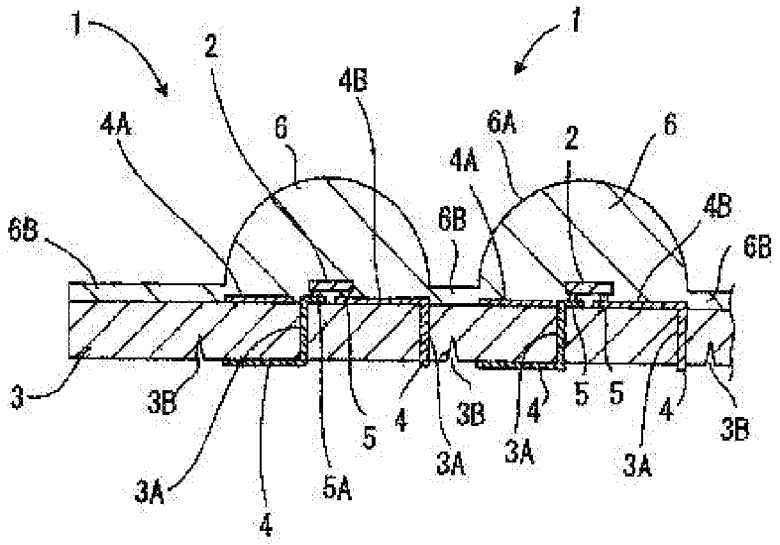


圖 18

圖式

(a)


1
2
4B
4A
6
6A
4A
2
6
6B
6B
4B
6B
3
3B
3A
4
5
5A
4
3B
3A
3A
4
5
5
4
3B

(b)

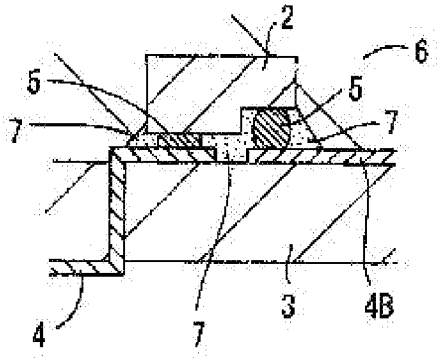

2
6
5
5
7
7
4
7
3
4B

圖 19

圖式

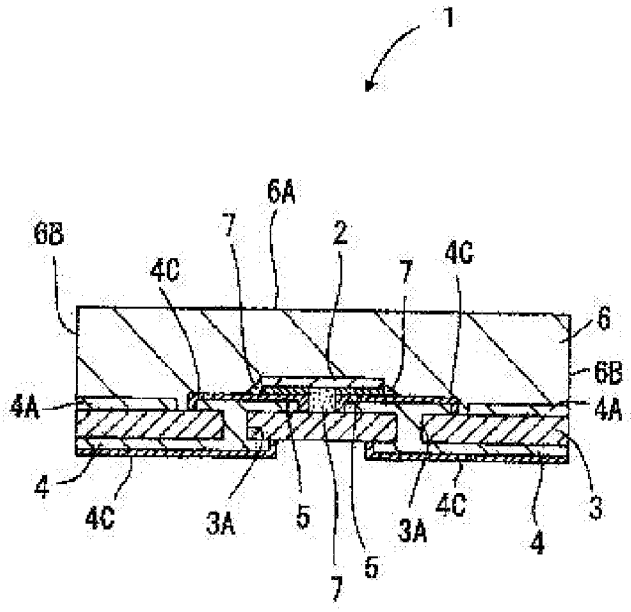


圖 20

圖式

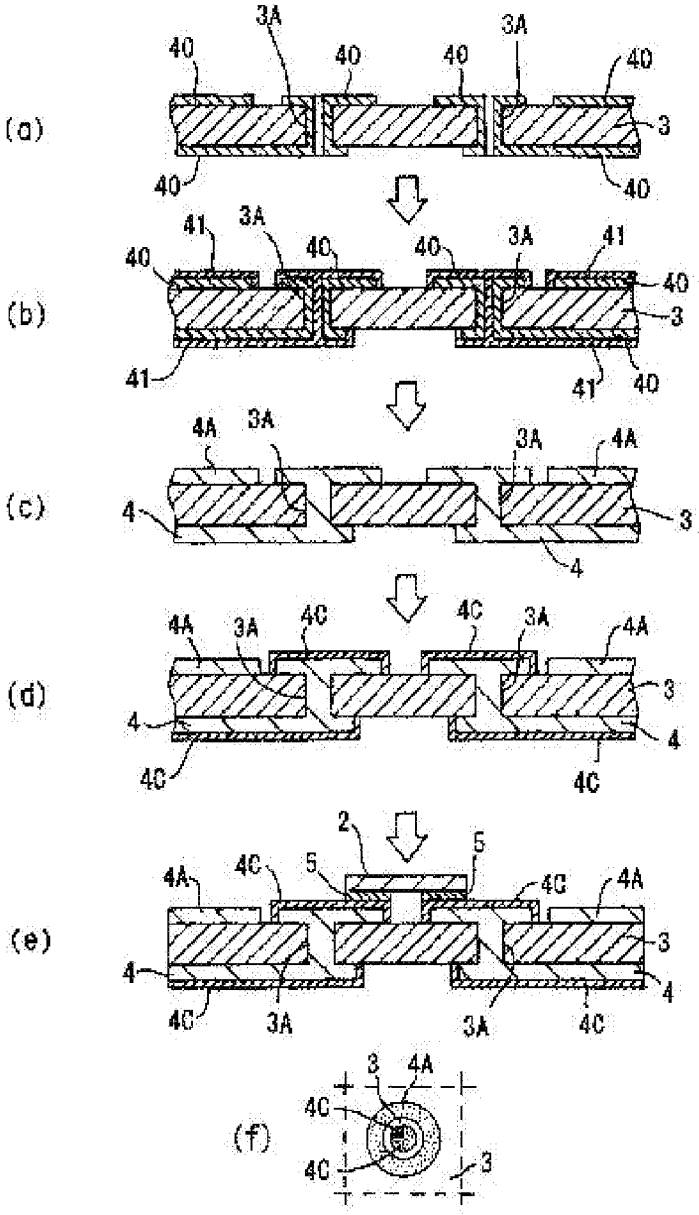


圖 21

圖式

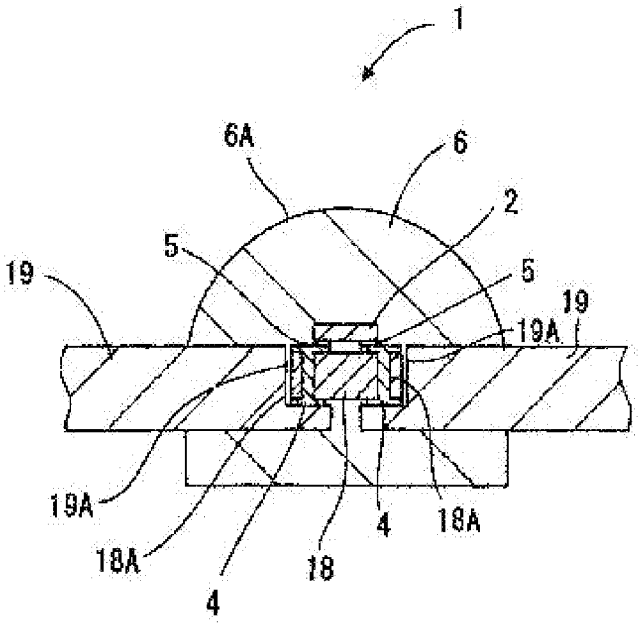


圖 22

圖式

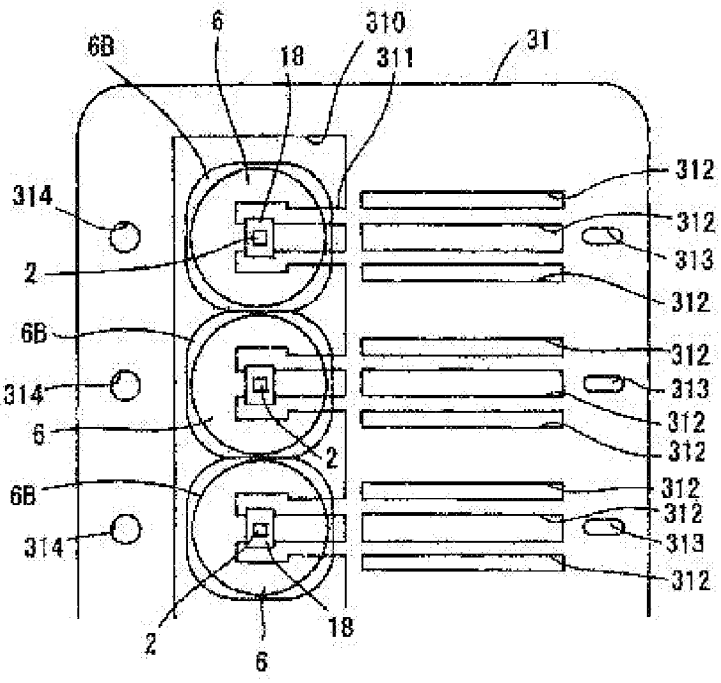

6
310
6B
18
311
31
312
314
312
2
313
312
6B
312
314
313
6
312
2
312
6B
312
312
314
313
312
2
18
6

圖 23

圖式

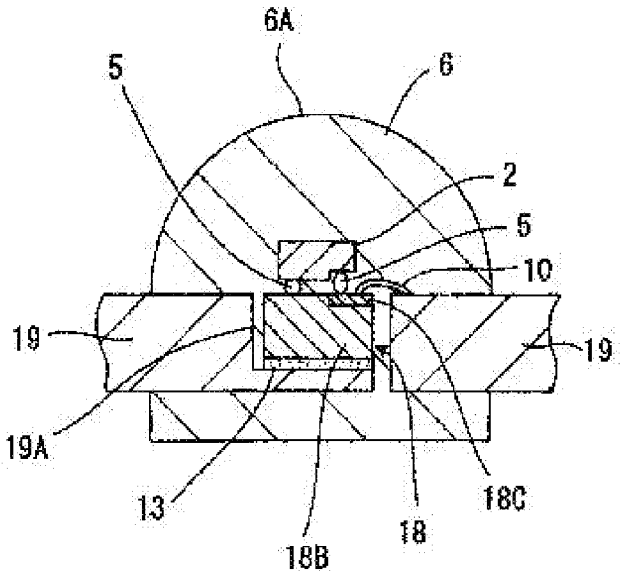


圖 24

圖式

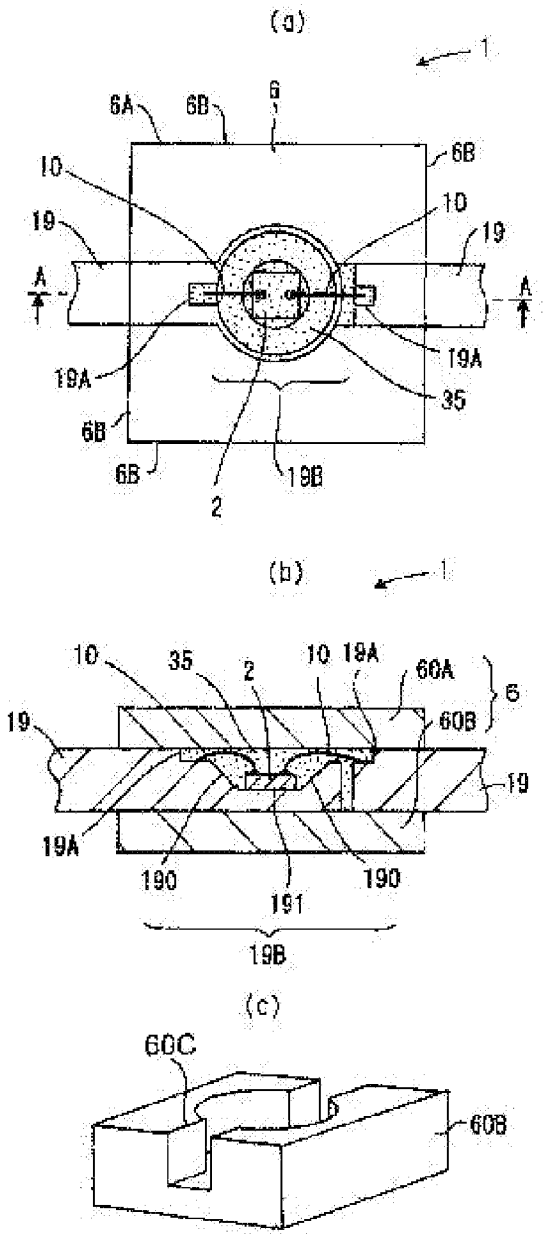

(a)
1
6A
6B
G
6B
10
10
19
19
A
A
19A
19A
35
6B
6B
19B
2
(b)
1
10
35
2
10
19A
60A
6
60B
19
19
19A
190
190
191
19B
(c)
60C
60B

圖 25

圖式

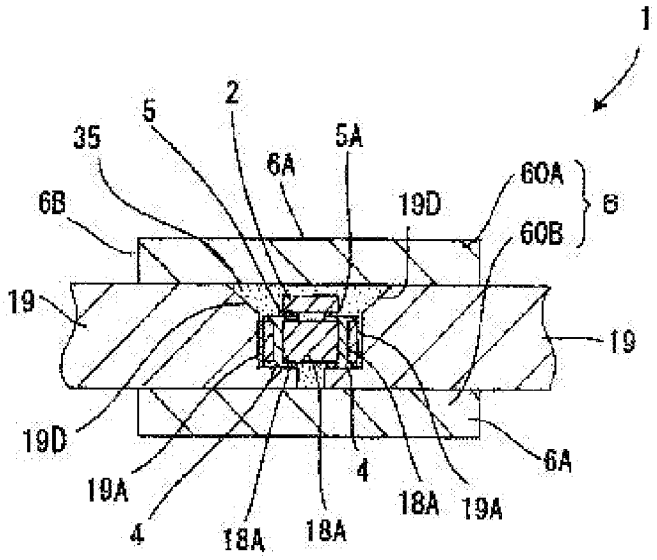


圖 26

圖式

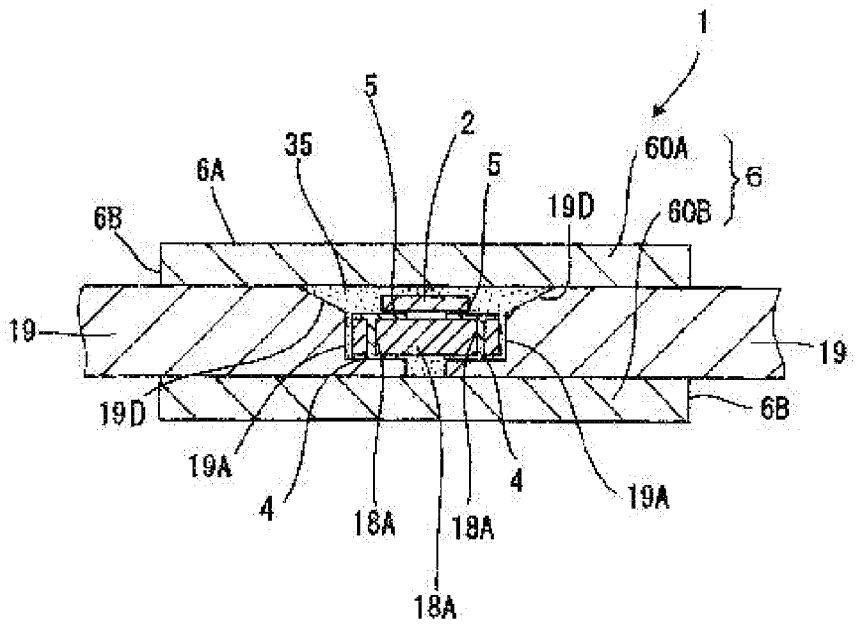
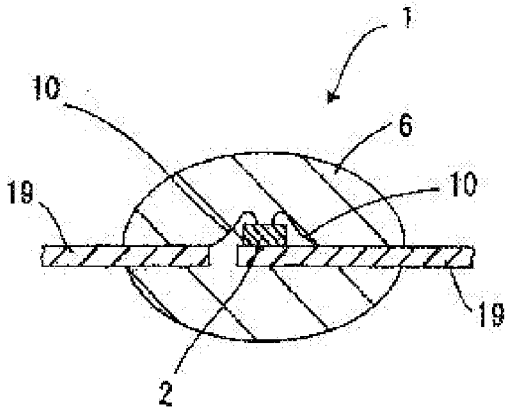


圖 27

圖式

(a)



(b)

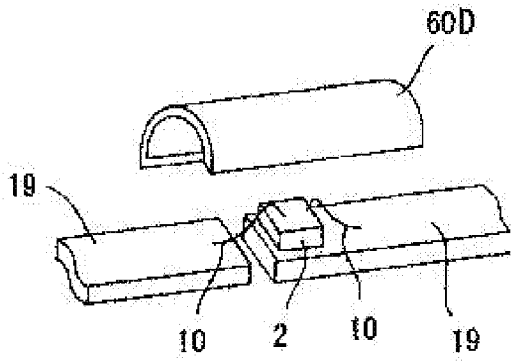


圖 28

圖式

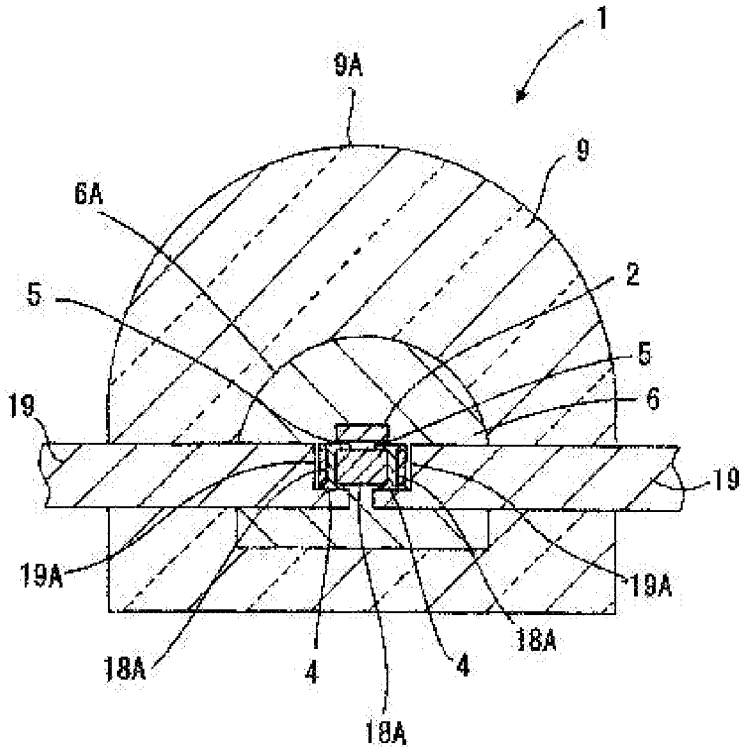


圖 29

圖式

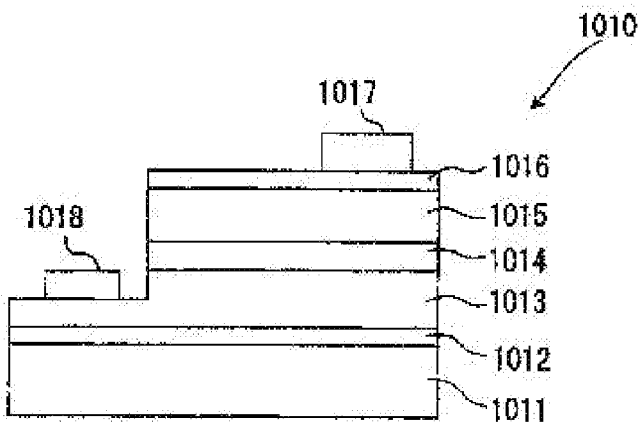


圖 30

圖式

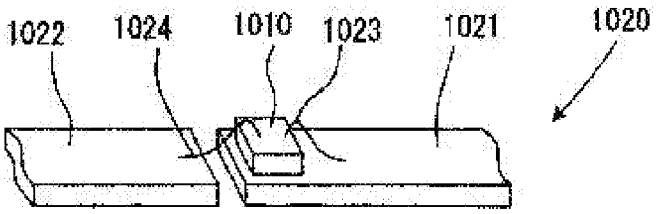


圖 31

圖式

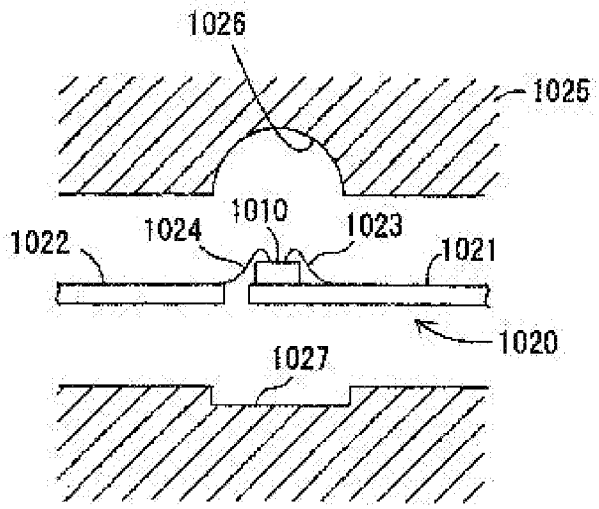


圖 32

圖式

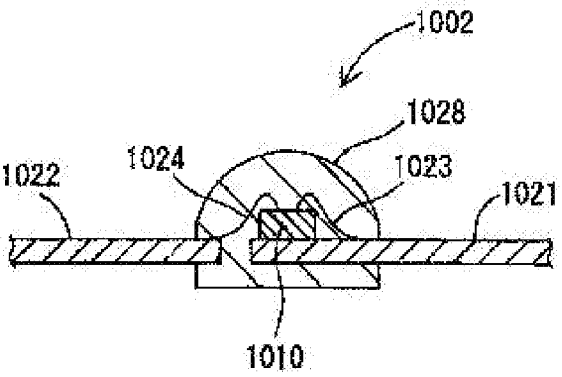


圖 33

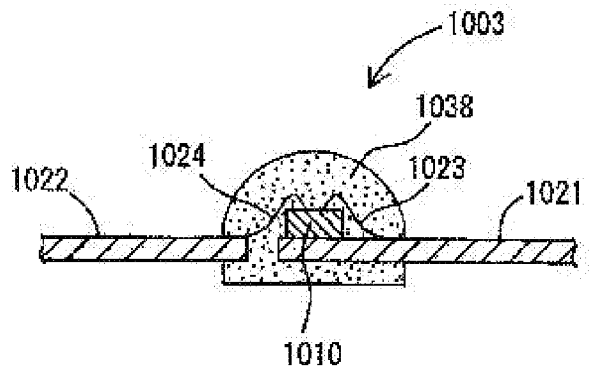


圖 34

圖式

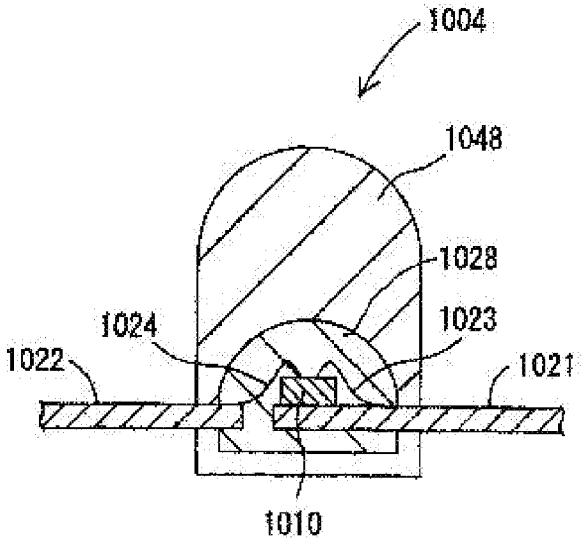


圖 35

圖式

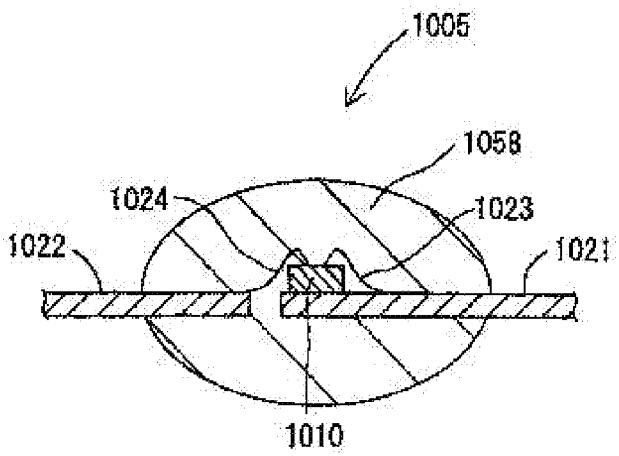


圖 36

圖式

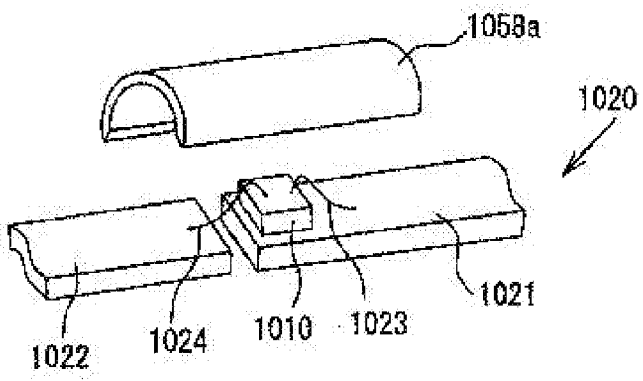


圖 37

圖式

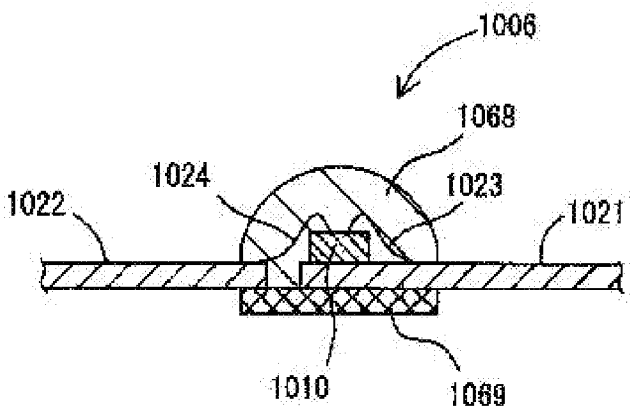


圖 38

圖式

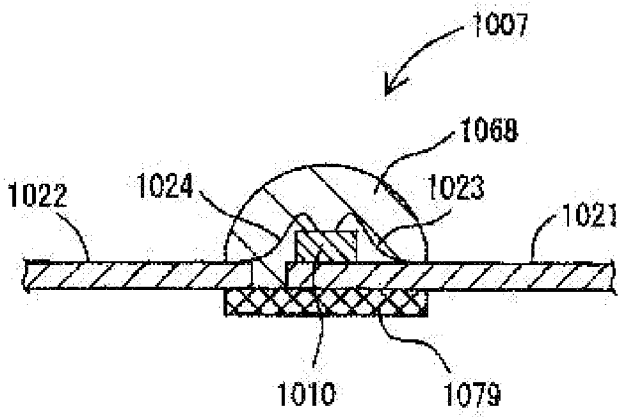


圖 39

圖式

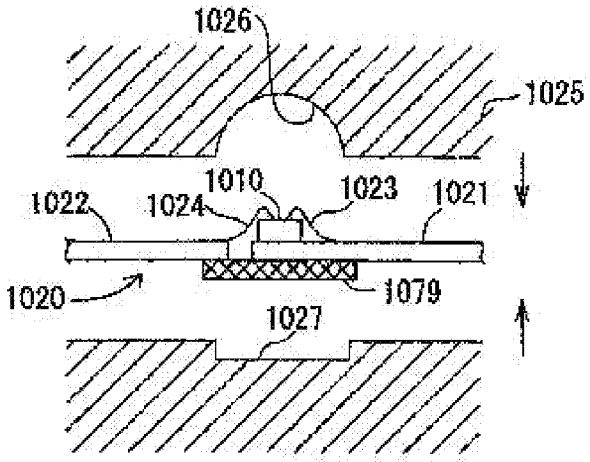


圖 40

圖式

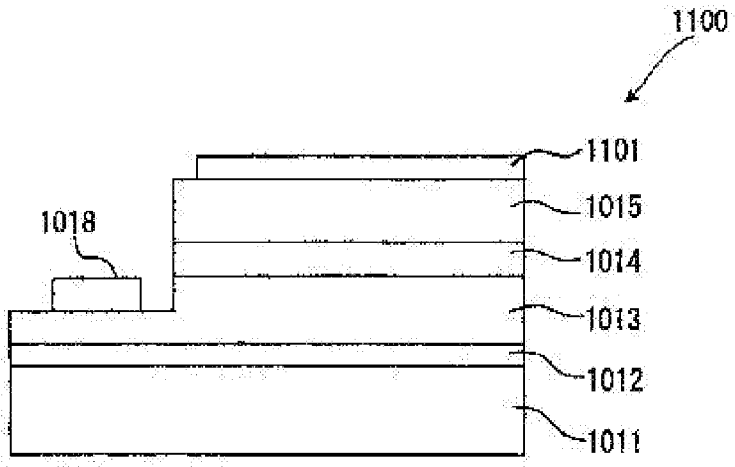


圖 41

圖式

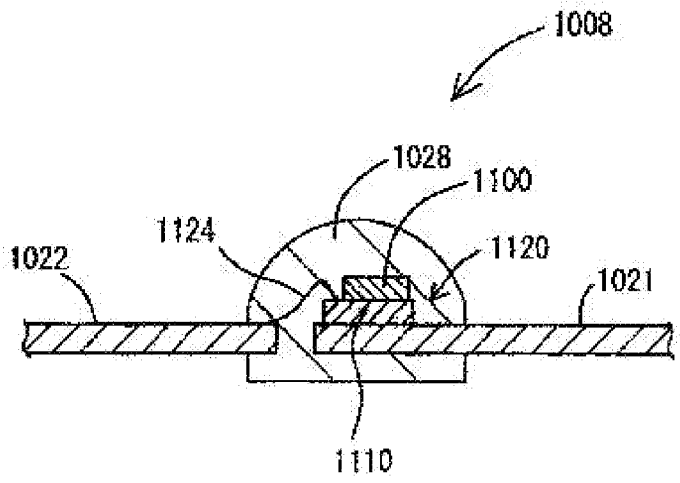


圖 42

圖式

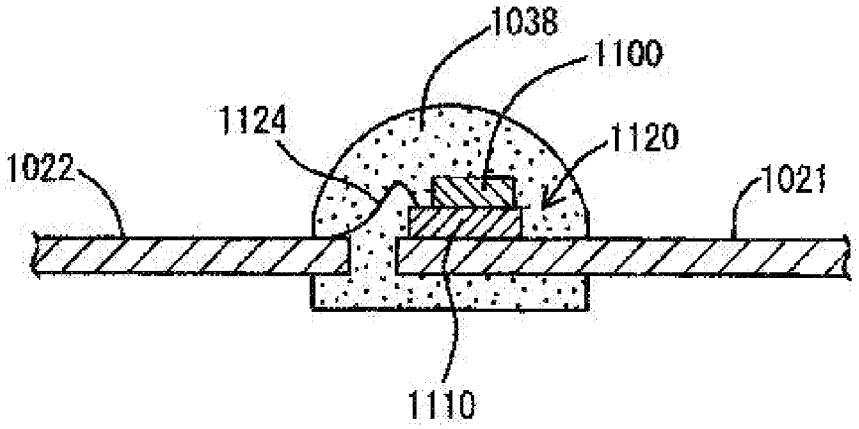


圖 43

圖式

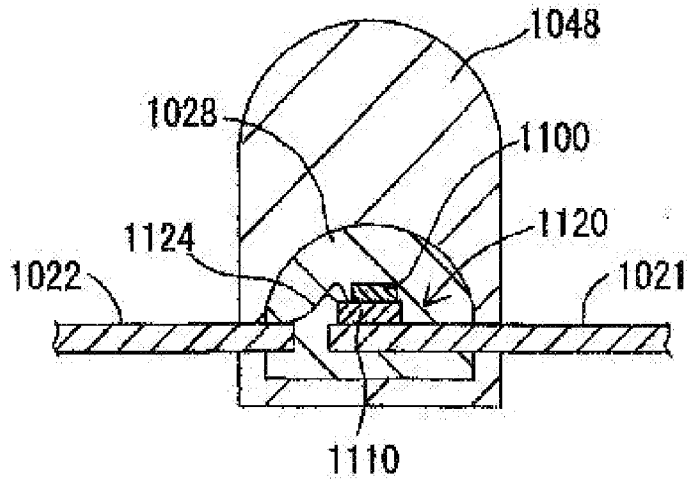


圖 44

圖式

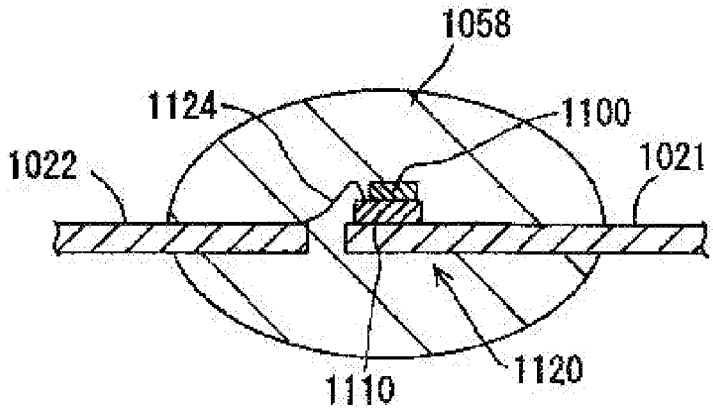


圖 45

圖式

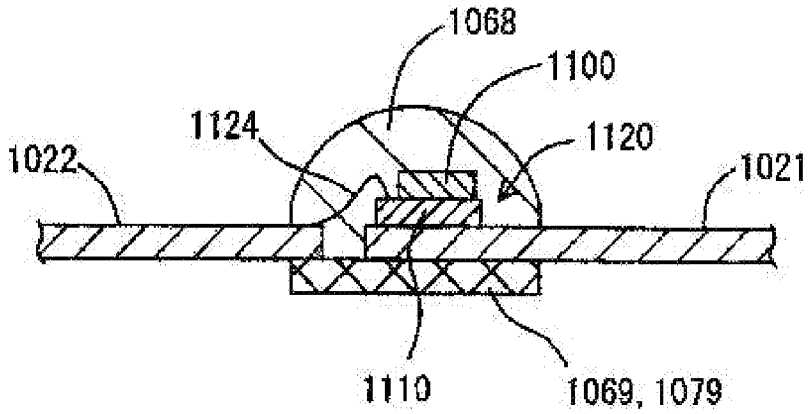


圖 46

圖式

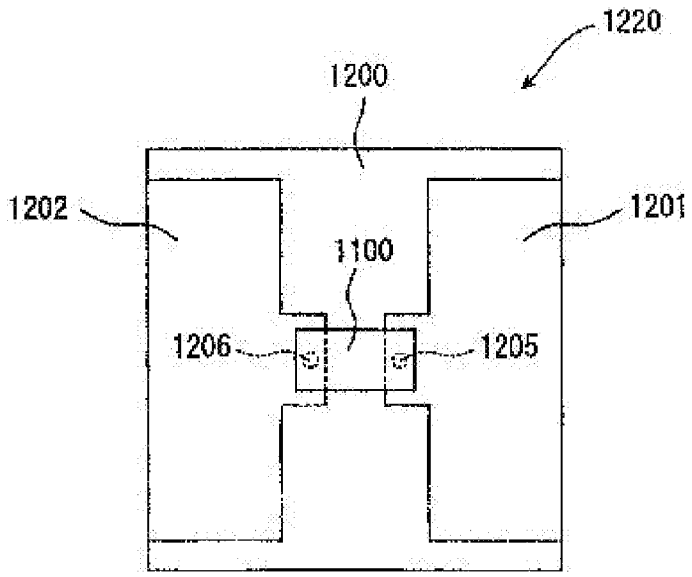


圖 47

圖式

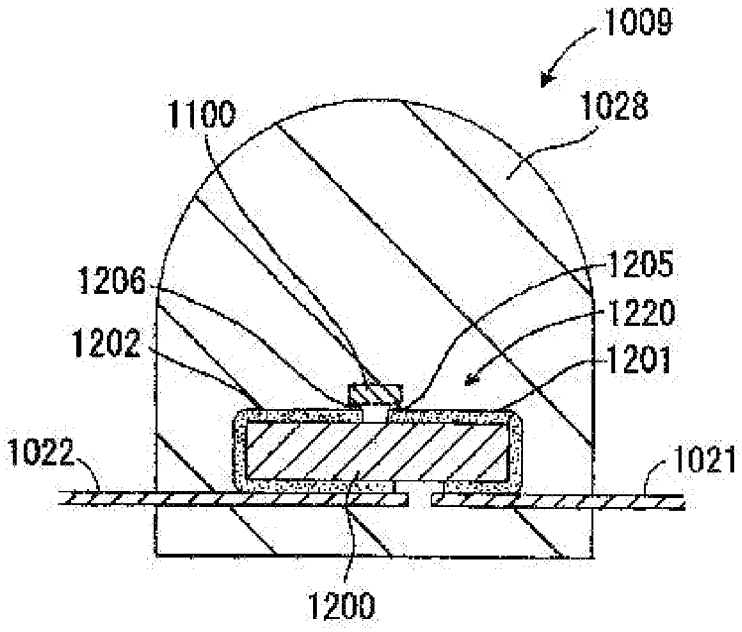


圖 48

圖式

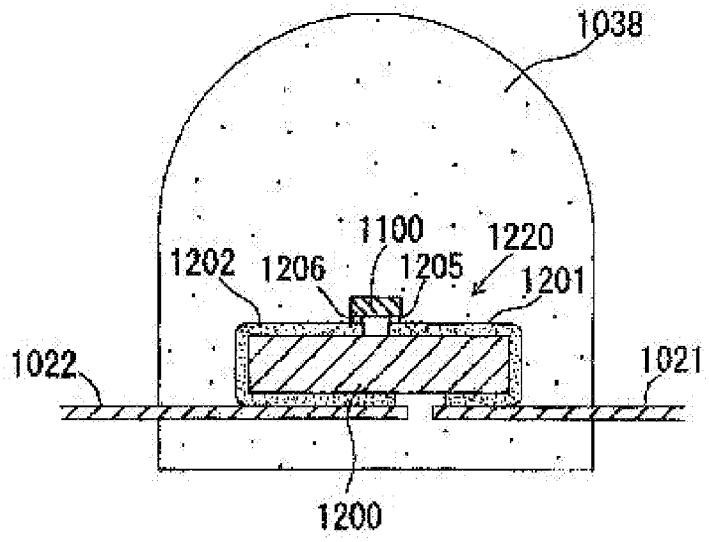


圖 49

圖式

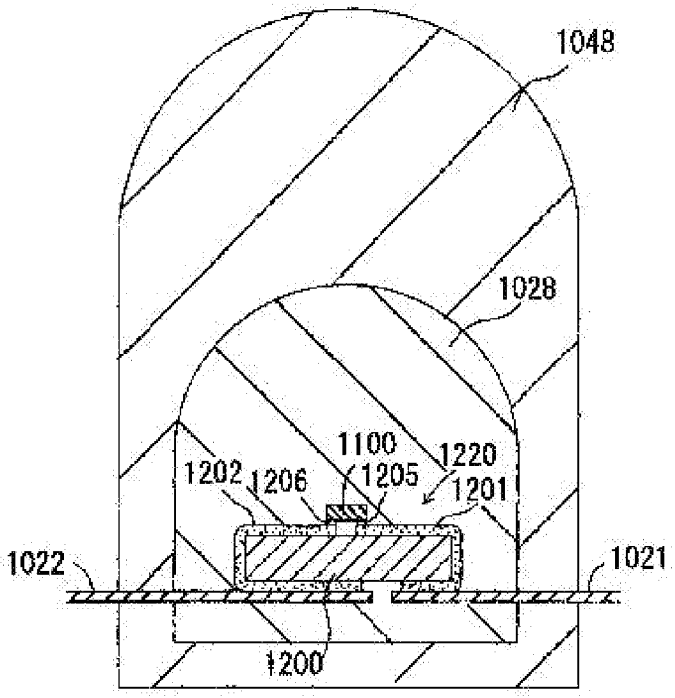


圖 50

圖式

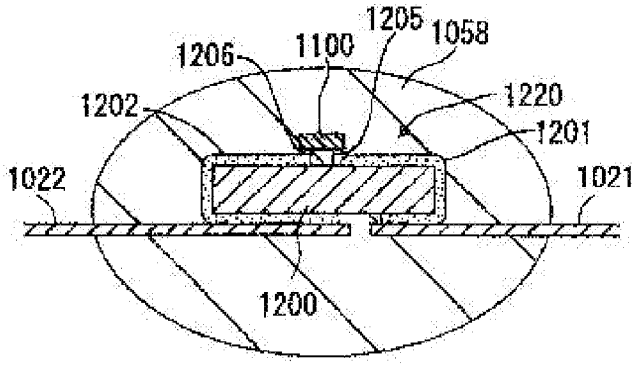


圖 51

圖式

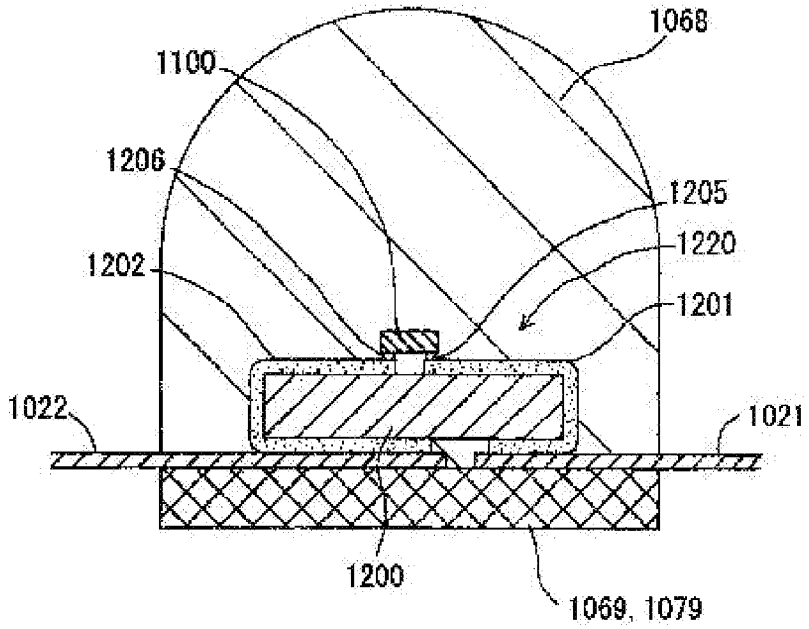


圖 52

圖式

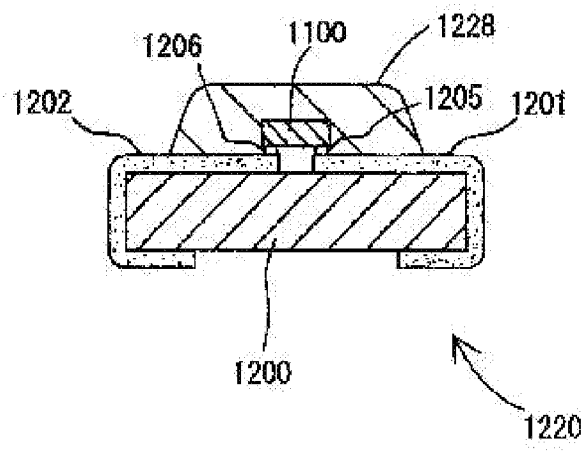


圖 53

圖式

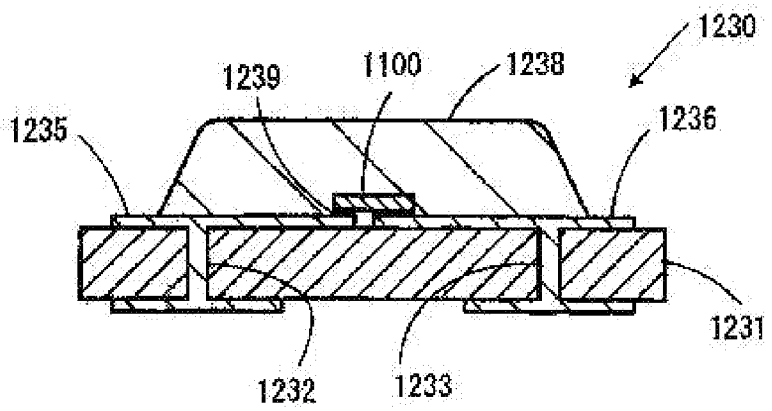


圖 54

圖式

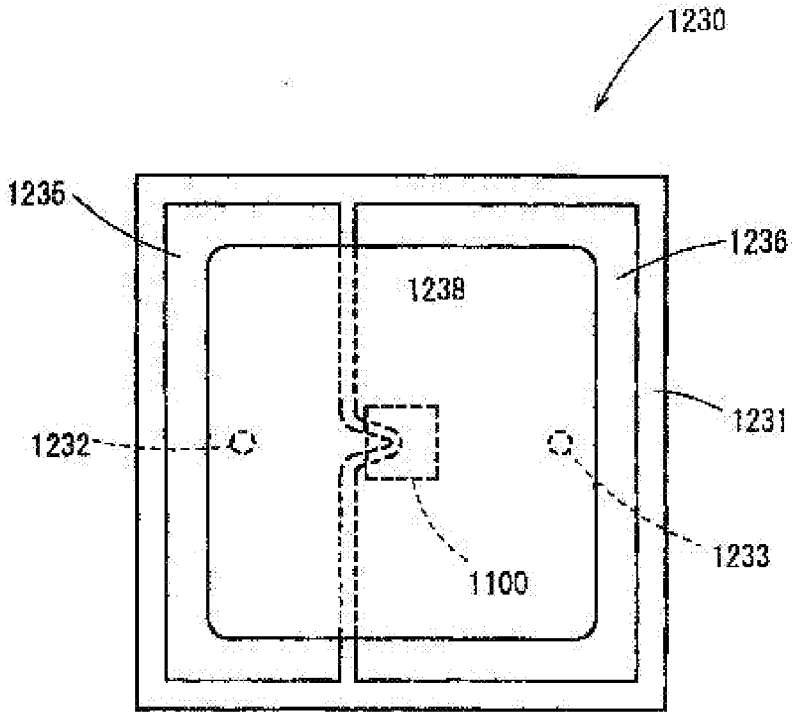


圖 55

圖式

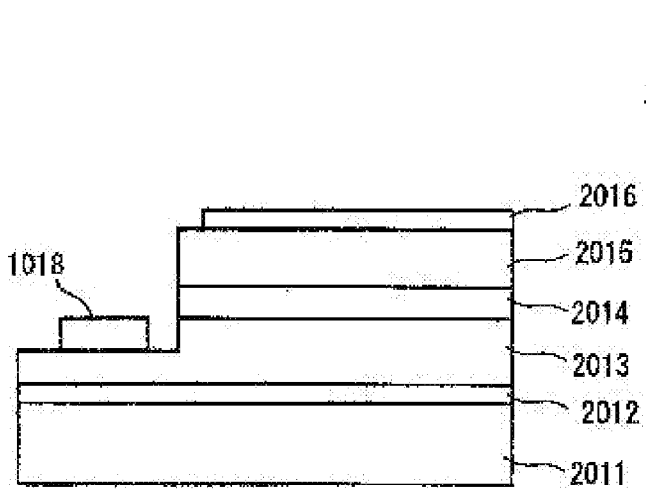


圖 56

圖式

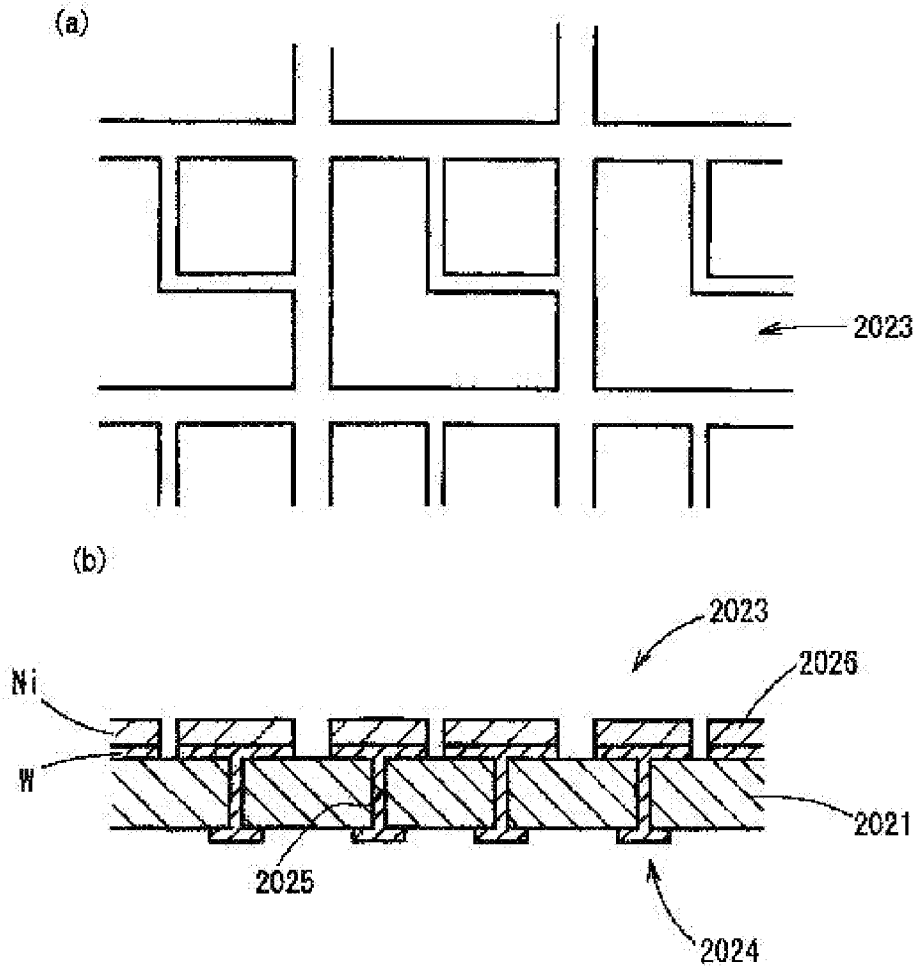


圖 57

圖式

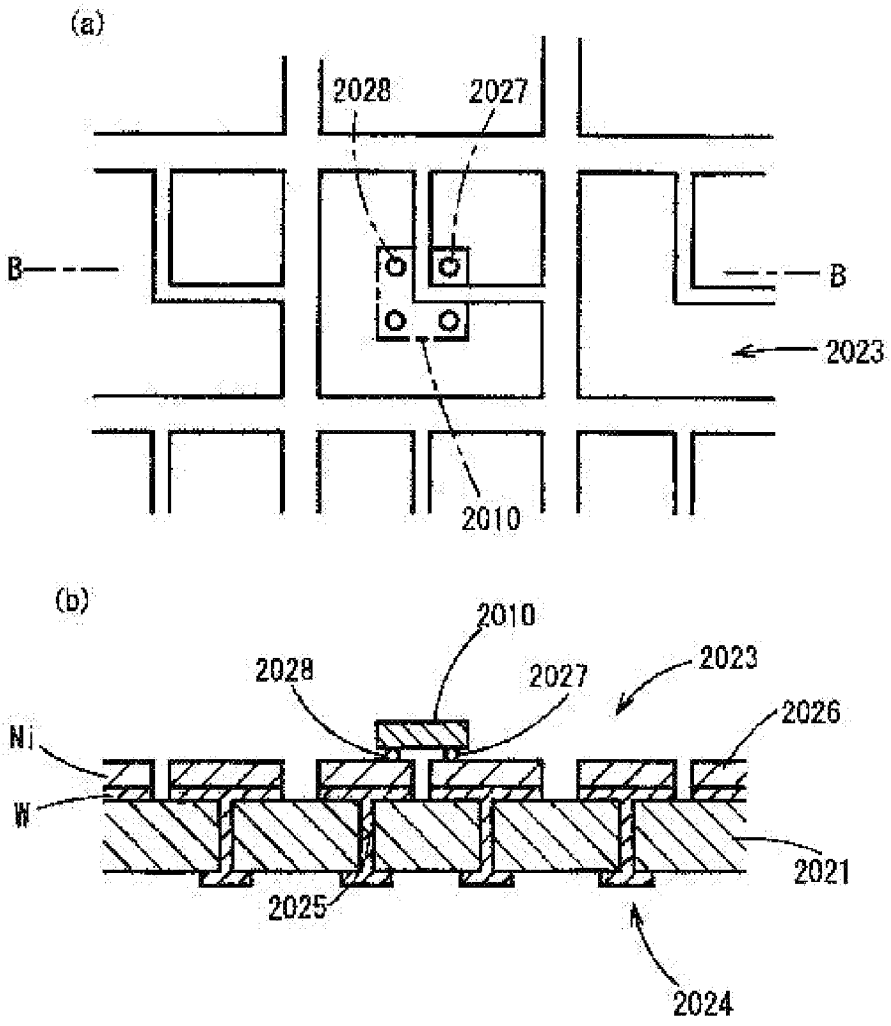

(a)
2028
2027
B
B
2023
2010
(b)
2010
2028
2027
2023
2026
Ni
W
2021
2025
2024

圖 58

圖式

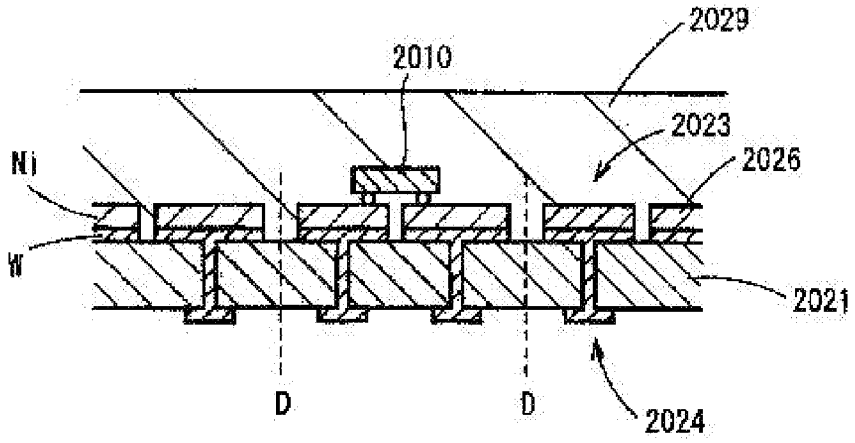


圖 59

圖式

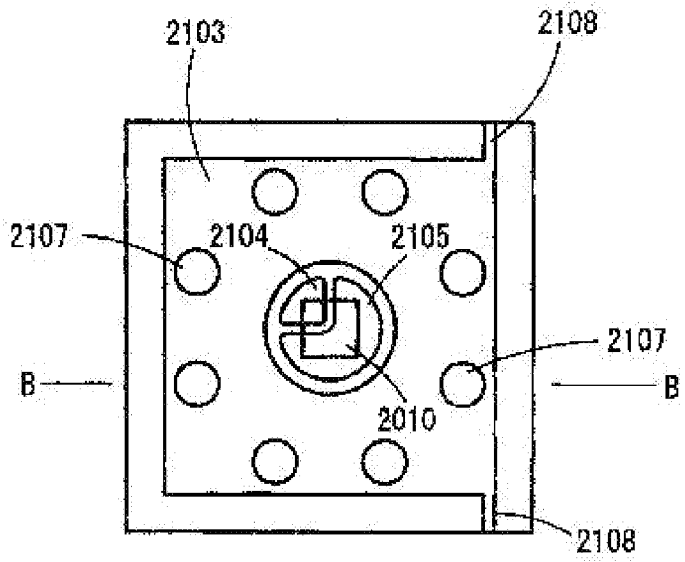


圖 60

圖式

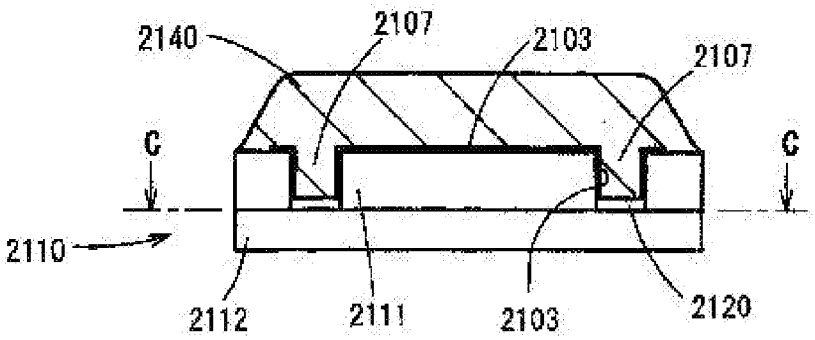


圖 61

圖式

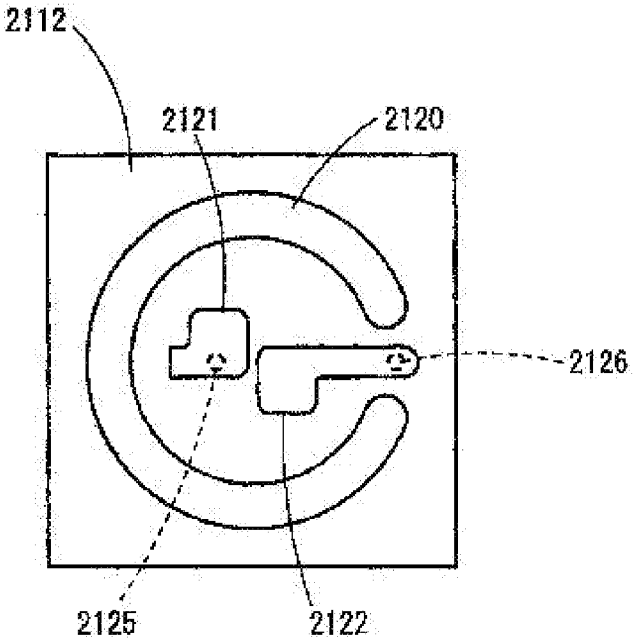


圖 62

圖式

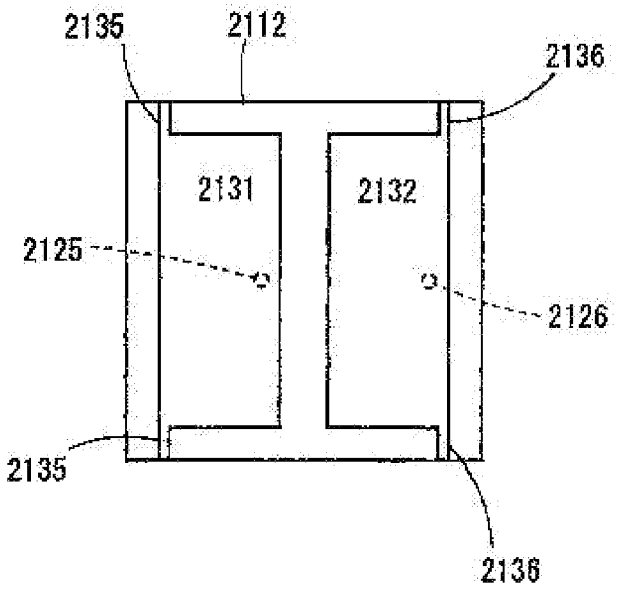


圖 63

圖式

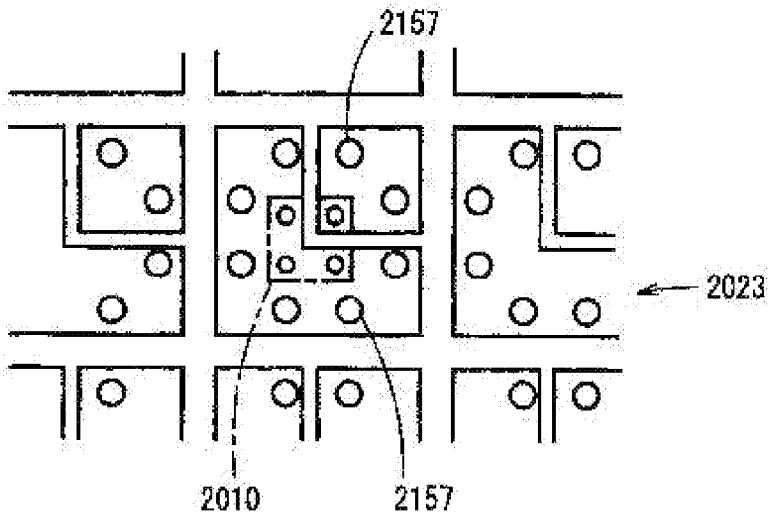


圖 64

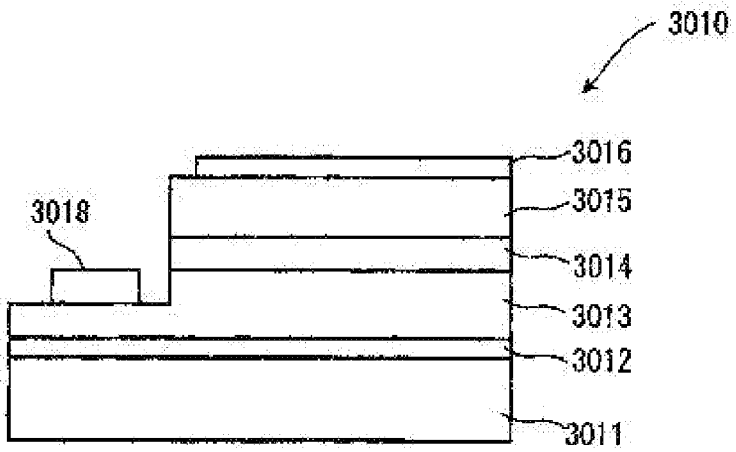


圖 65

圖式

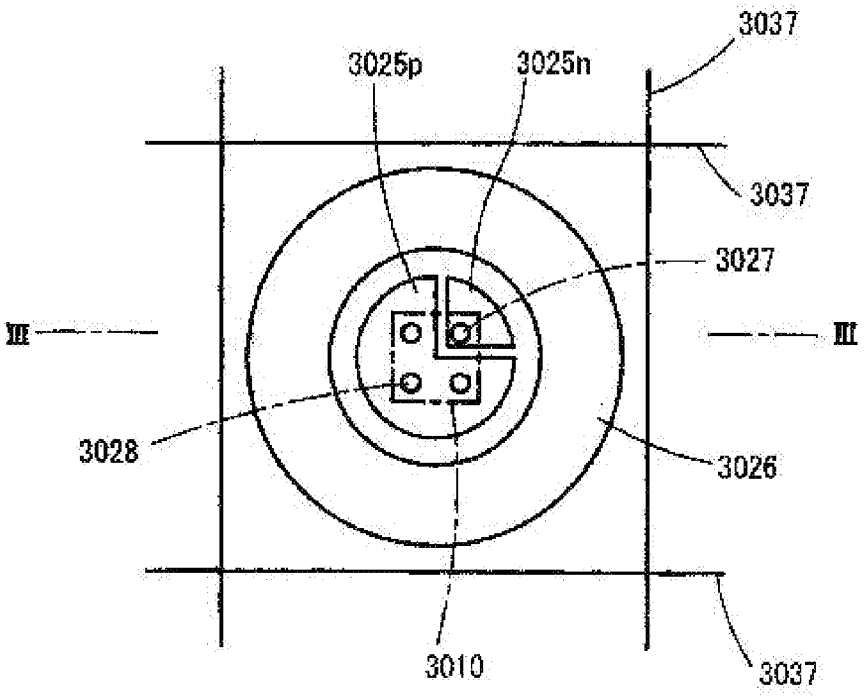


圖 66

圖式

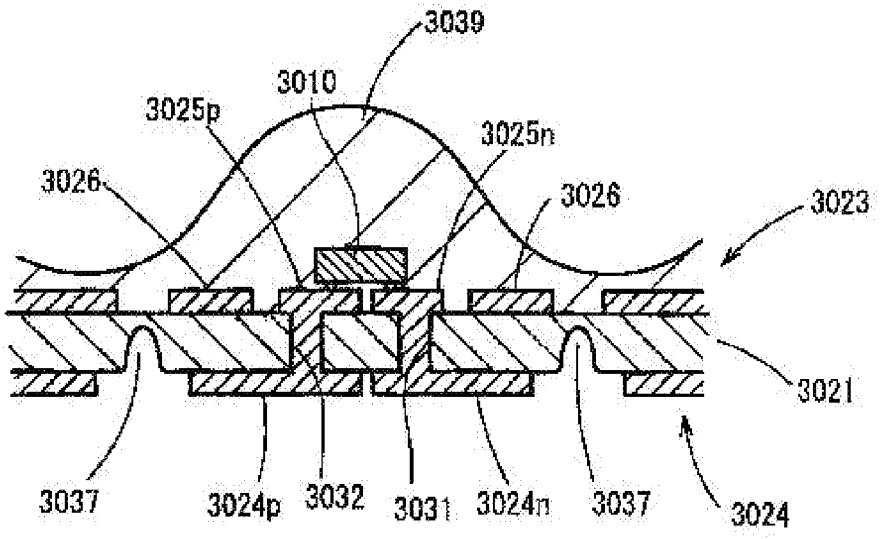

3039
3010
3025p
3025n
3026
3026
3023
3021
3037
3024p
3032
3031
3024n
3037
3024

圖 67

圖式

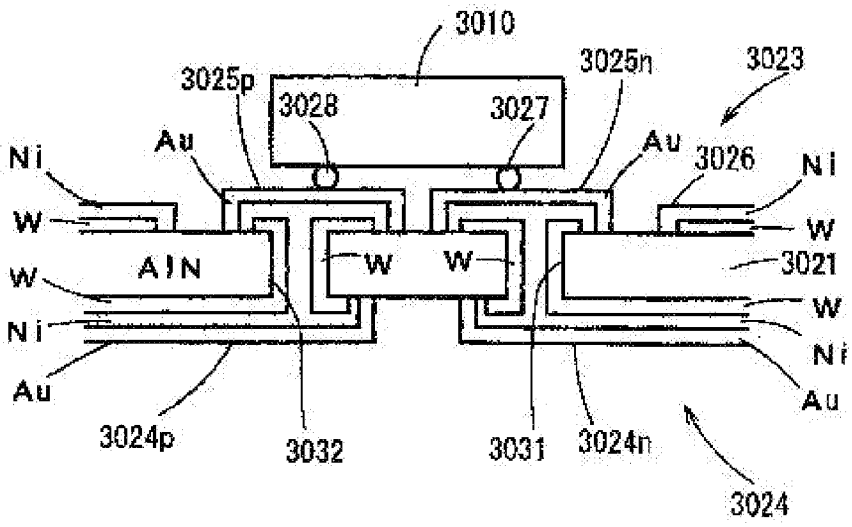

3010
3025p
3028
3027
3025n
3023
Au
Au
3026
Ni
Ni
W
W
AlN
W
W
3021
W
W
Ni
Ni
Au
Au
3024p
3032
3031
3024n
3024

圖 68

圖式

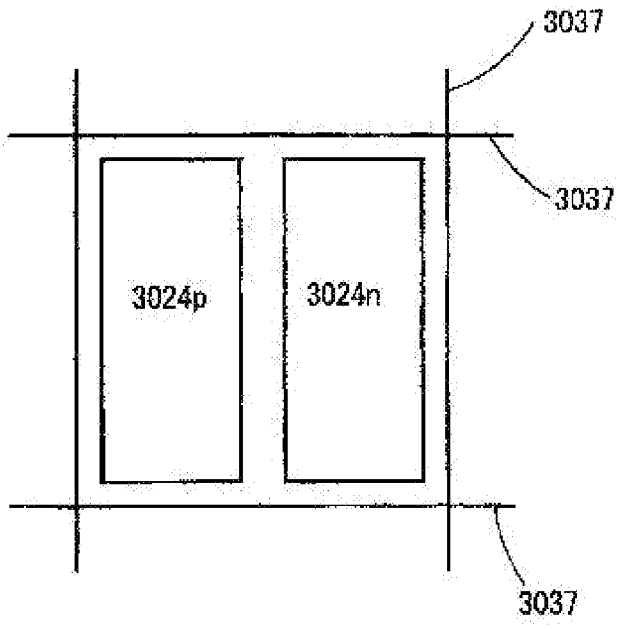


圖 69

圖式

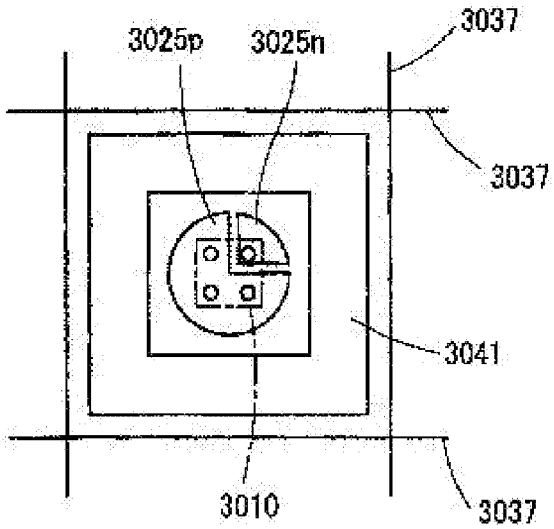


圖 70

圖式

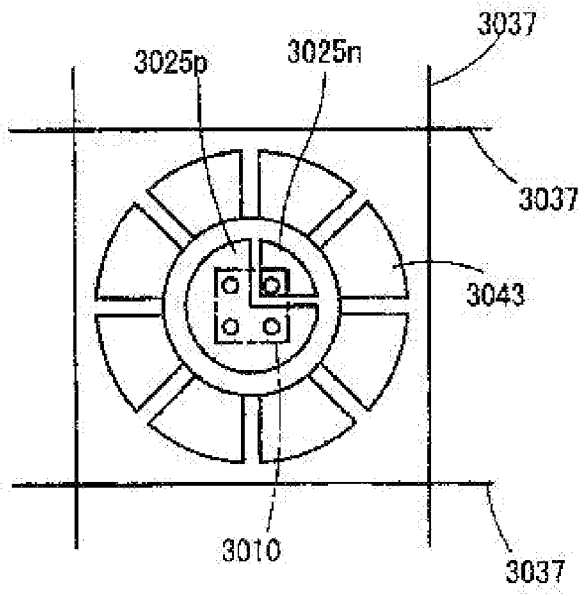


圖 71

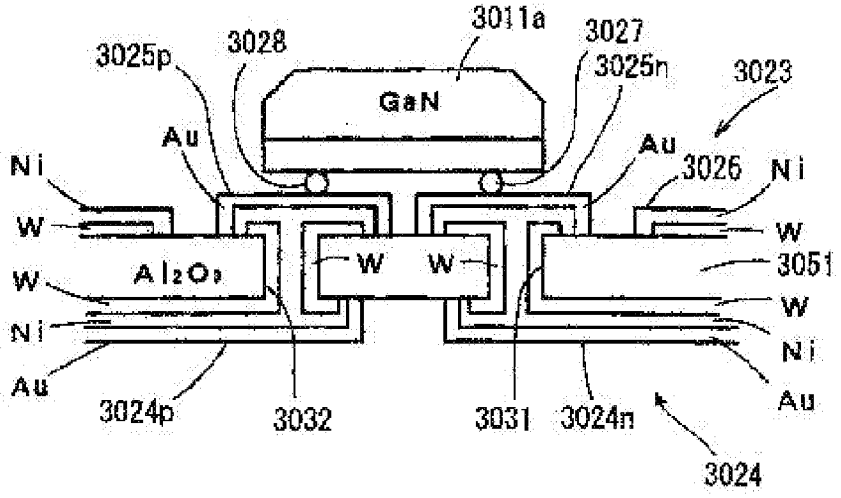

3011a
3027
3025p
3028
3025n
3023
GaN
Au
Au
Ni
3026
Ni
W
W
W
W
3051
Al_2O_3
W
W
Ni
Ni
Au
Au
3024p
3032
3031
3024n
3024

圖 72

圖式

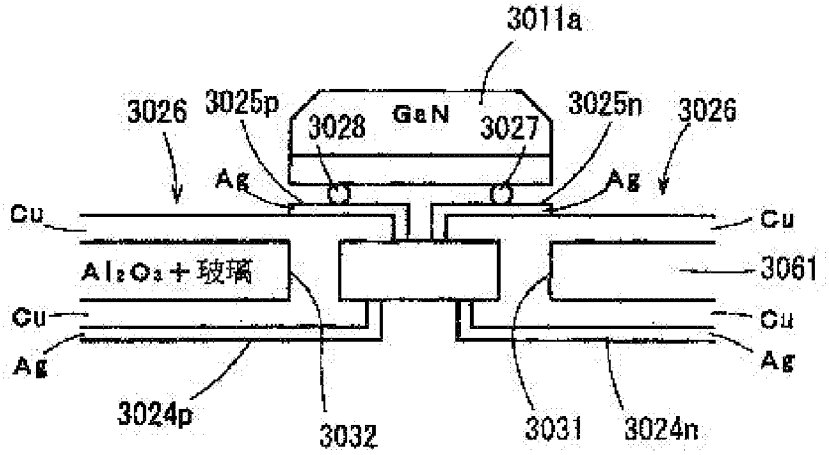

3011a
3026
3025p
3028
GaN
3027
3025n
3026
Ag
Ag
Cu
Cu
Al_2O_3＋玻璃
3061
Cu
Cu
Ag
Ag
3024p
3032
3031
3024n

圖 73

圖式

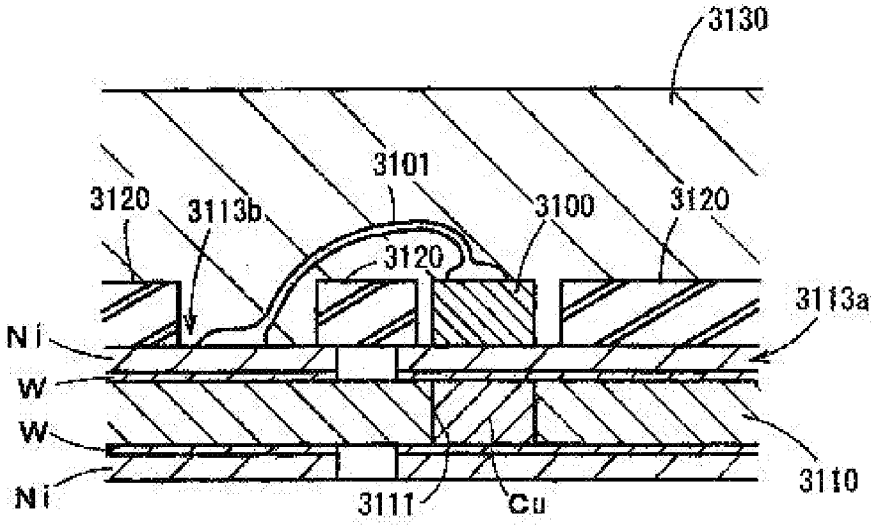

3130
3101
3120
3113b
3100
3120
3120
3113a
Ni
W
W
Ni
3111
Cu
3110

圖 74

圖式

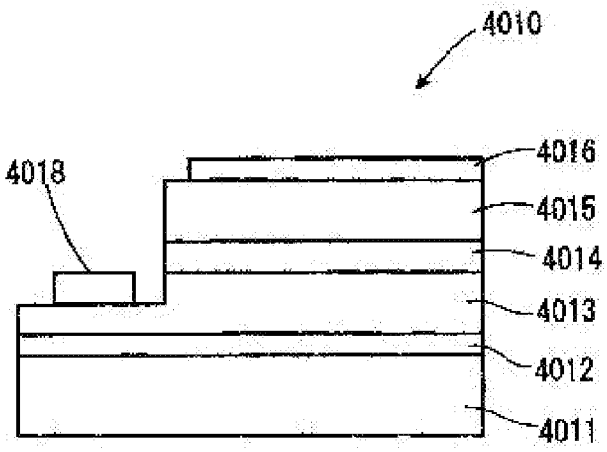


圖 75

圖式

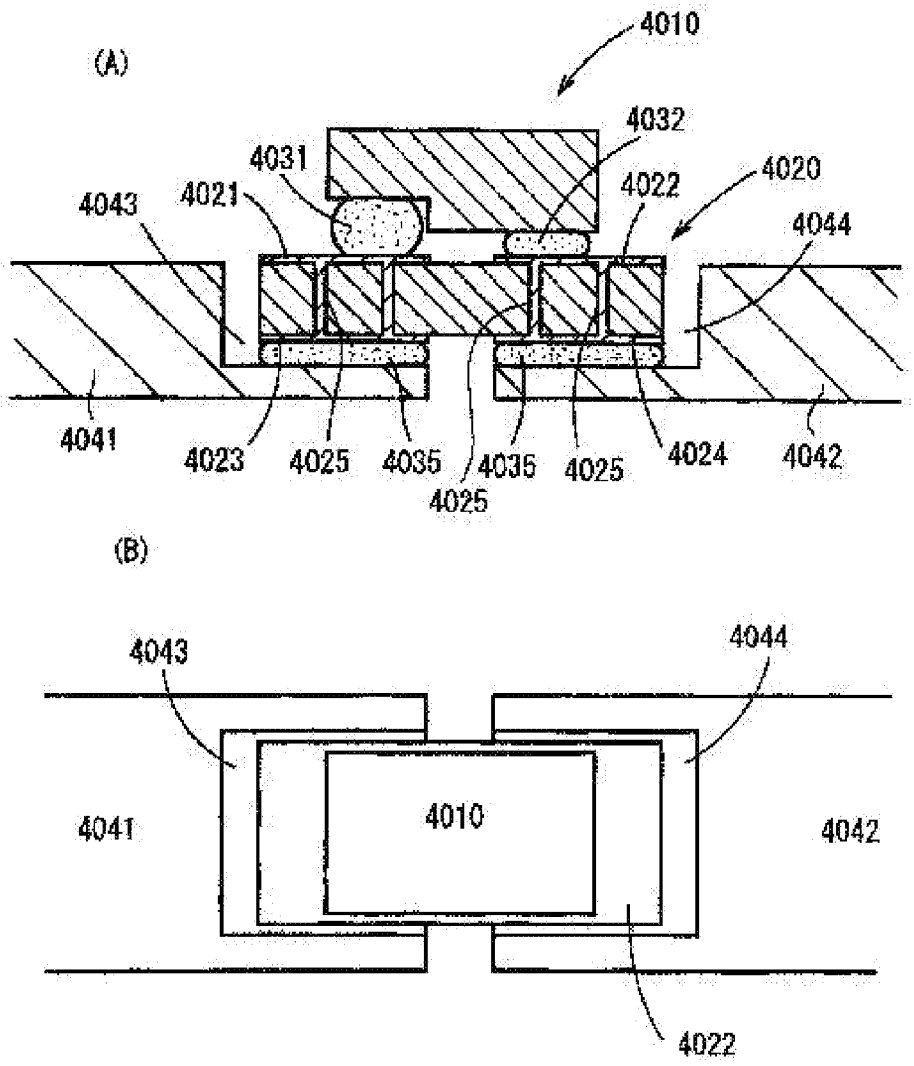

(A)
4010
4032
4031
4020
4021
4022
4043
4044
4041
4023
4025
4035
4035
4025
4024
4042
4025
(B)
4043
4044
4041
4010
4042
4022

圖 76

圖式

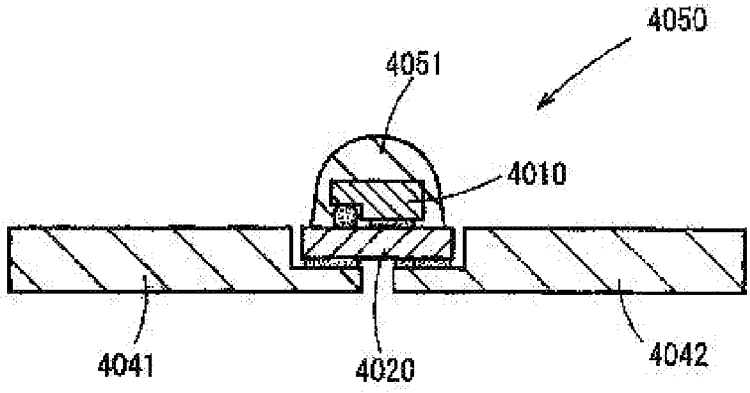


圖 77

圖式

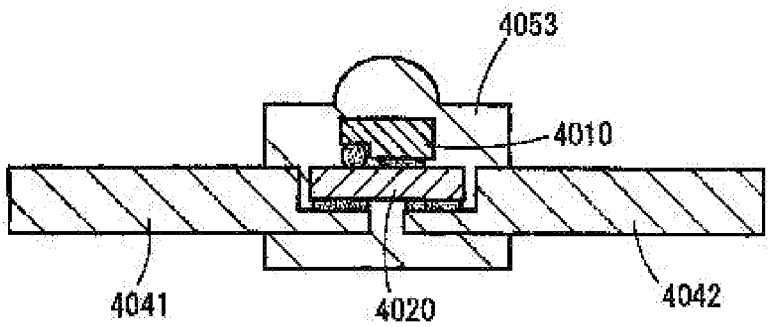


圖 78

圖式

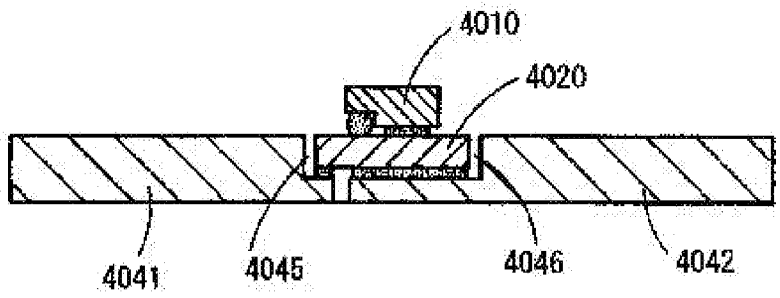


圖 79

圖式

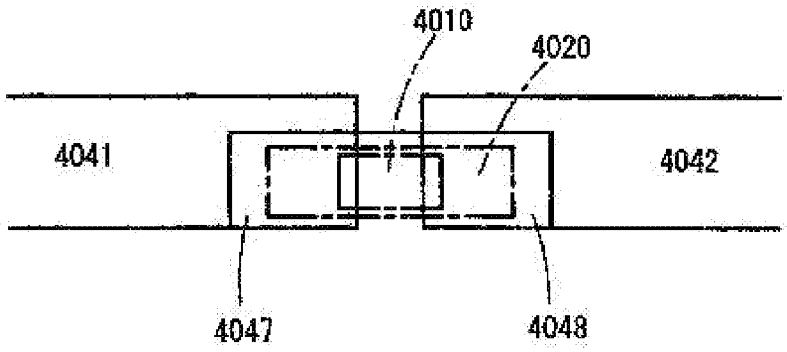


圖 80

圖式

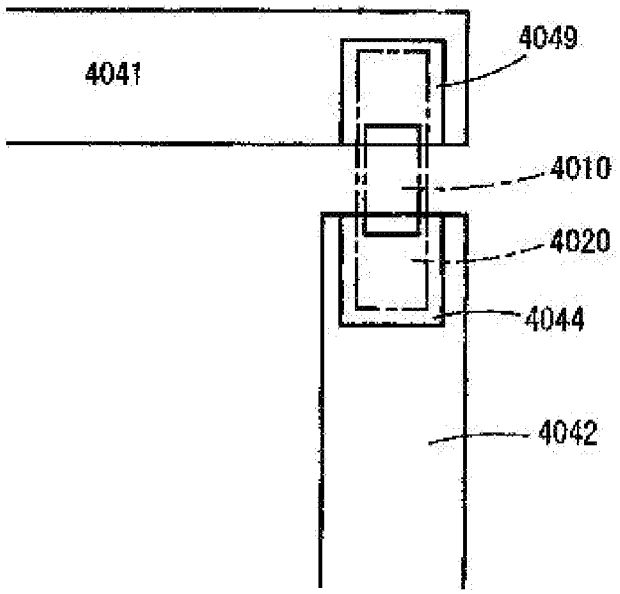


圖 81

圖式

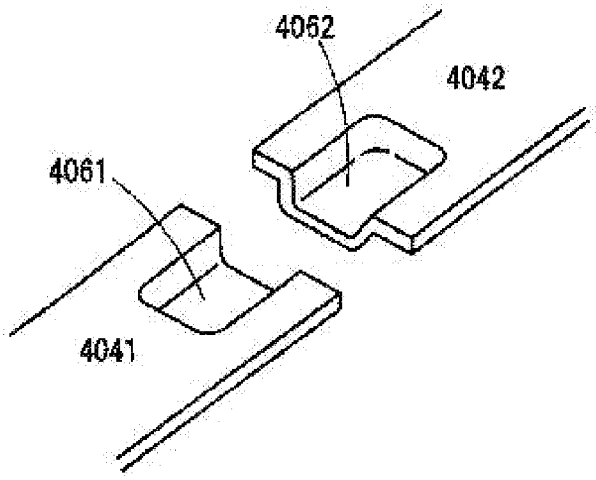


圖 82

圖式

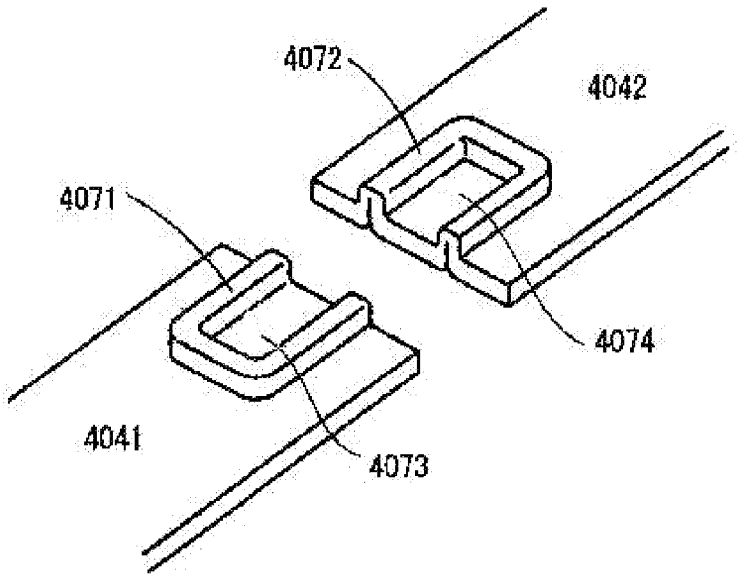


圖 83

圖式

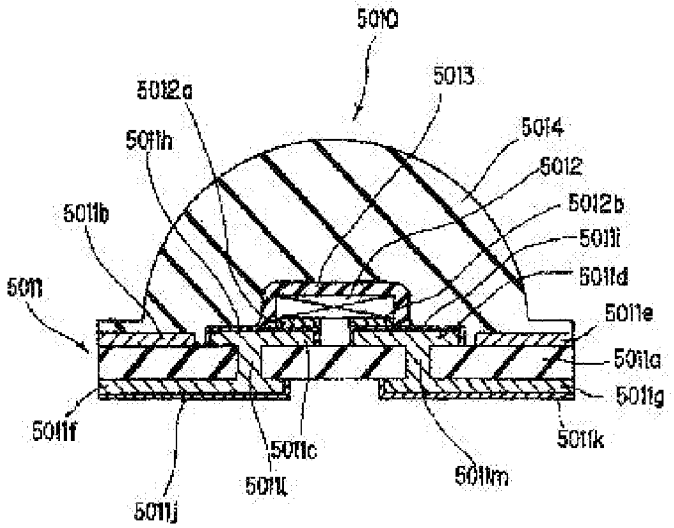

5010
5013
5012a
5011h
5014
5012
5012b
5011b
5011i
5011d
5011
5011e
5011a
5011g
5011f
5011k
5011c
5011l
5011m
5011j

圖 84

圖式

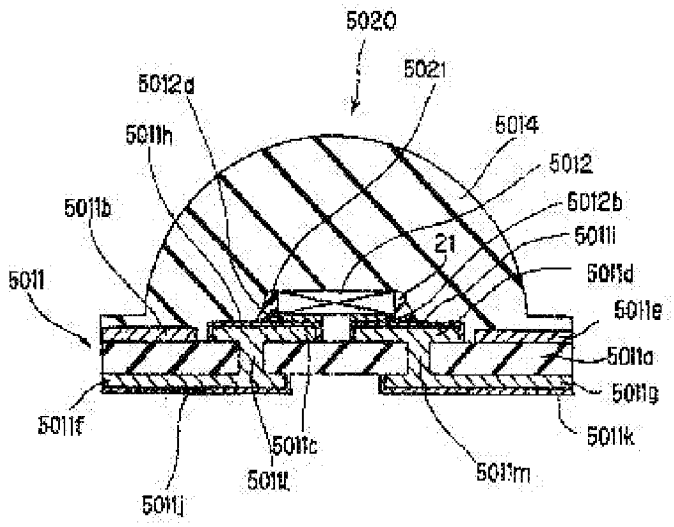

5020
5021
5012a
5011h
5014
5012
5011b
5012b
5011i
21
5011d
5011
5011e
5011a
5011g
5011f
5011c
5011k
5011l
5011m
5011j

圖 85

圖式

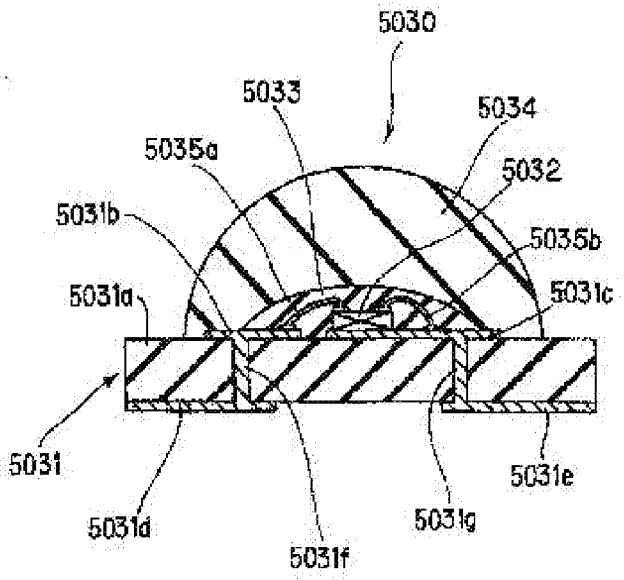

5030
5033
5034
5035a
5032
5031b
5035b
5031a
5031c
5031
5031d
5031f
5031g
5031e

圖 86

圖式

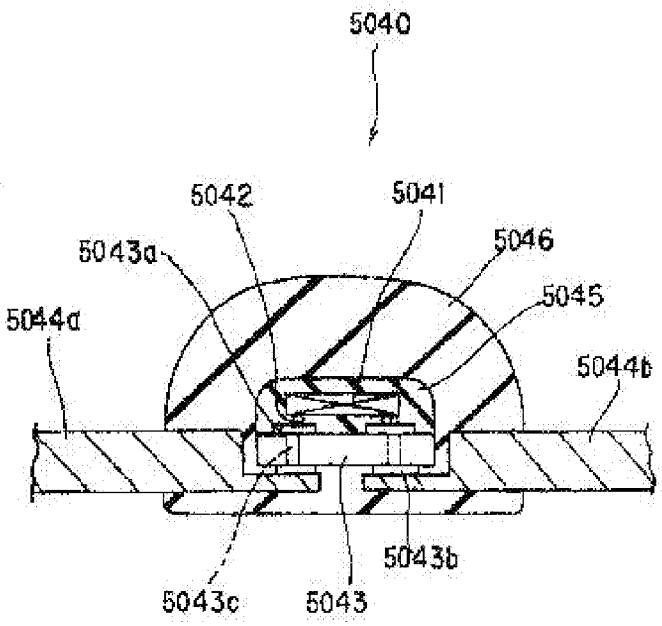


圖 87

副式

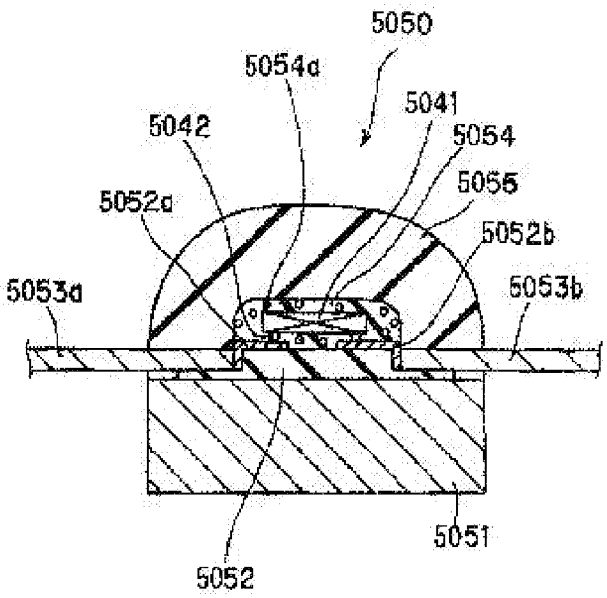

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5042
5054
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5052a
5052b
5053a
5053b
5051
5052

圖 88

圖式

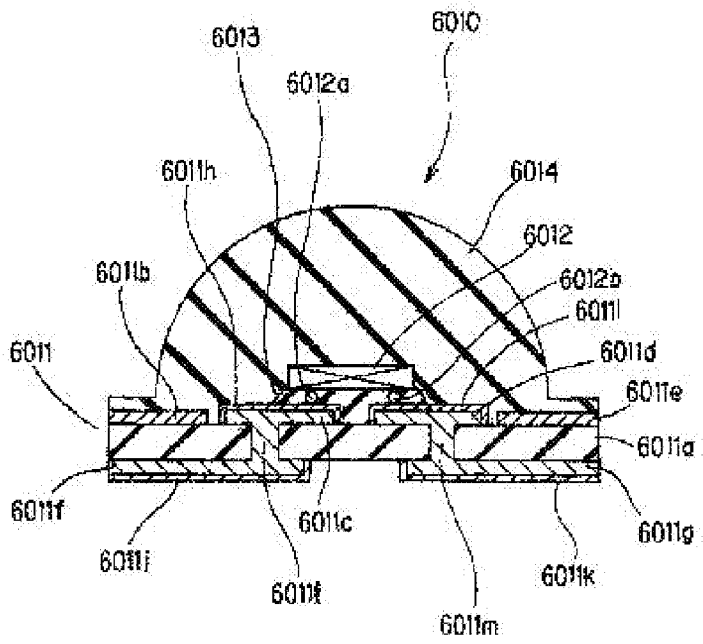

6013
6012a
6010
6011h
6014
6012
6011b
6012b
6011l
6011
6011d
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6011a
6011f
6011j
6011c
6011g
6011k
6011i
6011m

圖 89

圖式

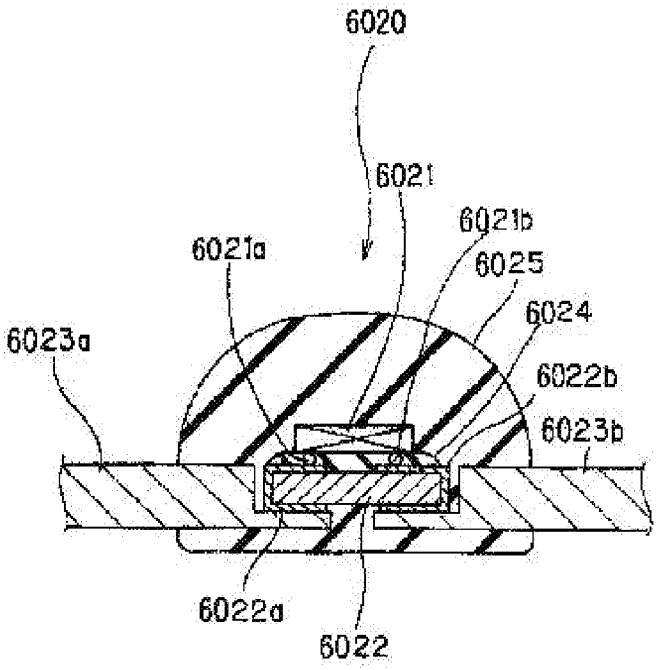

6020
6021
6021b
6021a
6025
6024
6023a
6022b
6023b
6022a
6022

圖 90

圖式

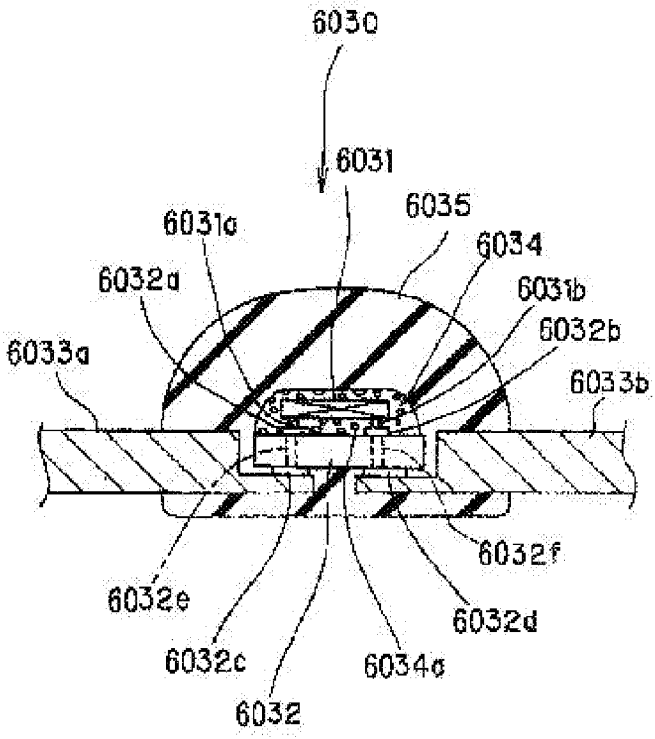

6030
6031
6035
6031a
6034
6032a
6031b
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6033a
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6034a
6032

圖 91

圖式

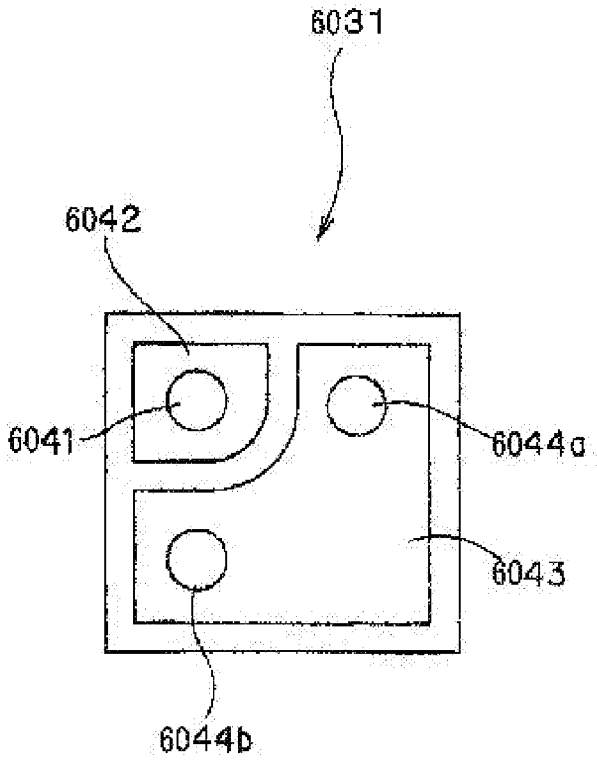


圖 92

圖式

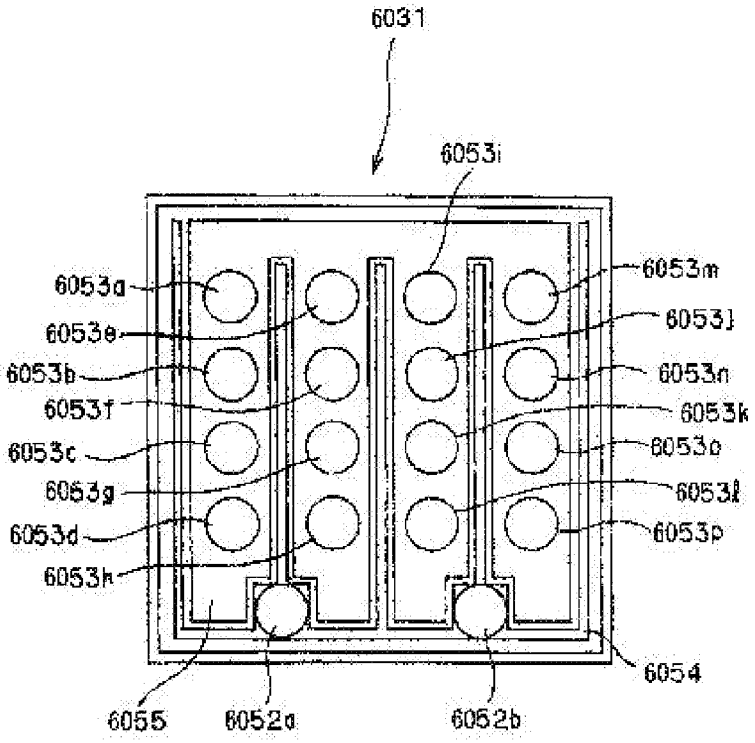

6031
6053i
6053a
6053e
6053b
6053f
6053c
6053g
6053d
6053h
6053m
6053j
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6053k
6053o
6053l
6053p
6054
6055
6052a
6052b

圖 93

圖式

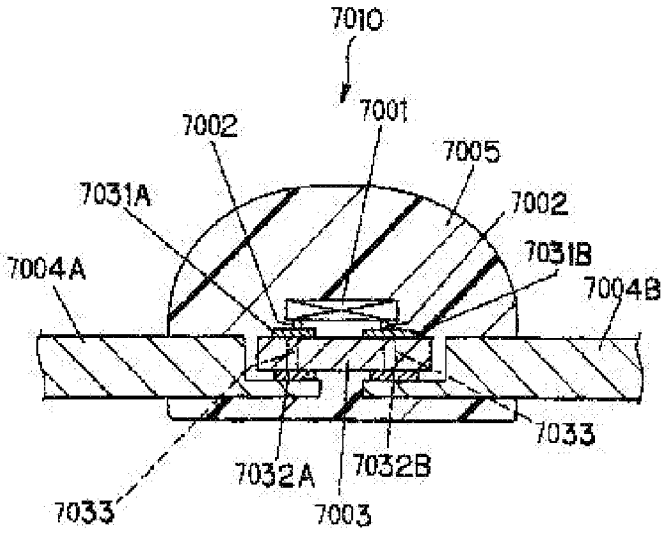

7010
7001
7002
7005
7031A
7002
7031B
7004A
7004B
7033
7032A
7032B
7033
7003

圖 94

圖式

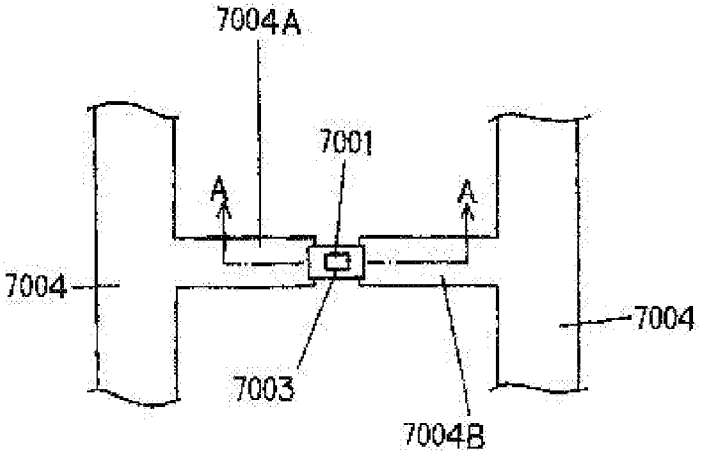


圖 95

圖式

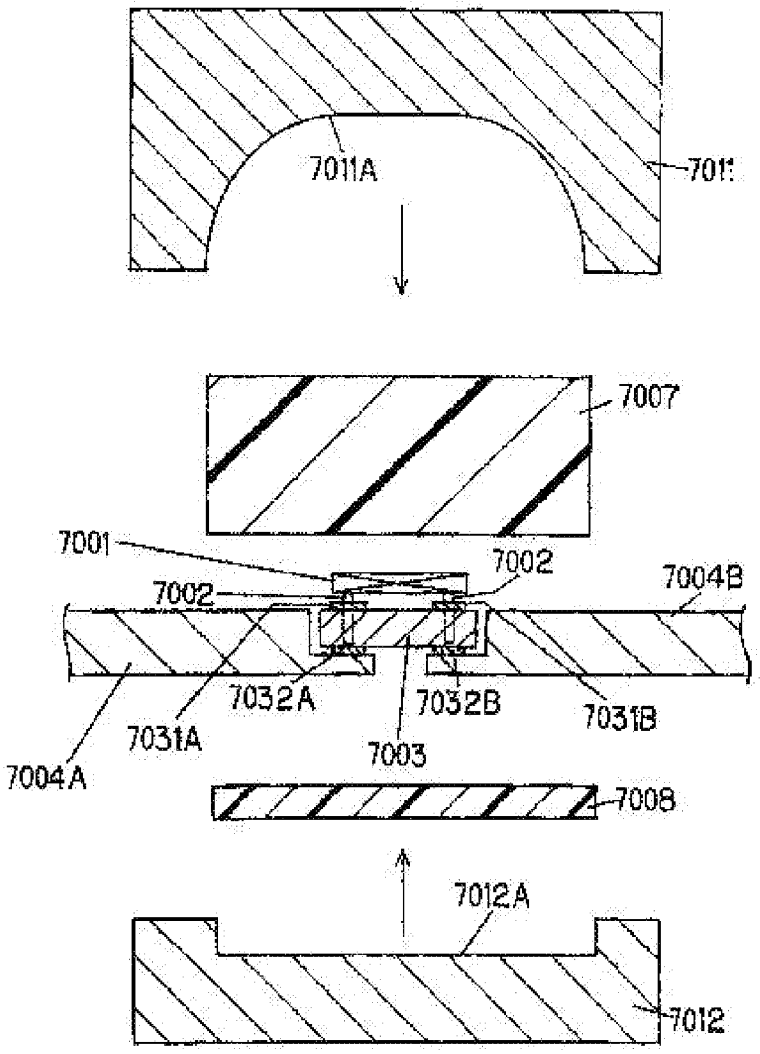

7011A
7011
7007
7001
7002
7002
7004B
7032A
7032B
7031B
7031A
7003
7004A
7008
7012A
7012

圖 96

圖式

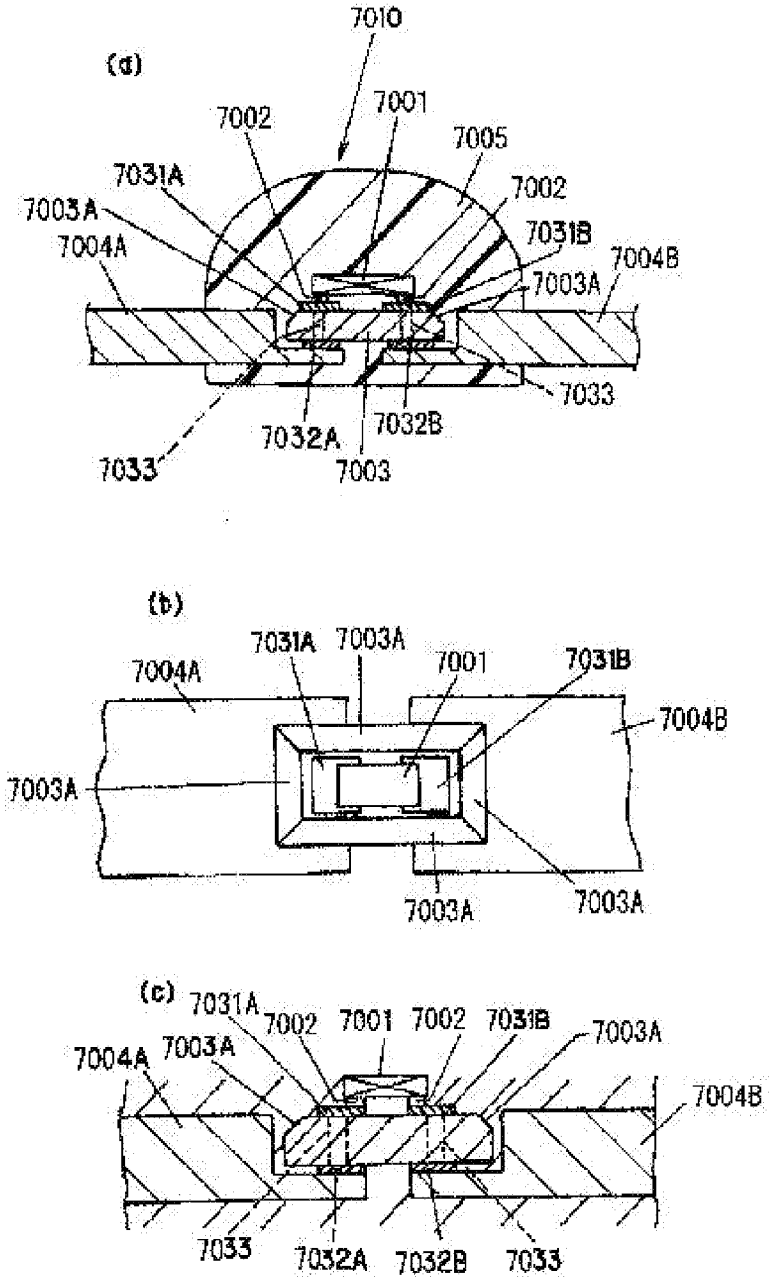

(a)
7010
7001
7002
7005
7031A
7002
7003A
7031B
7004A
7004B
7003A
7033
7032A
7032B
7033
7003
(b)
7031A
7003A
7001
7031B
7004A
7004B
7003A
7003A
7003A
(c)
7031A
7002
7001
7002
7031B
7003A
7004A
7003A
7004B
7033
7032A
7032B
7033

圖 97

圖式

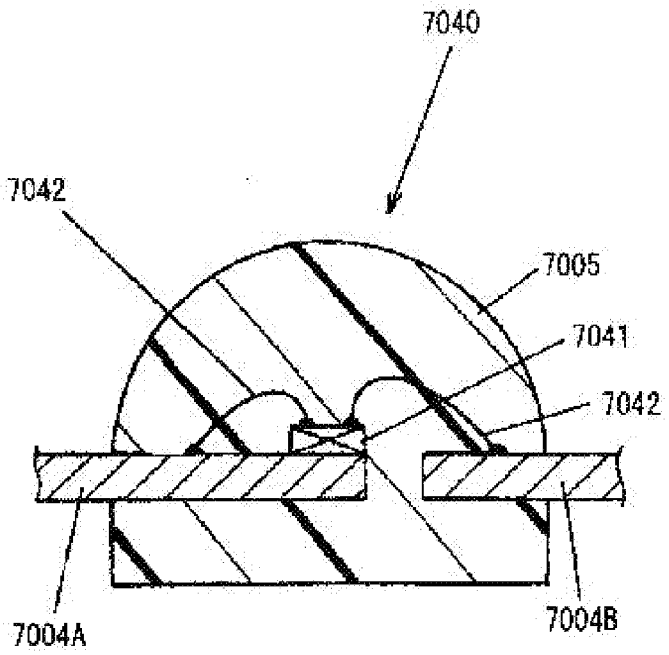


圖 98

圖式

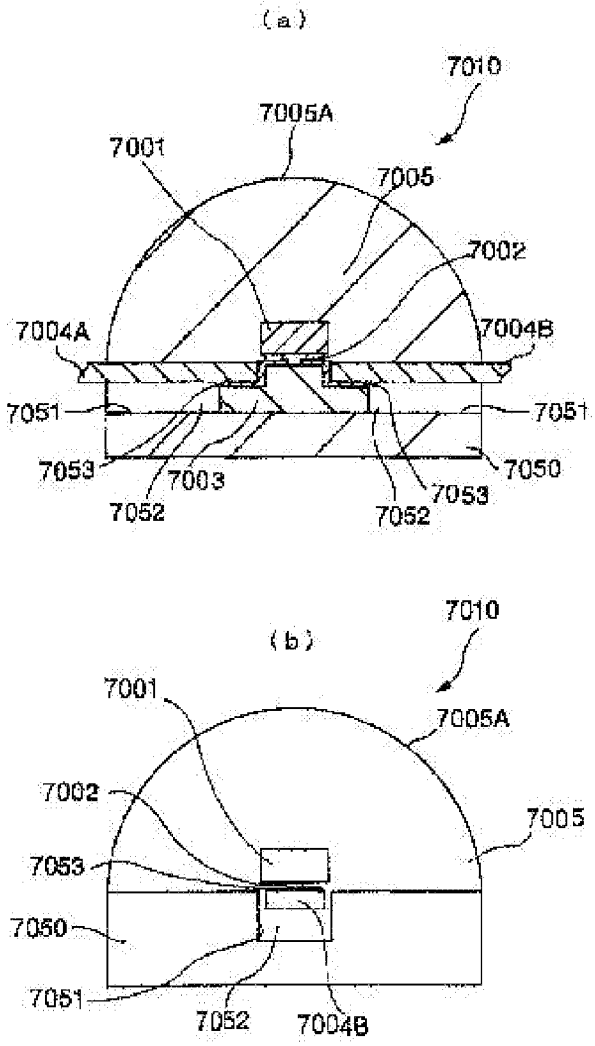
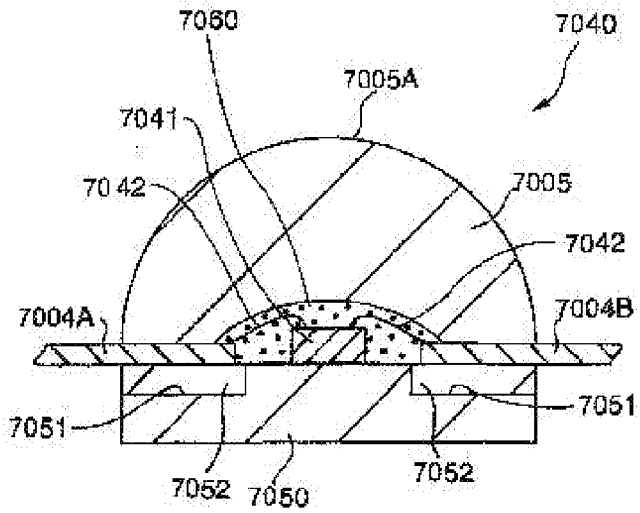

(a)
7010
7005A
7001
7005
7002
7004A
7004B
7051
7051
7053
7003
7050
7052
7052
7053
(b)
7010
7001
7005A
7002
7005
7053
7050
7051
7052
7004B

圖 99

圖式

(a)


7060
7040
7005A
7041
7042
7005
7042
7004A
7004B
7051
7051
7052
7050
7052

(b)

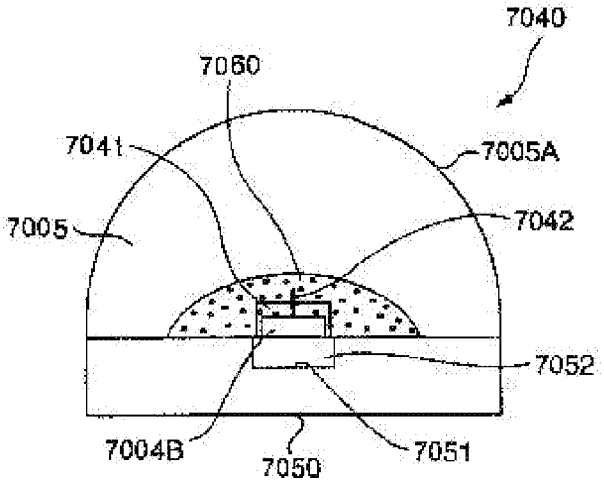

7040
7060
7041
7005A
7005
7042
7052
7004B
7050
7051

圖 100

Electronic Acknowledgement Receipt

EFS ID:	13263258
Application Number:	12745878
International Application Number:	
Confirmation Number:	4953
Title of Invention:	SLIM LED PACKAGE
First Named Inventor/Applicant Name:	Eun Jung Seo
Customer Number:	58027
Filer:	Hae-Chan Park/JungAh Kim
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P3962US00
Receipt Date:	16-JUL-2012
Filing Date:	02-JUN-2010
Time Stamp:	20:00:25
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	2012-07-16_P3962US00_IDS-SB08.pdf	392307 973b329a015c7c8a17648e38188e3af9133f364b	no	4

Warnings:	
Information:	

This is not an USPTO supplied IDS fillable form					
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Information:					
3	Foreign Reference	TW501276.pdf	1703478 14230379a2931fb5c9b282085146fc991d1ce946	no	18
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Warnings:					
Information:					
		Total Files Size (in bytes):	28187477		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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NOTICE OF ALLOWANCE AND FEE(S) DUE

58027 7590 08/01/2012
H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

EXAMINER
WILSON, ALLAN R

ART UNIT	PAPER NUMBER
2897	

DATE MAILED: 08/01/2012

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/745,878	06/02/2010	Eun Jung Seo	P3962US00	4953

TITLE OF INVENTION: SLIM LED PACKAGE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$300	$0	$2040	11/01/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

58027 7590 08/01/2012
H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/745,878	06/02/2010	Eun Jung Seo	P3962US00	4953

TITLE OF INVENTION: SLIM LED PACKAGE

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EXAMINER	ART UNIT	CLASS-SUBCLASS
WILSON, ALLAN R	2897	257-099000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/745,878	06/02/2010	Eun Jung Seo	P3962US00	4953

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SUITE 7500
VIENNA, VA 22182

EXAMINER	
WILSON, ALLAN R	

ART UNIT	PAPER NUMBER
2897	

DATE MAILED: 08/01/2012

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 205 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 205 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/745,878	SEO, EUN JUNG	
	Examiner	Art Unit	
	ALLAN R. WILSON	2897	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on 6/11/12 and the IDS filed on 7/20/12*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *1-5 and 7-17*.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 6/13/12, 7/16/12
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/ALLAN R WILSON/
Primary Examiner, Art Unit 2897

Election/Restrictions

Claims 1, 2, 5, 9, 13 and 17 are allowable. The restriction requirement between species, as set forth in the Office action mailed on 2/23/12, has been reconsidered in view of the allowability of claims to the elected invention pursuant to MPEP § 821.04(a). **The restriction requirement is hereby withdrawn as to any claim that requires all the limitations of an allowable claim.** Claims 3, 4, 7, 8, 10-12 and 14-16 directed to non-elected species are no longer withdrawn from consideration because the claim(s) requires all the limitations of an allowable claim.

In view of the above noted withdrawal of the restriction requirement, applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

Once a restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for the substance of this examiner's amendment was given in a telephone interview with Matthew Gill on 7/12/2012.

The application has been amended as follows:

Claim 1, last two lines, replace “the chip mounting recess and the groove are disposed in different regions of the first lead frame” with - -the chip mounting recess is not disposed directly above the groove- -.

Claim 18, cancelled.

Any inquiry concerning this communication or earlier communications from an examiner should be directed to Primary Examiner Allan Wilson whose telephone number is 571-272-1738. Examiner Wilson can normally be reached 7:00-4:00 Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Fernando Toledo can be reached on 571-272-1867. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Allan R. Wilson/
Primary Examiner, Art Unit 2897

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12745878	SEO, EUN JUNG
	Examiner	Art Unit
	ALLAN R WILSON	2815

SEARCHED			
Class	Subclass	Date	Examiner
257	98-100, 676, E33.059, E33.061, E33.066	6/28/12	AW
438	26, 123	6/28/12	AW

SEARCH NOTES		
Search Notes	Date	Examiner
See Examiner's search strategy and results – EAST Search History	6/28/12	AW

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
257	98-100, 676, E33.059, E33.061, E33.066	6/28/12	AW
438	26, 123	6/28/12	AW

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	12745878
Filing Date	2010-06-02
First Named Inventor	Eun Jung SEO
Art Unit	2897
Examiner Name	WILSON, ALLAN R
Attorney Docket Number	P3962US00

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/A.W./	1	20060220048		2006-10-05	Matsumoto et al.	
/A.W./	2	20030107316		2003-06-12	Murakami et al.	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
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Receipt date: 06/13/2012

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	12745878
Filing Date	2010-06-02
First Named Inventor	Eun Jung SEO
Art Unit	2897
Examiner Name	WILSON, ALLAN R
Attorney Docket Number	P3962US00

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
/A.W./	1	the Extended European Search Report of EP Application No. 08 85 6932.2 dated March 7, 2012.	☐

If you wish to add additional non-patent literature document citation information please click the Add button **Add**

EXAMINER SIGNATURE

Examiner Signature	/Allan Wilson/	Date Considered	06/27/2012

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

Receipt date: 06/13/2012

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	12745878
Filing Date	2010-06-02
First Named Inventor	Eun Jung SEO
Art Unit	2897
Examiner Name	WILSON, ALLAN R
Attorney Docket Number	P3962US00

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2012-06-13
Name/Print	Hae-Chan Park	Registration Number	50114

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Issue Classification

Application/Control No.	Applicant(s)/Patent Under Reexamination
12745878	SEO, EUN JUNG
Examiner	**Art Unit**
ALLAN R WILSON	2897

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
257	99	H 0 1 L 31 / 048 (2006.01.01)	

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
257	100	E33.059	E33.061	E33.066	
438	26				

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	16	17												
2	2		18												
3	3														
4	4														
5	5														
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6	7														
7	8														
8	9														
9	10														
10	11														
11	12														
12	13														
13	14														
14	15														
15	16														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	16	
/ALLAN R WILSON/ Primary Examiner.Art Unit 2897	7/12/12	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	12745878
Filing Date	2010-06-02
First Named Inventor	Eun Jung Seo
Art Unit	2897
Examiner Name	Wilson, Allan R.
Attorney Docket Number	P3962US00

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/A.W./	1	20040047151		2004-03-11	Bogner, et al.	Corresponds to TW501276

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
/A.W./	1	I246780	TW		2006-01-01	Toyoda Gosei Co., Ltd.; Sumita Optical Glass Inc.	English Abstract can be found on page 4	☐
/A.W./	2	501276	TW		2002-09-01	Osram Opto Semiconductors GmbH	Corresponds to US20040047151	☐
/A.W./	3	200636049	TW		2006-10-16	Koninklijke Philips Electronics N.V		☐

Receipt date: 07/16/2012	Application Number	12745878
INFORMATION DISCLOSURE STATEMENT BY APPLICANT **(Not for submission under 37 CFR 1.99)**	Filing Date	2010-06-02
	First Named Inventor	Eun Jung Seo
	Art Unit	2897
	Examiner Name	Wilson, Allan R.
	Attorney Docket Number	P3962US00

/A.W./	4	200522396	TW		2005-07-01	Lumileds Lighting U.S. LLCUS		☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
/A.W./	1	Taiwanese Office Action dated June 1, 2012, corresponding to U.S. Application No. 12/745,878	☒

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature	/Allan Wilson/	Date Considered	07/26/2012

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]See Kind Codes of USPTO Patent Documents at www.USPTO.GOVor MPEP 901.04. [2]Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5]Applicant is to place a check mark here if English language translation is attached.

Receipt date: 07/16/2012	Application Number	12745878
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Filing Date	2010-06-02
	First Named Inventor	Eun Jung Seo
	Art Unit	2897
	Examiner Name	Wilson, Allan R.
	Attorney Docket Number	P3962US00

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/hae-chan park/	Date (YYYY-MM-DD)	2012-07-16
Name/Print	/Hae-Chan Park/	Registration Number	50114

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S72	16	(("EUN JUNG") near2 (SEO)).INV.	US-PGPUB; USPAT; USOCR	ADJ	ON	2012/06/27 08:06
S73	2	US-20060220048-$.DID. OR US-20030107316-$.DID.	US-PGPUB; USPAT; USOCR	ADJ	ON	2012/06/27 08:08
S75	55	S74 and (LED or (light emitting diode)) same (groove or recess or cut$1out)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/06/27 08:16
S74	6233	((257/676) or (438/123)).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/06/27 08:16
S78	450	S77 and (LED or (light emitting diode)) with (groove or recess or cut$1out)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/06/27 08:50
S77	2704	S76 and lead frame	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/06/27 08:50
S76	15589	((257/98-100,E33.059,E33.061,E33.066) or (438/26)).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/06/27 08:50
S79	150	S77 and (LED or (light emitting diode)) near2 (groove or recess or cut$1out)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/06/27 08:51
L8	104	L7 not (@ad>"20081118" or @rlad>"20081118" or @pt1d>"20081118")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/06/28 06:30
L7	150	L6 and (LED or (light emitting diode)) near2 (groove or recess or cut$1out)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/06/28 06:30
L6	2708	L5 and lead frame	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/06/28 06:30
L5	15626	((257/98-100,E33.059,E33.061,E33.066) or (438/26)).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/06/28 06:30
L16	243	L15 not (@ad>"20081118" or @rlad>"20081118" or @pt1d>"20081118")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/06/28 06:34
L15	350	L11 and phosphor not (L13 or L14)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	ADJ	ON	2012/06/28 06:34

			IBM_TDB			
L14	78	L12 and phosphor$2 not L13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/06/28 06:34
L13	109	L12 and (LED or (light emitting diode)) same (thickness or height)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/06/28 06:34
L12	298	L9 and second adj2 lead frame	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/06/28 06:34
L11	714	L10 and (LED or (light emitting diode)) with (thickness or height)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/06/28 06:34
L10	2708	L9 and lead frame	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/06/28 06:34
L9	15626	((257/98-100,E33.059,E33.061,E33.066) or (438/26)).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/06/28 06:34
L17	15965	lead$1frame$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/06/28 06:40
L21	184	20 not (@ad>"20081118" or @rlad>"20081118" or @pt1d>"20081118")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/06/28 06:41
L20	243	17 and (LED or (light emitting diode)) same (groove or recess or cut$1out) not L19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/06/28 06:41
L19	55	L18 and (LED or (light emitting diode)) same (groove or recess or cut$1out)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2012/06/28 06:41
L18	6239	((257/676) or (438/123)).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/06/28 06:41

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L22	6	((257/98-100,E33.059,E33.061,E33.066) or (438/26)).CCLS.	UPAD	OR	OFF	2012/06/28 07:46

6/28/2012 8:02:02 AM
C:\Users\awilson\Documents\EAST\Workspaces\12\12745878.wsp

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/745,878	06/02/2010	Eun Jung Seo	P3962US00	4953

TITLE OF INVENTION:

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1770	$300	$2070	11/01/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 H.C. PARK & ASSOCIATES, PLC
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE	(B) RESIDENCE: (CITY and STATE OR COUNTRY)
Seoul Semiconductor Co., Ltd.	Seoul, Republic of Korea

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

☑ Issue Fee
☑ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _

4b. Payment of Fee(s):

☐ A check in the amount of the fee(s) is enclosed.
☑ Payment by credit card. Form PTO-2038 is attached.
☑ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 503698 .

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /hae-chan park/ Date October 22, 2012

Typed or printed name Hae-Chan Park Registration No. 50,114

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
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Electronic Patent Application Fee Transmittal

Application Number:	12745878
Filing Date:	02-Jun-2010
Title of Invention:	SLIM LED PACKAGE
First Named Inventor/Applicant Name:	Eun Jung Seo
Filer:	Hae-Chan Park/Sharon Price
Attorney Docket Number:	P3962US00

Filed as Large Entity

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1770	1770
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**2070**

Electronic Acknowledgement Receipt

EFS ID:	14038863
Application Number:	12745878
International Application Number:	
Confirmation Number:	4953
Title of Invention:	SLIM LED PACKAGE
First Named Inventor/Applicant Name:	Eun Jung Seo
Customer Number:	58027
Filer:	Hae-Chan Park/JungAh Kim
Filer Authorized By:	Hae-Chan Park
Attorney Docket Number:	P3962US00
Receipt Date:	22-OCT-2012
Filing Date:	02-JUN-2010
Time Stamp:	17:23:51
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$2070
RAM confirmation Number	4876
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Issue Fee Payment (PTO-85B)	P3962US00_Issue_Fee_Transmittal.pdf	239021 c41a52f7896724204401df27843cb14920faf048	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	31758 e1b012cc6a1fc572cba0d98d9eb9b44dd7f9e342	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	270779	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/745,878	11/27/2012	8319248	P3962US00	4953

58027 7590 11/07/2012

H.C. PARK & ASSOCIATES, PLC
1894 PRESTON WHITE DRIVE
RESTON, VA 20191

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 205 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Eun Jung Seo, Ansan-si, KOREA, REPUBLIC OF;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT7890225

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
SEOUL SEMICONDUCTOR CO., LTD.	12/23/2022

RECEIVING PARTY DATA

Name:	SMART HANDOVER LLC
Street Address:	8140 WALNUT HILL LANE
Internal Address:	SUITE 610
City:	DALLAS
State/Country:	TEXAS
Postal Code:	75231

PROPERTY NUMBERS Total: 5

Property Type	Number
Patent Number:	8319246
Patent Number:	8319248
Patent Number:	9350942
Patent Number:	8963196
Patent Number:	9899573

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Email: jason@ipval.com
Correspondent Name: JASON BOURGEOIS
Address Line 1: 4940 BROADWAY STREET
Address Line 2: SUITE 130
Address Line 4: SAN ANTONIO, TEXAS 78209

NAME OF SUBMITTER:	JASON BOURGEOIS
SIGNATURE:	/Jason Bourgeois/
DATE SIGNED:	04/07/2023
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 3

source=Assignment SSC to Smart Handover#page1.tif
source=Assignment SSC to Smart Handover#page2.tif
source=Assignment SSC to Smart Handover#page3.tif

PATENT ASSIGNMENT AGREEMENT

THIS PATENT ASSIGNMENT AGREEMENT (the "Agreement"), is made and entered into this 23 day of December, 2022 (the "Effective Date"), by and between Seoul Semiconductor Co., Ltd. ("Assignor") and Smart Handover, LLC ("Assignee") (each a "Party" and collectively the "Parties")

WHEREAS, Assignor is the owner of all rights, title and interest in and to the patents appearing below, and including without limitation, all extensions, continuations, and provisionals thereof (the "Patents").

U.S. Patent No. 8,319,246
U.S. Patent No. 8,319,248
U.S. Patent No. 9,530,942
U.S. Patent No. 8,963,196
U.S. Patent No. 9,899,573

WHEREAS, Assignor and Assignee have agreed on a Patent Purchase Agreement (the "Purchase Agreement") dated December 23, 2022, by and between Assignor and Assignee, the terms of which are incorporated herein by reference, that Assignor shall sell, transfer, assign and set over unto Assignee and Assignee shall accept all rights, title and interest in and to the Patents as specified in this Agreement;

NOW, THEREFORE, in consideration of the mutual covenants and agreements of the Parties and pursuant to the Purchase Agreement, and for other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, it is hereby agreed as follows:

1. Assignor hereby sells, transfers, assigns and sets over to Assignee all rights, title and interest (for all countries) in and to the Patents, and all the rights and privileges under any letters patent that may be granted under any extensions, continuations, and provisionals thereof; and all applications for industrial property protection, including without limitation, all applications for patents, utility models, copyright, and designs which may hereafter be filed for said Invention and Patents in any country or countries, together with the right to file such applications and the right to claim for the same the priority rights derived from the Patents under the patent laws of the United States, the International Convention for the Protection of Industrial Property, or any other international agreement or the domestic laws of the country in which any such application is filed, as may be applicable; and all applications for industrial property protection, including, without limitation, all applications for patents, utility models, copyrights and designs which may hereafter be filed for said Invention or Patent in any country or countries, together with the right

to file such applications; and all forms of industrial property protection, including, without limitation, patents, utility models, inventors' certificates, copyrights and designs which may be granted for said Patents in any country or countries and all extensions, renewals and reissues thereof; including all moral rights and all rights relating to the past, present and future including the benefit of any attorney client privilege or attorney work product privilege, all income, royalties, damages, rights to enforce, rights to sue, and any and all payments now or hereafter due or payable with respect thereto, and the right to bring any claim, sue, counterclaim, and recover for the past, present and future infringement, the right to sue for and recover all profits and damages by reason of past infringement by any party or parties for Assignee's and Assignee's successors' and assigns' own use and benefit. All rights to royalty income, including past, present, and future royalties, are also hereby conveyed by this instrument.

2. Assignor appoints Assignee, and Assignee's successors and assigns, as its attorney-in-fact to act in Assignor's name and to execute, deliver, and record any document or instrument of assignment or conveyance necessary to perfect, grant, and confirm the rights granted herein. Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks of the United States and any official of any country or countries foreign to the United States, whose duty is to issue patents or other evidence or forms of industrial property on applications as aforesaid, to issue the same to Assignee, its successors, assigns and legal representatives, or to such nominees as it may designate.

3. Assignor agrees that, whenever reasonably requested by Assignee and at Assignee's expense, Assignor will execute all papers, take all rightful oaths, and do all acts which may be reasonably necessary for securing and maintaining patents for the Invention in any country and for vesting title thereto in Assignee, its successors, assigns and legal representatives or nominees.

4. Assignor authorizes and empowers Assignee, its successors, assigns and legal representatives or nominees, to invoke and claim for any application for patent or other form of protection for the Invention, the benefit of the right of priority provided by the International Convention for the Protection of Industrial Property, as amended, or by any convention which may henceforth be substituted for it, or any other international agreement or the domestic laws of the country in which any such application is filed, as may be applicable, and to invoke and claim such right of priority without further written or oral authorization from Assignor.

5. Assignor hereby consents that a copy of this Agreement shall be deemed a full legal and formal equivalent of any assignment, consent to file or like document that may be required in any country for any purpose and more particularly in proof of the right of Assignee or nominee to claim the aforesaid benefit of the right of priority provided by the International Convention for the Protection of Industrial Property, as amended, or by any convention which may henceforth be substituted for it.

6. All of the rights, title and interest in and to the Patents sold, transferred, assigned and set over to Assignee hereunder include all income, royalties, damages, and payments now or hereafter due or payable with respect thereto, and all causes of action (whether in law or equity) and the

right to sue, counterclaim, and recover for the past, present and future infringement of the rights assigned or to be assigned hereunder.

Seoul Semiconductor Co., Ltd.

By: _____

Name: Woohyung Yi

Title: Patent Team Director

Date: 12/23/2022

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT7890237

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
SMART HANDOVER LLC	12/25/2022

RECEIVING PARTY DATA

Name:	SEMILED INNOVATIONS LLC
Street Address:	6841 VIRGINA PARKWAY
Internal Address:	STE 103-441
City:	MCKINNEY
State/Country:	TEXAS
Postal Code:	75071

PROPERTY NUMBERS Total: 6

Property Type	Number
Patent Number:	8309971
Patent Number:	8319246
Patent Number:	8319248
Patent Number:	9530942
Patent Number:	8963196
Patent Number:	9899573

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Email: jason@ipval.com
Correspondent Name: JASON BOURGEOIS
Address Line 1: 4940 BROADWAY STREET
Address Line 2: SUITE 130
Address Line 4: SAN ANTONIO, TEXAS 78209

NAME OF SUBMITTER:	JASON BOURGEOIS
SIGNATURE:	/Jason Bourgeois/
DATE SIGNED:	04/07/2023
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 2
source=Assignment Smart Handover to SemiLED 2#page1.tif
source=Assignment Smart Handover to SemiLED 2#page2.tif

ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, **Smart Handover, LLC**, a limited liability company duly organized and validly existing under the laws of the Texas, having an office at 8140 Walnut Hill Lane, Suite 500, Dallas, TX 75231; (***"Assignor"***), do hereby sell, assign, transfer, and convey unto **SemiLED LLC**, a limited liability company duly organized and validly existing under the laws of the Texas, having an office at 6841 Virginia Parkway, Suite 103-441, McKinney, TX 75071 (***"Assignee"***), or its designees, all right, title, and interest that exist today and may exist in the future in and to all of the following (collectively, the ***"Assigned Patent Rights"***):

(a) the invention disclosures, provisional patent applications, patent applications and patents, which are listed in the next page (the "***Patents***");

(b) causes of action (whether currently pending, filed, or otherwise) and other enforcement rights under, or on account of, any of the Patents, including, without limitation, all causes of action and other enforcement rights for (i) damages, (ii)injunctive relief, and (iii) other remedies of any kind for past, current, and future infringement; and

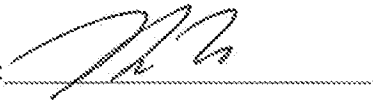
(c) all rights to collect royalties and other payments under or on account of any of the Patents and/or any item in the foregoing categories (b).

The terms and conditions of this Assignment of Assigned Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignors, its successors, assigns, and other legal representatives.

IN WITNESS WHEREOF the parties hereto have caused this Agreement to be executed by their duly authorized officers or representatives.

Date: Decenbe- 25, 2022

Assignor
Smart Handover, LLC

By: 

Name: Hao Ni
Title: Manager

Patents

Document No.	Title
US8309971B2	Light emitting diode having electrode pads.
US8319246B2	Semiconductor device and method for manufacturing same
US8319248B2	Slim LED package
US9530942B2	Slim LED package
US8963196B2	Slim LED package
US9899573B2	Slim LED package