

UNITED STATES PATENT AND TRADEMARK OFFICE

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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SAMSUNG ELECTRONICS CO., LTD. AND  
SAMSUNG ELECTRONICS AMERICA, INC.  
Petitioner

v.

SINOTECHNIX LLC  
Patent Owner

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Case IPR2025-00334  
U.S. Patent No. 9,412,913  
Claims 1-4, and 6

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**DECLARATION OF IOANNIS KYMISSIS, PH.D.**  
**ON BEHALF OF PETITIONER**

Name: Dr. Ioannis Kymissis



Signature:

Date: March 9, 2025

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Declaration of Dr. Ioannis Kymissis  
U.S. Patent No. 9,412,913  
Claims 1-4 and 6

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I, Ioannis Kymissis, declare as follows:

1. My name is Ioannis Kymissis.
2. I have been retained as an expert witness on behalf of Petitioner Samsung Electronics Co., LTD., and Samsung Electronics America, Inc. to provide expert opinions on the validity of U.S. Patent No. 9,412,913 (“913 Patent”).

**I. Introduction**

3. I am currently the Kenneth Brayer Professor in Electrical Engineering and Vice Dean of Infrastructure and Innovation at Columbia’s school of Engineering and Applied Science in New York, NY. I have been a faculty member in the Department of Electrical Engineering since 2006.

4. I received a bachelor’s (S.B.) in Electrical Engineering and Computer Science in 1998, a master’s (M.Eng.) in Electrical Engineering and Computer Science in 1999, and a doctoral degree (Ph.D.) in Electrical Engineering and Computer Science in 2003, all from Massachusetts Institute of Technology (MIT) in Cambridge, MA. I was a co-op at IBM research while I was a student, and worked at IBM’s laboratories in Yorktown Heights, New York, and Tokyo, Japan while also pursuing my undergraduate and M.Eng. degrees. Part of this work was on backplanes and new technologies for liquid crystal displays, in collaboration with IBM’s Display Business Unit. My Ph.D. thesis was in the field of field emission

displays. I also completed a post-doc at MIT, where I worked on OLED technologies, semiconductors, and quantum dot-based materials.

5. After my post-doc, I worked as a Technical Consultant and Senior Engineer at QDVision from 2005-2006. QDVision was, at that time, developing quantum dot sensitized OLED displays (QDLEDs) and quantum dot based downconversion elements for LCD display backlights (which is now known as QLED). As part of that work on QLED at QDVision, I developed some LED coating and co-packaging technologies at in collaboration with Luminus Devices. This included the dispersion of quantum dots in encapsulation materials used in LED packages and the integration of LED heatsinks. The QLED technology used in televisions today is partially based on this work, and uses quantum dots together with blue LEDs in the backlight.

6. I joined the faculty at Columbia University in 2006, where I have been teaching and conducting research for around 18 years. In general, I teach courses in solid state electronics, including undergraduate and graduate level courses in physics, thin film electronics, and displays. I have taught a course on displays for nearly 20 years, in which we cover a broad range of topics, including organic light emitting diode (“OLED”) displays, liquid crystal displays (“LCD”), visual

perception, color science, wave optics, emissive displays, and their mechanisms, display back panels, and 3D displays.

7. Over the course of my career, I have supervised many students, including around twenty Ph.D. candidates and fourteen post-doctoral associates. Several of these theses related to LED devices, and one current student is working on LCDs, including backplane design and backlight integration.

8. I have authored over 150 publications in peer-reviewed academic journals, transactions, and books. Many of these publications are in the field of OLED displays, LCD displays, color science, and display back panels. I have also presented at and/or contributed to over 150 conferences, where many of my presentations were on the topic of OLED displays, LCD displays, color science, and display back panels.

9. I am a named inventor in 51 issued U.S. patents across 39 families; many of these concern various designs and manufacturing methods for semiconductor-based devices, including LEDs, field effect transistor systems, methods for patterning thin films, and lithography techniques.

10. I am a member of and have held positions in many professional organizations, program committees, and editorial boards. I am currently President and have served as President Elect, Treasurer, Secretary, and Publication Chair for

the Society for Information Display (SID). I have also served as the Editor in Chief for the Journal of the Society for Information Display, and have served as an Associate Editor for the IEEE Open Journal of Immersive Displays, among other editorial boards.

11. I have received several awards for my technical experience. I am a fellow of Optica, SID, SPIE, the National Academy of Inventors, and the Institute of Electrical and Electronics Engineers.

12. A copy of my curriculum vitae (“CV”) is attached as Appendix A. My CV includes my employment history, education, awards, advisory positions, publications, conference presentations, and patents.

13. In general, I am familiar with matters involving patents, including analyzing claims from the perspective of a person of ordinary skill in the art at the time the purported invention was made.

14. I am familiar with the technology described in the ’913 Patent.

15. I am familiar with the knowledge and capabilities of a person of ordinary skill in the art as of December 3, 2007.

16. Below, I provide the list of exhibits that I considered during my preparation of this Declaration. I have reviewed all of the exhibits and all documents

mentioned in my Declaration. Further, my opinions are based on my technical education, experience, and training in the field.

| <b>Petitioner Exhibit No.</b> | <b>DESCRIPTION</b>                                                                |
|-------------------------------|-----------------------------------------------------------------------------------|
| 1001                          | U.S. Patent No. 9,412,913 (“’913 Patent”)                                         |
| 1003                          | U.S. Patent Publication No. 2004/0000727 (“Hsu”)                                  |
| 1004                          | Certified Translation of Japanese Patent Publication No. 2006-005281 (“Iwamasa”)  |
| 1005                          | U.S. Patent Publication No. 2007/0252250 (“Hui”)                                  |
| 1006                          | U.S. Patent Publication No. 2005/0280017 (“Oshio”)                                |
| 1007                          | Certified Translation of Japanese Patent Publication No. 2007-134376 (“Takasaki”) |
| 1008                          | File History of U.S. Patent No. 9,412,913                                         |
| 1009                          | U.S. Patent Publication No. 2005/0151149 (“Chia”)                                 |
| 1010                          | File History of U.S. Patent No. 8,963,196                                         |
| 1011                          | File History of U.S. Patent No. 8,659,050                                         |
| 1012                          | File History of U.S. Patent No. 8,319,248                                         |

17. To my knowledge and understanding, the ’913 Patent claims priority to U.S. Patent Application No. 14/161,377, filed January 22, 2014, which is a continuation of U.S. Patent Application No. 13/631,060, filed September 28, 2012, which is a continuation of U.S. Patent Application No. 12/745,878, filed June 2, 2010, which is a national entry application of PCT Application No. PCT/KR2008/006777, filed November 18, 2008. PCT Application No. PCT/KR2008/006777 originated from Korean Patent Application No. 10-2007-0124469, which was filed December 3, 2007. EX1001, Cover; EX1008, at 43-44. EX1010–EX1012.

18. I have been retained as an expert for Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. in the field of LED devices and LED packaging.

19. My compensation for this case is at my usual and customary rate for the time I spent on this IPR. My compensation is not and will not be affected by the outcome of this case.

20. I have no financial interest in the outcome of the case. I also do not have any financial interest in either Samsung Electronics Co., Ltd. or Samsung Electronics America, Inc.

21. I do not have personal contact with nor knowledge of the named inventors of the '913 Patent.

## **II. Relevant Law**

22. I am not an attorney. Petitioner's counsel has informed me about the following aspects of patent law, which I applied in my analysis and conclusions.

### **A. Person of Ordinary Skill in the Art**

23. I have been informed that a patent and prior art should be reviewed from the perspective of a person of ordinary skill in the art ("POSITA"). I understand that a POSITA is an individual who is hypothetical, is of ordinary creativity, and would have been familiar with the prior art as of the patent's claimed priority date.

24. I have been informed that there are various factors that are applicable in determining the level of a person of ordinary skill in the art. These include:

- (1) the educational level of the inventor;
- (2) type of problems encountered in the art;
- (3) prior art solutions to those problems;
- (4) rapidity with which innovations are made;
- (5) sophistication of the technology; and
- (6) educational level of active workers in the field.

25. I have been informed that not all such factors may be present in every case, and one or more of these or other factors may predominate.

**B. Claim Construction**

26. I have been informed that claim construction is a matter of law that will ultimately be determined by the Board. To determine the meaning of claim terms for the purposes of the *inter partes* review, I have been informed that one should generally use the ordinary and customary meaning as understood by a POSITA at the time of the claimed priority date, in view of the claim language, patent specification, and the file history. I have been informed that the proper interpretation of the claim term should be arrived at in light of the patent's claims, specification, and file history.

27. Further, I understand that although a claim term should be read in light of the specification, limitations should not be imported into the claim from the specification. I understand that interpreting a claim term to exclude a preferred embodiment is often inaccurate. I have also been informed that the prosecution history can facilitate the meaning of a claim term or a claim by demonstrating how the inventor understood the invention and by showing whether the inventor limited the claim term or claim during the course of prosecution or caused the claim scope to be narrower than it otherwise would be.

**C. Anticipation**

28. I understand that a patent claim is invalid for being anticipated if each limitation of that claim is present either explicitly, implicitly, or inherently in a single prior art reference. I also understand that, to be an inherent disclosure, the prior art reference must necessarily disclose the limitation, and the fact that the reference might possibly practice or contain a claimed limitation is insufficient to establish that the reference inherently teaches the limitation.

**D. Obviousness**

29. I have been informed that a claim is invalid if the claim would have been obvious from the perspective of a person of ordinary skill in the art at the time the alleged invention was made.

30. I understand that an obviousness evaluation involves consideration of several factors, including:

- a. the level of ordinary skill in the art at the time the application was filed;
- b. the scope and content of the prior art; and
- c. what differences, if any, existed between the claimed invention and the prior art.

31. In determining whether a combination based on multiple references would have been obvious, it is appropriate to consider, among other factors:

- a. whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;
- b. whether a person of ordinary skill in the art could implement a predictable variation, and would see the benefit of doing so;
- c. whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by those skilled in the art;
- d. whether a person of ordinary skill would have recognized a reason to combine known elements in the manner described in the claim;

- e. whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- f. whether the claim applies a known technique that had been used to improve a similar device or method in a similar way.

32. I understand that a claim is obvious if it combines old elements without any change to their respective functions. I also understand that a claim is obvious if the claim simply substitutes one element for another element known in the field, and the resulting combination yields predictable results. Further, while it may be helpful for there to be a reason for the combination, I understand that it is not strictly required to find an express teaching, suggestion, or motivation to combine within the references. Market forces, such as design incentives, can prompt variations of a product, either in the same field or a different field. Further, for techniques, if a technique has been used to improve one device and if a POSITA would recognize that applying the same technique would have improved a different device in a comparable way, then it would have been obvious if common sense directs one to combine multiple prior art references or add missing factors.

33. I have been informed and understand that hindsight bias must be avoided when determining obviousness. Accordingly, the patent's claims and

descriptions cannot be used as a roadmap when analyzing combinations of prior art references.

### III. Summary of Opinions

34. I conclude that claims 1–4 and 6 of the '913 Patent are anticipated and/or rendered obvious by the following prior art references: Hsu, Iwamasa, Hui, Oshio, and/or Takasaki as summarized below.

| Ground | 35 U.S.C. | Claims | Prior Art Reference(s) |
|--------|-----------|--------|------------------------|
| I      | §103      | 1–4, 6 | Hsu, Iwamasa           |
| II     | §103      | 1–4, 6 | Hsu, Iwamasa, Hui      |
| III    | §102      | 1–4, 6 | Oshio                  |
| IV     | §103      | 1–4, 6 | Oshio, Hui             |
| V      | §102      | 1–4    | Takasaki               |

### IV. Technology Background

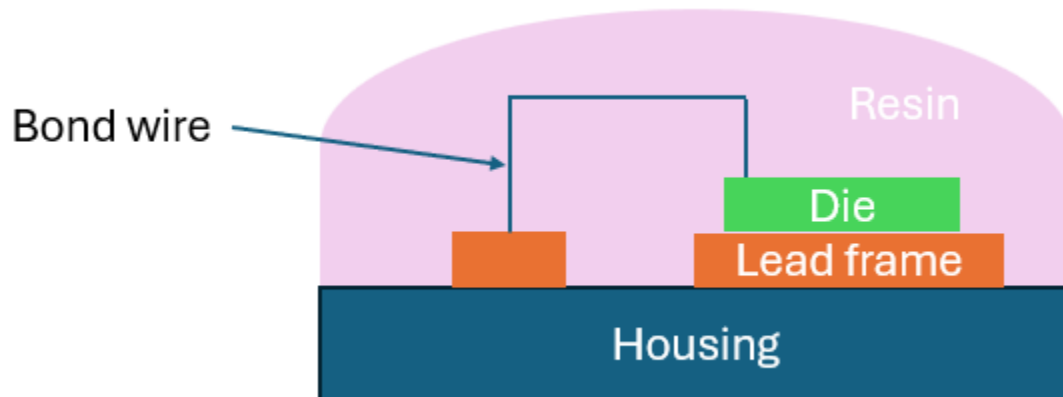
#### A. Light Emitting Diode Packages (“LED Packages”)

35. A light-emitting diode (“LED”) is a semiconductor device that emits light when an electric current passes through it. EX1001, 1:29–30.<sup>1</sup> To protect and support the LED chip, it is enclosed within a structure known as an LED package. EX1001, 1:31–32. In a lead frame-type LED package, metal lead frames serve as electrical conductors, delivering current to the LED chip. EX1001, 1:32–36. The package includes a housing with a cavity that holds the lead frame and LED chip.

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<sup>1</sup> In the rest of the Declaration, when I quote a portion of a prior art reference, I will also reproduce, where appropriate, the full paragraph of the prior art reference in which the quote appears.

This cavity is filled with an encapsulation material, which protects the LED chip, enhances light extraction, and provides mechanical stability. EX1001, 1:36–39. I have schematically illustrated below some of these fundamental structures that can be found in an LED package.



An LED emits light through recombination of electrons and holes by application of an electric current. An LED package means a package structure in which a light emitting diode chip, that is, an LED chip, is received. Many kinds of LED packages, particularly, a lead frame type LED package and a printed circuit board (PCB) type LED package, are well known in the art. ***The lead frame type LED package has a structure wherein a cavity of a housing for supporting a lead frame is filled with an encapsulation material, with the LED chip positioned in the cavity of the housing.***

EX1001, 1:29-38.

36. There are several practical considerations that must be addressed when designing LED packages, particularly those utilizing a lead frame structure. One of the challenges is degradation of the encapsulation resin over time, a phenomenon

often referred to as “yellowing.” This occurs due to prolonged exposure to the high-energy light emitted by the LED chip, which can lead to a reduction in light output and altered color characteristics.

Further, the encapsulation material of the LED package, which covers the LED chip, ***undergoes a yellowing phenomenon*** by energy generated from the LED chip emitting light. Such a ***yellowing phenomenon is a main cause of decreased luminescence performance and lifetime of the LED package.***

EX1001, 1:56-60.

37. Additionally, excessive generation of heat during LED operation can cause the encapsulation resin to expand and contract, potentially leading to delamination or detachment from the package, which can ultimately result in device failure. These thermal issues can be more noticeable in LED packages with miniaturized dimensions, where limited space constrains heat dissipation. In particular, lead frame-type LED packages may face fabrication challenges due to the thickness of the housing that supports the lead frame. EX1001, 1:43-45.

For the lead frame type LED package, the housing supporting the lead frame has an excessive thickness, which make it difficult to fabricate a thin lead frame type LED package.

EX1001, 1:43-45.



- a transparent **encapsulation material**.

40. As can be seen in Figure 2, “**first [lead frame]** and **second lead frame[]** separated from each other; . . . an **LED chip** mounted on a bottom surface of [a] chip mounting recess and connected with the **second lead frame** via a **bonding wire**; and a transparent **encapsulation material**.” EX1001, 2:13–24.

In accordance with an aspect of the present invention, a slim LED package includes: *first and second lead frames separated from each other*; a chip mounting recess formed on one upper surface region of the first lead frame by reducing a thickness of the one upper surface region below other upper surface regions of the first lead frame; an *LED chip mounted on a bottom surface of the chip mounting recess and connected with the second lead frame via a bonding wire*; and a *transparent encapsulation material* protecting the LED chip while supporting the first and second lead frames. The LED chip may have a thickness lower than or equal to a depth of the chip mounting recess.

EX1001, 2:13–24.

41. As further shown in Figure 2 in teal, the “slim LED package may further include **openings** or **grooves** formed on an upper or lower surface of the **first** or **second lead frame** to increase a bonding force between the **first** or **second frames** and the **encapsulation material**.” EX1001, 2:38–41. These **grooves**, such as **grooves 122, 142**, are on the lower surface of the **first** and **second lead frames** in Figure 2. As such, they prevent separation of an interfacial surface between the first lead frame, the second lead frame and the encapsulation material. EX1001, 3:16–21.

The slim LED package may further include *openings or grooves formed on an upper or lower surface of the first or second lead frame* to increase a bonding force between the first and second lead frames and the encapsulation material.

EX1001, 2:38–41.

Further, according to one embodiment of the present invention, openings or grooves are formed on the lead frames to increase a bonding force between the lead frames and an encapsulation material, *thereby preventing separation of an interfacial surface between the encapsulation material 20 and the lead frames.*

EX1001, 3:16–21.

## **B. Prosecution History**

42. I have reviewed the file history of the '913 Patent and its parent patents. EX1008 [FH of the '913 Patent]. EX1010-1012. Below, I summarize the relevant information from the file history of the '913 Patent and any additional relevant information from the file history of related applications that is pertinent to my opinion.

43. The '913 Patent was filed as No. 14/624,172 (“’172 Application”) on February 17, 2015. The '913 Patent is a continuation of a U.S. Patent Application No. 14/161,377 (“’377 Application”), filed January 22, 2014. The '377 Application is a continuation of a U.S. Patent Application No. 13/631,060 (“’060 Application”). The '060 Application is a continuation of a U.S. Patent Application No. 12/745,878 (“’878 Application”). The '878 Application is a national entry application of PCT

Application No. PCT/KR2008/006777, which was filed on November 18, 2008, which claims priority to Korean Patent Application No. 10-2007-0124469, which was filed December 3, 2007. EX1008 [FH of the '913 Patent]. EX1010-1012.

44. Originally, the '172 Application included claims 1–14, with claims 1 and 10 being independent claims. EX1008, 33–35. Both independent claims 1 and 10 were directed to a light emitting package. EX1008, 33, 34.

45. On July 9, 2015, the Examiner issued an Office Action. EX1008, 77. All claims 1-14 were objected to because the Examiner found that the limitations “bond force-increasing components” and “vertex” created confusion. EX1008, 79. Furthermore, the Examiner rejected all claims 1-14 as anticipated by U.S. Patent Publication No. 2005/051149 (“Chia”). EX1008, 79–83.

46. In response to that Office Action: (1) claim 1 was amended as follows:

~~“bond force-increasing~~ resin-holding components disposed ~~on at least a portion of at least one side of the lead frame~~ along at least two sides of the at least one of the first and second lead frames and are separated from each other at an area where the sides meet;”

(2) claim 4 was canceled; (3) claim 10 was amended as follows:

at least one of the first and second lead frames comprises ~~one or more bond force-increasing components~~ a circular hole disposed ~~along at least two sides~~ a side of at least one of the first lead frame and the second lead frame, and the ~~bond force-increasing components are~~ hole is disposed to be symmetric with respect to the first direction;

(4) Applicant argued that Chia does not disclose the features of amended claim 1 and 10. EX1008, 110–116.

47. On November 5, 2015, the Examiner issued a subsequent Office Action. EX1008, 120–128. In this Office Action, the Examiner again rejected claims 1, 3, 5–9, and 12 as anticipated by Chia. EX1008, 122-124. Additionally, the Examiner rejected claims 10, 11, 13, and 14 as obvious over Chia in view of U.S. Patent Publication No. 2005/0280017 (“Oshio”). EX1008, 124-125.

48. In response to that Office Action: (1) claim 1 was amended as follows:

wherein at least one of the first and second lead frames comprises ~~one or more~~ resin-holding components disposed along ~~at least two adjacent~~ sides of ~~the at least one of the first and second lead frames, and are the resin-holding components being~~ separated from each other at ~~an area where the sides meet corners of the adjacent sides;~~

(2) claims 10, 11, 13, and 14 were cancelled; and (3) Applicant argued that “the at least two sides” clearly belong entirely to one of either of the first and second lead frames, but not both, and therefore claim 1 is not anticipated by Chia. EX1008, 134–140.

49. On January 15, 2016, the Examiner issued an Advisory Action, in which the Examiner stated that the Applicants arguments “appear persuasive,” but stated that the amendments had not been entered because the amendments raised new issues that needed to be researched. EX1008, 146–149.

50. On February 22, 2016, the Examiner issued another Office Action. EX1008, 165-171. In this Office Action, the Examiner rejected claims 1 and 8 as anticipated by Chia, and claims 1, 3, and 7, and as being anticipated by U.S. Patent Publication No. 2015/0091040 (“Kobayakawa”). EX1008, 167-169. The Examiner also stated that “[c]laims 5, 6, and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.” EX1008, 169-170.

51. In response to that Office Action: (1) claim 1 was amended to recite “the resin-holding components are disposed on two adjacent sides of each of the first lead frame and the second lead frame;” and (2) claim 7 was amended to be an independent claim. EX1008, 182–188.

52. The Examiner issued a Notice of Allowance on May 4, 2016. EX1008, 208-215. In the “Reason for Allowance” section the Examiner stated that the prior art does not show “one of the lead frames [with] resin holding components disposed along adjacent sides which are separated for each other at corners of the sides, and the resin-holding components [being] disposed on two adjacent sides of both of the first and second lead frames.” EX1008, 213. The Examiner made similar arguments in regard to claim 7. EX1008, 213-214.

53. The '913 Patent issued on August 9, 2016. EX1001, Cover; EX1008, 243.

## **VI. Level Of Ordinary Skill In The Art**

54. I have reviewed the factors relevant for determining the level of a POSITA outlined in Section II.A in the context of the '913 Patent. The '913 Patent relates to LED devices. EX1001, Title, Abstract. The field of LED devices was well-researched by the earliest claimed priority date of the '913 Patent: December 3, 2007. As demonstrated by prior art of record in the prosecution history of the '913 Patent, the relevant field relates to LED devices and their packages. *See, e.g.,* EX1009 [Chia]. Accordingly, a person of ordinary skill in the relevant field or art ("POSITA") as of December 3, 2007 would have had a Bachelor's degree in Electrical Engineering, Material Science, Physics, or an equivalent field, and approximately two years of experience in the field of LEDs. Lack of professional experience can be substituted by additional education, and vice versa.

55. At the time of the claimed priority date of the '913 Patent (December 3, 2007), I met and/or exceeded the above requirements for a POSITA.

## **VII. Claim Construction**

56. I have reviewed the specification, the claims, and the file history of the '913 Patent.

57. I have been asked to determine if any claim term should be construed so the Board can understand how the prior art references read on the challenged claims. I have not identified any terms that the Board needs to construe for the purposes of this IPR.

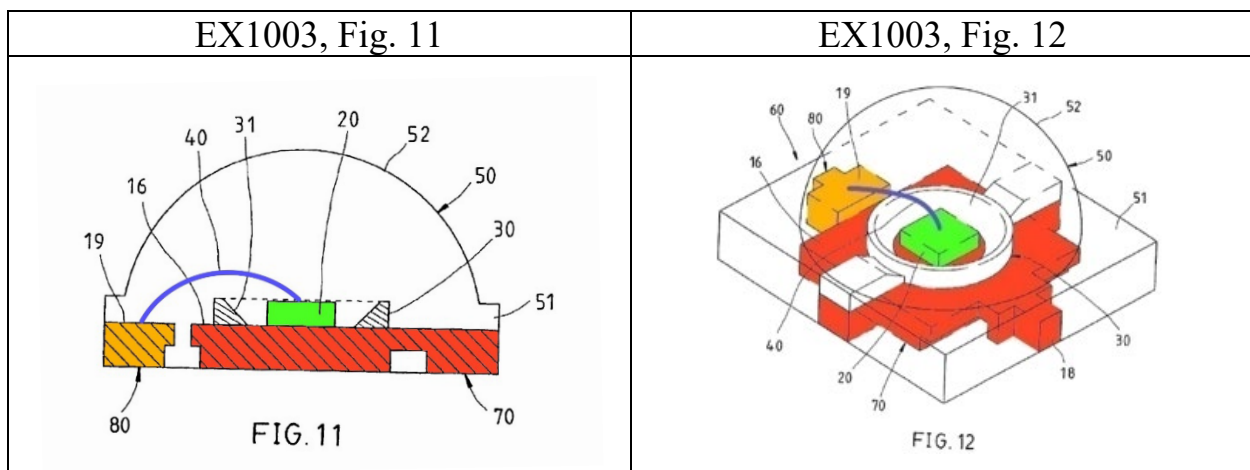
## VIII. Specific Grounds of Invalidity.

### A. Ground I: Hsu In Combination With Iwamasa Renders Obvious Claims 1-4, And 6.

#### 1. Overview of Hsu (EX1003)

58. I will begin with the description of prior art reference called Hsu. EX1003.

59. Already, Hsu disclosed a large part of the claimed subject matter before the '913 Patent. Similar to the '913 Patent, Hsu describes “LED package.” EX1003, Title. Examples of some of these packages (referred to as “LED package 60”) are shown below in Figures 11 and 12.



60. Hsu teaches that the LED 60 package includes a **first terminal 70**, a **second terminal 80**, the **LED die 20**, the reflecting ring 30, the **conductive wire 40**, and the encapsulant 50. *See* EX1003, [0025]. “The **first terminal 70** is formed by the main plate 16, the extending arm 18 located at a right side of the main plate 16, and the bridges 17 [not labeled in Figure 12] respectively located at upper and lower sides of the main plates 16.... The **second terminal 80**[] is the separate arm 19.”), EX1003, [0025]. The **first terminal** is made of an electrically conductive metal, and the **second terminal** is made of the same electrically conductive metal and is “spaced an appropriate distance apart from the first terminal”. EX1003, [0025]; *see also* EX1003, claim 6 (“a **second terminal** made of the electrically conductive metal and located at a side of said **first terminal** and spaced apart from said first terminal with a predetermined space.”).

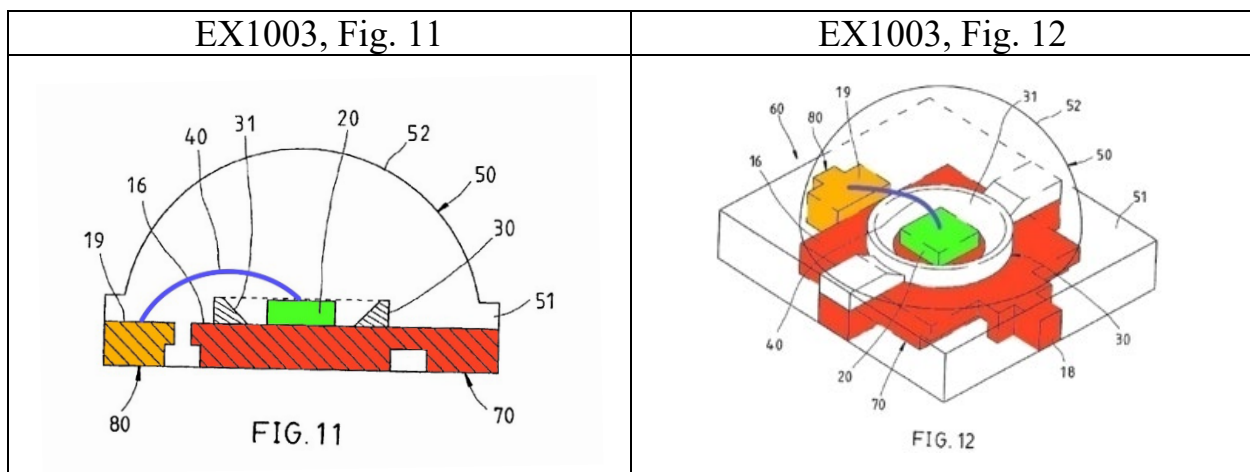
Referring to FIGS. 11-12, the **LED 60 package** made by the foregoing fabricative process structurally includes *a first terminal 70, a second terminal 80*, the LED die 20, the reflecting ring 30, the conductive wire 40, and the encapsulant 50. *The first terminal 70 is formed by the main plate 16, the extending arm 18 located at a right side of the main plate 16, and the bridges 17 respectively located at upper and lower sides of the main plates 16.* Additionally, *the first terminal 70 is made of an electrically conductive metal. The second terminal 80, which is the separate arm 19*, is located at a left side of the first terminal 70 and *spaced an appropriate distance apart from the first terminal 70 and made of the same electrically conductive metal.*

The LED die 20 has a bottom, which is smoothly bonded to a top surface of the main plate 16 of the first terminal 70 such that an electrode at the bottom of the LED die 20 is electrically connected to the first terminal 70. The reflecting ring 30, which is made of an opaque white plastic material, is molded on the top surface of the main plate 16 of the first terminal 70 by means of the injection molding technique and surrounds the die 20 and has the inner surface 31 facing upward as a slope. The conductive wire 40 is connected between the other electrode of the top surface of the die 20 and the top surface of the second terminal 80. The encapsulant 50, which material is the insulated epoxy resin with high transparency, encapsulates the die 20, the reflecting ring 30, and the conductive wire 40. Additionally, the base 51 of the encapsulant 50 covers the top surface of the first terminal 70 and the second terminal 80 and fills the space therebetween to remain two terminals 70 and 80 spaced apart in opposite relationship. The top of the encapsulant 50 is formed as the domed protrusion 52. When the LED package 60 is in use, generally take the first terminal 70 as positive electrode and the second terminal 80 as negative electrode such that the LED die 20 is charged by the electricity to emit white light. The emitted white light is then reflected from the inner surface 31 of the reflecting ring 30 to the dome-shaped protrusion of the encapsulant 50.

EX1003, [0025].

61. As I already noted in the paragraph above, Hsu also describes that the LED package includes an **LED die**. EX1003, [0025]. (“the LED 60 package . . . structurally includes a **first terminal 70**, a **second terminal 80**, the **LED die 20** the reflecting ring 30, the conductive wire 40, and the encapsulant 50.”). The **first**

**terminal** and the **LED die 20**, are configured to establish electrical connectivity. EX1003, [0025]. Specifically, “**LED die 20** has a bottom, which is smoothly bonded to a top surface of the main plate 16 of the **first terminal 70** such that an electrode at the bottom of the **LED die 20** is electrically connected to the **first terminal 70**.” EX1003, [0025].



Referring to FIGS. 11-12, the **LED 60 package** made by the foregoing fabricative process *structurally includes* a first terminal 70, a second terminal 80, *the LED die 20*, the reflecting ring 30, the conductive wire 40, and the encapsulant 50. The first terminal 70 is formed by the main plate 16, the extending arm 18 located at a right side of the main plate 16, and the bridges 17 respectively located at upper and lower sides of the main plates 16. Additionally, the first terminal 70 is made of an electrically conductive metal. The second terminal 80, which is the separate arm 19, is located at a left side of the first terminal 70 and spaced an appropriate distance apart from the first terminal 70 and made of the same electrically conductive metal. *The LED die 20 has a bottom, which is smoothly bonded to a top surface of the main plate 16 of the first terminal 70 such that an electrode at the*

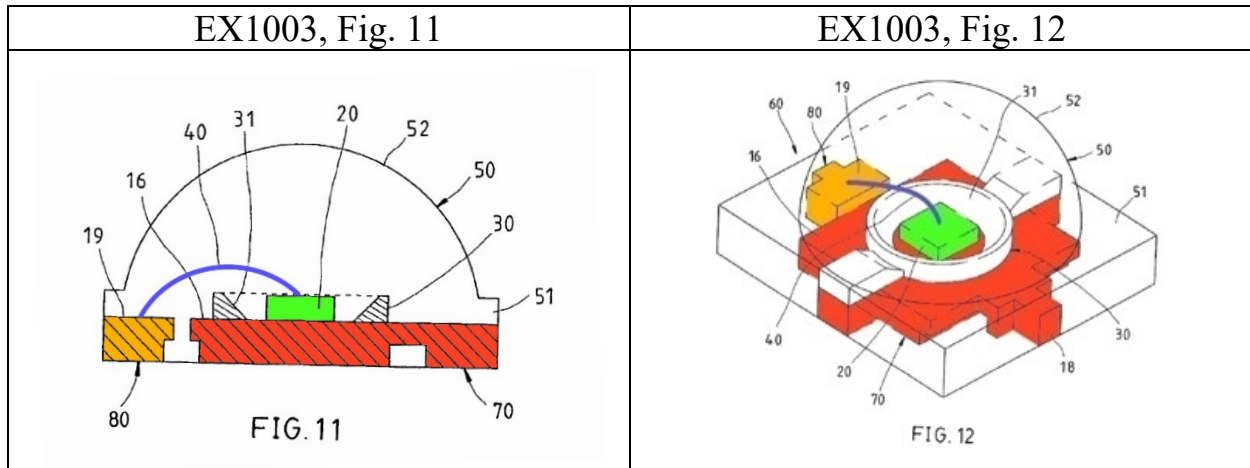
*bottom of the LED die 20 is electrically connected to the first terminal 70.* The reflecting ring 30, which is made of an opaque white plastic material, is molded on the top surface of the main plate 16 of the first terminal 70 by means of the injection molding technique and surrounds the die 20 and has the inner surface 31 facing upward as a slope. The conductive wire 40 is connected between the other electrode of the top surface of the die 20 and the top surface of the second terminal 80. The encapsulant 50, which material is the insulated epoxy resin with high transparency, encapsulates the die 20, the reflecting ring 30, and the conductive wire 40. Additionally, the base 51 of the encapsulant 50 covers the top surface of the first terminal 70 and the second terminal 80 and fills the space therebetween to remain two terminals 70 and 80 spaced apart in opposite relationship. The top of the encapsulant 50 is formed as the domed protrusion 52. When the LED package 60 is in use, generally take the first terminal 70 as positive electrode and the second terminal 80 as negative electrode such that the LED die 20 is charged by the electricity to emit white light. The emitted white light is then reflected from the inner surface 31 of the reflecting ring 30 to the dome-shaped protrusion of the encapsulant 50.

EX1003, [0025].

62. And as is also shown in Figures 11 and 12, the LED packaging further includes a “**conductive wire 40** [that] is connected between the other electrode of the top surface of the **die 20** and the top surface of the **second terminal 80**.”

EX1003, [0025]. Hsu also explains that the **conductive wire 40** can be made of gold, stating that it is used to “connect a top surface of the die 20 to a top surface of the separate arm 19 of the cell 11 with a gold conductive **wire 40** of 99% Au by wire

bonding technique such that the other electrode positioned on the top surface of the die 20 can be electrically connected with the separate arm 19.” EX1003, [0022].

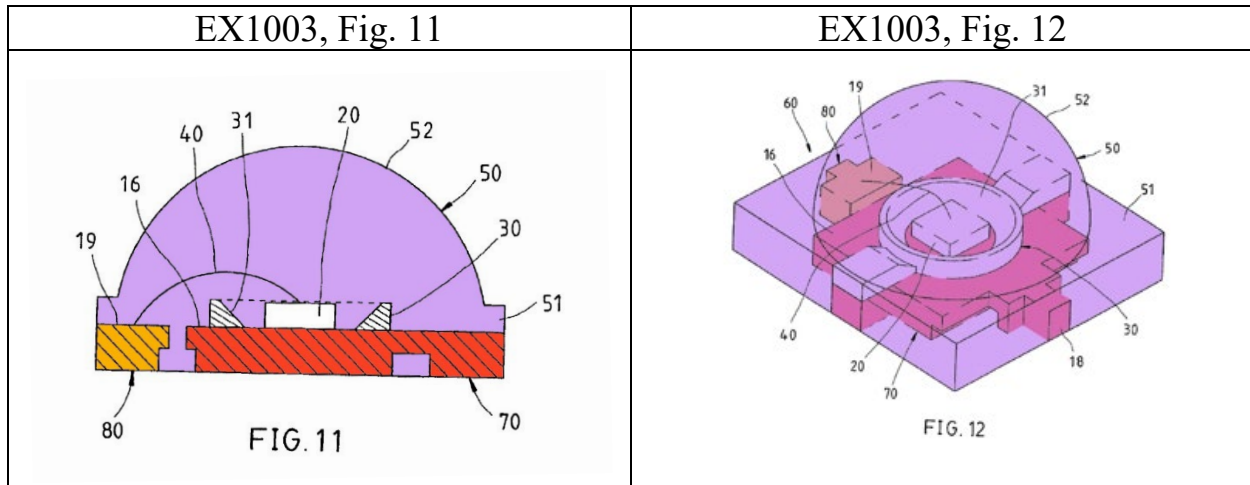


Step 4: Referring to FIGS. 8-9, **connect a top surface of the die 20 to a top surface of the separate arm 19 of the cell 11 with a gold conductive wire 40 of 99% Au** by wire bonding technique such that the other electrode positioned on the top surface of the die 20 can be electrically connected with the separate arm 19.

EX1003, [0022].

63. Furthermore, Hsu teaches that the LED package includes an “**encapsulant 50**, which material is [an] **insulated epoxy resin**” that provides structural and protective functions. EX1003, [0025]. The encapsulant (50) is designed to “cover[] the top surface of the **first terminal 70** and the **second terminal 80** and fill[] the space therebetween to remain two terminals 70 and 80 spaced apart in opposite relationship.” EX1003, [0025]. This configuration ensures

electrical isolation between the terminals. EX1003, [0025]; *see also* EX1003, Abstract, [0005], [0023], Claim 1, Claim 6.



Referring to FIGS. 11-12, the LED 60 package made by the foregoing fabricative process structurally includes a first terminal 70, a second terminal 80, the LED die 20, the reflecting ring 30, the conductive wire 40, and the encapsulant 50. The first terminal 70 is formed by the main plate 16, the extending arm 18 located at a right side of the main plate 16, and the bridges 17 respectively located at upper and lower sides of the main plates 16. Additionally, the first terminal 70 is made of an electrically conductive metal. The second terminal 80, which is the separate arm 19, is located at a left side of the first terminal 70 and spaced an appropriate distance apart from the first terminal 70 and made of the same electrically conductive metal. The LED die 20 has a bottom, which is smoothly bonded to a top surface of the main plate 16 of the first terminal 70 such that an electrode at the bottom of the LED die 20 is electrically connected to the first terminal 70. The reflecting ring 30, which is made of an opaque white plastic material, is molded on the top surface of the main plate 16 of the first terminal 70 by means of the injection molding technique and surrounds the die 20 and has the inner surface 31

facing upward as a slope. The conductive wire 40 is connected between the other electrode of the top surface of the die 20 and the top surface of the second terminal 80. *The encapsulant 50, which material is the insulated epoxy resin with high transparency, encapsulates the die 20, the reflecting ring 30, and the conductive wire 40. Additionally, the base 51 of the encapsulant 50 covers the top surface of the first terminal 70 and the second terminal 80 and fills the space therebetween to remain two terminals 70 and 80 spaced apart in opposite relationship. The top of the encapsulant 50 is formed as the domed protrusion 52.* When the LED package 60 is in use, generally take the first terminal 70 as positive electrode and the second terminal 80 as negative electrode such that the LED die 20 is charged by the electricity to emit white light. The emitted white light is then reflected from the inner surface 31 of the reflecting ring 30 to the dome-shaped protrusion of the encapsulant 50.

EX1003, [0025].

## 2. Iwamasa (EX1004)

64. Iwamasa teaches “a **lead frame**, methods of manufacturing the same, and a resin-sealed semiconductor device.” EX1004, [0001].

65. As illustrated in Figures 1(a) and 5, Iwamasa teaches a structure that includes a **Base 2**, with a “Die-Bonding Area 9 [] provided on the surface of **Base 2**.” EX1004, [0031].

Figures 1 (a) and (b) is a drawing of the minimum unit of Lead Frame 1. *As shown in Figure 1 (a), Die-Bonding Area 9 is provided on the surface of Base 2*, and Grooves 7 (7T, 7L, 7R, and 7B) are formed to stop the efflux of the die-bond material

around it. Groove 7 to stop the die-bond material consists of four Straight Grooves: 7T, 7L, 7R, and 7B. In order to prevent the efflux of the die-bond material, it is preferable that the groove to stop the efflux of the die-bond material is in a closed ring shape surrounding Die-Bonding Area 9. In the case of four Straight Grooves 7T, 7L, 7R, and 7B, as in the present embodiment, there are advantages such as that there are no diagonal lines or curved parts, making it easy to create a mold for press molding.

EX1004, [0031].

66. Iwamasa further explains that “**Semiconductor Dies** . . . are die-bonded to Die-Bonding Area 9 of **Base 2**,” and are thus physically attached.

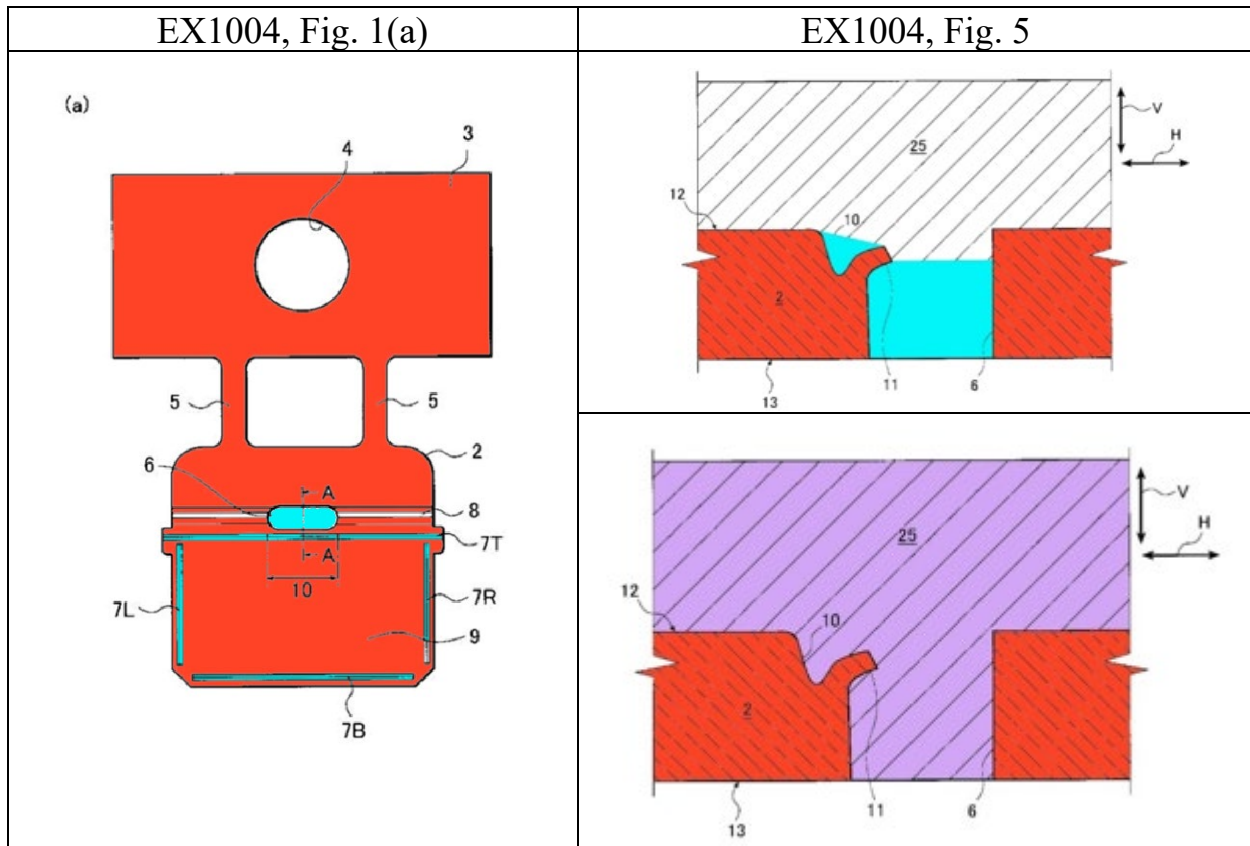
EX1004, [0040].

67. This arrangement also establishes electrical connectivity, because Iwamasa explicitly teaches that the dies are “electrically connected through **Base 2**.”

EX1004, [0040].

The rear surfaces on which the cathode K of Semiconductor Dies 21 and 22 are configured are die-bonded to Die-Bonding Area 9 of Base 2. This causes the cathode K of ***Semiconductor Dies 21 and 22 to be electrically connected through Base 2***. Each of Leads 23 and 24 is connected to Anode Terminals A1 and A2 on the surfaces of Semiconductor Dies 21 and 22. The inner ends of Semiconductor Dies 21 and 22 and Leads 23 and 24 connected thereto are resin-sealed with Sealing Resin 25. Sealing Resin 25 adheres to and connects Surface 12 of Base 2, the side surface and the inner surface of Through Hole 6. Back Surface 13 of Base 2 is exposed from Sealing Resin 25. This is to ensure that the back surface of Base 2 adheres to the heat sink, etc. during mounting. The top edge of the base is also exposed. This is to separate Coupling Part 5 shown in Figure 1 after implementing resin-sealing.

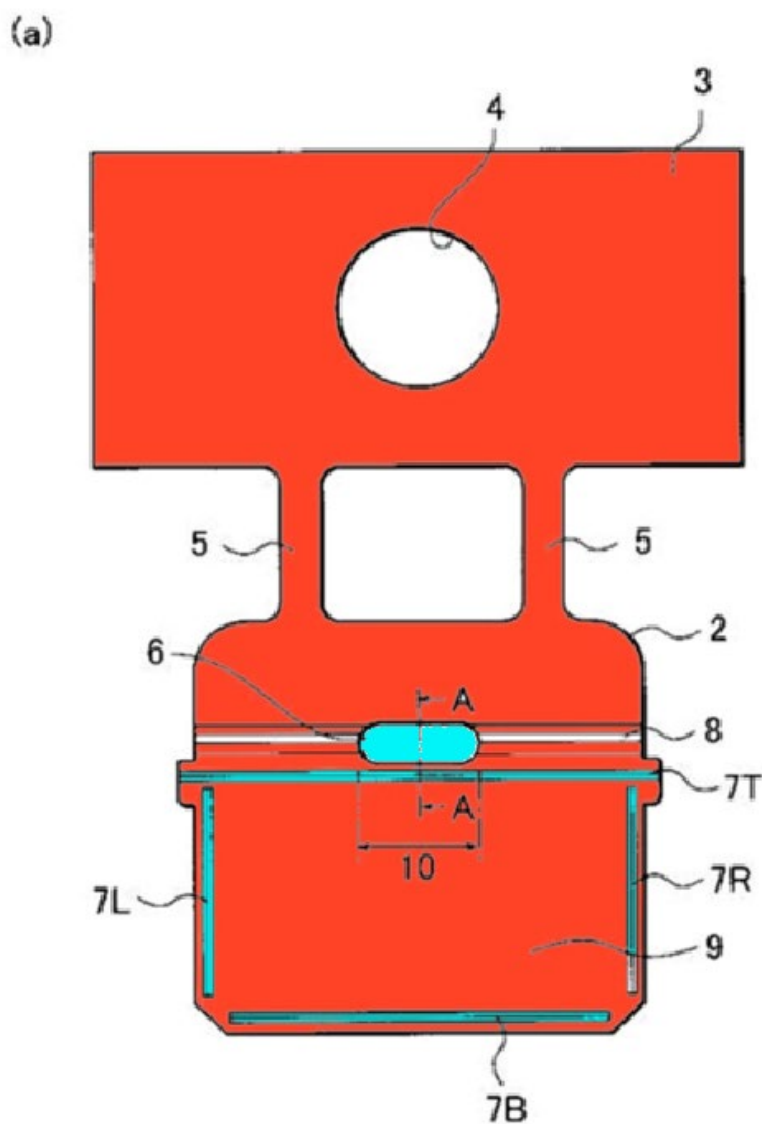
EX1004, [0040].



68. Iwamasa also discloses that the lead frame includes a “**Through Hole 6** [which] is provided adjacent to Die-Bonding Area 9.” EX1004, [0032].

69. Additionally, the top side of **Base 2** includes “**Grooves 7** (7T, 7L, 7R, and 7B).” EX1004, [0031].

70. Iwamasa describes that “**Groove 7** . . . consists of four **Straight Grooves**: 7T, 7L, 7R, and 7B.” EX1004, [0031].



EX1004, Figure 1(a).

71. Iwamasa describes that a “portion of the center of **Straight Groove 7T** is a **long groove 10** that separates Die-Bond Region 9 and **Through Hole 6**,” thereby

forming “Stopping Part 11 between Long Groove 10 and Through Hole 6.” EX1004, [0032].

72. Iwamasa teaches that this provides an “anchoring effect of the sealing resin.” EX1004, [0032].

Through Hole 6 is provided adjacent to Die-Bonding Area 9. As shown in Figure 2, Through Hole 6 is provided to communicate with Surface 12 provided with Die-Bonding Area 9 and Back Surface 13 thereof. *Straight Groove 7T exists, constituting Groove to stop the efflux of the die bond material 7 is interposed between Through Hole 6 and Groove to stop the afflux of bonding area 9. A portion of the center of Straight Groove 7T is a long groove 10 that separates Die-Bond Region 9 and Through Hole 6.* As shown in Figure 2, *the shape of Stopping Part 11 between Long Groove 10 and Through Hole 6 is changed toward the Through Hole 6 side to make the opening on the Surface 12 side of Through Hole 6 narrower, thereby providing the anchoring effect of the sealing resin.* Through Holes 6 is formed by a punching process, and it is a hole perpendicular to Front Surface 12 and Back Surface 13, continuing in the right angle from Front Surface 12 to Back Surface 13, except for the post-processed Stopping Part 11.

EX1004, [0032].

73. Iwamasa further explains that the “groove is filled with the sealing resin during the resin-sealing process.

74. Therefore, after resin sealing, the long groove helps improve the bond strength and adhesion between the sealing resin and the base.” EX1004, [0019].  
*See also*, EX1004, [Means of Solving the Problems] (“At least the retaining portion

was coated with a sealing **resin**, and preferably the through hole was filled with **resin** to improve the mechanical bond strength of the sealing **resin** and **Base 2**."); [0040] ("The inner ends of Semiconductor Dies 21 and 22 and Leads 23 and 24 connected thereto are resin-sealed with Sealing **Resin** 25. Sealing **Resin** 25 adheres to and connects Surface 12 of **Base 2**, the side surface and the inner surface of Through Hole 6. Back Surface 13 of **Base 2** is exposed from Sealing **Resin** 25. This is to ensure that the back surface of **Base 2** adheres to the heat sink, etc. during mounting; [0009] ("As the seal resin and the base are joined also inside the **through hole**, the bond strength and adhesion between the seal **resin** and the **base** are improved.").

Therefore, according to the present invention described in Claim 6, as the portion between the long groove and the through hole is reshaped toward the through-hole side in order to narrow the opening of the through hole, making it difficult for the sealing resin to escape from the through hold. In other words, the reshaped portion between the long groove and the through hole provides an anchoring effect as a stopper. Since the sealing resin and the base are joined even inside the through holes, the bond strength and adhesion between the seal resin and the base are improved. As the sealing resin covers the reshaped portion between the long groove and the through hole, a longer path can be formed from the exterior along the bonding surface of the base and the sealing resin to the semiconductor die, and this, in addition to the above-mentioned improvement in bonding strength and adhesion, improves the sealability of the package. From the viewpoint of bond strength and sealability, it is preferable to cover the entire through holes' inner surface with the sealing resin. Further, it is preferred to fill the through holes without leaving any gap. Since the back surface of the base is exposed from the sealing resin, the base acts as a heat dissipation

plate, improving heat dissipation. The through holes of the base can be easily formed to any size by punching, and the edges of the through holes are also less process-cured, making the second processing easier. If the long groove is pressed after the through hole is formed, the long groove may also be pressed in proximity to the through hole to reshape the part between the long groove and the through hole toward the through hole side to make the opening of the through holes narrower. This allows for simultaneous processing of the long groove and the portion between the long groove and through holes, thereby improving lead frame productivity. The number of through holes may be one or more than two, but increasing by even one provides sufficient bond strength. The long groove can stop the efflux of die bond materials such as solder, resin paste, etc. during the die-bonding process, and it separates the die bonding area from the through holes, preventing the efflux of the die bond material into the through holes. Since there is no bottom in the through hole, it is difficult to collect even if die bond material flows into the through hole. *As long as the long groove is not filled with a die bond material, etc., the long groove is filled with the sealing resin during the resin-sealing process. Therefore, after resin sealing, the long groove helps improve the bond strength and adhesion between the sealing resin and the base.*

EX1004, [0019].

### 3. Claims 1 And 6

#### i. [1Pre, 6Pre] A light emitting diode (LED) package, comprising

75. I understand that the preamble may not limit the claims. Regardless, Hsu teaches preambles [1Pre] and [6Pre].

76. Hsu discloses an “LED package and the process [of] making the same.”

EX1003, Title. For instance, in Figure 12 Hsu illustrates “a finished LED package



(“the LED 60 package . . . includes **a first terminal 70**” and “**a second terminal 80**.”). Hsu further explains that “[w]hen the LED package 60 is in use, generally [] the **first terminal 70** [is taken] as positive electrode and the **second terminal 80** as negative electrode such that the LED die 20 is charged by the electricity to emit white light.” EX1003, [0025].

Referring to FIGS. 11-12, the **LED 60 package** made by the foregoing fabricative process structurally includes **a first terminal 70, a second terminal 80**, the LED die 20, the reflecting ring 30, the conductive wire 40, and the encapsulant 50. The first terminal 70 is formed by the main plate 16, the extending arm 18 located at a right side of the main plate 16, and the bridges 17 respectively located at upper and lower sides of the main plates 16. Additionally, the first terminal 70 is made of an electrically conductive metal. The second terminal 80, which is the separate arm 19, is located at a left side of the first terminal 70 and spaced an appropriate distance apart from the first terminal 70 and made of the same electrically conductive metal. The LED die 20 has a bottom, which is smoothly bonded to a top surface of the main plate 16 of the first terminal 70 such that an electrode at the bottom of the LED die 20 is electrically connected to the first terminal 70. The reflecting ring 30, which is made of an opaque white plastic material, is molded on the top surface of the main plate 16 of the first terminal 70 by means of the injection molding technique and surrounds the die 20 and has the inner surface 31 facing upward as a slope. The conductive wire 40 is connected between the other electrode of the top surface of the die 20 and the top surface of the second terminal 80. The encapsulant 50, which material is the insulated epoxy resin with high transparency, encapsulates the die 20, the reflecting ring 30, and the conductive wire 40. Additionally, the base 51 of the

encapsulant 50 covers the top surface of the first terminal 70 and the second terminal 80 and fills the space therebetween to remain two terminals 70 and 80 spaced apart in opposite relationship. The top of the encapsulant 50 is formed as the domed protrusion 52. *When the LED package 60 is in use, generally take the first terminal 70 as positive electrode and the second terminal 80 as negative electrode such that the LED die 20 is charged by the electricity to emit white light.* The emitted white light is then reflected from the inner surface 31 of the reflecting ring 30 to the dome-shaped protrusion of the encapsulant 50.

EX1003, [0025].

80. Hsu also describes the structure of the terminals, stating that “[t]he **first terminal 70** is formed by the main plate 16, the extending arm 18 located at a right side of the main plate 16, and the bridges 17 respectively located at upper and lower sides of the main plates 16.” EX1003, [0025]. Additionally, “[t]he **second terminal 80**[ ] is the separate arm 19.” EX1003, [0025].

81. Claim 6 of Hsu also specifies that the LED package comprises “platelike **first terminal** made of an electrically conductive metal” and “a **second terminal** made of the electrically conductive metal and located at a side of said first terminal and spaced apart from said first terminal with a predetermined space.” EX1003, Claim 6. Hsu also teaches that “an LED die [has] a bottom bonded on a top surface of said **first terminal** such that an electrode located on the bottom of said die is electrically connected to said **first terminal**,” while “a conductive wire

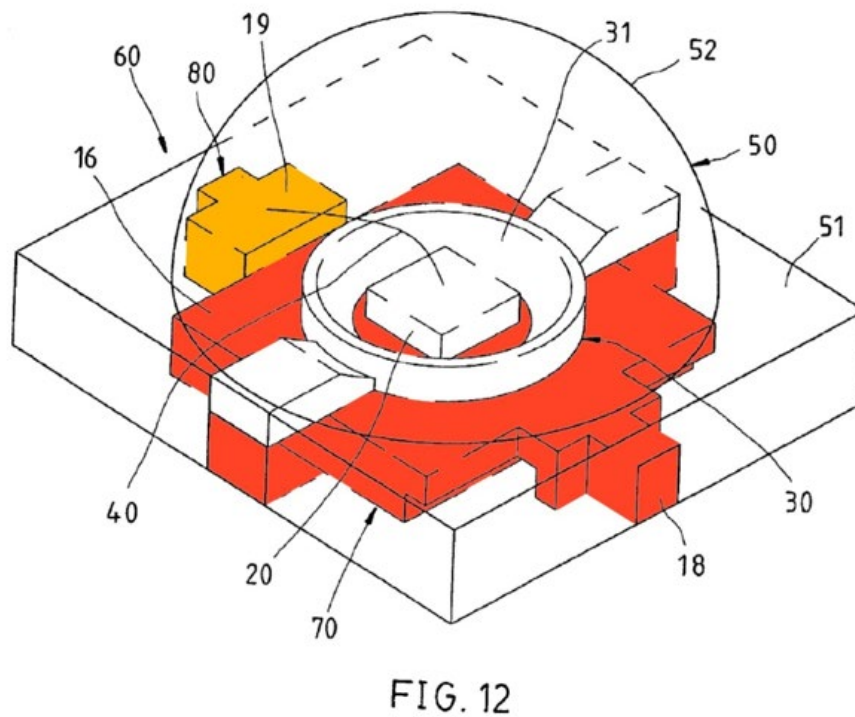
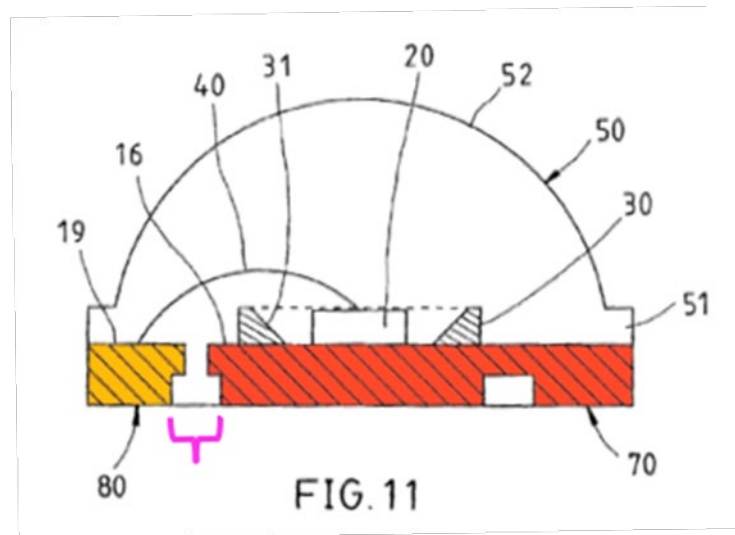
[connects] the other electrode on a top surface of said die to a top surface of said **second terminal**.” EX1003, Claim 6. *See also* EX1003, [0005], Claim 1.

Claim 6: *An LED package comprising:*  
*a platelike first terminal made of an electrically conductive metal;*  
*a second terminal made of the electrically conductive metal* and located at a side of said first terminal and spaced apart from said first terminal with a predetermined space;  
*an LED die having a bottom bonded on a top surface of said first terminal such that an electrode located on the bottom of said die is electrically connected to said first terminal;*  
a reflecting ring made of opaque white plastic and formed on the top surface of said first terminal by means of the molding technique to surround said die, said reflecting ring being provided with an upward sloping inner surface;  
a conductive wire connected the other electrode on a top surface of said die to a top surface of said second terminal, and  
an encapsulant made of insulated transparent epoxy resin and encapsulating said die, said reflecting ring and said conductive wire and covering said first terminal and said second terminal and filling the space between the first and second terminals to remain two terminals spaced apart, wherein said encapsulant has a top domelike protrusion.

EX1003, Claim 6.

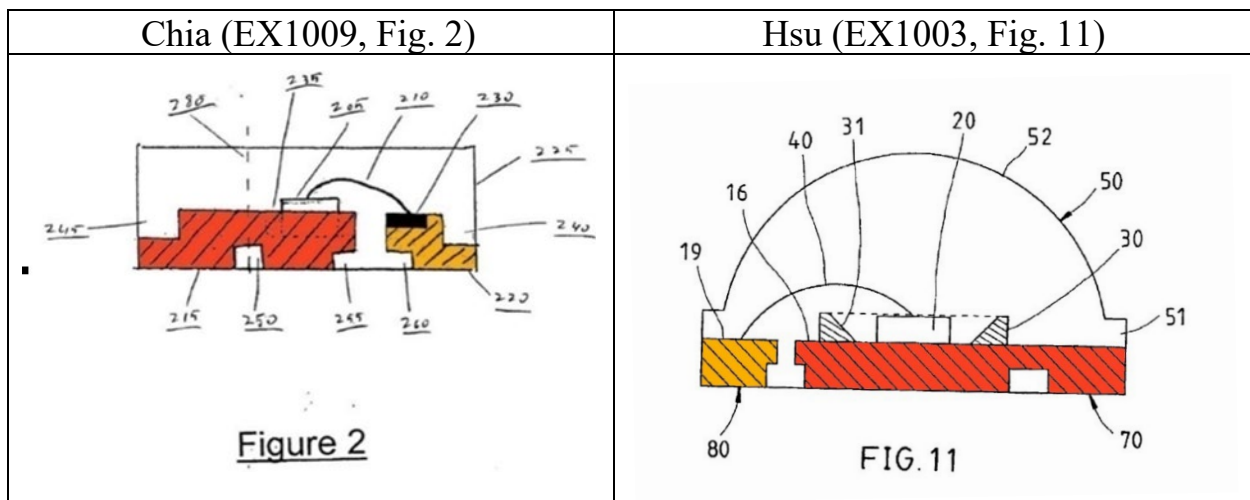
82. Hsu discloses that the **second terminal** is positioned to the side of the **first terminal** and separated from it by a defined space. EX1003, Claim 6 (“a **second terminal** made of the electrically conductive metal and located at a side of said **first terminal** and spaced apart from said **first terminal** with a predetermined space”). I have indicated this space below in Figure 11 with a **dark pink bracket**. Hsu further describes that “[t]he **second terminal 80**, which is the separate arm 19,

is located at a left side of the **first terminal 70** and spaced an appropriate distance apart from the **first terminal 70** and made of the same electrically conductive metal.” EX1003, [0025]. *See also* EX1003, [0005], Claim 1.



EX1003, Figs. 11 and 12.

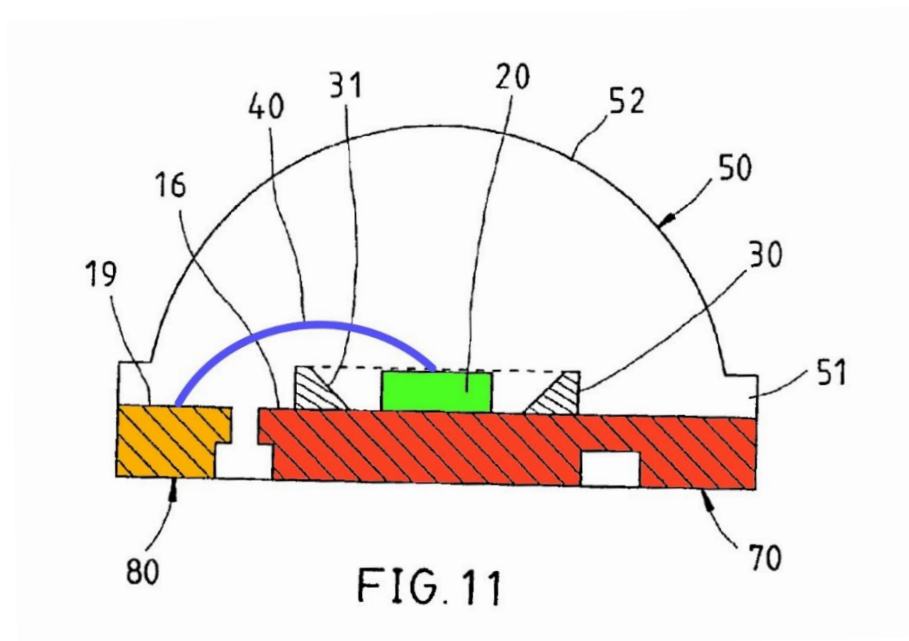
83. Hsu's **first terminal 70** and **second terminal 80** are just like the structures that the examiner determined to meet the claimed **first lead frame** and **second lead frame** during prosecution of the '913 Patent. Specifically, the examiner found that U.S. Patent Publication No. 2005/051149 ("Chia") disclosed in "at least figures 2-4 ... [a] light emitting diode (LED) package comprising: a **first lead frame 215** and a **second lead frame 220** separated from each other." EX1008, 80. As I have illustrated below, Chia's **first lead frame 215** and **second lead frame 220** closely resemble Hsu's **first terminal 70** and **second terminal 80**, both in structure and in their separation from one another.



- iii. [1B, 6B] an **LED chip** disposed on the **first lead frame** and electrically connected with **second lead frame**; and

84. Hsu teaches [1B] and [6B].

85. In particular, in Figures 11 and 12, Hsu shows an “LED 60 package,” which includes “**LED die 20.**” EX1003, [0025]. *See also* EX1003, Abstract, [0005], [0020], [0022], Claim 1, Claim 6.



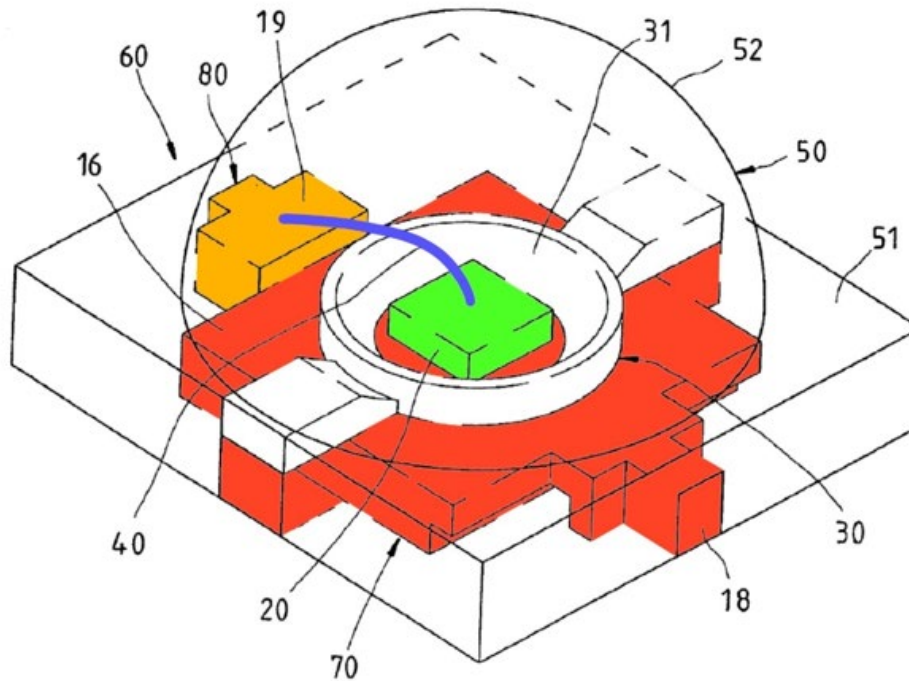


FIG. 12

EX1003, Figs. 11–12.

86. Hsu discloses that the “**LED die 20** has a bottom, which is smoothly bonded to a top surface of the main plate 16 of the **first terminal 70** such that an electrode at the bottom of the **LED die 20** is electrically connected to the **first terminal 70**,” to form an electrical connection between the LED die and the **first terminal**. EX1003, [0025]. Hsu further explains that “a white **LED die 20** is bonded on a top surface of each of the **main plates 16** of the frame 10 by means of silver adhesives (not shown).” EX1003, [0020]. *See also* EX1003, Abstract, [0005], [0026], Claim 1, Claim 6.

87. Hsu further teaches that a “**conductive wire 40** is connected between the other electrode of the top surface of the **die 20** and the top surface of the **second terminal 80**.” EX1003, [0025]. This wire establishes an electrical connection between the **LED die** and the **second terminal 80**. EX1003, [0025]; *see also* Figures 11 and 12. Hsu also explains that the conductive wire “[c]onnect[s] a top surface of the **die 20** to a top surface of the **separate arm 19** of the cell 11 with a gold conductive wire 40 of 99% Au by wire bonding technique such that the other electrode positioned on the top surface of the **die 20** can be *electrically connected with the separate arm 19*.” EX1003, [0022]. Therefore, Hsu specifically teaches an electrical contact between the **LED die** and the **second terminal**. *See also* EX1003, [0005], Abstract, Claim 1, Claim 6.

Step 4: Referring to FIGS. 8-9, *connect a top surface of the die 20 to a top surface of the separate arm 19 of the cell 11 with a gold conductive wire 40 of 99% Au by wire bonding technique such that the other electrode positioned on the top surface of the die 20 can be electrically connected with the separate arm 19.*

EX1003, [0022].

iv. [1C, 6C] a **resin** covering at least portions of surfaces of the **first** and **second lead frames**, wherein:

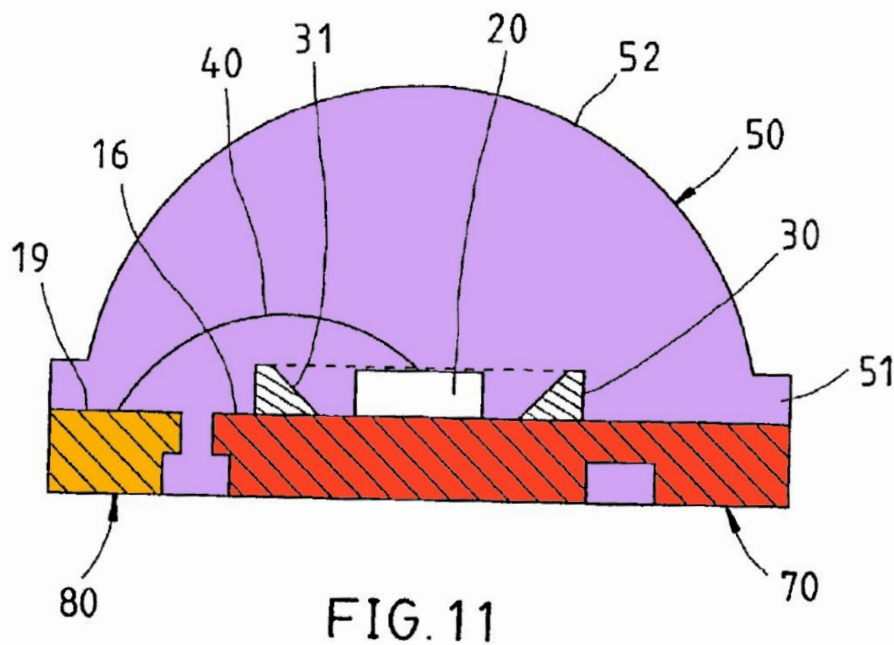
88. Hsu teaches [1C] and [6C].

89. Hsu discloses an “**encapsulant 50**, which material is the insulated epoxy **resin**.” EX1003, [0025]. This **encapsulant 50** “covers the top surface of the **first terminal 70** and the **second terminal 80**.” EX1003, [0025]. This is illustrated in Figures 11 and 12, which show the encapsulant applied over the **first terminal 70** and the **second terminal 80**. EX1003, [0025].

Referring to FIGS. 11-12, the LED 60 package made by the foregoing fabricative process structurally includes a first terminal 70, a second terminal 80, the LED die 20, the reflecting ring 30, the conductive wire 40, and the encapsulant 50. The first terminal 70 is formed by the main plate 16, the extending arm 18 located at a right side of the main plate 16, and the bridges 17 respectively located at upper and lower sides of the main plates 16. Additionally, the first terminal 70 is made of an electrically conductive metal. The second terminal 80, which is the separate arm 19, is located at a left side of the first terminal 70 and spaced an appropriate distance apart from the first terminal 70 and made of the same electrically conductive metal. The LED die 20 has a bottom, which is smoothly bonded to a top surface of the main plate 16 of the first terminal 70 such that an electrode at the bottom of the LED die 20 is electrically connected to the first terminal 70. The reflecting ring 30, which is made of an opaque white plastic material, is molded on the top surface of the main plate 16 of the first terminal 70 by means of the injection molding technique and surrounds the die 20 and has the inner surface 31 facing upward as a slope. The conductive wire 40 is connected between the other electrode of the top surface of the die 20 and the top surface of the second terminal 80. ***The encapsulant 50, which material is the insulated epoxy resin with high transparency, encapsulates the die 20, the reflecting ring 30, and the conductive wire 40. Additionally, the base 51 of the***

*encapsulant 50 covers the top surface of the first terminal 70 and the second terminal 80 and fills the space therebetween to remain two terminals 70 and 80 spaced apart in opposite relationship. The top of the encapsulant 50 is formed as the domed protrusion 52. When the LED package 60 is in use, generally take the first terminal 70 as positive electrode and the second terminal 80 as negative electrode such that the LED die 20 is charged by the electricity to emit white light. The emitted white light is then reflected from the inner surface 31 of the reflecting ring 30 to the dome-shaped protrusion of the encapsulant 50.*

EX1003, [0025].



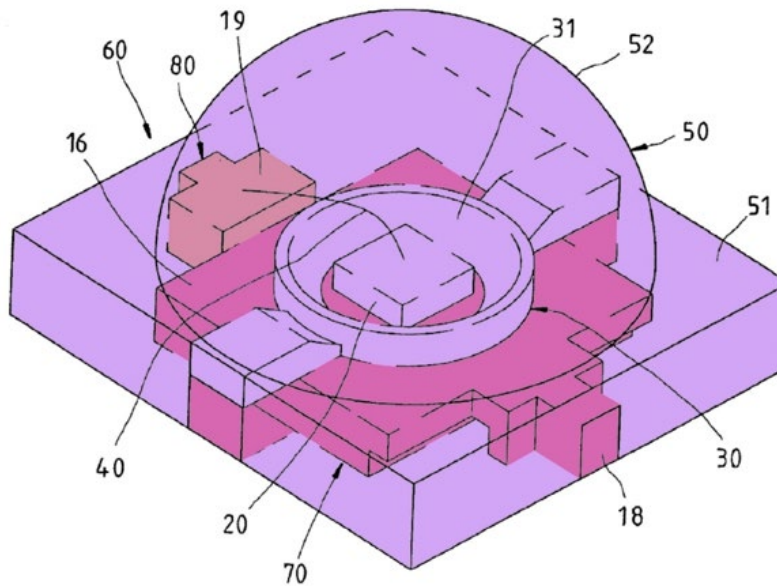


FIG. 12

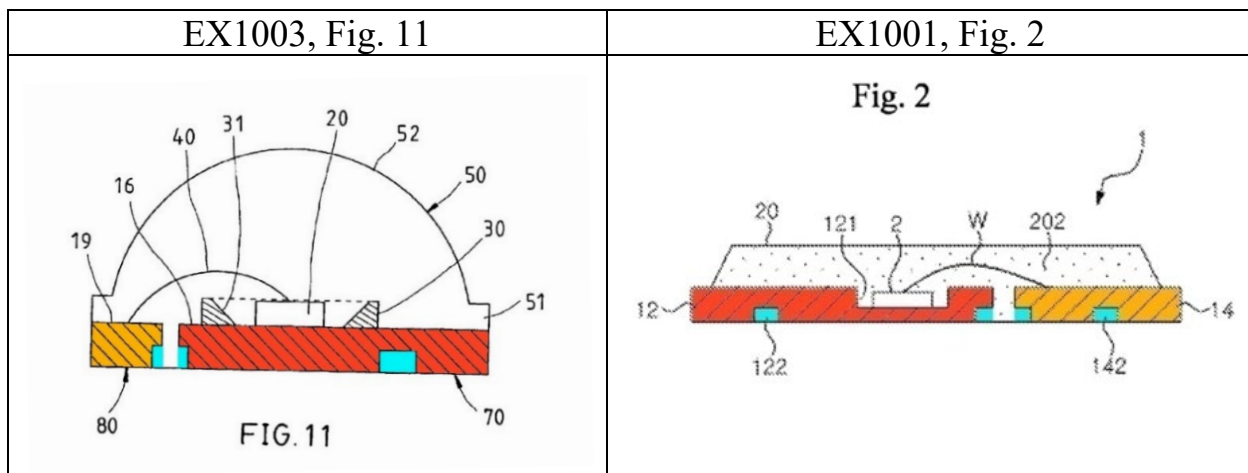
EX1003, Figs. 11-12.

90. Hsu further describes that the **encapsulant** is formed using epoxy **resin**. EX1003, [0005] “Step D: Form an **encapsulant** on each cell of the frame with epoxy resin by means of the molding technique, wherein the **encapsulant** encapsulates the die, the reflecting ring and the conductive wire, and covers the main plate and the separate arm and also fills the space between the main plate and the separate arm to remain their spaced apart in opposite relationship. Additionally, the **encapsulant** has a top domelike protrusion.” EX1003, [0005]. *See also* EX1003, Abstract, [0023], [0025], Claim 1, Claim 6.

- v. [1D, 6D] at least one of the **first** and **second lead frames** comprises **resin-holding components** disposed along adjacent sides of one of the **first** and **second lead frames**, the **resin-holding components** being separated from each other at corners of the adjacent sides; and:
- vi. [1E] the **resin-holding components** are disposed on two adjacent sides of each of the **first lead frame** and the **second lead frame**.

91. Hsu in combination with Iwamasa teaches [1D], [1E], and [6D].

92. As an initial matter, with respect to [1D] and [6D], the **first terminal 70** and **second terminal 80** each have **grooves** along their lateral and bottom sides. And these **grooves** are filled with **resin**. Therefore, the **grooves** function as **resin-holding components**. Note that they also closely resemble the “**openings or grooves are formed on the lead frames**” illustrated in Figure 2 of the '913 Patent. EX1001, 3:16–21.



93. These **grooves** function as **resin-holding components** because they retain **resin**, as demonstrated by Hsu's disclosure that the "**encapsulant 50 . . . with epoxy resin**," "fills the openings of the cell." EX1003, [0023].

Step 5: Referring to FIGS. 10-11, form an encapsulant 50 on each of the cells 11 of the frame 10 with epoxy resin by means of the injection molding technique. *The encapsulant 50 has a rectangle base 51, which corresponds to the cell 11 in size and fills the openings of the cell 11 and covers the surface of the frame 10 with a predetermined thickness.* All the bases 51 of the encapsulants 50 are integrated together initially, so that the encapsulants 50 not only cover the main plates 16, the bridges 17, the extending arms 18 and the separate arms 19 of the cells 11 but also the dividing bars 14 and 15 of the frame 10. In this embodiment of the present invention, the base 51 is higher than the frame 10 and substantially as high as the reflecting ring 30. The encapsulant 50 has a top domelike protrusion 52, which is located on the top of the base 51 and integrated with the base 51, and not only encapsulates the die 20, the reflecting ring 30, and the conductive wire 40 on the cell 11 to maintain the mechanism of the die 20 and to prevent water from infiltration, but also reflects the light emitted by the die 20 through the inner surface 31 of the reflecting ring 30. In addition, the encapsulant 50 is an insulator.

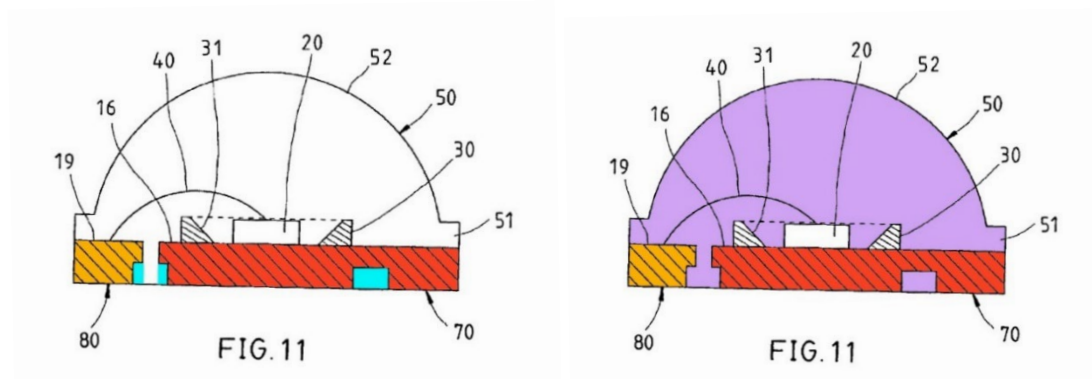
EX1003, [0023].

94. Hsu further explains that the **epoxy resin** "fills the space between the **main plate** and the **separate arm**," reinforcing that these grooves serve to contain and support the encapsulant. EX1003, [0005].

To achieve the foregoing objective of the present invention, the process for fabricating LED packages involves the following steps. Step A: Provide a platelike frame made of an electrically

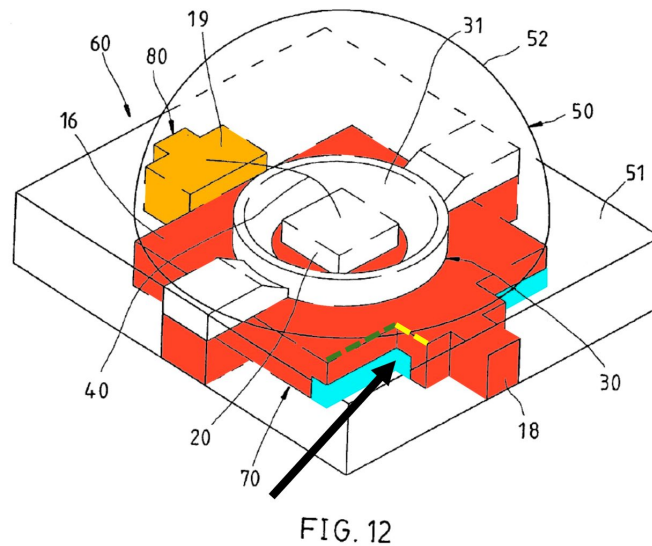
conductive metal. The frame has a plurality of cells, each of which includes a main plate and a separate arm, and no connection but a space between the main plate and the separate arm. Step B: Attach an LED die on a top surface of each main plate of the frame so as to electrically connect an electrode on a bottom side of the die to the main plate. Moreover, form a reflecting ring on each main plate with a molding technique, wherein the reflecting ring is made of opaque white plastic and has an upward sloping inner surface, and the die is positioned in the center of the reflecting ring. Step C: Connect the other electrode on a top surface of the die to a top surface of the separate arm with a conductive wire by means of wire bonding technique. Step D: ***Form an encapsulant on each cell of the frame with epoxy resin by means of the molding technique, wherein the encapsulant encapsulates the die, the reflecting ring and the conductive wire, and covers the main plate and the separate arm and also fills the space between the main plate and the separate arm to remain their spaced apart in opposite relationship. Additionally, the encapsulant has a top domelike protrusion.*** Step E: Cut the platelike frame substantially according to the size of each of the cells such that a plurality of LED packages are made.

EX1003, [0005].



EX1003, Fig. 11.

95. Furthermore, with respect to [1D] and [6D], Hsu teaches “**resin-holding components**” positioned along two adjacent sides of the first lead frame, as I have shown in Figure 12 with dark green and yellow dashed lines. EX1003, Fig. 11, Fig. 12. *See also* EX1003, [0025], Claim 1, Claim 6.



EX1003, Fig. 12.

96. Additionally, the combination of Hsu and Iwamasa renders [1D], [1E], and [6D] obvious. As shown above, Hsu discloses **grooves** that are connected rather than “separated from” each other at the corner (see black arrow) where two laterally adjacent sides of the **first terminal 70** meet. I have indicated this with dark green and yellow dashed lines. EX1003, Fig. 11, Fig. 12. Hsu also does not explicitly disclose **grooves** disposed on two adjacent sides of the **second terminal 80**.

97. Nevertheless, Hsu and Iwamasa together render [1D], [1E], and [6D] obvious and teach **resin-holding components** disposed on two adjacent sides of both the **first terminal 70** and the **second terminal 80**, where these components are separated at the corner between the upper and lateral sides of each terminal. *See* EX1001, 3:21–25 (referring to the upper surface of the LED package as an “upper side”), 6:18–21 (discussing “opposite sides of the lead frames 12, 14 facing each other”).

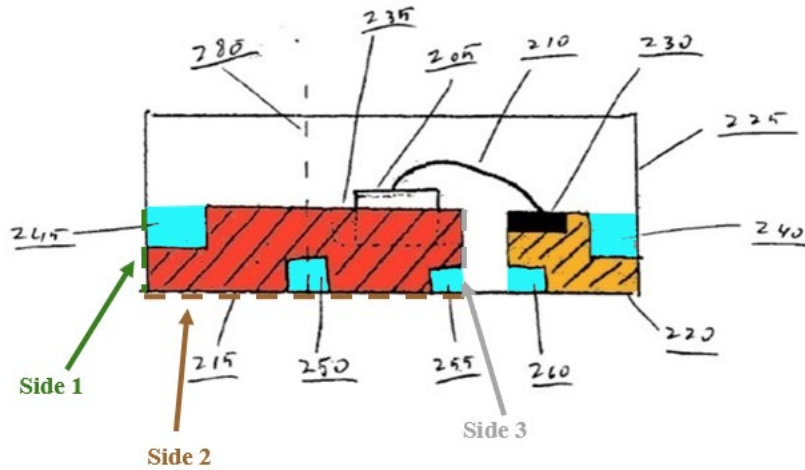
Moreover, an inside surface of the chip mounting recess serves to improve luminescence efficiency, as compared to a conventional PCB type LED package that is configured to reflect light emitted from the LED chip to an *upper side*.

EX1001, 3:21–25.

As clearly shown in FIG. 6, the first and second lead frames 12, 14 include first and second slant parts 125, 145, *which are formed on opposite sides of the lead frames 12, 14 facing each other in an inclined state*.

EX1001, 6:18–21.

98. I note that during prosecution of the '913 Patent, the Examiner found that “Chia illustrates in figures 2–4 the **resin-holding components 240, 245, 250, 255, 260** are disposed on three sides of at least one of the **first** and **second lead frames 215, 220**.” EX1008, 124.



### Figure 2

EX1009, Fig. 2.

99. Iwamasa, for instance, discloses a **lead frame** incorporating **grooves and holes** that serve the same purpose as the claimed **resin-holding components**.

Iwamasa describes that the *top surface* of its **Base 2** includes “**Grooves 7** (7T, 7L, 7R, and 7B),” and specifies that “**Groove 7** . . . consists of four **Straight Grooves: 7T, 7L, 7R, and 7B.**” EX1004, [0031].

Figures 1 (a) and (b) is a drawing of the minimum unit of Lead Frame 1. As shown in Figure 1 (a), Die-Bonding Area 9 is provided on the surface of Base 2, and Grooves 7 (7T, 7L, 7R, and 7B) are formed to stop the efflux of the die-bond material around it. Groove 7 to stop the die-bond material consists of four Straight Grooves: 7T, 7L, 7R, and 7B. In order to prevent the efflux of the die-bond material, it is preferable that the groove to stop the efflux of the die-bond material is in a closed ring shape surrounding Die-Bonding Area 9. In the case of four Straight Grooves 7T, 7L, 7R, and 7B, as in the present embodiment, there

are advantages such as that there are no diagonal lines or curved parts, making it easy to create a mold for press molding.

EX1004, [0031].

100. These **grooves** allow resin to flow in during the sealing process, improving adhesion. EX1004, [0031]. Iwamasa further states that “**groove** is filled with the sealing **resin** during the resin-sealing process. Therefore, after **resin** sealing, the long **groove** helps improve the bond strength and adhesion between the sealing **resin** and the **base**.” EX1004, [0019]; *see also* EX1004, [0040].

Therefore, according to the present invention described in Claim 6, as the portion between the long groove and the through hole is reshaped toward the through-hole side in order to narrow the opening of the through hole, making it difficult for the sealing resin to escape from the through hold. In other words, the reshaped portion between the long groove and the through hole provides an anchoring effect as a stopper. Since the sealing resin and the base are joined even inside the through holes, the bond strength and adhesion between the seal resin and the base are improved.

As the sealing resin covers the reshaped portion between the long groove and the through hole, a longer path can be formed from the exterior along the bonding surface of the base and the sealing resin to the semiconductor die, and this, in addition to the above-mentioned improvement in bonding strength and adhesion, improves the sealability of the package. From the viewpoint of bond strength and sealability, it is preferable to cover the entire through holes' inner surface with the sealing resin. Further, it is preferred to fill the through holes without leaving any gap.

Since the back surface of the base is exposed from the sealing resin, the base acts as a heat dissipation plate, improving heat dissipation.

The through holes of the base can be easily formed to any size by punching, and the edges of the through holes are also less

process-cured, making the second processing easier. If the long groove is pressed after the through hole is formed, the long groove may also be pressed in proximity to the through hole to reshape the part between the long groove and the through hole toward the through hole side to make the opening of the through holes narrower. This allows for simultaneous processing of the long groove and the portion between the long groove and through holes, thereby improving lead frame productivity.

The number of through holes may be one or more than two, but increasing by even one provides sufficient bond strength.

The long groove can stop the efflux of die bond materials such as solder, resin paste, etc. during the die-bonding process, and it separates the die bonding area from the through holes, preventing the efflux of the die bond material into the through holes. Since there is no bottom in the through hole, it is difficult to collect even if die bond material flows into the through hole. As long as the long groove is not filled with a die bond material, etc., the long groove is filled with the sealing resin during the resin-sealing process. Therefore, after resin sealing, the long groove helps improve the bond strength and adhesion between the sealing resin and the base.

EX1004, [0019]

The rear surfaces on which the cathode K of Semiconductor Dies 21 and 22 are configured are die-bonded to Die-Bonding Area 9 of Base 2. This causes the cathode K of Semiconductor Dies 21 and 22 to be electrically connected through Base 2.

Each of Leads 23 and 24 is connected to Anode Terminals A1 and A2 on the surfaces of Semiconductor Dies 21 and 22.

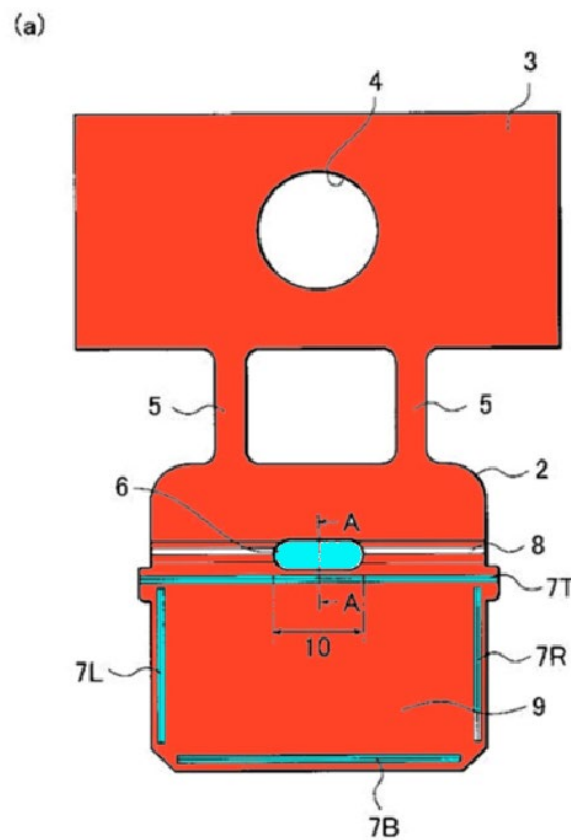
The inner ends of Semiconductor Dies 21 and 22 and Leads 23 and 24 connected thereto are resin-sealed with Sealing Resin 25. Sealing Resin 25 adheres to and connects Surface 12 of Base 2, the side surface and the inner surface of Through Hole 6.

Back Surface 13 of Base 2 is exposed from Sealing Resin 25. This is to ensure that the back surface of Base 2 adheres to the heat sink, etc. during mounting.

The top edge of the base is also exposed. This is to separate Coupling Part 5 shown in Figure 1 after implementing resin-sealing.

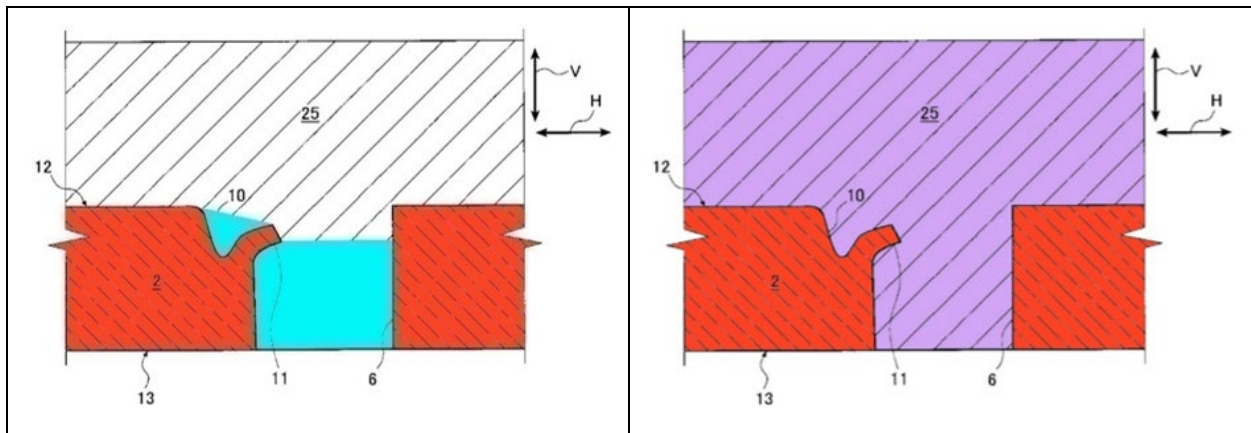
EX1004, [0040]

101. Iwamasa also explains that “the seal **resin** and the **base** are joined also inside the **through hole**, [so] the bond strength and adhesion between the seal **resin** and the **base** are improved.” EX1004, [0009].



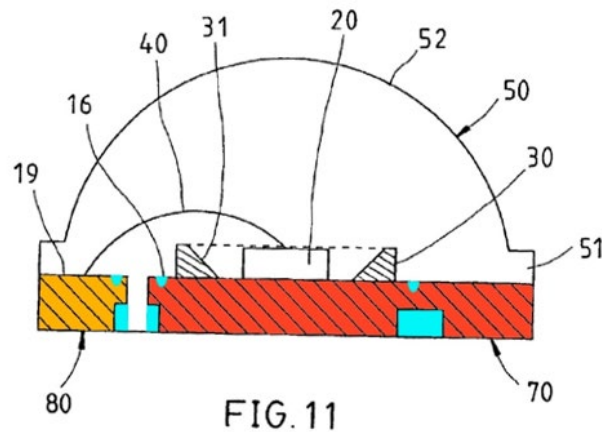
EX1004, Fig. 1(a).

102. A cross-sectional view of **groove 7T** near **through-hole 6** is provided by Iwamasa in Figure 5. As depicted, the **resin** fills both the **groove** and **through-hole 6** which enhances the “bond strength and adhesion between the seal **resin** and the **base**.” EX1004, [0009].

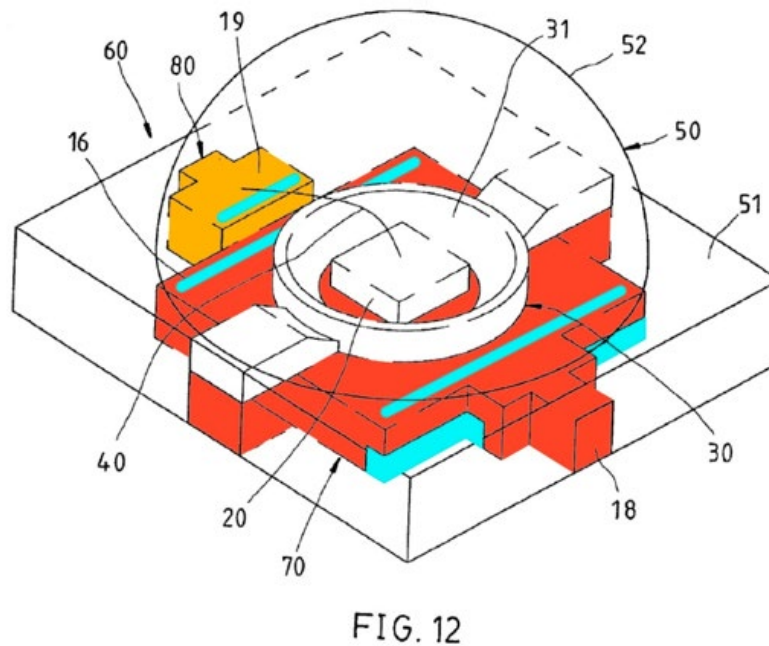


EX1004, Fig. 5.

103. A POSITA would have recognized that modifying Hsu by incorporating Iwamasa's **grooves** on the upper sides of both the **first lead frame** and **second lead frame** would have been an obvious design choice. Given the function of these **grooves** in improving resin adhesion, such a modification would have been straightforward and achievable with a reasonable expectation of success. Implementing these grooves in Hsu's structure would result in the configuration illustrated in the modified Figures 11 and 12 below.



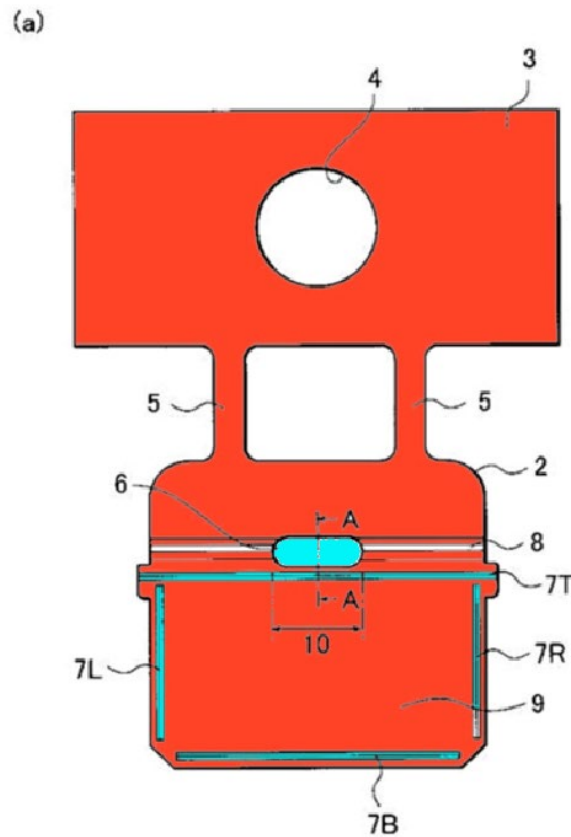
EX1003, Fig. 11 (modified).



EX1003, Fig. 12 (modified).

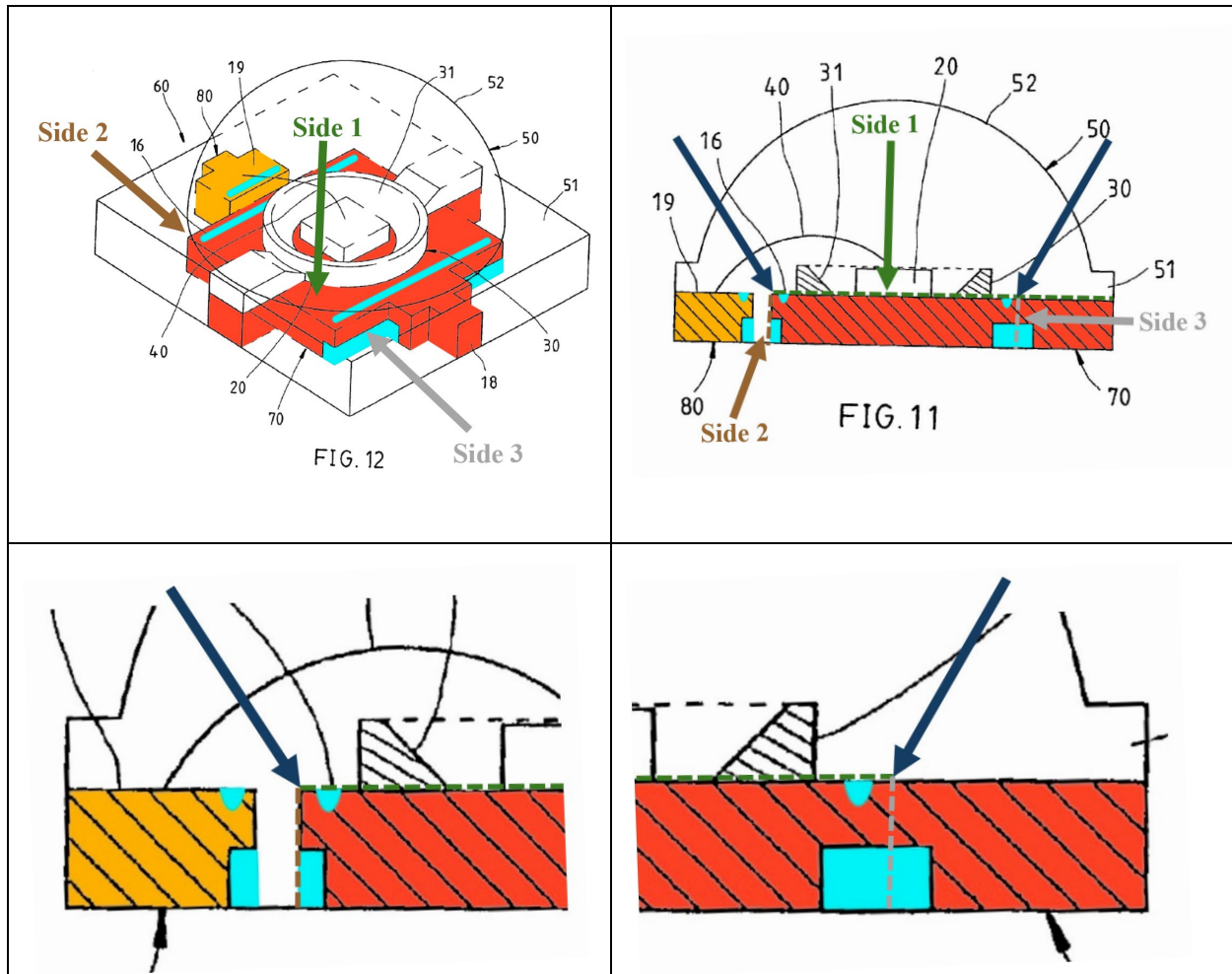
104. This proposed Hsu-Iwamasa modification simply involves adding **grooves** along the **upper side**, as taught by Iwamasa, along the **upper side** (“**Side 1**”) of Hsu’s **first terminal 70**. Just as Iwamasa’s **grooves 7T, 7L, 7B, and 7R** are

within the main body portion of the top side of the **base** (**groove 7T**).



where the upper side and **lateral side 2** meet (see arrow). Additionally, Hsu's **first**

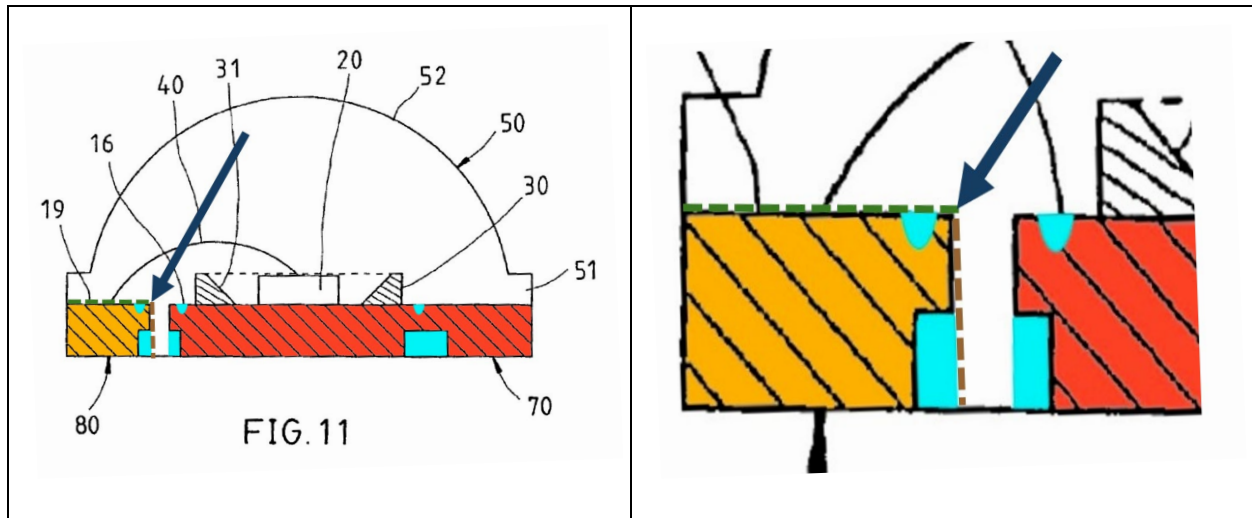
**terminal 70** includes a **groove** along its **lateral side** (“**Side 3**”) and another **groove** along the adjacent **upper side**, with these **grooves** also remaining separate at the **corner** where the **upper side** and **lateral side** intersect.



EX1003, Figs. 11 and 12 (modified as Hsu+Iwamasa).

105. Similarly, as with the **first terminal 70**, adding additional **grooves** along the **upper side** of Hsu’s **second terminal 80** would have been a straightforward modification. The added **groove** on the **upper side** of the **second terminal 80** remains separated from the **groove** on its adjacent **lateral side**, with

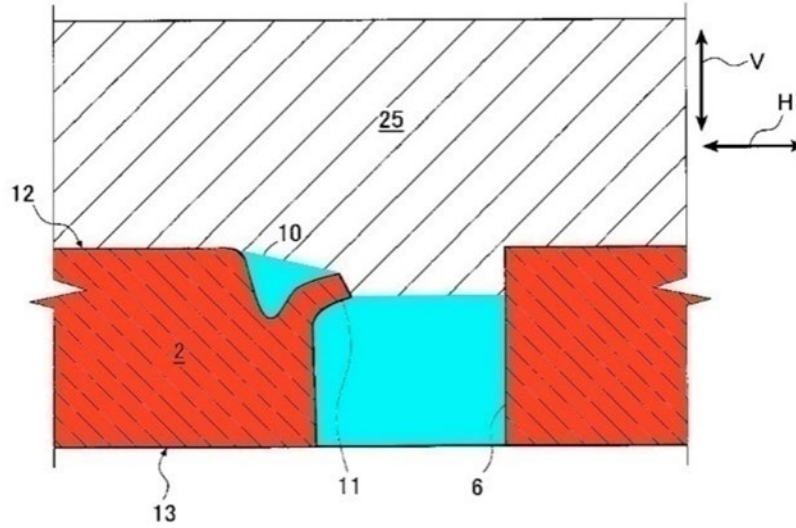
separation occurring at the **corner** where the **upper side** and adjacent **lateral side** meet.



EX1003, Fig. 11 (modified as Hsu+Iwamasa).

106. The proposed modification closely parallels Iwamasa's **groove 10** near **through hole 6**, which includes a "**Stopping Part 11**" positioned between two spaces that independently enhance bonding and adhesion between the **resin** and the underlying **base** terminal. See EX1004, [0009], [0019]. As illustrated in Figure 5, Iwamasa teaches that "**Long Groove 10** is positioned in some proximity to **Through Hole 6**," creating "**Stopping Part 11**." EX1004, [0038]; *see also* EX1004, [0036]. Furthermore, Iwamasa explains that "the shape of **Stopping Part 11** between **Long Groove 10** and **Through Hole 6** . . . provid[es] the anchoring effect of the sealing resin." EX1004, [0032]; *see also* EX1004, [0009], [0019]. A POSITA would have recognized that a similar **Stopping Part 11** could be formed at the corners of the

**first terminal 70** and **second terminal 80** where the two **grooves** meet, with a reasonable expectation of success in achieving the same anchoring and adhesion benefits.



EX1004, Fig. 5.

107. In my opinion, a POSITA would have been able to readily implement the proposed modification, as both Hsu and Iwamasa describe LED packages containing one or more metallic lead frames encapsulated in **resin**, with the lead frames incorporating at least one **resin-holding component**. See Paragraphs 58-68 [Overview of Hsu and Iwamasa], 75-90 [Ground I, 1Pre-C, 6Pre-C] above. Additionally, both Hsu and Iwamasa disclose lead frames with substantially planar upper surfaces. See EX1003, Claim 6 (“An LED package comprising: a platelike **first terminal**”), Figs. 11, 12; EX1004, Fig. 1. A POSITA would have recognized

the possibility for a separation between such planar surfaces and the resin during encapsulation.

108. Given this, a POSITA would have been motivated to apply Iwamasa's teachings to improve adhesion between the upper sides of Hsu's lead frames and the encapsulating resin. Iwamasa specifically demonstrates that this improvement can be achieved by introducing grooves near the outer edges of a lead frame's upper surface. *See* EX1004, [0019] ("groove is filled with the sealing resin during the resin-sealing process. Therefore, after resin sealing, the long groove helps improve the bond strength and adhesion between the sealing resin and the base."). Implementing this design in Hsu's lead frames would have been a predictable and effective solution to enhance resin adhesion and structural integrity.

109. The proposed modification would simply involve incorporating a known design feature into Hsu's structure to achieve a predictable improvement in bond strength between its lead frames and the encapsulating resin. Hsu's lead frames already include a resin-holding component along multiple lateral sides. *See* EX1003, [0005], [0023], [0025], Fig. 11, Fig. 12. Iwamasa's grooves serve as an additional type of resin-holding component, but instead of being positioned on the lateral sides, they are located on the upper surface of the lead frame. A POSITA would have recognized that adding Iwamasa's grooves to Hsu's lead frames would

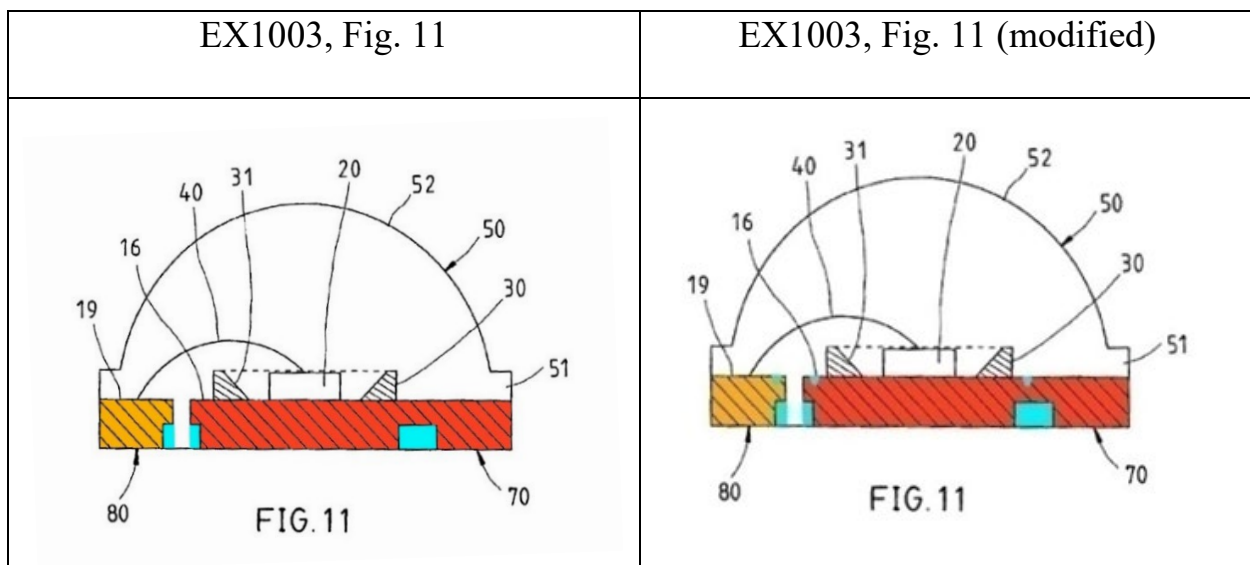
further enhance resin adhesion and increase bond strength in a predictable manner.

*See* EX1004, [0019], [0032], [0036].

vii. [6E] the **first** and the **second lead frames** comprise opposing sides facing each other, and the **resin-holding components** are disposed on the opposing sides.

110. Hsu alone or in combination with Iwamasa teaches [6E].

111. Particularly, as I have illustrated in Figure 11 below (on the left), Hsu discloses that the first and the second lead frames comprise opposing sides facing each other, and the grooves are disposed on the opposing sides. And as I am also showing on the right, Hsu as modified with Iwamasa discloses that the first and the second lead frames comprise opposing sides facing each other, and the grooves are disposed on the opposing sides.



EX1003, Fig. 11 (modified as Hsu+Iwamasa).

**4. Claims 2 and 3**

- i. [2] The LED package of claim 1, where the **resin-holding components** comprise at least one **hole**.
- ii. [3] The LED package of claim 2, wherein the **hole** is filled with the **resin** to increase the bonding force between the resin and the lead frames.

112. Hsu in combination with Iwamasa renders obvious claims [2] and [3].

113. As I already explained in Paragraphs 101-102, and as is shown in Figures 1(a) and 5, Iwamasa discloses a lead frame that includes **Through Hole 6**. For instance, Iwamasa describes that the “form shown in Figure 6 is a structure in which **Sealing Resin 25** is adhered to the entire interior surface of **Through Hole 6**, and **Through Hole [6]** is configured in **Sealing Resin 25** so as to pass through **Through Hole 6**.” EX1004, [0044].

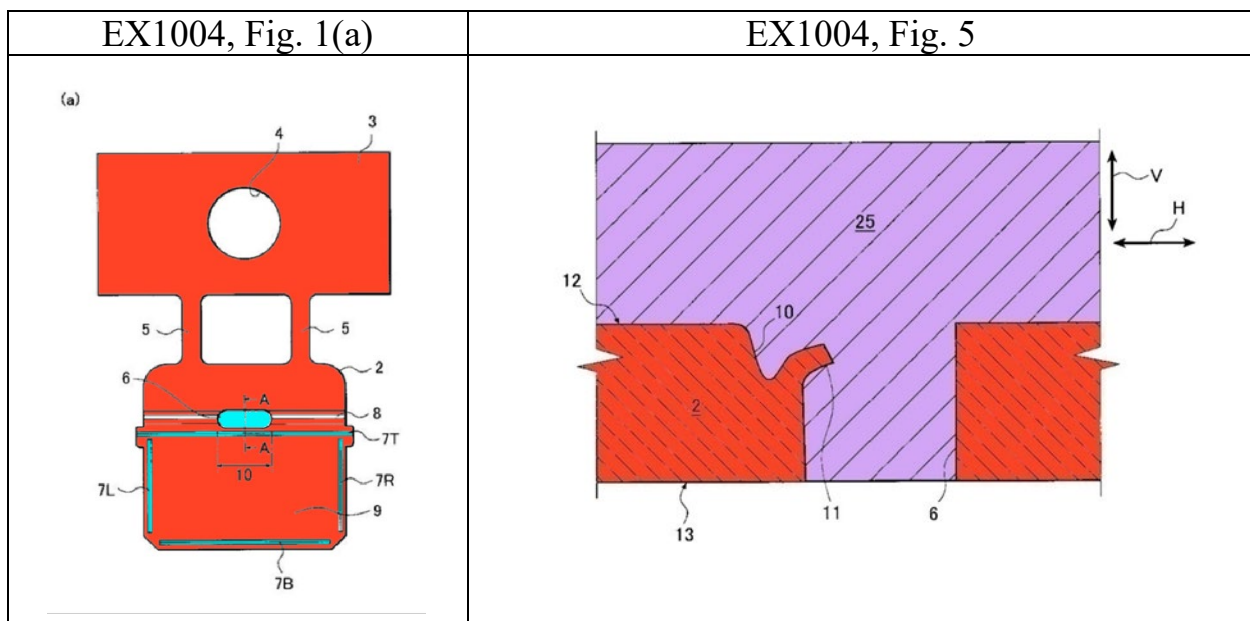
The form shown in Figure 6 is a structure in which Sealing Resin 25 is adhered to the entire interior surface of Through Hole 6, and Through Hole 26 is configured in Sealing Resin 25 so as to pass through Through Hole 6. According to this structure, the sealing resin in Through Hole 6 is unable to easily escape due to the presence of Stopping Part 11. Thus, the mechanical bond strength of Base 2 and Sealing Resin 25 with respect to the vertical direction V shown in the figure is improved.

In addition, the mechanical bond strength of Base 2 and Sealing Resin 25 with respect to the horizontal direction H shown in the figure is improved by fitting Sealing Resin 25 inside Through Hole 6.

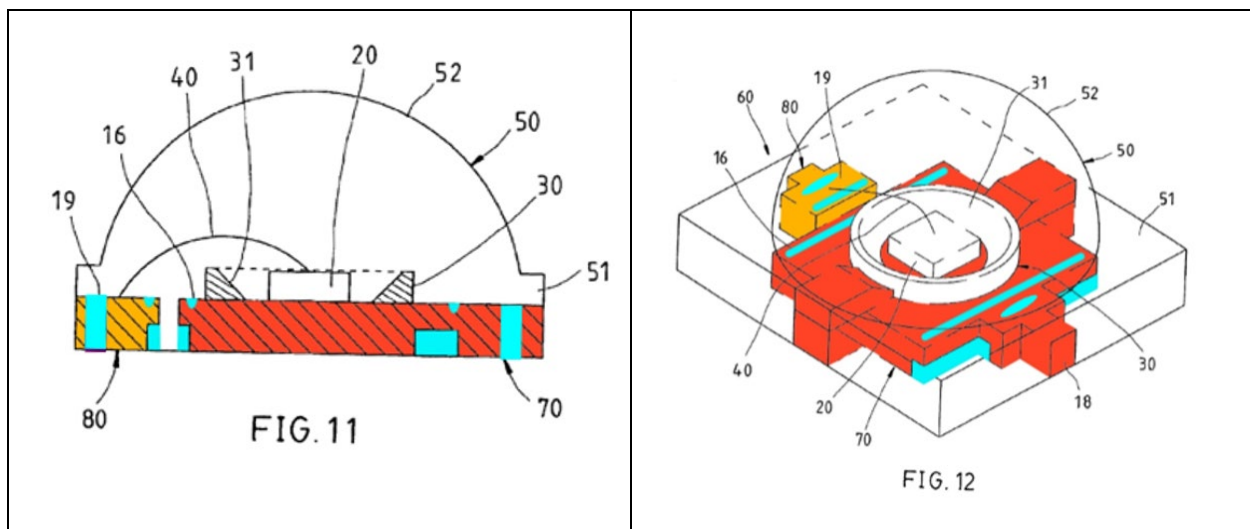
In addition to the mechanical bonding as described above, Sealing Resin 25 is also bonded to Base 2. If the adhesive area is increased by providing the number of Through Holes 6, this may improve the bond strength.

EX1004, [0044]

114. Additionally, Iwamasa teaches that “the **sealing resin** in **Through Hole 6** is unable to easily escape due to the presence of Stopping Part 11.” EX1004, [0044]. Iwamasa also teaches that “the mechanical bond strength of **Base 2** and **Sealing Resin 25** with respect to the vertical direction V shown in the figure is improved” and that “the mechanical bond strength of **Base 2** and **Sealing Resin 25** with respect to the horizontal direction H shown in the figure is improved by fitting **Sealing Resin 25** inside **Through Hole 6**.” EX1004, [0044]. This demonstrates that Iwamasa’s **lead frame** structure is specifically designed to be filled with **resin** in order to enhance the adhesion between the **lead frame** and the sealing **resin**.



115. A POSITA would have found it obvious to modify Hsu and incorporate Iwamasa's oval-shaped through-hole into Hsu's **first terminal 70** and/or **second terminal 80** as it would have merely been a straightforward design choice. Given that Iwamasa teaches that such through-holes enhance resin adhesion and mechanical bond strength, applying this feature to Hsu's structure would have been an obvious improvement. A POSITA would have had a reasonable expectation of success in implementing this modification, as reflected in the modified Figures 11 and 12 below.



EX1003, Figs. 11 and 12 (modified as Hsu+Iwamasa).

116. Both Hsu and Iwamasa disclose LED packages that incorporate one or more metallic lead frames encapsulated in resin, with the lead frames featuring at least one resin-holding component. *See* Paragraphs 58-68 [Overview of Hsu and Iwamasa], and Paragraphs 75-90, [Ground I, 1Pre-C, 6Pre-C] above. Additionally,

both references describe lead frames with substantially planar surfaces on their top sides. *See* EX1003, Claim 6 (“An LED package comprising: a platelike **first terminal**”), Figs. 11, 12; EX1004, Fig. 1. A POSITA would have recognized that such planar surfaces and the **resin** may separate.

117. Given this, a POSITA would have been motivated to apply Iwamasa’s approach to improving adhesion between Hsu’s lead frames and the surrounding resin. Iwamasa specifically teaches that adding a **through-hole** to a lead frame enhances bond strength by allowing **resin** to pass through and mechanically anchor the encapsulant to the frame. *See* EX1004, [0044], Figs. 1, 5, 6. Incorporating this feature into Hsu’s lead frames would have been an obvious modification to improve adhesion and structural stability.

The form shown in Figure 6 is a structure in which Sealing Resin 25 is adhered to the entire interior surface of Through Hole 6, and Through Hole 26 is configured in Sealing Resin 25 so as to pass through Through Hole 6. According to this structure, the sealing resin in Through Hole 6 is unable to easily escape due to the presence of Stopping Part 11. Thus, the mechanical bond strength of Base 2 and Sealing Resin 25 with respect to the vertical direction V shown in the figure is improved.

In addition, the mechanical bond strength of Base 2 and Sealing Resin 25 with respect to the horizontal direction H shown in the figure is improved by fitting Sealing Resin 25 inside Through Hole 6.

In addition to the mechanical bonding as described above, Sealing Resin 25 is also bonded to Base 2. If the adhesive area is increased by providing the number of Through Holes 6, this may improve the bond strength.

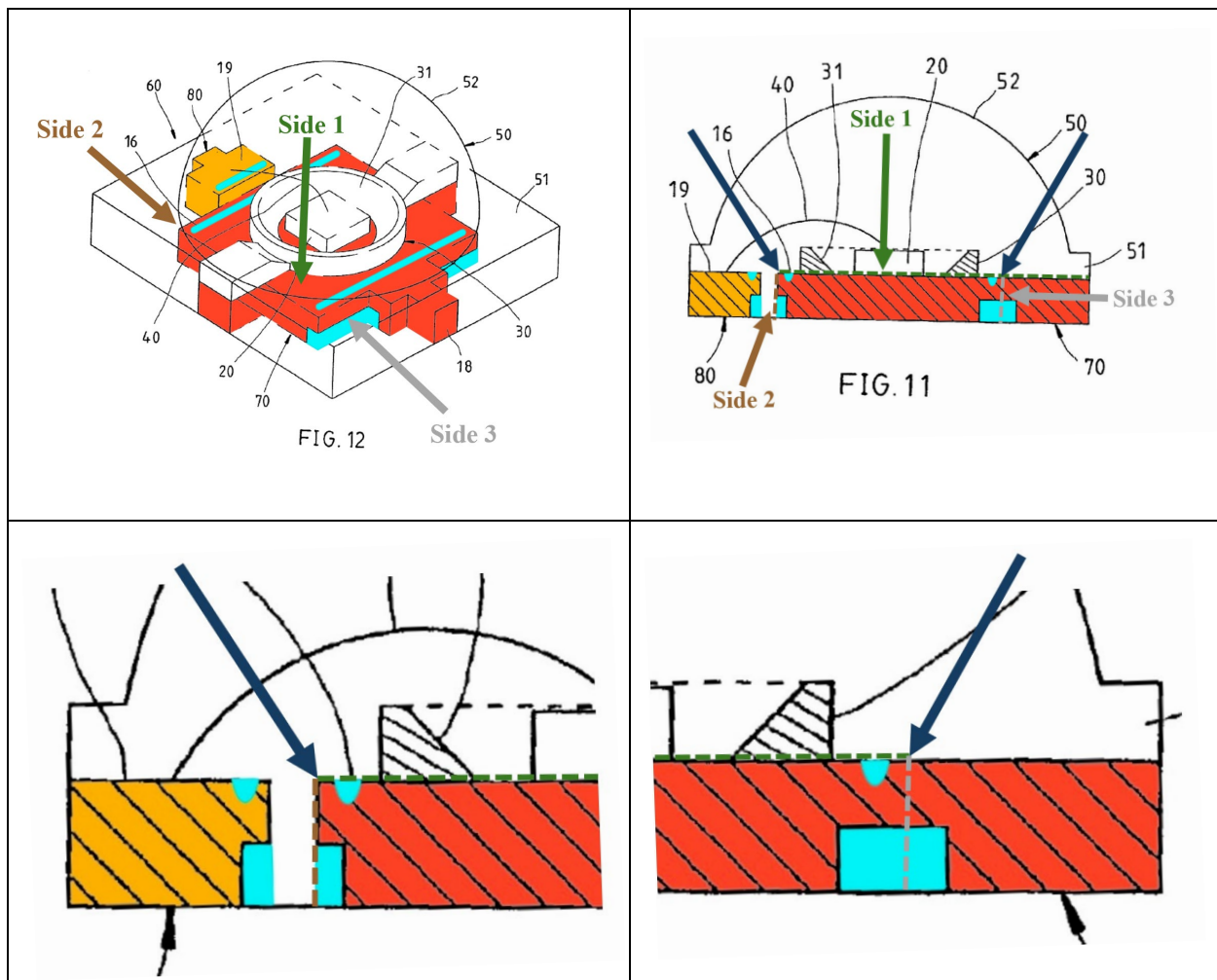
EX1004, [0044].

118. Furthermore, the proposed modification would simply involve incorporating a known design feature into Hsu to achieve a predictable improvement in bond strength between the **lead frame** and the encapsulating **resin**. Hsu's **lead frames** already include a **resin-holding component** along multiple lateral sides. *See* Paragraphs 88-109 [Ground I, Claims 1 and 6, limitations C–D] above. Iwamasa's **through-hole** serves as an additional type of **resin-holding component** designed to be filled with **resin**, enhancing adhesion by allowing the resin to anchor more effectively to the lead frame. A POSITA would have recognized that adding Iwamasa's **through-hole** to Hsu's **lead frames** would further strengthen the bond between the resin and the lead frame in a predictable manner. *See* EX1004, [0044], Figs. 1, 5, 6. At a minimum, it would have been obvious for a POSITA to try the addition of a **hole** along the upper side of Hsu's **first terminal 70** and **second terminal 80** alongside the **grooves** disposed thereon, as taught by Iwamasa's **Through Hole 6** disposed alongside its **Long Groove 10** of its **Base 2**. In particular, Iwamasa describes the need to improve bond strength between **lead frames** and overlying **resin**, and that such improvement could be achieved by adding **grooves** and **Through Hole 6** to the sides of **lead frames**.

5. Claim 4

- i. [4] The LED package of claim 1, wherein the **resin-holding components** are disposed on three sides of at least one of the **first** and **second lead frames**.

119. The Hsu-Iwamasa combination teaches claim [4]. In particular, as I am illustrating in Figures 11 and 12 of Hsu (which have been modified by Iwamasa), there are **grooves** on three sides of the **first terminal 70**.



EX1003, Figs. 11 and 12 (modified as Hsu+Iwamasa).

**B. Ground II: Hsu In Combination With Iwamasa and Hui Renders Obvious Claims 1-4, And 6.**

**1. Overview of Hui (EX1005)**

120. Hui describes surface mount devices designed for mounting electronic components, including light-emitting diodes (LEDs). EX1005, [0018]. Hui further provides detailed illustrations of its structure. For instance, in Figure 3, Hui shows an “enlarged perspective view of the **first** and **second electrode 110, 115** without the casing 105 where the **first** and **second electrodes** are separated by an insulation gap 370.” EX1005, [0022].

FIG. 3 depicts an enlarged perspective view of the first and second electrode 110, 115 without the casing 105 where the first and second electrodes are separated by an insulation gap 370. In some embodiments, the first electrode 110 includes the chip carrier part 120 that can further include protrusions or extensions portions 335, 340, first and second lead portions 320, 325 separated by an aperture 345, and a joined lead portion 330 that, in some implementations, is further bent at the first bend 305 and the second bend 310. The second electrode 115 can include first and second lead portions 322, 327 and joined lead portion 332 that, again in some implementations, is bent at the first and second bends 307, 312. The first and second lead portions 322, 327 can include head ends 337 and 342, respectively that are positioned juxtaposed to the chip carrier part 120. The second electrode 115 can further include first and second extended portions 322, 327 extending from the first and second head ends 337, 342, respectively.

EX1005, [0022].

121. In Figure 4, Hui provides a “partially transparent overhead view of the surface mount device 100,” offering insight into its overall configuration. EX1005, [0035].

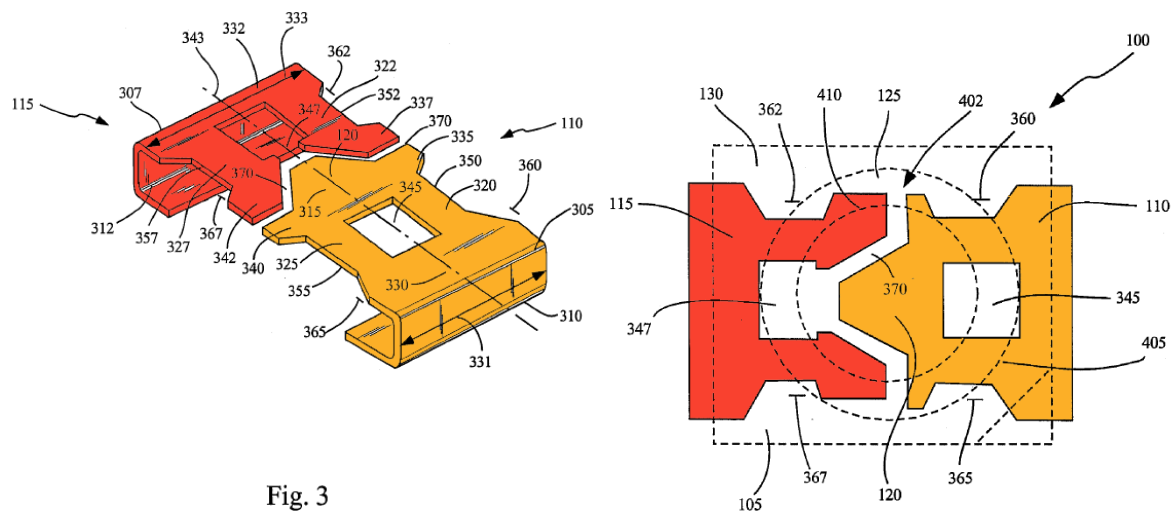
FIG. 4 depicts a partially transparent overhead view of the surface mount device 100, transparently illustrating the casing 105 so that the first and second electrodes 110, 115 are visible through the casing 105, according to some embodiments. The recess 125 in some implementations is generally conical in shape and includes a wall 402 that tapers from an outer perimeter of the recess at the second surface 130 of the casing 105 to an interior perimeter of the recess 410 at about the first and second electrodes 110, 115. As such, at least a portion of the first and second electrodes 110, 115 are exposed through the recess 125. Further, portions of the casing surrounding the exposed portions of the electrodes and within the interior perimeter 410 of the recess 125 are also exposed through the recess 126. The embodiment of FIG. 4 depicts portions of the first and second electrode 110, 115, portions of the insulation gap 370, a first portion of the aperture 345, and a first portion of the inlet 347 extending into and being exposed through the recess 125.

EX1005, [0035].

122. Hui also describes how the LED is typically mounted on and supported by the **first electrode 110** at the chip carrier part 120. Additionally, in some implementations, a fill material is used to partially or fully fill the recess 125 in the casing 105, surrounding or covering the LED, the exposed portions of the **first** and **second electrodes 110, 115**, and the electrical connections between the LED and the electrodes. EX1005, [0037].

An electronic element (e.g., optoelectronic element) is typically coupled with and/or supported by the first electrode 110 at the chip carrier part 120. The electronic element is further coupled with the second electrode 115 through a connection (e.g., a bond wire or other such connection). Further, the electronic element typically is at least partially exposed through the recess 125. ***Some implementations include the fill material that fills at least some of the recess 125 in the casing 105, and typically surrounds and/or covers the electronic element, the exposed portions of the first and second electrodes 110, 115, and the electrical connection(s) between the electronic element and the electrodes.*** The fill material may also, at least partially, cover and/or fill portions of the insulation gap 370, the aperture 345, and inlet 347 that extend into and are exposed through the recess 125.

EX1005, [0037].



EX1005, Figs. 3, 4.

**2. Claims 1 And 6**

- i. [1Pre, 6Pre] **A light emitting diode (LED) package, comprising**

123. Hsu teaches preambles [1Pre] and [6Pre] for at least the reasons I already explained in Paragraphs 75-77.

- ii. [1A, 6A] **a first lead frame and a second lead frame separated from each other;**

124. Hsu teaches [1A] and [6A] for at least the reasons I already explained in Paragraphs 78-83.

- iii. [1B, 6B] **an LED chip disposed on the first lead frame and electrically connected with second lead frame; and**

125. Hsu teaches [1B] and [6B] for at least the reasons I already explained in Paragraphs 84-87.

- iv. [1C, 6C] **a resin covering at least portions of surfaces of the first and second lead frames, wherein:**

126. Hsu teaches [1C] and [6C] for at least the reasons I already explained in Paragraphs 88-90.

- v. [1D, 6D] at least one of the **first** and **second lead frames** comprises **resin-holding components** disposed along adjacent sides of one of the **first** and **second lead frames**, the **resin-holding components** being separated from each other at corners of the adjacent sides; and:
- vi. [1E] the **resin-holding components** are disposed on two adjacent sides of each of the **first lead frame** and the **second lead frame**.

127. Hsu teaches [1D], [1E] and [6D] for at least the reasons I already explained in Paragraphs 91-109.

128. While silent in the claims, the '913 Patent states that “**slant parts 125, 145** disperse the force diagonally, thereby preventing the **encapsulation material 20** from being broken on the opposite sides of the **lead frames 12, 14**.” EX1001, 6:34–37. To the extent the “**resin-holding components**” require such slanted sides, Hsu in combination with Iwamasa and Hui teach [1D], [1E] and [6D].

129. In particular, such lead frames having slanted parts were well-known in the art, as shown by Hui. And it would have been obvious to a POSITA to use Hui’s “**first** and **second electrodes 110, 115**” that include such slanted sides. EX1005, [0035].

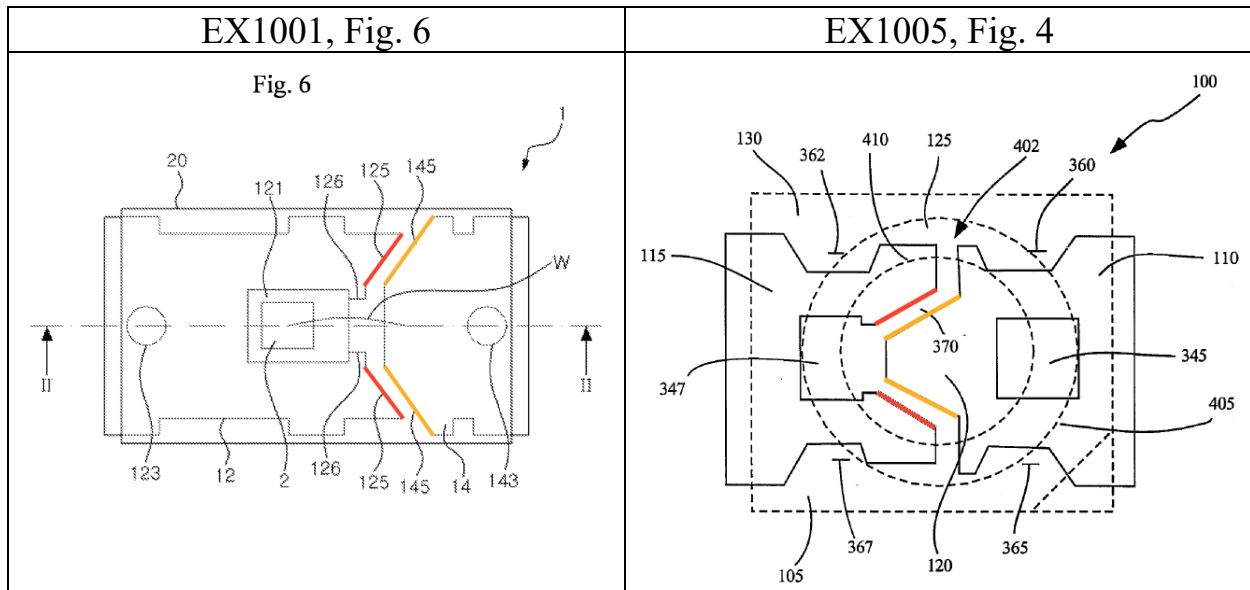


**FIG. 4 depicts a partially transparent overhead view of the surface mount device 100, transparently illustrating the casing 105 so that the first and second electrodes 110, 115 are visible through the casing 105, according to some embodiments.** The recess 125 in some implementations is generally conical in shape and includes a wall 402 that tapers from an outer perimeter of the recess at the second surface 130 of the casing 105 to an interior perimeter of the recess 410 at about the first and second electrodes 110, 115. As such, at least a portion of the first and second electrodes 110, 115 are exposed through the recess 125. Further, portions of the casing surrounding the exposed portions of the electrodes and within the interior perimeter 410 of the recess 125 are also exposed through the recess 126. The embodiment of FIG. 4 depicts portions of the first and second electrode 110, 115, portions of the insulation gap 370, a first portion of the aperture 345, and a first portion of the inlet 347 extending into and being exposed through the recess 125.

EX1005, [0035].

130. A POSITA would have recognized that further modifying the combination of Hsu and Iwamasa by incorporating Hui's teachings would have been

an obvious design choice. Specifically, replacing Hsu's **first terminal 70** and **second terminal 80** with Hui's **first** and **second electrodes 110, 115** that have slanted sides would have been a straightforward substitution. This modification involves nothing more than replacing one known component (Hsu's **first** and **second terminal**) with another known component (Hui's **first** and **second electrodes** with slanted sides) while achieving the predictable result of forming an LED package. A POSITA would have had a reasonable expectation of success in making this substitution, as it maintains the overall function of the lead frames.

131. It would have at minimum been obvious to explore different lead frame configurations, including those with varying shapes, such as the slanted-sided **first** and **second electrodes (110, 115)** taught by Hui. A POSITA would have been motivated to make this substitution because Hui explicitly teaches that “[t]he enhanced bonding provided through and around the **first** and **second electrodes 110, 115**, at least in part, enhance the stability of the **first** and **second electrodes 110, 115** relative to the casing 105 and the structural integrity of the surface mount device 100.” EX1005, [0047]. Hui further explains that “the structural integrity is further maintained, at least in part, through the electrodes 110, 115 adhering to the casing 105, the fill material, and/or the optoelectronic component.” EX1005, [0047]. Given these benefits, a POSITA would have understood that substituting Hsu's **first**

**terminal 70** and **second terminal 80** with Hui's **first** and **second electrodes (110, 115)** could improve structural stability and adhesion, making it an obvious design choice.

The enhanced bonding provided through and around the first and second electrodes 110, 115, at least in part, enhances the stability of the first and second electrode 110, 115 relative to the casing 105 and the structural integrity of the surface mount device 100. The structural integrity is further maintained, at least in part, through the electrodes 110, 115 adhering to the casing 105, the fill material, and/or the optoelectronic element. In some embodiments, however, the bonding or adhesion between casing material, and/or between casing material and fill material is greater than the bonding or adhesion established between the casing and the electrodes, and between the electrodes and the fill material.

EX1005, [0047].

- vii. [6E] the **first** and the **second lead frames** comprise opposing sides facing each other, and the **resin-holding components** are disposed on the opposing sides.

132. Hsu alone or in combination with Iwamasa and Hui teaches [6E] for at least the reasons I already explained in Paragraphs 110-111.

**3. Claims 2 and 3**

- i. [2] The LED package of claim 1, where the **resin-holding components** comprise at least one **hole**.
- ii. [3] The LED package of claim 2, wherein the **hole** is filled with the **resin** to increase the bonding force between the resin and the lead frames.

133. Hsu in combination with Iwamasa teaches claims [2] and [3] for at least the reasons I already discussed in Paragraphs 112-118.

**4. Claim 4**

- i. [4] The LED package of claim 1, wherein the **resin-holding components** are disposed on three sides of at least one of the **first** and **second lead frames**.

134. Hsu in combination with Iwamasa teaches claim [4] for at least the reasons I already discussed in Paragraph 119.

**C. Ground III: Oshio Anticipates Claims 1-4, And 6.**

**1. Overview of Oshio (EX1006)**

135. Oshio describes a semiconductor light-emitting device that incorporates a pair of leads (20 and 30) as part of its structural design. EX1006, [0030].

FIG. 1 is a schematic cross-sectional view illustrating the configuration of the relevant part of a semiconductor light emitting device according to an embodiment of the invention.

EX1006, [0030].

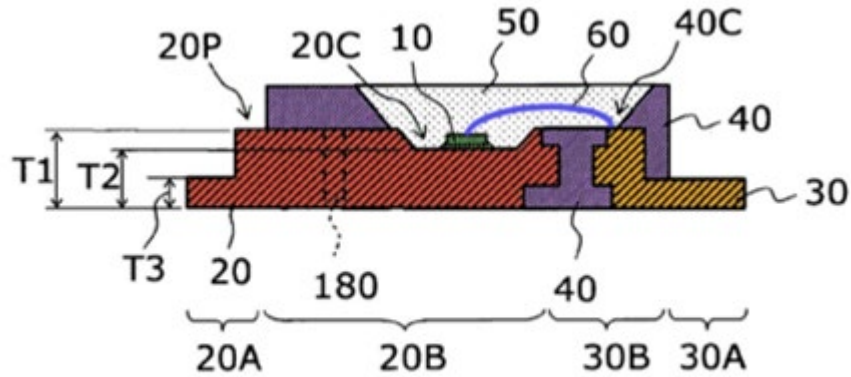


FIG. 1

EX1006, Fig. 1.

136. In Figures 1, 5A, 5B, and 12, Oshio shows that “the semiconductor light emitting device . . . comprises a pair of **leads 20** and **30**” and notes that it “is desirable that the **leads 20** and **30** be supplied in the form of the so-called ‘lead frame’.” EX1006, [0049], [0084]. This indicates that the leads are designed to function as part of a conventional lead frame structure commonly used in LED packages.

137. Oshio further details how the LED chip is integrated into this structure, explaining that an “**LED chip 10** is die bonded to the bottom face of the recess 20C of the **lead 20.**” EX1006, [0061].

The inner lead section 20B of the lead 20 has a cup-shaped recess 20C. On the other hand, the embedding resin 40 has a recess 40C, at the bottom of which are exposed in part the inner lead sections 20B and 30B including the recess 20C of the lead. The LED chip 10 is die bonded to the bottom face of the recess 20C of the lead 20. Eutectic solder, conductive paste, or gold (Au) bump can be

used as an adhesive for die bonding. The electrode of the LED chip 10 is connected to the other inner lead section 30B via bonding wire 60.

EX1006, [0061].

138. To complete the electrical connection, “electrode of the LED chip 10 is connected to the other inner lead section 30B via bonding wire 60.” EX1006, [0061]. Additionally, to secure and insulate the internal components, Oshio discloses that an “embedding resin 40 [is] formed to encompass inner lead sections 20B and 30B of the leads 20 and 30.” EX1006, [0049].

More specifically, the semiconductor light emitting device of this embodiment, which is a light emitting device of the so-called surface mount device (SMD) type, comprises a pair of leads 20 and 30, and embedding resin 40 formed to encompass inner lead sections 20B and 30B of the leads 20 and 30. A semiconductor light emitting chip 10 (hereinafter referred to as “LED chip”) is mounted on the lead 20. This semiconductor light emitting device can be mounted, for example, on an electrode pattern of various mounting substrates by soldering or welding outer lead sections 20A and 30A.

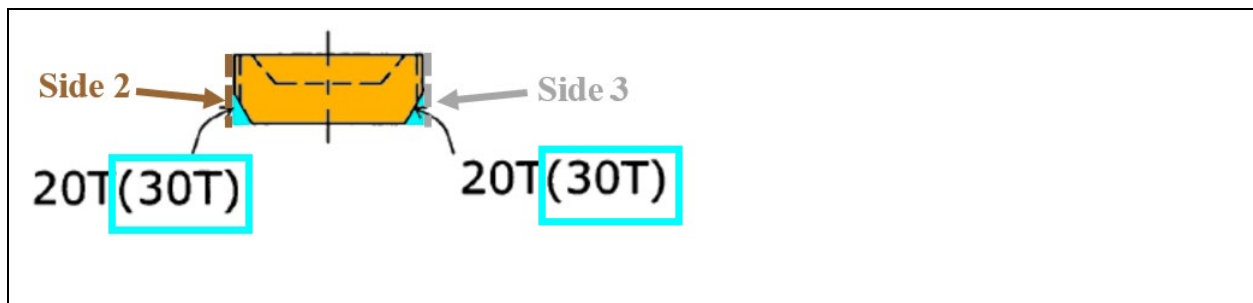
EX1006, [0049].

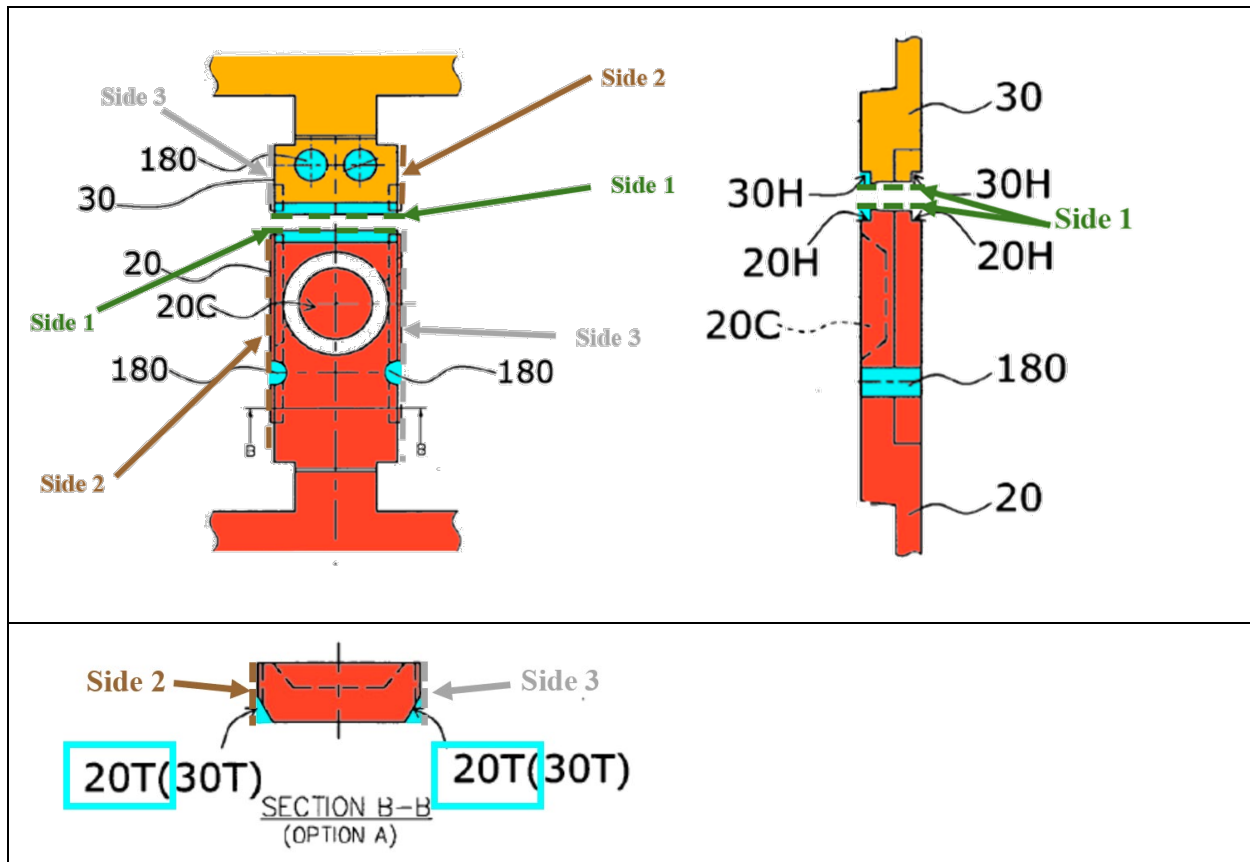
139. Furthermore, as illustrated in Figure 12, Oshio discloses that lead 20 and lead 30 incorporate multiple “structure[s] for enhancing bonding strength between leads 20, 30 and resin 40.” EX1006, [0034].

FIGS. 5A and 5B are schematic views illustrating the structure for enhancing bonding strength between leads 20, 30 and resin 40.

EX1006, [0034].

140. These structures are specifically designed to improve adhesion between the leads and the encapsulating resin, reducing the likelihood of detachment over time. Oshio further emphasizes the importance of such features, explaining that “it is therefore desirable to use a structure having increased bonding strength to avoid peeloff of these leads from the embedding resin 40.” EX1006, [0076]; *see also* EX1006, [0077].





EX1006, Fig. 12.

141. Oshio discloses multiple structural features designed to enhance the bond between the leads and the encapsulating resin. For example, Oshio teaches that “**asperities 20H and 30H** . . . provided at the tip of the inner lead sections of the **lead 20 and 30**,” respectively, improve “biting” into the **resin 40**, thereby increasing bonding strength. EX1006, [0079].

Moreover, asperities 20H and 30H can be provided at the tip of the inner lead sections of the lead 20 and 30 to improve “biting” to the resin 40, so that the bonding strength can be enhanced.

EX1006, [0079].

142. Additionally, Oshio describes a tapered design, explaining that “as shown as line A-A’ cross section in FIG. 5B,” a “**tapered portion 20T (30T)** with its width decreasing toward the rear face may be provided on the sidewall of the **lead 20 (30)**.” EX1006, [0080]. This tapered structure “facilitates supporting the **lead 20 (30)** with the **tapered portion 20T (30T)** obliquely from below, thereby preventing peeloff of the **resin 40**.” EX1006, [0080].

Furthermore, as shown as line A-A’ cross section in FIG. 5B, a tapered portion 20T (30T) with its width decreasing toward the rear face may be provided on the sidewall of the lead 20 (30). This facilitates supporting the lead 20 (30) with the tapered portion 20T (30T) obliquely from below, thereby preventing peeloff of the resin 40.

EX1006, [0080].

143. In addition to asperities and tapered portions, Oshio teaches the use of anchor holes to improve adhesion. Specifically, Oshio states that “**anchor holes 180** are provided through the **lead 20 (30)** so that the embedding **resin 40** may fill in these **anchor holes 180**,” explaining that this feature “serves to reduce ‘loosening’ between the leads and the injection molded object and to increase adhesion strength and contact area, so that peeloff of the leads from the **resin 40** can be prevented.” EX1006, [0078].

More specifically, anchor holes 180 are provided through the lead 20 (30) so that the embedding resin 40 may fill in these anchor holes 180. This serves to reduce “loosening” between the leads and the injection molded object and to increase adhesion

strength and contact area, so that peeloff of the leads from the resin 40 can be prevented.

EX1006, [0078].

144. Oshio further reinforces the importance of these design elements, stating that “the anchor holes 180, asperities 20H (30H), and tapered portion 20T (30T) described above . . . serve to reduce ‘loosening’ between the leads and the injection molded object and to increase adhesion strength and contact area, so that peeloff of the leads from the resin 40 can be prevented.” EX1006, [0081]; *see also* EX1006, [0051], [0087].

## **2. Claims 1 And 6**

### **i. [1Pre, 6Pre] A light emitting diode (LED) package, comprising**

145. I understand that the preamble may not limit the claims. Regardless, Oshio teaches preambles [1Pre] and [6Pre].

146. Figure 1 of Oshio shows “a semiconductor light emitting device.” EX1006, [0030].

FIG. 1 is a schematic cross-sectional view illustrating the configuration of the relevant part of a semiconductor light emitting device according to an embodiment of the invention.

EX1006, [0030].

147. The device is an LED package because it features “a package structure in which a light emitting diode chip, that is, an LED chip, is received.” EX1001, 1:31–32.

An LED package means a package structure in which a light emitting diode chip, that is, an LED chip, is received.

EX1001, 1:31–32.

148. As shown, “LED chip 10 is die bonded to the bottom face of the recess 20C of the lead 20.” EX1006, [0061]. Additionally, “[t]he electrode of the LED chip 10 is connected to the other inner lead section 30B via bonding wire 60.” EX1006, [0061].

The inner lead section 20B of the lead 20 has a cup-shaped recess 20C. On the other hand, the embedding resin 40 has a recess 40C, at the bottom of which are exposed in part the inner lead sections 20B and 30B including the recess 20C of the lead. ***The LED chip 10 is die bonded to the bottom face of the recess 20C of the lead 20.*** Eutectic solder, conductive paste, or gold (Au) bump can be used as an adhesive for die bonding. ***The electrode of the LED chip 10 is connected to the other inner lead section 30B via bonding wire 60.***

EX1006, [0061].

149. This configuration establishes electrical connectivity within the package. *See also* EX1006, Abstract (A “semiconductor light emitting chip mounted on a portion of the first inner section exposed in a recess provided on an upper face



ii. [1A, 6A] a **first lead frame** and a **second lead frame** separated from each other;

151. As illustrated in Figures 1 and 12, Oshio shows a semiconductor light-

*More specifically, the semiconductor light emitting device of this embodiment, which is a light emitting device of the so-called surface mount device (SMD) type, comprises a pair of leads 20 and 30, and embedding resin 40 formed to encompass inner lead sections 20B and 30B of the leads 20 and 30. A semiconductor light emitting chip 10 (hereinafter referred to as “LED chip”) is mounted on the lead 20. This semiconductor light emitting device can be mounted, for example, on an electrode pattern of various mounting substrates by soldering or welding outer lead sections 20A and 30A.*

EX1006, [0049].

152. Oshio further states that it “is desirable that the **leads 20** and **30** be supplied in the form of the so-called ‘lead frame’.” EX1006, [0084]. *See also* EX1006, Abstract (describing a semiconductor light-emitting device with “embedding resin; a **first lead**” and “a **second lead**.”), [0010–13], [0018–23], [0036–39], [0069], [0085–86], Claim 1, Claim 14. And Oshio also teaches that the **first lead** and the **second lead** are separated from each other, as I have shown with **dark pink brackets** below in Figures 1 and 12 of Oshio.

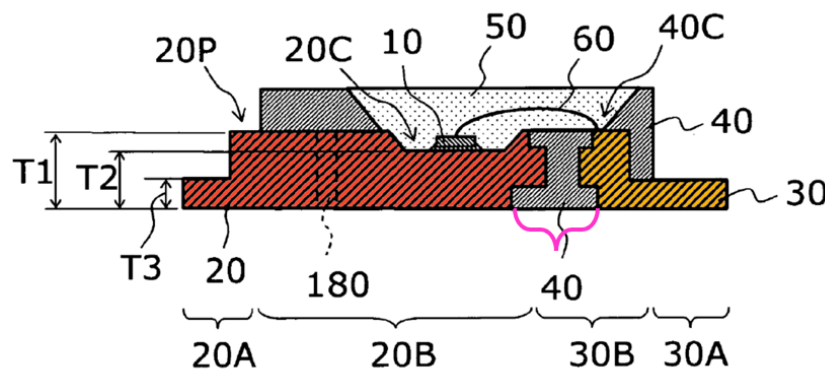


FIG. 1

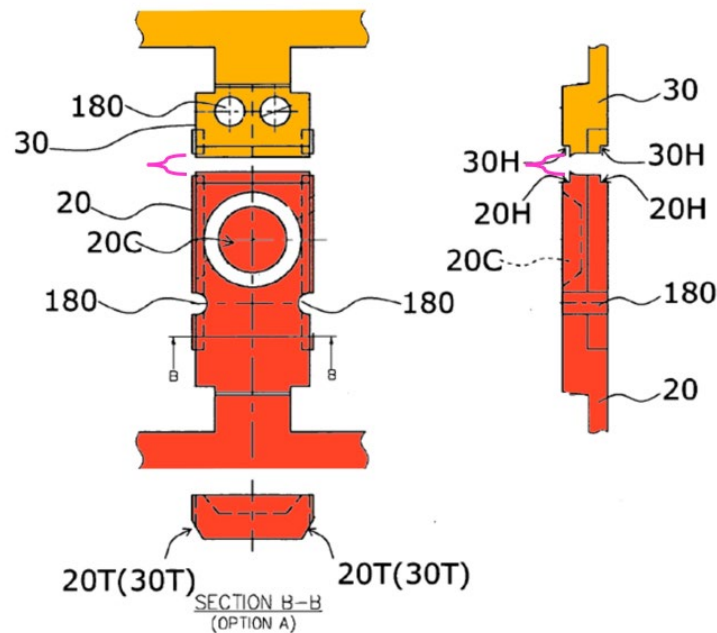


FIG. 12

EX1006, Figs. 1, 12.

- iii. [1B, 6B] an LED chip disposed on the first lead frame and electrically connected with second lead frame; and

153. Oshio teaches [1B] and [6B].

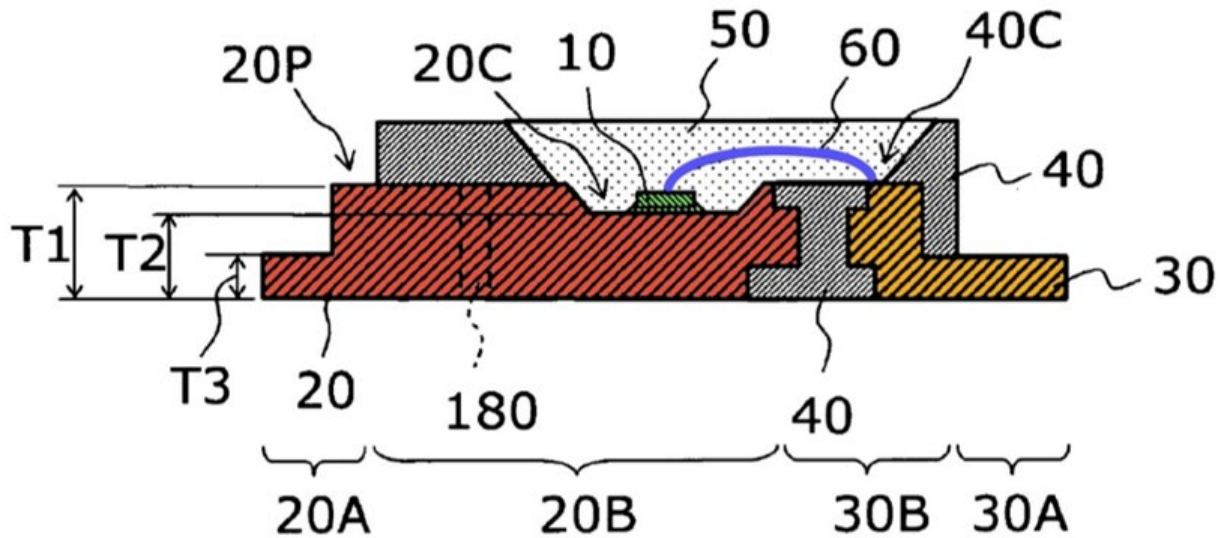
154. As depicted in Figure 1, Oshio discloses an “LED chip 10 [that] is die bonded to the bottom face of the recess 20C of the lead 20.” EX1006, [0061]. Oshio also discloses that the “electrode of the LED chip 10 is connected to the other inner lead section 30B via bonding wire 60.” EX1006, [0061]. I have illustrated this wire in Figure 1 below in blue. As can be seen from Figure 1, this wire connects the

**semiconductor light emitting chip** to the **second lead**, and establishes electrical connectivity between the **LED chip** and the **second lead**.

The inner lead section 20B of the lead 20 has a cup-shaped recess 20C. On the other hand, the embedding resin 40 has a recess 40C, at the bottom of which are exposed in part the inner lead sections 20B and 30B including the recess 20C of the lead. The LED chip 10 is die bonded to the bottom face of the recess 20C of the lead 20. Eutectic solder, conductive paste, or gold (Au) bump can be used as an adhesive for die bonding. The electrode of the LED chip 10 is connected to the other inner lead section 30B via bonding wire 60.

EX1006, [0061].

155. There are other parts of Oshio that also provide a disclosure of an electrical connection between the **LED chip** and the **second lead**. See EX1006, Abstract (describing a “semiconductor light emitting chip [that is] mounted on a portion of the first inner lead section exposed in a recess provided on an upper face of the embedding resin; and a wire connect[s] the semiconductor light emitting chip with the second lead.”), [0010–15], [0018–25], [0049], [0053], [0065–68], [0070], [0084], [0089], [0098], [0110], Claim 1, Claim 9, Claim 13, Claim 14.



EX1006, Fig. 1.

iv. [1C, 6C] a resin covering at least portions of surfaces of the first and second lead frames, wherein:

156. Oshio teaches [1C] and [6C].

157. As illustrated in Figures 1 and 2, Oshio discloses an “embedding resin 40 formed to encompass inner lead sections 20B and 30B of the leads 20 and 30.” EX1006, [0049].

More specifically, the semiconductor light emitting device of this embodiment, which is a light emitting device of the so-called surface mount device (SMD) type, comprises a pair of leads 20 and 30, and embedding resin 40 formed to encompass inner lead sections 20B and 30B of the leads 20 and 30. A semiconductor light emitting chip 10 (hereinafter referred to as “LED chip”) is

mounted on the lead 20. This semiconductor light emitting device can be mounted, for example, on an electrode pattern of various mounting substrates by soldering or welding outer lead sections 20A and 30A.

EX1006, [0049].

158. This embedding resin encapsulates portions of the lead structure, securing and insulating the inner lead sections. *See also* EX1006, [0010–13] (describing a semiconductor light-emitting device that includes “**embedding resin**; a **first lead** having a **first inner lead section** embedded in the **embedding resin**” and “a **second lead** having a **second inner lead section** embedded in the **embedding resin**.”), Abstract, [0018–23], [0038], [0061], [0071–75], [0089], [0092], [0095], Claim 1, Claim 14.

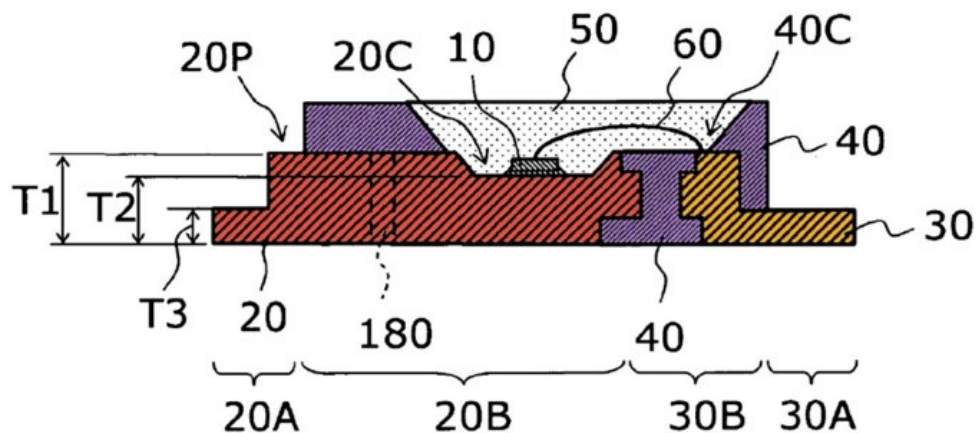


FIG. 1

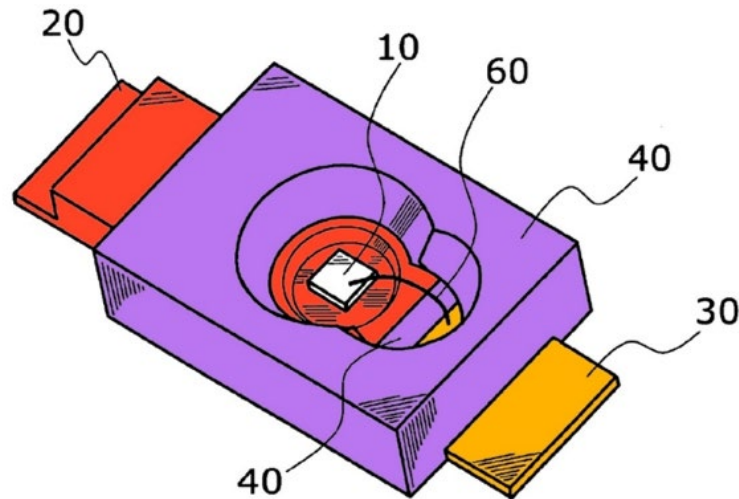


FIG. 2

EX1006, Figs. 1, 2.

- v. [1D, 6D] at least one of the **first** and **second lead frames** comprises **resin-holding components** disposed along adjacent sides of one of the **first** and **second lead frames**, the **resin-holding components** being separated from each other at corners of the adjacent sides; and:
- vi. [1E] the **resin-holding components** are disposed on two adjacent sides of each of the **first lead frame** and the **second lead frame**.

159. Oshio teaches [1D], [1E], and [6D].

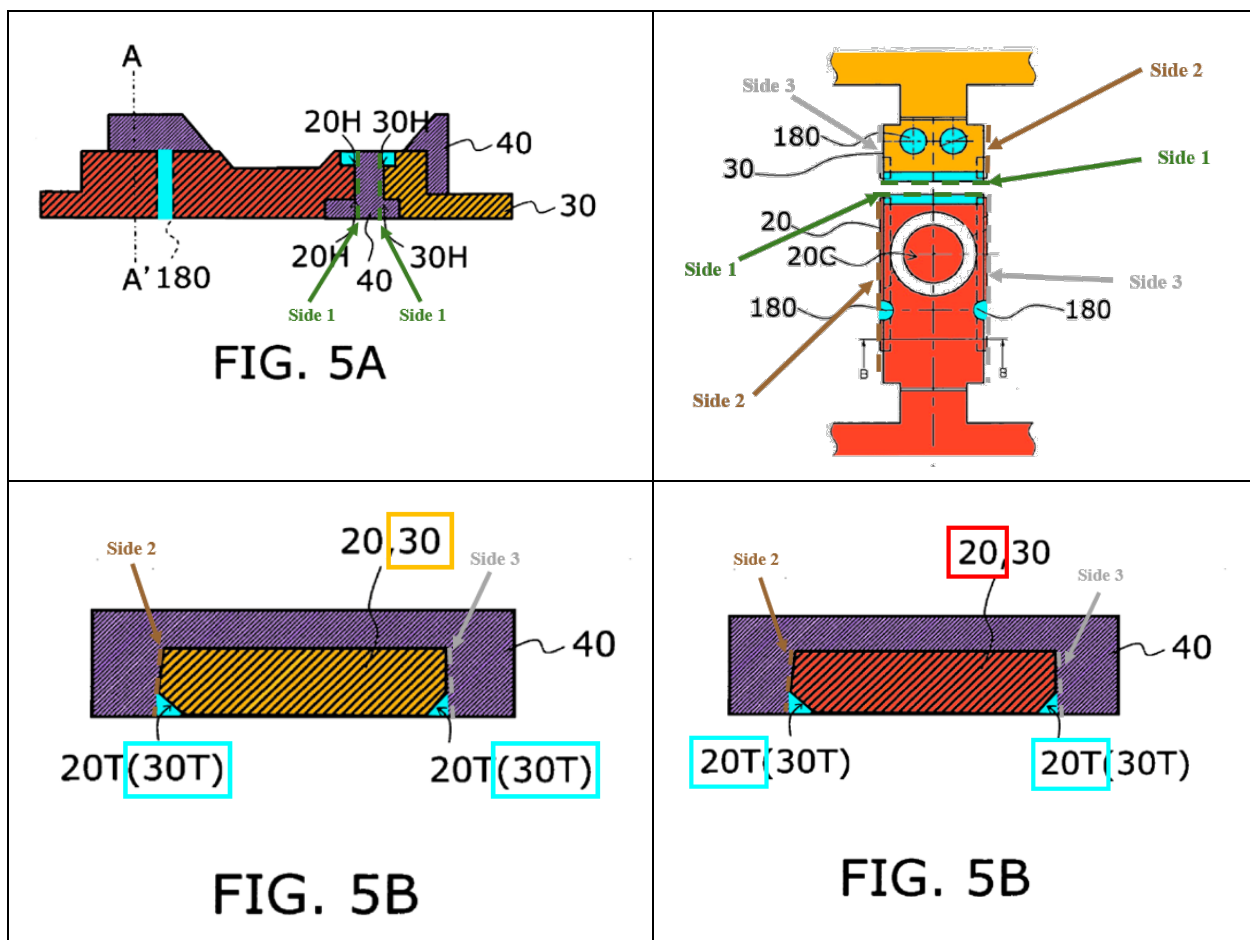
160. As illustrated in Figures 5A, 5B, and 12, Oshio discloses that its **lead 20** and **lead 30** incorporate multiple **resin-holding components**, described as “structure[s] for enhancing bonding strength between **leads 20, 30** and **resin 40**.”

EX1006, [0034].

FIGS. 5A and 5B are schematic views illustrating the structure for enhancing bonding strength between leads 20, 30 and resin 40.

EX1006, [0034].

161. These structures are specifically designed to improve adhesion and prevent separation of the leads from the encapsulating resin. *See* EX1006, [0076] (“It is therefore desirable to use a structure having increased bonding strength to avoid peeloff of these leads from the embedding resin 40.”), [0077].



EX1006, Figs. 5A, 5B, 12.

162. Oshio discloses multiple **resin-holding structures** designed to improve adhesion between the lead frame and the embedding resin. For example, Oshio teaches that “**asperities 20H** and **30H** . . . provided at the tip of the inner lead sections of the **lead 20** and **30**,” respectively, function “to improve ‘biting’ to the **resin 40**, so that the bonding strength can be enhanced.” EX1006, [0079].

Moreover, asperities 20H and 30H can be provided at the tip of the inner lead sections of the lead 20 and 30 to improve “biting” to the resin 40, so that the bonding strength can be enhanced.

EX1006, [0079]

163. Additionally, Oshio describes a **tapered structure**, explaining that “as shown as line A-A’ cross section in FIG. 5B,” “a **tapered portion 20T** [on the **first lead**] (**30T** [on the **second lead**]) with its width decreasing toward the rear face may be provided on the sidewall of the **lead 20** (**30**). This facilitates supporting the **lead 20** (**30**) with the **tapered portion 20T** (**30T**) obliquely from below, thereby preventing peeloff of the **resin 40**.” EX1006, [0080].

Furthermore, as shown as line A-A’ cross section in FIG. 5B, a tapered portion 20T (30T) with its width decreasing toward the rear face may be provided on the sidewall of the lead 20 (30). This facilitates supporting the lead 20 (30) with the tapered portion 20T (30T) obliquely from below, thereby preventing peeloff of the resin 40.

EX1006, [0080].

164. Oshio additionally discloses the use of **anchor holes** to strengthen the bond between the lead frame and the resin. Specifically, Oshio teaches that “**anchor holes 180** are provided through the **lead 20 (30)** so that the **embedding resin 40** may fill in these **anchor holes 180**,” and explains that this design “serves to reduce ‘loosening’ between the leads and the injection molded object and to increase adhesion strength and contact area, so that peeloff of the leads from the **resin 40** can be prevented.” EX1006, [0078].

More specifically, anchor holes 180 are provided through the lead 20 (30) so that the embedding resin 40 may fill in these anchor holes 180. This serves to reduce “loosening” between the leads and the injection molded object and to increase adhesion strength and contact area, so that peeloff of the leads from the resin 40 can be prevented.

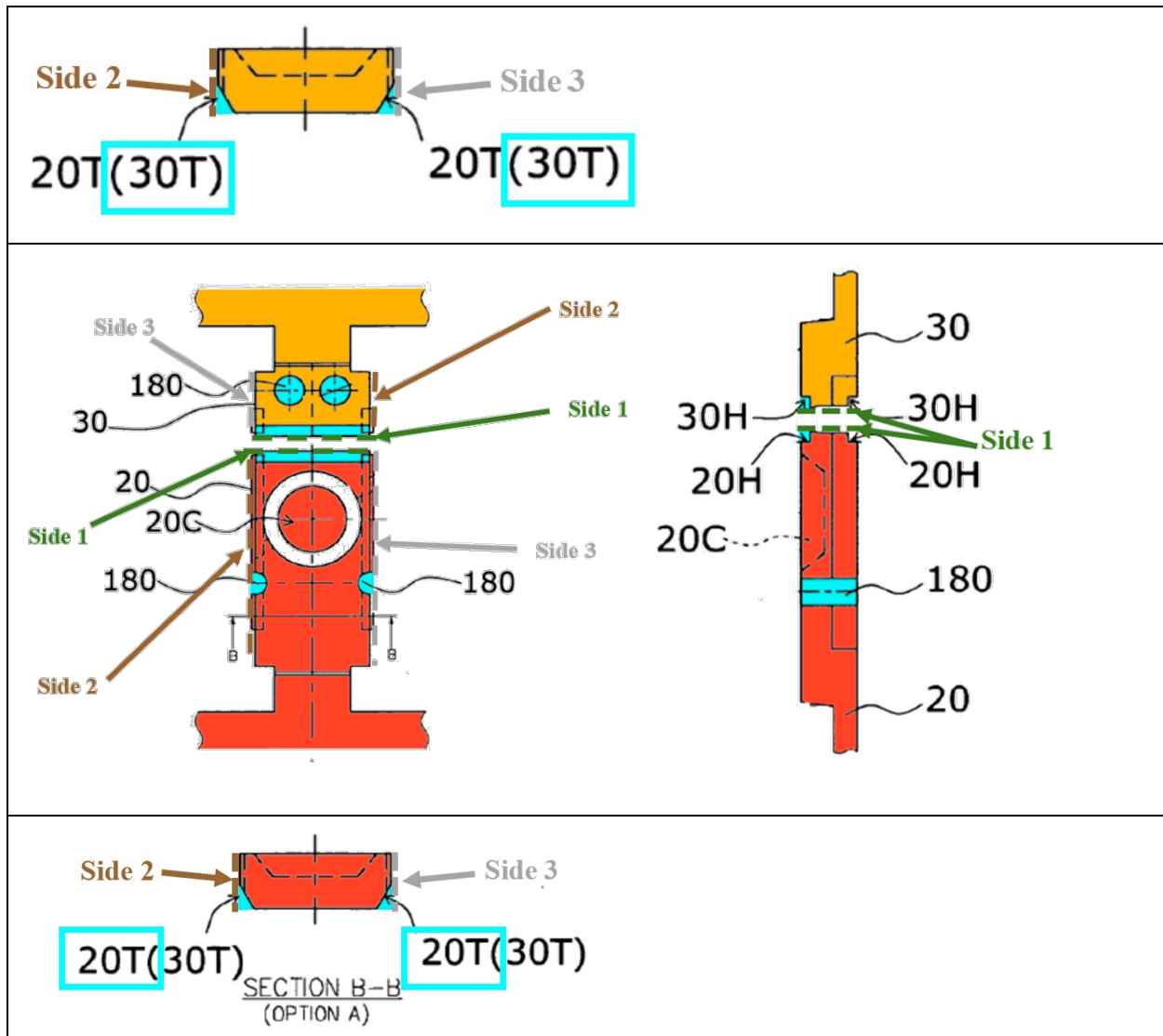
EX1006, [0078].

165. Oshio reiterates that the “**anchor holes 180, asperities 20H (30H), and tapered portion 20T (30T)** described above . . . serve to reduce ‘loosening’ between the leads and the injection molded object and to increase adhesion strength and contact area, so that peeloff of the leads from the **resin 40** can be prevented.” EX1006, [0081]; *see also* EX1006, [0051], [0087].

The anchor holes 180, asperities 20H (30H), and tapered portion 20T (30T) described above can be formed by presswork of the leads 20 and 30. They serve to reduce “loosening” between the leads and the injection molded object and to increase adhesion

strength and contact area, so that peeloff of the leads from the resin 40 can be prevented.

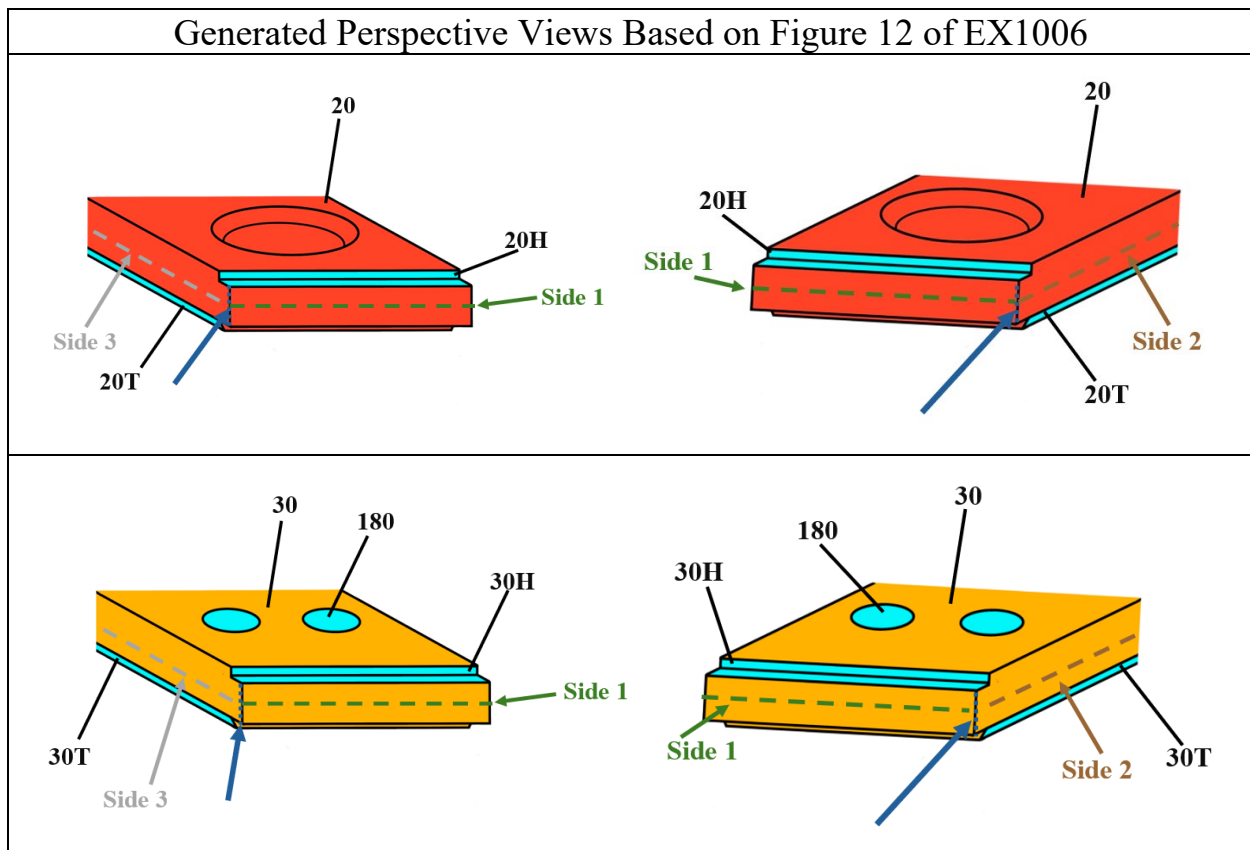
EX1006, [0081].



EX1006, Fig. 12.

166. Using the schematic views of Oshio's leads in Figure 12—a top view and two perpendicular cross-sectional views, I created the following perspective views of Oshio's **lead 20** and **lead 30** to clarify my explanation. As shown, Oshio

discloses that **upper asperity 20H** is positioned along the lateral side of **lead 20** that faces **lead 30** (“**Side 1**”). Additionally, Oshio teaches that **tapered portions 20T** are located along the lateral sides of **lead 20** adjacent to **Side 1** (“**Side 2**” and “**Side 3**”), with these **tapered portions** remaining separate from **upper asperity 20H** at the **corners** (marked in the Figures above with arrows) where **Side 2** and **Side 3** intersect with **Side 1**.



167. Similarly, Oshio discloses that, like **lead 20**, **lead 30** includes an **upper asperity 30H** positioned along the lateral side that faces **lead 20** (“**Side 1**”). Additionally, Oshio teaches that **tapered portions 30T** are located along the lateral

sides of **lead 30** adjacent to **Side 1** (“**Side 2**” and “**Side 3**”), with these tapered portions remaining separated from **upper asperity 30H** at the **corners** (marked in the Figures above with arrows) where **Side 2** and **Side 3** intersect with **Side 1**.

- vii. [6E] the **first** and the **second lead frames** comprise opposing sides facing each other, and the **resin-holding components** are disposed on the opposing sides.

168. Oshio teaches [6E].

169. As illustrated in Figure 5A, Oshio discloses that **lead 20** and **lead 30** have opposing sides that face each other, with **asperities 20H** and **30H** positioned on these opposing surfaces.

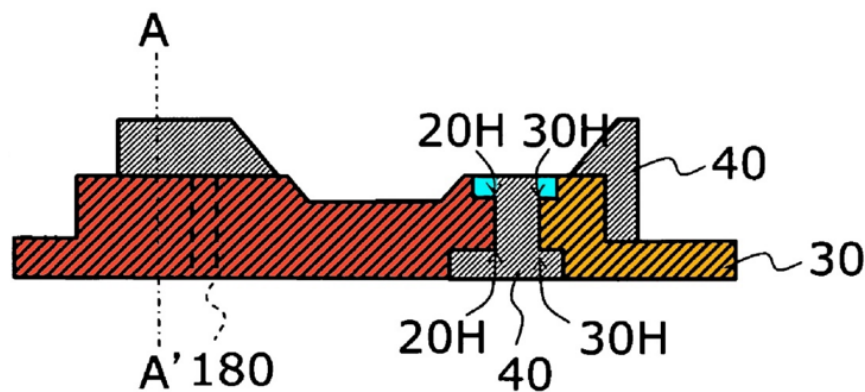


FIG. 5A

EX1006, Fig. 5A.

**3. Claims 2 and 3**

- i. [2] The LED package of claim 1, where the **resin-holding components** comprise at least one **hole**.
- ii. [3] The LED package of claim 2, wherein the **hole** is filled with the **resin** to increase the bonding force between the resin and the lead frames.

170. Oshio teaches claims [2] and [3] for at least the same reasons I already explained in Paragraphs 127-131 [Ground II, Claim 1, limitations 1D, 6D, 1E].

**4. Claim 4**

- i. [4] The LED package of claim 1, wherein the **resin-holding components** are disposed on three sides of at least one of the **first** and **second lead frames**.

171. Oshio teaches claim [4] for at least the same reasons I already explained in Paragraphs 127-131 [Ground II, Claim 1, limitations 1D, 6D, 1E].

**D. Ground IV: Oshio In Combination With Hui Renders Obvious Claims 1-4, And 6.**

**1. Claims 1 And 6**

- i. [1Pre, 6Pre] A light emitting diode (LED) package, comprising

172. Oshio teaches preambles [1Pre] and [6Pre] for at least the reasons I already explained in Paragraphs 145-149.

- ii. [1A, 6A] a **first lead frame** and a **second lead frame** separated from each other;

173. Oshio teaches [1A] and [6A] for at least the reasons I already explained in Paragraphs 150-152.

- iii. [1B, 6B] an **LED chip** disposed on the **first lead frame** and electrically connected with **second lead frame**; and

174. Oshio teaches [1B] and [6B] for at least the reasons I already explained in Paragraphs 153-155.

- iv. [1C, 6C] a **resin** covering at least portions of surfaces of the **first** and **second lead frames**, wherein:

175. Oshio teaches [1C] and [6C] for at least the reasons I already explained in Paragraphs 156-158.

- v. [1D, 6D] at least one of the **first** and **second lead frames** comprises **resin-holding components** disposed along adjacent sides of one of the **first** and **second lead frames**, the **resin-holding components** being separated from each other at corners of the adjacent sides; and:
- vi. [1E] the **resin-holding components** are disposed on two adjacent sides of each of the **first lead frame** and the **second lead frame**.

176. Oshio teaches [1D], [1E] and [6D] for at least the reasons I already explained in Paragraphs 159-167.

177. While silent in the claims, the '913 Patent states that “**slant parts 125, 145** [that] disperse the force diagonally, thereby preventing the **encapsulation**

material 20 from being broken on the opposite sides of the lead frames 12, 14.”

EX1001, 6:34–37. To the extent the “resin-holding components” require such slanted sides, Oshio in combination with Hui teaches [1D], [1E] and [6D]. In particular, such lead frames having slanted parts were well-known in the art, as shown by Hui. And it would have been obvious to a POSITA to use Hui’s “first and second electrodes 110, 115” that include such slanted sides. EX1005, [0035].

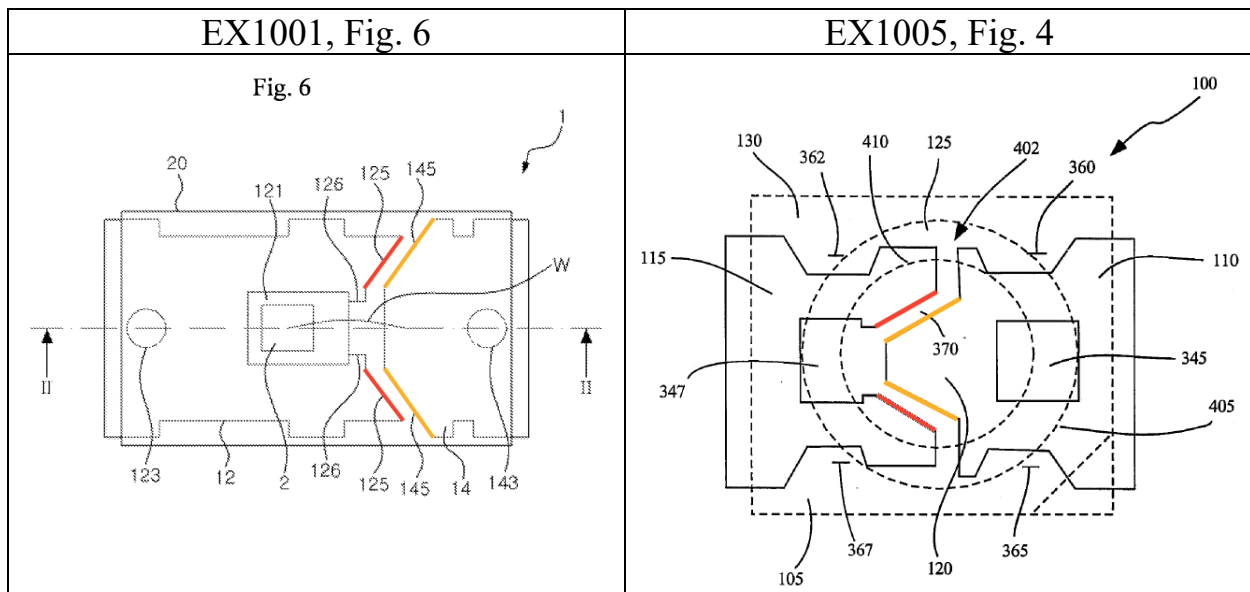


**FIG. 4 depicts a partially transparent overhead view of the surface mount device 100, transparently illustrating the casing 105 so that the first and second electrodes 110, 115 are visible through the casing 105, according to some embodiments.** The recess 125 in some implementations is generally conical in shape and includes a wall 402 that tapers from an outer perimeter of the recess at the second surface 130 of the casing 105 to an interior perimeter of the recess 410 at about the first and second electrodes 110, 115. As such, at least a portion of the first and second electrodes 110, 115 are exposed through the recess 125. Further, portions of the casing surrounding the exposed portions of the electrodes and within the interior perimeter 410 of the

recess 125 are also exposed through the recess 126. The embodiment of FIG. 4 depicts portions of the first and second electrode 110, 115, portions of the insulation gap 370, a first portion of the aperture 345, and a first portion of the inlet 347 extending into and being exposed through the recess 125.

EX1005, [0035].

178. A POSITA would have recognized that further modifying the combination of Oshio by incorporating Hui's teachings would have been an obvious design choice. Specifically, replacing Oshio's **lead 20** and **lead 30** with Hui's "**first** and **second electrodes 110, 115**" that feature slanted sides would have been a straightforward substitution. This modification involves nothing more than replacing one known component (Oshio's **lead 20** and **lead 30**) with another known component (Hui's **first** and **second electrodes** with slanted sides) while achieving the predictable result of forming an LED package. A POSITA would have had a reasonable expectation of success in making this substitution, as it maintains the overall function of the lead frames.

179. It would have at a minimum been obvious to explore different lead frame configurations, including those with varying shapes, such as the slanted-sided **first** and **second electrodes (110, 115)** taught by Hui. A POSITA would have been motivated to make this substitution because Hui explicitly teaches that "[t]he enhanced bonding provided through and around the **first** and **second electrodes 110,**

115, at least in part, enhance the stability of the **first** and **second electrodes 110, 115** relative to the casing 105 and the structural integrity of the surface mount device 100.” EX1005, [0047]. Hui further explains that “the structural integrity is further maintained, at least in part, through the electrodes 110, 115 adhering to the casing 105, the fill material, and/or the optoelectronic component.” EX1005, [0047]. Given these benefits, a POSITA would have understood that substituting Hsu’s **first terminal 70** and **second terminal 80** with Hui’s **first** and **second electrodes (110, 115)** could improve structural stability and adhesion, making it an obvious design choice.

The enhanced bonding provided through and around the first and second electrodes 110, 115, at least in part, enhances the stability of the first and second electrode 110, 115 relative to the casing 105 and the structural integrity of the surface mount device 100. The structural integrity is further maintained, at least in part, through the electrodes 110, 115 adhering to the casing 105, the fill material, and/or the optoelectronic element. In some embodiments, however, the bonding or adhesion between casing material, and/or between casing material and fill material is greater than the bonding or adhesion established between the casing and the electrodes, and between the electrodes and the fill material.

EX1005, [0047].

- vii. [6E] the **first** and the **second lead frames** comprise opposing sides facing each other, and the **resin-holding components** are disposed on the opposing sides.

180. Oshio alone or in combination with Hui teaches [6E] for at least the reasons I already explained in Paragraphs 168-169.

## 2. Claims 2 and 3

- i. [2] The LED package of claim 1, where the **resin-holding components** comprise at least one **hole**.
- ii. [3] The LED package of claim 2, wherein the **hole** is filled with the **resin** to increase the bonding force between the resin and the lead frames.

181. Oshio teaches claims [2] and [3] for at least the same reasons I already explained in Paragraph 170.

## 3. Claim 4

- i. [4] The LED package of claim 1, wherein the **resin-holding components** are disposed on three sides of at least one of the **first** and **second lead frames**.

182. Oshio teaches claim [4] for at least the same reasons I already explained in Paragraph 171.

## E. Ground V: Takasaki Anticipates Claims 1-4.

### 1. Overview of Takasaki (EX1007)

183. Takasaki is directed to “a light emitting diode device that can be made thinner and a method for manufacturing the same.” EX1007, [0011].

Another object of the present invention is to provide a light emitting diode device that can be made thinner and a method for manufacturing the same.

EX1007, [0011].

184. For example, Figures 1 and 2 of Takasaki show this “light emitting diode device 1” to have “a flat electrode plate (first electrode plate) 3 . . . and a flat electrode plate (second electrode plate) 4 . . . .” EX1007, [0056].

As shown in FIGS. 1 to 4 , the light emitting diode device 1 of Embodiment 1 has, in appearance, a flat rectangular encapsulant 2, a flat electrode plate (first electrode plate) 3 protruding from the lower part of one side surface of the encapsulant 2, and a flat electrode plate (second electrode plate) 4 protruding from the lower part of one side surface opposite the first side surface, and mounting holes 5 penetrating the electrode plates 3 and 4 are provided in the electrode plate portions protruding from both ends of the encapsulant 2. FIG. 1 is a perspective view of a light emitting diode device, FIG. 2 is a cross-sectional view taken along line A-A of FIG. 1, and FIG. 3 is a perspective view showing the state of the light emitting diode device with the transparent encapsulant removed. FIG. 4 is a perspective view of each component that constitutes a light emitting diode device, in which FIG. 4(a) shows a pair of electrode plates, FIG. 4(b) shows gold stud electrodes formed on the pair of electrode plates, and FIG. 4(c) shows a semiconductor chip.

EX1007, [0056].

185. Furthermore, the light emitting diode has an encapsulant made of transparent insulating resin. See EX1007, [Means for solving the problems] (“The white light emitting diode device has an encapsulant made of transparent insulating resin in which a yellow phosphor is dispersed.”).

The white light emitting diode device has an encapsulant made of transparent insulating resin in which a yellow phosphor is dispersed, a flat first electrode plate protruding from one end of the encapsulant, a flat second electrode plate protruding from the other end of the encapsulant, and a blue light emitting diode chip located within the encapsulant and having a p-electrode connected to the first electrode plate and an n-electrode connected to the second electrode plate, the first electrode plate and the second electrode plate being flat plate-like bodies of a constant thickness, and the lower surfaces of the first and second electrode plates are exposed to the lower surface of the encapsulant. The first and second electrode plate portions within the encapsulant are provided with through holes and recessed peripheral portions, and a portion of the lower surface is removed to make it thinner. The through holes, the openings, the recessed spaces, the thinned spaces, and the openings between the facing first and second electrode plates are filled with a resin that forms an encapsulant.

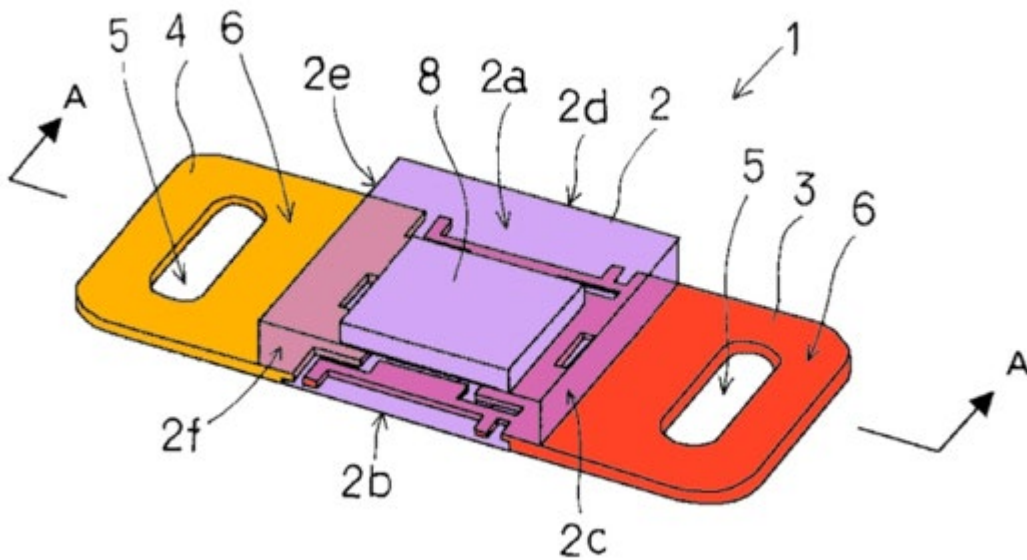
EX1007, [Means for solving the problems].

186. Takasaki further teaches that the encapsulant is used to seal the upper surfaces of the inner ends of a pair of **electrode plates 3** and **4**, as illustrated in Figure 1 below. See EX1007, [0056] (“The **encapsulant 2** is configured to seal first surfaces 6 (upper surfaces in FIG. 1) of the inner ends of a pair of **electrode plates 3** and **4** that are arranged in series and face each other.”

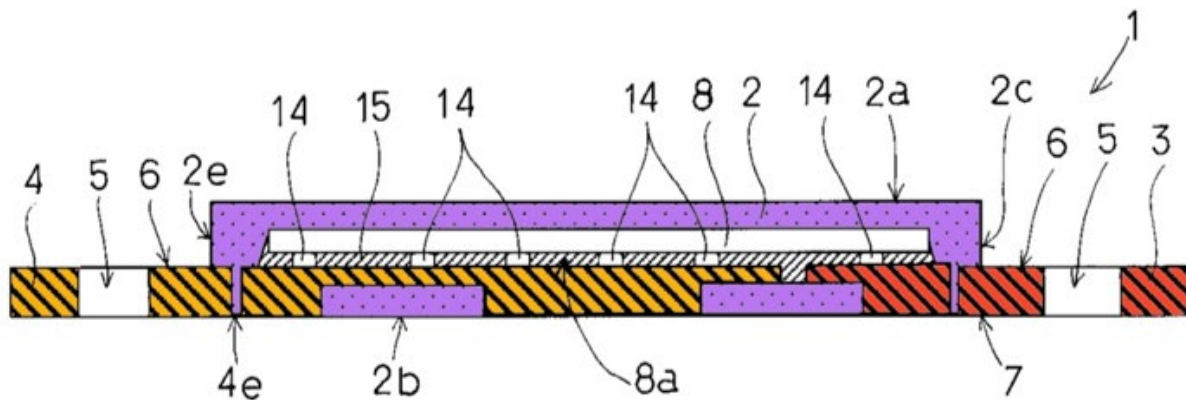
The encapsulant 2 is configured to seal first surfaces 6 (upper surfaces in FIG. 1) of the inner ends of a pair of electrode plates 3 and 4 that are arranged in series and face each other. The encapsulant 2 has a shape having a first surface 2a (the upper surface in FIG. 1), a second surface 2b (the lower surface in FIG. 1) that is the opposite surface to the first surface 2a, and a plurality of side surfaces (four side surfaces 2c to 2f) that connect

the periphery of the first surface 2a and the periphery of the second surface 2b. A pair of opposing side surfaces 2c, 2e of the encapsulant 2 are arranged across the electrode plates 3, 4 as shown in FIG. 1, and the remaining pair of side surfaces 2d, 2f extend along the edges of the electrode plates 3, 4 as described above.

EX1007, [0057]



EX1007, Fig. 1.



EX1007, Fig. 2.

187. Takasaki also discloses that the light-emitting diode device includes a “light emitting diode chip 8 [which] is mounted on the first surface 6 (upper surface) of each of the first and second electrode plates 3, 4 by flip chip connection.” EX1007, [0092].

According to the first embodiment, the following effects can be obtained.

(1) The second surfaces 7 (lower surfaces) of the first and second electrode plates 3 and 4 are exposed in a flat state on the lower surface of the light emitting diode device 1. Furthermore, a light emitting diode chip 8 is mounted on the first surface 6 (upper surface) of each of the first and second electrode plates 3, 4 by flip chip connection. As a result, when the light emitting diode device 1 is mounted on a mounting substrate, the heat generated in the light emitting diode chip 8 is dissipated to the mounting substrate from the second surfaces 7 of the first and second electrode plates 3, 4 which are in contact with the mounting substrate over a wide area, improving the heat dissipation characteristics and ensuring stable operation of the light emitting diode. Furthermore, the improved heat dissipation characteristics extend the life of the light emitting diode device 1. Therefore, it is possible to provide an excellent high-output white light emitting diode device 1 with good thermal characteristics.

EX1007, [0092].

188. And this “light emitting diode chip 8” emits blue light and is located within the encapsulant 2. EX1007, [0060].

A light emitting diode chip 8 that emits blue light is located within the encapsulant 2. The encapsulant 2 is made of a transparent insulating resin so that the light emitted from the light

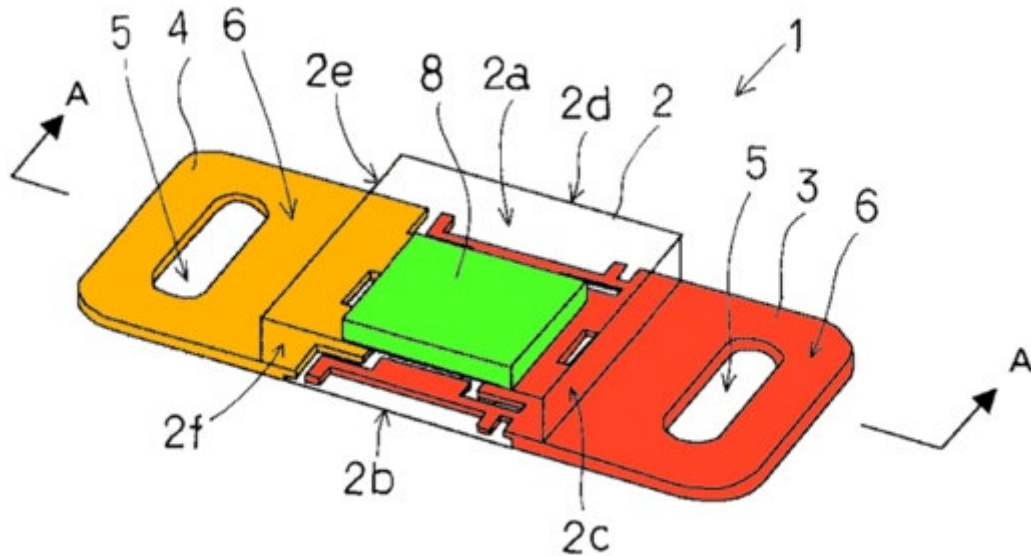
emitting diode chip 8 can be transmitted to the outside of the encapsulant 2. As the transparent insulating resin, an epoxy resin or a silicone resin, which is superior in resistance to ultraviolet light degradation and heat degradation compared to an epoxy resin, is used. Moreover, a yellow phosphor is dispersed and present within the resin that forms the encapsulant 2 so that the light emitting diode device 1 emits white light. As the yellow phosphor, yttrium aluminum garnet (YAG), which has yellow luminescence properties, is used.

EX1007, [0060].

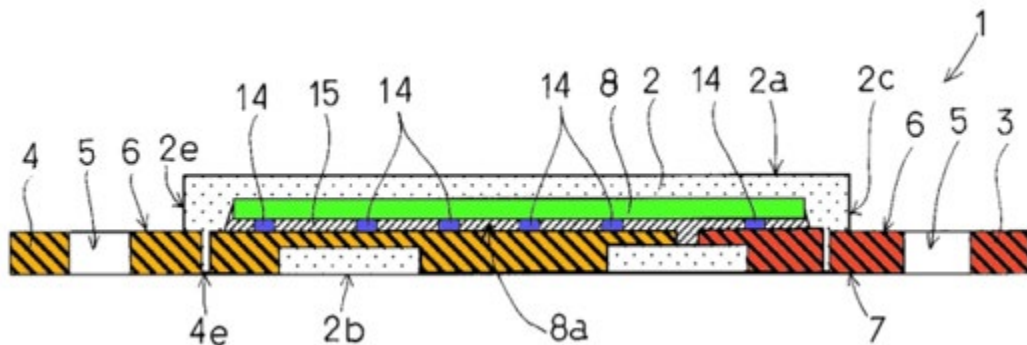
189. Takasaki further discloses that “the **electrode plates 3, 4** . . . a plurality of lands 9 are formed on the first surface 6” which “correspond[] to bump electrodes 11 provided on the first surface 8a of the **light emitting diode chip 8.**” EX1007, [0061].

As shown in FIGS. 2 and 3, the light emitting diode chip 8 is connected to the electrode plates 3 and 4 by flip chip connection as a connecting means. FIG. 4(a) is a perspective view showing the electrode plates 3, 4 in which a plurality of lands 9 are formed on the first surface 6. The land 9 is made of a gold stud electrode, for example, as shown in FIG. 4(b). The gold stud electrodes are formed by nail-head bonding gold wires to the electrode plates 3 and 4, and then cutting the gold wires near the connection portions. The cylindrical bonding tool (capillary) used for nail head bonding crushes the spherical tip (ball portion), resulting in the gold stud electrode taking on the shape shown in the schematic diagram of FIG. 4(b). These lands 9 are provided corresponding to bump electrodes 11 provided on the first surface 8a of the light emitting diode chip 8.

EX1007, [0061].



EX1007, Fig. 1.



EX1007, Fig. 2.

190. Takasaki teaches that “the connection portion between the bump electrode 11 provided on the first surface 8a of the **light emitting diode chip 8** and the lands 9 (gold stud electrodes) of the first electrode plate 3 and the second electrode plate 4” form “**a connection portion 14**,” or alternatively, instead of the

bump electrodes, the connection may be made by using a paste material of Au-Sn or a ribbon (sheet). EX1007, [0064], [0112].

In FIG. 2, the connection portion between the bump electrode 11 provided on the first surface 8a of the light emitting diode chip 8 and the lands 9 (gold stud electrodes) of the first electrode plate 3 and the second electrode plate 4 is shown as a connection portion 14.

EX1007, [0064].

In the embodiment, the case where the light emitting diode chip and the electrode plates (first and second electrode plates) are connected by a plurality of bump electrodes has been described. However, instead of the bump electrodes, the connection may be made by using a paste material of Au-Sn or a ribbon (sheet).

EX1007, [0112].

191. Takasaki further teaches a process in which “the **first electrode plate 3** and the **second electrode plate 4** are thinned by removing a predetermined depth from the second surface 7 side of the lead frame,” where the removal can be “performed, for example, by etching (half etching).” EX1007, [0080]. The etching can provide space, such as “**space 20a**” on the **first** and **second electrode plates 3, 4**. EX1007, [0081].

In FIG. 5, a single product forming portion 21 is shown. As shown in FIG. 5(a), in the product forming portion 21, the first electrode plate 3 and the second electrode plate 4 are thinned by removing a predetermined depth from the second surface 7 side of the lead frame 20. This removal is performed, for example, by etching (half etching). The lead frame 20 has a thickness of 0.2 mm, so that the etched portion has a thickness of 0.1 mm. The

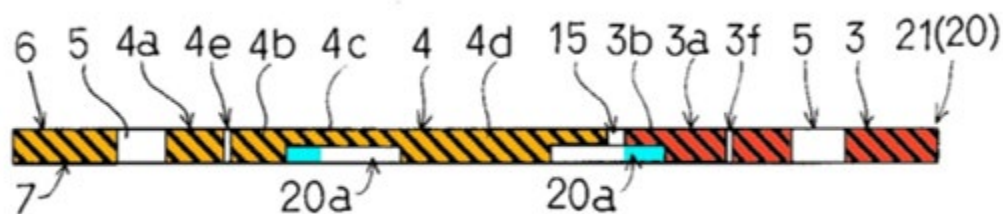
etched areas are, in the first electrode plate 3, the strip portion 3c outside the mid-width portion 3b, the recessed portion 3d, and the protruding portion 3e, and in the second electrode plate 4, a part of the same width portion 4a outside the mid-width portion 4b that faces the opening 17. In FIG. 5, 20a is a space 20a that is removed by etching.

EX1007, [0081].

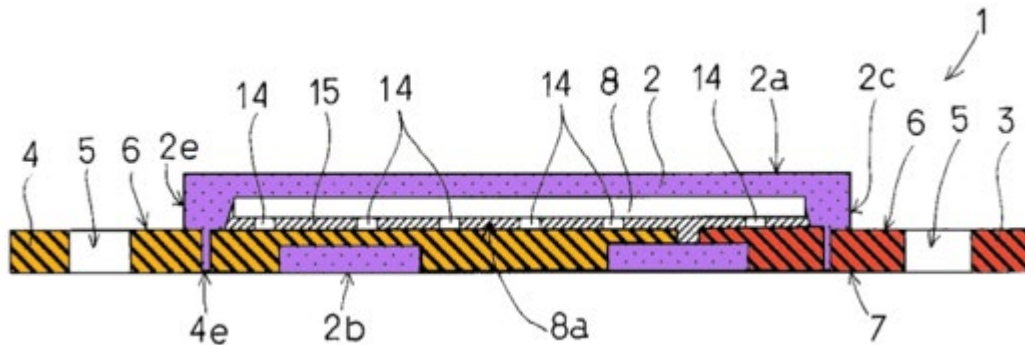
192. This space 20a can then holds the sealing body 2 formed of resin on the first and second electrode plates 3, 4, thereby “making it difficult for the electrode plates (first and second electrode plates 3, 4) to peel off from the sealing body, and improving the reliability of the sealing.” EX1007, [0093].

(2) In the electrode plate portions of the first and second electrode plates 3, 4 covered by the sealing body 2, the resin that forms the sealing body 2 is filled under the thin electrode plate portions, and the resin supports the thin electrode plate portions so that the electrode plates are well held by the sealing body 2, making it difficult for the electrode plates (first and second electrode plates 3, 4) to peel off from the sealing body, and improving the reliability of the sealing.

EX1007, [0093].



EX1007, Fig. 5(a).



EX1007, Fig. 2.

193. As can be readily seen in Figures 1 and 2 of Takasaki, the **electrode plates 3, 4** include **through holes 3f, 4e**. EX1007, [0073] (“the **electrode plates 3, 4** are formed with the **through holes 3f, 4e**.”

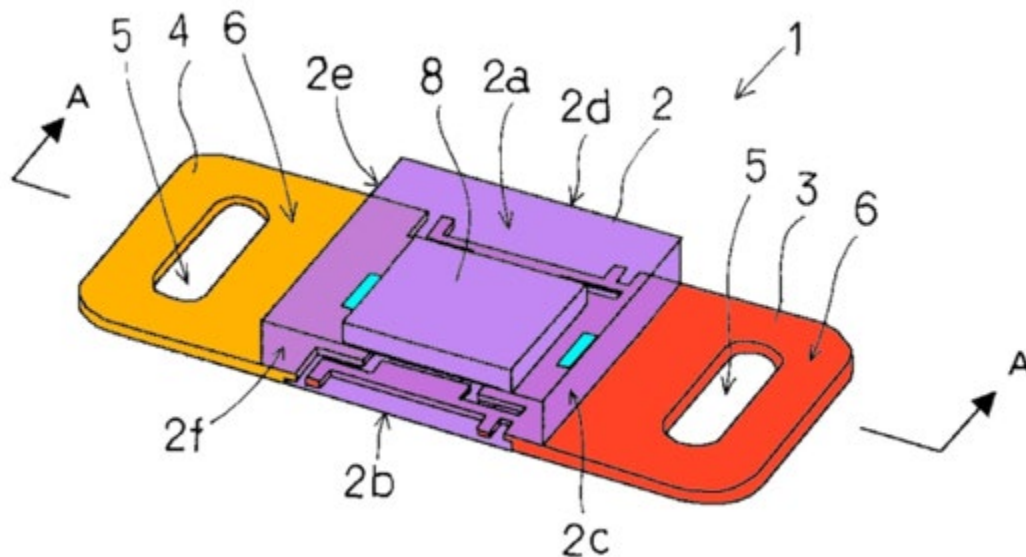
As described above, the electrode plates 3, 4 are formed with the through holes 3f, 4e, the medium width portion 3b, the strip portion 3c, the recessed portion 3d, the protruding portion 3e, the medium width portion 4b, the narrow portion 4c, and the narrow width portion 4d, as well as the openings 17 and the narrow grooves 3j, 4j. As a result, the facing portions between the peripheral edges of the first electrode plate 3 and the second electrode plate 4 have a complex interlocking structure. In addition, since the resin forming the encapsulant 2 fills the interlocking spaces, the contact area between the electrode plates 3, 4 and the resin is increased, and the interlocking structure is enlarged, thereby improving the adhesive strength between the encapsulant 2 and the electrode plates 3, 4. The adhesive strength between the encapsulant 2 and the electrode plates 3, 4 can be further increased by thinning a portion of the electrode plates 3, 4 and filling the thinned space with resin.

EX1007, [0073].

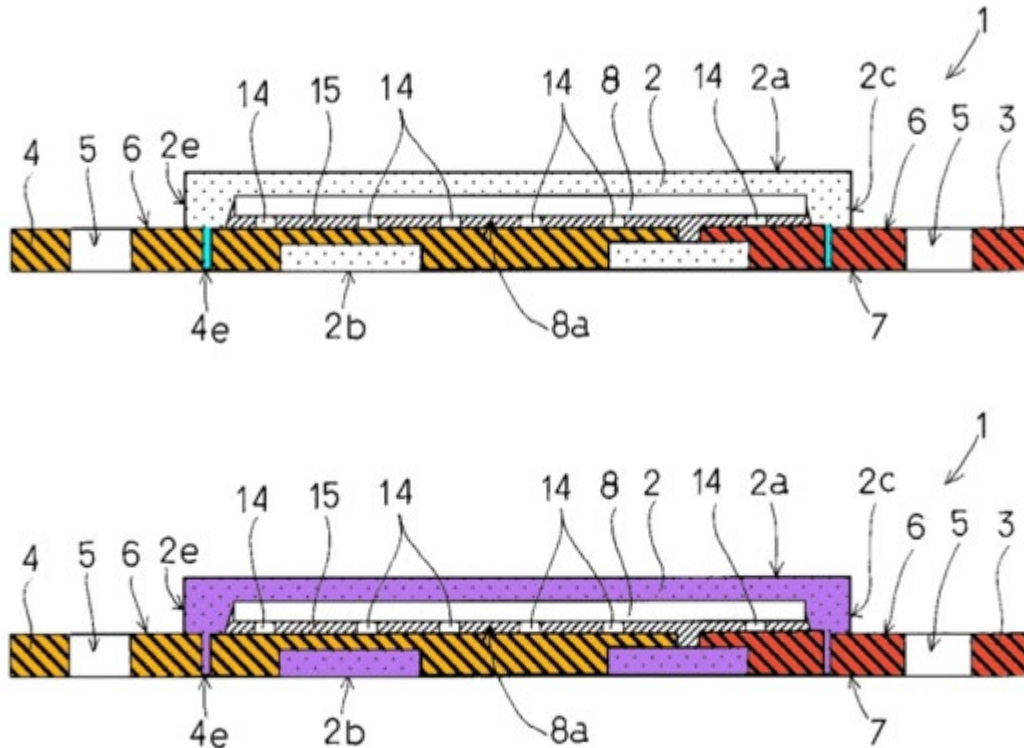
194. This structure provides structural stability to Takasaki's device. See EX1007, [0095] ("In the electrode plate portions of the **first** and **second electrode plates 3, 4** covered by the **encapsulant 2**, the **through holes (through holes 3f, 4e)** penetrating the electrode plates are filled with **resin** that forms the **encapsulant 2**, so that the **electrode plates** are held well by the **encapsulant 2**, the **electrode plates** are less likely to peel off from the **encapsulant 2**, and the reliability of the sealing is improved." EX1007, [0095].

(4) In the electrode plate portions of the first and second electrode plates 3, 4 covered by the encapsulant 2, the through holes (through holes 3f, 4e) penetrating the electrode plates are filled with resin that forms the encapsulant 2, so that the electrode plates are held well by the encapsulant 2, the electrode plates are less likely to peel off from the encapsulant 2, and the reliability of the sealing is improved.

EX1007, [0095].



EX1007, Fig. 1.



EX1007, Fig. 2.

## 2. Claim 1

**i. [1Pre] A light emitting diode (LED) package, comprising**

195. I understand that the preamble may not limit the claims. Regardless, Takasaki teaches [1Pre].

196. Takasaki is titled “Light emitting diode device and manufacturing methods thereof.” *See* EX1007, Title. And Takasaki teaches that an “object of the

present invention is to provide a light emitting diode device that can be made thinner.” EX1007, [0011].

Another object of the present invention is to provide a light emitting diode device that can be made thinner and a method for manufacturing the same.

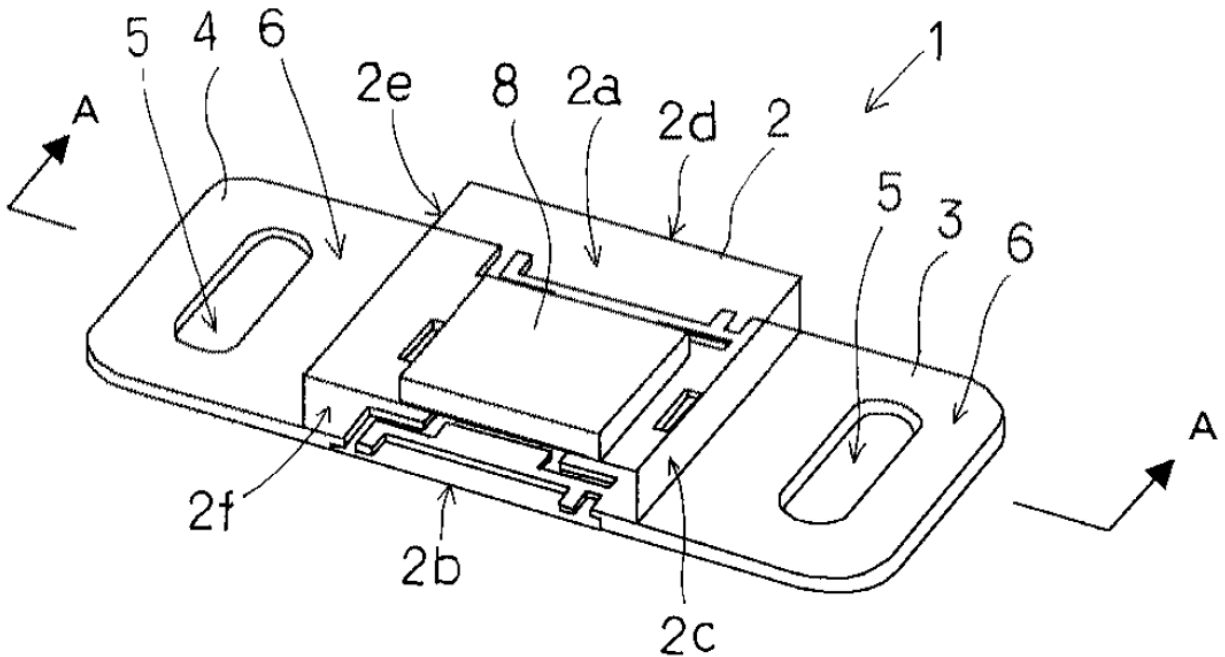
EX1007, [0011].

197. Takasaki shows structural composition of this LED device in Figures 1–4(a). As illustrated in these Figures, “the light emitting diode device 1 of Embodiment 1 has, in appearance, a flat rectangular encapsulant 2, a flat electrode plate (first electrode plate) 3 protruding from the lower part of one side surface of the encapsulant 2, and a flat electrode plate (second electrode plate) 4 protruding from the lower part of one side surface opposite the first side surface, and mounting holes 5 penetrating the electrode plates 3 and 4 are provided in the electrode plate portions protruding from both ends of the encapsulant 2.” EX1007, [0056].

As shown in FIGS. 1 to 4 , the light emitting diode device 1 of Embodiment 1 has, in appearance, a flat rectangular encapsulant 2, a flat electrode plate (first electrode plate) 3 protruding from the lower part of one side surface of the encapsulant 2, and a flat electrode plate (second electrode plate) 4 protruding from the lower part of one side surface opposite the first side surface, and mounting holes 5 penetrating the electrode plates 3 and 4 are provided in the electrode plate portions protruding from both ends of the encapsulant 2. FIG. 1 is a perspective view of a light emitting diode device, FIG. 2 is a cross-sectional view taken along line A-A of FIG. 1, and FIG. 3 is a perspective view showing the state of the light emitting diode device with the transparent encapsulant removed. FIG. 4 is a perspective view of

each component that constitutes a light emitting diode device, in which FIG. 4(a) shows a pair of electrode plates, FIG. 4(b) shows gold stud electrodes formed on the pair of electrode plates, and FIG. 4(c) shows a semiconductor chip.

EX1007, [0056].



EX1007, Fig. 1.

198. Takasaki further explains how the LED chip is positioned and connected within the package. Specifically, Takasaki discloses that that the “light emitting diode chip 8 is mounted on the first surface 6 (upper surface) of each of the first and second electrode plates 3, 4 by flip chip connection.” EX1007, [0092].

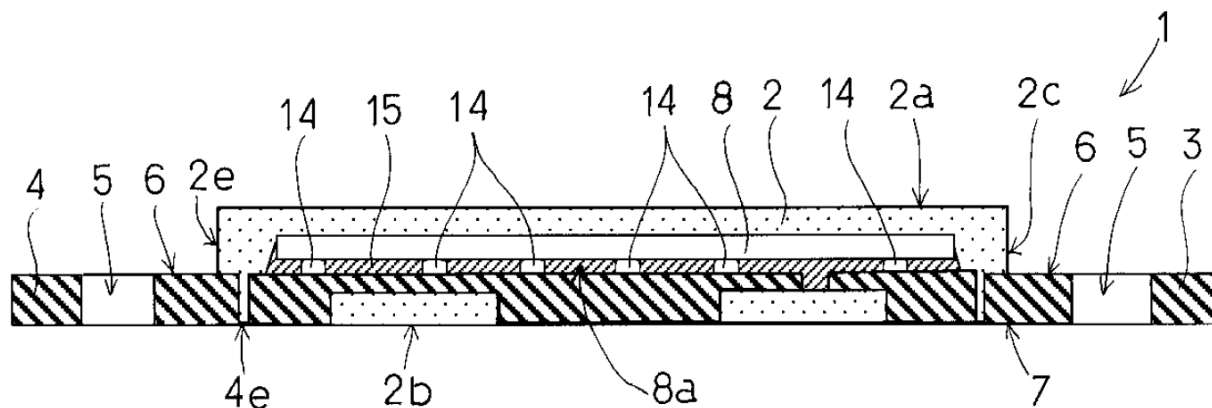
According to the first embodiment, the following effects can be obtained.

(1) The second surfaces 7 (lower surfaces) of the first and second electrode plates 3 and 4 are exposed in a flat state on the lower

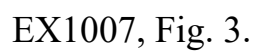
surface of the light emitting diode device 1. Furthermore, a light emitting diode chip 8 is mounted on the first surface 6 (upper surface) of each of the first and second electrode plates 3, 4 by flip chip connection. As a result, when the light emitting diode device 1 is mounted on a mounting substrate, the heat generated in the light emitting diode chip 8 is dissipated to the mounting substrate from the second surfaces 7 of the first and second electrode plates 3, 4 which are in contact with the mounting substrate over a wide area, improving the heat dissipation characteristics and ensuring stable operation of the light emitting diode. Furthermore, the improved heat dissipation characteristics extend the life of the light emitting diode device 1. Therefore, it is possible to provide an excellent high-output white light emitting diode device 1 with good thermal characteristics.

EX1007, [0092].

199. *See also, e.g.*, EX1007, [Problem to be solved], [Means for solving the problems], [0001], [0004], [0008–09], [0011–12], [0014], [0024], [0035], [0049–52], [0054–55], [0090], Claims 1–29.



EX1007, Fig. 2.



EX1007, Fig. 4(a).

- ii. [1A] a **first lead frame** and a **second lead frame** separated from each other;

200. Takasaki teaches [1A].

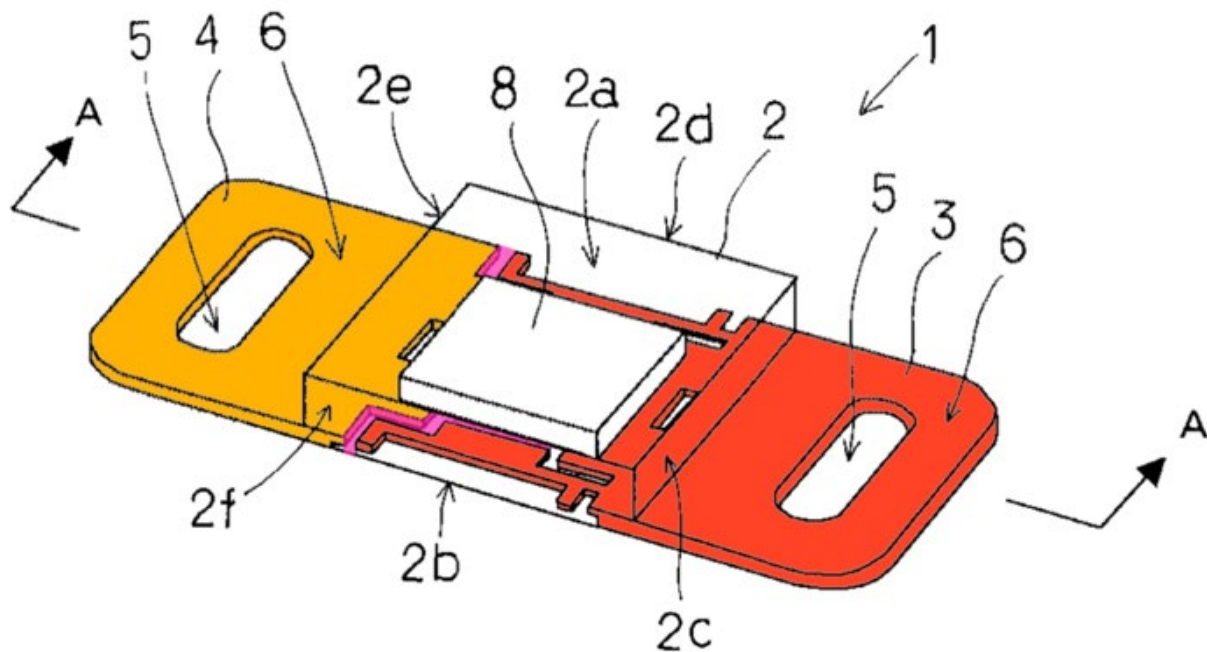
201. Takasaki's LED package includes two distinct electrode plates that are structurally and electrically **separated**. Specifically, Figures 1, 2, and 4(a) below illustrate this separation where "the light emitting diode device 1 of Embodiment 1 has . . . a **flat electrode plate (first electrode plate) 3** . . . and a **flat electrode plate (second electrode plate) 4** . . . ." EX1007, [0056]. Figure 1 provides "a perspective view of [the] light emitting diode device," while Figure 2 provides "a cross-sectional view taken along line A-A" of Figure 1. Moreover, Figure 4 provides "a perspective view of each component that constitutes a light emitting diode device, in which F[igure] 4(a) shows [the] pair of electrode plates . . . ." EX1007, [0056].

As shown in FIGS. 1 to 4, the light emitting diode device 1 of Embodiment 1 has, in appearance, a flat rectangular encapsulant 2, a flat electrode plate (first electrode plate) 3 protruding from the lower part of one side surface of the encapsulant 2, and a flat electrode plate (second electrode plate) 4 protruding from the lower part of one side surface opposite the first side surface, and mounting holes 5 penetrating the electrode plates 3 and 4 are provided in the electrode plate portions protruding from both ends of the encapsulant 2. FIG. 1 is a perspective view of a light emitting diode device, FIG. 2 is a cross-sectional view taken along line A-A of FIG. 1, and FIG. 3 is a perspective view showing the state of the light emitting diode device with the transparent encapsulant removed. FIG. 4 is a perspective view of

each component that constitutes a light emitting diode device, in which FIG. 4(a) shows a pair of electrode plates, FIG. 4(b) shows gold stud electrodes formed on the pair of electrode plates, and FIG. 4(c) shows a semiconductor chip.

EX1007, [0056].

202. Takasaki also describes “[a] light emitting diode device characterized by having . . . a conductive **first electrode plate** made of a flat plate-like body . . . [and] a conductive **second electrode plate** formed of a flat plate-like body, the second electrode plate being arranged in series with the first electrode plate . . .”). EX1007, claim 1. *See also*, EX1007, [Means for solving the problems], [0014], [0008], [0015–17], [0022], [0024], [0033], [0075], [0077], Claims 2–3, Claim 16.



EX1007, Figure 1.

203. Takasaki also describes the manufacturing process of the light emitting diode (LED) device in detail, explaining how the device is fabricated using a structured lead frame. Specifically, Takasaki discloses that “the light emitting diode device 1 is manufactured using a lead frame made of a flat plate of a constant thickness on which product forming portions for forming the light emitting diode device are arranged in a matrix. A **first electrode plate 3** and a **second electrode plate 4** are formed in the product forming section.” EX1007, [0058].

Also, as shown in FIG. 2, the second surface 7 (lower surface in FIGS. 1 and 2) of the electrode plates 3 and 4 opposite the first surfaces 6 are exposed on the second surface 2b side of the encapsulant 2. Further, the second surfaces 7 of the electrode plates 3 and 4 and the second surface 2b of the encapsulant 2 are positioned on approximately the same plate. As will be described later, the light emitting diode device 1 is manufactured using a lead frame made of a flat plate of a constant thickness on which product forming portions for forming the light emitting diode device are arranged in a matrix. A first electrode plate 3 and a second electrode plate 4 are formed in the product forming section. In addition, in the final step of manufacturing the light emitting diode device 1, the lead frame is cut lengthwise and crosswise with a dicing blade along the edges of the product forming section. As a result, the electrode plates 3, 4 are separated, the first surfaces 6 of the electrode plates 3, 4 are positioned on the same plate, and the second surfaces 7 of the electrode plates 3, 4 are positioned on the same plate.

EX1007, [0058].

204. Takasaki further explains the separation that occurs at the final step of manufacture to make sure that the initially connected lead frame structures are

divided into distinct electrode plates. EX1007, [0058] (“the final step of manufacturing the light emitting diode device 1, the lead frame is cut lengthwise and crosswise” such that “the **electrode plates 3, 4** are **separated . . . .**” .

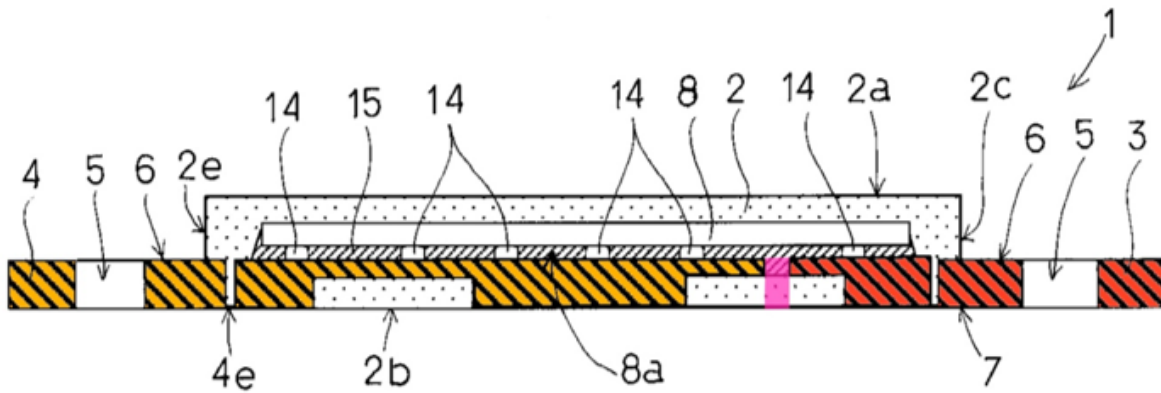
205. Takasaki explicitly teaches that the **flat electrode plate 3** and the **flat electrode plate 4** are separated by an “**opening 17** of a fixed width.” Takasaki states that “**openings 17** are formed between the strip portion 3c and the same width portion 4a and the medium width portion 4b, and between the protruding portion 3e and the narrow width portion 4d, and are bent.” EX1007, [0071]. This description indicates that the openings are consistently maintained across multiple structural regions of the electrode plates.

An opening 17 of a fixed width is provided between at least a portion of the peripheral surface of the first electrode plate 3 and at least a portion of the peripheral surface of the second electrode plate 4. The opening 17 is filled with a resin that forms the encapsulant 2, and is structured to increase the adhesive strength between the electrode plates 3 and 4 and the encapsulant 2. The openings 17 are formed between the strip portion 3c and the same width portion 4a and the medium width portion 4b, and between the protruding portion 3e and the narrow width portion 4d, and are bent.

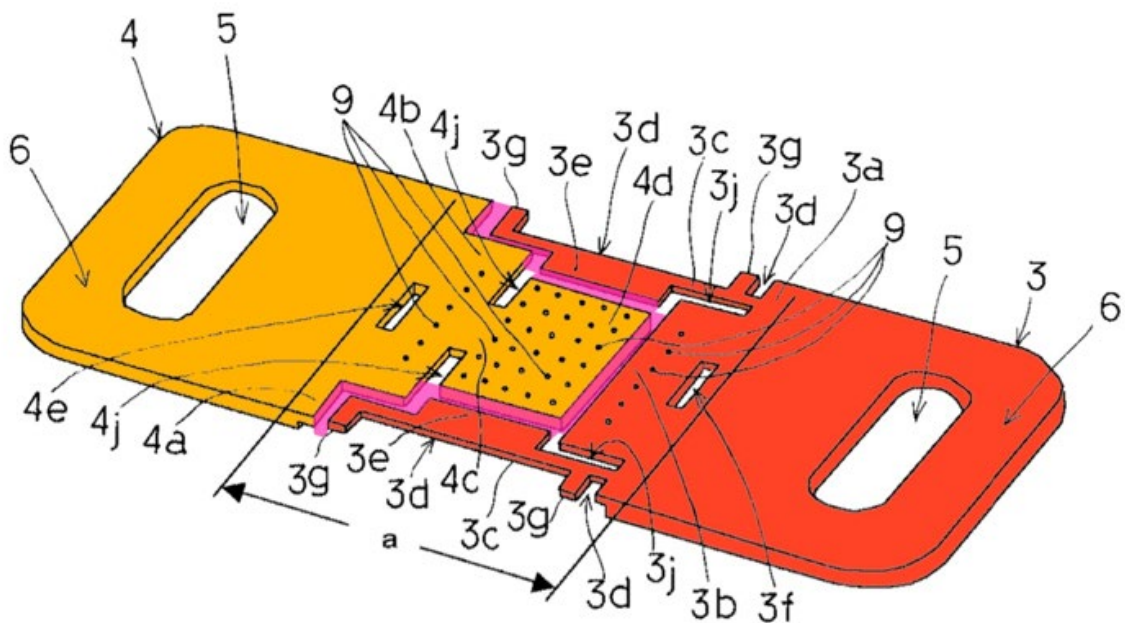
EX1007, [0071].

206. Takasaki also discloses this in claim 4, as it specifies that “an **opening** of a certain width is provided between at least a portion of a peripheral surface of the **first electrode plate** located within the encapsulant and at least a portion of a

peripheral surface of the **second electrode plate** located within the encapsulant, and the opening is filled with a resin that forms the encapsulant.”). EX1007, claim 4. See also EX1007, [0058] (“the **electrode plates 3, 4** are separated”), [0017], [0019], [0024], [0058], Claim 21.



EX1007, Fig. 2.



EX1007, Fig. 4(a).

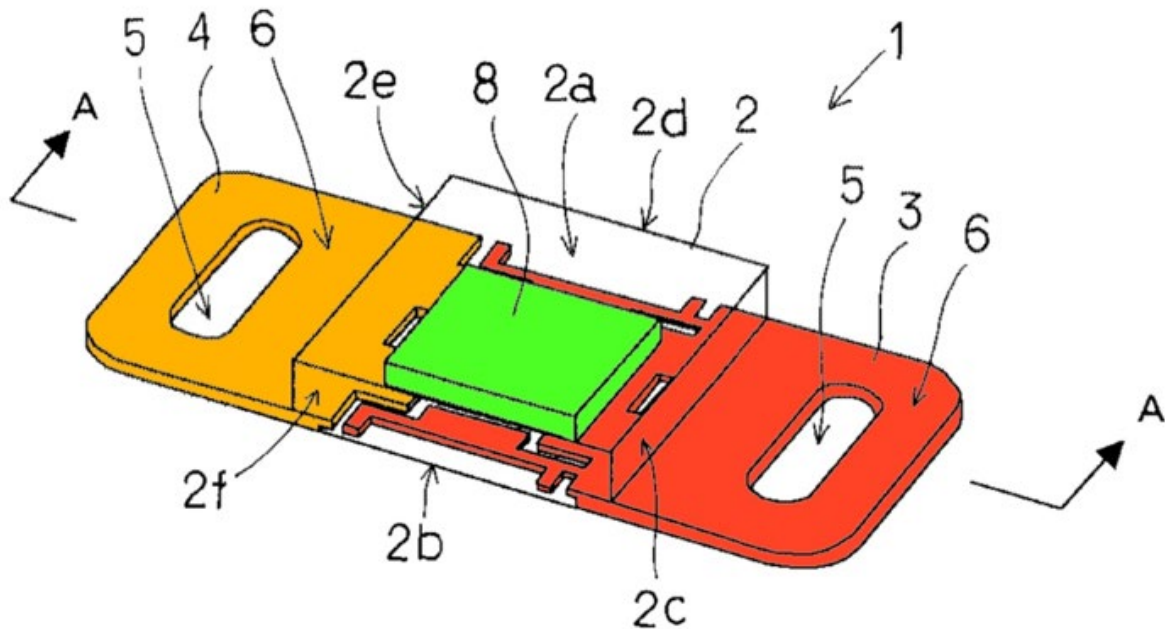
- iii. [1B] an LED chip disposed on the first lead frame and electrically connected with second lead frame; and

207. Takasaki teaches [1B]. For instance, as illustrated in Takasaki's Figures 1 and 2, the "light emitting diode chip 8 that emits blue light [is] located within the encapsulant 2." EX1007, [0060].

A light emitting diode chip 8 that emits blue light is located within the encapsulant 2. The encapsulant 2 is made of a transparent insulating resin so that the light emitted from the light emitting diode chip 8 can be transmitted to the outside of the encapsulant 2. As the transparent insulating resin, an epoxy resin or a silicone resin, which is superior in resistance to ultraviolet light degradation and heat degradation compared to an epoxy resin, is used. Moreover, a yellow phosphor is dispersed and present within the resin that forms the encapsulant 2 so that the light emitting diode device 1 emits white light. As the yellow phosphor, yttrium aluminum garnet (YAG), which has yellow luminescence properties, is used.

EX1007, [0060].

208. See also, e.g., EX1007, [Means for solving the problems], [0002–04], [0014], [0023–24], [0034–36], [0038], [0044], [0047], [0050], [0061–62], [0066], [0081], [0083–84], [0098–101], [0103–04], [0112], Claim 1, Claim 11, Claims 16–17.



EX1007, Fig. 1.

209. Takasaki discloses that the “**light emitting diode chip 8** is mounted on the first surface 6 (upper surface) of each of the **first** and **second electrode plates 3**, **4** by flip chip connection.” EX1007, [0092].

According to the first embodiment, the following effects can be obtained.

(1) The second surfaces 7 (lower surfaces) of the first and second electrode plates 3 and 4 are exposed in a flat state on the lower surface of the light emitting diode device 1. Furthermore, a light emitting diode chip 8 is mounted on the first surface 6 (upper surface) of each of the first and second electrode plates 3, 4 by flip chip connection. As a result, when the light emitting diode device 1 is mounted on a mounting substrate, the heat generated in the light emitting diode chip 8 is dissipated to the mounting substrate from the second surfaces 7 of the first and second electrode plates 3, 4 which are in contact with the mounting

substrate over a wide area, improving the heat dissipation characteristics and ensuring stable operation of the light emitting diode. Furthermore, the improved heat dissipation characteristics extend the life of the light emitting diode device 1. Therefore, it is possible to provide an excellent high-output white light emitting diode device 1 with good thermal characteristics.

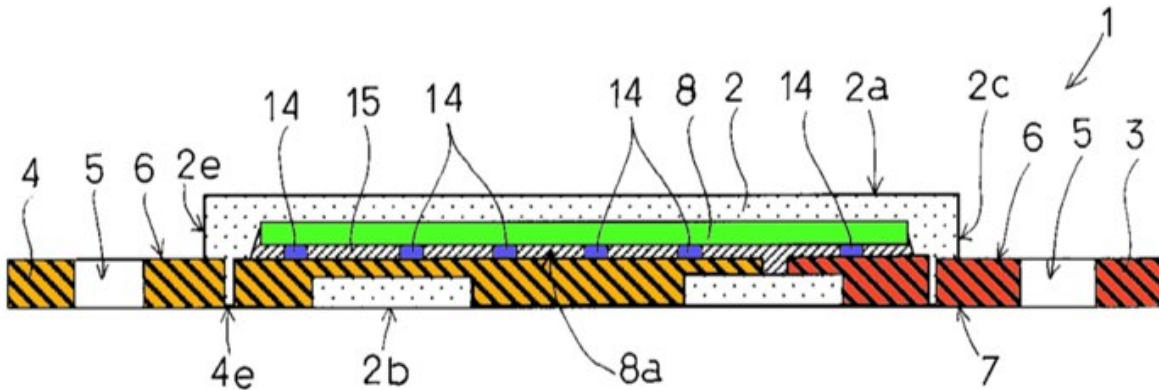
EX1007, [0092].

210. Takasaki further explains, for example, that in “the electrode plates **3**, **4** . . . a plurality of lands 9 are formed on the first surface 6” which “correspond[] to bump electrodes 11 provided on the first surface 8a of the **light emitting diode chip 8**.” EX1007, [0061]. And as provided in Figure 2 Takasaki also teaches that, “**the connection portion** between the bump electrode 11 provided on the first surface 8a of the **light emitting diode chip 8** and the lands 9 (gold stud electrodes) of the first electrode plate 3 and the second electrode plate 4” form “**a connection portion 14**.”

EX1007, [0064].

In FIG. 2, the connection portion between the bump electrode 11 provided on the first surface 8a of the light emitting diode chip 8 and the lands 9 (gold stud electrodes) of the first electrode plate 3 and the second electrode plate 4 is shown as a connection portion 14.

EX1007, [0064].



EX1007, Fig. 2.

211. Takasaki contemplates multiple connection methods between the light-emitting diode chip and the electrode plates. For instance, Takasaki further teaches that, as an alternative to bump electrodes “the connection may be made by using a paste material of Au-Sn or a ribbon (sheet).” EX1007, [0112].

In the embodiment, the case where the light emitting diode chip and the electrode plates (first and second electrode plates) are connected by a plurality of bump electrodes has been described. However, instead of the bump electrodes, the connection may be made by using a paste material of Au-Sn or a ribbon (sheet).

EX1007, [0112].

212. Additional disclosures in Takasaki further support this alternative connection approach. For example, Takasaki states that “[t]he white light-emitting diode device includes has . . . a flat **first electrode plate** protruding from one end of the encapsulant, a flat **second electrode plate** protruding from the other end of the encapsulant, and a blue **light emitting diode chip** located within the encapsulant

and having a p-electrode **connected to** the **first electrode plate** and an n-electrode **connected to** the **second electrode plate . . . .**”). EX1007, [Means for solving the problems].

The white light emitting diode device has an encapsulant made of transparent insulating resin in which a yellow phosphor is dispersed, a flat first electrode plate protruding from one end of the encapsulant, a flat second electrode plate protruding from the other end of the encapsulant, and a blue light emitting diode chip located within the encapsulant and having a p-electrode connected to the first electrode plate and an n-electrode connected to the second electrode plate, the first electrode plate and the second electrode plate being flat plate-like bodies of a constant thickness, and the lower surfaces of the first and second electrode plates are exposed to the lower surface of the encapsulant. The first and second electrode plate portions within the encapsulant are provided with through holes and recessed peripheral portions, and a portion of the lower surface is removed to make it thinner. The through holes, the openings, the recessed spaces, the thinned spaces, and the openings between the facing first and second electrode plates are filled with a resin that forms an encapsulant.

EX1007, [Means for solving the problems].

213. Similarly, Takasaki describes that the device comprises “a **light emitting diode chip** that is located within the sealed body, an electrode having a first polarity formed on the first surface is **connected to** the **first electrode plate** via a **connecting means**, an electrode having a second polarity formed on the first surface is **connected to** the **second electrode plate** via a **connecting means . . . .**”

EX1007, [0014].

A brief overview of representative inventions disclosed in this application is as follows.

The white light emitting diode device comprises:

an encapsulant made of transparent insulating resin having a first surface, a second surface opposite to the first surface, and a plurality of side surfaces connecting the periphery of the first surface and the periphery of the second surface, the resin having a dispersed yellow phosphor therein;

a conductive first electrode plate made of a flat plate-like body having one end located inside the encapsulant and another end protruding from the side surface to the outside of the encapsulant, a first surface located inside the encapsulant, and a second surface opposite to the first surface and exposed to the second surface side of the encapsulant;

a conductive second electrode plate formed of a flat plate-like body, the second electrode plate being arranged in series with the first electrode plate, one end side being located inside the sealing body with at least a portion of the circumferential surface facing the circumferential surface of the first electrode plate, the other end side being protruding from the side surface to the outside of the sealing body, the first surface being located inside the sealing body, and the second surface being the surface opposite to the first surface being exposed to the second surface side of the encapsulant; and

a light emitting diode chip that is located within the sealed body, an electrode having a first polarity formed on the first surface is connected to the first electrode plate via a connecting means, an electrode having a second polarity formed on the first surface is connected to the second electrode plate via a connecting means, and emits blue light, and radiates white light to the outside from the surface of the encapsulant.

EX1007, [0014].

214. *See also*, EX1007, [0039] (“Furthermore, a **light emitting diode chip** is mounted on the first surface (upper surface) of each of the **first** and **second electrode plates** by flip chip connection.”), [0014], [0023–24], [0026], [0036], [0044], [0047], [0061–62], [0066], [0081], [0083–84], [0098–101], [0103], Claim 1, Claim 11, Claims 16–17.

iv. [1C] a **resin covering at least portions of surfaces of the first and second lead frames**, wherein:

215. Takasaki teaches [1C].

216. Takasaki discloses that the “light emitting diode device has an **encapsulant made of transparent insulating resin**...” EX1007, [Means for solving the problems]. As shown in Figures 1 and 2, this encapsulant encloses the internal components of the device while allowing light transmission.

The white light emitting diode device has an encapsulant made of transparent insulating resin in which a yellow phosphor is dispersed, a flat first electrode plate protruding from one end of the encapsulant, a flat second electrode plate protruding from the other end of the encapsulant, and a blue light emitting diode chip located within the encapsulant and having a p-electrode connected to the first electrode plate and an n-electrode connected to the second electrode plate, the first electrode plate and the second electrode plate being flat plate-like bodies of a constant thickness, and the lower surfaces of the first and second electrode plates are exposed to the lower surface of the encapsulant. The first and second electrode plate portions within the encapsulant are provided with through holes and recessed peripheral portions, and a portion of the lower surface is removed to make it thinner. The through holes, the openings, the recessed

spaces, the thinned spaces, and the openings between the facing first and second electrode plates are filled with a resin that forms an encapsulant.

EX1007, [Means for solving the problems].

217. Takasaki further describes that the “**encapsulant 2** is configured to **seal** first surfaces 6 (upper surfaces in FIG. 1) of the inner ends of a pair of **electrode plates 3** and **4** that are arranged in series and face each other.” EX1007, [0057].

The encapsulant 2 is configured to seal first surfaces 6 (upper surfaces in FIG. 1) of the inner ends of a pair of electrode plates 3 and 4 that are arranged in series and face each other. The encapsulant 2 has a shape having a first surface 2a (the upper surface in FIG. 1), a second surface 2b (the lower surface in FIG. 1) that is the opposite surface to the first surface 2a, and a plurality of side surfaces (four side surfaces 2c to 2f) that connect the periphery of the first surface 2a and the periphery of the second surface 2b. A pair of opposing side surfaces 2c, 2e of the encapsulant 2 are arranged across the electrode plates 3, 4 as shown in FIG. 1, and the remaining pair of side surfaces 2d, 2f extend along the edges of the electrode plates 3, 4 as described above.

EX1007, [0057].

218. *See also, e.g.,* EX1007, [0025] (“selectively forming a **resin** layer on the first surface side of the **lead frame** using an insulating **resin** having a yellow phosphor dispersed therein so as to cover the semiconductor chip and the **first** and **second electrode plate** portions”).

Such a light emitting diode device includes the following manufacturing steps: (a) a step of preparing a light emitting diode chip that has an electrode having a first polarity and an

electrode having a second polarity on a first surface and emits blue light;

(b) a step of preparing a lead frame having at least one product forming section consisting of a rectangular frame

and a first electrode plate and a second electrode plate positioned within the frame, with a portion of the peripheral surface facing each other and arranged in series and supported by the frame at a connecting portion,

and the first surface of the first electrode plate portion and the second electrode plate portion facing the product forming section are arranged on the first surface of the product forming section, and are configured so that the semiconductor chip is stacked on the first surface of the product forming section;

(c) a step of preparing a lead frame made of a copper or copper alloy plate, which has a flat plate-like body of a certain thickness, which has a structure in which the semiconductor chip is stacked on the first surface of the first electrode plate portion and the second electrode plate portion on the facing side of the product forming section; and a step of overlapping the first surface of the lead frame with the second electrode plate portion, connecting the electrode of the semiconductor chip having the first polarity to the first electrode plate by a connecting means, and connecting the electrode of the semiconductor chip having the second polarity to the second electrode plate by a connecting means;

(d) a step of exposing the second surfaces of the first and second electrode plates and the first electrode plate portion and the second electrode plate portion away from the semiconductor chip, and selectively forming a resin layer on the first surface side of the lead frame using an insulating resin having a yellow phosphor dispersed therein so as to cover the semiconductor chip and the first and second electrode plate portions; and

(e) a step of cutting and removing the connecting portion and unnecessary resin layer.

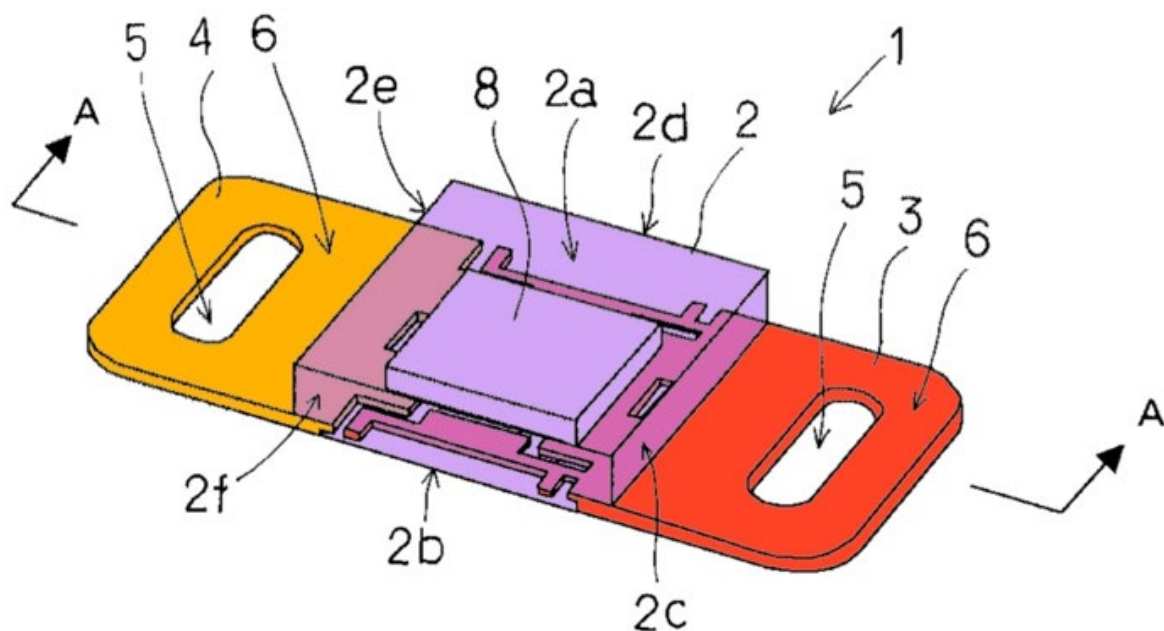
EX1007, [0025]

219. Takasaki also discusses measures to enhance adhesion between the encapsulant and the electrode plates, explaining that “as shown in FIG. 4(a), various measures are taken in the embodiment to improve the bondability (adhesion) of the electrode plate portions of the **electrode plates 3** and **4** covered by the **encapsulant 2** with the **resin** that forms the **encapsulant 2**. The area indicated by a in FIG. 4(a) is the sealing area in the **electrode plates 3** and **4**.”). EX1007, [0066].

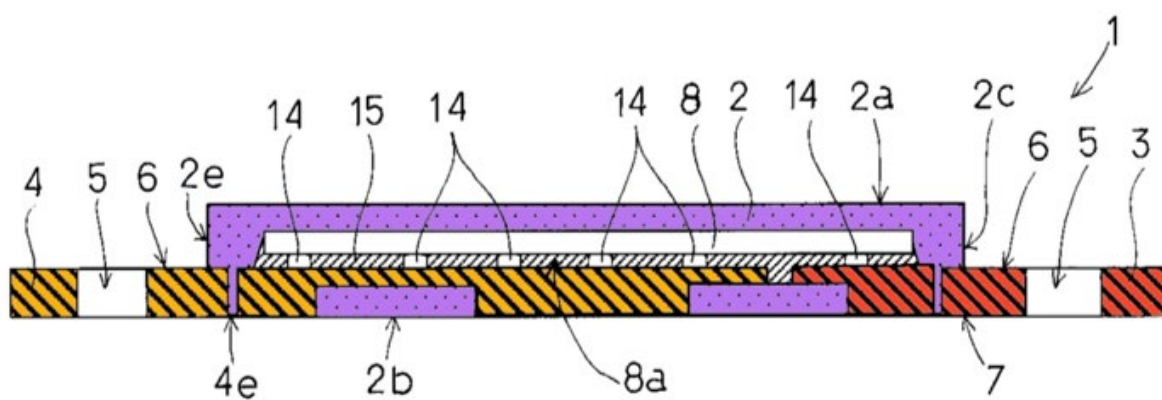
On the other hand, as shown in FIG. 4(a), various measures are taken in the embodiment to improve the bondability (adhesion) of the electrode plate portions of the electrode plates 3 and 4 covered by the encapsulant 2 with the resin that forms the encapsulant 2. The area indicated by a in FIG. 4(a) is the sealing area in the electrode plates 3 and 4.

EX1007, [0066].

220. *See also* EX1007, [Means for solving the problems], [0008], [0014], [0016], [0018–19], [0021], [0027], [0033], [0035], [0039], [0055], [0057–58], [0059], [0066], [0072], [0086–87], [0092], [0093–94], [0104], Claim 1, Claim 3, Claim 16, all providing disclosure of an encapsulant structure that ensures both protection and functional integration within the device.



EX1007, Fig. 1.



EX1007, Fig. 2.

- v. [1D] at least one of the **first** and **second lead frames** comprises **resin-holding components** disposed along adjacent sides of one of the **first** and **second lead frames**, the **resin-holding components** being separated from each other at **corners** of the adjacent sides; and
- vi. [1E] the **resin-holding components** are disposed on two adjacent sides of each of the **first lead frame** and the **second lead frame**.

221. Takasaki teaches [1D and 1E].

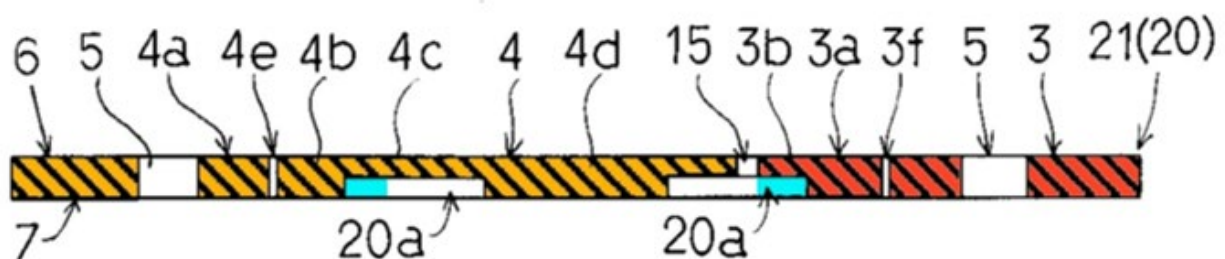
222. As an initial matter, Takasaki discloses “at least one of the **first** and **second lead frames** comprises **resin-holding components**” including as created by “**space 20a**” along multiple sides of the **first electrode plate 3** and the **second electrode plate 4**. This indicates that the electrode plates include structural features specifically designed to retain resin within the encapsulant. And as I explain further below, these **resin-holding components** formed by **space 20a** (in the **first electrode plate 3** and the **second electrode plate 4**) are formed by thinning portions of the **first** and **second electrode plates**, creating channels along multiple vertical sides of the plates. These channels serve as defined spaces that are subsequently filled with **resin**, ensuring secure encapsulation and improved adhesion between the encapsulant and the **first** and **second electrode plates**.

223. Takasaki describes a process in which “the **first electrode plate 3** and the **second electrode plate 4** are thinned by removing a predetermined depth from

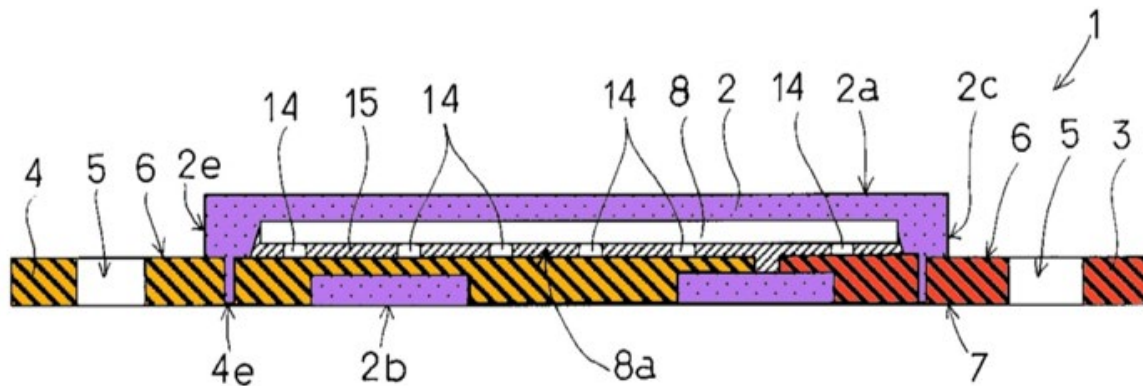
the second surface 7 side of the lead frame.” EX1007, [0081]. This thinning is achieved through material removal techniques such as “for example, by etching (half etching).” EX1007, [0081]. As a result of this etching process, structural features such as “space 20a” are formed on the first and second electrode plates 3 and 4. EX1007, [0081]. These spaces contribute to the formation of resin-holding components, providing defined areas where resin can be retained within the encapsulant. See also illustrations in Figures 5(a) and 2 below.

In FIG. 5, a single product forming portion 21 is shown. As shown in FIG. 5(a), in the product forming portion 21, the first electrode plate 3 and the second electrode plate 4 are thinned by removing a predetermined depth from the second surface 7 side of the lead frame 20. This removal is performed, for example, by etching (half etching). The lead frame 20 has a thickness of 0.2 mm, so that the etched portion has a thickness of 0.1 mm. The etched areas are, in the first electrode plate 3, the strip portion 3c outside the mid-width portion 3b, the recessed portion 3d, and the protruding portion 3e, and in the second electrode plate 4, a part of the same width portion 4a outside the mid-width portion 4b that faces the opening 17. In FIG. 5, 20a is a space 20a that is removed by etching.

EX1007, [0081].



EX1007, Fig. 5(a).



EX1007, Fig. 2.

224. Takasaki also discloses that the **space 20a** formed on the bottom side of the **first** and **second electrode plates 3, 4** serves to hold the **sealing body 2** formed of **resin**. This configuration improves the adhesion between the **first electrode plate 3** and **second electrode plate 4**, thereby making it difficult for the electrode plates (**first** and **second electrode plates 3, 4**) to peel off from the **sealing body**, and improving the reliability of the sealing.” EX1007, [0092]. Takasaki further explains that in the portions of the **first electrode plate 3** and **second electrode plate 4**, “the **resin** that forms the **sealing body 2** is filled **under the thin electrode plate portions**, and the **resin** supports the thin electrode plate portions so that the electrode plates are well held by the **sealing body 2**.” EX1007, [0093].

(2) In the electrode plate portions of the first and second electrode plates 3, 4 covered by the sealing body 2, the resin that forms the sealing body 2 is filled under the thin electrode plate portions, and the resin supports the thin electrode plate portions

so that the electrode plates are well held by the sealing body 2, making it difficult for the electrode plates (first and second electrode plates 3, 4) to peel off from the sealing body, and improving the reliability of the sealing.

EX1007, [0093].

225. Additional disclosures from Takasaki further support this. For example, Takasaki describes that “[i]n the electrode plate portion located within the encapsulant of the first and second electrode plates, the second surface side of the electrode plate is partially removed to make it thinner, and the removed portion is filled with a resin that forms the encapsulant.” EX1007, [0017]. *See also, e.g.*, EX1007, [Means for solving the problems], [0039], [0072], [0095], Claim 3, Claim 20.

(B) In the electrode plate portion located within the encapsulant of the first and second electrode plates, the second surface side of the electrode plate is partially removed to make it thinner, and the removed portion is filled with a resin that forms the encapsulant.

EX1007, [0017].

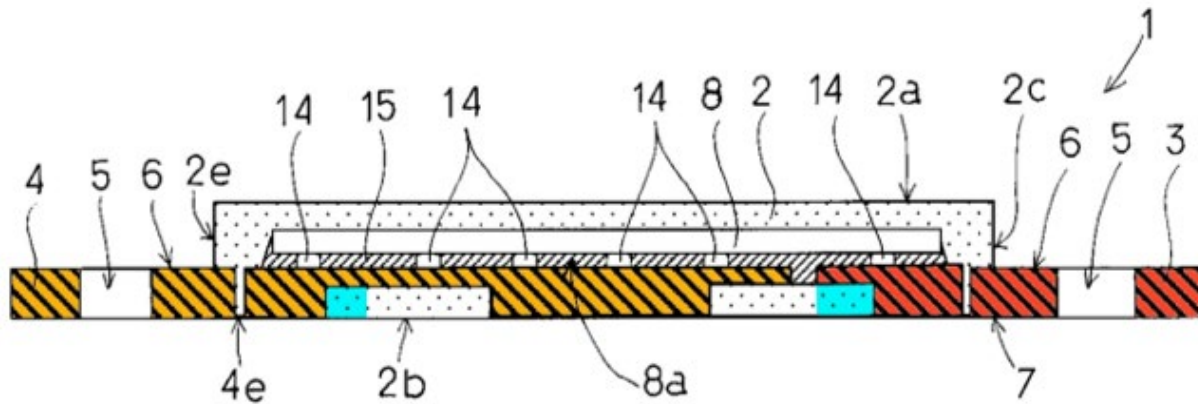
226. Takasaki further discloses that the thinned portion of electrode plate 4 shown on the left below extends “from the middle part of the same width portion 4a to the constricted part 4c.” EX1007, [0068]. As shown in Figures 2 and 7, this thinning process results in defined structural modifications to electrode plate 4.

Note that the **resin-holding components** are not visible in Figure 7, therefore I have indicated where they exist outside the plane of the page.

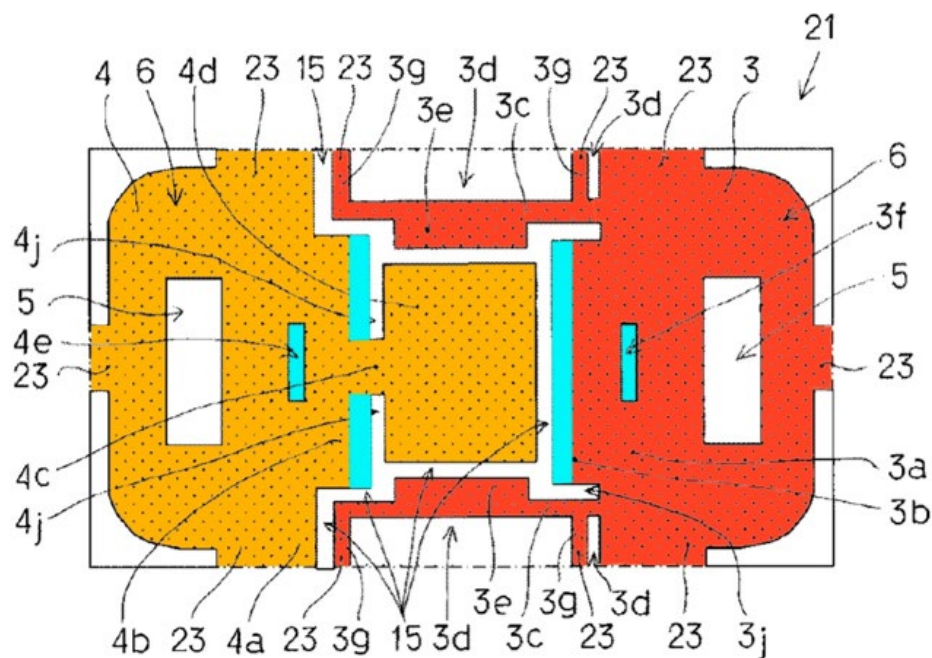
Further, as shown in FIGS. 1 and 2, on both sides of the second surface 7 of the second electrode plate 4, a predetermined thickness is removed from the middle part of the same width portion 4a to the constricted part 4c, making it thin. Then, this removed portion is filled with a resin that forms an encapsulant 2, as shown in FIG. 2. By filling the resin, the bonding between the encapsulant 2 and the second electrode plate 4 becomes strong. The portion of the second electrode plate 4 where the light emitting diode chip 8 is fixed is structured so that the electrode plate does not become thin and can efficiently transfer heat to the mounting board.

EX1007, [0068].

227. As depicted on the left side of Figure 7, the **thinned area** of **electrode plate 4**, positioned perpendicular to the constricted part 4c, creates **resin-holding components** along two vertical sides of **electrode plate 4**. On the right side of Figure 7, **electrode plate 3** includes a thinned region. This configuration introduces a **resin-holding component** along the vertical side of **electrode plate 3** that faces **electrode plate 4**.



EX1007, Fig. 2.



EX1007, Fig. 7.

228. Furthermore, Takasaki also discloses “at least one of the **first** and **second lead frames** comprises **resin-holding components**” in the form of **through-**

holes positioned along the upper and lower sides of both the first electrode plate 3 and the second electrode plate 4. These through-holes are filled with resin.

229. In particular, as shown in Figures 1, 2, and 7 below, Takasaki provides that “the electrode plates 3, 4 are formed with the through holes 3f, 4e.” EX1007, [0073]. Therefore, the through-holes serve a structural function within the encapsulated device by allowing resin to flow through and integrate with the electrode plates during encapsulation.

As described above, the electrode plates 3, 4 are formed with the through holes 3f, 4e, the medium width portion 3b, the strip portion 3c, the recessed portion 3d, the protruding portion 3e, the medium width portion 4b, the narrow portion 4c, and the narrow width portion 4d, as well as the openings 17 and the narrow grooves 3j, 4j. As a result, the facing portions between the peripheral edges of the first electrode plate 3 and the second electrode plate 4 have a complex interlocking structure. In addition, since the resin forming the encapsulant 2 fills the interlocking spaces, the contact area between the electrode plates 3, 4 and the resin is increased, and the interlocking structure is enlarged, thereby improving the adhesive strength between the encapsulant 2 and the electrode plates 3, 4. The adhesive strength between the encapsulant 2 and the electrode plates 3, 4 can be further increased by thinning a portion of the electrode plates 3, 4 and filling the thinned space with resin.

EX1007, [0073].

230. Takasaki further explains that the through-holes not only facilitate adhesion between the encapsulant and the electrode plates but also enhance mechanical stability by reducing the likelihood of delamination. EX1007, [0095]

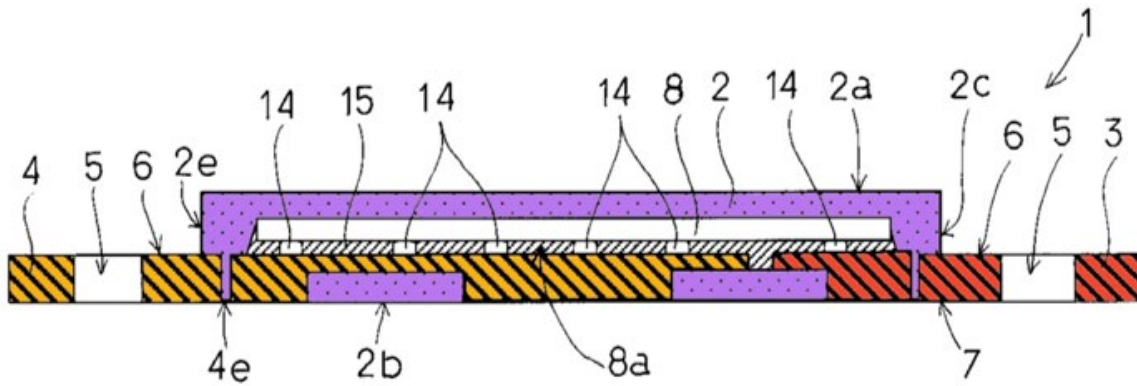
(“In the electrode plate portions of the **first** and **second electrode plates 3, 4** covered by the **encapsulant 2**, the **through holes (through holes 3f, 4e)** penetrating the electrode plates are filled with **resin** that forms the **encapsulant 2**, so that the **electrode plates** are held well by the **encapsulant 2**, the **electrode plates** are less likely to peel off from the **encapsulant 2**, and the reliability of the sealing is improved.” EX1007, [0095].

(4) In the electrode plate portions of the first and second electrode plates 3, 4 covered by the encapsulant 2, the through holes (through holes 3f, 4e) penetrating the electrode plates are filled with resin that forms the encapsulant 2, so that the electrode plates are held well by the encapsulant 2, the electrode plates are less likely to peel off from the encapsulant 2, and the reliability of the sealing is improved.

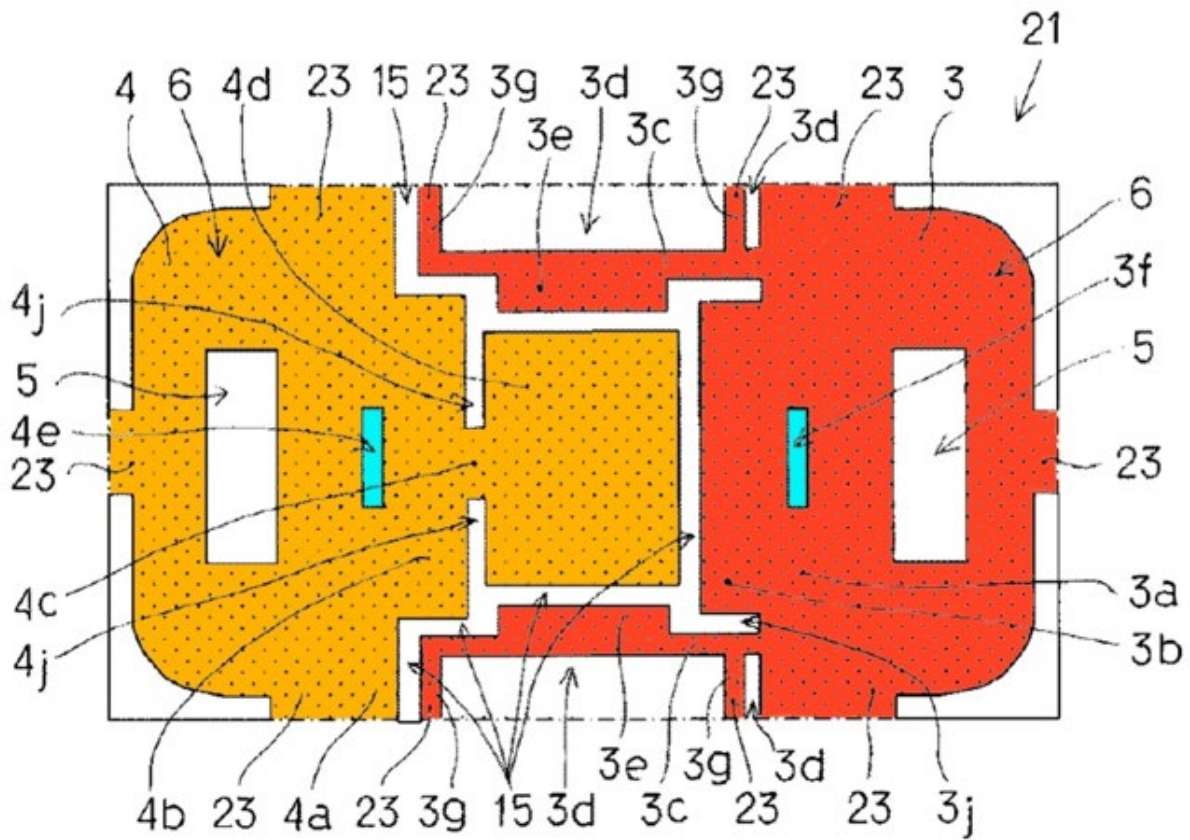
EX1007, [0095].

231. Additional disclosures reinforce this teaching. For example, EX1007, [0019] describes that “[t]he electrode plate portions of the **first** and **second electrode plates** located within the **encapsulant** are provided with **through holes** penetrating the **electrode plates**, and the **through holes** are filled with a **resin** that forms the **encapsulant**.”). *See also* EX1007, [Means for solving the problems], [0030], [0041], [0066], [0068], [0072], [0086], [0095], Claim 6, Claim 23. The **through holes 3f, 4e** form **resin-holding components** along the top and bottom sides of each of the **electrode plate 3** and the **electrode plate 4**.





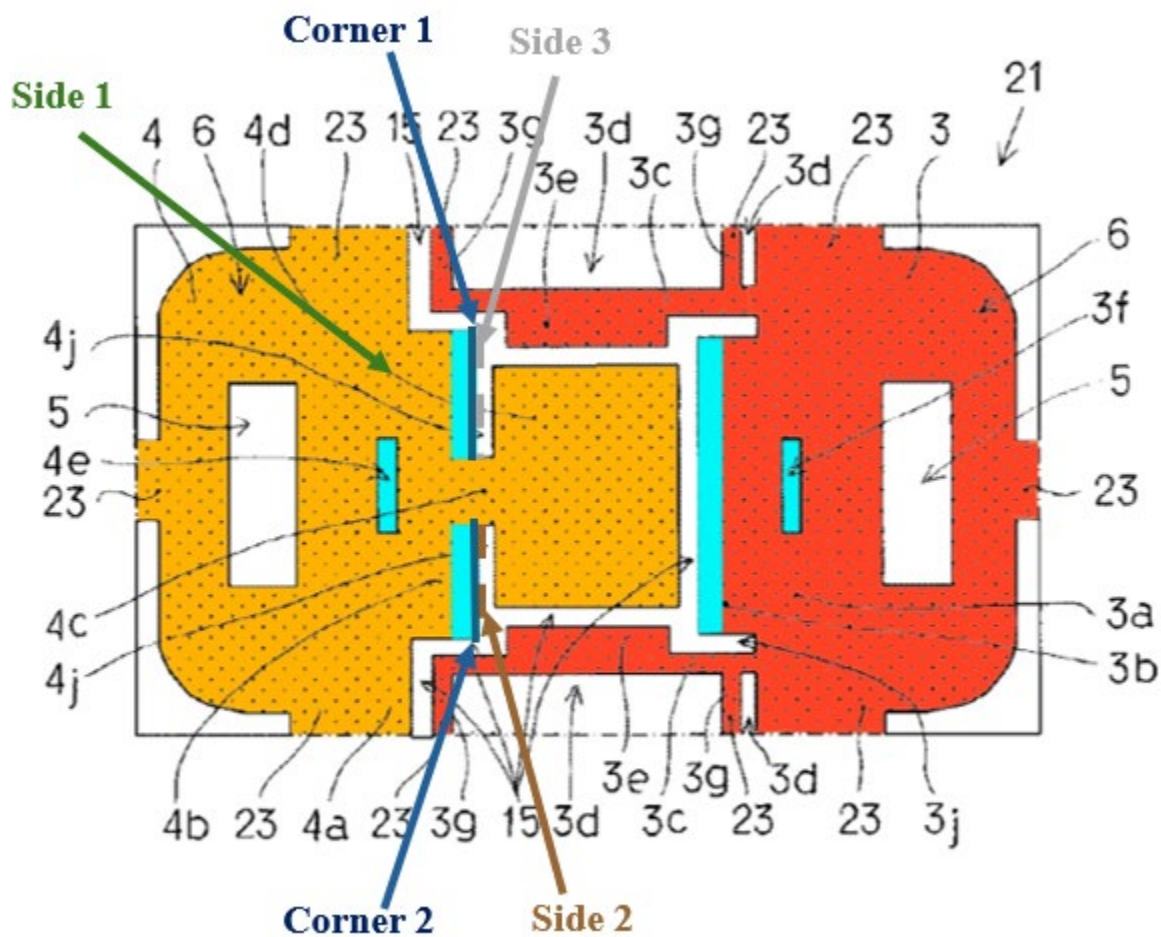
EX1007, Fig. 2.



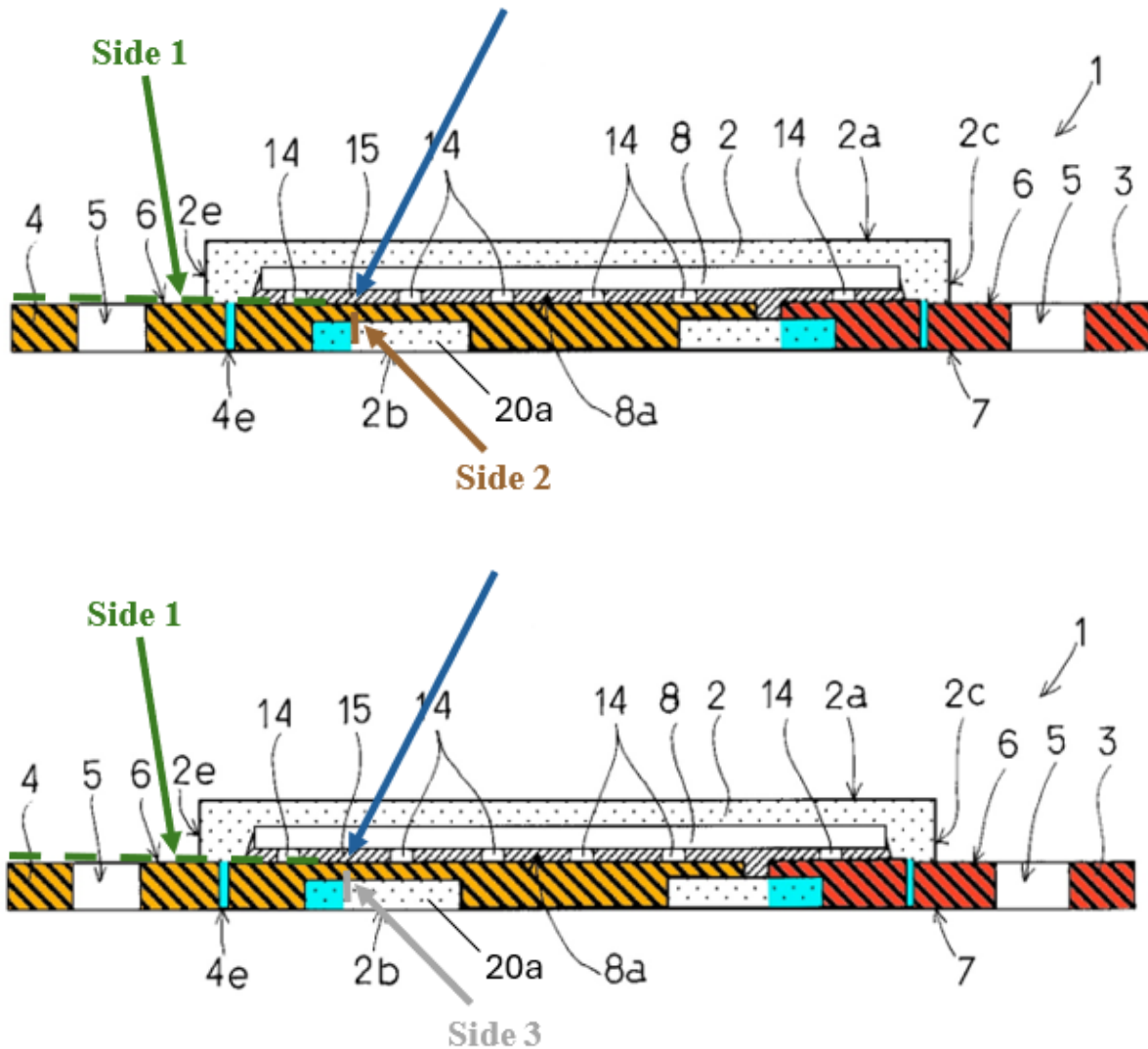
EX1007, Fig. 7.

232. Additionally, Takasaki discloses that the **resin-holding components**, that is, the **through-hole 4e** and the **opening 20a**, are “separated from each other at **corners** of the adjacent sides.” This is illustrated in, for example, Figures 2 and 7 of Takasaki.

233. In particular, Takasaki describes that the **through-hole 4e** is positioned along the **upper side** (“**Side 1**”) of the **second electrode plate 4**. This **upper side** is adjacent to two vertical sides (**vertical “Side 2”** and **vertical “Side 3”**), each of which includes a channel-like **resin-holding component**. Takasaki additionally discloses that the **through-hole** remains separated from the channel-like **resin-holding components** at the **corners** where **upper Side 1** meets **vertical Side 2** and **vertical Side 3**, respectively. This structural arrangement ensures that the through-hole and channel-like features do not merge, maintaining distinct resin-retention areas.



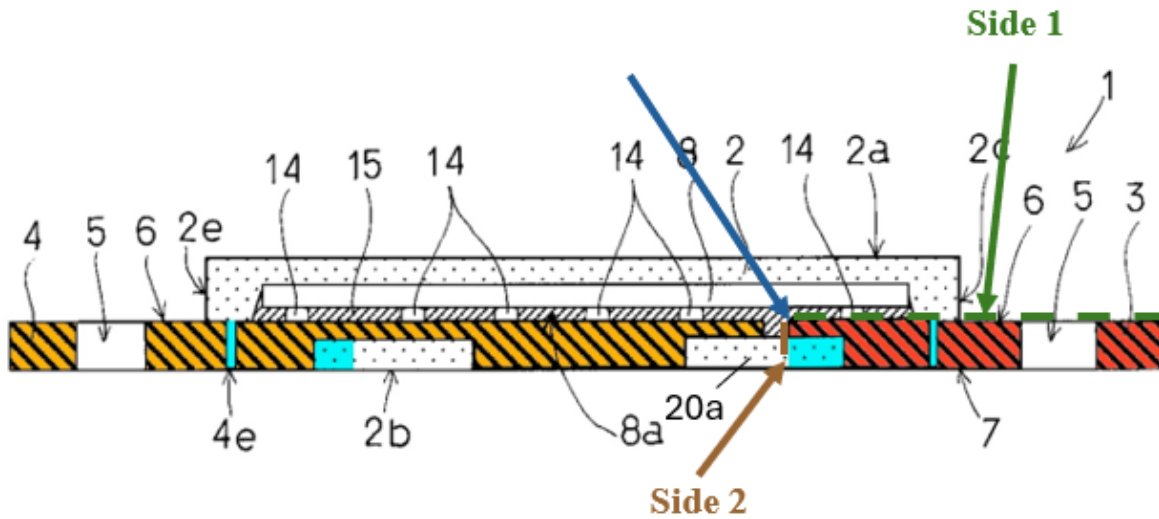
EX1007, Fig. 7.



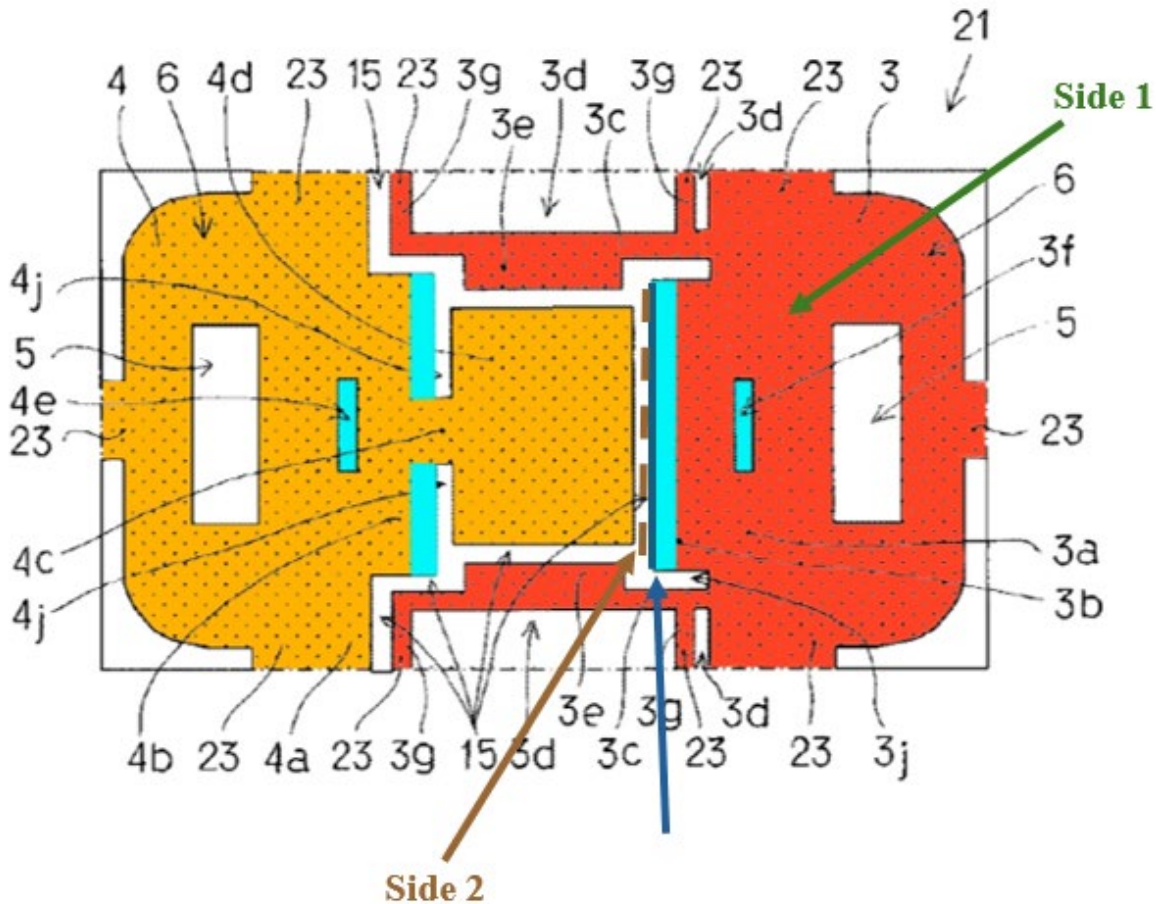
EX1007, Fig. 2 (label added indicating 20a).

234. Takasaki further discloses that the **through hole 3f** is disposed along the **upper Side 1** of the **first electrode plate 3**. As shown in Figures 2 and 7, the **through hole 3f** is placed near the boundary of the electrode plate. Additionally, Takasaki describes that along the **upper Side 1** of the **first electrode plate 3** is

adjacent to **vertical Side 2** of the **first electrode plate 3**. And a channel-like **resin-holding component** is disposed along this **vertical Side 2**.



EX1007, Fig. 2 (label added indicating 20a).



EX1007, Fig. 7.

### 3. Dependent Claims 2 and 3

- i. [2] The LED package of claim 1, wherein the **resin-holding components** comprise at least one **hole**.
- ii. [3] The LED package of claim 2, wherein the **hole** is filled with the **resin** to increase the bonding force between the resin and the lead frames.

235. Takasaki teaches [2] and [3].

236. Takasaki teaches that “the **electrode plates 3, 4** are formed with the **through holes 3f, 4e**.” EX1007, [0073]. As shown in Figures 1, 2, and 7, these

through-holes are integrated into the electrode plates to facilitate resin retention within the encapsulant.

As described above, the electrode plates 3, 4 are formed with the through holes 3f, 4e, the medium width portion 3b, the strip portion 3c, the recessed portion 3d, the protruding portion 3e, the medium width portion 4b, the narrow portion 4c, and the narrow width portion 4d, as well as the openings 17 and the narrow grooves 3j, 4j. As a result, the facing portions between the peripheral edges of the first electrode plate 3 and the second electrode plate 4 have a complex interlocking structure. In addition, since the resin forming the encapsulant 2 fills the interlocking spaces, the contact area between the electrode plates 3, 4 and the resin is increased, and the interlocking structure is enlarged, thereby improving the adhesive strength between the encapsulant 2 and the electrode plates 3, 4. The adhesive strength between the encapsulant 2 and the electrode plates 3, 4 can be further increased by thinning a portion of the electrode plates 3, 4 and filling the thinned space with resin.

EX1007, [0073].

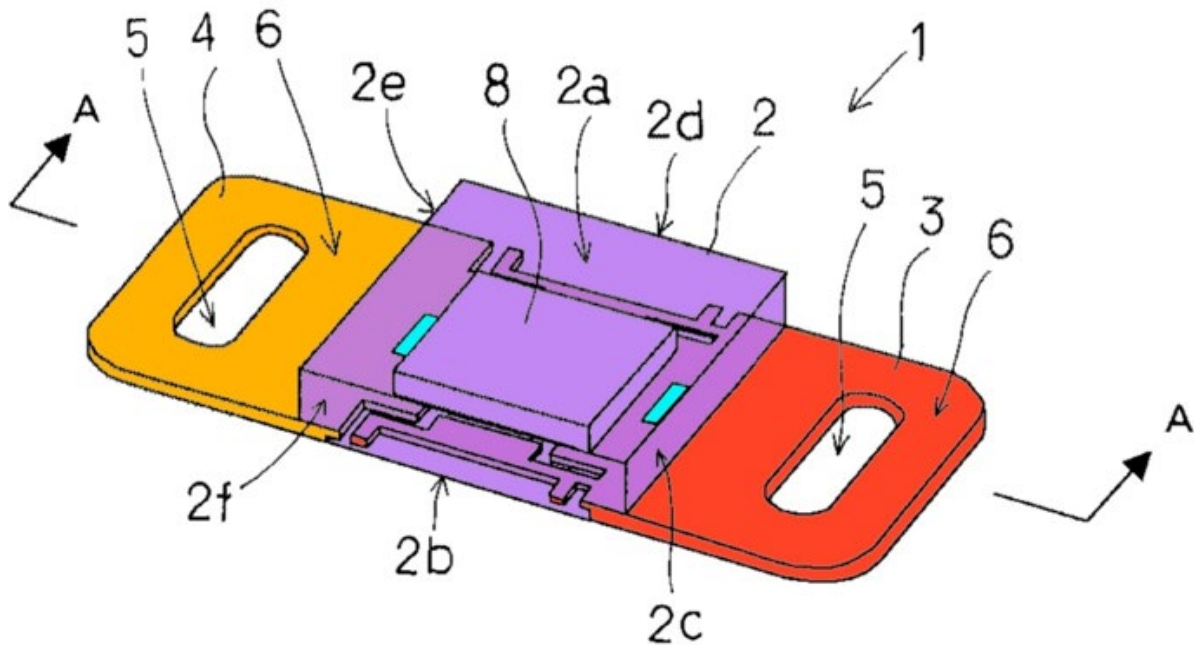
237. Takasaki further explains that in the resin-filled through-holes function to mechanically secure the electrode plates within the encapsulant. See, EX1007, [0095] (“In the electrode plate portions of the **first** and **second electrode plates 3, 4** covered by the **encapsulant 2**, the **through holes (through holes 3f, 4e)** penetrating the electrode plates are filled with **resin** that forms the **encapsulant 2**, so that the **electrode plates** are *held well* by the **encapsulant 2**, the **electrode plates** are *less likely to peel off* from the **encapsulant 2**, and the reliability of the sealing is improved.” See also, EX1007, [0019] where Takasaki provides a similar disclosure

(“The electrode plate portions of the **first** and **second electrode plates** located within the **encapsulant** are provided with **through holes** penetrating the **electrode plates**, and the **through holes** are filled with a **resin** that forms the **encapsulant**.”).

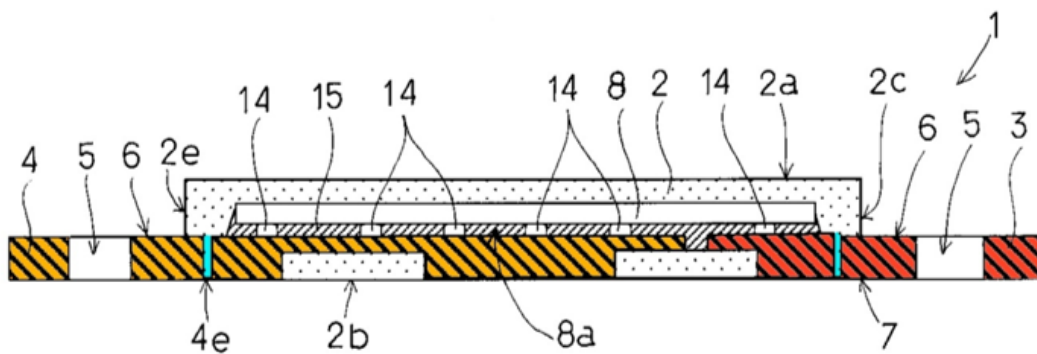
(D) The electrode plate portions of the first and second electrode plates located within the encapsulant are provided with through holes penetrating the electrode plates, and the through holes are filled with a resin that forms the encapsulant.

EX1007, [0019].

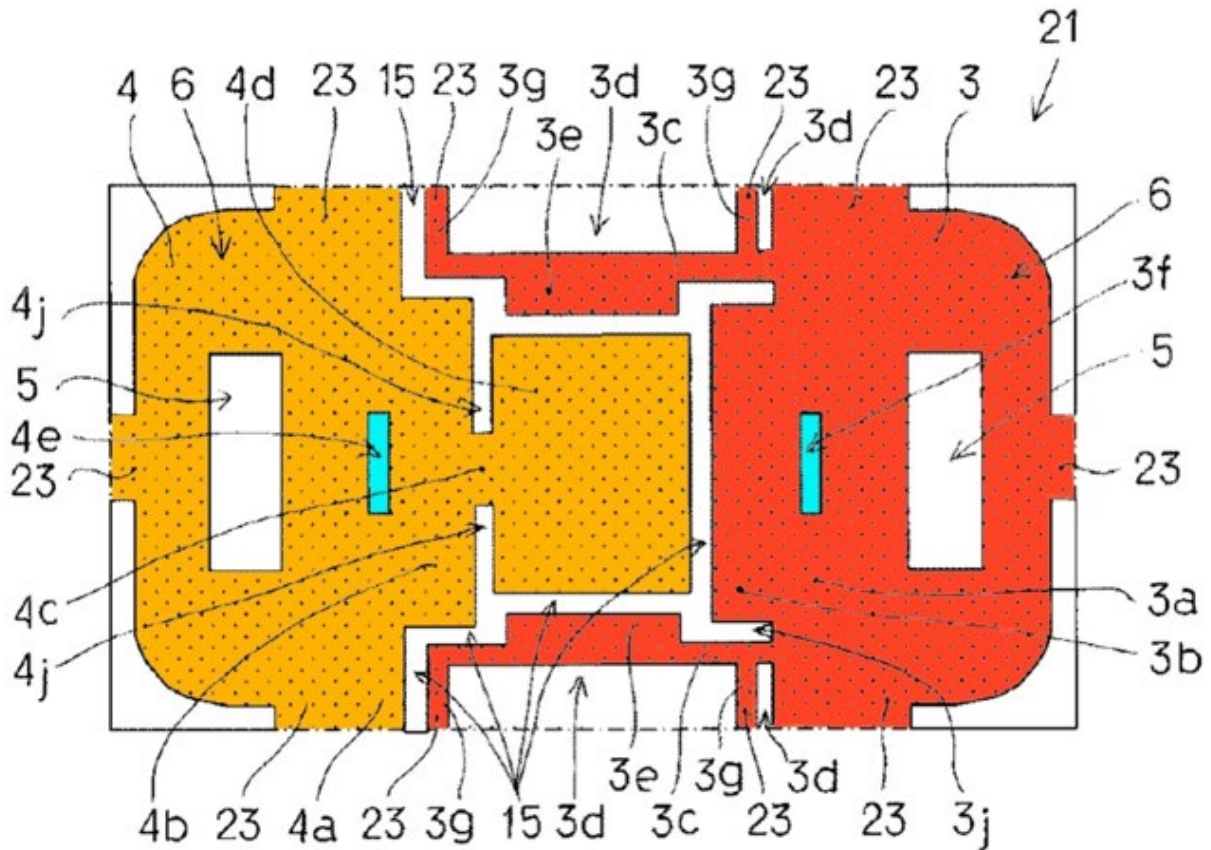
238. *See also* EX1007, [Means for solving the problems], [0030], [0041], [0066], [0068], [0072], [0086], [0095], Claim 6, Claim 23.



EX1007, Fig. 1.



EX1007, Fig. 2.

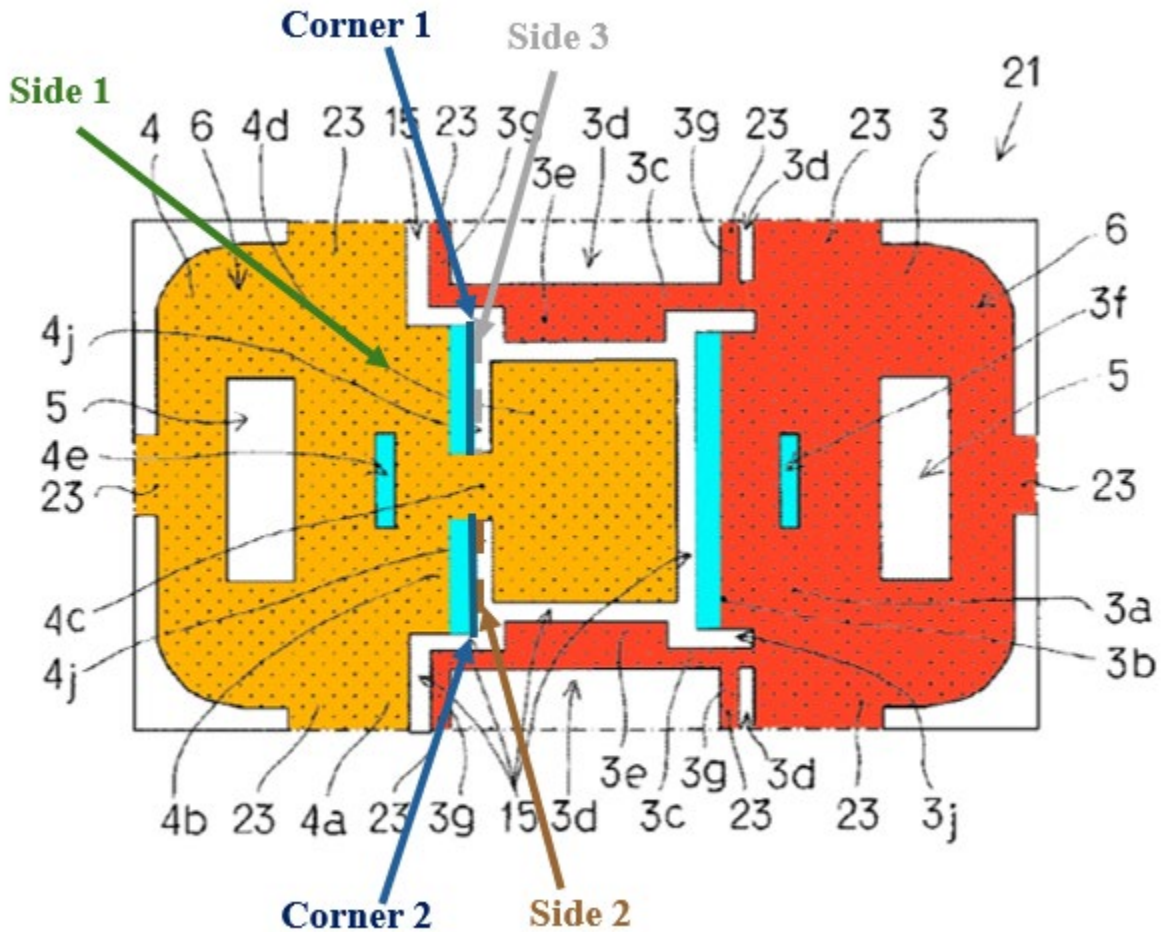


EX1007, Fig. 7.

**4. Dependent Claim 4**

- i. [4] The LED package of claim 1, wherein the **resin-holding components** are disposed on three sides of at least one of the **first** and **second lead frames**.

239. Takasaki teaches [4]. In particular, as is illustrated in figure 7, there are **resin-holding components** disposed along three (3) sides of the **electrode plate 4**.



EX1007, Fig. 7.

## IX. Conclusion

240. Accordingly, it is my opinion that claims 1-4, and 6 of the '913 Patent are unpatentable.

## X. Availability for Cross-Examination

241. In signing this declaration, I acknowledge that this declaration will be filed before the Patent Trial and Appeal Board of the United States and Patent Office

as evidence for a case. I also acknowledge that I may be subject to cross-examination in that case and that cross examination will occur in the United States. If I am required to submit to cross-examination, I will appear for cross-examination within the United States during the time allotted for cross-examination.

**XI. Right to Supplement**

242. I reserve the right to supplement my opinions in the future to consider any new information as it becomes available to me and to respond to any arguments that the Patent Owner may raise.

**XII. Jurat**

243. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

**CLAIMS AT ISSUE**

**Claim 1**

[1Pre] A light emitting diode (LED) package, comprising:

[1A] a first lead frame and a second lead frame separated from each other;

[1B] an LED chip disposed on the first lead frame and electrically connected with second lead frame; and

[1C] a resin covering at least portions of surfaces of the first and second lead frames, wherein:

[1D] at least one of the first and second lead frames comprises resin-holding components disposed along adjacent sides of one of the first and second lead frames, the resin-holding components being separated from each other at corners of the adjacent sides; and:

[1E] the resin-holding components are disposed on two adjacent sides of each of the first lead frame and the second lead frame.

**Claim 2**

[2] The LED package of claim 1, where the resin-holding components comprise at least one hole.

**Claim 3**

[3] The LED package of claim 2, wherein the hole is filled with the resin to increase the bonding force between the resin and the lead frames.

Claim 4

[4] The LED package of claim 1, wherein the resin-holding components are disposed on three sides of at least one of the first and second lead frames.

Claim 6

[6Pre] A light emitting diode (LED) package, comprising:

[6A] a first lead frame and a second lead frame separated from each other;

[6B] an LED chip disposed on the first lead frame and electrically connected with second lead frame; and

[6C] a resin covering at least portions of surfaces of the first and second lead frames, wherein

[6D] at least one of the first and second lead frames comprises resin-holding components disposed along adjacent sides of one of the first and second lead frames, the resin-holding components being separated from each other at corners of the adjacent sides; and

[6E] the first and the second lead frames comprise opposing sides facing each other, and the resin-holding components are disposed on the opposing sides.

# APPENDIX A

# Ioannis Kymissis

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## EDUCATION

Ph.D. in Electrical Engineering and Computer Science, May 2003  
Massachusetts Institute of Technology, Cambridge, MA  
Thesis title: Field Emission from Organic Materials  
Advisor: Prof. Akintunde I. Akinwande

M.Eng. in Electrical Engineering and Computer Science, May 1999  
Massachusetts Institute of Technology, Cambridge, MA  
Thesis title: Morphology and Performance in Pentacene  
Advisor: Prof. Akintunde I. Akinwande  
Co op with IBM Research Laboratories, Yorktown Heights, NY

S.B. in Electrical Engineering and Computer Science, May 1998  
Massachusetts Institute of Technology, Cambridge, MA

## EMPLOYMENT

**Vice Dean of Infrastructure and  
Innovation  
Columbia Engineering**

**Columbia University  
New York, NY  
2024 present**

**Department Chair  
Electrical Engineering**

**Columbia University  
New York, NY  
2020 2024**

**Kenneth Brayer Professor  
Electrical Engineering**

**Columbia University  
New York, NY  
2006 present**

PI, the Columbia Laboratory for Unconventional Electronics (CLUE).

**Technical consultant/Senior engineer**

**QDVision, Inc. (Now Samsung  
Electronics)  
Watertown, MA  
2005 2006**

Assisted the technical launch of the company. Built out facilities, interviewed, hired, and trained initial staff, developed the core processes and demonstration vehicles for the company. Acquired by Samsung Electronics, the company's technology is part of the QLED display platform.

**Postdoctoral Associate**  
**Laboratory for Organic Optics and**  
**Electronics**

**MIT**  
**Cambridge, MA**  
**2003 2006**

Advisor: Vladimir Bulovic.

**Research Assistant**  
**Microsystems Technology**  
**Laboratory**

**MIT**  
**Cambridge, MA**  
**1999 2003**

Thesis: Field Emission from Organic Semiconductors. Advisor: Tayo Akinwande

**Summer Intern**  
**IBM Research, Tokyo Research Lab**

**Yamato, Japan**  
**Summer 1999**

Developed a new characterization technique for analyzing ion density in liquid crystals and susceptibility of display alignment materials to charging and PDLC display systems. Advisor: Yoichi Taira

**Co-op Student**  
**IBM Research, T. J. Watson**  
**Research Lab**

**Yorktown Heights, NY**  
**1996-1999**

Led several aspects of the organic field effect transistor effort, most notably developing a photolithographic process for fabricating transistors and investigating the role of semiconductor crystallization on macroscopic performance parameters. Also worked on a program on screen printable high K dielectrics and novel lead free soldering systems. (Three assignments, Summer 1996, 1997, June 1998 January 1999). Advisors: Christos Dimitrakopoulos and Sampath Purushothaman

#### AWARDS

2022 Fellow, Optica  
2021 Fellow, IEEE  
2021 Outstanding Volunteer Award 2021 by IEEE Kolkata Section  
2019 Kenneth Brayer Professorship, Columbia University  
2019 IEEE EDS Distinguished Lecturer  
2018 40 under 40, Greek America Foundation  
2018 Fellow, Society for Information Display  
2017 Architizer A+ Award (Radiator Labs)  
2016 Finalist, Verizon Powerful Answers Award (Chromotion)  
2015 Winner, Verizon Powerful Answers Award (Radiator Labs)  
2014 National Academy of Engineering, Frontiers of Engineering Education Meeting Attendee  
2014 National Academy of Engineering, Indo American Frontiers of Science Meeting Attendee  
2014 Popular Science, Invention of the Year (Radiator Labs)  
2013 IBM faculty award  
2012 Interdigital Innovation Challenge, first prize  
2012 MIT/USDOE Clean Energy Prize, first prize  
2011 Ocean Optics Blue Ocean Award  
2011 Kim Award for Undergraduate Involvement  
2010 IBM Faculty award  
2009 Vodafone Americas Foundation Wireless Innovation Award  
2008 Google faculty award

|                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|--------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                | 2007 NSF CAREER award<br>2002 IVMC Shoulders Gray Spindt award<br>1998 2002 IBM Fellowship<br>2002 IBM Research First Plateau<br>2002 IBM Outstanding Technical Achievement Award<br>2000 2002 IBM Invention Achievement Award<br>1997 Tau Beta Pi, Eta Kappa Nu<br>1994 1998 National Merit Scholar                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| BEST<br>PAPER/POSTER<br>AWARDS | 2023 CMOC Best poster award<br>2021 IDW MEET Best Paper Award<br>2020 IEEE Xplore Highlight Paper<br>2018 International Symposium on Wearable Computers, 20 Year Impact Award<br>2018 IDW Distinguished Paper Award<br>2018 CMOC Best poster award<br>2015 IDW Distinguished Paper Award<br>2015 NYC Media Lab Best Demo award<br>2014 FlexTech Alliance, second place best poster<br>2014 Global Interposer Technology Conference, second place best poster<br>2013 IGERT workshop on Energy, Transportation, and Water Infrastructure 3rd place poster<br>2012 MRS Fall Meeting Best Poster finalist<br>2011 ACM SenSys'11 Best Student Demo Award<br>2011 IEEE Communications Society Award, Best Paper<br>2002 IEEE Electron Device Society Paul Rappaport Award                                                                                                                   |
| ADVISORY<br>POSITIONS          | Tangible Co founder and technical advisor. BOD member.<br>Solchroma SAB member<br>Chromation Co founder and CTO. BOD member.<br>Radiator Labs Co founder and technical advisor. BOD member.<br>Lumiode Co founder and interim CEO. BOD member.<br>Lelantos Co founder and technical advisor. BOD member.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| BOOK / BOOK<br>CHAPTERS        | Ioannis Kymissis (monograph). <i>Organic Field Effect Transistors: Theory, Fabrication and Characterization</i> Springer, New York, 2009.<br><br>Lamport ZA, Cavallari MR, Kymissis I. Large Area Flexible Organic Field effect Transistor Fabrication. Flexible Flat Panel Displays. 2023 Feb 14:47-66.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| PUBLICATIONS                   | <a href="https://scholar.google.com/citations?hl=en&amp;user=WcfE80C7d5MC&amp;view_op=list_works&amp;sortby=pubdate">https://scholar.google.com/citations?hl=en&amp;user=WcfE80C7d5MC&amp;view_op=list_works&amp;sortby=pubdate</a><br><br>154. Bae, Jisuk; Park, Soyoung; Jung, Haeji; Ko, Eun Hye; Kymissis, Ioannis; Kim, Chang Hyun; Polymer field effect transistors with inkjet printed silver electrodes: from device fabrication to circuit simulation Journal of Materials Science: Materials in Electronics 35 2 1 11 2024<br><br>153. Zhang, John Z; Graf, Lukas; Banerjee, Annesya; Yeiser, Aaron; McHugh, Christopher I; Kymissis, Ioannis; Lang, Jeffrey H; Olson, Elizabeth S; Nakajima, Hideko Heidi; An Implantable Piezofilm Middle Ear Microphone: Performance in Human Cadaveric Temporal Bones Journal of the Association for Research in Otolaryngology 1 9 2024 |

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#### SHORT COURSES

- (invited) SID Short course on MicroLED (Aug 2021)
- (invited) SID Seminar on MicroLED (Aug 2020)
- (invited, short course) SID Short Course on MicroLED, San Jose, CA, May 2019
- (invited) University of Bologna Summer School on Physical Sensing and processing; July 2019
- IEEE Expert Now online short course on organic field effect transistors (2006)

#### CONFERENCE PRESENTATIONS/ POSTERS/ DEMOS

- (invited) IDW 2022
- (invited, plenary) IEEE ECTC
- (invited) MRS Spring 2022
- (invited) ICDT invited presentation (TBD) (June 2021)
- (Invited, plenary) IEEE EDS Mini Colloquium on Photonics and Photovoltaics (Spain chapter) June 2020
- (Invited, plenary) IEEE EDS Brazil Chapter Seminar, Electronics on Anything, August 2020
- (invited, plenary) SID LA one day conference on Advanced Displays, Los Angeles, CA; February 2020
- (invited, plenary) MicroLED Display Summit, Nanjing China, December 2019

(invited, plenary) IEEE Frontiers In New Emerging Technology 2019 (FINE TECH) ; August 2019

(invited, plenary) IEEE EDSSC, Xi'an China, June 2019

Characterizing Image Retention for HDR OLED Displays SID Display Week 2020

Micro LED Defect Analysis via Photoluminescent and Cathodoluminescent Imaging, SID Display Week 2020

A brief survey of MicroLED Technologies, SID Display Week 2020

Bahamonde JA, Krishnaswamy H, Kymissis I. A Tunable Surface Acoustic Wave Device on Zinc Oxide via acoustoelectric interaction with AlGaIn/GaN 2DEG. InConference digest 2019 Jun.

A non reciprocal surface acoustic wave filter based on asymmetrical delay lines and parametric interactions MEMS 2020, Vancouver, Canada.

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(Invited) IDW 2018, Nagoya, Japan

(Invited, plenary) INMS 2018, Hamamatsu, Japan

(invited, plenary) Second annual workshop on MicroLED, Shenzhen China

Diagnosing SLE Arthritis with Dynamic Diffuse Optical Spectroscopy 2018 ACR/ARHP Annual Meeting

Kim Y, Marone A, Thompson SM, Sowah JN, Shulevitz HJ, Kim HK, Kymissis I, Hielscher AH. Conformable, Wearable and Scalable Imaging Bands for Assessing Joints Diseases. InMicroscopy Histopathology and Analytics 2018 Apr 3 (pp. JTh3A 34). Optical Society of America.

Colon Berrios, Aida R., Hassan Edrees, Daniel De Godoy, Peter Kinget, and Ioannis

Kymissis. "Die level processing for 3 D monolithic integration of piezoelectric MEMS on CMOS." In SOI 3D Subthreshold Microelectronics Technology Unified Conference (S3S), 2017 IEEE, pp. 1-3. IEEE, 2017.

Liang, W., Alexandrou, K., Klebanov, M., Kuo, C. C., Kymissis, I., Sundaram, K. B., Liou, J. J. (2017, July). Characterization of ESD protection devices under total ionizing dose irradiation. In Physical and Failure Analysis of Integrated Circuits (IPFA), 2017 IEEE 24th International Symposium on the (pp. 1-4). IEEE.

(Invited) Integrated Light Management as a Path to Miniaturizing Spectrometers Na dia K. Pervez, Tanya C. Garza, Michael J. Gazes, James I. Scholtz, Mark F. Comerford, and Ioannis Kymissis Imaging and Applied Optics 2017 (3D, AIO, COSI, IS, MATH, pcAOP) OSA Technical Digest (online) (Optical Society of America, 2017), paper ATh2A.3

(invited) National Research Center, Athens, Greece

(Invited) 2018 Workshop on smell sensing, AIT Tullin, Austria

(invited) ICDM 2018, "Surface treatment for OFETs" Guangzhou, China

(short course) ICDM 2018, "MicroLEDs" Guangzhou, China

(Invited) CMOC 2018, New Haven, CT

(invited) IWPSD, "X ray analysis of OFETs" New Delhi, India

(short course) IWPSD, "Quantum Dots in Displays" New Delhi, India

(Keynote, panelist) Boston HubWeek 2017

(Invited) SID Annual Symposium 2017

(Invited, plenary speaker) 2017 Hai'an Workshop on Microelectronics, Hai'an China

Colon Berrios AR, Edrees H, McGinn C, Cavallari MR, Kinget P, Kymissis I. CMOS integrated ZnO thin film bulk acoustic resonator with Si<sub>3</sub>N<sub>4</sub> susceptor layer for improved IR sensitivity. Device Research Conference (DRC), 2017

Bahamonde JA, Colon AR, Krishnaswamy H, Kymissis I. Acoustoelectric amplification of surface acoustic waves on ZnO deposited on AlGaN/GaN Epi. Device Research Conference (DRC), 2017

(invited) NYC Media Lab summit 2016, presentation and workshop

(Invited) CMOC 2016, New Haven, CT

Youngwan Kim, Christopher Choi, Theodore H Schwartz, Hongtao Ma, Ioannis Kymissis "Non display MicroLED devices" 2016 SID IZone demonstration, San Francisco, CA, May 2016.

A Masurkar, I Kymissis. Comparison of top and bottom contact pentacene field effect transistors using photocurrent microscopy. Device Research Conference (DRC), 2016

Radiation hardened graphene field effect transistors. K Alexandrou, A Masurkar, H Edrees, JF Wishart, Y Hao, N Petrone, J Hone, I Kymissis. Device Research Conference (DRC), 2016

(Invited) Bioelectronics and More 2016, Wiener Neustadt, Austria.

Youngwan Kim, Christopher Choi, En Chen Chen, Andy GS Daniel, Amrita Masurkar, Theodore H Schwartz, Hongtao Ma, Ioannis Kymissis "An ultra thin implantable system for cerebral blood volume monitoring using flexible OLED and OPD," 2015 IEEE International Electron Devices Meeting (IEDM), Washington, DC, 2015, pp. 29.6.1-26.6.4.

Hurst, Adam M; Chenet, Daniel; van der Zande, Arend; Kymissis, Ioannis; Hone, James; A molybdenum disulfide piezoelectric strain gauge Nanotechnology (IEEE NANO), 2015 IEEE 15th International Conference on 1122-1125 2015 IEEE

Shyuan Yang, Ioannis Kymissis. Large scale temperature monitoring system for detection of potential ebola patient Proceedings of the 8th ACM International Conference on Pervasive Technologies Related to Assistive Environments, 7/21/15

(Invited Paper) Brian R Tull, Zeynep Basaran, Dafna Gidony, Alexander B Limanov, James S Im, Ioannis Kymissis, Vincent W Lee. High Brightness, Emissive Microdisplay by Integration of III V LEDs with Thin Film Silicon Transistors. SID Symposium Digest of Technical Papers 2015/6/1

Fabio Carta, Htay Hlaing, Hassan Edrees, Shyuan Yang, Mingoo Seok, Ioannis Kymissis. Co development of complementary technology and modified CPL family for organic digital integrated circuits. MRS Proceedings, 2015 Volume 1795 19-25

Fall MRS, Boston, MA 2015.

(invited) SPIE Optics+Photonics, San Diego, CA 2015.

(invited) Fall MRS, Boston, MA 2014.

(invited) "An Implantable System for Brain Blood Flow Monitoring Using Flexible OLEDs and OPDs." Ioannis (John) Kymissis, Amrita Masurkar, Youngwan (Willis) Kim, En Chen (Patrick) Chen, Hongtao Ma, Theodore Schwartz. USAMC 17th Biannual Bioscience review, Baltimore MD. 2014.

"BEOL Integration with excimer laser recrystallization" Fabio Carta, Ioannis Kymissis. GIT 2013 (best poster award, 2nd place)

"A printable sensor for ammonia vapors." Kalpana, Shyuan Yang, Ioannis Kymissis, Howard Katz. FlexTech 2014, Phoenix, AZ.

"Metacapacitors: Printed Capacitors for High Efficiency Power Supplies." Shyuan Yang, Ioannis Kymissis. FlexTech 2014, Phoenix, AZ. (best poster award, 2nd place)

"An Implantable System for Brain Blood Flow Monitoring Using Flexible OLEDs and OPDs." FlexTech 2014, Phoenix, AZ.

(invited) "Thin Film Electronics for Mechanical Sensing and Actuation" Ioannis Kymissis. IEEE 2014 Packaging Symposium, Binghamton, NY

“Printable, High Performance Nanoparticle/Polymer Composite Capacitors” Shyuan Yang, Barry Van Tassell, Shuangyi Liu, Eli S. Leland, Daniel A. Steingart, Stephen O’Brien, Ioannis Kymissis. Fall MRS, December 2013. Boston MA

“Low Temperature Spray Deposition of Multilayer Polymer Ceramic Composite Capacitors” Barry Van Tassell, Paul Chando, Shyuan Yang, Shuangyi Liu, Limin Huang, Stephen O’Brien, Ioannis Kymissis, Daniel A Steingart. Fall MRS, December 2013. Boston MA

“Printable Ammonia Sensor Based on Organic Field Effect Transistor” Kalpana Besar, Ana Maria Rule, Patrick N. Breyse, Ioannis John Kymissis, Howard E Katz. Fall MRS, December 2013. Boston MA

“Electrophoretic Deposition of Solution Phase Ligand Exchanged Quantum Dots and Their Application in Optoelectronic Devices” Htay Hlaing, Seung Whan Lee, Irving P Herman, Ioannis Kymissis. Fall MRS, December 2013. Boston MA

“Analysis of Optimized Photovoltaic Devices Using Impedance Spectroscopy” Jonathan Beck, James Basham, David Gundlach, Ioannis Kymissis. Fall MRS, December 2013. Boston MA

“Investigation of Photocurrent and Photogeneration in Organic Field Effect Transistors” Amrita Masurkar, Ioannis Kymissis. Fall MRS, December 2013. Boston MA

“Monolithic versus Three Terminal Tandem Photovoltaics: A Detailed Balance Comparison” Octavi Escala Semonin, Paul A George, Robert A Barton, Ioannis Kymissis. Fall MRS, December 2013. Boston MA

“Graphene Electrodes for Quantum Dot Solar Cells” Robert A Barton, Octavi E Semonin, Joshua Choi, Nicholas Petrone, Yuanda Gao, James Hone, Jonathan Owen, Ioannis Kymissis. Fall MRS, December 2013. Boston MA

“Large Area CVD Graphene as Molecular Template and Transparent Electrode for Organic Solar Cells” Htay Hlaing<sup>1,2</sup>, Rob Barton<sup>1</sup>, Theanne Schiros<sup>1</sup>, Nicholas Petrone<sup>2</sup>, James Hone<sup>1,2</sup>, Ioannis Kymissis, Fall MRS, December 2013. Boston, MA.

“An implantable PVDF microphone for a totally implantable cochlear implant” Andy Zhang, Elizabeth Olson, Ioannis Kymissis. SPIE Optics+Photonics, August 2013. San Diego, CA.

“Solution Processed Organic Transistors with Chemically Modified Copper Electrodes.” Chang Hyun Kim, Htay Hlaing, Fabio Carta, Yvan Bonnassieux, Gilles Horowitz, and Ioannis Kymissis. FPI 11. June 2 11 2013, Aquitaine, France.

“Integrated CMOS Quantitative Polymerase Chain Reaction Lab on Chip,” Haig Norian, Ioannis Kymissis, Kenneth Shepard. 2013 Symposium on VLSI Circuits, to appear June 2013.

“Amorphous Silicon graphene anodes for lithium ion batteries”, Filippas Farmakis, Kostas Alexandrou, Costas Elmasides, Ioannis Kymissis and Nikolaos Georgoulas, SPIE Grenoble to appear April 2013

“Demo: An adaptive multihop network testbed for energy harvesting active networked tags (EnHANTS),” R. Margolies, L. Pena, K. Kim, Y. Kim, M.Wang, M. Gorlatova, J.

Sarik, J. Zhu, P. Kinget, I. Kymissis, and G. Zussman, in Proc. IEEE INFOCOM'13, Apr. 2013.

"Project based learning within a large scale interdisciplinary research effort," M. Gorlatova, J. Sarik, I. Kymissis, and G. Zussman, in Proc. ITiCSE 2013

"Printable, flexible, high performance capacitors for power circuit application," S. Yang, B. Van Tassell, P. Chando, C. Le, S. Liu, E. S. Leland, Conference D. A. Steingart, S. O'Brien, P. R. Kinget, I. Kymissis, , FlexTech Alliance, January 2013.

"Asymmetric Leakage in (Ba, Sr)TiO<sub>3</sub> Nano Particle/Parylene C Composite Capacitors," S. Yang, B. R. Tull, N. K. Pervez, L. Huang, E. S. Leland, D. Steingart, S. O'Brien, I. Kymissis, MRS Conference, Best Poster Award Nominee, November 2012.

"Metacapacitor: Flexible, low cost, high performance capacitor for power electronics" S. Yang, B. Van Tassell, P. Chando, C. Le, S. Liu, E. S. Leland, D. A. Steingart, S. O'Brien, P. R. Kinget, I. Kymissis, NY Best Conference, November 2010.

J. Sarik, C. Li, and I. Kymissis, "Fabricating electronics with rapid prototyping tools," in Proc. 6th TEI, Jan. 2012.

"Use of Subwavelength Structures to Improve Optics and Transport in Organic Photovoltaics." J. H. Beck, B. Ray, C. Tsai, R. R. Grote, R. M. Osgood, D. Englund, C. T. Black, M. A. Alam, I. Kymissis. MRS Fall 2012, Boston, MA.

"Electrostrictor with Monolithically Integrated CMOS TFT Control." Fabio Carta, Yu Jen Hsu, John Sarik, Ioannis Kymissis. CIMTEC 2012. June 10 14 2012, Montecatini Terme, Italy.

(invited) "Energy Harvesting Active Network Tags (EnHANTs)" Ioannis Kymissis. IdTechEx Energy Harvesting 2012.

"Active matrix PVDF array for thermal imaging and acoustic signal processing applications." Yu Jen Hsu, Shyuan Yang, Nadia Pervez, Ioannis Kymissis. SPIE Optics+Photonics 2012.

"High throughput pH and ion sensing via CMOS FGFET arrays" Alok Prabu, Shyuan Yang, Ioannis Kymissis, Kalle Levon. SPIE Optics+Photonics 2012.

"Fabrication and Electrochemical Characterization of Multiplexed Electrode System for DNA Biosensing. " Zeynep Basaran, Janet Lee, Marisa Buzzeo, Ioannis Kymissis. SPIE Optics+Photonics 2012.

"Evaluating Photovoltaic Performance Indoors," Y. Afsar, J. Sarik, M. Gorlatova, G. Zussman, I. Kymissis, in Proc. 2012 IEEE Photovoltaic Specialist Conference, Austin, TX, June 2012.

(Invited) "An Active Matrix Microphone." Ioannis Kymissis, Y. Hsu. ISDRS 2011.

"Electrical readout of photochromic state." Hassan Edrees, Nadia Pervez, Ioannis Kymissis. SPIE Optics+Photonics 2011.

"Sequential Lateral Solidification of Silicon on Low K Dielectrics for 3D Integrated

Circuits,” V.W. Lee, G.S. Ganot, A.B. Limanov, J.S. Im, I. Kymissis. T5.20, Materials Research Society Fall Meeting 2011.

“Method for Efficient Droplet Extraction from Covered Droplet in Oil Electrowetting on Dielectric Devices.” Haig Norian, Ioannis Kymissis and Kenneth Shepard; MRS Fall Meeting 2011.

“Demo: prototyping UWB enabled enhants.” Jianxun Zhu, Gerald Stanje, Robert Margolies, Maria Gorlatova, John Sarik, Zainab Noorbhaiwala, Paul Miller, Marcin Szczodrak, Baradwaj Vigraham, Luca Carloni, Peter Kinget, Ioannis Kymissis, and Gil Zussman. In Proceedings of the 9th international conference on Mobile systems, applications, and services (MobiSys '11). ACM, New York, NY, USA, 387 388. DOI=10.1145/1999995.2000048

“Demo: Organic solar cell equipped energy harvesting active networked tag (EnHANT) prototypes” Gerald Stanje, Paul Miller, Jianxun Zhu, Alexander Smith, Olivia Winn, Robert Margolies, Maria Gorlatova, John Sarik, Marcin Szczodrak, Baradwaj Vigraham, Luca Carloni, Peter Kinget, Ioannis Kymissis, and Gil Zussman. In Proceedings of the 9th ACM Conference on Embedded Networked Sensor Systems (SenSys '11). ACM, New York, NY, USA

(Invited) “Photocurrent And Noise Analysis as Alternative Approaches to Understanding OFET Behavior,” Ioannis Kymissis. Organic Electronics Workshop 2011

“Building interactive systems using unconventional electronics” John Sarik, Ioannis Kymissis. TEI 2011. 10.1145/1935701.1935788

“A piezoelectric polymer based tone analyzer with integrated organic field effect transistors”, Yu Jen Hsu and Ioannis Kymissis. MRS Spring Meeting 2011.

“An active matrix arrayed microphone with acoustic bandwidth response”, Yu Jen Hsu and Ioannis Kymissis. Transducers 2011 Beijing.

“An active matrix arrayed microphone with acoustic bandwidth response”, Yu Jen Hsu and Ioannis Kymissis. SPIE Photonic Devices + Applications 2011.

(Invited) “Locally amplified sensors for large area systems.” MRS Spring, 2011

“Photovoltaic Device Performance Enhancement by Interfacial Decoration of Bulk Heterojunctions with Semiconducting Nanocrystals” Theodore Kramer, Ioannis Kymissis, and Irving Herman. APS March Meeting 2011.

(Invited) “Photocurrent And Noise Analysis as Alternative Approaches to Understanding OFET Behavior,” I. Kymissis, ICEL'10, Ann Arbor, MI. October 2010.

“Lab kits using the Arduino Prototyping Platform”. T3C. John Sarik and Ioannis Kymissis. ASEE/IEEE Frontiers in Education. Washington, DC October 2010

“A directly addressed monolithic LED array as a projection source,” Vincent W. Lee, Ioannis Kymissis, SPIE Optics+Photonics 2010, San Diego, CA, Aug 2010

“Strain field and magnetic field sensors with OLED indicators employing piezoelectric and magnetoresistive gated OFET,” Hsin Jung Lee, Shyuan Yang, Yu Jen Hsu, Ioannis Kymissis, SPIE Optics+Photonics 2010, San Diego, CA, Aug 2010

“Photonic crystal spectrometer,” Nadia K. Pervez, Warren Cheng, Zhang Jia, Marshall P. Cox, Hassan M. Edrees, Ioannis Kymissis, SPIE Optics+Photonics 2010, San Diego, CA, Aug 2010

“Weak 2D photonic crystals for outcoupling of multiple color bands,” Nadia K. Pervez, Warren Cheng, Chee Wei Wong, Ioannis Kymissis, SPIE Optics+Photonics 2010, San Diego, CA, Aug 2010

“Demo: Prototyping Energy Harvesting Active Networked Tags with MICA2 Motes,” Gorlatova M., Sharma T., Shrestha D., Xu E., Chen J., Skolnik A., Piao D., Kinget P., Kymissis I., Rubenstein D., Zussman G., IEEE Conference on Sensor, Mesh and Ad Hoc Communications and Networks (SECON), Boston, MA, June 2010

(invited) I. Kymissis. “Hybrid Integration using Organic Semiconductors” CMOC 2010, Storrs, CT.

Z. Jia, V.W. Lee, L. Floreano, A. Verdini, A. Cossaro, A. Morgante, I. Kymissis. “Direct observation of pentacene thiol interaction using x ray spectroscopy” II6.86, MRS Conference, Spring 2010

“Performance of graphene nanoelectromechanical resonators” Changyao Chen, Sami Rosenblatt Kirill Bolotin, William Kalb, Philip Kim, Ioannis Kymissis, Horst Stormer, Tony Heinz, James Hone. APS March Meeting, 2010

“Photonic Crystal Spectrometer” Nadia Pervez, Warren Cheng, Zhang Jia, Marshall Cox, Hassan Edrees, Ioannis Kymissis, APS March Meeting, 2010

“Direct observation of pentacene thiol interaction using x ray spectroscopy” Zhang Jia, Vincent Lee, Luca Floreano, Alberto Verdini, Albano Cossaro, Alberto Morgante, Ioannis Kymissis. APS March Meeting, 2010

“Personalizing your pixels” John Sarik, Ioannis Kymissis. 4th ACM International Conference on Tangible, Embedded, and Embodied Interaction *TEI* pp 353-356, Cambridge, MA. January 2010.

“NEMS applications of graphene” Changyao Chen; Rosenblatt, Sami; Bolotin, Kirill I.; Kim, Philip; Kymissis, Ioannis; Stormer, Horst L.; Heinz, Tony F.; Hone, James; IEEE International Electron Devices Meeting (IEDM), 2009

“A Locally Amplified Organic Transistor Strain Sensor Based on a Piezoelectric Polymer” Y.J. Hsu, Z. Jia, I. Kymissis, Aug, 2009, SID MAC Symposium on Organic and Thin Film Electronics, Cornell University.

“Novel High Frequency Surface Mounted Optical Recording System for Chronic Intracranial Optical Imaging.” Ma, H. T. and Cox, M. and Bahlke, M. and Beck, J. and Zhao, M. and Kymissis, I. and Schwartz, T. *Epilepsia*, 50 p 393, 2009.

“Semiconductor Dielectric Interfacial Study using Spectral Spatial Photocurrent Probes and 1/f Noise Probe in Organic Field Effect Transistors.” Zhang Jia, Inanc Meric, Kenneth Shepard and Ioannis Kymissis. 2009 Fall MRS, Boston, MA.

“Strain Field and Magnetic Field Sensors with OLED Indicators Employing Piezoelectric and Magnetoresistive Gated OFET.” Hsin Jung Lee, Shyuan Yang, Yu Jen Hsu and Ioannis Kymissis. 2009 Fall MRS, Boston, MA.

“Semiconductor Dielectric Interfacial Study Using Spectral Spatial Photocurrent Probes and 1/f Noise Probe in Organic Field Effect Transistors” Zhang Jia, Inanc Meric, Kenneth Shepard, and Ioannis Kymissis. 2009 ISDRS, College Park, MD.

(invited) “A locally amplified strain sensor using piezoelectric polymers and Organic Field Effect Transistors” I. Kymissis. 2009 SPIE International Symposium on Optical Science and Technology, San Diego CA.

”Challenge: Ultra Low Power Energy Harvesting Active Networked Tags (EnHANTs)” Maria Gorlatova, Peter Kinget, Ioannis Kymissis, Dan Rubenstein, Xiaodong Wang, and Gil Zussman. Mobicom 2009, Beijing, China.

”An Array of Monolithic FBAR CMOS Oscillators for Mass Sensing Applications.” M.L. Johnston, I. Kymissis, and K.L. Shepard. Transducers 2009, Denver CO.

(invited) ”Flexible Electronics Activities in the United States.” 2nd International Symposium on Flexible Organic Electronics, Halkidiki, Greece. July 2009.

(invited) “Organic semiconductor based sensors for strain and reflectivity monitoring.” 2nd International Symposium on Flexible Organic Electronics, Halkidiki, Greece. July 2009.

“Organic Photovoltaics from Extended Aromatic Molecules.” Alon A. Gorodetsky, Marshall Cox, Noah J. Tremblay, Ioannis Kymissis, Colin Nuckolls. Symposium on Organic and Thin Film Electronics, Society for Information Displays, Ithaca, NY, August 18, 2009.

“Air Stable Organic Photovoltaics from Small Molecule Acene Derivatives.” Alon A. Gorodetsky, Marshall Cox, Noah J. Tremblay, Ioannis Kymissis, Colin Nuckolls. Organic Microelectronics and Optoelectronics Workshop V, American Chemical Society and Materials Research Society, San Francisco, CA, July 6 9, 2009.

“Spin cast high k non hysteresis barium titanate nanoparticle thin film as gate dielectric in organic thin film transistors” Z. Jia, L. Huang, S. O’Brien, I. Kymissis. MRS Spring 2009, San Francisco, CA.

“Photocurrent study of traps states in pentacene thin film transistors” Z. Jia, L. Banu, I. Kymissis. MRS Spring 2009, San Francisco, CA.

“A Locally Amplified Organic Transistor Sensor Based on a Piezoelectric Polymer” Y. J. Hsu, Z. Jia, I. Kymissis. MRS Spring 2009, San Francisco, CA.

“A Locally Amplified Organic Transistor Sensor Based on a Piezoelectric Polymer” Y. J. Hsu, Z. Jia, I. Kymissis. Connecticut Microelectronic and Optoelectronic Consortium Annual Meeting, 2009.

“Photocurrent study of traps states in pentacene thin film transistors”. Z. Jia, L. Banu, I. Kymissis. Connecticut Microelectronic and Optoelectronic Consortium Annual Meeting, 2009.

(invited) ”Integrated Circuits, Optics, and Sensors using Organic Field Effect Transistors and Photodetectors” International Meeting on Information Display/Asia Display 2008. Ilseon, Korea, 2008.

(invited) "Beyond mobility: optical and electrical probes for characterizing and understanding OFETs" I. Kyymissis. 2008 International Materials Research Conference (IMRC), Chongqing, China.

(invited) "Active matrix photodetection using OFETs and printed photoconductors" I. Kyymissis. 2008 International Materials Research Conference (IMRC), Chongqing, China.

∫∫∫Influence of Source Drain Contact Resistance on Mobility in Organic FETs,∫∫∫ K. Ryu, I. Nausieda, I. Kyymissis, V. Bulovic, and C.G. Sodini, 3rd Annual Organic Microelectronics Workshop, Seattle, WA, July 2007

"An Organic Imager for Flexible Large Area Electronics" I. Nausieda, K. Ryu, I. Kyymissis, A. Akinwande, V. Bulović, C. Sodini. 2007 International Solid State Circuits Conference (ISSCC), San Francisco, CA.

(invited) "Characterization of OFETs in the linear region of operation." ACS NERM, Binghamton, NY. October 2006. I. Kyymissis, K. Ryu, A. Wang, I. Nausieda, C. Sodini, V. Bulović.

"A Locally Amplified Organic Transistor Strain Sensor Based on a Piezoelectric Polymer" Y.J. Hsu, Z. Jia, I. Kyymissis, Nov, 2008, IEEE EDS Western Region Symposium, Rochester, New York.

"Control of Parasitics in OFETs Through Self aligned Processing." Ivan A Nausieda, Ioannis Kyymissis, and Vladimir Bulović. MRS Fall 2006, San Francisco, CA.

"Molecular Organic Electronic Circuits" V. Bulović, K. Ryu, C. G. Sodini, I. Kyymissis, A. Wang, I. Nausieda, A. I. Akinwande. IEEE/ACM International Conference on Computer Aided Design, 2006. ICCAD '06. Nov. 2006 Page(s):830 831

"A Self Aligned Fully Lithographic Process for Integrated OFETs." Ioannis Kyymissis, Kevin Ryu, Akintunde I. Akinwande, Charles G. Sodini and Vladimir Bulović. MRS Spring 2005, San Francisco, CA.

"A process for integrated organic photodetection." I. Kyymissis, C.G. Sodini, A. I. Akinwande and V. Bulović, SPIE Photonics West, San Jose, CA, January 2005

"An Organic Semiconductor Based Process for Photodetecting Applications." I. Kyymissis, C.G. Sodini, A. I. Akinwande and V. Bulović. International Electron Device Meeting, 2004, San Francisco, CA, December 2004.

"Process Control of Threshold Voltage in Organic FETs." A. Wang, I. Kyymissis, V. Bulović, and A.I. Akinwande. International Electron Device Meeting, 2004, San Francisco, CA, December 2004.

(invited) "What Will be the New Oxide for Organic Semiconductors?" I. Kyymissis, A.I. Wang, A.I. Akinwande, and V. Bulović. Society for Information Display Mid Atlantic Chapter OLED Research and Technology Conference, Park Ridge, NJ, November 2004

"Physical Extraction of Mobility in OFETs" K. Ryu, I. Kyymissis, V. Bulović and C. Sodini Society for Information Display Mid Atlantic Chapter OLED Research and Technology Conference, Park Ridge, NJ, November 2004

“Pentacene Organic TFT with Al<sub>2</sub>O<sub>3</sub> Gate Dielectric Deposited using Atomic Layer Deposition Method.” YongWoo Choi, JinSeong Park, Ioannis Kymissis, Annie Wang, Roy G. Gordon and Akintunde I. Akinwande. Materials Research Society Spring Meeting, San Francisco, CA, April 2004

“Fabrication of Active Devices and Logic Gates on Fibers.” YongWoo Choi, Ioannis Kymissis, Annie Wang, and Akintunde I. Akinwande, Materials Research Society Spring Meeting San Francisco, CA, April 2003

“Organic Field Emission Device Integrated with Organic Transistor.” I. Kymissis, A. I. Akinwande. International Electron Device Meeting, 2002, San Francisco, CA, December 2002.

“Field Emission from Organic Composites.” I. Kymissis, A. I. Akinwande. International Vacuum Microelectronics Conference 2002, Lyon, France, July 2002.

“Organic Conducting Composites for Field Emission Applications.” I. Kymissis, A. I. Akinwande. Materials Research Society Spring Meeting 2002, San Francisco, CA, April 2002.

“Novel CMP based process for fabricating arrays of double gated silicon field emitters.” L. Dvorson, I. Kymissis (presenting author), A. I. Akinwande. International Vacuum Microelectronics Conference 2001. Davis, CA. August 2001.

“Organic Semiconductor Thin Film Field Effect Transistors.” C. D. Dimitrakopoulos, J. Kymissis, S. Purushothaman, in Proceedings of The Int. Conf. on digital Printing Technologies, NIP16, Society of Imaging Science and Technology, Vancouver 2000, pp. 493 496.

“Organic transistors with low operating voltage and high mobility.” C. D. Dimitrakopoulos, S. Purushothaman, J. Kymissis, A. Callegari, D. A. Neumayer, P. R. Duncombe, R. B. Laibowitz, J. M. Shaw. Device Research Conference. Santa Barbara, CA 1999.

“Relatively Low Operating Voltage and High Field Effect Mobility Field Effect Transistors Based on Pentacene.” C. Dimitrakopoulos, S. Purushothaman, J. Kymissis, A. Callegari. Materials Research Society Fall Meeting, Boston, MA. December 1998.

“Parasitic power harvesting in shoes.” J. Kymissis, C. Kendall, J. Paradiso, N. Gershenfeld. IEEE Comput. Soc Digest of Papers. Second International Symposium on Wearable Computers 1998 Los Alamitos, CA.

#### SEMINARS AND CORPORATE PRESENTATIONS (SELECTED)

Boeing, Micron, KLA Tencor, University of Tampere (2019), ST Microelectronics, Agrate (2019), ST Microelectronics, Grenoble (2019), Rutgers (2019), SUSTECH (2018), Jordan University of Science and Technology (JUST) (2018), Kent state University (2018), McMaster University (2018), Honda research (2017), Abo Akademi (2017), Corning (2017), UCSD (2017), UDelaware (2017), IBM Research (2016), Microsoft (2016), Lehigh University (2016), University of Central Florida (2016), Checkpoint (2016), University of West Virginia (2016), KAUST (2016), Ecole Polytechnique (Paris) (2016), University of Pennsylvania (2015), Datacolor (2015), Jet Propulsion Laboratory (2015), Xerox (2014), University of Toronto (2014), UCLA (Material Science) (2014), NIST (2014), Princeton University (Mechanical Engineering) (2014), NC State (EE) (2013), Department of Physics, City College (2014), Cooper Union (2013), QDVision (2013), University of Michigan (2012), City College, Department of Chemistry, City

University of New York (2012), City College, Department of Chemical Engineering, City University of New York (2012), General Electric Global Research Center (2012), Microsoft (2012), Plextronics (2012), University of Iowa (2012), UC Irvine (2012), Ecole Polytechnique (Montreal) (2012), University of Florida (2012), Cooper Union (2011), Stanford Research Institute (2011), University of Washington (2011), Wake Forest (2010), University of Delaware (2010), Queens College (2009), University of Puerto Rico Mayagues (2009), Yale University (2009), Seoul National University (2008), Samsung Mobile Display (2008), University of Connecticut (2008), Princeton University (2008), TASC/Elettra (2008), Columbia University MRSEC colloquium (2007), Rochester Institute of Technology (2007), Cornell MSE Colloquium (2005), Binghamton EE (2005)

US PATENTS  
(ISSUED)

10,859,437 Integration of optical components within a folded optical path  
 10,663,361 Systems and methods for tactile sensing  
 10,656,013 Nanostructure based article, optical sensor and analytical instrument and method of forming same  
 10,652,963 LED display structures and fabrication of same  
 10,122,345 Co integrated bulk acoustic wave resonators  
 10,107,612 Systems and methods for contact localization through spatially overlapping signals  
 10,041,689 Wireless automatic temperature control of radiator heating  
 9,863,979 Systems, apparatus, and methods for energy monitoring  
 9,666,600 Direct bandgap substrates and methods of making and using  
 9,431,623 Flexible devices including semiconductor nanocrystals, arrays, and methods  
 9,420,701 Flexible direct or USB plug in platform for foldable or flexible electronics  
 9,390,920 Composition including material, methods of depositing material, articles including same and systems for depositing material  
 9,366,571 Photonic crystal sensor apparatus and techniques  
 9,293,553 Graphene electrodes for electronic devices  
 9,257,606 Direct bandgap substrates and methods of making and using  
 9,255,912 Monolithic FBAR CMOS structure such as for mass sensing  
 9,252,013 Methods and articles including nanomaterial  
 9,194,801 Systems and methods for a DNA based thermometer  
 9,120,149 Methods and articles including nanomaterial  
 9,099,661 OFET including PVDF TRFE CFE dielectric  
 9,096,425 Methods for depositing nanomaterial, methods for fabricating a device, methods for fabricating an array of devices and compositions  
 9,054,329 Light emitting devices and displays with improved performance  
 8,906,804 Composition including material, methods of depositing material, articles including same and systems for depositing materials  
 8,854,624 Photonic crystal spectrometer  
 8,835,941 Displays including semiconductor nanocrystals and methods of making same  
 8,750,517 Friend or foe detection  
 8,472,758 Optical structures including nanocrystals  
 8,470,617 Composition including material, methods of depositing material, articles including same and systems for depositing material  
 8,441,018 Direct bandgap substrates and methods of making and using  
 7,955,766 Software controlled maskless optical lithography using fluorescence feedback  
 7,858,975 Organic field effect transistor systems and methods  
 7,683,323 Organic field effect transistor systems and methods  
 7,345,764 Apparatus and method for a slim format spectrometer  
 6,870,312 Organic field emission device  
 6,569,707 Method for improving performance of organic semiconductors in bottom electrode structure  
 6,500,604 Method for patterning sensitive organic thin films

6,335,539 Method for improving performance of organic semiconductors in bottom electrode structure  
 6,180,956 Thin film transistors with organic inorganic hybrid materials as semiconductor channels

EXPERT TESTIMONY Kumar vs. American Family Insurance, No. 3:2021 cv 00068 (S. D. of Iowa)  
 Retained by Kumar, prepared expert report.

AcBel Polytech, Inc. v. Fairchild Semiconductor International, Inc., No. 1:13 cv 13046 (D. Mass.)  
 Retained by AcBel Polytech. Prepared expert reports. Deposed.

Samsung Display Company, Ltd., vs. Mianyang BOE. IPR AIA review 2023 01075.  
 Retained by Samsung Display. Prepared expert report, deposed. Advisory on IPR 2023 00988, IPR 2023 01075.

Samsung Display Company, Ltd., and Samsung Electronics America, Inc. vs. Mianyang BOE. ITC Investigation No. 337 TA 1378. Retained by Samsung Display.  
 Prepared expert report, deposed, testified.

#### UNIVERSITY LEADERSHIP

Chair. Provost research advisory committee to the library research subcommittee (PACL) (2022 present)  
 Chair, School at Columbia Advisory committee (2023 )  
 co chair, School at Columbia Advisory HOS search committee (2021 2023)  
 Faculty in Residence, Hartley Hall/first year zone (2012 present)  
 Columbia Maker Space, Director (2014 present)  
 Member, School at Columbia Advisory committee (2020 2023)  
 Provost Leadership Fellow (2017 2019)  
 Member. Provost research advisory committee to the library (PACL) + research subcommittee (2018 present)  
 CNI Shared Facilities, faculty Director (2016 present)  
 Faculty advisor, TBP (2016 present)  
 Faculty advisor, Columbia Space Initiative (2015 present)  
 Nano Initiative co chair (2014 2016)  
 CISE/Columbia Nano Initiative executive committee (2012 present)  
 EFRC: Thrust leader and executive committee member (2008 2014)  
 Institute for Data Sciences and Engineering: Space planning committee (2012 2019)  
 Columbia University Cleanroom Committee (2008 present)  
 NSEC: Outreach and education committee member (2008 2010)  
 Columbia Environmental Health and Safety Faculty Working Group (2008 2015)

#### DEPARTMENT LEADERSHIP

EE Department Chair (2020 2024)  
 EE Department vice chair (2019 2020)  
 EE Department undergraduate program chair (2010 2019)  
 EE Safety committee (2020 present)  
 EE Department ombudsman (2019 2020)

|                                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|---------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| UNIVERSITY<br>ADMINISTRATIVE<br>PROGRAMMING | Path to professorship (panelist) (2018 present)<br>Responsible conduct of research (panelist) (2019 present)<br>COI monitor (2017 2023)<br>Family Weekend (EE, Makerspace programs) (various)<br>Organizing committee, NanoDay 2009                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| EXTERNAL<br>ACADEMIC SERVICE                | FWO (Flanders Research Foundation) Energy, Electrical Engineering, Electronics and Mechanics External expert (2019 2023)<br>External Evaluator, National Technical University of Athens EE program (2021)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| PROGRAM<br>COMMITTEES                       | IEEE IFETC Program Committee 2022<br>IMID: Program committee/Advisory board 2019,2018<br>ICDT: International Advisory Board 2022, 2021, 2020, 2019, 2018<br>IDW: Program committee 2019, 2018, 2017, 2016, 2015<br>SID: EMD program committee 2022, 2021, 2020, 2019, 2018, 2017, 2016, 2015<br>SID: Vice program chair, 2019<br>SIGGRAPH: External reviewer 2022, 2021, 2020, 2018, 2017<br>EMC: Program committee 2022, 2021, 2020, 2019, 2018, 2017, 2016<br>IEDM: Program committee 2016, 2015, 2014<br>MRS: Symposium organizer 2021, 2019, 2015, 2013, 2011, 2009, 2007<br>DRC: GenChair 2014, TPC Chair 2013, TPC VC 2012, TPC member 2011, board member (2014 present)<br>SPIE: Symposium organizer 2023, 2022, 2021, 2020, 2019, 2018, 2017, 2016, 2015, 2014, 2013, 2012, 2011, 2010, 2009, 2003<br>LOPE c: VP Americas/program committee 2014, 2013, 2012, 2011<br>IEEE/MRS/ACS Organic Electronics Workshop: Executive committee 2009 2011<br>SID MAC Workshop on Organic and Thin Film Electronics, chair, 2009<br>CS/IEEE/MRS North East Regional Meeting, co organizer, 2006<br>International Vacuum Nanoelectronics Conference: Local arrangements 2004 |
| EDITORIAL<br>POSITIONS                      | Publication chair, Society for Information Display (SID) 2015 2018<br>Editor in Chief, Journal of the Society for Information Display (JSID). 2012 2015<br>Associate Editor, Journal of the Society for Information Display (JSID). 2015 present<br>Associate Editor, KIDS Journal of Information Display (KIDS JID). 2011 2016<br>Associate Editor, IEEE Transactions on Electron Devices (IEEE TED). 2014 2022<br>Associate Editor, IEEE Open Journal of Immersive Displays (2024 )<br>Advisory Board (EDS representative) Journal of Electronic Materials (2024 )                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| ELECTED<br>POSITIONS                        | EDS Distinguished Lecturer 2019 present<br>Armstrong Memorial Research Foundation, Board/Treasurer 2016 present<br>President Elect, Society for Information Display. 2022 present<br>Treasurer, Society for Information Display. 2020 2022<br>Secretary, Society for Information Display. 2018 2020<br>Director, Device Research Conference Inc. (a non profit foundation). 2014 present<br>VP Americas East, Society for Information Display. 2017 2018<br>IEEE EDS Regions 1 3 & 7 SRC Vice Chair; IEEE Electron Device Society. 2012 2017<br>Director, Society for Information Display, Mid Atlantic Chapter. 2012 2017<br>Publication Chair, Society for Information Display. 2015 2018<br>Chairman, EDS Vice chair. IEEE New York Section Electron Device/Solid State Circuit Society Joint Chapter. 2007 present<br>Secretary, Treasurer, Vice chair , Chair. Society for Information Display, Mid Atlantic Chapter. 2007 2011                                                                                                                                                                                                                                    |

GRADUATE THESES Completed:  
SUPERVISED

Christine McGinn (PhD, NIST)  
 “MicroLED and Microdevices for Next Generation Display Systems”, Keith Beherman, 2021 (PhD, Fathom Radiant)  
 “Non reciprocal Acoustic Devices for RF Communications”, Columbia University EE, Jose Bhanmode 2019 (PhD, Lelantos)  
 “Flexible Electronics for Large Area Sensing and Stimulation”, Columbia University EE, Caroline Yu 2019 (PhD, Apple)  
 “Domain Broadening in Periodic Poling of Thinned Lithium Niobate and Spectroscopic Methods for Whole Blood Analysis” Columbia University APAM, Peter Bullen 2019 (PhD, Lumentum)  
 “Optoelectronic Neural Implant Sensors for Cerebral Blood Volume Monitoring” Columbia University EE, Christopher Choi 2018 (PhD, Fenwick and West)  
 “Monolithic Integration Piezoelectric Resonators on CMOS for Radio Frequency and Sensing Applications” Columbia University EE, Aida Colon Berrios 2018 (PhD, Apple)  
 “Charge Injection and Transport in Pentacene Field Effect Transistors” Columbia University EE, Amrita Masurkar 2016 (PhD, BAE Systems)  
 “Monolithically Integrated Acoustic Resonators on CMOS for Radio Frequency Circuit Applications” Columbia University EE, Hassan Eddrees 2016 (PhD, Apple)  
 “Ionizing Radiation Effects on Graphene Based Field Effects Transistors” Columbia University EE, Kostas Alexandrou 2016 (PhD, Intel)  
 “Optimization of Printed Electronics”, Columbia University EE, Shyuan Yang 2015 (PhD, Apple)  
 “Excimer Laser Crystallization of Silicon Thin Films for Monolithic 3D Integration”, Columbia University EE, Fabio Carta 2015 (PhD, IBM)  
 “Harvest,” School of Visual Arts, MFA Damon Ahola, 2014 (MS, Lyft)  
 “Organic photovoltaic device architectures”, Columbia University EE, Jonathan Beck 2013 (PhD, Apple)  
 “Systems for Pervasive Electronics and Interfaces”, Columbia University EE, John Sarik 2013 (PhD, Nanohmics)  
 “Electrowetting on dielectrics”, Columbia University EE, Haig Norian (Co supervised with Ken Shepard) 2013 (PhD, ASML)  
 “Processes and Materials for Organic Photovoltaics”, Columbia University EE, 2012, Marshall Cox. (PhD, Kelvin)  
 “Ultrasound Data Communications for Ultra low power Wake up in Sensor Nodes”, Columbia University EE, 2012, Kshitij Yadav. Co supervised with Peter Kinget. (PhD, Qualcomm)  
 “Advanced Integration of Devices Enabled by Laser Crystallized Silicon”, Columbia University EE, 2012, Vincent Lee. (PhD, NSF)  
 “The Integration and Applications of Organic Thin Film Transistors and Ferroelectric Polymers” Columbia University EE, 2012, Yu Jen Hsu. (PhD, Space/X)  
 “Interfacial Studies in Organic Field Effect Transistors”, Columbia University APAM, 2011, Zhang Jia. (PhD, Meta)  
 Columbia University EE, Kevin Kam (PhD, Apple)  
 Columbia University EE, Vikrant Kumar (PhD, Apple)

In progress:

Columbia University EE, Zicong Huang  
 Columbia University EE, Peter Ballentine  
 Columbia University EE, Reem Alshanbari  
 Columbia University EE, Oliver Durnham

Columbia University EE, Megan Noga  
Columbia University EE, Huaquan Guo  
Columbia University EE, Ye Zhang

|               |                                                                          |
|---------------|--------------------------------------------------------------------------|
| POST DOCTORAL | Completed:                                                               |
| ASSOCIATES    | Sung Jin Kim (Chungbuk National University)                              |
| SUPERVISED    | Nadia Pervez (Rice University)                                           |
|               | Brian Tull (Space/X)                                                     |
|               | Htay Hliang (Applied Materials)                                          |
|               | En Chen Chen (KLA Tencor)                                                |
|               | Steve Park (KAIST)                                                       |
|               | Marco Roberto Cavallari (State University of Campinas (Unicamp), Brazil) |
|               | Lei (Andy) Zhang (University of Melbourne)                               |
|               | Stylianios Siontas (Lelantos)                                            |
|               | Zachary Lamport (Exponent)                                               |
|               | Sayan Dey (IIT Bhubaneswar)                                              |
|               | Rajinder Deol (Washington University)                                    |
|               | Sourabh Pal (Max Planck Institute for Polymer Physics)                   |
|               | Nikika Batra                                                             |

In progress:

|               |                             |
|---------------|-----------------------------|
| POST DOCTORAL | Completed:                  |
| ASSOCIATES    | Theanne Schiros (SUNY/FIT)  |
| CO SUPERVISED | Robert Barton (Amazon)      |
| (50%)         | Octavi Semonin (Powerhouse) |