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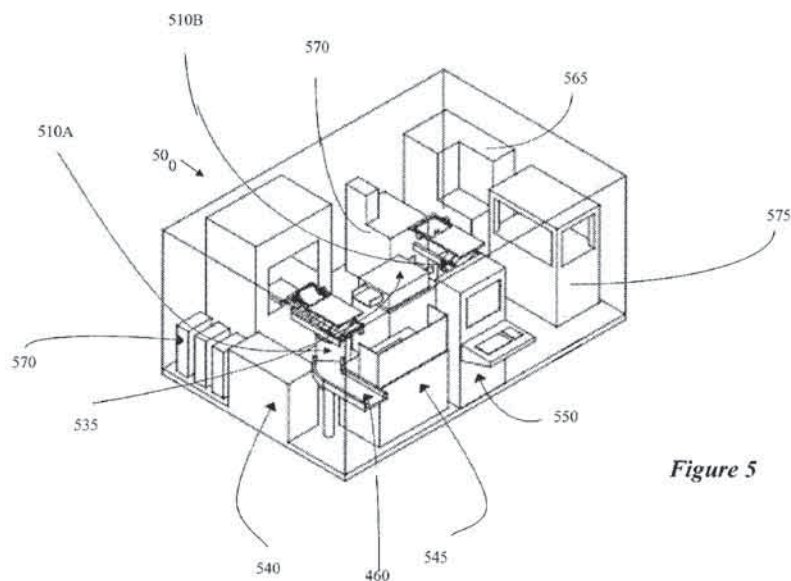


Figure 5

(57) Abstract: Systems and methods are provided for producing functional printed circuit boards. It is intended that the systems and methods described herein will allow the production of functional PCBs in a more efficient and less labor- and equipment-intensive manner than may be obtained using conventional production methods. The produced functional PCB would have the required mechanical, thermal, electrical, etc., characteristics enabling it to function in a manner corresponding to a design characteristics of a conventional PCB.

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## **METHOD AND APPARATUS FOR RAPID FABRICATION OF FUNCTIONAL PRINTED CIRCUIT BOARD**

### **CROSS-REFERENCE TO RELATED APPLICATIONS**

**[0001]** This Application is a continuation of and claims priority from U.S. Application, Serial Number 60/902,972, filed February 23, 2007; U.S. Application, Serial Number 60/972,657, filed September 14, 2007; and U.S. Application, Serial Number 60/997,807, filed October 5, 2007; the disclosure of all of which is incorporated herein by reference in its entirety.

### **BACKGROUND**

#### **1. Field of the Invention**

**[0002]** The general field of the invention relates to the field of the manufacture of printed circuit boards. More specifically, the present application relates to systems and methods for producing functional printed circuit boards, including functional prototype circuit boards, in a quick, safe, clean, waterless, efficient and compact manner.

#### **2. Related Arts**

**[0003]** Printed circuit boards (PCBs) are used to mechanically support and electrically connect electronic components using conductive pathways, or traces. In conventional PCB manufacture, such conductive pathways or traces are etched or milled from copper sheets laminated onto a non-conductive substrate. Such a process is relatively time consuming and utilizes harmful materials and solvents. Additionally, these processes generate waste material that needs to be disposed of in a safe and environmentally sound manner. PCBs may be used in any of a variety of applications, including computers, cell phones, and other electronics applications.

**[0004]** One issue associated with conventional PCB manufacture is that the production of the PCBs is a relatively complicated and time-consuming process. For example, to produce a single prototype PCB using conventional manufacturing methods, it may require, typically,

between 5 and 30 working days (including electronic component assembly and shipment times), mainly depending on complexity of the fabricated board. Additionally, because various stages of the production are typically performed using a variety of different equipment, which may be located in different locations, the production of conventional PCBs require logistical coordination which may lead to further delays. Consequently, conventional fabrication techniques introduce significant time delays, especially in prototype fabrication and design of new devices utilizing PCBs.

**[0005]** Another issue associated with conventional PCB manufacture is the intensive use of fabrication tools, such as masks and stencils throughout most process phases, thus requiring production of new tools and patterns for each design fabricated. As this is a fair overhead for mass production runs, small quantity production runs (such as New Product Introduction – NPI, and prototyping in particular) suffer enormous overhead of time, costs, handling and materials. The conventional use of masks also necessitates the use of hazardous materials and solvents, thereby requiring certain steps of the manufacturing to be carried out in specially designed facilities, which increase the manufacturing costs.

**[0006]** Recent trends in the industry lead to higher complexity PCB fabrication due to use of more complex technologies and higher demands in fabrication. Some examples are: higher clock frequencies, higher demands on controlled impedance, miniaturization which derives requirements for smaller traces, smaller pads and vias diameter and more layers. The smaller the features are, the harder it will be for conventional technology to handle them due to fundamental limitations of the traditional fabrication process. For instance, registration (i.e. lamination of separate board layers) is a problematic phase in terms of accuracy, which is driving conventional PCB fabrication down in terms of yield and accuracy.

**[0007]** The requirements on the registration between layers of traditional PCB manufacture increase with advanced technologies. Furthermore, registration is one of the bottlenecks in the process, requiring heavy and expensive equipment, and, most importantly, is a challenge in terms of accuracy and yield (as layers are fabricated individually, suffering individual, non-linear stretching, and then should be aligned and laminated in accuracies of tens of microns). Another bottleneck in conventional manufacturing process is the drilling. A typical

PCB contains hundreds to tens of thousands holes in various diameters, which require a set of drilling machines (e.g. mechanical and laser drilling machines), working in sequential order possibly with every lamination of every new layer to form the different via types (e.g. buried via). It is a costly chain in the process, both in time and money (e.g., due to the rapid wear out of small-diameter drillers), and can cost up to 30% of overall fabrication costs.

**[0008]** As is well known, conventional PCBs comprise conductive and insulative layers formed over a substrate. The conductive layers form conductive circuitry according to the desired design. The conductive circuitry is fabricated using masks, e.g., photoresist masks, to delineate the designed conductive circuitry to be formed on the substrate. Once the mask has been developed, techniques such as metal electroplating are utilized to deposit conductive material, e.g., copper, onto the unmasked areas of the substrate. In some designs the mask is then removed, while in others the mask remains on the PCB. Electroplating or electroless plating is also used for the interconnect fabrication, to provide electrical connection between the metal layers. For further discussion relating to this technology, specifically utilizing SU-8 as the resin for the photoresist, the reader is directed to U.S. patent 4,882,245, the content of which is incorporated herein by reference.

**[0009]** SU-8 is an octafunctional epoxidized novolac commercially available from Celanese Corporation of Dallas, Texas. As explained in the above cited '245 patent, when properly mixed with a photoinitiator and other components, SU-8 may be cured using exposure to radiation, e.g., selective UV illumination, to thereby delineate the circuitry over the substrate. The '245 patent recommends the use of UVE 1014, available from General Electric, of Fairfield, CT, as the photoinitiator, but other materials, e.g., triarylsulfonium salts, may be used.

**[0010]** Rapid prototyping is the automatic construction of physical objects or models using, e.g., solid freeform fabrication or direct writing. solid freeform fabrication (SFF) is a technique for manufacturing solid objects by the sequential delivery of energy and/or material to specified points in space to produce that solid. Rapid prototyping takes virtual designs from computer aided design (CAD) or animation modeling software, transforms them into thin, virtual, horizontal cross-sections and then creates each cross-section in physical space, one after the next until the model is finished. With additive fabrication, the machine reads in data from a CAD

drawing and lays down successive layers of liquid, powder, or sheet material, and in this way builds up the model from a series of cross sections. These layers, which correspond to the virtual cross section from the CAD model, are joined together or fused automatically to create the final shape. The primary advantage to additive fabrication is its ability to create rapidly almost any two or three-dimensional shape or geometric feature. Therefore, rapid prototyping is generally used to provide a physical model, but not necessarily a working model, of a designed part.

**[0011]** As PCBs are developed for a new product, it is common to first design a PCB and then produce a prototype of the PCB, which requires considerable time, effort and expense. The PCB prototype is then assembled with electronic components and then tested. Most often, the test results reveal either functional or performance deficiencies, so that the process is repeated until the last PCB prototype version is validated as correct and ready for mass production.

**[0012]** Currently, the absolute majority of PCB prototypes are produced in the same process and equipment and are made of the same materials as mass production PCB. This manufacturing process is very labor intensive and inefficient for prototype and low-quantity production, resulting in considerable waste of time, efforts and expense.

**[0013]** Therefore, there continues to be a long existing need in the life cycle of PCBs for the capability to rapidly and reliably move from the design stage through the prototype stage, to mass-production. Particularly, it is required to go directly from computer PCB designs to immediate prototypes economically and automatically.

**[0014]** PCB prototypes are of very high importance in the PCB development process, as they constitute the ultimate means and measure for testing the developed design, and are virtually the most important factor in taking the go-to-mass-production decision. Taking a risky go-to-mass-production decision which is based on PCB prototype which is not correlated in testing results to the mass-production fabricated PCB may result in failure of mass-production series produced, thereby causing significant loss of time and money.

**[0015]** Various technologies are currently used in the general art of rapid prototyping, including selective laser sintering (SLS), fused deposition modeling (FDM), stereolithography (SLA), laminated object manufacturing (LOM), electron beam melting (EBM), and 3D printing

(3DP). In general, the art of rapid prototyping provides a physical, rather than functional, validation of the designed product.

**[0016]** Several attempts have been previously made to provide rapid PCB prototyping and manufacturing systems. Some of them also proposed that mechanical rapid prototyping or similar techniques may be used for PCB fabrication. For example, it has been proposed to utilize extrusion to form metal traces over conventional PCB substrate. According to another proposal, UV laser is used to partially cure a resin, so as to form a partially cross-linked substrate. Metal traces are then deposited over the substrate in a conventional manner. The substrate is then placed in a mold to change its shape to a 3D shape, and is then completely cured to result in a 3D PCB. According to yet another proposal, 3D printing may be used for fabricating PCBs, using a printer head for dispensing conductive material and another printer head for dispensing insulative material. For further information about such techniques, the reader is directed to: WO0052976, US5,172,472, US5,099,090, US5,156,772, US6,169,605, US5,838,567, US5,264,061, and U.S. published application Nos. 2004/0077112.

**[0017]** All of these attempts have indeed proposed alternative rapid methods for PCB production, compared to the conventional PCB manufacture method. Conventional PCB manufacturing processes, systems and materials were tightly adapted, for over 60 years, to the desired functionality of the produced PCB (which depends on its use and target application). Therefore alternative manufacturing methods, which are different compared to conventional PCB manufacture methods, should be adapted to fit target PCB functionality criteria. Otherwise, the fabricated prototype PCB will be merely a mechanical, limited-functionality model, and not a fully functional electro-mechanical structure, as it is designated to be. To date, prior art attempts have failed to consider the functional value of the fabricated PCB, or provide means to control the functionality and adapt it to desired functionality criterions.

**[0018]** Generally, testing results depend on functional behavior of the PCB under different conditions. This behavior depends further on numerous properties, which are strictly defined in published PCB industry standards.

**[0019]** Yet, in spite of all efforts and available technology, rapid fabrication of PCB remains an elusive goal and to this day, PCB fabrication is made using decades-old techniques of

patterning, laminating, drilling conductor plating, solder resist, and screen printing. This protracted process causes delays and cost increases in both the design and manufacturing phases of any product utilizing a PCB. Accordingly, there is a need in the art for a revolutionary technology that would drastically reduce the fabrication time and manufacturing complexity. Additionally, there is a need in the art for a technique that would avoid or minimize the intensive use of toxic and/or hazardous materials of conventional fabrication methods. These methods are also extremely wasteful, as it is estimated that only about 7% of the materials used in the production process end up in the PCB. The remaining 93% are mainly disposed off as toxic waste, thereby causing significant environmental damage.

## **SUMMARY**

**[0020]** The following summary of the invention is described in order to provide a basic understanding of some aspects and features of the invention. This summary is not an extensive overview of the invention, and as such it is not intended to particularly identify key or critical elements of the invention, or to delineate the scope of the invention. Its sole purpose is to present some concepts of the invention in a simplified form as a prelude to the more detailed description that is presented below.

**[0021]** According to an aspect of the present invention, methods and apparatus for the quick and efficient production of functional PCBs and functional PCB prototypes, directly from computer designs, are provided.

**[0022]** A feature of the present invention is that the PCB fabricated, although produced of different materials and by different processes and machinery, compared to conventional manufacture methods (which are used in mass production), would yield testing results which highly correlate to the testing results of the same design when produced in conventional mass production methods.

**[0023]** It is another aspect of the present invention that the method and apparatus provided herein produce PCBs in correlation to important properties and specifications defined in prominent industry standards, as will be described in detail in the description. Furthermore, the present invention includes predetermined means for complying with current and future

standards in a structured manner, thus enabling flexibility in preparation to production of PCBs which comply with applicable industry standard, as specified for the required target application.

**[0024]** According to the various exemplary embodiments described in the present application, systems and/or methods are provided for producing functional printed circuit boards. It is intended that the systems and methods described herein will allow the production of functional PCBs in a more efficient and less labor- and equipment-intensive manner than may be obtained using conventional production methods. The produced functional PCB would have the required mechanical, thermal, electrical, etc., characteristics enabling it to function in a manner corresponding to design characteristics of a conventional PCB.

**[0025]** The invented equipment for fabricating PCBs is “office friendly” and suitable for use in clean operations, such as research and development facilities. Further, the systems and methods for fabricating the PCBs may result in the elimination (or tremendous reduction) of fabrication tools (e.g. masks and stencils) usage in this equipment, thus the fabrication process is easy to handle and very efficient for short production runs. Materials are selected for the various components of the PCBs that possess suitable electronic, electrical, electromagnetic, thermal and mechanical characteristics, as will be described in greater detail below.

**[0026]** According to an exemplary embodiment, rapid prototyping equipment is used to allow the production of functional PCBs in a shortened duration as compared to conventional methods (e.g., in as little as a several hours according to one exemplary embodiment). Such time savings may be achieved by changing not only the process phases involved in the manufacture of the PCBs, but also the equipment and materials used. Conventional PCB manufacturing requires tens to hundreds of skilled employees, very high investment in equipment and inventory, and large manufacturing facility. On the other hand, according to a particular exemplary embodiment, a PCB may be manufactured by a single operator using a single system that integrates various components that previously were part of multiple different machines. The process is fully automated and the single employee is merely responsible for replacing cartridges, load the system with fabrication data, simple system calibration etc. Optionally, electronic component assembly is integrated into the process so that a full turn-key system is provided.

**[0027]** According to an aspect of the invention, a PCB is fabricated without the use of a substrate or the conventional copper clad laminate (CCL). Rather, additive technologies, such as SFF techniques and/or electronic printing techniques, are utilized to fabricate a PCB from scratch, i.e., without a starting substrate. In one specific example, a radiation-curable liquid composition is deposited onto a tray. Then, the radiation-curable liquid composition is radiated to delineate the shape and the boundaries of the PCB, so as to provide a cured insulating layer. That is, the radiation can be provided selectively so as to cure the liquid to any size and shape PCB, including geometric forms within it (e.g. via holes). This first step generates an insulator that in essence replaces the conventional substrate that previously needed to be drilled and cut to the proper size and shape. After the insulating layer is cured, a conductive trace is deposited in an additive and maskless manner on the cured insulating layer using, e.g., ink jet, or other technology. Thereafter, another insulating layer is deposited using the radiation-curable liquid composition, and so on and so forth, until all of the layers are completed. Via metallization is also performed using additive technology, such as SFF. The PCB may then be flipped and another sequence of insulation and conductive layers provided on the other side, so as to generate a multi-layer, double-sided PCB. Various curing and baking steps may be utilized during the fabrication of each conductive and/or insulative layer. Among its various advantages, the inventive method avoids the problems of alignment and registration by performing registration for each layer while it is being fabricated, hence avoiding accumulation of inaccuracies.

**[0028]** According to an aspect of the invention, a method for fabricating at least one functional printed circuit board (PCB) is provided, comprising, a. obtaining a PCB fabrication data file; b. performing data conversion to generate a modified fabrication file corresponding to the fabrication data file; c. performing data transformation by modifying parameters specified in the modified fabrication file to account for variation in materials and processes utilized for fabricating the PCB, the data transformation generating a transformed fabrication file; d. providing a tray; e. using the transformed fabrication file to fabricate a dielectric layer by: i. depositing into the tray a liquid composition; ii. allowing the liquid composition to spread over the surface of the tray; and, iii. curing selected areas of the liquid composition to delineate the shape and the boundaries of the PCB to provide a cured insulating layer having a top and bottom surfaces; and, f. using the transformed fabrication file to fabricate a conductive layer by

depositing a conductive trace on at least one of the top and bottom surfaces of the cured insulating layer; to thereby provide a PCB having performance characteristics correlating to performance characteristics of a conventionally fabricated PCB using the fabrication data file. The method may further comprise repeating steps e and f a plurality of times over one of the top and bottom surfaces of the dielectric layer so as to provide a multi-layer one-sided PCB. The method may further comprise flipping the one-sided PCB so that the cured insulating layer becomes top layer on the tray, and repeating steps e and f a plurality of times on the other of the top and bottom surfaces of the dielectric layer so as to provide a multi-layered double-sided PCB. The method may further comprise repeating steps e and f a plurality of times over both of the top and bottom surfaces of the dielectric layer to provide a multi-layered double-sided PCB. The method may further comprise depositing one or more of an insulative solder mask layer, a conductive pad coating and a legend on the double-sided PCB using colored dielectric material.

**[0029]** Curing selected areas may comprise irradiating selected areas. Irradiating selected area may comprise directing UV radiation onto selected areas. Curing selected areas may further comprise a curing enhancement step following the irradiating the selected areas. The curing enhancement step may comprise a heating step. The heating step may comprise radiating the fabricated PCB with microwave radiation. In the method, step d may further comprise providing a release agent over the tray. Providing a release agent may comprise one of: providing a fabric layer over the tray or spreading a liquid releasing agent over the tray. The method may further comprise fabricating holes in the cured insulation layer by defining non-irradiated areas and cleaning the non-radiated areas after the curing step. The method may further comprise depositing conductive substance into selected holes to thereby fabricate conductive vias. Step e may comprise depositing into the tray a liquid composition comprising an octafunctional epoxidized novolac and photoinitiator. The liquid composition may further comprise nano-particles. Depositing a conductive trace may comprise using a deposition head to inject conductive substance onto the cured insulating layer. Each time step e is performed, sub-steps i. ii. and iii. may be repeated a plurality of times so as to fabricate the dielectric layer by fabricating a plurality of sub-layers. After each repetition of sub-step iii. heat may be applied to the fabricated PCB. Each time sub-steps i. ii. and iii. are performed, the method may further comprise fabricating holes in the sub-layer. Each time sub-steps i. ii. and iii. are performed, the

method may further comprise depositing conductive substance into selected holes. After a sequence of sub-steps i. ii. and iii. is performed a plurality of times, the method may further comprise depositing conductive substance into selected holes. At selected times wherein step e is performed, the method may further comprise fabricating curing enhancing tunnels in the fabricated dielectric layer. At selected times wherein step e is performed, the method may further comprise depositing soluble material to define voids in the fabricated dielectric layer. Each time step e is performed, sub-steps i. ii. and iii. may be repeated a plurality of times using at least two different dielectric materials, so as to fabricate the dielectric layer by fabricating a plurality of sub-layers having different dielectric insulation properties.

**[0030]** In the method, step e may further comprise mixing into the dielectric materials at least one of ingredients that assist in conductors adherence, ingredients that mechanically stabilize the dielectric material, and ingredients that thermally stabilize the dielectric and material. Step e may further comprise mixing into the dielectric materials ingredients that modify the insulating properties of the dielectric material. Step e may further comprise depositing onto the dielectric layer an intermediate layer formed for improved conductive material adherence to the dielectric layer. At selected times wherein step e is performed, the method may further comprise generating trenches on at least one surface of the dielectric layer and wherein step f comprises depositing at least part of the conductive trace into the channels. At selected times wherein step f is performed, the method may comprise depositing conductive traces of varying thickness as specified by the transformed fabrication file. At selected times wherein step f is performed, depositing conductive traces may comprise depositing a seed layer of conductive material and forming a main conductive layer over the seed layer. Forming a main conductive layer may comprise using electroplating. At selected times wherein step f is performed, the method may further comprise performing at least one of automated optical inspection of the formed conductive traces and electrical resistivity testing of the conductive traces.

**[0031]** The method may further comprise performing electrical testing at completion of fabrication of the PCB. A plurality of PCB boards may be fabricated concurrently within the tray. Each of steps e and f may further comprise selecting fabrication parameters according to at

least the desired insulation properties of the dielectric layer and resistivity properties of the conductive layer. Step e,ii, may further comprise planarizing a top surface of the liquid.

**[0032]** According to an aspect of the invention, a method for fabricating at least one functional printed circuit board (PCB) is provided, comprising: uploading PCB fabrication data file onto a controller; utilizing the controller to control operation of a central handling station to load and unload a fabrication tray onto and from a plurality of tray positioning stations; utilizing the controller to control operation of a dielectric dispenser to dispense a dielectric substance onto the tray and to control operation of a curing mechanism to cure the dielectric substance to form a dielectric layer; utilizing the controller to control operation of a conductor dispenser to dispense a conductive substance onto the dielectric layer; and, utilizing the controller to control operation of a thermal station to thermally process at least one of the dielectric substance and the conductive substance. Thermally processing may comprise exposing at least one of the dielectric substance and the conductive substance to at least one of: UV radiation, microwave radiation, and heater radiation. Controlling operation of the dielectric dispenser may comprise operating a liquid dispenser to dispense a radiation curable liquid onto the tray, and wherein curing the dielectric substance comprises radiating the liquid. Control operation of a dielectric dispenser may comprise operating a dispenser head to deposit dielectric substance according to layout design of the dielectric layer. The method may further comprise utilizing the controller to control operation of a planarizing mechanism to planarize the dielectric layer. Controlling operation of the conductor dispenser may comprise operating a printer jet to dispense conductive trace material.

**[0033]** The method may further comprise utilizing the controller to control operation of a flipping mechanism to flip a fabricated board so as to form conductive traces on both sides of the board. The method may further comprise fusing at least two fabricated boards together. The method may further comprise: operating the control console to generate a freeform fabrication file using at least the PCB fabrication data file; and, operating the control console to transform the freeform fabrication file into a transformed fabrication file, wherein selected data of the freeform fabrication file is transformed so as to enable correlating performance characteristics of the PCB to performance characteristics of a conventionally fabricated PCB. Transforming into

transformed fabrication file may further comprise generating files to control the curing mechanism to delineate vias. Transforming into transformed fabrication file may further comprise generating files to control the curing mechanism to delineate vias having oblique, non-vertical sidewalls. Transforming into transformed fabrication file may further comprise generating files to fabricate mating structures on each fabricated board to ensure alignment during the step of fusing the fabricated boards.

**[0034]** In the method, utilizing the controller to control operation of a conductor dispenser may comprise depositing conductive substance on both sides of the dielectric layer. The method may further comprise setting parameters of the curing mechanism to facilitate fabricating dielectric layer having properties corresponding to conventional PCB insulation layer fabricated according to the fabrication data file. The method may further comprise setting parameters of the conductor dispenser and the thermal station to facilitate fabricating conductive layer having properties corresponding to conventional PCB conductive traces fabricated according to the fabrication data file. Transforming into transformed fabrication file may further comprise changing a designed thickness of conductive lines to reduce resistivity. The method may further comprise utilizing the controller to control operation of the dielectric dispenser and the conductor dispenser to form vias by consecutively depositing thin dielectric sub-layers with holes defined therein and depositing conductive substance into the holes. At least two of the sub-layers may be formed using two different dielectric materials. The method may further comprise utilizing the controller to control operation of the dielectric dispenser and the conductor dispenser to form vias by depositing pillars of conductive substance and depositing dielectric layer about the pillars. The method may further comprise utilizing the controller to control operation of the dielectric dispenser, the conductor dispenser and a soluble material dispenser to form vias by depositing soluble material to delineate the vias, depositing dielectric layer about the soluble material, removing the soluble material to expose holes in the dielectric layer, and depositing conductive substance into the holes. The method may further comprise utilizing the controller to control operation of the conductor dispenser to form pad coating. The method may further comprise utilizing the controller to control operation of the dielectric dispenser to form solder mask and/or a legend.

**[0035]** According to an aspect of the invention, a method of fabricating a functional PCB is provided, comprising: forming a main dielectric layer having a top surface and a bottom surface by depositing a dielectric material onto a fabrication tray and exposing the dielectric material to a curing process to delineate the area and boundary of the main dielectric layer; forming a series of interleaving conductive trace layers and insulative layers on the top surface of the main dielectric layer; forming at least one conductive trace layer on the bottom surface of the main dielectric layer. Exposing the dielectric material to a curing process may comprise irradiating the dielectric material with an illumination source. Exposing the dielectric material to a curing process may comprise partially curing the main dielectric layer. Forming each of the conductive trace layers may be performed by depositing conductive material using direct-write method and at least partially curing the conductive material. The method may further comprise forming vias by forming holes in selected dielectric layers and depositing conductive material into the holes. Forming vias may comprise forming each dielectric layer by forming dielectric sub-layers having holes defined therein, and depositing conductive substance in holes of each sub-layer. Forming holes may comprise forming holes having oblique side walls. Forming holes may comprise depositing soluble material to define the holes prior to forming each insulative layer and removing the soluble material after forming each insulative layer.

**[0036]** The method may further comprise forming at least one of: pad coating, solder mask, and legend. Forming each of the insulative layers may comprise repeating operations of forming a sub-layer of fractional thickness of the insulative layer and curing the sub-layer prior to forming the next sub-layer. The method may further comprise forming holes in each sub-layer and depositing conductive material into the holes after curing the sub-layer. Forming holes may comprise varying the diameter of the holes in each sub-layer so that the resulting holes in each insulative layer comprise oblique sidewalls. Depositing conductive material may comprise coating sidewalls of selected holes and completely filling other holes. The method may further comprise performing electrical testing to verify functionality of the PCB. The method may further comprise concurrently forming a second functional PCB by: exposing the dielectric material to a curing process to delineate the area and boundary of a second main dielectric layer concurrently with forming the main dielectric layer; forming a series of interleaving conductive trace layers and insulative layers on the top surface of the second main dielectric layer; and,

forming at least one conductive trace layer on the bottom surface of the second main dielectric layer.

**[0037]** According to an aspect of the invention, a system for fabricating a printed circuit board (PCB) is provided, comprising: a central handling station comprising an extendable robot arm configured for holding a tray; at least one tray positioning mechanism positioned within reach of the robot arm and configured to accept the tray from the robot arm; at least one dielectric substance dispenser positioned within reach of the robot arm; at least one conductive substance dispenser positioned within reach of the robot arm; a curing station positioned within reach of the robot arm; and, an operator console coupled to and controlling operations of the dielectric substance dispenser, the conductive substance dispenser, and the curing station. The system may further comprise a fabrication station housing the dielectric substance dispenser, the conductive substance dispenser, and the tray positioning mechanism. The system may further comprise: a first fabrication station positioned within reach of the robot arm and housing the dielectric substance dispenser and one tray positioning mechanism; and, a second fabrication station positioned within reach of the robot arm and housing the conductive substance dispenser and a second tray positioning mechanism. The dielectric substance dispenser may comprise a liquid dispenser; and, a developing mechanism. The developing mechanism may comprise a radiation source. The radiation source may comprise a UV light source. The conductive substance dispenser may comprise a deposition head. The deposition head may be tiltable.

**[0038]** The system may further comprise a flipping mechanism configured to flip a board fabricated within the tray. The flipping mechanism may be situated within the central handling station. The system may further comprise a processor receiving and converting PCB fabrication data into control instructions for controlling operations of the dielectric substance dispenser, the conductive substance dispenser, and the heating station, and further transforming the control instructions to vary parameters of the PCB fabrication data. The system may further comprise a release mechanism operable to release a fabricated board from the tray. The system may further comprise a release agent dispenser positioned within reach of the robot arm. The system may further comprise a cleaning mechanism configured for cleaning substance undeveloped by the developing mechanism. The system may further comprise a solder mask applicator within reach

of the robot arm or a transfer robot. The system may further comprise a legend applicator, a pad coater, and/or electrical component assembly unit within reach of the robot arm or a transfer robot.

**[0039]** In the system, the release mechanism may comprise a tray opening mechanism. The system may further comprise a controller dynamically varying the focus of the radiation source. The system may further comprise a heater for heating the tray. The fabrication station may comprise an inert gas environment. At least one of the first and second fabrication station may comprise an inert gas environment. The tray may comprise a plurality of lockable sub-trays.

**[0040]** According to an aspect of the invention, a system for fabricating a printed circuit board (PCB) is provided, comprising: at least one dielectric subsystem for dielectric layers fabrication; at least one conductor subsystem for conductive layers fabrication; a curing subsystem; an operator console controlling operations of the system; and, a transfer mechanism for transferring the subsystems to one or more PCB work pieces. The dielectric sub-system may comprise: a liquid dispenser; and, a developing mechanism. The developing mechanism may comprise a radiation source. The conductor subsystem may comprise a printer head. The system may further comprise a chamber having inert gas environment during fabrication. The system may further comprise a fabrication tray housing the one or more PCB work pieces. The curing subsystem may comprise an oven. The curing subsystem may comprise a heater for heating the tray. The liquid dispenser may comprise a plurality of nozzles. The conductor subsystem may comprise a plurality of deposition heads. The conductor subsystem may comprise a seed layer dispenser and a conductive trace fabricator. The seed layer dispenser may comprise at least one deposition head and the conductive trace fabricator comprises an electroplating subsystem.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

**[0041]** The accompanying drawings, which are incorporated in and constitute a part of this specification, exemplify the embodiments of the present invention and, together with the description, serve to explain and illustrate principles of the invention. The drawings are intended

to illustrate major features of the exemplary embodiments in a diagrammatic manner. The drawings are not intended to depict every feature of actual embodiments nor relative dimensions of the depicted elements, and are not drawn to scale.

**[0042]** Figures 1 and 1A depict an example of a PCB fabrication system according to an embodiment of the invention.

**[0043]** Figures 2A and 2B illustrate radiation exposure according to embodiments of the invention.

**[0044]** Figures 3A and 3B depict dielectric layer fabrication according to an embodiment of the invention.

**[0045]** Figure 4 depicts an example of a PCB fabrication system according to another embodiment of the invention.

**[0046]** Figure 5 depicts an example of a PCB fabrication system according to yet another embodiment of the invention.

**[0047]** Figure 6 is a flow chart illustrating a PCB fabrication method according to an embodiment of the invention.

**[0048]** Figure 7A is a flow chart illustrating a PCB fabrication method according to another embodiment of the invention, while Figure 7B illustrates an example for layer registration.

**[0049]** Figure 8 depicts an embodiment of a system manager according to an embodiment of the invention.

**[0050]** Figure 9 illustrates a top view of a tray, as it is utilized for fabrication of PCB with a supporting frame, according to an embodiment of the invention.

**[0051]** Figure 10 illustrates a flipping mechanism according to an embodiment of the invention.

**[0052]** Figure 11 illustrates a process for data conversion and transformation according to an embodiment of the invention.

- [0053]** Figure 12 illustrates an example of a dielectric fabrication station according to an embodiment of the invention.
- [0054]** Figure 13 is a flow diagram summarizing the dielectric layer processing according to embodiments of the invention.
- [0055]** Figure 14 illustrate an example of a dielectric layer formed together with soluble material according to an embodiment of the invention.
- [0056]** Figure 15 illustrate various via structures according to embodiments of the invention.
- [0057]** Figure 16A is an abstract process diagram for via metallization and Figure 16B is a side view of a fabricated PCB according to an embodiment of the invention.
- [0058]** Figures 17A-17C illustrates via fabrication according to embodiments of the invention.
- [0059]** Figures 18A and 18B illustrate an embodiment of via metallization by filling the via with conductive material according to an embodiment of the invention.
- [0060]** Figure 19 illustrates three different via formations with or without the assistance of soluble material, according to an embodiment of the invention.
- [0061]** Figure 20 illustrates an example where the deposition head is tilted with respect to the tray.
- [0062]** Figure 21 illustrates another implementation of a system according to an embodiment of the invention.
- [0063]** Figures 22A-22E illustrate fabrication of several PCB's of different design on a single tray.
- [0064]** Figure 23 illustrate an example of a section of improved curing PCB, fabricated according to an embodiment of the invention.

**[0065]** Figures 24A and 24B illustrate an example of data transformation leading to changes in the geometric layout of the conductive traces so as to provide performance correlation to conventionally fabricated traces.

**[0066]** Figures 25A and 25B demonstrate combination of the methods according to the invention wherein the traces T1', T2' and T3' were thickened, and deposited into pre-fabricated recesses in the dielectric layer.

**[0067]** Figures 26A and 26B illustrate via transformation according to an embodiment of the invention.

**[0068]** Figures 27A and 27B illustrates transformation of dielectric layer Li of a PCB design, according to an embodiment of the invention..

**[0069]** Figures 28A and 28B illustrate an embodiment of the invention wherein the dielectric layer Li was transformed to three separate dielectric sub-layers.

## **DETAILED DESCRIPTION**

**[0070]** Various embodiments of the invention are generally directed to an innovative apparatus and method for Printed Circuit Board (PCB) prototyping and/or manufacturing. The apparatus is a single fully-automated, digital, integrated system that fabricates a complete functional PCB bare board, and optionally assembles electronic components on it. In some instances the system is capable of fabricating several PCBs concurrently. The fabricated PCB has insulating layers, conductor traces, metalized vias, and sacrificial holes just as a conventional PCB, except that all of these elements are fabricated using novel processes and fabrication system.

**[0071]** The system may be operated by one person to fabricate a fully functional PCB in a matter of hours, rather than days. Use of toxic and/or hazardous materials is avoided or minimized substantially, so that the system may be placed in an R&D facility for in-house prototyping of PCBs. Conventional tooling and requirements for masks and stencils are also avoided, so that the system can be a low-labor, quick turn-around alternative manufacturing

system for industrial PCB manufacturing facility. This delivers great benefits to electronics R&D operations, such as significant labor and cost savings, and time to market reduction, as well as the security aspect of keeping sensitive design in house during early development stages. Moreover, it enables fast and on-site response to design errors discovered during prototype testing without accumulating bugs. Another important feature is the option to divide on-board testing between separate teams and different setups (e.g. analog, digital, DC, RF) for opening bottlenecks, at minimal additional cost. These exemplary benefits and others not mentioned here will improve flexibility and integrity of PCB R&D process tremendously, turning fabrication of a PCB prototype from a burden to be avoided (as it is today) to an essential tool for simplifying and shortening PCB development process.

**[0072]** The system also delivers great benefits to PCB manufacturers, enabling very efficient fabrication of relatively small orders (e.g. prototypes, NPI) in very short time, thus giving a competitive edge to PCB manufacturers by cutting off response times to customers, while reducing the set-up efforts and the manual labor required for a manufacturing job. Other features and advantages would become clear from the following detailed description.

**[0073]** Figure 1 depicts an example of a PCB fabrication system 100 according to an embodiment of the invention. As shown in Figure 1A, which is focused on a central handling mechanism comprises a rotating table 110, positioned centrally in the system 100. An extendable arm 115 is affixed to the rotating table 110, and a tray holder 120 is connected at the end of the extendable arm 115 so as to hold tray 125. The rotating table 110, extendable arm 115, and tray holder 120, enable the system to place tray 125 at any of the stations surrounding the rotating table 110. In this illustration, the PCB 180 was lifted from tray 125 and flipped by flipping mechanism 185, which will be described further in detail. As can be understood, the invention is not limited to the use of these elements, and any other robotic system may be used to accomplish this task. In this embodiment, and corresponding to Figure 1, the stations surrounding table 110 are dielectric fabrication station 130, curing station 135, e.g., an oven, conductor fabrication station 145, and cleaning station 140. An extraction conveyor 160 may optionally be provided to extract the completed boards.

**[0074]** Each of the stations may include provisions for fabrication under given ambient and/or cleanliness conditions, e.g., vacuum environment, inert gas environment, e.g., argon, nitrogen, etc. Also, a main operator console 150 provides overall automated process management and user interface, and controls the operation of the various stations and tray handling mechanism of the system 100. The console 150 may alternatively be a remote station that controls several fabrication systems 100. Of course, any number of stations may be provided in the system, and the disclosure of the particular stations in this and other embodiments described herein is for illustration purposes and is not limiting the scope of the invention.

**[0075]** The system also includes cartridges 170 containing consumable fabrication material, which is stored under proper conditions. Proper material preparation equipment (not shown), conditions the fabrication material prior to usage by, e.g., heating, stirring, etc. The fabrication material may be in liquid or powder form and includes dielectric and conductor fabrication material. Other fabrication material that may be included are conductor coating, colored dielectric (e.g., for legend printing), resistive material, solder mask material, soluble material, lead, solder paste, water, cleaning solution, etc.

**[0076]** Detailed explanation of the various stations and their operation will be provided below. However, the general fabrication process of system 100 proceeds as follows. Standard CAD and/or CAM (computer aided manufacturing) files for bare board and optionally assembly files are uploaded (meaning, the system works with the same input which is sent today to PCB factory, as in common practice of PCB manufacture), onto the main operator console 150. The files are then converted and transformed into a fabrication file providing machine instructions for fabricating a fully functional PCB. Software simulation of the CAD may optionally be provided, including interaction with the user, e.g., inquiring whether trimming is needed for the specific design, control impedance values and other queries concerning design for manufacturing (DFM). The fabrication starts by the rotating table 110 placing the tray 125 into the dielectric fabrication station 130. There, a radiation-curable liquid composition is poured, sprayed, deposited, etc., into the tray 125.

**[0077]** Notably, in this specific embodiment a radiation curable liquid is used; however, as will be understood from the subject specification, other material forms may be used, such as, e.g., powder, or even solid (e.g., by turning the solid material to liquid, selectively). Moreover, the liquid may be curable by means other than radiation, such as, e.g., thermal curing, chemical curing, etc. In this respect, in this specification the term “cured” or “curing” refers to partial or complete curing, as the case may be. That is, various layers at various stages of fabrication may be cured to a given level, which may be controlled by the process management so that specific curing may be tailored to specific designs and specific material characteristics. Therefore, unless the term “fully cured” is used, the term “cured” in and of itself may mean partial or fully cured.

**[0078]** The liquid composition spreads evenly about the tray 125 to form a thin layer of resin. In some embodiments (not shown here) various means are used to ensure that the resin is spread evenly. A radiation source, e.g., a UV light source (shown in Figure 2), is then utilized to irradiate the liquid so as to delineate the shape and boundaries of the PCB. The radiation cures the irradiated area into a hardened dielectric material.

**[0080]** In this regards, one should note that a board layer, e.g., a dielectric layer, may comprise several fabricated layers. For example, one insulative board layer may comprise of several dielectric layers fabricated one on top of the other by the method described above. The total thickness of a board layer would be dictated by the required properties of the design, e.g., electrical insulative or mechanical properties. Furthermore, the tray, when positioned in the dielectric fabrication station, is capable of z-axis movement for adjusting distance from the spreading device with thickening of the fabricated PCB (e.g., once a layer has been spread and the PCB has been thickened, the tray is moved down in correlation to the thickness gained). Alternatively, the spreading device may be capable of z-axis movement for compensating the thickness gained during fabrication.

**[0081]** Figures 2A and 2B schematically illustrate the tray 225 filled with liquid 260 and being exposed to radiation. A radiation source, such as a UV laser 265A or a lamp 265B is used to radiate the liquid 260 to delineate the shape of the PCB and expose its entire area to radiation. Notably, locations of vias or other holes and other geometric patterns (e.g. trenches for conductive traces) are not irradiated, so that after curing and cleaning the holes are open and are

ready to accept conductive material. In this embodiment, the cleaning station 140 is used for removal and cleaning of resin that has not been radiated, such as resin at locations of vias, etc. However, in other embodiments of the invention, the dielectric fabrication station may deposit the dielectric material selectively (i.e. only on locations that requires curing and hardening of the material) and then perform curing, thereby not requiring a following step for removal and cleaning of uncured resin.

**[0082]** In Figure 2A, a writing mechanism is used to direct the light beam from source 265A to “write” the desired PCB shape, while in Figure 2B a dynamic mask 275 is used to transfer the desired shape by casting light through the mask and onto the liquid 260. Of course, other techniques may be used without departing from the scope of the invention. Since any shape may be generated by the radiation exposure, the system may even fabricate several PCBs 270 in parallel, as shown in Figures 2A and 2B. That is, once the exposed area 270 is cured, it forms the basis for a PCB. In essence, this step generates a substrate for PCB fabrication, thereby eliminating the need for a conventional starting substrate, such as a CCL.

**[0083]** Once the areas delineating the PCB on the first dielectric layer have been fully exposed to radiation, the tray may optionally be transferred for processing in the curing station, e.g., oven 135. Alternatively, thermal curing may be performed only after several layers have been fabricated. Thence, the tray is transferred to conductor fabrication station 145. At conductor fabrication station 145 conductive traces are deposited and via holes are metalized using, e.g., inkjet-like printing technology. After the printing, the conductive material may be cured using, e.g., sintering, and the tray may again be transferred to the curing station 135 for thermal curing if needed. Fabrication of conductive traces may be followed by testing, e.g. optical inspection of the conductive traces, to validate accuracy of conductor deposition and correlation to the fabrication instructions provided. Possibly, electrical testing for conductivity may follow, to validate electrical performance of the deposited conductors. Then, the tray is returned to the dielectric fabrication station 130, and a second layer of radiation-curable liquid composition is poured onto the tray. Cleaning and/or washing steps may be performed before or after each of the fabrication steps (e.g., by cleaning station 140), as needed.

**[0084]** The radiation source is again activated to expose areas of the insulating layer that should be cured to form an insulator above the conductive traces layer. Again, locations of vias or other holes and other geometric patterns (e.g. trenches for conductive traces) are not irradiated, so that after curing and cleaning the holes are open and are ready to accept conductive material. The tray may then again be processed at the curing station and transferred to the conductor fabrication station to metalize or deposit conductive material in the vias and generate the second layer of conductive traces. In this regards, some vias may be coated on their sidewalls only, while others may be completely filled with conductive material, as determined by the fabrication instructions.

**[0085]** As can be appreciated, once poured, the liquid resin spreads so as to naturally form a flat top surface. This is an advantageous feature of this embodiment of the invention. That is, at the end of fabrication of sandwiched conductive layer and dielectric layer, the top surface is flat, enabling easy fabrication of another conductive layer. In some circumstances, however, further flattening may be required using, e.g., forced leveling mechanisms such as blades, etc. An example is shown in Figures 3A and 3B, wherein a first layer of resin 310 has been cured, a conductive trace 315 has been deposited thereupon, a via 340 has been wall-coated with conductive material 350, and a second layer of resin 320 has been deposited on top, all within tray 325. In Figure 3A the insulation layer 320 has been exposed to radiation to delineate vias 330, while in Figure 3B the vias 330 are shown after they have been cleaned from excess, uncured resin 320. Once the structure of Figure 3B has been cured and optionally baked, it provides a flat top surface for deposition of the second metal layer, including deposition of conductive material into vias 330. As can be appreciated, obtaining the flat top may require some "relaxation" time (depending on viscosity, surrounding temperature etc.) to allow the liquid to spread evenly.

**[0086]** The above processing proceeds iteratively to generate as many metal tracing layers as desired. Then, the cured PCB is flipped using, e.g., flipping mechanism 185 on the rotating table 110, and the above sequence is repeated so as to generate conductive traces and pads on the bottom side of the PCB, as most PCBs have conductive layers both on the top and the bottom external surfaces. Any kind or number of layers (including dielectric layers) could be

fabricated on the bottom side of the PCB, provided that the first dielectric layer has been fabricated. Additionally, the PCB may be flipped as needed in fabrication process, according to fabrication order desired. As shown in Figure 1, the entire process may be monitored using cameras and other control means (not shown in the drawing). In this manner, a double-sided PCB (i.e. PCB with conductive elements on both outermost external sides. As can be appreciated, further conductive layers could be fabricated inside the PCB, to provide a multilayer double-sided PCB) is fabricated, without the use of a substrate and without the use of conventional PCB fabrication techniques.

**[0087]** Figure 4 depicts an example of a PCB fabrication system according to another embodiment of the invention. The elements in Figure 4 are similar to those of the embodiment of Figure 1; however, the dielectric and conductor fabrication stations have been eliminated. Instead, a unitary dielectric and conductor fabrication station 430 is utilized. The fabrication process may proceed generally as described with respect to Figure 1; however, both the insulative and conductive layers are fabricated in station 430, which includes elements for dispensing the radiation-curable liquid composition and for depositing the conductive trace. For example, the unitary station 430 may include a nozzle for dispensing the radiation-curable liquid composition and a printing jet for printing the conductive traces. In this manner, efficiency is improved as transfers between conductive and insulative stations are eliminated. Additionally, issues of registration are simplified, leading to higher accuracy.

**[0088]** Figure 5 depicts an example of a PCB fabrication system according to yet another embodiment of the invention. Generally, the PCB fabrication stations of Figure 5 may be similar to those of either Figure 1 or Figure 4, except that additional stations have been added. Notably, the additional stations provide facilities for testing the completed PCB and for populating the PCB with components. These stations include a solder paste dispensing station 565, an electrical testing station 570, and a pick and place station 575. An additional rotating table 510B is provided for handling boards for processing in the additional stations 565, 570 and 575. According to one feature of this embodiment, the curing station 535 is an oven that also serves as soldering oven. Moreover, in this embodiment oven 535 is utilized to transfer the board to the second rotating table 510B by means, such as, for example, a conveyor belt.

**[0089]** The description will now proceed with further descriptions of PCB fabrication methods according to embodiments of the invention. Figure 6 is a flow chart illustrating a PCB fabrication method according to an embodiment of the invention. The description of the process of Figure 6 will refer to the system of Figure 5, but it is equally applicable to other embodiments of a PCB fabrication system according to the invention. At 600 the proper board files, 602, custom data 604, and assembly files (if utilized) 606, are loaded onto operator console 550, and the data from these files undergo conversion and transformation into a fabrication file. Notably, in the context of this invention, data conversion relates to a change in the representation of the data to adapt it to the fabrication system. However, the design represented by the data is not modified. Thus, for example, in 600 the CAD data is converted so as to provide a fabrication file that resembles a freeform fabrication file in a way that it provides instructions for fabricating the PCB in sections, e.g., thin layers formed of cured liquid, sintered powder, etc. On the other hand, data transformation relates to modification of the original design so as to provide the intended performance of a conventional PCB, although the fabrication is done using non-conventional material and methods. Thus, the CAD data is transformed to account for, e.g., conductivity of the material used for the conductive lines and vias, dielectric constant of the cured dielectric material, etc. The transformed fabrication file also includes indication as to where an insulation material(s) and where a conductive material(s) should be deposited, exposure time, curing and/or baking time, etc., such that the resulting PCB would have properties that are highly correlated to conventional PCB fabricated using the original CAD data.

**[0090]** At 610 PCB board fabrication is performed, using the various stations of the system. As described previously, there is no substrate as a starting point, so the process begins at 611 by preparation of the tray. As is further detailed below, tray preparation is required, mainly, for facilitating release of the fabricated board (e.g., when fabrication is finished or when it has to be flipped), and may be performed, e.g., by coating the tray with release layer of soluble material. Then, a dielectric layer that serves as the starting layer of the board is fabricated in 612. The dielectric layer may be fabricated using any rapid prototyping/SFF/direct writing technique using dielectric material, such as radiation-curable liquid composition, sintering dielectric powder, etc. The dielectric layer may be cured using radiation exposure, chemical or thermal curing, etc., according to the converted and transformed design provided in the board file 602, and then the

cured or developed layer may be annealed or baked. It should be appreciated that the first dielectric layer need not be made in one single step, but rather may be made by curing or developing consecutive thin layers of liquid, powder, etc. Notably, by fabricating a first layer of dielectric material, the method of this embodiment obviates the need for a substrate as a starting material. Consequently, the PCB may be made to any size or shape desired by simply curing the starting material to the shape desired. This significant flexibility has many advantages, such as simplifying other processes within the system (e.g. low aspect ratio via metallization, by metalizing only partially height dielectric layer, as is further detailed in the following description).

**[0091]** Once the first dielectric layer is completed, the method proceeds to 614, wherein a conductive layer, or conductive traces, are deposited on the dielectric layer. Various methods may be used to deposit the conductive layer, including various direct writing or SFF methods. According to one embodiment, the conductive traces are deposited using printing technology, such as, e.g., inkjet printing technology. As with the dielectric layer, the conductive traces need not be deposited in a single pass, but rather may be constructed by printing thin layers one layer at a time. Each conductive layer may or may not be cured, be partially cured to a desired level, or baked prior to the deposition of the second conductive layer. Once the deposition of the conductive traces is completed, the PCB may be again annealed or baked. Step 616 is performed to metalize vias and any other interconnects, as needed. It should be appreciated that steps 614 and 616 could be performed in parallel (e.g., by using multiple deposition heads for conductive material; one for conductive traces deposition and one for via metallization). At 618 it is checked whether further layers are needed to be fabricated. If so, the steps 612-618 are repeated. The via metallization step 616 is performed in order to fill or coat the vias with conductive material. As explained above, fabrication of vias may necessitate further pre-processing (e.g., at station 540) to clean the vias from excess dielectric material before the metallization step 616 is performed. Also, while the term via metallization is used herein, it should be appreciated that the via may be filled or coated using conductive material which is not necessarily metal, so that the term via metallization is intended to cover such implementation.

**[0092]** The processing of 610 may be repeated on the other side of the PCB once the topside fabrication is completed. That is, once step 618 is reached and it is determined that the final layer has been fabricated, the process may check to determine whether conductive and/or insulating layers should be applied to the bottom side of the PCB. If so, in this particular example the PCB is flipped and step 610 repeated to fabricate conductive traces and insulation layers on the bottom side of the PCB.

**[0093]** When all processing 610 is completed, optional surface-finishing fabrication may be performed at 620. All stages of surface finish affect only the outermost external layers of the PCB. Thereby, surface finish phase may take place after completion of at least one outermost external layer, whether it is the top or the bottom layer of the PCB. In addition to the major surface finish stages (as described with respect to Figures 6 and 7), board painting can also optionally take place, and may be used in order to give the board an appearance similar to conventional PCBs. The coloring material may be based on epoxy. Alternatively, the dielectric material can be produced in various colors thus could be fabricated, e.g., as deep-green material, similar to most PCBs manufactured in conventional methods. In general, forming of green dielectric material is achieved by adding a pigment to the raw material during production process, or in the system, prior to deposition of the material.

**[0094]** In step 622 pad coating is provided. The phase of pad coating has important role in surface finish of the bare board, as the pads (including via holes which are designated for insert components) are the only contact points between the board and the components. Thence, a high-quality bond has to be provided between the components and some or all of the pads, both in terms of mechanical bond (e.g. pull/peel strength) and in terms of electrical bond (e.g. conductivity). Moreover, this bond must withstand various environment conditions, such as temperature variations. Such bond is usually provided by an intermediate material, which provides good interface between the component and the board's conductor, in terms of adhesion, conductivity etc. Several methods for pad coatings are known in the art, among them are HASL – hot air solder leveling (rarely used nowadays because of ROHS environmental regulation), electroless nickel/immersion gold, electroless nickel/electroless palladium/immersion gold and

other methods. All of these methods, common in conventional manufacture process, involve heavy use of chemical baths, solvents and hazardous processing.

**[0095]** The metallic bond described above is highly dependant on the material used on the board, the material used on the component, and the intermediate material bonding them together (e.g. solder flux when using soldering for components assembly). The material composition of the board is controllable during PCB production process and therefore can be adjusted between various types of surface finishes according to specific requirements of the circuit and the components. Therefore, according to a feature of the inventive process, a phase of pad coating is integrated into the process to provide several options for complying with specific application demands. For example, some boards may not require pad coating at all (e.g., pad coating may not be necessarily important to fabrication of some types of prototype PCBs), or simple coating such as organic solder preservative (OSP). Advantageously, OSP preserves the conductor surface from oxidation until it is soldered. On the other hand, for boards using features which require more complex coating (e.g. ENIG coating – electroless nickel immersion gold), such as chip on board applications or ball grid array (BGA) components, a corresponding pad coating is provided. Embodiments of the inventive system use the conductive fabrication station (e.g., station 545 in figure 5) for pad coatings, optionally with adapted material(s) for pad coatings, such as nano-silver, nano-gold ink or other similar materials. It is further important to note that the method of coating in the inventive process may vary according to the specific material used for conductors and pads, and the target application required. Also, since in the inventive method the conductive material may differ from the copper used in conventional PCB manufacture, pad coating may be performed with different materials, in order to provide the adequate material interface between the components and the board.

**[0096]** In step 624 a solder mask layer is fabricated on one or both sides of the PCB, on the uppermost surfaces of the board. Solder mask goals are mostly to insulate the external surfaces of the PCB and keep solder bridges from forming between the exposed traces (where no solder is required). Solder mask fabrication is a supported feature of the inventive system, although not necessarily required for some of the designs, and thus not necessarily implemented. In conventional PCB manufacturing methods, solder mask of Liquid Photo Imageable (LPI) is

screened onto the board and put in an oven for drying. Thereafter, the board is exposed to a light source and then developed to remove unexposed mask. A final baking of the board is required for curing of remaining mask.

**[0097]** According to embodiments of the invention, solder mask may be applied additively and without the use of masks, as opposed to conventional solder mask appliance method described above. According to one embodiment, solder mask is applied by depositing thin layer of the dielectric material (or a close variation of it, which may also be colored) using SFF machinery. For example, the dielectric fabrication station 530 may be used to deposit desired solder mask geometry, as received from the fabrication files. Alternatively, the solder mask station may utilize digital inkjet-based system, which applies solder mask in an additive manner by using highly accurate ink-jet printing of low viscosity ink. The printed ink provides properties similar to the solder mask used in conventional fabrication processes. For further information relating to this technology the reader is directed to US patent 6,754,551. Furthermore, other methods not described here could also be used for solder mask appliance.

**[0098]** Then a legend is fabricated at 626. The purpose of legend is to apply a nomenclature to aid in assembly. It generally consists of little white labeling of component that makes manual assembly significantly easier. Although not a needed feature for functionality of the PCB, it is supported by the inventive system and may be implemented according to the specific application requirements. In conventional method, legend is applied by screening onto the panel using a screen stencil, e.g., silk-screen, made from the legend film tool. The process is completed by curing in an oven.

**[0099]** According to embodiments of the invention, one of the following methods may be used for applying legend. According to one embodiment, the dielectric fabrication station 530 may be used with appropriate material for legend appliance. For example, thin film direct writing apparatus may be used for solidifying colored version of the dielectric material (preferably white colored, as is common in conventional PCB fabrication). The dielectric material may be colored by adding a pigment during production process. However, other materials may be used, provided they withstand further process steps (e.g. component soldering with high temperatures). Yet another embodiment utilizes ink-jet printing technique for legend

appliance, with proper adjustments and modifications for the inventive system. For example, the digital legend printer system LGP-809 manufactured by Printar, of Rehovot, Israel could be used. Alternatively, legend could also be applied by the conductive fabrication station, e.g. station 545 at figure 5. Furthermore, other methods not described here could also be used for legend appliance.

**[00100]** Summarizing surface finish phase 620, it should be appreciated that according to preferred embodiment of the invention, all steps in this phase (including pad coating at 622, solder mask appliance at 624 and legend appliance at 626) are performed using the dielectric fabrication station 530 and the conductive fabrication station 545, which are also used for board fabrication. Consequently, surface finish processes, conventionally performed by several additional machines (i.e. in conventional manufacturing process, there are several dedicated machines for legend, several dedicated machines for solder mask etc.), are advantageously performed by multi-purpose stations, thereby simplifying fabrication process and improving efficiency.

**[00101]** When steps 620 are completed, the PCB fabrication is basically completed and a bare PCB has been manufactured. Optionally, at step 630 the PCB is taken to station 570 for electrical testing. Board checking and/or testing will validate the board's intactness and functionality. It includes, mainly, resistivity and continuity checking with respect to permitted current flow, etc. Testing may be done by machinery used in nowadays relevant industry, such as flying probe testers. Possibly some adjustments may take place in order to achieve compatibility with embodiments of the inventive system, and adding other testing functions required to the fabricated board. Of course, other process verification and other tests may also be included in the various phases of the inventive machine. If the fabricated PCB has passed testing, a bare, fully functional PCB is provided at 640.

**[00102]** As illustrated in Figure 5, embodiments of the invention also contemplate integrating component assembly in the system. The assembly process 650 may be provided in modular fashion, so that component assembly machines may be integrated into the system. At this point, the PCB undergoes solder paste deposition 652, and is moved to solder paste deposition station 565, in order to coat the relevant parts of the board (e.g. pads) with soldering

material (e.g. soldering paste), crucial for the component assembly. According to embodiments of the invention, solder application may be performed in an additive manner, without the usage of masks and stencils. For that, an automatic high-accuracy solder-paste dispensing system may be used. Alternatively, other components of the system, e.g., the dielectric or conductive stations, may be used for paste dispensing. Solder will be dispensed in accordance with proper assembly data received and processed in data conversion and transformation phase.

**[00103]** For components population at stage 654, embodiments of the system may use conventional low-volume surface mount device (SMD) pick & place machines (e.g. pick and place machine 575), and may be subjected to modifications, with respect to the inventive system and substrate materials considerations. According to customer demands, through-hole components placement machinery may also be used. Soldering stage 656 may be performed in a conventional reflow oven. In one embodiment, the system will use dedicated reflow oven (or any other type of oven) for soldering. Alternatively, soldering could also be performed in the curing station 535. For example, in this exemplary embodiment, the curing station 535 is an oven that also serves as a soldering oven.

**[00104]** Figure 7A is a flow chart illustrating a PCB fabrication method according to another embodiment of the invention. The various steps of Figure 7A are somewhat similar to those of Figure 6, except that according to the method of Figure 7A the PCB is not made by iterative fabrication of dielectric and metallic layers, but rather by fabricating separate dielectric layers, forming conductive traces and vias upon each layer, and then fusing the layers together. For example, each separate layer may comprise several bonded dielectric sub-layers (which are bonded together, constituting a single dielectric layer having metallic traces deposited thereupon, on one or both sides). Such a layer may be thought of as one laminate layer, and all of the laminate layers are then fused or bonded together with intermediate dielectric substance (IDS) (such as prepreg etc.) to form the completed PCB.

**[00105]** An IDS has two main purposes: firstly, for isolation of electric intermediate conductors between adjacent layers (excluding vias) and, secondly, layers adhering (relevant at lamination stage). IDS layers may be processed in order to match the geometry of the surrounding dielectric substrates (e.g. form holes in the IDS which correspond to holes in the

surrounding substrates by carving/drilling/laser drilling/solid freeform fabrication etc.). IDS processing (not shown in figure 7A) may take place in parallel with dielectric fabrication process, thus shortening overall fabrication time. This is a repetitive process, as each multi-layer board contains several IDS layers which are used as intermediate layers between the dielectric layers.

**[00106]** At 700 the proper board files, 702, custom data 704, and assembly files (if utilized) 706, are loaded onto operator console 550, and the data from these files undergoes conversion and transformation into a fabrication file. The fabrication file somewhat resembles a freeform fabrication file in a way that it provides instructions for fabricating the PCB in sections, e.g., thin layers formed of cured liquid, sintered powder, etc. The fabrication file also includes indication as to where an insulation material and where a conductive material should be deposited, exposure time, curing and/or baking time, etc.

**[00107]** At 710 PCB board fabrication is performed, using the rotating table and the various stations of the system. As described previously, the process begins at 711 by preparation of the tray. Then, a dielectric layer is fabricated. The dielectric layer may be fabricated using any rapid prototyping technique using dielectric material, such as radiation-curable liquid composition, dielectric powder, etc. The dielectric layer may be cured using radiation exposure, sintering powder, etc., according to the design provided in the board file 702, and then may be annealed or baked for further curing. It should be appreciated that the first dielectric layer need not be made in one single step, but rather may be made by curing or exposing consecutive thin layers of liquid, powder, etc. Notably, by fabricating a first layer of dielectric material the method of this embodiment obviate the need for a substrate as a starting material. Consequently, the PCB may be made to any size or shape desired by simply curing or exposing the starting material to the shape desired.

**[00108]** Once the first dielectric layer is completed, the method proceeds to 714, wherein conductive traces are deposited on the dielectric layer. Various methods may be used to deposit the conductive layer, including various direct writing and rapid prototyping methods. According to one embodiment, the conductive traces are deposited using printing technology, such as, e.g., inkjet printing technology. As with the dielectric layer, the conductive traces need not be deposited in a single pass, but rather may be constructed by printing thin layers one layer at a

time. Each conductive layer may or may not be cured prior to the deposition of the second conductive layer. Once the deposition of the conductive traces is completed, the layer may be again annealed or backed. At step 716 vias metallization is performed, although, as explained above, via metallization may be performed together with metal tracing. At 718, automated optical inspection (AOI) is performed on the layer, validating tight correlation of deposited conductive traces to the fabrication file.

**[00109]** At step 713 it is checked whether further layers are needed to be fabricated. If so, the steps 712, 714, 716 and 718 are repeated. Otherwise, the processing proceeds to 715, wherein the individual layers fabricated are aligned and stacked. Fiducial marks may be provided on the layers to assist in alignment of the layers. The stack may then be fused or bonded together using, e.g., conventional annealing or bonding techniques. Alternatively, the layers may be attached together using a final polymerization and/or final curing step, thereby hardening the structure by fully-curing it. Once this step is completed, the processing proceeds the same as described with respect to Figure 6.

**[00110]** Figure 7B illustrates an embodiment facilitating alignment and registration of separate board layers, with respect to fabrication method described in figure 7A. Figure 7B is a side view, focusing on two adjacent PCB dielectric layers 700A and 700B that are aligned and registered together. Both the layers are covered with conductive traces 780. The layers are registered with IDS layer 720 in the middle. While utilizing solid freeform fabrication for dielectric layers fabrication, micro-geometrical aids for registration are fabricated on adjacent layers, for facilitating registration and gaining improved accuracy. These could be correlating pins 760 and sockets 740. The registration aids will be added to the fabrication file in data transformation phase, and will be limited to dielectric layer areas which are free of conductors and other features.

**[00111]** Various elements and steps of the PCB fabrication according to various embodiments of the invention will now be described in further details. As explained with respect to Figure 1, the main operator console 150 includes a central computing unit for operating the various components of the system. The central computing unit, schematically illustrated in Figure 8 and sometimes referred to herein as system manager (SM 800), may be composed

mainly of the following components. A process manager (PM 805) is responsible for overall management and supervision of the fabrication process (e.g., as a transaction), including sub-processes synchronization and coordination, process control, e.g., motion axes control, temperature levels, ramp-up and ramp-down over time, etc. Intra-machine communication interfaces 810 connect to some or all of the sub-components of the system. Some sub-components in the system may have independent process management and graphical user interface (GUI) embedded in it. Memory unit 815 stores algorithms for process (serial and parallel coordination and others optimized for efficiency, etc.) and other related data. For example, the memory unit 815 may store log files, video documentation of the fabrication process or relevant parts of it preconfigured or set manually, i.e., the cameras may have two functionalities – image processing dedicated internally for the manufacturing process and for fabrication documentation.

**[00112]** The algorithm may provide support for parallel processing of more than one board and/or more than one design. The algorithms may also perform preliminary analysis for fabrication request regarding estimated finish time, material cartridges sufficiency, estimated size variations (if any), mechanical variations, like shaping metal-trace trenches, via formatting, cure heating tunnels, thickness of conductive trace, thickness of layer, improving conductivity (e.g., by additional processing), electrical properties variations (may include requests for some additional parameter inputs from the user, such as working frequency) and others. LAN/WAN communication interfaces 820 are used for requests reception, remote configuration, queries of all sorts, etc. The system may include further external or internal communication interfaces (physical and or logical) as needed.

**[00113]** The system manager 800 may further include independent control and error recovery unit 825, responsible for external fabrication process supervision, error handling and recovery, etc. An operator GUI 830 provides the user with a configuration panel for calibration, fabrication setup, etc., fabrication process reports, operator log reports, system status reports, error reports, statistics, etc. A technician GUI 835 may be provided separately from the user GUI 830, providing access to all operator GUI abilities and advanced configuration panel for

system components and technician level log reports, errors, ability to access sub component directly and monitor and affect the process real time, etc.

**[00114]** In general, the system manager 800 manages and supervises the entire system, and might consist of all components described above or some of them, as well as other various components as needed. The system manager 800 may also support fabrication requests priority queuing, thus enabling receiving of multiple requests simultaneously.

**[00115]** The system manager controls operation of the system, including the central robot for handling the tray and moving it from station to station. The central robot may be based on conventional robots, such as the atmospheric robot Reliance ATR, available from Brooks Automation of Chelmsford, MA, or the Pro Six PS3, available from Epson Robots of Carson, CA. In the embodiment of Figure 1A, the central robot comprises a rotation table 110, extendable arm 115, and tray holder 120. The rotating table may be any conventional high-accuracy rotating table, such as Rundtakt available from Taktomat, of Pöttmes, Germany. Regardless of the actual implementation, the central robot needs to accurately place the tray at each station.

**[00116]** Accurate placing of the tray may also be facilitated by the design of the tray itself. Since the tray is transferred between stations, it may have adequate mechanical interface to the other stations, including the central robot mechanism and the flipping mechanism. As PCB positioning at each station should be highly accurate (in the range of few microns) during fabrication, the issue of anchoring and alignment is also important, especially when transferring the board between different stations. In one embodiment, two levels of tray alignment are provided. First, accurate alignment of the tray to stations' work surface is ensured. The stage may be anchored with state of the art mechanisms to the working surface of each station (many accurate anchoring methods are known, e.g. electromagnet anchoring, air pressure, vacuum).

**[00117]** Additionally, embodiments of the invention also ensure accurate alignment of the PCB within the fabrication tray. That is, once the first layer is exposed in the dielectric fabrication station, the coordinates of the exposed PCB with respect to the tray must be maintained, i.e., the PCB should not be able to move within the tray. Moreover, the PCB needs to be flipped for multi-layer, double-sided PCB fabrication. Therefore, the alignment

mechanism needs to ensure that the flipped PCB is returned to the tray at the proper alignment and in planer fashion for further processing.

**[00118]** According to one embodiment, PCB anchoring is obtained by using vacuum orifices positioned in defined positions on the fabrication tray. The vacuum orifices are operated by central vacuum system connected to some or all of the stations, as well as to the rotating table. The PCB will be anchored to the tray by operating the vacuum system. The vacuum orifices may be sealed by pistons in order to keep the fabrication surface planar (particularly during fabrication of first dielectric layer). Alternatively, other methods for anchoring may be used, e.g. using side-clamps, without departing from the scope of the invention. Also, camera-aided alignment system may be installed in some of the stations, for responding to miss-positioning of the PCB in the tray caused by movement of the fabrication tray between stations. Advantageously, and particularly with the process of figure 6, since all of the stations use additive non-contact processes and don't require stencils, masks etc., correction of miss-alignment is easy and requires only software-level adaptations for altering the coordinates of e.g., alignment marks. Notably, when misalignment of the tray is detected, the tray does not need to be mechanically re-positioned. Rather, once the misalignment is measured, the system manager may shift the coordinates of the next layer by the proper amount to correct for the misalignment. That and more, this method introduces great benefits compared to conventional PCB fabrication processes, which require mechanical alignment of all layers together. Specifically, the inventive system enables alignment for every layer (or even sub-layer) fabricated, thus errors accumulation is negligible, enabling fabricating boards with numerous layers and delicate features in a highly accurate manner.

**[00119]** Figure 9 illustrates a top view of the tray, as it is utilized for fabrication of PCB with a supporting frame, according to an embodiment of the invention. The supporting frame introduces several benefits, including easier handling, easier alignment, easier release, and easier flipping, as will be described below. The PCB 920 is formed in the middle of the tray 900, and includes supporting frame elements 925, which will be removed upon completion of the fabrication of the PCB. The supporting frame elements 925 enable easier handling and securing of the PCB, since mechanical devices may be utilized to secure the PCB in place by contacting

the supporting frame elements 925. The mechanical securing devices may be fitted to fixed model dimensions, regardless of actual fabricated PCB size. For instance, vacuum orifices could be just beneath the supporting frame and not across entire fabrication surface. According to such an embodiment, the supporting frame elements are of the same size and location regardless of the size of the PCB, while linking elements 935 connect the PCB to the supporting frame elements 925.

**[00120]** As shown in Figure 9, fabrication of alignment marks 930 may be provided on the supporting frame 925. These may be provided on the top surface of each dielectric layer. For the first dielectric fabricated layer alignment marks may also be provided on the bottom surface for enabling alignment after flipping the board. The alignment/fiducial marks may be placed on the same locations for each layer and may be of any shape. Notably, similar technology conventionally used for overlay alignment in semiconductor fabrication may be used, especially when the dielectric layers are transparent. The marks themselves may be made by carving fixed alignment patterns on the tray and allowing the dielectric material of the first layer to be formed in conforming shape, so as to provide alignment marks in the bottom surface. As PCB geometry is changed upon system input, these alignment marks are preferably positioned in a fabrication area not affected by the input, such as the support frame 925. Alternatively, the alignment marks on the bottom of the first dielectric layer fabricated may be formed by using soluble material as a support, to correlate with the desired geometry of the alignment marks. According to another exemplary embodiment, the alignment may be performed with specific data points on the board (e.g. fiducial holes or other circuit elements), without fabricating alignment marks.

**[00121]** The supporting frame may also be designed to enable easier rotation or flipping of the board. For example, rotation support sockets may be fabricated on the sides of the supporting frame elements, to allow rotation of the board with relatively simplistic mechanism. Figure 10 illustrates a flipping mechanism according to an embodiment of the invention. The flipping mechanism of Figure 10 may be positioned on top of the rotating table 1010 or at dedicated flipping station, etc. In this embodiment, strikers 1015 are inserted into the sockets formed in the supporting frame. The strikers may be movable in the Z-axis direction, as shown by the double-headed arrows, and may be rotated, as shown by the inward-facing arrows.

**[00122]** The tray itself should be made of material that functions properly with fabricating PCB according to embodiments of the invention. For example, when utilizing SU-8 or variations thereof as the dielectric material, the tray material needs to be compatible with the chemistry of the resin and with any temperature variation required during any annealing or baking. Also, the PCB's adhesion to the tray should also be considered, for holding board accurately in place. On the other hand, too strong adhesion can result in impossible release of board from stage, thus the choice of the right material for the stage must take adhesion into account.

**[00123]** Releasing of the PCB from the tray may be accomplished using various means. The tray material may be selected so as to have natural adhesion to the dielectric material, thus release of a relatively thin low aspect-ratio model such as a PCB should be done delicately. Various methods may be used to accomplish this task. According to one embodiment, mechanical methods are used for releasing the PCB from the tray. Some examples of such mechanisms are illustrated in Figure 10, however implementing only one such mechanism may suffice. These mechanisms include vacuum orifices (but operated in opposite direction). That is, a vacuum pump 1030 may be connected to vacuum orifices 1035 provided in the tray. For holding the board the pump 1030 is operated to generate vacuum, while for release the pump is operated in reverse so as to elevate the pressure and eject the board. Another mechanism shown in Figure 10 is lift pins, similar to lift pins used in semiconductor wafer fabrication. A lift mechanism 1050 pushes lift pins 1055 through holes 1060 provided in the tray 1005. The lift pins 1055 engage the board and lift it from the tray, whereupon strikers 1015 may engage the board. In one embodiment the lift pins are provided in a large matrix array, so as to essentially form a "bed of nails" to engage the board. Alternatively, or in addition, upper vacuum manipulator 1040 may engage the board from above and lift the board independently or in coordination with the pump 1030 or lift pins 1055.

**[00124]** Another method for assisting separation of the PCB from the tray is using heating. For instance, special material may be spread on the tray, of which adhesion to PCB is degraded upon temperature cycling. As shown in Figure 10, an optional heater element 1070 is provided so as to heat the tray 1005 to assist in releasing the board. Also, a fabric layer, such as nylon layer, may be stretched on the tray, and the board fabricated on the stretched nylon. Once the

board is released, the nylon may be pilled off from the board. Rather than using nylon, the tray may be coated by spraying, coating, printing, etc., a layer of release or soluble material as the initial layer, and then fabrication of PCB on top. The PCB is released by using heating, chemical, or other method to remove the release layer without adversely affecting the fabricated layer. In general, the release layer material may provide adhesiveness to the dielectric material, which is controlled by the process (e.g. by different temperature conditions, using release solvent). For example, soluble wax may be used as release layer material.

**[00125]** Another option illustrated in Figure 10 is having the tray made of two parts, and rotating each part as shown by arrows “R” so as to “break away” from the board. Prior to breaking away the board may be held by vacuum manipulators 1040. Other mechanical methods may be used, such as, e.g., prying the board using mechanical levers. This may be done by applying the levers to the supporting frame.

**[00126]** Figure 11 illustrates a process for data conversion and transformation according to an embodiment of the invention. Upon uploading (locally or by network) of fabrication data files containing the electrical and mechanical fabrication data (CAD and other data types), e.g. Gerber files and any other file types used for PCB fabrication, as well as inserting relevant operator inputs, a software conversion takes place. The system manager may be fitted with conventional DFM/DFA (design for manufacturing/design for assembly) processes, thereby creating simple plug and play interface with common DFM/DFA processes used conventionally in PCB manufacture. The system manager also enables convenient control and conversion of non-CAD data transferred to the system (e.g. control impedance data, conductor thickness, dielectric layers thickness and more). In some cases, design data may be uploaded to the inventive system (e.g. design routing file) instead or in addition to the fabrication data. At this stage, all of the data needed for the following stages will be derived and converted to the appropriate format(s) needed for each phase in the process, according to the relevant station.

**[00127]** The system will perform format conversion from conventional PCB fabrication files used (and any others that may be used in the future), into the input format relevant to each phase/station. Moreover, the system will also convert the non-CAD data received with the design to the relevant input format needed for the sub-system. For instance, dielectric layer

thickness values (which usually appear as raw data in PCB design files) will be combined with 2D CAD data geometry (received from layers Gerber file), to 3D CAD data designated for dielectric fabrication station.

**[00128]** Then, data transformation phase is performed on the converted fabrication file. Data transformation is distinguished from data conversion in a way that it transforms the actual dimensions and properties of the original fabrication files (rather than doing format conversion, which changes data representation but does not change the data itself), thereby creating output fabrication file of PCB which is slightly different (e.g. in dimensions, geometry) compared to the original fabrication files. Data transformation is used mainly in order to provide correlation in functionality and performance of fabricated board to its equivalent board fabricated by conventional manufacturing methods.

**[00129]** The inputs for data transformation may be standard PCB fabrication files, with original data retrieved (e.g. mechanical coordinates of layers, pads and traces, material, target parameters and more). Without departing from the scope of the invention, the input of the transformation algorithm may also be in different format and data representation from the original fabrication file. That is, data conversion may be applied prior to transformation, thereby converting format of original fabrication files. In performing the transformation, the fabrication file is changed (i.e. the data is changed, and not its representation, as is common in conversion), to reflect the inventive process requirements and in order to keep functional properties of the fabricated PCB correlated to the functional properties expected for the input fabrication file (when it is fabricated in standard mass-production process). Some of the modifications to the fabrication files may be done for each layer separately and according to graphic data contained in each layer, and some of the modifications can be done for a group of PCB layers (or even to all layers as a group). The resulting functional PCB should be correlated in functionality (as is defined by the use and target application of the PCB) to mass production PCB, and additionally to be closely correlated in external mechanical dimensions.

**[00130]** The description now turns to more detailed examples of various processing steps according to embodiments of the invention. Notably, the invented system enables the fabrication of multiple PCBs at once, e.g., multiple PCBs of a single design or multiple PCBs of different

designs, according to excess surface area left (e.g., a design of 5 x 5 cm can be fabricated up to 36 times on 30 x 30 cm effective processing area, for single fabrication cycle). The finished board may need simple separation process for detaching the finalized PCBs from each other. Alternatively, special easily-detached supports may be formed between separate boards which will be easily disconnected after completing the fabrication. Alternatively, each station may have provisions to accommodate more than a single tray, thereby enabling parallel processing of several trays simultaneously.

**[00131]** As discussed above, e.g., with respect to Figure 6, the inventive process follows a full-buildup method, building the board up from scratch, as no substrate or lamination processes are required. This is a tremendous benefit compared to conventional fabrication methods, as handling is simplified and higher accuracies can be achieved (no need for storing separate layers, intermediate layers, alignment of layers and lamination). Moreover, the use of SFF and direct writing technologies for construction of the board yields very high accuracies, thereby enable rapid fabrication of very complex multilayer PCBs, including HDI (high density interconnect) PCBs. Fabrication is finished when the board's last substrate layer is formed; meaning, the whole board is fabricated layer by layer in a sequential manner. Layers fabrication sequence proceeds as bottom-up process (meaning starting with the bottom layer, than the layer above etc.). However, layers fabrication sequence may vary according to further process steps (e.g. conductors tracing, alignment and registration methods chosen), specific types of PCBs, customers design characteristics, and other relevant considerations. Decision of how to build the PCB (meaning, order of layers fabrication) is only an example and may change upon a specific design. Each cycle, of course, is synchronized with other parallel processes running in the system in order to shorten overall running time.

**[00132]** Dielectric layer fabrication is performed according to software data derived, thereby forming a naked dielectric layer in the desired geometry (naked layer meaning no conductors or electrical components are formed or placed, only the dielectric substrate). Specifically, each layer fabrication may include: layer geometry (includes the X, Y and Z coordinates); via holes (blind vias, buried vias, micro vias, through holes); fiducial holes and other mechanical supports as needed; mechanical preparations for conductor fabrication step (for

instance, anchoring traces and pads by building trenches and lead baths); alignment marks; fiducial points; any other optional mechanical supports/aids/structures as will be needed (e.g. support frame described above).

**[00133]** As discussed above, the dielectric fabrication process is performed by SFF or direct writing. The dielectric fabrication station reads in data from a fabrication file, and lays down successive layers of liquid or powdered material, and in this way builds up the model from a series of cross sections. Thus, no drilling is involved. As drilling is a major, expensive, bottleneck in conventional PCB manufacture methods, the use of SFF technology for dielectric substrate fabrication is one of the major time, tooling and costs saving factors in the process.

**[00134]** According to embodiments of the invention, the dielectric layer is made using a specially designed dielectric material (single or complex material solutions) that is fitted to work with the proposed dielectric fabrication technology. According to one embodiment, SU-8 or a modified derivative of SU-8 (e.g. SU-8 which includes nano-composite filler) is used for fabricating the dielectric layers. The following are the major important characteristics for the dielectric fabrication material:

- a) Suitable for working with the dielectric fabrication system and technology, with respect to desired accuracies, resolutions, process speed, viscosity, planarization quality and planarization time, post-curing shrinkage etc.
- b) Has adequate material interfaces, especially relating to adhesion and bonding with coupled materials (specifically, the dielectric layer has to have good adherence to the conductive material, and to the dielectric materials itself – as it is fabricated in a layered fashion).
- c) Able to withstand all phases of the inventive fabrication process. Also, able to withstand process of components assembly and soldering, as the case may be (e.g., provide material properties such as high T<sub>g</sub> in order to withstand common soldering temperatures, which may reach the range of 250°C).
- d) Provides high correlation of electrical, electromagnetic, thermal and mechanical properties with conventionally manufactured printed circuit board dielectric material. Of course, such correlation also depends at the conductive material being used in the process. For further information regarding desired properties of dielectric materials used for PCB manufacture, the reader is directed to industry standards set IPC-41xx, which contains specifications to various types of materials according to target applications (e.g., IPC-4101, which describes specification of base materials for rigid and multilayer boards).
- e) Non-toxic and environment-friendly as possible, preferably recyclable.

Notably, the dielectric material may be mixed with other compositions for improving its properties. For instance, the use of  $\text{Cu}_2\text{O}$  (cuprous oxide) as dielectric enhancer within the dielectric material, for improving thermal dissipation, metallization, peel/pull strength of covering metal etc. Another example is by using nano-particles in order to improve materials properties such as heat resistance or thermal expansion parameters. Further, it should be noted that mixing the dielectric material with other compositions may take place during material production (e.g., a cartridge with the mixed material will be provided), or, alternatively, the final material may be mixed with other compositions in the system prior to deposition (e.g., in that case the system may have several containers for dielectric material and the compositions to be mixed).

**[00135]** According to one embodiment, a thin-film direct writing processing is utilized for the dielectric fabrication. The process starts by coating the tray with uniform, stable and planar layer of resin (e.g., SU-8), over a release layer, if such is used. Coating thickness may vary between few microns and hundreds of microns for a single layer, thus typical dielectric layer of multi-layer PCB could be formed in one coating cycle (although it could also be fabricated in several cycles of thinner layers if desired).

**[00136]** Resin coating may be performed by various methods. For example, conventional spin-coating technique may be utilized. Spray coaters, which spray planar and uniform layers of various materials with very high accuracies may also be used. Additionally, because SU-8 viscosity range is broad and can be adjusted to fit different applications, another option is to use ink-jetting process for depositing uniform SU-8 layer. For example, an  $\text{M}^3\text{D}^\circledast$  (maskless mesoscale material deposition) system available from Optomec of Albuquerque, NM, may be used. Notably, if the system utilizes an integrated dielectric and conductor fabrication station, as in Figure 4, one inkjet or inkjet bank may be used for depositing dielectric substance, while another inkjet or inkjet bank may be used for depositing conductive material.

**[00137]** The deposited dielectric substance is then exposed to radiation. For example, if the dielectric substance is a resin (e.g., SU-8), it is polymerized by exposure to UV-light. The exposure method may be maskless and tooling-free for integrating into the inventive system. Three examples of exposure methods may be referred to as vector-by-vector, integral and raster

scan. In a vector-by-vector method, conventional scanning device (e.g. scanning laser) is used, as in a commercial SLA machine. It uses an x-y motion system for moving either the laser beam, the fabrication stage itself, or both. The resolution is determined mainly by the laser spot diameter and the exposed material. The vector-by-vector apparatus may enable dynamic focusing of laser beam, thus trading off accuracy with speed and vice versa. This will enable adaptation to different model areas according to geometry. For instance, a flat area with no complex features will be fabricated using high diameter laser beam, while high-accuracy areas will be fabricated using small diameter laser beam. On the other hand, in integral laser exposure method, the entire surface is exposed in a single exposure cycle. The light from light source is shaped by using a mask or a dynamic mask generator (e.g., an LCD or mirror arrangement, such as the digital micromirror device (DMD) commercially marketed as DLP® technology by Texas Instruments, of Dallas, TX). Integral exposure has two main advantages: firstly, it is compatible with currently-used mask processing techniques (as the entire layer is exposed at once in a uniform manner, which is more similar to conventional mask exposure); secondly, it is a much faster process as large parts of the layer are fabricated simultaneously, without the need for vector-by-vector exposure of desired geometry. In a similar manner, raster exposure method may be utilized. Raster is similar to integral exposure as it exposes significant surface area. However, it does not cover the entire surface, thus scanning is applied (by moving the exposure head, the fabrication stage, or both).

**[00138]** Figure 12 illustrates an example of a fabrication station according to an embodiment of the invention. The fabrication station 1200 of Figure 12 may be utilized for dielectric fabrication. In this example, the fabrication station has an x-y-z stage 1205 supporting tray 1210. A consumable material tank 1215 contains fabrication material, such as resin, which is deposited onto the tray 1210. A radiation source, such as a UV laser, provide radiation beam. Shutter 1225 may be used to control the radiation beam. A mirror system 1230, such as a DLP® engine, serves as a dynamic illumination deflector. Additional optics 1235 may be utilized to further shape the radiation.

**[00139]** Incidentally, Figure 12 also illustrates an example of a tray positioning mechanism 1206, which may be utilized to positioned the tray and hold it in a desired location

and orientation in a repeatable manner. The positioning mechanism 1206 is only shown schematically, and any other mechanical device may be used to accomplish this task. The main issue here is to be able to repeatedly position the tray at the same location and orientation, or, alternatively, to accurately determine an offset of the tray from a given marker.

**[00140]** Depending on the process and material used, curing might need to be enhanced by heating with oven/hot-plate or other methods, to a level where it would be the most appropriate point for further fabrication of conductors on the dielectric layer. Unexposed material portions are then removed from crosslinked model (meaning sections which were not exposed by laser/light according to desired geometry). For example, resin (e.g., SU-8) may be developed in bath of PGMEA (Propylene Glycol Methyl Ether Acetate) and rinsed with alcohol. Alternatively, or additionally, mechanical methods may be utilized for removing unexposed substance. For instance, focused air and/or water and/or solvent pressure directed at the portions of unexposed material may be used to dislodge the loose material. Vacuum suction may also be utilized singly, or in combination with other methods. Suction may be combined with other methods for breaking stagnation layer of the material (e.g. spray little amount of solvent and/or ultrasonic vibrating), thus complete removal of excess material would be obtained.

**[00141]** Optionally, for finalization of curing process, a relatively long baking process, also called hard-baking, may be performed. Alternatively, hard baking may be performed only after the entire PCB has been fabricated.

**[00142]** Figure 13 is a flow diagram summarizing the dielectric layer processing according to embodiments of the invention. At step 1310 the tray is coated with the resin layer. Notably, if a releasing agent is used, the tray is coated first with the release agent and then with the resin. The coating of either may be done using spray coaters, inkjet coaters, spin coaters, etc. The resin is then exposed to radiation at 1320. The resin may be exposed to UV radiation using a vector-by-vector exposure, integral exposure, etc. If crosslinking enhancement is needed, it is performed at step 1330, which may be done using thermal treatment. The tray is then cleaned to remove excess unexposed material at 1340. This may be done, e.g., using chemical methods, mechanical methods, or combination of methods. This is followed by optional post processing, such as hard baking for finalizing the curing (e.g. crosslinking), at step 1350. As can be

appreciated, the embodiments mentioned herein with regards to the exemplary thin-film direct writing processing, are also applicable for other embodiments of dielectric fabrication (e.g., the aforementioned exposure methods, methods for removal/cleaning of unexposed material portions).

**[00143]** According to yet another embodiment, the dielectric layer is formed together with soluble material. This embodiment enables easy formation of vias and other sacrificial holes. In this example, a soluble material may be used as a convenient construction platform for the board, as well as placeholder for via and other holes while pouring dielectric material. The process of this example may proceed is as follows, with reference to Figure 14. A first station, e.g., the insulative layer fabrication station, is utilized to build a soluble material construction layer 1400. This layer 1400 may have boundaries 1405 to form a container platform for fabricating the dielectric layer. The soluble layer 1400 may be formed by SFF/RP using the same dielectric fabrication apparatus (possibly by different nozzles within the apparatus) or an independent station. Optionally, in this embodiment the soluble layer also has via place holders 1410.

**[00144]** A dielectric layer 1415 is then deposited onto the soluble container, allowing it to spread around the via place holders 1410. After depositing and curing (either partially or fully) the dielectric layer 1415, the via place holders 1410 are removed, by selectively pouring solvent on the soluble material. Furthermore, the whole construction or supports fabricated by soluble material can be washed away and removed at any time during fabrication process. This embodiment introduces several advantages, including: no need for cleaning via holes of excess dielectric material, the board is easily separated from the tray and fabrication of 3D structures that require support is enabled (e.g., the fabrication of alignment marks on the first dielectric layer fabricated). Moreover, the fabrication of 3D PCBs in complex shapes that require supports is enabled.

**[00145]** Then, a conductive layer of the PCB is fabricated. The conductive layer may include conductive traces and optionally pad coatings (only on external layers). According to software data derived, a conductive layer will be formed, on top of previously-fabricated dielectric layer. Conductive layer fabrication may include the following features: Conductive traces, involving different shapes, various widths and thickness (at X, Y and Z axis) and even

several materials. Generally, copper is used for the traces, while, gold, silver and other metals may be used.

**[00146]** The conductor fabrication station may use additive, maskless printed electronics methods and equipment for forming conductive structures. According to one embodiment, M<sup>3</sup>D technology is utilized. Other possible methods include ink-jetting, e.g., non-contact digital printing, such as piezoelectric ink-jetting of conductive fluids, as developed by Dimatix of Santa Clara, CA, laser engineered net shaping (LENS) developed by Sandia National Laboratories, or other direct writing technologies may be combined in the machine with significant elevation of accuracy and resolution. For further information on these technologies the reader is directed to U.S. Patents 7,045,015 and 6,046,426.

**[00147]** Other methods that may be utilized are by using special dispenser or paste printer for depositing high viscosity conductive paste. Also, the system may use conductive polymers, e.g., in an additive manner. The conductive polymer can be applied using the same station used for dielectric fabrication phase, or M<sup>3</sup>D system, or any other appropriate system and technology, with proper changes and modifications that may be needed.

**[00148]** According to embodiments of the invention, the conductive layer is made using a specially designed conductive material (single or complex material solutions) that is fitted to work with the proposed conductive fabrication technology. According to one embodiment, NMTI NanoSilver Ink(NTS05) by NanoMas Technologies of Binghamton, NY, or a modified derivative of it is used for fabricating the conductive layers. The following are the major important characteristics for the conductive fabrication material:

- a. Suitable to working with the conductive fabrication system and technology, with respect to desired accuracies, resolutions, process speed, viscosity, wetting angle, etc.
- b. Have adequate material interfaces, especially relating to adhesion and bonding with coupled materials. Specifically, excellent adhesion between conductive layers (thereby enabling building conductor thickness by sub-layers), good adhesion with the dielectric material as well as good bonding with components in typical component assembly process, e.g. soldering.
- c. In flex/rigid-flex applications, the conductive material has to provide some mechanical flexibility to support elongation of the board layer during bending.

- d. Able to withstand all phases of the inventive fabrication process. Also, able to withstand process of components assembly and soldering (e.g., provide material properties such as coefficient of thermal expansion (CTE) which is correlated to the CTE of dielectric material, to in order to keep board intactness under common soldering temperatures, which may reach the range of 250°C).
- e. Provides high correlation of electrical, electromagnetic, thermal and mechanical properties with conventionally manufactured printed circuit board conductive material (usually 99.8% copper is used nowadays). For instance, the conductivity of conductive layer when cured is a significant parameter for determining PCB functionality.

**[00149]** For any of the above printing methods, the system may have more than one deposition head, as each head might be designated for specific usage, for time saving and improved efficiency. For example, thick features, such as ground surface and wide traces deposition may be done with a wide nozzle, while thin features, e.g., thin traces deposition, may be done using a fine nozzle. Interconnects (vias) metallization may be done using a specialized nozzle.

**[00150]** It is important to note that all aforementioned technologies and systems may employ pre-processing, e.g., cleaning and/or heating the dielectric substrate prior to deposition, and/or post processing, e.g. cleaning and/or heating deposited material. For example, conventional M<sup>3</sup>D system supports two curing mechanisms: oven heating or laser sintering of conductive traces.

**[00151]** Via metallization may be performed by the same equipment and in parallel to conductor fabrication. The inventive system is able to metallize all kinds of vias, including buried, blind and through-hole vias. Two main metallization techniques may be used for vias: filling the via and wall coating the via. Filling the via is preferably applied to buried and blind vias, where the via is filled with fully-dense plug. Coating the via walls can be applied to all kinds of vias, and is a must for a through-hole via which is populated, e.g., with insert component. The following methods and processes described below are relevant to all metallization techniques, unless explicitly mentioned otherwise.

**[00152]** The via metallization may be achieved by one (or more) of the technologies and systems described above with respect to conductor fabrication. However, other methods may be

used for via metallization. For example, other methods include PVD (physical vapor deposition) or CVD (chemical vapor deposition). PVD is a group of vacuum coating techniques that are used to deposit thin film coatings of various materials. These technologies are used nowadays mainly for metal coatings on semiconductor wafers and hard disks, and typical fabrication processes require masks for deposition by geometry. However, PVD/CVD may be adapted to the inventive system and used for via metallization or even conductors fabrication. Of course, other methods for additive via metallization may be used.

**[00153]** Chemical methods may also be used to improve via metallization process reliability and adhesion between dielectric and conductive material. According to this embodiment, an intermediate material is sprayed, deposited or coated on the dielectric layer, thereby creating a seed layer on the dielectric layer. This material will improve adhesion to conductive material. Then, conductive material will be deposited to the vias (and possibly to the conductor tracing, thereby also improving adhesion of conductive traces with the dielectric layer), and improved adhesion will be achieved.

**[00154]** Moreover, the use of additive technology to generate the dielectric layers without the use of a substrate provides a unique opportunity to improve the structure of the vias. Figure 15 illustrates various via structures according to embodiments of the invention. As shown in Figure 15, the via sidewall is modified so as to be oblique, i.e., non-vertical sidewall. That is, most standard vias on PCBs have vertical cylindrical sidewall, since it is fabricated using conventional drilling. However, since according to the embodiment each dielectric layer is made using layering by additive technology, the shape of the sidewall of the via may be modified as shown in the examples of Figure 15 so as to assume a conical shape, a dual-conical shape, etc. The main idea behind these methods is to increase the surface area of via walls as much as possible, as well as making it more planar on x axis (i.e. supply as much horizontal surface area of the via as possible), by using various geometric manipulations. Metallization of such via holes with larger and more planar surface area is much easier to handle using additive deposition and delivers great results, i.e., critical parameters such as deposition uniformity, metal/substrate adhesion, deposited material properties (e.g. conductivity) and reliability are greatly improved, as compared to additive metallization of via holes with vertical sidewalls. Additionally, such

holes can be used for insertion of through-hole components. In that case, the shortest diameter cross-section should match the component's insert leg diameter, with sufficient spacing.

**[00155]** The exemplary methods of metallization enhancement illustrated in Figure 15 may be implemented by any of the systems according to embodiments of the invention. In particular, input CAD data analysis and transformation at the data transformation phase may include analysis of via holes surface area compared to board surface at all relevant layers. The CAD data will be interpolated according to this analysis, thus each via layout may be changed, with respect to preserving original board properties. In this manner, the board designer need not worry about the shape of the via, but rather design the board using conventional via structure. Then, when the design is loaded into the system, the data would be transformed and the data relating to the via structure would be changed to provide the selected modified via structure. The via metallization process parameters (e.g. thickness, deposition rate, material density etc.) will be set according to data interpolation in the data transformation phase.

**[00156]** One of the factors significantly affecting additive via metallization is the aspect ratio of the hole (i.e., the ratio between via height to its diameter). The higher the aspect ratio, the more difficult it is to metalize the via. According to the following embodiment, a method for facilitating via metallization is described. The method is seamlessly integrated in the inventive process (e.g. the process described in figure 6, or figure 7A), as will be further detailed below. The process is illustrated in Figures 16A and 16B. Figure 16A is an abstract process diagram, and Figure 16B is a side view of a fabricated PCB according to this embodiment.

**[00157]** As mentioned before, the inventive system fabricates the dielectric layer of the PCB using solid freeform fabrication technology, thereby enabling fabricating very thin layers of dielectric material. Thus, and as mentioned previously, one layer of the PCB could be fabricated additively, by many fabrication cycles of sub-layers. The process begins with fabrication of first dielectric sub-layer fabrication 1610, corresponding to board 1660 at figure 16B: The sub-layer d1 has been fabricated. Then, via metallization 1620 is performed on some or all of the via portions on the layer: the via v1 has been wall-coated with conductive coating c1. Afterwards, at step 1630 it is checked whether the dielectric layer of the board has been fabricated to its full height. If not, the process repeats itself, as can be seen in illustrations 1664 – 1670.

**[00158]** Once completed fabricating board layer to its full height, the process continues to conductive layer fabrication 1640 on the surface of the last dielectric layer fabricated: At 1670 the dielectric layer D has been completed to its full height (comprising d1, d2 and d3), and the via V has been also completed (comprising c1, c2 and c3). Then, the conductive layer, comprising traces t1, t2, t3 is fabricated on the dielectric layer d3 at step 1640.

**[00159]** According to another aspect of this embodiment, and corresponding to 1666, the portion of the via c2 may be coated higher than the level of sub-layer d2 and optionally to the surrounding edges, thereby creating thin annular ring of conductive material c2a. This annular ring is not used for conductance, as there are no conductors between the board layers. Instead, it is used for improved anchoring of the partial coating, and in order to provide better adhesion and support to the next portion of coating which will be fabricated. Furthermore, another important improvement being achieved by fabricating thin sub-layers is enhanced curing. Curing process of thin dielectric layers is more homogenous than on a thick layer. Therefore, improved and more accurate curing is provided to the fabricated sub-layer.

**[00160]** Figures 17A-17C illustrates via fabrication according to embodiments of the invention. Figure 17A illustrates a method of fabricating via layer by layer, having the dielectric layer formed first. At step 1710 a section of the PCB is shown, wherein a first dielectric layer d1 has a conductive trace c1 formed thereupon, and a second dielectric layer d2 with via hole v1 is formed over the conductive trace c1. In step 1712, the via hole v1 has been filled with a conductive material, and a second conductive trace c2 has been formed as well. In step 1714 another dielectric layer d3, having extended via hole v2, is formed over conductive trace c2. This process is repeated in steps 1716 and 1718 as many times as necessary to complete the via.

**[00161]** Figure 17B illustrates an embodiment wherein the full height of the via is constructed first, and then filled in the last step. As shown, in step 1720 a first dielectric layer d1 has a conductive trace c1 formed thereupon, and a second dielectric layer d2 with via hole v1 is formed over the conductive trace c1. In step 1722 a second conductor trace layer c2 is formed, but the via hole v1 is not filled with conductive material. In step 1724 a third dielectric layer, d3 is formed over the conductive trace c2, but the via hole v1 remains open. This continues as

many times as needed in step 1726, and at step 1728 the last conductor trace is formed and the via hole v1 is filled with conductive material.

**[00162]** The embodiment of Figure 17C is somewhat the reverse of the embodiment of Figure 17A. In step 1730 a first dielectric layer d1 has a conductive trace c1 formed thereupon, via hole v1. In step 1732 a conductor via CV1 is formed, prior to forming any dielectric about it. In step 1734 a dielectric layer, d2, is formed about the conductive via CV1. This continues as many times as needed in step 1736, and at step 1738 the last conductor trace is formed and may top the conductive via CV1. In any of the embodiments described herein, the vias may be filled with conductive material, e.g., by means of deposition, and then the deposited material is cured, e.g., by means of baking, focused laser sintering, etc. This results in the creation of blocked interconnects, therefore fitting only for holes not populated with through-hole components. The aforementioned embodiments of Figures 17A-17C are described as filled vias, and appear in exact height of PCB layer. It should be noted that these details are exemplary, and should not limit the scope of the invention (e.g., vias could be wall-coated rather than filled, and could be formed in any height relevant to the specific embodiment). Furthermore, it should be appreciated that the aforementioned embodiments of Figures 17A-17C also enable fabrication of wall-coated and, alternatively, filled through-hole vias (not shown in illustration). As mentioned above, filled through-hole are fabricated on a release layer of, e.g., soluble material, and not directly on the tray.

**[00163]** The deposition filling of vias can exceed the hole surface, thus forming small conductive protrusion, enabling interconnection between adjacent layers. Figures 18A and 18B illustrate an embodiment of via metallization by filling the via with conductive material according to an embodiment of the invention. As shown in Figure 18A, the conductive substance fills the hole and exceeds its surface by a predetermined amount. This may increase adhesion between portions of the via coating/fill which are fabricated in parts (i.e. dielectric walls and conductive coating/fill of the via are fabricated one after the other), thereby facilitating metallization of the via.

**[00164]** Figure 19 illustrates three different via formations with or without the use of soluble material. In Figure 19, the first dielectric layer 1905 is formed over a soluble layer 1900.

This is not necessary for these embodiments, but is shown as an example. Via 1910 is shown as a “free standing” via having sidewalls metalized. The via 1910 has a part that is extending above the dielectric layer 1905. The extending free standing part would be covered during the fabrication of the second dielectric layer. On the other hand, via 1915 is also formed to have a free standing part, but in order to support the free standing part during fabrication, the via is filled with soluble material 1920. Conversely, via 1925 is filled with dielectric material 1930 to provide support. Of course, the process may be reversed, i.e., one may first build the core with soluble or dielectric material and then coat it with conductive material. Moreover, it should be noted that through-hole filled via has to be fabricated on a release layer, of, e.g., soluble material, as the dense plug cannot be fabricated directly on the tray.

**[00165]** Depositing conductive material on the sidewalls of a via may be done by tilting the deposition head, tilting the tray, or both. Figure 20 illustrates an example where the deposition head 2010 is tilted with respect to the tray 2000. The deposition is then performed on the sidewall 2005 of a via made in dielectric layer 2020.

**[00166]** Figure 21 illustrates another implementation of a PCB fabrication system according to an embodiment of the invention. According to this embodiment, and as opposed to previous embodiments, the system architecture in Figure 21 is comprised of fixed-tray and moving stations. Figure 21 shows a side view of exemplary fixed-tray architecture. According to the illustration, the PCB 2150 is fabricated on fixed tray 2140. An upper fixture 2160 is holding x-y motion system 2170 (e.g. planar motor). The motion system is capable of moving a set of different fabrication devices. These devices correlate to "stations" in the former embodiments of moving tray. In this illustration, the devices are dielectric material deposition head 2110, conductive material deposition head 2120, focused curing apparatus 2130 (e.g. laser generator coupled to focusing optics) and volume curing apparatus 2180 (e.g. magnetron, hot plate). As should be appreciated, the fabrication devices described may be comprised of one or more separate units, while only the part which operates on the PCB is connected to the motion system (e.g., the conductive material deposition head 2120 may have a separate unit, e.g., atomizer which is above the upper fixture and connected to it by wires).

**[00167]** A feature of this embodiment is that some devices with similar functionality that were previously duplicated on different stations (in moving tray architecture) could be avoided. For example, in this embodiment the curing apparatus 2130 is used both for dielectric and conductors fabrication. In contrast, in the moving tray architecture, the curing apparatuses may be duplicated (e.g. two radiation curing devices, one in dielectric fabrication station and one on conductive fabrication station), as curing is usually performed closely to deposition of material.

**[00168]** Moreover, some of the devices may also have z-axis or rotation capability (e.g. curing apparatus which is operated in varying distances from the tray, tilting conductor deposition head for wall-coating of via holes). In addition, a z-axis movement mechanism may also be provided for the tray, e.g. for keeping correlation between board thickness to the required fabrication height (e.g., after deposition of dielectric layer the board is thickened and has to be moved down in order to compensate the increase in thickness). The system also includes mechanism for deposition on the bottom surface of the PCB, as those described in the application (e.g., upper board flipping device), which are not shown in the illustration. As should be understood from the aforementioned description, the apparatus may include additional devices as desired, in similar manner to the moving tray architecture. For example, electrical testing system, component placement system and other devices may be included in the apparatus, as required by the specific application.

**[00169]** A further feature of the subject invention is the ability to concurrently fabricate several PCB's of different designs on a single tray. According to this feature, the single plate comprises several (symmetrical/asymmetrical/mixed) mini "pixel-plates", which are serving as the building blocks for comprising, automatically, different size and shape configurations of smaller plate to fit different designs. Since there is a need for greater efficiency in terms of enabling multi design fabrication on single plate, and since designs may differ in their features (e.g. number of layers) or in process handling (e.g. different curing/baking profiles) within the different fabrication stations/phases, enabling single working plate that can be split to sub, smaller plates and that can be configured, operated and managed automatically to form single big plate or several smaller ones, is of the essence.

**[00170]** Fabricating several designs on a single tray 2250, as exemplified in Figure 22A, might be non-efficient use of the different stations of the inventive system, or, it might prevent better throughput of the system. For example, assuming two different designs are planned to be fabricated on single plate as illustrated in Figure 22A. Say that PCB-A design 2210 has 6 layers while PCB-B design 2220 in Figure 22A has 10 layers. If fabrication is handled on the same plate, PCB-A will be delayed of being supplied to the user since the other design (PCB-B) requires more fabrication time. Furthermore, PCB-A might be subjected to "over processing" (e.g. over exposure to curing/baking), which may cause undesirable change in characteristics and/or cause faults. Since fabrication machines are measured by their throughput for efficiency, and since while fabricating a single design, some stations are operational but others not, putting them in "wait status" until the design arrives according to a predetermined fabrication process, it causes time and money inefficiency.

**[00171]** Figures 22B-22E illustrate an embodiment of a plate that is built of smaller plates that are held together to form the big plate by mechanical, computer-controlled automation equipment. Each one of the smaller plates has a hole for vacuum fixture 2290, and pin or several pins so other pixel-plates neighbors can "inmate" with it to form greater plate. Each pixel-plate 2230 can mate with its neighbors as illustrated in Figure 22C, in parallel, serial, in a row, column or both. The decision of how to divide the whole panel/plate, into smaller ones will be made by dedicated algorithm which will take into consideration total plate size, number of designs needed to be fabricated, number of layers and their thickness, estimated staying time in each station and other parameters relevant.

**[00172]** After deciding of the split, advantageously each pixel-plate may have autonomous mechanical mechanism that can cause it to mate with its neighbor pixel-plates, as demonstrated in Figure 22B. It is possible that the mechanism will be on the outermost frame of the plate or just on the row and column as illustrated in Figures 22D and 22E. As these mechanisms will be the "master" in effecting what neighbor/row/column will be mated, other pixel-plates will be "slaves", being dictated who they will be mated with. As mentioned, it is possible that each and every pixel will be independent.

**[00173]** Turning back to Figure 22B, micro motors 2240 will reside at the "master" pixels or parallel to the beginning of every row/column which will move a lever 2260 to create a physical link to the neighbor pixel-plate. The mechanism suggested here, which comprises lever base with ball shaped axis 2270 and anchoring pin 2280, is just one method and others may be suggested as means of implementation. After splitting the plate into sub plates, each one of the sub plates may continue to perform its tasks in the inventive system separately and in parallel to other sub plates, thereby improving efficiency.

**[00174]** Yet another feature of the invention is facilitation of curing, i.e., cross linking, of the dielectric material. This feature is particularly beneficial for curing/cross-linking of photopolymer, like SU-8, while curing successive layers, one on top of each other, including conductive layers in between. One of the problems associated with curing photopolymers when one layer on top of another and trying to maintain properties like adhesion, is to enable better transferring of heat (heat dissipation) from the outermost surfaces and to the inside of the object. Some of the photopolymers, like the SU-8 and derivatives, require light source (usually UV range) and heating in order arrive at a fully cured state of the material. Heating is usually used for taking out the solvent.

**[00175]** According to an embodiment of the invention, it is desired to build layer on top of another to form a multilayer PCB. Thence, after curing the first layer (partially or fully), there is a need to deposit and then cure the second/next layer. The problem arises at this point and increases with every additional layer to be added – the ability to transfer the heat after the first layer is cured degrades (especially if the heating device is in the tray, e.g. hot plate). In order to enable better heat transfer (in case heating is selected as curing method in the system), better control and/or ability to cure/cross-link is achieved in the fabricated PCB design. The solution is to build additional tunnels into the fabricated design that will enable penetration of air and thus heat to the different location of the 3D object.

**[00176]** Figure 23 illustrate an example of a section of improved curing PCB, fabricated according to an embodiment of the invention. As illustrated in Figures 23, hollow tunnels can be formed side to side or just to a certain point/depth of the design (even in-depth of dielectric layers). For example, a tunnel could be crossing part of the PCB and connecting to via hole 2310,

crossing whole PCB and connecting to via hole 2320, and could be crossing the entire PCB 2330 or part of it 2340 without connecting to via holes. Building these tunnels is relatively easy since the system already uses solid freeform fabrication technology for building the dielectric layers, thus able to form 3D geometrical shape. These tunnels can be formed horizontally, vertically, or even diagonally. Tunnels may vary in size/diameter/shape, depending on the specific fabricated design and constraints (open spaces in outermost layers, number of layers, fabrication speed etc.). These tunnels have to be located in un-occupied spaces, meaning, ones which are not occupied with conductive traces, pads, electronic components etc. Also, their effect of electrical behavior will be minimal (if any), not effecting the functionality of the PCB. After building the tunnels, at the baking phase, heated air will be able to move rather easily and enable more uniform temperature exposure on the whole PCB structure, both for outermost surfaces as well as internal areas which were not in contact with air before.

**[00177]** The various embodiments described above should be utilized with the aim of fabricating a functional PCB. Functional PCB refers to the behavior of a PCB fabricated by the inventive process and system, and specifically to correlation of behavior and testing results of such a PCB to its mass-production equivalent (i.e. the PCB fabricated in conventional mass-production line according to the same fabrication files). In this respect, it should be noted that the required correlation in behavior and testing results may differ according to the target application and use of the fabricated PCB. For instance, when producing PCB which is designated for prototyping (these are usually used for no longer than few months, at most), then, e.g., correlation of corrosion durability tests are of less importance. On the other hand, when producing PCB which is designated for end-product, importance of corrosion durability is a significant factor which has to be correlated with the conventionally manufactured PCB.

**[00178]** As is well known in the art, PCB structures have very complex electro-mechanical characteristics that determine their functionality in large variety of applications. In the most generalized manner, the PCB is supposed to provide expected and accurate electronic functionality under various environment conditions, as defined by the specific design and the target application (e.g., PCBs for automotive have to meet set of requirements which is different compared to consumer electronics PCBs). Conventional PCB manufacturing processes,

equipment and materials have evolved for over 60 years, and are precisely adjusted and optimized for production of PCBs for variety of applications. The selection of processes and materials tightly depend on desired product functionality and application, which is defined in a comprehensive set of published PCB industry standards. Most of these are published by the worldwide standardization organization, IPC (Institute for Interconnecting and Packaging Electronic Circuits). Therefore, in order to achieve the goal of the inventive method and apparatus to manufacture a functional PCB which correlates in behavior and testing results to its conventional-production equivalent, important properties and characteristics of the PCB have to be tightly correlated with the conventionally produced equivalent PCB, despite the fact that the invention uses different materials and processes to manufacture the PCB. As noted before, the specific tests to be correlated depend on the target use and application of the PCB. The following exemplary description focuses on tests in context of prototyping purposes, but it should be understood that any set of tests may be correlated according to the target use and application.

**[00179]** While referring to prototyping, testing of functionality, performance and electronic behavior is generally defined by the following tests:

- 1) As power is connected to the PCB, it has to be measured correctly at the designed contact nodes.
- 2) For predetermined test vectors, the reaction at designated nodes has to fit the design.

As is known in the art, results of these tests depend on numerous parameters (e.g. thermal, electronic, mechanic parameters of the materials comprising the PCB, etc.). Thus, in order to achieve the behavior and testing results correlation, these parameters have to be correlated to those of the mass-production equivalent PCB. The following embodiment demonstrates important parameters and explains their effect on functionality and behavior of the PCB. Then, methods for controlling these parameters in the inventive process and correlating them to the desired values are described. Furthermore, it should be noted that the following discussion is exemplary in nature, and the scope of the invention should not be limited by this description.

**[00180]** Electrical Signal Integrity (SI) is a very important performance criteria in PCB design. SI is a combination of frequency and voltage/current, depending on the application. In

the last two decades, SI has become a serious design consideration in PCB design practice, in order to meet both functional performance and regulatory compliance requirements. In general, analog and digital systems are subject to many issues that can cause signal distortion and degrade SI, which affects system performance significantly, and thus most PCBs are designed to answer SI preservation issues. Furthermore, design requirements for Electromagnetic Compatibility (EMC) are also important, as the conductive/radiative emission from one electronic system to another has to be limited in order to comply with international standards and regulations. Therefore, as SI constitutes a major design consideration and affects PCB performance testing significantly, a PCB fabricated according to the invention has to provide SI in tight correlation with its conventionally produced equivalent. Translating this requirement to material properties, SI is primarily affected by shape and resistance of the conductors, and dissipation factor of the dielectric layers.

**[00181]** Another important issue of electronic performance is electrical impedance. It describes a measure of opposition to an Alternating Current (AC), extending the concept of resistance to AC circuits. As shown in theory, maximum signal power is transferred in a circuit when circuit impedances are matched. This principle is specifically important in high-frequency devices. High clock speeds of digital circuits require controlled impedance because of the fast rise and fall times of pulses. When there is a mismatch of impedance at any place in the transmission line, maximum signal transfer does not occur and some signal power is reflected from the mismatch. As mentioned before, in practice, these reflections affect performance and functionality of digital, high-frequency systems.

**[00182]** Consequently, controlled impedance is a very important electrical requirement of the design for many PCB applications, and thus the impedance of PCB fabricated according to the invention has to be tightly correlated to impedance of its conventionally produced equivalent. In general, impedance is affected by several factors: thickness of dielectric layers, dielectric constant, width and thickness of conductive traces and thickness of the solder mask. All of these parameters are strictly defined under published industry standards for numerous materials (e.g., IPC-4101 which describes properties and materials sheets of basic dielectric materials). As an

exemplary reference, illustrated herein is a representative equation which models the characteristic impedance of a transmission line:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

Where, R is the resistance per unit length, L is the inductance per unit length, G is the conductance of the dielectric per unit length, C is the capacitance per unit length, j is the imaginary unit, and  $\omega$  is the angular frequency.

**[00183]** The description now turns to describe various methods for controlling the aforementioned parameters, which affect SI and impedance. In general, these methods are distinguished between three levels of control: data transformation, processing techniques and selection of materials.

**[00184]** As explained above, the PCB design data undergoes both conversion and transformation. For performing the transformation, the inputs may be standard PCB fabrication files, with original data retrieved (e.g. mechanical coordinates of layers, pads and traces, material, target parameters and more). Without departing from the scope of the invention, the input of the transformation algorithm may also be in different format and data representation from the original fabrication file. As illustrated in, e.g., Figure 6, data conversion may be applied prior to transformation, thereby converting the format of original fabrication files. During transformation, the output fabrication file is changed (i.e. the data is changed, and not its representation, as is common in conversion), to reflect process requirements and in order to keep functional properties of the fabricated PCB correlated to the functional properties expected for the input fabrication file (when it is fabricated in conventional mass-production process), although it is fabricated by different processes and made of different materials. The modifications to the fabrication files may be done for each layer separately and according to graphic data contained in each – or the modifications can be done for a group of PCB layers (or even to all layers as a group). The functional PCB fabricated according to the invention should be correlated in functionality (as is defined by the use and target application of the PCB) to conventionally produced PCB, and additionally to be closely correlated in external mechanical dimensions.

**[00185]** As the inventive process uses freeform fabrication and direct writing technologies for rapid fabrication of PCBs, it also has to provide materials which support these technologies. Most often, these materials are somewhat different from conventional materials used in mass-production of PCBs. Thus, the materials selected for the inventive process have to comply with some of the important properties of conventional PCB materials, and, on the other hand, to provide processing capability in the selected solid freeform fabrication and direct writing technologies. Some examples for such materials are specified in the description. Yet, sometimes these materials need further process modification in order to fit with specific properties that are needed. Therefore, some of the methods further described in the following embodiments provide structured process means for controlling and/or improving required properties.

**[00186]** The following is an example for controlling the conductivity of a conductive layer, according to an embodiment of the invention. Because associated problems of common conductive inks (which are used in direct writing and solid freeform fabrication processes) to achieve bulk materials conductivity when cured (e.g., most mass-production PCB processes nowadays use 99.8% pure copper for conductors), conductivity of additively-fabricated board may be degraded when compared to mass-production board, thereby degrading performance of the board when compared to its conventionally produced equivalent. This may be compensated by data transformation, which increases dimensions of conductor traces in the design, creating conductors with larger cross-section and thereby improves conductivity. Most beneficially, conductor dimensions will be increased by thickness rather than by width, as changing conductor width may cause routing problems where nearby conductors on the same layer could intersect and short the circuit.

**[00187]** Figures 24A and 24B illustrate an example of data transformation leading to changes in the geometric layout of the conductive traces so as to provide performance correlation to conventionally fabricated traces. In this example, a PCB fabrication file F is the standard fabrication file and PCB fabrication file F' is its transformation for the inventive design. F and F' are both comprised of n dielectric layers. The illustration focuses on layer i, comparing F and F'. As can be seen in Figures 24A and 24B, the traces (T1, T2, T3 and T1', T2', T3' respectively)

were maintained with same values for x and y dimensions, while z dimension has increased in F', thereby improving conductivity of traces T1', T2' and T3'. The same process is applicable for all traces on all layers of the fabrication file, for keeping conductivity correlated to conventionally produced board produced according to fabrication file F.

**[00188]** Moreover, data transformation could be applied in order to create trenches for conductors in the dielectric layers, utilizing the flexibility of the inventive process to fabricate freeform dielectric layer in the desired shape. Trenches for conductors focus the deposited conductive material, thereby improving its density, which leads to improved final properties of the conductor, specifically conductivity. Figures 25A and 25B demonstrate combination of the methods described above: the traces T1', T2' and T3' were thickened, and deposited into pre-fabricated recesses in the dielectric layer. It should be further noted that the inventive fabrication system enables fabrication of conductors in different thicknesses on the same layer, as it uses direct writing/solid freeform fabrication method for conductor deposition. This is opposed to conventional manufacturing methods, in which all conductive traces on a layer are in the same height. The data transformation methods described herein may support this feature, enabling fabrication of conductors with different thicknesses on the same layer, e.g., in order to comply with specific performance requirements.

**[00189]** The aforementioned method of thickening conductors may cause conductors on adjacent layers to be too near, thereby reduce effective dielectric insulation between these layers. In such cases, the dielectric layer could be thickened as well, or adapted to provide better dielectric insulation. Some methods for controlling dielectric insulation will be further detailed below.

**[00190]** Further means for improving conductivity of vias is now described. In common practice of PCB design, most of the vias are wall-coated with copper; thereby providing electrical interconnection between different layers. In vias with relatively small diameter (which are usually buried or blind, and thus are not populated with insert components), conductivity may be too low because of the relatively small cross-section of the conductor. In such cases, conductivity may be increased by transforming the wall-coated via to filled via, thereby increasing cross section of the conductive interconnect and increasing conductance. As

demonstrated in Figures 26A and 26B, not all vias are transformed. In this example, vias V2 and V3 were transformed to filled vias (see V2' and V3' in the corresponding fabrication file F'), while via V1 was not transformed ( $V1 = V1'$ ), as it is above the diameter limit.

**[00191]** The description now turns to process techniques for controlling conductive materials properties, specifically conductivity. In common practice of additive deposition of metals on substrates, usually the liquid/powdered raw materials are deposited on the substrate and then sintered or cured in order to harden the material for achieving target material properties. The regime of the curing process, which may be performed by sintering or baking, has significant effect on final material properties. For specific example, when using Nanotechnologies AG-25-ST2 conductive silver ink with M<sup>3</sup>D deposition system, different material properties were achieved by utilizing different curing profiles. When laser sintering with intensity of 2800 J/cm<sup>2</sup> was used, resistivity of about 5.3  $\mu\Omega$ -cm was achieved. On the other hand, when the same material was cured with furnace sintering at 400°C for 2 hours, resistivity of about 3.8  $\mu\Omega$ -cm was achieved.

**[00192]** Therefore, according to embodiments of the invention, the transformation may also provide indication of processing parameters, such as curing time, curing temperature, and curing method. For example, the conductive fabrication station in the system has accurate control of curing profile of deposited conductive material(s). The transformation may also require more than one curing apparatus (e.g. laser sintering and furnace) to be used in the process in a certain order and under certain operating parameters. Coupled with curing profiles for custom material properties required, the inventive system can be rather easily calibrated to provide desired conductivity properties (e.g., for controlled impedance circuit which requires specific value of conductivity for the traces, a custom curing profile will be applied in order to bring the materials to the desired level of conductivity).

**[00193]** Another processing method which may be used to improve conductivity of additively deposited traces is by applying complementary processing, after depositing and curing the conductive element. A specific example is by using additive deposition process to direct write portion of the conductive element (e.g. achieve 20% of desired thickness of element), and then, after final cure of this seed-layer portion, to use methods such as electroplating to complete

the conductive element to the desired thickness. The electrodeposited material has supreme conductivity compared to the deposited seed-layer, thereby improving conductivity of the element. That and more, this method has the benefit that accurate plating is not required, as the seed layer defines the geometry of desired pattern, thus plating (e.g. electroplating) could then be applied on the entire board, without using masks (the electroplated metal will grow only on the seed-layer metallic surfaces).

**[00194]** The dielectric constant of the dielectric layers is also significantly important parameter, which should be tightly matched with the specification of the fabrication file (i.e., most standard fabrication files contain material information in the stack-up of layers, including specific insulation and thickness values of dielectric layers). The following methods provide ability to comply with various dielectric requirements while using a rather limited set of material(s). As with the conductive layer, one method is thickness transformation, i.e., the insulation requirement between layers is controlled by varying the thickness of the layers.

**[00195]** For instance, Figures 27A and 27B illustrates transformation of dielectric layer Li of a PCB design. According to the original fabrication file of Figure 27A, the layer is comprised of material with dielectric constant  $\epsilon_r$  in thickness  $T_i$ . In this example, the dielectric fabrication station contains only a single dielectric material with dielectric constant  $\epsilon_r'$  ( $\epsilon_r' < \epsilon_r$ ). To provide corresponding performance, the original layer Li is transformed to Li', which was thickened to  $T_i'$  in order to provide the dielectric insulation specified in the original fabrication file. It is further important to note that overall board thickness will be limited, to be in reasonable correlation to conventionally-produced equivalent (e.g., maximum overall thickness of the board would not exceed mass production equivalent by more than standard thickness tolerances of conventionally-produced process). As described in the application, very thin layers could be formed accurately, as solid freeform fabrication is used for dielectric layer fabrication and each layer may be comprised of several thin, sub-layers.

**[00196]** Another method of the invention is combining several dielectric materials with different dielectric constants and with compatible process behavior, in order to achieve desired dielectric properties of the original layer. In the example of Figures 28A and 28B, the dielectric layer Li was transformed to three separate dielectric sub-layers, which provide together the

insulation of Li, with overall thickness  $T_i'$  which is tightly correlated to original thickness  $T_i$ . In this embodiment, several dielectric materials with different dielectric constants are combined in different thicknesses in order to provide desired insulation, utilizing freeform additive capability of the inventive process, which enables precise fabrication of thin sub-layers.

**[00197]** According to another method of the invention, controlling dielectric material properties is enabled by using different curing profiles. For example, conventional SU-8 curing process is comprised of few sub-processes: un-cured material is deposited, optionally heated by short pre-bake process, then exposed to UV laser radiation, and afterwards it is often post-baked to finalize curing. Parameters such as pre-bake time and temperature profile, UV exposure intensity, exposure method (e.g. vector by vector, raster), exposure time, post-bake time and temperature profile, are significantly important in determining final properties of the fully-cured material. Thence, the inventive process provides custom curing profiles according to required material properties, allowing adaptation of dielectric material to various properties required in broad range of applications.

**[00198]** As showed in the former exemplary embodiments, various important characteristics of PCB were described along with the material properties which affect them, and their effect on fabricated PCB performance was explained. Then, methods and means for controlling these parameters in the inventive process were demonstrated. These methods are applied in order to provide fabricated PCB which is correlated in behavior and performance to its conventional production equivalent, thereby enabling performance testing of the fabricated PCB without notable degradations when compared to its conventionally-produced equivalent. Yet, it should be noted that the aforementioned discussion is provided as an example rather than a limitation of the invention. The reader familiar in the art could generalize these examples for controlling and improving further material properties which affect PCB performance (e.g. thermal properties such as glass transition temperature, mechanical properties like pull/peel strength), as needed according to published industry standard relevant to the target uses and applications.

**[00199]** As can be understood from the above description, the inventive fabrication system, process and materials are free of limitations associated with conventional PCB manufacture, and

thus have a broad area usability options, extending beyond the manufacture of conventional rigid PCBs. The following description provides two exemplary applications, in the areas of PCBs with embedded components and flexible/rigid-flex PCBs.

**[00200]** The ever growing demand to miniaturize, reduce weight and cost of functional PCBs, drives PCB manufacturers to embed electronic components inside the PCB. The potential is for embedding conventional discrete electronics, such as resistors, capacitors, transistors, batteries, photo-voltaics, sensors, memory, lasers, photo-detectors, magnets, loudspeakers and more. In recent years, there is also a potential to produce components in-situ during and as part of the process of fabricating PCB. In-situ production is currently focused mainly on resistors and capacitors, but production of other components, such as transistors, is emerging and is expected to grow with the availability of technologies. It is estimated that the PCB surface-area for many commercial PCBs is occupied up to 50% and more by components that require a low number of connections and hence can be buried or embedded inside the layers of the PCB. This will free a large part of the PCB area and enable either introducing higher functionality in the same area, with higher level of integration and/or reduction in manufactured PCB area and often, by that, a reduction in production cost.

**[00201]** Most of the requirements for embedding electronic components inside PCB layers are different for embedding discrete components and for in-situ production of components. The common requirements include: lower number of contacts, low component thickness and, typically, low power consumption to fit the limiting environmental conditions.

**[00202]** In-situ components will typically be of higher variance (lower accuracy) and lower range (e.g. capacitance range of in-situ capacitors will be limited to low-capacitance). Producing PCBs that accommodate discrete or in-situ embedded components requires specific care in selection of PCB materials, patterning methods and component placement process. Embedding discrete components further requires higher alignment precision and contact connection process. In-situ production requires also special design of components, selection of component materials and, typically, a process for measurement and trimming of component values.

**[00203]** The inventive process and system enable embedding both discrete electronic components and in-situ production, and provides end-to-end process support for embedding components, from the fabrication file to production. Embedding discrete components will typically require the following steps:

- a. Die bonding of components or bare dies onto a conductor layer.
- b. Dielectric lamination to insulate and avoid electrical shorts.
- c. Forming via contacts.
- d. Metallize contacts.

**[00204]** The inventive process accommodates regular die bonding and has the best tools for building accurately both insulation and contacts with the dielectric and conductive materials. Thereby, after attaching the discrete components onto a layer – all other production stages are standard, seamlessly integrated with, e.g., the fabrication process described at Figure 6. In order to support embedding discrete components, the inventive system can optionally incorporate a pick & place head that lifts components from a specific tray (e.g. pick and place machine 575 in Figure 5), and attaches each component in a pre-designated location. The components can be attached on top of a standard adhesive and pattern that is dispensed by the pick and place head – or directly on the semi-cured dielectric layer, which is slightly adhesive, thereby making the adhesive dispensing stage redundant. Following the components attachment stage, the inventive process is used to dispense dielectric material as an insulator and via holes in the pre-designed places, conductive material for conductor connections and vias metallization.

**[00205]** Currently, in-situ components production processes is provided by limited number of manufacturers. Production of in-situ components is typically achieved using ink-jetting, screen printing, thin film technology or sheet material-based components. Typically, resistive material is dispensed over conductive layer in patterns that provide pre-designed resistivity and, with different dielectric material, which provides pre-designed capacitance. Following the dispensing of the materials, the layer is cured or sintered to achieve final properties. More complex components are produced by combining the dispensing of conductive and dielectric materials in two or three dimensional patterns according to the specific design and the target application.

**[00206]** The inherent issue with all aforementioned technologies stated is that the dispensed material has to be sintered or cured, and subsequently measured, while measurement of capacitance or resistance values is difficult. Moreover, modifying these values (if found to be needed after measurement) by trimming or addition is almost impossible – or at least complex enough to render it almost impractical for standard commercial use. Hence, the accurate functionality of in-situ produced passives is limited by the ability to dispense materials accurately in three dimensions and control the curing or sintering of the materials. The inventive process allows for embedding accurate passive components by adding the dispensing of additional resistive materials and additional dielectric materials in the same way that conductive and dielectric materials are dispensed for fabricating the PCB. Measuring the values of dispensed passives in-process may be achieved by electrical testing equipment, e.g. the electrical testing unit 570 in Figure 5. The inventive process has the ability to accurately control the three dimensional deposition of materials by dispensing thin, even layers in a controlled fashion, and cure each layer before depositing the next one. If needed, modifying the value of the embedded passive can be achieved by using the inventive process to dispense additional layer of material where it is required, thereby rendering accurate passives as required by the designed.

**[00207]** Flexible PCBs are classified in two major types: flex and rigid-flex PCBs. Flex PCBs are strictly flexible, having no rigid materials attached (they may have stiffeners, which are not part of the layer stack-up). Rigid-flex PCBs have combinations of rigid and flexible materials. Flexible PCBs are fabricated by specifically adapted materials and processes. These are characterized by degraded panel utilization and degraded yield, and require high expertise. For example, fabrication costs for rigid-flex PCBs can be as much as five or seven times the cost of standard rigid PCB.

**[00208]** The inventive process could be specifically suited for the manufacturing of flex and rigid-flex PCBs. By operating the system with dielectric and conductive materials specifically adapted for these applications, it enables automated and easy fabrication, specifically for low quantities. For example, the additive fabrication process described herein can easily fabricate areas on the PCB with different number of layers. Additionally, the process can spread a dielectric layer selectively to accommodate automatically any shape and mix of flexible and

rigid areas on the same PCB. The ability to spread and cure dielectric layers of almost any thickness enables tailoring the degree of flexibility and the three dimensional mechanical properties according to a variety of design requirements. The ability to dispense conductors at a variety of thicknesses complements the control over the dielectric flexibility to render functional rigid-flex PCBs that requires very little manual labor for manufacturing.

**[00209]** As realized of the aforementioned examples, the process described herein may be extended to various applications. Further applications include the production of three dimensional PCBs, Multi Chip Modules (MCM), RF (Radio Frequency) and EM (Electro-Magnetic) shield/casing (conductive cover against RF interference and electromagnetic interference), fixing of damaged PCBs, and adding layers of special structures/features on existing PCBs. Moreover, the inventive fabrication process and technology, or parts thereof, may be adapted to highly efficient mass production.

**[00212]** Finally, it should be understood that processes and techniques described herein are not inherently related to any particular apparatus and may be implemented by any suitable combination of sub-systems. Further, various types of general purpose devices may be used in accordance with the teachings described herein. It may also prove advantageous to construct specialized apparatus to perform the method steps described herein. The present invention has been described in relation to particular examples, which are intended in all respects to be illustrative rather than restrictive. Those skilled in the art will appreciate that many different combinations of hardware, software, and firmware will be suitable for practicing the present invention. For example, the described software may be implemented in a wide variety of programming or scripting languages, such as Assembler, C/C++, perl, shell, PHP, Java, HFSS, CST, EEKO, etc.

**[00213]** The present invention has been described in relation to particular examples, which are intended in all respects to be illustrative rather than restrictive. Those skilled in the art will appreciate that many different combinations of hardware, software, and firmware will be suitable for practicing the present invention. Moreover, other implementations of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as

exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

## Claims

1. A method for fabricating at least one functional printed circuit board (PCB), comprising,
  - a. obtaining a PCB fabrication data file;
  - b. performing data conversion to generate a modified fabrication file corresponding to the fabrication data file;
  - c. performing data transformation by modifying parameters specified in the modified fabrication file to account for variation in materials and processes utilized for fabricating the PCB, the data transformation generating a transformed fabrication file;
  - d. providing a tray;
  - e. using the transformed fabrication file to fabricate a dielectric layer by:
    - i. depositing into the tray a liquid composition;
    - ii. allowing the liquid composition to spread over the surface of the tray; and,
    - iii. curing selected areas of the liquid composition to delineate the shape and the boundaries of the PCB to provide a cured insulating layer having a top and bottom surfaces; and,
  - f. using the transformed fabrication file to fabricate a conductive layer by depositing a conductive trace on at least one of the top and bottom surfaces of the cured insulating layer;to thereby provide a PCB having performance characteristics correlating to performance characteristics of a conventionally fabricated PCB using the fabrication data file.
2. The method of claim 1, further comprising repeating steps e and f a plurality of times over one of the top and bottom surfaces of the dielectric layer so as to provide a multi-layer one-sided PCB.

3. The method of claim 2, further comprising flipping the one-sided PCB so that the cured insulating layer becomes top layer on the tray, and repeating steps e and f a plurality of times on the other of the top and bottom surfaces of the dielectric layer so as to provide a multi-layered double-sided PCB.
4. The method of claim 1, further comprising repeating steps e and f a plurality of times over both of the top and bottom surfaces of the dielectric layer to provide a multi-layered double-sided PCB.
5. The method of claim 4, further comprising depositing an insulative solder mask layer.
6. The method of claim 4, further comprising depositing a conductive pad coating.
7. The method of claim 4, further comprising printing a legend on the double-sided PCB using colored dielectric material.
8. The method of claim 1, wherein curing selected areas comprises irradiating selected areas.
9. The method of claim 8, wherein irradiating selected area comprises directing UV radiation onto selected areas.
10. The method of claim 8, wherein curing selected areas further comprises a curing enhancement step following the irradiating the selected areas.
11. The method of claim 10, wherein the curing enhancement step comprises a heating step.

12. The method of claim 11, wherein the heating step comprises radiating the fabricated PCB with microwave radiation.
13. The method of claim 1, wherein step d further comprises providing a release agent over the tray.
14. The method of claim 13, wherein providing a release agent comprises one of: providing a fabric layer over the tray or spreading a liquid releasing agent over the tray.
15. The method of claim 4, further comprising fabricating holes in the cured insulation layer by defining non-irradiated areas and cleaning the non-radiated areas after the curing step.
16. The method of claim 14, further comprising depositing conductive substance into selected holes to thereby fabricate conductive vias.
17. The method of claim 1, wherein step e comprises depositing into the tray a liquid composition comprising an octafunctional epoxidized novolac and photoinitiator.
18. The method of claim 17, wherein the liquid composition further comprises nano-particles.
19. The method of claim 1, wherein depositing a conductive trace comprises using a deposition head to inject conductive substance onto the cured insulating layer.

20. The method of claim 4, wherein each time step e is performed, sub-steps i. ii. and iii. are repeated a plurality of times so as to fabricate the dielectric layer by fabricating a plurality of sub-layers.
21. The method of claim 20, wherein after each repetition of sub-step iii. heat is applied to the fabricated PCB.
22. The method of claim 20, wherein each time sub-steps i. ii. and iii. are performed, the method further comprises fabricating holes in the sub-layer.
23. The method of claim 22, wherein each time sub-steps i. ii. and iii. are performed, the method further comprises depositing conductive substance into selected holes.
24. The method of claim 22, wherein after a sequence of sub-steps i. ii. and iii. is performed a plurality of times, the method further comprises depositing conductive substance into selected holes.
25. The method of claim 4, wherein at selected times wherein step e is performed, the method further comprises fabricating curing enhancing tunnels in the fabricated dielectric layer.
26. The method of claim 4, wherein at selected times wherein step e is performed, the method further comprises depositing soluble material to define voids in the fabricated dielectric layer.
27. The method of claim 4, wherein each time step e is performed, sub-steps i. ii. and iii. are repeated a plurality of times using at least two different dielectric materials, so as to fabricate the

dielectric layer by fabricating a plurality of sub-layers having different dielectric insulation properties.

28. The method of claim 4, wherein step e further comprises mixing into the dielectric materials at least one of ingredients that assist in conductors adherence, ingredients that mechanically stabilize the dielectric material, and ingredients that thermally stabilize the dielectric and material.

29. The method of claim 4, wherein step e further comprises mixing into the dielectric materials ingredients that modify the insulating properties of the dielectric material.

30. The method of claim 4, wherein step e further comprises depositing onto the dielectric layer an intermediate layer formed for improved conductive material adherence to the dielectric layer.

31. The method of claim 4, wherein at selected times wherein step e is performed, the method further comprises generating trenches on at least one surface of the dielectric layer and wherein step f comprises depositing at least part of the conductive trace into the channels.

32. The method of claim 4, wherein at selected times wherein step f is performed, the method comprises depositing conductive traces of varying thickness as specified by the transformed fabrication file.

33. The method of claim 4, wherein at selected times wherein step f is performed, depositing conductive traces comprises depositing a seed layer of conductive material and forming a main conductive layer over the seed layer.

34. The method of claim 33, wherein forming a main conductive layer comprises using electroplating.
35. The method of claim 4, wherein at selected times wherein step f is performed, the method further comprises performing and least one of automated optical inspection of the formed conductive traces and electrical resistivity testing of the conductive traces.
36. The method of claim 4, further comprising performing electrical testing at completion of fabrication of the PCB.
37. The method of claim 4, wherein a plurality of PCB boards are fabricated concurrently within the tray.
38. The method of claim 1, wherein each of steps e and f further comprise selecting fabrication parameters according to at least the desired insulation properties of the dielectric layer and resistivity properties of the conductive layer.
39. The method of claim 1, wherein step e,ii, further comprises planarizing a top surface of the liquid.
40. A method for fabricating at least one functional printed circuit board (PCB), comprising,  
uploading PCB fabrication data file onto a controller;  
utilizing the controller to control operation of a central handling station to load and unload a fabrication tray onto and from a plurality of tray positioning stations;

utilizing the controller to control operation of a dielectric dispenser to dispense a dielectric substance onto the tray and to control operation of a curing mechanism to cure the dielectric substance to form a dielectric layer;

utilizing the controller to control operation of a conductor dispenser to dispense a conductive substance onto the dielectric layer; and,

utilizing the controller to control operation of a thermal station to thermally process at least one of the dielectric substance and the conductive substance.

41. The method of claim 40, wherein thermally process comprises exposing at least one of the dielectric substance and the conductive substance to at least one of: UV radiation, microwave radiation, and heater radiation.

42. The method of claim 40, wherein controlling operation of the dielectric dispenser comprises operating a liquid dispenser to dispense a radiation curable liquid onto the tray, and wherein curing the dielectric substance comprises radiating the liquid.

43. The method of claim 40, wherein control operation of a dielectric dispenser comprises operating a dispenser head to deposit dielectric substance according to layout design of the dielectric layer.

44. The method of claim 40, further comprising utilizing the controller to control operation of a planarizing mechanism to planarize the dielectric layer.

45. The method of claim 40, wherein controlling operation of the conductor dispenser comprises operating a printer jet to dispense conductive trace material.

46. The method of claim 45, further comprising utilizing the controller to control operation of a flipping mechanism to flip a fabricated board so as to form conductive traces on both sides of the board.
47. The method of claim 40, further comprising fusing at least two fabricated boards together.
48. The method of claim 40, further comprising:
- operating the control console to generate a freeform fabrication file using at least the PCB fabrication data file; and,
- operating the control console to transform the freeform fabrication file into a transformed fabrication file, wherein selected data of the freeform fabrication file is transformed so as to enable correlating performance characteristics of the PCB to performance characteristics of a conventionally fabricated PCB.
49. The method of claim 48, wherein transforming into transformed fabrication file further comprises generating files to control the curing mechanism to delineate vias.
50. The method of claim 49, wherein transforming into transformed fabrication file further comprises generating files to control the curing mechanism to delineate vias having oblique, non-vertical sidewalls.
51. The method of claim 49, wherein transforming into transformed fabrication file further comprises generating files to fabricate mating structures on each fabricated board to ensure alignment during the step of fusing the fabricated boards.

52. The method of claim 40, wherein utilizing the controller to control operation of a conductor dispenser comprises depositing conductive substance on both sides of the dielectric layer.
53. The method of claim 40, further comprising setting parameters of the curing mechanism to facilitate fabricating dielectric layer having properties corresponding to conventional PCB insulation layer fabricated according to the fabrication data file.
54. The method of claim 40, further comprising setting parameters of the conductor dispenser and the thermal station to facilitate fabricating conductive layer having properties corresponding to conventional PCB conductive traces fabricated according to the fabrication data file.
55. The method of claim 48, wherein transforming into transformed fabrication file further comprises changing a designed thickness of conductive lines to reduce resistivity.
56. The method of claim 40, further comprising utilizing the controller to control operation of the dielectric dispenser and the conductor dispenser to form vias by consecutively depositing thin dielectric sub-layers with holes defined therein and depositing conductive substance into the holes.
57. The method of claim 56, wherein at least two of the sub-layers are formed using two different dielectric materials.
57. The method of claim 40, further comprising utilizing the controller to control operation of the dielectric dispenser and the conductor dispenser to form vias by depositing pillars of conductive substance and depositing dielectric layer about the pillars.

58. The method of claim 40, further comprising utilizing the controller to control operation of the dielectric dispenser, the conductor dispenser and a soluble material dispenser to form vias by depositing soluble material to delineate the vias, depositing dielectric layer about the soluble material, removing the soluble material to expose holes in the dielectric layer, and depositing conductive substance into the holes.

59. The method of claim 40, further comprising utilizing the controller to control operation of the conductor dispenser to form pad coating.

60. The method of claim 40, further comprising utilizing the controller to control operation of the dielectric dispenser to form solder mask.

61. The method of claim 40, further comprising utilizing the controller to control operation of the dielectric dispenser to dispense colored dielectric substance to thereby form a legend.

62. A method of fabricating a functional PCB, comprising:

forming a main dielectric layer having a top surface and a bottom surface by depositing a dielectric material onto a fabrication tray and exposing the dielectric material to a curing process to delineate the area and boundary of the main dielectric layer;

forming a series of interleaving conductive trace layers and insulative layers on the top surface of the main dielectric layer;

forming at least one conductive trace layer on the bottom surface of the main dielectric layer.

63. The method of claim 62, wherein exposing the dielectric material to a curing process comprises irradiating the dielectric material with an illumination source.
64. The method of claim 62, wherein exposing the dielectric material to a curing process comprises partially curing the main dielectric layer.
65. The method of claim 62, wherein forming each of the conductive trace layers is performed by depositing conductive material using direct-write method and at least partially curing the conductive material.
66. The method of claim 62, further comprising forming vias by forming holes in selected dielectric layers and depositing conductive material into the holes.
67. The method of claim 66, wherein forming vias comprises forming each dielectric layer by forming dielectric sub-layers having holes defined therein, and depositing conductive substance in holes of each sub-layer.
68. The method of claim 66, wherein forming holes comprises forming holes having oblique side walls.
69. The method of claim 66, wherein forming holes comprises depositing soluble material to define the holes prior to forming each insulative layer and removing the soluble material after forming each insulative layer.
70. The method of claim 62, further comprising forming at least one of: pad coating, solder mask, and legend.

71. The method of claim 62, wherein forming each of the insulative layers comprises repeating operations of forming a sub-layer of fractional thickness of the insulative layer and curing the sub-layer prior to forming the next sub-layer.
72. The method of claim 71, further comprising forming holes in each sub-layer and depositing conductive material into the holes after curing the sub-layer.
73. The method of claim 72, wherein forming holes comprises varying the diameter of the holes in each sub-layer so that the resulting holes in each insulative layer comprise oblique sidewalls.
74. The method of claim 66, wherein depositing conductive material comprises coating sidewalls of selected holes and completely filling other holes.
75. The method of claim 62, further comprising performing electrical testing to verify functionality of the PCB.
76. The method of claim 62, further comprising concurrently forming a second functional PCB by:
- exposing the dielectric material to a curing process to delineate the area and boundary of a second main dielectric layer concurrently with forming the main dielectric layer;
  - forming a series of interleaving conductive trace layers and insulative layers on the top surface of the second main dielectric layer; and,
  - forming at least one conductive trace layer on the bottom surface of the second main dielectric layer.

77. A system for fabricating a printed circuit board (PCB) comprising:  
a central handling station comprising an extendable robot arm configured for holding a tray;  
at least one tray positioning mechanism positioned within reach of the robot arm and configured to accept the tray from the robot arm;  
at least one dielectric substance dispenser positioned within reach of the robot arm;  
at least one conductive substance dispenser positioned within reach of the robot arm;  
a curing station positioned within reach of the robot arm; and,  
an operator console coupled to and controlling operations of the dielectric substance dispenser, the conductive substance dispenser, and the curing station.
78. The system of claim 77, further comprising a fabrication station housing the dielectric substance dispenser, the conductive substance dispenser, and the tray positioning mechanism.
79. The system of claim 77, further comprising:  
a first fabrication station positioned within reach of the robot arm and housing the dielectric substance dispenser and one tray positioning mechanism; and,  
a second fabrication station positioned within reach of the robot arm and housing the conductive substance dispenser and a second tray positioning mechanism.
80. The system of claim 77, wherein the dielectric substance dispenser comprises:  
a liquid dispenser; and,  
a developing mechanism.

81. The system of claim 80, wherein the developing mechanism comprises a radiation source.
82. The system of claim 81, wherein the radiation source comprises a UV light source.
83. The system of claim 77, wherein the conductive substance dispenser comprises a deposition head.
84. The system of claim 83, wherein the deposition head is tiltable.
85. The system of claim 77, further comprising a flipping mechanism configured to flip a board fabricated within the tray.
86. The system of claim 85, wherein the flipping mechanism is situated within the central handling station.
87. The system of claim 77, further comprising a processor receiving and converting PCB fabrication data into control instructions for controlling operations of the dielectric substance dispenser, the conductive substance dispenser, and the heating station, and further transforming the control instructions to vary parameters of the PCB fabrication data.
88. The system of claim 77, further comprising a release mechanism operable to release a fabricated board from the tray.
89. The system of claim 77, further comprising a release agent dispenser positioned within reach of the robot arm.

90. The system of claim 80, further comprising a cleaning mechanism configured for cleaning substance undeveloped by the developing mechanism.
91. The system of claim 77, further comprising a solder mask applicator within reach of the robot arm or a transfer robot.
92. The system of claim 77, further comprising a legend applicator within reach of the robot arm or a transfer robot.
93. The system of claim 77, further comprising a pad coater within reach of the robot arm or a transfer robot.
94. The system of claim 77, further comprising electrical component assembly unit within reach of the robot arm or a transfer robot.
95. The system of claim 88, wherein the release mechanism comprises a tray opening mechanism.
96. The system of claim 81, further comprising a controller dynamically varying the focus of the radiation source.
97. The system of claim 77, further comprising a heater for heating the tray.

98. The system of claim 78, wherein the fabrication station comprises an inert gas environment.
99. The system of claim 79, wherein at least one of the first and second fabrication station comprises an inert gas environment.
100. The system of claim 77, wherein the tray comprises a plurality of lockable sub-trays.
101. A system for fabricating a printed circuit board (PCB), comprising  
at least one dielectric subsystem for dielectric layers fabrication;  
at least one conductor subsystem for conductive layers fabrication;  
a curing subsystem;  
an operator console controlling operations of the system; and,  
a transfer mechanism for transferring the subsystems to one or more PCB work pieces.
102. The system of claim 101, wherein the dielectric sub-system comprises:  
a liquid dispenser; and,  
a developing mechanism.
103. The system of claim 102, wherein the developing mechanism comprises a radiation source.
104. The system of claim 103, wherein the conductor subsystem comprises a printer head.

105. The system of claim 104, further comprising a chamber having inert gas environment during fabrication.

106. The system of claim 101, further comprising a fabrication tray housing the one or more PCB work pieces.

107. The system of claim 101, wherein the curing subsystem comprises an oven.

108. The system of claim 106, wherein the curing subsystem comprises a heater for heating the tray.

109. The system of claim 102, wherein the liquid dispenser comprises a plurality of nozzles.

110. The system of claim 103, wherein the conductor subsystem comprises a plurality of deposition heads.

111. The system of claim 101, wherein the conductor subsystem comprises a seed layer dispenser and a conductive trace fabricator.

112. The system of claim 111, wherein the seed layer dispenser comprises at least one deposition head and the conductive trace fabricator comprises an electroplating subsystem.

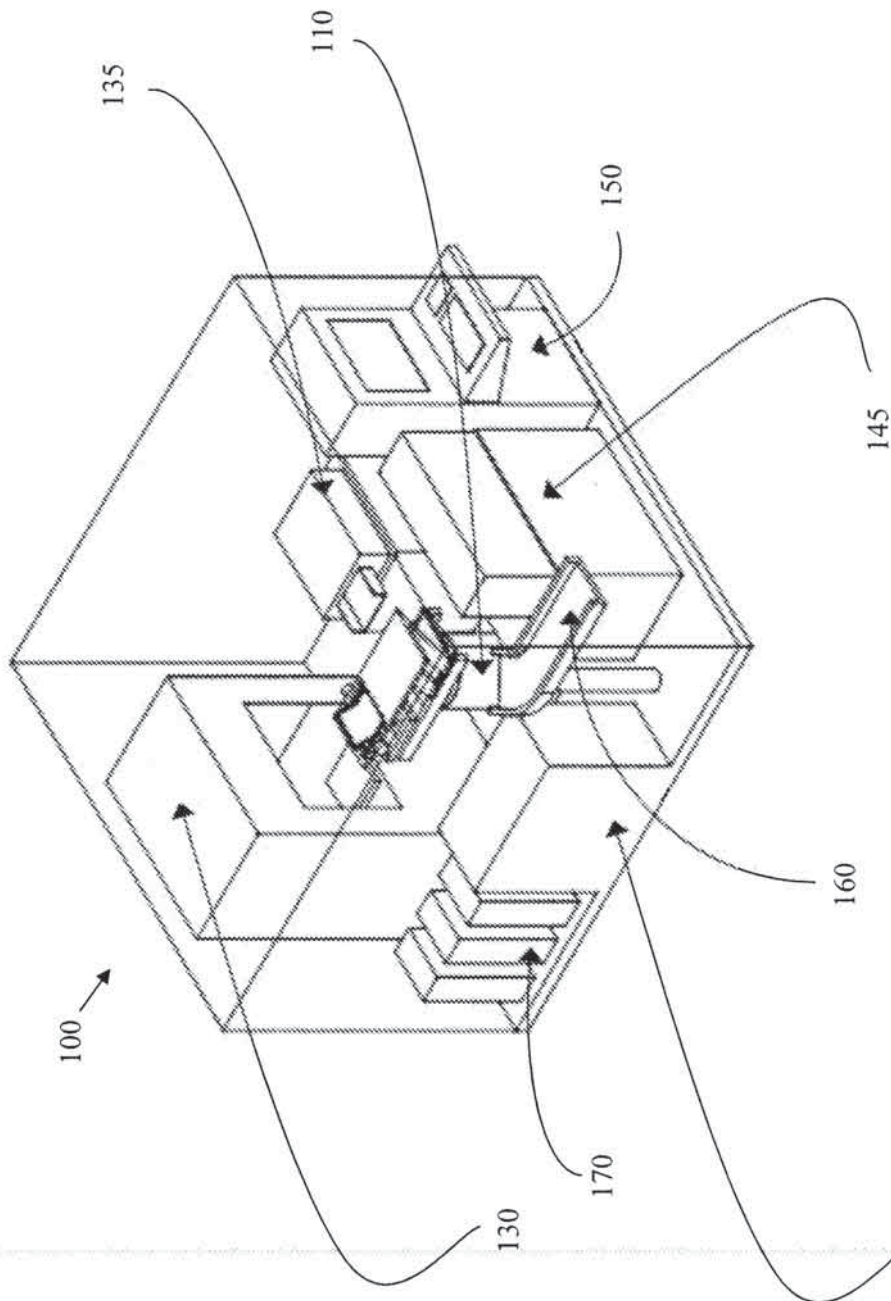


Figure 1

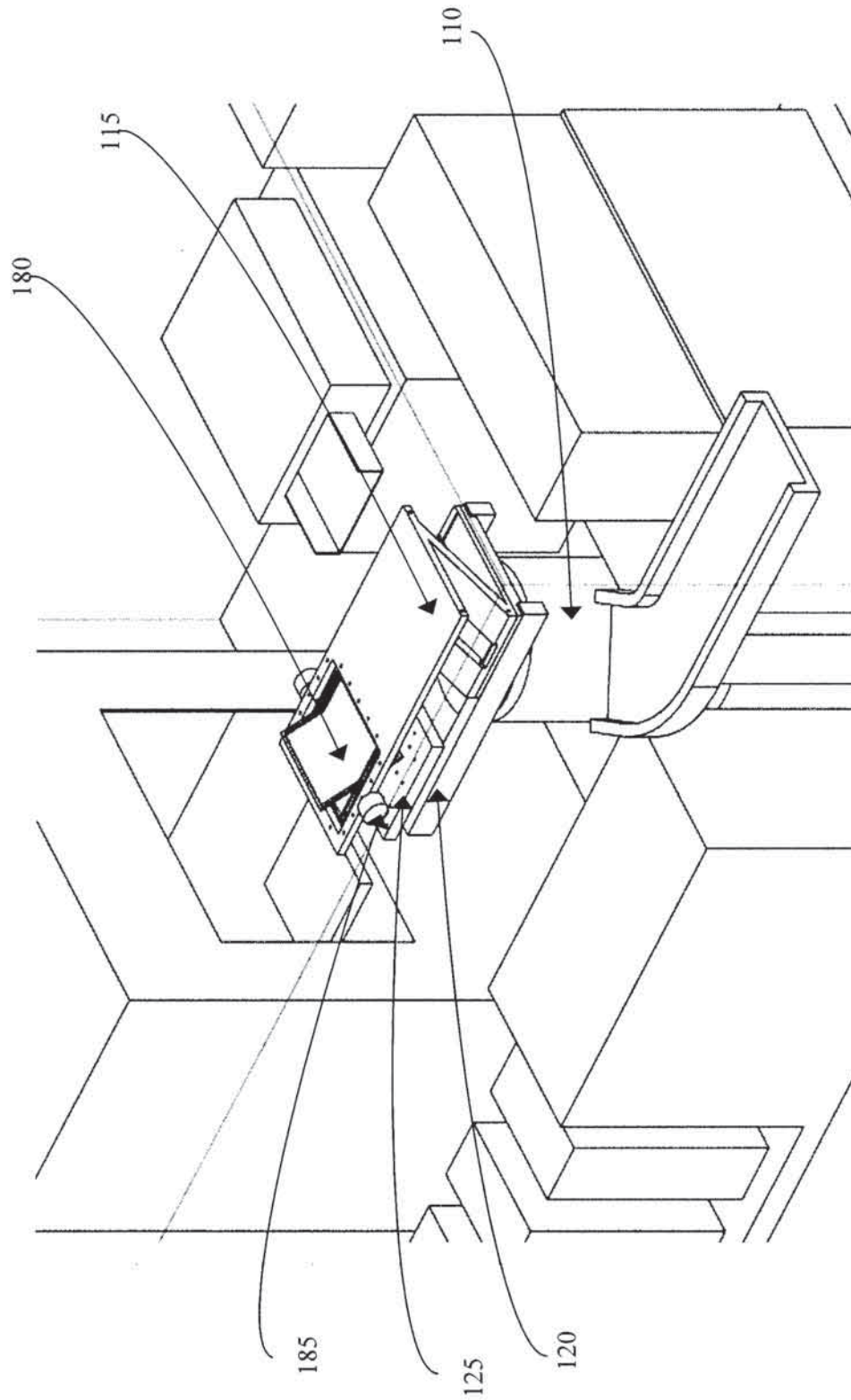
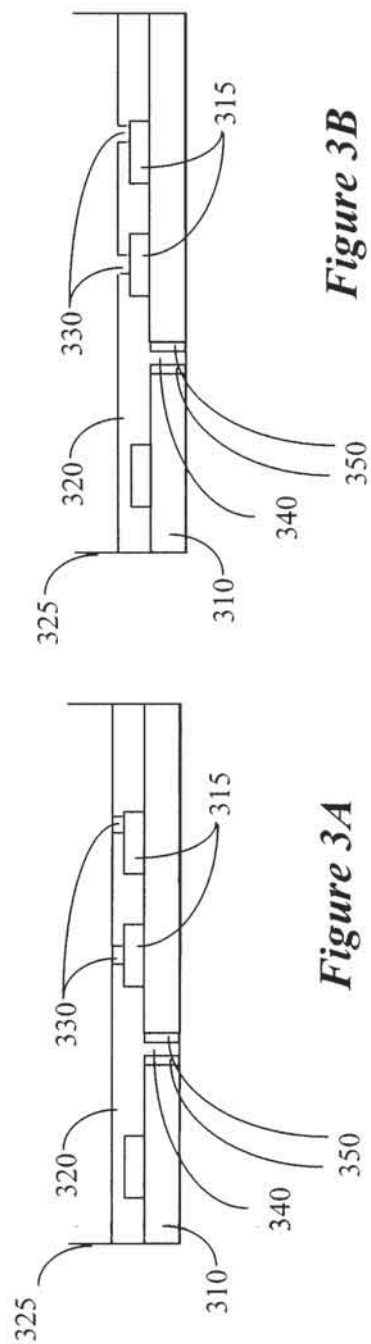
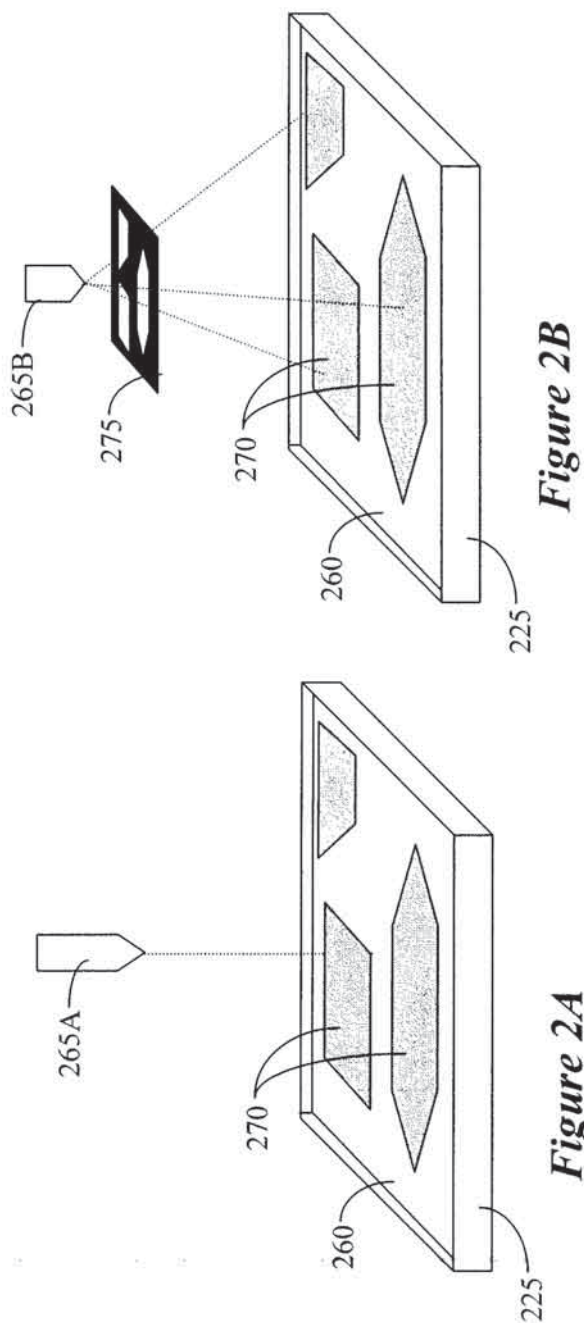


Figure 1A



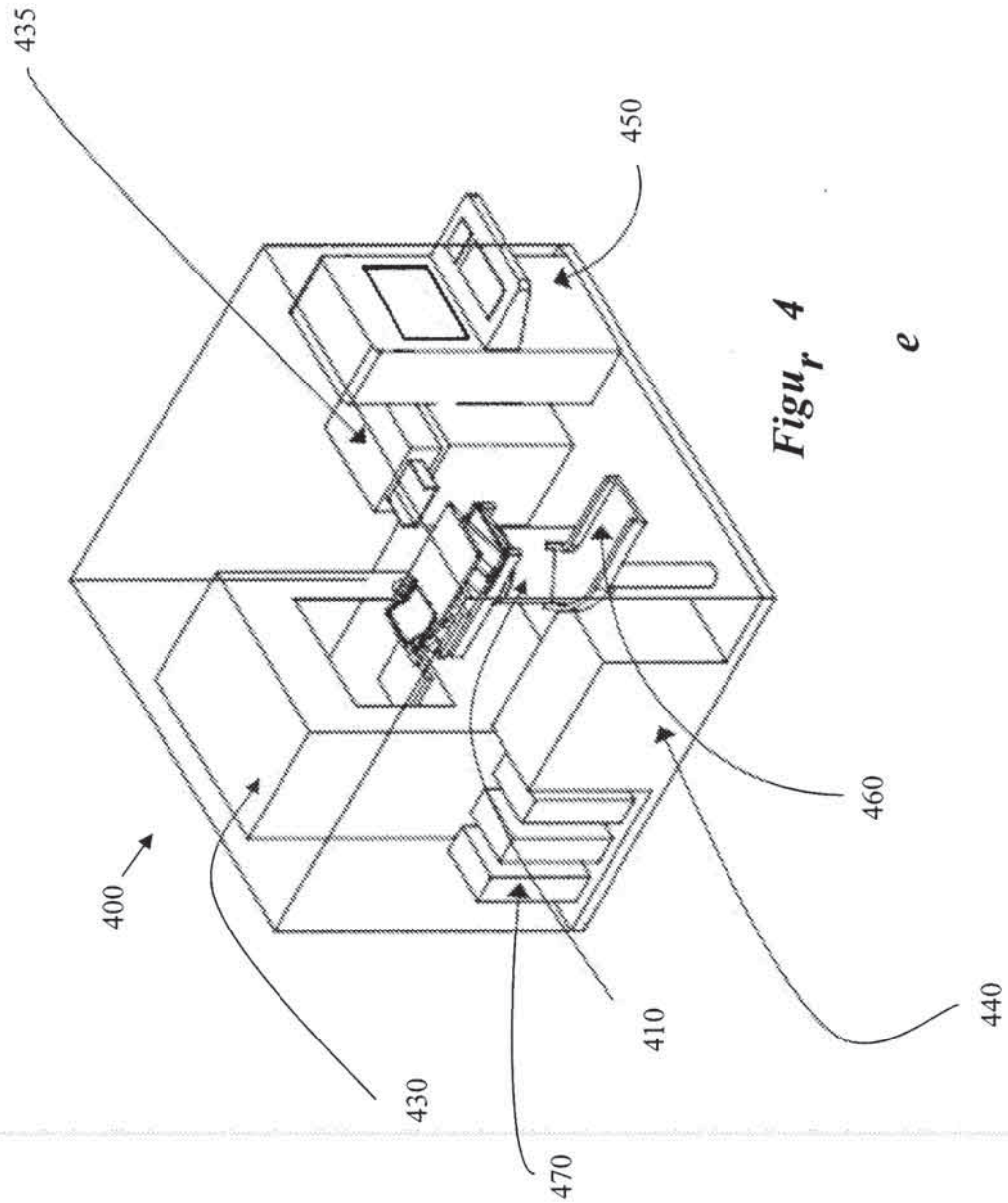
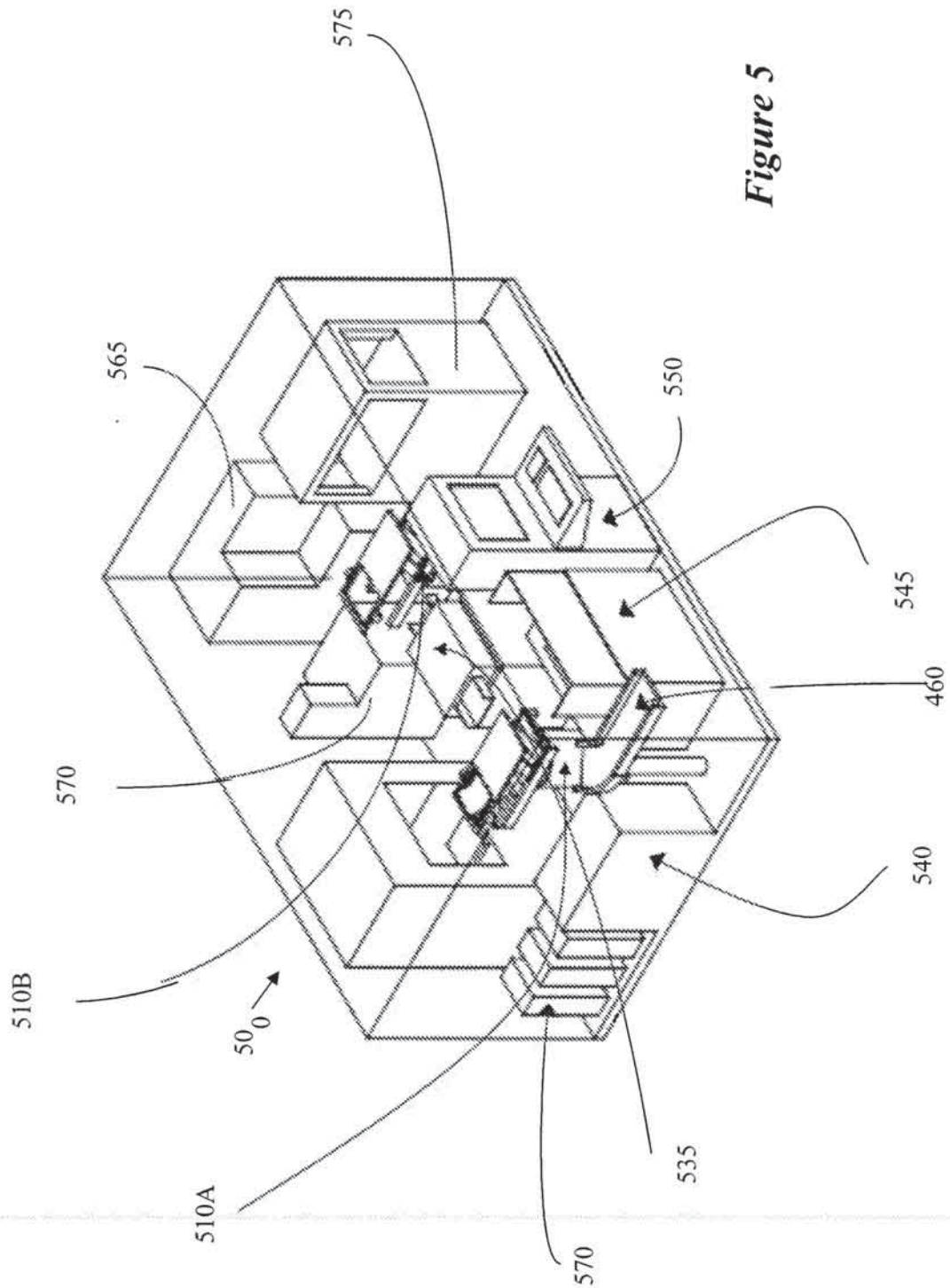
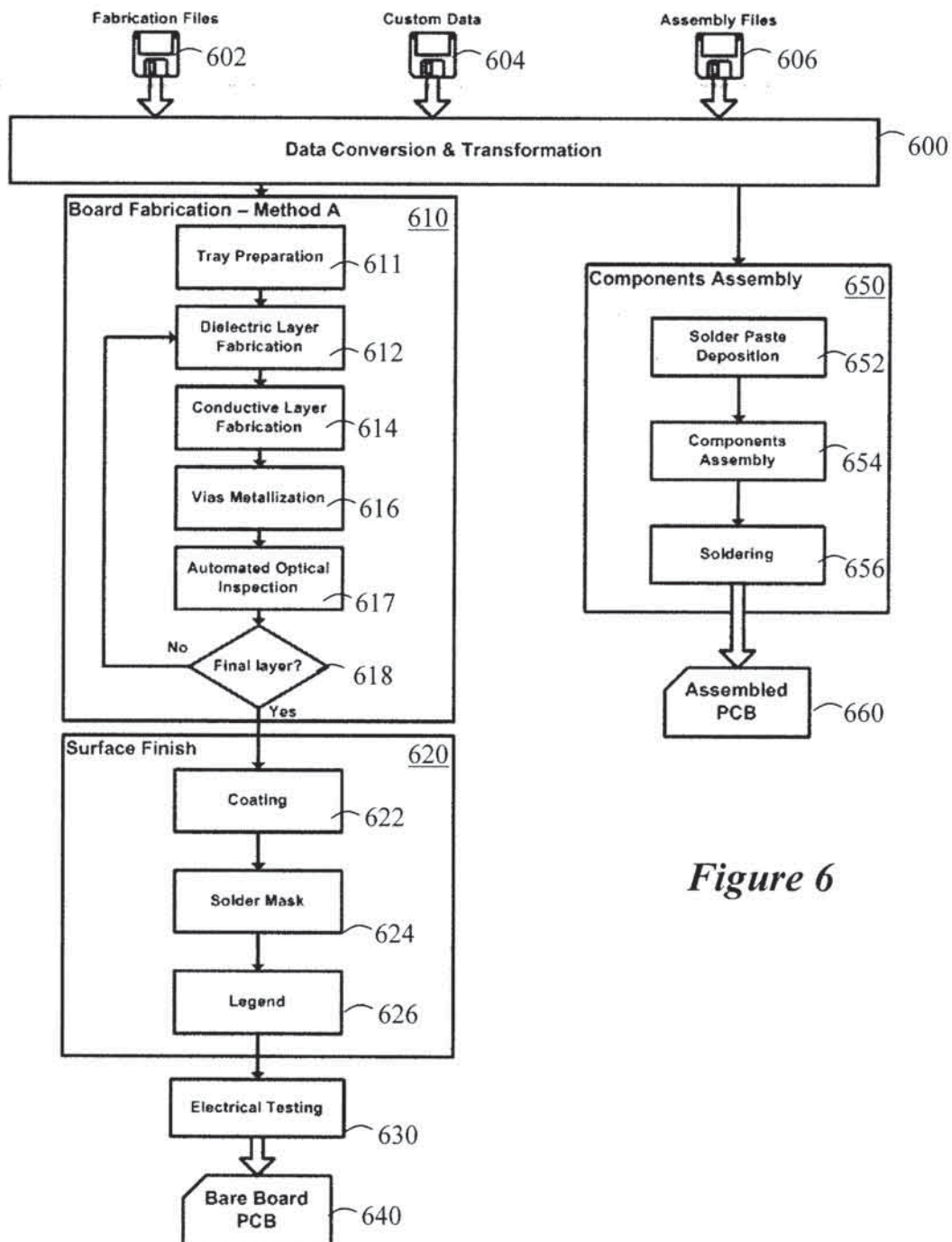


Figure 5



*Figure 6*

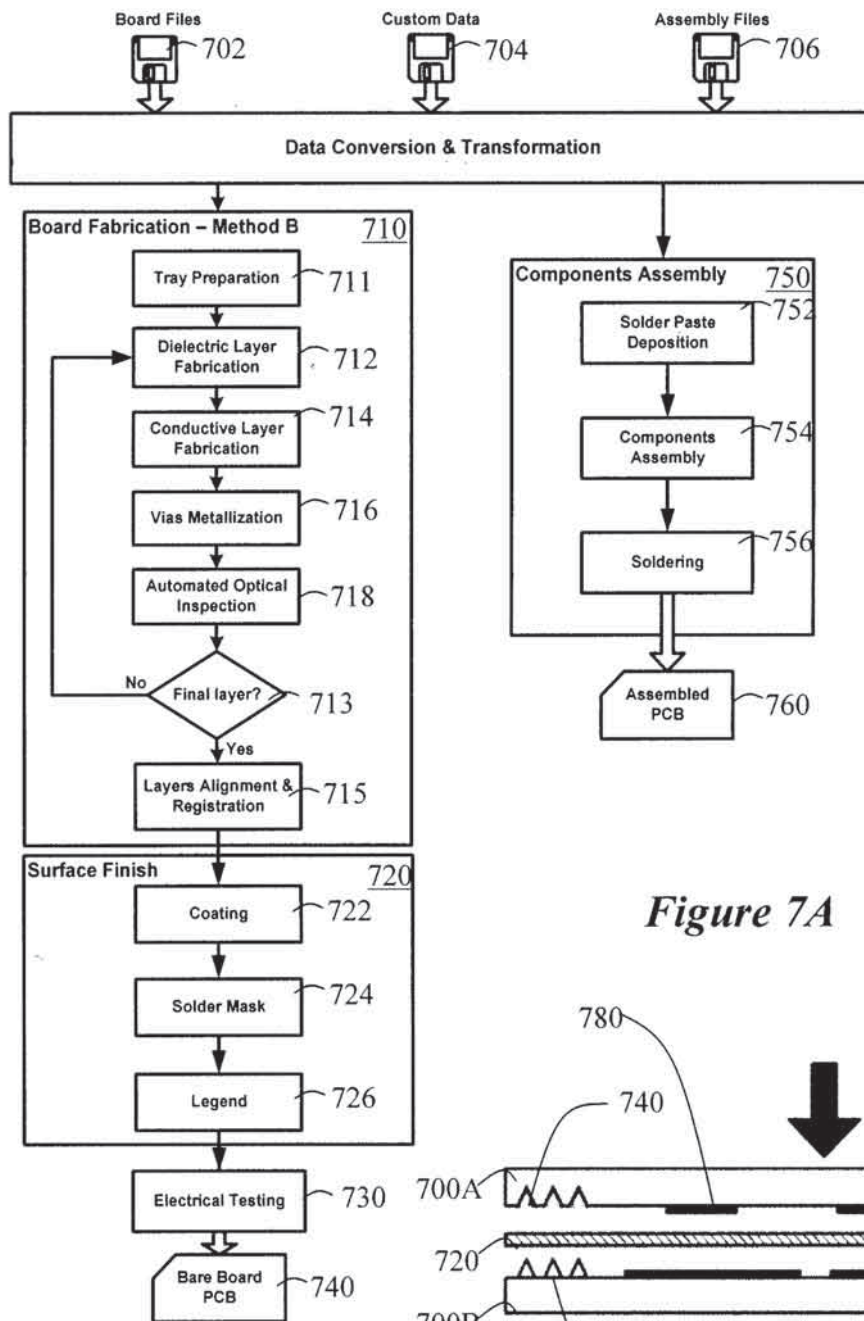


*Figure 7A*

*Figure 7B*

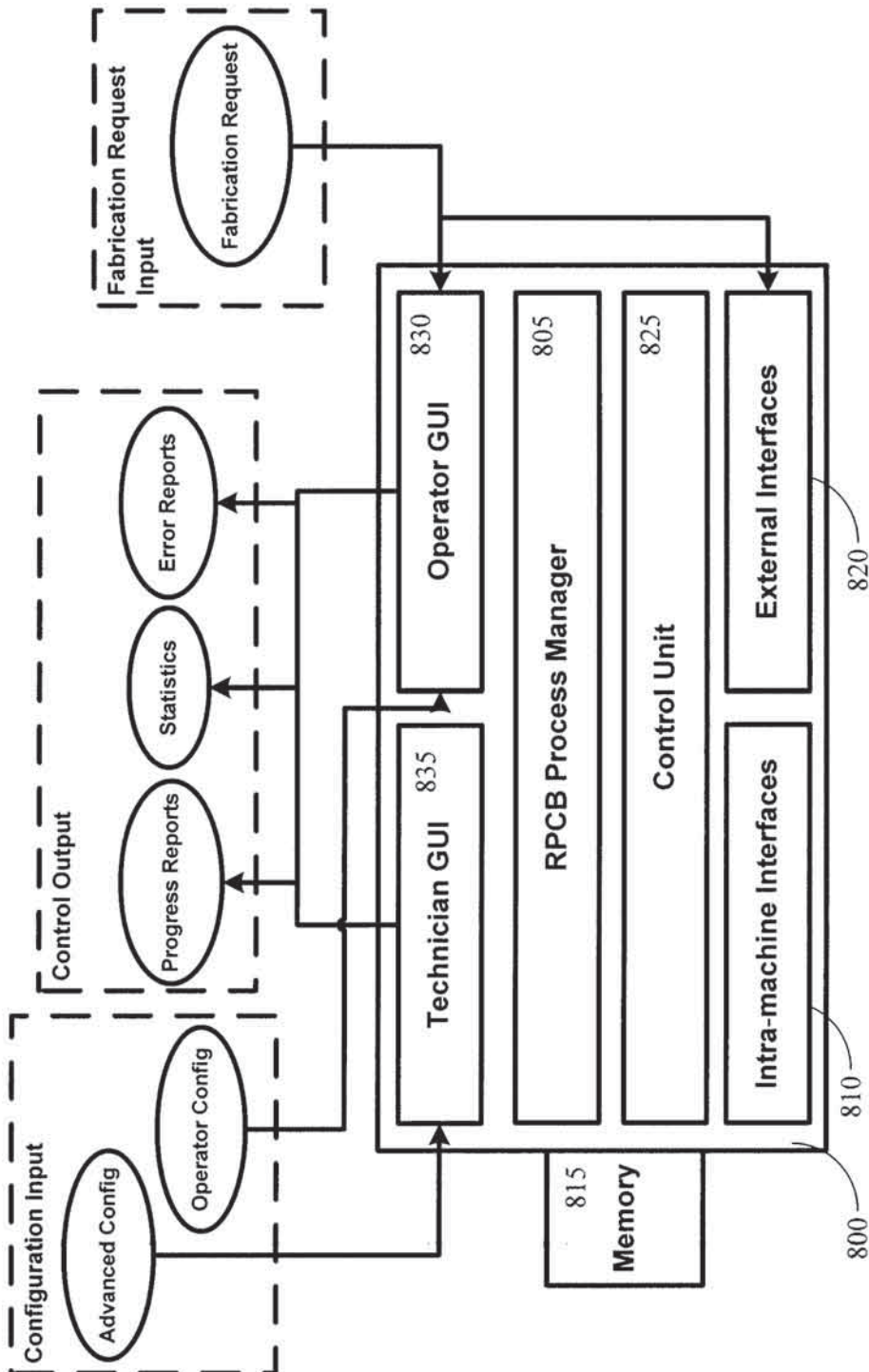
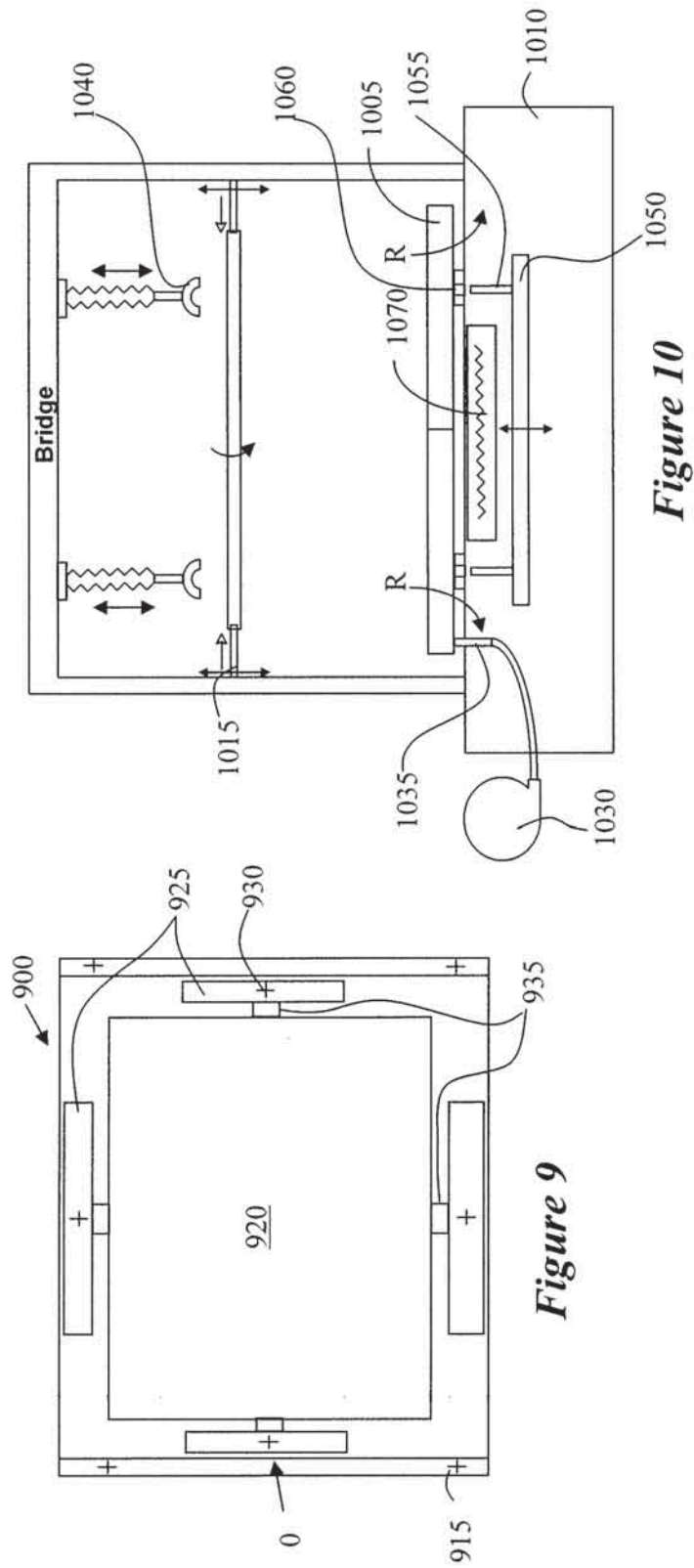


Figure 8



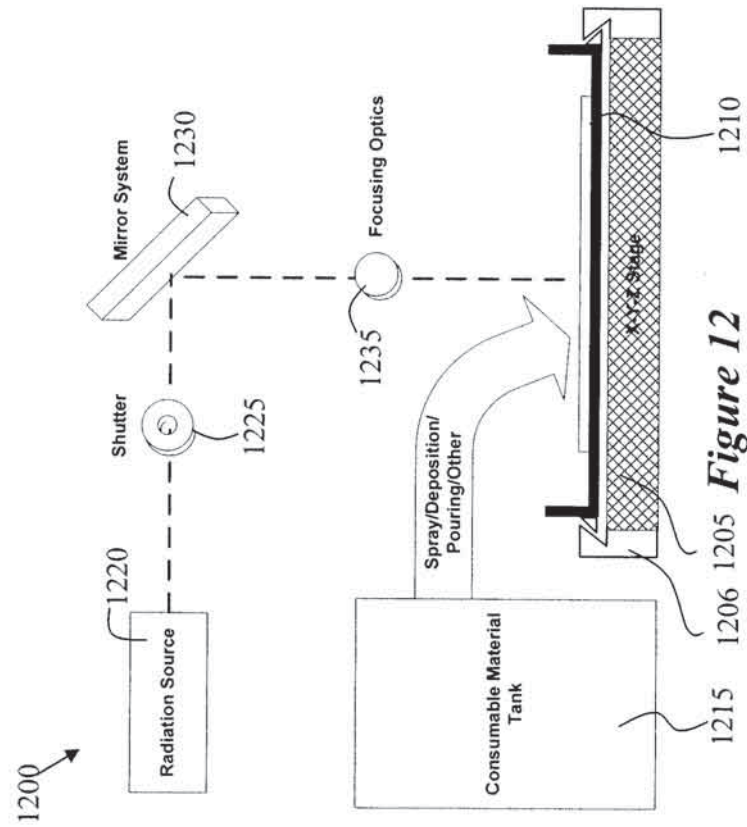


Figure 12

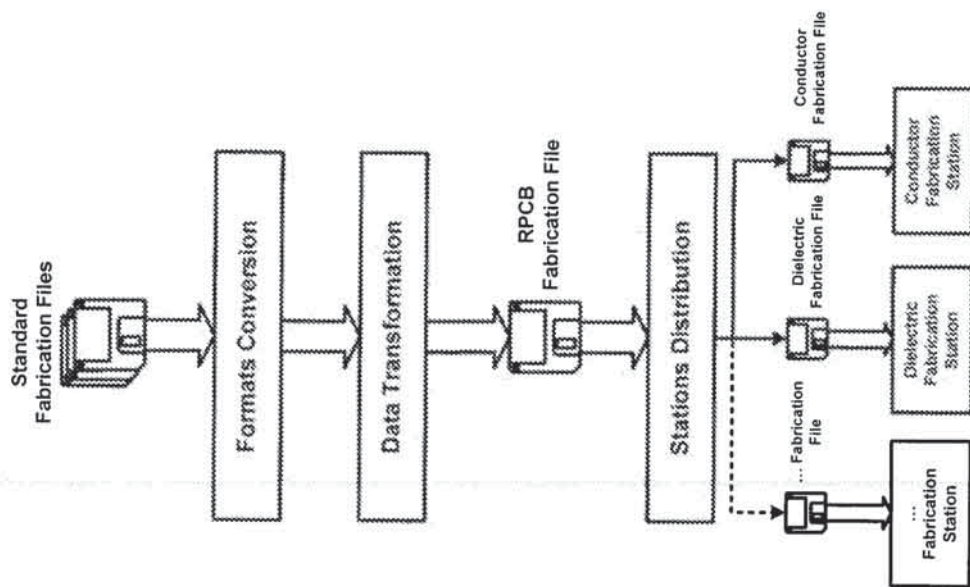
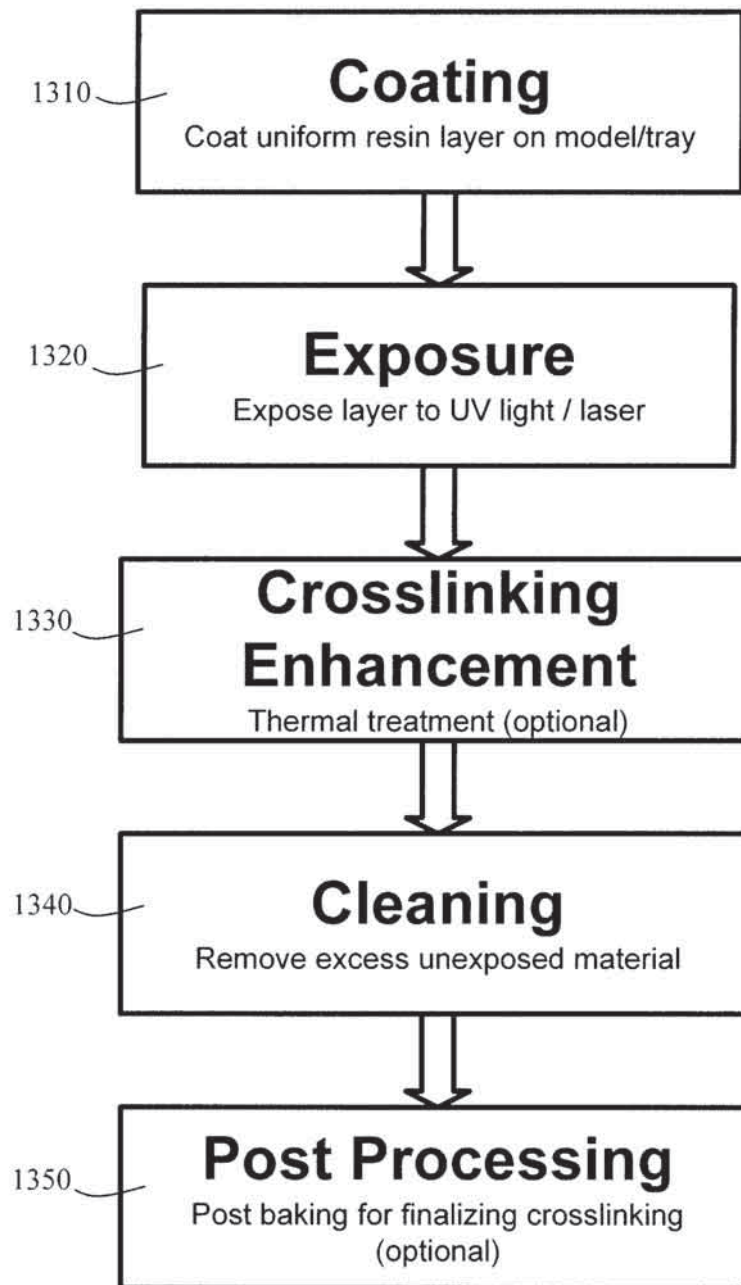


Figure 11

*Figure 13*

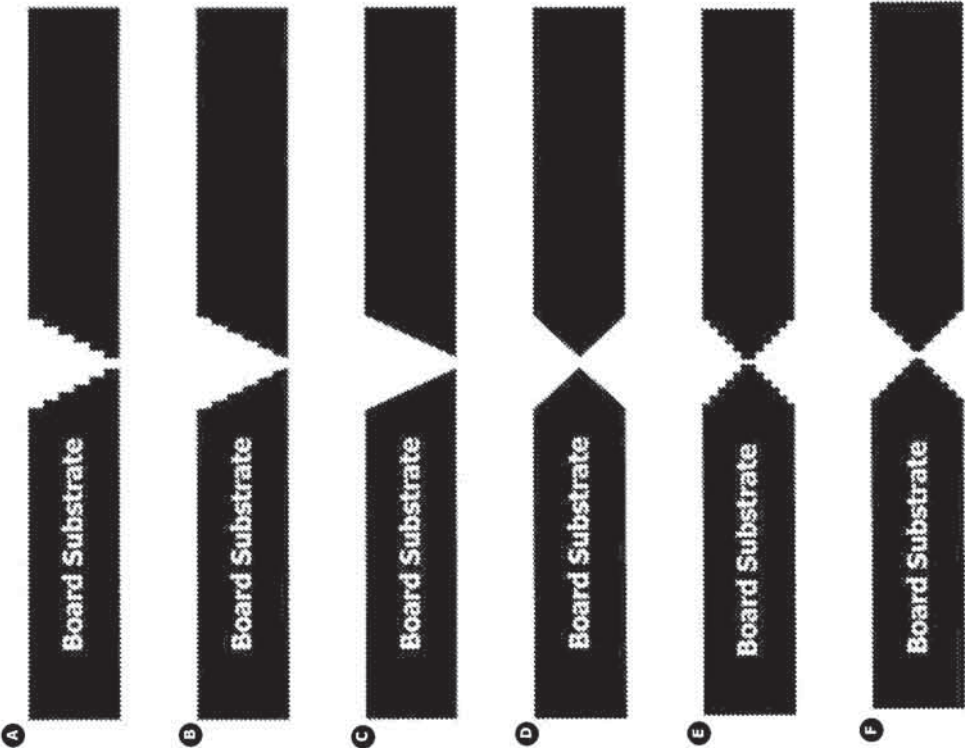


Figure 15

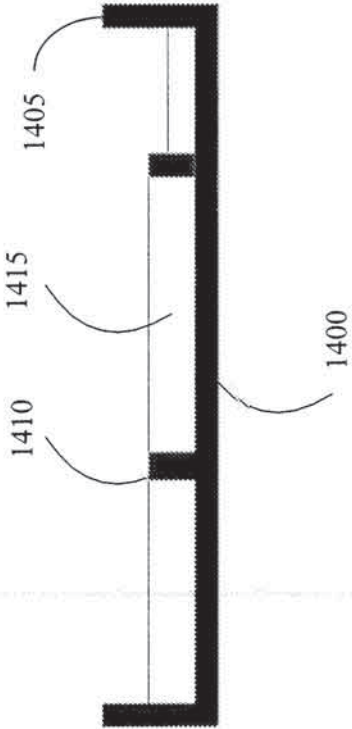


Figure 14

Figure 16B

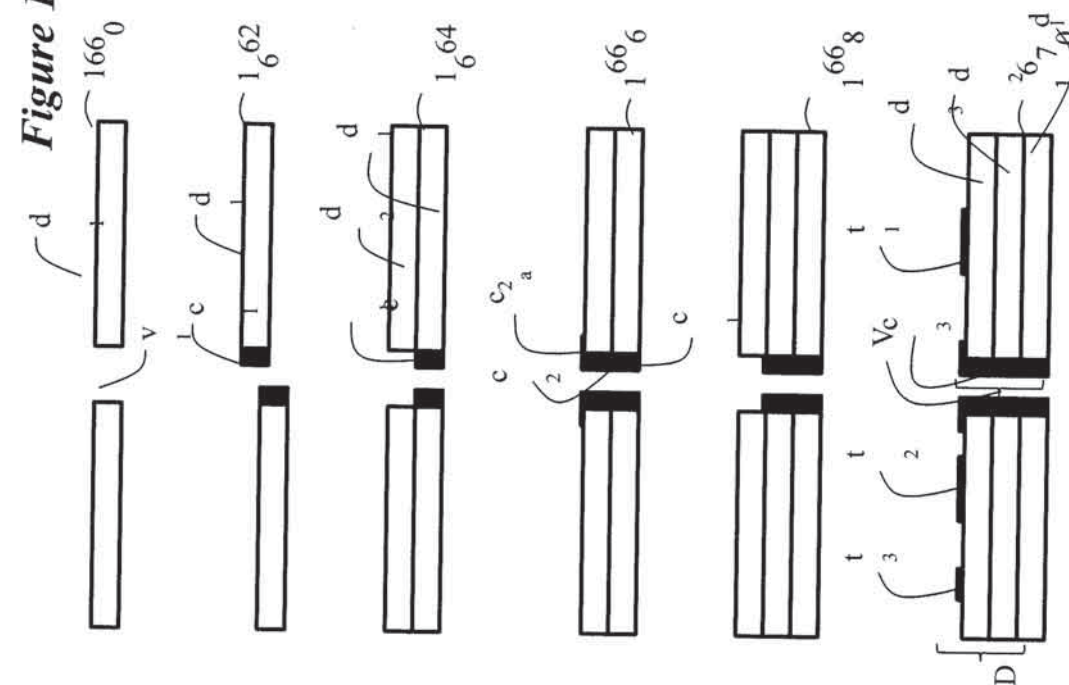
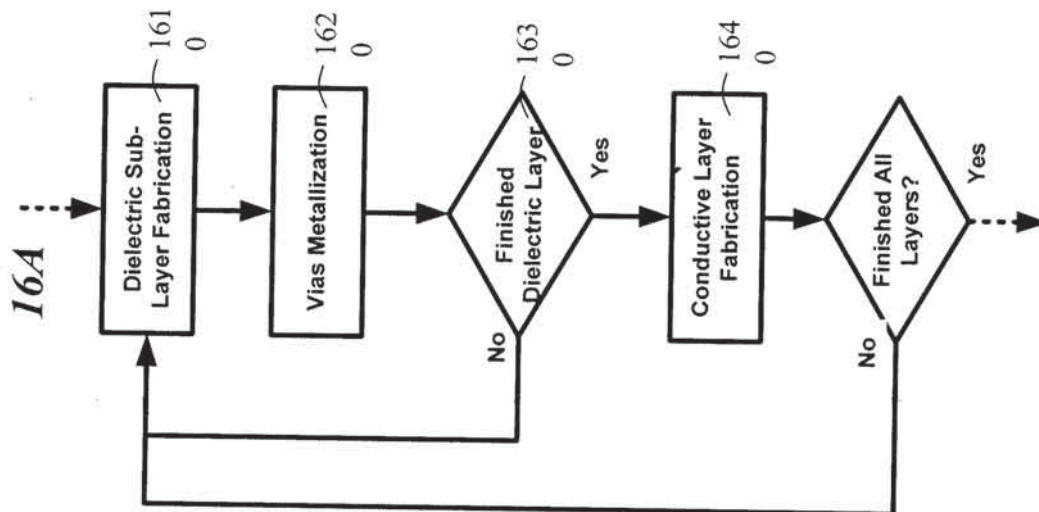


Figure 16A



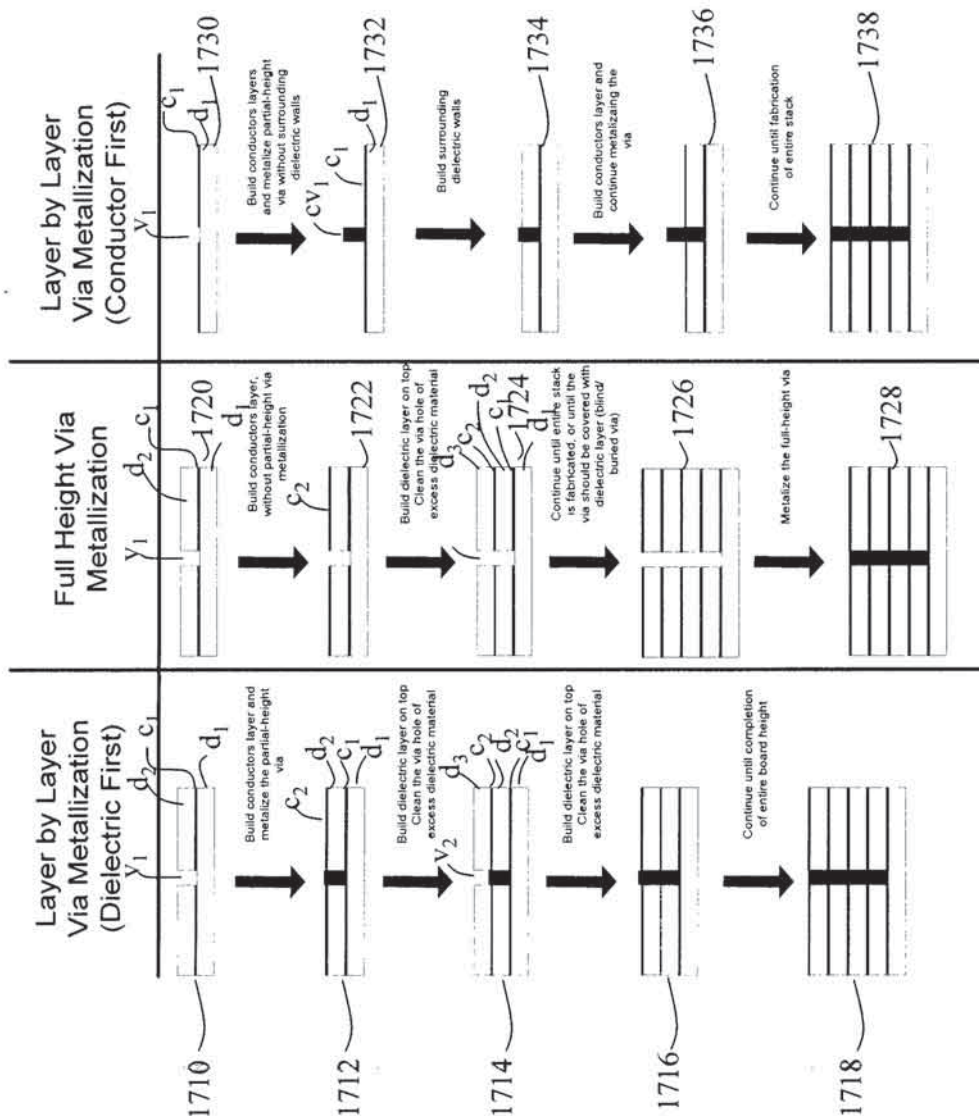
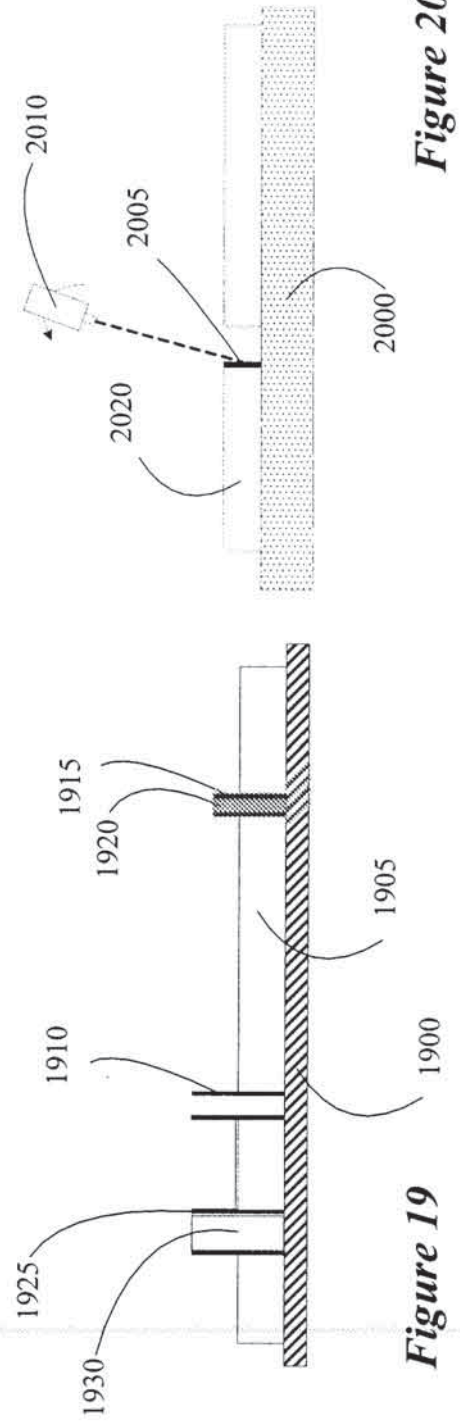
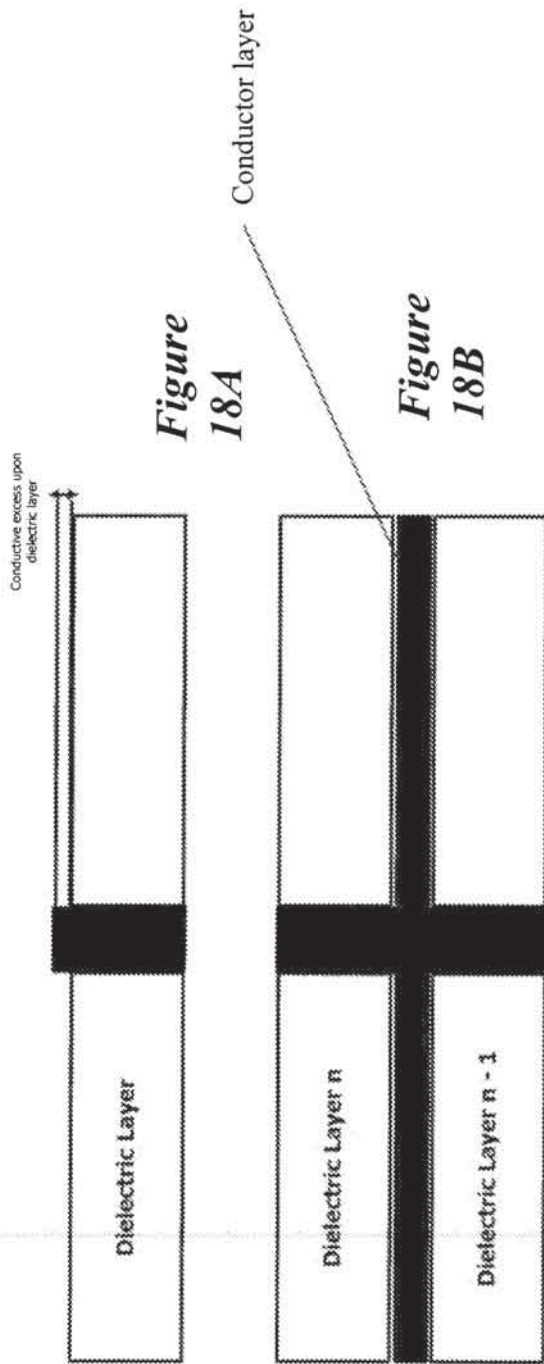


Figure 17C

Figure 17B

Figure 17A



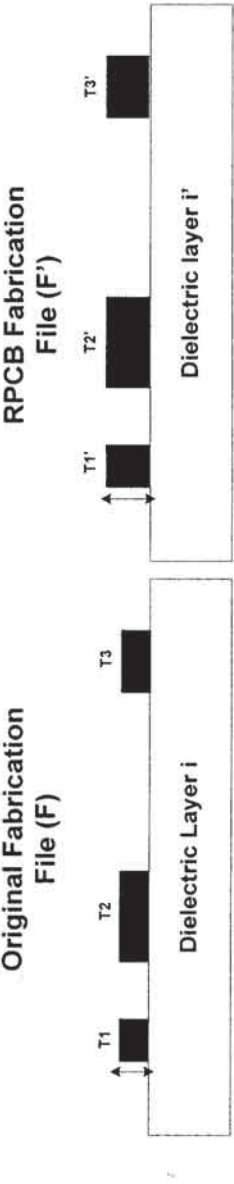
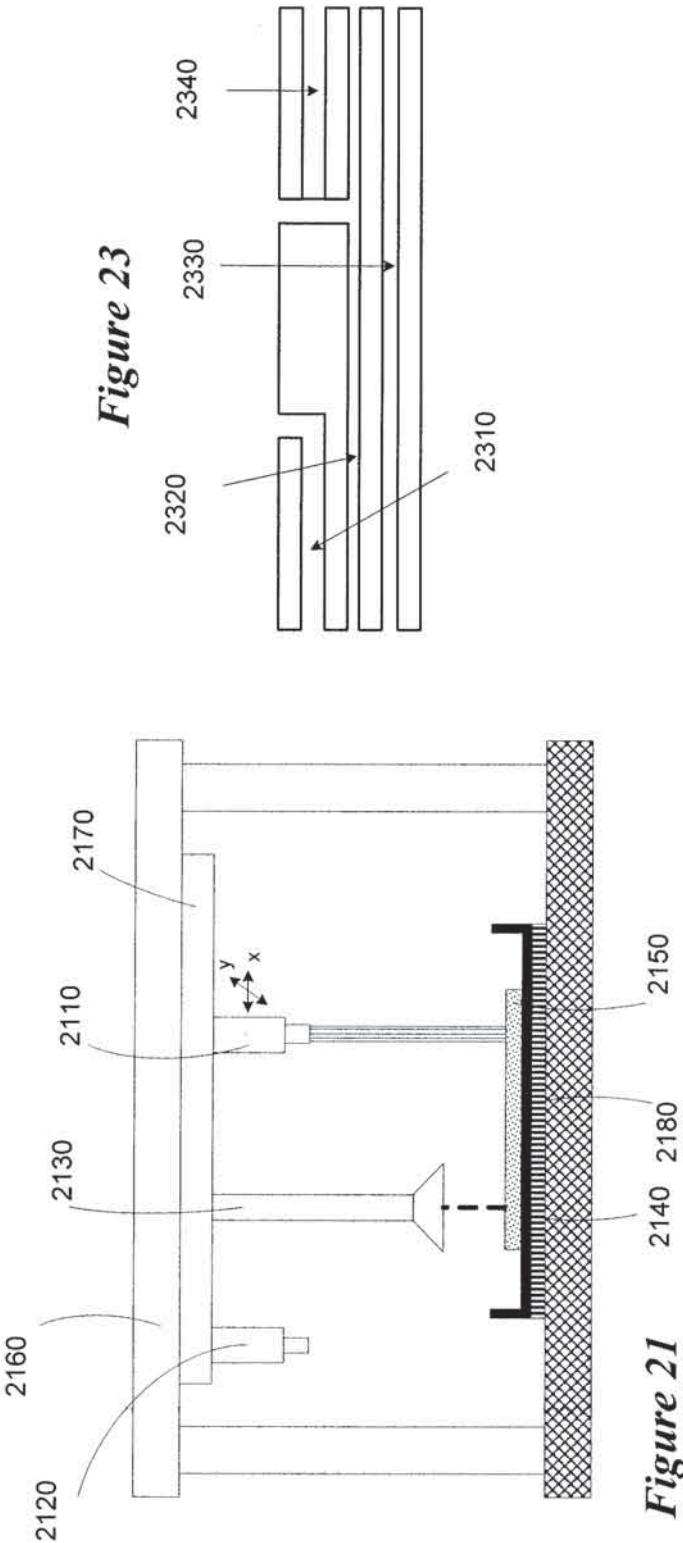


**Figure 24A**

**Figure 24B**

Figure 22A

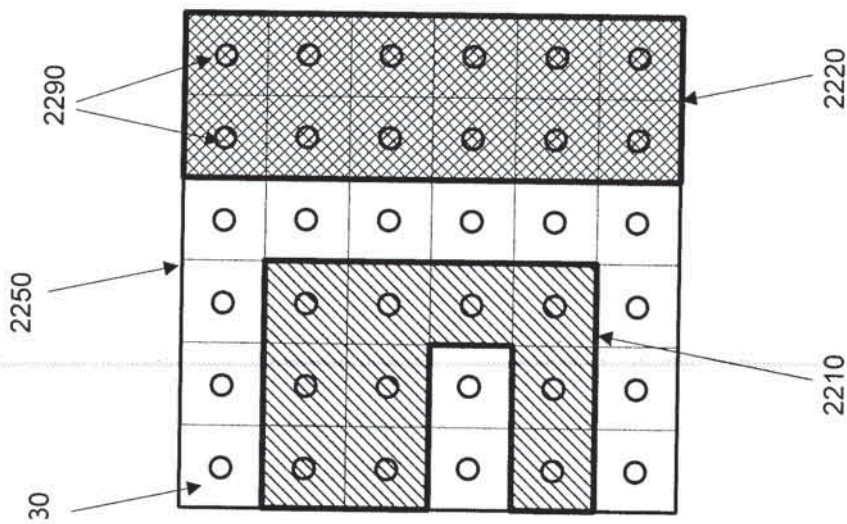


Figure 22B

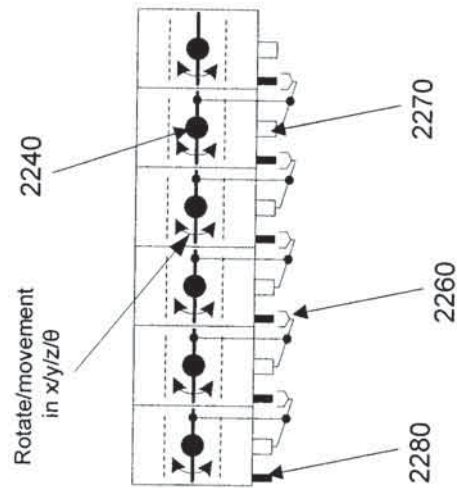


Figure 22C

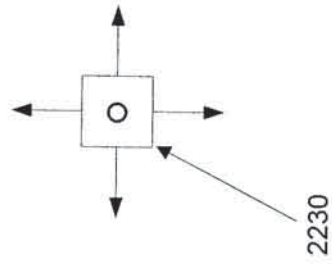


Figure 22D

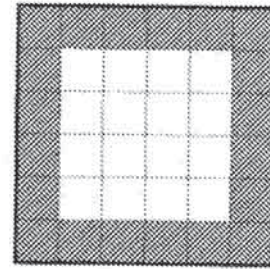
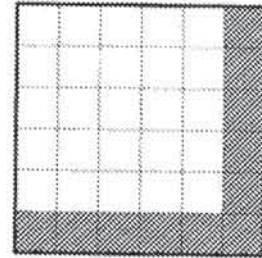


Figure 22E



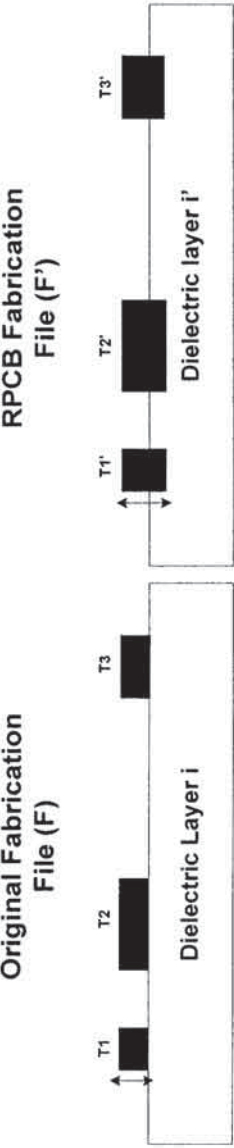


Figure 25A

Figure 25B

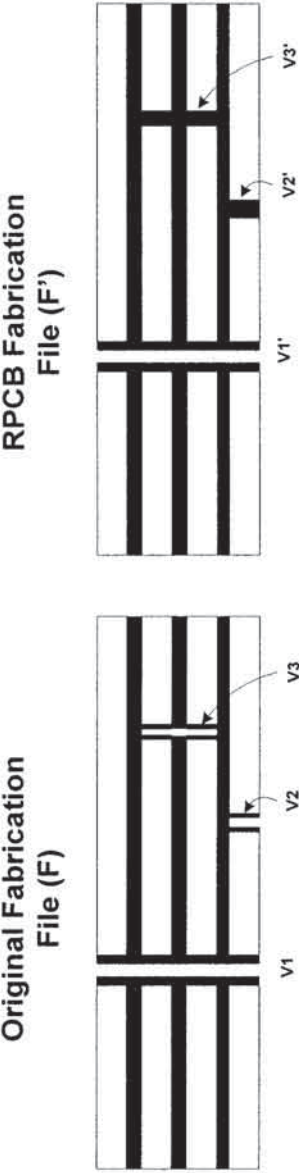


Figure 26A

Figure 26B



Figure 27A

Figure 27B

Original Fabrication  
File (F)

RPCB Fabrication  
File (F')



Figure 28A



Figure 28B