

Current Sources & Voltage References

Linden T. Harrison

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Contents

List of Figures and Photos xiii

List of Tables xxv

Acknowledgements xxix

1. A Short History of References 1

1.1 Introduction 1
1.2 The first JFETs and op amps 3
1.3 The first bandgaps 5
1.4 The buried-zener debuts 7
1.5 Advancements in technology 8
1.6 Other topologies emerge 9

2. An Introduction to Current Sources 13

2.1 An overview 13
2.2 Precision resistors, networks, and trimmers 21
2.3 Essential development equipment 29
2.3.1 Bench power supply unit 29
2.3.2 A thermostatically controlled oven 30
2.3.3 A calibrated, precision ammeter 30

3. The P-N Junction 31

3.1 Characteristics of the P-N junction 31

4. Using BJTs to Create Current Sources 47

4.1 Characteristics of the BJT 49
4.2 Using the BJT as a current source 67
4.3 Widlar current sources 74
4.4 Wilson current mirrors 81
4.5 Wyatt current source 87
4.6 Multiple current mirrors 89
4.7 Cascode current mirrors 91
4.8 Current scaling 95

EX-1006 003
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

4.9 Modified current sources and example applications 102
4.9.1 Running the current source from split power supplies 102
4.9.2 Improving power supply rejection 103
4.9.3 Alternative current divider 104
4.9.4 Modified three-transistor mirror-source 104
4.9.5 Current source linearly charges capacitor in VCO 105
4.9.6 Current source in a high-frequency laser transmitter 107
4.9.7 Temperature-compensated current sink 108
4.9.8 Compound current mirrors 109
4.9.9 Current mirrors help DACs control oscillator frequency and duty cycle 110
4.9.10 Using current sources as active loads 111
4.9.11 Modified current source squares the reference current 113
4.9.12 Digitally controlled variable current source 116
4.9.13 High-pass filter's response is set by compound current mirrors 116
4.9.14 Simple LED current sources 118
4.9.15 A low-noise AC amplifier biased by an LED current source 120
4.9.16 A composite BJT-JFET current source with very high output impedance 121
4.9.17 A composite BJT-MOSFET high-power current source 121
4.9.18 A DAC-controlled current pump uses a Wilson current source 122

5. Using Precision Matched-Pairs, Duals, and Quads 125
5.1 Precision BJT matched-pairs 125
5.2 Quality dual transistors 129
5.2.1 General-purpose BJT duals and quads 133

6. Using JFETs and CRDs to Create Current Sources 137
6.1 The JFET paved the way 137
6.2 Characteristics of the JFET 140
6.3 Using the JFET as a current source 151
6.4 The JFET cascode current source 163
6.5 JFET current regulator diodes 166
6.5.1 Characteristics of the CRD 168
6.5.2 A design guide 175

EX-1006 004
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

6.5.3 An overview of various popular CRD families 175
6.6 Using JFETs to create ultra-low-leakage diodes 180

7. Creating Medium-Power Current Sources with DMOS FETs 185
7.1 Depletion-mode DMOS FETs 186
7.2 The importance of silicon-gate 188
7.3 Characteristics of depletion-mode DMOS FETs 190
7.4 Depletion-mode DMOS current sources 195
7.5 The cascode DMOS current source 197
7.6 The JFET-DMOS cascode current source 199
7.7 Lateral depletion-mode DMOS FETs 200

8. Creating Current Sources with Power MOSFETs 203
8.1 Characteristics of enhancement-mode MOSFETs 204
8.2 Using the enhancement-mode MOSFET as a current source 218
8.3 Using "smart" power MOSFETS 228
8.4 IXYS power MOS current sources 229
8.5 Lateral enhancement-mode MOSFETs 230

9. Using Analog CMOS Arrays to Create Current Sources 231
9.1 RCA pioneered CMOS 231
9.2 Characteristics of CMOS FETs 235
9.3 Using CMOS linear arrays to create current sources 241
9.3.1 CMOS cascode current sources 245
9.4 Using ALD's programmable EPADs® to create precision current sources 252
9.5 ALD breaks the gate-threshold barrier 253

10. Using Monolithic IC Current Sources and Mirrors 261
10.1 National's LM134—a monolithic IC current source 261
10.2 Current source applications for the LM134 266
10.3 Using the LM134 as a temperature sensor 271
10.4 TI/Burr-Brown's REF-200 monolithic current source 273

11. Creating Precision Current Sources with Op Amps and Voltage References 281
11.1 How op amps evolved 281
11.2 Some op amp characteristics 286
11.3 Op amp supply bypassing and input protection 294
11.4 Creating current sources with op amps 296
11.5 Creating precision current regulators with op amps 311

EX-1006 005
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

12. An Introduction to Voltage References **319**

12.1 Introduction and history 319
12.2 Understanding voltage reference specifications 324
12.2.1 Initial accuracy (initial error) 326
12.2.2 Temperature drift (tempco, TC_{Vo}) 326
12.2.3 Long-term drift 332
12.2.4 Noise 333
12.2.5 Thermal hysteresis 335
12.2.6 Line regulation 336
12.2.7 Load regulation 336
12.2.8 Maximum output current rating (I_{OUT}; mA) 336
12.2.9 Supply voltage range 336
12.2.10 Supply current (I_S) or quiescent current (I_Q) 337
12.2.11 Dropout voltage 338
12.2.12 Turn-on settling time (t_{on}; μS) 338
12.2.13 Turn-on drift (dV/T) 338
12.2.14 Transient response 338
12.2.15 Sleep/Enable 338
12.2.16 Power dissipation 338
12.3 Enhancing the voltage reference design 339
12.3.1 Input and output bypassing 339
12.3.2 Noise reduction 341
12.3.3 Trimming 346
12.4 Unused terminals on the package 354
12.5 Package types 355
12.6 PCB layout 356
12.7 Why not do it yourself? 356
12.8 Comparing precision 359

13. The zener Diode and the TC zener Reference **363**

13.1 Introduction 363
13.2 Characteristics of the zener diode 365
13.3 Some simple zener applications 382
13.4 Temperature-compensated zeners 393

14. Characteristics of Monolithic Voltage References **403**

14.1 Bandgap voltage references 404
14.2 Buried-zener voltage references 415
14.3 The XFET® voltage reference 421
14.4 The Intersil/Xicor FGA™ voltage reference 424
14.5 Low-voltage considerations 426

14.6 Comparing the different topologies 433

15. A Review of Some Outstanding Monolithic Voltage References and Their Applications 437

Introduction 437
15.1 Applying the bandgap shunt reference 438
Analog Devices ADR510 441
Analog Devices ADR520 442
National Semiconductor LM4051-ADJ 444
Maxim MAX6138 446
Maxim MAX6006 448
Linear Technology LT1634 449
Linear Technology LT1389 449
15.2 Applying fixed-series bandgap references 451
Linear Technology LT1461 453
National Semiconductor LM4140 455
National Semiconductor LM4130 457
Analog Devices ADR390 458
Analog Devices ADR280 459
Analog Devices AD780 461
Maxim MAX6129 463
Maxim MAX6126 465
15.3 Applying adjustable-series bandgaps 466
Linear Technology LT6650 466
Maxim MAX6325 469
Maxim MAX6037-ADJ 470
Intersil/Xicor x60250 472
Analog Devices ADR01 474
Digital compensation 476
15.4 Using the Analog Devices' XFET® reference 478
Analog Devices ADR431A 479
15.5 Applying buried-zener references 483
Analog Devices AD688 484
Analog Devices AD586 486
Texas Instruments REF102 488
Linear Technology LT1021 490
Linear Technology LTZ1000 491
15.6 Applying the Intersil/Xicor FGA™ X60008 494
Intersil/Xicor x60008 495
Creating precision current source circuits 498
ISL60002 498

EX-1006 007
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

ISL60007 498
15.7 Multiple voltage references and multiple loads 501
Digitally selectable 5-reference calibrator 502
Same voltage to multiple loads 503
15.8 Monolithic voltage references—a look to the future 506

A. References and Tables 513
Power of 10 and Equivalents 513
Temperature scale conversion 515
Precision resistor comparisons 515
Gain vs. dB conversion Table 516
Reactance chart for filter design 517
Small signal model for the BJT 518
Simplified BJT models 518
BJT operating modes Table 519
JFET models 519
MOS transistor models 520
PPM to % converter 521
Allowable noise levels for n-bit systems 521
Different voltage reference configurations 522
Allowable tempco requirements 523

B. Glossary 525

C. Bibliography 535
C.1 PART I—Current Sources 535
C.2 PART II—Voltage References 540

D. Contact Information 543
D.1 SEMICONDUCTOR MANUFACTURERS 543
D.2 ELECTRONICS DISTRIBUTORS 549
D.3 PRECISION PASSIVES MANUFACTURERS 550
D.4 INSTRUMENTATION MANUFACTURERS 555
D.5 Magazines & Periodicals 557

Index 559

EX-1006 008
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

Chapter 4

Using BJTs to Create Current Sources

Today's silicon planar, epitaxial, bipolar junction transistors are but distant cousins of the early transistors invented at Bell Labs. Transistors have been the subject of hundreds of millions of dollars worth of research over the years, yet today we can buy them for pennies. As with the early development of the Internet by the U.S. Defense Advanced Research Projects Agency (DARPA), so it was with the support of the U.S. Department of Defense, particularly by the Air Force, that fueled the early R&D work into both the transistor and the integrated circuit. Airplanes, rockets, and missiles have payload, weight, and reliability concerns, which solid-state electronics helped improve dramatically. The Cold War was a propelling factor in this advance for the U.S. military, paralleled by the race to the moon and into space by NASA.

It is interesting to note that the earliest transistors were germanium (Ge) point-contact and mesa PNP types, which suffered from severe leakage, low resistance, and temperature drift, among other things. One recurring problem was that impurities seemed to settle on the surface of the chip (surface states) or at its junctions, causing the intended design specifications to shift unpredictably. Another more baffling question was why germanium reportedly turned from N-type to P-type material when it was heated, then allowed to cool. Then there were the persistently poor yield problems, which plagued transistor manufacturers for years. In some cases, manufacturers would get as little as one working transistor per wafer—not a very efficient or profitable situation. Although the semiconductor industry has always been competitive, it has for the most part shared much of the basic technology within itself. With that in mind, research continued at a frantic pace as every manufacturer tried to find the solutions to the yield and reliability problems that plagued the industry.

It was not until the early 1950s that the first germanium transistor was commercially developed and more than a decade later that practical NPN silicon types became commercially available and affordable. In the ten years following the debut of the first point-contact germanium transistor at Bell Labs, about a dozen other types were introduced (each of which depended on the process used in its manufacture). These included the grown junction, the alloy junction, the micro-alloy diffused junction, the epitaxial base type, and many others—all germanium. By the mid-50s, Raytheon was the largest transistor maker, producing roughly half of the world's market needs. It's largest market was supplying transistors to makers of hearing aids.

EX-1006 009
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

Although both germanium and silicon display a negative temperature coefficient (-ve TC), in that their resistance decreases with increasing temperature, it was found that a germanium transistor's resistance was far lower than that of its silicon counterpart, by a ratio of about 1000:1. It also had a correspondingly higher leakage current than silicon. Germanium offered a lower forward voltage than silicon (Figure 4.1), but it had a sloppy reverse characteristic, resulting in a soft knee (see Figure 4.1). Because of silicon's improved temperature characteristics and operating range, designers gradually switched away from the troublesome germanium transistors and used silicon almost exclusively.

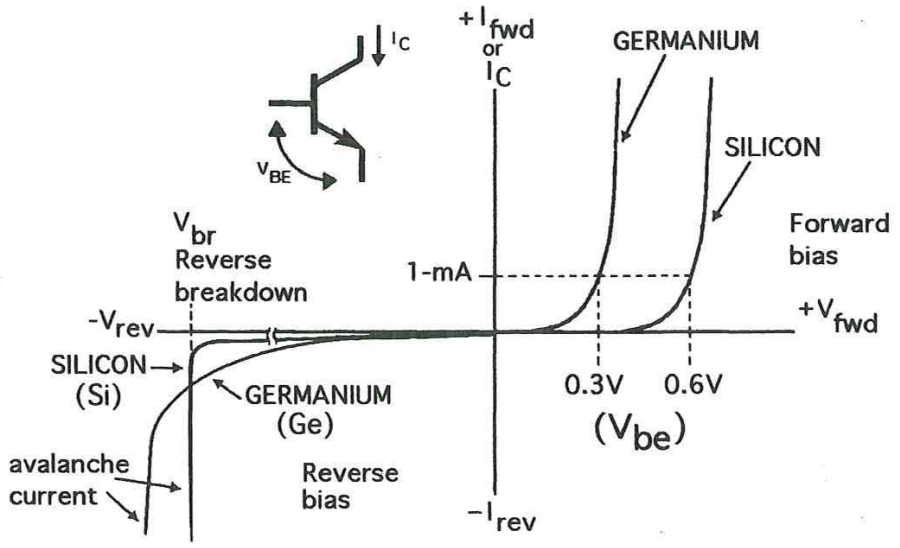


Figure 4.1. Comparing Germanium's V-I curve with Silicon's. While Germanium has a lower Vf_{wd} and V_{be}, it also has a very poor reverse characteristic.

So it followed that after 1954, when the first silicon transistors were introduced by Texas Instruments, most transistors and then integrated circuits used silicon, whether digital or analog, until the advent of gallium arsenide (GaAs) microwave transistors in the 1960s. The *epitaxial process* developed by Dr. Ian Ross's group at Bell Labs helped cure some of these manufacturing problems, while a little later (1959), Fairchild Semiconductor's Dr. Jean Hoerni's introduction of the *planar* silicon structure cured many more. Those two processes are the foundation of all of today's semiconductors. As other processes were developed over the course of time (such as Radiation Inc.'s *dielectric isolation* in the mid-60s, then Fairchild Semiconductor's isoplanar™ [isolated-planar] process in 1971), the yields went up, as did quality and device repeatability. Others contributed greatly, such as Transitron, National Semiconductor, Raytheon, Delco, Motorola Semiconductor, and General Electric, along with its sub-

EX-1006 010
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

sidiary RCA, which created some of the best power transistors ever made. The development and manufacture of a low-cost, reliable silicon transistor paved the way for all of today's integrated circuits.

In the United States, the following semiconductor manufacturers make today's discrete, small-signal silicon BJTs:

- Central Semiconductor
- Crystalonics
- Diodes, Inc.
- Fairchild Semiconductor
- Linear Integrated Systems
- Microsemi
- ON Semiconductor
- Philips Semiconductors
- Vishay
- Zetex

It's a tribute to all of the companies mentioned here, as well as the thousands of researchers and BJT engineers from the 1960s and '70s, that many of the products they created and modeled are still available today, some 40 years later, and still finding new applications in today's wireless digital world.

4.1 Characteristics of the BJT

The silicon planar, epitaxial, bipolar junction transistor (BJT) is both remarkably simple and complex at the same time. It is a current-operated semiconductor device, usually having three terminals that are designated the *base*, the *collector*, and the *emitter*. It is referred to as *planar* because of its design, which creates all three terminal connections at the surface of the chip. It is *epitaxial* because the chip is created in precisely controlled layers (epitaxy). It is referred to as a *junction transistor* because its inherent design creates distinct junctions between the P and N materials of which it is made. Actually, it has two junctions, unlike a diode, which has just one. It is referred to as a *bipolar* device because both electrons and holes are involved in the current flow. The transistor is available in either polarity, referred to as either an NPN or a PNP type. This is shown in Figure 4.2, together with the relevant polarities, currents, and voltages.

NPN types have free electrons, which are negative carriers, whereas PNP types have free holes, which are positive carriers. One sometimes hears the expression *hole current*, which refers to PNPs, or likewise *electron current*, which refers to NPNs. Electrons have a higher mobility than holes, and as a result tend to move faster through

EX-1006 011
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

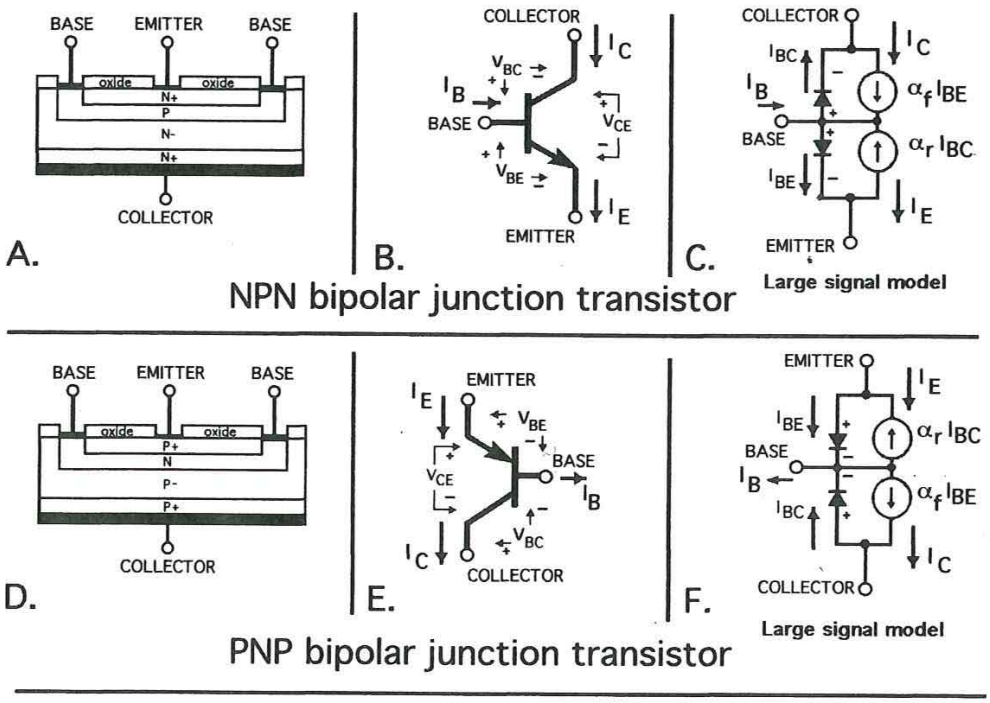


Figure 4.2. *Showing the structure of the BJT, as well as its various voltages, currents, and polarities. Notice the two inherent diodes that provide forward and reverse bias.*

the semiconductor crystal material. This higher speed capability translates into the fact that NPN types are more popular than PNPs. (This is true for not only BJTs but FETs too.) Advances over the past decade have closed the gap considerably between PNP/P-types and NPN/N-types, so that their speeds are much closer. BJTs are available as individual discretes and also as matched-pairs, duals, quads, and arrays, in standard metal, plastic, and surface-mount packages (Figure 4.3). In creating any kind of current source with BJTs, the best results will always be obtained when the devices used are matched-pairs or quads in a single package.

The BJT, being a three-lead device, is capable of three distinct modes of operation. These are the common base (CB), the common collector (CC), and the most familiar—the common emitter (CE). Table 4.1 summarizes some of the basic characteristics of the BJT's three operating modes. As you can see, the CE configuration provides a current gain, a voltage gain, and a power gain, which underscores its popularity. Small-signal transistors are generally categorized into several different types, namely general-purpose amplifiers, switching transistors, high-frequency RF (VHF/UHF) amplifiers, choppers, high-voltage, and low-noise. In addition, there are Darlington, medium-power, and power transistors. In theory, most of these can function as current sources,

EX-1006 012
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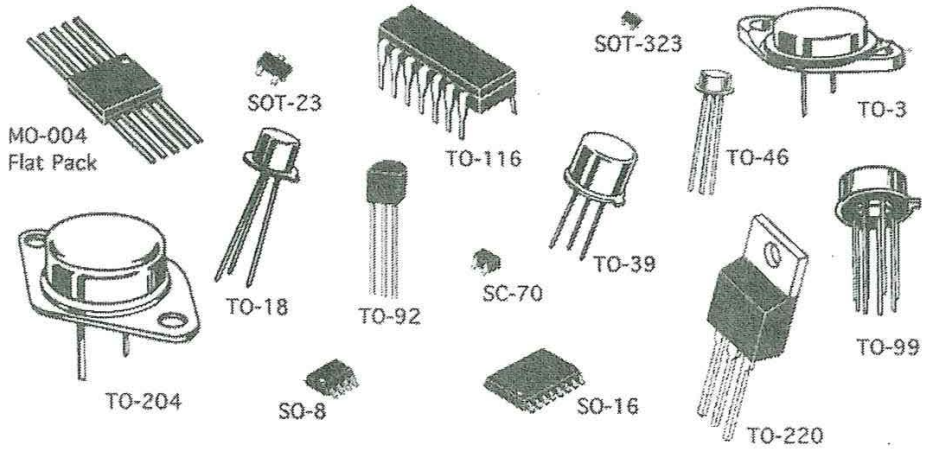


Figure 4.3. Examples of popular transistor packages.

with the exception of the Darlington type, which is generally considered to have poor bandwidth. Typically, general-purpose, low-noise, and high-frequency (small-signal) types are used in creating current sources.

In addition, the BJT has some unique subscript notations, which reference either the connection, current flow, or test condition used. In some situations one, two, or three subscript letters may be used. For example, I_C refers to the collector current, while C_{CB} refers to the capacitance between the collector and base. The term I_{CES} refers to the collector-to-emitter current, with the base shorted. (The last letter "S" refers to the condition of the remaining terminal, in this case the base, which is designated as being shorted to the common terminal, always the middle of the three subscript letters.) Thus, I_{CBO} refers to the collector-to-base leakage current, with the emitter terminal open (O) circuit and not shorted. The term $V_{CE(sat)}$ refers to the collector-to-emitter saturation voltage, measured at a particular collector current. The term h_{fe} refers to the forward (designated by "f") gain characteristic in CE mode (designated by "e"). A detailed study of the BJT is beyond the scope of this book, but some additional BJT equations and models are given in Appendix A. We will look here at some of the transistor's more relevant characteristics when viewed as potential current sources.

EX-1006 013
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Characteristic:	Common Base (CB)	Common Emitter (CE)	Common Collector (CC)
Current Gain:	No (< x1)	Yes	Yes
Voltage Gain:	Yes	Yes	No (< x1)
Power Gain:	Yes	Yes	Yes
Z_{in} (Ω) typical:	Low (< 100Ω)	Low (1KΩ)	High (>250KΩ)
Z_{out} (Ω) typical:	High (1MΩ)	High (50KΩ)	Low (< 500Ω)
Gain Formula:	$h_{fb} = \frac{I_C}{I_E}$	$h_{fe} = \frac{I_C}{I_B}$	$h_{fc} = \frac{I_E}{I_B}$

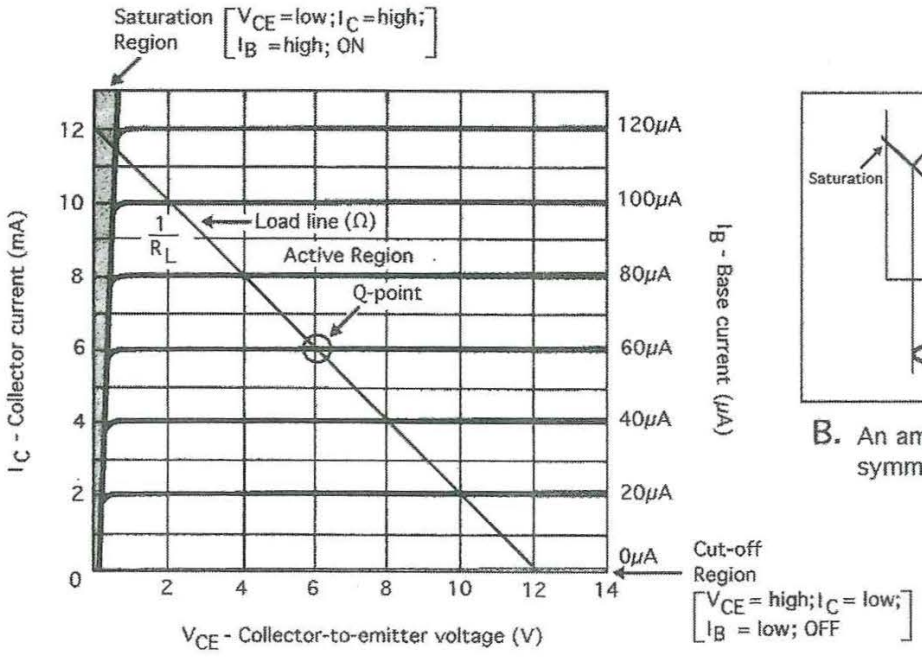
Table 4.1 Transistor operating modes

In the structure of the BJT, the base area is made narrow and is lightly doped. The NPN transistor has a P-type base, whereas the PNP has an N-type base. In order to function properly, the two junctions must be correctly biased. With an NPN transistor, the collector-base junction must be reverse-biased as seen from the base terminal, while the base-emitter junction must be forward-biased. This means that its collector must be positive/more positive than its base, and its emitter more negative than its base. With a PNP transistor the opposite is true: its collector-base junction must be forward-biased, while the base-emitter junction must be reverse-biased. This means that its emitter must be positive/more positive than its base, and its collector must be more negative than its base (see Figure 4.2).

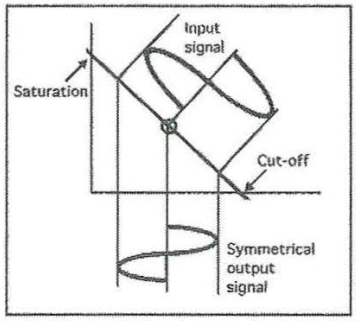
The bipolar transistor (both NPN and PNP) is a normally-off device until sufficient voltage (V_{BE}) and base current (I_B) are provided to turn it on, because it is a current-controlled device. The transistor can be biased into any one of three states: *cutoff* (off), *saturated* (full-on), or *active* (a predetermined state facilitated by biasing it halfway between saturation and cutoff) (Figure 4.4A). For example, in a 12-volt amplifier circuit, the transistor would normally be biased midway between the supply rails at 6 volts, to ensure a perfectly symmetrical AC signal swing (assuming that the input signal was also at the correct level) (Figure 4.4B).

The BJT relies on a small forward base current (I_{BE}) and a small forward voltage (V_{BE}) at its base, inducing and controlling a much larger forward current between the collector and the emitter. The base current (I_B) is very small in comparison with the collector and emitter currents. For small-signal transistors switching a few milliamps, the base current will likely be in microamps. The base current can be determined by:

EX-1006 014
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.



A. Typical transistor amplifier characteristics showing the load line and the three operating regions.



B. An amplifier's linear and symmetrical operation.

Figure 4.4. Some BJT characteristics.

$$I_B = I_E - I_C \qquad \text{(Eq.4.1)}$$

This current transfer relationship between base and collector is referred to as the *forward beta* or the *forward current gain* (aka β, βf, h_{FE}, or h_{fe}) in the CE configuration. To be meaningful, the gain should be specified at a particular collector-emitter voltage (V_{CE}), collector current (I_C), base current (I_B), and temperature. For example, the popular 2N3904 NPN general-purpose amplifier is specified at 25°C as having a minimum DC current gain of 70, when measured with a V_{CE} of 1 volt and a collector current of 1 mA. Its counterpart, the equally popular 2N3906 PNP general-purpose amplifier, is specified as having a minimum DC current gain of 80, under the same conditions. There is also a *reverse beta* (βr),which is sometimes referred to in technical material. However, for our purposes, gain is assumed to mean forward beta unless otherwise specified.

EX-1006 015
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

Under normal conditions, gain can be simply defined by the following:

$$\beta = \frac{I_C}{I_B} \qquad \text{(Eq.4.2)}$$

where,

$$I_C = \beta I_B \qquad \text{(Eq.4.3)}$$

and therefore:

$$I_B = \frac{I_C}{\beta} \qquad \text{(Eq.4.4)}$$

For example, let's assume we have an ideal NPN transistor, with no leakage. If we applied 10-μA current to its base and 1-mA current is induced to flow between its collector to emitter, then the transistor would theoretically have a beta of 100. From equation 4.2 we can calculate this as shown in equation 4.5:

$$\beta = \frac{1000\ \mu A}{10\ \mu A} = 100 \qquad \text{(Eq.4.5)}$$

A standard test circuit for measuring the BJT's gain is shown in Figure 4.5. Here two current meters are used, which allow one to see the corresponding collector current, for any particular applied base current.

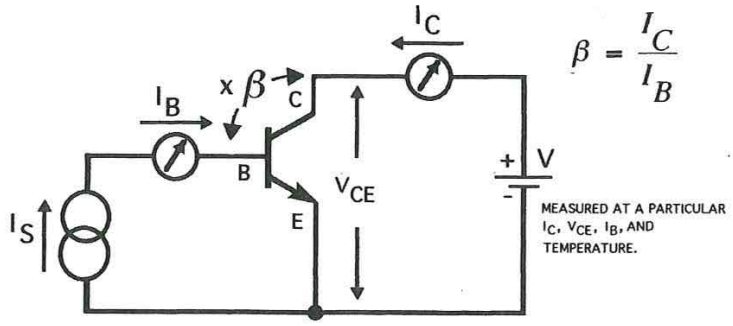


Figure 4.5. Current gain (h_{FE}) test circuit.

While in theory the base current alone directly controls the collector current via the transistor's beta, other factors can also contribute. For example, the base-to-emitter

EX-1006 016
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

voltage affects gain, because it determines the base current. The typical base voltage for a small-signal transistor ranges from about 0.65 to 0.95 volt. Too low a base voltage will not permit enough base current to flow, which will in turn restrict the amount of collector current. Another factor that can affect gain and cause unforeseen problems is by operating the device too close to its maximum V_{CE} voltage rating—a situation that should definitely be avoided.

Temperature can also affect beta, as shown in Figure 4.6. The two graphs clearly show that for most transistors gain increases with an increase in temperature. It shows the performance of two popular metal can transistors—the NPN 2N2222A and the PNP 2N2907A—over the full military temperature range. (Both devices are available in various other packages, including plastic, DIP, and surface-mount duals and quads.) In the case of the 2N2222A, the graph shows that with a V_{CE} of 1 volt and a collector current of 15 mA, gain increases by about 90% at 175°C, from its normalized value at 25°C. Likewise, h_{FE} decreases by about 50% at –55°C. With the 2N2907, gain also increases with temperature, although not quite as much (75%) because it is PNP, and it too decreases by about 50% at –55°C. In either case, increasing V_{CE} to 10 volts produces similar results over the same temperature range. Note that for either device, gain decreases beyond 60 or 70 mA, irrespective of collector-emitter voltage or temperature. As you can see, gain is most affected by collector current and temperature.

Gain is therefore temperature sensitive, and so with a small-signal transistor operating at low to medium currents, its gain will have a small positive temperature coefficient of between +0.3% to approximately +0.7%/°C, partly because of leakage currents, which we will cover shortly. In the transistor's saturation region, this changes to a small negative tempco of about –0.25%/°C.

Gain is a variable parameter that is difficult to control in processing and manufacturing. As a result, manufacturers normally provide only a minimum gain specification. The particular process will yield a range of gains, where any one device's value may typically range from, say, 100 to 350. Usually the manufacturer will test devices according to gain or some other desirable parameter such as $V_{CE\ max}$, and sort them into separate bins, categories, and part numbers. Devices with higher gains, or with gains close together, may cost more. Small-signal transistors tend to have gains ranging from around 60 to several hundred, whereas power transistors tend to have much lower gains, typically less than 50.

Exceptions to this include Darlington transistors, which can have gains of several hundred to several thousand, and special super-gain transistors created by semiconductor makers in the manufacture of analog ICs. These are specially processed BJTs that give very high gains (typically several thousand), but at the expense of breakdown voltage (just a few volts). However, by combining these super-gain transistors with regular IC transistors in a cascode configuration, it allows an IC design (typically an op amp) to achieve both high gain and a normal level of breakdown voltage. Super-gain transistors were first used in the architecture of the LM108 op amp in 1969.

EX-1006 017
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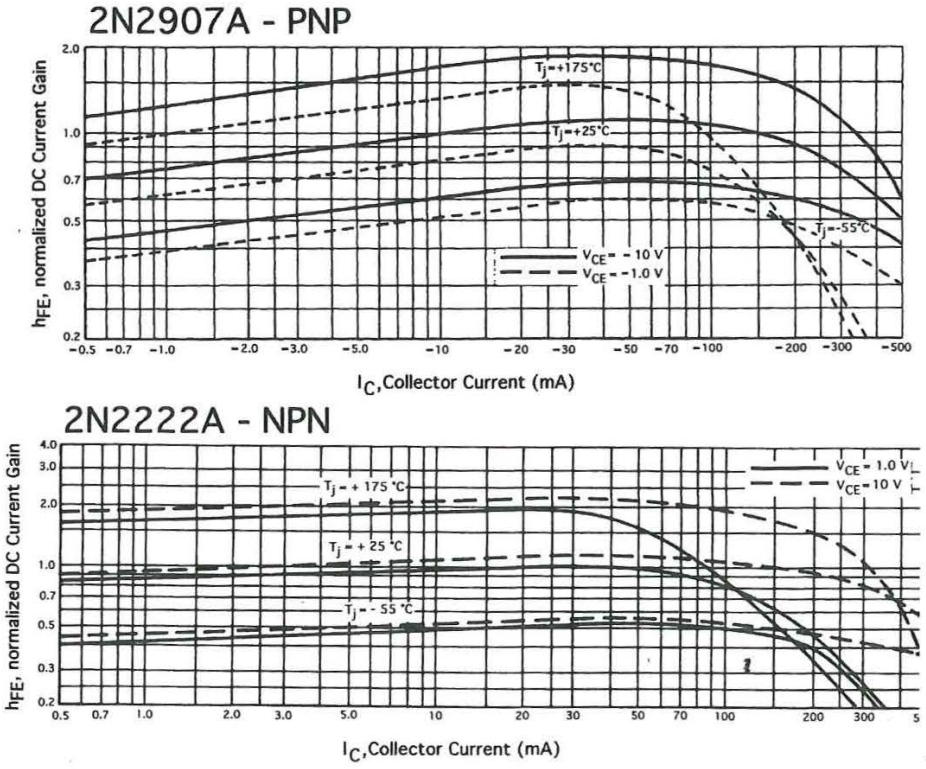


Figure 4.6. *Showing how temperature affects h_{FE}, and therefore the collector current for two popular general-purpose transistors, the PNP 2N2907A (upper graph) and the NPN 2N2222A (lower graph). Notice particularly how as temperature increases, that h_{FE} also increases, irrespective of whether the collector-emitter voltage is 1 volt or 10 volts.*

The transistor's beta is also interrelated with another mechanism called the *alpha* (α). Both of these characteristics are shown in Figure 4.7. Alpha is a figure of merit and a measure of the current gain between the emitter and collector, in the common-base configuration. This is not usually mentioned on a transistor's data sheet, as it is with beta or h_{FE}. It stands to reason that because few current carriers ever reach the collector from the emitter, the collector current will always be slightly less than the emitter current. Alpha usually ranges from 0.98 to 0.999 for today's silicon transistors. (Although beyond the scope of this book, alpha is composed of three other factors,

EX-1006 018
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

namely the collector efficiency, the emitter efficiency, and the base transport factor.) Alpha is related to these and can easily be determined from:

$$\alpha = \frac{I_C}{I_E} \qquad \text{(Eq.4.6)}$$

also:

$$\alpha = \frac{\beta}{1 + \beta} \qquad \text{(Eq.4.7)}$$

The alpha is directly related to the beta by:

$$\beta = \frac{\alpha}{1 - \alpha} \qquad \text{(Eq.4.8)}$$

As an example, if alpha equals 0.99, then from equation 4.8:

$$\beta = \frac{0.99}{1 - 0.99} = \frac{0.99}{0.01} = 99 \qquad \text{(Eq.4.9)}$$

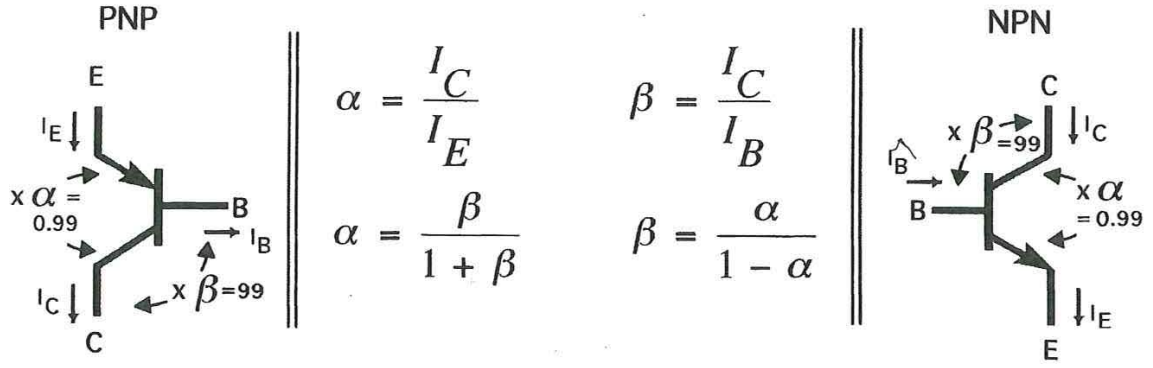


Figure 4.7. *Showing the mechanisms of alpha (α) and beta (β) in the bipolar junction transistor. Alpha relates to the collector current (I_C) versus emitter current (I_E), while beta relates to base current (I_B) versus collector current.*

As with beta, which has a forward and a reverse component, so too with alpha. The equations given so far all imply a forward alpha and a forward beta. The *reverse alpha*

EX-1006 019
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

(α_r) is typically half the value of the forward alpha's value, so that with the value given in equation 4.9, the reverse alpha's value would be 0.495. This may be described by:

$$\alpha_R = \frac{\beta_R}{1 + \beta_R} \qquad \text{(Eq.4.10)}$$

If one needed to compute the reverse beta for a circuit, it is given as:

$$\beta_R = \frac{\alpha_R}{\left(1 - \alpha_R\right)} \qquad \text{(Eq.4.11)}$$

So that using the same values as above would yield:

$$\beta_R = \frac{0.495}{(1 - 0.495)} = \frac{0.495}{0.505} = 0.98 \qquad \text{(Eq.4.12)}$$

Reverse beta is often just considered as being 1.0 and calculated as such.

Another important set of considerations are the BJT's various breakdown voltage specifications. These characteristics include the all-important collector-emitter breakdown voltage $V_{(BR)CEO}$, the collector-base breakdown voltage $V_{(BR)CBO}$, the collector-emitter breakdown voltage $V_{(BR)CES}$, and others. Many of these characteristics are usually specified at the beginning of a transistor's data sheet in the "absolute maximum ratings" section. BJTs are manufactured according to a particular *process*, much of which dictates the breakdown voltage of the device. In normal operation the V_{CE} is much higher than the V_{BE}. However, from the data sheet it is clear that the $V_{(BR)CBO}$ is usually the highest-rated voltage characteristic. Actually, this collector-base voltage is responsible for much of a BJT's tiny leakage current (I_{CBO}), which like any P-N junction will increase with either increased voltage or temperature. It is important to use the transistor within a range of operating voltages up to approximately 65% of its maximum voltage rating. Using the device close to its maximum voltage rating can cause unforeseen problems, such as changes in gain as already mentioned, as well as self-heating of its junctions.

Figure 4.8 shows a test circuit for measuring some of the NPN transistor's voltage characteristics. For example, $V_{(BR)CEO}$ (shown in Figure 4.8 A) is measured at a specified collector current, with the BJT's base open. $V_{(BR)CBO}$ (shown in Figure 4.8B) will test the breakdown voltage of the collector-base junction. It is measured at a specified collector current, with the emitter terminal open-circuit. $V_{(BR)CES}$ (see Figure 4.8A) tests the breakdown voltage of the collector-emitter junction, with the base shorted to the emitter. $V_{(BR)CER}$ (see Figure 4.8A) tests the breakdown voltage of the collector-emitter junction, with the base connected to the emitter via a specified resistor.

EX-1006 020
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

$V_{(BR)CEX}$ (see Figure 4.8A) tests the breakdown voltage of the collector-emitter junction, measured with the base-emitter junction forward-biased at a particular voltage or current. $V_{(BR)EBO}$ (shown in Figure 4.8B) will test the breakdown voltage of the emitter-base junction, when measured at a specified emitter current (I_E), with the collector terminal open-circuit.

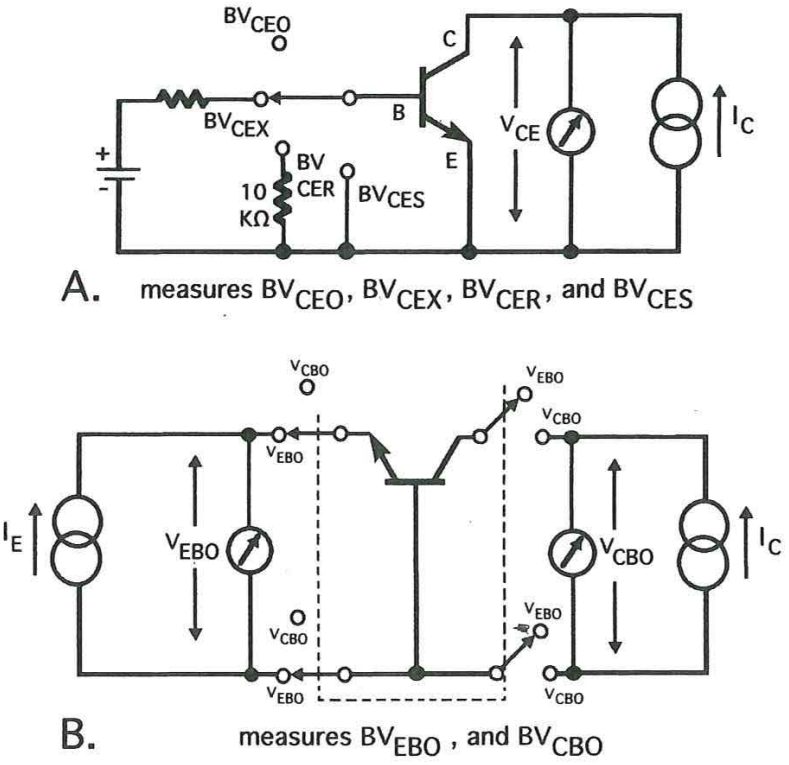


Figure 4.8. An NPN transistor's various $V_{(BR)CE}$ breakdown voltage test circuits.

Incidentally, the collector-base voltage V_{CBO} as well as the collector-emitter voltage V_{CEO} both have a small positive temperature coefficient of between +0.07 to +0.09%/°C.

No BJT is perfect: they all have some small degree of leakage currents, caused by minority carriers moving across the junctions. As mentioned previously, the collector-base junction is one of the main contributors to the BJT's leakage current. This particular current is known as the collector-to-base saturation current or the collector cutoff current (I_{CBO}), or as it is more commonly referred to, the I_{CO} leakage current. It is defined as the collector-base current with the junction reverse-biased and with the

EX-1006 021
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

emitter open-circuit. It is depicted in Figure 4.9 and is inherently related to the collector current, beta, and alpha by the following:

$$I_C = \frac{\alpha}{1-\alpha} I_B - \frac{I_{CBO}}{1-\alpha} \qquad \text{(Eq.4.13)}$$

$$I_C = \alpha I_E + I_{CBO} \qquad \text{(Eq.4.14)}$$

$$I_C = \alpha (I_C + I_B) + I_{CBO} \qquad \text{(Eq.4.15)}$$

$$I_C = \beta I_B + \frac{I_{CBO}}{1-\alpha} \qquad \text{(Eq.4.16)}$$

$$I_C = \beta I_B + (\beta + 1) I_{CBO} \qquad \text{(Eq.4.17)}$$

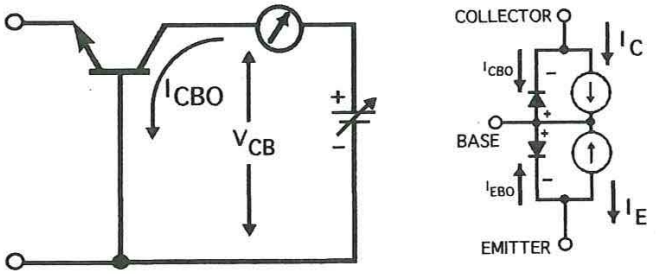


Figure 4.9. *I_{CO} -(I_{CBO}) the BJT's reverse collector-to-base leakage current.*

The I_{CO} leakage current comprises junction leakage currents, surface effects, recombination, and thermal effects. Just as with any P-N junction, leakage currents are caused by thermally generated electron-hole pairs (EHPs) and will increase exponentially with either increased voltage or temperature. I_{CO} has a temperature coefficient that doubles for each 11°C rise in temperature. For silicon devices, the I_{CO} leakage

EX-1006 022
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

current is usually extremely small, as shown here (where α_f and α_r are the forward and reverse alphas, and I_{CS} is the theoretical collector junction saturation current, given as 1.87×10^{-14}):

$$I_{CBO} = \left(1 - \alpha_f \alpha_r\right) I_{CS} \qquad \text{(Eq.4.18)}$$

$$= 9.536 \times 10^{-15} A$$

That's approximately 10 femto-amps! Manufacturers often specify the I_{CO} leakage current on their data sheets, and a typical maximum value at room temperature is 50 nA at a collector-to-base reverse voltage of 25 volts. This applies to either NPN or PNP devices. Figure 4.10 is an example of such, which shows a graph of the I_{CO} leakage current for the popular 2N5551 (TO-92) and the MMBT5551 (an SOT-23 surface-mount version). The 5551 is a high-voltage NPN general-purpose amplifier specified for operation at up to 160 volts. These devices are specified at room temperature, for a *maximum* I_{CO} value of 50 nA, at a collector-to-base reverse voltage of 120 volts. The graph shows an impressive 20 nA at 125°C.

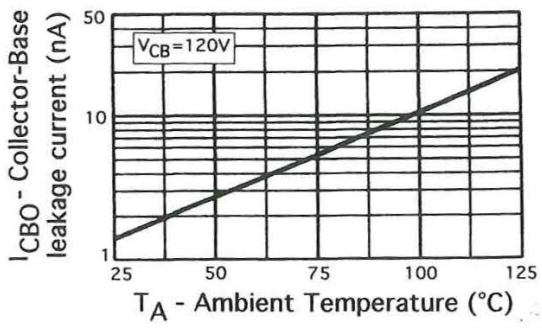


Figure 4.10. I_{CEO} reverse leakage current versus temperature for 2N5551/MMBT5551.

Another leakage current is the emitter-to-base leakage current (I_{EBO}), which is depicted in Figure 4.11. It is also referred to as the *emitter cutoff current* and is defined as the emitter-to-base current with the junction reverse-biased and with the collector open-circuit. I_{EBO} is often specified on a BJT's data sheet, at a typical maximum value at room temperature, of 100-nA leakage at an emitter-to-base reverse voltage of 5 volts for NPN devices. This is usually higher (1 μA) for PNP devices under similar bias conditions.

The largest leakage current for a BJT is the collector-emitter leakage current (I_{CEO}), which is the amplified leakage current of I_{CO}. This is because the I_{CO} leakage current (with the base open-circuit) will appear to the base terminal as though it were normal base current. As a result the transistor amplifies this base leakage current, which

EX-1006 023
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

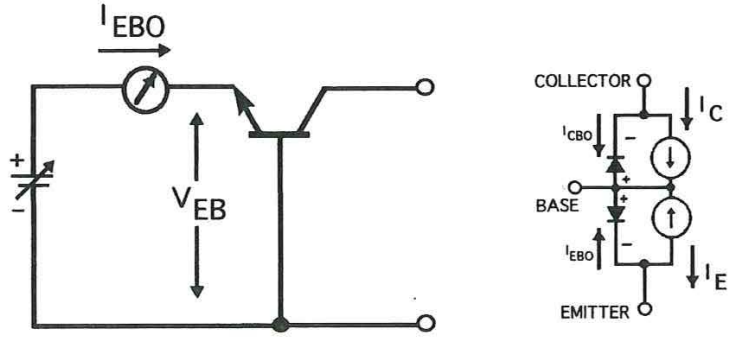


Figure 4.11. I_{EBO}*: the BJT's emitter-to-base reverse-biased leakage current.*

results in I_{CEO}. It is defined as the collector-emitter current with the junction reverse-biased and with the base open circuit. It is worth mentioning that this collector leakage current is also affected by changes in temperature, so that I_{CEO} increases in value four times for each 11˚C rise in temperature, and is also gain-dependent. I_{CEO} is depicted as one of the test circuits in Figure 4.12, and can be expressed by the following:

$$I_{CEO} = (\beta + 1)\, I_{CBO} \qquad \text{(Eq.4.19)}$$

also:

$$I_{CEO} = \frac{I_{CBO}}{1 + \alpha} \qquad \text{(Eq.4.20)}$$

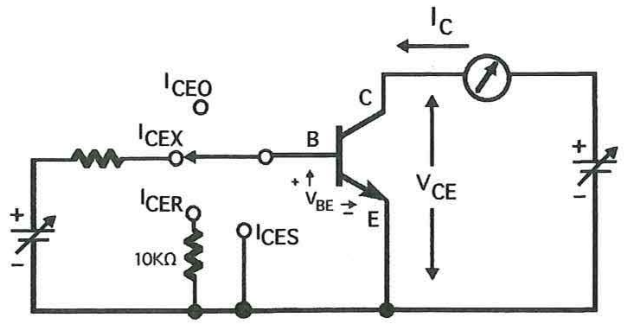


Figure 4.12. This circuit measures I_{CEO}*,* I_{CEX}*,* I_{CER}*, and* I_{CES}*.*

EX-1006 024
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Some other I_{CE} test circuits are also shown in Figure 4.12, which are sometimes referred to in device data sheets. These are the I_{CEX}, the collector-to-emitter leakage current specified at a particular voltage, or current bias at the base. Also I_{CES}, the collector-to-emitter leakage current specified at a particular collector-to-emitter voltage, with the base shorted to the emitter. Another is I_{CER}, the collector-to-emitter leakage current specified at a particular collector-to-emitter voltage, and with the base connected to the emitter via (typically) a 10-KΩ resistor. This leakage current increases in value three times for each 11°C rise in temperature.

To conclude our review of currents, remember that the transistor's largest current is the emitter current (I_E), which can be described by the following equations:

$$I_E = I_C + I_B \qquad \text{(Eq.4.21)}$$

$$I_E = (\beta + 1)\left(I_B + I_{CBO}\right) \qquad \text{(Eq.4.22)}$$

In addition, the collector current (I_C), which was previously described in equations 4.13 to 4.17, is the next largest current.

As mentioned previously, in order to function, the BJT relies on a small forward current and a small forward voltage at its base, where the base controls the current between the collector and emitter. This small base-to-emitter voltage is known as the base-to-emitter saturation voltage $V_{BE(sat)}$, and is required to correctly forward-bias (NPN) or reverse-bias (PNP) the junction. The transistor is composed of two junctions: the forward-biased base-emitter junction (similar in many respects to the diode, which we looked at in a previous chapter) and the reverse-biased collector-base junction. A transistor's DC performance often depends on its optimum bias point (Q-point, shown in Figure 4.4), within the circuit, and it must be correctly biased with respect to the supply voltages. This is the active state mentioned previously. To turn it on, the voltage applied at the base must be at or above the transistor's inherent V_{BE}, which for silicon is typically 0.65 volt. The theoretical relationship between this base-to-emitter voltage and the collector current (I_C) can be expressed by:

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right) \qquad \text{(Eq.4.23)}$$

where kT/q = 25.7 mV; I_C = the desired collector current; I_S = the theoretical reverse saturation current $\approx 1.87 \times 10^{-14}$ Amps. At a collector current of 1 mA, the resulting V_{BE} of a single transistor can be determined as follows:

EX-1006 025
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

$$V_{BE} = 0.0257 \text{ x } \ln 5.347 \text{ x } 10^{10}$$
$$= 0.635V \qquad \text{(Eq.4.24)}$$

Table 4.2 shows various collector currents and related V_{BE}s based on this relationship expressed in equation 4.23.

V_{BE} (V)	I_C
0.457	1-μA
0.516	10-μA
0.558	50-μA
0.576	100-μA
0.617	500-μA
0.634	1-mA
0.676	5-mA
0.694	10-mA
0.735	50-mA

Table 4.2 The Relationship between V_{BE} versus I_C

$V_{BE(sat)}$ is usually specified on a transistor's data sheet at a particular base current and collector current and can be measured as shown in Figure 4.15 (which is the same circuit for testing $V_{CE(sat)}$). For example, at 25°C the popular 2N3904 NPN general-purpose transistor has a $V_{BE(sat)}$ specification of 0.65 volt minimum to a maximum of 0.85 volt, at a base current of 1 mA and a collector current of 10 mA. With a 5-mA base current and a collector current of 10 mA, the maximum may be as high as 0.95 volt. The popular 2N3906 PNP general-purpose transistor has the same specifications, although other small-signal PNP devices will have different specs. This $V_{BE(sat)}$ voltage directly affects gain, because it determines the base current. Too low a base voltage will not permit enough base current to flow, which will in turn restrict the amount of collector current. Too high a base-emitter voltage can destroy the transistor, although most have an absolute maximum rating of several volts. This specification ranges from about 3 volts for some devices up to about 6 volts for others; the 2N3904 is rated for up to 6 volts, while the 2N3906 is rated for up to 5 volts. (Darlingtons have a higher absolute maximum rating often reaching 10 volts, but they are not really suitable as potential current sources.) Typically, a resistor is inserted in series with the base terminal, to limit the current and voltage to an appropriate level.

EX-1006 026
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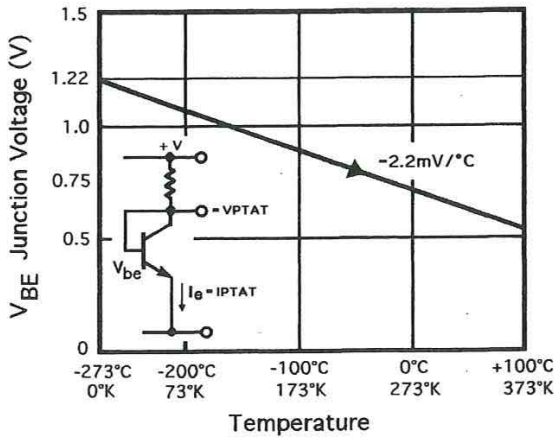


Figure 4.13. Showing the variation of base-emitter voltage (V_{BE}), with the emitter current proportional to absolute temperature ($I_E \alpha T$) in degrees Kelvin (°K).

When a silicon transistor's V_{BE} is correctly forward-biased, it can be used as a predictable voltage reference. Device physics suggests that BJTs have a V_{BE} yielding an approximate –2 mV/°C negative temperature coefficient. By extrapolating this temperature characteristic out to "absolute zero" (°K), with its emitter current considered proportional to absolute temperature (I_{PTAT}), it has been calculated that the V_{BE} will reach 1.205 volts at 0°K (–273°C). This V_{BE} can also be considered as proportional to absolute temperature (V_{PTAT}) and is shown in Figure 4.13. (It is one of the fundamental mechanisms by which the *bandgap cell* works and which results in a stable voltage reference. The typical bandgap voltage reference IC provides a compensating voltage, by purposely driving two transistors at different current densities and amplifying the resulting ΔV_{BE} difference, which has a positive TC. This is summed with the original negative TC V_{BE}, to provide a stable 1.205-volt reference voltage, but now with a zero TC. This is the basis for half of the monolithic voltage references on the market today. See Part 2 of this book for more on that topic.)

The V_{BE} voltage is usually specified as having a negative temperature coefficient of between –1.8% to –2.4mV/°C, depending on the process involved in the transistor's manufacture. As a rule of thumb, V_{BE} is usually calculated as having a tempco of –2.2 mV/°C. The two graphs in Figure 4.14 illustrate the general V_{BE} temperature sensitivity, using the 2N3904 and 2N3906 transistors as examples.

As current flows between the collector and emitter, a small voltage drop will occur between the collector and emitter. This is usually referred to as the collector-to-emitter saturation voltage or $V_{CE(sat)}$ and is measured in the common-emitter configuration at a particular collector current, and with a specified base current. This characteristic is shown on any BJT data sheet and usually specified at two different collector currents.

EX-1006 027
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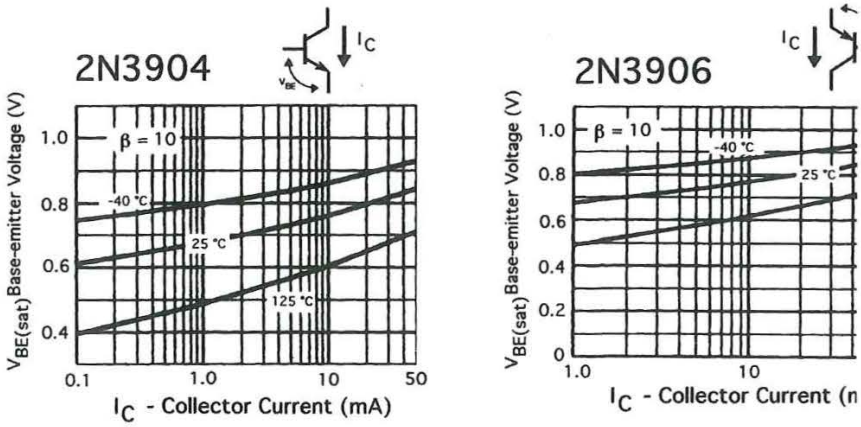


Figure 4.14. *$V_{BE(sat)}$: Base-emitter saturation voltage versus I_C: collector current for 2N3904 and 2N3906.*

It can be measured as shown in Figure 4.15. For most applications, a lower $V_{CE(sat)}$ is more desirable.

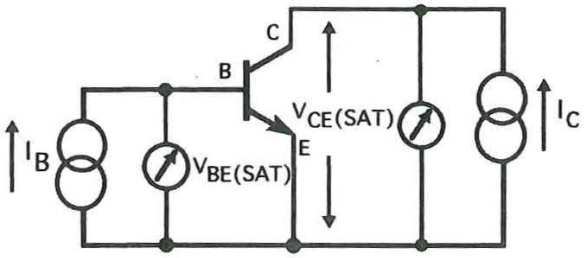


Figure 4.15. *An NPN transistor's $V_{CE(sat)}$ collector-to-emitter saturation voltage measurement circuit.*

$V_{CE(sat)}$ is a variable parameter that is difficult to control in processing and manufacturing. As a result, manufacturers normally provide only a maximum $V_{CE(sat)}$ specification. A particular process may yield a range of $V_{CE(sat)}$ values, where any one device's value may typically range from, say, 0.3 to 0.5 volt. Usually the manufacturer will test devices according to maximum $V_{CE(sat)}$ values and sort them into separate part numbers. Devices with lower values of $V_{CE(sat)}$ may cost more. Typically, small-signal general-purpose amplifiers and switches will have $V_{CE(sat)}$ values of between 0.2 and 0.35 volts. Because this collector-to-emitter voltage is temperature sensitive, it is usually specified (for small-signal transistors) as having a small positive temperature coeffi-

EX-1006 028
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

cient of between +0.22% to +0.4mV/°C. Higher-power devices have about half these values.

Another important characteristic of the BJT, which is uniquely related to V_{BE} and I_C, is its small-signal forward transconductance (aka g_m). G_m measures the effect of a change in collector current (I_C), for a specific change in V_{BE}, referenced to common-emitter mode. The input voltage and the output current are related by the transconductance, because the base voltage is *transferred* to the collector current and because g_m applies to *conductance*. In practical terms, transconductance is a measure of the BJT's ability to amplify and is a figure of merit. On a graph it appears as a steep or shallow slope and is usually measured in milli-Siemens (mS). G_m is usually measured as milliamps per volt (mA/V). G_m is seldom specified on data sheets, though, and should be either calculated or measured, thus:

$$I_C = g_m V_{BE} \qquad \text{(Eq.4.25)}$$

The transconductance value can be found by the following:

$$g_m = \frac{\Delta I_C}{\Delta V_{BE}} \qquad \text{(Eq.4.26)}$$

It can also be determined from:

$$g_m = \frac{1}{V_T} I_C \qquad \text{(Eq.4.27)}$$

where V_T is the BJT's thermal voltage (kT/q = 25.7 mV). It can also be expressed as:

$$g_m = \frac{I_C}{26} \qquad \text{(Eq.4.28)}$$

where I_C is calculated in milliamps.

These small voltages that occur in $V_{BE(sat)}$ and $V_{CE(sat)}$ can be viewed as internal bulk resistances within the transistor. Actually, as a rule of thumb, the small-signal BJT's base may be considered as having a resistance (R_B) of about 100 Ω; its collector (R_C) about 50 Ω; and its emitter (R_E) about 1 Ω. A reverse-biased junction such as the collector-base junction will typically have a resistance value of around 10 KΩ.

4.2 Using the BJT as a current source

The earliest current sources were built with vacuum tubes back in the 1940s and '50s. Then following the commercial introduction of the junction transistor, the earliest tran-

EX-1006 029
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

sistor-based current sources were germanium PNP types. As discussed in a previous chapter, because of germanium's unpredictability—particularly its instability with temperature—these current sources were not too practical. Eventually, when both NPN and PNP silicon transistors became available during the 1960s, analog designers could now build current sources that connected to either a positive or negative supply rail.

However, while better than their germanium counterparts in that they were more temperature stable, these current sources were neither accurate nor repeatable, because they were built using discrete transistors, diodes, and resistors (see Figure 4.16). When the silicon bipolar analog IC became a practical reality in the late 1960s, simple current sources began to be used in their architectures for purposes of biasing and stability. Their performances far outperformed their discrete predecessors, because all of the necessary components were integrated into the chip's design. As a result, much development focused on creating current sources for bipolar circuits between the mid-60s and the early '80s. At last, analog designers had found a reliable method of biasing their circuits and thereby improving the overall quality and accuracy of their products. As other technologies have since evolved, such as complimentary-bipolar (CB), analog CMOS, and gallium arsenide (GaAs) RF amplifiers, current sources were used in them also, with similarly good results.

After much research over two decades, the essential requirement found when using BJTs for creating precision current sources, sinks, and mirrors, was in using BJTs with tightly matched V_{BE}s, h_{FE}s, and used in a *monolithic* array. The most critical parameter is the ΔV_{BE}s, which can be viewed collectively like an op amp's offset voltage (V_{OS}), between a monolithic pair of transistors used as a current source (see Figure 4.17). To be clear, the ΔV_{BE} is the difference in voltage between the two V_{BE}s needed to equalize the two collector currents. If the transistors' V_{BE}s are the same and the collector voltages are the same, then the collector currents will also be the same. Actually, current source errors are exponentially proportional to the transistors' V_{BE}s, therefore it is *very important* that one begins with as closely matched devices as possible. Table 4.3 shows that even with a 1-mV ΔV_{BE} at a 100-μA collector current level, there will be a 3% current matching error.

Additionally, in a monolithic array, devices are inherently thermally matched (sharing the same package or substrate), otherwise the slightly different ground potentials, temperature differences/gradients, and overall long-term drift will quickly degrade a discrete circuit's performance. In fact, once a current source design has been built, one should measure its long-term TC V_{OS} stability (measured in μV/month). Ideally, one should aim for 1 μV/month or something close to that. Any accompanying resistors used should be tight tolerance (0.1% or better), low TC types (less than 50 ppm).

EX-1006 030
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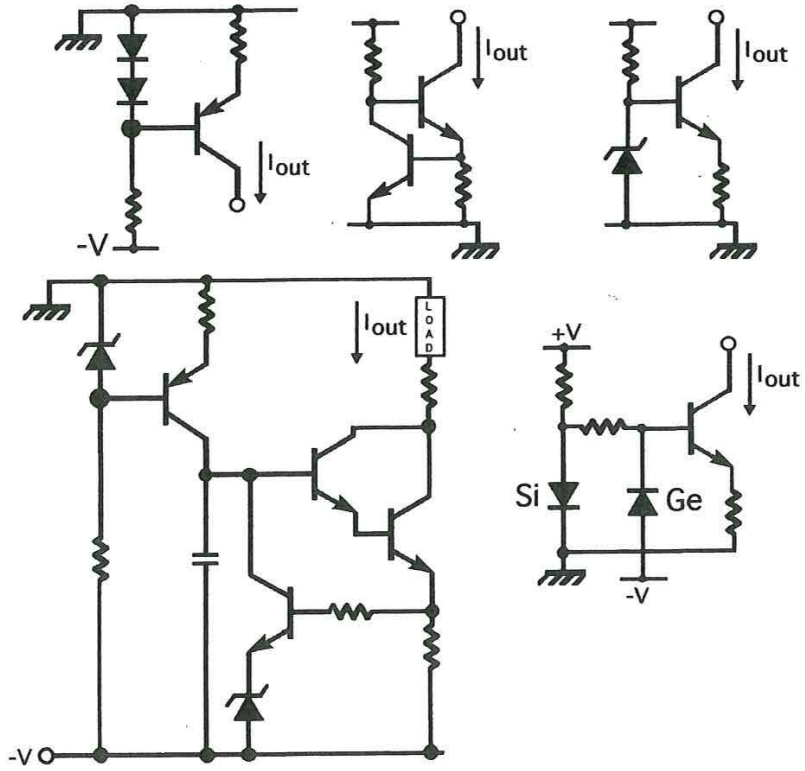


Figure 4.16. Early BJT current sources circa 1960s, and 1970s.

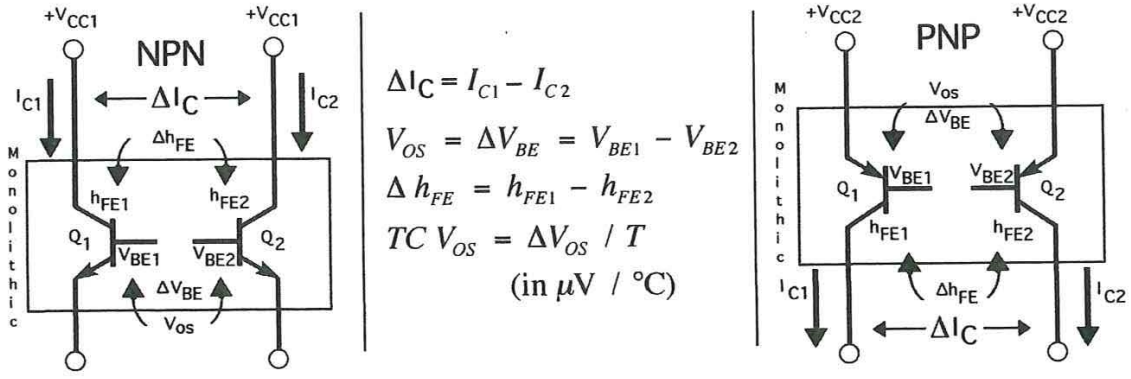


Figure 4.17. The importance of transistor matching.

EX-1006 031
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Ideally, they are also thermally matched, as in a monolithic resistor network (as made by Bourns, CTS, Caddock, Vishay, Philips Components Divn, Panasonic, and others).

ΔV_{BE}	% Current error/mismatch
1-mV	3%
2-mV	6%
3-mV	10%
4-mV	12%
5-mV	20%

Table 4.3 ΔV_{BE} vs. current errors percentage

Although using discrete transistors would appear to be more convenient and economical, this approach can be mostly discarded, other than at a feasibility or initial development phase, for lack of close matching, long-term accuracy and drift, as well as circuit repeatability. The increased performance, stability, and low drift of the monolithic dual or quad transistor array, versus using discrete transistors, far outweighs any added cost. This translates into making a reliable, successful product compared to making one that is troublesome and unsuccessful. The same holds true today and will tomorrow.

Another essential requirement for creating a precision current source, sink, or mirror is running it from a stable, low-noise voltage source. (This subject was discussed in Chapter 2, which suggested using a low-power, low-noise linear regulator such as a National Semiconductor LM2936 or similar.) For low current requirements (i.e., less than 5 mA), a precision low-noise voltage reference may even be used. In some applications, a small electrolytic capacitor (10 μF), in parallel with a 0.01-μF ceramic disc capacitor, may be required to bypass the regulated output to the current source supply. A hash-free regulated supply is essential in all precision work.

Unlike other semiconductors, the BJT does not lend itself very easily to being a two-lead current source. One can tie its base to the collector, which then forms a diode between the base and emitter, or one can invert the transistor into a type of clamp, but that's about all. Some other devices, such as the JFET, the current regulator diode (CRD), and the power MOSFET, can result in a two-lead current source configuration, but any worthwhile BJT current source requires an input terminal, an output terminal, and a voltage bias point. In some configurations, four terminals are needed. As a result, virtually all BJT current sources are configured as *current mirrors* (aka current reflectors), where an input current is mirrored at the output, in either a matched 1:1 or other ratio. This may be either a fraction or a multiple of the input, or scaled in some other manner. (We will look at multiple current mirrors—those with more than one output—as well as scaling later in the chapter.)

EX-1006 032
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

Although various BJT current source designs originally appeared, few of them were stable or else used an excessive number of components, as shown previously in Figure 4.16. The simplest two-transistor current sources of modern times are shown in Figure 4.18A and B, which can be built using a pair of either NPN or PNP devices. Technically speaking, the NPN circuit is a *mirror-sink*, while the PNP circuit is a *mirror-source*. This is because I_{C2} mirrors the current in I_{REF}, and the I_{C2} current is either flowing into the circuit (NPN) or out of it (PNP). In either case, the pair of transistors are assumed to have identical characteristics. The PNP version of this circuit works identically, but with all polarities and currents reversed. Of the two types, the PNP version is more commonly used.

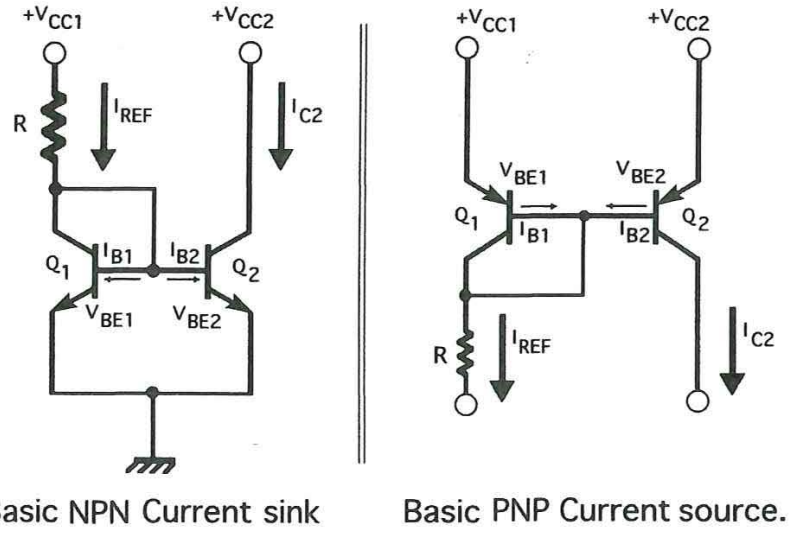


Figure 4.18. Basic BJT current mirrors.

In both current mirror circuits, Q_1's base and collector are shorted together, while the base and emitter act as a diode. The series resistor, R, provides a fixed voltage and current to Q_1's collector, as well as base current for Q_1 and Q_2. In the NPN circuit, because Q_1's collector and base are shorted, and its emitter is grounded, this clamps the V_{BE} at approximately 0.65 volt above ground. The PNP circuit has its V_{BE} at approximately 0.65 volt below VCC. Because both V_{BE}s are assumed here to be identical, so too will be their collector currents. If Q_1's V_{BE} is now impressed across transistor Q_2, then theoretically the reference current, I_{REF}, will be mirrored (duplicated) by Q_2.

Given:

$$I_{B1} = I_{B2};\ V_{BE1} = V_{BE2};\beta_{Q1} = \beta_{Q2} \qquad \text{(Eq.4.29)}$$

EX-1006 033
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

then to determine the reference current, I_{REF} in either NPN or PNP circuit:

$$I_{REF} = \left(\frac{V_{CC1} - V_{BE1}}{R} \right) \quad \text{(Eq.4.30)}$$

Also, because the reference current is composed of both Q_1's collector current and both base currents, then:

$$I_{REF} = I_{C1} + 2I_B \quad \text{(Eq.4.31)}$$

Therefore, the output current, I_{C2}, is determined by:

$$I_{OUT} = I_{C2} = \left(\frac{\beta}{\beta + 2} \right) \left(\frac{V_{CC1} - V_{BE1}}{R} \right) \quad \text{(Eq.4.32)}$$

$$\therefore I_{C1} \cong I_{C2} \quad \text{(Eq.4.33)}$$

The output resistance (r_o) for this particular configuration is given by the internal collector-to-emitter resistance (r_{ce}) of Q_2, derived from the BJT's small-signal model:

$$r_o = r_{ce2} \quad \text{(Eq.4.34)}$$

where r_{ce} is determined by:

$$r_{ce} = \frac{V_{CE}}{I_C} \quad \text{(Eq.4.35)}$$

As a working design example, the previous equations can be used to design two simple, practical 500-μA current sources in both NPN and PNP, with the following characteristics: Transistors: NMT-2222 (2N2222 type), a general-purpose NPN amplifier pair, in a SOT-6 surface-mount package. Also NMT-2907 (2N2907 type), a general-purpose PNP amplifier pair, in a SOT-6 surface-mount package. The +VCC equals 6 volts; V_{BE} equals 0.65 volt; and h_{FE} equals 50. Assuming that the base currents, gain, and base-to-emitter voltages are identical for both transistors, then:

EX-1006 034
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

$$V_{CC1} = V_{CC2} = 6V \qquad \text{(Eq.4.36)}$$
$$V_{BE1} = V_{BE2} = 0.65V$$
$$\beta_{Q1} = \beta_{Q2} = 50$$
$$I_{B1} = I_{B2} = 10\mu A$$
$$I_{OUT} = 500\mu A$$

The resulting circuits are shown in Figure 4.19.

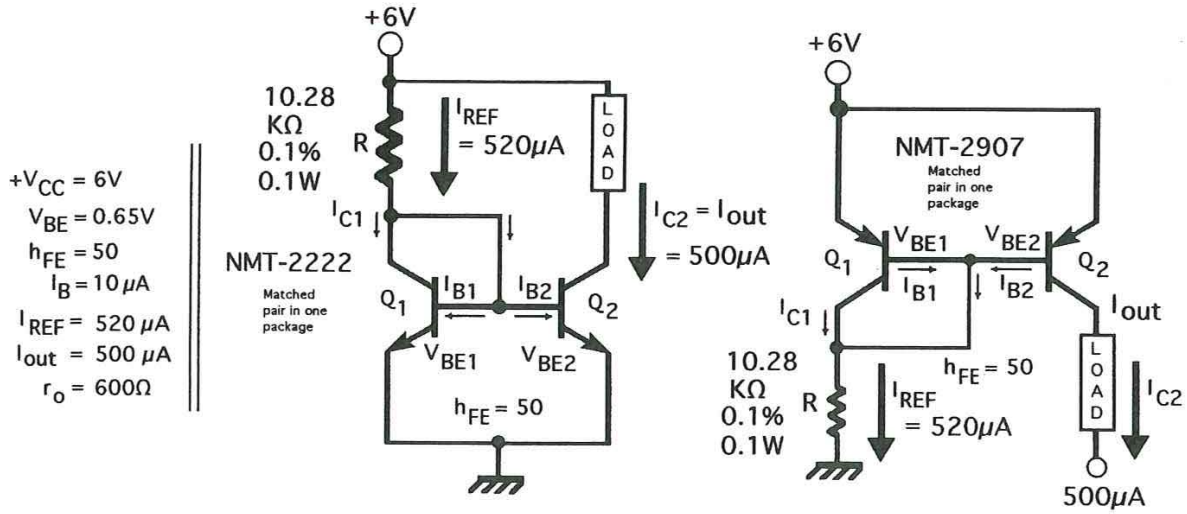


Figure 4.19. A simple 500 μA current source in both NPN and PNP designs.

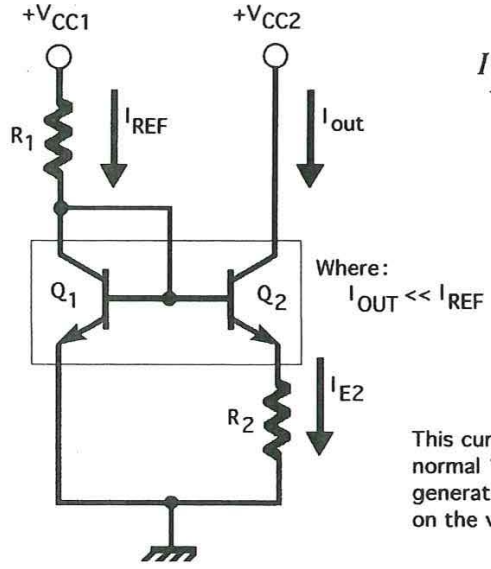
The circuit is a little deceptive, because at first glance one would deduce that I_{REF} is exactly equal to I_{OUT}, but this is a little misleading. One should remember that there is a difference between I_{REF} and I_{C1}. After all, I_{REF} is the *entire* reference current coming through the resistor (R), whereas I_{C1} is that part of the reference current flowing into Q_1's collector. The rest makes up the two base currents flowing into the bases of Q_1 and Q_2. This was defined previously in equation 4.36. As a result, the reference current should *not* be set at 500 μA, but slightly higher at 520 μA (to accommodate the two times I_B). This will result in an output current of 500 μA, as shown in Figure 4.19. Although this current source is one of the simplest (three components), not to mention quite popular, its regulation is soft and its output resistance is likewise poor at less than 1 KΩ. Others we will review shortly do a much better job in both regards. None-

EX-1006 035
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

theless, if you want a simple, three-component current source, this may be all you need for your application. Also, this current source is often used in conjunction with additional mirrors, which can either multiply or divide its output current (I_{C2}), or even invert it. We will look at this subject more, later in the chapter.

4.3 Widlar current sources

It is likely that the legendary Bob Widlar (who at 25 years old designed the first monolithic op amp—the μA702 at Fairchild Semiconductor in the mid-60s) ran into the same problem when creating the internal biasing for his op amps: he needed to design a better current source. In fact, Widlar designed several different BJT current sources, after all transistors were his pets, and he could make them do some amazing tricks. Widlar loved a challenge, and throughout his short but colorful career, he strove to create excellent products, so he created better current sources to fill his requirements.



$$I_{REF} = \frac{V_{cc1} - V_{be1}}{R_1}$$

$$I_{out} = \left(\frac{\frac{kT}{q}}{R_2}\right) \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

$$R_o = r_{ce2}\left(1 + g_{m2} R_2\right)$$

This current source is useful when the normal 1:1 output current ratio needs to generate smaller currents. It is dependent on the value of R_2 and the V_{BE} of Q_2.

Figure 4.20. Widlar's original current sink.

Figure 4.20 is a classic Widlar design; it retains the simplicity of the simple current source design we looked at previously, but provides greater output resistance and can accommodate smaller output currents (which are smaller than I_{REF}). At first glance, the only visible difference between this circuit and the one in Figure 4.19 is the addition of one more resistor, R_2. It is almost certainly a circuit he designed for his internal op amp biasing, because it works best for very small currents (10–500 μA). It may have caused him to look further into the subject of the silicon bandgap (V_{go}), and proportional currents and voltages (I_{PTAT} and V_{PTAT}), and their dependence on temperature. Alternatively, it may have been a by-product of this same subject. It is remarkable

EX-1006 036
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

to note that with the addition of two components, the circuit transforms from this basic current source into a simple bandgap voltage reference (see Figure 4.21). No doubt this entire subject caused Widlar and his process engineer, Dave Talbert, to look further into creating multiemitter transistor structures and ratioed emitters. Probably Widlar's greatest design (LM-109, the first 5-volt linear power regulator) was based on the bandgap cell, which he pioneered and which relied on ratioed emitters. The LM-109's control circuitry got its temperature compensation from the stable bandgap cell. Without it, the monolithic IC regulator would not have functioned properly at high currents and temperatures. Widlar was the first analog designer to do that.

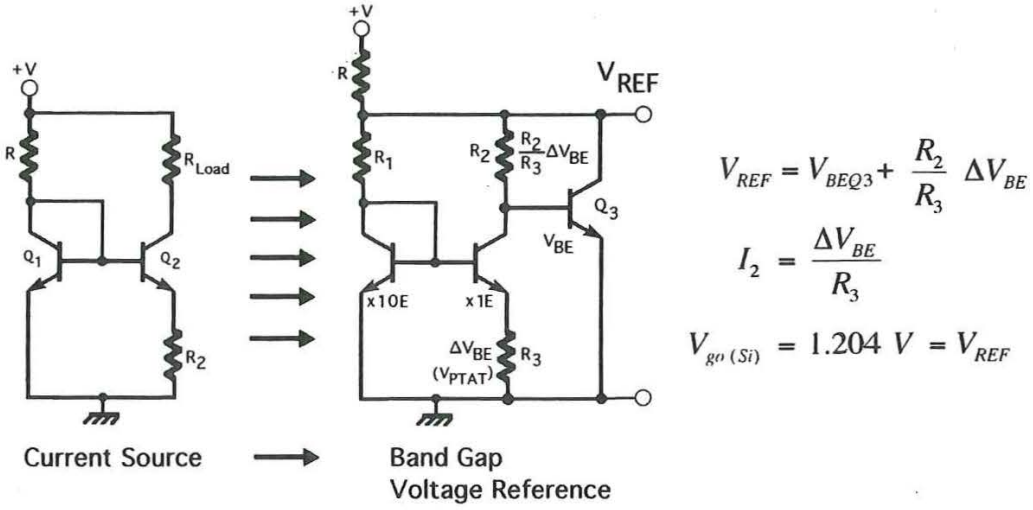


Figure 4.21. Widlar's Leap: Simple but ingenious, the transformation of his simple current-scaling current source into a simple bandgap voltage reference, by the addition of just two components. He did this in the mid-60s, as he created the world's first monolithic op amp, the Fairchild Semiconductor μA702. He was just 25 years old, and would become a legend.

(*Note*: For anyone wondering why I combined the subjects of current sources and voltage references into one book, Figure 4.21 should answer your question.)

Meanwhile, returning to Figure 4.20, by adding R_2 at Q_2's emitter (*emitter degeneration*), the output is no longer near-matched in a 1:1 current ratio, but is divided into a smaller current, which is also proportional to absolute temperature (I_{PTAT}). By changing R_2, you can produce a different output current ratio, such as 4:1, 10:1, and so on. In other words, it provides division of I_{REF}, where I_{C2} (the output current) is always smaller than I_{REF}. Whereas I_{REF} is calculated in the same manner as previously described (and in equation 4.30), both I_{OUT} and the output resistance (r_o) are determined differently, as shown in Figure 4.20. As a result, the output current depends on

EX-1006 037
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

both the value of R_2 and of transistor Q_2's V_{BE}. Actually, this technique helps compensate for mismatches in V_{BE}. Typically, the voltage value across R_2 should be made quite small (between 25 to 100 mV). The output resistance (r_o) for this circuit is significantly higher (between 10 KΩ to 100 KΩ) than in the simple current sources of Figs. 4.18 and 4.19, depending on the voltages and currents involved. Although the circuit works well, it is not the best BJT current source (it has its limitations), nor the easiest to work with, but remember it was part of an op amp's internal design and the particular needs of that circuit.

Widlar did a lot of work with current sources and produced several novel circuits and features for his op amp and regulator designs. Some of these were designed to compensate for the little-understood characteristics and limited capabilities of the early BJTs, not to mention applying them for the first time into the creation of monolithic analog integrated circuits—a totally uncharted area. Besides emitter degeneration, another technique he created or was first to utilize in his designs was *beta-compensation*. Even to this day, gain (h_{FE}, β) is a variable parameter that is difficult to control in manufacturing. Back in the 1960s, it was even worse, because the technology and processes were still in their infancy. As a result, manufacturers both then and now have only ever provided a *minimum* gain specification. Small-signal transistors, whether discretes or in a monolithic array, tend to have gains ranging from around 30 to several hundred, at low currents. So that when creating even simple current sources, as we have seen so far, where the initial calculations all assume that the characteristics are identical, in reality this is *not* the case. The technique Widlar devised for compensating for the beta mismatch in a pair of transistors (whether the beta value was high or low) was called *beta compensation*. The compensation was done by inserting a small resistance (typically between 22 to 100 Ω) in series with a BJT's base terminal. Because beta is also voltage-sensitive, this technique also helped compensate for changes in the input voltage. Figure 4.22 illustrates this concept more fully. Another compensation technique he developed (but more for his bandgap voltage references, rather than current sources) was the use of current scaling by emitter ratioing (emitter scaling) (Figure 4.22D). It was a key factor in making his bandgap cell work, which in turn led for the first time to real temperature compensation.

Later, as Widlar refined these techniques, he combined them into other designs, which took the form shown in Figure 4.23. The result was improved output regulation, less sensitivity to beta and V_{BE} mismatches, and increased output impedence.

A generic current source (inventor unknown), which also provides good regulation, is shown in Figure 4.24. Although this current source does not have the output resistance of the Widlar design and uses three transistors instead of two, it does provide reasonable accuracy and is easy to use. The design also reduces the effects of base currents and is often used in analog ICs.

In this circuit, Q_3's base and emitter form a diode in parallel with Q_1's collector and base. The series resistor, R, supplies a fixed voltage and current to Q_1's collector, as

EX-1006 038
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

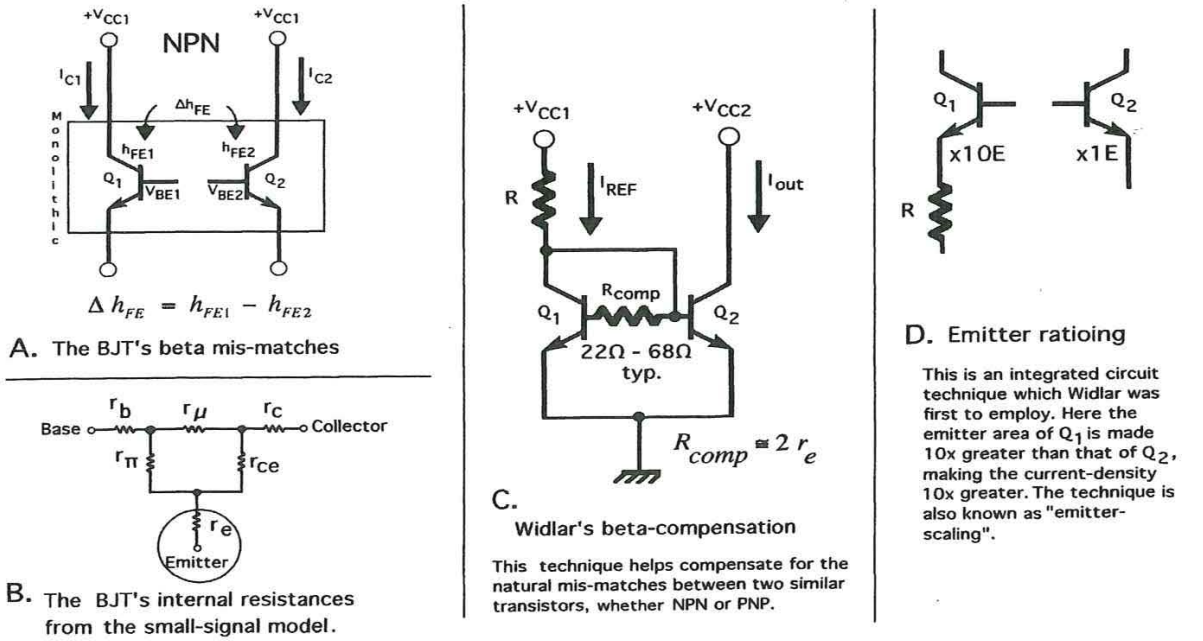


Figure 4.22. Some of Widlar's compensation techniques used in his current sources and band-gap voltage references.

well as base current to Q_3. Q_3's emitter and base (V_{BE}) clamps Q_1's collector at approximately 0.65 volt above its base. Q_3's emitter sits at approximately 0.65 volt above ground, because of the V_{BE} of both Q_1 and Q_2. Because both of their V_{BE}s are identical, so too will be their collector currents. As a result, the reference current, I_{REF}, will be duplicated by Q_2.

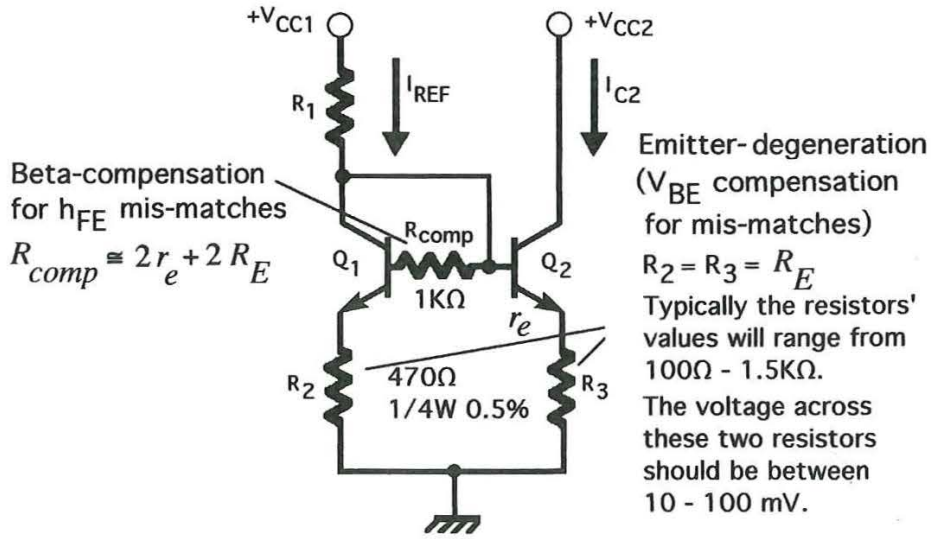
Given:

$$I_{B1} = I_{B2};\ V_{BE1} = V_{BE2};\ \beta_{Q1} = \beta_{Q2} \qquad \text{(Eq.4.37)}$$

The following determines the reference current, I_{REF}:

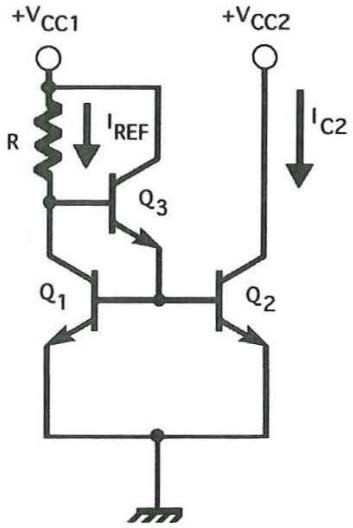
$$I_{REF} = \left(\frac{V_{CC1} - V_{BE3} - V_{BE1}}{R}\right) \qquad \text{(Eq.4.38)}$$

EX-1006 039
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.



$R_{comp} \cong 2r_e + 2R_E$

Figure 4.23. *Widlar's improved current sink. This configuration increases the output impedance (Z_{out}), as well as reducing the sensitivity of the transistor h_{FE} and V_{BE} mismatches.*



$$I_{REF} = \frac{V_{CC1} - V_{BE3} - V_{BE1}}{R}$$

$$I_{C2} = \frac{I_{REF}}{1 + \frac{2}{\beta^2 + \beta}}$$

$$R_o = r_{ce2}$$

Figure 4.24. *Basic three-transistor mirror-sink.*

EX-1006 040
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

Therefore, the output current, I_{C2}, is determined by:

$$I_{C1} \cong I_{C2} = I_{OUT} \quad \text{(Eq.4.39)}$$

$$I_{OUT} = \frac{I_{REF}}{\left[1 + \frac{2}{\left(\beta^2 + \beta\right)}\right]} \quad \text{(Eq.4.40)}$$

The output resistance (r_o) for this three-transistor current source is given by the internal collector-to-emitter resistance (r_{ce}), derived from the BJT's small-signal model:

$$r_o = r_{ce2} \quad \text{(Eq.4.41)}$$

where again r_{ce} is determined by:

$$r_{ce} = \frac{V_{CE}}{I_C} \quad \text{(Eq.4.42)}$$

As another working design example, the previous equations can be used to design a simple, practical NPN 250-μA current sink with the following characteristics: Transistors = MMPQ3904 (2N3904 type), a general-purpose NPN quad amplifier, in a SOIC-16 surface-mount package. The +VCC equals 9 volts; V_{BE} equals 0.65 volt; and h_{FE} equals 50. Also assuming that the base currents, gain, and base-to-emitter voltages are identical for all four transistors (we will only use three of them), then:

$$I_{REF} = \frac{(9 - 0.65 - 0.65)}{30.8K\Omega} = 250\mu A \quad \text{(Eq.4.43)}$$

The output current is:

$$I_{OUT} = \frac{250\mu A}{\left[1 + \frac{2}{\left(50^2 + 50\right)}\right]} = \frac{250\mu A}{1.000784} = 249.8\mu A \quad \text{(Eq.4.44)}$$

$$I_{C1} = I_{C2} = I_{OUT} = 250\mu A \quad \text{(Eq.4.45)}$$

EX-1006 041
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

If the transistor's beta changes by ±20% because of temperature changes, then we can calculate the difference as follows:

1) *With* $\beta = 40$ (-20%):

$$I_{OUT} = \frac{250\mu A}{\left[1 + \frac{2}{\left(40^2 + 40\right)}\right]} = \frac{250\mu A}{1.0012195} = 249.69\mu A$$

$$\therefore I_{OUT} = 249.69\mu A \qquad \text{(Eq.4.46)}$$

2) *With* $\beta = 60$ (+20%):

$$I_{OUT} = \frac{250\mu A}{\left[1 + \frac{2}{\left(60^2 + 60\right)}\right]} = \frac{250\mu A}{1.000546} = 249.86\mu A$$

$$\therefore I_{OUT} = 249.86\mu A \qquad \text{(Eq.4.47)}$$

The maximum difference is 0.31 microamps (or less than 0.2%), which is acceptable.

It is common to portray a circuit's characteristics by using the temperature coefficient (TC) as either a percentage or in parts per million. This is referred to as the circuit's *tempco*. For a current source, the tempco of the output current ($\alpha\ I_{O(TC)}$) is the ratio of change in output current, to the change in temperature (say, from 20°C to 85°C). This is usually expressed as a *percentage* of the output current (e.g., 0.025%) and is the average value for the total temperature change. You can determine the tempco from your data by the formula in equation 4.48:

$$\alpha I_{O\,(TC)} = \pm \left(\frac{I_o\ @\ T_2 - I_o\ @\ T_1}{I_o\ @\ 25°C} \right) \left(\frac{100\%}{T_2 - T_1} \right) \qquad \text{Eq.4.48}$$

For example, we needed to check a current source design over a temperature range of 0°C to +85°C. After taking some current measurements in a controlled environment, we obtained the following results:

EX-1006 042
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

I_{out} at 25°C = 252 μA

I_{out} at 0°C = 248 μA

I_{out} at 85°C = 267 μA

Using the equation 4.48 would yield:

$$T_C = \left(\frac{267\mu A - 248\mu A}{252\mu A}\right)\left(\frac{100}{85}\right) = 0.089\% \qquad \text{Eq.4.49}$$

We can also express the tempco as a value in *parts per million per degree Celsius* (ppm/°C), by using the formula in equation 4.47:

$$T_C = \left(\frac{I_o\ @\ T_2 - I_o\ @\ T_1}{I_o\ @\ 25°C}\right)\left(\frac{1 \times 10^6}{T_2 - T_1}\right) \qquad \text{Eq.4.50}$$

In this example, the output current's tempco could also be expressed as 887 ppm/°C—only a mediocre current source design over the temperature range. This would suggest that some more work may be needed to bring its tempco down to a few hundred ppm or lower.

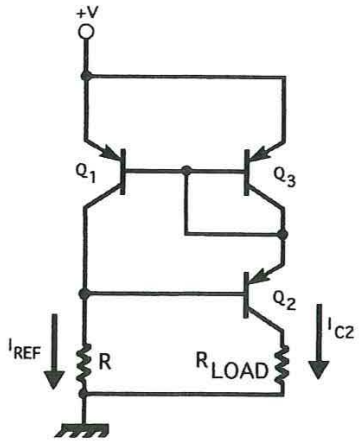
In summary, the lower the tempco, the less the current source will drift over the intended temperature range, and the more stable and reliable your circuit will be.

4.4 Wilson current mirrors

Of all BJT current sources, the most popular and widely used are the Wilson family, named after its inventor. The Wilson family can be configured as either a three- or a four-transistor cell, in either NPN or PNP versions. The three-transistor cells are referred to as *Basic Wilson* current mirrors, and the four-transistor versions are referred to as *Full Wilson* current mirrors. These current sources are configured as either mirror-sinks (NPNs) or mirror-sources (PNPs). They are all fast and have exceptionally low sensitivity to transistor gain mismatches. In addition, they provide high output resistance. We will look at the four types here, together with some practical examples.

The three-transistor current mirror cells are the NPN or PNP Basic Wilson circuits. Both versions are shown in Figure 4.25, along with the relevant equations. Technically speaking, the NPN circuit is a mirror-sink, while the PNP circuit is a mirror-source. The PNP version of this circuit (shown in Figure 4.25A) works identically, but with all polarities and currents reversed. Of the two types, the PNP version is more commonly used.

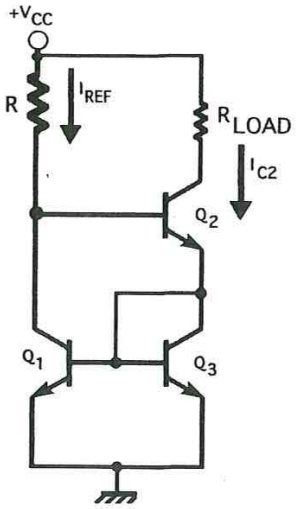
EX-1006 043
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.



$$I_{REF} = \frac{V_{CC1} - V_{BE2} - V_{BE3}}{R}$$

$$I_{C2} = I_{REF}\left(1 - \frac{2}{\left(\beta^2 + 2\beta + 2\right)}\right)$$

$$R_o = \frac{\beta r_{ce2}}{2}$$



A.
The basic Wilson PNP current mirror.

B.
The basic Wilson NPN current mirror.

Figure 4.25. Basic Wilson current mirrors.

As shown in the diagram, a reference current (I_{REF}) flowing through R splits between Q_1 and a small current flowing through the base of Q_2. This causes Q_2 to supply current to Q_3, while a small base current now also flows through Q_1. Transistors Q_1 and Q_3 function as a current mirror, with Q_1 supplying just enough current to keep Q_2 on, with negative feedback from Q1 and Q_3 regulating Q_2's current. This action cancels the base current drawn and makes Q_2's current relatively independent of gain (meaning that it is beta-compensated, but differently from Widlar's). As a result of the negative feedback, the output resistance (r_o) is higher, and the regulation is much sharper than any of the BJT current sources we have looked at so far. Although Q_2 is not critical, both Q_1 and Q_3 should be matched for gain and V_{BE}. Ideally, one should use a quad array device for best thermal and electrical matching, which will provide the best performance and repeatability. (A dual and a discrete will work okay, but not as well.)

Because both Q_1 and Q_3's V_{BE}s are assumed here to be identical, so too will be their collector currents. When Q_1's V_{BE} is impressed across transistor Q_3, then the reference current, I_{REF}, will be mirrored by Q_2 and Q_3. Given:

$$I_{B1} = I_{B3};\ V_{BE1} = V_{BE3};\beta_{Q1} = \beta_{Q3} \qquad \text{(Eq.4.51)}$$

EX-1006 044
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

To determine the reference current, I_{REF}, in either NPN or PNP circuit:

$$I_{REF} = \left(\frac{V_{CC} - V_{BE2} - V_{BE3}}{R} \right) \quad \text{(Eq.4.52)}$$

The output current, I_{C2}, is determined by:

$$I_{OUT} = I_{REF} \left(1 - \left(\frac{2}{\beta^2 + 2\beta + 2} \right) \right) \quad \text{(Eq.4.53)}$$

$$\therefore I_{C1} \cong I_{C2} \quad \text{(Eq.4.54)}$$

The output resistance (r_o) for this configuration is given by the internal collector-to-emitter resistance (r_{ce}) of Q_2 (derived from the BJT's small-signal model), times the beta, then divided by two, thus:

$$r_o = \frac{\beta r_{ce2}}{2} \quad \text{(Eq.4.55)}$$

where r_{ce} is determined by:

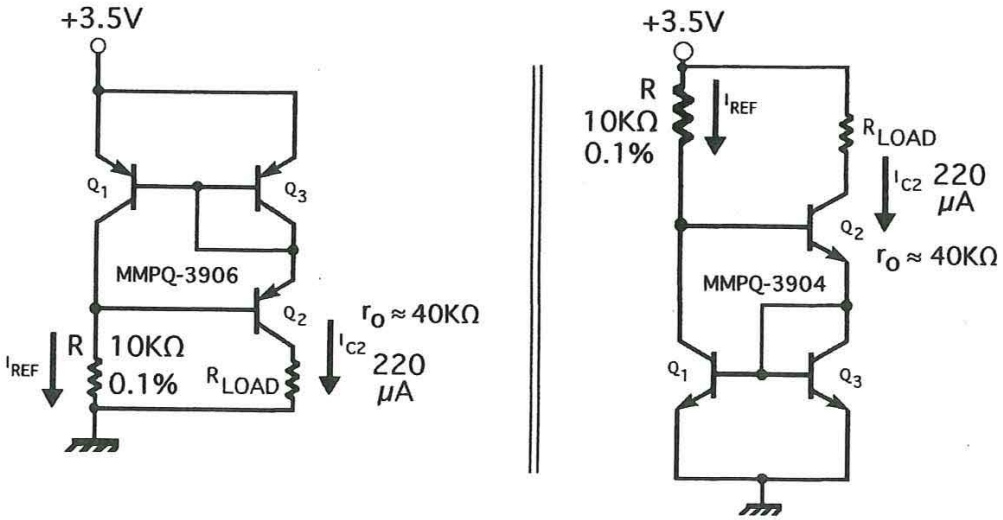
$$r_{ce} = \frac{V_{CE}}{I_C} \quad \text{(Eq.4.56)}$$

As a working design example, the previous equations can be used to design two simple, practical 220-μA current sources in both NPN and PNP versions, with the following characteristics: Transistors: MMPQ-3904 (2N3904 type), a general-purpose NPN amplifier quad, in a SOIC-16 surface-mount package. Also MMPQ-3906 (2N3906 type), a general-purpose PNP amplifier quad, also in a SOIC-16 surface-mount package. The +VCC supply equals 3.5 volts; V_{BE} equals 0.65 volt; and h_{FE} equals 50.

EX-1006 045
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

Assuming that the gain (h_{FE}), base currents (I_B), and V_{BE}s are identical for these transistors as given in equation 4.51, then:

$$V_{CC1} = 3.5V \qquad \text{(Eq.4.57)}$$
$$V_{BE1} = V_{BE3} = 0.65V$$
$$\beta_{Q1} = \beta_{Q3} = 50$$
$$I_{B1} = I_{B3} = 10\mu A$$
$$I_{OUT} = 220\mu A$$



A. PNP current mirror.

B. NPN current mirror.

Figure 4.26. Examples of low-voltage basic Wilson current mirrors.

Let's begin by determining the resistor setting value (R), so that:

$$R = \frac{3.5V - 0.65V - 0.65V}{220\mu A} = 10K\Omega \qquad \text{(Eq.4.58)}$$

EX-1006 046
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

The output current ($I_{C2} = I_{OUT}$) is given by:

$$I_{OUT} = 220\mu A\left(1 - \left(\frac{2}{50^2 + 2 \bullet 50 + 2}\right)\right) = 219.83\mu A \qquad \text{(Eq.4.59)}$$

The minimum output resistance (r_o) is approximately:

$$r_o = \frac{80000}{2} = 40K\Omega \qquad \text{(Eq.4.60)}$$

The resulting two circuits are shown in Figure 4.26. Although these current sources are the basic type of Wilson, they are very popular, with good regulation and output resistance. The Full Wilsons and cascodes, which we will review shortly, do an even better job. Nonetheless, if you want a simple, reliable four-component current sink or source, one of these may be all you need in your application. The best part is that they are both beta-compensated, and to illustrate this we can show that if the gain (h_{FE}) that we previously calculated at a nominal 50 changes by ±50%, the output current is still regulating really well. For a 50% reduction in gain, this would mean that the gain is now 25, thus:

$$I_{OUT} = 220\mu A\left(1 - \left(\frac{2}{25^2 + 2 \bullet 25 + 2}\right)\right) = 219.35\mu A \qquad \text{(Eq.4.61)}$$

For a 50% increase in gain, this would mean that the gain is now 75, thus:

$$I_{OUT} = 220\mu A\left(1 - \left(\frac{2}{75^2 + 2 \bullet 75 + 2}\right)\right) = 219.92\mu A \qquad \text{(Eq.4.62}$$

When you consider that the nominal output current with a gain of 50 is 219.83 μA (as shown in equation 4.59), this equates to a change in output of –0.22% for the 50% reduction in gain or a +0.041% for a 50% increase in gain. Even if the gain is increased to a phenomenal 150 (an increase of three times), the output is still at 219.98 μA, or an increase of only +0.068%. Even if the gain drops to 15, the change in output is still only –0.7%. That kind of regulation is impressive by any standard and a good example of beta-compensation (thanks to Mr. Widlar and Mr. Wilson). By the way, these circuits will probably work well down to about 2 volts or above 30 volts (but you don't want to get too close to any V_{BR} ratings or start to heat up the transistor junctions). These current sources are sometimes used in conjunction with additional mirrors, which can either multiply or divide their output current.

For much increased output resistance and equally good regulation, the Full Wilson current mirror is highly recommended. These circuits are based on a four-transistor

EX-1006 047
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

cell, as shown in Figure 4.27, along with the relevant equations. Again, the NPN circuit functions as a mirror-sink, while the PNP circuit is a mirror-source. Of the two types, the PNP version is more commonly used, because it is used primarily for precision biasing and as a high-impedance active load. Adding emitter degeneration (equal emitter resistors, with values typically of between 100 Ω and 1.5 KΩ), as shown in Figure 4.27, compensates for any slight mismatches in the transistors' V_{BE}s. This helps improve overall accuracy and fully optimizes the current source for best overall performance.

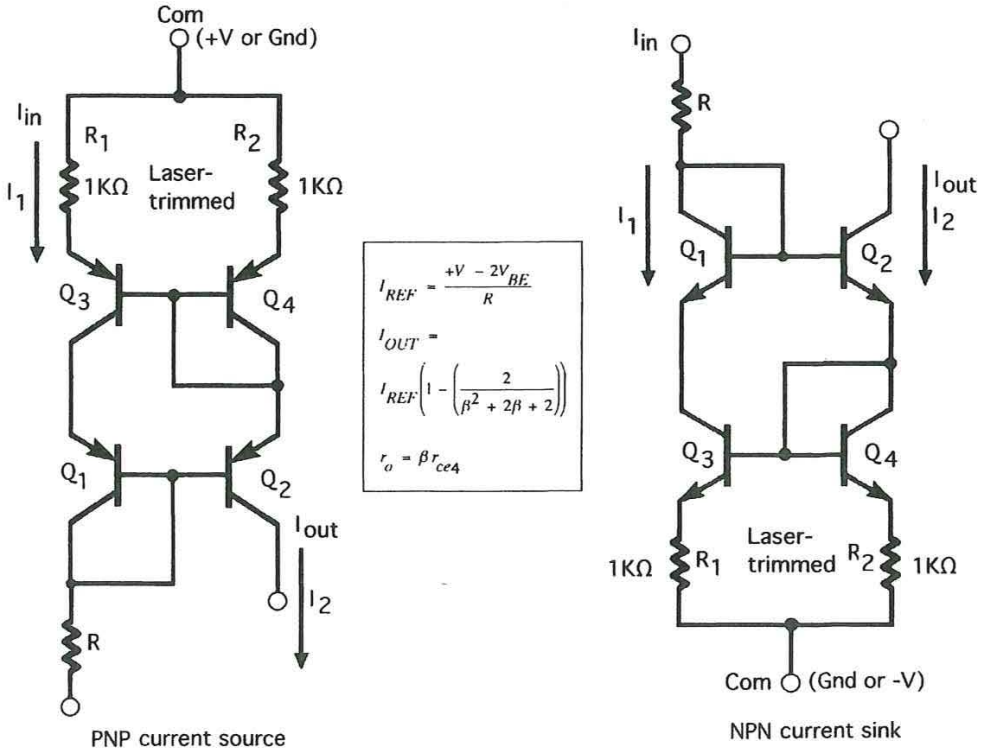


Figure 4.27. The best current mirror built with the BJT is the Full Wilson with emitter-degeneration. It provides high accuracy, excellent regulation, and very high output impedance. Building the circuit with a quad matched array improves the circuit's temperature coefficient.

While the calculations and equations are virtually the same as with the three-transistor cell, the noticeable difference is the equation for the output resistance, shown here:

$$r_o = \beta r_{ceQ4} \qquad \text{(Eq.4.63)}$$

EX-1006 048
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

where again r_{ce} is determined by:

$$r_{ce} = \frac{V_{CE}}{I_C} \qquad \text{(Eq.4.64)}$$

Here the output resistance is "beta times" the collector-emitter resitance of the transistor Q_4 (in both circuits), which can provide a value from hundreds of KΩ to tens of MΩ, depending on the voltage, current output, beta, and r_{ce} values. It's worth noting that the Texas Instruments/Burr-Brown REF-200 contains a Full Wilson current mirror and two current sources in a choice of either an eight-pin DIP or an eight-pin SOIC surface-mount package. That current mirror is specified as having a minimum output impedance of 20 MΩ, and the emitter degeneration resistors are laser-trimmed for optimum accuracy. It would be hard to match those specs, building your own.

In summary, the Wilson current mirrors are probably the first choice in building any current mirrors with the BJT. They offer higher accuracy (better than 0.01%), as well as a high output impedance, and building them in a monolithic rather than discrete form will render improved temperature tracking and a low tempco.

4.5 Wyatt current source

It's perhaps a coincidence that the three American engineers who have developed far-reaching and incredibly useful current sources all have their surnames start with a W, but it's true. So far we have met two of them, Mr. Widlar and Mr. Wilson. Now we come to the third member of the trio, Michael Wyatt. The *Cascode Peaking Current Source*, depicted here in Figure 4.28, was developed at Honeywell's Space Systems Division (Clearwater, Florida) by Michael Wyatt during development of a proprietary monolithic RF IC project in the late 1990s. Dr. Wyatt is a Senior Engineering Fellow at Honeywell, where he designs ICs. He holds numerous patents and previously won the much-coveted and prestigious *EDN* magazine's annual Best Design Idea award.

This circuit is a high-speed, accurate, cascoded current source, and has a rather unique design, as you can see. Vaguely reminiscent of Widlar's design, this too provides an output that is a fraction of the input current. Unlike other current sources, this one has a flat regulated current output, regardless of the circuit's input voltage level. In this design, two peaking current sources are welded together—an NPN sink together with a PNP source—to form a cascode. It acheives a low temperature coefficient, by virtue of using aluminum resistors (3333 ppm/°C), which first-order compensate the circuit. Other types of resistors may be used, which include solid carbon, copper, gold, or silver, all of which have similar tempcos.

EX-1006 049
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

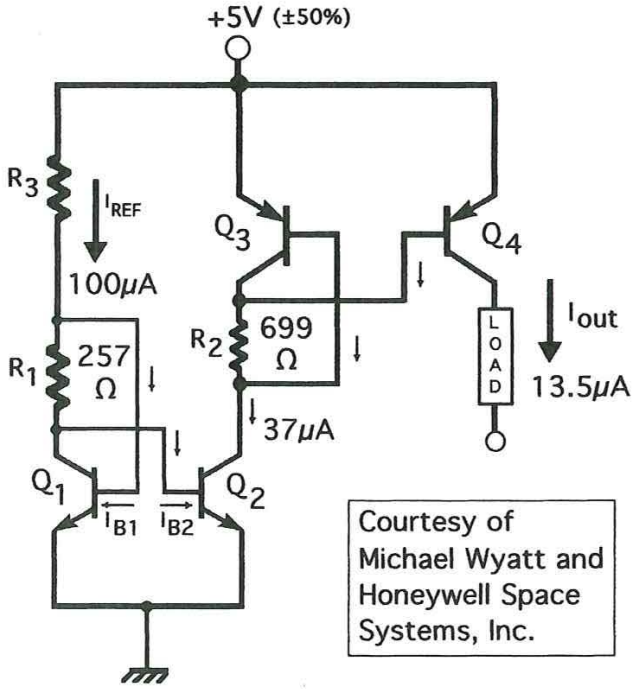


Figure 4.28. The Wyatt Cascode Peaking Current Source. This design reduces the input current to a lower level, and combines high accuracy with a constant output, and temperature compensation.

In this design, the following equations apply:

$$R_1 = \frac{V_T}{I_{IN}} \qquad \text{(Eq.4.65)}$$

$$I_{IN} = \frac{V_T}{R_1} \qquad \text{(Eq.4.66)}$$

where V_T is 25.7 mV, the transistor's theoretical thermal voltage. Resistor R_2 can be calculated by:

$$R_2 = e^1 \text{ x } R_1 \qquad \text{(Eq.4.67)}$$

EX-1006 050
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

and the output current can be approximated within 1% or 2% by:

$$I_{OUT} = I_{IN} \times e^{-2} \qquad \text{(Eq.4.68)}$$

As an example, we will create a 13.5-μA current source using a supply voltage of 5 volts DC and an input current of 100 μA. The NPN pair, which forms the first stage, reduces the 100 μA down to 37 μA at the collector of Q_2. This current is the input for Q_3 of the PNP pair, which again reduces the current down, so that Q_4's collector outputs a constant current of 13.5 μA. We can show this by the following:

$$R_1 = \frac{25.7mV}{100\mu A} = 257\Omega \qquad \text{(Eq.4.69)}$$

$$I_{IN} = \frac{25.7mV}{257\Omega} = 100\mu A \qquad \text{(Eq.4.70)}$$

$$R_2 = e^1 \text{ x } 257\Omega = 698.6\Omega \qquad \text{(Eq.4.71)}$$

and the output will be:

$$I_{OUT} = 100\mu\text{A} \times e^{-2} = 0.0001 \text{ x } 0.13533 = 13.53\mu A \qquad \text{(Eq.4.72)}$$

The output is perfectly flat with an input voltage range of between 2 and 10 volts, and with an input current range of 50 μA and 200 μA, over a temperature range of 0°C to 100°C—certainly an impressive design. The Wyatt current source can be optimized by building it using a monolithic complimentary quad device, along with those aluminum resistors. If an uncompensated (tempco) version is acceptable, then regular low-tempco, low-tolerance, metal-film resistors can be used instead. The Wyatt current source is the least known of the Widlar-Wilson-Wyatt trio, but it provides even sharper current regulation than other (non-1:1) types, not unlike the performance of a JFET cascode (see Chapter 6 for more on that).

4.6 Multiple current mirrors

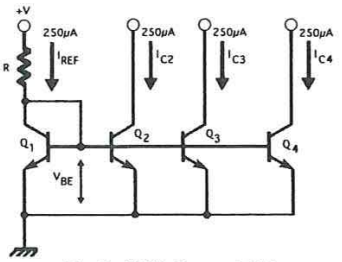
There are many occasions when one needs to build a current mirror with more than one output, as we have looked at up until now. Applications commonly include multi-stage amplifier biasing and high-impedance active loads. For simplicity's sake we will refer to these as multiple current mirrors. In the basic NPN current mirror shown in Fig-

EX-1006 051
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

ure 4.29, Q_1 is connected as a diode to ground and supplied with a fixed collector voltage and current via resistor R. Because Q_1's collector and base are shorted, and the emitter is grounded, the base is clamped via the V_{BE} at approximately 0.65 volt above ground. If Q_1's V_{BE} is now impressed across the parallel transistors Q_2, Q_3, and Q_4 (assumed to have identical V_{BE}s), then in theory the initial current I_{REF} is mirrored by the others, thus:

$$I_{REF} = I_2 = I_3 = I_4 \qquad \text{(Eq.4.73)}$$

That's the theory, but in practice as these additional transistors are added, an error term is introduced, which is caused by gain-dependent base-currents in Q_2, Q_3, and Q_4, which reduces I_{REF} by as much as 5%. This current error now adds to any errors caused by V_{BE} mismatches. Unfortunately, Widlar's technique of adding a small resistor in the base of the reference transistor for beta-compensation does not work well with these multiple mirrors. The relevant equations are included in the diagram. (The term *n* refers to the number of mirror channels. The diagram shows three, so here $n = 3$.)



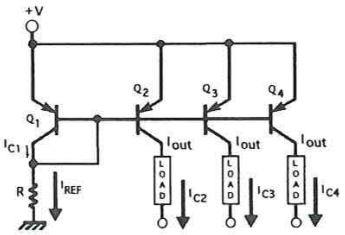
Basic NPN Current Mirror

$$I_{REF} = \frac{V_{CC} - V_{BE}}{R}$$

$$I_{out} = \frac{\beta \bullet I_{C2}}{\beta + n + 1}$$

$$I_{REF} = I_2 = I_3 = I_4$$

$$r_o = r_{ce}$$



Basic PNP Current Mirror

Figure 4.29. Examples of multiple current mirrors.

Linear IC manufacturers frequently refine their designs in order to improve specs, boost yields, and match new processes. Despite this long experience with bipolar designs over the course of more than four decades, manufacturing BJTs of any type or in any process with exactly matched h_{FE}s and V_{BE}s is still all but impossible. Only *precision matched-pairs* come closest to this ideal. (While various companies make duals/quad devices, they are not true matched-pairs. In the United States, only National Semiconductor and Analog Devices make such products.) Long ago, however, Bob Widlar found that by incorporating small-value resistors (typically in the range of 100 Ω to 1.5 KΩ), in the emitters of the transistors reduces the sensitivity of the output currents to these small V_{BE} mismatches—a technique referred to as *emitter degeneration*. So, to reduce the V_{BE} errors in the multiple current mirror, adding small-value emitter resistors is recommended, as shown in Figure 4.30. It will definitely help.

EX-1006 052
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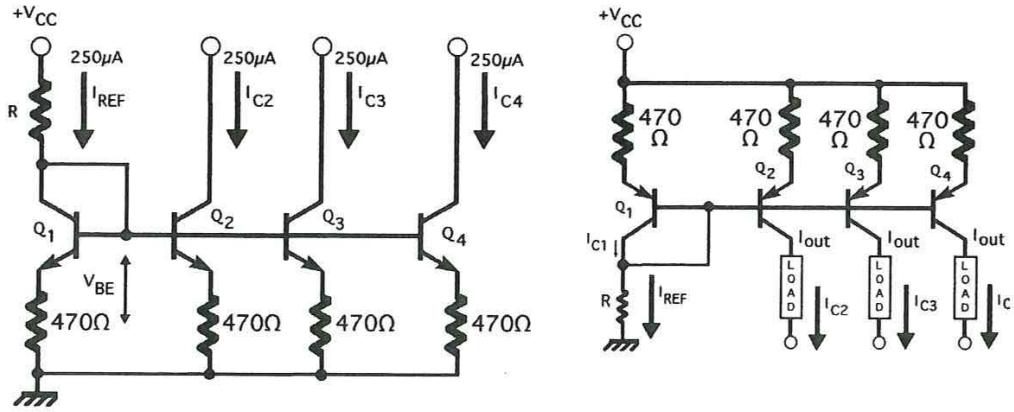


Figure 4.30. Emitter degeneration helps compensate for small V_{BE} mismatches.

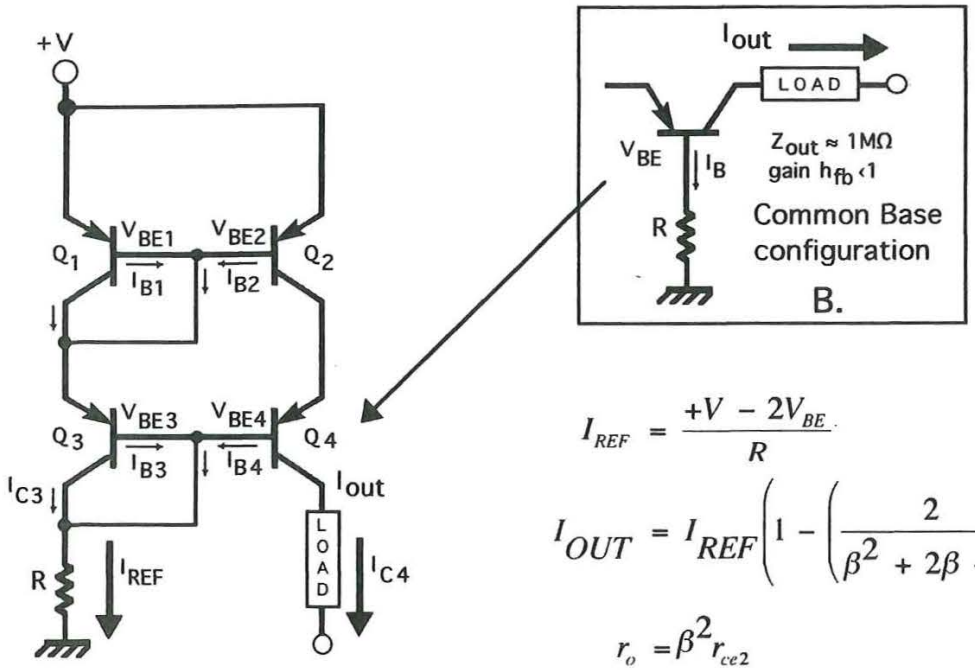
For more than two decades, manufacturers have used laser-trimming techniques (most notably for adjusting op amp offset voltages) to precisely trim the values of the bias resistors. Precision Monolithics Inc. (now a part of Analog Devices) was a pioneer in this technique known as *zener zapping*. It automatically trims V_{OS} at the wafer level, by using a computer-controlled laser to effectively short one or more of a string of zener diodes, and thereby reduces the offset voltage from the millivolt level to less than 100 μV. By using computer control, this process takes less than 1 second per device on the production line. Applying similar techniques to current sources would result in much improved accuracy. Any of the current mirrors shown in this chapter, whether NPN or PNP, can include emitter degeneration and could have their emitter resistors precisely trimmed, if you were to use the circuit as part of a custom-made ASIC.

4.7 Cascode current mirrors

Although the current mirrors depicted in Figures 4.29 and 4.30 are easy to work with and give adequate performance, they lack much output impedance, or sharp regulation, and are not very good at high frequency either. However, better regulation can be achieved by using two similar devices in a cascode configuration. An example of a PNP cascode current mirror is shown in Figure 4.31. The figure shows a PNP cascode, but the circuit may be configured as an NPN cascode. A monolithic quad device will be perfect for this application. Cascoding generally improves high-frequency operation and provides even greater output impedance (Z_{OUT}). It also permits higher-voltage operation and compliance and appreciably reduces the small-signal output conductance (h_{oe}).

You have probably noticed that at first glance this looks exactly like the Full Wilson circuit (shown in Figure 4.27), but upon closer inspection you will see it is not. In the Full

EX-1006 053
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.



A. The PNP Cascode Current Source

Figure 4.31. The Cascode configuration provides higher frequency response and maximum output impedance.

Wilson, the pair of upper base terminals go to the right. With the cascode, the same two bases go to the left, and in this circuit cascoding buffers the current source from the load. As you will recognize, this is a basic current mirror, but with a common-base PNP transistor inserted into each collector leg (see Figure 4.31B). While the common-base configuration provides no current gain ($h_{fb} = < 1$), it does provide a very high output impedance (Z_{OUT}), typically of more than 10 MΩ. The common-base transistor makes V_{CE} relatively constant for the mirror transistors but greatly increases the output resistance. This means that while the emitter voltage of Q_4 remains constant, variations in the load voltage are accommodated by Q_2's V_{CE}. As a result, the voltage drop across the current source remains constant. Here the reference current (I_{C3}) is regulated by Q_3, and R sets the desired current, as previously discussed. In early development, the resistor R could be substituted by a multiturn potentiometer. This would allow easy adjustment of the desired current level, which could range from a few μA to many milliamps. (Because its tempco will not be as good as a 0.1% tolerance, 50-ppm precision resistor, it should be replaced by a quality fixed resistor.) The cascode circuit provides an internal circuit impedance of more than 10 MΩ at current

EX-1006 054
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

levels less than 1 mA. It can be used equally well in circuits of more than 40 volts or down to about 3 volts, depending on one's exact choice of transistors. Because of its high impedance and reduced Miller capacitance, it also has very good high-frequency response. The basic equations for configuring the cascode circuit are shown here. It is assumed that the Q_1 and Q_2 pair, as well as the Q_3 and Q_4 pair, are all matched for V_{BE} and gain.

The following determines either the reference current, I_{REF}, or the value for resistor R:

$$I_{REF} = \frac{+V - 2V_{BE}}{R} \qquad \text{(Eq.4.74)}$$

$$R = \frac{+V - 2V_{BE}}{I_{REF}} \qquad \text{(Eq.4.75)}$$

The output current, I_{C2}, is determined by:

$$I_{OUT} = I_{REF}\left(1 - \left(\frac{2}{\beta^2 + 2\beta + 2}\right)\right) \qquad \text{(Eq.4.76)}$$

The output resistance (r_o) for this four-transistor cascode current source is given by the internal collector-to-emitter resistance (r_{ce}), derived from the BJT's small-signal model, times beta squared. This accounts for the very-high-output resistance, which can range from about 1 MΩ to more than 100 MΩ:

$$r_o = \beta^2 r_{ce2} \qquad \text{(Eq.4.77)}$$

where again r_{ce} is determined by:

$$r_{ce} = \frac{V_{CE}}{I_C} \qquad \text{(Eq.4.78)}$$

This inexpensive, five-component circuit can be used as either a precision current source or sink, because the load can be connected to either terminal. Alternately, one can build an NPN cascode configured similarly. Even lower h_{oe} (output conductance) for the same current is achieved by the cascode, as a result of degenerative feedback. Here the circuit's output conductance (g_o, measured in either μS or μmhos) is much less than the h_{oe} of the single (noncascode) BJT circuit—at least 10 times lower. You

EX-1006 055
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

can expect the cascode circuit's output conductance to be less than 20 μS. Regulation is about the same as the Wilson cells and will also have a really sharp knee, versus the softer knee of the other noncascode single BJT's circuits. The two big advantages with this circuit over most others is its much higher output resistance, and as a result its good high-frequency response.

Another example of a PNP cascode current mirror is shown in Figure 4.32. Here the bases of the cascode transistors are driven from a precision bandgap voltage reference, which provides a constant voltage and added temperature stability. It also provides multiple outputs, high output impedance, and good high-frequency performance. The circuit could be built using two PNP quad arrays. Transistors Q_1 to Q_4 could comprise one package, while the remaining Q_5 to Q_7 are the second package.

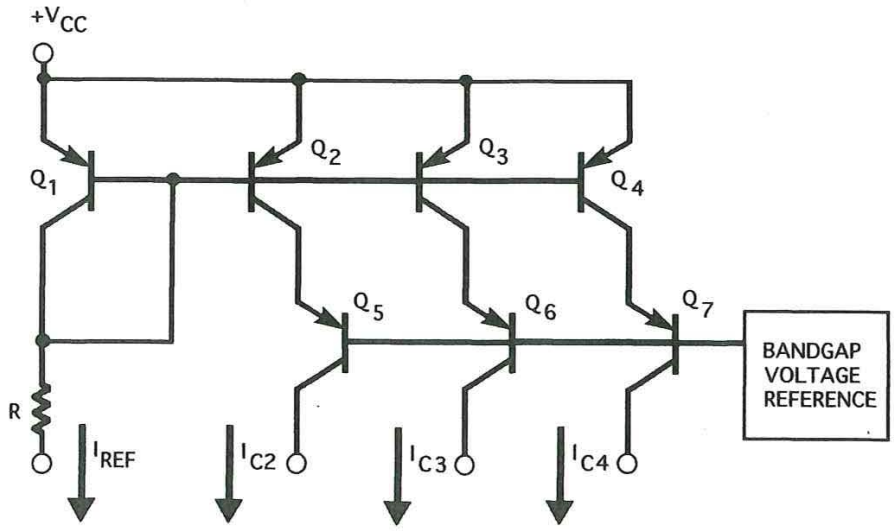


Figure 4.32. Multiple cascode current mirrors.

The following equation determines either the reference current, I_{REF}, or the value of the resistor R:

$$I_{REF} = \left(\frac{V_{CC1} - V_{BE1}}{R} \right) \qquad \text{(Eq.4.79)}$$

EX-1006 056
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

$$R = \left(\frac{V_{CC1} - V_{BE1}}{I_{REF}} \right) \qquad \text{(Eq.4.80)}$$

In this circuit the output current, I_{C2}, is determined by:

$$I_{OUT} = \frac{\beta I_{REF}}{\beta + n + 1} \qquad \text{(Eq.4.81)}$$

To further illustrate the importance of the PNP multiple cascode circuit, Figure 4.33 shows the biasing and input circuitry for a typical bipolar voltage-feedback op amp, using a PMOS transistor pair input stage. As you will recognize, the input stage relies on a PNP multiple cascode, as well as an NPN current mirror using emitter degeneration.

4.8 Current scaling

With the exception of the Widlar and the Wyatt current sources, up until now we have looked at current sources that generate input-to-output currents in a 1:1 ratio, but it is often necessary to generate integer multiples or fractions on an initial current. For the IC designer this is accomplished in the design by creating transistors with multiple emitters, or with bulk emitter area ratioed in either greater or lesser amounts. In this way a current can be made, say, 10 times or one-tenth of the initial input current. It is sometimes depicted in a manufacturer's circuit schematic as a number written next to the particular emitter (see Figure 4.22D). It is sometimes shown, for example, as 10E or 10A.

For the board-level designer, generating multiples or fractions of an initial current can be accomplished in different ways. One way to do this is by paralleling individual transistors as shown in the following circuits, in what is known as *current scaling*. The two circuits shown in Figure 4.34 are simple two times multipliers, which multiply the reference current (I_{REF}).

In either NPN or PNP multiplier circuits, the reference current, I_{REF}, is determined by:

$$I_{REF} = \left(\frac{V_{CC1} - V_{BE1}}{R} \right) \qquad \text{(Eq.4.82)}$$

Also because the reference current is composed of both Q_1's collector current and the three base currents, then:

$$I_{REF} = I_{C1} + 3I_B \qquad \text{(Eq.4.83)}$$

EX-1006 057
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

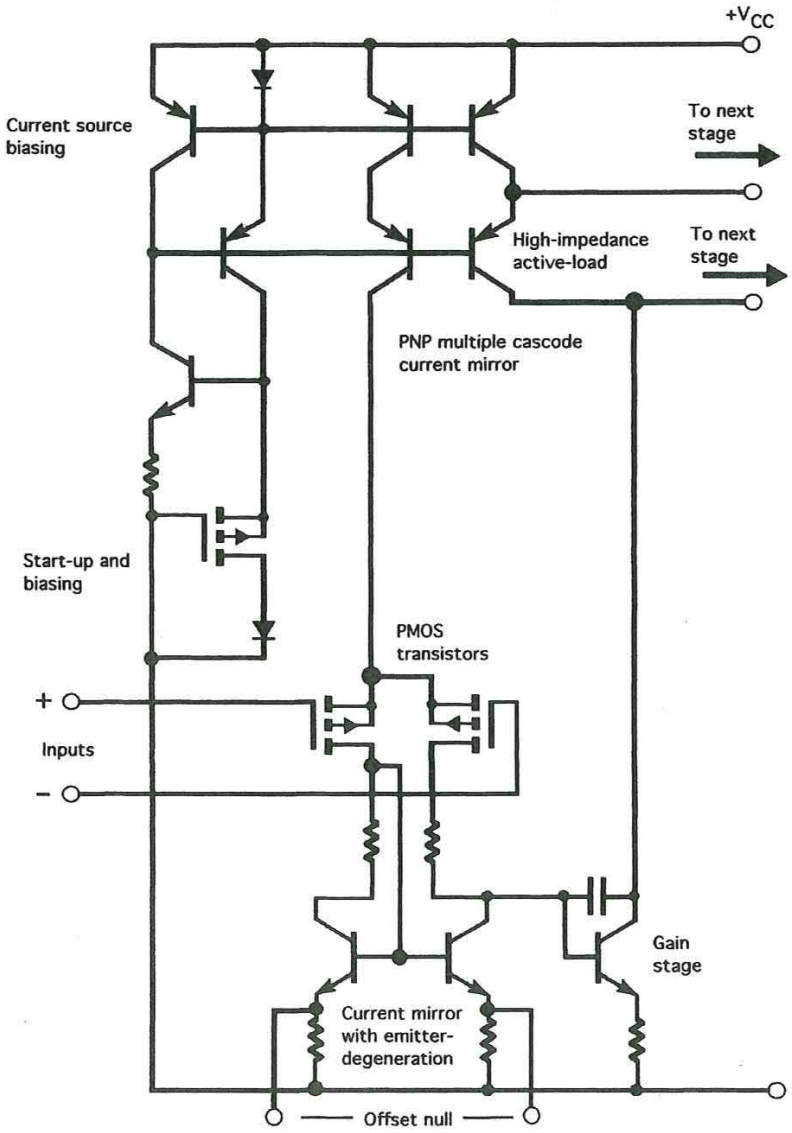


Figure 4.33. *Example showing how cascoded current sources and a current mirror are used for active loads and biasing in a typical bipolar-FET voltage-feedback op amp.*

EX-1006 058
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

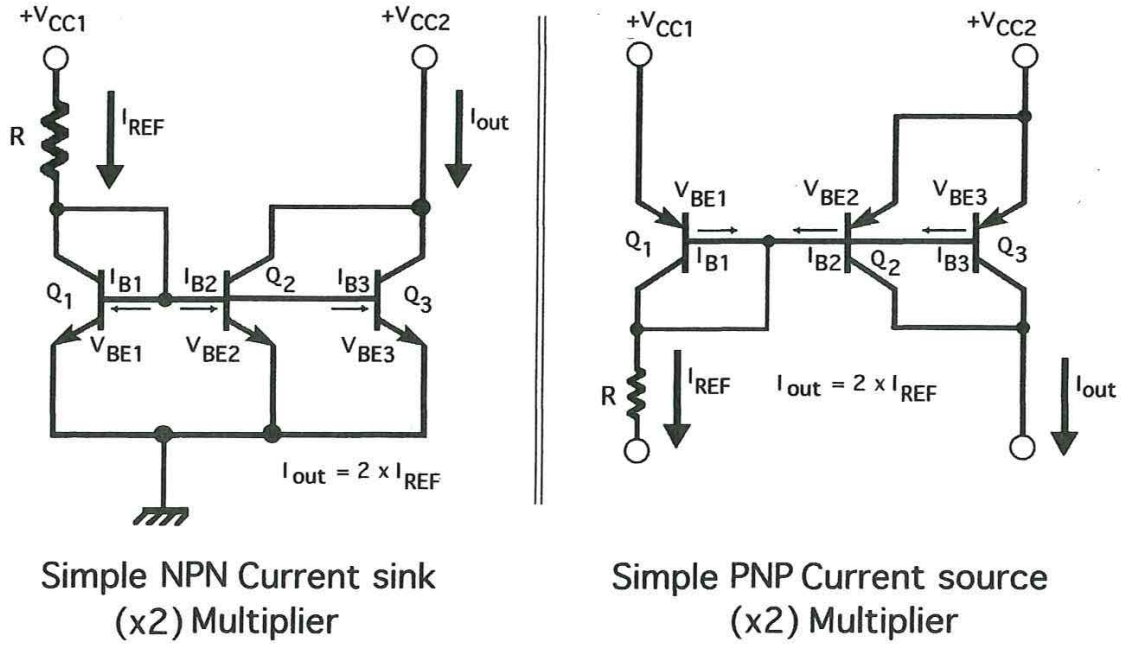


Figure 4.34. Examples of current multipliers.

Because the I_{REF} current is now mirrored by parallel-connected Q_2 and Q_3, the output current is therefore doubled. The output current, I_{C3}, is determined by:

$$I_{OUT} = 2\left(\frac{\beta}{\beta + 2}\right)\left(\frac{V_{CC1} - V_{BE1}}{R}\right) \qquad \text{(Eq.4.84)}$$

$$\therefore I_{C3} \cong 2I_{C1} \qquad \text{(Eq.4.85)}$$

The output resistance (r_o) for this configuration is given by the internal collector-to-emitter resistance (r_{ce}) of Q_3, derived from the BJT's small-signal model:

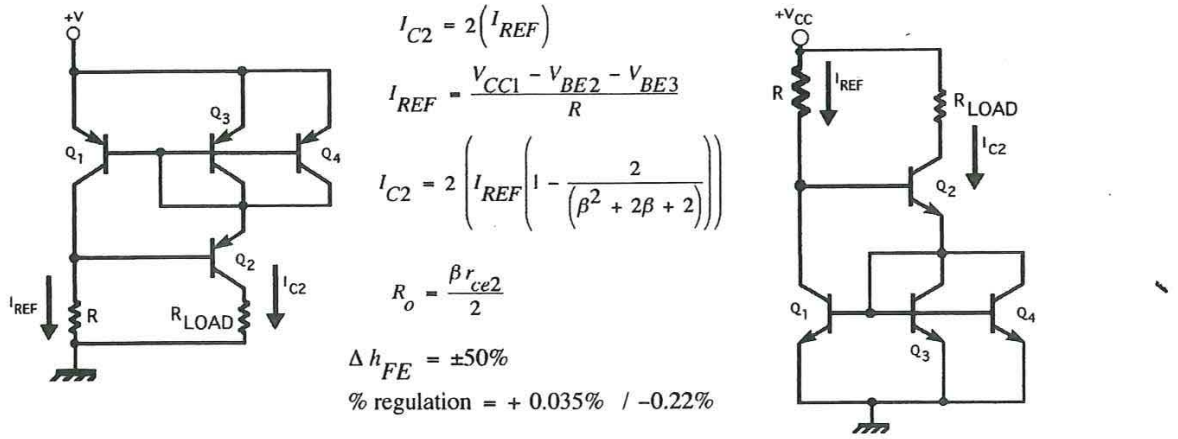
$$r_o = r_{ce3} \qquad \text{(Eq.4.86)}$$

where again r_{ce} is determined by:

$$r_{ce} = \frac{V_{CE}}{I_C} \qquad \text{(Eq.4.87)}$$

EX-1006 059
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

Overall, the circuits work well and are simple to use, but remember that they are somewhat sensitive to differences in transistor gain and have only a modest output resistance. Because of base current errors, their accuracy may be reduced (from that of a 1:1 circuit) by about 1% to 2%. They will work down to around 2 volts or up to about 30 volts depending on your choice of transistors.



A.
A modified basic Wilson PNP current source forms an effective x 2 multiplier.

B.
A modified basic Wilson NPN current sink forms an effective x 2 multiplier.

Figure 4.35. Examples of modified Wilson current multipliers.

For greater accuracy, the two circuits shown in Figure 4.35 (which are modified Basic Wilsons) would also provide two times multiplication, but with higher output resistance. The relevant equations are shown in the diagram. To illustrate how they work, let's design a 424-μA current source, with a 212-μA input. We will be using a quad device

EX-1006 060
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

such as an MMPQ-3904 (NPN) or an MMPQ-3906 (PNP), and assume that all of the V_{BE}s and h_{FE}s are identical. The supply voltage will be 6 volts. Therefore:

$$V_{CC1} = 6V \qquad \text{(Eq.4.88)}$$
$$V_{BE1} = V_{BE3} = V_{BE4} = 0.65V$$
$$\beta_{Q1} = \beta_{Q3} = \beta_{Q4} = 50$$
$$I_{B1} = I_{B3} = I_{B4} = 10\mu A$$
$$I_{REF} = 212\mu A$$
$$I_{OUT} = 424\mu A$$

We will begin by determining the resistor setting value (R), so that:

$$R = \frac{6V - 0.65V - 0.65V}{212\mu A} = 22.17K\Omega \qquad \text{(Eq.4.89)}$$

Because the I_{REF} current is now mirrored by parallel-connected Q_3 and Q_4, the output current is therefore doubled. The output current ($I_{C2} = I_{OUT}$) is determined by:

$$I_{OUT} = 2\left(212\mu A\left(1 - \left(\frac{2}{50^2 + 2 \bullet 50 + 2}\right)\right)\right) = 423.7\mu A \qquad \text{(Eq.4.90)}$$

The minimum output resistance (r_o) is approximately:

$$r_o = \frac{55000}{2} = 27.5K\Omega \qquad \text{(Eq.4.91)}$$

Because these current sources are a modification of the Basic Wilson, they are much less sensitive to gain mismatches (beta-compensated) and provide excellent regulation and reasonable output resistance. Let's calculate the difference in output for a ±50% change in beta. For a 50% reduction in gain, this would mean that the gain is now 25, thus:

$$I_{OUT} = 2\left(212\mu A\left(1 - \left(\frac{2}{25^2 + 2 \bullet 25 + 2}\right)\right)\right) = 422.74\mu A \qquad \text{(Eq.4.92)}$$

EX-1006 061
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

For a 50% increase in gain, this would mean that the gain is now 75, so that:

$$I_{OUT} = 2\left(212\mu A\left(1 - \left(\frac{2}{75^2 + 2 \bullet 75 + 2}\right)\right)\right) = 423.85\mu A \qquad \text{(Eq.4.93}$$

Considering that the nominal output current with a gain of 50 is 423.7 μA, this equates to a change in output of –0.22% for a 50% reduction in gain or a +0.035% for a 50% increase in gain. This is impressive regulation, all created by beta-compensation, but in practice because of base current errors, their accuracy may be reduced (from that of a 1:1 circuit) by about 1% to 2%. These circuits will probably work well down to about 2 volts or above 30 volts, if required.

Those were some examples of multiplying a current, but it's just as easy to *divide* the reference current. Consider this: if one paralleled the transistor normally handling the reference current, then the same reference current would flow, but now through two or more paralleled collectors (NPN) or emitters (PNP). Mirroring the current from either transistor will create an output that is just half of the reference current (i.e., divided by two). Figure 4.36 illustrates this point.

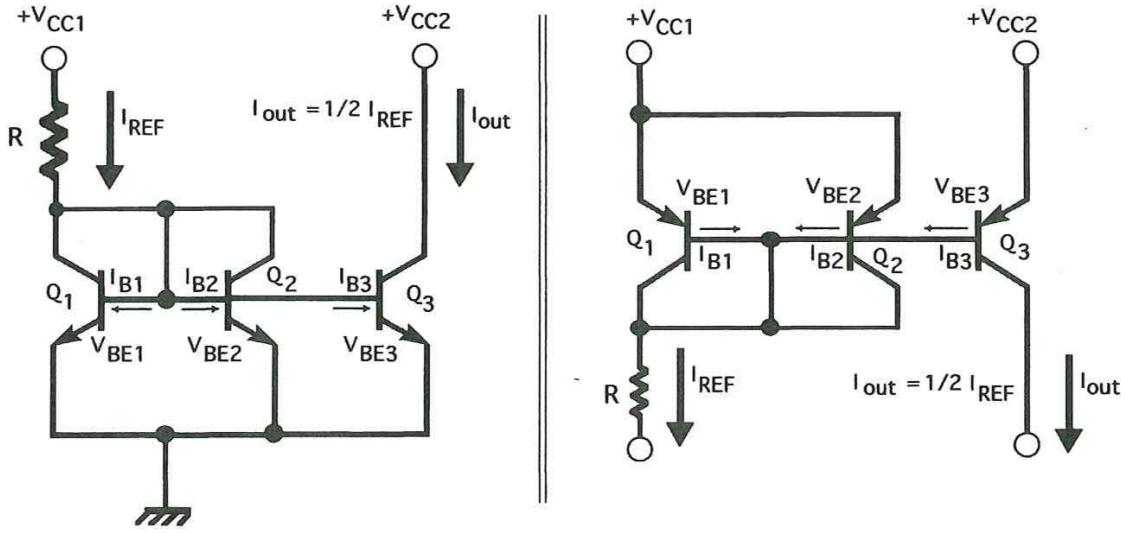


Figure 4.36. Examples of current dividers.

EX-1006 062
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To determine the reference current, I_{REF}, in either the NPN or PNP divider circuit:

$$I_{REF} = \left(\frac{V_{CC1} - V_{BE1}}{R} \right) \quad \text{(Eq.4.94)}$$

Also, because the reference current is composed of both Q_1's collector current and the three base currents, then:

$$I_{REF} = I_{C1} + 3I_B \quad \text{(Eq.4.95)}$$

The output current, I_{C3}, is determined by:

$$I_{OUT} = \frac{\left(\frac{\beta}{\beta + 2} \right) \left(\frac{V_{CC1} - V_{BE1}}{R} \right)}{2} \quad \text{(Eq.4.96)}$$

$$\therefore I_{C3} \cong \frac{I_{C1}}{2} \quad \text{(Eq.4.97)}$$

The output resistance (r_o) for this configuration is given by the internal collector-to-emitter resistance (r_{ce}) of Q_3, derived from the BJT's small-signal model:

$$r_o = r_{ce3} \quad \text{(Eq.4.98)}$$

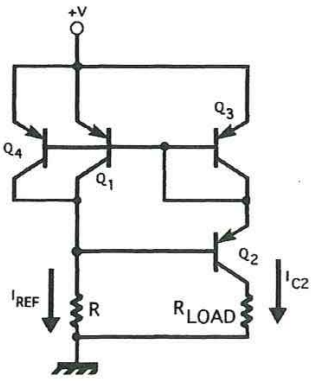
where again r_{ce} is determined by:

$$r_{ce} = \frac{V_{CE}}{I_C} \quad \text{(Eq.4.99)}$$

The two circuits work well and are simple to use, but they are sensitive to differences in transistor gain and have only a modest output resistance. In practice because of base current errors, their accuracy may be reduced (from that of a 1:1 mirror circuit) by about 1% to 2%. They will work down to around 2 volts or up to about 30 volts depending on the choice of transistors.

As with the previous multiplier circuits, we can use modified Basic Wilsons, which would also provide division-by-two, greater accuracy, and a higher output resistance. Two such circuits are shown in Figure 4.37. The relevant equations are shown in the diagram. As with the previous multiplication and division circuits, accuracy may be reduced (from that of a 1:1 mirror circuit), by about 1% to 2%. Either circuit can be easily built using a monolithic quad device, for optimum thermal considerations.

EX-1006 063
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.



$$I_{C2} = \left(\frac{I_{REF}}{2}\right)$$

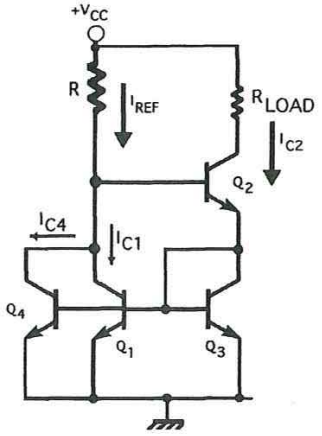
$$I_{REF} = \frac{V_{CC1} - V_{BE2} - V_{BE3}}{R}$$

$$I_{C2} = \left(\frac{I_{REF}\left(1 - \frac{2}{\left(\beta^2 + 2\beta + 2\right)}\right)}{2}\right)$$

$$R_o = \frac{\beta r_{ce2}}{2}$$

$$\Delta h_{FE} = \pm 50\%$$

% regulation = + 0.035% / −0.22%



A.
A modified basic Wilson PNP current source forms an effective (÷2) divider.

B.
A modified basic Wilson NPN current sink forms an effective (÷2) divider.

Figure 4.37. Examples of modified Wilson current dividers.

Another way of performing multiplication or division of the reference current is by adding resistors. This was alluded to previously when looking at Widlar's circuits (see Figure 4.20). Now, if a resistor is inserted in series with the emitter of Q_2 in the divided circuit in Figure 4.38, the output current ratio between the two devices is no longer matched, but is divided and dependent on V_{BE} and the value of the resistor. This is also true for the multiplier circuit in which the reference current is multiplied, by putting R_2 in series with Q_2's emitter. These circuits are reasonably resistant to changes in the supply voltage and have a medium output impedance, although they do have a somewhat higher temperature coefficient than some of the other circuits we have looked at.

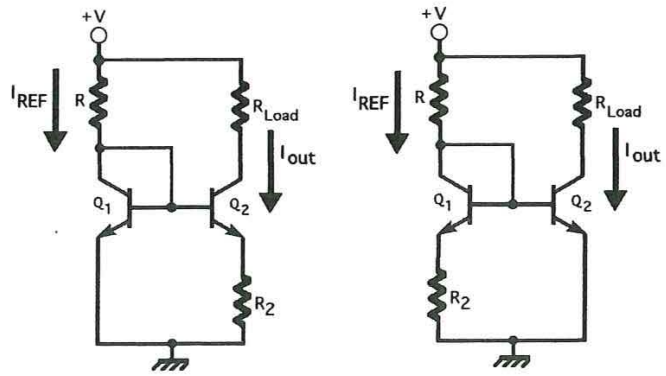
4.9 Modified current sources and example applications

For the rest of the chapter we will look at some applications, as well as some modified current sources, which may prove useful in one of your designs.

4.9.1 Running the current source from split power supplies

It's often necessary to run the current source in a split power supply situation. Figure 4.39 shows two examples: one a simple NPN 1.49-mA current sink and the other a simple PNP 3.47-mA current source. The relevant equations are shown, which apply to either configuration. Make sure that the combined +V and –V supply combination is a lot less than the breakdown voltage rating for the transistors you use. For higher out-

EX-1006 064
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.



Dividing the reference current.

Multiplying the reference current.

Figure 4.38. Adding an emitter resistor provides an alternative method.

put impedance, use either type of Wilson current mirror, or the cascode, and connected to the supply rails in a similar manner.

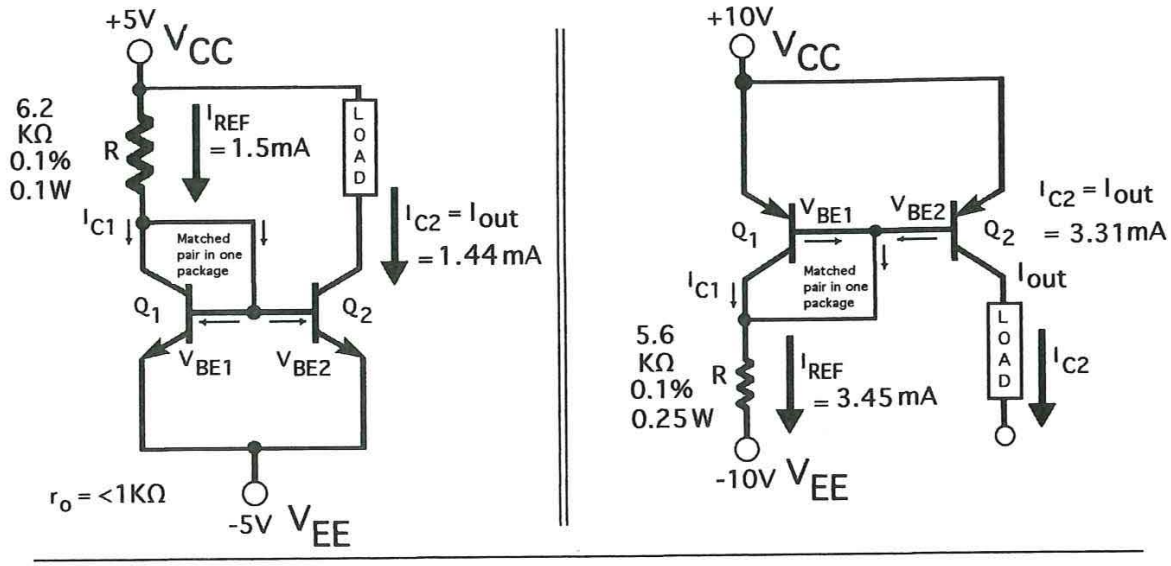
4.9.2 Improving power supply rejection

In a multiple-output current mirror, such as previously described in Figure 4.28, if greater power supply rejection is needed, then the circuit in Figure 4.40 can be used. For a 75% change in supply voltage, the output current will change only about 2%. Q_1 and Q_2 are both diode-connected and establish a two times V_{BE} potential at the bases of Q_3 and Q_4. This produces a potential of one times V_{BE} across the emitter resistors of Q_3 and Q_4, and causes current to flow in each collector. The current in R_2 and R_3 is I_{PTAT}, and the temperature coefficient (tempco) will be a little higher because of the 2 mV/°C change of V_{BE} with temperature. The output collector currents in Q_2 and Q_3 are determined by either transistor's V_{BE}, divided by its respective emitter resistor. Hence:

$$I_{OUT} = \frac{V_{BE}}{R_2} = \frac{0.7V}{467\Omega} = 1.5mA \qquad \text{(Eq.4.100)}$$

In some applications, using either a low-cost bandgap voltage reference IC (I_{OUT} = less than 10 mA) or a small linear regulator (I_{OUT} = less than 50 mA) nearby with bypass capacitors may be a much better solution, together with using a Wilson or cascode current source. This would significantly stabilize voltage levels, improve current regulation and accuracy, and boost the output impedance.

EX-1006 065
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.



$$I_{REF} = \frac{V_{CC} + V_{EE} - V_{BE}}{R} \qquad I_{OUT} = \left(\frac{\beta}{\beta + 2}\right)\left(\frac{V_{CC} + V_{EE} - V_{BE}}{R}\right)$$

$$R = \frac{V_{CC} + V_{EE} - V_{BE}}{I_{REF}} \qquad r_o = r_{ce2}$$

Figure 4.39. Simple current sources running on split (±) supplies.

4.9.3 Alternative current divider

In this circuit, shown as Figure 4.41, the input reference current I_{REF} is mirrored by I_{C1}. This current is then divided by two. The upper three transistors (Q_1, Q_2, and Q_3) comprise a Basic Wilson current source, which is a cascode for the constant current divider. This is made up by the five lower transistors (Q_4, Q_5, Q_6, Q_7, and Q_8). For optimum performance, Q_1 and Q_2 should be matched, as well as Q_4 with Q_5, and then Q_6 with Q_7 and Q_8. This would require using a quad transistor array for Q_1, Q_2, and Q_3; a dual transistor array for Q_4 and Q_5; and another quad package for Q_6, Q_7, and Q_8. The circuit would have precision, good regulation, a very high output impedance, and create two equal output currents. The circuit operates from around 3.6 volts up to the limiting voltage of the transistors.

4.9.4 Modified three-transistor mirror-source

The circuit in Figure 4.42 is a modified PNP version of the three-transistor current sink we looked at earlier in this chapter, plus an extra mirror transistor. The equations for this are shown in the diagram. The output current (I_{OUT}) is calculated differently

EX-1006 066
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

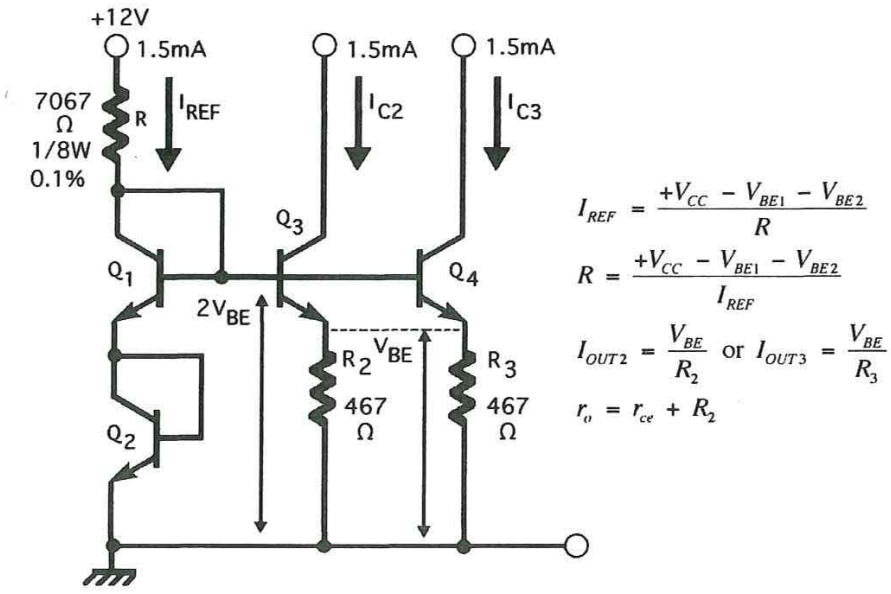


Figure 4.40. Improved NPN current mirror with enhanced power-supply rejection.

because it uses two output transitors (Q_3 and Q_4; thus n = 2). Normally one would likely incorporate small-value resistors in the emitters of the three upper transistors (Q_1, Q_3, and Q_4) for compensating any V_{BE} mismatches. If the application used a prime-grade, precision matched-pair instead, with a guaranteed maximum ΔV_{BE} of less than 1 mV, those emitter resistors would not be needed, in which case the error reduction would be proportional to beta^2. The circuit may be slow to turn off, because it has no base turn-off current. One way to remedy this is by adding either a reverse-biased diode or a resistor, as shown in the dotted line. In the case of the resistor, it may degrade accuracy somewhat.

4.9.5 Current source linearly charges capacitor in VCO

A current source is frequently used to charge a capacitor, because the constant current action generates a linear ramp across the capacitor. Figure 4.43 shows such a circuit. When the charge and discharge currents are identical, then the output waveform will also be symmetrical. When integrated into part of a timer or oscillator IC, this linear charging and discharging helps provide accuracy and repeatability. Depending on what kind of oscillator circuit the capacitor is part of, the output waveform may be a ramp, triangle, sine, square wave, and so on. The voltage-sensing circuit normally has an upper and a lower threshold. Assuming a constant charging current, then once the voltage level on the charging capacitor reaches the upper threshold, this triggers the circuit's output to change state. This turns the capacitor charging circuit off, while turning the discharge circuit on. The capacitor now discharges at a constant current. Once

EX-1006 067
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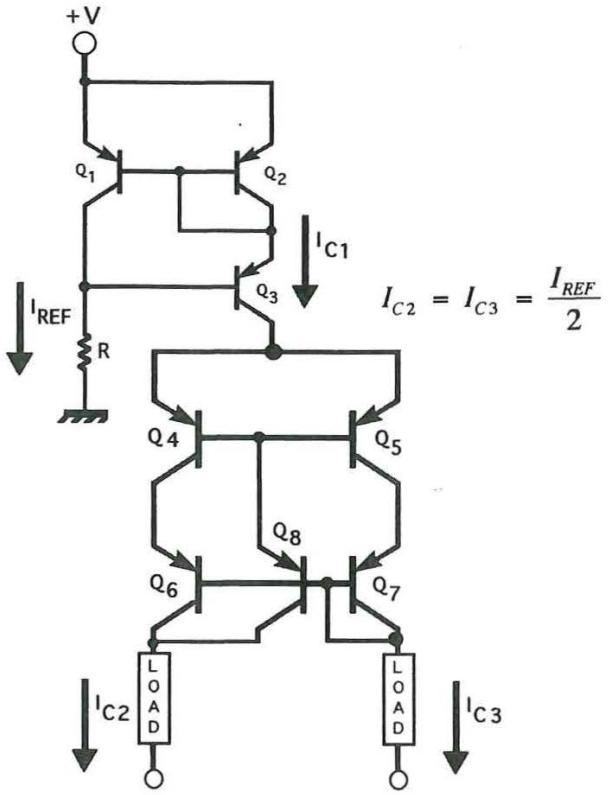


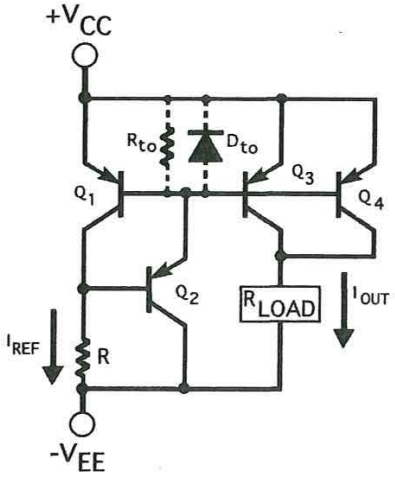
Figure 4.41. A novel current divider.

the discharge voltage level reaches the lower threshold, this triggers the output to change state again, and the process repeats.

In this circuit, transistors Q_1 and Q_2 form a composite NPN/PNP current source. Although it is simple, it is effective; it has low output capacitance, and thus offers a high bandwidth. The control voltage at the base of Q_1 establishes the current I_{REF} into the current mirror comprised of Q_3 and Q_4. Transistor Q_5 is simply used as a switch by the flip-flop's output, which controls the charge/discharge cycle. When Q_5 is off, the capacitor is linearly charged by the constant current through Q_2 and steering diode D_2. It may be expressed by the following equations:

$$Q = I t \ ; \text{ in coulombs} \qquad \text{(Eq.4.101)}$$

EX-1006 068
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.



$$R = \frac{V_{CC} + V_{EE} - V_{BE1} - V_{BE2}}{I_{REF}}$$

$$I_{REF} = \frac{V_{CC} + V_{EE} - V_{BE1} - V_{BE2}}{R}$$

$$I_{OUT} = I_{SET}\left(\frac{n\,\beta^2}{\beta^2 + n + 1}\right)$$

$$r_o = r_{ce3}$$

NOTE: R_{to} or D_{to} can be used to increase the circuit's turn-off speed.

Figure 4.42. Modified 3-transistor mirror-source.

$$I = \frac{Q}{t} \;;\; \text{in Amps} \qquad \text{(Eq.4.102)}$$

$$I = C\frac{\Delta V}{\Delta T} \;;\; \text{in Amps} \qquad \text{(Eq.4.103)}$$

Once the voltage across the capacitor has reached the comparator's upper trip-point (established by the voltage between R_2 and R_3), the flip-flop changes state and switches on Q_5. The I_{REF} current via Q_1 and Q_2 establishes the current into the current mirror Q_3 and Q_4. With D_2 now effectively reverse-biased, the capacitor discharges at a constant rate via Q_4 and Q_5. Once the lower threshold is reached (established by the voltage between R_3 and R_4), the flip-flop changes state again, and switches Q_5 off. The oscillator's duty cycle is fixed because the charge and discharge currents are identical. The circuit offers good stability, on the order of 100 ppm/°C, and needs at least 3.5 volts to function.

4.9.6 Current source in a high-frequency laser transmitter

In the example shown in Figure 4.44, a diode laser is controlled by an incoming AC waveform, and the resulting modulated beam is then transmitted down a fiber-optic cable. In order to set the correct biasing for the laser, a simple PNP current mirror is used to set a 30-mA quiescent current. The combination of R_2 and P_1 set the refer-

EX-1006 069
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

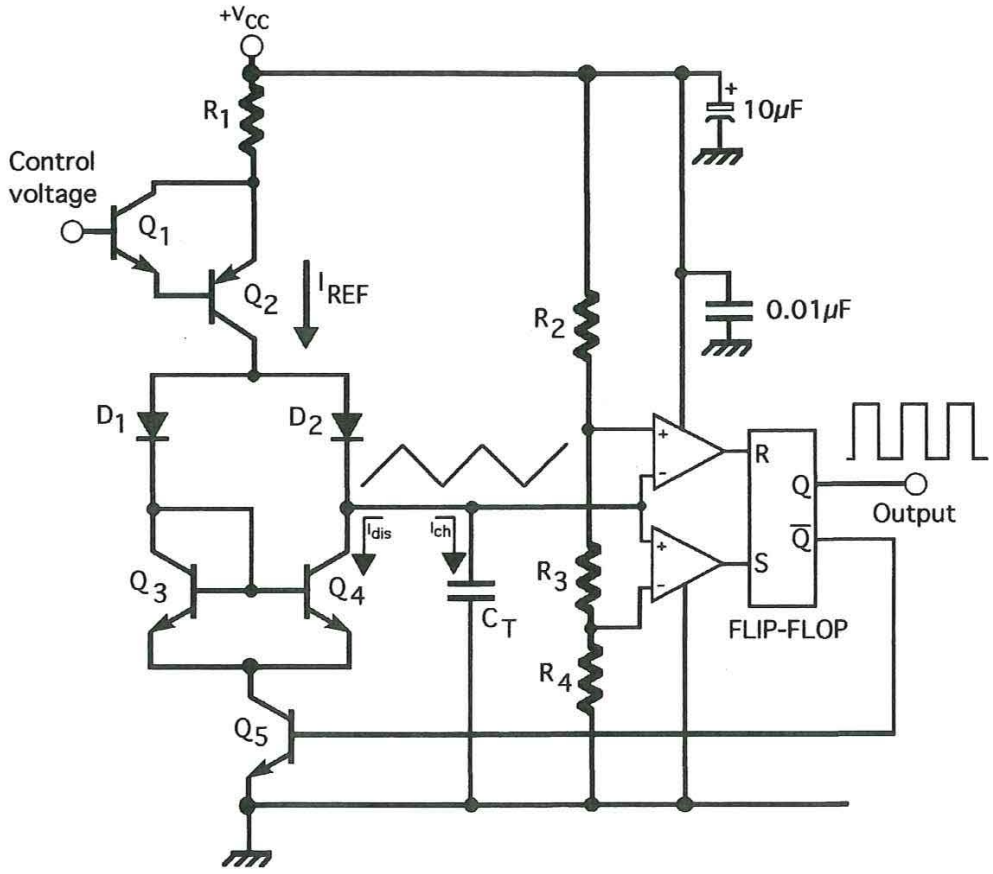


Figure 4.43. This current mirror precisely controls the charge and discharge time of a voltage-controlled oscillator.

ence current, I_{REF}. This current is mirrored by Q_2 as I_{C2}, and so powers the diode laser. Potentiometer P_1 allows adjustment for the optical power required, because this varies slightly from one diode laser to another. Diode D_1 guards the expensive laser diode against any reverse voltages.

4.9.7 Temperature-compensated current sink

Figure 4.45 shows one way of providing temperature compensation for a simple current sink or source. In this circuit, a quad matched array is used, so that differences in h_{FE}, V_{BE}, drift, and temperature effects are all minimized. It also uses a split power supply, although this could be a single positive and ground, or ground and negative supply. Here the collector currents for all four transistors are made identical, so that the output current I_{C4} mirrors the input current I_{C1}. The currents through R_1 and R_2 are equal, as are the currents through R_2 and R_5. The currents through R_3 and R_4 are equal, as are

EX-1006 070
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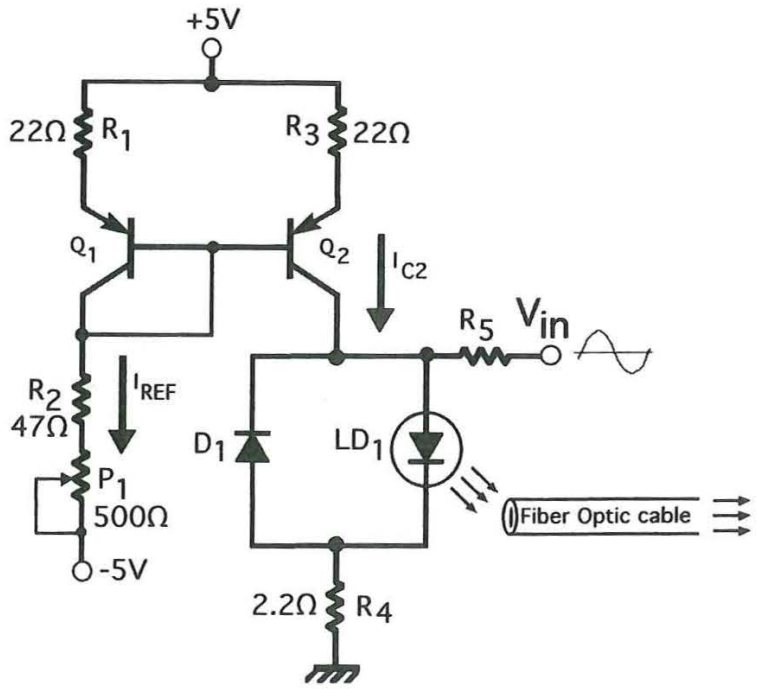


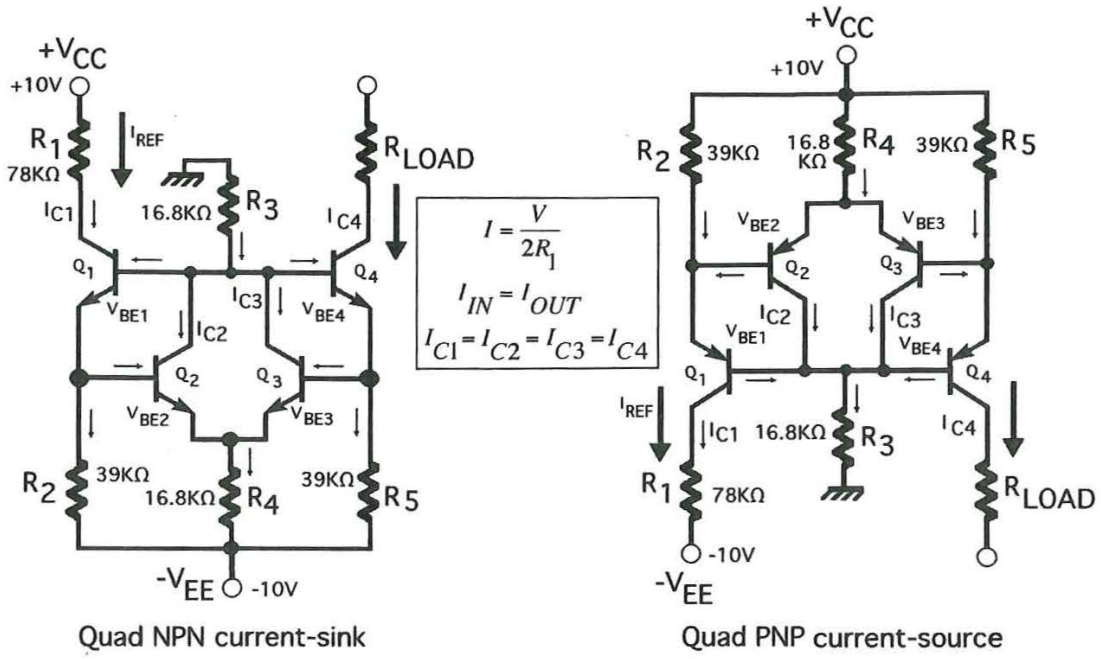
Figure 4.44. *This simple current source sets the quiescent current in this modulated laser transmitter.*

the collector currents I_{C2} and I_{C3} (which are also equal to the collector currents I_{C1} and I_{C4}). Transistors Q_2 and Q_3 both monitor the voltage on R_2 and R_5, repectively, and both compensate Q_1 and Q_4's V_{BE} temperature drift by creating a compensating temperature-dependent current in R_3. This action changes the base voltage of Q_1 and Q_4 so as to oppose their change in V_{BE}. As a result, a state of equilibrium is reached, where the current sink/source provides a constant current, despite changes in temperature. The design equations are shown in the diagram. Similar techniques are also used for current-limiting in some audio output stages and power supplies.

4.9.8 Compound current mirrors

It is common for designers, particularly IC designers, to create compound current mirrors, such as that shown in Figure 4.46. This circuit serves as an example and consists of a PNP quad array and an NPN quad array. Transistors Q_1 and Q_2 form a Basic Wilson current mirror, with I_{C1} mirroring I_{REF}. The current I_{C1} is now mirrored by the Modified Wilson current source Q_5, Q_6, and Q_7, and produces mirrored current I_{C2}. Transistor Q_8 separately mirrors I_{C1}, producing I_{C3}, which feeds into a separate load. The two resulting currents I_{C2} and I_{C3} now flow into the mirrored-sink comprising Q_3 and Q_4. Because this combination multiplies I_{REF} by two, it serves as a mirror-sink for I_{C2} and I_{C3}. Diodes D_1 and D_2 steer the currents and guard against reverse-bias con-

EX-1006 071
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Quad NPN current-sink

Quad PNP current-source

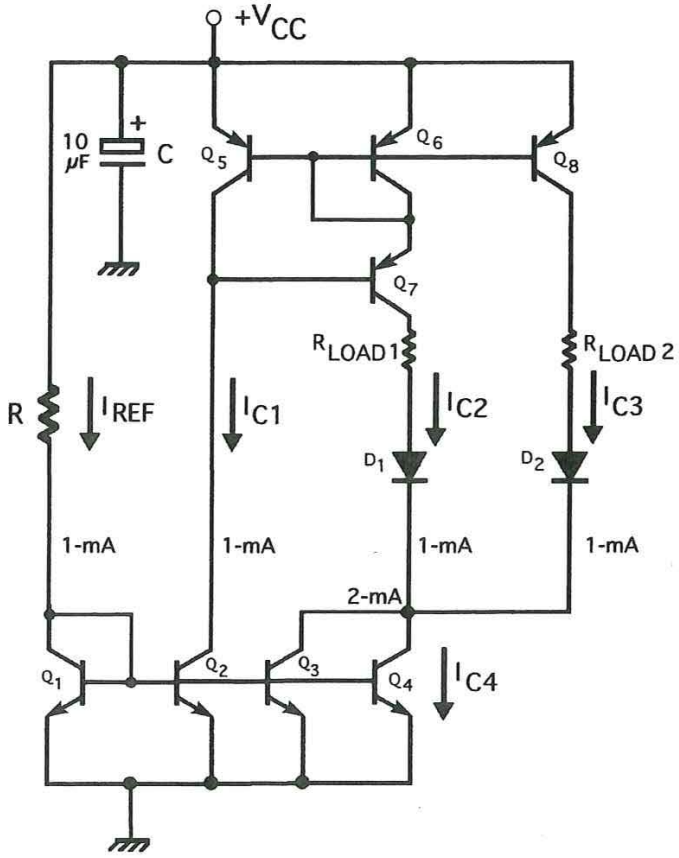
Figure 4.45. Temperature-compensated current sources.

ditions from the two loads. Higher accuracy will be attained if one uses a Wilson current source in place of Q_1 and Q_2. However, this will require more transistors and take up extra circuit board area. It comes down then to accuracy and cost versus size.

4.9.9 Current mirrors help DACs control oscillator frequency and duty cycle

In a machine-tool application, it is necessary to provide a variable drive frequency, with independent duty-cycle control. This circuit (shown as Figure 4.47) would be one of several motion-control circuits and part of a processor-based system. The frequency generation and duty-cycle control would use two 555 timer ICs. Frequency would range from 5 Hz to 250 Hz, and the duty cycle would be variable from 1% to 99%. One timer functions as an astable multivibrator, while the other is used as a one-shot. Rather than using resistors, two Full Wilson current mirrors are used, which improve accuracy, current regulation, impedance, and repeatability. Both mirrors provide constant currents for linearly charging the timing capacitors C_{T1} and C_{T2}. While both currents are regulated, they are also adjustable. This allows adjustment of both the frequency and the duty cycle. The use of Full Wilson current mirrors provides a very high impedance ($r_o = h_{FE} \times r_{ce}$) to either 555 timer circuit, as well as the DAC (both circuits are controlled by 8-bit DACs, which interface with the processor). The DACs set the reference currents for the current mirrors, which in turn duplicate the

EX-1006 072
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$$I_{REF} = \frac{+V_{CC} - V_{BE}}{R}$$

$$R = \frac{+V_{CC} - V_{BE}}{I_{REF}}$$

$$I_{REF} = I_{C1} = I_{C2} = I_{C3}$$

$$I_{C4} = 2\,I_{REF}$$

Figure 4.46. Compound current mirrors.

respective currents. One DAC circuit acts as the Frequency Select, while the other is the Duty-Cycle Select. The op amp acts as a buffer between I_{C1}'s RC timing components and I_{C2}'s high-impedance threshold input. The waveforms and equations are shown in the diagram. The design could use all bipolar devices or a mixture of bipolar and CMOS.

4.9.10 Using current sources as active loads

The circuit in Figure 4.48 shows a typical low-noise amplifier using active loads. There are many advantages in replacing the normal passive-resistive loads in front-end amplifiers with active loads in the form of current sources. Benefits include higher impedance, higher bandwidth, and increased precision. This is especially beneficial in low-noise front-end amplifiers, where the output impedance of the current source provides a high collector resistance, along with a small voltage drop. Noise levels in some precision amplifiers can reach below 1 nV/√Hz, if the circuit is designed well and uses matched transistors.

EX-1006 073
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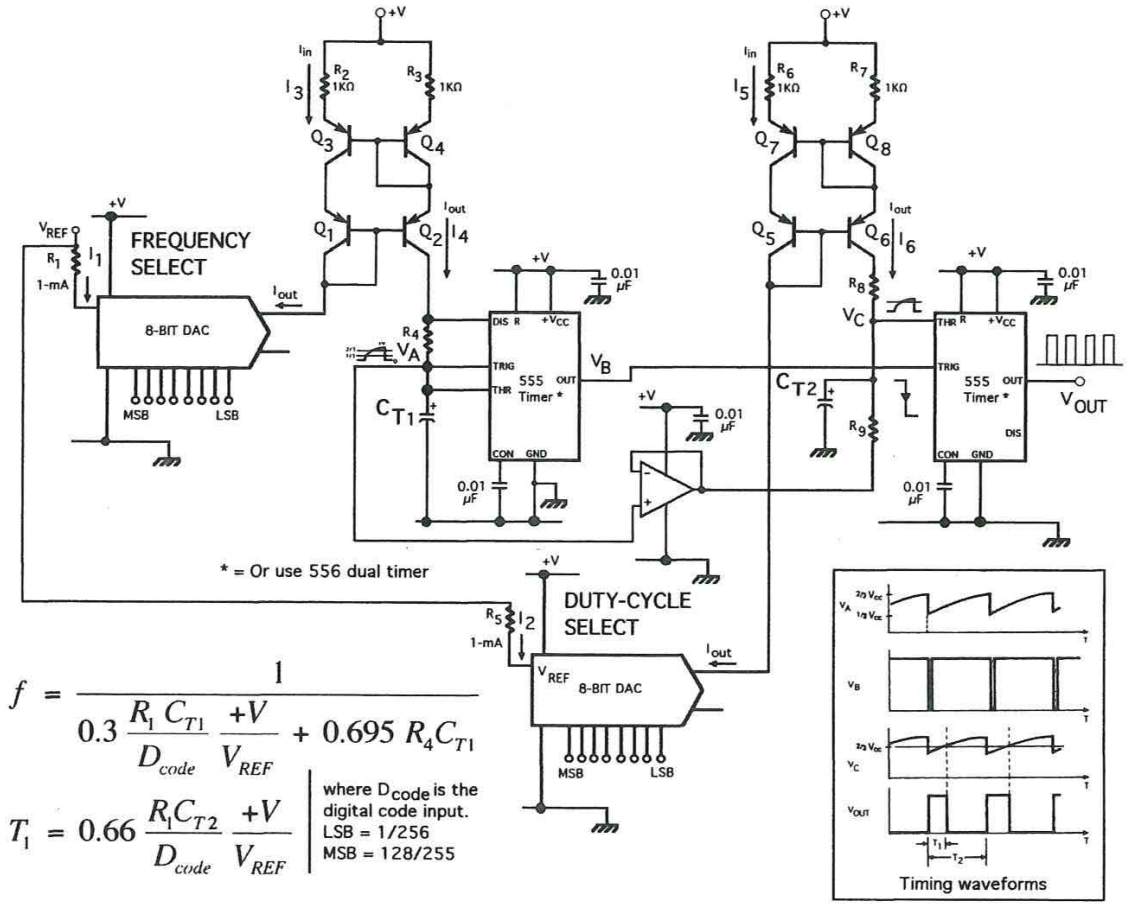


Figure 4.47. Current sources help create a digitally controlled frequency generator, with separate control of frequency and duty cycle.

In this circuit, transistors Q_1, Q_2, and Q_3 form a simple current mirror, with Q_2 and Q_3 mirroring the reference current. The reference current for the multiple PNP current sources is set up by R_2. Transistors Q_4 and Q_5 are the low-noise amplifier pair. The collector current for each transistor is provided by each current mirror. These currents flow through both emitters and feed into the Basic Wilson NPN current sink, which provides excellent regulation. The reference current for the Wilson current sink is set up by R_1. In this example, the I_{REF2} reference current is set for 1 mA, while the I_{REF1} reference current is set for 2 mA. All of the mirror-sources and sinks use emitter-degeneration resistors (R_E = 470 Ω), to reduce differences in the transistors' V_{BE}s and to

EX-1006 074
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

increase the output resistance. The effective load resistance of the differential pair is given as follows:

$$R_{L1} = R_{L2} = r_{ce4} \| \left(r_{ce2} \left(1 + g_m R_{E2} \right) \right) \qquad \text{(Eq.4.104)}$$

4.9.11 Modified current source squares the reference current

Previously in this chapter we looked at ways of multiplying and dividing the input reference current. The example depicted here in Figure 4.49 shows a means of providing a square-law relationship with a relatively low input current (I_{REF}). In this circuit, a simple NPN mirror (composed of transistors Q_1, Q_2, and Q_5) is used to provide a multiple mirror reference current, which is fed to the simple PNP mirror composed of transistors Q_3 and Q_4. As you probably noticed, the circuit is *not* connected quite as normal. A potentiometer is in series with R_1, which allows the input current to be changed, but then an added low-value resistor R_2 is connected in series with both NPN emitters. Additionally, the output is made at the junction of Q_4 and Q_5, via their respective collectors.

Normally with a 1:1 ratio current mirror, an exact duplicate of the input current will be produced at the output. If this were plotted on a graph, it would result in a straight diagonal line from zero (for I_{IN} vs. I_{OUT}). With this square-law circuit, because of the way it is configured, it produces an exponential curve at low currents (less than 400 μA). The transistors in this circuit are considered to have equal h_{FE}s, I_Bs, I_Cs, and V_{BE}s. As a result, the reference current is mirrored by several other currents, as follows:

$$I_{C1} = I_{C2} = I_{C3} = I_{C4} = I_{REF} \qquad \text{(Eq.4.105)}$$

The reference current is determined by:

$$I_{REF} = \left(\frac{V_{CC} - V_{BE1}}{R_{POT} + R_1 + R_2} \right) \qquad \text{(Eq.4.106)}$$

Because the base-emitter voltages are the same for this example, then:

$$V_{BE5} = V_{BE1} + R_2 \left(I_1 + I_2 \right) \qquad \text{(Eq.4.107)}$$

EX-1006 075
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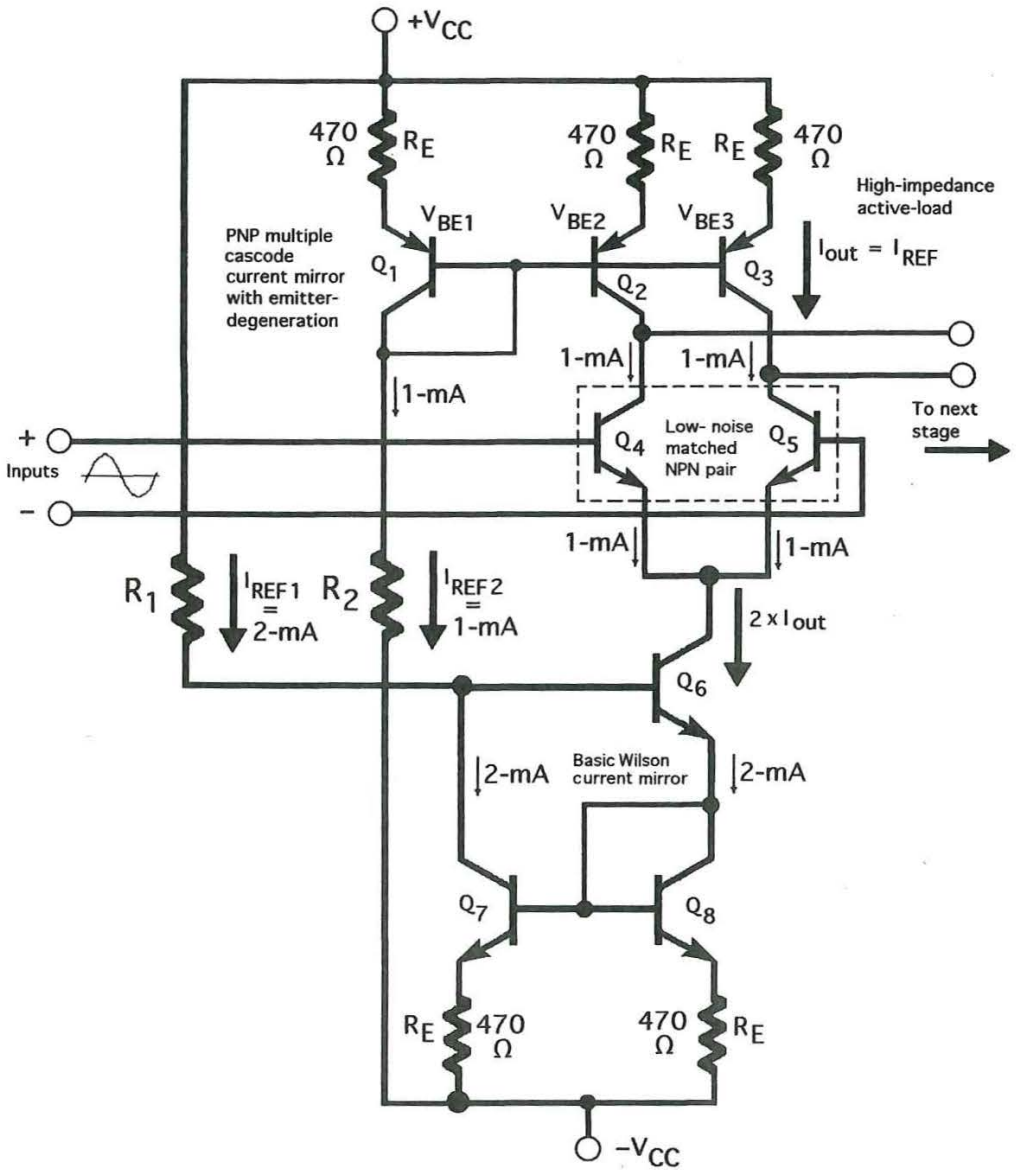


Figure 4.48. Current sources are used as active loads in this front-end differential amplifier circuit.

EX-1006 076
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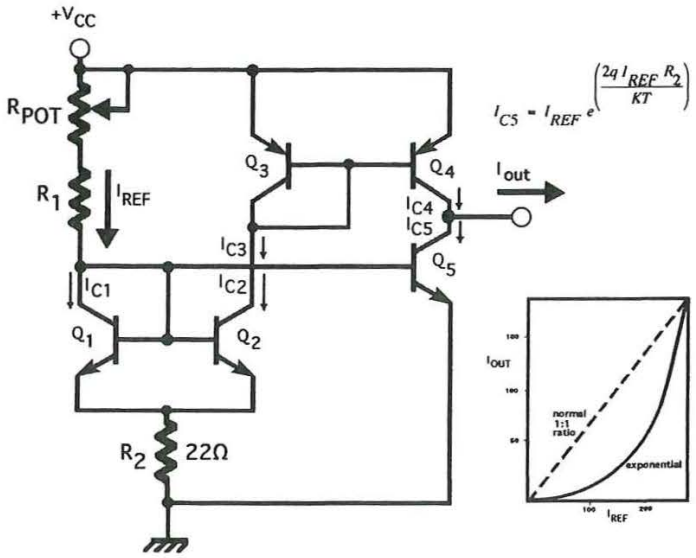


Figure 4.49. Composite current mirrors provide an exponential output current.

The ratio of collector currents between I_{REF} and I_5 can be found by:

$$\frac{I_{C5}}{I_{C1}} = e^{\frac{q\left(V_{BE5} - V_{BE1}\right)}{KT}} \qquad \text{(Eq.4.108)}$$

where: q is the charge on an electron (1.6×10^{-19} J);

K is Boltzmann's constant (1.38×10^{-23} J/°K);

T is the temperature (°Kelvin; 298°K = 25°C)

Transistor Q_5's collector current can be determined by:

$$I_{C5} = I_{REF}\, e^{\left(\frac{2q\, I_{REF}\, R_2}{KT}\right)} \qquad \text{(Eq.4.109)}$$

The output resistance for this configuration is fairly low and can be found by:

$$r_o = r_{ce} \qquad \text{(Eq.4.110)}$$

EX-1006 077
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The output current, I_{OUT}, can be described as:

$$I_{OUT} = I_5 - I_{REF} = I_5 - I_4 \qquad \text{(Eq.4.111)}$$

The circuit can be built using a PNP matched-pair and an NPN matched-quad, unless you want to integrate this into part of a custom IC design.

4.9.12 Digitally controlled variable current source

The circuit shown in Figure 4.50 illustrates how to provide an adjustable/variable current source with a digital interface, using a digital pot. The digital pot has 256 settings, and in this case (as an option) also has an on-board EEPROM. The EEPROM retains the last setting before power was removed. When the system is powered up again, the same setting is provided from the EEPROM. This saves the microcontroller time and program steps having to reconfigure the current source to the present setting. In this circuit, the resistance value in the digital pot translates into a particular current setting (I_{SET}) to the current source. The Full Wilson current source mirrors this current precisely and outputs the mirrored current to the load. Emitter degeneration is provided by resistors R_1 and R_2 to compensate for V_{BE} mismatches, and the current mirror presents a high-output impedance to the load. Manufacturers of digital pots that have an on-board EEPROM include Analog Devices, Maxim/Dallas, and Intersil/Xicor.

4.9.13 High-pass filter's response is set by compound current mirrors

The circuit shown in Figure 4.51 functions as a high-pass filter for signals coming from a high-impedance source. It allows one to filter signals based on their slew rate, rather than their frequency, and is best suited as an input stage to a more complex filter. A compound set of current mirrors is used in this design and allows one to adjust the filter's slew-rate response, as well as to alter the signal's baseline voltage level. Being able to zero out any DC errors and offsets, by adjusting or restoring the baseline level, is really helpful. Additionally, being able to filter out the noise or unwanted parts from a signal helps improve the signal-to-noise (S/N) ratio. It allows one to measure and work with those signals with greater precision and accuracy. The voltage at amplifier A_2's V_{REF} input is responsible for this function.

The signal input appears at amplifier A_1's inverting input, is processed, and then is available as a buffered output at amplifier A_3's V_{OUT} pin. The slew-rate cutoff is directly adjustable by changing I_{REF} with the potentiometer R_{POT}, located in transistor Q_2's collector. This current, shown in the diagram as 1 mA, is then mirrored as I_{M1} (mirrored current) and I_{M2}. Current I_{M2} is responsible for charging the capacitor C (47 μF), whose purpose is to retain the baseline voltage setting. This voltage is regulated using feedback from amplifiers A_2 and A_4 and diode D_2, by using currents I_{M2}, I_{M3}, and I_{M4}. If the output voltage at V_{OUT} attempts to rise, the current through diode D_2 is reduced, which in turn reduces the voltage on capacitor C. Alternately, if the output voltage at V_{OUT} attempts to fall, then the current through diode D_1 is increased, which in turn

EX-1006 078
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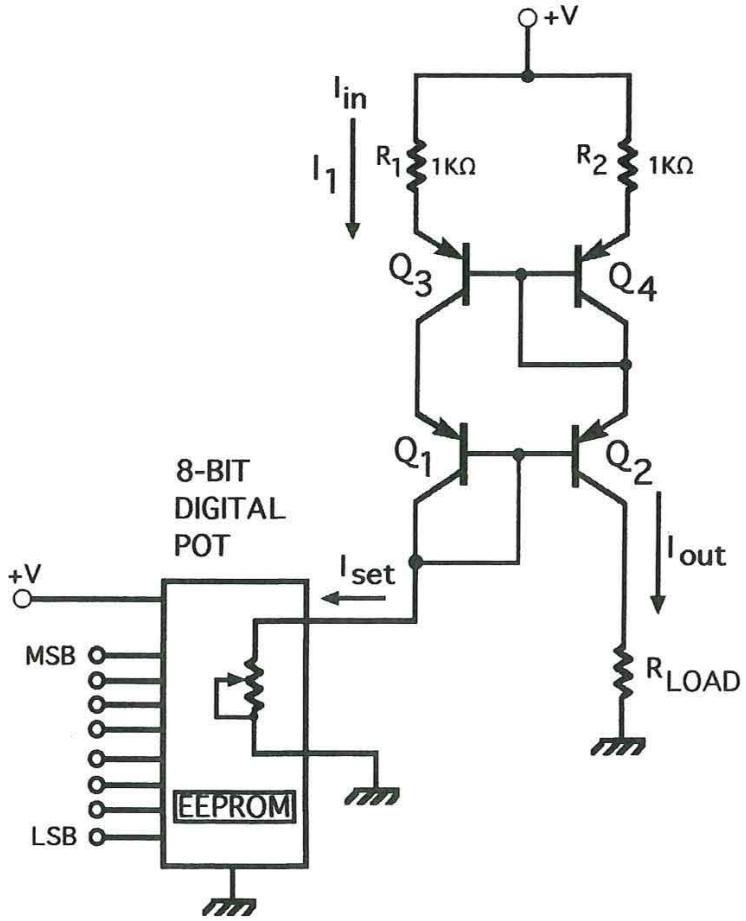


Figure 4.50. Full Wilson current source controlled by a digital pot. The EEPROM retains setting.

increases the capacitor's voltage to the level set by V_{REF}. Thus, it works like a voltage regulator or an AGC circuit.

Transistors Q_3 and Q_4 are part of the Q_1 and Q_2 mirror, but are configured as a current doubler (times two), because the two currents I_{M2} and I_{M3} are combined into I_{M4}, which flows through transistors Q_3 and Q_4. The two currents are required for symmetrical operation on AC signals. The circuit is probably best built using two quad arrays for the current mirrors and two dual op amps. Amplifiers A_1 and A_3 should both be quality precision types, while A_2 and A_4 need to be high-speed types, with a high slew rate (50 V/μS)—in fact, significantly higher than the highest signal frequency being filtered.

EX-1006 079
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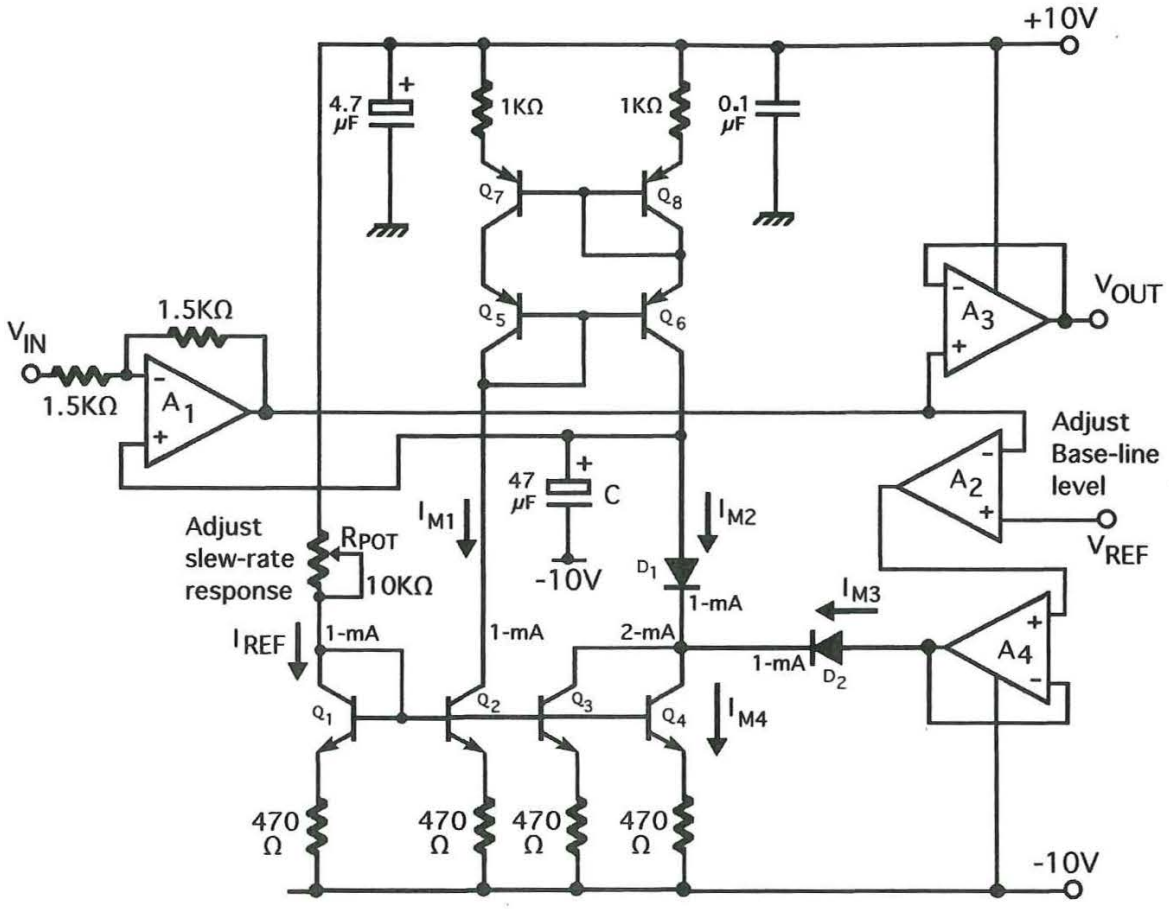


Figure 4.51. Compound current mirrors help tailor this high-pass filter's response.

4.9.14 Simple LED current sources

In Figure 4.52, some simple current sources can be created from the combination of a BJT and a visible red LED. The LED's forward voltage only serves as a voltage reference (not as a normal indicator) and approximately compensates the BJT over the temperature range. This is because the forward voltage of a red LED (V_{FWD} = 1.65 volt) and the forward base-emitter voltage (V_{BE} = 0.65 volt) of a transistor are well known and predictable. This is because of the relationship:

$$\frac{\Delta V_{BE}}{\Delta T} \cong \frac{V_{FWD}}{\Delta T} \cong -2.2mV/°C \qquad \text{(Eq.4.112)}$$

EX-1006 080
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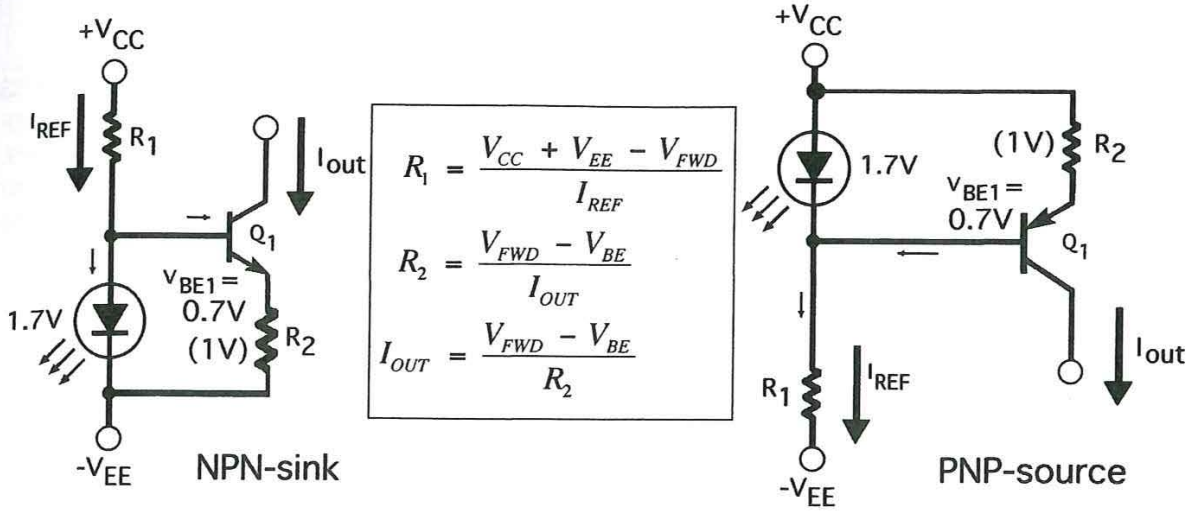


Figure 4.52. Using the forward voltage (V_{FWD}) of a red LED to temperature-compensate the transistor's V_{BE}.

The voltage difference (≈ 1 volt) is dropped across resistor R_2, which in turn provides a temperature-stabilized current at Q_1's emitter. Other color LEDs may be used for the same purposes, but they mostly all have higher bandgap voltages and thus forward voltages as shown in Table 4.4. Of all these the most practical and the cheapest is the standard red type.

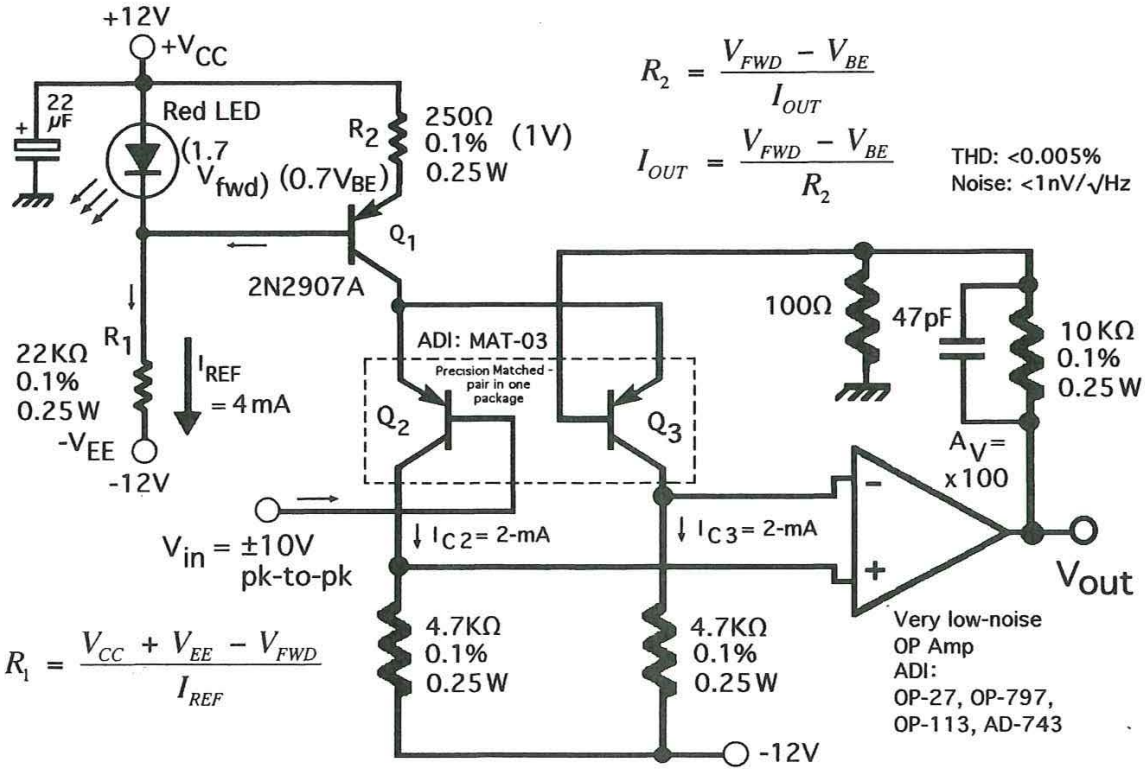
LED COLOR	FORWARD VOLTAGE $V_{(fwd)}$
Infra-Red (IR)	1.40V
Red	1.65V
High-efficiency red	2.20V
Pink	2.00
Orange	2.10
Yellow	2.20
Green	2.20
High-efficiency green	2.30
Blue	3.10
The forward voltage is measured @ 10-mA.	

EX-1006 081
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

Table 4.4 LED color vs. forward voltage.

4.9.15 A low-noise AC amplifier biased by an LED current source

Based on the simple LED-BJT current sources in the previous example, Figure 4.53 shows an LED-PNP current source being used in a dual-supply application and supplying a constant quiescent current to a matched-pair of very-low-noise transistors. The matched-pair forms a front-end amplifier, biased for very-low-voltage noise over the audio range. Each transistor of the matched-pair is biased at 2 mA. Therefore, the current source supplies a total of 4 mA. Using the Analog Devices MAT-03 matched-pair, along with its OP-27 very-low-noise precision op amp, helps reduce the THD for this simple circuit to less than 0.005%, with a noise level of less than 1 nV/√Hz, which is impressive.



Circuit courtesy of Analog Devices, Inc.

Figure 4.53. This simple LED-referenced current source is used at the input stage of this low-noise AC amplifier, where each of the matched transistor pair is fed a constant 2 mA to reduce voltage noise.

EX-1006 082
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4.9.16 A composite BJT-JFET current source with very high output impedance

If you wanted an extremely high output impedance, together with really sharp current regulation, then the circuit in Figure 4.54 would be a good possibility. In this 28-volt avionics circuit, the output current is set at 125 μA, provided by the Full Wilson PNP current mirror at the top, together with a pair of JFETs in a cascoded configuration. The Wilson current mirror provides accuracy and beta-compensation, while the cascoded complimentary JFETs sharpen regulation and boost the output impedance. The circuit's output impedance (g_o) is greater than 5 GΩ, because of the JFET cascode's very low output conductance. In fact, the output conductance for the circuit is about 0.001 μS (1 nSec). A BJT cascode mirror-sink is used, rather than a Full Wilson, because it adds even higher output resistance. The two capacitors are simply for stability, and the output current is determined by R_{SET}, R_3, and R_4. Emitter degeneration is provided by resistors R_1, R_2, R_5, and R_6, which compensate for differences in the NPN transistors' V_{BE}s. This circuit is probably best built using two quad arrays, together with two discrete JFETs, which could be either through-hole or surface-mount components. All resistors should be quality metal-film, one-eighth watt, with a 0.1% tolerance or better.

4.9.17 A composite BJT-MOSFET high-power current source

Although most current sources we have looked at are in the low microamp to low milliamp range, there may be occasions when one needs a power circuit, delivering amps. The circuit shown in Figure 4.55 uses a combination of a JFET current regulator diode (CRD1), NPN transistors, and resistors in order to set the power MOSFET's drain current. CRD1 provides the operating bias for transistor Q_1, irrespective of power supply fluctuations. The transistor is part of a Widlar bandgap voltage reference, whose temperature-stable 1.22-volt output is used as a reference voltage across the power MOSFET's source resistor, R_S. This forces the MOSFET to pass constant drain current irrespective of its drain-to-source voltage. The source resistor should be a precision, low-tempco, wirewound type, with its wattage dependent on the maximum current through it (+30% margin). The three NPN transistors that make up the bandgap voltage reference must be part of a monolithic array (i.e., CA3045, CA3046, MMPQ3904, MMPQ2222A), so that they share the same temperature characteristics. CRD1 was chosen because at 430 μA it has a flat temperature characteristic yielding 0 ppm/°C, and provides a stable operating bias for the NPN transistor, Q_1. As a result, this design provides a stable medium-power (1.22-Amp) current sink. In this design, the power MOSFET uses a TO-220 package, which should be mounted on a good-quality heatsink. In some designs, you may want to consider heatsinking the power resistor too.

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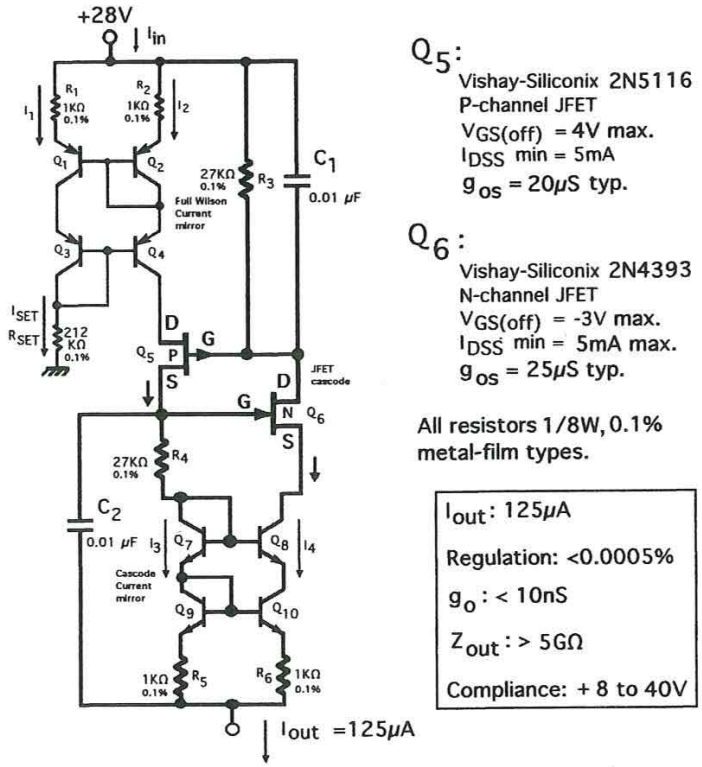


Figure 4.54. Composite cascoded BJT-JFET current source provides excellent regulation and ultra high output impedance.

4.9.18 A DAC-controlled current pump uses a Wilson current source

The circuit shown in Figure 4.56 functions as a bipolar current pump, which both sources and sinks current to the load. This design combines a Basic Wilson current mirror together with an 8-bit multiplying DAC. The venerable industry-standard Analog Devices DAC-08 (8-bit) has complementary current outputs, with a range of ±2 mA full-scale, and having a typical drift of about ±10 ppm/°C. The DAC's digital code ranges from 0000 0000 to 1111 1111, which corresponds to an output current range of –1.992 mA to +1.992 mA. The current source maintains linearity within one LSB (which is 15.6 μA). In this design, the circuit uses split power supplies of ±15 volts and a +10-volt reference voltage. The external voltage reference shown in the diagram as V_{REF} is 10 volts. This sets the I_1 reference current through resistor R_1 at 2 mA. Hence the DAC's outputs range from 0 to +1.992 mA or 0 to –1.992 mA. The processor sends the appropriate digital code to the DAC, whose output current changes to that value. This sets the current mirror's reference current through Q_1. Transistor Q_3 mirrors this current, which is regulated and buffered by Q_2. Diode D_1 matches the V_{CE} across Q_1 and Q_3, keeping the voltage constant across Q_3. Diodes D_2 and D_3 form a Baker

EX-1006 084
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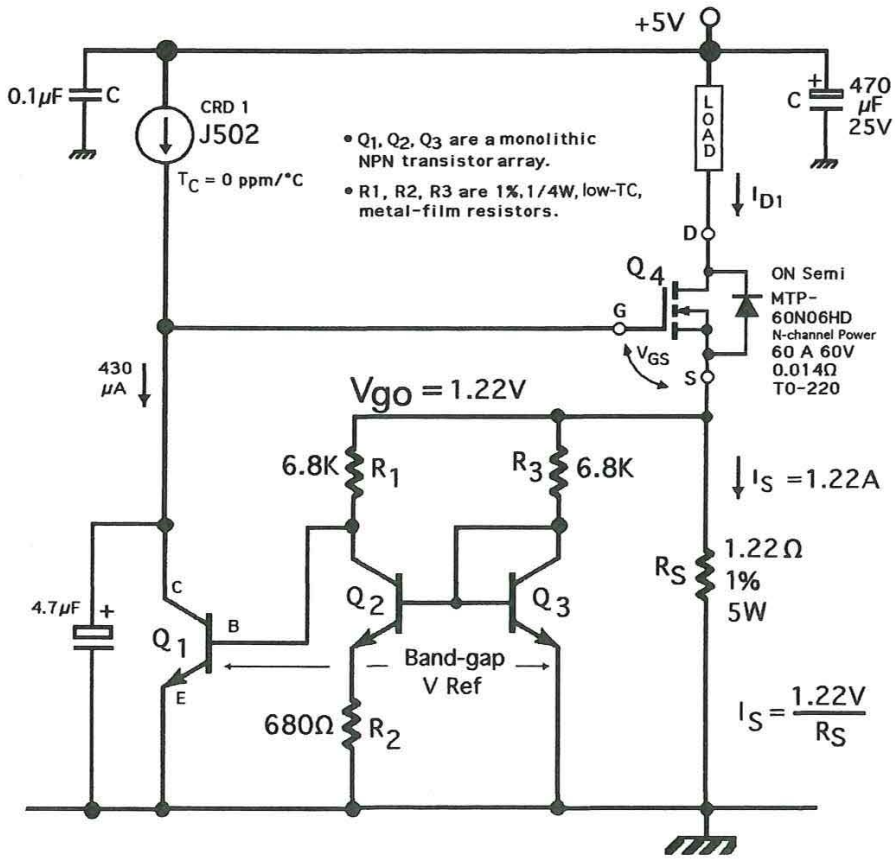


Figure 4.55. *A high-power BJT/Power MOSFET current sink using a Widlar band gap voltage reference for improved temperature stability and current regulation.*

clamp, preventing Q_2 from turning off, and so improving the overall switching speed of the circuit. Because D_3 also serves as a blocking diode between the DAC's output and the load, it is subject to very fast reverse voltages. Although the other diodes shown in the circuit can be regular 1N4148 switching diodes, D_3 should be a fast-recovery diode, such as a 1N4937 or similar (1 Amp; 600 volt; trr = 200 nS).

As you have seen in this chapter, some of the most precise current sources can be built with BJTs. Currents can be easily matched, multiplied, divided, scaled, or inverted in various ways. The best current sources are the Wilson, Widlar, Wyatt, and cascodes. When you consider how far the junction transistor has come since Dr. Shockley invented it in the late 1940s and Bob Widlar showed us how to use it in the '60s and '70s, how it has evolved and changed society, it has to be one of the most useful devices ever invented in the history of humankind. Invented and developed in America, transistors are now made in dozens of countries around the world. The BJT

EX-1006 085
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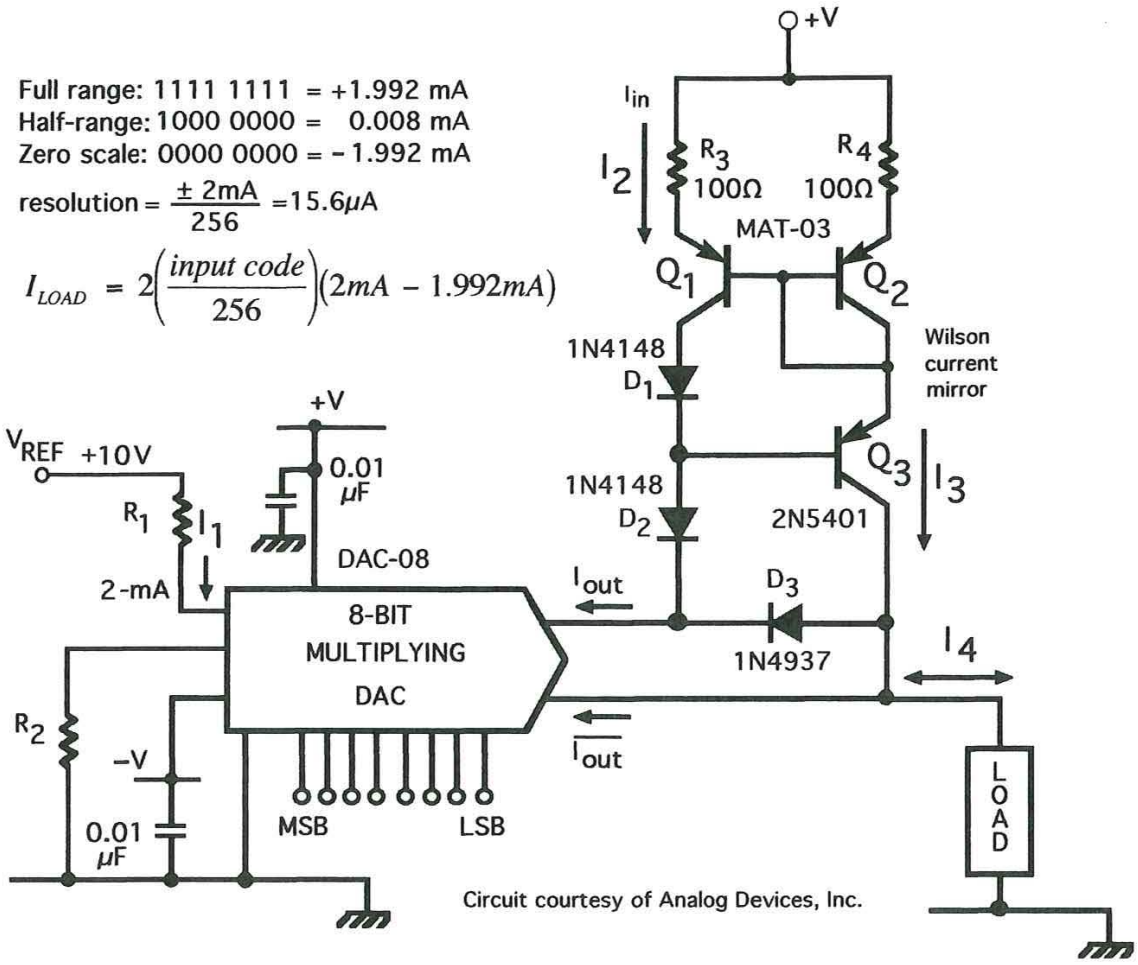


Figure 4.56. A digitally controlled bipolar current pump.

will surely be a major part of our electronics design kit for a few more decades to come, and with it the current source.

EX-1006 086
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Chapter 5

Using Precision Matched-Pairs, Duals, and Quads

5.1 Precision BJT matched-pairs

As we learned from the previous chapter, some of the most accurate BJT-based current sources that the designer can create at the circuit board level use precision matched-pairs and quads. These are available from Analog Devices, National Semiconductor, and second-source specialists Linear Integrated Systems. Precision matched monolithic BJT pairs and quads represent the highest quality and precision available in a silicon transistor. All three manufacturers make NPN matched-pairs. Analog Devices and Linear Integrated Systems also offer PNP matched-pairs. Additionally, Analog Devices makes a quad NPN device. Overall, Linear Integrated Systems provides a wider range of different package options than any other manufacturer. Some of the company's matched-pairs are super-gain transistors (not Darlingtons), with h_{FE}s upward of 1000. Many of the BJT circuits shown in Chapter 4 can be optimized by using any of these high-performance matched-pairs and quads.

What makes precision matched-pairs so special? Unlike dual transistors or multiple transistors that are packaged as an array, matched-pairs have specifications far exceeding those of high-performance discretes or a typical multitransistor array. Precision matched-pairs rely on a specially designed paralleled transistor structure (not unlike today's power MOSFET structure, which also uses many paralleled cells in order to create one single FET device with very low on-resistance). With the precision matched-pair/quad BJT, a similar technique dramatically reduces the base-emitter bulk resistance to levels typically less than an ohm (this resistance is often more than 50 Ω in a regular discrete transistor). They also receive special processing, in order to achieve these exotic characteristics. This includes a multiple passivation process, which stabilizes the important parameters over a wide temperature range, reduces leakage currents, and enhances the isolation between individual transistors. These parameters are also stabilized over a range of collector currents, which typically span from one microamp to several milliamps. Additionally, each transistor is individually tested against its published data sheet specifications over the full operating temperature range, and those characteristics, such as noise levels, gain matching, and offset voltage drift, all come close to matching the specs for the ideal transistor.

To illustrate this concept further, the best NPN matched-pairs have V_{BE}s that are matched to better than 50 μV (referred to as ΔV_{BE} or V_{OS}) and high h_{FE}s that are

EX-1006 087
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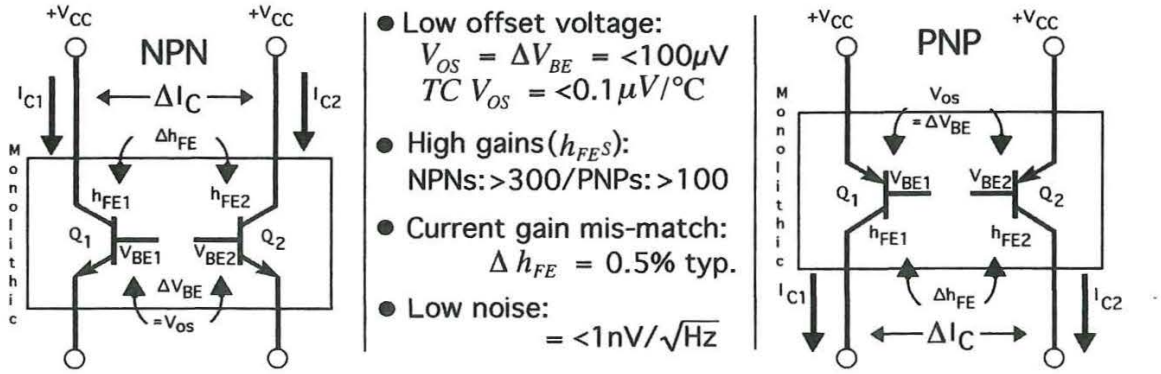


Figure 5.1. An example of excellent transistor matching using precision matched pairs.

matched to better than 0.5%. They have offset voltage drifts of less than 0.1 μV/°C, offset voltage CMRRs ($\Delta V_{OS}/\Delta V_{CB}$) that are better than 120 dB, and ultra-low base-emitter bulk resistance (r_{be}) of less than 0.5 Ω.They also feature very low noise levels, typically less than 1 nV/√Hz (see Figure 5.1). National Semiconductor's venerable LM194/394, for example, has specs that include a typical offset voltage of 25 μV, h_{FE} matching typically 0.5%, offset voltage drift less than 0.1 μV/°C, and a wide operating range of between 1 and 40 volts. Operation is specified at room temperature and over a range of either –55°C to +125°C (LM194) or –25°C to +85°C (LM394).

Analog Devices' MAT02 has specs that even improve on this, over the full military temperature range. In addition, it provides a quad NPN product, the MAT04, as well as lower-cost devices, the SSM2210 (NPN) and SSM2220 (PNP). See Table 5.1 for more specifics. When it comes to high-gain matched PNP pairs, Analog Devices' MAT03 has offsets of 100 μV max, while their lower-cost SSM2220 has offsets of 200 μV max. Unlike discrete PNPs, these devices have good h_{FE}s, as well as very low r_{bes}, and ultra-low noise. Linear Integrated Systems offers higher gain devices, but with higher V_{OS} (i.e., their LS352 has an h_{FE} of greater than 200 and a V_{OS} max of 500 μV). Linear Integrated Systems also offers some useful log-conformance, matched NPN and PNP duals in a choice of several different packages.

Unlike normal discrete or multiple transistors, which often require beta-compensation for h_{FE} mismatches, or emitter-degeneration resistors to compensate for differences in V_{BE}s, precision matched-pairs usually do not. In fact, these types of compensation may be completely eliminated in many applications. Because of their far superior specs, precision matched-pairs are ideal for use as differential input stages for high-gain instrumentation amplifiers, squaring and square root circuits, log/antilog amplifiers, converters, multiplier and divisor circuits, professional audio equipment, and precision current sources. With the exception of Analog Devices' MAT01 (an NPN pair), the other products (i.e., MAT02, 03, 04, and LM194/394) all include internal clamp

EX-1006 088
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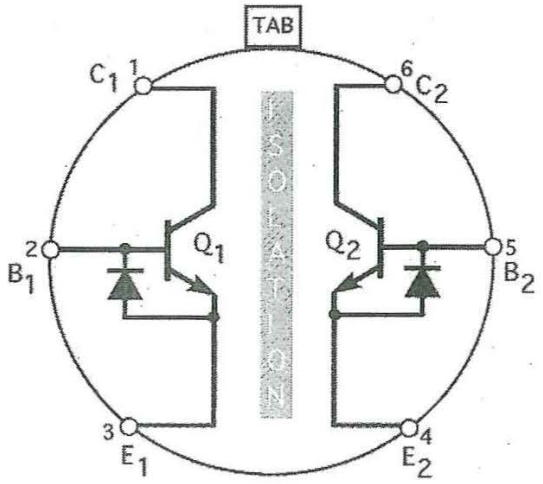


Figure 5.2. *Pin-out for National Semiconductor's LM194/LM394 and Analog Devices MAT02 dual monolithic transistors in a 6-lead, insulated header, metal-can package. Note that the substrate is connected to the case.*

diodes between the emitter and base junction of each transistor (see Figure 5.2). This feature serves a dual purpose: (1) it clamps the substrate to the most negative emitter and ensures complete isolation between the devices, and (2) the diodes help prevent degradation caused by reverse-biased emitter current, which could otherwise cause damage, instability, and drift of some of the key matching parameters.

Being precision devices, these matched-pairs and quads are intended for high-performance instrumentation. One could expect to pay a very high price for this level of quality, but many devices are inexpensive and affordable. Others are aimed at MIL/aerospace-type applications and are priced accordingly. National Semiconductor's LM194 and LM394B/C are available in an isolated header six-lead TO-5 metal can. The LM194 is identical to the LM394 except for tighter electrical specifications and a wider temperature range. Because the LM194 is a military/aerospace device, it is also the most costly of all the precision matched-pairs ($17.50 each), whereas the LM394 devices are considerably less expensive (ranging from approximately $3.30 to $5.20 each).

Analog Devices' MAT01/02/03 products are also available in an isolated header six-lead metal can. The MAT01 costs between approximately $5.60 (GH) to $9.30 (AH) each for 100 pieces. The MAT02, with its improved specs, costs between approximately $6.00 (FH) to $11.65 (EH) each at 100 pieces. The MAT03, the PNP matched-pair, costs between approximately $7.33 (FH) to $13.98 (EH) each at 100 pieces. The MAT04, the NPN matched-quad device, is considerably less expensive and costs approximately $3.95 each at 100 pieces for either the 14-pin DIP (FP) or the SOIC14

EX-1006 089
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(FS) device. The SSM2210 (a matched NPN pair) costs approximately $2.24 each at 1000 pieces in either DIP-8 or SOIC-8 packages. The SSM2220 (a matched PNP pair) costs approximately $2.73 each at 1000 pieces in either DIP-8 or SOIC-8 packages. These prices were shown on both manufacturers' respective Web sites but are applicable to U.S. buyers only.

Mfr.	Part #:	Matched pair/quad	Package options:	V_{os} max μV	TC V_{os} $\mu V/°C$	h_{FE} min	Δh_{FE} Max. %	e_n typ. $nV/\sqrt{Hz}$	Op. temp. range
NS	LM 194H	Dual NPN	1	100	0.3	300	2	1.8	MIL
NS	LM 394H	Dual NPN	1	150	1	200	4	1.8	Ind
NS	LM 394BH	Dual NPN	1	200	1.5	150	5	1.8	Ind
NS	LM 394CH	Dual NPN	1	200	1.5	150	5	1.8	Ind
AD	MAT 01AH	Dual NPN	3	100	0.5	500	3	6.1	MIL
AD	MAT 01GH	Dual NPN	3	500	1.8	250	3	6.1	MIL
AD	MAT 02EH	Dual NPN	3	50	0.3	400	2	0.9	Ind
AD	MAT 02FH	Dual NPN	3	150	1	300	4	0.9	Ind
AD	MAT 03EH	Dual PNP	3	100	0.5	80	3	0.7	Ind
AD	MAT 03FH	Dual PNP	3	200	1	60	6	0.7	Ind
AD	MAT 04FP	Quad NPN	5	400	2	300	4	1.8	Ind
AD	MAT 04FS	Quad NPN	6	400	2	300	4	1.8	Ind
AD	SSM 2210P	Dual NPN	2, 8	200	1	300	5	1.0	Ind
AD	SSM 2210S	Dual NPN	2, 8	200	1	300	5	1.0	Ind
AD	SSM 2210SZ	Dual NPN	2, 8	200	1	300	5	1.0	Ind
AD	SSM 2220P	Dual PNP	2, 8	200	1	80	2	1.0	Ind
AD	SSM 2220S	Dual PNP	2, 8	200	1	80	2	1.0	Ind
LIS	LSIT 120A	Dual NPN	2, 3, 4, 7, 8	400	3	200	2	1	Ind/MIL
LIS	LSIT 130A	Dual PNP	2, 3, 4, 7, 8	400	3	200	2	1	Ind/MIL
LIS	LS 301	Dual NPN	2, 3, 4, 7, 8	1000	5	2000	5	1	Ind/MIL
LIS	LS 302	Dual NPN	2, 3, 4, 7, 8	1000	5	1000	5	1	Ind/MIL
LIS	LS 303	Dual NPN	2, 3, 4, 7, 8	1000	5	2000	5	1	Ind/MIL
LIS	LS 310	Dual NPN	2, 3, 4, 7, 8	1000	2	150	10	1	Ind/MIL
LIS	LS 311	Dual NPN	2, 3, 4, 7, 8	1000	5	150	5	1	Ind/MIL
LIS	LS 312	Dual NPN	2, 3, 4, 7, 8, 9	500	2	200	5	1	Ind/MIL
LIS	LS 313	Dual NPN	2, 3, 4, 7, 8	1000	5	400	5	1	Ind/MIL
LIS	LS 318	Dual NPN #	2, 3, 4, 7, 8	400	5	150	5	1	Ind/MIL
LIS	LS 351	Dual PNP	2, 3, 4, 7, 8	1000	10	150	5	1.5	Ind/MIL
LIS	LS 352	Dual PNP	2, 3, 4, 7, 8, 9	500	2	200	5	1.5	Ind/MIL
LIS	LS 358	Dual PNP #	2, 3; 4, 7, 8	400	5	100	5	1	Ind/MIL

NOTES:
NS = National Semiconductor AD = Analog Devices LIS = Linear Integrated Systems
Package options:
1 = 6-lead, isolated header, TO-5 metal can; 2 = 8-pin plastic DIP; 3 = 6-lead, isolated header, TO-78 metal can;
4 = 6-lead, isolated header, TO-71; 5 = 14-pin plastic DIP; 6 = 14-pin SO; 7 = SOIC-8; 8 = SOT-23/8pin;
9 = SOT-23/6pin; # = Log conformance

Table 5.1 BJT precision matched-pairs and quads.

EX-1006 090
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5.2 Quality dual transistors

There was a time at the beginning of the electronics era (early 1960s) that dual transistors were readily available and were even used to build early modular op amps. Major vendors of the day included Fairchild Semiconductor, Union Carbide, Transitron, and Motorola Semiconductors. Quality dual transistors, unlike most of the general-purpose duals and quads that we will look at next, are matched, but to a lower degree than the ultra-precision devices we looked at previously. They are useful in development work and in lower accuracy applications. These monolithic devices share virtually identical characteristics and are also thermally matched, which is an important factor. As stated previously in Chapter 4, accuracy can always be significantly improved by adding relatively low-value resistors (100 Ω to 1.5 KΩ), inserted in either the uppermost emitters of PNP devices (see Figure 5.3A) or the lowest emitters of NPN devices. They can also be beta-compensated by incorporating a low-value resistor (typically between 22 Ω and 100 Ω) in the base of the reference transistor, Q_1, as shown in Figure 5.3B. In either case, the resistors should be quality metal-film types, ±1% tolerance or better, with a low tempco (less than 100 ppm). Some excellent current sources can be created using quality matched dual transistors, *if* either or both of these two techniques are employed, as shown in Figure 5.3.

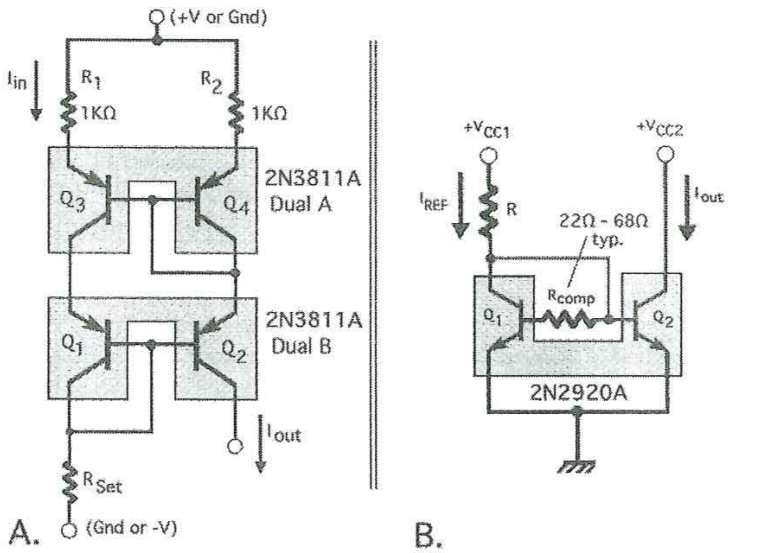


Figure 5.3. Examples showing how to improve matched duals for use as a current source (A) or a current sink (B).

EX-1006 091
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

Quality dual transistors are fairly uncommon, however. Most manufacturers today prefer to offer general-purpose duals and quads, and so do not publish specifications that includes the key matching data between the transistors (such as ΔV_{BE} or V_{OS} max, TC V_{OS}, and Δh_{FE}). Those particular specifications are shown with the precision matched-pairs and quads, and require that each transistor in a pair or quad be individually tested against its published data sheet specs. This adds cost and results in a more expensive device. A quality dual transistor does include most of those specs, although not as high performance (where a ΔV_{BE} might be 500 μV vs. 50 μV for a precision matched-pair). A general-purpose dual/quad does not include those specs at all. Two manufacturers that do make quality matched dual transistors are Central Semiconductor and Linear Integrated Systems. Notice the key matching specifications, ΔV_{BE} and Δh_{FE}. Table 5.2 shows some of these products.

Mfr.:	Part #:	Dual/quad NPN/PNP	Package options:	V_{CBO} (V)	I_C (mA)	f_t min (MHz)	h_{FE} min	Matching Δh_{FE} max. %	Matching ΔV_{BE} max. (mV)
CS	2N2915A	Dual NPN	1	45	30	60	60	10	1.5
CS	2N2916A	Dual NPN	1	45	30	150	60	10	1.5
CS	2N2919A	Dual NPN	1	60	30	60	60	10	1.5
CS	2N2920A	Dual NPN	1	60	30	60	150	10	1.5
CS	2N3727	Dual PNP	1	-45	-300	200	135	10	2.5
CS	2N3810A	Dual PNP	1	-60	-50	100	150	5	1.5
CS	2N3811A	Dual PNP	1	-60	-50	100	100	5	1.5
CS	2N4016	Dual PNP	1	-60	-300	200	135	10	2.5
LIS	IT124 *	Dual NPN	1,2,3,4	2	10	100	1500	10	5
LIS	LS301 *	Dual NPN	1,2,3,4,5	18	5	100	2000	5	1
LIS	LS302 *	Dual NPN	1,2,3,4,5	35	5	100	1000	5	1
LIS	LS303 *	Dual NPN	1,2,3,4,5	10	5	100	2000	5	1
LIS	LS310	Dual NPN	1,2,3,4,5	25	10	200	150	10	3
LIS	LS311	Dual NPN	1,2,3,4,5	45	10	200	150	5	1
LIS	LS313	Dual NPN	1,2,3,4,5	45	10	200	400	5	1
LIS	LS351	Dual PNP	1,2,3,4,5	-45	-10	200	150	5	1
LIS	LS3250A	Dual NPN	1,2,3,4,5	45	50	600	150	10	2
LIS	LS3250B	Dual NPN	1,2,3,4,5	40	50	600	100	10	5
LIS	LS3550A	Dual PNP	1,2,3,4,5	-45	-50	600	150	10	2
NS	LM3046M	5 x NPN #	6	20	50	>100	>50	10	5

NOTES: CS = Central Semiconductor LIS = Linear Integrated Systems NS = National Semiconductor

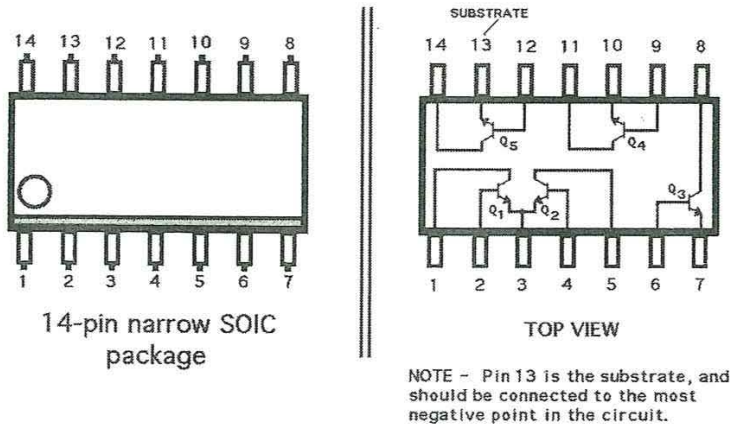
Package options:

1 = 6-lead, TO-78 metal can; 2 = 6-lead, TO-71 metal can; 3 = 8-pin plastic DIP; 4 = SOIC-8;

5 = SOT-23/6-pin ; 6 = SOIC-14 * = super-beta, v.low-voltage type # = 3 x NPN + a differential pair

Table 5.2 Closely matched dual NPN and PNP transistors.

EX-1006 092
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.



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Figure 5.4. *National Semiconductor LM3046M, a 5 × NPN transistor monolithic array, with matched V_{BE}s.*

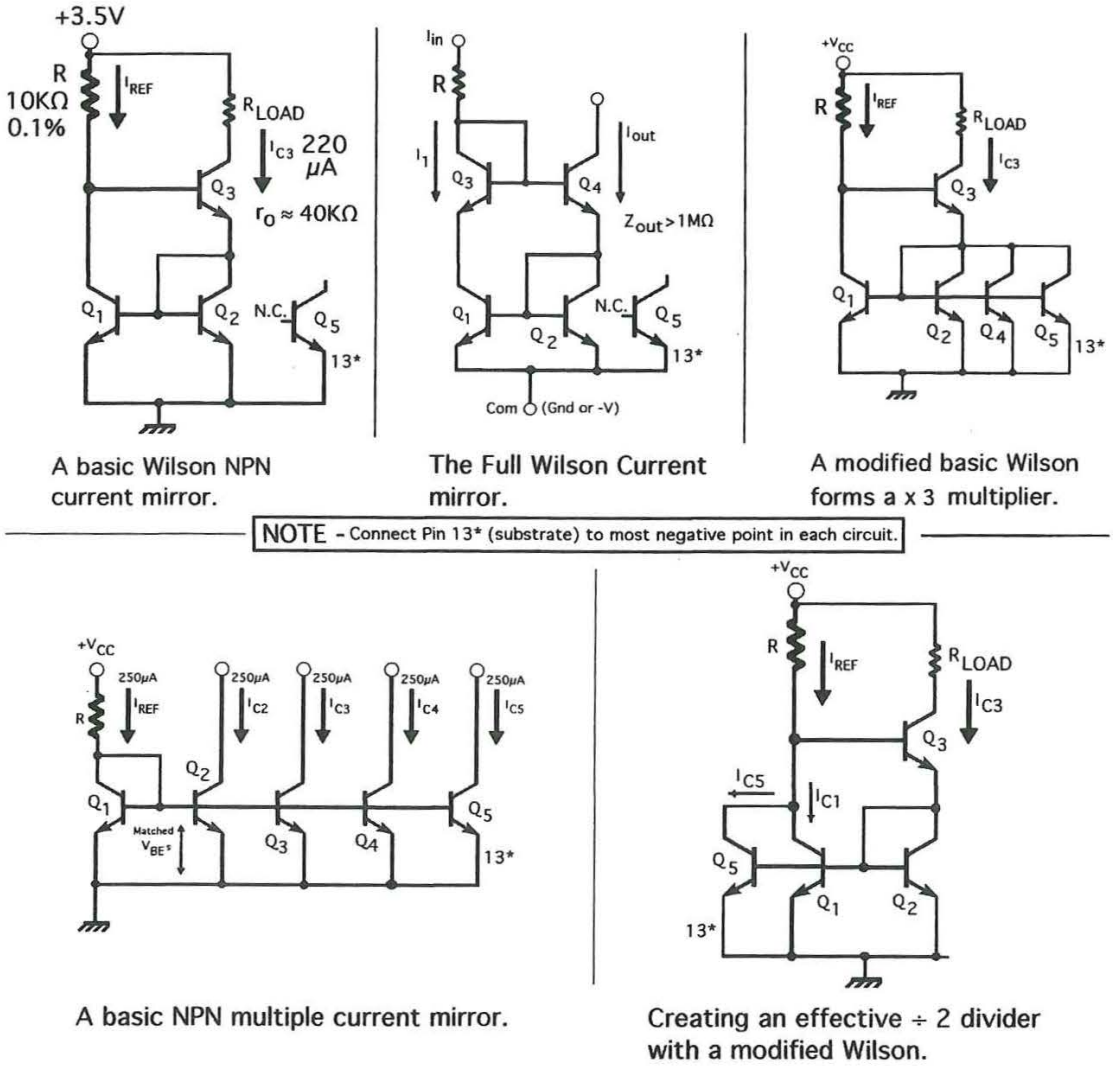
Back in the 1970s and early '80s, RCA Solid State developed and introduced a product line in dual-in-line packages, known as the CA-3000 series. These became the forerunners of most other BJT arrays/hybrids from various companies and were used mostly in front-end amplifier applications. (RCA was after all primarily a TV/radio manufacturer, and so the line was probably developed for use in such equipment.) Some devices were second-sourced by Motorola's Semiconductor Group and National Semiconductor, among others. When RCA's discrete and analog portfolio was sold off to Harris Semiconductor, it too made them. Today, however, they are no longer available, which is a pity because some of the products were closely matched and could easily be used for current source applications (e.g., CA3018A and CA3146 both had a maximum ΔV_{BE} of only 2 mV). Only National Semiconductor continues to produce one of those products, the LM3046 (a 14-pin SOIC shown in Figure 5.4), which contains an NPN differential pair as well as three general-purpose NPNs.

Although at first glance only the differential pair appears to have matched V_{BE}s, actually when one examines the data sheet carefully, all five transistors have their V_{BE}s matched to within ±5 mV of one another (typically 0.45 mV), and can therefore be used to create some inexpensive current sources. Because the device has a maximum collector current rating of 50 mA for each transistor, typical current (sink) levels can range from about 2 μA to about 10 mA, without heat dissipation becoming a major factor.

In some volume applications that may be noncritical or require only medium accuracy, the LM3046M can be useful, particularly because it is a surface-mount package. The best part is that the U.S. price at 1000 pieces is $0.45 each, which is extremely economical. Figure 5.5 shows some common current-sink designs that can be built using

EX-1006 093
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

the device. Because of its NPN format, these all take the form of common mirror-sinks, multipliers, dividers, as well as the ever-popular Wilson designs. Remember, though, that in any design using this device it is *very important* to always tie pin 13 (the substrate) to the most negative point in one's circuit, because the collector of each transistor in the package is isolated from the substrate by an integral diode. As a result, the substrate should be connected to the most negative point in the external circuit, in order to maintain isolation between the different transistors and to ensure normal operation.



A basic Wilson NPN current mirror.

The Full Wilson Current mirror.

A modified basic Wilson forms a x 3 multiplier.

A basic NPN multiple current mirror.

Creating an effective ÷ 2 divider with a modified Wilson.

Figure 5.5. LM3046M current source applications.

EX-1006 094
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

5.2.1 General-purpose BJT duals and quads

Today various general-purpose BJT duals and quads are readily available in the marketplace. Although most are not critically matched to the same degree as we have seen up until now, they are (usually) built with adjacent die from the same wafer and so are at least thermally matched. (Devices of the same type, but from different wafers, may be regarded as hybrids and are not a good choice for using in current source designs. They would be only slightly better than using random discrete transistors, which we have learned previously are not a good choice.) Therefore, general-purpose BJT duals and quads are useful in development work or in noncritical or low-accuracy applications, but remember that because these products are not matched, they will require V_{BE} and/or h_{FE} compensation for any semiprecision current source designs.

Dual transistors are available from Central Semiconductor, Crystalonics, Diodes Inc., Fairchild Semiconductor, Linear Integrated Systems, Microsemi, ON Semiconductors, Philips Semiconductors, and Vishay Semiconductors. They are available in different packages, including surface-mount, and in different temperature ranges. The largest makers of duals include Central Semiconductor, Fairchild Semiconductor, and Linear Integrated Systems. Crystalonics makes various former and discontinued Motorola Semiconductor parts, including some that are MIL/JAN-qualified devices. Microsemi also offers an impressive range of MIL/JAN-qualified devices in various packages. Common dual transistors offered by several manufacturers include 2N3811, IT130, and 2N4937 (all PNP pairs), as well as 2N2920, IT120, and 2N5794 (all NPN pairs). Table 5.3 gives an overview of the manufacturers and the types of products they offer.



Figure 5.6. *Just a few of the packages that have been used for the popular 2N3906, which include metal, plastic, and surface-mount types.*

EX-1006 095
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

Manufacturer:	Ultra-precision, matched duals and quads			Matched duals and quads			General purpose duals and quads		
	Metal-can /leaded	DIL/ leaded	Surface-mount	Metal-can /leaded	DIL/ leaded	Surface-mount	Metal-can /leaded	DIL/ leaded	Surface-mount
Analog Devices	√	√	√						
Central Semiconductor				√		√	√		√
Crystalonics							√	√	√
Diodes Inc.									√
Fairchild Semiconductor									√
Linear Int. Systems	√	√	√	√	√	√	√	√	√
Microsemi							√	√	√
National Semiconductor	√					√			
ON Semiconductor								√	√
Philips Semiconductors								√	√
Vishay Semiconductors								√	√

NOTES:

1. Ultra-precision matched devices are specified on their data sheet with ΔV_{BE}, Δh_{FE}, and TC_{VOS}.
2. Matched devices are specified on their data sheet with ΔV_{BE}, and /or Δh_{FE}.
3. General purpose devices do not have ΔV_{BE}, Δh_{FE}, or TC_{VOS} specified on their data sheet.
4. Some devices in all three categories are qualified to MIL/JAN standards.
5. Some general purpose quads are complementary, containing both a pair of NPN and PNP transistors.

Table 5.3 Manufacturers of dual and quad BJT transistors.

Quad transistors are available from Fairchild Semiconductor, Central Semiconductor, Crystalonics, ON Semiconductor, Diodes Inc., Microsemi, and others. Most products contain either all-NPN or all-PNP devices. Some examples include the PQ-3904 (four NPNs with similar specs to a 2N-3904) and the PQ-3906 (four PNPs with similar specs to a 2N-3906). Some are dual-complementary (two NPN and two PNP in the same package), such as the PQ-6002 and the PQ-6502 (two NPNs and two PNPs with specs based on 2N3904/3906), which can provide a simple current source and current sink in one package. A sample of some of these various devices are listed in Table 5.4.

In summary, some of the best and most accurate current sources that can ever be created at the circuit board level use well-proven BJT technology. Monolithic matched-pairs and quads represent the highest quality and precision available, while lower-priced matched-duals can also produce some excellent current sources. Even general-purpose duals and quads can produce good, stable current sources, so long as one remembers to include the necessary compensation. For many engineers designing with BJTs, with which they are more familiar, is easier than with other technologies. This will probably remain so for a long time to come.

EX-1006 096
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.

Part No.:	NPN/ PNP/ Comp.	Dual	Quad	V_{CEO} min (V)	V_{CBO} min (V)	I_C max (mA)	I_{CBO} max (nA)	h_{FE} min @ 1mA	F_T min (MHz)	
2222/A	NPN	√	√	40	75	1000	10	50	300	
2369	NPN		√	15	40	200	400	40		
2484	NPN		√	40	60	50	20	300	50	
2907/A	NPN	√	√	60	60	800	20	100	200	
3799	PNP		√	-60	-60	-50	20	200	60	
3904	NPN	√	√	40	60	200	50	70	300	
3906	PNP	√	√	-40	-40	-200	50	80	250	
5401	PNP	√		-150	-160	-200	50	50	100	
5551	NPN	√		160	180	200	50	80	100	
6002	Compl		√	30	60	500	30	50	200	
6502	Compl		√	30	60	500	30	50	200	
6600	Compl		√	45	60	50	10	150	50	
6700	Compl		√	40	40	200	50	50	200	
7043	NPN		√	250	250	500	100	25	50	
7051	Compl		√	150	150	500	100	25	50	
7093	PNP		√	-250	-250	-500	250	25	50	
BC846	NPN	√		65	80	100	15	150	100	
BC847	NPN	√		45	50	100	15	150	100	
BC848	NPN	√		30	30	100	15	150	100	
BC856	PNP	√		-65	-80	-100	15	150	100	
BC857	PNP	√		-45	-50	-100	15	150	100	
BC858	PNP	√		-30	-30	-100	15	150	100	

NOTES:

1. The numeric part numbers shown above are "generic". For example the "3906" may be prefixed with alpha characters such as "2N/PN-3906" (single),"FMB-3906" (a dual), or "MMPQ-3906" (quad). In addition to identifying the manufacturer, and type (dual or quad), the prefix often denotes the package type. For example, "MMPQ-2907A" is a quad PNP in a SOIC-16 package, while "FMB-2907A" is a dual PNP in a SOT-6 package, and "FFB-2907A" is a dual PNP in a SC-70 package.
2. The devices listed are available from multiple sources, and in various different packages.
3. "Comp" shown in column 2, denotes a complementary pair. The quad devices shown contain a pair of NPN and a pair of PNP devices. One such quad may be used to build a simple current source and sink.

Table 5.4 Common transistors available as dual and quads.

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