



Circuits, Devices and Systems Series 2

Analogue IC Design

The Current-Mode Approach

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Bipolar Current Mirrors

Barrie Gilbert

6.1 Introduction - The Ideal Current Mirror

Few readers of this book will need to be introduced to the concept of the current mirror; it has become a familiar icon of modern analog design. Accordingly, we will deal only briefly with the well-established foundations of the subject, already adequately presented in many excellent texts^[1], and concentrate instead on developments of the basic current-mirror forms, having properties suited to special, though not uncommon, applications. Some of these developments have been included only to illustrate the wide variety of possibilities, and may not have any immediate practical value; this is true of the high-ratio forms presented in Section 6.5.2.

In principle, the basic function could have been realized before the advent of the bipolar junction transistor (BJT), but the unique properties of this device opened the door to efficient and eminently practical forms of mirrors, now to be found in a large proportion of analog ICs (and in many digital ones, too). The design approach used here is based strongly on the translinear view of the BJT. In many cases, this will mean the invocation of strict-TL forms of which the classical current mirror is the simplest possible example. Just as probable, however, will be a strong dependence on the basic translinearity of the BJT, that is, the predictable behavior of many special-purpose current mirrors will frequently hinge on the unique relationship between collector current, I_C , and base-emitter voltage, V_{BE} ; they are “TN” circuits, although not always “TL” (see Chapter 2).

Current mirrors find endless uses not only in biasing applications of low to moderate accuracy, where their high output impedance makes them valuable as good approximations to ideal current sources. More complex mirrors provide special capabilities, such as high accuracy over many decades of current, exceptionally high output resistance, very low or high transfer ratios, and so on. Depending on how broad is one’s definition of a “current mirror”, the term can also embrace various types of useful nonlinear behavior and temperature shaping; we will certainly want to examine these important aspects of current-mirror design. Mirrors are also employed as broadband signal conveyors (as, for example, in current-mode amplifiers, described in other chapters of this book). We shall therefore spend some time examining the noise performance of common mirrors. A thorough discussion of dynamic behavior (AC gain and phase, and large-signal

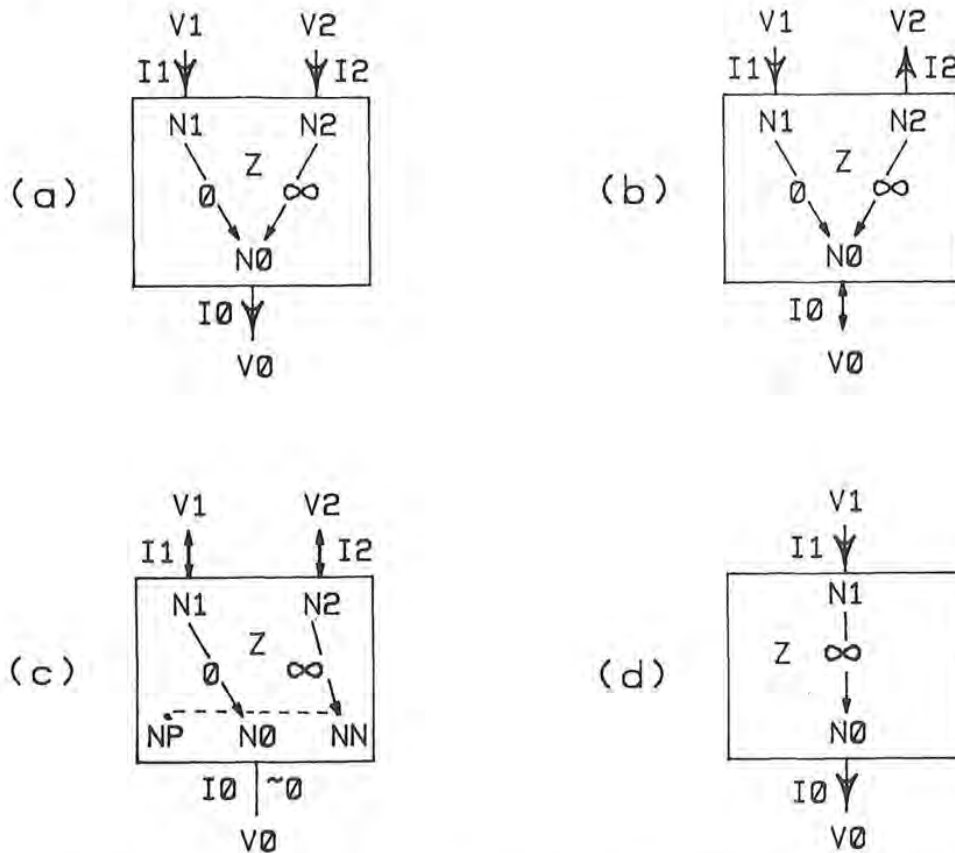


Figure 6.1 Generalized forms of (a) current mirror (b) current reflector (c) current conveyor and (d) current source.

transient response) is not included here, since it is a large topic in itself, and dependent on numerous details which lie beyond the scope of this brief survey of useful topologies. However, where appropriate, some aspects of dynamic behavior will be mentioned.

The simplest current mirror is a three-terminal device, Figure 6.1a, having an input node, N1, capable of accepting a current, I_1 , of only one polarity, an output node, N2, into which a replication, I_2 , of the input current flows in the same direction, and a common node, N0, in which the sum of the input and output currents flow. For now, we will assume the basic mirror to be built with NPN transistors; obviously, the polarity of bias voltages and direction of current flow will be reversed for PNP types. A practically-useful mirror is characterized by three desiderata, listed roughly in order of importance:

- 1) The current I_2 in the output branch should be essentially independent of the voltage V_2 on node N2, which may be biased at any potential from a

few hundred millivolts above the common node to many volts above it; that is, the incremental output resistance¹, r_o (more generally, impedance, z_o) should be relatively high, ideally infinite.

- 2) Both the large-signal mirror ratio, $M = I_2/I_1$, and the small-signal ratio $G=DI_2/DI_1$, should be essentially independent of the magnitude of the currents over many decades; that is, the ideal mirror is a *linear* element (so G/M). In signal-path applications, the gain magnitude and phase response should be benign functions of frequency, ideally, completely independent of it.
- 3) The DC voltage, V_1 , at the input node N1 should be small (say, within a few hundred millivolts of the common node) and it, and any AC voltage generated at this node, should be essentially independent of the input current, I_1 ; that is, the input resistance, r_i , (more generally, impedance, z_i) should be relatively low. In a formal context, it might be convenient to define an ideal mirror as one having an input impedance which approaches zero, but in practice this is rarely as important as achieving a near-zero output admittance (item 1).

We shall see that it is possible to design mirrors in which one or more of these characteristics can be highly refined. Frequently, such optimization is at the expense of other properties. For example, in directing attention to improving output resistance, the input resistance often has to increase. The particular way in which a mirror is optimized depends, of course, on the application. In many bias applications, for example, the emphasis will be on maintaining the highest possible output impedance (both the conductance and capacitance may need to be minimized): the input characteristics are less important here. On the other hand, in signal-path applications, it will often be found that quite high output conductances can be tolerated, while the input impedance (the reactive part often containing both capacitive and inductive components) must be minimized.

6.1.1 Mirrors, Reflectors, Conveyors, Sources

Before proceeding, it will be useful to compare the general properties of the current mirror with other cells having similar properties. The term “current reflector”, for example, is sometimes applied to a three terminal network (Figure 6.1b) which satisfies all of the basic criteria for a mirror, but in which the direction of the output current is reversed². However, this

¹Lower-case variables are used here to denote small-signal parameters.

²The terms “mirror” and “reflector” invite comparison with their optical counterparts. In conventional ray tracing, the direction of the ray is shown as reversing at the reflection surface.

terminology is not standardized. As signal-path cells, the mirror is an inverting stage while the reflector is non-inverting; a folded cascode can be viewed as a reflector. Current conveyors, dealt with at length in Chapter 3, can be viewed as a special kind of “double-mirror” capable of both sinking and sourcing currents at input and output. Figure 6.1c depicts an ideal current conveyor. Nodes N1 and N2 can now accept and deliver currents of either polarity. The voltage at N1 closely follows that at N0; little (ideally zero) current flows in N0. In practice, two extra terminals, NP and NN are required to provide biasing and a source of positive and negative current to the output. Many of the techniques for improving the performance of current mirrors to be described in this chapter can be applied to current conveyors.

Finally, Figure 6.1d shows a floating current source, which requires only two terminals. Since there is no external control of the current magnitude, sources of this kind are generally only used in DC biasing applications³. While it is perfectly possible to design two-terminal current-source circuits, it is customary to utilize three-terminal controlled sources because of the simplicity (particularly, as is often the case, when multiple sources are required) and flexibility they afford. Current mirrors are widely used in such applications, although where the emphasis is on current *generation* rather than *replication* even simpler circuits often suffice. Some transducers generate current-mode signals directly (such as photodiodes), but most signals, and all accurate fixed references, are in the form of voltages, requiring voltage-to-current (V/I) conversion. This is a large topic, and there have been some interesting developments, particularly in the field of wideband V/I conversion, in recent years. However, it is beyond the scope of the present discussion, which for the most part assumes that we are dealing with variables (bias levels and signals) which are already in the form of currents. Section 6.5.3 will show some simple techniques for V/I conversion.

6.2 One-transistor Mirrors

In the simplest possible scenario, a single BJT can be used as a mirror: node N1 (of Figure 6.1a) is the base, N2 the collector and N0 the emitter. Of course, the practical objection to this proposal is that the mirror ratio, M , is much higher than generally needed and poorly-controlled, being just the common-emitter current-gain, β , and not very linear. While these objections are all true, it is nevertheless useful to begin here, because we will discover that many of the properties of more familiar mirrors can be predicted from the behavior of the single transistor circuit.

Figure 6.2a shows the biasing for an NPN device. We wish to determine

³It is worth mentioning, however, that two-terminal current-source circuits can be devised in which the current is a function of some environmental factor, such as temperature.

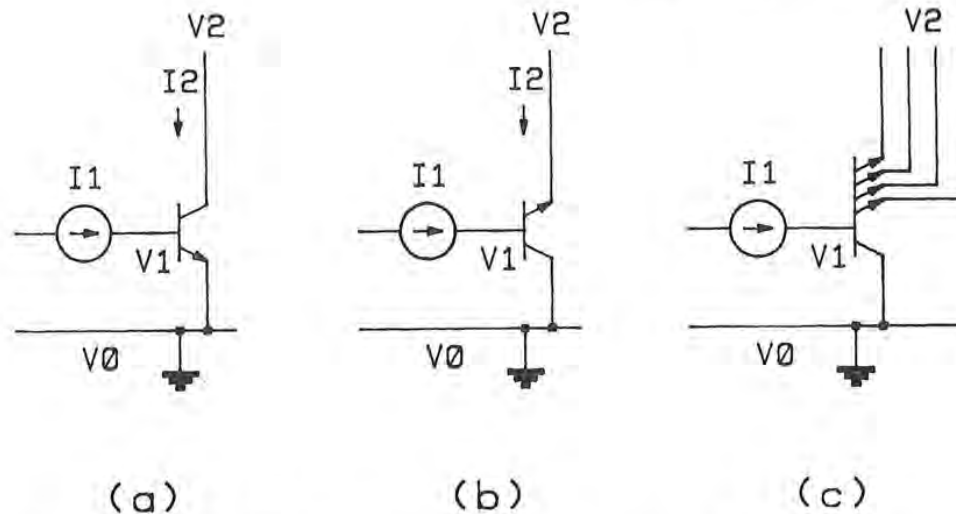


Figure 6.2 Single NPN transistor used as a rudimentary mirror; (a) usual forward active mode (b) inverse-mode (c) multiple outputs from inverse-mode transistor.

the input and output resistances. It will be assumed that β is independent of current over the range of interest. If β were also independent of V_2 , the output I_2 would always be simply βI_1 and the output resistance r_o would be infinite. In fact, β increases with V_2 due to base-width modulation, and in the customary BJT model would be exactly doubled⁴ when the collector bias voltage, V_{CB} (roughly, V_2), is equal to the forward Early voltage, V_{AF} .

It is important to note that for an ideal BJT operating at a fixed base current (I_1 in this case) V_{BE} does not vary *at all* with the collector voltage V_2 , surprising as that may seem. It follows that if we were to replace the fixed current drive I_1 with a fixed *voltage* drive precisely equal to $V_{BE(I_B=I_1)}$ the output would vary in exactly the same way with V_2 , and a constant current $I_B=I_1$ would flow in the base. To model this, the collector current can be written

$$I_C = I_2 = (1 + V_{CB}/V_{AF})I_{2(V_{CB}=0)} \quad (6.1)$$

Thus, the output resistance, near $V_{CB} \approx 0$, is unaffected by whether the base is current- or voltage-driven, and is simply

$$r_o = V_{AF}/I_2 \quad (6.1a)$$

For a transistor having some fixed but general value of V_{BE} , and having any beta (even *infinite*), we will find that Eq. 6.1 still applies, when the

⁴Indeed, one can usefully define V_{AF} as that value of V_{CB} which exactly halves the base width, thus doubling the collector current for a given base charge.

expression

$$I_C = I_2 = (1 + V_{CB}/V_{AF}) I_S(T) \exp(V_{BE}/V_T) \quad (6.1b)$$

is more appropriate⁵. Here, $I_S(T)$ is the “saturation current” for the device, typically 10^{-16} A, and $V_T = kT/q$ is the thermal voltage, approximately 26mV at $T=300$ K.

To trace the improvement in the design of current sources as we progress, it will be useful to assign bench-mark values to some of the parameters of a hypothetical “standard BJT” and the operating conditions. Thus, let V_{AF} be 100V, β_0 (the value of β at $V_{CB} = 0$ and also at zero frequency) be 100, the mirror’s output current, I_2 , be 1mA and the temperature, T , be 300K. Then, this primitive mirror has a calculated output resistance of 100k Ω . At low values of V_2 , r_o may fall due to quasi-saturation effects. When V_2 is less than V_{BE} (that is, the transistor enters saturation) the output resistance falls suddenly; thus, the lower limit on V_2 is about 200mV above the common node. At high values of V_2 , r_o may again diminish, due to the onset of avalanche multiplication in the collector. The absolute upper limit on V_2 is constrained by the BV_{CEO} of the transistor. These effects and limitations are found, to a greater or lesser extent, in fully-developed current mirrors.

As well as being poorly defined, the mirror ratio M is a function of V_2 . This raises an aspect of current mirror behavior which may be overlooked: not only does the output node exhibit a finite resistance, but the *small-signal gain*, G , varies with V_2 , being in this case β_0 at $V_2 = V_{BE}$ and, for example, $2\beta_0$ at $V_2 = V_{BE} + V_{AF}$. Beta is also a function of current and temperature.

The small-signal input resistance r_i is $\Delta V_1/\Delta I_1$, which in this case is the incremental emitter resistance $r_e = \Delta V_{BE}/\Delta I_2$ multiplied by β_0 , that is, $\beta_0 V_T/I_2$. Stated in terms of the input current, $r_i = V_T/I_1$, independent of beta. For $I_1=10\mu$ A, r_i is about 2.6k Ω . The incremental input resistance is often of less significance than the absolute variation in input voltage over the current range: following classical junction behavior, this varies by roughly 18mV for a 2:1 change, or 60mV for a decade change, in I_2 .

Uncontrolled mirrors of this sort are rarely used, although there are special applications in monolithic design where the beta-dependence of output current can be of value in compensating for the base current of other transistors in the circuit. An indirect example is the input bias-current cancellation scheme for an op-amp, described by Laude^[2].

In some cases, an inverted transistor can be used as a single-transistor mirror (Figure 6.2b). This approaches the behavior of a more typical current mirror, having a much lower, and more predictable, value of M , which is now the inverse beta, typically ranging from less than 1 to rarely more than 10, depending on the fabrication process and device geometry.

⁵For simplicity, we will uniformly assume that $\exp(V_{BE}/V_T - 1)$ and $\exp(V_{BE}/V_T)$ are essentially equal for most practical values of V_{BE} (see Chapter 2).

Within any given process, inverse beta has a much narrower range of values, typically varying by less than $\pm 20\%$ for all production lots under given operating conditions, and often as close as $\pm 3\%$ for all devices within a circuit, thus allowing fairly predictable design. V_2 must not exceed the open-base emitter-collector breakdown voltage, BV_{ECO} , typically 6V. Many modern circuits operate from a single 5V supply, so this need not be a serious shortcoming. An example of the use of an inverted transistor as a near-unity-gain mirror is found (as an incidental feature of the output-stage design) in a voltage-to-frequency converter described by Gilbert [3].

The output resistance r_o is now V_{AR}/I_2 , where V_{AR} is the inverse Early voltage, typical values being 2 to 10V. Since this is very much lower than V_{AF} , the output resistance is correspondingly lower than for normal-mode operation. However, the output capacitance of this rudimentary mirror is very low, being just C_{JE} , whereas the normally-operated device has an output capacitance of $C_{JC} + C_{JS}$. It is usually possible to realize a factor of at least ten in the reduction of the output capacitance. This may commend the use of inverted transistors as current sources in biasing applications of high-frequency circuits. For example, in biasing a differential pair, the capacitance at the common emitter node may be troublesome in creating a nuisance pole in the open-loop transfer function, sometimes called the "tail-pole" [4]. In such cases, the inexact value of the bias current may be more tolerable than the high capacitance of a standard current source. One further advantage of the inverted-mode operation is that it is an easy matter to create multiple current outputs from a single multi-emitter transistor (Figure 6.2c). This consumes very little chip area, because only a single collector region is needed and each additional emitter may require only 100 or 200 square microns including its surround. When carefully designed, the matching between these currents can be surprisingly good - typically within $\pm 1\%$. The effective value of the mirror ratio depends on the number of emitters and the particular geometry; the interested reader should consult the classical literature on I²L design, which uses NPN transistors in the inverse mode [5, 5a].

6.2.1 Single-Transistor Mirrors Using Lateral PNPs

Many junction-isolated IC processes are limited by the unavailability of a high-performance isolated-collector PNP transistor, and recourse to the lateral PNP is necessary for mirrors which source current from the positive supply. Later, we will discuss accurate mirrors using these devices, but at this point we will mention briefly some special aspects of lateral PNPs that affects their use as current sources.

The lateral PNP is often treated as a very poor relative in monolithic design texts. True, it has poor frequency response, begins to suffer from high-level injection effects at much lower currents than an NPN transistor, and exhibits other non-ideal aspects. Nevertheless, when used creatively, this device often provides very adequate performance in biasing applications, and

can even have advantages over fully-isolated vertical PNP transistors in some cases. Its structure can be found in most standard texts on monolithic design, but certain important peculiarities of its behavior are rarely discussed. For example, it is often said that the beta of a lateral PNP is quite low. In fact, in a well-controlled fabrication process, the *low-current* gain can be as high as that of the NPN transistor; values of 200-300 at $I_C = 1\mu\text{A}$ are not uncommon. However, due to the low doping concentration in the epi-layer, which forms the base of a lateral PNP, its beta is a very strong function of current, since the injected carriers modulate the effective base doping and thereby reduce emitter efficiency. This is simply the nature of high-level injection, the effects of which begin to be felt at about 1mA for a typical minimum-geometry NPN, but at current of perhaps one-hundredth of this for a lateral PNP. It can be shown that in *high-level injection* its large-signal beta, $\beta(I_C) = I_C/I_B$, is more appropriately specified, not as a constant, but as a function of the collector current and a parameter which will be called the “beta scaling current”, I_{BS} , such that

$$\beta(I_C) = I_{BS}/I_C \quad (6.2)$$

For a typical structure, I_{BS} is about 10mA, and is surprisingly stable over production lots, being traceable to the doping profile, device geometry, and other well-controlled parameters. I_{BS} is only a weak function of temperature. Thus, the beta would have a reliable value of one at $I_C=10\text{mA}$, ten at $I_C=1\text{mA}$ and so on. Collector currents of devices having their emitter-base junctions in parallel, and driven by a single source of I_B , or driven independently, will exhibit good matching, even though the V_{BE} is not “classical”, increasing by much more than 60mV/decade in the high-injection region, and also having a considerable excess component due to ohmic resistance. In low current operation, the beta matching of lateral PNPs is little different than for an NPN (possibly a little better).

Many interesting consequences of operation at high-level injection follow. First, the base current is

$$I_B = I_C^2/I_{BS} \quad (6.3)$$

that is, a *parabolic* function of I_C . Alternatively, the collector current is seen to be a square-root function of I_B , that is,

$$I_C = \sqrt{I_B I_{BS}} \quad (6.4)$$

At lower injection levels, the base current becomes asymptotic to its maximum (low-current) value, $\beta_{\max}$, and at very low currents it shows the customary decline again, as space-charge recombination begins to dominate the base current. We can empirically formulate the base current as

$$I_B = I_C \sqrt{(I_C/I_{BS})^2 + (1/\beta_{\max})^2} \quad (6.5)$$

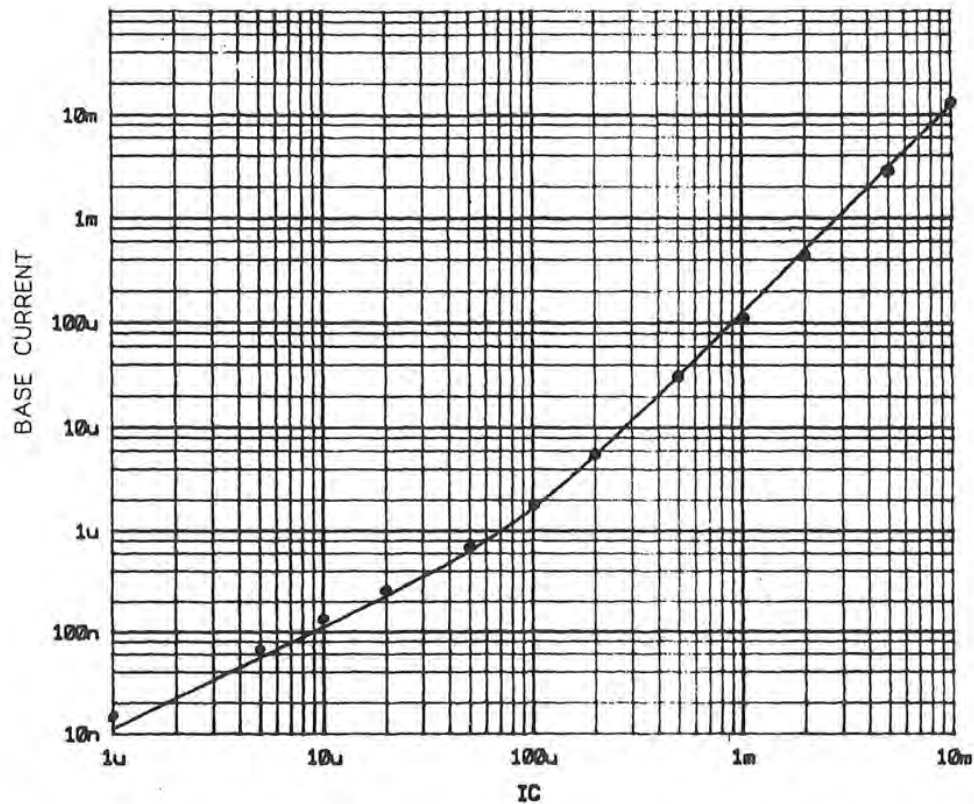


Figure 6.3 Measured base current of lateral PNPs compared to the empirical fit given in Eq. 6.5

Figure 6.3 shows the good agreement between this suggested formulation and measurements on a lateral PNP from a production monolithic process. In this case, I_{BS} was 8.1mA and β_{max} was 90. Similar close conformance has been found for a variety of different processes.

While it would be unwise to depend too heavily on this generally-reliable high-level behavior to implement some desired nonlinear function, it does suggest that a single lateral PNP may be valuable as a single-transistor mirror in biasing applications. An example is shown in Figure 6.4, where the "slewing" node of a high-speed op-amp must be driven by a fairly large current, say, 2mA. Using a conventional current mirror, using high-beta transistors and a mirror ratio of, say, 2, would require a driving current of 1mA. By relying on the nonlinear beta of a lateral PNP, with $I_{BS} = 10\text{mA}$, we can calculate (using Eq. 6.4) that I_B needs to be only 0.4mA.

There are other advantages to using single lateral PNPs in this way. Obviously, the chip area is less than that required by a two-transistor mirror; note in this connection that in multiple-output mirrors the common-base node corresponds to a single isolated epi region, another factor leading to

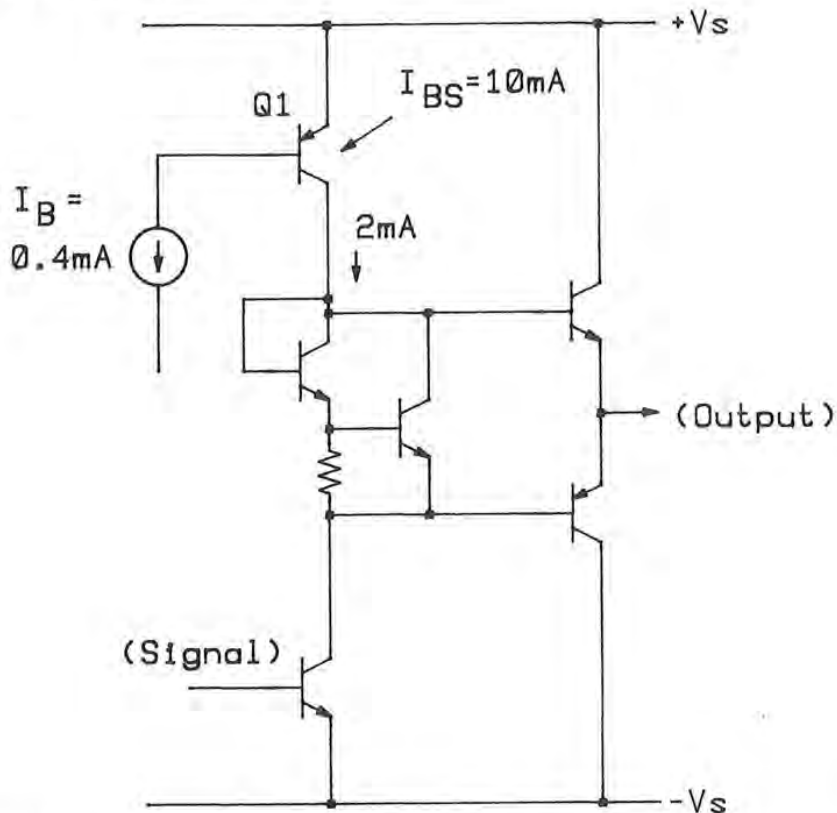


Figure 6.4 A simple open-base PNP current mirror (Q1) used to bias an op-amp slewing node with improved efficiency; remaining components are for illustrative purposes only.

reduced chip area. The output capacitance is only C_{JC} (the epi-substrate junction now only affects the input capacitance) and since the mirror gain is usually low, Miller multiplication of this capacitance is only moderate. A more subtle advantage is that the output resistance is higher than might be expected from low-current measurements of V_{AF} . This is because of another consequence of high-level injection, namely, the progressively-increasing charge concentration in the base at higher collector currents reduces the rate at which the depletion layer moves into the base, that is, the Early voltage of a lateral PNP increases at high values of I_C as the reduction of base width with collector bias decreases. In fact, it can be shown that the output conductance, g_o , is proportional to the square-root of collector current; for a typical device, its value can be pragmatically stated as $5\sqrt{I_C}$ microsiemens, when I_C is in milliamps. Figure 6.5 shows the close agreement with experimental results for g_o versus I_C , measured on seven samples.

Where a very low output capacitance is of dominant importance, a lateral PNP can also be operated in an inverse mode, with the output being taken from the emitter - usually a small circular diffusion of 5 to 20 μm in diameter

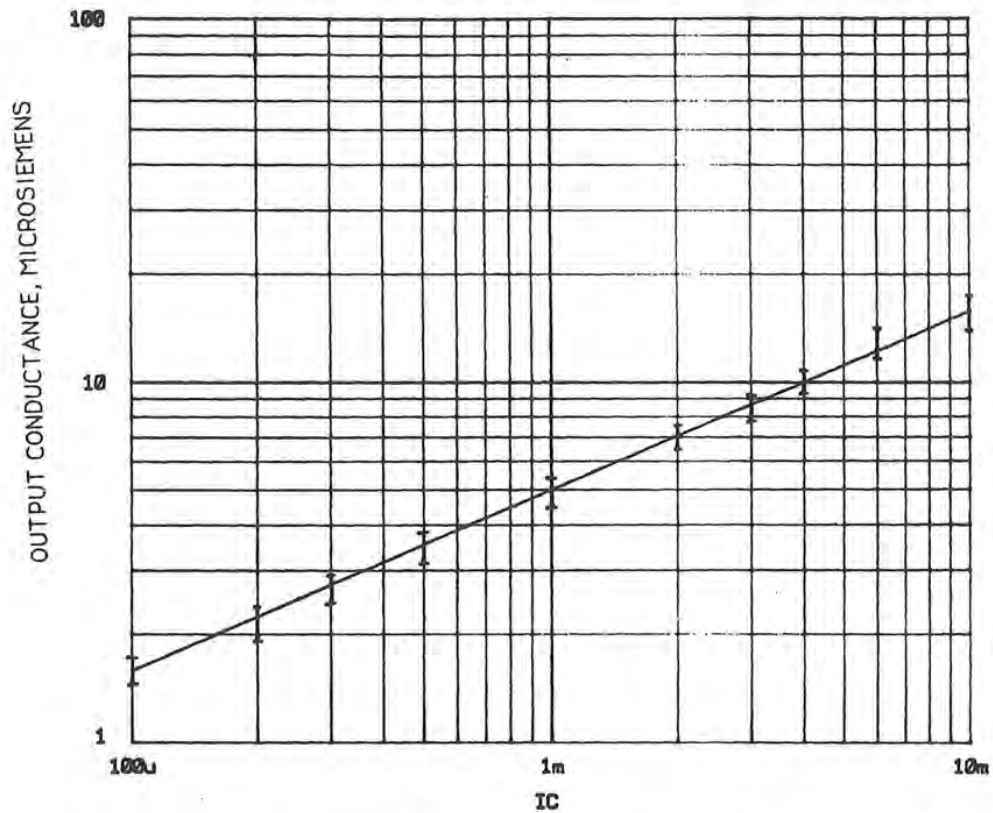


Figure 6.5 Measured output conductance of lateral PNP's compared to empirical fit of $5I_c^{0.5}$ microsiemens (I_c in mA)

- with the collector ring diffusion treated as the emitter common terminal. The inverse beta is lower, partly because more than half of the current injected from this ring flows outward to the surrounding isolation wall. However, the base scaling current is higher, due to the larger area of the effective emitter, so useful amounts of output can be generated before the lowered beta renders the device inefficient. Since the breakdown voltage of the emitter and collector are the same (that is, the BV_{CBO} of the corresponding NPN) the bias restrictions which arose with the inverted-mode operation of the NPN do not apply here. Note, however, that lateral PNP transistors can exhibit breakdown due to punch-through if the emitter-collector spacing is insufficient for the bias voltage; this occurs when the depletion layers penetrate into the base region far enough to reduce the effective base width to zero.

Current sources and mirrors based on lateral PNPs can take advantage of another possibility afforded by the structure, namely, the use of a split collector diffusion. Figure 6.6a shows a typical geometry, in which the two segments are of equal size; unequal segments can be used, and of course more

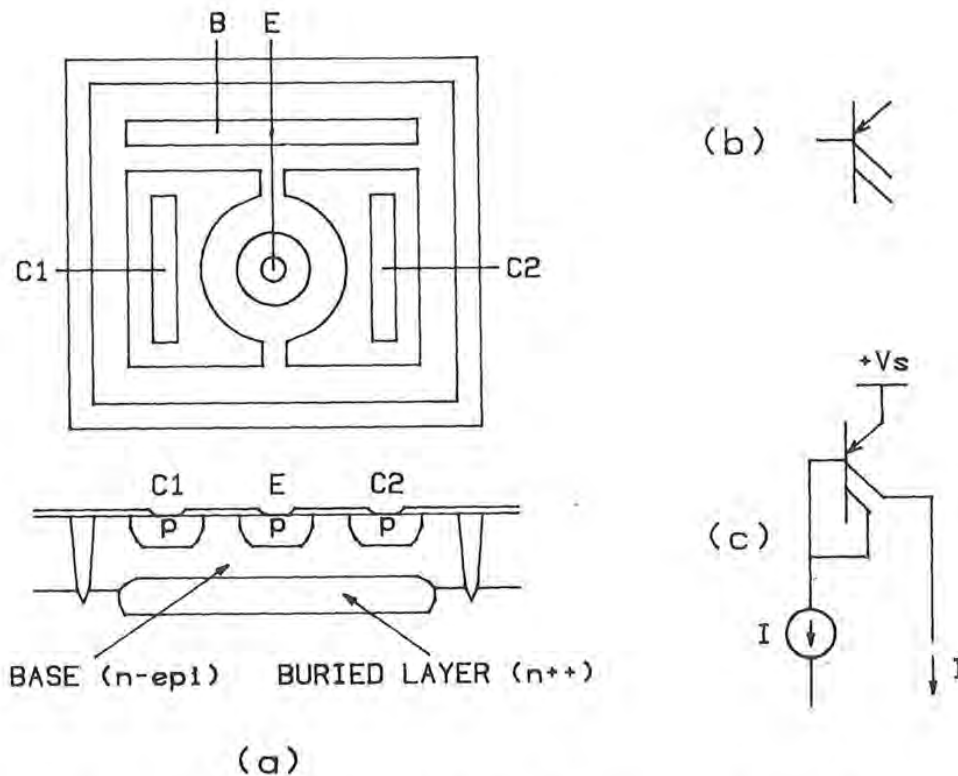


Figure 6.6 Split-collector lateral PNP: (a) plan view; (b) symbol; (c) connections to realize a unity-gain current mirror.

than two segments are possible. The unique nature of this device makes it valuable in numerous biasing applications. The current matching between halves of a two-collector lateral PNP is very good, routinely better than $\pm 1\%$, and using special layout precautions, employing cross-connected pairs of split-collector transistors, sources matched to better than $\pm 0.1\%$ (at equal V_{CB}) have been maintained in production. This is valuable when using the device to provide a pair of active loads for an amplifier input stage, for example. This matching does not depend on the V_{BE} matching of two separate transistors, as is the case when using normally-biased NPN transistors as current generators. One way of visualizing this is to imagine that the single 'dot' of the emitter is like a light bulb positioned at the centre of the collector ring - emitting holes rather than photons - which illuminates all points on the ring with equal 'flux'. Since the emitter and collector diffusions are defined on the same mask, the radial symmetry is excellent. Even more intriguing is the almost-zero sensitivity of this current match to thermal- or stress-gradients of the chip; these can severely degrade the matching of collector currents in a pair of NPNs, via their effect on V_{BE} ,

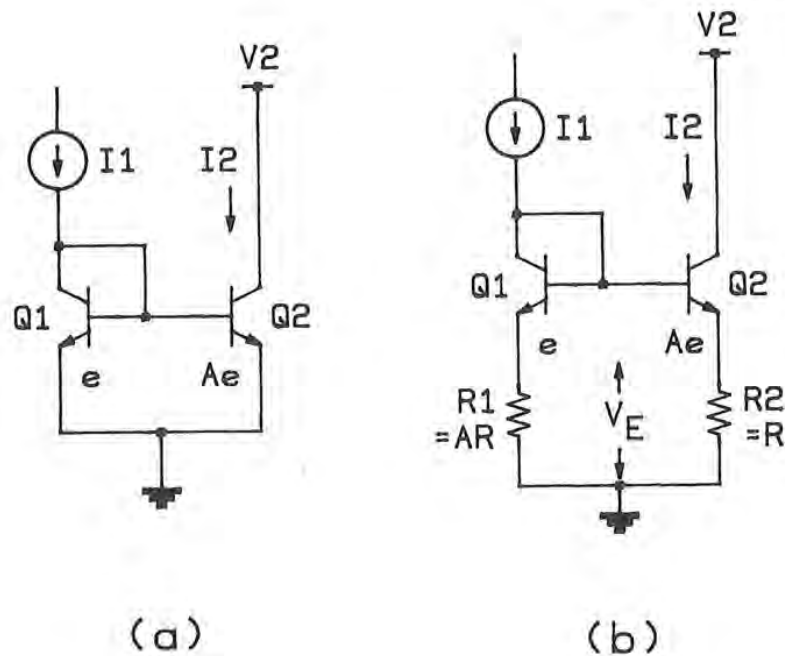


Figure 6.7 The classical NPN current mirror (a), with the addition of emitter degeneration (b).

which results in a current ratio error of 8% for a roughly 2mV ΔV_{BE} induced by a 1°C temperature difference between devices.

A split-collector lateral PNP transistor (two 180° collector segments) is occasionally used to realize a near-unity-gain mirror, by connecting one of the segments back to the base (Figure 6.6c). This is particularly effective at low currents, where the beta is high. Obviously, this idea can be extended to provide a ratio of 2 or 0.5 (using three 120° segments), or 3 or 0.33 (using four 90° segments). It is difficult to use more segments, limited by the minimum feature dimension and required spacing between these segments. Non-integral splits can be used, with reduced ratio accuracy.

6.3 Two-transistor Mirrors

The basic NPN current mirror (Figure 6.7a) is the simple theme from which endless variations and transformations can be spun, many of fundamental and pervasive value, others of which are mere curiosities awaiting exploitation. Although much has been written about this circuit in the many fine standard texts, there remain certain points of view that may not have been expressed or sufficiently stressed. It happens, for example, to be the simplest translinear circuit of practical interest, and we will begin here with the translinear view of this mirror.

Recall from Chapter 2 that in any loop containing an equal number of voltages across clockwise- and counterclockwise-biased PN junctions, the product of the current-densities in the two directions must be equal. Here, the

loop contains only one junction voltage in each direction, and these are one and the same voltage in this trivial case, namely, the V_{BE} of both transistors. Since the current densities are equal, the ratio of the collector currents must be identical to the emitter area ratio, A . In practice, this would only be exactly true if this ratio were an integer and realized by exact replication of a basic geometry, for example, by making Q2 from four basic units of Q1, and if both transistors were operated at identical values of V_{CB} , which demands in this case that $V_2 = V_{BE}$. Note that the finite ohmic resistances do not affect the accuracy of the currents, since they can be assumed to scale in proportion to A and therefore the excess V_{BE} which they contribute is identical for each device. Nor is the finite, temperature-dependent beta, including its nonlinearity with current, a source of error in the ratio of the *collector currents*.

Errors in the actual mirror ratio, M , arise because

- 1 V_2 is, in general, not equal to V_{BE} , and the finite output resistance will cause I_2 to increase with V_2 .
- 2 Some of I_1 is lost to the bases of both Q1 and Q2, so that $I_{C1} < I_1$.
- 3 Unless strict integer replication of geometry is used, there will be errors in the effective value of A and the ratio of junction resistances.
- 4 Even then, small random variations in emitter area and other sources of V_{BE} mismatch (including thermal gradients and strain) will occur.

6.3.1 Effect of Practical Device Imperfections

Errors in delineating the emitter area ratio A will result in essentially identical errors in the actual mirror ratio M . This is sometimes explained in terms of " V_{BE} mismatch", but this expression is helpful only as a reminder that a very small voltage difference between emitter nodes can have a large effect on accuracy. Indeed, there really can be no V_{BE} mismatch in this circuit, since in the current mirror both devices *operate at identical V_{BE}* , having their emitter-base junctions in parallel. However, we can translate an uncertainty in area ΔA into an equivalent V_{BE} error for the case (not true in the current mirror) where the transistors are operated at *identical collector currents*. This is well-known to be

$$\Delta V_{BE} = V_T \ln(1 + \Delta A) \quad (6.6)$$

which simplifies to

$$\Delta V_{BE} \approx V_T \Delta A \quad (6.6a)$$

for $\Delta A \ll 1$, amounting to $\pm 260 \mu\text{V}$ at $T = 300\text{K}$ for a $\pm 1\%$ area uncertainty. V_{BE} is also a function of emitter depth and other local variations in the device; these, and any further variabilities in V_{BE} , can be converted to a modified area ratio A' , which may have a value greater or less than A , by rearranging Eq. 6.6 to first calculate ΔA then

$$A' \approx A \exp(\Delta V_{\text{BE}}/V_T) \quad (6.7)$$

The error due to finite beta can be quickly determined by noting that

$$I_1 = I_{\text{C1}} + I_{\text{B1}} + I_{\text{B2}} = I_{\text{C1}} + I_{\text{C1}}/\beta_1 + I_{\text{C2}}/\beta_2 \quad (6.8)$$

and, if $V_2 = V_{\text{BE}}$ and good scaling disciplines have been observed, we can assume that $\beta_1 = \beta_2 = \beta_0$, so that

$$I_1 = I_{\text{C1}} + I_{\text{C1}}/\beta_0 + AI_{\text{C1}}/\beta_0$$

while $I_2 = AI_{\text{C1}}$

The actual mirror ratio, I_2/I_1 is therefore

$$M = \frac{A}{1 + (1 + A)/\beta_0} \quad (6.9)$$

For a classical mirror having $A = 1$ and our "standard" condition of $\beta_0 = 100$, the error in M is -2% . Note that for very large values of A the above expression correctly shows the current ratio is asymptotic to β_0 .

Finite Early voltage causes the output current to increase with the collector bias as given in Eq. 6.1. Combined with the loss due to finite beta, the complete expression is

$$I_2 = \frac{A(1 + V_2/V_{\text{AF}})}{1 + (1 + A)/\beta_0} I_1 \quad (6.10)$$

Note that this expression includes the voltage-dependence of beta, since I_2 increases at the same rate as β_2 , so the base current of Q_2 is constant with V_2 . The output resistance remains V_{AF}/I_2 , independent of β or A . The small-signal input resistance r_i is now essentially just the r_e of Q_1 , that is, V_T/I_1 , and is also independent of β , A , and V_{AF} . Note, however, that this is exactly the same as for the rudimentary one-transistor mirror.

6.3.2 Use of Emitter Resistors to Improve Accuracy

We will return to further developments of the translinear view of the current mirror later, but first examine the effect of adding resistors in the emitter branches (Figure 6.7b). This is usually referred to as emitter degeneration,

because the naturally-high gm of the devices is lowered in this way.

To understand how this works, first note that the V_{BE} of Q_2 is a function of both its collector current I_C and collector voltage V_{CB} . Starting with Eq. 6.1b

$$V_{BE} = V_{BE0} - V_T \ln(1 + V_{CB}/V_{AF}) \quad (6.1c)$$

Here, V_{BE0} the value of V_{BE} for some I_C and temperature, and at $V_{CB} = 0$, given by

$$V_{BE0} = V_T \ln(I_C/I_S(T)) \quad (6.1d)$$

So, if the mirror is to have a high output resistance, it must somehow be desensitized to the variation in the V_{BE} of Q_2 caused by output voltage variations. This is the function of emitter degeneration.

With reference to Figure 6.7b, it can be seen that the larger the "degeneration voltage", V_E , that is allowed to develop across resistors R_1 and R_2 , the less any variation of V_{BE} affects the output current I_2 . When V_E is very large, Q_2 might be considered to be operating essentially as a common-base stage, current-driven in its emitter, but there is a subtle and important difference. We can readily calculate the output resistance for this limiting case by considering just the variation of β_2 with V_2 . For now, assume that the resistor ratio R_1/R_2 is made equal to the emitter area ratio A , as indicated in the figure. This would normally be the case; the consequences of altering it are discussed later. Then, we can immediately write

$$V_E = I_2(1 + 1/\beta_2)R = (I_1 - I_2/\beta_2)AR$$

from which it follows that

$$M = \frac{I_2}{I_1} = \frac{A}{1 + (1 + A)/\beta_2} \quad (6.11)$$

Now, if β_2 were fixed, this is essentially the same result as given already in Eq. 6.9, but in fact

$$\beta_2 = \beta_0(1 + V_{CB}/V_{AF}) \quad (6.12)$$

Inserting this into Eq. 6.11 and finding the derivative dI_2/dV_{CB} yields the output conductance, from which the general output resistance can be shown to be

$$r_o' = \frac{V_{AF}}{A(A+1)I_1} \frac{\{\beta_0(1 + V_{CB}/V_{AF}) + 1 + A\}^2}{\beta_0} \quad (6.13a)$$

This is not very insightful, so let us consider some special cases. First, for the classical mirror with $A = 1$ and $\beta_0 \gg 1$, operating at with V_2 much less than

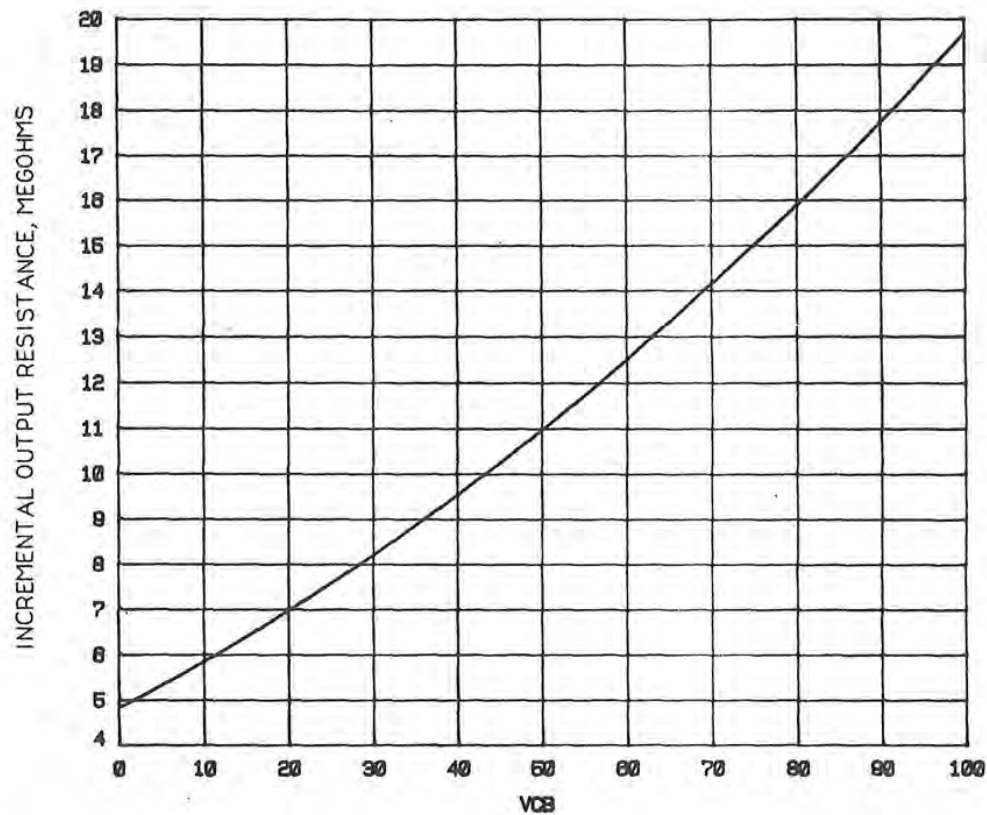


Figure 6.8 Output resistance of a highly-degenerated mirror operating at $I_C = 1\text{mA}$ varies from about $5\text{M}\Omega$ at $V_{CB} = 0$ to $20\text{M}\Omega$ at $V_{CB} = V_{AF}$.

V_{AF} , Eq. 6.13a simplifies to approximately

$$r_o' = \frac{V_{AF} \beta_o}{2I_2} \quad (6.13b)$$

with I_1 replaced by I_2 , appropriate for the conditions stated.

For example, using our benchmark device having $\beta_o = 100$ and $V_{AF} = 100\text{V}$, r_o' at 1mA is $5\text{M}\Omega$, 50 times the value for the basic mirror. The reason it is not beta times as high, as might be expected, is that a reduction in the base current of Q2 due to an increase in V_2 simultaneously reduces *two* sources of error: the first is in the loss of current conveyed from the emitter branch of Q2 to its collector (that is, alpha increases with V_2); the second is in the reduction of the base current lost from the input current I_1 . If the base node were grounded and the emitter of Q2 driven by an ideal current source of value I_2 , then r_o' would be simply $V_{AF}\beta_o/I_2$, the value sometimes given for the asymptotic output resistance of the highly-degenerated mirror. Errors in analysis can usually be traced to the use of small-signal modeling procedures,

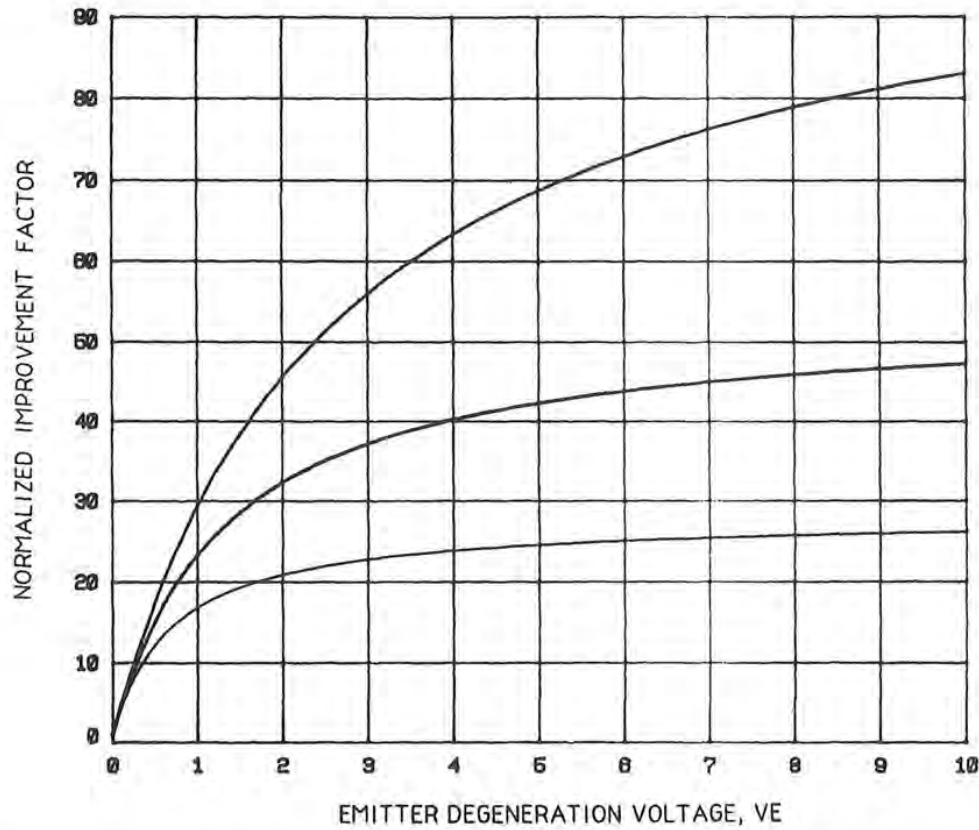


Figure 6.9 Improvement in output resistance versus degeneration voltage V_E , normalized to case where $V_E = 0$, for $\beta = 50, 100$ and 200 .

which do not accurately reflect alteration in the operating point of all devices.

Eq. 6.13a shows that the output resistance is also a function of the collector bias voltage, which is not often recognized; for the case where $A = 1$ and $\beta_o \gg 1$, it simplifies to

$$r_o' = \frac{V_{AF}\beta_o}{2I_2} (1 + V_{CB}/V_{AF})^2 \quad (6.13c)$$

Thus, at $V_{CB} = V_{AF}$ we would expect r_o' to be four times higher than at $V_{CB} = 0$, and that a curve of I_2 versus V_2 should be nonlinear. This is exactly what happens for our semi-ideal transistor, having $\beta = 100$, $V_{AF} = 100$, operating at $I_C = 1\text{mA}$ and using a very large value for R . Figure 6.8 shows a simulation result; the incremental r_o' which varies from about $5\text{M}\Omega$ to $20\text{M}\Omega$ between $V_{CB} = 0$ and $V_{CB} = V_{AF}$, as predicted by Eq. 6.13c. Nonlinearity in r_o' is rarely of concern; at high mirror ratios, and for *lower* values of V_E , the nonlinearity is reduced.

When the emitter resistors are of more practical value, the output resistance does not reach these asymptotic values. Figure 6.9 plots the ratio r_o'/r_o , that is, the improvement in output resistance compared to the basic mirror (Figure 6.7a), versus degeneration voltages of zero to 10V, with β_o set to 50, 100 and 200; note that the asymptotic value at $\beta_o = 100$ is 50, as previously found. These curves were calculated for $V_{AF} = 100V$.

It is sometimes desirable to achieve a mirror ratio other than unity entirely by the use of unequal emitter resistors, that is, keeping $A = 1$ but making $R_2 \neq R_1$. This situation could arise, for example, when a current gain of, say, five is needed, while the collector capacitance of the output device has to be minimal. The use of equal transistor sizes operating at unequal currents will inevitably result in a ΔV_{BE} between the emitter voltages. In the special case where I_1 is PTAT, this will track the PTAT voltages across the resistors, and the ratio will remain stable over temperature, for all combinations of emitter areas and resistor ratios. More commonly, I_1 will be temperature-stable and this ΔV_{BE} will now add (when $M < 1$) or subtract (when $M > 1$) from the stable voltage $V_E = I_1 R_1$ across emitter resistor R_1 (Figure 6.7b), resulting in a temperature dependence in the voltage across R_2 , and hence in the actual mirror ratio. If M is not greatly in error (because it is close to one, or because V_E is large, or because the resistor ratio has been adjusted to first-order correct the error), it can be shown that the residual drift has a fractional magnitude $(V_T/V_E \ln M)/300$ at $T = 300K$. For example, if the adjusted M were 5 and a V_E of 500mV were used, the drift would be $((26mV/500mV) \ln 5)/300 = 0.0028$ or 280 ppm/°C.

The input resistance of a mirror using emitter degeneration is approximately $V_T/I_1 + R_1$. This may be troublesome; if nothing else, the voltage at the common base node N1 erodes the output range, which now cannot go below $I_1 R_1 + V_{BE}$. In signal-path applications, the pole formed by R_1 and the C_{JS} of Q1 plus other parasitic capacitive components, will affect the HF response. Note that emitter resistors do not reduce the output deficit caused by finite beta. Beta compensation can be included by adding a resistor R_B of the correct value in the base of Q1, as shown in Figure 6.10. It can be shown that for V_{CB} close to zero (that is, neglecting base-width modulation errors) the necessary value is

$$R_B = \frac{\beta + 1}{\beta - A} (1 + A) (r_e + R_1) \quad (6.14)$$

For example, using $A = 2$, $I_1 = 1mA$ (so $r_e = 26\Omega$) and $R_1 = 500\Omega$ (so introducing about 500mV of degeneration) R_B should be 1.578k Ω if the factor involving beta is ignored, or 1.626k Ω if it is included and beta is assumed to be 100. Clearly, the method becomes unpredictable when A is comparable with β , and can never be precise since β_1 and β_2 are not in general equal; nevertheless, the technique is of considerable practical utility.

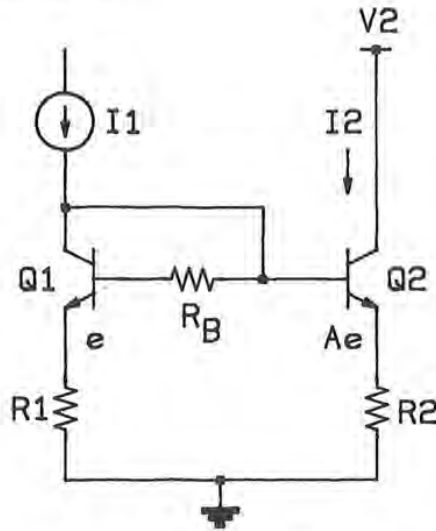


Figure 6.10 The inclusion of a resistor in the base of Q_1 helps to compensate for the finite beta of Q_2 .

6.3.3 Noise and Drift Considerations

Current mirrors generate noise. This arises from two sources: shot noise in the junctions and Johnson noise in the resistances (extrinsic and diffusion). At low frequencies, flicker noise will also be present.

Consider first the ideal non-degenerated mirror, that is, one using semi-ideal transistors (having high beta and Early voltage, and no ohmic resistances), with a general emitter ratio A . It is easy to show that the flatband noise spectral density (NSD) in the output due to shot noise is

$$s_I = \sqrt{2qI_1 A(A+1)} \quad (6.15a)$$

where q is the electronic charge, $1.6 \times 10^{-19} \text{C}$. This can be pragmatically stated as

$$s_I = \sqrt{I_1} \sqrt{A(A+1)} \times 17.9 \text{ pA}/\sqrt{\text{Hz}} \quad (6.15b)$$

when I_1 is expressed in mA. Thus, an ideal unity-gain current mirror operating at 1mA generates a NSD of 25.3pA/ $\sqrt{\text{Hz}}$. As a practical aside, it is important in verifying these expressions by simulation experiments using SPICE to note that collector currents must first be converted to voltages in order to use the NOISE analysis mode, and that this should be performed using the "H" element (current-controlled voltage-source, or ideal transresistance element) controlled by the bias voltage source for the collector, rather than by the use of a load resistor, which will also be modeled as having Johnson noise. Even a 1 Ω current-monitoring resistor will generate about 128pV/ $\sqrt{\text{Hz}}$, far more than the voltage generated in this same resistor by the 25pA/ $\sqrt{\text{Hz}}$ of the mirror in our example.

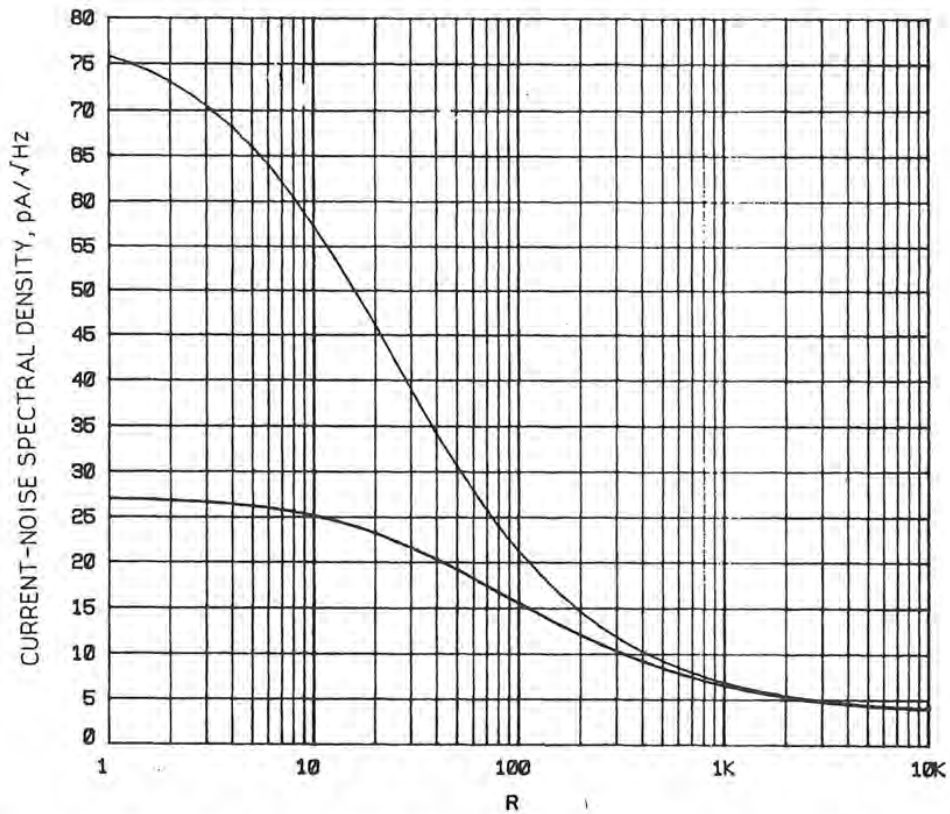


Figure 6.11 Collector current noise-spectral density versus degeneration resistance for a unity-gain mirror operating at 1mA, with $r_{bb'}$ = zero (lower curve) or 100Ω.

The inclusion of Johnson noise arising in the base resistance, $r_{bb'}$, in Q1 and Q2 is most simply carried out by invoking superposition, that is, by first calculating its contribution to the noise spectral density and later calculating the total noise. Base resistance noise can be shown to be

$$s_J = 2qI_1 \sqrt{\{A(A+1)r_{bb'}/kT\}} \quad (6.16a)$$

where $r_{bb'}$ is the base resistance of Q1, which evaluates to

$$s_J = I_1 \sqrt{\{A(A+1)r_{bb'}\}} \times 4.976 \text{ pA}/\sqrt{\text{Hz}} \quad (6.16b)$$

when I_1 is expressed in mA and $r_{bb'}$ is in ohms. Thus, the contribution to the total NSD due to 100Ω of $r_{bb'}$ in the otherwise-ideal unity-gain mirror at 1mA is about 70.4pA/√Hz, considerably more than the shot noise under these conditions. These expressions assume that $r_{bb'}$ scales with emitter area. Emitter contact resistance r_{ec} does not increase the overall noise in a properly-scaled mirror, because it reduces the transconductance of Q2 faster

than it increases the noise contribution of Q1.

The total NSD of the uncorrelated shot- and Johnson-noise sources sum to

$$s_T = \sqrt{\{s_I^2 + s_J^2\}} \quad (6.17)$$

Thus, the total NSD at the output of Q2 calculates to 74.8pA/√Hz for our example. To provide a better feel for the likely impact of this noise level, we can express 75pA/√Hz on a bias of 1mA as a dynamic range of 82.5dB in a 1MHz bandwidth. Emitter resistors reduce the effect of both the shot noise and Johnson noise. The full analysis is beyond the scope of this Chapter, but Figure 6.11 shows the reduction possible as the equal emitter resistors R are increased from 1Ω to 10kΩ in the "standard mirror" ($A = 1$, $I_1 = 1\text{mA}$) with an r_{bb} of zero and 100Ω.

Emitter resistors are also used to reduce errors due to strain- and thermally-induced shifts in V_{BE} . Such desensitizing is important in maintaining accurate balance in many monolithic circuits, where a power-dissipating transistor may be located close to a critical mirror⁶, and the resulting thermal gradient induces a ΔV_{BE} , or where inadequate die-attach uniformity leads to chip stresses. The improvement arises for the same reasons that degeneration reduces random noise, and can be readily calculated: it is roughly proportional to $(R+r_e)/r_e$, or $(V_R+V_T)/V_T$, where V_R is the voltage across the emitter resistors. Thus, by including just 240mV (about $9V_T$) of degeneration the sensitivity is reduced by an order of magnitude.

Degeneration can also reduce the absolute error in the mirror ratio, by transferring the matching requirement to resistors, rather than emitter areas. Well-designed resistors can match to $\pm 0.1\%$ or better, while the emitter-area match of small, single NPNs can be as poor as $\pm 1\%$ (corresponding to a ΔV_{BE} of 260μV at 300K). However, there is an interesting trap, here, which is not generally recognized. Imagine a unity-gain current mirror with nominally-identical emitter areas, but mismatched by ΔA . In the absence of emitter resistors, there would be an essentially identical error, ΔM , in the mirror ratio, but this would remain fixed over temperature; that is, there would be no *drift* in M . Likewise, if we inserted emitter resistors of sufficiently large value, the error due to ΔA would be swamped, and any error in the mirror ratio would be caused solely by ΔR . But for moderate values of R the ΔV_{BE} arising across the emitter nodes due to the ΔA will induce a drift in the output current, and at some critical value of R this drift will be maximized. It's easy to show that this will occur when the voltage across the resistors is kT/q , at which point the drift rate for small values of ΔA will be given approximately by

$$\Delta I_C / \Delta T = \Delta A \times 750\text{ppm}/^\circ\text{C} \quad (6.18)$$

⁶As well as fixed V_{BE} errors due to a stationary thermal gradient, distortion often arises in a poorly designed IC when the gradient fluctuates with load variations.

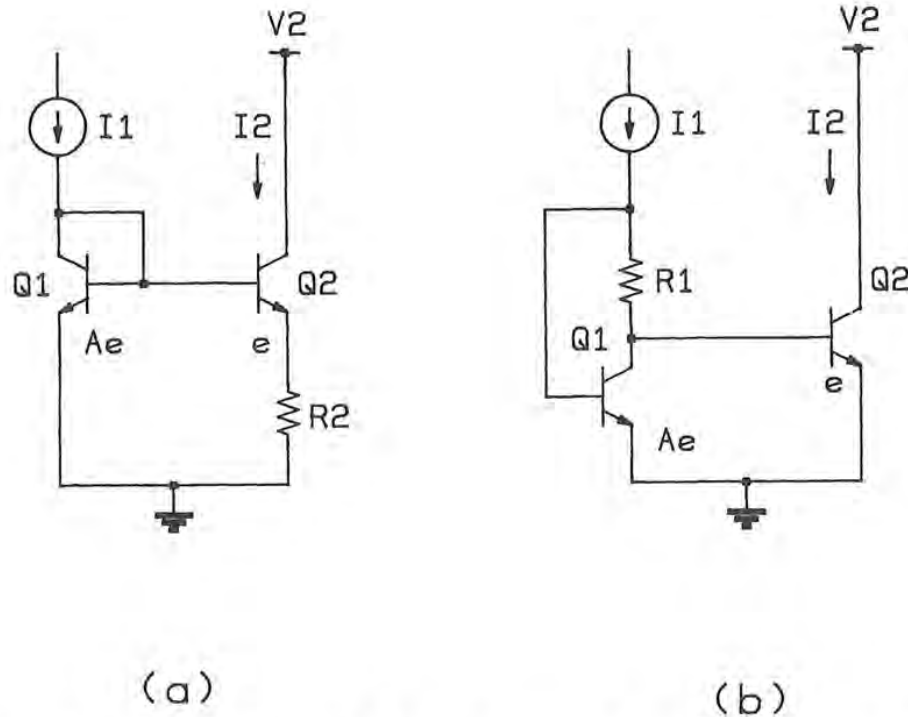


Figure 6.12 Two variants of the basic form: (a) the Widlar mirror for generating low currents and (b) the “gm-compensated” mirror.

For example, when $\Delta A = 0.1$ (a rather severe 2.5mV V_{BE} mismatch at $T = 300\text{K}$) the peak drift in I_C is 75ppm/ $^{\circ}\text{C}$; over the full military temperature range this results in a change of 1.4% in I_C .

6.3.4 Nonlinear Two-Transistor Mirrors

Numerous ways exist to alter the two-transistor mirror to effect various types of useful nonlinear behavior. Such circuits can be used to modify the shape of the transfer characteristic and the shape of the output over temperature. One of the earliest examples of this is the Widlar mirror [6, 6a] in which a resistor is added only to the emitter of Q2. This was intended to be useful in producing the small bias currents often needed in monolithic circuits without requiring the use of a large resistor R_o in the supply branch. Figure 6.12a shows the circuit, with Q1 shown as optionally having a larger area than Q2, since it is expected to be used in a current-lowering mode, aided by R_2 . The governing equation is

$$I_2 R_2 = V_{BE1} - V_{BE2} = V_T \ln(I_1 / A I_2) \quad (6.19)$$

the solution of which is transcendental for I_2 but which can easily be solved

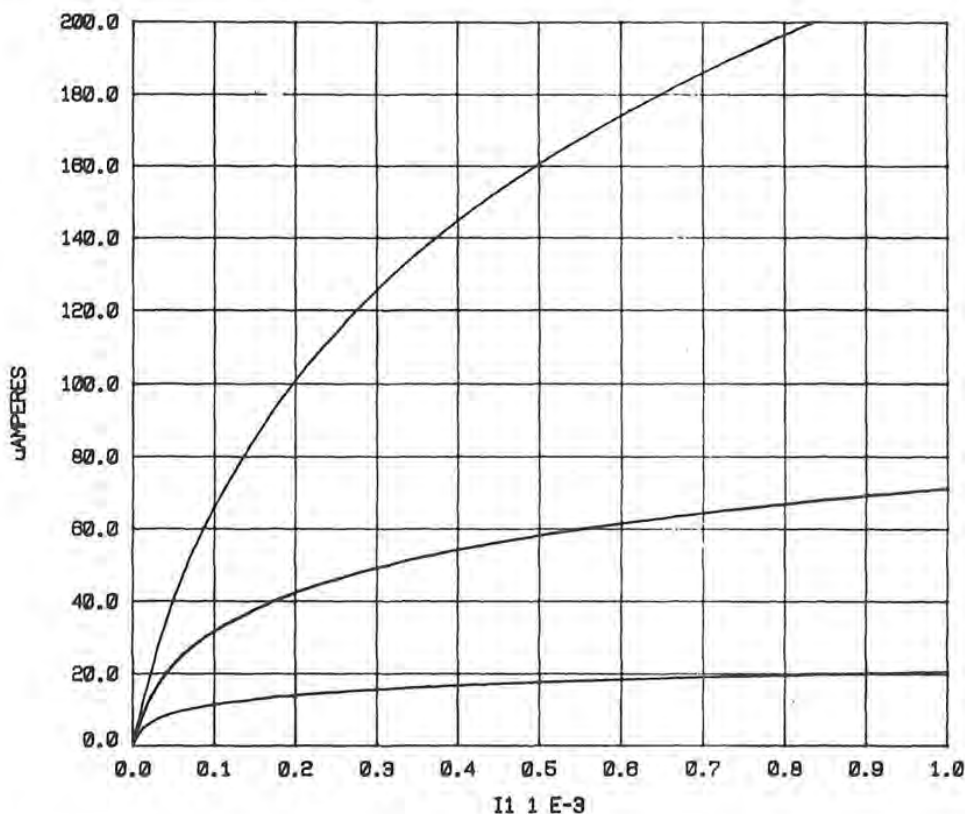


Figure 6.13 Output current versus input current for a Widlar mirror, having equal emitter areas and $R_2 = 200\Omega$ (upper curve), $1k\Omega$ or $5k\Omega$.

for R_2 given the values of I_2 and I_1 , when

$$R_2 = (V_T/I_2) \ln(I_1/AI_2) \quad (6.20a)$$

or, for the needed input I_1 given the values of I_2 and R_2 , when

$$I_1 = AI_2 \exp(I_2 R_2 / V_T) \quad (6.20b)$$

It is sometimes said of this mirror that I_2 is proportional to absolute temperature (PTAT) but clearly this is only approximately true under certain conditions, when the ratio I_1/AI_2 is very large. Figure 6.13 shows how I_2 varies with I_1 for various values of R_2 , using the general operating conditions maintained throughout the earlier examples; in this case $A = 1$. Note that the ratio I_2/I_1 is invariant if I_1 is PTAT; this "persistence of PTAT" is a common aspect of the current-mode transfer function of mixed (junction/resistor) circuits.

By altering the topology, placing R_1 in the *collector* of Q_1 , as shown in Figure 6.12b, a dramatic change in behavior occurs. This is sometimes called

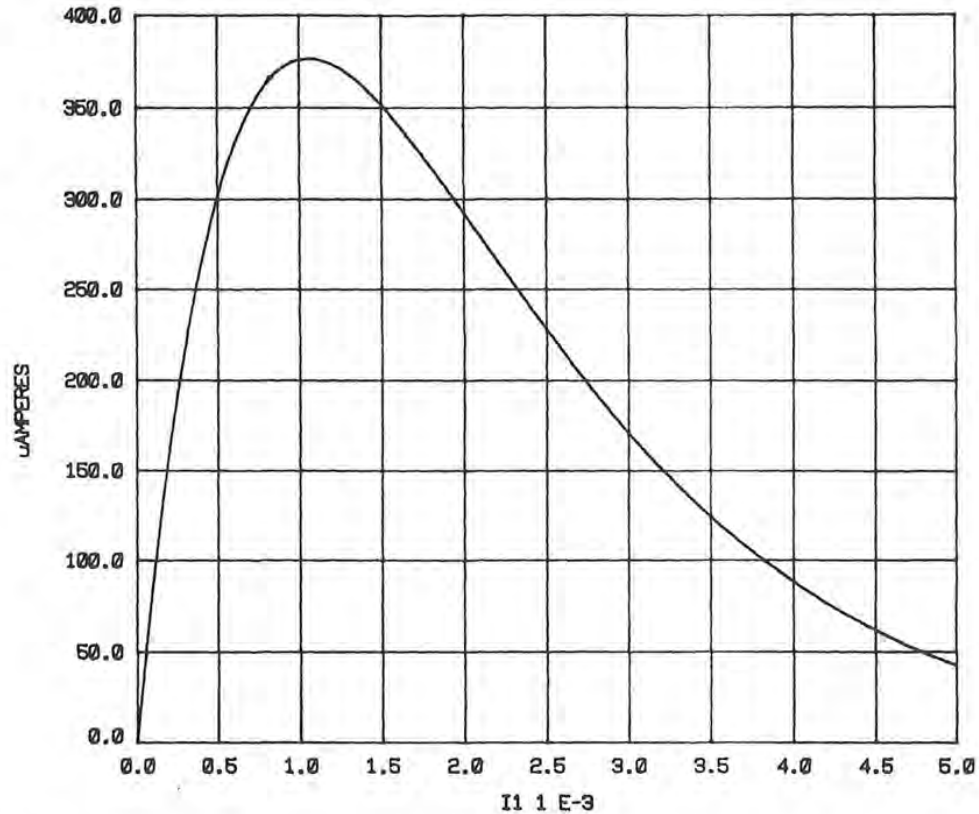


Figure 6.14 Output of the gm-compensated mirror versus input current, for $A = 1$ and $R_1 = 26\Omega$. Note that peak ratio of e^{-1} occurs at $I_1 = 1\text{mA}$.

the “gm compensated” mirror, because when R_1 is made equal to $1/g_m$, that is, the r_e of Q_1 operating at some specified I_1 , the increase in V_{BE1} caused by an increase in I_1 is exactly compensated by the increase in the voltage drop across R_1 . Consequently, the voltage delivered to the base-emitter junction of Q_2 is rendered insensitive to I_1 and therefore so is the output I_2 .

In fact, the behavior is much more interesting and general than this, and the circuit has many uses. In this case, an analytic expression for I_2 can be found:

$$V_{BE1} - I_1 R_1 = V_{BE2}$$

thus

$$I_2 = A I_1 \exp(-I_1 R_1 / V_T) \quad (6.21)$$

It is readily shown that I_2 peaks when $I_1 R_1 = V_T$ which is the condition previously noted as resulting in zero sensitivity to I_1 , at which point the

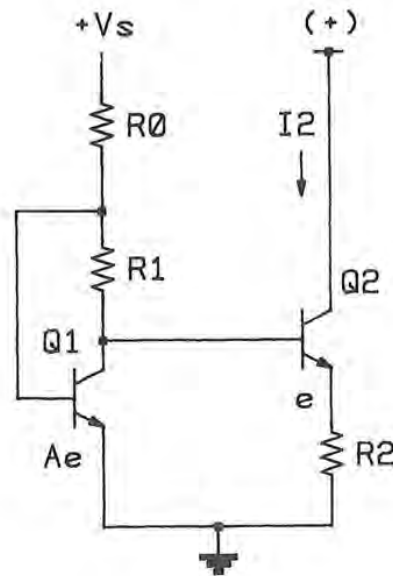


Figure 6.15 A fusion of the Widlar and gm-compensated mirrors provides relatively good regulation of a variable input current.

exponential factor has a value of e^{-1} or 0.368. Note that the area factor, A , has here been placed in the emitter of $Q2$, so that we can optionally restore the mirror ratio, M , to unity by making $A = e = 2.72$ (roughly $11/4$ in integer terms). Of course, in these recent analyses, we have neglected to account for the effects of beta and Early voltage; their inclusion is sometimes tractable, sometimes not, and always obscures the basic concepts. If high accuracy is essential, additional circuit elements invariably are required.

Figure 6.14 shows I_2 versus I_1 from 0 to 5mA, using $R_1 = 26\Omega$ and our "standard" transistors, with $A = 1$. It will be apparent that in addition to its utility in reducing the effect of input current variations when operated near the peak point, the circuit is useful in generating small currents, operating with voltage drops of much more than V_T across R_1 . In this way, much smaller resistor values are needed to produce a given output current than for the circuit of Figure 6.12a. For example, suppose we are using a Widlar mirror as part of a bias scheme to operate from a 5V supply and generate $I_2 = 1\mu A$. In order to keep the total resistance within reasonable bounds, we might set I_1 at $100\mu A$, requiring an R_0 of about $43k\Omega$, and choose to use two minimum-geometry transistors, so $A = 1$. Then, R_2 must be $59.5k\Omega$ (from Eq. 6.20b). On the other hand, using the circuit of Figure 6.12b we find R_1 can be 100 times smaller - 595Ω - since it has $100\mu A$, rather than $1\mu A$, flowing in it.

Now, in the Widlar mirror I_2 increases slightly with the supply voltage, while using the "gm-compensated" form it decreases. It is therefore likely that a lower sensitivity to the supply can be obtained by combining the two

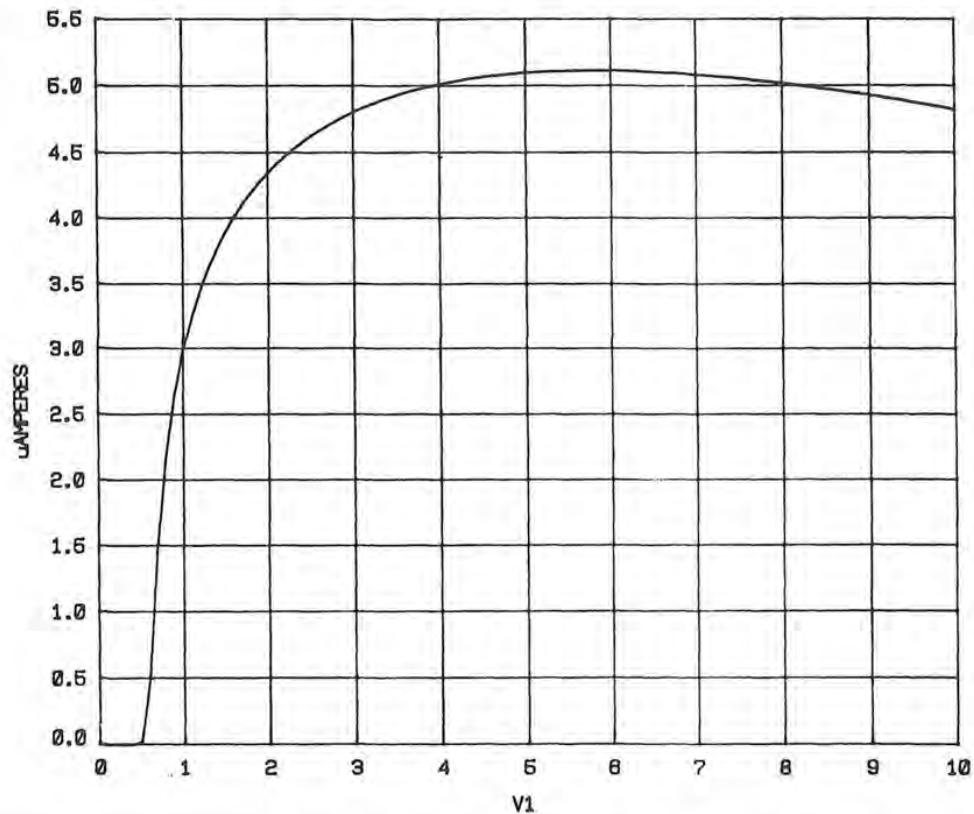


Figure 6.16 Output of the circuit of Figure 6.15; see text for details.

circuits, as shown in Figure 6.15. Under certain conditions, this can prove useful. Figure 6.16 shows the result for one such optimization, in which I_2 is designed to be $5\mu\text{A}$ for a 5V supply; here, $A = 1$, $R_0 = 18\text{k}\Omega$, $R_1 = 100\Omega$ and $R_2 = 15\text{k}\Omega$; the output is within 4% of its nominal value for supply voltages from 3V to 10V .

6.4 Three-transistor Mirrors

As is apparent, several variations can be found on the two-transistor theme: it is not surprising, therefore, to find that the addition of a third transistor considerably broadens the palette of the designer. Only a few of the numerous possibilities can be included in this brief survey. Most will have as their aim the improvement of accuracy, which most often means the reduction of beta-related errors.

6.4.1 The EF-Augmented Mirror

Figure 6.17a shows a commonly-used current-mirror, in which Q_3 operates as an emitter-follower (EF) and provides the base currents of Q_1 and Q_2 , so

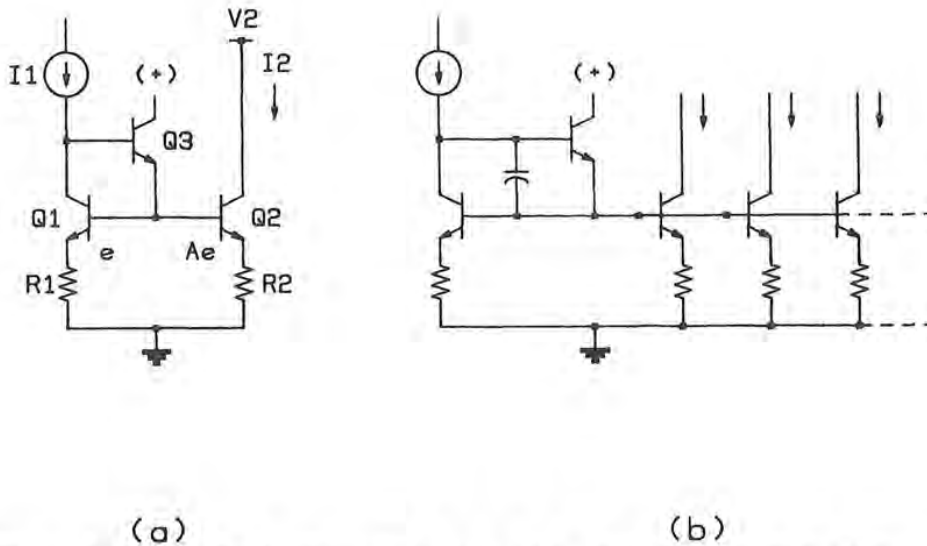


Figure 6.17 The EFA mirror in its basic form (a); this circuit is often used to provide multiple outputs (b); capacitor ensures HF stability.

augmenting their current gain. This mirror seems to have escaped being named, but, because we will refer to it several times in the rest of this Chapter, it will here be called the EF-augmented, or EFA, mirror. The use of emitter degeneration resistors and a non-unity area ratio is optional. It is readily shown that, assuming $R_1 = AR_2$ the mirror ratio is now

$$M = \frac{A}{1 + \left\{ \frac{1}{\beta_1} + \frac{A}{\beta_2} \right\} \frac{1}{\beta_3}} \quad (6.22)$$

so that even for quite large values of A , the beta errors are usually negligible, certainly now much less than other practical errors. For $A = 1$ and $\beta \gg 1$, this simplifies to

$$M = 1 - \frac{2}{\beta_1 \beta_3} \quad (6.22a)$$

where it has been assumed that the betas of Q1 and Q2 are equal. When this is not true (for example, when the output collector is very positively biased) the more complete expression must be used.

The output resistance, r_o' , using no emitter degeneration is the same as for the basic mirror - V_{AF} divided by the output current - but the maximum r_o' is now $V_{AF}\beta_2/I_2$, twice as high, for large amounts of degeneration.

The high internal current gain introduces the possibility of HF instability, since there are two "beta poles" in the basic circuit: from the base of Q3 to the base of Q1 is the beta pole of Q3; from here back to the base of Q3 is the beta

pole of Q1. In fact, a third pole may be generated by the emitter resistance of Q3 and the total capacitance on the base node, which includes the C_{π} of Q1 and Q2 (or more devices); this may become complex since the driving-point impedance is somewhat reactive. A complete discussion of the general HF response will not be included here. Suffice it to say that this system is often stable only because the much lower current in Q3 lowers its effective f_T to the point where it creates a dominant pole. Also, there is a small amount of feedforward around this slow device via the C_{JC} of Q1. By adding a further small capacitance across the base-emitter nodes of Q3 its beta is effectively removed from the HF loop. This is shown in Figure 6.17b, which also shows a more general scheme, including emitter degeneration and multiple outputs, now possible because of the higher effective beta.

6.4.2 Use of Cascodes to Raise Output Resistance

Some applications of current mirrors and sources require the highest possible output resistance. In these cases it is sometimes possible to place less emphasis on accuracy of the mirror ratio. A cascode transistor - a common-base stage, inserted between the output node and the mirror proper - can sometimes help. The maximum output resistance of a simple cascode, that is, when driven by a perfect current-source at its emitter, is $V_{AF}\beta/I$, and since the last mirror discussed can already attain that value using large amounts of emitter degeneration, we may need to look for further improvement. However, the use of a cascode allows the input resistance of the main mirror cell to be kept lower than possible using degeneration, and it can operate with a minimum output bias voltage which is lower, for the same output resistance.

Working on the assumption that it is the variation of beta with V_{CB} that limits r_o , we might try a Darlington⁷ cascode, to lower the base current variation, or an MOS or JFET device, which has essentially zero gate current. Such combinations are becoming very popular with the advent of combined Bipolar-MOS processes. In some cases, however, beta is not the limiting factor: to understand why, we need to look again at Eq. 6.1c, which shows the dependence of V_{BE} on V_{CB} :

$$V_{BE} = V_{BE0} - V_T \ln(1 + V_{CB}/V_{AF}) \quad (6.1c)$$

For small variations ΔV_{CB} near $V_{CB} = 0$, we can calculate the reverse transfer coefficient of the cascode to be

$$DV_{BE}/DV_{CB} = -V_T/V_{AF} \quad (6.1e)$$

that is, neglecting the beta-modulation effects of the output resistance, any

⁷The term "Darlington" configuration here refers to the use of a pair of transistors with common collectors and the emitter of the first connected to the base of the second so as to result in a very high effective beta, equal to the product of the individual betas.

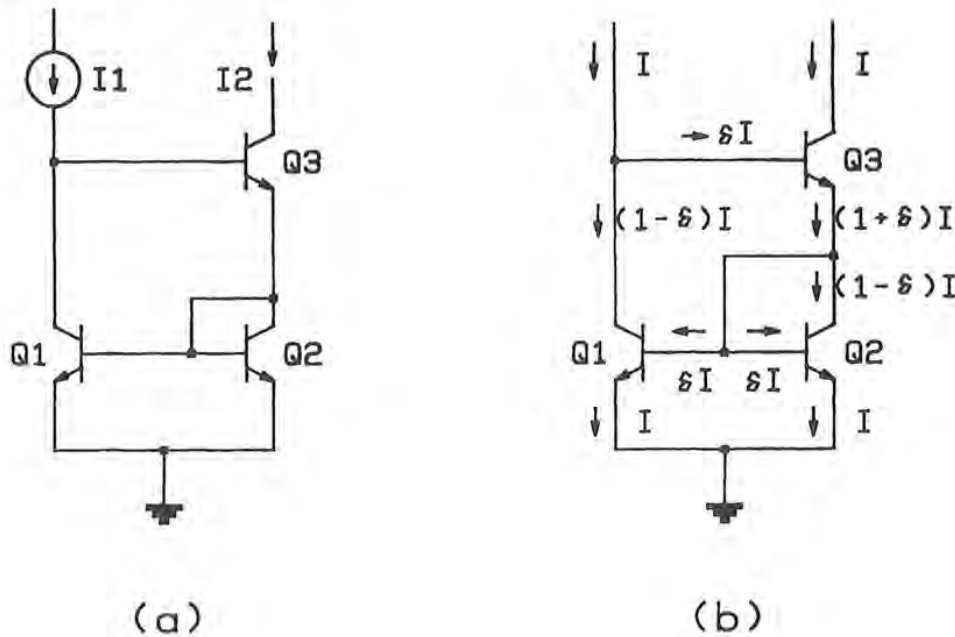


Figure 6.18 The Wilson mirror (a) and a simple way to understand how it achieves good accuracy for finite β .

variation in the voltage at the final output will cause the output node of the basic mirror to move and thus modulate the current. In short, it is still important to maximize the output resistance of the main mirror cell if the full benefits of a cascode are to be realized. The variation of V_{GS} with V_{DS} in a FET differs markedly, but the general idea of a reverse transfer ratio in the cascode still applies; in fact, the magnitude of the error is even greater.

6.4.3 The Wilson Mirror and Improvements

Sometime in 1967, George Wilson and the author set each other a mutual challenge as an overnight assignment: find a way of making a better current mirror using only three transistors. George won, and the Wilson mirror has become the first choice in many applications where good beta-immunity and high output resistance are needed.

The standard form (which, like the basic mirror, hardly needs repeating) is shown in Figure 6.18a. The circuit is not a panacea; its low beta-sensitivity, as we shall show, depends on beta-matching (unlike the EFA mirror just discussed) and the trick only works at unity-gain; significant errors can arise due to inequalities in the collector voltages of Q1 and Q2; the voltage at the output cannot approach the common node as any of the other mirrors presented so far; its noise performance is worse than the basic mirror; its AC response is strongly peaked. Nevertheless, it has proven to be a valuable cell, and we will later show some ways in which its utility can be extended.

The circuit is interesting in several ways. First, note that it contains a sub-cell, Q1/Q2, which is just a basic mirror; the input of this sub-cell is essentially the output of the complete mirror, with Q3 viewed as a cascode, and the output of the sub-cell becomes the input of the complete mirror. Thus, the Wilson mirror is a current-feedback circuit, the only mirror so far discussed that relies on feedback to establish its mirror ratio. We can think of its operation in this way: following the application of the input current, I_1 , Q3 would like to respond by generating a current beta times as large, but its emitter current is sensed by Q2, and mirrored back to the input, where a current-balance between I_1 and I_{C1} is established, requiring only the base current of Q3 to maintain, this current being in the nature of the error signal in a feedback loop. We might at this point be inclined to suggest that Q3 should therefore be made a Darlington, to reduce this "error" still further. If the sub-cell had no beta errors of its own (essentially true of the EFA mirror) that might be the correct thing to do. In fact, the finite base current of Q3 is needed to ensure that the mirror ratio is close to unity, as we will now see.

Figure 6.18b shows an approximate way of analyzing this circuit. We begin by assuming that the emitter currents of Q1 and Q2 are equal and of value I . This follows from the fact that they are assumed to be identical transistors and are operating with the same V_{BE} . Then, using the convention $\delta = I_B/I_E$, we find the collector current of Q1 to be $(1-\delta)I$, while the combined collector current of Q2 and the base currents of Q1 and Q2 sum to $(1+\delta)I$, which becomes the emitter current of Q3. To a good approximation, the base current of Q3 is δI , so the mirror ratio is

$$M = \frac{I_2}{I_1} = \frac{(1+\delta)I - \delta I}{(1-\delta)I + \delta I} \equiv 1 \quad (6.23)$$

whatever the value of δ (which is roughly $1/\beta$). A more careful analysis, but still assuming all betas are equal, yields

$$M = 1 - \frac{2}{\beta^2 + 2\beta + 2} \approx 1 - \frac{2}{\beta^2} \quad (6.24)$$

This result, given in most texts on the subject, suggests that the error in M due to finite beta is essentially the same as that for the EFA mirror (see Eq. 6.22a). In fact, it obscures an important detail, namely, that when the betas of Q1 and Q2 are *different*, there is a significant reduction in the accuracy promised by Eq. 6.24 and the Wilson mirror can very possibly be an order of magnitude worse than the EFA mirror in this regard. The complete expression is

$$M \approx 1 - \frac{2(\beta_1 - \beta_3) + 2}{\beta_1\beta_3 + 2\beta_1 + 2} \quad (6.24a)$$

Thus, if we assume $\beta_1 = 100$ and $\beta_3 = 95$ (a plausible 5% beta mismatch) the numerator evaluates to 12 rather than 2, so the error in the mirror ratio is

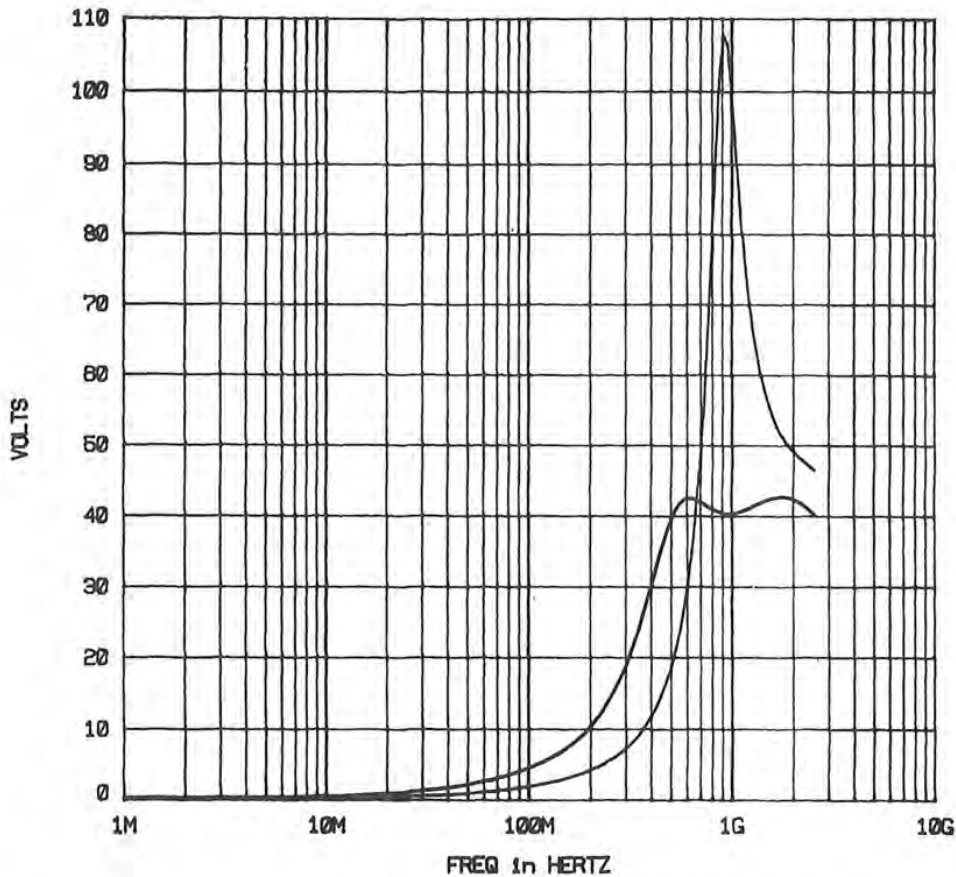


Figure 6.19 Impedance looking into the emitter of Q3, at a bias level of 1mA; see text for explanation of method used to lower the resonance.

six times worse than for the EFA mirror. The actual error in this case is still a fairly harmless 0.124%, but if this were a mirror built from lateral PNP transistors, where the betas might not just be low and mismatched, but strongly different because of high-level injection effects, the errors can be quite large.

It can be shown that the output resistance for the Wilson mirror is the same as for the heavily-degenerated basic mirror, that is

$$r_o' = \frac{V_{AF}\beta_o}{2I_2} (1 + V_{CB}/V_{AF})^2 \quad (6.25)$$

Emitter degeneration does not raise the output resistance of the Wilson mirror, because the output bias V_2 does not materially alter the V_{CB} of Q1; in fact, it is easily shown that the "attenuation factor" is V_{AF}/V_T , typically 4000:1.

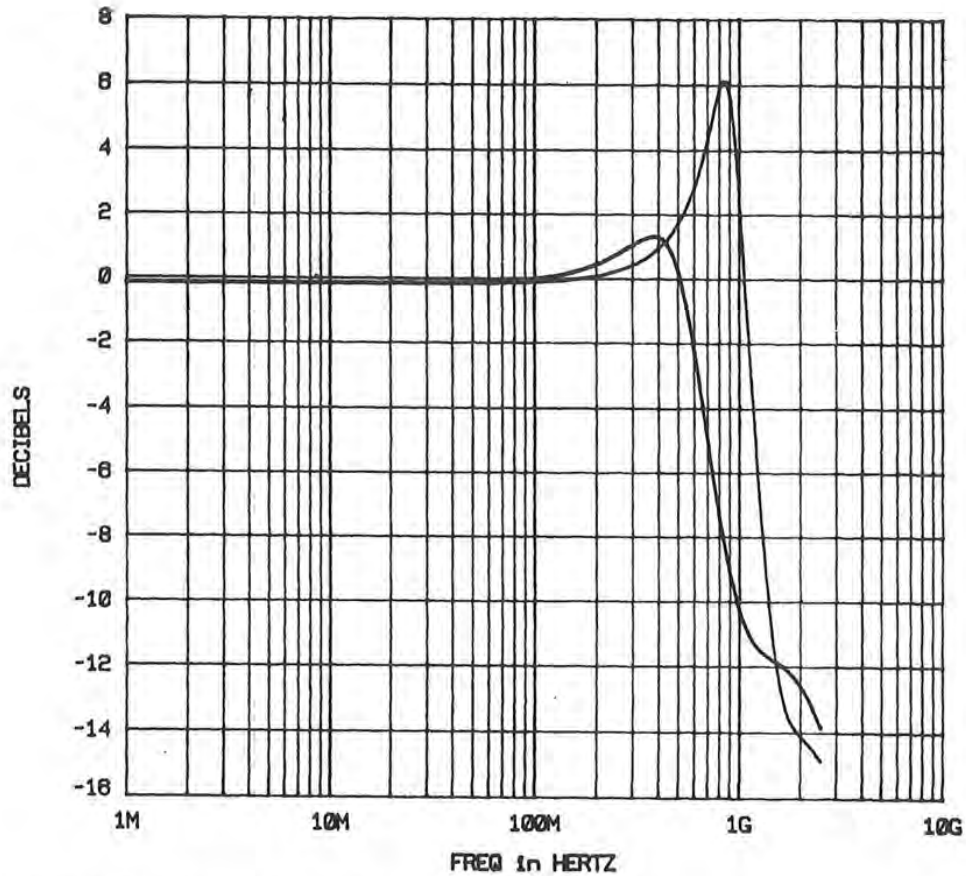


Figure 6.20 Current-mode AC response from the emitter of Q3 (Figure 6.19) to the output, with and without compensation capacitor of 5pF.

However, degeneration is often used for other reasons: it can transfer the burden of ratio-control from the emitter areas to a resistor ratio; it may obviate an error due mismatch in Q1 and Q2 (see below); it lowers the output noise.

Before discussing various improvements which can be made, one other useful property is worth mentioning. The impedance at the emitter of Q3, call it Z_3 , is quite low. Imagine a signal current of i applied to this node, and a bias current of I_1 applied to the normal mirror input. Q1 is forced to conduct I_1 , which requires that the V_{BE} of Q1 must remain at the constant value required by I_1 , whatever the value of i , which is therefore absorbed by Q3, and thus appears at the output. It follows that Z_3 ought to be nearly zero. Of course, a component δi flows in the base of Q3, thus modifying the collector current of Q1 and perturbing its V_{BE} . We can guess (correctly!) that at low frequencies Z_3 approximates to a resistance of $V_T/\beta I_1$, or about

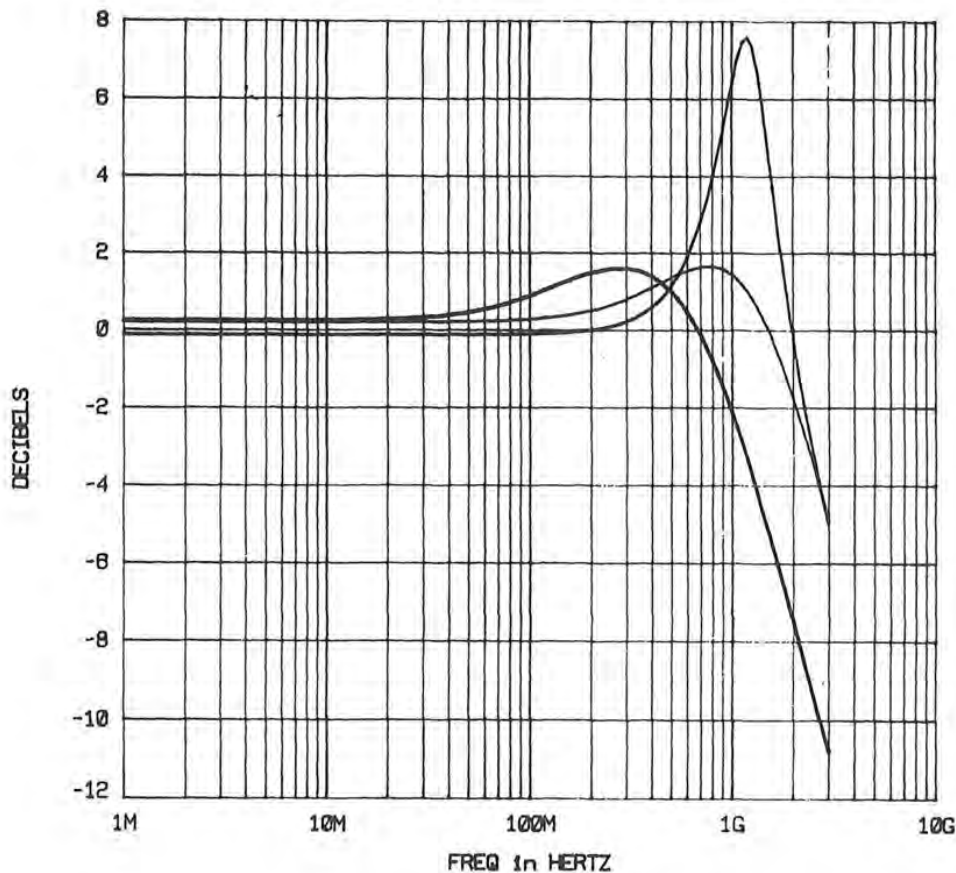


Figure 6.21 Comparison of AC responses of the three most popular mirrors: the Wilson is the most peaky; the EFA mirror has about half the bandwidth of the basic mirror, but the same 1.8dB of peaking.

0.26Ω for $I_1 = 1\text{mA}$. At high frequencies, the circuit becomes resonant (at about $f_T/3$) but Z_3 remains under 10Ω up to about $f_T/10$. Of course, device capacitances play a more important role at lower currents. Figures 6.19 and 6.20 show typical results for a circuit using equally-sized transistors with an f_T of about 3GHz. The flatness of both the impedance and the AC transfer function, with respect to this non-standard input, can be improved by the addition of a small capacitor across the collector-base junction of Q1.

While on the subject of AC response, we show in Figure 6.21 a comparison of the three most popular current mirrors: the basic mirror, the EFA mirror and the Wilson mirror. In all cases, equal transistor geometries were used, typical of a 3GHz NPN process, operating at a bias current of 1mA and without the use of emitter degeneration. The severe peaking of the Wilson mirror is apparent. In designing mirrors for current-path applications, much can be done to control the gain and phase response. In fact, the first

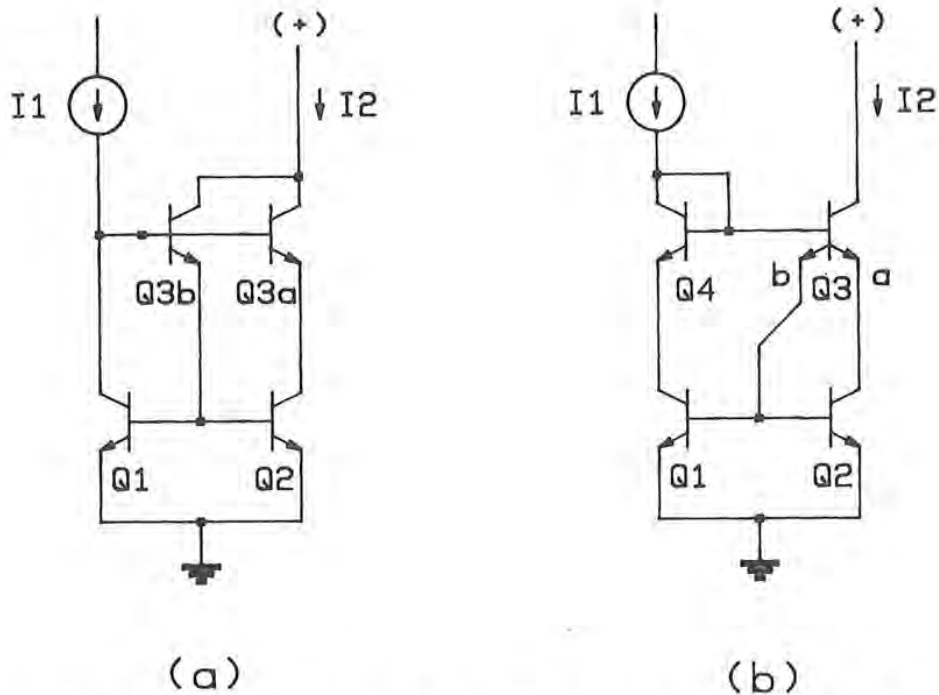


Figure 6.22 Improvements to the Wilson mirror: (a) separate path to bases of $Q1$ and $Q2$ lowers peaking in AC response; (b) extra diode $Q4$ lowers static errors due to V_{CB} mismatch between $Q1$ and $Q2$.

improvement to the Wilson mirror to be described has a flatter HF response as one of its benefits.

Figure 6.22a shows the circuit, in which an extra transistor $Q3b$ has been added to $Q3$ to supply the base currents of $Q1$ and $Q2$; in practice, this would simply be an additional emitter, as shown in Figure 6.22b. Figure 6.23 shows a useful improvement in the AC response. This is due to the radical alteration of the incremental resistance driving the common-base node. In the basic Wilson mirror, this resistance is the r_e of $Q3$; in the modified circuit it is increased by the factor $\beta/2$, thus forming a pole with the C_π of $Q1$ and $Q2$ at a much lower frequency, resulting in a more stable feedback path.

This modification has a second advantage, only of interest in low-voltage applications, which is that it allows the output node to drop closer to the common node before finally crashing (Figure 6.24). A more important improvement is the addition of an extra diode-connected transistor, $Q4$, in series with the collector of $Q1$ (Figure 6.22b). Its purpose is to equalize the V_{CB} of $Q1$ and $Q2$ and thereby remove a significant source of error in the mirror ratio. The magnitude of this error is quickly estimated: a ΔV_{CB} of one V_{BE} can be shown to alter the ratio of the sub-cell $Q1/Q2$ from unity to

$$M' = \exp(V_{BE}/V_{AF}) \quad (6.26)$$

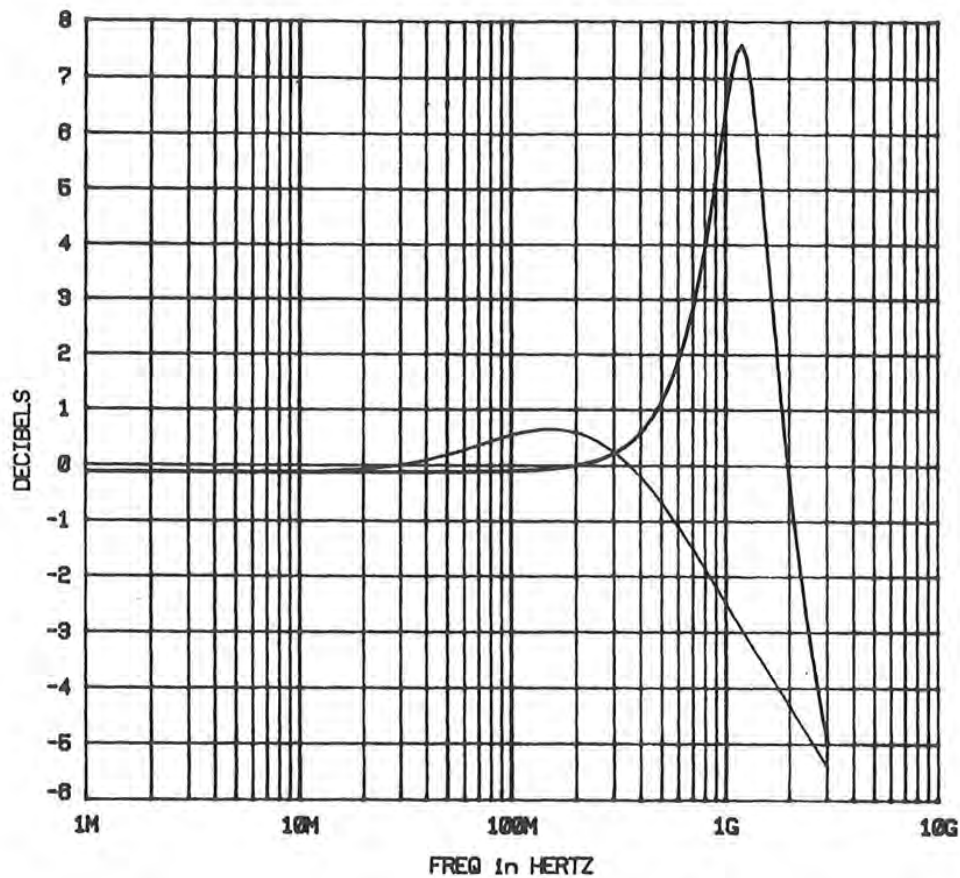


Figure 6.23 Reduction of HF peaking for the Wilson variant of Figure 6.22a.

which evaluates to about 1.007 for $V_{AF} = 100V$, and causes the output of the complete mirror to 0.7% too low. An approximate compensation can be provided, when the operating current is constrained to some small range, by replacing Q4 with a resistor.

The sub-cell can be rendered more accurate by the use of cross-connected transistors physically arranged on the chip as a quad [7]. This would be useful when a wide current range is to be handled, or when it is important to keep excess voltage drops to a minimum, but a narrow current range, and where headroom considerations allow, it is usually preferable to use emitter degeneration to improve the ratio accuracy.

6.5 Special-purpose Current Mirrors

It will be apparent that the idea of a "current mirror" has many extensions, and we will end this Chapter with a brief consideration of some of these; we

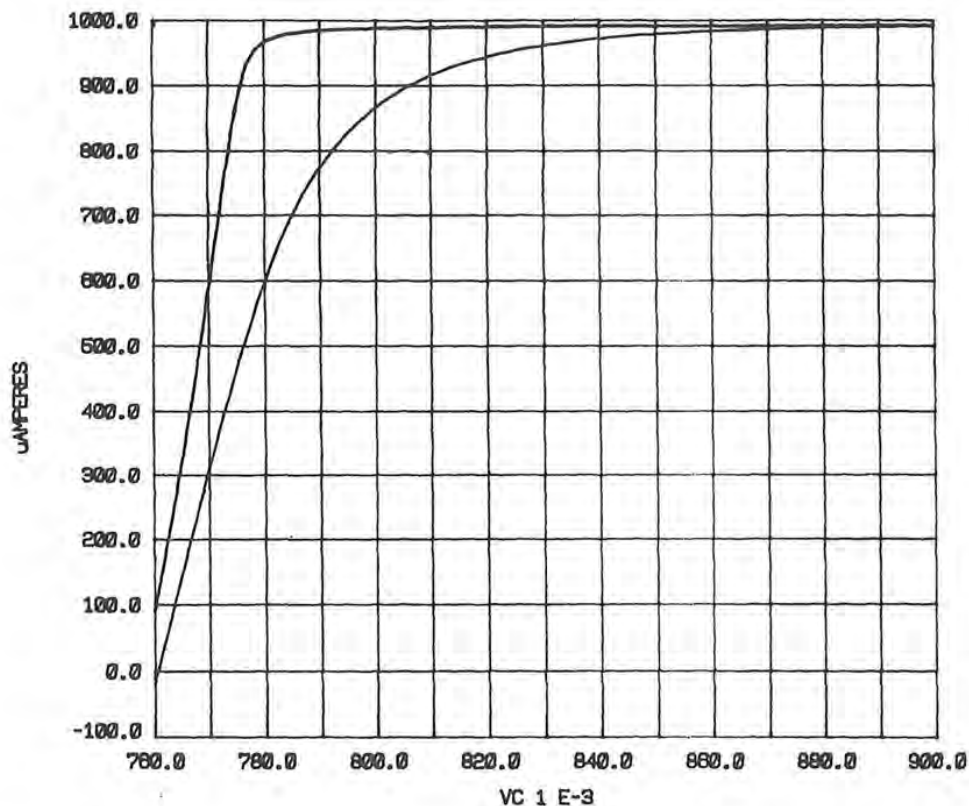


Figure 6.24 Improved low-voltage behavior for the variant of Figure 6.22a.

will touch upon the subject of current-mode amplifiers based on mirrors, which have many possible forms. Contemporary complementary bipolar processes are a great asset in this context; we will show a basic scheme which allows signals to be "ping-ponged" between two very low-voltage supplies, accruing gain in the process. Mirrors have also played a traditionally important role in op-amp design (in converting differential current signals from the input gm stage to single-sided form prior to the integration stage) and as active loads [1]. We will here consider a few generic forms that may be useful in special circumstances.

6.5.1 Variable-Ratio Mirrors

All the mirrors so far discussed have a current ratio which is fixed, either by emitter-area ratios alone, or in combination with resistor ratios. Often it is desirable to be able to control the mirror ratio in some other way, for example, by varying a current or voltage. Clearly, such circuits overlap the domain of multipliers, and many similarities are found; the differences are largely in the way in which we approach the form.

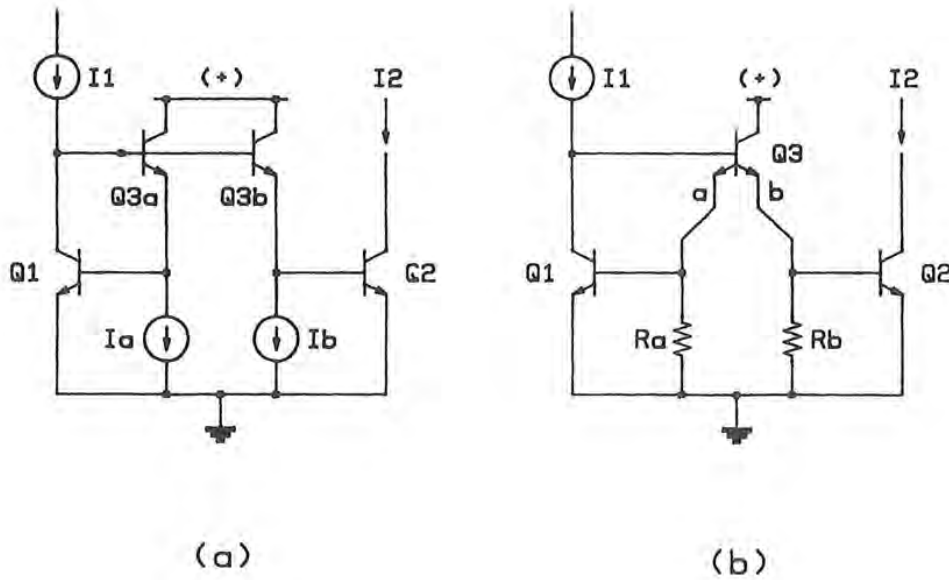


Figure 6.25 Variable ratio forms: (a) current-programmable; (b) resistor-programmable.

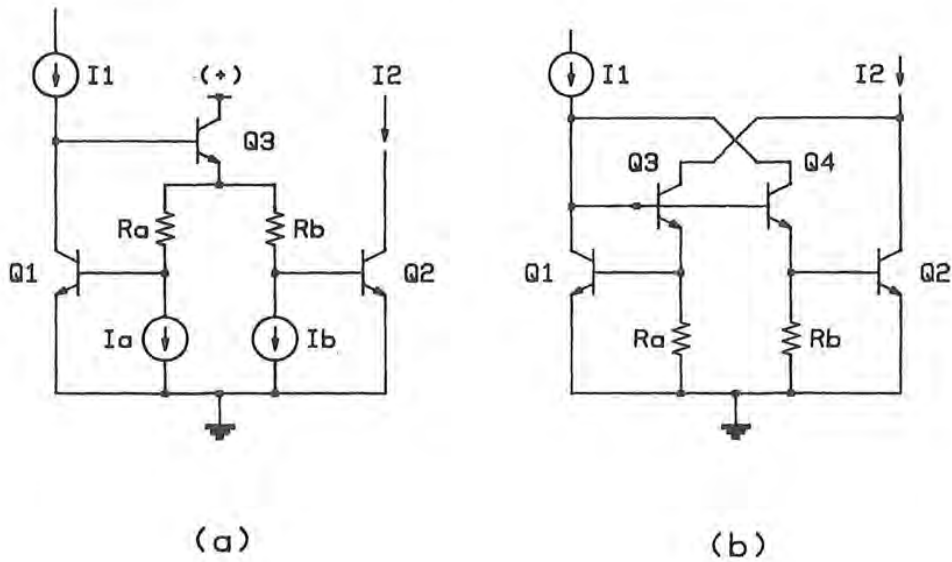


Figure 6.26 Further variable-ratio mirrors. The variant in (b) also exhibits a very high output resistance, through cancellation of the similar dependence of the V_{BE} of Q3 and Q2 on the output bias.

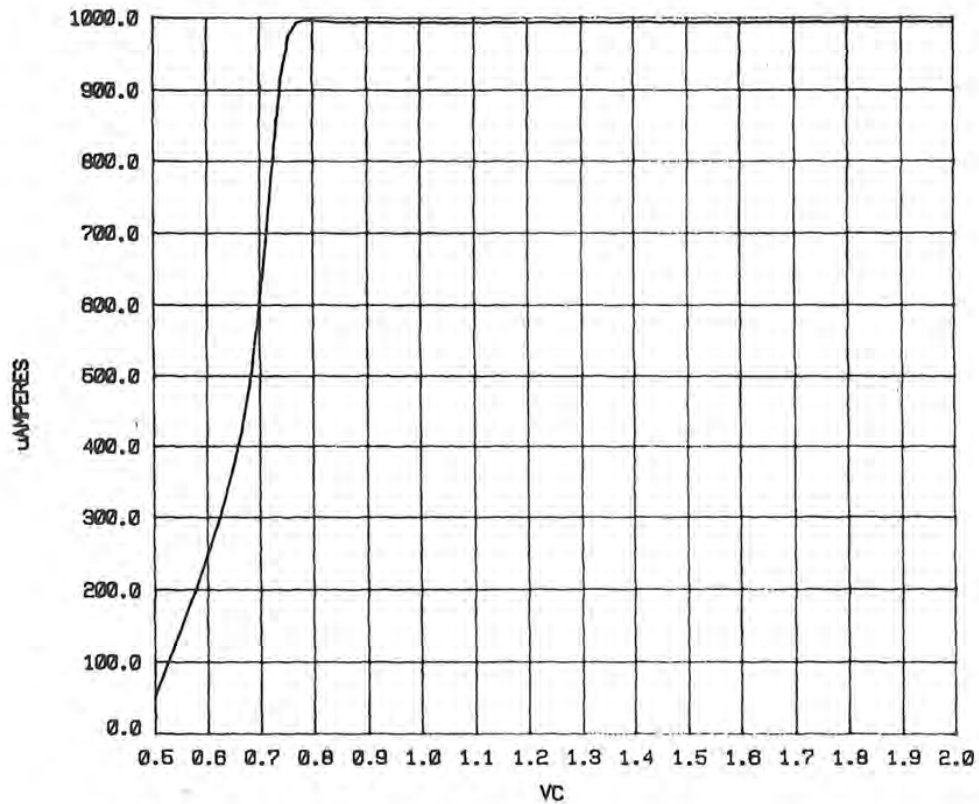


Figure 6.27 Output current of the circuit of Figure 6.26b at low voltages.

Figure 6.25a shows a cell that illustrates this ambiguity: it can be viewed as a simple one-quadrant translinear multiplier, or as a slight variant of the EFA current mirror (it would be exactly that if the two emitters of Q3 were shorted). The use of separate current biases to Q3a and Q3b allow us to control the mirror ratio, which, neglecting errors due to beta, is now

$$M = \frac{I_a}{I_b} \quad (6.27a)$$

In Figure 6.25b, the use of a single two-emitter transistor for Q3 illustrates a practical simplification: in this case, the current sources have been replaced by resistors Ra and Rb, allowing resistor control of the mirror ratio:

$$M = \frac{V_{BE1}/R_a}{V_{BE2}/R_b} \approx \frac{R_b}{R_a} \quad (6.27b)$$

In this case, the final ratio is not exact, because the V_{BE} of Q1 and Q2 are, in general, no longer equal.

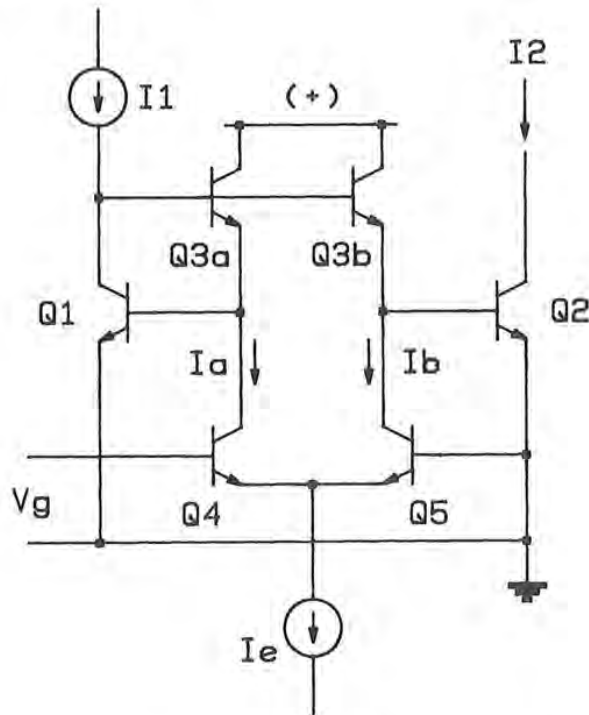


Figure 6.28 A variable current-gain cell with “linear-decibel” response and a practical range of -40dB to +20dB.

A more useful variant is shown in Figure 6.26a, where the differential voltage across the bases of Q1 and Q2 can be controlled by the currents Ia and Ib. The mirror ratio in this case is

$$M = \exp \frac{I_a R_a - I_b R_b}{V_T} \quad (6.28)$$

Stable operation over temperature requires that either the resistors or the currents be PTAT.

A further variant is shown in Figure 6.26b. In this case, the controllable ratio is effected in the same way as in Figure 6.25b, except that separate transistors Q3 and Q4 are used and their collectors have been cross-connected, which results in the V_{BE} of Q3 responding to the output bias (V_{C2}) in almost exactly the same way as the V_{BE} of Q2. Since these two devices are facing in opposite directions in the TL loop the output resistance is very much higher than it would be without this feature. Figure 6.27 shows the output characteristic from 0.5V to 2V; the current very rapidly attains its final value, beyond which point the incremental output resistance is much higher than that of the Wilson mirror.

A current-mirror having a voltage-variable ratio is shown in Figure 6.28. This will be recognized as another twist on the basic form shown in Figure

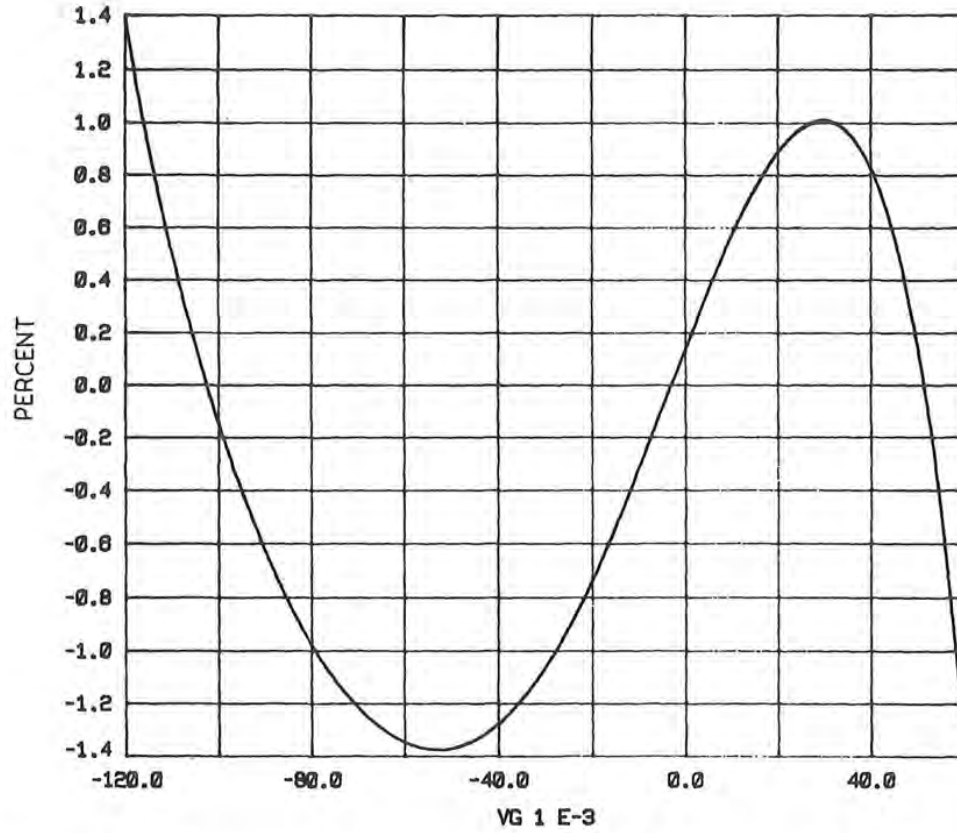


Figure 6.29 Percentage error in the mirror ratio for the circuit of Figure 6.28 is less than $\pm 1.4\%$ from $V_g = -120\text{mV}$ (-40dB) to $+60\text{mV}$ ($+20\text{dB}$).

6.25a. In this case, the currents I_a and I_b are provided by Q4 and Q5:

$$I_a = \frac{\exp(g)}{\exp(g) + 1} I_e \quad (6.29a)$$

and

$$I_b = \frac{1}{\exp(g) + 1} I_e \quad (6.29a)$$

where $g = V_g/V_T$. It follows from Eq. 27a that

$$M = \exp(g) \quad (6.30)$$

Thus, the decibel gain or loss is a linear function of the control voltage V_g .

Figure 6.29 shows that the gain error in a practical realization of this concept remains within $\pm 1.4\%$ from $V_g = -120\text{mV}$, corresponding to a loss

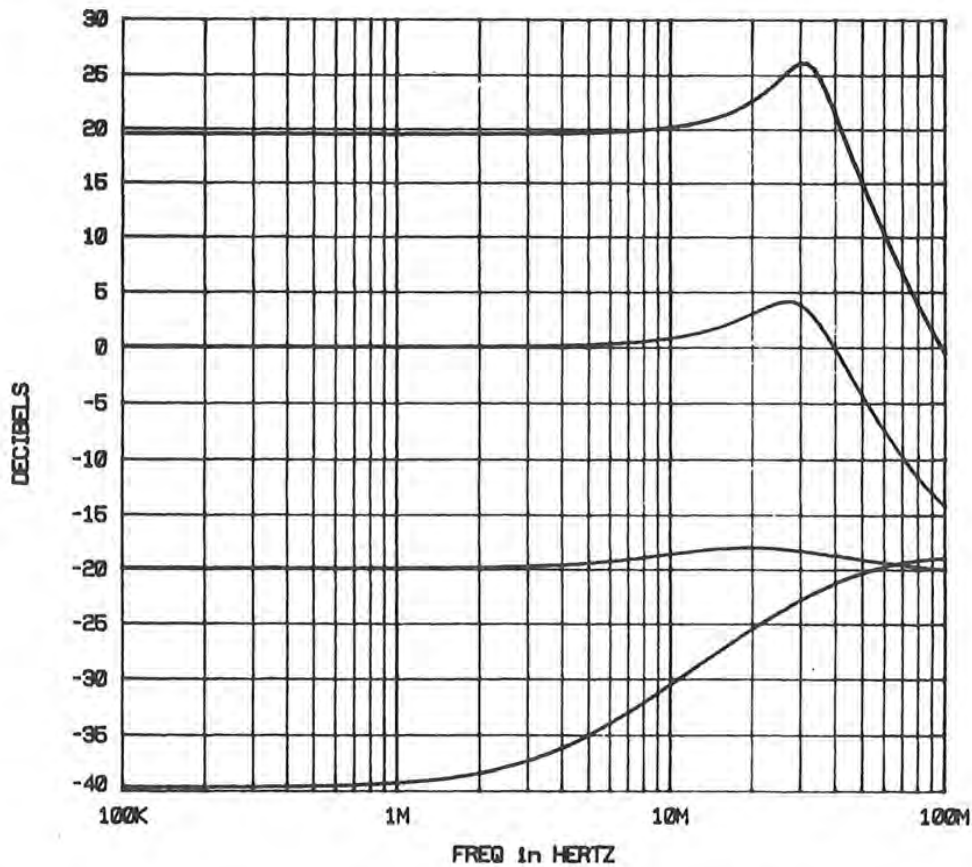


Figure 6.30 AC response for the circuit of Figure 6.28 at four gain settings.

of 40dB at $T = 300\text{K}$, up to $V_g = +60\text{mV}$, which provides a gain of 20dB. Some adjustment of emitter areas was used to achieve this result, for which the bias currents were $I_1 = 15\mu\text{A}$ and $I_e = 600\mu\text{A}$. The AC response for a 3GHz IC process operating under these conditions is shown in Figure 6.30. Some peaking is evident at the higher gains, and signal feedthrough limits HF performance at high attenuations. Nevertheless, this novel circuit may have applications in certain types of gain control, particularly since it can be extended using a complementary bipolar process to handle "two-quadrant" signals.

6.5.2 Mirrors Having Large Current Ratios

There is no particular difficulty in achieving high mirror ratios. In many cases, simple emitter area ratios will suffice, supported by current gain if necessary (as in the EFA mirror, which is not limited to the use of a single

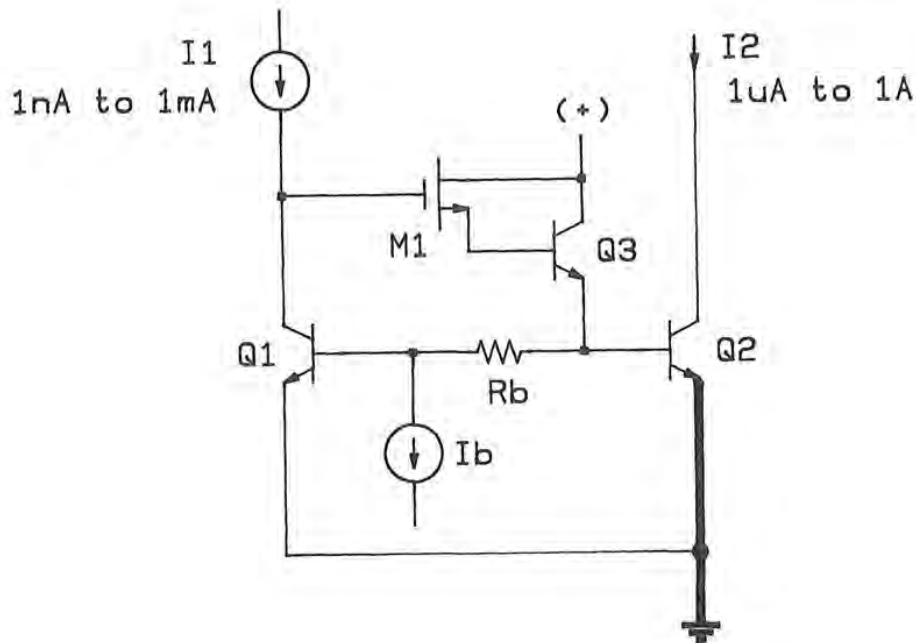


Figure 6.31 A method for augmenting the area ratio (100:1) between Q2 and Q1 to achieve a very high mirror gain at high current.

transistor for current boosting). In practical monolithic designs, emitter area ratios of up to 100:1 are not hard to achieve. Beyond that, one might wish to use some of the ideas presented in the last section: although the focus was on providing variable mirror ratios, it is evident that large ratios can be achieved by introducing fixed voltage offsets between the bases of an EF mirror. Figure 6.31 shows a mirror having a ratio of 1000:1, partly achieved by the use of a large area for the output device, Q2, needed anyway to handle the maximum current of 1A, and partly by the insertion of 59.5mV generated by I_b across the resistor R_b . To maintain an accurate ratio over temperature either I_b or R_b must be PTAT; at the relatively low value required here, R_b could be fabricated from the aluminum metallization (see Chapter 2 for a similar situation), allowing I_b to be fixed with temperature. Many practical ways exist to introduce the needed ΔV_{BE} to good accuracy. Note that the maximum base current of Q1, assuming a beta of 100 and a maximum I_{C1} of 1mA, will cause the peak output to be 1% too high. A combination of MOS and BJT is used to provide the large peak base current of Q2, and also maintain low errors at the smallest input of 1nA. Special attention is directed to the grounding of the emitters of Q1 and Q2; at high currents only a few tens of milliohms of improperly-located aluminum interconnect can severely degrade accuracy.

We have already seen how one can devise mirrors to generate a moderately small current from a larger one, using nonlinear mirrors, but suppose one needed a linear mirror to generate an accurate current only

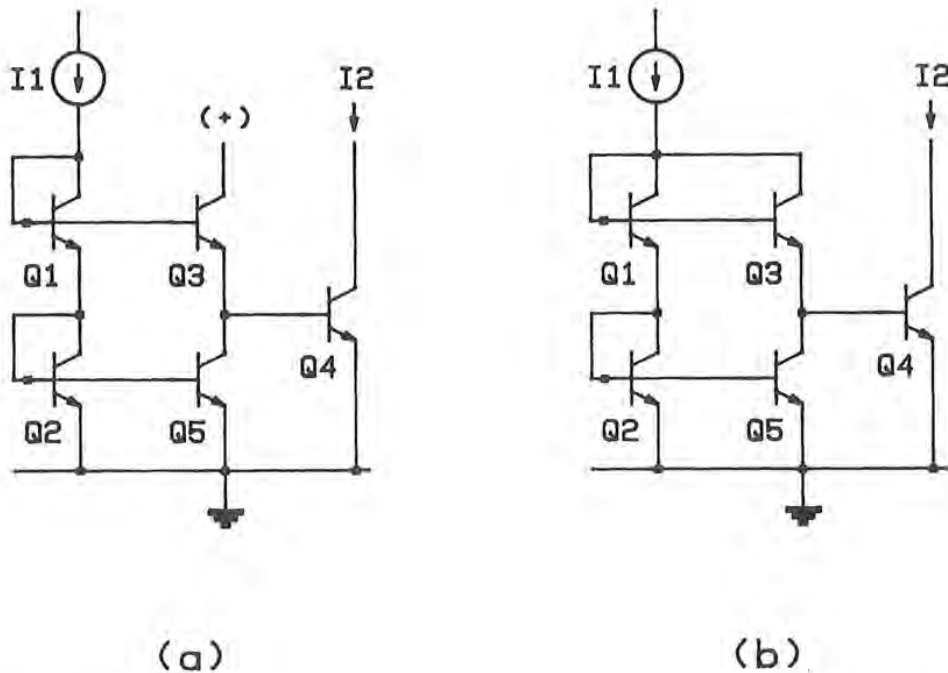


Figure 6.32 Translinear mirror cells with capability for very high ratios.

1/1000th as large as its input over a wide range. This is the inverse of the last problem, and although there are few applications for such a function, it is a useful point of departure in showing that the current mirrors we have discussed so far are only the simplest of a more general class of translinear-loop (TL) circuits.

Figure 6.32 shows two more complicated mirrors, differing only in the biasing of the collector of Q^3 . It is easily determined using the translinear principle that the mirror ratio of the (a) variant is

$$M = \frac{A_3 A_4}{A_1 A_5} \quad (6.31a)$$

while that of the (b) variant is

$$M = \frac{A_2}{A_2 + A_5} \frac{A_3 A_4}{A_1 A_5} \quad (6.31b)$$

(The reader might wish to verify that the absence of A_2 in Eq. 6.31a is not an error in analysis; it suggests that in the ideal case $Q2$ could be omitted. Is this correct?). These composite quotients make it easy to realize very large mirror ratios, and if beta were not finite, it would be as easy to have $M > 1$ as $M < 1$. In practice, the form is limited to operation with $M < 1$. With quite

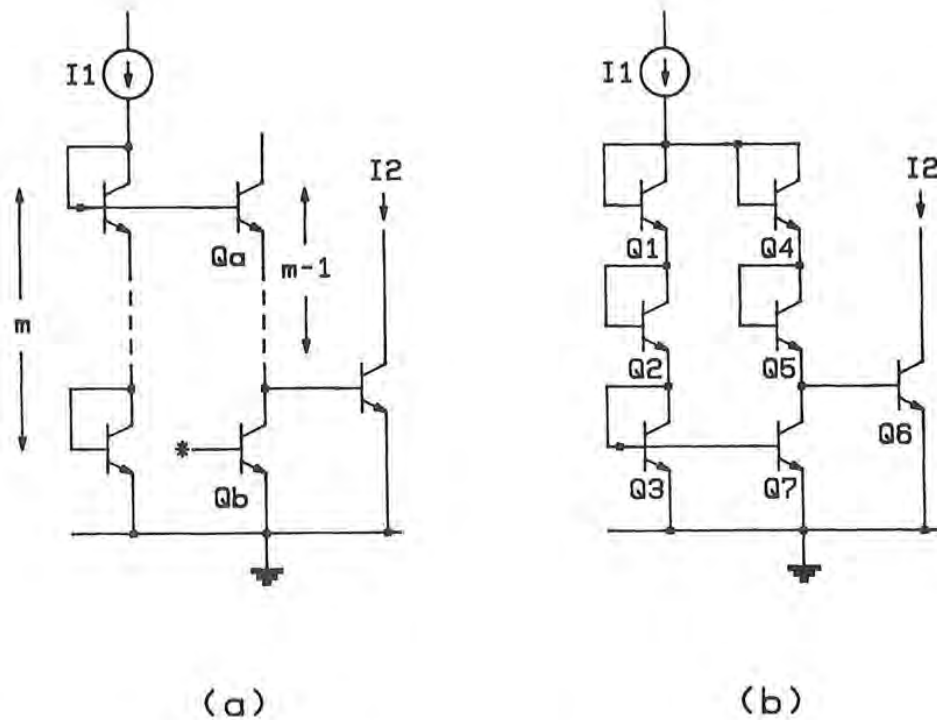


Figure 6.33 (a) The “general current mirror” and (b) an example using $m=3$.

moderate emitter areas, the (b) variant can realize exact attenuation ratios of several thousand.

Figure 6.33a shows the general form of these mirrors. Since the collector of Q_a can be connected to (1) the input node, (2) the output node or (3) a supply voltage, and the base of Q_b can be connected to (a) the base of the input diode or (b) the base of the output transistor, there are six further variants. Figure 6.33b shows a typical example, where $m = 3$. Its mirror ratio is

$$M = \frac{A_3^2 A_4 A_5 A_6}{(A_3 + A_7) A_7^2 A_2 A_3} \quad (6.32)$$

An interesting (but probably valueless) outcome of this is that one can generate a maximum attenuation ratio of 187272:1 using only 33 unit emitters. The reader is invited to find the minimum number of unit emitters required to achieve an attenuation ratio of one million, using this or any other form that preserves the ratio over a wide current range.

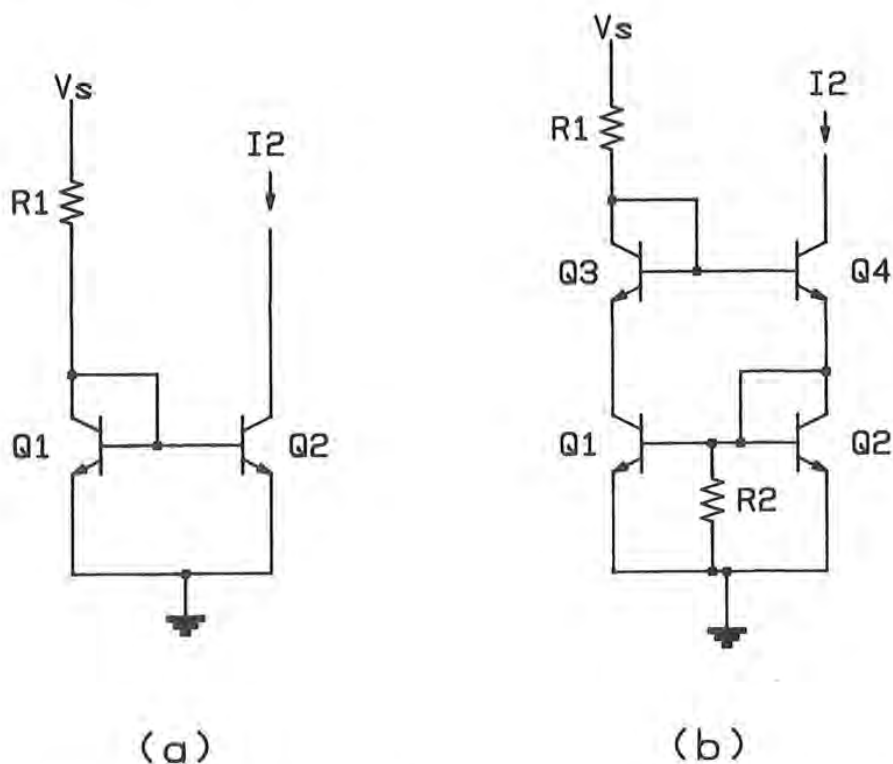


Figure 6.34 Supply-energized current-sources: (a) does not provide an output which is proportional to V_S ; the circuit shown in (b) does.

6.5.3 Supply-Tracking Current Sources

It is occasionally required to generate a current which is exactly proportional to a voltage. Numerous methods exist to achieve this, and where accuracy is of paramount concern, operational amplifier techniques are often employed. In many cases, however, simpler techniques not only suffice but can operate under conditions not possible using "high-level" solutions.

For example, suppose one wished to generate a current which was to be used as the scaling voltage for a nonlinear function, such as a multiplier or logarithmic amplifier, and the circumstances were such that this must track the supply voltage, V_S , with an accuracy of better than "8-bits" (0.25%) over the temperature range -55°C to $+125^{\circ}\text{C}$. This situation might arise if V_S were also to be used as the reference for a subsequent A/D converter. Then a simple mirror, resistively biased from the supply, such as shown in Figure 6.34a, would not be appropriate, partly because its current-in/current-out ratio is not very accurate, but more importantly because the voltage across R_1 is not the full supply voltage, but only $V_S - V_{BE}$. If we use an EFA or Wilson

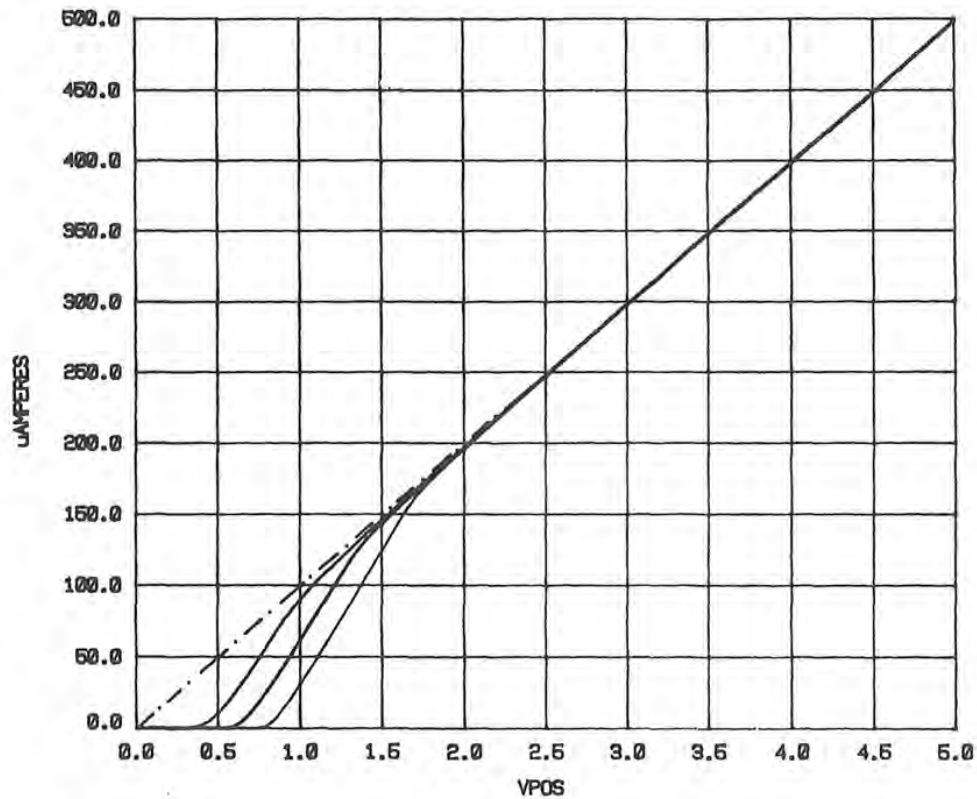


Figure 6.35 Demonstration of the very close proportionality in the output current (Figure 6.34) at -55°C , 25°C and 125°C .

mirror to deal with the basic accuracy issues, the deficit is doubled, that is, the output current is

$$I_2 = (V_S - 2V_{BE})/R_1 \quad (6.33)$$

However, Figure 6.34b shows how this problem can be sidestepped. An extra resistor, R_2 , has been added, in which flows a current V_{BE}/R_2 , which adds to the output:

$$I_2 = (V_S - 2V_{BE})/R_1 + V_{BE}/R_2 \quad (6.34)$$

Thus, when $R_2 = R_1/2$ the output current is proportional to V_S , although not tracking it all the way down to zero. Note that the "recovered" V_{BE} is exactly equal to the "lost" V_{BE} 's, ensuring accurate compensation. The effectiveness of this solution can be judged from Figure 6.35 which shows the output for a circuit using $R_1 = 10\text{k}\Omega$ from $V_S = 0$ to $+5\text{V}$ at -55°C , $+35^{\circ}\text{C}$ and $+125^{\circ}\text{C}$. R_2 was set to $4.9\text{k}\Omega$, slightly lower than theoretically required, to further reduce the already low temperature coefficient, which is now about

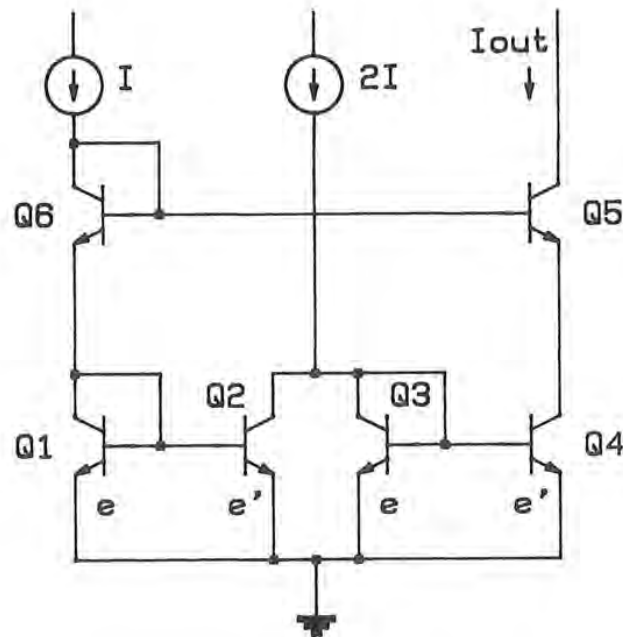


Figure 6.36 A novel circuit capable of extremely high output impedance.

40ppm/°C at $V_S = +2V$, 5ppm/°C at $V_S = +3V$ and only 2ppm/°C at $V_S = +5V$. The output error drops below $2.5\mu A$ for supply voltages as low as +2.5V, even at the minimum temperature.

6.5.4 Mirrors Having Very High or Negative r_o

Many methods can be devised to increase the output resistance r_o of a current mirror. To remain within the subject of bipolar mirrors, we will exclude those methods depending on the use of MOS cascodes. Two novel techniques are proposed, each having certain merits.

The circuit shown in Figure 6.36 can exhibit remarkably high output resistance, and because the cascode transistor, Q5, can have a small geometry, the output capacitance can be low, too. The two merits of this scheme are

- 1) The output resistance can be infinite and with practical tolerances held to many hundreds of megohms (positive or negative) at 1mA. Stated more generally, the Thevenin equivalent voltage can be reliably as high as 100 times the βV_{AF} product, typically 1 megavolt.
- 2) The output can approach the common terminal to within much less than one volt while still exhibiting the maximum value of r_o .

The disadvantages are:

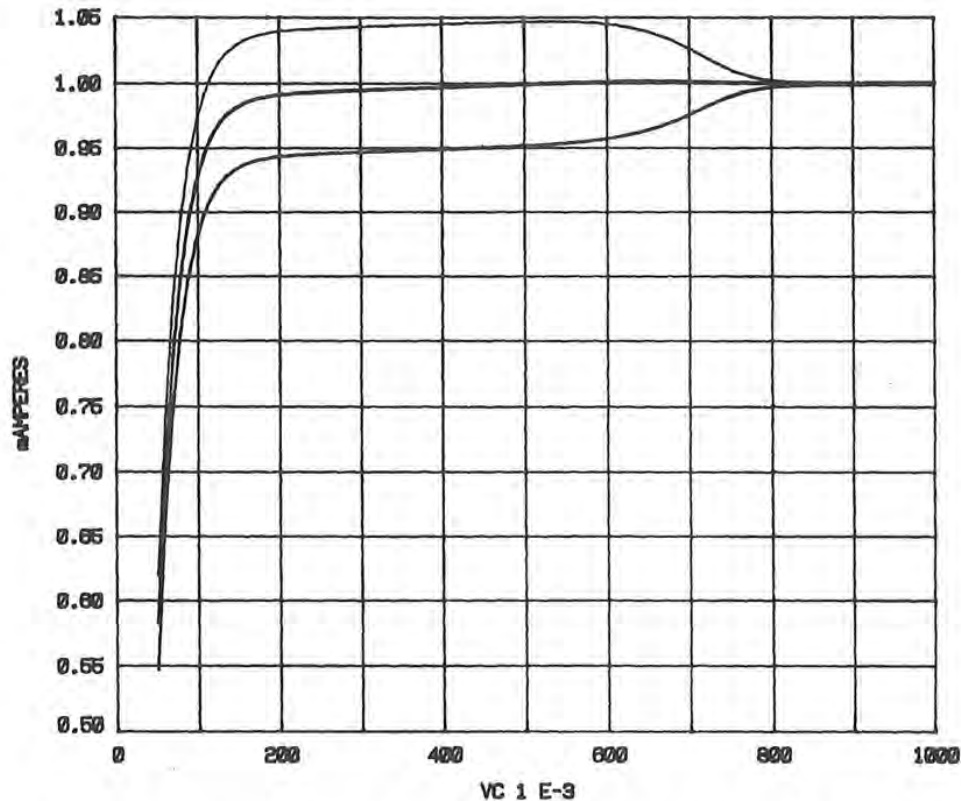


Figure 6.37 Output current versus output bias voltage (Figure 6.36), with a small adjustment to the ratio e'/e . (See text.) Note that the current is quite accurate even down to +100mV of bias.

- A) It requires two input currents; in fact, the output is the difference of these currents, but only to full accuracy when they are in the 2:1 ratio shown in the figure.
- B) The two inputs are at different potentials; this is easily remedied by the addition of another diode-connected transistor.
- C) The technique relies on good matching of beta.

The basic idea is to return the base current of Q5 through the unity-gain mirror Q1/Q2 to the input of the second unity-gain mirror Q3/Q4, and hence add this base current back to the effective input $2I - I$. The full analysis will not be given here, but it will be found that the beta errors of the two simple mirrors cancel. Now, in a practical implementation, it may happen that the emitter-area ratios of these mirrors may be slightly mismatched, as shown by the area factors e and e' in the figure. If we properly arrange these four transistors into a cross-connected quad, we can arrange for the ratio e'/e to

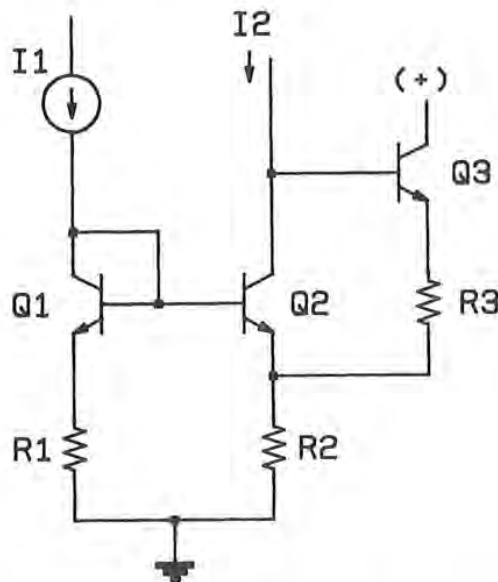


Figure 6.38 A simple circuit providing adjustable output resistance through infinity to negative values.

be very nearly equal for both mirrors. Under such conditions the absolute accuracy of the output and r_o remain very high even for quite large variations in e'/e . The following table was generated by simulation, for $I = 1\text{mA}$, $\beta = 100$, $V_{AF} = 100$:

Ratio e'/e	I_{out} at $V_{C5} = +5\text{V}$ (mA)	r_o ($\text{M}\Omega$)
1.00	0.9991	130
1.02	0.99995	284
1.04	1.00006	-1330
1.06	0.99944	-196
1.08	0.998	-105

The peak output (1.00014mA) occurred for $e'/e = 1.036$, which was also the value at which the output resistance passed through infinity. The sensitivity to the beta of Q5 was least at this value; I_{out} varied from 0.99985mA at $\beta = 50$, peaked at 1.00014mA at $\beta = 80$ and fell to its starting value at $\beta = 200$. Predictably, the temperature sensitivity of the simulated circuit was negligible.

An interesting feature of this circuit is its behavior at low output voltages, V_{C5} . When Q5 saturates, its base current increases rapidly; but the feedback path works to cancel this error, with the result that I_{out} holds up well, even when V_{C5} is only +100mV! Further, it was found that the ratio e'/e had about

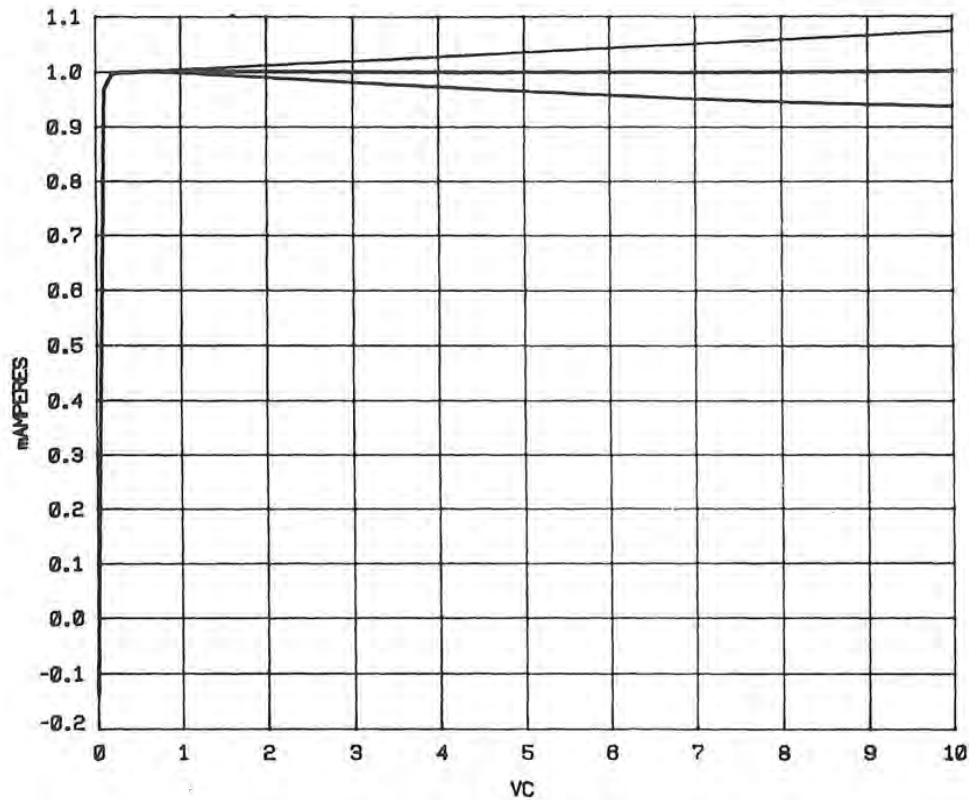


Figure 6.39 Output characteristic (Figure 6.38), showing variable r_o .

the same optimal value for this purpose, too. Figure 6.37 shows I_{out} in the region of V_{C5} from +50mV to +1V, for $e'/e = 1.00, 1.04$ and 1.08 .

Figure 6.38 shows another method for allowing the output resistance to be adjusted through infinity. In this case, a sample of the voltage at the output node is fed back to the emitter of Q2, via Q3 and R_3 . (This is an application where an MOS device would be better suited for Q3.) The theoretical value of R_3 depends on *a priori* knowledge of V_{AF} , hence the circuit is not truly designable. Nevertheless, it is of some interest in that it can provide a strongly negative output resistance, if desired. Figure 6.39 shows a simulation in which $R_1 = R_2 = 10\Omega$, and R_3 was either omitted (positive r_o), set to $26k\Omega$ (the theoretical value for infinite r_o when $V_{AF} = 100V$) or set to half the ideal value.

6.5.5 Voltage-following Mirrors: The GCM

In 1975 the author proposed^[7] a type of current mirror in which the input node (N1 of Figure 6.1a) followed the output node, N2. The application of this was in loading the collectors of a differential translinear cell (usually, a

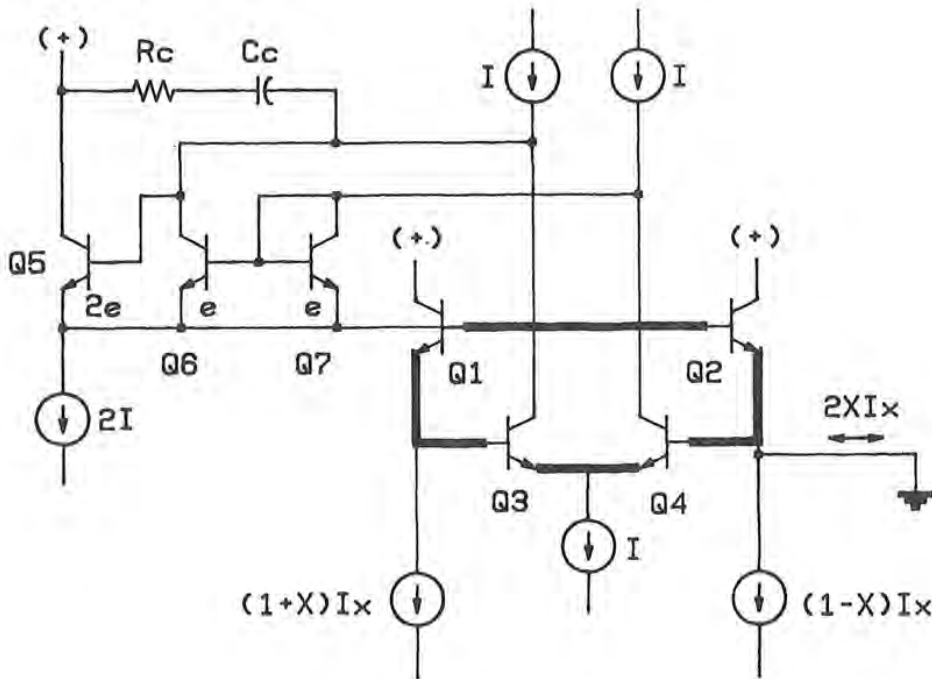


Figure 6.40 A wideband negative current mirror ("GCM").

multiplier) so as to convert the differential current output to a single-sided form, while simultaneously maintaining close equality in the voltage on these collectors, important to achieving very low distortion in certain case. This type of mirror has since been loosely termed the "GCM" (Gilbert current mirror) for want of a better name.

The original version of the circuit used lateral PNPs, but managed to bypass them at high frequencies. Seevinck suggested an all-NPN method of loading the main translinear cell^[8] reproduced here, slightly altered, as Figure 6.40. Transistors Q1, Q2, Q3 and Q4 form a translinear loop, shown by the bold line, in which Q3 and Q4 ideally operate at identical currents, I . Consequently, Q1 and Q2 are forced to operate at equal currents, essentially the "half-input" current $(1+X)I_x$. It follows directly that the current into the load must be this current, replicated in Q2, minus the other "half-input" $(1-X)I_x$, which amounts to just $2XI_x$.

The GCM has some nice features: note, for example, that the base current of Q3 is added to the signal $(1+X)I_x$, but a nominally-identical current is later subtracted at the base of Q4. Also, the collectors of Q1 and Q2 may be

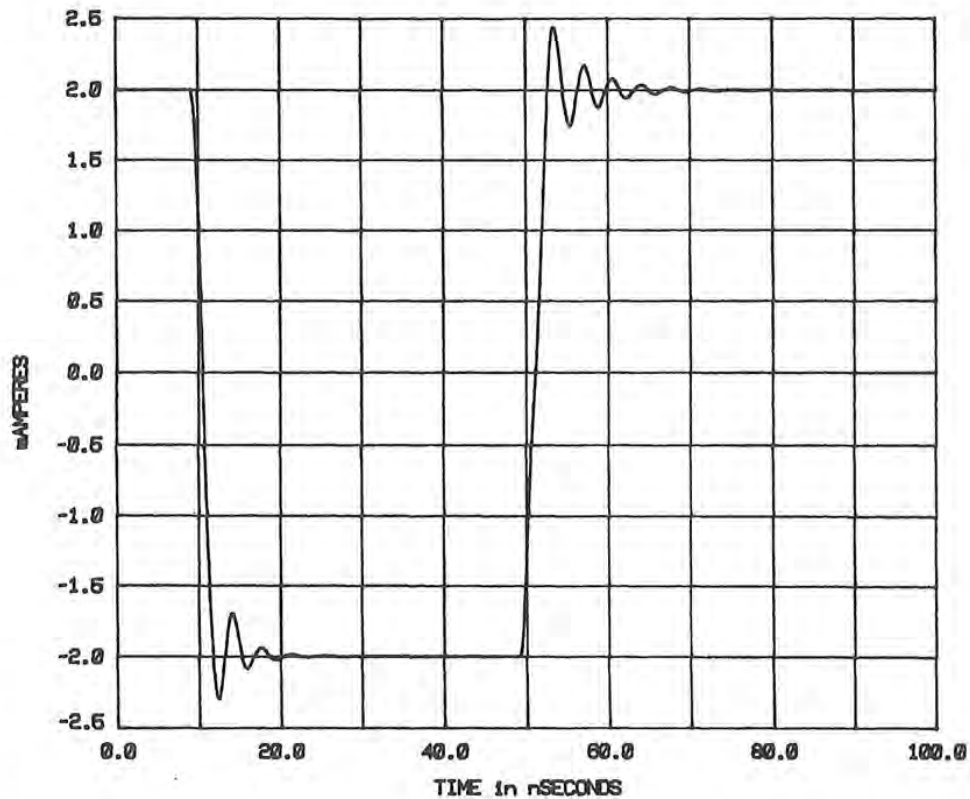


Figure 6.41 Typical transient response for the GCM.

taken to the full positive supply (to maximize the f_T of these devices) will have little concern for supply-sensitivity, because of the inherent balance of the circuit. HF compensation has been added (R_c and C_c), without which the circuit will be unstable over a wide range of tail currents. In a recent simulation, based on a 3GHz IC process, the following parameters were used: $I_x = 1.5\text{mA}$ (to comfortably handle a $\pm 1\text{mA}$ signal modulation, although the GCM operates right up to the limits with very low distortion); $I = 250\mu\text{A}$; $C_c = 3.5\text{pF}$, $R_c = 350\Omega$. The static nonlinearity was less than 0.05%. The input resistance (the effective resistance between the emitters of Q1 and Q2) was $< 40\text{m}\Omega$ up to 100kHz, and less than 1.5Ω at 10MHz. The typical full-scale transient response is shown in Figure 6.41; it shows a rise time of about 2ns. No serious attempt was made to optimize the pulse response. The GCM is worth reconsideration in these days of BiMOS and CB processes.

6.5.6 Applications of Complementarity to Mirrors

Apart from the obvious advantage of permitting "reversed-polarity" mirrors, the availability of high-quality PNP transistors which can be freely

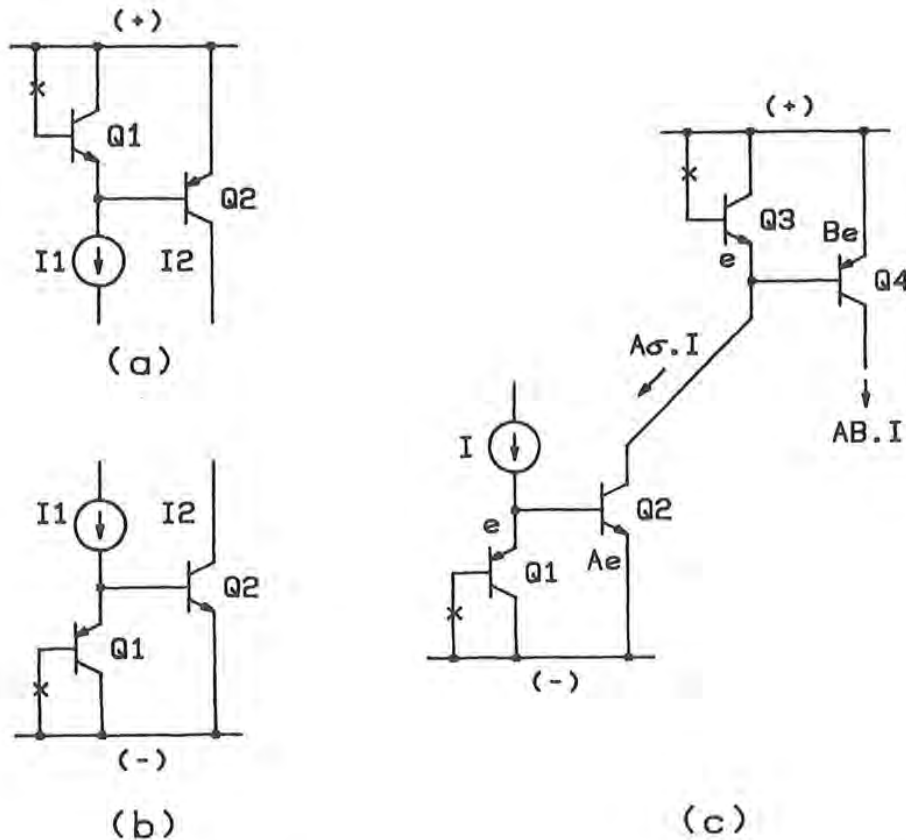


Figure 6.42 Adaptation of the basic current mirror to complementary design. In (a) and (b) the mirror ratio is uncertain; by alternating stages, the ratio accuracy is restored (see text).

mixed into a wideband signal path brings many benefits and encourages the invention of novel topologies, or the dusting-off of old ideas that just could not be realized in pre-CB days. We close this chapter, therefore, with a glimpse of just a few of the possibilities, and begin by introducing the concept of *balance* in a CB process, and proposing the use of a quantitative measure of this balance, the "sigma factor".

In monolithic circuit design, a very large dependence is placed on the reliability of device matching. Over the years, we have learned what to expect of V_{BE} matching, or resistor matching, or beta matching. We've also learned, incidentally, to take advantage of certain dependable correlations, such as that between beta and pinch resistance. Matching is an attribute of like devices. Resistors of a given construction match *because* they are all made in precisely the same way. In complementary bipolar design, however, there is clearly another dimension. The beta, or V_{BE} , or Early voltage, or base resistance, or breakdown voltages of a certain PNP geometry are not

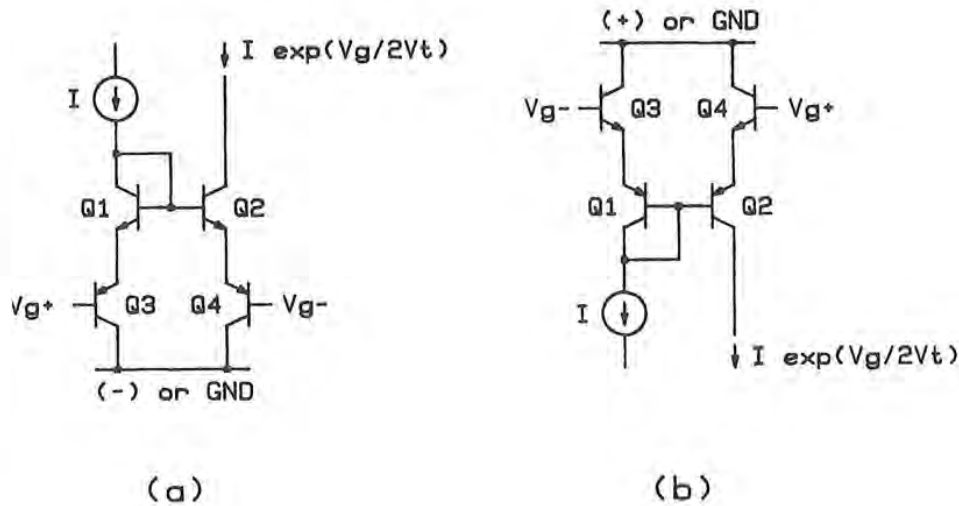


Figure 6.43 Mirrors having current-gain which can be controlled at a differential "high impedance" port.

expected to *match* the corresponding parameter of the NPN.

However, we welcome a high degree of *balance* in a CB process. For example, if the process designer had pushed for the highest possible speed in the NPN, it would probably all be lost if the speed of the PNP were not within a factor of, at most, two. Certainly, it would not help to have the extra NPN speed in making a fast, fully-complementary wideband signal path. It might also have necessitated some other compromises in the NPN performance. Likewise, it would be frustrating to design with PNPs having 40V breakdown voltages if the NPNs could only operate at 5V.

Obviously, balance in a complementary process is a valuable asset, and we might, in an ideal world, wish for it to be perfect, so that, for example, the base currents of an NPN and PNP exactly cancel at an input node. In the present context, we might wish for V_{BES} to be very similar, to allow a stronger interplay between devices and the preservation of accuracy in mixed-polarity mirrors. Such is not the case, but we may find that we can depend on certain parameters to reliably *track* in some way, either over all production lots, or at least over one chip length.

Thus, it is proposed that those parameters in a CB process needing this kind of predictability use a factor, σ , specific to the parameter to quantify the otherwise fuzzy notion of balance. The σ -factors for most parameters, such as beta, Early voltage, BV_{CEO} , and so on, will have a some simple ratio, with a definable mean and standard deviation. It is proposed that in each case, σ is

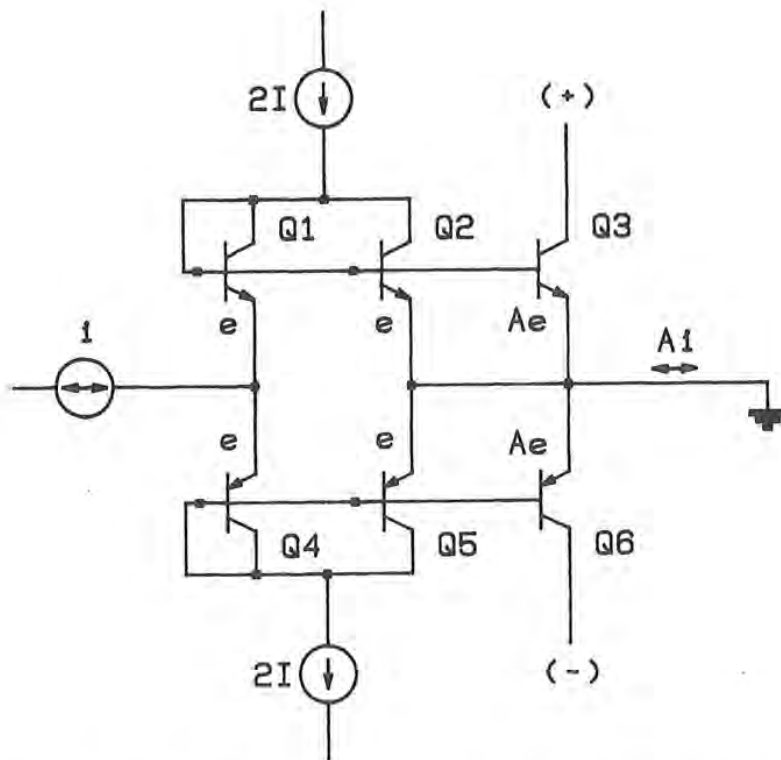


Figure 6.44 A pair of complementary mirrors placed back-to-back, plus another pair of diodes, makes a novel bidirectional mirror.

defined as the ratio of the NPN parameter to the PNP parameter. For translinear circuits, we are interested in current densities, and the appropriate metric here is the saturation current, I_S . Accordingly,

$$\sigma = I_{SN}/I_{SP} \quad (6.35)$$

Now, if we try to make a current-mirror out of mixed polarity devices, as shown in Figure 6.42a and 6.42b, we will find that this factor σ enters into the mirror ratio, which is therefore inexact. However, we can cancel this factor by cascading mirrors of opposite polarity, as shown in Figure 6.42c.

A useful attribute of these mixed-polarity mirrors is that they provide an uncommitted base, shown by the "x" in the above figures, which can be optionally used to voltage-control the ratio. Alternatively, we can avoid the σ -factor by using a circuit such as shown in Figure 6.43a and 6.43b. Here, we are back in the familiar territory of "matching" like against like, but, because of the good translinear properties of modern CB-process PNP transistors, we can confidently apply all the theory presented in Chapter 2. These mirrors come with a further bonus: a differential voltage-input port at which the mirror ratio can be controlled. The reader is invited to think about some of

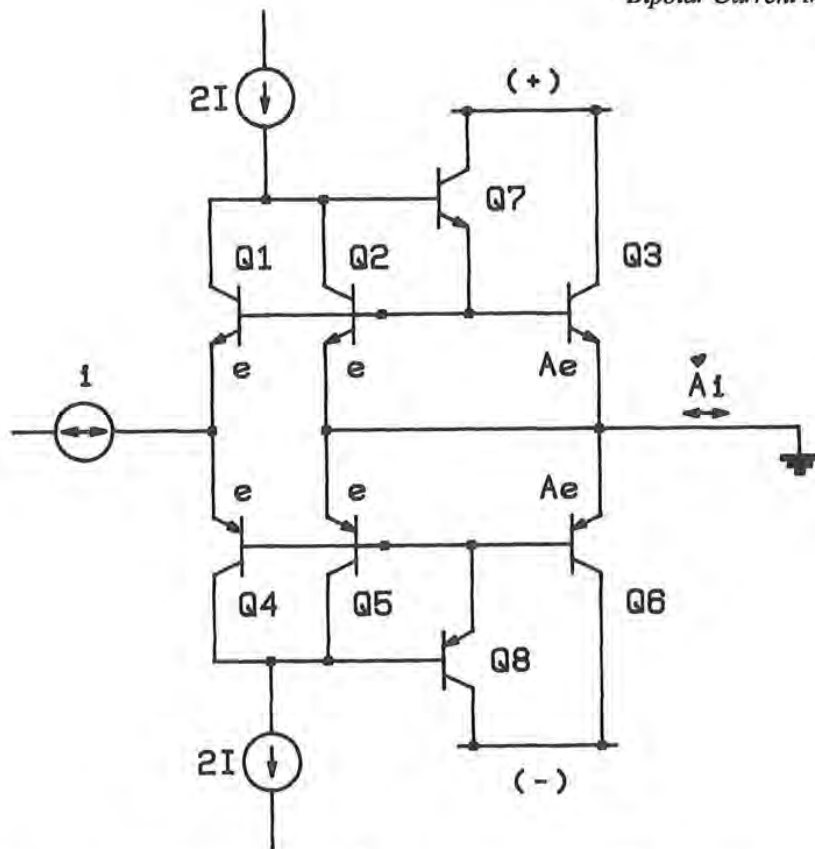


Figure 6.45 A development of the bidirectional mirror, providing higher gain.

the many ways in which this feature can be harnessed.

Finally, we propose a current-mirror form (Figure 6.44) which provides bidirectional current transport and a gain defined, in this case, by a fixed emitter area, A . The analysis follows standard TL practice. Figure 6.45 shows a development of this idea, which can be viewed as two EFA mirrors back-to-back, having the benefit of additional internal current gain to improve accuracy.

There is little doubt that the future of current-mode signal-processing will depend more and more on the unique benefits which are provided by the availability of a "translinear PNP" and the increasing use of complementary design techniques.

6.6 Acknowledgements

Paul Brokaw took a look at an early draft of this material and made some helpful observations, including some about my reckless disregard of rigor in connection with dimensional consistency in certain places (for example, Eqs. 6.15b and 6.16b). Normally, I'd agree, but there are times, I feel, when a simple cook-book formula is of value, and in these cases, a result can be

quickly obtained by "plugging in the numbers" with little risk of fire and brimstone. Alicia and Monica, who thought their job was done after checking over the manuscript for Chapter 2, started all over again when the present Chapter was finally completed at the eleventh hour. My sincere thanks to them for their diligence in digging for my slips, and to Mark Elbert for his useful comments along the way.

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Gallium Arsenide Analogue Integrated Circuit Design Techniques

Chris Toumazou and David Haigh

8.1 Introduction

Many high speed analogue circuits have been developed for bipolar technology. These circuits have generally used current as the main processing variable, and some of them are reviewed in Chapters 2, 4, 15 and 16. Work aimed at extending the maximum frequency capability of CMOS technology, described in Chapters 5 and 9, has also tended to employ current processing techniques. In designs for both bipolar and CMOS technology, a number of key current-based components have been found to be particularly valuable. These include the current mirror (Chapters 6 and 7), the high gain (or operational) transconductance amplifier (Chapter 4) and the high precision transconductor, which provides a tunable linear resistive element for integrated circuit filter realisation as described in Chapter 9.

Modern communication systems, both microwave and optical, are beginning to rely heavily on the high frequency circuit performance capabilities provided by III-V semiconductor materials, of which the most mature is Gallium Arsenide (GaAs). The applications of GaAs can be divided into digital and analogue. The analogue applications can be further subdivided into microwave circuits, and sampled data circuits based on switched capacitor circuit techniques [1]. Both the high quality switches and the high gain, fast settling operational amplifiers required in these systems can be realised using the GaAs Metal Semiconductor FET, or MESFET.

Examination of the designs developed for high speed GaAs analogue sampled data circuits reveals that they too rely extensively on current-processing and utilise a range of high quality fast current-based building blocks. This Chapter presents these building blocks and some of their applications. We include current mirrors (Section 8.3), single-ended to differential converters and differential to single-ended converters (Sections 8.4 and 8.5), a linearisation technique leading to a high quality transconductor (Section 8.6), operational transconductance amplifiers (Section 8.7), and buffer amplifiers (Section 8.8). Section 8.9 covers applications ranging from switched capacitor filters, microwave amplifiers and circuits for optical communication systems.

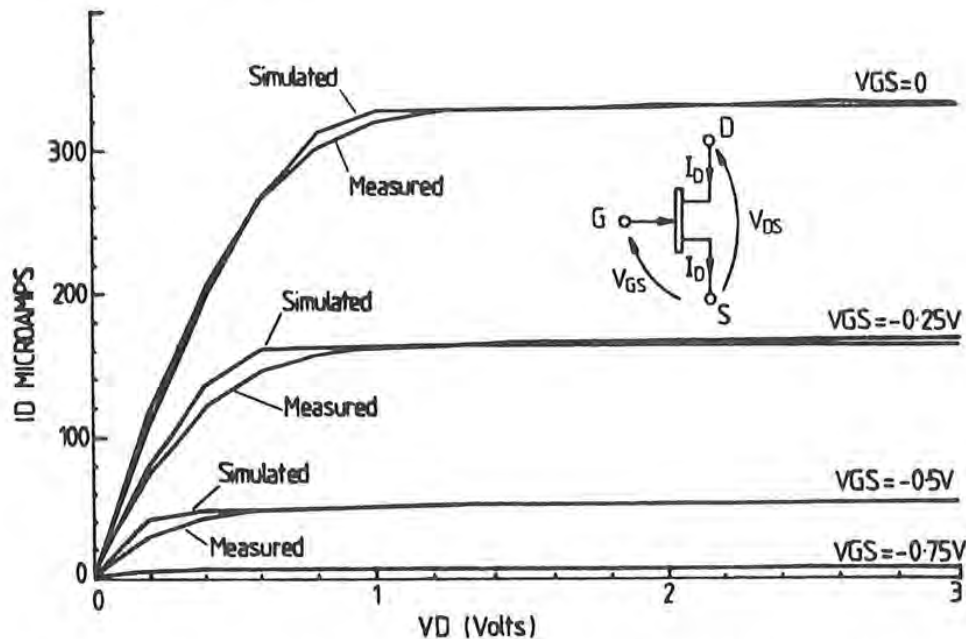


Figure 8.1 Measured and simulated characteristics for typical GaAs MESFET

8.2 Technology, Devices and Simulation

Circuit design techniques are heavily influenced by the fabrication technology involved. High speed GaAs technology is generally regarded as a challenge for circuit designers, principally on account of the lack of a P-channel device, low device gain and, in general, limitation to depletion mode devices. The most generally adopted active device in GaAs technology is the depletion mode N-channel Metal Semiconductor FET (MESFET) which can be produced with a relatively high degree of uniformity and which has a typical gate length in the range 0.5 to 1 micron. Gate widths vary between a minimum of about 10 microns and several hundred microns.

In view of the cost of GaAs technology and the time taken for processing, it is even more important than for other technologies that computer simulation forms the central component of circuit design. In this work, the circuit simulators used are SPICE 2G6 and HSPICE. In the case of SPICE, the GaAs MESFET is represented by the model for a silicon JFET with appropriately chosen parameters. For HSPICE, on the other hand, three levels of specific MESFET model are available. The parameters for these models are extracted from measurements on actual devices.

Measured characteristic curves for a 100 micron gate width MESFET produced by a typical 1 micron (gate length) GaAs process [2] are shown in Figure 8.1. The parameters given in Table 8.1 for a SPICE JFET model were obtained by optimisation (using TECAP) to give a best fit to the measured curves, as indicated by 'simulated' in Figure 8.1. The ideal JFET

Table 8.1 Key parameters for JFET model of GaAs MESFET

Parameter Name	Value	Units
VTO	-1	V
BETA	0.067E-3	mAV-2
LAMBDA (LF)	0.06	V-1
LAMBDA (HF)	0.3	V-1
RD	2920	Ohms
RS	2920	Ohms
CGS	0.39E-15	F
CGD	0.79	F
PB	0.79	V
IS	0.075E-15	A

Table 8.2 HSPICE MESFET parameters

Parameter	Value	Parameter	Value
Level	2	NI	1.45E10
BETA	0.067E-3	XTI	3
LAMBDA	0.3	AF	1
VTO	-1.0	RD	2920
EG	1.16	RS	2920
GAP1	1108	CGD	0.39E-15
GAP2	7.2E-4	CGS	0.39E-15
IS	0.075E-15	PB	0.79
N	1		

model assumes that saturation of I_d occurs at $V_{ds} = V_{gs} - V_T$, whereas actual devices can exhibit 'early saturation' at a lower voltage than this. It can be seen from Figure 8.1 that, for $V_{gs} = 0$, the saturation region begins when V_{ds} equals about 1 V, which is the device threshold voltage. Thus these devices do not exhibit the 'early saturation effect' of some GaAs processes [3]. Since the curves in Figure 8.1 are obtained by a semiconductor parameter analyser and are therefore low frequency measurements, the gradient in the saturation region does not reflect the high frequency output conductance (g_o) which can be many times higher due to dispersion effects [4], as indicated by the LF and HF values for LAMBDA in Table 8.1. As a result working device gain (transconductance/output conductance) figures as low as 20 are typical. Values of Gate-Source and Gate-Drain capacitances are derived by C-V measurements and by optimisation of the model parameters to fit measured s-parameter data. The

parameters for the more sophisticated level 2 HSPICE model, which will be used in some sections of this Chapter, are given in Table 8.2. This model is based on a cubic expression for the dependence of drain current on gate source voltage, rather than the simple square-law characteristic of the classical SPICE FET model.

The modelling of GaAs MESFET's is at a relatively immature stage compared with other technologies. Moreover, correct modelling is vitally important for successful design of linear, high frequency circuits and systems. Consequently, the development and utilisation of improved models forms an important component of on-going work in this field.

8.3 Current Mirrors

8.3.1 *Classification of Current Mirrors*

There are many different types of current mirror and we begin by considering some definitions and terms commonly used. Current mirrors are firstly categorised as positive or negative. Positive current mirrors have an output in the form of a current sink (quiescent output current positive). Thus they require a power supply which is at a relatively negative potential. Negative current mirrors have a current source output (quiescent output current negative) and require a more positive power supply.

Current mirrors may also be classified according to the orientation of the output signal current. If the output current variation has the same orientation as the input current variation, the mirror is described as non-inverting. If the orientations are opposite, then the mirror is inverting.

Finally, it is possible to combine voltage following and current following (mirroring) in a single component [5]. This component is referred to as a voltage-following current mirror. Such circuits can be regarded as special cases of the 2nd generation current conveyor CCII in which the voltage following input port Y is connected to the current following output port Z - see Chapter 3.

In a technology which provides high quality complementary devices, such as state of the art bipolar (see Chapters 6, 15 and 16) or CMOS (Chapters 5, 6, 7, 11, and 12), positive current mirrors may be realised simply using a pair of N-type (or NPN) devices. Negative current mirrors can be realised using a pair of P-type (or PNP) devices.

In a technology which does not provide complementary devices, the realisation of the negative current mirror has proved difficult. For example, in the past, bipolar technology was unable to provide high quality PNP devices. A circuit realisation which eliminated the need for high quality PNP transistors was proposed by Gilbert [6] but the circuit required identical input and output voltages to operate correctly and so level shifting circuitry was required, leading to increased complexity. An alternative scheme described by Barker and Hart [7] was based on the introduction of a local operational amplifier but this limited high frequency performance.

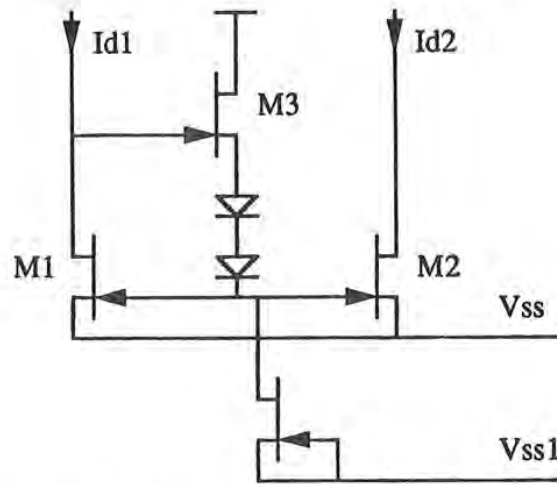


Figure 8.2 Positive GaAs current mirror

For GaAs technology using N-channel MESFET's the negative current mirror is the most useful because there is a requirement for a current mirror to act as a load for N-channel driver devices. The difficulty in realising fast negative current mirrors in NPN bipolar technology may seem discouraging to the development of current mirrors for GaAs technology where devices are limited to N-channel. However, we shall show that in the case of GaAs technology we can in fact utilise the special properties of the depletion mode N-channel MESFET devices to realise high performance negative current mirrors.

8.3.2 Positive Non-inverting Current Mirror

Figure 8.2 shows an existing positive non-inverting current mirror for GaAs technology [8]. Let us approximate GaAs MESFET drain current in the saturation region by a general expression of the form,

$$I_d = W F(V_{gs}) \quad (8.1)$$

where W is gate width, V_{gs} is the gate-source voltage and F is a non-linear function independent of V_{ds} (The effect of V_{ds} variations will be included later in computer simulations). Referring to Figure 8.2, the subsidiary feedback loop making use of the source follower M3 and diode chain maintain the gate of M1 at an appropriate voltage to absorb the incoming current I_{d1} .

Thus, the drain current in M1 is equal to the input current and generates a gate-source voltage V_{gs1} according to Equation 8.1,

$$I_{d1} = W_1 F(V_{gs1}) \quad (8.2)$$

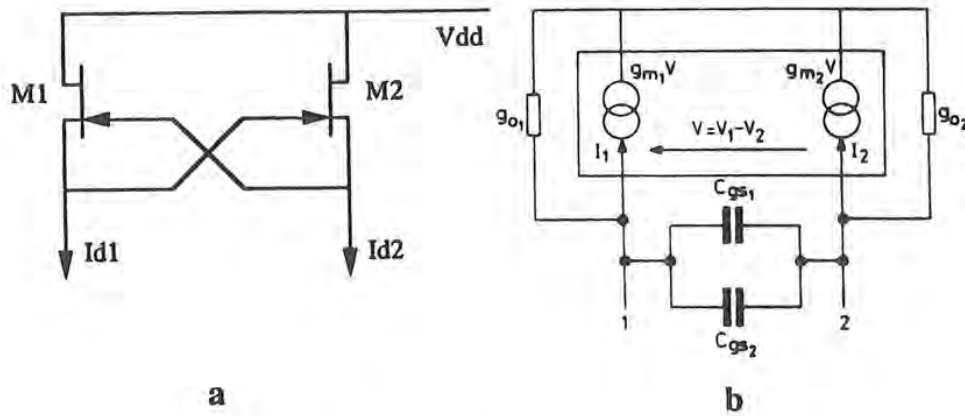


Figure 8.3 Negative GaAs current mirror
a Circuit **b** Model

This gate source voltage is applied directly to the gate-source port of M2, yielding an output current

$$I_{d2} = W_2 F(V_{gs1}) = (W_2/W_1) I_{d1} \quad (8.3)$$

Equation 8.3 shows that this mirror has a linear current transfer characteristic even for large signals. It has been used successfully as part of a sophisticated commercial GaAs operational amplifier circuit having a gain-bandwidth product of 500 MHz [8]. However, we shall show later that by avoiding the subsidiary feedback loop, even better high frequency performance is possible.

8.3.3 Negative Inverting Voltage-following Current Mirror

8.3.3.1 Basic Analysis

Figure 8.3a shows a pair of N channel GaAs MESFET's with gates and sources cross-coupled [2,9]. The operation of the circuit may be explained using the small-signal equivalent circuit in Figure 8.3b. Here, the controlled sources of the small-signal models for the two MESFET's are shown in a central block with the (parasitic) passive components outside. Analysis of the central block leads to the transmission matrix description

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & -1/gm_2 \\ 0 & gm_1/gm_2 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \quad (8.4)$$

The term gm_1/gm_2 in the transmission matrix is the current gain of the mirror, showing it has an inverting property when we take into account the transmission matrix sign convention. The unity term in the matrix embodies

the voltage following property. The term $-1/gm_2$ is an undesired term and its effect can be evaluated by considering the input impedance of the mirror.

If port 2 is terminated in a load impedance ZL_2 , the input impedance at port 1 is given by

$$Z_{i1} = (gm_2/gm_1)ZL_2 - 1/gm_1 \quad (8.5)$$

Similarly, for a load impedance ZL_1 at port 1, the input impedance at port 2 is given by

$$Z_{i2} = (gm_1/gm_2)ZL_1 + 1/gm_2 \quad (8.6)$$

Provided the load impedances ZL_1 and ZL_2 are much greater than $1/gm_1$ and $1/gm_2$, the input impedance at each port is proportional to the load impedance at the other port. These conditions for the proportional impedance property, or impedance transforming property, are generally satisfied in the circumstances where it is wished to utilise the current mirror, as we shall show in the applications of the current mirror to be presented later.

The impedance transforming property of the current mirror is of crucial significance for the design of high speed circuits. Although the input and output nodes of the current mirror are physically separate, the fact that parasitic capacitance at one node may be equivalently transferred to the other node means that they can be regarded in some respects as a single node. When the current mirror is used in a feedback loop, as is frequently required, this single-node feature minimises the number of poles introduced leading to increased stability margins and optimum dynamic response.

Turning to the large signal behaviour of the current mirror, we now assume a simple non-linear expression for MESFET drain current, in the saturation region, of the form

$$I_d = (KW/2) [V_{gs} - V_t]^2 \quad (8.7)$$

where K is a transconductance factor and V_t is the threshold voltage. The parameters K , V_t and gate length are assumed to be the same for all MESFET's in a circuit and channel length modulation is omitted at this stage. Assuming that both MESFET's in Figure 8.3a are biased in the saturation region, the drain currents can be described by

$$I_{d1} = I_{dss1} (V_{gs1}/V_t - 1)^2 \quad (8.8)$$

and

$$I_{d2} = I_{dss2} (V_{gs2}/V_t - 1)^2 \quad (8.9)$$

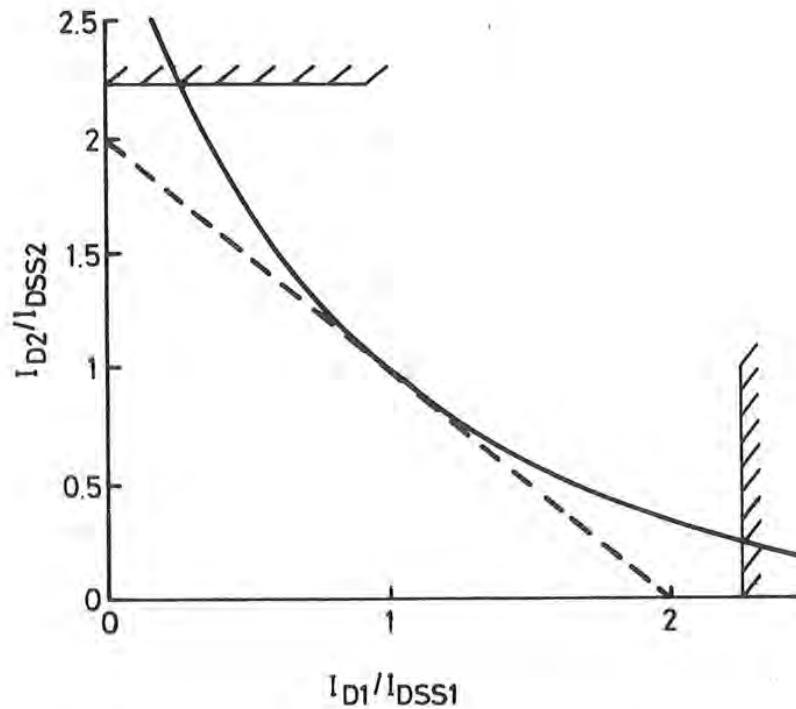


Figure 8.4 Large-signal current transfer characteristic

where $I_{dss} = (KW/2)V_t^2$ is the drain current for zero gate source voltage. The cross-coupled connection imposes the constraint $V_{gs1} = -V_{gs2}$ and therefore we obtain

$$\frac{I_{d2}}{I_{dss2}} = \frac{I_{d1}}{I_{dss1}} + 4 \left[1 - \sqrt{\frac{I_{d1}}{I_{dss1}}} \right] \quad (8.10)$$

Figure 8.4 shows I_{d2}/I_{dss2} plotted against I_{d1}/I_{dss1} . The currents for which the device Schottky diodes become forward biased ($V_{gs} = 0.5$ V) are $2.25 I_{dss}$ for a typical V_t of -1 V, and these limits are shown in Figure 8.4. Although the current transfer characteristic in Figure 8.4 is not linear, it is sufficiently close to the linear curve (shown dashed) for many applications, as we shall show in Section 8.7.

The above analysis of the basic current mirror in Figure 8.3a has ignored the MESFET output conductances g_o which are very significant for GaAs technology (typical $g_o = gm/20$). This parameter will seriously affect the current transfer accuracy and the port impedances of the current mirror. In order to obtain acceptable performance, we introduce cascoding techniques which will now be described.

8.3.3.2 Cascode Current Mirror Using a Seperate Bias Chain

Cascode circuit techniques have an overriding effect on the voltage gains of operational amplifiers using GaAs MESFET's. Without cascoding, the low device gain for GaAs MESFET's (gm/g_o) of typically 20 leads to amplifier gains of about 10. The introduction of single cascode techniques will lead to gains of the order of 100. Double cascode techniques will provide gains of the order of 1000. For applications in analogue signal processing systems, such as switched capacitor filters [10,11], gains of 1000 are generally required necessitating double cascode techniques. Special circuits which have the property of finite gain insensitivity [12], can tolerate amplifier gains of 40 dB produced by single cascode techniques. Since the current mirror is an important building block for the design of operational amplifiers, as well as other analogue components, we need to be able to realise both single cascode and double cascode current mirrors. Looked at it from an impedance point of view, the small-signal output (drain) conductance of a single MESFET, or basic current mirror as in Figures 8.2 or 8.3a, is of the order of g_o . For a single cascode MESFET or current mirror, this conductance is reduced to a figure of the order of g_o^2/g_m , and for a double cascode MESFET or current mirror, we obtain the much lower figure of g_o^3/g_m^2 .

The voltages on the gates of cascode transistors must be defined in such a way that the current mirror devices are maintained in the saturation region as far as possible. In general, the gate voltage bias can be provided in two ways, namely by using level shifting diodes or by using a 'double level shifting' technique which relies upon the ratioing of device gate widths [2]. The double level shifting approach has the advantage that both the voltage level shift introduced and the voltages required to keep the devices in saturation scale proportionally to the device threshold voltage V_t making circuit performance less sensitive to process variations. In this paper, we shall adopt the double level shifting technique.

In order to understand the double level shifting biasing technique, we begin by considering the following simple arrangement. A GaAs MESFET MA has its gate connected to its source so that its current is equal to its I_{DSS} . Its drain is connected to the source of a second MESFET MB such that both devices have the same drain current. Using the expression in Equation 8.7, it may be shown that the V_{gs} of MESFET B is given by

$$V_{gsB} = V_t [1 - \sqrt{(W_A/W_B)}] \quad (8.11)$$

By making the width of MESFET MB greater than that of MA, we obtain a negative V_{gs} for MB which amounts to a positive level shift between gate and source.

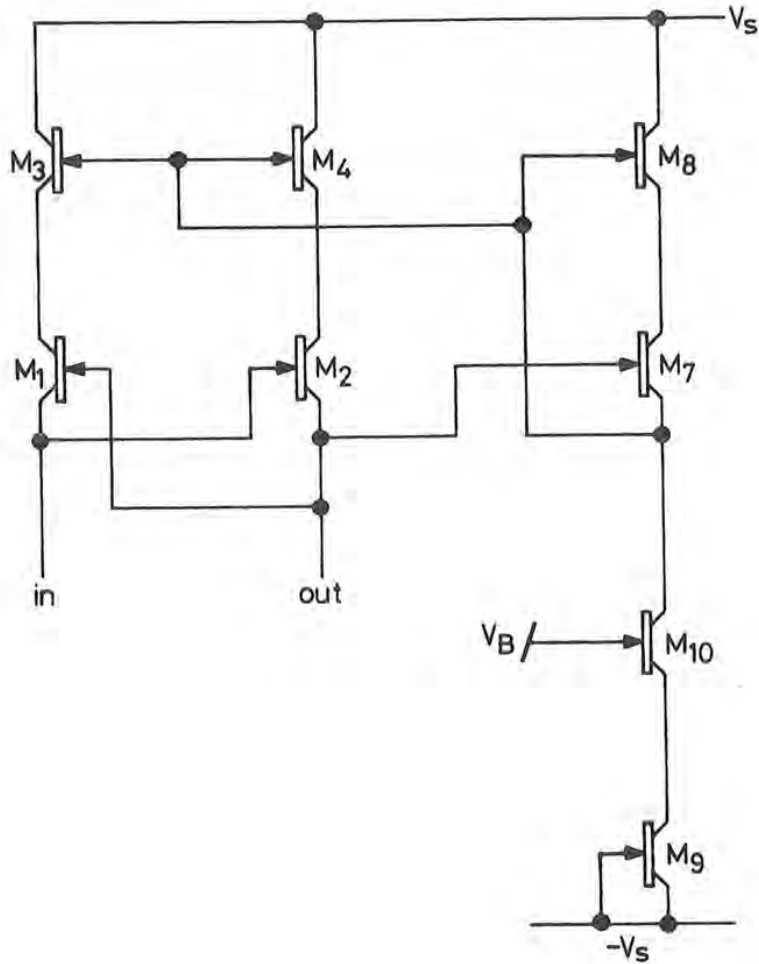


Figure 8.5 Single cascode current mirror using separate bias chain

In double level shifting, we effectively use a cascade of two such level shifts in order to maintain a MESFET current source in the saturation region. In the absence of 'early saturation', this requires a minimum V_{ds} , and hence a minimum level shift, equal to V_t . Thus each level shift stage requires a V_{gs} equal to $V_t/2$, which can be met, from Equation 8.11, by using a minimum device width ratio W_B/W_A of 4.

A single cascode current mirror using the double level shifting biasing technique is shown in Figure 8.5. M_1 and M_2 comprise the basic current mirror and M_3 and M_4 are the cascode transistors. A separate bias chain principally comprises source follower M_7 fed by a single cascode current source M_9 with cascoding MESFET M_{10} . The gate width of M_7 is made greater than that of M_9 , and M_3 and M_4 have gate widths larger than M_1 and M_2 , using practical gate width ratios of about 5. The combined level shifts produced by M_7 and M_3/M_4 are sufficient to maintain M_1 and M_2 in the

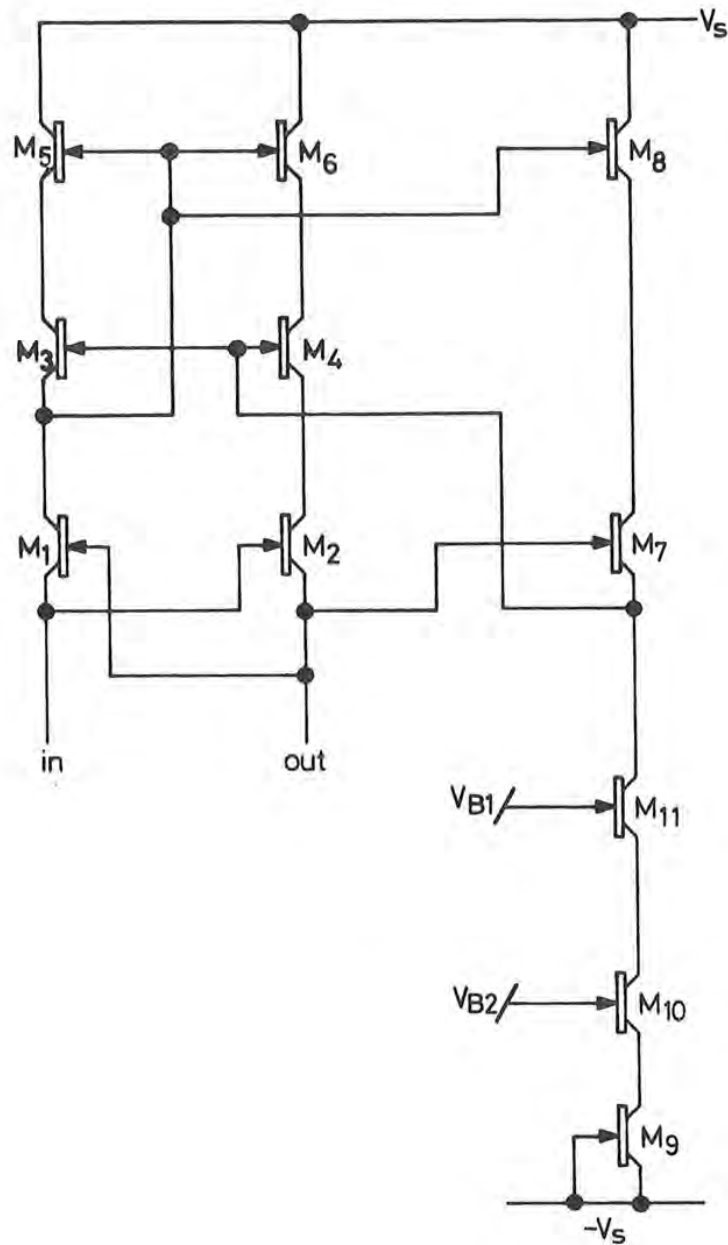


Figure 8.6 Double cascode current mirror using separate bias chain

saturation region, as required. MESFET M8 bootstraps the drain of M7, improving the source follower performance. Although this double level shifting circuit technique is intended to tolerate devices which do not exhibit early saturation [2], it is still advantageous for devices with early saturation, since it allows device width ratios to be reduced below the above figures.

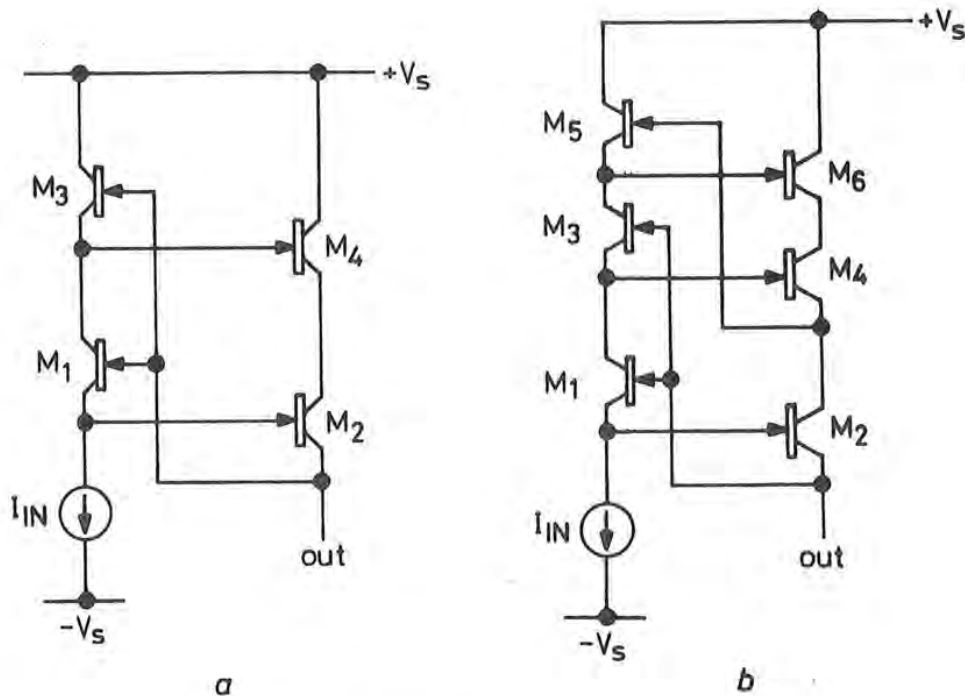


Figure 8.7 Cascode current mirrors
a Single cascode **b** Double cascode

For the realisation of a double cascode current mirror, another pair of cascode MESFET's must be introduced above M3 and M4 in Figure 8.5. In principle, the gates of these MESFET's could be biased via a second separate bias chain fed from the source of M7. However, such a current mirror has an excessive phase shift which leads to relatively large settling times when used to realise amplifiers. This might be attributable to the presence in the circuit of large loops encompassing relatively large numbers of devices. For the double cascode current mirror, therefore, the upper pair of cascode MESFET's are biased in an alternative way as indicated in Figure 8.6. This more direct method of biasing MESFET's M5 and M6 from the source of M3, which also provides bias for the gate of M8, allows the design of high gain operational amplifiers with very fast settling times, as we shall show in Section 8.7.

8.3.3.3 Economical Cascode Current Mirrors

We have shown that cascode current mirrors can be developed using a separate bias chain to bias the gates of the cascode MESFET's. The presence of the additional bias chain increases the power consumption of the current mirror and also increases the chip area requirement. In fact, it is possible to

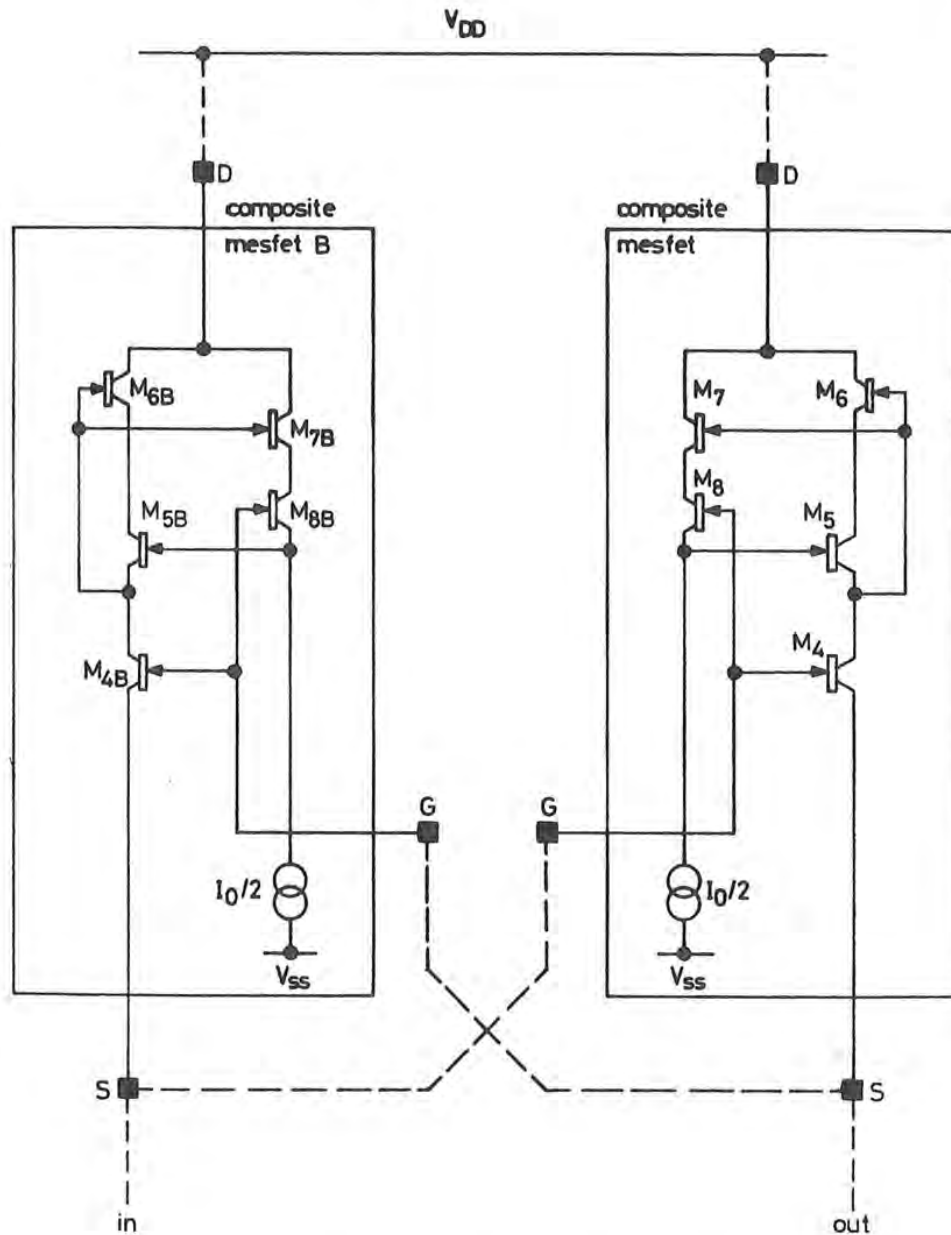


Figure 8.8 Current mirror using composite MESFET's

develop cascode current mirrors without additional bias chains in which the cascode MESFET's themselves provide the required voltages for their gates.

A single cascode current mirror based on this idea is shown in Figure 8.7a [13,14]. MESFET M_3 is biased from M_1 using self-bootstrapping [3]. Since the drain-gate voltage of M_1 is equal to the negative V_{gs} for a single

MESFET (M3), it follows from Equation 8.11 that in order to achieve a V_{gs} equal to V_t , an infinite device width ratio is needed. In practice, we achieve an acceptable approximation to full saturation of M1 by making the gate width of M3 about 10 times that of M1 (assuming no early saturation). The width of M4 is made much greater than that of M2 so that its negative V_{gs} assists the negative V_{gs} of M3 in keeping the more critical output MESFET M2 fully saturated. The realisation of a double cascode current mirror using this idea is shown in Figure 8.7b [2,9,13]. Additional cascode MESFET's M5 and M6 are biased in a similar way as are M3 and M4.

The current mirrors of Figure 8.7 are highly economical in the sense that the cascode MESFET's are performing two functions simultaneously, namely a double level shifting function and a cascoding function. The disadvantage that device M1 is not quite fully saturated in the absence of early saturation leads to increased drain-gate capacitance and hence increase in the settling time of amplifiers realised, as we shall show in Section 8.7.

8.3.3.4 *Current Mirror Using Composite MESFET's*

The current mirrors described in Section 8.3.3.2 used a separate bias chain in order to allow every MESFET to be properly maintained in saturation, which leads to optimum performance. In this Section, we present an alternative method of achieving the same aim, using the concept of a composite MESFET [15]. We illustrate the development of a current mirror using composite MESFET's for the double cascode case. Consider MESFET M4 in Figure 8.8. Its gate and source are treated as being the gate (G) and source (S) of a composite MESFET. The drain (D) of the composite MESFET is connected to the drain of M4 via cascode MESFET's M5 and M6, which are biased using the double level shift technique used to bias the current mirror in Figure 8.6. The gate of M5 in Figure 8.8 is biased from a separate bias chain as was M4 in Figure 8.6. M6 is biased from the source of M5 as in Figure 8.6, and M7 has the same function as M8 in Figure 8.6.

Having developed a double cascode composite MESFET with very low output conductance, the next stage is to combine two such composite devices according to the basic cross-coupled current mirror architecture of Figure 8.3a to form a fast high impedance current mirror, as shown in Figure 8.8. In this current mirror, all devices are properly saturated, facilitating the design of high performance pushpull operational amplifiers, as we shall see in Section 8.7.

8.3.4 *Linear negative current mirror*

In this Section, we combine two of the negative current mirrors of Figure 8.3a, to form the new current mirror in Figure 8.9. We now assume the general MESFET drain current expression given by Equation 8.1.

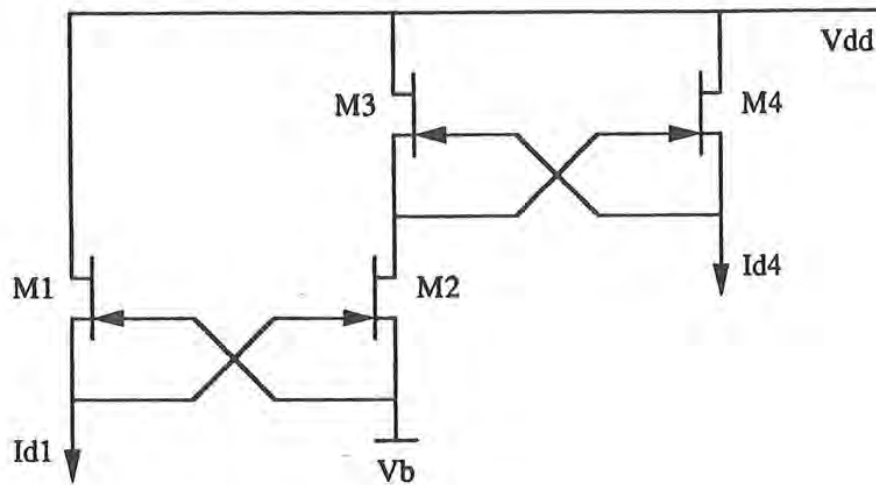


Figure 8.9 Linear negative GaAs current mirror

Referring to Figure 8.9, the drain current in M1 is equal to the input current and generates a gate-source voltage V_{gs1} according to Equation 8.1 of

$$I_{d1} = W_1 F(V_{gs1}) \quad (8.12)$$

This gate source voltage is inverted by the first current mirror and applied to M2. Since the drain current in M3 is equal to that in M2, its gate-source voltage is the same. Finally the gate-source voltage of M3 is inverted and applied to M4. Hence, the output current of the circuit is given by

$$I_{d4} = W_4 F(V_{gs1}) = (W_4/W_1) I_{d1} \quad (8.13)$$

Thus, we see that, although this current mirror is formed from two non-linear current mirrors, it has a linear transfer characteristic, even for large signals. Furthermore, the new mirror does not have the voltage following property of the mirror in Figure 8.3a and it is non-inverting.

8.3.5 Current mirror performance evaluation

We now compare the performances of the three basic, or non-cascoded, current mirrors in Figures 8.2, 8.3a and 8.9 by computer simulation using HSPICE with the level 2 MESFET parameters of Table 8.2. All devices had gate widths of 16 microns, which is a typical minimum gate width, and bias voltages were chosen to maintain MESFET drain-source voltages at around 3 V.

The DC transfer characteristics are shown in Figure 8.10. Curve 1 illustrates the predicted linearity of the current mirror of Figure 8.2 and curve 2 the non-linearity of the inverting current mirror of Figure 8.3a,

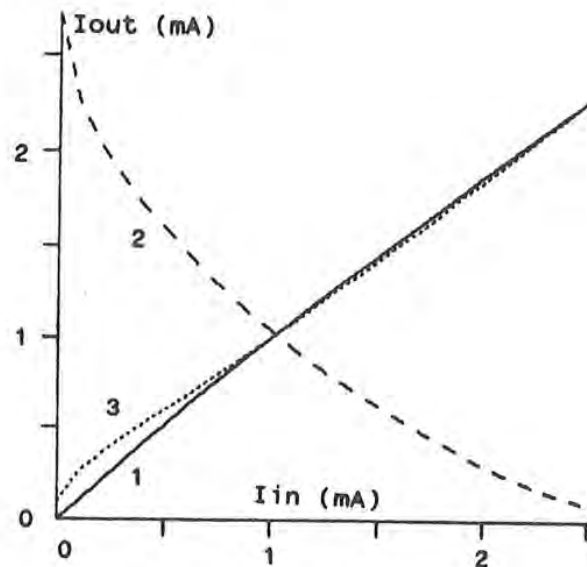


Figure 8.10 Current mirror DC current transfer curves
Curve 1 - Figure 8.2; Curve 2 - Figure 8.3a; Curve 3 - Figure 8.9

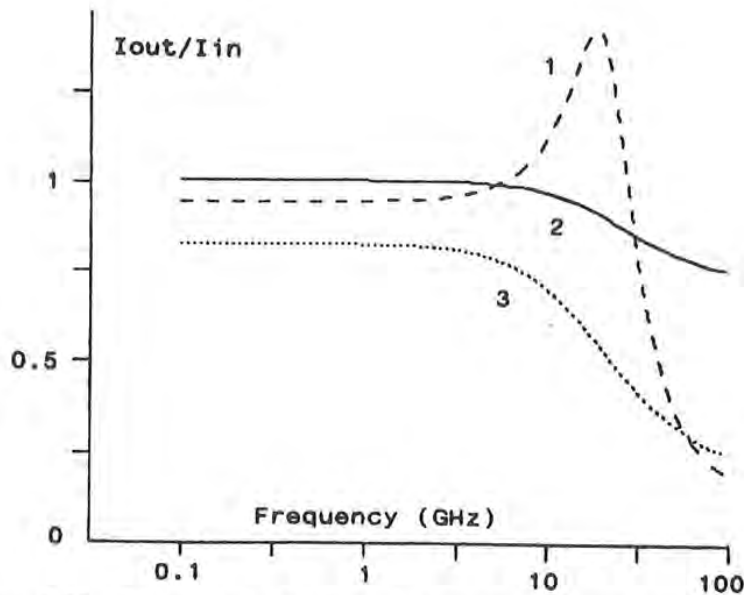


Figure 8.11 Current mirror output current/frequency responses
Curve 1 - Figure 8.2; Curve 2 - Figure 8.3a; Curve 3 - Figure 8.9

which was expected from the theoretical plot of Figure 8.4. Curve 3, for the new current mirror of Figure 8.9, confirms its linear operation.

The simulated frequency responses of the three current mirrors are compared in Figure 8.11, for short circuit conditions. These results

illustrate the expected tendency towards instability of the mirror in Figure 8.2, which was expected on account of the presence of an internal feedback loop. The new mirror of Figure 8.9 has the excellent stability and bandwidth of the mirror in Figure 8.3a but with slightly lower current gain due to the additional stage. The current mirrors will be used later as versatile, high performance, building blocks.

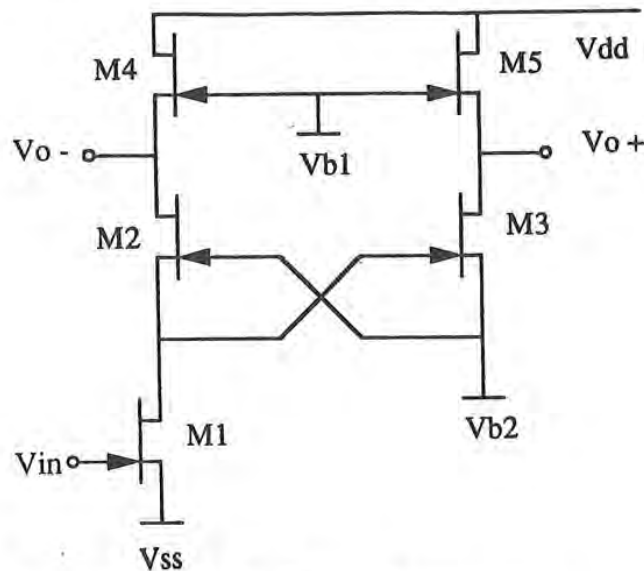


Figure 8.12 Single-ended to differential converter

8.4 Single-ended to Differential Converter

Differential mode circuits have the desirable features of reduced DC offset voltages and improved power supply rejection ratio compared with single-ended circuits. Thus there is a requirement to be able to convert a signal from single-ended mode to differential mode and vice versa.

A circuit which can be used to generate complementary signals from a single unbalanced signal is shown in Figure 8.12. The circuit, in which all devices have the same gate width, makes use of the non-linear inverting negative current mirror of Figure 8.3a. Its operation can conveniently be explained using the MESFET drain current expression of Equation 8.1. The input voltage in Figure 8.12 defines the V_{gs} of M1. Since M2 and M4 have the same drain current as M1, it follows that V_{o-} is equal to $-V_{in}$ and that the V_{gs} of M2 is equal to V_{in} . The V_{gs} of M2 is inverted by the current mirror when applied to M3 and since M5 shares the same drain current as M3, it follows that V_{o+} is equal to V_{in} . This circuit achieves a linear voltage-to-voltage transfer characteristic, inspite of the non-linear voltage-to-current transfer characteristic of the MESFET and the non-linear current-to-current transfer characteristic of the current mirror used.

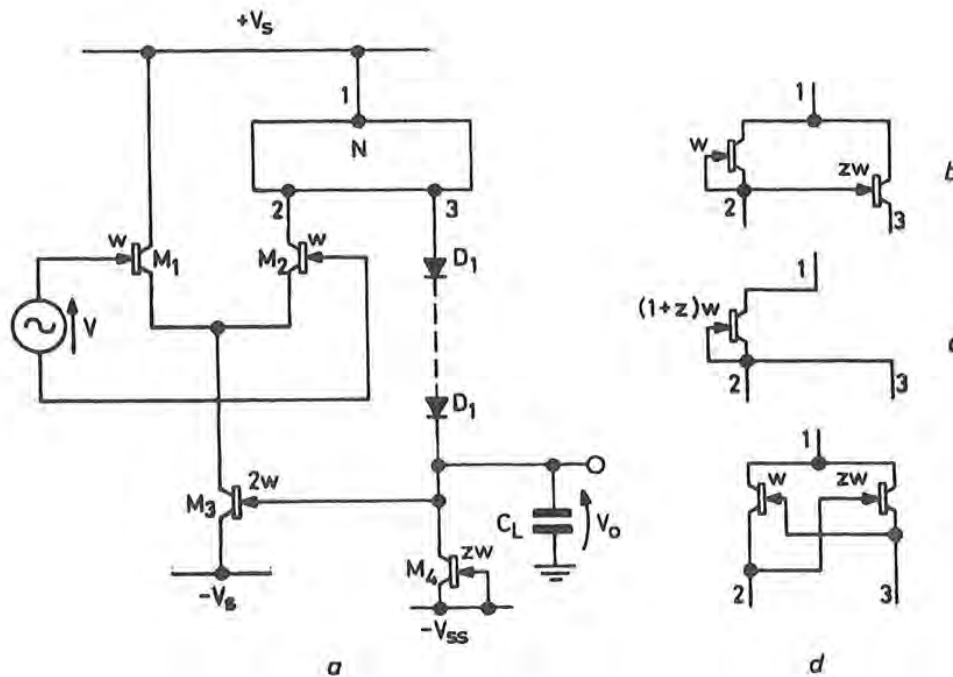


Figure 8.13 Differential to single-ended converter
 a Basic architecture b Subcircuit using source follower
 c Subcircuit using current source d Subcircuit using current mirror

8.5 Differential to Single-ended Converter

A general architecture for a differential to single-ended converter circuit is shown in Figure 8.13a [16,17]. The network 'N' is designed to ensure that the drain current of MESFET M2 is constant. Thus the small-signal currents in M1 and M3 are the same, leading to an overall voltage gain for the converter of the order of 0.5. This gain is acceptable for many applications, but a modification to allow higher gains has been presented [17]. For the network 'N' in Figure 8.13a, three configurations have been investigated and these are shown in Figures 8.13b, c and d. Figure 8.13b, used in converter configuration 1, is basically a current source connected MESFET and a source follower. Figure 8.13c, used in configuration 2, is simply a larger current source. Configuration 3 makes use of the basic voltage following current mirror of Figure 8.3a.

The simulated gain responses of the three configurations are shown in Figure 8.14 together with MESFET sizing and circuit conditions. It can be seen that configuration 3, using the voltage following current mirror, avoids the undesirable tendency towards instability and peaking of configuration 1, while providing a higher gain than configuration 2. The greater stability factor is attributed to the 'single node', or impedance transforming,

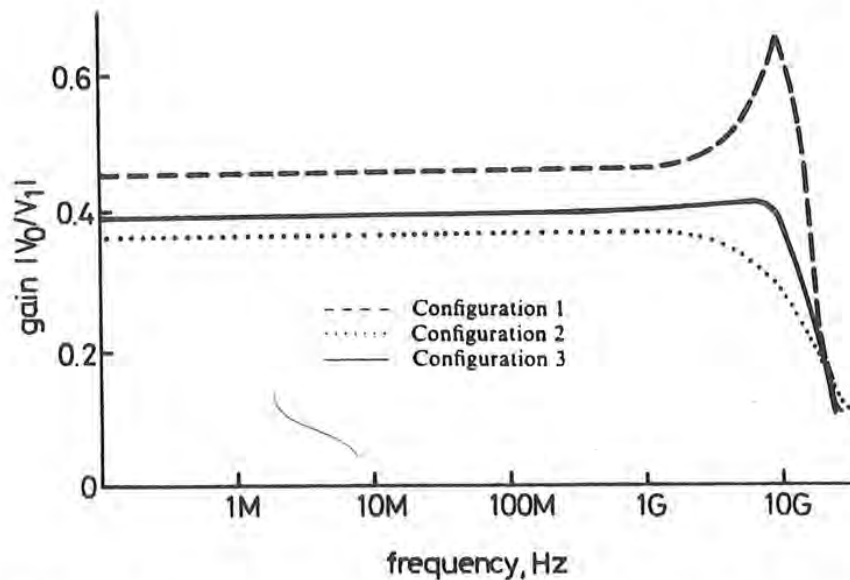


Figure 8.14 Differential-to-single ended converter amplitude responses
Gate width $W=50\ \mu\text{m}$; $Z=2$; $CL=39\ \text{fF}$ (=typical C_{gs}); $V_s=5\text{V}$, $V_{ss}=7.5\text{V}$

property of the current mirror. This property gives the added benefit that the gain is less dependent on the geometries of the devices, giving considerably greater freedom of design. Although the current mirror used has a non-linear current transfer characteristic, its non-linearity does not significantly affect the converter linearity because the mirror is within an internal feedback loop.

The differential to single ended converter using the current mirror can be used in conjunction with single ended input amplifiers, of the type to be described, for the realisation of high performance composite amplifiers with differential input capability [13,17].

8.6 Linear Transconductors

8.6.1 Linearisation Principles

We see in Chapters 4, 9, 10 and 17 that the linear transconductor, or voltage controlled current source, is a very powerful circuit building block for high frequency applications, including filters, amplifiers and components for optical communication systems. We now present a general approach for the design of linear transconductors using GaAs MESFET's, which is a generalisation of the approach in [18] developed for MOS technology.

We begin by assuming that the GaAs MESFET drain current in the saturation region can be described by a general expression of the form of Equation 8.1. Consider now the current function denoted I_o which is defined as

$$I_o = W F(V_{gs}) - W F(-V_{gs}) \quad (8.14)$$

We now express F as the sum of components which are even and odd in V_{gs} , which we denote as F_e and F_o . We thus obtain

$$I_o = 2 W F_o(V_{gs}) \quad (8.15)$$

For the system to be linear, I_o should be proportional to V_{gs} . Denoting the constant of proportionality G_m , this requires that

$$F_o(V_{gs}) = (G_m/2W) V_{gs} \quad (8.16)$$

The simplest model for the drain current of a GaAs MESFET in the saturation region ignoring channel length modulation is given by Equation 8.7, which may be written in even and odd parts as

$$I_d = (KW/2) [V_{gs}^2 + V_t^2] - K W V_t V_{gs} \quad (8.17)$$

The odd part of this expression satisfies the requirement of Equation 8.16 and gives a transconductance of

$$G_m = 2 K W (-V_t) \quad (8.18)$$

where $-V_t$ is positive for depletion mode devices. We now consider implementation of GaAs transconductors based on this linearisation principle.

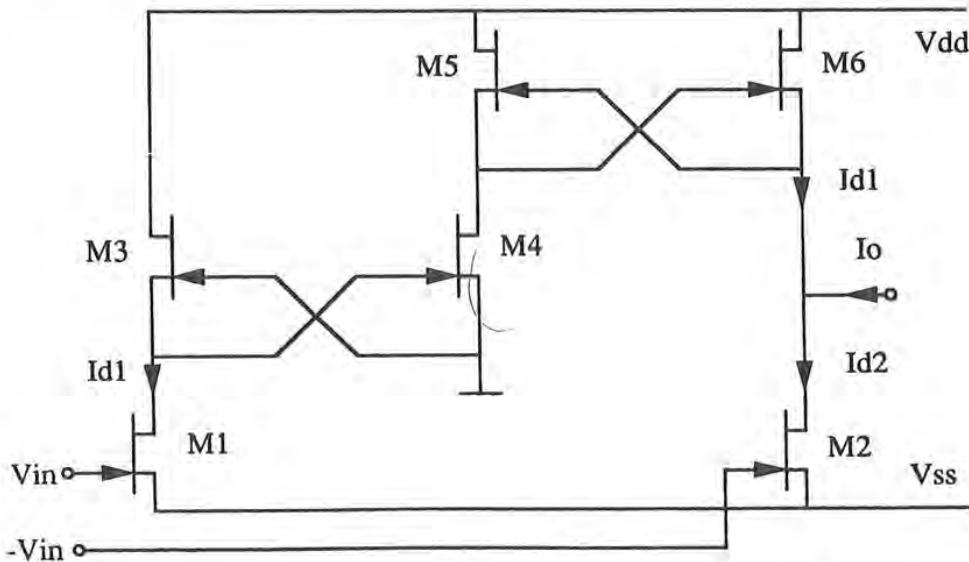


Figure 8.15 GaAs transconductors using non-inverting current mirror

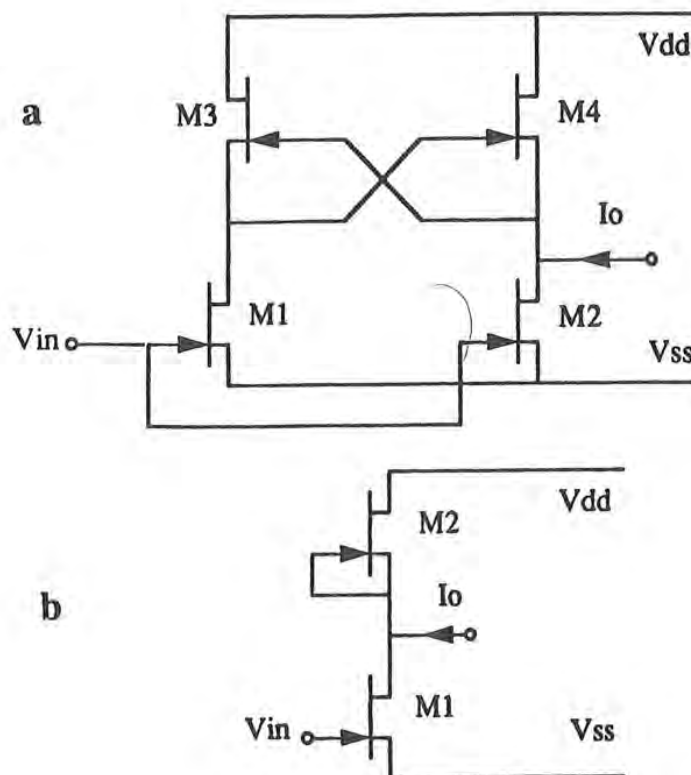


Figure 8.16 Alternative GaAs transconductors
a Using inverting current mirror **b** Classical inverter-type circuit

8.6.2 Linear Transconductor Implementation

8.6.2.1 Circuit Using Non-inverting Current Mirror

Consider the circuit in Figure 8.15. M1 and M2 are driver MESFET's and M3 to M6 comprise the linear non-inverting current mirror of Figure 8.9. This arrangement implements the required relationship in Equation 8.14 because the output current is the difference $I_{d1} - I_{d2}$ and M1 and M2 are driven by complementary V_{gs} inputs. This arrangement has the disadvantage that linearity depends on the input signals being truly complementary, which may be difficult to achieve in practice. The circuit in Figure 8.12 could in principle be used to generate these signals but, in fact, a much more attractive transconductor circuit is possible.

8.6.2.2 Transconductor Using Inverting Current Mirror

We now consider the transconductor architecture in Figure 8.16a. The input voltage is applied directly to MESFET's M1 and M2. MESFET M3 shares the same drain current as M1 and, provided its gate width equals that of M1

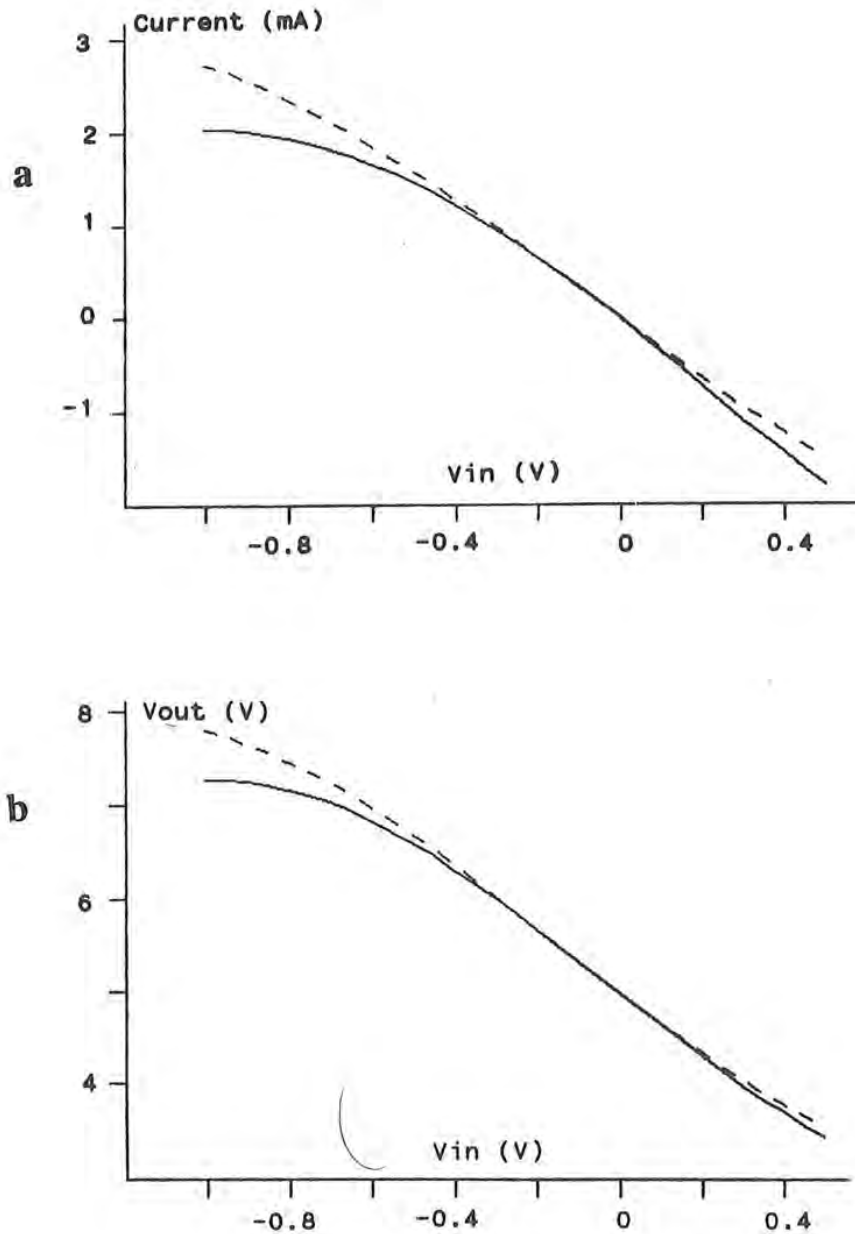


Figure 8.17 Simulated transconductor DC transfer characteristics
a Short-circuit load **b** $R_L = 1144 \text{ Ohm}$

($W_3 = W_1$), its V_{gs} equals V_{in} . MESFET M4 is cross-coupled to M3, and so the V_{gs} of M4 is equal to $-V_{in}$. Assuming that the gate widths for M2 and M4 are equal ($W_4 = W_2$), the output current I_o is the difference $I_{d2} - I_{d4}$, which satisfies Equation 8.14, the fundamental requirement for linearity, with W equal to W_2 .

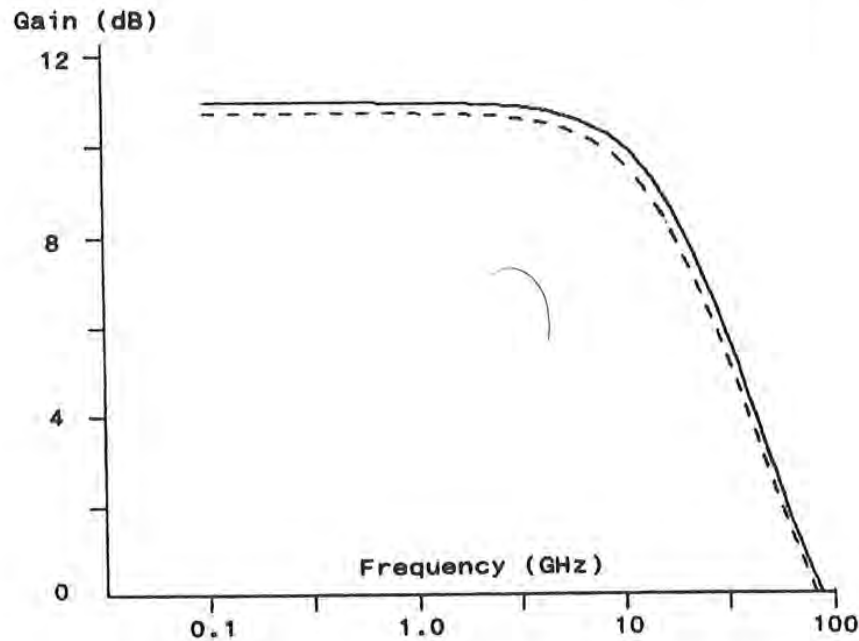


Figure 8.18 Transconductor frequency responses
 ——— Figure 8.16a - - - - Figure 8.16b

An alternative, but less elegant way of viewing this circuit, is that it permits the non-linear current transfer characteristic of the current mirror (Equation 8.10) to compensate for the non-linearity of the MESFET voltage-to-current transfer characteristic (Equation 8.7).

Figure 8.16b shows a conventional inverter circuit comprising a MESFET M1 fed from a current source connected MESFET M2. This circuit will be used as a benchmark for evaluation of the transconductor in Figure 8.16a. For comparison, the gate widths are the minimum 16 microns for the circuit in Figure 8.16a and 32 microns for the inverter in Figure 8.16b, required in order to achieve the same transconductance because the inverter does not realise a push-pull output.

Figure 8.17a shows the simulated DC current transfer characteristics of the transconductors in Figure 8.16. HSPICE was used with the level 2 MESFET parameters of Table 8.2. The outputs are short circuit and the input voltage ranges from cut-off ($V_{gs} = V_t = -1V$) to Schottky breakdown point ($V_{gs} = 0.5V$).

Figure 8.17b shows a comparison of the simulated voltage-to-voltage transfer characteristics of the same two transconductors for a load resistance of 1144 Ohm, giving a gain of approximately 11 dB. The results in Figure 8.17 show that even for a fairly sophisticated MESFET model, the new transconductor achieves greater linearity. The small signal frequency responses of the two transconductors in 11 dB gain configuration are shown

Table 8.3 Transconductor distortion figures ($V_{in} = 0.1 V_{peak}$)

Harmonic	Fo = 100MHz		Fo = 1 GHz	
	Fig. 8.16b	Fig. 8.16a	Fig. 8.16b	Fig. 8.16a
Fo (Vpeak)	0.3294	0.3511	0.3290	0.3503
2Fo (dB)	-37	-53	-37	-47
3Fo (dB)	-60	-62	-60	-61
4Fo (dB)	-99	-93	-98	-90
THD (%)	1.3	0.2	1.3	0.4

in Figure 8.18, confirming that both transconductors have a similar small signal bandwidth for a load resistance of 1144 Ohm.

A comparison of simulated distortion results for the transconductors in 11 dB gain configuration is shown in Table 8.3. The new transconductor achieves a significant improvement in total harmonic distortion (THD) at 100 MHz by a factor of about 6. This is reduced somewhat at 1 GHz. The reason for the greater variation of distortion with frequency for the new circuit is being investigated with improved modelling techniques.

The results in Figures 8.17 and 8.18 indicate that the transconductor in Figure 8.16a achieves improved linearity and lower distortion compared with existing circuits without any discernable penalty in terms of high frequency performance.

8.7 High Gain Operational Transconductance Amplifiers

8.7.1 General

The operational amplifier is a centrally key component for the realisation of many analogue circuits. For high frequency sampled data applications,

including GaAs switched capacitor filters and analogue-to-digital and digital-to-analogue converters [14], the requirements differ in key aspects from those for general purpose amplifiers [8,19-21]. For example, a high output impedance is preferred (current output instead of voltage output) in view of the capacitive loads. Settling time is a very important parameter since it

determines the maximum speed of circuit operation. DC gain must be above specified limits which are typically 60 dB, or 40 dB is permissible if finite gain insensitive switched capacitor circuits are adopted [12].

8.7.2 Circuits Using Diode Level-shifting

A basic structure for a moderate gain inverting amplifier is shown in Figure 8.19a; M1 is the driver transistor and M2 the cascode transistor. Assuming

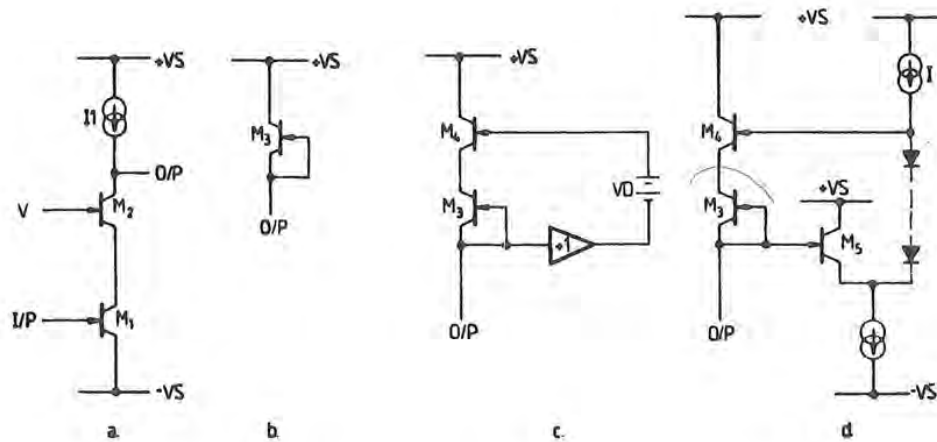


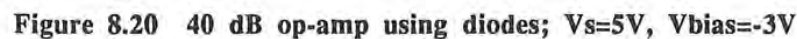
Figure 8.19 Basic amplifier techniques

a Basic inverter architecture b Single MESFET current source
c Cascode current source architecture d Cascode current source

an ideal current source, the voltage gain is $gm_1gm_2/(go_1go_2)$ which would have a typical value of 400. For the realisation of the current source, a single MESFET connected as in Figure 8.19b may in principle be used. However, this would reduce amplifier voltage gain to a low value of approximately gm_1/go_3 ; the typical low value of gm/go of about 20 makes it necessary to develop a high impedance current source using cascode techniques. This is shown in Figures 8.19c and d. In Figure 8.19c, the drain-source voltage of M3 is kept relatively constant (independent of V_O) by means of the buffer amplifier, DC voltage source (V_D) and source follower M4. A realisation of the buffer and DC source is as in Figure 8.19d, using the source follower M5, diode chain and associated current sources.

The realisation of a complete amplifier is shown in Figure 8.20. The devices M1 to M5 are as identified in Figure 8.19d; M6 realises the upper current source in Figure 8.19d; the lower current source in Figure 8.19d is realised in two parts, namely M7 and M8; finally, M9, M10 and M11 are cascode transistors which improve source follower performance. DC gain for this amplifier is typically $(gm/go)^2/4$ (about 40dB). For the bias MESFET's M5 - M11 in Figure 8.20, the gate widths (indicated as factors multiplying the minimum gate width) may be equal to the minimum, ie unity. The gate width in the input/output chain comprising M1 - M4 determines the amplifier transconductance and slew rate and the gate widths of these devices are defined as an amplifier scaling factor k multiplied by the minimum gate width.

SPICE simulation of a unit scaled amplifier using the typical MESFET model parameters of Table 8.1, indicates a DC gain of 41 dB, a gain-bandwidth product of 3.6 GHz and a phase margin of 70 degrees, when used



8.7.3 Circuits Using Device Width Ratioing

We illustrate biasing techniques based on device width ratioing by the design of a pushpull amplifier. A basic architecture for a pushpull amplifier is in fact realised by the transconductor architecture already shown in Figure 8.16a. The advantage of this push-pull arrangement is that it is possible to reduce the widths of M1 and M3 below those of M2 and M4 without affecting gain or transconductance, yielding a given transconductance and maximum output current for about half the effective area and power consumption compared with a simple (non push-pull) inverter (Figure 8.16b). However, the gain of the amplifier in Figure 8.16a is only of the order of $g_m/(2g_o)$, which is the same as for the inverter of Figure 8.16b, and it is thus necessary

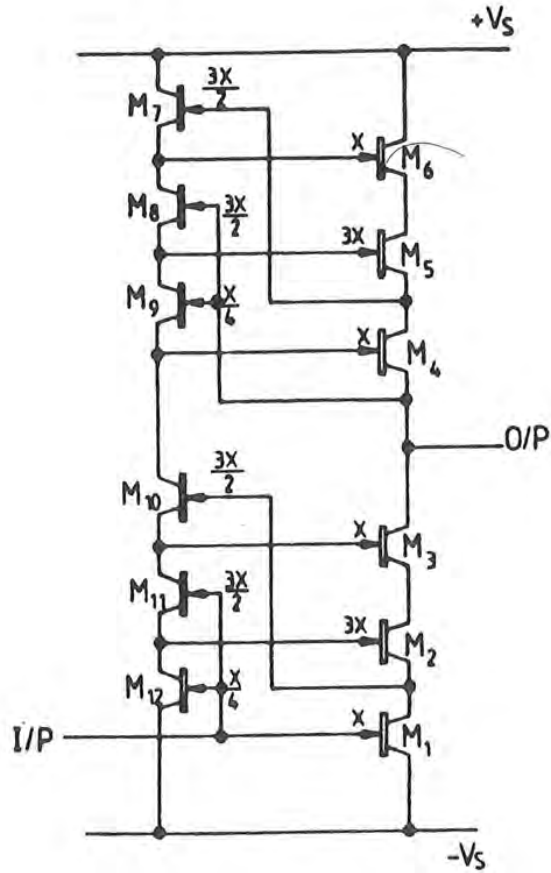
Figure 8.21 High gain double cascode amplifier; $V_s=5V$

Table 8.4 Operational amplifier performance parameters

Amplifier circuit	Minimum settling time (ps)	Load capacitance (pF)	DC gain (dB)	GB product (GHz)	Phase margin (deg)
Fig. 8.20	200	0.08	41	3.6	70
Fig. 8.21	457	0.8	63	3.1	64
Fig. 8.22	230	0.8	61	3.2	71
Fig. 8.24	215	0.8	65	3.1	70

to introduce double cascode techniques for each MESFET. The circuit in Figure 8.16a is now considered to consist of two parts; a current mirror consisting of M3 and M4, and a dual driver circuit consisting of M1 and M2. A double cascode version of the current mirror has already been shown in Figure 8.7b. This circuit is also used with modified connections to the gates and sources of M1 and M2 to form the double cascode dual driver required, and the final amplifier is shown in Figure 8.21 [2,13].

The simulated performance of the amplifier in Figure 8.21, with a 0.8 pF load capacitance, using the device parameters as in Table 8.1, gives the key performance parameters tabulated in Table 8.4. It can be seen that the low frequency voltage gain is 63 dB and that a minimum settling time of 457 ps is achieved.

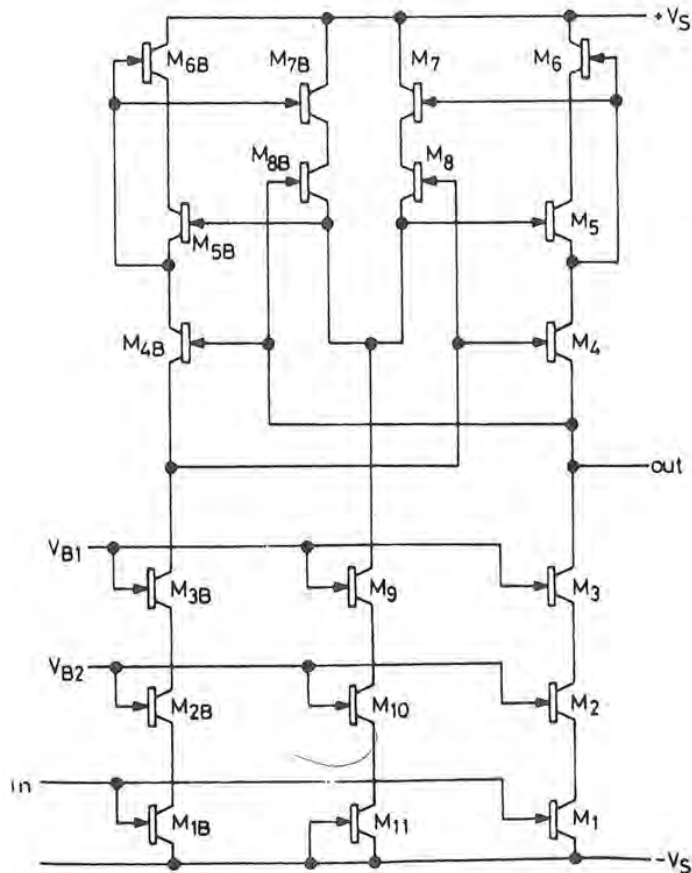


Figure 8.22 Amplifier using current mirror with composite MESFET's ($V_S=5V$; $V_{B1}=-2.2V$; $V_{B2}=-3.6V$; all devices $100\ \mu m$ except M7, M8 and M9 $200\ \mu m$ and M5, M6, M10, M5B, M6B, M10B $500\ \mu m$)

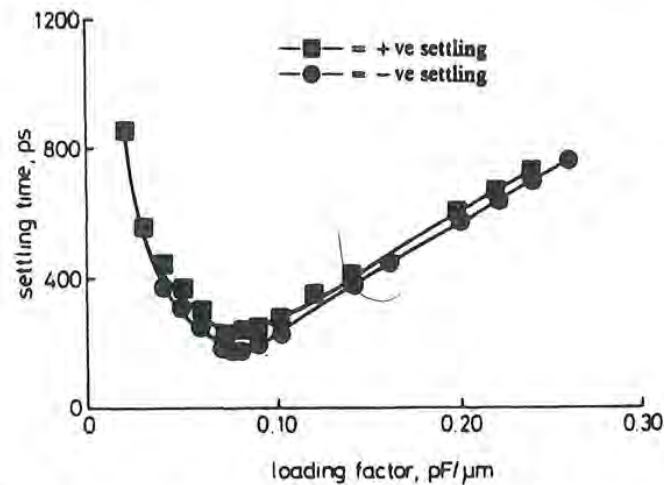


Figure 8.23 Settling time characterisation curve for amplifier in Figure 8.22

8.7.4 Fast Settling Architectures

The minimum settling time of the amplifier in Figure 8.21 permits its use in sampled data systems with maximum switching rates up to 400 MHz [22]. However, a second generation of amplifier architectures with even lower settling times aimed at higher frequency systems is possible, based on both non-pushpull and pushpull architectures [13,15]. We now concentrate on fast pushpull architectures which make use of the previously described current mirrors.

The current mirror using composite MESFET's of Figure 8.8 can be used to realise a fast settling push-pull amplifier and the circuit is shown in Figure 8.22. The current mirror comprises M4 - M8 and M4B - M8B, and also M9 - M11 which implement the required current source. M1 - M3 and M1B - M3B implement the double cascode dual input driver also required. For evaluation of the speed capability of operational amplifiers, a characterisation technique has been developed in which settling time is simulated as a function of load capacitance. For the amplifier in Figure 8.22, such settling time characterisation curves, for both positive and negative output voltage steps, are shown in Figure 8.23. In order to facilitate use of these curves for high speed circuit design [14,23], the load capacitance on the horizontal axis is divided by the amplifier's driver device gate width and referred to as loading factor. From Figure 8.23, the minimum settling time reaches 230 ps. It can be seen that the circuit features excellent symmetry of positive and negative settling. The simulated performance parameters for this amplifier are summarised in Table 8.4.

The double cascode current mirror using separate bias chain of Figure 8.6 can be used to realise a high gain, fast settling amplifier as shown in Figure 8.24 with drive circuitry similar to that already utilised in Figure 8.22. The

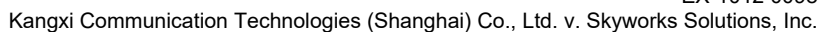


Figure 8.24 Amplifier using current mirror with separate bias chain
($V_s=5V$; $V_{B1}=-2.2V$; $V_{B2}=-3.6V$ all devices $100\text{ }\mu\text{m}$ except $M5, M6, M11, M16, M17\text{ }500\text{ }\mu\text{m}$)

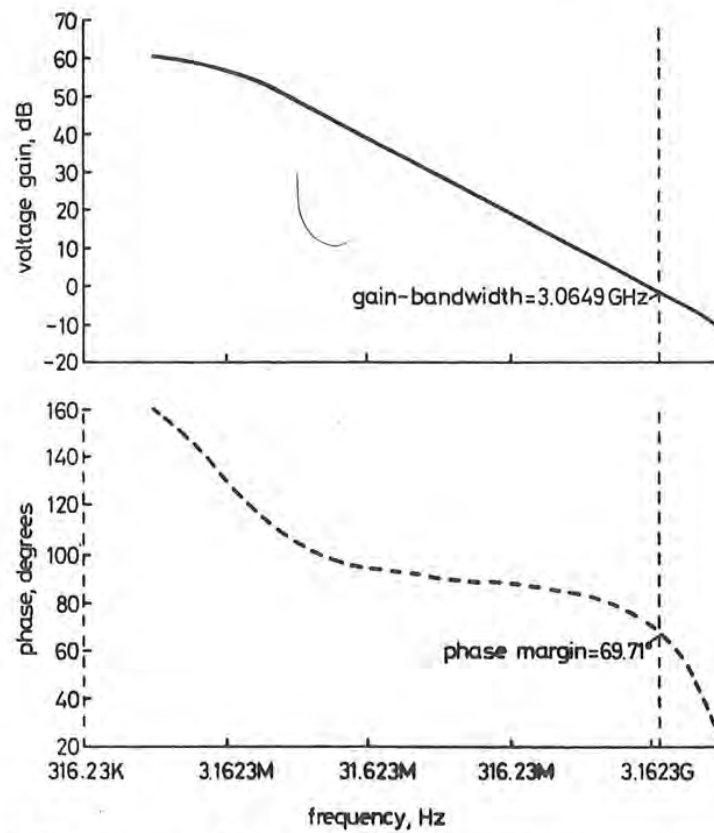


Figure 8.25 Gain and phase versus frequency responses for amplifier in Figure 8.24

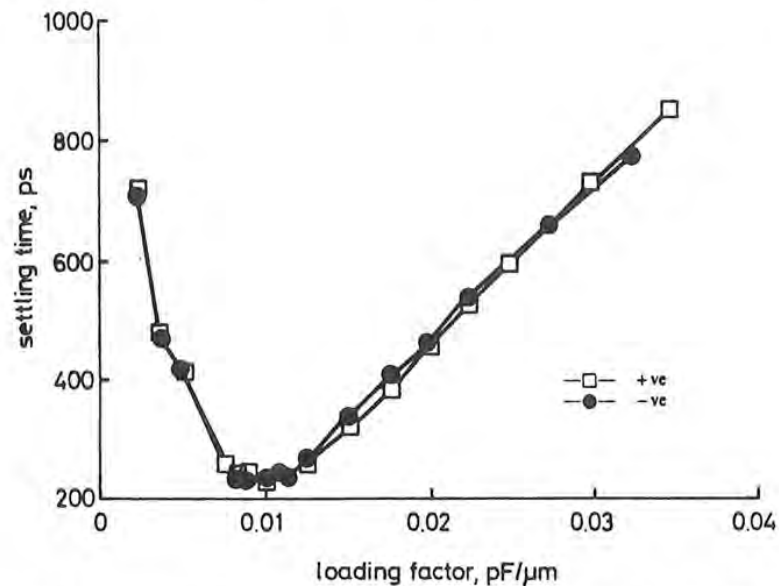


Figure 8.26 Settling time characterisation for amplifier in Figure 8.24

simulated gain and phase versus frequency responses for this amplifier are shown in Figure 8.25. The settling time characterisation curve is shown in Figure 8.26 (Key performance parameters are summarised in Table 8.4). The minimum settling time for positive and negative steps is the lowest achieved figure of 215 ps. The achievement of such fast settling amplifiers is an encouraging necessary step towards the development of switched capacitor filters with switching frequencies approaching 1 GHz.

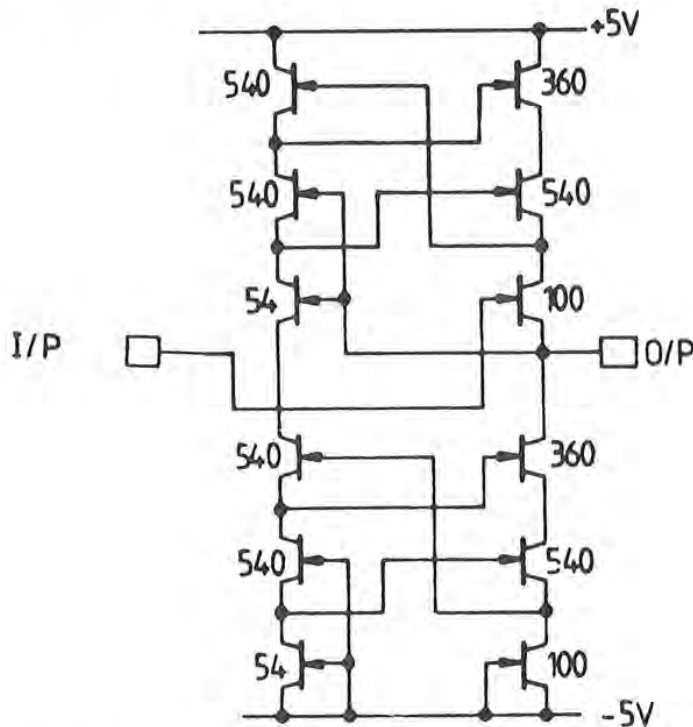


Figure 8.27 High quality unity gain buffer amplifier

8.8 Buffer Amplifiers

In integrated circuit design, on-chip impedance levels are usually much higher than off-chip impedance levels. It is thus necessary to introduce, into the chip output ports, buffer amplifiers which can tolerate off-chip loading impedances. Such buffers usually require a gain of unity, high input resistance, low input capacitance and ability to drive relatively high load capacitances. A suitable circuit for implementation in GaAs MESFET technology is shown in Figure 8.27. It is derived from the high gain double cascode amplifier of Figure 8.21 by a number of operations. We connect the original input terminal to the negative supply and create a new input terminal from the disconnected gate of MESFET M4. This results in a

buffer amplifier with a relative gain error from unity of the order of $1/A$, where A is the gain of the original amplifier, giving in this case a gain error of 0.1 %. The circuit in Figure 8.27 has a bandwidth of at least 100 MHz driving a signal of 1 V_{rms} into a 2 pF load.

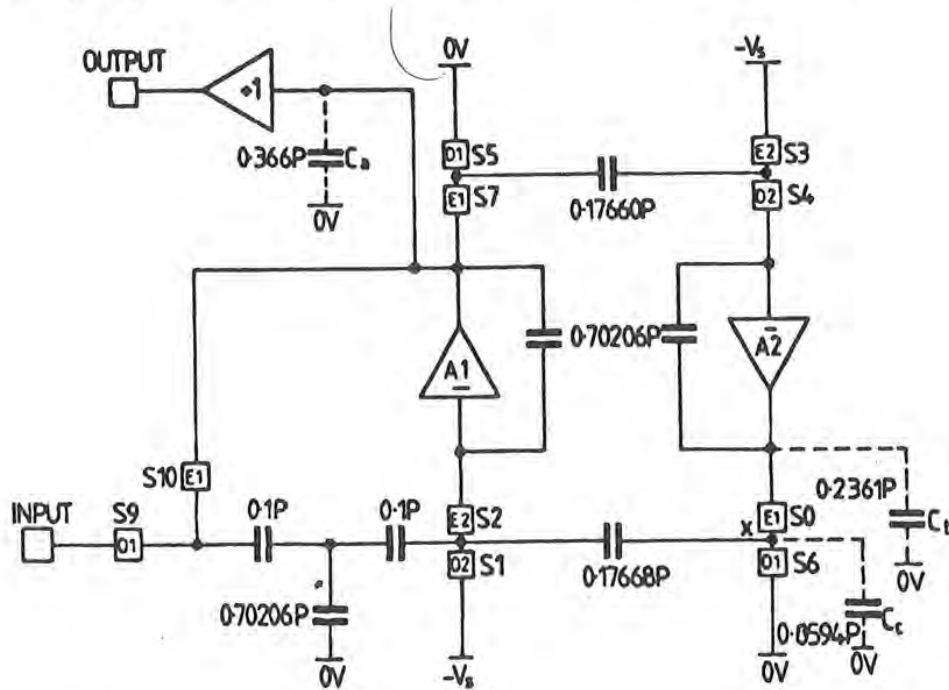


Figure 8.28 2nd order SC filter for implementation

8.9 Applications

8.9.1 Switched Capacitor Filter Example

A 2nd order switched capacitor bandpass filter designed to realise a Q-factor of 16, midband gain of unity and midband frequency of $1/25$ th of the switching frequency is shown in Figure 8.28 [11,14]. The design maximum switching frequency is 250 MHz using the single-stage, double-cascode, double-level-shifting operational amplifier design of Figure 8.21. When switched capacitor circuits are implemented in GaAs technology, switch control circuits are required to prevent forward biasing of the switch device gate-channel Schottky diodes [14]. In this filter example, the switch control circuit used is that of [24], which features low power consumption and low signal dependence of clock feedthrough. The switched capacitor circuit is designed for high frequency operation using an optimisation technique [11,14] based upon the amplifier settling time characterisation curves. In this approach, amplifier load capacitances are introduced to maintain acceptable settling behaviour and stability in all switching states.

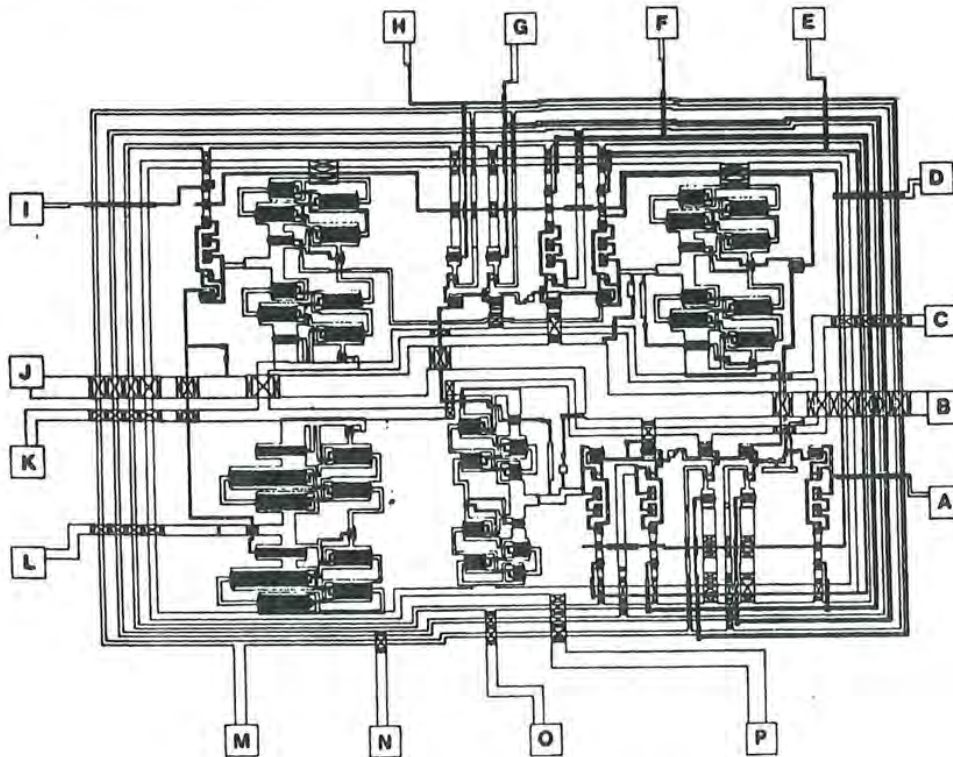


Figure 8.29 Layout plot for GaAs switched capacitor filter; total size 3.3 mm x 2.6 mm

The capacitors C_a , C_b and C_c in Figure 8.28 have been introduced as a result of the optimisation procedure.

The circuit was laid out using MAGIC with a specially written technology file for the Anadigics 0.5 microns GaAs process and a layout plot is shown in Figure 8.29. The size of the chip, which was fabricated by Anadigics, is 3.3 mm x 2.6 mm and the power consumption is 440 mW.

The filter was found to operate very accurately up to beyond its design maximum switching frequency of 250 MHz. The amplitude/frequency response was measured for switching frequencies of 300 MHz, 350 MHz and 400 MHz. The responses for 300 MHz and 400 MHz are shown in Figures 8.30a and b, respectively. Expanded passband plots for the above switching frequencies are shown in Figures 8.31a and b. Peak gains, -3 dB frequencies and calculated midband frequencies and Q-values are tabulated in Table 8.5. Midband frequency accuracies range from less than 1 % to about 2 % and represent a considerable improvement over the previous results presented in [25]. The Q-factor accuracy is reasonable for a 300 MHz switching frequency but the Q-factor reduces for higher switching frequencies. The peak noise at the output of the filter measured for a measuring bandwidth of 10 kHz is at -75 dB relative to the maximum signal

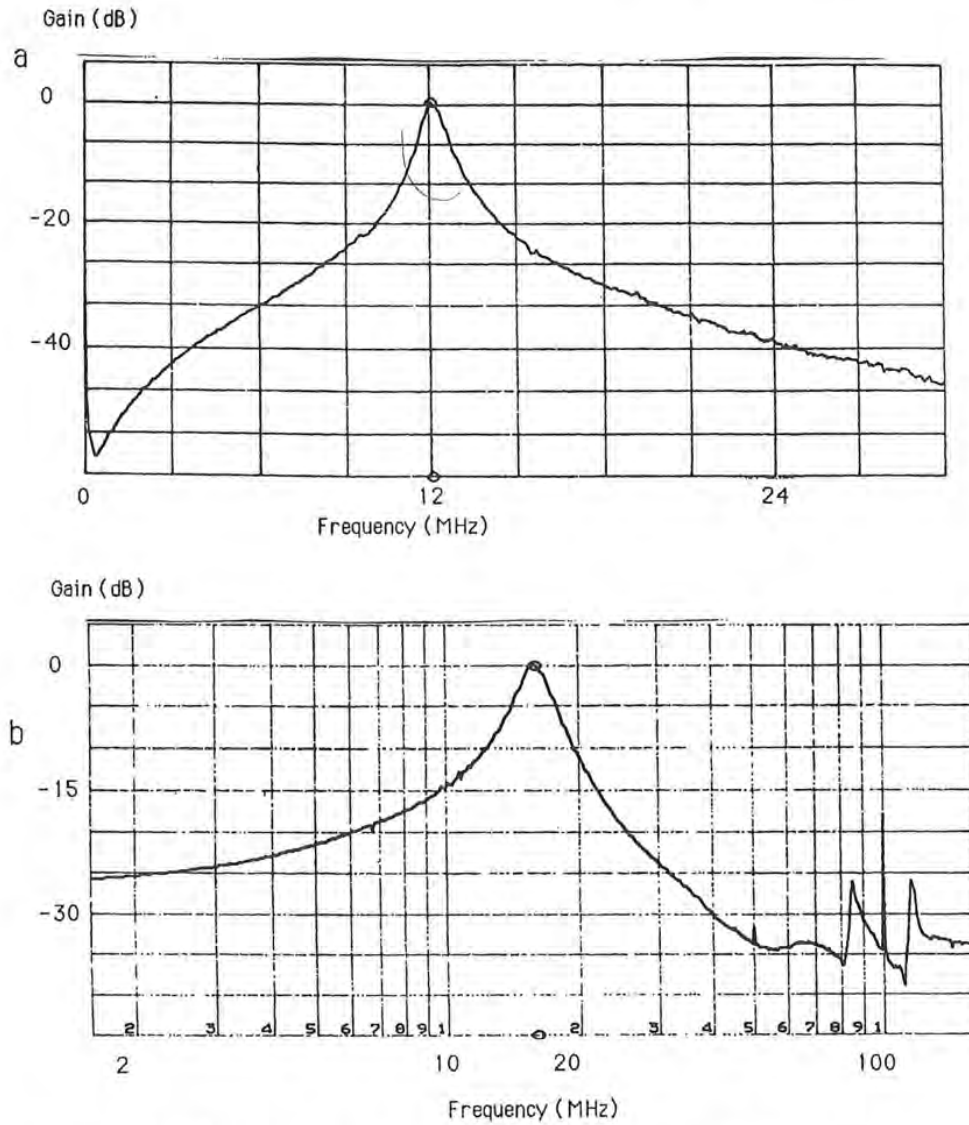


Figure 8.30 Measured amplitude/frequency responses of filter
 a 300 MHz switching frequency b 400 MHz switching frequency

Table 8.5 Measured Filter performance data

Switching Frequency (MHz)	Peak Gain (dB)	-3dB Frequencies		F_o $= (F_1 F_2)^{1/2}$ (MHz)	Q-factor $= F_o / (F_2 - F_1)$
		F1 (MHz)	F2 (MHz)		
300	-0.15	11.7	12.5	12.1	15
350	-0.20	13.5	14.7	14.1	12
400	-0.15	14.6	16.9	15.7	7

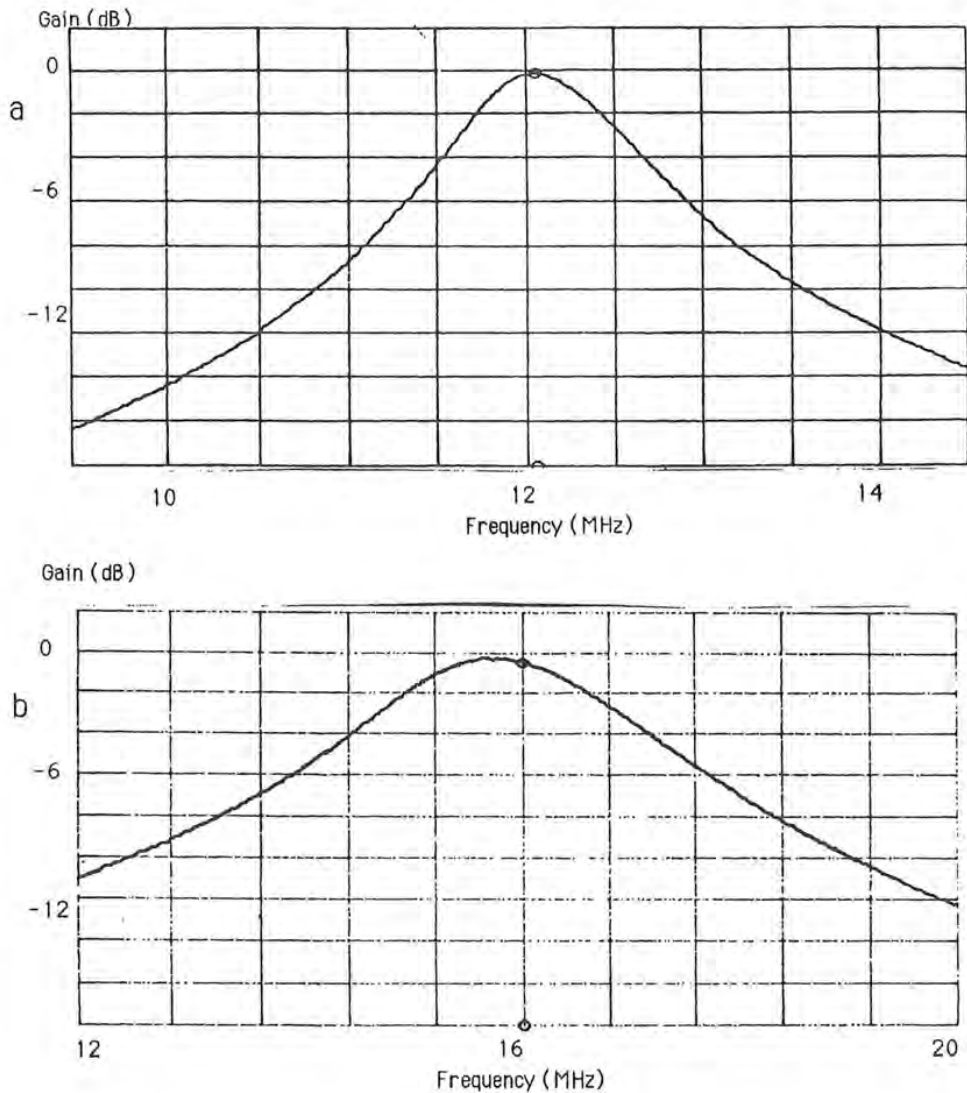


Figure 8.31 Measured expanded passband responses
a 300 MHz switching frequency **b** 400 MHz switching frequency

level. Observation of the filter output signal at the resonant frequency indicates a DC offset voltage of less than 50 mV and reasonably low levels of clock feedthrough.

In spite of the results achieved, the operational amplifier used in the design is relatively slow compared with more recent designs, such as those of Figures 8.22 and 8.24, and advanced designs implemented using state-of-the-art technology [26]. Thus future opportunities are opened up for SC systems operating with GigaHertz clock rates.

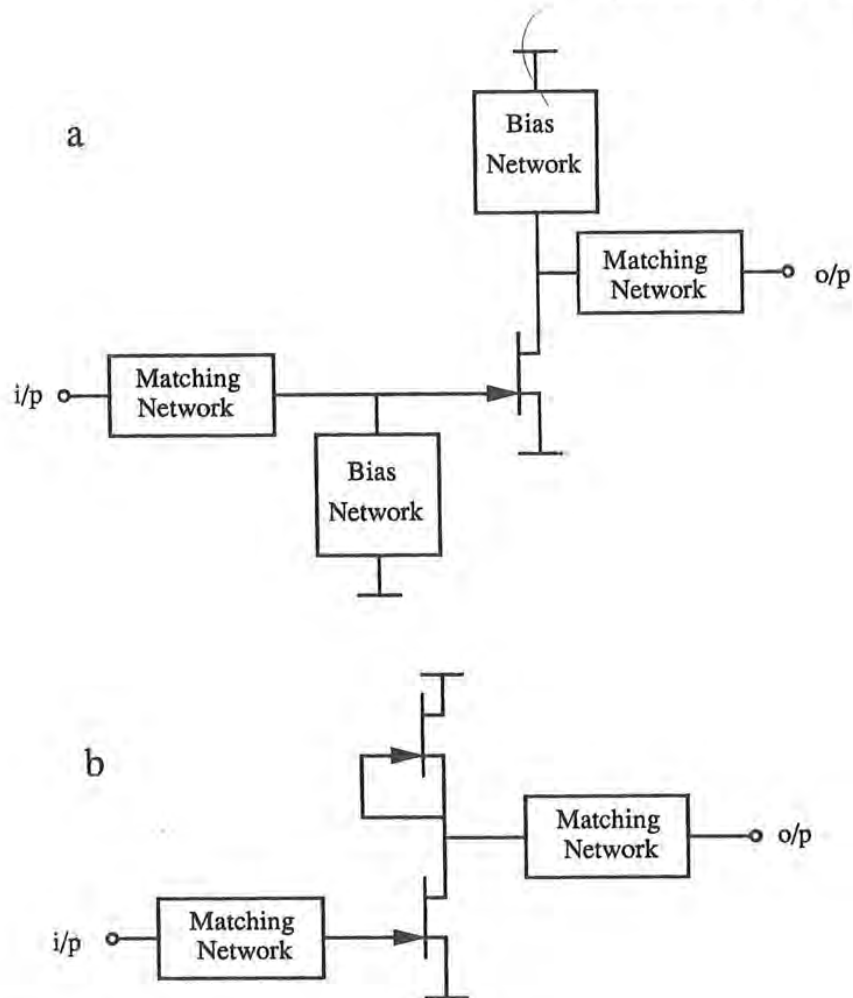


Figure 8.32 Microwave amplifier architectures
a Single MESFET **b** Inverter structure

8.9.2 Microwave Applications

8.9.2.1 Microwave Amplifiers

Traditional designs for microwave amplifier stages are based on either the single GaAs MESFET of Figure 8.32a or the classical inverter of Figure 8.32b [27,28]. In either case, the non-linear nature of the I_d vs V_{gs} characteristic of the GaAs MESFET (eg Equation 8.7) introduces a significant source of non-linearity. In many microwave systems, high linearity is essential and this means that conventional circuits often have to be operated in a 'backed-off' condition, that is with AC signals which are only a small fraction of the DC quantities [29].

However, a new generation of microwave amplifiers can be developed by replacing the active components in such conventional amplifier stages by the linearised transconductor of Figure 8.16a. The results in Figures 8.17 and 8.18 and also Table 8.3 indicate that this basic amplifier architecture will allow more linear circuit operation and permit AC signals which are larger proportions of the DC quantities resulting in improved signal handling capability, lower distortion and reduced chip area and power consumption.

8.9.2.2 Microwave Combiners

Apart from microwave amplifiers, a number of other microwave applications for advanced GaAs circuit designs are envisaged. Microwave combiners are important components in many microwave systems [30]. The successful achievement of a linearised transconductor as in Figure 8.16a could allow the realisation of combiners in monolithic microwave integrated circuit form by directly interconnecting the outputs of a number of transconductors with separate input signals. The high input impedance of the transconductors facilitates easy interfacing with preceding analogue or digital circuitry.

The achievement of low intermodulation distortion in this application may require the introduction of cascode techniques, as described in Section 8.3.3.2, within the transconductors [13].

8.9.2.3 New Approach to Integrated Microwave System Design

The adoption of more complex circuits for microwave applications could bring about a radically different design approach for monolithic microwave integrated systems. In conventional microwave IC design, typical GaAs MESFET gate widths are of the order of 300 microns. However, much smaller devices close to the minimum gate width for the process, typically 16 microns, could have decisive advantages. Such a twentyfold reduction of the scale of the devices and their interconnections in comparison with the signal wavelength would significantly increase the frequency range for which low frequency circuit techniques are useable. Bulky transmission lines for interconnections between components could in many cases be avoided and circuits can be envisaged which consist of 'islands' of high density circuitry, with interconnections between islands being conventional transmission lines.

One interesting possibility for high circuit density microwave systems is to exploit the wide bandwidth capability of current amplification [31], as described in Chapter 4. The linear current mirror in Figure 8.9 could be used as an amplifying component to achieve a good compromise between high gain and high bandwidth beyond that achievable with conventional architectures.

8.9.2.4 Microwave Buffers

Such a novel approach to monolithic microve integrated system design introduces a requirement to interface the high impedance on-chip microwave circuitry with low impedance off-chip microwave systems, thus leading to the concept of a microwave buffer. It is proposed that such a buffer could be realised using the transconductor of Figure 8.16a operating into a 50 Ohm load resistance. By making the output devices M2 and M4 about 100 microns wide, a transconductance of 20 milli-Siemens is achieved giving a unity voltage gain with reasonable linearity and efficiency.

8.9.3 Optical Applications

8.9.3.1 Driver Circuits for Wideband Optical Systems

In optical communication systems, information is contained in the optical signal in the form of frequency modulation or intensity modulation [32]. Both optical frequency and intensity are proportional to the current in a laser diode, which is non-linearly related to laser diode voltage. The requirement for linearity, which applies to digital as well as to analogue systems, makes it desirable that the driver circuit should have an output current which is linear with modulating signal. In present optical communication systems, with typical bandwidths of 0.5 GHz, the driver and detector circuits are realised using bipolar transistors.

The growth of communications is creating a demand for wideband optical systems operating up to around 15 GHz, necessitating the use of III-V semiconductor materials, and in particular Gallium Arsenide [14]. Thus there is a requirement for a range of GaAs building block circuits, not only for driver and detector circuits but also for non-regenerative optical-electronic-optical repeater circuits required while all-optical repeaters [32] are being developed.

Two possible applications of the GaAs circuits developed in this Chapter within the context of optical systems are shown in Figure 8.33. Figure 8.33a shows a proposal for a driver circuit for a laser diode. The current source Ib defines the quiescent diode current. The transconductor is the linearised transconductor developed in Section 8.6 and shown in Figure 8.16a. The high impedance voltage input provides convenient interfacing with both analogue and digital preceeding circuits. The transconductor can be operated with larger signal swings, minimising power consumption and chip area and optimising system performance.

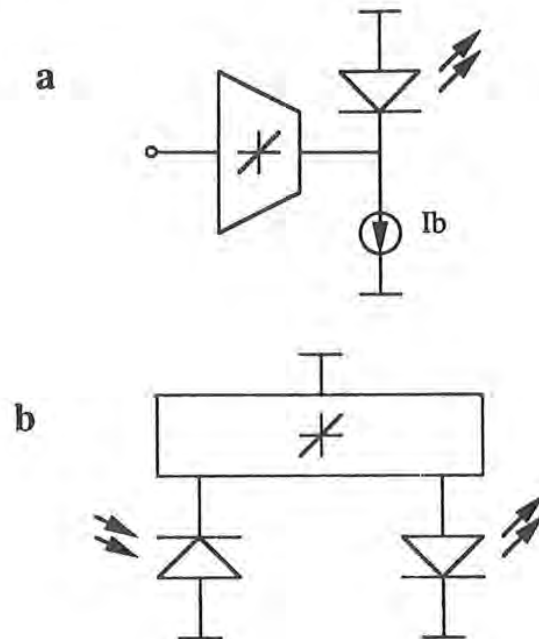


Figure 8.33 Circuits for optical applications
a Linear driver circuit **b** Non-regenerative repeater

8.9.3.2 Optical Repeater Circuits

The circuit in Figure 8.33b is a proposed non-regenerative linear repeater. The current mirror block is the linear negative current mirror developed in Section 8.3.4 (see Figure 8.9). The circuit achieves a linear current gain given by Equation 8.13. By making the gate width of M4 ten times that of the other MESFET's (which may be minimum size), a current gain of 20 dB can be achieved which is acceptable in some applications. The quiescent current of the laser diode is dependant on the gate width of M4 and an additional current source may be added. This circuit could be used as a photodetector circuit with the laser diode replaced by a resistor and voltage buffer.

8.9.4 Continuous-time Filtering

Filters play a major role in communication systems. GaAs technology has been used to realise integrated switched capacitor filters at frequencies up to 20 MHz, as described in Section 8.9.1, and it is anticipated that frequencies up to 100 MHz should be possible with this technique. Continuous-time filters realised using transconductors and capacitors implemented in GaAs technology could provide a means of realising integrated precision filters at higher frequencies.

The linearised transconductor developed in Section 8.6. is a candidate component for high frequency filter realisation. However, for filter real-

isation, a number of transconductor features are necessary which this transconductor does not yet have. These include the possibility of realising a negative transconductance and the electronic control of the transconductance value. The successful achievement of these requirements could lead to the realisation of filters which are viable for frequencies beyond 1 GHz.

8.10 Conclusions

Gallium Arsenide technology is maturing rapidly with the achievement of higher yields, lower costs and faster turnarounds. Current developments in modern wideband communication systems are creating a firm need for circuit and system components realised in this technology. In this Chapter, we have presented some design techniques specifically developed to yield optimum high frequency performance, while overcoming the material technological difficulties of Gallium Arsenide. It is hoped that the building blocks presented in this Chapter, ranging from low level subcircuits such as current mirrors, to experimentally confirmed system components such as high precision filters, will help to bring about the realisation of the possibilities that undoubtedly lie ahead. As in other technologies, the use of current is an essential aspect of Gallium Arsenide circuit techniques if the fastest circuit performance is to be achieved.

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