

**UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.**

**Before the Honorable MaryJoan McNamara
Administrative Law Judge**

In the Matter of

**CERTAIN WIRELESS FRONT-END MODULES
AND DEVICES CONTAINING THE SAME**

Inv. No. 337-TA-1413

COMPLAINANTS' *MARKMAN* BRIEF

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I. INTRODUCTION

Complainants Skyworks Solutions, Inc., Skyworks Solutions Canada, Inc., and Skyworks Global Pte. Ltd. (collectively, “Skyworks” or “Complainants”) submit this brief to address the meanings of six claim terms that the parties to this Investigation dispute. Because Skyworks’ proposed constructions are consistent with the intrinsic record and extrinsic evidence as shown below, Skyworks’ proposed constructions should be adopted.

By contrast, Respondents’ proposed constructions seek to do what infringers nearly always try to do—create through the *Markman* process defenses that simply do not exist in the ordinary meaning of the plain claim language. Despite there being no lexicography or disclaimer whatsoever, for example, Respondents ask the ALJ to import limitations into the patents’ claims through otherwise broad terms like “amplify” and “integrated circuit.” Respondents would twist these terms as limited solely to one type of amplifier (the type that increases current) or one type of integrated circuit (the type having a single die) to the exclusion of other, well-known types of amplifiers and integrated circuits—ignoring express disclosures in the patents that these other types are also covered embodiments. Respondents do so, moreover, inconsistently. For example, Respondents would limit the claims to an “increasing” type amplifier despite admitting (in their “current mirror” construction) that this same circuit must be capable of achieving any “target gain” (including unity gain). Respondents then argue that simple terms like “inhibiting” and “low-frequency” are somehow indefinite—despite Respondent Kangxi Communication Technologies (Shanghai) Co., Ltd. Inc. (“KCT”) having represented in an *Inter Partes* Review (“IPR”) petition to the Administrative Patent Judges (“APJs”) of the Patent Trial and Appeal Board (“PTAB”) just last month that “POSITAs understood” these “well-known” terms. Respondents’ litigation-driven constructions should be rejected.

Starting with the “current mirror” term from U.S. Patent No. 8,717,101 (the “’101 patent”), the parties agree that a “current mirror” can “achieve a target gain,” which can be a unity gain (meaning that the output current is equal to the input current). Skyworks’ proposed construction explains the essential characteristic by which a “current mirror” achieves such a gain: by “having at least two transistors with their base or gate terminals tied together.” This requirement is based on both the intrinsic record (including the prosecution history) and the extrinsic evidence, which consistently shows and describes current mirrors as having at least two transistors with their base or gate terminals tied together. In fact, one of Respondents’ own extrinsic references—RXM-0005 (Toumazou)—shows this very structure and calls it “the *simple theme* from which ... variations” of current mirrors are made. RXM-0005 (Toumazou) at 251.¹ Because Skyworks’ proposed construction captures this “simple theme, while Respondents’ and Staff’s excludes it, Skyworks’ proposed construction should be adopted.

The parties also dispute two similarly-worded terms from the ’101 patent—“amplifying the control current using a current mirror of a current amplifier to generate a correction current” (in claim 17) and “a current amplifier configured to amplify the control current to generate a correction current” (in claims 1 and 21). These terms each present the same dispute: whether the claims cover amplifiers configured to “achieve a target gain of the control current” as Skyworks contends, or are instead limited solely to the type of amplifiers that “increase the control current” as Respondents and Staff argue. Whereas Skyworks’ construction is consistent with both the intrinsic and extrinsic evidence, including well-known “unity gain” current amplifiers that do not “increase” their input, Respondents’ and Staff’s proposed construction would improperly exclude well-known types of current amplifiers that are within the scope of the

¹ In this brief, emphasis appearing in quotations has been added unless otherwise indicated.

patent’s disclosed embodiments. Because (1) express claim language recites that the “current mirror of a current amplifier” is what is used to “amplify” the control current, (2) it is undisputed that a “current mirror” can “achieve a **target** gain,” and (3) Respondents and Staff identify no lexicography or clear disclaimer limiting the claims solely to one type of amplifier (and, indeed, the patent states that the claimed amplifier should be capable of achieving “**any** suitable gain”), Skyworks’ proposed construction should be adopted. *See, e.g., Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996) (finding a construction that excludes a disclosed embodiment “is rarely, if ever, correct”); *Oatey Co. v. IPS Corp.*, 514 F.3d 1271, 1276-77 (Fed. Cir. 2008) (absent lexicography or disclaimer, we “do not interpret claim terms in a way that excludes embodiments disclosed in the specification”).

Turning to U.S. Patent No. 9,917,563 (the “’563 patent”), the parties dispute the term “integrated circuit”—specifically whether an “integrated circuit” can be “integrated on one or more dies” as Staff and Skyworks contend, or is instead limited solely to the types of integrated circuits that are “integrated on a [single] die” as Respondents argue. Because the intrinsic record is clear that an “integrated circuit” can use multiple dies, and because there are well-known types of “integrated circuits” made from one or more dies, Staff’s and Skyworks’ proposed construction should be adopted. *Vitronics*, 90 F.3d at 1583; *Oatey*, 514 F.3d at 1276-77.

For the remaining two claim terms—U.S. Patent No. 9,450,579’s (the “’579 patent”) “inhibiting” and “low-frequency” terms—the dispute centers on Respondents’ argument that skilled artisans would not be able to understand the terms, resulting in the claims being indefinite. Respondents bear a heavy burden to demonstrate their indefiniteness theories by clear and convincing evidence. *See BASF Corp. v. Johnson Matthey Inc.*, 875 F.3d 1360, 1365 (Fed. Cir. 2017). Yet, when Respondent KCT filed an IPR petition for the ’579 patent, it had no

trouble understanding the meanings of these terms and purporting to apply them to the asserted prior art. Indeed, as noted above, KCT's IPR petition states that "POSITAs understood" these "well-known" terms. Inexplicably, KCT says the opposite in this Investigation—that these same terms are now somehow beyond reasonable comprehension. KCT is mistaken. Because a skilled artisan would be able to understand these terms with reasonable certainty based on the intrinsic record (as Staff and Skyworks agree), each is definite. Accordingly, Respondents have failed to meet their heavy burden for these terms, and Staff's and Skyworks' proposed constructions should be adopted.

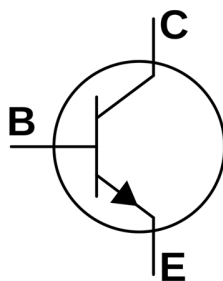
II. TECHNOLOGY BACKGROUND

A. Analog Circuits

An electrical circuit works, in part, by allowing the flow of electric charge through the circuit. The flow of charge is referred to as "current," while the electrical potential difference between two points in a circuit is called "voltage." A common analogy used to explain voltage and current is water traveling through a pipe, where voltage is analogous to the water pressure and current is analogous to the flow of water. The higher the pressure (voltage), the faster the flow (current). Wentzloff Decl. at ¶ 23.

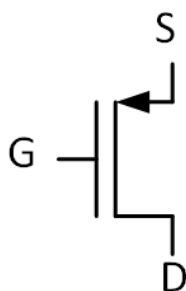
A common circuit component is a transistor, which can be thought of as having a variable resistance that depends upon the voltage or current into its control terminal.² One type of transistor is known as a bipolar junction transistor ("BJT"), shown in the figure below, which has three terminals: an emitter (E), a base (B), and a collector (C).

² Resistance in the context of circuits refers to how much a component resists the flow of current. Because a transistor can control how much current is able to flow through it, it can be thought of as having variable resistance.



A small current going into the base (B) of the transistor controls a larger current flowing from the collector (C) to the emitter (E). Wentzloff Decl. at ¶ 26.

Another type of transistor is called a Metal-Oxide-Semiconductor Field-Effect Transistor (“MOSFET”), shown in the figure below, also having three terminals: a gate (G), a source (S), and a drain (D).



A voltage difference applied between the gate (G) terminal and the source (S) terminal, which is called the gate-source voltage, controls a current flowing between the drain (D) and source (S) terminals and, thereby, the effective resistance between the source and drain. Wentzloff Decl. at ¶ 27.

1. Types of Amplifiers

An amplifier takes an input signal and produces an output signal that has a target gain relative to the input signal, while preserving the input signal’s characteristics like frequency, shape, or waveform. An amplifier can be a voltage amplifier or a current amplifier. A voltage

amplifier's gain is the ratio of its output voltage signal to its input voltage signal. Likewise, a current amplifier's gain is the ratio of its output current signal to its input current signal.

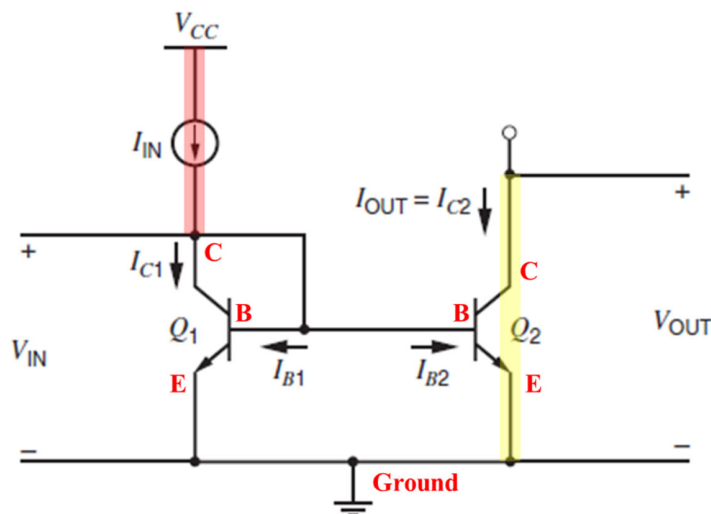
Amplifiers can be constructed to have any suitable gain. In some cases, the amplitude of the output signal may be greater than that of the input signal, in which case the amplifier's gain is greater than one. Many amplifiers have "unity gain," *i.e.*, a gain equal to 1, meaning the amplitudes of the output signal and the input signal are the same. Wentzloff Decl. at ¶¶ 28-29.

Unity gain amplifiers can serve a wide variety of purposes. For example, a unity gain current amplifier can serve as a buffer, isolating different parts of a circuit so that circuitry downstream of the amplifier does not negatively impact circuitry upstream of the amplifier. In an electronic circuit, for instance, the term "load" is used to refer to a component that draws power from the circuit in order to perform a particular function. During operation, the power demands of the load will often vary with time—drawing relatively little power during idle moments and drawing more power when the function the load performs is in active use. As an electronic device is used, the use of the device can cause variations in how the circuit downstream of the current amplifier operates, which can in turn cause variations in the current it draws. An example of a variation in usage would be to introduce a larger load (such as more resistance) at the output of the amplifier. A unity gain current amplifier can be beneficially used to isolate the input to the amplifier from the load that is connected to the amplifier's output and that uses the output current from the current amplifier. Using such a unity gain current amplifier, this output current will remain stable and equal to the input current despite variations in the load, because the unity gain current amplifier ensures that the output current remains substantially equal to the input current due to the amplifier's unity gain. Wentzloff Decl. at ¶¶ 30-34.

2. *Current Mirrors*

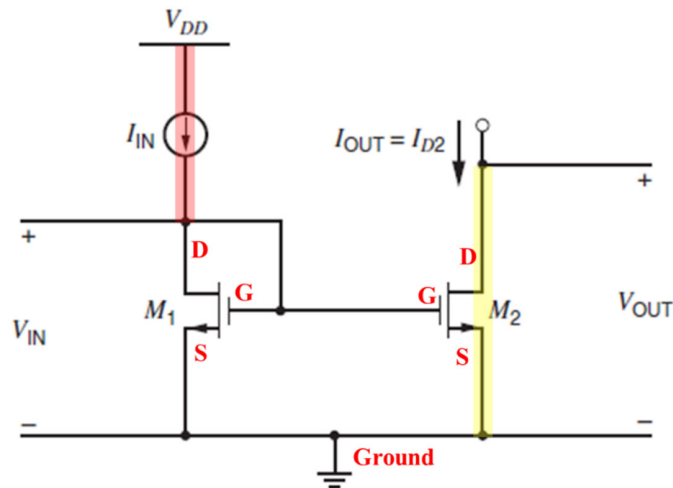
One type of current amplifier is known as a “current mirror.” Current mirrors have long been used as building blocks in analog circuits to mirror or replicate a reference current through an input branch into one or more output branches.

A basic current mirror with one input branch and one output branch is shown below. It has two transistors, specifically bipolar junction transistors (“BJTs”) in this example, labeled Q_1 (left) and Q_2 (right). As shown in the figure, the base terminals of these two transistors, labeled B, are connected and thus tied together.



CXM-0001 (Analysis and Design of Analog Integrated Circuits) at 253, Figure 4.2 (“The simplest form of a current mirror consists of two transistors. Fig. 4.2 shows a bipolar version of this mirror.”). Wentzloff Decl. ¶¶ 35-36.

As an alternative to using BJT transistors, a current mirror could instead use two MOSFET transistors as shown below. In this case, the MOSFETs’ gate terminals, labeled G, are connected and thus tied together—akin to tying together the BJTs’ base terminals in the example above.

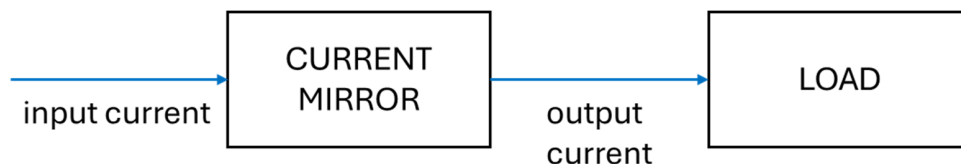


CXM-0001 (Analysis and Design of Analog Integrated Circuits) at 256, Figure 4.4. Wentzloff Decl. ¶41.

The output current of the current mirror can be the same magnitude as the input reference current, creating a current amplifier with unity gain, which is achieved by sizing the components of the output branch (*e.g.*, the I_{OUT} branch and its transistor M_2 , highlighted yellow in the figures above) to be the same size as the components of the input branch (*e.g.*, the I_{IN} branch, highlighted red in the figures above, and its transistor M_1). Alternatively, an output branch can be sized differently than the input branch, in which case the output current can be a scaled up or scaled down version of the input reference current, achieving non-unity gain. Wentzloff Decl. ¶¶36-42.

A current mirror is beneficial, whether it has unity or non-unity gain, because its output current is controlled by the input current, regardless of load variations downstream of the current mirror connected to its output that would otherwise cause the input current to vary (*e.g.*, if the load were directly connected to the input current with no current mirror). In a unity gain current

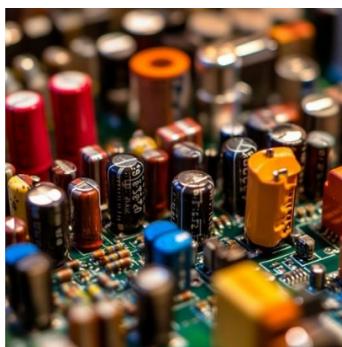
amplifier, this means the output current is the same as the input current, regardless of load variations.



In other words, in the absence of the current mirror, variations in the load that is connected to the output current would cause the output current to vary. By using a current mirror, however, the value of the output current will instead depend only on the input reference current, independent of any load variations downstream of the current mirror. Wentzloff Decl. ¶¶ 43-44. To achieve this fundamental mirroring function, a current mirror has a configuration of two transistors having their base or gate terminals tied together, thereby providing a stable output current that replicates the input current without being susceptible to variations of the load connected to the current mirror's output. Wentzloff Decl. ¶¶ 36-37, 43-44.

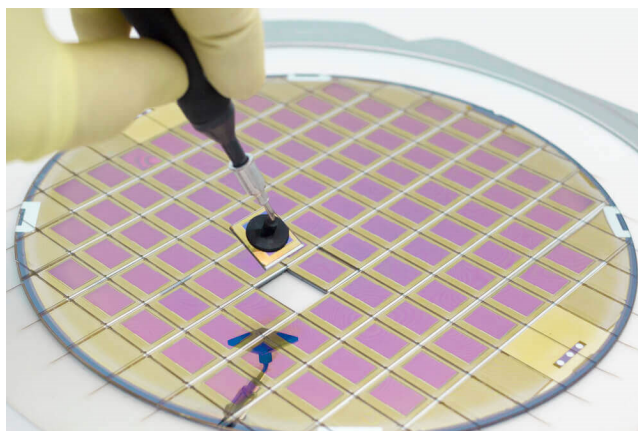
B. Integrated Circuits

Modern electronic devices predominantly use integrated circuits ("ICs"). Before the advent of ICs, circuits were formed by interconnecting individual discrete components, like transistors and capacitors, on a printed circuit board. An exemplary circuit board (green board) having discrete components (components attached to green board) is shown below:



Wentzloff Decl. at ¶¶ 45-46.

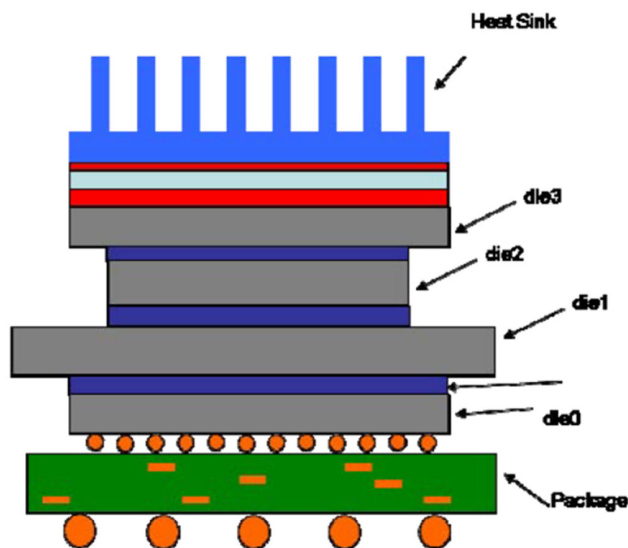
ICs, by contrast, form circuits by fabricating circuit components (transistors, interconnections, etc.) directly on semiconductor substrates. ICs are typically fabricated on semiconductor wafers, which are round discs of semiconductor material, and then cut into individual pieces. A single such individual piece is called a “die” or “chip.” The image below shows an exemplary semiconductor wafer that has been cut into multiple dies:



Wentzloff Decl. at ¶ 46.

Integrated circuits can be formed on a single die or across multiple dies. When formed on a single die, the IC is referred to as a “monolithic” integrated circuit. CXM-0007 (The Authoritative Dictionary of IEEE Standards Terms) at 708 (“**monolithic integrated circuit** An integrated circuit formed in a single piece of the substrate material.”). An IC may also be formed on two or more interconnected dies, referred to as a “multi-die” integrated circuit or “multichip” integrated circuit. *Id.* at 712 (“**multichip integrated circuit** An integrated circuit whose elements are formed on or within two or more semiconductor chips that are separately attached to a substrate.”). A three-dimensional integrated circuit (“3D IC”) is one example of a multi-die

integrated circuit. An exemplary 3D IC having four dies—labeled “die0,” “die1,” “die2,” and “die3”—is shown below:



CXM-0008 (Jain IEEE paper), at 2 (“Figure 1 schematically shows a multi-die 3D IC, with four unequally sized die”), Figure 1. Wentzloff Decl. at ¶¶ 47-49.

C. Radio Frequency Circuits

A radio frequency (“RF”) signal is an electromagnetic signal whose frequency—how quickly the signal oscillates—is sufficiently high that the signal is able to travel (radiate) through the air. Wireless communication, like cellular signals received by a cell phone or Wi-Fi signals received by a laptop or other device, rely on RF signals to carry information through the air. The specific radio frequency used by a particular wireless communication device to carry information through the air is commonly referred to as a “fundamental frequency.” See Kinget Decl. at ¶¶ 44-45, 60.

1. Frequency Bands

If two different wireless devices use the same fundamental frequency to convey information signals through the air, then these signals can interfere with one another, degrading a

receiving device's ability to accurately detect the information being conveyed. To reduce such interference, different types of wireless communications are commonly assigned different frequency "bands"—each being a range of radio frequencies surrounding a specific fundamental frequency—within which to operate, because receivers are able to distinguish information conveyed on different fundamental frequencies. For example, wireless devices using "5 GHz Wi-Fi" are assigned a frequency band ranging from 5.15 GHz to 5.85 GHz, whereas wireless devices using "2.4 GHz Wi-Fi" are assigned a frequency band ranging from 2.41 GHz to 2.47 GHz. Kinget Decl. at ¶¶ 44-45. Similarly, devices that use other types of wireless transmission standards such as the LTE or 5G cellular standards may use still other frequency bands for their transmissions, such as the band from 1.92 GHz to 1.98 GHz for LTE or the band from 3.3GHz to 3.8 GHz for 5G.

2. Interference

Even with separate frequency bands, RF signals can suffer from other sources of interference. A successful wireless device must be able to accurately transmit and receive its desired signals without them being corrupted or degraded by interference caused by other wireless signals. For example, an unwanted signal that is at or near the frequency of the desired signal can be created due to mixing. In particular, when two signals at different frequencies are present, certain circuit components can inadvertently permit these signals to mix together and generate unwanted signals at new frequencies, some of which may cause interference. For instance, a switch may undesirably mix two or more signals, such as a transmit signal at the fundamental frequency and a received signal at a lower frequency, to generate an undesired signal that interferes with the signals of interest. When an undesired signal interferes with a desired signal, such as a signal carrying a bank transaction or an email, the desired signal may become so corrupted as to be undecipherable or to convey inaccurate information to the receiver,

such as an incorrect amount for the bank transaction or garbling the intended contents of the email. As such, techniques and solutions for guarding against the degrading impacts of interference are an important part of wireless device design. Kinget Decl. at ¶¶ 47-49.

III. ASSERTED PATENTS

A. U.S. Patent Nos. 8,717,101 and 9,917,563

The '563 patent claims priority, through a series of continuations, to the '101 patent. Both the '101 and '563 patents share the same title, "Apparatus and methods for biasing power amplifiers," and specification. The '101 patent issued from U.S. Patent Application No. 13/468,749, filed on May 10, 2012. The '563 patent issued from U.S. Patent Application No. 15/377,842, filed on December 13, 2016, which is a continuation of U.S. Patent Application No. 14/825,053, which is a continuation of U.S. Patent Application No. 14/242,150, which is a continuation of the application that issued as the '101 patent. Both the '101 and '563 patents claim priority to U.S. Provisional Application No. 61/486,186 filed on May 13, 2011. Because the '101 and '563 patents share a common specification, all citations in this section are to the '101 patent. JXM-0001 ('101 patent), cover page; JXM-0002 ('563 patent), cover page.

1. Specification

The '101 patent relates to radio frequency ("RF") power amplifier systems and methods for biasing of power amplifiers. The background explains that it can be important to manage the amplification of RF signals because "amplifying the RF signal to an incorrect power level can cause a wireless device to transmit out of band." JXM-0001 ('101 patent) at 1:28-30. As such, the '101 patent explains that there was a need for "improved power amplifier systems" and "improving power amplifier biasing." *Id.* at 1:31-33.

Figure 5 illustrates one embodiment of the inventive power amplifier system of the '101 and '563 patents:

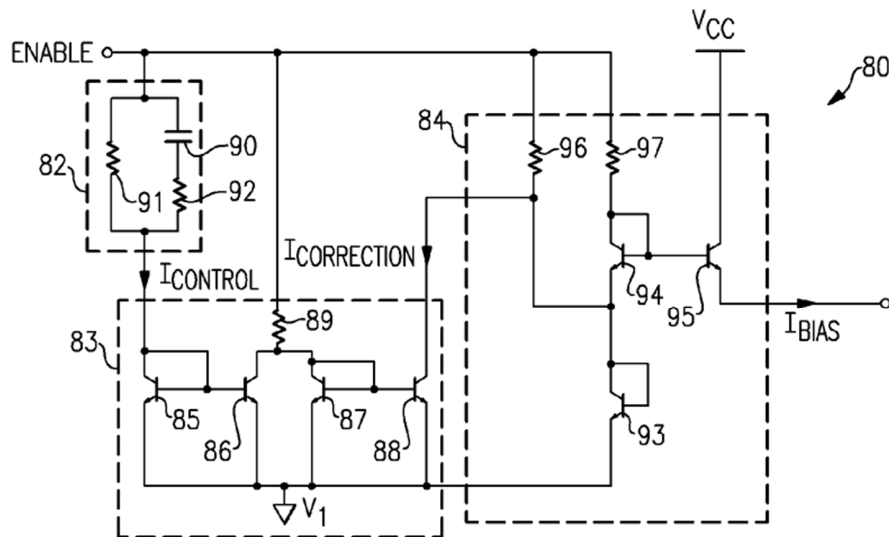


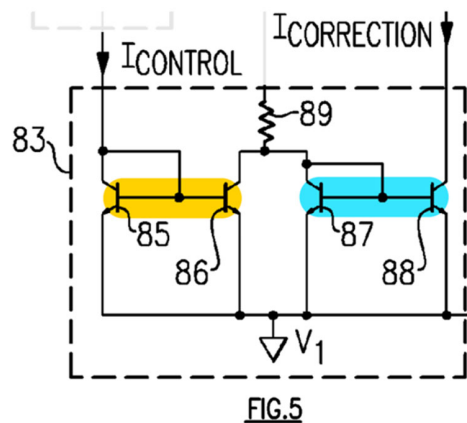
FIG.5

JXM-0001 ('101 patent) at Fig. 5. As shown, the power amplifier bias block 80 “includes a resistor-capacitor (RC) network 82, a current mirror 83, and a primary bias circuit 84.” *Id.* at 10:19-21. During operation, the RC network 82 uses an “enable” signal shown at the top left of Figure 5 to generate a control current labeled “ I_{CONTROL} .” *Id.* at 10:37-38. Amplifier 83 then uses the control current I_{CONTROL} to generate a correction current, labeled “ $I_{\text{CORRECTION}}$.” *Id.* at 10:62-11:1. Finally, primary bias circuit 84 uses the correction current $I_{\text{CORRECTION}}$, at least in part, to generate a bias current for the power amplifier, labeled “ I_{BIAS} ” at the right of the figure. *Id.* at 11:46-67. According to the '101 patent, such a power amplifier system “correct[s] for a variation in gain of the power amplifier when the power amplifier is enabled,” which “can improve the power amplifier’s performance.” *Id.* at 1:46-48; 4:39-42.

The '101 patent uses the terms “current mirror” and “current amplifier” interchangeably, referring to block 83 of Figure 5 as both “current mirror 83” and current “amplifier 83.” *Id.* at

10:62-65.³ Further, the '101 patent explains that “current mirror 83 operates as a current amplifier” that is configured “to achieve a target gain,” which can be “*any* suitable gain.” *Id.* at 10:21-23,11:39-45.

In the embodiment of Figure 5, an excerpt of which is below, the “current amplification circuits” comprise “a plurality of current mirrors combined (e.g., cascaded) to achieve a target gain.” *Id.* at 11:42-45.



Id. at Fig. 5 (partial, annotated); *id.* at 10:67-11:27. As shown in this excerpt of Figure 5, the bases of bipolar transistors 85 and 86 are connected by the trace highlighted in yellow, and the bases of transistors 87 and 88 are connected by the trace highlighted in blue. The '101 patent explains this, stating that “[t]he first NPN bipolar transistor 85 includes ... a base ... electrically connected to a base of the second NPN bipolar transistor 86” and that “a base ... of the third NPN bipolar transistor 87” is “electrically connected ... to a base of the fourth NPN bipolar transistor 88.” *Id.* at 11:7-27.

³ It is axiomatic that the same numeral must designate the same structure throughout a patent. *See* Manual for Patent Examining Procedure (“MPEP”) § 608.02; 37 C.F.R. § 1.84(p)(4) (“The same part of an invention appearing in more than one view of the drawing must always be designated by the same reference character, and the same reference character must never be used to designate different parts.”).

The '101 patent further discloses how components for the power amplifier can be arranged. For example, the '101 patent discloses that the “packaged power amplifier module 300 [of an embodiment of the invention] includes an IC or die 301.” JXM-0001 ('101 patent) at 13:49-50, *id.* at 13:54-56. The specification further explains that the inventive packaging structures can include the “die(s) disposed thereon.” *Id.* at 14:35-41.

2. Prosecution History

During prosecution of the '101 patent, Skyworks added the term “current mirror” by amendment to distinguish the '101 patent’s claimed invention from a different Skyworks patent cited during prosecution (U.S. Patent No. 7,869,775 (hereinafter, “Alon”)) (JXM-0004 ('101 File History) at Skyworks_ITC_000023309-320 (Alon)). One of the originally drafted claims, claim 18, recited in part: “amplifying the control current using a current amplifier to generate a correction current[.]” JXM-0004 ('101 File History), Application at Skyworks_ITC_000023157. The Patent Examiner rejected this claim as being “anticipated by Alon” in an Office Action dated August 2, 2013. *Id.*, Office Action at Skyworks_ITC_000023209. The Patent Examiner stated that Alon’s “device 204 [yellow] can be read as the claimed current amplifier” configured “to amplify the control current [207, blue] to generate a correction current (206 [green])”, as highlighted in the relevant part of Alon’s Figure 2 below:

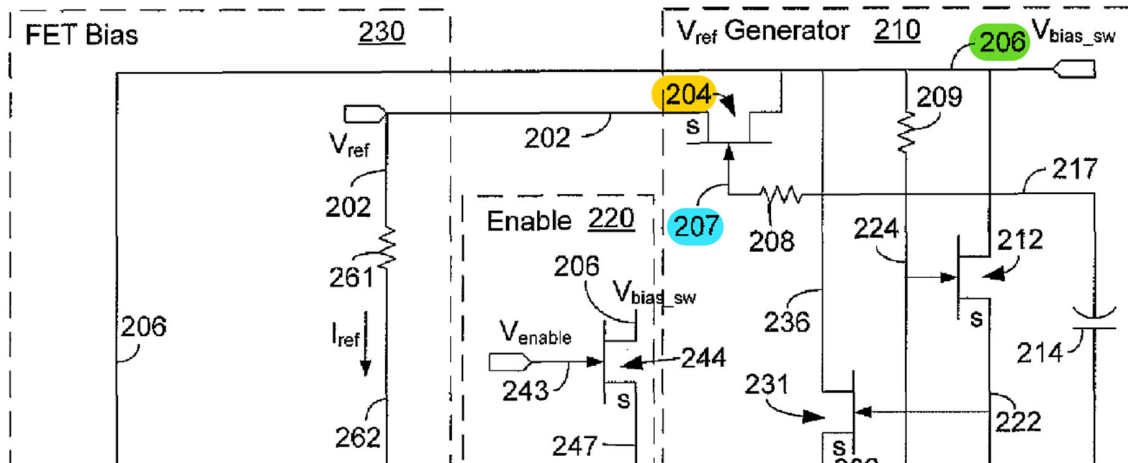


FIG. 2

Id. at Skyworks_ITC_000023210; *id.* at Alon (Skyworks_ITC_000023309-320), Fig. 2 (partial).

The Patent Examiner indicated that dependent application claim 21—which depended from application claim 18—“would be allowable if rewritten in independent form[.]” JXM-0004 (’101 File History), Office Action at Skyworks_ITC_000023211. Application claim 21 additionally recited: “wherein amplifying the control current further includes amplifying the control current using a current mirror of the current amplifier.” *Id.*, Application at Skyworks_ITC_000023158.

Skyworks responded by amending application claim 18 to recite “amplifying the control current using a current mirror of a current amplifier to generate a correction current[.]” JXM-0004 (’101 File History), 10/31/13 Amendment at Skyworks_ITC_000023226 (underlining in original). Skyworks explained in remarks accompanying this amendment that changing the claim language to recite a “current mirror” distinguished the invention claimed in the ’101 patent from Alon, arguing for example that after this amendment application “claim 18 [was] not anticipated nor rendered obvious by the cited art.” *Id.* at Skyworks_ITC_000023230. The Patent Examiner agreed, allowing the ’101 patent claims (as amended) in a Notice of

Allowability dated December 24, 2013. *Id.*, Notice of Allowability at Skyworks_ITC_000023242-445. In his reasons for allowance, the Examiner explained that the “prior art of record [e.g., Alon] ... fails to fairly teach or suggest the claimed circuit comprising ... ‘...the current amplifier including a current mirror’ structurally and functionally interconnected with other limitations in the manner as cited in the claim.” *Id.* at Skyworks_ITC_000023244 (emphasis in original).

B. U.S. Patent No. 9,450,579

The ’579 patent is entitled “Radio frequency devices having reduced intermodulation distortion.” The patent issued from U.S. Patent Application No. 14/833,076, filed on August 22, 2015, which claims priority to U.S. Patent Application No. 13/936,175, filed on July 6, 2013 and issued as U.S. Patent No. 9,148,194. The ’579 patent claims priority to U.S. Provisional Application No. 61/669,045, which was filed on July 7, 2012. JXM-0003 (’579 patent), cover page.

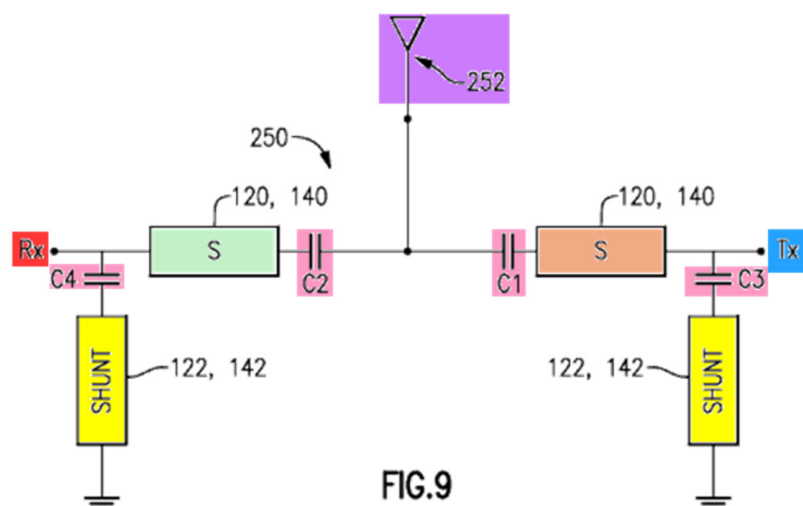
1. Specification

The ’579 patent relates to “a radio-frequency (RF) switch system” designed to reduce signal interference. JXM-0003 (’579 patent) at 1:34-37. The patent explains that “mixing products from other RF signals” can cause “an unwanted signal [to be] added to a desired signal.” *Id.* at 9:2-5. The patent refers to the amount of interference by the unwanted signal as “intermodulation distortion,” or “IMD.” *Id.* at 9:5-7. It explains that IMD is a problem because it “can contribute to the introduction of spurious signals into the RF system, thereby contributing to degradation of overall RF system linearity and IMD performance.” *Id.* at 6:49-53.

The ’579 patent addresses this problem, in part, through a switch configuration with “a capacitor connected in series with the switch configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.” *Id.* at 1:34-40. The

specification explains that the combination of these elements allows “a low-frequency jammer signal [to] be blocked or reduced from mixing with any ON or OFF paths” (*id.* at 9:49-53), which can decrease “interference.” *Id.* at 9:9-14.

Figure 9, reproduced below, illustrates an embodiment of the invention:



Id. at Fig. 9 (highlighting added).

The switching configuration 250 of Figure 9 includes an antenna 252 (highlighted purple). *Id.* at 9:23-24. The antenna 252 can be connected to a receive (Rx) port (highlighted red) of the switching configuration by a switch circuit S (highlighted green). *Id.* at 9:24-26. Similarly, the antenna 252 can also be connected to a transmit (Tx) port (highlighted blue) via a switch circuit S (highlighted orange). *Id.* at 9:28-30.

This switching configuration of Figure 9 includes capacitors (highlighted pink) “to inhibit a low-frequency blocker from mixing with a fundamental frequency.” *Id.* at 9:39-41. The specification states that “[w]ith the foregoing capacitors, a low-frequency jammer signal can be blocked or reduced from mixing with any ON or OFF paths.” *Id.* at 9:49-51. The ’579 patent

states that this “can lead to improvement in IMD performance, especially for low-frequency blocker signals.” *Id.* at 9:51-53.

2. Prosecution History

The prosecution history for the ’579 patent, as relevant here, includes a petition for *Inter Partes* Review (“IPR”) filed by Respondent KCT on November 12, 2024. CXM-0010 (’579 IPR Petition). In this IPR petition, KCT applied certain asserted prior art to the claim term “inhibiting a low-frequency blocker signal from mixing with a fundamental-frequency signal in the RF switch using the first capacitor” appearing in claim 7 of the ’579 patent. *Id.* at 48-52. KCT’s IPR petition characterized these elements of claim 7 as “well-known” concepts that “POSITAs understood[.]” *Id.* at 50.

IV. LEGAL BACKGROUND

The words of a claim “are generally given their ordinary and customary meaning” to a person of ordinary skill in the art at the time of the invention.⁴ *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*) (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). Claim terms should be construed in the context of the patent claim as a whole. *Aventis Pharms. Inc. v. Amino Chemicals Ltd.*, 715 F.3d 1363, 1373 (Fed. Cir. 2013) (citing *Vitronics*, 90 F.3d at 1582).

Ascertaining the ordinary and customary meaning of the claims requires considering “those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean.” *Phillips*, 415 F.3d at 1314 (quoting *Innova/Pure*

⁴ A person of ordinary skill in the art at the time of the alleged inventions of the ’579, ’101, and ’563 patents would have had at the time of the alleged invention at least a bachelor’s degree in Electrical Engineering or a related field and at least two years of training or additional work experience in the area of RF electronics, or a related field. The times of the alleged invention as used herein are the priority dates of July 7, 2012 for the ’579 patent and May 13, 2011 for the ’101 and ’563 patents. Wentzloff Decl. ¶¶ 21-22; Kinget Decl. ¶¶ 36-37.

Water, Inc. v. Safari Water Filtration Systems, Inc., 381 F.3d 1111, 1116 (Fed. Cir. 2004)).

These sources center on the intrinsic record, which is comprised of the claims themselves, the specification, and the prosecution history. *Id.* A claim term must be read in light of the specification of which it is a part. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995). As stated in *Phillips*, “the prosecution history can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be.” *Phillips*, 415 F.3d at 1317. Statements made during Patent Office proceedings, such as *inter partes* review proceedings, “can be considered for claim construction and relied upon” as part of the prosecution history. *Aylus Networks, Inc. v. Apple Inc.*, 856 F.3d 1353, 1362 (Fed. Cir. 2017); *see also, Core Optical Techs., LLC v. Fujitsu Network Commc 'ns., Inc.*, 2016 WL 7507760, at *2 (C.D. Cal. Sept. 12, 2016) (“the intrinsic record” developed during *inter partes* review proceedings “may inform on issues like claim construction”).

A patent specification may provide a special definition for a claim term that is not the same as the ordinary meaning it would otherwise have. *Phillips*, 415 F.3d at 1316. In this case, the specification’s lexicography controls the claim term’s meaning. *Id.*

Although the specification is highly relevant in determining the meaning of a claim term, courts must be careful to avoid “the danger of reading limitations from the specification into the claim.” *Phillips*, 415 F.3d at 1323. In *Phillips*, the Federal Circuit acknowledged that the distinction between reading claims in light of the specification and importing limitations from the specification into the claim can be difficult and stated that “although the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments.” 415 F.3d at 1323. To avoid importing limitations

from the specification into the claims, the Federal Circuit noted that it is important to remember that the purpose of the specification is to teach and enable those skilled in the art to make and use the invention, not to necessarily restrict the invention to specific examples provided in the specification. *Id.*

A specification or prosecution history may contain a disclaimer or disavowal of claim scope. Such a disclaimer or disavowal controls the meaning of a claim term, even if the ordinary meaning of the claim term might otherwise be different, if the disclaimer or disavowal is clear and unmistakable. *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1324-25 (Fed. Cir. 2003). However, “[a]bsent disclaimer or lexicography, the plain meaning of the claim controls.” *Toshiba Corp. v. Imation Corp.*, 681 F.3d 1358, 1369 (Fed. Cir. 2012) (citing *Thorner v. Sony Computer Ent. Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012); *Vitronics*, 90 F.3d at 1580); *see also Apple Inc. v. Omni Medsci, Inc.*, No. 2023-1034, 2024 WL 3084509, at *4 (Fed. Cir. June 21, 2024) (a claim term “must be given the full scope of its plain and ordinary meaning absent lexicography or disclaimer”).

Although intrinsic evidence is most informative in determining the claims’ customary and ordinary meaning, a court may use extrinsic evidence, which “consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises.” *Phillips*, 415 F.3d at 1317 (quoting *Markman*, 52 F.3d at 980 (*en banc*)).

V. DISPUTED CLAIM TERMS

A. “current mirror” (’101 patent claims 1, 2, 10, 11, 17, 18, 20, 21, 22)

Complainants	Respondents	Staff
Plain meaning, which is “one or more circuits configured to mirror a current, which can be configured to achieve a	Plain meaning, such as “one or more circuits configured to mirror a current, which can	Plain meaning, such as “one or more circuits configured to mirror a current, which can

target gain, having at least two transistors with their base or gate terminals tied together”	be configured to achieve a target gain”	be configured to achieve a target gain”
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It is undisputed among the private parties and Staff that the claimed “current mirror” comprises “one or more circuits configured to mirror a current, which can be configured to achieve a target gain....” This agreed portion of the meaning of “current mirror,” as one or more circuits that can achieve any “target gain,” is uniformly confirmed throughout the ’101 patent and the extrinsic evidence. At column 11, for example, the ’101 patent states unequivocally that “[a]s used herein, the term *current mirror* can refer to *current amplification circuits* including a plurality of current mirrors combined (e.g., cascaded) *to achieve a target gain.*” JXM-0001 (’101 patent) at 11:42-45. Skilled artisans reading the ’101 patent would have understood that a “target gain” is “achieved” by multiplying an input current by a suitable gain factor—such as a gain of 1 or greater—to produce an output current. Wentzloff Decl. ¶¶ 58-60. This too is confirmed by the ’101 patent, which explains that the “target gain” can be “*any suitable gain*” and can have *any “suitable magnitude.”* See JXM-0001 (’101 patent) at 11:39, 10:62-66.⁵ Indeed, extrinsic evidence demonstrates that a skilled artisan would already have had this broad meaning in mind even before reading the ’101 specification. Explaining the “general properties” of “current mirrors,” for example, a textbook that Respondents cite—Paul R. Gray et al., “Analysis and Design of Analog Integrated Circuits” (5th Ed. 2009) (hereinafter, “Gray”)—explains this meaning succinctly:

⁵ Notably, the ’101 specification uses the terms “current mirror” and “current amplifier” interchangeably when explaining the claimed invention. For example, in the span of just three lines, the ’101 patent refers to item 83 shown in Figure 5 as both “current mirror 83” and current “amplifier 83.” JXM-0001 (’101 patent) at 10:62-65. And, of course, Figure 5 depicts these circuits as coextensive. *Id.* at Fig. 5.

Ideally, the output current is equal to the input current multiplied by a desired current gain. If the gain is unity, the input current is reflected to the output, leading to the name *current mirror*.

CXM-0001⁶ (Gray) at 251 (underling added, italics original). Thus, as Gray explains, the very name—“current mirror”—comes from these circuits’ ability to amplify an input current by multiplying that current by a unity gain factor (i.e., by “1”) to produce a “mirror” image current at their output. Unity amplification, Gray states, is the “ideal” of a “current mirror.”⁷ And as their respective proposed constructions demonstrate, Respondents and Staff apparently agree.

Skyworks’ proposed construction goes on to explain that a “current mirror” requires “having at least two transistors with their base or gate terminals tied together.” Although Respondents and Staff omit this explanation, for the reasons demonstrated below, the claim language, specification, prosecution history, and extrinsic evidence all confirm that the claimed “current mirror” requires “at least two transistors with their base or gate terminals tied together.”

1. Claim Language and Prosecution History

The term “current mirror” appears in each of independent claims 1, 17, and 21,⁸ and was added by amendment during prosecution to distinguish the ’101 patent’s claimed invention from a different Skyworks patent reference called Alon (JXM-0004 (’101 File History) at Skyworks_ITC_000023309-320). Application claim 18, for example, corresponds to issued claim 17. JXM-0004 (’101 File History), Index of Claims, at Skyworks_ITC_000053250. As

⁶ Respondents rely on Gray as RXM-0007.

⁷ That skilled artisans would have understood an ideal “current mirror” to amplify with unity gain is confirmed by Respondents’ exhibit RXM-0006, a book entitled “Current Sources & Voltage References,” by Linden T. Harrison, published in 2005, which states that a current mirror’s output can be a “1:1 match” to its input, achieving unity amplification. RXM-0006 at 15, 528. A current mirror can, of course, amplify with non-unity gain—i.e., a gain greater than or less than 1.

⁸ Issued claims 1, 17, and 21 correspond to application claims 1, 18, and 23, respectively. *See*, JXM-0004 (’101 File History), Index of Claims, at Skyworks_ITC_000053250.

originally drafted, application claim 18 recited: “[a] method of biasing a power amplifier, the method comprising ... amplifying the control current using a current amplifier to generate a correction current[.]” *Id.*, Application at Skyworks_ITC_000023157. This version of the claim was rejected during prosecution as “anticipated by Alon” in an Office Action dated August 2, 2013. *Id.*, Office Action at Skyworks_ITC_000023209. Comparing the elements of the claim to Alon’s Figure 2 (reproduced in relevant detail, with highlighting added, below), the Patent Examiner stated that Alon’s “device 204 [yellow] can be read as the claimed current amplifier” configured “to amplify the control current [207, blue] to generate a correction current (206 [green])”:

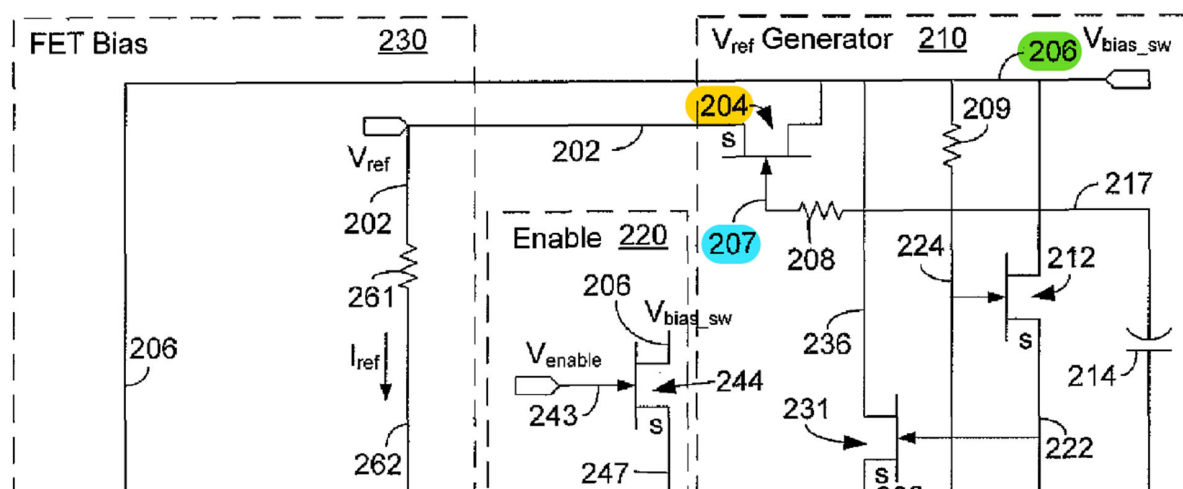


FIG. 2

Id. at Skyworks_ITC_000023210; *id.* at Alon (Skyworks_ITC_000023309-320), Fig. 2 (partial).

As shown above, Alon’s device 204 is a single field effect transistor (“FET”) that had its gate driven by the alleged “control current” 207, its source terminal 202 (also labeled “s”) connected to node “Vref” of FET Bias circuit 230, and its drain terminal 206 connected to the alleged “correction current,” which Alon identified as “Vbias_sw.” *Id.* at Alon (Skyworks_ITC_000023309-320), Fig. 2; *id.* at 5:48-53. Despite rejecting the independent claim, however, the

Examiner stated that dependent application claim 21—which was dependent from application claim 18—“would be allowable if rewritten in independent form[.]” *Id.*, Office Action at Skyworks_ITC_000023211. Application claim 21’s additional requirement over application claim 18 recited: “wherein amplifying the control current further includes amplifying the control current using a current mirror of the current amplifier.” *Id.*, Application at Skyworks_ITC_000023158. The Examiner thus recognized a distinction between a current amplifier comprised of a single field effect transistor, which the Examiner deemed unpatentable, versus use of a current mirror for a current amplifier, which the Examiner found to be patentably distinct from the prior art Alon reference. *Id.*, Office Action at Skyworks_ITC_000023211. Wentzloff Decl. ¶¶ 65-68.

Skyworks responded by amending what became issued claims 1, 17, and 21 to clarify that the current amplifier claimed in the ’101 patent was limited to a current mirror type of current amplifier. For example, Skyworks amended application claim 18 to recite “amplifying the control current using a current mirror of a current amplifier to generate a correction current[.]” JXM-0004 (’101 File History), Amendment at Skyworks_ITC_000023226 (underlining in original). In remarks accompanying this amendment, Skyworks explained that application claim 18 had “been amended to incorporate the limitations of original claim 21,” that “no new matter” had been added by this amendment, and that this amendment distinguished the invention claimed in the ’101 patent from Alon and its single transistor type of current amplifier, arguing for example that after this amendment application “claim 18 [was] not anticipated nor rendered obvious by the cited art.” *Id.* at Skyworks_ITC_000023229-230. The Patent Examiner agreed, allowing the ’101 patent claims (as amended) in a Notice of Allowability dated December 24, 2013. *Id.*, Notice of Allowability at Skyworks_ITC_000023242-245. Explaining his reasons for

allowance, the Examiner explained that the “prior art of record [e.g., Alon] considered individually or in combination, fails to fairly teach or suggest the claimed circuit comprising ... ‘...the current amplifier including a current mirror’ structurally and functionally interconnected with other limitations in the manner as cited in the claim.” *Id.*, Notice of Allowability at Skyworks_ITC_0000232344-345 (emphasis in original). Wentzloff Decl. ¶¶ 65-68.

By emphasizing that the ’101 patent claims, as granted, require a current mirror that is “structurally and functionally interconnected” in the manner the claims recite, the Examiner thus confirmed that the claimed “current mirror” requires at least two transistors as distinct from Alon’s single transistor structure. *Id.* Skyworks’ proposed construction—and its requirement of at least two transistors—is consistent with and required by this prosecution history. *See Phillips*, 415 F.3d at 1317 (“the prosecution history can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution”).

2. *Specification*

This requirement is further confirmed by the ’101 patent’s specification, which uniformly describes and depicts the claimed “current mirror” as comprising at least two transistors ***with their base or gate terminals tied together***. The patent states that the current amplification circuit can include “a plurality of current mirrors combined (e.g., cascaded) to achieve a target gain.” JXM-0001 (’101 patent) at 11:42-45. This is shown in Figure 5 (reproduced in relevant part below), which depicts a “current amplifier 83” as formed by two “current mirrors” (highlighted yellow and blue, respectively), each formed by a pair of transistors with their base terminals tied together:

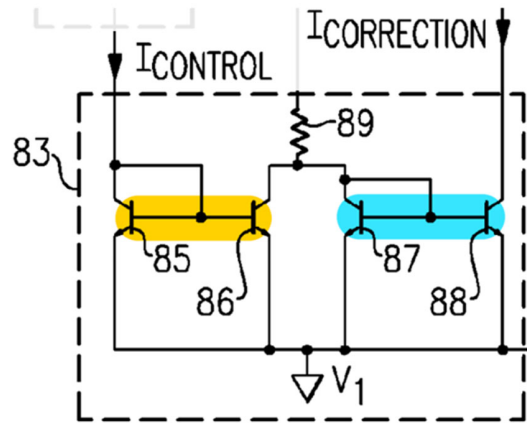
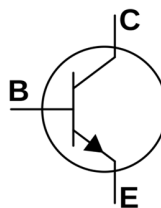


FIG.5

Id. at 10:62-11:27 and Fig. 5 (partial). The base terminal of a bipolar transistor is depicted in the figure below with the B notation.



Wentzloff Decl. ¶¶ 26, 62. Thus, in Figure 5 above, the bases of bipolar transistors 85 and 86 are connected by the trace highlighted in yellow, and the bases of bipolar transistors 87 and 88 are connected by the trace highlighted in blue. *Id.*

As the '101 patent's Summary of the Invention explains, a first "current mirror" (e.g., highlighted yellow in Figure 5 above) is formed from "a first bipolar transistor and a second bipolar transistor" having a signal line "electrically connected to a base of the first bipolar transistor and to a base of the second bipolar transistor[.]" JXM-0001 ('101 patent) at 1:65-2:7; *see also id.* at 11:10-15 ("The first NPN bipolar transistor 85 includes ... a base and a collector electrically connected to a base of the second NPN bipolar transistor 86"). Similarly, the second "current mirror" (e.g., highlighted blue) is formed from "a third bipolar transistor" and "a fourth bipolar transistor" where "a base of the third bipolar transistor" is electrically connected "to a

base of the fourth bipolar transistor[.]” *Id.* at col. 2:7-15; *see also* col. 11:16-21 (describing “a base and a collector of the third NPN bipolar transistor 87” as “electrically connected ... to a base of the fourth NPN bipolar transistor 88”). A skilled artisan reading the ’101 specification would thus conclude that the claimed current mirror has “at least two transistors with their base or gate terminals tied together.”⁹ Wentzloff Decl. ¶¶ 63-64.

3. *Extrinsic Evidence*

This conclusion is further confirmed by extrinsic evidence. Whether instantiated using bipolar transistors or MOS transistors, a key feature of a “current mirror” is that it has at least two transistors with their base terminals (for bipolar transistors) or gate terminals (MOS transistors) tied together. Staff’s exhibit SMX-0001, Steven M. Kaplan, “Electrical and Electronics Engineering Dictionary” (2004) (hereinafter, “Kaplan”), for example, defines a “current mirror” as “[a] circuit in which the current on one side is forced to be a replica of that of the other side” which is “[a]ccomplished, for instance, *by the bases and emitters of two bipolar junction transistors being connected together.*” SMX-0001 (Kaplan) at 159. This exhibit uses the phrase “for instance” because its example is for bipolar transistors, which have their base terminals connected together; for MOS transistors, which have gate terminals instead of base terminals, the gate terminals of the two MOS transistors are tied together. Wentzloff Decl. ¶¶ 69-70.

The Gray textbook, upon which Respondents also rely, similarly describes a “current mirror” as at least “two transistors” having their bases (bipolar) or gates (MOS) tied together.

⁹ As explained in the “Extrinsic Evidence” section below, a bipolar transistor has a base terminal, and a MOS transistor (another common type of transistor) instead has a gate terminal. Accordingly, a current mirror with bipolar transistors has the base terminals of its transistors connected together, and a current mirror with MOS transistors instead has the gate terminals of its transistors tied together. Wentzloff Decl. ¶¶ 26-27, 35, 41.

Gray explains, for example, that “a bipolar version of this mirror” is shown in its “simplest form” in “Fig. 4.2” as “two transistors” “ Q_1 ” and “ Q_2 ” having their base terminals tied together (shown with yellow highlighting below):

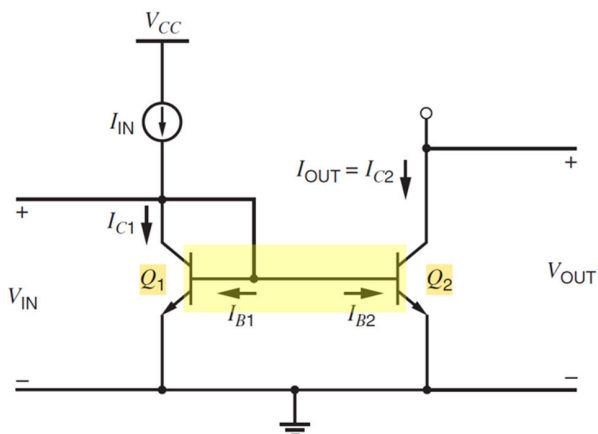


Figure 4.2 A simple bipolar current mirror.

CXM-0001 (Gray) at 253. The Gray textbook likewise defines “an MOS version of the simple current mirror” in “Figure 4.4” as transistors “ M_1 ” and “ M_2 ” having their gates tied together (shown with yellow highlighting below):

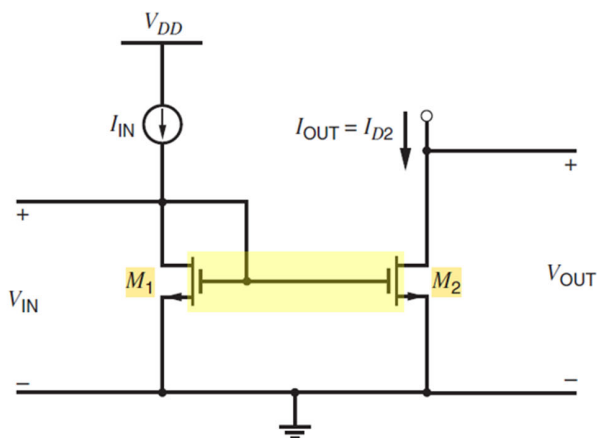
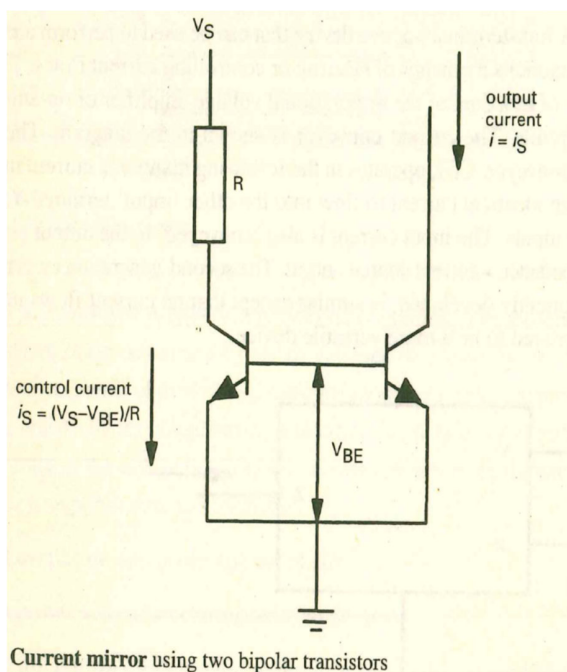


Figure 4.4 A simple MOS current mirror.

Id. at 255-56. In each case, whether bipolar or MOS, the key attribute of a “current mirror” is that it has at least two transistors with their base (bipolar) or gate (MOS) terminals tied together. *See also id.* at 827 and Fig. 12.26 (“We choose M_{25} to be matched to M_5 , so they form a unity-gain current mirror.”). Wentzloff Decl. ¶¶ 35, 41, 71.

Even Respondents' extrinsic evidence defines a current mirror as including two transistors whose bases are connected together. For example, Respondents' exhibit RXM-0002, "The Dictionary of Electronics," (3rd Edition 1998), shows the current mirror depicted below.



RXM-0002 (hereinafter, "Dictionary of Electronics") at 110. This dictionary goes on to (1) describe the "current mirror" as a circuit that forces the "current in one side of the circuit" to be "identical to the current in the other side of the circuit" (i.e., unity gain in this example), (2) state that the "simplest current mirror comprises just two transistors" (not one as Skyworks expects Respondents to suggest), and (3) state that "the bases ... of the two transistors [in the current mirror] are connected together." *Id.* Thus, Respondents' own extrinsic evidence establishes that the key attributes of a current mirror include the ability to have unity gain and having at least two transistors with their base or gate terminals connected together. Wentzloff Decl. ¶ 72.

4. Respondents' Expected Argument Is Mistaken

Respondents appear to rely on RXM-0005 (Toumazou), as they do in their invalidity contentions, to argue that the claimed current mirror can be a single transistor. RXM-0005

(Toumazou) at 242-243.¹⁰ Respondents’ argument is, however, squarely at odds with the ’101 patent’s prosecution history. As shown above, the original independent application claims did not recite a “current mirror,” and the Examiner rejected these claims based on Alon’s disclosure of a single transistor that he described as receiving the claimed “control current” and outputting the claimed “correction current.” JXM-0004 (’101 File History), Application at Skyworks_ITC_000023155-158; *id.*, Office Action at Skyworks_ITC_000023209; *id.* at Alon (Skyworks_ITC_000023309-320). At the same time, the Examiner indicated that the dependent claims reciting a “current mirror” **would be allowable** over Alon’s single transistor structure if rewritten in independent form—which applicants then did. *Id.*, Office Action at Skyworks_ITC_000023211. The Examiner then allowed the claims finding that Alon’s single transistor structure “fails to fairly teach or suggest the claimed circuit” comprising, “‘the current amplifier including a current mirror’ structurally and functionally interconnected with other limitations in the manner as cited in the claim.” *Id.*, Notice of Allowability at Skyworks_ITC_000023242-245 (emphasis in original). This history demonstrates that a single transistor—even one alleged to have the exact same “control current” input and “correction current” output as the claims recite—is **not** within the scope of these claims because that is what the Examiner found the ’101 claims’ “current mirror” language to distinguish with respect to Alon. Respondents expected attempts to recapture such a single transistor structure through claim construction are misplaced. *Spectrum Int’l, Inc. v. Sterilite Corp.*, 164 F.3d 1372, 1378-79

¹⁰ That a person of ordinary skill in the art would not consider such a single transistor a current mirror is highlighted by RXM-0005 (Toumazou) itself, where it states that there is a “practical objection to this proposal” of calling a single transistor a mirror. *Id.* at 242; Wentzloff Decl. ¶¶ 74-75.

(Fed. Cir. 1988) (“Indeed by distinguishing the claimed invention over the prior art, an applicant is indicating what the claims do not cover.”) (cleaned up).

Moreover, when Respondents’ misguided attempts to ignore the prosecution history are set aside, Toumazou (RXM-0005) actually supports *Skyworks*’ proposed construction. For example, Toumazou defines a “classical [] current mirror” as having at least two transistors (Q1 and Q2) with their base terminals tied together (shown with yellow highlighting below), just like Skyworks’ proposed construction.

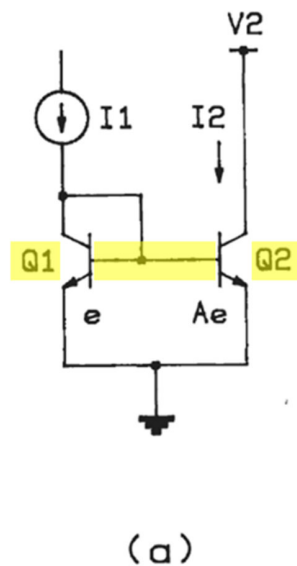


**Figure 6.7 The classical NPN current mirror (a),
emitter degeneration (b).**

RXM-0005 (Toumazou) at 251, Fig. 6.7(a). Toumazou, in fact, emphasizes that the “basic NPN *current mirror (Figure 6.7a) is the simple theme* from which endless variations and transformations can be spun[.]” *Id.* at 251 (emphasis added). Wentzloff Decl. ¶ 76. Skyworks’ construction is based on and consistent with this “simple theme” for a current mirror.

For these reasons, the term “current mirror” in the ’101 patent means “one or more circuits configured to mirror a current, which can be configured to achieve a target gain, having at least two transistors with their base or gate terminals tied together.”

B. “amplifying the control current using a current mirror of a current amplifier to generate a correction current” (’101 patent claims 17, 18, 20)

Complainants	Respondents	Staff
Plain meaning, which is “achieving a target gain of a control current, using a current mirror of a current amplifier, to generate a correction current”	Plain meaning, such as “increasing the control current using a current mirror of a current amplifier to generate a correction current	Plain meaning, such as “increasing the control current using a current mirror of a current amplifier to generate a correction current”

The dispute with respect to this term centers on whether the claimed amplifier must “achieve[] a target gain of a control current” as Skyworks contend, or is instead limited solely to amplifiers that “increase the control current” as Respondents and Staff argue. The claim language, specification, prosecution history, and extrinsic evidence all confirm that the claimed “current amplifier” amplifies by “achieving a target gain.”

1. Claim Language and Prosecution History

The claim language itself requires the use of “a current mirror of a current amplifier” for this claim step. In other words, the “current amplifier” that performs the act of “amplifying the control current ... to generate a correction current” must be a “current mirror of a current amplifier.” JXM-0001 (’101 patent) at claim 17. And it is undisputed among the private parties and Staff that a “current mirror” “can be configured to achieve a target gain,” and thus need not “increase the control current.” *See* Joint Claim Construction Chart (for “current mirror”).

The use of current mirrors with unity gain is common in the art, confirming that a current amplifier using a current mirror need not increase the input (i.e., need not have a gain greater than 1). Wentzloff Decl. ¶¶ 78-79. For example, Respondents’ RXM-0002 describes a “current mirror” as a circuit that forces the “current in one side of the circuit” to be “*identical* to the current in the other side of the circuit” (i.e., unity gain). RXM-0002 (Dictionary of Electronics) at 110. The Gray textbook refers to a unity gain current mirror in stating that “[i]f the gain is

unity, the input current is reflected to the output, leading to the name **current mirror**.” CXM-0001 (Gray) at 251 (underling added, italics original); *see also id.* at 253 (“If the transistors are identical, $I_{S1} = I_{S2}$ and (4.2) shows that the current flowing in the collector of Q_1 is mirrored at the collector of Q_2 ,” meaning that this current mirror has unity gain); *id.* at 827 (emphasis added) (“We choose M_{25} to be matched to M_5 , so they form a **unity-gain current mirror**.”); SMX-0001 (Kaplan) (emphasis added) (defining a “current mirror” as a “circuit in which the current on one side is forced to be a **replica** of that of the other side....”). Wentzloff Decl. ¶ 60.

The ’101 patent’s prosecution history confirms that the claimed “current amplifier” is not merely any type of “current amplifier,” but is instead a current mirror type of current amplifier (which can achieve any target gain and not necessarily increase its input). As explained above in connection with the term “current mirror,” in response to a rejection by the Patent Examiner for application claim 18 (granted claim 17), which required a “current amplifier” but not a “current mirror,” Skyworks amended application claim 18 to require a “current mirror.” In particular, Skyworks amended what became issued claims 1, 17, and 21 to clarify that the current amplifier claimed in the ’101 patent claims was limited to a “current mirror” for the current amplifier. Application claim 18 (issued claim 17), for example, was amended to recite “amplifying the control current using a current mirror of a current amplifier to generate a correction current”—adding the underlined language which had previously been in original claim 21. JXM-0004 (’101 File History), Amendment at Skyworks_ITC_000023226 (underlining in original). Skyworks also argued that the cited prior art did not disclose this current mirror for the current amplifier. *Id.* at Skyworks_ITC_000023230. In allowing the application claim 18, the Examiner explained that the “prior art of record considered individually or in combination, fails to fairly teach or suggest the claimed method comprising ... ‘amplifying the control current using a

current mirror of a current amplifier to generate a correction current’ structurally and functionally interconnected with other limitations in the manner as cited in the claim.” *Id.*, Notice of Allowability at Skyworks_ITC_000023244-45 (emphasis in original).¹¹ By emphasizing that the ’101 patent claims, as granted, require a current mirror, the Examiner thus confirmed that the claimed “current amplifier” is a “current mirror” type of amplifier. This prosecution history further confirms that the claimed “amplifying the control current using a current mirror of a current amplifier ...” does not require increasing the control current to generate the correction current, but instead need only achieve a target gain to amplify the control current (as for a “current mirror”). Wentzloff Decl. ¶ 79.

2. *Specification*

That the claimed act of “amplifying using a current mirror of a current amplifier ...” achieves a “target gain” is confirmed throughout the ’101 specification. The ’101 patent confirms that its current “amplifier” can have a gain of *any* “*suitable magnitude*.” JXM-0001 (’101 patent) at 10:62-66.¹² In addition, at column 11, the ’101 patent states unequivocally that “[a]s used herein, the term *current mirror* can refer to *current amplification circuits* including a plurality of current mirrors combined (e.g., cascaded) *to achieve a target gain*.” *Id.* at 11:42-45; *see also id.* at 11:39 (confirming that the “target gain” of the current mirror can be “any suitable gain”). Wentzloff Decl. ¶ 80.

¹¹ The Examiner made a similar statement with respect to claim 1 and the rest of the allowed claims. JXM-0004 (’101 File History), Notice of Allowability at Skyworks_ITC_000023244-46.

¹² As noted in connection with the “current mirror” term above, the ’101 specification uses the terms “current mirror” and “current amplifier” interchangeably when explaining the claimed invention. For example, in the span of just three lines, the ’101 patent refers to item 83 shown in Figure 5 as both “current mirror 83” and current “amplifier 83.” JXM-0001 (’101 patent) at 10:62-65. And, of course, Figure 5 depicts these circuits as coextensive. *Id.* at Fig. 5.

Because the claimed “current amplifier” is implemented as a “current mirror”—according to the express claim language—and because it is undisputed that a “current mirror” can achieve a “target gain” that can be unity, the claimed “current amplifier” can also achieve a target gain such as unity. In other words, the claimed current amplifier need not “increase” the control current to generate a correction current as Respondents and Staff contend, but instead can be configured to achieve any target gain. And it is common in the art to achieve a target gain of unity for a current mirror (*see* “current mirror” section above), as well as for a current amplifier (*see* Extrinsic Evidence section below).

Conversely, Respondents’ and Staff’s construction—which would limit the claims solely to an “increasing” type amplifier—would exclude embodiments squarely within the ’101 patent’s “*any* suitable gain” / *any* “suitable magnitude” disclosures, an outcome that the Federal Circuit holds is “rarely, if ever, correct.” *Vitronics*, 90 F.3d at 1583 (a construction that excludes a disclosed embodiment “is rarely, if ever, correct”); *see also CCS Technology, Inc. v. Panduit Corp.*, 778 Fed. Appx. 947, 950 (Fed. Cir. 2019) (“an interpretation which excludes a disclosed embodiment from the scope of the claim is rarely, if ever, correct” (cleaned up)); *Oatey*, 514 F.3d at 1276-77 (absent lexicography or disclaimer, we “do not interpret claim terms in a way that excludes embodiments disclosed in the specification”); *Medrad, Inc. v. MRI Devices Corp.*, 401 F.3d 1313, 1320 (Fed. Cir. 2005) (“A claim construction that does not encompass a disclosed embodiment is rarely, if ever, correct.” (cleaned up)).

3. *Extrinsic Evidence*

The extrinsic evidence further confirms that in connection with amplifiers, as for current mirrors, it is also common to amplify with unity gain. Wentzloff Decl. ¶ 81. For example, “Control of Three Phase Power Supplies for Ultra Low THD,” by Doncker et al., APEC ’91 Sixth Annual Applied Power Electronics Conference and Exhibition (1991) (“Doncker”)

confirms that to skilled artisans it is common to “amplify with unity gain.” CXM-0005 (Doncker) at 624. Further, “Microelectronic Circuit Design,” Jager, 4th Edition, McGraw-Hill (2010) (“Microelectronics Design”), shows and describes current amplifiers that have a gain of one (i.e., unity gain). CXM-0002 (Microelectronics Design) at 898-99 (“the common-base current *gain is simply α_o* . For the FET, α_o is *exactly 1*...”), Fig. 14.24, 14.25. Indeed, numerous extrinsic references describe amplifiers with unity gain. CXM-0001 (Gray) (emphasis added) at 284-85, 634 (“Compensation for *unity-gain* feedback operation ($f = 1$) [of a basic amplifier] is achieved ...”); *id.* at 635 (emphasis added) (“... the basic *amplifier has a unity-gain* bandwidth ...”); CXM-0003 (“Art of Electronics”) (emphasis added) at 318 (referring to “*unity gain* current amplifiers”); CXM-0004 (“Microelectronics Journal paper”) at 1086-87 (“*unity-gain current amplifier*” and “current operation amplifier (COA)” in “*unity-gain* closed loop configuration”). Wentzloff Decl. ¶ 82.

The consistent description in extrinsic evidence of “current amplifiers” and amplifying with unity gain confirms to a skilled artisan that to “amplify” with a “current mirror of a current amplifier” does not require increasing the input to generate the output, but instead includes achieving any target gain, including a gain of unity. Wentzloff Decl. ¶ 83.

Unity gain current amplifiers are commonly used in the art to prevent a circuit downstream from the current amplifier from affecting the input undesirably, thus isolating the input from the output. Wentzloff Decl. ¶ 84. This enables the output current from the amplifier to operate independent of the load connected to the output of the amplifier (i.e., the circuit connected to the output of the amplifier). *Id.* A unity gain current amplifier thus keeps the output current at the same level as the input current, while achieving this isolation feature. This

desirable characteristic of a unity gain current amplifier makes it a common circuit element in electronics. *Id.*

4. Respondents' Expected Argument Is Mistaken

Respondents and Staff improperly limit this claim term to “increasing” the control current to generate the correction current. In doing so, Respondents and Staff appear to rely on extrinsic evidence that suggests that “amplifying” means “increasing” and an amplifier “increases” the input current or voltage. RXM-0001 at 12-13; RXM-0009 (referring to “amplify” as “producing ... more power”); SMX-0001 (Kaplan) at 23, 158. An amplifier can, of course, increase an input to generate an output, but it need not do so. Respondents and Staff attempt to limit the claim to a particular type of amplifying using a current mirror type current amplifier—increasing the gain—even though this excludes well-known current amplifiers and current mirrors, and even though it is inconsistent with the ’101 patent specification’s description of achieving a target gain with a current mirror type of current amplifier. Such an attempt to exclude known types of amplifying with amplifiers is improper. *Wasica Fin. GmbH v. Cont’l Auto. Sys., Inc.*, 853 F.3d 1272, 1281 (Fed. Cir. 2017) (“If the intrinsic record supports several definitions of a term, the term may be construed to encompass all such consistent meanings.”). To be clear, it is common to amplify by increasing an input to generate an output and to use amplifiers to increase an input to generate an output, but it is also common to use amplifiers that amplify with unity gain. Wentzloff Decl. ¶¶ 82-84.

For these reasons, the term “amplifying the control current using a current mirror of a current amplifier to generate a correction current” in the ’101 patent means “achieving a target gain of a control current, using a current mirror of a current amplifier, to generate a correction current.”

C. “a current amplifier configured to amplify the control current to generate a correction current” (’101 patent claims 1, 2, 10, 11, 21, 22)

Complainants	Respondents	Staff
Plain meaning, which is “a current amplifier configured to achieve a target gain of a control current to generate a correction current”	Plain meaning, such as “a current amplifier configured to increase the control current to generate a correction current”	Plain meaning, such as “a current amplifier configured to increase the control current to generate a correction current”

The dispute with respect to this term is essentially the same as for the previous term—whether the claimed “current amplifier configured to amplify the control current ...” must be configured to “achieve a target gain of a control current” as Skyworks contends, or is instead limited solely to current amplifiers that “increase the control current” as Respondents and Staff argue. For the same reasons as set forth for the previous term, the claim language, prosecution history, specification, and extrinsic evidence all confirm that the claimed “current amplifier” amplifies by “achieving a target gain” and that the “current amplifier” need not “increase” the control current to generate the correction current as Respondents and Staff contend.

D. “integrated circuit” (’563 patent claims 14, 15, 17, 20)

Complainants	Respondents	Staff
Plain meaning, which is “a circuit made up of multiple interconnected electronic components integrated on one or more dies”	Plain meaning, which is “a circuit made up of multiple interconnected electronic components integrated on a die”	Plain meaning, such as “a circuit made up of multiple interconnected electronic components integrated on one or more dies”

The dispute with respect to this term centers on whether the claimed “integrated circuit” can be “integrated on one or more dies” as Staff and Skyworks contend, or is instead limited solely to the types of integrated circuits that are “integrated on a [single] die” as Respondents argue. The specification and extrinsic evidence confirm that the claimed “integrated circuit” can be “integrated on one or more dies.” Wentzloff Decl. ¶ 86.

1. Intrinsic Evidence

The '563 specification confirms that an “integrated circuit” (“IC”) can be made from “one or more dies” and need not be limited to a single die as Respondents contend. For example, the specification explains that the “packaged power amplifier module 300 includes an *IC or die* 301.” JXM-0002 ('563 patent) at 14:15-16. The specification further explains that the claimed amplifier module can be implemented in “dies” (plural). *Id.* at 14:66-15:2 (module “formed over the packaging substrate 320 and the components and *die(s)* disposed thereon.”). By explaining that the invention can be implemented in either an “IC” *or* in a “die,” and by explaining that the invention can be implemented on “dies,” the specification confirms that the “integrated circuit” can be made from “one or more dies” and should not be limited to a single die. Wentzloff Decl. ¶¶ 87-88. Conversely, Respondents’ proposed construction, which would exclude the disclosed “dies” (plural) embodiment from the scope of the '563 patent claims, should be rejected. *Oatey*, 514 F.3d at 1276-77 (“We ... do not interpret claim terms in a way that excludes embodiments disclosed in the specification”); *see also CCS Technology*, 778 Fed. Appx. at 950 (same); *Medrad*, 401 F.3d at 1320 (same); *Vitronics*, 90 F.3d at 1583 (same).

One embodiment in the '563 specification describes integrating the power amplifier and its bias block on a single die. *Id.* at 9:26-31 (emphasis added) (“The power amplifier bias block 50 and the power amplifier 32 *can be* integrated on a single die with one or more other components to form a packaged power amplifier module, which can be, for example, mounted to a RF circuit board associated with the wireless device 11 of FIG. 2.”); *id.* at 11:25-30 (“the power amplifier bias block 80 *can be* integrated on-chip with a power amplifier”). In so doing, the specification makes clear that the components “can be” integrated on a single die or chip, not that they *must be* integrated on a single die. Limiting the claimed invention beyond its ordinary meaning to an example embodiment, as Respondents seek to do here, is incorrect. *See, e.g., Innova/Pure Water*

381 F.3d at 1117 (“[P]articular embodiments appearing in the written description will not be used to limit claim language that has broader effect.”); *Aventis Pharma S.A. v. Hospira, Inc.*, 675 F.3d 1324, 1330 (Fed. Cir. 2012) (“It is ... not enough that the only embodiments, or all of the embodiments, contain a particular limitation to limit a claim term beyond its ordinary meaning.”) (internal citations omitted); *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) (“[T]his court has expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment.”). This is especially so given that the specification explains that the claimed amplifier module can be implemented in “dies” (plural). *Id.* at 14:66-15:2.

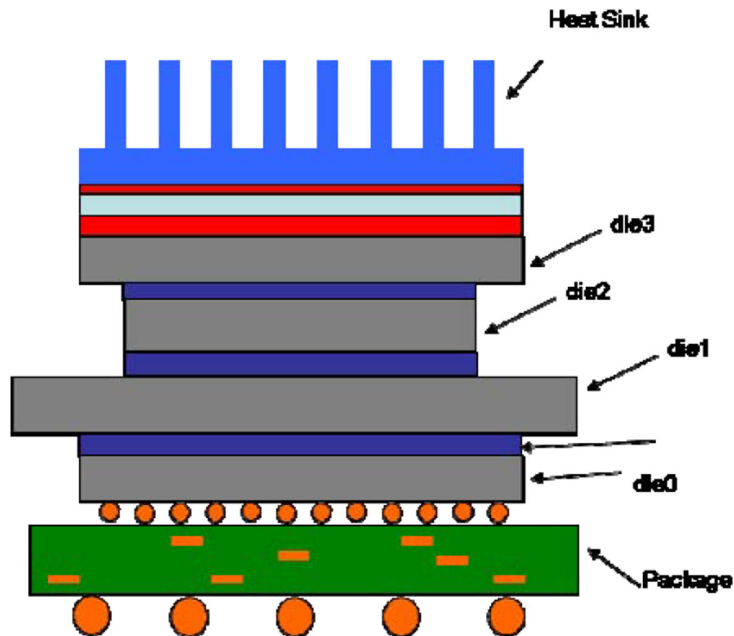
2. *Extrinsic Evidence*

This conclusion that an “integrated circuit” can be “integrated on one or more dies” is further confirmed by extrinsic evidence. The textbook “Integrated Circuit Design, Fabrication and Test,” by P. Shephard, McGraw-Hill (1996) (“Shephard”) describes numerous well-known integrated circuit types. For example, Shephard describes one type of integrated circuit as a “monolithic IC, where ... all the components and interconnections are on the semiconductor substrate.” CXM-0009 (Shephard) at 1. Respondents proposed construction apparently seeks to limit the claims solely to this “monolithic” type IC. But another type of integrated circuit is a “multichip integrated circuit,” which can include two or more semiconductor chips. Wentzloff Decl. ¶¶ 89-91; CXM-0007 (IEEE Dictionary) at 712. Given that there exists neither lexicography nor disclaimer anywhere in the ’579 patent limiting the claims to just one type of integrated circuit—and quite to the contrary, the specification teaches that both of these types could be used—limiting the claims as Respondents’ propose would be legal error. *Liebel-Flarsheim*, 358 F.3d at 906 (“[T]he claims of the patent will not be read restrictively unless the

patentee has demonstrated a clear intention to limit the claim scope using ‘words or expressions of manifest exclusion or restriction.’”).

The broad understanding of integrated circuit as encompassing “one or more dies” is further confirmed by the “Authoritative Dictionary of IEEE Standards Terms,” Seventh Edition (2006) (“IEEE Dictionary”), which explains that a “monolithic integrated circuit” is a circuit formed on a “single piece” of substrate whereas a “multichip integrated circuit” has its circuit elements formed “on or within two or more semiconductor chips.” CXM-0007 (IEEE Dictionary) at 708 (“**monolithic integrated circuit** An integrated circuit formed in a single piece of the substrate material.”) (bolding in original, underlining added); *id.* at 712 (“**multichip integrated circuit** An integrated circuit whose elements are formed on or within two or more semiconductor chips that are separately attached to a substrate.”) (bolding in original, underlining added). Wentzloff Decl. ¶ 91.

The extrinsic evidence confirms that another type of “integrated circuit” with more than one die is a “three-dimensional integrated circuit,” also called a “3D IC.” Wentzloff Decl. ¶ 92. For example, “Thermal Characteristics of Multi-Die, Three-Dimensional Integrated Circuits with Unequally Sized Die,” by Jain, published in 2010 in an IEEE journal (“Jain IEEE paper”), describes three-dimensional integrated circuits. CXM-0008 (Jain IEEE paper), at 1-2. An example of a three-dimensional integrated circuit from the Jain IEEE paper is shown below.



Id. at 2, Fig. 1. In describing this figure, this IEEE paper states that “Figure 1 schematically shows a multi-die **3D IC**, with **four** unequally sized **die**.” *Id.* This IEEE paper also refers numerous times to “three-dimensional integrated circuits,” or “3D ICs.” *Id.* at 1-2. In the “integrated circuit” shown in the figure above, four dies—die 0, die1, die2, and die 3—are included within the integrated circuit. Wentzloff Decl. ¶¶ 92-93.

Excluding well-known types of “integrated circuits” from the claim scope through claim construction—in particular, a “multichip integrated circuit” having two or more semiconductor chips” and a “three-dimensional integrated circuit”—would be improper. *3M Innovative Props. Co. v. Tredegar Corp.*, 725 F.3d 1315, 1333 (Fed. Cir. 2013) (“It is axiomatic that we will not narrow a claim term beyond its plain and ordinary meaning unless there is support for the limitation in the words of the claim, the specification, or the prosecution history.”); *Wasica*, 853 F.3d at 1281 (“If the intrinsic record supports several definitions of a term, the term may be construed to encompass all such consistent meanings.”). *Intell. Ventures Mgmt., LLC v. Xilinx, Inc.*, IPR2012-00020, Paper No. 34 at 8-9 (P.T.A.B. Feb. 11, 2014) (“It is uncontested that a

person of ordinary skill in the art knew that circuits could be arranged on a die and that an IC [*i.e.*, integrated circuit] could contain more than one die. Multi-die IC were well known in the art at the time of the invention.”).

3. Respondents’ Expected Argument Is Mistaken

In attempting to limit an “integrated circuit” to a single die, Respondents appears to rely on extrinsic evidence that suggests that an “integrated circuit” must be on a single piece of semiconductor. RXM-0001 at 169; RXM-0003 at 356; RXM-0009 at 213. It is, of course, possible and common to implement an integrated circuit on a single die, but it is also possible and common to use “multichip integrated circuits” or “three-dimensional integrated circuits” that include multiple dies as part of the “integrated circuit.” Wentzloff Decl. ¶¶ 94-95. As noted above, excluding well-known types of integrated circuits from the scope of the claim would be improper. *3M Innovative*, 725 F.3d at 1333; *Wasica*, 853 F.3d at 1281.

For these reasons, the term “integrated circuit” in the ’563 patent means “a circuit made up of multiple interconnected electronic components integrated on one or more dies.”

VI. RESPONDENTS’ INDEFINITENESS ARGUMENTS

Patent claims must particularly point out and distinctly claim the subject matter of the invention. 35 U.S.C. § 112. Accordingly, a claim is invalid as indefinite if, when “read in light of the specification delineating the patent, and the prosecution history, [the claim] fail[s] to inform, with reasonable certainty, those skilled in the art about the scope of the invention.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). If the claims read in light of the specification reasonably apprise a person of ordinary skill in the art of the scope of the invention, the claim is not indefinite. *Amgen Inc. v. F. Hoffman-La Roche Ltd.*, 580 F.3d 1340, 1371 (Fed. Cir. 2009).

A. “inhibiting” (’579 patent claim 7)

Complainants	Respondents	Staff
Plain meaning, which is “suppressing or reducing”	Indefinite	Plain meaning, which is “suppressing or reducing”
This term is not indefinite		This term is not indefinite

Staff and Skyworks agree that “inhibiting” a “low-frequency blocker signal” from mixing with “a fundamental frequency signal” in the RF switch requires simply “suppressing or reducing” the mixing of these two signals, and that this term is not indefinite. Respondents, by contrast, argue that “inhibiting” in the context of this ’579 patent claim is so lacking in meaning that a skilled artisan would have had no ability to understand what the claim was talking about with reasonable certainty.

As an initial matter, Respondent KCT is taking a fundamentally inconsistent position on this term in this Investigation from the position that it is simultaneously advancing to the PTAB in an IPR petition that it filed on November 12, 2024. In this Investigation, Respondents say that a skilled artisan would have no ability to reasonably understand what the claimed “inhibiting” is—despite express claim language explaining the purpose to inhibit “low-frequency” and “fundamental frequency” signals “from mixing” in the claimed “RF switch,” and extensive explanation of this purpose in the specification. But before the PTAB, KCT understood the meaning of “inhibiting” in attempting to apply the term to the asserted prior art. *See* CXM-0010 (’579 IPR Petition) at 50. Although KCT’s IPR Petition is mistaken as to the scope and content of the prior art (as well as numerous other issues including motivation to combine and reasonable expectation of success), KCT’s admission that skilled artisans would have understood what claim 7 means by “inhibiting” these signals “from mixing”—particularly in light of the plain language of claim 7 and clear teaching of the ’579 patent—condemns Respondents’ indefiniteness argument here. *Key Pharms. V. Hercon Lab’ys Corp.*, 161 F.3d 709, 714-15 (Fed.

Cir. 1998) (“We find highly questionable Hercon’s assertion on appeal that the trial court erred when it adopted the very construction Hercon urged upon the court ... we look with extreme disfavor on Hercon’s assertion.”); *N. Telecom Ltd. v. Samsung Elecs. Co.*, 215 F.3d 1281, 1290 (Fed. Cir. 2000) (“[W]e look with ‘extreme disfavor’ on appeals that allege error in claim constructions that were advocated below by the very party now challenging them.”).

As importantly, for the reasons demonstrated below, the claims, specification, and prosecution history allow those of ordinary skill in the art to ascertain with reasonable certainty the scope of the claim. *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1371 (Fed. Cir. 2014). Accordingly, Respondents have failed to prove indefiniteness by clear and convincing evidence, and Staff’s and Skyworks’ construction should be adopted.

1. Claim Language and Specification

The term “inhibiting” appears in claim 7 of the ’579 patent, which recites, in part:

inhibiting a low-frequency blocker signal from mixing with a fundamental-frequency signal in the RF switch using the first capacitor.

JXM-0003 (’579 patent) at 13:29-48 (claim 7) (emphasis added). This claim language clearly describes use of a “first capacitor” to “inhibit” “low-frequency” and “fundamental frequency” signals “from mixing” in the claimed “RF switch.” A skilled artisan reading this plain language would thus understand “inhibiting” to mean “suppressing or reducing” the mixing of these two recited signals. *See* Kinget Decl. at ¶¶ 51-53.

This meaning is further confirmed by the teaching of the ’579 patent’s specification. For example, the ’579 patent explains that “with the foregoing capacitors, a low-frequency jammer signal can be ***blocked or reduced*** from mixing with any [fundamental-frequency] signals.” JXM-0003 (’579 patent) at 9:49-53 (emphasis added); *see also id.* at Abstract (emphasis added) (“Radio-frequency (RF) devices are disclosed providing ***reduced*** intermodulation distortion”),

id. at 6:42-43 (emphasis added) (“it can be desirable to **reduce** susceptibility to interference within an RF system”), *id.* at 9:16-18 (emphasis added) (“systems can benefit significantly from RF switches having **reduced** IMDs.”). Because the specification contemplates both “blocking” (i.e., fully suppressing) and “reducing” (i.e., partially suppressing) as within the scope of the claimed “inhibiting,” a skilled artisan would understand the full scope of claim 7 to cover both. *See* Kinget Decl. at ¶¶ 53-55. Thus, consistent with this clear intrinsic evidence, Staff’s and Skyworks’ proposed construction of “inhibiting” encompasses both “suppressing or reducing.” *Id.*

Moreover, the ’579 patent’s specification teaches a “capacitor configured to **inhibit** a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.” JXM-0003 (’579 patent) at Abstract; *id.* at 1:37-40 (“[t]he system further includes a capacitor connected in series with the switch and configured to **inhibit** a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.”) (emphasis added); *see also id.* at 1:55-57, 2:2-4, 2:15-17, 2:36-38, 3:7-10, 9:39-41. Notably, the patent then proceeds to state that “[i]n **some** implementations, ... this technique can provide improved ... performance by **preventing** a low-frequency blocker signal from mixing with a fundamental frequency signal.” *Id.* at 9:67-10:3 (emphasis added). A skilled artisan reading this explanation, and particularly the patent’s statement that only in “**some** implementations” is the low-frequency signal fully “prevent[ed]” from mixing with the fundamental frequency signal, would thus understand that the patent also covers other implementations where such mixing is merely “reduced.” *See* Kinget Decl. at ¶ 55; *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1328 (Fed. Cir. 2002) (cautioning against “limiting the claimed invention to preferred embodiments” or specific examples in the specification); *see also Lowe v. ShieldMark, Inc.*, No. 2021-2164, 2022 WL

636100, at *5 (Fed. Cir. Mar. 4, 2022) (holding that the claimed invention is not limited to “tape with shoulders” because “tape with shoulders ... is just ‘*one embodiment*’ of the claimed invention and the structure explains that “[*o*]ther structures ... may also be used in place of ... shoulders”) (emphasis in original).

2. Prosecution History

As noted above, Respondent KCT, in its IPR Petition for the ’579 patent, understood the meaning of the term “inhibiting” and applied it to the asserted prior art with no apparent uncertainty. In its IPR Petition, for example, KCT states unequivocally that skilled artisans “*understood* this capacitor’s *inhibition* of low-frequency blocker signals from mixing with fundamental frequency signals ... to merely be a matter of design choice.” CXM-0010 (’579 IPR Petition) at 51. In this same Petition, KCT and its expert also purport to explain how the prior art supposedly meets this “inhibiting” claim language without professing confusion over what “inhibiting” means. *Id.* at 48-51. KCT’s attempt to now contend that the term “inhibiting” renders claim 7 invalid as indefinite is inconsistent with the positions it took before the PTAB, and should be rejected.

3. Extrinsic Evidence

Extrinsic evidence further confirms that the term “inhibiting” has definite meaning in the context of claim 7 and the patent’s teaching. For example, Dr. Kinget—a Professor of Electrical Engineering at Columbia University with over 25 years of experience in RF electronics—confirms that skilled artisans would understand the meaning of “inhibiting” in the context of claim 7 to be “reducing or suppressing.” Kinget Decl. ¶¶ 51-57.

4. Respondents’ Expected Argument Is Mistaken

Respondents appear to rely on extrinsic evidence in an apparent attempt to show that “inhibiting” could have different meanings. *See, e.g.*, RXM-0002, RXM-0010, RXM11, RXM-

0014, and RXM-0017. Respondents’ approach violates the fundamental legal principles articulated in *Nautilus, Energizer Holdings v. Int’l Trade Comm’n*, 435 F.3d 1366, 1370 (Fed. Cir. 2006), and the other precedent cited above—which is that the definiteness of a claim term must be considered in view of the surrounding claim language, teaching of the specification, and relevant prosecution history; not in a vacuum. *Nautilus*, 572 U.S. at 910; *Energizer Holdings*, 435 F.3d at 1370; *HZNP Medicines LLC v. Actavis Lab’ys UT, Inc.*, 940 F.3d 680, 688 (Fed. Cir. 2019). None of Respondents’ dictionaries purports to address, much less show, what the term “inhibiting” means *in the context of claim 7* of the ’579 patent. Nor do any of Respondents’ extrinsic references show that, *in the context of the ’579 patent*, this term lacks reasonably discernable meaning. To the contrary, the mere fact that “inhibiting” may have different usages in different dictionaries is simply inapposite to this term’s meaning in claim 7. Further, the meaning of the term “inhibit,” as part of a different term not present in claim 7, or otherwise in a context completely unrelated to that of claim 7, is irrelevant to how a person of ordinary skill in the art would understand its meaning in the context of claim 7 of the ’579 patent. Regardless of the meanings in Respondents’ extrinsic evidence, it is the meaning of the term “inhibit” in claim 7 of the ’579 patent that counts—and that meaning is reasonably certain to a person of ordinary skill in the art as shown above. Kinget Decl. ¶¶ 51-57.

For these reasons, Respondents have failed to demonstrate clear and convincing evidence that the term “inhibiting” is indefinite, and the term should be construed to mean “suppressing or reducing” as Staff and Skyworks propose.

B. “low-frequency” (’579 patent claim 7)

Complainants	Respondents	Staff
Plain meaning, which is “below the lower edge of the	Indefinite	Plain meaning, which is “below the lower edge of the

band containing the fundamental frequency”		band containing the fundamental frequency”
This term is not indefinite		This term is not indefinite

Staff and Skyworks agree that “low-frequency,” recited in the term “inhibiting a low-frequency blocker signal from mixing with a fundamental frequency signal in the RF switch,” simply means “below the lower edge of the band containing the fundamental frequency signal,” and that this term is not indefinite. Respondents, by contrast, argue that “low-frequency” is so lacking in meaning that a skilled artisan would have had no ability to understand what the claim was talking about with reasonable certainty. For the reasons demonstrated below, Respondents fail to prove indefiniteness by clear and convincing evidence, and Staff’s and Skyworks’ construction should be adopted.

First, as it does with the “inhibiting” term above, Respondent KCT is taking a fundamentally inconsistent position on this “low-frequency” term in this Investigation from the position that it is simultaneously advancing in its November 12, 2024 IPR Petition to the PTAB. In this Investigation, Respondents say that a skilled artisan would have no ability to reasonably understand what the claimed “low-frequency blocker signal” is—despite the express claim language contrasting a “low-frequency blocker signal” with a “fundamental-frequency signal,” and the patent’s copious explanation of these signals in the specification—because “low” is a term of degree. But before the PTAB, Respondent KCT’s IPR Petition states that this same “low-frequency blocker signal” term in ’579 patent claim 7 describes a “*well-known* low-frequency, ‘out-of-band blocker’ signal problem” that “POSITAs” would have “*understood*[.]” See CXM-0010 (’579 IPR Petition) at 50. Although KCT’s IPR Petition is mistaken as to the scope and content of the prior art (as well as numerous other issues including motivation to combine and reasonable expectation of success), KCT’s admission that skilled artisans would

have understood what “low-frequency block signal” means in light of the plain language of claim 7 and clear teaching of the ’579 patent condemns its indefiniteness argument here. *Key Pharms*, 161 F.3d at 714-15 (“We find highly questionable Hercon’s assertion on appeal that the trial court erred when it adopted the very construction Hercon urged upon the court ... we look with extreme disfavor on Hercon’s assertion.”); *N. Telecom Ltd.*, 215 F.3d at 1290 (“[W]e look with ‘extreme disfavor’ on appeals that allege error in claim constructions that were advocated below by the very party now challenging them.”).

Second, to the extent that Respondents argue that the mere presence of the word “low” in the term “low-frequency blocker signal” renders this term incomprehensible to a skilled artisan, Respondents mistake the law of indefiniteness. It is only when a term of degree is “purely subjective,” such that it depends “on the unpredictable vagaries of any one person’s opinion,” that such terms become indefinite. *Datamize, LLC v. Plumtree Software, Inc.*, 417 F.3d 1342, 1350-51 (Fed. Cir. 2005). By contrast, the “low-frequency blocker signal” of ’579 patent claim 7 is neither subjective nor unpredictable because the claim language expressly contrasts this signal with the claimed “fundamental-frequency signal.” Claim 7 thus states an objective test for determining whether the claimed “blocker signal” is “low-frequency”: whether its frequency is below the lower edge of the “fundamental-frequency signal” band.

Third, as shown below, the ’579 patent’s claims, specification, prosecution history, and extrinsic evidence confirm that “low-frequency” is not indefinite. Rather, the claims and specification provide boundaries that allow skilled artisans to ascertain with reasonable certainty the scope of the claim. *Interval Licensing*, 766 F.3d at 1371. Accordingly, Respondents have failed to meet their burden of proving by clear and convincing evidence that the term “low-frequency” renders claim 7 invalid as indefinite.

1. *Claim Language*

Independent claim 7 of the '579 patent recites in relevant in part:

controlling an RF switch of the RF device by placing the first switch circuit in an ON state and placing the third switch circuit in an OFF state; and

inhibiting a *low-frequency* blocker signal from mixing with a *fundamental-frequency* signal in the RF switch using the first capacitor.

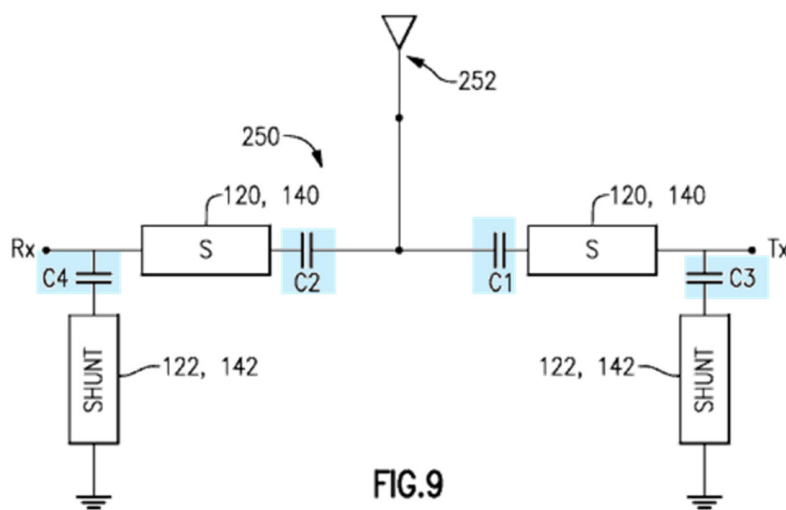
JXM-0003 ('579 patent) at 13:29-48 (emphasis added).

As is true for all claim terms, the term “low-frequency blocker signal” must be understood in the context of the surrounding claim language, and may not be considered solely in a vacuum. *Energizer Holdings*, 435 F.3d at 1370 (“Claim definiteness is analyzed ‘not in a vacuum, but always in light of the teachings of the prior art and of the particular application disclosure as it would be interpreted by one possessing the ordinary level of skill in the pertinent art.’”) (citing *In re Moore*, 439 F.2d 1232, 1235 (C.C.P.A. 1971)). Here, the plain language of claim 7 contrasts the claimed “low-frequency blocker signal” with “a fundamental-frequency signal in the RF switch.” JXM-0003 ('579 patent) at 13:46-48. The contrast drawn by this plain language confirms to a skilled artisan that the term “low-frequency,” in the context of '579 patent claim 7, means a frequency that is below the lower edge of the band containing the fundamental frequency. *Id.*; *see also* Kinget Decl. at ¶¶ 58-61. A skilled artisan would likewise understand—as Respondents apparently do not dispute—that the claimed “fundamental frequency” is a particular frequency in a band at which the claimed “radio-frequency (RF) device” operates. *Id.* Skyworks’ and Staff’s proposed construction of “low-frequency” as meaning “below the lower edge of the band containing the fundamental frequency” is thus entirely consistent with the language of claim 7.

2. *Specification*

The definiteness of the term “low-frequency blocker signal” is further confirmed by the ’579 patent’s specification, which consistently and repeatedly uses the term “low-frequency” in relation to a “fundamental frequency,” consistent with Staff’s and Skyworks’ proposed construction. For instance, the ’579 patent refers to a “capacitor configured to inhibit a *low-frequency* blocker signal from mixing with a *fundamental-frequency* signal in the switch.” JXM-0003 (’579 patent) at Abstract; *id.* at 1:37-40 (“[t]he system further includes a capacitor connected in series with the switch and configured to inhibit a *low-frequency* blocker signal from mixing with a *fundamental-frequency* signal in the switch.”) (emphasis added); *see also id.* at 1:55-57, 2:2-4, 2:15-17, 2:36-38, 3:7-10, 9:39-41, 9:49-53, 9:67-10:3. Each of these passages confirms the basic contrast recited in claim 7 itself, reinforcing to a skilled artisan that the “low-frequency blocker signal” is simply a signal that is below the lower edge of the band containing the “fundamental-frequency signal.”

Figure 9, copied below, likewise “shows an example where an RF switching configuration can include one or more capacitors to, for example, inhibit a *low-frequency* blocker from mixing with a *fundamental frequency*.” *Id.* at 3:7-10 (emphasis added).



Id. at Fig. 9. As the '579 patent explains, with capacitor C1, “a low-frequency jammer signal can be blocked or reduced from mixing with” the fundamental frequency during transmission. JXM-0003 ('579 patent) at 9:49-51, claim 7. As these disclosures demonstrate, the term “low-frequency” is not only used in the same way throughout the specification, it is used consistently with its usage in claim 7. *See id.* at claim 7, 1:55-57, 2:2-4, 2:15-17, 2:36-38, 3:7-10, 9:39-41, 9:49-53, 9:67-10:3. In other words, in both claim 7 and the specification, the term “low-frequency” is used in relation to the “fundamental frequency.” Based on the specification and claim language, a person of ordinary skill in the art would thus be able to ascertain the scope of “low-frequency” with reasonable certainty, and would understand it to mean “below the lower edge of the band containing the fundamental frequency.” Kinget Decl. at ¶¶ 58-63, 66.

3. ***Prosecution History***

As noted above, Respondent KCT, in its IPR Petition for the '579 patent, understood the meaning of the term “low-frequency” and applied it to the asserted prior art with no apparent uncertainty. Respondent KCT’s IPR Petition, for example, refers to “the *well-known* low-frequency, ‘out-of-band blocker’ signal problem” as something that “POSITAs *understood*[.]” CXM-0010 ('579 IPR Petition) at 50. In this same Petition, KCT and its expert also purport to explain how the prior art supposedly meets this “low-frequency” claim language without confusion over what “low-frequency” means. *Id.* at 48-51. KCT’s attempt to now contend that the term “low-frequency” renders claim 7 invalid as indefinite is inconsistent with the positions it took before the PTAB, and should be rejected.

4. ***Extrinsic Evidence***

Extrinsic evidence further confirms that “low-frequency” is not indefinite in claim 7. As Dr. Kinget explains, for example, a skilled artisan reading the '579 patent would readily understand the meaning of “low-frequency” in the context of claim 7 to be “below the lower

edge of the band containing the fundamental frequency.” Kinget Decl. at ¶¶ 58-66. Because a skilled artisan would be able to ascertain the meaning and scope of the term “low-frequency” with reasonable certainty, this term is both definite and valid. *Nautilus*, 572 U.S. at 910 (holding that § 112’s definiteness requirement requires only “that a patent’s claims, viewed in light of the specification and prosecution history, inform those skilled in the art about the scope of the invention with reasonable certainty”).

5. Respondents’ Expected Argument Is Mistaken

Respondents appear to rely primarily on extrinsic evidence, advancing a variety of dictionaries in an apparent attempt to show that “low-frequency” could have different meanings in different contexts. *See, e.g.*, RXM-0002, RXM-0010, RXM-0011, RXM-0013, RXM-0014, RXM-0016, RXM-0017. Respondents’ approach violates the fundamental legal principles articulated in *Nautilus*, *Energizer Holdings*, and the other precedent cited above—which is that the definiteness of a claim term must be considered in view of the surrounding claim language, teaching of the specification, and relevant prosecution history; not in a vacuum. *Nautilus*, 572 U.S. at 910; *Energizer Holdings*, 435 F.3d at 1370; *HZNP Medicines LLC v. Actavis Lab ’ys UT, Inc.*, 940 F.3d 680, 688 (Fed. Cir. 2019). None of Respondents’ dictionaries purports to address, much less show, what the term “low-frequency” means ***in the context of claim 7*** of the ’579 patent. Nor do any of Respondents’ extrinsic references show that, ***in the context of the ’579 patent***, this term lacks reasonably discernable meaning. To the contrary, the mere fact that “low-frequency” may have different usages in different dictionaries is simply inapposite to this term’s meaning in claim 7—where the express claim language identifies “low-frequency” as below the lower edge of the band containing the fundamental frequency. Kinget Decl. at ¶¶ 59, 66.

Finally, Respondents’ argument ignores that courts faced with similar intrinsic evidence have regularly construed terms like “low-frequency” as having clear and definite meaning. For

example, in *Saint Lawrence Commc'ns LLC v. Apple Inc.*, the court addressed a dispute over whether the word “low” in the claim term “low frequency portion” rendered the claim in question indefinite under § 112. *See* No. 2:16-cv-82, 2017 WL 2874526, at *11-12 (E.D. Tex. July 5, 2017). After analyzing the intrinsic record, the court “expressly reject[ed] Defendants’ indefiniteness argument” because “the relative bandwidths and the precise manner of filtering [were] implementation-specific details” within the skill of an ordinarily skilled artisan based on the patent’s teaching. *Id.* Similarly, in *ParkerVision, Inc. v. Qualcomm Inc.*, after considering the intrinsic record the court construed the term “lower frequency signal” to mean “a signal with frequency below the carrier signal frequency”—consistent with Staff’s and Skyworks’ proposed construction here. *See* No. 3:11-cv-00719, 2013 WL 633077, at *7-9 (M.D. Fla. Feb. 20, 2013).

For these reasons, Respondents have failed to demonstrate clear and convincing evidence that the term “low-frequency” is indefinite, and the term should be construed as Skyworks and Staff propose to mean “below the lower edge of the band containing the fundamental frequency.”

VII. AGREED UPON CONSTRUCTIONS

The parties agree on the constructions for those terms set forth in the Agreed Construction Section of their Joint Claim Construction Chart, filed November 27, 2024. These terms and constructions, as well as the rationale and support for the same, are set forth below:

Term	Agreed Upon Construction
“a gain correction circuit configured to generate a control current in response to activation of the power amplifier enable signal and to mirror the control current to generate a correction current”	Plain meaning, which is “a circuit for gain correction of the power amplifier configured to generate a control current in response to activation of the power amplifier enable signal and to mirror the control current to generate a correction current”
“time dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current” / “shaping an enable signal using a time-	Plain meaning, which is “a circuit configured to change an enable signal of the power amplifier to achieve a desired shape of a control current, where the control current changes based on time” / “changing an enable

dependent signal generator to generate the control current”	signal using a circuit to achieve a desired shape of a control current, where the control current changes based on time”
---	--

A. “a gain correction circuit configured to generate a control current in response to activation of the power amplifier enable signal and to mirror the control current to generate a correction current” (’563 patent, claims 14, 15, 17, and 20)

This term appears in claims 14, 15, 17, and 20 of the ’563 patent. Claim 14, for example, recites, among other things: the bias circuit including “a gain correction circuit configured to generate a control current in response to activation of the power amplifier enable signal and to mirror the control current to generate a correction current ...” JXM-0002 (’563 patent) at claim 14.

The parties agree that this term should be construed to mean “a circuit for gain correction of the power amplifier configured to generate a control current in response to activation of the power amplifier enable signal and to mirror the control current to generate a correction current.” The plain meaning of this term as well as the intrinsic evidence, including the specification for the ’563 patent, support this construction. For example, the ’563 patent explains:

In certain implementations described herein, a power amplifier bias block includes a primary biasing circuit and *a gain correction* block including a time-dependent signal generator and a current amplifier. The time-dependent signal generator can be used to shape the enable signal of the power amplifier so as to *generate a control current*, which can be amplified by the current amplifier to *generate a correction current*. The primary biasing circuit can use the correction current to correct for a variation in gain of the power amplifier that can occur shortly after the power amplifier is enabled.

JXM-0002 (’563 patent) at 8:54-67 (emphasis added). Thus, the parties agree that, according to the specification and the plain meaning, “a gain correction circuit configured to generate a control current in response to activation of the power amplifier enable signal and to mirror the control current to generate a correction current” is “a circuit for gain correction of the power

amplifier configured to generate a control current in response to activation of the power amplifier enable signal and to mirror the control current to generate a correction current.”

B. “time dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current” / “shaping an enable signal using a time-dependent signal generator to generate the control current” (’101 patent, claims 1, 2, 10, 11, 17, 18, 20, 21, and 22)

Different versions of this term appear in claims 1, 2, 10, 11, 17, 18, 20, 21 and 22 of the ’101 patent. Independent claims 1 and 21, for example, recite, among other things: the bias block including “a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current” JXM-0001 (’101 patent) at claims 1, 21. Independent claim 17 of the ’101 patent recites “shaping an enable signal using a time-dependent signal generator to generate the control current.” *Id.* at claim 17.

The parties agree that this term from claims 1 and 21 should be construed to mean “a circuit configured to change an enable signal of the power amplifier to achieve a desired shape of a control current, where the control current changes based on time.” Similarly, the parties agree that this term from claim 17 should be construed to mean “changing an enable signal using a circuit to achieve a desired shape of a control current, where the control current changes based on time.” The plain meaning, as well as the intrinsic evidence, including the specification for the ’101 patent, support this construction. For example, the ’101 patent explains:

The *time-dependent signal generator* or control block can be used **to shape the enable signal so as to generate a control current**, which can be amplified by the current amplifier to generate a correction current. The primary biasing circuit can use the correction current to correct for a variation in gain of the power amplifier that can occur shortly after the power amplifier is enabled.

JXM-0001 (’101 patent) at 8:39-49 (emphasis added). The specification also provides:

The RC network 82 can be used to *shape the enable signal ENABLE so as to generate the control current* I_{CONTROL}. For example, the capacitor 90 and the second resistor 92 can have an RC time-constant selected to *achieve the desired shape of the control current* I_{CONTROL}.

Id. at 10:37-41; *see also id.* 12:38-41 (“a time-dependent signal generator is used to generate a signal that can be used to adjust a power amplifier’s bias current during a time period within about 8 μ s after the power amplifier is enabled”), *id.* at 13:45-48.

Thus, the parties agree that, according to the plain meaning and the specification, these terms should be construed as set forth above.

VIII. CONCLUSION

For the reasons set forth above, Skyworks’ proposed constructions should be adopted.

Respectfully Submitted,

/s/ Derek A. Gosma

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DECLARATIONS

**UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.**

**Before the Honorable MaryJoan McNamara
Administrative Law Judge**

In the Matter of

**CERTAIN WIRELESS FRONT-END
MODULES AND DEVICES CONTAINING
THE SAME**

Investigation No. 337-TA-1413

**DECLARATION OF DAVID WENTZLOFF, PH.D.
IN SUPPORT OF COMPLAINANTS' *MARKMAN* BRIEF**

I, David Wentzloff, Ph.D., declare and state as follows:

I. INTRODUCTION

1. I have been retained as an independent expert in this Investigation by complainants Skyworks Solutions, Inc., Skyworks Solutions Canada, Inc., and Skyworks Global Pte. Ltd. (collectively, “Complainants”) to provide opinions concerning technical background to U.S. Patent 8,717,101 (the “’101 patent”) and U.S. Patent 9,917,563 (the “’563 patent”), as well as certain language that appears in the ’101 and ’563 patents. If called upon, I would be willing to testify as set forth in this declaration.

2. I understand that the parties to this Investigation submitted a joint claim construction chart listing the terms from the ’101 patent and the ’563 patent that are in dispute and each parties’ respective construction of that claim. I have reviewed the ’101 and ’563 patents, the ’101 and ’563 patents’ prosecution history, the parties’ joint claim construction chart, and the other materials that I cite and/or describe in more detail herein.

3. I am being compensated at my normal consulting rate of \$650 per hour. My compensation does not depend on the outcome of this Investigation, and in no way affects the substance of my statements in this Declaration.

II. PROFESSIONAL BACKGROUND

4. My qualifications are stated more fully in my curriculum vitae, which is attached as Exhibit A. Below is a summary of my education, work experience, and other qualifications.

5. I received a Bachelor of Science in Electrical Engineering from the University of Michigan in 1999, and a Master of Science and Ph.D. in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology, in 2002 and 2007, respectively.

6. Throughout the course of my education, including my B.S., M.S., and Ph.D. degrees, I was involved in the design and fabrication of RF, analog, and mixed-signal integrated circuits (IC) and the applications they enable in communications, sensing, and power management, as well as other applications. As a part of my B.S. degree, I focused on analog integrated circuits as my area of concentration, which included courses in discrete circuits, electromagnetics, CMOS and Bipolar transistors, and integrated circuits. My capstone design course was titled Monolithic Amplifier Circuits, which covered analog IC design with a design project. As a part of my Ph.D. I took every graduate-level analog and digital circuits course offered at MIT. This included an analog IC course, and an RF IC course, which covered amplifiers, biasing, and power amplifiers. My Ph.D. thesis at MIT was titled Pulsed-Based Ultra-Wideband Transmitters for Digital Communication. I studied novel RF IC designs for wideband transmitters, and fabricated a number of chips in Bipolar and CMOS processes to demonstrate these techniques.

7. Since August, 2007 I have been with the University of Michigan, Ann Arbor, where I am currently a Professor of Electrical Engineering and Computer Science. My research focuses on RF integrated circuits for wireless communication applications. This includes the study of novel circuit designs for RF ICs that achieve better performance, energy efficiency, or higher levels of integration. My group has fabricated dozens of RF chips to prototype these designs and characterize their performance with measured results. These results have been published in over 100 peer-reviewed conferences and journals. I have advised and graduated 25 Ph.D. students since 2007, and currently advise 10 Ph.D. candidates in my research group, all focused on RF IC design. I primarily teach circuits classes ranging from introductory-level circuits to graduate level analog and RF IC courses.

8. I received the 2009 DARPA Young Faculty Award, 2009-2010 Eta Kappa Nu Professor of the Year Award, 2011 DAC/ISSCC Student Design Contest Award, 2012 IEEE Subthreshold Microelectronics Conference Best Paper Award, the 2012 NSF CAREER Award, the 2014 ISSCC Outstanding Forum Presenter Award, the 2014-2015 Eta Kappa Nu ECE Professor of the Year Award, the 2014-2015 EECS Outstanding Achievement Award, and the 2015 Joel and Ruth Spira Excellence in Teaching Award. I have served on the technical program committee for ICUWB 2008-2010, ISLPED 2011-2015, S3S 2013-2014, RFIC 2013-2022, and ISSCC 2020-2022, and as a guest editor for the IEEE T-MTT, the IEEE Communications Magazine, and the Elsevier Journal of Signal Processing: Image Communication. I am a senior member of IEEE, IEEE Circuits and Systems Society, IEEE Microwave Theory and Techniques Society, IEEE Solid-State Circuits Society, and Tau Beta Pi.

9. In 2012, I co-founded Everactive to commercialize self-powered Internet of Things (IoT) sensors based on ultra-low power wireless SoCs. Throughout my teaching, research, and entrepreneurship experiences, I have had extensive experience in the design and fabrication of RF and analog integrated circuits. For example, I have evaluated hundreds of student design projects in analog IC courses and assessed their functionality and performance. I, along with my research group, have designed dozens of IC prototypes including the world's lowest power Bluetooth transmitter, the smallest fully-integrated transceiver, receivers for cellular communication in GSM, 3G, 4G, and recently 5G satellite communication, and WiFi wakeup receivers. These have used CMOS or Bipolar processes, and have been fully characterized in my lab at the University of Michigan. At Everactive, I have commercialized some of this technology into production-level designs that are now being shipped in industrial IoT products.

III. MATERIALS CONSIDERED

10. In preparing this declaration, I have reviewed the claims, specification, and file history of the '101 and '563 patents. I understand that the '101 patent issued from U.S. Patent Application No. 13/468,749, which was filed on May 10, 2012. I understand that the '563 patent issued from U.S. Patent Application No. 15/377,842, which was filed on December 13, 2016, and is a continuation of U.S. Patent Application No. 14/825,053, filed Aug. 12, 2015, which is a continuation of U.S. Patent Application No. 14/242,150, filed Apr. 1, 2014, which is a continuation of the U.S. Patent Application No. 13/468,749. Both the '101 and '563 patents also claim priority to U.S. Provisional Application No. 61/486,186, filed on May 13, 2011.

11. I have reviewed and understand the references and exhibits cited in this declaration.

12. My opinions are further based on my education, training, research, knowledge, and experience.

IV. UNDERSTANDING OF THE LAW

13. I am not an attorney. For this declaration, I have been informed about certain aspects of the law that are relevant to claim construction. My understanding of the law is set forth below.

14. I have been informed and understand that the terms of a patent claim are generally given their ordinary and customary meaning to a person of ordinary skill in the art at the time of the claimed invention, which is ordinarily when the priority application for the patent at issue was filed. For this declaration, I have assumed that the priority date for the '101 and '563 patents is May 13, 2011.

15. I have been informed and understand that a claim term should be construed in the context of the patent claim as a whole. I also have been informed and understand that the specification of the patent is relevant to a claim term's meaning and that a claim term must be read in light of the specification of which it is a part.

16. I have been informed and understand that a patent specification may provide a special definition for a claim term that is not the same as the ordinary and customary meaning it would otherwise have. When this is the case, the patent specification's own lexicography controls the claim term's meaning.

17. I have been informed and understand that a patent specification may contain a disclaimer or disavowal of claim scope. In order for such a disclaimer or disavowal to apply to a claim term, the disclaimer or disavowal must be clear and unmistakable. When that is the case, the disclaimer or disavowal controls, even if the ordinary and customary meaning of the claim term might otherwise include the disclaimed or disavowed subject matter.

18. I have been informed and understand that a patent's file history (also called its prosecution history) is relevant to the meaning of a patent's claim terms. In particular, an applicant's or patent owner's statements to the Patent Office characterizing its invention may give rise to prosecution disclaimer, which can arise from both claim amendments and arguments made to the Patent Office during patent prosecution, including during inter partes review (IPR) proceedings. I have been informed and understand that such a prosecution disclaimer must be clear and unmistakable to a person of ordinary skill in the art. For example, if a patentee or patent applicant makes a clear and unmistakable statement during prosecution to overcome a prior art reference, prosecution disclaimer applies, even if the patentee's disclaimer may not have been necessary to avoid the prior art reference. If, on the other hand, a patentee's or patent

applicant's statements made during prosecution are ambiguous or amenable to multiple reasonable interpretations, prosecution disclaimer does not apply.

19. I have been informed and understand that the claim language, specification, and prosecution history of patent, including IPR proceeding records, are referred to as "intrinsic evidence."

20. I have been informed and understand that evidence external to the patent and prosecution history are referred to as "extrinsic evidence." Such extrinsic evidence can include dictionaries, treatises or textbooks, or published technical papers. I have been further informed and understand that extrinsic evidence is less significant than the intrinsic evidence in determining the meaning of claim language, and that extrinsic evidence cannot be used to contradict the meaning of a claim term that is unambiguous in view of the intrinsic evidence.

V. LEVEL OF ORDINARY SKILL IN THE ART

21. A person of ordinary skill in the art (POSITA) at the time of the invention of the '101 and '563 patents would have had at the time of the alleged invention at least a Bachelor's Degree in Electrical Engineering or a related field and at least two years of training or additional work experience in the area of RF electronics, or a related field.

22. At the time of the alleged invention of the '101 and '563 patents, I would have qualified as a POSITA. All the opinions I express in this declaration have been made from the perspective of a POSITA in the field of the '101 and '563 patents at the time of the invention (May 13, 2011).

VI. BACKGROUND OF THE INVENTION

A. Analog Circuit Electrical Concepts

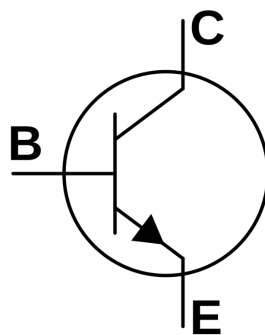
23. Voltage refers to the electrical potential difference between two points in a circuit. A voltage produces a current, which is the flow of electric charge through the circuit. A resistance is a material's tendency to resist the flow of current. To analogize to a common mechanical system of water in a hose, voltage is analogous to the pressure of the water, current is analogous to the flow of the water through the hose, and resistance is analogous to kinks in the hose that slow down the water flow. Ohm's law defines the relationship between voltage (V), current (I), and resistance (R) as: $V = I \times R$.

24. As noted above, resistance is the tendency to oppose current flow caused by a resistor. Impedance is a characteristic of a circuit element that measures the opposition to current flow from a more comprehensive list of circuit components, including inductors and capacitors. At any junction in the circuit, the total current entering the junction equals the total current leaving it. The sum of all electrical potential differences (voltages) around any closed loop in the circuit is zero. The current (I) flowing through a circuit branch between two points is directly proportional to the voltage (V) across the two points and inversely proportional to the impedance (Z) between them, expressed as $V = I \times Z$. This is a more comprehensive expression of Ohm's law as set forth above ($V = I \times R$). In other words, for a pure resistor where $Z = R$, Ohm's law can be expressed as $V = I \times R$.

25. The input impedance of a circuit block determines how much current flows into the input port of the circuit block when a voltage signal is applied. Conversely, the output impedance of a circuit block indicates how sensitive an outgoing signal from a port of the circuit block is subject to the input impedance of the next stage of a circuit. Proper matching of input and output impedances is crucial for efficient signal transfer and optimizing circuit performance for its designed purpose. In most cases, circuit blocks are added at the input or output of a circuit

specifically to control the value of the input or output impedances, respectively. For example, a microphone is a transducer that converts sound to an electrical signal. A speaker does the reverse, converts an electrical signal to sound. Because a microphone has a high output impedance, and a speaker has a low input impedance, if you connect a microphone directly to a speaker you will not hear any sound from the speaker because of the mismatch in impedances. By inserting an amplifier between the microphone and speaker, where the amplifier has high input impedance (to match the microphone output) and low output impedance (to match the speaker input), the amplified audio can be heard – even if the amplifier volume (gain) is turned down so that the speaker sound level is less than the original sound picked up by the microphone. This is referred to as transforming the impedance, in this example from a high impedance to a low impedance, to be able to drive the low impedance speaker from a high impedance microphone.

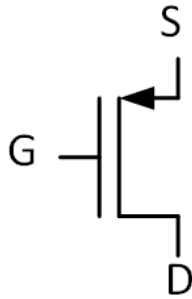
26. A bipolar junction transistor (BJT), shown in the figure below, is one type of semiconductor device with three terminals: an emitter (E), a base (B), and a collector (C).



It operates by using a small current going into the base (B) of the transistor to control a larger current flowing from the collector (C) to the emitter (E). The voltage difference between the base (B) and emitter (E) is called the base–emitter voltage. The voltage difference between the collector (C) and emitter (E) is called the collector–emitter voltage. The current (I_E) at the

emitter is the sum of the current (I_C) at the collector and the current (I_B) at the base, or $I_E = I_C + I_B$.

27. A Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is another type of semiconductor device with three terminals: a gate (G), a source (S), and a drain (D).



A MOSFET transistor operates by using a voltage difference applied between the gate (G) terminal and the source (S) terminal, which is called the gate-source voltage, to control a current flowing between the drain (D) and source (S) terminals.

B. Types of Amplifiers

28. Amplifiers in integrated circuits work by taking an input signal (voltage or current) and producing an output signal that has a gain relative to the input signal, while preserving the input signal's characteristics like frequency, shape, or waveform. When the gain is achieved of an output voltage relative to an input voltage, the amplifier is a voltage amplifier. When the gain is achieved of an output current relative to an input current, the amplifier is a current amplifier.

29. An amplifier that produces an output signal that is greater than the input signal has a gain of greater than one. For example, if the gain of a current amplifier is three (3), the output current is three times larger than the input current. Many amplifiers, however, have unity

gain, which means the amplitude of the output signal and the input signal are the same. That is, the gain is 1, or unity.

30. A simple current amplifier is the common-base current amplifier shown below.

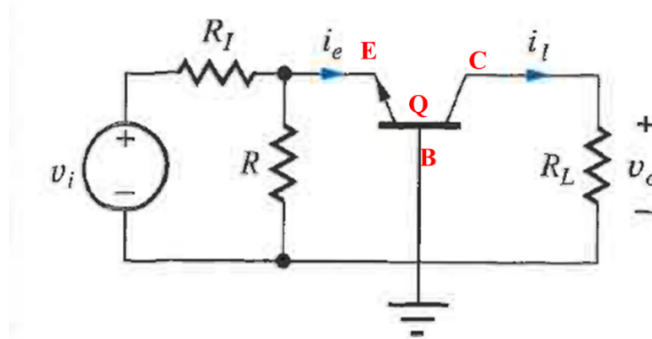


Figure 14.24 Common-base current gain.

CXM-0002 (Microelectronic Circuit Design) at 899, Figure 14.24. In this exemplary current amplifier, an input current i_e flows into the emitter terminal E (annotation E added) of the bipolar transistor Q (annotation Q added). An output current i_l flows from the collector terminal C (annotation C added) of the bipolar transistor Q. The gain of this current amplifier, which is the ratio of the output current i_l over the input current i_e , is slightly less than one, which is near unity gain. *See id.* at 898 (formula 14.88).

31. As another example, a MOSFET equivalent of the common-base current amplifier shown above is a common-gate amplifier, which has a current gain of one. *See id.* at 898-99 (“the common-base current **gain is simply** α_o . For the FET, α_o is **exactly 1**...”), Figure 14.25(b). The common-gate amplifier, therefore, has unity gain, or a gain of 1.

32. Amplifiers with unity gain—where the input and output magnitudes are the same—are very common in circuits. For example, one well known electronics textbook refers to an “amplifier” to “maintain unity gain,” “a unity gain feedback configuration” of an amplifier, and a “basic amplifier has a unity-gain bandwidth.” CXM-0001 (Analysis and Design of Analog Integrated Circuits) at 284-85, 634, 635. *See also* CXM-0003 (Art of Electronics) at 318

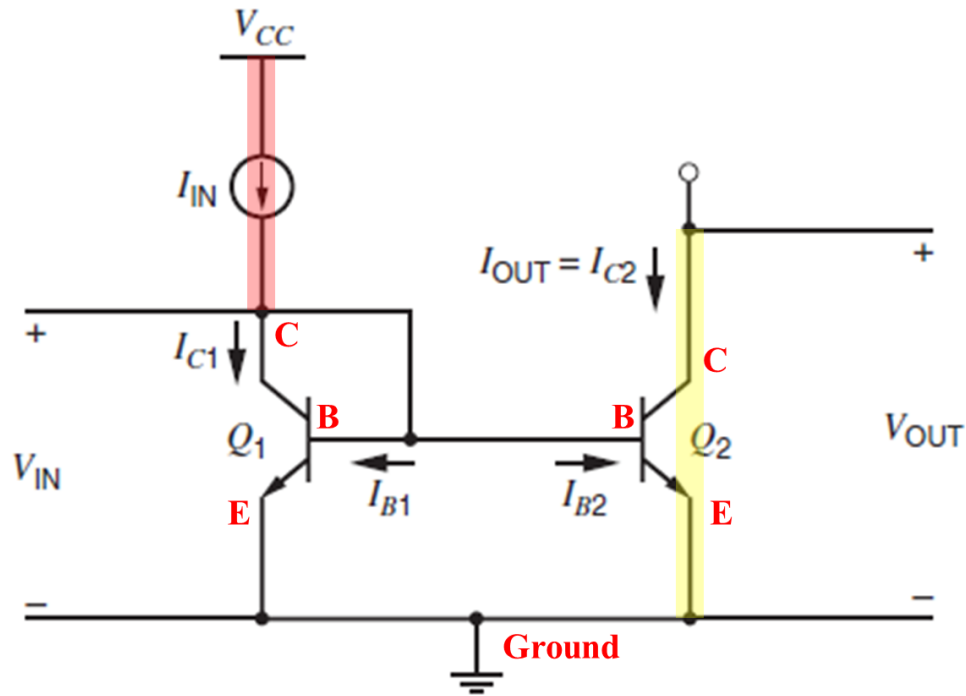
(referring to “unity gain current amplifiers”), CXM-0004 (paper entitled “High-speed CMOS unity-gain current amplifier”).

33. Unity gain amplifiers are commonly used in voltage amplifiers to act as a buffer between an input and an output circuit, and in current amplifiers to prevent a downstream circuit connected to the amplifier’s output from loading the amplifier improperly. Buffers with unity gain serve an important role of impedance transformation, as described in the microphone and speaker example above. This enables a circuit to drive an output signal onto a load, ideally regardless of the value of the load impedance, without impacting the amplitude of the input signal. *See, e.g.*, CXM-0007 (Authoritative Dictionary of IEEE Standards Terms) at 124 (“**buffer amplifier** ... An amplifier in which the reaction of output-load impedance variation on the input circuit is reduced to a minimum for isolation purposes.”); *id.* at 592 (“**isolation amplifier (buffer)** An amplifier employed to minimize the effects of a following circuit on the preceding circuit.”).

34. A common-base current amplifier or a common-gate current amplifier transforms an input current signal with a low input impedance into an output current of substantially the same amplitude, but with a high output impedance. After such impedance transformation and with a high output impedance, the unity gain current amplifier prevents the circuit downstream from loading the input undesirably. Instead, the unity gain current amplifier enables the output current, which substantially equals the input current due to the unity gain, to operate independent of loading and the voltage applied to the port where the output current flows out. This desirable characteristic of a unity gain current amplifier makes it a common circuit element in electronics.

C. Current Mirrors

35. Current mirrors have long been used as building blocks in analog circuits to mirror or replicate a reference current through an input branch into one or more output branches. A simple current mirror having two bipolar transistors is shown below.



CXM-0001 (Analysis and Design of Analog Integrated Circuits) at 253, Figure 4.2 (“The simplest form of a current mirror consists of two transistors. Fig. 4.2 shows a bipolar version of this mirror.”). This simple two-transistor theme, with the bases or gates of the transistors tied together, is the base from which numerous variations of the current mirror have been derived.

36. In this current mirror, the input branch is defined by bipolar transistor Q_1 and receives an input or reference current I_{IN} (highlighted red). The output branch of this current mirror is defined by bipolar transistor Q_2 , and the output current I_{C2} (highlighted yellow) is a replicated version of the reference current I_{IN} . In this current mirror, the base B (annotation B added) of each transistor Q_1 , Q_2 is tied together, which results in the voltage applied to each base

B being the same. In addition, the emitter E (annotation E added) of each transistor is, for this current mirror, connected to a common ground (labeled above). As a result, the base-emitter voltages of Q1 and Q2 are the same. Finally, the collector C (annotation C added) of transistor Q1 is tied to the base B of transistor Q1, meaning this transistor is diode connected. The diode-connected configuration of the reference transistor Q1 ensures that Q1 operates in an active region, which allows a stable relationship between its base current and collector current and allows the input current at the base (B) to be translated to a stable base-emitter voltage.

37. As explained above, the base-emitter voltages of each transistor Q₁ and Q₂ are the same. In other words, the input and output branches of the current mirror will operate identically if they are physically matched and placed in similar conditions. This means that the ratio of the output current to the input reference current is determined by the ratio of the physical dimensions of the output branch transistor Q₂ compared to the input branch transistor Q₁. If the input branch transistor Q₁ and the output branch transistor Q₂ are sized the same, the output current I_{C2} will equal the input reference current I_{IN}, and the current mirror will have unity gain. With reference to the current mirror shown above, the *Analysis and Design of Analog Integrated Circuits* textbook of CXM-0001 states that “[i]f the transistors are identical, $I_{S1} = I_{S2}$ and (4.2) shows that the current flowing in the collector of Q₁ is mirrored at the collector of Q₂,” meaning that this current mirror has unity gain. CXM-0001 at 253. The *Analysis and Design of Analog Integrated Circuits* textbook of CXM-0001 also states that “[i]f the gain is unity, the input current is reflected to the output, leading to the name *current mirror*.” CXM-0001 at 251 (emphasis in original). As set forth above, unity-gain current amplifiers are common in the electronics field, and such unity-gain current amplifiers can be implemented as unity-gain current mirrors. See also *id.* at 827 (“We choose M₂₅ to be matched to M₅, so they form a **unity-gain current**

mirror.”); SMX-0001 (Electrical and Electronics Engineering Dictionary) (“current mirror A circuit in which the current on one side is forced to be a replica of that of the other side. Accomplished, for instance, by the bases and emitters of two bipolar junction transistors being connected together.”).

38. By contrast, the *Analysis and Design of Analog Integrated Circuits* textbook of CXM-0001 also describes another type of circuit called cascaded transistors, meaning the output of a first transistor is connected as the input of a second transistor, as exemplified by Q_1 and Q_2 in the figure below.

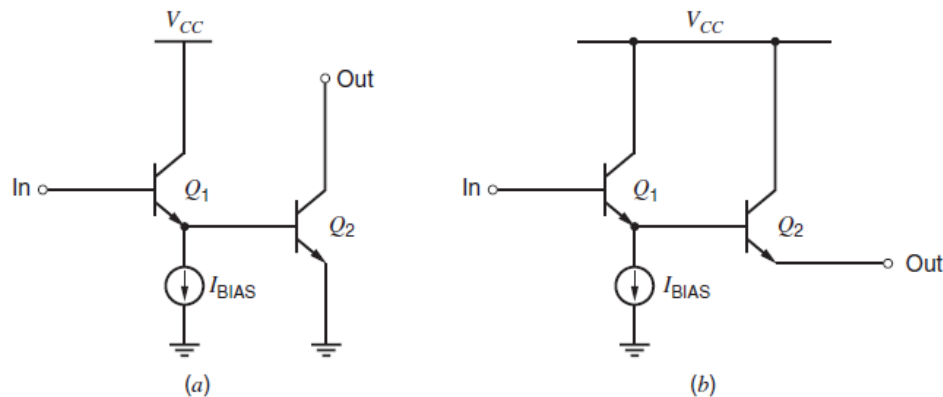


Figure 3.30 (a) Common-collector–common-emitter cascade. (b) Common-collector– common-collector cascade.

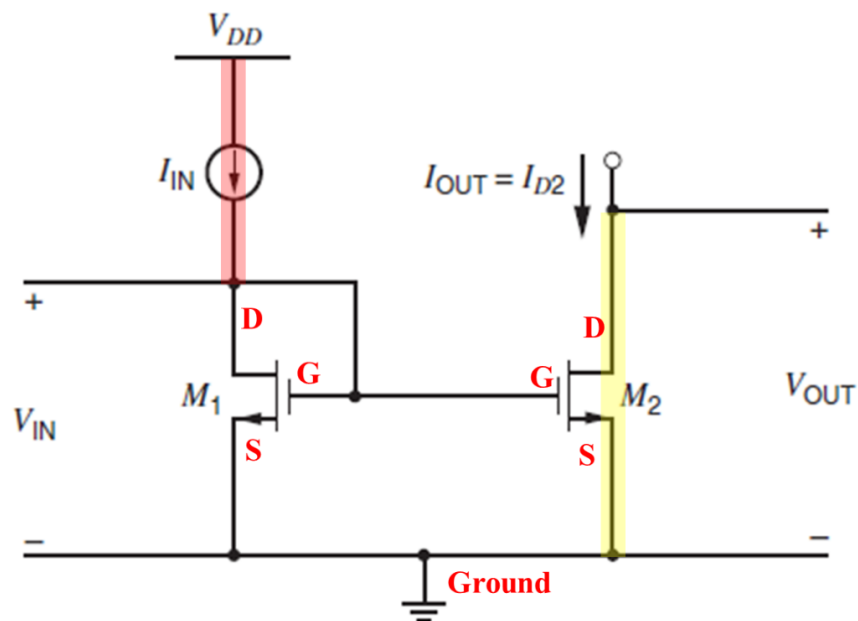
CXM-0001 at 202, Figure 3.30. Although the cascaded transistors can also appear to be a pair of transistors, they’re a distinct type of circuit compared to a current mirror, and they serve different design purposes and have different electrical properties. For example, the current mirror has high output impedance, whereas the cascaded transistors in Figure 3.30(b) have low output impedance. The *Analysis and Design of Analog Integrated Circuits* textbook of CXM-0001 nowhere refers to the cascaded transistors as a “current mirror.”

39. During its operation, the current mirror set forth above in paragraph 35 receives an input reference current through its input branch including the transistor Q_1 and replicates the

reference current to produce a consistent output current through its output branch including the transistor Q_2 , where the output reference current is of the same magnitude as the input reference current.

40. Each branch of a current mirror can, however, be sized differently to achieve a non-unity gain. It is possible, therefore, that each output branch will be sized the same as the input branch (to achieve unity gain) or that each output branch is sized differently to achieve a scaled up or scaled down version of the reference current I_{IN} .

41. A simple current mirror using two MOSFET transistors, and for present purposes the equivalent of the bipolar current mirror above, is shown below.



CXM-0001 (Analysis and Design of Analog Integrated Circuits) at 256, Figure 4.4. MOSFET transistors (e.g., M_1 and M_2 in the figure above) have a gate G (annotation G added), a source S (annotation S added), and a drain D (annotation D added), as opposed to a base, an emitter, and a collector in a bipolar transistor. Whereas the bipolar transistor current mirror above has a common base-emitter voltage for each transistor Q_1 and Q_2 , the equivalent MOSFET current

mirror has a common gate-source voltage for each transistor M_1 and M_2 . That is because, in the MOSFET current mirror depicted above, the gates of the two transistors M_1 and M_2 are tied together, and the sources of the two transistors M_1 and M_2 are also tied together to a common ground.

42. Therefore, like its bipolar counterpart, this MOSFET current mirror similarly receives an input reference current through its input branch including the transistor M_1 and replicates the reference current to produce a consistent output current through its output branch including the transistor M_2 . The ratio of the output current to the reference current is determined by the ratio of the physical dimensions of the output branch transistor M_2 compared to the input branch transistor M_1 . If the input branch transistor M_1 and the output branch transistor M_2 are sized the same, the output current I_{C2} will equal the reference current I_{IN} (unity gain).

43. An important benefit of current mirrors, whether having unity gain or non-unity gain, is that they have high output impedance. High output impedance makes the output current less sensitive to changes of the output voltage. This is particularly useful in analog circuits to ensure that the output current delivered by the current mirror remains stable despite variations in the output voltage, for example, V_{OUT} in the exemplary figure of a bipolar current mirror above. Put differently, current mirrors are designed to drive a stable output current regardless of the load impedance that is connected to the output of the current mirror (e.g., terminal C of transistor Q2 in the exemplary figure of a bipolar current mirror above). Rather, the value of the output current depends only on the reference current, which relies on the matching of physical dimensions between the reference branch transistor and the output branch transistor. MOSFET current mirrors, whether having unity gain or non-unity gain, also have the benefit of high output

impedance such that any load impedance that may be connected to the output branch wouldn't change the amount of the output current significantly.

44. A current mirror can be used as a current amplifier. When the ratio of physical dimensions of the current mirror's output branch compared to its input reference branch is one, the current mirror is a unity-gain current amplifier. For example, the simple bipolar current mirror and the simple MOSFET current mirror explained above both have properties similar to the unity-gain current amplifier explained in the previous section, such as low input impedance and high output impedance.

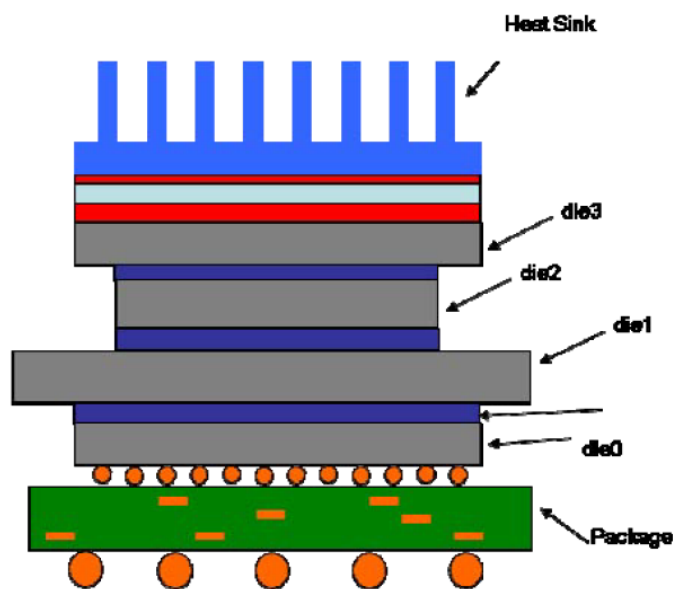
D. Integrated Circuits

45. Integrated circuits (ICs) are the building blocks of modern electronics including radio frequency (RF) devices used in cell phones and routers such as WiFi Front-end Modules (FEMs). The packing of progressively more and more circuitry into these devices has led to the development of more powerful, efficient, and cost-effective technology.

46. During the early days of the electronics industry, individual components like transistors, resistors, and capacitors were physically discrete parts that were interconnected on a circuit board or substrate. As technology in the electronics industry developed, discrete components began to limit the miniaturization trend of circuits and therefore hindered improvement in cost efficiency, performance, and reliability. The industry evolved by integrating individual components onto semiconductor substrates, dramatically increasing the density of components, reducing circuit size, reducing power requirements, and lowering costs. Today's circuits are typically fabricated on semiconductor wafers, which are cut into hundreds of thousands of individual pieces, called dies.

47. One type of integrated circuit is a monolithic integrated circuit, in which all integrated components are fabricated on a single die. CXM-0009 (Shepherd), at 1; CXM-0007 (Authoritative Dictionary of IEEE Standards Terms) at 708 (“**monolithic integrated circuit** An integrated circuit formed in a single piece of the substrate material.”). Another type of integrated circuit is multi-die integrated circuit (aka multichip integrated circuit), in which all integrated components are fabricated on two or more interconnected dies. *Id.* at 712 (“**multichip integrated circuit** An integrated circuit whose elements are formed on or within two or more semiconductor chips that are separately attached to a substrate.”). A monolithic integrated circuit is fabricated using a single semiconductor process, while a multi-die integrated circuit can be fabricated using different process technologies for each die tailored to each die’s function.

48. A multi-die integrated circuit is often packaged into a single package, e.g., a multi-chip module (MCM), a system-in-package (SiP), or a 3D integrated circuit (3D IC). An example multi-die integrated circuit is shown below.



CXM-0008 (Jain IEEE paper), at 2 (“Figure 1 schematically shows a multi-die 3D IC, with four unequally sized die”), Figure 1. CXM-0008 repeatedly refers to “three-dimensional integrated circuits” or “3D ICs.” *Id.* at 1-2. In this integrated circuit, four dies are integrated: die0, die1, die2, and die3.

49. The multi-die integrated circuit allows integration of heterogeneous technologies in one package, such as a single RF front-end module (FEM) package. The integration of heterogeneous technologies enables utilizing advantages of different semiconductor processes for various design goals of each different die. For example, for one die in a packaged integrated circuit, a standard CMOS semiconductor fabrication process might be the best technical fit for the circuit functions and might be more cost efficient than another semiconductor fabrication process technology, while for another die in the same packaged integrated circuit, a different semiconductor fabrication process technology might be the best technical fit. Further, a multi-die integrated circuit can achieve lower overall cost due to better yield and process optimization for individual dies.

VII. INTRODUCTION TO U.S. PATENT NOS. 8,717,101 AND 9,917,563

50. The '101 patent is titled “Apparatus and methods for biasing power amplifiers.” The patent issued from U.S. Patent Application No. 13/468,749, which was filed on May 10, 2012. JXM-0001 ('101 patent) at cover page. The '563 patent issued from U.S. Patent Application No. 15/377,842, which was filed on December 13, 2016 and which claims priority through a string of applications to the application that issued as the '101 patent. JXM-0002 ('563 patent) at cover page. The '101 and '563 patents also claim priority to U.S. Provisional Application No. 61/486,186 filed on May 13, 2011, which is the priority date I used for my analysis. JXM-0001 ('101 patent) at cover page; JXM-0002 ('563 patent) at cover page. The

'101 and '563 patents share a common specification, so in this section of my declaration, the citations are to the '101 patent.

51. The '101 patent relates generally to radio frequency ("RF") power amplifier systems and methods for biasing power amplifiers. The patent explains that "amplifying the RF signal to an incorrect power level can cause a wireless device to transmit out of band," which can make it important to manage this amplification. JXM-0001 ('101 patent) at 1:28-30. As such, the '101 patent states the need for "improved power amplifier systems" and "improving power amplifier biasing." *Id.* at 1:31-33.

52. The '101 patent addresses this problem, for example, through a "power amplifier system" that may contain a "bias block [that] includes a time dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current, a current amplifier configured to amplify the control current to generate a correction current, and a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current." JXM-0001 ('101 patent) at 1:37-46. According to the '101 patent, such a power amplifier system "correct[s] for a variation in gain of the power amplifier when the power amplifier is enabled," which "can improve the power amplifier's performance." *Id.* at 1:46-48; 4:39-42.

53. Figure 5 depicts one embodiment of the power amplifier system of the '101 and '563 patents:

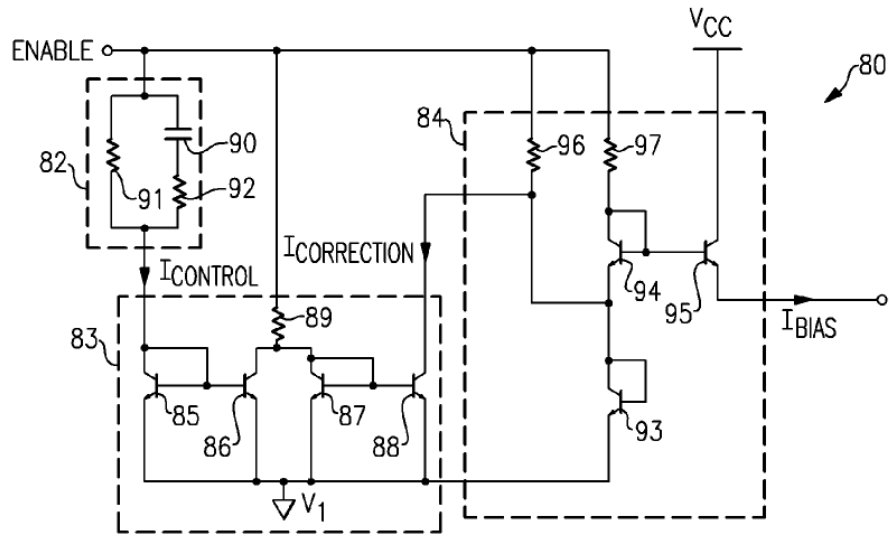
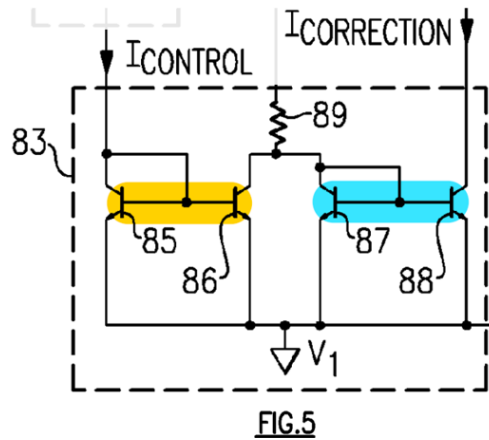


FIG.5

JXM-0001 ('101 patent) at Fig. 5. The depicted power amplifier bias block 80 includes “a resistor-capacitor (RC) network 82, a current mirror 83, and a primary bias circuit 84.” *Id.* at 10:19-21. During operation, the RC network 82 can use the enable signal to generate the control current I_{CONTROL} . *Id.* at 10:37-38. The RC network 82 functions as a time-dependent signal generator in performing its function. The current amplifier 83 can then use the control current I_{CONTROL} to generate the correction current $I_{\text{CORRECTION}}$. *Id.* at 10:62-11:1. The primary bias circuit 84 can then use the correction current, at least in part, to generate a bias current for the power amplifier. *Id.* at 11:46-67. The '101 patent refers to block 83 of Figure 5 as both a “current mirror 83” and current “amplifier 83.” *Id.* at 10:62-65. The specification explains that the “current mirror 83 operates as a current amplifier” that is configured “to achieve a target gain,” which can be “any suitable gain.” *Id.* at 10:21-23, 11:39-45.

54. In Figure 5, an excerpt of which is below, the “current amplifier can be formed by two “current mirrors.”



Id. at Fig. 5 (partial, annotated); 10:67-11:27. The specification states that “[t]he first NPN bipolar transistor 85 includes ... a base and a collector electrically connected to a base of the second NPN bipolar transistor 86” and that “a base and a collector of the third NPN bipolar transistor 87” is “electrically connected ... to a base of the fourth NPN bipolar transistor 88.” *Id.* at 11:7-27. As shown above, the bases of bipolar transistors 85 and 86 are connected by the trace highlighted in yellow, and the bases of transistors 87 and 88 are also connected by the trace highlighted in blue.

55. The '101 patent also discloses how components for the power amplifier can be arranged. The specification discloses “one example of a packaged power amplifier module” and further states that the “packaged power amplifier module 300 includes an IC or die 301.” JXM-0001 ('101 patent) at 13:49-50, *id.* at 13:54-56. In one embodiment, the '101 patent describes that “[t]he power amplifier bias block 50 and the power amplifier 32 can be integrated on a single die with one or more other components to form a packaged power amplifier module, which can be, for example, mounted to a RF circuit board associated” *Id.* at 9:8-12. However, the '101 patent also explains that “the packaged power amplifier module 300 can also include one or more packaging structures” where the packaging structures include “the components and die(s) disposed thereon.” *Id.* at 14:35-41.

56. I have summarized the relevant portions of the file history for my opinions in the “current mirror” section of my declaration below.

VIII. OPINIONS ON CLAIM CONSTRUCTION

A. “current mirror” (’101 patent claims 1, 2, 10, 11, 17, 18, 20, 21, 22)

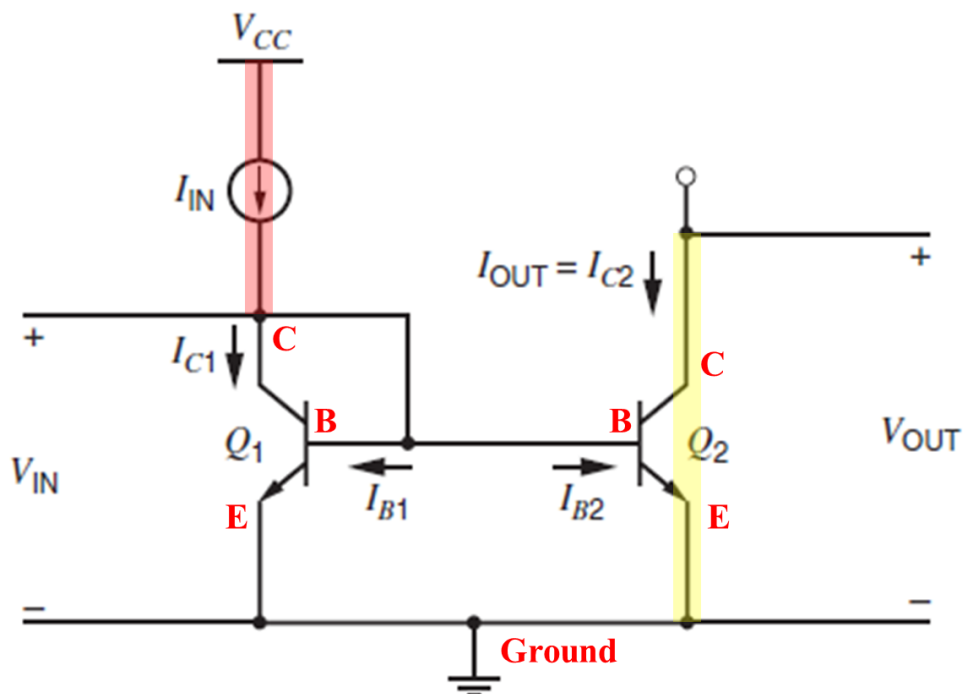
Complainants	Respondents	Staff
Plain meaning, which is “one or more circuits configured to mirror a current, which can be configured to achieve a target gain, having at least two transistors with their base or gate terminals tied together”	Plain meaning, such as “one or more circuits configured to mirror a current, which can be configured to achieve a target gain”	Plain meaning, such as “one or more circuits configured to mirror a current, which can be configured to achieve a target gain”

57. Complainants, Respondents, and Staff agree that a “current mirror” comprises “one or more circuits configured to mirror a current, which can be configured to achieve a target gain” Complainants’ proposed construction also requires that a “current mirror” “has[] at least two transistors with their base or gate terminals tied together.” This requirement of Complainants’ proposed construction is consistent with the claim language, specification, prosecution history, and extrinsic evidence.

58. Before addressing the requirement that a “current mirror” “has[] at least two transistors with their base or gate terminals tied together,” I will address the requirement—agreed upon by all parties—that a “current mirror” “can be configured to achieve a target gain.” This is set forth in the ’101 specification and extrinsic evidence. For example, the ’101 specification states that as “used herein, the term **current mirror** can refer to current amplification circuits including a plurality of current mirrors combined (e.g., cascaded) **to achieve a target gain.**” JXM-0001 (’101 patent) at 11:42-45 (emphasis added); *see also id.* at

11:39 (“any suitable gain”); *id.* at 10:62-66 (any “suitable magnitude”). This too is confirmed by the ’101 patent, which explains that the “target gain” can be “*any suitable gain*” and can have *any “suitable magnitude.”* See *id.* at 11:39, 10:62-66. The ’101 specification uses the terms “current mirror” and “current amplifier” interchangeably, referring to “current mirror 83” and current “amplifier 83.” JXM-0001 (’101 patent), col. 10:62-65; *id.* at Fig. 5. specification, that a current mirror can have a gain of unity or greater than unity.

59. A person of ordinary skill in the art would understand that such a “target gain” could be a gain of 1 or greater, or even less than one. A person of ordinary skill in the art would understand, either in or outside the context of the ’101 patent, that it is common to use a current mirror with unity gain. For example, I described the simple current mirror from CXM-0001 set forth below.



CXM-0001 at 253, Fig. 4.2. I also explained in the background section how this current mirror has unity gain when the transistors Q_1 and Q_2 are sized the same.

60. CXM-0001 also explains that “[i]deally, the output current is equal to the input current multiplied by a desired current gain. If the gain is unity, the input current is reflected to the output, leading to the name *current mirror*.” CMX-0001 at 251 (italics original). This means that the input current can be multiplied by a unity gain factor (i.e., by “1”) to produce an output current that matches the input current. It is common in the art to use current mirrors with unity gain (i.e., have a gain equal to 1). For example, RXM-0002 describes a current mirror that forces the “current in one side of the circuit” to be “identical to the current in the other side of the circuit,” meaning it achieves unity gain. RXM-0002 at 110; *see also* CMX-0001 at 253 (“If the transistors are identical, $I_{S1} = I_{S2}$ and (4.2) shows that the current flowing in the collector of Q_1 is mirrored at the collector of Q_2 ,” which is unity gain); *id.* at 827 (“We choose M_{25} to be matched to M_5 , so they form a unity-gain current mirror.”); SMX-0001 (defining a “current mirror” as a “circuit in which the current on one side is forced to be a replica of that of the other side....”). In sum, a “current mirror” can achieve a target gain that is unity, greater than unity, or even less than unity.

61. I will now turn to the requirement of Complainants’ proposed construction that a “current mirror” “has[] at least two transistors with their base or gate terminals tied together.”

Specification

62. The ’101 specification describes a “current mirror” as comprising at least two transistors with their base or gate terminals tied together. This is shown in Figure 5 (one part of which is shown below), which depicts two “current mirrors.” The bases of bipolar transistors 87 and 88 are connected by the trace highlighted in blue, and the bases of bipolar transistors 85 and 86 are connected by the trace highlighted in yellow.

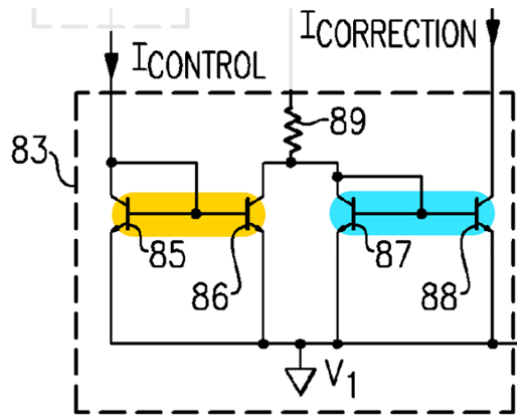


FIG.5

JXM-0001 ('101 patent) at 10:62-11:27, Fig. 5.

63. The '101 specification also sets forth that the bases of these transistors are tied together. *See id.*, at 1:65-2:7 (a “current mirror” is formed from “a first bipolar transistor and a second bipolar transistor” having a signal line “electrically connected to a base of the first bipolar transistor and to a base of the second bipolar transistor.”); *id.* at 11:10-15 (“The first NPN bipolar transistor 85 includes ... a base and a collector electrically connected to a base of the second NPN bipolar transistor 86”); *id.* at 2:7-15 (“a third bipolar transistor” and “a fourth bipolar transistor” where “a base of the third bipolar transistor” is electrically connected “to a base of the fourth bipolar transistor.”); *id.* at 11:16-21 (“a base and a collector of the third NPN bipolar transistor 87” as “electrically connected ... to a base of the fourth NPN bipolar transistor 88”).

64. Based on the disclosure of the '101 specification, a person of ordinary skill in the art would know—consistent with the plain meaning of a “current mirror” to a person of ordinary skill in the art—that the claimed “current mirror” has “at least two transistors with their base or gate terminals tied together.” Furthermore, there are countless variations of the two-transistor current mirror. In these variations, the two-transistor structure of the current mirror is apparent

File History

65. I understand that the file history can also be relevant to claim construction. The prosecution of the '101 patent makes clear that a “current mirror” must include at least two transistors, consistent with the plain meaning of the term to a person of ordinary skill in the art.

Id. at Skyworks_ITC_000023210; *id.* at Alon (Skyworks_ITC_000023309-320), Fig. 2 (partial). Alon's device 204 is a single transistor (a FET, or field effect transistor) that had its gate driven at 207 (blue). *Id.* at Alon (Skyworks_ITC_000023309-320), Fig. 2, col. 5:48-53. The Patent Office stated that dependent application claim 21—which depended from application claim 18—“would be allowable if rewritten in independent form[.]” *Id.*, 8/2/13 Office Action at Skyworks_ITC_000023211. This claim required, “wherein amplifying the control current further includes amplifying the control current using a current mirror of the current amplifier.” *Id.*, Application at Skyworks_ITC_000023158. Skyworks responded by amending what became issued claims 1, 17, and 21 of the '101 patent to require a current mirror type of current amplifier, for example by amending application claim 18 to require “amplifying the control current using a current mirror of a current amplifier to generate a correction current[.]” JXM-0004 ('101 File History), 10/31/13 Amendment at Skyworks_ITC_000023226 (underlining in original).

67. The Patent Office allowed the '101 claims as amended in a Notice of Allowability dated December 24, 2013. *Id.*, Notice of Allowability at Skyworks_ITC_000023242-45. Explaining reasons for allowance, the Patent Office explained that the “prior art of record [e.g., Alon] considered individually or in combination, fails to fairly teach or suggest the claimed circuit comprising ... ‘...the current amplifier including a current mirror’ structurally and functionally interconnected with other limitations in the manner as cited in the claim.” *Id.*, Notice of Allowability at Skyworks_ITC_000023244-45 (emphasis in original).

68. This prosecution history makes clear that the claimed current mirror requires at least two transistors—consistent with Complainants’ proposed construction, and not merely a single transistor.

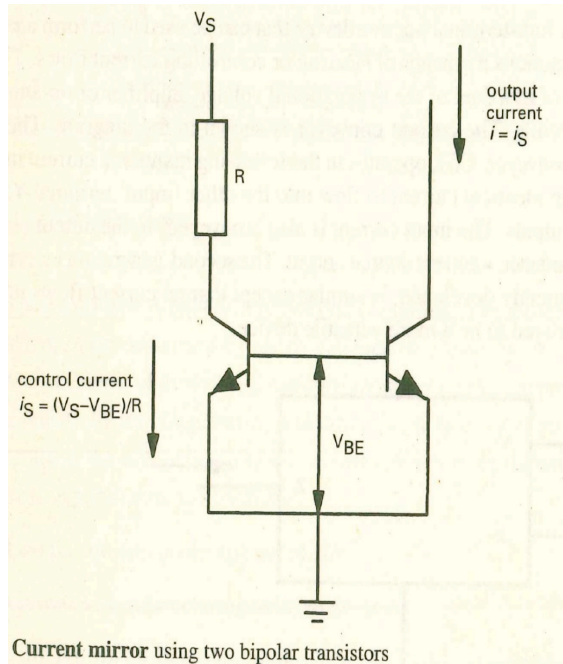
Extrinsic Evidence

69. This extrinsic evidence consistently describes a “current mirror” as having at least two transistors with their base terminals (for bipolar transistors) or gate terminals (MOS transistors) tied together. As a person of ordinary skill in the art knows, a bipolar transistor has a base terminal, whereas a MOS transistor has a gate terminal.

70. As an example, SMX-0001 is a dictionary that defines a “current mirror” as “[a] circuit in which the current on one side is forced to be a replica of that of the other side” which is “[a]ccomplished, for instance, by the bases and emitters of two bipolar junction transistors being connected together.” SMX-0001 at 159. The reference to bipolar transistors means that the base terminals are connected, but for a current mirror made from MOS transistors, the gate terminals would be tied together.

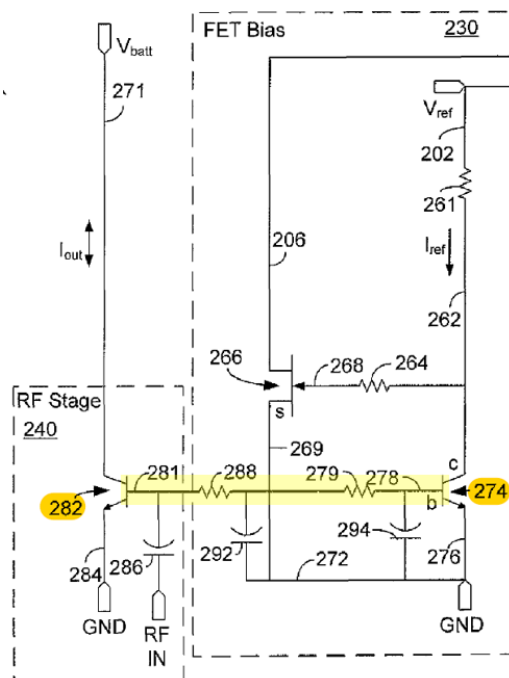
71. I described in the technical background section that CXM-0001 consistently describes and shows a current mirror having at least two transistors with their base or gate terminals tied together. In each case, whether using bipolar or MOS transistors, the key attribute of a “current mirror” is that it has at least two transistors with their base terminals (bipolar) or gate terminals (MOS) tied together. There are a wide variety of types of current mirrors. The key attribute of these current mirrors is that the base or gate terminals of the two transistors of the current mirror are tied together. There are a number of ways that the gates/bases of the two transistors can be tied together, but this is an important feature of a current mirror.

72. RXM-0002, another technical dictionary, also shows a current mirror with its base terminals tied together.



RXM-0002 at 110. This dictionary states that a “current mirror” (1) forces the “current in one side of the circuit” to be “identical to the current in the other side of the circuit” (i.e., a gain of 1, or unity gain), (2) states that the “simplest current mirror comprises just two transistors” (not only one as Respondents suggests), and (3) states that “the bases ... of the two transistors are connected together.” *Id.*

73. The Alon reference cited during the '101 patent's prosecution also discloses a “current mirror” (although not cited during prosecution) formed by at least two transistors having their bases or gates tied together. This is shown in Figure 2 below.



JXM-0004 (Alon in '101 File History), Fig. 2 (partial) and col. 7:22-25 (“transistor 274” and “transistor 282” form a “current mirror”).¹

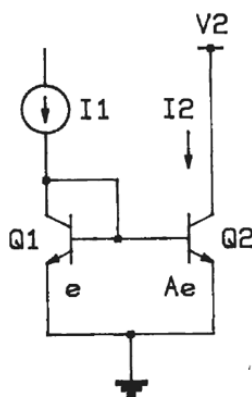
74. I understand that Respondents rely on RXM-0005, apparently to contend that a current mirror can be made from a single BJT transistor. RXM-0005 at 242-243. This is inconsistent with how a person of ordinary skill in the art would understand the term “current mirror.” RXM-0005 even admits this, by referring to “practical objection(s)” to this definition, and referring to the use of a single transistor as a mirror as a “proposal,” citing the following reasons: “Of course, the practical objection to this proposal is that the mirror ratio, M , is much higher than generally needed and poorly-controlled, being just the common-emitter current-gain, J_3 , and not very linear.” *Id.* at 242. Furthermore, RXM-0005 states that “Uncontrolled mirrors of this sort are rarely used.” *Id.* at 244. Therefore, a person of ordinary skill in the art would

¹ There is an error in this figure from Alon. Trace 269 should be connected between resistors 288 and 279, which would then form a current mirror.

describe the single transistor from RXM-0005 as simply having the current gain, β , of a bipolar transistor, and not as a current mirror.

75. Respondents' contention is also inconsistent with the '101 patent prosecution history I described above. As I described, the Patent Office found that Alon's single transistor was not a current mirror type of current amplifier, meaning that a single transistor should not be considered a current mirror.

76. Respondents' RXM-0005 also defines a "classical ... current mirror" consistent with the requirement that a current mirror has at least two transistors with their base terminals tied together (for RXM-0005, transistors Q1 and Q2).



(a)

**Figure 6.7 The classical NPN current mirror (a),
emitter degeneration (b).**

RXM-0005 at 251, Fig. 6.7(a). RXM-0005 goes on to call this "The basic NPN current mirror (Figure 6.7a) is the simple theme from which endless variations and transformations can be spun." *Id.* at 251. RXM-0005 further describes that "much has been written about this circuit in the many fine standard texts." *Id.* at 251.

B. “amplifying the control current using a current mirror of a current amplifier to generate a correction current” (’101 patent claims 17, 18, 20)

Complainants	Respondents	Staff
Plain meaning, which is “achieving a target gain of a control current, using a current mirror of a current amplifier, to generate a correction current”	Plain meaning, such as “increasing the control current using a current mirror of a current amplifier to generate a correction current	Plain meaning, such as “increasing the control current using a current mirror of a current amplifier to generate a correction current”

77. Respondents and Staff contend that the “amplifying the control current using a current mirror of a current amplifier ...” term requires “increasing” the control current to generate the correction current. I do not agree. Instead, consistent with Complainants’ proposed construction, this claim term requires only “achieving a target gain,” which is consistent with how a person of ordinary skill in the art would interpret this claim term.

Claim Language and File History

78. The claim language requires the use of “a current mirror of a current amplifier” for this claim step. This means that the “current amplifier” that performs the act of “amplifying the control current ... to generate a correction current” must be a “current mirror of a current amplifier.” JXM-0001 (’101 patent) at claim 17. I also understand that all the parties agree that a “current mirror” “can be configured to achieve a target gain” and need not “increase” the control current.

79. This requirement that the “current amplifier” in the claim is a “current mirror” type of current amplifier is confirmed by the prosecution history, which I described above in connection with the “current mirror” claim term. In short, in allowing application claim 18 over the prior art, the Patent Office confirmed that the claimed “current amplifier” is a “current mirror” type of amplifier. This further confirms that the claimed step of “amplifying the control current using a current mirror of a current amplifier ...” does not require increasing the control

current to generate the correction current, but instead need only achieve a target gain to amplify the control current.

Specification

80. The '101 patent confirms that its current “amplifier” can have *any* “*suitable magnitude*” for its gain. JXM-0001 ('101 patent) at 10:62-66. The '101 patent also states that “[a]s used herein, the term current mirror can refer to *current amplification circuits* including a plurality of current mirrors combined (e.g., cascaded) *to achieve a target gain.*” *Id.* at 11:42-45 (emphasis added); *id.* at 11:39 (“any suitable gain”).

81. It is common in the art to achieve a target gain of unity for a current mirror (*see* “current mirror” section above), as well as for a current amplifier, as set forth below.

Extrinsic Evidence

82. To a person of ordinary skill in the art, it is common for a current amplifier or a current mirror to amplify with unity gain. I described, for instance, in the technical background section above the use of unity gain current amplifiers, and I also described the purpose of these unity gain amplifiers (as well as unity gain current mirrors). For example, CXM-0002, “Microelectronic Circuit Design,” 4th Edition, McGraw-Hill (2010), describes current amplifiers that have a gain of one (i.e., unity gain). CXM-0002 at 898-99 (“the common-base current gain is simply α_o . For the FET, α_o is exactly 1...”), Fig. 14.24, 14.25. Other references also describe unity gain amplifiers. *See* CXM-0001 at 284-85, 634 (“Compensation for unity-gain feedback operation ($f = 1$) [of a basic amplifier] is achieved ...”); *id.* at 635 (emphasis added) (“... the basic amplifier has a unity-gain bandwidth ...”); CXM-0003 at 318 (referring to “unity gain current amplifiers”); CXM-0004 at 1086-87 (“unity-gain current amplifier” and “current operation amplifier (COA)” in “unity-gain closed loop configuration”). In addition, a person of

ordinary skill in the art would understand that it is common to “amplify” with unity gain. See CXM-0005, “Control of Three Phase Power Supplies for Ultra Low THD,” by Doncker et al., APEC ’91 Sixth Annual Applied Power Electronics Conference and Exhibition (1991), which refers to “amplify with unity gain.” CXM-0005 at 624.

83. I do not agree with Respondents’ and Staff’s attempt to limit this claim term to “increasing” the control current to generate the correction current. I understand that Respondents and Staff may rely on several extrinsic evidence references that describe “amplifying” as “increasing” and that an amplifier “increases” the input to create the output. It is common for an amplifier to increase an input to generate an output, but it need not do so. I described above that it is common to have unity gain current amplifiers and to amplify using unity gain, including with a unity gain current mirror. For this reason, there is no reason a person of ordinary skill in the art would require this claim term to require increasing the input to generate the output, as Respondents and Staff attempt to do in limiting the claim to a particular type of amplifying using a current mirror type current amplifier (one that increases).

84. For research and application, unity gain current amplifiers are commonly used in the art to prevent a downstream stage of a circuit that receives the output of the current amplifier from affecting the input to the current amplifier undesirably, thus isolating the input from the output. This electrical property enables the output current from the amplifier to operate independent of the load connected to the output of the amplifier, which is the circuit connected to the amplifier’s output. A unity gain current amplifier keeps the output current at the same level as the input current, while achieving this isolation feature. Because a unity gain current amplifier has this desirable characteristic, it is a common circuit element in electronics, including integrated circuits.

C. “a current amplifier configured to amplify the control current to generate a correction current” (’101 patent claims 1, 2, 10, 11, 21, 22)

Complainants	Respondents	Staff
Plain meaning, which is “a current amplifier configured to achieve a target gain of a control current to generate a correction current”	Plain meaning, such as “a current amplifier configured to increase the control current to generate a correction current”	Plain meaning, such as “a current amplifier configured to increase the control current to generate a correction current”

85. I understand the dispute for this claim term to be the same as for the previous claim term. In particular, the dispute is whether the claimed “current amplifier configured to amplify ...” must be configured to “achieve a target gain of a control current” as Complainants contend, or is instead limited solely to current amplifiers that “increase the control current” as Respondents and Staff argue. My opinions on this term are the same as for the previous term—the claimed “current amplifier” amplifies by “achieving a target gain” and the “current amplifier” need not “increase” the input to generate the output as Respondents and Staff contend.

D. “integrated circuit” (’563 patent claims 14, 15, 17, 20)

Complainants	Respondents	Staff
Plain meaning, which is “a circuit made up of multiple interconnected electronic components integrated on one or more dies”	Plain meaning, which is “a circuit made up of multiple interconnected electronic components integrated on a die”	Plain meaning, such as “a circuit made up of multiple interconnected electronic components integrated on one or more dies”

86. I understand the dispute for this term to be whether an “integrated circuit” can be “integrated on one or more dies” as Staff and Complainants contend, or whether it must be “integrated on a [single] die” as Respondents argue. A person of ordinary skill in the art would understand that an “integrated circuit” can be “integrated on one or more dies.”

Specification

87. The '563 specification describes that the “packaged power amplifier module 300 includes an *IC or die* 301.” JXM-0002 ('563 patent) (emphasis added) at 14:15-16. This means that the integrated circuit (IC) need not be on a single die in the '563 specification. The specification also states that the its amplifier module can be implemented in “dies” (plural). *Id.* at 14:66-15:2 (emphasis added) (module “formed over the packaging substrate 320 and the components and *die(s)* disposed thereon.”) The specification accordingly confirms to a person of ordinary skill in the art that an “integrated circuit” can be made from “one or more dies” and is not limited to single die.

88. The specification does describe using a single die. *Id.* at 9:26-31 (“The power amplifier bias block 50 and the power amplifier 32 can be integrated on a single die with one or more other components to form a packaged power amplifier module, which can be, for example, mounted to a RF circuit board associated with the wireless device 11 of FIG. 2.”); *id.* at 11:25-30. The specification, however, uses the permissive language “can be,” not the mandatory “must be.”

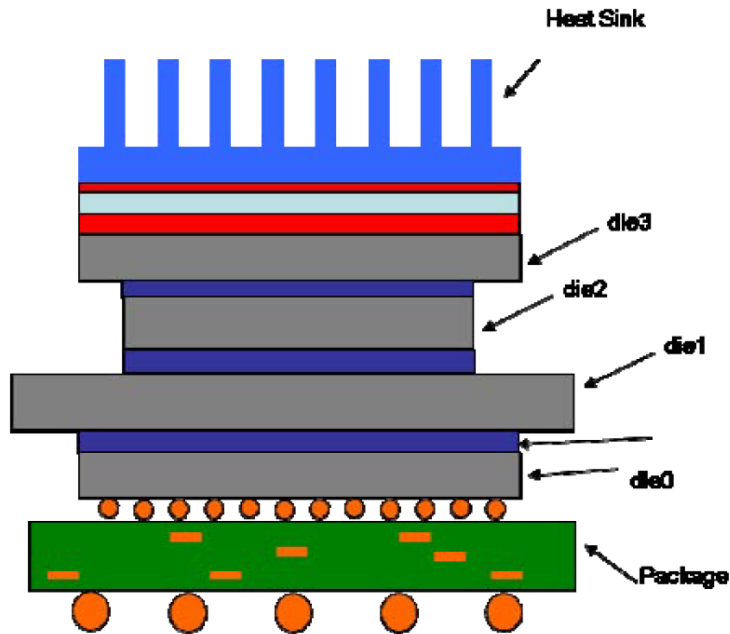
Extrinsic Evidence

89. A person of ordinary skill in the art would understand that there are multiple types of integrated circuits (ICs). As I described in the technical background section above, these types of integrated circuits include (1) monolithic integrated circuits, where a single die or piece of substrate makes up the integrated circuit, (2) multichip integrated circuits, where the circuit elements are formed on or within two or more semiconductor dies, and (3) three-dimensional integrated circuits (3D ICs), where multiple dies are stacked to form an integrated circuit. A person of ordinary skill in the art would understand that each of these types of “integrated circuits” should be included within the meaning of the claimed “integrated circuit.”

90. For example, CMX-0009, “Integrated Circuit Design, Fabrication and Test,” by P. Shepherd, McGraw-Hill (1996) describes one type of integrated circuit known to a person of ordinary skill in the art as a “monolithic IC, where ... all the components and interconnections are on the semiconductor substrate.” CMX-0009 at 1. CMX-0007, the “Authoritative Dictionary of IEEE Standards Terms,” Seventh Edition (2006), explains that a “monolithic integrated circuit” is a circuit formed on a “single piece” of substrate. CXM-0007 (IEEE Dictionary) (emphasis in original) at 708 (bolding in original, underlining added) (“**monolithic integrated circuit** An integrated circuit formed in a single piece of the substrate material.”).

91. CXM-0007 (IEEE Dictionary) also defines a “multichip integrated circuit” that has its circuit elements formed “on or within two or more semiconductor chips.” *Id.* at 712 (bolding in original, underlining added) (“**multichip integrated circuit** An integrated circuit whose elements are formed on or within two or more semiconductor chips that are separately attached to a substrate.”).

92. CMX-0008, “Thermal Characteristics of Multi-Die, Three-Dimensional Integrated Circuits with Unequally Sized Die,” by Jain, published in 2010 in an IEEE journal, describes three-dimensional integrated circuits. CXM-0008 at 1-2. This paper shows an example of a three-dimensional integrated circuit (3D IC) below.



CXM-0008 (Jain IEEE paper) at 2, Fig. 1.

93. In describing this figure, this CMX-0008 states that “Figure 1 schematically shows a multi-die 3D IC, with four unequally sized die.” *Id.* In the depicted “integrated circuit” shown in the figure above, die 0, die1, die2, and die 3 are included within the three-dimensional integrated circuit.

94. To a person of ordinary skill in the art, an “integrated circuit” can be made from one or more dies, not only a single die. Respondents’ proposed construction seeks to limit the claim to a single type of integrated circuit and to exclude other types of integrated circuits known to those of ordinary skill in the art.

95. It is possible and common to implement an integrated circuit on a single die; however, it is also common and possible to use “multichip integrated circuits” or “three-dimensional integrated circuits” that include multiple dies as part of the “integrated circuit.” Accordingly, to a person of ordinary skill in the art, the term “integrated circuit” in the ’563

patent means “a circuit made up of multiple interconnected electronic components integrated on one or more dies.”

IX. SUPPLEMENTATION

96. I reserve the right to supplement my opinions after I have had the opportunity to review further evidence that may be brought to my attention, including any critique of or comments on my declaration or alternative opinions advanced by or on behalf of Respondents.

Date: December 23, 2024



Dr. David Wentzloff

EXHIBIT A

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PROFESSIONAL EXPERIENCE

UNIVERSITY OF MICHIGAN, Ann Arbor, MI

Full Professor, with Tenure Sept. 2020 – Present
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Associate Professor, with Tenure Sept. 2013 – Aug. 2020
Assistant Professor Sept. 2007 – Aug. 2013

EVERACTIVE, Ann Arbor, MI June 2012 – Present
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MOVELLUS, Ann Arbor, MI Aug. 2013 – Present
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MASSACHUSETTS INSTITUTE OF TECHNOLOGY, Cambridge, MA Aug. 2002 – June 2007
Research Assistant – Microsystems Technology Laboratory

INTEL CORPORATION, Hillsboro, OR June 2004 – Aug. 2004
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Research Assistant – Laboratory for Electromagnetic and Electronic Systems

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TEACHING EXPERIENCE

UNIVERSITY OF MICHIGAN, Ann Arbor, MI
Lecturer – EECS496 Major Design Experience - Professionalism Winter 2022, Fall 2023, 2024
Lecturer – ENG100 Self-Driving Cars, Drones, and Beyond Winter 2019

<i>Lecturer – EECS522 Analog Integrated Circuits</i>	Winter '08-'13, '15-'16, '18, '20-'24
<i>Lecturer – EECS215 Introduction to Electronic Circuits</i>	Fall 2012, 2014, 2020
<i>Lecturer – EECS598 Advanced Topics in ICs</i>	Winter 2011, 2015
<i>Lecturer – EECS311 Electronic Circuits</i>	Fall 2008-11
<i>Lecturer – EECS413 Monolithic Amplifier Circuits</i>	Fall 2007, 2015
<i>Student Instructor – EECS 373 Design of Microprocessor-Based Systems</i>	Winter 1999

MASSACHUSETTS INSTITUTE OF TECHNOLOGY, Cambridge, MA	
<i>Teaching Assistant – 6.111 Introductory Digital Systems Laboratory</i>	Winter 2007
<i>Head Teaching Assistant – 6.002 Electronic Circuits</i>	Fall 2005

PROFESSIONAL SERVICE

1. IEEE International Solid-State Circuits Conference (ISSCC) 2020-2024
TPC Member, Wireless Subcommittee
2. IEEE Radio Frequency IC Conference (RFIC) 2013-2023
Low-Power Radios Sub-Committee Chair, Session Chair, Workshop Organizer, and TPC Member
3. IEEE International Symposium on Low-Power Electronics and Design (ISLPED) 2011-2016
TPC Member
4. IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S) 2013-2014
TPC Member
5. IEEE Conference on Ultra-Wideband (ICUWB) 2008-2010
Session Chair, TPC Member
6. Guest editor for the IEEE T-MTT, the IEEE Communications Magazine, and the Elsevier Journal of Signal Processing: Image Communication

AWARDS

1. University of Michigan Faculty Recognition Award, 2024
2. IEEE International Conference on Synthesis, Modeling, Analysis and Simulation Methods, and Applications to Circuit Design (SMACD), Best Paper Award, 2023
3. IEEE Custom Integrated Circuits Conference (CICC) 2020 Outstanding Invited Paper Award, 2020
4. ECE Innovator Award, SkyGig (role: advisor), 2018
5. Joel and Ruth Spira Excellence in Teaching Award, 2015
6. Eta Kappa Nu (HKN) Professor of the Year, 2014-2015
7. EECS Department Outstanding Achievement Award, 2015
8. ISSCC 2014 Outstanding Forum Speaker Award
9. NSF CAREER Award, 2012
10. IEEE Subthreshold Microelectronics Conference Best Paper Award, 2012
11. DAC/ISSCC Student Design Contest Award, 2011
12. Eta Kappa Nu (HKN) Professor of the Year Award, 2009-2010
13. DARPA Young Faculty Award, 2009
14. Analog Devices distinguished scholar, 2004
15. MIT Masterworks (1 of 9 annual awards for excellence in Master's research), 2002

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5. D. S. Truesdell, J. Boley, A. Wokhlu, A. Gravel, D. D. Wentzloff and B. H. Calhoun, "Modeling and Design of Cold-Start Charge Pumps for Photovoltaic Energy Harvesters," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 70, no. 11, pp. 4334-4345, Nov. 2023.
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8. A. J. Jinia, T.E. Maurer, C. A. Meert, O. V. Pakari, S. D. Clarke, H. S. Kim, D. D. Wentzloff, and S. A. Pozzi, "Prompt photofission neutron detection in depleted uranium," accepted for publication in *Physical Review Applied*, 2023.
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12. Abbas J. Jinia; Tessa E. Maurer; Christopher A. Meert; Michael Y. Hua; S. D. Clarke; Hun-Seok Kim; David D. Wentzloff; Sara A. Pozzi, "An Artificial Neural Network System for Photon-Based Active Interrogation Applications," *IEEE Access*, Vol. 9, 2021.
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15. O. Abdelatty, X. Chen, A. Alghaihab, D. Wentzloff, "Bluetooth Communication Leveraging Ultra-Low Power Radio Design," *Journal of Sensor and Actuator Networks (JSAN)*, **Featured Article**.
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2. "Millimeter-Scale Bluetooth Low Energy Transmitter With Dual Purpose Loop Antenna," Patent number 10,911,078, issued on February 2, 2021
3. "Ring oscillator based all-digital Bluetooth low energy transmitter," Patent number 10,567,154 on February 18, 2020
4. "Millimeter-Scale Bluetooth Low Energy Transmitter With Dual Purpose Loop Antenna," Patent number 10,911,078, February 2, 2021
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Pending

1. "Dual Chirp Modulation Scheme"
2. "Wake-Up Receiver For Narrowband IoT Applications"
3. "Systems And Methods For A Crystal-Less Bluetooth Low Energy Transceiver"
4. "Ultra Low Power Sensing Platform with Multimodal Radios,"
5. "Low Power High Gain Radio Frequency Amplifier For Sensor Apparatus."
6. "Quadrature Fully-Integrated Tri-Band GPS Receiver."
7. "Digital Quadrature Transmitter With Class-B I/Q Cell Sharing."

8. "A Low Power High Gain RF Amplifier Technique."
9. "Low-Power Receiver for FSK Back-Channel Embedded in 5.8GHz Wi-Fi OFDM Packets."
10. "A 12.1mW Quadrature Fully-Integrated Tri-Band GPS Receiver in 65nm CMOS."
11. "A Mixer-Last Architecture for High Efficiency Transmitters."

**UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.**

**Before the Honorable MaryJoan McNamara
Administrative Law Judge**

In the Matter of

**CERTAIN WIRELESS FRONT-END
MODULES AND DEVICES CONTAINING
THE SAME**

Investigation No. 337-TA-1413

**DECLARATION OF PETER KINGET, PH.D.
IN SUPPORT OF COMPLAINANTS' *MARKMAN* BRIEF**

I, Peter Kinget, Ph.D. declare and state as follows:

I. INTRODUCTION

1. I have been retained as an independent expert in this proceeding by complainants Skyworks Solutions, Inc., Skyworks Solutions Canada, Inc., and Skyworks Global Pte. Ltd. (collectively, “Complainants”) to provide expert opinions regarding the technology involved in this investigation as it relates to U.S. Patent 9,450,579 (the “’579 patent”), the understanding that a person of ordinary skill in the art would have had for certain claim language in the ’579 patent in view of the intrinsic and relevant extrinsic evidence, and whether certain claims read in light of the intrinsic record adequately inform a skilled artisan about the scope of the invention with reasonable certainty. The statements made herein are based on my personal knowledge, and if I am called to testify in this investigation, I could and would testify competently and truthfully with regard to them.

2. I am being compensated at my normal consulting rate of \$675 per hour. My compensation does not depend on the outcome of this matter, any testimony I may provide, and in no way affects the substance of my statements in this Declaration. I do not have any financial interest in any party to this case. If called upon, I expect to testify regarding the subject matter set forth in this declaration.

II. PROFESSIONAL BACKGROUND

3. My qualifications are stated more fully in my curriculum vitae, which is attached as Exhibit A. Below is a summary of my education, work experience, and other qualifications.

4. I received an engineering degree (*summa cum laude*) in electrical and mechanical engineering, as well as a Ph.D. (*summa cum laude* with congratulations of the jury) in electrical engineering from the Katholieke Universiteit Leuven, Belgium, in 1990 and 1996, respectively.

5. Throughout the course of my education, including my engineering and Ph.D. degrees, I was involved in the design and fabrication of analog and RF integrated circuits. As part of my PhD research, I developed RF CMOS circuits for mixers in RF transmitters.

6. After completing my Ph.D., I held multiple industry positions. From 1996 to 1999 I worked at Bell Laboratories, Lucent Technologies, in Murray Hill, New Jersey, as a Member of Technical Staff in the Design Principles Department. In that position, I worked on RF integrated circuits for communication applications, including voltage-controlled oscillators using on-chip spiral inductors. From 1999 to 2002, I held various technical and management positions in IC design and development at Broadcom, CeLight and MultiLink. While at Broadcom, I participated in the design of a highly integrated RF receiver (a.k.a. tuner) chip for cable modem applications.

7. In 2002, I joined the faculty of the Department of Electrical Engineering, Columbia University in New York, where I am currently the Bernard J. Lechner Professor of Electrical Engineering. From 2017-2020, I served as Department Chair for the Department of Electrical Engineering.

8. My current research interests include the design of analog, RF and power integrated circuits, the design of ultra-low voltage and ultra-low power analog and RF circuits, and the efficient implementation of next-G wireless communication systems including multi-antenna, cognitive radio, ultra-wideband pulse radio. I have published papers in journals and presented my work at conferences, and I have co-authored 3 books. I hold 41 US patents with

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several applications under review. My research group has received funding from the National Science Foundation, the Semiconductor Research Corporation, Department of Energy (ARPA-E), Department of Defense (DARPA), and an IBM Faculty Award. It has further received in-kind and grant support from several of the major semiconductor companies.

9. Throughout my various work and research experiences, I have had extensive experience in the design of RF integrated circuits. With my students, I have designed RF building blocks for frequencies operating from 100MHz to 10GHz demonstrating a variety of architectural and circuit innovations. I have worked on a large variety of blocks from highly integrated receivers for the 2.4GHz band, UWB receivers and transmitters, and phase-locked loops and voltage-controlled oscillators using on-chip inductors for a wide range of frequencies and applications.

10. I was elevated to the grade of IEEE Fellow in 2011 with the citation "*for contributions to analog and radio frequency integrated circuits*". I was an elected member of the IEEE Solid-State Circuits Society Adcom, the society's governing board (2011-2013 & 2014-2016), and was a member of the Board of the Armstrong Memorial Research Foundation (2008-2018). I was also a "Distinguished Lecturer" for the IEEE Solid-State Circuits Society (2009-2010 & 2015-2017) and an Associate Editor of the IEEE Journal of Solid-State Circuits (2003-2007) and the IEEE Transactions on Circuits and Systems II (2008-2009). I served as a member of the Technical Program Committee of the IEEE Custom Integrated Circuits Conference (CICC) (2000-2005, 2016-2018), the Symposium on VLSI Circuits (2003-2006), the European Solid-State Circuits Conference (2005-2010), and the International Solid-State Circuits Conference (2005-2012).

11. In 2020, I became the inaugural recipient of the “IEEE Solid-State Circuits Society 2020 Innovative Education Award.” I am also a co-recipient of the “Best Student Paper Award - 1st Place” at the 2008 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, of the “First Prize” in the 2009 Vodafone Americas Foundation Wireless Innovation Challenge, of the "Best Student Demo Award" at the 2011 ACM Conference on Embedded Networked Sensor Systems (ACM SenSys), of the "2011 IEEE Communications Society Award for Advances in Communication" for an outstanding paper in any IEEE Communications Society publication in the past 15 years, of the "First Prize (\$100K)" in the 2012 Interdigital Innovation Challenge (I2C), of the "Best Student Paper Award - 2nd Place" at the 2015 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, of the "Best Poster Award" at the 2015 IEEE Custom Integrated Circuits Conference (CICC), and of the "Best Student Paper Award - 3rd Place" at the 2018 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium.

12. I also work as a technical consultant to industry on analog and RF integrated circuit design. In the field of RF integrated circuits, I have provided technical advice to companies on the design of RF circuits and products for cellular communications, phase-locked loops, and ultra-low power communications.

III. MATERIALS CONSIDERED

13. In preparing this declaration, I have reviewed the claims, specification, and file history of the '579 patent. I understand that the '579 patent issued from U.S. Patent Application No. 14/833,076, which was filed on August 22, 2015 and is a divisional of U.S. Patent Application No. 13/936,175, which was filed on July 6, 2013. For the purposes of this declaration, I used the July 7, 2012 provisional application filing date as the date of invention for the '579 patent.

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14. I understand that the parties to this Investigation jointly submitted a chart listing the terms from the '579 patent that are in dispute and each parties' respective construction of that claim. EDIS Doc ID. 838211. I have reviewed the parties' jointly submitted claim chart.

15. I have reviewed and understand the references and exhibits cited in this declaration, and I have reviewed all the materials that I describe in more detail below.

16. My opinions are further based on my education, training, research, knowledge, and experience.

IV. LEGAL PRINCIPLES

17. I am not an attorney. For purposes of this declaration, Complainants' counsel has informed me about certain legal principles relating to claim construction. My understanding of these legal principles is described below.

18. I understand that a claim term should be understood in the context of the claim as a whole. I also understand that the specification informs a claim term's meaning. I further understand that a claim term must be read in light of the specification.

19. I understand that claim terms are generally given their ordinary and customary meaning, which is the meaning the term would have to a person of ordinary skill in the art at the time of the claimed invention. This is ordinarily when the priority application for the patent was filed. I have assumed that the priority date for the '579 patent is July 7, 2012 for this declaration.

20. I understand that a patent specification may provide a special definition for a claim term that differs from the ordinary meaning of the claim term. In this situation, the specification's lexicography controls the claim term's meaning.

21. I understand that a patent specification may contain a disclaimer or disavowal of claim scope. Such a disclaimer or disavowal must be clear and unmistakable. I further understand that such a disclaimer or disavowal controls, even if the plain meaning of the claim term might have included the disclaimed or disavowed subject matter.

22. I understand that a patent's file history, which is also called its prosecution history, may be considered when determining the meaning of a patent's claims. In particular, an applicant's or patent owner's statements to the Patent Office characterizing its invention may give rise to prosecution disclaimer. Such a prosecution disclaimer can arise from both claim amendments and arguments made to the Patent Office, including during an *inter partes* review (IPR). I understand that prosecution disclaimer must be clear and unmistakable to a person of ordinary skill in the art. I understand that if an applicant or patent owner makes a clear and unmistakable statement during prosecution to overcome a prior art reference, prosecution disclaimer applies, even if the patentee's disclaimer may not have been necessary to overcome a rejection. If, however, statements made during prosecution are ambiguous or amenable to multiple reasonable interpretations, prosecution disclaimer does not apply.

23. I understand that the claim language, specification, and prosecution history of patent (including the record in an IPR proceeding) are referred to as "intrinsic evidence."

24. I understand that evidence external to the patent and file history is referred to as "extrinsic evidence." I also understand that extrinsic evidence may include treatises, dictionaries, and opinions of an expert in the field that may be relevant in interpreting the meaning of a claim term. I further understand that intrinsic evidence is more significant than extrinsic evidence when determining the meaning of a claim term. I understand that, in the event of an inconsistency between intrinsic and extrinsic evidence, the intrinsic evidence controls in determining the meaning of a claim term.

25. I understand that the terms in a patent claim must be definite. I understand that while terms do not need to be defined with mathematical precision in a patent, the terms of a claim must inform a person of ordinary skill in the art about the scope of the terms and the scope of the invention with reasonable certainty.

26. I understand that a patent claim is indefinite if the claim, specification, and file history fail to inform with reasonable certainty the scope of the claimed invention to a person of

ordinary skill in the art. I understand that the claims, when read in light of the specification and prosecution history, must provide objective boundaries of the meaning of claim terms to a person of ordinary skill in the art.

V. OVERVIEW OF '579 PATENT AND PROSECUTION HISTORY

27. The '579 patent is titled "Radio frequency devices having reduced intermodulation distortion" and was issued on September 20, 2016. The '579 patent issued from U.S. Patent Application No. 14/833,076, filed on August 22, 2015, claiming priority to U.S. Patent Application No. 13/936,175, filed on July 6, 2013, and which issued as U.S. Patent No. 9,148,194. The '579 patent also claims priority to U.S. Provisional Application No. 61/669,045, filed on July 7, 2012. JXM-0003 ['579 patent] at cover page.

A. '579 Specification

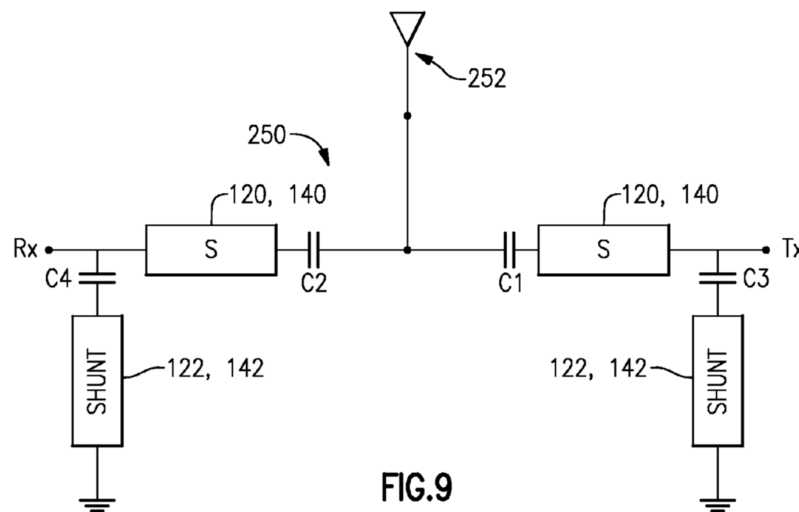
28. At a high level, the '579 patent relates to "a radio-frequency (RF) switch system" designed to reduce signal interference. JXM-0003 ['579 patent] at 1:34-37. The background of the patent explains that the transistor switches used in RF switches can be used to switch signals between one or more poles and one or more throws and that these switches can be controlled through transistor biasing or coupling. *Id.* at 1:24-28. The specification goes on to state that the use of biasing and coupling circuits with "RF switches can affect switching performance." *Id.* at 28-30.

29. More particularly, the '579 patent explains that "mixing products from other RF signals" can cause "an unwanted signal [to be] added to a desired signal" and that "[s]uch an effect can be particularly dominant in a multi-mode, multi-band environment." *Id.* at 9:2-5. The '579 patent refers to the amount of interference by the unwanted signal as "intermodulation distortion," or "IMD," and notes that it can "yield frequencies that are not harmonic

frequencies.” *Id.* at 9:5-7. The ’579 patent explains that this is problematic because it “can contribute to the introduction of spurious signals into the RF system, thereby contributing to degradation of overall RF system linearity and IMD performance.” *Id.* at 6:49-53.

30. The ’579 patent sets forth that it addresses this problem, in part, through an RF switch system that “includes a switch having a stack of field-effect transistors (FETs) connected in series between first and second nodes” and “a capacitor connected in series with the switch configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.” *Id.* at 1:34-40. According to the ’579 patent, the combination of these elements in the RF device may allow for “a low-frequency jammer signal [to] be blocked or reduced from mixing with any ON or OFF paths” (*id.* at 9:49-53), which can decrease “the overall susceptibility of a system to interference.” *Id.* at 9:9-14. Thus, the goal of the ’579 patent is to decrease signal interference by reducing or suppressing the mixing of a low-frequency blocker signal and a fundamental frequency signal, where the low-frequency blocker signal is below the band of the fundamental-frequency signal.

31. Figure 9 illustrates an embodiment of the invention.



Id. at Fig. 9.

32. The switching configuration 250 of Figure 9 can be used in a “single-pole-dual-throw (SPDT) application.” *Id.* at 9:22-23. The single pole is connected to antenna 252. *Id.* at 9:23-24. One of the throws can be connected to a receive (Rx) port via a switch circuit S (on the left of Fig. 9, near the Rx port). *Id.* at 9:24-26. Similarly, the other throw can be connected to a transmit (Tx) port via a switch circuit S (on the right of Fig. 9, near the Tx port). *Id.* at 9:28-30.

33. This configuration of Figure 9 includes “capacitors to inhibit a low-frequency blocker from mixing with a fundamental frequency.” *Id.* at 9:39-41. Each of capacitors C1 through C4 are provided between a node and a switching circuit. *Id.* at 9:41-49. “With the foregoing capacitors, a low-frequency jammer signal can be blocked or reduced from mixing with any ON or OFF paths.” *Id.* at 9:49-51. As the ’579 patent states, “[t]his can lead to improvement in IMD performance, especially for low-frequency blocker signals.” *Id.* at 9:51-53.

34. Capacitor C1, for instance, is used to inhibit a low-frequency blocker signal from mixing with the fundamental frequency signal in the switch, when the switch S just to the left of the Tx node is closed for transmission. According to the patent, this can provide “improved IMD [intermodulation distortion] performance. *Id.* at 9:64-10:3.

B. ’579 Patent Prosecution History

35. Of relevance to my opinions herein, I understand that on November 12, 2024, Respondent KCT filed a Petition for Inter Partes Review (IPR) of the ’579 patent. In this IPR petition, KCT applied the claim limitation of “inhibiting a low-frequency blocker signal from mixing with a fundamental-frequency signal in the RF switch using the first capacitor” to the prior art cited in the IPR petition. CXM-0010 [KCT ’579 IPR Petition] at 48-52.

VI. LEVEL OF ORDINARY SKILL IN THE ART

36. A person of ordinary skill in the art (POSITA) at the time of the alleged invention of the '579 patent would have had at the time of the alleged invention at least a Bachelor's Degree in Electrical Engineering or a related field and at least two years of training or additional work experience in the area of RF electronics, or a related field.

37. At the time of the alleged invention of the '579 patent, I would have qualified as a POSITA. All the opinions I express in this declaration have been made from the standpoint of a POSITA in the field of the '579 patent at the time of the invention (which I understand to be the priority date of July 7, 2012, for at least the purpose of this declaration).

VII. BACKGROUND OF THE INVENTION

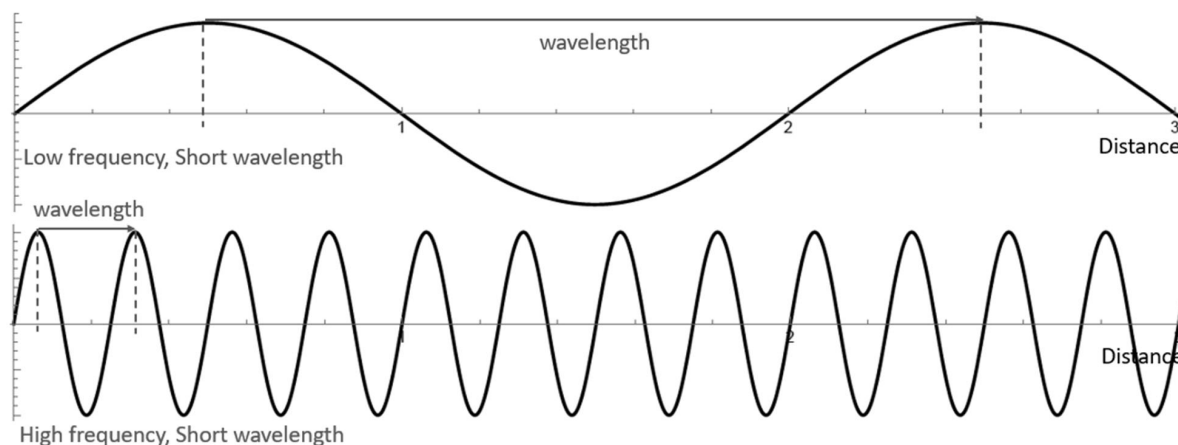
38. The '579 patent is titled "Radio Frequency Devices Having Reduced Intermodulation Distortion." The abstract, background, and summary generally describe "a radio-frequency (RF) switch system" including transistors and capacitors on a semiconductor substrate and configured in such a way as to improve RF device performance.

C. Radio Frequency Communications

39. Radio frequency (RF) circuits are essential for wireless communication systems, such as Wi-Fi devices, mobile phones, Bluetooth communications, and satellite communications. In wireless devices such as cell phones and wireless routers, radio frequency circuits work in conjunction with the analog and digital signal processing components to send wireless signals from a wireless device and receive wireless signals from other wireless devices.

40. Radio waves are a type of electromagnetic radiation that is used to convey signals in modern wireless communication systems. Two parameters characterize RF waves: frequency and wavelength. The figure below depicts two RF signals to illustrate the concepts of frequency

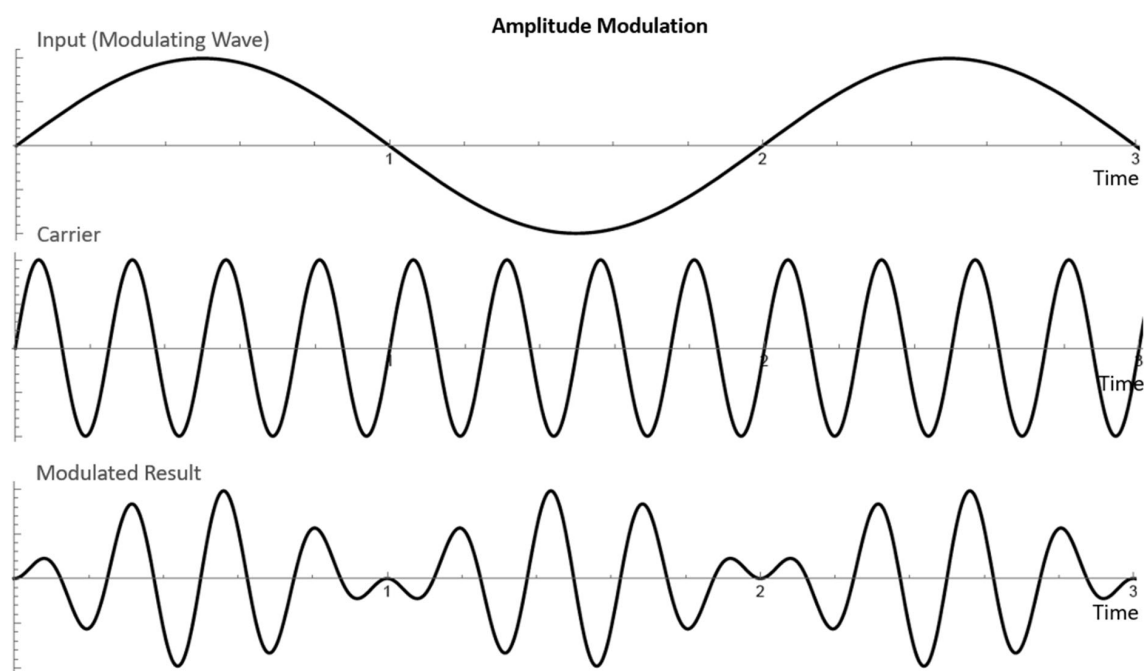
and wavelength.



41. As shown in the figure above, wavelength is the distance between identical points of two consecutive waves. For example, wavelength can be found by measuring the distance between the crests of two consecutive waves. Frequency is the number of cycles (or wavelengths) per unit time and is commonly measured in Hertz (Hz), which is the number of cycles per second. A higher frequency results in a shorter wavelength, and a lower frequency results in a longer wavelength, as shown in the figure above.

42. Radio waves are used to convey signals in wireless communications. However, waves carrying information (the input signals) cannot directly travel to their destination because very large antennas would be required. To save power and cost, communication systems use carrier waves to assist in transmitting information. A carrier wave is a wave having a generally constant frequency upon which an underlying signal is modulated to carry information. A carrier wave does not itself contain the desired information for transmission or reception, but is instead used to convey the underlying information. To add an intended input signal for transmission to a carrier wave, the input signal is transferred onto the carrier wave. This process is called modulation. The input signal can be transferred by, for example, changing the amplitude of the

carrier wave (amplitude modulation) or the frequency of the carrier wave (frequency modulation). An example of amplitude modulation of a carrier wave is shown in the figures below. The top figure shows an input signal and the middle figure shows a carrier wave. The resulting modulated RF signal has an amplitude of varying height corresponding to the amplitude of the input signal. The modulation process is reversed at the reception side for an RF signal in a process called demodulation.



43. At any given time, thousands of radio frequencies are being used around the world. To avoid interference, signals are transmitted on different frequency bands (essentially defined by the carrier frequency). In the United States, these frequency bands are assigned by the Federal Communications Commission. Radio frequency circuits are designed to operate in their intended frequency bands, which are certain ranges of frequency within the frequency spectrum, generally ranging from 3 kHz to 300 GHz.

D. Fundamental Frequency

44. The primary design goal of a radio frequency circuit is to handle RF signals with carrier frequencies that are within an intended frequency band. A fundamental frequency is within this intended frequency band. For example, a frequency band close to 2.4 GHz is used for Wi-Fi (hence the term 2.4 GHz Wi-Fi), as is a frequency band close to 5 GHz (hence the term 5 GHz Wi-Fi).

45. The frequency of a particular carrier wave and its sidebands around it that carry the underlying information need to lie within the frequency band. For example, for the 5 GHz Wi-Fi band the carrier with its sidebands have to be between 5.15 GHz to 5.85 GHz—that is, there is a 700 MHz frequency band available that is commonly referred to as the 5 GHz band. The lower end of this frequency band is 5.15 GHz, and the upper end of this frequency band is 5.85 GHz. For the 2.4GHz Wi-Fi band, the lower end of the frequency band is 2.41 GHz and the upper end is 2.47 GHz.

46. Each frequency band presents unique design challenges, such as noise management, impedance matching, and power efficiency. These design challenges require customized design approaches to optimize performance.

E. Interference

47. Radio frequency circuits operate in complex physical environments. Wireless communication channels experience noise, interference, and other disturbances over a wide range of frequencies. These unwanted RF signals can come from a variety of sources. For example, signals produced by surrounding RF transmitters at the same frequency can cause interference. External noise can creep into the radio frequency circuit and mix with a transmitted signal to produce unwanted frequencies. Therefore, an important design goal of radio frequency

circuits is to reduce the impact of interference. When unchecked, such noise and interference will degrade performance levels, such as reducing the signal-to-noise ratio (SNR) and sensitivity to detect weak signals and increasing the bit error ratio (BER), or corrupting the quality of transmitted signals. To mitigate impacts of unwanted frequencies, filters are often utilized to reduce or filter out unwanted frequencies.

48. An important characteristic of the quality of an RF device is linearity. Linearity refers to the ability of the RF device to create an output signal that is directly proportional to the input signal and to satisfy the superposition principle: the output to a sum of inputs is equal to the sum of the outputs to the individual inputs. Linearity is important to achieve high quality signal transmission and reception. Non-linearity refers to a non-proportional change between the output signal and the input signals that creates distortion. Non-linearity degrades signal quality.

49. When unwanted signals mix with a desired signal in an RF circuit, nonlinearities in RF circuit components can generate undesired harmonics and intermodulation products.

F. Radio Frequency Front-End Modules

50. A radio frequency front-end module (FEM) is a critical component in a wireless communication system. It is designed to manage the transmission and reception of RF signals between the antenna and the rest of the system. RF FEMs usually handle key functions such as amplification, filtering, and switching signals to ensure optimal system performance. An RF FEM typically includes an RF switch that allows for transmission and reception of signals.

VIII. OPINIONS ON CLAIM CONSTRUCTION

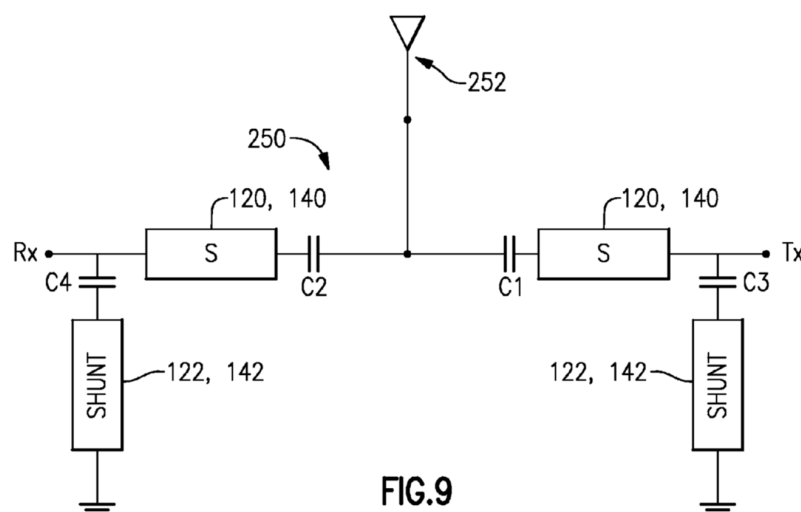
A. “inhibiting” (Claim 7)

Complainants’ Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction

Plain meaning, which is “suppressing or reducing” This term is not indefinite.	Indefinite.	Plain meaning, which is “suppressing or reducing” This term is not indefinite.
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51. A person of ordinary skill in the art would have understood the meaning of the claim term “inhibiting” in the context of claim 7 and the ’579 specification to be “reducing or suppressing.” I understand that Respondents contend that the term “inhibiting” is indefinite, rendering the claim invalid. In my opinion, claim 7, the ’579 specification, and the file history inform with reasonable certainty the scope of the claimed invention to a person of ordinary skill in the art, and this claim term is therefore not indefinite.

52. Claim 7 recites the term “inhibiting” in the context of the following claim element: “*inhibiting* a low-frequency blocker signal from mixing with a fundamental-frequency signal in the RF switch using the first capacitor.” JXM-0003 [’579 patent] at 13:29-48 (claim 7) (emphasis added). In the disclosed embodiment of Figure 9, the “first capacitor” used for this “inhibiting ...” step is capacitor C1.



Id. at Fig. 9.

53. In the context of claim 7, the “first capacitor” C1 of Figure 9’s embodiment is used to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the RF switch. For example, the ’579 patent states that “with the foregoing capacitor[], a low-frequency jammer signal can be **blocked or reduced** from mixing with any [signals, such as the fundamental frequency signal].” *Id.* at 9:49-53 (emphasis added). The specification also states that “[r]adio-frequency (RF) devices are disclosed providing **reduced** intermodulation distortion,” that “it can be desirable to **reduce** susceptibility to interference within an RF system,” and that “systems can benefit significantly from RF switches having **reduced** IMDs.” *Id.* at Abstract (emphasis added), 6:42-43 (emphasis added), 9:16-18 (emphasis added). These uses of “reduce” in the context of intermodulation distortion (IMD) relate to the “inhibiting ...” step of the claim. Based on these disclosures, a person of ordinary skill in the art would understand the term “inhibiting” in claim 7 to mean “reducing” or suppressing. This is consistent with Complainants’ proposed construction.

54. The ’579 specification also discloses the inhibiting claim step in several additional sections. *See, e.g., id.* at Abstract (“capacitor configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch”); *id.* at 1:37-40 (“The system further includes a capacitor connected in series with the switch and configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.”); *id.* at 1:55-57, 2:2-4, 2:15-17, 2:36-38, 3:7-10.

55. The ’579 patent also explains that “[i]n some implementations ... the foregoing example configurations described in reference to FIGS. 9 and 10 ... can yield a number of improvements. For example, this technique can provide improved IMD [intermodulation distortion] performance by preventing a low frequency blocker signal from mixing with a

fundamental frequency.” *Id.* at 9:64-10:3 (emphasis added). This statement uses the term “preventing,” which is a different term from “inhibiting.” A person of ordinary skill in the art would understand “inhibiting” in claim 7 to mean reducing or suppressing (including fully suppressing), but not to be limited to completely “preventing.”

56. I understand that Respondent KCT filed an inter partes review (IPR) petition for the ’579 patent, a portion of which is in CXM-0010. I understand that KCT contends that certain of the ’579 patent claims are not patentable in this IPR petition. In this IPR petition, KCT and its expert applied the “inhibiting ...” claim step to the prior art that they assert in the IPR petition renders claim 7 unpatentable. *Id.* at 48-52. In doing so, KCT and its expert take the position that a person of ordinary skill in the art “understood this capacitor’s inhibition of low-frequency blocker signals from mixing with fundamental frequency signals ... to merely be a matter of design choice.” *Id.* at 51. It appears, therefore, that KCT and its expert understood the meaning of the term “inhibiting” in this IPR petition, even though Respondents—including KCT—now argue in the ITC Investigation that the term “inhibiting” is indefinite.

57. I understand that Respondents cite certain extrinsic evidence references, such as RXM-0002, RXM-0010, RXM-0011, RXM-0014, and RXM-0017, to attempt to support their position that “inhibiting” is indefinite. Regardless of what certain evidence indicates about the meaning of the term “inhibit” in different contexts, the meaning in claim 7 and the ’579 patent is reasonably certain to a person of ordinary skill in the art (and is therefore not indefinite). That meaning, as stated above, is “reducing or suppressing,” and the ’579 specification supports this meaning for the term “inhibiting.”

B. “Low Frequency” (Claim 7)

Complainants’ Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
Plain meaning, which is “below the lower edge of the band containing the fundamental frequency” This term is not indefinite.	Indefinite.	Plain meaning, which is “below the lower edge of the band containing the fundamental frequency” This term is not indefinite.

58. A person of ordinary skill in the art would have understood the meaning of the claim term “low-frequency” in the context of claim 7 and the ’579 specification to be “below the lower edge of the band containing the fundamental frequency.” I understand that Respondents contend that the term “low-frequency” is indefinite, rendering the claim invalid. In my opinion, claim 7, the ’579 specification, and the file history inform with reasonable certainty the scope of the claimed invention to a person of ordinary skill in the art, and this claim term is therefore not indefinite.

59. Claim 7 of the ’579 patent uses the term “low-frequency” as part of the claim element “inhibiting a low-frequency blocker signal from mixing with a fundamental-frequency signal in the RF switch using the first capacitor.” The step of claim 7 immediately before this claim step is “controlling an RF switch of the RF device by placing the first switch circuit in an ON state and placing the third switch circuit in an OFF state.” JXM-0003 [’579 patent] at 13:29-48 (claim 7). The claim language itself provides a reference for the term “low-frequency.” In particular, the “low-frequency” blocker signal in claim 7 is used in the context of and in relation to the claimed “fundamental-frequency signal.” *Id.* at claim 7. This plain language of claim 7 indicates to a person of ordinary skill in the art that the “low-frequency” in claim 7 is relative to

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the lower edge of the band containing the fundamental frequency, meaning that the “low-frequency” is below this band. Consistent with this claim language, a person of ordinary skill in the art would understand term “low-frequency” in the context of claim 7 and the ’579 specification to mean “below the lower edge of the band containing the fundamental frequency.”

60. As I set forth in the technical background section of this declaration, a person of ordinary skill in the art would understand what a “fundamental frequency” is. In particular, a person of ordinary skill in the art would understand a “fundamental frequency” to mean the frequency of a carrier wave that lies in a frequency band in which a wireless device operates.

61. In my opinion, therefore, a person of ordinary skill in the art would be able to ascertain the meaning and scope of the term “low-frequency” with reasonable certainty, meaning that this claim term does not render claim 7 invalid as indefinite.

62. Like the claim language, the ’579 specification uses the term “low-frequency” in relation to a “fundamental frequency.” The ’579 patent refers to a “capacitor configured to inhibit a *low-frequency* blocker signal from mixing with a *fundamental-frequency* signal in the switch” (*id.* at Abstract, emphasis added) and “a capacitor connected in series with the switch and configured to inhibit a *low-frequency* blocker signal from mixing with a *fundamental-frequency* signal in the switch”) (*id.* at 1:37-40, emphasis added). There are numerous additional references to similar language relating “low-frequency” to a “fundamental frequency” in the ’579 specification. *Id.* at 1:55-57, 2:2-4, 2:15-17, 2:36-38, 3:7-10, 9:39-41, 9:49-53, 9:67-10:3.

63. Figure 9 of the ’579 patent is set forth below.

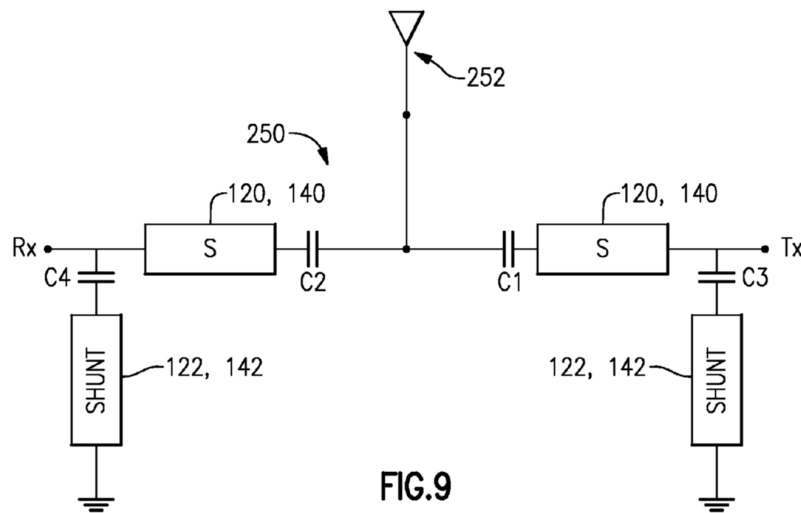


FIG.9

Id. at Fig. 9; *see id.* at 3:7-10 (“FIG. 9 shows an example where an RF switching configuration can include one or more capacitors to, for example, inhibit a low-frequency blocker from mixing with a fundamental frequency.”). Using capacitor C1 in Figure 9 “a low-frequency jammer signal can be blocked or reduced from mixing with” the fundamental frequency during transmission. *Id.* at 9:49-51. Based on the specification and claim 7 itself, a person of ordinary skill in the art would be able to ascertain the scope of “low-frequency” with reasonable certainty. As set forth above, a person of ordinary skill in the art would understand “low-frequency” in claim 7 to mean “below the lower edge of the band containing the fundamental frequency.”

64. I understand that Respondent KCT filed an inter partes review (IPR) petition for the ’579 patent, a portion of which is in CXM-0010. I understand that KCT contends that certain of the ’579 patent claims are not patentable in this IPR petition. In this IPR petition, KCT and its expert applied the “low-frequency” claim term to the prior art that they assert in the IPR petition renders claim 7 unpatentable. *Id.* at 48-52. In this IPR petition, KCT refers to “the well-known low-frequency, ‘out-of-band blocker’ signal problem.” *Id.* at 51. It appears, therefore, that KCT and its expert understood the meaning of the term “low-frequency” in this IPR petition, even

though Respondents—including KCT—now argue in the ITC Investigation that the term “low-frequency” is indefinite.

65. I understand that Respondents cite certain extrinsic evidence references, such as RXM-0002, RXM-0010, RXM-0011, RXM-0013, RXM-0014, RXM-0016, and RXM-0017, to attempt to support their position that “low-frequency” is indefinite. That “low-frequency” may be used in different contexts, as Respondents’ extrinsic evidence suggests, is not relevant to the meaning of claim 7, since claim 7 and the ’579 specification are clear that “low-frequency” is relative to, meaning at a lower frequency than, the lower edge of the band containing the fundamental frequency.

66. The meaning of “low-frequency” in the context of claim 7 of the ’579 specification to a person of ordinary skill in the art is “below the lower edge of the band containing the fundamental frequency,” and the ’579 specification and claim language supports this meaning for the term “low-frequency.” In my opinion, claim 7, the ’579 specification, and the file history inform with reasonable certainty the scope of the claimed invention to a person of ordinary skill in the art, and this claim term is therefore not indefinite.

IX. SUPPLEMENTATION

67. I reserve the right to adjust or supplement my opinions after I have had the opportunity to review further evidence or in light of additional documents that may be brought to my attention, including any critique of or comments on my declaration or alternative opinions advanced by or on behalf of Respondents.

Date: December 21, 2024



Dr. Peter Kinget

EXHIBIT A

Peter R. Kinget

Columbia University
Department of Electrical Engineering

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Research Interests:

- Design of high-performance chips for physics instrumentation, including the CERN Large Hadron Collider
- Efficient implementation of next-G wireless communications systems: radar, multi-antenna, cognitive radio, ultra-wideband pulse radio
- Design of ultra-low power electronics for Sensory and Cognitive Hardware and the Internet of Things
- Design of ultra-low voltage and ultra-low power analog and RF circuits in nanoscale CMOS technologies

Positions Held:

July 2016 – present	Bernard J. Lechner Professor of Electrical Engineering, Department of Electrical Engineering, Columbia University, New York (NY, USA).
July 2017 – June 2020	Chair of the Department of Electrical Engineering, Columbia University, New York (NY, USA).
July 2011 – June 2016	Professor, Department of Electrical Engineering, Columbia University, New York (NY, USA).
July 2014 – June 2016	Vice Chair of Faculty Affairs, Department of Electrical Engineering, Columbia University, New York (NY, USA).
July 2011 – July 2014	Director of Graduate Programs, Department of Electrical Engineering, Columbia University, New York (NY, USA).
Oct. 2012 – 2014	Founding (co-)Chair of the Smart Cities Center in the Institute for Data Sciences and Engineering, Columbia University, New York (NY, USA).
Sept. 2010 – Aug. 2011	Visiting Research Professor, Institut ICTEAM, Université Catholique de Louvain, Louvain la Neuve (Belgium).
July 2002 – June 2011	Associate Professor, Department of Electrical Engineering, Columbia University, New York (NY, USA) [Tenure July 2008].
April 2002 - June 2002	Principal Engineer at Multilink Corporation, Somerset (NJ, USA).
Sept. 2000 - Jan. 2002	Director, VLSI in the 'VLSI and Integrated Electro-optics Group' of Celight Inc., Iselin (NJ, USA).
July 1999 - August 2000	Senior Staff Scientist in the 'Analog and RF Microelectronics Group' of Broadcom Corporation, Irvine (CA, USA).
Oct. 1996 - June 1999	Member of Technical Staff (Principal Investigator) in the 'Design Principles Research Department' of the 'Wireless Laboratory' at Bell Laboratories, Lucent Technologies, Murray Hill (NJ, USA).
Sept. 1991 - Sept. 1996	Research assistant in the ESAT-MICAS laboratory of the Katholieke Universiteit Leuven, Leuven (Belgium).
Sept. 1990 - Aug. 1991	Belgian military service at the "Technical Department of the Army", Peutie (Belgium).
Spring 1998 and 2002	Adjunct Assistant Professor, Department of Electrical Engineering, Columbia University, New York (NY, USA).

Degrees:

- Sept. 1991 - May 1996 Ph.D. in Electrical Engineering from the Katholieke Universiteit Leuven (Belgium); “Summa cum laude with congratulations of the jury” (places thesis in the top 5% of all engineering Ph.D. theses); *Title* “Analog VLSI integration of parallel signal processing systems;” *Advisor* Prof. M. Steyaert; *Jury*: Profs Aernoudt (K.U. Leuven), Sansen (K.U. Leuven), Vandewalle (K.U. Leuven), De Man (IMEC/K.U. Leuven), and Jespers (U.C. Louvain).
- Oct. 1985 - July 1990 Engineering Degree (Ir.) in Electrical and Mechanical Engineering option Microelectronics from the Katholieke Universiteit Leuven, Leuven (Belgium); “Summa cum laude” (ranked in the top 3 of 360 graduating engineering students).

Honors and Distinctions:

- IEEE Solid-State Circuits Society Distinguished Lecturer [2015-2017]
- Elected Member of the IEEE Solid-State Circuits Society AdCom, the society’s governing board [2014-2016]
- Plenary speaker at the 2013 IEEE European Solid-State Circuits Conference (September 2013)
- Fellow of the IEEE [2011] “for contributions to analog and radio frequency integrated circuits”
- Elected Member of the IEEE Solid-State Circuits Society AdCom, the society’s governing board [2011-2013]
- IEEE Solid-State Circuits Society Distinguished Lecturer [2009-2010]
- Plenary speaker at the 2007 IEEE European Solid-State Circuits Conference (September 2007)
- Graduate fellowship for Ph.D. research from the National Fund for Scientific Research (NFWO) (Belgium) [1991-95]
- Fellowship for the participation to 'The Bessie Lawrence 17th International Summer Science Institute' at the Weizmann Institute of Science, Rehovot (Israel) (5 fellowships for all Belgian finishing high school students) (Summer 1985)

Awards:

- Inaugural Recipient of the “*IEEE Solid-State Circuits Society Innovative Education Award*” (Feb. 2020)
- Co-recipient of “*Best Student Paper Award – 3rd Place*” at the 2018 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium for “An 8-Element, 1-3GHz Direct Space-to-Information Converter for Rapid, Compressive-Sampling Direction-of-Arrival Finding Utilizing Pseudo-Random Antenna-Weight Modulation” (with Matt Bajor)
- Co-recipient “*Best Demo Award*” at the 2018 ACM/IEEE International Conference on the Internet of Things Design and Implementation (IoTDI) for “An Ultra-Low-Power Custom Integrated Circuit based Sound-Source Localization System” (with D. de Godoy, S. Xia, W. Fernandez, X. Jiang)
- Co-recipient “*Outstanding Student Paper – Runner up (2nd place)*” at the 2017 IEEE Custom Integrated Circuits Conference (CICC) for “A-236.3dB FoM Sub-Sampling Low-Jitter Supply-Robust Ring-Oscillator PLL for Clocking Applications with Feed-Forward Noise-Cancellation,” April 2018 (with S. Nagam)
- Co-recipient “*Best Poster Award*” at the 2015 IEEE Custom Integrated Circuits Conference (CICC) for “A Field-Programmable Noise-Canceling Wideband Receiver with High-Linearity Hybrid Class-AB-C LNTAs,” Sept. 2015 (with J. Zhu)
- Co-recipient of the “*Best Demo – Runner Up Award*” at 14th ACM Conference on Embedded Network Sensor Systems (SenSys) Nov. 2016, (with R. Chandrasekaran, D. de Godoy, S. Xia, M. Islam, B. Islam, S. Nirjon, and X. Jiang)
- Co-recipient of “*Best Student Paper Award – 2nd Place*” at the 2015 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium (with Yang Xu)
- Co-recipient of the “*Student Poster Award 2nd Place*” for “Metacapacitor: Large Area, Low Cost, High Performance Capacitors for Power Electronics,” FlexTech Alliance Conference, Feb. 2014

(with S. Yang, B. Van Tassell, C. Le, S. Liu, E. S. Leland, D. A. Steingart, S. O'Brien, and I. Kymissis)

- Co-recipient of the “*First Prize (\$100K) in the 2012 Interdigital Innovation Challenge (I2C)*” for “Ultrasonic Wireless Sensors” (with K. Yadav and I. Kymissis)
- Co-recipient of the “*2011 IEEE Communications Society Award for Advances in Communication*” for an outstanding paper published in any IEEE Communications Society publication in the previous 15 years for the paper entitled “Energy-Harvesting Active Networked Tags (EnHANTs) for Ubiquitous Object Networking,” (with M. Gorlatova, I. Kymissis, D. Rubenstein, X. Wang and G. Zussman)
- Co-recipient of the “*Best Student Demo Award*” for “Demo: Organic Solar Cell-equipped Energy Harvesting Active Networked Tag (EnHANT) Prototypes” at the ACM Conference on Embedded Networked Sensor Systems (ACM SenSys) 2011 (with G. Stanje, P. Miller, J. Zhu, A. Smith, O. Winn, R. Margolies, M. Gorlatova, J. Sarik, M. Szczodrak, B. Vigraham, L. Carloni, I. Kymissis, and G. Zussman)
- Co-recipient of the “*First Prize in the 2009 Vodafone Americas Foundation Wireless Innovation Challenge*” for “Active Networked Tags for Disaster Recovery Applications” (with G. Zussman, I. Kymissis, D. Rubenstein and X. Wang)
- Co-recipient of “*Best Student Paper Award – 1st Place*” at the 2008 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium (with F. Zhang and R. Gharpurey).
- *IBM Faculty Award* (March 2005)
- Award for the ‘*Best Engineering thesis of Applied Sciences for the class of 1990*’ (1 award among 360 students) at the Katholieke Universiteit Leuven (Belgium) granted by the class of 1965 (Oct. 1990).

Awards & Honors of Student Advisees:

- M.S./Ph.D. student Hongzhe Jiang received the “Armstrong Award for MS students” awarded to one M.S. student per year by the Electrical Engineering Department at Columbia University in May 2023.
- Ph.D. student Petar Barac was the recipient of a “Millman Teaching Assistant Award” from the Electrical Engineering Department at Columbia University in May 2023 for his exemplary service as a teaching assistant.
- Ph.D. student Petar Barac was the recipient of the “Graduate Service Award” from the Electrical Engineering Department at Columbia University in May 2023.
- Ph.D. student Rui (Ray) Xu received a NASA Graduate Research Fellowship for his research “Using SONOS Transistors as Radiation Detectors” for academic year 2022-2023.
- Ph.D. student Subhajit Ray received a 2023 SSCS Predoctoral Achievement Award. Twenty five awards were awarded in 2023 among a slate of international applicants.
- Ph.D. student Zhaowen Wang received the “Electrical Engineering Collaborative Research Award” at Columbia University for his research on Efficient and High-Performance Clocking Circuits for High-Speed Data Links in May 2022.
- Ph.D. student Zhaowen Wang received a 2022 SSCS Predoctoral Achievement Award. Twenty-five awards were awarded in 2022 among a slate of international applicants.
- Ph.D. student Guoxiang Han was the recipient of a “Millman Teaching Assistant Award” from the Electrical Engineering Department at Columbia University for his exemplary service as a teaching assistant in May 2020.
- Ph.D. student Sarthak Kalani received the “Electrical Engineering Collaborative Research Award” at Columbia University for his research on High Dynamic Range ADCs for the CERN LHC in collaboration with the Columbia Physics Nevis Laboratory in May 2019.
- Ph.D. student Guoxiang Han was the recipient of a “Millman Teaching Assistant Award” from the Electrical Engineering Department at Columbia University for her exemplary service as a teaching assistant in May 2019.
- M.S./Ph.D. student Zhaowen Wang received an “EE MS Award of Excellence” for his outstanding academic performance during his MS studies at the Electrical Engineering Department at Columbia University in May 2019.

- Ph.D. student Jianxun Zhu received the "Electrical Engineering Collaborative Research Award" at Columbia University for his research on Frequency-Translational Quadrature-Hybrid Receivers in May 2017.
- Ph.D. student Guoxiang Han was the recipient of a "Millman Teaching Assistant Award" from the Electrical Engineering Department at Columbia University for her exemplary service as a teaching assistant in May 2017.
- M.S./Ph.D. student Guoxiang Han received the "Armstrong Award for MS students" awarded to one M.S. student per year by the Electrical Engineering Department at Columbia University in May 2017.
- Ph.D. student Rabia Tugce Yazicigil received the "Electrical Engineering Collaborative Research Award" at Columbia University for her research on Compressive Sampling Rapid Interference Detection in May 2016.
- Ph.D. student Jianxun Zhu received a 2016 IEEE Solid-State Circuits Society Predoctoral Achievement Award. Ten awards were awarded in 2016 among a slate of international applicants.
- Ph.D. student Rabia Tugce Yazicigil was selected among the top 60 female graduate students and postdoctoral scholars nationwide to participate in the 2015 MIT Rising Stars in Electrical Engineering Computer Science and give an oral presentation on her research "Enabling Cognitive Radio Systems with Compressed-Sampling Rapid Spectrum Sensors" in November 2015.
- Ph.D. student Rabia Tugce Yazicigil won Second place at the Bell Labs Future X Days Student Research Competition in April 2015 with her research on "Enabling Cognitive Radio Systems with Compressed-Sampling Rapid Spectrum Sensors." Only 10 students were invited to present their innovative research at Bell Labs out of 50 applicants from North America.
- Ph.D. student Rabia Tugce Yazicigil was the recipient of a "Millman Teaching Assistant Award" from the Electrical Engineering Department at Columbia University for her exemplary service as a teaching assistant in May 2014.
- Ph.D. students Baradwaj Vigraham and Jayanth Kuppambatti received the "Electrical Engineering Collaborative Research Award" at Columbia University for their research on Switched Mode Analog Circuits in May 2014.
- M.S./Ph.D. student Jianxun Zhu received an "EE MS Award of Excellence" for his outstanding academic performance during his MS studies at the Electrical Engineering Department at Columbia University in May 2012.
- M.S./Ph.D. student Chengrui Le received the "Armstrong Award for MS students" awarded to one M.S. student per year by the Electrical Engineering Department at Columbia University in May 2011.
- M.S./Ph.D. student Baradwaj Vigraham received the "Armstrong Award for MS students" awarded to one M.S. student per year by the Electrical Engineering Department at Columbia University in May 2010.
- B.S. research project student Jiasi Chen received the undergraduate "Electrical Engineering Department Research Award" at Columbia University in May 2010.
- Ph.D. student Frank Zhang received the 2009 Jury Award from the Electrical Engineering Department of Columbia University for his Ph.D. thesis "Ultra-Wideband Pulse Radio Receivers in Digital CMOS". The Jury Award was established in 1991 for outstanding achievement by a graduate student in the areas of system communication or signal processing.
- Ph.D. Student Shih-An Yu received a IEEE 2008 Solid-State Circuits Society Predoctoral Fellowship. Only two fellowships were awarded in 2008 among a slate of international applicants.
- Ph.D. Student Frank Zhang received the "Millman Teaching Assistant Award" from the Electrical Engineering Department of Columbia University for his exemplary service as a teaching assistant in Fall 2005.

Professional Activities and Service:

- Member of the 2021 IEEE Donald O. Pederson Award in Solid-State Circuits Committee – the most distinguished award in solid-state circuits [2019-2022].
- Member of the Academic panel that reviewed the rehabilitation for Canarsie Tunnel on the L subway line for the MTA and NY Governor (Dec. 2018 – 2020)

- Co-founder of WiLO Networks Inc. (August 2021); startup commercializing technology developed in my group and licensed from Columbia University.
- Co-founder of Concurrent Wireless Inc. (June 2016); startup commercializing technology developed in my group and licensed from Columbia University.
- Co-founder of Seamless Devices Inc. (Nov. 2014); startup commercializing technology developed in my group and licensed from Columbia University.
- Board Member for the Armstrong Memorial Research Foundation, New York (NY, USA) [12/2008-2018].
- Member of the Technical Program Committee for the 2000-05 & 2016-2018 IEEE Custom Integrated Circuits Conference (CICC); Chairman of the wireless subcommittee 2001-04; Chair for panels & member of the organizing committee (2005).
- Co-Founder of the New York IEEE EDS/SSCS Chapter [Fall 2007]; SSCS Vice Chair [Fall 2007-Winter 2009]; Chapter Chair [Spring 2010-2011]; Treasurer [2012-2013].
- Program co-chair, “27th Symposium on Integrated Circuits and System Design” (SBCCI-2014) at ‘Chips in Aracaju’, Brazil, Sept. 2014.
- Member of the Technical Program Committee for the 2006-12 IEEE International Solid-State Circuits Conference (ISSCC).
- Member of the Technical Program Committee for the 2006-10 IEEE European Solid State Circuits Conference (ESSCIRC).
- Member of the Technical Program Committee for the 2003-06 IEEE VLSI Symposium on Circuits.
- *Grant Proposal Reviewer*: National Science Foundation, Flemish Science Foundation (Belgium), University of California MICRO program, Research Grants Council (RGC) of Hong Kong, Science Foundation Ireland.

Consulting Activities:

- Expert Witness on various patent litigation cases (under NDA).
- Jan. 2005 – 2012: Consultant, Bell Laboratories, Alcatel-Lucent, Murray Hill, NJ, USA.
- Various other consulting activities for semiconductor companies (under NDA).
- Nov. 2014 – Nov. 2017: Technical Advisor, Seamless Devices Inc., San Jose, CA, USA.
- Jan. 2017 – Dec. 2018: Technical Advisor, Concurrent Wireless Inc., New York, NY, USA.
- Jul. 2020 – May 2022: Technical Advisor, Seamless Microsystems Inc., Berkeley, CA, USA.
- Aug. 2021 – Jul. 2022: Technical Advisor, WiLO Networks Inc., CA, USA.

Journal Editor:

- Associate Editor for the IEEE Journal of Solid-State Circuits (03/2003-05/2007)
- Associate Editor for the IEEE Transactions on Circuits and Systems II (01/2008-12/2009)
- Guest Editor, IEEE Transactions on Circuits and Systems II, special issue on “Circuits and System Solutions For Nanoscale CMOS Design Challenges” (first quarter 2009)
- Associate Editor for the IEEE Open Journal of Solid-State Circuits (09/2019-02/2021)

Journal Reviewer:

- IEEE Journal of Solid-State Circuits.
- IEEE Transactions on Circuits and Systems I.
- IEEE Transactions on Circuits and Systems II.
- IEEE Transactions on Very Large Scale Integration Systems.
- IEEE Microwave and Wireless Components Letters.
- IEEE Transactions on Microwave Theory and Techniques.
- Solid-State Electronics.
- Integration, The VLSI Journal.
- Analog Integrated Circuits and Signal Processing.

Teaching:

- Spring 1998 EE6304 (M.S./Ph.D.) Advanced Electronic Circuits; topic: RF integrated circuits (adjunct professor, 13 students).
- Spring 2002 EE4303 (B.S./M.S.) Analog Integrated Circuit Design (adjunct professor, 15 students).
- Fall 2002 EE3201 (B.S.) Circuits Analysis (55 students, Eval. 3.4/5.0).
- Fall 2002 EE3081 (B.S.) Circuits Analysis Laboratory (56 students, Eval. 3.2/5.0).
- Spring 2003 EE1201 (B.S.) Introduction To Electrical Engineering (82 students, Eval. 3.8/5.0).
- Fall 2003 EE3201 (B.S.) Circuits Analysis (62 students, Eval. 4.0/5.0).
- Fall 2003 EE3081 (B.S.) Circuits Analysis Laboratory (64 students, Eval. 3.8/5.0).
- Spring 2004 EE6312 (M.S./Ph.D.) Advanced Analog Integrated Circuits (33 students, Eval. 3.8/5.0).
- Fall 2004 EE6314 (M.S./Ph.D.) Advanced Communication Circuits (11 students, Eval. 3.6/5.0).
- Spring 2005 EE6312 (M.S./Ph.D.) Advanced Analog Integrated Circuits (24 students, Eval. 3.9/5.0).
- Fall 2005 EE6314 (M.S./Ph.D.) Advanced Communication Circuits (16 students, Eval. 3.8/5.0).
- Spring 2006 EE6312 (M.S./Ph.D.) Advanced Analog Integrated Circuits (37 students, Eval. 3.6/5.0).
- Fall 2006 EE6314 (M.S./Ph.D.) Advanced Communication Circuits (17 students, Eval. 4.0/5.0).
- Fall 2007 EE6314 (M.S./Ph.D.) Advanced Communication Circuits (14 students, Eval. 4.25/5.0).
- Spring 2008 EE6312 (M.S./Ph.D.) Advanced Analog Integrated Circuits (27 students, Eval. 4.1/5.0).
- Fall 2008 EE6314 (M.S./Ph.D.) Advanced Communication Circuits (24 students, Eval. 4.14/5.0).
- Spring 2009 EE6312 (M.S./Ph.D.) Advanced Analog Integrated Circuits (25 students, Eval. 2.62/5.0).
- Fall 2009 EE6314 (M.S./Ph.D.) Advanced Communication Circuits (16 students, Eval. 3.89/5.0).
- Spring 2010 EE6901 (M.S./Ph.D.) Topics in Electrical and Computer Engineering: Advances in Phase Locked Loops (10 students, Eval. 4.2/5.0).
- Fall 2011 EE6314 (M.S./Ph.D.) Advanced Communication Circuits (14 students, Eval. 4.75/5.0).
- Spring 2012 EE6312 (M.S./Ph.D.) Advanced Analog Integrated Circuits (41 students, Eval. 4.24/5.0).
- Fall 2012 EE9303 (M.S./Ph.D.) Seminar in Electronic Circuits (Advanced Topics in IC Design) (17 students, Eval. 4.06/5.0).
- Spring 2013 EE6312 (M.S./Ph.D.) Advanced Analog Integrated Circuits (43 students, Eval. 4.61/5.0).
- Fall 2013 EE6314 (M.S./Ph.D.) Advanced Communication Circuits (25 students, Eval. 4.83/5.0).
- Spring 2014 EE6350 (M.S./Ph.D.) VLSI Design Lab (18 students, Eval. 4.43/5.0).

- Fall 2014 EE901 (M.S./Ph.D.) Topics in Electrical and Computer Engineering: Advances in Phase Locked Loops (25 students, Eval. 4.63/5.0).
- Spring 2015 EE6350 (M.S./Ph.D.) VLSI Design Lab (14 students, Eval. 5.0/5.0).
- Fall 2015 EE6314 (M.S./Ph.D.) Advanced Communication Circuits (20 students, Eval. 4.67/5.0).
- Spring 2016 EE6350 (M.S./Ph.D.) VLSI Design Lab (21 students, Eval. 4.86/5.0).
- Spring 2020 EE9303 (Ph.D.) Seminar in Electronic Circuits (Advanced Topics in IC Design) (12 students, No evaluation collected due to COVID-19).
- Fall B 2020 EE4312 (B.S./M.S.) Analog Electronic Circuits (5 students, Eval. 4.75/5.0).
- Spring 2020 EE9303 (Ph.D.) Seminar in Electronic Circuits (Advanced Topics in IC Design) (6 students, 5.0/5.0).
- Fall 2021 EE4312 (B.S./M.S.) Analog Electronic Circuits (68 students, Eval. 4.46/5.0).
- Spring 2022 EE6350 (M.S./Ph.D.) VLSI Design Lab (31 students, Eval. 4.83/5.0).
- Fall 2022 EE4312 (B.S./M.S.) Analog Electronic Circuits (75 students, Eval. 4.32/5.0).
- Spring 2023 EE6350 (M.S./Ph.D.) VLSI Design Lab (34 students, Eval. 4.90/5.0).
- Fall 2023 EE4312 (B.S./M.S.) Analog Electronic Circuits (70 students, Eval. 4.66/5.0).
- Spring 2024 EE6350 (M.S./Ph.D.) VLSI Design Lab (32 students, Eval. 4.82/5.0).
- Fall 2024 EE4312 (B.S./M.S.) Analog Electronic Circuits (93 students, in progress)

Students Supervised:

Doctoral Theses Advised:

1. Shouri Chatterjee, "Analog Design Techniques at 0.5V," October 21 2005; currently Professor at the Indian Institute of Technology Delhi, Dept. of Electrical Engineering, Delhi (India).
2. Babak Soltanian, "Design Techniques for Low-noise LC Voltage-controlled Oscillators," May 8 2006; currently at Cepand Inc., San Francisco, CA, USA.
3. Frank Zhang, "Ultra Wideband Pulse Radio Receivers in Digital CMOS Process," March 17 2008; currently at GlobalFoundries, Dallas, TX, USA.
4. Anuranjan Jha, "Current-Steering Digital-to-Analog Converter Based Pulse Generation Techniques for Ultra-Wideband Pulse Radio Transmitter," October 28 2008; currently at Apple, Cupertino, CA, USA.
5. Junhua Shen, "Design Techniques for Ultra-Low-Voltage and Ultra-Low-Power Pipelined ADCs," February 23 2010; currently at Analog Devices, Wilmington, MA, USA.
6. Ajay Balankutty, "Architectures and Circuit Design Techniques for Ultra Low Voltage CMOS Receivers," February 26 2010; currently at Intel Labs, Portland, OR, USA.
7. Yiping Feng, "Digitally Assisted Linearity Calibration Techniques for High Performance Direct Conversion Receivers," April 27 2010; currently at Blue Danube Labs, Warren, NJ, USA.
8. Shih-An Yu, "Design Techniques for Frequency Synthesizers in Highly Scaled CMOS Technologies," Dec. 15 2010; currently at TerraSILIC, Taipei, Taiwan.
9. Kshitij Yadav, "Ultrasound Data Communications for Ultra-low-power Wake-up in Sensor Nodes", Sept. 28 2012; co-advised with I. Kymissis; currently at Qualcomm, San Diego, CA, USA.

10. Karthik J. Tripurari , “RF Frontend for Spectrum Analysis in Cognitive Radio,” Nov. 15 2013; currently at Qualcomm, San Diego, CA, USA.
11. Baradwaj Vigraham, “Power Efficient Circuit Architectures for Receivers Leveraging Nanoscale CMOS”, March 14 2014; currently at Maxlinear, San Jose, CA, USA.
12. Jayanth Kuppambatti, “Design Techniques for Analog-to-Digital Converters in Scaled CMOS Technologies,” March 27 2014; currently at Seamless Microsystems, San Jose, CA, USA.
13. Chunwei Hsu, “Challenges and Solutions for High Performance Analog Circuits with Robust Operation in Low Power Digital CMOS,” Jan. 20 2014; currently at Analog Devices, Somerset, NJ, USA.
14. Rabia Tugce Yazicigil, “Compressive Sampling as an Enabling Solution for Energy-Efficient and Rapid Wideband RF Spectrum Sensing in Emerging Cognitive Radio Systems,” Feb. 29 2016; co-advised with J. Wright, currently Assistant Professor ECE at Boston University, Boston, MA, USA.
15. Jianxun Zhu, “Architectures and Circuit Techniques for High Performance Field Programmable CMOS Software Defined Radios,” Jan. 31st 2017; currently at Analog Devices, Somerset, NJ, USA.
16. Yang Xu, “Switched-Capacitor RF Receivers for High Interferer Tolerance,” Nov. 16th 2017; currently at Apple, Inc, Cupertino, CA, USA.
17. Gautam Gangasani, “Architectures and Circuits Leveraging Injection-Locked Oscillators for Ultra-Low Voltage Clock Synthesis and Reference-less Receivers for Dense Chip-to-Chip Communications,” March 27th 2018; currently at Marvell, Fishkill, NY, USA.
18. Tanbir Haque, “A Flexible RFIC Architecture for High-Sensitivity Reception and Compressed-Sampling Wideband Detection,” July 22nd 2019, co-advised with J. Wright; formerly at Interdigital Communications, Melville, NY, USA.
19. Vivek Mangal, “Energy Detecting Receivers for Wake-Up Radio Applications,” Sept. 27 2019; currently at WiLO Networks, CA, USA.
20. Daniel De Godoy, “Ultra-Low-Power IoT Solutions for Sound Source Localization: Combining Mixed-Signal Processing and Machine Learning,” Oct. 1 2019, co-advised with Xiaofan Jiang; currently at Skyworks, Austin, TX, USA.
21. Sarthak Kalani, “Voltage and time-domain analog circuit techniques for scaled CMOS technologies,” Nov. 11 2019; currently at Qualcomm Inc., San Jose, CA, USA.
22. Chengrui Le, “Design Techniques for Highly Integrated Hybrid-Switched-Capacitor-Resonant Power Converters for LED Lighting Applications,” Feb. 14 2020; currently at Apple Inc., Cupertino, CA, USA.
23. Shravan Nagam, “High Performance Sub-Sampling Phase Detector based Ring-Oscillator PLLs,” Feb. 28 2020; currently at Skyworks, Nashua, NH, USA.
24. Yudong Zhang, “Design of Power-Efficient Optical Transceivers and Design of High-Linearity Wireless Wideband Receivers,” April 9 2021; currently at Apple Inc., San Diego, CA, USA.
25. Guoxiang Han, “High-Performance Reconfigurable Radio-Frequency Integrated-Circuit Receiver Architectures for Concurrent Signal Reception,” April 26 2021; currently at Qualcomm Inc., San Jose, CA, USA.
26. Teng Yang, “In-situ and In-field temperature and transistor BTI sensing techniques with microprocessor-level implementation,” October 1 2021, co-advised with Mingoo Seok; currently at Intel Inc., Hillsboro, OR, USA.
27. Zhaowen Wang, “Efficient and High-Performance Clocking Circuits for High-Speed Data Links,” February 4 2022, currently at Xilinx Inc., San Jose, CA, USA.
28. Matt Bajor, “High Speed Direction of Arrival Sensing for Cognitive Radio Receivers,” September 9 2022, currently at Aspen Consulting, NJ, USA.
29. Subhajit Ray, “Ultra-low-power Audio Feature Extraction using Time-Mode Analog Signal Processing Circuits,” March 3 2023, currently at IBM Research, Yorktown, NY, USA.
30. Petar Barac, "LO-Path Modulated Receivers for Cognitive Radio and Phased Array Systems," December 10 2024.

Current Doctoral Students:

1. Scott Newton, "Synthesizing Analog Circuits using Digital CAD Tools," ongoing (started Fall 2014 – on leave).
2. Rui (Ray) Xu, "High Performance Analog Front Ends for Physics Experiments," ongoing (started Fall 2020).
3. Adam Chamberlain, "SONOS Devices in Analog Applications," ongoing (started Fall 2021).
4. Hongzhe Jiang, "High Performance Analog Interfaces," ongoing (started Fall 2022).

M.S. Student Research Projects:

- Yingrui Wei, "Design of Front-End Electronics for Airborne Gamma-Ray Detector," Summer and Fall 2024.
- Chuhan Xue and Jingyi Huang, "Platform for Chip Testing," Summer 2024.
- Yuechen He, "MOSbius: CMOS Circuits Lab on a Chip". Summer 2024.
- Cade Gleekel, "Mobius: CMOS Circuits Lab on a Chip", Summer and Fall 2023.
- Longyi Li, "Characterization of passive components at cryogenic temperatures," Fall 2022.
- Cade Gleekel, "Time-mode Analog Circuits," Summer and Fall 2022.
- X. Sun, Exploration of analog feature extractors for machine-learning applications," Spring 2022.
- Longyi Li, Yunfan Gao and Zhou Chen, "Mobius: Analog Circuits Lab on a Chip," Summer 2022.
- Ajay Bharadwaj, "Phase Interpolators for High Speed I/O Interfaces," Summer, Fall 2021.
- Hongzhe Jiang, "Class D Amplifiers in Skywater 130nm using Open-Source CAD Tools," Summer, Fall 2021.
- Hongyi Li, "CMOS Annealer Design Based on Injection Locking Oscillators" Spring 2020.
- Michael Unanian, "Efficient I/O for Data Center Communications," Fall 2017-Spring 2019.
- Andrew Kang, "VCO-OTAs for RF Receivers," Fall 2018-Spring 2019.
- Petar Barac, "Spectrum Scanning in Multi-Antenna Receivers," Fall 2018-Spring 2019.
- Sobhit Srivastava, "NanoPower Energy Harvesting," Fall 2018.
- Louisa Sainz de la Maza, "Ultra-Low-Power Wireless Communications in Tag Networks," Fall 2018
- Ciyuan Zhang, "Signal Processing for Compressive-Sampling Direction-of-Arrival Finder," Summer 2017 - Fall 2017
- Robert Blayne Kettlewell, "Compressive Sampling DSP on FPGAs," Summer 2016 – Fall 2016
- Zarion Jacobs, "Antennas for Phased Arrays," Fall 2015 – Spring 2016 – Summer 2016 – Fall 2016.
- Damla Dimlioglu, "Radiation Hard Analog-to-Digital Converter for the CERN LHC," Fall 2015 – Spring 2016
- Suhas Rao, "Analysis and Modeling of Voltage-Controlled Oscillator Based Amplifiers," Fall 2015 – Spring 2016
- Guoxiang Hang, "RF applications of Quadrature Hybrids," Fall 2015 – Spring 2016
- Sanket Gupta, "Voltage-Controlled Oscillator Based Linear Dropout Regulators," Spring 2015 – Fall 2015.
- Manoj Gupta, "Pseudo Random Noise generators for compressed sampling systems," Fall 2014-Fall 2015.
- Ethan (YiChen) Zhu, "FPGA Implementation of Compressive Sampling Recovery," Fall 2014.
- Jonathan Chang, "Analysis of FBAR Resonators, Fall 2014.
- Sagar Vaze, "Phase Locked Loops for Nanoscale CMOS," Fall 2013-Spring 2014.
- Mengxi Lin, "UWB Pulse Radio Interfaces with Enhanced Range for EnHANTs," Spring 2013, Summer 2013, Fall 2013.
- Vaibhav Pandey, "Coherent UWB Pulse Radio RF Front Ends," Spring – Fall 2013.
- Branislav Jovanovic, "Building Blocks for Cognitive Radio Systems," co-advised with H. Krishnaswamy, Fall 2012 – Spring 2013.
- Younwan Kim, "Energy Harvesting Module for EnHANTs," Spring 2013.
- Michael Whalen, "VLSI Implementation of PN Sequence Generators," Fall 2012.

- Xiang Li, "Efficient Residue Amplifiers for A/D conversion," Spring – Fall 2012.
- Meng Wang, "UWB Pulse Radio Interfaces for Energy Harvesting Active Networked Tags," Fall 2011-Fall 2012.
- Hao Wang, "UWB Pulse Radio Software Drivers," Spring 2012 – Fall 2012.
- Pranav Sood and Jian Lu, "UWB Pulse Radio Testing," Fall 2012.
- Scott Newton, "Review study of ADC specifications for Wireless Applications," Fall 2011-Spring 2012.
- Teng Yang, "Modeling and Analysis of Iterative Downconverters," Fall 2011-Spring 2012.
- Chen Keng, "Highly Integrated Power Factor Correction Circuits," Fall 2011-Spring 2012.
- Zuyang Cao and Jihing Zou, "Ultrasound Data Communications," Spring 2012.
- Ying Teng, "Efficient Controllers for Switched Capacitor DC/DC converters," Fall 2011.
- Jianxun Zhu, "Designing an Ultra-Wideband Interface for EnHANTs," Spring 2011.
- Yuan Zhou and Chengrui Le, "Opamp Design with Organic Transistors," Spring 2010-Fall 2010 (with Prof. Kymissis)
- Dinesh M.B. Maheswaran, "Design of a 300Msps 4bit ADC," Fall 2009-Fall 2010.
- Sudhir Nagaraj, "Ultra-low Voltage A/D Converter Testing," Spring 2010.
- William Lee, "Multi Source Sound Experiment Setup," Fall 2009 (with Prof. Kymissis).
- Chunwei Hsu, "A 10GHz DDFS-PLL in 65nm CMOS," Fall 2009-Spring 2010.
- Frank Fang, "Switched capacitor power converter design," Fall 2009-Spring 2010.
- Mingdong Hu, "Opamp Design with Organic Transistors," Summer 2009-Fall 2009 (with Prof. Kymissis).
- Ankita Nayak, "FPGA Implementation Of Digital Calibration For IIP3 Enhancement," Fall 2009.
- Tim Hyuk, "Mismatch modeling of MOM capacitors," Spring 2009-Fall 2009.
- Jayanth Narasimhan Kuppambatti, "Wireless Sensor Node Design," Fall 2008-Spring 2009.
- Ryan Roberts and Robin Stevenson, "Device Variation Characterization [90nm]," Spring 2008-Fall 2008.
- Navin Harwalkar, "Ultra Low Voltage, High Gain OTAs," Fall 2007-Fall 2008.
- Bingrui Yang and Xin Li, "Advanced Sound Processing," Fall 2007-Fall 2008 (with Prof. Kymissis)
- B.J. Lim, "Ultra Low Voltage Voltage Controlled Oscillator Design with High Power Supply Rejection," Spring 2008.
- Jonathan Tompson, Adam Dolin, "Wireless Testing of Integrated Circuits," Fall 2006-Fall 2007.
- Christos Vezirtzis, "Low Voltage Reference Circuits," Fall 2006-Fall 2007.
- H.S. Lin, "Device Variation Characterization," Summer 2006-Fall 2006.
- Chia-Yin Chen, "Automatic Measurement Setup for Device Variation Characterization," Spring 2006-Fall 2006.
- Tekalegn Habta Lemji, "Single-ended to Differential Signal Converter," Fall 2006.
- Kuo-Chih Feng, Jin Wook Son, Inanc Meric, "Wireless Testing of Integrated Circuits," Spring 2006.
- Ajay Balankutty, Tai-Chiao Chih, "Device Variation Characterization," Summer 2005-Fall 2005.
- Vasilios Giannopoulos, "Design of Low Voltage Programmable Gain Amplifiers," Spring 2005.
- Mustapha Abdulai, "Design of Low Voltage OTAs," Spring 2005.
- Steven Battle, Allen Chen, "Novel Frequency Divider Integrated Circuit," Fall 2004.
- Cheng-Feng Chu, "Design of a Quadrature LC Oscillator," Fall 2004.
- Zelalem Asmamaw, "Design of operational amplifiers for the time encoding machine," Summer 2004.
- Andrew Han, "RF powered circuits," Summer 2004.
- Han-Yun Chang, "Novel Frequency Divider Integrated Circuit," Fall 2003-Spring 2004.
- Theodore Kengne, "CMOS characterization for ultra-low voltage circuit design," Fall 2003.
- Chia-Hung Chen, Shi-Gun Pan, "Electrocardiogram Measurements," Fall 2002.
- Chao-Chieh Hsu, Shao-Hsune Lee, "Short Range Wireless Data Transmission," Fall 2002.

Undergraduate Student Research Projects:

- Rosnel Alejandro Leyva-Cortes “MOSbius: CMOS Circuits Lab on a Chip”, Fall 2024.
- Erin Suh and Nico de la Cruz, “Mobius: CMOS Circuits Lab on a Chip”, Spring 2024.
- Zichen (Doris) Qian and Nico de la Cruz, “Developing the Mobius circuit lab on a chip platform,” Spring 2023.
- Maria Gordiyenko and Nolan Tremelling, “Exploration of analog feature extractors for machine-learning applications,” Summer 2022.
- Wendy Fernandez (City University of New York, EE), “Enhancing Voice Localization by Shaping Audio Features Using Filters and Time-Delay Estimation” Fall 2017 – Spring 2018
- Louisa Sainz de la Maza, “Ultra-Low-Power Wireless Communications,” Fall 2017 – Spring 2018
- Christopher Kunkel, “Sound Processing for Localization,” Spring 2016.
- Christopher Kunkel, “Automatic Spectrum Occupancy Measurements,” Spring 2015, Summer 2014 (NSF/REU), Fall 2015.
- Jeffrey Yuan, “Automating Spectrum Occupancy Measurements.” Spring 2013, Summer 2013 (NSF/REU), Summer 2014 (NSF/REU), Fall 2014, Spring 2015, Summer 2015 (NSF/REU), Fall 2015.
- Zoga Borova, “Energy Harvesting Module for EnHANTs,” Summer 2013 (B.S. at Cooper Union in NYC)
- Allison Duh, “Spectrum Occupancy Measurements,” Fall 2012 – Spring 2013.
- Felipe de Oliveira (Stevens Institute of Technology), “FPGA implementation of a UWB pulse radio MAC,” Summer 2012.
- Jiasi Chen, “Interfacing Mica2 Motes with an UWB Receiver and Transmitter,” Fall 2009-Summer 2010.
- David Blumenfeld (UCLA), “Interfacing Ultrasound Wake-up Receivers to Mica2 Motes,” REU project, Summer 2010.
- Deep Shrestha, “An Automated System That Measures Energy Harvested By A Solar Cell Under Different Light Conditions,” Summer 2009-Spring 2010.
- Ben Waters, “Inductive power transfer,” Spring 2009-Fall 2009.
- Jiasi Chen, “Light energy harvesting measurements,” Spring 2009.
- Ed Chiang, “CMOS characterization for ultra-low voltage circuit design,” Spring 2005-Fall 2006.
- Hector Hung, Vladislav Adzic, “Implementation of simulation scripts for Monte-Carlo Simulation of device parameter variations and mismatch,” Summer 2005–Spring 2006.
- Vivek Rajeswaran, “CMOS characterization for ultra-low voltage circuit design,” Fall 2005-Spring 2006.
- Tawfiq Musah, “Voltage references operating from a low power supply,” Summer 2004-Spring 2005.
- Sebastian Sorgenfrei, “Design and simulation of compact, on-chip LC resonators,” Spring 2004-Fall 2004.
- Chia-Ching (Peter) Chen, “Implementation of parametrized layout cells for analog IC design,” Summer 2004.
- Eric Chang, Wacław Aleksander Godycki, “Novel Biasing for LC oscillators,” Summer 2003.

Visitors:

- Yang Zhang, Ph.D. Candidate, City University of Hong Kong; Visiting Scientist, January-May 2019.
- Debajit Basak, Ph.D. Candidate, City University of Hong Kong; Visiting Scientist, August-November 2017.
- Erjia Shi, Ph.D. Candidate, City University of Hong Kong; Visiting Scientist, March-May 2017.
- Jiangpeng Wang, Ph.D. Candidate, City University of Hong Kong; Visiting Scientist, March-May 2017.
- Alessandro Bertolini, M.S. student (Thesis Research Project), University of Brescia, January - June 2016.

- Domenico Nicita, M.S. student (Thesis Research Project), Politecnico di Torino, August 2014-Feb. 2015.
- Marco Daldoss, M.S. student (Thesis Research Project), University of Brescia, Visiting Scientist, Sept. 2013-Feb. 2014; July-August 2014.
- Chi-Tung Ko, Ph.D. Candidate, City University of Hong Kong; Visiting Scientist, March-April 2012.
- M. Crepaldi, Ph. D. Candidate, VLSI Research Laboratory, Dipartimento di Elettronica, Politecnico di Torino; Visiting Scientist, July 2008-Dec. 2009.
- C. Li, Institute of Micro-electronics, Peking University, Beijing, China; Ph.D. exchange student, Feb. 2008-Feb. 2009.
- Prof. J. Fernandez, Associate Professor, Technical University of Lisbon (Instituto Superior Técnico), Portugal; Visiting Scientist, March-Sept 2008.
- Prof. K. P. Pun, Assistant Professor, City University of Hong Kong; Visiting Scientist, May-July 2004.

Doctoral Thesis Reviewed: (theses reviewed as advisor not included)

- Palaskas, Yorgos, "Syllabic Companding Filters with Emphasis On Wireless Applications," November 1 2002, Member of the Jury, Columbia University, NY, USA.
- Laiho, Mika, "Mixed-Mode Cellular Array Processor Realization for Analyzing Brain Electrical Activity in Epilepsy," June 28, 2003, Pre-examiner, Helsinki University of Technology, Finland.
- Li, Shaorui, "Q-Enhanced LC Filters With Automatic Tuning," April 26, 2004, Chair of the Jury, Columbia University, NY, USA.
- Ranganathan, Sanjeev, "Discrete-Time Parametric Amplification Using Mosfets," May 28, 2004, Chair of the Jury, Columbia University, NY, USA.
- Ozgun, Mehmet, "Power Management of Integrated Analog Filters", March 4 2004, Member of the Jury, Columbia University, NY, USA.
- Baki, Rola Abdul, "Robust design and distortion analysis of fully integrated image reject RF CMOS frontends," July 2005, External examiner, McGill University, Montreal, Canada.
- Li, Chuxiang, "Advanced Signal Processing and Resource Scheduling In Space-Time Communication Systems," October 6 2006, Member of the Jury, Columbia University, NY, USA.
- Yoshizawa, Atsushi, "Dynamically Biased Filters with High Linearity," November 13 2006, Member of the Jury, Columbia University, NY, USA.
- Stanic, Nebojsa, "Low Voltage RF Integrated Filters and Communication Circuits", December 8 2006, Chair of the Jury, Columbia University, NY, USA.
- Kwak, Kyung Joon, "Minimalist Detection and Counting Protocols in Wireless Sensor Networks", April 29, 2008, Member of the Jury, Columbia University, NY, USA.
- Weltin-Wu, Colin, "Design of Low Power, High Speed Level Crossing ADCs and Continuous Time DSPs," December 16, 2011, Member of the Jury, Columbia University, NY, USA.
- KO, Chi-Tung, "High Resolution, Multi-Stage, Time-to-Digital Converters," March 15, 2013, External Examiner, City University of Hong Kong, Hong Kong, SAR, China.
- Sarik, John, "Systems for Pervasive Electronics and Interfaces," April 9, 2013, Member of the Jury, Columbia University, NY, USA.
- Huang, Xiongchuan, "Ultra-low-power Event-driven Radio Design," March 18, 2014, Member of the Jury, Delft University of Technology, Delft, The Netherlands.
- Chakrabarti, Anandaroop, "Architectures and Integrated Circuits for Efficient, High-power "Digital" Transmitters for Millimeter-wave Applications," May 13, 2015, Chair of the Jury, Columbia University, NY, USA.
- Yang, Shyuan, "Optimization of Printed Electronics," September 18, 2015, Member of the Jury, Columbia University, NY, USA.
- Liu, Supeng, "Design of Low Power Fractional-N Digital Phase Locked Loop for FMCW Radar Application," January 2016, External Examiner, Nanyang Technological University, Singapore.

- Zhou, Jin, “Integrated Self-Interference Cancellation for Full-Duplex and Frequency-Division Duplexing Wireless Communication Systems,” September 20, 2016, Member of the Jury, Columbia University, NY, USA.
- Li, Jiangyi, “Very-Large-Scale-Integration Circuit Techniques in Internet-of-Things Applications,” February 19, 2017, Member of the Jury, Columbia University, NY, USA.
- Negar Reiskaramian, “Fully Integrated Magnetic-Free Non-Reciprocal Components by Breaking Lorentz Reciprocity: from Physics to Applications,” May 14 2019, Chair of the Jury, Columbia University, NY, USA.
- Sohail Ahasan, “Architectures and Integrated Circuits leveraging Multi-phase Clocking of Passive Mixers for applications in RF/MM-wave and Electro-optical Systems,” October 8, 2021, Columbia University, NY, USA.
- Dongkwun Kim, “Energy-efficient integrated power management architectures for emerging needs of IoT devices to data centers,” December 10, 2021, Chair of the Jury, Columbia University, NY, USA.
- Mohammad Khorshidian, “Advances in linear periodically time variant circuits: From high performance filters to magnetic-free inductorless nonreciprocal components,” January 27, 2021, Chair of the Jury, Columbia University, NY, USA.
- Stephen Xia, “Selective Audio Filtering for Enabling Acoustic Intelligence in Mobile, Embedded, and Cyber-Physical Systems,” April 21, 2022, Chair of the Jury, Columbia University, NY, USA.
- Liwei Zhou, “Model predictive critical soft-switching enable high-performance software-defined power electronics: Converter configuration, efficiency, and redundancy,” May 5, 2022, Chair of the Jury, Columbia University, NY, USA.
- Hetong, Wang, “Wideband Continuous-Time Delta Sigma Modulators with High Power Efficiency,” December 13, 2022, External Examiner, City University of Hong Kong, Hong Kong, SAR, China.
- Armagan Dascurcu, “Enabling Technologies for Next-Generation Systems: MIMO, Extreme Bandwidths, TeraHertz, and Heterogeneous Integration,” September 18, 2023, Member of the Jury, Columbia University, NY, USA.
- Bo Zhang, “Energy-Efficient Hardware Design for Machine Learning with In-Memory Computing,” November 29, 2023, Member of the Jury, Columbia University, NY, USA.
- Kevin Kam, “Wireless Sensor Hardware Development for Advanced Smart Cities Application”, March 6, 2024, Chair of the Jury, Columbia University, NY, USA.
- Matthew Janes, “Manhattan Converter Family: Partial Power Processing, Module Stacking with Linear Complexity, Efficiency and Power-Density, in DC and AC Applications”, September 9, 2024, Chair of the Jury, Columbia University, NY, USA.
- Sasank Garikapati, “Architectures Leveraging Switched Capacitor Circuits for Emerging Wireless Applications”, September 25, 2024, Member of the Jury, Columbia University, NY, USA.

Grants

(Total Granted: \$22.3M; PK's Share: \$11.4M)

- P. Kinget, “Low noise integrated oscillators”, NY State Office of Science, Technology, and Academic Research, Research Grant, 07/01/02 – 06/30/03.
- P. Kinget, “IC design for UWB locationing”, Motorola University Partnerships in Research, Research Grant, 09/01/03 – 06/30/06.
- P. Kinget and Y. Tsvividis, “Acquisition of Test & Measurement Equipment for Research in Wireless and Mixed-Signal Circuits”, NSF - Major Research Instrumentation, Instrumentation Grant, Columbia University Match, 07/01/03 – 08/30/05.
- P. Kinget, “Noise and interference cancellation loops for integrated oscillators”, Semiconductor Research Corporation, Research Grant, 04/01/04 - 03/31/06.
- P. Kinget and R. Gharpurey (Univ. of Texas), “Collaborative Research: Architecture and Implementation of Intelligent Transceivers for Ultra-Wideband Communication”, National Science Foundation (ENG), Research Grant, 09/2004- 08/2008.

- P. Kinget and Y. Tsvividis, "0.5V Analog Integrated Circuits for nanoscale CMOS technologies", Analog Devices, Research Grant, 09/01/04 – 08/30/08.
- P. Kinget and Y. Tsvividis, "Analog Circuits for nanoscale CMOS technologies", Intel Corporation, Research Grant, 10/01/05 – 09/30/08.
- P. Kinget, "Analog & RF Integrated Circuits", Silicon Laboratories, Cash Gift, 11/2004-11/2007.
- P. Kinget, "Fabrication of BiCMOS test-circuits (30 mm²)", Philips Semiconductors, In-Kind Donation of free chip fabrication 2004-2005.
- P. Kinget, "Ultra Low Voltage Analog Interface Circuits", Realtek Corporation, Research Grant, 09/01/2005-08/30/2007.
- P. Kinget, "Multi-Band RF Front-ends", Toshiba Corporation, Research Grant, 09/01/2005-08/30/2008.
- P. Kinget, "REU supplement for ECS 0424312: Collaborative Research: Architecture and Implementation of Intelligent Transceivers for Ultra-Wideband Communications", National Science Foundation (ENG), Research Grant, 06/01/2005-05/31/2006.
- P. Kinget, "Contact-less circuit measurement technology for non-damaging and non-polluting on-wafer measurement of device parameter variations during manufacture", IBM Faculty Award, 11/2005.
- P. Kinget, "Fabrication of 90nm CMOS circuits (3x16 mm²)", United Microelectronics, In-Kind Donation of free chip fabrication 2005-2008.
- P. Kinget, "High Speed and RF Integrated Circuits", Lucent Technologies, Research Grant, 02/01/2006-08/31/2006.
- P. Kinget, "Ultra-low Voltage CMOS Analog Interfaces", Broadcom Corporation, Unrestricted Gift, 09/01/2007
- P. Kinget, "RFIC Synthesizers with an Ultra Broad Frequency Range", Alcatel-Lucent & LGS Innovations, Research Sub Contract, 09/01/2006-08/31/2010.
- P. Kinget, "Ultra-low Voltage CMOS Analog Interfaces", Broadcom Corporation, Unrestricted Gift, 09/01/2008.
- P. Kinget, "Analog & RF Integrated Circuits", Silicon Laboratories, Cash Gift, 09/01/2008-08/30/2009.
- P. Kinget, "Analog & RF Integrated Circuits", Marvell Semiconductor, Cash Gift, 09/01/2008-08/30/2009.
- P. Kinget, "Fabrication of 65nm CMOS circuits (2.5mm²)", Mediatek, In-Kind Donation of free chip fabrication , Nov 2008.
- M. Banu (MHI Consulting) & P. Kinget, "RF-System and Integrated Electronics for Low-Cost Smart Antenna Arrays," National Science Foundation (STTR-Phase I), 07/01/2008-06/30/2009.
- P. Kinget, "Analog and RF Integrated Circuit Design", Analog Devices, Research Grant, 09/01/2008-8/31/2009.
- I. Kymissis, P. Kinget, D. Rubenstein, G. Zussman, "Self-Powered, Networked Tags for Active Tracking of Physical Objects", Google Research Grant, 2009.
- P. Kinget, "Fabrication of 65nm CMOS circuits (4mm²)", ST Microelectronics, In-Kind Donation of free chip fabrication , April 2009.
- P. Kinget, "Fabrication of 90nm CMOS circuits (2.2mm²)", United Microelectronics, In-Kind Donation of free chip fabrication , April 2009.
- G. Zussman, P. Kinget, I. Kymissis, D. Rubenstein and X. Wang, "Active Networked Tags for Disaster Recovery Applications," First Prize Wireless Foundation Challenge, Vodafone Foundation, 07/2009-06/2012.
- P. Kinget, "Ultra-low Voltage CMOS Analog Interfaces", Broadcom Corporation, Unrestricted Gift, 09/01/2009.
- P. Kinget and I. Kymissis, "Ultrasonic wireless data for extremely low-power wake-up receivers," National Science Foundation, Research Grant, 09/2009-08/2012.
- P. Kinget, "Analog and RF Integrated Circuit Design", Analog Devices, Research Grant, 09/01/2009-8/31/2010.

- P. Kinget, "Ultra-Low Power Short-Range Coherent Wireless Links: Circuits and Architectures Adapted to Nanoscale CMOS," Texas Instruments, Research Grant, 06/01/2010-05/31/2013.
- P. Kinget, "Analog & RF Integrated Circuits", Silicon Laboratories, Cash Gift, 03/01/2010.
- P. Kinget, "Fabrication of 65nm CMOS circuits (5.75mm²)", Mediatek, In-Kind Donation of free chip fabrication valued at May 2010.
- P. Kinget and I. Kymissis, "REU Extension: Ultrasonic wireless data for extremely low-power wake-up receivers," National Science Foundation, Research Grant, 06/2010-08/2010.
- R. Gharpurey and P. Kinget, "Collaborative Research: Iterative Downconversion for Broadband Signal Digitization," National Science Foundation, 08/01/2010-07/31/2013.
- P. Kinget, "Ultra-low Voltage CMOS Analog Interfaces", Broadcom Foundation, Charitable Gift, 11/01/2010.
- P. Kinget, "Fabrication of 65nm CMOS circuits (1mm²)", ST Microelectronics, In-Kind Donation of free chip fabrication, June 2010.
- D. Rubenstein, P. Kinget, I. Kymissis, X. Wang, G. Zussman, "NetSE: Medium: Active Networked Tags: Ultra-Low Power Networking for Object Locating and Tracking", National Science Foundation, 08/2010-07/2013.
- P. Kinget, "Variation-Tolerant Noise-Shaping ADCs with Embedded Digital Bias and Vdd Scalable from 0.5V to 1.2V for Nanoscale CMOS," Semiconductor Research Corporation, Research Grant, 02/01/11-01/31/14.
- S. O'Brien, D. Steingart, A. Couzis, S. Sanders, I. Kymissis and P. Kinget, "ADEPT: Metacapacitors – Efficient Integrated Power Management", Dept. of Energy, ARPA-E, Research Grant, 09/01/2010-08/31/2013.
- P. Kinget, "Donation of laboratory test equipment", Interdigital Corporation, Equipment Donation, 12/2010.
- P. Kinget, "Study of energy consumption efficiency of analog versus digital computing for telecommunications applications," Bell Laboratories, Alcatel-Lucent, Cash Gift, 11/2010
- P. Kinget, "Analog and RF Integrated Circuit Design", Analog Devices, Research Grant, 01/01/2011-12/31/2011.
- P. Kinget, "Fabrication of 65nm CMOS circuits (3.25mm²)", ST Microelectronics, In-Kind Donation of free chip fabrication, March and June 2011.
- D. Rubenstein, P. Kinget, I. Kymissis, X. Wang, G. Zussman, "REU-Extension: NetSE: Medium: Active Networked Tags: Ultra-Low Power Networking for Object Locating and Tracking", National Science Foundation, 06/2011-07/2013.
- R. Gharpurey (UT-Austin), P. Kinget and H. Krishnaswamy, "A broadband mixed-signal iterative downconversion spectrum analyzer for signal recognition applications", DARPA, CLASIC, 09/01/2011-08/31/2014.
- P. Kinget, "Ultra-low Voltage CMOS Analog Interfaces," Broadcom Foundation, Charitable Gift, 11/01/2011.
- P. Kinget, "Analog & RF Integrated Circuits", Silicon Laboratories, Cash Gift, 12/01/2011.
- P. Kinget, "Analog and RF Integrated Circuit Design," Analog Devices, Research Grant, 01/01/2012-12/31/2012.
- P. Kinget, "Fabrication of 65nm CMOS circuits (4.5mm²)", ST Microelectronics, In-Kind Donation of free chip fabrication, March & April 2012.
- K. Yadav, I. Kymissis and P. Kinget, "SBIR Phase I: Ultrasound Data Communications for Wireless Sensors and Real Time Location Systems," National Science Foundation, 06/01/2012-12/31/2012.
- H. Krishnaswamy and P. Kinget, "CMOS RF Field-Programmable Full-Duplex T/R Module based on a Generalized RF Vector-DAC Power-amplifier Array and an Interferer-Reflecting Low-Noise Receiver Front End," DARPA, RF-FPGA, 06/01/2012-05/31/2016.
- P. Kinget, "Fabrication of 65nm CMOS circuits (2.4mm²)", Texas Instruments, In-Kind Donation of free chip fabrication, Sept. 2012.
- M. Seok and P. Kinget, "Self-Aware Computing for Cyber Physical Systems," Catalyst Foundation, Research Grant, 1/1/2013-12/31/2016.

- P. Kinget, "Analog and RF Integrated Circuit Design", Analog Devices, Research Grant, 01/01/2013-12/31/2013.
- P. Kinget, "Ultra-low Voltage CMOS Analog Interfaces", Broadcom Foundation, Charitable Gift, 11/01/2012.
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- P. Kinget, "Fabrication of 65nm CMOS circuits (2.4mm²)", ST Microelectronics, In-Kind Donation of free chip fabrication, March 2013.
- P. Kinget, "REU supplement for Collaborative Research: Iterative Downconversion for Broadband Signal Digitization," National Science Foundation, 04/15/2013.
- P. Kinget, "Fabrication of 65nm CMOS circuits (1.96mm²)", ST Microelectronics, In-Kind Donation of free chip fabrication, June 2013.
- P. Kinget, "Fabrication of 55nm CMOS circuits (2mm²)", VIA Telecom, In-Kind Donation of free chip fabrication, June 2013.
- P. Kinget, "Switched-Mode Signal Processing: An Innovative Paradigm for High Performance Analog in Nanoscale CMOS," National Science Foundation, 09/01/2013-08/30/2016.
- P. Kinget, "Hybrid Two-Step PLLs for Digital SoCs in Nanoscale CMOS," Semiconductor Research Corporation, 02/01/2014-01/31/2017.
- P. Kinget, "Analog & RF Integrated Circuits", Silicon Laboratories, Cash Gift, 1/1/2014.
- P. Kinget, "Analog and RF Integrated Circuit Design," Analog Devices, Research Grant, 01/01/2014-12/31/2014.
- P. Kinget, I. Kymissis, J. Wright and A. Zeira, "GOALI: Low-Power, Multi-Tiered, Shared-Spectrum Access Terminals using Compressive Scanning and On-Top-of-CMOS BAW Filter Banks," National Science Foundation, 2014-2017.
- P. Kinget and I. Kymissis, "Bulk-acoustic Resonators Integrated On Top of CMOS for High Performance RF Applications," DARPA, Study under RF-FPGA, , 2014-2015. P. Kinget, "Fabrication of 40nm CMOS circuits (5.6mm²)", United Microelectronics Corporation (UMC), In-Kind Donation of free chip fabrication, August 2014.
- P. Kinget, "Analog and RF Integrated Circuit Design", Analog Devices, Research Grant, 01/01/2015-12/31/2015.
- P. Kinget, "Analog & RF Integrated Circuits", Silicon Laboratories, Cash Gift, 7/10/2015.
- P. Kinget, "GOALI: Low-Power, Multi-Tiered, Shared-Spectrum Access Terminals using Compressive Scanning and On-Top-of-CMOS BAW Filter Banks," REU Extension, National Science Foundation, 2015-2016.
- P. Kinget, "GOALI: Low-Power, Multi-Tiered, Shared-Spectrum Access Terminals using Compressive Scanning and On-Top-of-CMOS BAW Filter Banks," RET Extension, National Science Foundation, 2015-2016.
- P. Kinget, "Switched-Mode Signal Processing: An Innovative Paradigm for High Performance Analog in Nanoscale CMOS," REU extension, National Science Foundation, 2015-2016.
- P. Kinget, "Analog and RF Integrated Circuit Design", Analog Devices, Research Grant, 01/01/2016-12/31/2016.
- P. Kinget, "Analog & RF Integrated Circuits", Silicon Laboratories, Cash Gift, 11/2016.
- P. Kinget, "Analog and RF Integrated Circuit Design", Analog Devices, Research Grant, 01/01/2017-12/31/2017.
- M. Seok and P. Kinget, "Self-Aware Computing for Cyber Physical Systems," Catalyst Foundation, Research Grant, 1/1/2017-12/31/2019.
- X. Jiang, P. Kinget, S. Nirjon, and J. New, "Improving Pedestrian Safety in Urban Cities using Intelligent Wearable Systems," National Science Foundation, 6/01/2017-05/31/2019.
- K. Bergman, M. Lipson, A. Gaeta, P. Kinget (Columbia PIs), "PINE: Photonic Integrated Networked Energy efficient datacenters," Department of Energy, ARPA-E (Phase 1), Research Grant, 06/01/07-05/31/19.
- J. Wright and P. Kinget, "AITF: Learning and Adapting Sparse Recovery Algorithms for RF Spectrum Sensing," National Science Foundation, 6/01/2017-05/31/2019.
- P. Kinget, "Analog & RF Integrated Circuits", Silicon Laboratories, Cash Gift, 11/2017.

- P. Kinget, “Analog and RF Integrated Circuit Design”, Analog Devices, Research Grant, 01/01/2018-12/31/2018.
- P. Kinget, “Analog & RF Integrated Circuits”, Silicon Laboratories, Cash Gift, 11/2018.
- P. Kinget, “Analog and RF Integrated Circuit Design”, Analog Devices, Research Grant, 01/01/2019-12/31/2019.
- P. Kinget, “Development of a Full-Field X-ray Fluorescence Imaging System for Near Real-Time Trace Element Microanalysis of Complex Biological Systems”, Department of Energy, subaward via Brookhaven National Labs, Research Grant, 2019-2020
- P. Kinget, “Analog and RF Integrated Circuit Design”, Analog Devices, Research Grant, 01/01/2020-12/31/2020.
- P. Kinget, I. Kymissis and Lelantos, Inc., “STTR Phase I: CMOS Integrated Piezoelectric Vapor Sensors”, Phase I, 7/1/2020-2/9/2021
- P. Kinget, “Analog & RF Integrated Circuits”, Silicon Laboratories, Cash Gift, 11/2020.
- P. Kinget, “Analog and RF Integrated Circuit Design”, Analog Devices, Research Grant, 01/01/2021-12/31/2021.
- P. Kinget, “Adaptable Tactical Communications”, Department of Defense (Army), STTR with Aspen Consulting Group, Phase I and Phase II, 1/3/2020 - 3/31/2022
- P. Kinget, “Analog & RF Integrated Circuits”, Silicon Laboratories, Cash Gift, 06/2021.
- P. Kinget, I. Kymissis and Lelantos, Inc., “STTR Phase II: CMOS Integrated Piezoelectric Vapor Sensors”, Phase II, 9/1/2021 – 8/31/2023
- P. Kinget, “Gift for Chip Fabrication for EE6350 VLSI Design Lab Spring 2022,” Apple Inc., Cash Gift, 10/2021
- P. Kinget, “Analog and RF Integrated Circuit Design”, Analog Devices, Research Grant, 01/01/2023-12/31/2023.
- P. Kinget, “Gift for Chip Fabrication for EE6350 VLSI Design Lab Spring 2023,” Apple Inc., Cash Gift, 08/2022
- P. Kinget, “Using SONOS Transistors as Radiation Detectors,” NASA Graduate Fellowship for Ray Xu, Fall 2022-Spring 2023, 08/2022
- P. Kinget, “Analog and RF Integrated Circuit Design”, Analog Devices, Research Grant, 01/01/2024-12/31/2024.
- P. Kinget, “Using SONOS Transistors as Radiation Detectors,” NASA Graduate Fellowship for Ray Xu, Fall 2023-Spring 2024, 08/2023
- P. Kinget, “Gift for Chip Fabrication for EE6350 VLSI Design Lab Spring 2024,” Apple Inc., Cash Gift, 08/2023
- P. Kinget, “Gift for Chip Fabrication for EE6350 VLSI Design Lab Spring 2025,” Apple Inc., Cash Gift, 08/2024

Columbia Service Activities:

- Chair of the ‘Ph.D. admissions committee’ (F22, S23, F23, S24, F24)
- Department Chair (F17-S20)
- Vice-Chair for Faculty Affairs (Hiring & Jr. Faculty Mentoring) (F14, S15, F15, S16)
- Chair of the Faculty Recruitment Committee (F14, S15, F15, S16).
- Member of the ‘Ph.D. admissions committee’ (F06, S07, F07, S08, F11, S12, F12, S13, F13, S14, F14, S15, F15, S16).
- M.S. student advisor (F02-present).
- B.S. EE student advisor; F04/S05 4 students, F05/S06 6 students, F06/S07 6 students, F07/S08 5 students, F21/S22 6 students.
- SEAS Dean’s Taskforce on MS and Executive Programs (F13).
- EE Dept. Director for Graduate Programs (F11, S12, F12, S13, F13, S14).
- Chair of the Graduate Curriculum Committee (F13, S14).
- Co-Chair of the Teaching Lab Renovation Committee (F13, S14).

- Co-Chair of the Smart Cities Center in the Institute for Data Sciences and Engineering (IDSE) (F12, S13, F13, S14).
- Chair of the 'M.S. admissions committee' (F07, S08, F08, S09, F09, S10, F11, S12, F12, S13); member (F14, S14).
- Member of the 'EE Strategic Planning Committee' (F09, S10, F12, S13, F13, S14)
- Coordinated Hiring in Integrated Circuits and Systems (F07, S08, F12, S13, F13, S14)
- Member of the 'EE publicity committee' (F08, S09)
- Member (F03, S04, F04, S05, F05, S06) and Chair (F06, S07, F07, S08) of the 'EE computing committee'.
- EE Teaching Assistants coordinator (F04, S05, F05, S06).
- Minuteer EE faculty meetings (F02, S03, F03, S04).
- Contributor to M.S., Ph.D., B.S. open houses (lab tours and/or research presentations) (F02-present).
- Co-organizer of regular "Columbia Integrated Systems Laboratory Research Seminar" (F02-present).
- Instrumental in establishing and maintaining the "EE Students Projects Laboratory."

Publications:

U.S. Patents:

1. US 6,188,291: (02/13/2001) Gopinathan, Kinget, Long, Melville, "Injection locked multi-phase signal generator".
2. US 6,281,721: (08/28/2001) Kinget, Krishnapura, "Programmable frequency divider".
3. US 6,671,341: (12/30/2003) Kinget, Krishnapura, "Glitch free phase switching synthesizer".
4. US 7,076,169: (07/11/2006) Shpantzer, Meiman, Tseytlin, Ritterbush, Salamon, Feldman, Demir, Kinget, Krishnapura, Roychowdhury, "System and method for orthogonal frequency division multiplexed optical communications".
5. US 7,106,388: (09/12/2006) Vorenkamp, Wakayama, Jaffe, Carr, Venes, Kinget, Marz, Nguyen, "Digital IF demodulator for video applications".
6. US 7,167,651: (01/23/2007) Shpantzer, Tseytlin, Achiam, Salamon, Smilanski, Ritterbush, Cho, Khurgin, Meiman, Demir, Feldmann, Kinget, Krishnapura, Roychowdhury, Schwarzwald, Sciabarra, "System and method for code division multiplexed optical communications".
7. US 7,847,667: (12/07/2010) Kinget, Zhang, "Systems and methods for reducing circuit area".
8. US 7,847,633: (12/07/2010) Kinget, "Low voltage operational transconductance amplifier".
9. US 7,884,658: (02/08/2011) Kinget, Yu, "Circuits for Forming the Inputs of a Latch".
10. US 8,030,999: (10/04/2011) Chatterjee, Kinget, Tsividis, "Low Voltage Operational Transconductance Amplifier Circuits."
11. US 8,305,247: (11/06/2012) Pun, Chatterjee, Kinget, "Low Voltage Digital to Analog Converter, Comparator, and Sigma-Delta Modulator Circuits."
12. US 8,441,287: (05/14/2013) Chatterjee, Kinget, "Low Voltage Track and Hold Circuits."
13. US 8,594,603: (11/26/2013) Balankutty, Kinget, "Systems and Methods for Cancelling Interferers in a Receiver."
14. US 8,699,627: (04/15/2014) Crepaldi, Kinget, "Systems and Methods for Wirelessly Receiving Data."
15. US 8,704,553: (04/22/2014) Pun, Chatterjee, Kinget, "Low Voltage Comparator Circuits."
16. US 8,711,288: (04/29/2014) Vorenkamp, Wakayama, Jaffe, Carr, Venes, Kinget, Marz, Nguyen, "Digital IF demodulator for video applications."
17. US 8,849,227: (09/30/2014) Feng, Kinget, "Systems and Methods for Controlling the Second Order Intercept Point in Receivers."
18. US 9,143,144: (9/22/2015) Kuppambatti, Shen, Kinget, "Systems and Methods for Providing a Pipelined Analog to Digital Converter."
19. US 9,154,244: (10/6/2015): Feng, Kinget, "Systems and Methods for Controlling the Second Order Intercept Point of Receivers."
20. US 9,178,551: (11/3/2015) Vigraham, Kinget, "Circuits and Methods for Pulse Radio Receivers."

21. US 9,197,224: (11/24/2015) Kinget, Hsu, Yu, Tripurari, "Circuits and Methods for a Combined Phase Detector."
22. US 9,246,504: (1/26/2016) Shen, Kinget, "Circuits and Methods for Implementing a Residue Amplifier."
23. US 9,455,757: (9/27/2016) Tripurari, Kinget, Krishnaswamy, Yang, "Circuits and methods for performing harmonic rejection mixing."
24. US 9,424,952: (8/23/2016) Seok, Kinget, Yang, "Circuits, methods, and media for detecting and countering aging degradation in memory cells."
25. US 9,654,126: (5/16/2017) Kuppambatti, Shen, Kinget, "Systems and methods for providing a pipelined analog-to-digital converter."
26. US 9,755,590: (9/5/2017) Vigraham, Kinget, "Circuits for low noise amplifiers."
27. US 9,755,680: (9/5/2017) Zhu, Kinget, "Circuits for Field-Programmable Front Ends."
28. US 9,762,273: (9/12/2017) Kinget, Wright, Yazicigil, "Circuits and Methods for Detecting Interferers."
29. US 9,954,497: (4/24/2018) Zhu, Kinget, Krishnaswamy, "Circuits for Low Noise Amplifiers with Interferer Reflecting Loops."
30. US 10,084,414: (9/25/2018) Vigraham, Kuppambatti, Kinget, "Circuits and methods for switched-mode operational amplifiers."
31. US 10,122,345: (11/6/2018) Edrees, Kymissis, Kinget "Co-integrated bulk acoustic wave resonators."
32. US 10,122,396: (11/6/2018) Kinget, Wright, Yazicigil, "Circuits and methods for detecting interferers."
33. US 10,148,253: (12/04/2018) Xu, Kinget, "Circuits for switched capacitor receiver front-ends."
34. US 10,615,803: (04/07/2020) Nagam, Kinget, "Compact phase-locked loop with low jitter and reference spurs."
35. US 10,644,735: (05/05/2020) Kinget, Wright, Yazicigil, "Circuits and methods for detecting interferers."
36. US 10,763,787: (09/01/2020) Zhu, Kinget, "Circuits for wireless communication on multiple frequency bands."
37. US 10,819,284: (10/27/2020) Han, Haque, Kinget, "Circuits for modulated-mixer-clock multi-branch receivers."
38. US 10,833,694: (11/10/2020) De Godoy, Jiang, Kinget, "Circuits and methods for time-delay to digital converters."
39. US 10,854,945: (12/01/2020) Zhu, Kinget, "Circuits for wireless communication on multiple frequency bands."
40. US 11,050,457: (06/29/2021) Mangal, Kinget, "Circuits For Continuous-Time Clockless Analog Correlators"
41. US 11,281,957: (03/24/2022) Mangal, Kinget, "Systems, methods, and media for multi-antenna, directional backscatter tags"
42. US 11,374,599: (06/28/2022) Haque, Kinget, Bajor, "Circuits for Identifying Interferers using Compressed-Sampling"
43. US 11,402,458: (08/02/2022) Bajor, Wright, Haque, Kinget, "Circuits and Methods for Using Compressive Sampling to Detect Direction of Arrival of Signal of Interest"
44. US 11,705,932: (07/18/2023) Han, Kinget, Haque, "Circuits for Intermediate-Frequency-Filterless Double-Conversion Receivers"
45. US 11,791,854: (10/17/2023) Han, Kinget, Haque, "Circuits for Intermediate-Frequency-Filterless Double-Conversion Receivers"

U.S. Patent Applications:

1. US Patent Application: Kinget, Plouchart, "Systems and Methods for Providing Power to a Device under Test," November-14-2008 (abandoned).
2. US Patent Application: Yu, Kinget, "Multilayer Resonant Integrated Circuit with Distributed Capacitor," June-25-2009.
3. US Patent Application: Kuppambatti, Vigraham, Kinget, "Circuits, Methods and Media for Providing Delta-Sigma Modulators," Sept-29-2014 (abandoned).

4. US Patent Application: Seok, Kinget, Yang, Kim, "Circuits for Temperature Monitoring," Nov-03-2014.
5. US Patent Application: Zhu, Kinget, "Circuits for field-programmable receiver front ends," May-11-2016.
6. US Patent Application: Bajor, Wright, Haque, Kinget, "Circuits and methods for using compressive sampling to detect direction of arrival of a signal of interest," May-22-2019.
7. US Patent Application: Mangal, Kinget, "Circuits and methods for wake-up receivers," Jan-6-2020.

Several filed but not yet published.

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- Peter Kinget and Michiel Steyaert, Analog VLSI integration of massive parallel signal processing systems, Kluwer Academic Publishers, ISBN 0-7923-9823-8, 1996.
- S. Chatterjee, K.P. Pun, N. Stanic, Y. Tsvividis, and P. Kinget, Analog Circuit Design Techniques at 0.5V, Springer, ISBN 978-0-387-69953-0, 2007.
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90. Teng Yang, Karthik Tripurari, Harish Krishnaswamy and Peter R. Kinget, "A 0.5GHz-1.5GHz Order Scalable Harmonic Rejection Mixer," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2013.
91. Jianxun Zhu, Harish Krishnaswamy, and Peter Kinget "A DC-9.5GHz Noise-Canceling Distributed LNA in 65nm CMOS," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2013.
92. J. Kuppambatti and P. R. Kinget, "A Low Power Zero-Crossing Pipeline-SAR ADC with on-Chip Dynamically Loaded Pre-Charged Reference," European Solid-State Circuits Conference (ESSCIRC), Sept. 2013.
93. P. Kinget, B. Vigraham, J. Kuppambatti, C-W Hsu, "Scaling Analog Circuits," **plenary talk**, IEEE European Solid-State Circuits Conference, Sept. 2013.
94. C. Le, M. Kline, D. L. Gerber, S. R. Sanders, and P. R. Kinget, "A Stackable Switched-Capacitor DC/DC Converter IC for LED Drivers with 90% Efficiency," IEEE Custom Integrated Circuits Conference (CICC), Sept. 2013.
95. J. Kuppambatti, B. Vigraham and P. R. Kinget, "A 0.6V 70MHz 4th-Order Continuous-Time Butterworth Filter with 55.8dB SNR, 60dB THD at +2.8dBm Output Signal Power," IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2014.
96. J. Zhou, P.R. Kinget, and H. Krishnaswamy, "A Blocker-Resilient Wideband Receiver with Low-Noise Active Two-Point Cancellation of >0dBm TX Leakage and TX Noise in RX Band for FDD/Co-existence," IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2014.
97. T. Yang, S. Kim, P.R. Kinget, and M. Seok, "0.6-to-1.0V 279um², 0.92uW Temperature Sensor with Less Than +3.2/-3.4°C Error for On-Chip Dense Thermal Monitoring," IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2014.

98. S. Yang, B. Van Tassell, C. Le, S. Liu, E. S. Leland, D. A. Steingart, P. Kinget, S. O'Brien, I. Kymissis, "Metacapacitor: Large Area, Low Cost, High Performance Capacitors for Power Electronics", FlexTech Alliance Conference, Poster, Feb. 2014.
Received the "Student Poster Award 2nd Place."
99. Y. Xu, J. Zhu, and P.R. Kinget, "A Blocker-Tolerant RF Front End with Harmonic-Rejecting N-Path Filtering," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2014.
100. H. Krishnaswamy, K. Tripurari, Y. Xu, L. Zhang, D. Gidony, B. Jovanovic, and P. R. Kinget, "RF Channelizer Architectures using Iterative Downconversion for Concurrent or Fast-Switching Spectrum Analysis," **invited talk**, International Midwest Symposium on Circuits and Systems (MWSCAS), August 2014.
101. C-W. Hsu and P. R. Kinget, "A Supply-Scalable Differential Amplifier With Pulse-Controlled Common-Mode Feedback," IEEE Custom Integrated Circuits Conference (CICC), Sep. 2014
102. C-W. Hsu and P. R. Kinget, "A 40MHz 4th-order Active-UGB-RC Filter using VCO-Based Amplifiers with Zero Compensation," IEEE European Solid-State Circuits Conference (ESSCIRC), Sep. 2014.
103. T. Yang, D. Kim, P. R. Kinget, and M. Seok, "In-situ Techniques for In-field Sensing of NBTI Degradation in an SRAM Register File," IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2015.
104. R. Yazicigil, T. Haque, M. Whalen, J. Yuan, J. Wright, and P.R. Kinget, "A 2.7-3.7GHz Rapid Interferer Detector Exploiting Compressed Sampling with a Quadrature Analog-to-Information Converter," IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2015.
105. Y. Xu and P. R. Kinget, "A Switched-Capacitor RF Front End with Embedded Programmable High Order Filtering and a +15dBm OB-B1dB," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2015.
Received the "Best Student Paper Award – 2nd place"
106. J. Zhu and P.R. Kinget, "A Field-Programmable Noise-Canceling Wideband Receiver with High-Linearity Hybrid Class-AB-C LNTAs," IEEE Custom Integrated Circuits Conference (CICC), Sept. 2015.
Received the "Best Student Poster Award"
107. P.R. Kinget, "Scaling Analog Circuits into Deep Nanoscale CMOS: Obstacles and Ways to Overcome Them," **invited talk**, IEEE Custom Integrated Circuits Conference (CICC), Sept. 2015.
108. J. Zhu and P. R. Kinget, "A Very-Low-Noise Frequency-Translational Quadrature-Hybrid Receiver for Carrier Aggregation," IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2016.
109. R. Yazicigil, T. Haque, M. Kumar, J. Yuan, J. Wright, and P. R. Kinget, "Time-Segmented Quadrature Analog-to-Information Converter for Rapid Detection of up to 6 Interferers in the 2.7-3.7GHz PCAST Band," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2016.
110. R. Yazicigil, T. Haque, J. Zhu, Y. Xu, and P. R. Kinget, "RF Circuit and System Innovations for a New Generation of Wireless Terminals," IEEE International Symposium on Circuits and Systems (ISCAS), **invited talk**, Special Session on "Design Enhancements and Simulation Methods for Radio Frequency Circuits and Systems in Emerging Applications," May 2016.
111. Z. Dai, S. Gupta, S. Kalani and P. R. Kinget, "3.7 μ W 0.8V VCO-Integrator-Based High-Efficiency Capacitor-Free Low-Dropout Voltage Regulator," IEEE International Symposium on Circuits and Systems (ISCAS), May 2016.
112. S. Kalani, S. Nagam and P. R. Kinget, "Charge Pump Optimization and Output Spur Reduction in VCO-based OTAs for Active-RC Analog Filters," IEEE International Symposium on Circuits and Systems (ISCAS), May 2016.
113. S. Newton and P. R. Kinget, "A 4th-Order Analog Continuous-Time Filter Designed Using Standard Cells and Automatic Digital Logic Design Tools," IEEE International Symposium on Circuits and Systems (ISCAS), May 2016.
114. Y. Xu and P. R. Kinget, "A Chopping Switched-Capacitor RF Receiver with Integrated Blocker Detection, +31dBm OB-IIP3, and +15dBm OB-B1dB," IEEE Symposium on VLSI Circuits, June 2016.

115. T. Yang, P. R. Kinget, M. Seok, "Register File Circuits and Post-Deployment Framework to Monitor Aging Effects in Field," European Solid-State Circuits Conference (ESSCIRC), pp. 425-428, Sept. 2016.
116. R. T. Yazicigil, T. Haque, J. Wright and P. R. Kinget, "Band-Pass Compressive Sampling as an Enabling Technology for Rapid Wideband RF Spectrum Sensing," **invited paper**, 50th Asilomar Conference on Signals, Systems, and Computers, pp. 1032-1036, Nov. 2016.
117. R. Chandrasekaran, D. de Godoy, S. Xia, M. Islam, B. Islam, S. Nirjon, P. Kinget, X. Jiang, "Demo: SEUS - A Wearable Multi-Channel Acoustic Headset Platform to Improve Pedestrian Safety," Proceedings of the 14th ACM Conference on Embedded Network Sensor Systems, SenSys '16. Nov. 2016.
Recipient of the Best Demo – Runner Up Award
118. D. L. Gerber, M. Kline, S. R. Sanders., C. Le, P. R. Kinget, "An Integrated Multilevel Converter with Sigma Delta Control for LED Lighting," Applied Power Electronics Conference and Exhibition (APEC), pp. 2398-2403, March 2017.
119. T. Yang, J. Li, M. Yang, P. R. Kinget and Mingoo Seok, "An Area-Efficient Microcontroller with an Instruction-Cache Transformable to an Ambient Temperature Sensor and a Physically Unclonable Function," IEEE Custom Integrated Circuits Conference (CICC), May 2017.
120. V. Mangal and P. R. Kinget, "An Ultra-Low-Power Wake-Up Receiver with Voltage-Multiplying Self-Mixer and Interferer-Enhanced Sensitivity," IEEE Custom Integrated Circuits Conference (CICC), pp. 1-4, May 2017.
121. S. Nagam and P. R. Kinget, "A -236.3dB FoM Sub-Sampling Low-Jitter Supply-Robust Ring-Oscillator PLL for Clocking Applications with Feed-Forward Noise-Cancellation," IEEE Custom Integrated Circuits Conference (CICC), pp. 1-4, May 2017.
- 122. Outstanding Student Paper – Runner up**
123. S. Kalanni, A. Bertolini, A. Richelli and P. R. Kinget, "A 0.2V 492nW VCO-based OTA with 60kHz UGB and 207 μ VRMS noise," IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1-4, May 2017.
124. T. Haque, M. Bajor, Y. Zhang, J. Zhu, Z. Jacobs, R. Kettlewell, J. Wright and P.R. Kinget, "A Direct RF-to-Information Converter for Reception and Wideband Interferer Detection Employing Pseudo-Random LO Modulation," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2017, pp. 268-271.
125. Y. Zhang, J. Zhu and P. R. Kinget, "A Wideband Receiver with +32.5dBm Effective OB-IIP3 Using Baseband IM3 Cancellation," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2017, pp. 3-6.
126. M. Bajor, T. Haque, J. Wright, and P. R. Kinget, "Theory and Design of a Direct Space-to-Information Converter for Rapid Detection of Interferer DoA," IEEE 86th Vehicular Technology Conference (VTC2017-Fall), Sept. 2017.
127. A. R. Colon-Berrios, H. Edrees, C. McGinn, M. R. Cavallari, P. Kinget and I. Kymissis, "CMOS integrated ZnO thin film bulk acoustic resonator with Si₃N₄ susceptor layer for improved IR sensitivity," 75th Annual Device Research Conference (DRC), South Bend, IN, 2017, pp. 1-2.
128. T. Yang, P. K. Chundi, S. Kim, E. Kursun, M. Kim, P. R. Kinget, M. Seok, "Compact and Voltage-Scalable Sensor for Accurate Thermal Sensing in Dynamic Thermal Management," **invited talk**, International Midwest Symposium on Circuits and Systems (MWSCAS), August 2017, pp. 33-36.
129. A. R. Colon-Berrios, H. Edrees, D. de Godoy, P. Kinget and I. Kymissis, "Die-level processing for 3-D monolithic integration of piezoelectric MEMS on CMOS," IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), October 2017.
130. M. Seok, P. R. Kinget, T. Yang, J. Li and D. Kim, "Recent advances in in-situ and in-field aging monitoring and compensation for integrated circuits: Invited paper," *2018 IEEE International Reliability Physics Symposium (IRPS)*, March, 2018, pp. 5C.1-1-5C.1-6.
131. S. Nagam and P. R. Kinget, "A 0.008mm² 2.4GHz Type-I Sub-Sampling Ring-Oscillator-based Phase-Locked Loop with a -239.7dB FoM and -64dBc Reference Spurs," IEEE Custom Integrated Circuits Conference (CICC), April 2018. **Best Student Paper Award Finalist**

132. D. de Godoy, X. Jiang, and P. R. Kinget, "A 78.2nW 3-Channel Time-Delay-to-Digital Converter using Polarity Coincidence for Audio-based Object Localization," IEEE Custom Integrated Circuits Conference (CICC), April 2018.
133. D. de Godoy, B. Islam, S. Xia, M. Islam, R. Chandraskaran, Y. Chen, S. Nirjoh, P. Kinget, and F. Jiang, "PAWS: A Wearable Acoustic System for Pedestrian Safety," ACM/IEEE International Conference on Internet-of-Things Design and Implementation (IoTDI), April 2018.
134. D. de Godoy, S. Xia, W. Fernandez, X. Jiang, P. Kinget, "Demo: An Ultra-Low-Power Custom Integrated Circuit based Sound-Source Localization System," ACM/IEEE International Conference on Internet-of-Things Design and Implementation (IoTDI), April 2018.
Recipient of the Best Demo Award
135. S. Buchanan, T. Haque, P. Kinget, and J. Wright, "Efficient Model-Free Learning To Overcome Hardware Nonidealities In Analog-To-Information Converters," IEEE International Conference on Acoustics, Speech and Signal Processing (ICASP), April 2018, pp. 3574-3578.
136. S. Kalani, T. Haque, R. Gupta, and P. R. Kinget, "Using VCO-OTA TIAs to Break the Gain, Linearity and Power Consumption Trade-Offs in Passive Mixer Based Direct-Conversion Receivers," IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1-4, May 2018.
137. D. Basak, S. Kalani, P. Kinget, and K.P. Pun, "An On-Chip Static and Dynamic DAC Error Correction Technique for High Speed Multibit Delta- Sigma Modulators," IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1-4, May 2018.
138. M. Bajor, T. Haque, G. Han, C. Zhang, J. Wright and P. R. Kinget, "An 8-Element, 1-3GHz Direct Space-to-Information Converter for Rapid, Compressive-Sampling Direction-of-Arrival Finding Utilizing Pseudo-Random Antenna-Weight Modulation," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2018, pp. 116-119. **Best Student Paper Award – 3rd Place.**
139. V. Mangal, G. Atzeni and P. R. Kinget, "Multi-Antenna Directional Backscatter Tags," European Microwave Conference (EuMW), Madrid, Spain, Sept.'18, pp. 174-177.
140. G. Gangasani and P. R. Kinget, "A 19Gb/S RX for VSR-C2C Links with Clock-Less DFE and High-BW CDR Based on Master-Slave ILOs in 14nm CMOS," European Solid-State Circuits Conference (ESSCIRC), Sept. 2018, pp. 182-185.
141. J. Lombardi, F. Pearsall, N. Farahmand, B. Van Tassel, E. Leland, L. Huan, S. Liu, S. Yang, C. Le, I. Kymissis, P. Kinget, S. Sanders, D. Steingart, S. O'Brien, "Polymer-Nanocrystal Nanocomposite Capacitors and Their Applications in Energy Storage," IEEE Nanotechnology Materials and Devices Conference, 2018, pp. 1-4.
142. P. Kinget, "Compressed Sensing Based Radio Architectures for Rapidly Finding Interferers in the Spectral and Spatial Domains," 55th Annual AOC Symposium and Convention, Nov. 2018.
143. V. Mangal and P. Kinget, "A 0.42nW 434MHz -79.1dBm Wake-Up Receiver with a Time-Domain Integrator," International Solid-State Circuits Conference (ISSCC), Feb. 2019.
144. G. Gangasani and P. R. Kinget, "a 0.5V, 9GHz Sub-Integer Frequency Synthesizer Using Multi-Phase Injection-Locked Prescaler for Phase-Switching-Based Programmable Division with Automatic Injection-Lock Calibration in 45nm CMOS," International Symposium on Circuits and Systems (ISCAS), May 2019.
145. G. Han, T. Haque, M. Bajor, J. Wright and P. R. Kinget, "A 0.3-to-1.3GHz Multi-Branch Receiver with Modulated Mixer Clocks for Concurrent Dual-Carrier Reception and Rapid Compressive-Sampling Spectrum Scanning," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2019
146. V. Mangal and P. R. Kinget, "A -80.9dBm 450MHz Wake-Up Receiver with Code-Domain Matched Filtering using a Continuous-Time Analog Correlator," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2019.
147. T. Haque, G. Han, M. Bajor, J. Wright and P. R. Kinget, "Flexible Architectures for Concurrent Reception of Multiple RF Carriers and Compressed-Sampling Signal Detection in Frequency and Direction-of-Arrival," IEEE MTT-S International Microwave Conference on Hardware and Systems for 5G and beyond (IMC-5G), Aug. 2019.

148. Z. Wang, Y. Zhang, Y. Onizuka, and P. R. Kinget, "A High Accuracy, Multi-Phase Injection-Locked, 8-Phase, 7GHz Clock Generator in 65nm with 7bit Phase Interpolators for High-Speed Data Links," International Solid-State Circuits Conference (ISSCC), Feb. 2021.
149. S. Nagam, Y. Fan, and P.R. Kinget, "Auxiliary Feed-Forward Noise Cancellation for a Generic Type-II Ring Oscillator PLL," International Symposium on Circuits and Systems (ISCAS), May 2021.
150. Z. Wang and P. R. Kinget, "A 65nm CMOS, 3.5-to-11GHz, Less-Than-1.45LSB-INLpp, 7b Twin Phase Interpolator with a Wideband, Low-Noise Delta Quadrature Delay-Locked Loop for High-Speed Data Links," International Solid-State Circuits Conference (ISSCC), Feb. 2022.
151. P. Barac, M. Bajor, and P. R. Kinget, "Compressive-Sampling Spectrum Scanning with a Beamforming Receiver for Rapid, Directional, Wideband Signal Detection," IEEE 95th Vehicular Technology Conference (VTC2022), June 2022.
152. S. Ray and P. R. Kinget, "A 31-Feature, 80nW, 0.53mm² Audio Analog Feature Extractor based on Time-Mode Analog Filterbank Interpolation and Time-Mode Analog Rectification," IEEE Symposium on VLSI Circuits, June 2022.
153. M. Bajor, R. Li, C. Pappas, E. Olsen, J. Sucec, P. Barac, P. Kinget, and S. Pizzo, "High-Speed Sensing of the Electromagnetic (EM) Environment for Cognitive Radio Receivers," 12th Annual Gnu Radio Conference, Washington, D.C., Sept. 2022
154. R. Xu, J. Ban, S. Kalani, C. Hsu, S. Ray, B. Kirby, G. Matos, J. Gonski, A. Smith, D. Panchal, M. Unanian, X. Yang, N. Sun, J. Parsons, T. Andeen, and P. Kinget, "COLUTA: Custom 8-Channel 15-bit 40-MSPS ADC for the ATLAS Liquid Argon Calorimeter Readout," IEEE Nuclear Science Symposium and Medical Imaging, Nov. 2022
155. P. Barac, M. Bajor, R. Li, C. Pappas, and P. R. Kinget, "High-Speed Compressive Sensing-Based Spectral and Angular Sensing with a Dual Mode Hardware Architecture", GOMACTech, March 2023
156. S. Ray, X. Sun, N. Tremmel, M. Gordiyenko, and P. Kinget, "How Tiny Can Analog Filterbank Features Be Made for Ultra-low-power On-device Keyword Spotting?" tinyML Research Symposium, March 2023
157. P. Barac, M. Bajor, and P. R. Kinget, "A Beamforming Receiver Using a Time-Modulated LO-Path Vector Modulator Achieving Amplitude and Phase Control with 0.2 dB RMS Gain Error and 1.4 Degree RMS Phase Error," IEEE Custom Integrated Circuits Conference (CICC), pp. 1-4, April 2024
158. Z. Wang, H. Jiang, and P. R. Kinget, "A Digital Pre-Distortion Technique for High-Linearity, Low-Power, Compact Phase Interpolators," International Symposium on Circuits and Systems (ISCAS), pp. 1-4, May 2024.
159. R. Xu, E. Raguzin, S. Mandal, G. Deptuch, and P. R. Kinget, "Cryogenic Characterization of a 5-6 GHz LC VCO for CMOS-Quantum Co-Integration," IEEE Quant. Comp. and Eng. Conf., *accepted for presentation*, Sept. 2024.

Professional Society Magazines

- P. Kinget, "Teaching IC Design: From Concepts to Testing a Fabricated Custom Chip [Society News]," IEEE Solid-State Circuits Magazine, vol. 15, no. 3, pp. 87–93, 2023, doi: 10.1109/MSSC.2023.3283976.

Conference Sessions & Forums

- May 22 2000, Custom Integrated Circuits Conference (Orlando, FL), co-chaired session 8 "Low-Power Low-Voltage Wireless Systems."
- May 24 2000, Custom Integrated Circuits Conference (Orlando, FL), chaired session 25 "Oscillators, PLLs and Applications."
- May 7 2001, Custom Integrated Circuits Conference (San Diego, CA), chaired session 10 "Frequency Synthesizers and VCOs."
- June 17 2004, Symposium on VLSI Circuits (Honolulu, HI); chaired session "Frequency synthesizers and oscillators."

- June 17 2004, Symposium on VLSI Circuits (Honolulu, HI); chaired session “RF Circuit Techniques.”
- October 4 2004, Custom Integrated Circuits Conference (Orlando, FL), co-chaired session 25 “Broadband circuits and frequency synthesis.”
- June 16 2005, Symposium on VLSI Circuits (Kyoto, Japan); co-chaired session 8 “Analog Techniques.”
- June 17 2005, Symposium on VLSI Circuits (Kyoto, Japan); co-chaired session 12 “High Quality Audio Chips.”
- December 19 2005, IEEE International Conference on Electronic Devices and Solid-State Circuits (Hong Kong, SAR China) chaired session 3C “Ultra-wideband.”
- Feb. 15 2007, International Solid-State Circuits Conference, San Francisco, CA; co-organized and chaired the “Low-Voltage Analog Amplifier Design for Filtering and A/D Conversion” design forum.
- Sept. 13 2007, European Solid-State Circuits Conference (Munich, DE), co-chaired session C9L-F “High Speed Communications.”
- Feb. 7 2008, International Solid-State Circuits Conference, San Francisco, CA; co-organized the “Digitally Assisted Analog & RF Circuits” design forum.
- Feb. 12 2009, International Solid-State Circuits Conference, San Francisco, CA; co-organized the “Clock Synthesis Design” design forum.
- April 2025, IEEE Custom Integrated Circuits Conference (CICC) (Boston, MA); Luncheon Speaker: “MOSbius: Testing chips at the lunch table” (*upcoming*)

Conference Panels

- September 23 2003, IEEE Custom Integrated Circuits Conference 2003 (San Jose, CA): Organized and moderated the evening panel: “Are (analog) device models really that bad, or are they just a convenient excuse?”
- June 17 2004, IEEE Symposium on VLSI Circuits (Honolulu, Hawai'i, USA): Co-organized (with A. Matsuzawa) and Moderated the rump session: “Analog CAD: computer aided design, or, computer accelerated disasters?” (see Digest of Technical Papers Symposium on VLSI Circuits, 2004, June 2004, pp. 117)
- June 16 2005, IEEE Symposium on VLSI Circuits (Kyoto, Japan); Moderated the rump session “Digitizing the radio to the antenna. Will Radios still need analog in 2010?”
- September 20 2005, IEEE Custom Integrated Circuits Conference (CICC) (San Jose, CA); panelist for “Will Continued process-Node Shrinks Kill High-Performance Analog Design?”
- Sept. 17 2007, IEEE Custom Integrated Circuits Conference (CICC) (San Jose, CA); panelist for “Are analog designers hopeless at scaling? Will digital designers eat their lunch at 45nm and below?”
- Sept. 28 2015, IEEE Custom Integrated Circuits Conference (CICC) (San Jose, CA); panelist for “Impedance Mismatch between Academia and Industry”
- Feb. 2016, IEEE International Solid-State Circuits Conference (ISSCC) (San Francisco, CA); evening panelist for “Do We Need to Downscale Our Radios Below 20nm?”
- May 2 2017, IEEE Custom Integrated Circuits Conference (CICC) (Austin, TX); panelist for “Your Favorite Analog/Mixed-Signal/RF Circuits”
- April 2025, IEEE Custom Integrated Circuits Conference (CICC) (Boston, MA); panelist for “Do we really need a linear-gain amplifier anymore?” (*upcoming*)

Talks, Seminars & Webinars:

(Note: invited and plenary talks at conferences are included under ‘Publications in Refereed Proceedings’)

- February 1996, Stanford University (Stanford, CA), research seminar, “From Neurons to Upconversion.”

- February 1996, University of California Berkeley (Berkeley, CA), research seminar, "From Neurons to Upconversion."
- August 27 2002, Texas Instruments (Warren, NJ): "An injection locking scheme for precision quadrature generation."
- December 5 2002, University of California (Berkeley, CA): "An injection locking scheme for precision quadrature generation."
- December 5 2002, National Semiconductor (Santa Clara, CA): "An injection locking scheme for precision quadrature generation."
- January 14 2003, Second Annual New York State Conference on Microelectronics Design (Rochester, NY): "High Frequency, Integrated Oscillators."
- February 27 2003, IBM Research (Yorktown, NY): "High Frequency, Integrated Oscillators."
- May 19 2003, California Institute of Technology (Pasadena, CA): "An injection locking scheme for precision quadrature generation."
- September 19 2003, Silicon Laboratories (Austin, TX): "Current Research at the high speed analog and RF IC laboratory" and "An injection locking scheme for precision quadrature generation."
- September 26 2003, IBM Research (Yorktown Heights, NY): "Current Research at the high speed analog and RF IC laboratory" and "An injection locking scheme for precision quadrature generation."
- November 12 2003, Katholieke Universiteit Leuven (Leuven, Belgium); research seminar: "Current Research at the high speed analog and RF IC laboratory" and "An injection locking scheme for precision quadrature generation."
- April 22 2004, Philips Semiconductors (Fishkill, NY), "Analog and RF Integrated Circuits, Research Overview."
- March 17 2005, Massachusetts Institute of Technology (Cambridge, MA), Analog VLSI and Biological Systems Group Seminar: "0.5 V Analog Integrated Circuits for Nanoscale CMOS Technologies".
- March 18 2005, Harvard University (Cambridge, MA), Electrical Engineering Seminar: "0.5 V Analog Integrated Circuits for Nanoscale CMOS Technologies."
- April 8 2005, IMEC (Leuven, Belgium); Seminar: "0.5 V Analog Integrated Circuits for Nanoscale CMOS Technologies."
- May 24 2005, Toshiba Corp. (Yokohama, Japan), "Analog and RF IC Design Research, Overview."
- June 9 2005, Philips Semiconductors (Fishkill, NY), "Analog and RF Integrated Circuits Research using Philips' Qubic4plus."
- June 15 2005, Tokyo University (Tokyo, Japan); Seminar: "0.5 V Analog Integrated Circuits for Nanoscale CMOS Technologies."
- August 5 2005, Philips Research (Eindhoven, The Netherlands), "Analog and RF Integrated Circuits Research using Philips' Qubic4plus."
- October 17 2005, Broadcom Corporation (Irvine, CA): "0.5V Analog Integrated Circuits."
- December 14 2005, National Taiwan University (Taipei, Taiwan); IEEE SSCS Taipei Chapter Short Course "0.5 V Analog Integrated Circuits for Nanoscale CMOS Technologies."
- December 15 2005, Realtek Corp. (Hsinchu, Taiwan), "Ultra low voltage analog design techniques for nanoscale CMOS technologies."
- December 15 2005, National Tsing Hua University (Hsinchu, Taiwan), IEEE SSCS Taipei Chapter Short Course, "0.5 V Analog Integrated Circuits for Nanoscale CMOS Technologies."
- December 16 2005, UMC Corp. (Hsinchu, Taiwan), "Ultra low voltage analog design techniques for nanoscale CMOS technologies."
- May 30 2006, Ecole Polytechnique de Lausanne (EPFL) and The Western Switzerland Chapter on Solid State Circuits (Lausanne, Switzerland); seminar "0.5V Analog integrated circuits for nanoscale CMOS technologies."
- May 31 2006, Institut de Microélectronique, Electromagnétisme et Photonique, MINATEC, INPG, Institut National Polytechnique de Grenoble (Grenoble, France); seminar "0.5V Analog integrated circuits for nanoscale CMOS technologies."

- August 11 2006, Philips Research (Eindhoven, The Netherlands), "Analog and RF Integrated Circuits Research using Philips' Qubic4plus."
- Oct. 19 2006, University of Texas at Austin (Austin, TX); Analog and RF IC research seminar series, "0.5V Analog integrated circuits for nanoscale CMOS technologies."
- Oct. 20 2006, Silicon Laboratories (Austin, TX), "0.5V Analog integrated circuits for nanoscale CMOS technologies."
- Jan. 17 2007, University of Washington (Seattle, WA); Analog IC research seminar series, "0.5V Analog integrated circuits for nanoscale CMOS technologies."
- Jan. 18 2007, Oregon State University (Corvallis, OR); Analog IC research seminar series, "0.5V Analog integrated circuits for nanoscale CMOS technologies."
- January 19 2007, Intel Corporation (Hillsboro, OR); research seminar, "0.5V Analog integrated circuits for nanoscale CMOS technologies."
- April 19 2007, National Semiconductor (Santa Clara, CA); NSVL Distinguished Faculty Seminar, "Designing Analog and RF Circuits for Ultra-low Supply Voltages."
- April 19 2007, Marvell Technology Group (Santa Clara, CA): "Designing Analog and RF Circuits for Ultra-low Supply Voltages."
- April 19 2007, Stanford University (Stanford, CA); RAD seminar series, "Designing Analog and RF Circuits for Ultra-low Supply Voltages."
- April 19 2007, LSI Corp. (San Jose, CA): "Designing Analog and RF Circuits for Ultra-low Supply Voltages."
- April 20 2007, University of California at Berkeley (Berkeley, CA); Berkeley Wireless Research Center Seminars, "Designing Analog and RF Circuits for Ultra-low Supply Voltages."
- May 31 2007, CrystalMedia Technology (Milpitas, CA): "Designing Analog and RF Circuits for Ultra-low Supply Voltages."
- August 10 2007, Analog Devices Inc. (Wilmington, MA): "Designing Analog and RF Circuits for Ultra-low Supply Voltages."
- Oct. 1 2007, Massachusetts Institute of Technology (Cambridge, MA), Dept. of Electrical Engineering: "Designing Analog and RF Circuits for Ultra-low Supply Voltages."
- Oct. 17 2007, IBM Corp., Research Division (Yorktown Heights, NY): "Designing Analog and RF Circuits for Ultra-low Supply Voltages."
- Jan. 17 2008, University of Toronto and IEEE Toronto Section (Toronto, CA): "Designing Analog and RF Circuits for Ultra-low Supply Voltages."
- Jan. 18 2008, University of Toronto Engineering Science Education Conference (Toronto, CA), "Moore's Law and Integrated Analog and RF Circuits."
- Feb. 7 2008, Qualcomm Corp. (Campbell, CA): "Designing Analog and RF Circuits for Ultra-low Supply Voltages."
- April 2 2008, Special Symposium 'From Signal to Information Displayed in a Wireless World', Columbia University Science & Technology Ventures (New York, NY): "Self-powered wireless sensor systems" (with John Kymissis).
- May 29 2008, Silicon Laboratories (Austin, TX): "Current Research In RF IC Design: From Ultra-Low Voltage To Ultra-Wideband."
- June 23 2008, Dimes colloquium, Technical University of Delft (Delft, The Netherlands): "Designing Analog and RF Circuits for Ultra-low Supply Voltages."
- June 24, 2008, IMEC Holst Centre (Eindhoven, The Netherlands): "Analog and RF IC Design Research: From Ultra-low Voltage to Ultra-wideband."
- July 8, 2008, LETI-Minatec (Grenoble, France): "Designing Analog and RF Circuits for Ultra-low Supply Voltages."
- July 8, 2008, ST-Microelectronics (Grenoble, France): "Designing Analog and RF circuits for Ultra-low Supply Voltages: Inductor-less Receivers and Ultra-small PLLs in ST's 45nm CMOS."
- July 23, 2009, Thomson Labs (Paris, France): "Energy Harvesting Active Networked Tags."
- July 28, 2009, University of Bordeaux (Bordeaux, France): "Designing Analog and RF Circuits in Nanoscale CMOS Technologies: Scale the Supply, Reduce the Area and Use Digital Gates."

- Sept. 17, 2009, **IEEE SSCS Distinguished Lecture**, Inaugural meeting of the Princeton/Central Jersey SSCS Chapter at Rutgers University (Piscataway, NJ): "Designing Analog and RF Circuits in Nanoscale CMOS Technologies: Scale the Supply, Reduce the Area and Use Digital Gates."
- Sept. 22, 2009, **IEEE SSCS Distinguished Lecture**, Dept. of Electronic Engineering, Chinese University of Hong Kong and IEEE EDS/SCSS Hong Kong Chapter (Hong Kong SAR): "Designing Analog and RF Circuits in Nanoscale CMOS Technologies: Scale the Supply, Reduce the Area and Use Digital Gates."
- Sept. 24, 2009, **IEEE SSCS Distinguished Lecture**, National Taiwan University and IEEE SSCS Taipei Chapter (Taipei, Taiwan): "Designing Analog and RF Circuits in Nanoscale CMOS Technologies: Scale the Supply, Reduce the Area and Use Digital Gates."
- Nov. 8, 2009, **IEEE SSCS Distinguished Lecture**, Tel Aviv University and IEEE SSCS Israel Chapter (Tel Aviv, Israel): "Short Course: Designing Analog and RF Circuits for Ultralow Supply Voltages"
- Nov. 11, 2009, Research Seminar Technion (Haifa, Israel): "Designing Analog and RF Circuits in Nanoscale CMOS Technologies: Scale the Supply, Reduce the Area and Use Digital Gates."
- Nov. 20, 2009, Research Seminar University of Texas at Dallas, TxACE Texas Analog Center of Excellence (Dallas, TX): "Designing Analog and RF Circuits in Nanoscale CMOS Technologies: Scale the Supply, Reduce the Area and Use Digital Gates."
- February 4, 2010, Electrical and Computer Engineering Seminar, Carnegie Mellon University (Pittsburgh, PA): "Designing Analog and RF Circuits in Nanoscale CMOS Technologies: Scale the Supply, Reduce the Area and Use Digital Gates."
- March 8, 2010, **IEEE SSCS Distinguished Lecture**, Benelux IEEE Solid-State Circuits Society Chapter and IMEC (Leuven, Belgium): "Designing Analog and RF Circuits in Nanoscale CMOS Technologies: Scale the Supply, Reduce the Area and Use Digital Gates."
- May 20, 2010, ICS Seminar, University of Texas at Austin (Austin, TX): "Enhancing RF Receivers using Interference Cancellation and Digital Assistance."
- Jan. 15, 2011, **IEEE SSCS Distinguished Lecture**, IIT Delhi IEEE Circuits and Systems Society Chapter (Delhi, India): "Advanced Design Techniques for Integrated Voltage Controlled Oscillators."
- March 17, 2011, Seminar in Electronics and Communications, Université catholique de Louvain (Louvain-la-neuve, Belgium): "Nanoscale CMOS: Challenges and Opportunities for Cyber Physical/Bio Systems."
- June 23, 2011, Research Seminar, ST Microelectronics (Grenoble, France): "Enhancing RF Receivers using Interference Cancellation and Digital Assistance."
- July 14, 2011, Research Seminar at NXP Research, NXP (Eindhoven, The Netherlands): "Enhancing RF Receivers using Interference Cancellation and Digital Assistance."
- April 26, 2012, Research Seminar at the Advanced Design Group, Intel Corporation (Hillsboro, Oregon): "Voltage scaling trade-offs in VCOs and PLLs."
- April 27, 2012, Research Seminar, Silicon Laboratories (Austin, Texas): "Ultra low power, short range wireless communications: from using RF pulses to ultrasound clicks."
- July 17, 2012, Research Seminar, Ansem N.V. (Heverlee, Belgium): "Ultra low power, short range wireless communications: from using RF pulses to ultrasound clicks."
- July 25, 2012, Research Seminar, NXP Research and IMEC Holst Centre (Eindhoven, The Netherlands): "Ultra low power, short range wireless communications: from using RF pulses to ultrasound clicks."
- October 24, 2012, Research Seminar, Kilby Labs, Texas Instruments (Dallas, TX): "Ultra low power, short range wireless communications: from using RF pulses to ultrasound clicks."
- January 9, 2013, Research Seminar, Silicon Laboratories (Austin, Texas): "Power and Area-Efficient Reference Charging Techniques for Pipeline ADCs."
- March 5, 2013, Remote Research Seminar, ST Microelectronics (Noida, Delhi, India): "Trends in CMOS Technologies: An Analog Designer's Perspective."
- July 16, 2013, Research Seminar, Broadcom Corporation (Bunnik, The Netherlands): "Power and Area-Efficient Reference Charging Techniques for Pipeline ADCs."
- July 26, 2013, Research Seminar, IMEC Holst Centre (Eindhoven, The Netherlands): "Ultra low power, short range wireless communications: from using RF pulses to ultrasound clicks."

- July 26, 2013, Research Seminar, NXP Semiconductors (Eindhoven, The Netherlands): “Power and Area-Efficient Reference Charging Techniques for Pipeline ADCs.”
- November 22, 2013, Research Seminar, Silicon Laboratories (Austin, Texas): “Scaling Analog Circuits.”
- December 4, 2013, Keynote for the Honorary Professorship of M. Pelgrom at the Sint-Barbara Festival at the K.U.Leuven Engineering and Applied Sciences School (Leuven, Belgium): “The Perfect Match: Why It Matters for Transistors.”
- March 19, 2014, Microelectronics Colloquium, T.U. Delft, (Delft, The Netherlands): “Scaling Analog and RF Circuits: Why and How.”
- April 2, 2014, Distinguished Lecture, University of Texas at Austin, (Austin, Texas): “Scaling Analog and RF Circuits: Why and How.”
- April 11, 2014, Invited Lecture, Workshop on “Connected, Autonomous Systems” organized by NY EDS/SSCS Chapter, (New York, NY): “Ultra low power, short range wireless communications: from using RF pulses to ultrasound clicks.”
- August 20, 2014, Research Seminar, NXP Semiconductors (Leuven, Belgium): “Ultra Low Power, Short Range Wireless Communications: From Using RF Pulses To Ultrasound Clicks.”
- September 20, 2014, Invited Lecture, 2014 IEEE North Jersey Advanced Communications Symposium (Hoboken, NJ): “Ultra Low Power, Short Range Wireless Communications: From Using RF Pulses To Ultrasound Clicks.”
- November 12, 2014, Research Seminar, United Microelectronics (Hsin-Chu, Taiwan): “Scaling Analog and RF Circuits: Why and How”
- November 12, 2014, Research Seminar, VIA Telecom (Taipei, Taiwan): “Scaling Analog and RF Circuits: Why and How”
- November 13, 2014, Distinguished Lecture, Dept. of Electrical Engineering, National Taiwan University (Taipei, Taiwan): “Scaling Analog and RF Circuits: Why and How”
- April 30, 2015, **IEEE SSCS Distinguished Lecture**, IEEE Solid-State Circuits Society Santa Clara Valley Chapter, (Santa Clara, CA): “Scaling Analog Circuits: Why and How”
- May 27, 2015, University Seminar Series Lecture, Global Foundries (Malta, NY): “Scaling Analog and RF Circuits: Why and How”
- July 10 2015, Research Seminar, Silicon Laboratories (Austin, Texas): “RF Circuit and System Innovations for a New Generation of Wireless Terminals”
- January 11 2016, **IEEE SSCS Distinguished Lecture**, IEEE Solid-State Circuits Webinar: “Scaling Analog Circuits: Why and How”
- May 20 2016, **IEEE SSCS Distinguished Lecture**, IEEE Solid-State Circuits Society Boston Chapter, (Massachusetts Institute of Technology, Boston, MA): “Scaling Analog Circuits: Why and How”
- July 28 2016, **IEEE SSCS Distinguished Lecture**, IEEE Solid-State Circuits Society Benelux Chapter, (Katholieke Universiteit Leuven, Belgium): “Scaling Analog Circuits: Why and How”
- September 29 2016, Research Seminar, Silicon Laboratories (Austin, Texas): “Frequency Translational Quadrature Hybrid Receivers for Carrier Aggregation”
- October 31 2016, **IEEE SSCS Distinguished Lecture**, IEEE Solid-State Circuits Society Macau Chapter, (Macau, SAR, China): “RF Circuit and System Innovations to Enable a New Generation of Wireless Terminals: Field programmability, Ultra-high Linearity, and Compressive Spectrum Scanning”
- March 29 2017, **IEEE SSCS Distinguished Lecture**, IEEE Solid-State Circuits Society Ireland Chapter, (Tyndall Institute, Cork, Ireland): “RF Circuit and System Innovations to Enable a New Generation of Wireless Terminals: Field programmability, Ultra-high Linearity, and Compressive Spectrum Scanning”
- November 4 2017, Research Seminar, Silicon Laboratories (Austin, Texas): “Ambient-Aware Receiver Systems for Next Generation Shared Spectrum Access Deployments”
- August 9 2018, Invited Talk, IEEE Solid-State Circuits Society Benelux Chapter, (Katholieke Universiteit Leuven, Belgium): “Ambient-Aware Receiver Systems for Next Generation Shared Spectrum Access Deployments—or—How to Leverage Compressed Sampling in RF Scanners”

- October 17 2018, Invited Talk, Naval Research Laboratory, (Washington, DC): "Compressed Sensing Based Radio Architectures for Rapidly Finding Interferers in the Spectral and Spatial Domains"
- November 29 2018, Invited Talk, US Army CERDEC Lab, (Aberdeen, Maryland): "Compressed Sensing Based Radio Architectures for Rapidly Finding Interferers in the Spectral and Spatial Domains"
- March 8 2019, Research Seminar, Silicon Laboratories (Austin, Texas): "A 420 picoWatt Wake-Up Receiver; Are you serious?"
- April 24 2019, Electrical and Systems Engineering Seminar, Department of Electrical and Systems Engineering, University of Pennsylvania (Philadelphia, Pennsylvania): "Connecting Bits to the Physical World"
- July 2 2019, Research Seminar in 'ATX - TechTalk Tuesdays,' Cirrus Logic (Austin, Texas), "Connecting Bits to the Physical World"
- August 20 2019, Invited Talk, IEEE Solid-State Circuits Society Benelux Chapter, (Katholieke Universiteit Leuven, Belgium): "A 420 picoWatt Wake-Up Receiver; Are you serious?"
- September 26 2019, Distinguished Lecture, Department of Electrical and Computer Engineering, Boston University (Boston, MA): "Connecting Bits to the Physical World"
- November 21 2019, IEEE SSCS/CASS Atlanta Joint Chapter Seminar, Department of Electrical and Computer Engineering, Georgia Institute of Technology (Atlanta, GA): "Connecting Bits to the Physical World"
- December 12 2019, Semiconductor Research Corporation (SRC), Workshop on New Trajectories for Analog Electronics, IBM Research, (Almaden, CA): "The World is Analog – Future Challenges"
- December 11, 2020, Research Seminar (remote), Silicon Laboratories (Austin, Texas): "A High Accuracy, Multi-Phase Injection-Locked, 8-Phase, 7GHz Clock Generator in 65nm with 7bit Phase Interpolators for High-Speed Data Links"
- Jan 23 2022, Research Seminar (remote), Silicon Laboratories (Austin, Texas): "A Very High Linearity Twin Phase Interpolator with a Low-Noise, Wideband Delta Quadrature DLL for High-Speed Data-Link Clocking"

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CERTIFICATE OF SERVICE

I, Lanta M. Chase, hereby certify that on December 23, 2024 I caused a copy of the foregoing, **COMPLAINANTS' MARKMAN BRIEF**, to be filed and served upon the following parties as indicated below:

The Honorable Lisa R. Barton Secretary U.S. International Trade Commission 500 E Street, S.W. Washington, DC 20436	☒ Via Electronic Filing ☐ Via Hand Delivery (2 Copies) ☐ Via Overnight Delivery ☐ Via Facsimile
The Honorable MaryJoan McNamara Administrative Law Judge U.S. International Trade Commission 500 E Street, S.W., Room 317 Washington, DC 20436	☐ Via Hand Delivery (2 Copies) ☐ Via Overnight Delivery ☐ Via Facsimile ☒ Via Electronic Mail McNamara337@usitc.gov
Linda Chang, Esq. Office of Unfair Import Investigations U.S. International Trade Commission 500 E Street, S.W., Room 401 Washington, DC 20436	☐ Via Hand Delivery (2 Copies) ☐ Via Overnight Delivery ☐ Via Facsimile ☒ Via Electronic Mail: Linda.chang@usitc.gov
Timothy R. Shannon (Lead Counsel) Duane Morris LLP 100 High Street, Suite 2400 Boston, MA 02110 <i>Counsel for Kangxi Communication Techs (Shanghai) Co., Ltd. and Grand Chip Labs, Inc.</i>	☐ Via Hand Delivery (2 Copies) ☐ Via Overnight Delivery ☐ Via Facsimile ☒ Via Electronic Mail: DM_KCT_ITC_1413@duanemorris.com FM-KCT-1413@fostermurphy.com
S. Alex Lasher (Lead Counsel) Quinn Emanuel Urquhart & Sullivan, LLP 1300 I Street NW, Suite 900 Washington, DC 20005 <i>Counsel for Ruijie Networks Co., Ltd.</i>	☐ Via Hand Delivery (2 Copies) ☐ Via Overnight Delivery ☐ Via Facsimile ☒ Via Electronic Mail: alexlasher@quinnemanuel.com qeruijie@quinnemanuel.com

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/s/ Lanta M. Chase
Lanta M. Chase