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16 **UNITED STATES DISTRICT COURT**
17 **CENTRAL DISTRICT OF CALIFORNIA**
18 **SOUTHERN DIVISION**

19 SKYWORKS SOLUTIONS, INC.,

20 Plaintiff,

21 v.

22 KANGXI COMMUNICATION
TECHNOLOGIES (SHANGHAI)
23 CO., LTD., AND GRAND CHIP
LABS, INC.,

24 Defendants.
25
26
27
28

CASE NUMBER: 8:24-cv-00974

**COMPLAINT FOR PATENT
INFRINGEMENT**

JURY TRIAL DEMANDED

NATURE OF THE ACTION

1
2 1. Plaintiff Skyworks Solutions, Inc. (“Skyworks”) brings this Complaint
3 in the Central District of California (the “District”) against Defendants Kangxi
4 Communication Technologies (Shanghai) Co., Ltd., (“KXComTech”) and Grand
5 Chip Labs, Inc. (“GCLI”) (collectively, “KCT” or the “KCT Defendants”) for
6 infringement of United States Patent Nos. 8,717,101 (the “’101 patent”), 9,917,563
7 (the “’563 patent”), 9,450,579 (the “’579 patent”), and 9,148,194 (the “’194 patent”)
8 (collectively, the “Asserted Patents”).

THE PARTIES

A. Skyworks

10
11 2. Skyworks is a California Corporation with its principal place of
12 business at 5260 California Avenue, Irvine, California 92617. Skyworks is
13 renowned in the wireless semiconductor industry for its innovative approach to radio
14 frequency and semiconductor system design. It is a worldwide leader in the Wi-Fi
15 front-end-module (“FEM”) industry based in part on the success of its strong and
16 long-standing investments in research and development right here in California and
17 throughout the United States. Wi-Fi is a family of wireless network protocols based
18 on the Institute of Electrical and Electronics Engineers (“IEEE”) 802.11 series of
19 standards. Skyworks provides innovative Wi-Fi FEM chips that are used in a wide
20 array of products that play critical roles in the U.S. economy, including in enabling
21 reliable Wi-Fi connectivity for the network of wireless devices that power today’s
22 economy and infrastructure.

23 3. Skyworks’ technology enables everything from daily essentials like
24 smartphones, computers, and Internet of Things (IoT) devices to societal necessities
25 like lifesaving patient telemetry in hospitals, advanced security systems, and
26 industrial automation. Skyworks’ technology also serves the aerospace and national
27 defense sectors, among others.

1 4. As one of the largest producers of Wi-Fi FEMs in the world (Ex. 1
2 [Mordor Intelligence Report] at 4), Skyworks is committed to developing innovative
3 solutions to meet the ever-evolving demands for wireless communication across
4 many industries. To that end, Skyworks spent more than \$600 million on research
5 and development in 2022 alone, for example, and it has been awarded more than
6 4,600 patents worldwide in recognition of its pioneering innovations. (Skyworks
7 Solutions, Inc., *2022 Annual Report*, [<https://perma.cc/LU9D-7TBQ>] at 83, 88.)

8 5. Skyworks employs thousands of scientists, engineers, and other
9 personnel in the United States, including at its numerous facilities right here in
10 California.

11 **B. The KCT Defendants**

12 6. Defendant KXComTech is a corporation organized under the laws of
13 the People’s Republic of China (“PRC”), with its principal place of business located
14 at 5th Floor, Building 10, No.399 Keyuan Road, Pudong New Area, Shanghai, PRC.

15 7. Established in 2014, KXComTech offers Wi-Fi FEM products
16 compliant with the Wi-Fi 6, 6E, and 7 protocols, among others. According to its
17 website, KXComTech was “founded by seasoned experts with global experience[]
18 in the field of RF chip design, application, production, and sales” and operates with
19 a mission to “provide wireless devices with faster speed, lower latency, higher
20 capacity and wider coverage for more complex and diversified network access
21 scenarios.” (KXComTech, *About Us*, [<https://perma.cc/ST82-V7TA>].)
22 KXComTech has stated publicly that “most of [its] R&D teams” have “overseas
23 work experience” at American semiconductor companies, like Skyworks. (Ex. 2
24 [KCT Press Release] (“Most of the R&D teams ... have overseas work experience
25 in RFAxis (acquired by Skyworks in 2016), RFMD (merged into Qorvo), Anadigics
26 and other internationally renowned RF front-end chip companies[.]”).)

27 8. KXComTech purports to work with distributors to sell its products in
28 the United States, China, and Taiwan. (KXComTech, *Distributors*,

1 [https://perma.cc/39JG-J7Y6].) It also sells its products directly in all three markets.
2 (KXComTech, *Sales Support*, [https://perma.cc/2PTT-F9XZ].)

3 9. On November 17, 2023, KXComTech was officially listed on the
4 Shanghai Stock Exchange's Science and Technology Innovation Board.
5 (KXComTech, *IPO Press Release*, [https://perma.cc/6D7X-VUU6].) According to
6 its public offering filings, KXComTech employs 156 people, has a market
7 capitalization of \$1.24 billion, and an enterprise value of \$1.16 billion.

8 10. GCLI is a corporation organized under Nevada law and domiciled in
9 California with a principal place of business at 14151 Newport Ave., Suite 204,
10 Tustin, CA 92780. (Ex. 3 [GCLI California Corporation Registration].) GCLI is a
11 wholly owned subsidiary of KXComTech. (KXComTech, *Sales Support*,
12 [https://perma.cc/2PTT-F9XZ].)

13 11. On information and belief, GCLI is directly controlled by KXComTech
14 and handles business development for and sales of KXComTech Wi-Fi FEM
15 products in the United States.

16 12. KCT has recently announced its intent to attempt to displace Skyworks
17 in the market for Wi-Fi FEM chips. (Wi-Fi Now, *Meet KXcomtech: On track to ship*
18 *hundreds of millions in Wi-Fi FEMs in 2022*, [https://perma.cc/R3R7-5B47].) For
19 instance, KCT advertises its products as being pin-to-pin compatible with Skyworks'
20 products (*see, e.g.*, Ex. 4 [KCT Product Roadmap Presentation] at 8-24), and has
21 publicly compared its products to Skyworks' products "in terms of linearity,
22 efficiency, noise figure, and other performance metrics" (KXComTech, *IPO Press*
23 *Release*, [https://perma.cc/6D7X-VUU6]). KCT chose to locate its United States
24 sales and marketing entity, GCLI, less than ten miles from Skyworks' corporate
25 headquarters. Moreover, KCT has intentionally targeted and continues to target
26 Skyworks' customers in an attempt to convince them to switch to purchasing Wi-Fi
27 FEMs from KCT, and to incorporate those KCT FEMs into their Wi-Fi enabled
28 products. KCT has engaged in this conduct despite knowledge of Skyworks' patent

1 portfolio generally and the Asserted Patents in particular. On information and belief,
 2 the Wi-Fi FEMs that KCT offers for sale to Skyworks' customers copy Skyworks'
 3 technology, including the technology covered by the Asserted Patents.

4 **JURISDICTION AND VENUE**

5 13. This is a civil action for patent infringement under the patent laws of
 6 the United States, 35 U.S.C. § 1 *et seq*, including 35 U.S.C. §§ 271, 281, 283, 284,
 7 and 285.

8 14. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§
 9 1331 and 1338(a).

10 **A. KXComTech**

11 15. KXComTech is subject to this Court's specific and general personal
 12 jurisdiction due at least to its substantial business in this State and District, including
 13 by regularly doing or soliciting business, engaging in other persistent conduct
 14 targeting residents of California and this District, and/or deriving substantial revenue
 15 from infringing goods offered for sale, sold, and imported vicariously through and/or
 16 in concert with its related entities, alter egos, intermediaries, agents, distributors,
 17 partners, subsidiaries, clients, customers, affiliates, and/or consumers.

18 16. For instance, GCLI is responsible for selling KXComTech's products
 19 to customers in the United States and for developing KXComTech's business in U.S.
 20 markets. GCLI is 100% owned by KXComTech (Wi-Fi Now, *David L. Recker*,
 21 [<https://perma.cc/AJT7-MDWU>] (identifying GCLI as a "[w]holly owned US
 22 subsidiary of KXcomtech")), and KXComTech's chairman, Dr. Ping Peng, is
 23 GCLI's corporate president, treasurer, and sole director (Ex. 5 [GCLI Corporate
 24 Registration]). GCLI is registered to do business in California and maintains its
 25 principal place of business in this District located at 14151 Newport Ave., Suite 204,
 26 Tustin. (Ex. 3 [GCLI California Corporation Registration].)

27 17. On information and belief, KXComTech also directs and authorizes the
 28 sale and distribution of infringing products in California, including in this District.

For instance, KXComTech's website lists an individual employed by GCLI as its General Representative of North America for sales. (KXComTech, *Sales Support*, [https://perma.cc/2PTT-F9XZ].) Further, KXComTech's website lists Disman Bakner as its United States distributor for the California market. (KXComTech, *Distributors*, [https://perma.cc/FYC6-XH8A].) On information and belief, KXComTech directs and authorizes both GCLI and Disman Bakner to distribute infringing products in California.

18. Venue is proper in this District as to KXComTech because it is a foreign corporation organized under the laws of the People's Republic of China, with a principal place of business in Shanghai, China. Because KXComTech is not a resident of the United States, it may be sued in any judicial district pursuant to 28 U.S.C. § 1391(c)(3).

B. GCLI

19. This Court has personal jurisdiction over GCLI because it is domiciled in California and lists its principal place of business in California. (Ex. 3 [GCLI California Corporation Registration].)

20. This Court also has personal jurisdiction over GCLI because it regularly transacts business in this District by, among other things, offering infringing products to customers, business affiliates, and partners located in the District. For instance, an individual employed by GCLI is listed on KXComTech's website as KXComTech's General Representative of North America for sales. (KXComTech, *Sales Support*, [https://perma.cc/2PTT-F9XZ].)

21. Venue is proper in this District as to GCLI pursuant to at least 28 U.S.C. §§ 1391(b)(1), 1391(b)(2), 1391(c)(2), 1391(d), and 1400(b) because GCLI is subject to personal jurisdiction in this District, has a regular and established place of business in this District, and has committed acts of infringement in this District. For example, GCLI lists its principal place of business as 14151 Newport Ave., Suite 204, Tustin, CA 92780, which is located in this District less than five miles from the

1 Ronald Reagan Federal Building and United States Courthouse. (Ex. 3 [GCLI
2 California Corporation Registration].)

3 **FACTUAL BACKGROUND**

4 **A. Technology Background**

5 22. The Asserted Patents relate to an innovative collection of technologies
6 for improving the performance and design of FEMs, including Wi-Fi FEMs. These
7 technologies relate to various aspects and features of FEMs, including power
8 amplifiers, low-noise amplifiers, and radio frequency switches.

9 23. Skyworks has been at the forefront of advancing wireless connectivity
10 technologies, and its commitment to innovation can be seen across all of its business
11 segments, including its Wi-Fi FEM product offerings.

12 24. Wi-Fi FEMs are integrated circuits contained in wireless routers (and
13 many other devices) that enable wireless communication with a user device (*e.g.*, a
14 computer or smartphone) so that the user device can transmit and receive
15 information with other systems, such as via the internet. Wi-Fi FEMs are typically
16 located between the wireless router's antenna and its transceiver and are generally
17 comprised of semiconductor components, including but not limited to, power
18 amplifiers, low noise amplifiers, and switches.

19 25. When a user device accesses the internet, it sends signals requesting
20 data and receives the data in response. When a user device uses Wi-Fi to request
21 access to the internet, it sends a wireless signal to the wireless router. The wireless
22 router processes the signal and passes it to the internet. When the internet responds,
23 the wireless router processes the response, determines which user device to send the
24 response to (if there are multiple user devices connected to the wireless router), and
25 wirelessly sends the response to the appropriate user device.

26 26. Proper wireless communication between a user device and a wireless
27 router requires transmission of strong and clear wireless signals. However, myriad
28 external factors can weaken or warp the signal during transmission. As a result,

1 signals received by a wireless router often need to be adjusted so that they can reach
2 their intended destination in a discernable fashion. This signal adjustment is
3 typically performed by the wireless router's Wi-Fi FEM. In addition, a wireless
4 router uses its Wi-Fi FEM to amplify signals for transmission.

5 27. For example, during the transmission of a wireless signal from the
6 wireless router to a user device, outside noise sources may disrupt the transmitted
7 signal. This disruption is commonly referred to as "interference," and it can decrease
8 the strength and quality of the signal sent from the wireless router to the user device.
9 To prevent this, the wireless router sends the signal from its transceiver to the Wi-Fi
10 FEM for adjustment for wireless transmission. The Wi-Fi FEM uses power
11 amplifiers to strengthen the signal without distorting it. This reduces the impact of
12 any interference the signal might experience during transmission so that a strong and
13 clear signal can be received by the user device.

14 28. Further, when the wireless router receives a signal from the user device,
15 factors such as the distance between the wireless router and the user device can
16 reduce the signal strength. To account for this, the wireless router uses the Wi-Fi
17 FEM for adjustment of the received wireless signal. The Wi-Fi FEM can use its
18 low-noise amplifier to both amplify the strength of the signal and isolate the signal
19 from interference. This ensures that the signal received by the wireless router is
20 strong enough for the wireless router to properly process and route.

21 29. The Asserted Patents reflect Skyworks' many years of dedication,
22 expertise, and investment in research and development related to Wi-Fi FEMs.
23 Designing Wi-Fi FEM chips that can keep pace with new wireless networking
24 capabilities has posed significant challenges for Wi-Fi FEM producers—especially
25 given the increasing need for smaller and more efficient chips. The technologies of
26 the Asserted Patents address these challenges by enhancing Wi-Fi FEM performance
27
28

1 in a power-efficient manner through use of improved circuitry associated with power
2 amplifiers and innovative RF switch systems.

3 **B. The Asserted Patents¹**

4 30. As set forth below, KCT has been and is still infringing the Asserted
5 Patents by making, using, offering for sale, selling, or importing RF FEMs that
6 practice the Asserted Patents, or by contributing to infringement or inducing others
7 to infringe. KCT's acts of infringement have occurred within this District and
8 elsewhere throughout the United States.

9 i) The '101 Patent

10 31. The '101 patent, entitled "Apparatus and methods for biasing power
11 amplifiers," was duly and legally issued on May 6, 2014, and has been in full force
12 and effect since its issuance. A true and correct copy of the '101 patent is attached
13 hereto as Exhibit 6.

14 32. Skyworks owns all rights to the '101 patent, including the full and
15 exclusive right to enforce the patent and seek all legal and equitable remedies for
16 infringement thereof.

17 33. The '101 patent relates generally to radio frequency ("RF") power
18 amplifier systems and methods for biasing of power amplifiers.

19 34. The '101 patent explains that prior art power amplifiers struggled to
20 granularly manage the "amplification of a RF signal," which is necessary because
21 "amplifying the RF signal to an incorrect power level can cause a wireless device to
22 transmit out of band." (Ex. 6 ['101 patent] at 1:28-30.) As such, the '101 patent
23

24
25 ¹ All non-technical descriptions of the Asserted Patents included in this Complaint
26 are presented to give a general background to the patents. Statements made in
27 connection with these non-technical descriptions are not intended nor should they be
28 used for purposes of patent claim construction. Skyworks presents these statements
subject to and without waiver of its right to argue that claim terms should be
construed in a particular way under claim interpretation jurisprudence and the
relevant evidence.

1 explains that there was a need for “improved power amplifier systems” and
2 “improving power amplifier biasing.” (*Id.* at 1:31-33.)

3 35. The ’101 patent addresses this problem, for example, through a “power
4 amplifier system” that may contain a “bias block [that] includes a time dependent
5 signal generator configured to shape an enable signal of the power amplifier to
6 generate a control current, a current amplifier configured to amplify the control
7 current to generate a correction current, and a primary biasing circuit configured to
8 generate a bias current for the power amplifier based at least partly on the correction
9 current.” (*Id.* at 1:37-46.) According to the ’101 patent, such a power amplifier
10 system “correct[s] for a variation in gain of the power amplifier when the power
11 amplifier is enabled” (*id.* at 1:46-48), which “can improve the power amplifier’s
12 performance” (*id.* at 4:39-42).

13 ii) The ’563 Patent

14 36. The ’563 patent, entitled “Apparatus and methods for biasing of power
15 amplifiers,” was duly and legally issued on March 13, 2018, and has been in full
16 force and effect since its issuance.² A true and correct copy of the ’563 patent is
17 attached hereto as Exhibit 7.

18 37. Skyworks owns all rights to the ’563 patent, including the full and
19 exclusive right to enforce the patent and seek all legal and equitable remedies for
20 infringement thereof.

21 38. The ’563 patent relates generally to RF power amplifier systems and
22 methods for biasing of power amplifiers.

23 39. The ’563 patent explains that prior art power amplifiers struggled to
24 granularly manage the “amplification of a RF signal,” which is important because
25 “amplifying the RF signal to an incorrect power level can cause a wireless device to
26

27 ² The ’563 patent is a continuation of U.S. patent application No. 14/825,053, which
28 is a continuation of U.S. patent application No. 14/242,150, which is a continuation
of U.S. patent application No. 13/468,749 that issued as the ’101 patent that
Skyworks asserts in this Complaint.

1 transmit out of band.” (Ex. 7 [’563 patent] at 1:38-41.) As such, the ’563 patent
2 explains that there was a need for “improved power amplifier systems” and
3 “improving power amplifier biasing.” (*Id.* at 1:42-44.)

4 40. The ’563 patent addresses this problem, for example, through a “power
5 amplifier system” that may contain a “bias block [that] includes a time dependent
6 signal generator configured to shape an enable signal of the power amplifier to
7 generate a control current, a current amplifier configured to amplify the control
8 current to generate a correction current, and a primary biasing circuit configured to
9 generate a bias current for the power amplifier based at least partly on the correction
10 current.” (*Id.* at 1:48-58.) According to the ’563 patent, such a power amplifier
11 system “correct[s] for a variation in gain of the power amplifier when the power
12 amplifier is enabled” (*id.* at 1:58-60), which “can improve the power amplifier’s
13 performance” (*id.* at 4:52-55). Additionally, the ’563 patent describes techniques to
14 arrange the components of its inventive power amplifier system in a way that can
15 allow “the magnitude of the components of the time-dependent signal generator [to]
16 be reduced to a size suitable for on-chip integration.” (*Id.* at 9:1-7.)

17 iii) The ’579 Patent

18 41. The ’579 patent, entitled “Radio frequency devices having reduced
19 intermodulation distortion,” was duly and legally issued on September 20, 2016, and
20 has been in full force and effect since its issuance.³ A true and correct copy of the
21 ’579 patent is attached hereto as Exhibit 8.

22 42. Skyworks owns all rights to the ’579 patent, including the full and
23 exclusive right to enforce the patent and seek all legal and equitable remedies for
24 infringement thereof.

25 43. The ’579 patent relates generally to “a radio-frequency (RF) switch
26 system” designed to reduce signal interference. (Ex. 8 [’579 patent] at 1:34-37.)
27

28 ³ The ’579 patent is a division of application No. 13/936,175, filed on July 6, 2013,
which issued as U.S. Patent No. 9,148,194.

1 44. The '579 patent explains that “mixing products from other RF signals”
2 can cause “an unwanted signal [to be] added to a desired signal” and that “[s]uch an
3 effect can be particularly dominant in a multi-mode, multi-band environment.” (*Id.*
4 at 9:2-5.) The '579 patent refers to the unwanted signal as “intermodulation
5 distortion” or “IMD” and notes that it can “yield frequencies that are not harmonic
6 frequencies.” (*Id.* at 9:5-7.) The '579 patent explains that this is problematic
7 because it “can contribute to the introduction of spurious signals into the RF system,
8 thereby contributing to degradation of overall RF system linearity and IMD
9 performance.” (*Id.* at 6:49-53.)

10 45. The '579 patent addresses this problem, for example, through an RF
11 device designed to reduce IMD. (*Id.* at Abstract.) The RF device may contain an
12 RF switch system that “includes a switch having a stack of field-effect transistors
13 (FETs) connected in series between first and second nodes” (*id.* at 1:34-37) and “a
14 capacitor connected in series with the switch configured to inhibit a low-frequency
15 blocker system from mixing with a fundamental-frequency signal in the switch” (*id.*
16 at 1:37-40). According to the '579 patent, this system can allow for “a low-
17 frequency jammer signal [to] be blocked or reduced from mixing with any ON or
18 OFF paths” (*id.* at 9:49-53), which can improve the “linearity of the system building
19 blocks,” leading to a decrease in “the overall susceptibility of a system to
20 interference” (*id.* at 9:9-14).

21 iv) The '194 Patent

22 46. The '194 patent, entitled “Radio-frequency switch system having
23 improved intermodulation distortion performance,” was duly and legally issued on
24 September 29, 2015, and has been in full force and effect since its issuance. A true
25 and correct copy of the '194 patent is attached hereto as Exhibit 9.

26 47. Skyworks owns all rights to the '194 patent, including the full and
27 exclusive right to enforce the patent and seek all legal and equitable remedies for
28 infringement thereof.

1 48. The '194 patent relates generally to “a radio-frequency (RF) switch
2 system” designed to reduce signal interference. (Ex. 9 ['194 patent] at 1:31-37.)

3 49. The '194 patent explains that “mixing products from other RF signals”
4 can cause “an unwanted signal [to be] added to a desired signal” and that “[s]uch an
5 effect can be particularly dominant in a multi-mode, multi-band environment.” (*Id.*
6 at 8:55-60.) The '194 patent refers to the unwanted signal as “intermodulation
7 distortion” or “IMD” and notes that it can “yield frequencies that are not harmonic
8 frequencies.” (*Id.*) The '194 patent explains that this is problematic because it “can
9 contribute to the introduction of spurious signals into the RF system, thereby
10 contributing to degradation of overall RF system linearity and IMD performance.”
11 (*Id.* at 6:38-44.)

12 50. The '194 patent addresses this problem through, for example, an RF
13 device designed to reduce IMD. (*Id.* at Abstract.) The RF device may contain an
14 RF switch system that “includes a switch having a stack of field-effect transistors
15 (FETs) connected in series between first and second nodes” (*id.* at 1:31-34) and “a
16 capacitor connected in series with the switch and configured to inhibit a low-
17 frequency blocker signal from mixing with a fundamental-frequency signal in the
18 switch” (*id.* at 1:34-37). According to the '194 patent, this system can allow for “a
19 low-frequency jammer signal [to] be blocked or reduced from mixing with any ON
20 or OFF paths,” which can “lead to improvement in IMD performance, especially for
21 low-frequency blocker signals.” (*Id.* at 9:35-38.)

22 51. As set forth below, KCT's Wi-Fi FEMs infringe the foregoing Asserted
23 Patents.

24 **COUNT I – INFRINGEMENT OF U.S. PATENT NO. 8,717,101**

25 52. Skyworks re-alleges and incorporates by reference the allegations of
26 the preceding paragraphs of this Complaint, as if fully set forth herein.

27 53. The '101 patent is valid and enforceable under the United States Patent
28 Laws.

1 54. In violation of 35 U.S.C. § 271, KCT has been and is still infringing,
2 directly or indirectly, literally or under the doctrine of equivalents, the '101 patent
3 by making, using, offering for sale, selling, or importing infringing Wi-Fi 6, 6E and
4 7 FEMs, including, but not limited to, the KCT8547HE, KCT8539S, KCT8239S,
5 and KCT8576HE Wi-Fi FEMs (the "Accused KCT Products").⁴

6 55. The Accused KCT Products infringe at least claims 1, 2, 10-11, 17, 18,
7 20, 21, and 22 of the '101 patent.

8 56. For instance, the Accused KCT Products infringe independent claims
9 1, 17, and 21 of the '101 patent for at least the reasons described in Skyworks'
10 exemplary infringement charts set forth as Exhibits 10-13.

11 57. With respect to claims 2 and 22, the Accused KCT Products further
12 contain a resistor-capacitor (RC) network in a time-dependent signal generator.
13 Thus, the Accused KCT Products infringe claims 2 and 22 of the '101 patent.

14 58. With respect to claim 10, the Accused KCT Products further contain a
15 bipolar transistor in a power amplifier. The bipolar transistor has an emitter, a base,
16 and a collector, the base configured to receive a radio frequency (RF) signal and a
17 bias current. Thus, the Accused KCT Products infringe claim 10 of the '101 patent.

18 59. With respect to claim 11, the bipolar transistor contained in Accused
19 KCT Products has an emitter electrically connected to a power low voltage. The
20 bipolar transistor has a collector configured to generate an amplified version of the
21 RF signal. Thus, the Accused KCT Products infringe claim 11 of the '101 patent.

22 60. With respect to claim 18, the Accused KCT Products further use a
23 resistor-capacitor (RC) network of a time-dependent signal generator. Thus, the
24 Accused KCT Products infringe claim 18 of the '101 patent.

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28 ⁴ Skyworks' infringement allegations regarding the '101 patent extend to all KCT
Wi-Fi FEMs embodying an infringing power amplifier system, including KCT Wi-
Fi 6, 6E, and 7 FEMs.

1 61. With respect to claim 20, when generating a bias current, the Accused
2 KCT Products further shape the bias current so as to compensate for a gain variation
3 of a transistor. On information and belief, the transistor is a heterojunction bipolar
4 transistor (HBT). Thus, the Accused KCT Products infringe claim 20 of the '101
5 patent.

6 62. KCT has had knowledge of the '101 patent at least since March 7, 2023,
7 when Skyworks sent a letter to KCT's President informing KCT that its 2.4 GHz
8 and 5 GHz Wi-Fi FEMs infringed the claims of certain Skyworks patents, including
9 (but not limited to) the '101 patent family, and including without limitation U.S.
10 Patent Nos. 9,136,803, 9,667,203, 9,917,563, and 10,566,943. (Ex. 14 [2023 Notice
11 Letter] at 1-2.) Skyworks met with KCT and gave a presentation outlining KCT's
12 infringement. Skyworks further sent a letter to KCT on April 23, 2024, providing
13 notice of KCT's infringement of each Asserted Patent, including the '101 patent.
14 (Ex. 15 [2024 KCT Notice Letter].) Despite receiving notice of its infringement,
15 KCT has continued to infringe Skyworks' patented technology, including the
16 technology claimed in the '101 patent, and made no effort to avoid infringement.
17 These actions demonstrate KCT's willful, blatant, and egregious disregard for
18 Skyworks' patent rights.

19 63. On information and belief, KCT actively, knowingly, and intentionally
20 has induced and continues to induce infringement of the '101 patent by, for example,
21 controlling the design and manufacture of, offering for sale, selling, supplying, and
22 otherwise providing instruction and guidance regarding the Accused KCT Products,
23 with the knowledge and specific intent to encourage and facilitate acts of direct
24 infringement with respect to such products, including by resellers, retailers, end
25 product manufacturers, and end users of the Accused KCT Products, both inside and
26 outside the United States. For example, KCT's website advertises the Accused KCT
27 Products as integrating "a high-efficiency high-linearity power amplifier (PA)" that
28 includes a "power detector" for "accurately monitoring [] output power from the

[power amplifier].” (KXComTech, *KCT8547HE-1*, [<https://perma.cc/7QFB-L3FW>]; KXComTech, *KCT8539S*, [<https://perma.cc/WRA7-GDPD>]; KXComTech, *KCT8576HE*, [<https://perma.cc/A72U-RFMF>]); *see also* KXComTech, *KCT8239S*, [<https://perma.cc/NS2E-VPYU>] (describing the KCT8239S product as “a fully integrated 802.11b/g/n/ac/ax WLAN RF Front-end module (FEM) which incorporates key RF functionality,” which is “integrated with a high-efficiency power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated matching network and a single-pole, double-throw (SPDT) switch all in one device”).) Further, KCT advertises the Accused KCT Products as being pin-to-pin compatible with Skyworks’ products. For instance, KCT’s product roadmap presentation published in the second quarter of 2023 indicated that the accused KCT8576HE product is pin-to-pin compatible with Skyworks’ SKY85746-11 product. (Ex. 4 [KCT Product Roadmap Presentation] at 13.) On information and belief, KCT sells and distributes infringing products to customers in the United States both directly and through third-party distributors like Disman Bakman. (KXComTech, *Sales Support*, [<https://perma.cc/2PTT-F9XZ>]; KXComTech, *Distributors*, [<https://perma.cc/FYC6-XH8A>].) On information and belief, KCT’s distributors, customers, and end users directly infringe the ’101 patent by, for example, making, using, offering to sell, and/or selling within the United States, and importing into the United States, without authority or license, both the Accused KCT Products themselves and/or products containing the Accused KCT Products.

64. KCT also contributes to infringement of the ’101 patent by selling for importation into the United States, importing into the United States, and/or selling within the United States after importation the Accused KCT Products, which are not suitable for substantial non-infringing use and which embody a material part of the invention described in the ’101 patent. These Accused KCT Products are known by KCT to be especially made or especially adapted for use in the infringement of the ’101 patent. Specifically, on information and belief, KCT sells the Accused KCT

1 Products to resellers, retailers, and end product manufacturers with knowledge that
2 such entities perform acts of direct infringement with the Accused KCT Products.
3 On information and belief, KCT sells and distributes infringing products to
4 customers in the United States both directly and through third-party distributors like
5 Disman Bakman. (KXComTech, *Sales Support*, [<https://perma.cc/2PTT-F9XZ>];
6 KXComTech, *Distributors*, [<https://perma.cc/FYC6-XH8A>].) On information and
7 belief, KCT's distributors, customers, and end users directly infringe the '101 patent
8 by, for example, making, using, offering to sell, selling within the United States,
9 and/or importing into the United States, without authority or license, both the
10 Accused KCT Products themselves and/or products containing the Accused KCT
11 Products.

12 65. As a result of KCT's infringement of the '101 patent, Skyworks has
13 been damaged. Skyworks is entitled to recover for damages sustained as a result of
14 KCT's wrongful acts in an amount to be proven at trial, and in no event less than a
15 reasonable royalty for the use made of the invention by KCT, together with interest
16 and costs as fixed by the Court.

17 66. In addition, KCT's infringing acts have caused and are causing
18 immediate and irreparable harm to Skyworks.

19 67. On information and belief, KCT's infringement of the '101 patent has
20 been and continues to be willful. For the reasons stated above, KCT has had
21 knowledge of the '101 patent and its infringement of the '101 patent since at least
22 March 7, 2023. Nevertheless, KCT has deliberately continued to infringe in a
23 wanton, malicious, and egregious manner, with reckless disregard for Skyworks'
24 patent rights. Thus, KCT's infringing actions have been and continue to be
25 consciously willful.

26 68. Based on the information alleged in this claim, Skyworks is informed
27 and believes, and thereon alleges, that this is an exceptional case—including because
28

1 of KCT's copying of the '101 patent in the Accused KCT Products—which warrants
2 an award of attorneys' fees to Skyworks pursuant to 35 U.S.C. § 285.

3 **COUNT II – INFRINGEMENT OF U.S. PATENT NO. 9,917,563**

4 69. Skyworks re-alleges and incorporates by reference the allegations of
5 the preceding paragraphs of this Complaint, as if fully set forth herein.

6 70. The '563 patent is valid and enforceable under the United States Patent
7 Laws.

8 71. In violation of 35 U.S.C. § 271, KCT has been and is still infringing,
9 directly or indirectly, literally or under the doctrine of equivalents, the '563 patent
10 by making, using, offering for sale, selling, or importing Wi-Fi 6, 6E and 7 FEMs
11 that infringe the '563 patent, including but not limited to the Accused KCT
12 Products.⁵

13 72. The Accused KCT Products infringe at least claims 14, 15, 17, and 20
14 of the '563 patent.

15 73. For instance, the Accused KCT Products infringe independent claim 14
16 of the '563 patent for at least reasons described in Skyworks' exemplary
17 infringement charts set forth as Exhibits 16-19.

18 74. With respect to claim 15, the Accused KCT Products further contain a
19 first transistor in a primary bias circuit. The Accused KCT Products' correction
20 current, as identified in the exemplary infringement charts for claim 14 (Exs. 16-19),
21 is configured to change a current flowing through the first transistor. Thus, the
22 Accused KCT Products infringe claim 15 of the '563 patent.

23 75. With respect to claim 17, the Accused KCT Products further contain a
24 current mirror in a gain correction circuit. The current mirror is configured to
25 generate the correction current by mirroring the control current as in claim 14. The
26

27
28 ⁵ Skyworks' infringement allegations regarding the '563 patent extend to all KCT
Wi-Fi FEMs embodying an infringing power amplifier system, including KCT Wi-
Fi 6, 6E, and 7 certified FEMs.

1 current mirror is further configured to receive a power amplifier enable signal. Thus,
2 the Accused KCT Products infringe claim 17 of the '563 patent.

3 76. With respect to claim 20, the Accused KCT Products further contain a
4 second transistor in a primary bias circuit. The second transistor is electrically
5 coupled to the first transistor as in claim 15. The second transistor is further
6 configured to provide a bias signal to a power amplifier. Thus, the Accused KCT
7 Products infringe claim 20 of the '563 patent.

8 77. KCT has had knowledge of the '563 patent at least since March 7, 2023,
9 when Skyworks sent a letter to KCT's President informing KCT that its 2.4 GHz
10 and 5 GHz Wi-Fi FEMs infringed the claims of certain Skyworks patents, including
11 (but not limited to), the '563 patent. (Ex. 14 [2023 Notice Letter] at 1-2.) Skyworks
12 met with KCT and gave a presentation outlining KCT's infringement. Skyworks
13 further sent a letter to KCT on April 23, 2024, providing notice of KCT's
14 infringement of each Asserted Patent, including the '563 patent. (Ex. 15 [2024 KCT
15 Notice Letter].) Despite receiving notice of its infringement, KCT has continued to
16 infringe Skyworks' patented technology, including the technology claimed in the
17 '563 patent, and made no effort to avoid infringement. These actions demonstrate
18 KCT's willful, blatant, and egregious disregard for Skyworks' patent rights.

19 78. On information and belief, KCT actively, knowingly, and intentionally
20 has induced and continues to induce infringement of the '563 patent by, for example,
21 controlling the design and manufacture of, offering for sale, selling, supplying, and
22 otherwise providing instruction and guidance regarding the Accused KCT Products,
23 with the knowledge and specific intent to encourage and facilitate acts of direct
24 infringement with respect to such products, including by resellers, retailers, end
25 product manufacturers, and end users of the Accused KCT Products, both inside and
26 outside the United States. For example, KCT's website advertises the Accused KCT
27 Products as integrating "a high-efficiency high-linearity power amplifier (PA)" that
28 includes a "power detector" for "accurately monitoring [] output power from the

[power amplifier].” (KXComTech, *KCT8547HE-1*, [<https://perma.cc/7QFB-L3FW>]; KXComTech, *KCT8539S*, [<https://perma.cc/WRA7-GDPD>]; KXComTech, *KCT8576HE*, [<https://perma.cc/A72U-RFMF>]); *see also* KXComTech, *KCT8239S*, [<https://perma.cc/NS2E-VPYU>] (describing the KCT8239S product as “a fully integrated 802.11b/g/n/ac/ax WLAN RF Front-end module (FEM) which incorporates key RF functionality,” which is “integrated with a high-efficiency power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated matching network and a single-pole, double-throw (SPDT) switch all in one device”).) Further, KCT advertises the Accused KCT Products as being pin-to-pin compatible with Skyworks’ products. For instance, KCT’s product roadmap presentation published in the second quarter of 2023 indicated that the accused KCT8576HE product is pin-to-pin compatible with Skyworks’ SKY85746-11 product. (Ex. 4 [KCT Product Roadmap Presentation] at 13.) On information and belief, KCT sells and distributes infringing products to customers in the United States both directly and through third-party distributors like Disman Bakman. (KXComTech, *Sales Support*, [<https://perma.cc/2PTT-F9XZ>]; KXComTech, *Distributors*, [<https://perma.cc/FYC6-XH8A>].) On information and belief, KCT’s distributors, customers, and end users directly infringe the ’563 patent by, for example, making, using, offering to sell, and/or selling within the United States, and importing into the United States, without authority or license, both the Accused KCT Products themselves and/or products containing the Accused KCT Products.

79. KCT also contributes to infringement of the ’563 patent by selling for importation into the United States, importing into the United States, and/or selling within the United States after importation the Accused KCT Products, which are not suitable for substantial non-infringing use and which embody a material part of the invention described in the ’563 patent. These Accused KCT Products are known by KCT to be especially made or especially adapted for use in the infringement of the ’563 patent. Specifically, on information and belief, KCT sells the Accused KCT

1 Products to resellers, retailers, and end product manufacturers with knowledge that
2 such entities perform acts of direct infringement with the Accused KCT Products.
3 On information and belief, KCT sells and distributes infringing products to
4 customers in the United States both directly and through third-party distributors like
5 Disman Bakman. (KXComTech, *Sales Support*, [<https://perma.cc/2PTT-F9XZ>];
6 KXComTech, *Distributors*, [<https://perma.cc/FYC6-XH8A>].) On information and
7 belief, KCT's distributors, customers, and end users directly infringe the '563 patent
8 by, for example, making, using, offering to sell, selling within the United States,
9 and/or importing into the United States, without authority or license, both the
10 Accused KCT Products themselves and/or products containing the Accused KCT
11 Products.

12 80. As a result of KCT's infringement of the '563 patent, Skyworks has
13 been damaged. Skyworks is entitled to recover for damages sustained as a result of
14 KCT's wrongful acts in an amount to be proven at trial, and in no event less than a
15 reasonable royalty for the use made of the invention by KCT, together with interest
16 and costs as fixed by the Court.

17 81. In addition, KCT's infringing acts have caused and are causing
18 immediate and irreparable harm to Skyworks.

19 82. On information and belief, KCT's infringement of the '563 patent has
20 been and continues to be willful. For the reasons stated above, KCT has had
21 knowledge of the '563 patent and its infringement of the '563 patent since at least
22 March 7, 2023. Nevertheless, KCT has deliberately continued to infringe in a
23 wanton, malicious, and egregious manner, with reckless disregard for Skyworks'
24 patent rights. Thus, KCT's infringing actions have been and continue to be
25 consciously willful.

26 83. Based on the information alleged in this claim, Skyworks is informed
27 and believes, and thereon alleges, that this is an exceptional case—including because
28

1 of KCT's copying of the '563 patent in the Accused KCT Products—which warrants
2 an award of attorneys' fees to Skyworks pursuant to 35 U.S.C. § 285.

3 **COUNT III – INFRINGEMENT OF U.S. PATENT NO. 9,450,579**

4 84. Skyworks re-alleges and incorporates by reference the allegations of
5 the preceding paragraphs of this Complaint, as if fully set forth herein.

6 85. The '579 patent is valid and enforceable under the United States Patent
7 Laws.

8 86. In violation of 35 U.S.C. § 271, KCT has been and is still infringing,
9 directly or indirectly, literally or under the doctrine of equivalents, the '579 patent
10 by making, using, offering for sale, selling, or importing Wi-Fi 6, 6E and 7 FEMs
11 that practice the '579 patent, including but not limited to the Accused KCT
12 Products.⁶

13 87. The Accused KCT Products infringe at least claims 1 and 7 of the '579
14 patent.

15 88. For instance, the Accused KCT Products infringe independent claims 1
16 and 7 of the '579 patent for at least the reasons described in Skyworks' exemplary
17 infringement charts set forth as Exhibits 20-23.

18 89. KCT has had knowledge of the '579 patent and its infringement of the
19 '579 patent at least since April 23, 2024, when Skyworks sent a letter to KCT
20 providing notice of KCT's infringement of each Asserted Patent, including the '579
21 patent. (Ex. 15 [2024 KCT Notice Letter].) Even before April 23, 2024, KCT was,
22 at a minimum, willfully blind to its infringement of the '579 patent. For instance,
23 KCT touts that “most of [its] R&D team[]” had prior overseas industry experience
24 before being hired to work at KCT, including at Skyworks. (Ex. 2 [KCT Press
25 Release] (“Most of the R&D teams ... have overseas work experience [at] RFaxis
26

27 ⁶ Skyworks' infringement allegations regarding the '579 patent extend to all KCT
28 Wi-Fi FEMs embodying an infringing RF switch system, including KCT Wi-Fi 6,
6E, and 7 certified FEMs.

(acquired by Skyworks in 2016), RFMD (merged into Qorvo), Anadigics and other internationally renowned RF front-end chip companies[.]”.) KCT also touts that the products developed by this team of engineers—a team comprised of engineers who, on information and belief, were formerly employed by Skyworks or Skyworks affiliates—are “pin-to-pin” copies of Skyworks’ Wi-Fi FEM chips (Ex. 4 [KCT Product Roadmap Presentation] at 15), and allegedly are comparable “in terms of linearity, efficiency, noise figure, and other performance metrics” (KXComTech, *IPO Press Release*, [<https://perma.cc/6D7X-VUU6>]). At the same time, KCT has been aware that Skyworks *patented* the technologies contained in its Wi-Fi FEM products, and that KCT’s “pin-to-pin” copies infringed these patents, at least since March 7, 2023, when Skyworks sent a letter to KCT’s President informing KCT that its 2.4GHz and 5 GHz Wi-Fi FEMs infringed. (Ex. 14 [2023 Notice Letter] at 1-2.) Indeed, Skyworks even met with KCT and gave a presentation outlining KCT’s infringement. Under the circumstances present here, KCT knew or should have known of the high probability that it infringed Skyworks’ patented technologies, including the ’579 patent, by making, using, selling, offering for sale, and importing its own pin-to-pin compatible Wi-Fi FEM chips.

90. On information and belief, KCT actively, knowingly, and intentionally has induced and continues to induce infringement of the ’579 patent by, for example, controlling the design and manufacture of, offering for sale, selling, supplying, and otherwise providing instruction and guidance regarding the Accused KCT Products, with the knowledge and specific intent to encourage and facilitate acts of direct infringement with respect to such products, including by resellers, retailers, end product manufacturers, and end users of the Accused KCT Products, both inside and outside the United States. For example, KCT’s website advertises the Accused KCT Products as integrating “a high-efficiency high-linearity power amplifier (PA)” that includes a “power detector” for “accurately monitoring [] output power from the [power amplifier].” (KXComTech, *KCT8547HE-1*, [[-23-](https://perma.cc/7QFB-</p>
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1 L3FW]; KXComTech, *KCT8539S*, [<https://perma.cc/WRA7-GDPD>]; KXComTech,
 2 *KCT8576HE*, [<https://perma.cc/A72U-RFMF>]; *see also* KXComTech, *KCT8239S*,
 3 [<https://perma.cc/NS2E-VPYU>] (describing the KCT8239S product as “a fully
 4 integrated 802.11b/g/n/ac/ax WLAN RF Front-end module (FEM) which
 5 incorporates key RF functionality,” which is “integrated with a high-efficiency
 6 power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated
 7 matching network and a single-pole, double-throw (SPDT) switch all in one
 8 device”).) Further, KCT advertises the Accused KCT Products as being pin-to-pin
 9 compatible with Skyworks’ products. For instance, KCT’s product roadmap
 10 presentation published in the second quarter of 2023 indicated that the accused
 11 KCT8576HE product is pin-to-pin compatible with Skyworks’ SKY85746-11
 12 product. (Ex. 4 [KCT Product Roadmap Presentation] at 13.) On information and
 13 belief, KCT sells and distributes infringing products to customers in the United
 14 States both directly and through third-party distributors like Disman Bakman.
 15 (KXComTech, *Sales Support*, [<https://perma.cc/2PTT-F9XZ>]; KXComTech,
 16 *Distributors*, [<https://perma.cc/FYC6-XH8A>].) On information and belief, KCT’s
 17 distributors, customers, and end users directly infringe the ’579 patent by, for
 18 example, making, using, offering to sell, and/or selling within the United States, and
 19 importing into the United States, without authority or license, both the Accused KCT
 20 Products themselves and/or products containing the Accused KCT Products.

21 91. KCT also contributes to infringement of the ’579 patent by selling for
 22 importation into the United States, importing into the United States, and/or selling
 23 within the United States after importation the Accused KCT Products, which are not
 24 suitable for substantial non-infringing use and which embody a material part of the
 25 invention described in the ’579 patent. These Accused KCT Products are known by
 26 KCT to be especially made or especially adapted for use in the infringement of the
 27 ’579 patent. Specifically, on information and belief, KCT sells the Accused KCT
 28 Products to resellers, retailers, and end product manufacturers with knowledge that

1 such entities perform acts of direct infringement with the Accused KCT Products.
2 On information and belief, KCT sells and distributes infringing products to
3 customers in the United States both directly and through third-party distributors like
4 Disman Bakman. (KXComTech, *Sales Support*, [<https://perma.cc/2PTT-F9XZ>];
5 KXComTech, *Distributors*, [<https://perma.cc/FYC6-XH8A>].) On information and
6 belief, KCT's distributors, customers, and end users directly infringe the '579 patent
7 by, for example, making, using, offering to sell, selling within the United States,
8 and/or importing into the United States, without authority or license, both the
9 Accused KCT Products themselves and/or products containing the Accused KCT
10 Products.

11 92. As a result of KCT's infringement of the '579 patent, Skyworks has
12 been damaged. Skyworks is entitled to recover for damages sustained as a result of
13 KCT's wrongful acts in an amount to be proven at trial, and in no event less than a
14 reasonable royalty for the use made of the invention by KCT, together with interest
15 and costs as fixed by the Court.

16 93. In addition, KCT's infringing acts have caused and are causing
17 immediate and irreparable harm to Skyworks.

18 94. On information and belief, KCT's infringement of the '579 patent has
19 been and continues to be willful. For the reasons stated above, KCT has had
20 knowledge of the '579 patent and its infringement of the '579 patent since at least
21 April 23, 2024. Nevertheless, KCT has deliberately continued to infringe in a
22 wanton, malicious, and egregious manner, with reckless disregard for Skyworks'
23 patent rights. Thus, KCT's infringing actions have been and continue to be
24 consciously willful.

25 95. Based on the information alleged in this claim, Skyworks is informed
26 and believes, and thereon alleges, that this is an exceptional case—including because
27 of KCT's copying of the '579 patent in the Accused KCT Products—which warrants
28 an award of attorneys' fees to Skyworks pursuant to 35 U.S.C. § 285.

1 **COUNT IV – INFRINGEMENT OF U.S. PATENT NO. 9,148,194**

2 96. Skyworks re-alleges and incorporates by reference the allegations of
3 the preceding paragraphs of this Complaint, as if fully set forth herein.

4 97. The '194 patent is valid and enforceable under the United States Patent
5 Laws.

6 98. In violation of 35 U.S.C. § 271, KCT has been and is still infringing,
7 directly or indirectly, literally or under the doctrine of equivalents, the '194 patent
8 by making, using, offering for sale, selling, or importing Wi-Fi 6, 6E and 7 FEMs
9 that practice the '194 patent, including but not limited to the Accused KCT
10 Products).⁷

11 99. The Accused KCT Products infringe at least claim 4 of the '194 patent
12 for at least the reasons described in Skyworks' exemplary infringement charts set
13 forth as Exhibits 24-27.

14 100. KCT has had knowledge of the '194 patent and its infringement of the
15 '194 patent at least since April 23, 2024, when Skyworks sent a letter to KCT
16 providing notice of KCT's infringement of each Asserted Patent, including the '579
17 patent. (Ex. 15 [2024 KCT Notice Letter].) Even before April 23, 2024, KCT was,
18 at a minimum, willfully blind to its infringement of the '194 patent. For instance,
19 KCT touts that "most of [its] R&D team[]" had prior overseas industry experience
20 before being hired to work at KCT, including at Skyworks. (Ex. 2 [KCT Press
21 Release] ("Most of the R&D teams ... have overseas work experience [at] RFaxis
22 (acquired by Skyworks in 2016), RFMD (merged into Qorvo), Anadigics and other
23 internationally renowned RF front-end chip companies[.]").) KCT also touts that
24 the products developed by this team of engineers—comprised at least in part of
25 engineers who, on information and belief, were formerly employed by Skyworks or
26

27 _____
28 ⁷ Skyworks' infringement allegations regarding the '194 patent extend to all KCT
Wi-Fi FEMs embodying an infringing RF switch system, including KCT Wi-Fi 6,
6E, and 7 certified FEMs.

1 Skyworks affiliates—are “pin-to-pin” copies of Skyworks’ Wi-Fi FEM chips (Ex. 4
 2 [KCT Product Roadmap Presentation] at 15), and allegedly are comparable “in terms
 3 of linearity, efficiency, noise figure, and other performance metrics” (KXComTech,
 4 *IPO Press Release*, [<https://perma.cc/6D7X-VUU6>]). At the same time, KCT has
 5 been aware that Skyworks ***patented*** the technologies contained in its Wi-Fi FEM
 6 products, and that KCT’s “pin-to-pin” copies infringed these patents, at least since
 7 March 7, 2023, when Skyworks sent a letter to KCT’s President informing KCT that
 8 its 2.4GHz and 5 GHz Wi-Fi FEMs infringed other patents in Skyworks’ portfolio.
 9 (Ex. 14 [2023 Notice Letter] at 1-2.) Indeed, Skyworks even met with KCT and
 10 gave a presentation outlining KCT’s infringement. Under the circumstances present
 11 here, KCT knew or should have known of the high probability that it infringed
 12 Skyworks’ patented technologies, including the ’194 patent, by making, using,
 13 selling, offering for sale, and importing its own pin-to-pin compatible Wi-Fi FEM
 14 chips.

15 101. On information and belief, KCT actively, knowingly, and intentionally
 16 has induced and continues to induce infringement of the ’194 patent by, for example,
 17 controlling the design and manufacture of, offering for sale, selling, supplying, and
 18 otherwise providing instruction and guidance regarding the Accused KCT Products,
 19 with the knowledge and specific intent to encourage and facilitate acts of direct
 20 infringement with respect to such products, including by resellers, retailers, end
 21 product manufacturers, and end users of the Accused KCT Products, both inside and
 22 outside the United States. For example, KCT’s website advertises the Accused KCT
 23 Products as integrating “a high-efficiency high-linearity power amplifier (PA)” that
 24 includes a “power detector” for “accurately monitoring [] output power from the
 25 [power amplifier].” (KXComTech, *KCT8547HE-1*, [<https://perma.cc/7QFB-L3FW>]; KXComTech, *KCT8539S*, [<https://perma.cc/WRA7-GDPD>]; KXComTech,
 26 *KCT8576HE*, [<https://perma.cc/A72U-RFMF>]); *see also* KXComTech, *KCT8239S*,
 27 [<https://perma.cc/NS2E-VPYU>] (describing the KCT8239S product as “a fully
 28

1 integrated 802.11b/g/n/ac/ax WLAN RF Front-end module (FEM) which
2 incorporates key RF functionality,” which is “integrated with a high-efficiency
3 power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated
4 matching network and a single-pole, double-throw (SPDT) switch all in one
5 device”).) Further, KCT advertises the Accused KCT Products as being pin-to-pin
6 compatible with Skyworks’ products. For instance, KCT’s product roadmap
7 presentation published in the second quarter of 2023 indicated that the accused
8 KCT8576HE product is pin-to-pin compatible with Skyworks’ SKY85746-11
9 product. (Ex. 4 [KCT Product Roadmap Presentation] at 13.) On information and
10 belief, KCT sells and distributes infringing products to customers in the United
11 States both directly and through third-party distributors like Disman Bakman.
12 (KXComTech, *Sales Support*, [<https://perma.cc/2PTT-F9XZ>]; KXComTech,
13 *Distributors*, [<https://perma.cc/FYC6-XH8A>].) On information and belief, KCT’s
14 distributors, customers, and end users directly infringe the ’194 patent by, for
15 example, making, using, offering to sell, and/or selling within the United States, and
16 importing into the United States, without authority or license, both the Accused KCT
17 Products themselves and/or products containing the Accused KCT Products.

18 102. KCT also contributes to infringement of the ’194 patent by selling for
19 importation into the United States, importing into the United States, and/or selling
20 within the United States after importation the Accused KCT Products, which are not
21 suitable for substantial non-infringing use and which embody a material part of the
22 invention described in the ’194 patent. These Accused KCT Products are known by
23 KCT to be especially made or especially adapted for use in the infringement of the
24 ’194 patent. Specifically, on information and belief, KCT sells the Accused KCT
25 Products to resellers, retailers, and end product manufacturers with knowledge that
26 such entities perform acts of direct infringement with the Accused KCT Products.
27 On information and belief, KCT sells and distributes infringing products to
28 customers in the United States both directly and through third-party distributors like

1 Disman Bakman. (KXComTech, *Sales Support*, [<https://perma.cc/2PTT-F9XZ>];
2 KXComTech, *Distributors*, [<https://perma.cc/FYC6-XH8A>].) On information and
3 belief, KCT's distributors, customers, and end users directly infringe the '194 patent
4 by, for example, making, using, offering to sell, selling within the United States,
5 and/or importing into the United States, without authority or license, both the
6 Accused KCT Products themselves and/or products containing the Accused KCT
7 Products.

8 103. As a result of KCT's infringement of the '194 patent, Skyworks has
9 been damaged. Skyworks is entitled to recover for damages sustained as a result of
10 KCT's wrongful acts in an amount to be proven at trial, and in no event less than a
11 reasonable royalty for the use made of the invention by KCT, together with interest
12 and costs as fixed by the Court.

13 104. In addition, KCT's infringing acts have caused and are causing
14 immediate and irreparable harm to Skyworks.

15 105. On information and belief, KCT's infringement of the '194 patent has
16 been and continues to be willful. For the reasons stated above, KCT has had
17 knowledge of the '194 patent and its infringement of the '194 patent since at least
18 April 23, 2024. Nevertheless, KCT has deliberately continued to infringe in a
19 wanton, malicious, and egregious manner, with reckless disregard for Skyworks'
20 patent rights. Thus, KCT's infringing actions have been and continue to be
21 consciously willful.

22 106. Based on the information alleged in this claim, Skyworks is informed
23 and believes, and thereon alleges, that this is an exceptional case—including because
24 of KCT's copying of the '194 patent in the Accused KCT Products—which warrants
25 an award of attorneys' fees to Skyworks pursuant to 35 U.S.C. § 285.

26 **PRAYER FOR RELIEF**

27 WHEREFORE, Skyworks respectfully requests that this Court enter judgment
28 in its favor as follows and award Skyworks the following relief:

- 1 a) A judgment that KCT has infringed at least one or more claims of the Asserted
- 2 Patents, directly and/or indirectly, literally and/or under the doctrine of
- 3 equivalents;
- 4 b) An award of damages sufficient to compensate Skyworks for KCT's
- 5 infringement under 35 U.S.C. § 284;
- 6 c) An adjudication that KCT's infringement has been willful and deliberate, and
- 7 an award to Skyworks of treble damages and pre-judgment interest under 35
- 8 U.S.C. § 284;
- 9 d) An adjudication that this case is exceptional under 35 U.S.C. § 285, and an
- 10 award to Skyworks of its reasonable attorneys' fees;
- 11 e) An award to Skyworks of its costs and expenses in this action;
- 12 f) A permanent injunction restraining and enjoining KCT and its officers,
- 13 directors, agents, servants, employees, successors, assigns, parents,
- 14 subsidiaries, affiliated or related companies, attorneys, and all others in active
- 15 concert or participation with any of the foregoing, from directly or indirectly
- 16 infringing the Asserted Patents;
- 17 g) Such other and further relief as the Court deems just and proper.

18 **DEMAND FOR JURY TRIAL**

19 Pursuant to Rule 38 of the Federal Rules of Civil Procedure and Local Rule
20 38-1 of this Court, Skyworks hereby demands a trial by jury as to all issues so triable.

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1 Dated: May 6, 2024

Respectfully Submitted,

3 **SKYWORKS SOLUTIONS, INC.**

5 By: /s/ James M. Dowd

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20 *Attorneys for Plaintiff Skyworks Solutions, Inc.*

EXHIBIT 1

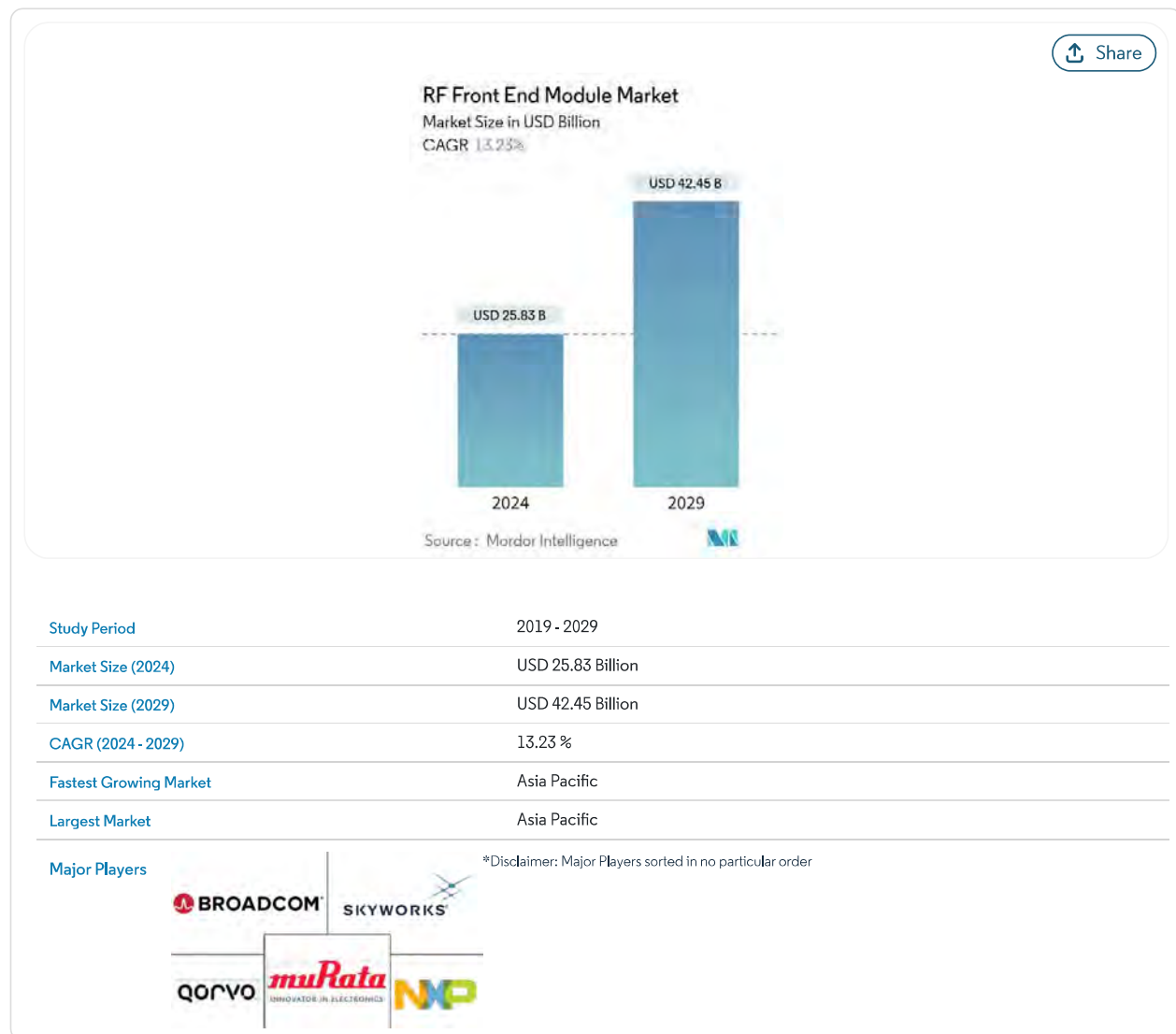
RF FRONT END MODULE INDUSTRY SIZE & SHARE ANALYSIS - GROWTH TRENDS & FORECASTS (2024 - 2029)

The Report Covers RF Front End Module Market Size & Growth. The Market is Segmented by Component (RF Filters, RF Switches, RF Power Amplifiers, and Other Components), Application (Consumer Electronics, Automotive, Military, Wireless Communication, and Other Applications), and Geography (North America, Europe, Asia-Pacific, and Rest of the World). The Market Sizes and Forecasts are Provided in Terms of Value (USD) for all the Above Segments.

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Radio Frequency (RF) Front End Module Market Size



Radio Frequency (RF) Front End Module Market Analysis

The RF Front End Module Market size is estimated at USD 25.83 billion in 2024, and is expected to reach USD 42.45 billion by 2029, growing at a CAGR of 13.23%.

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work and withstand the harsh space environment, they need extra effort in in-circuit redesign and implementation. The RF front-end design is considered one of the better and more feasible choices in expert research, which consists of an S-band transceiver that is fully implemented using COTS components. If further implemented in nanosatellites, the market in this sector shall grow significantly during the forecast period.

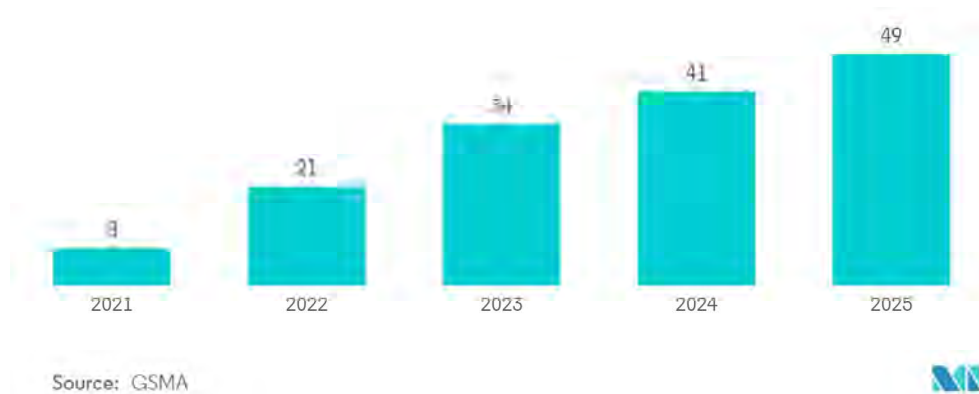
- An RF front-end module refers to the circuitry in a radio receiver circuit between a radio receiver's antenna input and the mixer stage or the transmitter's power amplifier.
- The exponential increase in mobile communication devices on a unit basis and rising data traffic due to data-intensive applications have led RF FEM providers to lead innovation, such as high-frequency bands in handsets. Additionally, per the Cisco Visual Networking Index, the global mobile data traffic is expected to increase sevenfold between 2017 and 2022, with a CAGR of 46%, reaching 77.5 exabytes per month by 2022.
- Qorvo introduced the first dual-band front-end module (FEM) for Wi-Fi 6, the SKY85334-11 and SKY85750-11. It is designed ideally for customer premise equipment (CPE), combining the performance required to deliver HD/4K video with the efficiency needed for IoT. Also, by featuring linearity, power dissipation, and efficiency for access points, routers, and gateways, where regulatory, thermals, or Power-over-Ethernet (PoE) limitations demand low current consumption, the modules overlook integration at switching, low-noise amplifier (LNA) with bypass and power amplifier (PA) as applications.
- Moreover, the constant increase in defense budgets in developing and developed nations and the demand for technologically-advanced products in the arsenal of national and international armed forces are expected to further fuel the global market's growth. Military radio frequency and electronic warfare applications are expected to grow in addition to the technological advancements in autonomous vehicles and drones.
- RF power amplifiers (PA), thus, form an integral part of all the base stations for wireless mobile infrastructure. They represent one of the most expensive components of sub-assemblies in modern infrastructure equipment. The GaN RF semiconductors used in these power amplifiers must evolve with the economic and technical realities facing the designers and users of these RF PAs.
- Due to government-imposed lockdowns and travel and trade restrictions, many industries, such as electronics, automotive, aerospace & defense, and telecommunications, were forced to shut down their operations, lowering the demand for RF power semiconductors in 2020. As of 2022, several RF component makers have reorganized their supply chains by working with regional raw material suppliers. In the future, this is projected to reduce the burden of the COVID-19 pandemic on producers.

Radio Frequency (RF) Front End Module Market Trends

RF Filters to Witness Significant Growth

- Radiofrequency (RF) filters are widely used in the communication industry to eliminate white noise interference when receiving and transferring data across various channels. These filters are often employed in operating fields, such as television broadcasting, wireless communication, and radios operating from medium to high frequencies. This is done to provide reliable, error-free, and appropriate communication from one end to the other. Band-reject, high-pass, band-pass, and low-pass filters are the four types of RF filters.
- RF filters are used with radio receivers to ensure that only the appropriate frequencies are broadcasted, filtering out undesirable bands of frequencies. They are a crucial component of wireless technology. These filters are built to function at frequencies ranging from medium to extremely high, such as megahertz and gigahertz. Due to their working feature, they are most commonly employed in equipment like broadcast radio, wireless communications, and television.
- Mobile computing devices are becoming more popular among mobile users and business travelers who need constant mobility and connection. Consumers use these gadgets for various tasks, including accessing social media applications, surfing the web, reading news, and checking emails. The growing internet penetration rate and the availability of high data rates at affordable speeds are driving the demand for mobile computing devices.
- Network traffic is increasing exponentially, owing to the growing use of mobile computing devices. The proliferation of mobile computing devices (such as smartphones, tablets, and laptops) with increased capabilities is driving internet bandwidth. The increased need for new RF functionalities in smartphones and tablets has resulted from incorporating advanced wireless technologies, such as LTE and Wi-Fi.
- Furthermore, RF filters play an essential function in the cell phone environment. Mobile phones, for example, require a particular number of bands to function effectively. Without the right RF filter, the various bands cannot coexist simultaneously. This will result in the rejection of certain bands, such as the Wi-Fi, public safety, and global navigation satellite system (GNSS). RF filters are crucial because they allow all bands to coexist simultaneously.
- The increasing rate as a share of mobile connections in Canada will reach 49% by 2025 from 8% in 2021.

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[!\[\]\(b246cff486eb7c4dec085261afe05404_img.jpg\) Understand The Key Trends Shaping This Market](#)
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Asia-Pacific to Witness Major Growth

- The Asia-Pacific is expected to witness significant growth. The advancement in consumer electronics and growing defense equipment requirements with the considerable growth of major emerging economies, such as China, India, and South Korea, will further boost the demand for the RF component market.
- The flourishing Integrated Circuit (IC) industry, expanding the SOI ecosystem in the Asia-Pacific, and increasing the use of SOI in IoT applications act as growth opportunities for the RF Front End Module (RFFE). According to Forbes, the number of IoT devices will surpass 3.5 billion by 2023, with Asia leading the highest market share. By 2023, Northeast Asia will be a market for more than 2.2 billion devices.
- For data transmission over 2G, 3G, and 4G/ Long-term Evolution (LTE), mobile devices require dedicated front-end modules (FEMs). FEMs use RF-SOI chips, which integrate switches, power amplifiers, antenna tuning components, power management units, and filters on a single platform for IoT applications. Hence, this caters to the market growth in the region.
- Further, increasing the production of vehicles in the Asia-Pacific is expected to drive the demand for compact dual-band RF front-end modules for global positioning system (GPS) operating in the L1-band (1574.42-1576.42 MHz) and satellite digital audio radio system (SDARS) operating in the S-band (2320-2345 MHz). This, in turn, may boost the market in the region. China is the largest maker of electric vehicles and leads with the highest level of EV uptake over the projection period. By 2030, the share of EVs in new vehicle sales is estimated to reach 57% across all road transport modes (i.e., two-wheelers, cars, buses, and trucks).
- Furthermore, as front-end modules are essential to many wireless applications, such as base stations and 5G smartphones, China's massive capital investment project designed to nurture the domestic semiconductor industry has rolled out its second funding phase. The project is scheduled for the next five years with a budget of YUAN 204.15 billion (USD 28.9 billion). By addressing RF front-end modules, Huawei creates an opportunity to ponder areas that need attention for developing the necessary technologies, designs, and IPs, possibly expected to begin designing a whole integrated module system in China. This further penetrates future growth for the market.

RF Front End Module Market - Market CAGR (%), By Region, Global





Radio Frequency (RF) Front End Module Industry Overview

The RF front-end module market is fragmented due to high market rivalry. With increasing innovation, partnerships, and mergers, the market is expected to have high competition in the forecasted period. Key players in the market are Broadcom Inc., Skyworks Solutions, Inc., etc.

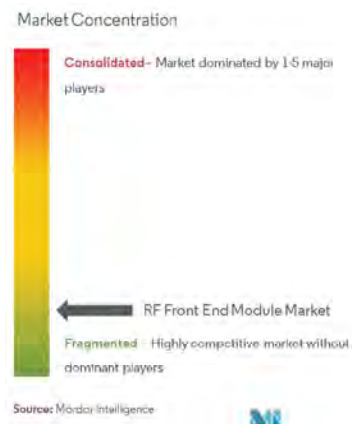
In June 2022, Qualcomm Technologies Inc. announced the launch of Wi-Fi 7 front-end modules that offered enhanced wireless performance in automotive and internet-connected devices. The introduction of the RFFE modules aligned with the company's objective to extend its handset range with modem-to-antenna solutions for automotive and IoT.

In February 2022, Murata Manufacturing announced the expansion of its millimeter-wave RF front-end portfolio for 5G wireless infrastructure applications. The three beam-forming ICs and two up-down converters offered flexibility to interchange ICs for full IF-to-RF coverage across the n257, n258, and n260 bands.

Radio Frequency (RF) Front End Module Market Leaders

- 1 Broadcom Inc.
- 2 Skyworks Solutions, Inc.
- 3 Murata Manufacturing Co., Ltd.
- 4 Qorvo, Inc.
- 5 NXP Semiconductors N.V.

*Disclaimer: Major Players sorted in no particular order



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Radio Frequency (RF) Front End Module Market News

- May 2022: Nordic Semiconductor launched the nRF5340 Audio DK for Bluetooth LE audio development, enabling better audio quality with LC3 codec, more extended playtime, and new features, such as multi-stream audio and broadcast audio.
- November 2021: Qualcomm Technologies Inc. rolled out a new family of RF filters targetting mid and high-frequency bands used by 5G networks. The UltraBAW filters covered a wide frequency range of 2.7 GHz to 7.2 GHz, including the 5 GHz and 6 GHz bands used by Wi-Fi. The chips complemented filters based on the UltraSAW technology.

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Radio Frequency (RF) Front End Module Industry Segmentation

The RF front-end module incorporates all the circuitry between the antenna and at least one mixing stage of a receiver and possibly the transmitter's power amplifier.

The RF front-end module market is segmented by component (RF filters, RF switches, RF power amplifiers, and other components), application (consumer electronics, automotive, military, wireless communication, and other applications), and geography (North America (United States, Canada), Europe (Germany, United Kingdom, France, and the rest of Europe), Asia-Pacific (India, China, Japan, and the rest of Asia-Pacific), and rest of the World (Latin America, Middle East and Africa)). The market sizes and forecasts are provided in terms of value (USD) for all the above segments. Further, the report covers the major vendors in the market and their investments. The report also presents a comprehensive study of the geographical segmentation of the market and the impact of COVID-19 on the market.



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Radio Frequency (RF) Front End Module Market Research FAQs

How big is the RF Front End Module Market?



What is the current RF Front End Module Market size?



Who are the key players in RF Front End Module Market?



Which is the fastest growing region in RF Front End Module Market?



Which region has the biggest share in RF Front End Module Market?



What years does this RF Front End Module Market cover, and what was the market size in 2023?



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RF Front End Module Industry Report

Statistics for the 2024 RF Front End Module market share, size and revenue growth rate, created by Mordor Intelligence™ Industry Reports. RF Front End Module analysis includes a market forecast outlook for 2024 to 2029 and historical overview. Get a sample of this industry analysis as a free report PDF download.

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EXHIBIT 2

Home (/En/) > News (/En/News/) > Company Events (/En/News/Company-Events/)

R&D Center of Kangxi Communication Technologies (Shanghai) Co., Ltd was successfully identified as Shanghai Enterprise Technology Center

Release time: 2022-10-24 21:52:29 Hits: 475

After eight years of development, Kangxi Communication Technologies (Shanghai) Co., Ltd has gradually established a highly specialized, automated, and advanced domestic RF front-end chip R&D center. Most of the R&D teams graduated from Lehigh University in the United States, University of Surrey in the United Kingdom, University of Regina in Canada, and University of California, Los Angeles, Shanghai Jiao Tong University, Xi'an Jiaotong University, Southeast University, University of Electronic Science and Technology of China and other well-known universities, and have overseas work experience in RFAxis (acquired by Skyworks in 2016), RFMD (merged into Qorvo), Anadigics and other internationally renowned RF front-end chip companies, rich experience in RF front-end chip research and development and global technical vision, provide a solid guarantee for the company's technology innovation in the field of RF front-end chips.

Kangxi Communication Wireless RF Front-end Chip R&D Center, after becoming an enterprise R&D institution in Pudong New Area in 2021, has been innovated and upgraded again, and successfully been identified as a Shanghai Enterprise Technology Center in October 2022, named "Kangxi Communication Technology (Shanghai) Co., Ltd. Technology Center".

Announcement original URL:

<http://sheitc.sh.gov.cn/jsjb/20221024/62b69d5697a948d497598539508ba2a9.html>

(<http://sheitc.sh.gov.cn/jsjb/20221024/62b69d5697a948d497598539508ba2a9.html>).

PREV: KCT won the 2020 "Outstanding supplier" Award of T&W (/En/News/Company-Events/712.html)

NEXT: Kxcomtech's Wi-Fi 7 RF Front-End Chip Empowers French Telecoms's Cutting-Edge Router - Freebox Ultra Wi-Fi 7 Router (/En/News/Company-Events/838.html)

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- > LNA + SW Modules (/En/Products/LNA--SW-Modules)
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Markets

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Tel: +86 2168386910 E-mail: Evan.chen@kxcomtech.com

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EXHIBIT 3

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Standing - FTB	Good
Standing - Agent	Good
Standing - VCFCF	Good
Formed In	NEVADA
Entity Type	Stock Corporation - Out of State - Stock
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Mailing Address	14151 NEWPORT AVE. SUITE 204 TUSTIN, CA 92780
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09/12/2016

GRAND CHIP LABS INC (3945169)



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Initial Filing Date	09/12/2016
Status	Active
Standing - SOS	Good
Standing - FTB	Good
Standing - Agent	Good
Standing - VCFCF	Good
Formed In	NEVADA
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LEADING Wireless Future

Kangxi Communication Technologies
Product Portfolio

Leading RF Technologies, Bridging Wireless Communication

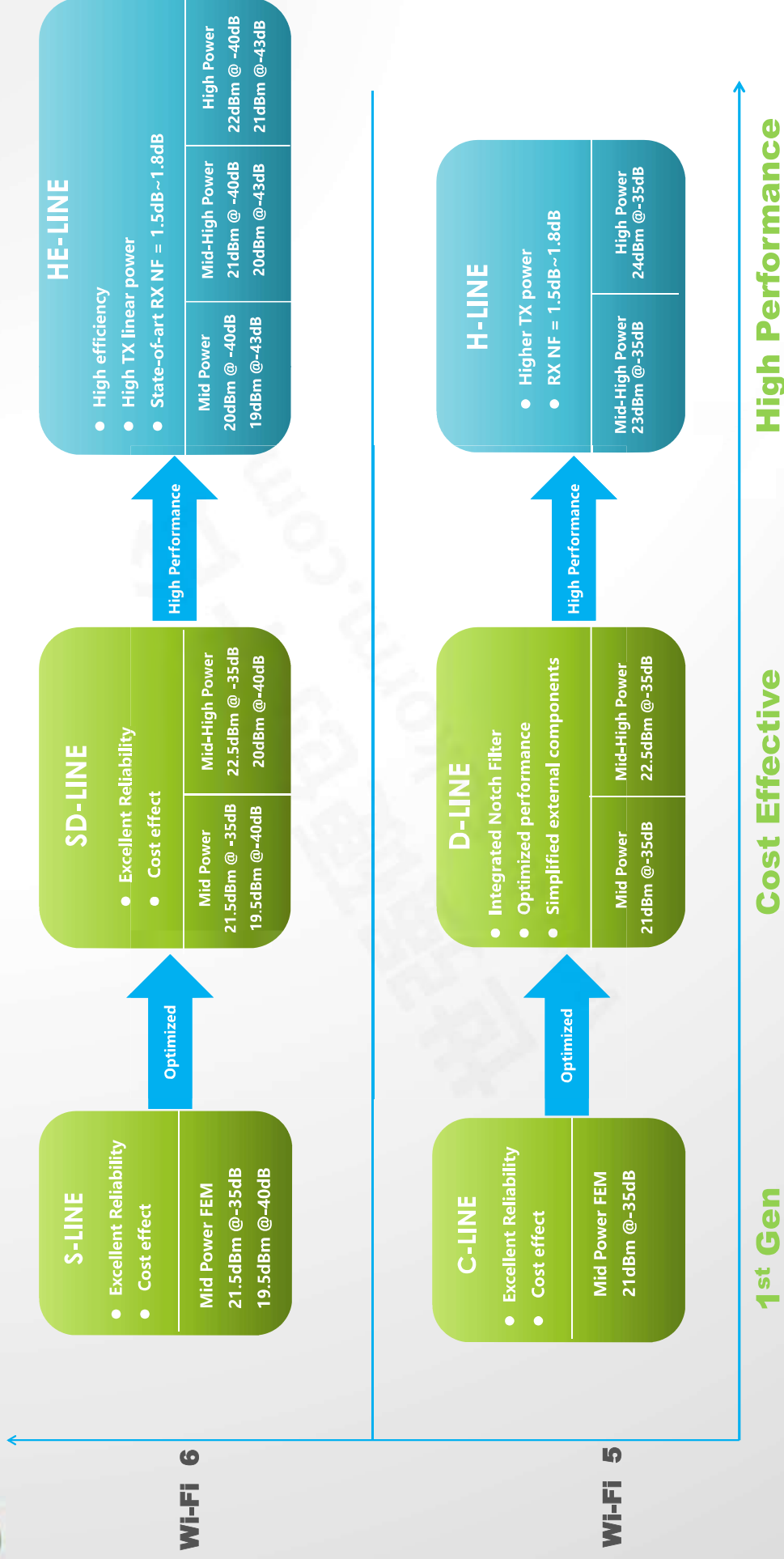
2023 Q2



KCT Product Roadmap

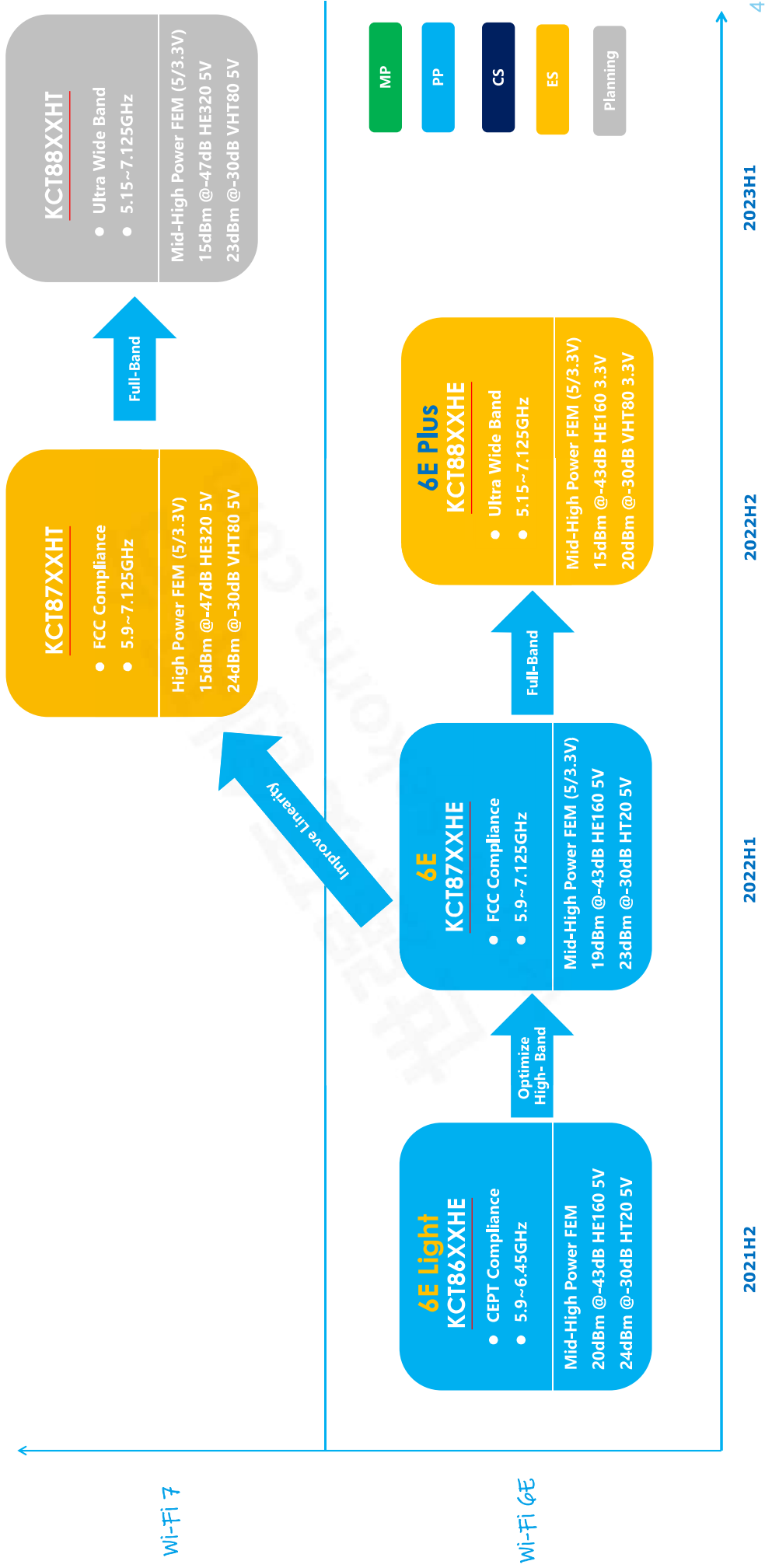


Product Roadmap – Wi-Fi 5/6 (for CPE, PON, AP Router)





Product Roadmap – Wi-Fi 6E/7 (for Infrastructure)





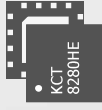
KXcomtech Wi-Fi 7 Portfolio for Qualcomm

2.4GHz

5.15-5.925GHz

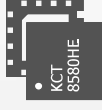
5.9~7.125GHz

5.15~7.125GHz



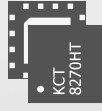
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LGA 3x3mm, Vdet & CPLR
22dBm/ EHT40 @-43dB
25.5dBm /HT20 @-30dB
NF = 1.6dB

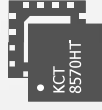


New!

QFN 3x3mm, Vdet & CPLR
20dBm /EHT160 @-43dB
25.5dBm /HT20 @-30dB
NF = 1.7dB

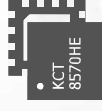


LGA 3x3mm, Vdet & CPLR
20dBm EHT40 @-43dB
24dBm HT20 @-30dB
NF = 1.4dB

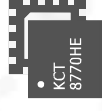


New!

QFN 3x3mm, Vdet & CPLR
18dBm EHT160 @-45dB
24dBm HT20 @-30dB
NF = 1.8dB

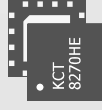


QFN 3x3mm, CPLR & Vdet
17dBm EHT160 @-43dB
24dBm HT20 @-30dB
NF = 1.8dB

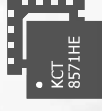


New!

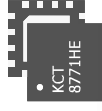
QFN 3mmx3mm, Vdet & CPLR
15.5dBm EHT320 @-43dB
23.5dBm HT20 @-30dB
NF = 1.8dB



LGA 3x3mm, CPLR & Vdet
18dBm HE40 @-40dB
20dBm HT20 @-30dB
NF = 1.5dB

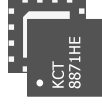


QFN 3x3mm, CPLR & Vdet
17.5dBm HE160 @-40dB
20dBm HT20 @-30dB
NF = 1.7dB



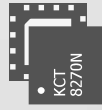
New!

QFN 3x3mm, CPLR & Vdet
13dBm EHT320 @-43dB
20dBm HT20 @-30dB
NF = 1.8dB

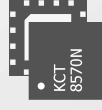


Coming Soon!

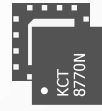
QFN 3x3mm, CPLR & Vdet
15dBm EHT160 @-43dB
19dBm HT20 @-30dB
NF = 2.2dB



LGA 3x3mm, Vdet & CPLR
21dBm EHT40 @-43dB wDPD
24.5dBm HT20 @-30dB wDPD
NF = 1.7dB

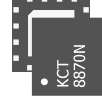


QFN 3x3mm, Vdet & CPLR
21dBm EHT160 @-43dB wDPD
24.5dBm HT20 @-30dB wDPD
NF = 1.8dB



New!

QFN 3x3mm, Vdet & CPLR
17dBm EHT320 @-43dB wDPD
24.5dBm HT20 @-30dB wDPD
NF = 1.7dB



Coming Soon!

QFN 3x3mm, Vdet & CPLR
16dBm EHT160 @-43dB wDPD
24.5dBm HT20 @-30dB wDPD
NF = 2.0dB

5V
High Power
Linear FEM

5V
Mid-High
Linear
FEM

3.3V
Mid-High
Linear
FEM

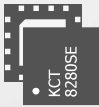
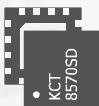
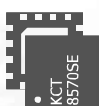
3.3~5V
Non-Linear
FEM



KXcomtech Wi-Fi 6/6E Portfolio Qualcomm

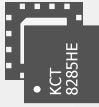
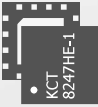
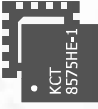
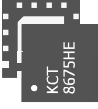
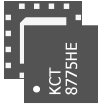
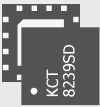
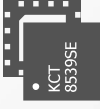
2.4GHz	5.15~5.925GHz	5.9~6.45GHz	5.9~7.125GHz
 <i>New!</i> LGA 3x5mm, CLPR & Vdet 21.5dBm HE40 @-43dB 25dBm HT20 @-30dB NF = 1.5dB	 <i>New!</i> QFN 3x5mm, CPLR & Vdet 19.5dBm HE160 @-43dB 25.5dBm HT20 @-30dB NF = 1.8dB	 QFN 3x5mm, CPLR & Vdet 19.5dBm HE160 @-43dB 24dBm HT20 @-30dB NF = 2.0dB	 <i>New!</i> QFN 3x5mm, CPLR & Vdet 15.5dBm EHT320 @-43dB 23dBm HT20 @-30dB NF = 1.9dB

5V Cost-effective

 <i>Planning!</i>	QFN 3x3mm, CPLR & Vdet 22dBm/ EHT40 @-43dB 25.5dBm /HT20 @-30dB NF = 2.0dB		QFN 3x3mm, CPLR & Vdet 21dBm HE160 @-40dB 24dBm HT20 @-30dB NF = 2.8dB	 <i>Planning!</i>	QFN 3x3mm, CPLR & Vdet 18dBm EHT160 @-45dB 24dBm HT20 @-30dB NF = 2.1dB



KXcomtech Wi-Fi 6/6E/7 Portfolio Broadcom

2.4GHz	5.15-5.925GHz	5.9~6.45GHz	5.9~7.125GHz
 ES LGA 3x5mm, CLPR & Vdet 22dBm EHT40 @-45dB 26dBm HT20 @-30dB NF = 1.7dB	 ES LGA 3x5mm, CLPR & Vdet 17dBm EHT160 @-45dB 25dBm VHT80 @-30dB NF = 2.1dB		 Wi-Fi 7 ES LGA 3x5mm, CLPR & Vdet 14dBm HE320 @-45dB 23dBm VHT80 @-30dB NF = 2.5dB
 Wi-Fi 6 QFN 3x5mm, Vdet 21.5dBm HE40 @-43dB 26dBm HT20 @-30dB NF = 1.5dB	 QFN 3x3mm, Vdet 22dBm HE40 @-43dB 25.5dBm HT20 @-30dB NF = 1.5dB	 New! QFN 3x5mm, Vdet 19dBm HE160 @-43dB 25.5dBm HT20 @-30dB NF = 1.8dB	 Wi-Fi 6 New! QFN 3x5mm, Vdet 15dBm EHT320 @-43dB 23.0dBm HT20 @-30dB NF = 1.9dB
 MIS 3x3mm, Vdet 20dBm HE40 @-43dB 24dBm HT20 @-30dB NF = 1.5dB	 MIS 3x3mm, Vdet 19.5dBm HE160 @-43dB 24dBm HT20 @-30dB NF = 1.7dB	 MIS 3x3mm, Vdet 20.5dBm HE160 @-43dB 24dBm HT20 @-30dB NF = 1.8dB	 PR MNAI MIS 3x3mm, Vdet 15.5dBm EHT320 @-43dB 23.0dBm HT20 @-30dB NF = 1.9dB
 New! QFN 3x3mm, Vdet 20.5dBm HE40 @-43dB 24.5dBm HT20 @-30dB NF = 2.5dB	 New! QFN 3x3mm, Vdet 20.5dBm HE160 @-43dB 24dBm HT20 @-30dB NF = 1.9dB	 Planning QFN 3x3mm, Vdet 20dBm HE160 @-43dB 24dBm HT20 @-30dB NF = 2.1dB	

Wi-Fi 6
Cost-effective





Full Product List

Wi-Fi Infrastructure

HT Line | High-End Wi-Fi 7 FEM 2.4G & 5GHz & 6GHz

Part No.	Frequency (GHz)	Vcc (V)	TX Power@ -40dB(dBm)	TX Power@ -45dB(dBm)	TX Gain (dB)	RX Gain (dB)	RX NF (dB)	Package (mm)	P2P Part
<u>KCT8278HT</u>	2.4 - 2.5	5	23.5	21.5	34	18.5	1.7	LGA 24L 3*5*0.812	SKY85355-11 QPF4257
<u>KCT8578HT</u>	5.9 - 7.1	5	21	17	30	17	2.1	LGA 24L 3*5*0.812	SKY85799-11 QPF4557
<u>KCT8778HT</u>	5.1 - 5.9	5	19	14	29	13.5	2.5	LGA 24L 3*5*0.812	SKY85795-11 QPF4657
<u>KCT8270HT</u>	2.4 - 2.5	5	21	18	30	14.5	1.4	LGA 16L 3*3*0.76	SKY85358-11 QPF4259
<u>KCT8280HT</u>	2.4 - 2.5	5	22.5	19.5	31.5	13.5	1.6	LGA 16L 3*3*0.76	SKY85358-11 QPF4259
<u>KCT8570HT</u>	5.1 - 5.9	5	21.5	18	31	16.5	1.8	QFN 16L 3*3*0.75	SKY85791-11 SKY85797 QPF4559 RTC66506

N Line | N-Line - High Efficiency DPD FEM Solution 2.4G & 5GHz & 6GHz

Part No.	Frequency (GHz)	Vcc (V)	TX Power With DPD @-40dB(dBm)	TX Power With DPD @-35dB(dBm)	TX Gain (dB)	RX Gain (dB)	RX NF (dB)	Package (mm)
<u>KCT8239N</u>	2.4 - 2.5	5	22	22.8	31.5	16	1.5	MIS 16L 3*3*0.75
<u>KCT8576N</u>	5.15 - 5.85	5	20.5	24	30.5	16.5	1.7	QFN 16L 2.5*2.5*0.55
<u>KCT8539N</u>	5.15 - 5.95	5	20.5	23.7	31.5	16	1.7	MIS 16L 3*3*0.75
<u>KCT8270N</u>	2.4 - 2.5	5	22	23	29	14	1.7	LGA16L 3*3*0.76
<u>KCT8570N</u>	5.15 - 5.95	5	22.5	23.5	30.5	16	1.8	QFN16L 3*3*0.75
<u>KCT8770N</u>	5.9 - 7.1	5	22.5	24	33	14	1.7	QFN16L 3*3*0.75
<u>KCT8870N</u>	5.1 - 7.1	5	20.5	23.5	31.5	13.5	2.0	QFN16L 3*3*0.75
<u>KCT8278N</u>	2.4 - 2.5	5	22	24.5	33	19	1.8	LGA 24L 3*5*0.812
<u>KCT8578N</u>	5.9 - 7.1	5	21	24	32	13	2.2	LGA 24L 3*5*0.812
<u>KCT8778N</u>	5.1 - 5.9	5	22.5	24	33	14	2.0	LGA 24L 3*5*0.812

HE Line | High-End Wi-Fi 6E FEM - 6GHz

Part No.	Frequency (GHz)	Vcc (V)	TX Power@ -40dB(dBm)	TX Power@ -35dB(dBm)	TX Gain (dB)	RX Gain (dB)	RX NF (dB)	Package (mm)	P2P Part
<u>KCT8728HE</u>	5.9 - 7.1	5	19.5	22	30.0	13.5	1.9	LGA 24L 3*5*0.812	SKY85780-11
<u>KCT8748HE</u>	5.9 - 7.1	5	19.0	21.5	29.0	13.5	1.9	LGA 24L 3*5*0.812	SKY85784-11 QPF4658
<u>KCT8770HE</u>	5.9 - 7.1	5	20.0	22	30.0	14.0	1.8	QFN 16L 3*3*0.75	SKY85783-11 QPF4659 SKY85798-11
<u>KCT8775HE</u>	5.9 - 7.1	5	19.5	22	30.0	14.0	1.9	MIS 16L 3*3*0.57	SKY85781-11 QPF4656
<u>KCT8771HE</u>	5.9 - 7.1	3.3	18	19	29.5	13.0	1.8	QFN 16L 3*3*0.75	SKY85783-11
<u>KCT8773HE</u>	5.9 - 7.1	3.3	16.5	18.5	29	13.5	2.0	MIS 16L 3*3*0.55	SKY85781-11 QPF4656
<u>KCT8774HE</u>	5.9 - 7.1	3.3	17.5	18.5	30	13.5	1.9	QFN 16L 2.5*2.5*0.55	QPF4632
<u>KCT8871HE</u>	5.1 - 7.1	3.3	15.5	18	29	13	2.2	QFN 16L 3*3*0.75	QPF4730
<u>KCT8648HE</u>	5.9 - 6.4	5	21	23	31	14.5	2.0	QFN 24L 3*5*0.75	SKY85784-11 QPF4658
<u>KCT8675HE</u>	5.9 - 6.4	5	22	23	32	15.5	1.8	MIS 16L 3*3*0.57	SKY85781-11 QPF4656

Wi-Fi Infrastructure

HE Line | High-End Wi-Fi 6 FEM - 5GHz

Part No.	Frequency (GHz)	Vcc (V)	TX Power@ -40dB(dBm)	TX Power@ -35dB(dBm)	TX Gain (dB)	RX Gain (dB)	RX NF (dB)	Package (mm)	P2P Part
<u>KCT8528HE</u>	5.15 – 5.85	5	21	23.5	31.5	16	1.7	QFN 24L 3*5*0.75	SKY85743-21 QPF4516B RTC76780
<u>KCT8548HE</u>	5.15 – 5.85	5	21	23	30.5	16	1.9	QFN 24L 3*5*0.75	SKY85747-11 QPF4588 RTC66504
<u>KCT8528HE-1</u>	5.15 – 5.85	5	22	24	30	17	1.8	QFN 24L 3*5*0.75	SKY85743-21 QPF4516B RTC76780
<u>KCT8548HE-1</u>	5.15 – 5.925	5	22	24	30.5	16.5	1.8	QFN 24L 3*5*0.75	SKY85747-11 QPF4588 RTC66504
<u>KCT8570HE</u>	5.15 – 5.85	5	20.5	22.5	30.5	16.5	1.8	QFN 16L 3*3*0.75	SKY85791-11 QPF4559 SKY85797 RTC66506
<u>KCT8571HE</u>	5.15 – 5.85	3.3	17.5	19	30	16.5	1.7	QFN 16L 3*3*0.55	SKY85750-11 QPF4528
<u>KCT8580HE</u>	5.15 – 5.85	5	22.5	24.5	30	16.5	1.7	QFN 16L 3*3*0.75	SKY85791-11 QPF4559 SKY85797 RTC66506
<u>KCT8575HE</u>	5.15 – 5.85	5	21.5	23	32	16.5	1.7	MIS 16L 3*3*0.57	SKY85755-11 QPF4526
<u>KCT8575HE-1</u>	5.15 – 5.85	5	21.5	23	31	17.5	1.7	MIS 16L 3*3*0.57	SKY85755-11 QPF4526
<u>KCT8585HE</u>	5.15 – 5.85	5	22	24.0	30.5	17	1.8	MIS 16L 3*3*0.57	SKY85755-11 QPF4526

Wi-Fi Infrastructure

HE Line | High-End Wi-Fi 6 FEM - 5GHz

Part No.	Frequency (GHz)	Vcc (V)	TX Power@ -40dB(dBm)	TX Power@ -35dB(dBm)	TX Gain (dB)	RX Gain (dB)	RX NF (dB)	Package (mm)	P2P Part
<u>KCT8539HE</u>	5.15 – 5.85	5	21.5	23	31	16.5	1.7	QFN 16L 3*3*0.75	QPF4526 QPF4506B RTC7676E
<u>KCT8531HE</u>	5.15 – 5.85	5	21.5	23	31	16.5	1.7	QFN 16L 3*3*0.75	QPF4526 QPF4506B RTC7676E
<u>KCT8539HE-1</u>	5.15 – 5.85	5	21.5	23	31	16.5	1.9	QFN 16L 3*3*0.75	QPF4526 QPF4506B RTC7676E
<u>KCT8547HE-1</u>	5.15 – 5.85	5	19	20.5	29	16	1.6	MIS 16L 3*3*0.55	QPF4506B
<u>KCT8545HE</u>	5.15 – 5.85	5	19	21.5	30	16	1.8	QFN 16L 2.5*2.5*0.55	QPF4550
<u>KCT8546HE(Q)</u>	5.15 – 5.85	5	19.5	20.5	30	16	1.7	QFN 16L 2.5*2.5*0.55	QPF4550 RTC66534
<u>KCT8546QL</u>	5.15 – 5.85	3.3	16	17.5	29.5	16.5	1.8	QFN 16L 2.5*2.5*0.55	QPF4550 QPF4532
<u>KCT8576HE</u>	5.15 – 5.85	5	21	23	30.5	15.5	1.8	QFN 16L 2.5*2.5*0.55	SKY85746-11 QPF4551
<u>KCT8574HE</u>	5.15 – 5.85	3.3	18	19.5	30	16.5	1.7	QFN 16L 2.5*2.5*0.55	SKY85748-11 QPF4532 RTC7699

HE Line | High-End Wi-Fi 6 FEM – 2.4GHz

Part No.	Frequency (GHz)	Vcc (V)	TX Power@ -40dB(dBm)	TX Power@ -35dB(dBm)	TX Gain (dB)	RX Gain (dB)	RX NF (dB)	Package (mm)	P2P Part
<u>KCT8243HE</u>	2.4 – 2.5	5	22.5	24.5	33.5	15	1.5	QFN 24L 3*5*0.75	SKY85331-11 QPF4216 RTC76470
<u>KCT8248HE</u>	2.4 – 2.5	5	21.5	23.5	33.5	16	1.5	QFN 24L 3*5*0.75	SKY85333-11 QPF4288 RTC66204
<u>KCT8248HE-1</u>	2.4 – 2.5	5	23	24.5	33.5	15	1.5	LGA 24L 3*5*0.812	SKY85333-11 QPF4288 RTC66204
<u>KCT8276HE</u>	2.4 – 2.5	5	22.5	24.5	31.5	16	1.7	QFN 16L	SKY85326-11 QPF4200
	3.3	3.3	19.5	21	31.5	16	1.7	3*3*0.55	
<u>KCT8270HE</u>	2.4 – 2.5	5	21	23	30	14.5	1.4	LGA 16L	SKY85340-11 QPF4228 RTC66266
	3.3	3.3	18	19	29	14.5	1.5	3*3*0.76	
<u>KCT8280HE</u>	2.4 – 2.5	5	22.5	24.0	31.5	13.5	1.6	LGA 16L 3*3*0.76	SKY85358-11 QPF4259
<u>KCT8247HE-1</u>	2.4 – 2.5	5	21	22.5	30	15.5	1.5	MIS 16L 3*3*0.57	SKY85337-11 QPF4206B RTC7646E
<u>KCT8285HE</u>	2.4 – 2.5	5	23	24.5	34	15.5	1.5	MIS 16L 3*3*0.57	SKY85337-11 QPF4206B RTC7646E
<u>KCT8246HE(Q)</u>	2.4 – 2.5	5	20.5	23	30	16	1.5	QFN 16L 3*3*0.55	SKY85326-11 QPF4200 RTC66266
<u>KCT8246QL</u>	2.4 – 2.5	3.3	17	19.5	29.5	15	1.6	QFN 16L 3*3*0.55	SKY85319-11 QPF4200
<u>KCT8237HE</u>	2.4 – 2.5	5	21.5	22.5	30	15.5	1.6	QFN 16L 3*3*0.55	SKY85347-11

Wi-Fi Infrastructure

S & SD LINE | High Cost-Performance Wi-Fi 6 FEM 2.4G & 5GHz

Part No.	Frequency (GHz)	Vcc (V)	TX Power@ -40dB(dBm)	TX Power@ -35dB(dBm)	TX Gain (dB)	RX Gain (dB)	RX NF (dB)	Package (mm)	P2P Part
<u>KCT8239S</u>	2.4 – 2.5	5	20.5	22	29	19	2.6	MIS16L 3*3*0.55	SKY85337-11 QPF4206B RTC7646
<u>KCT8239SD</u>	2.4 – 2.5	5	21.5	23.5	30	15.5	2.5	QFN16L 3*3*0.75	SKY85337-11 QPF4206B RTC7646
<u>KCT8245SD</u>	2.4 – 2.5	5	22	23	31	15	2.6	QFN16L 2.5*2.5*0.55	QPF4211
<u>KCT8539SD</u>	5.15 – 5.85	5	20	21.5	30	14	3.1	QFN16L 3*3*0.75	QPF4555B RTC7676
<u>KCT8531SD-1</u>	5.15 – 5.85	5	22	23	30.5	13.5	3.0	QFN16L 3*3*0.75	QPF4526 RTC7676
<u>KCT8539SD-1</u>	5.15 – 5.85	5	22	23	30.5	13.5	3.0	QFN16L 3*3*0.75	QPF4526 RTC7676
<u>KCT8539S-1</u>	5.15 – 5.85	5	20.5	22.5	32	17	1.8	MIS16L 3*3*0.57	SKY85755-11 QPF4526 RTC7676E
<u>KCT8539S</u>	5.15 – 5.85	5	20	21.5	30	14	2.6	LGA16L 3*3*0.85	QPF4555B RTC7676
<u>KCT8539S-M</u>	5.15 – 5.85	5	19	21.5	30	15	2.6	MIS16L 3*3*0.55	QPF4555B RTC7676
<u>KCT8570SD</u>	5.15 – 5.85	5	21	23	30.5	14.5	2.9	QFN16L 3*3*0.75	SKY85791-11 QPF4559 RTC66506

Wi-Fi Infrastructure

H LINE | High-End Wi-Fi 5 FEM – 2.4GHz

Part No.	Frequency (GHz)	Vcc (V)	TX Power@ -35dB(dBm)	TX Power@ -30dB(dBm)	TX Gain (dB)	RX Gain (dB)	RX NF (dB)	Package (mm)	P2P Part
<u>KCT8223H</u>	2.4 – 2.5	5	23.5	24.5	30.5	15.5	1.5	QFN16L 3*3*0.55	SKY85319-11 RFFM4252 RTC7625HE
<u>KCT8227H</u>	2.4 – 2.5	5	22	23.5	31	15	1.6	QFN16L 2.5*2.5*0.55	SKY85303-21 RTC7626HE
<u>KCT8232H</u>	2.4 – 2.5	5	23.5	25	32.5	15	2.0	QFN24L 3*5*0.75	SKY85309-11 QPF4219 RTC7662
<u>KCT8523H</u>	5.15 – 5.85	5	22.5	24	30	15.5	2.0	QFN16L 3*3*0.55	SKY85712-21 RFFM4552 RTC5639E
<u>KCT8526H</u>	5.15 – 5.85	5	23	24	31	16.5	1.7	QFN16L 3*3*0.55	SKY85712-21 RFFM4552 RTC5639E
<u>KCT8527H</u>	5.15 – 5.85	5	22.5	23.5	32	16.5	1.6	QFN16L 2.5*2.5*0.55	SKY85746-11 RTC5638HE
<u>KCT8528H</u>	5.15 – 5.85	5	23.5	25	32	16	1.7	QFN24L 3*5*0.75	SKY85728-11 QPF4519 RTC7672

D LINE | High Cost-Performance Wi-Fi 5 FEM - 5GHz

Part No.	Frequency (GHz)	Vcc (V)	TX Power@ -35dB(dBm)	TX Power@ -30dB(dBm)	TX Gain (dB)	RX Gain (dB)	RX NF (dB)	Package (mm)	P2P Part
<u>KCT8522D</u>	5.15 – 5.85	5	21.5	22.5	30.5	14	3.0	QFN16L 3*3*0.55	SKY85712-21 RTC5639
<u>KCT8523D</u>	5.15 – 5.85	5	22.5	23.5	31.5	15	3.0	QFN16L 3*3*0.55	SKY85712-21 RTC5639E
<u>KCT8525D</u>	5.15 – 5.85	5	20.5	21.5	30.5	13.5	3.0	QFN16L 2.5*2.5*0.55	SKY85717-21 RTC5638HS
<u>KCT8525D-1</u>	5.15 – 5.85	5	21.5	22.5	31	14	2.8	QFN16L 2.5*2.5*0.55	SKY85717-21 RTC5638H
<u>KCT8529D</u>	5.15 – 5.85	5	22	23	31	14	2.8	QFN16L 2.5*2.5*0.55	SKY85746-11 RTC5638HE
<u>KCT8529D-1</u>	5.15 – 5.85	5	22.5	23.5	31	14	2.8	QFN16L 2.5*2.5*0.55	SKY85746-11 RTC5638HE
<u>KCT8534D</u>	5.15 – 5.85	3.3	17	19.5	30.5	14	3.0	QFN16L 2.5*2.5*0.55	SKY85717-21 RTC5638H

D LINE | High Cost-Performance Wi-Fi 5 FEM – 2.4GHz

Part No.	Frequency (GHz)	Vcc (V)	TX Power@ -35dB(dBm)	TX Power@ -30dB(dBm)	TX Gain (dB)	RX Gain (dB)	RX NF (dB)	Package (mm)	P2P Part
<u>KCT82226D</u>	2.4 – 2.5	5	21.5	22.5	27.5	16.5	3	QFN16L 3*3*0.55	SKY85310-21 RTC7625H
<u>KCT8226D-1</u>	2.4 – 2.5	5	23	24	30.5	17.5	2.7	QFN16L 3*3*0.55	SKY85310-21 RTC7625H
<u>KCT82227B</u>	2.4 – 2.5	5	22	23	29.5	16	3.3	QFN16L 2.5*2.5*0.55	SKY85303-21 RTC7626H/HE/HS
<u>KCT82227D</u>	2.4 – 2.5	5	21.5	22.5	28	16	3	QFN16L 2.5*2.5*0.55	SKY85303-21 RTC7626HS
<u>KCT82227D-1</u>	2.4 – 2.5	5	23	24	30.5	17	2.6	QFN16L 2.5*2.5*0.55	SKY85303-21 RTC7626HS
<u>KCT82229D</u>	2.4 – 2.5	5	21.5	22.5	27.5	16.5	3	LGA16L 2.5*2.5*0.83	SKY85330-21 SKY85329-21
<u>KCT8229D-1</u>	2.4 – 2.5	5	22.5	23.5	28	15	3.4	LGA16L 2.5*2.5*0.83	SKY85330-21 SKY85329-21
<u>KCT8236D</u>	2.4 – 2.5	5	23.5	24.5	30	15.5	2.5	QFN16L 3*3*0.75	

C LINE | High Cost-Effective Wi-Fi 5 FEM Solution - 5GHz

Part No.	Frequency (GHz)	V _{cc} (V)	TX Power@ -35dB(dBm)	TX Power@ -30dB(dBm)	TX Gain (dB)	RX Gain (dB)	RX NF (dB)	Package (mm)	P2P Part
<u>KCT8533C</u>	5.15-5.85	3.3	18	19	29	12	3.0	QFN16L 3*3*0.55	SKY85703-11 RTC5633
<u>KCT8535C</u>	5.15-5.85	5 3.3	21.5 18	22.5 19	28 28	12 12	3.0+ 3.0+	LGA12L 2*2*0.75	SKY85734-11 SKY85735-11
<u>KCT8536C</u>	5.15-5.85	5 3.3	20.5 17	21.5 18	27.5 26.5	13 12.5	3.0+ 3.0+	LGA12L 2*2*0.76	SKY85734-11 SKY85735-11
<u>KCT8537C</u>	5.15-5.85	5	21	22	29	13	3.0	QFN16L 2.3*2.3*0.55	SKY85753-11

Wi-Fi Infrastructure

RF Switch

Part No.	Function	VDD (V)	Frequency (GHz)	Tsw (ns)	Interface	P - 0.1dB (dBm)	Insertion Loss (dB)	Isolation (dB)	Package (mm)	P2P Part
<u>KCT2821L</u>	SPDT for WiFi5	3.0~3.6	1.0~3.0	150	GPIO	32	0.60@ 2.4~2.5 GHz 0.65@ 1.0~3.0 GHz	23 @ 2.4~2.5 GHz 20 @ 1.0~3.0 GHz	SC-70, 6L, 1.25*2.1	SKY13343 RTC6603SP
<u>KCT2823L</u>	SP3T for WiFi6/6E	1.6~4.2	1.0~7.2	120	GPIO	32	0.55@ 5.8 GHz 0.85@ 7.2 GHz	40@ 5.8 GHz 26@ 7.2 GHz	QFN, 1.1*1.1	RTC66014 MXD8730L
<u>KCT2824L</u>	DPDT for WiFi6/6E/7	1.6~4.2	0.5~7.125	120	GPIO	32	0.55@ 5.8 GHz 0.95@ 7.2 GHz	40@ 5.8 GHz 30@ 7.2 GHz	DFN, 1.5*1.5	SKY13355 RTC66015
<u>KCT2825L</u>	SPDT for WiFi6/6E	1.6~4.2	0.5~7.125	55	GPIO	34	0.55@ 5.8 GHz 0.65@ 7.2 GHz	28@ 5.8 GHz 25@ 7.2 GHz	DFN, 6L, 1.0*1.0	SKY13585 RTC7608 MXD8723E
<u>KCT2826L</u>	SPDT for WiFi5	3.0~3.6	0.1~6.0	250	GPIO	32	0.55 @ 2.4~2.5GHz 0.60 @ 0.1~3.0GHz 0.80 @ 3.0~6.0GHz	34 @ 2.4~2.5GHz 33 @ 0.1~3.0GHz 23 @ 3.0~6.0GHz	DFN, 6L, 1.5*1.5	SKY13314 RTC6609SP
<u>KCT2828L</u>	SPDT for WiFi5/6	3.0~3.6	1.0~6.0	250	GPIO	32	0.40 @ 2.4~2.5GHz 0.50 @ 1.0~3.0GHz 0.70 @ 3.0~6.0GHz	29 @ 2.4~2.5GHz 28 @ 1.0~3.0GHz 26 @ 3.0~6.0GHz	DFN, 6L, 1.0*1.0	SKY13351 RTC6608OSP
<u>KCT2829L</u>	SPDT for WiFi5/6/6E	3.3	0.5~7.125	120	GPIO	32	0.55@ 5.8 GHz 0.65@ 7.2 GHz	28@ 5.8 GHz 25@ 7.2 GHz	DFN, 1.0*1.0	SKY13351 RTC6608 MXD8721E

Wi-Fi Infrastructure

RF PA

Part No.	Frequency (GHz)	Vcc (V)	TX Power@ -35dB(dBm)	TX Power@- 30dB(dBm)	TX Gain (dB)	Package (mm)	P2P Part
<u>KCT6225H</u>	2.4~2.5	5	24.5	25.5	31.5	QFN16L 3*3*0.75	SE2623L SE2576
<u>KCT6526H</u>	5.15~5.8	5	22.5	24.0	32.5	QFN20L 4*4*0.75	SKY85402-11 RFFM5542

Dual-Band Wi-Fi 5 FEM

Part No.	Vcc (V)	TX Power@ -35dB(dBm)	TX Gain (dB)	TX Icq (mA)	RX Gain (dB)	RX NF (dB)	Package (mm)	P2P Part
<u>KCT8822L</u>	3.3	17 @2.4G 17 @5G	31 @2.4G 31 @5G	150 @2.4G 150 @5G	16 @2.4G 16 @5G	3.2 @2.4G 3.2 @5G	LGA24L 4*4*0.75	SE5516

Wi-Fi Infrastructure

Filter

Part No.	Description	Frequency (GHz)	Insertion Loss (dB)	Attenuation (dB)	Package (mm)	P2P
<u>KCT3231</u>	2.4GHz Wi-Fi	2.4	1.8	33 dB @1559~1606MHz 53 dB @2300~2370MHz 43 dB @2510~2690MHz	1.4*1.1*0.73	SAFEA2G45MCOFOA
<u>KCT3232</u>	2.4GHz Wi-Fi (Cost-Effective)	2.4	1.4	30 dB @1559~1606MHz 39 dB @2300~2370MHz 42 dB @2510~2570MHz	1.1*0.9*0.65	SAFFB2G45MAOFOA
<u>KCT3233</u>	2.4GHz Wi-Fi (High Performance)	2.4	1.5	33 dB @1559~1606MHz 53 dB @2300~2370MHz 49 dB @2500~2505MHz	1.1*0.9*0.65	SAFOA2G45MAOGOA

Diplexer

Part No.	Frequency (GHz)	Isolation (dB)	Insertion Loss (dB)	Return Loss (dB)	Attenuation (dB)	Package (mm)
<u>KCT2494G93T01AB</u>	2400-2496 4900-5950	30 @ 0.03~2.7GHz 28 @ 4.9-5.95GHz	0.50 @2.4~2.5GHz 1.10 @4.9~5.95GHz	18 @2.4~2.5GHz 20 @4.9~5.95GHz	28 @4.8~5.95GHz 17 @9.8~11.9GHz	1.6*0.8mm
<u>KCT2494G93T11AB</u>	2400-2496 4900-5950	30 @ 0.03~2.7GHz 28 @ 4.9-5.95GHz	0.50 @2.4~2.5GHz 1.10 @4.9~5.95GHz	18 @2.4~2.5GHz 20 @4.9~5.95GHz	28 @4.8~5.95GHz 17 @9.8~11.9GHz	1.6*0.8mm
<u>KCT2494G93J01AA</u>	2400-2500 5150-7125	39 @ 2.4 - 2.5GHz 35 @ 5.15-7.125GHz	0.56 @ 2.4 - 2.5GHz 0.88 @ 5.15-7.125GHz	20 @ 2.4 - 2.5GHz 14 @ 5.15-7.125GHz	41 @ 2.4 - 2.5GHz 40 @15.15-17.625GHz	1.6*0.8mm

RF FEM

Part No.	Frequency (GHz)	Voltage (V)	Psat (dBm)	RX NF (dB)	Package (mm)	P2P Part
<u>KCT8101L</u>	0.78~0.96	3.3	27.5	3.0	QFN16L 3*3*0.75	RFX1010
<u>RT201</u>	2.4~2.5	3.3	22.5	3.0	QFN16L 3*3*0.75	RFX2401C
<u>RT202</u>	2.4~2.5	3.3	22.5	3.0	QFN16L 3*3*0.75	RFX2402E
<u>KCT8204L</u>	2.4~2.5	3.3	22.5	3.0	QFN16L 3*3*0.55	/
<u>KCT8205L</u>	2.4~2.5	3.3	22.5	3.0	QFN16L 3*3*0.75	RFX2411N
<u>KCT8206L</u>	2.4~2.5	3.3	21.5	3.0	QFN16L 3*3*0.75	RFX2401C

LNA/SW

Part No.	Frequency (GHz)	Vcc (V)	LNA Gain (dB)	NF (dB)	Bypass Loss (dB)	Package (mm)	P2P Part
<u>KCT4521L</u>	5.15~5.85	3.3	17	1.9	4.5	QFN16L 2.3*2.3*0.55	RFFM4554
<u>KCT4221L</u>	2.4~2.5	3.3	15	1.4	6	QFN16L 2.3*2.3*0.55	SKY85201 RTC7663
<u>KCT4222L</u>	2.4~2.5	3.3	10	2.5	1.5	QFN16L 2.3*2.3*0.55	SKY85201 RTC7663

Wireless Connectivity

WLAN FEM

Part No.	Protocol	Vcc (V)	TX Power @ -35dB (dBm)	TX Icq (mA)	RX NF (dB)	Package (mm)	Qualcomm Platform	P2P Part
<u>KCT8552C</u>	Wi-Fi 5	3.3	17.5	200	3.0	QFN16L 2.3*2.3*0.55	QCA6164A QCA6174A QCA9377	SKY85716-11 RFFM8528
<u>KCT8553C</u>	Wi-Fi 5	3.3 3.7	18 19	200 210	3.0 3.0	QFN16L 2.3 * 2.3 *0.55	WCN3660B (3rd Generation)	SKY85720-11 RFFM8516 RTC7637S
<u>KCT8255HE</u>	Wi-Fi 6	3.8	21.5	150	2.2	MIS 16L, 2.0*2.4*0.65	WCN6850/51 WCN6855/56	WLAN7207H QM42195

Automotive V2X

5GHz FEM

Part No.	Vcc (V)	Output Power TC1 (dBm)	Gain (dB)	LTE EVM %	ACPR (dBc)	TX Icq (mA)	RX Gain (dB)	RX NF (dB)	Package (mm)	P2P Part
<u>KCT7526AT</u>	5	26	31	3.2	-36	165	15.5	1.7	QFN16L 3*3*0.55	RFFM8500Q
<u>KCT7528AT</u>	5	27	30	3.2	-36	195	17	1.8	QFN24L 3*5*0.75	SKY21043

Naming Rule

Function type		Protocol / Customization / Function	
2	Switch		
3	Filter	C, D, H S, SD, HE HT AT	Wi-Fi 5 Products
4	LNA/SW		Wi-Fi 6 Products
6	PA		Wi-Fi 7 Products
7	Automotive C-V2X		Automotive Products
8	FEM	Q, QL	Quantenna Platform
9	iFEM (integrated FEM)	L	Low Voltage Product
Frequency band		N	Linearizable FEM
1	Sub 1GHz	Application	
2	2.4GHz		
3	N77/N78 Band	0,1	Bluetooth / NB-IoT/ ZigBee
5	5GHz	2,3,4,7,8	Wi-Fi Infrastructure
6	6E EU Band	5,6,	Cellular
7	6E US Band		
8	Dual Band		



Thank you

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Note: This document is subject to the latest released version, the previous data is invalid



EXHIBIT 5

ENTITY INFORMATION

ENTITY INFORMATION

Entity Name:

GRAND CHIP LABS INC

Entity Number:

E0368252016-4

Entity Type:

Domestic Corporation (78)

Entity Status:

Active

Formation Date:

08/21/2016

NV Business ID:

NV20161493127

Termination Date:

Annual Report Due Date:

8/31/2024

Compliance Hold:

REGISTERED AGENT INFORMATION

Name of Individual or Legal Entity:

Registered Agents Inc.*

Status:

Active

CRA Agent Entity Type:

Registered Agent Type:

Commercial Registered Agent

NV Business ID:

Office or Position:

Manager

Jurisdiction:

Street Address:

401 Ryland st, ste 200a, Reno, NV, 89502, USA

Mailing Address:

OFFICER INFORMATION

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President	PING PENG	2692 BELGREEN ST, LAS VEGAS, NV, 89135, USA	07/04/2022	Active
Secretary	KATHY LI	2692 BELGREEN ST, LAS VEGAS, NV, 89135, USA	07/04/2022	Active
Treasurer	PING PENG	2692 BELGREEN ST, LAS VEGAS, NV, 89135, USA	07/04/2022	Active
Director	PING PENG	2692 BELGREEN ST, LAS VEGAS, NV, 89135, USA	07/04/2022	Active

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Number of No Par Value Shares:

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EXHIBIT 6

9469425



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United States Patent and Trademark Office

March 21, 2024

THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM
THE RECORDS OF THIS OFFICE OF:

PATENT NUMBER: 8,717,101

ISSUE DATE: May 6, 2014

By Authority of the
Under Secretary of Commerce for Intellectual Property
and Director of the United States Patent and Trademark Office

John Burson
Certifying Officer





US008717101B2

(12) **United States Patent**
Li et al.

(10) **Patent No.:** **US 8,717,101 B2**
(45) **Date of Patent:** **May 6, 2014**

(54) **APPARATUS AND METHODS FOR BIASING POWER AMPLIFIERS**

(75) Inventors: **Ping Li**, Dunstable, MA (US); **Paul T. DiCarlo**, Marlborough, MA (US)

(73) Assignee: **Skyworks Solutions, Inc.**, Woburn, MA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 23 days.

(21) Appl. No.: **13/468,749**

(22) Filed: **May 10, 2012**

(65) **Prior Publication Data**

US 2012/0286873 A1 Nov. 15, 2012

Related U.S. Application Data

(60) Provisional application No. 61/486,186, filed on May 13, 2011.

(51) **Int. Cl.**
H03G 3/30 (2006.01)

(52) **U.S. Cl.**
USPC **330/285; 330/278**

(58) **Field of Classification Search**
USPC 330/285, 296, 278, 298, 288
See application file for complete search history.

(56) **References Cited**

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* cited by examiner

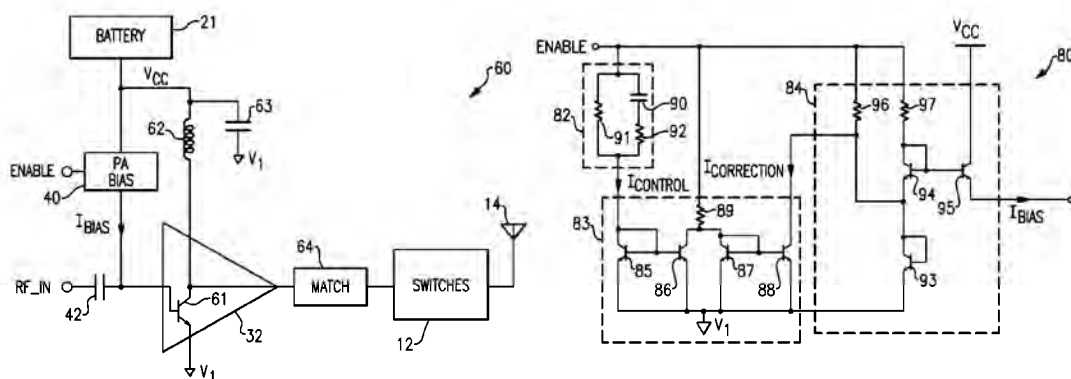
Primary Examiner — Hieu Nguyen

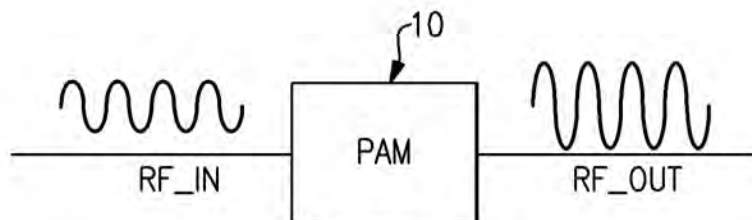
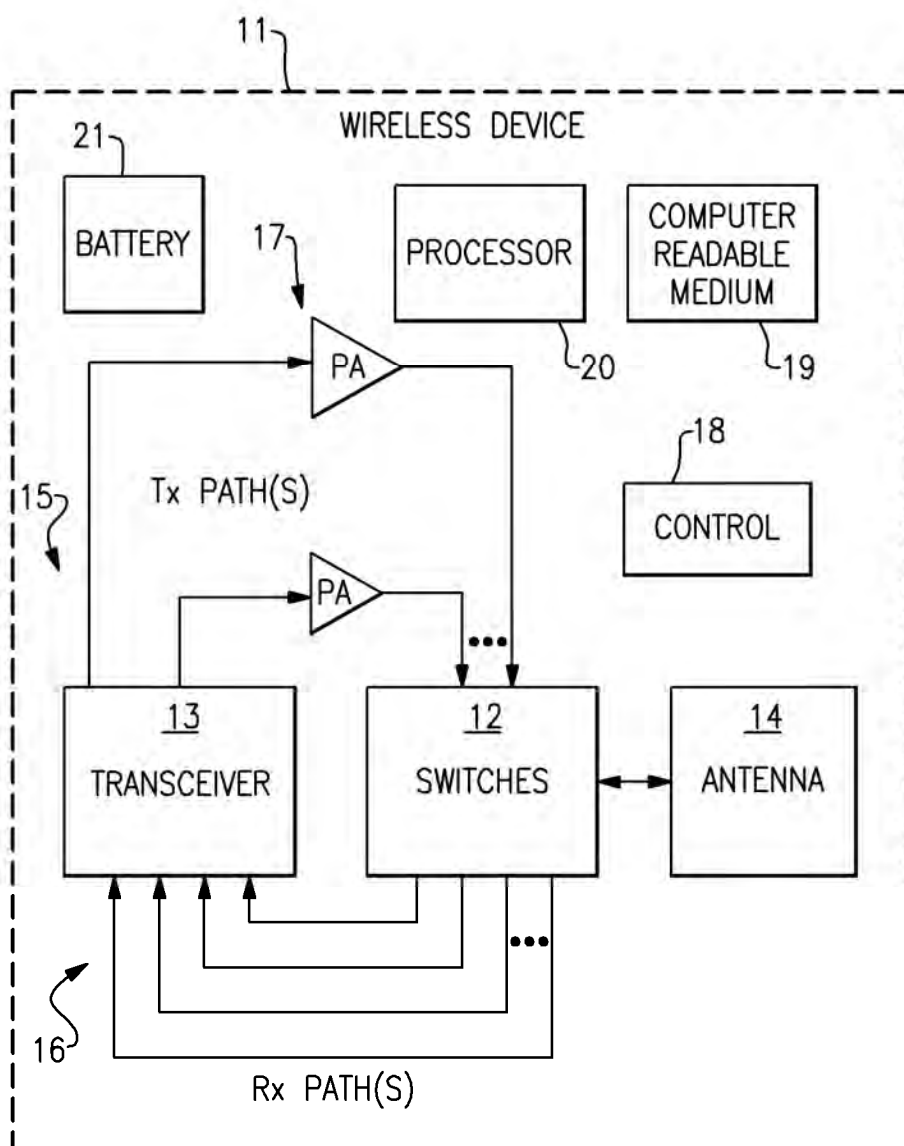
(74) *Attorney, Agent, or Firm* — Knobbe, Martens, Olson & Bear, LLP

(57) **ABSTRACT**

Apparatus and methods for biasing a power amplifier are disclosed. In one embodiment, a method of biasing a power amplifier includes shaping an enable signal using a time-dependent signal generator to generate a control current, amplifying the control current using a current amplifier to generate a correction current, and generating a bias current for a power amplifier using a primary biasing circuit. The primary biasing circuit is configured to use the correction current to correct for a variation in gain of the power amplifier when the power amplifier is enabled.

25 Claims, 7 Drawing Sheets



**FIG. 1****FIG. 2**

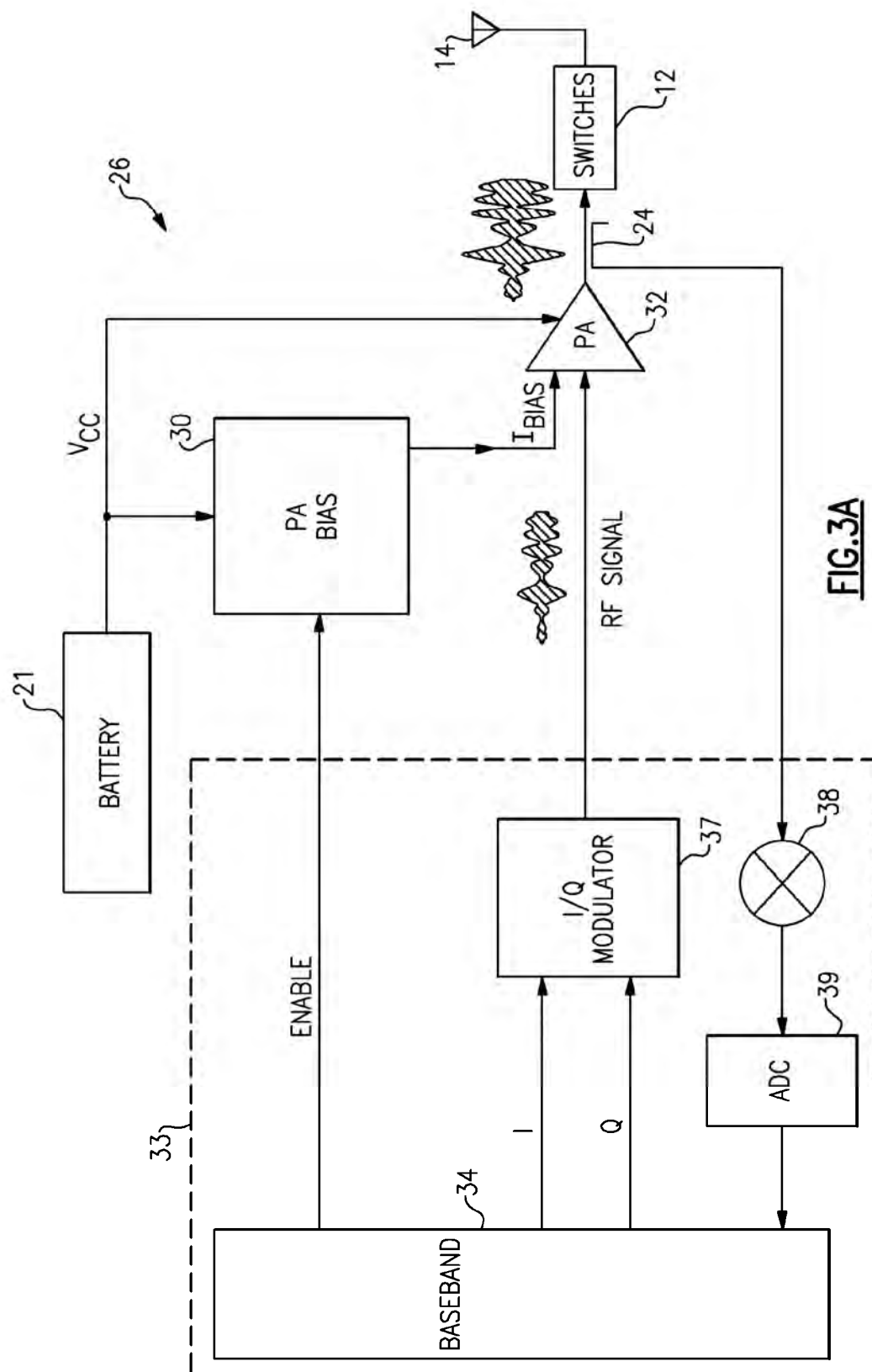
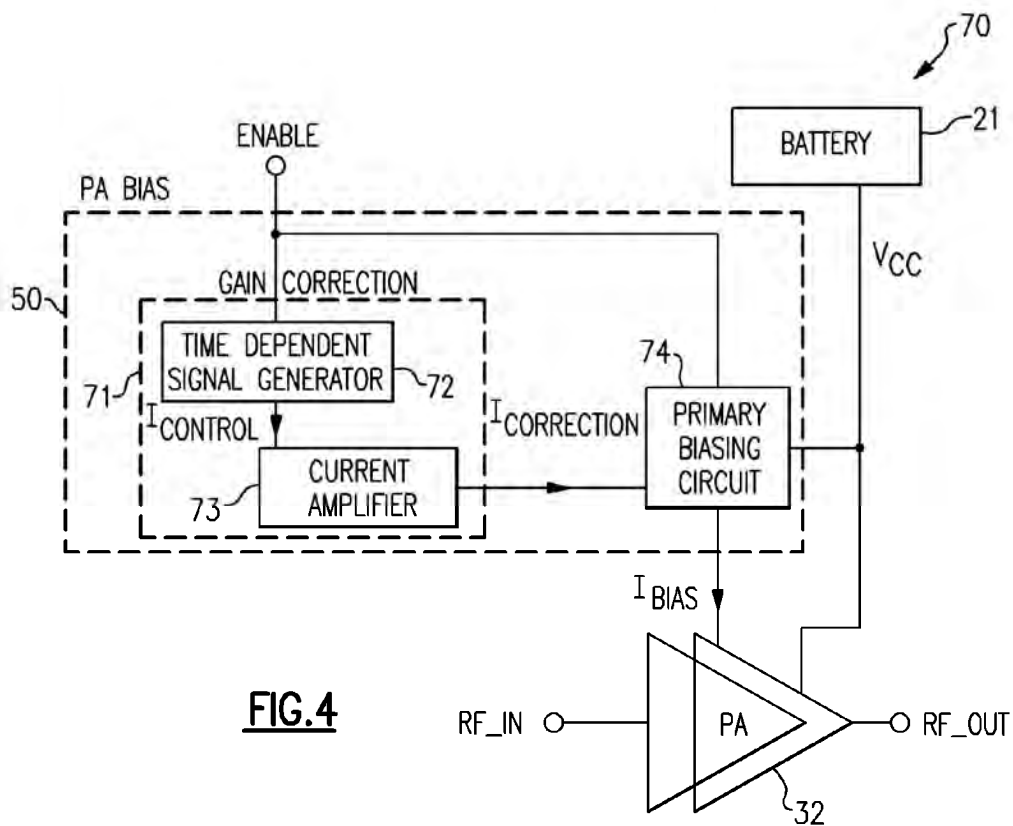
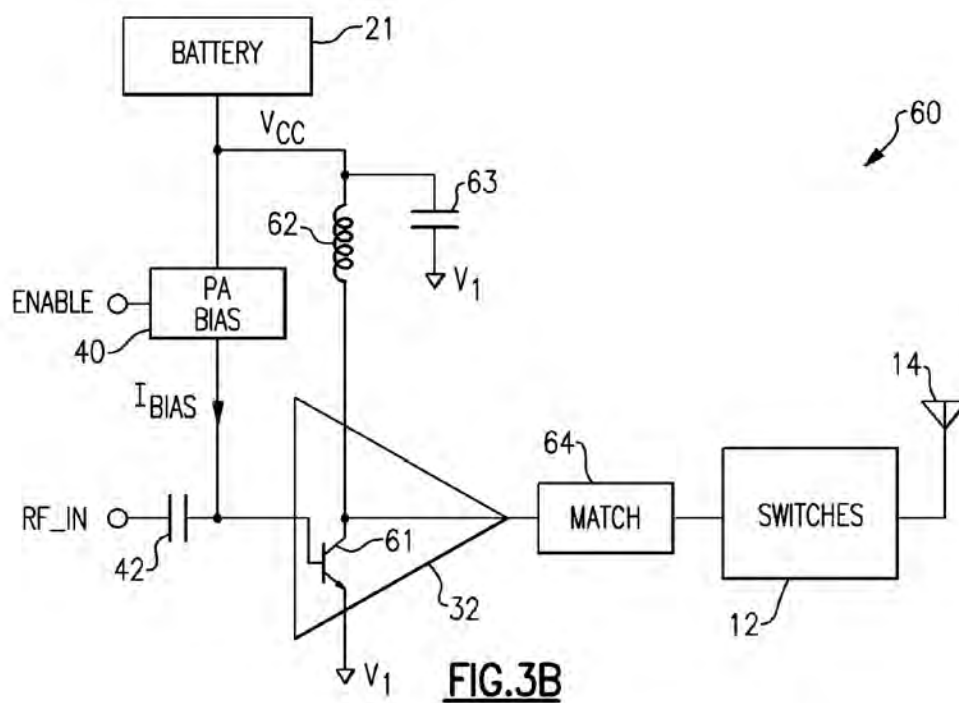


FIG. 3A



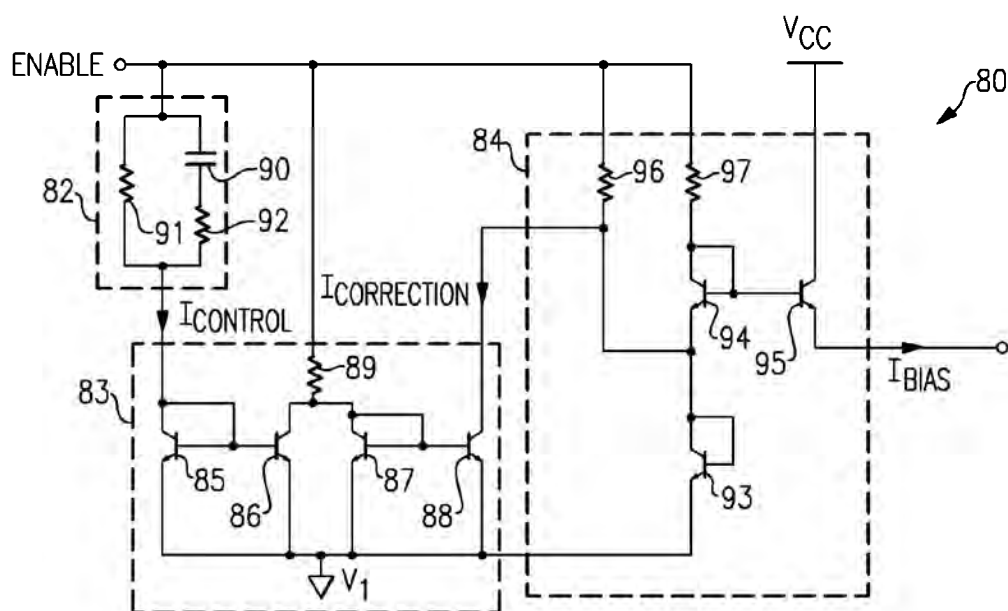


FIG. 5

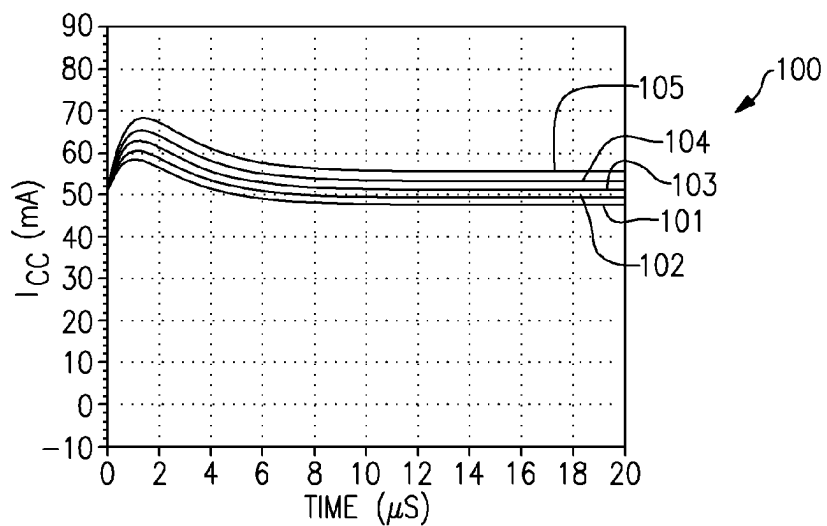


FIG. 6

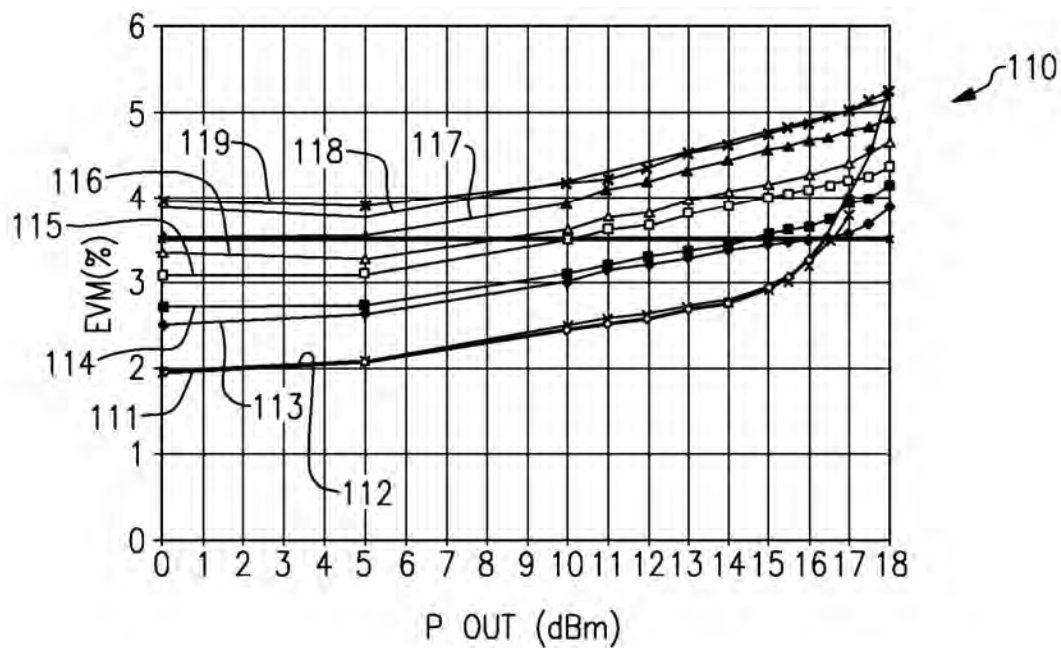


FIG. 7A

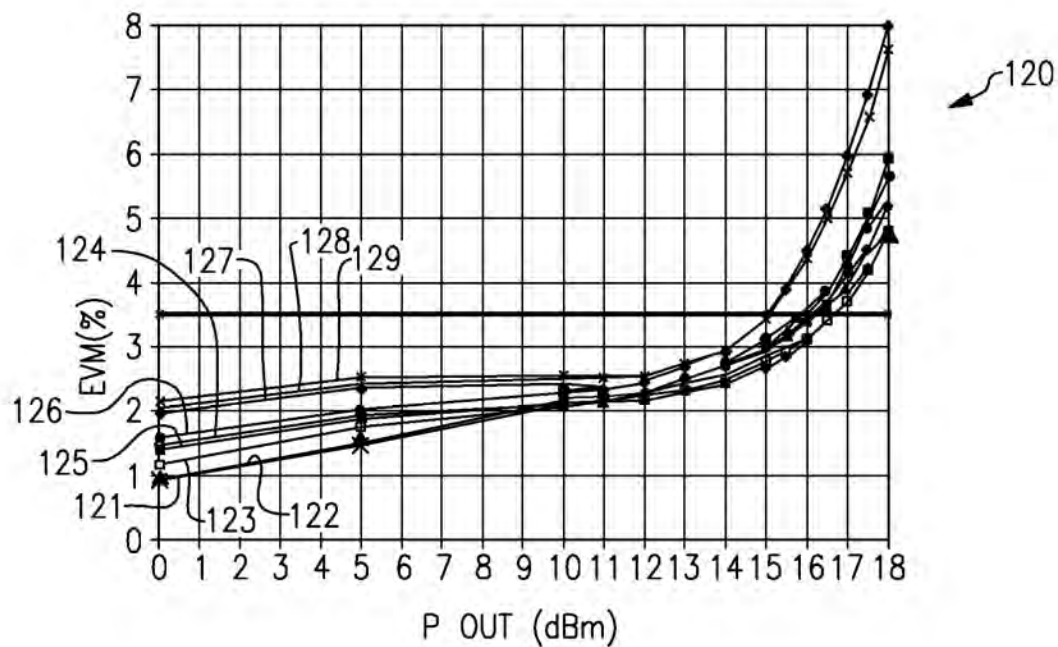
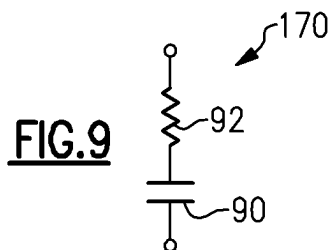
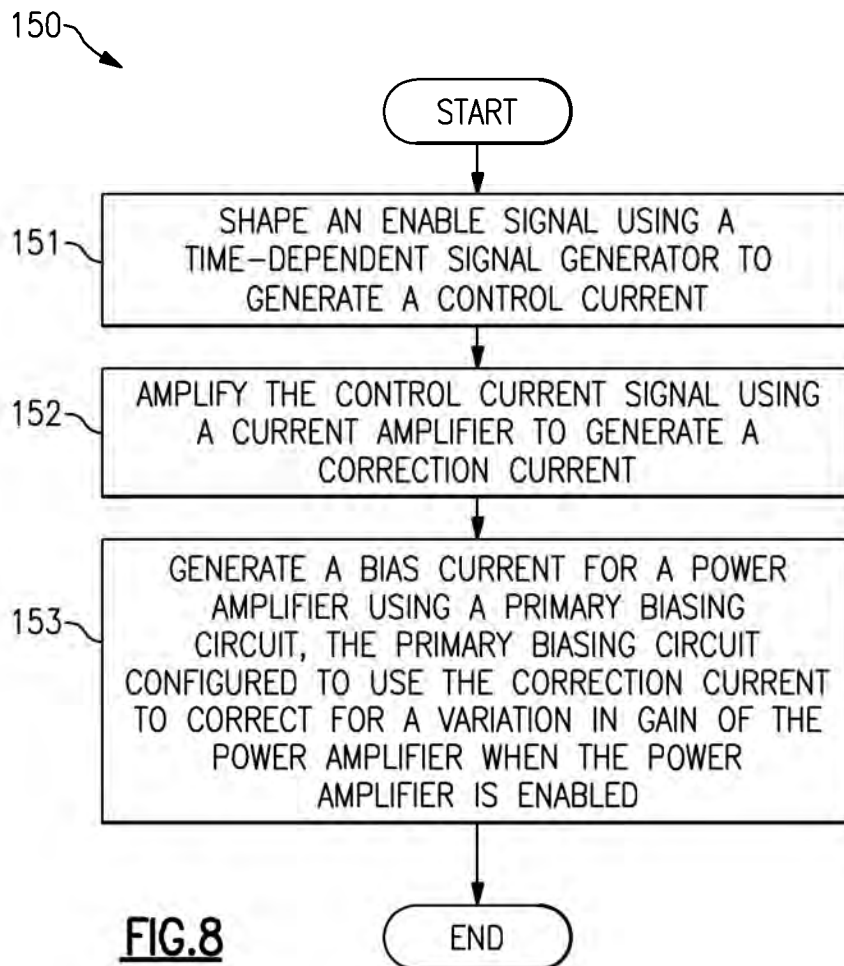


FIG. 7B



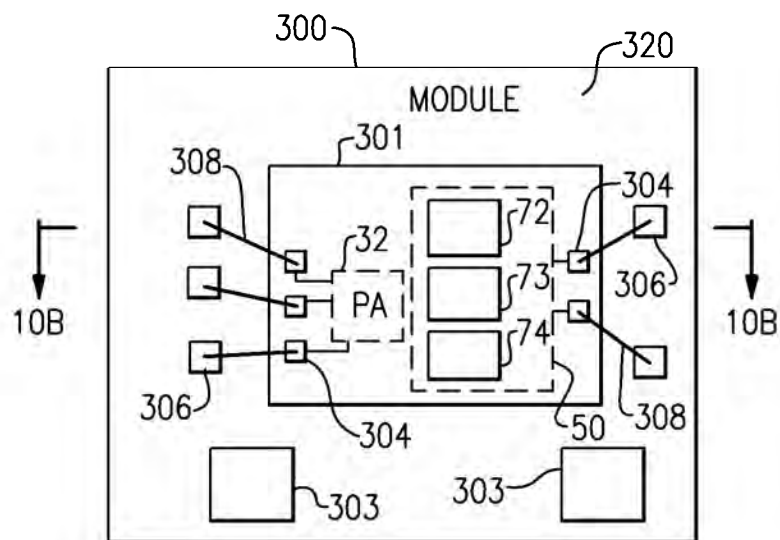


FIG. 10A

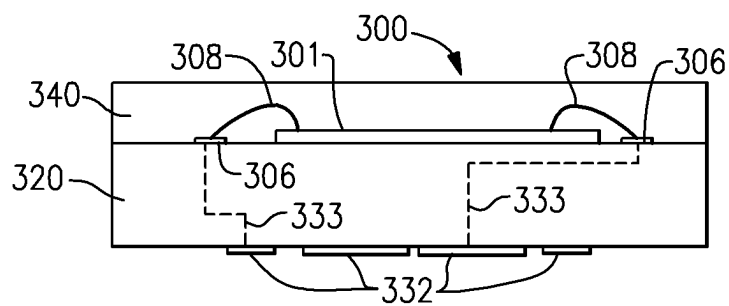


FIG. 10B

US 8,717,101 B2

1

APPARATUS AND METHODS FOR BIASING
POWER AMPLIFIERSCROSS-REFERENCE TO RELATED
APPLICATIONS

This application claims the benefit of priority under 35 U.S.C. §119(e) of U.S. Provisional Patent Application No. 61/486,186, filed May 13, 2011 entitled "APPARATUS AND METHODS FOR BIASING POWER AMPLIFIERS", which is herein incorporated by reference in its entirety.

BACKGROUND

1. Field

Embodiments of the invention relate to electronic systems, and in particular, to radio frequency (RF) electronics.

2. Description of the Related Technology

RF power amplifiers can be used to boost the power of a RF signal having a relatively low power. Thereafter, the boosted RF signal can be used for a variety of purposes, included driving the antenna of a transmitter.

Power amplifiers can be included in mobile phones to amplify a RF signal for transmission. For example, in mobile phones that communicate using a wireless local area network (WLAN) protocol and/or any other suitable communication standard, a power amplifier can be used to amplify the RF signal. It can be important manage the amplification of a RF signal, as amplifying the RF signal to an incorrect power level can cause a wireless device to transmit out of band.

There is a need for improved power amplifier systems. Furthermore, there is a need for improving power amplifier biasing.

SUMMARY

In certain embodiments, the present disclosure relates to a power amplifier system including a power amplifier configured to amplify a radio frequency (RF) signal and a bias block for biasing the power amplifier. The bias block includes a time dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current, a current amplifier configured to amplify the control current to generate a correction current, and a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current. The bias current is configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled.

In several embodiments, the time dependent signal generator includes a resistor-capacitor (RC) network. In accordance with a number of embodiments, the RC network includes a first resistor and a first capacitor electrically connected in series between the current amplifier and an input of the bias circuit configured to receive the enable signal. In several embodiments, the RC network further includes a second resistor having a first end electrically connected to the input of the current mirror and a second end electrically connected to the input of the bias circuit configured to receive the enable signal.

According to certain embodiments, the second resistor has a resistance ranging between about 10 k Ω and about 100 k Ω , the first capacitor has a capacitance ranging between about 10 pF and about 100 pF, and the first resistor has a resistance ranging between about 10 k Ω and about 100 k Ω .

In a number of embodiments, the current amplifier includes a current mirror. In several embodiments, the current mirror includes a first bipolar transistor and a second bipolar trans-

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sistor, the first bipolar transistor including an emitter electrically connected to an emitter of the second bipolar transistor and to a power low voltage, and a collector electrically connected to a base of the first bipolar transistor and to a base of the second bipolar transistor, the collector of the first bipolar transistor configured to receive at least a portion of the control current. In certain embodiments, the current mirror further includes a resistor, a third bipolar transistor and a fourth bipolar transistor, the third bipolar transistor including an emitter electrically connected to an emitter of the fourth bipolar transistor and to the power low voltage, and a collector electrically connected to a first end of the resistor, to the collector of the second bipolar transistor, to a base of the third bipolar transistor, and to a base of the fourth bipolar transistor, the collector of the fourth bipolar transistor configured to generate the compensation current. In several embodiments, the resistor further includes a second end configured to receive the enable signal.

According to some embodiments, the power amplifier system further includes a transceiver for providing the RF signal to the power amplifier.

In a number of embodiments, the power amplifier includes a bipolar transistor having an emitter, a base and a collector, the base configured to receive the RF signal and the bias current. In certain embodiments, the emitter is electrically connected to a power low voltage and the collector is configured to generate an amplified version of the RF signal.

In several embodiments, the primary bias circuit includes a first resistor, a second resistor, a first bipolar transistor, and a second bipolar transistor, the first resistor including a first end electrically connected to the emitter of the first bipolar transistor at a node configured to receive the correction current, and a second end electrically connected to a first end of the second resistor at a node of the bias circuit configured to receive the enable signal, the second resistor including a second end electrically connected to a collector of the first bipolar transistor, a base of the first bipolar transistor, and to a base of the second bipolar transistor. According to certain embodiments, the second bipolar transistor includes a collector electrically connected to a battery voltage and an emitter configured to generate the bias current. In a number of embodiments, the primary bias circuit further includes a third bipolar transistor having an emitter electrically connected to the power low voltage and a base and a collector electrically connected to the emitter of the first bipolar transistor.

In certain embodiments, the present disclosure relates to a method of biasing a power amplifier. The method includes shaping an enable signal using a time-dependent signal generator to generate a control current, amplifying the control current using a current amplifier to generate a correction current, and generating a bias current for a power amplifier using a primary biasing circuit, the primary biasing circuit configured to use the correction current to correct for a variation in gain of the power amplifier when the power amplifier is enabled.

In a number of embodiments, shaping the enable signal includes using a resistor capacitor (RC) network of the time dependent signal generator. In some embodiments, the RC network includes a first resistor and a first capacitor electrically connected in series, the RC network configured to receive the enable signal and to generate the control current.

In several embodiments, amplifying the control current further includes amplifying the control current using a current mirror of the current amplifier.

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In accordance with a number of embodiments, generating the bias current includes shaping the bias current so as to compensate for a gain variation of a heterojunction bipolar transistor (HBT).

In certain embodiments, the present disclosure relates to a bias circuit for biasing a power amplifier. The bias circuit includes a time dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current, a current amplifier configured to amplify the control current to generate a correction current, and a primary biasing block configured to generate a bias current for the power amplifier based at least partly on the correction current. The bias current is configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled.

In several embodiments, the time dependent signal generator includes a resistor-capacitor (RC) network. In a number of embodiments, the RC network includes a first resistor and a first capacitor electrically connected in series between the current amplifier and an input of the bias circuit configured to receive the enable signal.

In accordance with certain embodiments, the current amplifier includes a current mirror.

In several embodiments, the primary bias block includes a first resistor, a second resistor, a first bipolar transistor, and a second bipolar transistor, the first resistor including a first end electrically connected to the emitter of the first bipolar transistor at a node configured to receive the correction current, and a second end electrically connected to a first end of the second resistor at a node of the bias circuit configured to receive the enable signal, the second resistor including a second end electrically connected to a collector of the first bipolar transistor, a base of the first bipolar transistor, and to a base of the second bipolar transistor. In a number of embodiments, the second bipolar transistor includes a collector electrically connected to a battery voltage and an emitter configured to generate the bias current.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a power amplifier module for amplifying a radio frequency (RF) signal.

FIG. 2 is a schematic block diagram of an example wireless device that can include one or more of the power amplifier modules of FIG. 1.

FIG. 3A is a schematic block diagram of one example of a power amplifier system.

FIG. 3B is a schematic block diagram of another example of a power amplifier system.

FIG. 4 is a schematic block diagram of one example of a power amplifier system including a power amplifier bias block according to one embodiment.

FIG. 5 is a circuit diagram of a power amplifier bias block according to one embodiment.

FIG. 6 is a graph of one example of collector current versus time.

FIG. 7A is a graph of one example of dynamic error vector magnitude (EVM) versus output power.

FIG. 7B is a graph of another example of dynamic EVM versus output power.

FIG. 8 is a flow chart illustrating a method for biasing a power amplifier in accordance with one embodiment.

FIG. 9 is a circuit diagram of a time-dependent signal generator in accordance with one embodiment.

FIG. 10A is a schematic diagram of one example of a packaged power amplifier module.

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FIG. 10B is a schematic diagram of a cross-section of the packaged power amplifier module of FIG. 10A taken along the lines 10B-10B.

DETAILED DESCRIPTION OF EMBODIMENTS

The headings provided herein, if any, are for convenience only and do not necessarily affect the scope or meaning of the claimed invention.

Apparatus and methods for biasing power amplifiers are disclosed herein. In certain implementations, a power amplifier and a power amplifier bias block are provided. The power amplifier can be used to amplify a radio frequency (RF) signal for transmission, and the power amplifier bias block can be used to bias the power amplifier. The power amplifier bias block can receive an enable signal that can be used to enable or disable the power amplifier so as to pulse the power amplifier's output.

In certain implementations, the power amplifier bias block includes a primary biasing circuit and a gain correction block including a time-dependent signal generator and a current amplifier. The time-dependent signal generator or control block can be used to shape the enable signal so as to generate a control current, which can be amplified by the current amplifier to generate a correction current. The power amplifier bias block can generate a bias current for the power amplifier using the primary biasing circuit and the correction current. The correction current can be used to adjust the magnitude of the bias current so as to compensate for a variation in gain of the power amplifier over time when the power amplifier is transitioned from a disabled state to an enabled state. For example, shortly after a power amplifier is enabled, absent compensation the current of a primary biasing circuit can come up slow due to thermal effects, and the power amplifier's gain can be low. By including the time-dependent signal generator and the current amplifier, a current boost can be provided to the power amplifier so as to provide the power amplifier with a substantially flat gain response versus time. Correcting for gain variation in the power amplifier can improve the power amplifier's performance, including, for example, the power amplifier's dynamic error vector magnitude (EVM).

Overview of Power Amplifier Systems

FIG. 1 is a schematic diagram of a power amplifier module 10 for amplifying a radio frequency (RF) signal. The illustrated power amplifier module (PAM) 10 can be configured to amplify an RF signal RF_IN to generate an amplified RF signal RF_OUT. As described herein, the power amplifier module 10 can include one or more power amplifiers, including, for example, multi-stage power amplifiers.

FIG. 2 is a schematic block diagram of an example wireless or mobile device 11 that can include one or more of the power amplifier modules of FIG. 1. The wireless device 11 can include power amplifier bias circuits implementing one or more features of the present disclosure.

The example wireless device 11 depicted in FIG. 2 can represent a multi-band and/or multi-mode device such as a multi-band/multi-mode mobile phone. In certain embodiments, the wireless device 11 can include switches 12, a transceiver 13, an antenna 14, power amplifiers 17, a control component 18, a computer readable medium 19, a processor 20, and a battery 21.

The transceiver 13 can generate RF signals for transmission via the antenna 14. Furthermore, the transceiver 13 can receive incoming RF signals from the antenna 14.

It will be understood that various functionalities associated with the transmission and receiving of RF signals can be

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achieved by one or more components that are collectively represented in FIG. 2 as the transceiver 13. For example, a single component can be configured to provide both transmitting and receiving functionalities. In another example, transmitting and receiving functionalities can be provided by separate components.

Similarly, it will be understood that various antenna functionalities associated with the transmission and receiving of RF signals can be achieved by one or more components that are collectively represented in FIG. 2 as the antenna 14. For example, a single antenna can be configured to provide both transmitting and receiving functionalities. In another example, transmitting and receiving functionalities can be provided by separate antennas. In yet another example, different bands associated with the wireless device 11 can be provided with different antennas.

In FIG. 2, one or more output signals from the transceiver 13 are depicted as being provided to the antenna 14 via one or more transmission paths 15. In the example shown, different transmission paths 15 can represent output paths associated with different bands and/or different power outputs. For instance, the two example power amplifiers 17 shown can represent amplifications associated with different power output configurations (e.g., low power output and high power output), and/or amplifications associated with different bands. Although FIG. 2 illustrates a configuration using two transmission paths 15, the wireless device 11 can be adapted to include more or fewer transmission paths 15.

The power amplifiers 17 can be used to amplify a wide variety of RF signals. For example, one or more of the power amplifiers 17 can receive an enable signal that can be used to pulse the output of the power amplifier to aid in transmitting a wireless local area network (WLAN) signal or any other suitable pulsed signal. Each of the power amplifiers 17 need not amplify the same type of signal. For example, one power amplifier can amplify a WLAN signal, while another power amplifier can amplify, for example, a Global System for Mobile (GSM) signal, a code division multiple access (CDMA) signal, a W-CDMA signal, a Long Term Evolution (LTE) signal, or an EDGE signal.

One or more features of the present disclosure can be implemented in the foregoing example modes and/or bands, and in other communication standards.

In FIG. 2, one or more detected signals from the antenna 14 are depicted as being provided to the transceiver 13 via one or more receiving paths 16. In the example shown, different receiving paths 16 can represent paths associated with different bands. Although FIG. 2 illustrates a configuration using four receiving paths 16, the wireless device 11 can be adapted to include more or fewer receiving paths 16.

To facilitate switching between receive and transmit paths, the switches 12 can be configured to electrically connect the antenna 14 to a selected transmit or receive path. Thus, the switches 12 can provide a number of switching functionalities associated with an operation of the wireless device 11. In certain embodiments, the switches 12 can include a number of switches configured to provide functionalities associated with, for example, switching between different bands, switching between different power modes, switching between transmission and receiving modes, or some combination thereof. The switches 12 can also be configured to provide additional functionality, including filtering and/or duplexing of signals.

FIG. 2 shows that in certain embodiments, a control component 18 can be provided for controlling various control functionalities associated with operations of the switches 12, the power amplifiers 17, and/or other operating component

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(s). Non-limiting examples of the control component 18 are described herein in greater detail.

In certain embodiments, a processor 20 can be configured to facilitate implementation of various processes described herein. For the purpose of description, embodiments of the present disclosure may also be described with reference to flowchart illustrations and/or block diagrams of methods, apparatus (systems) and computer program products. It will be understood that each block of the flowchart illustrations and/or block diagrams, and combinations of blocks in the flowchart illustrations and/or block diagrams, may be implemented by computer program instructions. These computer program instructions may be provided to a processor of a general purpose computer, special purpose computer, or other programmable data processing apparatus to produce a machine, such that the instructions, which execute via the processor of the computer or other programmable data processing apparatus, create means for implementing the acts specified in the flowchart and/or block diagram block or blocks.

In certain embodiments, these computer program instructions may also be stored in a computer-readable memory 19 that can direct a computer or other programmable data processing apparatus to operate in a particular manner, such that the instructions stored in the computer-readable memory produce an article of manufacture including instruction means which implement the acts specified in the flowchart and/or block diagram block or blocks. The computer program instructions may also be loaded onto a computer or other programmable data processing apparatus to cause a series of operations to be performed on the computer or other programmable apparatus to produce a computer implemented process such that the instructions that execute on the computer or other programmable apparatus provide steps for implementing the acts specified in the flowchart and/or block diagram block or blocks.

The battery 21 can be any suitable battery for use in the wireless device 11, including, for example, a lithium-ion battery.

FIG. 3A is a schematic block diagram of one example of a power amplifier system 26. The illustrated power amplifier system 26 includes the switches 12, the antenna 14, the battery 21, a directional coupler 24, a power amplifier bias block 30, a power amplifier 32, and a transceiver 33. The illustrated transceiver 33 includes a baseband processor 34, an I/Q modulator 37, a mixer 38, and an analog-to-digital converter (ADC) 39.

The baseband signal processor 34 can be used to generate an I signal and a Q signal, which can be used to represent a sinusoidal wave or signal of a desired amplitude, frequency, and phase. For example, the I signal can be used to represent an in-phase component of the sinusoidal wave and the Q signal can be used to represent a quadrature component of the sinusoidal wave, which can be an equivalent representation of the sinusoidal wave. In certain implementations, the I and Q signals can be provided to the I/Q modulator 37 in a digital format. The baseband processor 34 can be any suitable processor configured to process a baseband signal. For instance, the baseband processor 34 can include a digital signal processor, a microprocessor, a programmable core, or any combination thereof. Moreover, in some implementations, two or more baseband processors 34 can be included in the power amplifier system 26.

The I/Q modulator 37 can be configured to receive the I and Q signals from the baseband processor 34 and to process the I and Q signals to generate a RF signal. For example, the I/Q modulator 37 can include DACs configured to convert the I

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and Q signals into an analog format, mixers for upconverting the I and Q signals to radio frequency, and a signal combiner for combining the upconverted I and Q signals into a RF signal suitable for amplification by the power amplifier 32. In certain implementations, the I/Q modulator 37 can include one or more filters configured to filter frequency content of signals processed therein.

The power amplifier bias block 30 can receive an enable signal ENABLE from the baseband processor 34 and a battery or power high voltage V_{CC} from the battery 21, and can use the enable signal ENABLE to generate a bias current I_{BIAS} for the power amplifier 32. Although FIG. 3A illustrates the battery 21 directly generating the power high voltage V_{CC} , in certain implementations the power high voltage V_{CC} can be a regulated voltage generated by a regulator that is electrically powered using the battery 21. The power amplifier 32 can receive the RF signal from the I/Q modulator 37 of the transceiver 33, and can provide an amplified RF signal to the antenna 14 through the switches 12.

The directional coupler 24 can be positioned between the output of the power amplifier 32 and the input of the switches 12, thereby allowing an output power measurement of the power amplifier 32 that does not include insertion loss of the switches 12. The sensed output signal from the directional coupler 24 can be provided to the mixer 38, which can multiply the sensed output signal by a reference signal of a controlled frequency so as to downshift the frequency content of the sensed output signal to generate a downshifted signal. The downshifted signal can be provided to the ADC 39, which can convert the downshifted signal to a digital format suitable for processing by the baseband processor 34. By including a feedback path between the output of the power amplifier 32 and the baseband processor 34, the baseband processor 34 can be configured to dynamically adjust the I and Q signals to optimize the operation of the power amplifier system 26. For example, configuring the power amplifier system 26 in this manner can aid in controlling the power added efficiency (PAE) and/or linearity of the power amplifier 32.

FIG. 3B is a schematic block diagram of another example of a power amplifier system 60. The illustrated power amplifier system 60 includes a power amplifier bias block 40, the battery 21, the power amplifier 32, an inductor 62, a first capacitor 63, a second capacitor 42, an impedance matching block 64, the switches 12, and the antenna 14.

The illustrated power amplifier 32 includes a bipolar transistor 61 having an emitter, a base, and a collector. The emitter of the bipolar transistor 61 can be electrically connected to a first or power low voltage V_1 , which can be, for example, ground, and a radio frequency input signal RF_IN can be provided to the base of the bipolar transistor 61 through the first capacitor 42. The bipolar transistor 61 can amplify the RF input signal RF_IN and provide the amplified RF signal at the collector. The bipolar transistor 61 can be any suitable device. In one implementation, the bipolar transistor 61 is a heterojunction bipolar transistor (HBT).

The power amplifier 32 can be configured to provide the amplified RF signal to the switches 12. The impedance matching block 64 can be used to aid in terminating the electrical connection between the power amplifier 32 and the switches 12. For example, the impedance matching block 64 can be used to increase power transfer and/or reduce reflections of the amplified RF signal.

The inductor 62 can be included to aid in electrically powering the power amplifier 32 with the power high voltage V_{CC} from the battery 21 while choking or blocking high frequency RF signal components. The inductor 62 can include a first end electrically connected to the power high voltage V_{CC} and a

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second end electrically connected to the collector of the bipolar transistor 61. The first or decoupling capacitor 63 is electrically connected between the power high voltage V_{CC} and the power low voltage V_1 and can provide a low impedance path to high frequency signals, thereby reducing the noise of the power high voltage V_{CC} , improving power amplifier stability, and/or improving the performance of the inductor 62 as a RF choke.

The power amplifier bias block 40 is configured to receive an enable signal ENABLE and the battery or power high voltage V_{CC} . The power amplifier bias block 40 can use the enable signal ENABLE and the battery voltage V_{CC} to generate a bias current I_{BIAS} for biasing the power amplifier 32. For example, as illustrated in FIG. 3B, the power amplifier bias block 40 can be used to generate a bias current I_{BIAS} that can be used to bias the base of the bipolar transistor 61 of the power amplifier 32. The power amplifier bias block 40 can use the enable signal ENABLE to control or vary a magnitude of the bias current I_{BIAS} so as to enable or disable the power amplifier and thereby pulse the power amplifier's output. For example, when the enable signal ENABLE indicates the power amplifier 32 should be activated, the power amplifier bias block 40 can change the amplitude of the bias current I_{BIAS} so as to achieve a desired gain of the power amplifier 32. Similarly, when the enable signal ENABLE indicates that the power amplifier 32 should be deactivated, the power amplifier bias block 40 can decrease the bias current I_{BIAS} such that the gain of the power amplifier 32 is equal to about 0.

Although FIG. 3B illustrates one implementation of the power amplifier 32, skilled artisans will appreciate that the teachings described herein can be applied to a variety of power amplifier structures, including, for example, multi-stage power amplifier structures and/or power amplifiers employing other transistor structures.

Overview of Power Amplifier Bias Circuits

In certain implementations described herein, a power amplifier bias block includes a primary biasing circuit and a gain correction block including a time-dependent signal generator and a current amplifier. The time-dependent signal generator can be used to shape the enable signal of the power amplifier so as to generate a control current, which can be amplified by the current amplifier to generate a correction current. The primary biasing circuit can use the correction current to correct for a variation in gain of the power amplifier that can occur shortly after the power amplifier is enabled. Compensating for gain variation in the power amplifier can improve the power amplifier's performance, including, for example, the power amplifier's dynamic error vector magnitude (EVM).

Including both the current amplifier and the time-dependent signal generator can permit the power amplifier bias block to be included on-die with the power amplifier. For example, by amplifying the control current generated by the time-dependent signal generator, the magnitude of the components of the time-dependent signal generator can be reduced to a size suitable for on-chip integration. In certain implementations, the time-dependent signal generator can include a resistor-capacitor (RC) network, and the current amplifier can be used to amplify the control current so as to reduce a magnitude of the resistor and/or capacitor needed to generate a suitable correction current, thereby permitting the time-dependent signal generator to be integrated on-chip with the power amplifier.

FIG. 4 is a schematic block diagram of one example of a power amplifier system 70 including a power amplifier bias block 50 according to one embodiment. The illustrated power amplifier system 70 includes the power amplifier bias block

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50, the battery 21, and the power amplifier 32. The power amplifier 32 can be a single or multi-stage power amplifier, and in certain implementations can be similar to the power amplifier 32 described above with reference to FIG. 3B. The battery 21 can be any suitable battery, such as a lithium-ion battery, and be used to provide the battery or power high voltage V_{CC} to the power amplifier bias block 50 and to the power amplifier 32. The power amplifier bias block 50 and the power amplifier 32 can be integrated on a single die with one or more other components to form a packaged power amplifier module, which can be, for example, mounted to a RF circuit board associated with the wireless device 11 of FIG. 2.

The power amplifier bias block 50 includes a gain correction block 71 and a primary biasing circuit 74. The gain correction block 71 includes a time-dependent signal generator or control block 72 and a current amplifier 73. The power amplifier bias block 50 can receive an enable signal ENABLE, and use the enable signal ENABLE to generate a bias current I_{BIAS} using charge stored on the battery 21. The bias current I_{BIAS} can be provided to, for example, a base of a bipolar transistor of the power amplifier 32, as was described earlier.

The enable signal ENABLE can be used to control the power amplifier 32 so as to pulse the output of the power amplifier 32. For example, when the power amplifier 32 is configured to transmit a WLAN signal, the enable signal ENABLE can be selectively controlled so as to pulse the output of the power amplifier 32.

The power amplifier 32 can be configured to operate in a relatively noisy environment. For example, a die including the power amplifier 32 and the power amplifier bias block 50 can be provided in an electronic system that includes other electronic components including other power amplifiers, such as power amplifiers amplifying GSM and/or EDGE signals. These electronic components can cause noise on the power high voltage V_{CC} . Additionally, the power amplifier 32 can also be exposed to other non-ideal operation conditions. For example, the power amplifier 32 and the power amplifier bias block 50 can be exposed to a thermal gradient, and thus can be at different operating temperatures. Furthermore, the level of the power high voltage V_{CC} can vary depending on a charge of the device that the power amplifier 32 and the power amplifier bias block 50 are used in. The power amplifier bias block 50 can be used to compensate for a gain variation of the power amplifier 32 arising from these sources, as well as from other sources.

The power amplifier bias block 50 includes the time-dependent signal generator 72, which can be used to generate a control current $I_{CONTROL}$ when the enable signal ENABLE is transitioned from a disabled state to an enabled state. The control current $I_{CONTROL}$ can be provided to the current amplifier 73, which can amplify the control current $I_{CONTROL}$ to generate a correction current $I_{CORRECTION}$. The correction current $I_{CORRECTION}$ can be used by the primary biasing circuit 74 to correct for a variation in gain over time that can occur shortly after the power amplifier 32 is enabled. For example, shortly after the power amplifier 32 is enabled, absent compensation the current of the primary biasing circuit 74 can come up slow due to thermal effects, and the gain of the power amplifier 32 can be low. By using the time-dependent signal generator 72 and the current amplifier 73 to provide a transient current boost to the power amplifier 32 after being enabled, the power amplifier 32 can be configured to have a substantially constant gain over time.

By including the current amplifier 73 to amplify the control current $I_{CONTROL}$ generated by the time-dependent signal generator 72, the magnitude of the components of the time-

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dependent signal generator 72 can be reduced. For example, the current amplifier 73 can be used to amplify the control current $I_{CONTROL}$ so as to reduce a size of a component of the time-dependent signal generator 72 needed to generate a correction current with correct time constant, thereby permitting the time-dependent signal generator to be integrated on-chip with the power amplifier 32.

The primary bias circuit 74 can be configured to generate a relatively constant bias current output that can be adjusted by the correction current $I_{CORRECTION}$ to correct for a variation in gain of the power amplifier 32 that can occur shortly after the power amplifier 32 is enabled. In certain implementations, the primary bias circuit 74 can be a conventional bias circuit that is modified such that the output of the bias circuit is adjusted based on the amplitude of the correction current $I_{CORRECTION}$. Additional detail of the primary bias circuit 74 can be as described later below.

FIG. 5 is a circuit diagram of a power amplifier bias block 80 according to one embodiment. The power amplifier bias block 80 includes a resistor-capacitor (RC) network 82, a current mirror 83, and a primary bias circuit 84. The RC network 82 operates as a time-dependent signal generator and the current mirror 83 operates as a current amplifier. The power amplifier bias block 80 is configured to receive an enable signal ENABLE and a battery or power high voltage V_{CC} , and to generate a bias current I_{BIAS} .

The RC network 82 includes a first resistor 91, a second resistor 92, and a capacitor 90. The first resistor 91 includes a first end electrically connected to a first end of the capacitor 90 at an input of the RC network 82 configured to receive the enable signal ENABLE. The first resistor 91 further includes a second end electrically connected to a first end of the second resistor 92 at an output of the RC network 82 configured to provide the control current $I_{CONTROL}$ to the current mirror 83. The second resistor 92 further includes a second end electrically connected to a second end of the capacitor 90.

The RC network 82 can be used to shape the enable signal ENABLE so as to generate the control current $I_{CONTROL}$. For example, the capacitor 90 and the second resistor 92 can have an RC time-constant selected to achieve the desired shape of the control current $I_{CONTROL}$. The RC time-constant can be selected based on a system parameter of the electronic system that the power amplifier bias block 80 is used in, including, for example, a transition time of the enable signal ENABLE. In certain implementations, the time-constant of the second resistor 92 and the capacitor 90 is in the range of about 0.1 μ s to about 10 μ s, for example, about 1 μ s.

In certain implementations, the capacitor 90 has a capacitance ranging between about 10 pF to about 50 pF, for example, about 25 pF. The second resistor 92 can have any suitable resistance, including, for example, a resistance in the range of about 10 k Ω to about 100 k Ω , for example, about 50 k Ω . Although one implementation of the capacitor 90 and the second resistor 92 is illustrated, other configurations are possible. For example, the order of the second resistor 92 and the capacitor 90 in the series combination of the second resistor 92 and the capacitor 90 can be reversed. The first resistor 91 can have any suitable value, including, for example, a resistance in the range of about 1 k Ω to about 20 k Ω , for example, about 10 k Ω . In certain implementations, such as the implementation shown in FIG. 9, the first resistor 91 can be omitted.

To aid in reducing the area of the RC network 82, the current mirror 83 can be used to amplify the control current $I_{CONTROL}$ to generate the correction current $I_{CORRECTION}$. Thus, the amplifier 83 can be used to obtain a correction current $I_{CORRECTION}$ of a suitable magnitude, while reducing the size of the components of the RC network 82 relative to a

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scheme omitting a current amplifier. By amplifying the control current $I_{CONTROL}$ in this manner, the power amplifier bias block 80 can be integrated on-chip with a power amplifier without having to use a relatively large resistor, which may not provide enough current variation to provide suitable gain compensation.

The illustrated current mirror 83 includes a first NPN bipolar transistor 85, a second NPN bipolar transistor 86, a third NPN bipolar transistor 87, a fourth NPN bipolar transistor 88, and a resistor 89. The first NPN bipolar transistor 85 includes an emitter electrically connected to the first or power low voltage V_1 , which can be, for example, ground, and a base and a collector electrically connected to a base of the second NPN bipolar transistor 86 at an input of the current mirror 83 configured to receive the control current $I_{CONTROL}$. The second NPN bipolar transistor 86 further includes an emitter electrically connected to the power low voltage V_1 , and a collector electrically connected to a first end of the resistor 89, to a base of the fourth NPN bipolar transistor 88, and to a base and a collector of the third NPN bipolar transistor 87. The third and fourth NPN bipolar transistors 87, 88 each include an emitter electrically connected to the power low voltage V_1 . The resistor 89 includes a second end configured to receive the enable signal ENABLE. The fourth NPN bipolar transistor 88 further includes a collector configured to generate the correction current $I_{CORRECTION}$.

The resistor 89 can have any suitable resistance, including, for example, a resistance selected based on the voltage level of power amplifier enable signal ENABLE and/or system requirements. In certain implementations, the resistor 89 has a resistance ranging between about 10 k Ω to about 50 k Ω , for example, about 20 k Ω . By electrically connected the second end of the resistor 89 to the enable signal ENABLE, the power consumption of the power amplifier bias block 80 can be reduced when the enable signal ENABLE is low. However, in other implementations, the current mirror 83 can be configured in other ways.

The current mirror 83 can have any suitable gain. In one implementation, the current mirror 83 is configured to amplify the control current $I_{CONTROL}$ by a factor ranging between about 5 to about 50, for example, about 10. As used herein, the term current mirror can refer to current amplification circuits including a plurality of current mirrors combined (e.g., cascaded) to achieve a target gain.

The primary bias circuit 84 can be used to generate a bias current I_{BIAS} for a power amplifier, such as the power amplifier 32 of FIG. 4. The illustrated primary bias circuit 84 includes a first resistor 96, a second resistor 97, a first NPN bipolar transistor 93, a second NPN bipolar transistor 94 and a third NPN bipolar transistor 95. The first resistor 96 includes a first end electrically connected to a first end of the second resistor 97 at an input of the primary bias circuit 84 configured to receive the enable signal ENABLE. The first resistor 96 further includes a second end electrically connected to an emitter of the second NPN bipolar transistor 94 and to a base and a collector of the first NPN bipolar transistor 93 at an input of the primary bias circuit 84 configured to receive the correction current $I_{CORRECTION}$. The first NPN bipolar transistor 93 further includes an emitter electrically connected to the power low voltage V_1 . The second resistor 97 further includes a second end electrically connected to a base and a collector of the second NPN bipolar transistor 94 and to a base of the third NPN bipolar transistor 95. The third NPN bipolar transistor 95 further includes a collector electrically connected to the power high voltage V_{CC} and an emitter configured to generate the bias current I_{BIAS} .

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The first NPN bipolar transistor 93 can aid in level-shifting the voltage of the emitter of the second NPN bipolar transistor 94, which in turn can impact the emitter voltage of the third NPN bipolar transistor 95. Thus, inclusion of the first NPN bipolar transistor 93 can aid in establishing suitable DC operating voltage levels of the power amplifier bias block 80.

The first and second resistors 96, 97 can be tuned to control the steady-state amplitude of the bias current I_{BIAS} when the enable signal ENABLE is activated. For example, the current through the second NPN bipolar transistor 94 can be established using the first and second resistors 96, 97, and can be mirrored using the third NPN bipolar transistor 95 to generate the bias current I_{BIAS} .

After the enable signal ENABLE becomes activated, the RC network 82 can generate a control current $I_{CONTROL}$ that can be amplified by the current mirror 83 to generate the correction current $I_{CORRECTION}$. As illustrated in FIG. 5, the correction current $I_{CORRECTION}$ can be used to vary or change the current through the second NPN bipolar transistor 94. For example, when the correction current $I_{CORRECTION}$ decreases, the current through the second NPN bipolar transistor 94 can increase, which in turn can increase the bias current I_{BIAS} generated using the third NPN bipolar transistor 95. The second NPN bipolar transistor 94 can also aid in reversing the direction of the correction current $I_{CORRECTION}$ so that it is suitable to be provided to the base of the fifth NPN bipolar transistor 95. Although one variation of a primary bias circuit is illustrated, other implementations can be used.

FIG. 6 is a graph 100 of one example of collector current versus time. The graph 100 begins at a time zero that is associated with enabling a power amplifier. The graph 100 includes a first plot 101, a second plot 102, a third plot 103, a fourth plot 104 and a fifth plot 105, which correspond to different battery voltage values. In particular, the first, second, third, fourth, and fifth plots 101-105 correspond to battery voltage values of about 3.2 V, about 3.4 V, about 3.6 V, about 3.8 V, and about 4.0 V, respectively.

In certain implementations described herein, a time-dependent signal generator is used to generate a signal that can be used to adjust a power amplifier's bias current during a time period within about 8 μ s after the power amplifier is enabled. Thereafter the power amplifier's bias current can be substantially constant until the power amplifier's enable signal is deactivated. In certain implementations, the power amplifier's bias current can vary by more than about 50% during the initial time period that the correction current is used to adjust the power amplifier's bias current.

FIG. 7A is a graph 110 of one example of dynamic error vector magnitude (EVM) versus output power. The graph 110 is for one example of a power amplifier bias block that does not include a time-dependent signal generator and a current amplifier. The graph 110 includes plots of EVM versus output power for a variety of different battery voltage levels. For example, the graph 110 includes plots 111-119, which correspond to battery voltages ranging between about 3.2 V and about 4.2 V.

FIG. 7B is a graph 120 of another example of dynamic EVM versus output power. The graph 120 is for one implementation of a power amplifier bias block that includes a time-dependent signal generator and a current amplifier. The graph 120 includes plots of EVM versus output power for a variety of different battery voltage levels. For example, the graph 120 includes plots 121-129, which correspond to battery voltages between about 3.2 V and about 4.2 V. The graph 120 shows that the EVM of the power amplifier system can be improved by including the time-dependent signal generator and the current amplifier.

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FIG. 8 is a flow chart illustrating a method 150 for biasing a power amplifier in accordance with one embodiment. It will be understood that the method 150 can include greater or fewer operations and the operations may be performed in any order, as necessary.

The method 150 starts at a block 151, in which an enable signal of a power amplifier is shaped using a time-dependent signal generator to generate a control current. The power amplifier can be any suitable power amplifier, such as a power amplifier configured to amplify a WLAN signal. In certain implementations, the time-dependent signal generator includes a resistor-capacitor (RC) network configured to generate a transient control current that begins after an enable signal of the power amplifier is activated. In certain implementations, the transient control current reaches a steady-state value within about 8 μ s after the enable signal is activated. In certain implementations, the steady-state value of the transient control current can be about 0 mA.

In an ensuing block 152, the control current is amplified using the current amplifier to generate a correction current. In certain implementations, the current amplifier amplifies the correction current by a factor ranging between about 5 to about 50. The current amplifier can aid the time-dependent signal generator in shaping the enable signal by reducing the size of the circuit components of the time-dependent signal generator needed to achieve a desired time constant associated with gain compensation.

The method 150 continues at a block 153, in which a bias current for the power amplifier is generated using the primary biasing circuit. The primary biasing circuit is configured to use the correction current to generate a bias current for the power amplifier so as correct for a variation in gain of the power amplifier when the power amplifier is enabled. For example, the primary biasing circuit can be configured to adjust the amplitude of the bias current based on the correction current, such as by adding the correction current to a nominal bias current value.

FIG. 9 is a circuit diagram of a time-dependent signal generator 170 in accordance with one embodiment. The time-dependent signal generator 170 includes a resistor 92 and a capacitor 90, which can be similar to the resistor 92 and the capacitor 90 of the time-dependent signal generator 82 of FIG. 5. However, in contrast to the time-dependent signal generator 82 of FIG. 5, the time-dependent signal generator 170 of FIG. 9 does not include the resistor 91 of FIG. 4. In certain implementations, the time-constant of the resistor 92 and the capacitor 90 is in the range of about 0.1 μ s to about 10 μ s, for example, about 1 μ s.

FIG. 10A is a schematic diagram of one example of a packaged power amplifier module 300. FIG. 10B is a schematic diagram of a cross-section of the packaged power amplifier module 300 of FIG. 10A taken along the lines 10B-10B.

The packaged power amplifier module 300 includes an IC or die 301, surface mount components 303, wirebonds 308, a package substrate 320, and encapsulation 340. The package substrate 320 includes pads 306 formed from conductors disposed therein. Additionally, the die 301 includes pads 304, and the wirebonds 308 have been used to electrically connect the pads 304 of the die 301 to the pads 306 of the package substrate 301.

As illustrated in FIGS. 10A and 10B, the die 301 includes the power amplifier 32 and the power amplifier bias block 50 formed therein. The power amplifier bias block 50 includes the time dependent signal generator 72, the current amplifier 73, and the primary biasing circuit 74. In certain implementations, the time-dependent signal generator 72 can include a

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resistor-capacitor (RC) network, and the current amplifier 73 can be used to amplify a control current from the RC network to generate a correction current, which can be used by the primary biasing circuit 74 to generate a bias current for the power amplifier 32 that corrects for a gain variation of the power amplifier 32 associated with transitioning the power amplifier from a disabled state to an enabled state. Using the current amplifier 73 to amplify the control current from the time-dependent signal generator 72 can reduce a magnitude of the resistor and/or capacitor needed to generate a suitable correction current, thereby permitting the time-dependent signal generator 72 to be integrated on-chip with the power amplifier 32, as shown in FIG. 10A.

The packaging substrate 320 can be configured to receive a plurality of components such as the die 301 and the surface mount components 303, which can include, for example, surface mount capacitors and/or inductors.

As shown in FIG. 10B, the packaged power amplifier module 300 is shown to include a plurality of contact pads 332 disposed on the side of the packaged power amplifier module 300 opposite the side used to mount the die 301. Configuring the packaged power amplifier module 300 in this manner can aid in connecting the packaged power amplifier module 300 to a circuit board such as a phone board of a wireless device. The example contact pads 332 can be configured to provide RF signals, bias signals, power low voltage(s) and/or power high voltage(s) to the die 301 and/or the surface mount components 303. As shown in FIG. 10B, the electrical connections between the contact pads 332 and the die 301 can be facilitated by connections 333 through the package substrate 320. The connections 333 can represent electrical paths formed through the package substrate 320, such as connections associated with vias and conductors of a multilayer laminated package substrate.

In some embodiments, the packaged power amplifier module 300 can also include one or more packaging structures to, for example, provide protection and/or to facilitate handling of the packaged power amplifier module 300. Such a packaging structure can include overmold or encapsulation 340 formed over the packaging substrate 320 and the components and die(s) disposed thereon.

It will be understood that although the packaged power amplifier module 300 is described in the context of wirebond-based electrical connections, one or more features of the present disclosure can also be implemented in other packaging configurations, including, for example flip-chip configurations.

Applications

Some of the embodiments described above have provided examples in connection with mobile phones. However, the principles and advantages of the embodiments can be used for any other systems or apparatus that have needs for power amplifier systems.

Such power amplifier systems can be implemented in various electronic devices. Examples of the electronic devices can include, but are not limited to, consumer electronic products, parts of the consumer electronic products, electronic test equipment, etc. Examples of the electronic devices can also include, but are not limited to, memory chips, memory modules, circuits of optical networks or other communication networks, and disk driver circuits. The consumer electronic products can include, but are not limited to, a mobile phone, a telephone, a television, a computer monitor, a computer, a hand-held computer, a personal digital assistant (PDA), a microwave, a refrigerator, an automobile, a stereo system, a cassette recorder or player, a DVD player, a CD player, a VCR, an MP3 player, a radio, a camcorder, a camera, a digital

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camera, a portable memory chip, a washer, a dryer, a washer/dryer, a copier, a facsimile machine, a scanner, a multi functional peripheral device, a wrist watch, a clock, etc. Further, the electronic devices can include unfinished products.

Conclusion

Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not limited to." The word "coupled", as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Likewise, the word "connected", as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words "herein," "above," "below," and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word "or" in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

Moreover, conditional language used herein, such as, among others, "can," "could," "might," "can," "e.g.," "for example," "such as" and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments or that one or more embodiments necessarily include logic for deciding, with or without author input or prompting, whether these features, elements and/or states are included or are to be performed in any particular embodiment.

The above detailed description of embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise form disclosed above. While specific embodiments of, and examples for, the invention are described above for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. For example, while processes or blocks are presented in a given order, alternative embodiments may perform routines having steps, or employ systems having blocks, in a different order, and some processes or blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these processes or blocks may be implemented in a variety of different ways. Also, while processes or blocks are at times shown as being performed in series, these processes or blocks may instead be performed in parallel, or may be performed at different times.

The teachings of the invention provided herein can be applied to other systems, not necessarily the system described above. The elements and acts of the various embodiments described above can be combined to provide further embodiments.

While certain embodiments of the inventions have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; further-

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more, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

What is claimed is:

1. A power amplifier system comprising:

a power amplifier configured to amplify a radio frequency (RF) signal; and

a bias block for biasing the power amplifier, the bias block including a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current, a current amplifier configured to amplify the control current to generate a correction current, and a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current, the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled, the current amplifier including a current mirror.

2. The power amplifier system of claim 1 wherein the time-dependent signal generator includes a resistor-capacitor (RC) network.

3. The power amplifier system of claim 2 wherein the RC network includes a first resistor and a first capacitor electrically connected in series between the current amplifier and an input of the bias circuit configured to receive the enable signal.

4. The power amplifier system of claim 3 wherein the first capacitor has a capacitance ranging between about 10 pF and about 100 pF.

5. The power amplifier system of claim 4 wherein the first resistor has a resistance ranging between about 10 kΩ and about 100 kΩ.

6. The power amplifier system of claim 1 wherein the current mirror includes a first bipolar transistor and a second bipolar transistor, the first bipolar transistor including an emitter electrically connected to an emitter of the second bipolar transistor and to a power low voltage, and a collector electrically connected to a base of the first bipolar transistor and to a base of the second bipolar transistor, the collector of the first bipolar transistor configured to receive at least a portion of the control current.

7. The power amplifier system of claim 6 wherein the current mirror further includes a resistor, a third bipolar transistor and a fourth bipolar transistor, the third bipolar transistor including an emitter electrically connected to an emitter of the fourth bipolar transistor and to the power low voltage, and a collector electrically connected to a first end of the resistor, to the collector of the second bipolar transistor, to a base of the third bipolar transistor, and to a base of the fourth bipolar transistor, the collector of the fourth bipolar transistor configured to generate the compensation current.

8. The power amplifier system of claim 7 wherein the resistor further includes a second end configured to receive the enable signal.

9. The power amplifier system of claim 1 further comprising a transceiver for providing the RF signal to the power amplifier.

10. The power amplifier system of claim 1 wherein the power amplifier includes a bipolar transistor having an emitter, a base and a collector, the base configured to receive the RF signal and the bias current.

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11. The power amplifier system of claim 10 wherein the emitter is electrically connected to a power low voltage and the collector is configured to generate an amplified version of the RF signal.

12. A power amplifier system comprising:

a power amplifier configured to amplify a radio frequency (RF) signal; and

a bias block for biasing the power amplifier, the bias block including a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current, a current amplifier configured to amplify the control current to generate a correction current, and a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current, the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled, the time-dependent signal generator including a resistor-capacitor (RC) network, the RC network including a first resistor and a first capacitor electrically connected in series between the current amplifier and an input of the bias circuit configured to receive the enable signal, the RC network further including a second resistor having a first end electrically connected to the input of the current mirror and a second end electrically connected to the input of the bias circuit configured to receive the enable signal.

13. The power amplifier system of claim 12 wherein the second resistor has a resistance ranging between about 10 Ω and about 100 k Ω .

14. A power amplifier system comprising:

a power amplifier configured to amplify a radio frequency (RF) signal; and

a bias block for biasing the power amplifier, the bias block including a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current, a current amplifier configured to amplify the control current to generate a correction current, and a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current, the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled, the primary bias circuit including a first resistor, a second resistor, a first bipolar transistor, and a second bipolar transistor, the first resistor including a first end electrically connected to the emitter of the first bipolar transistor at a node configured to receive the correction current, and a second end electrically connected to a first end of the second resistor at a node of the bias circuit configured to receive the enable signal, the second resistor including a second end electrically connected to a collector of the first bipolar transistor, a base of the first bipolar transistor, and to a base of the second bipolar transistor.

15. The power amplifier system of claim 14 wherein the second bipolar transistor includes a collector electrically connected to a battery voltage and an emitter configured to generate the bias current.

16. The power amplifier system of claim 15 wherein the primary bias circuit further includes a third bipolar transistor having an emitter electrically connected to the power low voltage and a base and a collector electrically connected to the emitter of the first bipolar transistor.

17. A method of biasing a power amplifier, the method comprising:

shaping an enable signal using a time-dependent signal generator to generate a control current;

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amplifying the control current using a current mirror of a current amplifier to generate a correction current; and generating a bias current for a power amplifier using a primary biasing circuit, the primary biasing circuit configured to use the correction current to correct for a variation in gain of the power amplifier when the power amplifier is enabled.

18. The method of claim 17 wherein shaping the enable signal includes using a resistor-capacitor (RC) network of the time-dependent signal generator.

19. The method of claim 18 wherein the RC network includes a first resistor and a first capacitor electrically connected in series, the RC network configured to receive the enable signal and to generate the control current.

20. The method of claim 17 wherein generating the bias current includes shaping the bias current so as to compensate for a gain variation of a heterojunction bipolar transistor (HBT).

21. A bias circuit for biasing a power amplifier, the bias circuit comprising:

a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current;

a current amplifier configured to amplify the control current to generate a correction current, the current amplifier including a current mirror; and

a primary biasing block configured to generate a bias current for the power amplifier based at least partly on the correction current, the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled.

22. The bias circuit of claim 21 wherein the time-dependent signal generator includes a resistor-capacitor (RC) network.

23. The bias circuit of claim 22 wherein the RC network includes a first resistor and a first capacitor electrically connected in series between the current amplifier and an input of the bias circuit configured to receive the enable signal.

24. A bias circuit for biasing a power amplifier, the bias circuit comprising:

a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current;

a current amplifier configured to amplify the control current to generate a correction current; and

a primary biasing block configured to generate a bias current for the power amplifier based at least partly on the correction current, the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled, the primary bias block including a first resistor, a second resistor, a first bipolar transistor, and a second bipolar transistor, the first resistor including a first end electrically connected to the emitter of the first bipolar transistor at a node configured to receive the correction current, and a second end electrically connected to a first end of the second resistor at a node of the bias circuit configured to receive the enable signal, the second resistor including a second end electrically connected to a collector of the first bipolar transistor, a base of the first bipolar transistor, and to a base of the second bipolar transistor.

25. The bias circuit of claim 24 wherein the second bipolar transistor includes a collector electrically connected to a battery voltage and an emitter configured to generate the bias current.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 8,717,101 B2
APPLICATION NO. : 13/468749
DATED : May 6, 2014
INVENTOR(S) : Li et al.

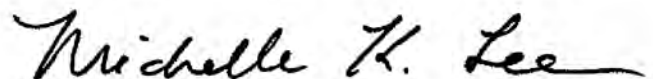
Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims

In column 17 at line 29, In Claim 13, change “10 Ω ” to --10 k Ω --.

Signed and Sealed this
Twenty-first Day of October, 2014



Michelle K. Lee
Deputy Director of the United States Patent and Trademark Office

EXHIBIT 7

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United States Patent and Trademark Office

March 21, 2024

THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM
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PATENT NUMBER: 9,917,563

ISSUE DATE: *March 13, 2018*

By Authority of the
Under Secretary of Commerce for Intellectual Property
and Director of the United States Patent and Trademark Office

John Burson
Certifying Officer





US009917563B2

(12) **United States Patent**
Li et al.

(10) **Patent No.:** **US 9,917,563 B2**
(45) **Date of Patent:** ***Mar. 13, 2018**

(54) **APPARATUS AND METHODS FOR BIASING OF POWER AMPLIFIERS**

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Woburn, MA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **15/377,842**

(22) Filed: **Dec. 13, 2016**

(65) **Prior Publication Data**

US 2017/0093355 A1 Mar. 30, 2017

Related U.S. Application Data

(63) Continuation of application No. 14/825,053, filed on Aug. 12, 2015, now Pat. No. 9,667,203, which is a (Continued)

(51) **Int. Cl.**
H03G 3/30 (2006.01)
H03F 3/213 (2006.01)

(Continued)

(52) **U.S. Cl.**
CPC **H03G 3/3042** (2013.01); **H03F 3/195** (2013.01); **H03F 3/213** (2013.01); **H04B 1/3827** (2013.01);

(Continued)

(58) **Field of Classification Search**

USPC 330/285, 296, 288, 289
See application file for complete search history.

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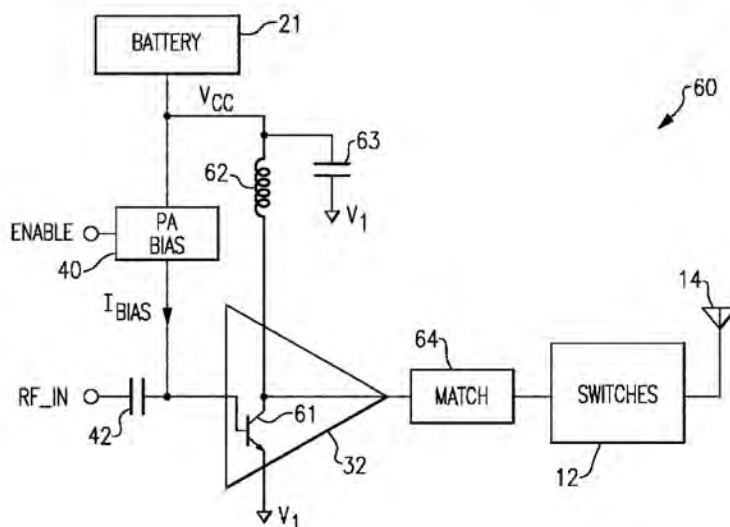
Primary Examiner — Hieu Nguyen

(74) *Attorney, Agent, or Firm* — Knobbe Martens Olson & Bear LLP

(57) **ABSTRACT**

Apparatus and methods for biasing of power amplifiers are disclosed. In one embodiment, a mobile device includes a transceiver that generates a radio frequency signal and a power amplifier enable signal, a power amplifier that provides amplification to the radio frequency signal and that is biased by a bias signal, and a bias circuit that receives the power amplifier enable signal and generates the bias signal. The bias circuit includes a gain correction circuit that generates a correction current in response to activation of the power amplifier enable signal, and a primary biasing circuit that generates the bias signal based on the correction current and the power amplifier enable signal.

20 Claims, 7 Drawing Sheets



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Related U.S. Application Data

continuation of application No. 14/242,150, filed on Apr. 1, 2014, now Pat. No. 9,136,803, which is a continuation of application No. 13/468,749, filed on May 10, 2012, now Pat. No. 8,717,101.

(60) Provisional application No. 61/486,186, filed on May 13, 2011.

(51) Int. Cl.

H03F 3/195 (2006.01)

H04B 1/3827 (2015.01)

(52) U.S. Cl.

CPC *H03F 2200/18* (2013.01); *H03F 2200/336*
(2013.01); *H03F 2200/387* (2013.01); *H03F*
2200/451 (2013.01)

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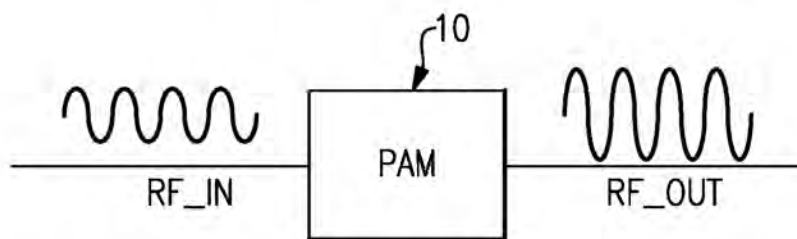
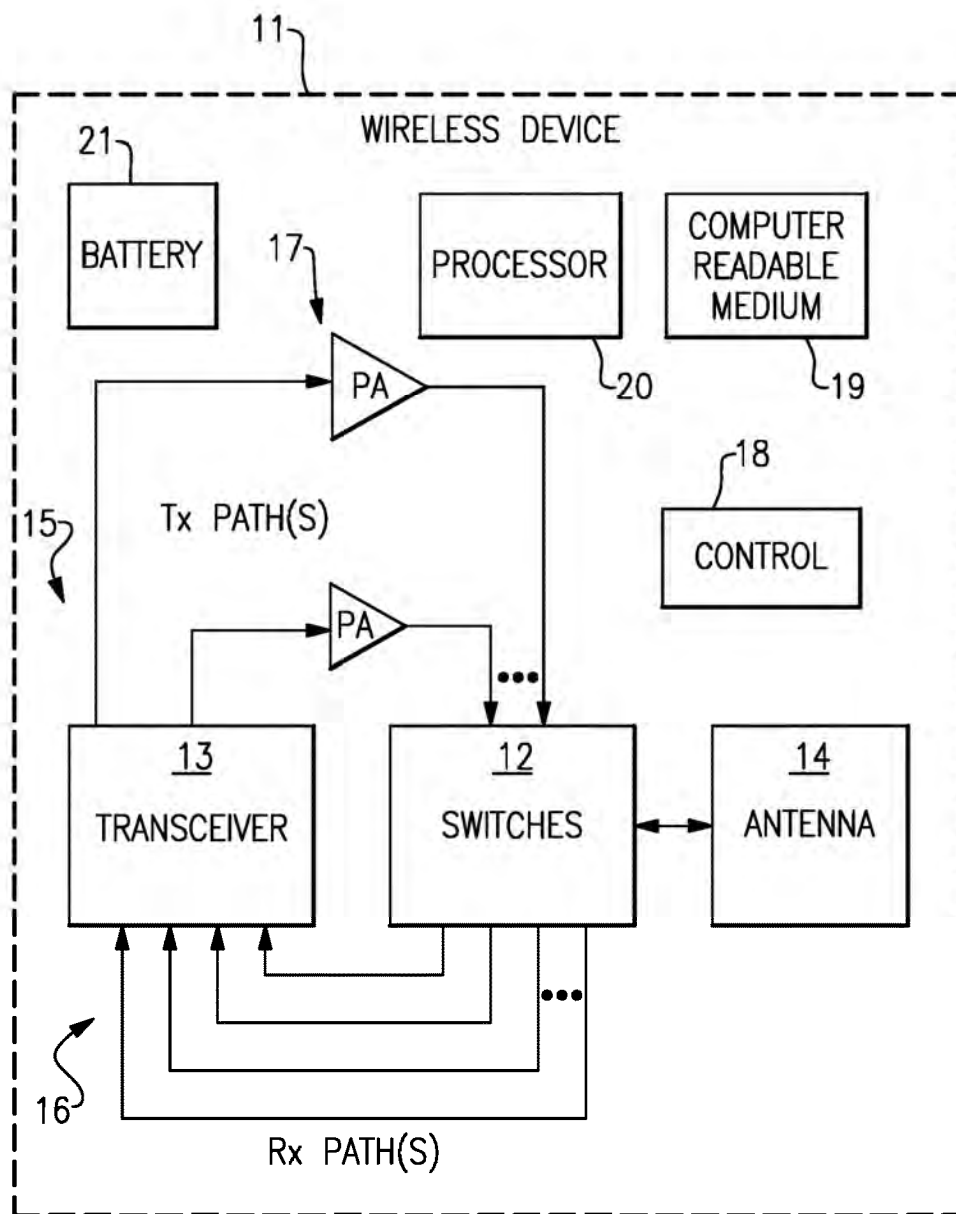
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**FIG. 1****FIG. 2**

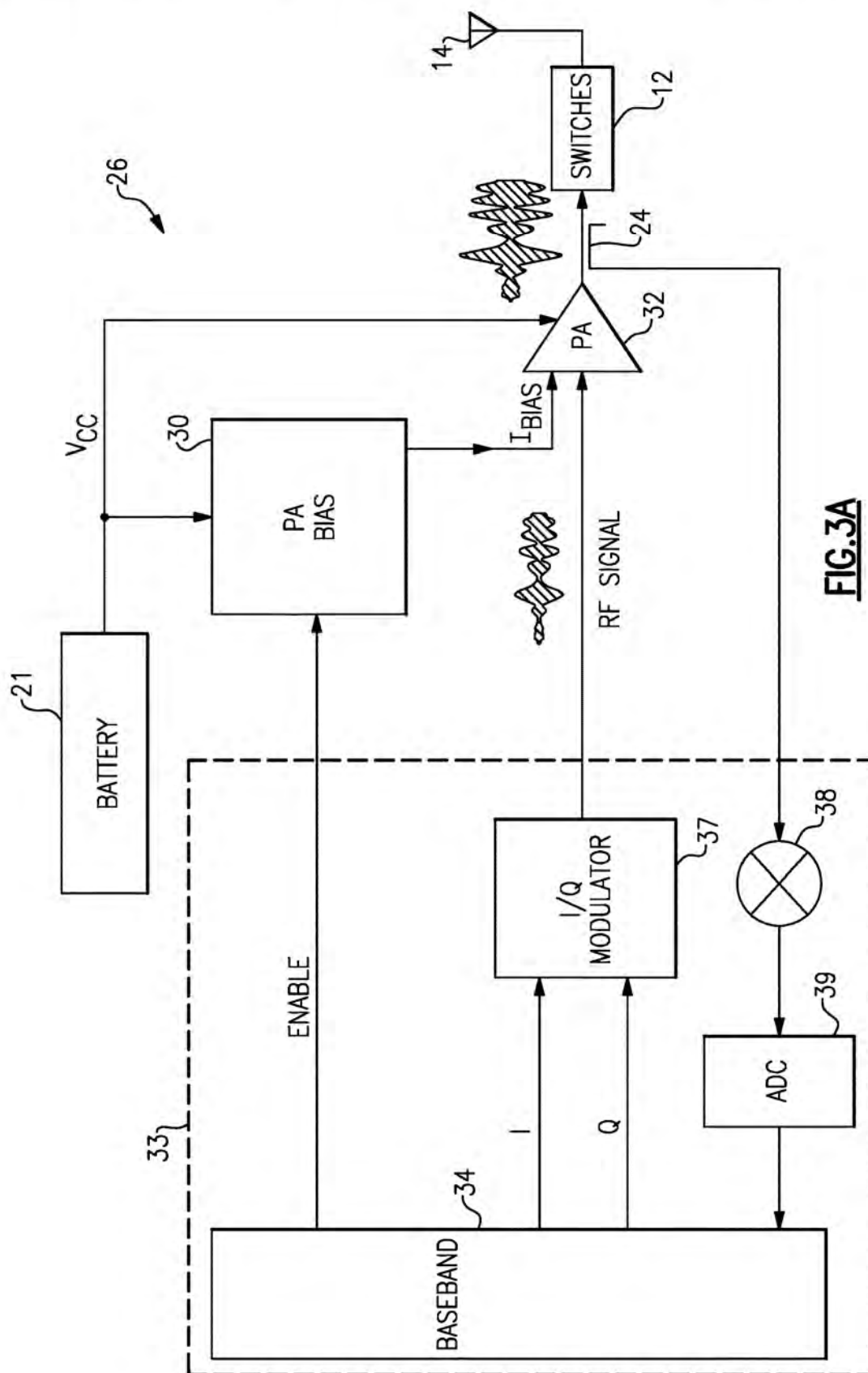
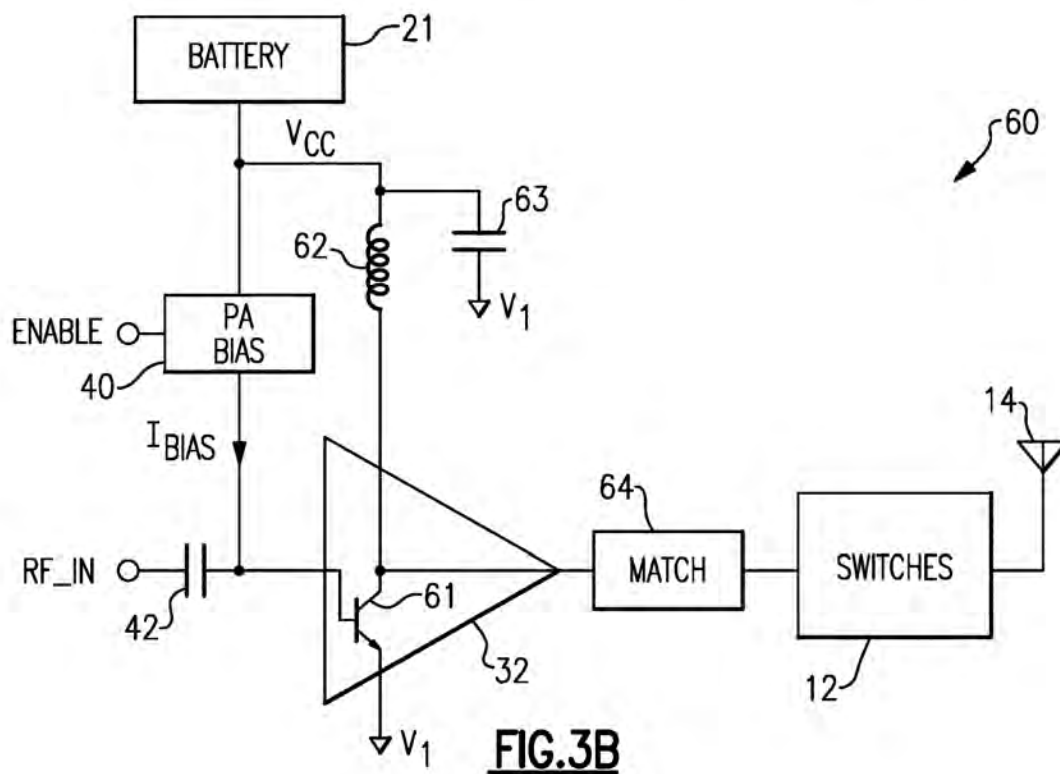
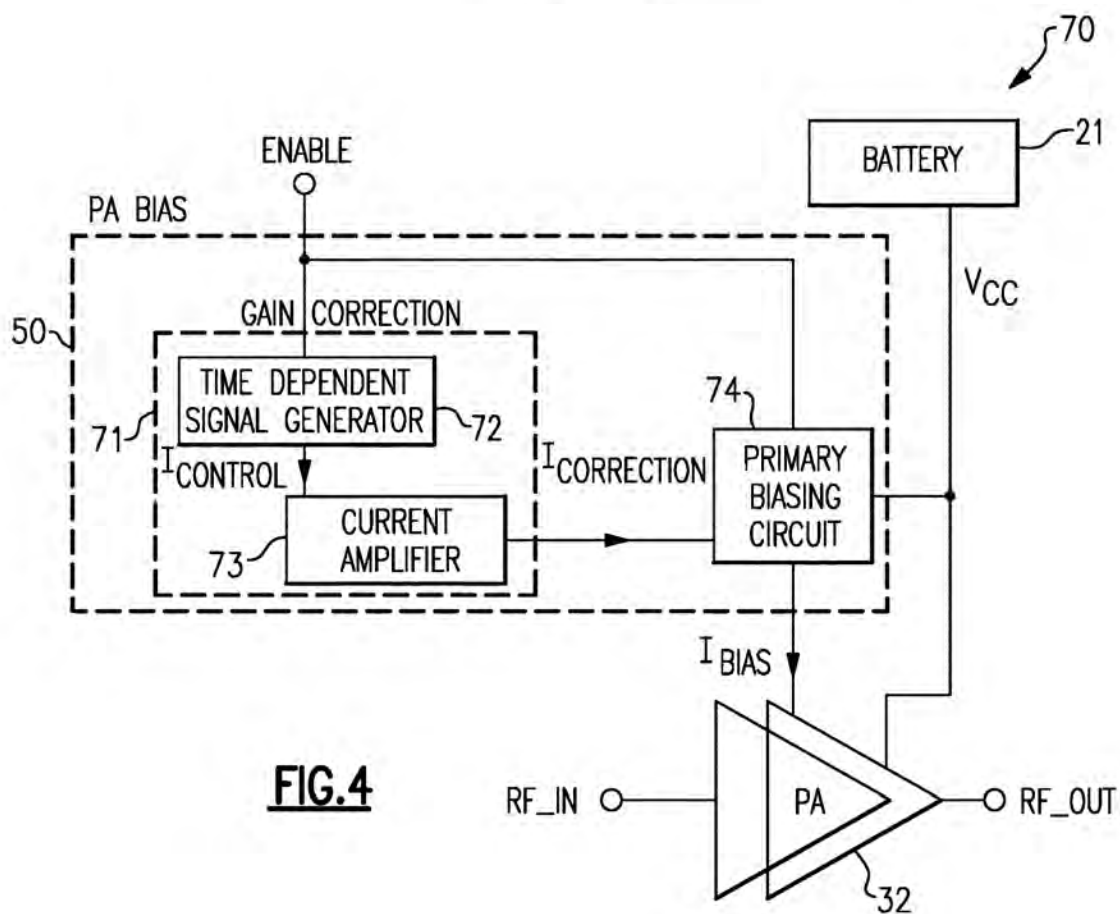


FIG. 3A

**FIG. 3B****FIG. 4**

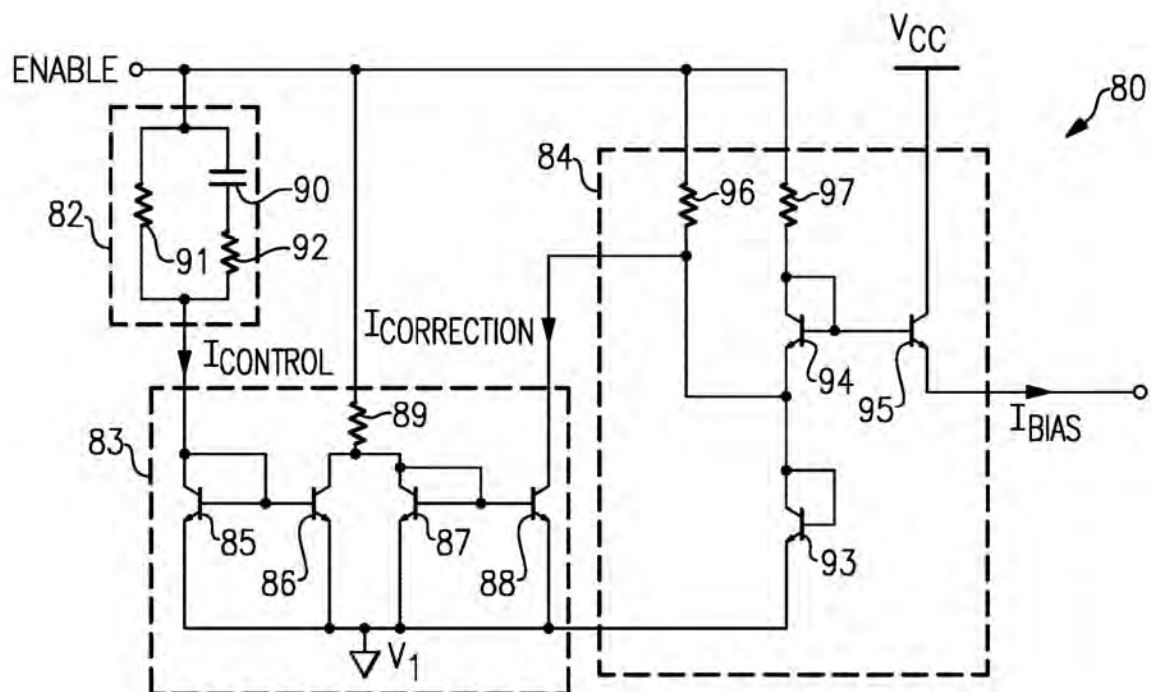


FIG.5

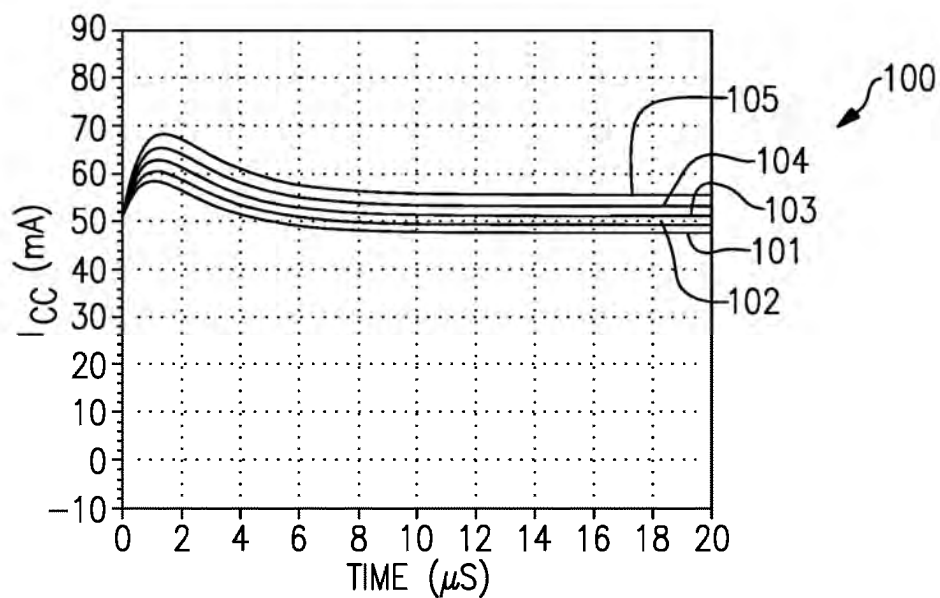
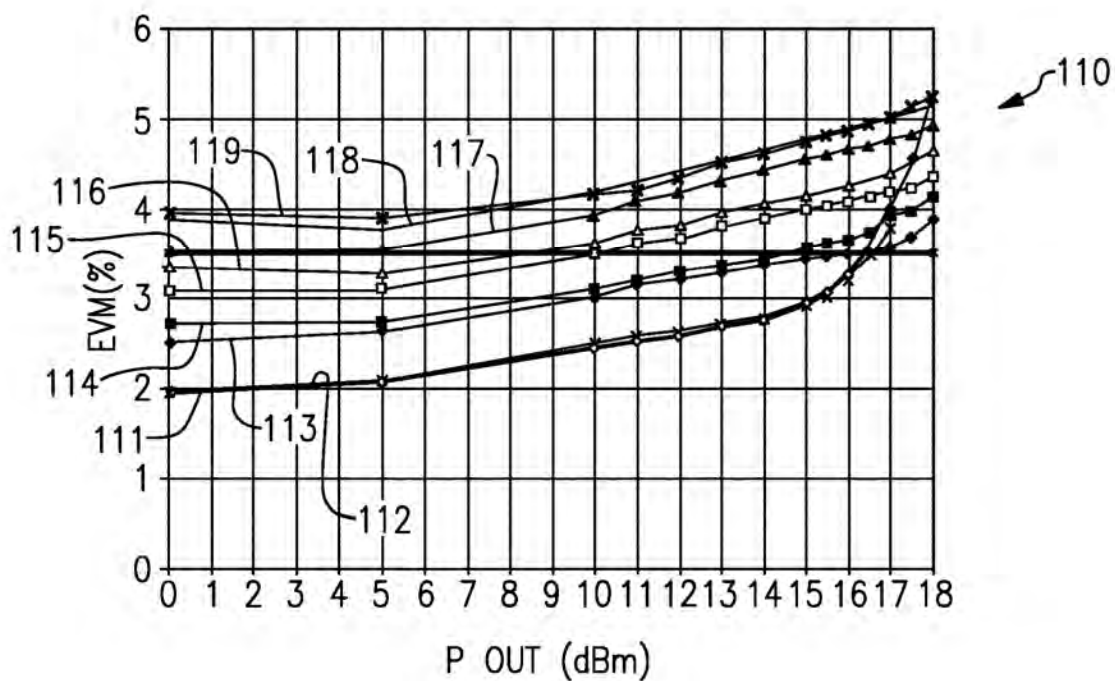
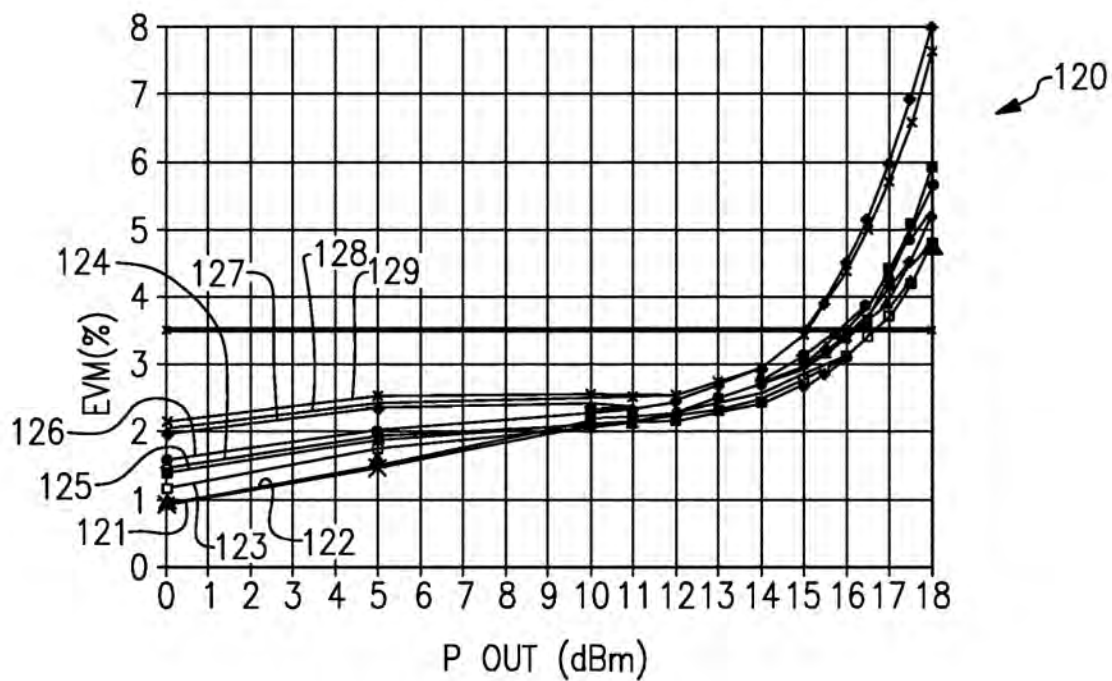
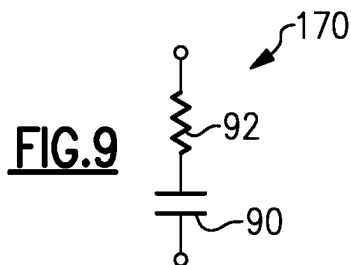
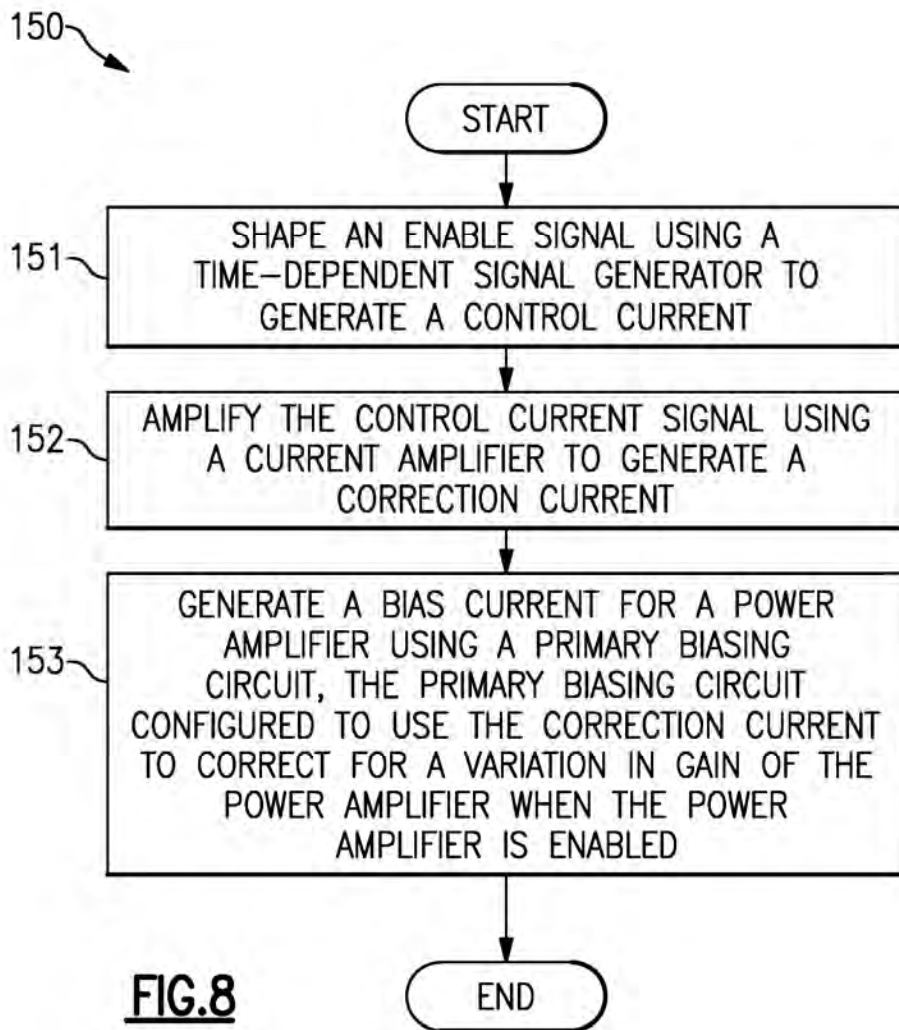


FIG.6

**FIG. 7A****FIG. 7B**



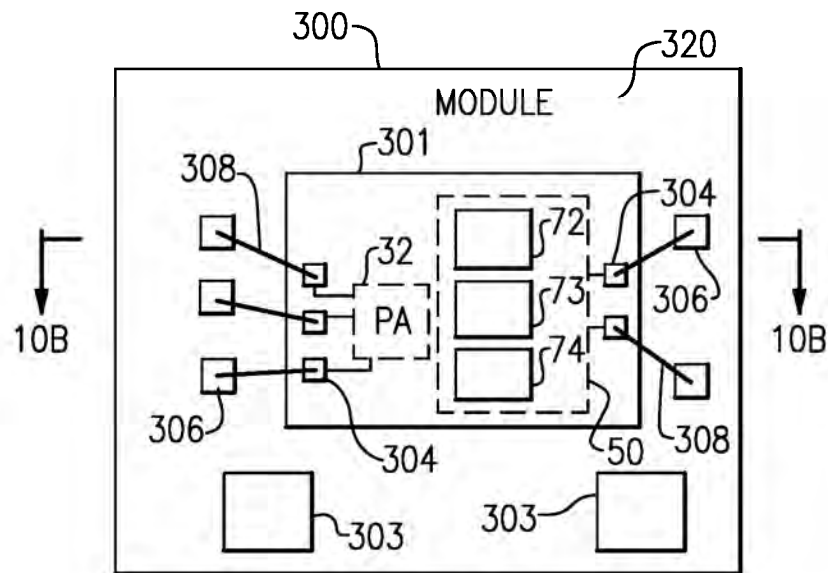


FIG. 10A

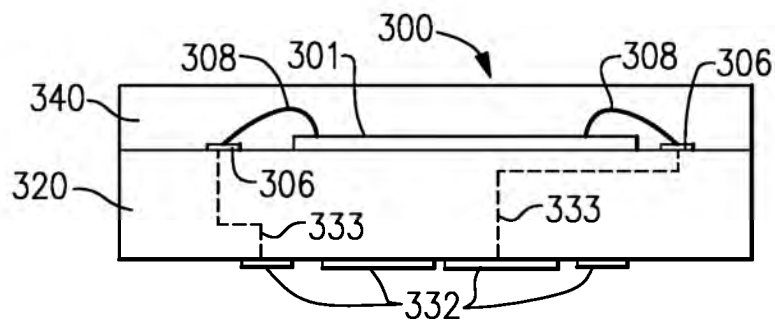


FIG. 10B

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APPARATUS AND METHODS FOR BIASING
OF POWER AMPLIFIERSCROSS-REFERENCE TO RELATED
APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 14/825,053, filed Aug. 12, 2015 titled "APPARATUS AND METHODS FOR POWER AMPLIFIER BIASING," which is a continuation of U.S. patent application Ser. No. 14/242,150, filed Apr. 1, 2014, titled "APPARATUS AND METHODS FOR BIASING A POWER AMPLIFIER," which is a continuation of U.S. patent application Ser. No. 13/468,749, filed May 10, 2012, titled "APPARATUS AND METHODS FOR BIASING POWER AMPLIFIERS," which claims the benefit of priority under 35 U.S.C. §119(e) of U.S. Provisional Patent Application No. 61/486,186, filed May 13, 2011 titled "APPARATUS AND METHODS FOR BIASING POWER AMPLIFIERS," each of which are herein incorporated by reference in their entireties.

BACKGROUND

Field

Embodiments of the invention relate to electronic systems, and in particular, to radio frequency (RF) electronics.

Description of the Related Technology

RF power amplifiers can be used to boost the power of a RF signal having a relatively low power. Thereafter, the boosted RF signal can be used for a variety of purposes, included driving the antenna of a transmitter.

Power amplifiers can be included in mobile phones to amplify a RF signal for transmission. For example, in mobile phones that communicate using a wireless local area network (WLAN) protocol and/or any other suitable communication standard, a power amplifier can be used to amplify the RF signal. It can be important manage the amplification of a RF signal, as amplifying the RF signal to an incorrect power level can cause a wireless device to transmit out of band.

There is a need for improved power amplifier systems. Furthermore, there is a need for improving power amplifier biasing.

SUMMARY

In certain embodiments, the present disclosure relates to a power amplifier system including a power amplifier configured to amplify a radio frequency (RF) signal and a bias block for biasing the power amplifier. The bias block includes a time dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current, a current amplifier configured to amplify the control current to generate a correction current, and a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current. The bias current is configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled.

In several embodiments, the time dependent signal generator includes a resistor-capacitor (RC) network. In accordance with a number of embodiments, the RC network includes a first resistor and a first capacitor electrically connected in series between the current amplifier and an input of the bias circuit configured to receive the enable signal. In several embodiments, the RC network further

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includes a second resistor having a first end electrically connected to the input of the current mirror and a second end electrically connected to the input of the bias circuit configured to receive the enable signal.

According to certain embodiments, the second resistor has a resistance ranging between about 10 k Ω and about 100 k Ω , the first capacitor has a capacitance ranging between about 10 pF and about 100 pF, and the first resistor has a resistance ranging between about 10 k Ω and about 100 k Ω .

In a number of embodiments, the current amplifier includes a current mirror. In several embodiments, the current mirror includes a first bipolar transistor and a second bipolar transistor, the first bipolar transistor including an emitter electrically connected to an emitter of the second bipolar transistor and to a power low voltage, and a collector electrically connected to a base of the first bipolar transistor and to a base of the second bipolar transistor, the collector of the first bipolar transistor configured to receive at least a portion of the control current. In certain embodiments, the current mirror further includes a resistor, a third bipolar transistor and a fourth bipolar transistor, the third bipolar transistor including an emitter electrically connected to an emitter of the fourth bipolar transistor and to the power low voltage, and a collector electrically connected to a first end of the resistor, to the collector of the second bipolar transistor, to a base of the third bipolar transistor, and to a base of the fourth bipolar transistor, the collector of the fourth bipolar transistor configured to generate the compensation current. In several embodiments, the resistor further includes a second end configured to receive the enable signal.

According to some embodiments, the power amplifier system further includes a transceiver for providing the RF signal to the power amplifier.

In a number of embodiments, the power amplifier includes a bipolar transistor having an emitter, a base and a collector, the base configured to receive the RF signal and the bias current. In certain embodiments, the emitter is electrically connected to a power low voltage and the collector is configured to generate an amplified version of the RF signal.

In several embodiments, the primary bias circuit includes a first resistor, a second resistor, a first bipolar transistor, and a second bipolar transistor, the first resistor including a first end electrically connected to the emitter of the first bipolar transistor at a node configured to receive the correction current, and a second end electrically connected to a first end of the second resistor at a node of the bias circuit configured to receive the enable signal, the second resistor including a second end electrically connected to a collector of the first bipolar transistor, a base of the first bipolar transistor, and to a base of the second bipolar transistor. According to certain embodiments, the second bipolar transistor includes a collector electrically connected to a battery voltage and an emitter configured to generate the bias current. In a number of embodiments, the primary bias circuit further includes a third bipolar transistor having an emitter electrically connected to the power low voltage and a base and a collector electrically connected to the emitter of the first bipolar transistor.

In certain embodiments, the present disclosure relates to a method of biasing a power amplifier. The method includes shaping an enable signal using a time-dependent signal generator to generate a control current, amplifying the control current using a current amplifier to generate a correction current, and generating a bias current for a power amplifier using a primary biasing circuit, the primary biasing

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circuit configured to use the correction current to correct for a variation in gain of the power amplifier when the power amplifier is enabled.

In a number of embodiments, shaping the enable signal includes using a resistor capacitor (RC) network of the time dependent signal generator. In some embodiments, the RC network includes a first resistor and a first capacitor electrically connected in series, the RC network configured to receive the enable signal and to generate the control current.

In several embodiments, amplifying the control current further includes amplifying the control current using a current mirror of the current amplifier.

In accordance with a number of embodiments, generating the bias current includes shaping the bias current so as to compensate for a gain variation of a heterojunction bipolar transistor (HBT).

In certain embodiments, the present disclosure relates to a bias circuit for biasing a power amplifier. The bias circuit includes a time dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current, a current amplifier configured to amplify the control current to generate a correction current, and a primary biasing block configured to generate a bias current for the power amplifier based at least partly on the correction current. The bias current is configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled.

In several embodiments, the time dependent signal generator includes a resistor-capacitor (RC) network. In a number of embodiments, the RC network includes a first resistor and a first capacitor electrically connected in series between the current amplifier and an input of the bias circuit configured to receive the enable signal.

In accordance with certain embodiments, the current amplifier includes a current mirror.

In several embodiments, the primary bias block includes a first resistor, a second resistor, a first bipolar transistor, and a second bipolar transistor, the first resistor including a first end electrically connected to the emitter of the first bipolar transistor at a node configured to receive the correction current, and a second end electrically connected to a first end of the second resistor at a node of the bias circuit configured to receive the enable signal, the second resistor including a second end electrically connected to a collector of the first bipolar transistor, a base of the first bipolar transistor, and to a base of the second bipolar transistor. In a number of embodiments, the second bipolar transistor includes a collector electrically connected to a battery voltage and an emitter configured to generate the bias current.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a power amplifier module for amplifying a radio frequency (RF) signal.

FIG. 2 is a schematic block diagram of an example wireless device that can include one or more of the power amplifier modules of FIG. 1.

FIG. 3A is a schematic block diagram of one example of a power amplifier system.

FIG. 3B is a schematic block diagram of another example of a power amplifier system.

FIG. 4 is a schematic block diagram of one example of a power amplifier system including a power amplifier bias block according to one embodiment.

FIG. 5 is a circuit diagram of a power amplifier bias block according to one embodiment.

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FIG. 6 is a graph of one example of collector current versus time.

FIG. 7A is a graph of one example of dynamic error vector magnitude (EVM) versus output power.

FIG. 7B is a graph of another example of dynamic EVM versus output power.

FIG. 8 is a flow chart illustrating a method for biasing a power amplifier in accordance with one embodiment.

FIG. 9 is a circuit diagram of a time-dependent signal generator in accordance with one embodiment.

FIG. 10A is a schematic diagram of one example of a packaged power amplifier module.

FIG. 10B is a schematic diagram of a cross-section of the packaged power amplifier module of FIG. 10A taken along the lines 10B-10B.

DETAILED DESCRIPTION OF EMBODIMENTS

The headings provided herein, if any, are for convenience only and do not necessarily affect the scope or meaning of the claimed invention.

Apparatus and methods for biasing power amplifiers are disclosed herein. In certain implementations, a power amplifier and a power amplifier bias block are provided. The power amplifier can be used to amplify a radio frequency (RF) signal for transmission, and the power amplifier bias block can be used to bias the power amplifier. The power amplifier bias block can receive an enable signal that can be used to enable or disable the power amplifier so as to pulse the power amplifier's output.

In certain implementations, the power amplifier bias block includes a primary biasing circuit and a gain correction block including a time-dependent signal generator and a current amplifier. The time-dependent signal generator or control block can be used to shape the enable signal so as to generate a control current, which can be amplified by the current amplifier to generate a correction current. The power amplifier bias block can generate a bias current for the power amplifier using the primary biasing circuit and the correction current. The correction current can be used to adjust the magnitude of the bias current so as to compensate for a variation in gain of the power amplifier over time when the power amplifier is transitioned from a disabled state to an enabled state. For example, shortly after a power amplifier is enabled, absent compensation the current of a primary biasing circuit can come up slow due to thermal effects, and the power amplifier's gain can be low. By including the time-dependent signal generator and the current amplifier, a current boost can be provided to the power amplifier so as to provide the power amplifier with a substantially flat gain response versus time. Correcting for gain variation in the power amplifier can improve the power amplifier's performance, including, for example, the power amplifier's dynamic error vector magnitude (EVM).

Overview of Power Amplifier Systems

FIG. 1 is a schematic diagram of a power amplifier module 10 for amplifying a radio frequency (RF) signal. The illustrated power amplifier module (PAM) 10 can be configured to amplify an RF signal RF_IN to generate an amplified RF signal RF_OUT. As described herein, the power amplifier module 10 can include one or more power amplifiers, including, for example, multi-stage power amplifiers.

FIG. 2 is a schematic block diagram of an example wireless or mobile device 11 that can include one or more of the power amplifier modules of FIG. 1. The wireless device

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11 can include power amplifier bias circuits implementing one or more features of the present disclosure.

The example wireless device 11 depicted in FIG. 2 can represent a multi-band and/or multi-mode device such as a multi-band/multi-mode mobile phone. In certain embodiments, the wireless device 11 can include switches 12, a transceiver 13, an antenna 14, power amplifiers 17, a control component 18, a computer readable medium 19, a processor 20, and a battery 21.

The transceiver 13 can generate RF signals for transmission via the antenna 14. Furthermore, the transceiver 13 can receive incoming RF signals from the antenna 14.

It will be understood that various functionalities associated with the transmission and receiving of RF signals can be achieved by one or more components that are collectively represented in FIG. 2 as the transceiver 13. For example, a single component can be configured to provide both transmitting and receiving functionalities. In another example, transmitting and receiving functionalities can be provided by separate components.

Similarly, it will be understood that various antenna functionalities associated with the transmission and receiving of RF signals can be achieved by one or more components that are collectively represented in FIG. 2 as the antenna 14. For example, a single antenna can be configured to provide both transmitting and receiving functionalities. In another example, transmitting and receiving functionalities can be provided by separate antennas. In yet another example, different bands associated with the wireless device 11 can be provided with different antennas.

In FIG. 2, one or more output signals from the transceiver 13 are depicted as being provided to the antenna 14 via one or more transmission paths 15. In the example shown, different transmission paths 15 can represent output paths associated with different bands and/or different power outputs. For instance, the two example power amplifiers 17 shown can represent amplifications associated with different power output configurations (e.g., low power output and high power output), and/or amplifications associated with different bands. Although FIG. 2 illustrates a configuration using two transmission paths 15, the wireless device 11 can be adapted to include more or fewer transmission paths 15.

The power amplifiers 17 can be used to amplify a wide variety of RF signals. For example, one or more of the power amplifiers 17 can receive an enable signal that can be used to pulse the output of the power amplifier to aid in transmitting a wireless local area network (WLAN) signal or any other suitable pulsed signal. Each of the power amplifiers 17 need not amplify the same type of signal. For example, one power amplifier can amplify a WLAN signal, while another power amplifier can amplify, for example, a Global System for Mobile (GSM) signal, a code division multiple access (CDMA) signal, a W-CDMA signal, a Long Term Evolution (LTE) signal, or an EDGE signal.

One or more features of the present disclosure can be implemented in the foregoing example modes and/or bands, and in other communication standards.

In FIG. 2, one or more detected signals from the antenna 14 are depicted as being provided to the transceiver 13 via one or more receiving paths 16. In the example shown, different receiving paths 16 can represent paths associated with different bands. Although FIG. 2 illustrates a configuration using four receiving paths 16, the wireless device 11 can be adapted to include more or fewer receiving paths 16.

To facilitate switching between receive and transmit paths, the switches 12 can be configured to electrically connect the antenna 14 to a selected transmit or receive path.

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Thus, the switches 12 can provide a number of switching functionalities associated with an operation of the wireless device 11. In certain embodiments, the switches 12 can include a number of switches configured to provide functionalities associated with, for example, switching between different bands, switching between different power modes, switching between transmission and receiving modes, or some combination thereof. The switches 12 can also be configured to provide additional functionality, including filtering and/or duplexing of signals.

FIG. 2 shows that in certain embodiments, a control component 18 can be provided for controlling various control functionalities associated with operations of the switches 12, the power amplifiers 17, and/or other operating component(s). Non-limiting examples of the control component 18 are described herein in greater detail.

In certain embodiments, a processor 20 can be configured to facilitate implementation of various processes described herein. For the purpose of description, embodiments of the present disclosure may also be described with reference to flowchart illustrations and/or block diagrams of methods, apparatus (systems) and computer program products. It will be understood that each block of the flowchart illustrations and/or block diagrams, and combinations of blocks in the flowchart illustrations and/or block diagrams, may be implemented by computer program instructions. These computer program instructions may be provided to a processor of a general purpose computer, special purpose computer, or other programmable data processing apparatus to produce a machine, such that the instructions, which execute via the processor of the computer or other programmable data processing apparatus, create means for implementing the acts specified in the flowchart and/or block diagram block or blocks.

In certain embodiments, these computer program instructions may also be stored in a computer-readable memory 19 that can direct a computer or other programmable data processing apparatus to operate in a particular manner, such that the instructions stored in the computer-readable memory produce an article of manufacture including instruction means which implement the acts specified in the flowchart and/or block diagram block or blocks. The computer program instructions may also be loaded onto a computer or other programmable data processing apparatus to cause a series of operations to be performed on the computer or other programmable apparatus to produce a computer implemented process such that the instructions that execute on the computer or other programmable apparatus provide steps for implementing the acts specified in the flowchart and/or block diagram block or blocks.

The battery 21 can be any suitable battery for use in the wireless device 11, including, for example, a lithium-ion battery.

FIG. 3A is a schematic block diagram of one example of a power amplifier system 26. The illustrated power amplifier system 26 includes the switches 12, the antenna 14, the battery 21, a directional coupler 24, a power amplifier bias block 30, a power amplifier 32, and a transceiver 33. The illustrated transceiver 33 includes a baseband processor 34, an I/Q modulator 37, a mixer 38, and an analog-to-digital converter (ADC) 39.

The baseband signal processor 34 can be used to generate an I signal and a Q signal, which can be used to represent a sinusoidal wave or signal of a desired amplitude, frequency, and phase. For example, the I signal can be used to represent an in-phase component of the sinusoidal wave and the Q signal can be used to represent a quadrature component of

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the sinusoidal wave, which can be an equivalent representation of the sinusoidal wave. In certain implementations, the I and Q signals can be provided to the I/Q modulator 37 in a digital format. The baseband processor 34 can be any suitable processor configured to process a baseband signal. For instance, the baseband processor 34 can include a digital signal processor, a microprocessor, a programmable core, or any combination thereof. Moreover, in some implementations, two or more baseband processors 34 can be included in the power amplifier system 26.

The I/Q modulator 37 can be configured to receive the I and Q signals from the baseband processor 34 and to process the I and Q signals to generate a RF signal. For example, the I/Q modulator 37 can include DACs configured to convert the I and Q signals into an analog format, mixers for upconverting the I and Q signals to radio frequency, and a signal combiner for combining the upconverted I and Q signals into a RF signal suitable for amplification by the power amplifier 32. In certain implementations, the I/Q modulator 37 can include one or more filters configured to filter frequency content of signals processed therein.

The power amplifier bias block 30 can receive an enable signal ENABLE from the baseband processor 34 and a battery or power high voltage V_{CC} from the battery 21, and can use the enable signal ENABLE to generate a bias current I_{BIAS} for the power amplifier 32. Although FIG. 3A illustrates the battery 21 directly generating the power high voltage V_{CC} , in certain implementations the power high voltage V_{CC} can be a regulated voltage generated by a regulator that is electrically powered using the battery 21. The power amplifier 32 can receive the RF signal from the I/Q modulator 37 of the transceiver 33, and can provide an amplified RF signal to the antenna 14 through the switches 12.

The directional coupler 24 can be positioned between the output of the power amplifier 32 and the input of the switches 12, thereby allowing an output power measurement of the power amplifier 32 that does not include insertion loss of the switches 12. The sensed output signal from the directional coupler 24 can be provided to the mixer 38, which can multiply the sensed output signal by a reference signal of a controlled frequency so as to downshift the frequency content of the sensed output signal to generate a downshifted signal. The downshifted signal can be provided to the ADC 39, which can convert the downshifted signal to a digital format suitable for processing by the baseband processor 34. By including a feedback path between the output of the power amplifier 32 and the baseband processor 34, the baseband processor 34 can be configured to dynamically adjust the I and Q signals to optimize the operation of the power amplifier system 26. For example, configuring the power amplifier system 26 in this manner can aid in controlling the power added efficiency (PAE) and/or linearity of the power amplifier 32.

FIG. 3B is a schematic block diagram of another example of a power amplifier system 60. The illustrated power amplifier system 60 includes a power amplifier bias block 40, the battery 21, the power amplifier 32, an inductor 62, a first capacitor 63, a second capacitor 42, an impedance matching block 64, the switches 12, and the antenna 14.

The illustrated power amplifier 32 includes a bipolar transistor 61 having an emitter, a base, and a collector. The emitter of the bipolar transistor 61 can be electrically connected to a first or power low voltage V_L , which can be, for example, ground, and a radio frequency input signal RF_IN can be provided to the base of the bipolar transistor 61 through the first capacitor 42. The bipolar transistor 61

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can amplify the RF input signal RF_IN and provide the amplified RF signal at the collector. The bipolar transistor 61 can be any suitable device. In one implementation, the bipolar transistor 61 is a heterojunction bipolar transistor (HBT).

The power amplifier 32 can be configured to provide the amplified RF signal to the switches 12. The impedance matching block 64 can be used to aid in terminating the electrical connection between the power amplifier 32 and the switches 12. For example, the impedance matching block 64 can be used to increase power transfer and/or reduce reflections of the amplified RF signal.

The inductor 62 can be included to aid in electrically powering the power amplifier 32 with the power high voltage V_{CC} from the battery 21 while choking or blocking high frequency RF signal components. The inductor 62 can include a first end electrically connected to the power high voltage V_{CC} and a second end electrically connected to the collector of the bipolar transistor 61. The first or decoupling capacitor 63 is electrically connected between the power high voltage V_{CC} and the power low voltage V_L and can provide a low impedance path to high frequency signals, thereby reducing the noise of the power high voltage V_{CC} , improving power amplifier stability, and/or improving the performance of the inductor 62 as a RF choke.

The power amplifier bias block 40 is configured to receive an enable signal ENABLE and the battery or power high voltage V_{CC} . The power amplifier bias block 40 can use the enable signal ENABLE and the battery voltage V_{CC} to generate a bias current I_{BIAS} for biasing the power amplifier 32. For example, as illustrated in FIG. 3B, the power amplifier bias block 40 can be used to generate a bias current I_{BIAS} that can be used to bias the base of the bipolar transistor 61 of the power amplifier 32. The power amplifier bias block 40 can use the enable signal ENABLE to control or vary a magnitude of the bias current I_{BIAS} so as to enable or disable the power amplifier and thereby pulse the power amplifier's output. For example, when the enable signal ENABLE indicates the power amplifier 32 should be activated, the power amplifier bias block 40 can change the amplitude of the bias current I_{BIAS} so as to achieve a desired gain of the power amplifier 32. Similarly, when the enable signal ENABLE indicates that the power amplifier 32 should be deactivated, the power amplifier bias block 40 can decrease the bias current I_{BIAS} such that the gain of the power amplifier 32 is equal to about 0.

Although FIG. 3B illustrates one implementation of the power amplifier 32, skilled artisans will appreciate that the teachings described herein can be applied to a variety of power amplifier structures, including, for example, multi-stage power amplifier structures and/or power amplifiers employing other transistor structures.

Overview of Power Amplifier Bias Circuits

In certain implementations described herein, a power amplifier bias block includes a primary biasing circuit and a gain correction block including a time-dependent signal generator and a current amplifier. The time-dependent signal generator can be used to shape the enable signal of the power amplifier so as to generate a control current, which can be amplified by the current amplifier to generate a correction current. The primary biasing circuit can use the correction current to correct for a variation in gain of the power amplifier that can occur shortly after the power amplifier is enabled. Compensating for gain variation in the power amplifier can improve the power amplifier's performance, including, for example, the power amplifier's dynamic error vector magnitude (EVM).

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Including both the current amplifier and the time-dependent signal generator can permit the power amplifier bias block to be included on-die with the power amplifier. For example, by amplifying the control current generated by the time-dependent signal generator, the magnitude of the components of the time-dependent signal generator can be reduced to a size suitable for on-chip integration. In certain implementations, the time-dependent signal generator can include a resistor-capacitor (RC) network, and the current amplifier can be used to amplify the control current so as to reduce a magnitude of the resistor and/or capacitor needed to generate a suitable correction current, thereby permitting the time-dependent signal generator to be integrated on-chip with the power amplifier.

FIG. 4 is a schematic block diagram of one example of a power amplifier system 70 including a power amplifier bias block 50 according to one embodiment. The illustrated power amplifier system 70 includes the power amplifier bias block 50, the battery 21, and the power amplifier 32. The power amplifier 32 can be a single or multi-stage power amplifier, and in certain implementations can be similar to the power amplifier 32 described above with reference to FIG. 3B. The battery 21 can be any suitable battery, such as a lithium-ion battery, and be used to provide the battery or power high voltage V_{CC} to the power amplifier bias block 50 and to the power amplifier 32. The power amplifier bias block 50 and the power amplifier 32 can be integrated on a single die with one or more other components to form a packaged power amplifier module, which can be, for example, mounted to a RF circuit board associated with the wireless device 11 of FIG. 2.

The power amplifier bias block 50 includes a gain correction block 71 and a primary biasing circuit 74. The gain correction block 71 includes a time-dependent signal generator or control block 72 and a current amplifier 73. The power amplifier bias block 50 can receive an enable signal ENABLE, and use the enable signal ENABLE to generate a bias current I_{BIAS} using charge stored on the battery 21. The bias current I_{BIAS} can be provided to, for example, a base of a bipolar transistor of the power amplifier 32, as was described earlier.

The enable signal ENABLE can be used to control the power amplifier 32 so as to pulse the output of the power amplifier 32. For example, when the power amplifier 32 is configured to transmit a WLAN signal, the enable signal ENABLE can be selectively controlled so as to pulse the output of the power amplifier 32.

The power amplifier 32 can be configured to operate in a relatively noisy environment. For example, a die including the power amplifier 32 and the power amplifier bias block 50 can be provided in an electronic system that includes other electronic components including other power amplifiers, such as power amplifiers amplifying GSM and/or EDGE signals. These electronic components can cause noise on the power high voltage V_{CC} . Additionally, the power amplifier 32 can also be exposed to other non-ideal operation conditions. For example, the power amplifier 32 and the power amplifier bias block 50 can be exposed to a thermal gradient, and thus can be at different operating temperatures. Furthermore, the level of the power high voltage V_{CC} can vary depending on a charge of the device that the power amplifier 32 and the power amplifier bias block 50 are used in. The power amplifier bias block 50 can be used to compensate for a gain variation of the power amplifier 32 arising from these sources, as well as from other sources.

The power amplifier bias block 50 includes the time-dependent signal generator 72, which can be used to gen-

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erate a control current $I_{CONTROL}$ when the enable signal ENABLE is transitioned from a disabled state to an enabled state. The control current $I_{CONTROL}$ can be provided to the current amplifier 73, which can amplify the control current $I_{CONTROL}$ to generate a correction current $I_{CORRECTION}$. The correction current $I_{CORRECTION}$ can be used by the primary biasing circuit 74 to correct for a variation in gain over time that can occur shortly after the power amplifier 32 is enabled. For example, shortly after the power amplifier 32 is enabled, absent compensation the current of the primary biasing circuit 74 can come up slow due to thermal effects, and the gain of the power amplifier 32 can be low. By using the time-dependent signal generator 72 and the current amplifier 73 to provide a transient current boost to the power amplifier 32 after being enabled, the power amplifier 32 can be configured to have a substantially constant gain over time.

By including the current amplifier 73 to amplify the control current $I_{CONTROL}$ generated by the time-dependent signal generator 72, the magnitude of the components of the time-dependent signal generator 72 can be reduced. For example, the current amplifier 73 can be used to amplify the control current $I_{CONTROL}$ so as to reduce a size of a component of the time-dependent signal generator 72 needed to generate a correction current with correct time constant, thereby permitting the time-dependent signal generator to be integrated on-chip with the power amplifier 32.

The primary bias circuit 74 can be configured to generate a relatively constant bias current output that can be adjusted by the correction current $I_{CORRECTION}$ to correct for a variation in gain of the power amplifier 32 that can occur shortly after the power amplifier 32 is enabled. In certain implementations, the primary bias circuit 74 can be a conventional bias circuit that is modified such that the output of the bias circuit is adjusted based on the amplitude of the correction current $I_{CORRECTION}$. Additional detail of the primary bias circuit 74 can be as described later below.

FIG. 5 is a circuit diagram of a power amplifier bias block 80 according to one embodiment. The power amplifier bias block 80 includes a resistor-capacitor (RC) network 82, a current mirror 83, and a primary bias circuit 84. The RC network 82 operates as a time-dependent signal generator and the current mirror 83 operates as a current amplifier. The power amplifier bias block 80 is configured to receive an enable signal ENABLE and a battery or power high voltage V_{CC} , and to generate a bias current I_{BIAS} .

The RC network 82 includes a first resistor 91, a second resistor 92, and a capacitor 90. The first resistor 91 includes a first end electrically connected to a first end of the capacitor 90 at an input of the RC network 82 configured to receive the enable signal ENABLE. The first resistor 91 further includes a second end electrically connected to a first end of the second resistor 92 at an output of the RC network 82 configured to provide the control current $I_{CONTROL}$ to the current mirror 83. The second resistor 92 further includes a second end electrically connected to a second end of the capacitor 90.

The RC network 82 can be used to shape the enable signal ENABLE so as to generate the control current $I_{CONTROL}$. For example, the capacitor 90 and the second resistor 92 can have an RC time-constant selected to achieve the desired shape of the control current $I_{CONTROL}$. The RC time-constant can be selected based on a system parameter of the electronic system that the power amplifier bias block 80 is used in, including, for example, a transition time of the enable signal ENABLE. In certain implementations, the time-con-

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stant of the second resistor 92 and the capacitor 90 is in the range of about 0.1 μ s to about 10 μ s, for example, about 1 μ s.

In certain implementations, the capacitor 90 has a capacitance ranging between about 10 pF to about 50 pF, for example, about 25 pF. The second resistor 92 can have any suitable resistance, including, for example, a resistance in the range of about 10 k Ω to about 100 k Ω , for example, about 50 k Ω . Although one implementation of the capacitor 90 and the second resistor 92 is illustrated, other configurations are possible. For example, the order of the second resistor 92 and the capacitor 90 in the series combination of the second resistor 92 and the capacitor 90 can be reversed. The first resistor 91 can have any suitable value, including, for example, a resistance in the range of about 1 k Ω to about 20 k Ω , for example, about 10 k Ω . In certain implementations, such as the implementation shown in FIG. 9, the first resistor 91 can be omitted.

To aid in reducing the area of the RC network 82, the current mirror 83 can be used to amplify the control current $I_{CONTROL}$ to generate the correction current $I_{CORRECTION}$. Thus, the amplifier 83 can be used to obtain a correction current $I_{CORRECTION}$ of a suitable magnitude, while reducing the size of the components of the RC network 82 relative to a scheme omitting a current amplifier. By amplifying the control current $I_{CONTROL}$ in this manner, the power amplifier bias block 80 can be integrated on-chip with a power amplifier without having to use a relatively large resistor, which may not provide enough current variation to provide suitable gain compensation.

The illustrated current mirror 83 includes a first NPN bipolar transistor 85, a second NPN bipolar transistor 86, a third NPN bipolar transistor 87, a fourth NPN bipolar transistor 88, and a resistor 89. The first NPN bipolar transistor 85 includes an emitter electrically connected to the first or power low voltage V_1 , which can be, for example, ground, and a base and a collector electrically connected to a base of the second NPN bipolar transistor 86 at an input of the current mirror 83 configured to receive the control current $I_{CONTROL}$. The second NPN bipolar transistor 86 further includes an emitter electrically connected to the power low voltage V_1 , and a collector electrically connected to a first end of the resistor 89, to a base of the fourth NPN bipolar transistor 88, and to a base and a collector of the third NPN bipolar transistor 87. The third and fourth NPN bipolar transistors 87, 88 each include an emitter electrically connected to the power low voltage V_1 . The resistor 89 includes a second end configured to receive the enable signal ENABLE. The fourth NPN bipolar transistor 88 further includes a collector configured to generate the correction current $I_{CORRECTION}$.

The resistor 89 can have any suitable resistance, including, for example, a resistance selected based on the voltage level of power amplifier enable signal ENABLE and/or system requirements. In certain implementations, the resistor 89 has a resistance ranging between about 10 k Ω to about 50 k Ω , for example, about 20 k Ω . By electrically connected the second end of the resistor 89 to the enable signal ENABLE, the power consumption of the power amplifier bias block 80 can be reduced when the enable signal ENABLE is low. However, in other implementations, the current mirror 83 can be configured in other ways.

The current mirror 83 can have any suitable gain. In one implementation, the current mirror 83 is configured to amplify the control current $I_{CONTROL}$ by a factor ranging between about 5 to about 50, for example, about 10. As used herein, the term current mirror can refer to current amplifi-

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cation circuits including a plurality of current mirrors combined (e.g., cascaded) to achieve a target gain.

The primary bias circuit 84 can be used to generate a bias current I_{BIAS} for a power amplifier, such as the power amplifier 32 of FIG. 4. The illustrated primary bias circuit 84 includes a first resistor 96, a second resistor 97, a first NPN bipolar transistor 93, a second NPN bipolar transistor 94 and a third NPN bipolar transistor 95. The first resistor 96 includes a first end electrically connected to a first end of the second resistor 97 at an input of the primary bias circuit 84 configured to receive the enable signal ENABLE. The first resistor 96 further includes a second end electrically connected to an emitter of the second NPN bipolar transistor 94 and to a base and a collector of the first NPN bipolar transistor 93 at an input of the primary bias circuit 84 configured to receive the correction current $I_{CORRECTION}$. The first NPN bipolar transistor 93 further includes an emitter electrically connected to the power low voltage V_1 . The second resistor 97 further includes a second end electrically connected to a base and a collector of the second NPN bipolar transistor 94 and to a base of the third NPN bipolar transistor 95. The third NPN bipolar transistor 95 further includes a collector electrically connected to the power high voltage V_{CC} and an emitter configured to generate the bias current I_{BIAS} .

The first NPN bipolar transistor 93 can aid in level-shifting the voltage of the emitter of the second NPN bipolar transistor 94, which in turn can impact the emitter voltage of the third NPN bipolar transistor 95. Thus, inclusion of the first NPN bipolar transistor 93 can aid in establishing suitable DC operating voltage levels of the power amplifier bias block 80.

The first and second resistors 96, 97 can be tuned to control the steady-state amplitude of the bias current I_{BIAS} when the enable signal ENABLE is activated. For example, the current through the second NPN bipolar transistor 94 can be established using the first and second resistors 96, 97, and can be mirrored using the third NPN bipolar transistor 95 to generate the bias current I_{BIAS} .

After the enable signal ENABLE becomes activated, the RC network 82 can generate a control current $I_{CONTROL}$ that can be amplified by the current mirror 83 to generate the correction current $I_{CORRECTION}$. As illustrated in FIG. 5, the correction current $I_{CORRECTION}$ can be used to vary or change the current through the second NPN bipolar transistor 94. For example, when the correction current $I_{CORRECTION}$ decreases, the current through the second NPN bipolar transistor 94 can increase, which in turn can increase the bias current I_{BIAS} generated using the third NPN bipolar transistor 95. The second NPN bipolar transistor 94 can also aid in reversing the direction of the correction current $I_{CORRECTION}$ so that it is suitable to be provided to the base of the fifth NPN bipolar transistor 95. Although one variation of a primary bias circuit is illustrated, other implementations can be used.

FIG. 6 is a graph 100 of one example of collector current versus time. The graph 100 begins at a time zero that is associated with enabling a power amplifier. The graph 100 includes a first plot 101, a second plot 102, a third plot 103, a fourth plot 104 and a fifth plot 105, which correspond to different battery voltage values. In particular, the first, second, third, fourth, and fifth plots 101-105 correspond to battery voltage values of about 3.2 V, about 3.4 V, about 3.6 V, about 3.8 V, and about 4.0 V, respectively.

In certain implementations described herein, a time-dependent signal generator is used to generate a signal that can be used to adjust a power amplifier's bias current during a

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time period within about 8 μ s after the power amplifier is enabled. Thereafter the power amplifier's bias current can be substantially constant until the power amplifier's enable signal is deactivated. In certain implementations, the power amplifier's bias current can vary by more than about 50% during the initial time period that the correction current is used to adjust the power amplifier's bias current.

FIG. 7A is a graph 110 of one example of dynamic error vector magnitude (EVM) versus output power. The graph 110 is for one example of a power amplifier bias block that does not include a time-dependent signal generator and a current amplifier. The graph 110 includes plots of EVM versus output power for a variety of different battery voltage levels. For example, the graph 110 includes plots 111-119, which correspond to battery voltages ranging between about 3.2 V and about 4.2 V.

FIG. 7B is a graph 120 of another example of dynamic EVM versus output power. The graph 120 is for one implementation of a power amplifier bias block that includes a time-dependent signal generator and a current amplifier. The graph 120 includes plots of EVM versus output power for a variety of different battery voltage levels. For example, the graph 120 includes plots 121-129, which correspond to battery voltages between about 3.2 V and about 4.2 V. The graph 120 shows that the EVM of the power amplifier system can be improved by including the time-dependent signal generator and the current amplifier.

FIG. 8 is a flow chart illustrating a method 150 for biasing a power amplifier in accordance with one embodiment. It will be understood that the method 150 can include greater or fewer operations and the operations may be performed in any order, as necessary.

The method 150 starts at a block 151, in which an enable signal of a power amplifier is shaped using a time-dependent signal generator to generate a control current. The power amplifier can be any suitable power amplifier, such as a power amplifier configured to amplify a WLAN signal. In certain implementations, the time-dependent signal generator includes a resistor-capacitor (RC) network configured to generate a transient control current that begins after an enable signal of the power amplifier is activated. In certain implementations, the transient control current reaches a steady-state value within about 8 μ s after the enable signal is activated. In certain implementations, the steady-state value of the transient control current can be about 0 mA.

In an ensuing block 152, the control current is amplified using the current amplifier to generate a correction current. In certain implementations, the current amplifier amplifies the correction circuit by a factor ranging between about 5 to about 50. The current amplifier can aid the time-dependent signal generator in shaping the enable signal by reducing the size of the circuit components of the time-dependent signal generator needed to achieve a desired time constant associated with gain compensation.

The method 150 continues at a block 153, in which a bias current for the power amplifier is generated using the primary biasing circuit. The primary biasing circuit is configured to use the correction current to generate a bias current for the power amplifier so as correct for a variation in gain of the power amplifier when the power amplifier is enabled. For example, the primary biasing circuit can be configured to adjust the amplitude of the bias current based on the correction current, such as by adding the correction current to a nominal bias current value.

FIG. 9 is a circuit diagram of a time-dependent signal generator 170 in accordance with one embodiment. The time-dependent signal generator 170 includes a resistor 92

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and a capacitor 90, which can be similar to the resistor 92 and the capacitor 90 of the time-dependent signal generator 82 of FIG. 5. However, in contrast to the time-dependent signal generator 82 of FIG. 5, the time-dependent signal generator 170 of FIG. 9 does not include the resistor 91 of FIG. 4. In certain implementations, the time-constant of the resistor 92 and the capacitor 90 is in the range of about 0.1 μ s to about 10 μ s, for example, about 1 μ s.

FIG. 10A is a schematic diagram of one example of a packaged power amplifier module 300. FIG. 10B is a schematic diagram of a cross-section of the packaged power amplifier module 300 of FIG. 10A taken along the lines 10B-10B.

The packaged power amplifier module 300 includes an IC or die 301, surface mount components 303, wirebonds 308, a package substrate 320, and encapsulation 340. The package substrate 320 includes pads 306 formed from conductors disposed therein. Additionally, the die 301 includes pads 304, and the wirebonds 308 have been used to electrically connect the pads 304 of the die 301 to the pads 306 of the package substrate 301.

As illustrated in FIGS. 10A and 10B, the die 301 includes the power amplifier 32 and the power amplifier bias block 50 formed therein. The power amplifier bias block 50 includes the time dependent signal generator 72, the current amplifier 73, and the primary biasing circuit 74. In certain implementations, the time-dependent signal generator 72 can include a resistor-capacitor (RC) network, and the current amplifier 73 can be used to amplify a control current from the RC network to generate a correction current, which can be used by the primary biasing circuit 74 to generate a bias current for the power amplifier 32 that corrects for a gain variation of the power amplifier 32 associated with transitioning the power amplifier from a disabled state to an enabled state. Using the current amplifier 73 to amplify the control current from the time-dependent signal generator 72 can reduce a magnitude of the resistor and/or capacitor needed to generate a suitable correction current, thereby permitting the time-dependent signal generator 72 to be integrated on-chip with the power amplifier 32, as shown in FIG. 10A.

The packaging substrate 320 can be configured to receive a plurality of components such as the die 301 and the surface mount components 303, which can include, for example, surface mount capacitors and/or inductors.

As shown in FIG. 10B, the packaged power amplifier module 300 is shown to include a plurality of contact pads 332 disposed on the side of the packaged power amplifier module 300 opposite the side used to mount the die 301. Configuring the packaged power amplifier module 300 in this manner can aid in connecting the packaged power amplifier module 300 to a circuit board such as a phone board of a wireless device. The example contact pads 332 can be configured to provide RF signals, bias signals, power low voltage(s) and/or power high voltage(s) to the die 301 and/or the surface mount components 303. As shown in FIG. 10B, the electrically connections between the contact pads 332 and the die 301 can be facilitated by connections 333 through the package substrate 320. The connections 333 can represent electrical paths formed through the package substrate 320, such as connections associated with vias and conductors of a multilayer laminated package substrate.

In some embodiments, the packaged power amplifier module 300 can also include one or more packaging structures to, for example, provide protection and/or to facilitate handling of the packaged power amplifier module 300. Such a packaging structure can include overmold or encapsulation

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340 formed over the packaging substrate 320 and the components and die(s) disposed thereon.

It will be understood that although the packaged power amplifier module 300 is described in the context of wire-bond-based electrical connections, one or more features of the present disclosure can also be implemented in other packaging configurations, including, for example flip-chip configurations.

Applications

Some of the embodiments described above have provided examples in connection with mobile phones. However, the principles and advantages of the embodiments can be used for any other systems or apparatus that have needs for power amplifier systems.

Such power amplifier systems can be implemented in various electronic devices. Examples of the electronic devices can include, but are not limited to, consumer electronic products, parts of the consumer electronic products, electronic test equipment, etc. Examples of the electronic devices can also include, but are not limited to, memory chips, memory modules, circuits of optical networks or other communication networks, and disk driver circuits. The consumer electronic products can include, but are not limited to, a mobile phone, a telephone, a television, a computer monitor, a computer, a hand-held computer, a personal digital assistant (PDA), a microwave, a refrigerator, an automobile, a stereo system, a cassette recorder or player, a DVD player, a CD player, a VCR, an MP3 player, a radio, a camcorder, a camera, a digital camera, a portable memory chip, a washer, a dryer, a washer/dryer, a copier, a facsimile machine, a scanner, a multi functional peripheral device, a wrist watch, a clock, etc. Further, the electronic devices can include unfinished products.

Conclusion

Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not limited to." The word "coupled", as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Likewise, the word "connected", as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words "herein," "above," "below," and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word "or" in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

Moreover, conditional language used herein, such as, among others, "can," "could," "might," "can," "e.g.," "for example," "such as" and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments or that one or more embodiments necessarily include logic for deciding, with or without

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author input or prompting, whether these features, elements and/or states are included or are to be performed in any particular embodiment.

The above detailed description of embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise form disclosed above. While specific embodiments of, and examples for, the invention are described above for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. For example, while processes or blocks are presented in a given order, alternative embodiments may perform routines having steps, or employ systems having blocks, in a different order, and some processes or blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these processes or blocks may be implemented in a variety of different ways. Also, while processes or blocks are at times shown as being performed in series, these processes or blocks may instead be performed in parallel, or may be performed at different times.

The teachings of the invention provided herein can be applied to other systems, not necessarily the system described above. The elements and acts of the various embodiments described above can be combined to provide further embodiments.

While certain embodiments of the inventions have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

What is claimed is:

1. A mobile device comprising:

a transceiver configured to generate a radio frequency signal and a power amplifier enable signal;

a power amplifier configured to provide amplification to the radio frequency signal, the power amplifier configured to receive a bias signal that biases the power amplifier; and

a bias circuit configured to receive the power amplifier enable signal and to generate the bias signal, the bias circuit including a gain correction circuit configured to generate a control current in response to activation of the power amplifier enable signal and to mirror the control current to generate a correction current, and a primary biasing circuit configured to generate the bias signal based on the correction current and the power amplifier enable signal.

2. The mobile device of claim 1 wherein the primary bias circuit includes a first transistor, the correction current configured to change a current flowing through the first transistor.

3. The mobile device of claim 2 wherein the primary bias circuit further includes a resistor, the first transistor configured to receive the power amplifier enable signal via the resistor.

4. The mobile device of claim 2 wherein the primary bias circuit further includes a second transistor electrically coupled to the first transistor and configured to provide the bias signal to the power amplifier.

5. The mobile device of claim 1 wherein the power amplifier includes an output configured to provide a wireless

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local area network signal, the power amplifier enable signal operable to pulse the output of the power amplifier.

6. The mobile device of claim 1 wherein the gain correction circuit includes a current mirror configured to generate the correction current by mirroring the control current, the current mirror configured to receive the power amplifier enable signal.

7. The mobile device of claim 1 wherein the gain correction circuit includes a time-dependent signal generator that receives the power amplifier enable signal at an input and generates the control current at an output, the time-dependent signal generator including a capacitor and a first resistor electrically connected in a first electrical path from the input to the output.

8. The mobile device of claim 7 wherein the time-dependent signal generator further includes a second resistor electrically connected in a second electrical path from the input to the output.

9. A method of power amplifier biasing, the method comprising:

generating a radio frequency signal and a power amplifier enable signal using a transceiver;
providing amplification to the radio frequency signal using a power amplifier;
generating a control current in response to activation of the power amplifier enable signal using a gain correction circuit;
mirroring the control current to generate a correction current using the gain correction circuit;
generating a bias signal based on the correction current and the power amplifier enable signal using a primary biasing circuit; and
biasing the power amplifier using the bias signal.

10. The method of claim 9 wherein generating the bias signal includes changing a current flowing through a first bipolar transistor of the primary biasing circuit based on the correction current, and providing the power amplifier enable signal to a collector and a base of the first bipolar transistor via a first resistor of the primary biasing circuit.

11. The method of claim 10 wherein generating the bias signal further includes providing the power amplifier enable signal to an emitter of the first bipolar transistor via a second resistor of the primary biasing circuit.

12. The method of claim 10 wherein generating the bias signal further includes generate a bias current using an emitter of a second bipolar transistor of the primary biasing circuit, the second bipolar transistor including a base coupled to the base of the first bipolar transistor.

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13. The method of claim 9 wherein mirroring the control current includes receiving the control current at an input of a current mirror and providing the correction current at an output of the current mirror, the method further including controlling the current mirror using the power amplifier enable signal.

14. A packaged module comprising:

a package substrate; and

an integrated circuit attached to the package substrate and including a power amplifier configured to provide amplification to a radio frequency signal and a bias circuit configured to receive a power amplifier enable signal and to generate a bias signal that biases the power amplifier, the bias circuit including a gain correction circuit configured to generate a control current in response to activation of the power amplifier enable signal and to mirror the control current to generate a correction current, and a primary biasing circuit configured to generate the bias signal based on the correction current and the power amplifier enable signal.

15. The packaged module of claim 14 wherein the primary bias circuit includes a first transistor, the correction current configured to change a current flowing through the first transistor.

16. The packaged module of claim 15 wherein the primary bias circuit further includes a resistor, the first transistor configured to receive the power amplifier enable signal via the resistor.

17. The packaged module of claim 14 wherein the gain correction circuit includes a current mirror configured to generate the correction current by mirroring the control current, the current mirror configured to receive the power amplifier enable signal.

18. The packaged module of claim 14 wherein the gain correction circuit includes a time-dependent signal generator that receives the power amplifier enable signal at an input and generates the control current at an output, the time-dependent signal generator including a capacitor and a first resistor electrically connected in a first electrical path from the input to the output.

19. The packaged module of claim 18 wherein the time-dependent signal generator further includes a second resistor electrically connected in a second electrical path from the input to the output.

20. The packaged module of claim 15 wherein the primary bias circuit further includes a second transistor electrically coupled to the first transistor and configured to provide the bias signal to the power amplifier.

* * * * *

EXHIBIT 8

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United States Patent and Trademark Office

March 21, 2024

THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM
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PATENT NUMBER: 9,450,579

ISSUE DATE: *September 20, 2016*

By Authority of the
Under Secretary of Commerce for Intellectual Property
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John Burson
Certifying Officer





US009450579B2

(12) **United States Patent**
Madan et al.

(10) **Patent No.:** **US 9,450,579 B2**
(45) **Date of Patent:** **Sep. 20, 2016**

(54) **RADIO FREQUENCY DEVICES HAVING
REDUCED INTERMODULATION
DISTORTION**

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(73) Assignee: **Skyworks Solutions, Inc.**, Woburn,
MA (US)

(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/833,076**

(22) Filed: **Aug. 22, 2015**

(65) **Prior Publication Data**

US 2015/0365088 A1 Dec. 17, 2015

Related U.S. Application Data

(62) Division of application No. 13/936,175, filed on Jul.
6, 2013, now Pat. No. 9,148,194.

(60) Provisional application No. 61/669,045, filed on Jul.
7, 2012.

(51) **Int. Cl.**

H04B 1/44 (2006.01)

H03K 17/687 (2006.01)

H04B 1/48 (2006.01)

H03K 17/693 (2006.01)

H01L 21/84 (2006.01)

(Continued)

(52) **U.S. Cl.**

CPC **H03K 17/687** (2013.01); **H01L 21/84**

(2013.01); **H01L 27/0629** (2013.01); **H01L**
27/1203 (2013.01); **H03K 17/693** (2013.01);
H04B 1/44 (2013.01); **H04B 1/48** (2013.01);
H03K 2217/0018 (2013.01); **H03K 2217/0054**
(2013.01)

(58) **Field of Classification Search**

CPC **H04B 1/44**
USPC **455/78, 87, 252.1, 296; 438/178, 197,**
438/381; 327/427, 434, 436, 437
See application file for complete search history.

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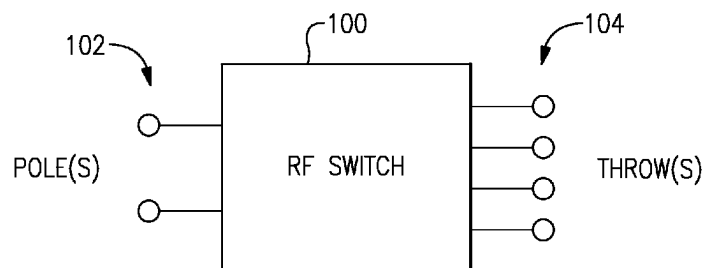
Primary Examiner — Tuan H Nguyen

(74) *Attorney, Agent, or Firm* — Chang & Hale LLP

(57) **ABSTRACT**

Radio-frequency (RF) devices are disclosed providing reduced intermodulation distortion. Disclosed RF and semiconductor devices can include a semiconductor substrate, a switch formed on the semiconductor substrate having a stack of field-effect transistors (FETs) connected in series, and a capacitor formed on the semiconductor substrate and connected in series with the switch, the capacitor configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

18 Claims, 9 Drawing Sheets



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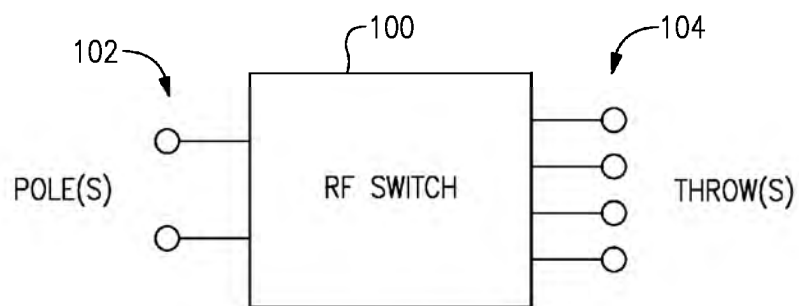


FIG.1

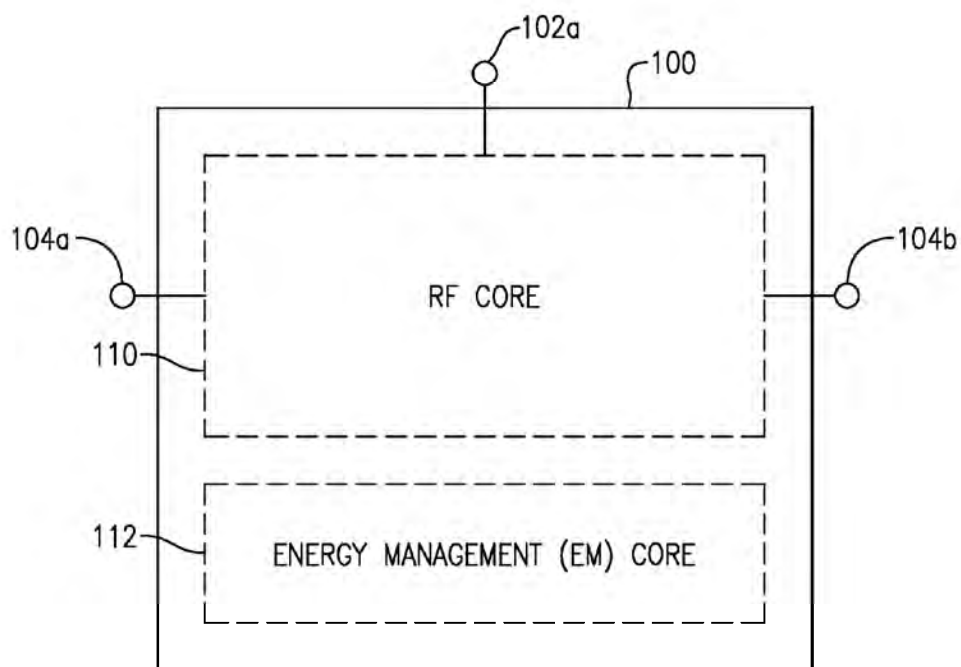


FIG.2

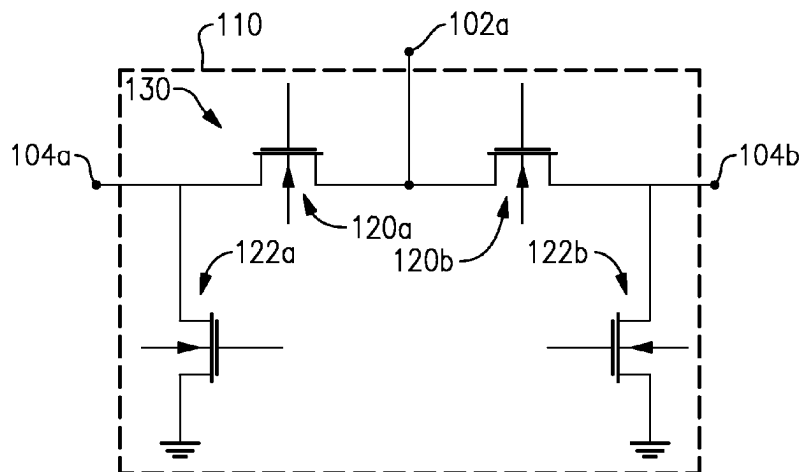


FIG. 3

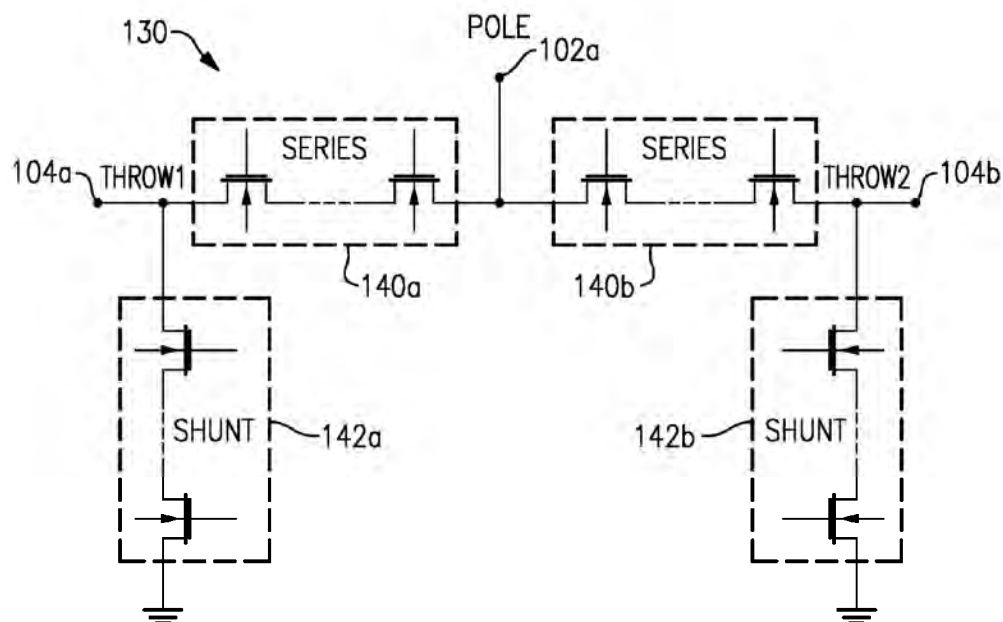


FIG. 4

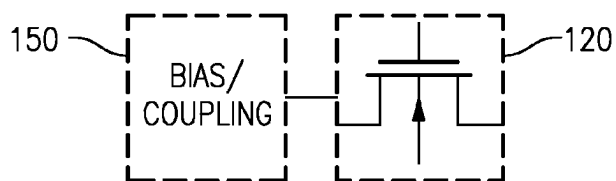


FIG.5

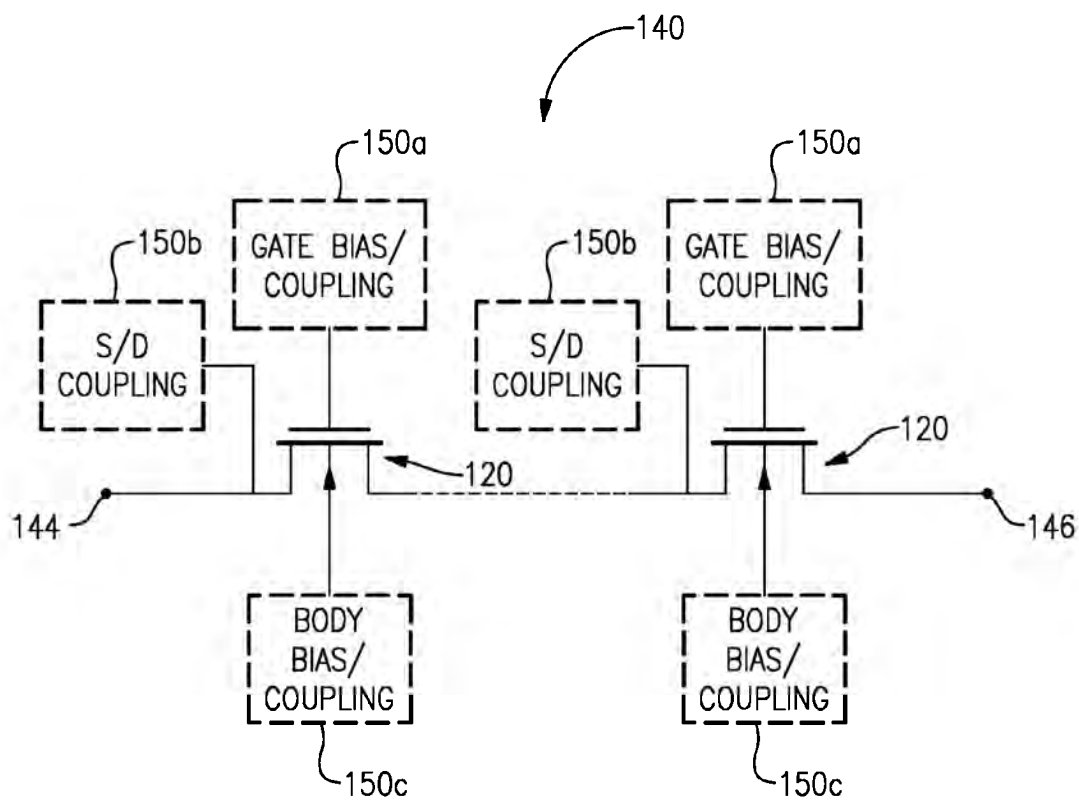


FIG.6

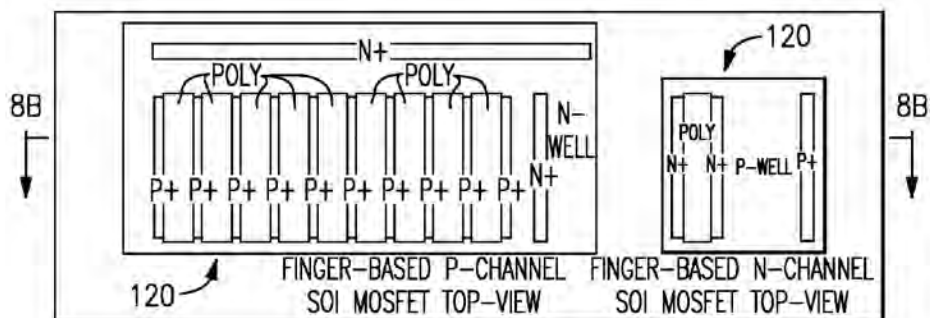
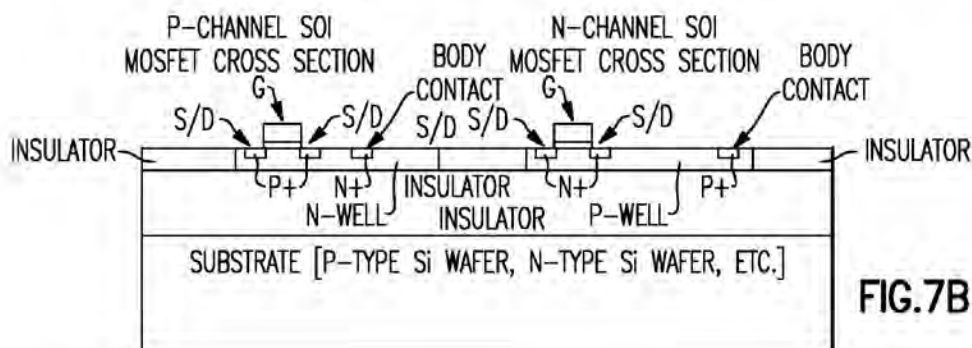
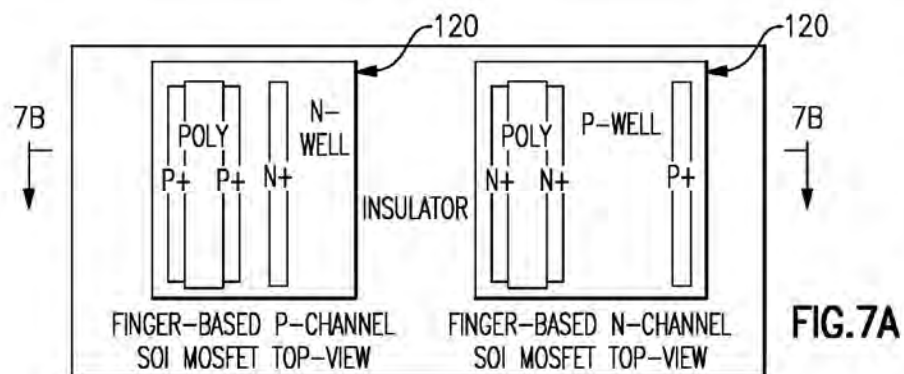


FIG. 8A

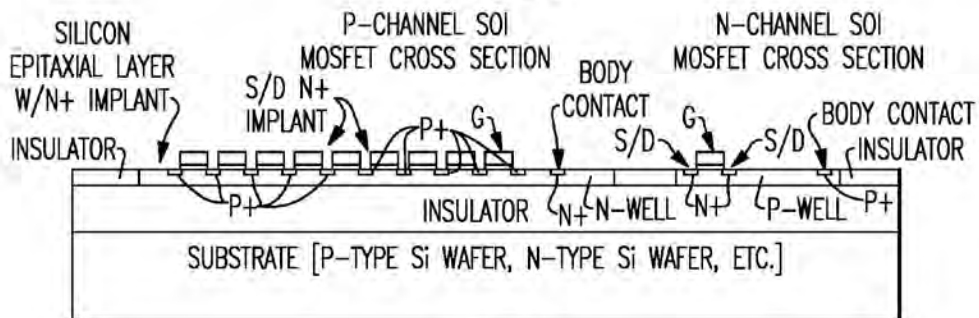


FIG. 8B

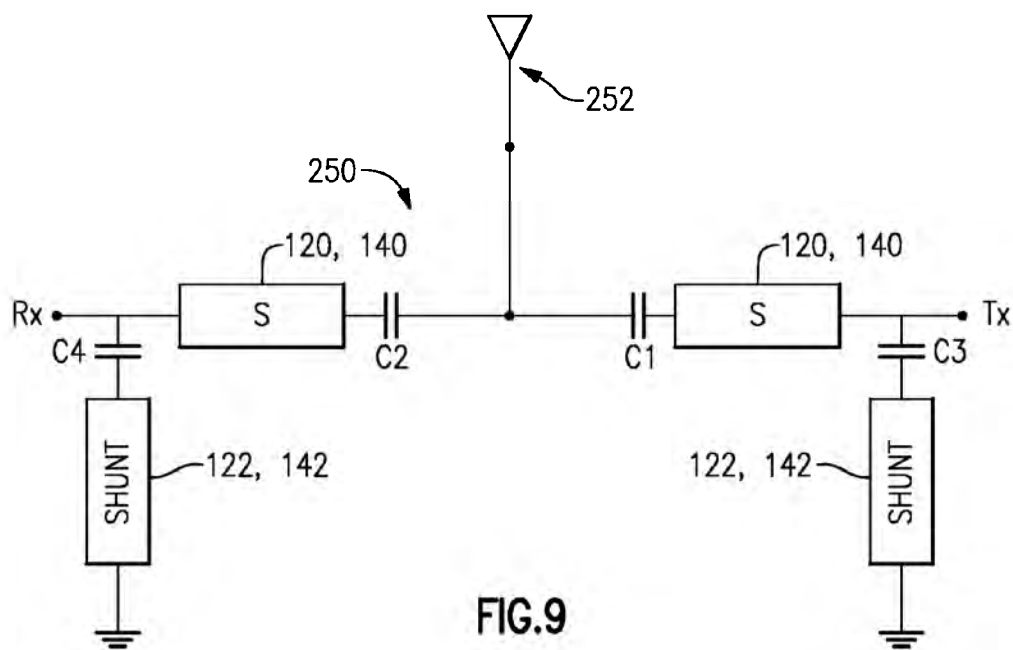


FIG. 9

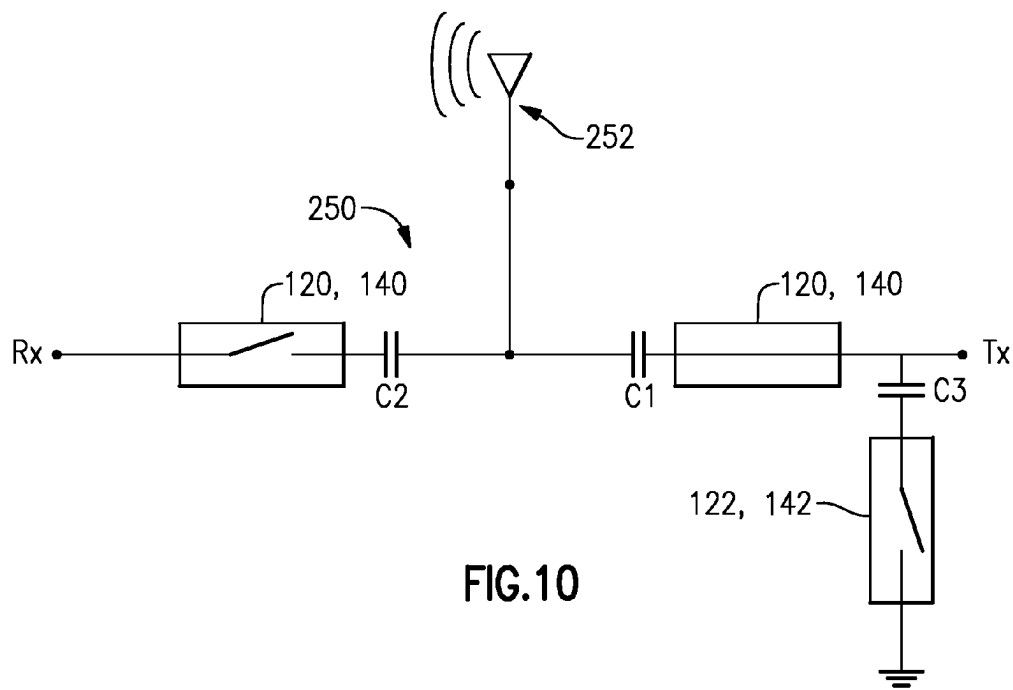
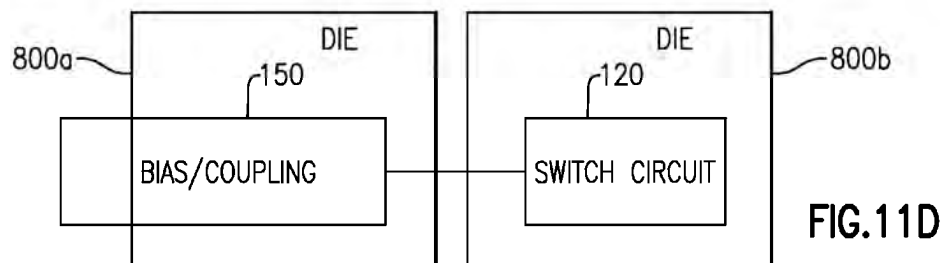
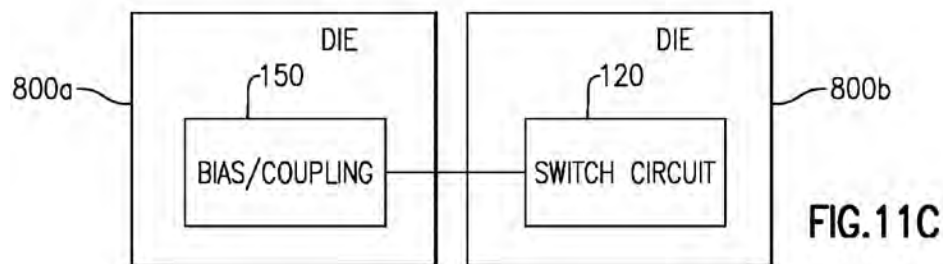
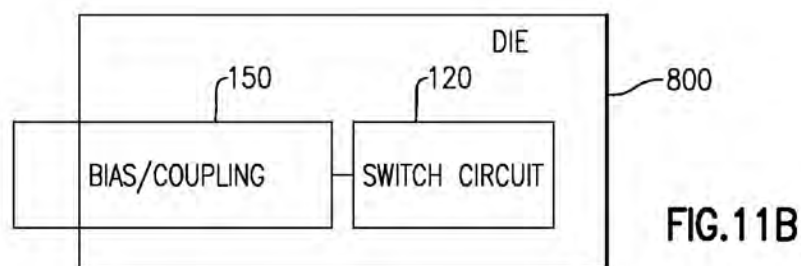
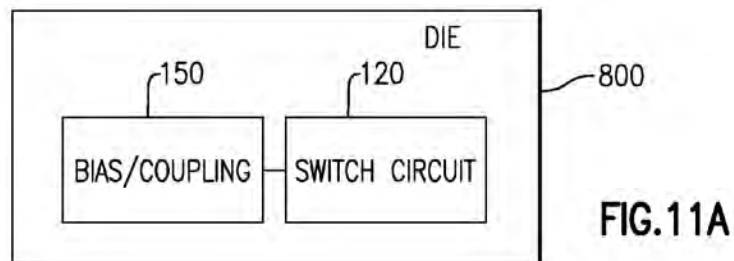


FIG. 10



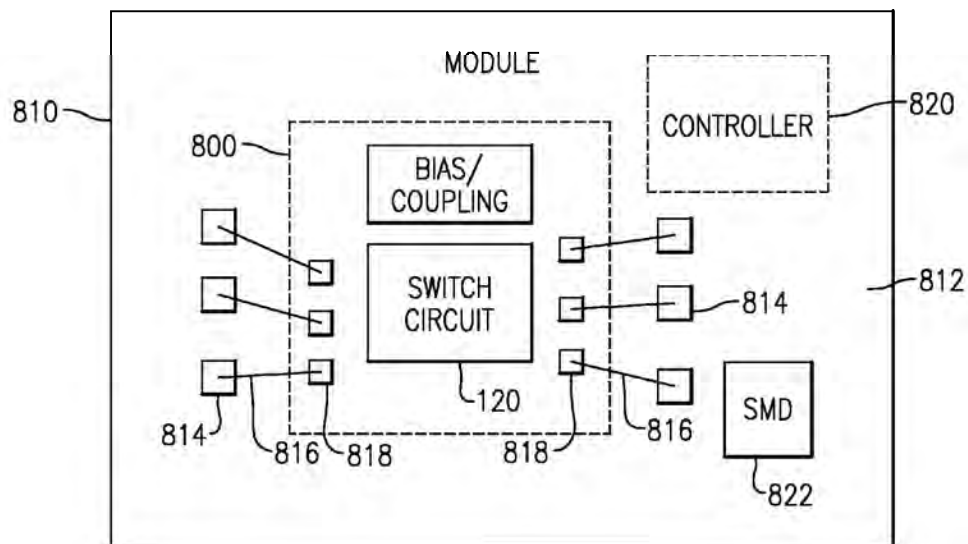


FIG. 12A

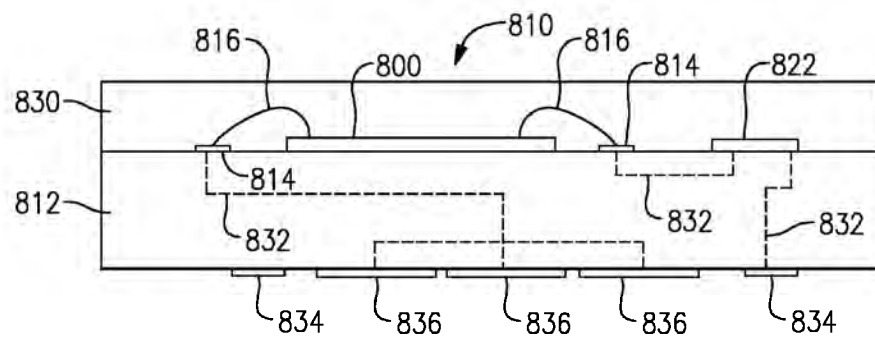


FIG. 12B

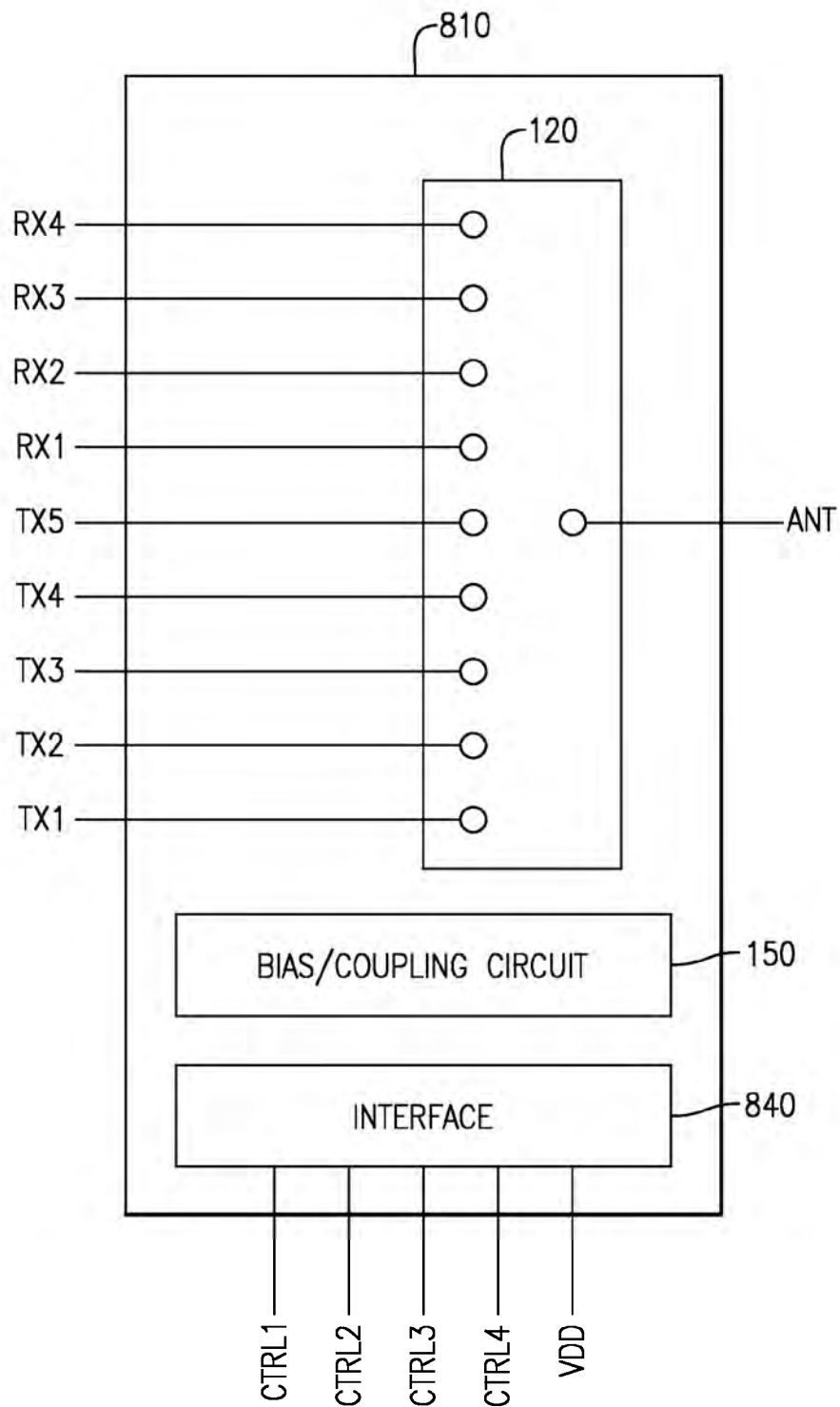


FIG.13

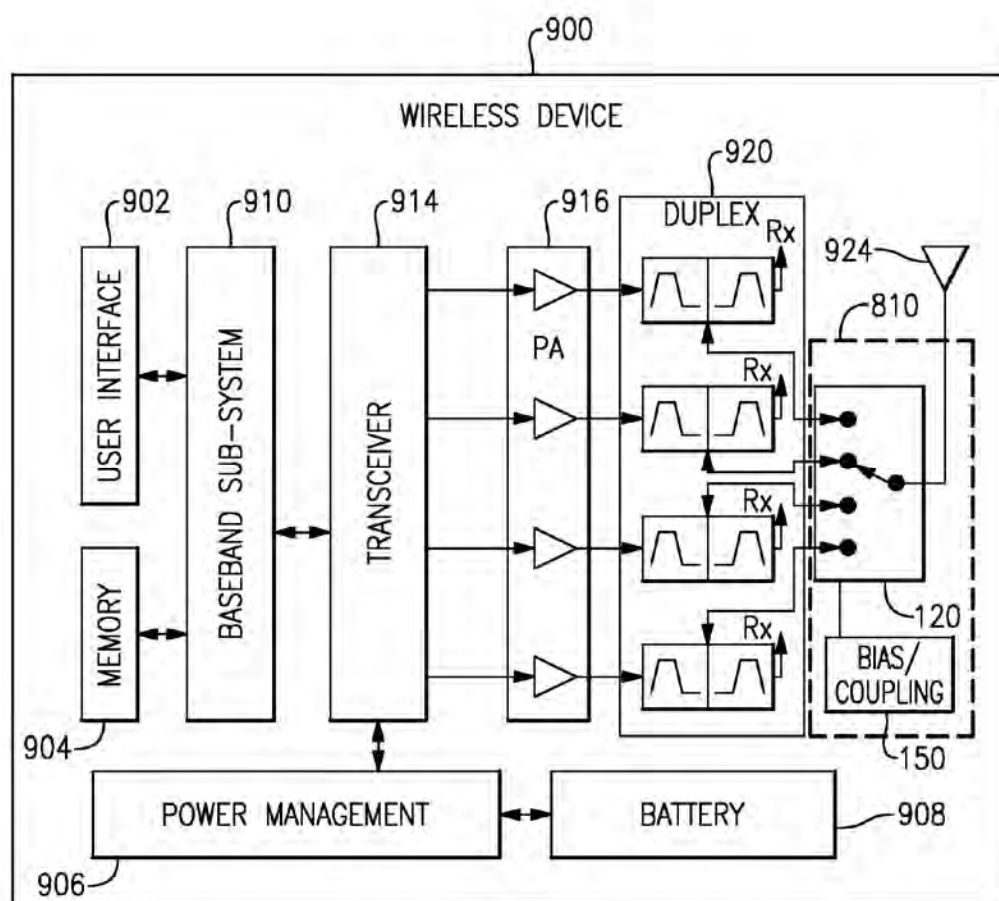


FIG.14