RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION

RELATED APPLICATION

This application is a divisional of U.S. patent application Ser. No. 13/936,175, filed on Jul. 6, 2013, titled "Radio-Frequency Switch System Having Improved Intermodulation Distortion Performance," which claims priority to U.S. Provisional Application No. 61/669,045, filed on Jul. 7, 2012, and entitled "Radio-Frequency Switch System Having Improved Intermodulation Distortion Performance," the disclosures of which are hereby incorporated by reference in its entirety.

BACKGROUND

1. Field

The present disclosure generally relates to the field of electronics, and more particularly, to radio-frequency switches.

2. Description of Related Art

Radio-frequency (RF) switches, such as transistor switches, can be used to switch signals between one or more poles and one or more throws. Transistor switches, or portions thereof, can be controlled through transistor biasing and/or coupling. Design and use of bias and/or coupling circuits in connection with RF switches can affect switching performance.

SUMMARY

In some implementations, the present disclosure relates to a radio-frequency (RF) switch system that includes a switch having a stack of field-effect transistors (FETs) connected in series between first and second nodes. The system further includes a capacitor connected in series with the switch and configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

In some embodiments, the FETs can be silicon-on-insulator (SOI) FETs. In some embodiments, the first node can be an antenna node. The capacitor can be disposed between the switch and the antenna node. The switch can be part of a transmit path such that the second node of the switch is an input node for an amplified RF signal. The switch can be part of a receive path such that the second node of the switch is an output node for an RF signal received from the antenna.

According to some implementations, the present disclosure relates to a semiconductor die having a semiconductor substrate and a switch formed on the semiconductor substrate and having a stack of field-effect transistors (FETs) connected in series. The die further includes a capacitor formed on the semiconductor substrate and connected in series with the switch. The capacitor is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

In some embodiments, the die can further include an insulator layer disposed between the FETs and the semiconductor substrate. The die can be a silicon-on-insulator (SOI) die.

In a number of implementations, the present disclosure relates to a method for fabricating a semiconductor die. The method includes providing a semiconductor substrate and forming a stack of field-effect transistors (FETs) on the semiconductor substrate so as to be connected in series. The method further includes forming a capacitor on the semiconductor substrate so as to be connected in series with an end of the stack. The capacitor is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the stack.

In some embodiments, the method can further include forming an insulator layer between the FETs and the semiconductor substrate.

In accordance with some implementations, the present disclosure relates to a radio-frequency (RF) switch module that includes a packaging substrate configured to receive a plurality of components. The module further includes a semiconductor die mounted on the packaging substrate. The die includes a switch having a stack of field-effect transistors (FETs) connected in series. The module further includes a capacitor connected in series with the switch. The capacitor is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

In some embodiments, the semiconductor die can be a silicon-on-insulator (SOI) die. In some embodiments, the capacitor can be part of the same semiconductor die as the FETs. In some embodiments, the capacitor can be part of a second die mounted on the packaging substrate. In some embodiments, the capacitor circuit can be disposed at a location outside of the semiconductor die.

In an number of implementations, the present disclosure relates to a wireless device that includes a transceiver configured to process RF signals. The wireless device further includes an antenna in communication with the transceiver. The wireless device further includes a switch module interconnected to the antenna and the transceiver and configured to selectively route RF signals to and from the antenna. The switch module includes a switch having a stack of field-effect transistors (FETs) connected in series. The switch module further includes a capacitor connected in series with the switch. The capacitor is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

BRIEF DESCRIPTION OF THE DRAWINGS

Various embodiments are depicted in the accompanying drawings for illustrative purposes, and should in no way be interpreted as limiting the scope of the inventions. In addition, various features of different disclosed embodiments can be combined to form additional embodiments, which are part of this disclosure. Throughout the drawings, reference numbers may be reused to indicate correspondence between reference elements.

FIG. **1** schematically shows a radio-frequency (RF) switch configured to switch one or more signals between one or more poles and one or more throws.

FIG. **2** shows that the RF switch **100** of FIG. **1** can include an RF core and an energy management (EM) core.

FIG. **3** shows an example of the RF core implemented in an single-pole-double-throw (SPDT) configuration.

FIG. **4** shows an example of the RF core implemented in an SPDT configuration where each switch arm can include a plurality of field-effect transistors (FETs) connected in series.

FIG. **5** schematically shows that controlling of one or more FETs in an RF switch can be facilitated by a circuit configured to bias and/or couple one or more portions of the FETs.

FIG. **6** shows examples of the bias/coupling circuit implemented on different parts of a plurality of FETs in a switch arm.

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FIGS. **7**A and **7**B show plan and side sectional views of an example finger-based FET device implemented in a silicon-on-insulator (SOI) configuration.

FIGS. **8**A and **8**B show plan and side sectional views of an example of a multiple-finger FET device implemented in an SOI configuration.

FIG. **9** shows an example where an RF switching configuration can include one or more capacitors to, for example, inhibit a low-frequency blocker from mixing with a fundamental frequency.

FIG. **10** shows an example where the switching configuration of FIG. **9** is in a transmit mode.

FIGS. **11**A-**11**D show examples of how various components for biasing, coupling, and/or facilitating the example configurations of FIGS. **9**-**10** can be implemented.

FIGS. **12**A and **12**B show an example of a packaged module that can include one or more features described herein.

FIG. **13** shows that in some embodiments, one or more features of the present disclosure can be implemented in a switch device such as a single-pole-multi-throw (SPMT) switch configured to facilitate multi-band multi-mode wireless operation.

FIG. **14** shows an example of a wireless device that can include one or more features described herein.

DETAILED DESCRIPTION

The headings provided herein, if any, are for convenience only and do not necessarily affect the scope or meaning of the claimed invention.

Example Components of a Switching Device:

FIG. **1** schematically shows a radio-frequency (RF) switch **100** configured to switch one or more signals between one or more poles **102** and one or more throws **104**. In some embodiments, such a switch can be based on one or more field-effect transistors (FETs) such as silicon-on-insulator (SOI) FETs. When a particular pole is connected to a particular throw, such a path is commonly referred to as being closed or in an ON state. When a given path between a pole and a throw is not connected, such a path is commonly referred to as being open or in an OFF state.

FIG. **2** shows that in some implementations, the RF switch **100** of FIG. **1** can include an RF core **110** and an energy management (EM) core **112**. The RF core **110** can be configured to route RF signals between the first and second ports. In the example single-pole-double-throw (SPDT) configuration shown in FIG. **2**, such first and second ports can include a pole **102***a* and a first throw **104***a*, or the pole **102***a* and a second throw **104***b*.

In some embodiments, EM core **112** can be configured to supply, for example, voltage control signals to the RF core. The EM core **112** can be further configured to provide the RF switch **100** with logic decoding and/or power supply conditioning capabilities.

In some embodiments, the RF core **110** can include one or more poles and one or more throws to enable passage of RF signals between one or more inputs and one or more outputs of the switch **100**. For example, the RF core **110** can include a single-pole double-throw (SPDT or SP2T) configuration as shown in FIG. **2**.

In the example SPDT context, FIG. **3** shows a more detailed example configuration of an RF core **110**. The RF core **110** is shown to include a single pole **102***a* coupled to first and second throw nodes **104***a*, **104***b* via first and second transistors (e.g., FETs) **120***a*, **120***b*. The first throw node **104***a* is shown to be coupled to an RF ground via an FET **122***a* to provide shunting capability for the node **104***a*. Similarly, the second throw node **104***b* is shown to be coupled to the RF ground via an FET **122***b* to provide shunting capability for the node **104***b*.

In an example operation, when the RF core **110** is in a state where an RF signal is being passed between the pole **102***a* and the first throw **104***a*, the FET **120***a* between the pole **102***a* and the first throw node **104***a* can be in an ON state, and the FET **120***b* between the pole **102***a* and the second throw node **104***b* can be in an OFF state. For the shunt FETs **122***a*, **122***b*, the shunt FET **122***a* can be in an OFF state so that the RF signal is not shunted to ground as it travels from the pole **102***a* to the first throw node **104***a*. The shunt FET **122***b* associated with the second throw node **104***b* can be in an ON state so that any RF signals or noise arriving at the RF core **110** through the second throw node **104***b* is shunted to the ground so as to reduce undesirable interference effects to the pole-to-first-throw operation.

Although the foregoing example is described in the context of a single-pole-double-throw configuration, it will be understood that the RF core can be configured with other numbers of poles and throws. For example, there may be more than one poles, and the number of throws can be less than or greater than the example number of two.

In the example of FIG. **3**, the transistors between the pole **102***a* and the two throw nodes **104***a*, **104***b* are depicted as single transistors. In some implementations, such switching functionalities between the pole(s) and the throw(s) can be provided by switch arm segments, where each switch arm segment includes a plurality of transistors such as FETs.

An example RF core configuration **130** of an RF core having such switch arm segments is shown in FIG. **4**. In the example, the pole **102***a* and the first throw node **104***a* are shown to be coupled via a first switch arm segment **140***a*. Similarly, the pole **102***a* and the second throw node **104***b* are shown to be coupled via a second switch arm segment **140***b*. The first throw node **104***a* is shown to be capable of being shunted to an RF ground via a first shunt arm segment **142***a*. Similarly, the second throw node **104***b* is shown to be capable of being shunted to the RF ground via a second shunt arm segment **142***b*.

In an example operation, when the RF core **130** is in a state where an RF signal is being passed between the pole **102***a* and the first throw node **104***a*, all of the FETs in the first switch arm segment **140***a* can be in an ON state, and all of the FETs in the second switch arm segment **104***b* can be in an OFF state. The first shunt arm **142***a* for the first throw node **104***a* can have all of its FETs in an OFF state so that the RF signal is not shunted to ground as it travels from the pole **102***a* to the first throw node **104***a*. All of the FETs in the second shunt arm **142***b* associated with the second throw node **104***b* can be in an ON state so that any RF signals or noise arriving at the RF core **130** through the second throw node **104***b* is shunted to the ground so as to reduce undesirable interference effects to the pole-to-first-throw operation.

Again, although described in the context of an SP2T configuration, it will be understood that RF cores having other numbers of poles and throws can also be implemented.

In some implementations, a switch arm segment (e.g., **140***a*, **140***b*, **142***a*, **142***b*) can include one or more semiconductor transistors such as FETs. In some embodiments, an FET may be capable of being in a first state or a second state and can include a gate, a drain, a source, and a body (sometimes also referred to as a substrate. In some embodiments, an FET can include a metal-oxide-semiconductor field effect transistor (MOSFET). In some embodiments, one

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or more FETs can be connected in series forming a first end and a second end such that an RF signal can be routed between the first end and the second end when the FETs are in a first state (e.g., ON state).

At least some of the present disclosure relates to how an FET or a group of FETs can be controlled to provide switching functionalities in desirable manners. FIG. **5** schematically shows that in some implementations, such controlling of an FET **120** can be facilitated by a circuit **150** configured to bias and/or couple one or more portions of the FET **120**. In some embodiments, such a circuit **150** can include one or more circuits configured to bias and/or couple a gate of the FET **120**, bias and/or couple a body of the FET **120**, and/or couple a source/drain of the FET **120**.

Schematic examples of how such biasing and/or coupling of different parts of one or more FETs are described in reference to FIG. **6**. In FIG. **6**, a switch arm segment **140** (that can be, for example, one of the example switch arm segments **140***a*, **140***b*, **142***a*, **142***b* of the example of FIG. **4**) between nodes **144**, **146** is shown to include a plurality of FETs **120**. Operations of such FETs can be controlled and/or facilitated by a gate bias/coupling circuit **150***a*, and a body bias/coupling circuit **150***c*, and/or a source/drain coupling circuit **150***b*.

Gate Bias/Coupling Circuit

In the example shown in FIG. **6**, the gate of each of the FETs **120** can be connected to the gate bias/coupling circuit **150***a* to receive a gate bias signal and/or couple the gate to another part of the FET **120** or the switch arm **140**. In some implementations, designs or features of the gate bias/coupling circuit **150***a* can improve performance of the switch arm **140**. Such improvements in performance can include, but are not limited to, device insertion loss, isolation performance, power handling capability and/or switching device linearity.

Body Bias/Coupling Circuit

As shown in FIG. **6**, the body of each FET **120** can be connected to the body bias/coupling circuit **150***c* to receive a body bias signal and/or couple the body to another part of the FET **120** or the switch arm **140**. In some implementations, designs or features of the body bias/coupling circuit **150***c* can improve performance of the switch arm **140**. Such improvements in performance can include, but are not limited to, device insertion loss, isolation performance, power handling capability and/or switching device linearity.

Source/Drain Coupling Circuit

As shown in FIG. **6**, the source/drain of each FET **120** can be connected to the coupling circuit **150***b* to couple the source/drain to another part of the FET **120** or the switch arm **140**. In some implementations, designs or features of the coupling circuit **150***b* can improve performance of the switch arm **140**. Such improvements in performance can include, but are not limited to, device insertion loss, isolation performance, power handling capability and/or switching device linearity.

Examples of Switching Performance Parameters:

Insertion Loss

A switching device performance parameter can include a measure of insertion loss. A switching device insertion loss can be a measure of the attenuation of an RF signal that is routed through the RF switching device. For example, the magnitude of an RF signal at an output port of a switching device can be less than the magnitude of the RF signal at an input port of the switching device. In some embodiments, a switching device can include device components that introduce parasitic capacitance, inductance, resistance, or conductance into the device, contributing to increased switching device insertion loss. In some embodiments, a switching device insertion loss can be measured as a ratio of the power or voltage of an RF signal at an input port to the power or voltage of the RF signal at an output port of the switching device. Decreased switching device insertion loss can be desirable to enable improved RF signal transmission.

Isolation

A switching device performance parameter can also include a measure of isolation. Switching device isolation can be a measure of the RF isolation between an input port and an output port an RF switching device. In some embodiments, it can be a measure of the RF isolation of a switching device while the switching device is in a state where an input port and an output port are electrically isolated, for example while the switching device is in an OFF state. Increased switching device isolation can improve RF signal integrity. In certain embodiments, an increase in isolation can improve wireless communication device performance.

Intermodulation Distortion

A switching device performance parameter can further include a measure of intermodulation distortion (IMD) performance. Intermodulation distortion (IMD) can be a measure of non-linearity in an RF switching device.

IMD can result from two or more signals mixing together and yielding frequencies that are not harmonic frequencies. For example, suppose that two signals have fundamental frequencies f_1 and f_2 ($f_2>f_1$) that are relatively close to each other in frequency space. Mixing of such signals can result in peaks in frequency spectrum at frequencies corresponding to different products of fundamental and harmonic frequencies of the two signals. For example, a second-order intermodulation distortion (also referred to as IMD2) is typically considered to include frequencies f_1+_2 f_2-f_1, $2f_1$, and $2f_2$. A third-order IMD (also referred to as IMD3) is typically considered to include $2f_1+f_2$, $2f_1-f_2$, f_1+2f_2, f_1-2f_2. Higher order products can be formed in similar manners.

In general, as the IMD order number increases, power levels decrease. Accordingly, second and third orders can be undesirable effects that are of particular interest. Higher orders such as fourth and fifth orders can also be of interest in some situations.

In some RF applications, it can be desirable to reduce susceptibility to interference within an RF system. Non linearity in RF systems can result in introduction of spurious signals into the system. Spurious signals in the RF system can result in interference within the system and degrade the information transmitted by RF signals. An RF system having increased non-linearity can demonstrate increased susceptibility to interference. Non-linearity in system components, for example switching devices, can contribute to the introduction of spurious signals into the RF system, thereby contributing to degradation of overall RF system linearity and IMD performance.

In some embodiments, RF switching devices can be implemented as part of an RF system including a wireless communication system. IMD performance of the system can be improved by increasing linearity of system components, such as linearity of an RF switching device. In some embodiments, a wireless communication system can operate in a multi-band and/or multi-mode environment. Improvement in intermodulation distortion (IMD) performance can be desirable in wireless communication systems operating in a multi-band and/or multi-mode environment. In some embodiments, improvement of a switching device IMD performance can improve the IMD performance of a wireless communication system operating in a multi-mode and/or multi-band environment.

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Improved switching device IMD performance can be desirable for wireless communication devices operating in various wireless communication standards, for example for wireless communication devices operating in the LTE communication standard. In some RF applications, it can be desirable to improve linearity of switching devices operating in wireless communication devices that enable simultaneous transmission of data and voice communication. For example, improved IMD performance in switching devices can be desirable for wireless communication devices operating in the LTE communication standard and performing simultaneous transmission of voice and data communication (e.g., SVLTE).

High Power Handling Capability

In some RF applications, it can be desirable for RF switching devices to operate under high power while reducing degradation of other device performance parameters. In some embodiments, it can be desirable for RF switching devices to operate under high power with improved intermodulation distortion, insertion loss, and/or isolation performance.

In some embodiments, an increased number of transistors can be implemented in a switch arm segment of a switching device to enable improved power handling capability of the switching device. For example, a switch arm segment can include an increased number of FETs connected in series, an increased FET stack height, to enable improved device performance under high power. However, in some embodiments, increased FET stack height can degrade the switching device insertion loss performance.

Examples of FET Structures and Fabrication Process Technologies:

A switching device can be implemented on-die, off-die, or some combination thereon. A switching device can also be fabricated using various technologies. In some embodiments, RF switching devices can be fabricated with silicon or silicon-on-insulator (SOI) technology.

As described herein, an RF switching device can be implemented using silicon-on-insulator (SOI) technology. In some embodiments, SOI technology can include a semiconductor substrate having an embedded layer of electrically insulating material, such as a buried oxide layer beneath a silicon device layer. For example, an SOI substrate can include an oxide layer embedded below a silicon layer. Other insulating materials known in the art can also be used.

Implementation of RF applications, such as an RF switching device, using SOI technology can improve switching device performance. In some embodiments, SOI technology can enable reduced power consumption. Reduced power consumption can be desirable in RF applications, including those associated with wireless communication devices. SOI technology can enable reduced power consumption of device circuitry due to decreased parasitic capacitance of transistors and interconnect metallization to a silicon substrate. Presence of a buried oxide layer can also reduce junction capacitance or use of high resistivity substrate, enabling reduced substrate related RF losses. Electrically isolated SOI transistors can facilitate stacking, contributing to decreased chip size.

In some SOI FET configurations, each transistor can be configured as a finger-based device where the source and drain are rectangular shaped (in a plan view) and a gate structure extends between the source and drain like a rectangular shaped finger. FIGS. **7**A and **7**B show plan and side sectional views of an example finger-based FET device implemented on SOI. As shown, FET devices described herein can include a p-type FET or an n-type FET. Thus, although some FET devices are described herein as p-type devices, it will be understood that various concepts associated with such p-type devices can also apply to n-type devices.

As shown in FIGS. **7**A and **7**B, a pMOSFET can include an insulator layer formed on a semiconductor substrate. The insulator layer can be formed from materials such as silicon dioxide or sapphire. An n-well is shown to be formed in the insulator such that the exposed surface generally defines a rectangular region. Source (S) and drain (D) are shown to be p-doped regions whose exposed surfaces generally define rectangles. As shown, S/D regions can be configured so that source and drain functionalities are reversed.

FIGS. **7**A and **7**B further show that a gate (G) can be formed on the n-well so as to be positioned between the source and the drain. The example gate is depicted as having a rectangular shape that extends along with the source and the drain. Also shown is an n-type body contact. Formations of the rectangular shaped well, source and drain regions, and the body contact can be achieved by a number of known techniques. In some embodiments, the source and drain regions can be formed adjacent to the ends of their respective upper insulator layers, and the junctions between the body and the source/drain regions on the opposing sides of the body can extend substantially all the way down to the top of the buried insulator layer. Such a configuration can provide, for example, reduced source/drain junction capacitance. To form a body contact for such a configuration, an additional gate region can be provided on the side so as to allow, for example, an isolated P+ region to contact the Pwell.

FIGS. **8**A and **8**B show plan and side sectional views of an example of a multiple-finger FET device implemented on SOI. Formations of rectangular shaped n-well, rectangular shaped p-doped regions, rectangular shaped gates, and n-type body contact can be achieved in manners similar to those described in reference to FIGS. **7**A and **7**B.

The example multiple-finger FET device of FIGS. **8**A and **8**B can be made to operate such that a drain of one FET acts as a source of its neighboring FET. Thus, the multiple-finger FET device as a whole can provide a voltage-dividing functionality. For example, an RF signal can be provided at one of the outermost p-doped regions (e.g., the leftmost p-doped region); and as the signal passes through the series of FETs, the signal's voltage can be divided among the FETs. In such an example, the rightmost p-doped region can act as an overall drain of the multi-finger FET device.

In some implementations, a plurality of the foregoing multi-finger FET devices can be connected in series as a switch to, for example, further facilitate the voltage-dividing functionality. A number of such multi-finger FET devices can be selected based on, for example, power handling requirement of the switch.

Examples of Bias and/or Coupling Configurations for Improved Performance:

Described herein are various examples of how FET-based switch circuits can be biased and/or coupled to yield one or more performance improvements. In some embodiments, such biasing/coupling configurations can be implemented in SOI FET-based switch circuits. It will be understood that some of the example biasing/coupling configurations can be combined to yield a combination of desirable features that may not be available to the individual configurations. It will also be understood that, although described in the context of RF switching applications, one or more features described herein can also be applied to other circuits and devices that utilize FETs such as SOI FETs.

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Example Configurations

Intermodulation distortion (IMD) measures an unwanted signal added to a desired signal due to mixing products from other RF signals. Such an effect can be particularly dominant in a multi-mode, multi-band environment. IMD can the result from two or more signals mixing together to yield frequencies that are not harmonic frequencies.

System designers typically strive to reduce interference susceptibility through, for example, improved linearity. A given system's linearity can govern how much IMD will occur within it, which in turn can create interferences. Through improved linearity of the system building blocks, such as an RF switch, the overall susceptibility of a system to interference can be decreased.

Performance features such as a lower IMD in RF switches can be an important factor in wireless-device designs. For example Long Term Evolution (LTE) systems can benefit significantly from RF switches having reduced IMDs. As a more specific example, system designs for simultaneous voice and data on LTE (SVLTE) can benefit significantly from RF switches having ultra-low levels of IMDs.

FIG. **9** shows a switching configuration **250** in an example context of a single-pole-dual-throw (SPDT) application. The single pole is shown to be connected to an antenna **252**. One of the two throws is shown to be coupled to a receive (Rx) port via a switch circuit S. The Rx port can be coupled to a ground via a shunt switch circuit.

Similarly, the other throw is shown to be coupled to a transmit (Tx) port via a switch circuit S. The Tx port can be coupled to the ground via a shunt switch circuit.

In some embodiments, each of the switch circuits ("S" and "Shunt") can include one or more FETs such as SOI FETs. A single FET is sometimes referred to herein with a reference numeral **120** or **122**, and a stack of such FETs is sometimes referred to herein with a reference numeral **140** or **142**. In some embodiments, the "S" and "Shunt" switches can include one or more features described herein to provide various advantageous functionalities.

The switching configuration of FIG. **9** is shown to include capacitors to inhibit a low-frequency blocker from mixing with a fundamental frequency. For example, a capacitor C**1** is provided between the antenna node and the switch arm S of the Tx throw. Similarly, a capacitor C**2** is provided between the antenna node and the switch arm S of the Rx throw. For the shunt arms, a capacitor C**3** is provided between the Tx node and its shunt switch arm. Similarly, a capacitor C**4** is provided between the Rx node and its shunt switch arm. In some embodiments, a shunt arm may or may not be provided for the Rx node. With the foregoing capacitors, a low-frequency jammer signal can be blocked or reduced from mixing with any ON or OFF paths. This can lead to improvement in IMD performance, especially for low-frequency blocker signals.

FIG. **10** shows an example operating configuration where some of the foregoing capacitors can provide desirable switching functionalities. In the example, the switching configuration is in a transmit mode. Accordingly, the transmit switch arm is ON (closed), and the receive switch arm is OFF (open). The shunt arm for the Tx node is OFF (open).

In some embodiments, capacitors C**1**-C**4** described in reference to FIGS. **9** and **10** can be implemented on the same die as their respective switch circuits, off of the die, or any combination thereof.

In some implementations, and as described herein, the foregoing example configurations described in reference to FIGS. **9** and **10** can be relatively simpler and easier to implement, and can yield a number of improvements. For example, this technique can provide improved IMD performance by preventing a low-frequency blocker signal from mixing with a fundamental frequency signal.

Examples of Implementations in Products:

Various examples of FET-based switch circuits and bias/coupling configurations described herein can be implemented in a number of different ways and at different product levels. Some of such product implementations are described by way of examples.

Semiconductor Die Implementation

FIGS. **11**A-**11**D schematically show non-limiting examples of such implementations on one or more semiconductor die. FIG. **11**A shows that in some embodiments, a switch circuit **120** and a bias/coupling circuit **150** having one or more features as described herein can be implemented on a die **800**. FIG. **11**B shows that in some embodiments, at least some of the bias/coupling circuit **150** can be implemented outside of the die **800** of FIG. **11**A.

FIG. **11**C shows that in some embodiments, a switch circuit **120** having one or more features as described herein can be implemented on a first die **800***a*, and a bias/coupling circuit **150** having one or more features as described herein can be implemented on a second die **800***b*. FIG. **11**D shows that in some embodiments, at least some of the bias/coupling circuit **150** can be implemented outside of the first die **800***a* of FIG. **11**C.

Packaged Module Implementation

In some embodiments, one or more die having one or more features described herein can be implemented in a packaged module. An example of such a module is shown in FIGS. **12**A (plan view) and **12**B (side view). Although described in the context of both of the switch circuit and the bias/coupling circuit being on the same die (e.g., example configuration of FIG. **11**A), it will be understood that packaged modules can be based on other configurations.

A module **810** is shown to include a packaging substrate **812**. Such a packaging substrate can be configured to receive a plurality of components, and can include, for example, a laminate substrate. The components mounted on the packaging substrate **812** can include one or more dies. In the example shown, a die **800** having a switching circuit **120** and a bias/coupling circuit **150** is shown to be mounted on the packaging substrate **812**. The die **800** can be electrically connected to other parts of the module (and with each other where more than one die is utilized) through connections such as connection-wirebonds **816**. Such connection-wirebonds can be formed between contact pads **818** formed on the die **800** and contact pads **814** formed on the packaging substrate **812**. In some embodiments, one or more surface mounted devices (SMDs) **822** can be mounted on the packaging substrate **812** to facilitate various functionalities of the module **810**.

In some embodiments, the packaging substrate **812** can include electrical connection paths for interconnecting the various components with each other and/or with contact pads for external connections. For example, a connection path **832** is depicted as interconnecting the example SMD **822** and the die **800**. In another example, a connection path **832** is depicted as interconnecting the SMD **822** with an external-connection contact pad **834**. In yet another example a connection path **832** is depicted as interconnecting the die **800** with ground-connection contact pads **836**.

In some embodiments, a space above the packaging substrate **812** and the various components mounted thereon can be filled with an overmold structure **830**. Such an overmold structure can provide a number of desirable func-

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tionalities, including protection for the components and wirebonds from external elements, and easier handling of the packaged module **810**.

FIG. **13** shows a schematic diagram of an example switching configuration that can be implemented in the module **810** described in reference to FIGS. **12**A and **12**B. In the example, the switch circuit **120** is depicted as being an SP9T switch, with the pole being connectable to an antenna and the throws being connectable to various Rx and Tx paths. Such a configuration can facilitate, for example, multi-mode multi-band operations in wireless devices.

The module **810** can further include an interface for receiving power (e.g., supply voltage VDD) and control signals to facilitate operation of the switch circuit **120** and/or the bias/coupling circuit **150**. In some implementations, supply voltage and control signals can be applied to the switch circuit **120** via the bias/coupling circuit **150**.

Wireless Device Implementation

In some implementations, a device and/or a circuit having one or more features described herein can be included in an RF device such as a wireless device. Such a device and/or a circuit can be implemented directly in the wireless device, in a modular form as described herein, or in some combination thereof. In some embodiments, such a wireless device can include, for example, a cellular phone, a smart-phone, a hand-held wireless device with or without phone functionality, a wireless tablet, etc.

FIG. **14** schematically depicts an example wireless device **900** having one or more advantageous features described herein. In the context of various switches and various biasing/coupling configurations as described herein, a switch **120** and a bias/coupling circuit **150** can be part of a module **810**. In some embodiments, such a switch module can facilitate, for example, multi-band multip-mode operation of the wireless device **900**.

In the example wireless device **900**, a power amplifier (PA) module **916** having a plurality of PAs can provide an amplified RF signal to the switch **120** (via a duplexer **920**), and the switch **120** can route the amplified RF signal to an antenna. The PA module **916** can receive an unamplified RF signal from a transceiver **914** that can be configured and operated in known manners. The transceiver can also be configured to process received signals. The transceiver **914** is shown to interact with a baseband sub-system **910** that is configured to provide conversion between data and/or voice signals suitable for a user and RF signals suitable for the transceiver **914**. The transceiver **914** is also shown to be connected to a power management component **906** that is configured to manage power for the operation of the wireless device **900**. Such a power management component can also control operations of the baseband sub-system **910** and the module **810**.

The baseband sub-system **910** is shown to be connected to a user interface **902** to facilitate various input and output of voice and/or data provided to and received from the user. The baseband sub-system **910** can also be connected to a memory **904** that is configured to store data and/or instructions to facilitate the operation of the wireless device, and/or to provide storage of information for the user.

In some embodiments, the duplexer **920** can allow transmit and receive operations to be performed simultaneously using a common antenna (e.g., **924**). In FIG. **14**, received signals are shown to be routed to "Rx" paths (not shown) that can include, for example, a low-noise amplifier (LNA).

A number of other wireless device configurations can utilize one or more features described herein. For example, a wireless device does not need to be a multi-band device. In another example, a wireless device can include additional antennas such as diversity antenna, and additional connectivity features such as Wi-Fi, Bluetooth, and GPS.

General Comments:

Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not limited to." The word "coupled", as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words "herein," "above," "below," and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word "or" in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

The above detailed description of embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise form disclosed above. While specific embodiments of, and examples for, the invention are described above for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. For example, while processes or blocks are presented in a given order, alternative embodiments may perform routines having steps, or employ systems having blocks, in a different order, and some processes or blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these processes or blocks may be implemented in a variety of different ways. Also, while processes or blocks are at times shown as being performed in series, these processes or blocks may instead be performed in parallel, or may be performed at different times.

The teachings of the invention provided herein can be applied to other systems, not necessarily the system described above. The elements and acts of the various embodiments described above can be combined to provide further embodiments.

While certain embodiments of the inventions have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

What is claimed is:

1. A semiconductor die comprising:

a semiconductor substrate;

a first switch circuit formed on the semiconductor substrate connected between an antenna node and a transmit node;

a second switch circuit formed on the semiconductor substrate and connected between the antenna node and a receive node;

a first capacitor formed on the semiconductor substrate and connected in series with the first switch circuit between the first switch circuit and the antenna node;

a second capacitor formed on the semiconductor substrate and connected in series with the second switch circuit between the second switch circuit and the antenna node; and

a first shunt arm formed on the semiconductor substrate and connected to the first switch circuit and the transmit node, the first shunt arm including a third switch circuit connected to ground.

2. The semiconductor die of claim **1** further comprising an insulator layer disposed between the first and second switch circuits and the semiconductor substrate.

3. The semiconductor die of claim **2** wherein the semiconductor die is a silicon-on-insulator (SOI) die.

4. The semiconductor die of claim **1** wherein the first shunt arm includes a third capacitor connected in series with the first switch circuit between the first switch circuit and the transmit node.

5. The semiconductor die of claim **4** further comprising a second shunt arm connected to the second switch circuit and the receive node, the second shunt arm including a fourth switch circuit connected to ground.

6. The semiconductor die of claim **5** wherein the second shunt arm includes a fourth capacitor connected in series with the second switch circuit between the second switch circuit and the receive node.

7. A method for operating a radio-frequency (RF) device, the method comprising:

providing an RF device including a first switch circuit connected between an antenna node and a transmit node, a second switch circuit connected between the antenna node and a receiver node, a first capacitor connected in series with the first switch circuity between the first switch circuit and the antenna node, a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node, and a first shunt arm connected to the first switch circuit and the transmit node, the first shunt arm including a third switch circuit connected to ground;

controlling an RF switch of the RF device by placing the first switch circuit in an ON state and placing the third switch circuit in an OFF state; and

inhibiting a low-frequency blocker signal from mixing with a fundamental-frequency signal in the RF switch using the first capacitor.

8. The method of claim **7** wherein the first switch circuit is formed on an insulator layer disposed between the first switch circuit and a semiconductor substrate.

9. The method of claim **7** wherein the RF switch is a silicon-on-insulator (SOI) switch.

10. The method of claim **7** wherein the first shunt arm includes a third capacitor connected in series with the first switch circuit between the first switch circuit and the transmit node.

11. The method of claim **10** wherein the RF device further includes a second shunt arm connected to the second switch circuit and the receive node, the second shunt arm including a fourth switch circuit connected to ground.

12. The method of claim **11** wherein the second shunt arm includes a fourth capacitor connected in series with the second switch circuit between the second switch circuit and the receive node.

13. A wireless device comprising:

a transceiver configured to process RF signals;

an antenna in communication with the transceiver; and

a switch module interconnected to the antenna and the transceiver and configured to selectively route RF signals to and from the antenna, the switch module including a first switch connected between the antenna and a transmit node, a second switch connected between the antenna and a receive node, a first capacitor connected in series with the first switch between the first switch and the antenna, a second capacitor connected in series with the second switch between the second switch and the antenna, and a first shunt arm connected to the first switch and the transmit node, the first shunt arm including a third switch connected to ground.

14. The wireless device of claim **13** wherein the first switch is formed on a silicon-on-insulator (SOI) die of the wireless device.

15. The wireless device of claim **13** wherein the first capacitor is part of the same semiconductor die as the first switch.

16. The wireless device of claim **13** wherein the first shunt arm includes a third capacitor connected in series with the first switch between the first switch and the transmit node.

17. The wireless device of claim **16** wherein the switch module further includes a second shunt arm connected to the second switch and the receive node, the second shunt arm including a fourth switch connected to ground.

18. The wireless device of claim **17** wherein the second shunt arm includes a fourth capacitor connected in series with the second switch between the second switch and the receive node.

* * * * *

EXHIBIT 9

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United States Patent and Trademark Office

March 21, 2024

THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM THE RECORDS OF THIS OFFICE OF:

PATENT NUMBER: *9,148,194*
ISSUE DATE: *September 29, 2015*

By Authority of the
Under Secretary of Commerce for Intellectual Property
and Director of the United States Patent and Trademark Office

John Burson
Certifying Officer



(12) **United States Patent**
Madan et al.

(10) **Patent No.: US 9,148,194 B2**
(45) **Date of Patent: Sep. 29, 2015**

(54) **RADIO-FREQUENCY SWITCH SYSTEM HAVING IMPROVED INTERMODULATION DISTORTION PERFORMANCE**

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(72) Inventors: **Anuj Madan**, Cambridge, MA (US); **Fikret Altunkilic**, North Andover, MA (US); **Guillaume Alexandre Blin**, Carlisle, MA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 74 days.

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H04B 1/48	(2006.01)
H03K 17/693	(2006.01)
H01L 21/84	(2006.01)
H01L 27/06	(2006.01)
H01L 27/12	(2006.01)

(52) **U.S. Cl.**

CPC ***H04B 1/44*** (2013.01); ***H01L 21/84*** (2013.01); ***H01L 27/0629*** (2013.01); ***H01L 27/1203*** (2013.01); ***H03K 17/693*** (2013.01); ***H04B 1/48*** (2013.01); *H03K 2217/0018* (2013.01); *H03K 2217/0054* (2013.01)

(58) **Field of Classification Search**

CPC H04B 1/44
USPC 455/78, 87, 252.1, 296; 438/178, 197, 438/381; 327/427, 434, 436, 437

See application file for complete search history.

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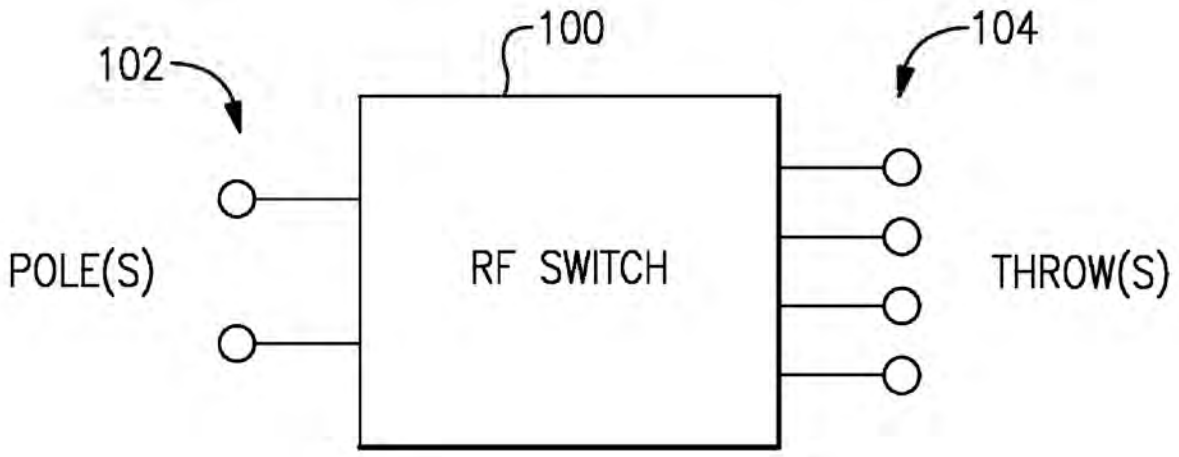
Primary Examiner — Tuan H Nguyen

(74) *Attorney, Agent, or Firm* — Fernando Hale & Chang LLP

(57) **ABSTRACT**

Radio-frequency (RF) switch circuits are disclosed providing improved switching performance. An RF switch system includes a switch having a stack of field-effect transistors (FETs) connected in series between first and second nodes. A capacitor connected in series with the switch is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

11 Claims, 9 Drawing Sheets



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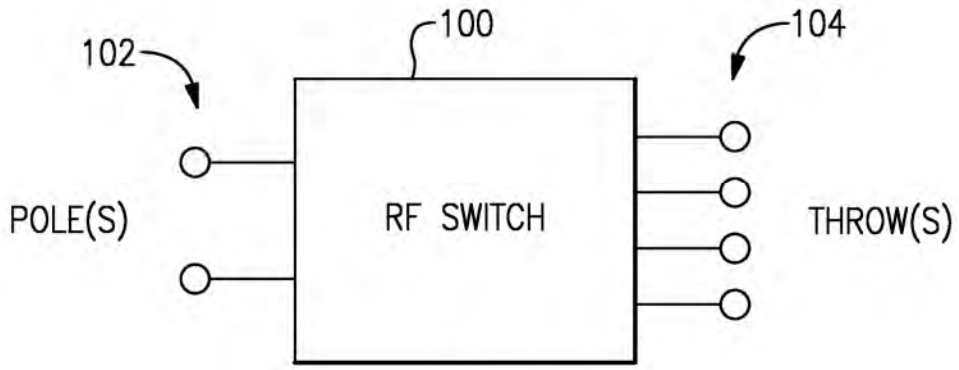


FIG.1

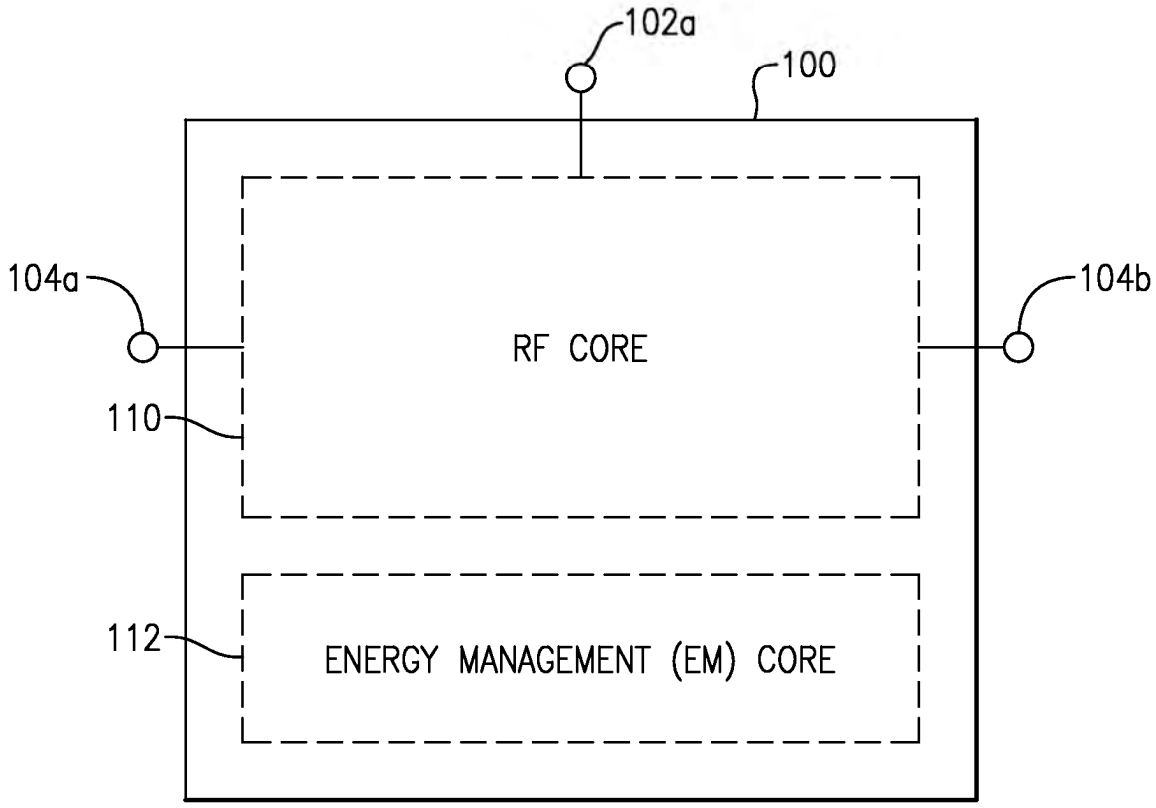


FIG.2

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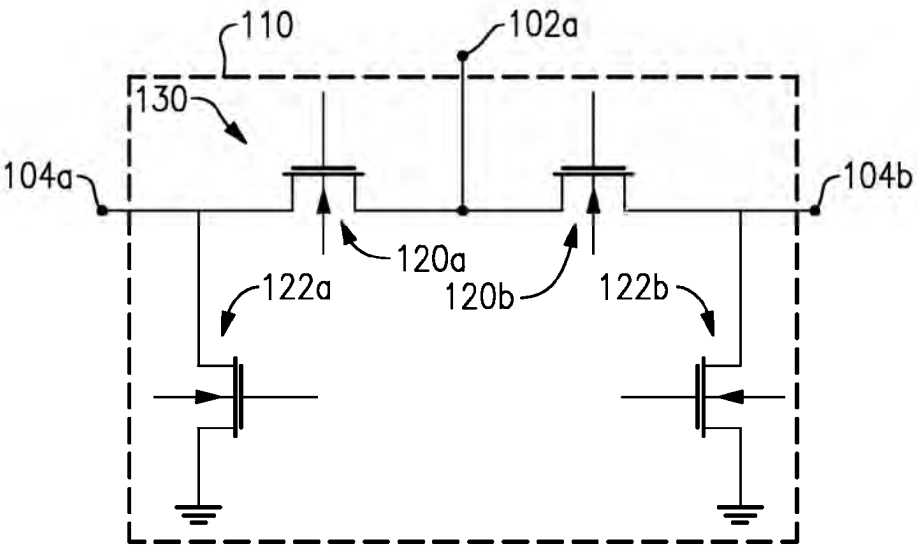


FIG.3

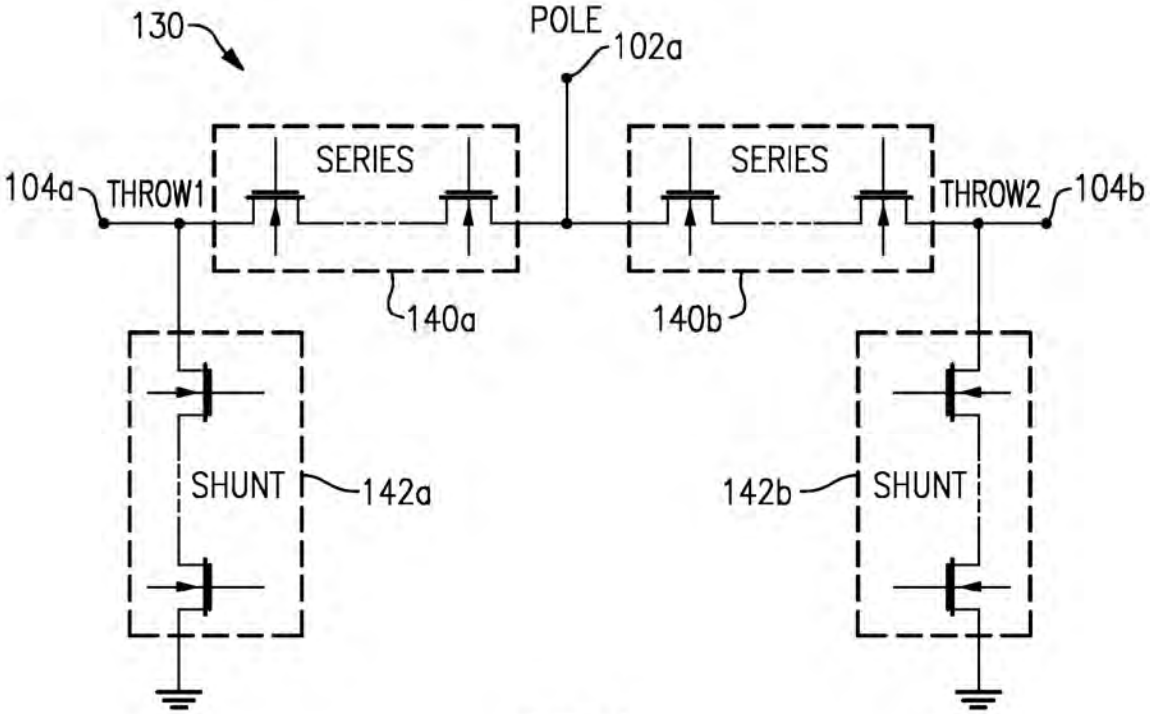


FIG.4

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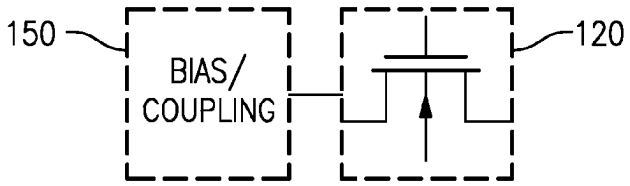


FIG.5

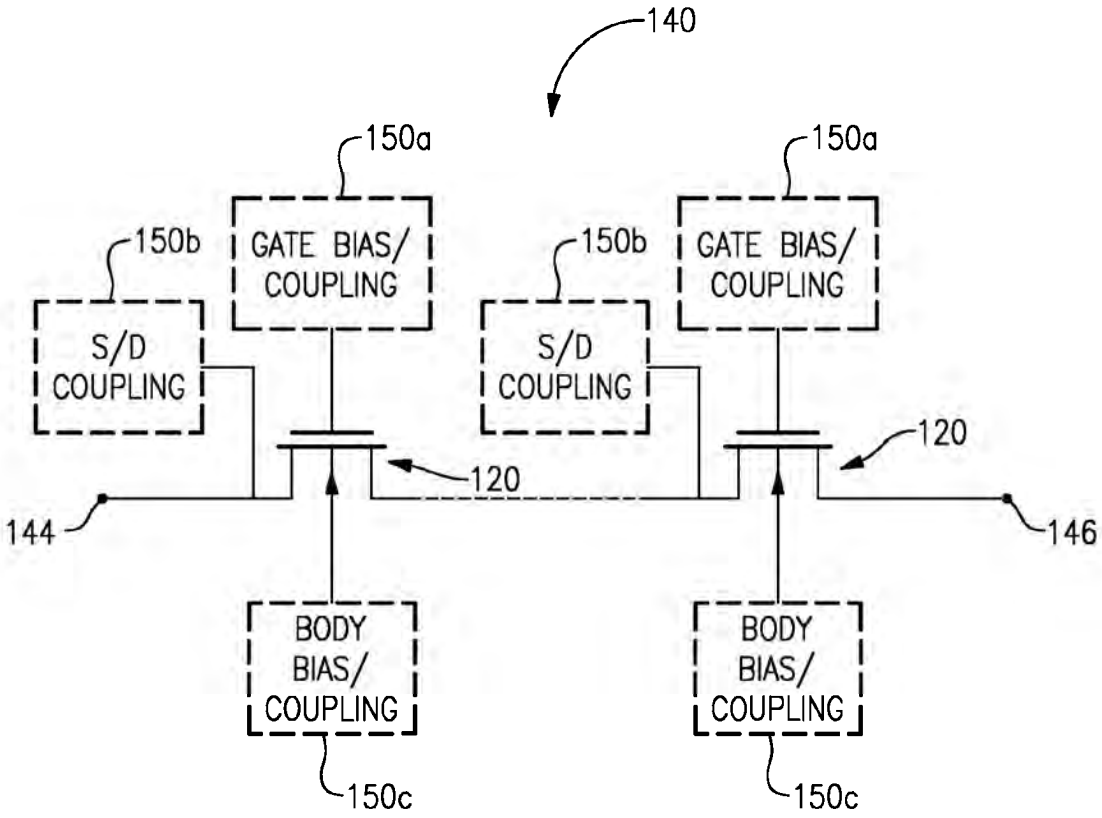


FIG.6

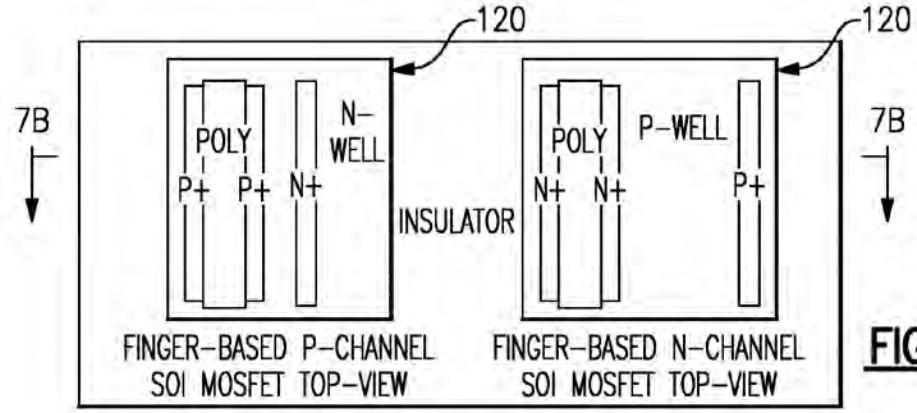


FIG.7A

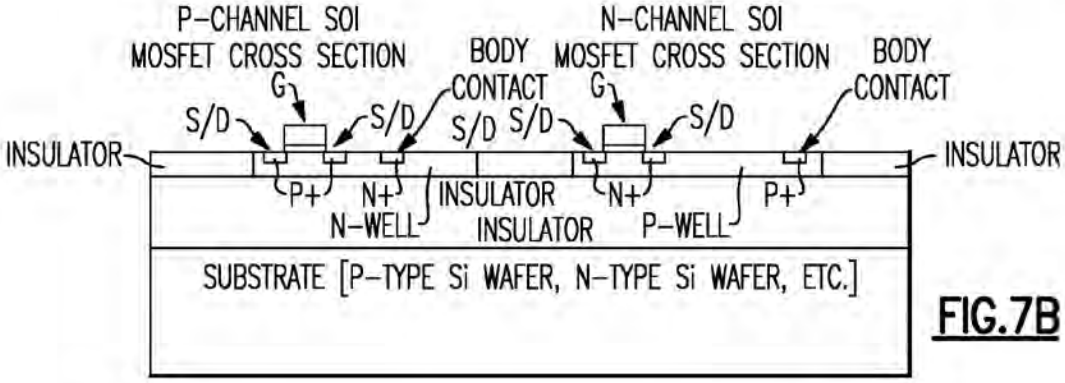


FIG.7B

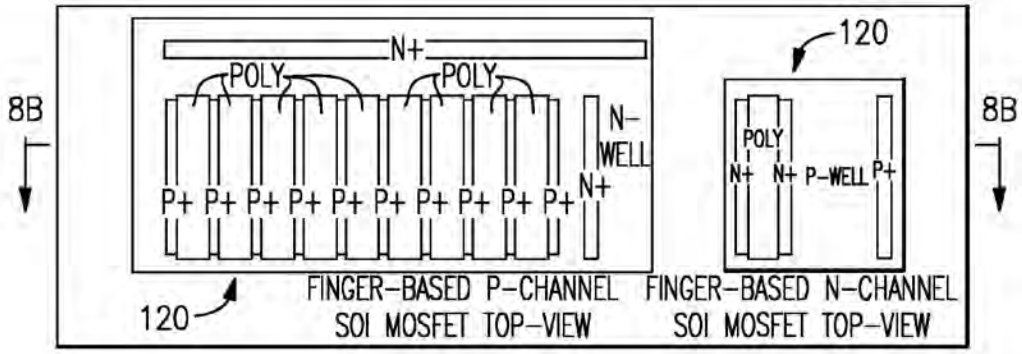


FIG.8A

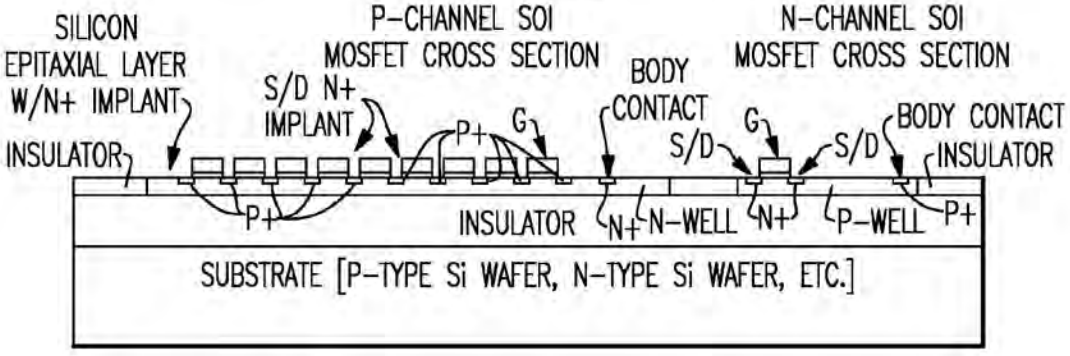


FIG.8B

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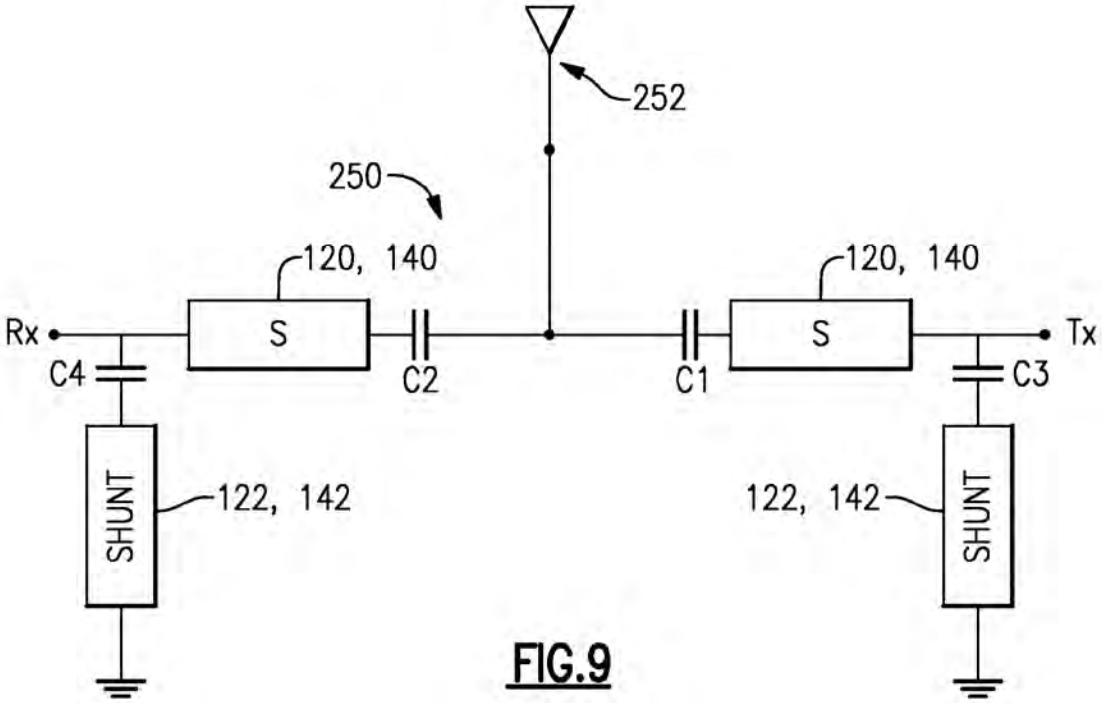


FIG.9

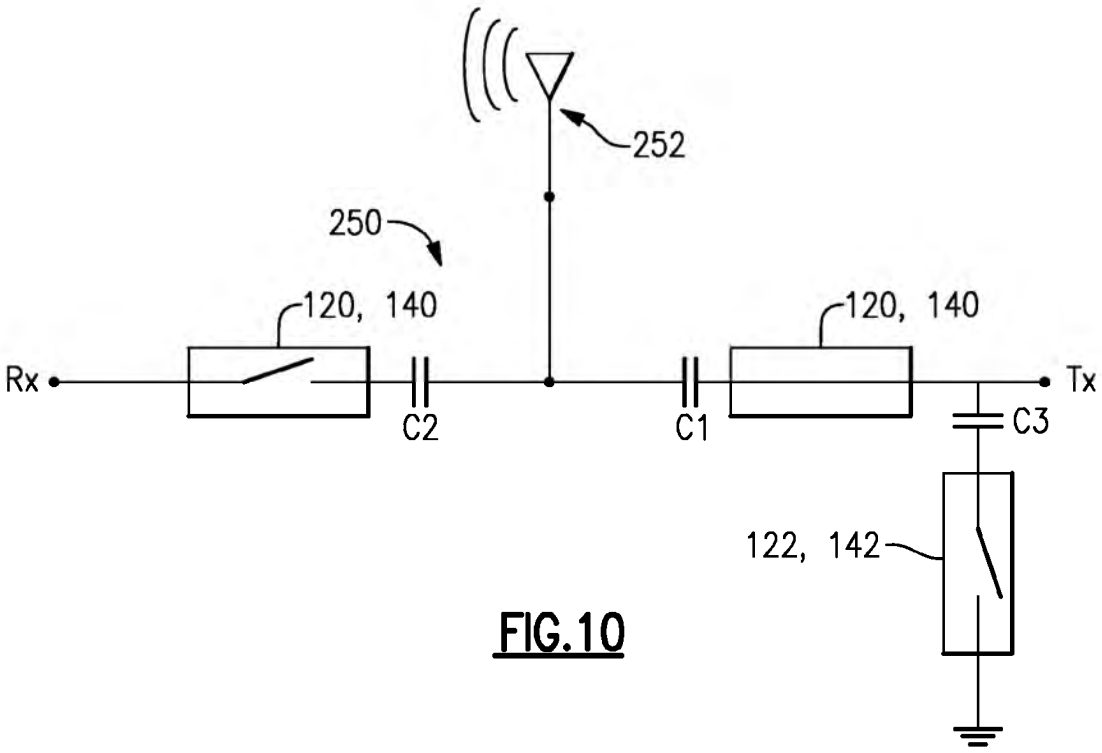


FIG.10

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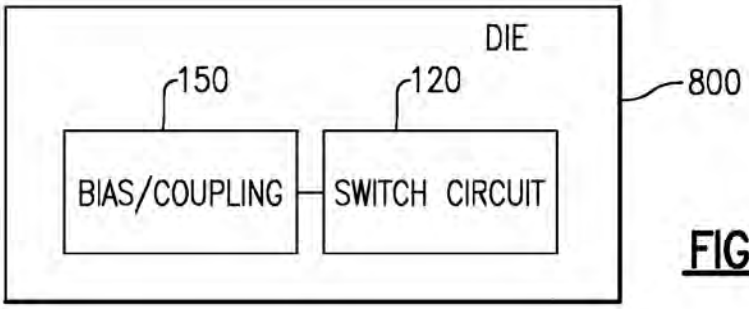


FIG.11A

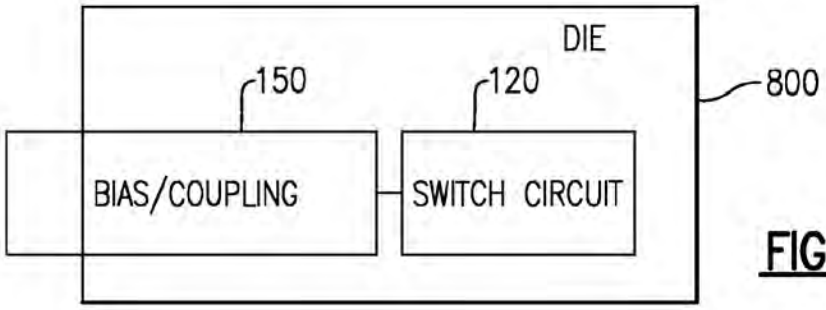


FIG.11B

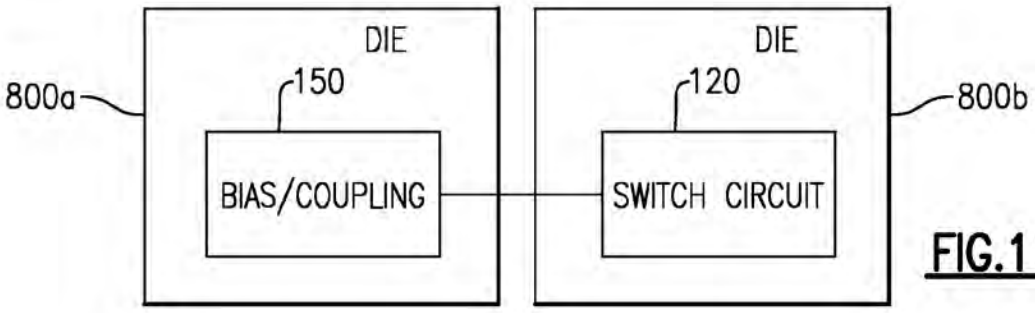


FIG.11C

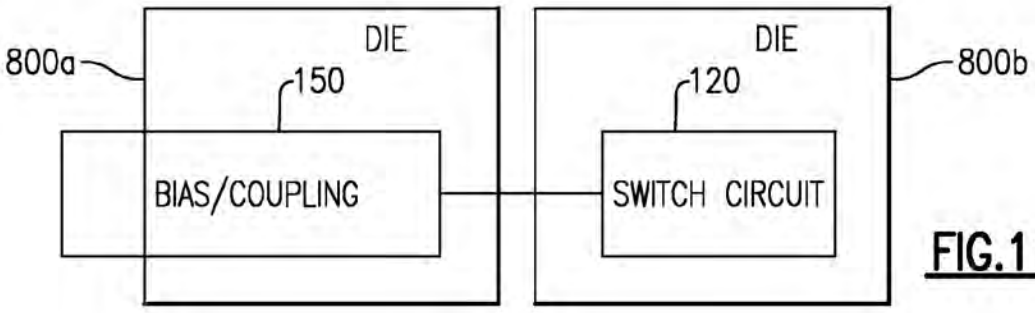


FIG.11D

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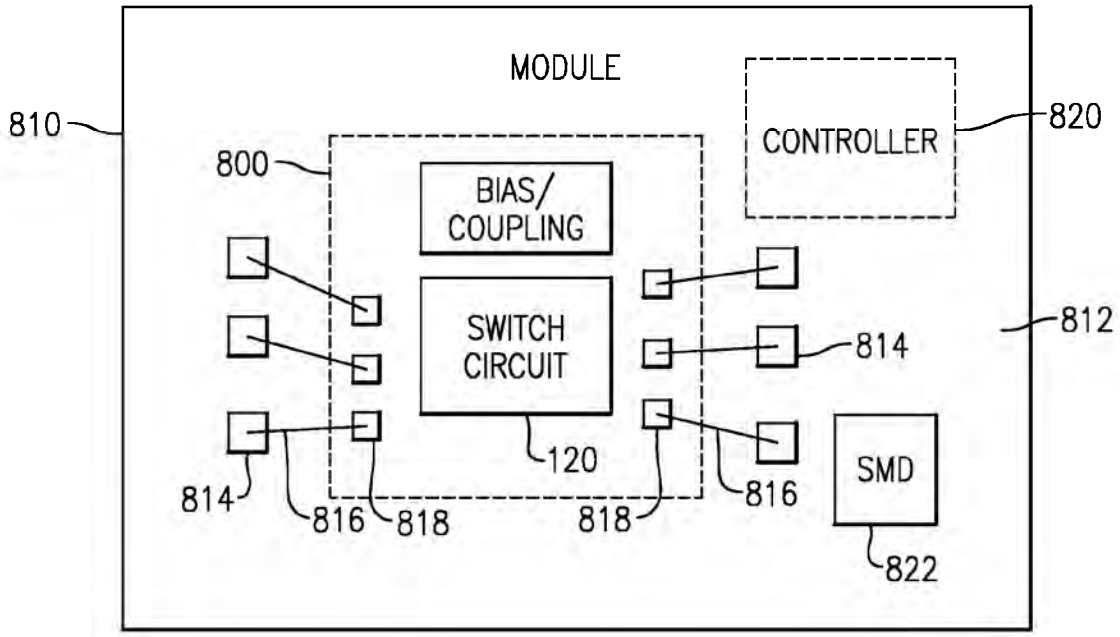


FIG.12A

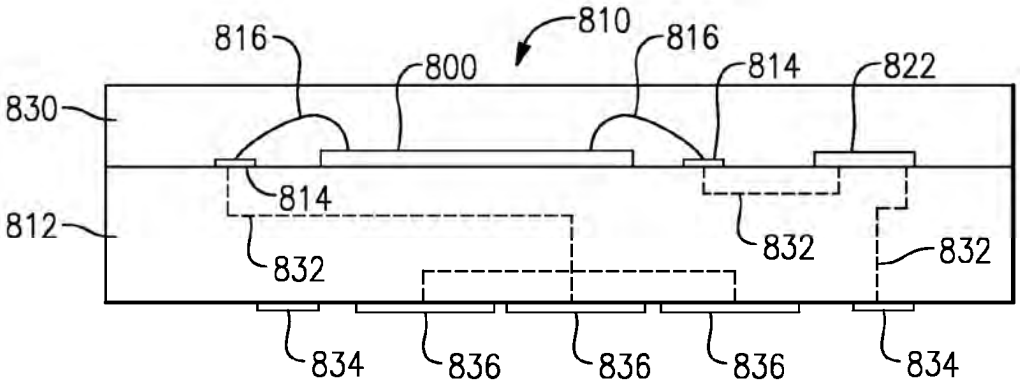


FIG.12B

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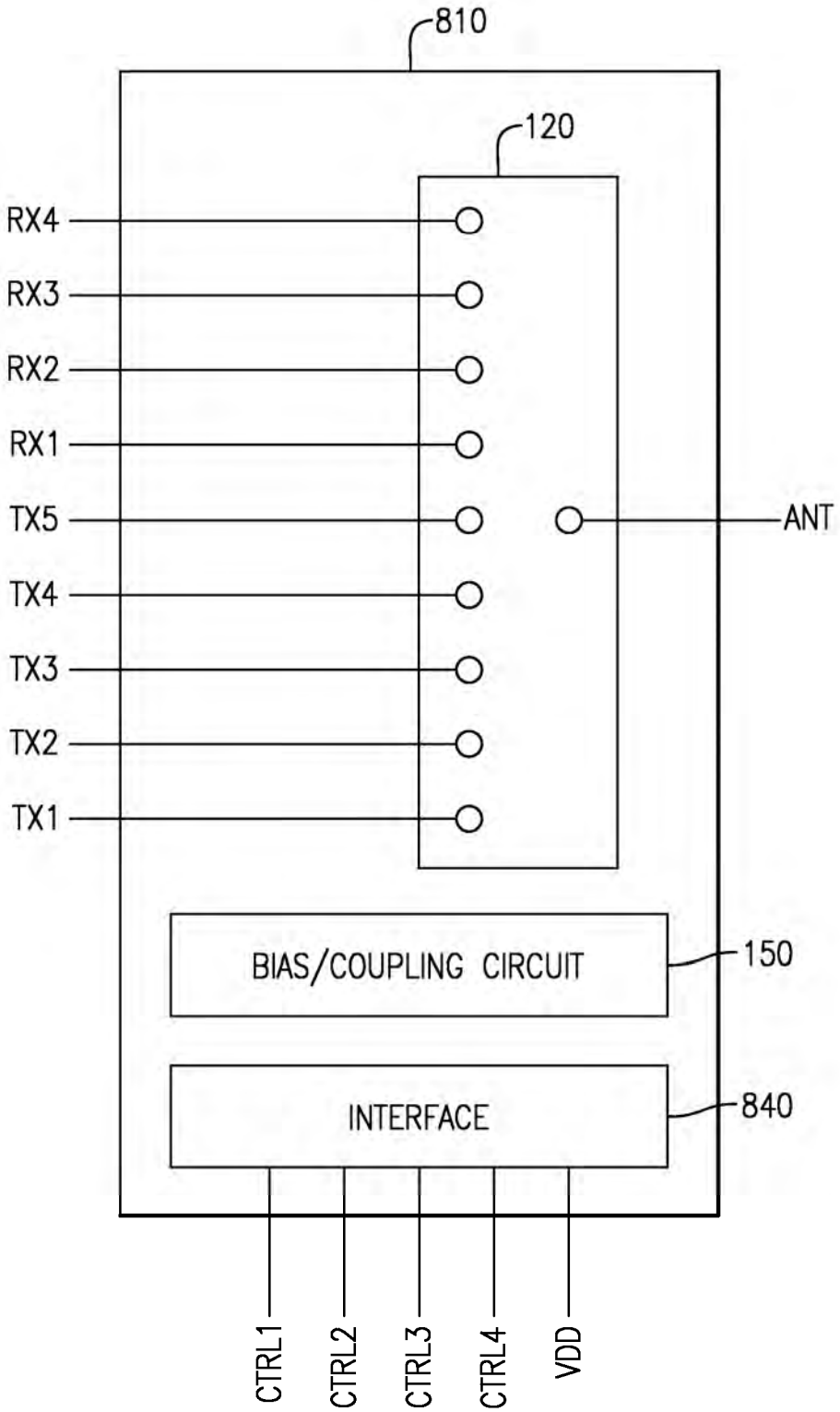


FIG.13

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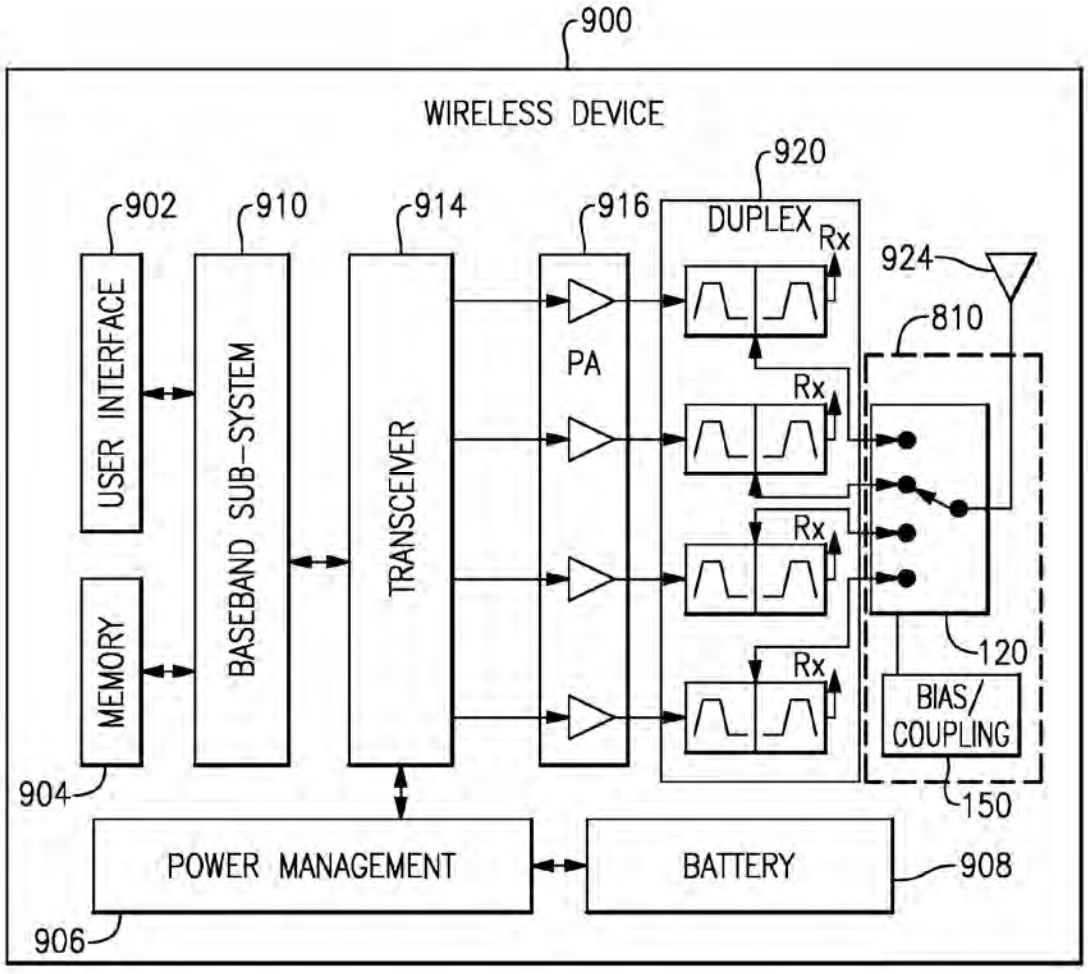


FIG. 14

RADIO-FREQUENCY SWITCH SYSTEM HAVING IMPROVED INTERMODULATION DISTORTION PERFORMANCE

RELATED APPLICATION

This application claims the benefit of priority under 35 U.S.C. §119(e) of U.S. Provisional Application No. 61/669,045, filed on Jul. 7, 2012, and entitled "Radio-Frequency Switch System Having Improved Intermodulation Distortion Performance," the disclosure of which is hereby incorporated by reference in its entirety.

BACKGROUND

1. Field

The present disclosure generally relates to the field of electronics, and more particularly, to radio-frequency switches.

2. Description of Related Art

Radio-frequency (RF) switches, such as transistor switches, can be used to switch signals between one or more poles and one or more throws. Transistor switches, or portions thereof, can be controlled through transistor biasing and/or coupling. Design and use of bias and/or coupling circuits in connection with RF switches can affect switching performance.

SUMMARY

In some implementations, the present disclosure relates to a radio-frequency (RF) switch system that includes a switch having a stack of field-effect transistors (FETs) connected in series between first and second nodes. The system further includes a capacitor connected in series with the switch and configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

In some embodiments, the FETs can be silicon-on-insulator (SOI) FETs. In some embodiments, the first node can be an antenna node. The capacitor can be disposed between the switch and the antenna node. The switch can be part of a transmit path such that the second node of the switch is an input node for an amplified RF signal. The switch can be part of a receive path such that the second node of the switch is an output node for an RF signal received from the antenna.

According to some implementations, the present disclosure relates to a semiconductor die having a semiconductor substrate and a switch formed on the semiconductor substrate and having a stack of field-effect transistors (FETs) connected in series. The die further includes a capacitor formed on the semiconductor substrate and connected in series with the switch. The capacitor is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

In some embodiments, the die can further include an insulator layer disposed between the FETs and the semiconductor substrate. The die can be a silicon-on-insulator (SOI) die.

In a number of implementations, the present disclosure relates to a method for fabricating a semiconductor die. The method includes providing a semiconductor substrate and forming a stack of field-effect transistors (FETs) on the semiconductor substrate so as to be connected in series. The method further includes forming a capacitor on the semiconductor substrate so as to be connected in series with an end of the stack. The capacitor is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the stack.

In some embodiments, the method can further include forming an insulator layer between the FETs and the semiconductor substrate.

In accordance with some implementations, the present disclosure relates to a radio-frequency (RF) switch module that includes a packaging substrate configured to receive a plurality of components. The module further includes a semiconductor die mounted on the packaging substrate. The die includes a switch having a stack of field-effect transistors (FETs) connected in series. The module further includes a capacitor connected in series with the switch. The capacitor is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

In some embodiments, the semiconductor die can be a silicon-on-insulator (SOI) die. In some embodiments, the capacitor can be part of the same semiconductor die as the FETs. In some embodiments, the capacitor can be part of a second die mounted on the packaging substrate. In some embodiments, the capacitor circuit can be disposed at a location outside of the semiconductor die.

In an number of implementations, the present disclosure relates to a wireless device that includes a transceiver configured to process RF signals. The wireless device further includes an antenna in communication with the transceiver. The wireless device further includes a switch module interconnected to the antenna and the transceiver and configured to selectively route RF signals to and from the antenna. The switch module includes a switch having a stack of field-effect transistors (FETs) connected in series. The switch module further includes a capacitor connected in series with the switch. The capacitor is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

BRIEF DESCRIPTION OF THE DRAWINGS

Various embodiments are depicted in the accompanying drawings for illustrative purposes, and should in no way be interpreted as limiting the scope of the inventions. In addition, various features of different disclosed embodiments can be combined to form additional embodiments, which are part of this disclosure. Throughout the drawings, reference numbers may be reused to indicate correspondence between reference elements.

FIG. **1** schematically shows a radio-frequency (RF) switch configured to switch one or more signals between one or more poles and one or more throws.

FIG. **2** shows that the RF switch **100** of FIG. **1** can include an RF core and an energy management (EM) core.

FIG. **3** shows an example of the RF core implemented in an single-pole-double-throw (SPDT) configuration.

FIG. **4** shows an example of the RF core implemented in an SPDT configuration where each switch arm can include a plurality of field-effect transistors (FETs) connected in series.

FIG. **5** schematically shows that controlling of one or more FETs in an RF switch can be facilitated by a circuit configured to bias and/or couple one or more portions of the FETs.

FIG. **6** shows examples of the bias/coupling circuit implemented on different parts of a plurality of FETs in a switch arm.

FIGS. **7**A and **7**B show plan and side sectional views of an example finger-based FET device implemented in a silicon-on-insulator (SOI) configuration.

FIGS. **8**A and **8**B show plan and side sectional views of an example of a multiple-finger FET device implemented in an SOI configuration.

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FIG. **9** shows an example where an RF switching configuration can include one or more capacitors to, for example, inhibit a low-frequency blocker from mixing with a fundamental frequency.

FIG. **10** shows an example where the switching configuration of FIG. **9** is in a transmit mode.

FIGS. **11**A-**11**D show examples of how various components for biasing, coupling, and/or facilitating the example configurations of FIGS. **9-10** can be implemented.

FIGS. **12**A and **12**B show an example of a packaged module that can include one or more features described herein.

FIG. **13** shows that in some embodiments, one or more features of the present disclosure can be implemented in a switch device such as a single-pole-multi-throw (SPMT) switch configured to facilitate multi-band multi-mode wireless operation.

FIG. **14** shows an example of a wireless device that can include one or more features described herein.

DETAILED DESCRIPTION

The headings provided herein, if any, are for convenience only and do not necessarily affect the scope or meaning of the claimed invention.

Example Components of a Switching Device:

FIG. **1** schematically shows a radio-frequency (RF) switch **100** configured to switch one or more signals between one or more poles **102** and one or more throws **104**. In some embodiments, such a switch can be based on one or more field-effect transistors (FETs) such as silicon-on-insulator (SOI) FETs. When a particular pole is connected to a particular throw, such a path is commonly referred to as being closed or in an ON state. When a given path between a pole and a throw is not connected, such a path is commonly referred to as being open or in an OFF state.

FIG. **2** shows that in some implementations, the RF switch **100** of FIG. **1** can include an RF core **110** and an energy management (EM) core **112**. The RF core **110** can be configured to route RF signals between the first and second ports. In the example single-pole-double-throw (SPDT) configuration shown in FIG. **2**, such first and second ports can include a pole **102***a* and a first throw **104***a*, or the pole **102***a* and a second throw **104***b*.

In some embodiments, EM core **112** can be configured to supply, for example, voltage control signals to the RF core. The EM core **112** can be further configured to provide the RF switch **100** with logic decoding and/or power supply conditioning capabilities.

In some embodiments, the RF core **110** can include one or more poles and one or more throws to enable passage of RF signals between one or more inputs and one or more outputs of the switch **100**. For example, the RF core **110** can include a single-pole double-throw (SPDT or SP2T) configuration as shown in FIG. **2**.

In the example SPDT context, FIG. **3** shows a more detailed example configuration of an RF core **110**. The RF core **110** is shown to include a single pole **102***a* coupled to first and second throw nodes **104***a*, **104***b* via first and second transistors (e.g., FETs) **120***a*, **120***b*. The first throw node **104***a* is shown to be coupled to an RF ground via an FET **122***a* to provide shunting capability for the node **104***a*. Similarly, the second throw node **104***b* is shown to be coupled to the RF ground via an FET **122***b* to provide shunting capability for the node **104***b*.

In an example operation, when the RF core **110** is in a state where an RF signal is being passed between the pole **102***a* and the first throw **104***a*, the FET **120***a* between the pole **102***a* and the first throw node **104***a* can be in an ON state, and the FET **120***b* between the pole **102***a* and the second throw node **104***b* can be in an OFF state. For the shunt FETs **122***a*, **122***b*, the shunt FET **122***a* can be in an OFF state so that the RF signal is not shunted to ground as it travels from the pole **102***a* to the first throw node **104***a*. The shunt FET **122***b* associated with the second throw node **104***b* can be in an ON state so that any RF signals or noise arriving at the RF core **110** through the second throw node **104***b* is shunted to the ground so as to reduce undesirable interference effects to the pole-to-first-throw operation.

Although the foregoing example is described in the context of a single-pole-double-throw configuration, it will be understood that the RF core can be configured with other numbers of poles and throws. For example, there may be more than one poles, and the number of throws can be less than or greater than the example number of two.

In the example of FIG. **3**, the transistors between the pole **102***a* and the two throw nodes **104***a*, **104***b* are depicted as single transistors. In some implementations, such switching functionalities between the pole(s) and the throw(s) can be provided by switch arm segments, where each switch arm segment includes a plurality of transistors such as FETs.

An example RF core configuration **130** of an RF core having such switch arm segments is shown in FIG. **4**. In the example, the pole **102***a* and the first throw node **104***a* are shown to be coupled via a first switch arm segment **140***a*. Similarly, the pole **102***a* and the second throw node **104***b* are shown to be coupled via a second switch arm segment **140***b*. The first throw node **104***a* is shown to be capable of being shunted to an RF ground via a first shunt arm segment **142***a*. Similarly, the second throw node **104***b* is shown to be capable of being shunted to the RF ground via a second shunt arm segment **142***b*.

In an example operation, when the RF core **130** is in a state where an RF signal is being passed between the pole **102***a* and the first throw node **104***a*, all of the FETs in the first switch arm segment **140***a* can be in an ON state, and all of the FETs in the second switch arm segment **104***b* can be in an OFF state. The first shunt arm **142***a* for the first throw node **104***a* can have all of its FETs in an OFF state so that the RF signal is not shunted to ground as it travels from the pole **102***a* to the first throw node **104***a*. All of the FETs in the second shunt arm **142***b* associated with the second throw node **104***b* can be in an ON state so that any RF signals or noise arriving at the RF core **130** through the second throw node **104***b* is shunted to the ground so as to reduce undesirable interference effects to the pole-to-first-throw operation.

Again, although described in the context of an SP2T configuration, it will be understood that RF cores having other numbers of poles and throws can also be implemented.

In some implementations, a switch arm segment (e.g., **140***a*, **140***b*, **142***a*, **142***b*) can include one or more semiconductor transistors such as FETs. In some embodiments, an FET may be capable of being in a first state or a second state and can include a gate, a drain, a source, and a body (sometimes also referred to as a substrate. In some embodiments, an FET can include a metal-oxide-semiconductor field effect transistor (MOSFET). In some embodiments, one or more FETs can be connected in series forming a first end and a second end such that an RF signal can be routed between the first end and the second end when the FETs are in a first state (e.g., ON state).

At least some of the present disclosure relates to how an FET or a group of FETs can be controlled to provide switching functionalities in desirable manners. FIG. **5** schematically shows that in some implementations, such controlling of an

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FET **120** can be facilitated by a circuit **150** configured to bias and/or couple one or more portions of the FET **120**. In some embodiments, such a circuit **150** can include one or more circuits configured to bias and/or couple a gate of the FET **120**, bias and/or couple a body of the FET **120**, and/or couple a source/drain of the FET **120**.

Schematic examples of how such biasing and/or coupling of different parts of one or more FETs are described in reference to FIG. **6**. In FIG. **6**, a switch arm segment **140** (that can be, for example, one of the example switch arm segments **140***a*, **140***b*, **142***a*, **142***b* of the example of FIG. **4**) between nodes **144**, **146** is shown to include a plurality of FETs **120**. Operations of such FETs can be controlled and/or facilitated by a gate bias/coupling circuit **150***a*, and a body bias/coupling circuit **150***c*, and/or a source/drain coupling circuit **150***b*.

Gate Bias/Coupling Circuit

In the example shown in FIG. **6**, the gate of each of the FETs **120** can be connected to the gate bias/coupling circuit **150***a* to receive a gate bias signal and/or couple the gate to another part of the FET **120** or the switch arm **140**. In some implementations, designs or features of the gate bias/coupling circuit **150***a* can improve performance of the switch arm **140**. Such improvements in performance can include, but are not limited to, device insertion loss, isolation performance, power handling capability and/or switching device linearity.

Body Bias/Coupling Circuit

As shown in FIG. **6**, the body of each FET **120** can be connected to the body bias/coupling circuit **150***c* to receive a body bias signal and/or couple the body to another part of the FET **120** or the switch arm **140**. In some implementations, designs or features of the body bias/coupling circuit **150***c* can improve performance of the switch arm **140**. Such improvements in performance can include, but are not limited to, device insertion loss, isolation performance, power handling capability and/or switching device linearity.

Source/Drain Coupling Circuit

As shown in FIG. **6**, the source/drain of each FET **120** can be connected to the coupling circuit **150***b* to couple the source/drain to another part of the FET **120** or the switch arm **140**. In some implementations, designs or features of the coupling circuit **150***b* can improve performance of the switch arm **140**. Such improvements in performance can include, but are not limited to, device insertion loss, isolation performance, power handling capability and/or switching device linearity.

Examples of Switching Performance Parameters:

Insertion Loss

A switching device performance parameter can include a measure of insertion loss. A switching device insertion loss can be a measure of the attenuation of an RF signal that is routed through the RF switching device. For example, the magnitude of an RF signal at an output port of a switching device can be less than the magnitude of the RF signal at an input port of the switching device. In some embodiments, a switching device can include device components that introduce parasitic capacitance, inductance, resistance, or conductance into the device, contributing to increased switching device insertion loss. In some embodiments, a switching device insertion loss can be measured as a ratio of the power or voltage of an RF signal at an input port to the power or voltage of the RF signal at an output port of the switching device. Decreased switching device insertion loss can be desirable to enable improved RF signal transmission.

Isolation

A switching device performance parameter can also include a measure of isolation. Switching device isolation can be a measure of the RF isolation between an input port and an output port an RF switching device. In some embodiments, it can be a measure of the RF isolation of a switching device while the switching device is in a state where an input port and an output port are electrically isolated, for example while the switching device is in an OFF state. Increased switching device isolation can improve RF signal integrity. In certain embodiments, an increase in isolation can improve wireless communication device performance.

Intermodulation Distortion

A switching device performance parameter can further include a measure of intermodulation distortion (IMD) performance. Intermodulation distortion (IMD) can be a measure of non-linearity in an RF switching device.

IMD can result from two or more signals mixing together and yielding frequencies that are not harmonic frequencies. For example, suppose that two signals have fundamental frequencies f_1 and f_2 ($f_2>f_1$) that are relatively close to each other in frequency space. Mixing of such signals can result in peaks in frequency spectrum at frequencies corresponding to different products of fundamental and harmonic frequencies of the two signals. For example, a second-order intermodulation distortion (also referred to as IMD2) is typically considered to include frequencies f_1+f_2 f_2-f_1, $2f_1$, and $2f_2$. A third-order IMD (also referred to as IMD3) is typically considered to include $2f_1+f_2$, $2f_1-f_2$, f_1+2f_2, f_1-f_2. Higher order products can be formed in similar manners.

In general, as the IMD order number increases, power levels decrease. Accordingly, second and third orders can be undesirable effects that are of particular interest. Higher orders such as fourth and fifth orders can also be of interest in some situations.

In some RF applications, it can be desirable to reduce susceptibility to interference within an RF system. Non linearity in RF systems can result in introduction of spurious signals into the system. Spurious signals in the RF system can result in interference within the system and degrade the information transmitted by RF signals. An RF system having increased non-linearity can demonstrate increased susceptibility to interference. Non-linearity in system components, for example switching devices, can contribute to the introduction of spurious signals into the RF system, thereby contributing to degradation of overall RF system linearity and IMD performance.

In some embodiments, RF switching devices can be implemented as part of an RF system including a wireless communication system. IMD performance of the system can be improved by increasing linearity of system components, such as linearity of an RF switching device. In some embodiments, a wireless communication system can operate in a multi-band and/or multi-mode environment. Improvement in intermodulation distortion (IMD) performance can be desirable in wireless communication systems operating in a multi-band and/or multi-mode environment. In some embodiments, improvement of a switching device IMD performance can improve the IMD performance of a wireless communication system operating in a multi-mode and/or multi-band environment.

Improved switching device IMD performance can be desirable for wireless communication devices operating in various wireless communication standards, for example for wireless communication devices operating in the LTE communication standard. In some RF applications, it can be desirable to improve linearity of switching devices operating in wireless communication devices that enable simultaneous transmission of data and voice communication. For example, improved IMD performance in switching devices can be desirable for wireless communication devices operating in

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the LTE communication standard and performing simultaneous transmission of voice and data communication (e.g., SVLTE).

High Power Handling Capability

In some RF applications, it can be desirable for RF switching devices to operate under high power while reducing degradation of other device performance parameters. In some embodiments, it can be desirable for RF switching devices to operate under high power with improved intermodulation distortion, insertion loss, and/or isolation performance.

In some embodiments, an increased number of transistors can be implemented in a switch arm segment of a switching device to enable improved power handling capability of the switching device. For example, a switch arm segment can include an increased number of FETs connected in series, an increased FET stack height, to enable improved device performance under high power. However, in some embodiments, increased FET stack height can degrade the switching device insertion loss performance.

Examples of FET Structures and Fabrication Process Technologies:

A switching device can be implemented on-die, off-die, or some combination thereon. A switching device can also be fabricated using various technologies. In some embodiments, RF switching devices can be fabricated with silicon or silicon-on-insulator (SOI) technology.

As described herein, an RF switching device can be implemented using silicon-on-insulator (SOI) technology. In some embodiments, SOI technology can include a semiconductor substrate having an embedded layer of electrically insulating material, such as a buried oxide layer beneath a silicon device layer. For example, an SOI substrate can include an oxide layer embedded below a silicon layer. Other insulating materials known in the art can also be used.

Implementation of RF applications, such as an RF switching device, using SOI technology can improve switching device performance. In some embodiments, SOI technology can enable reduced power consumption. Reduced power consumption can be desirable in RF applications, including those associated with wireless communication devices. SOI technology can enable reduced power consumption of device circuitry due to decreased parasitic capacitance of transistors and interconnect metallization to a silicon substrate. Presence of a buried oxide layer can also reduce junction capacitance or use of high resistivity substrate, enabling reduced substrate related RF losses. Electrically isolated SOI transistors can facilitate stacking, contributing to decreased chip size.

In some SOI FET configurations, each transistor can be configured as a finger-based device where the source and drain are rectangular shaped (in a plan view) and a gate structure extends between the source and drain like a rectangular shaped finger. FIGS. **7**A and **7**B show plan and side sectional views of an example finger-based FET device implemented on SOI. As shown, FET devices described herein can include a p-type FET or an n-type FET. Thus, although some FET devices are described herein as p-type devices, it will be understood that various concepts associated with such p-type devices can also apply to n-type devices.

As shown in FIGS. **7**A and **7**B, a pMOSFET can include an insulator layer formed on a semiconductor substrate. The insulator layer can be formed from materials such as silicon dioxide or sapphire. An n-well is shown to be formed in the insulator such that the exposed surface generally defines a rectangular region. Source (S) and drain (D) are shown to be p-doped regions whose exposed surfaces generally define rectangles. As shown, S/D regions can be configured so that source and drain functionalities are reversed.

FIGS. **7**A and **7**B further show that a gate (G) can be formed on the n-well so as to be positioned between the source and the drain. The example gate is depicted as having a rectangular shape that extends along with the source and the drain. Also shown is an n-type body contact. Formations of the rectangular shaped well, source and drain regions, and the body contact can be achieved by a number of known techniques. In some embodiments, the source and drain regions can be formed adjacent to the ends of their respective upper insulator layers, and the junctions between the body and the source/drain regions on the opposing sides of the body can extend substantially all the way down to the top of the buried insulator layer. Such a configuration can provide, for example, reduced source/drain junction capacitance. To form a body contact for such a configuration, an additional gate region can be provided on the side so as to allow, for example, an isolated P+ region to contact the Pwell.

FIGS. **8**A and **8**B show plan and side sectional views of an example of a multiple-finger FET device implemented on SOI. Formations of rectangular shaped n-well, rectangular shaped p-doped regions, rectangular shaped gates, and n-type body contact can be achieved in manners similar to those described in reference to FIGS. **7**A and **7**B.

The example multiple-finger FET device of FIGS. **8**A and **8**B can be made to operate such that a drain of one FET acts as a source of its neighboring FET. Thus, the multiple-finger FET device as a whole can provide a voltage-dividing functionality. For example, an RF signal can be provided at one of the outermost p-doped regions (e.g., the leftmost p-doped region); and as the signal passes through the series of FETs, the signal's voltage can be divided among the FETs. In such an example, the rightmost p-doped region can act as an overall drain of the multi-finger FET device.

In some implementations, a plurality of the foregoing multi-finger FET devices can be connected in series as a switch to, for example, further facilitate the voltage-dividing functionality. A number of such multi-finger FET devices can be selected based on, for example, power handling requirement of the switch.

Examples of Bias and/or Coupling Configurations for Improved Performance:

Described herein are various examples of how FET-based switch circuits can be biased and/or coupled to yield one or more performance improvements. In some embodiments, such biasing/coupling configurations can be implemented in SOI FET-based switch circuits. It will be understood that some of the example biasing/coupling configurations can be combined to yield a combination of desirable features that may not be available to the individual configurations. It will also be understood that, although described in the context of RF switching applications, one or more features described herein can also be applied to other circuits and devices that utilize FETs such as SOI FETs.

Example Configurations

Intermodulation distortion (IMD) measures an unwanted signal added to a desired signal due to mixing products from other RF signals. Such an effect can be particularly dominant in a multi-mode, multi-band environment. IMD can the result from two or more signals mixing together to yield frequencies that are not harmonic frequencies.

System designers typically strive to reduce interference susceptibility through, for example, improved linearity. A given system's linearity can govern how much IMD will occur within it, which in turn can create interferences. Through improved linearity of the system building blocks, such as an RF switch, the overall susceptibility of a system to interference can be decreased.

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Performance features such as a lower IMD in RF switches can be an important factor in wireless-device designs. For example Long Term Evolution (LTE) systems can benefit significantly from RF switches having reduced IMDs. As a more specific example, system designs for simultaneous voice and data on LTE (SVLTE) can benefit significantly from RF switches having ultra-low levels of IMDs.

FIG. **9** shows a switching configuration **250** in an example context of a single-pole-dual-throw (SPDT) application. The single pole is shown to be connected to an antenna **252**. One of the two throws is shown to be coupled to a receive (Rx) port via a switch circuit S. The Rx port can be coupled to a ground via a shunt switch circuit.

Similarly, the other throw is shown to be coupled to a transmit (Tx) port via a switch circuit S. The Tx port can be coupled to the ground via a shunt switch circuit.

In some embodiments, each of the switch circuits ("S" and "Shunt") can include one or more FETs such as SOI FETs. A single FET is sometimes referred to herein with a reference numeral **120** or **122**, and a stack of such FETs is sometimes referred to herein with a reference numeral **140** or **142**. In some embodiments, the "S" and "Shunt" switches can include one or more features described herein to provide various advantageous functionalities.

The switching configuration of FIG. **9** is shown to include capacitors to inhibit a low-frequency blocker from mixing with a fundamental frequency. For example, a capacitor C**1** is provided between the antenna node and the switch arm S of the Tx throw. Similarly, a capacitor C**2** is provided between the antenna node and the switch arm S of the Rx throw. For the shunt arms, a capacitor C**3** is provided between the Tx node and its shunt switch arm. Similarly, a capacitor C**4** is provided between the Rx node and its shunt switch arm. In some embodiments, a shunt arm may or may not be provided for the Rx node. With the foregoing capacitors, a low-frequency jammer signal can be blocked or reduced from mixing with any ON or OFF paths. This can lead to improvement in IMD performance, especially for low-frequency blocker signals.

FIG. **10** shows an example operating configuration where some of the foregoing capacitors can provide desirable switching functionalities. In the example, the switching configuration is in a transmit mode. Accordingly, the transmit switch arm is ON (closed), and the receive switch arm is OFF (open). The shunt arm for the Tx node is OFF (open).

In some embodiments, capacitors C**1**-C**4** described in reference to FIGS. **9** and **10** can be implemented on the same die as their respective switch circuits, off of the die, or any combination thereof.

In some implementations, and as described herein, the foregoing example configurations described in reference to FIGS. **9** and **10** can be relatively simpler and easier to implement, and can yield a number of improvements. For example, this technique can provide improved IMD performance by preventing a low-frequency blocker signal from mixing with a fundamental frequency signal.

Examples of Implementations in Products:

Various examples of FET-based switch circuits and bias/coupling configurations described herein can be implemented in a number of different ways and at different product levels. Some of such product implementations are described by way of examples.

Semiconductor Die Implementation

FIGS. **11**A-**11**D schematically show non-limiting examples of such implementations on one or more semiconductor die. FIG. **11**A shows that in some embodiments, a switch circuit **120** and a bias/coupling circuit **150** having one or more features as described herein can be implemented on a die **800**. FIG. **11**B shows that in some embodiments, at least some of the bias/coupling circuit **150** can be implemented outside of the die **800** of FIG. **11**A.

FIG. **11**C shows that in some embodiments, a switch circuit **120** having one or more features as described herein can be implemented on a first die **800***a*, and a bias/coupling circuit **150** having one or more features as described herein can be implemented on a second die **800***b*. FIG. **11**D shows that in some embodiments, at least some of the bias/coupling circuit **150** can be implemented outside of the first die **800***a* of FIG. **11**C.

Packaged Module Implementation

In some embodiments, one or more die having one or more features described herein can be implemented in a packaged module. An example of such a module is shown in FIGS. **12**A (plan view) and **12**B (side view). Although described in the context of both of the switch circuit and the bias/coupling circuit being on the same die (e.g., example configuration of FIG. **11**A), it will be understood that packaged modules can be based on other configurations.

A module **810** is shown to include a packaging substrate **812**. Such a packaging substrate can be configured to receive a plurality of components, and can include, for example, a laminate substrate. The components mounted on the packaging substrate **812** can include one or more dies. In the example shown, a die **800** having a switching circuit **120** and a bias/coupling circuit **150** is shown to be mounted on the packaging substrate **812**. The die **800** can be electrically connected to other parts of the module (and with each other where more than one die is utilized) through connections such as connection-wirebonds **816**. Such connection-wirebonds can be formed between contact pads **818** formed on the die **800** and contact pads **814** formed on the packaging substrate **812**. In some embodiments, one or more surface mounted devices (SMDs) **822** can be mounted on the packaging substrate **812** to facilitate various functionalities of the module **810**.

In some embodiments, the packaging substrate **812** can include electrical connection paths for interconnecting the various components with each other and/or with contact pads for external connections. For example, a connection path **832** is depicted as interconnecting the example SMD **822** and the die **800**. In another example, a connection path **832** is depicted as interconnecting the SMD **822** with an external-connection contact pad **834**. In yet another example a connection path **832** is depicted as interconnecting the die **800** with ground-connection contact pads **836**.

In some embodiments, a space above the packaging substrate **812** and the various components mounted thereon can be filled with an overmold structure **830**. Such an overmold structure can provide a number of desirable functionalities, including protection for the components and wirebonds from external elements, and easier handling of the packaged module **810**.

FIG. **13** shows a schematic diagram of an example switching configuration that can be implemented in the module **810** described in reference to FIGS. **12**A and **12**B. In the example, the switch circuit **120** is depicted as being an SP9T switch, with the pole being connectable to an antenna and the throws being connectable to various Rx and Tx paths. Such a configuration can facilitate, for example, multi-mode multi-band operations in wireless devices.

The module **810** can further include an interface for receiving power (e.g., supply voltage VDD) and control signals to facilitate operation of the switch circuit **120** and/or the bias/coupling circuit **150**. In some implementations, supply voltage and control signals can be applied to the switch circuit **120** via the bias/coupling circuit **150**.

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Wireless Device Implementation

In some implementations, a device and/or a circuit having one or more features described herein can be included in an RF device such as a wireless device. Such a device and/or a circuit can be implemented directly in the wireless device, in a modular form as described herein, or in some combination thereof. In some embodiments, such a wireless device can include, for example, a cellular phone, a smart-phone, a hand-held wireless device with or without phone functionality, a wireless tablet, etc.

FIG. **14** schematically depicts an example wireless device **900** having one or more advantageous features described herein. In the context of various switches and various biasing/coupling configurations as described herein, a switch **120** and a bias/coupling circuit **150** can be part of a module **810**. In some embodiments, such a switch module can facilitate, for example, multi-band multip-mode operation of the wireless device **900**.

In the example wireless device **900**, a power amplifier (PA) module **916** having a plurality of PAs can provide an amplified RF signal to the switch **120** (via a duplexer **920**), and the switch **120** can route the amplified RF signal to an antenna. The PA module **916** can receive an unamplified RF signal from a transceiver **914** that can be configured and operated in known manners. The transceiver can also be configured to process received signals. The transceiver **914** is shown to interact with a baseband sub-system **910** that is configured to provide conversion between data and/or voice signals suitable for a user and RF signals suitable for the transceiver **914**. The transceiver **914** is also shown to be connected to a power management component **906** that is configured to manage power for the operation of the wireless device **900**. Such a power management component can also control operations of the baseband sub-system **910** and the module **810**.

The baseband sub-system **910** is shown to be connected to a user interface **902** to facilitate various input and output of voice and/or data provided to and received from the user. The baseband sub-system **910** can also be connected to a memory **904** that is configured to store data and/or instructions to facilitate the operation of the wireless device, and/or to provide storage of information for the user.

In some embodiments, the duplexer **920** can allow transmit and receive operations to be performed simultaneously using a common antenna (e.g., **924**). In FIG. **14**, received signals are shown to be routed to "Rx" paths (not shown) that can include, for example, a low-noise amplifier (LNA).

A number of other wireless device configurations can utilize one or more features described herein. For example, a wireless device does not need to be a multi-band device. In another example, a wireless device can include additional antennas such as diversity antenna, and additional connectivity features such as Wi-Fi, Bluetooth, and GPS.

General Comments

Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not limited to." The word "coupled", as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words "herein," "above," "below," and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word "or" in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

The above detailed description of embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise form disclosed above. While specific embodiments of, and examples for, the invention are described above for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. For example, while processes or blocks are presented in a given order, alternative embodiments may perform routines having steps, or employ systems having blocks, in a different order, and some processes or blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these processes or blocks may be implemented in a variety of different ways. Also, while processes or blocks are at times shown as being performed in series, these processes or blocks may instead be performed in parallel, or may be performed at different times.

The teachings of the invention provided herein can be applied to other systems, not necessarily the system described above. The elements and acts of the various embodiments described above can be combined to provide further embodiments.

While certain embodiments of the inventions have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

What is claimed is:

1. A radio-frequency (RF) switch system comprising:
- a first switch circuit connected between an antenna node and a transmit node;
- a second switch circuit connected between the antenna node and a receive node;
- a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node;
- a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node;
- a first shunt arm connected to the first switch circuit and the transmit node, the first shunt arm including a third switch circuit connected to ground; and
- a second shunt arm connected to the second switch circuit and the receive node, the second shunt arm including a fourth switch circuit connected to ground.

2. The switch system of claim **1** wherein at least one of the first and second capacitors is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

3. The switch system of claim **1** wherein the first shunt arm includes a third capacitor connected between the third switch circuit and the transmit node, and the second shunt arm includes a fourth capacitor connected between the fourth switch circuit and the receive node.

4. A radio-frequency (RF) switch system comprising:
- a first switch circuit connected between an antenna node and a transmit node;

a second switch circuit connected between the antenna node and a receive node;

a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node;

a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node;

a first shunt arm connected to the first switch circuit and the transmit node, the first shunt arm including a third switch circuit connected to ground and a third capacitor connected between the third switch circuit and the transmit node.

5. A method for fabricating a semiconductor die, the method comprising:

providing a semiconductor substrate;

forming a first switch circuit on the semiconductor substrate so as to be connected between an antenna node and a transmit node;

forming a second switch circuit on the semiconductor substrate so as to be connected between the antenna node and a receive node;

forming a first capacitor on the semiconductor substrate so as to be connected in series with the first switch circuit between the first switch circuit and the antenna node;

forming a second capacitor on the semiconductor substrate so as to be connected in series with the second switch circuit between the second switch circuit and the antenna node;

forming a first shunt arm connected to the first switch circuit and the transmit node, the first shunt arm including a third switch circuit connected to ground; and

forming a second shunt arm connected to the second switch circuit and the receive node, the second shunt arm including a fourth switch circuit connected to ground.

6. The method of claim **5** further comprising forming an insulator layer between the first switch circuit and the semiconductor substrate.

7. A radio-frequency (RF) switch module comprising:

a packaging substrate configured to receive a plurality of components;

a semiconductor die mounted on the packaging substrate, the die including a first switch circuit connected between an antenna node and a transmit node and a second switch circuit connected between the antenna node and a receive node;

a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node;

a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node;

a first shunt arm connected to the first switch circuit and the transmit node, the first shunt arm including a third switch circuit connected to ground; and

a second shunt arm connected to the second switch circuit and the receive node, the second shunt arm including a fourth switch circuit connected to ground.

8. The switch module of claim **7** wherein at least one of the first and second capacitors is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

9. The switch module of claim **7** wherein the first capacitor is part of the same semiconductor die as the first switch circuit.

10. The switch module of claim **7** wherein the first capacitor is part of a second die mounted on the packaging substrate.

11. The switch module of claim **7** wherein the first capacitor is disposed at a location outside of the semiconductor die.

* * * * *

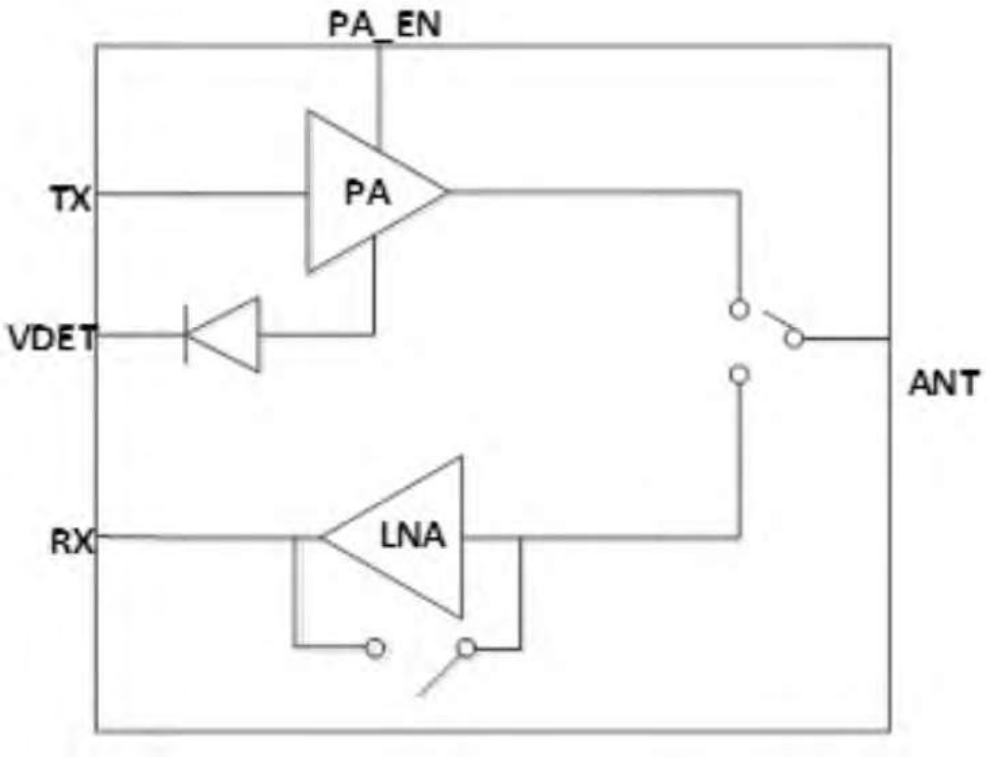
EXHIBIT 10

EXHIBIT 10
SKYWORKS SOLUTIONS, INC.'S INFRINGEMENT CHART
KCT8539S
U.S. Patent No. 8,717,101
Independent Claims 1, 17, and 21

Skyworks Solutions, Inc. ("Skyworks") provides this exemplary claim chart for independent claims 1, 17, and 21 of U.S. Patent No. 8,717,101 (the "'101 patent") applied to Kangxi Communication Technologies (Shanghai) Co., Ltd's and Grand Chip Labs, Inc.'s (collectively, "KCT") KCT8539S product. The disclosures in this claim chart directed to the KCT8539S are also more broadly directed to any sale, offer for sale, use, or importation of the KCT8539S in the U.S., including in an end product such as a wireless router or as a standalone product that is not incorporated in an end product.

The claim chart below demonstrates infringement by comparing each element of the charted claims to corresponding components, aspects, and/or features of the KCT8539S product. This claim chart is not intended to constitute an expert report on infringement. This claim chart includes information provided by way of example, and not by way of limitation.

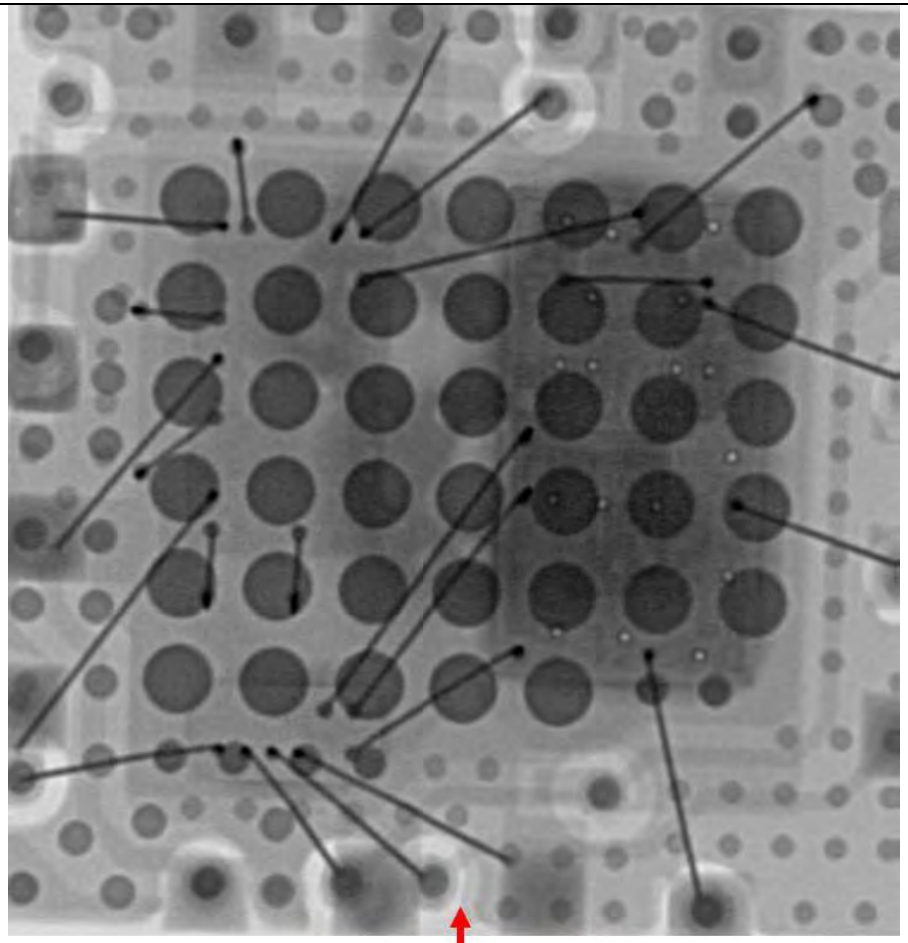
The analysis set forth below is based only upon information from publicly available sources regarding the KCT8539S product. Further analysis of non-public information during fact discovery will likely assist in identifying all infringing features and functionalities used by KCT in the KCT8539S product. Accordingly, Skyworks reserves the right to supplement this infringement analysis once such information is made available to Skyworks. Further, Skyworks reserves the right to supplement this infringement analysis, as appropriate, upon issuance of an order construing any terms recited in the asserted claims or as other circumstances so merit.

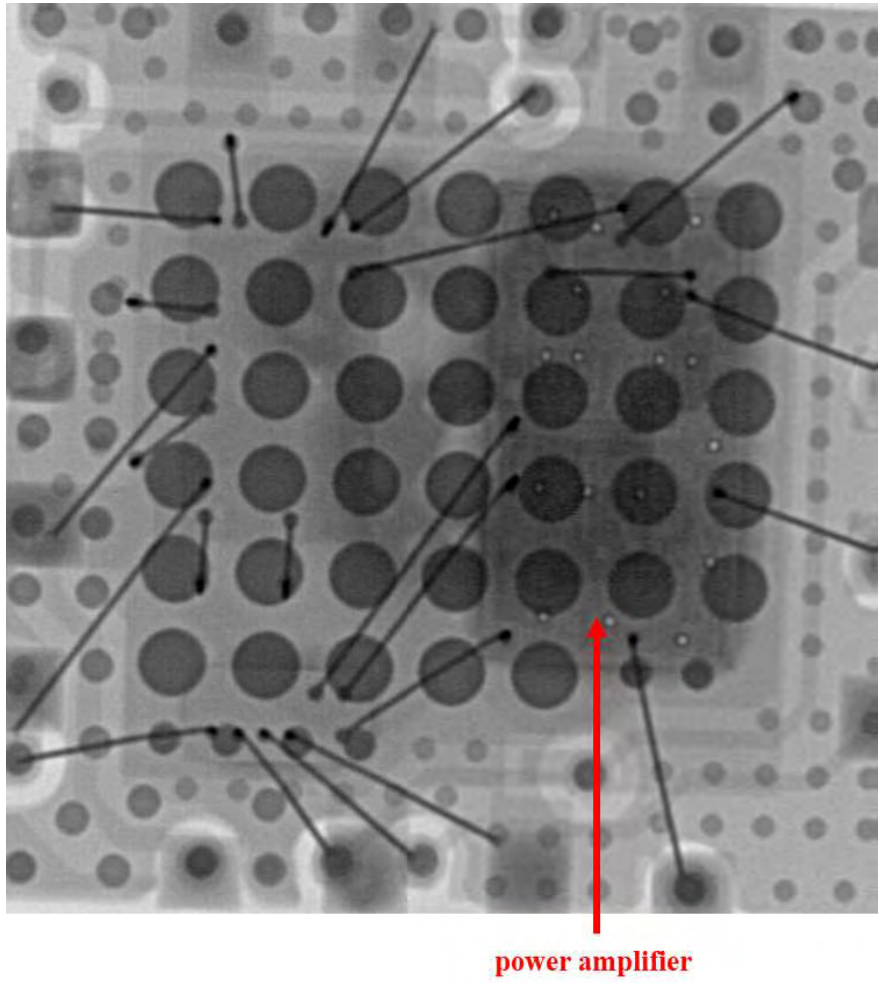
Claims	KCT8539S
1[pre] A power amplifier system comprising:	To the extent the preamble of claim 1 is limiting, the KCT8539S includes a power amplifier system. The KCT8539S is a product for Wi-Fi connectivity. For example, the following image for the KCT8539S is a simplified block diagram for this product.[1]  *See, e.g.*, simplified block diagram for KCT8539S The KCT8539S is, according to KCT, "a highly integrated RF front-end integrated circuit incorporat[ing] key RF functionality needed for IEEE 802.11a/n/ac/ax WLAN systems operating in the 5.15-5.85GHz

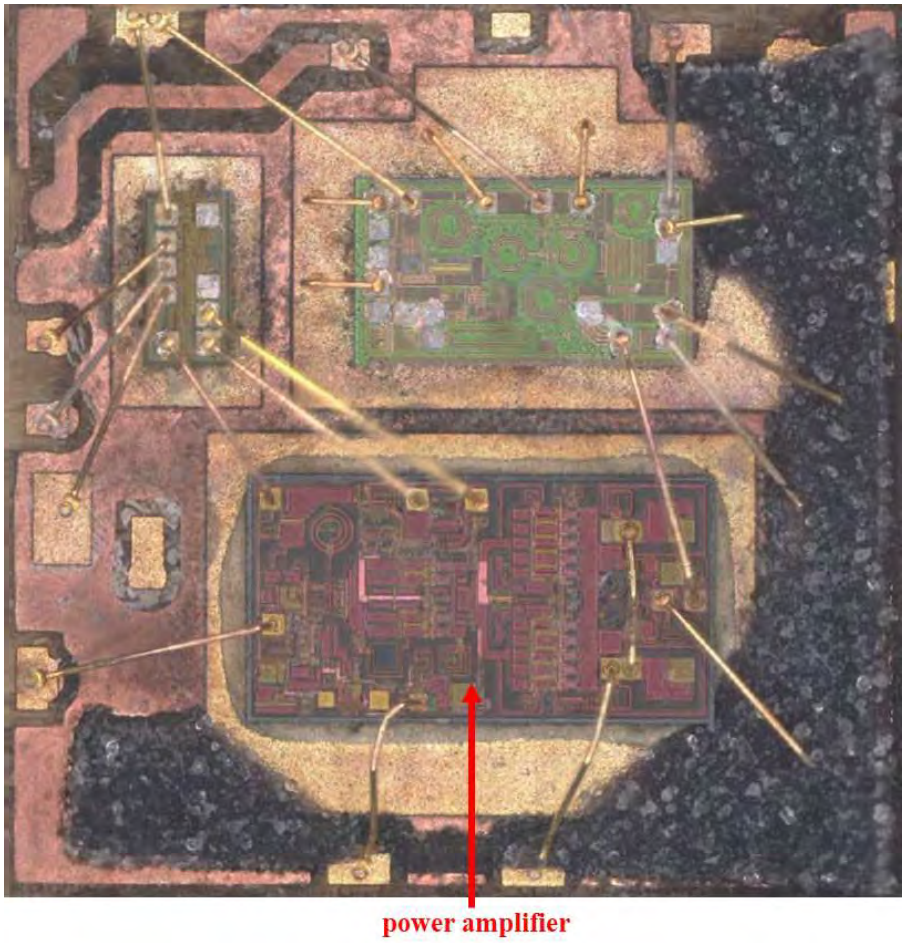
[1] *See* https://perma.cc/DA7F-4CED.

	range. KCT8539S integrates a high-efficiency high-linearity power amplifier (PA), a low noise amplifier (LNA) with bypass ….”[2] For example, the image below of the KCT8539S shows a power amplifier system (as indicated by the corresponding label below) within the KCT8539S.

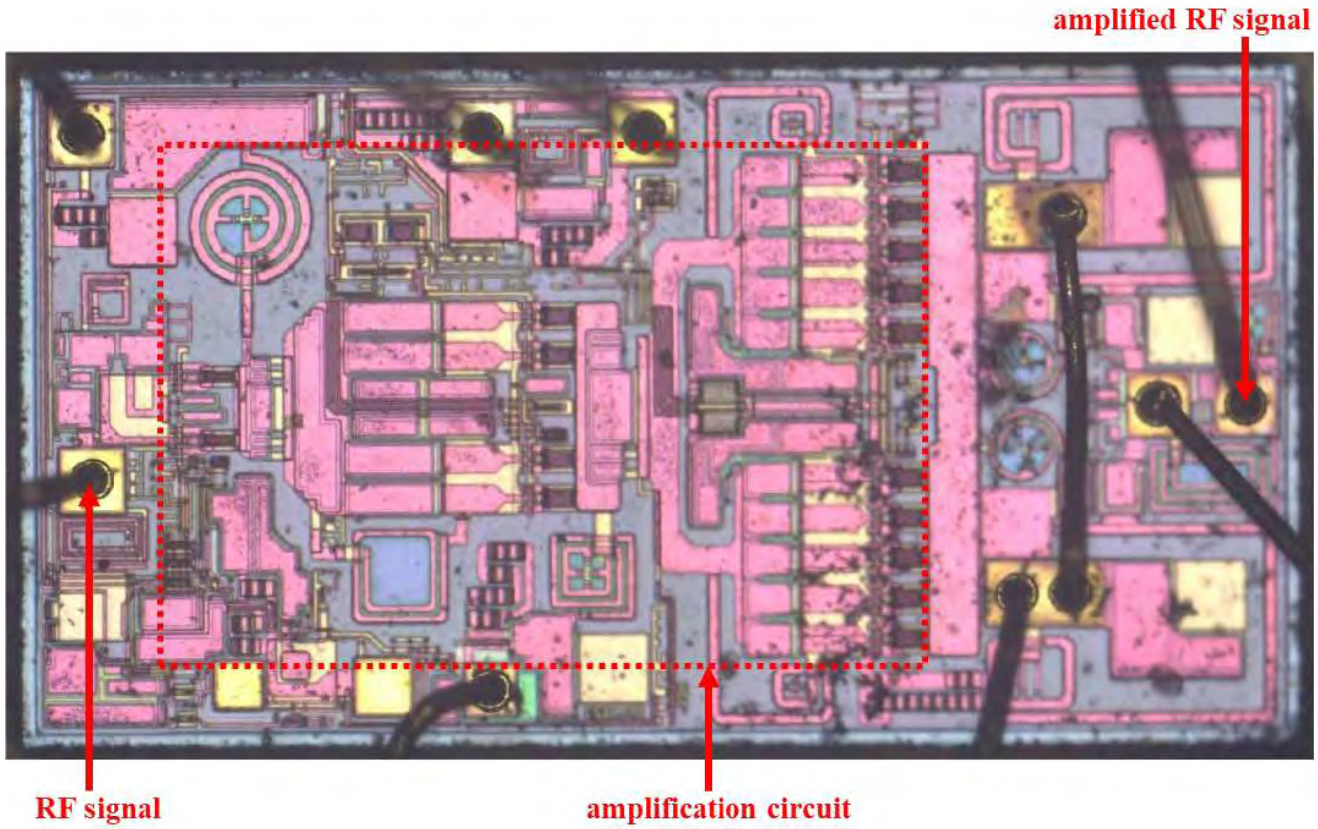
[2] *See* https://perma.cc/DA7F-4CED.

	 *See, e.g.*, photo of KCT8539S showing three dies of the power amplifier system
1[A] a power amplifier configured to amplify a radio	The KCT8539S includes a power amplifier configured to amplify a radio frequency (RF) signal.

frequency (RF) signal; and	For example, the image of the KCT8539S below shows a power amplifier (as indicated by the corresponding label below) as part of the power amplifier system.  *See, e.g.*, photo of KCT8539S showing three dies, including a die for the power amplifier of the power amplifier system

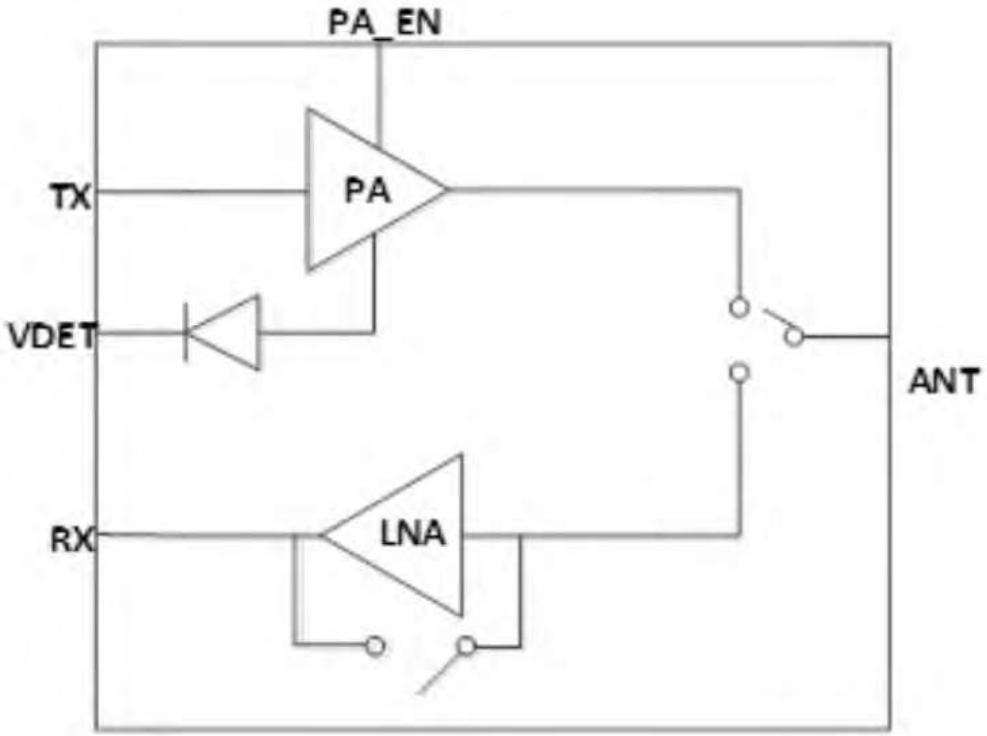
	The image below shows the die of the power amplifier as part of the power amplifier system for the KCT8539S.  *See, e.g.*, photo of KCT8539S showing three dies, including the die for the power amplifier of the power amplifier system

The image below shows an enlarged view of the power amplifier die of the KCT8539S. The power amplifier in the KCT8539S is coupled so that it is configured to receive as an input a radio frequency (RF) signal, as labeled below, and amplify the RF signal to output an amplified RF signal, as labeled below. The dashed box with the corresponding label below is one example of an amplification circuit that provides the amplification of the RF signal.

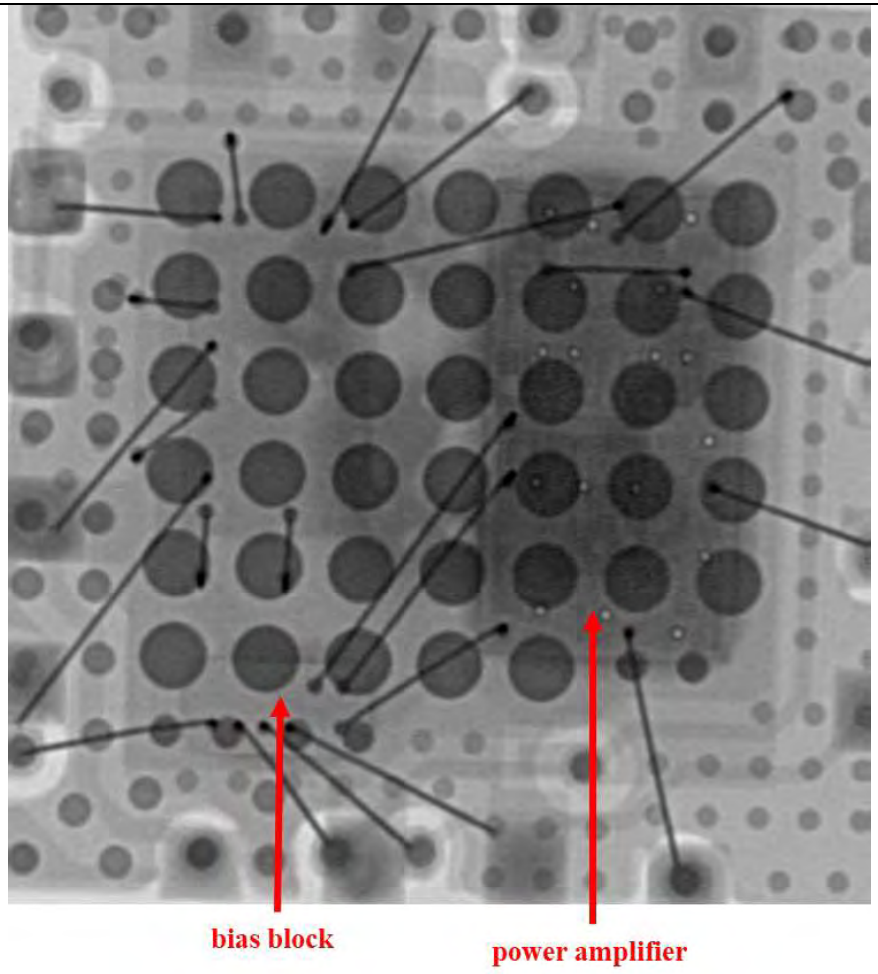


See, e.g., photo of the power amplifier die in KCT8539S

As shown below in KCT's simplified block diagram for the KCT8539S, a power amplifier (labelled as "PA") is part of the KCT8539S product. Specifically, the KCT8539S "integrates a high-efficiency high-

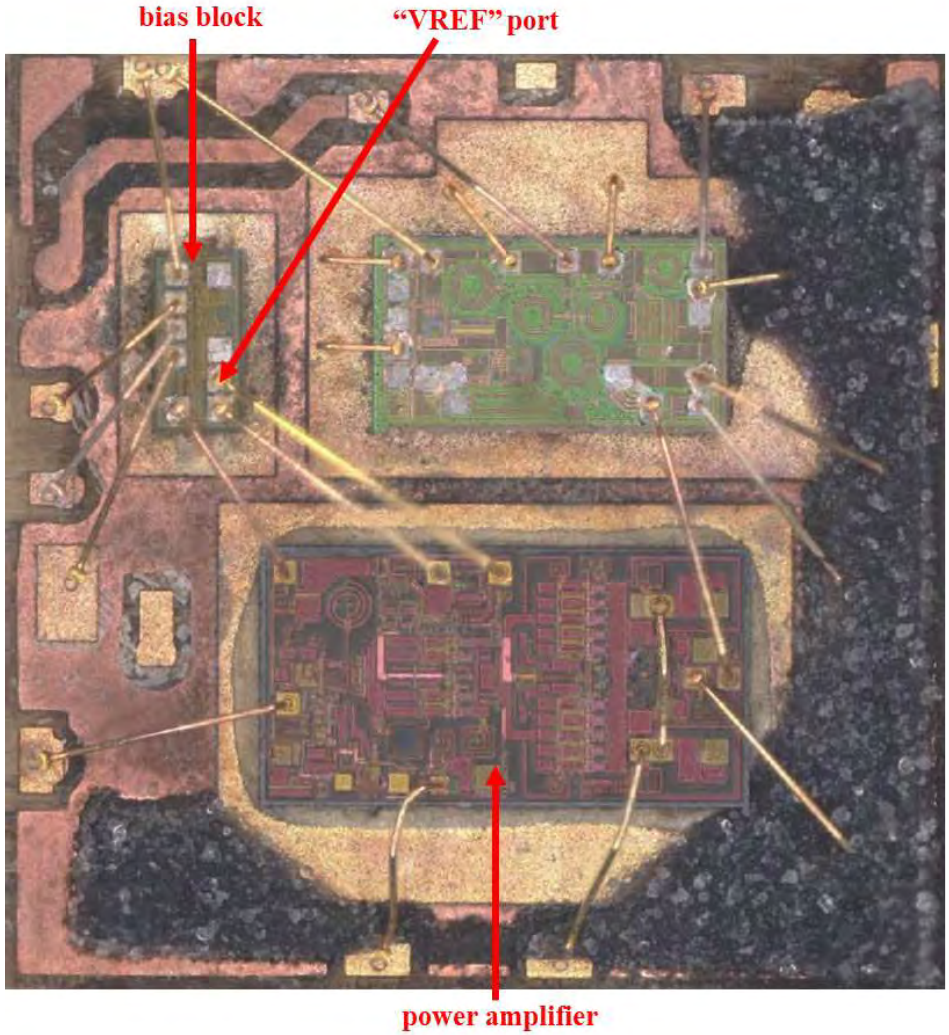
	linearity power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated matching network, LO rejection, and harmonic filters all in one device."[3]  *See, e.g.*, simplified block diagram for KCT8539S
1[B] a bias block for biasing the power amplifier,	The KCT8539S includes a bias block for biasing the power amplifier. For example, the image of the KCT8539S below shows a bias block (as indicated by the corresponding label below) as part of the power amplifier system.

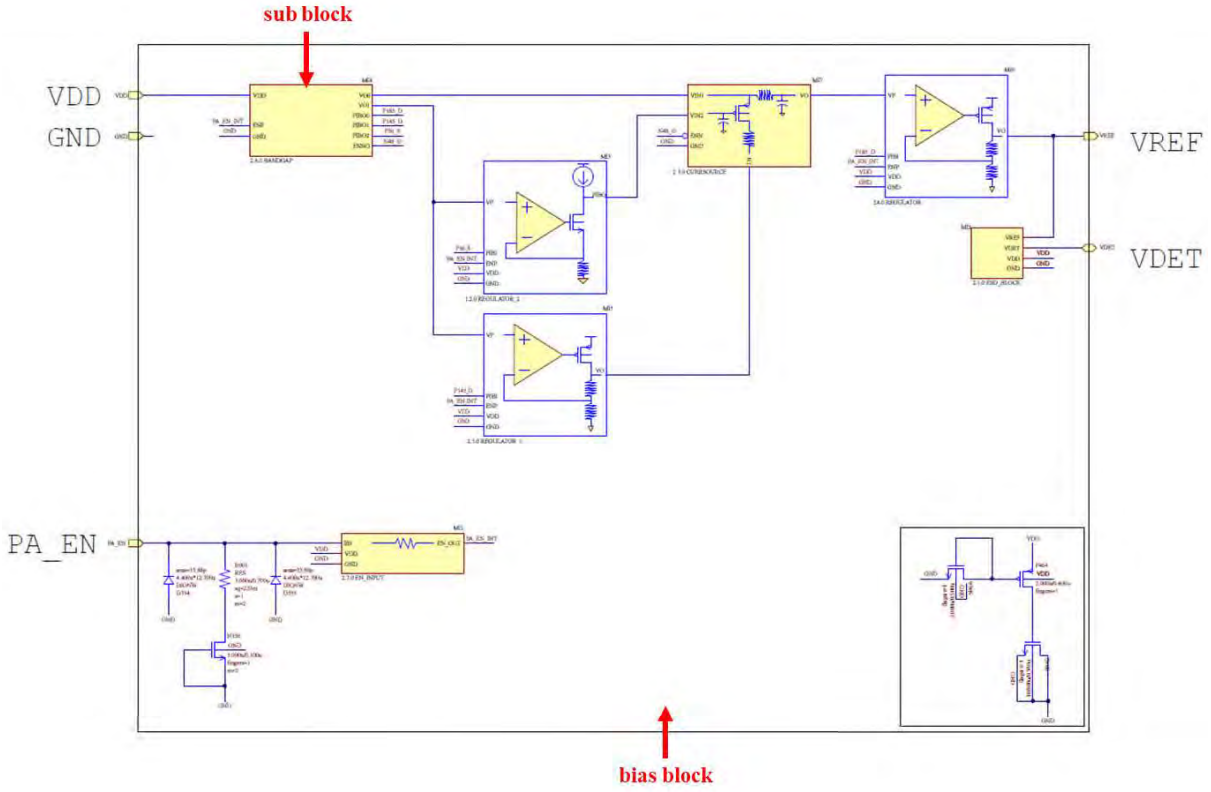
[3] *See* https://perma.cc/DA7F-4CED.

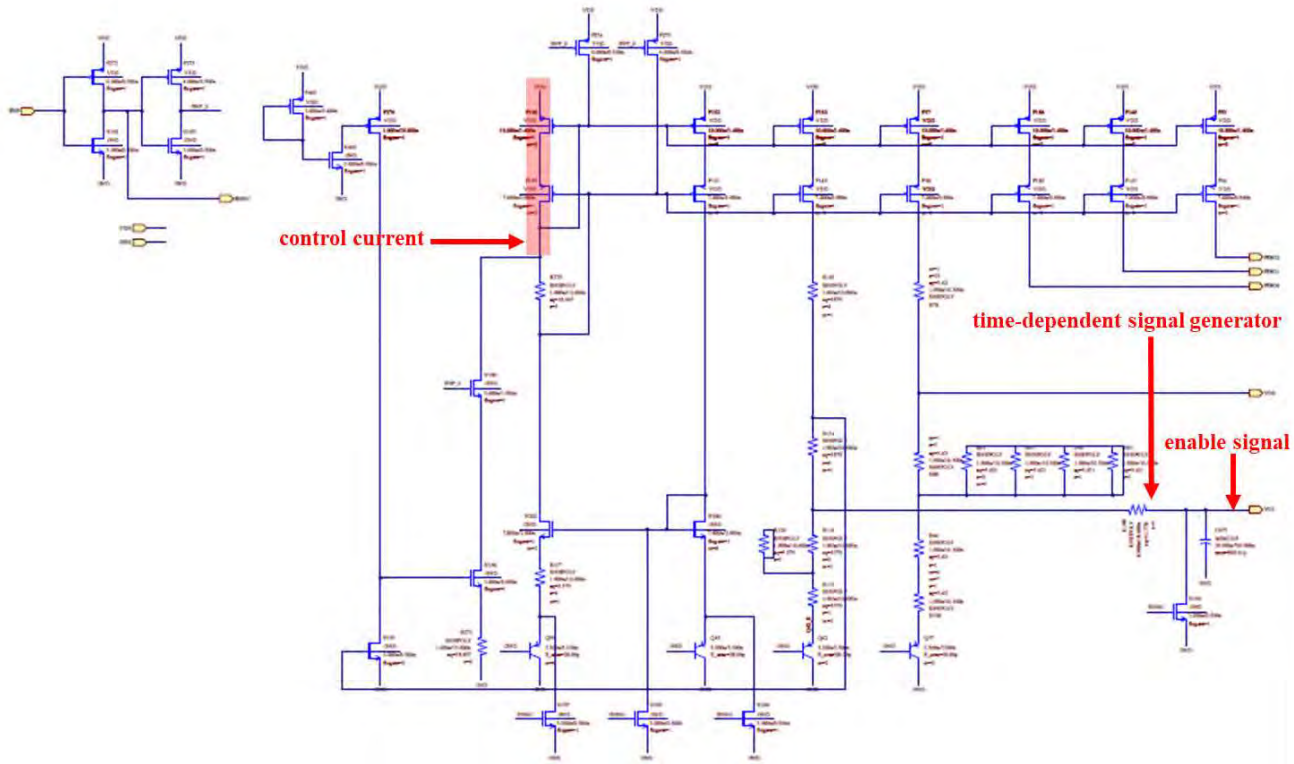


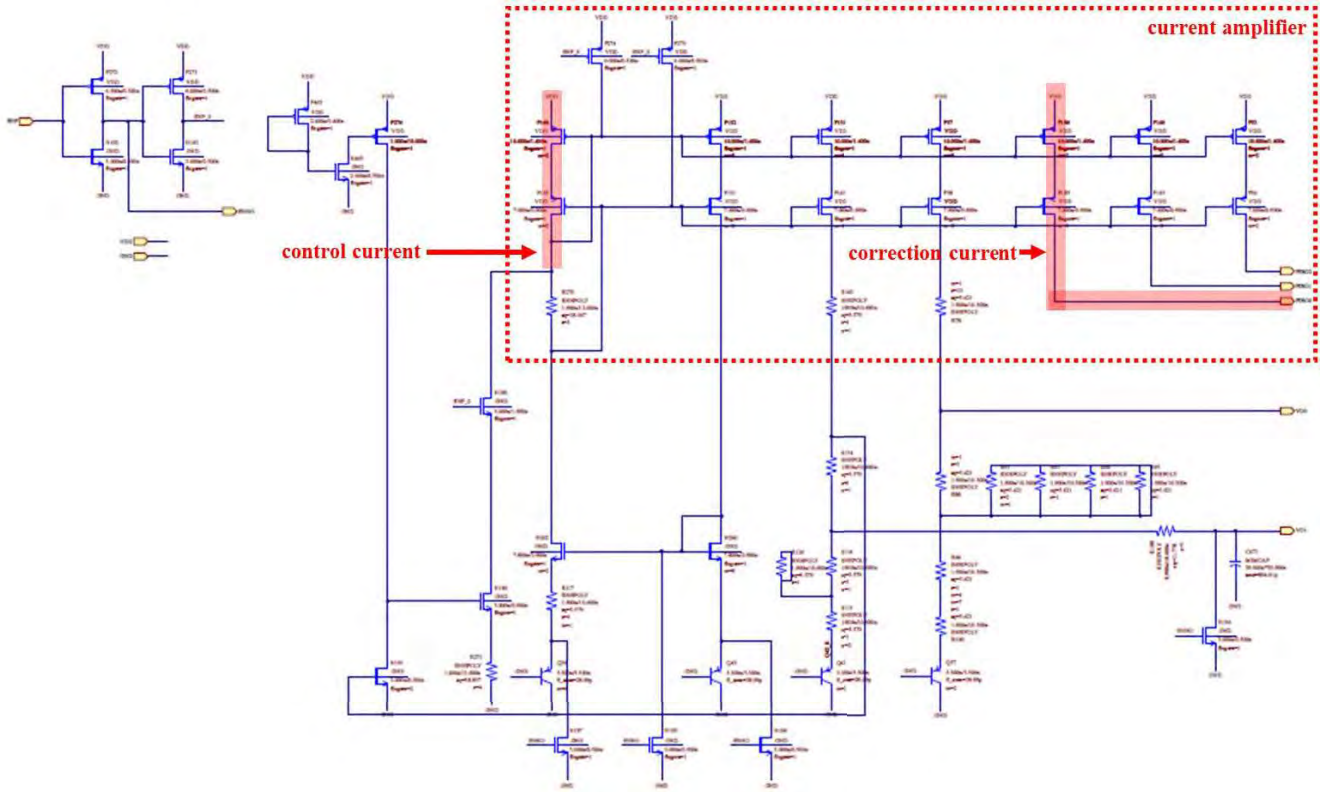
See, e.g., photo of KCT8539S showing three dies, including a die for the bias block and a die for the power amplifier of the power amplifier system

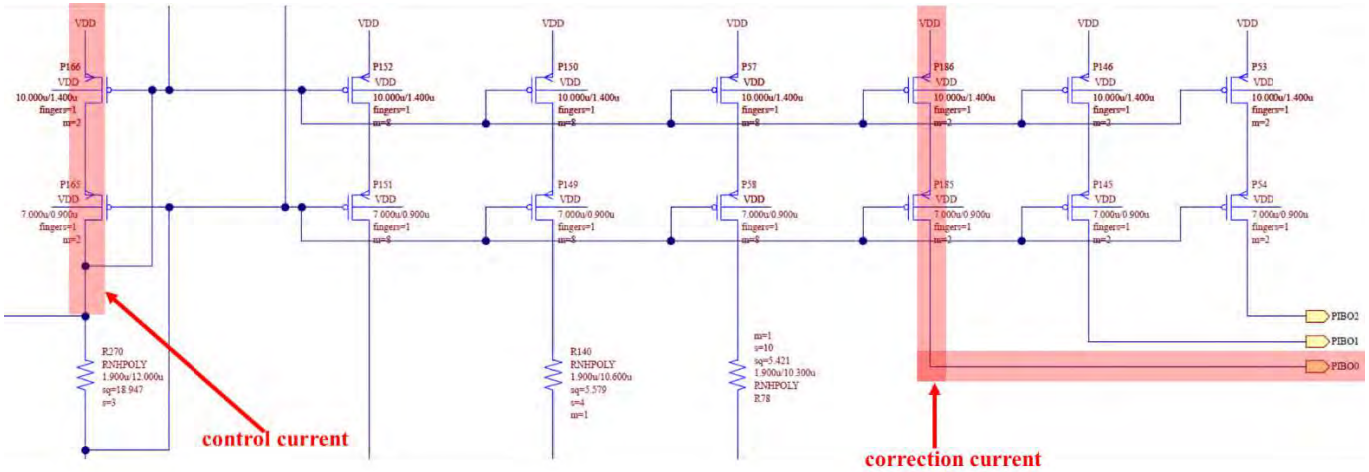
The image below shows the power amplifier and the bias block within the power amplifier system in another angle for the KCT8539S. The bias block is coupled to the power amplifier so that the bias block

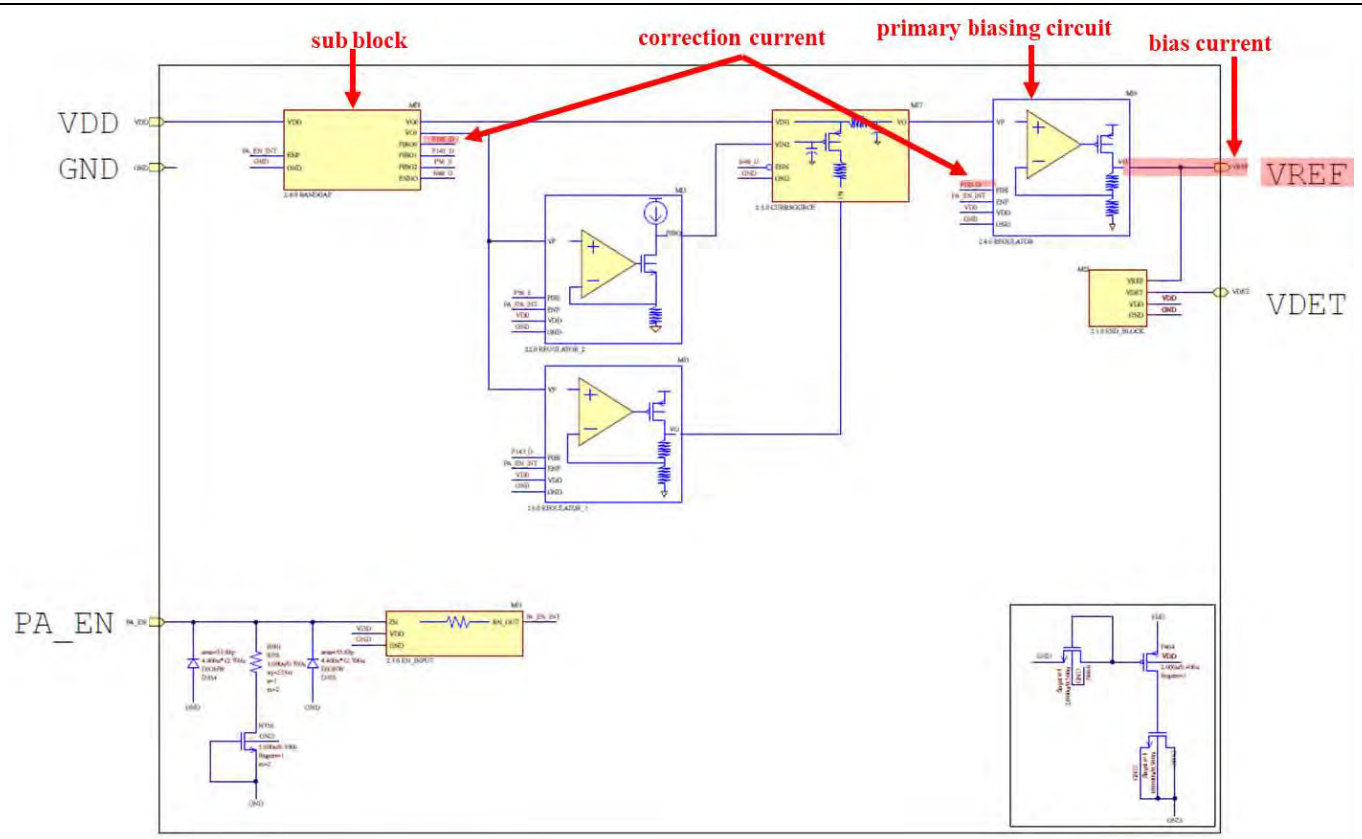
	biases the power amplifier using a bias current through a wire bond connecting a "VREF" port (as indicated by the corresponding label below) of the bias block to the power amplifier.  *See, e.g.*, photo of KCT8539S showing three dies, including a die for the bias block and a die for the power amplifier of the power amplifier system

	See also elements 1[C]-1[E] (showing details of the bias circuit).
1[C] the bias block including a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current,	The KCT8539S includes the bias block including a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current. For example, the reverse engineered schematic below is for the bias block (as indicated by the corresponding label below) in the KCT8539S. It includes a sub block (as indicated by the corresponding label below). The sub block includes a time-dependent signal generator.  *See, e.g.*, reverse engineered schematic of the bias block of KCT8539S

	The reverse engineered schematic below for the KCT8539S shows the internal details of the sub block set forth above. This schematic includes a time-dependent signal generator (as indicated by the corresponding label below). This time-dependent signal generator is configured to shape an enable signal (as indicated by the corresponding label below) of the power amplifier to generate a control current (as indicated by the corresponding label below). The time-dependent signal generator shapes the enable signal to generate the control current in that the enable signal is a time-dependent voltage and the control current depends on the enable signal.  *See, e.g.*, reverse engineered schematic of the sub block of KCT8539S
1[D] a current amplifier configured	In the KCT8539S, the bias block includes a current amplifier configured to amplify the control current to generate a correction current.

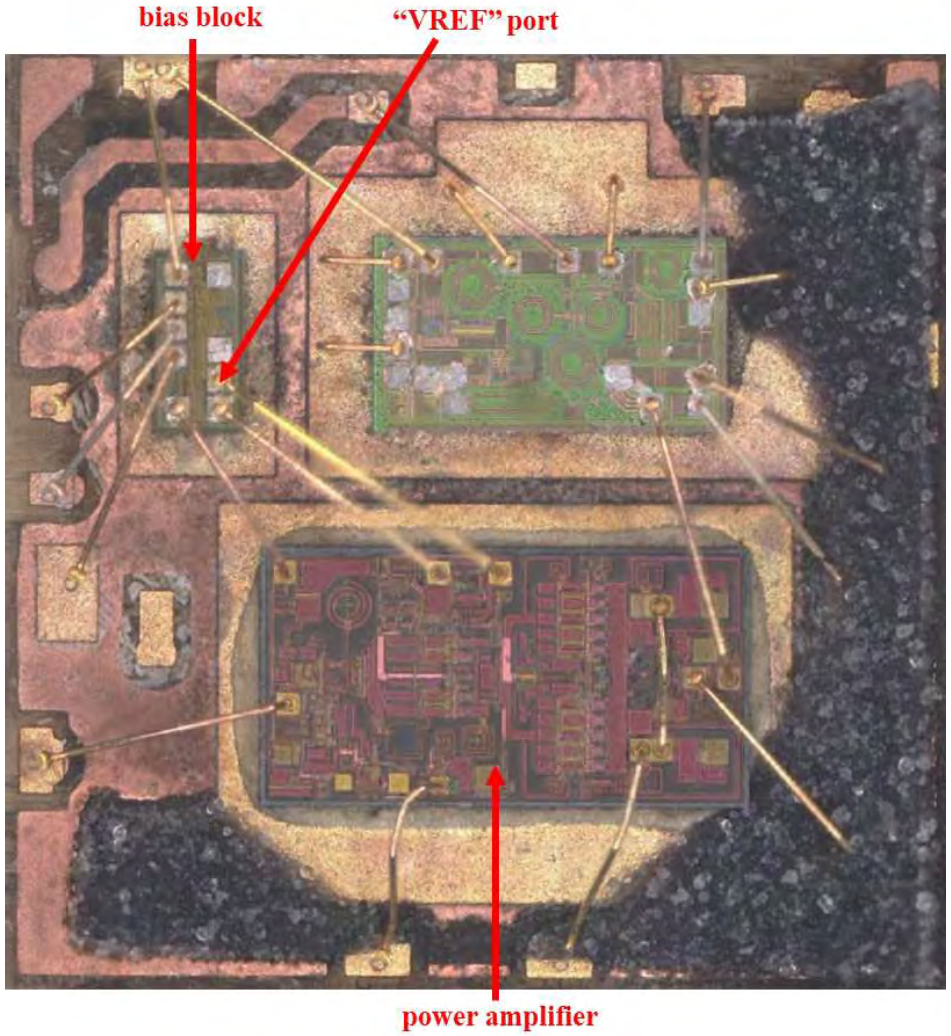
to amplify the control current to generate a correction current,	For example, as shown by the reverse engineered schematic below for the sub block of the KCT8539S, the bias block includes a current amplifier (as indicated by the corresponding label below). The current amplifier is configured to amplify the control current to generate a correction current (as indicated by the corresponding label below). The dashed box with the label below is one example of a current amplifier that amplifies the control current to generate the correction current.  *See, e.g.*, reverse engineered schematic of the sub block of KCT8539S The schematic below for the KCT8539S is an enlarged view of a portion of the current amplifier identified above, which is a current mirror configured to amplify the control current to generate the correction current. As set forth in the '101 patent, a current mirror can have any suitable gain. *See* '101 patent,

	11:39-45. For example, the current mirror in KCT8539S is configured to amplify the control current by a factor of about 1, based on the multiple numbers designated in the schematic below (e.g., "m=2" for the control current and "m=2" for the correction current).  *See, e.g.*, enlarged portion of reverse engineered schematic of the sub block of KCT8539S
1[E] and a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current,	In the KCT8539S, the bias block includes a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current. For example, as shown in the reverse engineered schematic for the KCT8539S below, a primary biasing circuit (as indicated by the corresponding label below) is configured to generate a bias current (as indicated by the corresponding label below) for the power amplifier based at least partly on the correction current.



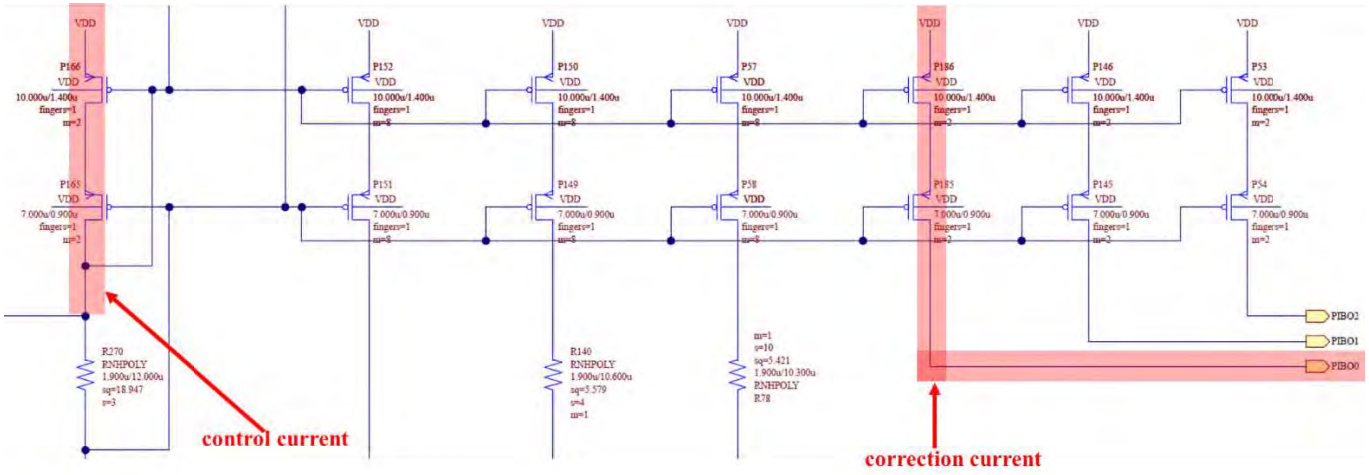
See, e.g., reverse engineered schematic of the bias block of KCT8539S

The bias block biases the power amplifier using the bias current through a wire bond connecting a "VREF" port (as highlighted above and indicated by the corresponding label below) of the bias block to the power amplifier.

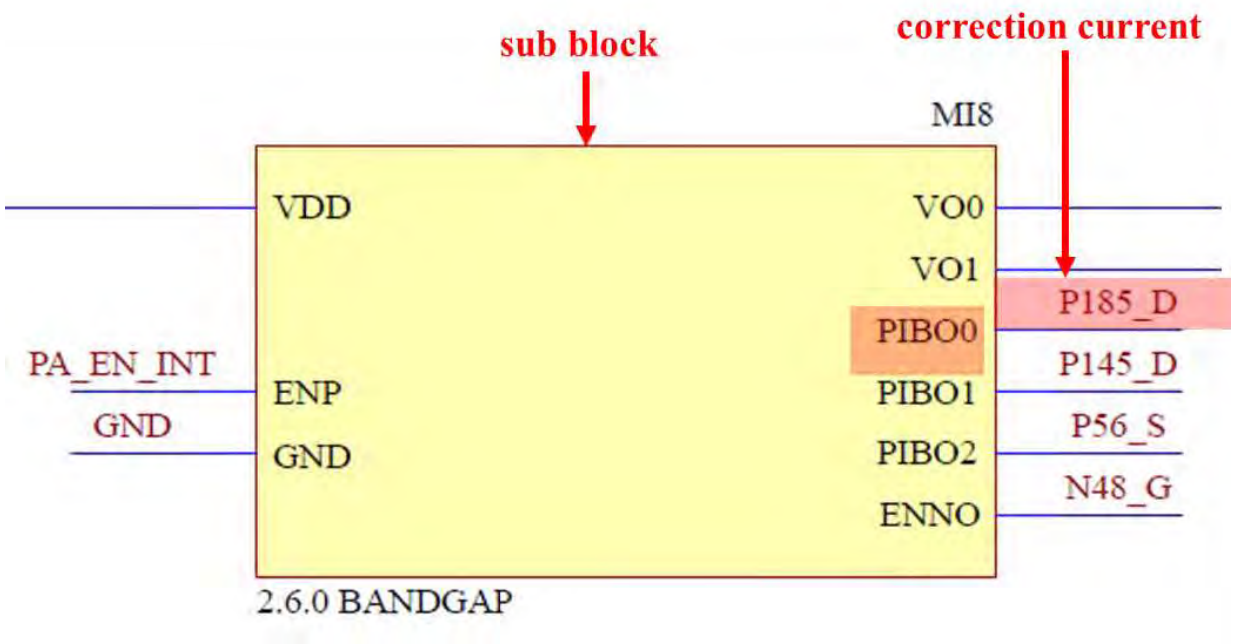


See, e.g., photo of KCT8539S showing three dies, including a die for the bias block and a die for the power amplifier of the power amplifier system

The correction current is output by the "PIBO0" port of the sub block including the time-dependent signal generator, as shown by the reverse engineered schematics below.

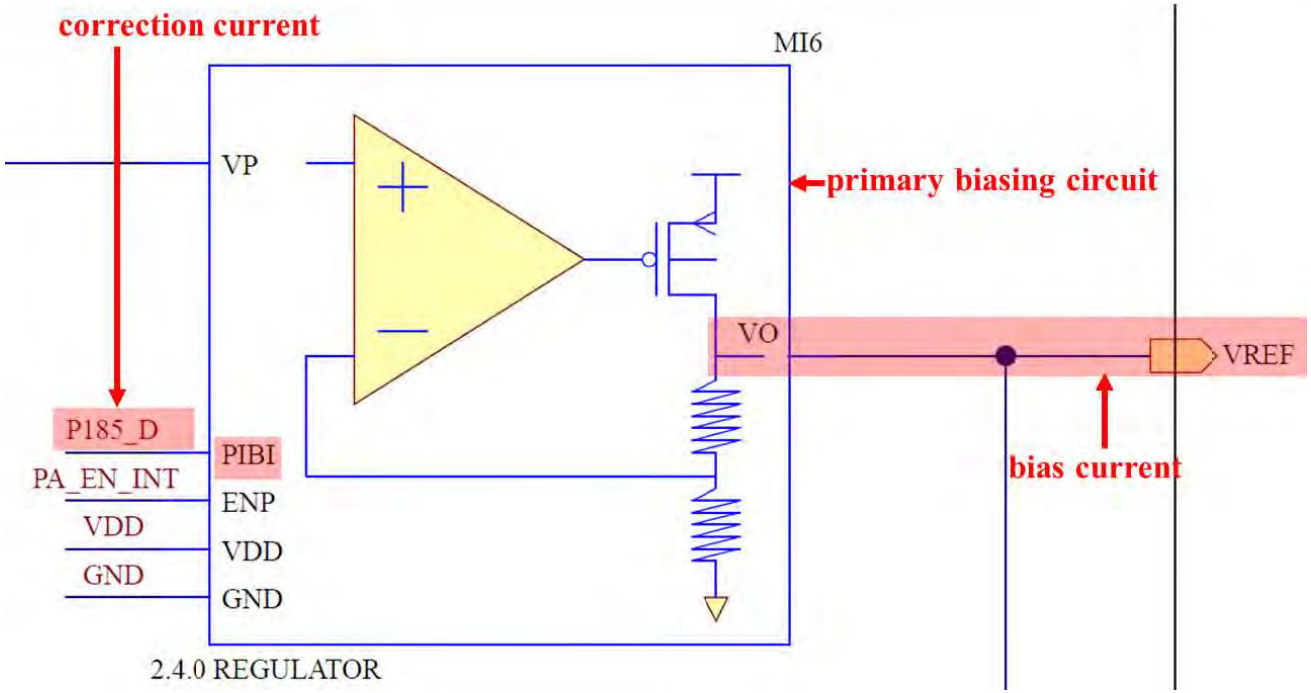


See, e.g., enlarged portion of reverse engineered schematic of the sub block of KCT8539S



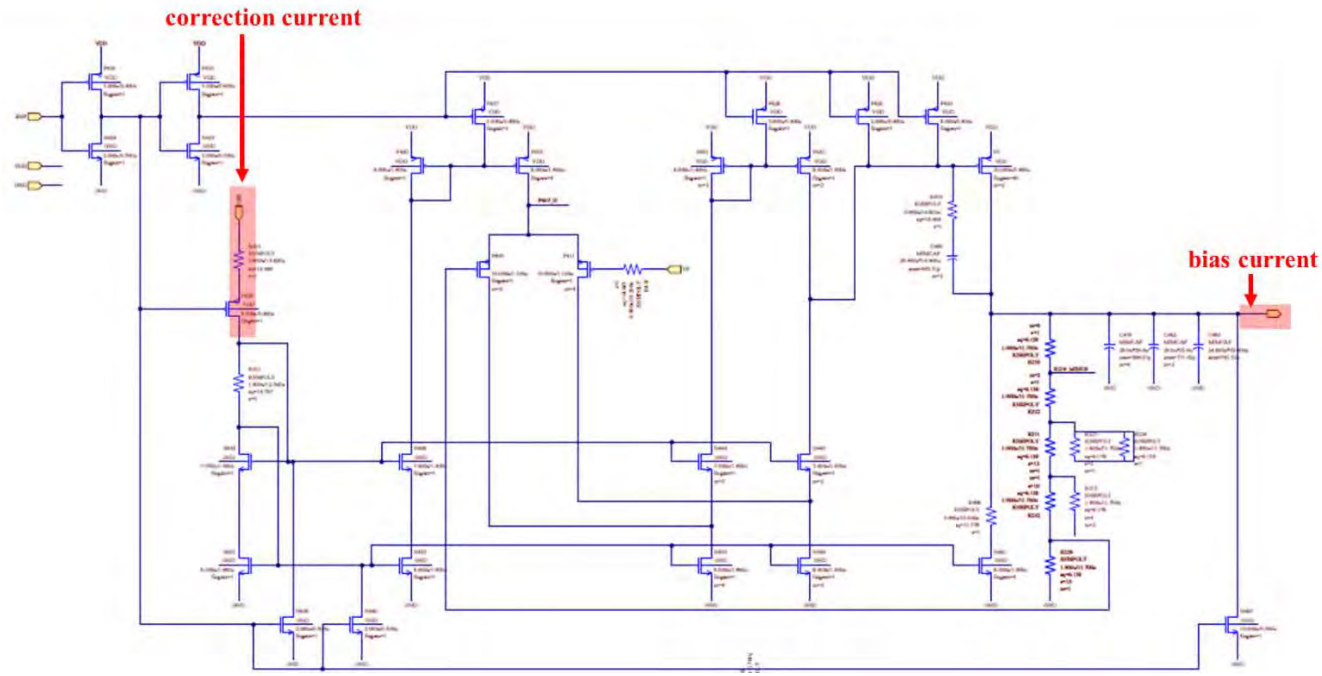
See, e.g., enlarged portion of reverse engineered schematic of the bias block of KCT8539S

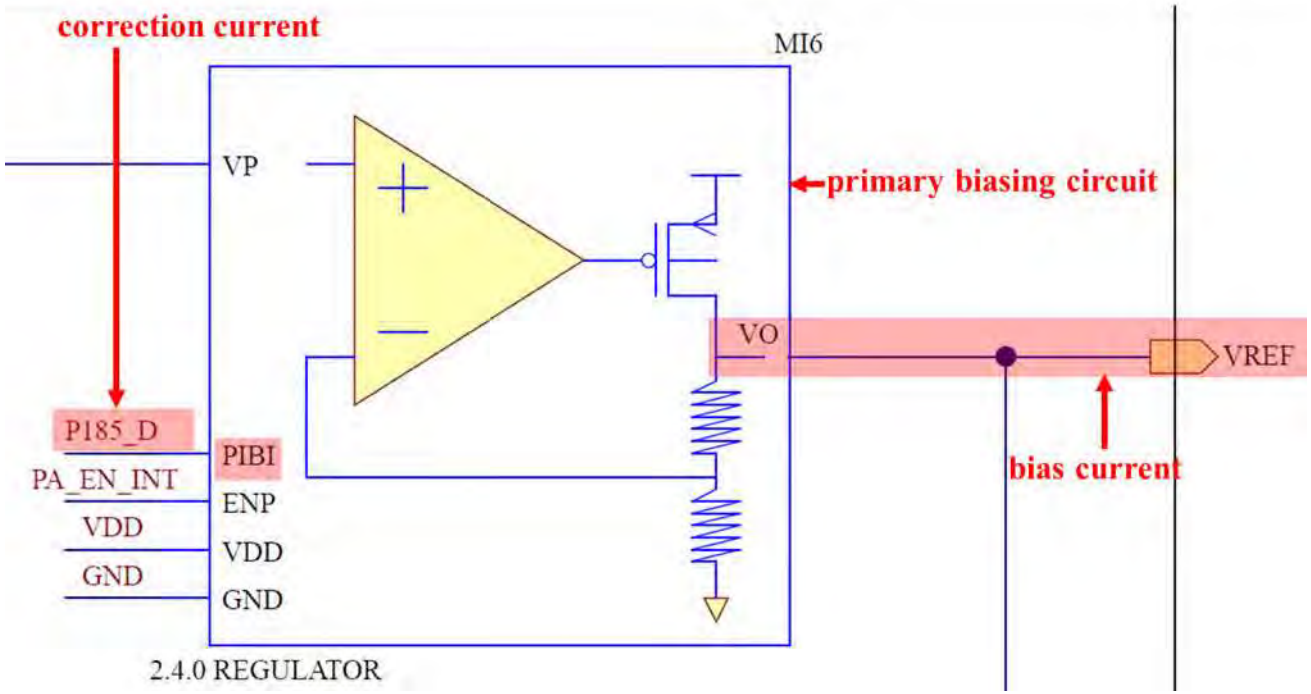
The "PIBO0" port of the sub block (shown above and as corresopnding to P185_D) including the time-dependent signal generator is connected to the "PIBI" port of the primary biasing circuit (as indicated by the corresponding label below showing P185_D connecting to PIBI), as shown by the schematic below.



See, e.g., enlarged portion of reverse engineered schematic of the bias block of KCT8539S

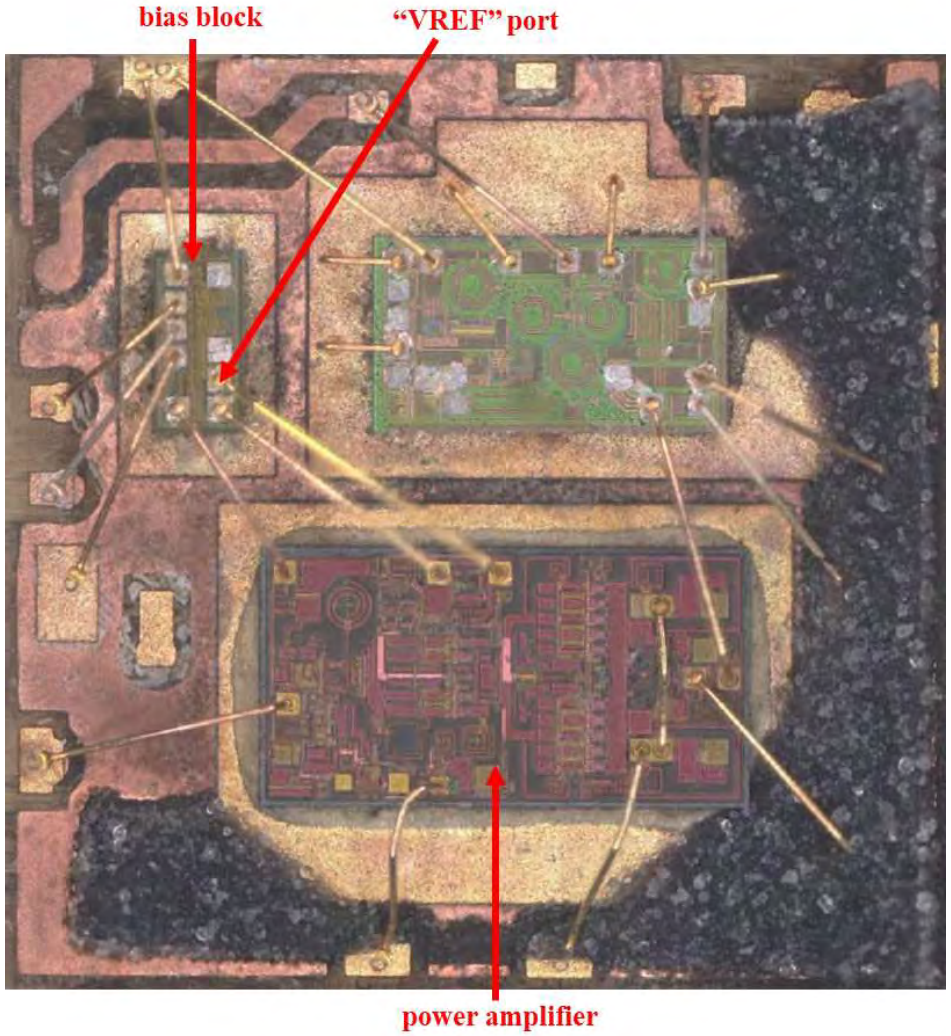
As shown by the schematic below for the primary biasing circuit of the KCT8539S, the primary biasing circuit takes in the correction current as an input and generates the bias current for the power amplifier (as set forth above) based at least partly on the correction current.

	 *See, e.g.*, reverse engineered schematic of the primary biasing circuit of KCT8539S
1[F] the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled,	In the KCT8539S, the bias current is configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled. For example, the bias current is output by the "VREF" port of the bias block, as shown by the reverse engineered schematic for the KCT8539S below.

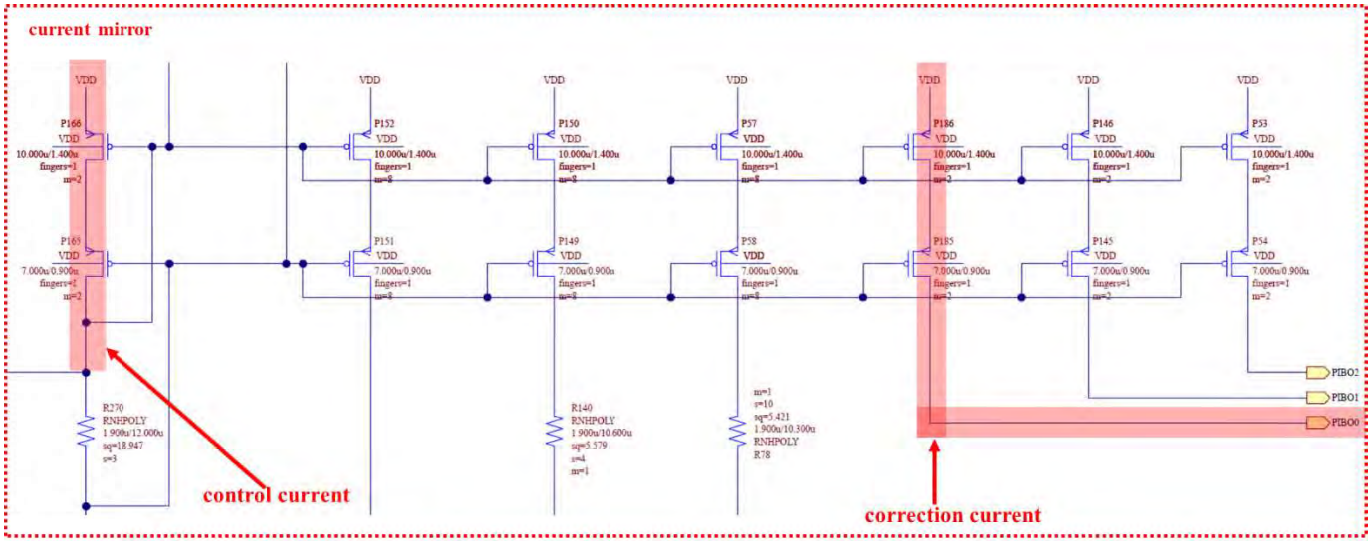


See, e.g., enlarged portion of reverse engineered schematic of the bias block of KCT8539S

This bias current is input to the power amplifier for biasing the power amplifier to provide a suitable gain, including to correct for a variation in gain of the power amplifier when the power amplifier is enabled. As shown by the image below, the "VREF" port of the bias block is coupled to the die for the power amplifier via a wire bond.



See, e.g., photo of KCT8539S showing three dies, including a die for the bias block and a die for the power amplifier of the power amplifier system

1[G] the current amplifier including a current mirror.	In the KCT8539S, as shown by the reverse engineered schematic below, the current amplifier in the bias block includes a current mirror. The dashed box with the label below is one example of a current mirror that is included in the current amplifier.  *See, e.g.*, enlarged portion of reverse engineered schematic of the sub block of KCT8539S For example, as explained in 1[D], the current amplifier in the bias block includes a current mirror configured to amplify the control current by a factor of about 1.
17[pre] A method of biasing a power amplifier, the method comprising:	To the extent the preamble of claim 17 is limiting, the KCT8539S performs a method of biasing a power amplifier. For example, as explained in 1[pre] through 1[B], the KCT8539S includes a bias block for biasing a power amplifier.
17[A] shaping an enable signal using a time-dependent signal	The KCT8539S shapes an enable signal using a time-dependent signal generator to generate a control current.

generator to generate a control current;	For example, as explained in 1[C], the KCT8539S includes a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current.
17[B] amplifying the control current using a current mirror of a current amplifier to generate a correction current; and	The KCT8539S amplifies the control current using a current mirror of a current amplifier to generate a correction current. For example, as explained in 1[D], the KCT8539S includes a current amplifier configured to amplify the control current to generate a correction current. As explained in 1[G], the current amplifier includes a current mirror that amplifies the control current to generate a correction current.
17[C] generating a bias current for a power amplifier using a primary biasing circuit, the primary biasing circuit configured to use the correction current to correct for a variation in gain of the power amplifier when the power amplifier is enabled.	The KCT8539S generates a bias current for a power amplifier using a primary biasing circuit, the primary biasing circuit configured to use the correction current to correct for a variation in gain of the power amplifier when the power amplifier is enabled. For example, as explained in 1[E], the KCT8539S includes a primary biasing circuit used to generate a bias current for the power amplifier based at least partly on the correction current. As explained in 1[F], the bias current is configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled. Since the bias current is at least partly based on the correction current, the primary biasing circuit is configured to use the correction current to correct for a variation in gain of the power amplifier when the power amplifier is enabled.
21[pre] A bias circuit for biasing a power amplifier, the bias circuit comprising:	To the extent the preamble of claim 21 is limiting, the KCT8539S includes a bias circuit for biasing a power amplifier. For example, as explained in 1[pre] through 1[B], the KCT8539S includes a bias block, which is a bias circuit, for biasing a power amplifier.
21[A] a time-dependent signal generator configured to shape an enable	The KCT8539S includes the bias circuit comprising a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current.

signal of the power amplifier to generate a control current;	For example, as explained in 1[C], the KCT8539S includes a bias circuit including a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current.
21[B] a current amplifier configured to amplify the control current to generate a correction current,	The KCT8539S includes the bias circuit comprising a current amplifier configured to amplify the control current to generate a correction current. For example, as explained in 1[D], the bias circuit in the KCT8539S includes a current amplifier configured to amplify the control current to generate a correction current.
21[C] the current amplifier including a current mirror; and	In the KCT8539S, the current amplifier includes a current mirror. For example, as explained in 1[G], the current amplifier in the KCT8539S includes a current mirror.
21[D] a primary biasing block configured to generate a bias current for the power amplifier based at least partly on the correction current,	The KCT8539S includes the bias circuit comprising a primary biasing block configured to generate a bias current for the power amplifier based at least partly on the correction current. For example, as explained in 1[E], the bias circuit in the KCT8539S includes a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current.
21[E] the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled.	In the KCT8539S, the bias current is configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled. For example, as explained in 1[F], the bias current is input to the power amplifier for biasing the power amplifier to provide a suitable gain, including to correct for a variation in gain of the power amplifier when the power amplifier is enabled.

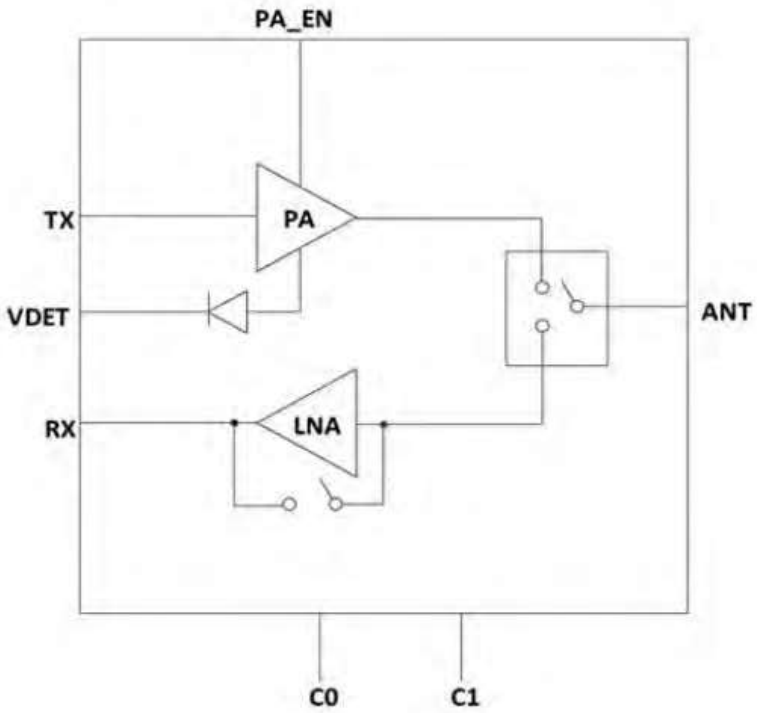
EXHIBIT 11

EXHIBIT 11
SKYWORKS SOLUTIONS, INC.'S INFRINGEMENT CHART
KCT8547HE
U.S. Patent No. 8,717,101
Independent Claims 1, 17, and 21

Skyworks Solutions, Inc. ("Skyworks") provides this exemplary claim chart for independent claims 1, 17, and 21 of U.S. Patent No. 8,717,101 (the "'101 patent") applied to Kangxi Communication Technologies (Shanghai) Co., Ltd's and Grand Chip Labs, Inc.'s (collectively, "KCT") KCT8547HE product. The disclosures in this claim chart directed to the KCT8547HE are also more broadly directed to any sale, offer for sale, use, or importation of the KCT8547HE in the U.S., including in an end product such as a wireless router or as a standalone product that is not incorporated in an end product.

The claim chart below demonstrates infringement by comparing each element of the charted claims to corresponding components, aspects, and/or features of the KCT8547HE product. This claim chart is not intended to constitute an expert report on infringement. This claim chart includes information provided by way of example, and not by way of limitation.

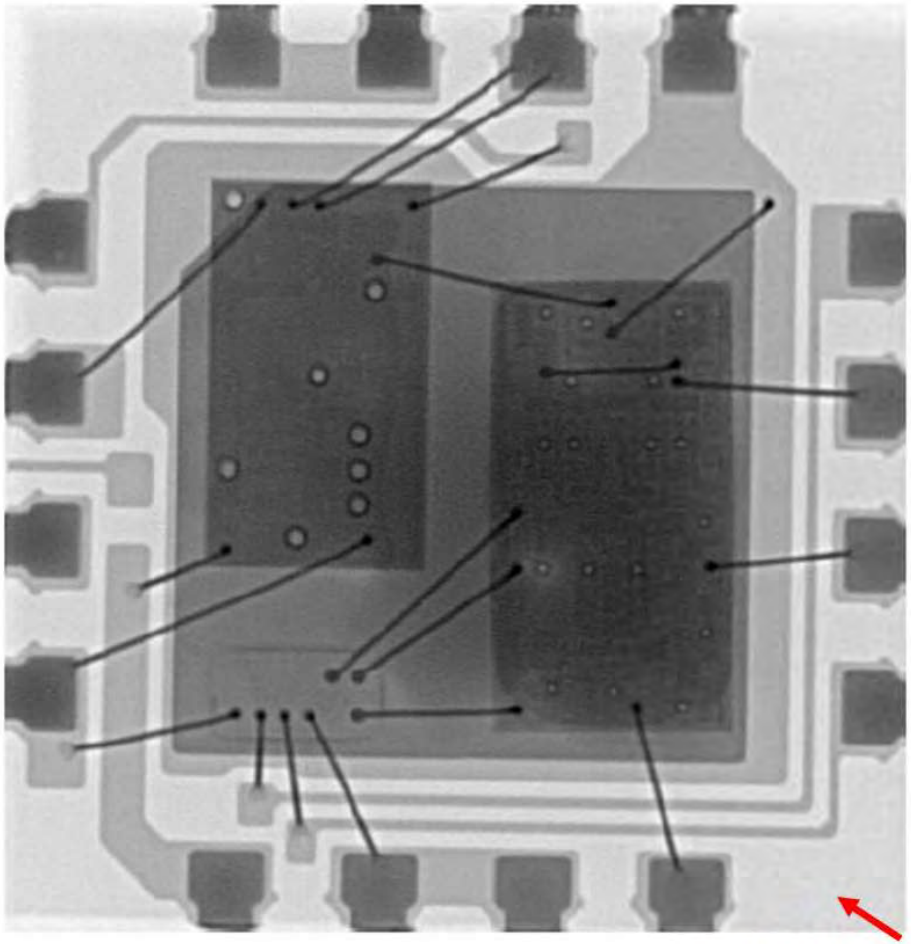
The analysis set forth below is based only upon information from publicly available sources regarding the KCT8547HE product. Further analysis of non-public information during fact discovery will likely assist in identifying all infringing features and functionalities used by KCT in the KCT8547HE product. Accordingly, Skyworks reserves the right to supplement this infringement analysis once such information is made available to Skyworks. Further, Skyworks reserves the right to supplement this infringement analysis, as appropriate, upon issuance of an order construing any terms recited in the asserted claims or as other circumstances so merit.

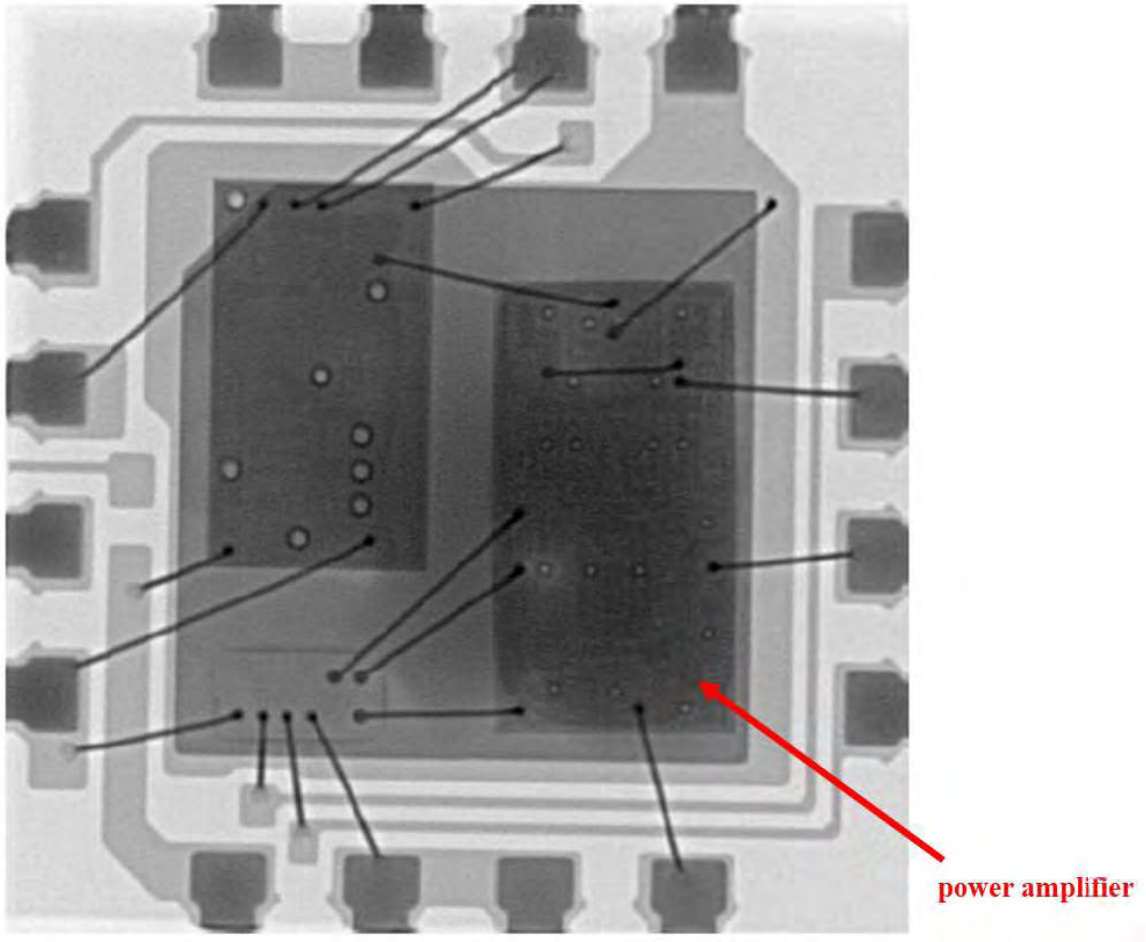
Claims	KCT8547HE
1[pre] A power amplifier system comprising:	To the extent the preamble of claim 1 is limiting, the KCT8547HE includes a power amplifier system. The KCT8547HE is a product for Wi-Fi connectivity. For example, the following image for the KCT8547HE is a simplified block diagram for this product.[1]  *See, e.g.*, simplified block diagram for KCT8547HE The KCT8547HE is, according to KCT, "a highly integrated RF Front-End Integrated Circuit incorporate[ing] key RF functionality needed for IEEE 802.11a/n/ac/ax WLAN systems operating in the

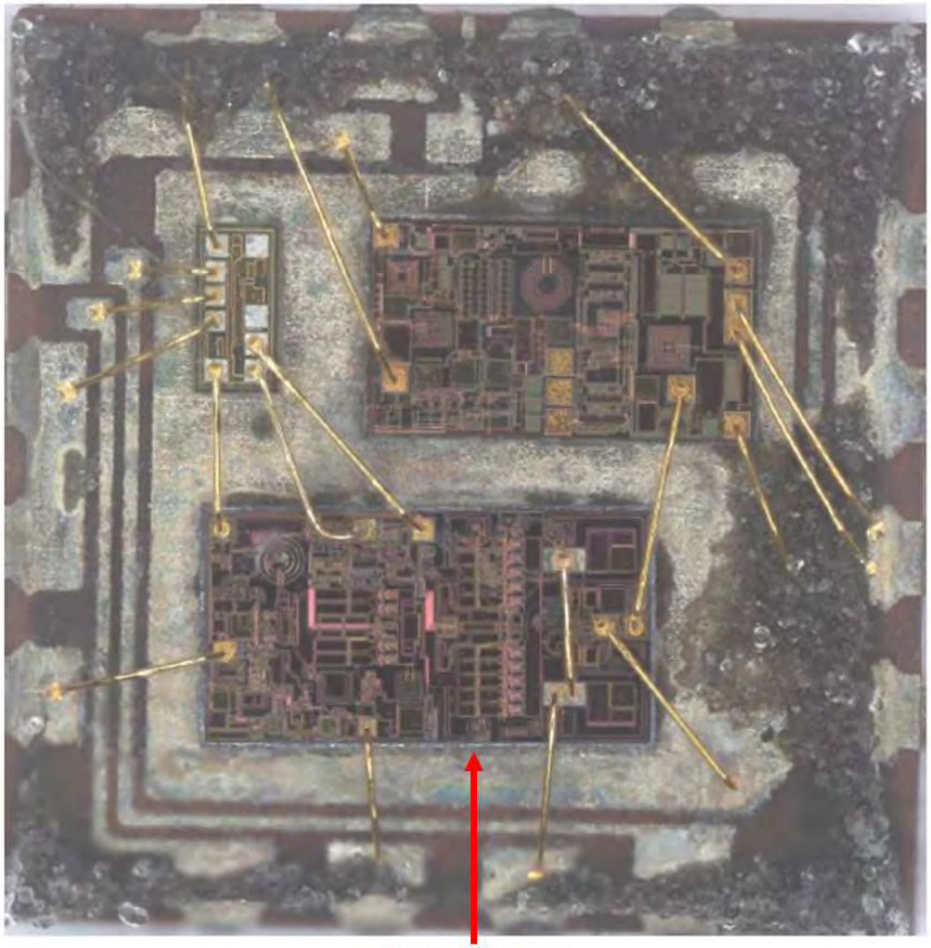
[1] *See* https://perma.cc/GV2Y-HD8A.

	5.15-5.95GHz range. KCT8547HE-1 integrates a high-efficiency high-linearity power amplifier (PA), a low noise amplifier (LNA) with bypass ….”[2] For example, the image below of the KCT8547HE shows a power amplifier system (as indicated by the corresponding label below) within the KCT8547HE.

[2] *See* https://perma.cc/GV2Y-HD8A.

	 *See, e.g.*, photo of KCT8547HE showing three dies of the power amplifier system
1[A] a power amplifier configured to amplify a radio	The KCT8547HE includes a power amplifier configured to amplify a radio frequency (RF) signal. For example, the image of the KCT8547HE below shows a power amplifier (as indicated by the corresponding label below) as part of the power amplifier system.

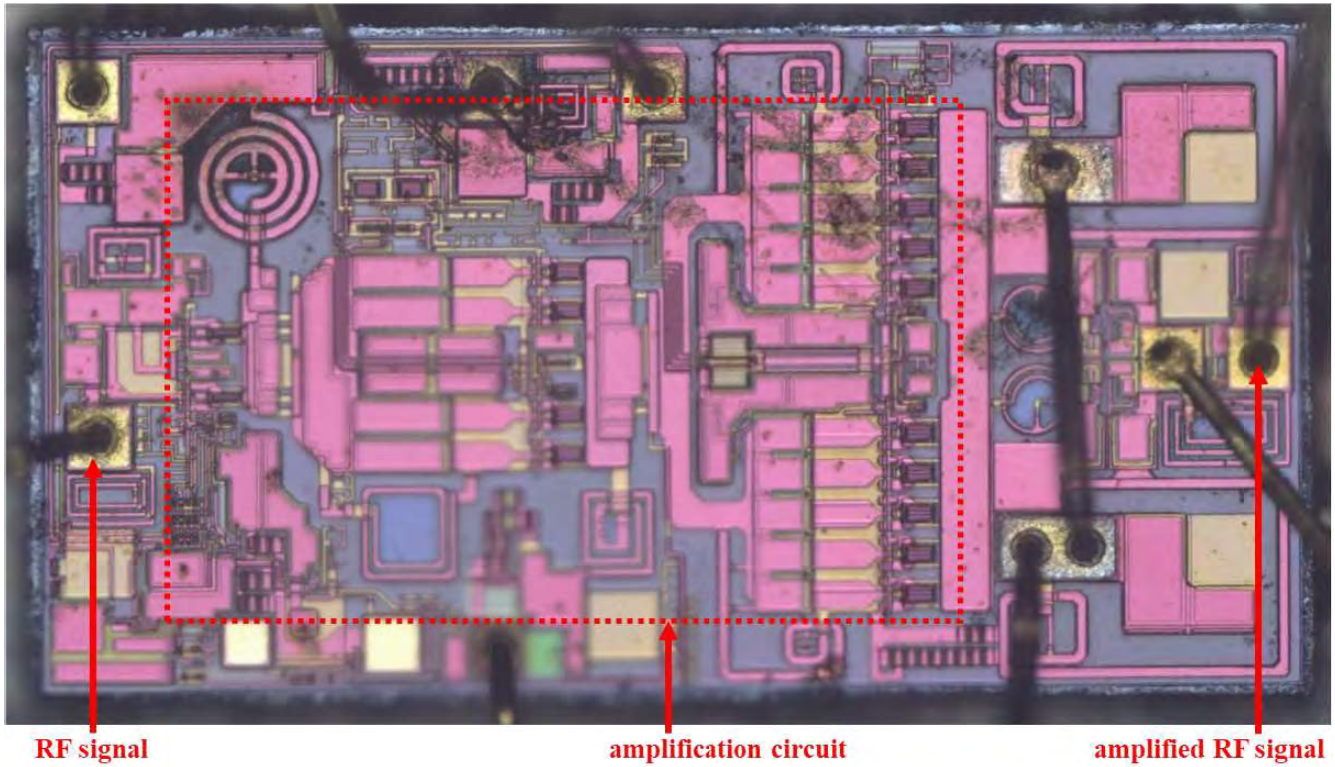
frequency (RF) signal; and	 *See, e.g.*, photo of KCT8547HE showing three dies, including a die for the power amplifier of the power amplifier system The image below shows the die of the power amplifier as part of the power amplifier system for the KCT8547HE.



See, e.g., photo of KCT8547HE showing three dies, including the die for the power amplifier of the power amplifier system

The image below shows an enlarged view of the power amplifier die of the KCT8547HE. The power amplifier in the KCT8547HE is coupled so that it is configured to receive as an input a radio frequency

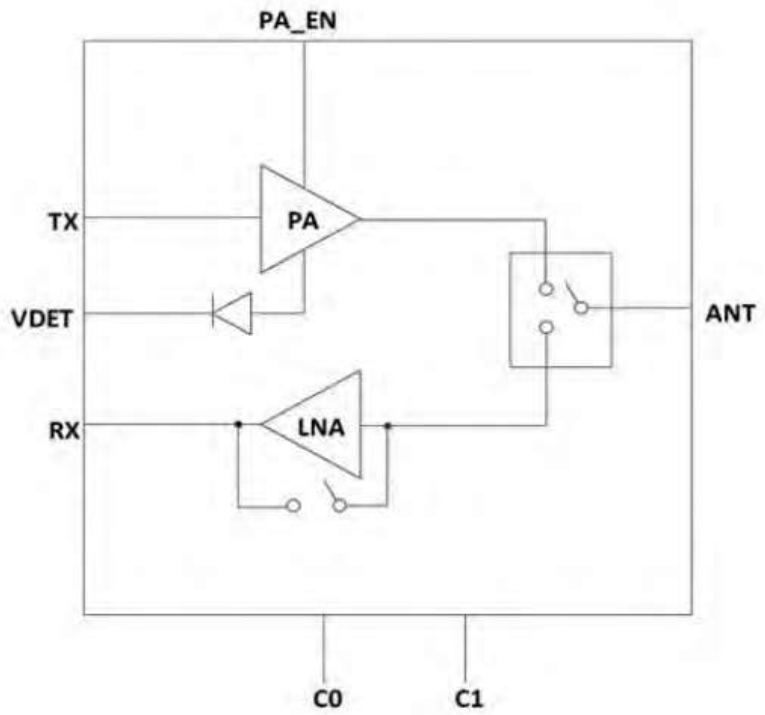
(RF) signal, as labeled below, and amplify the RF signal to output an amplified RF signal, as labeled below. The dashed box with the corresponding label below is one example of an amplification circuit that provides the amplification of the RF signal.

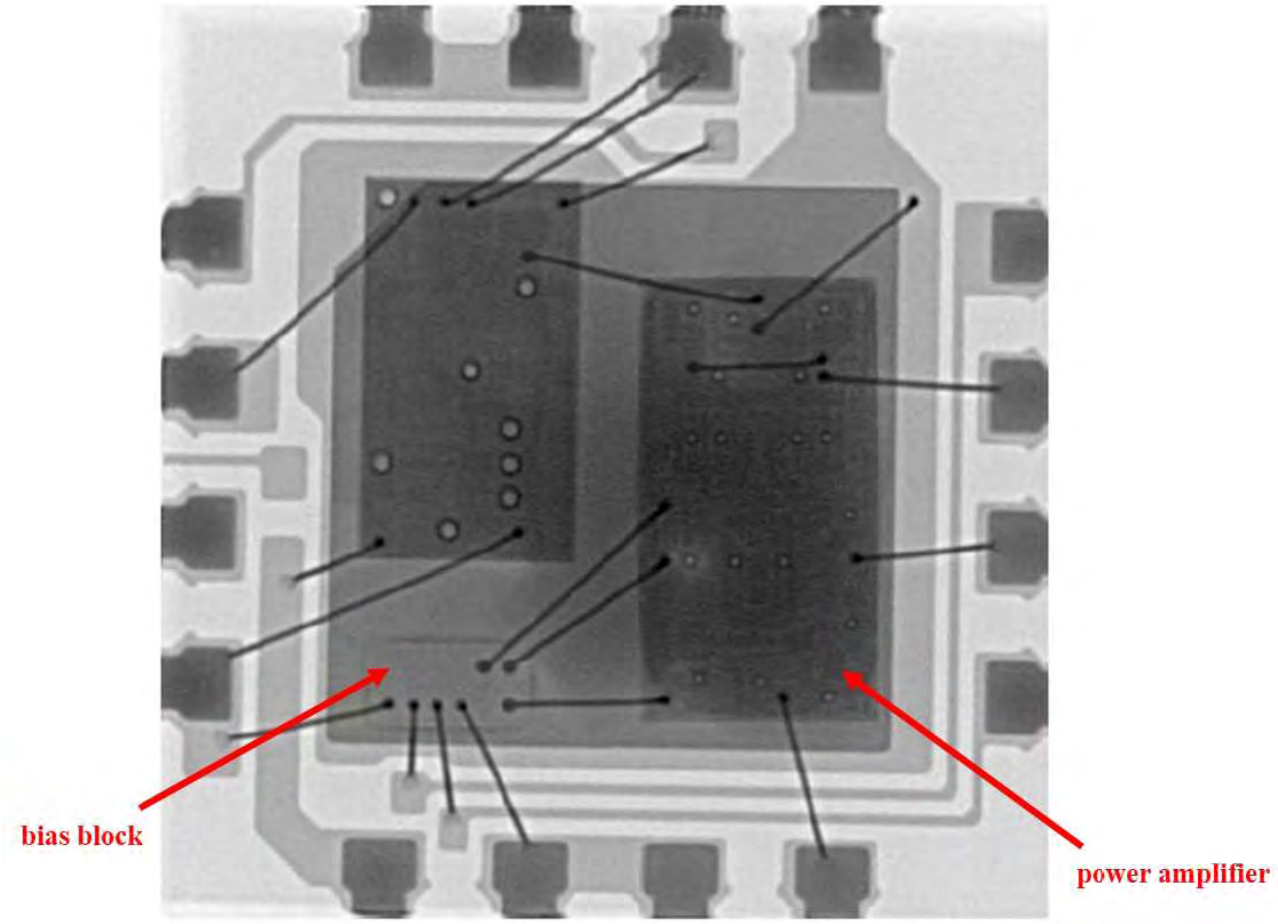


See, e.g., photo of the power amplifier die in KCT8547HE

As shown below in KCT's simplified block diagram for the KCT8547HE, a power amplifier (labelled as "PA") is part of the KCT8547HE product. Specifically, the KCT8547HE "integrates a high-efficiency high-linearity power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated matching network and harmonic filters all in one device."[3]

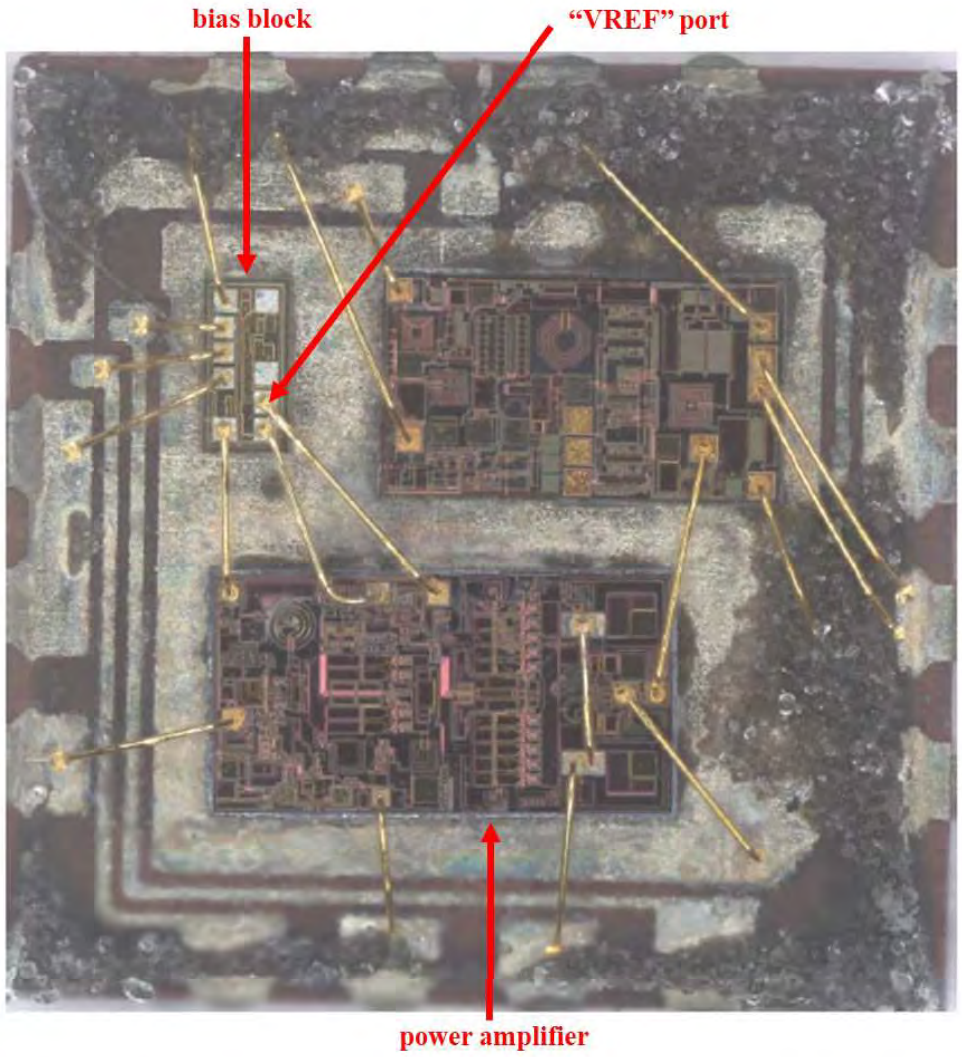
[3] *See* https://perma.cc/GV2Y-HD8A.

	 *See, e.g.*, simplified block diagram for KCT8547HE
1[B] a bias block for biasing the power amplifier,	The KCT8547HE includes a bias block for biasing the power amplifier. For example, the image of the KCT8547HE below shows a bias block (as indicated by the corresponding label below) as part of the power amplifier system.



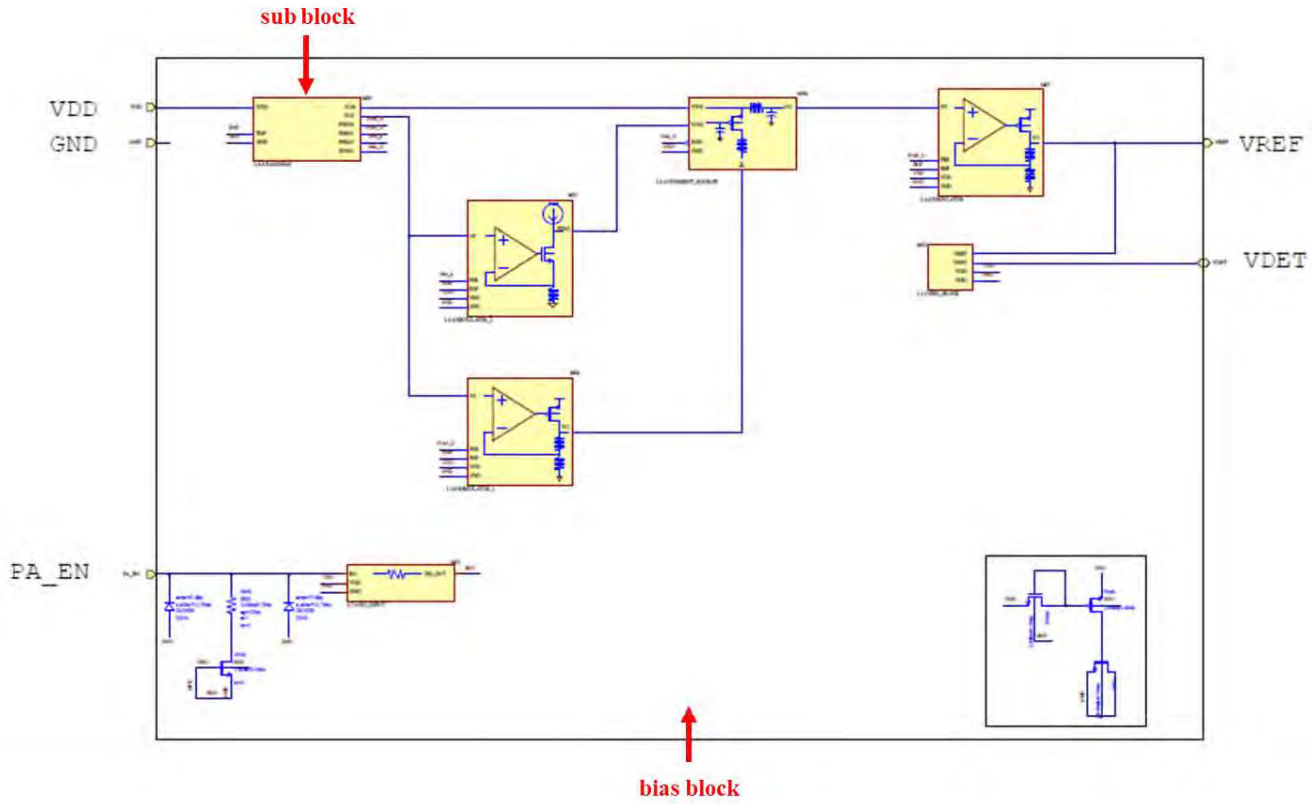
See, e.g., photo of KCT8547HE showing three dies, including a die for the bias block and a die for the power amplifier of the power amplifier system

The image below shows the power amplifier and the bias block within the power amplifier system in another angle for the KCT8547HE. The bias block is coupled to the power amplifier so that the bias block biases the power amplifier using a bias current through a wire bond connecting a "VREF" port (as indicated by the corresponding label below) of the bias block to the power amplifier.

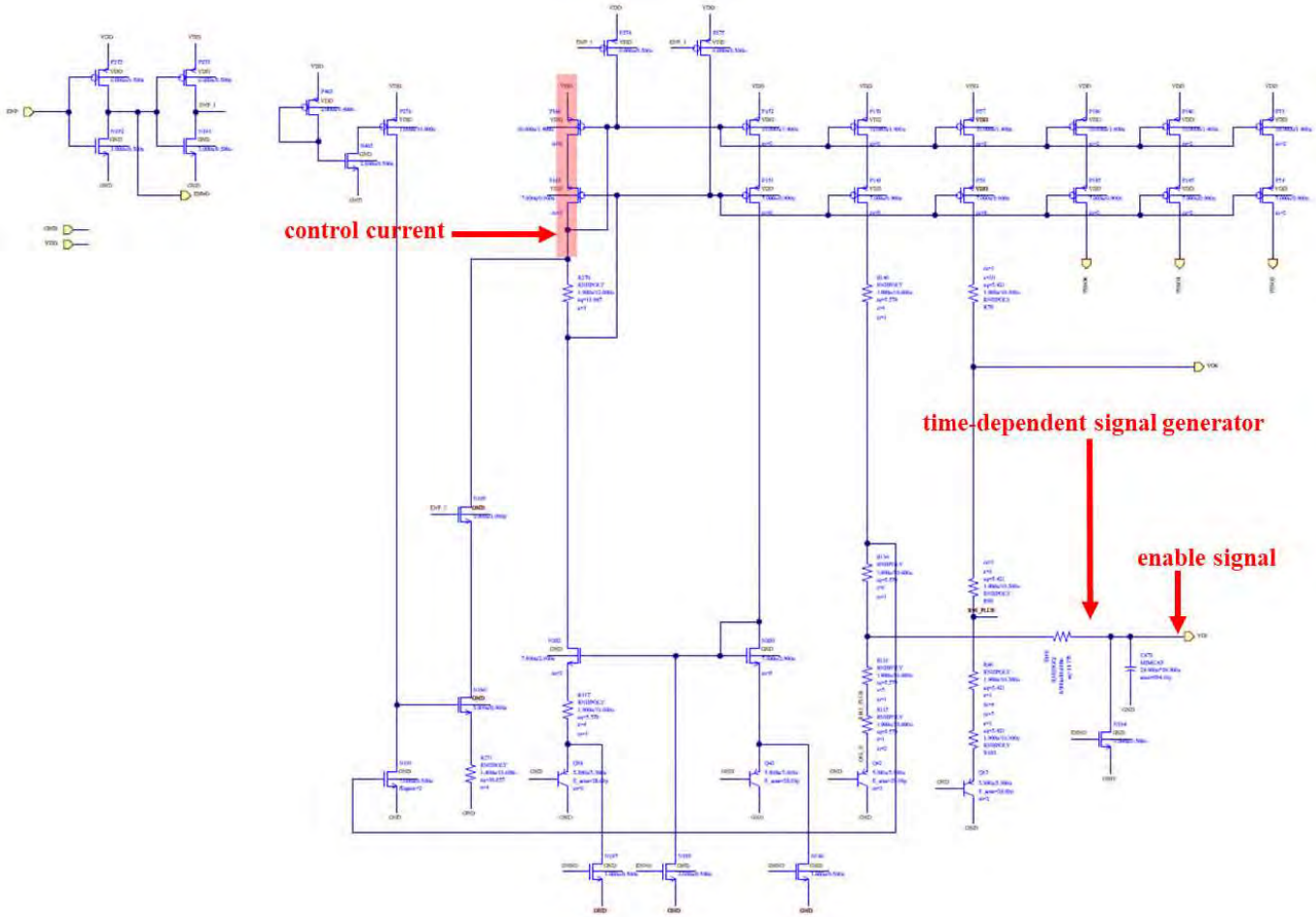


See, e.g., photo of KCT8547HE showing three dies, including a die for the bias block and a die for the power amplifier of the power amplifier system

See also elements 1[C]-1[E] (showing details of the bias circuit).

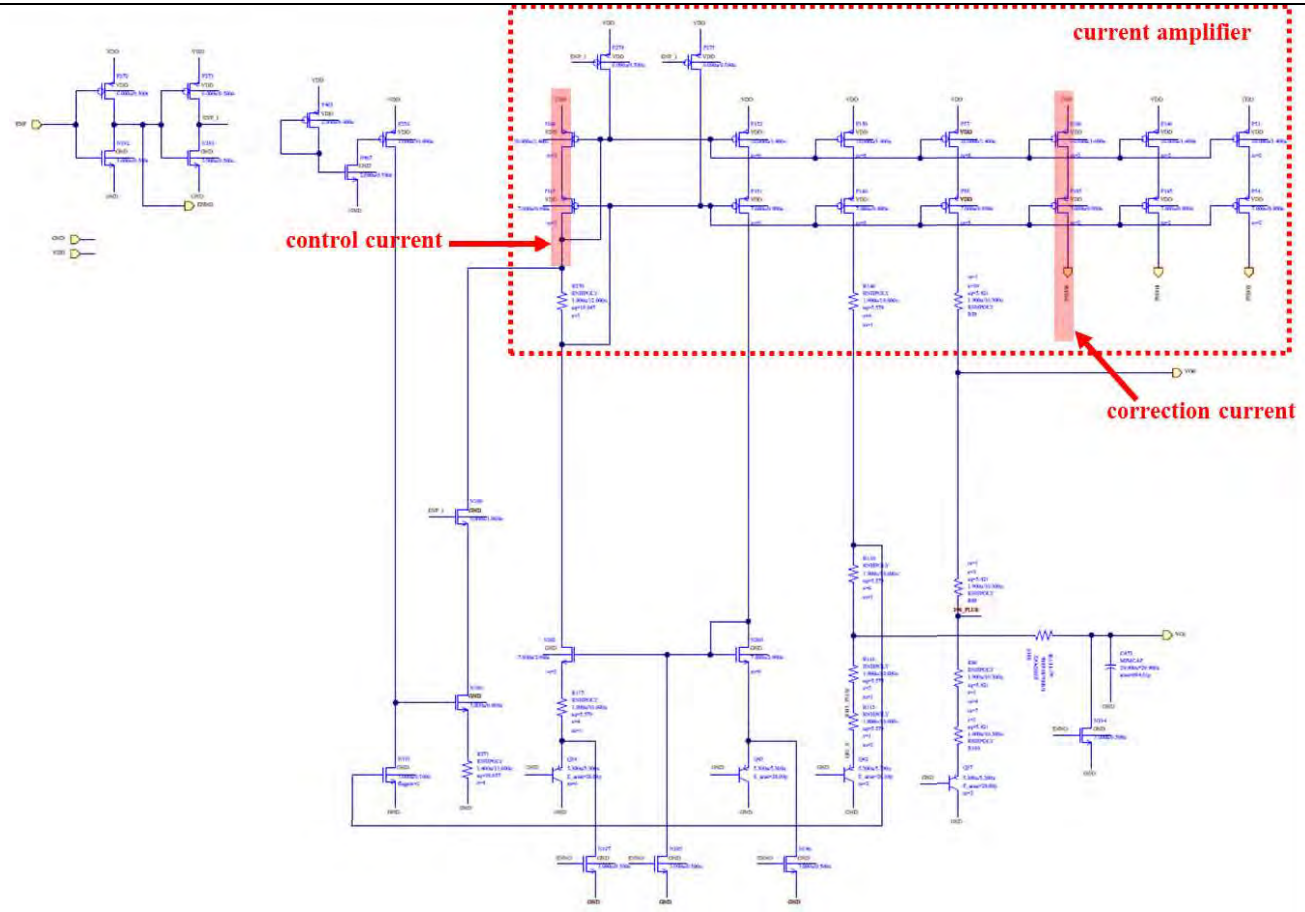
1[C] the bias block including a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current,	The KCT8547HE includes the bias block including a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current. For example, the reverse engineered schematic below is for the bias block (as indicated by the corresponding label below) in the KCT8547HE. It includes a sub block (as indicated by the corresponding label below). The sub block includes a time-dependent signal generator.  *See, e.g.*, reverse engineered schematic of the bias block of KCT8547HE The reverse engineered schematic below for the KCT8547HE shows the internal details of the sub block set forth above. This schematic includes a time-dependent signal generator (as indicated by the

corresponding label below). This time-dependent signal generator is configured to shape an enable signal (as indicated by the corresponding label below) of the power amplifier to generate a control current (as indicated by the corresponding label below). The time-dependent signal generator shapes the enable signal to generate the control current in that the enable signal is a time-dependent voltage and the control current depends on the enable signal.



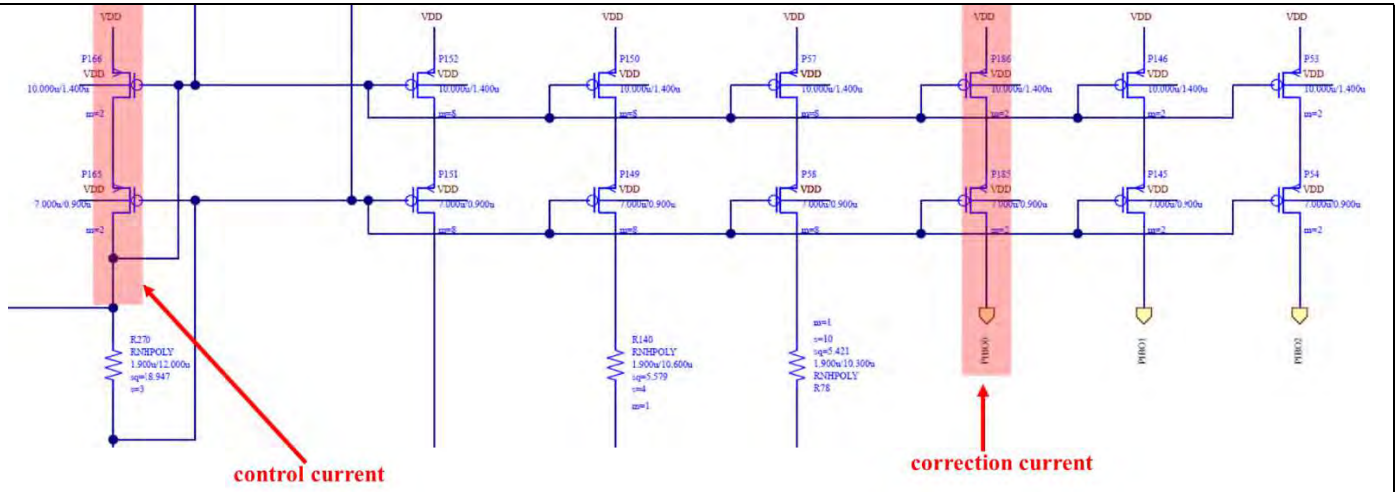
See, e.g., reverse engineered schematic of the sub block of KCT8547HE

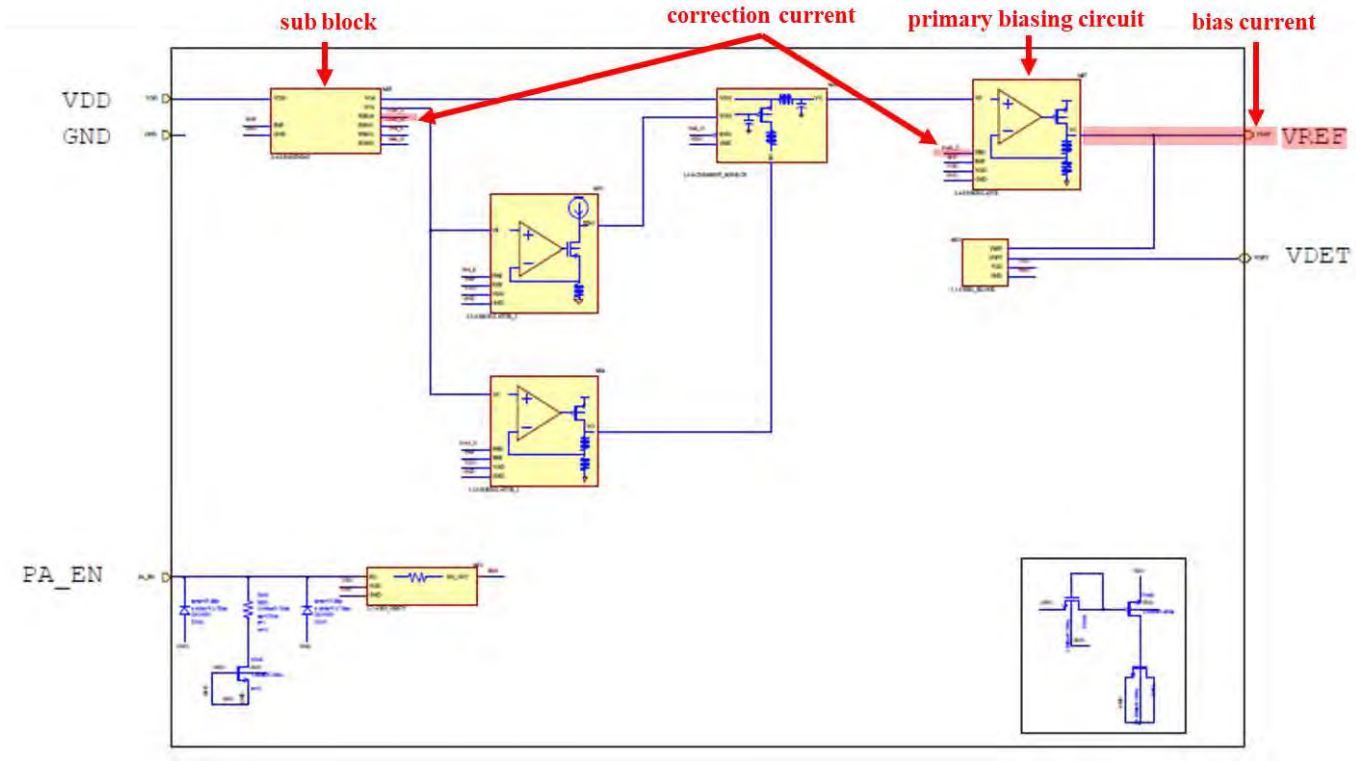
1[D] a current amplifier configured to amplify the control current to generate a correction current,	In the KCT8547HE, the bias block includes a current amplifier configured to amplify the control current to generate a correction current. For example, as shown by the reverse engineered schematic below for the sub block of the KCT8547HE, the bias block includes a current amplifier (as indicated by the corresponding label below). The current amplifier is configured to amplify the control current to generate a correction current (as indicated by the corresponding label below). The dashed box with the label below is one example of a current amplifier that amplifies the control current to generate the correction current.



See, e.g., reverse engineered schematic of the sub block of KCT8547HE

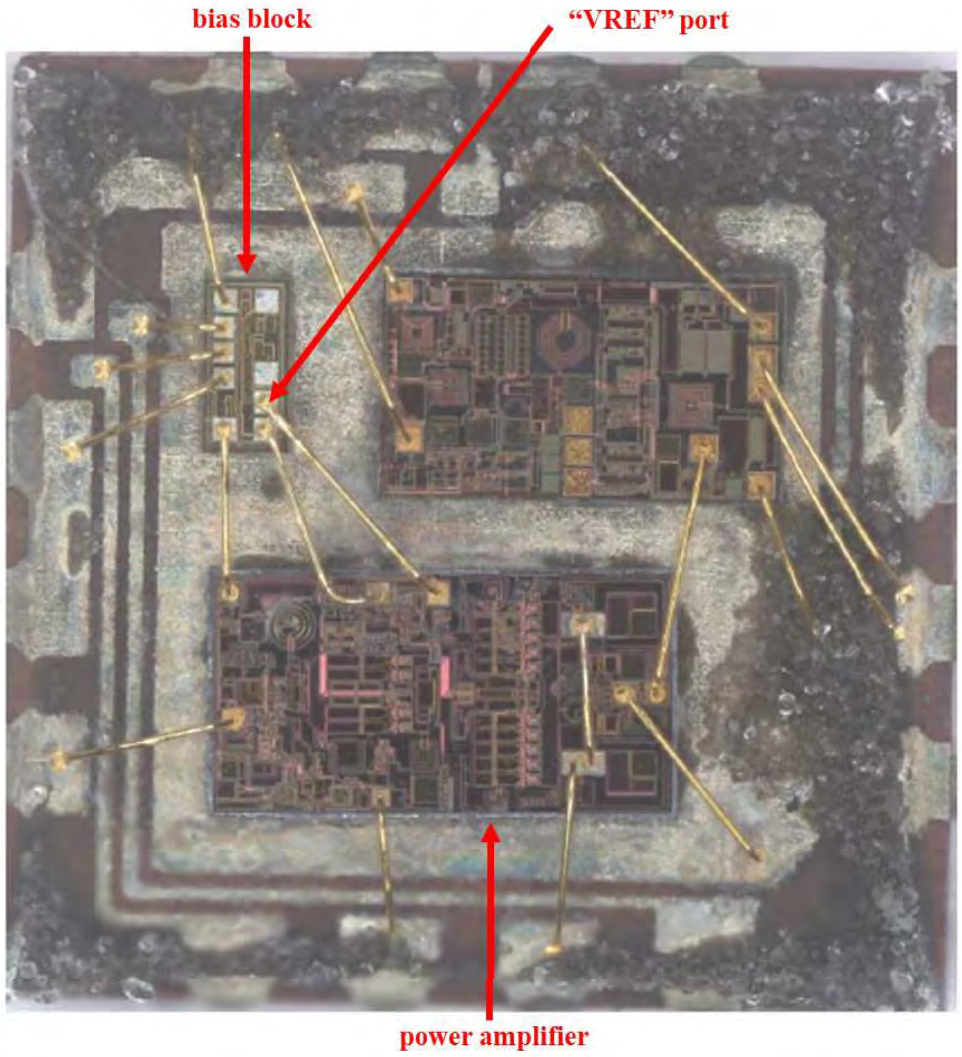
The schematic below for the KCT8547HE is an enlarged view of a portion of the current amplifier identified above, which is a current mirror configured to amplify the control current to generate the correction current. As set forth in the '101 patent, a current mirror can have any suitable gain. *See* '101 patent, 11:39-45. For example, the current mirror in KCT8547HE is configured to amplify the control current by a factor of about 1, based on the multiple numbers designated in the schematic below (e.g., "m=2" for the control current and "m=2" for the correction current).

	 *See, e.g.*, enlarged portion of reverse engineered schematic of the sub block of KCT8547HE
1[E] and a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current,	In the KCT8547HE, the bias block includes a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current. For example, as shown in the reverse engineered schematic for the KCT8547HE below, a primary biasing circuit (as indicated by the corresponding label below) is configured to generate a bias current (as indicated by the corresponding label below) for the power amplifier based at least partly on the correction current.

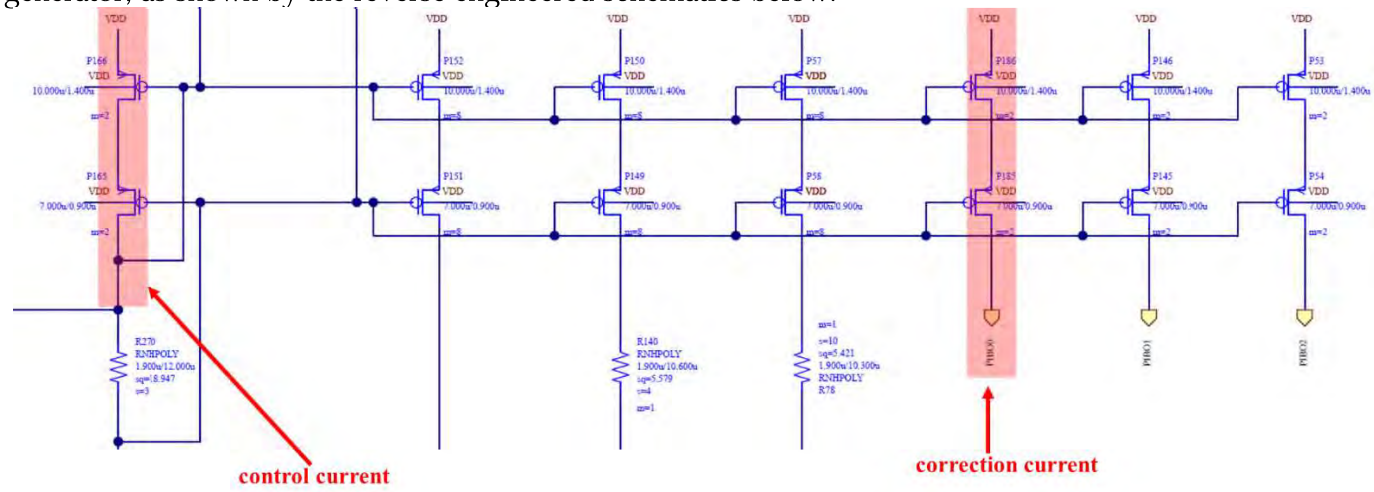


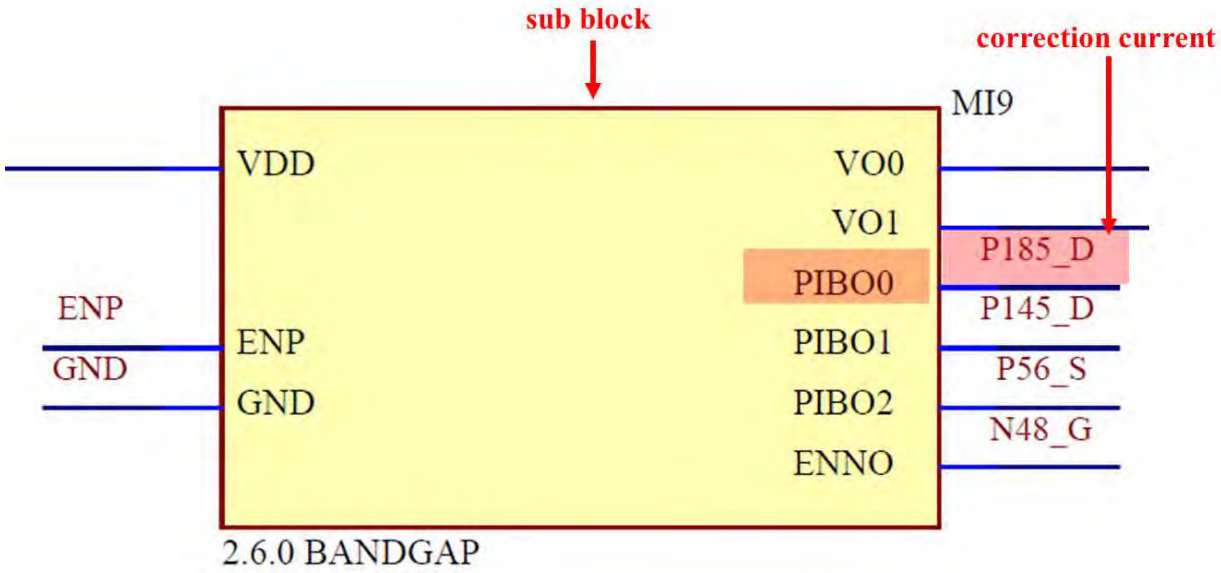
See, e.g., reverse engineered schematic of the bias block of KCT8547HE

The bias block biases the power amplifier using the bias current through a wire bond connecting a "VREF" port (as highlighted above and indicated by the corresponding label below) of the bias block to the power amplifier.



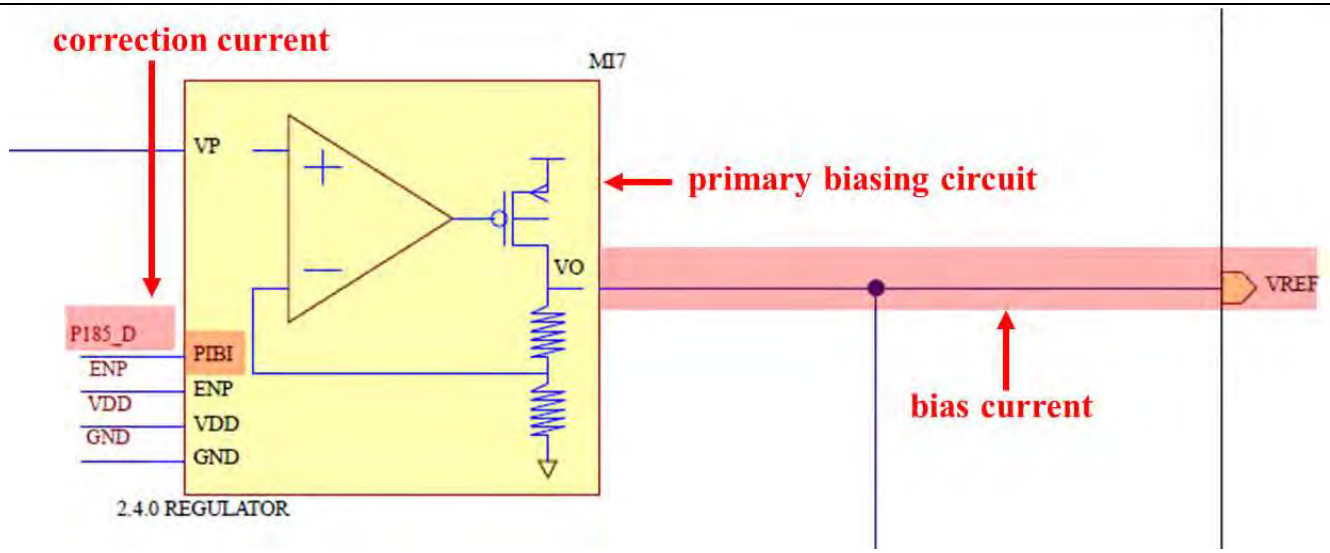
See, e.g., photo of KCT8547HE showing three dies, including a die for the bias block and a die for the power amplifier of the power amplifier system

	The correction current is output by the "PIBO0" port of the sub block including the time-dependent signal generator, as shown by the reverse engineered schematics below.  *See, e.g.*, enlarged portion of reverse engineered schematic of the sub block of KCT8547HE



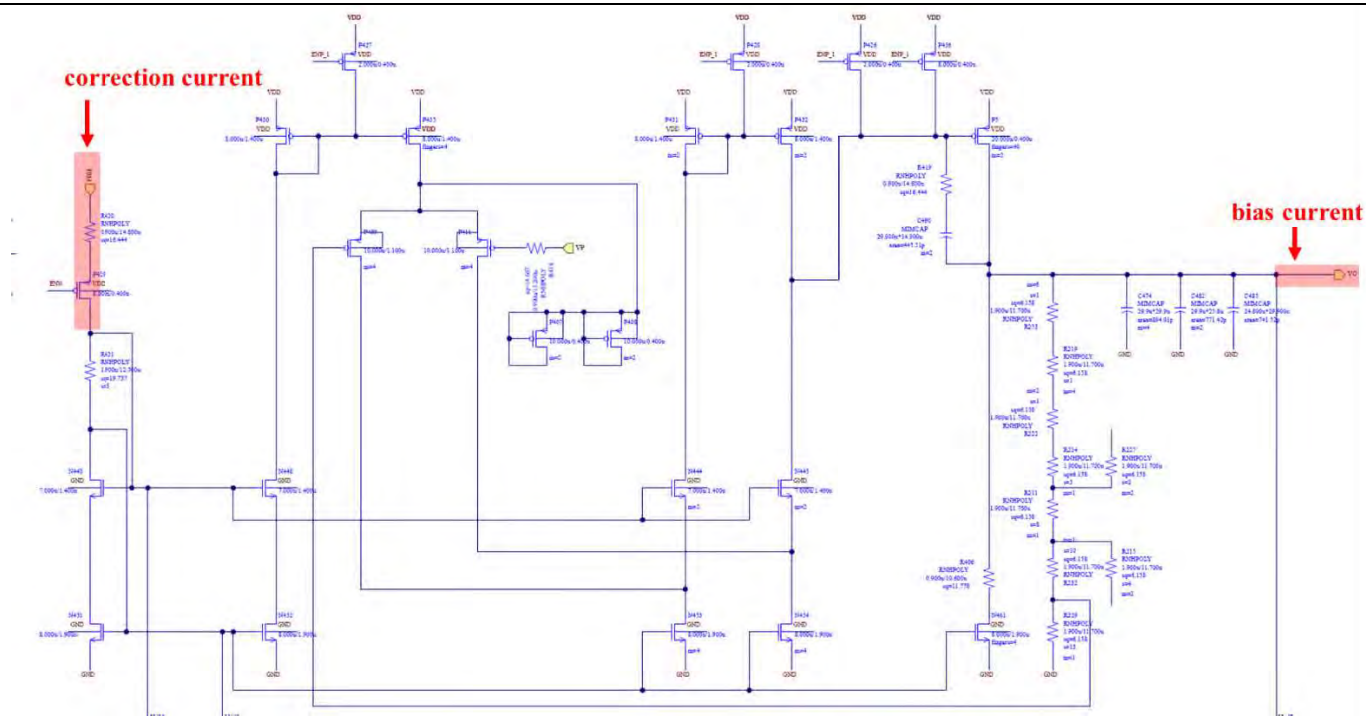
See, e.g., enlarged portion of reverse engineered schematic of the bias block of KCT8547HE

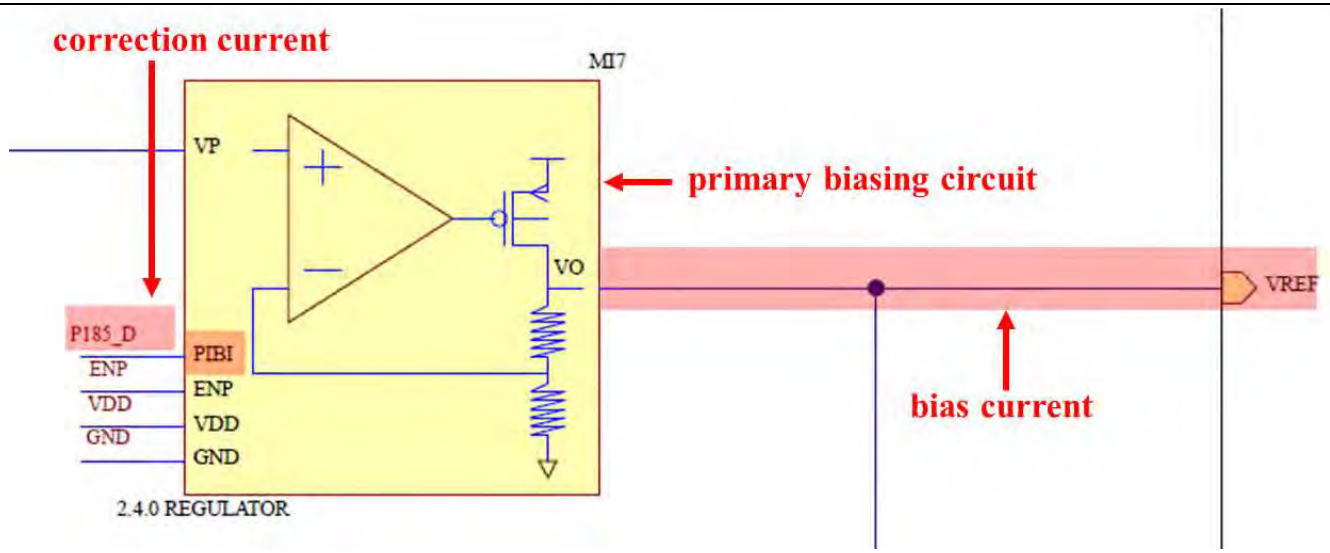
The "PIBO0" port of the sub block (shown above and as corresopnding to P185_D) including the time-dependent signal generator is connected to the "PIBI" port of the primary biasing circuit (as indicated by the corresponding label below showing P185_D connecting to PIBI), as shown by the schematic below.



See, e.g., enlarged portion of reverse engineered schematic of the bias block of KCT8547HE

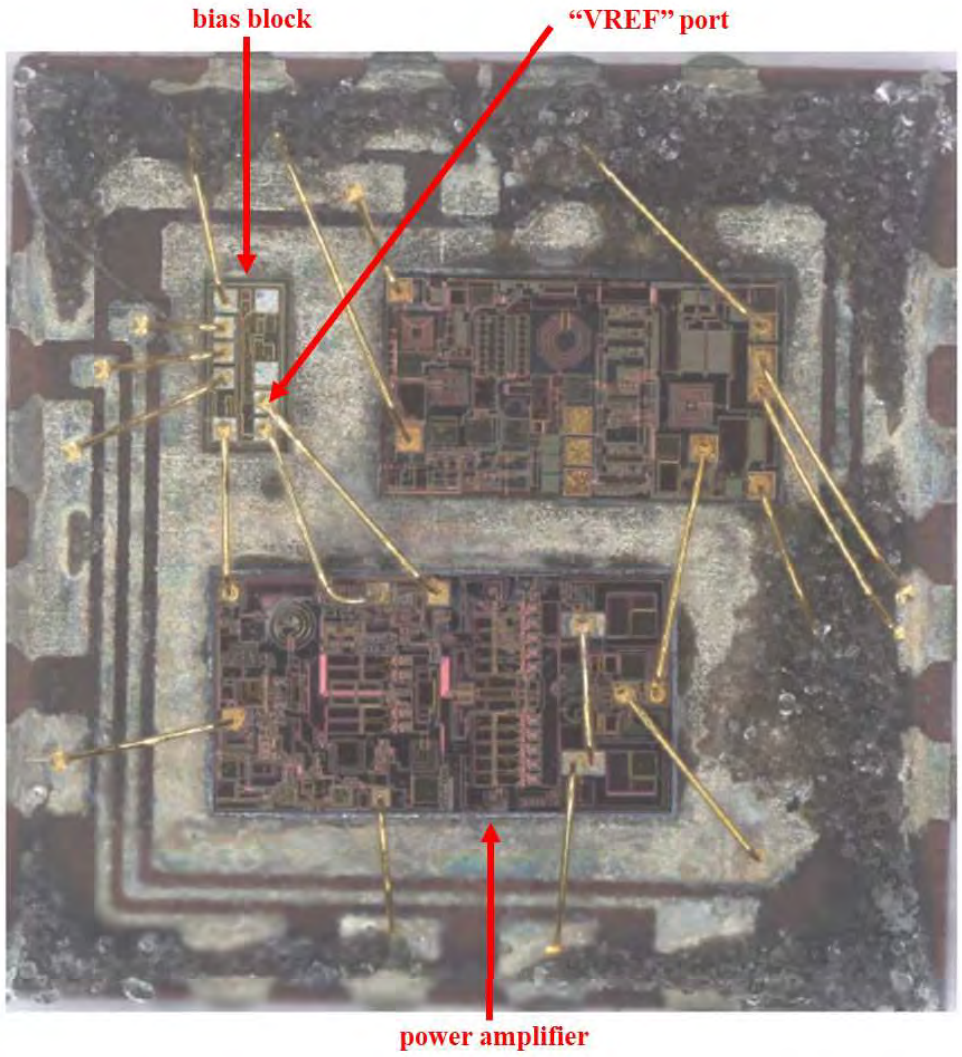
As shown by the schematic below for the primary biasing circuit of the KCT8547HE, the primary biasing circuit takes in the correction current as an input and generates the bias current for the power amplifier (as set forth above) based at least partly on the correction current.

	 *See, e.g.*, reverse engineered schematic of the primary biasing circuit of KCT8547HE
1[F] the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled,	In the KCT8547HE, the bias current is configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled. For example, the bias current is output by the "VREF" port of the bias block, as shown by the reverse engineered schematic for the KCT8547HE below.

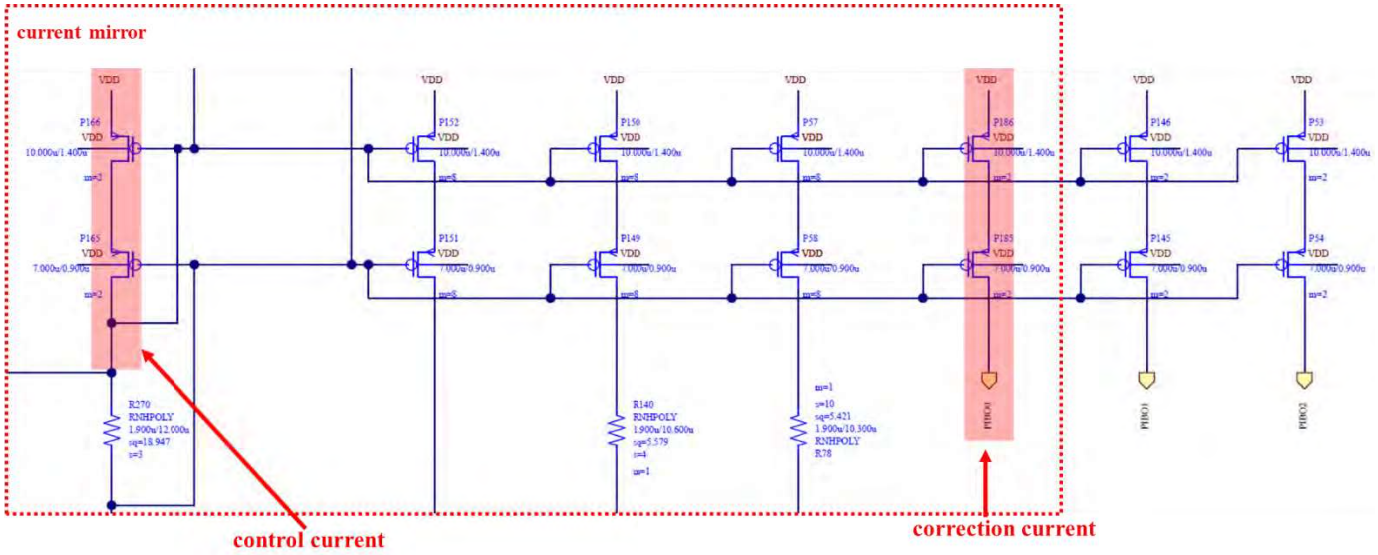


See, e.g., enlarged portion of reverse engineered schematic of the bias block of KCT8547HE

This bias current is input to the power amplifier for biasing the power amplifier to provide a suitable gain, including to correct for a variation in gain of the power amplifier when the power amplifier is enabled. As shown by the image below, the "VREF" port of the bias block is coupled to the die for the power amplifier via a wire bond.



See, e.g., photo of KCT8547HE showing three dies, including a die for the bias block and a die for the power amplifier of the power amplifier system

1[G] the current amplifier including a current mirror.	In the KCT8547HE, as shown by the reverse engineered schematic below, the current amplifier in the bias block includes a current mirror. The dashed box with the label below is one example of a current mirror that is included in the current amplifier.  *See, e.g.*, enlarged portion of reverse engineered schematic of the sub block of KCT8547HE For example, as explained in 1[D], the current amplifier in the bias block includes a current mirror configured to amplify the control current by a factor of about 1.
17[pre] A method of biasing a power amplifier, the method comprising:	To the extent the preamble of claim 17 is limiting, the KCT8547HE performs a method of biasing a power amplifier. For example, as explained in 1[pre] through 1[B], the KCT8547HE includes a bias block for biasing a power amplifier.
17[A] shaping an enable signal using a time-dependent signal	The KCT8547HE shapes an enable signal using a time-dependent signal generator to generate a control current.

generator to generate a control current;	For example, as explained in 1[C], the KCT8547HE includes a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current.
17[B] amplifying the control current using a current mirror of a current amplifier to generate a correction current; and	The KCT8547HE amplifies the control current using a current mirror of a current amplifier to generate a correction current. For example, as explained in 1[D], the KCT8547HE includes a current amplifier configured to amplify the control current to generate a correction current. As explained in 1[G], the current amplifier includes a current mirror that amplifies the control current to generate a correction current.
17[C] generating a bias current for a power amplifier using a primary biasing circuit, the primary biasing circuit configured to use the correction current to correct for a variation in gain of the power amplifier when the power amplifier is enabled.	The KCT8547HE generates a bias current for a power amplifier using a primary biasing circuit, the primary biasing circuit configured to use the correction current to correct for a variation in gain of the power amplifier when the power amplifier is enabled. For example, as explained in 1[E], the KCT8547HE includes a primary biasing circuit used to generate a bias current for the power amplifier based at least partly on the correction current. As explained in 1[F], the bias current is configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled. Since the bias current is at least partly based on the correction current, the primary biasing circuit is configured to use the correction current to correct for a variation in gain of the power amplifier when the power amplifier is enabled.
21[pre] A bias circuit for biasing a power amplifier, the bias circuit comprising:	To the extent the preamble of claim 21 is limiting, the KCT8547HE includes a bias circuit for biasing a power amplifier. For example, as explained in 1[pre] through 1[B], the KCT8547HE includes a bias block, which is a bias circuit, for biasing a power amplifier.
21[A] a time-dependent signal generator configured to shape an enable	The KCT8547HE includes the bias circuit comprising a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current.

signal of the power amplifier to generate a control current;	For example, as explained in 1[C], the KCT8547HE includes a bias circuit including a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current.
21[B] a current amplifier configured to amplify the control current to generate a correction current,	The KCT8547HE includes the bias circuit comprising a current amplifier configured to amplify the control current to generate a correction current. For example, as explained in 1[D], the bias circuit in the KCT8547HE includes a current amplifier configured to amplify the control current to generate a correction current.
21[C] the current amplifier including a current mirror; and	In the KCT8547HE, the current amplifier includes a current mirror. For example, as explained in 1[G], the current amplifier in the KCT8547HE includes a current mirror.
21[D] a primary biasing block configured to generate a bias current for the power amplifier based at least partly on the correction current,	The KCT8547HE includes the bias circuit comprising a primary biasing block configured to generate a bias current for the power amplifier based at least partly on the correction current. For example, as explained in 1[E], the bias circuit in the KCT8547HE includes a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current.
21[E] the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled.	In the KCT8547HE, the bias current is configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled. For example, as explained in 1[F], the bias current is input to the power amplifier for biasing the power amplifier to provide a suitable gain, including to correct for a variation in gain of the power amplifier when the power amplifier is enabled.

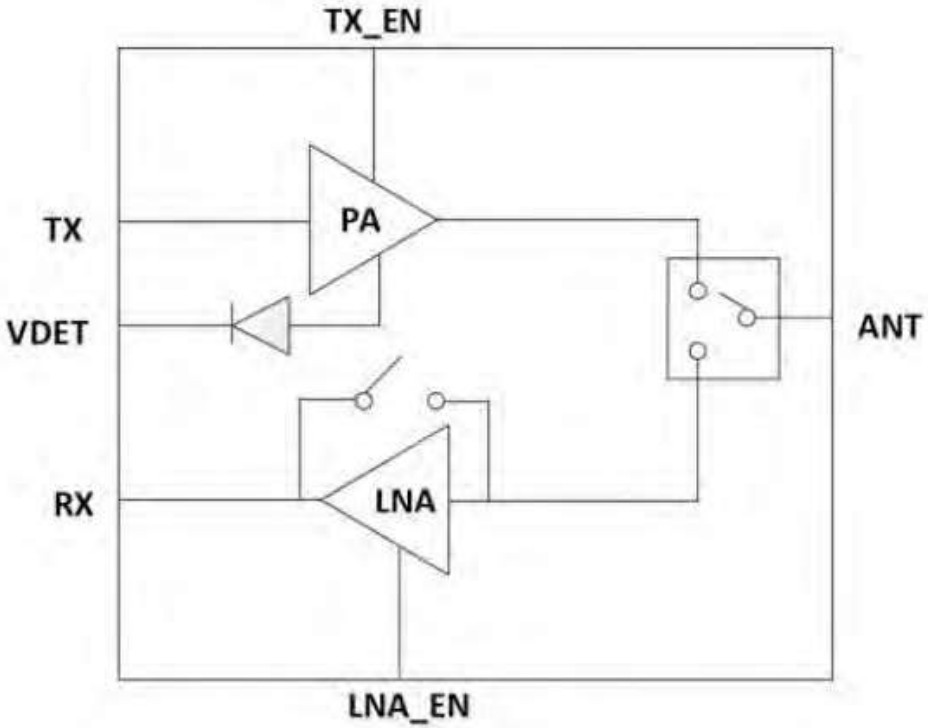
EXHIBIT 12

EXHIBIT 12
SKYWORKS SOLUTIONS, INC.'S INFRINGEMENT CHART
KCT8576HE
U.S. Patent No. 8,717,101
Independent Claims 1, 17, and 21

Skyworks Solutions, Inc. ("Skyworks") provides this exemplary claim chart for independent claims 1, 17, and 21 of U.S. Patent No. 8,717,101 (the "'101 patent") applied to Kangxi Communication Technologies (Shanghai) Co., Ltd's and Grand Chip Labs, Inc.'s (collectively, "KCT") KCT8576HE product. The disclosures in this claim chart directed to the KCT8576HE are also more broadly directed to any sale, offer for sale, use, or importation of the KCT8576HE in the U.S., including in an end product such as a wireless router or as a standalone product that is not incorporated in an end product.

The claim chart below demonstrates infringement by comparing each element of the charted claims to corresponding components, aspects, and/or features of the KCT8576HE product. This claim chart is not intended to constitute an expert report on infringement. This claim chart includes information provided by way of example, and not by way of limitation.

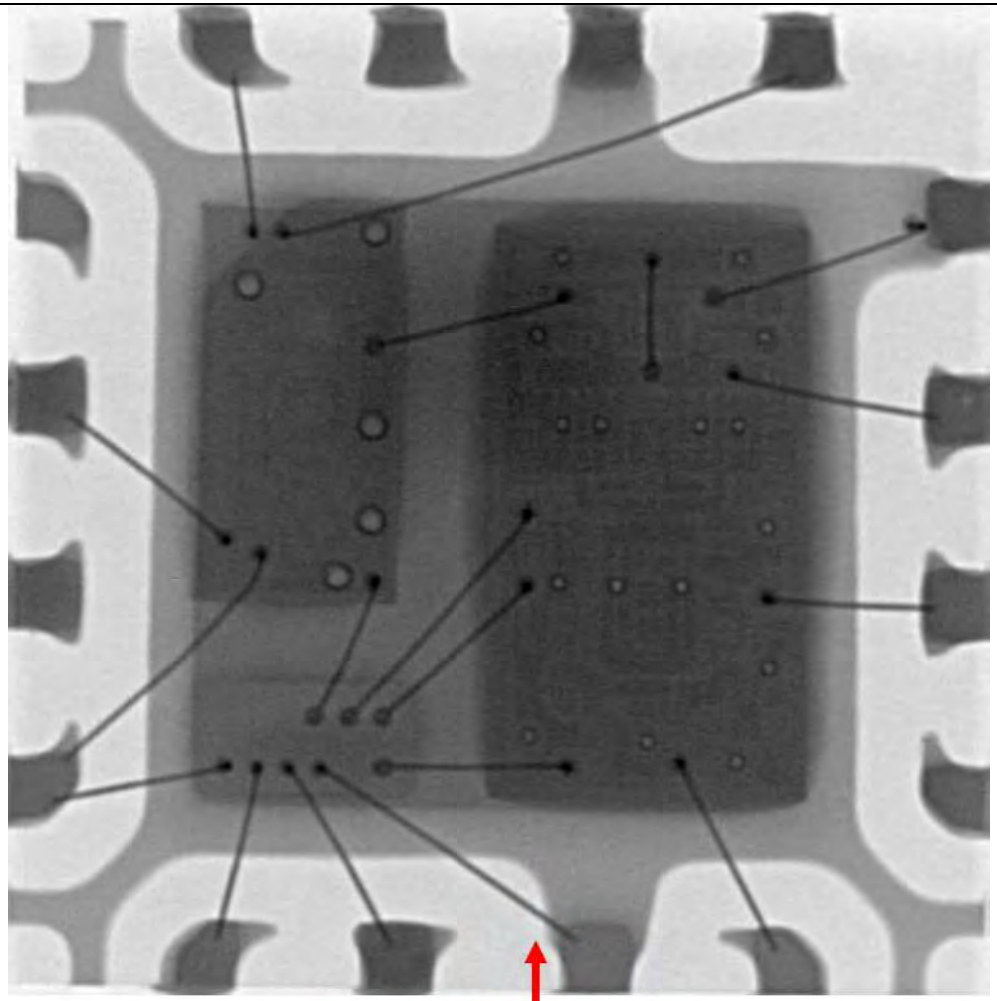
The analysis set forth below is based only upon information from publicly available sources regarding the KCT8576HE product. Further analysis of non-public information during fact discovery will likely assist in identifying all infringing features and functionalities used by KCT in the KCT8576HE product. Accordingly, Skyworks reserves the right to supplement this infringement analysis once such information is made available to Skyworks. Further, Skyworks reserves the right to supplement this infringement analysis, as appropriate, upon issuance of an order construing any terms recited in the asserted claims or as other circumstances so merit.

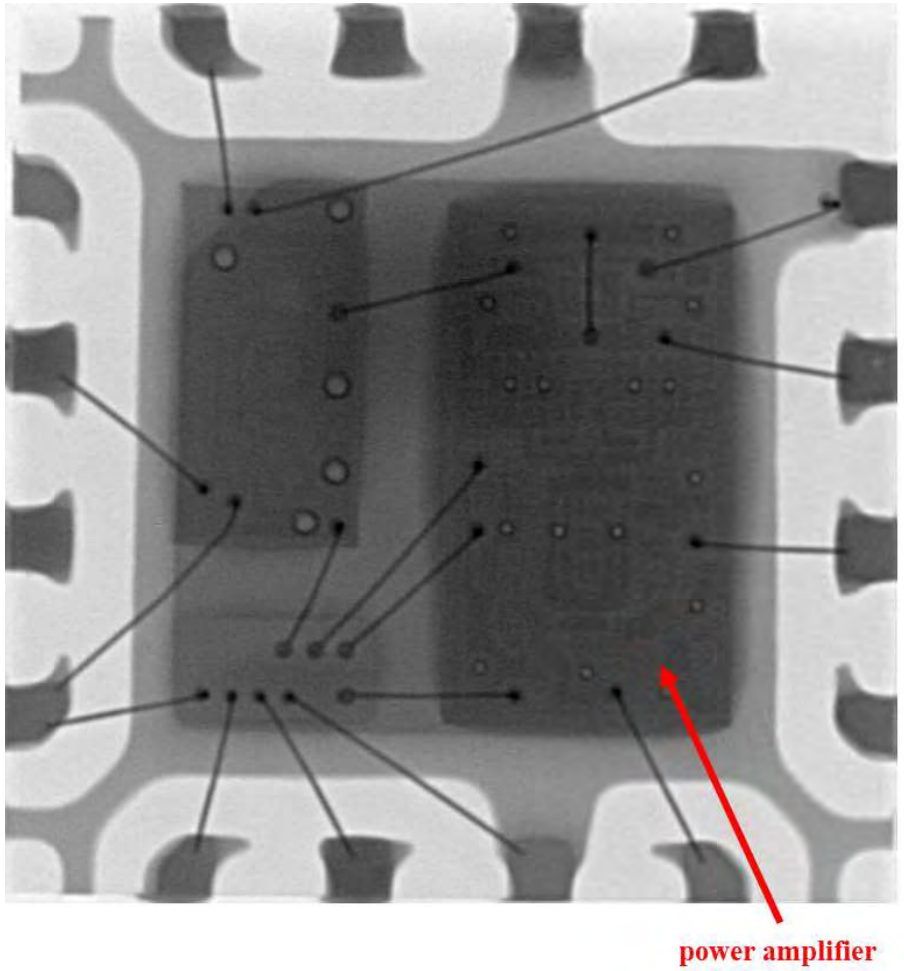
Claims	KCT8576HE
1[pre] A power amplifier system comprising:	To the extent the preamble of claim 1 is limiting, the KCT8576HE includes a power amplifier system. The KCT8576HE is a product for Wi-Fi connectivity. For example, the following image for the KCT8576HE is a simplified block diagram for this product.[1]  *See, e.g.*, simplified block diagram for KCT8576HE The KCT8576HE is, according to KCT, "a highly integrated RF front-end integrated circuit incorporat[ing] key RF functionality needed for IEEE 802.11a/n/ac/ax WLAN systems operating in the 5.15-5.95GHz

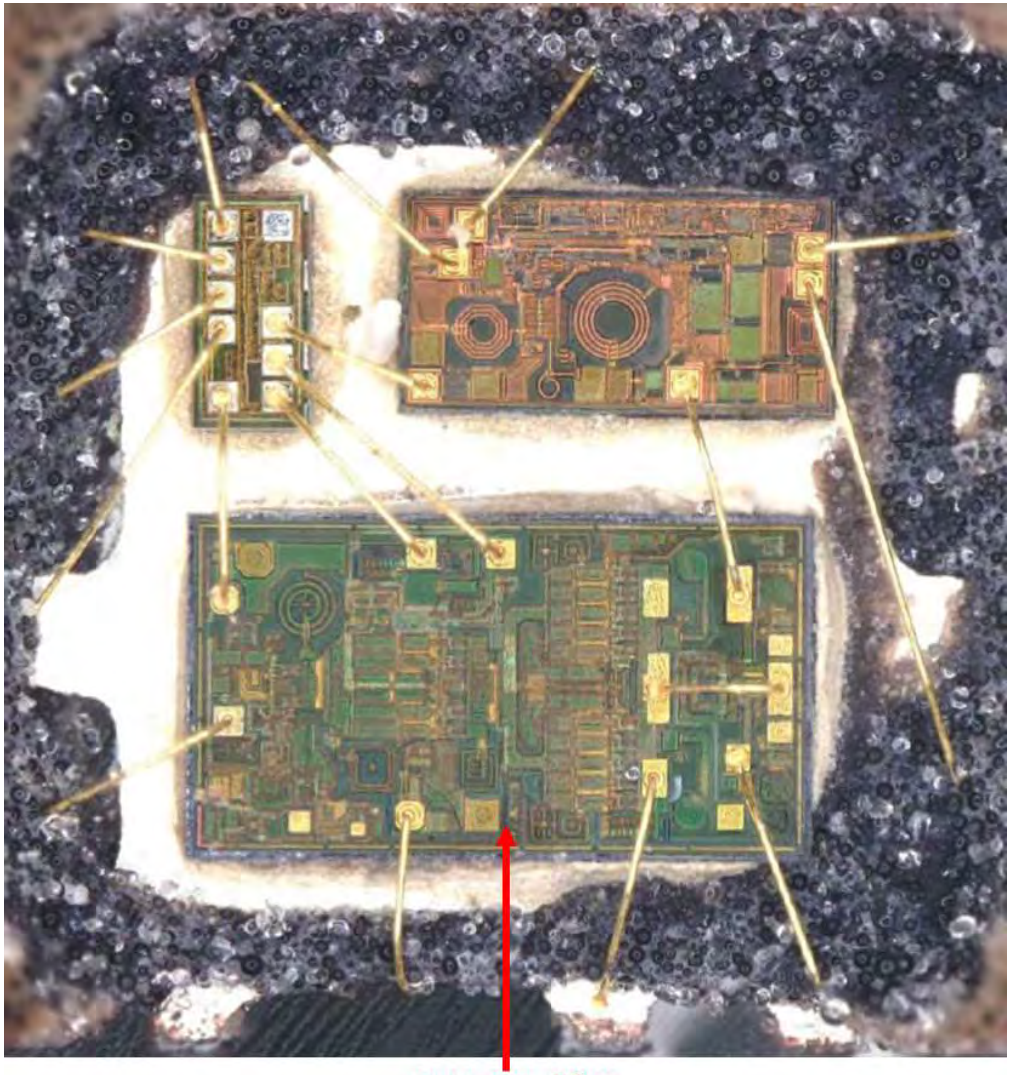
[1] *See* https://perma.cc/N2ZN-83UW.

	range. KCT8576HE integrates a high-efficiency, high-linearity power amplifier (PA), a low noise amplifier (LNA) with bypass ….”[2] For example, the image below of the KCT8576HE shows a power amplifier system (as indicated by the corresponding label below) within the KCT8576HE.

[2] *See* https://perma.cc/N2ZN-83UW.

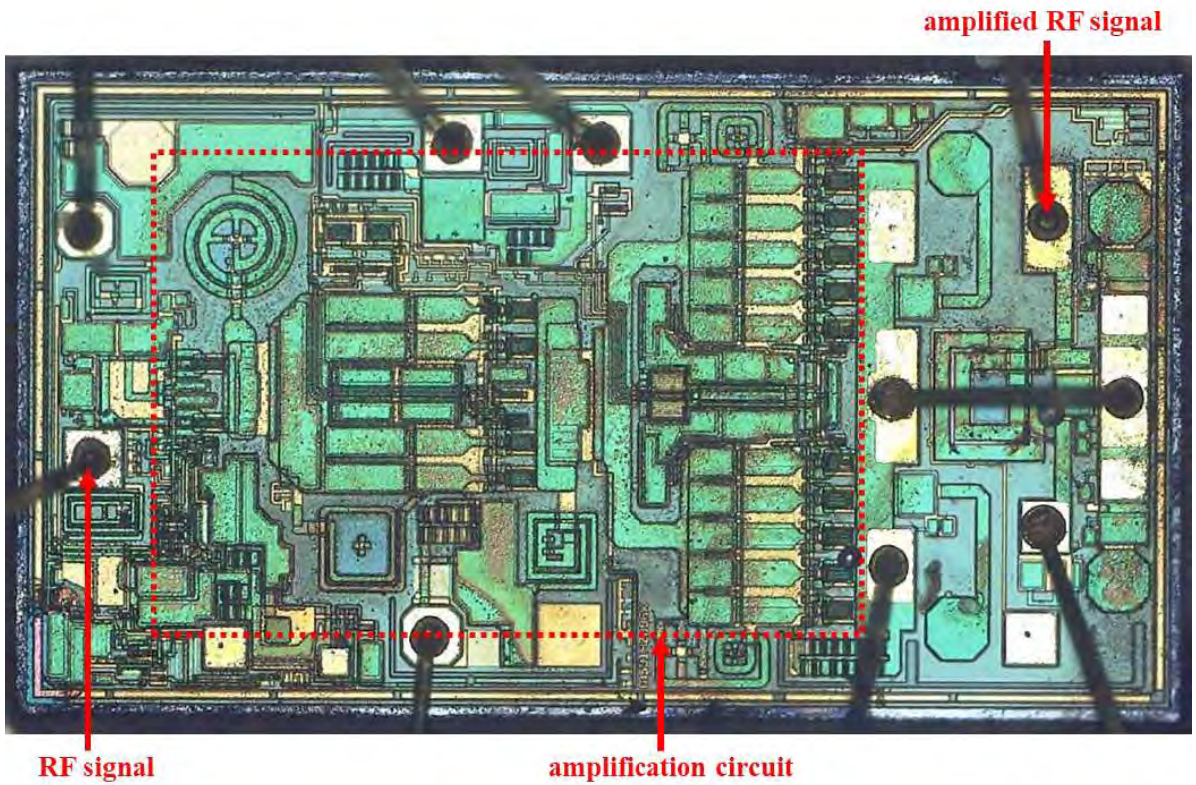
	 *See, e.g.*, photo of KCT8576HE showing three dies of the power amplifier system
1[A] a power amplifier configured	The KCT8576HE includes a power amplifier configured to amplify a radio frequency (RF) signal.

to amplify a radio frequency (RF) signal; and	For example, the image of the KCT8576HE below shows a power amplifier (as indicated by the corresponding label below) as part of the power amplifier system.  *See, e.g.*, photo of KCT8576HE showing three dies, including a die for the power amplifier of the power amplifier system

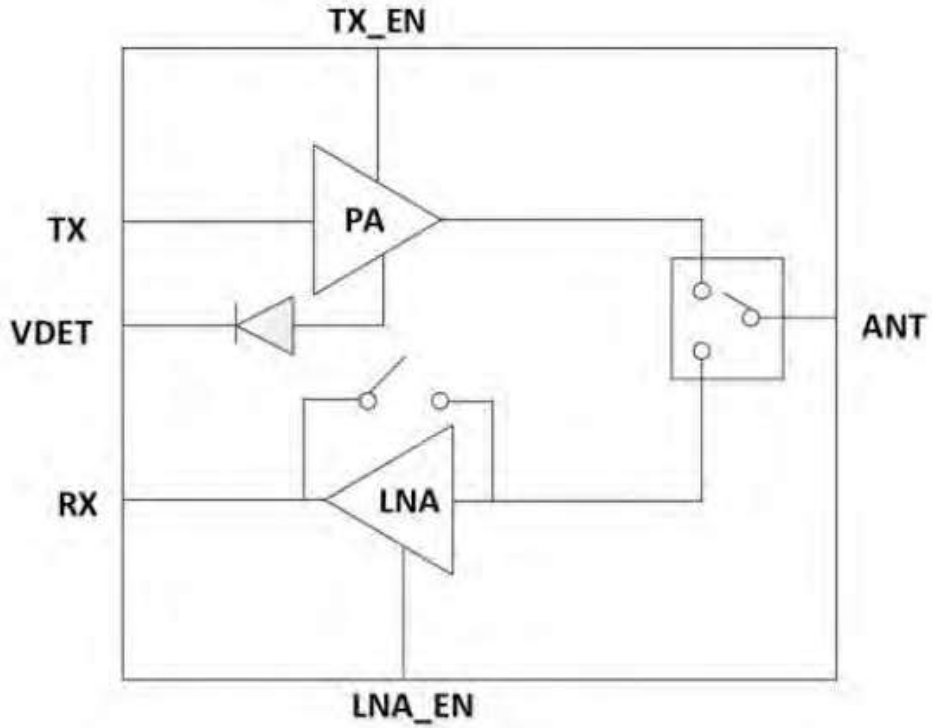
	The image below shows the die of the power amplifier as part of the power amplifier system for the KCT8576HE. 

See, e.g., photo of KCT8576HE showing three dies, including the die for the power amplifier of the power amplifier system

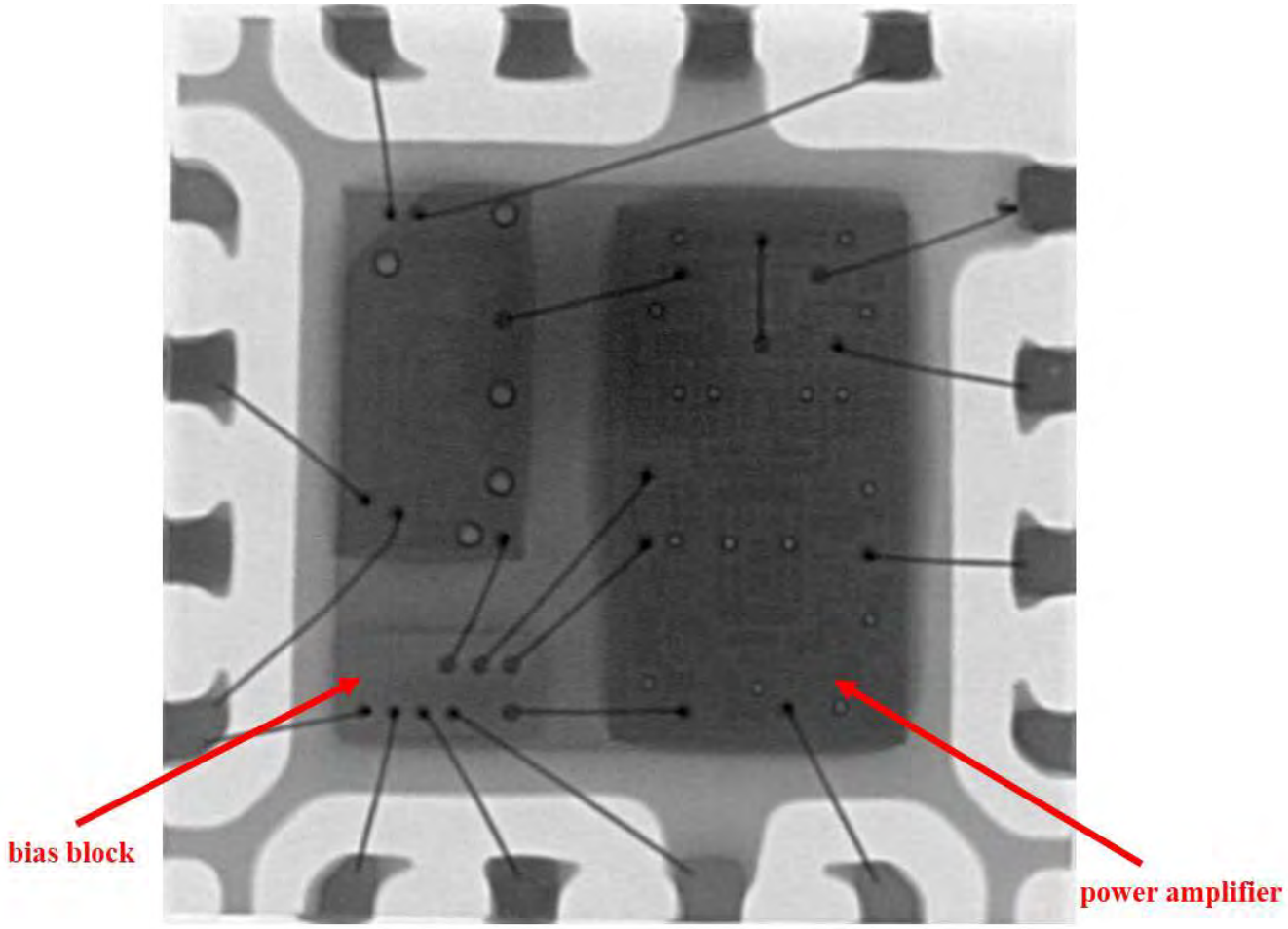
The image below shows an enlarged view of the power amplifier die of the KCT8576HE. The power amplifier in the KCT8576HE is coupled so that it is configured to receive as an input a radio frequency (RF) signal, as labeled below, and amplify the RF signal to output an amplified RF signal, as labeled below. The dashed box with the corresponding label below is one example of an amplification circuit that provides the amplification of the RF signal.



See, e.g., photo of the power amplifier die in KCT8576HE

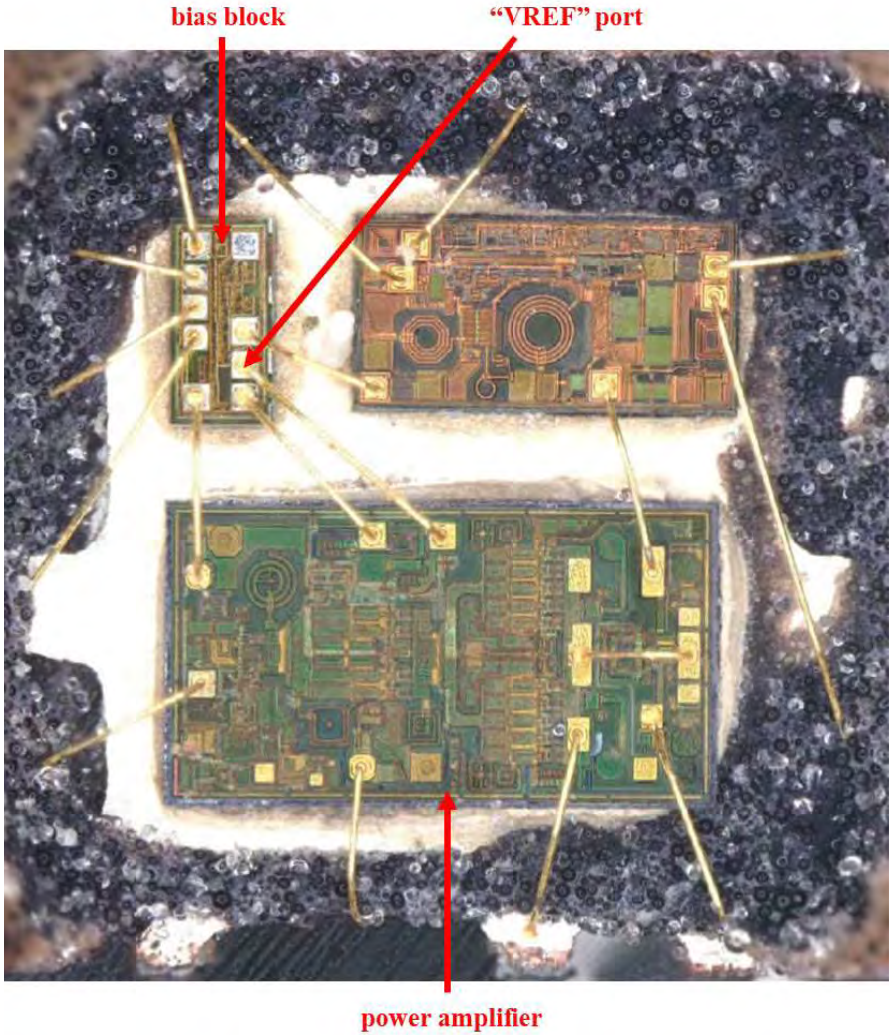
	As shown below in KCT's simplified block diagram for the KCT8576HE, a power amplifier (labelled as "PA") is part of the KCT8576HE product. Specifically, the KCT8576HE "integrates a high-efficiency, high-linearity power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated matching network, LO rejection, and harmonic filters all in one device."[3]  *See, e.g.*, simplified block diagram for KCT8576HE
1[B] a bias block for biasing the power amplifier,	The KCT8576HE includes a bias block for biasing the power amplifier. For example, the image of the KCT8576HE below shows a bias block (as indicated by the corresponding label below) as part of the power amplifier system.

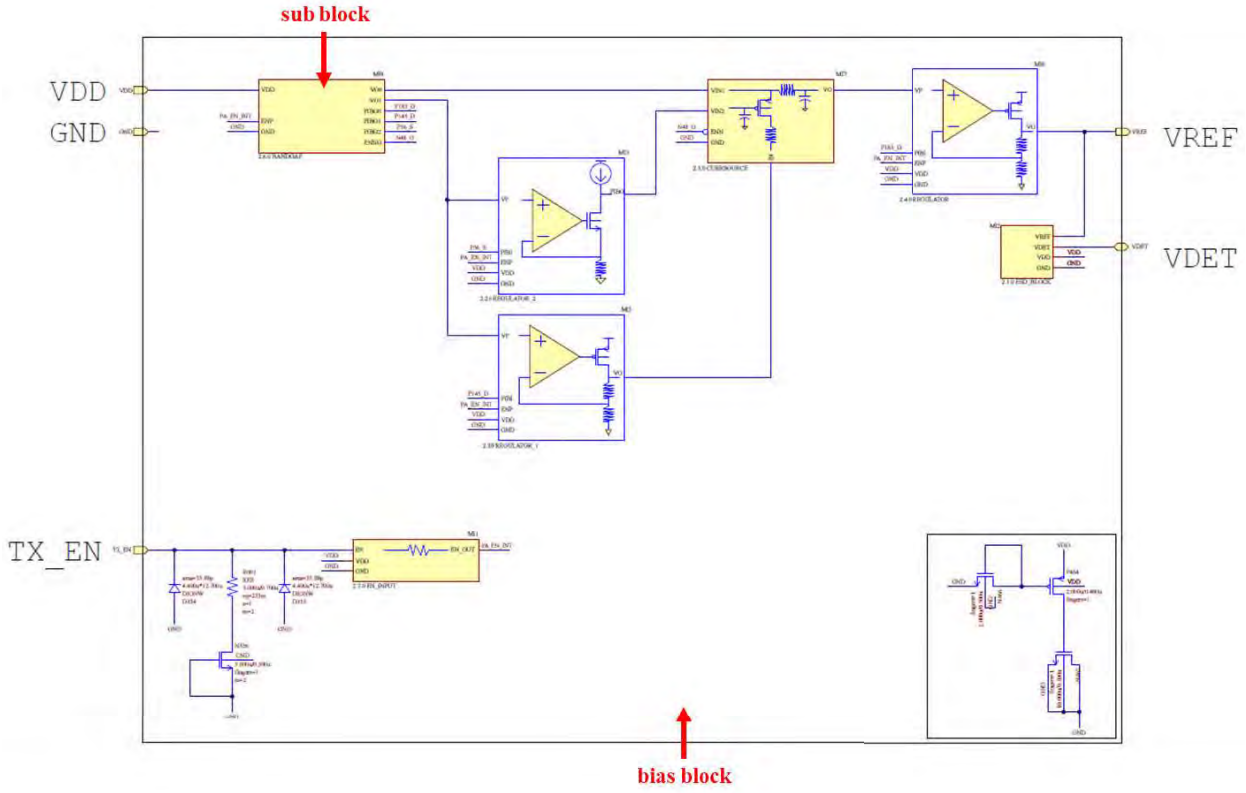
[3] *See* https://perma.cc/N2ZN-83UW.

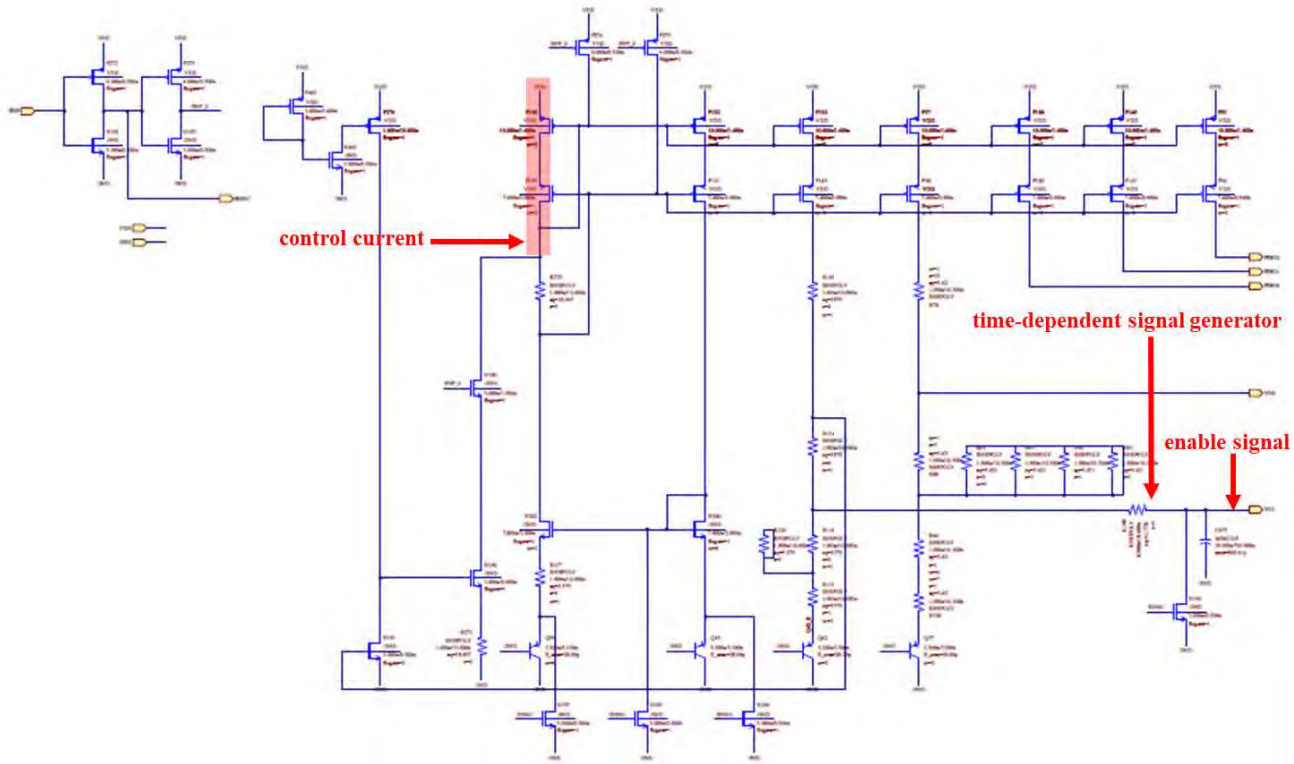


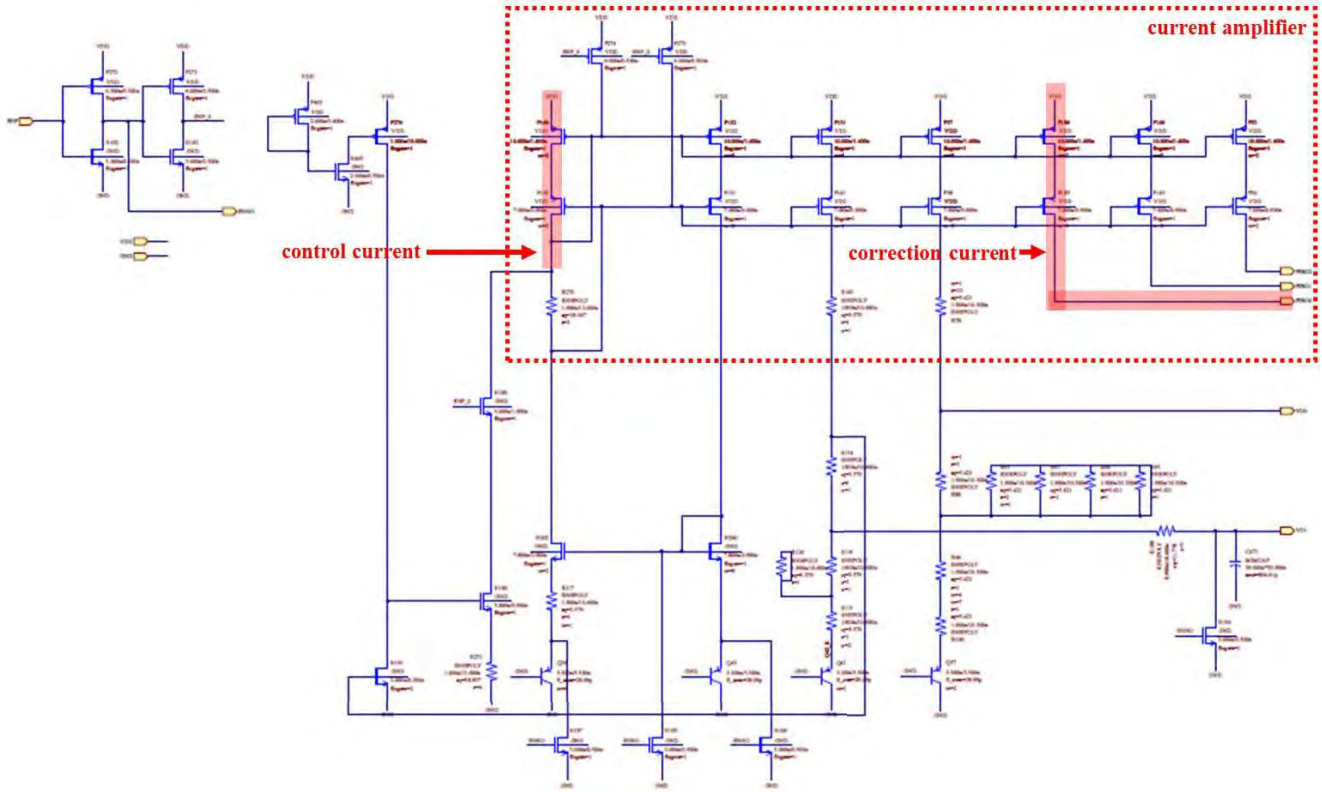
See, e.g., photo of KCT8576HE showing three dies, including a die for the bias block and a die for the power amplifier of the power amplifier system

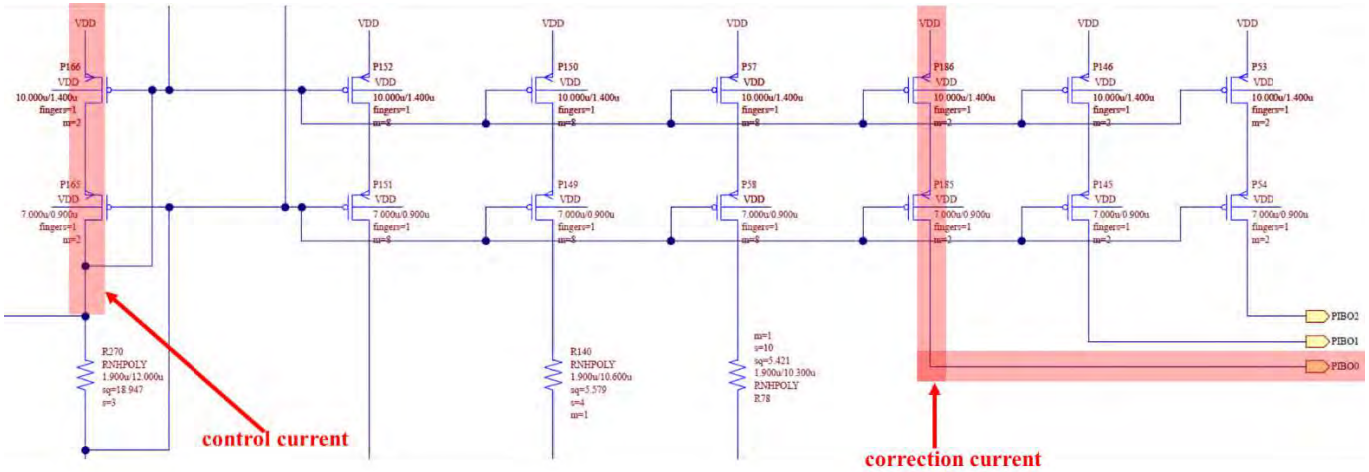
The image below shows the power amplifier and the bias block within the power amplifier system in another angle for the KCT8576HE. The bias block is coupled to the power amplifier so that the bias block

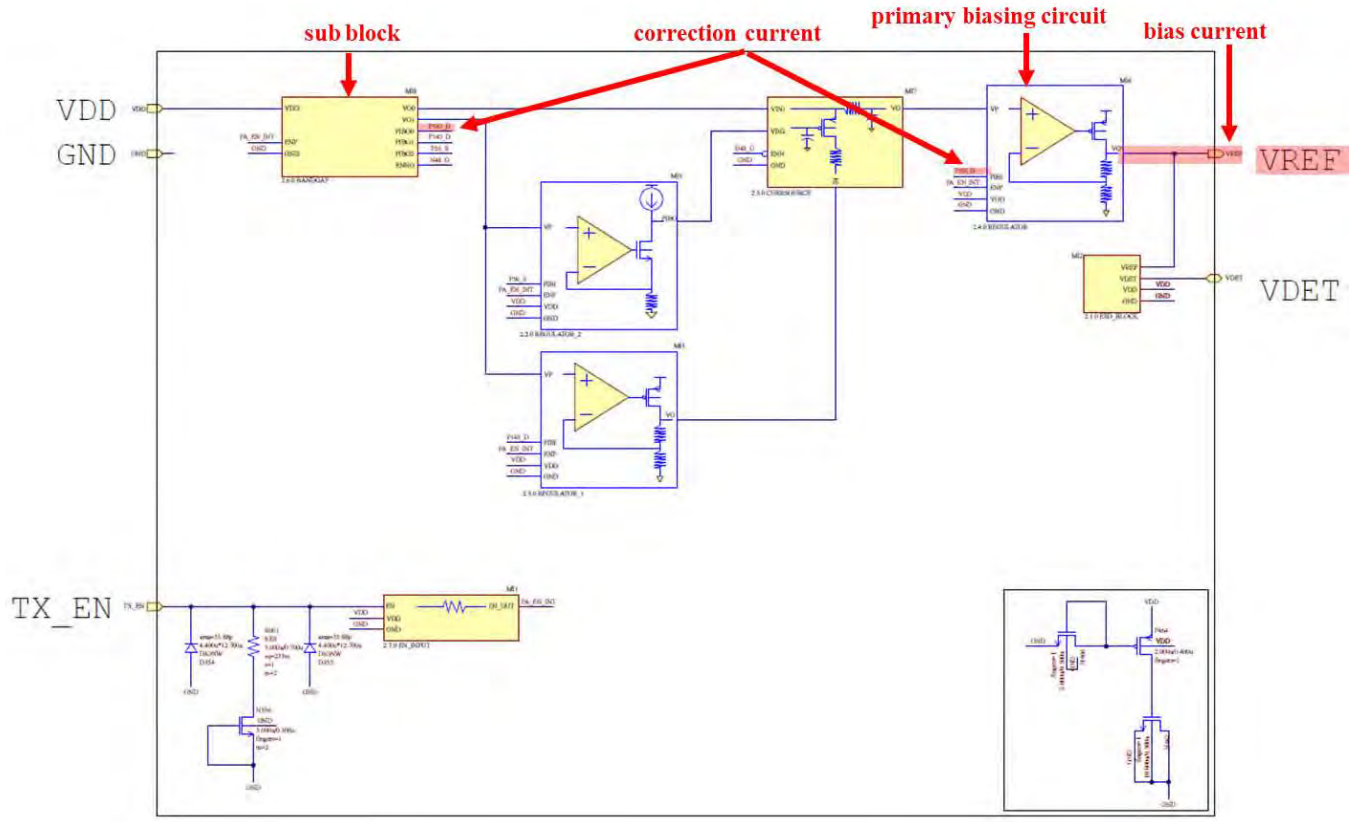
	biases the power amplifier using a bias current through a wire bond connecting a "VREF" port (as indicated by the corresponding label below) of the bias block to the power amplifier.  *See, e.g.*, photo of KCT8576HE showing three dies, including a die for the bias block and a die for the power amplifier of the power amplifier system

	See also elements 1[C]-1[E] (showing details of the bias circuit).
1[C] the bias block including a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current,	The KCT8576HE includes the bias block including a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current. For example, the reverse engineered schematic below is for the bias block (as indicated by the corresponding label below) in the KCT8576HE. It includes a sub block (as indicated by the corresponding label below). The sub block includes a time-dependent signal generator.  *See, e.g.*, reverse engineered schematic of the bias block of KCT8576HE

	The reverse engineered schematic below for the KCT8576HE shows the internal details of the sub block set forth above. This schematic includes a time-dependent signal generator (as indicated by the corresponding label below). This time-dependent signal generator is configured to shape an enable signal (as indicated by the corresponding label below) of the power amplifier to generate a control current (as indicated by the corresponding label below). The time-dependent signal generator shapes the enable signal to generate the control current in that the enable signal is a time-dependent voltage and the control current depends on the enable signal.  *See, e.g.*, reverse engineered schematic of the sub block of KCT8576HE
1[D] a current amplifier configured	In the KCT8576HE, the bias block includes a current amplifier configured to amplify the control current to generate a correction current.

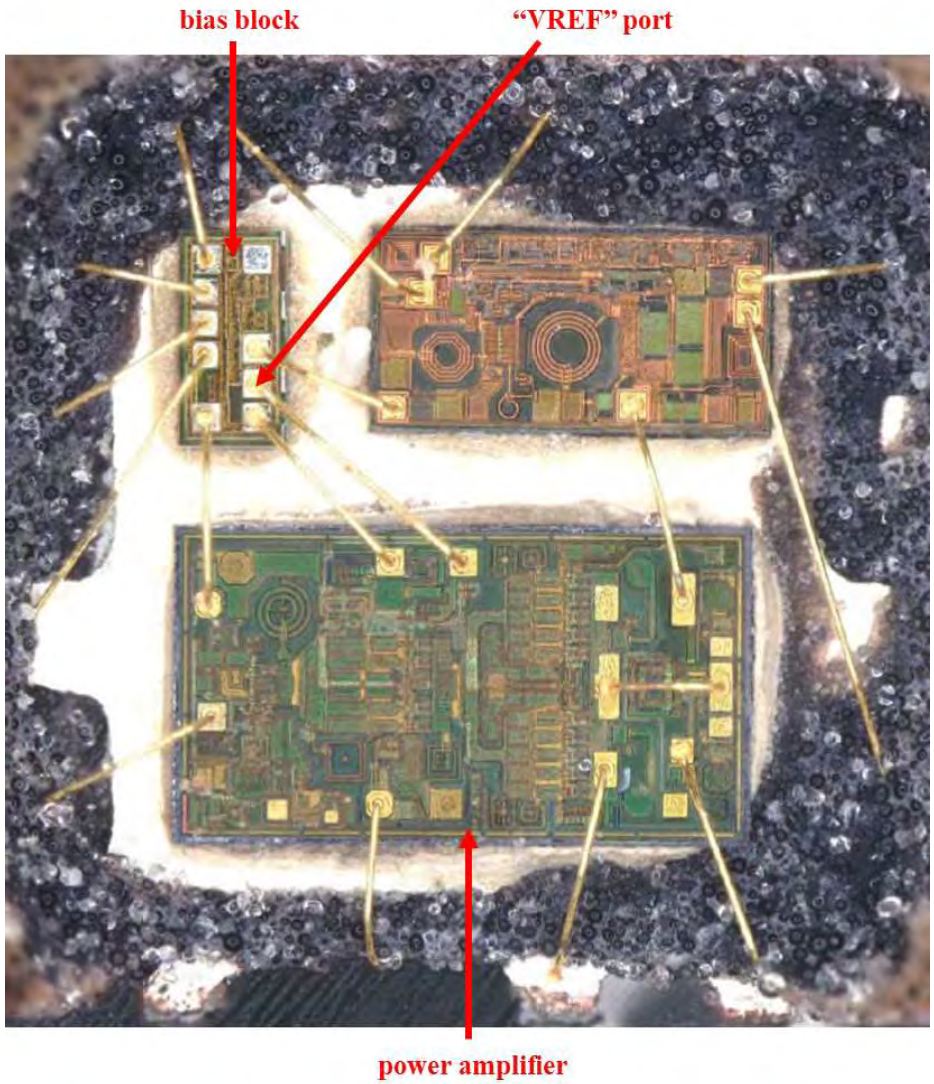
to amplify the control current to generate a correction current,	For example, as shown by the reverse engineered schematic below for the sub block of the KCT8576HE, the bias block includes a current amplifier (as indicated by the corresponding label below). The current amplifier is configured to amplify the control current to generate a correction current (as indicated by the corresponding label below). The dashed box with the label below is one example of a current amplifier that amplifies the control current to generate the correction current.  *See, e.g.*, reverse engineered schematic of the sub block of KCT8576HE The schematic below for the KCT8576HE is an enlarged view of a portion of the current amplifier identified above, which is a current mirror configured to amplify the control current to generate the correction current. As set forth in the '101 patent, a current mirror can have any suitable gain. *See* '101

	patent, 11:39-45. For example, the current mirror in KCT8576HE is configured to amplify the control current by a factor of about 1, based on the multiple numbers designated in the schematic below (e.g., "m=2" for the control current and "m=2" for the correction current).  *See, e.g.*, enlarged portion of reverse engineered schematic of the sub block of KCT8576HE
1[E] and a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current,	In the KCT8576HE, the bias block includes a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current. For example, as shown in the reverse engineered schematic for the KCT8576HE below, a primary biasing circuit (as indicated by the corresponding label below) is configured to generate a bias current (as indicated by the corresponding label below) for the power amplifier based at least partly on the correction current.

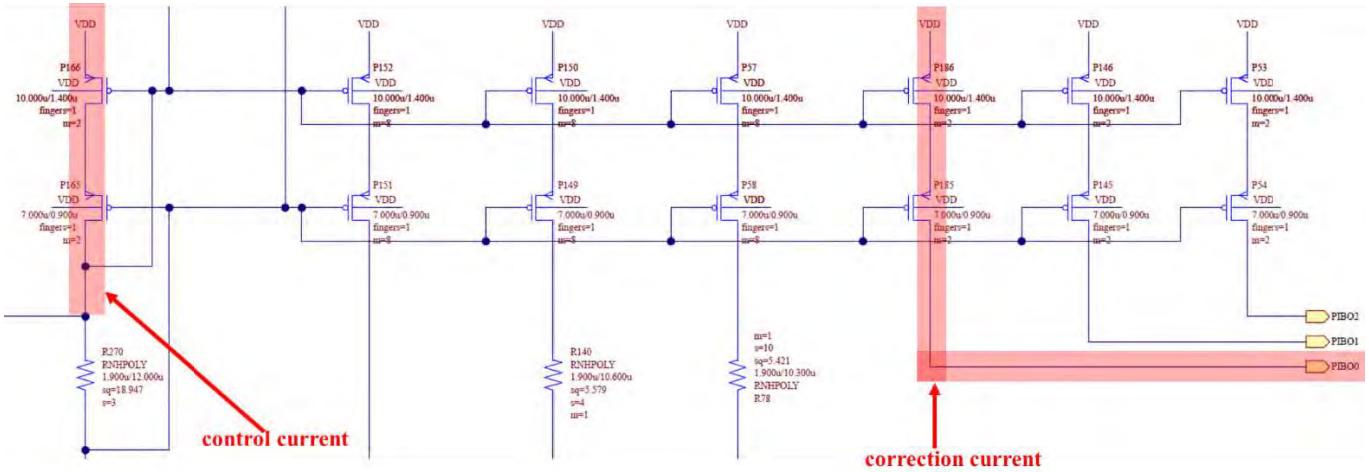


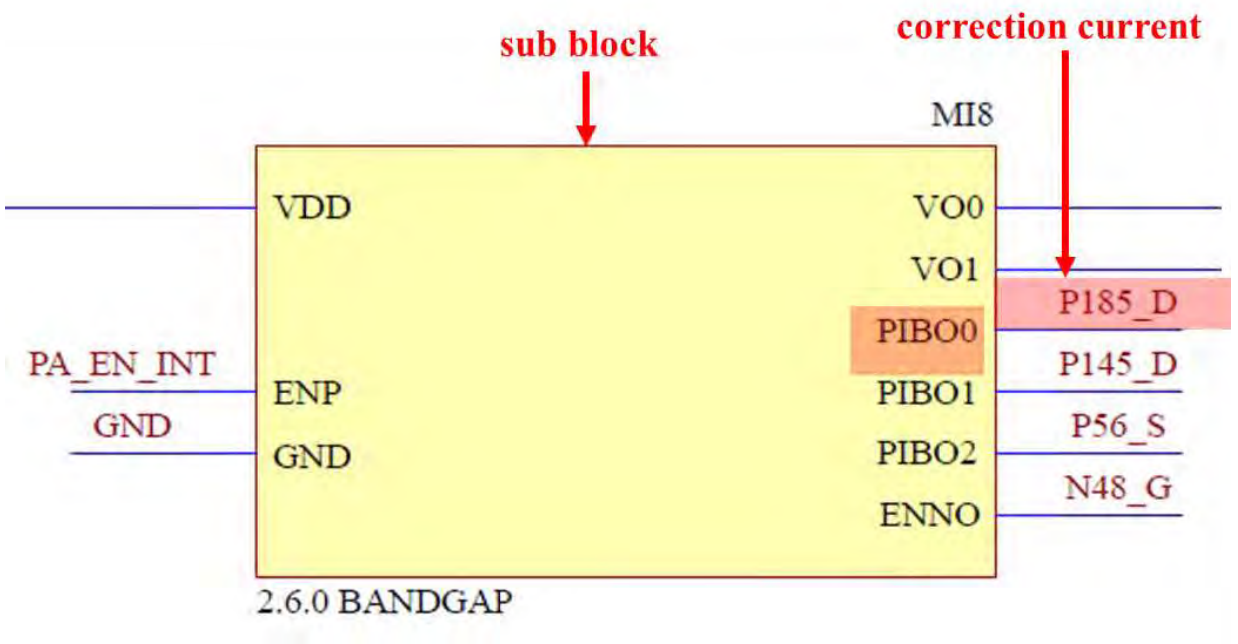
See, e.g., reverse engineered schematic of the bias block of KCT8576HE

The bias block biases the power amplifier using the bias current through a wire bond connecting a "VREF" port (as highlighted above and indicated by the corresponding label below) of the bias block to the power amplifier.



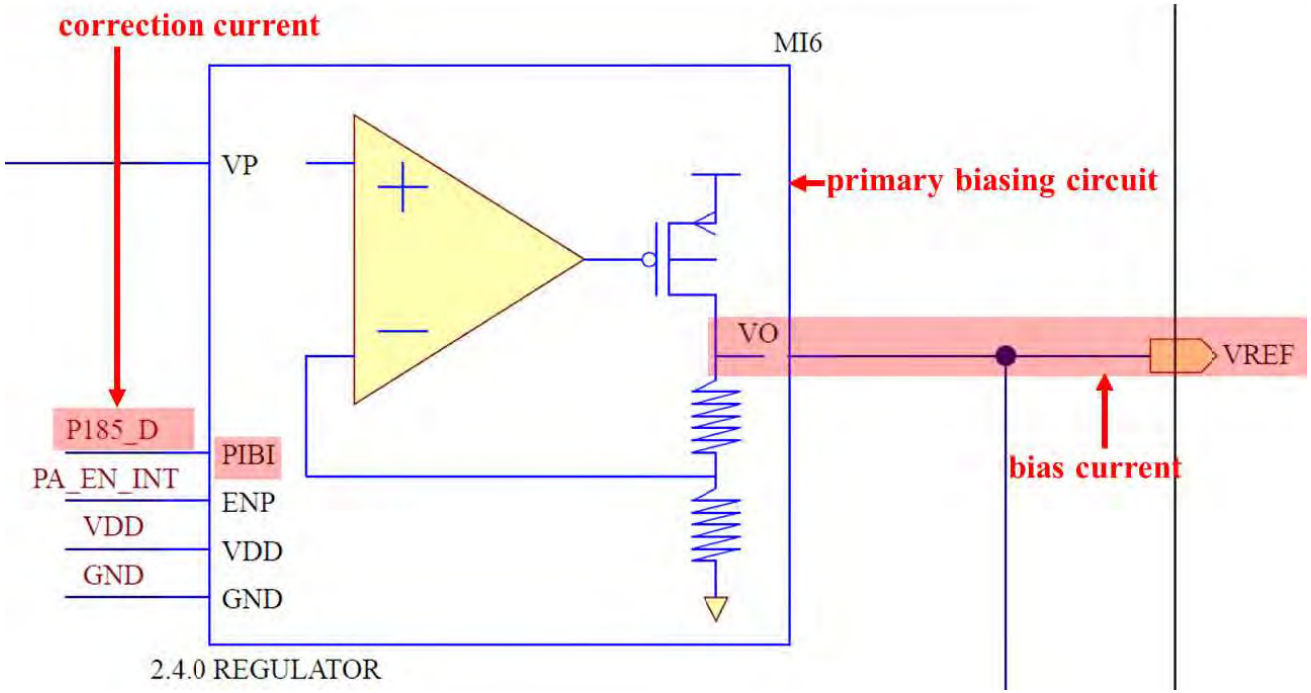
See, e.g., photo of KCT8576HE showing three dies, including a die for the bias block and a die for the power amplifier of the power amplifier system

	The correction current is output by the "PIBO0" port of the sub block including the time-dependent signal generator, as shown by the reverse engineered schematics below.  *See, e.g.*, enlarged portion of reverse engineered schematic of the sub block of KCT8576HE



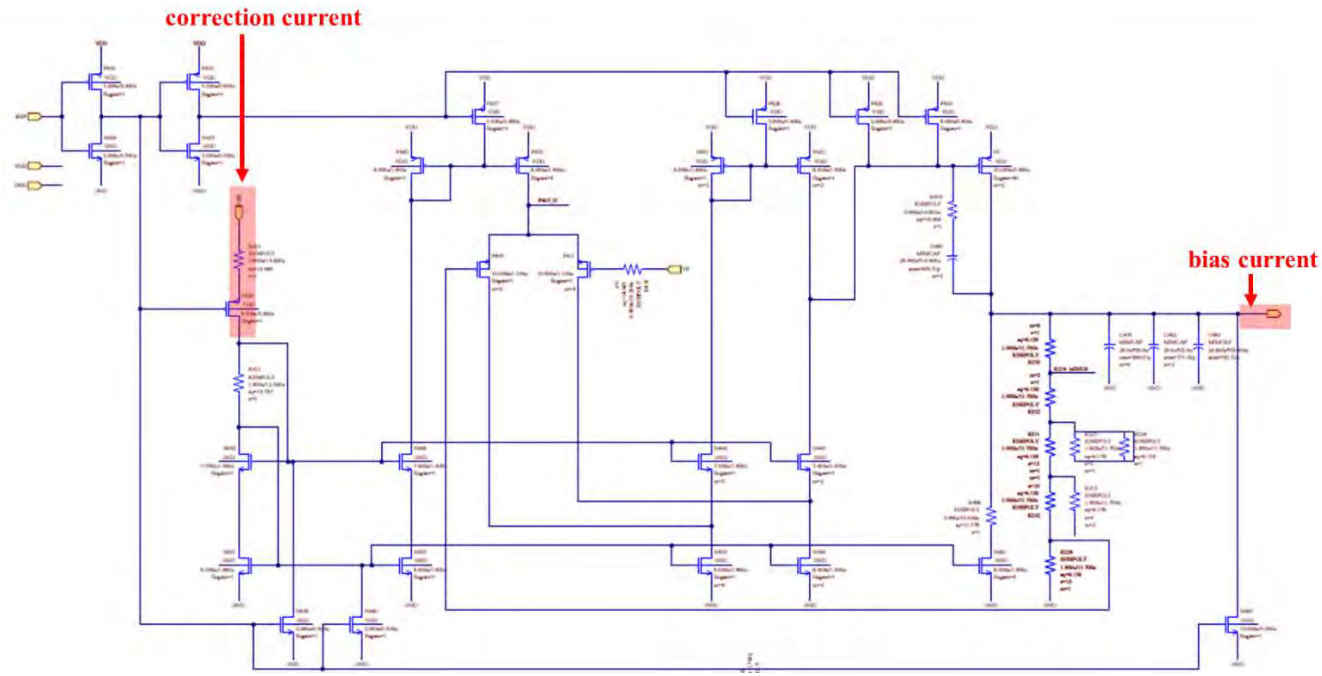
See, e.g., enlarged portion of reverse engineered schematic of the bias block of KCT8576HE

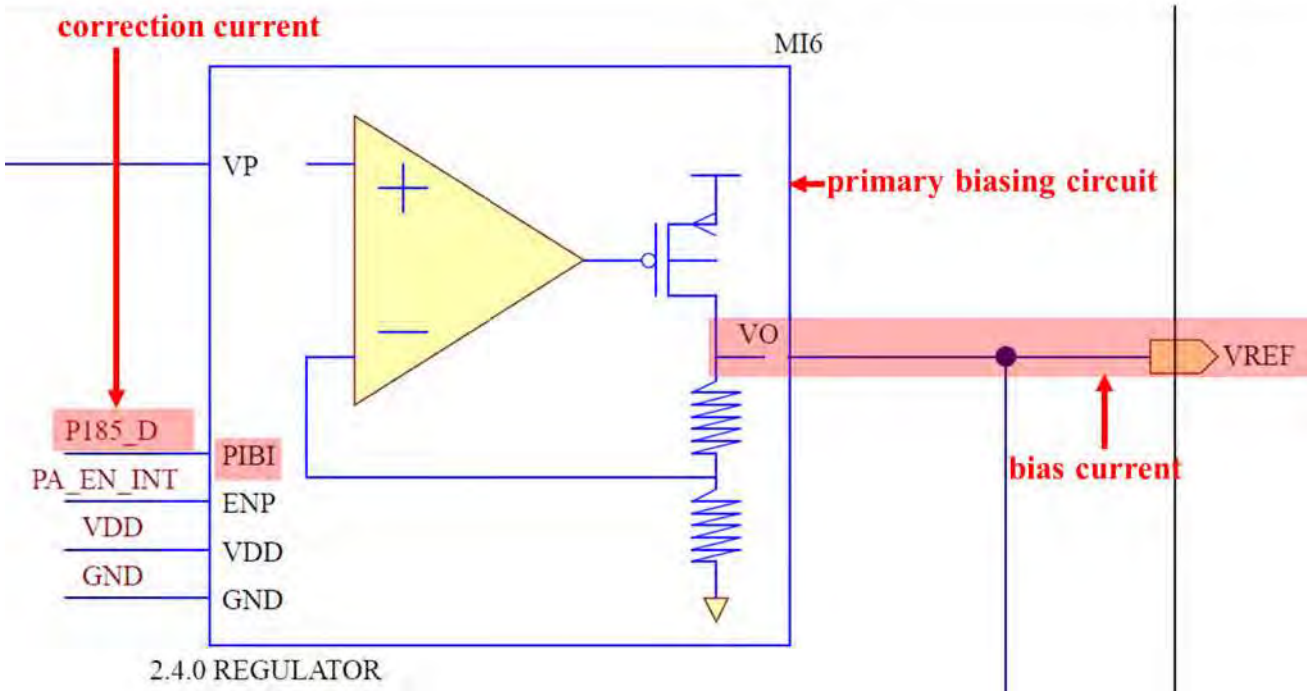
The "PIBO0" port of the sub block (shown above and as corresopnding to P185_D) including the time-dependent signal generator is connected to the "PIBI" port of the primary biasing circuit (as indicated by the corresponding label below showing P185_D connecting to PIBI), as shown by the schematic below.



See, e.g., enlarged portion of reverse engineered schematic of the bias block of KCT8576HE

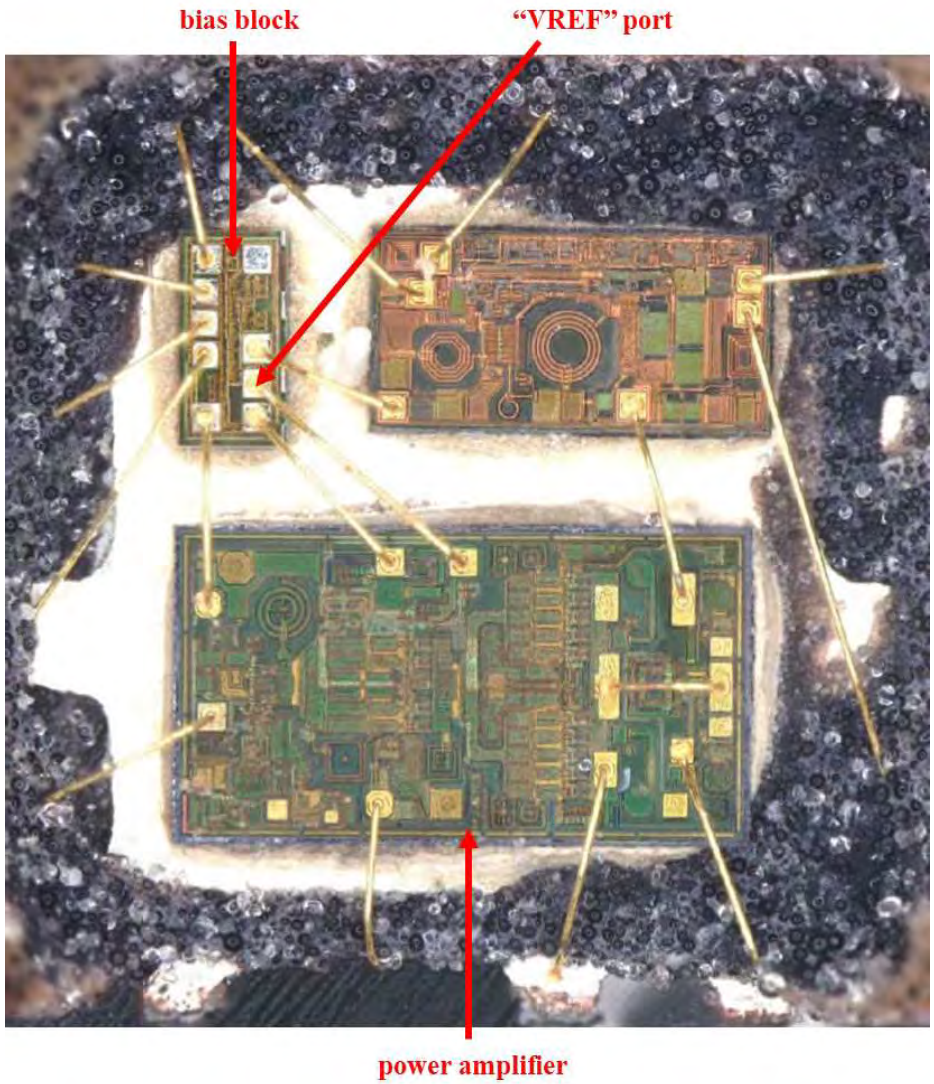
As shown by the schematic below for the primary biasing circuit of the KCT8576HE, the primary biasing circuit takes in the correction current as an input and generates the bias current for the power amplifier (as set forth above) based at least partly on the correction current.

	 *See, e.g.*, reverse engineered schematic of the primary biasing circuit of KCT8576HE
1[F] the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled,	In the KCT8576HE, the bias current is configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled. For example, the bias current is output by the "VREF" port of the bias block, as shown by the reverse engineered schematic for the KCT8576HE below.

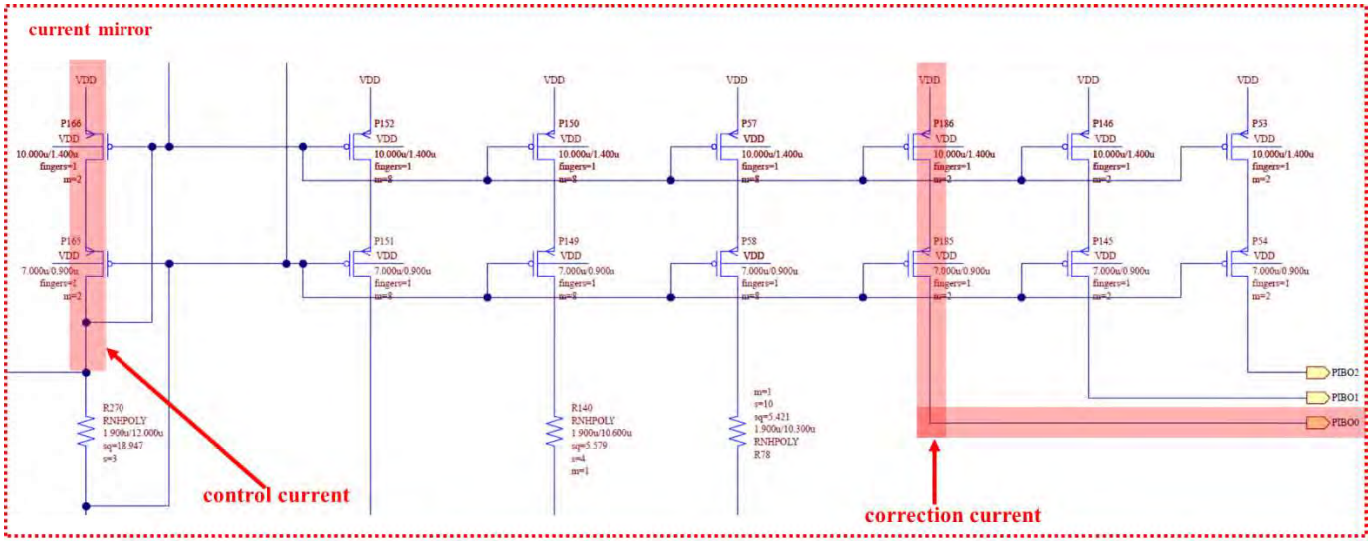


See, e.g., enlarged portion of reverse engineered schematic of the bias block of KCT8576HE

This bias current is input to the power amplifier for biasing the power amplifier to provide a suitable gain, including to correct for a variation in gain of the power amplifier when the power amplifier is enabled. As shown by the image below, the "VREF" port of the bias block is coupled to the die for the power amplifier via a wire bond.



See, e.g., photo of KCT8576HE showing three dies, including a die for the bias block and a die for the power amplifier of the power amplifier system

1[G] the current amplifier including a current mirror.	In the KCT8576HE, as shown by the reverse engineered schematic below, the current amplifier in the bias block includes a current mirror. The dashed box with the label below is one example of a current mirror that is included in the current amplifier.  *See, e.g.*, enlarged portion of reverse engineered schematic of the sub block of KCT8576HE For example, as explained in 1[D], the current amplifier in the bias block includes a current mirror configured to amplify the control current by a factor of about 1.
17[pre] A method of biasing a power amplifier, the method comprising:	To the extent the preamble of claim 17 is limiting, the KCT8576HE performs a method of biasing a power amplifier. For example, as explained in 1[pre] through 1[B], the KCT8576HE includes a bias block for biasing a power amplifier.
17[A] shaping an enable signal using a time-dependent signal	The KCT8576HE shapes an enable signal using a time-dependent signal generator to generate a control current.

generator to generate a control current;	For example, as explained in 1[C], the KCT8576HE includes a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current.
17[B] amplifying the control current using a current mirror of a current amplifier to generate a correction current; and	The KCT8576HE amplifies the control current using a current mirror of a current amplifier to generate a correction current. For example, as explained in 1[D], the KCT8576HE includes a current amplifier configured to amplify the control current to generate a correction current. As explained in 1[G], the current amplifier includes a current mirror that amplifies the control current to generate a correction current.
17[C] generating a bias current for a power amplifier using a primary biasing circuit, the primary biasing circuit configured to use the correction current to correct for a variation in gain of the power amplifier when the power amplifier is enabled.	The KCT8576HE generates a bias current for a power amplifier using a primary biasing circuit, the primary biasing circuit configured to use the correction current to correct for a variation in gain of the power amplifier when the power amplifier is enabled. For example, as explained in 1[E], the KCT8576HE includes a primary biasing circuit used to generate a bias current for the power amplifier based at least partly on the correction current. As explained in 1[F], the bias current is configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled. Since the bias current is at least partly based on the correction current, the primary biasing circuit is configured to use the correction current to correct for a variation in gain of the power amplifier when the power amplifier is enabled.
21[pre] A bias circuit for biasing a power amplifier, the bias circuit comprising:	To the extent the preamble of claim 21 is limiting, the KCT8576HE includes a bias circuit for biasing a power amplifier. For example, as explained in 1[pre] through 1[B], the KCT8576HE includes a bias block, which is a bias circuit, for biasing a power amplifier.
21[A] a time-dependent signal generator configured to shape an enable	The KCT8576HE includes the bias circuit comprising a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current.

signal of the power amplifier to generate a control current;	For example, as explained in 1[C], the KCT8576HE includes a bias circuit including a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current.
21[B] a current amplifier configured to amplify the control current to generate a correction current,	The KCT8576HE includes the bias circuit comprising a current amplifier configured to amplify the control current to generate a correction current. For example, as explained in 1[D], the bias circuit in the KCT8576HE includes a current amplifier configured to amplify the control current to generate a correction current.
21[C] the current amplifier including a current mirror; and	In the KCT8576HE, the current amplifier includes a current mirror. For example, as explained in 1[G], the current amplifier in the KCT8576HE includes a current mirror.
21[D] a primary biasing block configured to generate a bias current for the power amplifier based at least partly on the correction current,	The KCT8576HE includes the bias circuit comprising a primary biasing block configured to generate a bias current for the power amplifier based at least partly on the correction current. For example, as explained in 1[E], the bias circuit in the KCT8576HE includes a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current.
21[E] the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled.	In the KCT8576HE, the bias current is configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled. For example, as explained in 1[F], the bias current is input to the power amplifier for biasing the power amplifier to provide a suitable gain, including to correct for a variation in gain of the power amplifier when the power amplifier is enabled.

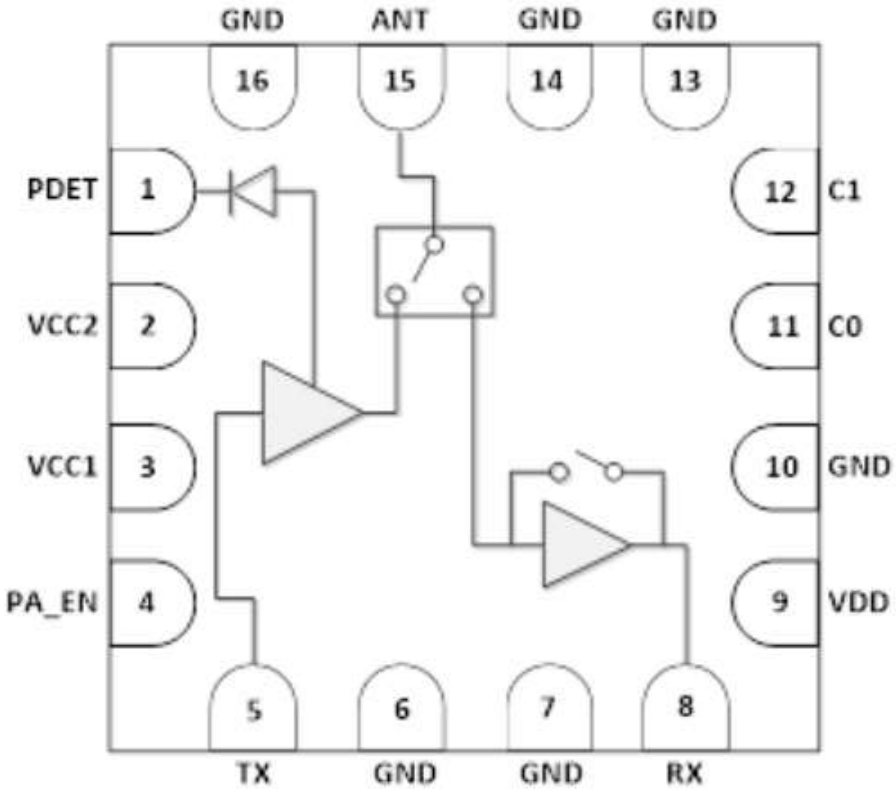
EXHIBIT 13

EXHIBIT 13
SKYWORKS SOLUTIONS, INC.'S INFRINGEMENT CHART
KCT8239S
U.S. Patent No. 8,717,101
Independent Claims 1, 17, and 21

Skyworks Solutions, Inc. ("Skyworks") provides this exemplary claim chart for independent claims 1, 17, and 21 of U.S. Patent No. 8,717,101 (the "'101 patent") applied to Kangxi Communication Technologies (Shanghai) Co., Ltd's and Grand Chip Labs, Inc.'s (collectively, "KCT") KCT8239S product. The disclosures in this claim chart directed to the KCT8239S are also more broadly directed to any sale, offer for sale, use, or importation of the KCT8239S in the U.S., including in an end product such as a wireless router or as a standalone product that is not incorporated in an end product.

The claim chart below demonstrates infringement by comparing each element of the charted claims to corresponding components, aspects, and/or features of the KCT8239S product. This claim chart is not intended to constitute an expert report on infringement. This claim chart includes information provided by way of example, and not by way of limitation.

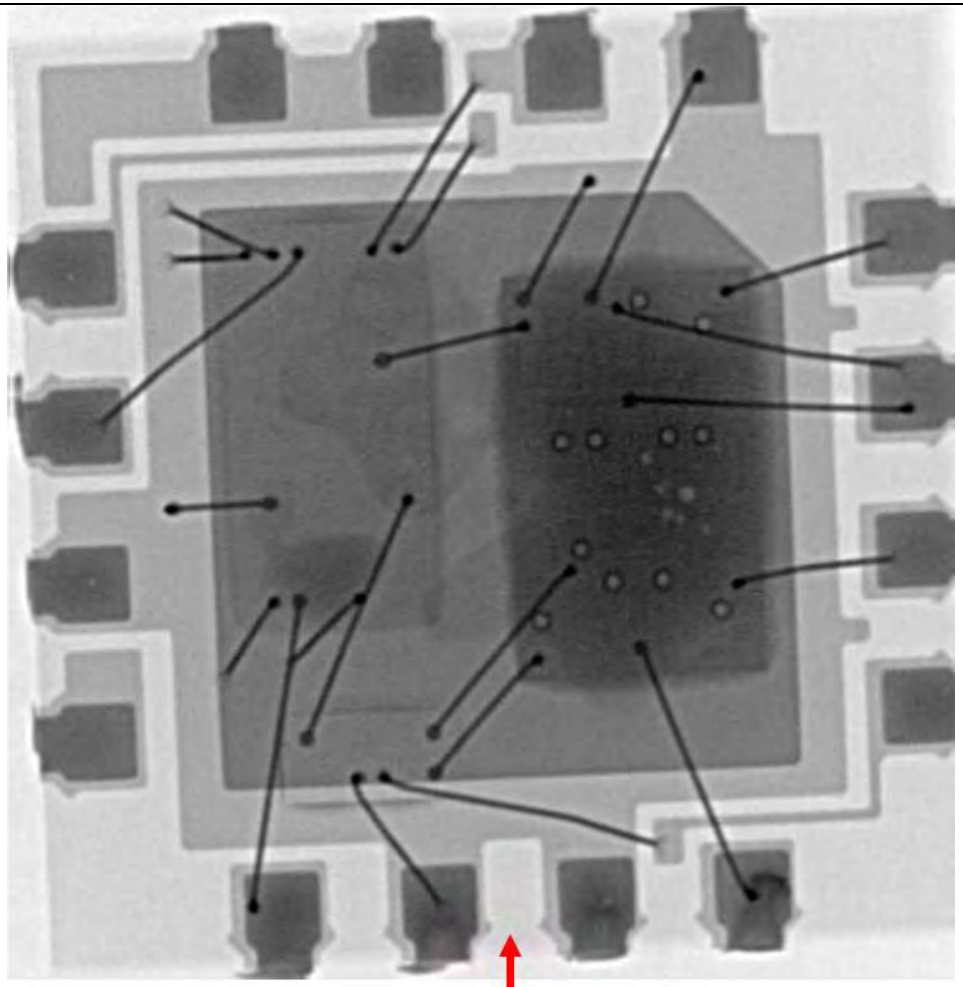
The analysis set forth below is based only upon information from publicly available sources regarding the KCT8239S product. Further analysis of non-public information during fact discovery will likely assist in identifying all infringing features and functionalities used by KCT in the KCT8239S product. Accordingly, Skyworks reserves the right to supplement this infringement analysis once such information is made available to Skyworks. Further, Skyworks reserves the right to supplement this infringement analysis, as appropriate, upon issuance of an order construing any terms recited in the asserted claims or as other circumstances so merit.

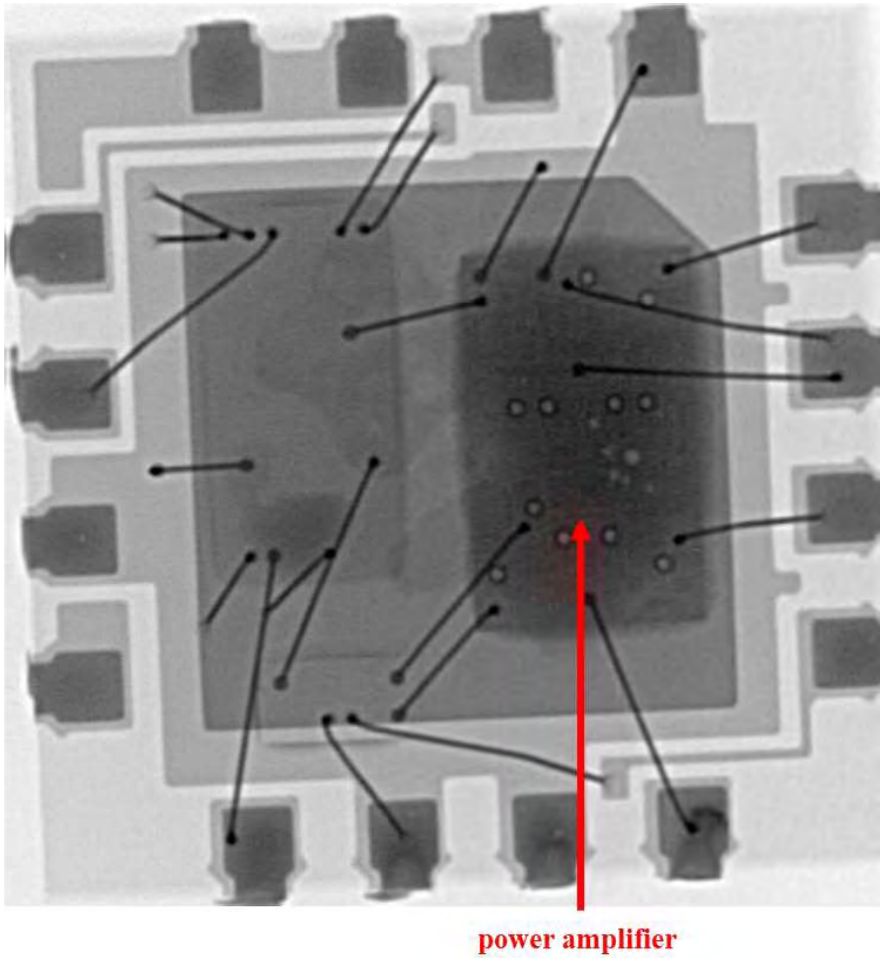
Claims	KCT8239S
1[pre] A power amplifier system comprising:	To the extent the preamble of claim 1 is limiting, the KCT8239S includes a power amplifier system. The KCT8239S is a product for Wi-Fi connectivity. For example, the following image for the KCT8239S is a simplified block diagram for this product.[1]  *See, e.g.*, simplified block diagram for KCT8239S

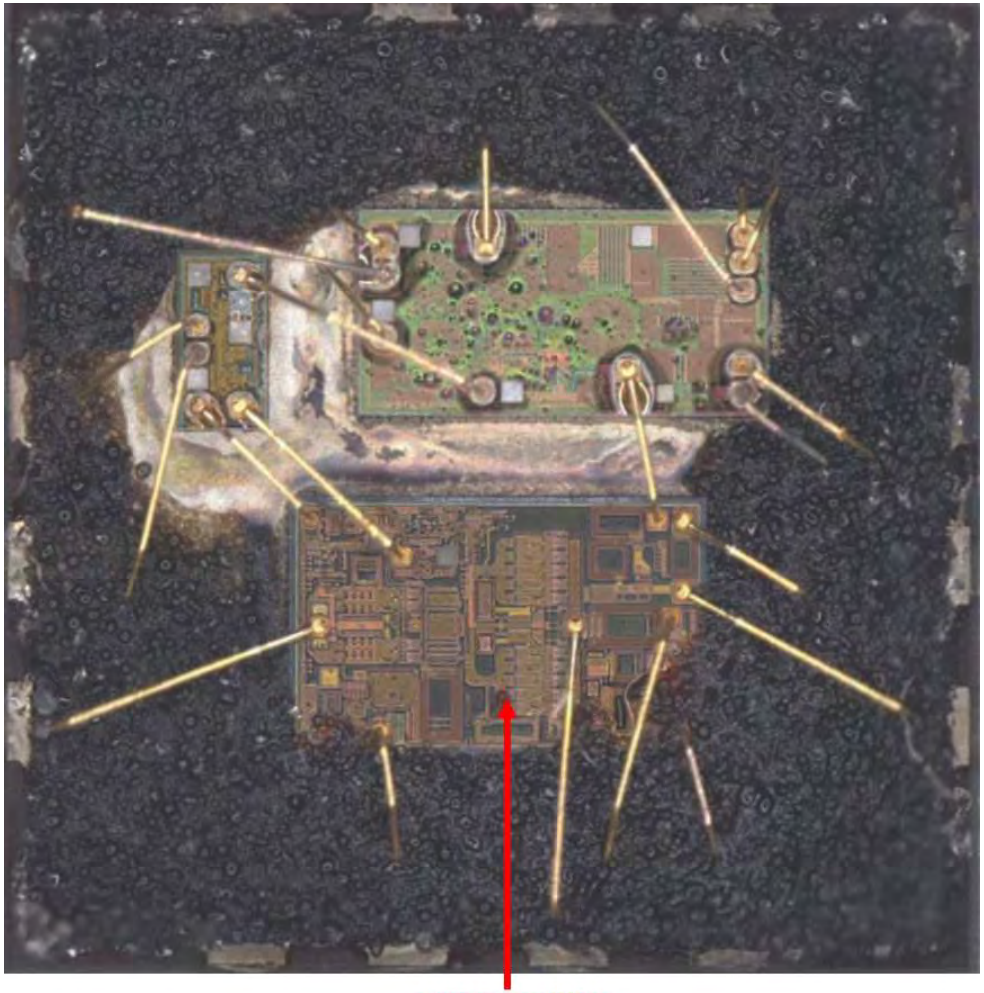
[1] *See* https://perma.cc/NS2E-VPYU.

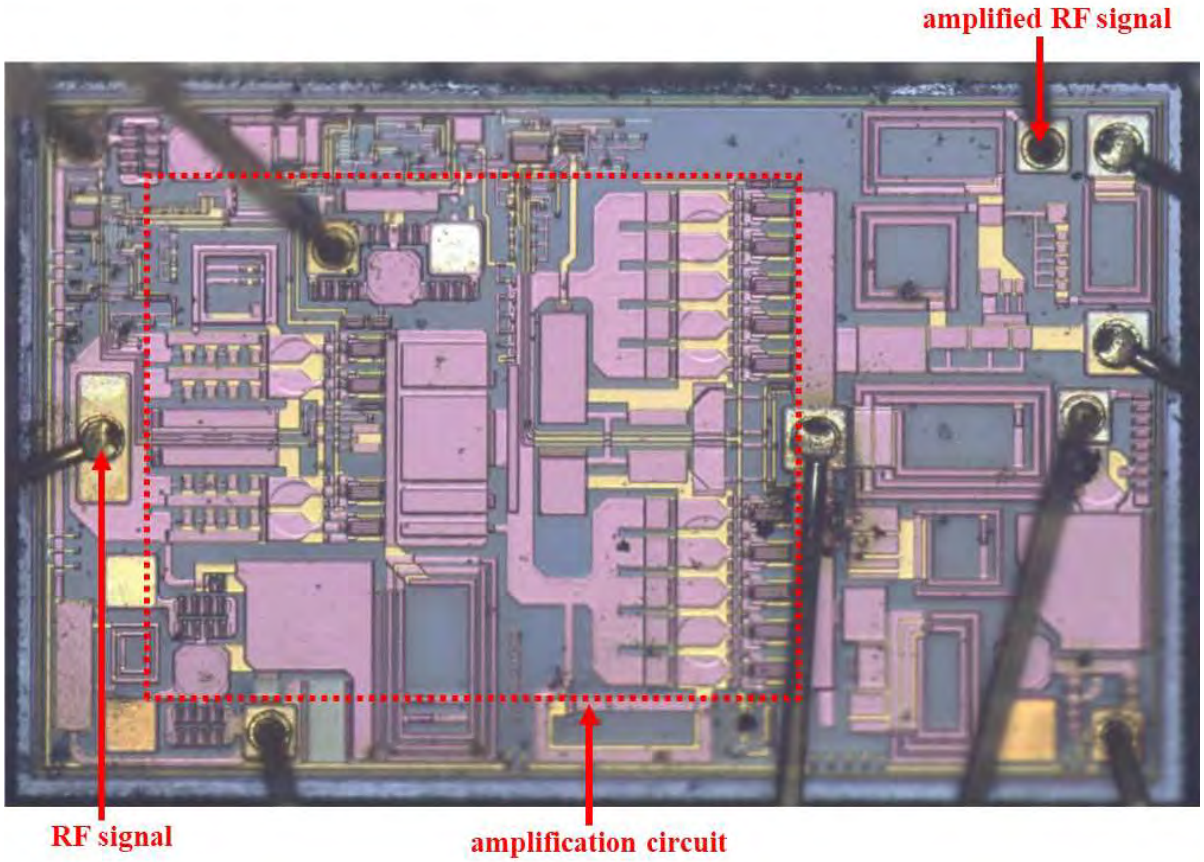
	The KCT8239S is, according to KCT, "a fully integrated 802.11b/g/n/ac/ax WLAN RF Front-end module (FEM) which incorporates key RF functionality. It is integrated with a high-efficiency power amplifier (PA), a low noise amplifier (LNA) with bypass …."[2] For example, the image below of the KCT8239S shows a power amplifier system (as indicated by the corresponding label below) within the KCT8239S.

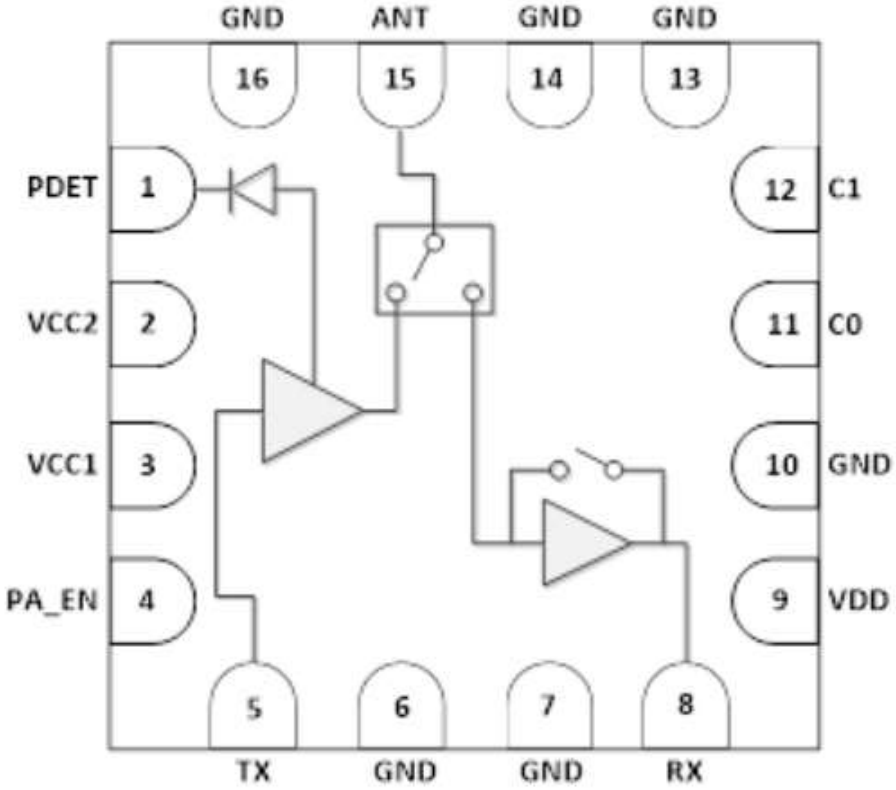
[2] *See* https://perma.cc/NS2E-VPYU.

	 *See, e.g.*, photo of KCT8239S showing three dies of the power amplifier system
1[A] a power amplifier configured	The KCT8239S includes a power amplifier configured to amplify a radio frequency (RF) signal.

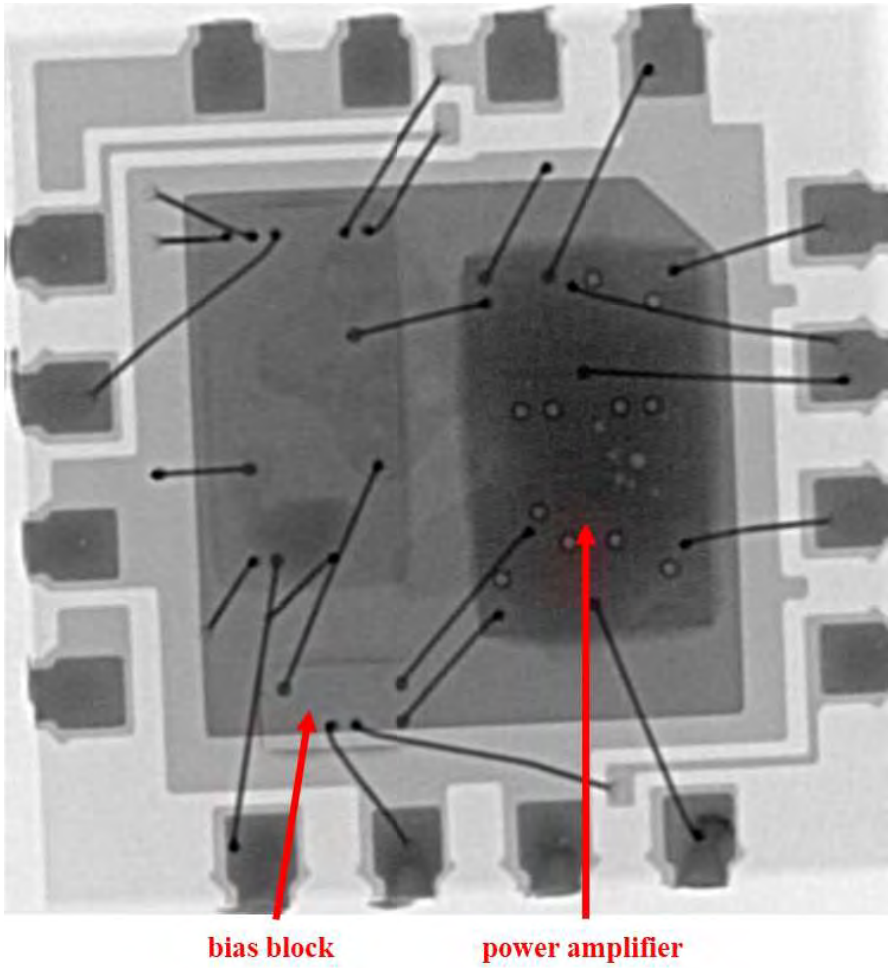
to amplify a radio frequency (RF) signal; and	For example, the image of the KCT8239S below shows a power amplifier (as indicated by the corresponding label below) as part of the power amplifier system.  *See, e.g.*, photo of KCT8239S showing three dies, including a die for the power amplifier of the power amplifier system

	The image below shows the die of the power amplifier as part of the power amplifier system for the KCT8239S.  *See, e.g.*, photo of KCT8239S showing three dies, including the die for the power amplifier of the power amplifier system

	The image below shows an enlarged view of the power amplifier die of the KCT8239S. The power amplifier in the KCT8239S is coupled so that it is configured to receive as an input a radio frequency (RF) signal, as labeled below, and amplify the RF signal to output an amplified RF signal, as labeled below. The dashed box with the corresponding label below is one example of an amplification circuit that provides the amplification of the RF signal.  *See, e.g.*, photo of the power amplifier die in KCT8239S

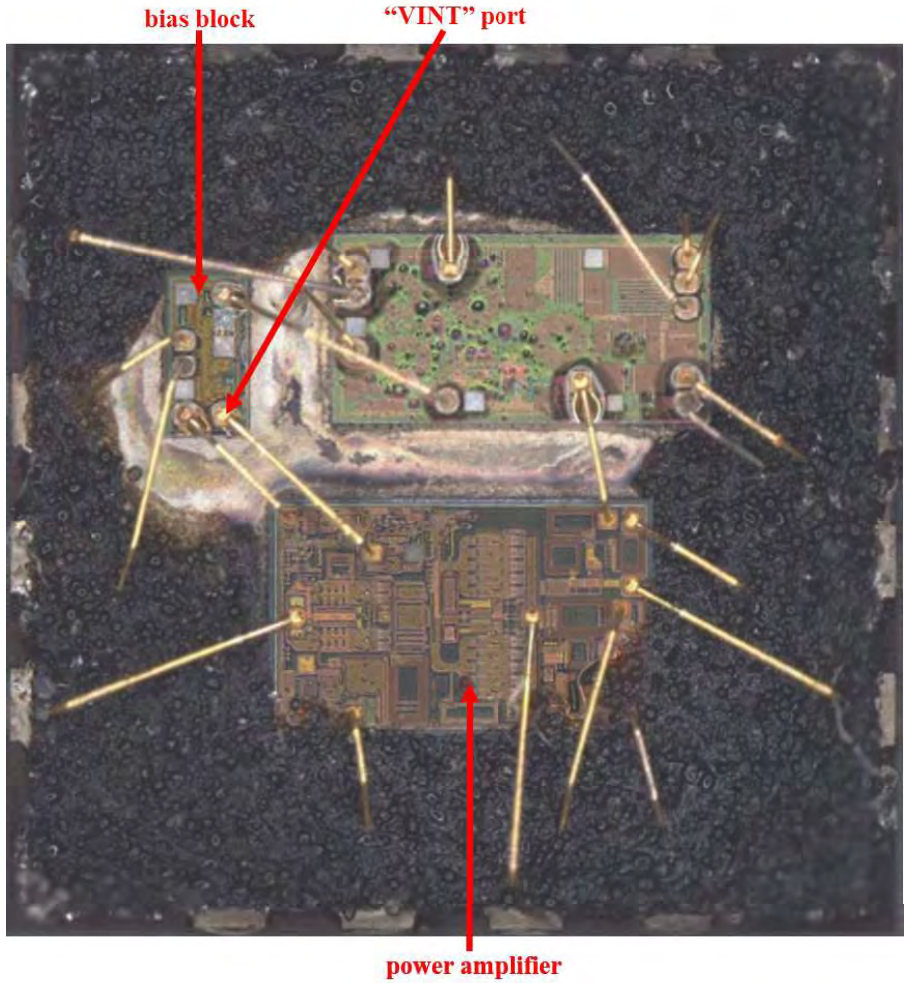
	As shown below in KCT's simplified block diagram for the KCT8239S, a power amplifier is part of the KCT8239S product. Specifically, the KCT8239S "is integrated with a high-efficiency power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated matching network and a single-pole, double-throw (SPDT) switch all in one device."[3]  *See, e.g.*, simplified block diagram for KCT8239S
1[B] a bias block for biasing the power amplifier,	The KCT8239S includes a bias block for biasing the power amplifier. For example, the image of the KCT8239S below shows a bias block (as indicated by the corresponding label below) as part of the power amplifier system.

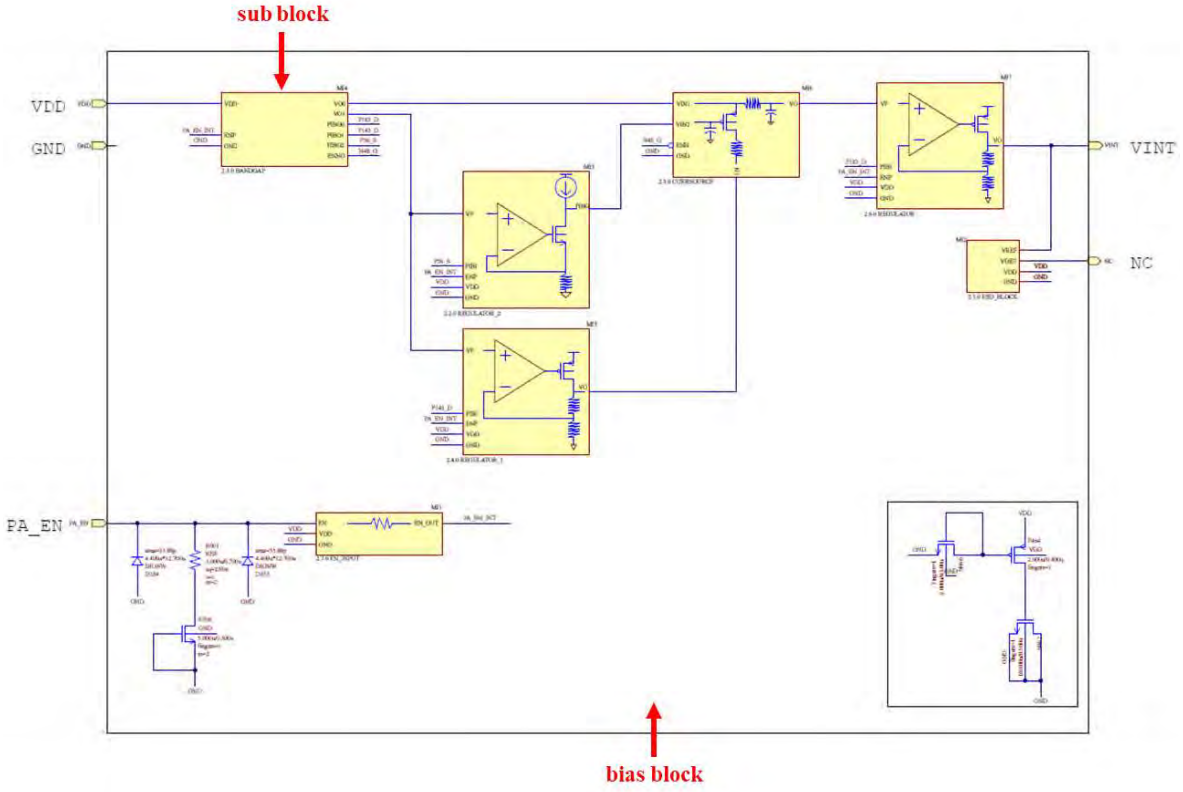
[3] *See* https://perma.cc/NS2E-VPYU.

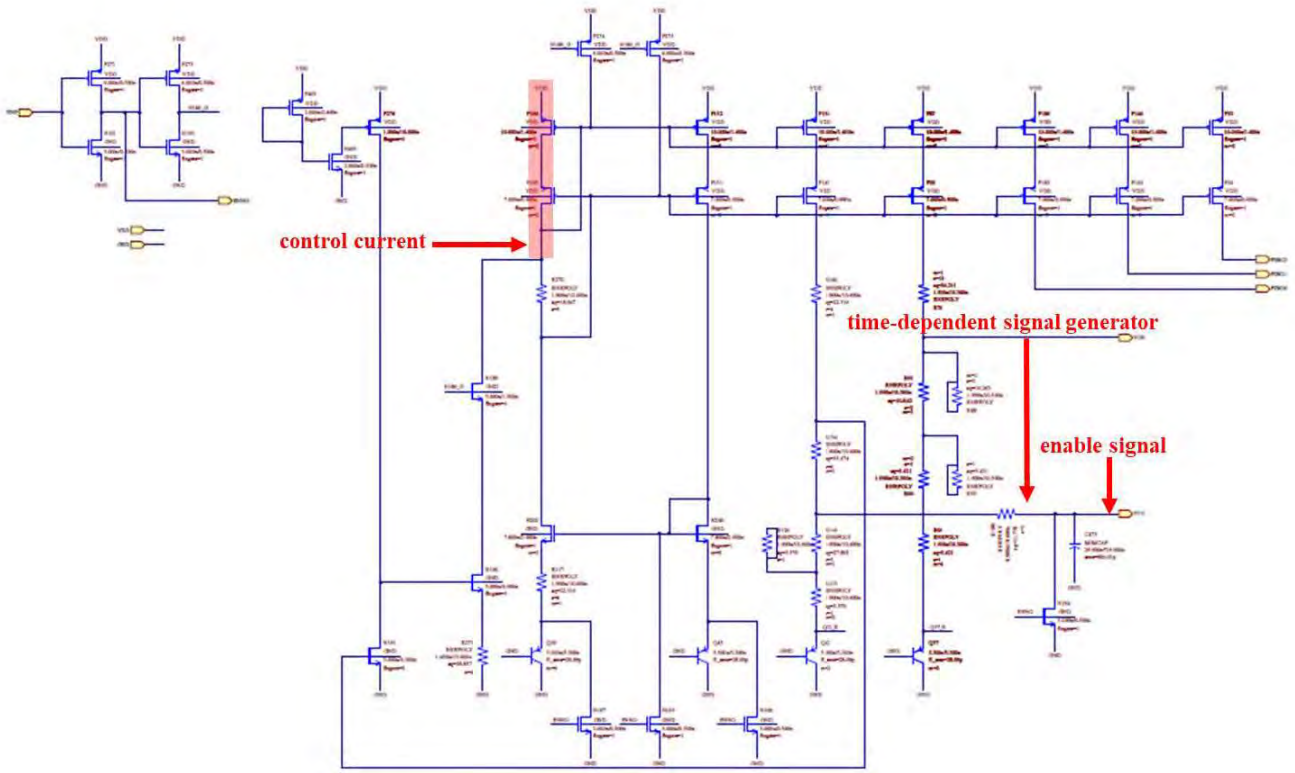


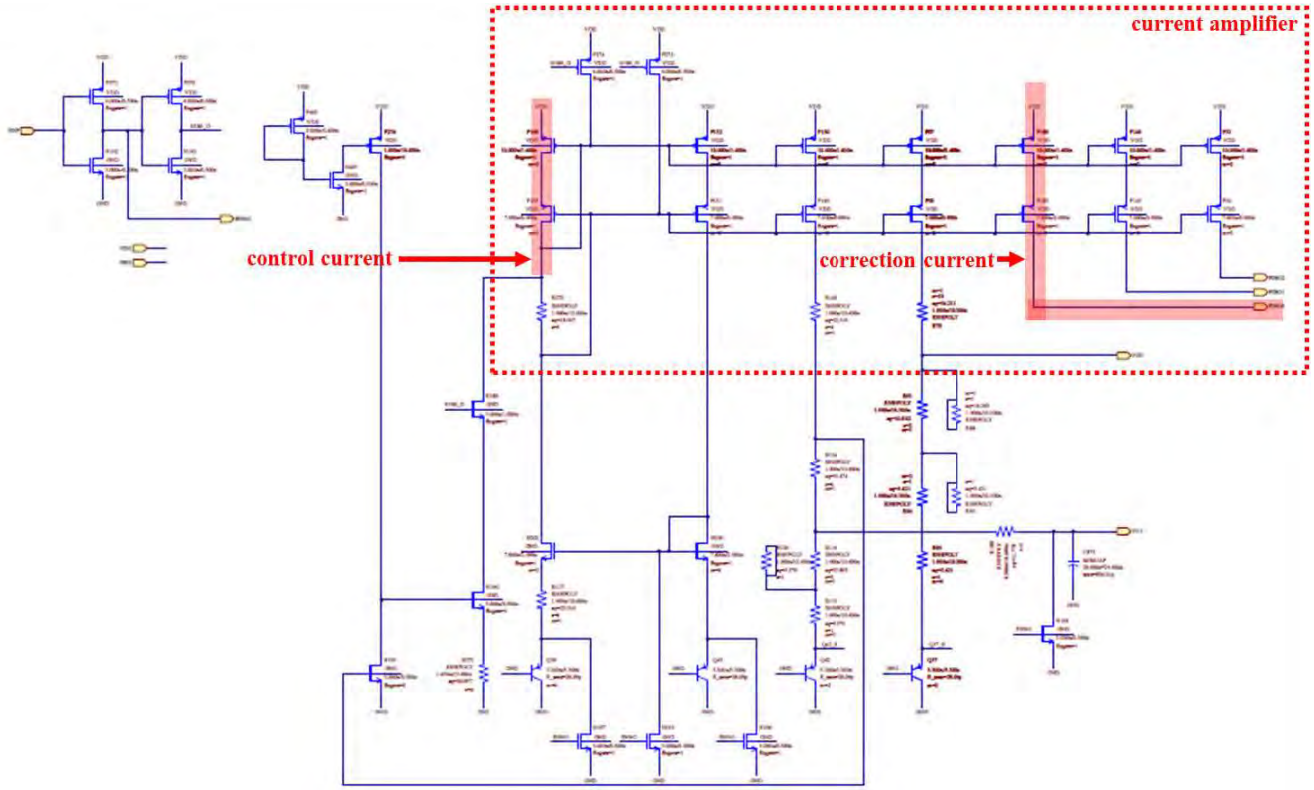
See, e.g., photo of KCT8239S showing three dies, including a die for the bias block and a die for the power amplifier of the power amplifier system

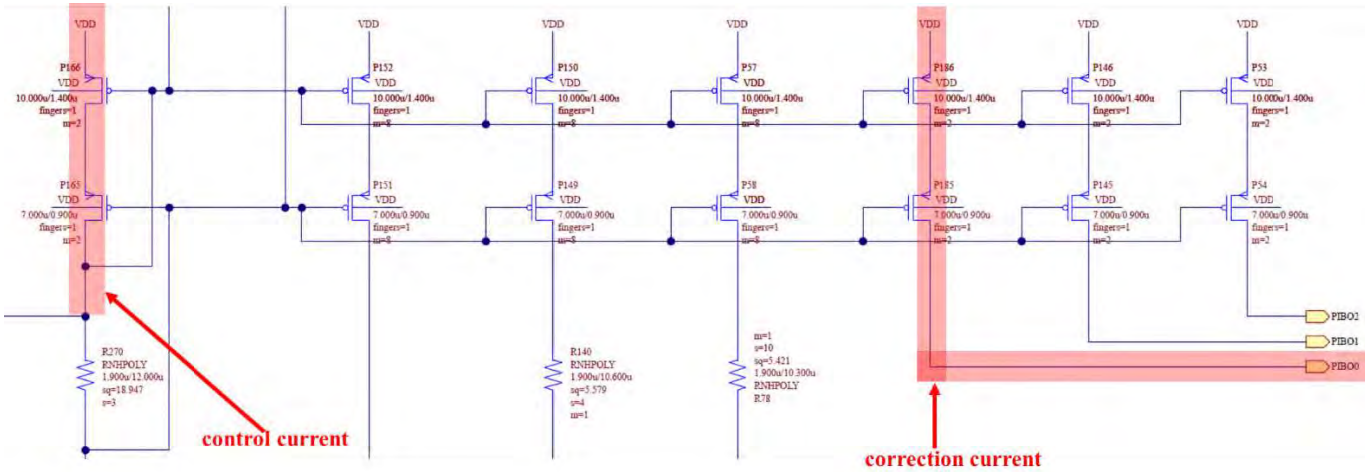
The image below shows the power amplifier and the bias block within the power amplifier system in another angle for the KCT8239S. The bias block is coupled to the power amplifier so that the bias block

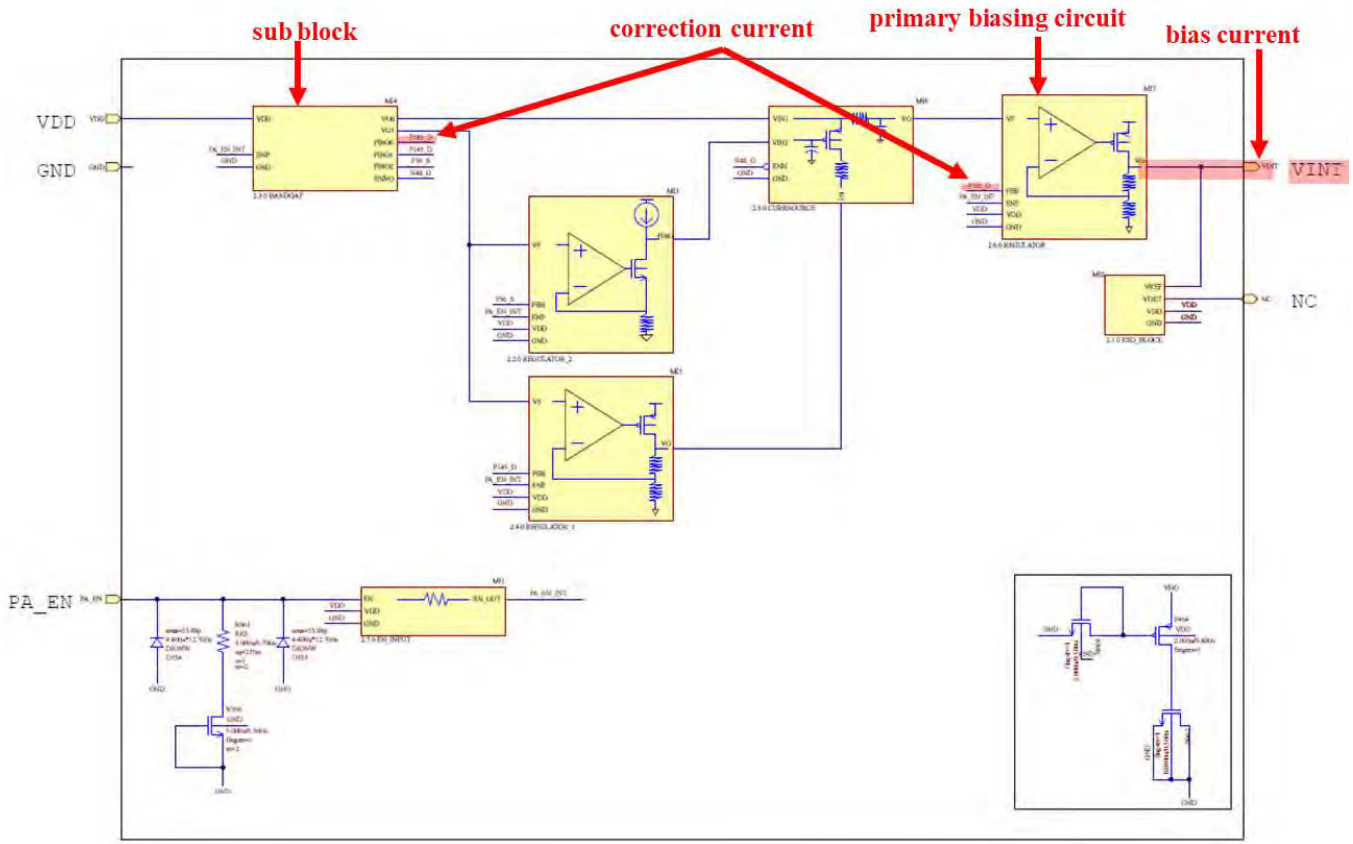
	biases the power amplifier using a bias current through a wire bond connecting a "VINT" port (as indicated by the corresponding label below) of the bias block to the power amplifier.  *See, e.g.*, photo of KCT8239S showing three dies, including a die for the bias block and a die for the power amplifier of the power amplifier system *See also* elements 1[C]-1[E] (showing details of the bias circuit).

1[C] the bias block including a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current,	The KCT8239S includes the bias block including a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current. For example, the reverse engineered schematic below is for the bias block (as indicated by the corresponding label below) in the KCT8239S. It includes a sub block (as indicated by the corresponding label below). The sub block includes a time-dependent signal generator.  *See, e.g.*, reverse engineered schematic of the bias block of KCT8239S The reverse engineered schematic below for the KCT8239S shows the internal details of the sub block set forth above. This schematic includes a time-dependent signal generator (as indicated by the corresponding

	label below). This time-dependent signal generator is configured to shape an enable signal (as indicated by the corresponding label below) of the power amplifier to generate a control current (as indicated by the corresponding label below). The time-dependent signal generator shapes the enable signal to generate the control current in that the enable signal is a time-dependent voltage and the control current depends on the enable signal.  *See, e.g.*, reverse engineered schematic of the sub block of KCT8239S
1[D] a current amplifier configured to amplify the control	In the KCT8239S, the bias block includes a current amplifier configured to amplify the control current to generate a correction current.

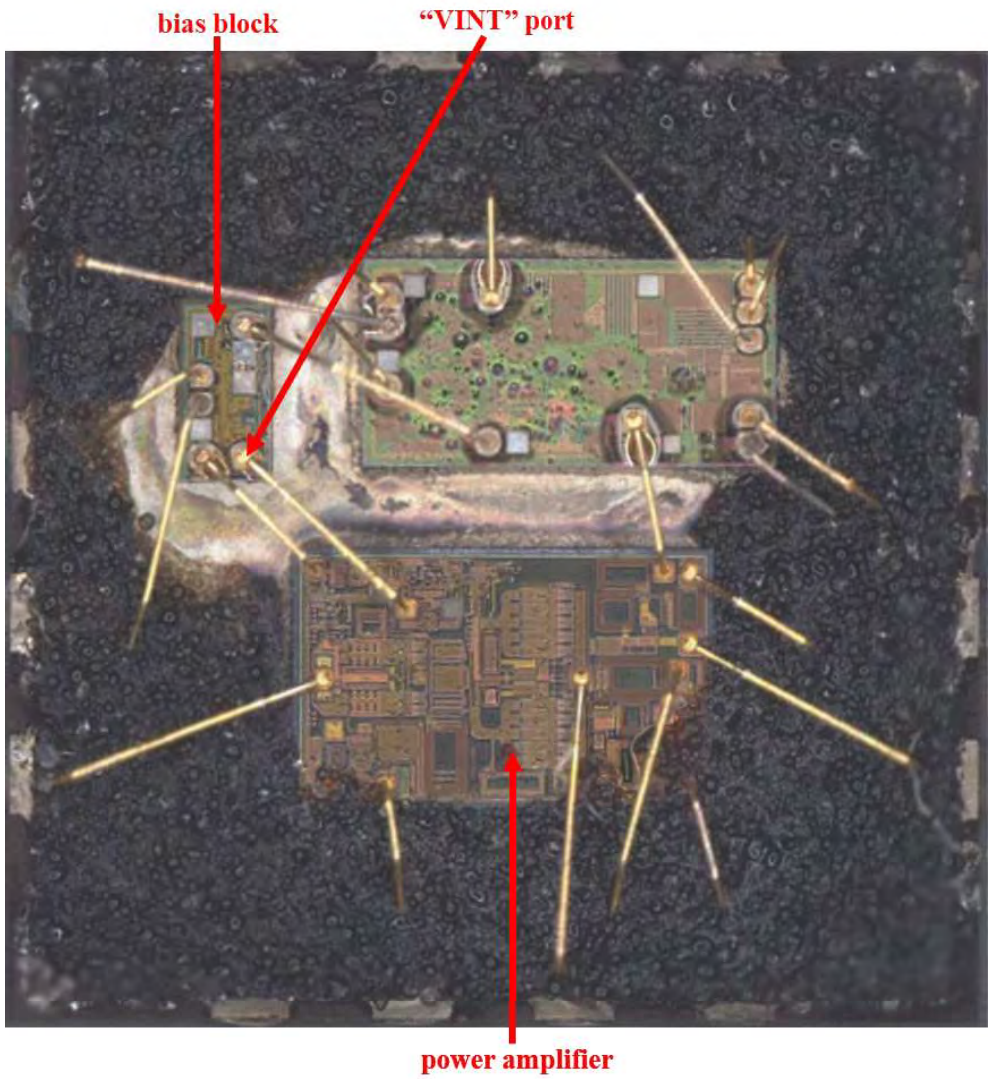
current to generate a correction current,	For example, as shown by the reverse engineered schematic below for the sub block of the KCT8239S, the bias block includes a current amplifier (as indicated by the corresponding label below). The current amplifier is configured to amplify the control current to generate a correction current (as indicated by the corresponding label below). The dashed box with the label below is one example of a current amplifier that amplifies the control current to generate the correction current.  *See, e.g.*, reverse engineered schematic of the sub block of KCT8239S The schematic below for the KCT8239S is an enlarged view of a portion of the current amplifier identified above, which is a current mirror configured to amplify the control current to generate the correction current. As set forth in the '101 patent, a current mirror can have any suitable gain. *See* '101 patent, 11:39-45. For example, the current mirror in KCT8239S is configured to amplify the control current by a

	factor of about 1, based on the multiple numbers designated in the schematic below (e.g., "m=2" for the control current and "m=2" for the correction current).  *See, e.g.*, enlarged portion of reverse engineered schematic of the sub block of KCT8239S
1[E] and a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current,	In the KCT8239S, the bias block includes a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current. For example, as shown in the reverse engineered schematic for the KCT8239S below, a primary biasing circuit (as indicated by the corresponding label below) is configured to generate a bias current (as indicated by the corresponding label below) for the power amplifier based at least partly on the correction current.

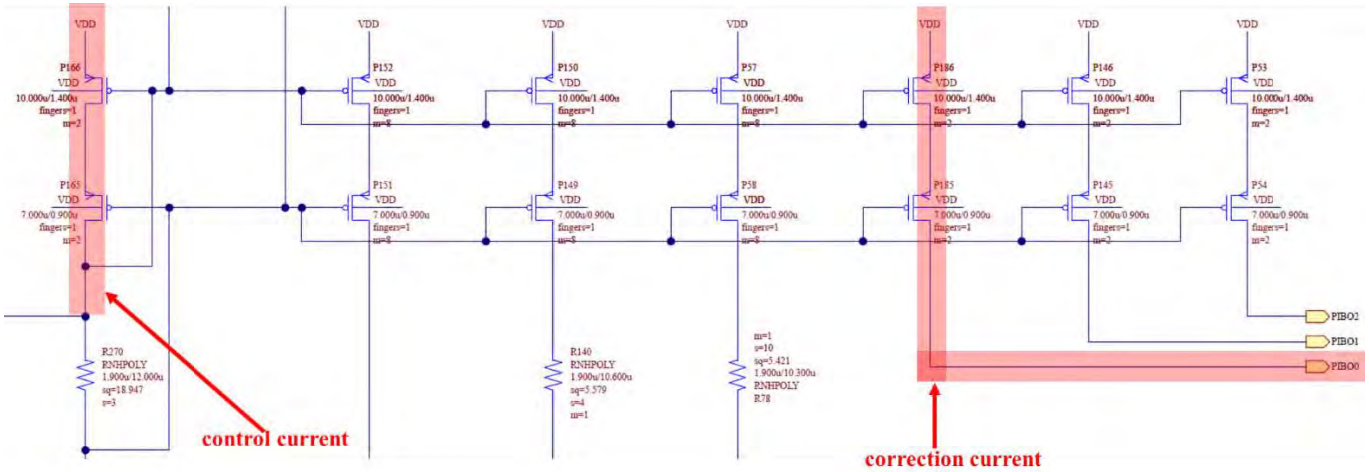


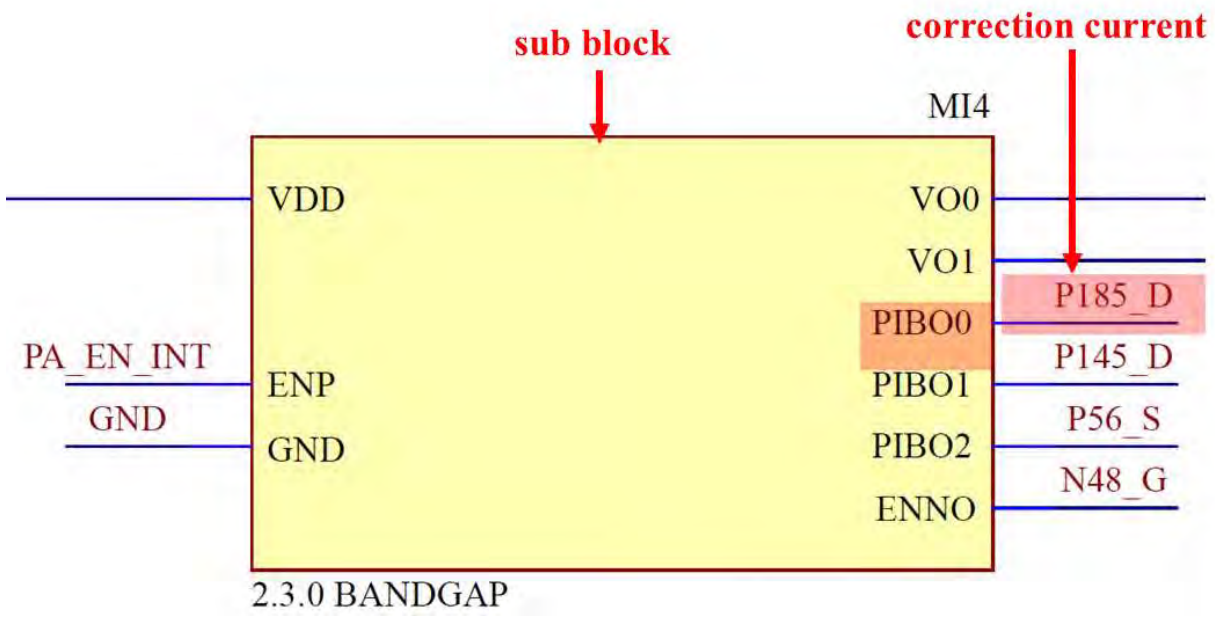
See, e.g., reverse engineered schematic of the bias block of KCT8239S

The bias block biases the power amplifier using the bias current through a wire bond connecting a "VINT" port (as highlighted above and indicated by the corresponding label below) of the bias block to the power amplifier.



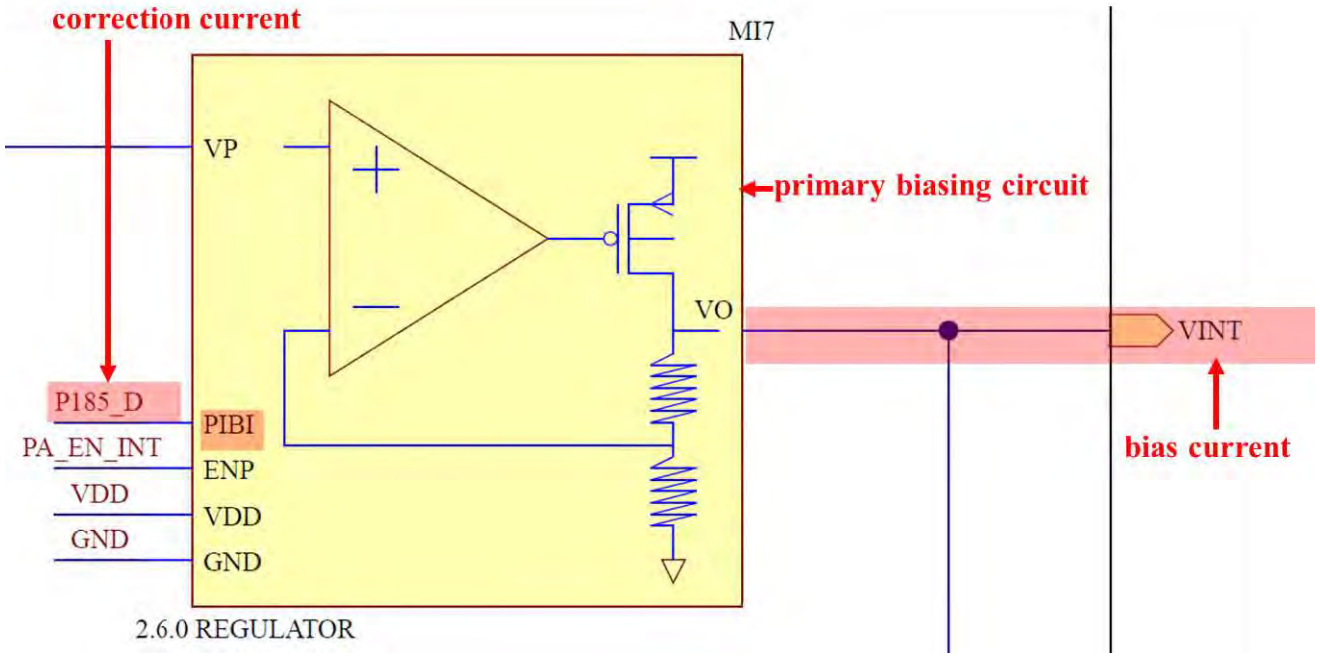
See, e.g., photo of KCT8239S showing three dies, including a die for the bias block and a die for the power amplifier of the power amplifier system

	The correction current is output by the "PIBO0" port of the sub block including the time-dependent signal generator, as shown by the reverse engineered schematics below.  *See, e.g.*, enlarged portion of reverse engineered schematic of the sub block of KCT8239S



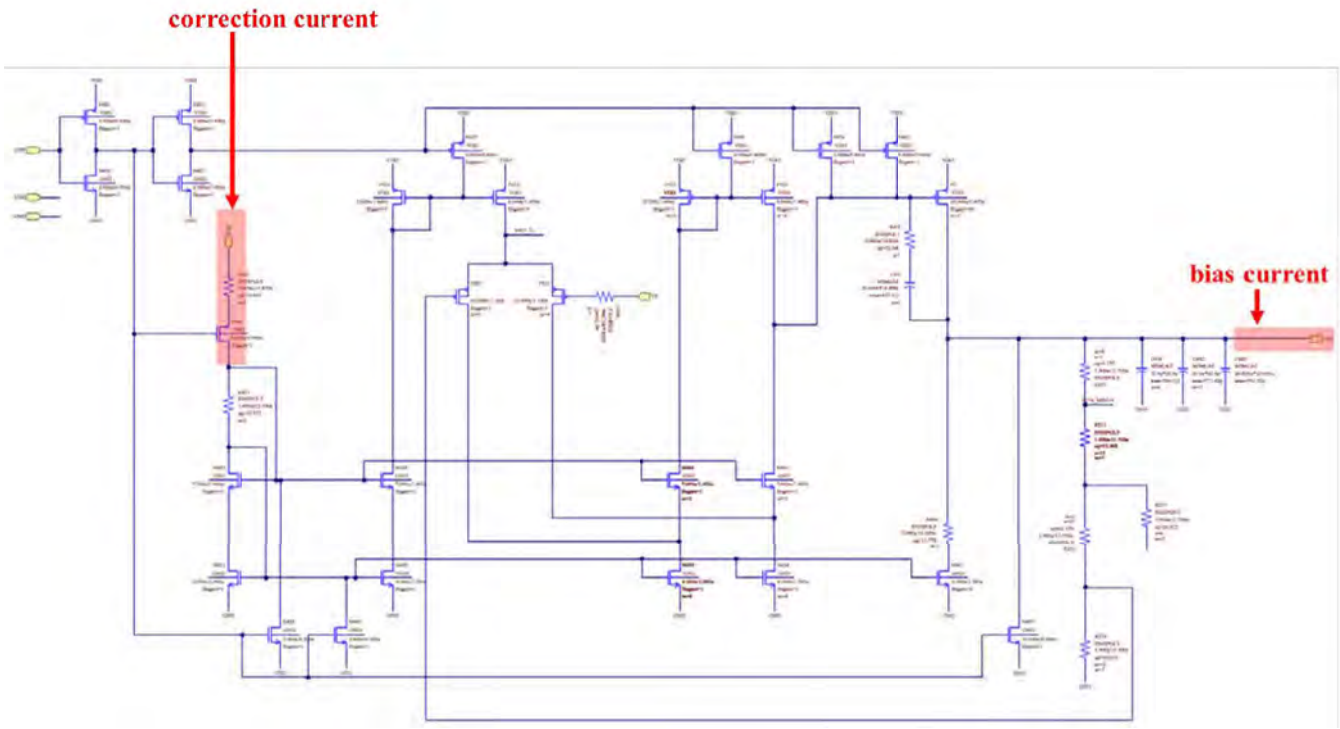
See, e.g., enlarged portion of reverse engineered schematic of the bias block of KCT8239S

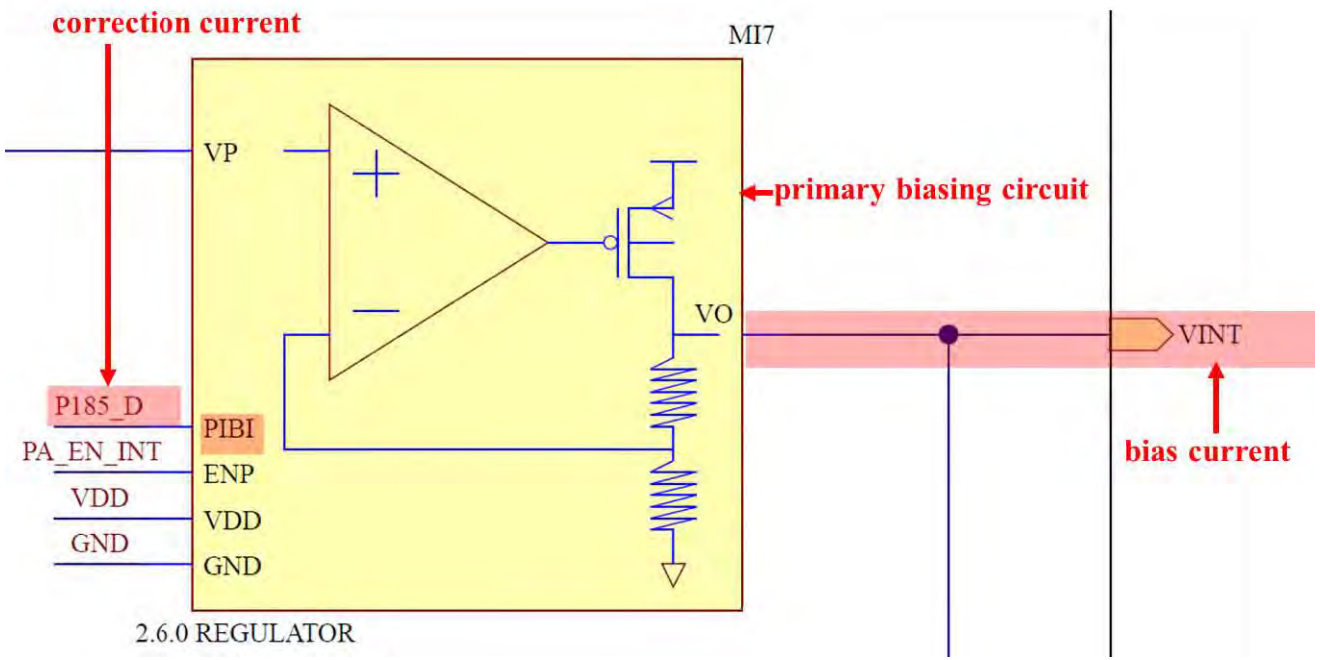
The "PIBO0" port of the sub block (shown above and as corresopnding to P185_D) including the time-dependent signal generator is connected to the "PIBI" port of the primary biasing circuit (as indicated by the corresponding label below showing P185_D connecting to PIBI), as shown by the schematic below.



See, e.g., enlarged portion of reverse engineered schematic of the bias block of KCT8239S

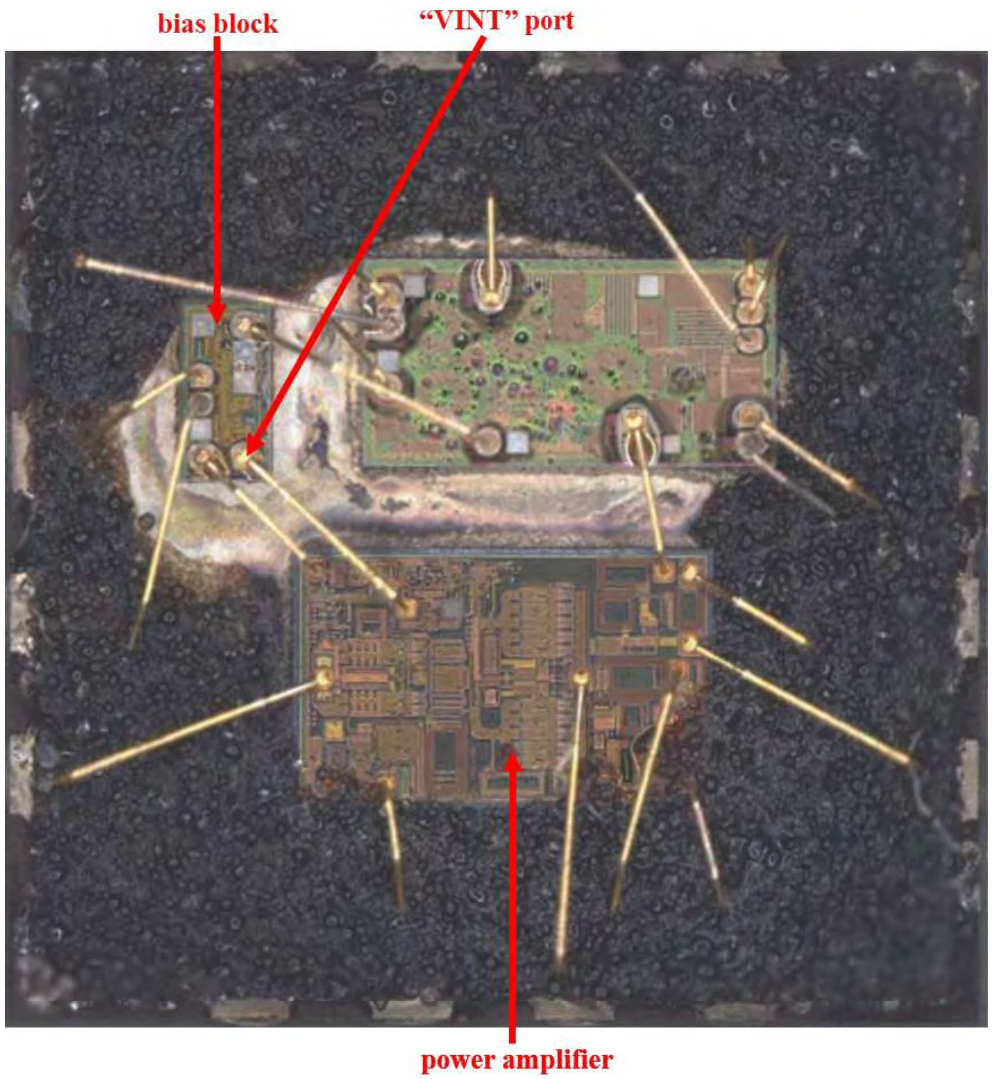
As shown by the schematic below for the primary biasing circuit of the KCT8239S, the primary biasing circuit takes in the correction current as an input and generates the bias current for the power amplifier (as set forth above) based at least partly on the correction current.

	 *See, e.g.*, reverse engineered schematic of the primary biasing circuit of KCT8239S
1[F] the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled,	In the KCT8239S, the bias current is configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled. For example, the bias current is output by the "VINT" port of the bias block, as shown by the reverse engineered schematic for the KCT8239S below.

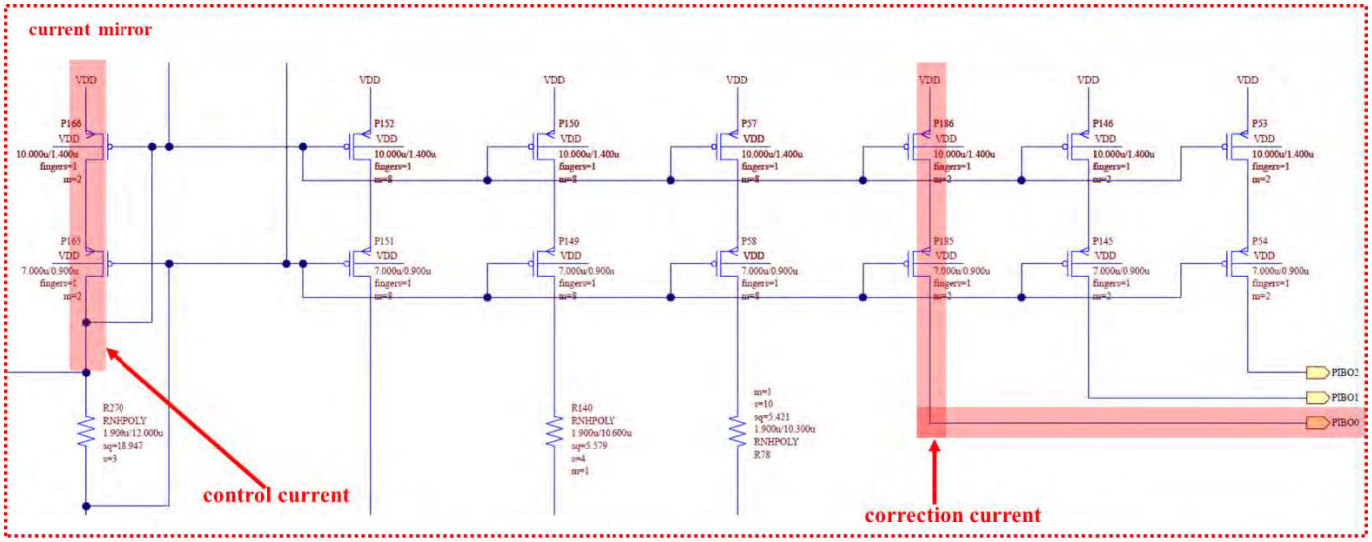


See, e.g., enlarged portion of reverse engineered schematic of the bias block of KCT8239S

This bias current is input to the power amplifier for biasing the power amplifier to provide a suitable gain, including to correct for a variation in gain of the power amplifier when the power amplifier is enabled. As shown by the image below, the "VINT" port of the bias block is coupled to the die for the power amplifier via a wire bond.



See, e.g., photo of KCT8239S showing three dies, including a die for the bias block and a die for the power amplifier of the power amplifier system

1[G] the current amplifier including a current mirror.	In the KCT8239S, as shown by the reverse engineered schematic below, the current amplifier in the bias block includes a current mirror. The dashed box with the label below is one example of a current mirror that is included in the current amplifier.  *See, e.g.*, enlarged portion of reverse engineered schematic of the sub block of KCT8239S For example, as explained in 1[D], the current amplifier in the bias block includes a current mirror configured to amplify the control current by a factor of about 1.
17[pre] A method of biasing a power amplifier, the method comprising:	To the extent the preamble of claim 17 is limiting, the KCT8239S performs a method of biasing a power amplifier. For example, as explained in 1[pre] through 1[B], the KCT8239S includes a bias block for biasing a power amplifier.
17[A] shaping an enable signal using a time-dependent signal	The KCT8239S shapes an enable signal using a time-dependent signal generator to generate a control current.