generator to generate a control current;	For example, as explained in 1[C], the KCT8239S includes a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current.
17[B] amplifying the control current using a current mirror of a current amplifier to generate a correction current; and	The KCT8239S amplifies the control current using a current mirror of a current amplifier to generate a correction current. For example, as explained in 1[D], the KCT8239S includes a current amplifier configured to amplify the control current to generate a correction current. As explained in 1[G], the current amplifier includes a current mirror that amplifies the control current to generate a correction current.
17[C] generating a bias current for a power amplifier using a primary biasing circuit, the primary biasing circuit configured to use the correction current to correct for a variation in gain of the power amplifier when the power amplifier is enabled.	The KCT8239S generates a bias current for a power amplifier using a primary biasing circuit, the primary biasing circuit configured to use the correction current to correct for a variation in gain of the power amplifier when the power amplifier is enabled. For example, as explained in 1[E], the KCT8239S includes a primary biasing circuit used to generate a bias current for the power amplifier based at least partly on the correction current. As explained in 1[F], the bias current is configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled. Since the bias current is at least partly based on the correction current, the primary biasing circuit is configured to use the correction current to correct for a variation in gain of the power amplifier when the power amplifier is enabled.
21[pre] A bias circuit for biasing a power amplifier, the bias circuit comprising:	To the extent the preamble of claim 21 is limiting, the KCT8239S includes a bias circuit for biasing a power amplifier. For example, as explained in 1[pre] through 1[B], the KCT8239S includes a bias block, which is a bias circuit, for biasing a power amplifier.
21[A] a time-dependent signal generator configured to shape an enable	The KCT8239S includes the bias circuit comprising a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current.

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IPR2025-00372
Part 3 of 4

signal of the power amplifier to generate a control current;	For example, as explained in 1[C], the KCT8239S includes a bias circuit including a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current.
21[B] a current amplifier configured to amplify the control current to generate a correction current,	The KCT8239S includes the bias circuit comprising a current amplifier configured to amplify the control current to generate a correction current. For example, as explained in 1[D], the bias circuit in the KCT8239S includes a current amplifier configured to amplify the control current to generate a correction current.
21[C] the current amplifier including a current mirror; and	In the KCT8239S, the current amplifier includes a current mirror. For example, as explained in 1[G], the current amplifier in the KCT8239S includes a current mirror.
21[D] a primary biasing block configured to generate a bias current for the power amplifier based at least partly on the correction current,	The KCT8239S includes the bias circuit comprising a primary biasing block configured to generate a bias current for the power amplifier based at least partly on the correction current. For example, as explained in 1[E], the bias circuit in the KCT8239S includes a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current.
21[E] the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled.	In the KCT8239S, the bias current is configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled. For example, as explained in 1[F], the bias current is input to the power amplifier for biasing the power amplifier to provide a suitable gain, including to correct for a variation in gain of the power amplifier when the power amplifier is enabled.

EXHIBIT 14

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March 7, 2023

Kangxi Communication Technologies (Shanghai) Co., Ltd.
5th Floor, Building 10
No. 399 Keyuan Road
Pudong New Area, Shanghai
Attention: President and CEO

Re: Notice of Skyworks Solutions, Inc. Patents / Potential Infringement of Skyworks Patent(s): US Patent # 7,409,200

Dear Mr. President / CEO,

I am writing to you on behalf of Skyworks Solutions, Inc. ("Skyworks") as representative IP legal counsel for Skyworks regarding the above referenced matter. It has come to the attention of Skyworks that Kangxi Communications Technologies / Grand Chips Technology Corporation ("Kangxi"), with Corporate Headquarters listed respectively as Kangxi Communication Technologies (Shanghai) Co., Ltd., 5th Floor, Building 10, No. 399 Keyuan Road Pudong New Area, Shanghai / Grand Chip Labs Inc. 14151 Newport Ave, Unit 204, Tustin, CA 92780, is currently manufacturing, having manufactured, using, offering for sale, selling and importing certain products that appear to fall directly within the scope of certain Skyworks Intellectual Property Rights. As such, Skyworks is taking this opportunity to apprise Kangxi of our Intellectual Property Rights in writing in order to communicate our serious concerns regarding the currently offered Kangxi product(s) that we believe utilize certain claimed subject matter of Skyworks Patent(s).

Based upon our analysis, it is our belief that certain Kangxi products, in particular the KCT8528HE product, appear to fall within the scope of and likely infringes US Patent # 7,409,200, along with other related KCT products of similar design. In particular, we direct your attention to Claims 1, 2 and 18 of US Patent # 7,409,200, which appear to be directly relevant to the KCT8528HE product, along with other related KCT products of similar design. Further, be advised that US Patent # 7,409,200 further includes the following corresponding family of related patents: European Patent EP1774590B1 and Chinese Patent CN1998079B. In addition, we are currently conducting further analysis of the components within the KCT8528HE products as these individual components may also likely be covered by Skyworks Patents as well.

Skyworks as a technology company respects the intellectual property rights of others and accordingly treats such intellectual property matters very seriously and we reasonably anticipate that Kangxi does as well. Accordingly, Skyworks fully intends to enforce its Patent rights, and as such, Kangxi may want to carefully consider Skyworks' Patent rights in connection with its KCT8528HE product, along with other KCT products of similar design.

Moreover, after further technical analysis of your currently offered products, it appears that the KCT82XXXX and KCT85XXX series of products may also be likely covered by claims contained in the following nine (9) listed Skyworks Patents below:

US Patent # 9,136,803

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US Patent # 9,667,203
US Patent # 9,917,563
US Patent # 10,566,943
US Patent # 9,628,029
US Patent # 10,158,333
US Patent # 9,503,026
US Patent # 9,825,591
US Patent # 10,236,829

In addition to the above, we will also be conducting an analysis of your upcoming offering of WiFi-7 (IEEE 802.11be) products as well, as we suspect that there may likely be potential infringement issues relating to this technology as well.

Accordingly, Skyworks would like to discuss this serious matter with you at your earliest convenience. Please be advised that Skyworks will undertake ALL appropriate and necessary steps to ensure that its Intellectual Property Rights are protected and preserved with respect to any third party. Skyworks, in conjunction with discussing and addressing this matter, may also be prepared to discuss potentially offering Kangxi a patent license for your usage of our patented technology.

Please contact me at your earliest convenience so that we may begin to discuss this matter. Accordingly, we look forward from hearing from you within fifteen (15) business days acknowledging receipt of this communication, as well as designating a time, no later than April 13, 2023, to preliminarily discuss this matter. I look forward to hearing from you in the immediate future.

We look forward to the resolution of this matter.

Best regards,

Stephen Warhola | Skyworks Solutions, Inc.
Vice President and Chief Intellectual Property Counsel, Legal
5260 California Ave. | Irvine, CA 92617
949-231-4756 (Direct) | stephen.warhola@skyworksinc.com

C: David L. Recker, GM
david.recker@kxcomtech.com
Grand Chip Labs Inc.
14151 Newport Ave
Unit 204
Tustin, CA 92780

Enclosure: US Patent # 7,409,200

US007409200B2

(12) **United States Patent**
Derbyshire et al.

(10) **Patent No.: US 7,409,200 B2**
(45) **Date of Patent: Aug. 5, 2008**

(54) **MODULE INTEGRATION INTEGRATED CIRCUITS**

(75) Inventors: **James H. Derbyshire**, Ottawa (CA); **Alan J. A. Trainor**, Harlow (GB)

(73) Assignee: **SiGe Semiconductor Inc.**, Ottawa, Ontario (CA)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 906 days.

(21) Appl. No.: **10/857,938**

(22) Filed: **Jun. 2, 2004**

(65) **Prior Publication Data**

US 2005/0079851 A1 Apr. 14, 2005

Related U.S. Application Data

(63) Continuation-in-part of application No. 10/680,208, filed on Oct. 8, 2003.

(51) **Int. Cl.**
H04B 1/28 (2006.01)

(52) **U.S. Cl.** **455/333**; 455/339; 455/341; 333/246; 257/723

(58) **Field of Classification Search** 257/723, 257/724, 784; 455/252.1, 323, 333, 334, 455/338, 339, 340, 341; 333/166, 185, 246, 333/260

See application file for complete search history.

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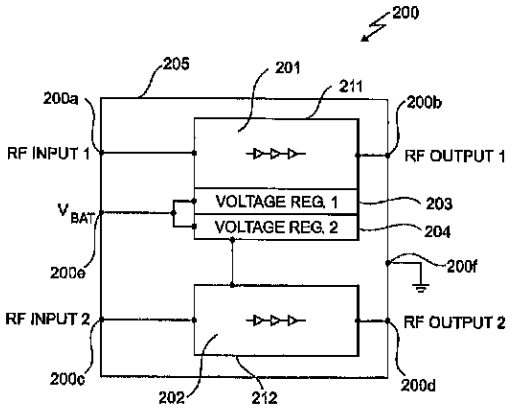
(Continued)

Primary Examiner—Edward Urban
Assistant Examiner—Nhan T. Le
(74) *Attorney, Agent, or Firm*—Townsend and Townsend and Crew LLP

(57) **ABSTRACT**

A first signal conditioning circuit is formed from a first portion, a second portion and a third portion. Signal conditioning functions of each of these portions are facilitated by a predetermined type of integrated semiconductor die within which they are formed. Two different semiconductor dies are thus provided for facilitating integration of the first through third signal conditioning portions therein. Wire bonds are provided between the two different semiconductor dies in order to form circuit paths between the different first through third portions. The signal routing using between the two different semiconductor dies provides for completing of the first signal conditioning circuit having a first signal conditioning function. For example, circuits such as interstage matching circuits are disposed on a different semiconductor die than power amplifier circuits.

34 Claims, 6 Drawing Sheets



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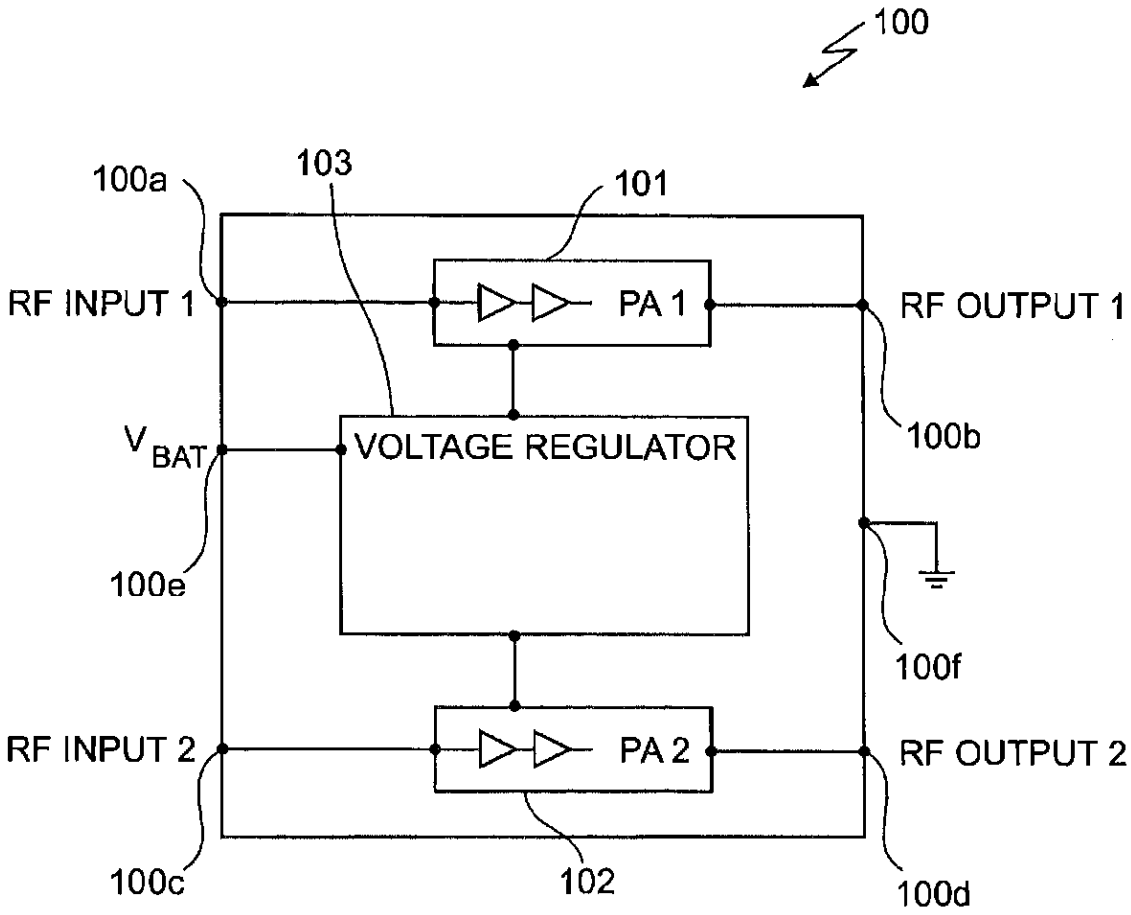


Figure 1
(PRIOR ART)

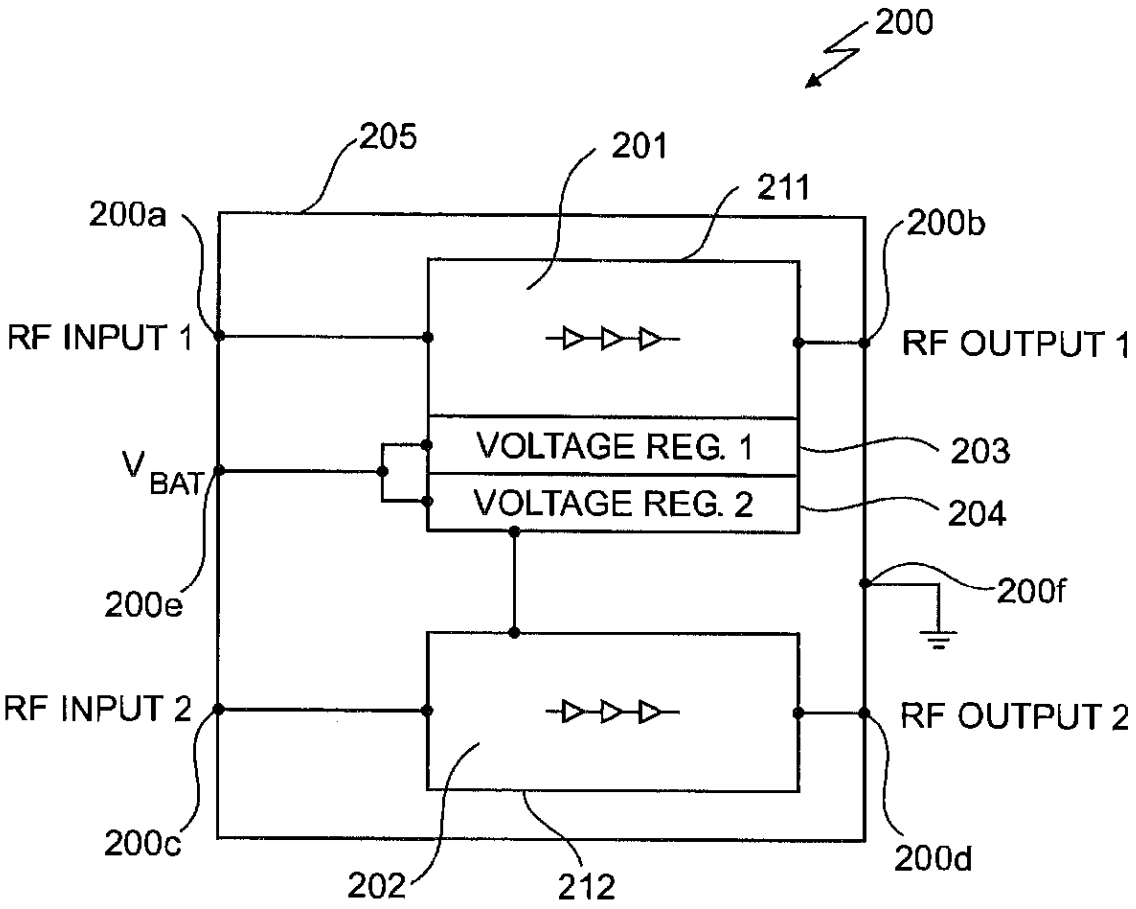

200
205
201
211
200a
200b
RF INPUT 1
RF OUTPUT 1
VOLTAGE REG. 1
203
V_{BAT}
VOLTAGE REG. 2
204
200e
200f
RF INPUT 2
RF OUTPUT 2
200c
200d
202
212

Figure 2

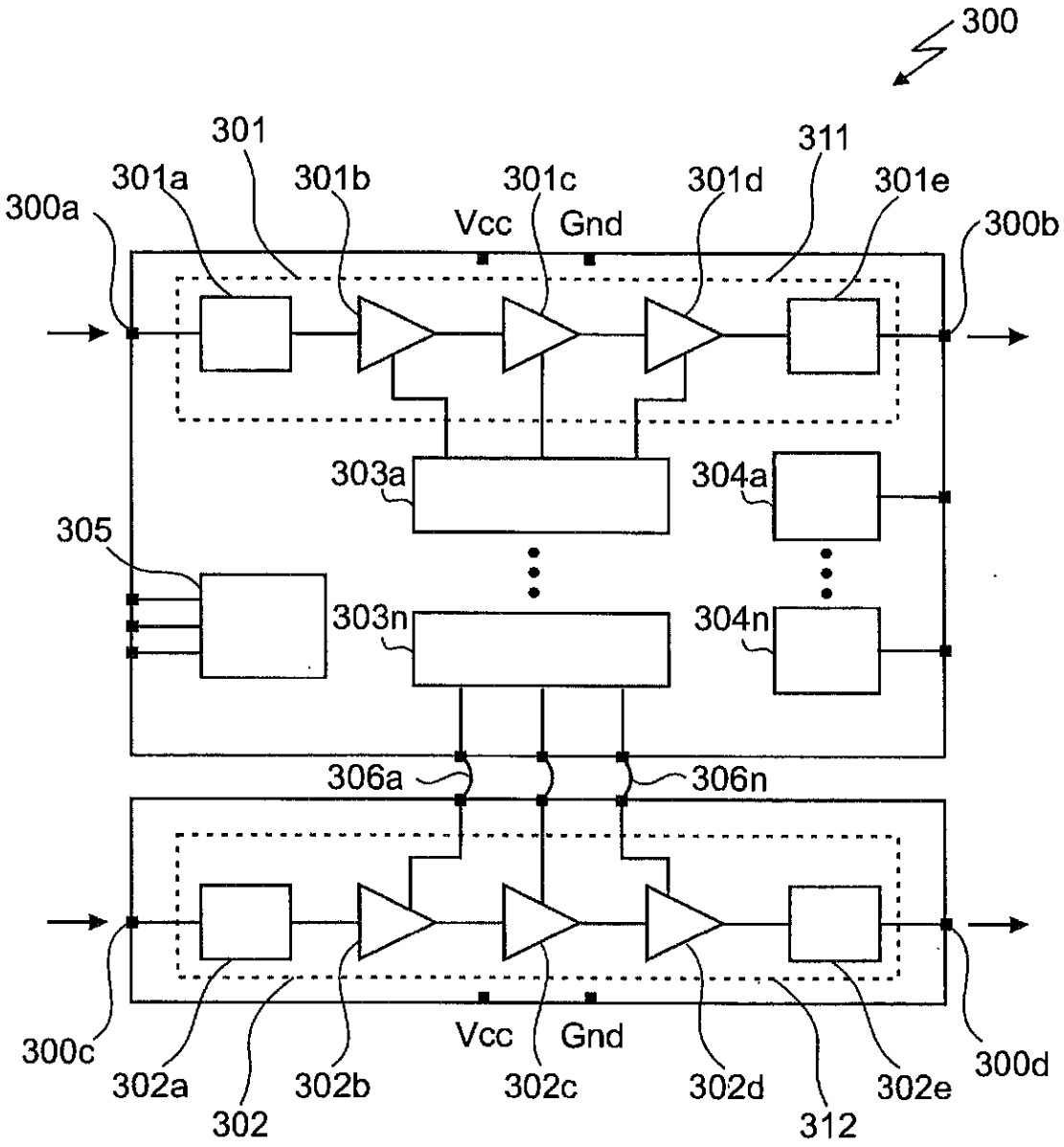

300
301
301a
301b
301c
301d
311
301e
300a
300b
Vcc
Gnd
303a
304a
305
303n
304n
306a
306n
300c
300d
302a
302
302b
302c
302d
312
302e
Vcc
Gnd

Figure 3

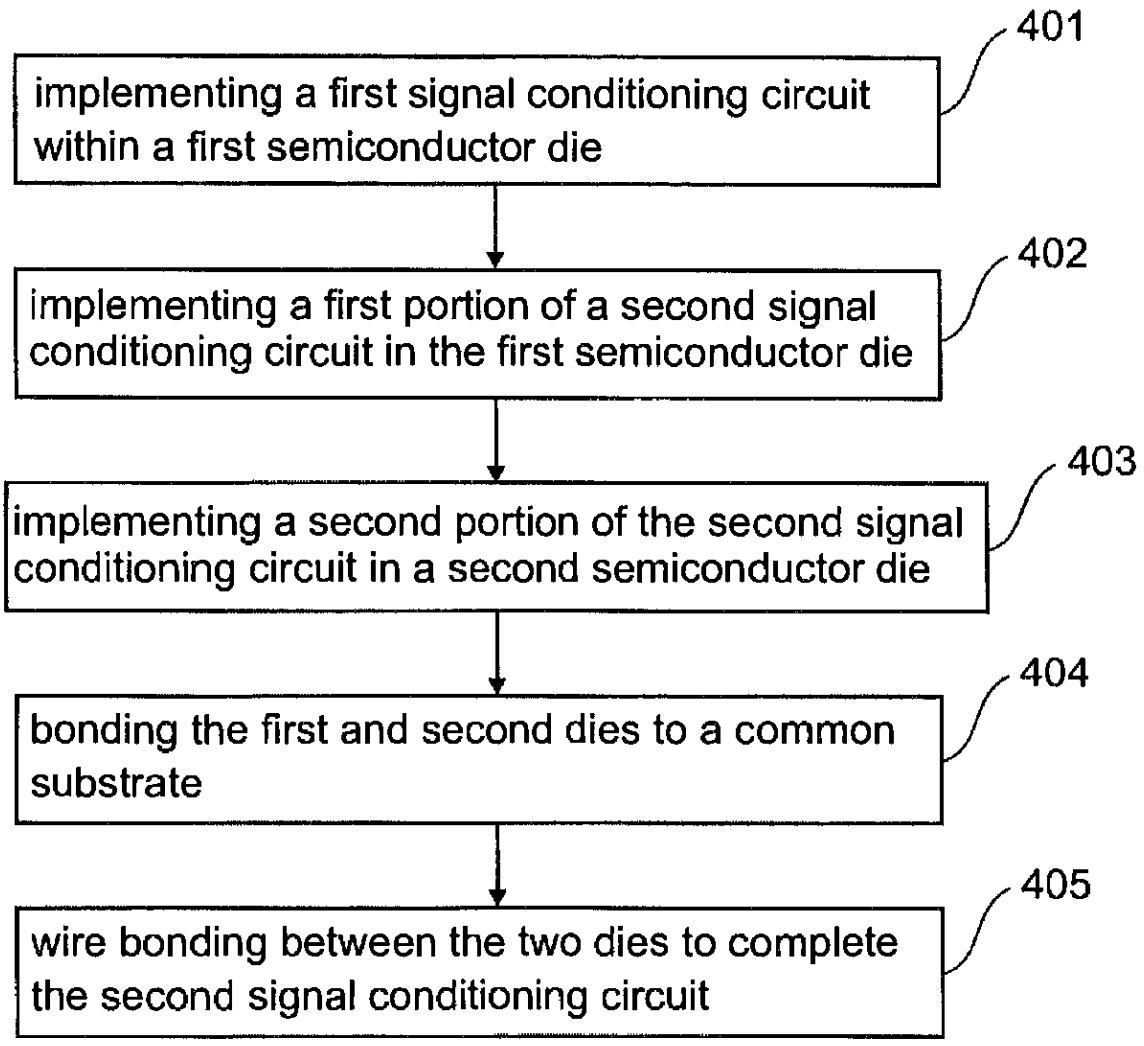

401
implementing a first signal conditioning circuit within a first semiconductor die
402
implementing a first portion of a second signal conditioning circuit in the first semiconductor die
403
implementing a second portion of the second signal conditioning circuit in a second semiconductor die
404
bonding the first and second dies to a common substrate
405
wire bonding between the two dies to complete the second signal conditioning circuit

Figure 4

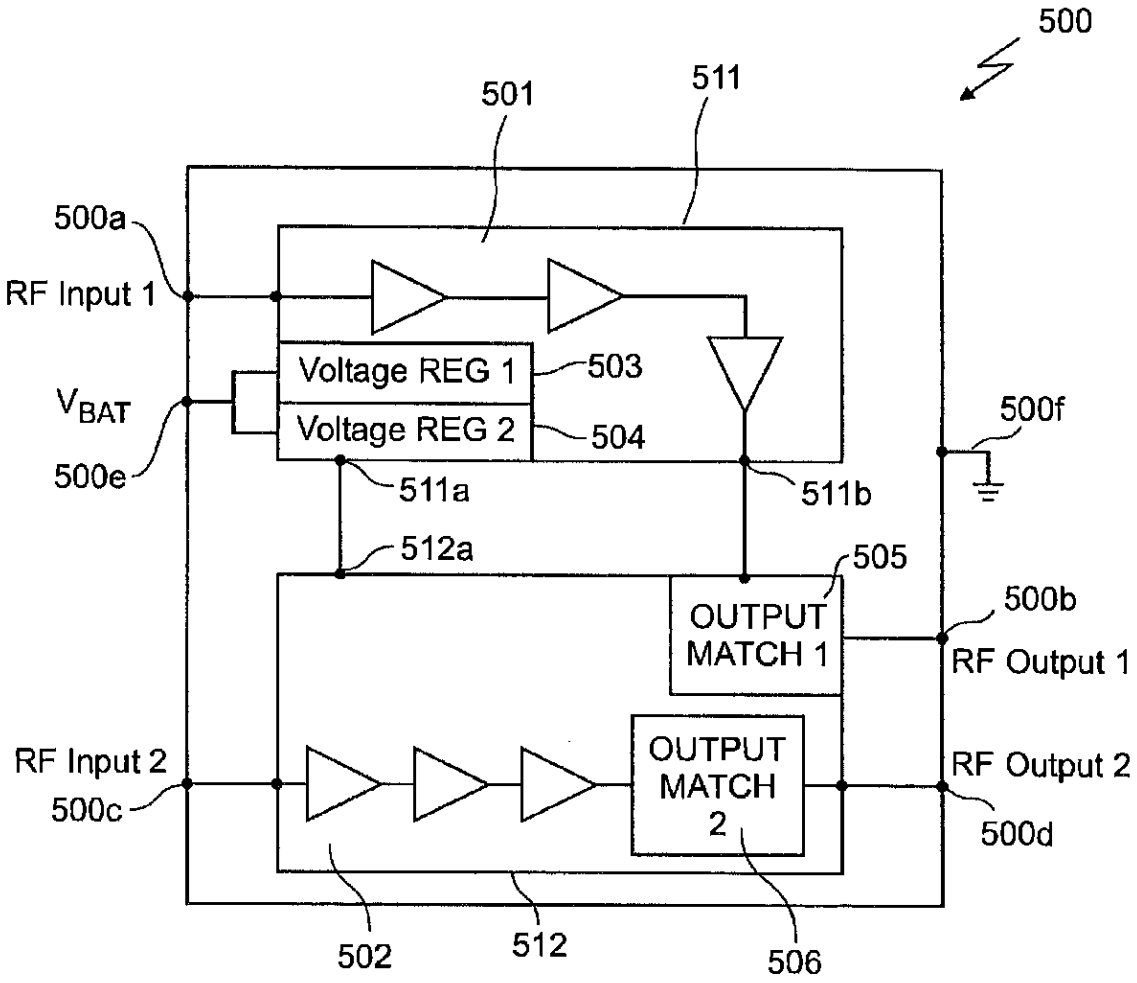

500
501
511
500a
RF Input 1
Voltage REG 1
503
V_{BAT}
Voltage REG 2
504
500e
500f
511a
511b
512a
505
OUTPUT MATCH 1
500b
RF Output 1
RF Input 2
OUTPUT MATCH 2
RF Output 2
500c
500d
502
512
506

Figure 5

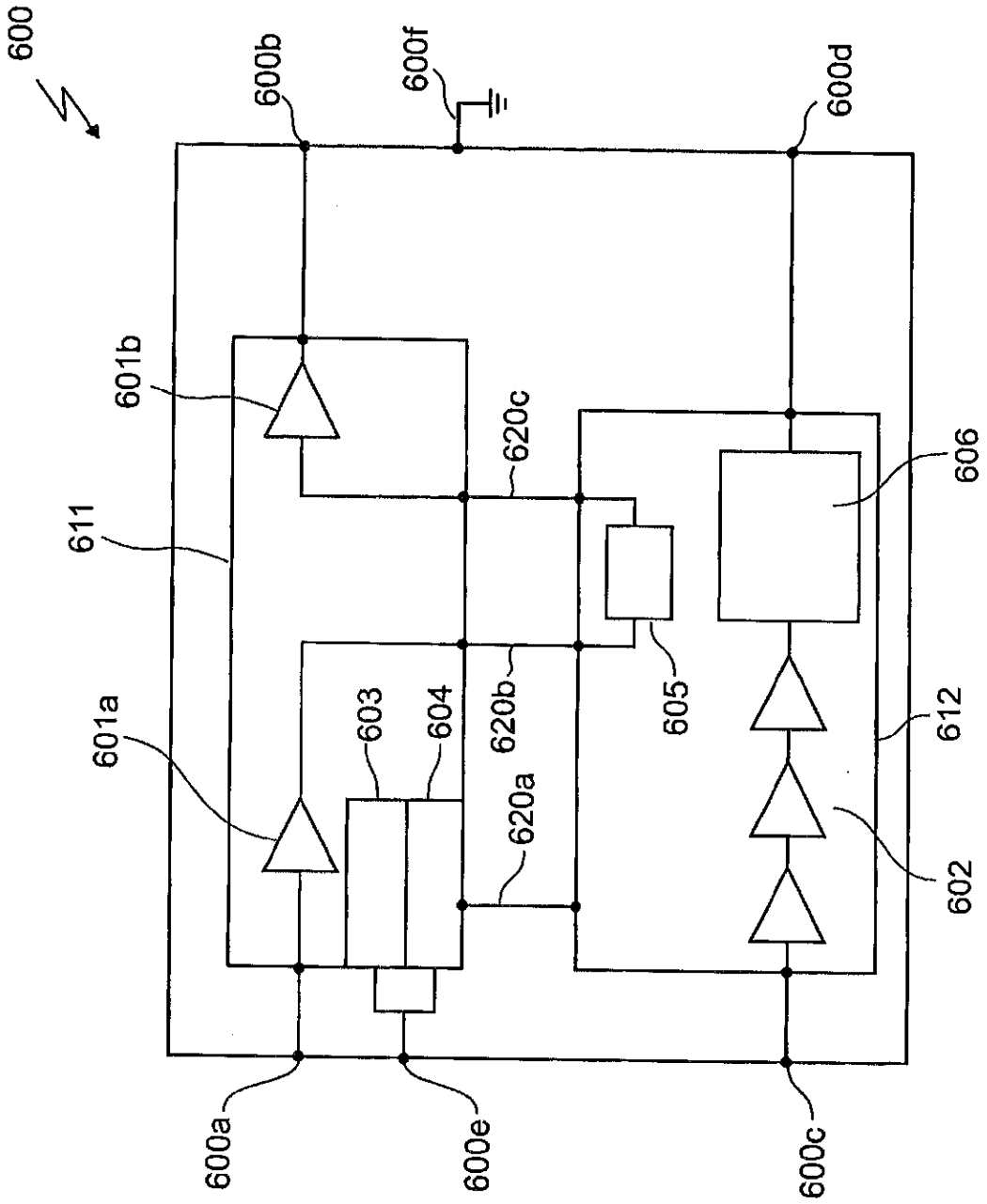

600
600b
600f
600d
601b
620c
606
611
605
603
604
620b
601a
612
620a
602
600a
600e
600c

Figure 6

MODULE INTEGRATION INTEGRATED CIRCUITS

This application is a continuation in part of U.S. patent application Ser. No. 10/680,208, filed on: Oct. 8, 2003.

FIELD OF THE INVENTION

The invention relates to the field of RF front-end circuits and more specifically to the field of multi-standard RF front-end circuits implemented in a small module size.

BACKGROUND OF THE INVENTION

Typically, manufacturers in the area of wireless products wish to implement radio media interface circuits into radio terminals, such as PCMCIA cards or dongles, which typically must operate within the context of two or more radio standards but in accordance with one standard at any one time. These radio standards are for example collectively referred to as the IEEE 802 standard, which is well known to those of skill in the art. This standard is typically divisible into a number of individual radio standards including one standard at 5.8 GHz, known as 802.11a, and another two standards at 2.45 GHz, known as 802.11b and 802.11 g.

In terms of these radio standards, manufacturers are often interested in building radio terminals that will be able to operate at 802.11a, b, and g standards, with only one particular standard being active at any one time. As a result, the manufacturers are interested in acquiring a front-end module that incorporates receive and transmission elements such as the low noise amplifiers (LNA), power amplifiers (PA), impedance matching components, and RF switches for all the standards that the terminal or card must deal with. Thus providing them with flexibility in their radio terminal designs.

Unfortunately, PAs and other components such as the LNA, are highly specialized components that have specifications that generally do not overlap with other radio frequency bands. Thus, a 5.8 GHz PA is generally not suitable for use 2.4 GHz PA. As a result, distinct components such as the LNAs and PAs are incorporated into the module in order to accommodate different radio standards. Moreover, many of the high performance RF components such as PAs and LNAs have a relatively low level of ancillary circuit integration. For example, voltage regulation circuits, temperature regulation circuits, control circuits and other circuits that are used for control and optimization of the operation of the PA are often not integrated into a same die with the PA but rather disposed as discrete components, on separate semiconductor substrates, within the module surrounding the PA die. It is well understood by most module designers that adding more components to the module increases cost, reduces yield and durability while resulting in an increase in module size. This effect is compounded when additional circuitry is used for each active RF component such as an RF switch, LNA, and PA.

Recent advances in SiGe BiCMOS technology have allowed for progressively higher levels of integration of high-performance RF components. For example, a high-performance 2.45 GHz PA for the 802.11b/g standard implemented in SiGe BICMOS technology can incorporate voltage and temperature regulation circuitry along with various power optimization and control schemes manifested in control circuitry. The benefit of such high levels of integration are well understood by the IC design community and include reduced module sizes, reduced cost, reduced assembly time, and increased yield and module longevity. Moreover, for PAs in particular, the robustness of the PA in tolerating of mismatch conditions to the antenna can be improved with voltage standing wave ratio (VSWR) sensing circuitry and PA output power sensing circuitry integrated into the PA chip. In this particular example, a determination of high VSWR might lead to the generation of a control signal to reduce power output and thereby protect one or more PA gain stages from over voltage conditions. Clearly, integration of this type of ancillary circuitry into the PA has the potential to increase PA performance and robustness with a minimum increase in the module size. In respect of LNAs, the integration of bias point control circuitry is important.

However, the usage of SiGe BiCMOS technology in the industry is currently limited. For example, for 5.8 GHz PAs, only a small number of manufacturers are utilizing SiGe for whereas several end users are utilizing GaAs or group III-V based technologies. The GaAs based technologies however offer more gain per stage and lower losses in the RF signal path at 5.8 GHz. GaAs based technology, however, is often unsuitable for the integration of ancillary circuits for use with the GaAs based RF component. Voltage regulation, for example, may not be integrated into the GaAs based PA due to the lack of suitable elementary devices within the GaAs based technology. Therefore, in the context of a module, the module designer is compelled to add those additional circuits, or dies, for supporting of the GaAs based components. As mentioned previously, the addition of more components causes a detriment to the module size and cost.

A need therefore exists to for providing a compact RF module that supports a number of RF standards. It is therefore an object of the invention to provide a compact RF module that overcomes the limitations of the prior art by facilitating integration of multiple circuit components into a same module in order to support a number of RF standards.

SUMMARY OF THE INVENTION

In accordance with the invention there is provided an electronic apparatus comprising: a first integrated circuit semiconductor die comprising; a first portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along a first signal path; a second integrated circuit semiconductor die comprising: a second portion of the first signal conditioning circuit integrated within the second integrated circuit die and disposed along the first signal path for performing a first signal conditioning function along with the first portion of a first signal conditioning circuit for a signal propagating along the first signal path; and, a substrate for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies.

In accordance with the invention there is provided a method of manufacturing a module comprising: providing a first signal conditioning circuit comprising a first portion and a second portion; implementing the first portion of the first signal conditioning circuit within a first semiconductor die; implementing the second portion of the first signal conditioning circuit within a second semiconductor die; bonding the first and second dies to a common substrate; and, forming electrical connections between the two dies to complete the first signal conditioning circuit from the first portion of the first signal conditioning circuit and the second portion of the first signal conditioning circuit.

In accordance with the invention there is provided an electronic apparatus comprising: a first integrated circuit semiconductor die comprising: a first portion of a first signal conditioning circuit integrated within the first integrated cir-

cuit die and disposed along a first signal path; a third portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along the first signal path; a second integrated circuit semiconductor die comprising: a second portion of the first signal conditioning circuit integrated within the second integrated circuit die and disposed along the first signal path for performing a first signal conditioning function along with the first and third portions of the first signal conditioning circuit for a signal propagating along the first signal path; and, a substrate for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies.

BRIEF DESCRIPTION OF THE DRAWINGS

Exemplary embodiments of the invention will now be described in conjunction with the following drawings, in which:

FIG. **1** illustrates a prior art integration of components into a module;

FIG. **2** illustrates a first embodiment of the invention, a module **200** having two semiconductor substrates integrated within the module, as opposed to three, as shown in FIG. **1**;

FIG. **3** illustrates a second embodiment of the invention, which illustrates a more specific implementation of the first embodiment of the invention;

FIG. **4** illustrates the method of manufacturing a circuit in accordance in accordance with an embodiment of the present invention; and,

FIG. **5** illustrates a third embodiment of the invention, a module **500** having two semiconductor substrates integrated within the module.

FIG. **6** illustrates a fourth embodiment of the invention, a module **600** having first and second integrated circuit semiconductor dies, **611** and **612**, integrated within the module **600**.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

FIG. **1** illustrates a prior art integration of components into a module **100**. Disposed within the module **100** is a first signal conditioning circuit **101**, a second signal conditioning circuit **102** and a voltage regulator circuit **103**. The first signal conditioning circuit is disposed between a first RF signal input port **100***a* and a first RF signal output port **10***b*. The second signal conditioning circuit is disposed between a second RF signal input port **100***c* and a second RF signal output port **100***d*. A regulated supply voltage is provided to both the first and second signal conditioning circuits from the regulator circuit **103**, which is disposed on a different semiconductor substrate than the first and second signal conditioning circuits, **101** and **102**. A supply voltage is provided to the regulator circuit **103** from a battery (not shown) through a positive supply voltage input port **100***e* and through a ground port **100***f*. The first and second signal conditioning circuits are also connected to the ground port **100***f*.

The voltage regulator circuit **103** is disposed as the third component of this module **100**. Typically, the voltage regulation properties of the regulator circuit **103** are not optimized for operating with either the first or the second signal conditioning circuits in order to save on module cost **100**. But, a trade-off in the module **100** specifications allows for the use of a single regulator circuit **103** for regulating the supply voltage to both signal conditioning circuits. Providing a separate voltage regulator for each signal conditioning circuit would unfortunately add another semiconductor substrate to the module **100** and result in an increased module cost.

For example, the module **100** shown in FIG. **1** is for use in cellular telephones, where two cellular band power amplifier circuits (PAs) are incorporated into the module as the first and second signal conditioning circuits, **101** and **102**. In such a module, the voltage regulation circuit is typically silicon-based and disposed with power amplifier modules of two different types, such as GaAs based PAs. It is not uncommon to find that the module size is determined by the area required for the ancillary circuits, such as the voltage regulation circuit **103**, rather than by the area required by core RF components, such as the PAs.

Referring to the prior art module illustrated in FIG. **1**, all circuits included into the module are disposed as discrete components. Unfortunately, this leads to progressively larger and more expensive modules as functionality and performance are increased. A further disadvantage of the old technology lies in the additional assembly cost and additional assembly time associated with placing and wiring these numerous circuits and components within the module **100**. It is well understood that in designing and manufacturing of the module, the area requirements grow in proportionality to the number of circuits and components used. Furthermore, the probability of manufacturing errors and defects increases in proportion to the number of circuits and components required in the design.

FIG. **2** illustrates a first embodiment of the invention, a module **200** having two semiconductor substrates integrated within the module, as opposed to three, as shown in FIG. **1**. A first signal conditioning circuit **201** is formed on a first semiconductor substrate **211** and a second signal conditioning circuit **202** is formed on a second semiconductor substrate **212**. The first signal conditioning circuit **201** is disposed between a first RF signal input port **200***a* and a first RF signal output port **200***b*. The second signal conditioning circuit **202** is disposed between a second RF signal input port **200***c* and a second RF signal output port **200***d*.

In addition, a first ancillary circuit **203** and a second ancillary circuit **204** are disposed on the first semiconductor substrate **211**. The first ancillary circuit **203**, in the form of a first voltage regulator circuit, is for providing a first regulated supply voltage to the first signal conditioning circuit **201**. The second ancillary circuit **203**, in the form of a second voltage regulator circuit, is for providing a second regulated supply voltage to the second signal conditioning circuit **202**. An unregulated supply voltage from a source (not shown) is provided to the first and second regulator circuits through a positive supply voltage terminal **200***e* and a ground terminal **200***f*. In this embodiment, the first and second voltage regulator circuits, **203** and **204**, are integrated into the first semiconductor substrate **211**, along with the first signal conditioning circuit **201**. A first interface port **211** a disposed on the first semiconductor die **211** and connected to the second ancillary circuit **204** connects the second ancillary circuit **204** to the second semiconductor die using a second interface port **212***a*. The second interface port **212***a* is connected to the second signal conditioning circuit **202**. For example, the first signal conditioning circuit comprises an amplifying circuit, such as a PA circuit or a low noise amplifier (LNA) circuit.

The integration of circuit components into the module **200** provides for a first integrated circuit formed in a first semiconductor substrate **211** and manufactured using a first semiconductor process. Disposed within the first integrated circuit is the first signal conditioning circuit **201** for performing a first signal conditioning function and the first ancillary circuit **203** electrically coupled to the first signal conditioniug circuit

201 only for use by the first signal conditioning circuit 201 during operation thereof. The second ancillary circuit 204 is for other than being used by the first signal conditioning circuit 201 during operation thereof. The second integrated circuit 202 is electrically coupled to the second ancillary circuit 204 and formed in the second semiconductor substrate 212 and co-packaged with the first integrated circuit 211 within the module 200. The second integrated circuit 202 operates in conjunction with the second ancillary circuit 204, via the connection between the first and second interface ports, 211*a* and 212*a*, for performing the second signal conditioning function. Optionally, the second signal conditioning function is a similar function to the function performed by the first signal conditioning circuit 201.

Advantageously, the integration of circuit functionality into one or more of the semiconductor substrates offers immediate benefit. Integration of these ancillary circuits into the same die area already occupied by one of the other core components is efficient in respect of die area usage. The integration into a module 200, as shown in FIG. 2, allows for integration of different signal conditioning circuits that do not have overlap in their RF bands. The first signal conditioning circuit 201 is for example integrated within the first semiconductor substrate 211 using SiGe BiCMOS technology, along with the first and second voltage regulator circuits, 203 and 204. The second signal conditioning circuit 202 is, for example, integrated into the semiconductor substrate 212 using a GaAs process. As a result of this integration, the completed module 200 accommodates different radio standards in a single package. For example, for a 5.8 GHz PA, the second signal conditioning circuit 202 is used and for a 2.45 GHz PA the first signal conditioning circuit is used 201.

FIG. 3 illustrates a second embodiment of the invention, which illustrates a more specific implementation of the first embodiment of the invention. Referring to FIG. 3, a module 300 having two semiconductor substrates, 311 and 312, integrated therein, is shown. A first signal conditioning circuit 301 is formed on a first semiconductor substrate 311 and a second signal conditioning circuit 302 is formed on a second semiconductor substrate 312. The first signal conditioning circuit 301 is disposed between a first RF signal input port 300*a* and a first RF signal output port 300*b* along a first signal path. The second signal conditioning circuit 302 is disposed between a second RF signal input port 300*c* and a second RF signal output port 300*d* along a second signal path.

A first plurality of ancillary circuitry 303*a* through 303*n*, in the form of a first plurality of control circuitry, is disposed within the first semiconductor substrate 311. At least one of the plurality 303*n* of ancillary circuitry, 303*a* through 303*n*, is unrelated to the operation of the first signal conditioning circuit 301 and used for accommodating the requirements of the second signal conditioning circuit 302 formed on the second semiconductor substrate 312. A plurality of electrical connections, 306*a* through 306*n*, —in the form of wire bonds, for example, is used for electrically coupling the at least one of the plurality 303*n* of ancillary circuitry to the second semiconductor substrate 312 for use by the second signal conditioning circuit 302. The plurality of electrical connections are disposed between a first plurality of interface ports disposed on the first semiconductor die and connected to the a least one of the plurality 303*n* of ancillary circuitry, 303*a* through 303*n*, and a second plurality of interface ports. The second plurality of interface ports are connected to the second signal conditioning circuit 302. The second signal conditioning circuit 302 is for performing a second signal conditioning function in conjunction with the a least one of the plurality 303*n* of ancillary circuitry, 303*a* through 303*n*, connected thereto. The first signal conditioning circuit 301 is for performing a first signal conditioning function independent of the second signal conditioning circuit 302. As a result, RF signals propagating along the first signal path and the second signal path do not interfere with each other because the signal paths are separated on separate semiconductor dies.

Referring to the embodiment shown in FIG. 3, the first signal conditioning circuit comprises a first impedance transforming circuit 301*a*, in series witb three amplification stages, 301*b* through 301*d*, and in series with a second impedance transfonning circuit 301*e*. Disposed within the second signal conditioning circuit are a third impedance transforming circuit 302*a*, in series with three amplification stages, 302*b* through 302*d*, and in series with a second impedance transforming circuit 302*e*. Although the signal conditioning circuits are disposed on different semiconductor substrates, they perform similar functions. In this case, both signal conditioning circuits comprise PAs since they are used in RF amplification applications and as a result provide similar functions.

In addition, a plurality of power detector circuits 304*a* through 304*n* are also preferably integrated within the first semiconductor substrate 311. These power detector circuits are preferably used for detecting of RF output signal power being propagated from the first RF signal output port 300*b* and the second RF signal output port 300*d*. Other circuit blocks, such as circnit block 305, are also integrated within the first semiconductor substrate. Because the first semiconductor substrate is preferably manufactured using a process that supports a plurality of suitable elementary devices, such as SiGe BiCMOS, the integration of the first and second ancillary circuits is facilitated and serves to reduce space in the module without the addition of additional circuit components manufactured on additional semiconductor substrates, which causes a detriment to the module size and cost. Preferably, the semicondnctor process that supports a larger scale of integration is utilized for integrating of a larger plurality of integrated circuit components therein.

Integration of a majority of ancillary circuit functionality into one or more of the semiconductor dies offers inunediate benefit. Integration of these ancillary circuits into the same die area used by one of the core components is very efficient in respect of area usage within the module. The integration into a module, as shown in FIG. 2 and FIG. 3, allows for integration of different signal conditioning circuits into a same module that do not have overlap in their RF bands.

Optionally, a carrier platform, element 205 shown in FIG. 2, is used for supporting the various semiconductor dies, 211 and 212, and optionally other electrical components. The carrier platform 205 is for example a multi-layer laminate or even a silicon-based platform. The function of the carrier platform 205 is to support the semiconductor dies and to provide a means of interconnecting the electrical signals and power supply rails for each semiconductor die, 211 and 212. The embodiments of the invention are applicable for use in modules and other types of sub-assemblies where more than one component is co-located. Co-location referring to the disposition of the module components in close enough proximity such that PCB traces, wirebonds or other technologies are used to interconnect the components to each other. Often the components are in close enough proximity that wirebonding from one semiconductor die to another is sufficient. Thus, these semiconductor dies, 211 and 212, are placed onto the carrier platform 205 and wirebonded or flip-chipped to establish an electrical connection to interconnect traces forming part of the carrier platform 205. Typically, after placement of

semiconductor dies and upon completion of wiring therebetween a mold compound is applied to finish the module.

Advantageously, only one of the semiconductor substrates within the module are designed to incorporate all the additional regulation and optimization circuitry required by the other signal conditioning circuits in the form of active RF components. In this manner, die area within the module is minimized, and thereby cost, and the number of components that require circuit connections therebetween is minimized. Furthermore, selection of active RF components on the basis of RF performance is greatly facilitated without placing additional regulation and additional optimization circuits for the greater performing RF components.

Disposing the first and second signal conditioning circuits on separate substrates advantageously eliminates crosstalk issues therebetween. Thus, output signal noise is minimized. Prior to designing of a module, a module designer of skill in the art determines which signal conditioning circuits will pose problems when integrated on a same semiconductor die and as such those circuits are integrated on separate dies.

FIG. **4** illustrates a method steps for manufacturing a circuit for reducing crosstalk therein. A first signal conditioning circuit is implemented within a first semiconductor die, in step **401**. A first portion of a second signal conditioning circuit is implemented in the first semiconductor die, in step **402**. Referring to step **403**, a second portion of the second signal conditioning circuit is implemented in a second semiconductor die. Thereafter, in step **404**, the first and second dies are bonded to a common substrate, and in step **405**, wire bonding between the two dies is performed to complete the second signal conditioning circuit.

FIG. **5** illustrates a third embodiment of the invention, a module **500** having two semiconductor substrates, **511** and **512**, integrated within the module. A first portion of a first signal conditioning circuit **501** and first and second ancillary circuits, **503** and **504**, are integrated on a first semiconductor substrate **511** and a second portion of the first signal conditioning circuit **505** as well as first and second portions of the second signal conditioning circuit, **502** and **506**, are integrated on a second semiconductor substrate **512**. The first portion of the first signal conditioning circuit **501** is disposed between a first RF signal input port **500***a* and a first semiconductor substrate output port **511***b*, where the second portion of the first signal conditioning circuit **505** is coupled between the first semiconductor substrate output port **511***b* and a first RF signal output port **500***b*. The first portion of the second signal conditioning circuit **502** and the second portion of the second signal conditioning circuit **506** are disposed in series between a second RF signal input port **500***c* and a second RF signal output port **500***d*.

The first ancillary circuit **503**, in the form of a first voltage regulator circuit, is for providing a first regulated supply voltage to the first portion of the first signal conditioning circuit **501**. The second ancillary circuit **504**, in the form of a second voltage regulator circuit, is for providing a second regulated supply voltage to the second portion of the first signal conditioning circuit **505** and to the first and second portions of the second signal conditioning circuit, **502** and **506**. An unregulated supply voltage from a source (not shown) is provided to the first and second regulator circuits through a positive supply voltage terminal **500***e* and a ground terminal **500***f*.

The integration of circuit components into the module **500** provides for a first integrated circuit formed in a first semiconductor substrate **511** and manufactured using a first semiconductor process. Disposed within the first integrated circuit is the first portion of the first signal conditioning circuit **501** for performing a first signal conditioning function in conjunction with the second portion of the first signal conditioning circuit **505** and the first and second ancillary circuits **503** and **504** electrically coupled to the first and second portions of the first signal conditioning circuit, **501** and **505**, respectively. The second ancillary circuit **504** is for other than being used by the first portion of the first signal conditioning circuit **501** during operation thereof. The second integrated circuit **502** includes the first portion of the second signal conditioning circuit **502** and the second portions of the first and second signal conditioning circuits, **505** and **506**, where these portions operate using the electrically coupled second ancillary circuit **504** formed in the first semiconductor substrate **511** and co-packaged with the first integrated circuit **511** within the module **500**.

The second integrated circuit **502** operates in conjunction with the second ancillary circuit **504**, via a connection between the first and second interface ports, **511***a* and **512***a*. Optionally, the second signal conditioning function is a similar function to the function performed by the first signal conditioning circuit **501**.

For example, the first semiconductor substrate **511** is a SiGe semiconductor substrate and the first signal conditioning circuit **501** and **505** is a PA circuit, which is known to have high loss, or low quality factor, when integrated on the silicon wafer. It is well known to those of skill in the art that inductors disposed on the silicon substrate suffer performance degradation due to absorption of RF energy within the substrate and other factors, as compared to inductors that are integrated on a semi-insulating GaAs substrate. Thus, for example, the second semiconductor substrate **512** is a GaAs substrate, where low-loss passive devices are integrated therein for use by the second portion of the first signal conditioning circuit **501**. For example, the second portion of the first signal conditioning circuit **505** is an impedance matching circuit, for use with the first portion of the first signal conditioning circuit **501** in the form of a 2.4 GHz SiGe-based PA. The first portion of the second signal conditioning circuit is for example in the form of a 5 GHz PA.

Advantageously, this integration scheme provides a module designer with the best attributes of both semiconductor substrates, which in this case are silicon and GaAs, in order to achieve a high level of performance, and integration, with a low number of module components. Of course, other components, such as transmission lines, capacitors, and inductors for use by the SiGe-based die, are integrated within the second semiconductor substrate in order to provide increased operating efficiency.

Advantageously, the integration of circuit functionality into one or more of the semiconductor substrates offers immediate benefit. Integration of these ancillary circuits into the same die area already occupied by one of the other core components is efficient in respect of die area usage. The integration into a module **200**, **500**, as shown in FIGS. **2** and **5**, allows for integration of different signal conditioning circuits that do not have overlap in their RF bands. The first signal conditioning circuit **201** and, **501** and **505**, is for example integrated within the first semiconductor substrate **211**, **511** using SiGe BiCMOS technology, along with the first and second voltage regulator circuits, **203** and **204**, and **503** and **504**. The second signal conditioning circuit **202**, **502** and **506**, for example, is integrated into the semiconductor substrate **212**, **512** using a GaAs process. As a result of this integration, the completed module **200**, **500** accommodates

different radio standards in a single package. For example, for a 5.8 GHz PA, the second signal conditioning circuit **202**, **502** and **506** is used for the 5.8 GHz PA and for a 2.45 GHz PA the first signal conditioning circuit **201**, **501** and **505** is used.

FIG. **6** illustrates a fourth embodiment of the invention, a module **600** having first and second integrated circuit semiconductor dies, **611** and **612**, integrated within the module **600**. A first portion of a first signal conditioning circuit **601***a*, a third portion of the first signal conditioning circuit **601***b* and first and second ancillary circuits, **603** and **604**, are integrated within the first integrated circuit semiconductor die **611**. A second portion of the first signal conditioning circuit **605** as well as first and second portions of the second signal conditioning circuit, **602** and **606**, are integrated on the second integrated circuit semiconductor die **612**.

The first portion of the first signal conditioning circuit **601***a* is disposed between a first RF signal input port **600***a* and an electrical connection **620***b* that connects an output port of the first portion of the first signal conditioning circuit **601***a* to a second portion of the first signal conditioning circuit **605** disposed in the second integrated circuit semiconductor die **612**. An input port of the third portion of the first signal conditioning circuit **601***b* is coupled to an output port of the second portion of the first signal conditioning circuit **605** using an electrical connection **602***c*, where an output port of the third portion of the first signal conditioning circuit **601***b* forms an RF signal output port **600***b*. Thus, a first signal path is formed from the first RF signal input port **600***a* through to the first RF signal output port **600***b*.

A first portion of a second signal conditioning circuit **602** and the second portion of the second signal conditioning circuit **606** are disposed in series between a second RF signal input port **600***c* and a second RF signal output port **600***d*. A first ancillary circuit **603**, in the form of a first voltage regulator circuit, is for providing a first regulated supply voltage to the first portion and third portions of the first signal conditioning circuit, **601***a* and **601***b*. The second ancillary circuit **604**, in the form of a second voltage regulator circuit, is for providing a second regulated supply voltage to the second portion of the first signal conditioning circuit **605** and to the first and second portions of the second signal conditioning circuit, **602** and **606**, through an electrical connection **620***a*. An unregulated supply voltage from a source (not shown) is provided to the first and second regulator circuits through a positive supply voltage terminal **600***e* and a ground terminal **600***f*.

The function of the first signal conditioning circuit, **601***a*, **605** and **601***b*, is to provide a first signal conditioning function utilizing the portions thereof disposed in the first and second integrated circuit semiconductor dies, **611** and **612**. Preferably, the second portion of the first signal conditioning circuit **605** is an interstage matching circuit for performing an impedance match between the first and third portions, **601***a* and **601***b*, which are preferably in the form of power amplifier circuits. Thus, for example, if the first integrated circuit semiconductor die **611** includes silicon and the second integrated circuit semiconductor die **612** includes GaAs, then a signal propagating from the first portion **601***a* leaves the first semiconductor substrate **611**, using electrical connection **620***b*, for interstage matching using the second portion **605**. Thereafter, once the signal has been interstage matched, the signal leaves the second integrated circuit semiconductor die **612** and is propagated along using electrical connection **620***c* to the first integrated circuit semiconductor die **611**, where it is received by an input port of the third portion **601***b*.

Optionally, the second portion of the first signal conditioning circuit **605** is coupled to the RF input port **600***a* for receiving of the RF input signal directly and serves to provide an impedance match between the input port and the third portion of the first signal conditioning circuit **601***b*.

Advantageously, the integration of the second portion of the first signal conditioning circuit **605** within the second integrated circuit semiconductor die **612** allows for signal conditioning operations that are more easily, or more cost effectively, facilitated by devices manufactured within the second integrated circuit semiconductor die **612** to be performed by circuitry integrated within the second integrated circuit semiconductor die for a signal propagating along the first signal path. Furthermore, those devices that allow for signal conditioniug operations that are more easily, or more cost effectively, facilitated by devices manufactured withiu the first integrated circuit semiconductor die **611** to be performed by circuitry disposed within the first integrated circuit semiconductor die **611** for the signal propagating along the first signal path.

When the module design is performed, the signal conditioning circuit and ancillary circuits are integrated on the semiconductor dies in such a manner that the area of the die is minimized and other issues, such as noise and cornstalk, are also reduced. In the prior art, different signal conditioning and ancillary circuits are often disposed within the modules without foresight given to a reduction in module area and minimization of individual semicouductor die usage. Typically many different semiconductors dies are disposed within the module on the substrate, which unfortunately increases the manufacturing costs and does not result in a compact module size. Additionally, using some semiconductor manufacturing technologies is more costly for implementing of certain ancillary circuitry. For example, GaN and InP technologies have much larger costs associated with die are usage than silicon-based technologies. As a result, implementing an ancillary circuit in InP or GaN becomes significantly more expensive than implementing the functionally similar ancillary circuit in a silicon based technology.

Though the embodiments of the invention refer to two or more signal conditioning circuits such as power amplifiers, it well understood and appreciated in the art that the efficient provision of ancillary circuits necessary or beneficial to the operation of other types of circuits is enabled using this invention. For example, other signal conditioning circuits, such as memory buffers are envisioned for use exclusively by a separate PLL-type circuit and die. In the context of a module, this invention is very useful because it obviates the placement of some additional dies within. It does, however, require that the IC designer and module designer work with an overall view of the modnle objectives and the requirements of the various functional circuits in the module. With this invention and the realization that some ancillary circuits will be integrated into the same semiconductor die area as the signal conditioning circuits unrelated to those ancillary circuits, the partitioning of signal conditioning circuits and the ancillary circuits becomes an optimization task.

Though the above embodiments refer to a SiGe BiCMOS manufacturing technology, other suitable manufacturing technologies for integration of the ancillary circuitry is also supported according to the invention.

The embodiments of the invention further advantageously allow for integration of silicon-based technologies with other technologies such as GaAs, InP, and GaN that do not support a similar level of component integration.

Numerous other embodiments may be envisaged without departing from the spirit or scope of the invention.

What is claimed is:

1. An electronic apparatus comprising:

a first integrated circuit semiconductor die comprising:

a first portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along a first signal path; and

a second integrated circuit semiconductor die comprising;

a second portion of the first signal conditioning circuit integrated within the second integrated circuit die and disposed along the first signal path for performing a first signal conditioning function along with the first portion of a first signal conditioning circuit for a signal propagating along the first signal path; and,

a substrate for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies.

2. An electronic apparatus according to claim 1, comprising a second signal conditioning circuit comprising a first portion of the second signal conditioning circuit and a second portion of the second signal conditioning circuit integrated within the second integrated circuit die for performing a second signal conditioning function on a signal propagating along a second signal path that is different than the first signal path.

3. An electronic apparatus according to claim 2, wherein the first signal conditioning function and the second signal conditioning function provide similar signal conditioning functions.

4. An electronic apparatus according to claim 1, wherein the first integrated circuit die is manufactured using a first semiconductor process and utilizes a silicon based technology.

5. An electronic apparatus according to claim 4, wherein the second integrated circuit die is manufactured using a second semiconductor process and utilizes other than a silicon based technology.

6. An electronic apparatus according to claim 1, wherein the first portion of the first signal conditioning circuit comprises at least a power amplifier circuit and where the function of the first portion of the first signal conditioning circuit is for amplifying of an input signal using the at least a power amplifier circuit.

7. An electronic apparatus according to claim 6, wherein the second portion of the first signal conditioning circuit comprises an impedance matching circuit.

8. An electronic apparatus according to claim 2, wherein the second signal conditioning circuit comprises at least a power amplifier circuit and where the function of the first portion of the second signal conditioning circuit is for amplifying of an input signal using the at least a power amplifier circuit.

9. An electronic apparatus according to claim 8, wherein the second portion of the second signal conditioning circuit comprises an impedance matching circuit and where the function of the first portion of the second signal conditioning circuit is for amplifying of an input signal using the at least a power amplifier circuit.

10. An electronic apparatus according to claim 2, wherein the first semiconductor process does not facilitate manufacturing and integration of at least one of the second portion of the first signal conditioning circuit and the second portion of the second signal conditioning circuit.

11. An electronic apparatus according to claim 1, wherein the second integrated circuit die is manufactured using a second semiconductor process that is different from that used to manufacture the first integrated circuit die.

12. An electronic apparatus according to claim 1, wherein the first integrated circuit die is derived from a first semiconductor wafer comprised of one of Si, SiGe, GaAs, InP, and GaN.

13. An electronic apparatus according to claim 12, wherein the second integrated circuit die is derived from a second semiconductor wafer that is comprised of other one of Si, SiGe, GaAs, InP, and GaN.

14. An electronic apparatus according to claim 1, wherein the first integrated circuit die is manufactured using a BiCMOS process.

15. An electronic apparatus according to claim 1, wherein the second portion of the first signal conditioning circuit comprises at least one of a capacitor and an inductors and a signal transmission line.

16. An electronic apparatus according to claim 2, comprising: a first ancillary circuit integrated within the first integrated circuit die and electrically coupled to the first portion of the first signal conditioning circuit for use during operation thereof.

17. An electronic apparatus according to claim 16, comprising a second ancillary circuit integrated within the first integrated circuit semiconductor die and electrically coupled to the second portion of the first signal conditioning circuit and to the first and second portions of the second signal conditioning circuit for other than performing the first or the second signal conditioning function and for use by the second portion of the first signal conditioning circuit and the first and second portions of the second signal conditioning circuit during operation thereof.

18. A method of manufacturing a module comprising:

providing a first signal conditioning circuit comprising a first portion and a second portion;

providing a second signal conditioning circuit comprising a first portion and a second portion;

implementing the first portion of the first signal conditioning circuit within a first semiconductor die;

implementing the second portion of the first signal conditioning circuit within a second semiconductor die;

implementing the first and second portions of the second signal conditioning circuit in the second semiconductor die;

bonding the first and second dies to a common substrate; and,

forming electrical connections between the two dies to complete the first signal conditioning circuit from the first portion of the first signal conditioning circuit and the second portion of the first signal conditioning circuit.

19. A method according to claim 18, wherein the first semiconductor die comprises a first portion of a first signal path and the second semiconductor die comprises a second portion of the first signal path, the first signal path disposed between a first input port and a first output port.

20. A method according to claim 19, wherein the second semiconductor die comprises a second signal path that is other than the second portion of the first signal path and in approximate RF isolation therefrom.

21. A method according to claim 18, wherein the second semiconductor die is manufactured using a more expensive semiconductor process than that used for manufacturing of the first semiconductor die.

22. A method according to claim 18, wherein the first portion of the first signal conditioning circuit is more cost effectively implemented in the first semiconductor die.

23. A method according to claim 18, wherein the first semiconductor die does not facilitate implementation of the second portion of the first signal conditioning circuit therein.

24. A method according to claim 18, wherein implementing of the second portion of the first signal conditioning circuit within the second semiconductor die provides increased performance in signal conditioning as compared to implementing of the second portion of the first signal conditioning circuit within the first semiconductor die.

25. A method according to claim 18, wherein prior to implementing the first signal conditioning circuit comprises partitioning of the first signal conditioning circuit into the first portion aud the second portion.

26. An electronic apparatus comprising:

a first integrated circuit semiconductor die comprising:

a first portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along a first signal path;

a third portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along the first signal path; and

a second integrated circuit semiconductor die comprising;

a second portion of the first signal conditioning circuit integrated withiu the second integrated circuit die and disposed along the first signal path for performing a first signal conditioning function along with the first and third portions of the first signal conditioning circuit for a signal propagating along the first signal path; and,

a snbstrate for supporting the first aud second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies.

27. An electronic apparatus according to claim 26, comprising:

a first RF signal input port coupled with an input port of the first portion of the first signal conditioning circuit for receiving of a first RF input signal; and

a first RF signal outpnt port coupled with an output port of the third portion of the first signal conditioning circuit for providing of a first RF output signal,

wherein the first signal path is disposed between the first RF signal input port and the first RF signal output port,

wherein the coupling circuit comprises;

a first electrical connection disposed between an output port the first portion of the first signal conditioning circnit and an input port of the second signal conditioning portion of the first signal conditioning circuit; and,

a second electrical connection disposed between an output port the second portion of the first signal conditioning circuit and an input port of the third signal conditioning portion of the first signal conditioning circuit.

28. An electronic apparatus according to claim 26, comprising:

a first RF signal input port coupled with an input port of the second portion of the first signal conditioning circuit for receiving of a first RF input signal; and

a first RF signal output port coupled with an output port of the third portion of the first signal conditioning circuit for providing of a first RF output signal,

wherein the first signal path is disposed between the first RF signal input port and the first RF signal output port,

wherein the coupling circuit comprises;

a second electrical connection disposed between an output port the second portion of the first signal conditioning circuit and an input port of the third signal conditioning portion of the first signal conditioning circuit.

29. An electronic apparatus according to claim 26, comprising a second signal conditioning circuit comprising a first portion of the second signal conditioning circuit and a second portion of the second signal conditioning circuit integrated within the second integrated circuit die for performing a second signal conditioning function on a signal propagating along a second signal path that is different than the first signal path.

30. An electronic apparatus according to claim 26, wherein the first integrated circuit die is derived from a first semiconductor wafer comprised of one of Si, SiGe, GaAs, InP, and GaN.

31. An electronic apparatus according to claim 30, wherein the second integrated circuit die is derived from a second semiconductor wafer that is comprised of the other one of Si, SiGe, GaAs, InP, and GaN.

32. An electronic apparatus according to claim 26, wherein the second portion of the first signal conditioning circuit comprises an interstage matching circuit.

33. An electronic apparatus according to claim 26, comprising a first ancillary circuit integrated within the first integrated circuit die and electrically coupled to the first portion and the third portion of the first signal conditioning circuit for use during operation thereof.

34. An electronic apparatus according to claim 33, comprising a second ancillary circuit integrated within the first integrated circuit semiconductor die and electrically coupled to the second portion of the first signal conditioning circuit for use during operation thereof.

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EXHIBIT 15

SKYWORKS®

April 23, 2024

Kangxi Communications Technologies (Shanghai) Co., Ltd.
5th Floor, Building 10
No. 399 Keyuan Road
Pudong New Area, Shanghai
ATTN: Ping Peng, Chairman

RE: Notice of Infringement of Skyworks Solutions, Inc.'s Patents

Dear Dr. Peng:

I write to follow up on my letter of March 7, 2023 and our meeting on May 9, 2023, in which Skyworks Solutions, Inc. ("Skyworks") informed Kangxi Communication Technologies Co. Ltd.'s and Grand Chips Technology Corporation's (collectively, "KCT") that at least your KCT82XXXX and KCT85XXXX series products infringed Skyworks's patents.

Despite providing KCT with notice of infringement as outlined above, KCT continues to sell at least the following infringing products:

1. At least the KCT8547HE, KCT8539S, KCT8239S, and KCT8576HE products infringe at least claims 1, 2, 10-11, 17, 18, 20, 21, and 22 of U.S. Patent No. 8,717,101.

2. At least the KCT8547HE, KCT8539S, KCT8239S, and KCT8576HE products infringe at least claims 14, 15, 17, and 20 of U.S. Patent No. 9,917,563.

3. At least the KCT8547HE, KCT8539S, KCT8239S, and KCT8576HE products infringe at least claims 1 and 7 of U.S. Patent No. 9,450,579.

4. At least the KCT8547HE, KCT8539S, KCT8239S, and KCT8576HE products infringe at least claim 4 of U.S. Patent No. 9,148,194.

5. At least the KCT8547HE, KCT8539S, KCT8239S, and KCT8576HE products infringe at least claims 1, 2, 6, 10-12, 15, 18, 19, 20, and 23-25 of U.S. Patent No. 7,409,200.

All KCT products containing the same infringing features as the above-referenced products also infringe the same Skyworks patents, including KCT's recent Wi-Fi 7 (IEEE 802.11be) products. Each of the patents identified above are attached to this letter for your convenience.

Skyworks respects the intellectual property rights of others and accordingly takes such intellectual property matters very seriously. Unless KCT immediately agrees to cease selling the products

described above, and any similarly infringing products, Skyworks will be left with no choice but to defend its intellectual property rights and seek all appropriate relief.

I look forward to your prompt response.

Best regards,

Stephen Warhola | Skyworks Solutions, Inc.
Vice President and Chief Intellectual Property Counsel, Legal
5260 California Ave. | Irvine, CA 92617

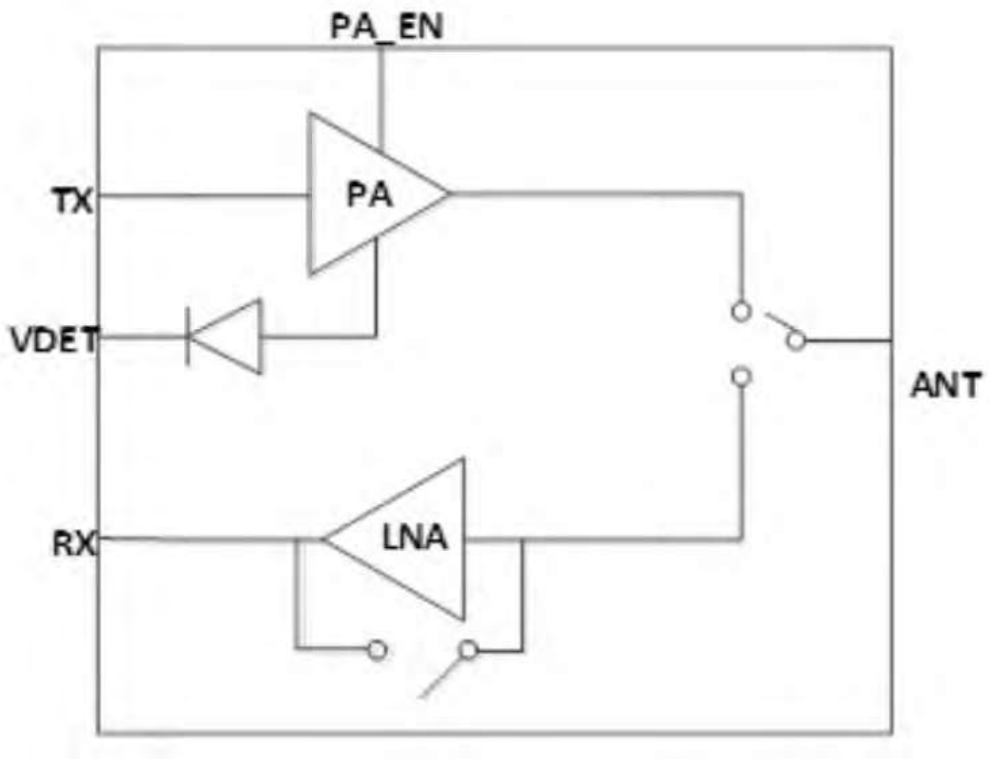
EXHIBIT 16

EXHIBIT 16
SKYWORKS SOLUTIONS, INC.'S INFRINGEMENT CHART
KCT8539S
U.S. Patent No. 9,917,563
Independent Claim 14

Skyworks Solutions, Inc. ("Skyworks") provides this exemplary claim chart for independent claim 14 of U.S. Patent No. 9,917,563 (the "'563 patent") applied to Kangxi Communication Technologies (Shanghai) Co., Ltd's and Grand Chip Labs, Inc.'s (collectively, "KCT") KCT8539S product. The disclosures in this claim chart directed to the KCT8539S are also more broadly directed to any sale, offer for sale, use, or importation of the KCT8539S in the U.S., including in an end product such as a wireless router or as a standalone product that is not incorporated in an end product.

The claim chart below demonstrates infringement by comparing each element of the charted claim to corresponding components, aspects, and/or features of the KCT8539S product. This claim chart is not intended to constitute an expert report on infringement. This claim chart includes information provided by way of example, and not by way of limitation.

The analysis set forth below is based only upon information from publicly available sources regarding the KCT8539S product. Further analysis of non-public information during fact discovery will likely assist in identifying all infringing features and functionalities used by KCT in the KCT8539S product. Accordingly, Skyworks reserves the right to supplement this infringement analysis once such information is made available to Skyworks. Further, Skyworks reserves the right to supplement this infringement analysis, as appropriate, upon issuance of an order construing any terms recited in the asserted claims or as other circumstances so merit.

Claim	KCT8539S
14 [pre] A packaged module comprising:	To the extent the preamble of claim 1 is limiting, the KCT8539S includes a packaged module. The KCT8539S is a module for Wi-Fi connectivity. For example, the following image for the KCT8539S is a simplified block diagram for this product.[1]  *See, e.g.*, simplified block diagram for KCT8539S The KCT8539S is, according to KCT, "a highly integrated RF front-end integrated circuit incorporat[ing] key RF functionality needed for IEEE 802.11a/n/ac/ax WLAN systems operating in the 5.15-5.85GHz

[1] *See* https://perma.cc/DA7F-4CED.

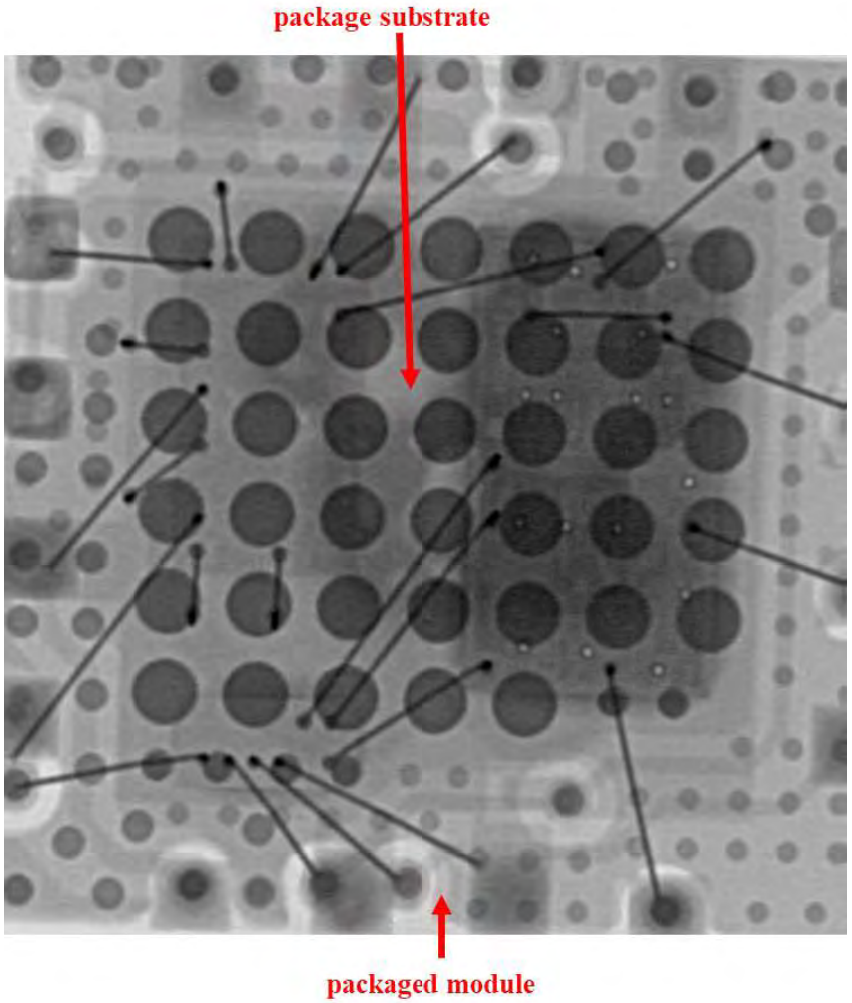
range. KCT8539S integrates a high-efficiency high-linearity power amplifier (PA), a low noise amplifier (LNA) with bypass ….”[2]

As another example, the image below of the KCT8539S shows a packaged module (as indicated by the corresponding label below) for the KCT8539S.

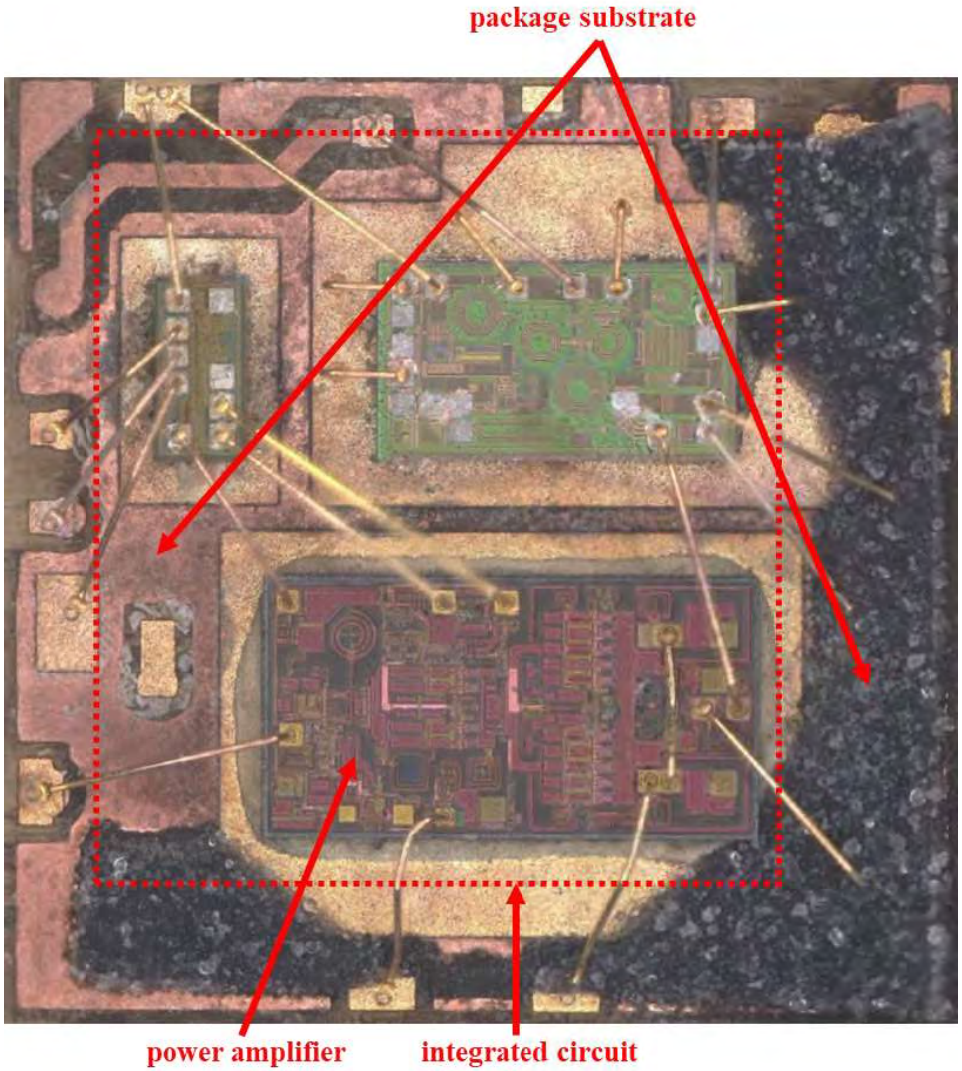


See, e.g., photo of KCT8539S

[2] *See* https://perma.cc/DA7F-4CED.

14[A] a package substrate; and	The KCT8539S includes a package substrate. For example, the image of the KCT8539S below shows a package substrate (as indicated by the corresponding label below) as part of the packaged module.  *See, e.g.*, photo of KCT8539S

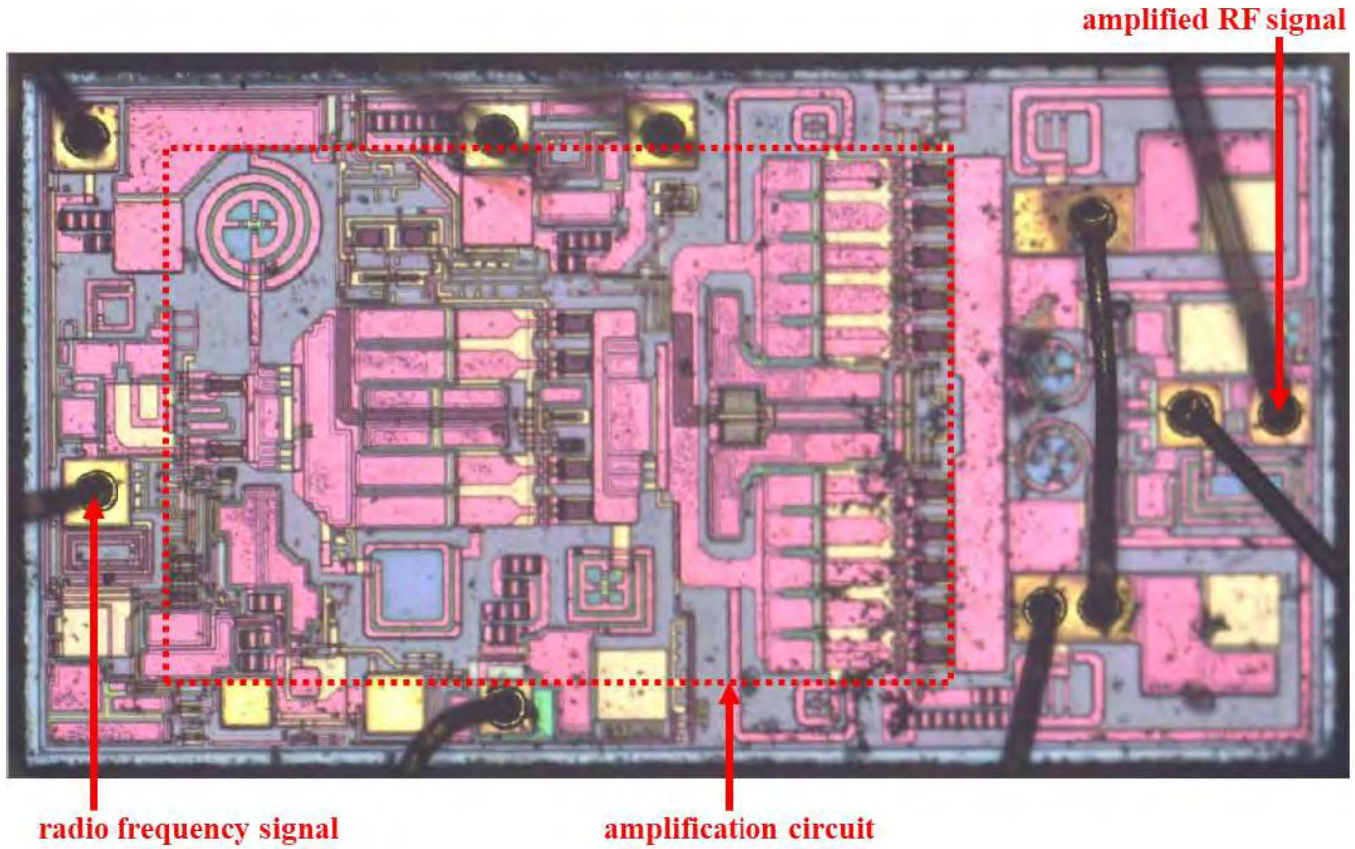
14[B] an integrated circuit attached to the package substrate and including a power amplifier configured to provide amplification to a radio frequency signal	The KCT8539S includes an integrated circuit attached to the package substrate and including a power amplifier. For example, the image of the KCT8539S below shows an integrated circuit (as indicated by the corresponding label below) attached to the package substrate and including a power amplifier (as indicated by the corresponding label below).



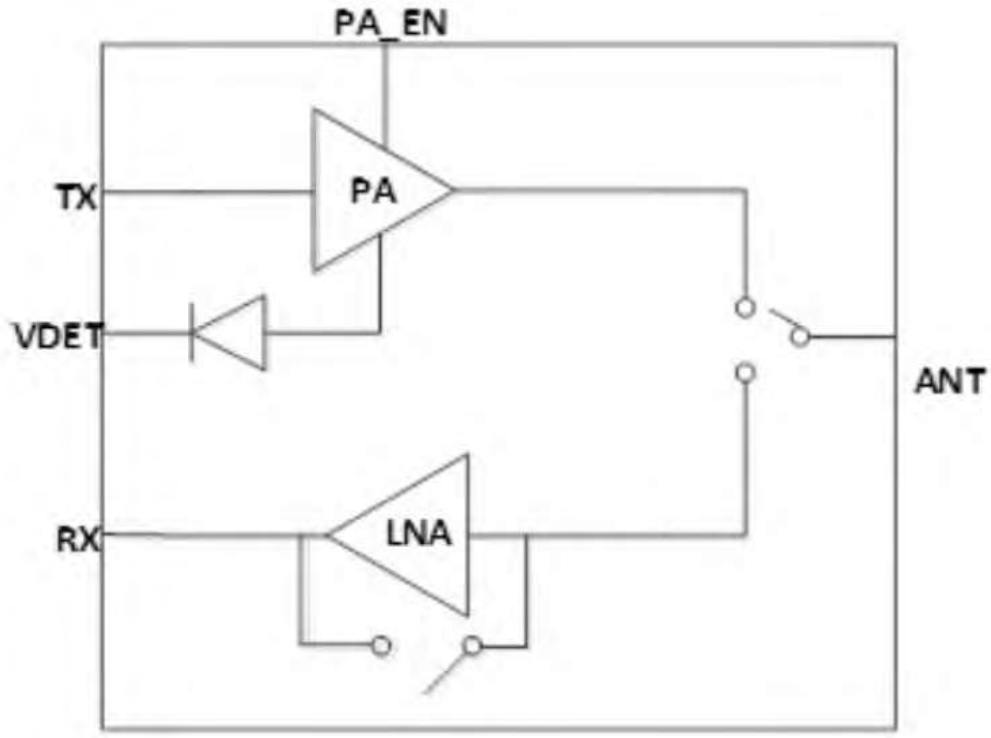
See, e.g., photo of KCT8539S showing an integrated circuit having three dies including a die for the power amplifier

The power amplifier in the KCT8539S is configured to provide amplification to a radio frequency signal.

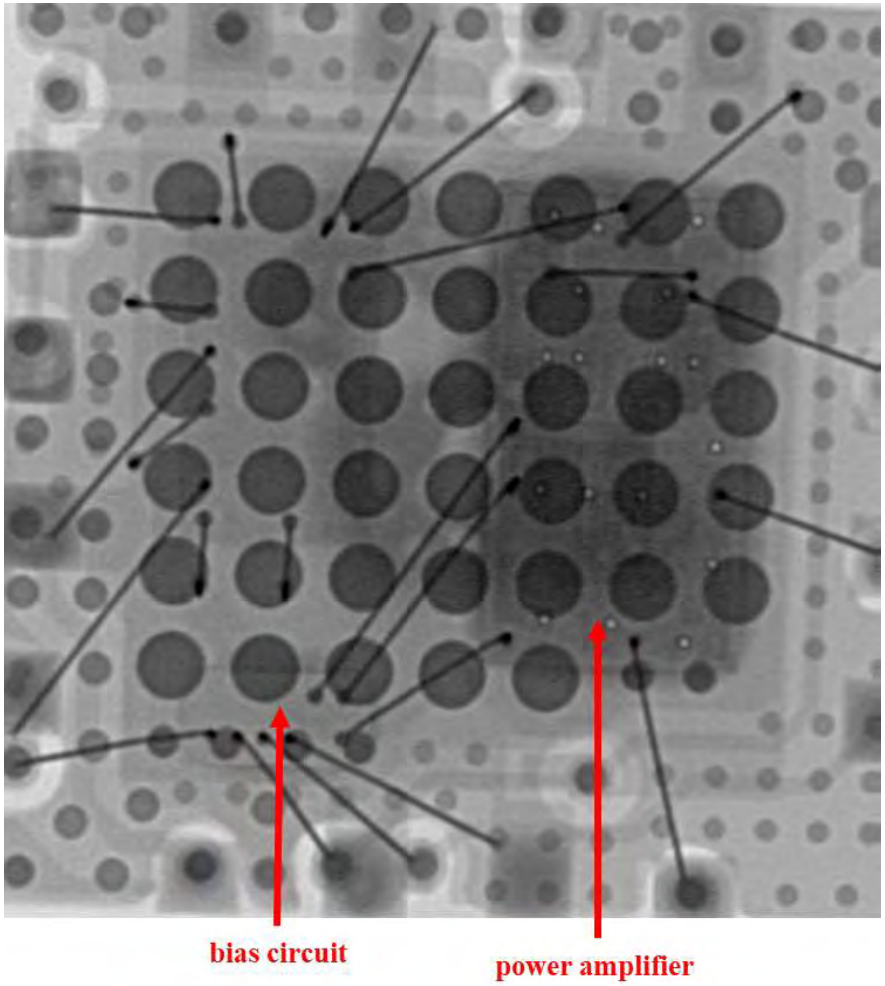
For example, the image below shows an enlarged view of the power amplifier die of the KCT8539S. The power amplifier is coupled in such a way that it is configured to receive as an input a radio frequency (RF) signal, as labeled below as the radio frequency signal, and amplify the radio frequency signal to output an amplified RF signal, as labeled below. The dashed box with the corresponding label below is one example of an amplification circuit that provides the amplification of the radio frequency signal.

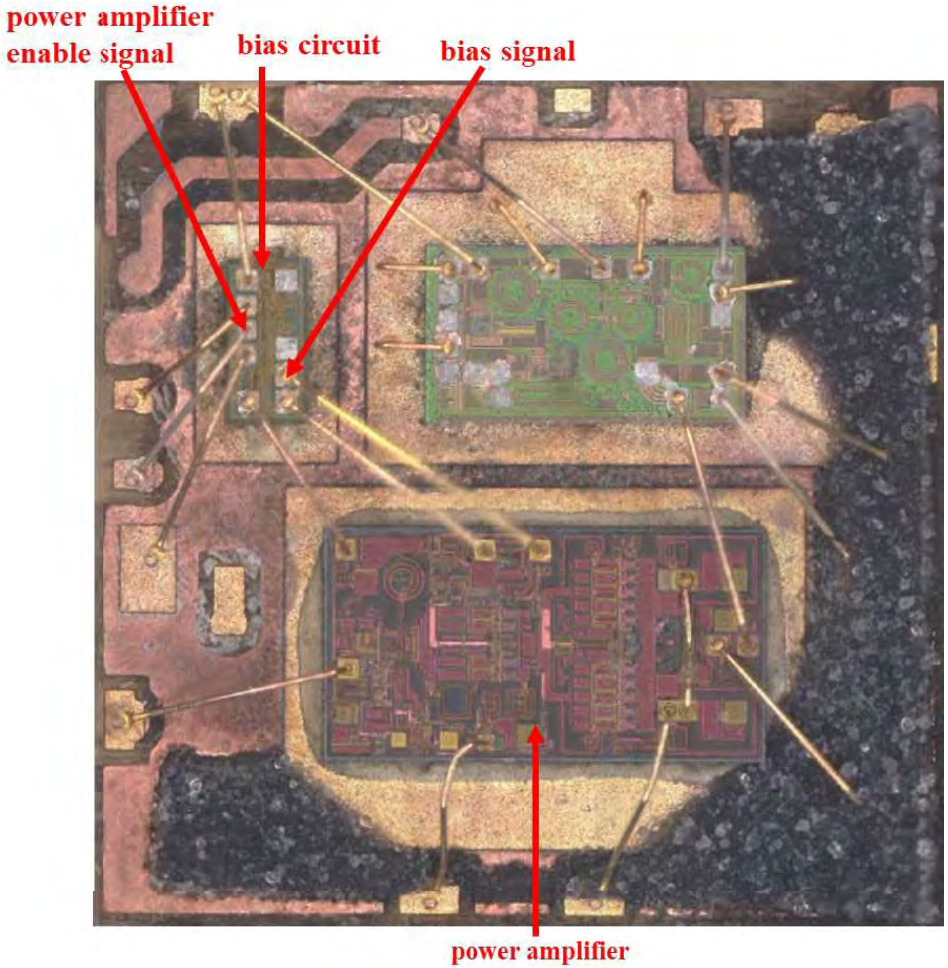


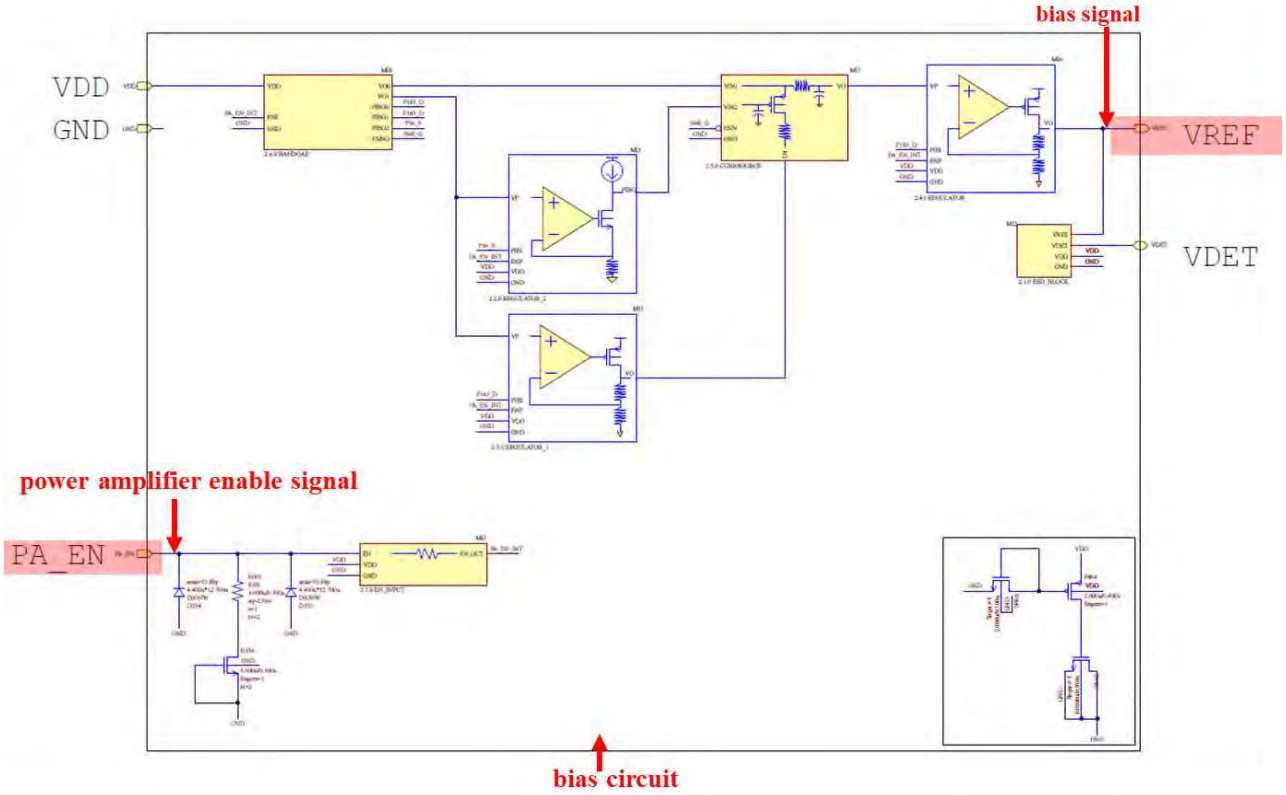
See, e.g., photo of the power amplifier die of KCT8539S

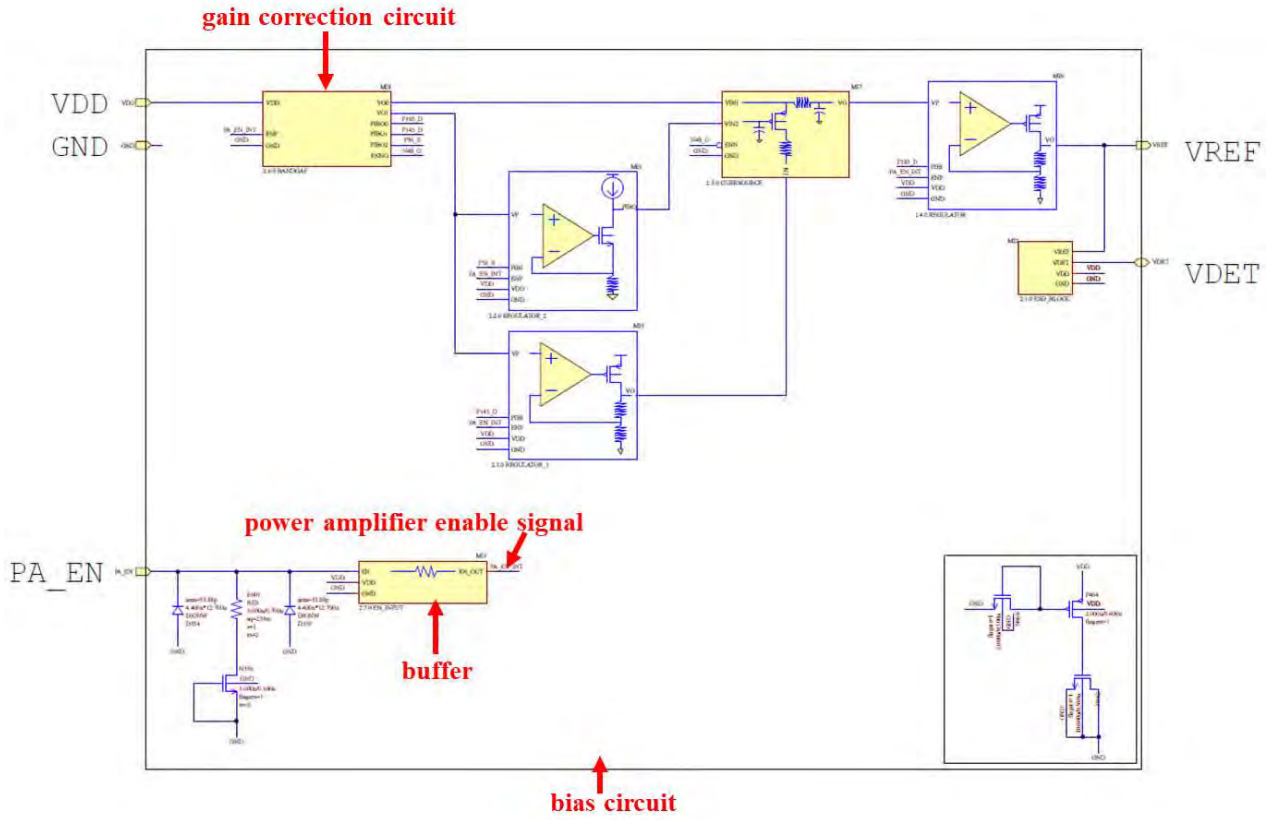
	As shown below in KCT's simplified block diagram for the KCT8539S, a power amplifier (labelled as "PA") is part of the KCT8539S product. Specifically, the KCT8539S "integrates a high-efficiency high-linearity power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated matching network, LO rejection, and harmonic filters all in one device."[3]  *See, e.g.*, simplified block diagram for KCT8539S
14[C] and a bias circuit configured to receive a power amplifier enable	The KCT8539S includes a bias circuit configured to receive a power amplifier enable signal and to generate a bias signal that biases the power amplifier.

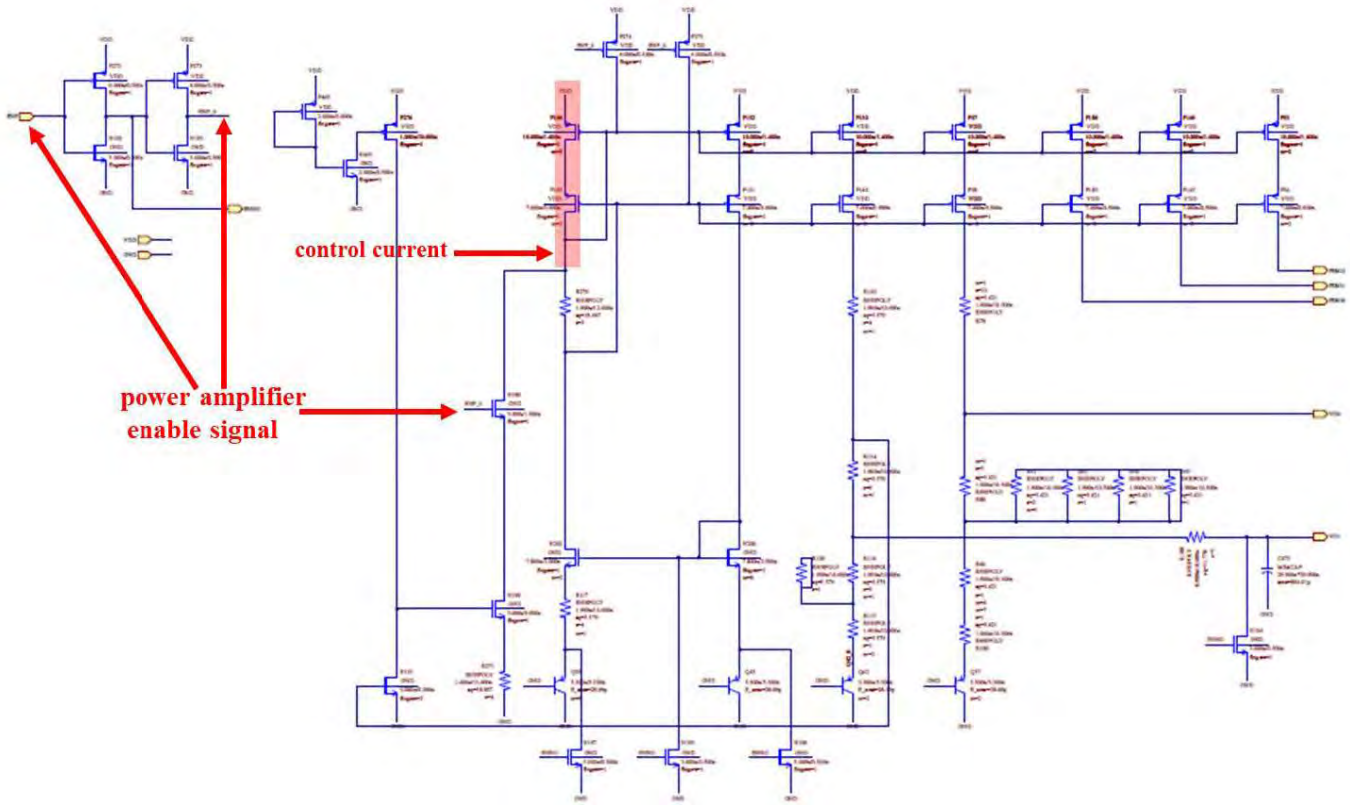
[3] *See* https://perma.cc/DA7F-4CED.

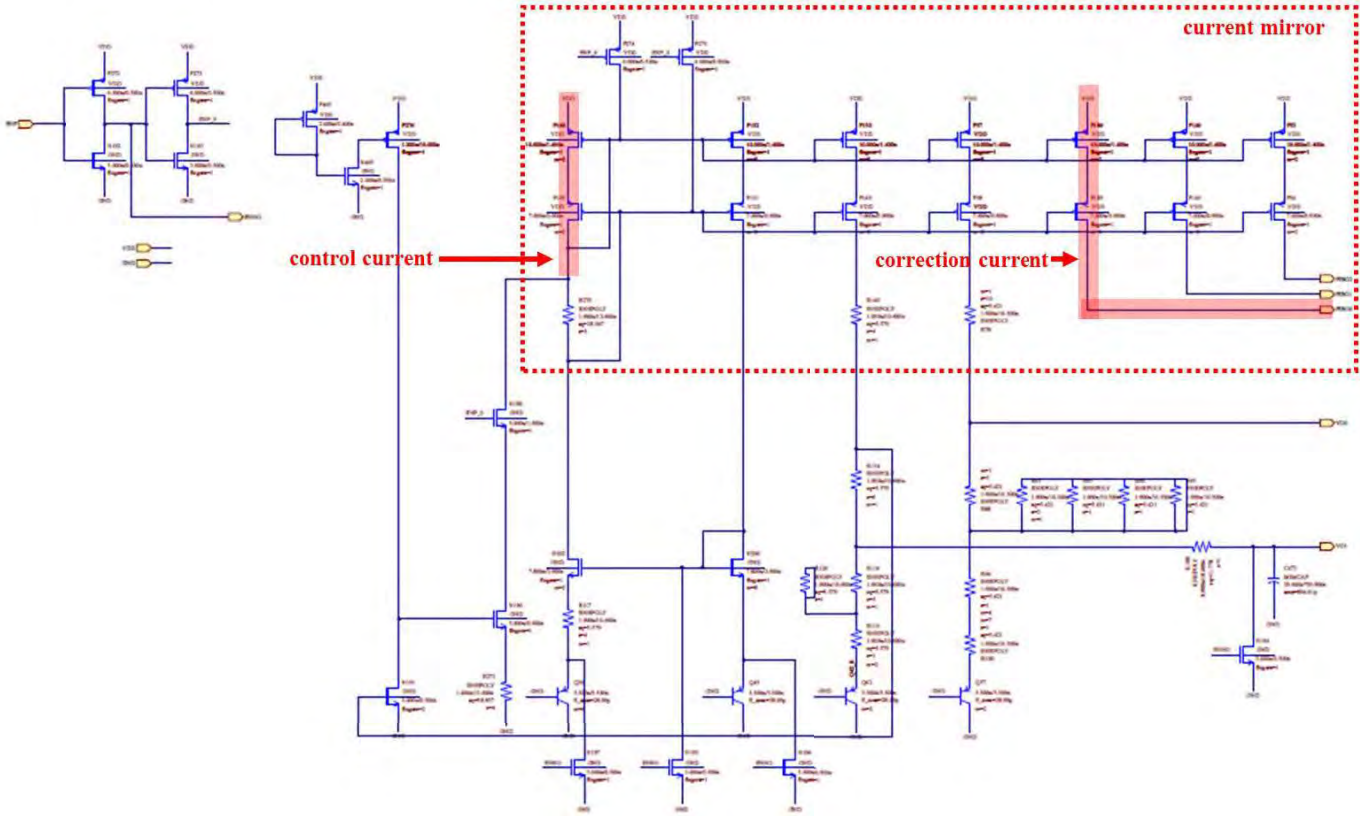
signal and to generate a bias signal that biases the power amplifier,	For example, the image of the KCT8539S below shows a bias circuit and the power amplifier (as indicated by the corresponding labels, respectively).  *See, e.g.*, photo of KCT8539S showing three dies, including a die for the bias circuit and a die for the power amplifier

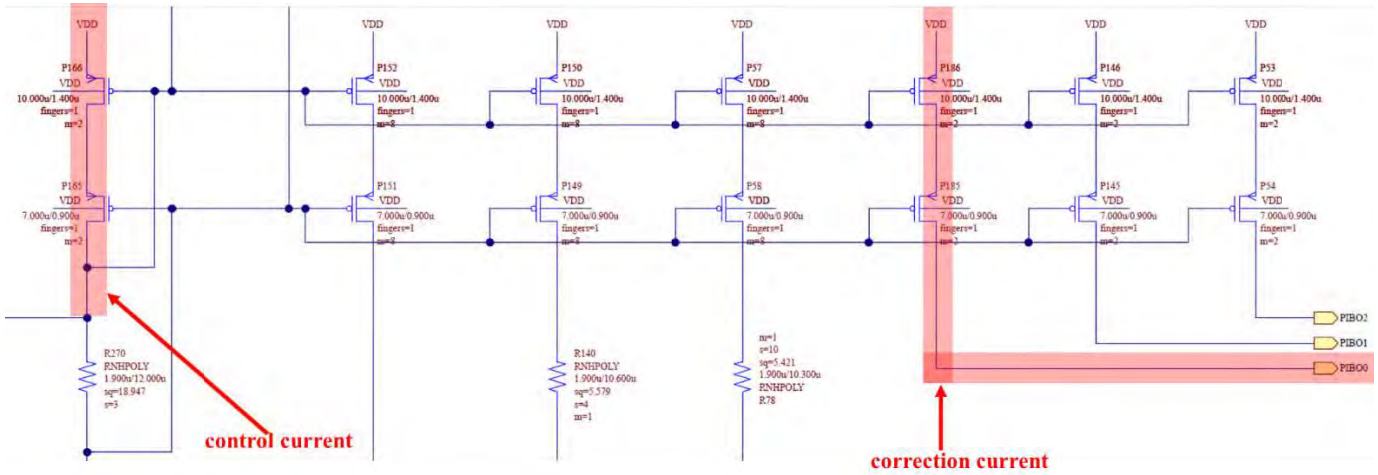
	As another example, the image of the KCT8539S below shows the bias circuit and the power amplifier (as indicated by the corresponding labels, respectively).  *See, e.g.*, photo of KCT8539S showing three dies, including a die for the bias circuit and a die for the power amplifier

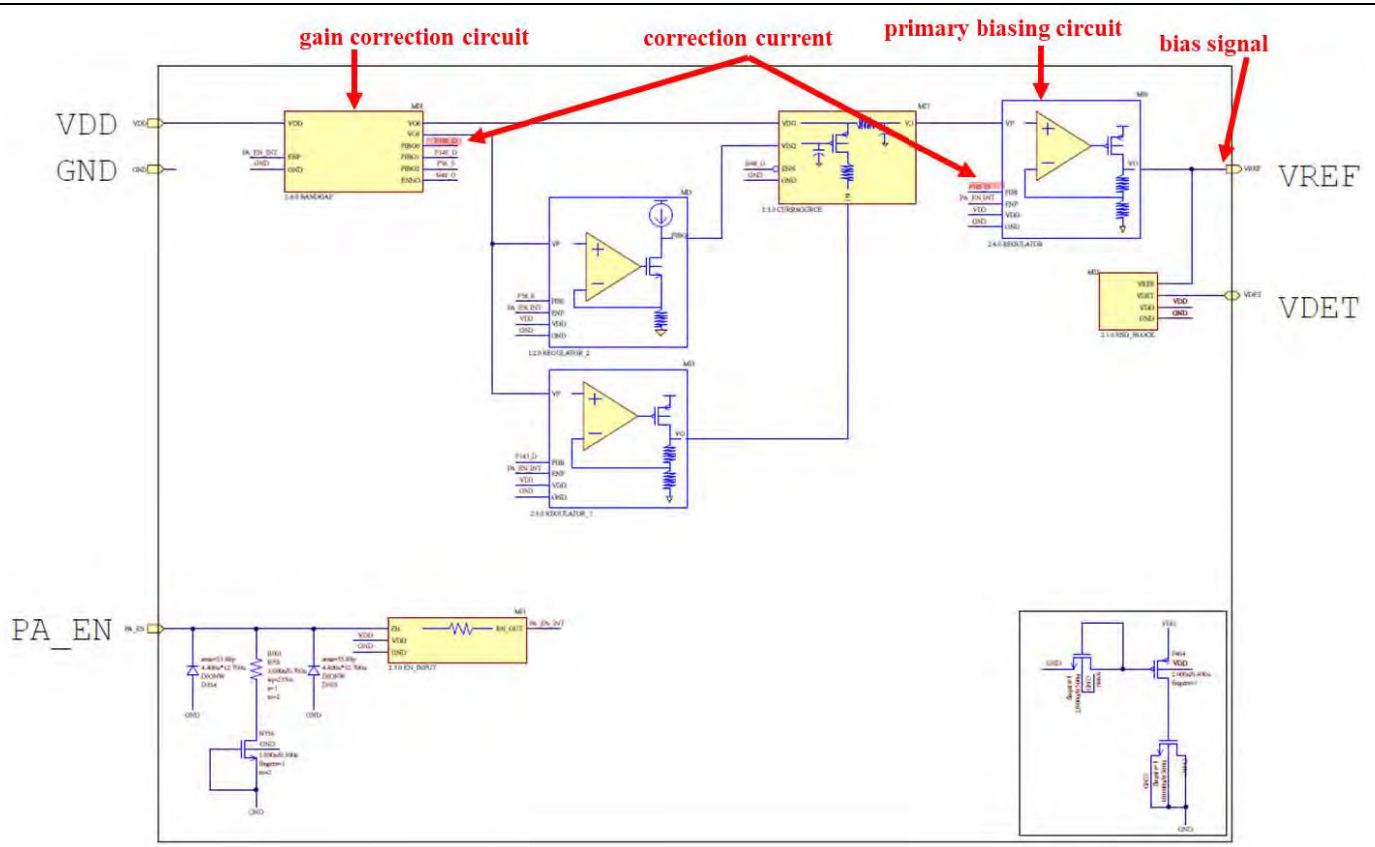
	The bias circuit is coupled to the packaged module's interface through a wire bond in such a way that the bias circuit is configured to receive a power amplifier enable signal (as indicated by the corresponding label above). The bias circuit is coupled to the power amplifier by a wire bond in such a way that the bias circuit is configured to generate a bias signal (as indicated by the corresponding label above) that biases the power amplifier. The reverse engineered schematic below is for the bias circuit (as indicated by the corresponding label below) in the KCT8539S. As highlighted below, the bias circuit includes a "PA_EN" port configured to receive the power amplifier enable signal and a "VREF" port configured to output the bias signal that biases the power amplifier.  *See, e.g.*, reverse engineered schematic of the bias circuit of KCT8539S

	See also elements 14[D] through 14[F] (showing details of the bias circuit).
14[D] the bias circuit including a gain correction circuit configured to generate a control current in response to activation of the power amplifier enable signal,	The KCT8539S includes the bias circuit including a gain correction circuit configured to generate a control current in response to activation of the power amplifier enable signal. For example, the reverse engineered schematic below for the bias circuit in the KCT8539S shows that the bias circuit includes a gain correction circuit (as indicated by the corresponding label below).  *See, e.g.*, reverse engineered schematic of the bias circuit of KCT8539S

	The reverse engineered schematic below for the KCT8539S shows the internal details of the gain correction circuit set forth above. The gain correction circuit receives the power amplifier enable signal (as indicated by the corresponding label below). The power amplifier enable signal is coupled in a way such that the gain correction circuit is configured to generate the control current (as indicated by the corresponding label below) in response to activation of the power amplifier enable signal.  *See, e.g.*, reverse engineered schematic of the gain correction circuit of KCT8539S

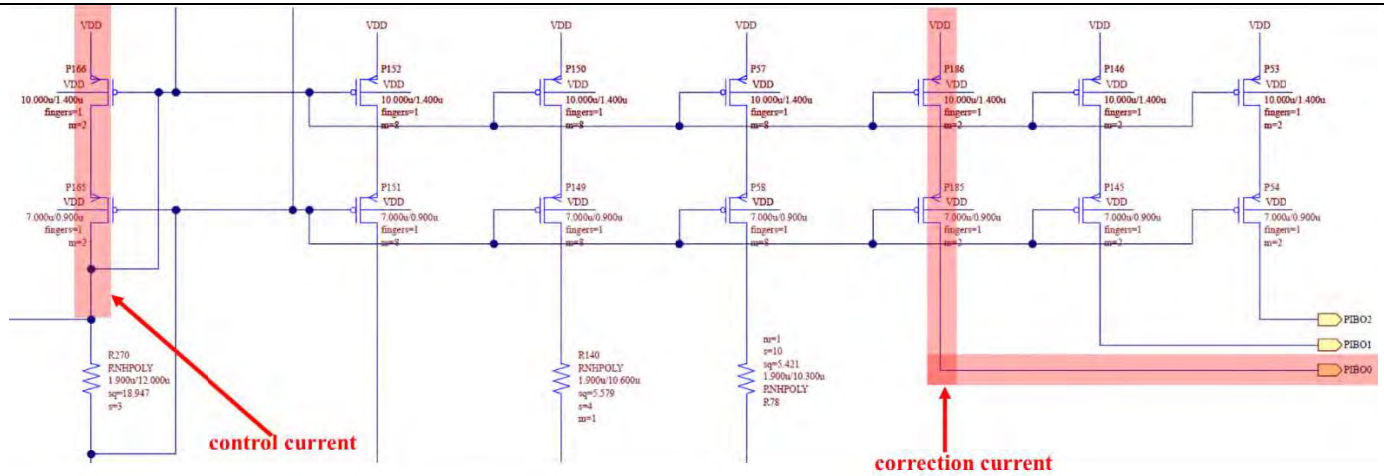
14[E] and to mirror the control current to generate a correction current,	In the KCT8539S, the bias circuit and its gain correction circuit mirrors the control current to generate a correction current. For example, as shown by the reverse engineered schematic below for the gain correction circuit of the KCT8539S, the gain correction circuit includes a current mirror (as indicated by the corresponding label below). The current mirror is configured to mirror the control current to generate the correction current (as indicated by the corresponding label below). The dashed box with the label below is one example of a current mirror that mirrors the control current to generate the correction current.  *See, e.g.*, reverse engineered schematic of the gain correction circuit of KCT8539S

	The schematic below for the KCT8539S is an enlarged view of a portion of the current mirror identified above, which is configured to mirror the control current to generate the correction current. As set forth in the '563 patent, a current mirror can have any suitable gain when mirroring a current. *See* '563 patent, 11:63-12:2. For example, the current mirror in KCT8539S is configured to mirror the control current by a factor of about 1, based on the multiple numbers designated in the schematic below (e.g., "m=2" for the control current and "m=2" for the correction current).  *See, e.g.*, enlarged portion of reverse engineered schematic of the gain correction circuit of KCT8539S
14[F] and a primary biasing circuit configured to generate the bias signal based on the correction current and the power amplifier enable signal.	In the KCT8539S, the bias circuit includes a primary biasing circuit configured to generate the bias signal based on the correction current and the power amplifier enable signal. For example, as shown in the reverse engineered schematic for the KCT8539S below, a primary biasing circuit (as indicated by the corresponding label below) is configured to generate the bias signal (as indicated by the corresponding label below) for the power amplifier based on the correction current and the power amplifier enable signal.

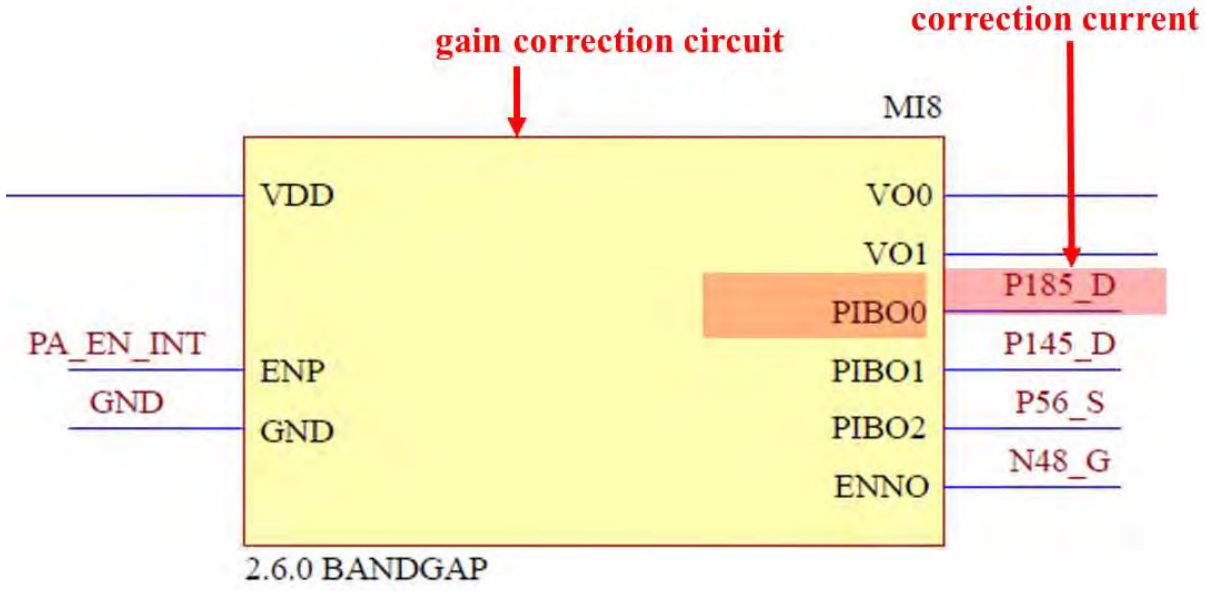


See, e.g., reverse engineered schematic of the bias circuit of KCT8539S

The correction current is output by the "PIBO0" port of the gain correction circuit, as shown by the reverse engineered schematics below.

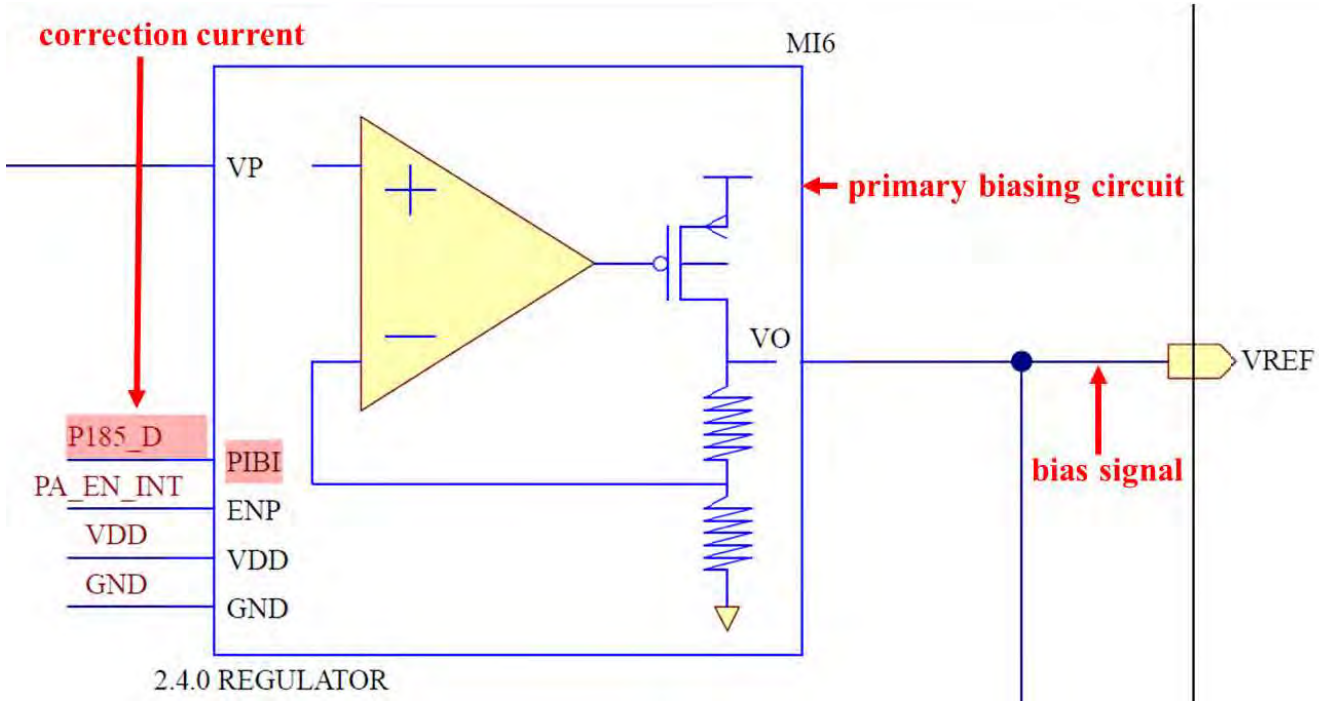


See, e.g., enlarged portion of reverse engineered schematic of the gain correction circuit of KCT8539S



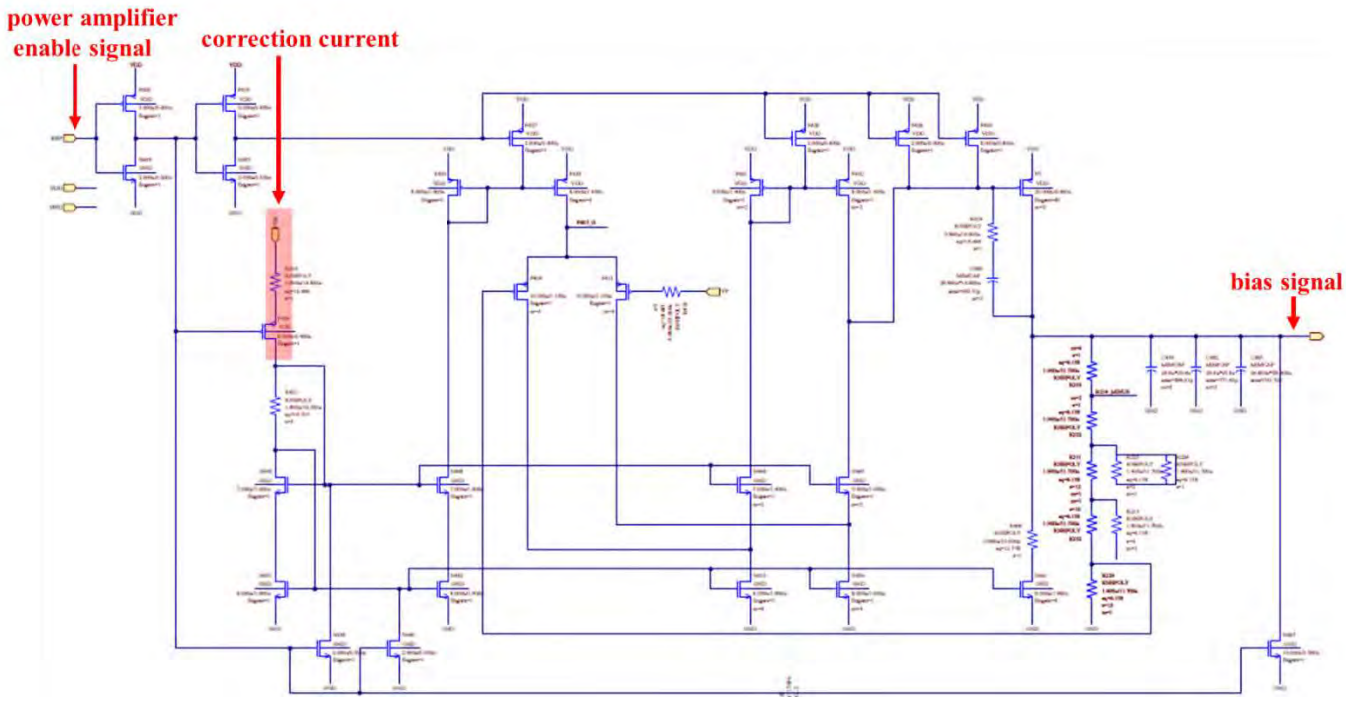
See, e.g., enlarged portion of reverse engineered schematic of the bias circuit of KCT8539S

The "PIBO0" port of the gain correction circuit (shown above and as corresponding to P185_D) is connected to the "PIBI" port of the primary biasing circuit (as indicated by the corresponding label below showing P185_D connecting to PIBI), as shown by the schematic below.



See, e.g., enlarged portion of reverse engineered schematic of the bias circuit of KCT8539S

As shown by the schematic below for the primary biasing circuit of the KCT8539S, the primary biasing circuit takes in the correction current (as indicated by the corresponding label below) as an input and the power amplifier enable signal (as indicated by the corresponding label below) as another input so that the primary biasing circuit is configured to generate the bias signal based on the correction current and the power amplifier enable signal.



See, e.g., reverse engineered schematic of the primary biasing circuit of KCT8539S

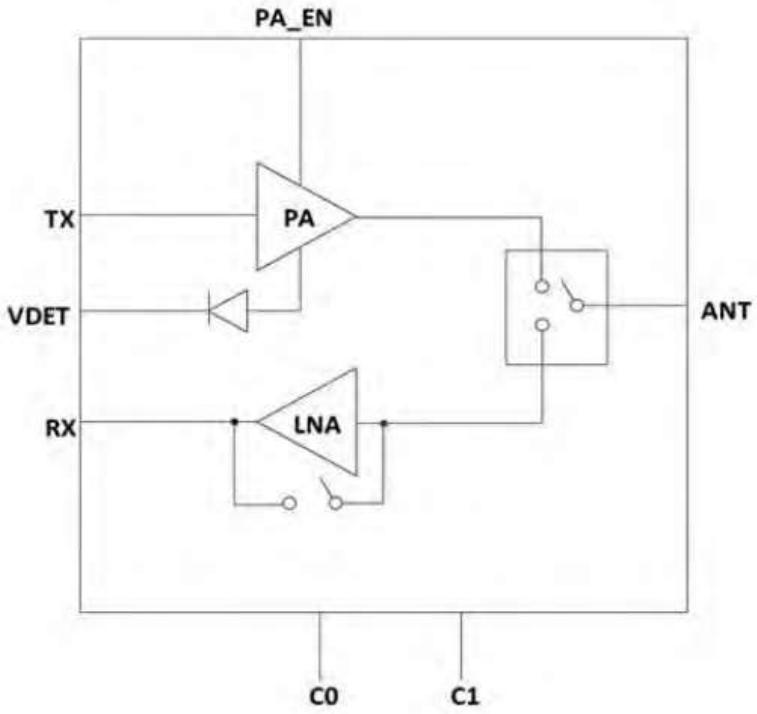
EXHIBIT 17

EXHIBIT 17
SKYWORKS SOLUTIONS, INC.'S INFRINGEMENT CHART
KCT8547HE
U.S. Patent No. 9,917,563
Independent Claim 14

Skyworks Solutions, Inc. ("Skyworks") provides this exemplary claim chart for independent claim 14 of U.S. Patent No. 9,917,563 (the "'563 patent") applied to Kangxi Communication Technologies (Shanghai) Co., Ltd's and Grand Chip Labs, Inc.'s (collectively, "KCT") KCT8547HE product. The disclosures in this claim chart directed to the KCT8547HE are also more broadly directed to any sale, offer for sale, use, or importation of the KCT8547HE in the U.S., including in an end product such as a wireless router or as a standalone product that is not incorporated in an end product.

The claim chart below demonstrates infringement by comparing each element of the charted claim to corresponding components, aspects, and/or features of the KCT8547HE product. This claim chart is not intended to constitute an expert report on infringement. This claim chart includes information provided by way of example, and not by way of limitation.

The analysis set forth below is based only upon information from publicly available sources regarding the KCT8547HE product. Further analysis of non-public information during fact discovery will likely assist in identifying all infringing features and functionalities used by KCT in the KCT8547HE product. Accordingly, Skyworks reserves the right to supplement this infringement analysis once such information is made available to Skyworks. Further, Skyworks reserves the right to supplement this infringement analysis, as appropriate, upon issuance of an order construing any terms recited in the asserted claims or as other circumstances so merit.

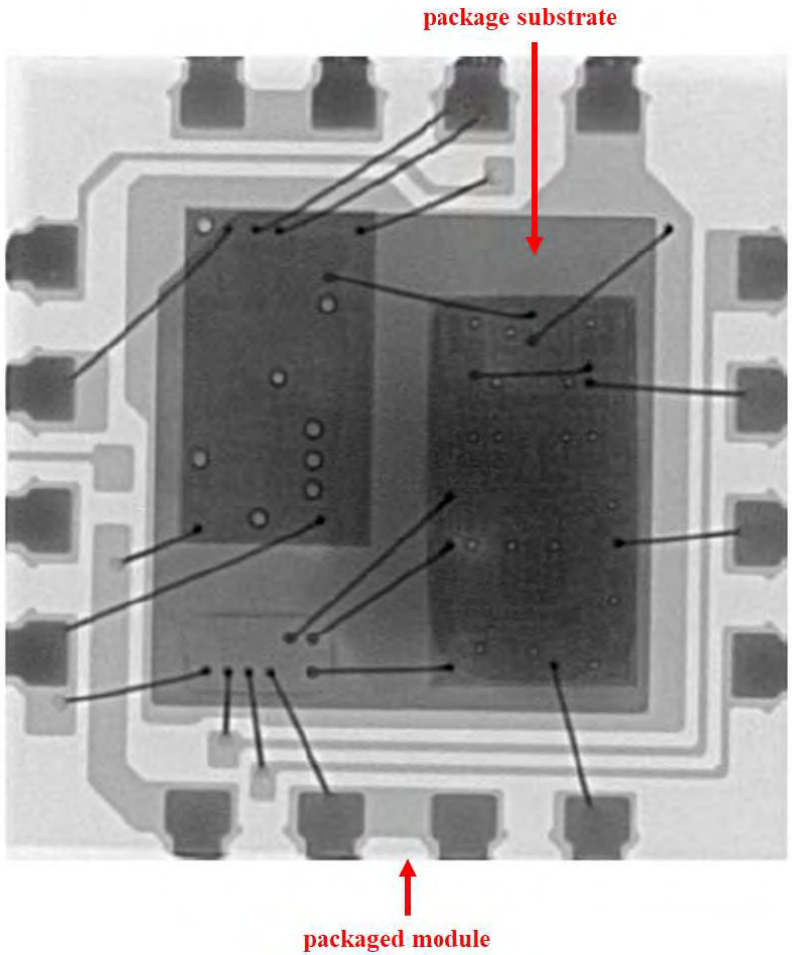
Claim	KCT8547HE
14 [pre] A packaged module comprising:	To the extent the preamble of claim 1 is limiting, the KCT8547HE includes a packaged module. The KCT8547HE is a module for Wi-Fi connectivity. For example, the following image for the KCT8547HE is a simplified block diagram for this product.[1]  *See, e.g.*, simplified block diagram for KCT8547HE The KCT8547HE is, according to KCT, "a highly integrated RF Front-End Integrated Circuit incorporat[ing] key RF functionality needed for IEEE 802.11a/n/ac/ax WLAN systems operating in the

[1] *See* https://perma.cc/GV2Y-HD8A.

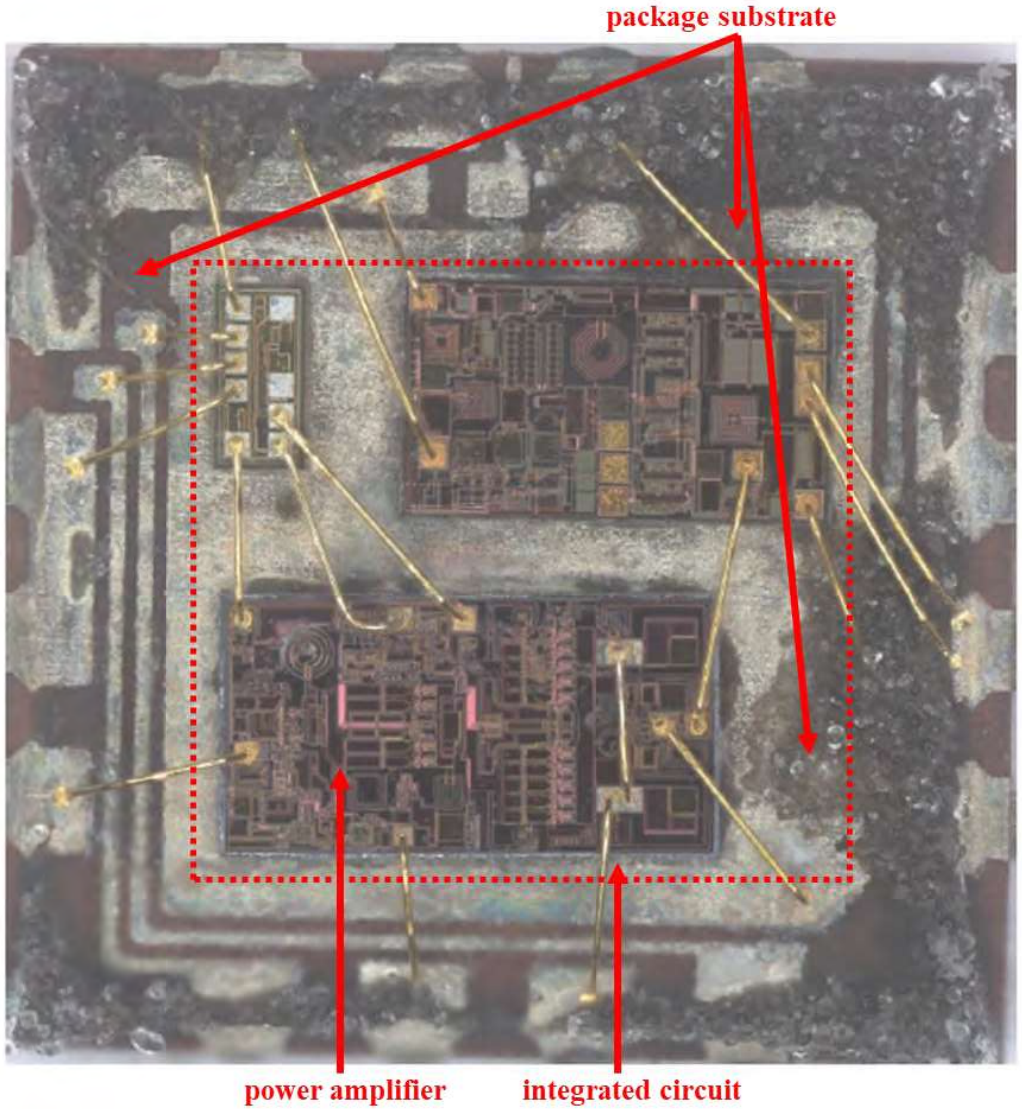
	5.15-5.95GHz range. KCT8547HE-1 integrates a high-efficiency high-linearity power amplifier (PA), a low noise amplifier (LNA) with bypass ….”[2] As another example, the image below of the KCT8547HE shows a packaged module (as indicated by the corresponding label below) for the KCT8547HE.

[2] *See* https://perma.cc/GV2Y-HD8A.

	 *See, e.g.*, photo of KCT8547HE
14[A] a package substrate; and	The KCT8547HE includes a package substrate. For example, the image of the KCT8547HE below shows a package substrate (as indicated by the corresponding label below) as part of the packaged module.

	 *See, e.g.*, photo of KCT8547HE
14[B] an integrated circuit attached to the package substrate and including a power amplifier configured	The KCT8547HE includes an integrated circuit attached to the package substrate and including a power amplifier.

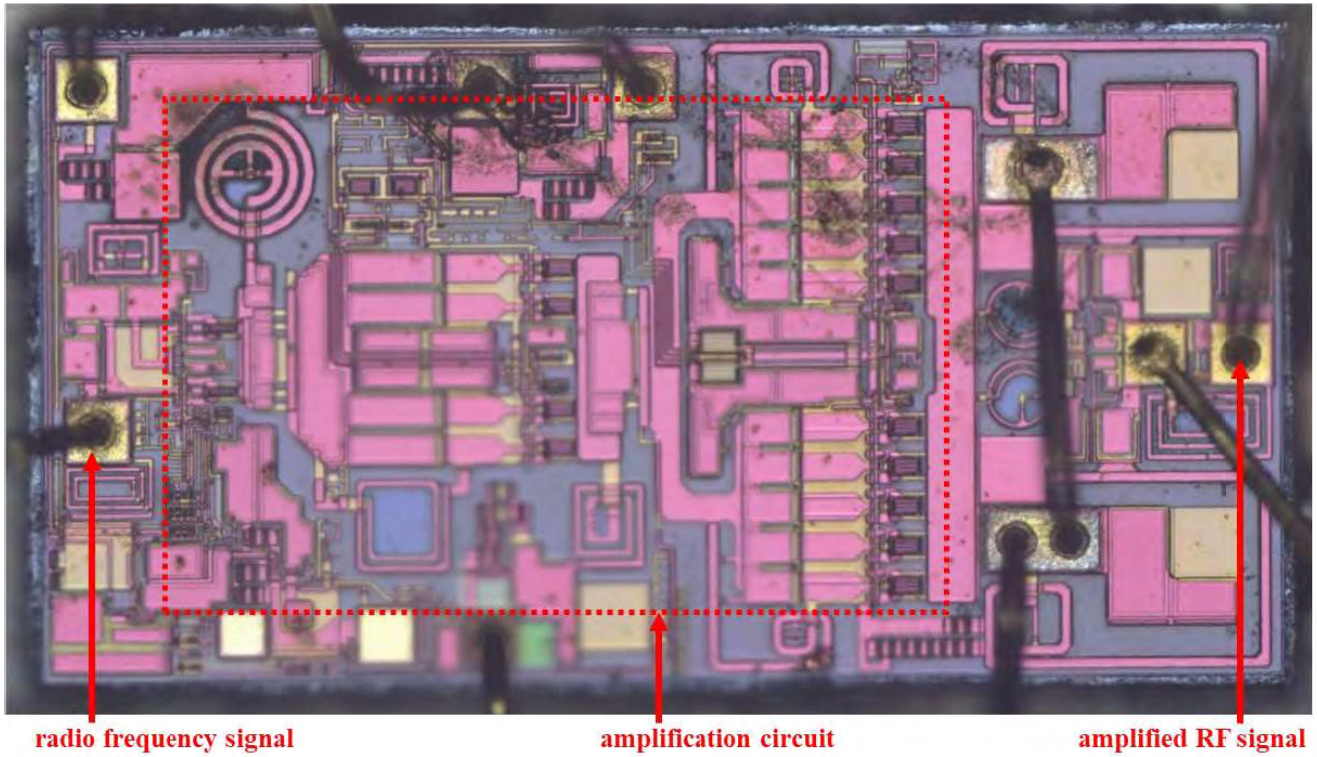
to provide amplification to a radio frequency signal	For example, the image of the KCT8547HE below shows an integrated circuit (as indicated by the corresponding label below) attached to the package substrate and including a power amplifier (as indicated by the corresponding label below).



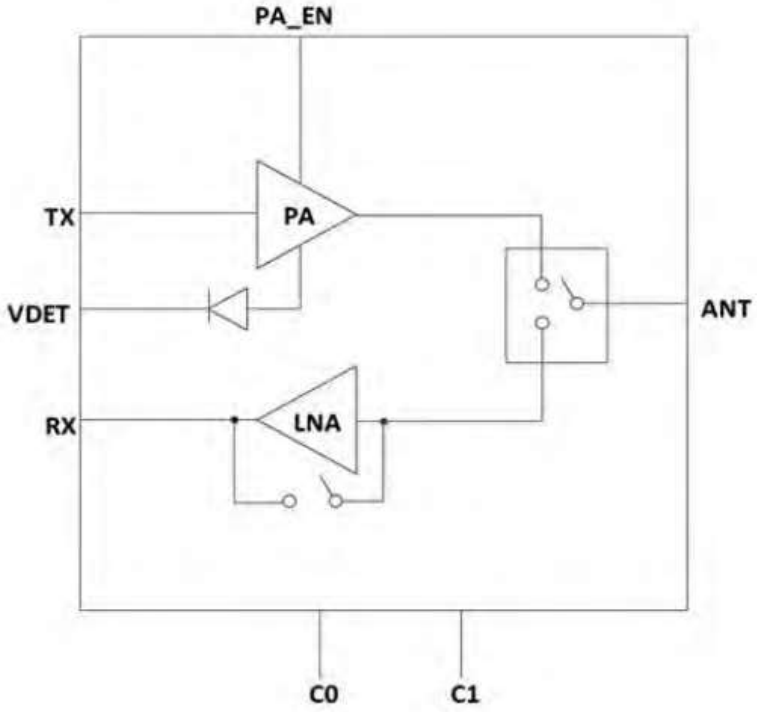
See, e.g., photo of KCT8547HE showing an integrated circuit having three dies including a die for the power amplifier

The power amplifier in the KCT8547HE is configured to provide amplification to a radio frequency signal.

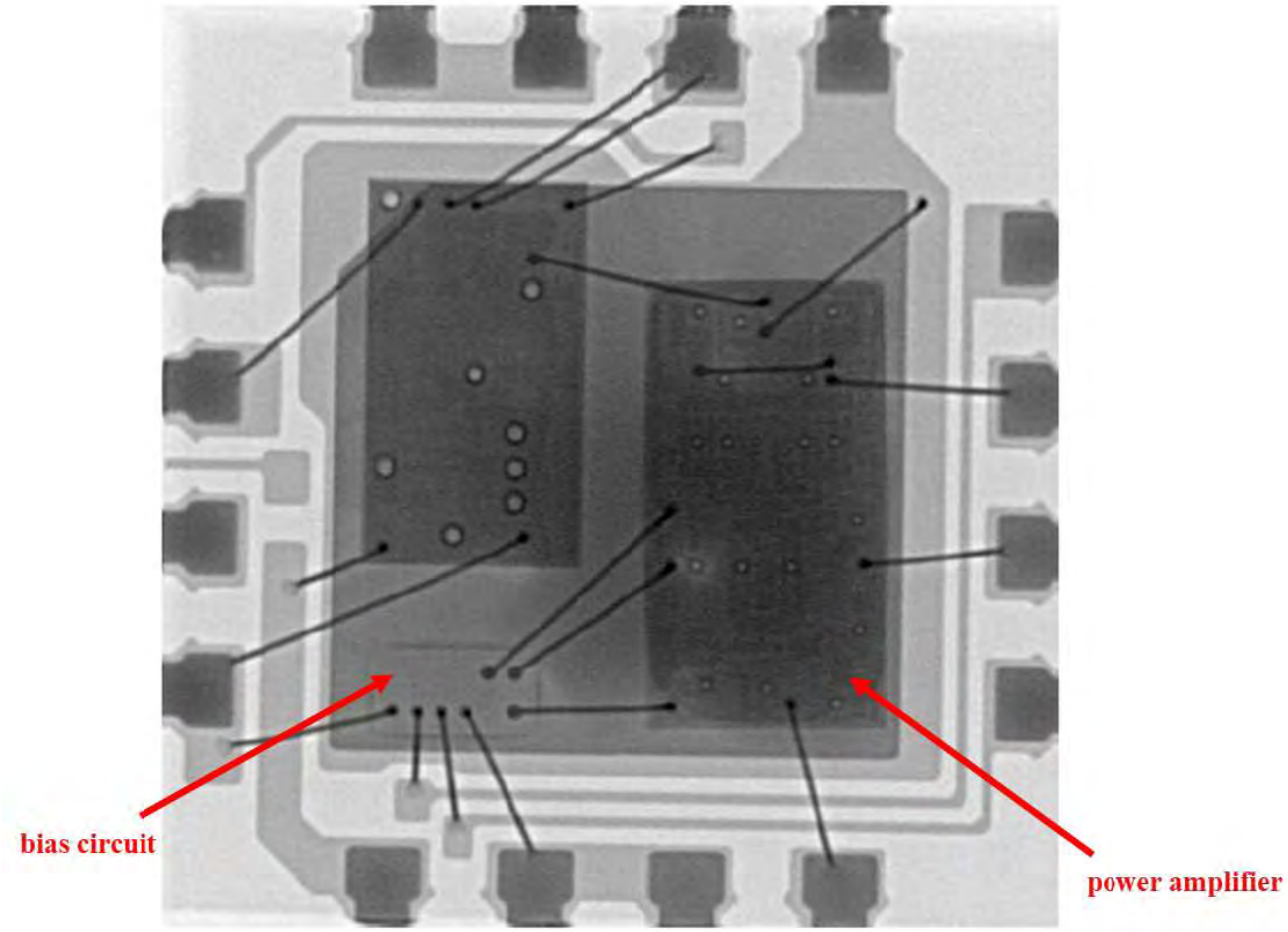
For example, the image below shows an enlarged view of the power amplifier die of the KCT8547HE. The power amplifier is coupled in such a way that it is configured to receive as an input a radio frequency (RF) signal, as labeled below as the radio frequency signal, and amplify the radio frequency signal to output an amplified RF signal, as labeled below. The dashed box with the corresponding label below is one example of an amplification circuit that provides the amplification of the radio frequency signal.

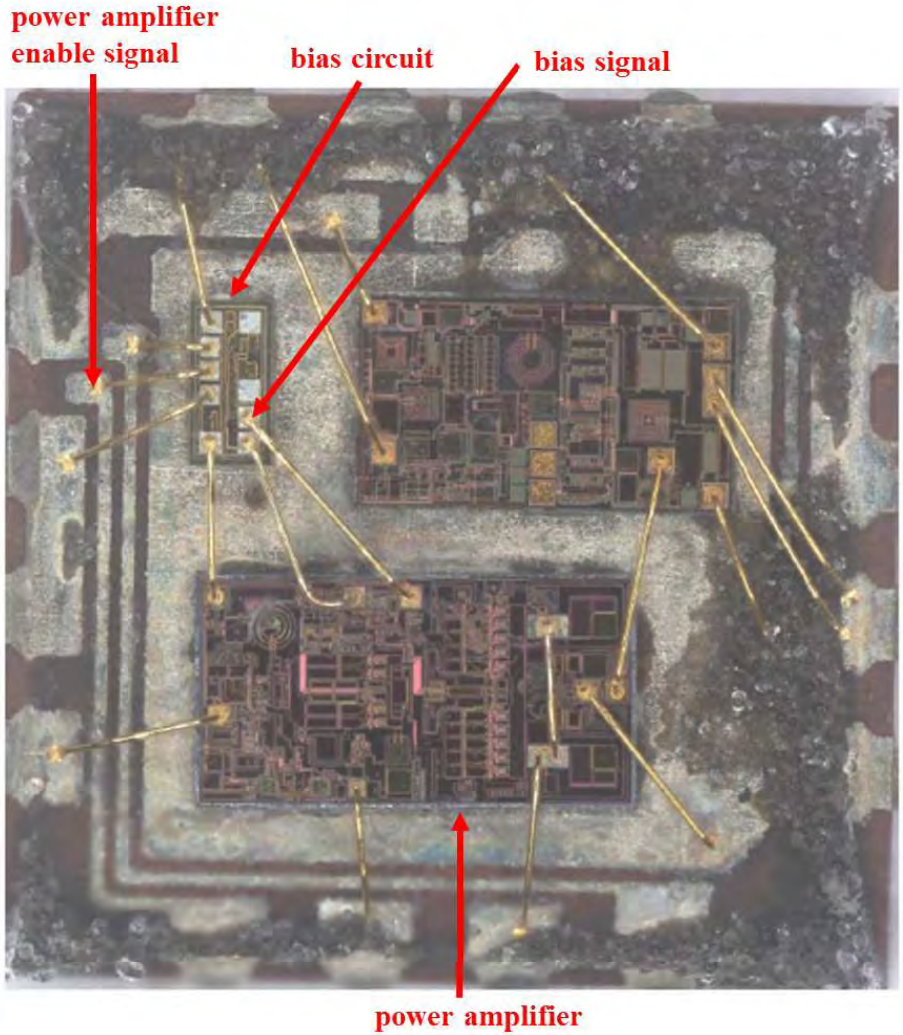


See, e.g., photo of the power amplifier die of KCT8547HE

	As shown below in KCT's simplified block diagram for the KCT8547HE, a power amplifier (labelled as "PA") is part of the KCT8547HE product. Specifically, the KCT8547HE "integrates a high-efficiency high-linearity power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated matching network and harmonic filters all in one device."[3]  *See, e.g.*, simplified block diagram for KCT8547HE
14[C] and a bias circuit configured to receive a power amplifier enable	The KCT8547HE includes a bias circuit configured to receive a power amplifier enable signal and to generate a bias signal that biases the power amplifier.

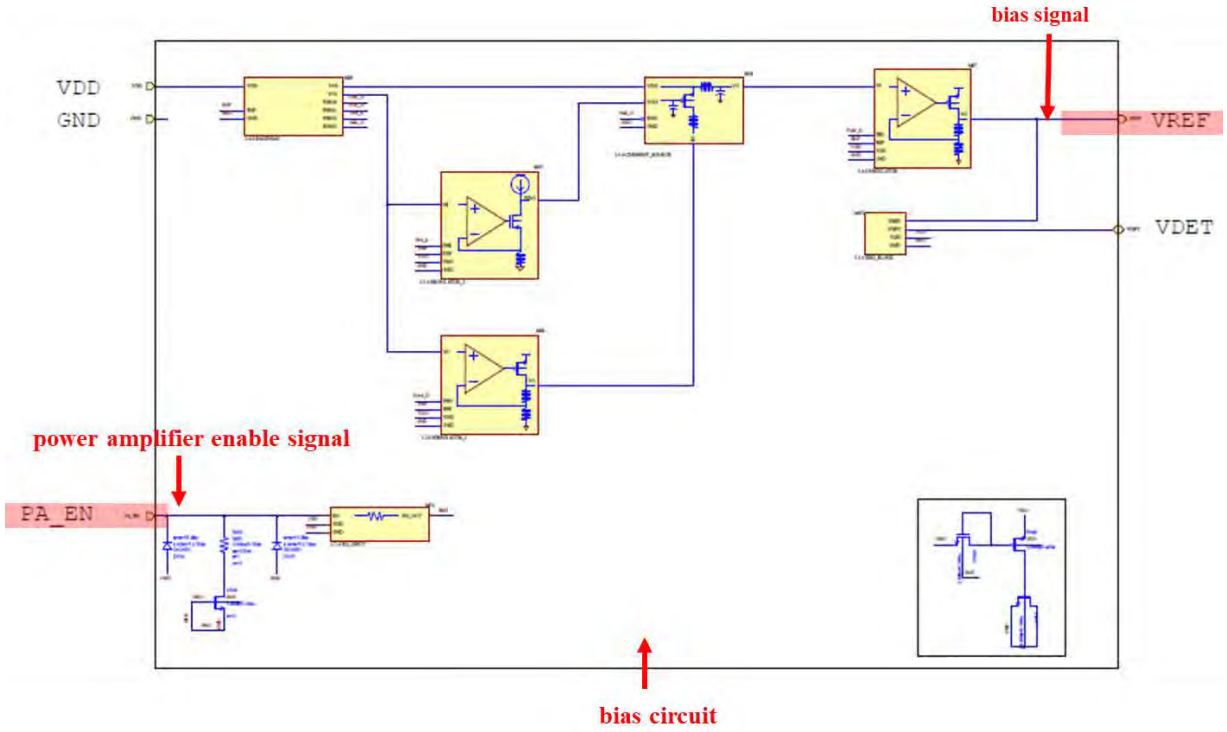
[3] *See* https://perma.cc/GV2Y-HD8A.

signal and to generate a bias signal that biases the power amplifier,	For example, the image of the KCT8547HE below shows a bias circuit and the power amplifier (as indicated by the corresponding labels, respectively).  *See, e.g.*, photo of KCT8547HE showing three dies, including a die for the bias circuit and a die for the power amplifier

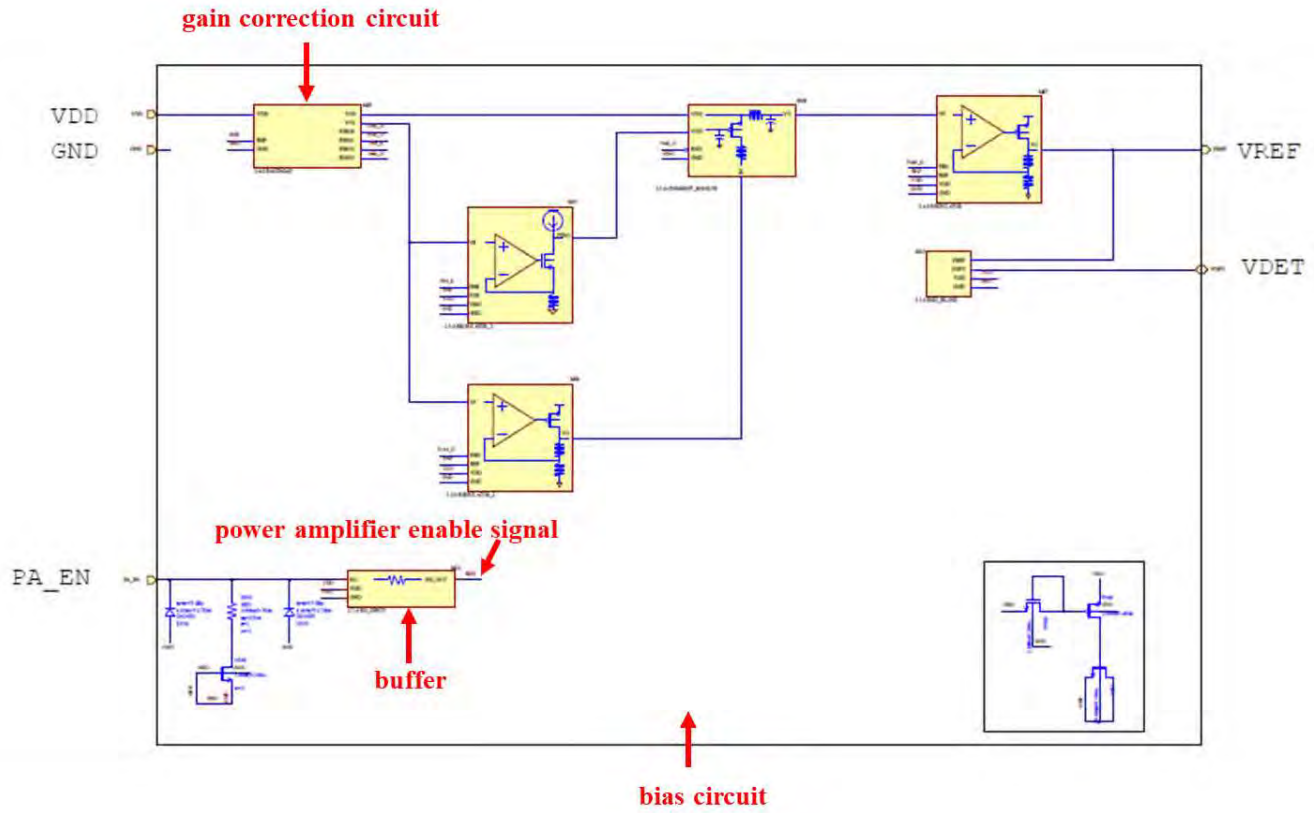
	As another example, the image of the KCT8547HE below shows the bias circuit and the power amplifier (as indicated by the corresponding labels, respectively).  *See, e.g.*, photo of KCT8547HE showing three dies, including a die for the bias circuit and a die for the power amplifier

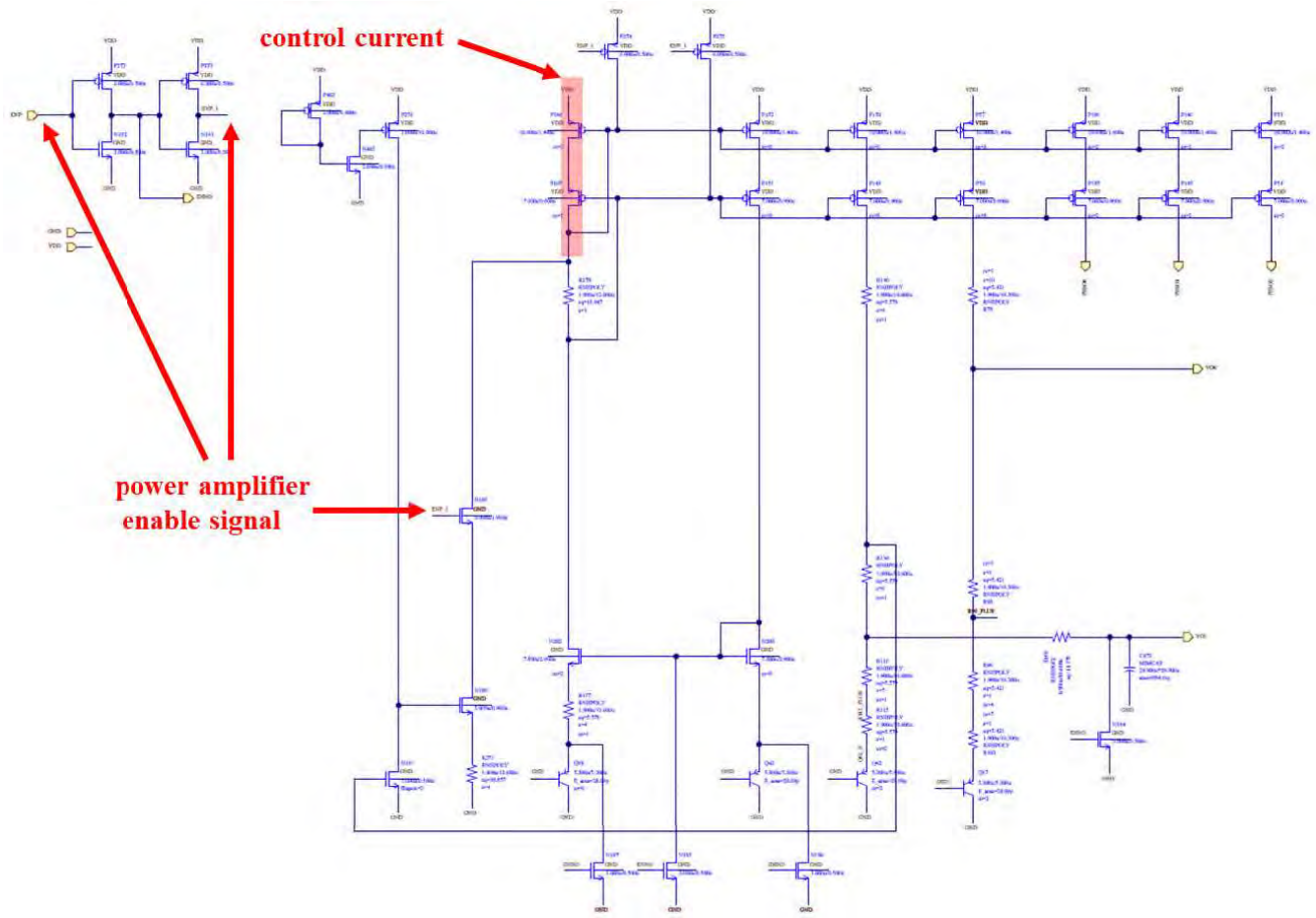
The bias circuit is coupled to the packaged module's interface through a wire bond in such a way that the bias circuit is configured to receive a power amplifier enable signal (as indicated by the corresponding label above). The bias circuit is coupled to the power amplifier by a wire bond in such a way that the bias circuit is configured to generate a bias signal (as indicated by the corresponding label above) that biases the power amplifier.

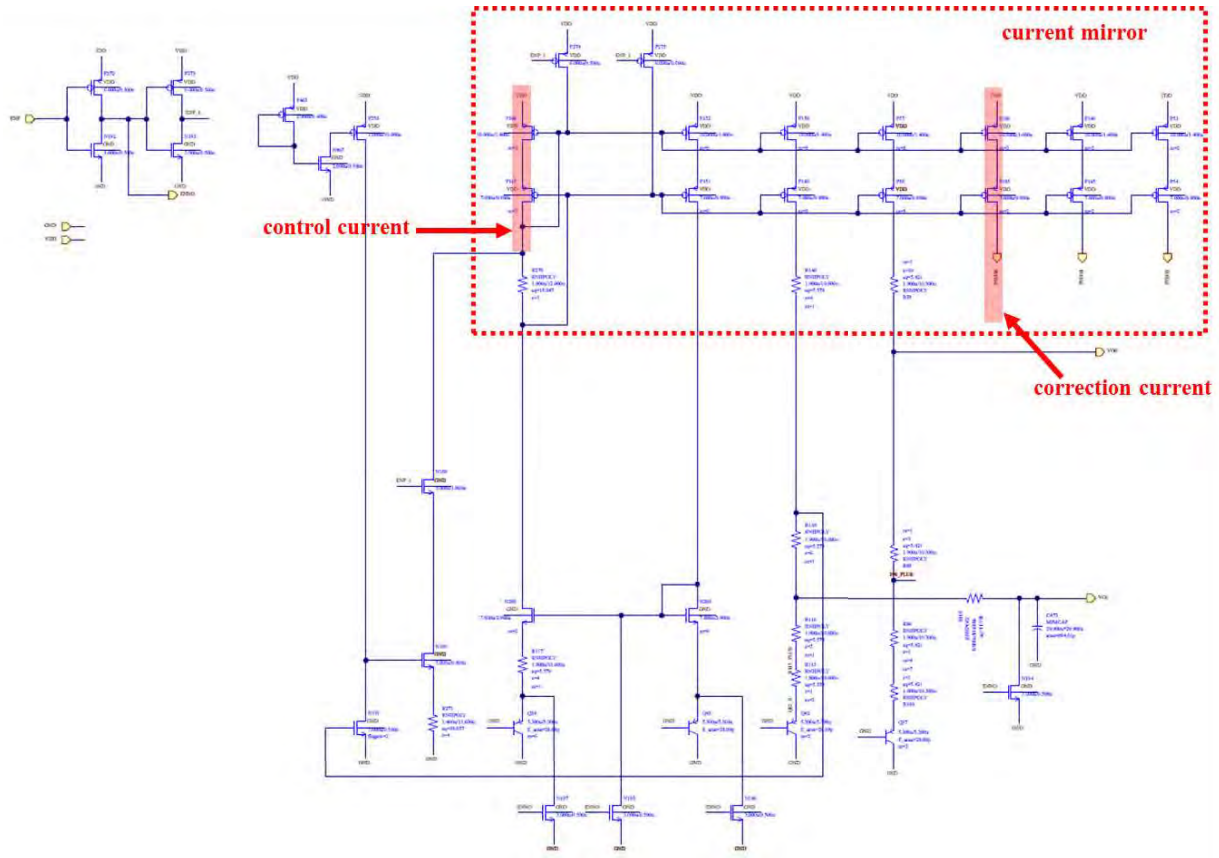
The reverse engineered schematic below is for the bias circuit (as indicated by the corresponding label below) in the KCT8547HE. As highlighted below, the bias circuit includes a "PA_EN" port configured to receive the power amplifier enable signal and a "VREF" port configured to output the bias signal that biases the power amplifier.

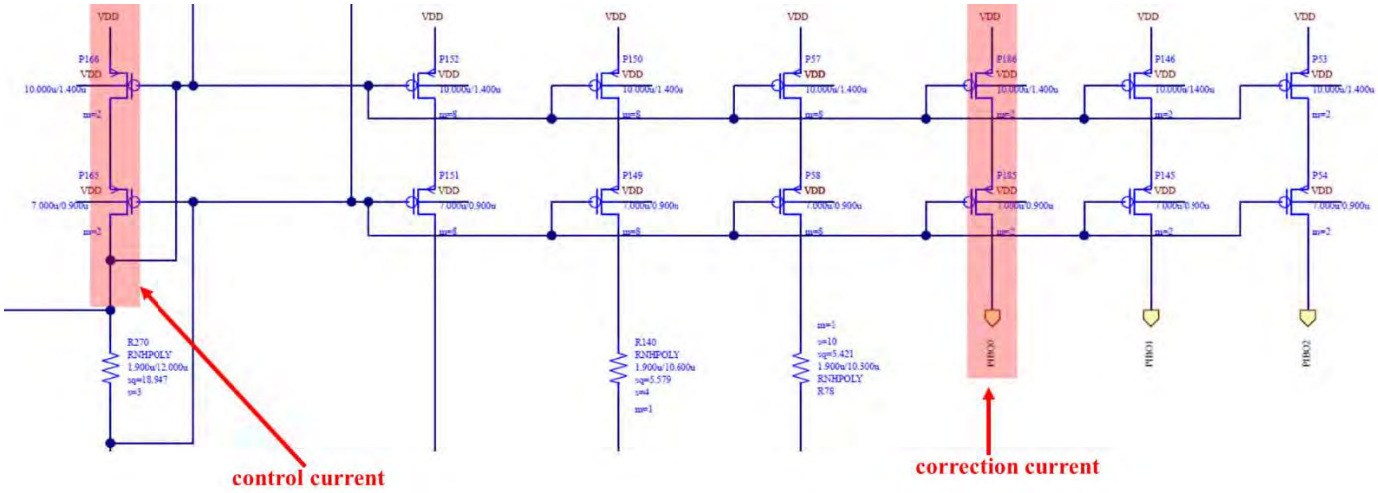


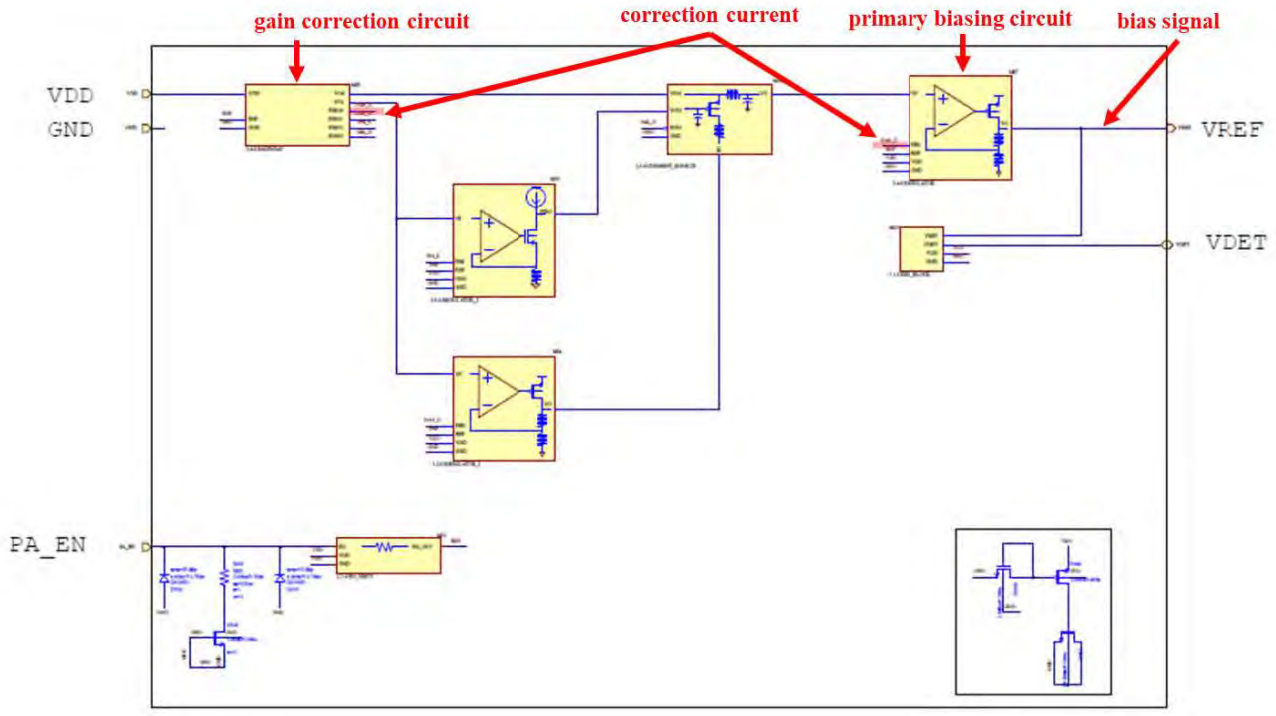
See, e.g., reverse engineered schematic of the bias circuit of KCT8547HE

	See also elements 14[D] through 14[F] (showing details of the bias circuit).
14[D] the bias circuit including a gain correction circuit configured to generate a control current in response to activation of the power amplifier enable signal,	The KCT8547HE includes the bias circuit including a gain correction circuit configured to generate a control current in response to activation of the power amplifier enable signal. For example, the reverse engineered schematic below for the bias circuit in the KCT8547HE shows that the bias circuit includes a gain correction circuit (as indicated by the corresponding label below).  *See, e.g.*, reverse engineered schematic of the bias circuit of KCT8547HE The reverse engineered schematic below for the KCT8547HE shows the internal details of the gain correction circuit set forth above. The gain correction circuit receives the power amplifier enable signal (as

	indicated by the corresponding label below). The power amplifier enable signal is coupled in a way such that the gain correction circuit is configured to generate the control current (as indicated by the corresponding label below) in response to activation of the power amplifier enable signal.  *See, e.g.*, reverse engineered schematic of the gain correction circuit of KCT8547HE

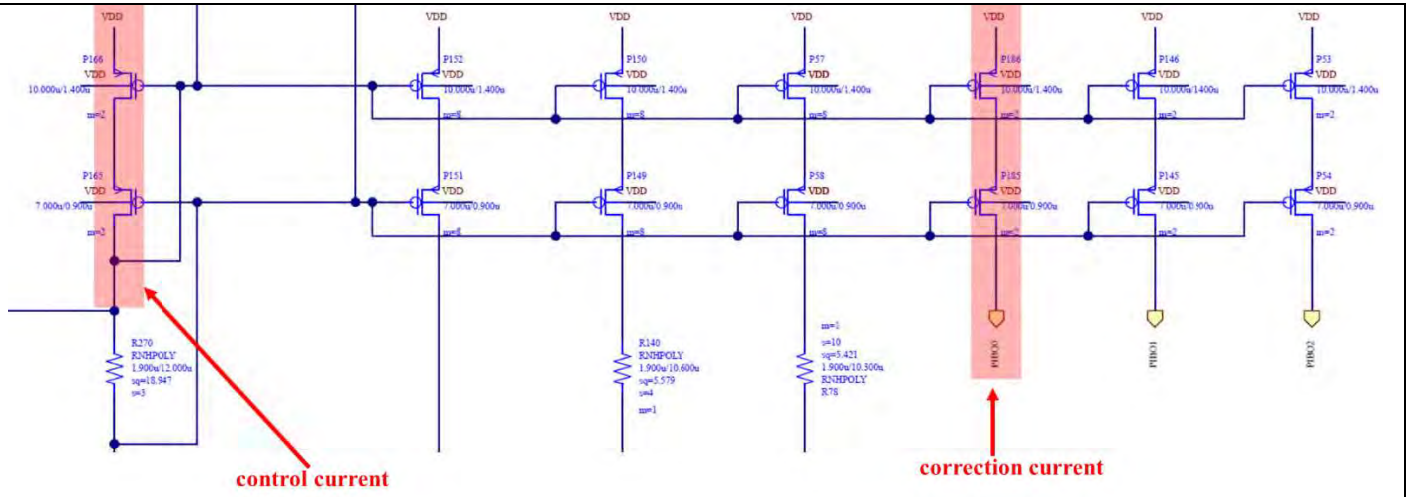
14[E] and to mirror the control current to generate a correction current,	In the KCT8547HE, the bias circuit and its gain correction circuit mirrors the control current to generate a correction current. For example, as shown by the reverse engineered schematic below for the gain correction circuit of the KCT8547HE, the gain correction circuit includes a current mirror (as indicated by the corresponding label below). The current mirror is configured to mirror the control current to generate the correction current (as indicated by the corresponding label below). The dashed box with the label below is one example of a current mirror that mirrors the control current to generate the correction current.  *See, e.g.*, reverse engineered schematic of the gain correction circuit of KCT8547HE

	The schematic below for the KCT8547HE is an enlarged view of a portion of the current mirror identified above, which is configured to mirror the control current to generate the correction current. As set forth in the '563 patent, a current mirror can have any suitable gain when mirroring a current. *See* '563 patent, 11:63-12:2. For example, the current mirror in KCT8547HE is configured to mirror the control current by a factor of about 1, based on the multiple numbers designated in the schematic below (e.g., "m=2" for the control current and "m=2" for the correction current).  *See, e.g.*, enlarged portion of reverse engineered schematic of the gain correction circuit of KCT8547HE
14[F] and a primary biasing circuit configured to generate the bias signal based on the correction current and the power amplifier enable signal.	In the KCT8547HE, the bias circuit includes a primary biasing circuit configured to generate the bias signal based on the correction current and the power amplifier enable signal. For example, as shown in the reverse engineered schematic for the KCT8547HE below, a primary biasing circuit (as indicated by the corresponding label below) is configured to generate the bias signal (as indicated by the corresponding label below) for the power amplifier based on the correction current and the power amplifier enable signal.

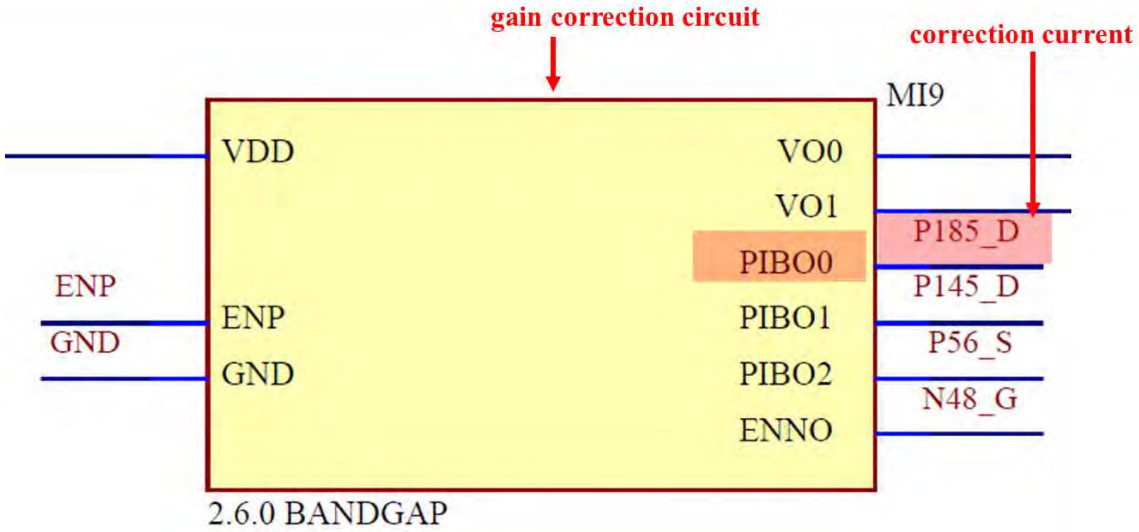


See, e.g., reverse engineered schematic of the bias circuit of KCT8547HE

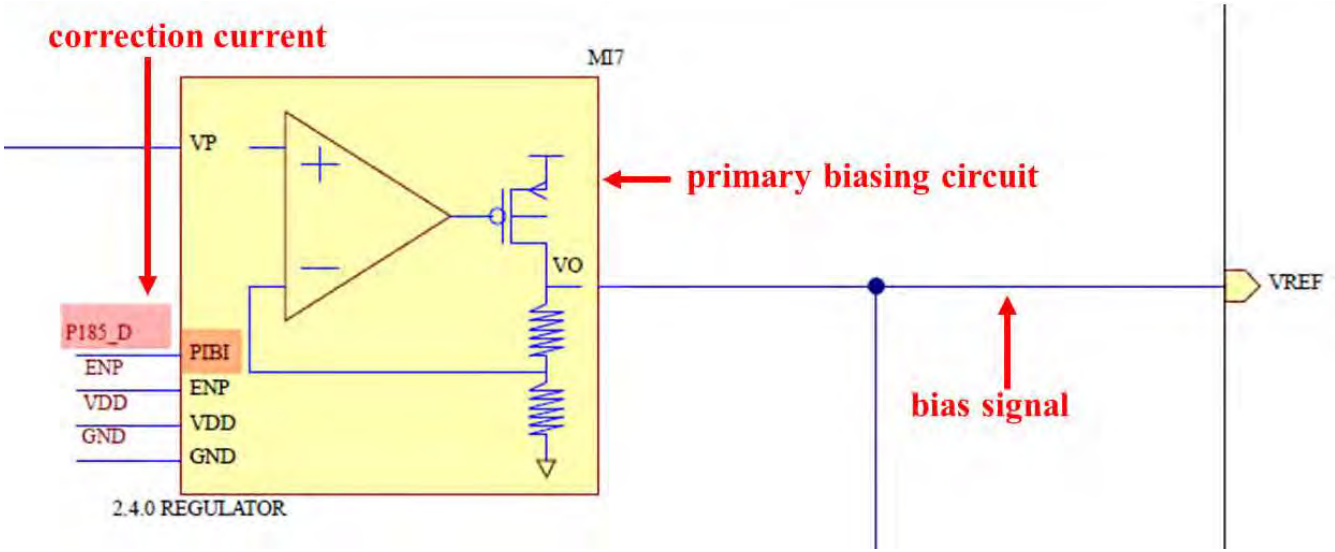
The correction current is output by the "PIBO0" port of the gain correction circuit, as shown by the reverse engineered schematics below.

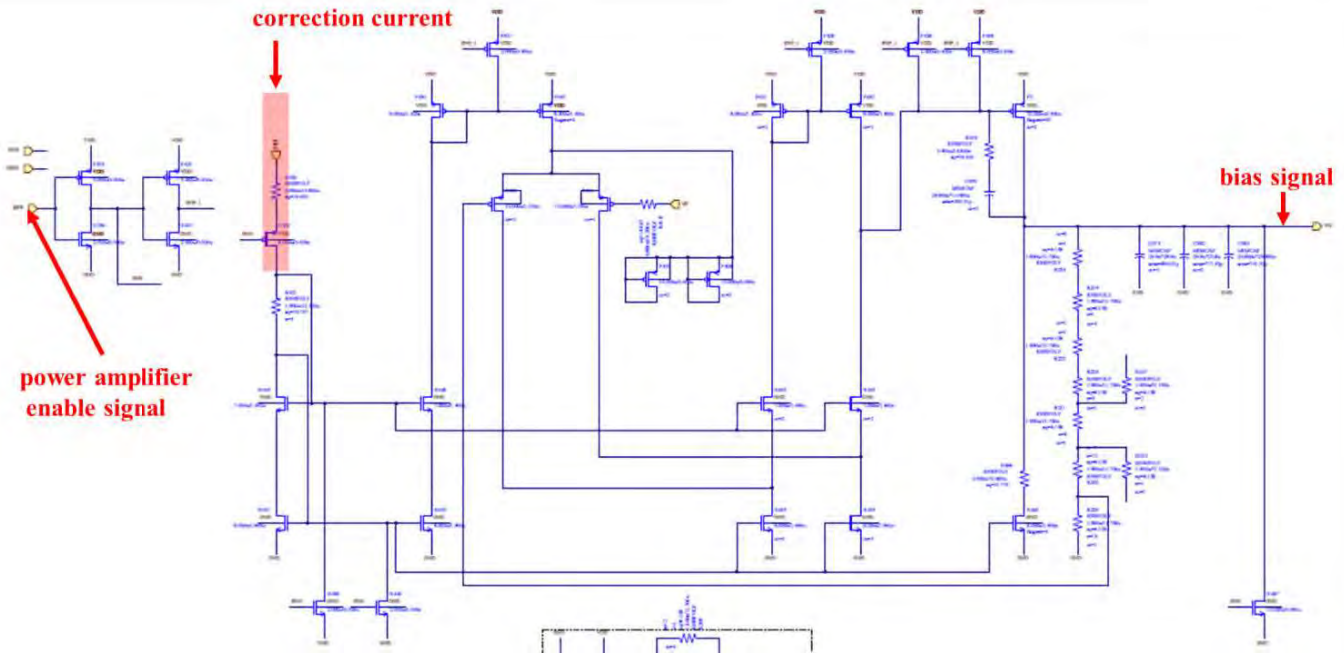


See, e.g., enlarged portion of reverse engineered schematic of the gain correction circuit of KCT8547HE



See, e.g., enlarged portion of reverse engineered schematic of the bias circuit of KCT8547HE

	The "PIBO0" port of the gain correction circuit (shown above and as corresponding to P185_D) is connected to the "PIBI" port of the primary biasing circuit (as indicated by the corresponding label below showing P185_D connecting to PIBI), as shown by the schematic below.  *See, e.g.*, enlarged portion of reverse engineered schematic of the bias circuit of KCT8547HE As shown by the schematic below for the primary biasing circuit of the KCT8547HE, the primary biasing circuit takes in the correction current (as indicated by the corresponding label below) as an input and the power amplifier enable signal (as indicated by the corresponding label below) as another input so that the primary biasing circuit is configured to generate the bias signal based on the correction current and the power amplifier enable signal.



See, e.g., reverse engineered schematic of the primary biasing circuit of KCT8547HE

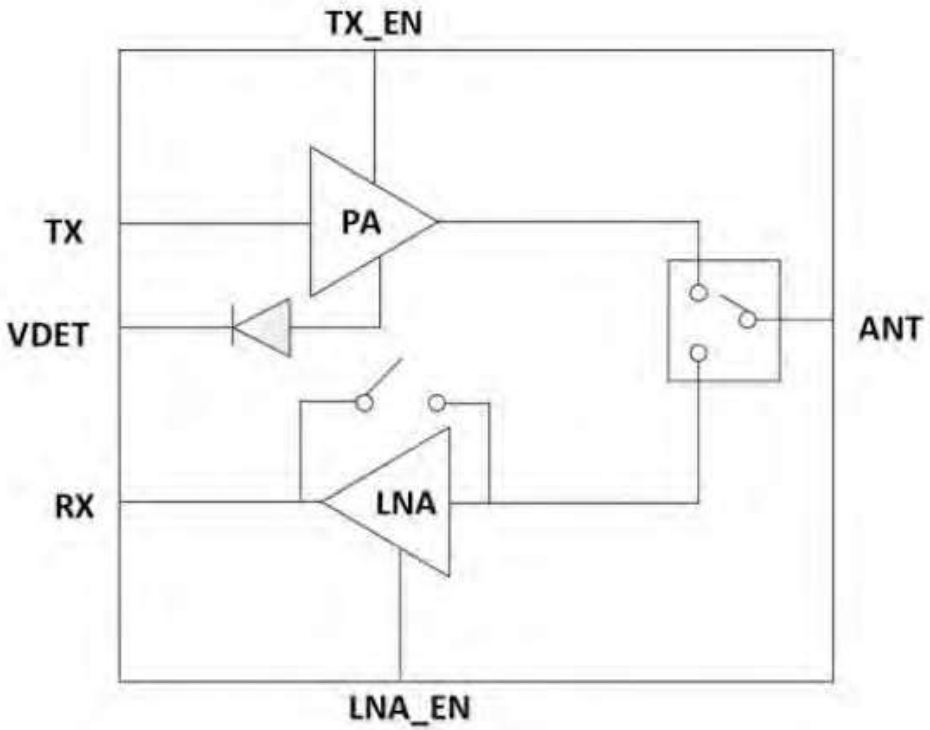
EXHIBIT 18

EXHIBIT 18
SKYWORKS SOLUTIONS, INC.'S INFRINGEMENT CHART
KCT8576HE
U.S. Patent No. 9,917,563
Independent Claim 14

Skyworks Solutions, Inc. ("Skyworks") provides this exemplary claim chart for independent claim 14 of U.S. Patent No. 9,917,563 (the "'563 patent") applied to Kangxi Communication Technologies (Shanghai) Co., Ltd's and Grand Chip Labs, Inc.'s (collectively, "KCT") KCT8576HE product. The disclosures in this claim chart directed to the KCT8576HE are also more broadly directed to any sale, offer for sale, use, or importation of the KCT8576HE in the U.S., including in an end product such as a wireless router or as a standalone product that is not incorporated in an end product.

The claim chart below demonstrates infringement by comparing each element of the charted claim to corresponding components, aspects, and/or features of the KCT8576HE product. This claim chart is not intended to constitute an expert report on infringement. This claim chart includes information provided by way of example, and not by way of limitation.

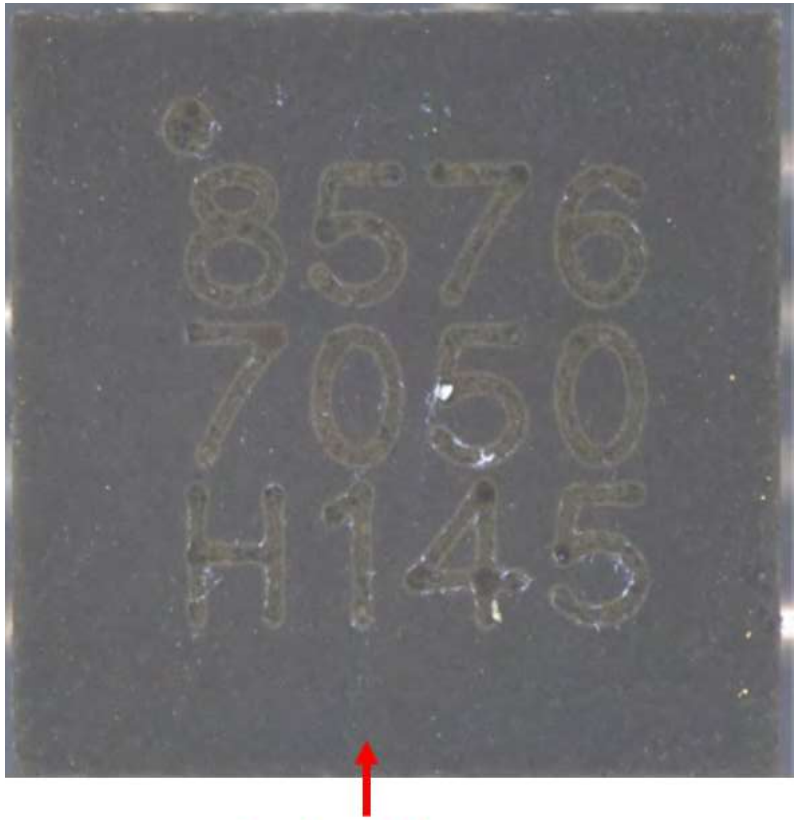
The analysis set forth below is based only upon information from publicly available sources regarding the KCT8576HE product. Further analysis of non-public information during fact discovery will likely assist in identifying all infringing features and functionalities used by KCT in the KCT8576HE product. Accordingly, Skyworks reserves the right to supplement this infringement analysis once such information is made available to Skyworks. Further, Skyworks reserves the right to supplement this infringement analysis, as appropriate, upon issuance of an order construing any terms recited in the asserted claims or as other circumstances so merit.

Claim	KCT8576HE
14 [pre] A packaged module comprising:	To the extent the preamble of claim 1 is limiting, the KCT8576HE includes a packaged module. The KCT8576HE is a module for Wi-Fi connectivity. For example, the following image for the KCT8576HE is a simplified block diagram for this product.[1]  *See, e.g.*, simplified block diagram for KCT8576HE The KCT8576HE is, according to KCT, "a highly integrated RF front-end integrated circuit incorporat[ing] key RF functionality needed for IEEE 802.11a/n/ac/ax WLAN systems operating in the 5.15-5.95GHz

[1] *See* https://perma.cc/N2ZN-83UW.

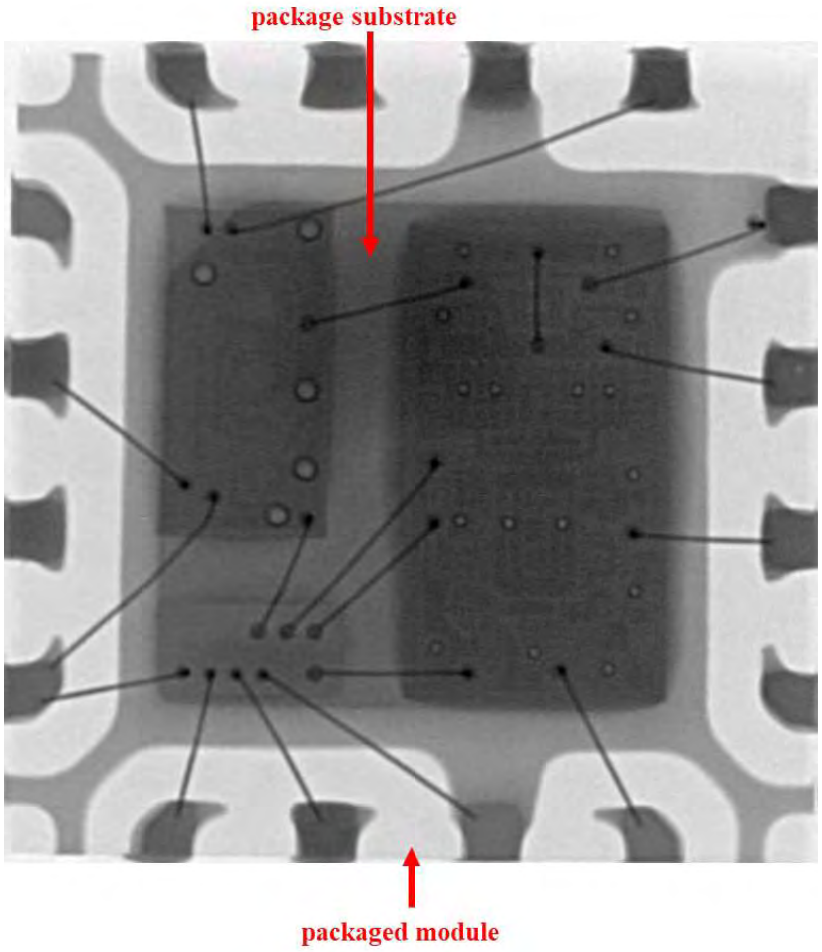
range. KCT8576HE integrates a high-efficiency, high-linearity power amplifier (PA), a low noise amplifier (LNA) with bypass ….”[2]

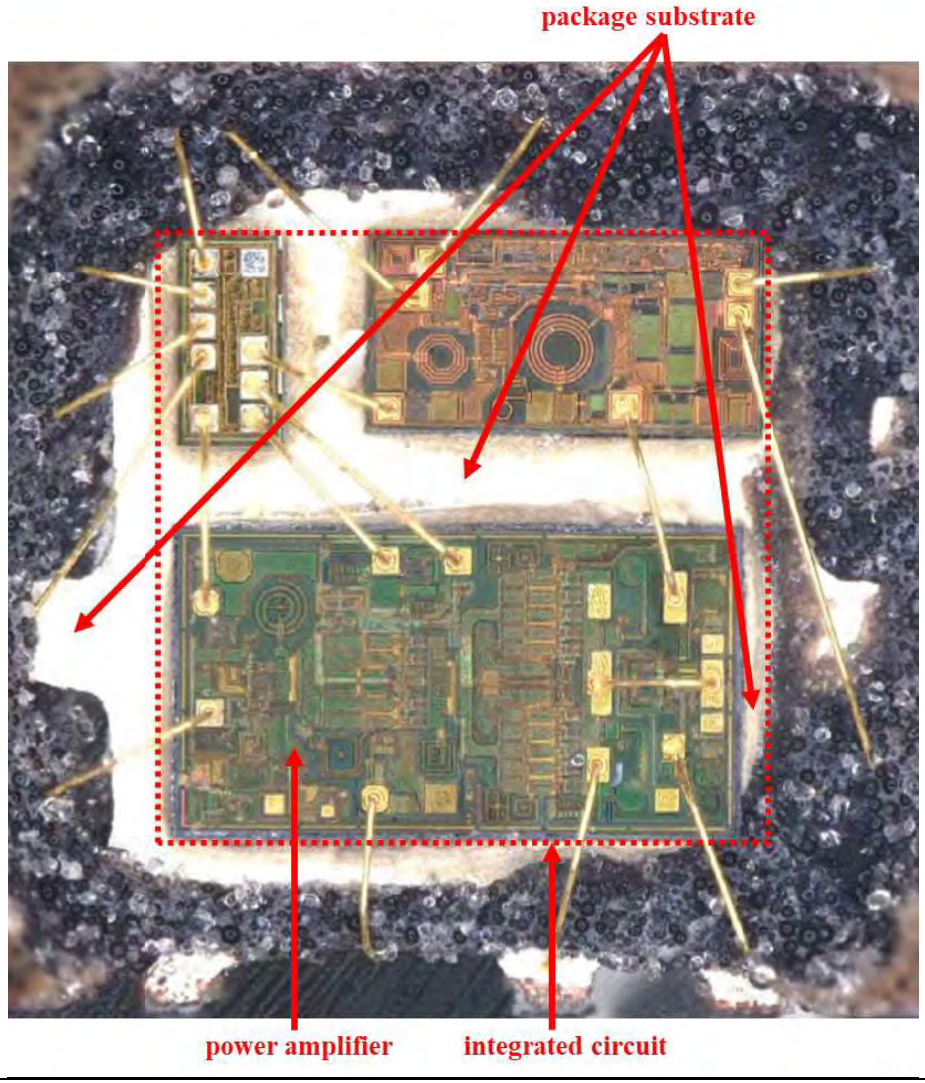
As another example, the image below of the KCT8576HE shows a packaged module (as indicated by the corresponding label below) for the KCT8576HE.



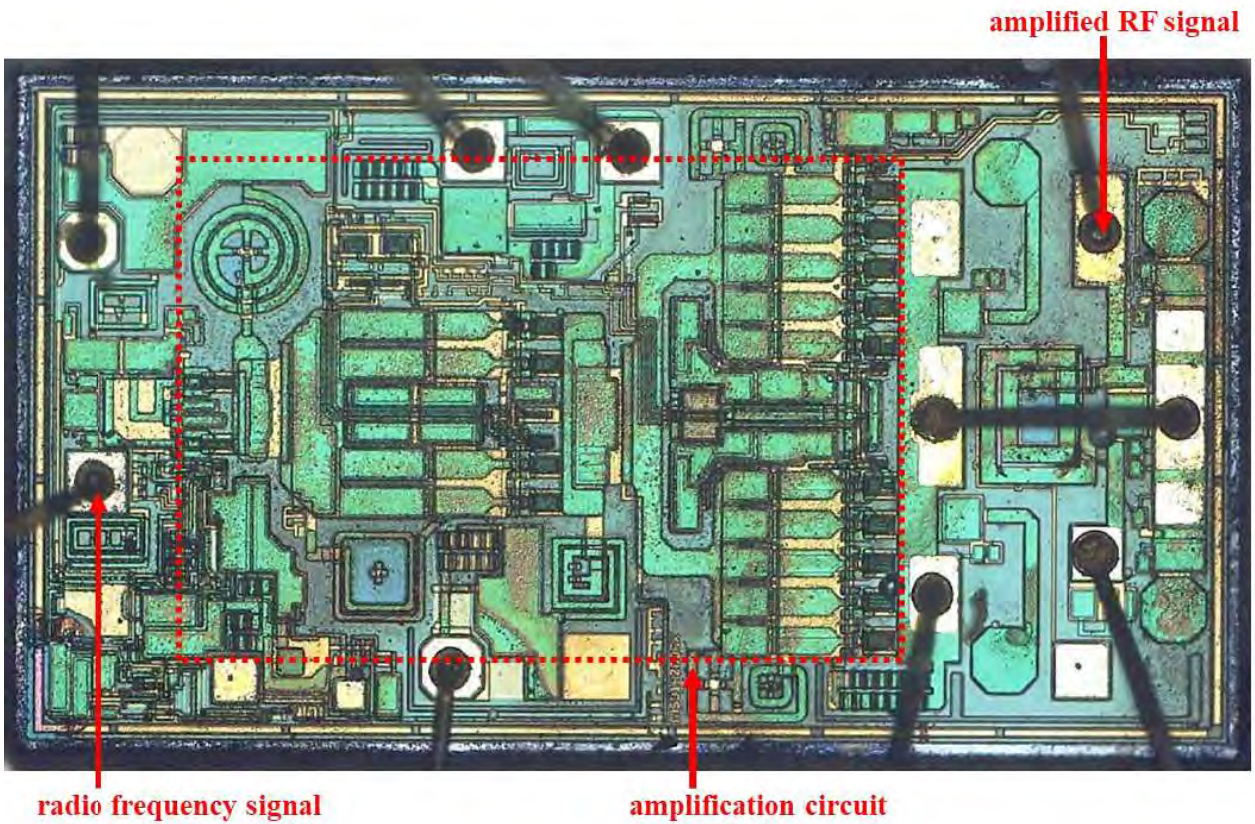
See, e.g., photo of KCT8576HE

[2] *See* https://perma.cc/N2ZN-83UW.

14[A] a package substrate; and	The KCT8576HE includes a package substrate. For example, the image of the KCT8576HE below shows a package substrate (as indicated by the corresponding label below) as part of the packaged module.  *See, e.g.*, photo of KCT8576HE
14[B] an integrated circuit attached to the	The KCT8576HE includes an integrated circuit attached to the package substrate and including a power amplifier.

package substrate and including a power amplifier configured to provide amplification to a radio frequency signal	For example, the image of the KCT8576HE below shows an integrated circuit (as indicated by the corresponding label below) attached to the package substrate and including a power amplifier (as indicated by the corresponding label below). 

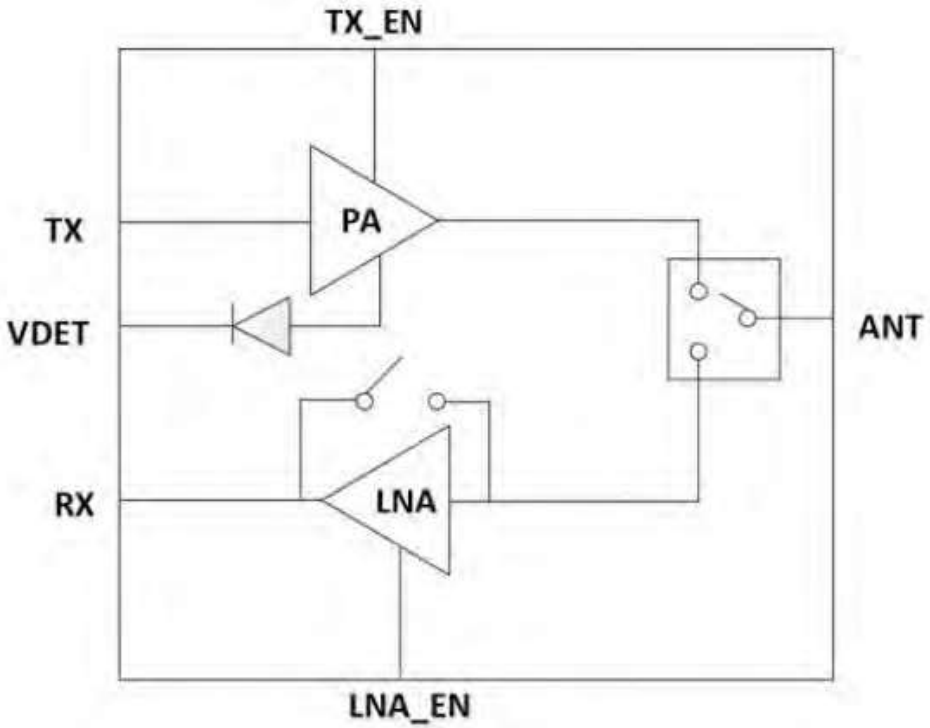
	See, e.g., photo of KCT8576HE showing an integrated circuit having three dies including a die for the power amplifier The power amplifier in the KCT8576HE is configured to provide amplification to a radio frequency signal. For example, the image below shows an enlarged view of the power amplifier die of the KCT8576HE. The power amplifier is coupled in such a way that it is configured to receive as an input a radio frequency (RF) signal, as labeled below as the radio frequency signal, and amplify the radio frequency signal to output an amplified RF signal, as labeled below. The dashed box with the corresponding label below is one example of an amplification circuit that provides the amplification of the radio frequency signal.

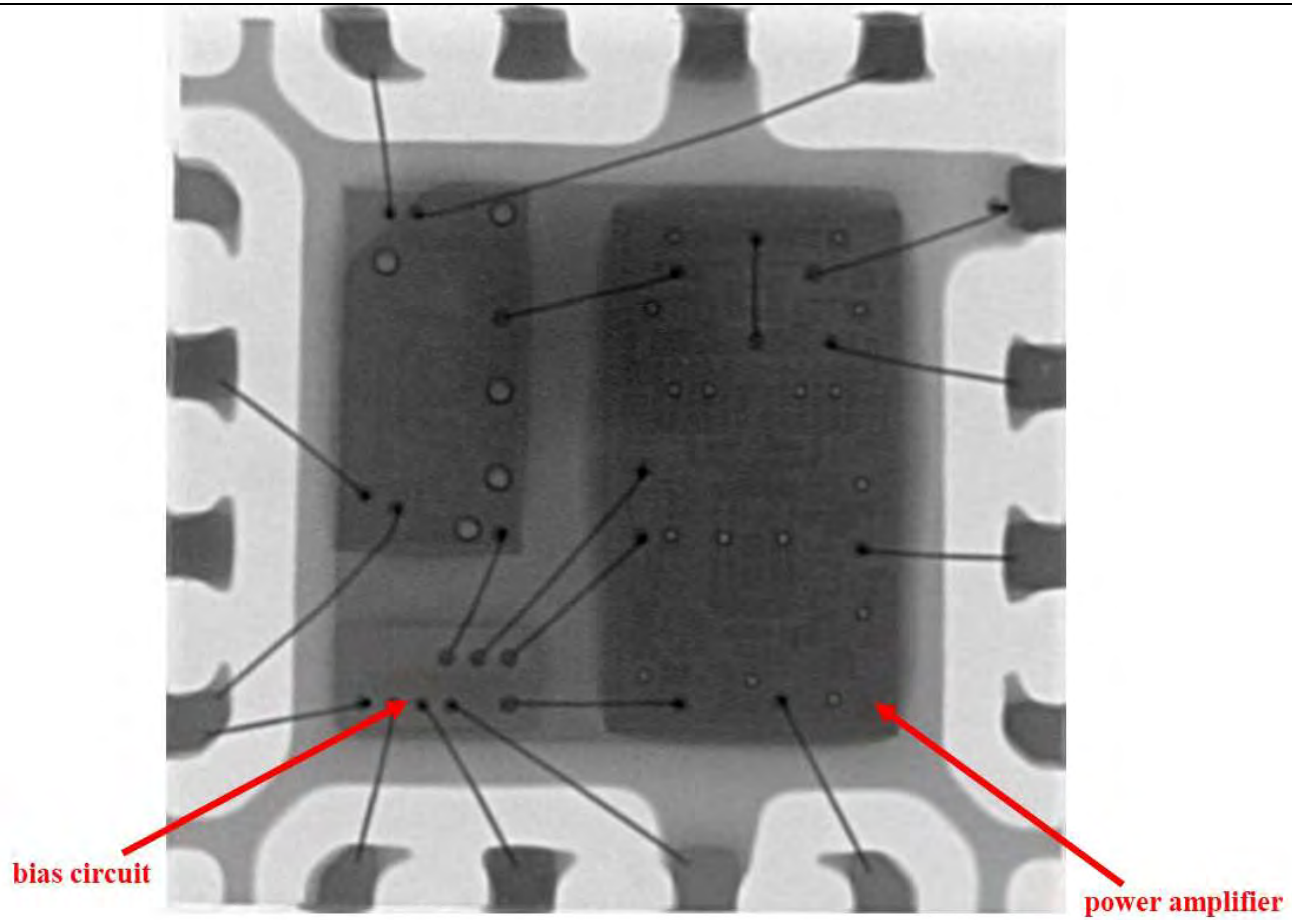


See, e.g., photo of the power amplifier die of KCT8576HE

As shown below in KCT's simplified block diagram for the KCT8576HE, a power amplifier (labelled as "PA") is part of the KCT8576HE product. Specifically, the KCT8576HE "integrates a high-efficiency, high-linearity power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated matching network, LO rejection, and harmonic filters all in one device."[3]

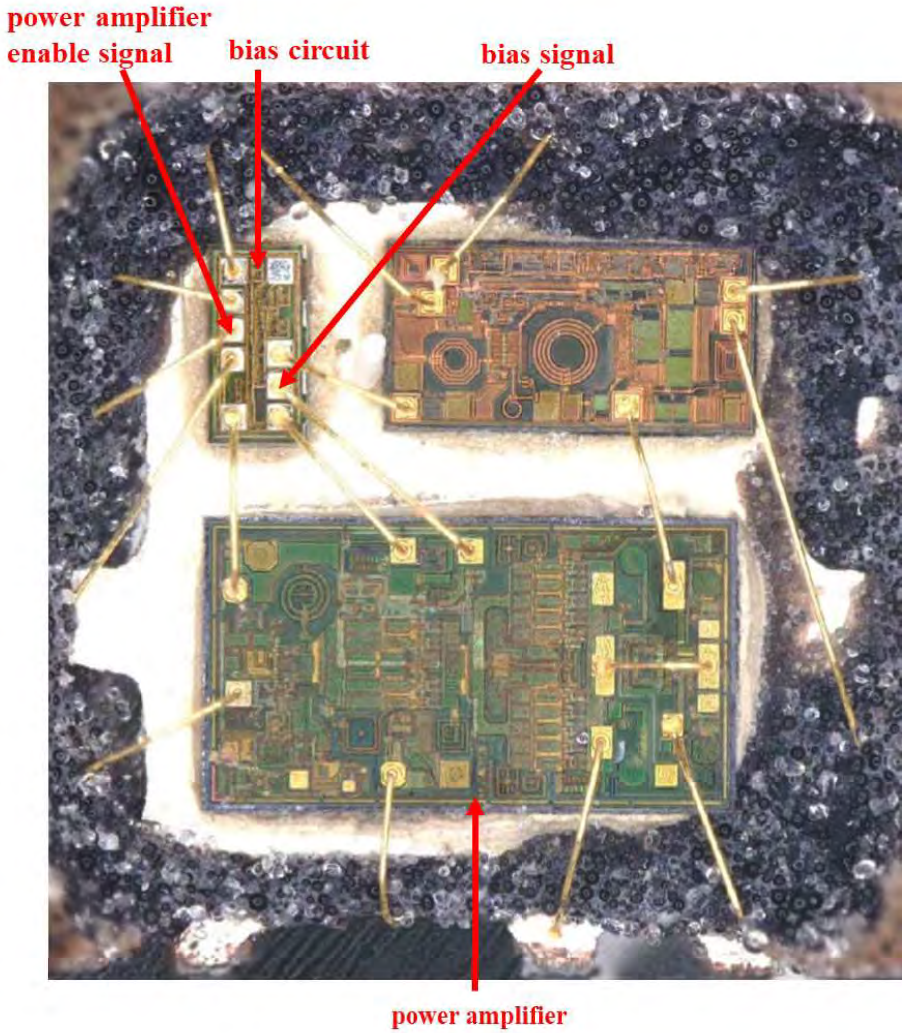
[3] *See* https://perma.cc/N2ZN-83UW.

	 *See, e.g.*, simplified block diagram for KCT8576HE
14[C] and a bias circuit configured to receive a power amplifier enable signal and to generate a bias signal that biases the power amplifier,	The KCT8576HE includes a bias circuit configured to receive a power amplifier enable signal and to generate a bias signal that biases the power amplifier. For example, the image of the KCT8576HE below shows a bias circuit and the power amplifier (as indicated by the corresponding labels, respectively).



See, e.g., photo of KCT8576HE showing three dies, including a die for the bias circuit and a die for the power amplifier

As another example, the image of the KCT8576HE below shows the bias circuit and the power amplifier (as indicated by the corresponding labels, respectively).

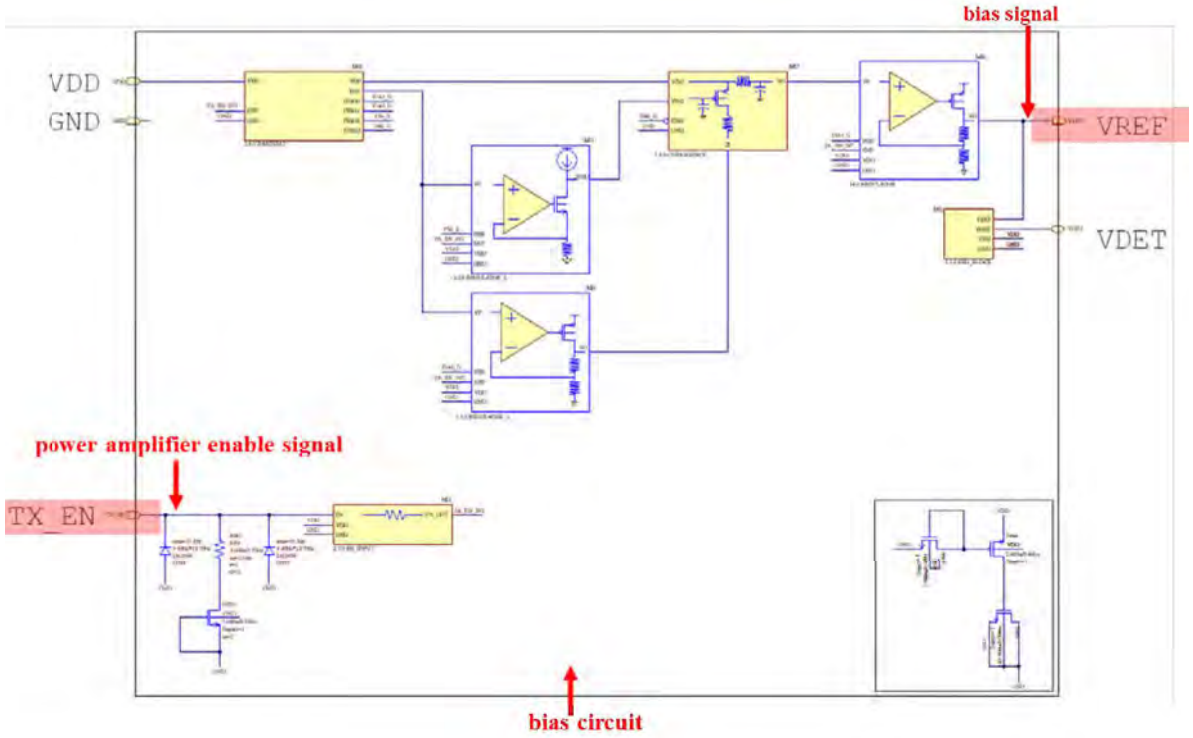


See, e.g., photo of KCT8576HE showing three dies, including a die for the bias circuit and a die for the power amplifier

The bias circuit is coupled to the packaged module's interface through a wire bond in such a way that the bias circuit is configured to receive a power amplifier enable signal (as indicated by the corresponding label

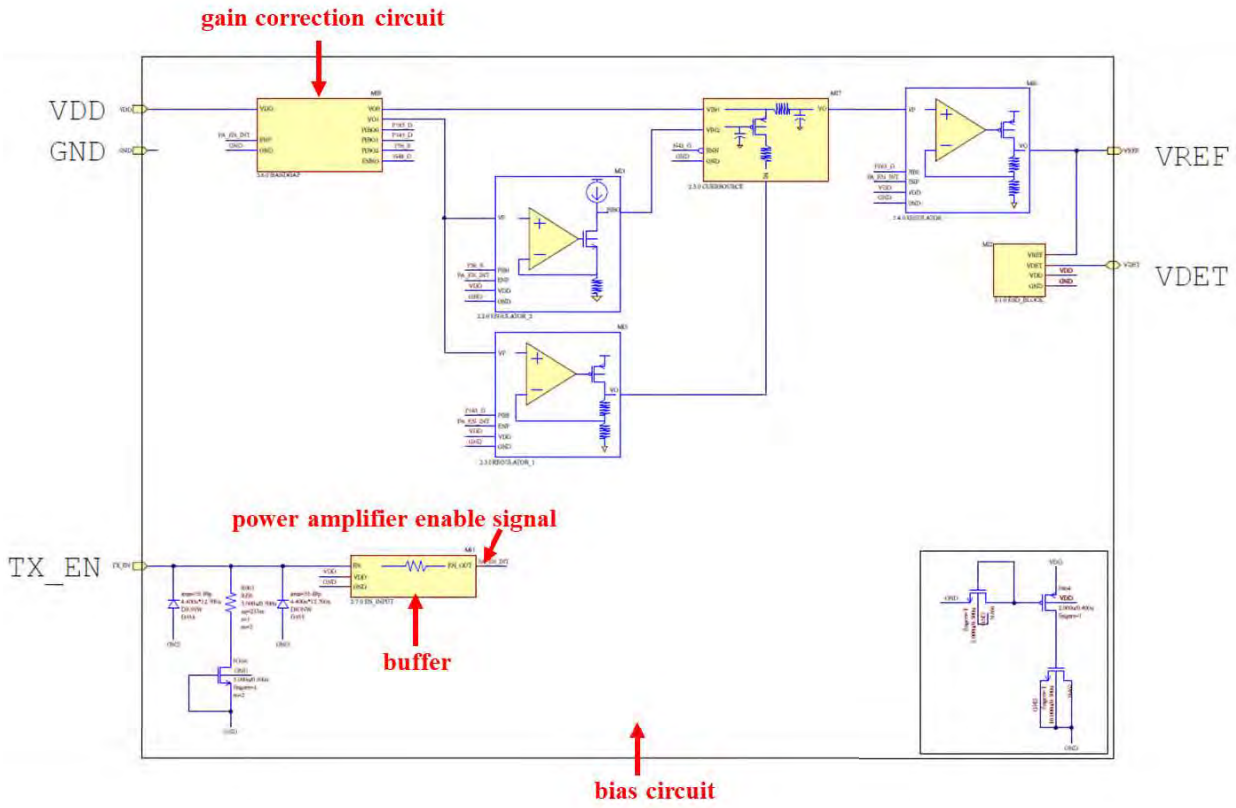
above). The bias circuit is coupled to the power amplifier by a wire bond in such a way that the bias circuit is configured to generate a bias signal (as indicated by the corresponding label above) that biases the power amplifier.

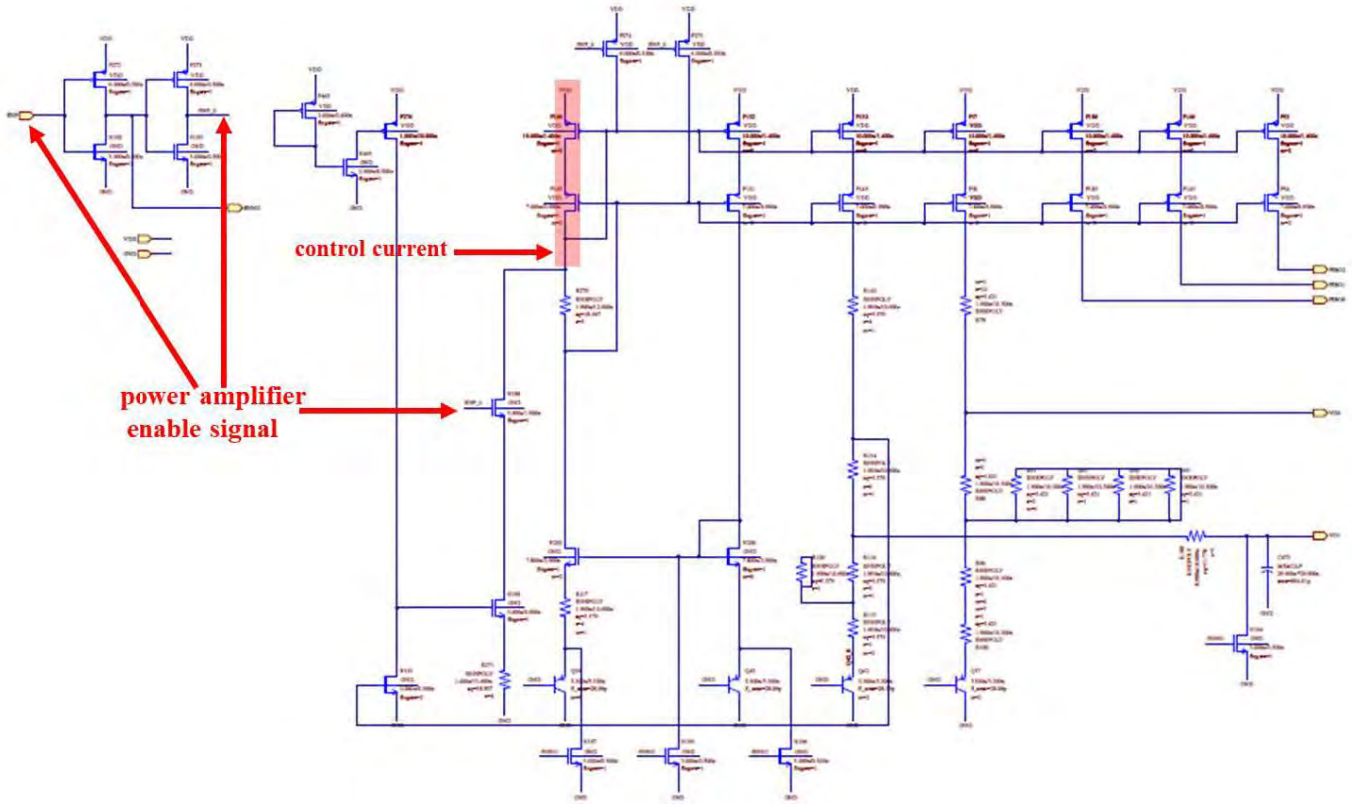
The reverse engineered schematic below is for the bias circuit (as indicated by the corresponding label below) in the KCT8576HE. As highlighted below, the bias circuit includes a "TX_EN" port configured to receive the power amplifier enable signal and a "VREF" port configured to output the bias signal that biases the power amplifier.



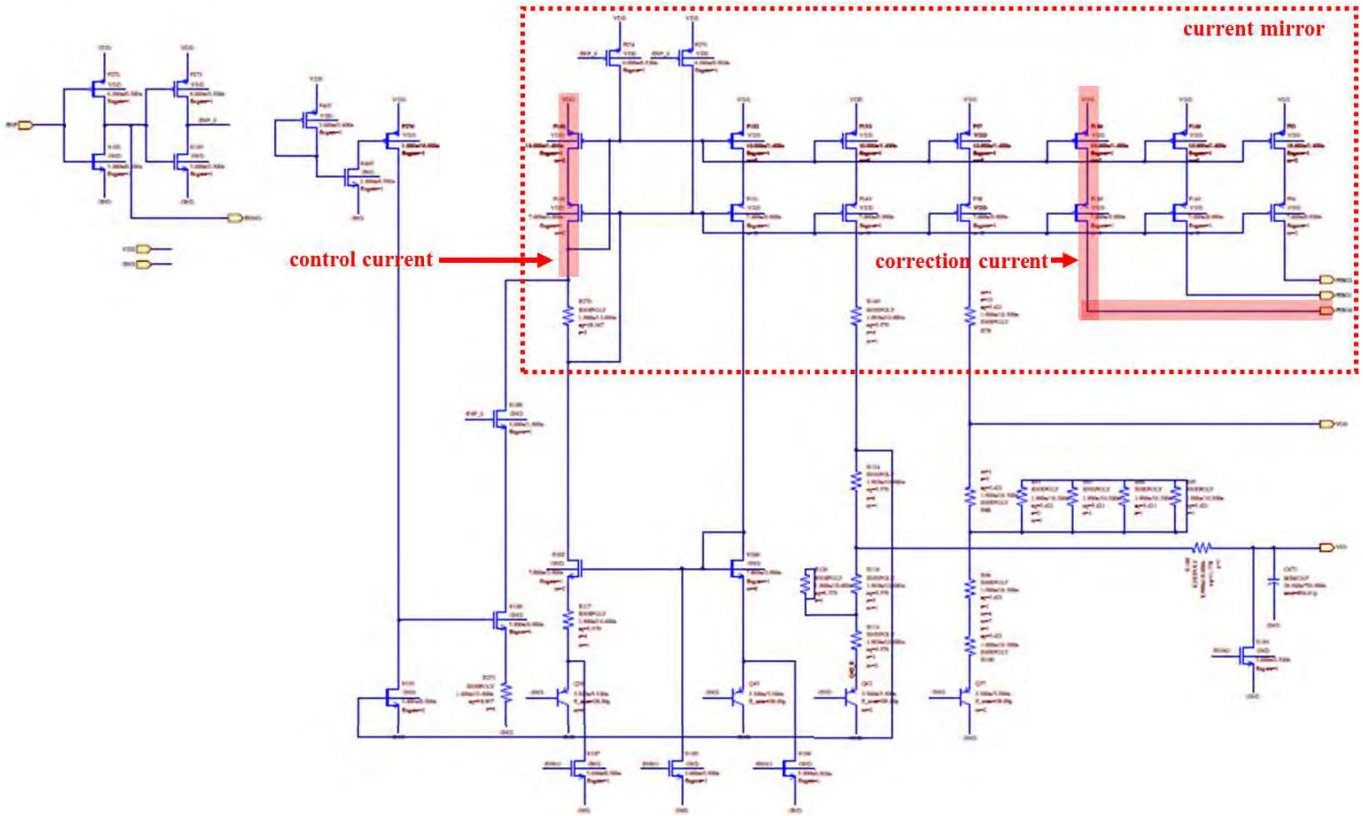
See, e.g., reverse engineered schematic of the bias circuit of KCT8576HE

See also elements 14[D] through 14[F] (showing details of the bias circuit).

14[D] the bias circuit including a gain correction circuit configured to generate a control current in response to activation of the power amplifier enable signal,	The KCT8576HE includes the bias circuit including a gain correction circuit configured to generate a control current in response to activation of the power amplifier enable signal. For example, the reverse engineered schematic below for the bias circuit in the KCT8576HE shows that the bias circuit includes a gain correction circuit (as indicated by the corresponding label below).  *See, e.g.*, reverse engineered schematic of the bias circuit of KCT8576HE The reverse engineered schematic below for the KCT8576HE shows the internal details of the gain correction circuit set forth above. The gain correction circuit receives the power amplifier enable signal (as indicated by the corresponding label below). The power amplifier enable signal is coupled in a way such

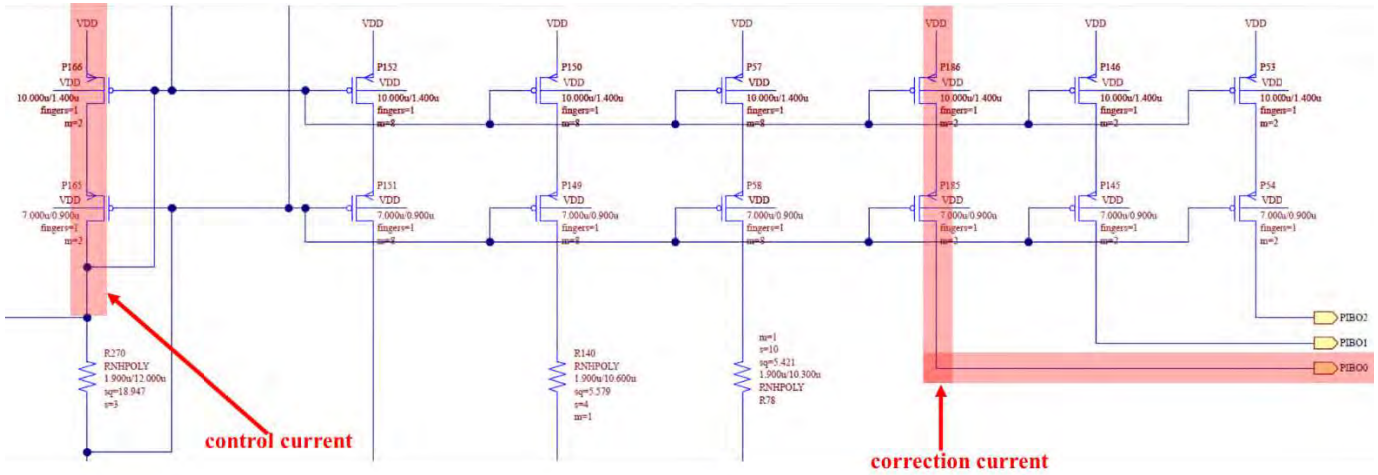
	that the gain correction circuit is configured to generate the control current (as indicated by the corresponding label below) in response to activation of the power amplifier enable signal.  *See, e.g.*, reverse engineered schematic of the gain correction circuit of KCT8576HE
14[E] and to mirror the control current to generate a correction current,	In the KCT8576HE, the bias circuit and its gain correction circuit mirrors the control current to generate a correction current. For example, as shown by the reverse engineered schematic below for the gain correction circuit of the KCT8576HE, the gain correction circuit includes a current mirror (as indicated by the corresponding label

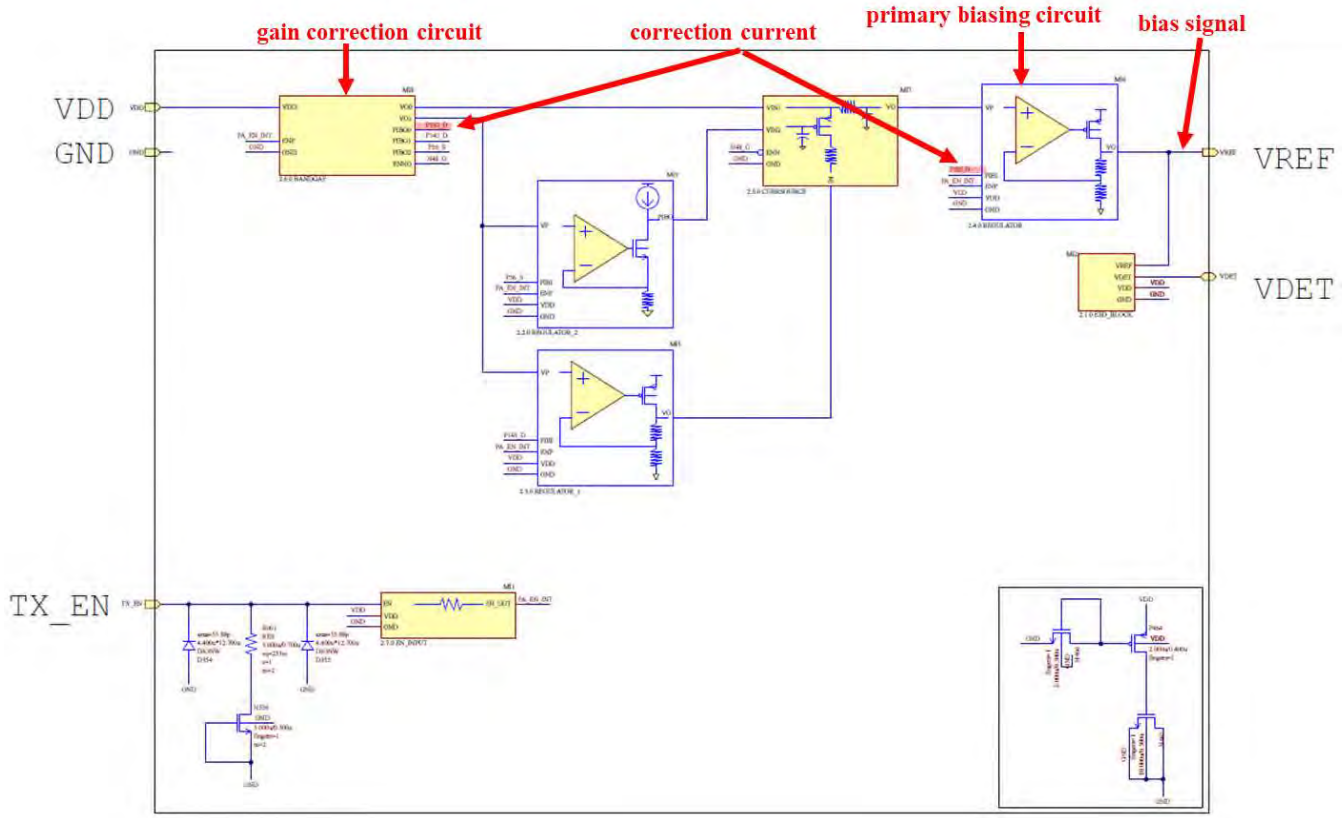
below). The current mirror is configured to mirror the control current to generate the correction current (as indicated by the corresponding label below). The dashed box with the label below is one example of a current mirror that mirrors the control current to generate the correction current.



See, e.g., reverse engineered schematic of the gain correction circuit of KCT8576HE

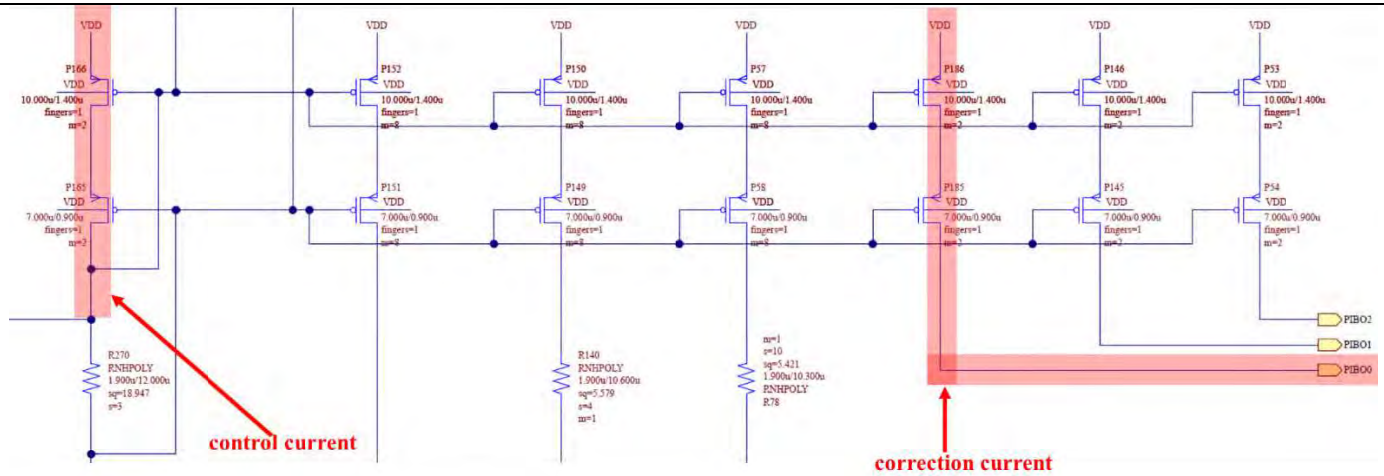
The schematic below for the KCT8576HE is an enlarged view of a portion of the current mirror identified above, which is configured to mirror the control current to generate the correction current. As set forth in the '563 patent, a current mirror can have any suitable gain when mirroring a current. *See* '563 patent, 11:63-12:2. For example, the current mirror in KCT8576HE is configured to mirror the control current by a

	factor of about 1, based on the multiple numbers designated in the schematic below (e.g., "m=2" for the control current and "m=2" for the correction current).  *See, e.g.*, enlarged portion of reverse engineered schematic of the gain correction circuit of KCT8576HE
14[F] and a primary biasing circuit configured to generate the bias signal based on the correction current and the power amplifier enable signal.	In the KCT8576HE, the bias circuit includes a primary biasing circuit configured to generate the bias signal based on the correction current and the power amplifier enable signal. For example, as shown in the reverse engineered schematic for the KCT8576HE below, a primary biasing circuit (as indicated by the corresponding label below) is configured to generate the bias signal (as indicated by the corresponding label below) for the power amplifier based on the correction current and the power amplifier enable signal.

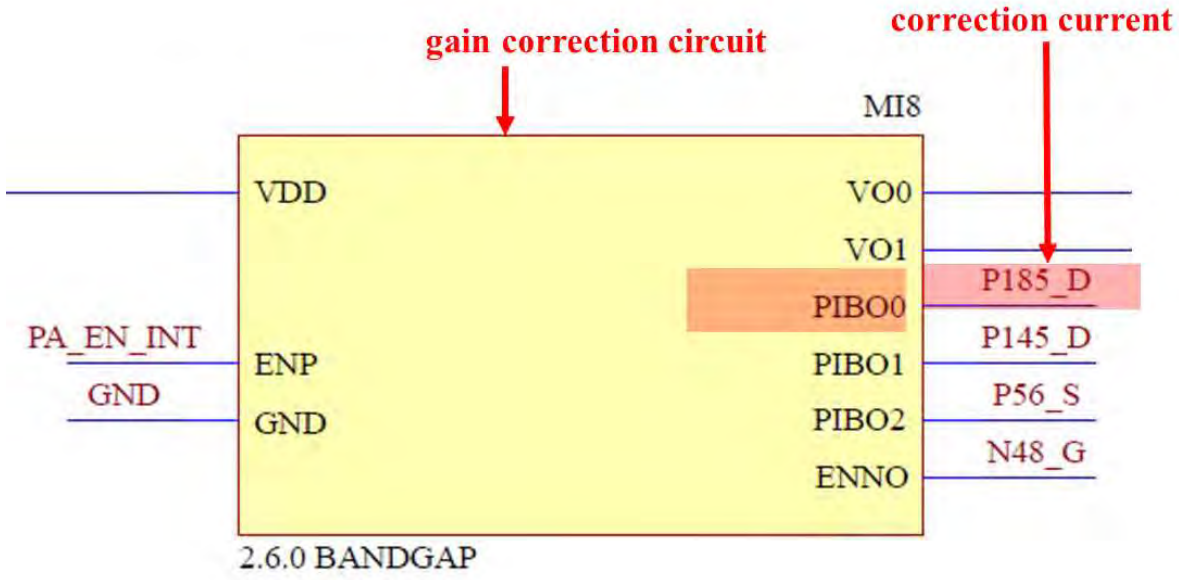


See, e.g., reverse engineered schematic of the bias circuit of KCT8576HE

The correction current is output by the "PIBO0" port of the gain correction circuit, as shown by the reverse engineered schematics below.

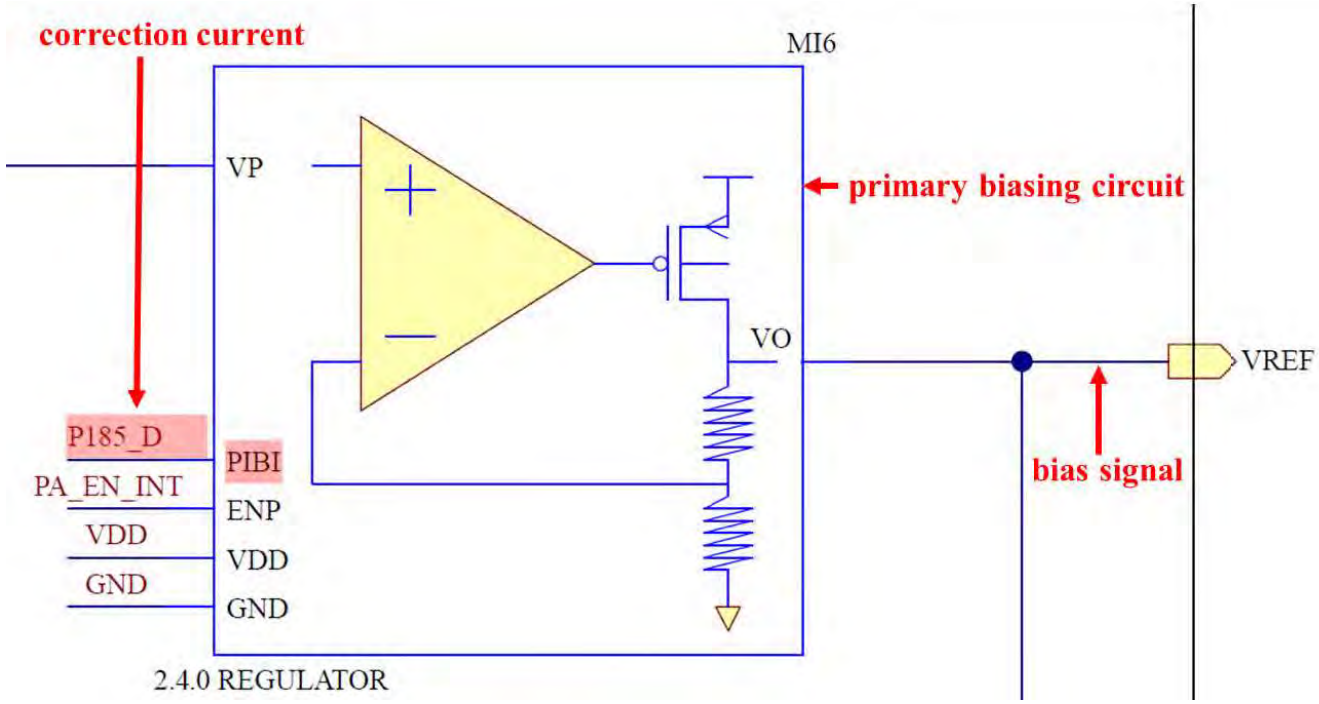


See, e.g., enlarged portion of reverse engineered schematic of the gain correction circuit of KCT8576HE



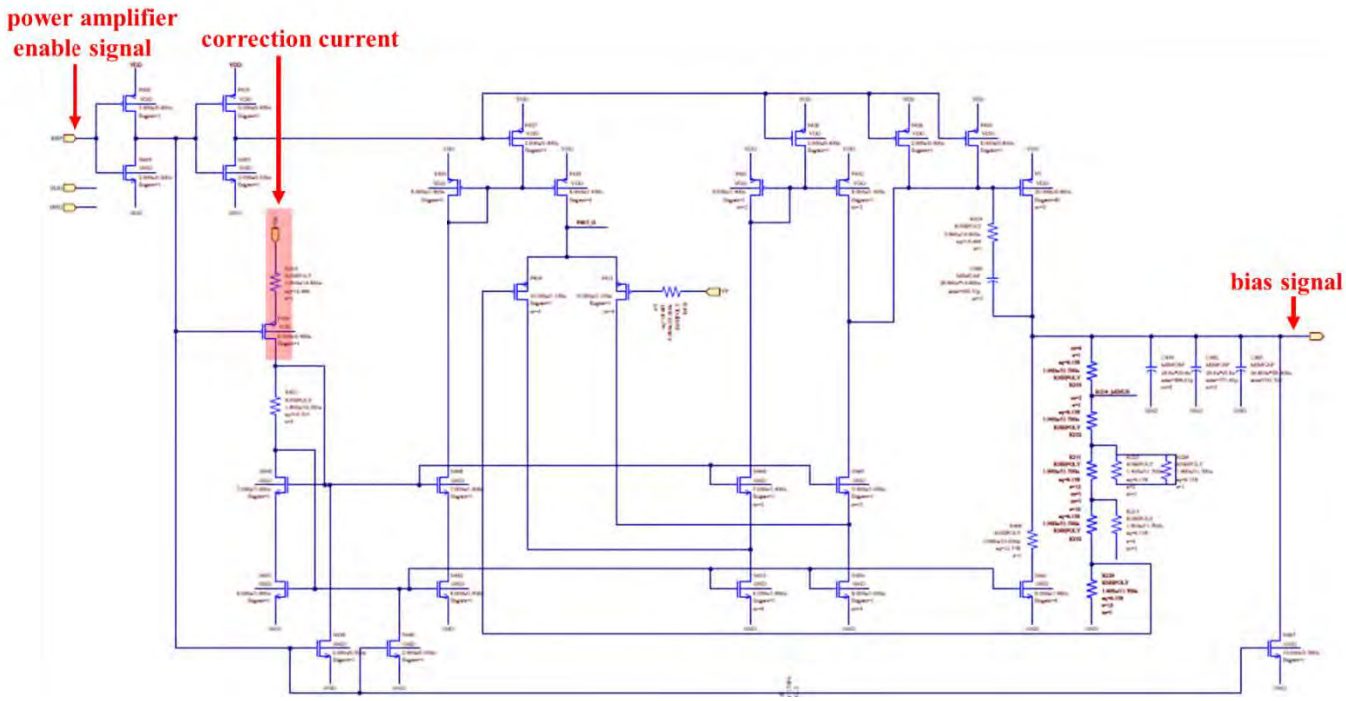
See, e.g., enlarged portion of reverse engineered schematic of the bias circuit of KCT8576HE

The "PIBO0" port of the gain correction circuit (shown above and as corresponding to P185_D) is connected to the "PIBI" port of the primary biasing circuit (as indicated by the corresponding label below showing P185_D connecting to PIBI), as shown by the schematic below.



See, e.g., enlarged portion of reverse engineered schematic of the bias circuit of KCT8576HE

As shown by the schematic below for the primary biasing circuit of the KCT8576HE, the primary biasing circuit takes in the correction current (as indicated by the corresponding label below) as an input and the power amplifier enable signal (as indicated by the corresponding label below) as another input so that the primary biasing circuit is configured to generate the bias signal based on the correction current and the power amplifier enable signal.



See, e.g., reverse engineered schematic of the primary biasing circuit of KCT8576HE

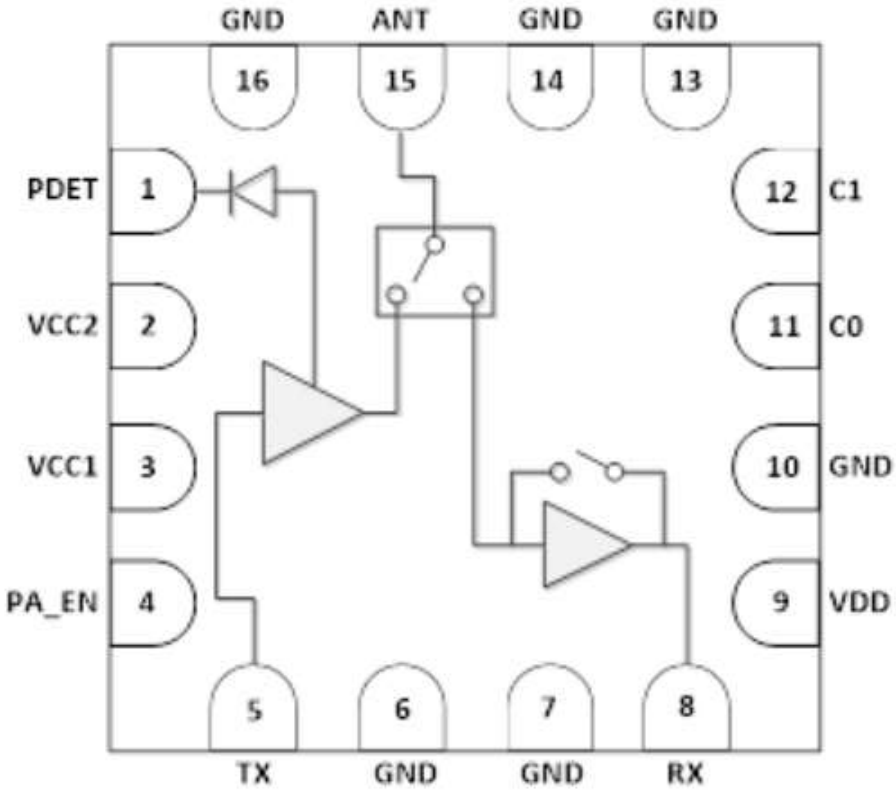
EXHIBIT 19

EXHIBIT 19
SKYWORKS SOLUTIONS, INC.'S INFRINGEMENT CHART
KCT8239S
U.S. Patent No. 9,917,563
Independent Claim 14

Skyworks Solutions, Inc. ("Skyworks") provides this exemplary claim chart for independent claim 14 of U.S. Patent No. 9,917,563 (the "'563 patent") applied to Kangxi Communication Technologies (Shanghai) Co., Ltd's and Grand Chip Labs, Inc.'s (collectively, "KCT") KCT8239S product. The disclosures in this claim chart directed to the KCT8239S are also more broadly directed to any sale, offer for sale, use, or importation of the KCT8239S in the U.S., including in an end product such as a wireless router or as a standalone product that is not incorporated in an end product.

The claim chart below demonstrates infringement by comparing each element of the charted claim to corresponding components, aspects, and/or features of the KCT8239S product. This claim chart is not intended to constitute an expert report on infringement. This claim chart includes information provided by way of example, and not by way of limitation.

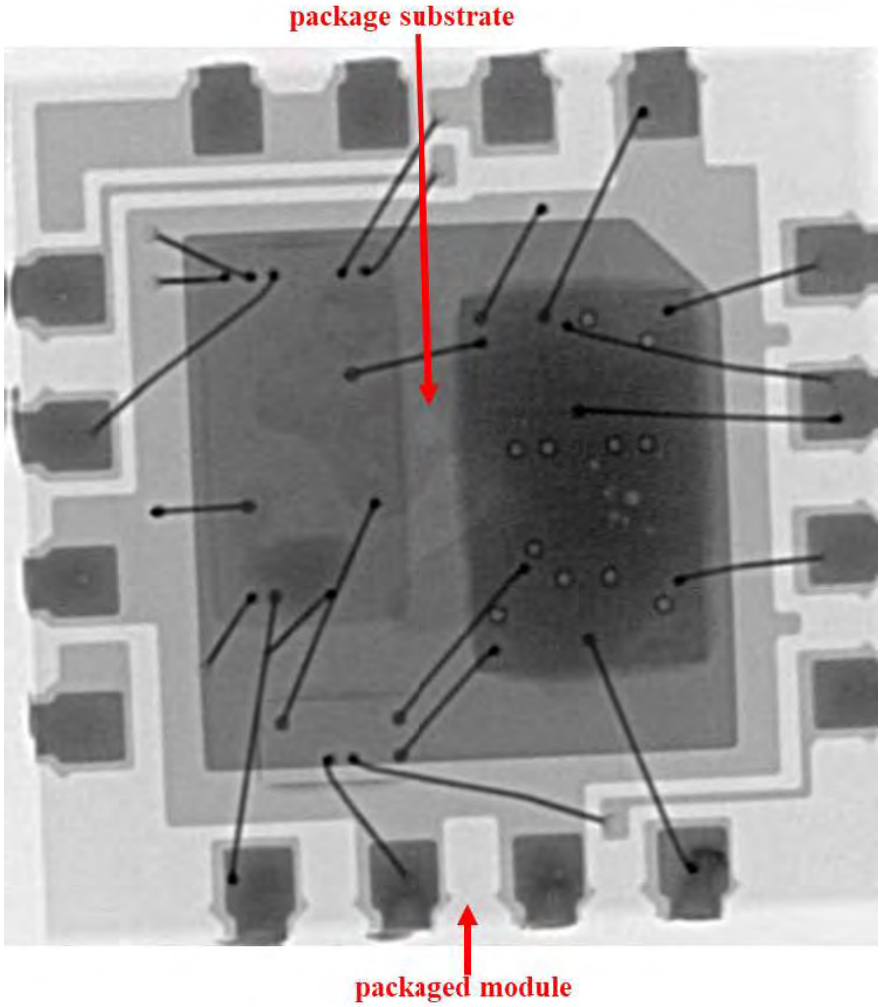
The analysis set forth below is based only upon information from publicly available sources regarding the KCT8239S product. Further analysis of non-public information during fact discovery will likely assist in identifying all infringing features and functionalities used by KCT in the KCT8239S product. Accordingly, Skyworks reserves the right to supplement this infringement analysis once such information is made available to Skyworks. Further, Skyworks reserves the right to supplement this infringement analysis, as appropriate, upon issuance of an order construing any terms recited in the asserted claims or as other circumstances so merit.

Claim	KCT8239S
14 [pre] A packaged module comprising:	To the extent the preamble of claim 1 is limiting, the KCT8239S includes a packaged module. The KCT8239S is a module for Wi-Fi connectivity. For example, the following image for the KCT8239S is a simplified block diagram for this product.[1]  *See, e.g.*, simplified block diagram for KCT8239S

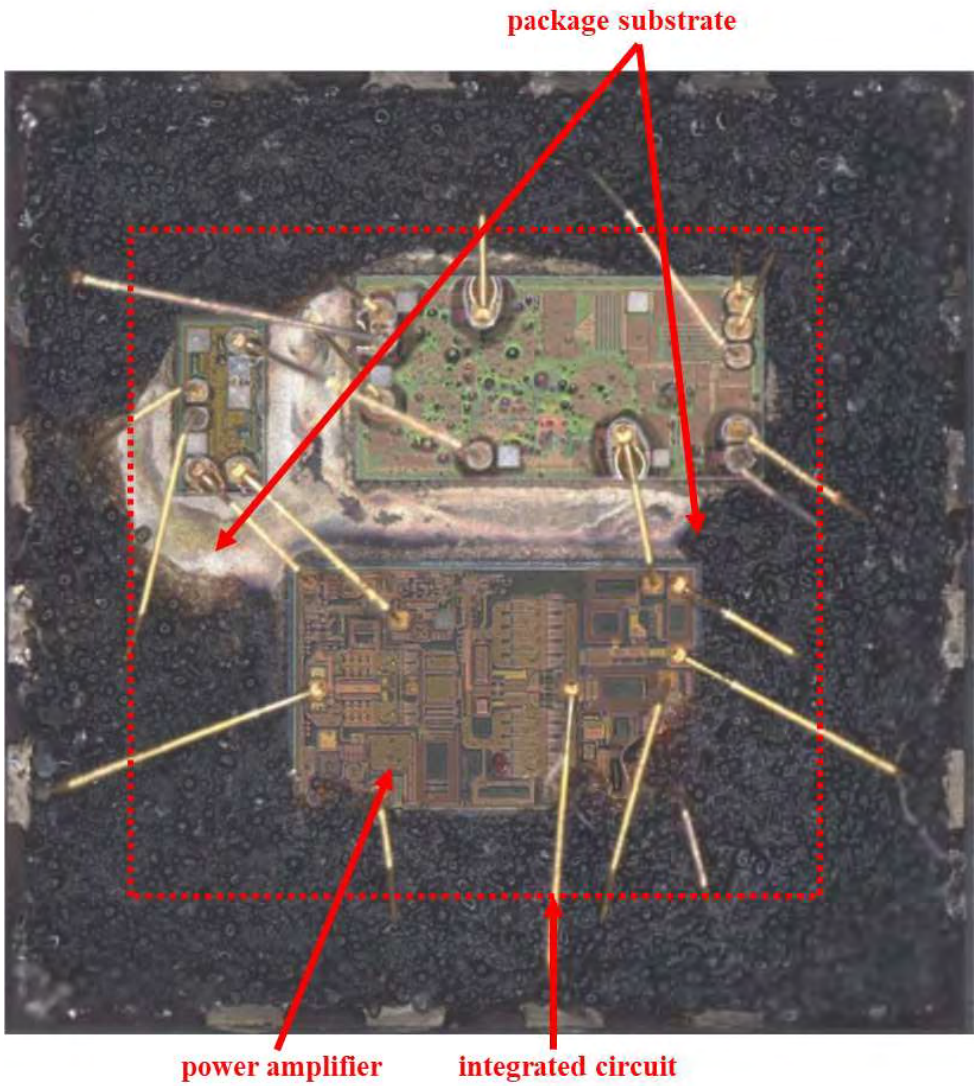
[1] *See* https://perma.cc/NS2E-VPYU.

	The KCT8239S is, according to KCT, "a fully integrated 802.11b/g/n/ac/ax WLAN RF Front-end module (FEM) which incorporates key RF functionality. It is integrated with a high-efficiency power amplifier (PA), a low noise amplifier (LNA) with bypass …."[2] As another example, the image below of the KCT8239S shows a packaged module (as indicated by the corresponding label below) for the KCT8239S.  *See, e.g.*, photo of KCT8239S

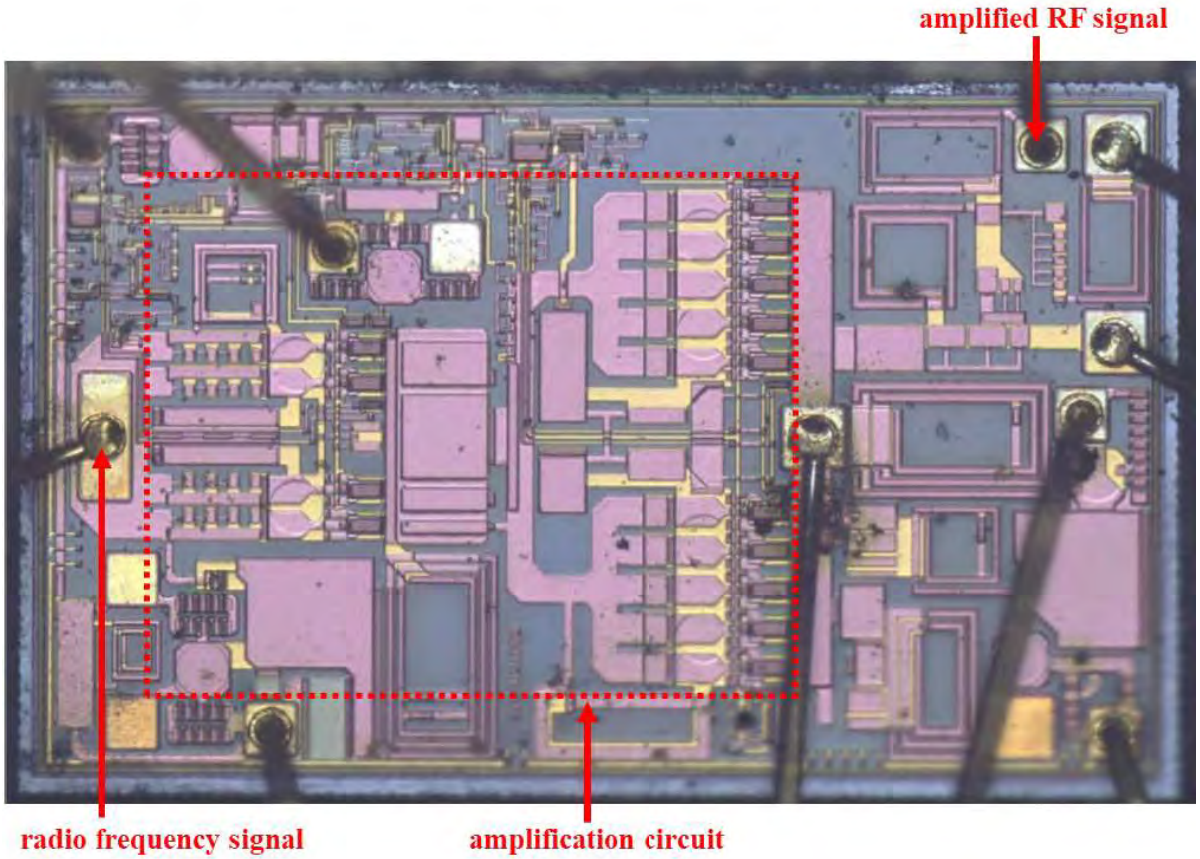
[2] *See* https://perma.cc/NS2E-VPYU.

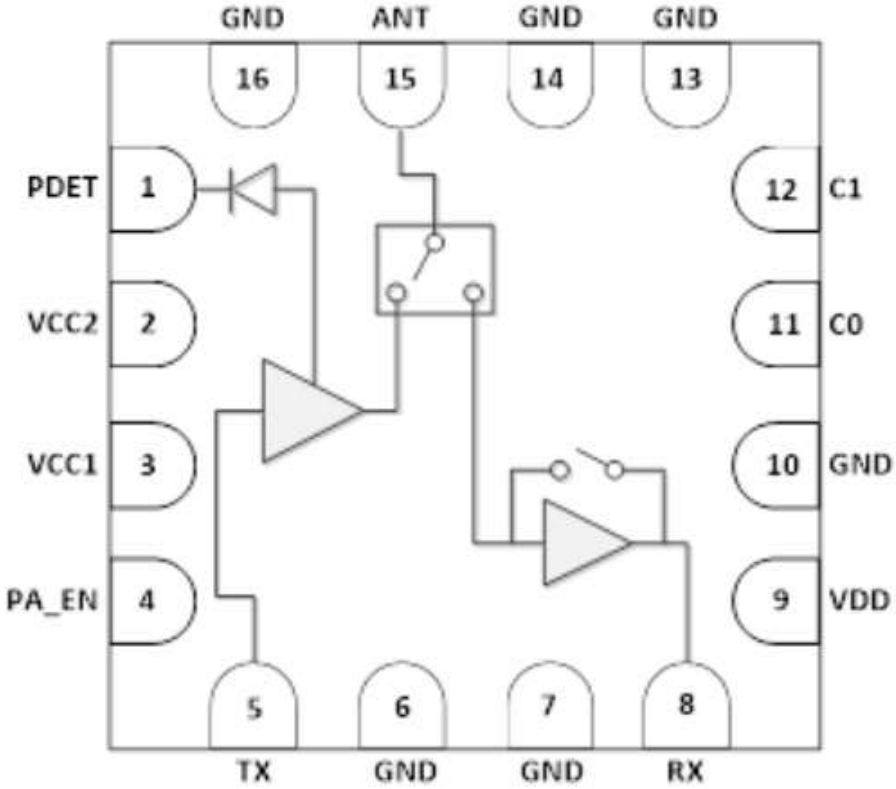
14[A] a package substrate; and	The KCT8239S includes a package substrate. For example, the image of the KCT8239S below shows a package substrate (as indicated by the corresponding label below) as part of the packaged module.  *See, e.g.*, photo of KCT8239S

14[B] an integrated circuit attached to the package substrate and including a power amplifier configured to provide amplification to a radio frequency signal	The KCT8239S includes an integrated circuit attached to the package substrate and including a power amplifier. For example, the image of the KCT8239S below shows an integrated circuit (as indicated by the corresponding label below) attached to the package substrate and including a power amplifier (as indicated by the corresponding label below).

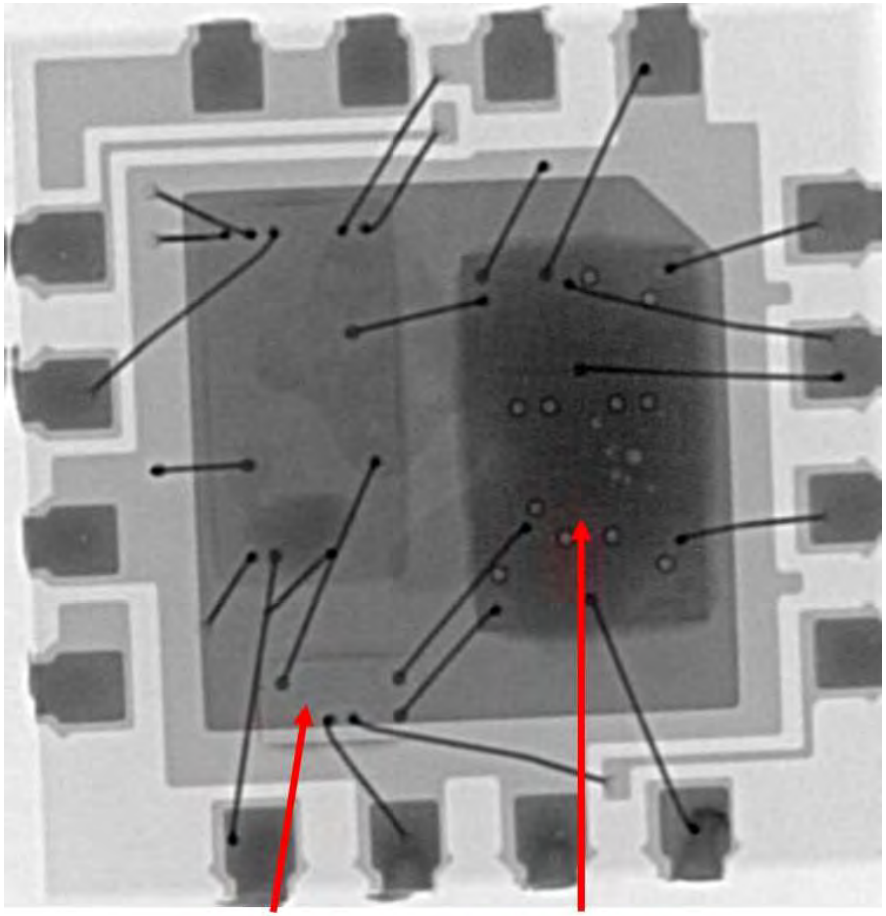


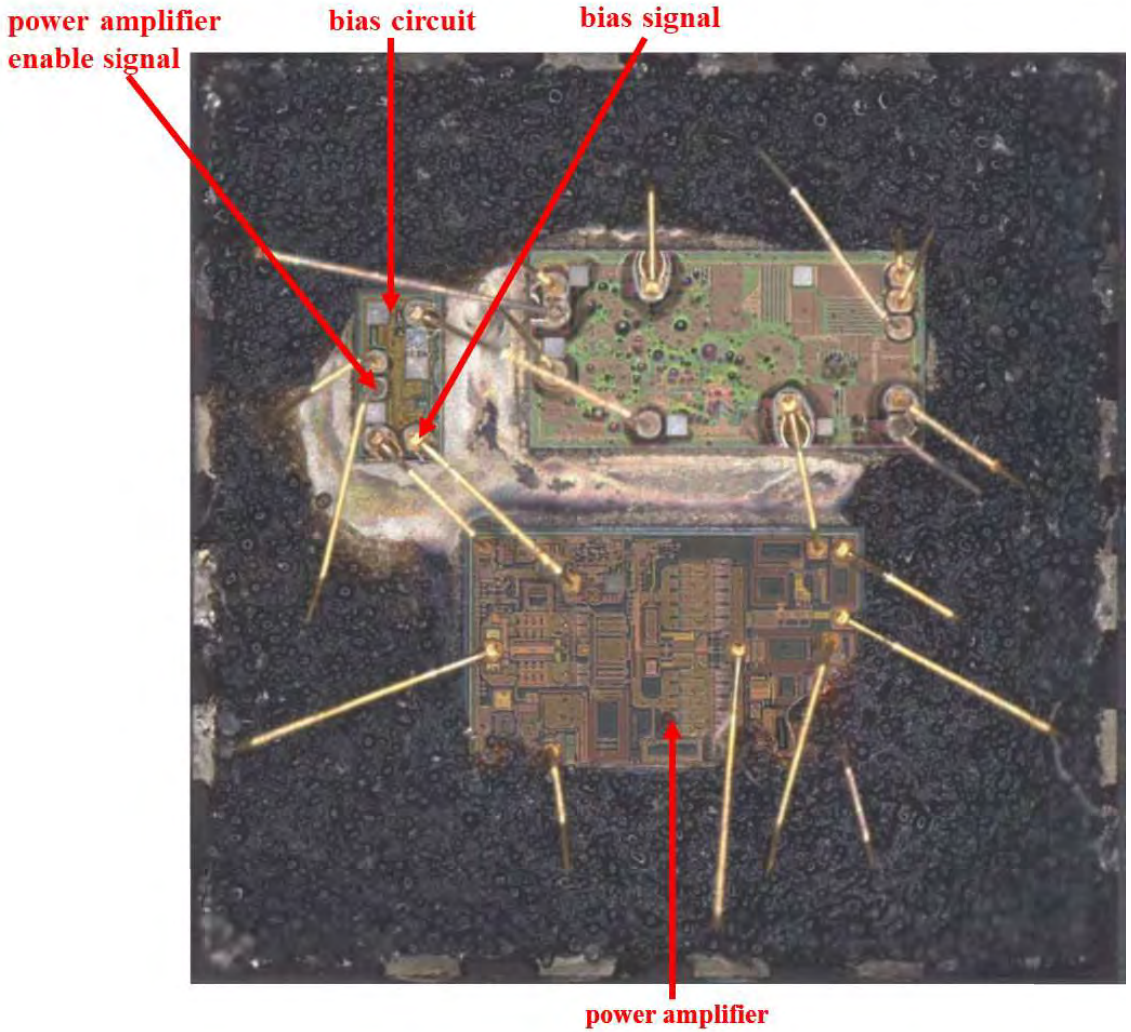
See, e.g., photo of KCT8239S showing an integrated circuit having three dies including a die for the power amplifier

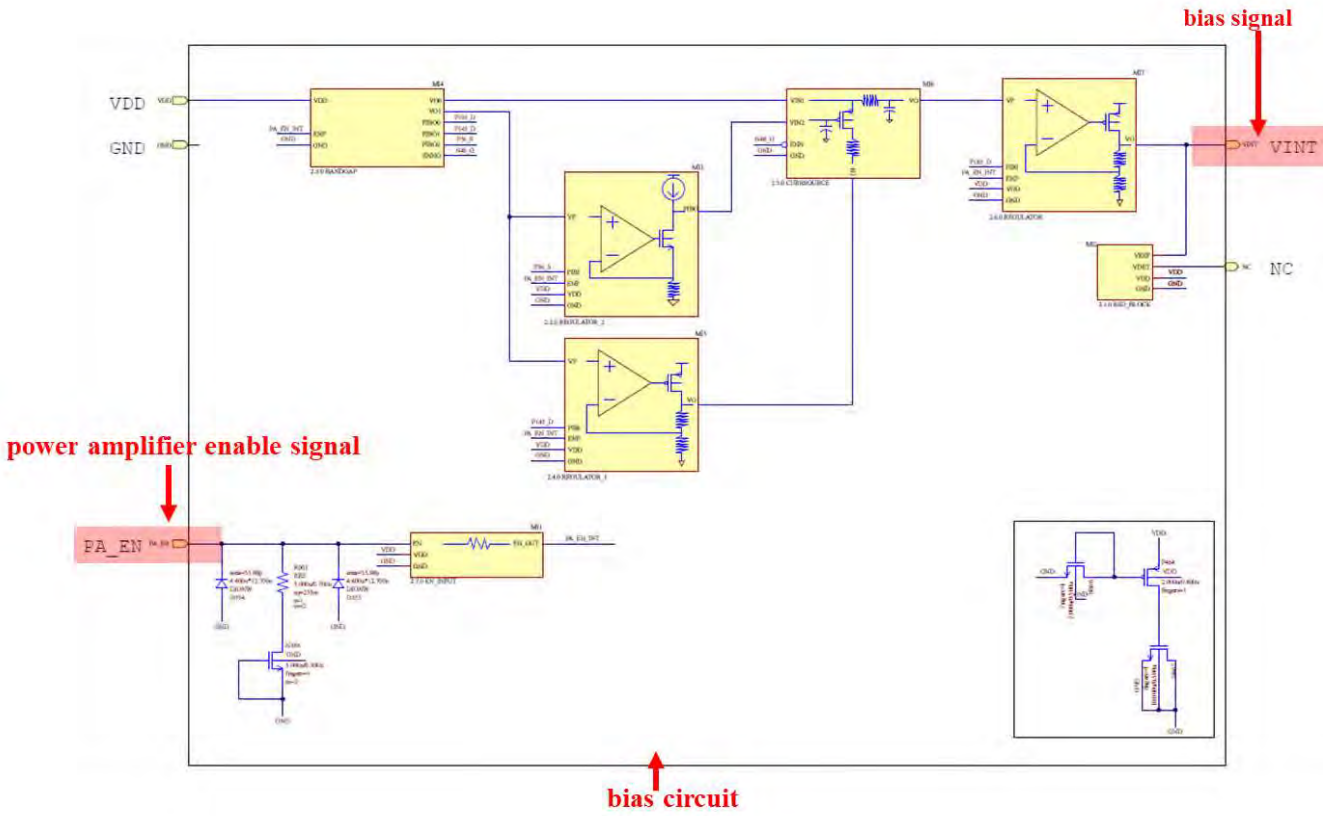
	The power amplifier in the KCT8239S is configured to provide amplification to a radio frequency signal. For example, the image below shows an enlarged view of the power amplifier die of the KCT8239S. The power amplifier is coupled in such a way that it is configured to receive as an input a radio frequency (RF) signal, as labeled below as the radio frequency signal, and amplify the radio frequency signal to output an amplified RF signal, as labeled below. The dashed box with the corresponding label below is one example of an amplification circuit that provides the amplification of the radio frequency signal.  *See, e.g.*, photo of the power amplifier die of KCT8239S

	As shown below in KCT's simplified block diagram for the KCT8239S, a power amplifier is part of the KCT8239S product. Specifically, the KCT8239S "is integrated with a high-efficiency power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated matching network and a single-pole, double-throw (SPDT) switch all in one device."[3]  *See, e.g.*, simplified block diagram for KCT8239S
14[C] and a bias circuit configured to receive a power	The KCT8239S includes a bias circuit configured to receive a power amplifier enable signal and to generate a bias signal that biases the power amplifier.

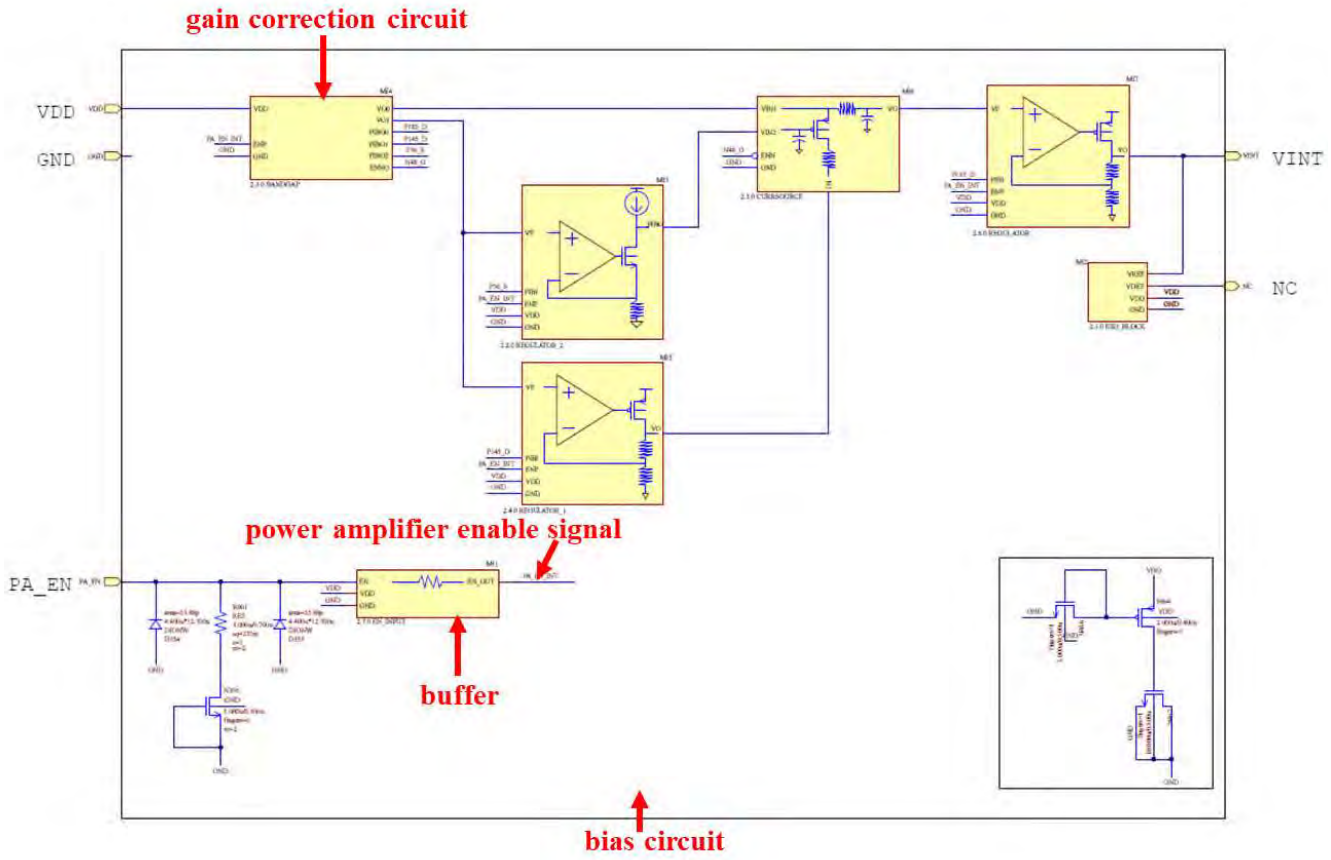
[3] *See* https://perma.cc/NS2E-VPYU.

amplifier enable signal and to generate a bias signal that biases the power amplifier,	For example, the image of the KCT8239S below shows a bias circuit and the power amplifier (as indicated by the corresponding labels, respectively).  *See, e.g.*, photo of KCT8239S showing three dies, including a die for the bias circuit and a die for the power amplifier

	As another example, the image of the KCT8239S below shows the bias circuit and the power amplifier (as indicated by the corresponding labels, respectively).  *See, e.g.*, photo of KCT8239S showing three dies, including a die for the bias circuit and a die for the power amplifier

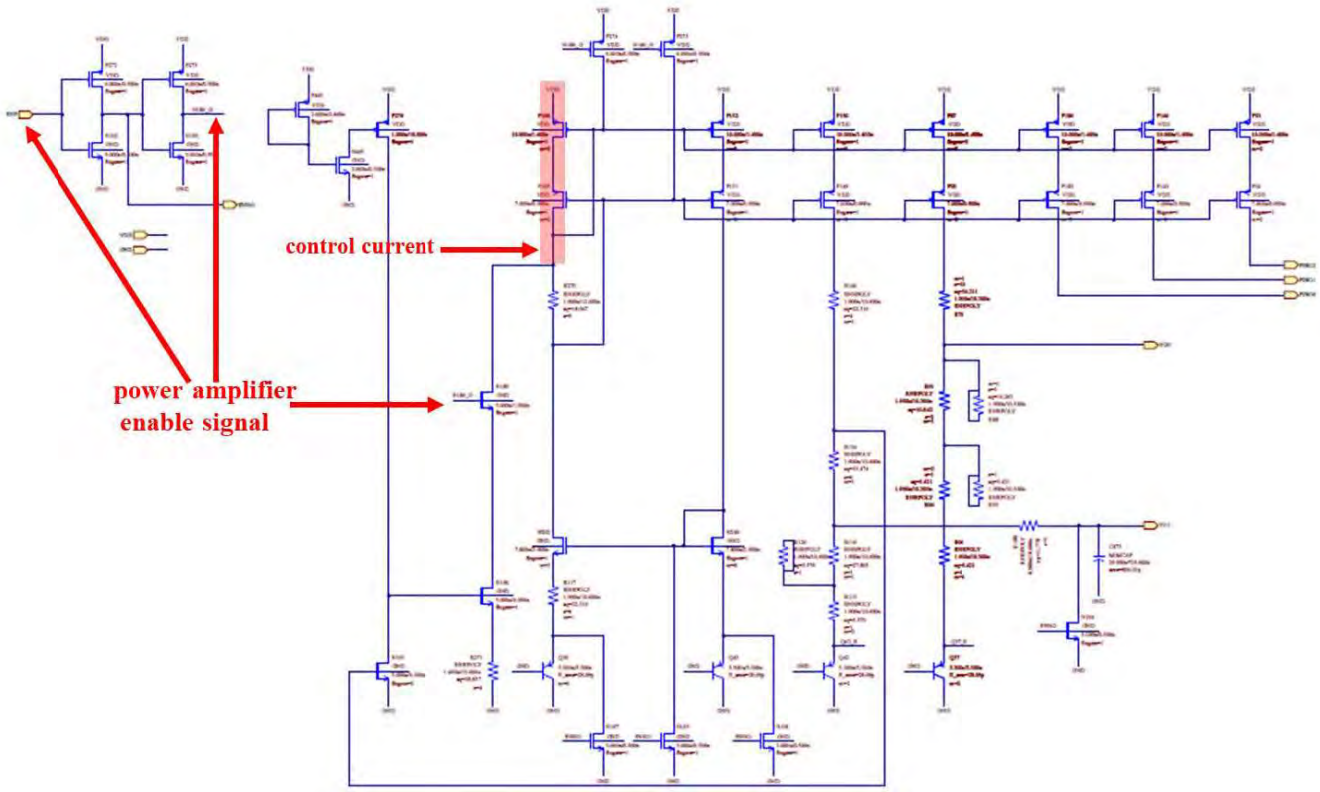
	The bias circuit is coupled to the packaged module's interface through a wire bond in such a way that the bias circuit is configured to receive a power amplifier enable signal (as indicated by the corresponding label above). The bias circuit is coupled to the power amplifier by a wire bond in such a way that the bias circuit is configured to generate a bias signal (as indicated by the corresponding label above) that biases the power amplifier. The reverse engineered schematic below is for the bias circuit (as indicated by the corresponding label below) in the KCT8239S. As highlighted below, the bias circuit includes a "PA_EN" port configured to receive the power amplifier enable signal and a "VINT" port configured to output the bias signal that biases the power amplifier. 

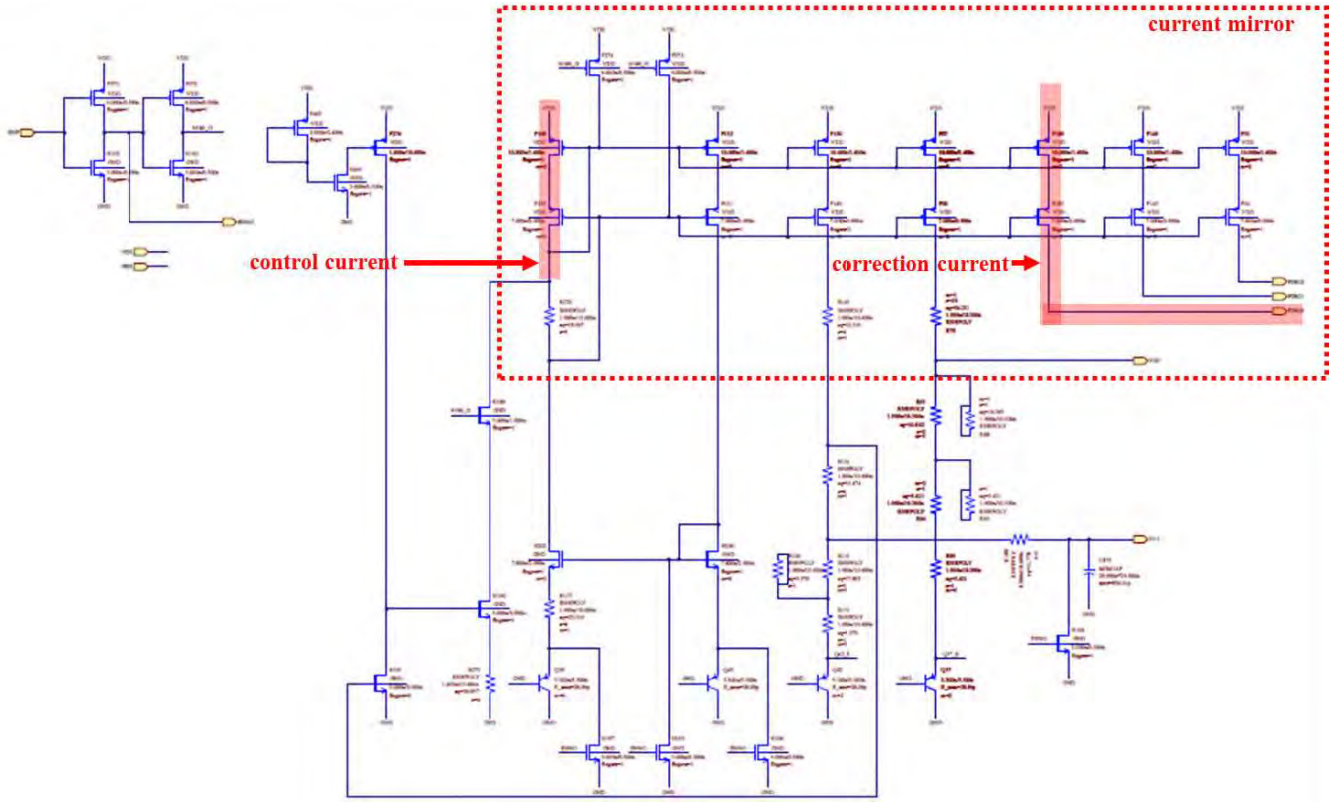
	See, e.g., reverse engineered schematic of the bias circuit of KCT8239S *See also* elements 14[D] through 14[F] (showing details of the bias circuit).
14[D] the bias circuit including a gain correction circuit configured to generate a control current in response to activation of the power amplifier enable signal,	The KCT8239S includes the bias circuit including a gain correction circuit configured to generate a control current in response to activation of the power amplifier enable signal. For example, the reverse engineered schematic below for the bias circuit in the KCT8239S shows that the bias circuit includes a gain correction circuit (as indicated by the corresponding label below).



See, e.g., reverse engineered schematic of the bias circuit of KCT8239S

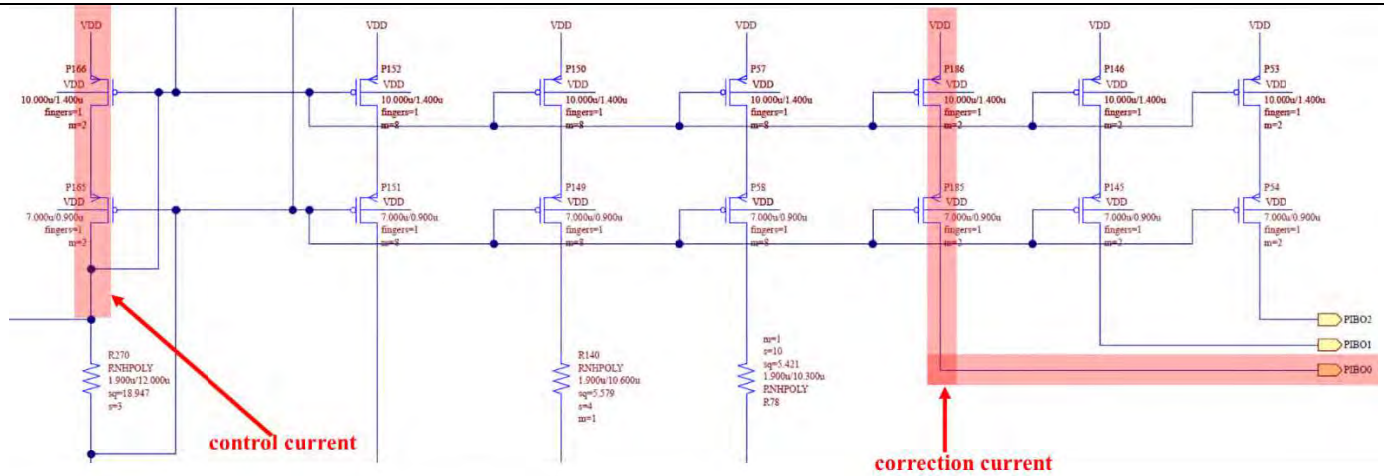
The reverse engineered schematic below for the KCT8239S shows the internal details of the gain correction circuit set forth above. The gain correction circuit receives the power amplifier enable signal (as indicated by the corresponding label below). The power amplifier enable signal is coupled in a way such that the gain correction circuit is configured to generate the control current (as indicated by the corresponding label below) in response to activation of the power amplifier enable signal.

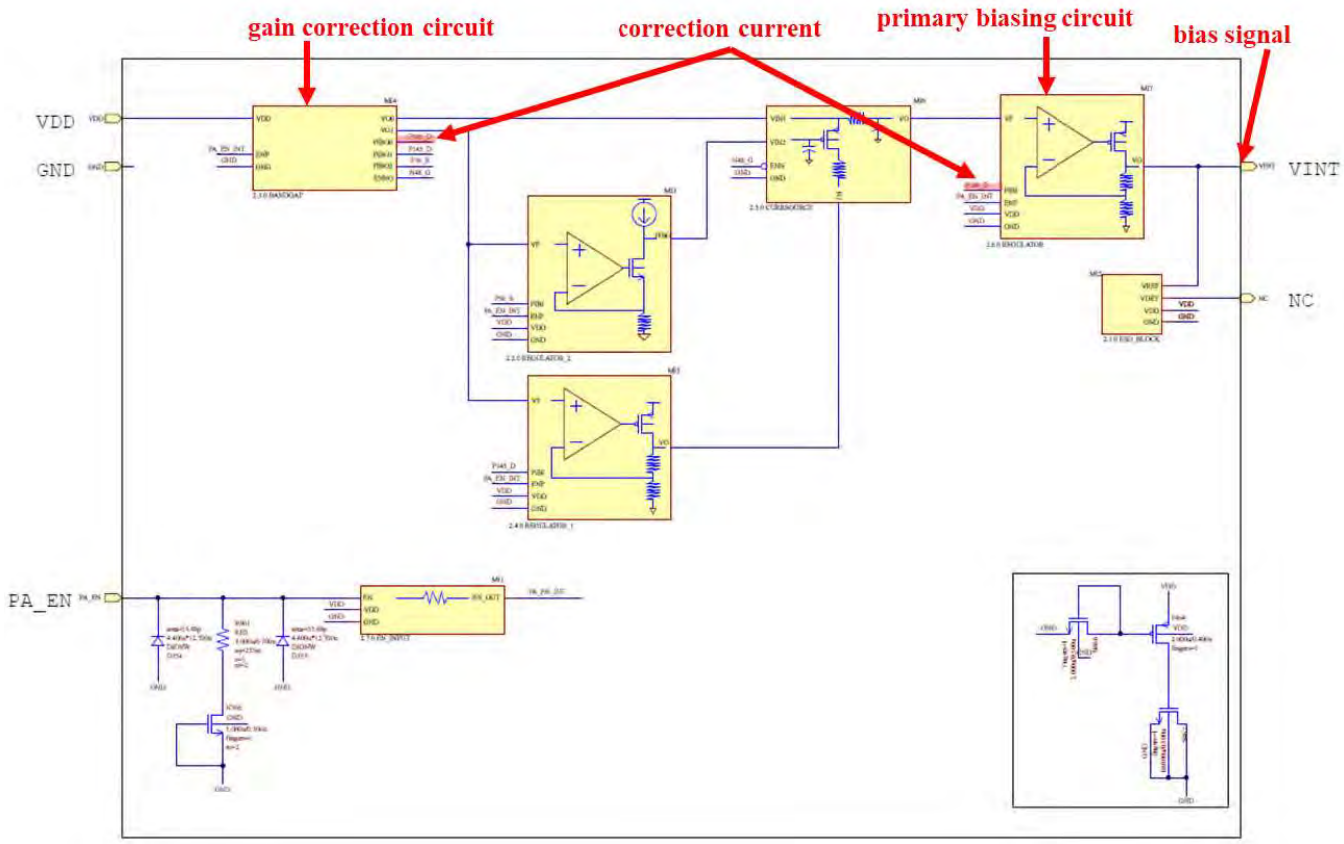
	 *See, e.g.*, reverse engineered schematic of the gain correction circuit of KCT8239S
14[E] and to mirror the control current to generate a correction current,	In the KCT8239S, the bias circuit and its gain correction circuit mirrors the control current to generate a correction current. For example, as shown by the reverse engineered schematic below for the gain correction circuit of the KCT8239S, the gain correction circuit includes a current mirror (as indicated by the corresponding label below). The current mirror is configured to mirror the control current to generate the correction current (as indicated by the corresponding label below). The dashed box with the label below is one example of a current mirror that mirrors the control current to generate the correction current.



See, e.g., reverse engineered schematic of the gain correction circuit of KCT8239S

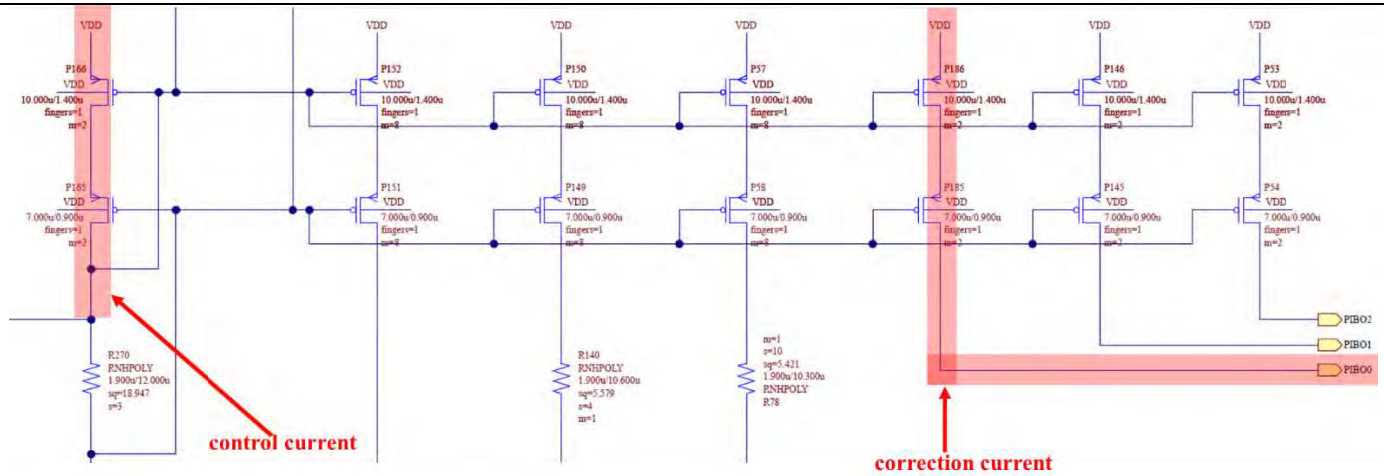
The schematic below for the KCT8239S is an enlarged view of a portion of the current mirror identified above, which is configured to mirror the control current to generate the correction current. As set forth in the '563 patent, a current mirror can have any suitable gain when mirroring a current. *See* '563 patent, 11:63-12:2. For example, the current mirror in KCT8239S is configured to mirror the control current by a factor of about 1, based on the multiple numbers designated in the schematic below (e.g., "m=2" for the control current and "m=2" for the correction current).

	 *See, e.g.*, enlarged portion of reverse engineered schematic of the gain correction circuit of KCT8239S
14[F] and a primary biasing circuit configured to generate the bias signal based on the correction current and the power amplifier enable signal.	In the KCT8239S, the bias circuit includes a primary biasing circuit configured to generate the bias signal based on the correction current and the power amplifier enable signal. For example, as shown in the reverse engineered schematic for the KCT8239S below, a primary biasing circuit (as indicated by the corresponding label below) is configured to generate the bias signal (as indicated by the corresponding label below) for the power amplifier based on the correction current and the power amplifier enable signal.

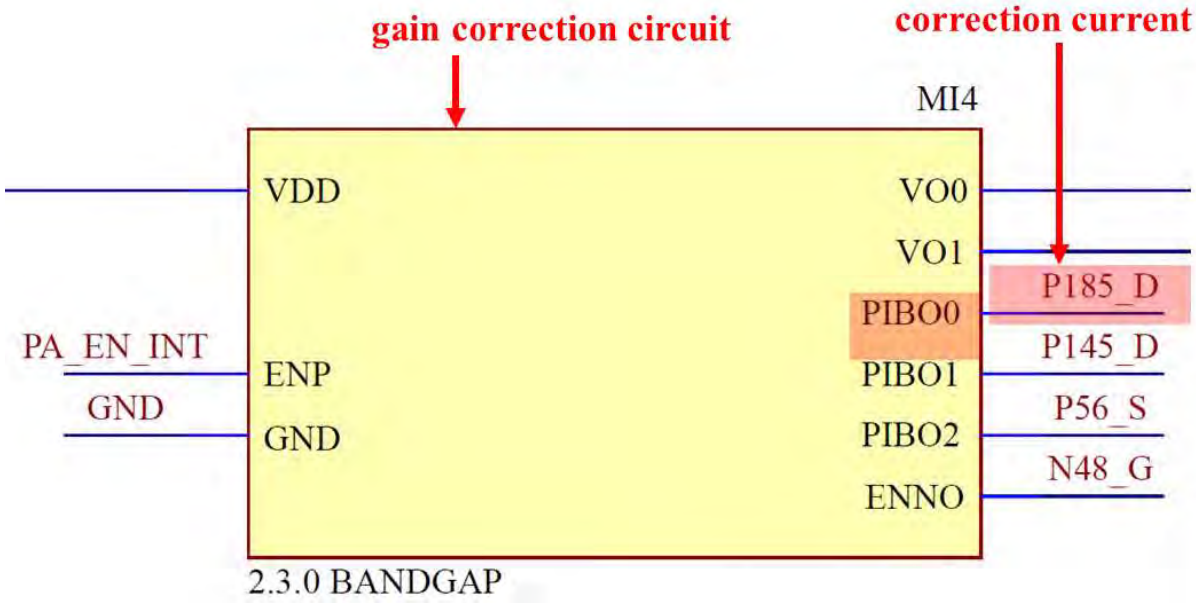


See, e.g., reverse engineered schematic of the bias circuit of KCT8239S

The correction current is output by the "PIBO0" port of the gain correction circuit, as shown by the reverse engineered schematics below.

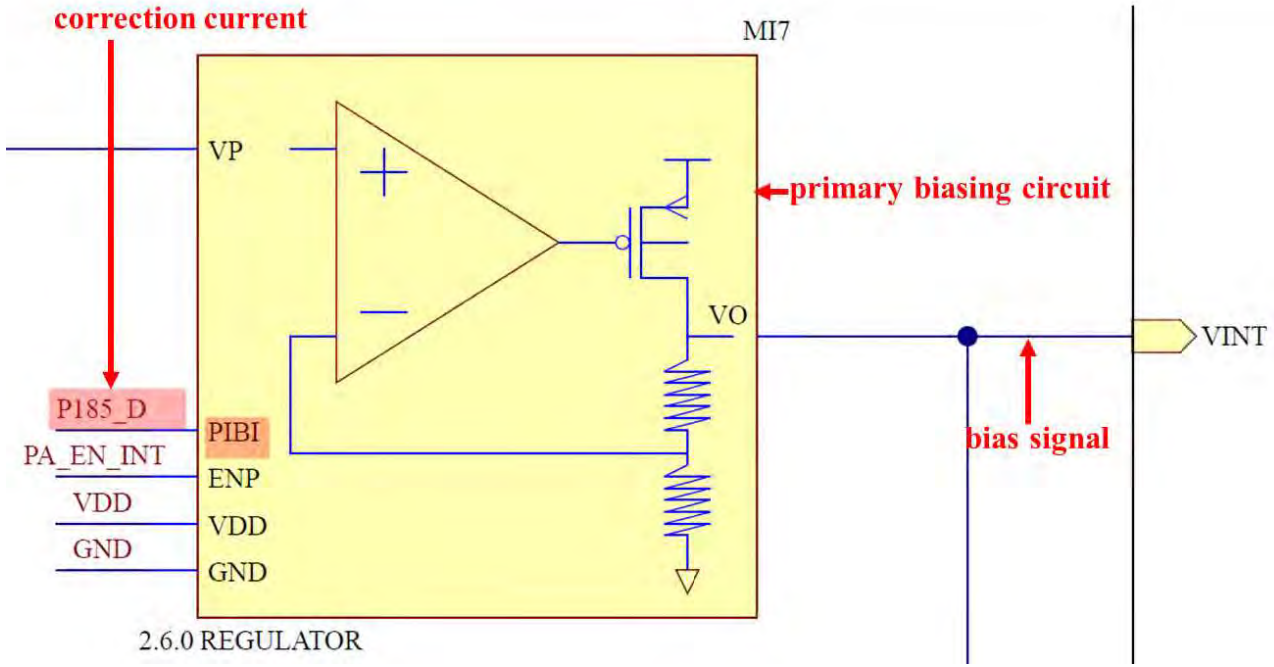


See, e.g., enlarged portion of reverse engineered schematic of the gain correction circuit of KCT8239S



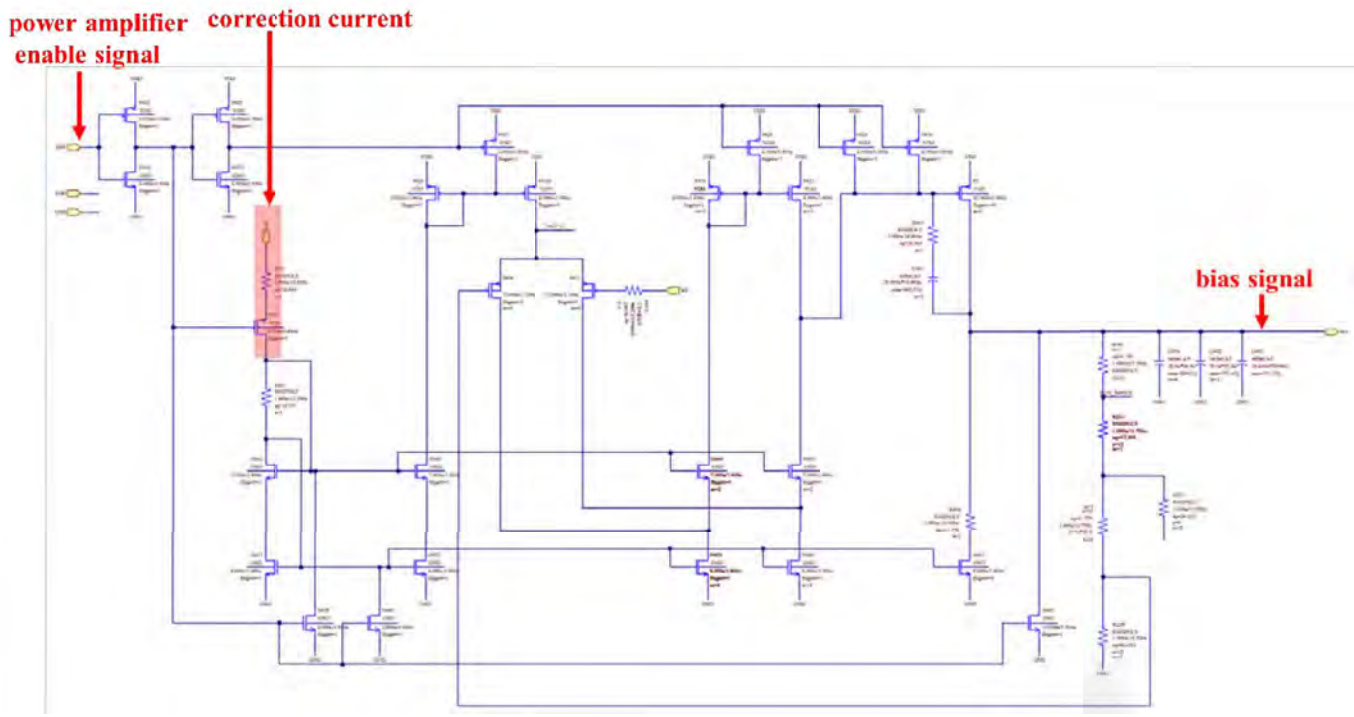
See, e.g., enlarged portion of reverse engineered schematic of the bias circuit of KCT8239S

The "PIBO0" port of the gain correction circuit (shown above and as corresponding to P185_D) is connected to the "PIBI" port of the primary biasing circuit (as indicated by the corresponding label below showing P185_D connecting to PIBI), as shown by the schematic below.



See, e.g., enlarged portion of reverse engineered schematic of the bias circuit of KCT8239S

As shown by the schematic below for the primary biasing circuit of the KCT8239S, the primary biasing circuit takes in the correction current (as indicated by the corresponding label below) as an input and the power amplifier enable signal (as indicated by the corresponding label below) as another input so that the primary biasing circuit is configured to generate the bias signal based on the correction current and the power amplifier enable signal.



See, e.g., reverse engineered schematic of the primary biasing circuit of KCT8239S

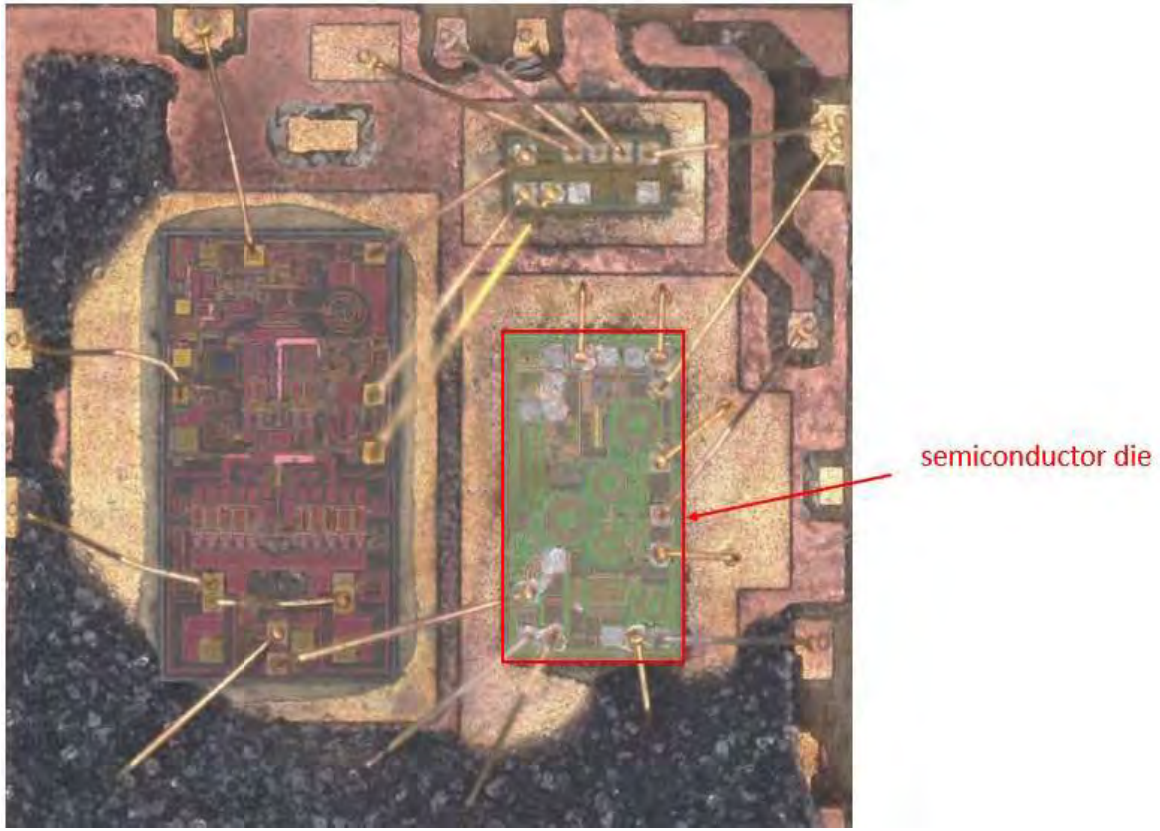
EXHIBIT 20

EXHIBIT 20
SKYWORKS SOLUTIONS, INC.'S INFRINGEMENT CHART
KCT8539S
U.S. Patent No. 9,450,579
Independent Claims 1 and 7

Skyworks Solutions, Inc. ("Skyworks") provides this exemplary claim chart for independent claims 1 and 7 of U.S. Patent No. 9,450,579 (the "'579 patent") applied to Kangxi Communication Technologies (Shanghai) Co., Ltd's and Grand Chip Labs, Inc.'s (collectively, "KCT") KCT8539S product. The disclosures in this claim chart directed to the KCT8539S are also more broadly directed to any sale, offer for sale, use, or importation of the KCT8539S in the U.S., including in an end product such as a wireless router or as a standalone product that is not incorporated in an end product.

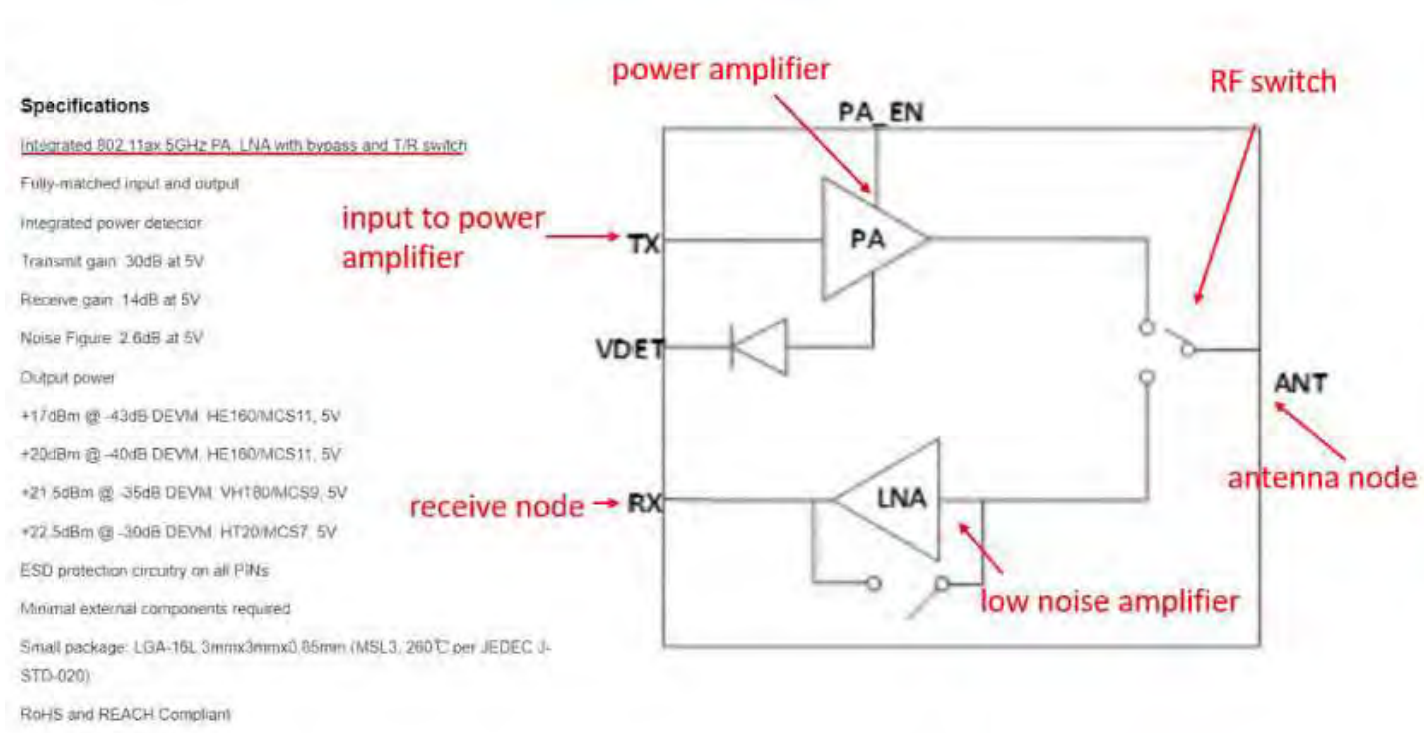
The claim chart below demonstrates infringement by comparing each element of the charted claims to corresponding components, aspects, and/or features of the KCT8539S product. This claim chart is not intended to constitute an expert report on infringement. This claim chart includes information provided by way of example, and not by way of limitation.

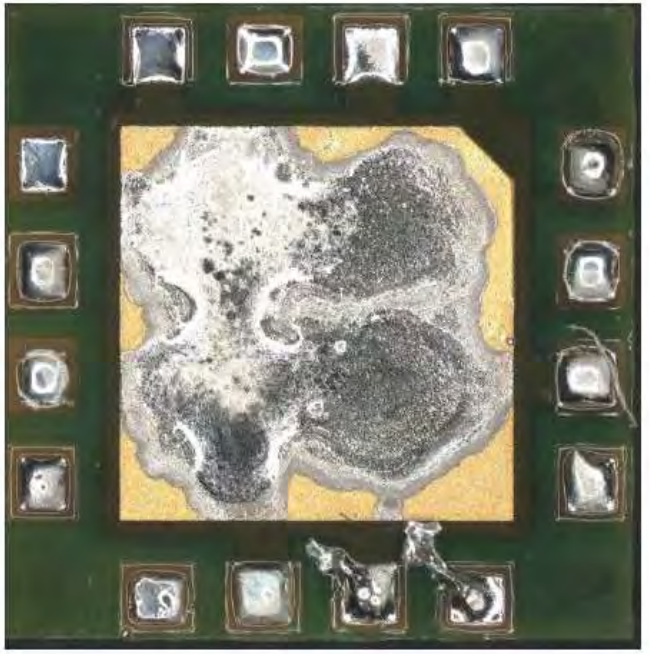
The analysis set forth below is based only upon information from publicly available sources regarding the KCT8539S product. Further analysis of non-public information during fact discovery will likely assist in identifying all infringing features and functionalities used by KCT in the KCT8539S product. Accordingly, Skyworks reserves the right to supplement this infringement analysis once such information is made available to Skyworks. Further, Skyworks reserves the right to supplement this infringement analysis, as appropriate, upon issuance of an order construing any terms recited in the asserted claims or as other circumstances so merit.

Claim	KCT8539S
1[pre] A semiconductor die comprising:	To the extent that the preamble of claim 1 is limiting, the KCT8539S comprises a semiconductor die. For example, the KCT8539S has a semiconductor die, highlighted by the red box below.  *See, e.g.*, photo of the KCT8539S product identifying the semiconductor die.

Claim	KCT8539S
	For example, the KCT8539S product description below states that the KCT8539S is an "RF Front-end Module" that "incorporates key RF functionality needed for IEEE 802.11a/n/ac/ax WLAN systems operating in the 5.15-5.85GHz range."[1]  KCT8539S **5GHz 802.11ax RF Front-End Module** **Introduction** KCT8539S is a highly integrated RF Front-End Integrated Circuit incorporates key RF functionality needed for IEEE 802.11a/n/ac/ax WLAN systems operating in the 5.15-5.85GHz range. KCT8539S integrates a high-efficiency high-linearity power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated matching network, LO rejection, and harmonic filters all in one device. KCT8539S has simple and low-voltage control logic, and requires minimal external components. A power detector is also integrated for accurately monitoring of output power from the PA. KCT8539S is assembled in a compact, low-profile 3x3x0.85mm 16-lead LGA package. KCT8539S is the ideal RF front-end solution for implementing 5GHz high-power WLAN systems supporting multiple standards including 802.11a/n/ac/ax. *See, e.g.*, KCT8539S product description, https://perma.cc/DA7F-4CED. For example, the KCT8539S has an RF switch (indicated by the corresponding red arrow in the figure below) that selectively allows either transmission or reception of signals.[2] The KCT product description describes the switch as a "T/R switch" (indicated by the red underlining in the text below). The figure below also shows the power amplifier (indicated by the corresponding red arrow below), the antenna node (indicated by the corresponding red arrow below), the receive node (indicated by the corresponding red arrow below), the low noise amplifier

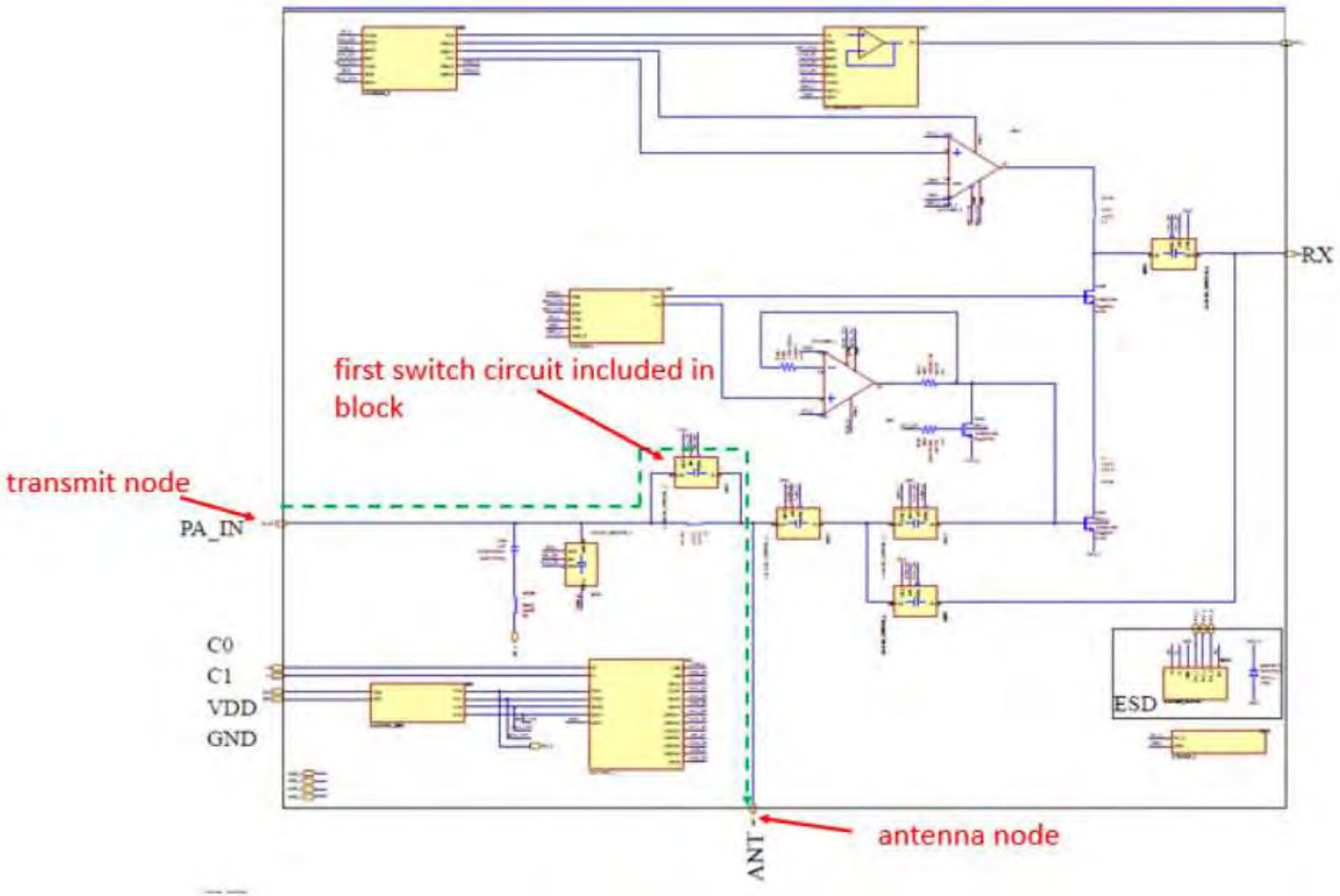
[1] *See* https://perma.cc/DA7F-4CED.
[2] *See* https://perma.cc/DA7F-4CED.

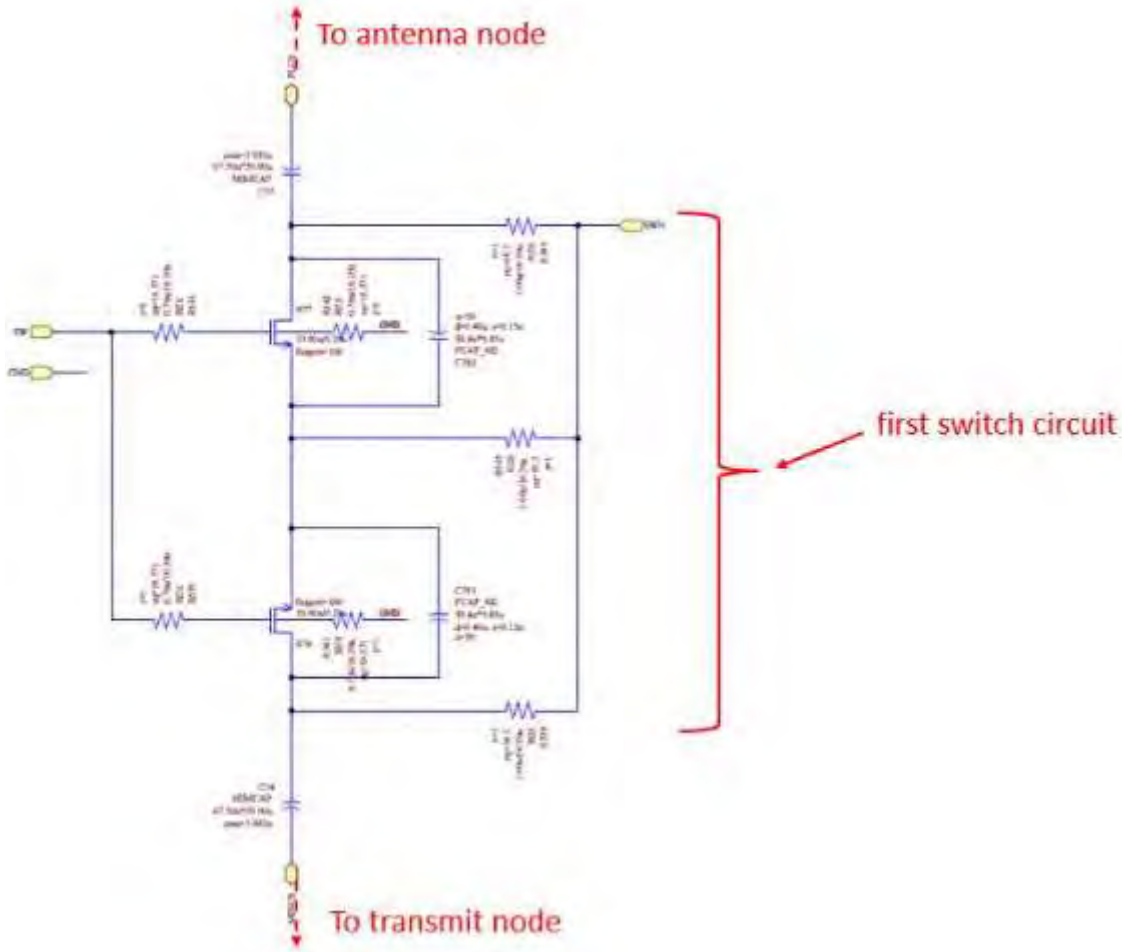
Claim	KCT8539S
	(indicated by the corresponding red arrow below), and the input to the power amplifier (indicated by the corresponding red arrow below).  *See, e.g.*, KCT8539S product description and simplified block diagram, https://perma.cc/DA7F-4CED. For example, the photos below show the exterior of the KCT8539S device die package, front (left) and back (right).

Claim	KCT8539S
	  *See, e.g.* photo of the KCT8539S product, exterior of package, front (left) and back (right).
1[A] a semiconductor substrate;	The KCT8539S comprises a semiconductor substrate. For example, a semiconductor substrate for the KCT8539S (indicated by white grid lines below) is the material upon which the devices on the die are fabricated.

Claim	KCT8539S
	 *See, e.g.*, photo of the KCT8539S product, annotated to show the location of the semiconductor substrate.
1[B] a first switch circuit	The KCT8539S comprises a first switch circuit formed on the semiconductor substrate connected between an antenna node and a transmit node.

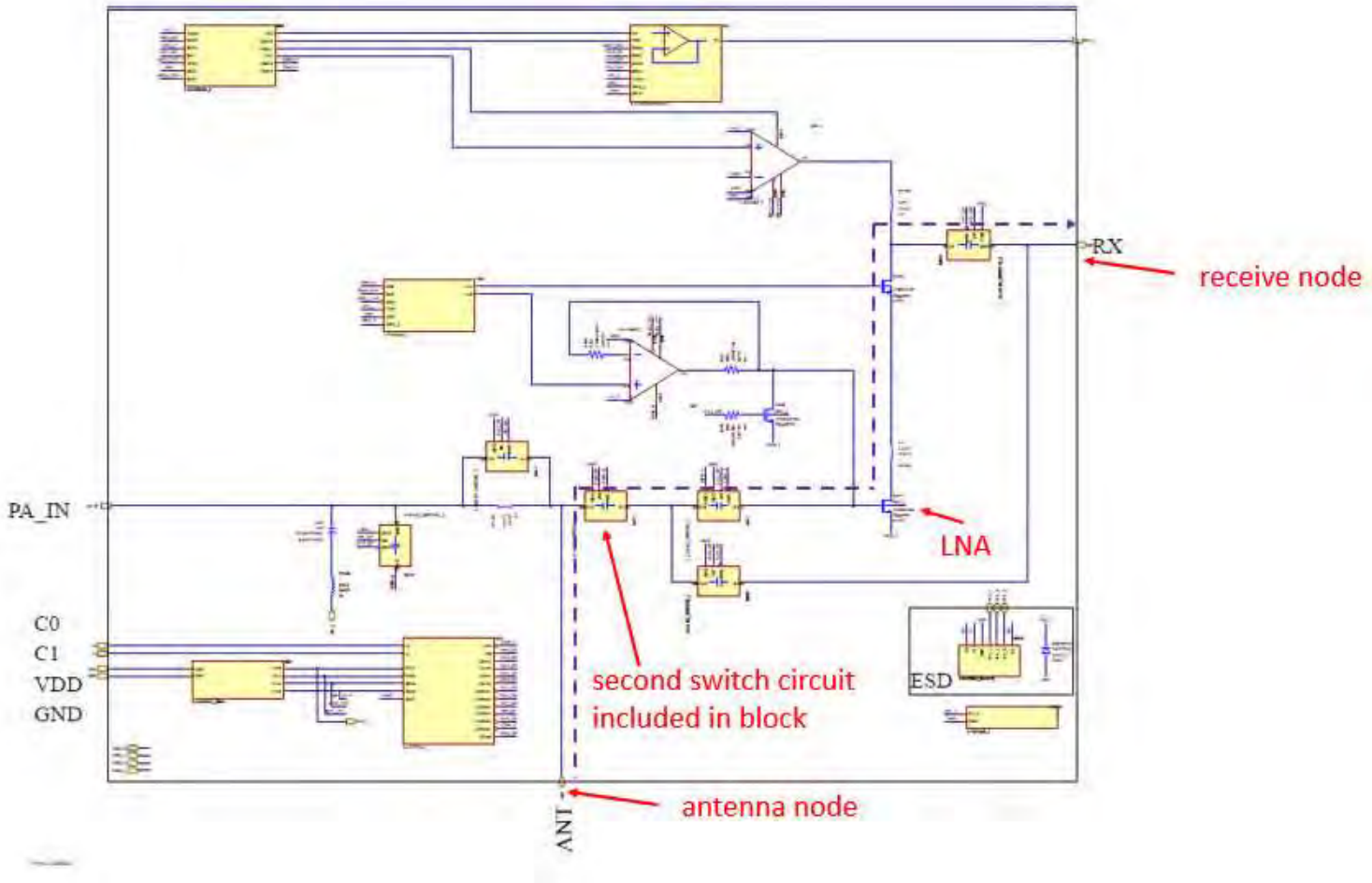
Claim	KCT8539S
formed on the semiconductor substrate connected between an antenna node and a transmit node;	For example, in the KCT8539S, the first switch circuit (located within the block and identified by the corresponding red arrow below) is connected between the antenna node (indicated by the corresponding red arrow below) and the transmit node (indicated by the corresponding red arrow below). In transmit mode, the signal path from the transmit node, through the first switch circuit, and to the antenna node is shown by the green dashed line below. The first switch circuit is formed on the semiconductor substrate.

Claim	KCT8539S
	 *See, e.g.*, reverse engineered circuit schematic of the KCT8539S product's low noise amplifier die, annotated to show the location of a first switch circuit, transmit node, and antenna node. For example, in the KCT8539S, the first switch circuit (indicated by the corresponding red arrow below) is between the transmit node and the antenna (ANT) node, as shown in the expanded view below.

Claim	KCT8539S
	 *See, e.g.*, reverse engineered circuit schematic of KCT8539S product showing an expanded view of the block containing the first switch circuit on the low noise amplifier die. *See also*, 1[pre]-1[A].

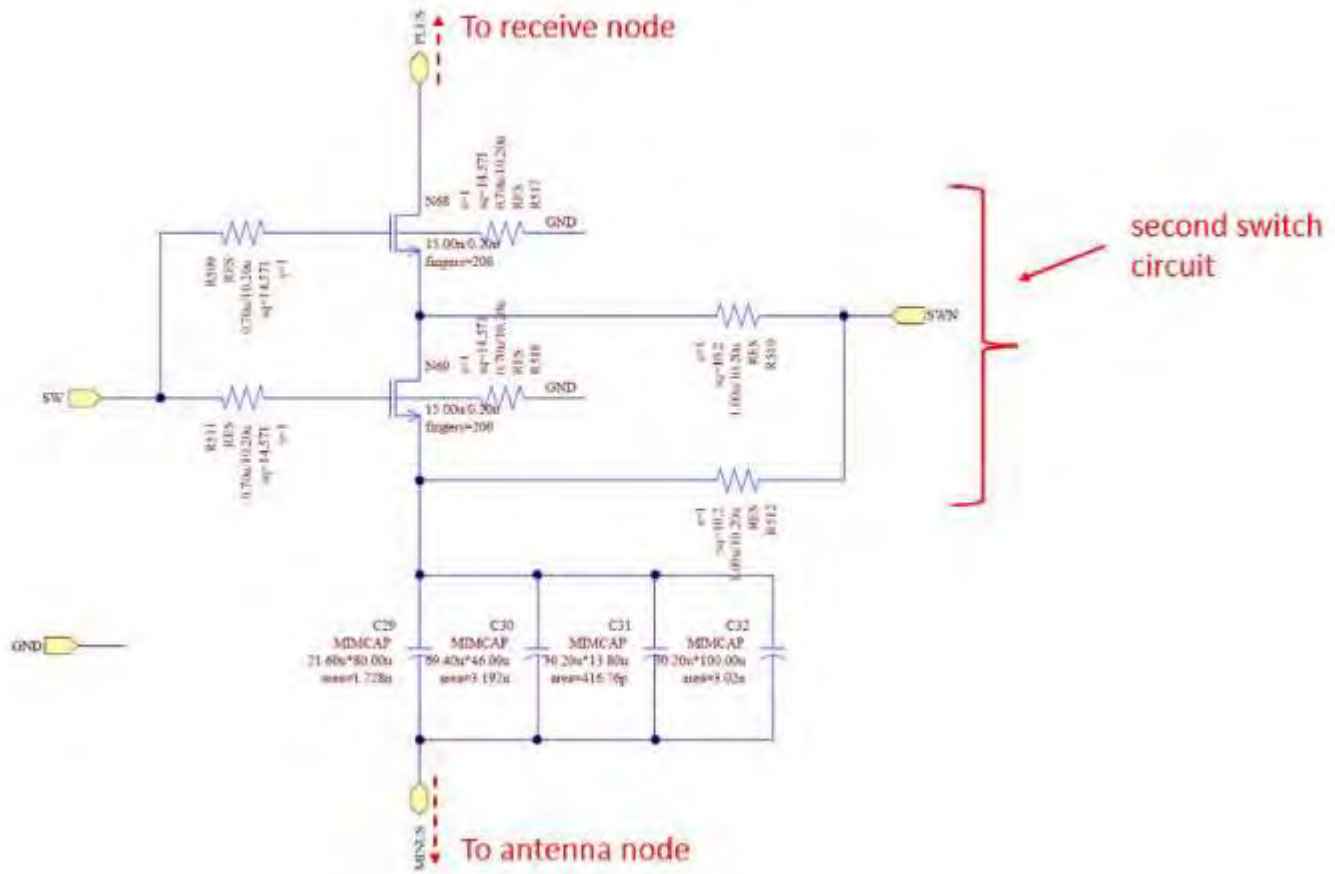
Claim	KCT8539S
1[C] a second switch circuit formed on the semiconductor substrate and connected between the antenna node and a receive node;	The KCT8539S comprises a second switch circuit formed on the semiconductor substrate and connected between the antenna node and a receive node. For example, in the KCT8539S, the second switch circuit (located in the block identified by the corresponding red arrow below) is connected between the antenna node (indicated by the corresponding red arrow below) and the receive node (indicated by the corresponding red arrow below). In receive mode, the approximate signal path from the antenna node to the receive node through the low noise amplifier (LNA) is shown by the dashed purple line in the figure below. The second switch circuit is formed on the semiconductor substrate.

Claim	KCT8539S

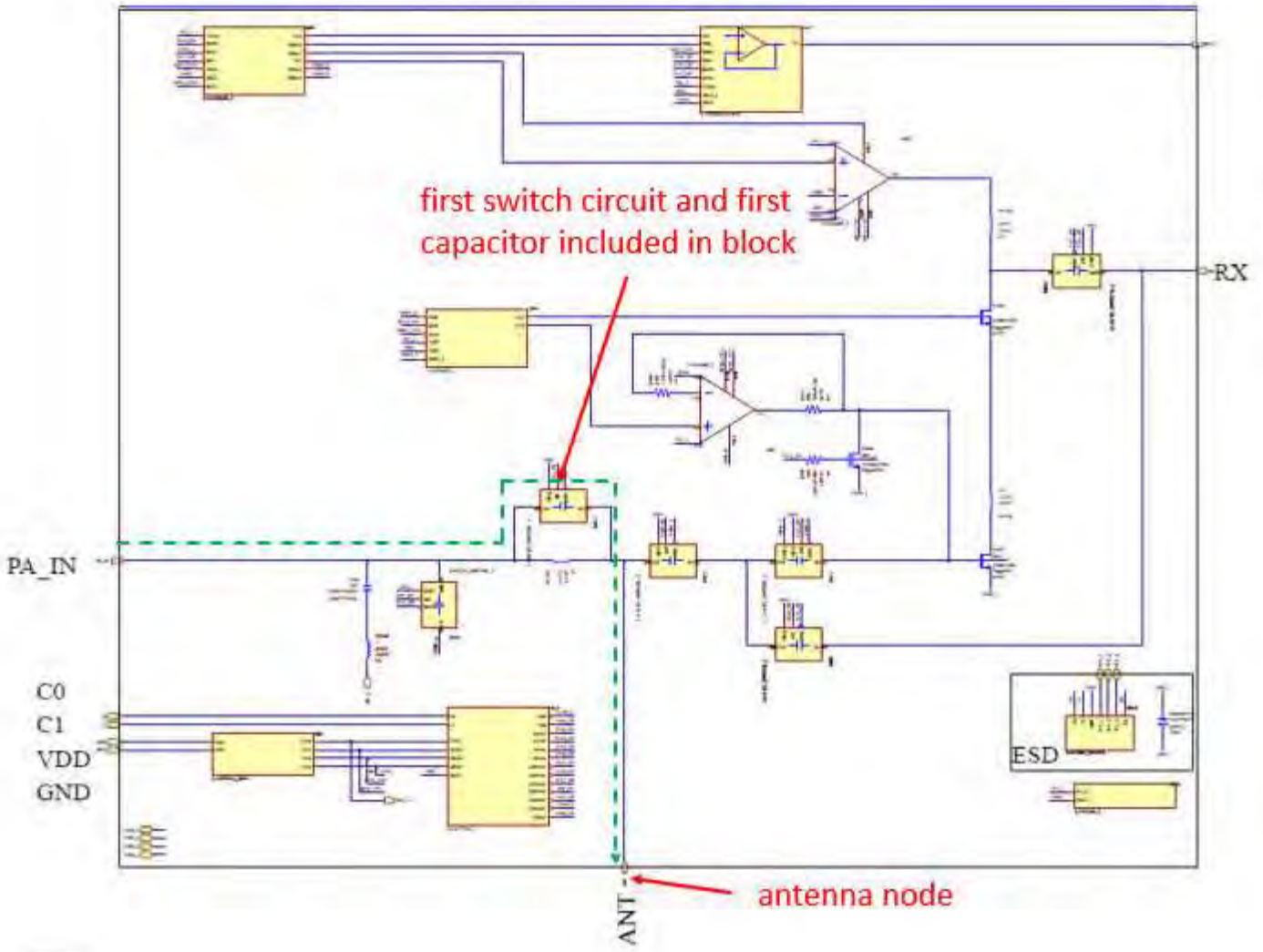


See, e.g., reverse engineered circuit schematic of the KCT8539S product's low noise amplifier die, annotated to show the location of a second switch circuit, receive node, low noise amplifier (LNA), and antenna node.

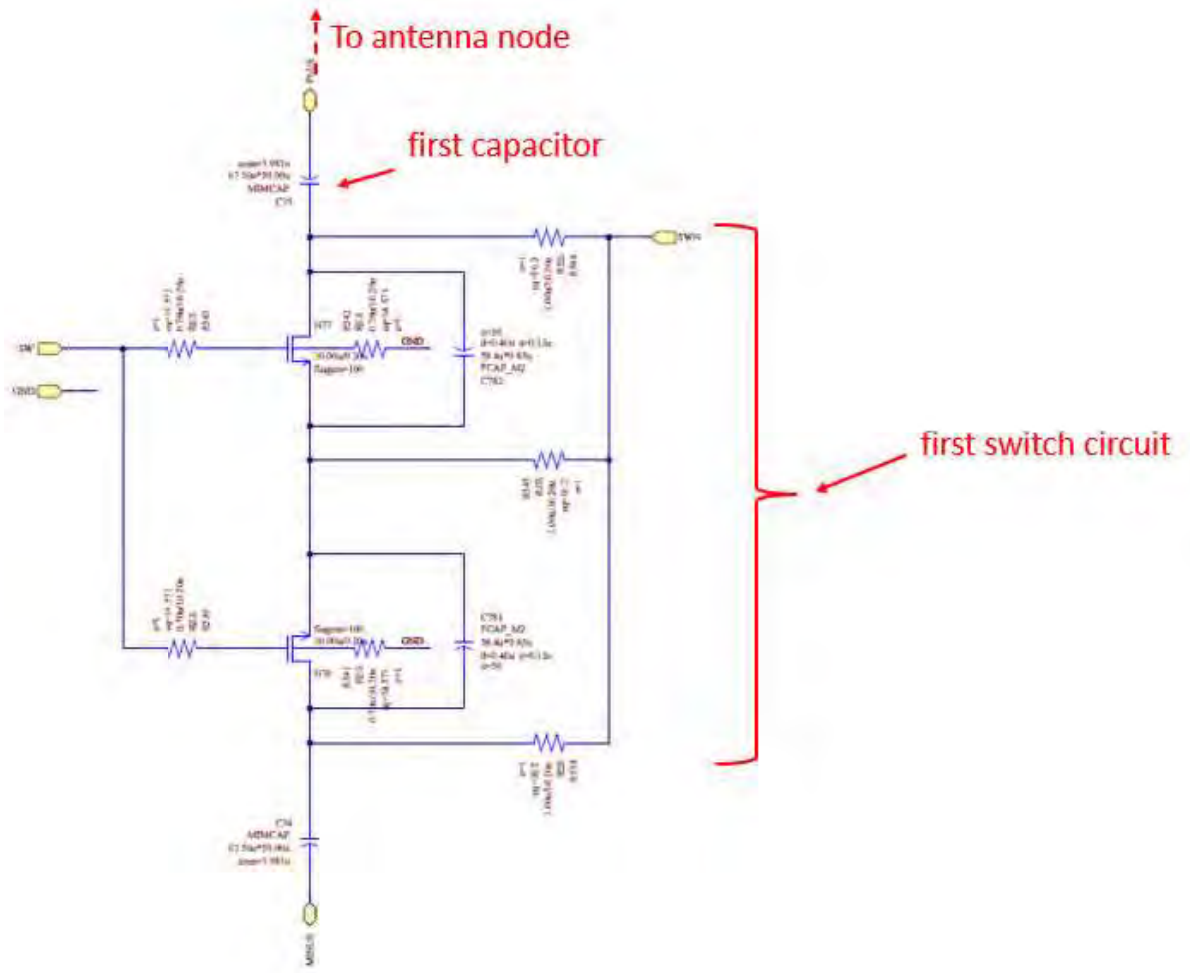
For example, in the KCT8539S, the second switch circuit (indicated by the corresponding red arrow below) is between the receive node and the antenna (ANT) node, as shown in the expanded view below.

Claim	KCT8539S
	 *See, e.g.*, reverse engineered circuit schematic of KCT8539S product showing an expanded view of block containing the second switch circuit on the low noise amplifier die. *See also*, 1[pre]-1[A].
1[D] a first capacitor formed	The KCT8539S comprises a first capacitor formed on the semiconductor substrate and connected in series with the first switch circuit between the first switch circuit and the antenna node.

Claim	KCT8539S
on the semiconductor substrate and connected in series with the first switch circuit between the first switch circuit and the antenna node;	For example, in the KCT8539S, the first capacitor (indicated by the corresponding red arrow below) is formed on the semiconductor substrate and is connected in series with the first switch circuit (located within the block identified by the corresponding red arrow below). The approximate signal path during transmit mode is shown by the green dashed line in the figure below. In addition, the first capacitor is located between the first switch circuit and the antenna node (ANT) (indicated by the corresponding red arrow below).

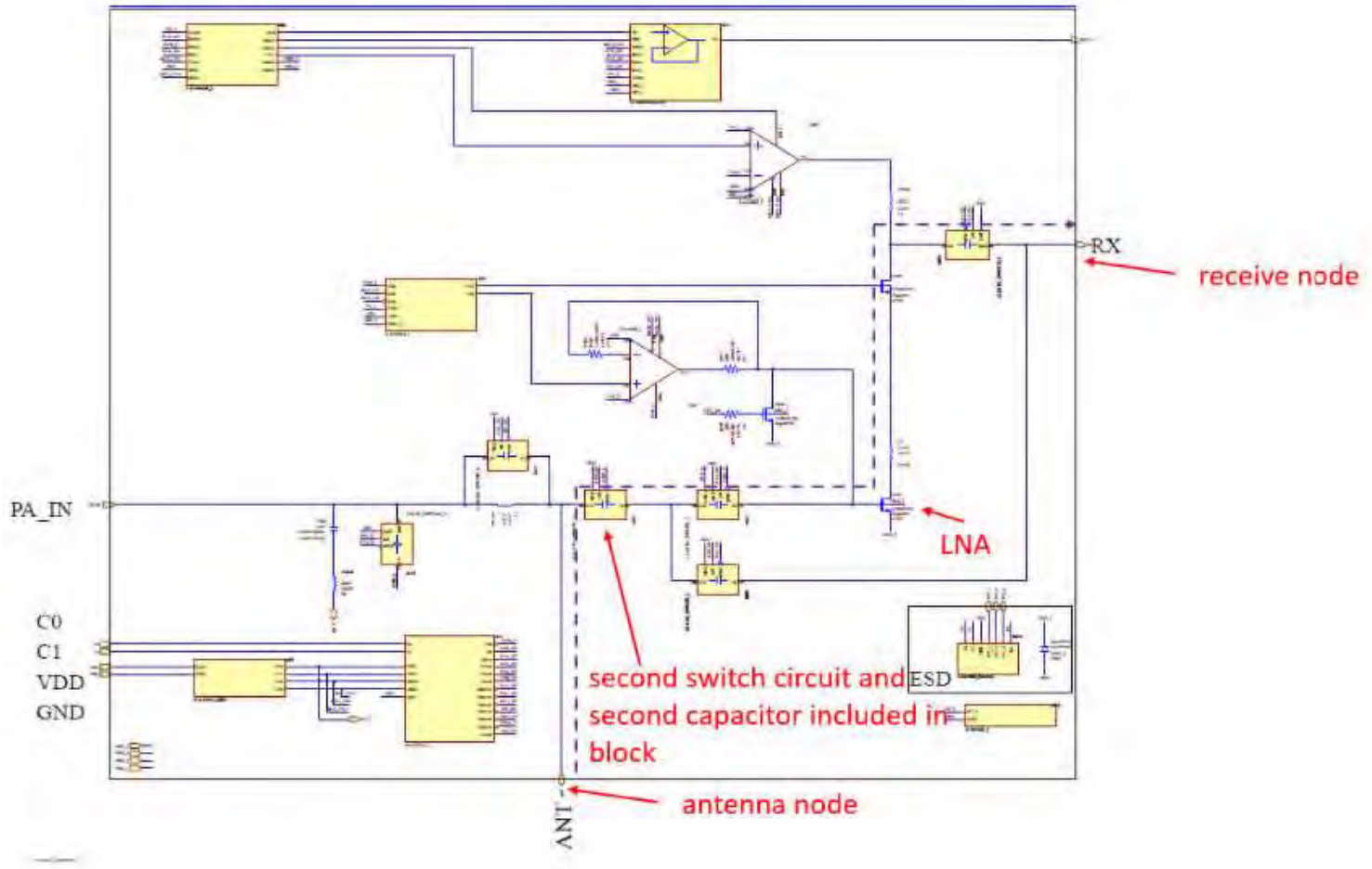
Claim	KCT8539S
	

Claim	KCT8539S
	See, e.g., reverse engineered circuit schematic of the KCT8539S product's low noise amplifier die, annotated to show the location of a first switch circuit, first capacitor, and antenna node. For example, in the KCT8539S, the first switch circuit and first capacitor are in series. In addition, the first capacitor is between the first switch circuit and the antenna (ANT) node.

Claim	KCT8539S
	 *See, e.g.*, reverse engineered circuit schematic of the KCT8539S product showing an expanded view of circuit block containing the first switch circuit and first capacitor on the low noise amplifier die. *See also*, 1[A].

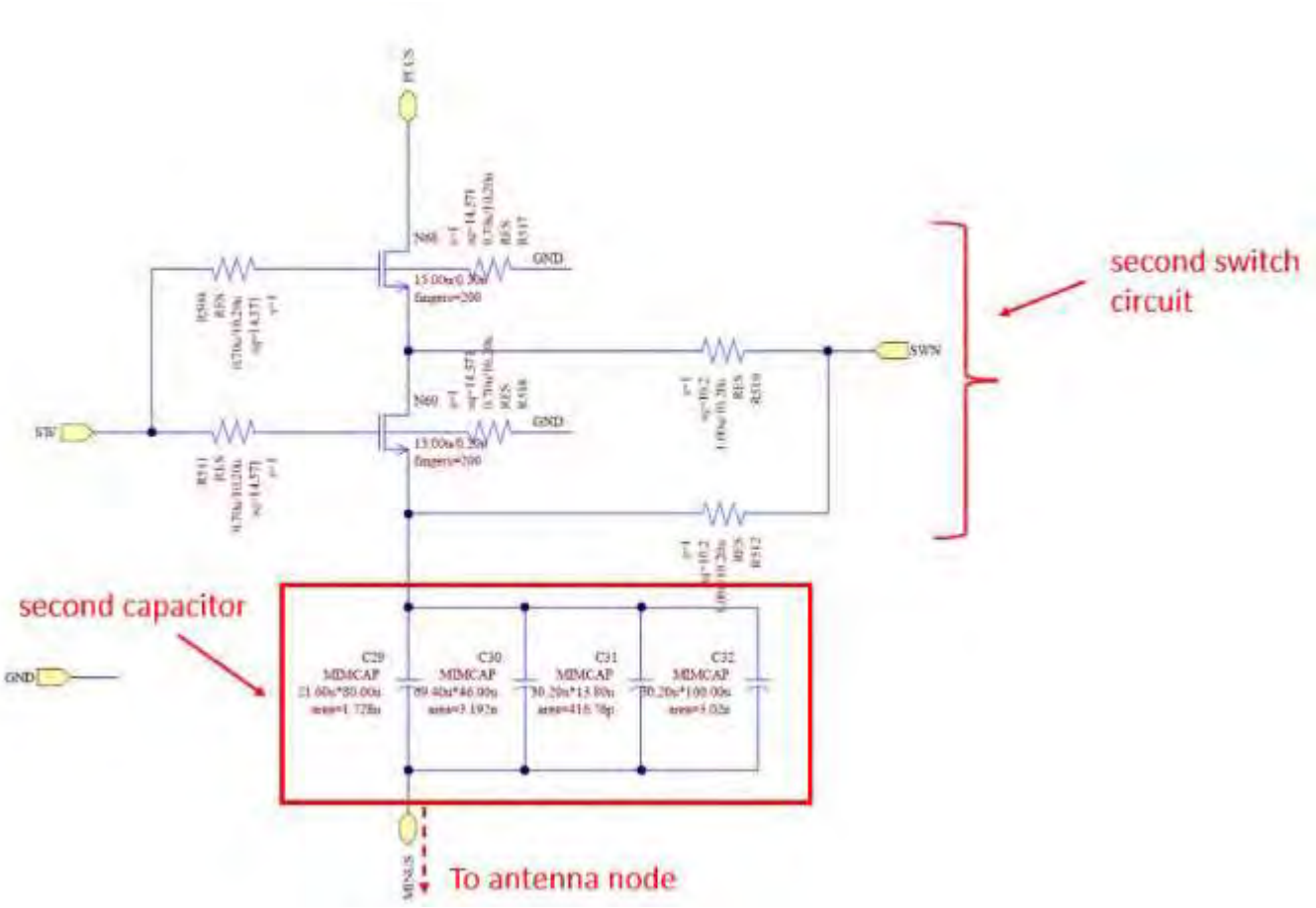
Claim	KCT8539S
1[E] a second capacitor formed on the semiconductor substrate and connected in series with the second switch circuit between the second switch circuit and the antenna node; and	The KCT8539S comprises a second capacitor formed on the semiconductor substrate and connected in series with the second switch circuit between the second switch circuit and the antenna node. For example, in the KCT8539S, the second capacitor (indicated by the corresponding red arrow below) is formed on the semiconductor substrate. In receive mode, the approximate signal path from the antenna node (indicated by the corresponding red arrow below) to the receive node (indicated by the corresponding red arrow below) through the low noise amplifier (LNA) (indicated by the corresponding red arrow below) is shown by the dashed purple line in the figure below. The second capacitor and the second switch circuit are in the block as indicated by the corresponding red arrow below.

Claim	KCT8539S

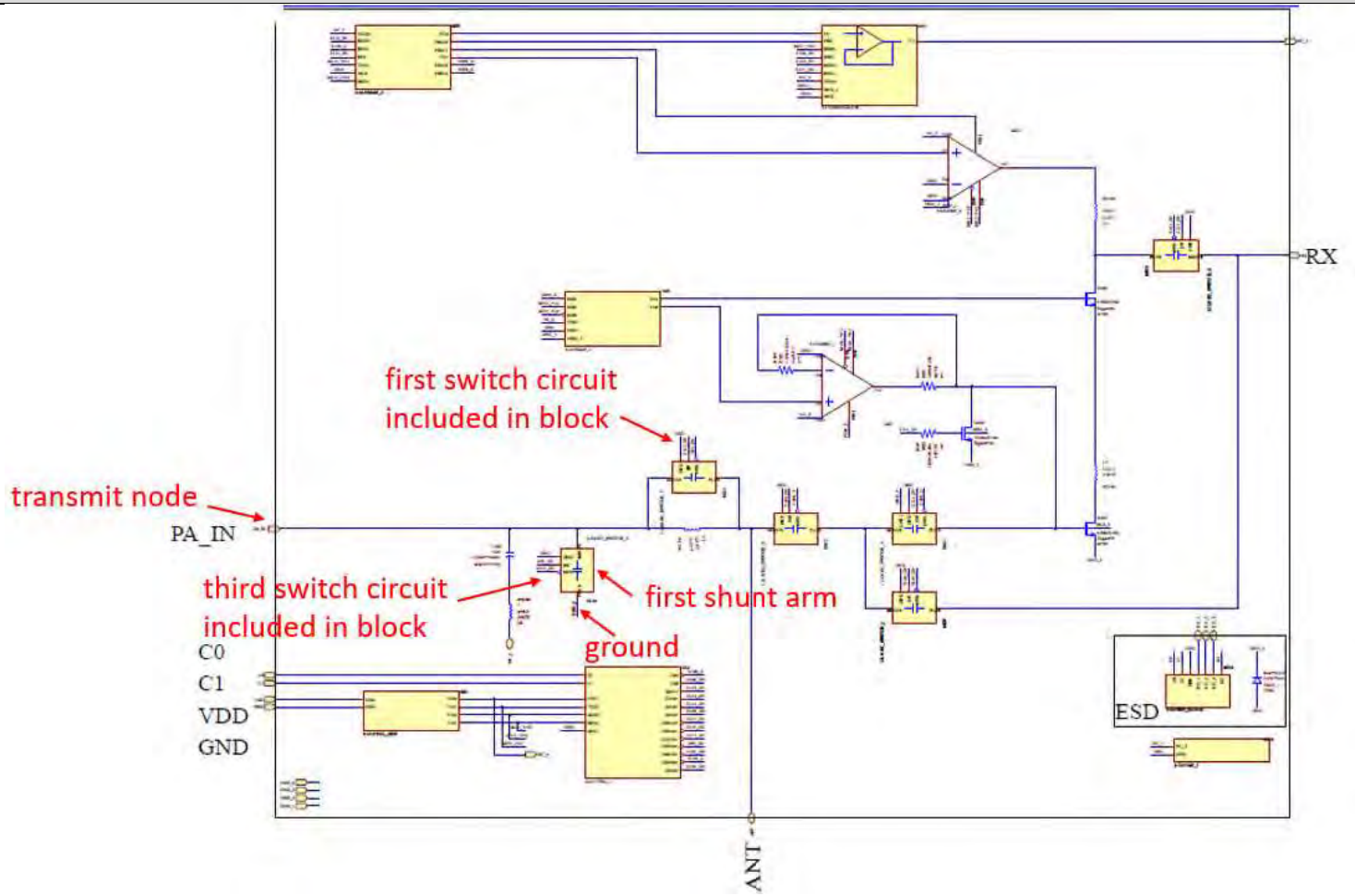


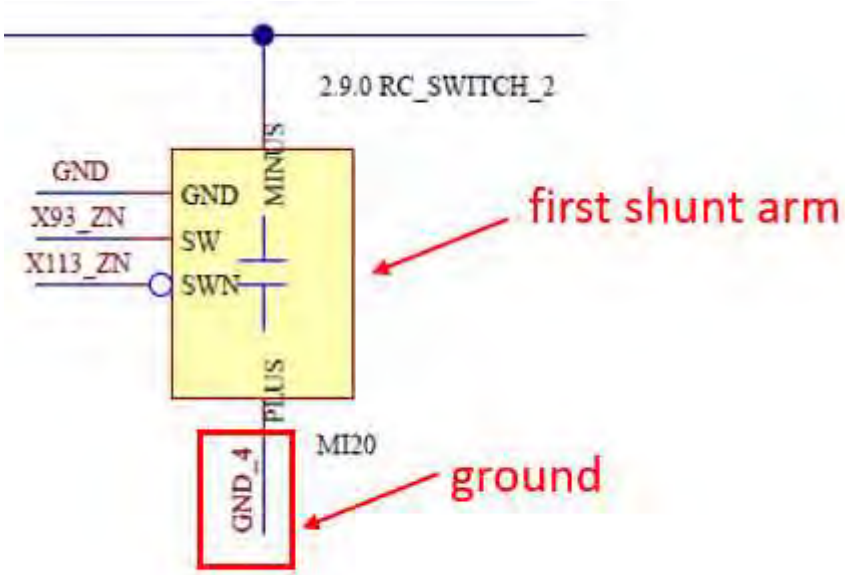
See, e.g., reverse engineered circuit schematic of the KCT8539S product's low noise amplifier die, annotated to show the antenna node, receive node, low noise amplifier (LNA), second switch circuit, and second capacitor.

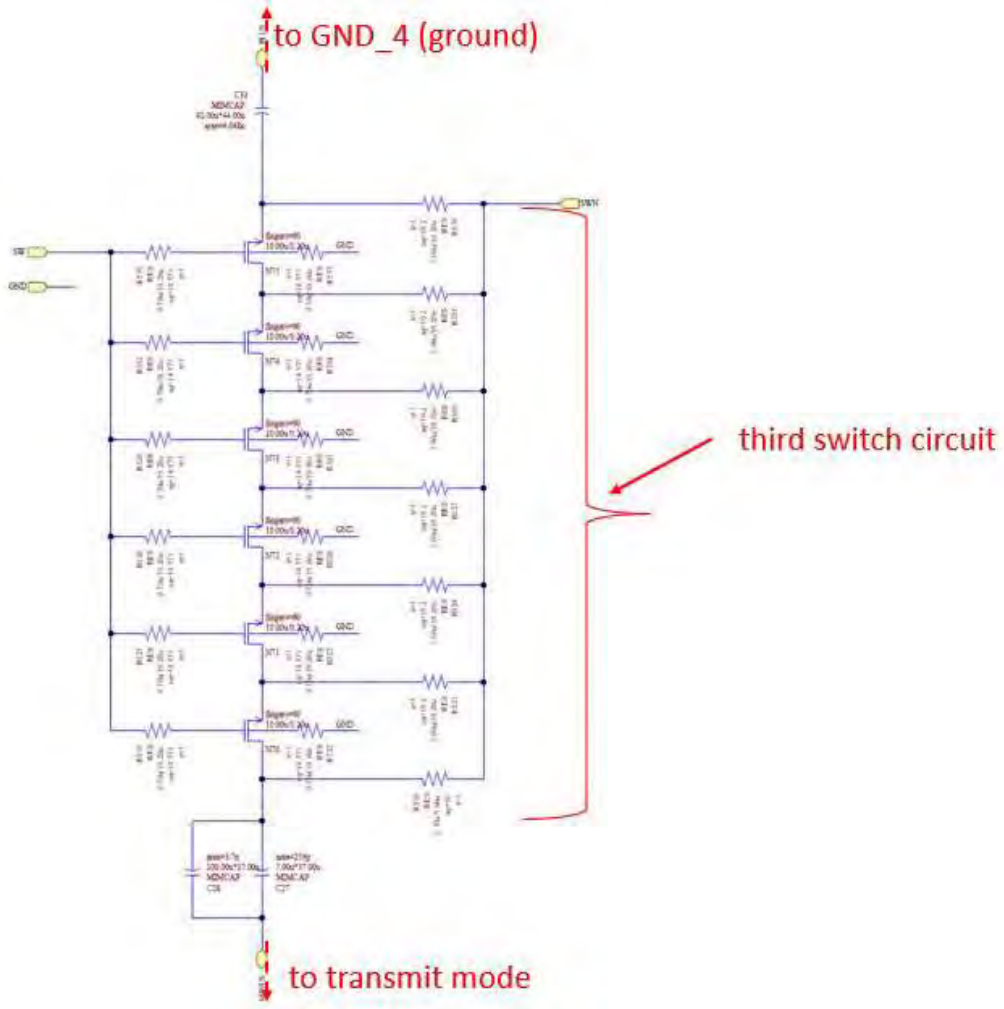
For example, in the KCT8539S, the second capacitor (indicated by the corresponding red arrow below) is connected in series with the second switch circuit (indicated by the corresponding red bracket below). In addition,

Claim	KCT8539S
	the second capacitor is located between the second switch circuit and the antenna node (indicated by the corresponding red arrow below).  *See, e.g.*, reverse engineered circuit schematic of the KCT8539S product showing an expanded view of the box including the second capacitor and second switch circuit on the low noise amplifier die.

Claim	KCT8539S
	See also, 1[A].
1[F] a first shunt arm formed on the semiconductor substrate and connected to the first switch circuit and the transmit node, the first shunt arm including a third switch circuit connected to ground.	The KCT8539S comprises a first shunt arm formed on the semiconductor substrate and connected to the first switch circuit and the transmit node, the first shunt arm including a third switch circuit connected to ground. For example, in the KCT8539S, the first shunt arm (indicated by the corresponding red arrow identifying the corresponding block below) is formed on the semiconductor substrate and is connected to the first switch circuit (indicated by the red arrow identifying the corresponding block below) and the transmit node (indicated by the corresponding red arrow below). The first shunt arm (indicated by the corresponding red arrow identifying the corresponding block below) includes a third switch circuit (indicated by the red arrow identifying the corresponding block below) connected to ground (indicated by the corresponding red arrow below).

Claim	KCT8539S
	 *See, e.g.*, reverse engineered circuit schematic of the KCT8539S product's low noise amplifier die identifying the first shunt arm, the first switch circuit, third switch circuit, transmit node, and ground.

Claim	KCT8539S
	For example, an enlarged view of the circuit schematic block corresponding to the first shunt arm (indicated by the corresponding red arrow below) shows that it is connected to ground (GND_4) (indicated by the corresponding red arrow below).  *See, e.g.*, reverse engineered circuit schematic of the KCT8539S product showing the ground connection of the first shunt arm on the low noise amplifier die. For example, in the KCT8539S, the first shunt arm shown below includes a third switch circuit (indicated by the corresponding red arrow and bracket).

Claim	KCT8539S
	 *See, e.g.*, reverse engineered circuit schematic of the KCT8539S product showing an expanded view of the first shunt arm, identifying the third switch circuit on the low noise amplifier die. *See also*, 1[A].

Claim	KCT8539S
7[pre]. A method for operating a radio-frequency (RF) device, the method comprising:	To the extent that the preamble of claim 7 is limiting, the KCT8539S performs a method for operating a radio-frequency (RF) device, comprising the steps shown below and for claim elements 7[A]-7[C]. For example, the KCT8539S product description below states that the KCT8539S is an "RF Front-end Module" which "incorporates key RF functionality needed for IEEE 802.11a/n/ac/ax WLAN systems operating in the 5.15-5.85GHz range."[3]  KCT8539S **5GHz 802.11ax RF Front-End Module** **Introduction** KCT8539S is a highly integrated RF Front-End Integrated Circuit incorporates key RF functionality needed for IEEE 802.11a/n/ac/ax WLAN systems operating in the 5.15-5.85GHz range. KCT8539S integrates a high-efficiency high-linearity power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated matching network, LO rejection, and harmonic filters all in one device. KCT8539S has simple and low-voltage control logic, and requires minimal external components. A power detector is also integrated for accurately monitoring of output power from the PA. KCT8539S is assembled in a compact, low-profile 3x3x0.85mm 16-lead LGA package. KCT8539S is the ideal RF front-end solution for implementing 5GHz high-power WLAN systems supporting multiple standards including 802.11a/n/ac/ax. *See, e.g.*, KCT8539S product description, https://perma.cc/DA7F-4CED.

[3] *See* https://perma.cc/DA7F-4CED.