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UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.

Before the Honorable MaryJoan McNamara
Administrative Law Judge

In the Matter of **CERTAIN WIRELESS FRONT-END MODULES AND DEVICES CONTAINING THE SAME**	Inv. No. 337-TA-1413

EXPERT REPORT OF DAVID RICKETTS REGARDING THE INVALIDITY OF U.S. PATENT NOS. 8,717,101 AND 9,917,563

Skyworks Ex 2005
Kangxi v. Skyworks
IPR2025-00372

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Table of Exhibits and Abbreviations

Abbr. (if any)	Document	Ex. No.	**Bates No.**
'563 Patent	U.S. Patent 9,917,563	Ex.1001	KCT-ITC_0775201-KCT-ITC_0775218
'101 Patent	U.S. Patent 8,717,101	Ex.1002	KCT-ITC_0775114-KCT-ITC_0775131
'563 Pros. History	Prosecution History for U.S. Patent 9,917,563	Ex.1003	N/A
Ishimaru	U.S. Patent Publication 2009/0212863	Ex.1004	KCT-ITC_0172741-KCT-ITC_0172747
Ichitsubo	U.S. Patent Publication 2004/0232982	Ex.1005	KCT-ITC_1001836-KCT-ITC_1001858
Harrison	Excerpts of Linden T. Harrison, Current Sources and Voltage References, A Design Reference for Electronics Engineers (Elsevier 2005)	Ex.1006	KCT-ITC_0171560-KCT-ITC_0171657
Marra	U.S. Patent Publication 2011/0025422	Ex.1007	KCT-ITC_0172895-KCT-ITC_0172913
Johnson	*Johnson*, "Silicon-Germanium BiCMOS HBT Technology for Wireless Power Amplifier Applications," IEEE J. Solid State Circuits, Vol. 39, No. 10 (Oct. 2004)	Ex.1008	KCT-ITC_0172001- KCT-ITC_0172010
Laplante	Excerpts of Laplante, Comprehensive Dictionary of Electrical Engineering (2d Ed. 2005)	Ex.1009	KCT-ITC_0179909-KCT-ITC_0180651
Doherty	U.S. Patent Publication No. 2011/0128078	Ex.1010	KCT-ITC_0172929-KCT-ITC_0172944
Gilbert	*Barrie Gilbert*, "Bipolar Current Mirrors", Chapter 6 *in* Tomazou *et al.*, Analog IC Design: The Current Mode Approach (Reprinted 2008)	Ex.1011	KCT-ITC_0172179-KCT-ITC_0172290
Gray	Excerpts of Gray *et al.*, Analysis and Design of Analog Integrated Circuits (5th Ed. 2009)	Ex.1012	KCT-ITC_1001660-KCT-ITC_1001765
Grebene	Excerpts of Grebene, Bipolar and MOS Analog Integrated Circuit Design (2003)	Ex.1013	KCT-ITC_0180795
Illingworth	Excerpts of Illingworth, Dictionary of Electronics (3d Ed. 1998)	Ex.1014	KCT-ITC_0171658-KCT-ITC_0171663
Munford Dec.	Declaration of June Ann Munford	Ex.1015	N/A
TriQuint	TriQuint Semiconductor, Application Note TVS Protection and Bias Sequencing for HBT Amplifiers, p. 1 (June 2009)	Ex.1016	KCT-ITC_0172403-KCT-ITC_0172413

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Akagi	Certified Translation of Japanese Patent Application Publication No. JP 2009-283991	Ex.1017	KCT-ITC_0171936-KCT-ITC_0171966
Hedberg	U.S. Patent No. 6,831,517	Ex.1018	KCT-ITC_0173492-KCT-ITC_0173506
Joint C.C. Chart	Joint Claim Construction Chart in ITC Inv. No. 337-TA-1413	Ex.1019	N/A
Gilbert Biography	VintageTek biography, Barrie Gilbert, available at https://vintagetek.org/barrie-gilbert/	Ex.1020	N/A
Diels	*Diels,* Single-Package Integration of RF Blocks for a 5 GHz WLAN Application, IEEE Transactions On Advanced Packaging, Vol. 24, No. 3, (August 2001)	Ex.1021	KCT-ITC_1001650-KCT-ITC_1001657
Horowitz	*Horowitz,* Elementary Electricity and Electronics, Component by Component, (1986)	Ex.1022	KCT-ITC_0201298-KCT-ITC_0201447
Yanjun	*Yanjun,* "A 2.4-GHz SiGe HBT power amplifier with bias current controlling circuit", Chinese Institute of Electronics, Journal of Semiconductors, Vol. 30, No. 5, (May 2009)	Ex.1023	KCT-ITC_0174202-KCT-ITC_0174204
Resp. Markman Br.	Respondents' Markman Briefs in ITC Inv. No. 337-TA-1413	Ex.1024	N/A
Fourth Supplemental R&O to KCT's First Set of Interrogatories	Complainants' Fourth Supplemental Responses and Objections to Respondents Grand Chip Labs, Inc.'s and Kangxi Communication Technologies (Shanghai) Co., Ltd.'s First Set of Interrogatories to Complainants (NOS. 1-21)	Ex.1025	N/A
Chyurlia Dep. Tr.	Deposition Transcript of Peter Chyurlia, Ph.D. (February 19, 2025)	Ex.1026	N/A
'224 Patent	U.S. Patent No. 8,260,224	Ex.1027	KCT-ITC_0173887-KCT-ITC_0173902
Collelo	*Collelo,* "Skyworks' RF Chips are key components in today's most popular smartphones.", Morningstar Equity Research (July 31, 2013)	Ex.1028	Skyworks_ITC_000018682-Skyworks_ITC_000018701
Huang	*Huang,* "A Highly Integrated Single Chip 5-6 GHz Front-End IC Based on SiGe BiCMOS that Enhances 802.11ac WLAN Radio Front-End Designs", IEEE Radio Frequency Integrated Circuits Symposium, (2015)	Ex.1029	Skyworks_ITC_000019823-Skyworks_ITC_000019826

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Huang II	*Huang,* "A Compact 5-6 GHz T/R Module Based on SiGe BiCMOS and SOI that Enhances 256 QAM 802.11ac WLAN Radio Front-End Designs", IEEE (2014)	Ex.1030	Skyworks_ITC_000019815-Skyworks_ITC_000019818
Huang III	*Huang,* "A Highly Integrated Dual-Band SiGe Power Amplifier that Enables 256 QAM 802.11ac WLAN Radio Front-End Designs", IEEE Radio Frequency Integrated Circuits Symposium (2012)	Ex.1031	Skyworks_ITC_000019819-Skyworks_ITC_000019822
Huang IV	*Huang,* "A Highly Integrated Single Chip 5-6 GHz Front-End IC Based on SiGe BiCMOS that Enhances 802.11ac WLAN Radio Front-End Designs", IEEE Radio Frequency Integrated Circuits Symposium (2015)	Ex.1032	Skyworks_ITC_000019823-Skyworks_ITC_000019826
Huang V	*Huang,* "A Multimode 5-6 GHz SiGe BiCMOS PA Design Powers Emerging Wireless LAN Radio Standards", IEEE (2017)	Ex.1033	Skyworks_ITC_000019827-Skyworks_ITC_000019830
Huang VI	*Huang,* "A Multimode SiGe BiCMOS 5-6 GHz Front-End IC that Enables 802.11ac Wave 2 and 802.11ax Wireless LAN Front-End Designs", The Electrochemical Society, Vol. 75, No. 151, (2016)	Ex.1034	Skyworks_ITC_000019831-Skyworks_ITC_000019840
Chen	*Chen,* "On the Characterization of Thermal Coupling Resistance in a Current Mirror", IEEE Radio Frequency Integrated Circuits Symposium (2016)	Ex.1035	Skyworks_ITC_000019873-Skyworks_ITC_000019876
Huang VII	*Huang,* "Novel Silicon-on-Insulator SP5T Switch-LNA Front-End IC Enabling Concurrent Dual-band 256-QAM 802.11ac WLAN Radio Operations", IEEE Radio Frequency Integrated Cicruits Symposium (2013)	Ex.1036	Skyworks_ITC_000019877-Skyworks_ITC_000019880
RFMD	RFMD Design Application Note – AN035, Gain Block Active Bias Circuit (2002)	Ex.1037	Skyworks_ITC_000110940-Skyworks_ITC_000110946
Gray II	Excerpts of Gray *et al.*, Analysis and Design of Analog Integrated Circuits (5th Ed. 2009)	Ex.1038	Skyworks_ITC_000018918-Skyworks_ITC_000019814[1]

[1] Given Gray's length, I include as an exhibit the relevant excerpted portion.

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Bolton	*Bolton,* "SWKS: Simply the Best Positioned Supplier in the Wireless Front-End; Initiating Coverage with a Buy", Needham & Company, LLC (June 30, 2010)	Ex.1039	Skyworks_ITC_000018594-Skyworks_ITC_000018617
--	*Skyworks Solutions, Inc.,* "Skyworks unveils family of front-end solutions", Microwave Journal (February 28, 2012)	Ex.1040	Skyworks_ITC_000018917
--	*Skyworks Solutions, Inc.,* "Skyworks ramps GPS/GNSS solutions for Samsung", Microwave Journal (February 3, 2012)	Ex.1041	Skyworks_ITC_000018916
Bylund	*Bylund,* "What Makes Skyworks Solutions One of America's Best Companies" (February 27, 2013)	Ex.1042	Skyworks_ITC_000018660-Skyworks_ITC_000018665
Caplinger	*Caplinger,* "How Skyworks Solutions Soared 39% Since Mid-October (Hint: It's Not Just Apple)" (November 17, 2014)	Ex.1043	Skyworks_ITC_000018586-Skyworks_ITC_000018589
Chen II	*Chen,* "America's Best Managed Companies", Forbes	Ex.1044	Skyworks_ITC_000018573-Skyworks_ITC_000018585
--	"Skyworks Upgraded to Strong Buy on Healthy Q4 Results", Zacks Equity Research (November 11, 2024)	Ex.1045	Skyworks_ITC_000018657-Skyworks_ITC_000018659
--	*Skyworks Solutions, Inc.,* "Skyworks Receives Best Vendor and Outstanding Delivery Awards from ZTE" (September 18, 2012)	Ex.1046	Skyworks_ITC_000018655-Skyworks_ITC_000018656
--	"High Power FEMs for Ultra-fast Wi-Fi 6E applications", Electronics360 News Desk (February 10, 2021)	Ex.1047	Skyworks_ITC_000110938-Skyworks_ITC_000110939
--	"High Power front-end modules for Wi-Fi 6 applications from Skyworks", Electronics360 News Desk (February 26, 2020)	Ex.1048	Skyworks_ITC_000110947-Skyworks_ITC_000110948
'579 Patent	U.S. Patent No. 9,450,579	Ex.1049	KCT-ITC_0775150-KCT-ITC_0775167
DI Stipulation	Representative Domestic Industry Products Stipulation	Ex.1050	N/A
Ayoub Dep. Tr.	Deposition Transcript of Miriam Hanna Ayoub (February 14, 2025)	Ex.1051	N/A
Zhao Dep. Tr.	Deposition Transcript of Huan (Steve) Zhao (January 30, 2025)	Ex.1052	N/A
Yoon 2007	*Yoon,* "Static and Dynamic Error Vector Magnitude Behavior of 2.4-GHz Power	Ex.1053	KCT-ITC_0460550-KCT-ITC_0460554

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	Amplifier", IEEE Transactions on Microwave Theory and Techniques, Vol. 55, No. 4 (April 2007)		
Yoon 2009	*Yoon,* "2.4 GHz WLAN InGaP/GaAs Power Amplifier with Temperature Compensation Technique", ETRI Journal, Vol. 31, No. 5 (October 2009)	Ex.1054	N/A
'101 Pros. History	Prosecution History for U.S. Patent 8,717,101	Ex.1055	N/A
Hsieh-Yee Dec.	Declaration of Ingrid Hsieh-Yee, Ph.D.	Ex.1056	N/A
Li Dep. Tr.	Deposition Transcript of Ping Li (Rough) (February 26, 2025)	Ex.1057	N/A

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I. INTRODUCTION

1. I have been retained by counsel for Respondents, Kangxi Communication Technologies (Shanghai) Co., Ltd., and Grand Chip Labs, Inc. ("Respondents" or "KCT") as an expert in ITC Investigation No. 337-TA-1413. I expect to testify at the hearing and in deposition regarding the matters set forth in this report, if asked by the ALJ or the parties' attorneys.

2. For purposes of this report, I was asked to evaluate certain claims of U.S. Patent No. 8,717,101 (the "'101 Patent") and U.S. Patent No. 9,917,563 (the "'563 Patent") (the "Asserted Patents"). These include claims 1-2, 10-11, 17-18, and 20-22 of the '101 Patent and claims 14, 15, 17, and 20 of the '563 Patent (the "Asserted Claims"). Specifically, I was asked to assess various prior art documents to evaluate the invalidity of the Asserted Claims, consider and address Complainants Skyworks Solutions, Inc., Skyworks Solutions Canada, Inc. and Skyworks Global Pte. Ltd.'s ("Complainants" or "Skyworks") invalidity defenses, and ultimately opine on whether the Asserted Claims are invalid, among other things.

3. I expect that my testimony will include my opinion that claims 1-2, 10-11, 17-18, and 20-22 of the '101 Patent and 14, 15, 17, and claims 20 of the '563 Patent are invalid. I further expect to testify regarding the prosecution of the Asserted Patent, the knowledge of a person of ordinary skill in the art ("POSITA") at the time of the invention of the Asserted Patents, the state of the art the time of the invention of the Asserted Patents, and my own background, experience, and qualifications.

II. BACKGROUND AND QUALIFICATIONS

4. In this section, I provide a summary of my relevant qualifications and professional experiences pertinent to the technology of the Asserted Claims. A more fulsome

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listing of my qualifications and professional experiences is provided in my curriculum vitae, attached this report as Appendix A.

5. I am currently Full Professor of Electrical and Computer Engineering at the North Carolina State University. In my position I conduct research and teach undergraduate and graduate students in the area of electrical and computer engineering. The courses I teach include Advanced Analog Integrated Circuit ("IC") Design, Radio System Design, Analog Circuit Laboratory and Power Management IC Design. I also lead a research group that conducts research and design of electrical and electronic circuits, including millimeter wave and microwave circuits and systems, wireless power transfer circuits, power electronics and nano-electronic and nano-photonic devices. I lead research in power electronics and power conversion integrated circuits. I have served in my current position since 2012.

6. I have collaborated with numerous industries in power electronics, wireless power, radio frequency circuits and others. During this time, I worked with engineers of varying experience, including those with 2-20 years, including engineers with 5 years of experience.

7. Prior to my current position, I served as an Assistant Professor of Electrical and Computer Engineering and held a courtesy appointment in the Materials Science Department at Carnegie Mellon University from 2006 to 2012. I taught undergraduate and graduate device physics, which included photovoltaic devices.

8. I received my B.S. and M.S. in Electrical Engineering in 1995 and 1997, respectively, from Worcester Polytechnic Institute in Worcester, Massachusetts. I received my Ph.D. in Electrical Engineering from Harvard University in Cambridge, Massachusetts in 2006.

9. Prior to entering academia, I worked as an engineer in private industry holding several engineering and managerial positions where I developed and oversaw the development of

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electrical and electronic circuits, including those related to power transfer, power conversion, and semiconductor design in wired and wireless circuits and systems.

10. From 1995 to 1999, I held a position as an engineer and senior engineer at American Power Conversion, where I designed uninterruptable power supplies (UPS), AC-DC and DC-DC converters. The AC-DC converters were originally developed for solar power grids to convert DC power from solar panels to AC energy to power homes. The technology also included methods to transfer energy from the solar panels directly to the grid, as well as microgrid, at home solar installations and voltage and current inverters. In addition, I worked on AC-DC and DC-DC converters as well as battery chargers.

11. From 1999 to 2001, I held a position as a Principal Consultant at Renaissance Design, Inc., where I designed power management ICs for DC-DC converters and DC-AC inverters.

12. From 2000 to 2002, I held a position as a Manager of New Product Development at ON Semiconductor Corp., where I was responsible for six product development teams including market analysis, business development, system design, integrated circuit design and testing. In that role I oversaw the development of over twenty power management ICs, also known as power ASICs, in bipolar, CMOS, and BiCMOS technologies. These ICs related to DC-DC converters among other power electronic circuits.

13. From 2002 to 2003, I held the position of Advanced System Engineering Manager at ON Semiconductor Corp., where I directed a team of system engineers to develop multi-phase power management ICs for Intel and AMD microprocessors. In and around this period I was designing power amplifiers, including those in SiGe HBT.

[redacted]

14. In 2006 I received my PhD on the topic of advanced oscillator topologies and radio frequency integrated circuits. My work on integrated circuit oscillators was included in the 2008 McGraw-Hill Yearbook of Science and Technology and discussed in Nature, the pre-eminent science journal. In addition, my work on advanced materials for circuits included the first Si-Ge shell-core nanowire oscillator on plastic.

15. Since 2006, I have conducted research at the forefront of radio frequency power amplifier design. I have published numerous journal and conference papers on power amplifiers, with multiple designs being the best reported in the world at the date of publication. I have experience in design and testing of power amplifiers in various technologies, such as Silicon Germanium, complementary metal oxide semiconductor (CMOS), Silicon on Insulator, etc.

16. I have published two books, at least 50 academic journal papers and 78 conference papers, as shown in my curriculum vitae, in RF systems, wireless power transfer circuits, magnetic circuits and materials, analog circuits, RF circuits and nanoscale devices.

17. I am the recipient of the National Science Foundation CAREER award for work in emerging magnetic devices known as spin-torque oscillators. I also received the Defense Advanced Research Projects Young Faculty Award for my work in emerging magnetic devices.

III. PRIOR EXPERT TESTIMONY AND COMPENSATION

18. I have previously testified as an expert at trial or by deposition. Included in Appendix B is a listing of all other cases in which I have so testified during the previous six (6) years.

19. I am being compensated at my rate of $725 per hour for my services. I also am compensated for my expenses in relation to this matter. My compensation is not dependent on or

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related in any manner to the outcome of this litigation or my opinions in this report. I have no financial interest whatsoever in the outcome of this litigation.

IV. FACTS AND DATA CONSIDERED IN CONNECTION WITH THIS REPORT

20. I have reviewed and considered in connection with forming the opinions I provide in this report all materials cited herein and listed in the Table of Abbreviations as well as those documents listed in Appendix C.

V. RELEVANT LEGAL STANDARDS

21. I am not an attorney and have not been asked to offer my opinion on the law. I have been informed of the applicable legal standards set forth in this report. The applicable legal standards that I have applied are set out in Appendix D.

VI. OVERVIEW OF RELEVANT TECHNOLOGY

A. RF Device Basics

22. The '101 and '563 Patents concern components or circuits found in many RF devices, namely the PA and its accompanying bias circuit. *See* '101 Patent 1:16-17 ("invention relates to electronic systems, and in particular, to radio frequency (RF) electronics").[2]

23. The RF power amplifier and bias circuit are typically used in connection with the device's antenna. Antennas transmit and receive RF signals.[3]

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[2] The '101 and '563 Patents share a common specification, but differ in their claims. To the extent I provide a citation to column(s) and line number(s) of one patent, it should be understood that the other patent has the same content, but at slightly different columns and line numbers. For brevity, I typically cite to only one.

[3] RF signals are alternating current ("AC") signals, in which a single waveform (*i.e.* ∿) is referred to as a "cycle" and the number of cycles per second is called the "frequency." This frequency is measured in "Hertz" (Hz) where 1Hz = 1 cycle/second. The RF signals also have an "amplitude" which is the height of each signal peak when plotted on a voltage versus time plot. An RF signal itself can be thought of as a high-frequency carrier frequency (*e.g.,* 2.5 Gigahertz) modulated or encoded with data. The RF carrier is modulated (*e.g.,* the frequency or amplitude is changed) to "carry" the information/data of interest to the device. That process is outside the

[redacted]

24. Significantly, many of the antennas in RF systems undertake only one function – transmit or receive – at a time. [4] During transmit periods, the antenna and its supporting circuitry broadcast an outbound data-encoded signal to the world. During receive periods, the antenna and its supporting circuitry cease broadcasting, and instead "listen" for and pick up inbound data-encoded RF signals, in from the air. The antenna does one thing at a time. The antenna and its supporting electronics must therefore toggle between these two modes – transmitting mode and receiving mode – many hundreds or even thousands of times per second.

B. The Power Amplifier

25. When a typical wireless device is transmitting signals (*i.e.*, in sending or "transmit" mode"), the microprocessor in the underlying device, followed by upstream components within the device, passes a data-encoded RF signal to a power amplifier situated near the device antenna. The PA, as the name suggests, amplifies the data-encoded RF signal to a power level (or amplitude) suitable for broadcast by the antenna, so as to increase its transmission range. *See* '101 Patent at 1:19-22 ("RF power amplifiers can be used to boost the power of a RF signal having a relatively low power. Thereafter, the boosted RF signal can be used for a variety of purposes, included driving the antenna of a transmitter."). The amplified RF signal is then sent to (and thus drives) the device's antenna, which radiates the signal into the surrounding environment, to be picked-up and received by another antenna on another wireless device.

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scope of this case. The patents-in-suit concern the amplification of the RF signals, but are agnostic about the format or information those RF signals happen to carry.

[4] The reason for this is because attempting to simultaneously transmit and receive signals through the same antenna could cause significant interference in both the incoming and outgoing RF signals, degrade the encoded data, and damage sensitive components.

[redacted]

26. Many contemporary devices turn the PA "on" when needed (meaning when the system and antenna are in transmit mode, amplifying a system-generated RF signal and sending it out via the antenna) and turn the PA "off" and let it sit dormant when not needed (such as when the system and antenna are in receive mode, listening for and picking up inbound RF signals from others over the air). The PA is turned on and off, just as the system toggles between transmit mode and receive mode, hundreds or thousands of times per second. This is done for a number reasons, including at least to reduce power consumption of the system.

27. The primary – in many cases, only – component in the PA is a core transistor, commonly a bipolar junction transistor ("BJT").[5] For purposes of the '101 and '563 Patents, a transistor can be thought of as a device that, when properly turned on and placed in an operational state ("enabled"), takes in a small signal and generates an amplified version of the input signal. A PA is an amplifier that has been optimized to produce high output power and often high efficiency at that output power.

28. The on/off switching of the PA can be done by turning on and off the PA's "bias current" ("I_{BIAS}"), as the PA does not operate (or consume substantial power) when it is not biased. [6] The PA is supplied with a DC bias, e.g. I_{BIAS}, that takes the underlying transistor from a non-operational state ("off") to an operational state ("on"). Once enabled, and thus turned on, the PA is able to begin amplifying whatever signal (e.g. outbound RF signal) is fed into it. *See* '101 Patent at 4:12-19.

[5] A POSITA understood that some PAs also used something called a field effect transistor ("FET"). Because the patents use a BJT for their preferred embodiment, and the claims are directed to control/correction/bias currents, I focus on the BJT.

[6] Current is measured in amperes and abbreviated "I." Voltages are measured in volts and abbreviated "V."

[redacted]

VII. OVERVIEW OF THE ASSERTED PATENTS

A. Problem and Solution

29. At the time of the invention of the '101 and '563 Patents, enablement – *i.e.* the turning on the PA – that was commonly accomplished through a simple on/off signal.[7] When the system wanted the PA on, it generated a fixed, flat, "enable" voltage signal. An ancillary "biasing circuit" (called a "bias block"), adjacent to the PA, took the fixed, flat enable voltage and generated a corresponding fixed, flat bias current (I_{BIAS}), which it then fed to the PA. The PA turned on. Now in transmit mode, the PA was fed an outbound RF signal. The PA amplified the RF signal.

30. The amplified signal was fed (via a RF switch) to the antenna. The antenna received it and radiated (broadcast) it out to the world. Some short time later, the system stopped transmitting data, and the enable signal was set back to zero. The bias block stopped delivering I_{BIAS}. The PA turned off. The system toggled to receive mode. The transmit side of the system sat idle, waiting for the next "on" enable signal.

31. One problem with this approach was that many conventional RF PAs do not achieve full amplification (meaning the desired ratio of the output amplitude versus the input amplitude, also known in the art as "gain") instantaneously when turned on. As the '101 Patent explains:

> [S]hortly after a power amplifier is enabled, absent compensation[,] the current of a primary biasing circuit can come up slow due to thermal effects, and the power amplifier's gain can be low.

[7] Not always, as I will show as part of my prior art invalidity opinions. However, this is generally speaking from the perspective of the '101/'563 Patents, at the priority date, without the inventor's apparent knowledge of all the prior art.

[redacted]

'101 Patent at 4:32-35; *see also* 8:42-45 ("a variation in gain of the power amplifier [] can occur shortly after the power amplifier is enabled.").

32. That is, during the first several microseconds after being turned on (*i.e.* after the enabling I_{BIAS} is supplied), the amplification gain of the transistor/amplifier starts out low before rising. It takes time (*e.g.* 5-50 µS, depending on the PA) for the gain to reach steady-state. During this ramp-up period, the power amplifier is amplifying the subject RF signal at a gain/amplification level less than the ultimate steady state. *See, e.g.*, '101 Patent 4:28-42.

33. The power amplifier may under-amplify the RF signal for several or tens of microseconds while it warms up – introducing distortion and non-linearity in the signal sent to the antenna. This can be a problem. *See* '101 Patent at 2:28-33 ("It can be important manage the amplification of a RF signal, as amplifying the RF signal to an incorrect power level can cause a wireless device to transmit out of band. There is [therefore] a need for improved power amplifier systems. Furthermore, there is a need for improving power amplifier biasing.").

34. The inventors' alleged solution was to "shape" the PA's I_{BIAS} current, changing it over time while "on" (*i.e.* rendering it not fixed/flat) to account for – and counteract – the natural shape of the gain response of the PA during start-up. '101 Patent 4:32-35 ("shortly after a power amplifier is enabled, absent compensation[,] the current of a primary biasing circuit can come up slow due to thermal effects, and the power amplifier's gain can be low.") Specifically, the inventors' solution was to boost the enabling I_{BIAS} current for a short time after enablement, compensating the gain of the PA to compensate for the PA's gain lag. '101 Patent 4:28-32 ("The correction current can be used to adjust the magnitude of the bias current so as to compensate for a variation in gain of the power amplifier over time when the power amplifier is transitioned from a disabled state to an enabled state."); 4:37-39 ("a current boost can be provided to the

power amplifier so as to provide the power amplifier with a substantially flat gain response versus time."). By briefly over-biasing the PA, pushing up the gain during the warm-up period, the net effect would be a near-flat gain and output over time. *Id.* The initially-*high*-then-steady shape of the I_{BIAS} would, for a sufficient duration (*i.e.* long enough to achieve the "substantially flat gain response versus time"), counteract the initially-*low*-then-steady shape of the PA's uncompensated/natural gain response. *Id.* at 4:32-35 (gain "come[s] up slow"); 9:56-60 (same); 8:42-45 (similar); 4:37-39 (compensatory "current boost"); 9:60-64 (same). The two shapes would (roughly) cancel each other. The resulting goal was "a substantially flat gain response versus time." '101 at 4:38-39. "Correcting for gain variation in the power amplifier can improve the power amplifier's performance." *Id.* at 4:39-41.[8]

35. In order to shape the bias current, the inventors developed the notion of a "correction current" ($I_{CORRECTION}$) that would combine with, and thus add shape to, the fixed, flat bias current that would conventionally emerge from the bias circuitry. Figure 4 (annotated below) showed the invention:

[8] One metric of improved gain flatness is the PA's dynamic error vector magnitude (EVM), but this metric is not at issue for the claim construction disputes on which I opine.

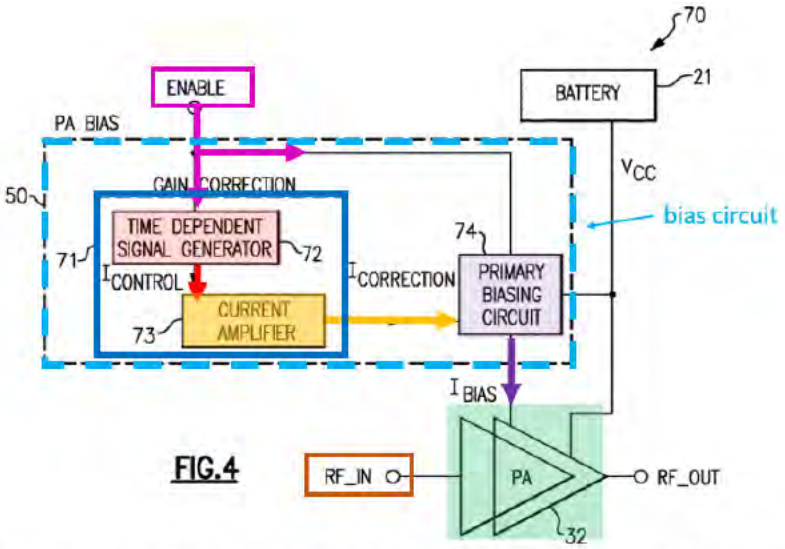


FIG.4

36. The bias circuit (50) consists of a conventional primary bias circuit (74) driven by a conventional, unmodified enable signal, plus a supplemental "gain correction circuit" (71) that generates the supplemental $I_{CORRECTION}$ to add shape to the I_{BIAS} that emerges from the primary bias circuit (74). That $I_{CORRECTION}$ is generated within the gain correction circuit by using a "time dependent signal generator" (72) to generate a small version of the desired shape ($I_{CONTROL}$), and then scaling up that shape to an appropriate amplitude using a current amplifier (73). In sum, in operation, the enable signal (pink arrow) is activated at startup, switching from off to on. The time dependent signal generator, in response, takes that flat "on" signal and generates a shaped control current (red arrow) that is received by current amplifier (gold). The current amplifier (gold) scales up the control current into a correction current (gold arrow). The primary biasing circuit (purple) receives the shaped correction current and correspondingly adjusts the magnitude of the bias current (purple arrow) so as to compensate for a variation in gain of the power amplifier during startup. The short-term "boost" in bias current helps overcome the PA's low gain during startup.

37. Figure 5 shows a more specific embodiment of the general structure set forth in Fig. 4. The inventors use a resistor-capacitor circuit (82) to generate the time-dependent signal

[redacted]

that provides an initial boost before settling into a steady state. Amplifier 83, comprised of a "current mirror" configuration of transistors, scales up the $I_{CONTROL}$ into a larger version, $I_{CORRECTION}$. That $I_{CORRECTION}$, in turn, combines with the base current generated in primary biasing circuit (84) to generate the shaped I_{BIAS}.

38. Notably, the inventors sought to co-locate their new "shaping"/corrective PA bias block on the same semiconductor "die" as the PA. *See, e.g.,* '101 Patent, 8:50-63, 9:65-10:7, 10:62-11:6, 13:19-27, 14:7-13. A **die**, in the context of integrated circuits, is a small block of semiconducting material on which a given functional circuit is fabricated. Dies are commonly made of silicon or gallium arsenide. One or more dies, in turn, can be mounted on a common package substrate, with tiny jumper "bond' wires connecting points on the die to pins on the ultimate package.

B. Prosecution History of the Asserted Patents

1. Prosecution History of the '101 Patent

39. I note that the '101 Patent issued on May 6, 2014 from U.S. Patent Application No. 13/468,749, filed May 10, 2012. The '101 Patent claims priority to U.S. Provisional Application No. 61/486,186 filed on May 13, 2011.

40. During prosecution of the '101 Patent, the Applicant originally presented Claims 1-28. I note the Examiner rejected claims 1-3, 6-7, 12-14, 18-20, and 22-25 under Alon et al. (U.S. Patent No. 7,869,775), and claims 4-5, 8-11, 15-17, 21, and 26-28 were objected to as being dependent upon a rejected base claim. *See* '101 Patent File History, 55-57 (Non-Final Office Action (August 2, 2013) at 2-4).

41. Specifically, the Patent Office rejected the independent claims over prior art, but indicated that the dependent claims that recited a "current mirror" were allowable. EX-1002 88-

[redacted]

90. To overcome the rejection, the Applicant amended the independent claims to recite that the current amplifier also included a "current mirror." The amendment to Claim 1 is representative:

> 1. (Currently Amended) A power amplifier system comprising:
>
> a power amplifier configured to amplify a radio frequency (RF) signal; and
>
> a bias block for biasing the power amplifier, the bias block including a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current, a current amplifier configured to amplify the control current to generate a correction current, and a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current, the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled, the current amplifier including a current mirror.

'101 Patent File History, 38 (Amendment and Response to Office Action (October 31, 2013) at 2).

42. In response, the Examiner allowed the independent claims, asserting:

> Claims 1-3, 6-7, 9-14 are allowed over the prior art of record. The prior art of record considered individually or in combination, fails to fairly teach or suggest the claimed circuit comprising, among other limitations and unobvious limitations of "…the current amplifier including a current mirror" structurally and functionally interconnected with other limitations in the manner as cited in the claim.

'101 Patent File History, 25 (Notice of Allowance (December 24, 2013) at 2).

43. However, as shown below, creating a boost in bias current to compensate for the gain variation of a PA at startup, including using a current amplifier including a current mirror, was already known.

[redacted]

2. Prosecution History of the '563 Patent

44. I note that the '563 Patent issued on March 13, 2018 from U.S. Patent Application No. 15/377,842, filed December 13, 2016. The '563 Patent is a continuation of a series of patents leading back to U.S. Patent No. 8,717,101 Patent. The '563 Patent claims earliest priority to U.S. Provisional Application No. 61/486,186, filed May 13, 2011.

45. During prosecution of the '563 Patent, the Applicant originally presented 20 claims. Independent claim 1 was originally presented as follows:

> 1. A mobile device comprising:
>
> a transceiver configured to generate a radio frequency signal and a power amplifier enable signal;
>
> a power amplifier configured to provide amplification to the radio frequency signal, the power amplifier configured to receive a bias signal that biases the power amplifier; and
>
> a bias circuit configured to receive the power amplifier enable signal and to generate the bias signal, the bias circuit including a gain correction circuit configured to generate a correction current in response to activation of the power amplifier enable signal, and a primary biasing circuit configured to generate the bias signal based on the correction current and the power amplifier enable signal.

'563 Patent File History, 295 (Application (December 13, 2016) at 26).

46. The Examiner rejected Claims 1-20 of the '563 Patent for non-statutory double patenting over claims 1-20 of U.S. Patent No. 9,136,803.

[redacted]

> ***Double Patenting***
>
> Claims 1-20 are rejected on the ground of nonstatutory obviousness-type **double patenting** as being unpatentable over claims 1-20 of U.S. Patent No. 9,136,803. Although the conflicting claims are not identical, they are not patentably distinct from each other because all of the limitations of the present claims are present in the patented claims.

'563 Patent File History, 237 (Non-Final Office Action (February 27, 2017) at 2).

47. The Examiner also rejected Claims 1-6, 8-12, 14-17, 19 and 20 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Wakita et al. (U.S. Patent No. 8,692,619). *Id.*

48. In response, the Applicant amended as filed Claim 14 (which issued as claim 14) as follows:

> 14. (Currently Amended) A packaged module comprising:
>
> a package substrate; and
>
> an integrated circuit attached to the package substrate and including a power amplifier configured to provide amplification to a radio frequency signal and a bias circuit configured to receive a power amplifier enable signal and to generate a bias signal that biases the power amplifier, the bias circuit including a gain correction circuit configured to generate a control current ~~correction current~~ in response to activation of the power amplifier enable signal and to mirror the control current to generate a correction current, and a primary biasing circuit configured to generate the bias signal based on the correction current and the power amplifier enable signal.

'563 Patent File History, 58 (Amendment and Response to Office Action (May 16, 2017) at 4).

49. The applicant pointed to the entire claim element of "a bias circuit ... enable signal" to distinguish the prior art. *Id.* The applicant did not point to any particular features to explain what was missing in the art, nor did it make any clear and unmistakable statements about the meaning of any of the terms in the claim element identified. The applicant instead argued

[redacted]

that the prior art relied upon in the Office Action did not qualify as prior art based on its filing dates, which was accurate. In response, the examiner withdrew the rejections. *Id.* at 0064-65.

50. The Examiner subsequently allowed the claims, asserting that the prior art did not "fairly teach or suggest the claimed circuit ... to mirror the control current to generate a correction current ... structurally and functionally interconnected with other limitations in the manner cited in the claim." '563 Patent File History, 17-18 (Notice of Allowance (November 1, 2017) at 2-3). However, as shown below, creating a boost in bias current to compensate for the gain variation of a PA at startup, including mirroring currents to do so, was already known.

51. Although *Ishimaru* was disclosed during prosecution of the '563 Patent, the Examiner did not discuss, apply, or otherwise meaningfully address its disclosure. Thus, neither the same or similar combinations of prior art, nor the arguments set forth below, were before the examiner during prosecution.

C. Claim Construction of the Asserted Claims

52. I understand that a claim construction order has not yet been entered in this matter. I further understand that the parties have agreed to the construction of certain terms and have proposed competing constructions for other terms. My understanding of the various constructions is set forth in the table below.

DISPUTED CONSTRUCTIONS

Disputed Claim Term	Patent(s) and Claim(s)	Complainants' Final Proposed Construction	Respondents' Final Proposed Construction	Staff's Final Proposed Construction
"a current amplifier configured to amplify the control current to generate a	'101 patent, claims 1, 2, 10, 11, 21, 22	Plain meaning, which is "a current amplifier configured to **achieve a target gain** of a control current to generate	Plain meaning, which is "a current amplifier configured to **increase the control current** to	Plain meaning, which is "a current amplifier configured to **increase the control current** to

[redacted]

correction current"		a correction current"	generate a correction current"	generate a correction current"
"amplifying the control current using a current mirror of a current amplifier to generate a correction current"	'101 patent, claims 17, 18, 20	Plain meaning, which is "**achieving a target gain** of a control current, using a current mirror of a current amplifier, to generate a correction current"	Plain meaning, which is "**increasing the control current** using a current mirror of a current amplifier to generate a correction current"	Plain meaning, which is "**increasing the control current** using a current mirror of a current amplifier to generate a correction current"
"current mirror"	'101 patent, claims 1, 2, 10, 11, 17, 18, 20, 21, 22 '563 patent, claim 17	Plain meaning, which is "one or more circuits configured to mirror a current, which can be configured to achieve a target gain, **having at least two transistors with their base or gate terminals tied together**"	Plain meaning, which is "one or more circuits configured to mirror a current, which can be configured to achieve a target gain"	Plain meaning, which is "one or more circuits configured to mirror a current, which can be configured to achieve a target gain"
"integrated circuit"	'563 patent, claims 14, 15, 17, 20	Plain meaning, which is "a circuit made up of multiple interconnected electronic components **integrated on one or more dies**"	Plain meaning, which is "a circuit made up of multiple interconnected electronic components integrated **on a die**"	Plain meaning, which is "a circuit made up of multiple interconnected electronic components integrated **on one or more dies**"

AGREED CONSTRUCTIONS

"a gain correction circuit configured to generate a control current in response to activation of the power amplifier enable signal	'563 patent, claims 14, 15, 17, 20	Plain meaning, which is "a circuit for gain correction of the power amplifier configured to generate a control current in response to activation of the power amplifier enable signal and to

[redacted]

and to mirror the control current to generate a correction current"		mirror the control current to generate a correction current"
"time dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current" / "shaping an enable signal using a time-dependent signal generator to generate the control current"	'101 patent, claims 1, 2, 10, 11, 17, 18, 20, 21, 22	Plain meaning, which is "a circuit configured to change an enable signal of the power amplifier to achieve a desired shape of a control current, where the control current changes based on time" / "changing an enable signal using a circuit to achieve a desired shape of a control current, where the control current changes based on time"

53. In this report, I have based my opinions on each of the claim constructions in the above tables. Where there are competing constructions, I have explained in my opinions below how the prior art satisfies both constructions. For terms not listed in the above tables, I have based my opinions on the plain and ordinary meaning of the term as would have been understood by a POSITA in the context of the Asserted Patents.

VIII. STATE OF THE ART AT THE TIME OF INVENTION

A. Priority Date of the Asserted Claims

54. The '563 Patent and '101 Patent claim priority to May 13, 2011. '101 Patent 1:7-21; '563 Patent 1:7-11 (provisional application 61/486,186, filed on May 13, 2011.) Solely for the purposes of the Report, I have been instructed to assume the priority date for the Asserted Patents is May 13, 2011.

B. Person of Ordinary Skill in the Art

55. In defining "a person of ordinary skill in the art" ("POSITA"), I have been advised to consider factors such as (1) the levels of education and experience of the inventor and other persons actively working in the field; (2) the types of problems encountered in the field; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; and (5) the

[redacted]

sophistication of the technology. I further understand that a POSITA is presumed to think along conventional lines; having ordinary creativity and not being an automaton. As such, a POSITA would be able to fit the teachings of multiple prior art references together like a puzzle and have the capability of understanding the scientific and engineering principles applicable to the pertinent art. I understand that a POSITA is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

56. In my opinion, with respect to the '563 and '101 Patents, a POSITA would have been someone knowledgeable and familiar with analog and RF circuit design. A POSITA would have gained knowledge of these concepts through a mixture of training and work experience, such as by having at least a bachelor's degree in electrical engineering, or related field, and at least two to three years of training or additional work experience in the area of RF electronics, or a related field. Additional hands-on and design experience could compensate for less formal education, and vice versa, at the time of the priority date of each patent. The knowledge and skill of a POSITA is further reflected in the prior art references themselves, as well as the State of the Art, discussed below.

57. As of May 2011, my education and experience made me at least a POSITA, and the opinions expressed in this Report are informed by my knowledge of the state of the art and the level of ordinary skill in the art of persons within my field during the relevant timeframe (*i.e.*, May 2011).

58. For purposes of this Report, in general, and unless otherwise noted, my statements and opinions, such as those regarding my experience and the understanding of a POSITA generally, reflect the knowledge that existed in the field as of May 2011. Unless otherwise stated,

[redacted]

when I provide my understanding and analysis below, it is consistent with the level of a POSITA prior to May 2011.

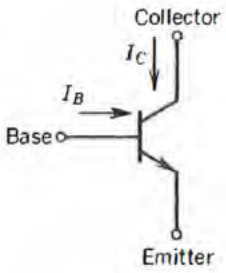
59. I would expect that my analyses or opinions in this report would not substantially change if it were found that the level of ordinary skill in the art for the Asserted Patents is found to be slightly higher or lower than the level I articulate above.

C. State of the Art

60. In the following section I describe the state of the art for power amplifier systems as of May 13, 2011. The prior art references, and the discussions of what was known to a POSITA, provide the factual support for the general description of the state of the art at the time of the invention, and provide additional motivation to modify or combine the reference.

1. The Gain Variation of Power Amplifier at Startup Was Known

61. A POSITA in May 2011 understood that a PA was commonly implemented using one or more transistors (such as a bipolar junction transistor (BJT)) to amplify an RF signal. A BJT transistor has three terminals, "collector", "base" and "emitter" labelled as such in the figure below.



Grebene 58. The biasing and operation of such transistors to amplify a signal applied to the base of the transistor was well known. Horowitz 218, 220-228; Harrison 47-50, 52-55; Illingworth 38; *see, e.g.*:

[redacted]

> Transistor circuits are usually designed to amplify an ac input voltage rather than dc current. In this type of arrangement, the ac is superimposed on the dc. The dc is used to establish specific quiescent emitter and collector currents. These *bias currents* should set the idling voltage (voltage before ac is applied to the circuit) at the collector at one-half of E_{CC}. Because the collector voltage, V_C, is equal to $E_{CC} - I_C R_C$, V_C should be idling at about $E_{CC}/2$.

Horowitz 218.

> Bias or idling conditions are established when there is no ac voltage at the input of the circuit, or $E_{IN} = 0$. At this time, only the dc emitter supply voltage less the base-emitter voltage is across R_C the only component in this circuit that is outside of the transistor.

Horowitz 220.

> As was true in the common-base circuit, it is also desirable here to let the voltage at the collector terminal in this circuit idle at $E_{cc}/2$ volts. To do this, the idling voltage across R_c must be equal to half of the supply voltage, or $I_C R_C = E_{CC}/2$. Because I_C is related to I_B, I_B is set by the designer of the circuit to equal the desired le divided by beta. I_B can, of course, be set by using the proper base resistor, R_B, in the circuit. Ac signal voltage is usually fed through a capacitor to the base and applied between the base and emitter to the transistor. The input voltage varies the base and hence collector current in step with the cyclic variations of the ac. A magnified version of the ac input voltage is developed across the collector resistor by the ac collector current flowing through it.

Horowitz 222-223.

> The ac input signal adds a variable current to the dc idling current in the base. It is amplified by the transistor so that a magnified version of the ac input is across R_C. When the voltage at the base is at its peak in the cycle, the collector current is also at its peak. Because the voltage across R_C is the product of the collector current with R_C, this voltage is also at its maximum level.

Horowitz 222-224.

62. A POSITA in May 2011 was well aware that the gain response of a PA "varies with temperature" and that "at temperatures below the [PA's] steady-state operating temperature," the gain of a PA will be lower than it would be at the steady-state operating temperature (assuming the same bias signal). Doherty ¶¶5-6; *see, e.g.*:

[redacted]

> Although various fluctuations in physical characteristics caused by changing operating conditions can affect the gain or phase response of the PA, the temperature of the PA has a profound affect on its response.

Doherty ¶5.

> The gain and phase response of a PA varies with temperature such that at temperatures below the steady-state operating temperature, the actual gain exhibited by the PA having a specific bias signal applied thereto will be less than the expected gain of the PA at steady-state operating temperatures in response to that same specific bias signal, and correspondingly, the actual phase response at a specific bias may be different from the expected phase response of the PA at steady-state operating temperatures. As the PA warms up, the actual gain of the PA increases to its expected value while the phase response of the PA approaches an expected steady-state phase response. In order to achieve a desired target operating gain and phase response, a standard or steady-state bias level can be applied to the PA while the PA is operating at its steady-state operating temperature, but at temperatures below the steady-state operating temperature, the standard bias level is insufficient to achieve the target operating response.

Doherty ¶6. It was known that, as the PA warms up, the gain of the PA approaches its steady-state expected value. A POSITA was thus aware that "at temperatures below the steady-state operating temperature, the standard bias level is insufficient to achieve the target operating response." Doherty ¶6. This problem existed in conditions where "the PA's temperature fluctuates between idle temperatures and its steady-state operating temperature" and this fluctuation "causes variations in the gain and phase of the PA away from the target operating response." Doherty ¶8; *see, e.g.*:

> Due to its profound affect on the gain and phase response of the PA, one main contributor to unwanted changes in a PA's response and dynamic EVM is thermal changes of the PA caused by dynamic heating effects. Under pulsed conditions, the PA's temperature fluctuates between idle temperatures and its steady-state operating temperature, which in turn causes variations in the gain and phase of the PA away from the target operating response. One particular situation for which this can occur, is when the PA receives an RF signal data burst, after it has remained idle long enough that its temperature has fallen below its steady-state operating temperature. In one standard RF transmitter application, a TX enable is received 500 ns to 1 us before the RF signal data to be transmitted is received. If the PA is sufficiently small, this time period is long enough to allow the PA to turn on and warm-up to its steady-state operating temperature. If the PA is large, the time period

[redacted]

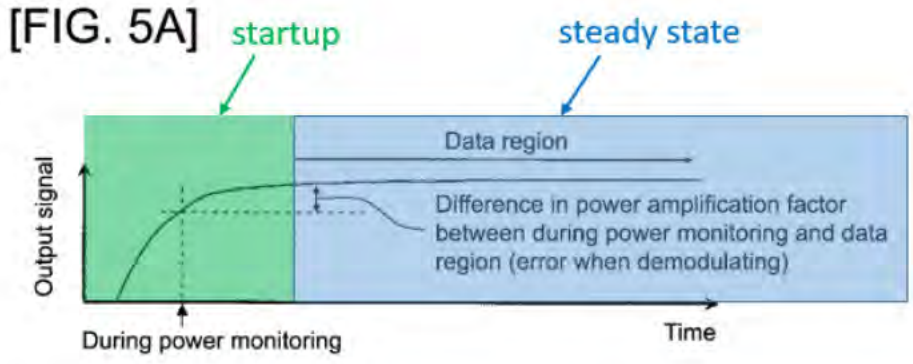
> between receipt of the Tx enable and the receipt of RF signal data may be shorter than the time the PA needs to reach its steady-state operating temperature. In this case, some of the RF signal data may be received and amplified while the PA is in a thermally changing state during which the gain and phase response of the amplifier is also changing. This occurs primarily at the beginning of the pulse sequence, when the PA is coolest and hence at a temperature farthest from its steady-state operating temperature.

Doherty ¶8.

63. Further, it was known that a PA was conventionally operated in bursts, turning it on just before, and off just after, transmission of a signal, "in order to suppress power consumption" when not in use. Akagi ¶4; *see, e.g.*:

> In a communication device such as a wireless LAN, it is not such that an input signal is not always ON at the time of transmission in a system, but such that a burst operation is performed wherein an ON state in which the input signal is input and an OFF state in which the input signal is not input are repeated. In an off state in which an input signal is not input, a usage method in which a high-frequency power amplifier is turned off by being synchronized to a burst operation is often used in order to suppress power consumption of a system. In the conventional high-frequency power amplifier in FIG. 4, the DC power source E1 is turned on and off by being synchronized to the burst operation, but the DC power source E2 is always on.

Akagi ¶4. Consistent with Doherty discussed above, it was well known that the gain (or "power amplification factor") of the PA is lower at startup (green) than at steady state (blue), as shown below:



Akagi Fig. 5A (annotated), ¶6.

[redacted]

64. A POSITA also knew that this issue of the PA gain being too low on startup could be addressed using resistor-capacitor based "speedup" circuits to provide a temporary boost to the I_{BIAS} supplied to a PA. For example, Doherty described that a "common approach" to avoid "unwanted ... gain variations" in the PA was to "to speed up the gain ... response of the PA by applying an external resistor and speed-up capacitor to provide more forward [bias] current earlier to the PA." Doherty ¶9; *see, e.g.*:

> In order to ensure low dynamic EVM and an output signal that is not distorted by unwanted gain and phase variations, a PA is generally not used unless it is thermally stable. A common approach to avoid the problem of dynamic EVM is simply to wait until a PA is thermally stable before using it to amplify the signal. A second common approach is to speed up the gain and phase response of the PA by applying an external resistor and speed-up capacitor to provide more forward current earlier to the PA. Although the speed-up capacitor can improve the time response of the PA, as a passive mechanism it cannot provide the additional forward current until the RF input signal itself arrives. Consequently, the beginning of the RF signal data will suffer from some amount of dynamic EVM and the additional current may not be sufficient to bring the PA into a thermally stable state at a desired rate.

Doherty ¶9. Likewise, Akagi described that in "the conventional high-frequency power amplifier", a resistor and capacitor circuit (Akagi Fig. 4, R1, C1) is generally used so that "immediately after the DC power source E1 is turned on, an instantaneous current flows into the bias circuit" to cause the PA's "bias point" to be "set to be high, and the power amplification factor becomes high" to provide "power amplification factor correction" to compensate for the thermal properties of the PA. Akagi ¶7, Fig. 4 (R1, C1); *see, e.g.*:

> Thus, in the conventional high-frequency power amplifier, as illustrated in FIG. 4, a method wherein a circuit in which the resistor R1 and the capacitor C1 as an example of a capacitance element are connected in parallel is inserted in series between the DC power source E1 and the bias circuit 130 is generally used. In this case, immediately after the DC power source E1 is turned on, an instantaneous current flows into the bias circuit 130 via the capacitance 1, and the same voltage as the DC voltage of the DC power source E1 is applied to the bias circuit 130. The voltage value applied to the bias circuit 130 gradually decreases according to a time constant determined by the resistor R1 and the capacitor C1, and finally reaches a value corresponding to a voltage drop caused by the current flowing through the

[redacted]

> resistor R1. Thus, for the amplifier, the DC voltage of the DC power source E1 is applied immediately after the power source is turned on, the bias point is set to be high, and the power amplification factor becomes high, but, as time advances, current flows through the resistor R1, causing a voltage drop, and the amplifier operates at a low bias point and the power amplification factor becomes small by the amount of voltage drop. Thus, the power amplification factor correction is performed based on the thermal response.

Akagi ¶7. Thus, a POSITA had a well-developed understanding of using time-dependent current generation, including RC speedup circuits, to adapt a PA biasing circuit to boost a PA's I_{BIAS} in the period just after enablement of the PA.

2. Current Mirrors Were Widely Known

65. Current mirrors were likewise commonplace and formed part of the general knowledge in the art long before May 2011. As discussed further below, a POSITA was well versed in their multiple and various structures, from single-transistor mirrors, to complicated, multi-transistor designs. A POSITA understood how to use and include current mirrors in analog circuit designs, including RF PAs and their biasing circuits. Their behavior and benefits were predictable and well documented. They were pervasive in the literature.

66. For example, the current mirror had "become a familiar icon of modern analog design." Gilbert 239. They were "widely used in analog integrated circuits [] as biasing elements." Gray 251. Indeed, current mirrors were considered "particularly useful building blocks for analog circuit design" because "they provide a means of establishing the DC bias levels within the circuit." Grebene 170. Using current mirrors in biasing had advantages including "superior insensitivity of circuit performance to variations in power supply and temperature." Gray 251.

67. As its name suggests, a current mirror is a circuit that "replicates" (in the sense of "reproduces", "reflects", "replicates", "duplicates" *etc.*) —*i.e.* "mirrors"—an input current as its

output current. Grebene 170 ("the reference current" is "**reproduced or reflected"** and "because of this property" are "known as *current mirror* circuits."); *see, e.g.*:

> In a constant-current stage, the reference current in one branch of the circuit is accurately reproduced or reflected in a second branch, relatively independent of the absolute values of the device parameters. Because of this property, these subcircuits are also known as *current mirror* circuits. Such circuit configurations are particularly useful building blocks for analog circuit design, since they provide a means of establishing the dc bias levels within the circuit, within the accuracy of the matching or tracking properties of the monolithic components.

Grebene 170. Gilbert 240 ("an output node ... into which a **replication**" of "the input current flows in the same direction"); *see, e.g.*:

> The simplest current mirror is a three-terminal device, Figure 6.la, having an input node, N1, capable of accepting a current, I_1, of only one polarity, an output node, N2, into which a replication, I_2, of the input current flows in the same direction, and a common node, N0, in which the sum of the input and output currents flow.

Gilbert 240. Gray 251 ("[T]he input current is **reflected** to the output, **leading to the name *current mirror***."); *see, e.g.*:

> A current mirror is an element with at least three terminals, as shown in Fig. 4.1. The common terminal is connected to a power supply, and the input current source is connected to the input terminal. Ideally, the output current is equal to the input current multiplied by a desired current gain. If the gain is unity, the input current is reflected to the output, leading to the name current mirror. Under ideal conditions, the current-mirror gain is independent of input frequency, and the output current is independent of the voltage between the output and common terminals.

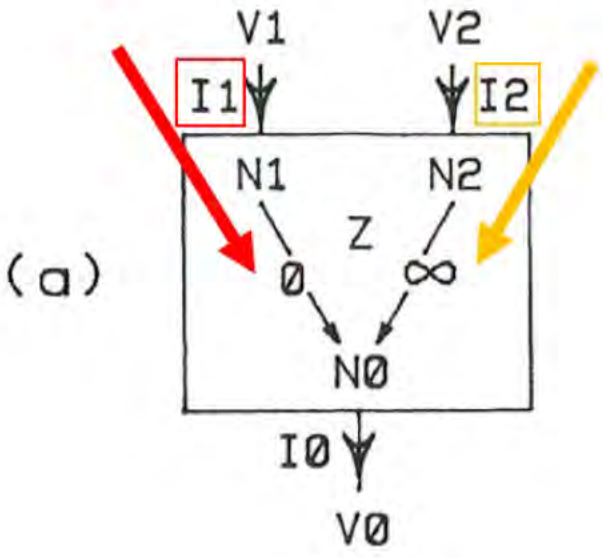
Gray 251. Barrie Gilbert started his textbook chapter on "Bipolar Current Mirrors" by observing that "[f]ew readers of this book will need to be introduced to the concept of the current mirror; it has become a familiar icon of modern analog design." Gilbert 239. Barrie Gilbert was one of the pre-eminent industry leaders in analog circuit design. Gilbert Biography ("Barrie was likely the most famous analog circuit designer in the world."). Barrie Gilbert was featured, for example, on "the cover of the Fall 2007 IEEE Solid-State Circuits Society News issue and

virtually the entire issue devoted to him." Gilbert Biography (showing IEEE issue cover page titled "The Gears of Genius: Barrie Gilbert and Analog Circuits").

68. Gilbert begins by describing the "generalized form" of a current mirror. He described the "simplest current mirror" was a three node device, with "an input node, N1, capable of accepting a current I1" (red arrow) of "only one polarity, an output node, N2, into which a **replication** I2" (gold arrow) of "the input current flows in the same direction, and a common node, N0, in which the sum of the input and output currents flow." Gilbert 240; *see, e.g.*:

> The simplest current mirror is a three-terminal device, Figure 6.la, having an input node, N1, capable of accepting a current, I_1, of only one polarity, an output node, N2, into which a replication, I_2, of the input current flows in the same direction, and a common node, N0, in which the sum of the input and output currents flow.

Gilbert 240.



Gilbert 240, Fig. 6.1a (annotated); *accord* Gray Fig. 4.1a.

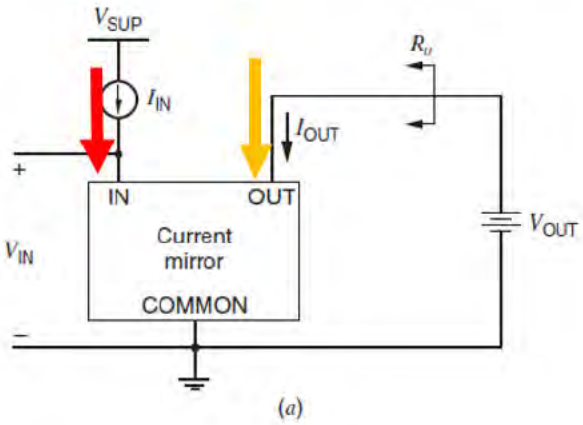
[redacted]

69. In such current mirrors, the replicated current (I2, gold arrow above) is pulled into the mirror, and is thus called a "current sink." This arrangement is referred to as a "positive" current mirror. Gilbert 330; Gray Fig. 4.1; *see, e.g.*:

> There are many different types of current mirror and we begin by considering some definitions and terms commonly used. Current mirrors are firstly categorised as positive or negative. Positive current mirrors have an output in the form of a current sink (quiescant output current positive). Thus they require a power supply which is at a relatively negative potential. Negative current mirrors have a current source output (quiescant output current negative) and require a more positive power supply.

Gilbert 330.

70. Current mirrors having a common node at the more positive power supply, and replicate the input current as a current source flowing out of the output of the current mirror are referred to as "negative" current mirrors. *see*, Gilbert 330; Gray 252, Fig. 4.1(b). Gray likewise depicts the same fundamental inputs and outputs of a current mirror:



Gray Fig. 4.1(a) (annotated).

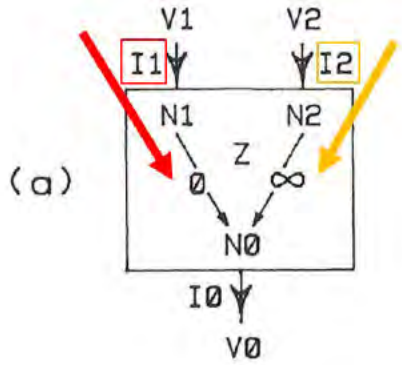
71. This ability of a current mirror to take an input current that is acting as a current source (*red*), and then replicate that same current *i.e. mirror* it, to create a current *sink* at the output node of the mirror, was well known to a POSITA. This was a common reason to include

[redacted]

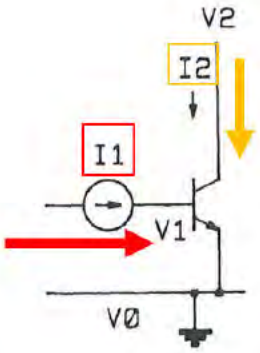
a current mirror in a circuit, *i.e.*, when one needed to couple a current source from one circuit as a current sink pulling a replicated amount of current from another circuit.

Single Transistor Current Mirrors

72. Current mirrors were known to come in many forms. For example, it was well known to use a single transistor to take, *e.g.*, a current source as an input current, and then replicate (*mirror*) it to an output terminal of the transistor as, *e.g.*, a current sink. For example, Gilbert provides a section on "One-transistor Mirrors", describing how to arrange a single BJT transistor as a current mirror.



Gilbert 240, Fig. 6.1a (annotated)



Gilbert 243, Fig. 6.2a (annotated)

73. Gilbert explained that "[i]n the simplest possible scenario, a single BJT can be used as a mirror." Gilbert 242 (section titled "One-transistor Mirrors"). With reference to the transistor in Fig. 6.2 (above), Gilbert explained that node Nl (of the general current mirror form shown in Figure 6. la) is the base of the transistor in Fig. 6.2a (*i.e.* the input of the current mirror), and likewise, N2 is the collector (*i.e.* the output of the current mirror), and N0 the emitter (*i.e.* the common node of the current mirror). Gilbert 242; *see, e.g.*:

> In the simplest possible scenario, a single BJT can be used as a mirror: node N1 (of Figure 6. la) is the base, N2 the collector and N0 the emitter. Of course, the practical objection to this proposal is that the mirror ratio, M, is much higher than generally needed and poorly-controlled, being just the common-emitter current-gain, J3, and

[redacted]

> not very linear. While these objections are all true, it is nevertheless useful to begin here, because we will discover that many of the properties of more familiar mirrors can be predicted from the behavior of the single transistor circuit.

Gilbert 242.

74. While "not very linear" and "poorly-controlled" compared to other current mirrors, the "mirror ratio, M" of the single BJT mirror is the "common-emitter current-gain, β". Gilbert 242. The output is scaled by the amplification factor of the BJT, namely the common-emitter current-gain, β. That is because in a BJT biased into its active region, the collector current (I_C) and base current (I_B) are generally related by the equation: $I_C = I_B * \beta$. Illingworth 38; Gilbert 242-243; *see, e.g.*:

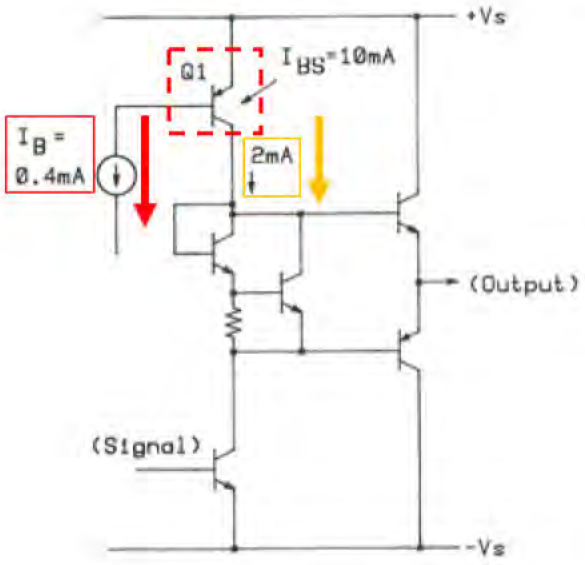
> **beta current gain factor** *Syn.* common-emitter forward-current transfer ratio; forward current gain. Symbol: β. The short-circuit current-amplification factor in a bipolar transistor with ►common-emitter connection: $\beta = \alpha I_c / \alpha I_B$ V_{CE} constant where I_C is the collector current and I_B is the base current; the collector voltage, V_{CE}, is constant. β is always greater than unity and practical values up to 500 are used.

Illingworth 38.

> It will be assumed that β is independent of current over the range of interest. If β were also independent of V_2, the output I_2 would always be simply βI_1 and the output resistance r_0 would be infinite. In fact, β increases with V_2 due to base-width modulation, and in the customary BJT model would be exactly doubled when the collector bias voltage, V_{CB} (roughly, V_2), is equal to the forward Early voltage, V_{AF}.

Gilbert 243.

75. Similarly, in the following example, Gilbert shows and describes a single transistor current mirror, "Q1", to bias "an operational amplifier".



Gilbert, Fig. 6.4 (annotated)

Gilbert Fig. 6.4 (annotated).

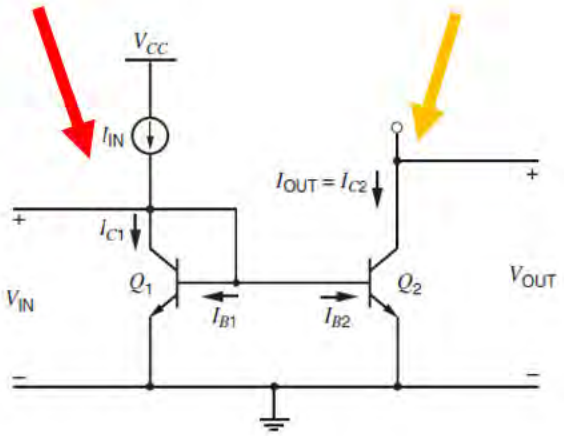
76. Gilbert described the transistor Q1 in the above figure as a "simple open-base PNP **current mirror**", "used to bias an [operational amplifier] ... with improved efficiency." Gilbert 248; *see, e.g.*:

> Figure 6.4 A simple open-base PNP current mirror (Q1) used to bias an op-amp slewing node with improved efficiency; remaining components are for illustrative purposes only.

Gilbert 248.

Two Transistor Current Mirrors

77. Long before May 2011, undergraduate electrical engineering students were likewise conversant with the basic two-transistor current mirror form. Gray 253, Fig. 4.2; Gilbert 251, Fig. 6.7a. For example, a "simple bipolar current mirror" is shown in the annotated Figure 4.2 below, with the input current annotated in red and the mirrored output current in yellow.



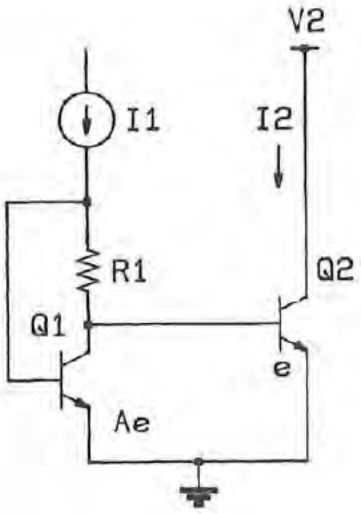
Gray 253 Fig. 4.2.

78. This two-transistor current mirror format was a heavily documented, staple of analog circuit design having highly predictable behaviors and advantages, readily known to undergraduate level students.

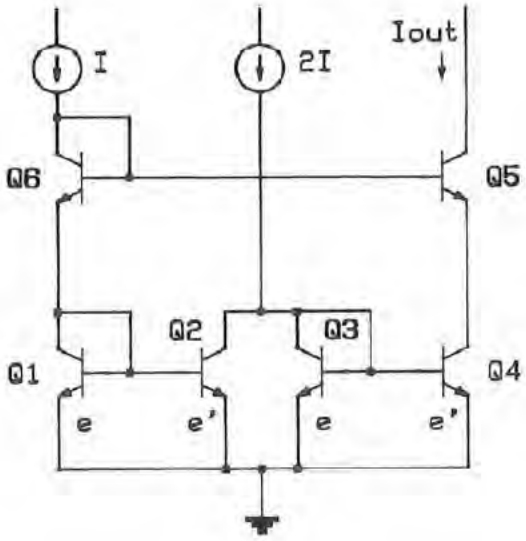
Advanced Current Mirrors

79. Although a POSITA knew of simple single and two transistor current mirror designs, a POSITA also knew that "current mirrors" were not limited to any one configuration or arrangement.

80. More advanced, multi-transistor structures were likewise known for mirroring an input current to an output current, with various connections between the gates of the mirrors. Gilbert 261, Fig. 6.12b, 276-77, Fig. 6.25b; Gilbert 292, Fig. 6.42c.



Gilbert 261, Fig. 6.12b.



Gilbert 286, Fig. 6.36.

81. One well-known benefit of current mirrors was that they could be configured to provide a desired current amplification when mirroring the current, such that the "output current is equal to the input current multiplied by a desired current gain." Gray 251; *see, e.g.*:

> A current mirror is an element with at least three terminals, as shown in Fig. 4.1. The common terminal is connected to a power supply, and the input current source is connected to the input terminal. Ideally, the output current is equal to the input current multiplied by a desired current gain. If the gain is unity, the input current is

[redacted]

> reflected to the output, leading to the name current mirror. Under ideal conditions, the current-mirror gain is independent of input frequency, and the output current is independent of the voltage between the output and common terminals.

Gray 251. It was well known that one could advantageously set the gain by controlling the size of the transistors involved. Gray 254, 257; *see, e.g.*:

> Thus for identical devices Q1 and Q2, the gain of the current mirror is approximately unity… In practice, the devices need not be identical… Since the saturation current of a bipolar transistor is proportional to its emitter area, the first term in (4.6) shows that the gain of the current mirror can be larger or smaller than unity because the emitter areas can be ratioed. If the desired current-mirror gain is a rational number, *M/N*, the area ratio is usually set by connecting *M* identical devices called *units* in parallel to form *Q*2 and *N* units in parallel to form *Q*1 to minimize mismatch arising from lithographic effects in forming the emitter regions

Gray 254.

> Equation 4.17 shows that the gain of the current mirror can be larger or smaller than unity because the transistor sizes can be ratioed. To ratio the transistor sizes, either the widths or the lengths can be made unequal in principle. In practice, however, the lengths of *M*1 and *M*2 are rarely made unequal.

Gray 257. In the case of bipolar transistors, this was done by scaling emitter area. Gilbert 280; Grebene 172; *see, e.g.*:

> There is no particular difficulty in achieving high mirror ratios. In many cases, simple emitter area ratios will suffice, supported by current gain if necessary (as in the EFA mirror, which is not limited to the use of a single transistor for current boosting). In practical monolithic designs, emitter area ratios of up to 100: 1 are not hard to achieve.

Gilbert 280.

> The basic current-voltage equations (4.1) through (4.8) hold over a broad temperature range (typically -60 to + 150°C) and over six orders of magnitude of current. Thus, the basic current mirror circuit of Figure 4.1 provides a means of obtaining a current reference level, independent of implicit device parameters, which can be "scaled" by proper choice of the emitter areas of the two transistors. Assuming typical V_{BE} mismatch of < ± 1 mV and β in the range of 100-200, the typical output current /**2** would be within ±5% of I_{ref} over a wide range of temperature and current levels.

Grebene 172.

[redacted]

82. Thus, there was a robust state of the art in current mirrors at the time of the purported invention. A POSITA knew how to design and implement a wide variety of mirror circuits, from single transistor to complicated multi-transistor circuits, all achieving well understood, predictable behavior in replicating, *i.e.*, mirroring an input current to an output current.

3. BJT Power Amplifiers Were Commonly Implemented Using Heterojunction Bipolar Transistors (HBTs)

83. By May 2011, it was well known to implement PAs using bipolar junction transistors (BJT). *Supra* §VIII.C.1. As early as 2004, I was implementing BJT PAs with SiGe HBTs in my research activities. Furthermore, it was well-known, general knowledge in the art that a high performing type of BJT for RF PAs was a BJT with a wide band gap emitter, known as a Heterojunction Bipolar Transistor (HBT). *See, e.g.,* Illingworth 259 (defining HBT, including, *e.g.*, "A bipolar junction transistor that incorporates a wide band gap emitter" with the result of reduced base resistance, "maximizing the desired injection of carriers from emitter to base…. HBTs are used at radio- and microwave frequencies, in integrated circuit and power applications"). HBTs were known to be specifically adapted for high performance to meet the demands of RF power amplification applications. *See, e.g.,* Illingworth 259 (describing that the HBT properties "leads to **an improvement in the high-frequency performance** of the transistor. **HBTs are used at radio- and microwave frequencies**, in integrated circuit and power applications, and in optoelectronic ICs."); *see, e.g.*:

> **heterojunction bipolar transistor** (HBT) A bipolar junction transistor that incorporates a wide band gap emitter. The emitter-base junction is a heterojunction between semiconductors of different energy band gap. The following are typical material systems: AIGaAs(emitter)/GaAs(base); AllnAs/InGaAs; Si/SiGe
>
> The wider band gap of the emitter reduces significantly the injection of majority carriers from base to emitter, thus maximizing the desired injection of carriers from

[redacted]

> emitter to base. This eliminates the requirement for a heavily doped emitter to achieve the same result, and consequently allows the base doping to be increased. An increase in base doping is desirable from a device viewpoint as the base resistance can be reduced significantly. This leads to an improvement in the high-frequency performance of the transistor. HBTs are used at radio- and microwave frequencies, in integrated circuit and power applications, and in optoelectronic ICs.

Illingworth 259. In fact, HBTs were the dominant, market leading form for RF PAs implemented with BJTs, with well-documented advantages known to a POSITA. TriQuint 1 ("RF medium and high **power amplifiers realized with HBT technology are increasingly popular in telecommunications systems** due to the **inherently superior linearity and efficiency performance** compared to competing technologies. The **reliability of HBT RF devices is well known to be excellent** from Highly Accelerated Stress Testing (HAST) and High Temperature Operating Lifetime (HTOL) testing."); Yanjun 1 ("In past years, **HBT PAs have dominated the medium power transmitter market due to their excellent linearity and PAE**.").

84. It was known that HBTs came in a variety of advantageous forms, including Gallium Arsenide (GaAs) and Silicon Germanium (SiGe). Illingworth 259.

85. Thus, the use of BJT transistors to form a PA, including the HBT form of BJTs and their advantages, formed part of the general knowledge in the art before the invention.

4. Packaging of Power Amplifiers and Biasing Circuits Was Common Knowledge and Routine

86. By May 2011, it was well known to a POSITA to include both PAs and their bias circuits on an integrated circuit ("IC"), to achieve commonly understood benefits in terms of size, cost, uniformity of component characteristics and thermal responses.

87. Analog signal processing functions in wireless communications were frequently consolidated into a single package called a "front end module." These modules included PAs

[redacted]

and their bias circuits on a single IC. Doherty ¶¶58-60 (describing PA and bias circuit on same integrated circuit), ¶89; Marra ¶¶65-68 (describing PA biasing, and disclosing an "integrated circuit" having both "an amplifier and a bias circuit"); Hedberg 2:37-43 (an advantage of "a bias regulator and an output transistor of a power amplifier[] fabricated upon a common integrated-circuit substrate" is "close thermal coupling between the bias regulator and the power amplifier.").

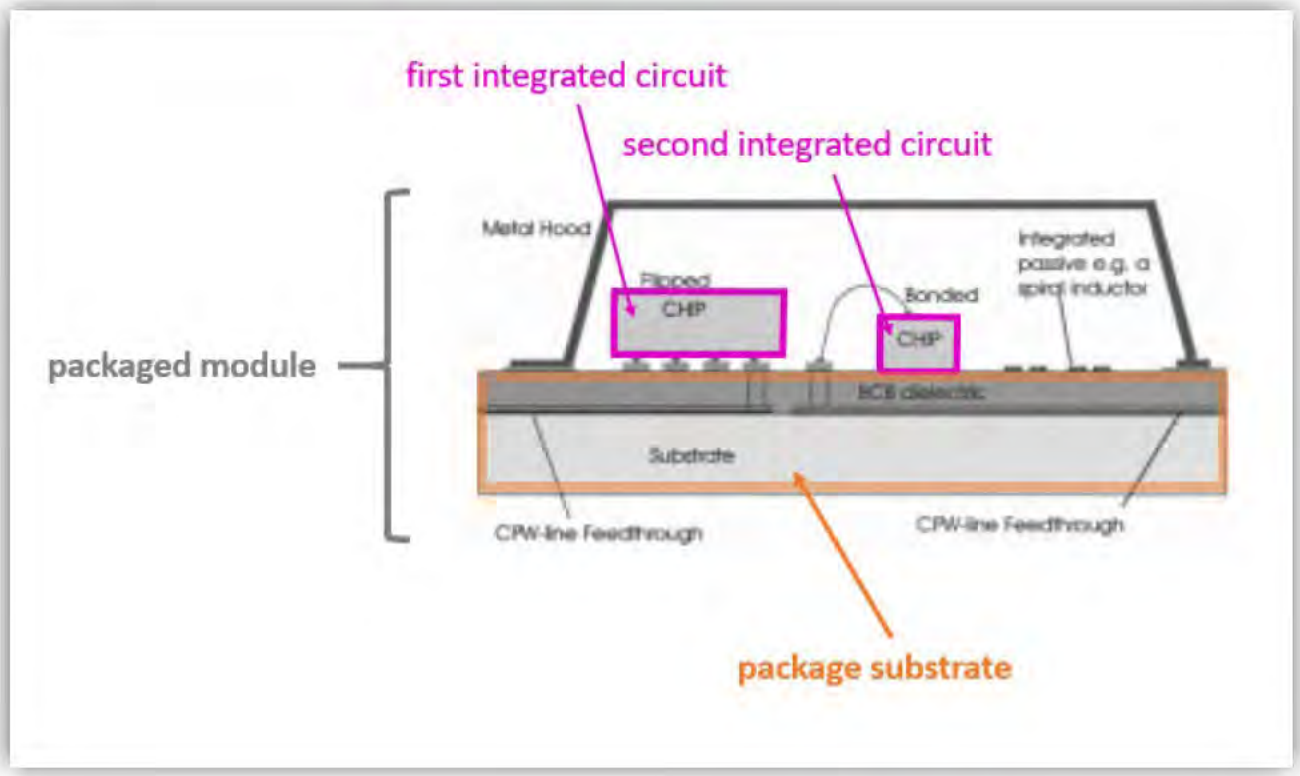
88. A POSITA understood that packaging is the process of enclosing an IC (*i.e.* the semiconductor "die" or "chip")[9] within a protective casing that shields it from environmental damage while also providing electrical connections allowing it to be connected within an electronic device. ICs were implemented in packaged modules because "die[s] or chips have to ultimately be packaged to be useful." Laplante 003; *see, e.g.*:

> **package** in MMIC technology, die or chips have to ultimately be packaged to be useful. An example of a package is the T07 "can." TheMMIC chip is connected within the can with bond wires connecting from pads on the chip to lead pins on the package. The package protects the chip from the environment and allows easy connection of the chip with other components needed to assemble an entire system, such as a DBS TV receiver.

Laplante 003.

89. It was also well known to package two or more ICs together on a common package substrate to form what was known as a "multi-chip module." For example, *Diels* depicted a representative module:

[9] A semiconductor "die" is a "chip." Illingworth 125.



Diels Fig. 2 (annotated, reproduced in part).

IX. INVALIDITY OF THE ASSERTED CLAIMS OVER THE PRIOR ART

A. Summary of Opinions Relating to the Invalidity of the Asserted Patents Based on Prior Art

90. It is my opinion that claims 14, 15, 17, and 20 of the '563 Patent are invalid as obvious over the following references.

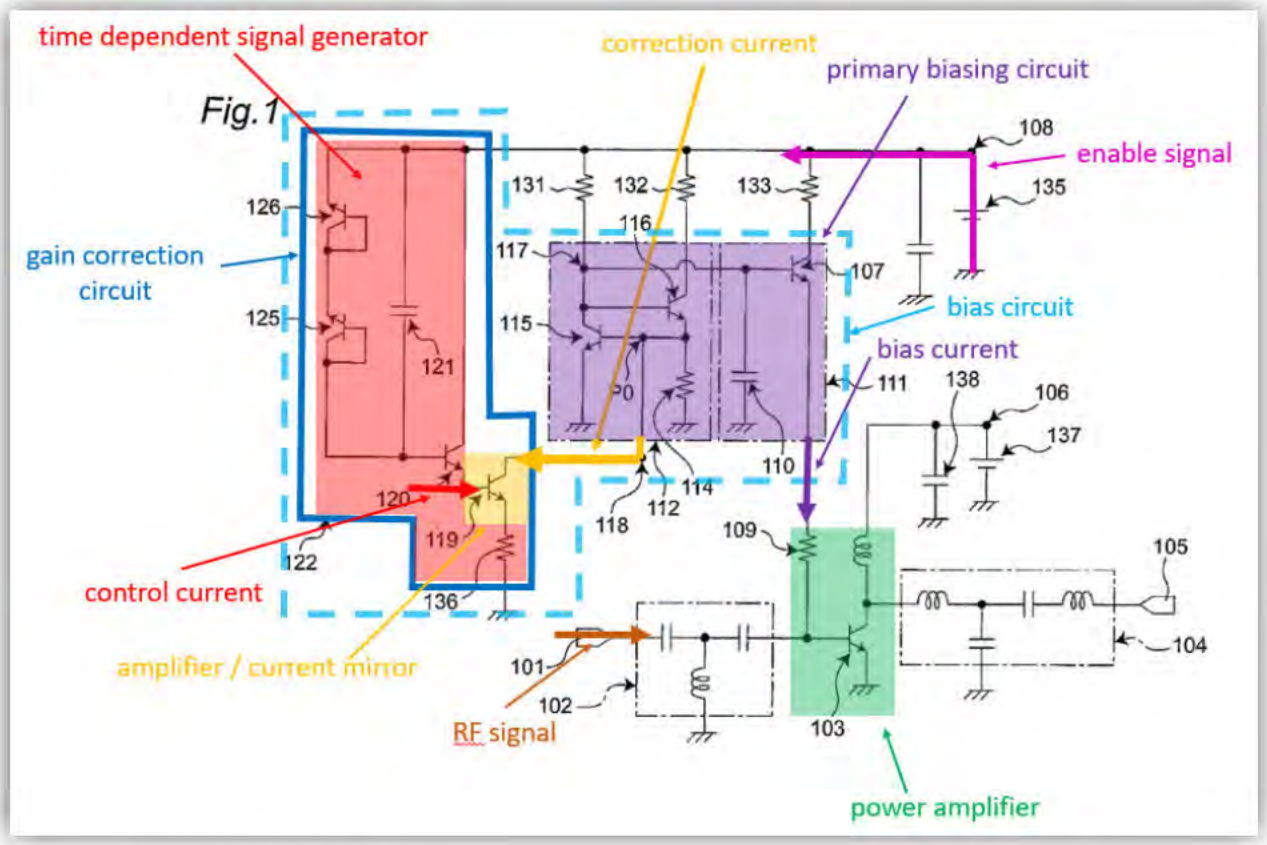
Claims	Basis	References
14, 15, 17, and 20	Obvious	Ishimaru in view of Ichitsubo
14, 15, 17, and 20	Obvious	Ishimaru in view of Johnson
14, 15, 17, and 20	Obvious	Ishimaru in view of Ichitsubo and Harrison
14, 15, 17, and 20	Obvious	Ishimaru in view of Johnson and Harrison

[redacted]

91. It is my opinion that claims 1-2,10-11, 17-18, and 20-22 of the '101 Patent are invalid as obvious over the following references.

Claims	Basis	References
1-2, 10-11, 17-18, and 21-22	Anticipation	Ishimaru
1-2, 10-11, 17-18, and 20-22	Obvious	Ishimaru in view of Harrison
20	Obvious	Ishimaru alone or in view of Johnson
20	Obvious	Ishimaru in view of Harrison and Johnson

92. The use of biasing circuitry to generate a boost current to correct for low gain when a PA is enabled (i.e. at startup) was known in the prior art. For example, Ishimaru discloses a nearly identical architecture for a PA bias circuit that addresses the same PA gain variation arising from thermal effects at startup. Ishimaru ¶¶52-54. Ishimaru's architecture is illustrated below:



Ishimaru Fig. 1 (annotated).

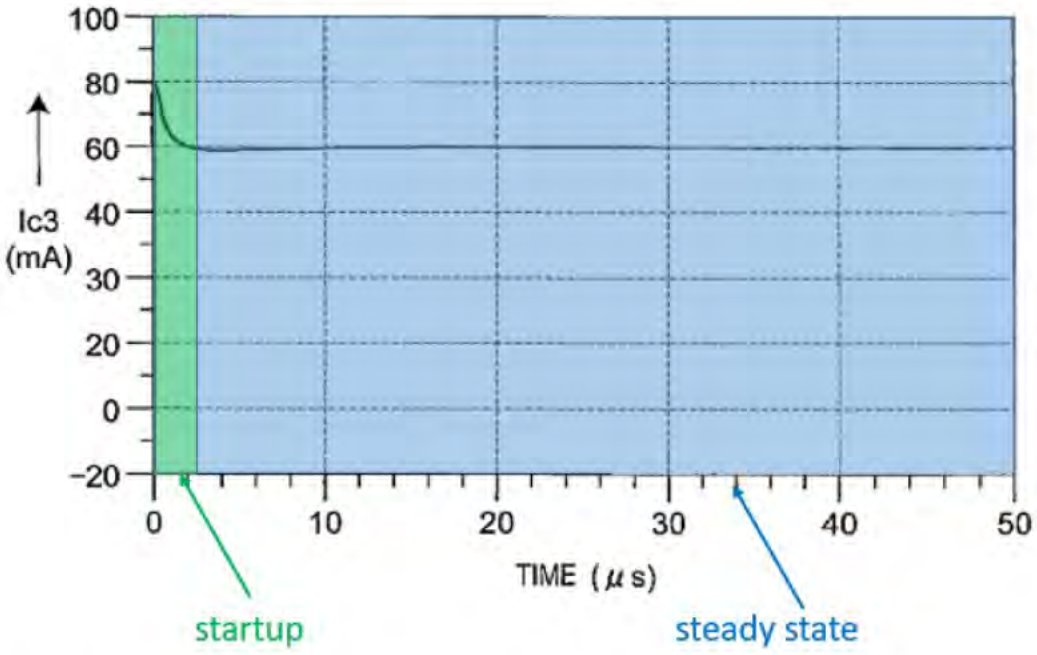
93. Ishimaru's enable signal (pink arrow) is activated at startup, causing a time-dependent signal generator (red) to generate a shaped control current ($I_{CONTROL}$) (red arrow) that is received by a current amplifier (gold) implemented as a current mirror. The current mirror replicates (*i.e.* mirrors) and amplifies $I_{CONTROL}$ (red arrow) to form a correction current ($I_{CORRECTION}$) (gold arrow) pulled from a primary biasing circuit (purple).

94. Ishimaru's time-dependent signal generator and amplifier/current mirror together form a gain correction circuit (dark blue), which Ishimaru calls a "speedup circuit." The speedup circuit (dark blue) is a gain correction circuit in that it is a circuit that generates $I_{CONTROL}$ and $I_{CORRECTION}$ (gold arrow) shaped for the purpose of correcting for the low gain of the PA (green) at startup. The $I_{CONTROL}$ and $I_{CORRECTION}$ (gold arrow) are shaped to temporarily pull current out

of the PA's primary biasing circuit (purple) in an amount and duration necessary to cause the primary biasing circuit to provide a corresponding temporary boost in bias current (I_{BIAS}) to the PA (green) to boost its gain during the startup period when its gain would otherwise be too low. The $I_{CORRECTION}$ is thus configured to compensate for the thermal startup characteristics of a given PA, *i.e.*, the PA's gain over time absent compensation.

95. The resulting short "boost" in I_{BIAS} is provided to the PA to overcome its low gain at startup, thereby reaching steady state sooner and providing a flatter gain response versus time, as illustrated by Ishimaru:

Fig.3



Ishimaru Fig. 3 (annotated).

Thus, Ishimaru is a parallel disclosure to the '563 Patent, directed to the same problem and proposing the same solution, but using slightly different words to describe the same concepts.

[redacted]

B. Summary of the Prior Art References

1. US 2009/0212863 to Ishimaru et al. ("Ishimaru")

96. Ishimaru is a patent application published on August 27, 2009. I have been informed and understand that Ishimaru is prior art to the Asserted Patents at least under pre-AIA 35 U.S.C. §102(b).

97. Ishimaru is titled "Power Amplifier" and relates to "a high frequency power amplifier to be used in radio communication devices or the like." Ishimaru Abstract, ¶1.

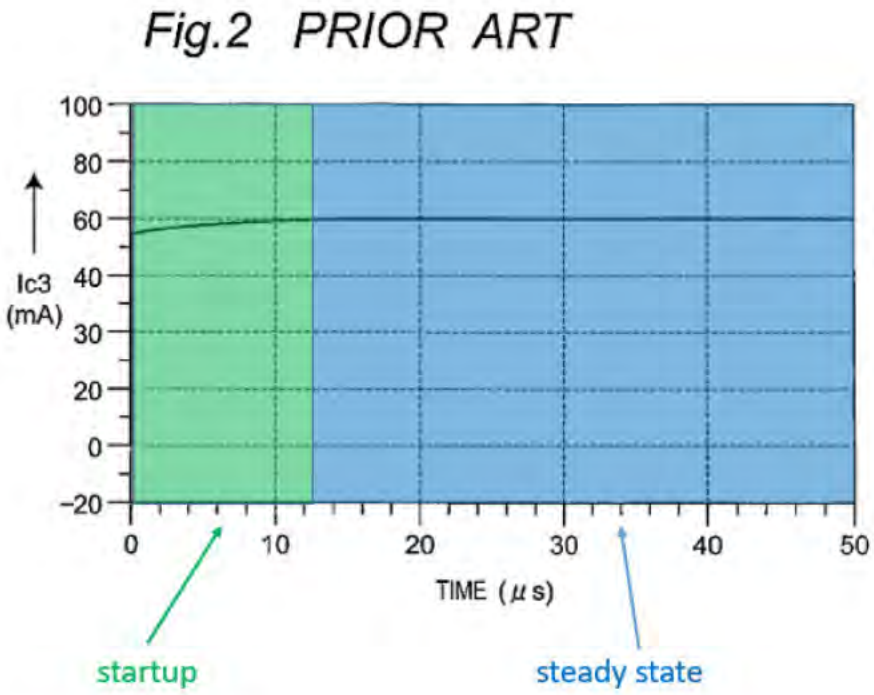
98. Ishimaru explains that PAs in communication systems such as those using "Orthogonal Frequency Division Multiplex[ing]" have "such a circuit design for linearization that the system runs on a linear amplification range of enough smaller outputs than a maximum output of the power amplifier" so that the output RF signal "is not distorted in the power amplifier." *Id.* ¶2.

99. Ishimaru further explains that "linear amplification" "means that even with input signal power changed, the output signal power is amplified at a constant ratio for output while the phase keeps unchanged." Further, Ishimaru explains that in some communication systems, "slight changes of amplification gain as small as 0.2 to 0.3 dB may matter," *i.e.*, affect a communication link. *Id.* ¶3.

100. A POSITA would thus understand that Ishimaru is from the same field of art as the Asserted Patents because it relates to the field of RF electronics generally, PAs specifically, and controlling/compensating gain in particular.

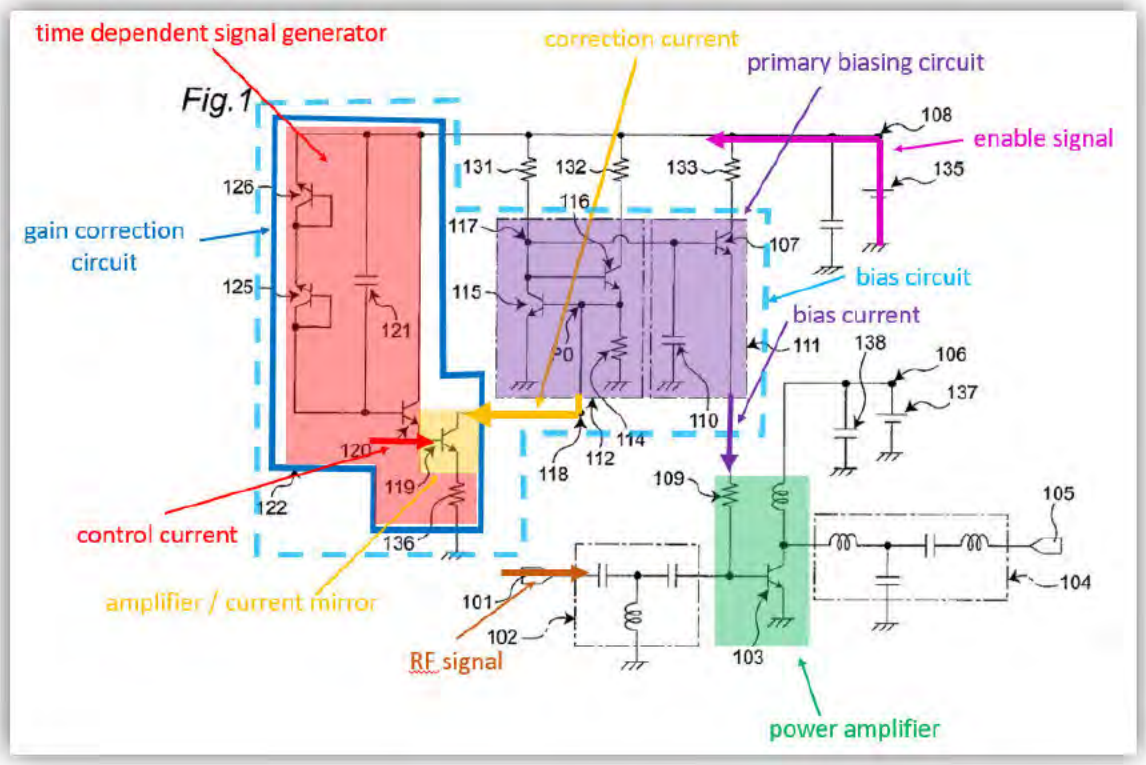
101. Ishimaru explains that thermal changes that occur slowly during startup can last for "tens to several hundreds of microseconds" and affect the "amplification ratio" of the PA

during that time. Ishimaru ¶4. In an example of such gain variation of the PA at startup, Ishimaru showed how collector current of the PA comes up slowly (~10 us in this example):



Ishimaru Fig. 2 (annotated).

102. Ishimaru's solution, shown in Figure 1 below, was a PA and bias circuit that included a "speedup circuit" that "transiently (temporarily) increases" the I_{BIAS} fed to the amplifier transistor by the bias circuit during the period after startup. Ishimaru ¶13. Speedup circuit 122 includes transistors 119, 120, resistance element 136, as well as a capacitance element 121 connected between the base of transistor 120 and bias terminal 108. Ishimaru ¶50-51.



Ishimaru Fig. 1 (annotated).

103. Figure 1 shows an input signal terminal 101 that receives a high-frequency signal (brown arrow) as an input signal, and this input signal passes through an input matching circuit 102, and is then amplified by amplifier transistor 103 (green). The amplifier transistor 103 outputs a signal through output matching circuit 104 to output signal terminal 105. Figure 1 also depicts a bias circuit 111 and a bias power source section 112, which together constitute a bias power source section (purple), and a speedup circuit 122 (dark blue). Ishimaru ¶¶43, 46, 49.

104. Bias circuit 111 includes a bias transistor 107 and capacitance element 110, where a collector of the bias transistor is connected to a bias terminal 108, which is in turn connected to a control voltage source 135. Ishimaru ¶44. The emitter of the bias transistor 107 is connected to the base of the amplifier transistor 103, and "supplies a base bias current" (purple arrow) to the base of the amplifier transistor (green). Ishimaru ¶43. Power source circuit 112 is connected

[redacted]

to the base of the bias transistor 107. Ishimaru ¶46. Power source circuit 112 has a connecting point P0, which is connected to an output terminal 118 of a speedup circuit 122. Ishimaru ¶49.

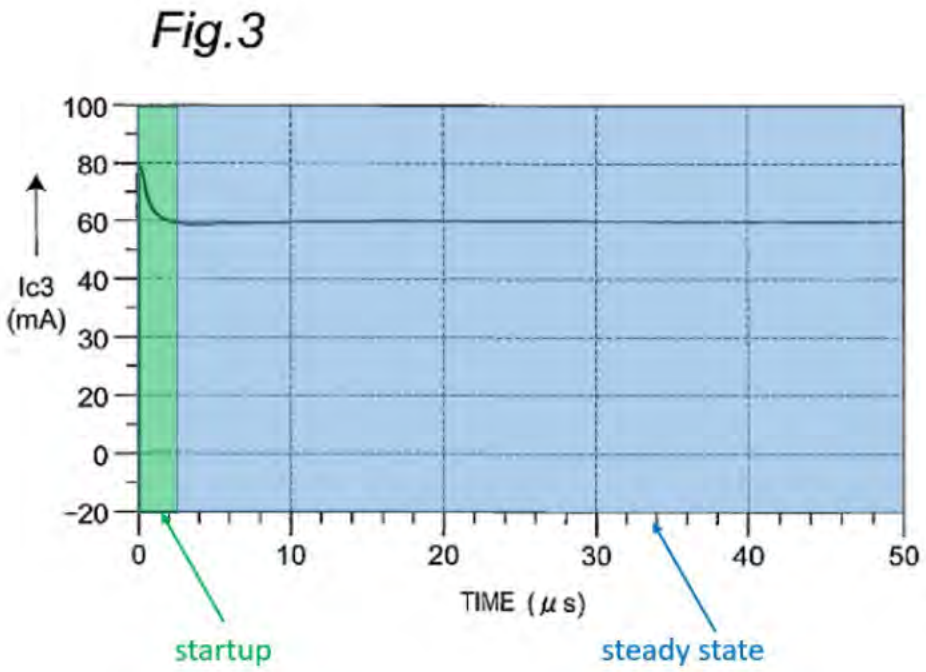
105. The circuit used "capacitance element 121" "at turn-on of the amplifier" to generate an $I_{CORRECTION}$ (gold arrow) that "transiently (temporarily) flows" out of the biasing circuit from "output terminal 118." That causes the voltage on the base of bias transistor 107 to "transiently increase[]", causing the bias "current fed to the amplifier transistor 103" to likewise "transiently increase[]." Ishimaru ¶52.

106. As illustrated in annotated Figure 1, a POSITA understood that the bias circuit (light blue) consists of a conventional "primary bias circuit" 111, 112 (purple) driven by a conventional, unmodified "enable signal" (pink), plus a gain correction circuit (speedup circuit) (dark blue) that generates the $I_{CORRECTION}$ (gold arrow) to shape the bias current (purple arrow) that emerges from the primary bias circuit. That $I_{CORRECTION}$ is generated by the gain correction circuit using a time-dependent signal generator (red) to generate a small $I_{CONTROL}$ (red arrow) with the desired shape, and then scaling up that shaped signal to an appropriate amplitude using a "current amplifier" (gold). The current amplifier replicates (*i.e.* mirrors) and amplifies $I_{CONTROL}$ (red arrow) to form $I_{CORRECTION}$ (gold arrow), which is pulled from the primary biasing circuit (purple).

107. Ishimaru explains that, at a rise time of control voltage source 135 (which is input to bias terminal 108 and is the enable signal), "with electric charge flowing into the capacitance element 121" "a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower." Ishimaru ¶52. The I_{BIAS} (purple arrow) fed "to the amplifier transistor 103 is forcedly increased at turn-on

of the amplifier." *Id.* ¶54. This means that "at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases." *Id.* ¶52.

108. Accordingly, to compensate for the startup phenomenon shown in Figure 2 (above), Ishimaru disclosed simulation results of the transient boost in PA collector current at PA startup. Ishimaru ¶54, Fig. 3.



Ishimaru Fig. 3 (annotated).

109. Ishimaru taught that the forced transient boost in current corrected for the startup gain variation of the PA:

> Therefore, at the rise time, the **power amplification factor of the amplifier transistor 103 transiently increases**, so that the **time elapsing until temperature variations due to heat generation** of the amplifier transistor 103 **come to an equilibrium** on the whole circuit is shortened, with a result of **reduced distortion of the amplification signal** (e.g., modulated wave signal).

Ishimaru ¶52 (emphases added).

> Thus, occurrence of **distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed**, so that the **linearity** of the

[redacted]

> circuit in burst operation is **improved**. That is, **gain variations** due to collector current variations of **the power amplifier** using a bipolar transistor **can be compensated.**

Ishimaru ¶54 (emphases added).

2. US 2004/0232982 to Ichitsubo et al. ("Ichitsubo")

110. Ichitsubo is a patent application published on November 25, 2004. I have been informed and understand that Ichitsubo is prior art to the Asserted Patents under at least 35 U.S.C. §102(b).

111. Ichitsubo is titled "RF Front-End Module for Wireless Communication Devices" and relates to a "radio frequency (RF) power amplifier[] (PA) module." Ichitsubo Abstract, ¶2.

112. Ichitsubo described that its PA module teachings were applicable to wireless communication devices and protocols, including cellular and WLAN/802.11. Ichitsubo ¶¶27, 35. Ichitsubo taught using various semiconductor technologies for the PA module, including "Silicon Bipolar, CMOS, RFCMOS, [BiCMOS], SiGe, GaAs HBT, HEMT, etc." Ichitsubo ¶8.

113. A POSITA thus understood Ichitsubo is from the same field of art as the Asserted Patents because it relates to the field of RF electronics generally, a wide range of PAs specifically, and packaging PAs in modules particularly.

114. Ichitsubo explains that "[p]ortable devices ... with wireless communication capability are being developed in ever decreasing size for convenience of use." Ichitsubo ¶2. As expected by a POSITA, Ichitsubo describes assembly in a small, convenient packaged module: A "PA module provides a unitary or common component which may be conveniently assembled in a RF transmission device, with correspondingly simplified assembly, compact 3D size, and enhanced RF amplification performance." Ichitsubo ¶¶8, 24, 28 ("amplifier module is compact and has smaller foot print"), ¶35 (PA module has "a miniature size of a few millimeters.").

[redacted]

115. Referencing Figure 1 (below), Ichitsubo describes a "radio frequency power amplifier (PA) module 14" (*packaged module*) (gray), in which various circuitry—"input impedance matching network 18, the output impedance matching network 20, the power amplifiers 24, the bias circuit 22, and the power sensor 26 "are integrated on an integrated circuit (IC)" (*integrated circuit*) (pink). Ichitsubo ¶25. More specifically, the referenced circuitry was "fabricated in an integrated circuit on a semiconductor chip." Ichitsubo ¶25, ¶38. Ichitsubo, in short, combines the PAs 24 and their bias circuit 22 on the same die/chip.

116. The overall PA module is built on a variety of "module substrate 12" (*package substrate*) types, including a "multiplayer printed circuit board (PCB), lead frame, lower-temperature co-fired ceramics (ITCC), or other suitable electronic materials." Ichitsubo ¶25.

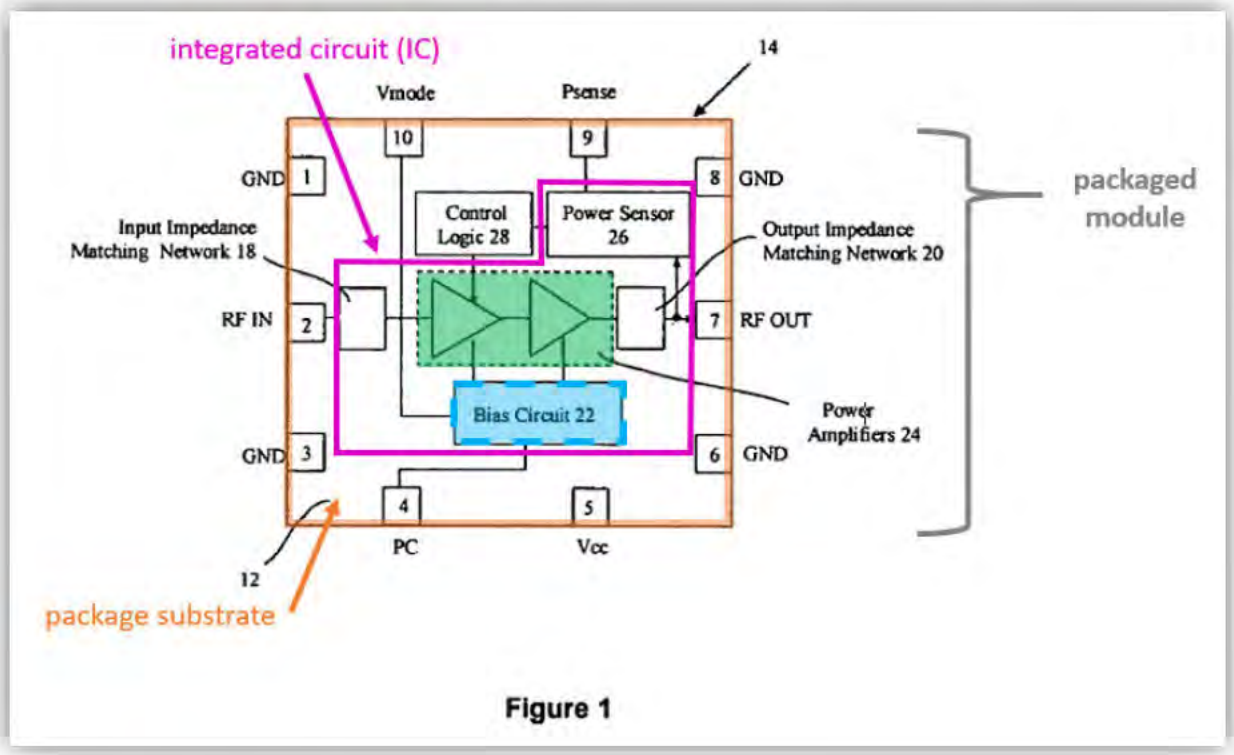
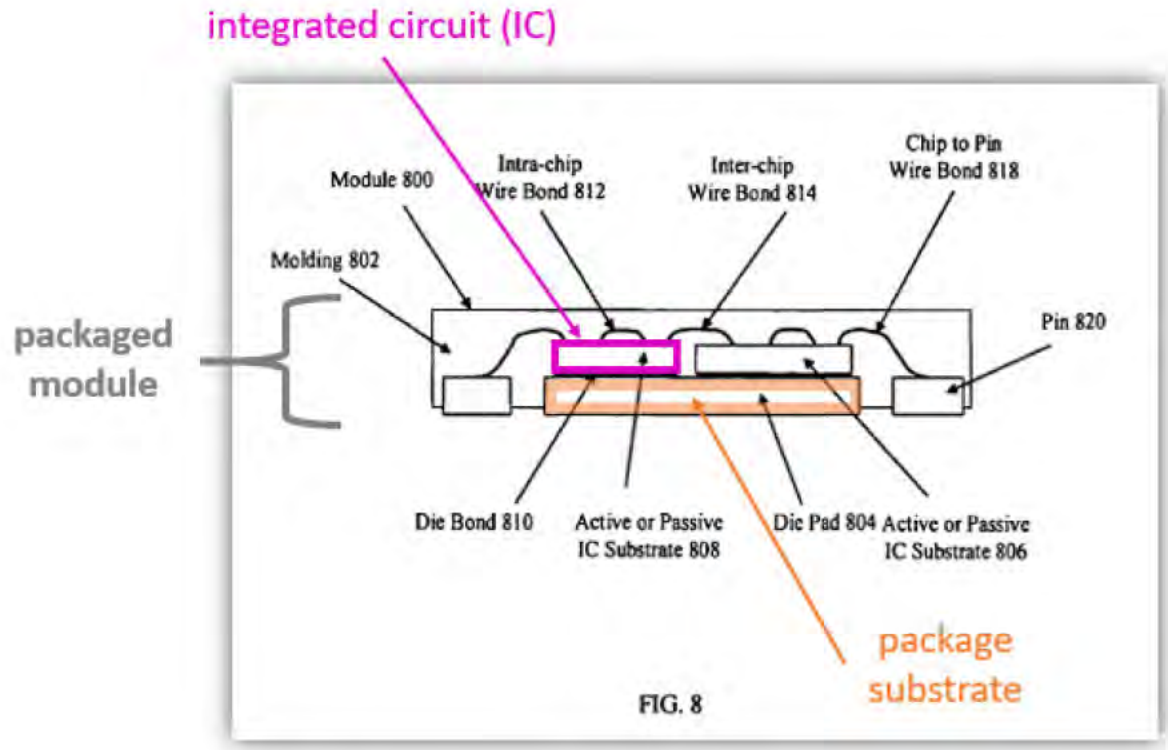


Figure 1

Ichitsubo Fig. 1 (annotated).

[redacted]

117. Ichitsubo also shows a cross-sectional view of packaging, describing and showing the mounting of the IC to the package substrate in the packaged module:



Ichitsubo Fig. 8 (annotated), ¶8.

3. Silicon-Germanium BiCMOS HBT Technology for Wireless Power Amplifier Applications ("Johnson")

118. Johnson is an article from IEEE Journal of Solid-State Circuits, Vol. 39, No. 10, (Oct. 2004) titled "Silicon-Germanium BiCMOS HBT Technology for Wireless Power Amplifier Applications. I have been informed and understand that Johnson was published and accessible to the interested public before to the priority date of the Asserted Patents and is prior art to the Asserted Patents at least under 35 U.S.C. §102(b).

119. Johnson describes PAs as "key components in the wireless communications industry" with SiGe HBTs demonstrating the "requisite combination and performance required

[redacted]

for wireless PA applications." Johnson 1609. Johnson demonstrated a front-end module ("FEM") having SiGEe HBT PAs, biasing, and additional circuitry (*e.g.* power control, antenna switch, impedance matching *etc.*) on a single IC packaged on a substrate for the benefit of making the "PA module simpler and more cost-effective." Johnson 1609, 1612.

120. A POSITA thus understood that Johnson is from the same field of art as the Asserted Patents because it relates to the field of RF electronics generally and packaging of PAs and related circuitry in front-end modules specifically.

121. Johnson discusses the use of SiGe HBTs for PAs and demonstrates a one-chip solution including biasing and control circuitry for PA applications. Johnson 1605. Johnson states that SiGe HBTs are finding increased use for their "favorable thermal properties", "volume manufacturing capability", "design automation support" and "favorable device ruggedness for PA applications." Johnson 1612.

122. Johnson demonstrates an on-chip front-end module ("FEM") that consists of a package substrate of a "low-temperature-cured ceramic (LTCC)." Johnson 1610. Johnson packaged the "die" by mounting it using "flip-chip technology onto the substrate surface," to achieve "extremely low parasitic inductance and good thermal conductivity together with a small footprint." *Id.* Johnson described the packaged IC for power amplifier "modules." *Id.* 1612 ("SiGe BiCMOS flip-chip together with LTCC is a very strong path for PA modules.").

4. Current Sources and Voltage References, A Design Reference for Electronics Engineers (Elsevier 2005) ("Harrison")

123. Harrison is a book titled "Current Sources & Voltage References" and its Chapter 4 is titled "Using BJTs to Create Current Sources." Harrison 47. I have been informed and understand that Harrison published and was accessible to the interested public before the priority

[redacted]

date of the Asserted Patents and is prior art to the Asserted Patents at least under pre-AIA 35 U.S.C. §102(b).

124. Harrison explains that a bipolar junction transistor (or "BJT") is a "current-operated semiconductor device" with "three terminals that are designated the base, the collector, and the emitter." Harrison 49.

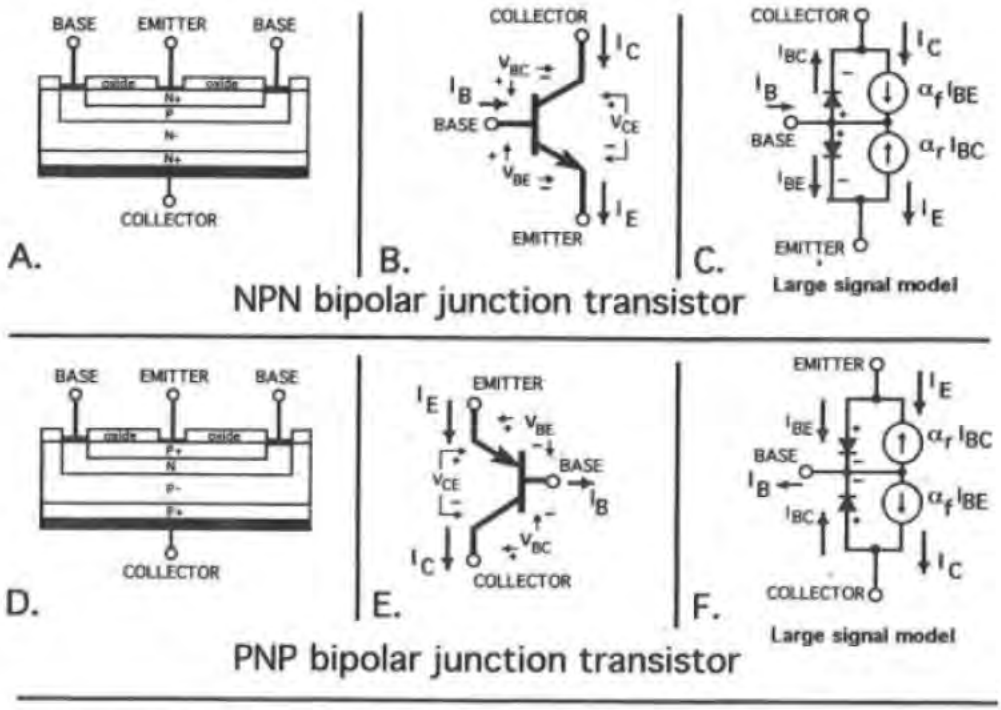


Figure 4.2. *Showing the structure of the BJT, as well as its various voltages, currents, and polarities. Notice the two inherent diodes that provide forward and reverse bias.*

Harrison 50, Fig. 4.2.

125. Harrison explains that "simple current sources" using bipolar analog transistors were used starting in the late 1960s "for purposes of biasing and stability" and analog circuit designers "found a reliable method of biasing their circuits and thereby improving the overall quality and accuracy of their products." *Id.* 68. Harrison further explains that "virtually all BJT current sources are configured as *current mirrors* (aka current reflectors), where an input current is mirrored at the output, in either a matched 1:1 or other ratio." *Id.* 70.

[redacted]

126. A POSITA thus understood that Harrison is from the same field of art as the Asserted Patents because it describes the operation of analog circuit components, such as bipolar junction transistors, that are used in RF electronics and PAs.

127. Harrison illustrates simple two-transistor current source designs using BJT NPN transistors:

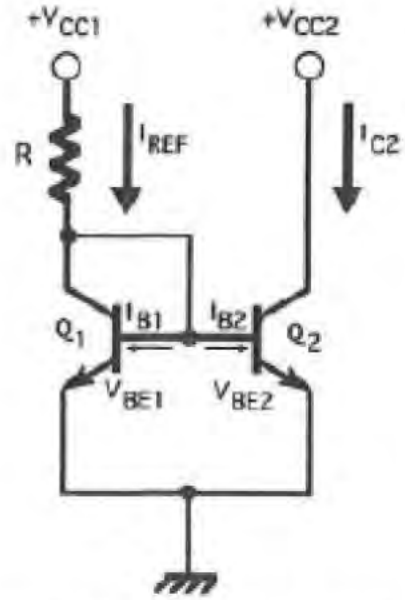


Figure 4.18. Basic BJT current mirrors.

Harrison Fig. 4.18 (reproduced in part), 71 ("reference current, I_{REF}, will be mirrored (duplicated)").

128. Harrison's two-transistor current mirror shown and described in Fig. 4.18 was a widely understood circuit, well established in the general knowledge of a POSITA. §VIII.C.2; Gray 251-54, 257, Fig. 4.2; Gilbert 251, 280, Fig. 6.7(a); Grebene 171. Harrison is exemplary of that general knowledge.

C. Motivation to Combine Prior Art

[redacted]

1. Ishimaru and Ichitsubo

129. A POSITA would have been motivated to combine Ishimaru's teaching of a PA and bias circuit with Ichitsubo's packaging teachings of implementing a PA and bias circuit on an IC attached to a package substrate in a packaged module for at least the following reasons.

130. First, as I explain in the detailed claim mapping below §IX.D.1 ([14.0]-[14.2]), the combination involves nothing more than using Ichitsubo as an express disclosure of the type of IC packaging that a POSITA already understands would be used for Ishimaru in view of the general knowledge in the art. Nothing about the structures, methods or concepts disclosed in *Ishimaru* would need to be changed to implement Ishimaru's power amplifier and bias circuit on a packaged IC—that is understood and expected of Ishimaru when incorporating it into a wireless communications device.

131. Second, as described in the State of the Art section, a POSITA would have been motivated by any one of the numerous and well-known advantages of packaged ICs, which are demanded by the electronics market, including: decreased size, cost and power consumption, increased reliability and durability, and ease of manufacturing and assembly. §VIII.C.4. The combination involves nothing more than following the well-established path of commercial circuit integration and packaging for the same benefits that have made packaged ICs dominate the electronics industry, such as protecting the chip from the environment and allowing easy connections; indeed, to make the chip "useful." Laplante 003. Given the market demands and practices, a POSITA would have been readily motivated to package Ishimaru's power amplifier and bias circuit using the packaged IC teachings of Ichitsubo.

132. Third, a POSITA would have also been motivated by the express teachings, suggestions and motivations of Ichitsubo itself. For example, a POSITA would have been

[redacted]

motivated by Ichitsubo's description of a "radio frequency (RF) power amplifiers (PA) module" for use in wireless devices being "developed in **ever decreasing size for convenience** of use," and teaching of a "**compact 3D size**" PA module having "**enhanced amplification performance**" that "can be **used in a wide range [of] wireless communication devices** such as cellular phone[s], mobile computers, and handheld wireless digital devices" Ichitsubo ¶¶2, 24, 35 (emphases added). Ichitsubo explains that its solution to these problems – a unitary PA module "which may be **conveniently assembled** in a RF transmission device" – has advantages including "**minimiz[ing] device count** and/or **printed circuit board real estate,**" "**simplified assembly**, **compact 3D size**, and **enhanced RF amplification performance**." Ichitsubo. ¶¶9, 24, 25 (emphases added). In other words, Ichitsubo expressly teaches benefits of packaging readily applicable to Ishimaru's PA and bias circuit for its intended use with "radio communication devices." Ishimaru Abstract. A POSITA would have been motivated to follow these teachings in Ichitsubo to predictably achieve a compact, reliable fabrication of Ishimaru's PA and bias circuit. Ishimaru ¶¶42-52; Ichitsubo ¶¶8, 25.

133. Further, a POSITA would have a reasonable expectation of success in implementing Ishimaru's teachings following Ichitsubo's packaging teachings of a PA module because implementing a power amplifier and bias circuit on an IC inside a packaged module was no more than the routine exercise of skill for a POSITA making the PA module simpler and more cost effective. §VIII.C.4 (discussing *e.g.*, Doherty ¶¶58-60, 89; Marra ¶¶65-68; Hedberg 2:37-43).

134. Nor is there anything counterintuitive, technologically challenging, or unique about the notion of the claimed integration and packaging. The specification of the Asserted Patents only briefly describes the packaging involved, and does so at a high level of generality,

[redacted]

without providing any technological solutions or advances in the technology of IC fabrication or packaging. *See, e.g.,*'563 Patent 14:9-15:8, Figs. 10A, 10B. This lack of detail in the Asserted Patents is not surprising given the well-developed state of the art for ICs and packaging as discussed above.

135. Further, a POSITA understood that the implementation of Ishimaru's speedup circuit facilitated the use of resistors and capacitors of suitable size that could be implemented in an on-chip integration with the PA. Ishimaru's transistors 119/120 provide amplification to the current that charges capacitor 121 and flows to ground through resistor 136. Ishimaru Fig. 1, ¶¶55-56. Owing to the very high gain of transistors 119/120, the current in the capacitor can be made very small, and therefore the capacitor 121 can be made small for a given time constant. Likewise, the size of resistor 136 can be small as the capacitor current (I_{C121}) is generally the resistor current (I_{R136}) divided by the gain of transistors 119 and 120. This is consistent with the disclosure of the '563 Patent, which describes how amplifying $I_{CONTROL}$ with amplifier 73 allows one to "reduce a magnitude of the resistor and/or capacitor needed to generate a suitable correction current, thereby permitting the time-dependent signal generator 72 to be integrated on-chip with the power amplifier 32." '563 Patent 14:36-41.

136. Elaborating on this point, Ishimaru's speedup circuit facilitated the use of resistors and capacitors of suitable size because Ishimaru uses significant amplification of its C121 current in its speedup circuit, prevents the need for resistors or capacitors anywhere near the size that could be an impediment to on-chip integration with the PA. More specifically, a POSITA understands that Ishimaru applies a large current amplification (by virtue of transistors 119, and 120) to the transient current controlled by "capacitance element 121." (*see* Ishimaru ¶¶52, 55-56, Fig. 1 (capacitor 121, transistors 119 and 120, and resistor 136)). The current in resistor 136

[redacted]

is used to charge the capacitor 121, through transistors 119 and 120. Owing to the very high gain of transistors 119 and 120, the current in the capacitor can be made very small, and therefore the capacitor 121 can be made very small for a given time constant. This is consistent with the Asserted Patents' discussion of using amplification to allow for small components for integrated circuits. *See, e.g.,* '563 Patent 14:36-41. Likewise, the size of resistor 136 can be small as the capacitor current (I_{C121}) is the resistor current (I_{R136}) divided by the gain of transistors 119 and 120. The physical size of a resistor in an integrated circuit is directly attributable to its resistance value, *i.e.* a large resistor is physically large, and *vice versa*. The current through a small resistor, however, is larger for a given voltage. In Ishimaru, a physically small resistor can be used for resistor 136 as its current, when traced back to capacitor 121, will be greatly reduced by the gain of 119 and 120. A small resistor has the benefit of being easily implementable on an integrated circuit due to its small size. Thus, this amplification and the presence of transistors 119 and 120 — which themselves provide effective resistance — permits very small resistor and capacitor values in Ishimaru's circuit.

2. Ishimaru and Johnson

137. A POSITA would have been motivated to combine Ishimaru's teaching of a PA and bias circuit with Johnson's teachings of SiGe heterojunction bipolar transistor (HBT) PAs and packaging of such PAs and bias circuits on an IC attached to a package substrate in a packaged module.

Johnson's SiGe HBT Teachings

138. A POSITA would have been motivated to implement Ishimaru's BJT as an HBT (as taught by Johnson) for at least the following reasons.

[redacted]

139. Ishimaru expressly discloses a solution for RF PAs implemented as BJTs, and a POSITA would reasonably draw the inference that Ishimaru disclosed the use of its solution for the market leading forms of such BJTs, namely HBTs. §VIII.C.3. Indeed, it was conventional to use HBTs in the context of radio communication devices having RF PAs using BJT transistors like Ishimaru's.

140. Ishimaru is directed to an incremental improvement in the startup behavior of BJT-based RF PAs that is directed at the margin of high performing devices, i.e., the type of BJT-based RF PAs commonly implemented as HBTs. A POSITA understood that HBTs, as BJTs, suffer the same thermal effects described by Ishimaru, and would likewise benefit in the same way as other BJTs.

141. A POSITA would have been motivated to use an HBT for Ishimaru's BJT PA 103 to achieve any one of a host of known benefits such as their "improvement in the high frequency performance of the transistor" (Illingworth), their "inherently superior linearity and efficiency performance" (TriQuint), their "reliability [being] well known to be excellent" (TriQuint), and other advantages in cost, size, robustness, etc. (Yanjun). *See* §VIII.C.3. Doing so would involve nothing more than using a market-leading prior art technique (using HBT type of BJT-based RF PAs) according to conventional wisdom for the benefits and successes confirmed by the market and reported by others.

142. With respect to Johnson specifically, Johnson taught multiple advantages, that would motivate adoption of its HBT teachings, including "[e]xcellent power control," "favorable device ruggedness for PA applications," and "favorable thermal properties, lower cost of wafer processing, and the higher integration capabilities." Johnson 1610, 1612.

[redacted]

143. A POSITA would have been motivated to implement at least the power amplifier of Ishimaru as an HBT following the express teachings and benefits stated by Johnson and that were well-known in the art, as discussed above. *See also* §VIII.C.3. Doing so would involve nothing more than using a market-leading prior art technique (using HBT for PAs) according to conventional wisdom for nothing more than the benefits reported and successful adoption of the technique by others. Moreover, there were only a finite number of suitable BJTs to use for PAs, and a POSITA would have been motivated to try at least the ones that had been reported positively, including SiGe HBTs such as Johnson's.

144. Finally, there would have been nothing technologically counterintuitive about implementing Ishimaru's PA system with an HBT as compared to other forms of a BJT. Indeed, the Asserted Patents reference HBTs in passing, without any special significance, criticality, challenges, or counterintuitive concepts or properties. *See, e.g.,* '101 Patent 7:53-55. This lack of detail is consistent with the well-developed state of the art for HBT RF PAs. *See* §VIII.C.3. Furthermore, the selection of a market-leading BJT type (HBT) would have been viewed with a reasonable expectation of success with predictable benefits, all well within the skill of a POSITA as demonstrated by the popularity of HBTs in the marketplace.

Johnson's Packaging Teachings

145. A POSITA would have been motivated to combine Ishimaru's teaching of a PA and bias circuit with Johnson's packaging teachings of implementing a PA and bias circuit on an IC attached to a package substrate in a packaged module for at least the reasons set out above with respect to Ichitsubo's teachings. §IX.C.1.

146. Johnson is an express disclosure of the type of IC packaging that a POSITA already understands would be used for Ishimaru. Further, a POSITA would have been motivated

[redacted]

to combine Johnson's express packaging teaching with Ishimaru by any one of the numerous and well-known advantages of packaged ICs. §VIII.C.4.

147. A POSITA also would have found motivation in the express teachings and suggestions of Johnson itself. For example, Johnson teaches that focusing on whole system PA design and "adopting the chip-partitioning strategy best suited for the particular radio architecture" results in "advantages in terms of performance, cost, and size." Johnson 1605. Johnson explains that the solution of SiGe BiCMOS flip-chip together with LTCC allows for integration of bias circuitry into the PA "making the PA module simpler and more cost-effective." Johnson 1609. Johnson explains that its solution is a "very strong path for PA modules" and "exhibits superior performance and stability together with a low component count for the entire front-end solution." Johnson 1612.

148. In other words, Johnson expressly teaches benefits of packaging readily applicable to Ishimaru's PA and bias circuit for its intended use with "radio communication devices." Ishimaru Abstract. A POSITA would have been motivated to follow these teachings in Johnson to predictably achieve a compact, reliable fabrication of Ishimaru's PA and bias circuit. Ishimaru ¶¶42-52; Johnson 1609, 1612.

149. Further, a POSITA would have a reasonable expectation of success in implementing Ishimaru's teachings following Johnson's packaging teachings of a PA module because implementing a power amplifier and bias circuit on an IC inside a packaged module was no more than the routine exercise of skill for a POSITA making the PA module simpler and more cost effective. §VIII.C.4 (discussing *e.g.*, Doherty ¶¶58-60, 89; Marra ¶¶65-68; Hedberg 2:37-43). Nor is there anything counterintuitive, technologically challenging, or unique about

[redacted]

the notion of the claimed integration and packaging, as the state of the art for ICs and packaging was well-developed as discussed above.

3. Ishimaru and Harrison

150. I discuss the motivation to combine Ishimaru and Harrison in §IX.D.2 below.

D. Detailed Opinions Relating to the Invalidity of the '563 Patent Based on Prior Art

151. For the reasons detailed below, it is my opinion that claims 14, 15, 17, and 20 of the '563 patent are invalid based on the disclosure of one or more prior art references.

152. My citations below to one or more references are merely exemplary and representative of the disclosure in the various prior art references. In no way should the citations below be considered limiting or the only relevant disclosure in any prior art reference.

1. Claims 14, 15, 17, and 20 are Obvious over Ishimaru Alone or, Alternatively, Ishimaru in View of Ichitsubo or Johnson

Claim 14

[14.0] A packaged module comprising:

[14.1] a package substrate; and;

[14.2] an integrated circuit attached to the package substrate and including

153. Ishimaru alone or, alternatively, Ishimaru in view of Ichitsubo or Johnson discloses these limitations.

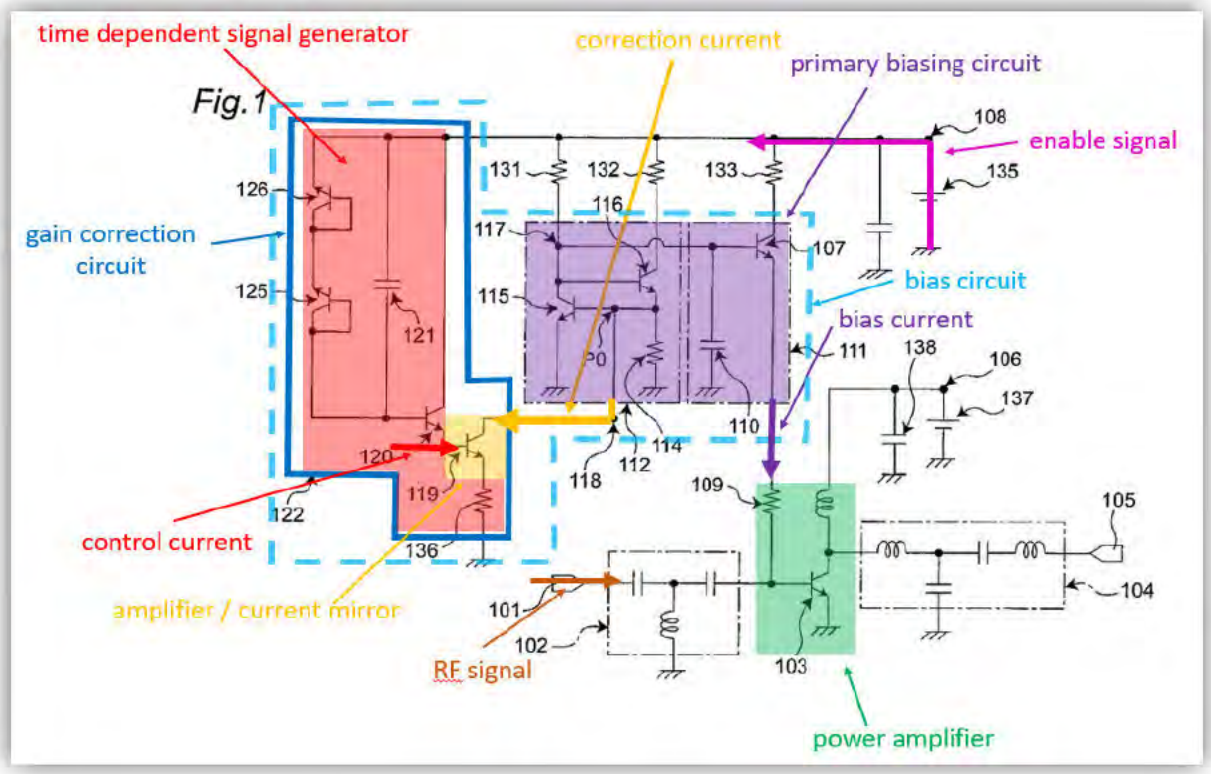
154. Ishimaru discloses a PA (green) and bias circuit (blue) for use in a radio communications devices. Ishimaru Abstract, ¶1, Fig. 1; *see, e.g.*:

> In the power amplifier of the invention, at a start of power amplification by an amplifier transistor 103 serving as an amplification section, a speedup circuit 122 transiently increases a bias which is fed to the amplifier transistor 103 via a bias power source section composed of a bias circuit 111 and a power source circuit 112. As a result, the power amplification factor of the amplifier transistor 103 is

[redacted]

transiently increased at the start of power amplification by the amplifier transistor 103. Thus, the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal such as a modulated-wave signal. Accordingly, in the invention, it becomes possible to suppress distortion increases of an amplification signal due to heat generation at the start time without using any temperature sensing element.

Ishimaru Abstract.



Ishimaru Fig. 1 (annotated).

155. While Ishimaru does not expressly describe the extra detail of its PA (green) and bias circuit (blue) being in an *integrated circuit attached to* a *package substrate* as part of a *packaged module* as claimed, that is nonetheless understood by a POSITA for several reasons. First, Ishimaru discloses that its PA and bias circuit is for "a high frequency power amplifier **to be used in radio communication devices or the like.**" Ishimaru Abstract ¶1. A POSITA

[redacted]

readily understood that the overwhelming majority of these types of circuits were designed as packaged ICs. Laplante 003 ("die[s] or chips have to ultimately be packaged to be useful."); Johnson 1609, 1612, Fig. 17; Diels Fig. 2; Hedberg; §VIII.C.4; *see, e.g.*:

> **package** in MMIC technology, die or chips have to ultimately be packaged to be useful. An example of a package is the T07 "can." The MMIC chip is connected within the can with bond wires connecting from pads on the chip to lead pins on the package. The package protects the chip from the environment and allows easy connection of the chip with other components needed to assemble an entire system, such as a DBS TV receiver.

Laplante 003.

156. Second, Ishimaru is directed to an incremental improvement in the startup behavior of PAs that is directed at the margin of high performing devices, *i.e.*, the type implemented in packaged ICs.

157. Third, Ishimaru is directed to improvements in the startup behavior of PAs, which requires additional circuitry. Such additional circuitry would be routine and expected to be integrated into an IC and packaged.

158. For these reasons, a POSITA reading Ishimaru in 2011 understood that Ishimaru's "radio communication device" with its PA (green) and bias circuits (blue) would be implemented in *an integrated circuit attached to a package substrate in a packaged module* as claimed. Thus, while not explicitly stated, it is my opinion that the packaging limitations claimed are nonetheless disclosed to a POSITA in view of the reasonable inferences that a skilled artisan would draw when reading Ishimaru.

(a) Ishimaru in view of Ichitsubo

159. To the extent it is argued that Ishimaru does not explicitly state that PA (green) and bias circuits (blue) in a "radio communication device" would be implemented in *an*

[redacted]

integrated circuit attached to a package substrate in a packaged module as claimed, Ishimaru in view of Ichitsubo discloses this limitation.

160. It is my opinion that a POSITA would have been motivated to implement Ishimaru's PA (green) and bias circuit (blue) in the form of *an integrated circuit attached to a package substrate* as part of *a packaged module* in view of Ichitsubo, for the reasons described in the Motivation to Combine section above (§IX.C.1) and as I further explain below.

(1) Packaged Module

161. Referencing Figure 1 (below), Ichitsubo describes a "radio frequency power amplifier (PA) module 14" (*packaged module*) (gray). Ichitsubo ¶ 25; *see, e.g.*:

> FIG. 1 shows a system diagram of the radio frequency power amplifier (PA) module 14 for wireless communications in accordance to an embodiment of the present invention. The PA module is built on a module substrate 12, which can be a multiplayer printed circuit board (PCB), lead frame, lower-temperature co-fired ceramics (ITCC), or other suitable electronic materials. The substrate includes metal pins adapted to receive connecting terminals of integrated circuits including the Power Amplifiers 24, the Bias Circuit 22, the Power Sensor 26, and optionally Control Logic 28. The Power Amplifiers 24, the Power Sensor 26, the Bias Circuit 22, can be fabricated in an integrated circuit on a semiconductor chip. The Power Amplifiers 24 can be of one or multiple Stages. In the particular example shown in FIG. 1, two Sequentially connected Stages of power transistors are employed. The power amplifier IC has an electrically conductive metal layer to be bonded to the top metal layer of the module. The power amplifier IC 24 can also include, in accordance with another feature of the present invention, input impedance matching circuit 18 and output impedance matching circuit 20. The input and output impedance matching networks are prefer ably based on the 50-ohm standard of the RF industry.

Ichitsubo ¶25. The PA module is a *packaged module* in that it contains, simplifies and protects, *i.e.* packages, one or more ICs in a unitary module for assembly into larger device. Ichitsubo ¶¶3, 24, 84; *see, e.g.*:

> The PA module provides a unitary or common component which may be conveniently assembled in a RF transmission device, with correspondingly simplified assembly, compact 3D size, and enhanced RF amplification performance. In accordance with the present invention, the term "module" refers to

[redacted]

such a unitary device for wireless communications, comprising integrated power amplifiers and other circuitry and auxiliary electronic components.

Ichitsubo ¶24.

FIG. 8 shows a cross-sectional view of another embodiment of an RF module 800. The module 800 encapsulates circuit elements in a molding 802 such as a plastic molding. Pins 820 are provided to provide electrical I/Os for the module. The pins 820 are connected to active or passive substrates 806-808 using chip to pin wire-bonds 818. The substrates 806-808 are bonded to a die pad 804 using die bond 810, which can be a suitable epoxy or can be solder, among others. Additionally, connections inside a chip can be wire-bonded using intra-chip wire-bond 812. Moreover, connections between chips can be wire-bonded using interchip wire-bonds 814. In one embodiment, the pins can be gold plated (Au Plating). A ground base of nickel plating is provided to attach one or more dies thereto. Wires are bonded between the dies and the gold-plated pins. The entire assembly is then **encapsulated** in a mold to **protect the power amplifier from environmental variables** such as humidity and temperature and physical stress, among others.

Ichitsubo ¶84 (emphasis added).

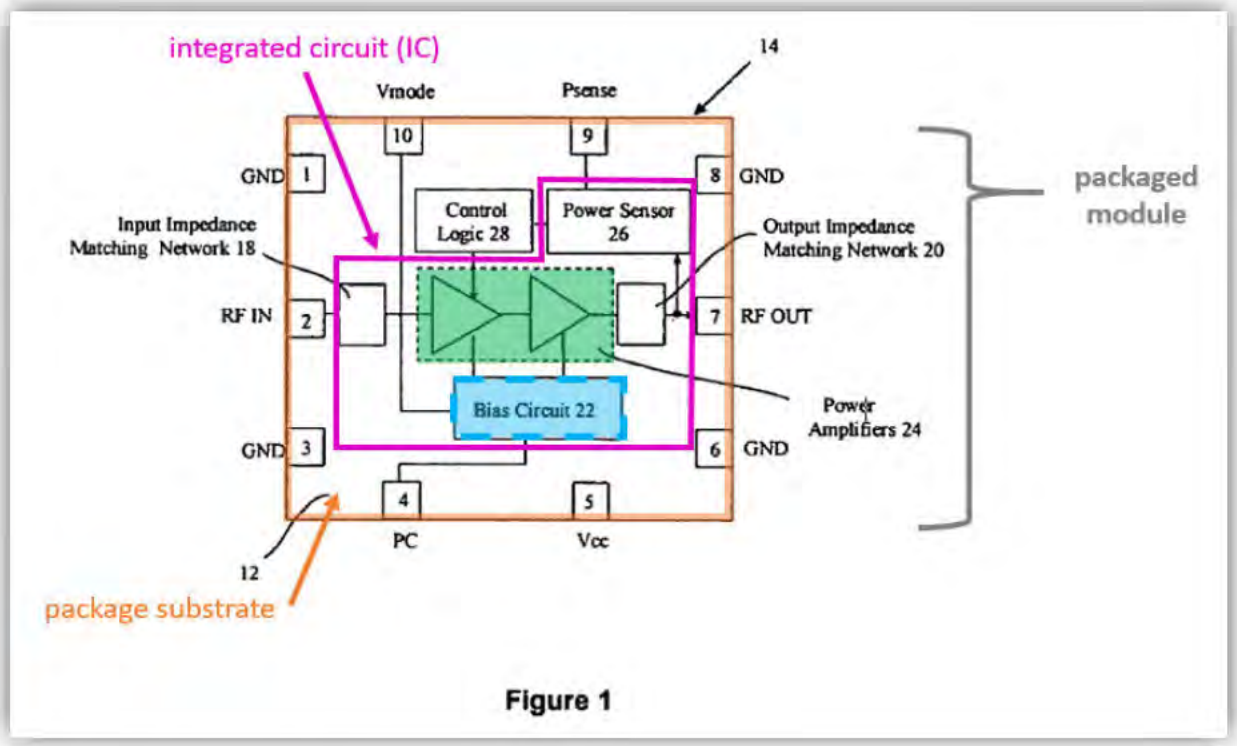


Figure 1

Ichitsubo Fig. 1 (annotated).

[redacted]

(2) Integrated Circuit

162. Ichitsubo's packaged module includes *an integrated circuit* (pink). Specifically, Ichitsubo teaches that a PA and bias circuit, plus more various circuitry ("input impedance matching network 18, the output impedance matching network 20, the power amplifiers 24, the bias circuit 22 and the power sensor 26"), are "integrated on an integrated circuit (IC)" conventionally in the form of a "semiconductor integrated circuit (IC) chip or die" (*integrated circuit*) (pink). Ichitsubo ¶¶3, 25, 38; *see, e.g.*:

> A major component of the wireless communication device is the radio frequency PA. **The PA is conventionally in the form of a semiconductor integrated circuit (IC) chip or die in which signal amplification is effected with substantial power**. The amplifier chip is interconnected in a circuit with certain off-chip components such as inductors, capacitors, resistors, and transmission lines used for controlling operation of the amplifier chip and providing impedance matching of the input and output RF signals. The amplifier chip and associated components are typically assembled, on a printed circuit board (PCB) in which the components are interconnected by layers printed metal circuits and layers of dielectric substrates.

Ichitsubo ¶3 (emphasis added).

> FIG. 1 shows a system diagram of the radio frequency power amplifier (PA) module 14 for wireless communications in accordance to an embodiment of the present invention. The PA module is built on a module substrate 12, which can be a multiplayer printed circuit board (PCB), lead frame, lower-temperature co-fired ceramics (ITCC), or other suitable electronic materials. The substrate includes metal pins adapted to receive connecting terminals of integrated circuits including the Power Amplifiers 24, the Bias Circuit 22, the Power Sensor 26, and optionally Control Logic 28. **The Power Amplifiers 24, the Power Sensor 26, the Bias Circuit 22, can be fabricated in an integrated circuit on a semiconductor chip**. The Power Amplifiers 24 can be of one or multiple stages. In the particular example shown in FIG. 1, two sequentially connected stages of power transistors are employed. The power amplifier IC has an electrically conductive metal layer to be bonded to the top metal layer of the module. The power amplifier IC 24 can also include, in accordance with another feature of the present invention, input impedance matching circuit 18 and output impedance matching circuit 20. The input and output impedance matching networks are prefer ably based on the 50-ohm standard of the RF industry.

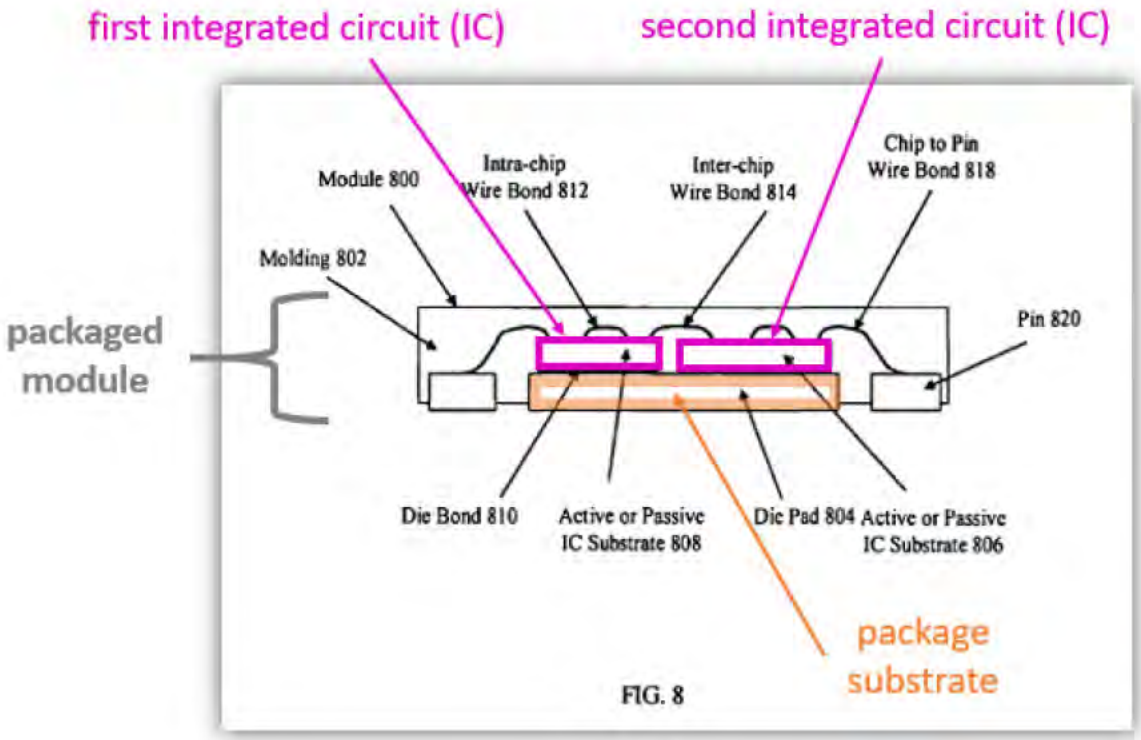
Ichitsubo ¶25 (emphasis added).

[redacted]

> In one embodiment, the input impedance matching network 18, the output impedance matching network 20, **the power amplifiers 24, the bias circuit 22 and the power sensor 26 are integrated on an integrated circuit (IC).** The IC includes top terminals or bonding Pins which provide various input and output connections to the internal components of the chip. The top terminals are electrically joined to one or more of the plates in the module Substrate 12. In the preferred embodiment, the chip includes Gallium Arsenide Heterojunction Bipolar Transistors (GaAs HBT). However, other Semiconductor materials may also be used.

Ichitsubo ¶38 (emphasis added).

163. Under Complainant's construction, an IC can include integration across multiple dies (§VII.C), but that does not distinguish the art, which likewise discloses a packaged module having multiple chips integrated therein on a common package substrate:



Ichitsubo Fig. 8 (annotated).

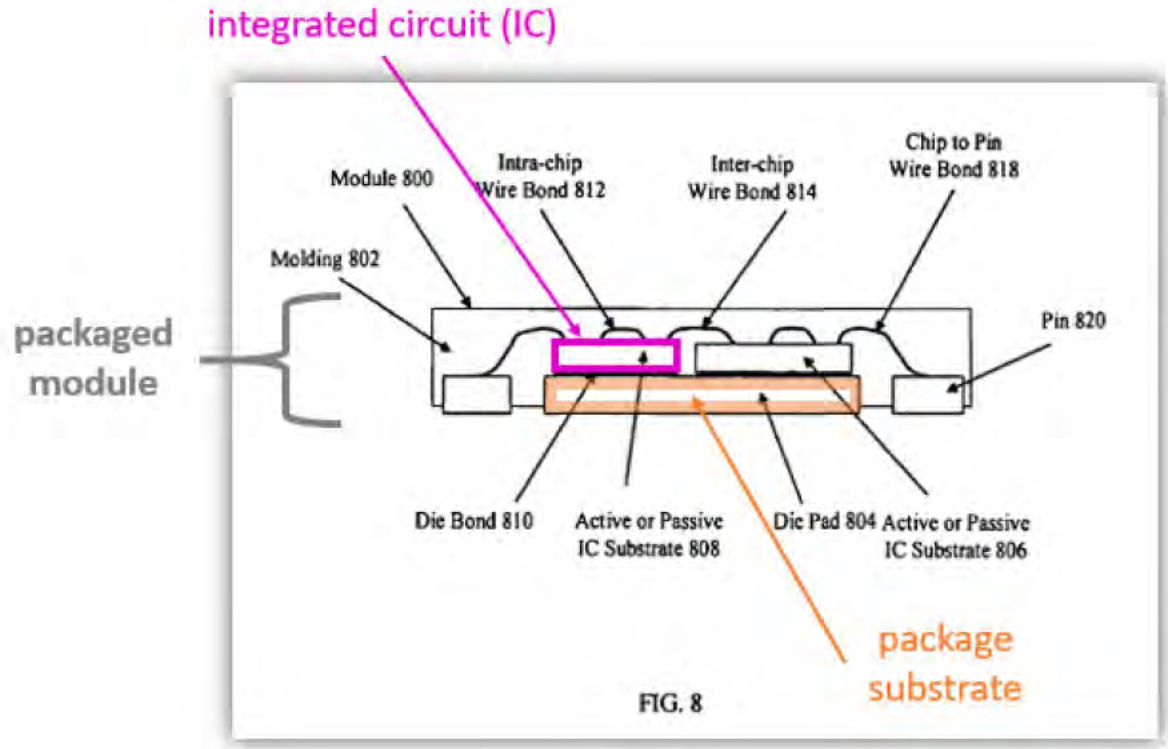
164. Thus, even under Complainant's one-or-more-chip construction, Ichitsubo not only literally discloses that (since it discloses all the claimed components on one chip) but the

[redacted]

relaxed/reduced degree of integration would be even more easily accomplished on multiple dies for the same reasons (*e.g.* miniaturization, efficiency) set forth above.

(3) Package Substrate

165. As illustrated in Fig. 8, Ichitsubo also teaches that the PA module has a variety of "module substrate 12" (*package substrate*) (brown) types, including a "multiplayer printed circuit board (PCB), lead frame, lower-temperature co-fired ceramics (LTCC), or other suitable electronic materials." This "RF power amplifier module includes a **multi-layer three-dimensional substrate** having a bottom metal layer adapted to bond with the printed circuit board (PCB) of a wireless communications device" and this substrate "has one or more upper layers adapted to receive the amplifier chip and other off-chip components" (*integrated circuit attached to the package substrate*). The IC is electrically connected and otherwise secured to the package substrate (*integrated circuit attached to the package substrate*). For example, the PA "is **built on** a module substrate 12," which "has one or more upper **layers adapted to receive** the amplifier chip." Ichitsubo ¶ 29 (emphases added). Furthermore, referencing Figure 8 (below), Ichitsubo discloses that its integrated circuits can be "**bonded**" to a substrate (e.g. die pad 804) "using die bond 810." Ichitsubo ¶ 84 (emphasis added).



Ichitsubo Fig. 8 (annotated).

(b) Ishimaru in view of Johnson

166. In the alternative, to the extent it is argued that Ishimaru does not explicitly state that power amplifier (green) and bias circuits (light blue) in a "radio communication device" would be implemented in *an integrated circuit attached to a package substrate in a packaged module* as claimed, Ishimaru in view of Johnson discloses this limitation.

167. It is my opinion that a POSITA would have been motivated to implement Ishimaru's PA (green) and bias circuit (blue) in the form of *an integrated circuit attached to a package substrate* as part of *a packaged module* in view of Johnson, for the reasons described in the Motivation to Combine section above (§IX.C.2) and as I further explain below.

[redacted]

168. Refencing Fig. 12 (below), Johnson describes the major components of a BiCMOS HBT die including bias and power control circuitry, voltage regulation, and temperature compensation integrated directly into the PA. Johnson, 1609.

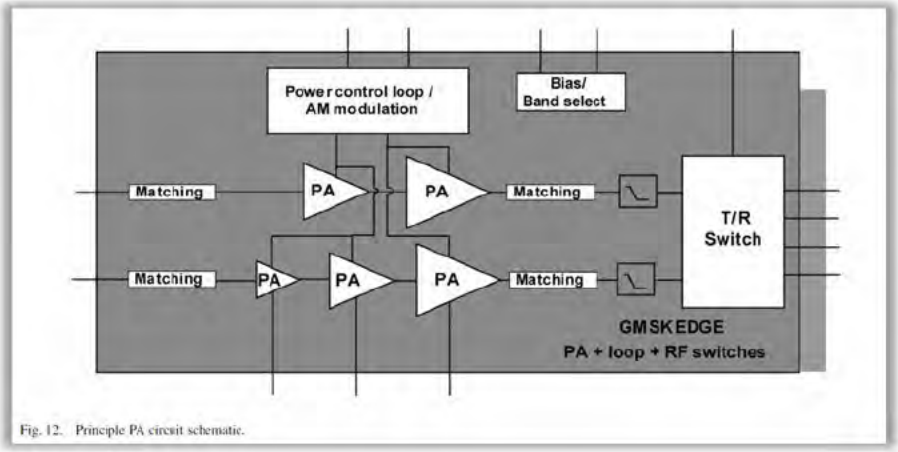


Fig. 12. Principle PA circuit schematic.

Johnson Fig. 12.

169. Johnson discloses a "die" (*integrated circuit*) that is flip chip mounted onto a "low-temperature-cured ceramic (LTCC) provide a very low thermal resistance" (*a package substrate*). The substrate surface "thereby providing extremely low parasitic inductance and good thermal conductivity together with a small footprint." Johnson 1610. Johnson further discloses that the SiGe BiCMOS flip chip (*integrated circuit*) together with "LTCC" (*the package substrate*) "is a very strong path for PA modules." (*packaged module*). Johnson, p. 1612.

170. Johnson concludes with the following paragraph:

> PA designs have been demonstrated for GSM, GPRS, and EDGE wireless standards using a SiGe HBT technology. The GPRS/EDGE FEM shown here exceeds the 15:1 VSWR requirement at 33 dBm with an overall efficiency of 37%. The SiGe HBT was optimized to simultaneously provide ruggedness and speed and is compatible with the base 0.5 um CMOS. The favorable thermal properties, lower cost of wafer processing, and the higher integration capabilities demonstrated by these SiGe PAs make them a compelling choice for wireless applications. A SiGe BiCMOS flip-chip together with LTCC is a very strong path for PA modules. The

[redacted]

> combined module exhibits superior performance and stability together with a low component count for the entire front-end solution.

Johnson 1612.

171. This paragraph and its reference to "a strong path for PA modules" is discussing modules for use in a larger electronic product, namely as part of "the entire front-end solution" for wireless applications using cellular telephone standards (GSM, GPRS, and EDGE), *i.e.* in cell phones. *Id.* A POSITA understood this to include modules *packaged* as required for integration and use in the referenced larger electronic systems.

172. As shown in Fig. 17 (below), Johnson discloses a photo of the die (*integrated circuit*) containing modulator, power amplifiers, biasing circuits, switch, and associated circuitry.

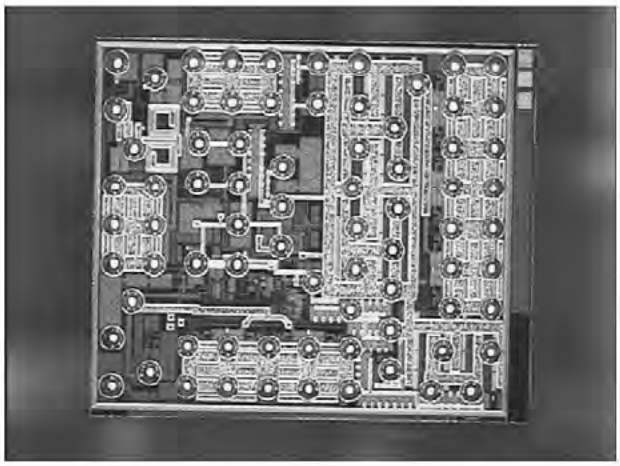


Fig. 17. EDGE FEM die, including two PAs, an antenna switch, and an AM modulator using PMOS.

Johnson Fig. 17, 1612.

[14.2.1] a power amplifier configured to provide amplification to a radio frequency signal and

173. Ishimaru discloses this limitation. Ishimaru discloses "a high-frequency power amplifier to be used in radio communication devices." Ishimaru ¶ 1. The circuitry for the PA includes "an amplification section having a first transistor for performing power amplification"

[redacted]

(green) (*a power amplifier configured to provide amplification*), as well as "a bias power source section" and "a speedup circuit." Ishimaru ¶¶10-12; *see, e.g.*:

> an amplification section having a first transistor for performing power amplification;

Ishimaru ¶10.

> a bias power source section having a second transistor for feeding a bias to the first transistor; and

Ishimaru ¶11.

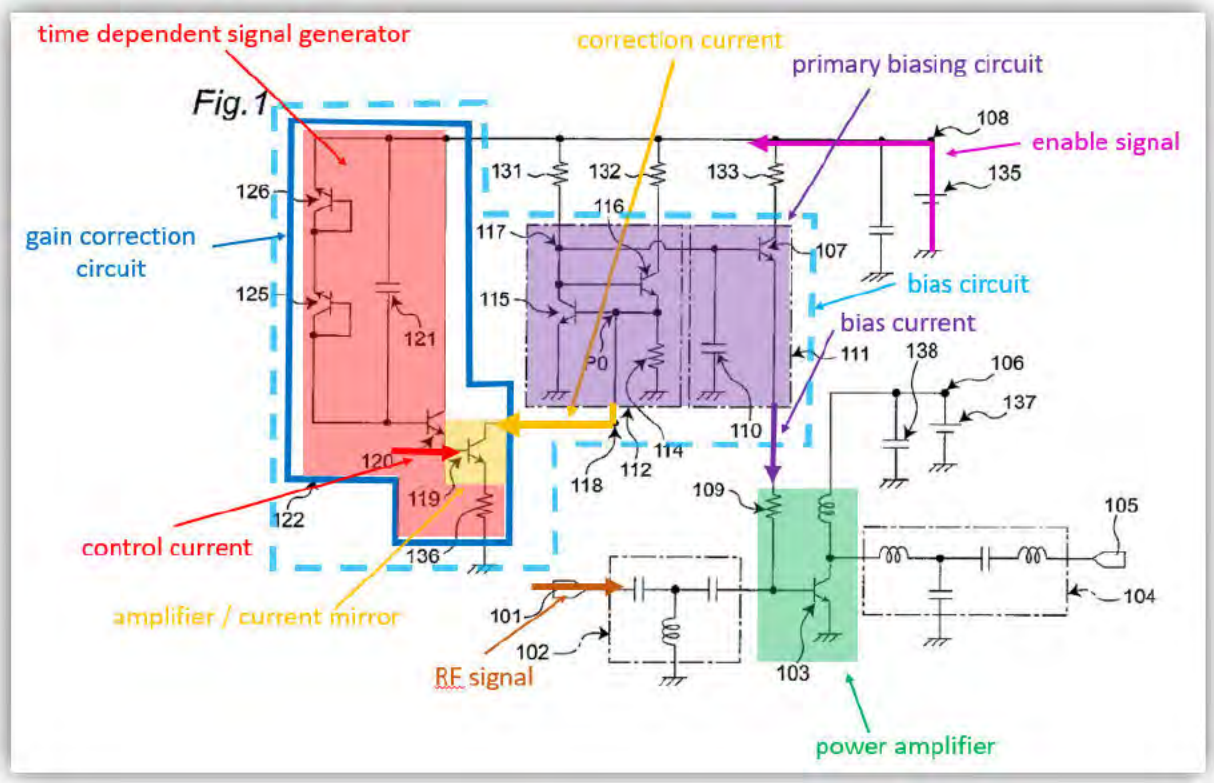
> a speedup circuit for transiently increasing the bias fed to the first transistor by bias power source section at a start of the power amplification.

Ishimaru ¶12.

174. As illustrated in Figure 1 (annotated below), Ishimaru further discloses that "a high-frequency signal as an input signal [is] inputted from an input signal terminal 101, … is amplified by an amplifier transistor 103 serving as a first transistor, and then, … outputted from an output signal terminal 105." Ishimaru ¶42; *see, e.g.*:

> In this power amplifier, a high-frequency signal as an input signal inputted from an input signal terminal 101, passing through an input matching circuit 102, is amplified by an amplifier transistor 103 serving as a first transistor, and then, after passing through an output matching circuit 104, outputted from an output signal terminal 105. In FIG. 1, reference sign 106 denotes a collector bias terminal of the amplifier transistor 103. Between the collector bias terminal 106 and the ground are connected a DC power source 137 and a capacitance element 138. The amplifier transistor 103 forms an amplification section.

Ishimaru ¶42.



Ishimaru Fig. 1 (annotated).

175. Because Ishimaru is directed to a PA for a radio communications device, it is my opinion that a POSITA reading Ishimaru understood that the high-frequency input signal at input terminal 101 is a *radio frequency signal* (brown arrow) for amplification by amplifier transistor 103 (*a power amplifier configured to provide amplification*) to generate an amplified radio frequency signal at output terminal 105.

[14.2.2] a bias circuit configured to receive a power amplifier enable signal and to generate a bias signal that biases the power amplifier, the bias circuit including

176. Ishimaru discloses this limitation. As shown in Figure 1, Ishimaru discloses a "speedup circuit 122," "power source circuit 112," and "bias circuit 111" (collectively, *a bias circuit*) (light blue) that receives a "control voltage from voltage source 135" (*power amplifier*

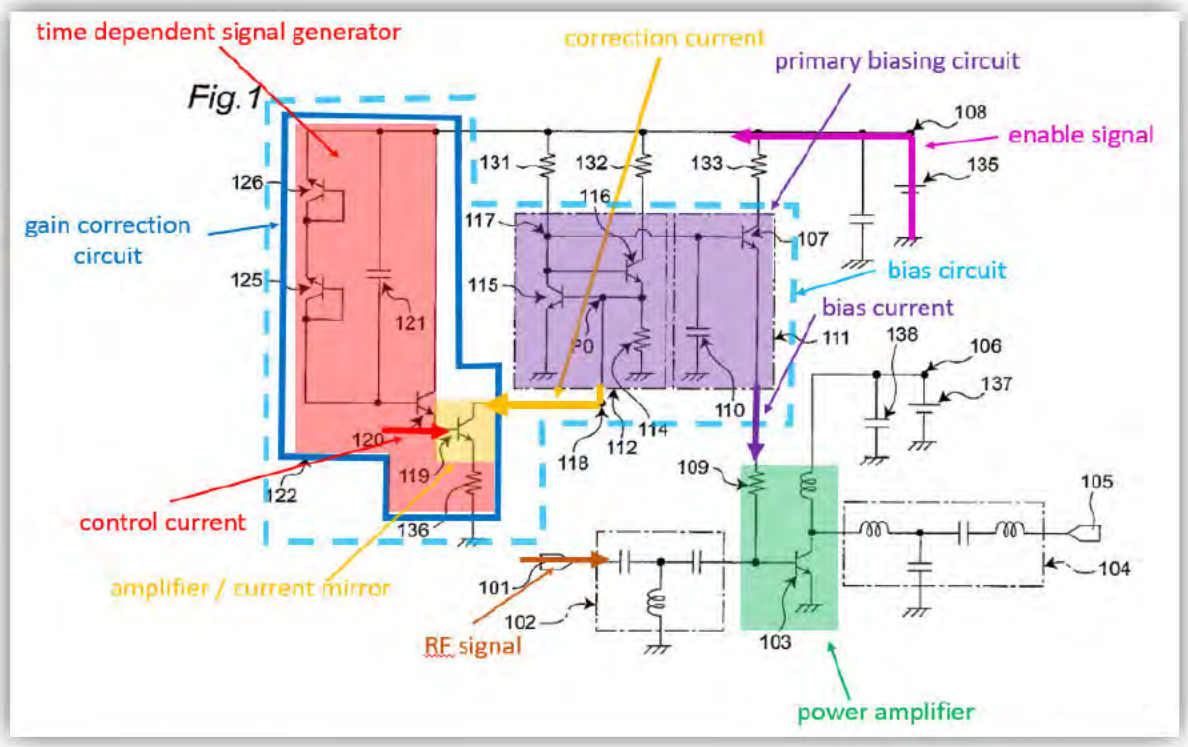
[redacted]

enable signal) (pink arrow) and supplies a "base bias current" (*generate a bias signal*) (purple arrow) to the "base terminal of amplifier transistor 103" (*biases the power amplifier*) (green).

Ishimaru Abstract, ¶¶24, 31, 49-52; *see, e.g.*:

> In the power amplifier of the invention, at a start of power amplification by an amplifier transistor 103 serving as an amplification section, a speedup circuit 122 transiently increases a bias which is fed to the amplifier transistor 103 via a bias power source section composed of a bias circuit 111 and a power source circuit 112. As a result, the power amplification factor of the amplifier transistor 103 is transiently increased at the start of power amplification by the amplifier transistor 103. Thus, the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal such as a modulated-wave signal. Accordingly, in the invention, it becomes possible to suppress distortion increases of an amplification signal due to heat generation at the start time without using any temperature sensing element.

Ishimaru Abstract.



Ishimaru Fig. 1 (annotated).

[redacted]

177. Ishimaru discloses two distinct power sources, denoted as ("⊣⊢") in Fig. 1 (above) to serve distinct functions. The first power source, DC voltage 137, is connected to provide a constant DC power to amplification transistor 103. Ishimaru ¶42. The second power source, control voltage source 135 (*an enable signal*) at bias terminal 108, "controls turn-on and -off of power amplification." Ishimaru ¶24; *see, e.g.*:

> Accordingly, in this invention, at the start of power amplification, i.e., immediately after the control voltage source that controls turn-on and -off of the power amplification is turned on so that the bias voltage is applied from the control voltage source to the first transistor via the bias power source section, the current following into the base of the first transistor is transiently increased by the speedup circuit. As a result of this, variations in the operating current due to heat generation of the power amplifier or the like can be canceled, by which variations in amplification factor can be suppressed, and improvement of the linearity can be achieved. That is, without use of any temperature sensing element, since the speedup circuit enabled to adjust the transient response of the operating current is connected to the bias power source section, distortion increases of the amplification signal (modulated-wave signal) due to heat generation can be suppressed.

Ishimaru ¶24. Thus, Ishimaru's control voltage is *a power amplifier enable signal*. The operation of Ishimaru's voltage source 135 is consistent with the '563 Patent's description that "an enable signal that can be used to enable or disable the power amplifier so as to pulse the power amplifier's output." '563 Patent 4:29-31.

178. As explained in limitations 14.2.2.1-2 below (§IX.D.1 ([14.2.2.1]-[14.2.2.2])) Ishimaru further discloses that, in response to the control voltage from source 135 being turned on (*power amplifier enable signal*), the I_{BIAS} (*bias signal*) that is applied to the base of amplifier transistor 103 transiently (temporarily) increases due to the operation of the speedup circuit 122, power source circuit 112, and bias circuit 111 (*configured to . . . generate a bias signal that biases the power amplifier*). Ishimaru ¶31; *see, e.g.*:

> According to the power amplifier of this embodiment, by electric charge flowing into the capacitance element at a rise time of the control voltage of the control voltage source (upon turn-on of the amplifier), a current transiently (temporarily)

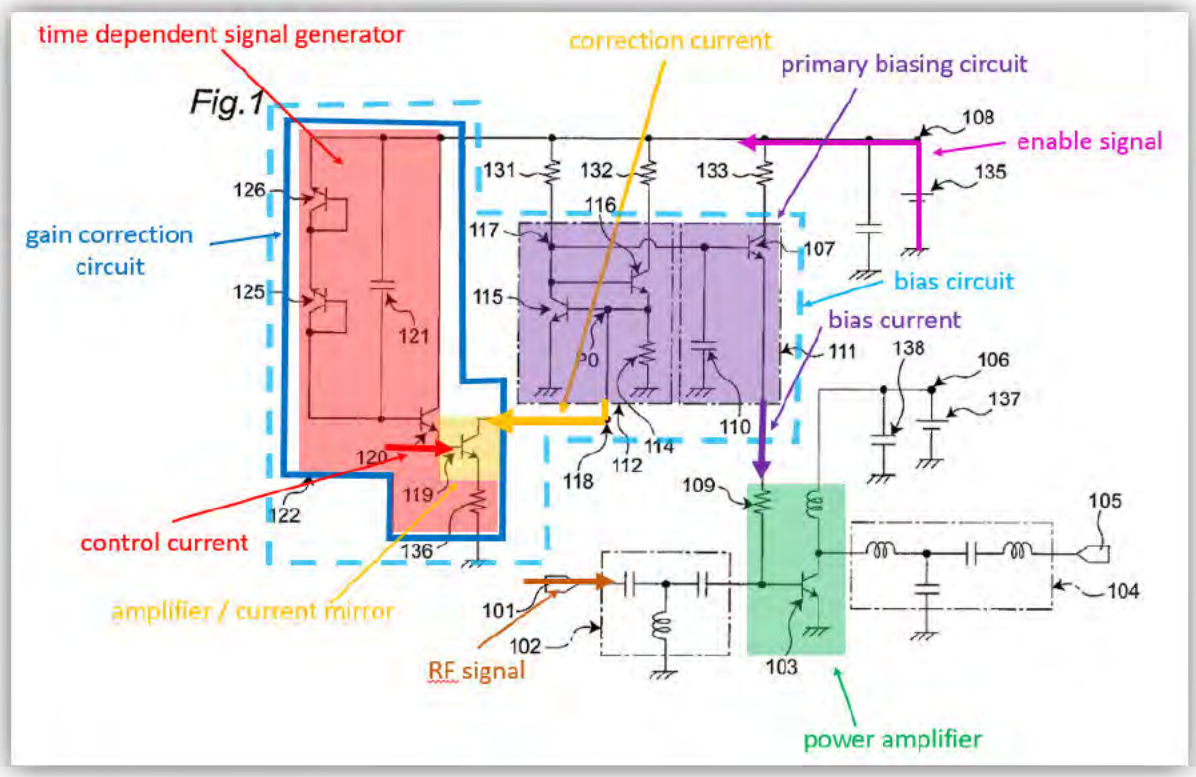
[redacted]

flows into the collector of the fifth transistor, causing the voltage value of the collector to lower. As a result, due to a change of the bias point of the third transistor, the voltage of the connecting terminal at which the collector of the third transistor is connected to the base of the second transistor is temporarily increased. Thus, the current fed to the first transistor by the second transistor is transiently increased at the rise time. Therefore, the power amplification factor of the first transistor is transiently increased at the rise time, so that the time elapsing until temperature variations due to heat generation of the first transistor come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).

Ishimaru ¶31.

[14.2.2.1] a gain correction circuit configured to generate a control current in response to activation of the power amplifier enable signal and to mirror the control current to generate a correction current

179. Ishimaru discloses this limitation.



Ishimaru Fig. 1 (annotated).

[redacted]

180. With reference to Figure 1, Ishimaru discloses a speedup circuit 122 (*gain correction circuit*) (dark blue) that includes a capacitance element 121, diodes 125 and 126, transistors 119 and 120, and resistance element 136. Ishimaru ¶¶50-51; *see, e.g.*:

> The speedup circuit 122 has a fifth transistor 119 whose collector is connected to the output terminal 118, and a sixth transistor 120 whose emitter is connected to a base of the fifth transistor 119. The emitter of the fifth transistor 119 is connected to the ground via a resistance element 136.

Ishimaru ¶50.

> The speedup circuit 122 also has a capacitance element 121 which is connected between a base of the sixth transistor 120 and the bias terminal 108, and two diodes 125, 126 which are connected in series between the base of the sixth transistor 120 and the bias terminal 108.

Ishimaru ¶51. In response to the "rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier)," (*activation of the power amplifier enable signal*) (pink arrow), the speedup circuit applies a transient or time-varying current to the base of transistor 119 (*control current*) (red arrow). Ishimaru ¶52. This is a control current at least because it is used to control the correction to the biasing of Ishimaru's PA to compensate for gain variation, as discussed next.

181. This $I_{CONTROL}$ (red arrow) is amplified by transistor 119, resulting in a transient current being pulled into the collector of transistor 119 from node 118, *a correction current*, $I_{CORRECTION}$ (gold arrow). Ishimaru ¶52; *see, e.g.*:

> In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the

[redacted]

> time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).

Ishimaru ¶52.

182. Ishimaru's speedup circuit 122 (dark blue) is a *gain correction circuit* in that it is a circuit for gain correction of Ishimaru's power amplifier (green) and is configured to *generate a control current in response to activation of the power amplifier enable signal and to mirror the control current to generate a correction current*, as already explained. The speedup circuit 112 (dark blue) shapes the $I_{CORRECTION}$ (gold arrow) as a "current that transiently (temporarily) flows" out of the PA's *primary biasing circuit* (purple). Ishimaru ¶52. This $I_{CORRECTION}$ (gold arrow) is shaped in an amount and duration necessary to cause the *primary biasing circuit* to send a corresponding temporary boost in I_{BIAS} to the PA (green) to boost its gain during the startup period when it would otherwise be too low, *i.e.* to correct for the gain variation of the PA. Ishimaru ¶52.

183. More specifically, Ishimaru discloses:

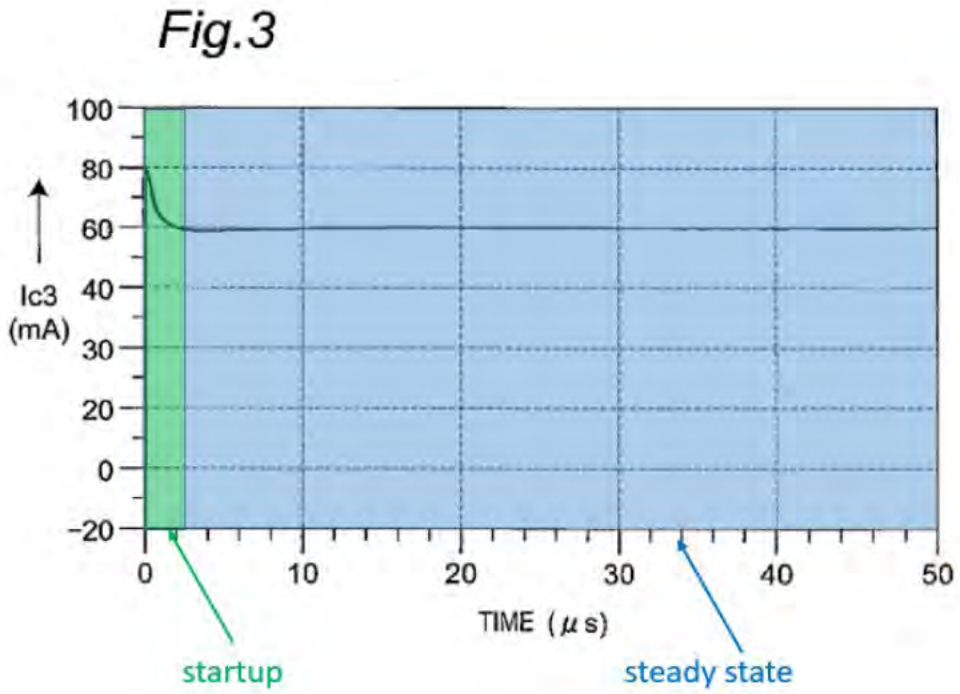
> Thus, occurrence of **distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed**, so that the **linearity** of the circuit in burst operation is **improved**. That is, **gain variations** due to collector current variations of the **power amplifier** using a bipolar transistor **can be compensated.**

Ishimaru ¶54 (emphases added).

184. The speedup circuit/gain correction circuit (dark blue) achieves this PA gain correction by shaping the $I_{CORRECTION}$ (gold arrow) to cause a temporary voltage increase at the base of transistor 107 in the *primary biasing circuit* (purple), which transiently boosts the amount of "bias base current" (*bias signal*), i.e., an I_{BIAS} (purple arrow) supplied to bias the PA's amplifier transistor 103. Ishimaru ¶52. That transiently boosts the gain of the PA based on the

[redacted]

$I_{CORRECTION}$, compensating for the low gain of PA at startup. Ishimaru ¶52. This boost is shown by the increased collector current through amplifier transistor 103 during startup shown in annotated Figure 3 of Ishimaru below.



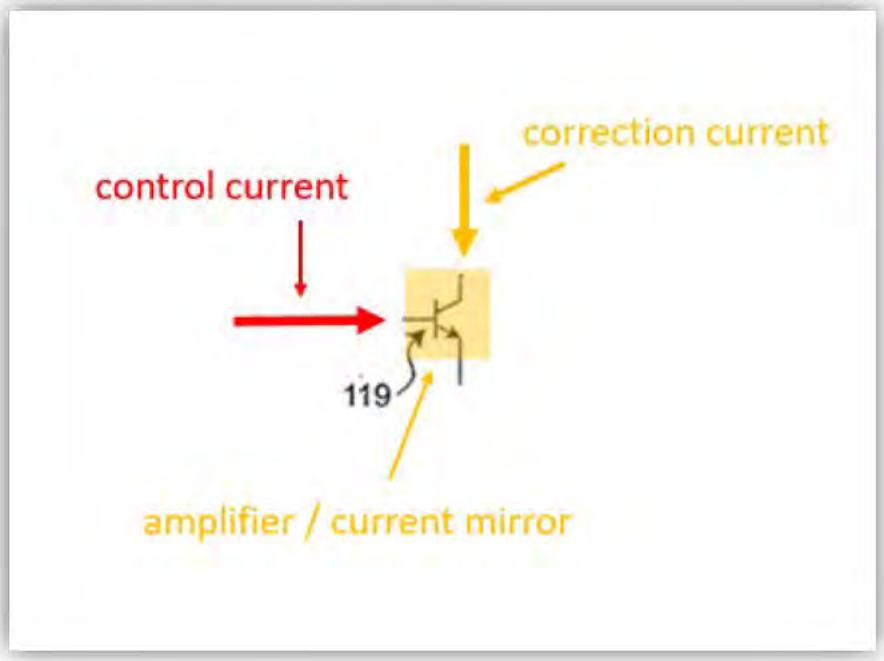
Ishimaru Fig. 3 (annotated).

185. Thus, it is my opinion that a POSITA reviewing Ishimaru understood that the base current applied to transistor 119 is an $I_{CONTROL}$ (red arrow) because it controls generation of transistor 119's collector current $I_{CORRECTION}$ (gold arrow), which, in turn, ultimately controls I_{BIAS} (purple) generated by bias circuit 111 that is applied to the base of amplifier transistor 103, thus leading to the transient increase in the collector current through the PA transistor to correct the gain of the power amplifier.

(a) Configured to Mirror

[redacted]

186. As shown in Fig. 1, partially reproduced below, Ishimaru's transistor 119 is a current mirror that is configured to replicate, *i.e.*, *configured to mirror* (gold) the $I_{CONTROL}$ (red arrow) to generate the $I_{CORRECTION}$ (gold arrow).



Ishimaru Fig. 1 (annotated) (partial).

187. Consistent with the discussion of current mirrors in the State of the Art section, transistor 119 as connected in Ishimaru is configured to mirror in that it is configured to replicate (reproduce, duplicate, reflect, etc.), *i.e., mirror* the current at its input (the base of transistor 119) to generate the current at its output (the collector of transistor 119). *See supra* §VIII.C.2; *see also* Ishimaru Fig. 1.

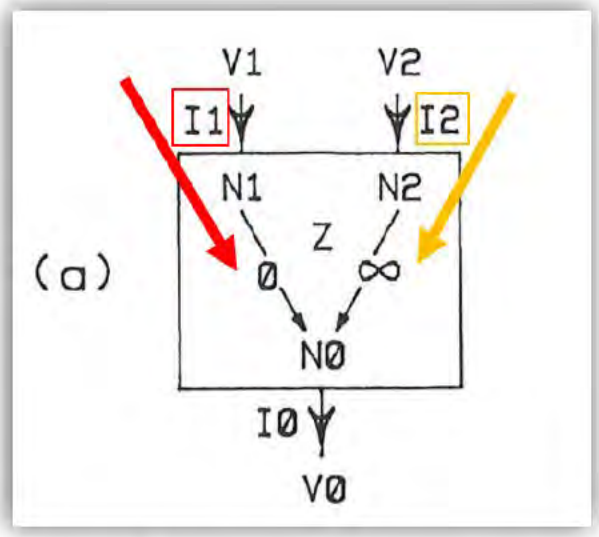
188. When connected as shown in Ishimaru, transistor 119 takes the general, three-node form set out by Barrie Gilbert and Gray for a *current mirror*. Gilbert Fig. 6.1a; Gray Fig. 4.1. Accordingly, in the side-by-side images below, Ishimaru's transistor 119 is used as a current mirror in that node Nl (of *Gilbert* Figure 6.la showing a current mirror) is the base of

[redacted]

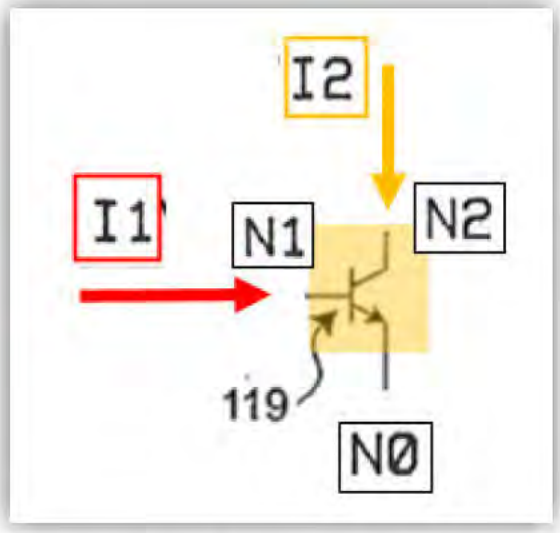
transistor 119, N2 the collector of transistor 119, and N0 the emitter of transistor 119, with the circuit replicating (and scaling) current I1 to generate output current I2. Gilbert 242, Fig. 6.1a; Gray Fig. 4.1; *see, e.g.*:

> In the simplest possible scenario, a single BJT can be used as a mirror: node N1 (of Figure 6. la) is the base, N2 the collector and NO the emitter.

Gilbert 242.

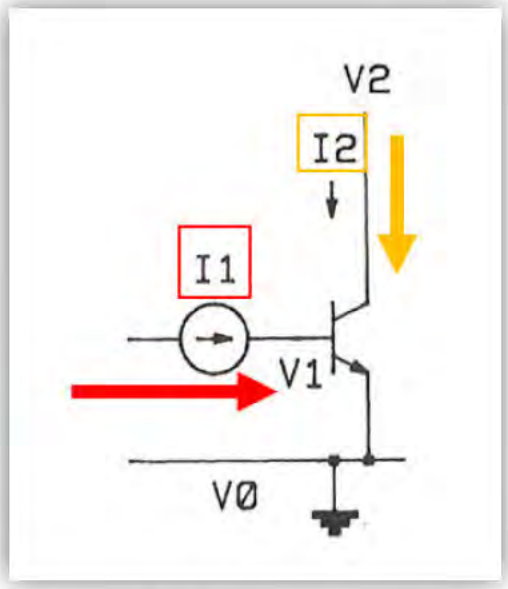


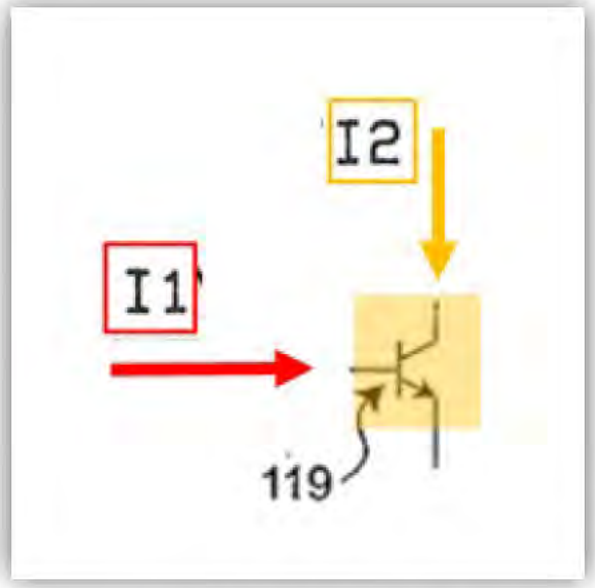
Gilbert 240, Fig. 6.1a (annotated)



Ishimaru Fig. 1 (annotated)(partial)

189. Likewise, Ishimaru's transistor 119 is connected and used in the same way as Gilbert's single-transistor current mirror of his Figure 6.2a.





Gilbert 243, Fig. 6.2a (annotated) **Ishimaru Fig. 1 (annotated) (partial).**

190. In addition to the replication discussed above, Ishimaru's current mirror is further configured to amplify the $I_{CONTROL}$, scaling it up by the amplification factor to form $I_{CORRECTION}$, namely the common-emitter current-gain, β, of the transistor 119, which quantifies the "mirror ratio (discussed below) of Ishimaru's current mirror. *See supra* §VIII.C.2, Illingworth 38; Gilbert 242-243; *see, e.g.*:

> **beta current gain factor** *Syn.* common-emitter forward-current transfer ratio; forward current gain. Symbol: β. The short-circuit current-amplification factor in a bipolar transistor with ►common-emitter connection: $\beta = \alpha I_c / \alpha I_B$ V_{CE} constant where I_C is the collector current and I_B is the base current; the collector voltage, V_{CE}, is constant. β is always greater than unity and practical values up to 500 are used.

Illingworth 38.

> In the simplest possible scenario, a single BJT can be used as a mirror: node Nl (of Figure 6. la) is the base, N2 the collector and NO the emitter.
>
> Figure 6.2a shows the biasing for an NPN device. We wish to determine the input and output resistances. It will be assumed that β is independent of current over the range of interest. If β were also independent of V_2, the output I_2 would always be simply βI_1 and the output resistance r_o would be infinite. In fact, β increases with

[redacted]

> V_2 due to base-width modulation, and in the customary BJT model would be exactly doubled when the collector bias voltage, V_{CB} (roughly, V_2), is equal to the forward Early voltage, V_{AF}.

Gilbert 242-243.

191. While Gilbert recognizes that other current mirror forms have wider flexibility at the design stage, that is not pertinent to Ishimaru. First, the single-transistor mirror is nonetheless a current mirror. The claims do not have a performance requirement. Moreover, as Gilbert describes, the single-transistor mirror has the advantage that its mirror ratio, β, is high, making it suitable for Ishimaru's circuit, which requires a high mirror ratio.

192. More specifically, the current at the collector (I_{C119}) of transistor 119 (a transistor having β_{119}) is generally related to the current at the transistor's base (I_{B119}) by the equation: $I_{C119} = \beta_{119} * I_{B119}$. Thus, the ratio of the input current I_{B119} to the output current I_{C119} is generally β_{119}. The gain through the transistor is the "mirror ratio", "M", by which Ishimaru's current mirror scales the $I_{CONTROL}$ to generate the $I_{CORRECTION}$. Gilbert 242-243; Ishimaru Fig. 1. The gain of transistor 119 can be configured to a target value by designing the voltage and current biasing of the transistor 119 (within the constraints of the circuit), such that a targeted and desired β (from within an available range, *e.g.,* of about 60 to 150 or more), can be achieved.[10] The time constant of the transient can then be tuned through the choice of components, namely C121 and R136. Ishimaru ¶¶55-56; *see, e.g.*:

> In the power amplifier of this embodiment also, the capacitance value of the capacitance element 121 of the speedup circuit 122 is adjusted so as to cancel transient variations in gain due to the temperature variations at a start of power amplification. As a result of this, deterioration of the linearity due to variations of

[10] While the single-transistor current mirror of Ishimaru does not have as widely controllable a mirror ratio as other current mirrors (a mirror ratio of, e.g., 2 is better suited for other current mirror forms), the single transistor mirror is suitable if one needs a high mirror ratio, such as can be provided by the β factor controllable by appropriately biasing the single-transistor mirror.

[redacted]

> amplification gain can be canceled so that the value of dynamic EVM (error vector magnitude) can be improved.

Ishimaru ¶55.

> In addition, the capacitance element 121 of the speedup circuit 122 may be a capacitance element whose capacitance value is changeable. In this case, changing the capacitance value of the capacitance element 121 makes it possible to adjust the time duration during which the bias fed to the amplifier transistor 103 at a start of amplification operation by the speedup circuit 122 via the bias power source section composed of the power source circuit 112 and the bias circuit 111 is kept increased.

Ishimaru ¶56.

193. Thus, transistor 119 as connected in Ishimaru is a current mirror in that it constitutes a circuit configured to mirror a current, which can be configured to achieve a target gain. Consistent with the plain meaning for "current mirror" proposed by Respondents, transistor 119 is a circuit that has electrical interconnections, including input/output and other connections that permit current to flow through the circuit. *See*:

> Plain meaning, such as "one or more circuits configured to mirror a current, which can be configured to achieve a target gain"

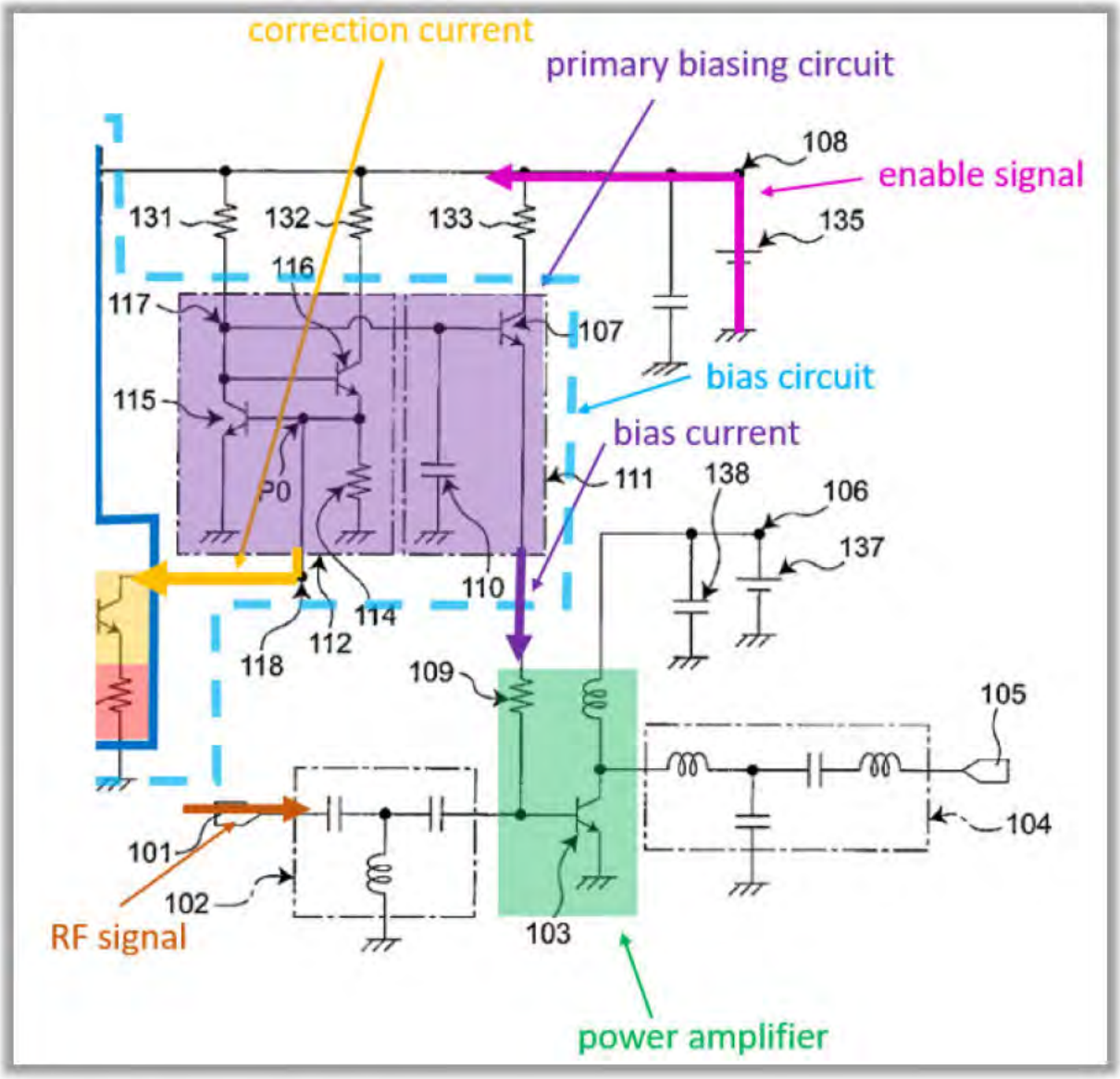
§VII.C.

194. Ishimaru thus discloses a speedup circuit 122 for correcting the gain of the PA (*a gain correction circuit*) (dark blue) that, in response to "a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier)"*(in response to activation of the power amplifier enable signal*) (pink arrow), generates a transient or time-varying current via capacitor 121 that is amplified (by transistor 120) and applied to the base of transistor 119 (*generate a control current*) (red arrow) that is replicated, *i.e.*, mirrored (and scaled up) at the collector of transistor 119 in the form of a transient or time-varying current (*mirror the control current to generate a correction current*) (gold arrow) that is pulled from node 118 to affect the generation of I_{BIAS} (*bias signal*) (purple arrow) applied to the base of amplifier transistor 103.

[redacted]

[14.2.2.2] and a primary biasing circuit configured to generate the bias signal based on the correction current and the power amplifier enable signal.

195. Ishimaru discloses this limitation. *See supra* limitation [14.2.2.1]. As shown in the portion of Figure 1 reproduced below, Ishimaru discloses a power source circuit 112 and bias circuit 111, which constitute *the primary biasing circuit* (purple) which together supply a "base bias current" (I_{BIAS}, *the bias signal*) (purple arrow) to the amplifier transistor 103. As I explain below, this I_{BIAS} is based on the control voltage (*the power amplifier enable signal*) (pink arrow) and the current drawn out of node 118 (*the correction current*) (gold arrow).



Ishimaru Fig. 1 (partial) (annotated).

196. Ishimaru discloses that "bias circuit 111 and the power source circuit 112 constitute a bias power source section." Ishimaru ¶ 46; *see, e.g.*:

> A power source circuit 112 is connected to the base terminal of the bias transistor 107 of the bias circuit 111. The bias circuit 111 and the power source circuit 112 constitute a bias power source section.

Ishimaru ¶ 46. The combination of this circuitry is a *primary biasing circuit* in that it is the main circuitry used to generate the "base bias current" that biases the operating point of the transistor

[redacted]

of the PA (green) to its intended state (e.g. *enabled*, and biased to operate at its intended operating point, suitable for amplification). *See, e.g.,* Horowitz 218, 220-228; Harrison Fig. 2.1; *see, e.g.*:

> Transistor circuits are usually designed to amplify an ac input voltage rather than dc current. In this type of arrangement, the ac is superimposed on the dc. The dc is used to establish specific quiescent emitter and collector currents. These *bias currents* should set the idling voltage (voltage before ac is applied to the circuit) at the collector at one-half of E_{CC}. Because the collector voltage, V_C, is equal to $E_{CC} - I_C R_C$, V_C should be idling at about $E_{CC}/2$.

Horowitz 218.

> Bias or idling conditions are established when there is no ac voltage at the input of the circuit, or $E_{IN} = 0$. At this time, only the dc emitter supply voltage less the base-emitter voltage is across R_C the only component in this circuit that is outside of the transistor.

Horowitz 220.

> As was true in the common-base circuit, it is also desirable here to let the voltage at the collector terminal in this circuit idle at $E_{cc}/2$ volts. To do this, the idling voltage across R_c must be equal to half of the supply voltage, or $I_C R_C = E_{CC}/2$. Because I_C is related to I_B, I_B is set by the designer of the circuit to equal the desired le divided by beta. I_B can, of course, be set by using the proper base resistor, R_B, in the circuit. Ac signal voltage is usually fed through a capacitor to the base and applied between the base and emitter to the transistor. The input voltage varies the base and hence collector current in step with the cyclic variations of the ac. A magnified version of the ac input voltage is developed across the collector resistor by the ac collector current flowing through it.

Horowitz 223.

197. More specifically, bias circuit 111 is "composed of the bias transistor 107 and a capacitance element 110" connected to the base of bias transistor 107. Ishimaru ¶ 45; *see, e.g.*:

> A bias circuit 111 composed of the bias transistor 107 and a capacitance element 110 connected to a base terminal of the bias transistor 107 has a function of increasing the base bias current in response to an increase in signal strength of the input signal, and functions to keep the amplification ratio of an output signal as well as its phase rotation after amplification constant even when the signal strength of the input signal has changed.

[redacted]

Ishimaru ¶45. Bias transistor 107's collector is connected to bias terminal 108 through a resistor 133, and the bias terminal 108 is connected to control voltage source 135 (*the power amplifier enable signal*) (pink arrow). Ishimaru ¶44; *see, e.g.*:

> The bias transistor 107 has its collector connected to a bias terminal 108 via a resistance element 133. The bias terminal 108 is connected to a control voltage source 135.

Ishimaru ¶44. The emitter of bias transistor 107 is connected to a base terminal of the amplifier transistor 103 via resistance element 109 and "supplies a base bias current to the base of amplification transistor 103." Ishimaru ¶43; *see, e.g.*:

> Also, a bias transistor 107 as a second transistor is a transistor that supplies a base bias current to a base terminal of the amplifier transistor 103. An emitter of the bias transistor 107 is connected to a base terminal of the amplifier transistor 103 via a resistance element 109. The resistance element 109 is a ballast (stabilization) resistor which is inserted in a base bias channel to prevent thermal runaway of the amplifier transistor 103.

Ishimaru ¶43. Thus, the "base bias current" provided by bias transistor 107 to the amplifier transistor 103 is *a bias signal*.

198. Bias transistor 107 in circuit 111 operates in conjunction with power source circuit 112 to generate I_{BIAS} applied to the amplifier transistor 103 and thus, circuit 111 and 112, collectively are *a primary biasing circuit* (purple).

199. More specifically, as shown in the portion of the annotated Figure 1 above, node 117 of circuit 112 is connected to the base terminal of the bias transistor 107 and, thus, controls the bias point of transistor 107 and, consequently, the transistor 107's collector current. Ishimaru ¶¶46, 48; *see, e.g.*:

> A power source circuit 112 is connected to the base terminal of the bias transistor 107 of the bias circuit 111. The bias circuit 111 and the power source circuit 112 constitute a bias power source section.

[redacted]

Ishimaru ¶46. Node P0 of power source circuit 112 (*i.e.*, the base of transistor 115 and emitter of transistor 116) is connected to output terminal 118 of speedup circuit 122. Ishimaru ¶¶48-49; *see, e.g.*:

> In this embodiment, as shown in FIG. 1, the power source circuit 112 has a third transistor 115, a fourth transistor 116, and a resistance element 114. The third transistor 115 has its collector connected to the base of the bias transistor 107 and its emitter connected to the ground. Also, a base of the third transistor 115 is connected to an emitter of the fourth transistor 116. The collector of the third transistor 115 is connected to the bias terminal 108 via a resistance element 131. Meanwhile, the fourth transistor 116 has its emitter connected to the ground via the resistance element 114 and its collector connected to the bias terminal 108 via a resistance element 132.

Ishimaru ¶48.

200. Ishimaru explains that, at a rise time of the control voltage from the control voltage source 135, "a current transiently (temporarily) from the output terminal 118" flows into the speedup circuit 122. Ishimaru ¶52; *see, e.g.*:

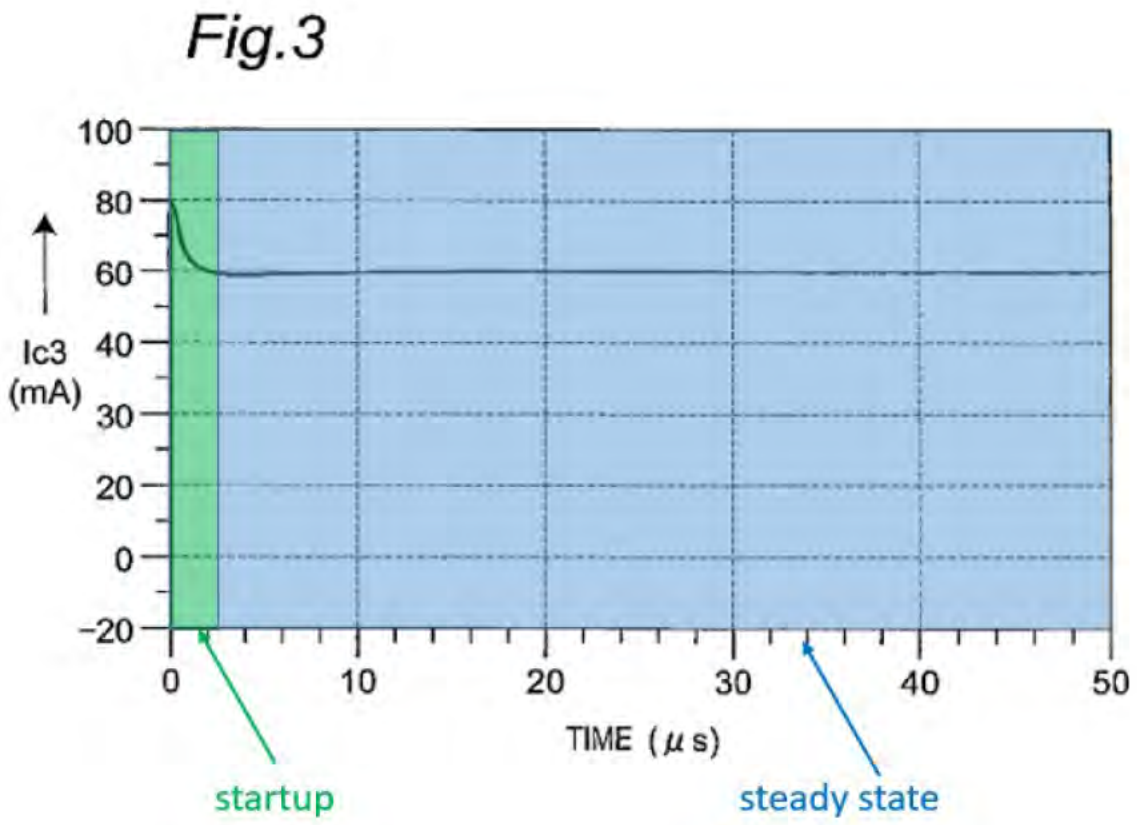
> In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).

Ishimaru ¶52.

201. As explained for limitation [14.2.2.1] above, this current is $I_{CORRECTION}$. The transient rise in $I_{CORRECTION}$ causes the voltage at output terminal 118 to lower, which raises the voltage at the collector of transistor 115 (node 117), which controls the bias transistor 107, and

[redacted]

this causes "the current fed to the amplifier transistor by the bias transistor 107" (*the bias signal*) to transiently increase. Ishimaru ¶52. Figure 3, which shows the transient response of the collector current of the amplifier transistor 103, illustrates how the transient rise in $I_{CORRECTION}$ causes the collector current of PA transistor 103 to temporarily increase during startup. Ishimaru ¶54.



Ishimaru Fig. 3 (annotated).

202. This transient increase in the collector current of amplifier transistor 103 is due to a transient increase in the I_{BIAS} because the collector current amplifies I_{BIAS} via PA transistor 103's amplification factor β. Further, Ishimaru explicitly explains that the collector current 103 (also called "operating current Ic3") "comes to a steady state in about ¼ of the time of transient

[redacted]

response of the comparative example of Fig. 2," which is the transient response without speedup circuit 122. Ishimaru ¶¶53-54; *see, e.g.*:

> Next, FIG. 3 shows an example (simulation result) of transient response of the operating current (collector current Ic3) of the amplifier transistor 103 in the power amplifier of this embodiment. In this embodiment, the current to be fed from the bias transistor 107 to the amplifier transistor 103 is forcedly increased at turn-on of the amplifier, with the result that the value of the operating current Ic3 comes to a steady state in about 1/4 the time of transient response of the comparative example of FIG. 2. Thus, occurrence of distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed, so that the linearity of the circuit in burst operation is improved. That is, gain variations due to collector current variations of the power amplifier using a bipolar transistor can be compensated.

Ishimaru ¶54.

203. Accordingly, Ishimaru discloses a bias power source section with a bias circuit 111 and power source section 112 (together, *a primary biasing circuit*) that provides I_{BIAS} (*a bias signal*). At turn-on (*i.e.,* enablement) of power amplification, this I_{BIAS} is based on the current pulled from terminal 118 and the control voltage from the control voltage source 135 (*configured to generate the bias signal based on the correction current and the power amplifier enable signal*).

204. Therefore, it is my opinion that Claim 14 is rendered obvious by Ishimaru alone.

205. It also is my opinion that Claim 14 is rendered obvious by Ishimaru in view of Ichitsubo.

206. It also is my opinion that Claim 14 is rendered obvious by Ishimaru in view of Johnson.

Claim 15

[15] The packaged module of claim 14 wherein the primary bias circuit includes a first transistor, the correction current configured to change a current flowing through the first transistor.

[redacted]

207. Ishimaru discloses this limitation. As shown in the annotated excerpt of Figure 1 below, Ishimaru discloses that bias power source section (*the primary bias circuit*) (purple) includes transistor 115, which is *a first transistor* (red). Ishimaru ¶ 48; *see, e.g.*:

> In this embodiment, as shown in FIG. 1, the power source circuit 112 has a third transistor 115, a fourth transistor 116, and a resistance element 114. The third transistor 115 has its collector connected to the base of the bias transistor 107 and its emitter connected to the ground. Also, a base of the third transistor 115 is connected to an emitter of the fourth transistor 116. The collector of the third transistor 115 is connected to the bias terminal 108 via a resistance element 131. Meanwhile, the fourth transistor 116 has its emitter connected to the ground via the resistance element 114 and its collector connected to the bias terminal 108 via a resistance element 132.

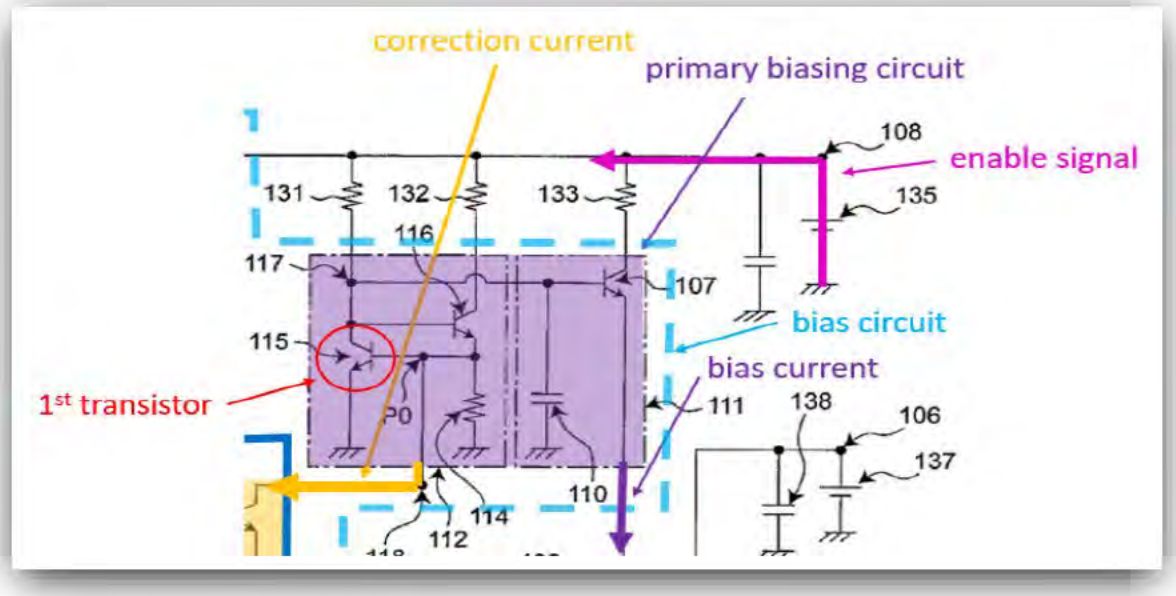
Ishimaru ¶48. As described with respect to limitation [14.2.2.2] *supra*, the base of transistor 115 is connected to connecting point P0, through which $I_{CORRECTION}$ (gold) flows into speedup circuit 122. Ishimaru ¶¶49, 52. When the amplifier turns on in response to the control voltage from the control voltage source 135, the $I_{CORRECTION}$ temporarily increases, which lowers the voltage at the base of transistor 115. Ishimaru ¶52; *see, e.g.*:

> In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).

Ishimaru ¶52.

[redacted]

208. A POSITA understands that this change in the voltage at the base of transistor 115 changes the bias point of transistor 115 and, thus, changes the current flowing through (*i.e.*, from the collector to the emitter) transistor 115.



Ishimaru Fig. 1 (partial) (annotated).

209. Thus, Ishimaru discloses that the bias power source section (*the primary bias circuit*) (purple) has a transistor 115 (*includes a first transistor*) (red) where a change in the current flowing into speedup circuit 112 changes the current flowing through transistor 115 (*the correction current configured to change a current flowing through the first transistor*).

210. Therefore, it is my opinion that Claim 15 is rendered obvious by Ishimaru alone.

211. It also is my opinion that Claim 15 is rendered obvious by Ishimaru in view of Ichitsubo.

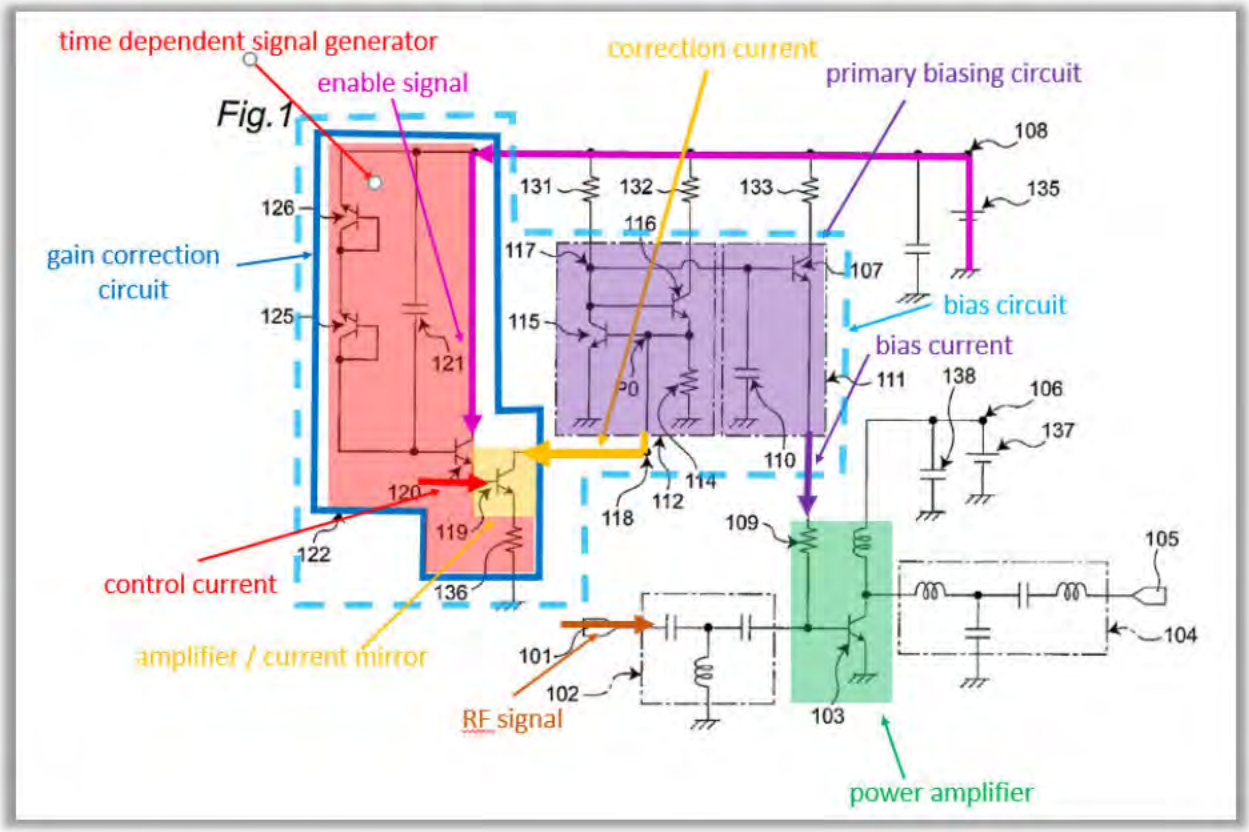
212. It also is my opinion that Claim 15 is rendered obvious by Ishimaru in view of Johnson.

Claim 17

[redacted]

[17] The packaged module of claim 14 wherein the gain correction circuit includes a current mirror configured to generate the correction current by mirroring the control current, the current mirror configured to receive the power amplifier enable signal.

213. Ishimaru discloses this limitation for the same reason as discussed with respect to limitation [14.2.2.1] *supra*. Specifically, the speedup circuit (*gain correction circuit*) (dark blue) includes transistor 119 (*current mirror*) (gold) configured to generate $I_{CORRECTION}$ (gold arrow) by mirroring $I_{CONTROL}$ (red arrow), where the current mirror is configured to receive the *power amplifier enable signal* (purple arrow) as illustrated in the annotations of Fig. 1, below.



Ishimaru Fig. 1 (annotated).

214. Therefore, it is my opinion that Claim 15 is rendered obvious by Ishimaru alone.

[redacted]

215. It also is my opinion that Claim 15 is rendered obvious by Ishimaru in view of Ichitsubo.

216. It also is my opinion that Claim 15 is rendered obvious by Ishimaru in view of Johnson.

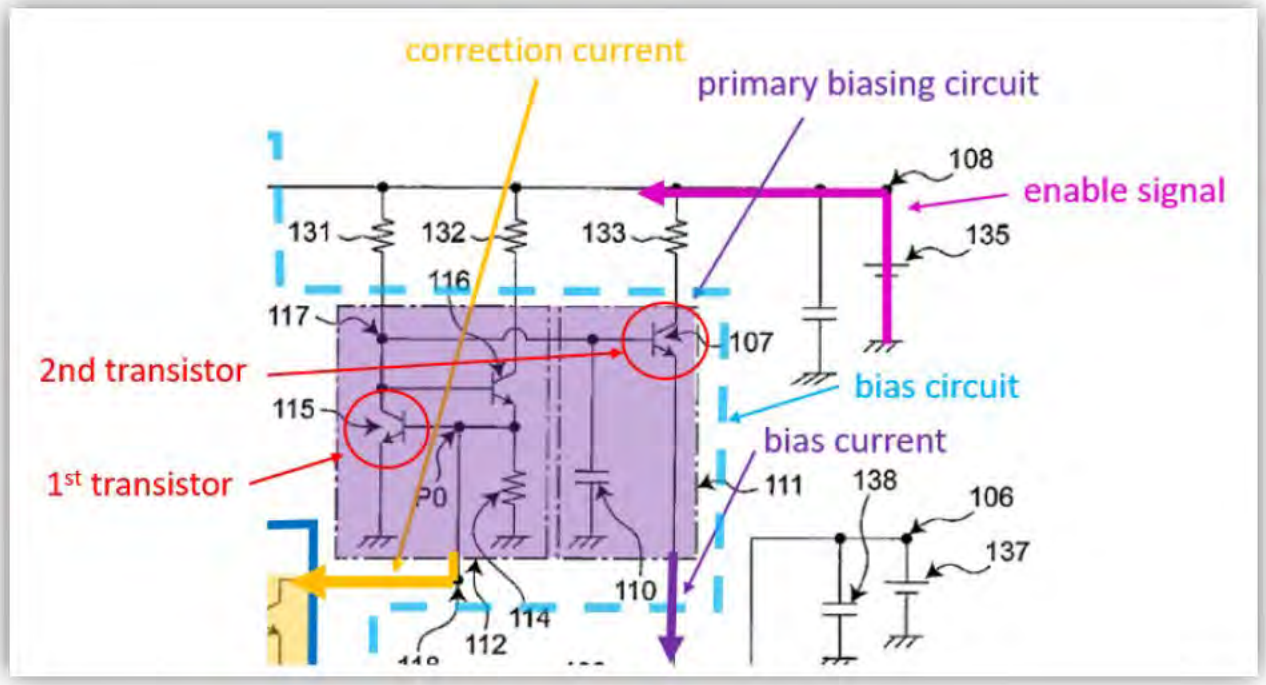
Claim 20

[20] The packaged module of claim 15 wherein the primary bias circuit further includes a second transistor electrically coupled to the first transistor and configured to provide the bias signal to the power amplifier.

217. Ishimaru discloses this limitation. As shown in the portion of Annotated Fig. 1 below, Ishimaru discloses that bias power source section (*the primary bias circuit*) (purple) includes a transistor 115 (*the first transistor*) (red circle) and transistor 107 (*a second transistor*) (red circle). Transistor 115 "has its collector connected to the base" of "transistor 107," and transistor 107 "supplies a base bias current (purple) to a base terminal of the amplifier transistor 103." Ishimaru ¶¶48, 43; *see, e.g.*:

> Also, a bias transistor 107 as a second transistor is a transistor that supplies a base bias current to a base terminal of the amplifier transistor 103. An emitter of the bias transistor 107 is connected to a base terminal of the amplifier transistor 103 via a resistance element 109. The resistance element 109 is a ballast (stabilization) resistor which is inserted in a base bias channel to prevent thermal runaway of the amplifier transistor 103.

Ishimaru ¶43.



Ishimaru Fig. 1 (partial) (annotated).

218. Ishimaru thus discloses a bias power source (*the primary bias circuit*) including transistor 107 (*a second transistor*) (red circle) with a base connected to the collector of transistor 115 (*electrically coupled to the first transistor*) (red circle) where transistor 107 "supplies a base bias current" (*is configured to provide the bias signal*) (purple) "to a base terminal of the amplifier transistor 103" (*to the power amplifier*).

219. Therefore, it is my opinion that Claim 20 is rendered obvious by Ishimaru alone.

220. It is also my opinion that Claim 20 is rendered obvious by Ishimaru in view of Ichitsubo.

221. It is also my opinion that Claim 20 is rendered obvious by Ishimaru in view of Johnson.

[redacted]

2. Claims 14, 15, 17, and 20 are Obvious Over Ishimaru in View of Harrison, or, alternatively, Ishimaru in View of Ichitsubo or Johnson and Further in View of Harrison

222. My opinions in this Section are submitted to address Complainant's claim construction of *current mirror* which adds the limitations that the *current mirror* must have "at least two transistors with their base or gate terminals tied together." While it is my opinion that the State of the Art (§VIII.C.2) demonstrates that a POSITA understood that a *current mirror* is not limited to any specific number or configuration of transistors, Harrison discloses a current mirror even under Complainant's claim construction.

223. For this Section, I incorporate my opinions in Section §IX.D.1 above, where I explain how Ishimaru, and, alternatively, how Ishimaru in view of Ichitsubo or Johnson disclose each limitation of the Asserted Claims of the '563 Patent. However, to the extent it is argued that Ishimaru does not expressly disclose or render obvious a *current mirror,* Harrison discloses this limitation.

Claim 14

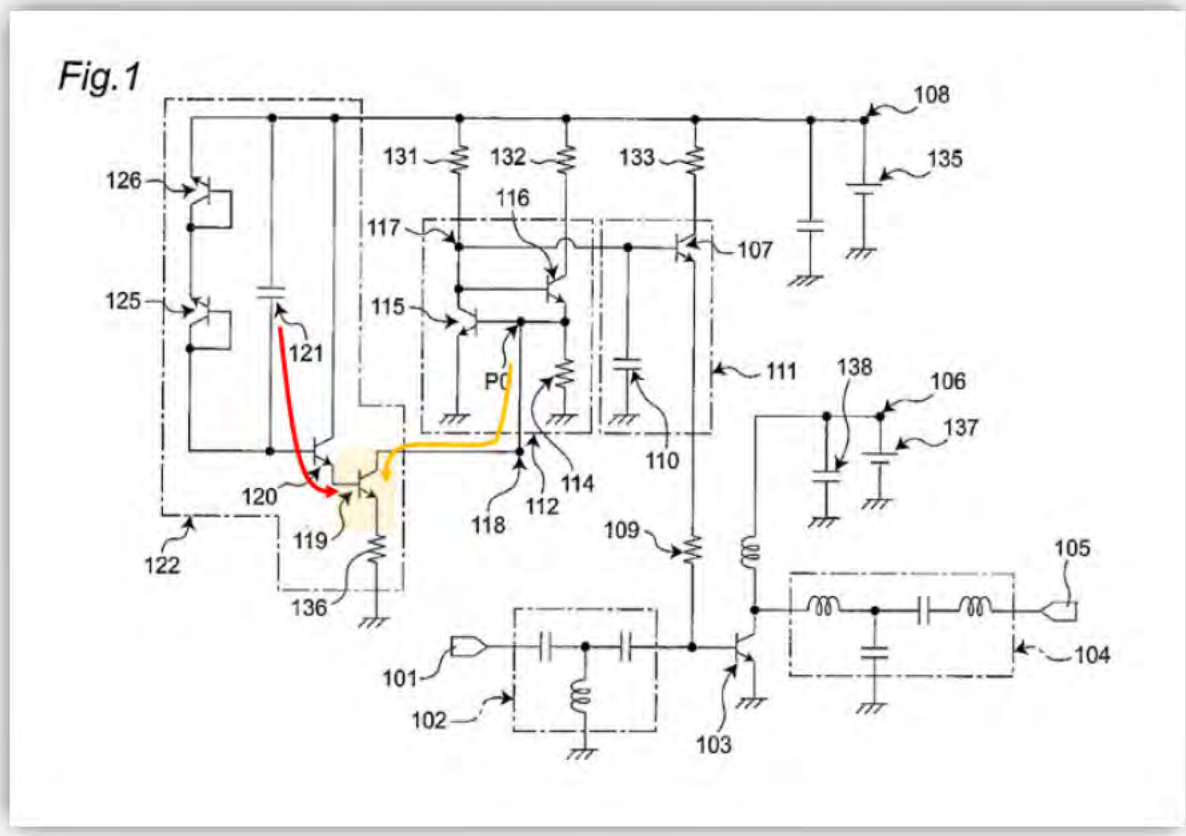
224. For all the limitations in Claim 14, I incorporate my opinions in §IX.D.1 above, where I explain how Ishimaru and, alternatively, Ishimaru in view of Ichitsubo or Johnson disclose the limitations. I further address limitation [14.2.2.1] below in view of Harrison's disclosure of a *current mirror*.

[14.2.2.1] a gain correction circuit configured to generate a control current in response to activation of the power amplifier enable signal and to mirror the control current to generate a correction current

225. As discussed in §IX.D.1, Ishimaru discloses a speedup circuit 122 that responds at "a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier)" to generate a time-varying current via capacitor 121 that is amplified by and 119 (*current*

[redacted]

amplifier). §V.D.1. Furthermore, as illustrated in the annotated Figure 1, below, a POSITA recognizes that Ishimaru uses the amplified version of the current (red arrow) as a current sink to pull a specifically shaped $I_{CORRECTION}$ (gold arrow) out of the primary biasing circuit.



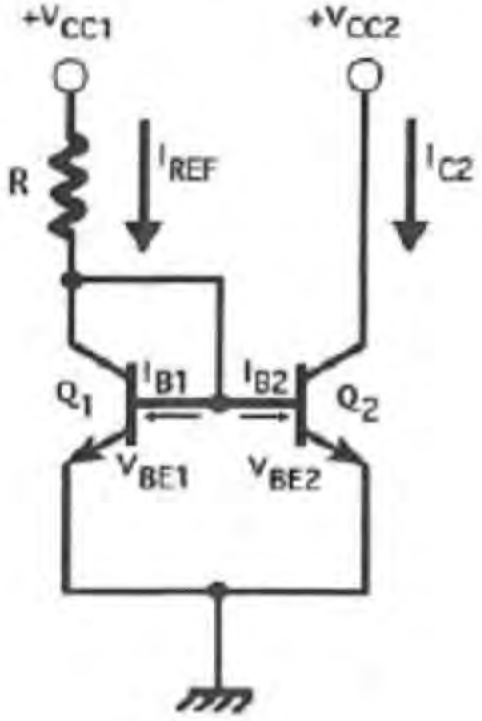
Ishimaru Fig. 1 (annotated).

226. A POSITA readily recognizes the coupling of the left and right sides of Ishimaru's circuit as involving a current source generated on the left side that is replicated as a current sink on the right side, which is a coupling that takes the general form of a *current mirror* (*i.e.* transistor 119 as discussed in §IX.B.1 above).

227. A POSITA further recognizes that the current source / current sink coupling of Ishimaru would be well suited for, and ready for improvement by, the use of additional current

mirror structures to couple the two sides of Ishimaru's circuit to achieve the well-known benefits of such current mirrors.

228. In that regard, Harrison teaches a well-known "basic" current mirror using NPN transistors that operates as a "mirror-sink," as shown in the excerpt of Figure 4.18 below:



Harrison 71; Fig. 4.18.

229. As can be seen in Figure 4.18 above, this current mirror also satisfies Complainant's proposed construction of current mirror in that it has at least two transistors (Q1 and Q2) with their base terminals tied together. §VII.C; Harrison 71, Fig. 4.18; *see, e.g.*:

> In both current mirror circuits, Q_1's base and collector are shorted together, while the base and emitter act as a diode. The series resistor, R_1, provides a fixed voltage and current to Q_1's collector, as well as base current for Q_1 and Q_2. In the NPN circuit, because Q_1's collector and base are shorted, and its emitter is grounded, this clamps the V_{BE} at approximately 0.65 volt above ground.

[redacted]

Harrison 71. Furthermore, the basic current mirror above is a circuit configured to mirror I_{REF} to I_{C2}, and is configurable to achieve a target gain that can be finely tuned by adjusting the ratio of the transistor sizes. Harrison 95 (describing "current scaling" by setting the ratio of the emitter area); *see also* Gilbert 280; Gray 254, 257; Grebene 172; *see, e.g.*:

> With the exception of the Widlar and the Wyatt current sources, up until now we have looked at current sources that generate input-to-output currents in a 1:1 ratio, but it is often necessary to generate integer multiples or fractions on an initial current. For the IC designer this is accomplished in the design by creating transistors with multiple emitters, or with bulk emitter area ratioed in either greater or lesser amounts. In this way a current can be made, say, 10 times or one-tenth of the initial input current. It is sometimes depicted in a manufacturer's circuit schematic as a number written next to the particular emitter (see Figure 4.22D). It is sometimes shown, for example, as 10E or 10A.
>
> For the board-level designer, generating multiples or fractions of an initial current can be accomplished in different ways. One way to do this is by paralleling individual transistors as shown in the following circuits, in what is known as *current scaling*.

Harrison 95.

> There is no particular difficulty in achieving high mirror ratios. In many cases, simple emitter area ratios will suffice, supported by current gain if necessary (as in the EFA mirror, which is not limited to the use of a single transistor for current boosting). In practical monolithic designs, emitter area ratios of up to 100:1 are not hard to achieve.

Gilbert 280.

> Since the saturation current of a bipolar transistor is proportional to its emitter area, the first term in (4.6) shows that the gain of the current mirror can be larger or smaller than unity because the emitter areas can be ratioed. If the desired current-mirror gain is a rational number, M/N, the area ratio is usually set by connecting M identical devices called *units* in parallel to form $Q2$ and N units in parallel to form $Q1$ to minimize mismatch arising from lithographic effects in forming the emitter regions.

Gray 254.

> Equation 4.17 shows that the gain of the current mirror can be larger or smaller than unity because the transistor sizes can be ratioed. To ratio the transistor sizes, either the widths or the lengths can be made unequal in principle. In practice, however, the lengths of $M1$ and $M2$ are rarely made unequal.

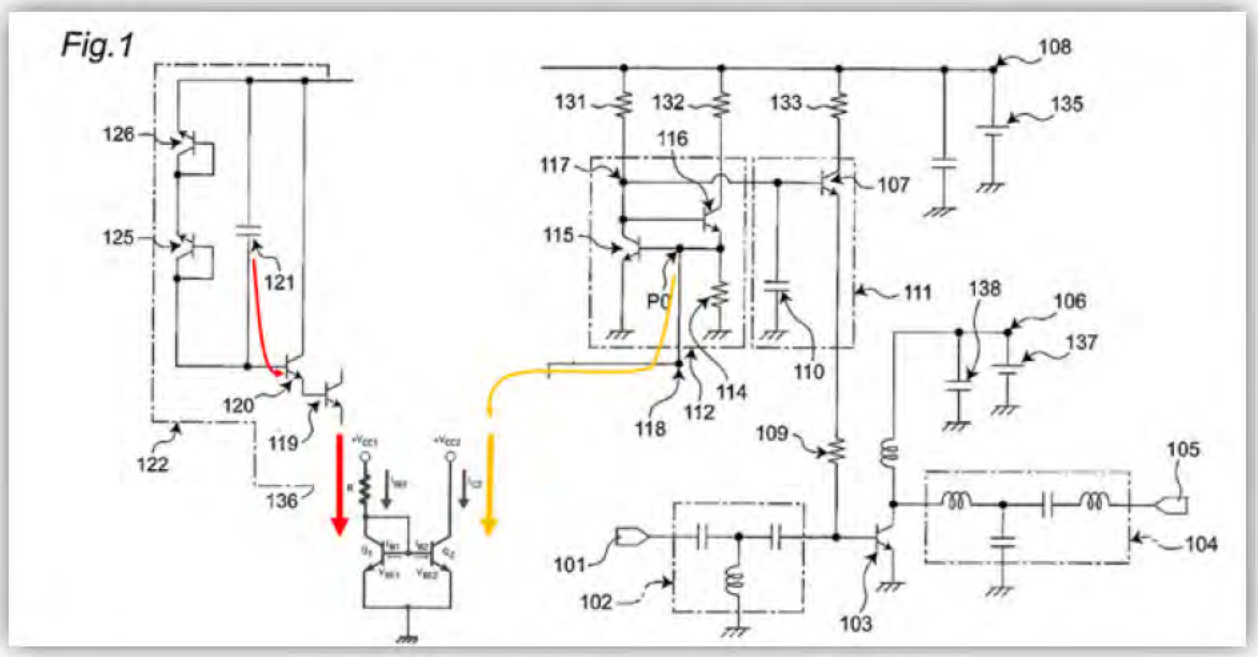
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Gray 257.

> The basic current-voltage equations (4.1) through (4.8) hold over a broad temperature range (typically -60 to + 150°C) and over six orders of magnitude of current. Thus, the basic current mirror circuit of Figure 4.1 provides a means of obtaining a current reference level, independent of implicit device parameters, which can be "scaled" by proper choice of the emitter areas of the two transistors. Assuming typical V_{BE} mismatch of $< \pm 1$ mV and β in the range of 100-200, the typical output current /**2** would be within ±5% of I_{ref} over a wide range of temperature and current levels.

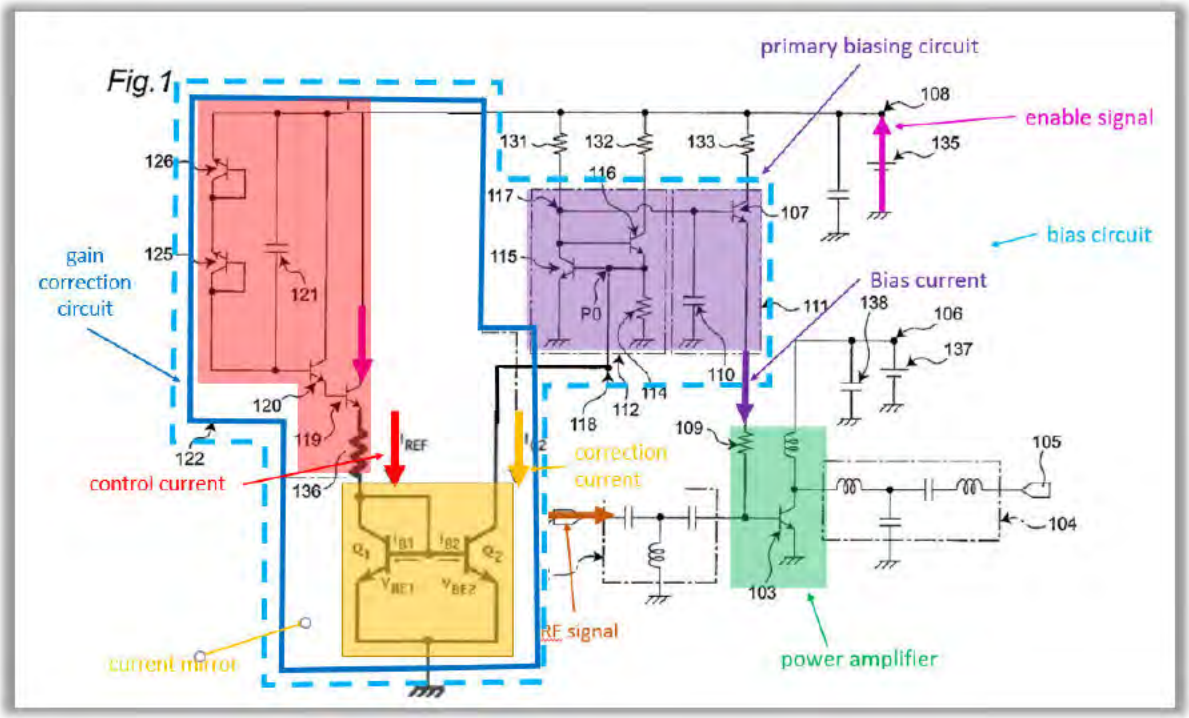
Grebene 172.

230. A POSITA would recognize modifying the speedup circuit as taught by Ishimaru to add a basic current mirror as taught by Harrison would be beneficial because it provides flexibility in allowing a broader range of voltages and a broader range of amplification due to the ability to achieve the desired current amplification by changing the ratios of transistor sizes in the basic current mirror. §VIII.C.2. In my opinion, a POSITA would easily and advantageously apply Harrison's teaching to Ishimaru as illustrated below in the following annotated figures, derived from Ishimaru's Figure 1 and Harrison's Figure 4.18:



[redacted]

231. As illustrated above, a basic current mirror such as taught by Harrison can be advantageously added to Ishimaru's speedup circuit by interposing the basic current mirror at the emitter of transistor 119, and then connecting node P0/118 to the collector of current mirror transistor Q2. The collector of transistor 119 is then connected to the control voltage source (*the enable signal*).



232. As shown in the above annotations, Ishimaru's speedup circuit modified with Harrison's basic current mirror is a gain correction circuit (dark blue) that responds at "a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier)" in response to activation of the PA enable signal (pink) to generate a transient current signal via capacitor 121 that is amplified by transistors 120 and 119 and passed through resistor 136 to generate a control current (red arrow). Ishimaru modified with Harrison then takes this amplified time varying current signal (red arrow) and mirrors it using the basic *current mirror* to generate a time-varying $I_{CORRECTION}$ (gold arrow) that is pulled from node 118.

[redacted]

233. It is my opinion that a POSITA would have been highly motivated to combine Ishimaru's teaching of a bias circuit for a PA with Harrison's disclosure of a basic current mirror and have a reasonable expectation of success for at least the following reasons.

234. Harrison discloses a "basic" current mirror. Harrison 71. Current mirrors were well-known in the art and were considered "a familiar icon of modern analog design." Gilbert 239. Indeed, current mirrors were "widely used in analog integrated circuits" "as biasing elements" and were "particularly useful building blocks for analog circuit design." Gray 251; Grebene 170*; see, e.g.*:

> Current mirrors made by using active devices have come to be widely used in analog integrated circuits both as biasing elements and as load devices for amplifier stages. The use of current mirrors in biasing can result in superior insensitivity of circuit performance to variations in power supply and temperature. Current mirrors are frequently more economical than resistors in terms of the die area required to provide bias current of a certain value, particularly when the required value of bias current is small.

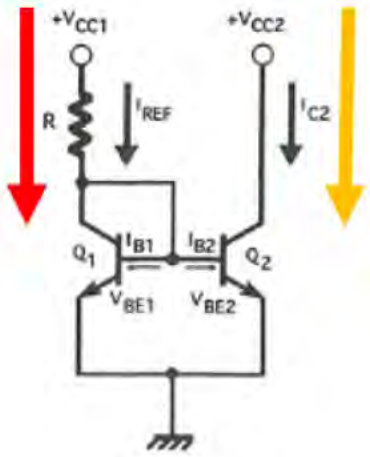
Gray 251.

> In a constant-current stage, the reference current in one branch of the circuit is accurately reproduced or reflected in a second branch, relatively independent of the absolute values of the device parameters. Because of this property, these subcircuits are also known as *current mirror* circuits. Such circuit configurations are particularly useful building blocks for analog circuit design, since they provide a means of establishing the de bias levels within the circuit, within the accuracy of the matching or tracking properties of the monolithic components.

Grebene 170.

235. One of these advantages was that current mirrors take a reference current in one branch of a circuit and accurately reproduce or reflect that current in a second branch of that circuit, and can do so "relatively independent of the absolute values of the device parameters." *Id.*; Grebene 171. Thus, current mirrors were useful in coupling circuits together such that an input current could advantageously be provided into one branch of a circuit and the current

mirror would then replicate (or *mirror*) that current such that the current mirror would pull a mirrored version of that current out of the second branch of the circuit. Harrison illustrates this configuration (called a current sink), where the input branch is annotated in red and the output branch is annotated in yellow. Harrison 71.



Basic NPN Current sink

Basic BJT current mirrors.

Harrison (Fig. 4.18) (annotated).

236. Further, current mirrors were known to be useful in providing desired current scaling when mirroring a current (called **current mirror gain**) by changing the ratios of transistor sizes. Harrison 95 (describing "current scaling" by setting the ratio of the emitter area)*; see, e.g.*:

> With the exception of the Widlar and the Wyatt current sources, up until now we have looked at current sources that generate input-to-output currents in a 1:1 ratio, but it is often necessary to generate integer multiples or fractions on an initial current. For the IC designer this is accomplished in the design by creating transistors with multiple emitters, or with bulk emitter area ratioed in either greater or lesser amounts. In this way a current can be made, say, 10 times or one-tenth of the initial input current. It is sometimes depicted in a manufacturer's circuit schematic as a number written next to the particular emitter (see Figure 4.22D). It is sometimes shown, for example, as 10E or 10A.

[redacted]

> For the board-level designer, generating multiples or fractions of an initial current can be accomplished in different ways. One way to do this is by paralleling individual transistors as shown in the following circuits, in what is known as *current scaling*.

Harrison 95. In the case of bipolar junction transistors, this would be done by changing the relative sizes of the emitters of the current mirror transistors. Gray 25. Scaling transistor sizes in current mirrors to achieve granular, targeted levels of scaling that could (be fine-tuned was well understood as of the priority date of the Asserted Patents and described in multiple textbooks. Gray 251-257; Grebene 172; Gilbert 252, 280*; see, e.g.*:

> Since the saturation current of a bipolar transistor is proportional to its emitter area, the first term in (4.6) shows that the gain of the current mirror can be larger or smaller than unity because the emitter areas can be ratioed. If the desired current-mirror gain is a rational number, *M/N*, the area ratio is usually set by connecting *M* identical devices called *units* in parallel to form *Q*2 and *N* units in parallel to form *Q*1 to minimize mismatch arising from lithographic effects in forming the emitter regions.

Gray 254.

> Equation 4.17 shows that the gain of the current mirror can be larger or smaller than unity because the transistor sizes can be ratioed. To ratio the transistor sizes, either the widths or the lengths can be made unequal in principle. In practice, however, the lengths of *M*1 and *M*2 are rarely made unequal.

Gray 257.

> The basic current-voltage equations (4.1) through (4.8) hold over a broad temperature range (typically -60 to + 150°C) and over six orders of magnitude of current. Thus, the basic current mirror circuit of Figure 4.1 provides a means of obtaining a current reference level, independent of implicit device parameters, which can be "scaled" by proper choice of the emitter areas of the two transistors. Assuming typical V_{BE} mismatch of < ± 1 mV and β in the range of 100-200, the typical output current /**2** would be within ±5% of I_{ref} over a wide range of temperature and current levels.

Grebene 172.

> There is no particular difficulty in achieving high mirror ratios. In many cases, simple emitter area ratios will suffice, supported by current gain if necessary (as in the EFA mirror, which is not limited to the use of a single transistor for current

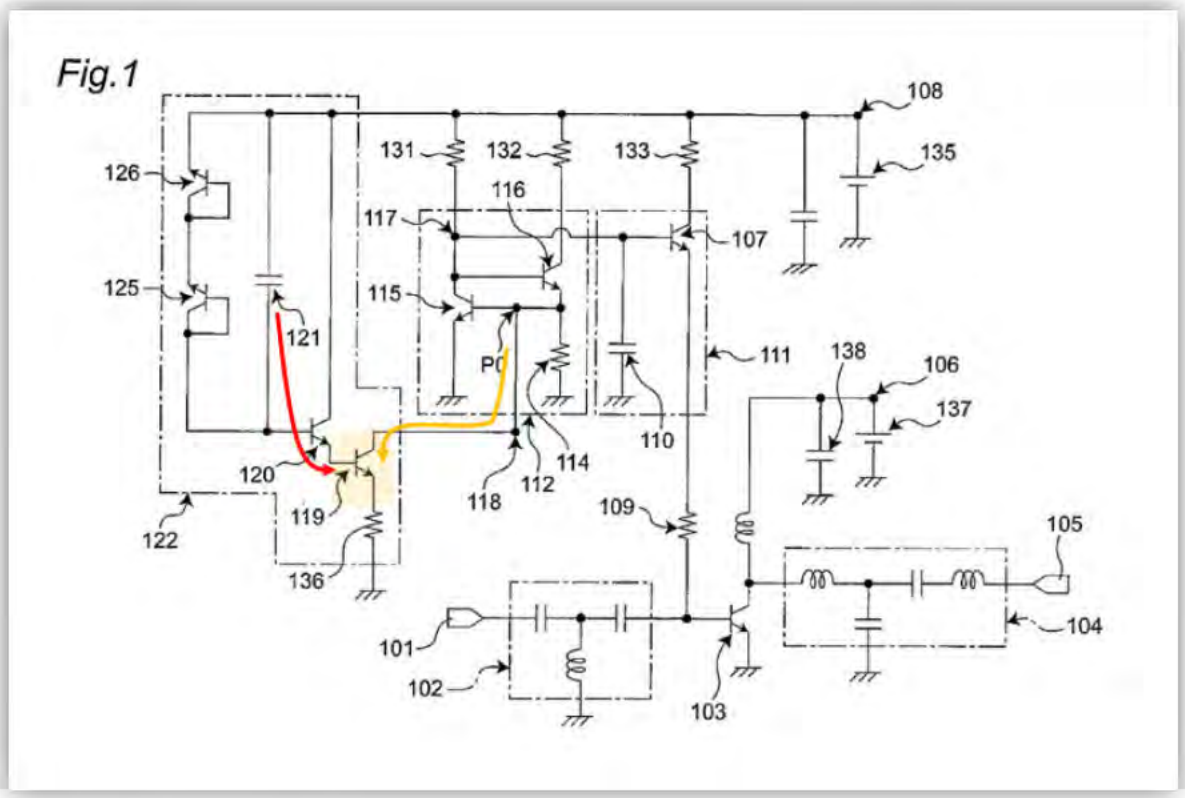
[redacted]

> boosting). In practical monolithic designs, emitter area ratios of up to 100:1 are not hard to achieve.

Gilbert 280.

237. In addition, a POSITA understood that Harrison's two-transistor current mirror would advantageously provide better isolation between the left side and the right side of Ishimaru's circuit. First, because there are separate emitter currents and paths in the two-transistor mirror, there is a degree of separation between the left and right sides of the circuit. Second, it avoids the issue that using a single transistor like Ishimaru's 119 as the current mirror has coupling (parasitic) between its base and collector due to standard parasitic capacitance. This coupling across 119 can create unwanted coupling across the transistor, such that noise on one side of the circuit can pass to the other side. Adding Harrison's two-transistor current mirror does not have this limitation, providing better isolation between the input and output current signals than Ishimaru provides.

238. A POSITA would thus have been motivated to modify the teachings of Ishimaru to add a basic current mirror as taught by Harrison because a POSITA understood that Ishimaru's circuit is designed to amplify the current that flows through capacitor 121 (annotated in red below) to generate the current sink pulled from node 118 (annotated in yellow). Ishimaru ¶¶50-52, Fig. 1.



Ishimaru Fig. 1 (annotated).

239. A POSITA recognized that Ishimaru used a current source (red) from circuit 122 to generate a current sink (yellow) from 112, coupling the two circuits using the current mirroring provided by transistor 119. A POSITA readily understood that this coupling could be improved by use of the basic current mirror of Harrison because of multiple advantages of providing an additional stage of fine tuning the current amplification. The additional stage of fine tuning would give the designer an additional degree of freedom in designing the circuit, would provide better isolation between the two sides of the circuit, and allow fine tuning in a final amplification stage that had higher configurability of its mirror ratio, M, in scaling the mirrored current. *See also* §VIII.C.2 (discussing two-transistor mirrors).

[redacted]

240. Adding a basic current mirror similar to that taught by Harrison allows for an additional stage of amplification that can be finely tuned with granular scaling of the current by adjusting the emitter area of the current mirror transistors, as discussed above. Being able to scale currents in this manner would be useful for a circuit designer wanting to establish a speedup control circuit that could advantageously be reused and adapted for different PA applications and product lines. That is because a POSITA understood that different PAs have different startup and steady state operating qualities, and that the gain variation in Ishimaru's Figure 2 is specific to a given PA in a given layout, in a specific operating point and use case. The corresponding corrective transient current thus has a specific amplitude and duration that is suitable for the application at issue.

241. For example, using different PA circuit layouts (*i.e.* where components are dimensionally closer or farther away from each other), different PA packaging, or different PA integrated circuits using a different semiconductor manufacturing process (*e.g.*, Gallium Arsenide ("GaAs") Heterojunction Bipolar Transistors ("HBTs") (together "GaAs HBTs"), or Silicon Germanium Bipolar CMOS HBTs ("SiGe BiCMOS HBTs")), will result in different thermal behaviors and startup effects, and so the amount of correction required will vary. Ishimaru itself recognizes that temperature effects depend on the layout of the PA and the amount of correction required varies across applications. Ishimaru ¶23 ("[T]urn-on behavior of the control voltage source in the amplifier depends on the layout of the amplifier, particularly on the placement of transistors[.]"), ¶3 ("In some communication systems, slight changes of amplification gain as small as 0.2 to 0.3 dB may matter."), ¶4 ("there are some cases in which variations in amplification ratio or phase on the order of several tens to several hundreds of μs

[redacted]

caused by relatively slow temperature increases due to heat generation as an example do matter."); *see, e.g.*:

> That is, heat generation of transistors becomes larger in a transistor for signal amplification involving larger current consumption (first transistor), and smaller in a transistor for bias Supply (second transistor). Then, in stages before the temperature's reach to the equilibrium, the temperature is higher at around the signal-amplification transistor and lower increasingly with increasing distance from the signal-amplification transistor, where these temperature differences cause the current value to vary, forming a cause of distortion of the modulated-wave signal. Therefore, turn-on behavior of the control voltage source in the amplifier depends on the layout of the amplifier, particularly on the placement of transistors, and amplifiers of the same layout result in the same characteristics as to turn-on and -off transient variations of the amplifiers.

Ishimaru ¶23.

> It should be noted here that the linear amplification mentioned above means that even with input signal power changed, the output signal power is amplified at a constant ratio for output while the phase keeps unchanged. In some communication systems, slight changes of amplification gain as small as 0.2 to 0.3 dB may matter

Ishimaru ¶3.

> As another aspect of the linear amplification, there are some cases in which variations in amplification ratio or phase on the order of several tens to several hundreds of us caused by relatively slow temperature increases due to heat generation as an example do matter. As a circuit for correcting effects of such heat generation by the power amplifier's own, there has been shown, in U.S. Pat. No. 4.924, 194 (see FIG. 1), a circuit in which heat generation of an amplifier transistor is detected by a temperature sensing element (PIN diode) thermally coupled to the amplifier transistor and the detection result is reflected on a bias voltage of the amplifier transistor

Ishimaru ¶4.

242. Thus, Ishimaru provides express motivation for a POSITA to add a current mirror of similar design to Harrison's for its intended purpose in order to provide flexibility in scaling Ishimaru's current, including allowing a designer to tune the operation of Ishimaru's corrective current transient in Figure 3 to a higher peak (such as for a PA having a larger gain variation). A POSITA would have recognized that Harrison's two-transistor current mirror would

[redacted]

advantageously provide an extra degree of freedom in tuning Ishimaru's circuit to compensate for the gain problems of a given PA.

243. Modifying the teachings of Ishimaru with the basic current mirror taught by Harrison would involve no more than combining prior art elements (Ishimaru and a conventional current mirror) according to known methods (coupling a current source through a positive current mirror to a current sink, while scaling the mirror's gain to provide tunable amplification) to yield predictable results. Adding a current mirror simply uses a known technique (scaling currents between two branches of a current mirror) to improve Ishimaru by scaling its currents between the two branches of its circuits in the same way.

244. The combined teachings of Ishimaru and Harrison is consistent with the disclosure of the Asserted Patents in that the term *current mirror* can include current amplification circuits formed from a plurality of current mirrors combined (*e.g.*, cascaded) to achieve a target gain. '101 Patent 11:42-45*; see, e.g.*:

> As used herein, the term current mirror can refer to current amplification circuits including a plurality of current mirrors combined (e.g. cascaded) to achieve a target gain.

'101 Patent 11:42-45.

245. Thus, for the above-mentioned reasons, it is my opinion that Ishimaru in view of Harrison renders Claim 14 obvious.

246. It is also my opinion that Ishimaru in view of Ichitsubo and further in view of Harrison renders Claim 14 obvious.

247. It is also my opinion that Ishimaru in view of Johnson and further in view of Harrison renders Claim 14 obvious.

Claim 15

[redacted]

248. For all the limitations in Claim 15, I incorporate my opinions in §IX.D.1 ([15]) above, where I explain how Ishimaru and, alternatively, Ishimaru in view of Ichitsubo or Johnson disclose the limitations.

249. Thus, for the above reasons, it is my opinion that the combinations of Ishimaru in view of Harrison, Ishimaru in view of Ichitsubo and further in view of Harrison, and Ishimaru in view of Johnson and further in view of Harrison each renders Claim 15 obvious.

Claim 17

[17] The packaged module of claim 14 wherein the gain correction circuit includes a current mirror configured to generate the correction current by mirroring the control current, the current mirror configured to receive the power amplifier enable signal.

250. For all the limitations in Claim 17, I incorporate my opinions in §IX.D.1 ([17]) above, where I explain how Ishimaru and, alternatively, Ishimaru in view of Ichitsubo or Johnson disclose the limitations.

251. I also incorporate my opinions with respect to limitation [14.2.2.1] in §IX.D.2 ([14.2.2.1]) above, where I explain how Ishimaru in view of Harrison discloses a current mirror.

252. Thus, for the above reasons, it is my opinion that the combinations of Ishimaru in view of Harrison, Ishimaru in view of Ichitsubo and further in view of Harrison, and Ishimaru in view of Johnson and further in view of Harrison each renders Claim 17 obvious.

Claim 20

253. For all the limitations in Claim 20, I incorporate my opinions in §IX.D.1 ([20]) above, where I explain how Ishimaru and, alternatively, Ishimaru in view of Ichitsubo or Johnson disclose the limitations.

[redacted]

254. Thus, for the above reasons, it is my opinion that the combinations of Ishimaru in view of Harrison, Ishimaru in view of Ichitsubo and further in view of Harrison, and Ishimaru in view of Johnson and further in view of Harrison each renders Claim 20 obvious.

E. Detailed Opinions Relating to the Invalidity of the '101 Patent Based on Prior Art

255. For the reasons detailed below, it is my opinion that claims 1-2, 10-11, 17-18, and 20-22 of the '101 patent are invalid based on the disclosure of one or more prior art references.

256. My citations below to one or more references are merely exemplary and representative of the disclosure in the various prior art references. In no way should the citations below be considered limiting or the only relevant disclosure in any prior art reference.

1. Claims 1-2, 10-11, 17-18, and 21-22 are Anticipated by Ishimaru

Claim 1

[1.0] A power amplifier system comprising:

257. To the extent that the preamble is limiting, the bias and PA circuitry in Ishimaru's Figure 1 is *a power amplifier system* for "a high-frequency power amplifier to be used in radio communication devices." Ishimaru ¶¶1, 41, Fig. 1. The circuitry for the PA system includes "an amplification section having a first transistor for performing power amplification", as well as "a bias power source section", "bias circuit," and "a speedup circuit." Ishimaru Abstract, ¶¶10-12, Fig. 1 (annotated below); *see, e.g.*:

> In the power amplifier of the invention, at a start of power amplification by an amplifier transistor 103 serving as an amplification section, a speedup circuit 122 transiently increases a bias which is fed to the amplifier transistor 103 via a bias power source section composed of a bias circuit 111 and a power source circuit 112. As a result, the power amplification factor of the amplifier transistor 103 is transiently increased at the start of power amplification by the amplifier transistor 103. Thus, the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal such as a

[redacted]

> modulated-wave signal. Accordingly, in the invention, it becomes possible to suppress distortion increases of an amplification signal due to heat generation at the start time without using any temperature sensing element.

Ishimaru Abstract.

> an amplification section having a first transistor for performing power amplification;

Ishimaru ¶10.

> a bias power source section having a second transistor for feeding a bias to the first transistor; and

Ishimaru ¶11.

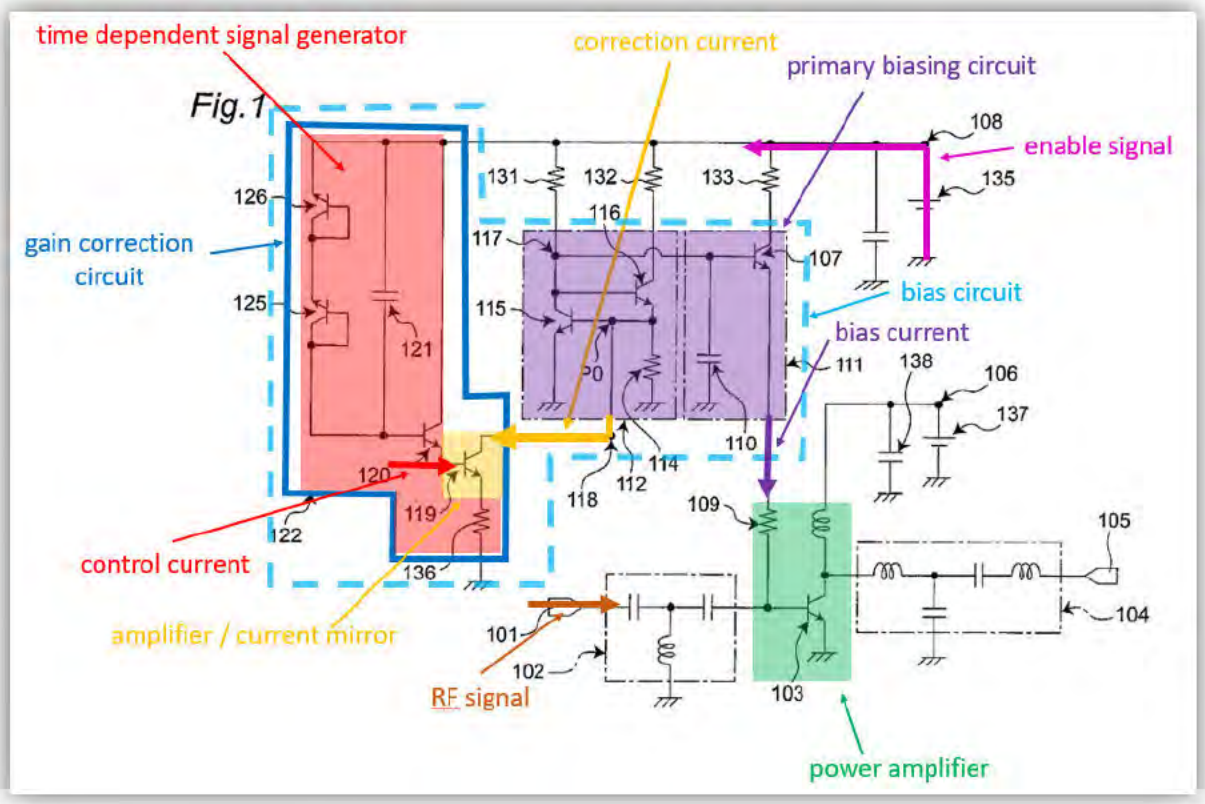
> a speedup circuit for transiently increasing the bias fed to the first transistor by bias power source section at a start of the power amplification.

Ishimaru ¶12.

[1.1] a power amplifier configured to amplify a radio frequency (RF) signal; and

258. Ishimaru discloses this limitation. Ishimaru discloses a *power amplifier configured to amplify a radio frequency RF signal* (green) in radio communications devices.

Ishimaru ¶¶1, 41, Fig. 1.



Ishimaru Fig. 1 (annotated).

259. Ishimaru discloses "a high-frequency power amplifier to be used in radio communication devices." Ishimaru ¶1. The circuitry for the PA includes "an amplification section having a first transistor for performing power amplification" (green) (*a power amplifier*). Ishimaru ¶¶10-12. As illustrated in Figure 1 (annotated above), Ishimaru further discloses that "a high-frequency signal as an input signal [is] inputted from an input signal terminal 101, … is amplified by an amplifier transistor 103 serving as a first transistor, and then, … outputted from an output signal terminal 105" (*power amplifier configured to amplify).* Ishimaru ¶42; *see, e.g.*:

> In this power amplifier, a high-frequency signal as an input signal inputted from an input signal terminal 101, passing through an input matching circuit 102, is amplified by an amplifier transistor 103 serving as a first transistor, and then, after passing through an output matching circuit 104, outputted from an output signal terminal 105. In FIG. 1, reference sign 106 denotes a collector bias terminal of the

[redacted]

> amplifier transistor 103. Between the collector bias terminal 106 and the ground are connected a DC power source 137 and a capacitance element 138. The amplifier transistor 103 forms an amplification section.

Ishimaru ¶42.

260. Specifically, because Ishimaru is directed to a PA for a **radio** communications device, a POSITA reading Ishimaru understood that the high-frequency input signal at input terminal 101 is a *radio frequency (RF) signal* (brown arrow) for amplification by amplifier transistor 103 (*a power amplifier configured to provide amplification*) to generate an amplified radio frequency signal at output terminal 105.

[1.2] a bias block for biasing the power amplifier, the bias block including

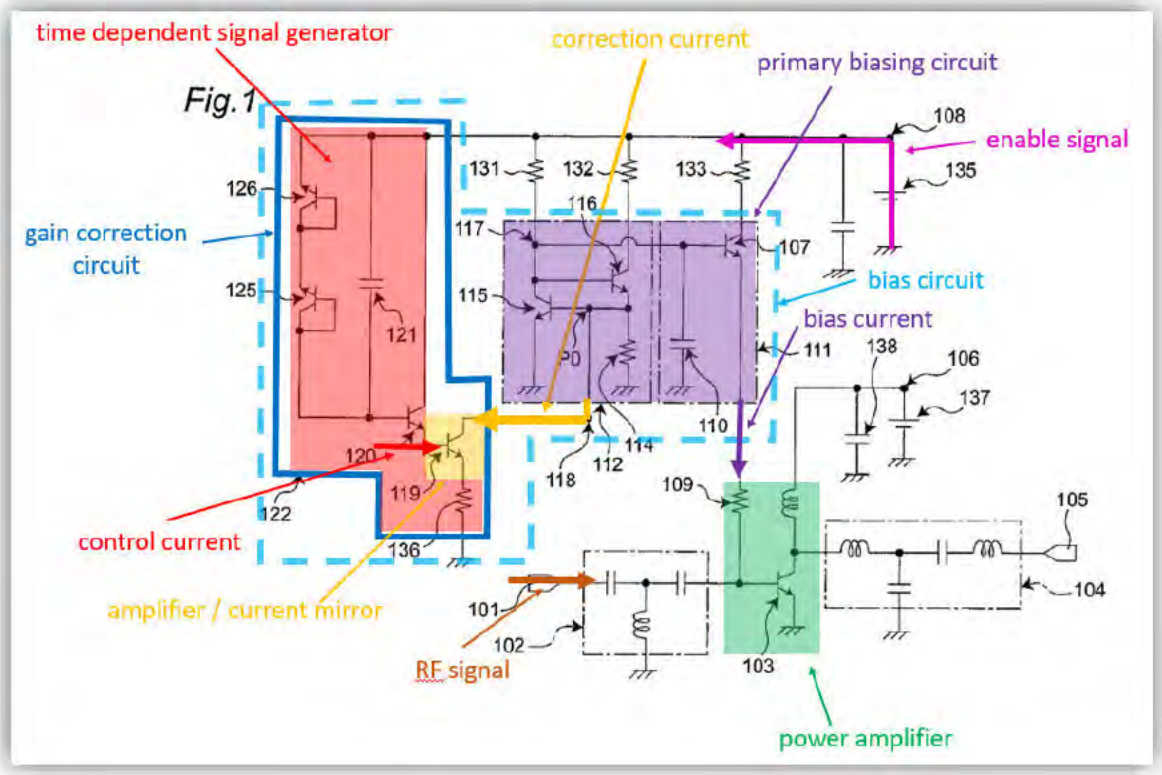
261. Ishimaru discloses this limitation. As shown in Figure 1 (annotated), Ishimaru discloses a "speedup circuit 122," "power source circuit 112," and "bias circuit 111" (collectively, *a bias block*) (light blue) that receives a control voltage from voltage source 135 (enable signal) (pink arrow) and supplies a "base bias current" (I_{BIAS}) (purple arrow) to the base terminal of amplifier transistor 103 (*biasing the power amplifier*) (green). Ishimaru Abstract, ¶¶24, 31, 43, 45, 49-52; *see, e.g.*:

> In the power amplifier of the invention, at a start of power amplification by an amplifier transistor 103 serving as an amplification section, a speedup circuit 122 transiently increases a bias which is fed to the amplifier transistor 103 via a bias power source section composed of a bias circuit 111 and a power source circuit 112. As a result, the power amplification factor of the amplifier transistor 103 is transiently increased at the start of power amplification by the amplifier transistor 103. Thus, the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal such as a modulated-wave signal. Accordingly, in the invention, it becomes possible to suppress distortion increases of an amplification signal due to heat generation at the start time without using any temperature sensing element.

Ishimaru Abstract.

A bias circuit 111 composed of the bias transistor 107 and a capacitance element 110 connected to a base terminal of the bias transistor 107 has a function of increasing the base bias current in response to an increase in signal strength of the input signal, and functions to keep the amplification ratio of an output signal as well as its phase rotation after amplification constant even when the signal strength of the input signal has changed.

Ishimaru ¶45.



Ishimaru Fig. 1 (annotated).

[1.2.1] a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current,

262. Ishimaru discloses this limitation. Ishimaru discloses two power sources, denoted as ("⊣⊢") in Figure 1 (annotated above) that serve different functions. The first power source, DC voltage 137, is connected to provide a constant DC power to amplification transistor 103.

[redacted]

Ishimaru ¶42. The second power source, control voltage source 135 at bias terminal 108, "controls turn-on and -off of power amplification." Ishimaru ¶24; *see, e.g.*:

> Accordingly, in this invention, at the start of power amplification, i.e., immediately after **the control voltage source that controls turn-on and -off of the power amplification is turned on** so that the bias voltage is applied from the control voltage source to the first transistor via the bias power source section, the current following into the base of the first transistor is transiently increased by the speedup circuit. As a result of this, variations in the operating current due to heat generation of the power amplifier or the like can be canceled, by which variations in amplification factor can be suppressed, and improvement of the linearity can be achieved. That is, without use of any temperature sensing element, since the speedup circuit **enabled** to adjust the transient response of the operating current is connected to the bias power source section, distortion increases of the amplification signal (modulated-wave signal) due to heat generation can be suppressed.

Ishimaru ¶24. Thus, Ishimaru's control voltage is *an enable signal of the power amplifier* (pink) as the PA is only operable when the bias is active and the bias is only active when the terminal 108 is high. The operation of Ishimaru's voltage source 135 is consistent with the '101 Patent's description of "an enable signal that can be used to enable or disable the power amplifier so as to pulse the power amplifier's output." '101 Patent 5:29-40.

263. With reference to Figure 1, Ishimaru discloses a speedup circuit 122 (dark blue) that includes a capacitance element 121, diodes 125 and 126, transistors 119 and 120, and resistance element 136 (*a time-dependent signal generator*) (red). Ishimaru¶¶ 50-51; *see, e.g.*:

> The speedup circuit 122 has a fifth transistor 119 whose collector is connected to the output terminal 118, and a sixth transistor 120 whose emitter is connected to a base of the fifth transistor 119. The emitter of the fifth transistor 119 is connected to the ground via a resistance element 136.

Ishimaru ¶50.

> The speedup circuit 122 also has a capacitance element 121 which is connected between a base of the sixth transistor 120 and the bias terminal 108, and two diodes 125, 126 which are connected in series between the base of the sixth transistor 120 and the bias terminal 108.

[redacted]

Ishimaru ¶51. In response to the "rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier)," (*enable signal*) (pink arrow), the speedup circuit applies a transient or time-varying current to the base of transistor 119 (*control current*) (red arrow). Ishimaru ¶52; *see, e.g.*:

> In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).

Ishimaru ¶52. This is a control current at least because it is used to control the correction to the biasing of Ishimaru's PA to compensate for gain variation, as discussed next.

264. Ishimaru's speedup circuit 122 (dark blue) includes a *time dependent signal generator* (red) in that it is a circuit configured to change an enable signal (pink arrow) of the PA to achieve a desired shape of ($I_{CONTROL}$) (red arrow), where the control current changes based on time. The shaping eventually results in the corresponding time-dependent current shown in Figure 3. Ishimaru ¶¶8-12, 52-56, Fig. 3. As explained in more detail below with respect to limitation [1.2.2], the speedup circuit 112 (dark blue) shapes $I_{CONTROL}$ (red arrow) and amplifies it to form a correction current ($I_{CORRECTION}$) (gold arrow) as a "current that transiently (temporarily) flows" out of the PA's primary biasing circuit (purple). Ishimaru ¶52.; *see infra* limitation [1.2.2]. The time-dependent shape of the $I_{CONTROL}$ (red arrow) is thereby used to shape the $I_{CORRECTION}$ (gold arrow) in an amount and duration necessary to cause the primary biasing

[redacted]

circuit to send a corresponding temporary boost in I_{BIAS} to the PA (green) to boost its gain during the startup period when its gain would otherwise be too low, *i.e.* to correct for the gain variation of the PA. Ishimaru ¶¶8-12, 52-55, Figs. 2 and 3. The speed up circuit, and its capacitor 121, changes the flat nature of the enable/on signal into a signal that is not just "on", but instead is made to have a desired time-varying shape for compensating PA gain variation. Ishimaru ¶¶49-52, 55-56; *see, e.g.*:

> In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).

Ishimaru ¶52.

> Next, FIG. 3 shows an example (simulation result) of transient response of the operating current (collector current Ic3) of the amplifier transistor 103 in the power amplifier of this embodiment. In this embodiment, the current to be fed from the bias transistor 107 to the amplifier transistor 103 is forcedly increased at turn-on of the amplifier, with the result that the value of the operating current Ic3 comes to a steady state in about 1/4 the time of transient response of the comparative example of FIG. 2. Thus, occurrence of distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed, so that the linearity of the circuit in burst operation is improved. That is, gain variations due to collector current variations of the power amplifier using a bipolar transistor can be compensated.

Ishimaru ¶54.

[1.2.2] a current amplifier configured to amplify the control current to generate a correction current, and

[redacted]

265. Ishimaru discloses this limitation. The *control current* ($I_{CONTROL}$) (red arrow) is amplified by transistor 119, (*current amplifier*) (gold) resulting in the transient *correction current* ($I_{CORRECTION}$) (gold arrow) being pulled into the collector of transistor 119 from node 118. Ishimaru ¶52; *see also supra* limitation [1.2.1]; *see, e.g.*:

> In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).

Ishimaru ¶52.

266. A POSITA recognized that transistor 119 amplifies its base current by the beta factor, β, of transistor 119 to provide amplification, *e.g.*, 60 to 150 or higher. Harrison 53-55; Illingworth 38 (practical β values can be "up to 500"); *see, e.g.*:

> **beta current gain factor** *Syn.* common-emitter forward-current transfer ratio; forward current gain. Symbol: β. The short-circuit current-amplification factor in a bipolar transistor with ►common-emitter connection: $\beta = \alpha I_c / \alpha I_B$ V_{CE} constant where I_C is the collector current and I_B is the base current; the collector voltage, V_{CE}, is constant. β is always greater than unity and practical values up to 500 are used.

Illingworth 38. Thus, transistor 119 is a *current amplifier configured to amplify* the current at its base (red arrow) (*the control current*) to generate the amplified $I_{CORRECTION}$ at its collector (gold arrow) (*to generate a correction current*). $I_{CORRECTION}$ (gold arrow) is a "current that transiently (temporarily) flows" out of the PA's primary biasing circuit (purple). Ishimaru ¶52. $I_{CORRECTION}$ (gold arrow) is a correction current in that it is shaped in an amount and duration necessary to

[redacted]

cause the primary biasing circuit (discussed below) to send a corresponding temporary boost in I_{BIAS} (purple arrow) to the PA (green) to boost its gain during the startup period when its gain would otherwise be too low, *i.e.* to correct for the gain variation of the PA. Ishimaru ¶¶8-12, 52, 55, Figs. 2 and 3. *See also, infra,* limitation [1.2.4] (discussing amplifier implemented as a current mirror with amplification due to mirror ratio); *see, e.g.*:

> an amplification section having a first transistor for performing power amplification;

Ishimaru ¶10.

> a bias power source section having a second transistor for feeding a bias to the first transistor; and

Ishimaru ¶11.

> a speedup circuit for transiently increasing the bias fed to the first transistor by bias power source section at a start of the power amplification.

Ishimaru ¶12.

> In the power amplifier of this embodiment also, the capacitance value of the capacitance element 121 of the speedup circuit 122 is adjusted so as to cancel transient variations in gain due to the temperature variations at a start of power amplification. As a result of this, deterioration of the linearity due to variations of amplification gain can be canceled so that the value of dynamic EVM (error vector magnitude) can be improved.

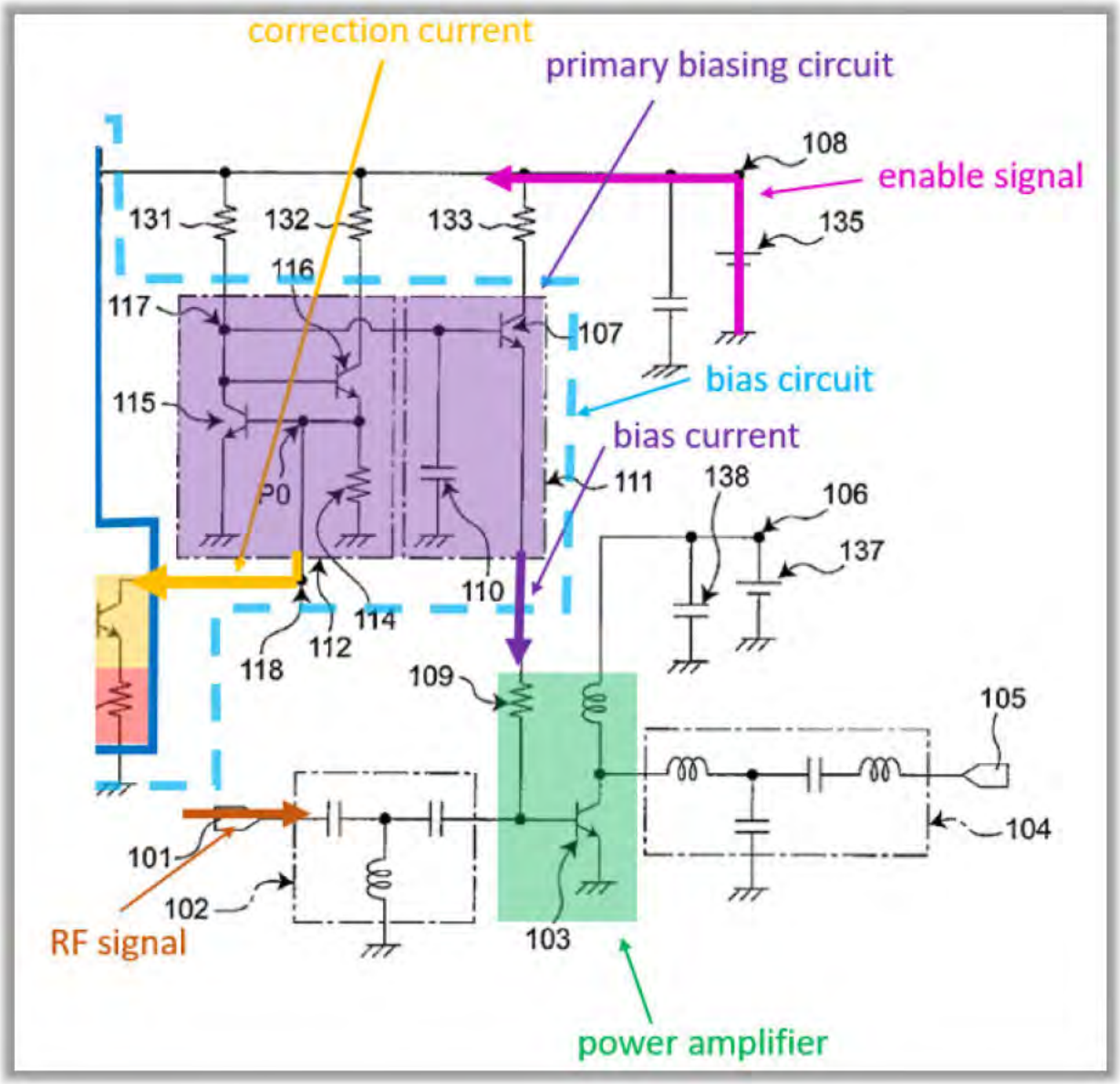
Ishimaru ¶55.

> ***[1.2.3] a primary biasing circuit configured to generate a bias current for the power amplifier based at least partly on the correction current, the bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled,***

267. Ishimaru discloses this limitation. As shown in the portion of Figure 1 reproduced below, Ishimaru discloses a power source circuit 112 and bias circuit 111, which constitute *the primary biasing circuit* (purple) which together supply a "base bias current" ($I_{BIAS,}$ *a bias current for the power amplifier*) (purple arrow) to the amplifier transistor 103. As

[redacted]

explained below, this boost I_{BIAS} is based on the current drawn out of node 118 ($I_{CORRECTION}$, *the correction current*) (gold arrow) when the control voltage is applied (*the power amplifier is enabled*) (pink arrow) to correct for a variation in gain of the PA at startup.



Ishimaru Fig. 1 (partial) (annotated);

268. Ishimaru explains that "bias circuit 111 and the power source circuit 112 constitute a bias power source section." Ishimaru ¶46; *see, e.g.*:

[redacted]

> A power source circuit 112 is connected to the base terminal of the bias transistor 107 of the bias circuit 111. The bias circuit 111 and the power source circuit 112 constitute a bias power source section.

Ishimaru ¶46. The combination of this circuitry is a *primary biasing circuit* in that it is the main circuitry used to generate the I_{BIAS} that biases the operating point of the transistor of the PA (green) to its intended state (e.g. *enabled*, and biased to operate at its intended operating point, suitable for amplification). *See, e.g.,* Horowitz 218, 220, 222-228; Harrison Fig. 2.1; *see, e.g.*:

> Transistor circuits are usually designed to amplify an ac input voltage rather than dc current. In this type of arrangement, the ac is superimposed on the dc. The dc is used to establish specific quiescent emitter and collector currents. These *bias currents* should set the idling voltage (voltage before ac is applied to the circuit) at the collector at one-half of E_{CC}. Because the collector voltage, V_C, is equal to $E_{CC} - I_C R_C$, V_C should be idling at about $E_{CC}/2$.

Horowitz 218.

> Bias or idling conditions are established when there is no ac voltage at the input of the circuit, or $E_{IN} = 0$. At this time, only the dc emitter supply voltage less the base-emitter voltage is across R_C the only component in this circuit that is outside of the transistor.

Horowitz 220.

> As was true in the common-base circuit, it is also desirable here to let the voltage at the collector terminal in this circuit idle at $E_{cc}/2$ volts. To do this, the idling voltage across R_c must be equal to half of the supply voltage, or $I_C R_C = E_{CC}/2$. Because I_C is related to I_B, I_B is set by the designer of the circuit to equal the desired le divided by beta. I_B can, of course, be set by using the proper base resistor, R_B, in the circuit. Ac signal voltage is usually fed through a capacitor to the base and applied between the base and emitter to the transistor. The input voltage varies the base and hence collector current in step with the cyclic variations of the ac. A magnified version of the ac input voltage is developed across the collector resistor by the ac collector current flowing through it.

Horowitz 223. More specifically, bias circuit 111 is "composed of the bias transistor 107 and a capacitance element 110" connected to the base of bias transistor 107. Ishimaru ¶45; *see, e.g.*:

> A bias circuit 111 composed of the bias transistor 107 and a capacitance element 110 connected to a base terminal of the bias transistor 107 has a function of increasing the base bias current in response to an increase in signal strength of the input signal, and functions to keep the amplification ratio of an output signal as well

[redacted]

> as its phase rotation after amplification constant even when the signal strength of the input signal has changed.

Ishimaru ¶45. Bias transistor 107's collector is connected to bias terminal 108 through a resistor 133, and the bias terminal 108 is connected to control voltage source 135 (*enable signal*) (pink arrow). Ishimaru ¶44; *see, e.g.*:

> The bias transistor 107 has its collector connected to a bias terminal 108 via a resistance element 133. The bias terminal 108 is connected to a control voltage source 135.

Ishimaru ¶44. The emitter of bias transistor 107 is connected to a base terminal of the amplifier transistor 103 via resistance element 109 and "supplies a base bias current to the base of amplification transistor 103." Ishimaru ¶43; *see, e.g.*:

> Also, a bias transistor 107 as a second transistor is a transistor that supplies a base bias current to a base terminal of the amplifier transistor 103. An emitter of the bias transistor 107 is connected to a base terminal of the amplifier transistor 103 via a resistance element 109. The resistance element 109 is a ballast (stabilization) resistor which is inserted in a base bias channel to prevent thermal runaway of the amplifier transistor 103.

Ishimaru ¶43. The "base bias current" (I_{BIAS}) is *a bias current*.

269. Bias transistor 107 in circuit 111 operates in conjunction with power source circuit 112 to generate I_{BIAS} that is applied to the amplifier transistor 103 and thus, circuit 111 and 112, collectively are *a primary biasing circuit* (purple).

270. More specifically, as shown in the portion of the annotated Figure 1 above, node 117 of circuit 112 is connected to the base terminal of the bias transistor 107 and, thus, controls the bias point of transistor 107 and, consequently, the transistor 107's collector current. Ishimaru ¶¶46, 48; *see, e.g.*:

> A power source circuit 112 is connected to the base terminal of the bias transistor 107 of the bias circuit 111. The bias circuit 111 and the power source circuit 112 constitute a bias power source section.

[redacted]

Ishimaru ¶46. Node P0 of power source circuit 112 (*i.e.*, the base of transistor 115 and emitter of transistor 116) is connected to output terminal 118 of speedup circuit 122. *Id.* ¶¶48-49; *see, e.g.*:

> In this embodiment, as shown in FIG. 1, the power source circuit 112 has a third transistor 115, a fourth transistor 116, and a resistance element 114. The third transistor 115 has its collector connected to the base of the bias transistor 107 and its emitter connected to the ground. Also, a base of the third transistor 115 is connected to an emitter of the fourth transistor 116. The collector of the third transistor 115 is connected to the bias terminal 108 via a resistance element 131. Meanwhile, the fourth transistor 116 has its emitter connected to the ground via the resistance element 114 and its collector connected to the bias terminal 108 via a resistance element 132.

Id. ¶48.

271. Ishimaru explains that, at a rise time of the control voltage from the control voltage source 135, "a current transiently (temporarily) from the output terminal 118" flows into the speedup circuit 122. Ishimaru ¶52. As explained in [1.2.2] above, this current is $I_{CORRECTION}$. Ishimaru ¶52; *see, e.g.*:

> In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).

Ishimaru ¶52. The transient rise in $I_{CORRECTION}$ causes the voltage at output terminal 118 to lower, which raises the voltage at the collector of transistor 115 (node 117), which controls the bias transistor 107, and this causes "the current fed to the amplifier transistor by the bias transistor

[redacted]

107" (*the bias signal*) to transiently increase to correct for a variation in gain of the PA when the PA is enabled. Ishimaru ¶52, *see also* ¶¶8-12, 31, 53-55, Figs. 2 and 3; *see, e.g.*:

> According to the power amplifier of this embodiment, by electric charge flowing into the capacitance element at a rise time of the control voltage of the control voltage source (upon turn-on of the amplifier), a current transiently (temporarily) flows into the collector of the fifth transistor, causing the voltage value of the collector to lower. As a result, due to a change of the bias point of the third transistor, the voltage of the connecting terminal at which the collector of the third transistor is connected to the base of the second transistor is temporarily increased. Thus, the current fed to the first transistor by the second transistor is transiently increased at the rise time. Therefore, the power amplification factor of the first transistor is transiently increased at the rise time, so that the time elapsing until temperature variations due to heat generation of the first transistor come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).

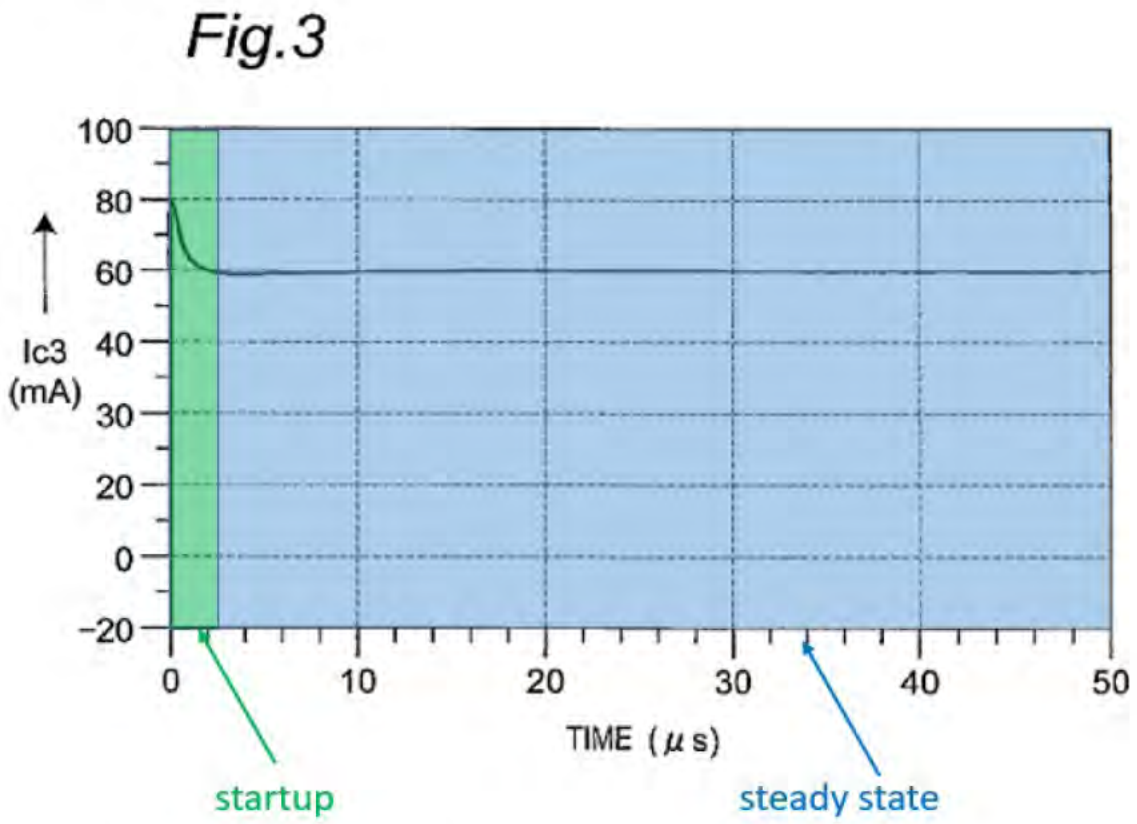
Ishimaru ¶31.

272. Figure 3, which shows the transient response of the collector current of the amplifier transistor 103, illustrates how the transient rise in $I_{CORRECTION}$ causes the collector current of the amplifier transistor 103 to temporarily increase during startup to compensate for gain variations due to collector current variations of the PA using a bipolar transistor (*to correct for a variation in gain of the power amplifier when the power amplifier is enabled*). Ishimaru ¶54, Fig. 3; *see, e.g.*:

> Next, FIG. 3 shows an example (simulation result) of transient response of the operating current (collector current Ic3) of the amplifier transistor 103 in the power amplifier of this embodiment. In this embodiment, the current to be fed from the bias transistor 107 to the amplifier transistor 103 is forcedly increased at turn-on of the amplifier, with the result that the value of the operating current Ic3 comes to a steady state in about 1/4 the time of transient response of the comparative example of FIG. 2. Thus, occurrence of distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed, so that the linearity of the circuit in burst operation is improved. That is, gain variations due to collector current variations of the power amplifier using a bipolar transistor can be compensated.

Ishimaru ¶54.

[redacted]



Ishimaru Fig. 3 (annotated), *contrast* Fig. 2, ¶53.

273. More specifically, the transient rise in $I_{CORRECTION}$ causes the collector current of the amplifier transistor 103 to temporarily increase during startup *to correct for a variation in gain of the power amplifier when the power amplifier is enabled*:

> Thus, occurrence of **distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed**, so that the **linearity** of the circuit in burst operation is **improved**. That is, **gain variations** due to collector current variations of the power amplifier using a bipolar transistor **can be compensated**.

Ishimaru ¶54.

274. This transient increase in the collector current of amplifier transistor 103 is due to a transient increase in I_{BIAS} (*a bias signal*) into amplifier transistor 103 because the collector current amplifies the base bias current via the amplifier transistor 103's amplification factor β.

[redacted]

Further, Ishimaru explicitly explains that the collector current 103 (also called "operating current Ic3") "comes to a steady state in about ¼ of the time of transient response of the comparative example of Fig. 2," which is the transient response without speedup circuit 122. Ishimaru ¶¶53-54, Figs. 2 and 3; *see, e.g.*:

> FIG. 2 shows an example of transient response of an operating current (collector current Ic3) of the amplifier transistor 103 in a comparative example in which the speedup circuit 122 is removed in the circuit of FIG. 1. In this comparative example having no speedup circuit, due to the fact that a temperature increasing rate of the bias transistor 107 is slower than that of the amplifier transistor 103, the value of the current fed from the bias circuit 111 to the amplifier transistor 103 continues to vary, the variations in current value making a cause of signal distortion.

Ishimaru ¶53

> Next, FIG. 3 shows an example (simulation result) of transient response of the operating current (collector current Ic3) of the amplifier transistor 103 in the power amplifier of this embodiment. In this embodiment, the current to be fed from the bias transistor 107 to the amplifier transistor 103 is forcedly increased at turn-on of the amplifier, with the result that the value of the operating current Ic3 comes to a steady state in about 1/4 the time of transient response of the comparative example of FIG. 2. Thus, occurrence of distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed, so that the linearity of the circuit in burst operation is improved. That is, gain variations due to collector current variations of the power amplifier using a bipolar transistor can be compensated.

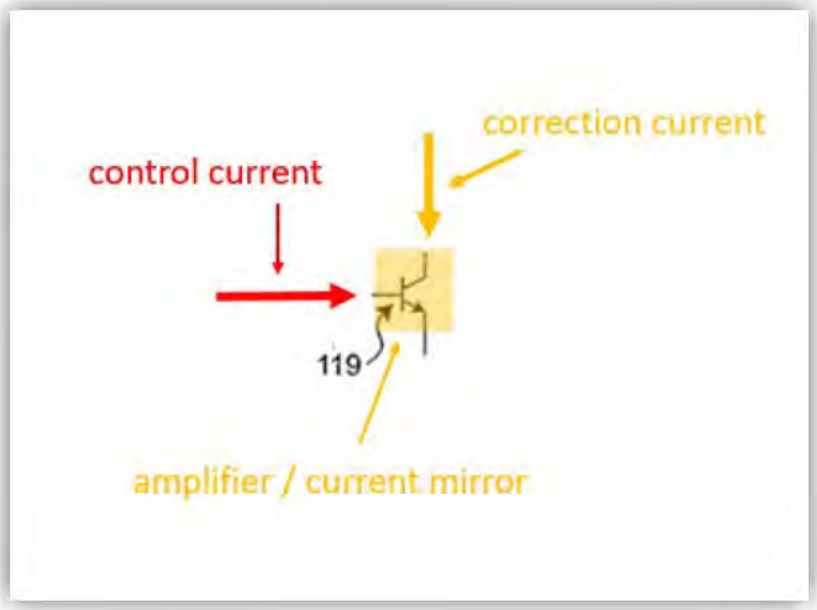
Ishimaru ¶54.

275. Accordingly, Ishimaru discloses *a primary biasing circuit* (purple) configured to generate a *bias current* (purple arrow) for the *power amplifier* (green) based at least partly on the *correction current* (gold arrow), the *bias current configured to correct for a variation in gain of the power amplifier* (purple arrow) at startup (*when the power amplifier is enabled*).

[1.2.4] the current amplifier including a current mirror.

276. Ishimaru's transistor 119 is a current amplifier. *See supra* limitation [1.2.2]. Like the preferred embodiment of the '101 Patent, a current mirror can constitute the current

amplifier. *See* '101 Patent 10:23. As shown in Figure 1, annotated and partially reproduced below, Ishimaru's transistor 119 is a *current amplifier including a current mirror* (gold) in that transistor 119 is configured to replicate (*i.e. mirror*) and scale (amplify) the $I_{CONTROL}$ *(red arrow)* to generate the $I_{CORRECTION}$ *(gold arrow)*.



Ishimaru Fig. 1 (annotated) (partial).

277. Consistent with the discussion of current mirrors in the State of the Art section, transistor 119 as connected in Ishimaru is configured to mirror in that it is configured to replicate (reproduce, duplicate, reflect, etc.), *i.e., mirror* the current at its input (the base of transistor 119) to generate the current at its output (the collector of transistor 119). §VIII.C.2; Ishimaru Fig. 1.

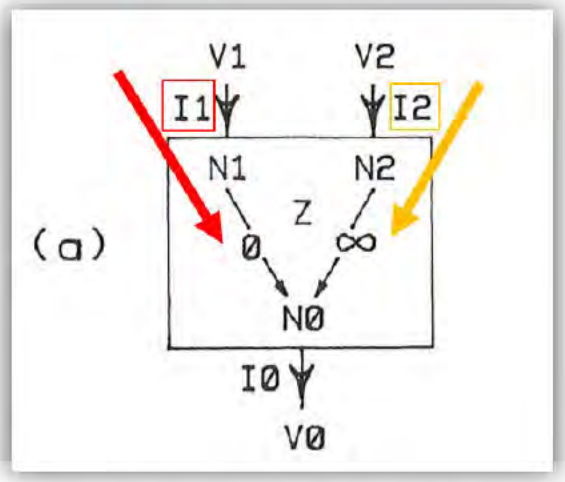
278. When connected as shown in Ishimaru, transistor 119 takes the general, three-node form set out by Barrie Gilbert and Gray for a *current mirror*. Gilbert Fig. 6.1a; Gray Fig. 4.1. Accordingly, in the side-by-side images below, Ishimaru's transistor 119 is used as a current mirror in that node Nl (of Gilbert Figure 6.la showing a current mirror) is the base of transistor 119, N2 the collector of transistor 119, and N0 the emitter of transistor 119, with the

[redacted]

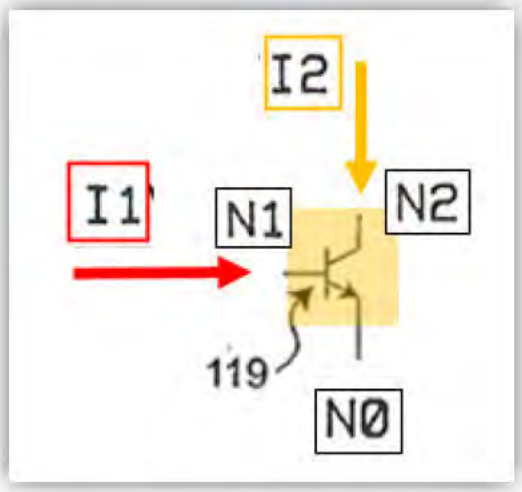
circuit replicating (and scaling) current I1 to generate output current I2. Gilbert 242, Fig. 6.1a; Gray Fig. 4.1; *see, e.g.*:

> In the simplest possible scenario, a single BJT can be used as a mirror: node N1 (of Figure 6. la) is the base, N2 the collector and NO the emitter.

Gilbert 242.

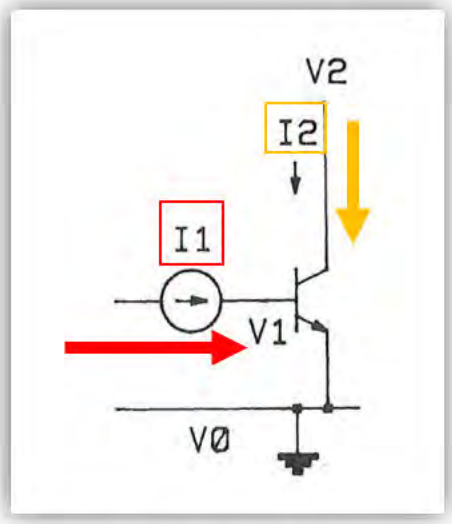


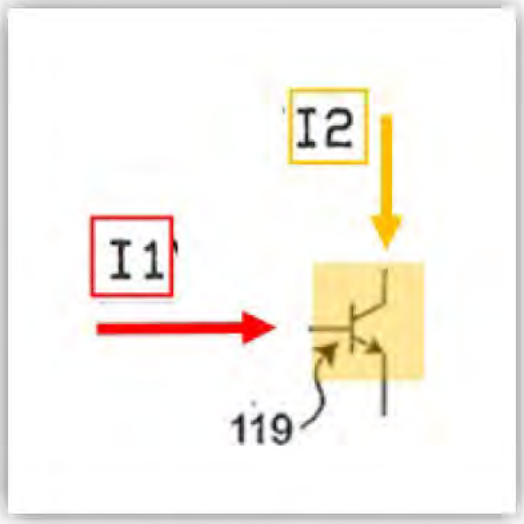
Gilbert 240, Fig. 6.1a (annotated)



Ishimaru Fig. 1 (annotated)(partial)

279. Likewise, Ishimaru's transistor 119 is connected and used in the same way as Gilbert's single transistor current mirror shown in his Figure 6.2a:





Gilbert 243, Fig. 6.2a (annotated) **Ishimaru Fig. 1 (annotated)(partial)**

280. In addition to the replication discussed above, Ishimaru's current mirror is further configured to **amplify** the $I_{CONTROL}$, scaling it up by the amplification factor, namely scaling by the common-emitter current-gain, β, of the transistor 119, which quantifies the "mirror ratio" (discussed below) of Ishimaru's current mirror. §VIII.C.2, Illingworth 38; Gilbert 242-243; *see, e.g.*:

> **beta current gain factor** *Syn.* common-emitter forward-current transfer ratio; forward current gain. Symbol: β. The short-circuit current-amplification factor in a bipolar transistor with ►common-emitter connection: $\beta = \alpha I_c / \alpha I_B$ V_{CE} constant where I_C is the collector current and I_B is the base current; the collector voltage, V_{CE}, is constant. β is always greater than unity and practical values up to 500 are used.

Illingworth 38.

> In the simplest possible scenario, a single BJT can be used as a mirror: node Nl (of Figure 6. la) is the base, N2 the collector and NO the emitter.
>
> Figure 6.2a shows the biasing for an NPN device. We wish to determine the input and output resistances. It will be assumed that β is independent of current over the range of interest. If β were also independent of V_2, the output I_2 would always be simply βI_1 and the output resistance r_o would be infinite. In fact, β increases with V_2 due to base-width modulation, and in the customary BJT model would be

[redacted]

> exactly doubled when the collector bias voltage, V_{CB} (roughly, V_2), is equal to the forward Early voltage, V_{AF}.

Gilbert 242-243.

281. While Gilbert recognizes that other current mirror forms have wider flexibility at the design stage, that is not pertinent to Ishimaru. First, the single-transistor mirror is nonetheless a current mirror. The claims do not have a performance requirement. Moreover, as Gilbert describes, the single-transistor mirror has the advantage that its mirror ratio, β, is high, making it suitable for Ishimaru's circuit, which requires a high mirror ratio.

282. More specifically, the current at the collector (I_{C119}) of transistor 119 (a transistor having β_{119}) is generally related to the current at the transistor's base (I_{B119}) by the equation: $I_{C119} = \beta_{119} * I_{B119}$. *Id.*; Ishimaru Fig. 1. Thus, the ratio of the input current I_{B119} to the output current I_{C119} is generally β_{119}. Ishimaru Fig. 1. The gain through the transistor is the "mirror ratio", "M", by which Ishimaru's *current mirror* scales the $I_{CONTROL}$ to generate the $I_{CORRECTION}$ Gilbert 242-243; Ishimaru Fig. 1. The gain of transistor 119 can be configured to a target value by designing the voltage and current biasing of the transistor 119 (within the constraints of the circuit), such that a targeted and desired β (from within an available range, *e.g.,* of about 60 to 150 or more), can be achieved.[11] The time constant of the transient can then be tuned through the choice of components, namely C121 and R136. Ishimaru ¶¶55-56; *see also, infra,* Claim 2; *see, e.g.*:

> In the power amplifier of this embodiment also, the capacitance value of the capacitance element 121 of the speedup circuit 122 is adjusted so as to cancel transient variations in gain due to the temperature variations at a start of power

[11] While the single-transistor current mirror of Ishimaru does not have as widely controllable a mirror ratio as other current mirrors (a mirror ratio of, e.g., 2 is better suited for other current mirror forms), the single transistor mirror is suitable if one needs a high mirror ratio, such as can be provided by the β factor controllable by appropriately biasing the single-transistor mirror.

[redacted]

> amplification. As a result of this, deterioration of the linearity due to variations of amplification gain can be canceled so that the value of dynamic EVM (error vector magnitude) can be improved.

Ishimaru ¶55.

> In addition, the capacitance element 121 of the speedup circuit 122 may be a capacitance element whose capacitance value is changeable. In this case, changing the capacitance value of the capacitance element 121 makes it possible to adjust the time duration during which the bias fed to the amplifier transistor 103 at a start of amplification operation by the speedup circuit 122 via the bias power source section composed of the power source circuit 112 and the bias circuit 111 is kept increased.

Ishimaru ¶56.

283. Thus, transistor 119 as connected in Ishimaru is a *current mirror* in that it constitutes a circuit configured to mirror a current, which can be configured to achieve a target gain. Consistent with the plain meaning for "current mirror" proposed by Respondents, transistor 119 is a circuit that has electrical interconnections, including input, output, and other connections that permit current to flow through the circuit. *See*:

> Plain meaning, such as "one or more circuits configured to mirror a current, which can be configured to achieve a target gain"

§VII.C.

284. Therefore, it is my opinion that Ishimaru anticipates Claim 1.

Claim 2

[2] The power amplifier system of claim 1 wherein the time-dependent signal generator includes a resistor-capacitor (RC) network.

285. Ishimaru discloses this limitation. As illustrated in Figure 1 (annotated above), Ishimaru's PA system includes a speedup circuit (dark blue) that includes a *time-dependent signal generator* (red) that "transiently (temporarily) increases" the I_{BIAS} fed to the amplifier transistor by the bias circuit during the period after startup. Ishimaru ¶13; *see, e.g.*:

[redacted]

> According to the power amplifier of this invention, at a start of power amplification by the first transistor of the amplification section, the speedup circuit transiently (temporarily) increases the bias fed to the first transistor by the bias power source section, so that the power amplification factor of the first transistor is transiently increased at the start of power amplification. Thus, the time elapsing until temperature variations due to heat generation of the first transistor (amplifier transistor) that performs the power amplification come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated-wave signal).

Ishimaru ¶13. Speedup circuit 122 includes transistors 119, 120, *resistor* 136, as well as a *capacitor* 121 connected between the base of transistor 120 and bias terminal 108. Ishimaru ¶¶50-51, 55-56; *see, e.g.*:

> The speedup circuit 122 has a fifth transistor 119 whose collector is connected to the output terminal 118, and a sixth transistor 120 whose emitter is connected to a base of the fifth transistor 119. The emitter of the fifth transistor 119 is connected to the ground via a resistance element 136.

Ishimaru ¶50.

> The speedup circuit 122 also has a capacitance element 121 which is connected between a base of the sixth transistor 120 and the bias terminal 108, and two diodes 125, 126 which are connected in series between the base of the sixth transistor 120 and the bias terminal 108.

Ishimaru ¶51. The charging time of capacitor 121 depends on the size of the capacitor and the resistance through R136 to ground, which sets the shape of the control current from the speedup circuit 122. Ishimaru ¶¶55-56; *see, e.g.*:

> In the power amplifier of this embodiment also, the capacitance value of the capacitance element 121 of the speedup circuit 122 is adjusted so as to cancel transient variations in gain due to the temperature variations at a start of power amplification. As a result of this, deterioration of the linearity due to variations of amplification gain can be canceled so that the value of dynamic EVM (error vector magnitude) can be improved.

Ishimaru ¶55.

> In addition, the capacitance element 121 of the speedup circuit 122 may be a capacitance element whose capacitance value is changeable. In this case, changing the capacitance value of the capacitance element 121 makes it possible to adjust the time duration during which the bias fed to the amplifier transistor 103 at a start of

[redacted]

> amplification operation by the speedup circuit 122 via the bias power source section composed of the power source circuit 112 and the bias circuit 111 is kept increased.

Ishimaru ¶56. A POSITA understands that this speedup circuit forms an *RC network*.

286. More specifically, a POSITA understands that Ishimaru applies a large current amplification (by virtue of transistors 119, and 120)[12] to the transient current controlled by "capacitance element 121." Ishimaru ¶¶52, 55-56, Fig. 1 (capacitor 121, transistors 119 and 120, and resistor 136); *see, e.g.*:

> In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).

Ishimaru ¶52. When the enable signal turns on, capacitor 121 charges by virtue of current flowing through transistor 119, transistor 120 and resistor 136 to ground. Owing to the very high gain of transistors 119 and 120, the current in the capacitor can be made very small, and therefore the capacitor 121 can be made small for a given time constant. Likewise, the size of resistor 136 can be small as the capacitor current (I_{C121}) is generally the resistor current (I_{R136}) divided by the gain of transistors 119 and 120. In Ishimaru, a physically small resistor can be used for R136 as its current, when traced back to C121, will be greatly reduced by the gain of

[12] Each transistor has an amplification factor, "β" that relates the transistor's base current to its collector current. (*e.g.* Illingworth 38).

[redacted]

119 and 120. Increasing the size of R136, or the size of C121, will slow the rate at which C121 charges, providing the circuit with a time-dependent signal that has a longer time constant. Conversely, a smaller C121 and/or R136 will allow the capacitor to charge more rapidly, providing a time-dependent signal that reaches steady state more quickly. In this way, the time constant of Ishimaru's speedup circuit depends on the size of capacitor C121, resistor R136, and the current gain value, β, of transistor 119 and 120. This is further corroborated by Horowitz when discussing the common emitter amplifier circuit, where "beta is an important factor in determining the operation of the circuit." Horowitz 223, 224, *e.g.*:

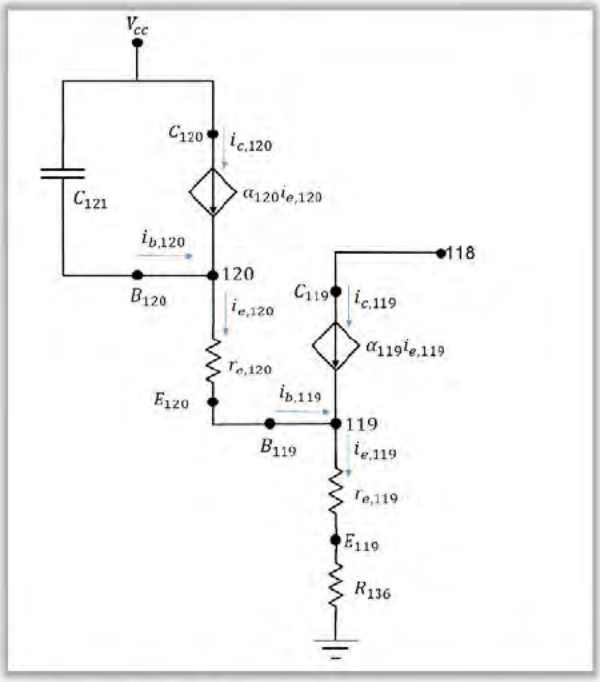
> In determining the base current, therefore, you can consider R_E as being in series with the base, replacing the lead at which arrow "x" is pointing. But before putting it there, R_E must be multiplied by beta. This is because the actual voltage developed across R_E is due to a current equal to beta multiplied by the current flowing in the base circuit. So in order for the same voltage to be developed across the resistor when moved to the base circuit as was developed across it in its original location, R_E must be multiplied by beta before being relocated. As a result, the total resistance in the base circuit is $R_B + \beta R$.

Horowitz 224 (referencing Fig. 8-8 on page 223). This is further, independent support for my opinion. Thus, Ishimaru's *time-dependent signal generator* includes *a resistor-capacitor (RC) network* that includes capacitor 121 and resistor 136.

287. While unnecessary to my opinions, to the extent one wanted to confirm the relationships of the timing of Ishimaru's circuit as controlled by capacitor 121 and resistor 136, one could do so in a variety of ways. The following analysis is one of several ways one might characterize the behavior of the RC network in Ishimaru's speed-up circuit. Nothing about my opinions depends on the following particular formulation. Nonetheless, my opinions are further consistent with and further supported by the following derivation of an approximate time constant for the Ishimaru speed-up circuit.

[redacted]

288. For example, one approximation of an RC time constant, τ, associated with Ishimaru's speed-up circuit can be derived by modeling the effective resistance of transistor 119 and 120 by the small-signal T-model shown below.



Ishimaru Speedup Circuit Small Signal T model.

289. As derived in Appendix E, the effective resistance seen by Ishimaru's speed-up circuit is approximated by the following equation:

$$R_{eff,120} = (\beta + 1)(r_{e,120}) + (\beta + 1)^2 (r_{e,119} + R_{136})$$

For the series resistor, $R_{eff,120}$, and capacitor, $C_{,121}$, in Ishimaru's circuit, the time constant can be defined:

$$\tau = \left[(\beta + 1)(r_{e,120}) + (\beta + 1)^2 (r_{e,119} + R_{136})\right] C_{121}$$

290. From this definition of the RC time constant (τ), it is apparent that the time constant of Ishimaru's speedup circuit primarily depends on the second term (i.e., $(\beta + 1)^2 (r_{e,119} + R_{136}) C_{121}$). This is due to the fact that a transistor current gain value, β, is

[redacted]

commonly on the order of, *e.g.*, 100, or higher. If we assume $\beta = 100$, then second term from (13) has a multiplier term (i.e., $(\beta + 1)^2$) of approximately 10,000. We also note that the value of $r_{e,119}$ is negligible in the Ishimaru circuit.

291. Thus, I have further provided support for my conclusion that that the time constant of Ishimaru's speedup circuit depends at least, and indeed primarily, on the values of R_{136}, $C_{,121}$, and the current gain value, β, of transistors 119 and 120.

292. Therefore, it is my opinion that Ishimaru anticipates Claim 2.

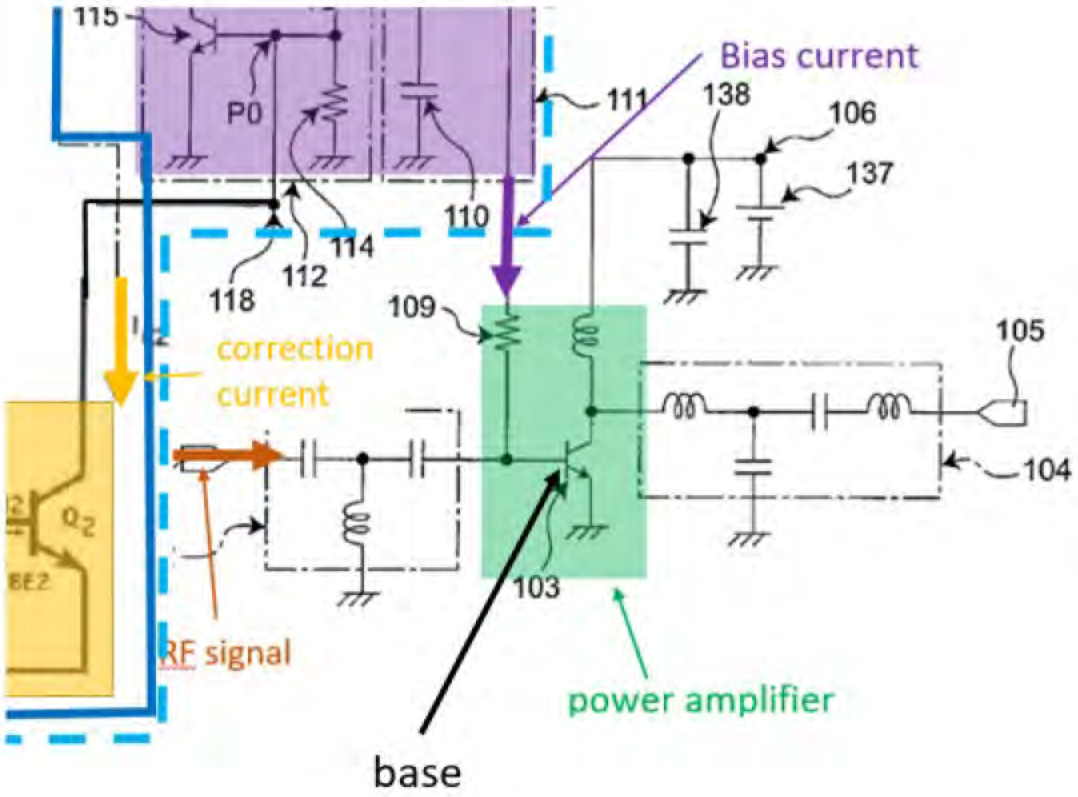
Claim 10

[10] The power amplifier system of claim 1 wherein the power amplifier includes a bipolar transistor having an emitter, a base and a collector, the base configured to receive the RF signal and the bias current.

293. Ishimaru discloses this limitation. Ishimaru discloses that transistor 103 is a *bipolar transistor*. Ishimaru ¶¶54, 55. In Ishimaru, the base of transistor 103 receives the "high-frequency signal" for "radio communication devices" from terminal 101 (*where the base is configured to receive the RF signal*) and bias transistor 107 "supplies a base bias current to a base terminal of the amplifier transistor 103" (*the base receives the bias current*). Ishimaru ¶¶41-42*; see, e.g.*:

> In this power amplifier, a high-frequency signal as an input signal inputted from an input signal terminal 101, passing through an input matching circuit 102, is amplified by an amplifier transistor 103 serving as a first transistor, and then, after passing through an output matching circuit 104, outputted from an output signal terminal 105. In FIG. 1, reference sign 106 denotes a collector bias terminal of the amplifier transistor 103. Between the collector bias terminal 106 and the ground are connected a DC power source 137 and a capacitance element 138. The amplifier transistor 103 forms an amplification section.

Ishimaru ¶42. As illustrated in the annotated portion of Figure 1 below, the base of transistor 103 receives *the RF signal* (brown arrow) and the *bias current* (purple arrow):



Ishimaru, Fig. 1 (partial) (annotated); *see* §VIII.C.1 (showing BJT terminals).

294. Therefore, it is my opinion that Ishimaru anticipates Claim 10.

Claim 11

[11] The power amplifier system of claim 10 wherein the emitter is electrically connected to a power low voltage and the collector is configured to generate an amplified version of the RF signal.

295. Ishimaru discloses this limitation. Figure 1 (annotated partial below) shows an input signal terminal 101 that receives a high-frequency signal (brown arrow) as an input signal, and this input signal passes through an input matching circuit 102, and is then amplified by amplifier transistor 103 (green). The amplifier transistor 103 outputs a signal through output matching circuit 104 to output signal terminal 105 as an amplified version of the RF input signal

[redacted]

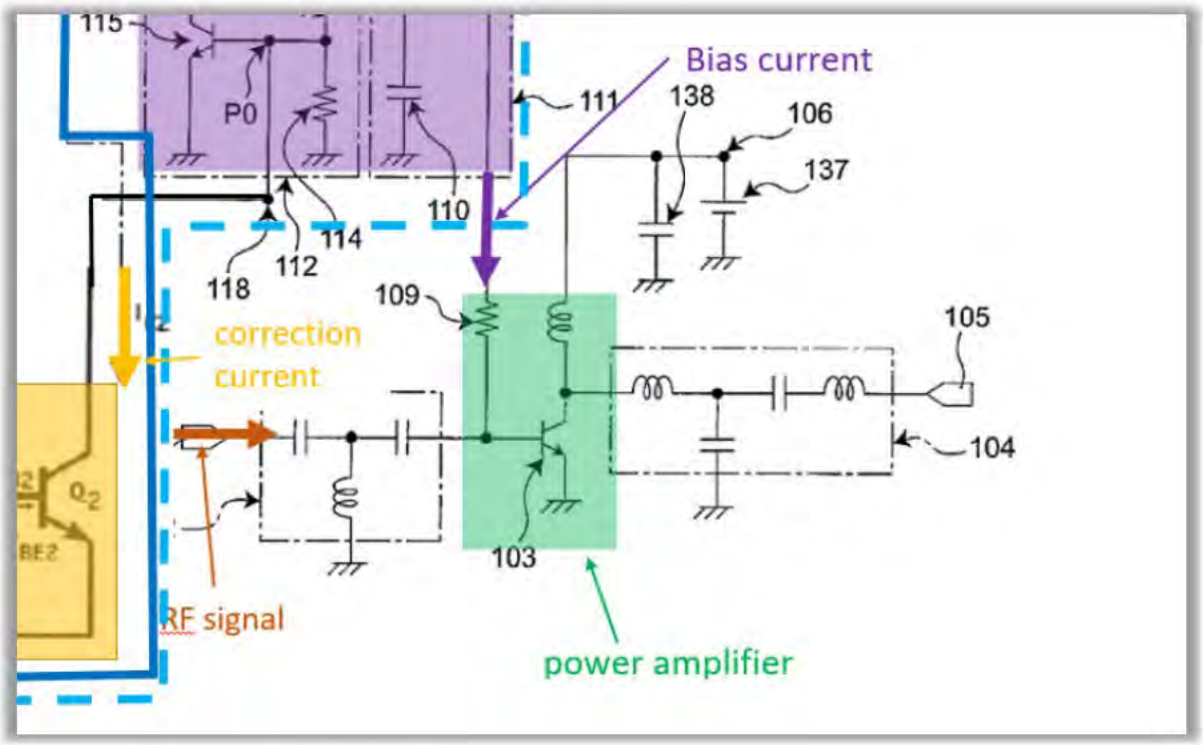
(*the collector is configured to generate an amplified version of the RF signal*). Ishimaru ¶¶41-43, 46, 49*; see, e.g.*:

> In this power amplifier, a high-frequency signal as an input signal inputted from an input signal terminal 101, passing through an input matching circuit 102, is amplified by an amplifier transistor 103 serving as a first transistor, and then, after passing through an output matching circuit 104, outputted from an output signal terminal 105. In FIG. 1, reference sign 106 denotes a collector bias terminal of the amplifier transistor 103. Between the collector bias terminal 106 and the ground are connected a DC power source 137 and a capacitance element 138. The amplifier transistor 103 forms an amplification section.

Ishimaru ¶42.

> A power source circuit 112 is connected to the base terminal of the bias transistor 107 of the bias circuit 111. The bias circuit 111 and the power source circuit 112 constitute a bias power source section.

Ishimaru ¶46.



Ishimaru, Fig. 1 (partial) (annotated).

[redacted]

296. Figure 1 further illustrates that the emitter of transistor 103 is electrically connected to Ground which a POSITA understood was a *power low voltage*. Ishimaru's disclosure is consistent with the disclosure of the '101 Patent, in which the emitter of the bipolar transistor 61 is likewise connected to ground. '101 Patent 7:45-51, Fig. 3B*; see, e.g.*:

> The illustrated power amplifier 32 includes a bipolar transistor 61 having an emitter, a base, and a collector. The emitter of the bipolar transistor 61 can be electrically connected to a first or power low voltage V_1 , which can be, for example, ground, and a radio frequency input signal RF_IN can be provided to the base of the bipolar transistor 61 through the first capacitor 42.

'101 Patent 7:45-51.

297. Therefore, it is my opinion that Ishimaru anticipates Claim 11.

Claim 17

[17.0] A method of biasing a power amplifier, the method comprising:

298. To the extent the preamble is limiting, Ishimaru discloses this limitation for the same reasons as discussed with respect to limitation [1.2].

[17.1] shaping an enable signal using a time-dependent signal generator to generate a control current;

299. Ishimaru discloses this limitation for the same reasons as discussed with respect to limitation [1.2.1].

[17.2] amplifying the control current using a current mirror of a current amplifier to generate a correction current; and

300. Ishimaru discloses this limitation for the same reasons as discussed with respect to limitations [1.2.2] and [1.2.4].

[17.3] generating a bias current for a power amplifier using a primary biasing circuit, the primary biasing circuit configured to use the correction current to correct for a variation in gain of the power amplifier when the power amplifier is enabled.

[redacted]

301. Ishimaru discloses this limitation for the same reasons as discussed with respect to limitation [1.2.3].

302. Therefore, it is my opinion that Ishimaru anticipates Claim 17.

Claim 18

[18] The method of claim 17 wherein shaping the enable signal includes using a resistor-capacitor (RC) network of the time-dependent signal generator.

303. Ishimaru discloses this limitation for the same reasons as discussed with respect to Claim 2.

304. Therefore, it is my opinion that Ishimaru anticipates Claim 18.

Claim 21

[21.0] A bias circuit for biasing a power amplifier, the bias circuit comprising:

305. To the extent that the preamble is limiting, Ishimaru discloses a bias circuit (light blue) as illustrated in Figure 1, as discussed in limitation [1.2].

[21.1] a time-dependent signal generator configured to shape an enable signal of the power amplifier to generate a control current;

306. Ishimaru discloses this limitation for the same reasons as discussed with respect to limitation [1.2.1].

[21.2] a current amplifier configured to amplify the control current to generate a correction current, the current amplifier including a current mirror; and

307. Ishimaru discloses this limitation for the same reasons as discussed with respect to limitations [1.2.2] and [1.2.4].

[21.3] a primary biasing block configured to generate a bias current for the power amplifier based at least partly on the correction current, the

[redacted]

bias current configured to correct for a variation in gain of the power amplifier when the power amplifier is enabled.

308. Ishimaru discloses this limitation for the same reasons as discussed with respect to limitation [1.2.3].

309. Therefore, it is my opinion that Ishimaru anticipates Claim 21.

Claim 22

[22] The bias circuit of claim 21 wherein the time-dependent signal generator includes a resistor-capacitor (RC) network.

310. Ishimaru discloses this limitation for the same reasons as discussed with respect to Claim 2.

311. Therefore, it is my opinion that Ishimaru anticipates Claim 22.

312. To the extent that Complainants argue that any limitation of Claims 1-2, 10-11, 17-18, and 21-22 that I have discussed above is not disclosed by Ishimaru, it is my opinion that Ishimaru renders the claims above obvious in view of the general knowledge in the art.

2. Claims 1-2, 10-11, 17-18, and 20-22 are Obvious over Ishimaru in View of Harrison

313. For this Section, I incorporate my opinions in §IX.E.1 above as to how Ishimaru discloses each limitation of the Asserted Claims. However, to the extent it is argued that Ishimaru does not expressly disclose or render obvious a *current mirror*, Ishimaru in view Harrison discloses this limitation.

Claim 1

314. For all the limitations of Claim 1, I incorporate my opinions from §IX.E.1 ([1]) above as to how Ishimaru discloses each limitation of Claim 1.

315. To the extent it is argued that Ishimaru does not expressly disclose or render obvious a *current mirror*, Ishimaru in view Harrison discloses this limitation, as I explain below.

[redacted]

[1.2.4] the current amplifier including a current mirror.

316. Ishimaru in view of Harrison discloses this limitation for the same reasons as discussed with respect to limitation [14.2.2.1] of the '563 Patent. I incorporate my opinions from §IX.D.2 ([1]) above related to the '563 Patent as to how Ishimaru in view of Harrison renders Claim 1 obvious. It is my opinion that a POSITA would have been highly motivated to combine Ishimaru's teaching of a bias circuit for a PA with Harrison's disclosure of a basic current mirror and have a reasonable expectation of success for at least the reasons set out in §IX.D.2 ([1]) above.

Claim 17

317. For all the limitations of Claim 17, I incorporate my opinions from Section §IX.E.1 ([17]) above as to how Ishimaru discloses each limitation of Claim 17.

318. To the extent it is argued that Ishimaru does not expressly disclose or render obvious a *current mirror*, Ishimaru in view Harrison discloses this limitation, as I explain below.

[17.2] amplifying the control current using a current mirror of a current amplifier to generate a correction current; and

319. Ishimaru in view of Harrison discloses this limitation for the same reasons as discussed with respect to limitation [1.2.4]. I incorporate my opinions from §IX.D.2 above where I explain how Harrison discloses a *current mirror* and why a POSITA would have been motivated to combine Harrison's teachings with Ishimaru.

320. Thus, for the above reasons, Ishimaru in view of Harrison renders obvious Claim 17.

Claim 21

321. For all the limitations of Claim 21, I incorporate my opinions from Section §IX.E.1 ([21]) above as to how Ishimaru discloses each limitation of Claim 21.

[redacted]

322. To the extent it is argued that Ishimaru does not expressly disclose or render obvious a *current mirror*, Ishimaru in view Harrison discloses this limitation, as I explain below.

> ***[21.2] a current amplifier configured to amplify the control current to generate a correction current, the current amplifier including a current mirror; and***

323. Ishimaru in view of Harrison discloses this limitation for the same reasons as discussed with respect to limitation [1.2.4]. I incorporate my opinions from §IX.D.2 above where I explain how Harrison discloses a *current mirror* and why a POSITA would have been motivated to combine Harrison's teachings with Ishimaru.

324. Thus, for the above reasons, Ishimaru in view of Harrison renders obvious Claim 21.

Claims 2, 10-11, 18, 20 and 22.

325. I incorporate my opinions in §IX.E.1 ([2], [10]-[11], [18], [20], and [22]) *supra*, where I explain how Ishimaru discloses the limitations of Claims 2, 10-11, 18, and 22. I also incorporate my opinions in §IX.E.3 *infra*, where I explain how Ishimaru in view of the general knowledge of the art renders obvious Claim 20; and §IX.D.2 *supra*, where I explain why a POSITA would have been motivated to combine Harrison's teachings with Ishimaru.

326. Thus, for the above reasons, Ishimaru in view of Harrison renders obvious Claims 2, 10-11, 18, 20 and 22.

3. Claim 20 is Obvious over Ishimaru in View of the General Knowledge in the Art

Claim 20

> ***[20]. The method of claim 17 wherein generating the bias current includes shaping the bias current so as to compensate for a gain variation of a heterojunction bipolar transistor (HBT).***

[redacted]

327. Ishimaru discloses this limitation for the reasons as discussed with respect to Claim 10 and limitation [1.2.3], and further in view of the general knowledge in the art concerning HBT transistors. *See* §VIII.C.3.

328. As discussed for Claim 10 and limitation [1.2.3], Ishimaru discloses shaping the bias current to compensate for a gain variation of the BJT used for its PA transistor 103 for radio communication devices. *See supra* Claim 10 and limitation [1.2.3]; Ishimaru ¶¶1, 54, 55*; see, e.g.*:

> Next, FIG. 3 shows an example (simulation result) of transient response of the operating current (collector current Ic3) of the amplifier transistor 103 in the power amplifier of this embodiment. In this embodiment, the current to be fed from the bias transistor 107 to the amplifier transistor 103 is forcedly increased at turn-on of the amplifier, with the result that the value of the operating current Ic3 comes to a steady state in about 1/4 the time of transient response of the comparative example of FIG. 2. Thus, occurrence of distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed, so that the linearity of the circuit in burst operation is improved. That is, gain variations due to collector current variations of the power amplifier using a bipolar transistor can be compensated.

Ishimaru ¶54.

329. A POSITA would understand Ishimaru's solution to apply to all types of BJT processes for PAs for such radio communications devices, of which heterojunction bipolar transistors (HBT) were a popular, market-leading form for RF PAs. *See* §VIII.C.3. As explained in the State of the Art, it was part of the general knowledge in the art to use the HBT form of BJT, as was widely done and well documented, for bipolar junction transistor implementations of RF PAs. §VIII.C.3. This is because HBTs were an improved form of BJTs, with well-documented advantages for RF power amplification, including, *e.g.*, having the robustness, speed, density, and linearity necessary for such circuits. §VIII.C.3.

[redacted]

330. While Ishimaru does not expressly refer to the use of HBTs, that is nonetheless understood by a POSITA for several reasons. First, Ishimaru expressly discloses a solution for RF PAs implemented as BJTs, and a POSITA would reasonably draw the inference that Ishimaru disclosed the use of its solution for the market leading forms of such BJTs, namely HBTs. §VIII.C.3. Indeed, it was conventional to use HBTs in the context of radio communication devices having RF PAs using BJT transistors like Ishimaru's.

331. Second, Ishimaru is directed to an incremental improvement in the startup behavior of BJT-based RF PAs that is directed at the margin of high performing devices, *i.e.*, the type of BJT-based RF PAs commonly implemented as HBTs. A POSITA understood that HBTs, as BJTs, suffer the same thermal effects described by Ishimaru, and would likewise benefit in the same way as other BJTs. For these reasons, while not explicitly stated, the HBT form claimed is nonetheless disclosed to a POSITA in view of the reasonable inferences that a skilled artisan would draw when reading Ishimaru.

332. To the extent it is argued that a POSITA would not have drawn the reasonable inference that Ishimaru's PA would employ BJTs using the market-leading HBT form, that would have at minimum been obvious to a POSITA in view of the general knowledge in the art, for the same reasons discussed above and evidenced by the well-known advantages of HBTs for RF PAs. §VIII.C.3. A POSITA would have been motivated to use an HBT for Ishimaru's BJT PA 103 to achieve any one of a host of known benefits such as their "improvement in the high frequency performance of the transistor" (Illingworth), their "inherently superior linearity and efficiency performance" (TriQuint), their "reliability [being] well known to be excellent" (TriQuint), and other advantages in cost, size, robustness, *etc.* (Johnson). §VIII.C.3. A POSITA would have been motivated to implement at least the PA of Ishimaru as an HBT following these

[redacted]

well-documented advantages. §VIII.C.3. Doing so would involve nothing more than using a market-leading prior art technique (using HBT type of BJT-based RF PAs) according to conventional wisdom for the benefits and successes confirmed by the market and reported by others. Finally, there would have been nothing technologically counterintuitive about implementing Ishimaru's PA system with an HBT as compared to other forms of a BJT. Indeed, the '101 Patent references HBTs in passing, without any special significance, criticality, challenges, or counterintuitive concepts or properties. '101 Patent 7:53-55*; see, e.g.*:

> In one implementation, the bipolar transistor 61 is a heterojunction bipolar transistor (HBT).

'101 Patent 7:53-55. This lack of detail is consistent with the well-developed state of the art for HBT RF PAs. §VIII.C.3. Furthermore, given Ishimaru's teachings, the selection of a market-leading BJT type (HBT) would have been viewed with a reasonable expectation of success with predictable benefits, all well within the skill of a POSITA as demonstrated by the popularity of HBTs in the marketplace. §VIII.C.3.

333. Therefore, it is my opinion that Claim 20 is rendered obvious by Ishimaru in view of the general knowledge in the art concerning HBT transistors.

4. Claim 20 is Obvious Over Ishimaru in View of Johnson

334. For this Section, I incorporate my opinions in §IX.E.3 *supra*, wherein I explain how Ishimaru in view of the general knowledge in the art discloses the limitations of Claim 20.

335. To the extent it is argued that a POSITA would not have found it obvious to implement Ishimaru's BJT using the market-leading HBT form, Johnson expressly discloses an HBT for PAs.

[redacted]

336. Johnson discloses SiGe HBTs had found "increasing use in wireless PA applications" due to "favorable thermal properties," "volume manufacturing capability," and "design automation support," which had all "long been recognized." Johnson at 1612.

337. Johnson discloses that the "favorable thermal properties, lower cost of wafer processing, and the higher integration capabilities" of such HBTs "make them a compelling choice for wireless applications" and provide a "very strong path for PA modules." Johnson 1612.

338. For the reasons discussed above in §IX.C.2 it is my opinion that a POSITA would have been motivated to modify Ishimaru with Johnson's teachings of an HBT for PA modules. Doing so would involve nothing more than using a market-leading prior art technique (using HBT for PAs) according to conventional wisdom for nothing more than the benefits reported and successful adoption of the technique by others.

339. Thus, for the above reasons, it is my opinion that Ishimaru in view of Johnson renders Claim 20 obvious.

5. Claim 20 is Obvious over Ishimaru in View of Harrison and Johnson

340. I incorporate my opinions in §IX.E.4 above where I explain how Ishimaru in view of Johnson discloses the limitations of Claim 20. I also incorporate my opinions in §IX.E.4 ([17]) above, where I explain how Ishimaru in view of Harrison discloses the limitations of Claim 17.

341. Thus, for the above reasons, it is my opinion that Ishimaru in view of Harrison and Johnson renders obvious Claim 20.

F. Rebuttal to Complainants' Interrogatory Responses Relating to the Invalidity of the Asserted Patents in view of the Prior Art

[redacted]

342. I have been provided with and reviewed Complainants' first and second supplemental responses to Interrogatory No. 7, dated February 19, 2025, and the material cited, which are directed to the invalidity of the Asserted Patents in view of the prior art.

343. Complainants' responses do not change my opinions for all the reasons that I have expressed above. I further address the primary arguments more specifically below. However, I note that many of Complainants' arguments in the responses are vague and written in a confusing manner. To the extent that Complainants articulate their arguments more clearly in an expert report or at trial, I reserve the right to further respond.

344. Complainants argue that Ishimaru's control voltage source 135 is not an "enable signal":

> Ishimaru's control voltage source 135 is, as its name suggests, a voltage source, such as a battery or a regulated voltage. Ishimaru consistently uses the term "source" for both control voltage source 135 and DC power source 137, using the same symbol ("⊣⊢"), and never refers to control voltage source 135 as an enable signal. As a voltage source, control voltage source 135 provides a fixed output and is not, for example, a signal sent from other circuit components indicating when to enable versus disable. As such, it is not a signal that enables. In particular, as shown in Fig. 1 and consistent with Ishimaru's description of its control voltage source, Ishimaru's control voltage source 135 is a power source for supplying power, via resistor 133 and transistor 107, for the bias current for amplifier transistor 103. Ishimaru at ¶¶24, 31, 52, Fig. 1. Notably, Ishimaru fails to disclose a signal that enables that is separate from the power source 135, and thus fails to disclose a signal that allows circuitry to be enabled or disabled while a power source still powers at least part of the circuitry.

Second Supplemental Response to Interrogatory No. 7 at 128

345. This argument is incorrect for all the reasons that I have stated above, where I explain why Ishimaru's voltage source 135 is an *enable signal*. Complainant's argument is not commensurate with any requirement in the claims. To the extent Complainant is advancing new claim construction arguments, I understand that is not proper. Nor is it warranted. Ishimaru discloses an enable signal under the plain and ordinary meaning of the claim terms. Further,

[redacted]

while not required by the claims, I explain that Ishimaru discloses two distinct power sources to serve distinct functions. The first power source, DC voltage 137, is connected to provide a constant DC power to amplification transistor 103. Ishimaru ¶42. The second power source, control voltage source 135 (*an enable signal*) at bias terminal 108, "controls turn-on and -off of power amplification." Ishimaru ¶24. *See* §IX.B.1 *supra.*

346. Further, Complainants rely on Harrison to argue that Ishimaru's transistor 119 is not a current mirror because it cannot "be configured to achieve a target gain." Specifically:

> Ishimaru's transistor 119 is incapable of mirroring or replicating a current. Instead, Ishimaru's transistor 119, as KCT admits, is "***poorly-controlled***" and is "constrained by the ***limited configurability of the β*** (amplification factor)". … The β (amplification factor) for a transistor such as Ishimaru's transistor 119 is specified in ranges ("e.g., 60 to 150 or more," or "up to 500"), because the level of amplification will vary during operation as operating conditions (e.g., the amount of current, the temperature) change, making the output current different from, rather than replicating, the input current. . . . In addition, aside from a lack of controllability during operation, Ishimaru's transistor 119 would have an unknown β value due to processing variations during manufacturing of the transistor 119. Because Ishimaru's transistor 119 is unable to consistently replicate a specific current, because the output can at best fall somewhere within a broad range, it is not "configured to mirror a current."

Second Supplemental Response to Interrogatory No. 7 at 132-33 (emphasis original).

347. I disagree with this argument for the reasons I expressed above in §IX.D and §IX.E. Complainant's arguments are not commensurate with the claims. Complainant appears to be arguing a quality metric that is not present in the claims, or the proposed constructions for current mirror. Further, Complainant appears to be mistaken as to the nature of any "admission". The quoted recitations about "poorly-controlled" and "limited configurability" is taken out of context. The quoted material is not referring to transistor 119 as it exists in Ishimaru's circuit. As I explained above, transistor 119 as connected in Ishimaru is a current mirror that is configured to achieve a target gain. That is, the gain of Ishimaru's transistor 119 is controlled by

[redacted]

designing the voltage and current biasing so that the transistor 119 operates with a desired gain that is within the range of transistor 119's β. Thus, contrary to Complainants' assertion, the gain of transistor 119, as connected in Ishimaru, is controlled to achieve a target gain.

348. Complainants further rely on Harrison to argue that "[b]ecause the gain and output of Ishimaru's transistor 119 is uncontrollable and thus not controlled, the input to transistor 119 is not a "control current." Second Supplemental Response to Interrogatory No. 7 at 134.

349. I disagree with this argument for the reasons I expressed above in Section §IX.D and §IX.E where I explain why the input to transistor 119 is a *control current*. Further, for the reasons I explained above, Complainants' argument is incorrect that the gain and output of Ishimaru's transistor 119 is "uncontrollable and thus not controlled." Again, as I explained, the gain of transistor 119 as connected in Ishimaru is controlled. *See supra* §IX.D and §IX.E.

350. Complainants also argue that there is no motivation to combine Harrison with Ishimaru. Second Supplemental Response to Interrogatory No. 7 at 138-140. I disagree for the reasons that I have already expressed above in §IX.D.2, where I explain in detail why a POSITA would be motivated to improve Ishimaru with Harrison's current mirror and how a POSITA would go about doing so. I further address Claimants' specific arguments below.

351. First, Claimants argue that there is no motivation to combine because:

> Adding Harrison's current mirror—even if it can precisely control the amount of amplification applied to the uncontrolled, unpredictable output of transistors 119 and 120—cannot undo or counteract the variable amplification of transistors 119 and 120, so will not provide for better, higher, or finer tuning or configurability of the amplification.

Second Supplemental Response to Interrogatory No. 7 at 138.

[redacted]

352. I disagree. The output of transistors 119 and 120 is not "uncontrolled, unpredictable" — nothing about the circuit design of Ishimaru would support that conclusion. As I explained above, a POSITA would be motivated to add Harrison's current mirror to Ishimaru's transistor 119 and 120 for a variety of reasons, including to achieve isolation, as well as granular, targeted levels of scaling or more fine-tuning in addition to the amplification and mirroring already provided by transistor 119. The reasoning of the motivation to combine is not undermined by Complainant's argument.

353. Second, Claimants argue:

> Ishimaru's use of an uncontrolled, unpredictable level of amplification that varies during operation is the exact opposite of and contrary to a level of amplification that is sufficiently controlled and precise to achieve a target gain and mirror a current, like that provided by a current mirror. As such, Ishimaru teaches away from the use of a current mirror for amplification, and a POSITA would not be motivated to add a current mirror to Ishimaru's circuit to provide amplification, as KCT contends.

Second Supplemental Response to Interrogatory No. 7 at 139.

354. I disagree with this argument. The amplification in Ishimaru is not "uncontrolled, unpredictable" that varies during operation — nothing about the circuit design of Ishimaru would support that conclusion. As I have previously explained, the gain of transistor 119, as implemented in Ishimaru's circuit, is controlled by designing the voltage and current biasing of transistor 119 to achieve a desired target. There is nothing in Ishimaru that disparages or otherwise teaches away from the use of a current mirror; that is not consistent with Ishimaru, which already uses a current mirror.

355. Third, Complainants argue:

> adding a current mirror to Ishimaru's circuit, as KCT proposes, is contrary to the purported benefit of and solution provided by Ishimaru's circuit, as Ishimaru solves its problem without controlling the bias current. Ishimaru explains that the prior art used temperature sensing to control the bias current to the amplifier transistor, but

[redacted]

> it proposes a simpler solution that eliminates temperature sensing altogether. Ishimaru at [0005]. Instead, Ishimaru suggests achieving its objectives by simply increasing the bias to the amplifier transistor. Ishimaru at [0007]-[0012]. Ishimaru emphasizes that its solution does not use any temperature sensing elements. Ishimaru at Abstract, [0007], [0024]. As such, Ishimaru teaches away from the use of a current mirror.

Second Supplemental Response to Interrogatory No. 7 at 139-140.

356. I disagree with this argument. This contention is particularly vague and ambiguous. The argument mischaracterizes Ishimaru. Ishimaru does not disparage or otherwise teach away from any and all temperature sensors. Ishimaru certainly does not disparage or otherwise teach away from temperature effects in a power amplifier and its primary biasing circuit. As I have previously explained, Ishimaru does control the bias current. Further, Complainants appear to be equating a current mirror with temperature sensing elements or misunderstands the operation of Ishimaru. As I explained above, a POSITA would have been motivated to use Harrison's current mirror in Ishimaru's circuit for many reasons (e.g., isolation, granularity and fine-tuning), which do not include use as a temperature sensing element.

357. Fourth, Complainants argue:

> the proposed combination requires adding at least two additional transistors (the transistors that form the alleged current mirror that KCT adds to Ishimaru). Generally, a POSITA would not be motivated to add more components to Ishimaru because doing so increases costs, complexity, and size. This is especially true for Ishimaru's circuit, which has no need for the level of control provided by a current mirror.

Second Supplemental Response to Interrogatory No. 7 at 140.

358. I disagree with this argument. The number of components required to add Harrison's current mirror is trivial relative to Ishimaru's circuit. As I have explained above, a POSITA would be motivated to improve Ishimaru with a current mirror, and adding the components to do so would be a routine undertaking. To the extent the additional components

[redacted]

would add any complexity and cost, those considerations would be outweighed by the benefits of a current mirror that I have previously discussed.

359. Fifth, Complainants also argue:

> there is no alleged deficiency or issue with operation of Ishimaru's circuit that would require the addition of the alleged current mirror that KCT seeks to add to Ishimaru. KCT has not shown that adding this alleged current mirror is a simple substitution of a known element for an existing element or that its alleged benefits would be known. Instead, KCT simply seeks to add an alleged current mirror to a functioning circuit in Ishimaru for no reason.

Second Supplemental Response to Interrogatory No. 7 at 140.

360. I disagree with this argument. I have previously explained the numerous reasons a POSITA would have been motivated to improve Ishimaru's circuit with Harrison's current mirror.

361. Finally, Complainants argue the following based on the prosecution history of the '101 Patent.

> Furthermore, under any reasonable construction or interpretation of the term "current mirror," Ishimaru's transistor 119 is not a "current mirror" at least because the file history of the '101 patent makes clear that a single transistor in not a "current mirror." '101 Patent File History, Non-final Office Action (August 2, 2013) at 3-4 (Examiner indicating subject matter "the current amplifier includes a current mirror" is allowable over cited reference U.S. Patent No. 7,869,775 to Alon *et al.* ("Alon") because Alon's alleged "current amplifier"—single transistor 204—is not a "current mirror").

Second Supplemental Response to Interrogatory No. 7 at 130-131.

362. I disagree. I have reviewed the Non-final Office Action and Alon. First, although the Examiner refers to a "current 207," Alon's written description does not refer to reference 207 as a current. Alon does not mention reference 207 at all. Although reference 207 does appear in Alon's Fig. 2, the reference is simply designating the gate terminal of FET 204. Similarly, the Examiner refers to a "correction current (206)." However, reference 206 also is not described as a current, but instead is described as a "drain terminal 206" or a "connection 206." Alon, 5:48-

[redacted]

53; 6:4-30. Second, neither the Examiner nor the Applicant referred to Alon's FET 204 as a current mirror. Third, the lack of discussion about current mirrors is not surprising because a POSITA would recognize that FETs, such as FET 204, do not mirror or replicate currents. A FET is a voltage-controlled device, not a current-controlled device. As such, any current that may be present at the FET's gate is erroneous, miniscule leakage current, not a control curren that is replicated at the FET's source. FETs thus are unlike BJTs (including the BJTs in the Asserted Patents) where the BJT's base current is mirrored by the collector current by the BJT's gain factor. Finally, nowhere in the office action or amendment, does the prosecution history make reference to or distinguish anything based on the number of transistors. Nowhere did the applicant (or the examiner) articulate a special meaning for a current mirror that would be inconsistent with the pain and ordinary meaning of current mirror, that I've used in this report, and reflected, for example, in Barrie Gilbert's treatise on BJT current mirrors.

X. SECONDARY CONSIDERATIONS OF NON-OBVIOUSNESS

363. As part of developing my opinion on the invalidity of the asserted claims of the '101 and '563 Patents I also considered so-called secondary considerations of non-obviousness. *See* Appendix D (law). To do that I have reviewed Skyworks' responses (original, First Supplemental, and Second Supplemental) to Interrogatory No. 8, which I understand asked Skyworks to detail the bases that support or otherwise relate to any secondary considerations of non-obviousness. I also reviewed the rough transcript of the deposition of one of the named inventions, Dr. Ping Li. Based on my review of Skyworks' responses to Interrogatory No. 8 I understand that Skyworks identified seven categories of evidence that it contends demonstrates the non-obviousness of the asserted claims of the '101 and '563 patents, *i.e.* (i) long-felt but

[redacted]

unresolved need; (ii) failure of others; (iii) unexpected results; (iv) teaching away by others; (v) praise by others; (vi) commercial success; and (vii) copying by competitors.

364. In general, in my view, the evidence Skyworks has cited in its responses to Interrogatory No. 8 does not have a clear connection (and in a number of cases no connection) to the purported inventions claimed in the '101 and '563 Patents. In some instances the evidence refers only obliquely to issues of PA lag at start-up. In others, the evidence makes clear that it is referring to a different solution to the PA start-up issue. In others, it is not clear what connection the evidence has to the purported inventions claimed in the '101 and '563 Patents. I note also that in a number of instances Skyworks' interrogatory responses speak in vague or conclusory terms, making it difficult to discern the basis for a number of the Skyworks' positions.[13]. The evidence Skyworks lists in its responses to Interrogatory No. 8 does not have a clear connection with purported inventions claimed in the '101 and '563 Patents, which I understand is necessary for such evidence to be relevant to questions of obviousness. *See* Appendix D (law). As a result, Skyworks' purported evidence of secondary considerations of non-obviousness does not change my opinion as to the obviousness of the asserted claims of the '101 and '563 Patents, as set forth above.

A. Long-Felt but Unsolved Need[14]

365. Skyworks' evidence of a purported long-felt but unsolved need consists of a few citations to the '101 Patent. *See* Fourth Supplemental R&O to KCT's First Set of Interrogatories

[13] For at least this reason, I reserve the right to reply to any and all secondary considerations should its expert provide opinions on this topic, including any such opinions in the rebuttal to this report.

[14] I reproduce the category descriptors used by Skyworks in its response to Interrogatory No. 8 for convenience and for ease of reference. Doing so is not a concession that such a condition is met or that the cited evidence supports such a conclusion.

[redacted]

at 158-59, 169-70 (citing '101 Patent at 1:31-33, 1:49-59, and 4:32-39). While the cited portions of '101 Patent state – generally – that there is a need for improved power amplifier systems, they do not support all of the details Skyworks discusses, *e.g.* "significant dynamic distortion occurred when the power amplifier was turned on' in Wi-Fi applications, "Wi-Fi" uses bits early in the transmission to properly interpret the data that follows," long-felt need for a power amplifier that could control distortion at the beginning of a data burst, a "distortion problem, including at the beginning of the transmission," etc. *See* Fourth Supplemental R&O to KCT's First Set of Interrogatories at 168-70. These additional concepts are not mentioned in the '101 or '563 Patents and are beyond their scope. *See generally* §VII (patents and claims directed to PA biasing structures). The '101 and '563 Patents do not address concepts like transmission preambles/the beginning of data bursts. I note that Skyworks does not appear to offer any evidence outside of the '101 Patent to support its positions with regard to its characterization of either the supposed long-felt but unsolved need or the problem the '101 and '563 Patents purportedly solved. Fourth Supplemental R&O to KCT's First Set of Interrogatories at 158-159, 168-70. [redacted]

366. Moreover, the problem identified by the '101/'563 Patents (PA lag at start-up) was known before the '101/'563 Patents, as were various solutions. By way of example, U.S. Patent No. 8,260,224 – filed on December 2, 2009 – noted that "[a]lthough various fluctuations in physical characteristics caused by changing operating conditions can affect the gain or phase response of the PA, the temperature of the PA has a profound affect on its response" and that EVM – a type of distortion – can increase under "pulsed conditions." *See* KCT-ITC_0173887-0173902 (US 8,260,224) ("'224 Patent") 1:56-65; *see also id.* 1:60-2:11. The '224 Patent went

[redacted]

on to note some known solutions. The first was waiting until the PA is thermally stable. *See id.* 2:12-26. The '224 Patent further described a "second common approach is to speed up the gain and phase response of the PA by applying an external resistor and speed-up capacitor to provide more forward current earlier to the PA." *Id.* That is, the '224 Patent describes using a resistor-capacitor ("RC") network to provide additional current to the PA to compensate for the lag of the PA as it first turns on. Ishimaru also disclosed using an RC network to "speedup" the gain response at turn on. *See* §IX.B.1 *supra*. Furthermore, the '224 Patent itself discloses yet another solution: using a "preheat" bias signal to cause the PA to approach a steady-state level of operation prior to receipt of the RF signal. *See, e.g.,* '224 Patent 2:56-4:47. Thus, in my opinion, Skyworks has not established that there was a long-felt but unsolved need (*i.e.* to "control distortion at the beginning of a data burst") as set forth in Skyworks' responses to Interrogatory No. 8.

367. I note that Skyworks makes assertions such as "there was a long-felt need for a power amplifier that could control distortion at the beginning of a data burst" and that "Skyworks invented and reduced to practice a power amplifier that could address this distortion problem" and that the purported inventions of the '101 and '563 Patents "contributed to these products' performance, including their high linear output power, such as by improving their power amplifiers' dynamic error vector magnitude (EVM)." Fourth Supplemental R&O to KCT's First Set of Interrogatories at 169-70, 173. To the extent Skyworks contends that the '101 and '563 Patents as being directed to more general PA performance improvements, namely EVM I note that EVM is reference only in the specification of the '101 and '563 Patents, but the claims make no mention of EVM. *E.g.,* '101 Patent 4:39-43.

[redacted]

368. Regardless, to the extent Skyworks characterizes the '101 and '563 Patents as the first solution to the issue of distortion caused by dynamic EVM,, this is incorrect for other reasons. For starters, Ishimaru itself already explained and addressed the "dynamic EVM." *E.g.* Ishimaru at ¶ 33 ("According to the power amplifier of this embodiment, deterioration of the linearity due to the variations of amplification gain can be canceled so that the value of dynamic EVM (error vector magnitude can be improved)"). Furthermore two papers by S. Yoon provide further evidence that temperature related effects on EVM were known in the art and others had already published the thermal behavior of PAs, including the relationship to dynamic EVM, and described solutions for correcting or mitigating the thermal effects of the PA to address dynamic EVM.

369. The first paper (Yoon 2009) summarized the dynamic EVM phenomenon, and summarized yet another prior art solution to address it:

> This letter **presents a high performance 2.4 GHz two-stage power amplifier (PA)** operating in the temperature range from -30°C to +85°C for IEEE 802.11g, wireless local area network application. It is implemented in InGaP/GaAs hetero-junction bipolar transistor technology and **has a bias circuit employing a temperature compensation technique for error vector magnitude (EVM) performance. The technique uses a resistor made with a base layer of HBT. The design improves EVM performance** in cold temperatures **by increasing current**. The **implemented PA has a dynamic EVM of less than 4%,** a gain of over 26 dB, and a current less than 130 mA below the output power of 19 dBm across the temperature range from -30oC to +85°C.

Yoon 2009 Abstract. The paper describes static vs dynamic EVM, explains relationships between dynamic EVM and WiFi PA pulsing as part of time-domain duplexing (TDD):

> EVM measured with a PA continuously turned on is called a static EVM. A dynamic EVM is measured by turning on a PA when the signal is applied to the input of a PA. Interestingly, the dynamic EVM is worse than the static EVM [3]. WLAN applications use a same frequency band for a transmitter (Tx) and a receiver (Rx). Hence, WLAN systems need a switch to perform time domain duplexing (TDD). When a signal is being received through an Rx, it is obviously

more efficient if the Tx is off. For this reason, the dynamic EVM should be monitored rather than the static EVM.

Yoon 2009 601. The paper proposed a thermal solution for naturally/inherently increasing bias current to the base of the power amplifying transistor by putting a temperature sensitive resistor (R_{TC}) in the bias circuit, as shown in the right hand portion of the figure below:

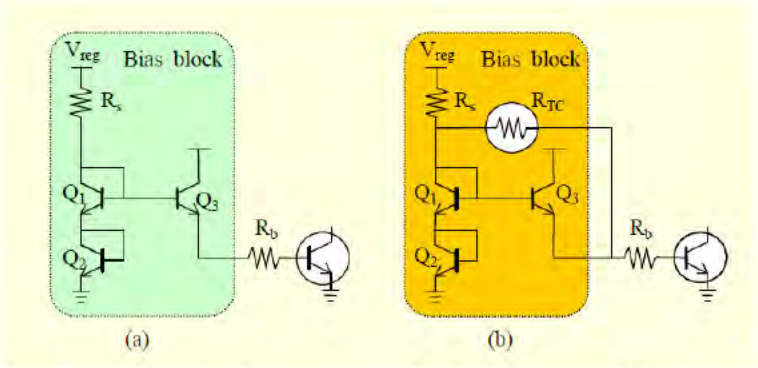


Fig. 2. (a) Common bias circuit and (b) the proposed bias circuit with temperature compensation resistor.

Yoon 2009 Fig. 2. *See also id.* 602.

370. The Yoon 2009 paper also makes reference (at 601) to an earlier paper by the same author, which I refer to as Yoon 2007, and discuss below.

371. Yoon 2007 also has a detailed explanation of dynamic EVM, modeling the thermal impact at each startup/enablement of a pulsed PA, and concludes by describing the flattening of dynamic EVM by adding a R-C network to the PA circuit:

[redacted]

Abstract—**This paper presents error vector magnitude (EVM) behavior under two different modes of a reference voltage ($V_{\rm ref}$); one is a static EVM with a constant $V_{\rm ref}$ and the other is a dynamic EVM with a pulsed $V_{\rm ref}$. A 2.4-GHz two-stage power amplifier (PA) is implemented by GaAs HBT technology to investigate EVM behavior for IEEE 802.11 g wireless local area network application. A square wave pulse with the duty cycle of 50% is applied as $V_{\rm ref}$ for dynamic operation mode.**

In this paper, it is shown that a dynamic EVM is worse than a static EVM because a transient response of PA output distorts preamble and SIGNAL **in orthogonal frequency division multiplexing signal bursts. This transient response is explained by a two-pole thermal network in this study, and transient response experiments with a resistor–capacitor (R–C) network at a power supply were performed for verification.**

Yoon 2007 Abstract. The paper described why dynamic EVM was pertinent to the TDD nature of Wi-Fi/WLAN. Yoon 2007 643.

372. Yoon 2007 provided plots of the thermal startup phenomenon of a power amplifying transistor:

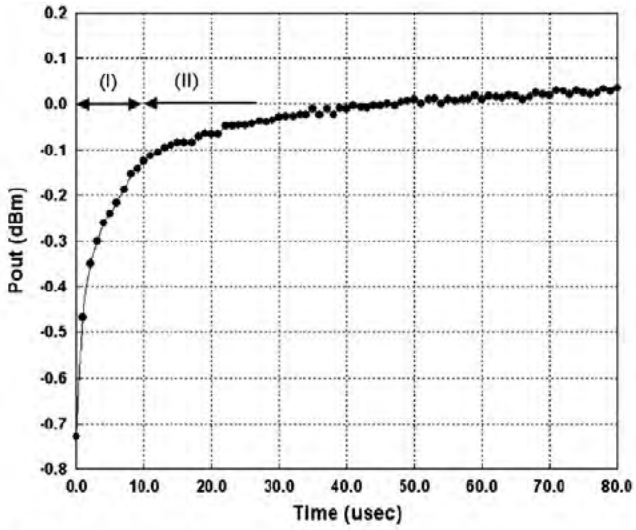


Fig. 4. Measured transient response of PA output with single-tone frequency of 2.4 GHz.

Yoon 2007 Fig. 4; *see also id.* 643-644.

373. Yoon 2007 explains the impact on dynamic EVM, with the startup timing and phenomenon of the PA being modeled by the thermal resistance and capacitance of the PA. Yoon 2007 at 645-646. The paper describes "When a PA is turned on, it takes time for the

power device to reach steady state, presenting a maximum output power level. It is called a thermal time constant, and is expressed by [equation in image below"

$$\tau_{\text{thermal}} = R_{\text{th}} \cdot C_{\text{th}}. \qquad (2)$$

Yoon 2007 646.

374. Yoon 2007 then discusses adding an "R-C network" to "present a flatter transient response". Yoon 2007 646. Figure 9 shows the added R-C network:

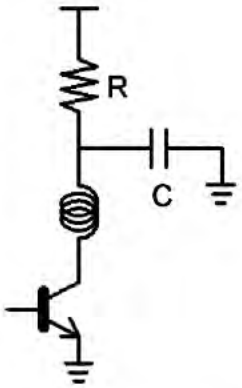
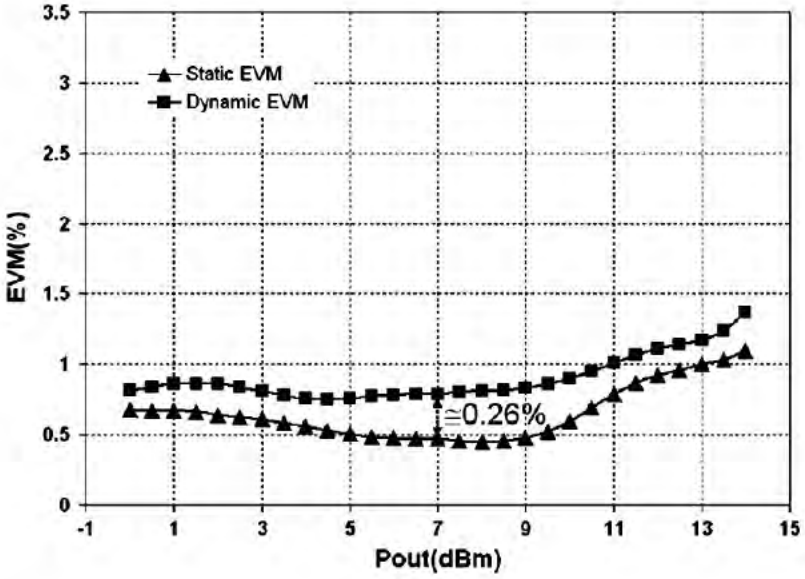


Fig. 9. *R–C* network at power supply to change flatness of transient response.

Yoon 2007 Fig. 9; *see also id.* 645-646.

[redacted]



(b)

Fig. 11. EVM behavior with: (a) 5.6- and (b) 10-Ω resistors at *R–C* network.

Yoon 2007 Fig. 11(b); *see also id.* 646. The figure above is described as showing flattening by the addition of the Figure 9 R-C network.

375. These papers, Yoon 2007 and Yoon 2009, not only provide further evidence supporting my opinion that the startup thermal phenomenon of a power amplifying transistor was already known in the prior art, but they also provide evidence of other solutions to the dynamic EVM issue, including adapting the bias circuit of the PA with a thermal solution (adding a special resistor per Yoon 2009), or adding a R-C network (per Yoon 2007).

376. [redacted]

[redacted] Accordingly, I disagree that at the time of the '101 and '563 Patents there existed a long-felt but unsolved need to address either dynamic EVM or, more generally, the PA start-up lag phenomenon.

B. Failure of Others

377. With regard to a purported "failure of others" Skyworks cites primarily on its own publications (*e.g.* white papers) and from these documents draws the conclusion that "none of those [other Wi-Fi FEM companies] had implemented the technology claimed in the '101 and '563 Patents." Fourth Supplemental R&O to KCT's First Set of Interrogatories at 170. As an initial matter, it is not clear to me how statements about Skyworks leads to a conclusion that others had tried and failed to implement a solution to the PA start-up lag issue. [redacted] However, Skyworks does not draw a connection to whatever market success/position Skyworks may have enjoyed to the purported inventions claimed in the '101 and '563 Patents. Consistent with this, the passage Skyworks quotes from refers to "materials," not particular PA biasing circuits. *See* Fourth Supplemental R&O to KCT's First Set of Interrogatories at 170 (quoting from Skyworks_ITC_000018682). Even assuming there was a discussion of particular PA biasing circuits, the passages suggest that Skyworks was on par with other RF chip manufacturers. *See* Skyworks_ITC_000018682 at Skyworks_ITC_000018689 ("We don't see Qualcomm's RF360 dominating the RF space, especially since silicon has traditionally

[redacted]

offered subpar performance relative to other materials used by Skyworks ***and others***, and phone makers have the opportunity to use other RF solutions alongside of RF360's.") (emphasis added).

378. [redacted]

[redacted]

Neither this, nor the circuits disclosed in the other cited documents discloses the specific circuit disclosed in the '101 or '563 Patents nor does Skyworks provide any mapping of those circuits that are disclosed to the claimed inventions of the '101 and '563 Patents. *See* Fourth Supplemental R&O to KCT's First Set of Interrogatories at 170 (citing Skyworks_ITC_000019815-818; Skyworks_ITC_000019819-822; Skyworks_ITC_000019823-826; Skyworks_ITC_000019827-830; Skyworks_ITC_000019831-840; Skyworks_ITC_000019873-876; Skyworks_ITC_000019877-880). [redacted]

[redacted] Thus, to the extent Skyworks contends the cited documents evidence recognition of Skyworks' PA technology, it appears to be for technology outside of the '101/'563 Patents. [redacted] Here again though, it is my opinion that this cited evidence does not indicate that others tried, and failed, at either implementing the claimed inventions of the '101 and '563 Patents or, more generally, solving the PA start-up lag issue. Indeed, as set forth with regard to "Long-felt but Unsolved Need," others had already found solutions to this same issue.

C. Unexpected Results and Teaching Away

379. As evidence that its solution produced an unexpected result and that other references taught away from it, Skyworks points to a two references: Gray et al., Analysis and Design of Analog Integrated Circuits, Fifth Edition (2009) (Gray II) and the RFMD application note. Skyworks contends that the claimed inventions of the '101 and '563 Patents was "counterintuitive to the prevailing teachings at the time," including Gray II and the RFMD application note. As to Gray II, Skyworks points to a page taken from a section related to Op Amps titled "Improving Slew-Rate in MOS Op Amps." *See* Fourth Supplemental R&O to KCT's First Set of Interrogatories at 159-60 (citing Gray II at 689). Op-Amps are quite different than PA's, in a number of respects. A power amplifier is designed to maximize output power and efficiency. An Op-Amp (operational amplifier) is designed to be used as a multi-purpose amplifier for small signal (low power) often used to do circuit operations, such as a summarion or differential measurement, or to amplify very small signals. To the extent Skyworks is relying on this portion of Gray II to support conclusions as to biasing of PAs I disagree that it is relevant.

[redacted]

Furthermore, the portion Skyworks cites to is focused on steady-state operation, not issues concerning an initial "start-up" phase, as is the '101 and '563 Patents. Similarly, the portion of Gray II Skyworks cites to is silent as to any temperature-based effects, as is the '101 and '563 Patents. Put differently, the portion of Gray II Skyworks cites to is not directed to the same component as the '101 and '563 Patents, let alone the same issue/problem.[15] For at least these reasons Gray II does not "teach away" from the claimed inventions of the '101 and '563 Patents, nor does Gray II indicate that the results were unexpected.

380. As to the RFMD application note, I note here that Skyworks generally cites to the entirety of the application note, rather than any specific page. *See* Fourth Supplemental R&O to KCT's First Set of Interrogatories at 171-172. This leaves me to guess at which portion of this application note Skyworks is relying on to support its contention.[16] In general though, the RFMD application note is focused on steady-state operation of particular gain block amplifiers. *See generally* Skyworks_ITC_000110940-946. The '101 and '563 Patents, in contrast, are focused on the initial PA start-up lag, a phenomenon that happens before the PA reaches steady-state operation. For that reason, the RFMD application note is focused on a different phase of operation, *i.e.* something different than what the '101 and '563 Patents are focused on. Thus, the RFMD application note does not "teach away" from the claimed inventions of the '101 and '563

[15] I note also that Skyworks later cites to a range of nearly 900 pages of Gray II, *i.e.* effectively all of Gray II. Fourth Supplemental R&O to KCT's First Set of Interrogatories at 171 ("*see generally* Skyworks_ITC_000018918-9814"). It is not feasible, nor efficient, for me to review all of Gray II to evaluate whether some, as-of-yet unidentified portion, somehow supports Skyworks' contention. If and when Skyworks points to a more specific portion, I reserve the right to address those arguments at that point.

[16] Here again, if and when Skyworks points to a more specific portion, I reserve the right to address those arguments at that point.

[redacted]

Patents. Nor does it indicate that the claimed inventions of the '101 and '563 Patents were unexpected.[17]

381. Furthermore, as set forth above, it was known in the art to use an RC circuits to boost the initial current to a PA to compensate for gain variation due to thermal effects of a PA. *See e.g.*, '224 Patent 1:56-2:26; *see also* §IX.B.2 (discussing Ichimaru). Current mirrors were similarly well-known in their operation and utility. §VIII.C.2. The '101 and '563 Patents use these known components in standard ways (*e.g.* to boost/"speed up" initial current to the PA, to mirror/amplify current etc.) to solve a known issue (PA start-up lag). There was nothing unexpected about how the '101 and '563 Patents deployed these components or the result they were intended to achieve.

D. Praise by Others

382. Skyworks' evidence includes a number of articles with statements generally supportive of Skyworks or discussing Skyworks' market position or generally discussing Skyworks' product offerings. *See* Fourth Supplemental R&O to KCT's First Set of Interrogatories at 172 (citing Skyworks_ITC_000018594; Skyworks_ITC_000018917; Skyworks_ITC_000018916; Skyworks_ITC_000018682; Skyworks_ITC_000018660; Skyworks_ITC_000018586; Skyworks_ITC_000018573; Skyworks_ITC_000018657. Having reviewed these documents I do not see any specific reference to the claimed inventions of the '101 and '563 Patents. Moreover, general statements about things like "linear band bias control" and "high efficiency PAs" do not translate into praise of the claimed inventions of the '101 and '563 Patents. For starters, "linear bias control" is identified as something distinct from a power

[redacted]

[redacted]

amplifier in Skyworks' own literature. *See* Skyworks_ITC_000018594. "Efficiency" of a PA is also something that is not necessarily related to the claimed inventions of the '101 and '563 Patents. Efficiency of a power amplifier can turn on things distinct from what Skyworks contends the '101 and '563 Patents are directed to (*e.g.* improvements on dynamic error vector magnitude, or error avoidance). Indeed, it is not clear whether the reference to the "high efficiency PA's" is praise of specific Skyworks products or rather statements about a general category of products. Put simply, the general statements of Skyworks success in the market place do not have a clear connection to the claimed inventions of the '101 and '563 Patents, *e.g.* purported improvements to the bias circuit for the PAs buried the transmit path that is itself a sub-circuit of the overall FEM. I say this not only because there are various components that make up a FEM and determine its performance (the PA being only one), but also that Skyworks sells (and has sold) a wide variety of non-FEM, non-PA components, making it hard (if not impossible) to draw a clear link between the overall performance of Skyworks as a company and the claimed inventions of the '101 and '563 Patents. The same is true for the award Skyworks cites to. *See* Skyworks_ITC_000018655.

383. The purported praise of Skyworks' domestic industry products faces similar issues.[18] For starters, I note that the two references Skyworks cites to are non-technical online articles that are broadly discussing macro-level features of the various products. *See generally* Skyworks_ITC_000110938, Skyworks_ITC_000110947. They are not attempting to review or analyze technical details such as particulars of a sub-circuit (PA biasing circuit) buried within a

[18] This assumes that Skyworks' domestic industry products do, in fact, practice one or more of the claimed inventions of the '101 or '563 Patents. I understand that is a disputed point between the parties. I reserve the right to provide my full opinions on that if/when asked and in accordance with the schedule.

[redacted]

component that is itself only one component of the PA. Furthermore, references to things like "high linear output power" do not translate into praise for the claimed inventions of the '101 and '563 Patents. As noted above, a FEM is comprised of various functional blocks, *e.g.* sub-components, typically a PA, a switch and LNA and a controller. Most active components in a circuit, *e.g.* transistors, introduce the prospect of creating non-linearities in the FEM's output. The PA is just one area where non-linearities can be introduced. A FEM's switch is another. The linearity of a FEM's output is thus determined by various factors, not merely the PA. [redacted]



[redacted]

E. Commercial Success

[redacted]

384. I begin by reiterating a point made previously. A FEM is comprised of various functional blocks, typically a PA, a switch, and LNA and a controller. While the '101 and '563 Patents are directed to purported improvements to a sub-circuit to the PA (*i.e.* the biasing circuit), the PA itself is just one of a number of components that make up the overall FEM. As noted above with regard to the purported praise by others, the overall performance of the FEM is the product of its constituent components working well and working together well. By way of example, a high-functioning PA would not translate into a high-functioning FEM if the switch performance was sub-par. And vice versa. Any number of factors go into determining the overall performance of the FEM; the PA is just one of them.[19] Given this, it is very hard (likely impossible) to attribute sales success of a FEM to the performance of any one portion of one component within that FEM.

385. With this in mind, I have reviewed the documents cited by Skyworks that it uses to conclude that Skyworks has "enjoyed significant commercial success as a result of the innovations in the '101 and '563 Patents." I do not draw the same conclusion based on the cited documents. For all the reasons stated in the preceding paragraph (and in relation to the "Praise by Others"), the overall sales of the FEMs that purportedly practice the '101 and '563 Patents are not, in my opinion, attributable to the claimed inventions of the '101 and '563 Patents. It does not appear Skyworks points to any documents that draw a link between the purported sales success of its products that allegedly practice the '101 and '563 Patents and the claimed invention of the '101 and '563 Patents. *See* Fourth Supplemental R&O to KCT's First Set of

[redacted]

[redacted]

Interrogatories at 173-74. [redacted]

[redacted]

386. The remaining evidence Skyworks cites discuss Skyworks' overall revenue and market share, without reference to any specific products, let alone particular features of those products. Here again, for the same reasons set for above (*e.g.* diversity of Skyworks' overall product portfolio), I do not agree that it is appropriate to draw a connection between Skyworks overall market success/position and the claimed inventions of the '101 and '563 Patents. A number of the documents though do make clear that Skyworks was a market leader and had a significant market share. Skyworks' overall revenue and market share (and, indeed, possibly also the revenue associated with the Skyworks products that purportedly practice the claimed inventions of the '101 and '563 Patents) could just as easily be attributed to Skyworks' established market position and visibility in the market as it could to the claimed inventions of the '101 and '563 Patents.

F. Copying

387. As an initial matter, it appears Skyworks assumes for purposes of secondary considerations of non-obviousness that various of KCT's products infringe the '101 and '563 Patents. *See* Fourth Supplemental R&O to KCT's First Set of Interrogatories at 175-76 (KCT's products "incorporate the inventions of the '101 and '563 patents, often in the exact manner that the inventions are described in the specifications of the '101 and '563 patents.") I understand that infringement is a disputed issue, with KCT denying that any of the products Skyworks has

[redacted]

accused infringe either the '101 and '563 patents. Suffice it to say that if KCT's products do not infringe the asserted claims of the '101 and '563 Patents, then there is no "copying."

[redacted]

[redacted]

do not have a basis on which to better evaluate that statement. If/when Skyworks is permitted to backfill that statement with evidence, I reserve the right to respond.

[redacted]

391. In sum, as stated above, based on what Skyworks has contended and the evidence it has currently pointed to, I do not see a clear connection between the claimed inventions of the '101 and '563 Patents and the various evidence Skyworks points to with regard to its supposed secondary considerations of non-obviousness.

XI. ENABLEMENT AND WRITTEN DESCRIPTION

392. In my opinion, Complainant's technical domestic industry ("Tech DI") contentions rely on an illogical, far-flung, and expansive claim scope that, if accepted, would render all of the Asserted Claims invalid for lack of enablement and written description.

393. First, it is my opinion that the Asserted Claims – if deemed to cover Skyworks' Tech DI theory – are invalid under the enablement requirement because the specification of the Asserted Patents fails to teach a POSITA how to make and use the full scope of the claimed invention without undue experimentation.

394. Second, it is my opinion that the Asserted Claims – if deemed to cover Skyworks' Tech DI theory – are invalid under the written description requirement because the specification

[redacted]

of the Asserted Patents fails to reasonably convey to a POSITA that the inventors had possession of the full scope of the claimed subject matter.

[redacted]

1. Claim Requirements

398. The '563 and '101 Asserted Claims all require biasing a power amplifier with a bias current/bias signal generated by a primary biasing circuit:

[redacted]

- "bias circuit configured to . . . generate a bias signal that biases the power amplifier [and having] "a primary bias circuit configured to generate the bias signal [that biases the power amplifier]." ('563 Claim 14)
- "a bias block for biasing the power amplifier, the bias block including . . . a primary biasing circuit configured to generate a bias current for the power amplifier." ('101 Claim 1)
- "A method of biasing a power amplifier, the method comprising: . . . generating a bias current for a power amplifier using a primary biasing circuit." ('101 Claim 17)
- "A bias circuit for biasing a power amplifier, the bias circuit comprising: . . . a primary biasing block configured to generate a bias current for the power amplifier." ('101 Claim 21)

399. Furthermore, under a stipulated construction of the "gain correction circuit . . . correction current" claim element, '543 Claim 14 requires "a circuit for gain *correction of the power amplifier*." *See* Parties' Joint Chart Setting Forth Parties' Post-Hearing Claim Construction (EDIS No. 842303) (Jan. 30, 2025), at 4 (emphasis added).

400. All of the remaining claims depend from one or more of the foregoing claims and therefore also have one or more of the above listed requirements. Furthermore, none of the dependent claims narrow the independent claims in a way that would cure the deficiency addressed in this section of my report. Thus, my opinions in this section apply to all '101 and '563 Asserted Claims.

[redacted]

[redacted]

[redacted]

404. As set out below, I analyzed the enablement requirement by considering the factors identified to me in the legal instruction provided by counsel:

Lack of Direction, Guidance and Working Examples in the Specification.

405. In forming my opinions as to whether undue experimentation would be needed to make and use the full scope of the claimed invention, I first considered the amount of direction

[redacted]

[redacted]

or guidance presented by the patent specification, as well as the presence or absence of working examples in the patent specification.

[redacted]

[redacted]

[redacted]

[redacted]

State of the Art, Predictability in the Art, and the Relative Skill at the Time of the Invention

[redacted]

[redacted]

419. In my opinion, these considerations also indicate that the level of experimentation would have been undue.

Breadth of the Claims, Nature of the Invention, and The Quantity of Experimentation Necessary to Realize the Full Scope of the Claims

420. In forming my opinions as to whether undue experimentation would be needed to make and use the full scope of the claimed invention, I also considered the breadth of the claims and nature of the invention.

[redacted]

[redacted]

[redacted]

[redacted] [redacted].

4. Detailed Analysis – Written Description

427. Per the law section above, I understand that the written description requirement requires supporting disclosure in the specification for the full scope of a claim.

428. I understand that the patentee's infringement allegations can be relevant to a written description analysis insofar as those allegations demonstrate the asserted scope of the claims.

[redacted] [redacted]

[redacted] [redacted]

[redacted]

[redacted]

[redacted].

5. Skywork's Responsive Contention Does Not Cure the Enablement and Written Description Failure.

[redacted]

[redacted]

> [redacted]

[redacted]

[redacted]

[redacted]

[redacted]

XII. RIGHT TO SUPPLEMENT AND USE DEMONSTRATIVES

439. I understand that before the hearing certain terms of the '563 and '101 Patents may be construed, which terms may have constructions that differ from those I have relied upon in this Report. Should the meaning of any claim term discussed in this Report be construed, I reserve the right to supplement my opinions accordingly.

440. I understand that I will have the opportunity to use demonstrative exhibits at the hearing to summarize and/or support my opinions. I have not yet begun to work on any such demonstrative exhibits, aside from those included in this Report, but I expressly reserve the right to do so. Any demonstrative exhibits will be disclosed to Skyworks by the deadlines and in the manner required by the International Trade Commission.

[redacted]



Executed on February 28, 2025

Dr. David Ricketts

CERTIFICATE OF SERVICE

I, Richard Hughes, hereby certify that on February 28, 2025, the foregoing **EXPERT REPORT OF DAVID RICKETTS REGARDING THE INVALIDITY OF U.S. PATENT NOS. 8,717,101 AND 9,917,563** was served upon the following parties as indicated:

Linda Chang, Esq. Office of Unfair Import Investigations U.S. International Trade Commission 500 E Street, S.W. Washington, DC 20436 Email: Linda.Chang@usitc.gov	☐ **Via hand delivery** ☐ **Via courier (FedEx)** ☐ **Via facsimile** ☐ **Via first class mail** ☒ **Via electronic mail** ☒ **Via Box**
Counsel for Complainants **Skyworks Solutions, Inc., Skyworks Solutions Canada, Inc., and Skyworks Global Pte. Ltd.** WILMER CUTLER PICKERING HALE AND DORR LLP James M Dowd (Lead) 350 s. Grand Ave., Suite 2400 Loas Angeles, CA 90071 Email: WHSkyworks-KCT1413servicelist@wilmerhale.com	☐ **Via hand delivery** ☐ **Via courier (FedEx)** ☐ **Via facsimile** ☐ **Via first class mail** ☒ **Via electronic mail**
Counsel for **D-Link Systems Inc. and D-Link Corporation** Ric Macchiaroli Pillsbury Winthrop Shaw Pittman LLP 7900 Tysons One Place, Suite 500 Tysons, VA 22102 DLINK-1413@pillsburylaw.com	☐ **Via hand delivery** ☐ **Via courier (FedEx)** ☐ **Via facsimile** ☐ **Via first class mail** ☒ **Via electronic mail**
Counsel for **Ruijie Networks Co., Ltd.** S. Alex Lasher Quinn Emanuel Urquhart & Sullivan, LLP 1300 I Street NW, Suite 900 Washington, DC 20005 alexlasher@quinnemanuel.com qeruijie@quinnemanuel.com	☐ **Via hand delivery** ☐ **Via courier (FedEx)** ☐ **Via facsimile** ☐ **Via first class mail** ☒ **Via electronic mail**

/s/ *Richard Hughes*
Richard Hughes
Duane Morris LLP
30 South 17th Street
Philadelphia, PA 19103
Telephone: 215.979.1000

Appendix A to Expert Report of David Ricketts Regarding the Invalidity of U.S. Patent Nos. 8,717,101 and 9,917,563

Dr. David S. Ricketts
Full Professor

I.B BRIEF RESUME

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1. Education background:

Ph.D., Electrical Engineering, 2006, Harvard University
M.Sc., Electrical Engineering, 1997, Worcester Polytechnic Institute
B.Sc., Electrical Engineering, 1995, Worcester Polytechnic Institute

2. Professional experience:

Full Professor, 2012 – present, Department of Electrical and Computer Engineering North Carolina State University, Raleigh, NC

Visiting Researcher (Research Scientist), 7/2012 – 8/2013, MTL-ECE Massachusetts Institute of Technology, Cambridge, MA

Visiting Associate Professor, 9/2012-12/2012, School of Engineering and Applied Science Harvard University, Cambridge, MA

Assistant Professor, 2006 – 2012, Department of Electrical and Computer Engineering Carnegie Mellon University, Pittsburgh, PA

Manager of New Product Development &Advanced System Engineering, 2001 – 2003, ON Semiconductor, East Greenwich, RI

Principal Consultant, 1999-2001, Renaissance Design, Inc., Warwick, RI

IC Technology Unit Manager, 1995-1999, American Power Conversion, Billerica, MA

3. Scholarly and creative activities:

Type	***Number***
Books	3
Book Chapters	2
Refereed Journal Article	52
Other Journal Article (submitted)	0
Conference Paper, Refereed	82
Conference Presentation, (no paper)	7
Patent (filed)	2
Academic Workshops Chaired	20
Research Presentations, Invited	66

4. Membership in professional organizations:

IEEE, 1997-present (senior member since 2015)

5. Scholarly and professional honors:

- 2022 Chancellors Innovation Fund
- 2021 William F. Lane Outstanding Teaching Award

- Best Paper Award, IEEE Asia-Pacific Microwave Conference 2016.
- IEEE Senior Member, 2015
- Certificate of Teaching Excellence, Derek Bok Center, Harvard University, 2013
- **NSF CAREER AWARD, 2011.**
- Wimmer Teaching Fellow, Carnegie Mellon University, 2009.
- George Tallman Ladd Research Award, Carnegie Mellon University, 2009.
- National Academy of Engineers Frontiers of Engineering Education Recipient, 2009.
- **DARPA Young Faculty Award, 2008.**
- McGraw Hill Yearbook of Science and Technology, 2008.

6. Professional service on campus:

Faculty Teaching Evaluation Committee (ECE Department) 2022-present
Faculty Search Committee (ECE Department) – Fall/Spring 2021/22 & 2019/20
Course Curricula Committee (ECE Department) - 2015-present
Faculty Search Committee (ECE Department) – Fall/Spring 2016/2017
Senior Design Director Search Committee (ECE Department) - 2014
Participated in Engineering Open House (ECE Department), 2014

7. Professional service off campus:

Advisor DARPA Commercialization Office - 2023-24
Topic Editor, IEEE JMW 2022-2023
Track Editor, IEEE T-MTT Oct 2019-2022
Chair, IEEE Chapter ACME (Joint chapter of Antennas and Propagation (AP), Electronic Packaging Society (EP), Microwave Theory and Techniques (MTT), and Electron Devices (ED) 2019-
Technical Committee **Chair** for IEEE T-MTT 9 Society 2020-2022
Technical Committee **Vice-chair** for IEEE T-MTT 7 Society 2015-2019
Technical Program **Chair**: Enabling Nanomanufacturing for Rapid Innovation, TRC/NSF Workshop, Aug. 2013
Technical Program Committee (member) – IEEE International Microwave Symposium 2014-;
Technical Program Committee IEEE BioWireless 2012-2015.
Session Chair - Nanotechnology, CMOS Emerging Technologies Conf., Banff, Canada 2009; NANO-DDS, Chemically-Synthesized, Biomimetic Systems and Biologically-Inspired Architectures Session, August 2011.

II.B. INSTRUCTIONAL DEVELOPMENT

Include innovations in courses and curricula**.**

Creation of a new STEM poral interactRF.org (supported by ONR research grant) to teach RF and microwave engineering. This portal supports national education workshops and a full semester online course using an e-learning platform.

ECE 592 Analog Laboratory (graduate). Introduced graduate version of ECE 426 to allow for more advanced hands-on projects.

ECE 426 Analog Laboratory. Re-booted a retired course with Dr. Besnoff (teaching professor). Developed 12 new lectures and an entirely new course project where students build a drone from scratch, making their own printed circuit boards and coding an Arduino for flight control

ECE 714 Advanced Analog IC Design (ADCs). CAF Completed S18. (NCSU) Fall 2015. Developing new course for advanced analog IC design. Includes ~ 35 online lectures, and 10 interactive labs/workshops for students to practice hands on design. Full course, including labs, are available online for the public.

ECE 424/524 – CAF completed S17- 492(592) Radio Systems Design: (NCSU) Spring 2014+. Developed new experiential undergraduate course in radio system design. Includes 34 online lectures, and 10 interactive labs/workshops for students to practice hands on design. Full course, including labs, are available online for the public.

ECE 592 Analog-to-digital Converters: (NCSU) Fall 2013. Developed new course for ADCs as part of ECS circuit's curriculum.

ES139/239 Innovation in Science and Technology (Harvard): Fall 2012. Co-developed new format, assignments and teaching materials for primarily undergraduate innovation course.

ECE 18-605/606 Innovation in Science and Technology (CMU): Fall 2009. Developed interdisciplinary course on innovation between ECE and CMU's Engineering Technology Innovation Management masters program.

ECE 18-513 RF Circuits and Antennas for Wireless Systems (CMU): Fall 2008. Co-developed w. D. Stancil a new capstone design course in RF circuits & antennas.

ECE 18-610 Fundamentals of Modern CMOS Devices (CMU): Spring 2008, Developed introductory graduate course in CMOS device physics.

ECE 18-310 Fundamentals of Semiconductor Devices (CMU): Spring 2007. Developed entirely new content for undergraduate device physics course.

II.C. MENTORING ACTIVITIES

Include undergraduate academic advising and assessments thereof, if applicable, graduate committees, postdoctoral advising, advising student organizations, special projects with students, and Department of Public Instruction assessments of supervising student teaching.

Currently, member of **___4__** PhD and **__0___**MS committees.

1. Participated in **___29_____** Masters/PhD graduate committees.
2. Advisor to **__6___** nonthesis MS students.

POST-DOCTORAL RESEARCHER SUPERVISION

1. Jordan Besnoff (F2020, now research Prof NCSU 2021-)
2. Morteza Abbasi (2013-2016, research Prof. NCSU, 2016-18)
3. Jordan Besnoff (2014, now at Oakridge National Labs)
4. Junfeng Xu (2013, now at SpaceX)
5. Mathew Trotter (2013, Disney Research)
6. Mathew Chabalko (2012, now at Disney Research)
7. Darmin Arumugum (2012, now at JPL)
8. Limin Cao (2010,2012)
9. Joshua Smith (2010-2012, now at NRL)
10. Shingo Tamaru (2008-2010, now at AIST, Japan)

GRADUATE STUDENT SUPERVISION NCSU

1. Prya Darshni (PhD Canddiate, 2026)
2. Hongtao Zhong (PhD Candidate, 2025)
3. Shian Su (PhD Candidate, 2025)
4. Joe Zhou (PhD Candiate 2023)
5. Karan Maru F20-S21 RA
6. Sriraj Kandala, Summer 2020 RA
7. Bhaumik Jain Summer-Fall 2020 RA
8. Matt Dwyer Summer-Fall 2020. RA
9. William Harris (PhD candidate, 2019)
10. Junyu Shen (PhD candidate, 2019)
11. Hangjin Liu (PhD Candidate, 2021)
12. You Zhou (PhD Candidate, 2021)
13. Deeksha Lal (PhD 2018)
14. Samyak Parakh (MS, 2018)
15. Rafael de Silva (PhD candidate, 2020)
16. Michael Aiken (MS 2017, PhD Candidate)
17. Viswanath Ramesh (Initial PhD work 2015-2016)

GRADUATE STUDENT SUPERVISION CMU

1. Emre Karagozler, PhD 2013
2. Wei Tai, PhD 2012
3. Darmin Arumugam, PhD 2012
4. Weihua Hu, PhD 2012
5. Chongzhe Li, MS 2012
6. Zacherias George, MS 2012
7. En Shi, MS 2010
8. Qianyu Liu, MS 2009

GRADUATE COMMITTEES

1. Yongduk Oh (PhD Candidate 2023)
2. Jaewoo Kim (MS 2021)
3. Sarah Colebaugh

4. Weifu Li (PhD Candidate 2019)
5. Kirti Bhanushali (PhD candidate 2018)
6. Weihu Wang (PhD candidate 2018)
7. Yunjia Zhu (MS candidate Textiles 2017)
8. Junan Zhu (PhD candidate 2016)
9. Yunjia Zhu (MS candidate 2016)
10. Anirban Sarkar, (PhD candidate 2016)
11. Sandeep Hari, (PhD candidate 2018)
12. Kevin Green (PhD candidate 2016)
13. Ying Yi Tang, PhD 2015 (CMU)
14. Mohammad Noman, PhD 2013 (CMU)
15. Erkan Alpman, PhD 2007 (CMU)

UNDERGRADUATE STUDENT SUPERVISION

1. Bryan Wilson – S24
2. Jason Apsell F22-
3. Zander Selleseth F-22-
4. Jonathan Weeks – S32-
5. Yiyang Ye – S23/Summer
6. Maya Clinton F22-S23 (MechE)
7. Cole Contos F22
8. Jason Abell F22-S23
9. Landon Calton F22
10. Frank di Lustro S21
11. Alan Davila Summer 2020
12. Casey Crouse Spring 2020-Summer 2020
13. Jacob Abramow Spring 2020
14. Jeremy Peterson Sprinf 2020-Summer 2020
15. Laura Walker Spring 2020
16. Ryan Hardy REU Spring 2020-Spring 2021
17. Matt Dywer Connor Walker REU Fall/Spring 2019
18. Matt Dwyer REU 2019 Summer.
19. Casey Crouse REU 2019 Summer.
20. Zack Miller, Felix Chamielec, Danny Krafft, Grason Humphrey, Sufian Ahmad (NCSU UG Senior Design: Qi Charger, 2019)
21. Matt Dwyer, S19 (NCSU, Undergrad Research)
22. Shakti Reddy, F18/S19 (NCSU, Undergrad Research)
23. Shane Reagan, Zach Cline, Daniel Robson, Andrew Cragg, (NCSU UG Senior Design: Pringles Radar 2017/18)
24. Christian Burke, F17/S18 (NCSU, Undergrad Research)
25. Bill Zhou (BSEE) Fall 2016 (NCSU, Undergrad Research)
26. Akshay Iyer, Stephen Kerr, William Stepp, Kirk Weston, (NCSU UG Senior Design: Magnetic Sports Tracking, 2015/16)
27. Shaunak Turaga (BSEE), Fall/Spring 2014/15 (NCSU, Undergrad Research)
28. Mathew Briley (BSEE), Fall/Spring 2014/15 (NCSU, Undergrad Research)
29. Adeola Salu (BS), Spring 2013 (Harvard, Independent Study)
30. Zackary Hamad (BS), Spring 2011 (Harvard, independent Study)
31. Andrew Hillenius (BS), Summer/Fall, 2011 (CMU, Independent Study)
32. Chongzhe Li (BS), Spring 2010 (CMU, Independent Study)

33. Christopher Heidelberger (BS), Summer 2009, (CMU) NSF REU
34. Yue Lu (BS), Summer 2007 (CMU Independent Study)

SPECIAL STUDENT ADVISING

1. Karan Maru, S20 (NCSU MSEE Research)
2. Bhaumik Jain, F19 (NCSU, MSEE Research)
3. Sriraj Kandala, F19 (NCSU, MSEE Research)
4. Sandesh Shanmukha, S19 (NCSU, MSEE Research)
5. Shubhankar Patwardham F17/S18/F18 (NCSU, Ind. Study)
6. Amrutha Anantha S18 (NCSU, Ind. Study)
7. David Philpott S2017 (NCSU, Ind. Study)
8. Shenoy Akshat S2017 (NCSU, Ind. Study)
9. Sayan Das Fall 2016 (NCSU, Ind. Study)
10. Rounak Lokare Spring 2016 (NCSU, Ind. Study)
11. Swaroop Mohapatra Spring 2016 (NCSU, Ind. Study)
12. Ganapati Pai Spring 2016 (NCSU, Ind. Study)
13. Mahmoud Metwally 2015 (NCSU, MS research)
14. Ashwin Thyagarajan Spring 2015 (NCSU Ind. Study)
15. Reza Chavoshisani 2015 (PhD – 1 year visiting scholar)
16. Abhishek Malhotra (MS), Spring/Summer, 2013 (NCSU, Independent Study)
17. Syed Saad (MS), Summer 2011 (CMU, Independent Study)
18. Brian Lee (MS), Summer 2011 (CMU, Independent Study)
19. Ashwath Krishnan (MS), Summer 2010 (CMU, Independent Study)
20. Akshat Gupta (MS), Fall 2009 (CMU, Independent Study)
21. Heer Ghandi (MS), Fall 2007 (CMU, Independent Study)

GRADUATE COMMITTEES: 2023 ones listed

Student name	Degree [defense]	Chair	Member	Comment
Shian Su	PhD	X		Qual S21
Hongtao Zhong	PhD	X		Qual S22

II.D. MASTER'S AND DOCTORAL THESES DIRECTED AND BEING DIRECTED Show numbers and dates in each category

I am actively directing the theses of **__2__**Ph.D. students and **__0__** Master with Thesis option (MST) students.
I have graduated **__8__**PhD and **__4__** MST students. I was the sole chair of **_5_**of the **_7_**PhD committees; I was the sole chair of **__4__** of the **__4__** MST committees.

Master's and Doctoral Theses Currently under direction

Student name	Degree	Committee Approved	POW Approved	Qualifying Review (date)	Preliminary Exam (date)	Notes
Shian Su	PhD			S21		RA
Hongtao Zhong	PhD			S21		RA

Doctoral Theses Directed

Student name	Degree [date]
Joe Zhou	May 2024
Carter Harris	May 2020
Junyu Shen	Aug 2019
Deeksha Lal	May 2019
Emre Karagozler	Jan 2013
Wei Tai	May 2012
Darmin Arumugam	Jan 2012
Weihua Hu	Aug 2012

Master's Directed

Student name	Degree [date]
Samyak Parakh	Dec. 2017
Fenglan Yang	May 2015
Chongzhe Li (CMU)	Dec. 2012
Zacherias George (CMU)	Aug 2005
En Shi (CMU)	May 2010
Qianyu Liu (CMU)	May 2009

III. SCHOLARSHIP

III.A. PUBLICATIONS, AWARDS, AND ED. BOARD/PROGRAM COMMITTEE

List items as applicable, e.g., original research articles and research review articles in peer-reviewed journals, refereed articles that are pedagogy or extension-related, research abstracts, books; interdisciplinary/multidisciplinary works; invited and contributed research presentations; appointments or election to study sections and editorial boards; creative or professional works; exhibitions; juried shows, honors; awards, fellowships, prizes, competitions, and other pertinent evidence.

BOOKS

1. Radio System Design, D. S. Ricketts, Igram Spark, 2015.
2. Electrical Solitons: Theory, Design and Applications, D. S. Ricketts and D. Ham, CRC Press, 2010.
3. The Designers Guide to Jitter in Ring Oscillators, J. A. McNeill and D. S. Ricketts, Springer Verlag, 2009.

BOOK CHAPTERS

1. D. S. Ricketts, Xiaofeng Li, and Donhee Ham, "Soliton Electronics," in Circuits for Emerging Technologies - CMOS and Beyond, CRC Press 2008.
2. X. Li, D. S. Ricketts, and D. Ham, "Solitons in electrical networks," McGraw-Hill 2008 Yearbook of Science and Technology, McGraw-Hill, 2008.

DISCUSSION PI'S WORK

1. Nature, News & Views article by Thomas H. Lee, "Electrical solitons come of age," Nature, vol. 440, 36-37, Mar. 2006.

JOURNAL PUBLICATIONS
Graduate student author; undergraduate author

1. J. Besnoff, H. Zhong, S. Su, R. Kaveti, N. Maiya, S. Krishna, N. Garland, A. Bandokar and D. S. Ricketts, " Sweat-powered, mm scale, continuous time sensor systems with Bluetooth Low Energy2 (BLE) Backscatter. *IEEE ACCESS*, accepted 2024.
2. W. C. Harris and D. S. Ricketts, "Maximum Gain Enhancement n Wireless Power Transfer using Anisotropic Metamaterials," Scientific Reports, Sci Rep 13, 7726 (2023). https://doi.org/10.1038/s41598-023-32415-9
3. J. Shen and D. S. Ricketts, "Compact W-Band "Swan Neck" Turnstile Junction Orthomode Transducer Implemented by 3-D Printing," in IEEE Transactions on Microwave Theory and Techniques, vol. 68, no. 8, pp. 3408-3417, Aug. 2020
4. **M. Dwyer** and D. S. Ricketts, "The North Carolina state university rabbit radar: Build a frequency-modulated continuous-wave radar in a day [application notes]," IEEE Microwave Magazine, vol. 21, no. 5, pp. 136–145, 2020..[**Invited]**
5. D. S. Ricketts, "A modern 16-qam digital radio you can design and build at home [application notes]," IEEE Microwave Magazine, vol. 21, no. 7,pp. 10–22, 2020.
6. **W. C. Harris**, D. D. Stancil, and David S. Ricketts, "Improved wireless power transfer efficiency with non-perfect lenses," Applied Physics Letters 114:14, April 2019.
7. D. S. Ricketts, E. Shi, X. Li, N. Sun, O.O.. Yildrim and D. Ham, "Electrical Solitons for Microwave Systems," IEEE Microwave Magazine, April 2019 [**Invited]**.

8. **J. Shen** and D. S. Ricketts, "Additive Manufacturing of Complex Millimeter-Wave Waveguides Structures Using Digital Light Processing," in IEEE Transactions on Microwave Theory and Techniques, vol. 67, no. 3, pp. 883-895, March 2019.
9. D. S. Ricketts, **J. Shen**, J. Dunn, “Expanding the Antenna Frontier With Antenna Synthesis and 3D Printing”, (Cover article), Microwave Engineering Europe, Sept. 2018.
10. **D. Lal**, A. M. A. Ali and D. S. Ricketts, "Analysis and Comparison of High-Resolution GS/s Samplers in Advanced BiCMOS and CMOS," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 5, pp. 532-536, May 2018.
11. J. Besnoff, M. Abbasi and D. S. Ricketts, "Ultrahigh-Data-Rate Communication and Efficient Wireless Power Transfer at 13.56 MHz," in IEEE Antennas and Wireless Propagation Letters, vol. 16, pp. 2634-2637, 2017.
12. M. Abbasi, B. Wang, S. Tamaru, H. Kubota, A. Fukushima and D. S. Ricketts, "Accurate De-Embedding and Measurement of Spin-Torque Oscillators," in IEEE Transactions on Magnetics, vol. 53, no. 11, pp. 1-4, Nov. 2017.
13. **V. Pasku** et al., "Magnetic Field-Based Positioning Systems," in IEEE Communications Surveys & Tutorials, vol. 19, no. 3, pp. 2003-2017, thirdquarter 2017.
14. W. Tai, M. Abbasi and D. S. Ricketts, “Analysis and design of high-power and efficient, millimeter-wave power amplifier systems using zero degree combiners,” IET J. of Electronics, pp. 1-11, Jul. 2017.
15. M. Chabalko, J. Besnoff, M. Laifenfeld and D. S. Ricketts, "Resonantly Coupled Wireless Power Transfer for Non-Stationary Loads With Application in Automotive Environments," in IEEE Transactions on Industrial Electronics, vol. 64, no. 1, pp. 91-103, Jan. 2017.
16. Abbasi M, Ricketts DS. A high-power, broadband 245-285 GHz balanced frequency doubler in 45 nm SOI CMOS Microwave and Optical Technology Letters. 58: 423-426, 2016.
17. **M. E. Karagozler**, S. C. Goldstein and D. S. Ricketts, "Scalable self-assembly process for the fabrication of sub-millimetre three-dimensional cylindrical tubes," in IET Micro & Nano Letters, vol. 11, no. 1, pp. 4-8, 1 2016.
18. M.Abbasi, D.S.Ricketts, “A 275 GHz-285 GHz Balanced Frequency Quadrupler in 45nm SOI CMOS,” Electronic Letters, vol.51, no.18, pp.1424-1426, Sept 2015.
19. J. Besnoff, M. Abbasi and D. S. Ricketts, "High Data-Rate Communication in Near-Field RFID and Wireless Power Using Higher Order Modulation," in IEEE Transactions on Microwave Theory and Techniques, vol. 64, no. 2, pp. 401-413, Feb. 2016.
20. J. Besnoff, M. Chabalko and D. S. Ricketts, "A Frequency-Selective Zero-Permeability Metamaterial Shield for Reduction of Near-Field Electromagnetic Energy," in IEEE Antennas and Wireless Propagation Letters, vol. 15, pp. 654-657, 2016.
21. M. J. Chabalko, J. Besnoff and D. S. Ricketts, "Magnetic Field Enhancement in Wireless Power With Metamaterials and Magnetic Resonant Couplers," in IEEE Antennas and Wireless Propagation Letters, vol. 15, pp. 452-455, 2016.
22. M. Chabalko and D. S. Ricketts, “Experimental characterization of Fabry-Perot resonances of magnetostatic volume waves in near-field metamaterials”, Applied Physics Letters, 106, 062401 (2015).
23. **Ozcan, O.; Weihua Hu**; Sitti, M.; Bain, J.; Ricketts, D.S., "Investigation of tip current and normal force measured simultaneously during local oxidation of titanium using dual-mode scanning probe microscopy," Micro & Nano Letters, IET , vol.9, no.5, pp.332,336, May 2014
24. Ricketts, D.S.; Chabalko, M.; **Hillenius, A**., "Tri-Loop Impedance and Frequency Matching With High- Q Resonators in Wireless Power Transfer,"Antennas and Wireless Propagation Letters, IEEE , vol.13, no., pp.341,344, Jan. 2014.
25. **D. Arumugam**, J. Griffin, D. Stancil and D. S. Ricketts, “Three-Dimensional Position and Orientation Measurements using Magnetoquasistatic Fields and Complex Image Theory,” Antennas and Propagation Magazine, IEEE, vol.56, no.1, pp.160,173, Feb. 2014
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Graduate student author; undergraduate author

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INVITED CONFERENCE PRESENTATIONS (WITHOUT PAPERS)
Graduate student author; <u>undergraduate author</u>

1. D. S. Ricketts, W. Harris, J. Zhu, D. Baron, "Dynamic artificial surfaces for mm-wave imaging using photon induced plasmas in silicon lenses." DMI Online Workshop on Energy/Quantum/Metamaterials, Dec, 2020.
2. D. S. Ricketts, "Lessons from Build-a-Radio/Radar in a Day: The Ins and Outs of Experiential Design for Students," European Microwave Week, Teaching Microwave Engineering Special Session, Sept 2020.
3. M. Abbasi and D. S. Ricketts, "100 Gb/s All-electronic Radios: Opportunities and Challenges", GomacTech, Mar. 2014
4. **W. Tai, C. Li, Z. Li, G. Yahalom,** D.S. Ricketts, V. Stojanovic and J. Dawson, "A 45 GHz Asymmetric Multilevel Outphasing Transmitter in 45nm SOI CMOS," Student Research Int. Solid-State Circuits Conf, IEEE, Feb. 2012.
5. J.R. Smith, **W. Hu, Y.Y. Dang, O. Ozcan**, M. Sitti, J. Bain, R. Davis and D. S. Ricketts, "Writing Si nanowires on Si (100) with an STM tip: surface preparation and initial results," Materials Research Symposium, M11.50, Boston, MA, Nov. 2009
6. R. S. Friedman, M. C. McAlpine, D. S. Ricketts, D. Ham, C. M. Lieber, "Fully integrated high frequency nanowire ring oscillators," Materials Research Symposium, Mar. 2005.
7. D. S. Ricketts, "Current sensing and accuracy for CPU multi-phase DC-DC converters: the sub 20 mV challenge," IBM Power Delivery Symposium, 2002.

ACADEMIC WORKSHOPS and SHORT COURSES (Chair or Co-Chair)

1. RF and Electronic Warfare Workshop with NSA. Dec. 2023.
2. "Build a Foxhole Radio" International Microwave Symposium, San Diego, CA June, 2023
3. RF Engineering workshop, US Navay Academy, May 2023
4. RF Bootcamp in residence course, delivered at UT Dallas in collaboration with Texas Analog Center of Excellence. May 2023.
5. 12th Tom Brazil Doctoral School of microwaves "Build a Frequency Modulated Continuous Wave Radar in 1-day" IEEE European Microwave Week, Milan, Italy, Sept 2022.
6. 11th Tom Brazil Doctoral School of microwaves "Build a modern digital radio" IEEE European Microwave Week, London, UK, June 2021.
7. "Build a NIST Atomic Clock Radio" International Microwave Symposium, Denver, Co June, 2022.
8. 5th European Micwoave Student and Doctoral School: "Build a Frequency Modulated Continuous Wave Radar in 1-day" IEEE European Microwave Week, Utrecht, NL 2020 (virtual).
9. Frequency-Modulated Continuous Wave Radar in 1-day", European Microwave, Utrecht, NL, 2020.
10. "4th European Microwave Student and Doctoral Schools: Build a modern digital radio," IEEE ," IEEE European Microwave Week, Paris, France, Oct 2019.
11. "Build a 950 MHz radar in a day," IEEE Int. Microwave Symposium, Boston, MA, June 2019.
12. "Design, Fab and Test Your Own Microwave Component," Industry Workshop, IEEE Int. Microwave Symposium, Boston, MA, June 2019..
13. "From Bits to Waves: Building a Modern Digital Radio in 1 Day – Hand-on Workshop," IEEE Asia Pacific Microwave Conference, Kyoto, Japan, 2018.
14. "4th European Microwave Student and Doctoral Schools: Build a modern digital radio," IEEE ," IEEE European Microwave Week, Madrid, Spain, Sep 2017.
15. "Build a 16 QAM Radio – Student Design Competition," IEEE Int. Microwave Symposium, Philadelphia, PA, June 2018.
16. "Design, Fab and Test Your Own Microwave Component," Industry Workshop, IEEE Int. Microwave Symposium, Philadelphia, PA, June 2018.
17. "3rd European Microwave Student and Doctoral Schools: Build a modern digital radio," IEEE ," IEEE European Microwave Week, Nuremberg, Germany, Oct 2017.
18. "Build a Modern Digital Radio in a day," Int. Microwave Symposium, Honolulu, HI, June 2017.
19. "From Bits to Waves: Building a Modern Digital Radio in 1 Day – Hand-on Workshop," IEEE Asia Pacific Microwave Conference, New Delhi, India, Nov 2016.
20. "From Bits to Waves: Building a Modern Digital Radio in 1 Day – Hand-on Workshop," IEEE European Microwave Week, London, UK, Oct 2016.
21. "From Bits to Waves: Building a Modern Digital Radio in 1 Day – Hand-on Workshop," EDICON, Boston, MA, Sep. 2016.
22. "Emerging devices for Microwave Circuits and Systems," IEEE Int. Microwave Symposium, San Francisco CA,, May 2016.

23. "Build a Modern Digital Radio in a day," IEEE Int. Microwave Symposium, San Francisco, CA, May 2016.
24. "Build a Modern Digital Radio in a day," IEEE Radio Wireless Week, Austin, Texas, Jan, 2016.

INVITED RESEARCH PRESENTATIONS, Universities and Industry

1. "From one to one million Volts," ECE Colloquim, NCSU Apr. 2024
2. "Live from Faraday's Lab": An Intuitive and Historical Perspective on Electromagnetism" IEEE MTT Webinar, May 2022.
3. "NCSU Rabbit Radar: Design, Simulation & Building your own Frequency Modulated Continuous Wave Radar at Home," IEEE MTT-S Virtual Lecture, Sept, 2020
4. "From Bits to Waves - Building a Modern Digital Radio," Cadence Live, August 2020.
5. "Data, Sensors and New Technologies for Smart Cities," RMIT, Melbourne Australia, Mar 2019.
6. "New Approaches to IoT in Smart Cities," Western Sydney University, Sydney, Australia, Mar 2019.
7. "Enhancing, Shaping and Steering WPT Fields," WPT NSF ERC Industry Workshop, Alexandria, VA, Dec 2018.
8. "High-speed GaN RF DC-DC Converter design," Power America Webinar, NCSU, Oct. 2018.
9. "High-speed Communication & Field Enhancement Using Artificial Materials," Pennsylvania State University, Oct 2018.
10. "Modern Digital Radios," EuMW Microapp Lecture, Madrid Sept. 2018.
11. "Sensors and Networks for Smart Cities," City of San Diego, CA, Apr 2018.
12. "Emerging Technologies in Sensors for Smart Cities," Facebook, Dublin, Feb 2018.
13. "Science in Microwaves," NSF Workshop at IMS2017, June 2017.
14. "Magic with Magnetic Fields: NFL Football Tracking", Raleigh Engineers Club, Raleigh, NC, June 2017.
15. "Maximum power and phase noise in spin-torque oscillators," AIST Dec 2016.
16. "High-power, broadband multipliers for high-speed microscale radios," IEEE IMS invited workshop presentation, May 2016.
17. "Advances in wireless power transfer research: challenges and opportunities," General Motors, Feb. 2016.
18. "Magic with magnetic fields: NFL football tracking and advances in wireless power transfer & communication," Univ. of Washington, Feb, 2015.
19. "State of the art and future of high-speed wireless transceivers: Opportunities and challenges for near-THz communication," CMOS Emerging Technologies Conference, **Plenary, Invited**, May 2015.
20. "Advances in wireless power transfer research from academia: Challenges and opportunities," Wireless Power Summit, **Invited**, Berkeley, CA, Nov 2014.
21. "Advances in high-speed integrated and nanoelectronics," AIST Nov 2014.
22. "Watt-level, Highly Efficient, Fully Integrated all-Silicon Linear Power Amplification for mm-Wave Radar and Communications," Berkeley Nov. 2014.
23. "High-speed integrated circuits: From water waves to optical sampling," Analog Devices, Oct 2014.
24. "Advanced RF substrates: Applications in mm-wave electronics," DuPont 2014.
25. "Advanced mm-wave Circuits and Systems," Nuvotronics, 2014.
26. "Watt-level, Highly Efficient, Fully Integrated all-Silicon Linear Power Amplification for mm-Wave Radar and Communications," University of Delft, Netherlands, 2014
27. "Watt-level, Highly Efficient, Fully Integrated all-Silicon Linear Power Amplification for mm-Wave Radar and Communications," University of Pavia, Italy, 2014
28. "Magnetoquasistatics: Emerging Applications in Sports Visualization and Enhanced Wireless Power Transfer," University of Perugia, Italy, 2014
29. "Power, Sensing and Communication: Opportunities for a wireless world," General Motors Research, Herzlia Israel, Oct. 2013.
30. "Enabling Rapid Innovation in Nanomanufacturing," ENRI NSF workshop keynote, Napa, CA. Aug. 2013.
31. "Watt-level, Highly Efficient, Fully Integrated Linear Power Amplification for mm-Wave Radar and Communications," MIT, Boston Ma, May 2013.
32. "Watt-level, Highly Efficient, Fully Integrated Linear Power Amplification for mm-Wave Radar and Communications," Qualcomm, San Diego, CA, Jan 2013.
33. "Impedance Matched Magnetoquasistatic Wireless Power: On the equivalence of inductive and strongly coupled magnetic resonance and the challenges of multiple and mobile receivers" Qualcomm, San Diego, CA, Jan 2013.

34. RF from Kilometer to Millimeter Waves: NFL Football Tracking and High-power mm-Wave Circuits and Systems," POSTECH, Korea Aug 2012 (Distinguished Lecturer)
35. "Watt-level, Highly Efficient, Fully Integrated Linear Power Amplification for mm-Wave Radar and Communications," Jet Propulsion Laboratory, Pasadena, CA, Jul 2012.
36. "NFL Football Tracking, Microrobots and Nanoelectronics: Novel applications of Analog Circuits, E&M and MEMS," University of FL, Apr 2012.
37. "RF devices, circuits & systems: from nanometers to kilometers," University of Illinois, Urbana Champagne, Apr 2012.
38. "Applications of Analog Circuits and Electromagnetics in mm-wave RF and μRobots," NCSU Mar 2012.
39. "RF from Kilometer- to Millimeter-waves: NFL Football Tracking and Power Amplifier Circuits & Systems," UMich. Mar 2012.
40. "RF devices, circuits and systems: from nanometer to kilometer" University of Utah, Feb 2012
41. "NFL Football Tracking and Microrobots: Novel Applications of Analog Circuits, MEMS and E&M," Harvard University, Feb 2012
42. "RF devices, circuits and systems: from nanometer to kilometer," Duke Univ, Jan 2012
43. "At the boundaries of high-frequency analog & RF ICs: Speed, energy and uncertainty", Univ. NC State, NC, Dec 2011, (**Invited, Distinguished Lecturer**)
44. "Quasistatics in E&M: Sports Visualization, Wireless Power and Microrobots," Ga Tech, GA Nov. 2011.
45. "RF devices, circuits and systems: from nanometer to kilometer," Univ. of Texas, Austin, Oct 2011
46. "RF devices, circuits and systems: from nanometer to kilometer," Princeton Univ., Oct 2011
47. "High-speed PA and ADCs," Univ. Wisconsin, Oct. 2011
48. "At the boundaries of high-frequency analog & RF ICs: Speed, energy and uncertainty", GA Tech, GA, May 2011
49. "RF PA's and spin-torque oscillators for RF," University of FL, Mar, 2011
50. "Tip-directed, Field-assisted Nanofabrication," NIST, Mar 2011.
51. "Extending the boundaries of analog and RF electronics," Brown Univ., Mar, 2011.
52. "Nanoscale magnetics for integrated power conversion and RF," ARL, Jan, 2011.
53. "Ultimate limitation of conversion in conventional ADCs," ONR Superconducting Electronics Program, San Diego, Jan. 2011.
54. "Tip-assisted, field emission nanofabrication," Zyvex Corp., Apr., 2010.
55. "Tip-assisted Nanofabrication," Worcester Polytechnic Institute, MA, Mar. 2010.
56. "Spin Torque Oscillators for Agile RF," DARPA YFA Program, Oct. 2009.
57. "Perspectives on electrical oscillators," IBM Research, NY, Apr., 2009
58. "Electrical oscillators and phase noise," NIST, Boulder, CO, Oct. 2008
59. "Creativity in science and engineering," Innovation in Science and Engineering, Harvard University, Oct. 2008
60. "The Double Helix, a case study in scientific discovery," Innovation in Science & Technology, Paris University Consortium, Paris France, 2008.
61. "Creativity in science and engineering," Innovation in Science & Technology, Paris University Consortium, Paris France, 2008.
62. "New directions : soliton mode-locking and nanowire circuits," CMU, Sept. 2006
63. "Electrical soliton oscillators" University of Michigan, Mar, 2006
64. "Electrical soliton oscillator and nanowire Circuits," University of California, Berkeley, Apr. 2006
65. "Electrical soliton oscillators," Cornell University, Mar 2006.
66. "Electrical solitons," The Cooper Union, Feb. 2006.

<u>STEM Workshops, K-12</u>

1. STEM workshop for middle-school students in collaboration with Naval Information Warfare Center Atlantic STEM. July 2023.
2. IEEE Project CONNECT workshop teaching High School how to build AM radio. June 2023.

III.C. ORGANIZATION PARTICIPATION

Participation in centers, consortia, institutes, interdisciplinary/multidisciplinary activities and other organized scholarly efforts between departments within and across colleges or institutions

N/A

IV. EXTENSION AND ENGAGEMENT WITH CONSTITUENCIES OUTSIDE THE UNIVERSITY

Faculty Affliate (2023-) Bloomberg Cities Center, Kennedy School of Government
Faculty Associate (2014-), Innovation Fellow (2011-2014) Technology and Entrepreneurship Center, School of Engineering and Applied Science (SEAS), Harvard University. Courtesy appointment in SEAS for collaboration on innovation with students and faculty. Guest lecture in ES139/239 courses and assist with program development for symposia.

IV.A ACCOMPLISHMENTS

List accomplishments as applicable, e.g., bulletins, brochures, reports, pamphlets, non-refereed publications, computer software, educational videotapes, slide sets, popular press articles, and other pertinent evidence.

Experiential ECE Lectures – 800,000 You Tube views (two lectures)

Online dissemination of RF system design - ~**200,000 You Tube** views. Non-NCSU watch **800+ hours viewed per month** of PIs RF system design YouTube videos.

Developed two online courses including 70 video lectures and 20 laboratory assignments.
www.rickettslab.org/radiosystemdesign
www.rickettslab.org/adc

IV.B. PROGRAM IMPACTS

Describe results/impact of accomplishment.

N/A

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VI. SERVICE TO THE UNIVERSITY AND PROFESSIONAL SOCIETIES

University service (department, college, and university committees and governance organizations); state, regional, national and international professional activities and committee work, including professional associations.

DEPARTMENT SERVICE

Teaching Review Committee F22-
Promotion, Tenure Committee Co-Chair 2023
Marketing and Communication (ECE Department) – 2020-22
ECE Open House (ECE Department) – 2020-
Faculty Search Committee (ECE Department) – 2017, 2019, 2022
Course Curricula Committee (ECE Department) - 2015-present
Senior Design Director Search Committee (ECE Department) - 2014
Participated in Engineering Open House (ECE Department), 2014

UNIVERSITY SERVICE
N/A

PROFESSIONAL SOCIETIES

Chair, IEEE Chapter ACME (Joint chapter of Antennas and Propagation (AP), Electronic Packaging Society (EP), Microwave Theory and Techniques (MTT), and Electron Devices (ED) 2019-2023

Technical Committee **Chair** for IEEE T-MTT 9 Society 2020-2022

Technical Committee **Vice-chair** for IEEE T-MTT 7 Society 2015-2019

Technical Program **Chair**: Enabling Nanomanufacturing for Rapid Innovation, TRC/NSF Workshop, Aug. 2013

Technical Program Committee (member) – IEEE International Microwave Symposium 2014-;

Technical Program Committee IEEE BioWireless 2012-2015.

Session Chair - Nanotechnology, CMOS Emerging Technologies Conf., Banff, Canada 2009; NANO-DDS, Chemically-Synthesized, Biomimetic Systems and Biologically-Inspired Architectures Session, August 2011.

NSF Panelist (6 panels)

Reviewer for journals: ACS Nano Letters, Journal of Solid State Circuits (IEEE)Electron Device Letters (IEEE)Transactions on Circuits and Systems (IEEE)Proceedings of the National Academy of Sciences, MacArthur Foundation (Fellows program)Nano Letters, Sensors Journal of Applied Physics, Journal of Emerging and Selected Topics in Power Electronics, IET Circuits, Devices & Systems, IEEE Transactions on Power Electronics, IEEE Antennas and Wireless Propagation Letters, IEEE Transaction on Antennas and Propagation, IEEE Microwave and Wireless Components Letters, IEEE Transactions on Biomedical Circuits and Systems, Micromcahines, IET Microwaves, Antennas & Propagation, International Journal of Circuit Theory and Applications, Scientific Reports.

Appendix B to Expert Report of David Ricketts Regarding the Invalidity of U.S. Patent Nos. 8,717,101 and 9,917,563

1. David S. Ricketts - Expert Testimony Deposition & Trial (last 6 years)

DuaneMorris (2024-)
Case – In the Matter of Certain Wireless Front-End Modules and Devices Containing the Same
Case No. No. 337-TA-1413
Retained by Respondent Kangxi Communication Technologies (Shanghai) Co., Ltd. ("KCT")

Bond, Schoeneck & King NY (2024-)
Case – Signify North America Corporation et al. (Patent Owner) v. Lepro Innovation Inc. et al.
Case No. 2:22-cv-02095-JAD-DJA (Patent Owner)
Retained by Patent Owner

Bunsow De Mory CA (2024)
Case – Tesla, INC vs. Relink US LLC (Patent Owner)
Case No. IPR2024-00389
Retained by Patent Owner

Nixon Peabody CA (2024-)
Case - CogniPower LLC (Patent Owner) v. Anker Innovations LTD and Fantasia Trading LLC
Case No. C.A. No. 19-cv-02293-CFC-SRF
Retained by Patent Owner

Case - CogniPower LLC (Patent Owner) v. Samsung
Case No. 2:23-cv-160 - JRG
Retained by Patent Owner

Banner Witcoff DC (2024)
Case – SMA Solar Technology AG (Junior Party) v. SolarEdge Technologies Ltd.(Senior Party)
Case No. Patent Interference No. 106,144 (DK)
Retained by Senior Party

Daignault Iyer LLP (2023-)
Case – Parker Vision (Patent Owner) v. REALTEK SEMICONDUCTOR CORP.
Case No. 6:22-cv-01162-ADA
Retained by Patent Owner

Case – Parker Vision (Patent Owner) v. REALTEK SEMICONDUCTOR CORP.
Case No. 6:22-cv-00375
Retained by Patent Owner

Case – Parker Vision (Patent Owner) v. NXP SEMICONDUCTORS N.V., NXP B.V., NXP USA, INC. D/B/A NXP SEMICONDUCTORS USA, INC.,
Case No. 6:23-cv-00389
Retained by Patent Owner

Case – Parker Vision (Patent Owner) v. MEDIATEK INC. AND MEDIATEK USA INC.
Case No. 6:22-cv-01163-ADA
Retained by Patent Owner

Case – Parker Vision (Patent Owner) v. MEDIATEK INC. AND MEDIATEK USA INC.
Case No. 6:23-cv-00375-ADA
Retained by Patent Owner

Case – Parker Vision (Patent Owner) v. TEXAS INSTRUMENTS INCORPORATED
USA INC.
Case No. 6:23-cv-00384
Retained by Patent Owner

McKool Smith Tx (2023-2024)
Case - Mojo Mobility (Patent Owner) v. Samsung
Case No. 2:22-cv-00398
Retained by Patent Owner

Anderson Dailey LLP (2023-)
Case – Joy Laskar, Ph.D. v. Phillip W. Hurd; and Patrick A. Jenkins
Case No. 1:18-cv-4570-WMR
Retained by Plaintiff

Kramer Alberti CA (2023-2024)
Case – Polaris Powerled Tech LLC (Patent Owner) v. Samsung
Civil Action No. 2:22-cv-00469-JRG
Retained by Patent Owner

King & Wood Mallesons, Melbourne, Victoria, Australia (2023-)
Case –- Federal Court of Australia
Proceeding No. VID 122/2023
Retained by Respondents

Perkins Coie, San Francisco, CA (2023-)
Case –- The Noco Company, Inc. (Patent Owner) v. Shenzhen Gooloo E-Commerce Co., Ltd.
NDOH Case No. 1:20-cv-01171-PAB
Retained by Defendant

Case –- SHENZHEN XINZEXING E-COMMERCE CO., LTD., (Petitioner) v. SHENZHEN CARKU
TECHNOLOGY CO., LTD.(Patent Owner)
IPR2024-00222
Retained by Patent Owner

Case –- Shenzhen Chic Electrics Co., Ltd. (Petitioner) v. Pilot, Inc.(Patent Owner)
IPR2023-00810
Retained by Petitioner

Case –- In the Matter of Certain Portable Battery Jump Starters and Components Thereof
ITC Investigation No. 337-TA-1360
Retained by Respondents

Case –- In the Matter of Certain Portable Battery Jump Starters and Components Thereof
ITC Investigation No. 337-TA-1359
Retained by Respondents

Heim, Payne & Chorush, Houston, Tx (2022)
Case - Apple Inc. et al. (Petitioner) v. Arigna Technology Ltd (Patent Owner)
IPR2022-01037
Retained by Patent Owner

Norton Rose Fulbright, Toronto, Canada (2022-2023)
Case – *Canadian Tire Corporation, Limited (Defendant) v. The Noco Company, Inc (Plaintiff)*
Court File No. T-343-20

Jurisdiction: Federal Court, Canada.
Retained by Defendant

Russ August & Kabat, Los Angeles, CA (2021-2023)

Case - *APPLE INC.*, (Petitioner) v. *SCRAMOGE TECHNOLOGY LTD.*, (Patent Owner)
IPR2022-00351
IPR2022-00120
IPR2022-00117
Retained by Patent Owner

Powell Gilbert, London (2022)

Case –*Shenzhen Carku Technology Co., Ltd. (Claimant) and The NOCO Company (Defendant)*
Claim No. HP-2020-000018
Jurisdiction: The High Court of Justice Business and Property Courts of England and Wales.
Retained by Claimant

Kramer, Day, Burlingame (2020-2023)

Case - *Garrity Power Services LLCvs. Samsung Electronics Ltd.*
Case Number – Texas Eastern District Case No. 2:20-cv-00269
EPR - 9,906,067 Control No. 90/014,746
Retained by Patent Owner (Garrity)

Perkins Coie, San Francisco, CA (2021-2022) Validity/Invalidity

Case – *The NOCO Company vs. Shenzhen Carku Technology Co., Ltd. And others* (Respondents)
Case Number - USITC 337-TA-1256
Retained by Respondents

Stern Kessler Goldstein & Fox, Washington, DC (2019-2020)

Case - *Samsung Electronics Co., Ltd. et al.* (Petitioner) *v. NuCurrent, Inc.*(Patent Owner)
Case Number - IPR2019-00858,
Case Number - IPR2019-00859
Case Number - IPR2019-00860
Case Number - IPR2019-00861
Case Number - IPR2019-00862
Case Number - IPR2019-00863
Case Number - IPR2019-01217
Case Number – PGR2019-0049
Case Number – PGR2019-0050
Retained by Patent Owner (NuCurrent)

Appendix C to Expert Report of David Ricketts Regarding the Invalidity of U.S. Patent Nos. 8,717,101 and 9,917,563

Materials Considered

Pleadings

- Respondent's Claim Construction Brief including RXM-1 – RXM-18 and JXM-1 – JXM-6
- Complainants' Claim Construction Brief including CXM-1 – CXM-10
- Staff's Claim Construction Brief including SXM-1 – SXM-2

Discovery Requests and Responses

- Complainants' Second Supplemental Responses and Objections to Respondents Grand Chip Labs, Inc.'s and Kangxi Communications Technologies (Shanghai) Co., Ltd.'s First Set of Interrogatories to Complainants (Nos. 7-8) (dated 11-08-2024)
- Complainants' Fourth Supplemental Responses and Objections to Respondents Grand Chip Labs, Inc.'s and Kangxi Communications Technologies (Shanghai) Co., Ltd.'s First Set of Interrogatories to Complainants (Nos. 7-8) (dated 02-19-2025)
- Complainants' First Supplemental Responses and Objections to Respondents Grand Chip Labs, Inc.'s and Kangxi Communications Technologies (Shanghai) Co., Ltd.'s First Set of Interrogatories to Complainants (Nos. 1-2, 10-18) (dated 02-19-2025) including Exhibits A-D, I-K (including supplemental exhibits)
- Complainants' Supplemental Domestic Industry Contentions (dated 01-28-2025)
- Complainants' Supplemental Domestic Industry Contentions (dated 02-19-2025)
- Kangxi Communications Technologies (Shanghai) Co. and Grand Chip Labs, Inc.'s Disclosure of Initial Invalidity Contentions (dated 10-22-2024) including Appendices A-B
- Kangxi Communications Technologies (Shanghai) Co. and Grand Chip Labs, Inc.'s Disclosure of Amended Invalidity Contentions (dated 01-29-2025) including Amended Appendices A-B
- Kangxi Communications Technologies (Shanghai) Co. and Grand Chip Labs, Inc.'s Disclosure of Second Amended Invalidity Contentions (dated 02-19-2025)
- Kangxi Communications Technologies (Shanghai) Co. and Grand Chip Labs, Inc.'s Non-Burden Contentions Other Than Domestic Industry and Remedy (dated 11-08-2024)
- Kangxi Communications Technologies (Shanghai) Co. and Grand Chip Labs, Inc.'s Non-Burden Contentions Concerning Domestic Industry and Remedy (dated 11-08-2024)
- Kangxi Communications Technologies (Shanghai) Co. and Grand Chip Labs, Inc.'s Amended Non-Burden Contentions Other Than Domestic Industry and Remedy (dated 02-19-2025)
- Kangxi Communications Technologies (Shanghai) Co. and Grand Chip Labs, Inc.'s Amended Non-Burden Contentions Concerning Domestic Industry (Technical Prong) (dated 02-24-2025)
- Kangxi Communications Technologies (Shanghai) Co. and Grand Chip Labs, Inc.'s Second Amended Non-Burden Contentions Other Than Domestic Industry and Remedy (dated 02-23-2025)

Deposition Transcripts

- February 5, 2025 Deposition Transcript of David Recker

- January 30, 2025 Deposition Transcript of Huan (Steve) Zhao
- January 27, 2025 Deposition Transcript of Qiang Yu
- January 14, 2025 Deposition Transcript of Kathy Li
- February 14, 2025 Deposition Transcript of Miriam Hanna
- February 18, 2025 Deposition of Sudhanshu Mehta

Other Documents

- Petition for *Inter Partes* Review of U.S. Patent 8,717,101 and Corresponding Exhibits
- Petition for *Inter Partes* Review of U.S. Patent 8,917,563 and Corresponding Exhibits
- Skyworks_ITC_000018682
- Skyworks_ITC_000019819
- Skyworks_ITC_000019877
- Skyworks_ITC_000019815
- Skyworks_ITC_000019823
- Skyworks_ITC_000019873
- Skyworks_ITC_000019831
- Skyworks_ITC_000019827
- Skyworks_ITC_000018918
- Skyworks_ITC_000018594
- Skyworks_ITC_000018917
- Skyworks_ITC_000018916
- Skyworks_ITC_000018660
- Skyworks_ITC_000018586
- Skyworks_ITC_000018573
- Skyworks_ITC_000018657
- Skyworks_ITC_000018655
- Skyworks_ITC_000018755
- Skyworks_ITC_000019841
- Skyworks_ITC_000011177
- Skyworks_ITC_000110940
- Skyworks_ITC_000110938
- Skyworks_ITC_000110947
- KCT-ITC_0054264
- KCT-ITC_0131657
- KCT-ITC_0004409
- KCT-ITC_0116894
- KCT-ITC_0129691
- KCT-ITC_0042456
- KCT-ITC_0144900
- KCT-ITC_0145215
- KCT-ITC_0145274

- KCT-ITC_0145297
- KCT-ITC_0145327
- KCT-ITC_0145359
- KCT-ITC_0145378
- KCT-ITC_0145398
- KCT-ITC_0145423
- KCT-ITC_0145454
- KCT-ITC_0145480
- KCT-ITC_0145508
- KCT-ITC_0145534
- KCT-ITC_0145561
- KCT-ITC_0133093
- KCT-ITC_0181533
- KCT-ITC_0181566
- KCT-ITC_0181635
- KCT-ITC_0290692
- KCT-ITC_0290696
- KCT-ITC_0278519
- KCT-ITC_0263451
- KCT-ITC_0499217
- KCT-ITC_0498527
- KCT-ITC_0499204
- KCT-ITC_0313830
- KCT-ITC_0310109
- KCT-ITC_0289666
- KCT-ITC_0313868
- KCT-ITC_0344539
- KCT-ITC_0772056
- KCT-ITC_0842514
- KCT-ITC_0453378
- KCT-ITC_0313832
- KCT-ITC_0313839
- KCT-ITC_0313870
- KCT-ITC_0313877
- KCT-ITC_0314249
- KCT-ITC_0237878
- KCT-ITC_0237888
- KCT-ITC_0237901
- KCT-ITC_0243995
- KCT-ITC_0244389
- KCT-ITC_0244013

- KCT-ITC_0237114
- COM-ITC-000042
- Skyworks_ITC_000011155

Appendix D to Expert Report of David Ricketts Regarding the Invalidity of U.S. Patent Nos. 8,717,101 and 9,917,563

I am not an attorney and have not been asked to offer my opinion on the law. I have bene informed and understand however that certain legal standards are to be applied by technical experts in forming opinions regarding the invalidity of patent claims. I have relied on instructions from counsel as to the applicable legal standards, which I have applied in forming my opinions expressed in this report. My understanding of the applicable legal standards is set forth below.

I understand that the claims of an issued patent are presumed valid, but those claims can be proven invalid by clear and convincing evidence that they fail to comply with one or more of the legal requirements. I understand that clear and convincing evidence is a higher standard than a preponderance of the evidence, but a lower standard than beyond a reasonable doubt.

A. Anticipation

It is my understanding that a claim is "anticipated" if each and every element of the claim is disclosed in a single prior art reference. I understand that each element of a patent claim may be disclosed by a prior art reference either expressly or inherently. I understand that an element of a patent claim is inherent in a prior art reference if the element must necessarily be present and such would be recognized by one of ordinary skill in the art. However, I understand that inherency cannot be established by mere probabilities or possibilities. I understand that the description in the written reference does not have to be in the same words as the claim, but all of the requirements of the claim must be there, either expressly or inherently. I understand that if the disclosure of a prior art reference is sufficient to show that the natural result flowing from the operation as taught would result in the performance of the questioned function, the disclosure is regarded as sufficient to anticipate

Below is a non-exhaustive list of ways that a patent claim anticipated:

(1) If the claimed invention was already publicly known or publicly used by others in the United States before the effective filing date for the claim at issue;

(2) If the claimed invention was already patented or described in a printed publication anywhere in the world before the effective filing date for the claim at issue. A reference is a "printed publication" if it is accessible to those interested in the field;

(3) If the claimed invention was already patented or described in a printed publication anywhere in the world one year before the effective filing date for the claim at issue. A reference is a "printed publication" if it is accessible to those interested in the field;

I understand that evaluating whether a patent claim is "anticipated" is a two-step process. In the first step, the claim language is construed by a court, which I discussed in my report. The second step involves a comparison of the claim, as construed by the court, to the prior art on a limitation-by-limitation basis.

I also understand that it is possible for extra material not explicitly contained in a single prior art document to also be considered for the purposes of anticipation if the prior art document incorporates by reference that extra material.

B. Obviousness

I understand that a patent claim is invalid if the claimed invention would have been obvious to a person of ordinary skill in the field as of its effective filing date. This means that even if all of the limitations of the claim cannot be found in a single prior art reference, the claim may nonetheless be invalid as obvious.

I understand that the ultimate conclusion of whether a claim is obvious should be based upon evaluating certain factors:

(1) The level of ordinary skill in the field that someone would have had as of the effective filing date of the claimed invention. I describe my opinion as to the level of ordinary skill a person must have to qualify as a person of ordinary skill in the art in the body of my report.

(2) The scope and content of the prior art. In order to be considered as prior art to an asserted patent, these references must be reasonably related or pertinent to the claimed invention of that patent. A reference is reasonably related if it is in the same field as the claimed invention or is from another field to which a person of ordinary skill in the field would look to solve a known problem. In order for a reference to be "reasonably pertinent" to the problem, it must logically have commended itself to an inventor's attention in considering his problem. In determining whether a reference is reasonably pertinent, one should consider the problem faced by the inventor, as reflected - either explicitly or implicitly - in the specification.

(3) What difference, if any, existed between the claimed invention and the prior art.

(4) Any objective evidence (sometimes called "secondary considerations") that may shed light on the obviousness or not of the claimed invention.

I understand that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. In other words, when a claim simply arranges prior art elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, then such a combination is obvious. Moreover, when a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination is likely to be obvious unless the combination yields an unpredictable result.

I understand that when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill in the art can implement a predictable variation, such a variation is likely unpatentable. For the same reason, if a technique has been used to improve one device, and one of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. One question to consider is whether the improvement is more than the predictable use of prior art elements according to their established functions.

I understand that it may often be necessary, in a validity analysis, to look to interrelated teachings of multiple patents or other publications or pieces of prior art; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by one of ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

I understand that a validity analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim; it is appropriate to take account of the inferences and creative steps that a person of ordinary skill in the art would employ. I understand that a person of ordinary skill in the art is also a person of ordinary creativity.

I understand that a claim composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art. I understand that it can be important to identify a reason that would have prompted a person of ordinary skill in the art in the relevant field to combine the elements in the way the claimed new invention does. Therefore, I am informed that in determining whether a claimed combination is obvious, the correct question is whether the combination was obvious to a person of ordinary skill in the art at

the time of the alleged invention. I am told that one of the ways in which subject matter can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims. I understand that any need or problem known in the field of endeavor at the time of alleged invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.

I understand that one should not assume that a person of ordinary skill in the art attempting to solve a problem will be led only to those elements of prior art designed to solve the same problem. Instead, I understand that since familiar items may have obvious uses beyond their primary purposes, in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple prior art references together like pieces of a puzzle.

I understand that, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, then it is likely the product is not of innovation but of ordinary skill and common sense. I understand that, in such an instance, the fact that the combination was obvious to try may show that the combination is obvious.

I understand that, when determining whether a claimed invention is obvious, any "secondary considerations" of non-obviousness should also be considered. I further understand that there must be a nexus between any alleged secondary considerations and the Asserted Claims. In addition, I understand that the burden of introducing evidence of secondary considerations generally is on the patent owner.

I understand secondary considerations of non-obviousness can involve one or more of the following:

(5) Whether the invention satisfied a long-felt but unresolved need;

(6) Whether others had tried and failed to make the invention;

(7) Whether the invention achieved unexpected results;

(8) Whether the inventor proceeded contrary to accepted wisdom in the field;

(9) Whether others in the field praised the invention;

(10) Whether the invention was commercially successful as a result of the merits of the claimed invention (rather than the result of design needs or market-pressure advertising or similar activities);

(11) Whether others having ordinary skill in the field independently made the claimed invention at about the same time the inventor made the invention;

(12) Whether others copied the invention.

It is my understanding that any assertion of the above indicia must be accompanied by a "nexus" between the merits of the invention and the evidence offered. For example, commercial success of a product is relevant to obviousness if the success of the product is attributable to the patented features of the claimed invention. If, on the other hand, commercial success is due to, for example, features of the product not claimed in the patent, due to claimed features that existed in the prior art, and/or due to advertising, promotion, salesmanship or the like, then any commercial success should not be considered an indication of non-obviousness.

C. Written Description

I understand that a patent claim is invalid if the patent does not contain an adequate written description of the claimed invention. This is known as the "written description" requirement. I understand that the purpose of this written description requirement is to demonstrate that the inventor was in possession of the claimed invention at the time the

application for the patent was filed, even though the claim may have changed or new claims added since that time. I understand that the purpose of the written description requirement is to ensure that the scope of the right to exclude others, as set forth in the claims, does not overreach the scope of the inventor's contribution to the field of art as described in the patent specification, and to prevent the inventor from later asserting that he invented that which he did not.

I understand that the written description requirement is satisfied if a POSITA reading the original patent application at the time it was filed would have recognized that the patent application described the invention as claimed, even though the description may not use the exact words found in the claim. A requirement in a claim need not be specifically disclosed in the patent application as originally filed if a POSITA would understand that the missing requirement is necessarily implied in the patent application as originally filed. I understand that the description must do more than merely disclose that which would render the claimed invention obvious. I understand that the written description requirement may be satisfied by any combination of the words, structures, figures, diagrams, formulas, etc., contained in the patent application.

Likewise, I understand that where a specification does not disclose claimed subject matter, it is not sufficient for written description purposes to argue that a POSITA might be able to construct the claimed subject matter from the teachings of the disclosure. I have been instructed that it is not proper for purposes of the written description requirement to use the knowledge of a POSITA to speculate as to what the inventor might have envisioned, but failed to disclose.

I understand that material later added to the claims by amendment is not inherent to the original specification for the purposes satisfying the written description requirement if that

amendment would broaden the scope of the invention beyond that which is supported in the initial disclosure.

I understand that the written description requirement requires supporting disclosure in the specification for the full scope of a claim. I understand that the patentee's infringement allegations can be relevant to a written description analysis insofar as those allegations demonstrate the asserted scope of the claims.

D. Enablement

I understand that a patent claim is invalid if the patent at the time it was filed did not contain a description of the claimed invention that is sufficiently full and clear to enable a POSITA at the time to make and use the full scope of the invention. This is known as the "enablement" requirement. The purpose of this requirement is to ensure that the public, in exchange for the patent rights given to the inventor, obtains from the inventor a full disclosure of how to make and use the invention.

I understand that the patent is not required to disclose information that would be known to persons of skill in the art. The patent may be enabling even though it does not expressly state some information if a POSITA could make and use the invention without having to do excessive experimentation. In determining whether excessive experimentation is required, the following factors may be considered:

(1) the quantity of experimentation necessary;

(2) the amount of direction or guidance presented;

(3) the presence or absence of working examples;

(4) the nature of the invention;

(5) the state of the prior art;

(6) the relative skill of those in the art;

(7) the predictability or unpredictability of the art; and

(8) the breadth of the claims.

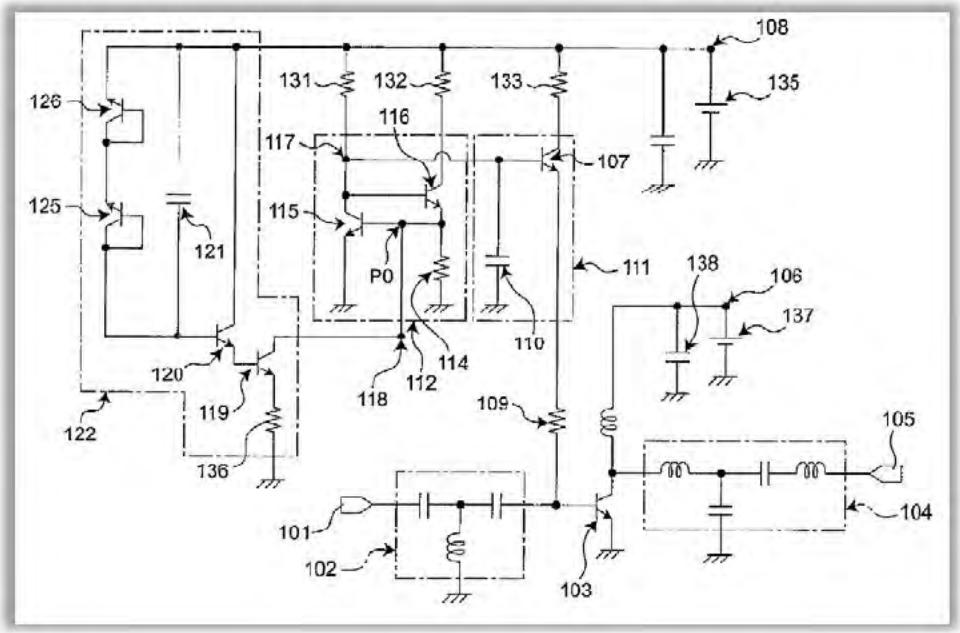
I understand that these factors are illustrative, and all need not be reviewed and met to find a disclosure enabling or not.

I understand that the enablement requirement is met if the specification enables any mode of making and using the invention, provided that the full scope of the invention is enabled. The patent need not enable an optimized or commercially viable process or method of practicing the invention unless the claims specify that the invention is directed to an optimized or commercially viable process. I understand that the "how to use" prong of the enablement requirement further requires that the specification disclose a practical utility for the invention. In other words, the specification must disclose a practical use for the invention.

Finally, I understand that the question of whether a patent is enabling is judged as of the date the application for the patent was first filed.

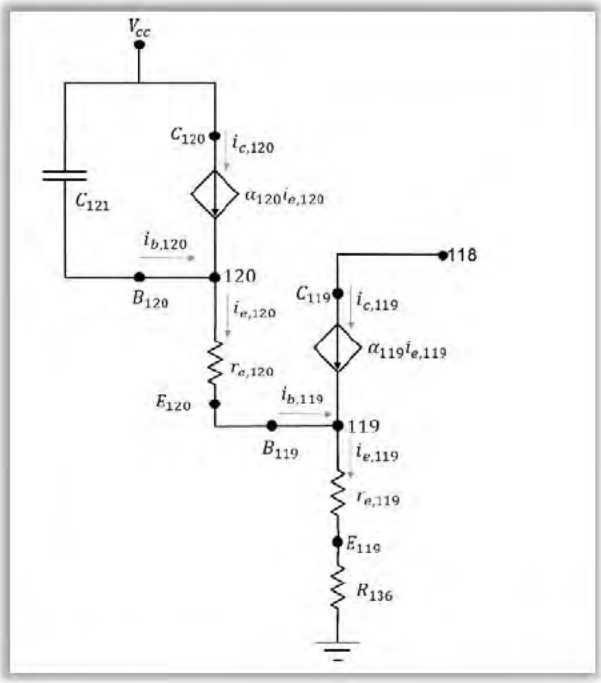
Appendix E to Expert Report of David Ricketts Regarding the Invalidity of U.S. Patent Nos. 8,717,101 and 9,917,563

1. The Ishimaru speedup circuit shown in Fig.1 (below) forms an RC network. The RC network has a time constant that depends on at least capacitor 121 and resistor 136. While unnecessary to my opinions, to the extent one wanted to confirm the relationships of the timing of Ishimaru's circuit as controlled by capacitor 121 and resistor 136, one could do so in a variety of ways. The following analysis is one of several ways one might characterize the behavior of the RC network in Ishimaru's speed-up circuit. Nothing about my opinions depends on the following particular formulation. Nonetheless, my opinions are further consistent with and further supported by the following derivation of an approximate time constant for the *Ishimaru* speed-up circuit.



Ishimaru Fig. 1.

2. For example, one approximation of an RC time constant associated with Ishimaru's speed-up circuit can be derived by modeling transistor 119 and 120 by the small-signal T-model for BJTs shown below.



Ishimaru Speedup Circuit Small T model.

In an exemplary derivation, I first calculate the effective resistance seen by transistor 119, $R_{eff,119}$.

$$R_{eff,119} = \frac{V_{B,119}}{i_{b,119}} \tag{1}$$

Note that the current $i_{e,119}$ can be defined as:

$$i_{e,119} = \frac{V_{b,119}}{r_{e,119} + R_{136}} \tag{2}$$

Based on the well-known BJT current-voltage relationships in active mode, we can define $i_{b,119}$ in terms of $i_{e,119}$:

$$i_{b,119} = (1 - \alpha)i_{e,119} = \frac{i_{e,119}}{(\beta + 1)} \tag{3}$$

Now substituting, (2) into (3):

$$i_{b,119} = \left(\frac{1}{(\beta + 1)}\right)\left(\frac{V_{b,119}}{r_{e,119} + R_{136}}\right) = \frac{V_{b,119}}{(\beta + 1)(r_{e,119} + R_{136})} \tag{4}$$

Finally, utilizing (4) into (1), $R_{eff,119}$ can be rewritten:

$$R_{eff,119} = \frac{V_{B,119}}{i_{b,119}} = \frac{V_{B,119}}{\frac{V_{b,119}}{(\beta+1)(r_{e,119}+R_{136})}} = (\beta+1)(r_{e,119}+R_{136}) \quad (5)$$

Now that I have determined the effective resistance seen by transistor 119, I will evaluate the effective resistance seen by transistor 120, $R_{eff,120}$.

$$R_{eff,120} = \frac{V_{B,120}}{i_{b,120}} \quad (6)$$

Similar to the equation for 119, the current $i_{e,120}$ can be defined as:

$$i_{e,120} = \frac{V_{b,120}}{r_{e,120}+R_{eff,119}} \quad (7)$$

Again, based on the well-known BJT current-voltage relationships in active mode, we can define $i_{b,120}$ in terms of $i_{e,120}$:

$$i_{b,120} = (1-\alpha)i_{e,120} = \frac{i_{e,120}}{(\beta+1)} \quad (8)$$

Substituting (7) into (8):

$$i_{b,120} = \frac{i_{e,120}}{(\beta+1)} = \frac{V_{b,120}}{(\beta+1)(r_{e,120}+R_{eff,119})} \quad (9)$$

Next with (6) and (9), the effective resistance of $R_{eff,120}$ can be defined as:

$$R_{eff,120} = \frac{V_{B,120}}{i_{b,120}} = \frac{V_{b,120}}{\frac{V_{b,120}}{(\beta+1)(r_{e,120}+R_{eff,119})}} = (\beta+1)(r_{e,120}+R_{eff,119}) \quad (10)$$

Finally, substituting the effective resistance of 119 into (10):

$$R_{eff,120} = (\beta+1)(r_{e,120}+R_{eff,119}) = (\beta+1)(r_{e,120}) + (\beta+1)^2\,(r_{e,119}+R_{136}) \quad (11)$$

Now for a series resistor and capacitor, the time constant is well known to be defined as below:

$$\tau = RC \quad (12)$$

For the series resistor, $R_{eff,120}$, and capacitor, $C_{,121}$, in Ishimaru's circuit, this becomes:

$$\tau = \left[(\beta+1)(r_{e,120}) + (\beta+1)^2\,(r_{e,119}+R_{136})\right]C_{121} \quad (13)$$

Thus from (13), it is apparent that the time constant of *Ishimaru's* speedup primarily circuit depends on the second term (i.e., $(\beta + 1)^2\ (r_{e,119} + R_{136})C_{121}$). This is due to the fact that a transistor current gain value, β, is commonly on the order of, *e.g.*, 60-150, or higher. If we assume $\beta = 100$, then second term from (13) has a multiplier term (i.e., $(\beta + 1)^2$) of approximately 10,000. We also note that the value of $r_{e,119}$ is negligible in the *Ishimaru* circuit. Thus from (13), I have further provided support for my conclusion that that the time constant of Ishimaru's speed-up circuit depends at least, and indeed primarily, on the values of R_{136}, $C_{,121}$, and the current gain value, β, of transistors 119 and 120.