

AMENDED APPENDIX B-03

Invalidity Chart for U.S. Patent No. 9,917,563 (“’563 Patent”)¹ U.S. Patent Publication No. 2009/0212863 (“*Ishimaru*”)

I. Overview

The asserted claims of the ’563 Patent are obvious in view of:

- U.S. Patent Publication No. 2009/0212863 (“*Ishimaru*”),² in view of U.S. Patent Publication No. 2004/0232982 to Ichitsubo et al., “RF Front-End Module for Wireless Communication Devices” (“*Ichitsubo*”)³ or Johnson, Silicon-Germanium BiCMOS HBT Technology for Wireless Power Amplifier Applications, IEEE Journal of Solid-State Circuits, Vol. 39, No. 10, (Oct. 2004) (“*Johnson*”)⁴; and
- *Ishimaru* in view of *Ichitsubo* or *Johnson* and further in view of Linden T. Harrison, Current Sources & Voltage References (2005) (“*Harrison*”)⁵

The following additional references are illustrative of the state of the art and the knowledge of a person of ordinary skill in the art (“POSITA”):

- Japanese Patent Publication No. 2005-027130 to Morisawa (Certified Translation) (“*Morisawa*”). *Morisawa* published on January 27, 2005 and is prior art to the Group 1 Patents at least under Pre-AIA 35 U.S.C. § 102(b).⁶

¹In addition to the ’563 Patent, Complainant asserts a parent patent in the same patent family, US 8,717,101 (“the ’101 Patent”). These contentions refer to the two patents, collectively, as the “Group 1 Patents.”

² *Ishimaru* published on August 27, 2009 and is prior art to the ’563 Patent at least under Pre-AIA 35 U.S.C. § 102(b).

³ *Ichitsubo* published November 25, 2004 and is prior art to the Group 1 patents under Pre-AIA 35 U.S.C. § 102(b).

⁴ *Johnson* published in October 2004 and is prior art to the Group 1 Patents at least under Pre-AIA 35 U.S.C. § 102(b).

⁵ *Harrison* was published in 2005 and is prior art to the Group 1 Patents under Pre-AIA 35 U.S.C. § 102(b).

⁶ *Morisawa* is charted against the ’563 Patent in Appendix B-02.

- *Grebene*, Bipolar and MOS Analog Integrated Circuit Design (2003) (“*Grebene*”) was published in 2003 and is prior art to the Group 1 Patents under Pre-AIA 35 U.S.C. § 102(b).
- *Gray*, Analysis and Design of Analog Integrated Circuits (5th Ed 2009) (“*Gray*”) was published in 2009 and is prior art to the Group 1 Patents under Pre-AIA 35 U.S.C. § 102(b).
- Barrie Gilbert, Bipolar Current Mirrors,” Chapter 6 in Toumazou *et al.*, Analogue IC Design - The Current-Mode Approach (Reprinted 2008) (“*Gilbert*”) was published in 2008 and is prior art to the Group 1 Patents under Pre-AIA 35 U.S.C. § 102(b).
- *Illingworth*, Dictionary of Electronics (3rd Ed. 1998). *Illingworth* published in 1998 and is prior art to the Group 1 Patents at least under Pre-AIA 35 U.S.C. § 102(b).
- *Laplante*, Comprehensive Dictionary of Electrical Engineering (2nd Ed. 2005). *LaPlante* published in 2005 and is prior art to the Group 1 Patents at least under Pre-AIA 35 U.S.C. § 102(b).
- U.S. Patent No. 6,831,517 to Hedberg, “Bias-Management System and Method for Programmable Rf Power Amplifier” (“*Hedberg*”) was published on December 14, 2004, and is prior art to the Group 1 Patents under Pre-AIA 35 U.S.C. § 102(b).
- *Diels*, Single-Package Integration of RF Blocks for a 5 GHz WLAN Application, IEEE Transactions On Advanced Packaging, Vol. 24, No. 3, (August 2001) (“*Diels*”). *Diels* was published in 2001, and is prior art to the Group 1 Patents under Pre-AIA 35 U.S.C. § 102(b).
- *Murase*, Multi-chip Transmitter/Receiver Module Using High Dielectric Substrates for 5.8 Ghz ITS Applications, 1999 MTT-S Digest (“*Murase*”). *Murase* published in 1999 and is prior art to the Group 1 Patents under Pre-AIA 35 U.S.C. § 102(b).
- U.S. Patent Pub. 2011/0128078 to Doherty et al., “System and Method of Prebias for Rapid Power Amplifier Response Correction” (“*Doherty*”) was published on June 2, 2011 and is prior art to the Group 1 Patents under at least Pre-AIA 35 U.S.C. § 102(e).
- Japanese Patent Publication No. 2009-283991 to Akagi (Certified Translation) (“*Akagi*”). *Akagi* published on December 3, 2009 and is prior art to the Group 1 Patents at least under Pre-AIA 35 U.S.C. § 102(b).
- EIC Corp. ECP052D Component, on sale as of 2004, which is prior art to the Group 1 Patents under Pre-AIA 35 U.S.C. § 102(b).

- TriQuint Semiconductor, Application Note TVS Protection and Bias Sequencing for HBT Amplifiers (June 2009) (“*Triquint*”) published in 2009 and is prior art to the Group 1 Patents under Pre-AIA 35 U.S.C. § 102(b).

Respondent’s contentions and claim charts take into account Complainants’ apparent constructions. Respondent’s assertion that a particular limitation is disclosed by a prior-art reference, or Respondent’s assertion that a particular claim limitation is disclosed by a prior-art reference in a particular manner, may be based in whole or in part on Complainants’ apparent claim interpretations, infringement theories, and/or mappings. In relying on Complainants’ apparent claim interpretations, infringement theories, and/or mappings, Respondent does not admit that Complainants’ apparent claim interpretations, infringement theories, and/or mappings are supportable or proper or that the claim limitations in question are definite or otherwise amenable to construction. Respondent will argue for appropriate constructions of any term or claim of any patent at issue in this action pursuant to the procedural schedule. Respondent reserves the right to modify and/or amend the analysis in this chart based on claim constructions and/or any changes or explanations of apparent claim constructions, infringement theories and/or mappings.

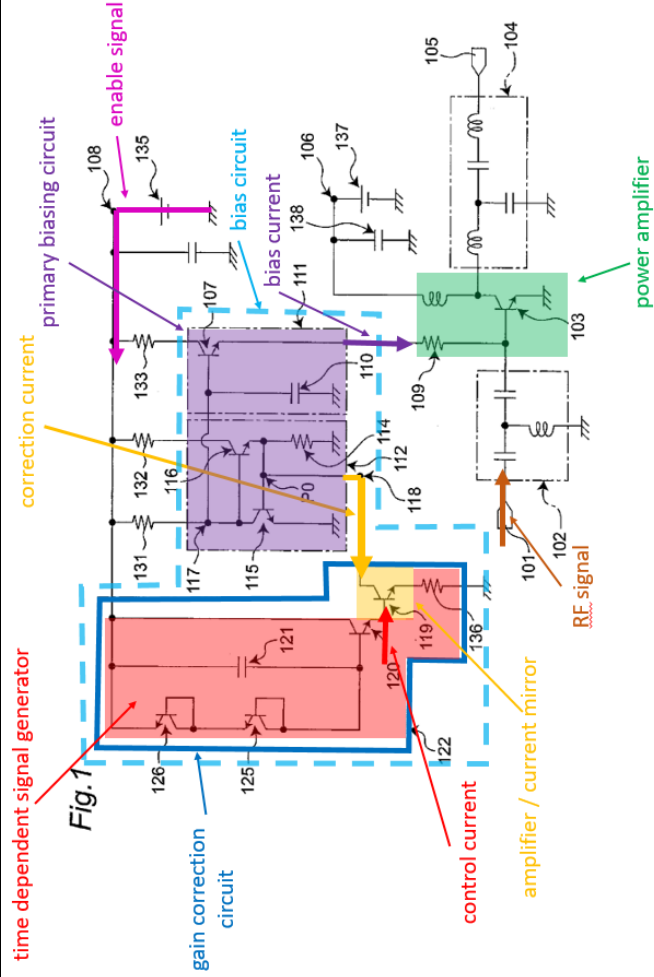
The citations to portions of any prior-art reference in this chart are exemplary only. Respondent will rely on the entirety of the references cited in this chart to show that the asserted claims are invalid. Discovery is ongoing and Respondent will update this chart as appropriate based on the results of its investigation, including third-party discovery.

II. State of the Art

Respondents also incorporate by reference their discussion of the state of the art found in Appendix A-03 (“State of the Art”).

III. Claim Chart

Claim Language	Ishimaru Alone and/or in Combination with Other References
[14a] 14. A packaged module comprising: a package substrate; and [14b] an integrated circuit attached to the package substrate and including	The preamble is not limiting, at least not with respect to the recitation of “a packaged module.” The body of the claim defines a structurally complete invention (apart from its failure to meet the requirements of 35 U.S.C. § 112). To the extent the preamble is limiting, <i>a packaged module comprising a package substrate and an integrated circuit attached to the package substrate</i> is disclosed by: • <i>Ishimaru</i> in view of <i>Ichitsubo</i> or <i>Johnson</i>. <i>Ishimaru</i> discloses a power amplifier (green) and bias circuit (light blue) for use in a radio communications device. <i>Ishimaru</i> Abstract, ¶1, Fig. 1.



Ishimaru Fig. 1 (annotated).

While *Ishimaru* does not expressly describe the extra detail of its power amplifier (green) and bias circuit (light blue) being in an integrated circuit attached to a package substrate as part of a packaged module as claimed, that is nonetheless understood by a POSITA for several reasons. First, *Ishimaru* discloses that its power amplifier and bias circuit is for “a high frequency power amplifier to be used in radio communication devices or the like.” *Ishimaru* Abstract, ¶1. A POSITA readily understood that the overwhelming majority of these types of circuits were designed as packaged ICs. *Laplante* 003 (“die[s] or chips have to ultimately be packaged to be useful.”); *Johnson* 1609, 1612, Fig. 17; *Diels* Fig. 2; *Hedberg*. Second, *Ishimaru* is directed to an incremental improvement in the startup behavior of power amplifiers that is directed at the margin of high performing devices, i.e., the type implemented in packaged ICs. Third, *Ishimaru* is directed

Claim Language	<i>Ishimaru</i> Alone and/or in Combination with Other References
	to improvements in the startup behavior of power amplifiers, which requires additional circuitry. Such additional circuitry would be routine and expected to be integrated into an IC and packaged. For these reasons, a POSITA reading <i>Ishimaru</i> in 2011 understood that <i>Ishimaru</i>’s “radio communication device” with its power amplifier (green) and bias circuits (light blue) would be implemented in an integrated circuit attached to a package substrate in a packaged module as claimed. Thus, while not explicitly stated, the packaging limitations claimed are nonetheless disclosed to a POSITA in view of the reasonable inferences that a skilled artisan would draw when reading <i>Ishimaru</i>. <u><i>Ishimaru</i> in view of <i>Ichitsubo</i></u> To the extent that Complainant argues that <i>Ishimaru</i> does not explicitly state that power amplifier (green) and bias circuits (light blue) in a “radio communication device” would be implemented in an integrated circuit attached to a package substrate in a packaged module as claimed, it would have been obvious to implement <i>Ishimaru</i>’s PA (green) and bias circuit (light blue) in the form of an integrated circuit attached to a package substrate as part of a packaged module in view of <i>Ichitsubo</i>, for the reasons described below. Referencing Figures 1 and 8 (below), <i>Ichitsubo</i> describes a “radio frequency power amplifier (PA) module 14” (packaged module) (gray). <i>Ichitsubo</i> ¶25. The PA module is a packaged module in that it contains, simplifies and protects, i.e. packages, one or more ICs (pink) in a unitary module for assembly into larger device. <i>Ichitsubo</i> ¶¶3, 24, 84.

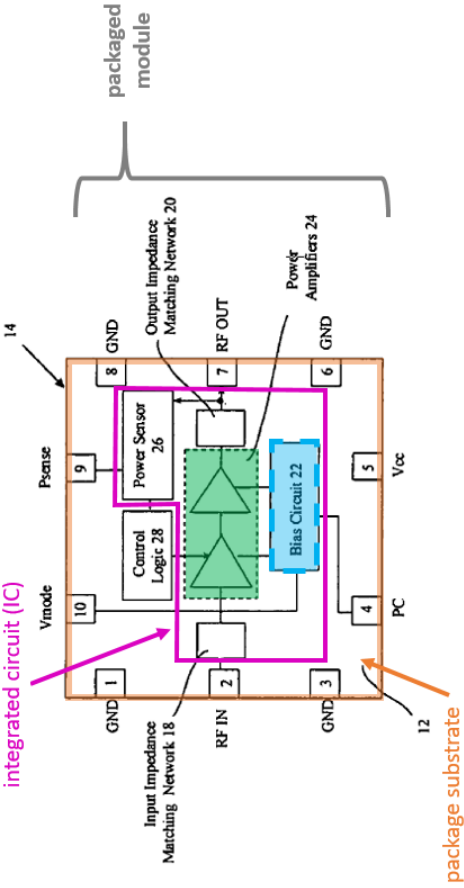


Figure 1

Ichitsubo Fig. 1 (annotated).

Claim Language	Ishimaru Alone and/or in Combination with Other References
	The diagram illustrates a packaged module (800) containing two integrated circuits (ICs). The first IC (pink) is connected to the substrate (808) via intra-chip wire bonds (812) and die bonds (810). The second IC (pink) is connected to the first IC via inter-chip wire bonds (814) and to the substrate (806) via chip-to-pin wire bonds (818) and die pads (804). The entire assembly is covered by a molding (802). Labels include: Module 800, Molding 802, Intra-chip Wire Bond 812, Inter-chip Wire Bond 814, Chip to Pin Wire Bond 818, Pin 820, Die Bond 810, Active or Passive IC Substrate 808, Die Pad 804 Active or Passive IC Substrate 806, and package substrate. FIG. 8 <i>Ichitsubo</i> Fig. 8 (annotated). The packaged module includes an <i>integrated circuit</i> (pink). Specifically, <i>Ichitsubo</i> teaches that a PA and bias circuit, plus more circuitry (e.g., impedance matching 18/19, power sensor 26), are “integrated on an integrated circuit (IC)” conventionally in the form of a “semiconductor integrated circuit (IC) chip or die” (<i>integrated circuit</i>) (pink). <i>Ichitsubo</i> ¶¶25, 38. Under Complainant’s construction, an IC can include integration across multiple dies, but that does not distinguish the art, which likewise discloses a packaged module having multiple chips integrated therein on a common package substrate: Thus, even under Complainant’s one-or-more-chip construction, <i>Ichitsubo</i> not only literally discloses that (since it discloses all the claimed components on one chip) but the relaxed/reduced

Claim Language	<i>Ishimaru Alone and/or in Combination with Other References</i>
	degree of integration would be even more easily accomplished on multiple dice for the same reasons (e.g. miniaturization, efficiency) set forth above. As illustrated in Fig. 8, <i>Ichitsubo</i> also teaches that the PA module has a variety of “module substrate 12” (<i>package substrate</i>) (orange) types, including a “multilayer printed circuit board (PCB), lead frame, lower-temperature co-fired ceramics (LTCC), or other suitable electronic materials.” This “RF power amplifier module includes a multi-layer three-dimensional substrate” and this substrate “has one or more upper layers adapted to receive the amplifier chip” (<i>integrated circuit attached to the package substrate</i>). <i>Ichitsubo</i> ¶25, 29, 84. FIG. 8

Ichitsubo Fig. 8 (annotated).

Claim Language	<i>Ishimaru Alone and/or in Combination with Other References</i> <i>Ichitsubo</i> discloses advantages of the “radio frequency (RF) power amplifiers (PA) module,” where “[t]he PA module provides a unitary or common component which may be conveniently assembled in a RF transmission device, with correspondingly simplified assembly, compact 3D size, and enhanced RF amplification performance.” <i>Ichitsubo</i>, ¶¶ 2, 24. <u><i>Ishimaru in view of Johnson</i></u> To the extent that Complainant argues that <i>Ishimaru</i> does not explicitly state that power amplifier (green) and bias circuits (light blue) in a “radio communication device” would be implemented in an integrated circuit attached to a package substrate in a packaged module as claimed, it would have been obvious to implement <i>Ishimaru</i>’s PA (green) and bias circuit (light blue) in the form of an integrated circuit attached to a package substrate as part of a packaged module in view of <i>Johnson</i>, for the reasons described above below. <i>Johnson</i> discloses: Fig. 12. Principle PA circuit schematic. <i>Johnson</i>, Fig. 12 (showing PA schematic of the major components on the BiCMOS HBT die).
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Claim Language	Ishimaru Alone and/or in Combination with Other References
	Fig. 17. EDGE FEM die, including two PAs, an antenna switch, and an AM modulator using PMOS. <i>Johnson</i>, Fig. 17, p. 1612 (showing photo of die (<i>integrated circuit</i>) containing modulator, power amplifiers, biasing circuits, switch, and associated circuitry) <i>Johnson</i> discloses a “die” (<i>integrated circuit</i>) that is flip chip mounted onto a “low-temperature-cured ceramic (LTCC) provide a very low thermal resistance” (<i>a package substrate</i>) the substrate surface, thereby providing extremely low parasitic inductance and good thermal conductivity together with a small footprint.” <i>Johnson</i> further discloses that the SiGe BiCMOS flip chip (<i>integrated circuit</i>) together with “LTCC” (<i>the package substrate</i>) “is a very strong path for PA modules.” (<i>package module</i>). <i>Johnson</i>, p. 1612. “The combined module exhibits superior performance and stability together with a low component count for the entire front-end solution.” <i>Johnson</i>, p. 1612.

Motivation to Combine

A POSITA would have been motivated to combine *Ishimaru*'s teaching of a PA and bias circuit with *Ichitsubo*'s or *Johnson*'s packaging teachings of implementing a PA and bias circuit on an IC attached to a package substrate in a packaged module for at least the following reasons.

First, the combination involves nothing more than using *Ichitsubo* or *Johnson* as an express disclosure of the type of IC packaging that a POSITA already understands would be used for *Ishimaru* in view of the general knowledge in the art. Nothing about the structures, methods or concepts disclosed in *Ishimaru* would need to be changed to implement *Ishimaru*'s power amplifier and bias circuit on a packaged IC—that is understood and expected of *Ishimaru* when incorporating it into a wireless communications device.

Second, as described in the State of the Art (App. A-03, §II.C), a POSITA would have been motivated by any one of the numerous and well-known advantages of packaged ICs, which are demanded by the electronics market, including: decreased size, cost and power consumption, increased reliability and durability, and ease of manufacturing and assembly. The combination involves nothing more than following the well-established path of commercial circuit integration and packaging for the same benefits that have made packaged ICs dominate the electronics industry, such as protecting the chip from the environment and allowing easy connections; indeed, to make the chip “useful.” *Laplante* 503. Given the market demands and practices, a POSITA would have been readily motivated to package *Ishimaru*'s power amplifier and bias circuit using the packaged IC teachings of *Ichitsubo* or *Johnson*. More specifically:

A POSITA was very familiar with packaged modules and package substrates, and their readily apparent benefits of IC(s) on a package substrate, in terms of protection, durability, smaller size, smaller cost, and greater stability provided. *See* State of the Art (App. A-03 § II.C.2)

A POSITA was very familiar with ICs, and their readily apparent benefits of integrating components onto them in terms of smaller size, smaller cost, and greater stability provided by single integrated circuit. *See* State of the Art (App. A-03 § II.C.1). Furthermore, it was well-known to implement a power amplifier module and a biasing circuit on a single integrated circuit. *See* State of the Art (App. A-03, § II.C.1)

Claim Language	Ishimaru Alone and/or in Combination with Other References
	(discussing, e.g., ECP052 data sheet, <i>Marra, Hedberg, Johnson, Ichitsubo, Tsurumaki</i>); See also <i>Morisawa</i> Claim Chart at Appendix B-02 (power amplifier and bias circuitry on a single integrated circuit). Third, a POSITA would have also been motivated by the express teachings, suggestions, and motivations of <i>Ichitsubo</i> and <i>Johnson</i> themselves. For example, a POSITA would have been motivated by <i>Ichitsubo</i>'s description of a "radio frequency (RF) power amplifiers (PA) module" for use in wireless devices being "developed in ever decreasing size for convenience of use," and teaching of a "compact 3D size" PA module having "enhanced amplification performance" that "can be used in a wide range [of] wireless communication devices such as cellular phone[s], mobile computers, and handheld wireless digital devices." <i>Ichitsubo</i> ¶¶2, 24, 35. <i>Ichitsubo</i> explains that its solution to these problems – a unitary PA module "which may be conveniently assembled in a RF transmission device" – has advantages including "minimiz[ing] device count and/or printed circuit board real estate," "simplified assembly, compact 3D size, and enhanced RF amplification performance." <i>Id.</i> ¶¶9, 24, 25. In other words, <i>Ichitsubo</i> expressly teaches benefits of packaging readily applicable to <i>Ishimaru</i>'s PA and bias circuit for its intended use with "radio communication devices." <i>Ishimaru</i> Abstract. A POSITA would have been motivated to follow these teachings in <i>Ichitsubo</i> to predictably achieve a compact, reliable fabrication of <i>Ishimaru</i>'s PA and bias circuit. <i>Id.</i> ¶¶42-52; <i>Ichitsubo</i> ¶¶8, 25. With respect to <i>Johnson</i>, <i>Johnson</i> taught multiple advantages, that would motivate adoption of its teachings, in whole or in part: "SiGe BiCMOS technology is finding increasing use in wireless PA applications. The favorable thermal properties, volume manufacturing capability, and design automation support of SiGe BiCMOS technology have long been recognized. Detailed investigation of the SOA analysis of SiGe HBTs reveals favorable device ruggedness for PA applications." <i>Johnson</i>, p. 1612. "PA designs have been demonstrated for GSM, GPRS, and EDGE wireless standards using a SiGe HBT technology specifically tailored to meet the divergent requirements of high VSWR robustness at high output power and high linearity. The GPRS/EDGE FEM shown here exceeds the 15:1 VSWR requirement at 33 dBm with an overall efficiency of 37%. The SiGe HBT was

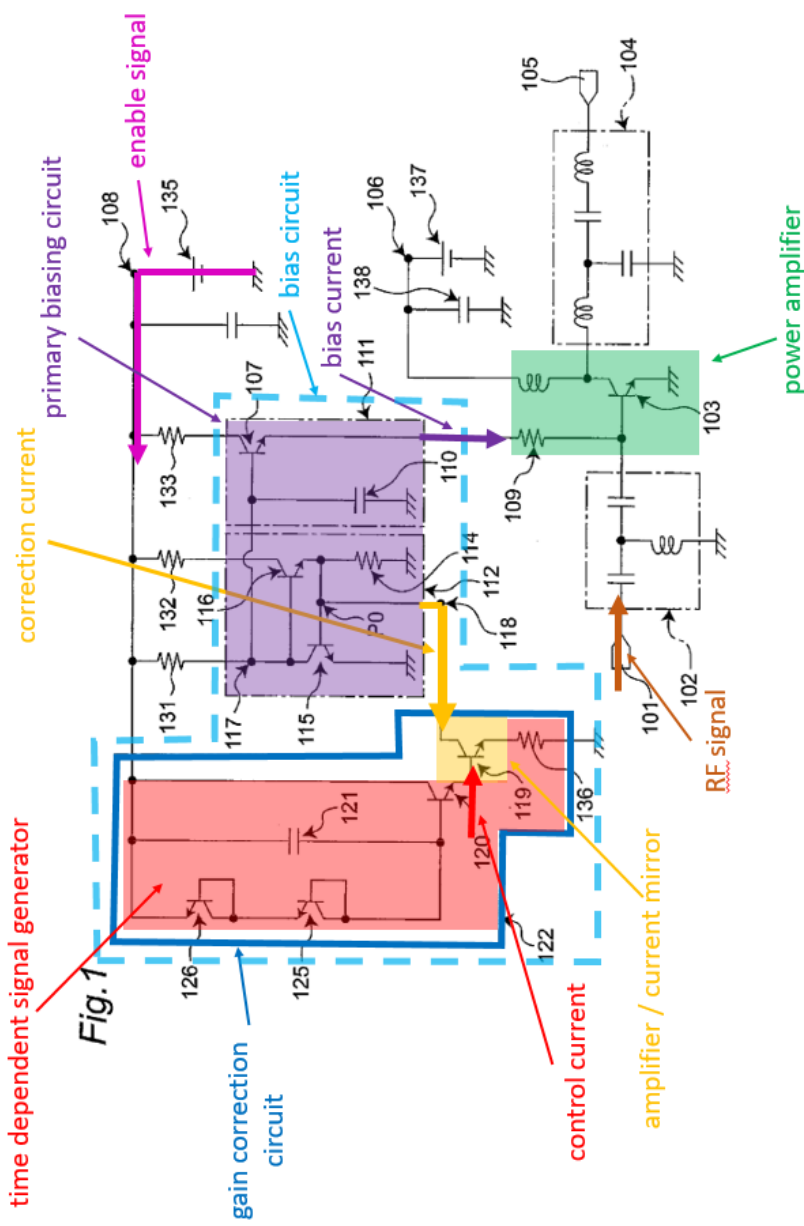
Claim Language	<i>Ishimaru</i> Alone and/or in Combination with Other References
	optimized to simultaneously provide ruggedness and speed and is compatible with the base 0.5 μm CMOS. The favorable thermal properties, lower cost of wafer processing, and the higher integration capabilities demonstrated by these SiGe PAs make them a compelling choice for wireless applications. A SiGe BiCMOS flip-chip together with LTCC is a very strong path for PA modules. The combined module exhibits superior performance and stability together with a low component count for the entire front-end solution.” <i>Johnson</i>, p. 1612. “Excellent power control is achieved with on-chip PMOS, which regulates the PA collector voltage in the FEM.” <i>Johnson</i>, 1610. A POSITA would have understood additional benefits of combining a BiCMOS teaching, such as <i>Johnson</i> or <i>Ichitsubo</i>. See, e.g., <i>Illingworth</i> defines BiCMOS as “[i]ntegrated circuits that contain both bipolar junction transistors and complementary MOS transistors (CMOS). The combination of both types of device on the same chip has a wide variety of functions and allows the advantages of both processes to be exploited.” <i>Illingworth</i>, p. 38-39. “BiCMOS circuits provide improved system performance and a reduction in the number of components, hence reduced chip sizes and lower costs.” <i>Illingworth</i>, p. 39. <u>Fourth</u>, the modification would combine prior art elements (<i>Ishimaru</i>’s disclosures combined with well-understood and known techniques of mounting an integrated circuit on a package substrate) to yield predictable results (providing a commercially suitable and stable platform to provide connections from the IC to other components). Doing so would involve nothing more than using a known technique (providing the structural and electrical support for an IC) to implement a known solution (package substrates) to achieve predictable results (providing a commercially suitable and stable product environment for an IC). <u>Further</u>, the modification would have been within the capabilities of POSITA and viewed as having a reasonable expectation of success. A POSITA would have a reasonable expectation of success in implementing <i>Ishimaru</i>’s teachings following <i>Ichitsubo</i>’s of <i>Johnson</i>’s packaging teachings of a PA module because implementing a power amplifier on an IC inside a packaged module was no more than the routine exercise of skill for a POSITA making the PA module

Claim Language	Ishimaru Alone and/or in Combination with Other References
[14b.1] a power amplifier configured to provide amplification to a radio frequency signal and	simpler and more cost effective. State of the Art (App. A-03, § II.C) (e.g. <i>Marra</i> ¶¶65-68; <i>Johnson</i> 1609, 1612). A POSITA understood that the implementation of <i>Ishimaru</i>'s speedup circuit facilitated the use of resistors and capacitors of suitable size that could advantageously be implemented in an on-chip integration with the PA. <i>Ishimaru</i>'s transistors 119/120 provide amplification to the current that charges capacitor 121 and flows to ground through resistor 136. <i>Ishimaru</i> Fig. 1, ¶¶55-56. Owing to the very high gain of transistors 119/120, the current in the capacitor can be made very small, and therefore the capacitor 121 can be made small for a given time constant. Likewise, the size of resistor 136 can be small as the capacitor current (I_{C121}) is generally the resistor current (I_{R136}) divided by the gain of transistors 119 and 120. This is consistent with the disclosure of the '563 Patent, which describes how amplifying $I_{CONTROL}$ with amplifier 73 allows one to "reduce a magnitude of the resistor and/or capacitor needed to generate a suitable correction current, thereby permitting the time-dependent signal generator 72 to be integrated on-chip with the power amplifier 32." '563 Patent 14:36-41. Nor is there anything counterintuitive, technologically challenging, or unique about the notion of the claimed integration and packaging. The specification of the '563 Patent only briefly describes the packaging involved, and does so at a high level of generality, without providing any technological solutions or advances in the technology of IC fabrication or packaging. '563 Patent 14:9-15:8, Figs. 10A, 10B. This lack of detail in the '563 Patent is not surprising given the well-developed state of the art for ICs and packaging as discussed above. State of the Art (App. A-03, § II.C).
[14b.1] a power amplifier configured to provide amplification to a radio frequency signal and	<i>Ishimaru</i> discloses a power amplifier configured to provide amplification to a radio frequency (RF) signal. See, e.g.: <i>Ishimaru</i> discloses "a high-frequency power amplifier to be used in radio communication devices." <i>Ishimaru</i> ¶1. The circuitry for the power amplifier includes "an amplification section having a first transistor for performing power amplification" (<i>green</i>) (<i>a power amplifier configured to provide amplification</i>), as well as "a bias power source section" and "a speedup circuit." <i>Ishimaru</i> ¶¶10-12. As illustrated in Figure 1 (annotated below), <i>Ishimaru</i> further

Claim Language

Ishimaru Alone and/or in Combination with Other References

discloses that “a high-frequency signal as an input signal [is] inputted from an input signal terminal 101, ... is amplified by an amplifier transistor 103 serving as a first transistor, and then, ... outputted from an output signal terminal 105.” *Ishimaru* ¶42.

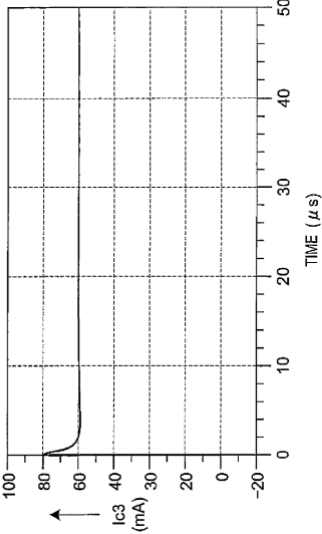


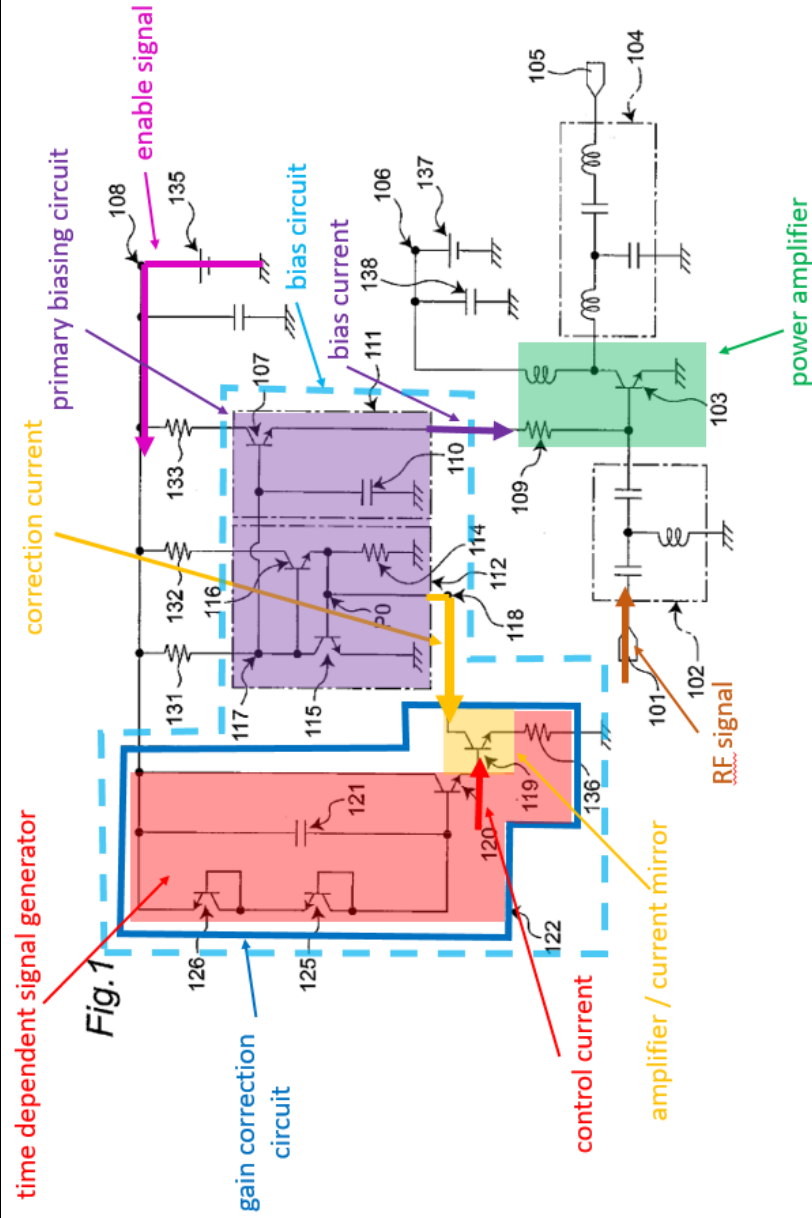
Ishimaru Fig. 1 (annotated).

Because *Ishimaru* is directed to a PA for a **radio** communications device, a POSITA reading *Ishimaru* understood that the high-frequency input signal at input terminal 101 is a *radio*

Claim Language	<i>Ishimaru</i> Alone and/or in Combination with Other References
	<i>frequency signal</i> (brown arrow) for amplification by amplifier transistor 103 (<i>a power amplifier configured to provide amplification</i>) to generate an amplified radio frequency signal at output terminal 105. <i>Ishimaru</i> discloses: “The present invention relates to power amplifiers and, for example, to a high-frequency power amplifier to be used in radio communication devices or the like.” <i>Ishimaru</i> at ¶ 1. “FIG. 1 is a circuit diagram showing a circuit construction in an embodiment of the power amplifier of the invention. In this power amplifier, a high-frequency signal as an input signal inputted from an input signal terminal 101, passing through an input matching circuit 102, is amplified by an amplifier transistor 103 serving as a first transistor, and then, after passing through an output matching circuit 104, outputted from an output signal terminal 105. In FIG. 1, reference sign 106 denotes a collector bias terminal of the amplifier transistor 103. Between the collector bias terminal 106 and the ground are connected a DC power source 137 and a capacitance element 138. The amplifier transistor 103 forms an amplification section.” <i>Ishimaru</i> at ¶¶ 41 - 42. “Technical Problem Accordingly, an object of the present invention is to provide a power amplifier which is capable of suppressing distortion increases of an amplification signal due to heat generation upon start-up without using any temperature sensing element.” <i>Ishimaru</i> at ¶¶ 6-7. “Solution to Problem In order to achieve the above object, there is provided a power amplifier comprising: an amplification section having a first transistor for performing power amplification; a bias power source section having a second transistor for feeding a bias to the first transistor; and a speedup

Claim Language	<i>Ishimaru</i> Alone and/or in Combination with Other References
	circuit for transiently increasing the bias fed to the first transistor by bias power source section at a start of the power amplification.” <i>Ishimaru</i> at ¶¶ 8-12. “In the power amplifier of the invention, at a start of power amplification by an amplifier transistor 103 serving as an amplification section, a speedup circuit 122 transiently increases a bias which is fed to the amplifier transistor 103 via a bias power source section composed of a bias circuit 111 and a power source circuit 112. As a result, the power amplification factor of the amplifier transistor 103 is transiently increased at the start of power amplification by the amplifier transistor 103. Thus, the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal such as a modulated-wave signal. Accordingly, in the invention, it becomes possible to suppress distortion increases of an amplification signal due to heat generation at the start time without using any temperature sensing element.” <i>Ishimaru</i>, Abstract; see also ¶¶ 7, 13, Fig. 1. “Next, FIG. 3 shows an example (simulation result) of transient response of the operating current (collector current Ic3) of the amplifier transistor 103 in the power amplifier of this embodiment. In this embodiment, the current to be fed from the bias transistor 107 to the amplifier transistor 103 is forcibly increased at turn-on of the amplifier, with the result that the value of the operating current Ic3 comes to a steady state in about 4 the time of transient response of the comparative example of FIG. 2. Thus, occurrence of distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed, so that the linearity of the circuit in burst operation is improved. That is, gain variations due to collector current variations of the power amplifier using a bipolar transistor can be compensated.” <i>Ishimaru</i> at ¶ 54, Fig. 1, Fig. 2, Fig. 3. “In the power amplifier of this embodiment also, the capacitance value of the capacitance element 121 of the speedup circuit 122 is adjusted so as to cancel transient variations in gain due to the temperature variations at a start of power amplification. As a result of this, deterioration of

Claim Language	Ishimaru Alone and/or in Combination with Other References
	the linearity due to variations of amplification gain can be canceled so that the value of dynamic EVM (error vector magnitude) can be improved.” <i>Ishimaru</i> at ¶ 55, Fig. 1. Fig.3  The graph shows a current I_{c3} in milliamperes (mA) on the y-axis (ranging from -20 to 100) against time in microseconds (μs) on the x-axis (ranging from 0 to 50). The curve starts at 0 mA at 0 μs, rises sharply to a peak of approximately 80 mA, and then gradually decreases to about 60 mA by 50 μs. <i>Ishimaru</i>, Fig. 3.
[14b.2] a bias circuit configured to receive a power amplifier enable signal and to generate a bias signal that biases the power amplifier, the bias circuit including	<i>Ishimaru</i> discloses a bias circuit configured to receive a power amplifier enable signal and to generate a bias signal that biases the power amplifier. See, e.g.: <i>Ishimaru</i> discloses a “speedup circuit 122”, “power source circuit 112”, and “bias circuit 111” (collectively a bias circuit) (light blue) that receives “a control voltage source 135” (power amplifier enable signal) (pink arrow) and supplies a “base bias current” (generate a bias signal) (purple arrow) to the “bias terminal of amplifier transistor 103” (biases the power amplifier) (green). <i>Ishimaru</i> Abstract, ¶¶24, 31, 49-52.



Ishimaru, Fig. 1 (annotated).

Ishimaru discloses that the control voltage from control voltage source 135 at bias terminal 108 “controls turn-on and -off of power amplification.” Ishimaru ¶24. Thus, Ishimaru’s control voltage is a *power amplifier enable signal*. As explained in limitations [14b.2.a-b] below, Ishimaru further discloses that, in response to the control voltage from source 135 being turned on (*power amplifier enable signal*), the I_{BIAS} (*bias signal*) that is applied to the base of amplifier transistor 103 transiently (temporarily) increases due to the operation of the speedup circuit 122,

Claim Language	Ishimaru Alone and/or in Combination with Other References
	power source circuit 112, and bias circuit 111 (<i>configured to . . . generate a bias signal that biases the power amplifier</i>). <i>Ishimaru</i> ¶31. <i>Ishimaru</i> discloses: “Also, a bias transistor 107 as a second transistor is a transistor that supplies a base bias current to a base terminal of the amplifier transistor 103. An emitter of the bias transistor 107 is connected to a base terminal of the amplifier transistor 103 via a resistance element 109. The resistance element 109 is a ballast (stabilization) resistor which is inserted in a base bias channel to prevent thermal runaway of the amplifier transistor 103.” <i>Ishimaru</i> at ¶43. “The bias transistor 107 has its collector connected to a bias terminal 108 via a resistance element 133. The bias terminal 108 is connected to a control voltage source 135.” “A bias circuit 111 composed of the bias transistor 107 and a capacitance element 110 connected to a base terminal of the bias transistor 107 has a function of increasing the base bias current in response to an increase in signal strength of the input signal, and functions to keep the amplification ratio of an output signal as well as its phase rotation after amplification constant even when the signal strength of the input signal has changed.” <i>Ishimaru</i> at ¶¶44-45. “A power source circuit 112 is connected to the base terminal of the bias transistor 107 of the bias circuit 111. The bias circuit 111 and the power source circuit 112 constitute a bias power source section. The power source circuit 112 feeds generally a sum of a “base-emitter voltage” of the amplifier transistor 103 and a “base-emitter voltage” of the bias transistor 107 to the base terminal of the bias transistor 107. That is, the power source circuit 112 feeds a voltage double the base-emitter voltage (hereinafter, referred to as VBE) of a transistor used in the power source circuit 112 to the base terminal of the bias transistor 107. It is noted that voltage drops of the ballast resistor 109 are neglected in this case.” <i>Ishimaru</i> at ¶¶46-47.

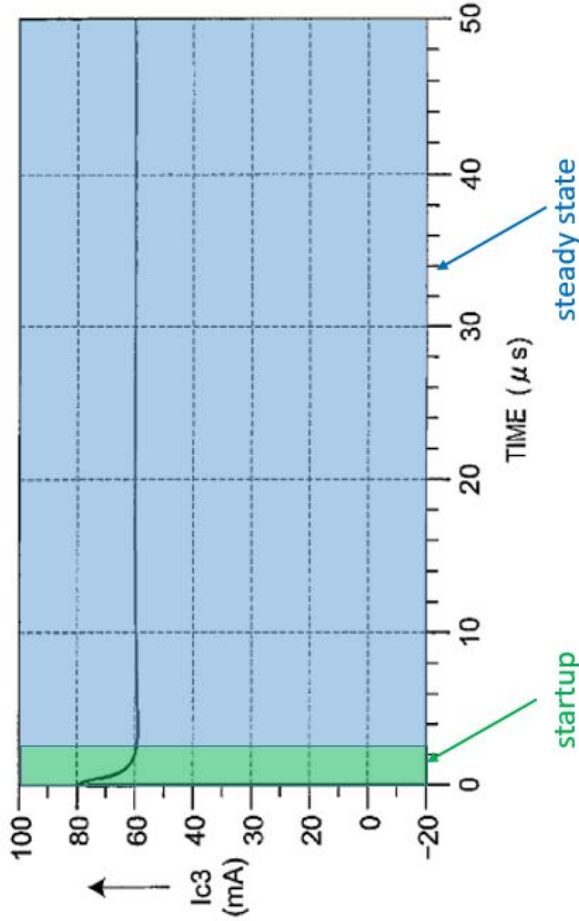
Claim Language	<i>Ishimaru</i> Alone and/or in Combination with Other References
	“In this embodiment, as shown in FIG. 1, the power source circuit 112 has a third transistor 115, a fourth transistor 116, and a resistance element 114. The third transistor 115 has its collector connected to the base of the bias transistor 107 and its emitter connected to the ground. Also, a base of the third transistor 115 is connected to an emitter of the fourth transistor 116. The collector of the third transistor 115 is connected to the bias terminal 108 via a resistance element 131. Meanwhile, the fourth transistor 116 has its emitter connected to the ground via the resistance element 114 and its collector connected to the bias terminal 108 via a resistance element 132.” <i>Ishimaru</i> at ¶ 48. “A connecting point P0 between the base of the third transistor 115 and the emitter of the fourth transistor 116 in the power source circuit 112 is connected to an output terminal 118 of a speedup circuit 122. The speedup circuit 122 has a fifth transistor 119 whose collector is connected to the output terminal 118, and a sixth transistor 120 whose emitter is connected to a base of the fifth transistor 119. The emitter of the fifth transistor 119 is connected to the ground via a resistance element 136. The speedup circuit 122 also has a capacitance element 121 which is connected between a base of the sixth transistor 120 and the bias terminal 108, and two diodes 125, 126 which are connected in series between the base of the sixth transistor 120 and the bias terminal 108. In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is

Claim Language	Ishimaru Alone and/or in Combination with Other References
	With reference to Figure 1 (annotated) above, <i>Ishimaru</i> discloses a speedup circuit 122 (a gain correction circuit) (dark blue) that includes a capacitance element 121, diodes 125 and 126, transistors 119 and 120, and resistance element 136. <i>Ishimaru</i> ¶¶50-51. In response to the “rise time of the control voltage source 135 (at turn-on of the amplifier)” (in response to activation of the power amplifier enable signal) (pink arrow), the speedup circuit applies a transient or time-varying current to the base of transistor 119 (control current) (red arrow). <i>Ishimaru</i> ¶52. This is a control current at least because it is used to control the correction to the biasing of <i>Ishimaru</i>’s power amplifier to compensate for gain variation, as discussed next. This $I_{CONTROL}$ (red arrow) is mirrored and amplified by transistor 119, resulting in a transient current being pulled into the collector of transistor 119 from node 118, a correction current, $I_{CORRECTION}$ (gold arrow). <i>Ishimaru</i> ¶52. <i>Ishimaru</i>’s speedup circuit 122 (dark blue) is a gain correction circuit in that it is a circuit for gain correction of <i>Ishimaru</i>’s power amplifier (green) and is configured to generate a control current in response to activation of the power amplifier enable signal and to mirror the control current to generate a correction current, as already explained. The speedup circuit 112 (dark blue) shapes the $I_{CORRECTION}$ (gold arrow) as a “current that transiently (temporarily) flows” out of the power amplifier’s primary biasing circuit (purple). <i>Ishimaru</i> ¶52. This $I_{CORRECTION}$ (gold arrow) is shaped in an amount and duration necessary to cause the primary biasing circuit to send a corresponding temporary boost in I_{BIAS} to the power amplifier (green) to boost its gain during the startup period when it would otherwise be too low, i.e. to correct for the gain variation of the power amplifier. <i>Ishimaru</i> ¶52. More specifically: Thus, occurrence of distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed, so that the linearity of the circuit in burst operation is improved. That is, gain variations due to collector current variations of the power amplifier using a bipolar transistor can be compensated.

Ishimaru ¶54.

The speedup circuit/gain correction circuit (dark blue) achieves this power amplifier gain correction by shaping the $I_{CORRECTION}$ (gold arrow) to cause a temporary voltage increase at the base of transistor 107 in the primary biasing circuit (purple), which transiently boosts the amount of “bias base current” (bias signal), i.e., an I_{BIAS} (purple arrow) supplied to bias the power amplifier’s amplifier transistor 103 (green). Ishimaru ¶52. That transiently boosts the gain of the power amplifier based on the $I_{CORRECTION}$, compensating for the low gain of power amplifier at startup. Ishimaru ¶52. This boost is shown by the increased collector current through amplifier transistor 103 during startup shown in Figure 3 of Ishimaru. Ishimaru Fig. 3.

Fig.3

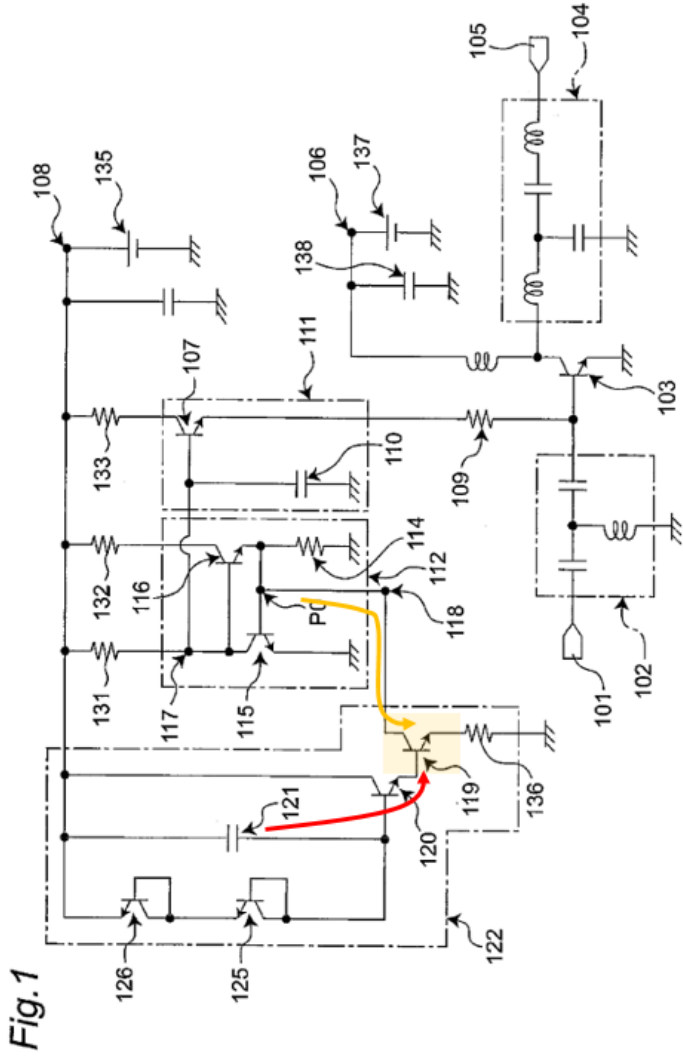


Claim Language	Ishimaru Alone and/or in Combination with Other References
	Ishimaru Fig. 3 (annotated). Thus, a POSITA reviewing <i>Ishimaru</i> understood that the base current applied to transistor 119 is an $I_{CONTROL}$ (red arrow) because it controls generation of transistor 119's collector current $I_{CORRECTION}$ (gold arrow), which, in turn, ultimately controls I_{BIAS} (purple) generated by bias circuit 111 that is applied to the base of amplifier transistor 103, thus leading to the transient increase in the collector current through the power amplifier transistor to correct the gain of the power amplifier. <u>Mirror the Control Current / Current Mirror</u> <i>Ishimaru</i>'s transistor 119 (the <i>current amplifier</i>) is a <i>current mirror</i> that is configured to replicate (i.e. configured to mirror (gold)) the $I_{CONTROL}$ (red arrow) to generate the $I_{CORRECTION}$ (gold arrow), as shown in Fig. 1, partially reproduced below: The diagram shows a transistor symbol labeled '119'. A red arrow labeled 'control current' points to the base of the transistor. A gold arrow labeled 'correction current' points to the collector of the transistor. A label '119' points to the transistor symbol. A label 'amplifier / current mirror' points to the transistor symbol.

Claim Language	Ishimaru Alone and/or in Combination with Other References
	Ishimaru Fig. 1 (annotated) (partial). Consistent with the discussion of current mirrors in the State of the Art section, transistor 119 as connected in <i>Ishimaru</i> is configured to mirror in that it is configured to replicate (reproduce, duplicate, reflect, etc.), <i>i.e.</i>, <i>mirror</i> the current at its input (the base of transistor 119) to generate the current at its output (the collector of transistor 119). State of the Art (Appendix A-03, § II.B); <i>Ishimaru</i> Fig. 1. When connected as shown in <i>Ishimaru</i>, transistor 119 takes the general, three-node form set out by Barrie Gilbert and Gray for a <i>current mirror</i>. <i>Gilbert</i> Fig. 6.1a; <i>Gray</i> Fig. 4.1. Accordingly, in the side-by-side images below, <i>Ishimaru</i>'s transistor 119 is used as a current mirror in that node N1 (of <i>Gilbert</i> Figure 6.1a showing a current mirror) is the base of transistor 119, N2 the collector of transistor 119, and N0 the emitter of transistor 119, with the circuit replicating (and scaling) current I1 to generate output current I2. <i>Gilbert</i> 242, Fig. 6.1a; <i>Gray</i> Fig. 4.1. The diagram consists of two side-by-side circuit schematics. The left schematic, labeled (a), shows a transistor with base node N1, collector node N2, and emitter node N0. A red arrow labeled I1 points into node N1, and a yellow arrow labeled I2 points out of node N2. The right schematic shows a similar transistor configuration with nodes N1, N2, and N0, and currents I1 and I2. The two diagrams are used to compare the current mirror configuration in Ishimaru with the one in Gilbert. <i>Gilbert</i> 240, Fig. 6.1a (annotated) <i>Ishimaru</i> Fig. 1 (annotated) (partial)

Claim Language	<i>Ishimaru</i> Alone and/or in Combination with Other References Likewise, <i>Ishimaru</i>'s transistor 119 is connected and used in the same way as <i>Gilbert</i>'s single transistor current mirror shown in his Figure 6.2a. <i>Gilbert</i> 243, Fig. 6.2a (annotated) <i>Ishimaru</i> Fig. 1 (annotated) (partial) In addition to the replication discussed above, <i>Ishimaru</i>'s current mirror is further configured to amplify the $I_{CONTROL}$, scaling it up by the amplification factor to form $I_{CORRECTION}$, namely scaling by the common-emitter current-gain, β, of the transistor 119, which quantifies the "mirror ratio" (discussed below) of <i>Ishimaru</i>'s current mirror. State of the Art (App. A-03, § II.B), <i>Illingworth</i> 38; <i>Gilbert</i> 242-243. The current at the collector (I_{C119}) of transistor 119 (a transistor having β_{119} is generally related to the current at the transistor's base (I_{B119}) by the equation: $I_{C119} = \beta_{119} * I_{B119}$. Thus, the ratio of the input current I_{B119} to the output current I_{C119} is generally β_{119}. The gain through the transistor is the "mirror ratio", "M", by which <i>Ishimaru</i>'s current mirror scales the $I_{CONTROL}$ to generate the $I_{CORRECTION}$. <i>Gilbert</i> 242-243; <i>Ishimaru</i> Fig. 1. The gain of transistor 119 can be configured to a target value by designing the voltage and current biasing of the transistor 119 (within the constraints of the circuit), such that a β in a range, e.g., of about 60 to 150 or
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Claim Language	Ishimaru Alone and/or in Combination with Other References
	more, can be achieved. The time constant of the transient can then be tuned through the choice of components, namely C121 and R136. <i>Ishimaru</i> ¶¶55-56. Thus, transistor 119 as connected in <i>Ishimaru</i> is a <i>current mirror</i> in that it constitutes a circuit configured to mirror a current, which can be configured to achieve a target gain. Transistor 119 is a circuit that has electrical interconnections, including input/output, and other connections that permit current to flow through the circuit. <i>Ishimaru</i> thus discloses a speedup circuit 122 for correcting the gain of the PA (<i>a gain correction circuit</i>) (dark blue) that, in response to “a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier)” (<i>in response to activation of the power amplifier enable signal</i>) (pink arrow), generates a transient or time-varying current via capacitor 121 that is amplified (by transistor 120) and applied to the base of transistor 119 (<i>generate a control current</i>) (red arrow) that is replicated, <i>i.e.</i>, mirrored (and scaled up) at the collector of transistor 119 in the form of a transient or time-varying current (<i>mirror the control current to generate a correction current</i>) (gold arrow) that is pulled from node 118 to affect the generation of I_{BIAS} (<i>bias signal</i>) (purple arrow) applied to the base of amplifier transistor 103. <u>Ishimaru in view of Harrison discloses this limitation.</u> To the extent Complainant asserts that <i>Ishimaru</i> does not disclose mirroring a current, <i>Ishimaru</i> in view of <i>Harrison</i> discloses this limitation. As discussed above for this limitation, <i>Ishimaru</i> discloses a speedup circuit 122 that responds at “a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier)” to generate a time-varying current via capacitor 121 that is amplified by 120 and 119. Furthermore, as illustrated in the annotated Figure 1, below, a POSITA recognizes that <i>Ishimaru</i> uses the amplified version of the current (red arrow) as a current sink to pull a specifically shaped correction current (gold arrow) out of the primary biasing circuit.



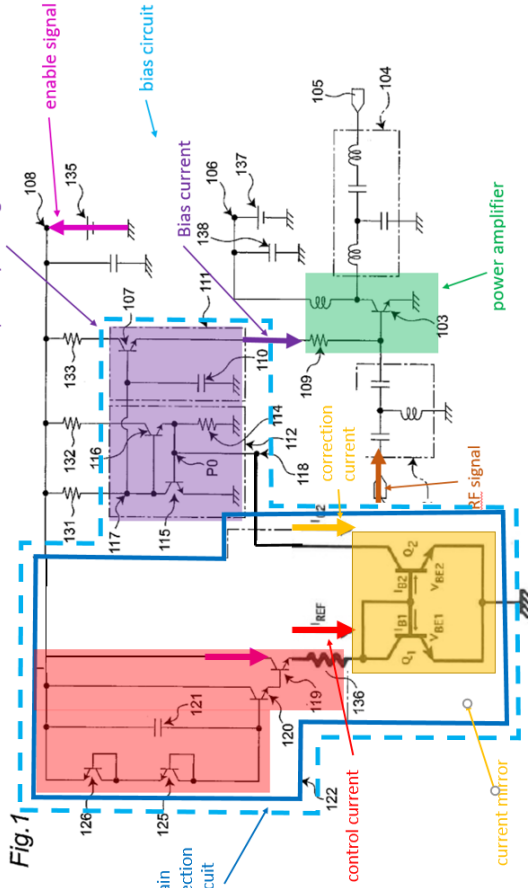
Ishimaru Fig. 1 (annotated).

A POSITA readily recognizes the coupling of the left and right sides of *Ishimaru*'s circuit as involving a current source generated on the left side that is replicated as a current sink on the right side, which is a coupling that takes the general form of a *current mirror* (i.e. transistor 119 as discussed above for this limitation).

A POSITA further recognizes that the current source / current sink coupling of *Ishimaru* would be well suited for, and ready for improvement by, the use of additional current mirror structures

Claim Language	<i>Ishimaru</i> Alone and/or in Combination with Other References
	to couple the two sides of <i>Ishimaru</i>'s circuit to achieve the well-known benefits of such current mirrors. In that regard, <i>Harrison</i> teaches a well-known "basic" current mirror using NPN transistors that operates as a "mirror-sink," as shown in the excerpt of Figure 4.18 below: <i>Harrison</i> 71, Fig. 4.18. As shown in Fig. 4.18, <i>Harrison</i>'s current mirror has at least two transistors (Q1 and Q2) with their base terminals tied together. <i>Harrison</i> 71, Fig. 4.18. Further, <i>Harrison</i>'s current mirror is a circuit configured to mirror I_{REF} to I_{C2}, and is configurable to achieve a target gain that can be finely tuned by adjusting the ratio of the transistor sizes. <i>Harrison</i> 95 (describing "current

Claim Language	<i>Ishimaru</i> Alone and/or in Combination with Other References
	scaling” by setting the ratio of the emitter area). See also <i>Gilbert</i> 280; <i>Gray</i> 254, 257; <i>Grebene</i> 172. A POSITA would recognize modifying the speedup circuit as taught by <i>Ishimaru</i> to add a basic current mirror as taught by <i>Harrison</i> would be beneficial because it provides flexibility in allowing a broader range of voltages and a broader range of amplification due to the ability to achieve the desired current amplification by changing the ratios of transistor sizes in the basic current mirror. See <i>State of the Art</i> (App. A-03, § II.B). Obviousness does not require bodily incorporation of references or building an actual circuit, but the ease with which a POSITA would advantageously apply <i>Harrison</i>’s teaching to <i>Ishimaru</i> as illustrated below in the following annotated figures, derived from <i>Ishimaru</i>’s Figure 1 and <i>Harrison</i>’s Figure 4.18. As illustrated above, a basic current mirror such as taught by <i>Harrison</i> can be advantageously added to <i>Ishimaru</i>’s speedup circuit by interposing the basic current mirror at the emitter of transistor 119, and then connecting node P0/118 to the collector of current mirror transistor Q2. The collector of transistor 119 is then connected to the control voltage source (<i>the enable signal</i>).

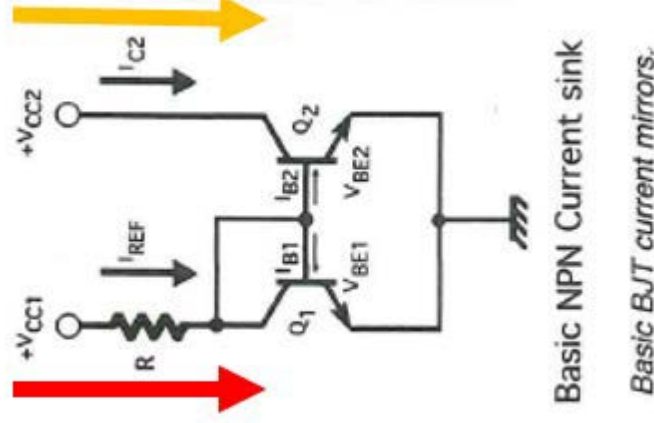


As shown in the above annotations, *Ishimaru*’ speedup circuit modified with *Harrison*’s basic current mirror is a gain correction circuit (dark blue) that responds at “a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier)” in response to activation of the PA enable signal (pink) to generate a transient current signal via capacitor 121 that is amplified by transistors 120 and 119 and passed through resistor 136 to generate a control current (red arrow). *Ishimaru* modified with *Harrison* then takes this amplified time varying current signal (red arrow) and mirrors it using the basic *current mirror* to generate a time-varying correction current (gold arrow) that is pulled from node 118.

A POSITA would have been highly motivated to combine *Ishimaru*’s teaching of a bias circuit for a PA with *Harrison*’s disclosure of a basic current mirror and have a reasonable expectation of success for at least the following reasons:

Harrison discloses a “basic” current mirror. *Harrison* 71. Current mirrors were well-known in the art and were considered “a familiar icon of modern analog design.” *Gilbert* 239. Indeed,

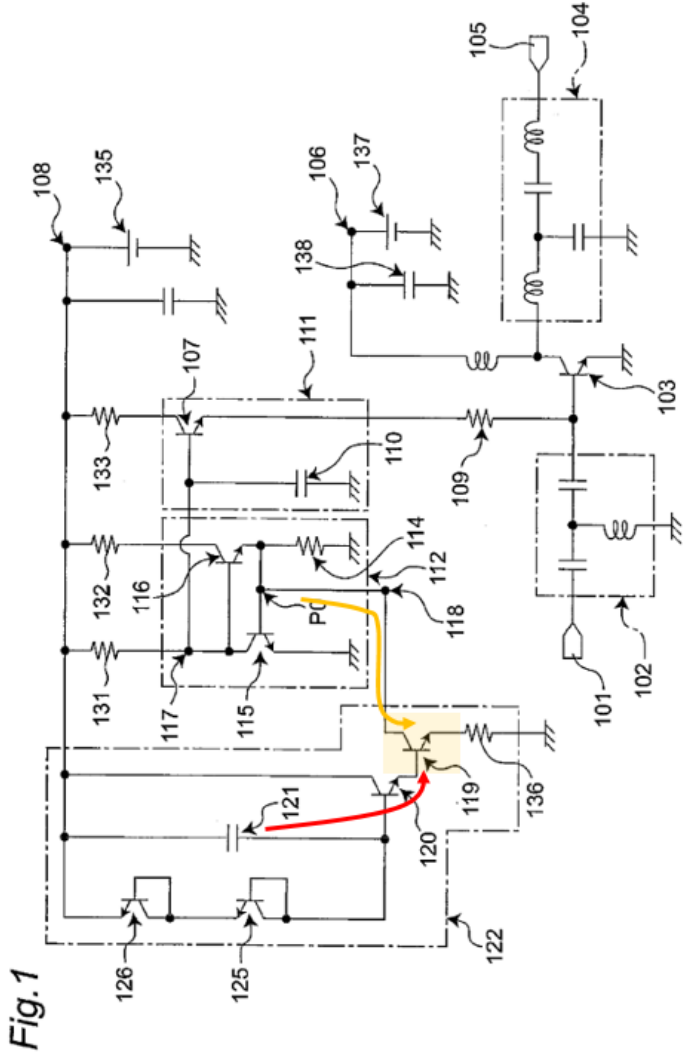
Claim Language	<i>Ishimaru</i> Alone and/or in Combination with Other References
	current mirrors were “widely used in analog integrated circuits” “as biasing elements” and were “particularly useful building blocks for analog circuit design.” <i>Gray</i> 251; <i>Grebene</i> 170. One of these advantages was that current mirrors take a reference current in one branch of a circuit and accurately reproduce or reflect that current in a second branch of that circuit, and can do so “relatively independent of the absolute values of the device parameters.” <i>Grebene</i> 170-171. Thus, current mirrors were useful in coupling circuits together such that an input current could be provided into one branch of a circuit and the current mirror would then replicate (or <i>mirror</i>) that current such that the current mirror would pull a mirrored version of that current out of the second branch of the circuit. <i>Harrison</i> illustrates this configuration (called a current sink), where the input branch is annotated in red and the output branch is annotated in yellow. <i>Harrison</i> 71.



Harrison Fig. 4.18 (annotated).

Further, current mirrors were known to be useful in providing desired current scaling when mirroring a current (called **current mirror gain**) by changing the ratios of transistor sizes. Harrison 95 (describing “current scaling” by setting the ratio of the emitter area). In the case of bipolar junction transistors, this would be done by changing the relative sizes of the emitters of the current mirror transistors. Gray 25. Scaling transistor sizes in current mirrors to achieve granular, targeted levels of scaling that could advantageously be fine-tuned was well understood

Claim Language	Ishimaru Alone and/or in Combination with Other References
	as of the priority date of the '101 Patent, and described in multiple textbooks. See <i>Gray</i> 251-257; <i>Grebene</i> 172; <i>Gilbert</i> 252, 280. In addition, a POSITA understood that <i>Harrison</i>'s two-transistor current mirror would advantageously provide better isolation between the left side and the right side of <i>Ishimaru</i>'s circuit. First, because there are separate emitter currents and paths in the two-transistor mirror, there is a degree of separation between the left and right sides of the circuit. Second, it avoids the issue that using a single transistor like <i>Ishimaru</i>'s 119 as the current mirror has coupling (parasitic) between its base and collector due to standard parasitic capacitance. This coupling across 119 can create unwanted coupling across the transistor, such that noise on one side of the circuit can pass to the other side. Adding <i>Harrison</i>'s two-transistor current mirror does not have this limitation, providing better isolation between the input and output current signals than <i>Ishimaru</i> provides. A POSITA would thus have been motivated to modify the teachings of <i>Ishimaru</i> to add a basic current mirror as taught by <i>Harrison</i> because a POSITA understood that <i>Ishimaru</i>'s circuit is designed to amplify the current that flows through capacitor 121 (annotated in red below) to generate the current sink pulled from node 118 (annotated in yellow). <i>Ishimaru</i> ¶¶50-52, Fig. 1.



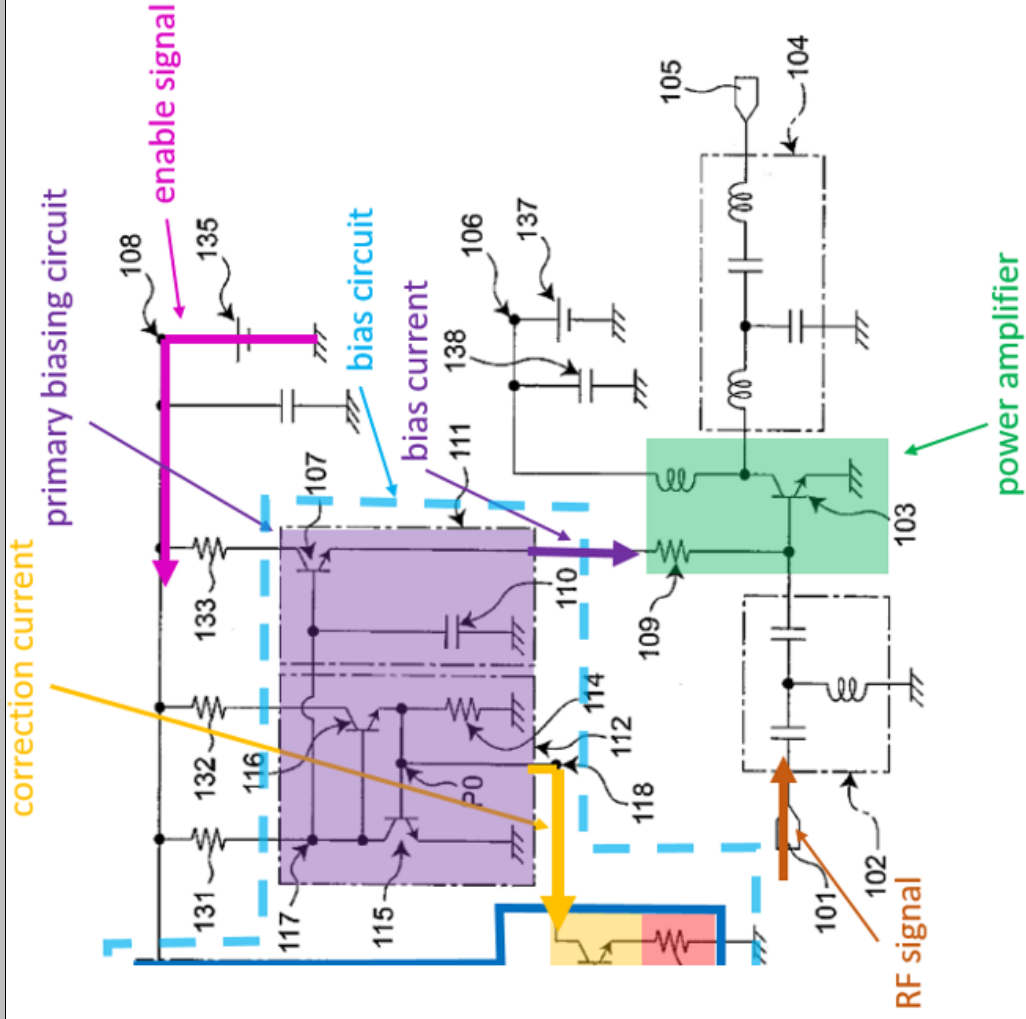
Ishimaru Fig. 1 (annotated).

A POSITA recognized that *Ishimaru* used a current source (red) from circuit 122 to generate a current sink (yellow) from 112, coupling the two circuits using the current mirroring provided by transistor 119. A POSITA readily understood that this coupling could be improved by use of the basic current mirror of *Harrison* because of multiple advantages of providing an additional stage of fine tuning the current amplification. The additional stage of fine tuning would give the designer an additional degree of freedom in designing the circuit, would provide better isolation between the two sides of the circuit, and allow fine tuning in a final amplification stage that had

Claim Language	Ishimaru Alone and/or in Combination with Other References
	better linearity, better control, and higher configurability of its mirror ratio, M, in scaling the mirrored current.). <i>See also</i> State of the Art (App. A-03, § II.B) (discussing two-transistor mirrors). A POSITA would understand that, without the additional teachings of <i>Harrison</i>, <i>Ishimaru</i>'s circuit is constrained by the limited configurability of the β (amplification factor) of transistors 119 and 120. <i>Harrison</i> 53-55. A POSITA was aware that the β of transistors 119 and 120 would be, <i>e.g.</i>, 60 to 150 or more, meaning that the gain of <i>Ishimaru</i>'s transistors 119 and 120 would be a relatively large and cumbersome gain (for example, x100 for transistor 120 and x100 for transistor 119 would result in a total gain of 10,000). <i>Harrison</i> 53-55; <i>Illingworth</i> 38 (practical β values can be "up to 500"). While the β values provide amplification, and, for transistor 119 provide a mirror ratio, that mirror ratio is "not very linear" and "poorly-controlled" compared to other current mirrors, such as the basic current mirror of <i>Harrison</i>. <i>Gilbert</i> 242; <i>Harrison</i> 53-55. Thus, a POSITA readily understood that having to rely upon just the β gains of transistors 119 and 120 is another factor making <i>Ishimaru</i>'s circuit overly complicated and constrained. Adding a basic current mirror similar to that taught by <i>Harrison</i>, however, allows for an additional stage of amplification that can be finely tuned, linear, tightly controlled and granular scaling of the current by adjusting the emitter area of the current mirror transistors, as discussed above. Being able to scale currents in this manner would be useful for a circuit designer wanting to establish a speedup control circuit that could advantageously be reused and adapted for different power amplifier applications and product lines. That is because a POSITA understood that different power amplifiers have different startup and steady state operating qualities, and that the gain variation in <i>Ishimaru</i>'s Figure 2 is specific to a given power amplifier in a given layout, in a specific operating point and use case. The corresponding corrective transient current thus has a specific amplitude and duration that is suitable for the application at issue. For example, using different power amplifier circuit layouts (<i>i.e.</i> where components are dimensionally closer or farther away from each other), different power amplifier packaging, or different power amplifier integrated circuits using a different semiconductor manufacturing process (<i>e.g.</i>, Gallium Arsenide ("GaAs") Heterojunction Bipolar Transistors ("HBTs") (together "GaAs HBTs"), or Silicon Germanium Bipolar CMOS HBTs ("SiGe BiCMOS HBTs")), will

Claim Language	<i>Ishimaru</i> Alone and/or in Combination with Other References
	result in different thermal behaviors and startup effects, and so the amount of correction required will vary. <i>Ishimaru</i> itself recognizes that temperature effects depend on the layout of the power amplifier and the amount of correction required varies across applications. <i>Ishimaru</i> ¶23 (“[T]urn-on behavior of the control voltage source in the amplifier depends on the layout of the amplifier, particularly on the placement of transistors[.]”), ¶3 (“In some communication systems, slight changes of amplification gain as small as 0.2 to 0.3 dB may matter.”), ¶4 (“there are some cases in which variations in amplification ratio or phase on the order of several tens to several hundreds of μs caused by relatively slow temperature increases due to heat generation as an example do matter.”). Thus, <i>Ishimaru</i> provides express motivation for a POSITA to add a current mirror of similar design to <i>Harrison</i>’s for its intended purpose in order to provide flexibility in scaling <i>Ishimaru</i>’s current, including allowing a designer to tune the operation of <i>Ishimaru</i>’s corrective current transient in Figure 3 to a higher peak (such as for a power amplifier having a larger gain variation). A POSITA understands that <i>Ishimaru</i>’s circuit otherwise constrains the ability to tune the $I_{CORRECTION}$ at node 118 as a function of the current through capacitor 121 because of the common, fixed relationships caused by transistor 119 and resistor 136 and the design constraints that limit the configurability of the amplification factors β of transistors 119 and 120. A POSITA would have recognized that <i>Harrison</i>’s two-transistor current mirror would advantageously provide an extra degree of freedom in tuning <i>Ishimaru</i>’s circuit to compensate for the gain problems of a given PA. Modifying the teachings of <i>Ishimaru</i> with the basic current mirror taught by <i>Harrison</i> would involve no more than combining prior art elements (<i>Ishimaru</i> and a conventional current mirror) according to known methods (coupling a current source through a positive current mirror to a current sink, while scaling the mirror’s gain to provide tunable amplification) to yield predictable results. Adding a current mirror simply uses a known technique (scaling currents between two branches of a current mirror) to improve <i>Ishimaru</i> by scaling its currents between the two branches of its circuits in the same way.

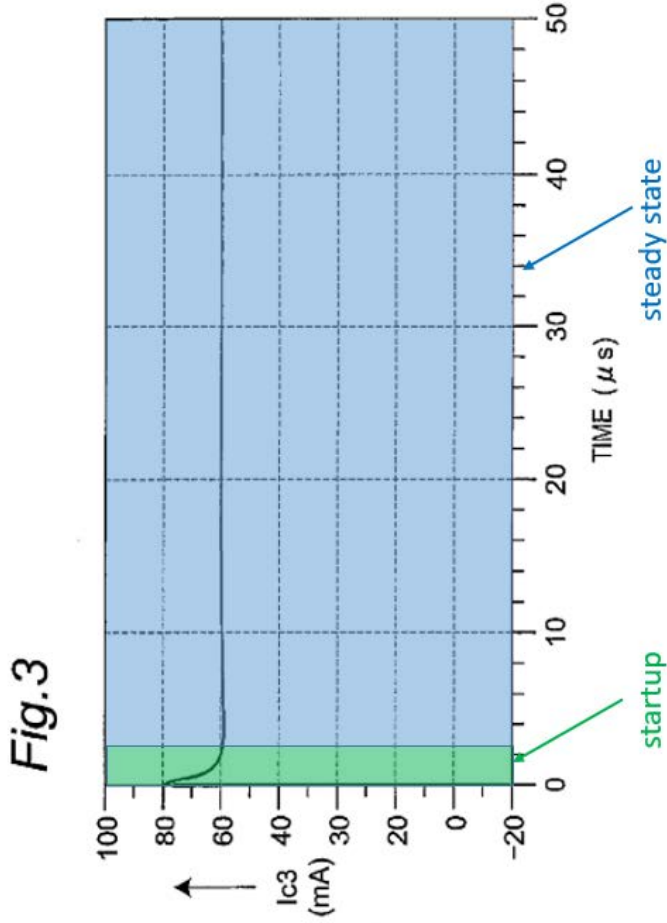
Claim Language	<i>Ishimaru</i> Alone and/or in Combination with Other References
	The combined teachings of <i>Ishimaru</i> and <i>Harrison</i> is consistent with the disclosure of the '101 Patent that the term <i>current mirror</i> can refer to current amplification circuits including a plurality of current mirrors combined (e.g., cascaded) to achieve a target gain. '101 Patent 11:42-45.
[14b.2.b] and a primary biasing circuit configured to generate the bias signal based on the correction current and the power amplifier enable signal.	<i>Ishimaru</i> discloses a primary biasing circuit configured to generate a bias signal based on the correction current and the power amplifier enable signal. See, e.g.: <i>Ishimaru</i> discloses a power source circuit 112 and bias circuit 111, which constitute the primary biasing circuit (purple) which together supply a “base bias current” (I_{BIAS}, the bias signal) (purple arrow) to the amplifier transistor 103. As explained below, this I_{BIAS} is based on the control voltage (the power amplifier enable signal) (pink arrow) and the current drawn out of node 118 (the correction current) (gold arrow).



Ishimaru, Fig. 1 (annotated) (partial).

Claim Language	Ishimaru Alone and/or in Combination with Other References
	Ishimaru explains that “bias circuit 111 and the power source circuit 112 constitute a bias power source section.” <i>Ishimaru</i> ¶46. The combination of this circuitry is a <i>primary biasing circuit</i> in that it is the main circuitry used to generate the “base bias current” that biases the operating point of the transistor of the PA (<i>green</i>) to its intended state (e.g. <i>enabled</i>, and biased to operate at its intended operating point, suitable for amplification). <i>See, e.g., Horowitz</i> 218, 220, 222-228; <i>Harrison</i> Fig. 2.1. More specifically, bias circuit 111 is “composed of the bias transistor 107 and a capacitance element 110” connected to the base of bias transistor 107. <i>Ishimaru</i> ¶45. Bias transistor 107’s collector is connected to bias terminal 108 through a resistor 133, and the bias terminal 108 is connected to control voltage source 135 (<i>the power amplifier enable signal</i>) (<i>pink arrow</i>). <i>Ishimaru</i> ¶44. The emitter of bias transistor 107 is connected to a base terminal of the amplifier transistor 103 via resistance element 109 and “supplies a base bias current to the base of amplification transistor 103.” <i>Ishimaru</i> ¶43. This “base bias current” (I_{BIAS}) is a <i>bias current</i>. Bias transistor 107 in circuit 111 operates in conjunction with power source circuit 112 to generate I_{BIAS} applied to the amplifier transistor 103 and thus, circuit 111 and 112, collectively are a <i>primary biasing circuit</i> (<i>purple</i>). More specifically, as shown in the portion of the annotated Figure 1 above, node 117 of circuit 112 is connected to the base terminal of the bias transistor 107 and, thus, controls the bias point of transistor 107 and, consequently, the transistor 107’s collector current. <i>Ishimaru</i> ¶¶46, 48. Node P0 of power source circuit 112 (<i>i.e.</i>, the base of transistor 115 and emitter of transistor 116) is connected to output terminal 118 of speedup circuit 122. <i>Id.</i> ¶¶48-49. <i>Ishimaru</i> explains that, at a rise time of the control voltage from the control voltage source 135, “a current transiently (temporarily) from the output terminal 118” flows into the speedup circuit 122. <i>Ishimaru</i> ¶52. As explained above, this current is $I_{CORRECTION}$. The transient rise in $I_{CORRECTION}$ causes the voltage at output terminal 118 to lower, which raises the voltage at the collector of transistor 115 (node 117), which controls the bias transistor 107, and this causes “the current fed to the amplifier transistor by the bias transistor 107” (<i>the bias signal</i>) to transiently increase. <i>Id.</i> Figure 3, which shows the transient response of the collector current of the amplifier

transistor 103, illustrates how the transient rise in $I_{CORRECTION}$ causes the collector current of PA transistor 103 to temporarily increase during startup. *Id.* ¶54.

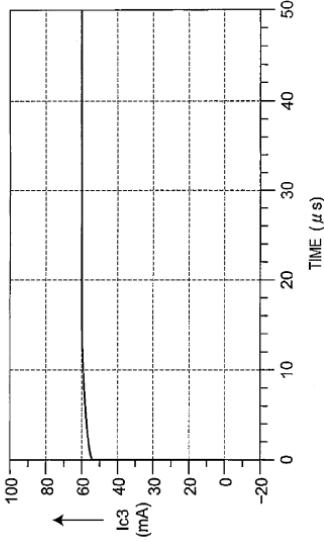
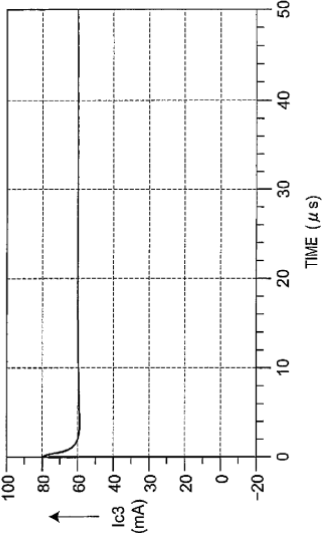


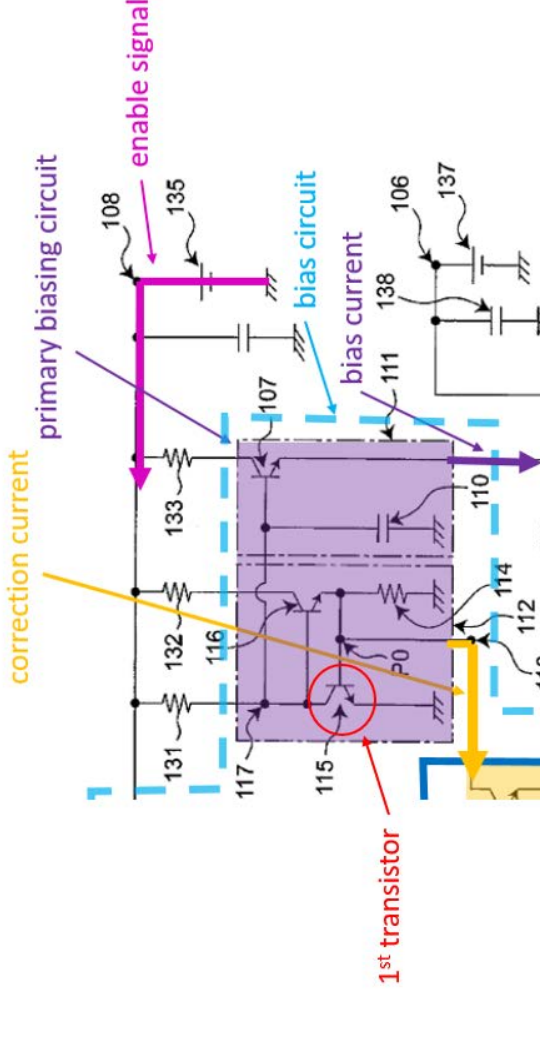
Ishimaru Fig. 3 (annotated).

This transient increase in the collector current of amplifier transistor 103 is due to a transient increase in the I_{BIAS} because the collector current amplifies I_{BIAS} via PA transistor 103's amplification factor β . Further, *Ishimaru* explicitly explains that the collector current 103 (also called "operating current I_{c3} ") "comes to a steady state in about $\frac{1}{4}$ of the time of transient response of the comparative example of Fig. 2," which is the transient response without speedup circuit 122. *Ishimaru* ¶¶53-54.

Claim Language	<i>Ishimaru Alone and/or in Combination with Other References</i>
	Accordingly, <i>Ishimaru</i> discloses a bias power source section with a bias circuit 111 and power source section 112 (together, <i>a primary biasing circuit</i>) that provides I_{BIAS} (a bias signal). At turn-on (<i>i.e.</i>, enablement) of power amplification, this I_{BIAS} is based on the current pulled from terminal 118 and the control voltage from the control voltage source 135 (<i>configured to generate the bias signal based on the correction current and the power amplifier enable signal</i>). <i>Ishimaru</i> discloses: “Also, a bias transistor 107 as a second transistor is a transistor that supplies a base bias current to a base terminal of the amplifier transistor 103. An emitter of the bias transistor 107 is connected to a base terminal of the amplifier transistor 103 via a resistance element 109. The resistance element 109 is a ballast (stabilization) resistor which is inserted in a base bias channel to prevent thermal runaway of the amplifier transistor 103. The bias transistor 107 has its collector connected to a bias terminal 108 via a resistance element 133. The bias terminal 108 is connected to a control voltage source 135. A bias circuit 111 composed of the bias transistor 107 and a capacitance element 110 connected to a base terminal of the bias transistor 107 has a function of increasing the base bias current in response to an increase in signal strength of the input signal, and functions to keep the amplification ratio of an output signal as well as its phase rotation after amplification constant even when the signal strength of the input signal has changed. A power source circuit 112 is connected to the base terminal of the bias transistor 107 of the bias circuit 111. The bias circuit 111 and the power source circuit 112 constitute a bias power source section. The power source circuit 112 feeds generally a sum of a “base-emitter voltage” of the amplifier transistor 103 and a “base-emitter voltage” of the bias transistor 107 to the base terminal of the bias transistor 107. That is, the power source circuit 112 feeds a voltage double the base-emitter voltage (hereinafter, referred to as VBE) of a transistor used in the power source circuit 112 to

Claim Language	<i>Ishimaru</i> Alone and/or in Combination with Other References
	the base terminal of the bias transistor 107. It is noted that voltage drops of the ballast resistor 109 are neglected in this case.” <i>Ishimaru</i> at ¶¶ 43 - 47. “In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).” <i>Ishimaru</i> at ¶ 52. “In the power amplifier of this embodiment also, the capacitance value of the capacitance element 121 of the speedup circuit 122 is adjusted so as to cancel transient variations in gain due to the temperature variations at a start of power amplification. As a result of this, deterioration of the linearity due to variations of amplification gain can be canceled so that the value of dynamic EVM (error vector magnitude) can be improved.” <i>Ishimaru</i> at ¶ 55. “Next, FIG. 3 shows an example (simulation result) of transient response of the operating current (collector current Ic3) of the amplifier transistor 103 in the power amplifier of this embodiment. In this embodiment, the current to be fed from the bias transistor 107 to the amplifier transistor 103 is forcedly increased at turn-on of the amplifier, with the result that the value of the operating current Ic3 comes to a steady state in about 4 the time of transient response of the comparative example of FIG. 2. Thus, occurrence of distortions of the amplification signal due to temperature variations in the amplifier circuit is suppressed, so that the linearity of the circuit in burst operation is improved. That is, gain variations due to collector current variations of the

Claim Language	Ishimaru Alone and/or in Combination with Other References
	power amplifier using a bipolar transistor can be compensated.” <i>Ishimaru at ¶ 54, Fig. 1, Fig. 2, Fig. 3.</i> “In the power amplifier of this embodiment also, the capacitance value of the capacitance element 121 of the speedup circuit 122 is adjusted so as to cancel transient variations in gain due to the temperature variations at a start of power amplification. As a result of this, deterioration of the linearity due to variations of amplification gain can be canceled so that the value of dynamic EVM (error vector magnitude) can be improved.” <i>Ishimaru at ¶ 55, Fig. 1.</i> <i>Fig.2 PRIOR ART</i>  <i>Fig.3</i>  <i>Ishimaru, Figs. 2 and 3.</i>
	Claim 15
[15] 15. The packaged module of claim 14 wherein the primary	<i>Ishimaru discloses a primary bias circuit, discussed in claim 14b.2.b, where the primary bias circuit includes a first transistor [and] the correction current configured to change a current flowing through the first transistor. See, e.g.:</i> As shown in the annotated excerpt of Figure 1 below, <i>Ishimaru</i> discloses that bias power source section (the primary bias circuit) (purple) includes transistor 115, which is a first transistor (red). <i>Ishimaru ¶48.</i> As described with respect to limitation [14b.2.b], the base of transistor 115 is

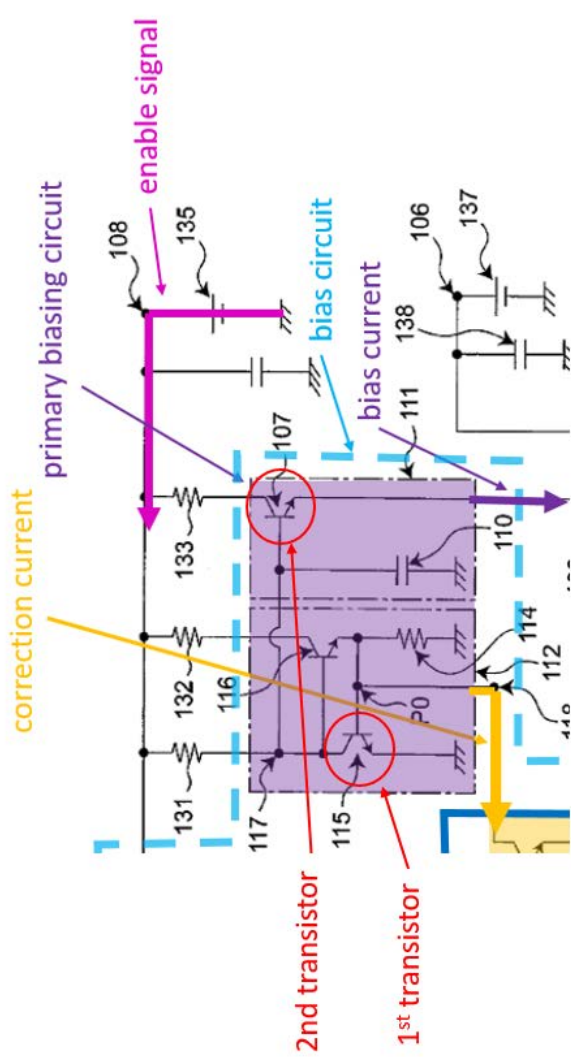
Claim Language	Ishimaru Alone and/or in Combination with Other References
bias⁷ circuit includes a first transistor, the correction current configured to change a current flowing through the first transistor.	connected to connecting point P0, through which $I_{CORRECTION}$ (gold) flows into speedup circuit 122. <i>Id.</i> ¶49, 52. When the amplifier turns on in response to the control voltage from the control voltage source 135, the $I_{CORRECTION}$ temporarily increases, which lowers the voltage at the base of transistor 115. <i>Id.</i> ¶52. A POSITA understands that this change in the voltage at the base of transistor 115 changes the bias point of transistor 115 and, thus, changes the current flowing through (i.e., from the collector to the emitter) transistor 115 (configured to change a current flowing through the first transistor).  <i>Ishimaru, Fig. 1 (annotated) (partial).</i>

⁷ Claims 15 and 20 refer to “the primary bias circuit,” but that term is never defined. Respondents assume that this term refers to the “primary biasing circuit” in claim 14 and addressed in [14b.2.b].

Claim Language	Ishimaru Alone and/or in Combination with Other References
	Thus, <i>Ishimaru</i> discloses that the bias power source section (<i>the primary bias circuit</i>) (purple) has a transistor 115 (<i>includes a first transistor</i>) (red) where a change in the current flowing into speedup circuit 112 changes the current flowing through transistor 115 (<i>the correction current configured to change a current flowing through the first transistor</i>). <i>Ishimaru</i> discloses: “In this embodiment, as shown in FIG. 1, the power source circuit 112 has a third transistor 115, a fourth transistor 116, and a resistance element 114. The third transistor 115 has its collector connected to the base of the bias transistor 107 and its emitter connected to the ground. Also, a base of the third transistor 115 is connected to an emitter of the fourth transistor 116. The collector of the third transistor 115 is connected to the bias terminal 108 via a resistance element 131. Meanwhile, the fourth transistor 116 has its emitter connected to the ground via the resistance element 114 and its collector connected to the bias terminal 108 via a resistance element 132.” <i>Ishimaru</i> at ¶ 48. “A connecting point P0 between the base of the third transistor 115 and the emitter of the fourth transistor 116 in the power source circuit 112 is connected to an output terminal 118 of a speedup circuit 122.” <i>Ishimaru</i> at ¶ 49. “In the speedup circuit 122, with electric charge flowing into the capacitance element 121 at a rise time of the control voltage of the control voltage source 135 (at turn-on of the amplifier), a current transiently (temporarily) flows from the output terminal 118 into the fifth transistor 119, causing the voltage value of the output terminal 118 to lower. As a result, due to a change of the bias point of the third transistor 115, the voltage of a connecting terminal 117, which connects the collector of the third transistor 115 to the base of the bias transistor 107, transiently increases. Thus, at the rise time, the current fed to the amplifier transistor 103 by the bias transistor 107 transiently increases. Therefore, at the rise time, the power amplification factor of the amplifier transistor 103 transiently increases, so that the time elapsing until temperature variations due to heat generation of the amplifier transistor 103 come to an equilibrium on the

Claim Language	<i>Ishimaru Alone and/or in Combination with Other References</i>
	whole circuit is shortened, with a result of reduced distortion of the amplification signal (e.g., modulated wave signal).” <i>Ishimaru</i> at ¶ 52. A POSITA would understand that, because the current through transistor 119 (the correction current) changes the voltage value of output terminal 118, bias point of transistor 115 (the first transistor) and the collector voltage of terminal 117, the current flowing through transistor 115 changes because of the correction current.
[17] 17. The packaged module of claim 14 wherein the gain correction circuit includes a current mirror configured to generate the correction current by mirroring the control current, the current mirror configured to receive the power amplifier enable signal.	Claim 17 <i>Ishimaru</i> discloses a gain correction circuit [that] includes a current mirror configured to generate the correction current by mirroring the control current, the current mirror configured to receive the power amplifier enable signal. See, e.g.: <i>Ishimaru</i> discloses this limitation for the same reason as discussed with respect to limitation [14b.2.a]. Specifically, the speedup circuit (gain correction circuit) (dark blue) includes transistor 119 (current mirror) (gold) configured to generate $I_{CORRECTION}$ (gold arrow) by mirroring $I_{CONTROL}$ (red arrow), where the current mirror is configured to receive the power amplifier enable signal (pink arrow) as illustrated in the annotations of Fig. 1, below.

Claim Language	The diagram illustrates a complex electronic circuit, labeled Fig. 1. It features several interconnected blocks and components: Time dependent signal generator (121): A red-shaded block on the left containing transistors 125 and 126, and a capacitor 120. Gain correction circuit (115): A blue-shaded block in the center containing transistors 117, 118, and 119, and a capacitor 121. Correction current (131-133): A yellow-shaded block at the top containing resistors 131, 132, and 133. Primary biasing circuit (108): A purple-shaded block on the right containing transistors 106 and 107, and a capacitor 135. Enable signal (135): A pink arrow pointing to the primary biasing circuit. Bias circuit (111): A blue-shaded block containing transistors 110 and 111, and a capacitor 138. Bias current (110): A blue arrow pointing to the bias circuit. Control current (122): A red arrow pointing to the gain correction circuit. Amplifier / current mirror (101): A yellow-shaded block at the bottom containing transistors 101 and 102, and a resistor 136. RF signal (102): A red arrow pointing to the amplifier / current mirror. Power amplifier (103): A green-shaded block on the right containing transistors 103 and 104, and a capacitor 105.
	<i>Ishimaru</i> Fig. 1 (annotated). <u>Ishimaru in view of Harrison discloses this limitation.</u> To the extent Complainant argues that <i>Ishimaru</i> does not disclose a current mirror, <i>Ishimaru</i> in view of <i>Harrison</i> discloses this limitation for the same reasons as discussed with respect to limitation [14b.2.a].
	Claim 20

Claim Language	Ishimaru Alone and/or in Combination with Other References
[20] 20. The packaged module of claim 15 wherein the primary bias circuit further includes a second transistor electrically coupled to the first transistor and configured to provide the bias signal to the power amplifier.	Ishimaru discloses a primary bias circuit, discussed in claim 14b.2.b and claim 15, where the primary bias circuit includes a second transistor electrically coupled to the first transistor and configured to provide the bias signal to the power amplifier. See, e.g.: As shown in the portion of Annotated Fig. 1 below, Ishimaru discloses that bias power source section (the primary bias circuit) (purple) includes a transistor 115 (the first transistor) (red circle) and transistor 107 (a second transistor) (red circle). Transistor 115 “has its collector connected to the base” of “transistor 107,” and transistor 107 “supplies a base bias current (purple) to a base terminal of the amplifier transistor 103.” Ishimaru ¶¶48, 43.  Ishimaru, Fig. 1 (annotated excerpt). Ishimaru thus discloses a bias power source (the primary bias circuit) including transistor 107 (a second transistor) (red circle) with a base connected to the collector of transistor 115 (electrically coupled to the first transistor) (red circle) where transistor 107 “supplies a base bias

Claim Language	<i>Ishimaru</i> Alone and/or in Combination with Other References
	current” (is configured to provide the bias signal) (purple) “to a base terminal of the amplifier transistor 103” (to the power amplifier). <i>Ishimaru</i> discloses: “In this embodiment, as shown in FIG. 1, the power source circuit 112 has a third transistor 115, a fourth transistor 116, and a resistance element 114. The third transistor 115 has its collector connected to the base of the bias transistor 107 and its emitter connected to the ground. Also, a base of the third transistor 115 is connected to an emitter of the fourth transistor 116. The collector of the third transistor 115 is connected to the bias terminal 108 via a resistance element 131. Meanwhile, the fourth transistor 116 has its emitter connected to the ground via the resistance element 114 and its collector connected to the bias terminal 108 via a resistance element 132.” <i>Ishimaru</i> at ¶¶ 48. “A connecting point P0 between the base of the third transistor 115 and the emitter of the fourth transistor 116 in the power source circuit 112 is connected to an output terminal 118 of a speedup circuit 122.” <i>Ishimaru</i> at ¶ 49. “Also, a bias transistor 107 as a second transistor is a transistor that supplies a base bias current to a base terminal of the amplifier transistor 103. An emitter of the bias transistor 107 is connected to a base terminal of the amplifier transistor 103 via a resistance element 109. The resistance element 109 is a ballast (stabilization) resistor which is inserted in a base bias channel to prevent thermal runaway of the amplifier transistor 103.” <i>Ishimaru</i> at ¶ 43.