Single and Dual Input Packaged 5.5-6.5GHz, 20W, Quasi-MMIC GaN-HEMT Doherty Power Amplifier

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***Abstract*—This paper presents the design, the realization and the power characteristics of plastic low cost packaged symmetric Doherty Power Amplifiers (DPA) operating in the 5.5-6.5GHz bandwidth. A single input (SI-DPA) and a dual input (DI-DPA) DPAs are proposed based on two power bars composed of two GaN HEMT cells (8 fingers of 275µm unit gate width). Input and output matching networks are designed on passive GaAs MMIC technology. To our knowledge, it is the first published SI and DI-DPAs working in C band, designed using Quasi-MMIC technology and assembled in plastic package.**

The measured power results under Continuous Wave (CW) signal of the SI-DPA demonstrate a maximum output power (P_{OUT}) upper than 20W (43.5dBm) with 50% drain efficiency (DE), 42% power added efficiency (PAE), 11dB of insertion gain (G_I) in the 5.5-6.5GHz bandwidth. At 6dB Output power Back-Off (OBO), the drain efficiency is greater than 35% (32% PAE). The DPA linearity has been investigated with a 256QAM modulation signal of 30MHz bandwidth and using Digital Pre-Distortion (DPD) leading to a 50dBc Adjacent Channel Leakage Ratio (ACLR) at a 34 dBm average output power.

The designed DI-DPA is identical to the SI-DPA without input power splitter. It demonstrates that the adjustment of power ratio between the main and the peak amplifiers associated with adequate bias points, improves all the power performances: linearity, PAE, OBO and G_I. The DI-DPA reaches a 12.5 dB G_I , a maximum P_{OUT} equal to 44dBm (3.5dB gain compression) with 45% PAE. Moreover, in the same previous bandwidth, 40% PAE with 4° of AM/PM variation are obtained at 6dB$_{OBO}$ and 36% PAE (AM/PM=3°) at 8dB$_{OBO}$.

***Index Terms*— High Power Amplifier, Quasi-MMIC, GaN HEMTs, Doherty Power Amplifier, Dual Input Doherty, plastic packaging, Digital Pre-Distortion.**

I. Introduction

Doherty Power Amplifiers using GaN HEMT devices are good candidates to address high output power, low power consumption over wide ranges of OBO. Moreover, MMIC DPA architectures are clearly promising to reach very high performances in terms of PAE and OBO range[1], [2].

While GaN MMIC technology provides best integration and reproducibility, it also suffers from an important constraint in terms of cost effectiveness for high volume production. To overcome this main constraint, the so called "Quasi-MMIC" for the realization of passive matching circuit appears as a good solution in order to achieve simultaneously high technical performances (PAE, OBO and linearity), low size, high production yield and cost effectiveness up to C band and beyond [3], [4].

II. Key technologies

A. 0.25µm GaN HEMT Technology

The transistors are based on 0.25µm AlGaN/GaN technology from UMS, qualified on a 4-inches-diameter SiC substrate for drain bias up to 30V. The gate to drain break-down voltage is higher than 120V. When optimally matched this transistor demonstrates around 4.5W/mm of saturated RF output power and a maximum PAE above 50% at 10GHz [5].

B. Quasi-MMIC technology in over molded QFN package

The DPA combines GaN power bars and input/output matching circuits realized on passive GaAs MMICs technology developed for high power density functions [6]. These circuits have been assembled in a 54 leads 8x8mm over molded plastic package using a high thermal conductivity glue to reduce the thermal resistance as compared to standard solutions. This low-cost solution allows a good trade-off between electrical (high frequency) and industrial constraints (assembly rules). The interconnections between GaN power bars and GaAs passive MMICs and also the ones between GaAs devices and package leads are realized with wire bonds. All these interconnections networks have been defined according to the industrial rules and have been simulated on 3D EM tools in order to build multi-ports passive networks for overall DPA design.

III. DPA oriented characterization of GaN HEMTs

The 8x275µm GaN HEMT power transistor cells have been simulated using the extracted electric model from UMS foundry. The GaN HEMT has also been measured as described in [], at V_{DS0}=30V, in AB, B and C classes for different frequencies in the operating bandwidth. Fig. 1 presents the simulated and measured PAE versus P_{OUT} curves for different optimal load admittances (Y_L) at 6.2GHz for GaN HEMT transistor operating in AB class (I_{DS0}=50mA/mm). The load admittances at second harmonic are verified and located in the favorable areas on the smith chart.

The measurements show that in perfect conditions, the PAE of the GaN HEMT power bar is greater than 55% in the OBO range from P_{OUTMAX}=39.4dBm to P_{OUTOBO}=33.4dBm.

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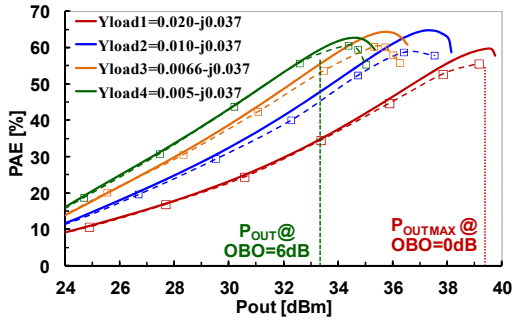


Fig. 1. Measured (solid lines) and simulated (dash lines) PAE versus P_{out} for different load admittances at f_0=6.2GHz (AB class) – V_{DS0}=30V.

Table I summarizes the measured and simulated values of the input impedances (Z_{IN}) at the gate-port and the load admittances (Y_L) at the drain port for the carrier and the peak HEMTs at f_0 = 6.2GHz.

TABLE I
USEFUL Z_{IN} AND Y_L FOR THE DPA DESIGN

	OBO = 0dB			OBO = 6dB		
	Z_{IN} (•)	$Y_{L,MAX}$ (S)		Z_{IN} (•)	$Y_{L,MAX}$ (S)	
Class	R_{IN}+jX_{IN}	$G_{L,MAX}$	$B_{L,MAX}$	R_{IN}+jX_{IN}	$G_{L,MAX}$	$B_{L,MAX}$
AB	0.84-j2.56	0.040	0.071	0.57-j1.67	0.010	0.071
C	0.80-j3.68	0.040	0.071	0.42-j3.61	0.010	0.071

A. Design approach

The theory about DPA is well documented [8], [9].

The design takes into account the quasi-MMIC technology constraints (key point of the design) thanks to a full 3D EM simulation of the interconnection network into the QFN environment. The schematic used for the proposed symmetrical packaged Quasi-MMIC SI-DPA is given in Fig.2.

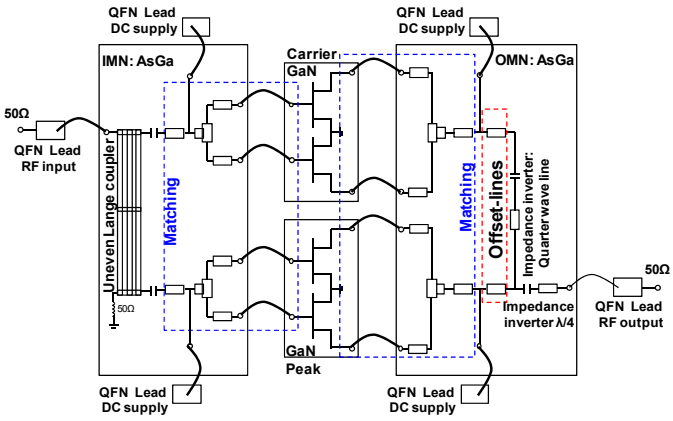


Fig. 2. Schematic of the proposed Quasi-MMIC SI-DPA

The design process requires the optimization of the offset lines in order to ensure that the load admittance modulation Y_L at the intrinsic main drain plane remains real along the OBO path on the Smith chart [10]. On the other hand, the Norton transformations are widely applied in order to find realistic values of Output Matching Network (OMN) passive elements (line widths and lengths). The linearity of the SI-DPA is improved using an uneven input Lange coupler delivering a higher power to the carrier branch. Consequently, on the one hand, the peak amplifier operates in shallow C class in order to present smooth AM/AM and AM/PM variations when it begins to conduct. On the other hand, the gain of DPA increases, thereby limits the Doherty gain penalty. A distributed quasi-lumped transformation is applied to reduce the input impedance transformer and the size of the final DPAs. Finally, the linear and non-linear stability of the QFN packaged SI-DPA is ensured using STAN software™.

The OMN optimization goal consists in obtaining, in the operating bandwidth [5.5-6.5] GHz, the following conductances at the carrier and peak drain planes:

- At maximum Output Power (OBO = 0dB):
  - $G_{L,C}$ equal to $G_{L,MAX}$ from table I.
  - $G_{L,P}$ equal to $G_{L,MAX}$ from table I.
- At OBO = 6dB
  - $G_{L,C}$ equal to G_{LMAX}/2 from table I.
  - $G_{L,P}$ equal to a very low conductance.

The terminations at second harmonic are chosen with respect of the criterion defined in [11].

The quiescent biasing current of the carrier stage is about 130mA (~25mA/mm) (AB near B class); a -7V gate bias voltage $V_{GS0,P}$ is applied to the peaking stage (class C). The DPAs work with a 30V drain bias voltage V_{DS0} applied to both stages.

B. DI-DPA configuration

The DI-DPA structure is identical to the SI-DPA one without the input Lange coupler. It enables the main and the peak amplifiers to be driven with two different signals. This configuration, associated to appropriate bias points, enables optimizing the performances of the DPA, i.e.: the trade-off PAE/linearity in terms of AM/AM and AM/PM variations is made possible. We name the separate management of the two input signals: Input Signal Engineering (ISE) of a DPA.

The main amplifier works in AB class and the peak amplifier in AB/B class. The input power of the peak amplifier is adjusted so that its output power compensates the compression of the main amplifier, leading to a flat output power of the DPA. The ISE enables optimizing the variation of the impedance presented to the main amplifier along the OBO, leading to optimized characteristics of the DPA.

IV. EXPERIMENTAL RESULTS

A. Small signal measurements

Fig. 3(a) shows a photograph of the assembled SI-DPA in QFN plastic package. To achieve the measurements using SMA connections, the 8x8mm SI and DI-DPA QFN are implemented on printed circuit boards including an additional Low Frequency decoupling stage as shown in (b) and (c).

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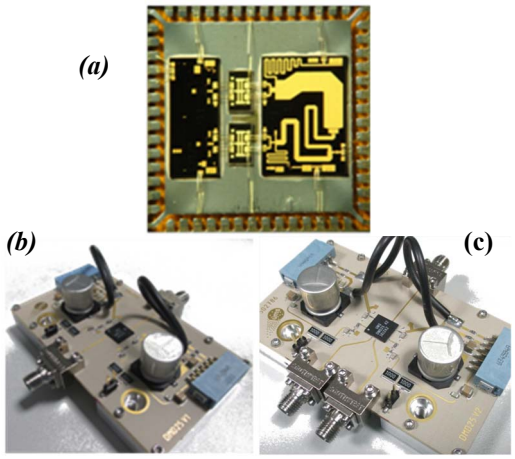


Fig. 3. (a): Photograph of the assembly DPA in QFN plastic package. Photograph of the SI-DPA (b) and the DI-DPA (c) assembly boards.

Power sweeps and small signal measurements are performed using a setup based on Keysight PNA-X.

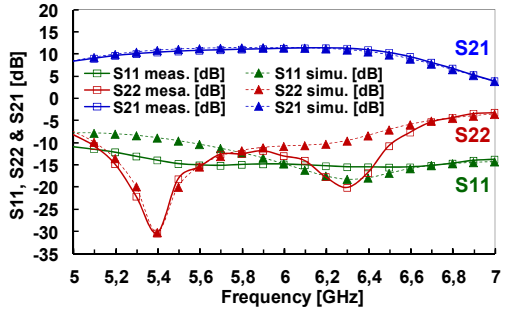


Fig. 4. Measured and simulated SI-DPA S-parameters

The input and output of the QFN-package define the calibration reference planes.

All measurements of the SI-DPA are realized at $V_{DS0,M}$ = $V_{DS0,P}$ = 30V, I_{DS0}=130mA (~25mA/mm) and $V_{GS0,P}$ = -7V. Fig. 4 highlights the good agreement between simulated and measured S-parameters in the [5-7] GHz bandwidth.

B. Large signal measurements

Fig. 5 compares the SI-DPA back-simulations results at 6.2GHz with measurements results of a conventional Deep class AB PA (V_{DS0}=30V, I_{DS0}= ~25mA/mm). At 6.5dB$_{OBO}$, the SI-DPA presents around 13 points of PAE improvement.

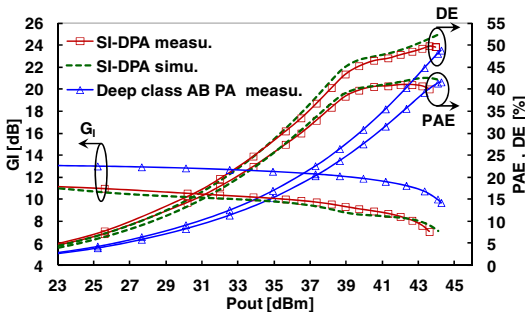


Fig. 5. CW Measured and simulated DE, PAE and G_I at 6.2GHz

Fig. 6 presents the measured PAE of two boards of the same SI-DPA versus frequency for 2 P_{OUT}: 43.5dBm (0dB OBO) and 37dBm (6.5dB OBO).

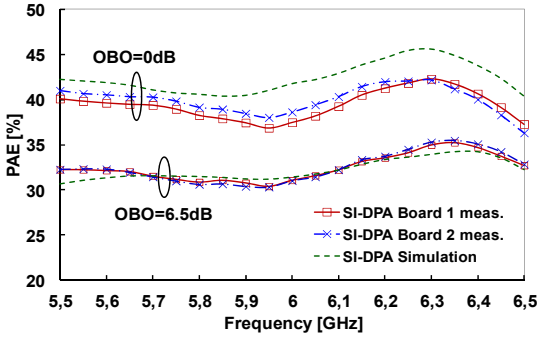


Fig. 6. CW Measured PAE vs. Frequency at OBO=0dB and OBO=6.5dB

C. Modulated Signal Measurements and Linearization

The linearity performance of the SI-DPA has been tested using a 256QAM (160Mbit/s) signal with 9 dB PAPR (Roll-off=0.2) and 30MHz bandwidth. The SI-DPA exhibits a -31dBc ACLR for a 34dBm average P_{OUT}. Thanks to a DPD with memory, a 19dBc improvement of ACLR is obtained (Fig. 7).

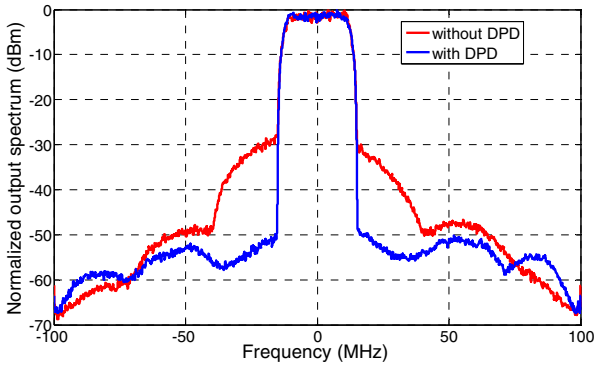


Fig. 7. Measured spectrum of the DPA for a 256QAM with (red line) and w/o DPD including memory (blue line) at average channel output power of 34dBm (f_0=6.2GHz, I_{DS0} = 220mA, $V_{DS0,M}$= $V_{DS0,P}$=30V, V_{GS0P}=-6V)

D. Comparison between Conventional Deep class AB PA, SI-DPA and DI-DPA comparison

Fig. 8 exhibits, for the same output level, the comparison of a conventional Deep class AB PA ($V_{DS0,M}$ = V_{DS0P} = 30V, I_{DS0}= 50mA/mm) with the SI-DPA ($V_{DS0,M}$ = V_{DS0P} =30V, $V_{GS0,P}$ = -7V, $I_{DS0,P}$=0A, $I_{DS0,M}$=25mA/mm) and with the DI-DPA ($V_{DS0,M}$=25V, $I_{DS0,M}$=50mA/mm, $V_{DS0,P}$=30V, $I_{DS0,P}$= 10mA/mm). PAE performance of the DI-DPA is clearly higher than those obtained with the AB PA or the SI-DPA.

When the relative amplitude and phase and the bias points of the two input paths are optimized, the DI-DPA demonstrates a maximum P_{OUT} equal to 44dBm (G_I =12.5dB) with 45% PAE at 6.2GHz. 40% PAE is obtained at 6dB$_{OBO}$ and 27% at 10dB$_{OBO}$.

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TABLE II
COMPARISON WITH OTHER DOHERTY AMPLIFIERS USING GAN HEMT 0.25µM TECHNOLOGY

	[1]	[3]	[12]	[13]	This work SI-DPA	This work DI-DPA
Year	2013	2014	2016	2017	2017	2017
Frequency (GHz)	6.65-7.35	5.8-8.8	6.5	6.7-7.3	5.5-6.5	5.5-6.5
Small-signal Gain (dB)	10	7.5-10	18	15	11	12.5
Peak Power (dBm)	38	36	42	38	43.5	44
PAE @ OBO= 6dB (%)	41[a,b]	31-39	24[a]	40	32-36	42
PAE @ OBO= 9dB (%)	40[a,b]	30-36	21[a]	32	23	35
GaN die area (mm^2)	22.08	8.4	4.1	9	2.256	2.256
Package	Bare-die	Bare-die	9x9 QFN	Bare-die	8x8 QFN	8x8 QFN

[a] Read from graph. [b] Drain efficiency (PAE level is not given).

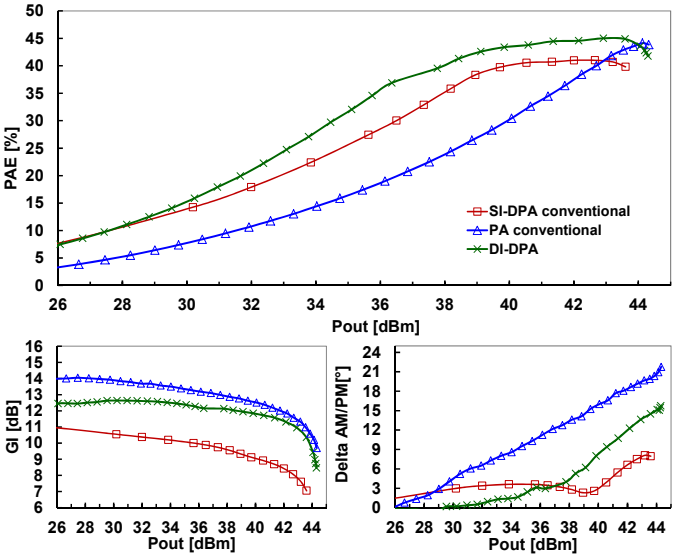


Fig. 8. CW measurements: Comparison of power performances between Conventional deep class AB PA, SI-DPA and the DI-DPA.

E. Comparison with State-of-the-art DPAs.

The performances of the presented amplifiers (SI-DPA and DI-DPA) are compared with the previous published GaN HEMT 0.25µm DPAs in Table II.

V. CONCLUSION

In this paper two low cost C band Doherty amplifiers (SI-DPA and DI-DPA) are presented. This work shows that advanced plastic package, can generate innovative microwave functions, achieving simultaneously high technical performances, low size, high production yield and cost effectiveness.

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