

Sampled Analog Filtering Using Switched Capacitors as Resistor Equivalents

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Abstract—The equivalence between resistor-capacitor (RC) filtering circuits and circuits containing switches and ratioed capacitors is examined. We have demonstrated the advantages of ratioed capacitors for integrated active filters experimentally, using a specially designed integrated MOS test chip. Polysilicon gate technology was used to fabricate the chip, with the capacitors being formed by two levels of polysilicon. For the theoretical description, and as a design aid, attention is drawn to the general equivalence between a resistor and a circuit element consisting of a capacitor and two switches. Nonideal effects, which set limits to the generality, are also discussed.

I. INTRODUCTION

THIS PAPER examines a concept which makes use of the periodic switching of capacitors to obtain useful analog functions. The basic concept, and a suggestion that it should be applicable to monolithic integrated-circuit technology, was outlined by a previous writer [1]. Since then, both the generality of the concept, and the possibilities for applications, appear to have been overlooked. This may be explained partly by a heavy emphasis in recent years on radically new methods for analog sampled-data filtering, such as CCD transversal filtering [2], [3], and MOS recursive filtering [4]. The purpose of the present work is to draw attention to the general equivalence between resistor-capacitor (RC) networks, and networks in which the resistors are replaced by combinations of capacitors and switches. To demonstrate some possibilities of this equivalence for integrated-circuit technology, a monolithic integrated MOS test chip was designed and experimentally applied to several examples.

Essentially, the concept is a transfer of charge between nodes by means of switches and capacitors. Over periods of time which are long compared to the periodic interval of the switches, the transfer of charge is quasi-continuous, and equivalent to the continuous flow of current in resistors. The name "switched capacitor" will be used for the basic circuit element, which consists of a capacitor and two analog switches.

Previous work has pointed out that the effective values of resistors can be increased by time switching, and an analysis of filtering applications was given [5]. However, time switching adds an additional variable (duty ratio) which can further

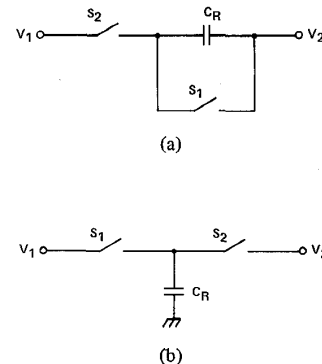


Fig. 1. (a) Series-switched capacitor circuit. (b) Parallel-switched capacitor circuit.

degrade the precision of the RC time constants. In contrast, the precision of switched capacitor circuits is governed by the switching frequency and by the capacitor ratios, which can be controlled to extremely high precision in MOS-type integrated-circuit technologies [6], [7]. Work done independently on the switched capacitor approach is reported elsewhere in this issue [8].

II. SWITCHED CAPACITOR CIRCUIT PRINCIPLES

A. Basic Circuit Element

Consider the switched capacitor network in Fig. 1(a), which will be referred to as the "series switched capacitor." Initially, we assume both ports 1 and 2 to be voltage driven. During the on period of S_1 , the capacitor C_R is initialized, while during the on period of S_2 (S_1 off), net charge $C_R(v_1 - v_2)$ is transferred. As this delivery occurs at every sampling interval T , this represents an average current flow of $C_R(v_1 - v_2)/T$. The network shown in Fig. 1(a), therefore, simulates a resistor R of value

$$R = \frac{T}{C_R} \quad (1)$$

An alternate version (parallel-switched capacitor) shown in Fig. 1(b) also simulates a resistor as defined. Equation (1) indicates the possibility of simulating ratioed resistors by the switching of ratioed capacitors. Further, the resistive ratios can be varied by using different switching frequencies for different resistors.

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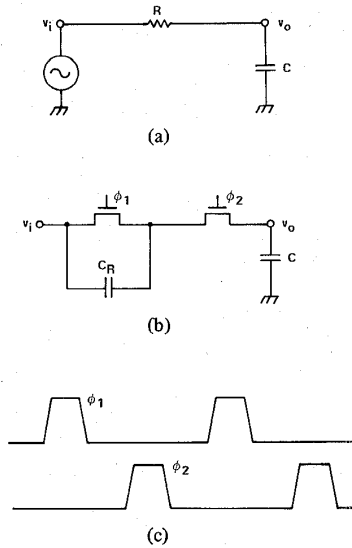


Fig. 2. (a) RC circuit. (b) Its switched-capacitor (series) equivalent. (c) Clocking scheme for the switched-capacitor circuit.

B. Extrapolation to RC Circuit

The previous section assumes both ends of the resistor are voltage driven. For further demonstration of the concept, we consider the simple passive RC circuit and the corresponding series-switched capacitor realization, as shown in Fig. 2(a) and 2(b), respectively. The ideal switches are replaced by MOS transistors, using nonoverlapping two-phase clocks, ϕ_1 and ϕ_2 , as shown in Fig. 2(c). The equivalence between the two cases in Fig. 2(a) and 2(b) may be found by noting that in Fig. 2(a) the net transfer of charge is given by:

$$\Delta Q = \int_{t_1}^{t_2} i \, dt = \frac{v_i(t_2) - v_o(t_1)}{R} \delta t \quad (2)$$

where

$$\delta t = t_2 - t_1. \quad (3)$$

The equivalent charge transferred in the switched capacitor circuit of Fig. 2(b) for clock period T is

$$\Delta Q = \{v_o(nT) - v_o((n-1)T)\}C. \quad (4)$$

The voltage v_o may be obtained from the difference equation for the circuit as

$$v_o(nT) = v_o((n-1)T) + \frac{C_R}{C_R + C} \{v_i(nT) - v_o((n-1)T)\}. \quad (5)$$

Combining the last two expressions,

$$\Delta Q = \{v_i(nT) - v_o((n-1)T)\} \frac{CC_R}{C + C_R} \quad (6)$$

where nT and $(n-1)T$ correspond to t_2 and t_1 in (2) of the continuous case, and T corresponds to δt .

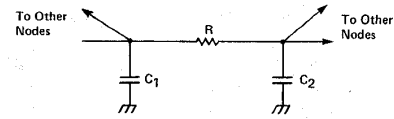


Fig. 3. A general RC circuit.

From (2) and (6), the equivalent resistor achieved by the switched capacitive network may be expressed as

$$R = T \left(\frac{1}{C_R} + \frac{1}{C} \right). \quad (7)$$

If $C \gg C_R$, (7) reduces to (1). From (7), it follows that the effective time constant, measured in clock periods, is given by $(C + C_R)/C_R$, or approximately C/C_R in most cases. A similar analysis for the parallel-switched capacitor also leads to (6) and (7), but with an extra input delay.

A more exact response can be obtained from the z -transform of (5). The differences between the two solutions are unimportant for signal frequencies much lower than the clock frequency (see Section III-B). However, z -transform analysis may be useful where precision is necessary, such as for high Q circuits.

C. Generalization

Fig. 3 shows a part of a general network where neither side of the resistor is voltage driven. The resistive equivalent for the series-switched capacitor can be derived, in terms of the figure, as

$$R = \frac{C_1 C_2 + (C_1 + C_2) C_R}{C_1 C_2 C_R} T, \quad (8)$$

and for the parallel-switched capacitor, the equivalence is

$$R = \frac{C_1 C_2 + (C_1 + C_2) C_R + C_R^2}{C_1 C_2 C_R} T. \quad (9)$$

Similarly, if two resistors are connected to a capacitive node, as node v_o in Fig. 2(b), the resistive equivalents are modified to include terms in all three capacitances connected to the node. As the degree of interconnection rises, the complexity of the resistive equivalence expression increases. The question arises as to how far it is useful to carry the resistor/switched capacitor equivalence, when as mentioned previously, the z -transform solution is more exact as signal frequency becomes comparable to the clock frequency. There are a number of answers to this. First, many active filters have most resistors voltage driven at one or both ends (operational amplifier virtual grounds or outputs) making the simpler equations adequate. Second, recognizing the equivalence opens up the whole body of continuous active filter knowledge for selection of suitable active filter topologies and parameters. Once this has been done, a difference equation analysis may then be useful to perform the final accurate solution. Third, there are situations where a difference equation analysis is too complex or does not provide a good insight, for example, where more than one clocking frequency is used.

D. Nonideal Properties of the Switched Capacitor

The discussion has, so far, been idealistic from the point of view that the switches were considered ideal. However, realizing the switches by MOS transistors introduces some secondary effects to the network, which we shall now discuss.

1) *Clock feedthrough, offset error, and noise:* Clock feedthrough is caused by the inherent capacitance between diffusion and gate of the switching transistors, including channel charging and discharging capacitance. Its effect appears as the ratio of the feedthrough capacitance to the load capacitance, multiplied by the clock pulse height. This is discussed in Section III-C.

Offset error is caused by leakage current in the switched capacitor, between sampling periods, which in active filter configurations shows up as a component of output voltage offset, as will be seen in Section III-C.

Random noise in an active switched-capacitor filter comes from two sources, the switched capacitors, and the operational amplifier. The switched capacitor noise is mainly thermal or Nyquist noise. As will be seen in Section III-C, this noise is about 20 dB lower than the input noise in present MOS operational amplifiers.

2) *Nonlinear p-n junction capacitance:* In the network of Fig. 2(b), we notice that two p-n junctions (diffusions) appear between the ideal switches. In both cases, they reduce the nominal resistive value of the capacitors by the ratio $2C_D/(C_R + 2C_D)$, where C_D is the average value of the junction capacitance of each diffusion. The voltage dependence of C_D also causes amplitude-dependent distortion of the signal. These factors introduce design limitations on the minimum value of C_R relative to the size of the switches.

3) *Incomplete transfer of charge:* Since the switches have finite ON resistance, the maximum switching rate of the switched capacitor networks will be determined by the need to ensure that relatively complete charge transfer has occurred during the finite pulsewidths of the clocks. This sets a limit on the maximum size of C_R , relative to the size of the switches, and limits the precision (i.e., amplitude and frequency distortion and noise), which deteriorates with an increase in sampling frequency.

The effects of finite pulsewidth of the ϕ_2 clock may be approximated for the series-switched capacitor as follows, for the passive RC circuit:

$$v_o(nT) = v_o((n-1)T) + \frac{C_R}{C_R + C} \{1 - e^{-\Delta/rC_s}\} \{v_i(nT) - v_o((n-1)T)\} \quad (10)$$

where

Δ is the pulsewidth of the clock ϕ_2 ,
 r is the average resistance of the switch S_2 , and
 C_s is the equivalent capacitive value of C and C_R in series.

Comparing (10) with (5), we observe that one effect of finite pulsewidth is to increase the resistive value of the switched capacitor by the proportion $1/(1 - e^{-\Delta/rC_s})$. For example, if

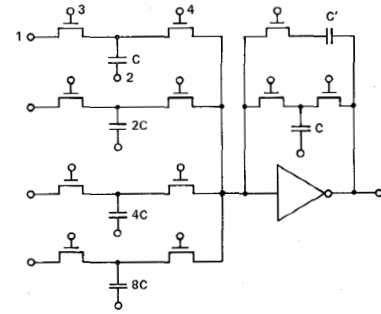


Fig. 4. Circuit diagram of the chip.

Δ is four times rC_s , the resistive value of the series-switched capacitor increases by 1.86 percent.

In addition, the nonideal behavior of the ϕ_1 switch will mean distortion of the signal, for finite pulsewidth, because the ON resistance of the switch is dependent on the signal, i.e., the channel charge is modulated by the signal.

III. EXPERIMENTAL DEMONSTRATION

A. Description of the Test Chip

The experiments were conducted on a test chip containing binary-ratioed switched capacitors, n-channel MOS transistors acting as switches, and an MOS amplifier with a feedback capacitor. The process technology used to fabricate the chip was enhancement-mode silicon-gate using two levels of polysilicon, so that all capacitors used have polysilicon-oxide-polysilicon construction. The circuit diagram and a photomicrograph of the test chip are shown in Figs. 4 and 5, respectively. The smallest capacitor (C in Fig. 4) is of value 0.5 pF. Suitable connections were provided so that both series- and parallel-switched capacitor modes could be simulated. As we wished to minimize the chip area per RC section, a single-ended amplifier was used, consisting of three cascaded inverting stages. The open-loop gain was approximately 800. A differential amplifier would be preferable for many applications, to reject possible common-mode interference from the dc power supply and ground connections. However, in this experiment, we were able to reduce such effects to levels where random noise became dominant by circuit precautions. Measures used to prevent oscillation were separate grounds for each stage of the amplifier; relatively large feedback capacitance; and the relatively large off-chip loading capacitance.

The single-ended amplifier was used in a manner equivalent to an operational-amplifier inverting-mode configuration by using switched-capacitor (i.e., resistor) feedback to make the input a "virtual ground" at the quiescent self-biasing level.

B. Demonstration of First-Order LP Filters

Both passive and active first-order filters were simulated. The passive example was constructed using an on-chip series-switched capacitor, an off-chip load capacitor, with the amplifier not activated. Fig. 6 shows the frequency response for two

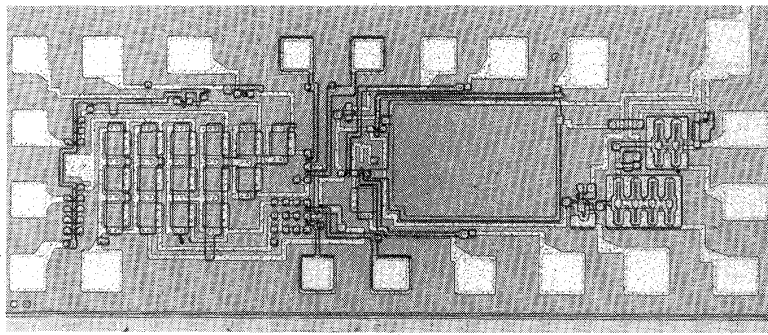


Fig. 5. Photomicrograph of the chip.

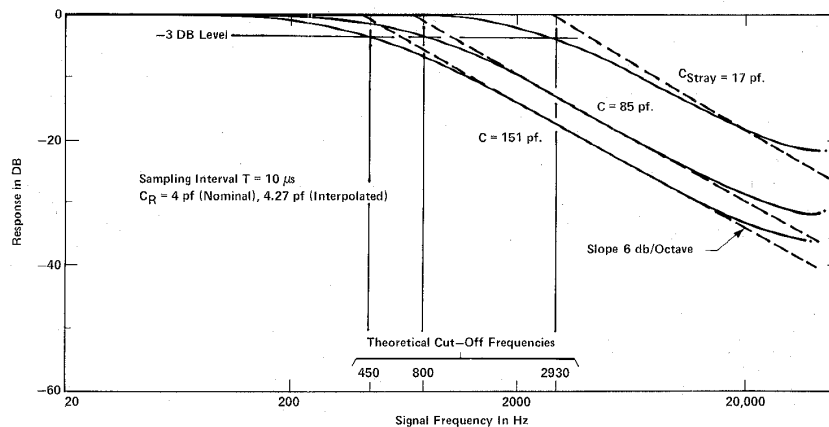


Fig. 6. Frequency response of the passive-series switched capacitor circuit shown in Fig. 1(a).

capacitance loadings as marked. The third response was used to obtain an estimate of the stray capacitance. Including this estimated stray capacitance, the other two curves match the expected frequency and frequency rolloff closely except for signal frequencies which are comparable to the Nyquist limit, where a significant divergence occurs. The reason is that for such frequencies the signal amplitude varies by a large amount between sampling intervals, so that the first-order interpolation is no longer valid, and the difference equation solution as in (5) must be employed. However, this effect will be unimportant because filter response will typically be low near the Nyquist frequency.

A first-order active RC low-pass filter was set up as in Fig. 7(a), and also the parallel-switched capacitor equivalent of this filter, as in Fig. 7(b). The low frequency gain of the switched-capacitor version of the filter is determined by the ratio C_i/C_f if the switched capacitors are operated at the same frequency. Experimental results for the frequency response are shown in Fig. 8. Here, only the input switched capacitor was changed, with values as noted, to change the dc closed-loop gain but not the corner frequency. In the passband region, for

a signal output of 1 V rms, the second-harmonic distortion was 50 dB below the signal response.

As a further experiment, the curves of Fig. 8 were duplicated using only a single input capacitor, C in Fig. 4, but making its clocking frequency in ratio 1, $\frac{1}{2}$, $\frac{1}{4}$ to the feedback-switched capacitor. This demonstrates a means of obtaining a wider range of resistance values than is possible using a single clocking frequency, while limiting switched capacitor areas. Further experimental use of the principle is described in Section III-D.

One further remark: all the experiments reported here were conducted using integrally related clocks. There is no absolute requirement for such a constraint. However, using nonintegral ratios in the input and feedback circuits could give rise to additional feedthrough noise problems. On the other hand, such noise might be tolerably small in filters having feedback capacitors to suppress the effect, suggesting the possibility of increased flexibility in varying the gain or frequency response.

C. Clock Feedthrough, Offset Error, and Noise

Fig. 9 shows the output of the circuit of Fig. 7(b) with no input signal, demonstrating the offset error effects mentioned

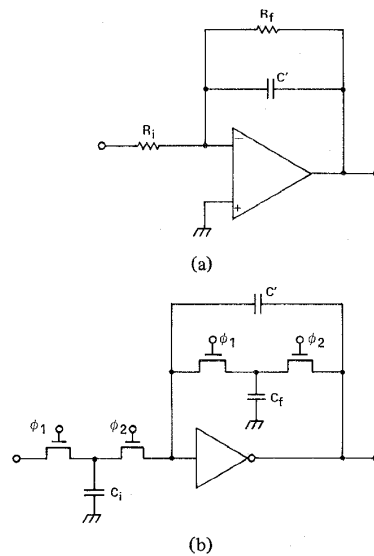


Fig. 7. (a) First-order active RC low-pass filter. (b) First-order low-pass filter circuit using parallel-switched capacitors.

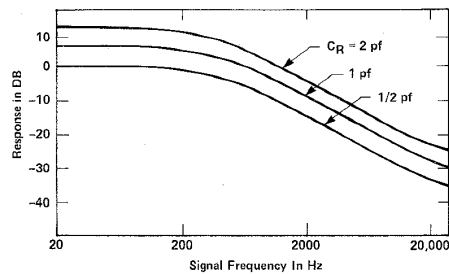


Fig. 8. Frequency response of the circuit in Fig. 7(b), for nominal dc gains of 1, 2, and 4. Sampling interval is $12.5 \mu\text{s}$.

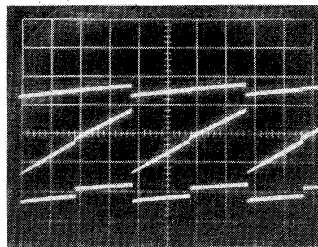


Fig. 9. Picture demonstrating the effect of leakage at low sampling frequency (50 Hz) for the circuit shown in Fig. 7(b). Horizontal scale: 5 ms/cm. Vertical: 0.01 V/cm. There are three traces.

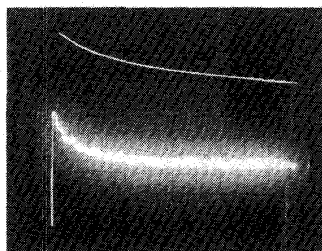


Fig. 10. Frequency spectrum of the low-pass filter [Fig. 2(b)]. Top trace shows the transfer function of the filter. The bottom trace shows the noise spectral density (amplified by 70 dB) at the output terminal of the device. Horizontal: 0.5 kHz/div. Vertical: 10 dB/div.

in Section II-D. There are three separate traces shown. The input switched capacitor circuit is shut off, so the amplifier is in self-biasing mode, with the output voltage acquiring enough offset to feedback, through the feedback-switched capacitor, a current equal to the net leakage current onto the summing junction. The clock frequency was lowered to 50 Hz to make the effects visible. The top trace is for a substrate bias of -5 V. The vertical discontinuity is happening at (ϕ_1 on), when the leakage-canceling charge is delivered back to the summing junction. As leakage thereafter is accumulated, it is integrated in the feedback capacitor and a ramp is generated at the output. The average output offset developed here is 2.5 mV. The middle trace of Fig. 9 is as in the top trace except with substrate bias increased from -5 to -7 V. This is the point of onset of high diffusion leakage, which increases the average output offset to 11 mV.

The bottom trace of Fig. 9 is with substrate bias at -5 V again, but with ϕ_2 of the input-switched capacitor in Fig. 7(b) also operating. The summing junction is now picking up the leakage onto the input switched capacitor C_i , which is appearing as a step when ϕ_2 is turned on, i.e., halfway up the ramp. There is additionally leakage from the feedback-switched capacitor C_f which is part of the vertical discontinuity at the end of the ramp—a positive step canceled by the larger negative feedback charge caused by the output offset.

Not readily visible in Fig. 9 is the clock feedthrough from overlap capacitance of the transistor switches, as at this low clock frequency, the on time of the clocks is relatively short. The feedthrough amplitude here is 6 mV. In active filters, its theoretical amplitude is given by the clock pulse height times the ratio of feedthrough capacitance to feedback capacitance. It is evident that active switched-capacitive filters must be operated with a feedback capacitor, otherwise the amplifier is open loop to capacitive feedthrough from the switches.

Concerning random noise, the noise output of the active filter circuit of Fig. 7(b) was measured at a clock rate of 100 kHz. For unity-gain configuration, the rms noise from 10 Hz to 10 kHz was 60 μ V with a $1/f$ spectrum, after circuit precautions were taken to reduce the common-mode noise from power supply and ground. To separate the amplifier random noise from that due to the switched capacitors, the passive

filter of Fig. 2(b) was then studied. Fig. 10 shows a spectrum analyzer photograph for the passive single pole filter with a 38 pF load. The top trace is the frequency response up to 50 kHz. The bottom trace shows the noise spectrum (with a low noise preamplifier of gain 70 dB). The noise spectrum at 100 Hz bandwidth averages ~ 130 dB.

The rms random noise from 10 Hz to 10 kHz was measured to be 7 μ V. This suggests that as far as the switched capacitor circuits are concerned, independent of the operational amplifier, it is possible to attain a signal-to-noise ratio of over 100 dB for audio filtering, assuming a 1-V dynamic range.

D. A Second-Order Bandpass Filter

A bandpass filter was designed using the same chip described in Section III-A. The transfer function realized is of the form:

$$H(s) = \frac{GS}{S^2 + \frac{\omega_p}{Q_{po}} S + \omega_p^2} \quad (11)$$

where ω_p is the resonant frequency in radians per second, Q_{po} is the nominal selectivity, and GQ_{po}/ω_p is the gain at resonance. The topology chosen to realize the above transfer function is the so-called biquad configuration [9]. This configuration was chosen because it allows noninteractive variation of the resonant frequency and the selectivity of the filter by changing individual resistors (in our case, switched capacitors). The circuit required three of the test chips, and is shown in Fig. 11. The block (C, f) denotes the switched capacitor whose resistive equivalent value is $1/fC$. The list of selected capacitors and frequency multiples used, which might be called the program for the filter, is shown at the bottom left of the figure.

In this filter, the gain at resonance is controlled by the ratio of the switched capacitor values only, and is independent of the value of C' . Identical sampling frequencies f_1 and f_2 were used so that the gain was only determined by the capacitive ratio C_1/C_2 . The selectivity Q of the filter was adjusted by varying the frequency ratio f_4/f_2 , using equal values of capacitors ($C_2 = C_4$). All clocks were synchronized to a master clock of frequency f_o .

The unit II in Fig. 11 must function as an inverting amplifier

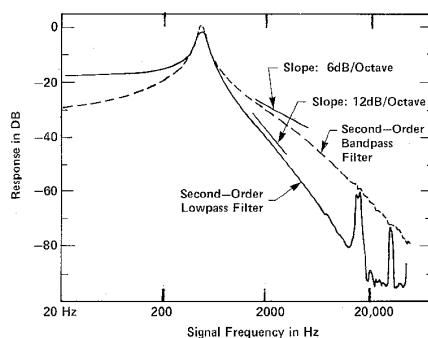


Fig. 11. Second-order active bandpass switched capacitor filter circuit using the biquad configuration.

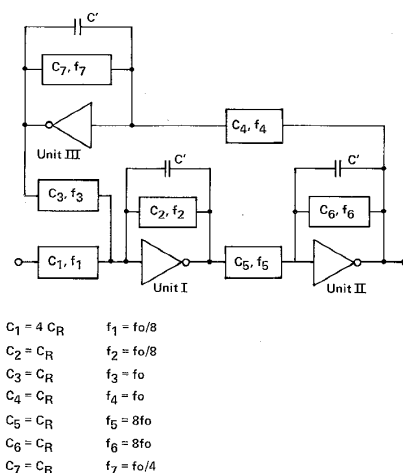


Fig. 12. Frequency response of the filter circuit shown in Fig. 11.

of unity gain. To suppress clock feedthrough (see Section II-D), the relatively large integrating capacitor C' was used and the sampling frequencies for the switched capacitors in unit II were increased by a factor of 8 to make the corner frequency of unit II relatively high.

The frequency response of the circuit is shown in Fig. 12. The sampling frequency for the master clock f_o was 125 kHz. The center frequency for the bandpass filter is at approximately 500 Hz. The upper curve shows the second-order bandpass transfer function, while the lower curve is the second-order low-pass function. The measured Q of the filter is 7.07 compared to a theoretical Q of 8. The slopes of the transfer functions beyond the resonant frequency are seen to correspond closely to the theoretical rolloff for the bandpass and low-pass functions, respectively. However, the slope of the bandpass transfer function does not follow the 6 dB/octave rolloff near the low frequency limit of the circuit because of the additional feedback resistance used for the integrating block (unit III in Fig. 11). Although aliasing occurs above the lowest clock frequency in the circuit, the response has been

shown for the extended frequency range, to indicate the amplitude of the clock feedthrough. In the low-pass transfer function, the first feedthrough peak occurs at a frequency corresponding to f_1 and f_2 (15.625 kHz), while the next peak occurs at the frequency corresponding to f_7 (31.25 kHz).

IV. CONCLUSIONS

We have demonstrated the possibility of replacing active RC filters in the audio frequency range with fully integrated MOS LSI circuits, using switched capacitor elements in place of resistors. It is possible to modify the filter characteristics such as gain, cut-off frequency or resonant frequency, and selectivity, by varying either the switched-capacitor clock frequencies, or the capacitor values, or both.

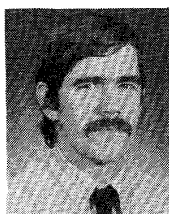
The conventional theory and design methods normally used for active RC filters may be directly applied in many practical situations without significant change, or used as a design aid along with more exact z -transform analysis. The clocks required are simple. As the switched capacitor is, by itself,

passive in nature, it does not cause problems for stability apart from that which is inherent in active *RC* filters.

Both "series-" and "parallel-" switched capacitor configurations have been investigated experimentally. We believe the series-switched capacitor to be the more useful of the two, because the parallel-switched capacitor introduces an additional delay term (Z^{-1}) into the transform equations, complicating the analysis and the circuit behavior.

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