



US 20020118067A1

(19) **United States**

(12) **Patent Application Publication**
Hirayama

(10) **Pub. No.: US 2002/0118067 A1**

(43) **Pub. Date: Aug. 29, 2002**

(54) **ANALOG AMPLIFIER CIRCUIT**

Publication Classification

(75) **Inventor: Tomohisa Hirayama, Tokyo (JP)**

(51) **Int. Cl.⁷ H03F 3/191**

(52) **U.S. Cl. 330/302**

Correspondence Address:

FOLEY AND LARDNER

SUITE 500

3000 K STREET NW

WASHINGTON, DC 20007 (US)

(57)

ABSTRACT

(73) **Assignee: NEC CORPORATION**

(21) **Appl. No.: 10/079,536**

(22) **Filed: Feb. 22, 2002**

(30) **Foreign Application Priority Data**

Feb. 23, 2001 (JP) 2001-048037

An analog amplifier circuit having an amplifier, an input matching circuit thereof and an output matching circuit thereof, said input matching circuit and said output matching circuit comprising: a circuit portion which capacitively functions with respect to a first frequency while inductively functions with respect to a second frequency, so as to match with respect to both of said first frequency and second frequency.

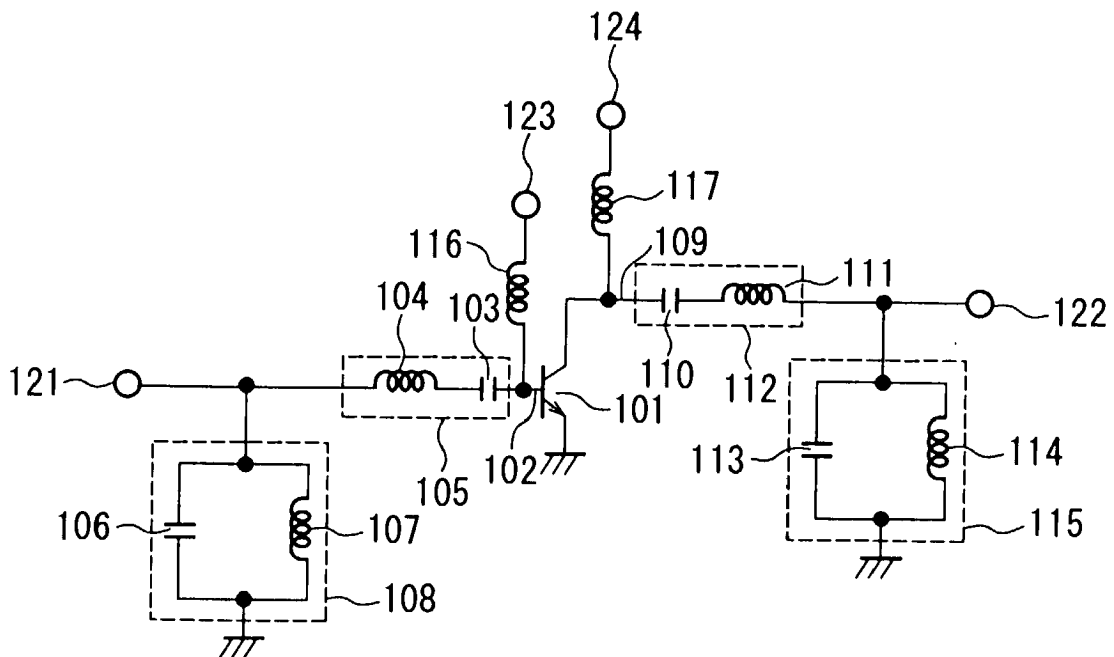


FIG. 1

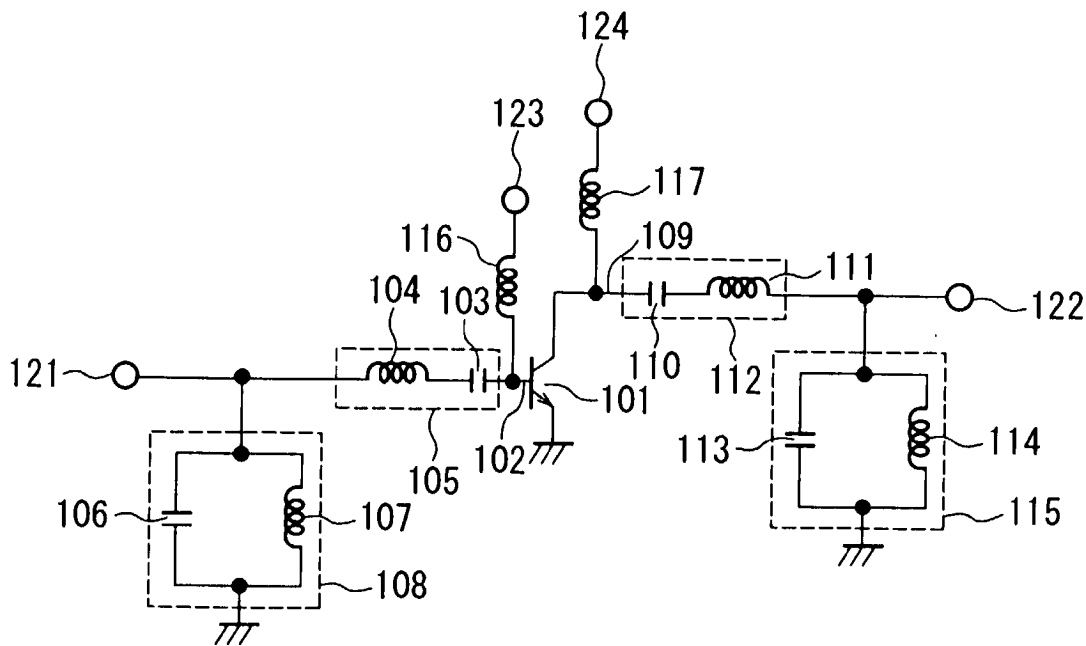


FIG. 2A

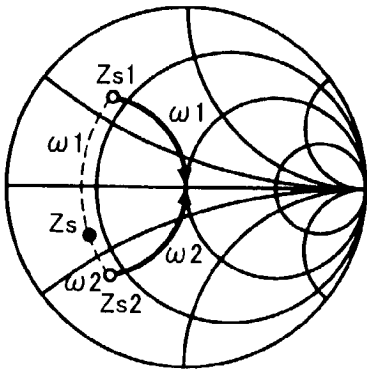


FIG. 2B

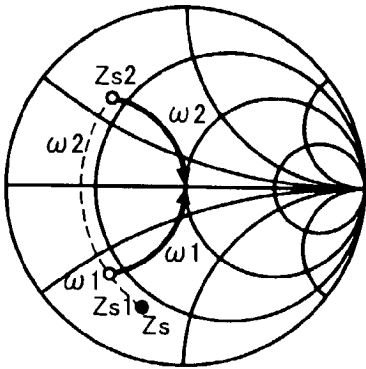


FIG. 2C

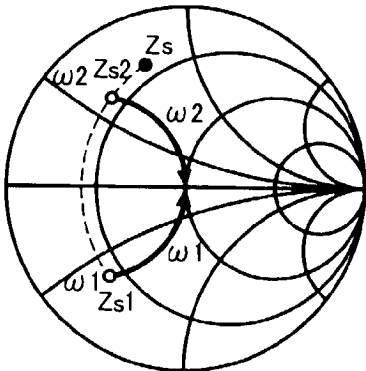


FIG. 3

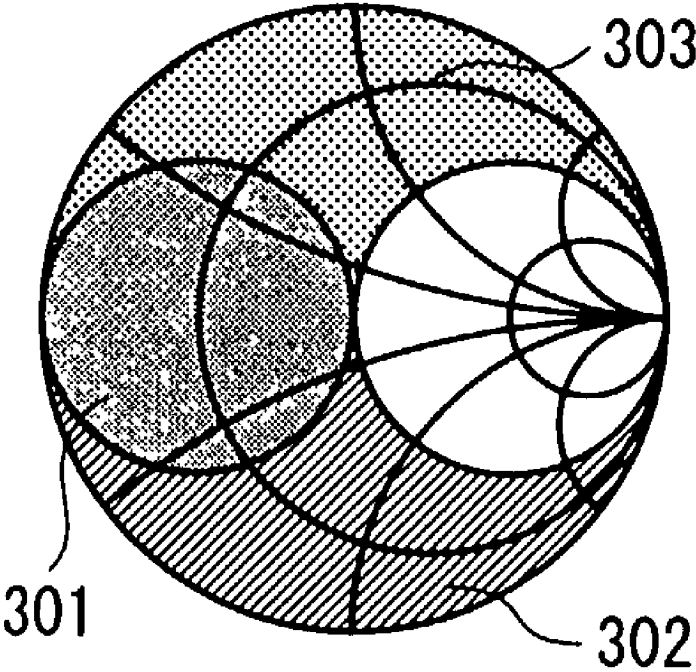


FIG. 4

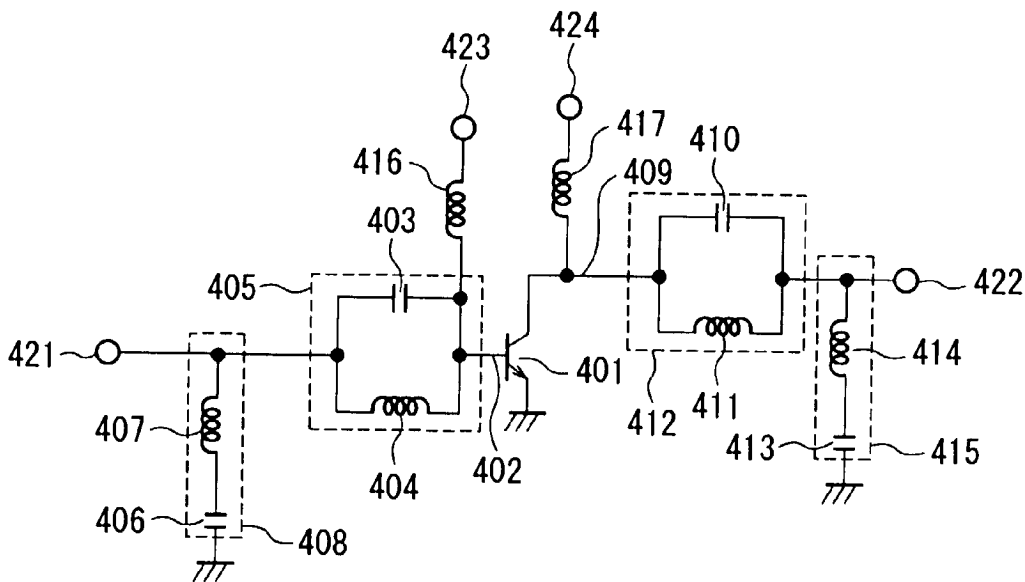


FIG. 5A

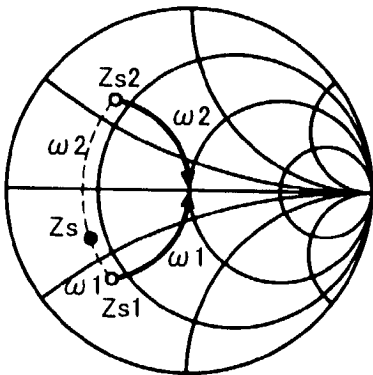


FIG. 5B

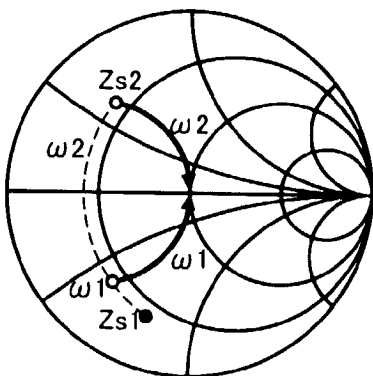


FIG. 5C

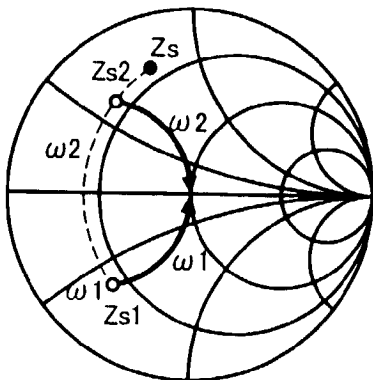


FIG. 6

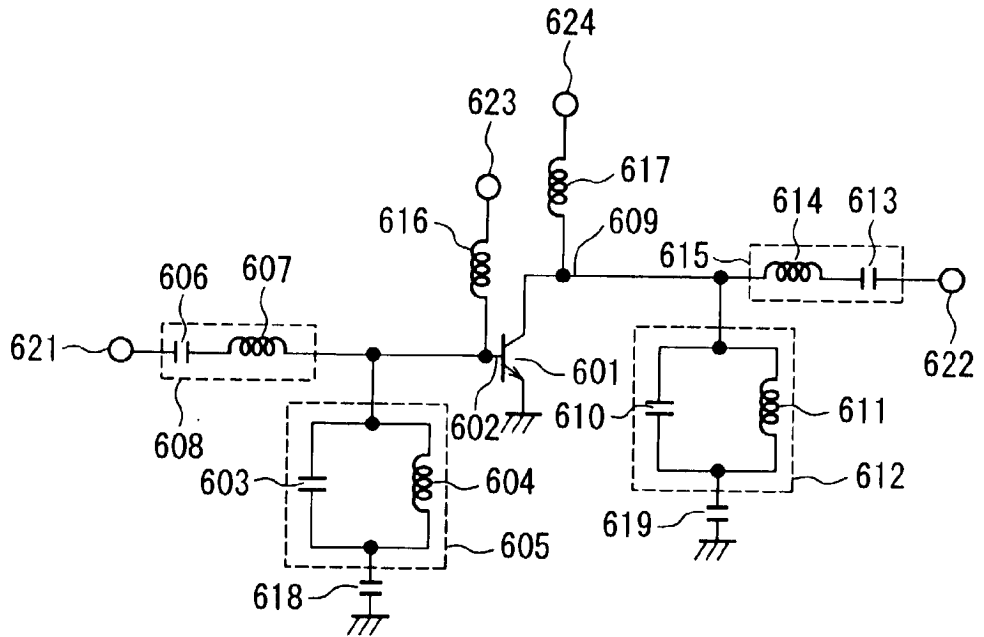


FIG. 7A

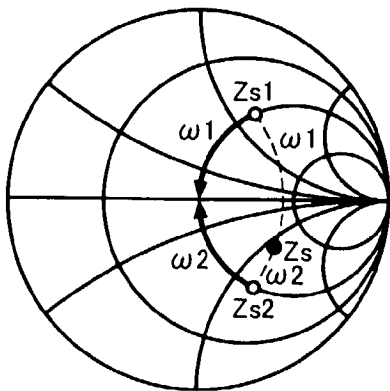


FIG. 7B

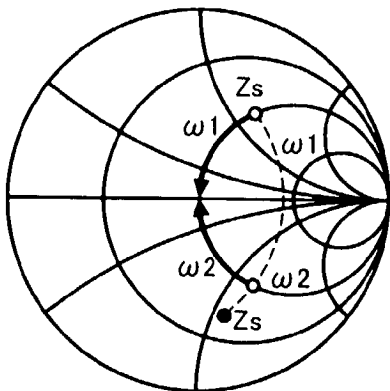


FIG. 7C

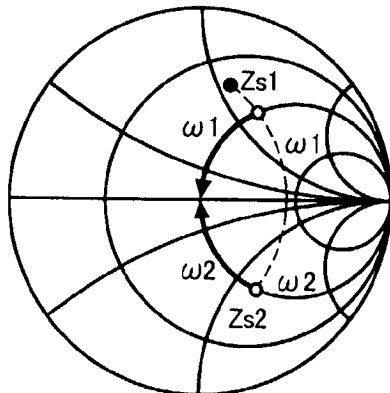


FIG. 8

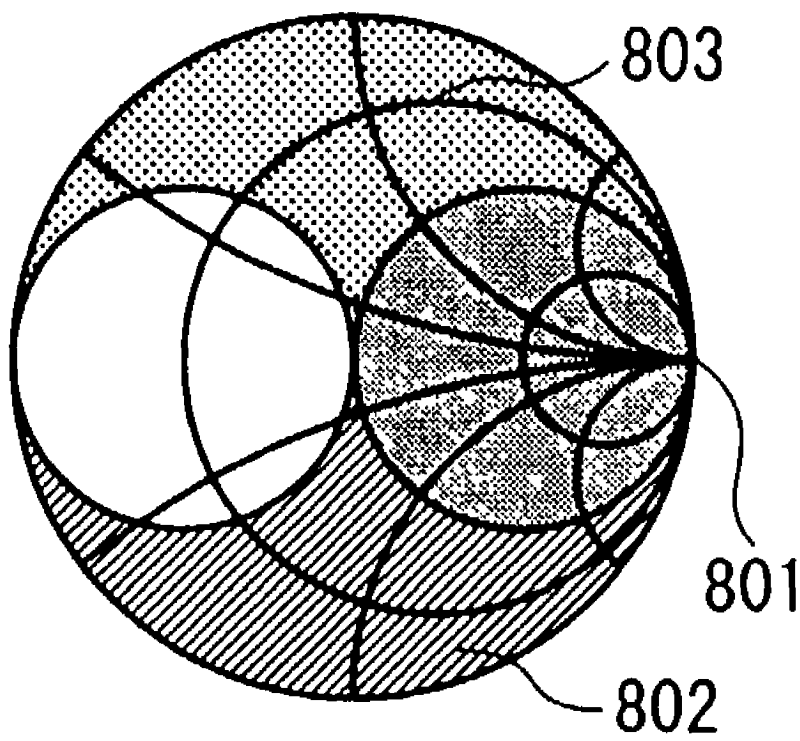


FIG. 9

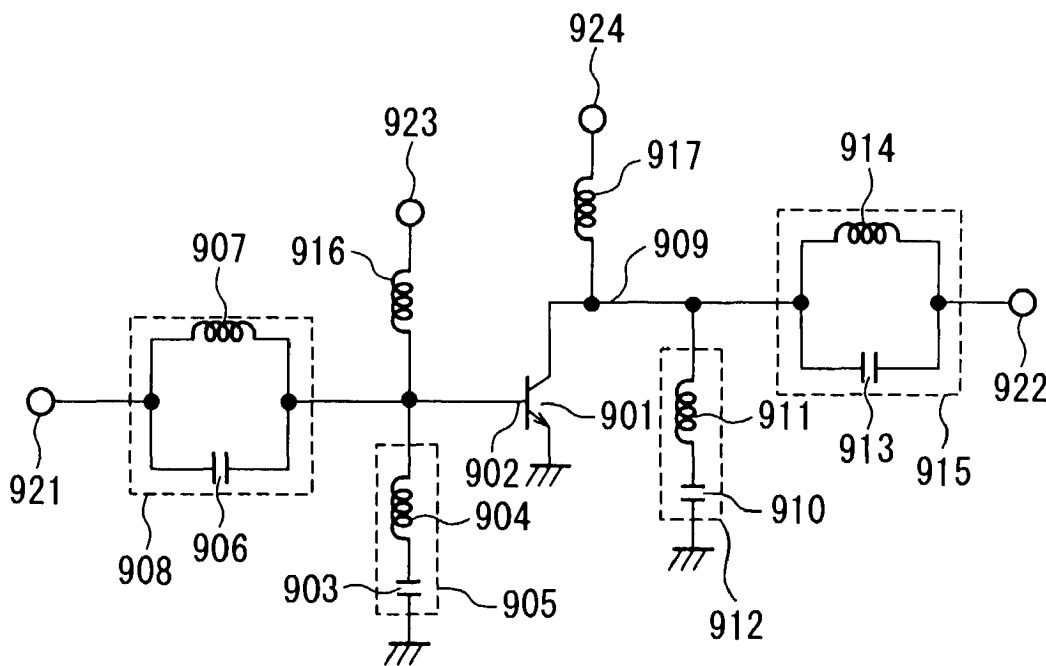


FIG. 10A

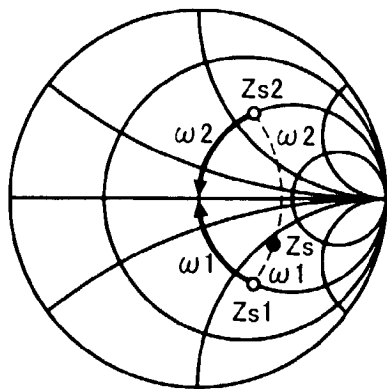


FIG. 10B

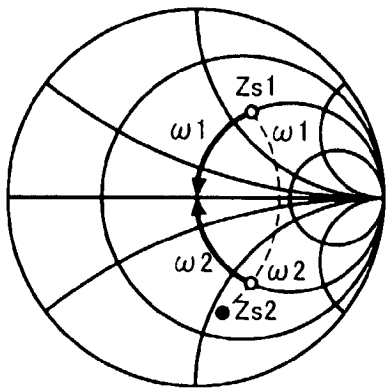


FIG. 10C

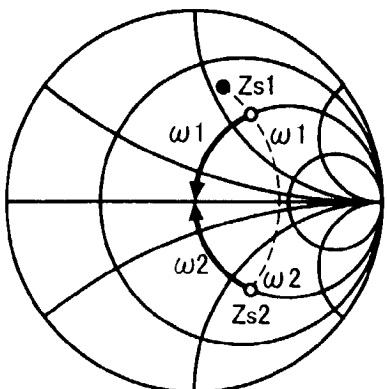


FIG. 11

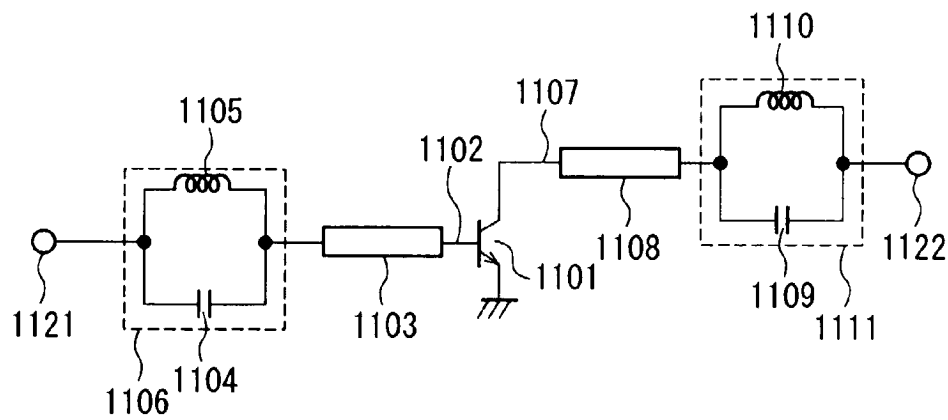


FIG. 12

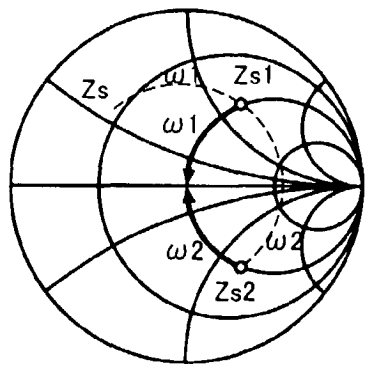


FIG. 13

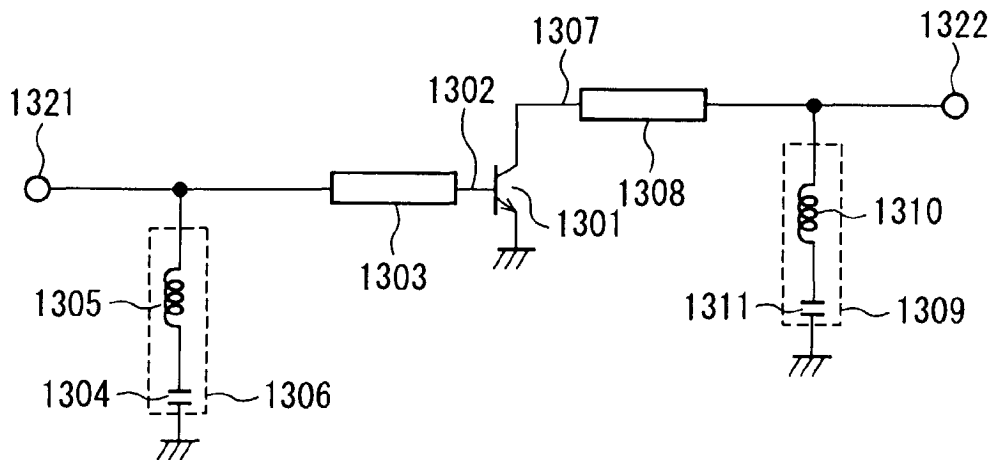


FIG. 14

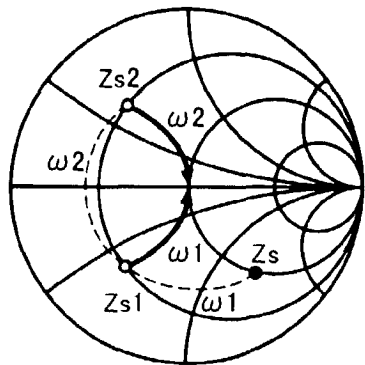
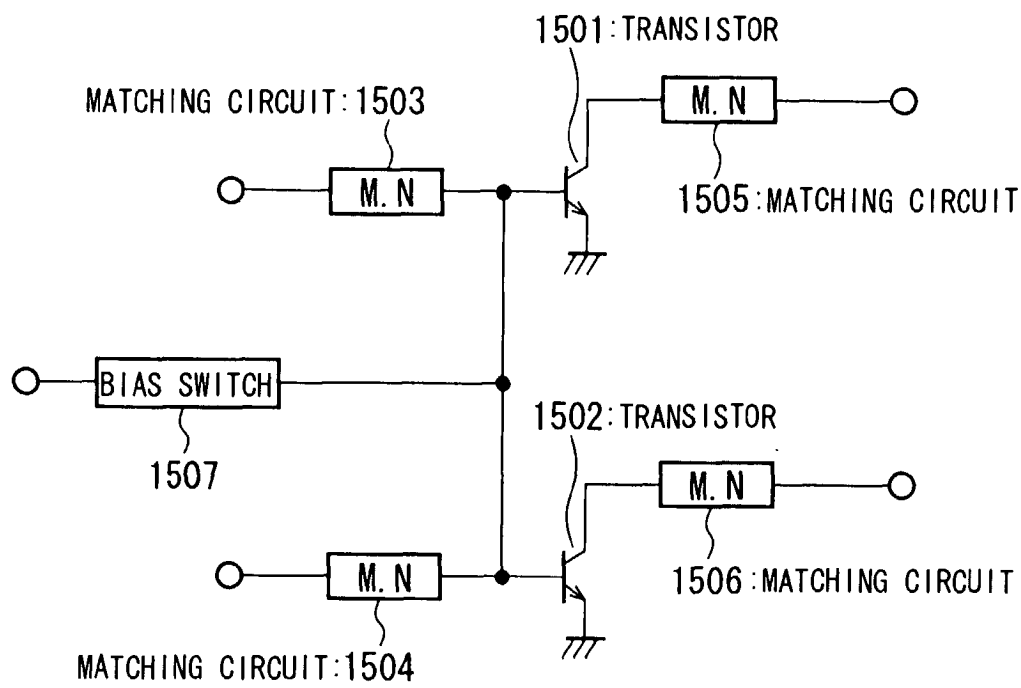


FIG. 15
PRIOR ART



ANALOG AMPLIFIER CIRCUIT

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to an analog amplifier circuit and, more particularly, to an amplifier circuit, which can be suitably applied to an amplifier circuit for a dual band.

[0003] 2. Related Background Art

[0004] In an amplifier circuit to be used in a mobile terminal such as a mobile telephone or a personal handy phone system (abbreviated as "a PHS"), an impedance is normally converted by the use of a matching circuit connected to an amplifier in such a manner as to obtain an optimum noise figure, an optimum gain, an optimum efficiency or an optimum distortion at a required frequency. An amplifier to be used at a dual band has been required for a recent mobile telephone. As described in the literature (for example, IEEE, Journal of Solid-State Circuit, Vol. 35, August, 2000, p. 1109), there has been proposed a dual band amplifier circuit in which a power amplifier having respective matching circuits for two frequencies is provided for switching the matching circuits according to a frequency that is used.

[0005] FIG. 15 is a circuit diagram illustrating the arrangement of a conventional dual band amplifier circuit. As illustrated in FIG. 15, two amplifiers (i.e., transistors 1501 and 1502) which are matched according to frequencies, respectively, are provided in such a manner as to correspond to a dual band by switching the two amplifiers according to a frequency band to be used by means of a switch 1507.

[0006] However, in the conventional amplifier circuit as illustrated in FIG. 15, because the amplifiers which are matched according to the frequency are provided, four matching circuits 1503 to 1506 and the two amplifiers 1501 and 1502 are required, thereby increasing the area of a chip, and further, inducing an increase in cost.

SUMMARY OF THE INVENTION

[0007] Consequently, an object of the present invention is to provide an analog amplifier circuit that can be used at two frequency bands, wherein the area of a chip can be reduced, and further, the cost can be reduced.

[0008] To achieve the above-noted objects, the present invention adopts the following basic technical constitution.

[0009] The aspect of the present invention is an analog amplifier circuit having an amplifier, an input matching circuit thereof and an output matching circuit thereof, the input matching circuit and the output matching circuit comprising: a circuit portion which capacitively functions with respect to a first frequency while inductively functions with respect to a second frequency, so as to perform impedance matching with respect to both of the first frequency and second frequency that is different from the first frequency.

[0010] According to the present invention, a series resonance circuit comprising an inductor and a capacitor is used as the circuit which becomes capacitive with respect to the first frequency while becomes inductive with respect to the

second frequency which is different from the first frequency in the matching circuit. Otherwise, a parallel resonance circuit comprising an inductor and a capacitor is used as the circuit that becomes capacitive with respect to the first frequency while becomes inductive with respect to the second frequency in the matching circuit.

[0011] Furthermore, the another aspect of the present invention is an analog amplifier circuit having an amplifier, an input matching circuit thereof and an output matching circuit thereof, the input matching circuit and the output matching circuit comprising: a phase rotating element for rotating a phase of an input signal to the amplifier or an output signal therefrom, so as to set an impedance of the phase rotating element in such a manner as to become inductive with respect to the first frequency while to become capacitive with respect to the second frequency which is different from the first frequency; and a circuit portion which capacitively functions with respect to the first frequency while inductively functions with respect to the second frequency, so as to perform impedance matching with respect to both of the first frequency and second frequency.

[0012] According to the present invention, a series resonance circuit comprising an inductor and a capacitor is used as the circuit adjusted in such a manner as to become capacitive with respect to the first frequency while to become inductive with respect to the second frequency; in the meantime, a parallel resonance circuit comprising an inductor and a capacitor is used as the circuit adjusted in such a manner as to become capacitive with respect to the first frequency while to become inductive with respect to the second frequency. According to the present invention, a transmission line is used as the phase rotating element.

[0013] Moreover, according to the present invention, an impedance can be matched such that each of reflection coefficients from a signal source or a load is 0.3 or less with respect to the two frequencies, that is, a maximum gain of the amplifier can be achieved in the above mentioned matched state. According to the present invention, the impedance can be matched within the circle of a constant noise figure, which is lower, by 0.5 dB than in the matched state in which minimum noise characteristics of the amplifier can be achieved with respect to the two frequencies.

[0014] Additionally, according to the present invention, the impedance can be matched within a constant output circle, which is lower by 0.5 dB than in the matched state in which a maximum saturated output of the amplifier can be achieved with respect to the two frequencies. Alternatively, the impedance is matched within a circle of a constant efficiency, which is lower, by 5% than in the matched state in which a maximum efficiency of the amplifier can be achieved with respect to the two frequencies. According to the present invention, the amplifier is a bipolar transistor or a field effect transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIG. 1 is a circuit diagram of the present invention.

[0016] FIG. 2A is a diagram illustrating the locus of impedance conversion in the first embodiment of the present invention.

[0017] FIG. 2B is a diagram illustrating the locus of impedance conversion in the second embodiment of the present invention.

[0018] FIG. 2C is a diagram illustrating the locus of impedance conversion in the third embodiment of the present invention.

[0019] FIG. 3 is a diagram illustrating impedance regions of a transistor in which a impedance can be converted to 50Ω in each of first to sixth embodiments according to the present invention.

[0020] FIG. 4 is another circuit diagram of the present invention.

[0021] FIG. 5A is a diagram illustrating the locus of impedance conversion in the fourth embodiment of the present invention.

[0022] FIG. 5B is a diagram illustrating the locus of impedance conversion in the fifth embodiment of the present invention.

[0023] FIG. 5C is a diagram illustrating the locus of impedance conversion in the sixth embodiment of the present invention.

[0024] FIG. 6 is another circuit diagram of the present invention.

[0025] FIG. 7A is a diagram illustrating the locus of impedance conversion in the seventh embodiment of the present invention.

[0026] FIG. 7B is a diagram illustrating the locus of impedance conversion in the eighth embodiment of the present invention.

[0027] FIG. 7C is a diagram illustrating the locus of impedance conversion in the ninth embodiment of the present invention.

[0028] FIG. 8 is a diagram illustrating impedance regions of a transistor in which a impedance can be converted to 50Ω in each of seventh to twelfth embodiments according to the present invention.

[0029] FIG. 9 is another circuit diagram of the present invention.

[0030] FIG. 10A is a diagram illustrating the locus of impedance conversion in the tenth embodiment of the present invention.

[0031] FIG. 10B is a diagram illustrating the locus of impedance conversion in the eleventh embodiment of the present invention.

[0032] FIG. 10C is a diagram illustrating the locus of impedance conversion in the twelfth embodiment of the present invention.

[0033] FIG. 11 is a circuit diagram illustrating the arrangement of a 13th embodiment according to the present invention.

[0034] FIG. 12 is a diagram illustrating the locus of impedance conversion in the 13th embodiment according to the present invention.

[0035] FIG. 13 is a circuit diagram illustrating the arrangement of a 14th embodiment according to the present invention.

[0036] FIG. 14 is a diagram illustrating the locus of impedance conversion in the 14th embodiment according to the present invention.

[0037] FIG. 15 is a circuit diagram illustrating the arrangement of a conventional amplifier circuit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0038] A description will be given below of modes carrying out the present invention. In configuring an amplifier circuit having a matching circuit, passive elements for use in the matching circuit mostly include a capacitor, an inductor and a transmission line without any electric power loss. Since an impedance of each of these elements is varied according to a frequency, it is difficult to match two frequency bands at the same time in the normal circuit arrangement.

[0039] In view of this fact, two frequencies are matched at the same time with a circuit arrangement as illustrated in FIG. 1 according to the present invention. In FIG. 1, each of circuits 105, 108, 112 and 115 is either a series resonance circuit or a parallel resonance circuit.

[0040] For example, the circuit 105 is a series resonance circuit while the circuit 108 is a parallel resonance circuit. Explanation will be made on the case where an input impedance of a transistor:

$$Z_s = 50 \times (0.3 - j0.2) = 15 - j10$$

[0041] (wherein $j^2 = -1$)

[0042] is matched to 50Ω with respect to two angular frequencies ω_1 and ω_2 (ω is $2\pi f$, wherein f represents a frequency, and here, ω is hereinafter referred to as "a frequency").

[0043] In the series resonance circuit 105 connected to a transistor 101, values of an inductor 104 and a capacitor 103, both of which are used in the resonance circuit 105, are suitably selected, and further, its resonance frequency is set between the first frequency ω_1 and the second frequency ω_2 ($\omega_1 < \omega_2$). Then, the impedance of the resonance circuit becomes inductive with respect to the first frequency ω_1 while the impedance of the resonance circuit becomes capacitive with respect to the second frequency ω_2 in the resonance circuit as a whole, thus producing a feature that the resonance circuit looks like separate elements with respect to the two frequencies ω_1 and ω_2 .

[0044] At this time, an input impedance of the device:

$$Z_s = 50 \times (0.3 - j0.2)$$

[0045] is moved clockwise along a constant resistance circle, in which $R = 50 \times 0.3$ (Ω), as illustrated in FIG. 2 (see an arrow ω_1 in FIG. 2), since the impedance of the resonance circuit 105 is inductive at the first frequency ω_1 by the circuit 105.

[0046] In contrast, the input impedance of the device is moved counterclockwise on the same constant resistance circle, as indicated by another arrow in FIG. 2, since the impedance of the resonance circuit is capacitive at the second frequency ω_2 .

[0047] Here, in order to convert the impedance to 50Ω by the use of the circuit 108, the destination of the conversion

by the circuit **105** need be located along a constant conductance circle, in which $G=0.02 \times 1$ (S), passing through the center of the Smith chart.

[0048] The values of the capacitor **104** and the inductor **103**, which meet the above-described condition, are determined as described below.

[0049] Since an intersection between the constant resistance circle, in which $R=50 \times 0.3$ (Ω), and the constant conductance circle, in which $G=0.02 \times 1$ (S), is located at $50 \times (0.3 + j0.46)$, an inductance **L1** required by the resonance circuit **105** with respect to the first frequency $\omega 1$ becomes as follows:

$$j\omega L1 = 50 \times (0.3 + j0.46) - 50 \times (0.3 - j0.2) = j33$$

[0050] In the same manner, since another intersection between the above-described two circles is located at $50 \times (0.3 - j0.46)$, a capacitance required by the resonance circuit **105** with respect to the second frequency $\omega 2$ becomes as follows:

$$1/j\omega 2C1 = 50 \times (0.3 - j0.46) - 50 \times (0.3 - j0.2) = -j13$$

[0051] As a result, since the impedance of the entire resonance circuit is $j(\omega L - 1/\omega C)$, the inductance **L1** of the resonance circuit **105** with respect to the first frequency $\omega 1$ and the capacitance **C1** of the resonance circuit **105** with respect to the second frequency $\omega 2$ can be obtained by getting solutions to the following two equations:

$$\omega L - 1/\omega 1C = \omega L1 = 33$$

[0052] with respect to the first frequency $\omega 1$; and

$$\omega 2L - 1/\omega 2C = 1/\omega 2C1 = 13$$

[0053] with respect to the second frequency $\omega 2$

[0054] wherein reference character L designates an inductance value of the inductor **104** for use in the circuit **105** and reference character C denotes a capacitance value of the capacitor **103**.

[0055] Since unknown values in the above-described two equations are the inductance L and the capacitance C in this case, each of the equations has a unique solution. Consequently, the use of the series resonance circuit **105** enables the impedance of the device to be converted to the value along the constant conductance circle at the two frequencies.

[0056] Thereafter, the two points along the constant conductance circle, in which $G=0.02$ (S), converted by the series resonance circuit **105** are converted into 50Ω by the parallel resonance circuit **108**.

[0057] In the case of the parallel resonance circuit, values of the inductor and the capacitor, both of which are used in the resonance circuit, are suitably selected, and further, its resonance frequency is set between the first frequency $\omega 1$ and the second frequency $\omega 2$ ($\omega 1 < \omega 2$). Then, the impedance of the resonance circuit becomes capacitive with respect to the first frequency $\omega 1$ while the impedance of the resonance circuit becomes inductive with respect to the second frequency $\omega 2$ in the resonance circuit.

[0058] In order to convert the points on the circle, in which $G=0.02$ (S), that is, $50 \times (0.3 + j0.46)$ and $50 \times (0.3 - j0.46)$ {which are $0.02 \times (1 - j1.5)$ and $0.02 \times (1 + j1.5)$ based on an

admittance, respectively} into 50Ω , **C2** and **L2** meeting equations below are required:

$$j\omega 1C2 = 0.02 - 0.02 \times (1 - j1.5) = j0.03$$

[0059] with respect to the first frequency $\omega 1$; and

$$1/j\omega 2L2 = 0.02 - 0.02 \times (1 + j1.5) = -j0.03$$

[0060] with respect to the second frequency $\omega 2$.

[0061] Therefore, in order to establish the inductance value **L2** and capacitance value **C2** of the parallel resonance circuit **108**, since the entire admittance is $\omega C - 1/\omega L$, the inductance **L2** of the parallel resonance circuit **108** and the capacitance **C2** of the resonance circuit can be obtained by getting solutions to the following two equations:

$$\omega 1C - 1/\omega 1L = 0.03; \text{ and}$$

$$\omega 2C - 1/\omega 2L = -0.03$$

[0062] wherein reference character L designates an inductance value of an inductor **107** for use in the circuit **108** and reference character C denotes a capacitance value of a capacitor **106**.

[0063] Since unknown values in the above-described two equations are L and C in this case, each of the equations has a unique solution. Consequently, the use of the parallel resonance circuit **108** enables the impedance of the device to be converted to 50Ω at the two frequencies.

[0064] Although the explanation has been made on the circuit arrangement and its function, in which the impedance:

$$R = 50 \times (0.3 - j0.2) = 15 - j10$$

[0065] is matched to 50Ω at the two frequencies, the circuit **105** may be a parallel resonance circuit while the circuit **108** may be a series resonance circuit according to the impedance of the device.

[0066] Alternatively, as illustrated in **FIG. 9** or **11**, a parallel circuit may be first connected to the input terminal, and then, a series circuit may be connected to the parallel circuit.

[0067] With any arrangement, the element parameters are determined based on the same concept as that of the above-described specific mode, thus producing the same functions and effects as those in the above-described specific mode.

[0068] In another mode according to the present invention, a impedance of a device can be converted into a desired impedance by the use of a resonance circuit after performing a phase shift of the impedance on a transmission line. Referring to **FIG. 11**, a phase is rotated on a transmission line **1103** in such a manner that an impedance of an amplifier becomes inductive at a first frequency $\omega 1$ while it becomes capacitive at a second frequency $\omega 2$, and then, the impedance is converted into a value around the center of the Smith chart by the resonance circuit.

[0069] For example, when input impedance of the device $R = 50 \times (0.3 + j0.46)$ (Ω) is matched to 50Ω , the length of the transmission line **1103** for rotating the phase is designed such that the phase is rotated by 37° at the first frequency $\omega 1$ while by 90° at the second frequency $\omega 2$, so that the impedance after the rotation of the phase becomes $50 + j76$ (Ω) which is inductive at the first frequency $\omega 1$ while $50 - j76$ (Ω) which is capacitive at the second frequency $\omega 2$, as illustrated in **FIG. 12**.

[0070] Furthermore, since in this case, the input impedance is on a constant resistance circle, in which $R=50\Omega$, a

parallel resonance circuit is connected in series, in which the impedance is $-j76\Omega$ at ω_1 while $j76\Omega$ at ω_2 , so that the impedance can be converted to 50Ω at the center of the Smith chart at both of the two frequencies, for the same reason as described above.

[0071] In this manner, the use of the transmission line and the resonance circuit enables the impedance to be converted at both of the two frequencies.

[0072] Moreover, the above-described technique can be applied to the case where an active element constituting the amplifier is either a bipolar transistor or a field effect transistor in the same manner, thus providing the matching circuit for converting the impedance into an optimum impedance at either of the two frequencies.

[0073] Next, examples according to the present invention will be described in reference to the accompanying drawings.

[0074] (First Embodiment)

[0075] FIG. 1 is a circuit diagram illustrating the arrangement of the first embodiment of the present invention. Referring to FIG. 1, there are provided a series resonance circuit 105 including a capacitor 103 and an inductor 104, connected in series between an input (a base) 102 of a transistor 101 having a grounded emitter and an input terminal 121; a parallel resonance circuit 108 including a capacitor 106 and an inductor 107, connected in parallel between the input terminal 121 and a ground; another series resonance circuit 112 including a capacitor 110 and an inductor 111, connected in series between an output (a collector) 109 of the transistor 101 and an output terminal 122; and another parallel resonance circuit 115 including a capacitor 113 and an inductor 114, connected in parallel between the output terminal 122 and the ground. Inductors 116 and 117 are bias choke coils, which are connected to the input and output of the transistor 101 at respective ones of ends thereof while connected to bias powers at the respective other ends 123 and 124 thereof.

[0076] In this example according to the present invention, the series resonance circuits 105 and 112 provided in series inductively function with respect to a first frequency ω_1 while they capacitively function with respect to a second frequency ω_2 ($\omega_1 < \omega_2$) by the above-described technique.

[0077] At this time, an input impedance Z_s is moved to points Z_{s1} and Z_{s2} with respect to ω_1 and ω_2 , respectively, on the Smith chart, as indicated by a broken line in FIG. 2A.

[0078] In contrast, the parallel resonance circuits 108 and 115 capacitively function with respect to the frequency ω_1 while they inductively function with respect to the frequency ω_2 . At this time, Z_{s1} and Z_{s2} are moved as indicated by a solid line in FIG. 2A. As a result, the impedance can be matched at one and the same point (to 50Ω in this example) with respect to both of the two frequencies.

[0079] Theoretically, in the case where the input/output impedance of the transistor 101 falls within a region 301 in FIG. 3, the impedance can be matched to 50Ω with respect to both of the two frequencies with the above-described arrangement.

[0080] (Second Embodiment)

[0081] Subsequently, a description will be given of a second embodiment of the present invention. In the second embodiment of the present invention, series resonance circuits 105 and 112 inductively function with respect to both of a first frequency ω_1 and a second frequency ω_2 in the arrangement illustrated in FIG. 1. In this case, if an impedance Z_s of a transistor falls within a region 302 in FIG. 3, the impedance can be matched to 50Ω with respect to both of the two frequencies. In other words, in the case where the input impedance of the device falls within the region 302, the parallel resonance circuits 108 and 115 convert the impedance of the device into 50Ω from a capacitive part (i.e., an imaginary part is negative) on a constant conductance circle, in which $G=0.02$ (S), with respect to the first frequency ω_1 while into 50Ω from an inductive part (i.e., an imaginary part is positive) with respect to the second frequency ω_2 . FIG. 2B is a diagram illustrating the locus of impedance conversion in the second embodiment of the present invention.

[0082] (Third Embodiment)

[0083] Furthermore, a description will be given of a third embodiment according to the present invention. In the third embodiment of the present invention, series resonance circuits 105 and 112 capacitively function with respect to both of a first frequency ω_1 and a second frequency ω_2 in the arrangement illustrated in FIG. 1. In this case, if an input impedance Z_s of a transistor falls within a region 303 in FIG. 3, the impedance can be matched to 50Ω with respect to both of the two frequencies. In other words, in the case where the impedance of the device falls within the region 303, the parallel resonance circuits 108 and 115 convert the impedance of the device into 50Ω from an inductive part (i.e., an imaginary part is positive) on a constant conductance circle, in which $G=0.02$ (S), with respect to the second frequency ω_2 while into 50Ω from a capacitive part (i.e., an imaginary part is negative) with respect to the first frequency ω_1 . FIG. 2C is a diagram illustrating the locus of impedance conversion in the third embodiment of the present invention.

[0084] (Fourth Embodiment)

[0085] FIG. 4 is a circuit diagram illustrating the arrangement of another example according to the present invention. Referring to FIG. 4, in this embodiment, there are provided a parallel resonance circuit 405 including a capacitor 403 and an inductor 404 connected in parallel between an input (a base) 402 of a transistor 401 having a grounded emitter and an input terminal 421; a series resonance circuit 408 including a capacitor 406 and an inductor 407 connected in series between the input terminal 421 and a ground; another parallel resonance circuit 412 including a capacitor 410 and an inductor 411 connected in series between an output (a collector) 409 of the transistor 401 and an output terminal 422; and another series resonance circuit 415 including a capacitor 413 and an inductor 414 connected in series between the output terminal 422 and the ground. Inductors 416 and 417 are bias choke coils, and terminals 423 and 424 are connected to bias power sources.

[0086] In the fourth embodiment of the present invention in FIG. 4, the parallel resonance circuits 405 and 412 provided in series capacitively function with respect to a first frequency ω_1 while they inductively function with respect to a second frequency ω_2 ($\omega_1 < \omega_2$) by the above-described technique. At this time, an input impedance Z_s is moved to

points Z_{s1} and Z_{s2} with respect to ω_1 and ω_2 , respectively, on the Smith chart, as indicated by a broken line in FIG. 5A.

[0087] In contrast, the series resonance circuits 108 and 115 inductively function with respect to the frequency ω_1 while they capacitively function with respect to the frequency ω_2 . At this time, Z_{s1} and Z_{s2} are moved as indicated by a solid line in FIG. 5A.

[0088] With this arrangement, the impedance can be matched at one and the same point (to 50Ω in this example) with respect to both of the two frequencies. Theoretically, in the case where the input/output impedance of the transistor falls within a region 301 in FIG. 3, the impedance can be matched to 50Ω with respect to both of the two frequencies with the above-described arrangement.

[0089] (Fifth Embodiment)

[0090] Subsequently, a description will be given of a fifth embodiment according to the present invention. In the fifth embodiment of the present invention, parallel resonance circuits 405 and 412 inductively function with respect to both of a first frequency ω_1 and a second frequency ω_2 in the arrangement illustrated in FIG. 4. In this case, if an input impedance Z_s of a transistor 401 falls within a region 302 in FIG. 3, the impedance can be matched to 50Ω with respect to both of the two frequencies. That is to say, in the case where the impedance of the device falls within the region 302, the series resonance circuits 408 and 415 convert the impedance of the device into 50Ω from a capacitive part (i.e., an imaginary part is negative) on a constant conductance circle, in which $G=0.02$ (S), with respect to the first frequency ω_1 while into 50Ω from an inductive part (i.e., an imaginary part is positive) with respect to the second frequency ω_2 . FIG. 5B is a diagram illustrating the locus of impedance conversion in the fifth embodiment of the present invention.

[0091] (Sixth Embodiment)

[0092] Next, a description will be given of a sixth embodiment according to the present invention. In the sixth embodiment of the present invention, parallel resonance circuits 405 and 412 capacitively function with respect to both of a first frequency ω_1 and a second frequency ω_2 in the arrangement illustrated in FIG. 4. In this case, if an input impedance Z_s of a transistor falls within a region 303 in FIG. 3, the impedance can be matched to 50Ω with respect to both of the two frequencies. In other words, in the case where the impedance of the device falls within the region 303, the series resonance circuits 408 and 415 convert the impedance of the device into 50Ω from an inductive part (i.e., an imaginary part is positive) on a constant conductance circle, in which $G=0.02$ (S), with respect to the second frequency ω_2 while into 50Ω from a capacitive part (i.e., an imaginary part is negative) with respect to the first frequency ω_1 . FIG. 5C is a diagram illustrating the locus of impedance conversion in the sixth embodiment of the present invention.

[0093] (Seventh Embodiment)

[0094] FIG. 6 is a circuit diagram illustrating the arrangement of a further example according to the present invention. Referring to FIG. 6, there are provided a parallel resonance circuit 605 including a capacitor 603 and an inductor 604 connected in parallel between an input (a base) 602 of a transistor 601 having a grounded emitter and a

ground; a series resonance circuit 608 including a capacitor 606 and an inductor 607 connected in series between the input 602 of the transistor 601 and an input terminal 621; another parallel resonance circuit 612 including a capacitor 610 and an inductor 611 connected in parallel between an output (a collector) 609 of the transistor 601 and the ground; and another series resonance circuit 615 including a capacitor 613 and an inductor 614 connected in series between the output 609 of the transistor 601 and an output terminal 622. Inductors 616 and 617 are bias choke coils. Here, reference numerals 618 and 619 designate DC cutting capacitors.

[0095] Subsequently, a description will be given of a seventh embodiment according to the present invention. In the seventh embodiment of the present invention, the parallel resonance circuits 605 and 612 inductively function with respect to a first frequency ω_1 while they capacitively function with respect to a second frequency ω_2 ($\omega_1 < \omega_2$) by the above-described technique in the arrangement illustrated in FIG. 6. At this time, an input impedance Z_s of the transistor is moved to points Z_{s1} and Z_{s2} on the Smith chart with respect to ω_1 and ω_2 , as indicated by a broken line in FIG. 7A.

[0096] In contrast, the series resonance circuits 608 and 615 capacitively function with respect to the frequency ω_1 while they inductively function with respect to the frequency ω_2 . At this time, Z_{s1} and Z_{s2} are moved as indicated by a solid line in FIG. 7A. As a result, the impedance can be matched at one and the same point (to 50Ω in this example) with respect to both of the two frequencies.

[0097] Theoretically, in the case where the input/output impedance of the transistor falls within a region 801 in FIG. 8, the impedance can be matched to 50Ω with respect to both of the two frequencies with the above-described arrangement.

[0098] (Eighth Embodiment)

[0099] Subsequently, a description will be given of an eighth embodiment according to the present invention. In the eighth embodiment of the present invention, parallel resonance circuits 605 and 612 inductively function with respect to both of a first frequency ω_1 and a second frequency ω_2 in the arrangement illustrated in FIG. 6. In this case, if an input impedance Z_s of a transistor falls within a region 802 in FIG. 8, the impedance can be matched to 50Ω with respect to both of the two frequencies. That is to say, in the case where the impedance of the device falls within the region 802, the series resonance circuits 608 and 615 convert the impedance of the device into 50Ω from an inductive part (i.e., an imaginary part is positive) on a constant resistance circle, in which $R=50\Omega$, with respect to ω_1 while into 50Ω from a capacitive part (i.e., an imaginary part is negative) with respect to ω_2 . FIG. 7B is a diagram illustrating the locus of impedance conversion in the eighth embodiment of the present invention.

[0100] (Ninth Embodiment)

[0101] Next, a description will be given of a ninth embodiment according to the present invention. In the ninth embodiment of the present invention, parallel resonance circuits 605 and 612 inductively function with respect to both of a first frequency ω_1 and a second frequency ω_2 in the arrangement illustrated in FIG. 6. In this case, if an input impedance Z_s of a transistor falls within a region 803 in

FIG. 8, the impedance can be matched to 50Ω with respect to both of the two frequencies. That is to say, in the case where the impedance of the device falls within the region **803**, the series resonance circuits **608** and **615** convert the impedance of the device into 50Ω from an inductive part (i.e., an imaginary part is positive) on a constant resistance circle, in which $R=50\Omega$, with respect to ω_1 while into 50Ω from a capacitive part (i.e., an imaginary part is negative) with respect to ω_2 . **FIG. 7C** is a diagram illustrating the locus of impedance conversion in the ninth embodiment of the present invention.

[0102] (Tenth Embodiment)

[0103] **FIG. 9** is a circuit diagram illustrating the arrangement of a still further example according to the present invention. Referring to **FIG. 9**, in this example, there are provided a series resonance circuit **905** including a capacitor **903** and an inductor **904** connected in series between an input (a base) **902** of a transistor **901** having a grounded emitter and a ground; a parallel resonance circuit **908** including a capacitor **906** and an inductor **907** connected in parallel between the input **902** of the transistor **901** and an input terminal **921**; another series resonance circuit **912** including a capacitor **910** and an inductor **911** connected in series between an output (a collector) **909** of the transistor **901** and the ground; and another parallel resonance circuit **915** including a capacitor **913** and an inductor **914** connected in parallel between the output **909** of the transistor **901** and an output terminal **922**. Inductors **916** and **917** are bias choke coils, to which bias voltages are supplied from terminals **923** and **924**, respectively.

[0104] Subsequently, a description will be given of a tenth embodiment according to the present invention. In the tenth embodiment of the present invention, the series resonance circuits **905** and **912** inductively function with respect to a first frequency ω_1 while they capacitively function with respect to a second frequency ω_2 ($\omega_1 < \omega_2$) by the above-described technique in the arrangement illustrated in **FIG. 9**. At this time, a transistor terminal impedance Z_s is moved to points Z_{s1} and Z_{s2} on the Smith chart with respect to ω_1 and ω_2 , as indicated by a broken line in **FIG. 10A**.

[0105] In contrast, the parallel resonance circuits **908** and **915** connected in series capacitively function with respect to the frequency ω_1 while they inductively function with respect to the frequency ω_2 . At this time, Z_{s1} and Z_{s2} are moved as indicated by a solid line in **FIG. 10A**. As a result, the impedance can be matched at one and the same point (to 50Ω in this example) with respect to both of the two frequencies.

[0106] Theoretically, in the case where the input/output impedance of the transistor falls within a region **801** in **FIG. 8**, the impedance can be matched to 50Ω with respect to both of the two frequencies.

[0107] (Eleventh Embodiment)

[0108] Subsequently, a description will be given of an eleventh embodiment according to the present invention. In the eleventh embodiment of the present invention, series resonance circuits **905** and **912** inductively function with respect to both of a first frequency ω_1 and a second frequency ω_2 in the arrangement illustrated in **FIG. 9**. In this case, if an input impedance Z_s of a transistor **901** falls within a region **802** in **FIG. 8**, the impedance can be

matched to 50Ω with respect to both of the two frequencies. That is to say, in the case where the impedance of the device (i.e., the transistor **901**) falls within the region **802**, the parallel resonance circuits **908** and **915** convert the impedance of the device into 50Ω from an inductive part (i.e., an imaginary part is positive) on a constant resistance circle, in which $R=50\Omega$, with respect to ω_1 while into 50Ω from a capacitive part (i.e., an imaginary part is negative) with respect to ω_2 . **FIG. 10B** is a diagram illustrating the locus of impedance conversion in the eleventh embodiment of the present invention.

[0109] (Twelfth Embodiment)

[0110] Next, a description will be given of a twelfth embodiment according to the present invention. In the twelfth embodiment of the present invention, series resonance circuits **905** and **912** capacitively function with respect to both of a first frequency ω_1 and a second frequency ω_2 in the arrangement illustrated in **FIG. 9**. In this case, if an input impedance of a transistor falls within a region **303** in **FIG. 3**, the impedance can be matched to 50Ω with respect to both of the two frequencies. In other words, in the case where the impedance of the device falls within the region **303**, the parallel resonance circuits **905** and **912** convert the impedance of the device into 50Ω from an inductive part (i.e., an imaginary part is positive) on a constant resistance circle, in which $R=50\Omega$, with respect to ω_1 while into 50Ω from a capacitive part (i.e., an imaginary part is negative) with respect to ω_2 . **FIG. 10C** is a diagram illustrating the locus of impedance conversion in the twelfth embodiment of the present invention.

[0111] Although the matching circuits respectively disposed at the input and the output are of the same type in the above described first to twelfth embodiments, matching circuits of different types in combination can produce the same effects.

[0112] (13th Embodiment)

[0113] **FIG. 11** is a circuit diagram illustrating the arrangement of a 13th embodiment according to the present invention. Referring to **FIG. 11**, in this embodiment, there are provided a phase rotating element **1103**, and a parallel resonance circuit **1106** including a capacitor **1104** and an inductor **1105** connected in parallel, the element **1103** and the circuit **1106** being connected in series between an input (a base) **1102** of a transistor **1101** having a grounded emitter and an input terminal **1121**; and a phase rotating element **1108**, and another parallel resonance circuit **1111** including a capacitor **1109** and an inductor **1110** connected in parallel, the element **1108** and the circuit **1111** being connected in series between an output (a collector) **1107** of the transistor **1101** and an output terminal **1122**. The phase of the input impedance and output impedance of the transistor **1101** is rotated so as to become inductive with respect to a first frequency ω_1 and capacitive with respect to a second frequency ω_2 , and further, the parallel resonance circuit which becomes capacitive with respect to the first frequency ω_1 while becomes inductive with respect to the second frequency ω_2 is connected in series, thereby matching the two frequencies at the same time. With respect to the frequencies ω_1 and ω_2 , a transistor terminal impedance Z_s is moved to an inductive impedance Z_{s1} at the first frequency ω_1 while to a capacitive impedance Z_{s2} at the second frequency ω_2 on the Smith chart by the phase

rotating elements **1103** and **1108**, as indicated by a broken line in **FIG. 12** (in this case, $\omega_1 < \omega_2$).

[0114] Moreover, when the parallel resonance circuits **1106** and **1111** capacitively function with respect to the first frequency ω_1 while they inductively function with respect to the second frequency ω_2 , Z_s moves as indicated by a solid line in **FIG. 12**. As a result, the impedance can be matched (to 50Ω in this example) with respect to the two frequencies. Additionally, the impedance of the device can be allowed to approach an optimum matching point.

[0115] (14th Embodiment)

[0116] **FIG. 13** is a circuit diagram illustrating the arrangement of a 14th embodiment according to the present invention. Referring to **FIG. 13**, in this embodiment, there are provided a phase rotating element **1303** connected between an input (a base) **1302** of a transistor **1301** and an input terminal **1321**; a series resonance circuit **1306** including a capacitor **1304** and an inductor **1305**, connected in series between a connecting point of the input terminal **1321** to the phase rotating element **1303** and a ground; a phase rotating element **1308** connected between an output (a collector) **1307** of the transistor **1301** and an output terminal **1322**; and another series resonance circuit **1311** including a capacitor **1309** and an inductor **1310**, connected between a connecting point of the phase rotating element **1308** to the output terminal **1322** and the ground. With this circuit arrangement, the phase of the input impedance and output impedance of the transistor **1301** are rotated so as to become capacitive with respect to a first frequency ω_1 and become inductive with respect to a second frequency ω_2 , and further, the circuit which becomes inductive with respect to the first frequency ω_1 while becomes capacitive with respect to the second frequency ω_2 is connected in parallel, thereby matching the two frequencies at the same time.

[0117] With respect to the frequencies ω_1 and ω_2 , a transistor terminal impedance Z_s is moved to a capacitive impedance Z_{s1} at the first frequency ω_1 while to an inductive impedance Z_{s2} at the second frequency ω_2 on the Smith chart by the phase rotating elements **1303** and **1308**, as indicated by a broken line in **FIG. 14** (in this case, $\omega_1 < \omega_2$).

[0118] Moreover, when the series resonance circuits **1306** and **1311** inductively function with respect to the first frequency ω_1 while they capacitively function with respect to the second frequency ω_2 , Z_s moves as indicated by a solid line in **FIG. 14**. As a result, the impedance can be matched (to 50Ω in this example) with respect to the two frequencies. In this way, the impedance of the device can be allowed to approach an optimum matching point.

[0119] (15th Embodiment)

[0120] In a 15th embodiment according to the present invention, when each of reflection coefficients from a signal source or a load is 0.3 or less with respect to the two frequencies, a maximum gain of the amplifier can be achieved in the matched state in each of the above-described first to 14th examples. In the case in which the reflection coefficient from the load or the signal source is 0.3 or less, i.e., -10 dB or less at the two frequencies, the amplifier circuit can achieve the maximum gain due to a reduced electric power loss.

[0121] (16th Embodiment)

[0122] In a 16th embodiment according to the present invention, the impedance can be within the circle of a constant noise figure which is higher by 0.5 dB than in the matched state in which minimum noise characteristics of the amplifier can be achieved with respect to the two frequencies in each of the above-described first to 14th embodiments. In this case, degradation of the noise characteristics from the optimum value can be suppressed to 12% or less, thereby achieving the excellent amplifier having a lower noise.

[0123] (17th Embodiment)

[0124] In a 17th embodiment according to the present invention, the impedance can be matched within a constant output circle which is lower by 0.5 dB than in the matched state in which a maximum saturated output of the amplifier can be achieved with respect to the two frequencies in each of the above-described first to 14th embodiments. In this case, degradation of the saturated output can be suppressed to 12% or less in a transmission power amplifier having a high saturated output.

[0125] (18th Embodiment)

[0126] In an 18th embodiment according to the present invention, the impedance is within a circle of a constant efficiency which is lower by 5% than in the matched state in which a maximum efficiency of the amplifier can be achieved with respect to the two frequencies in each of the above-described first to 14th embodiments.

[0127] Since power consumption of the power amplifier for the mobile terminal in the mobile telephone or the like occupies about 60% of the total power consumption, the present invention is effective because it can achieve the amplifier in which the degradation of efficiency can be suppressed to the minimum.

[0128] Although in each of the above-described embodiments, the bipolar transistor has been used as the amplifier device, a field effect transistor may be used instead. The amplifier circuit of a high gain can be achieved in the case of the use of the bipolar transistor; an amplifier circuit of a low cost can be achieved in a silicon-based device in the case of the use of the field effect transistor; and an amplifier circuit of a high efficiency can be achieved in a compound-based device in the case of the use of the field effect transistor. The optimum device can be appropriately selected according to the specifications required for the system.

[0129] As described above, the matching circuit according to the present invention is configured by the use of at least one of a circuit which becomes capacitive with respect to a first frequency while becomes inductive with respect to a second frequency, so as to match with respect to both of the first frequency and the second frequency at the same time, thereby producing the effect that the arrangement with only one amplifier can cover both of the two bands. In comparison with the conventional circuit arrangement, the elements can be reduced in size and number, thus reducing the area occupied by the amplifier circuit and reducing the manufacturing cost.

What is claimed is:

1. An analog amplifier circuit having an amplifier element, an input matching circuit thereof and an output

matching circuit thereof, said input matching circuit and said output matching circuit comprising:

a circuit portion which capacitively functions with respect to a first frequency while inductively functions with respect to a second frequency which is different from said first frequency, so as to perform impedance matching with respect to both of said first frequency and second frequency.

2. The analog amplifier circuit according to claim 1, wherein said circuit portion comprising a series resonance circuit having an inductor and a capacitor.

3. The analog amplifier circuit according to claim 1, wherein said circuit portion comprising a parallel resonance circuit having an inductor and a capacitor.

4. An analog amplifier circuit having an amplifier element, an input matching circuit thereof and an output matching circuit thereof, said input matching circuit and said output matching circuit comprising:

a phase rotating element for rotating a phase of an input signal to said amplifier element and that of an output signal therefrom, so as to set an impedance of said phase rotating element in such a manner as to become inductive with respect to said first frequency while to become capacitive with respect to said second frequency which is different from said first frequency; and

a circuit portion which capacitively functions with respect to said first frequency while inductively functions with respect to said second frequency, so as to perform impedance matching with respect to both of said first frequency and second frequency.

5. The analog amplifier circuit according to claim 4, wherein said circuit portion comprising a series resonance circuit having an inductor and a capacitor.

6. The analog amplifier circuit according to claim 4, wherein said circuit portion comprising a parallel resonance circuit having an inductor and a capacitor.

7. The analog amplifier circuit according to claim 4, wherein said phase rotating element comprising a transmission line.

8. The analog amplifier circuit according to claim 1, wherein each of reflection coefficients of a signal source side and a load side is 0.3 or less with respect to said first frequency and said second frequency, in a matched state.

9. The analog amplifier circuit according to claim 1, wherein an input impedance and output impedance of said analog amplifier circuit in a matched state falls within a circle of a constant noise figure which is higher by 0.5 dB on a Smith chart than a state in which minimum noise characteristics of said amplifier element can be achieved with respect to said first frequency and said second frequency.

10. The analog amplifier circuit according to claim 1, wherein an input impedance and output impedance of said analog amplifier circuit in a matched state falls within a circle of a constant output which is lower by 0.5 dB on a Smith chart than a state in which a maximum saturated output of said amplifier element can be achieved with respect to said first frequency and said second frequency.

11. The analog amplifier circuit according to claim 1, wherein an input impedance and output impedance of said analog amplifier circuit in a matched state falls within a circle of a constant efficiency which is lower by 5% on a Smith chart than a state in which a maximum efficiency of

said amplifier element can be achieved with respect to said first frequency and said second frequency.

12. The analog amplifier circuit according to claim 1, wherein said amplifier element comprising a bipolar transistor.

13. The analog amplifier circuit according to claim 1, wherein said amplifier element comprising a field effect transistor.

14. An analog amplifier circuit having a transistor serving as an amplifier, an input matching circuit thereof and an output matching circuit thereof, an input terminal of said analog amplifier circuit and an output terminal of said analog amplifier circuit,

said input matching circuit comprising:

a first series resonance circuit having a first capacitor and a first inductor, connected in series between an input terminal of said transistor and said input terminal of said analog amplifier circuit; and

a first parallel resonance circuit having a second capacitor and a second inductor, connected in parallel between said input terminal of said analog amplifier circuit and a ground;

said output matching circuit comprising:

a second series resonance circuit having a third capacitor and a third inductor, connected in series between an output terminal of said transistor and said output terminal of said analog amplifier circuit; and

a second parallel resonance circuit having a fourth capacitor and a fourth inductor, connected in parallel between said output terminal of said analog amplifier circuit and said ground;

wherein said first and second series resonance circuits inductively function with respect to a first frequency while said first and second series resonance circuits capacitively function with respect to a second frequency which is different from said first frequency, so as to perform impedance matching with respect to said first frequency and said second frequency.

15. The analog amplifier circuit according to claim 14, wherein said first and second parallel resonance circuits capacitively function with respect to said first frequency while said first and second parallel resonance circuits inductively function with respect to said second frequency.

16. An analog amplifier circuit having a transistor serving as an amplifier, an input matching circuit thereof and an output matching circuit thereof, an input terminal of said analog amplifier circuit and an output terminal of said analog amplifier circuit,

said input matching circuit comprising:

a first series resonance circuit having a first capacitor and a first inductor, connected in series between an input terminal of said transistor and said input terminal of said analog amplifier circuit; and

a first parallel resonance circuit having a second capacitor and a second inductor, connected in parallel between said input terminal of said analog amplifier circuit and a ground;

said output matching circuit comprising:

- a second series resonance circuit having a third capacitor and a third inductor, connected in series between an output terminal of said transistor and said output terminal of said analog amplifier circuit; and
- a second parallel resonance circuit having a fourth capacitor and a fourth inductor, connected in parallel between said output terminal of said analog amplifier circuit and said ground;

wherein said first and second series resonance circuits inductively function with respect to both of a first frequency and a second frequency which is different from said first frequency, and said first and second parallel resonance circuits inductively function with respect to said first frequency while said first and second parallel resonance circuits capacitively function with respect to said second frequency.

17. An analog amplifier circuit having a transistor serving as an amplifier, an input matching circuit thereof and an output matching circuit thereof, an input terminal of said analog amplifier circuit and an output terminal of said analog amplifier circuit,

said input matching circuit comprising:

- a first series resonance circuit having a first capacitor and a first inductor, connected in series between an input terminal of said transistor and said input terminal of said analog amplifier circuit; and
- a first parallel resonance circuit having a second capacitor and a second inductor, connected in parallel between said input terminal of said analog amplifier circuit and a ground;

said output matching circuit comprising:

- a second series resonance circuit having a third capacitor and a third inductor, connected in series between an output terminal of said transistor and said output terminal of said analog amplifier circuit; and
- a second parallel resonance circuit having a fourth capacitor and a fourth inductor, connected in parallel between said output terminal of said analog amplifier circuit and said ground;

wherein said first and second series resonance circuits capacitively function with respect to both of a first frequency and a second frequency which is different from said first frequency, and said first and second parallel resonance circuits inductively function with respect to said first frequency while said first and second parallel resonance circuits capacitively function with respect to said second frequency.

18. An analog amplifier circuit having a transistor serving as an amplifier, an input matching circuit thereof and an output matching circuit thereof, an input terminal of said analog amplifier circuit and an output terminal of said analog amplifier circuit,

said input matching circuit comprising:

- a first parallel resonance circuit having a first capacitor and a first inductor, connected in parallel between an input terminal of said transistor and said input terminal of said analog amplifier circuit; and

- a first series resonance circuit having a second capacitor and a second inductor, connected in series between said input terminal of said analog amplifier circuit and a ground;

said output matching circuit comprising:

- a second parallel resonance circuit having a third capacitor and a third inductor, connected in parallel between an output terminal of said transistor and said output terminal of said analog amplifier circuit; and
- a second series resonance circuit having a fourth capacitor and a fourth inductor, connected in series between said output terminal of said analog amplifier circuit and said ground;

wherein said first and second parallel resonance circuits capacitively function with respect to a first frequency while said first and second parallel resonance circuits inductively function with respect to a second frequency which is different from said first frequency, so as to perform impedance matching with respect to said first frequency and said second frequency.

19. The analog amplifier circuit according to claim 18, wherein said first and second series resonance circuits inductively function with respect to said first frequency while said first and second series resonance circuits capacitively function with respect to said second frequency.

20. An analog amplifier circuit having a transistor serving as an amplifier, an input matching circuit thereof and an output matching circuit thereof, an input terminal of said analog amplifier circuit and an output terminal of said analog amplifier circuit,

said input matching circuit comprising:

- a first parallel resonance circuit having a first capacitor and a first inductor, connected in parallel between an input terminal of said transistor and said input terminal of said analog amplifier circuit; and
- a first series resonance circuit having a second capacitor and a second inductor, connected in series between said input terminal of said analog amplifier circuit and a ground;

said output matching circuit comprising:

- a second parallel resonance circuit having a third capacitor and a third inductor, connected in parallel between an output terminal of said transistor and said output terminal of said analog amplifier circuit; and
- a second series resonance circuit having a fourth capacitor and a fourth inductor, connected in series between said output terminal of said analog amplifier circuit and said ground;

wherein said first and second parallel resonance circuits inductively function with respect to both of a first frequency and a second frequency which is different from said first frequency, and said first and second series resonance circuits inductively function with respect to said first frequency while said first and second series resonance circuits capacitively function with respect to said second frequency.

21. An analog amplifier circuit having a transistor serving as an amplifier, an input matching circuit thereof and an

output matching circuit thereof, an input terminal of said analog amplifier circuit and an output terminal of said analog amplifier circuit,

said input matching circuit comprising:

- a first parallel resonance circuit having a first capacitor and a first inductor, connected in parallel between an input terminal of said transistor and said input terminal of said analog amplifier circuit; and
- a first series resonance circuit having a second capacitor and a second inductor, connected in series between said input terminal of said analog amplifier circuit and a ground;

said output matching circuit comprising:

- a second parallel resonance circuit having a third capacitor and a third inductor, connected in parallel between an output terminal of said transistor and said output terminal of said analog amplifier circuit; and
- a second series resonance circuit having a fourth capacitor and a fourth inductor, connected in series between said output terminal of said analog amplifier circuit and said ground;

wherein said first and second parallel resonance circuits capacitively function with respect to both of a first frequency and a second frequency which is different from said first frequency, and said first and second series resonance circuits inductively function with respect to said first frequency while said first and second series resonance circuits capacitively function with respect to said second frequency.

22. An analog amplifier circuit having a transistor serving as an amplifier, an input matching circuit thereof and an output matching circuit thereof, an input terminal of said analog amplifier circuit and an output terminal of said analog amplifier circuit,

said input matching circuit comprising:

- a first parallel resonance circuit having a first capacitor and a first inductor, connected in parallel between an input terminal of said transistor and a ground; and
- a first series resonance circuit having a second capacitor and a second inductor, connected in series between said input terminal of said transistor and said input terminal of said analog amplifier circuit;

said output matching circuit comprising:

- a second parallel resonance circuit having a third capacitor and a third inductor, connected in parallel between an output terminal of said transistor and said ground; and
- a second series resonance circuit having a fourth capacitor and a fourth inductor, connected in series between said output terminal of said transistor and said output terminal of said analog amplifier circuit;

wherein said first and second parallel resonance circuits inductively function with respect to a first frequency while said first and second parallel resonance circuits capacitively function with respect to a second frequency which is different from said first frequency,

so as to perform impedance matching with respect to said first frequency and said second frequency.

23. The analog amplifier circuit according to claim 22, wherein said first and second series resonance circuits capacitively function with respect to said first frequency while said first and second series resonance circuits inductively function with respect to said second frequency.

24. An analog amplifier circuit having a transistor serving as an amplifier, an input matching circuit thereof and an output matching circuit thereof, an input terminal of said analog amplifier circuit and an output terminal of said analog amplifier circuit,

said input matching circuit comprising:

- a first parallel resonance circuit having a first capacitor and a first inductor, connected in parallel between an input terminal of said transistor and a ground; and
- a first series resonance circuit having a second capacitor and a second inductor, connected in series between said input terminal of said transistor and said input terminal of said analog amplifier circuit;

said output matching circuit comprising:

- a second parallel resonance circuit having a third capacitor and a third inductor, connected in parallel between an output terminal of said transistor and said ground; and
- a second series resonance circuit having a fourth capacitor and a fourth inductor, connected in series between said output terminal of said transistor and said output terminal of said analog amplifier circuit;

wherein said first and second parallel resonance circuits inductively function with respect to both of a first frequency and a second frequency which is different from said first frequency, and said first and second series resonance circuits capacitively function with respect to said first frequency while said first and second series resonance circuits inductively function with respect to said second frequency.

25. An analog amplifier circuit having a transistor serving as an amplifier, an input matching circuit thereof and an output matching circuit thereof, an input terminal of said analog amplifier circuit and an output terminal of said analog amplifier circuit,

said input matching circuit comprising:

- a first parallel resonance circuit having a first capacitor and a first inductor, connected in parallel between an input terminal of said transistor and a ground; and
- a first series resonance circuit having a second capacitor and a second inductor, connected in series between said input terminal of said transistor and said input terminal of said analog amplifier circuit;

said output matching circuit comprising:

- a second parallel resonance circuit having a third capacitor and a third inductor, connected in parallel between an output terminal of said transistor and said ground; and
- a second series resonance circuit having a fourth capacitor and a fourth inductor, connected in series

between said output terminal of said transistor and said output terminal of said analog amplifier circuit;

wherein said first and second series resonance circuits capacitively function with respect to both of a first frequency and a second frequency which is different from said first frequency, and said first and second series resonance circuits capacitively function with respect to said first frequency while said first and second series resonance circuits inductively function with respect to said second frequency.

26. An analog amplifier circuit having a transistor serving as an amplifier, an input matching circuit thereof and an output matching circuit thereof, an input terminal of said analog amplifier circuit and an output terminal of said analog amplifier circuit,

said input matching circuit comprising:

a first series resonance circuit having a first capacitor and a first inductor, connected in series between said input terminal of said transistor and a ground; and

a first parallel resonance circuit having a second capacitor and a second inductor, connected in parallel between an input terminal of said transistor and said input terminal of said analog amplifier circuit;

said output matching circuit comprising:

a second series resonance circuit having a third capacitor and a third inductor, connected in series between said output terminal of said transistor and said ground; and

a second parallel resonance circuit having a fourth capacitor and a fourth inductor, connected in parallel between an output terminal of said transistor and said output terminal of said analog amplifier circuit;

wherein said first and second series resonance circuits capacitively function with respect to a first frequency while said first and second series resonance circuits inductively function with respect to a second frequency which is different from said first frequency, so as to perform impedance matching with respect to said first frequency and said second frequency.

27. The analog amplifier circuit according to claim 26, wherein said first and second parallel resonance circuits inductively function with respect to said first frequency while said first and second parallel resonance circuits capacitively function with respect to said second frequency.

28. An analog amplifier circuit having a transistor serving as an amplifier, an input matching circuit thereof and an output matching circuit thereof, an input terminal of said analog amplifier circuit and an output terminal of said analog amplifier circuit,

said input matching circuit comprising:

a first series resonance circuit having a first capacitor and a first inductor, connected in series between said input terminal of said transistor and a ground; and

a first parallel resonance circuit having a second capacitor and a second inductor, connected in parallel between an input terminal of said transistor and said input terminal of said analog amplifier circuit;

said output matching circuit comprising:

a second series resonance circuit having a third capacitor and a third inductor, connected in series between said output terminal of said transistor and said ground; and

a second parallel resonance circuit having a fourth capacitor and a fourth inductor, connected in parallel between an output terminal of said transistor and said output terminal of said analog amplifier circuit;

wherein said first and second series resonance circuits inductively function with respect to both of a first frequency and a second frequency which is different from said first frequency, and said first and second parallel resonance circuits capacitively function with respect to said first frequency while said first and second parallel resonance circuits inductively function with respect to said second frequency.

29. An analog amplifier circuit having a transistor serving as an amplifier, an input matching circuit thereof and an output matching circuit thereof, an input terminal of said analog amplifier circuit and an output terminal of said analog amplifier circuit,

said input matching circuit comprising:

a first series resonance circuit having a first capacitor and a first inductor, connected in series between said input terminal of said transistor and a ground; and

a first parallel resonance circuit having a second capacitor and a second inductor, connected in parallel between an input terminal of said transistor and said input terminal of said analog amplifier circuit;

said output matching circuit comprising:

a second series resonance circuit having a third capacitor and a third inductor, connected in series between said output terminal of said transistor and said ground; and

a second parallel resonance circuit having a fourth capacitor and a fourth inductor, connected in parallel between an output terminal of said transistor and said output terminal of said analog amplifier circuit;

wherein said first and second series resonance circuits capacitively function with respect to both of a first frequency and a second frequency which is different from said first frequency, and said first and second parallel resonance circuits capacitively function with respect to said first frequency while said first and second parallel resonance circuits inductively function with respect to said second frequency.

30. An analog amplifier circuit having a transistor serving as an amplifier, an input matching circuit thereof and an output matching circuit thereof for performing impedance matching with respect to a first frequency and a second frequency which is different from said first frequency, an input terminal of said analog amplifier circuit and an output terminal of said analog amplifier circuit,

said input matching circuit comprising:

a first phase rotating element, one end of which being connected to said input terminal of said transistor, for rotating a phase of an input signal; and

a first resonance circuit, one end of which being connected to said input terminal of said analog amplifier circuit and the other end thereof being connected to the other end of said first phase rotating element;

said output matching circuit comprising:

a second phase rotating element, one end of which being connected to said output terminal of said transistor, for rotating a phase of an output signal of said transistor; and

a second resonance circuit, one end of which being connected to said output terminal of said analog amplifier circuit and the other end thereof being connected to the other end of said second phase rotating element.

31. An analog amplifier circuit having a transistor serving as an amplifier, an input matching circuit thereof and an output matching circuit thereof for performing impedance matching with respect to a first frequency and a second frequency which is different from said first frequency, an input terminal of said analog amplifier circuit and an output terminal of said analog amplifier circuit,

said input matching circuit comprising:

a first phase rotating element, one end of which being connected to said input terminal of said transistor, the other end thereof being connected to said input terminal of said analog amplifier circuit, for rotating a phase of an input signal; and

a first resonance circuit, one end of which being connected to said input terminal of said analog amplifier circuit and the other end thereof being connected to a ground;

said output matching circuit comprising:

a second phase rotating element, one end of which being connected to said output terminal of said transistor, the other end thereof being connected to said output terminal of said analog amplifier circuit, for rotating a phase of an output signal of said transistor; and

a second resonance circuit, one end of which being connected to said output terminal of said analog amplifier circuit and the other end thereof being connected to said ground.

* * * * *