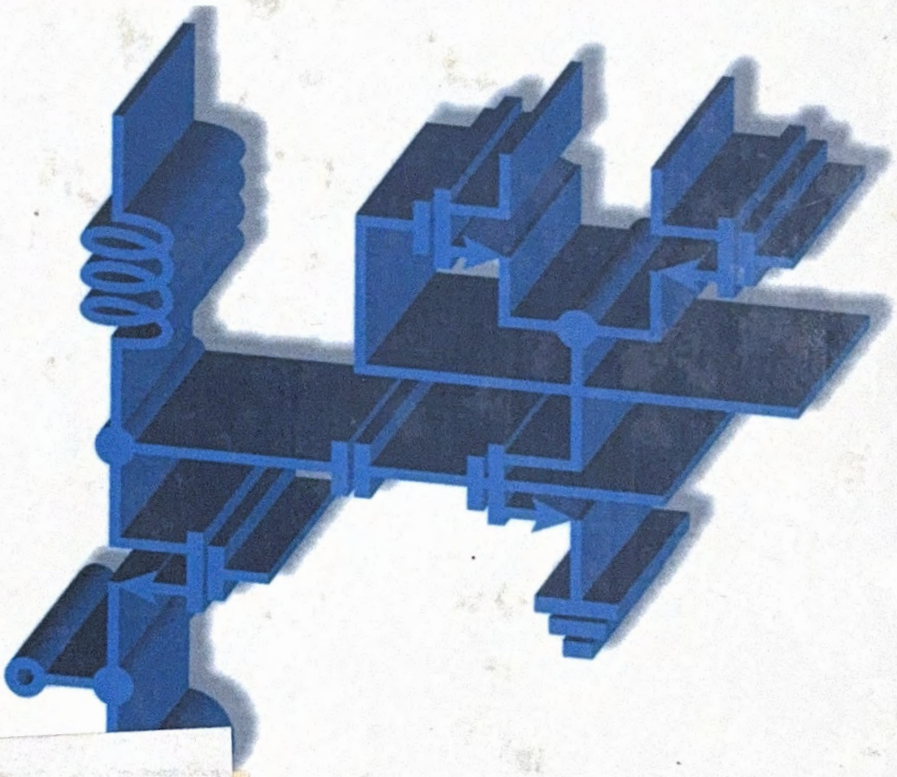
RF MICROELECTRONICS



BEHZAD RAZAVI

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RF MICROELECTRONICS

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To the memory
of my parents

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Preface

The annual worldwide sales of cellular phones has exceeded $2.5B. With 4.5 million customers, home satellite networks comprise a $2.5B industry. The global positioning system is expected to become a $5B market by the year 2000. In Europe, the sales of equipment and services for mobile communications will reach $30B by 1998. The statistics are overwhelming.

The radio frequency (RF) and wireless market has suddenly expanded to unimaginable dimensions. Devices such as pagers, cellular and cordless phones, cable modems, and RF identification tags are rapidly penetrating all aspects of our lives, evolving from luxury items to indispensable tools. Semiconductor and system companies, small and large, analog and digital, have seen the statistics and are striving to capture their own market share by introducing various RF products.

RF design is unique in that it draws upon many disciplines unrelated to integrated circuits (ICs). The RF knowledge base has grown for almost a century, creating a seemingly endless body of literature for the novice.

This book deals with the analysis and design of RF integrated circuits and systems. Providing a systematic treatment of RF electronics in a tutorial language, the book begins with the necessary background knowledge from microwave and communication theory and leads the reader to the design of RF transceivers and circuits. The text emphasizes both architecture and circuit level issues with respect to monolithic implementation in VLSI technologies. The primary focus is on bipolar and CMOS design, but most of the concepts can be applied to other technologies as well. The reader is assumed to have a basic understanding of analog IC design and the theory of signals and systems.

The book consists of nine chapters. Chapter 1 gives a general introduction, posing questions and providing motivation for subsequent chapters. Chapter 2 describes basic concepts in RF and microwave design, emphasizing the effects of nonlinearity and noise.

Chapters 3 and 4 take the reader to the communication system level, giving an overview of modulation, detection, multiple access techniques, and wireless standards. While initially appearing to be unnecessary, this material is in fact essential to the concurrent design of RF circuits and systems.

Chapter 5 deals with transceiver architectures, presenting various receiver and transmitter topologies along with their merits and drawbacks. This chapter

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also includes a number of case studies that exemplify the approaches taken in actual RF products.

Chapters 6 through 9 address the design of RF building blocks: low-noise amplifiers and mixers, oscillators, frequency synthesizers, and power amplifiers, with particular attention to minimizing the number of off-chip components. An important goal of these chapters is to demonstrate how the system requirements define the parameters of the circuits and how the performance of each circuit impacts that of the overall transceiver.

I have taught approximately 80% of the material in this book in a 4-unit graduate course at UCLA. Chapters 3, 4, 8, and 9 had to be shortened in a ten-week quarter, but in a semester system they can be covered more thoroughly.

Much of my RF design knowledge comes from interactions with colleagues. Helen Kim, Ting-Ping Liu, and Dan Avidor of Bell Laboratories, and David Su and Andrew Gzegorek of Hewlett-Packard Laboratories have contributed to the material in this book in many ways. The text was also reviewed by a number of experts: Stefan Heinen (Siemens), Bart Jansen (Hewlett-Packard), Ting-Ping Liu (Bell Labs), John Long (University of Toronto), Tadao Nakagawa (NTT), Gitty Nasserbakht (Texas Instruments), Ted Rappaport (Virginia Tech), Tirdad Sowlati (Gennum), Trudy Stetzler (Bell Labs), David Su (Hewlett-Packard), and Rick Wesel (UCLA). In addition, a number of UCLA students, including Farbod Behbahani, Hooman Darabi, John Leete, and Jacob Rael, "test drove" various chapters and provided useful feedback. I am indebted to all of the above for their kind assistance.

I would also like to thank the staff at Prentice Hall, particularly Russ Hall, Maureen Diana, and Kerry Reardon for their support.

Behzad Razavi
July 1997

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1

INTRODUCTION TO RF AND WIRELESS TECHNOLOGY

"This phone uses GFSK modulation in DECT-TDMA/TDD with zero-IF I/Q detection," said the engineer. "How can we modify it to work with DCS1800 as well?" asked the manager. "We would need to add a duplexer, at least one more LO with SSB mixing, and probably two SAW filters," replied the engineer . . .

Telephones have gotten much more complicated than they used to be. So have RF circuits. The nonspecialist who uses a cellular phone (cellphone) to call home probably does not know that hundreds of scientists and engineers have worked for almost a century to make wireless technology affordable. Nor does he know that there is more computing power in the phone than in some of the early personal computers.

Wireless technology came to existence when, in 1901, Guglielmo Marconi successfully transmitted radio signals across the Atlantic Ocean. The consequences and prospects of this demonstration were simply overwhelming; the possibility of replacing telegraph and telephone communications with wave transmission through the "ether" portrayed an exciting future. However, while two-way wireless communication did materialize in military applications, wireless transmission in daily life remained limited to one-way radio and television broadcasting by large, expensive stations. Ordinary two-way phone conversations would still go over wires for many decades.

The invention of the transistor, the development of Shannon's information theory, and the conception of the cellular system—all at Bell Laboratories—paved the way for affordable mobile communications, as originally implemented in car phones and eventually realized in portable cellular phones.

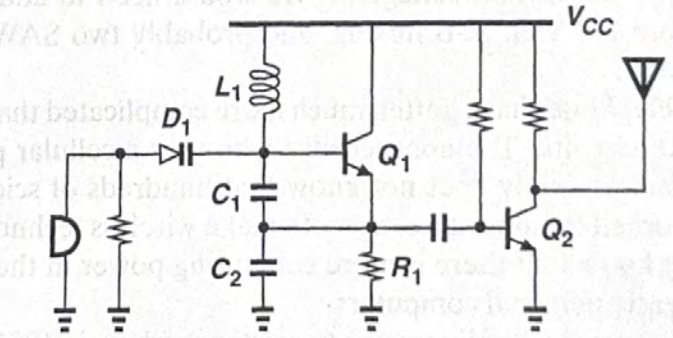
But why the sudden surge in wireless electronics? Market surveys show that in the United States more than 28,000 people join the cellular phone system *every day*, motivating competitive manufacturers to provide phone sets with increasingly higher performance and lower cost. In fact, the present goal

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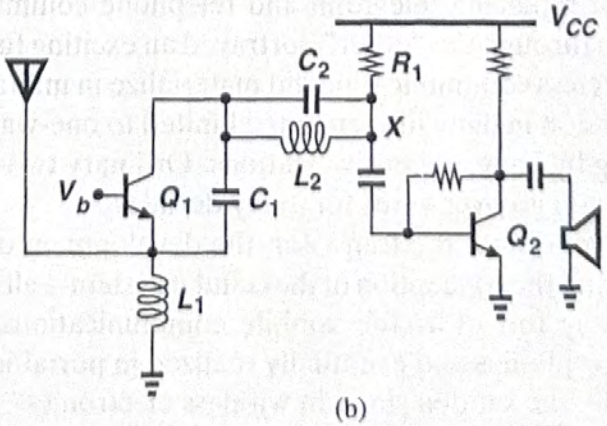
is to reduce both the power consumption and price of cellphones by 30% every year—although it is not clear for how long this rate can be sustained. A more glorious prospect, however, lies in the power of two-way wireless communication when it is introduced in other facets of our lives: home phones, computers, facsimile, and television. While an immediate objective of the wireless industry is to combine cordless and cellular phones so as to allow seamless communications virtually everywhere, the long-term plan is to produce an "omnipotent" wireless terminal that can handle voice, data, and video as well as provide computing power. Other luxury items such as the global positioning system (GPS) are also likely to become available through this terminal sometime in the future. Personal communication services (PCS) are almost here.

1.1 COMPLEXITY COMPARISON

To gain an early perspective on modern RF design, first consider the system depicted in Fig. 1.1, a simple frequency modulation (FM) transceiver. In Fig. 1.1(a), Q_1 operates as both an oscillator and a frequency modulator; that



(a)



(b)

Figure 1.1 (a) FM transmitter, (b) FM receiver.

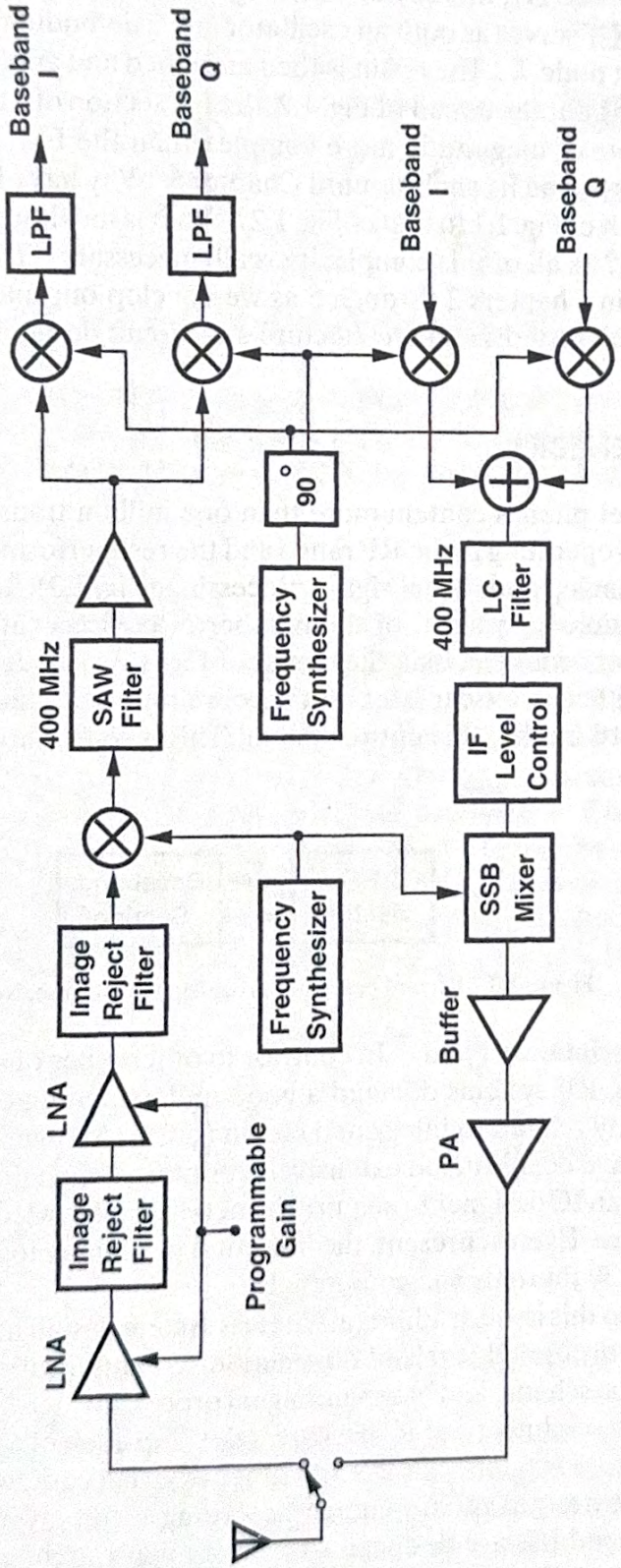


Figure 1.2 RF section of a cellphone [1]

is, the audio signal produced by the microphone varies the bias voltage across the varactor diode D_1, thereby modulating the frequency of oscillation. In the receive path, Q_1 serves as both an oscillator and a demodulator, generating the audio signal at node X. The result is then amplified and applied to the speaker.

Now consider the circuit of Fig. 1.2, the RF section of a cellphone [1]. This circuit is orders of magnitude more complex than the FM circuits of Fig. 1.1, and we will postpone its analysis until Chapter 5. Why have RF designers gone from the circuit of Fig. 1.1 to that of Fig. 1.2? What is the thought process behind this evolution? Is all of this complexity really necessary? These questions will be answered in Chapters 2 through 5 as we develop our understanding of RF communication systems and architecture and circuit design issues.

1.2 DESIGN BOTTLENECK

Today's pocket phones contain more than one million transistors, with only a small fraction operating in the RF range and the rest performing low-frequency "baseband" analog and digital signal processing (Fig. 1.3). In other words, the baseband section is, in terms of the number of devices, yet several orders of magnitude more complex than the circuit of Fig. 1.2. The definition of RF and baseband will become clear later, but here we note that the RF section is still the design bottleneck of the entire system. This is so for three reasons.

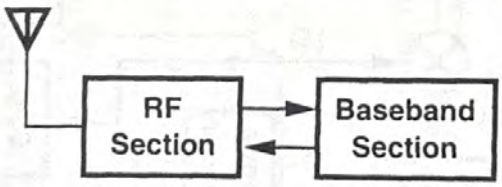


Figure 1.3 RF and baseband processing in a transceiver.

Multidisciplinary Field In contrast to other types of analog and mixed-signal circuits, RF systems demand a good understanding of many areas that are not directly related to integrated circuits (ICs). Shown in Fig. 1.4, most of these areas have been studied extensively for more than half a century, making it difficult for an IC designer to acquire the necessary knowledge in a reasonable amount of time. Even at present, the literature pertaining to RF design appears in more than 30 journals and conferences.

Owing to this issue, traditional wireless system design has been carried out at somewhat disjointed levels of abstraction: communication theorists create the modulation scheme and baseband signal processing; RF system experts plan the transceiver architecture; IC designers develop each of the building blocks; and manufacturers "glue" the ICs and other external components together. In fact, architectures are often planned according to the available off-the-shelf components, and ICs are designed to serve as many architectures as possible, leading to a great deal of redundancy at both system and circuit levels.

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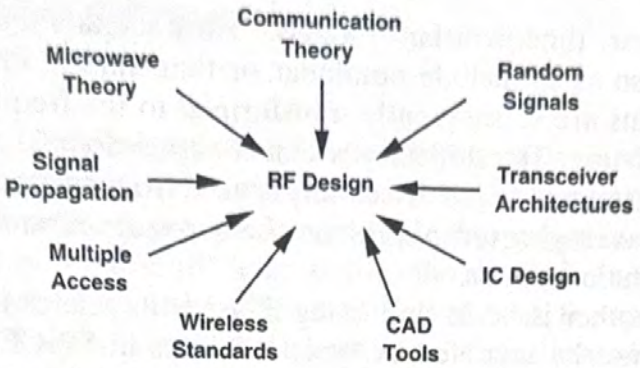


Figure 1.4 Disciplines required in RF design.

As the industry moves toward higher integration and lower cost, RF and wireless design demands increasingly more "concurrent engineering," thereby requiring IC designers to have sufficient knowledge of all the disciplines shown in Fig. 1.4.

RF Design Hexagon RF circuits must process analog signals with a wide dynamic range at high frequencies. It is interesting to note that the signals must be treated as analog even if the modulation is digital or the amplitude carries no information. (This will be clarified in later chapters.) The trade-offs involved in the design of such circuits can be summarized in the "RF design hexagon" shown in Fig. 1.5, where almost any two of the six parameters trade with each other to some extent. We will see these trade-offs in Chapters 6 to 9, but our observation here is that, while digital circuits directly benefit from advances in IC technologies, RF circuits do not as much. This issue is exacerbated by the fact that RF circuits often require external components—for example, inductors—that are difficult to bring onto the chip even in modern IC processes.

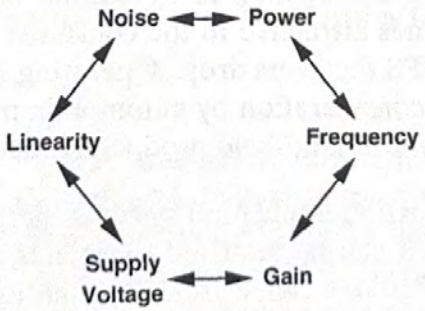


Figure 1.5 RF design hexagon.

Design Tools Computer-aided analysis and synthesis tools for RF ICs are still in their infancy, forcing the designer to rely on experience, intuition, or inefficient simulation techniques to predict the performance. For example, nonlinearity, time variance, and noise in RF circuits usually require studying the spectrum of signals, but the standard ac analysis available in SPICE uses

only linear, time-invariant models. Thus, circuits are simulated in the time domain so as to include nonlinear or time-variant effects, and the resulting waveforms are subsequently transformed to the frequency domain to obtain the spectrum. The difficulty is that the time-domain simulation must be run for a long period to resolve closely spaced frequency components. In addition, spectral averaging techniques may be necessary if random noise is used in the time-domain analysis.

Another issue in simulating RF circuits relates to external components that cannot be modeled by typical devices in SPICE. For example, surface acoustic wave (SAW) filters, used in both the receive and the transmit paths, exhibit input and output impedances that can be characterized only by scattering (S) parameters—essentially a table of numbers. Modeling such circuits with RLC networks provides a first-order approximation, but it may not predict effects such as instability and impedance mismatch.

1.3 APPLICATIONS

In addition to familiar wireless products such as pagers and cellular phones, RF technology has created many other markets that display a great potential for rapid growth, each presenting its own set of challenges to RF designers.

WLANs Communication among people or pieces of equipment in a crowded area can be realized through a wireless local area network (WLAN). Using frequency bands around 900 MHz and 2.4 GHz, WLAN transceivers can provide mobile connectivity in offices, hospitals, factories, etc., obviating the need for cumbersome wired networks. Portability and reconfigurability are prominent features of WLANs.

GPS The use of GPS to determine one's location as well as obtain directions becomes attractive to the consumer market as the cost and power dissipation of GPS receivers drop. Operating in the 1.5-GHz range, such systems are under consideration by automobile manufacturers, but they may be available as low-cost hand-held products sometime in the near future.

RF IDs RF identification systems, simply called "RF IDs," are small, low-cost tags that can be attached to objects or persons so as to track their position. Applications range from luggage in airports to troops in military operations. Low power consumption is especially critical here as the tag's lifetime may be determined by that of a single small battery. RF ID products in the 900-MHz and 2.4-GHz range have recently appeared in the market.

Home Satellite Network The programs and services available through satellite television have attracted many consumers to home satellite networks. Operating in the 10-GHz range, these networks require the addition of a dish antenna and a receiver to a television set and directly compete with cable TV.

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1.4 ANALOG AND DIGITAL SYSTEMS

To gain a general, preliminary view of wireless transceivers, first consider the simple "analog" architecture shown in Fig. 1.6. In the transmit path, the signal generated by the microphone modulates a high-frequency carrier, and the result is amplified and "buffered" so as to drive the antenna. In the receive path, the signal is amplified by a low-noise amplifier (LNA), the spectrum is translated to a lower frequency by a "downconverter" (usually a mixer) to facilitate subsequent demodulation, and the demodulated output is amplified to drive the speaker.

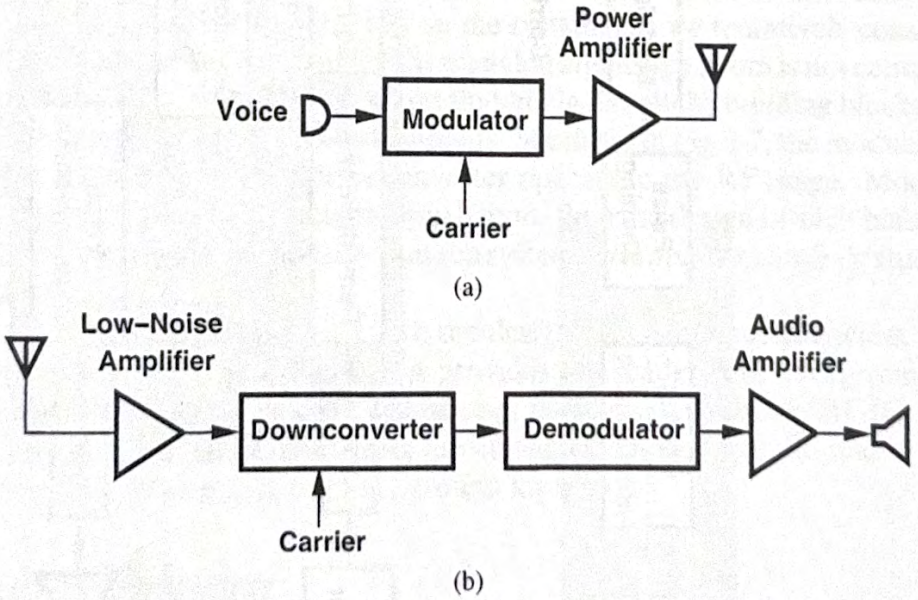


Figure 1.6 Block diagram of a generic analog RF system: (a) transmitter, (b) receiver.

Now, consider the "digital" transceiver shown in Fig. 1.7. Here, the voice signal is first digitized by an analog-to-digital converter (ADC) and compressed to reduce the bit rate and hence the required bandwidth [Fig. 1.7(a)]. Next, the data undergoes "coding" and "interleaving" [2]. These two functions format the data such that the receiver can detect and minimize errors by performing the reverse operations. Since rectangular pulses are usually not optimum for modulation, the data is then "shaped" before it is applied to the modulator and the power amplifier (PA). In the receive path [Fig. 1.7(b)], the signal is amplified, downconverted, and digitized. Subsequently, demodulation, equalization, decoding and deinterleaving, and decompression are performed in the digital domain. The resulting data is then converted to analog form by a digital-to-analog converter (DAC), amplified, and applied to the speaker.

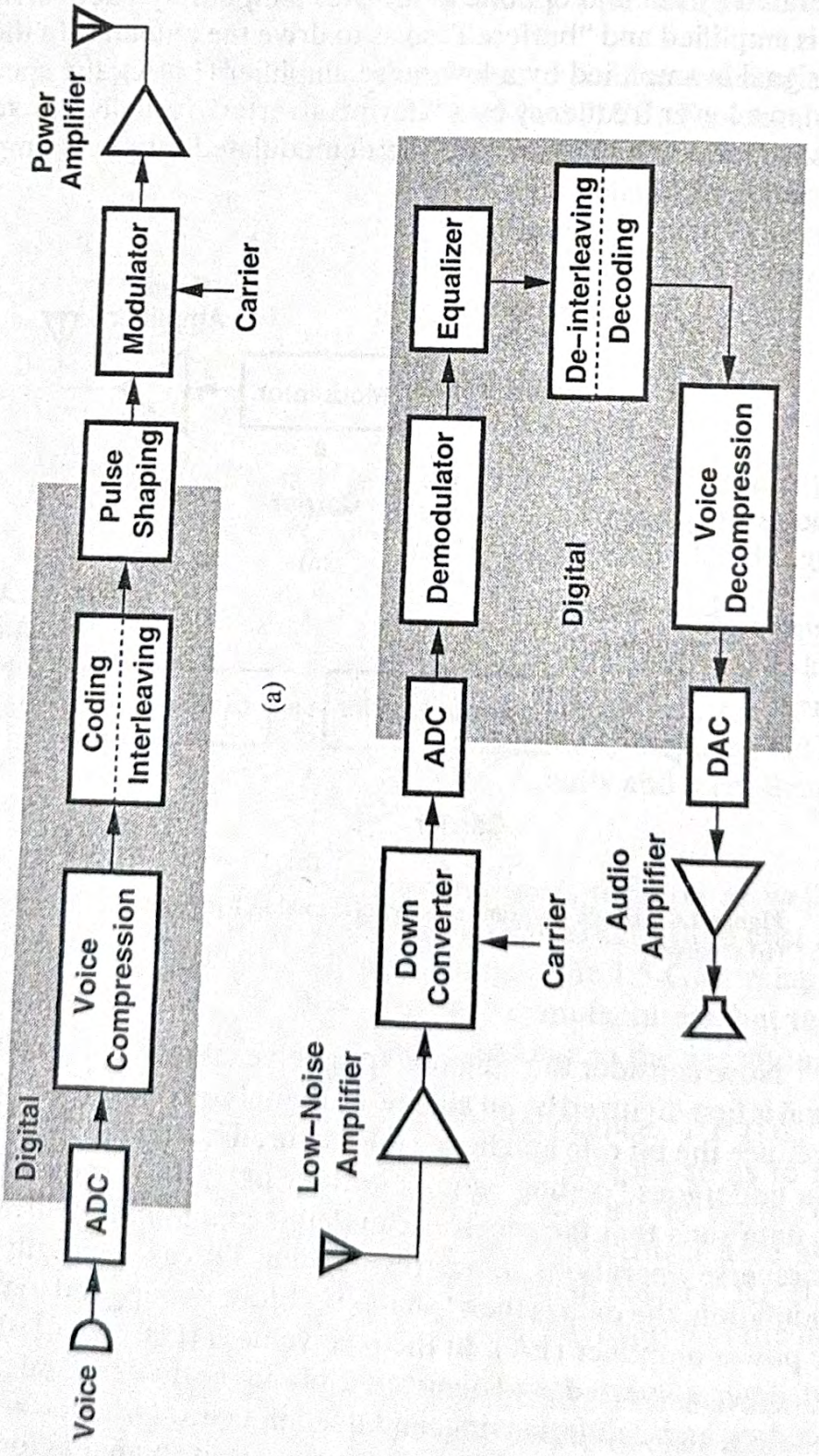


Figure 1.7 Block diagram of a generic digital RF system: (a) transmitter, (b) receiver.

In the simplest case, the performance of these transceivers can be quantified in terms of the maximum distance across which they operate while providing satisfactory reception. This is determined by both the power delivered to the antenna and the sensitivity of the receiver, particularly the noise of the LNA.[1] However, in a realistic environment, many different transceivers operate simultaneously, often in close proximity, thereby interfering with each other. Furthermore, the communication medium is quite complex: reflections from buildings and other obstacles can result in destructive interference at a given point, suppressing the received signal strength to undetectable levels. In such an environment, signal processing in the digital transceiver achieves a higher performance than that of the analog system.

Looking at the two transceivers of Figs. 1.6 and 1.7, the reader may wonder which parts are related to "RF electronics." As we will see in other chapters, the exact definition of RF depends on the system, but we tentatively consider the signal to be in the RF domain if it is analog and its spectrum is not centered around zero frequency. This indicates that in Fig. 1.6 all the building blocks except for the audio amplifier are RF circuits. Similarly, in Fig. 1.7, the modulator, the PA, the LNA, and the downconverter operate in the RF range. Modern RF electronics, however, includes much more than the design of such building blocks. For example, the trade-offs at the system level must be carefully studied in each case [3, 4].

This book primarily deals with the design of RF integrated circuits, but, following the premise of Fig. 1.4, it provides the reader with background in other related areas as well. As will be seen throughout the book, RF ICs, RF architectures, and wireless systems are strongly coupled, and the reader will frequently need to utilize this background knowledge.

1.5 CHOICE OF TECHNOLOGY

The viable IC technology for RF circuits continues to change. Performance, cost, and time to market are three critical factors influencing the choice of technologies in the competitive RF industry. In addition, issues such as level of integration, form factor, and prior (successful) experience play an important role in the decisions made by the designers.

At present, GaAs and silicon bipolar and BiCMOS technologies constitute the major section of the RF market. Usually viewed as a low-yield, high-power, high-cost option, GaAs field-effect and heterojunction devices nonetheless have maintained a strong presence in RF products [5], especially in power amplifiers and front-end switches.

While GaAs processes offer useful features such as higher (breakdown voltage)(cutoff frequency) product, semi-insulating substrate, and high-quality inductors and capacitors, silicon devices in a VLSI technology can potentially

[1] The type of modulation is also an important factor, but we ignore it for the moment.

provide both higher levels of integration and lower overall cost, as demonstrated in complex circuits such as frequency synthesizers. In fact, all building blocks of typical transceivers are available in silicon bipolar technologies from many manufacturers.

The third contender is CMOS technology. Supported by the enormous momentum of the digital market, CMOS devices have achieved high transit frequencies, e.g., tens of gigahertz in the 0.35-μm generation. As we will see in this book, "RF CMOS" has suddenly become the topic of active research. CMOS technology must nevertheless resolve a number of practical issues: substrate coupling of signals that differ in amplitude by 100 dB, parameter variation with temperature and process, and device modeling for RF operation.

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6

LOW-NOISE AMPLIFIERS AND MIXERS

With wireless standards and transceiver architectures described in Chapters 4 and 5, we move farther down to the circuit level in this and subsequent chapters. Beginning with the first circuits in the receive path, we describe the design of low-noise amplifiers and downconversion mixers, emphasizing techniques suited to integration in VLSI technologies. Following an overview of general issues such as stability and input matching, we study the design of bipolar and CMOS LNAs and introduce a number of circuit topologies from the state of the art. Next, we deal with mixers, defining noise figure and conversion gain and describing implementation in both bipolar and CMOS technologies. Finally, we analyze noise in mixers and in cascaded stages.

6.1 LOW-NOISE AMPLIFIERS

6.1.1 General Considerations

In addition to the RF design hexagon described in Chapter 1, a number of other considerations govern the design of low-noise amplifiers. Table 6.1 lists typically acceptable values for the performance metrics of LNAs used in heterodyne architectures. It is instructive to consider each value and its effect on the overall performance.

Since the LNA is the first gain stage in the receive path, its noise figure directly adds to that of the system. With a duplexer NF of approximately 2 dB, this results in an overall value of 4 dB, if the noise of the stages following the LNA is neglected. Thus, if, for example, an SNR of 8 dB in a bandwidth of 200 kHz is required, the input sensitivity is about -109 dBm (Section 2.4).

To gain a better feeling for a noise figure of 2 dB, suppose, as shown in Fig. 6.1, we represent the input-referred noise of a bipolar transistor by a series resistor, i.e., $NF = 1 + R_{eq}/R_S$ (the device capacitances and other resistances

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TABLE 6.1 Typical LNA characteristics in heterodyne systems.

NF	2 dB
IIP_3	−10 dBm
Gain	15 dB
Input and Output Impedance	50 Ω
Input and Output Return Loss	−15 dB
Reverse Isolation	20 dB
Stability Factor	> 1

are neglected here). Since the input-referred noise voltage per unit bandwidth in given by

$$\overline{V_n^2} = 4kT\left(r_b + \frac{1}{2g_m}\right) \tag{6.1}$$

$$= 4kT\left(r_b + \frac{V_T}{2I_C}\right), \tag{6.2}$$

where I_C is the collector current, we have $R_{eq} = r_b + V_T/(2I_C)$. For $NF =$ 2 dB, R_{eq} must not exceed 29 Ω. Thus, Q_1 must be relatively large and biased at a high current. In practice, the noise contributed by the load resistor and the following stages necessitate a lower value for $r_b + V_T/(2I_C)$.

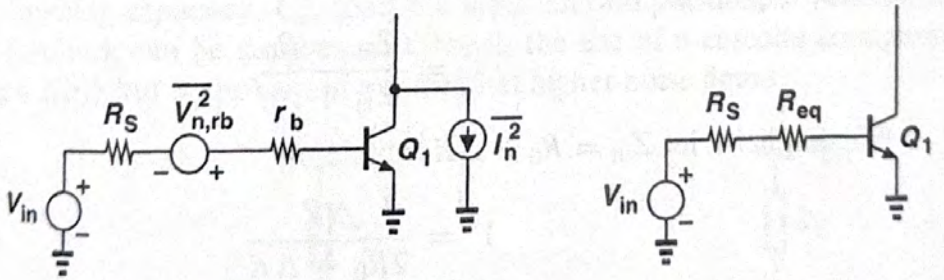


Figure 6.1 Modeling noise of a bipolar transistor with an equivalent resistor.

The value of −10 dBm listed in Table 6.1 for the IP_3 together with $NF =$ 2 dB leads to a certain spurious-free dynamic range. We calculate the maximum magnitude of two adjacent interferers whose intermodulation product remains below the noise floor. From Section 2.4,

$$SFDR = \frac{2}{3}(IP_3 - F) - 12\text{ dB} \tag{6.3}$$

$$= 61\text{ dB}. \tag{6.4}$$

The minimum gain of the LNA in a heterodyne architecture is governed by three parameters: the loss of the image-reject filter and the noise figure and IP_3 of the mixer. For a filter loss of 4 to 5 dB, a mixer noise figure of 10 dB, and

a mixer IP_3 of +5 dBm, a gain of 20 dB in the LNA adequately suppresses the input-referred noise while maintaining a reasonable equivalent IP_3. We will examine the performance of cascaded stages more rigorously at the end of the chapter. Note that the LNA must provide this gain while driving 50 Ω.

In homodyne architectures, the absence of the image-reject filter relaxes the gain and drive requirements of the LNA. However, the issue of flicker noise in the baseband circuits makes it desirable to maximize the gain in the RF range.

The interface between the antenna and the LNA entails an interesting issue that divides analog designers and microwave engineers. Considering the LNA as a *voltage* amplifier, we may expect that the ideal value of its input impedance is infinity. From the noise point of view, we may require a transformation network to precede the LNA so as to obtain minimum NF. From signal power point of view, we may utilize conjugate matching between the antenna and the LNA. While each of these choices has certain merits and drawbacks, the last one is dominant in today's systems, i.e., the LNA is designed to have a 50-Ω resistive input impedance. This is because the bandpass filter following the antenna (e.g., the duplexer) is usually designed to be used in various transceiver systems and must therefore operate with a standard termination impedance, typically 50 Ω. If the source and load impedances seen by the filter deviate from 50 Ω significantly, then the passband and stopband characteristics of the filter may exhibit considerable loss and ripples.

The quality of the input matching is expressed by the input "return loss," defined as $20 \log |\Gamma|$, where Γ is the reflection coefficient with respect to a source impedance R_0:

$$\Gamma = \frac{Z_{in} - R_0}{Z_{in} + R_0}. \tag{6.5}$$

For simplicity, let $Z_{in} = R_0 + \Delta R$, obtaining

$$\Gamma = \frac{\Delta R}{2R_0 + \Delta R}. \tag{6.6}$$

Thus, for a return loss of −15 to −20 dB in a 50-Ω system, $\Delta R \approx 15$ to 9 Ω. In reality, process and temperature variations and residual reactive terms impose a tighter range on ΔR.

In heterodyne architectures, the LNA *output* impedance must also be equal to 50 Ω so as to drive the image-reject filter with minimum loss and ripple. Similar return loss constraints apply here as well.

The reverse isolation of LNAs determines the amount of LO signal that leaks from the mixer to the antenna. The leakage arises from capacitive paths, substrate coupling, and bond wire coupling. In heterodyne receivers with a high first IF, the image-reject filter and the front-end duplexer significantly suppress the leakage because the LO frequency falls in their stopband. In homodyne topologies, on the other hand, the leakage is attenuated primarily by the LNA reverse characteristics.

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In addition to the above parameters, the stability of LNAs is also of concern. In the presence of feedback paths from the output to the input, the circuit may become unstable for certain combinations of source and load impedances. Since the terminal impedances of duplexers and image-reject filters cannot be modeled accurately in SPICE simulations, an LNA design that is nominally stable may oscillate at the extremes of manufacturing variations and perhaps at unexpectedly high or low frequencies.

A constant often used to characterize the stability of circuits is the Stern stability factor, defined as

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|}, \tag{6.7}$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$. If $K > 1$ and $\Delta < 1$, then the circuit is unconditionally stable, i.e., it does not oscillate with any combination of source and load impedances. The difficulty in using K is that the S parameters of the circuit must be calculated (or measured) for a wide frequency range to ensure that K remains greater than unity at all frequencies. With SPICE simulations, for example, some postprocessing is necessary to compute K.

Equation (6.7) suggests that stability improves as S_{12} decreases, i.e., as the reverse isolation of the circuit increases. In traditional RF design, this is accomplished by "neutralizing" the input-output capacitive path, as shown in Fig. 6.2(a). That is, L_1 and C_μ resonate at the frequency of interest. In IC design, however, the parasitic capacitances of the floating inductor and the coupling capacitor, C_1, load the input and output nodes. Alternatively, the feedback can be suppressed through the use of a cascode configuration [Fig. 6.2(b)], but at the cost of a somewhat higher noise figure.

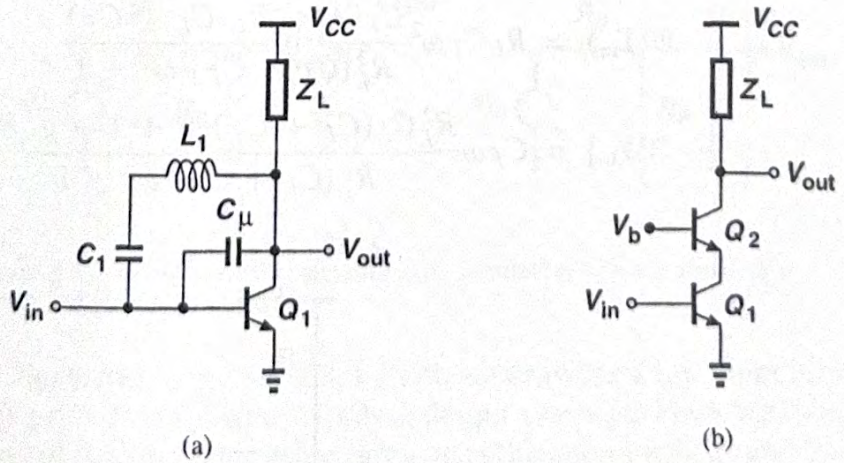


Figure 6.2 Stabilization by (a) neutralization and (b) cascoding.

We should also note that K is a pessimistic measure of stability for it allows arbitrary variation in the source and load impedances seen by the circuit. On the other hand, if the load impedance of an LNA is well defined, e.g., in a homodyne

or image-reject architecture, then stability is achieved by simply ensuring that the real part of the input impedance remains positive at all frequencies. This criterion is justified by the one-port model of oscillators described in Chapter 7.

As other amplifiers, LNAs may become unstable because of ac ground and supply loops resulting from bond wire inductance. For the frequency range of 900 MHz and above, even a few nanohenries of inductance may provide considerable coupling between two stages through the ground node, thereby causing oscillation. For this reason, precautions in the design and layout as well as accurate package modeling are essential.

As a final general note, we should remark that the low noise required of LNAs typically governs the choice of the topologies and parameter values employed in the design. As will be seen below, this often means that *only one transistor*—usually the input device—can be the dominant contributor to NF, thus ruling out configurations such as emitter or source followers and resistive feedback.

6.1.2 Input Matching

In order to illustrate the difficulties in creating an input resistance of 50 Ω, we study a number of circuit configurations.

Consider the common-source stage depicted in Fig. 6.3. We note that at sufficiently high frequencies, C_F shorts the gate and drain terminals of M_1, creating an input resistance roughly equal to $R_L||(1/g_m)$. Thus, the circuit can in principle provide an input resistance equal to 50 Ω at the frequency of interest. More specifically, the real and imaginary parts of the input admittance, excluding C_{GS}, can be written as

$$\Re\{Y_{\text{in}}\} = R_L C_F \omega^2 \frac{C_F + g_m R_L (C_L + C_F)}{R_L^2 (C_L + C_F)^2 \omega^2 + 1} \tag{6.8}$$

$$\Im\{Y_{\text{in}}\} = C_F \omega \frac{R_L^2 C_L (C_L + C_F)\omega^2 + 1 + g_m R_L}{R_L^2 (C_L + C_F)^2 \omega^2 + 1}. \tag{6.9}$$

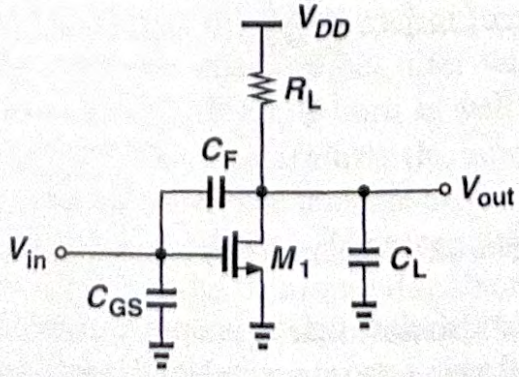


Figure 6.3 Common-source stage.

If $g_m R_L \gg 1$, $C_L \gg C_F$, and $\omega \approx 1/(R_L C_L)$, these expressions reduce to

$$\Re\{Y_{in}\} = \frac{g_m}{2}\frac{C_F}{C_L} \tag{6.10}$$

$$\Im\{Y_{in}\} = C_F\omega\left(1 + \frac{g_m R_L}{2}\right), \tag{6.11}$$

suggesting that proper choice of $2C_L/(g_m C_F)$ can yield a 50-Ω input resistance. The drawback of this topology is the relatively low voltage gain at high frequencies due to the bandwidth limitation at the output node.

In Fig. 6.4(a), a 50-Ω resistor is placed in parallel with the input, and the capacitive part of the input impedance is canceled by an external inductor. The termination resistor, however, generates noise as well. In fact, as shown in Fig. 6.4(b) and proved in Chapter 2, the noise figure of a stage consisting of a parallel resistor R_P with respect to a source resistance R_S is

$$NF = 1 + \frac{R_S}{R_P}. \tag{6.12}$$

For $R_P = R_S$, the noise figure of the LNA exceeds 3 dB. The key point here is that the circuit must exhibit a 50-Ω input resistance without the thermal noise of a 50-Ω resistor.

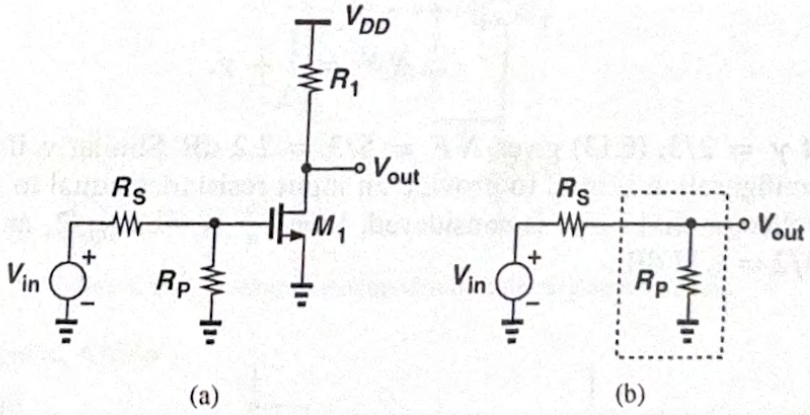


Figure 6.4 (a) Resistive termination, (b) calculation of noise figure of a termination resistor.

In Fig. 6.5(a), negative shunt feedback provides a low input impedance, generating a 50-Ω real part with proper design. Shown in Fig. 6.5(b) is an implementation of this topology, where M_3 senses the output voltage and feeds back a current signal. The difficulties in this case are twofold. First, the feedback signal may contain substantial noise, thus raising the noise figure to unacceptable levels. Second, the total phase shift around the loop may create instability for certain source and load impedances. [Note the similarity between the LNA of Fig. 6.5(b) and a three-stage ring oscillator.]

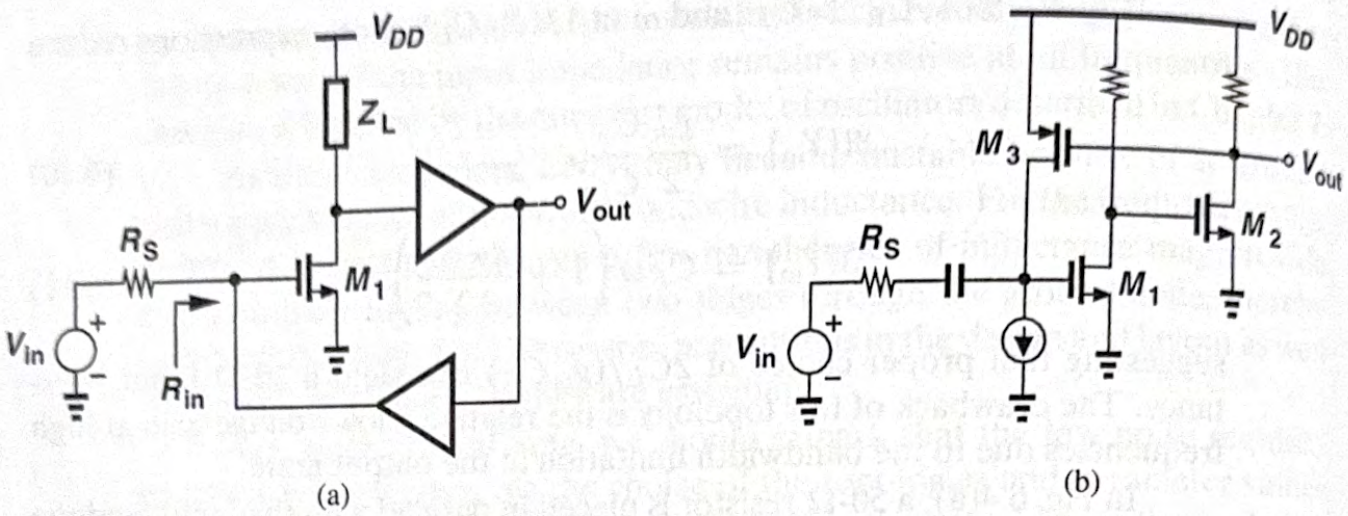


Figure 6.5 (a) Input resistive termination by feedback, (b) simple implementation of (a).

Figure 6.6(a) depicts a common-gate stage designed to exhibit an input resistance of 50 Ω; that is, $1/(g_m + g_{mb}) = 50\ \Omega$. The input capacitance may be nulled by means of an external inductor. The principal drawback of this method is that the transconductance of the input transistor cannot be arbitrarily high, thus imposing a lower bound on the noise figure. Considering only the channel thermal noise of M_1, $I_n^2 = 4kT\gamma g_m$ (where $\gamma = 2/3$ for long-channel devices), and using the equivalent circuits of Figs. 6.6(b) and (c), the reader can easily prove that the noise figure is

$$NF = 1 + \gamma. \tag{6.13}$$

If $\gamma = 2/3$, (6.13) gives $NF = 5/3 = 2.2$ dB. Similarly, if a common-base configuration is used to provide an input resistance equal to R_S and only the collector shot noise is considered, then $I_n^2 = 4kTg_m/2$, and hence $NF = 3/2 = 1.77$ dB.

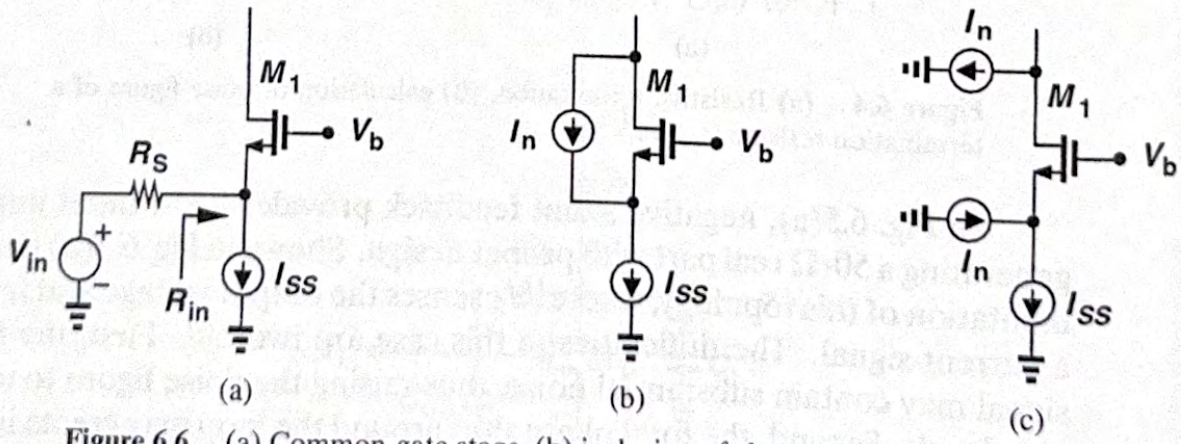


Figure 6.6 (a) Common-gate stage, (b) inclusion of channel noise, (c) equivalent circuit of (b).

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While the above calculations suggest a reasonable noise figure for matched-input common-gate and common-base topologies, in reality other sources of noise degrade the performance substantially. In short-channel MOSFETs, the factor γ may be quite higher than 2/3 [1], and in bipolar transistors, the effect of the base resistance thermal noise may even exceed that of the collector shot noise. Furthermore, in both cases the bias current source and possibly the load generate additional noise.

Another method of creating an input resistance of 50 Ω is illustrated in Fig. 6.7. Neglecting the gate-drain and source-bulk capacitance, we can write

$$Z_{\text{in}} \approx \frac{g_m L_1}{C_{GS}} + L_1 s + \frac{1}{C_{GS} s}. \tag{6.14}$$

Thus, proper choice of g_m, L_1, and C_{GS} yields a 50-Ω real part. In practice, the last two terms may not resonate at the frequency of interest, necessitating the use of off-chip components at the input. At high frequencies, the required value of L_1 becomes comparable with the inductance of the ground bond wire, requiring multiple bonds or accurate modeling of the wire inductance. Also, the reduction of the equivalent transconductance as a result of degeneration may magnify the noise contributed by the devices connected to the drain of M_1.

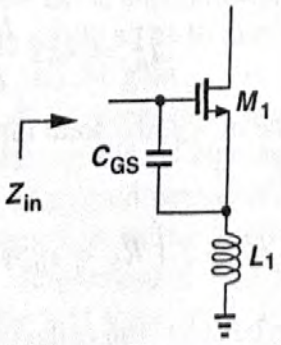


Figure 6.7 Resistive termination by inductive degeneration.

6.1.3 Bipolar LNAs

We first study a simple common-emitter stage to understand its limitations. Consider the circuit shown in Fig. 6.8(a), where Q_2 and I_1 define the bias current of Q_1, R_1 isolates the signal path from the noise of Q_2, and R_2 sustains the same voltage drop as that across R_1 resulting from the finite base current of Q_1. If R_1 is sufficiently greater than R_S, the effect of the bias circuit upon the LNA's performance can be neglected.

From Eq. (6.2), we note that Q_1 must be a large device biased at a relatively high current. Increasing the device size, however, leads to a higher input capacitance (both C_{je} and the Miller multiplication of C_{jc}), in effect attenuating the input signal and "magnifying" the noise of Q_1 and R_c. Fur-

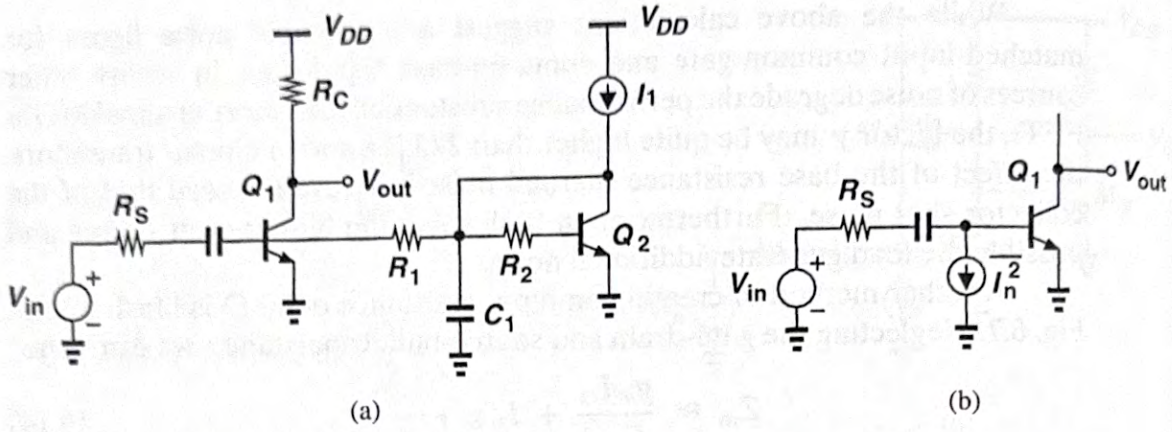


Figure 6.8 (a) Simple bipolar LNA, (b) inclusion of base shot noise.

thermore, larger collector-base and collector-substrate capacitance lowers the voltage gain, and increasing the bias current results in larger base-emitter diffusion capacitance ($\approx g_m \tau_F$) as well as greater base shot noise. For these reasons, the noise figure reaches a minimum for a particular choice of the size and bias current of Q_1.

As the next step in improving the accuracy of (6.2), we include the base shot noise as a current source [Fig. 6.8(b)]:

$$\overline{I_n^2} = 4kT\frac{I_C/\beta}{2V_T}. \tag{6.15}$$

For a source resistance of R_S, the total input-referred noise voltage including that of R_S is given by

$$\overline{V_{\text{tot}}^2} = 4kT\left(R_S + r_b + \frac{1}{2g_m} + \frac{g_m R_S^2}{2\beta}\right), \tag{6.16}$$

where the correlation between the collector shot noise and base shot noise has been neglected. The noise figure is therefore equal to

$$NF = \frac{V_{\text{tot}}^2}{4kTR_S} \tag{6.17}$$

$$= 1 + \frac{r_b}{R_S} + \frac{1}{2g_m R_S} + \frac{g_m R_S}{2\beta}. \tag{6.18}$$

The noise figure reaches a minimum of $NF_{\text{min}} = 1 + \sqrt{(1+2g_m r_b)/\beta}$ for $R_{S,\text{opt}} = \sqrt{\beta(1+2g_m r_b)}/g_m$. This equation does not take into account the effect of parasitic capacitances. However, a reasonable high-frequency approximation is to simply calculate the magnitude of β at the frequency of operation; that is, $|\beta| \approx f_T/f$ [2]. The accurate value of NF must be eventually obtained from simulations.

The relation obtained above for $R_{S,\text{opt}}$ suggests that a matching network placed between the antenna and the LNA can provide minimum noise figure by

transforming the antenna output impedance to $R_{s,\text{opt}}$. As mentioned earlier, however, conjugate matching is more widely used than "noise matching."

It is instructive to calculate the input IP_3 of the CE stage of Fig. 6.8(a). The collector current of Q_1 can be written as

$$I_C \approx I_S \exp \frac{V_{BE0} + V_{\text{in}}}{V_T} \tag{6.19}$$

$$= I_S \exp \frac{V_{BE0}}{V_T} \left[1 + \frac{V_{\text{in}}}{V_T} + \frac{1}{2}\left(\frac{V_{\text{in}}}{V_T}\right)^2 + \frac{1}{6}\left(\frac{V_{\text{in}}}{V_T}\right)^3 + \cdots \right] \tag{6.20}$$

Comparing (6.20) with (2.11), we have $\alpha_1 = (1/V_T) I_S \exp(V_{BE0}/V_T)$ and $\alpha_3 = [1/(6V_T^3)] I_S \exp(V_{BE0}/V_T)$, and hence, from (2.28), $IP_3 = 2\sqrt{2}V_T$. This voltage corresponds to a power level of -12.7 dBm across a 50-Ω resistor. Thus, to achieve an IP_3 greater than -10 dBm, additional linearization is usually necessary.

The small-signal gain of the common-emitter stage depends on both the parasitics of Q_1 and the load impedance. If the LNA is to drive a 50-Ω load while maintaining a reasonable gain, a second stage may be necessary. Thus, the first stage must drive the input capacitance of the second stage and exhibit sufficient gain to minimize the noise contribution of the latter. The two stages are typically designed as one entity so as to minimize the overall noise figure and maximize the input IP_3 and the gain.

With the above study of the limitations of a common-emitter stage, we now consider a number of state-of-the art bipolar LNAs.

Fig. 6.9(a) shows the simplified circuit of a 900-MHz LNA consisting of two common-emitter stages, one with inductive generation and the other with resistive feedback [2]. Implemented with the bond wire that provides the ground connection to the first stage, inductor L_e plays two roles in the circuit: it both allows conjugate matching of the input and linearizes the circuit. Neglecting the effect of C_μ and r_π, we can write the input impedance as

$$Z_{\text{in}} = r_b + \frac{g_m L_e}{C_\pi} + L_e s + \frac{1}{C_\pi s}. \tag{6.21}$$

Thus, with proper choice of g_m, L_e, and C_π, we have $r_b + g_m L_e / C_\pi = 50\ \Omega$, while the last two terms in (6.21) cancel.

The feedback in the second stage serves to both linearize the circuit and lower the output impedance, but at the cost of higher noise. The interface between the two stages in an example of a common problem: the proper choice of gain of the first stage and noise and nonlinearity of the second. We note that the gain of the first stage must be high enough to minimize the noise contributed by the second stage, but not so high that the overall IP_3 is limited by the nonlinearity of Q_2. Thus, the full design requires some iteration to arrive at an acceptable compromise.

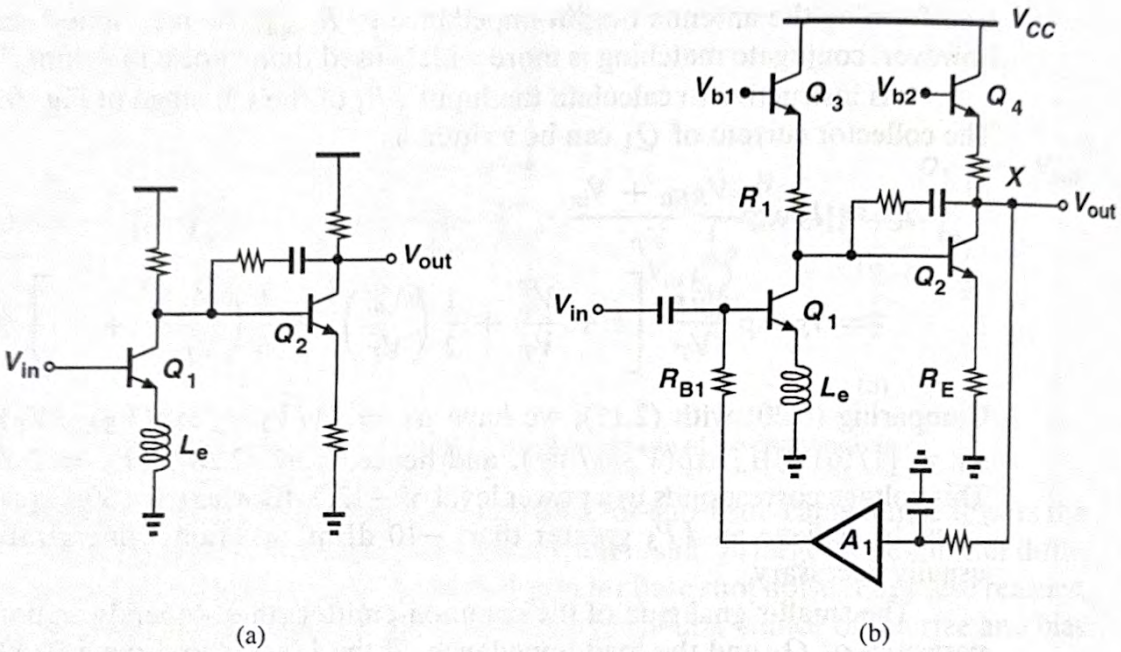


Figure 6.9 (a) Two-stage LNA in [2], (b) biasing of the LNA.

The dc biasing of the LNA shown in Fig. 6.9(a) must ensure constant gain against temperature and supply voltage variations. Fig. 6.9(b) illustrates the biasing network in simplified form [2]. Amplifier A_1 along with resistor R_{B1} provides the base current of Q_1 such that $V_X \approx 1.2$ V. In addition, bandgap techniques are utilized to generate a voltage proportional to absolute temperature, V_{PTAT}. Added to a multiple of V_{BE}, this voltage controls the bases of Q_3 and Q_4 so as to make their small-signal gain independent of temperature and supply voltage. For example, since $V_{b1} = V_{PTAT} + 2V_{BE}$, the collector current of Q_1 can be expressed as $I_{C1} \approx (V_{PTAT} + 2V_{BE} - V_{BE3} - V_{BE2})/R_1 = V_{PTAT}/R_1$, where the voltage drop across R_E is neglected. Thus, the dc gain of the first stage is equal to $A_{v1} = g_{m1}R_1 = I_{C1}R_1/V_T = V_{PTAT}/V_T$. At 900 MHz, on the other hand, the impedance of L_1 is significant, resulting in incomplete cancellation of terms and yielding some temperature dependence.

Fabricated in a 13-GHz BiCMOS technology and operating from a 5-V supply, the circuit of Fig. 6.9 achieves a noise figure of 2.2 dB, an input IP_3 of -10 dBm, and a gain of 16 dB at 900 MHz [2].

Another bipolar LNA designed to drive a 50-Ω load is depicted in Fig. 6.10 [3]. Employing negative feedback through a monolithic transformer to linearize the circuit, the LNA can operate with supply voltages as low as one V_{BE}. Interestingly, the transformer reduces the amplifier gain at both low and high frequencies, helping to stabilize the circuit. The external inductor L_1 and capacitor C_1 provide conjugate matching at the input.

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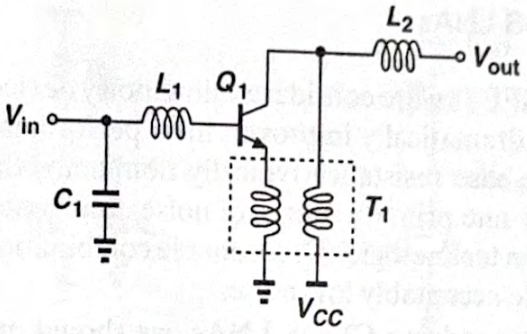


Figure 6.10 Bipolar LNA incorporating transformer feedback.

Drawing 2 mA from a 1.9-V supply, the circuit of Fig. 6.10 achieves a noise figure of 2.8 dB and a gain of 9.6 dB at 1.9 GHz in an 11-GHz BiCMOS technology. The transformer feedback boosts the input IP_3 to -3 dBm.

Another possible topology for bipolar LNAs is a common-base configuration (Fig. 6.11). This circuit offers three advantages over a common-emitter counterpart: simpler input matching, higher linearity, and greater reverse isolation. Neglecting the emitter and base resistance, we can write the input impedance as $(g_m + C_\pi s)^{-1}$, obtaining a 50-Ω resistive component for $I_C \approx 0.5$ mA. The effect of C_π is either negligible or canceled by an external inductor.

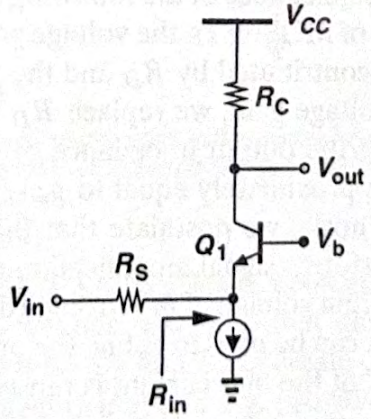


Figure 6.11 Common-base LNA.

In a common-base circuit, the source resistance, R_S, linearizes the input-output characteristic by "softening" the emitter current excursions. This is in contrast to a common-emitter stage where the source resistance experiences only the base current variations. With $R_S = g_m^{-1} (= 50\ \Omega)$, simulations predict an input IP_3 of approximately -6.8 dBm for the circuit of Fig. 6.11. This topology also exhibits a high reverse isolation if the base bias is properly bypassed, proving especially useful in homodyne architectures. As mentioned in Section 6.1.2, the primary drawback of a common-base stage is a relatively high noise figure.

6.1.4 CMOS LNAs

While MOSFETs were considered slow, noisy devices up to about a decade ago, scaling has dramatically improved their performance. Unlike bipolar transistors, whose base resistance typically dominates the noise figure, MOSFETS exhibit only one primary source of noise, that generated in the channel. Thus, in submicron technologies, a reasonable combination of device and bias current may provide acceptably low noise.

Before studying CMOS LNAs, we should mention that the distributed gate resistance of MOS devices also contributes thermal noise. For a total gate resistance R_g, it can be shown that the equivalent lumped model yields a spot noise voltage of $\overline{v_{ng}^2} = 4kTR_g/3$ [4]. Nevertheless, this resistance can be minimized by laying out the transistor as a parallel combination of many narrower devices.

Basic common-source and common-gate LNA configurations have properties and limitations similar to those of common-emitter and common-base circuits. One exception is that, for typical bias currents and dimensions used in RF applications, MOS devices are more linear than bipolar transistors.

To arrive at a CMOS LNA topology, let us consider the common-source stage shown in Fig. 6.12(a), where C_1 represents the parasitic capacitance of M_1 and the input capacitance of the following stage. Owing to the typically low transconductance of MOSFETs, the voltage gain of this circuit is relatively low, making the noise contributed by R_D and the following stage quite significant. To increase the voltage gain, we replace R_D with a current source, as shown in Fig. 6.12(b). If the output impedance of M_2 is sufficiently high, the gain of this circuit is approximately equal to $g_{m1}/(C_1 s)$. Since the current source itself contributes noise, we postulate that the overall input-referred noise is reduced if M_2 performs signal amplification as well [Fig. 6.12(c)] [5]. As the bias current and drain voltage of M_2 strongly depend on the supply voltage, a dc feedback network can be used to define the operating point [Fig. 6.12(d)]. The key idea here is that the bias current is reused to provide a higher equivalent transconductance: $g_{m1} + g_{m2}$. The circuit, however, exhibits a relatively high input resistance.

The circuit of Fig. 6.12(d) is followed by a similar stage so as to drive a 50-Ω load. Note that a common-source stage exhibits a higher drive efficiency than does a source follower because the gain of the former is equal to $g_m R_L$ while that of the latter is $g_m R_L/(1 + g_m R_L)$ [5]. With $g_m \approx 1/R_L$, the common-source stage has a voltage gain of unity, whereas the source follower suffers from attenuation by a factor of 2.

Fabricated in a 0.5-μm CMOS technology and operating from a 2.7-V supply, the 900-MHz LNA of Fig. 6.12(d) exhibits a minimum noise figure of 1.9 dB (with an external matching network), a gain of 15.6 dB, and an input IP_3 of -3.2 dBm. The power dissipation is 20 mW.

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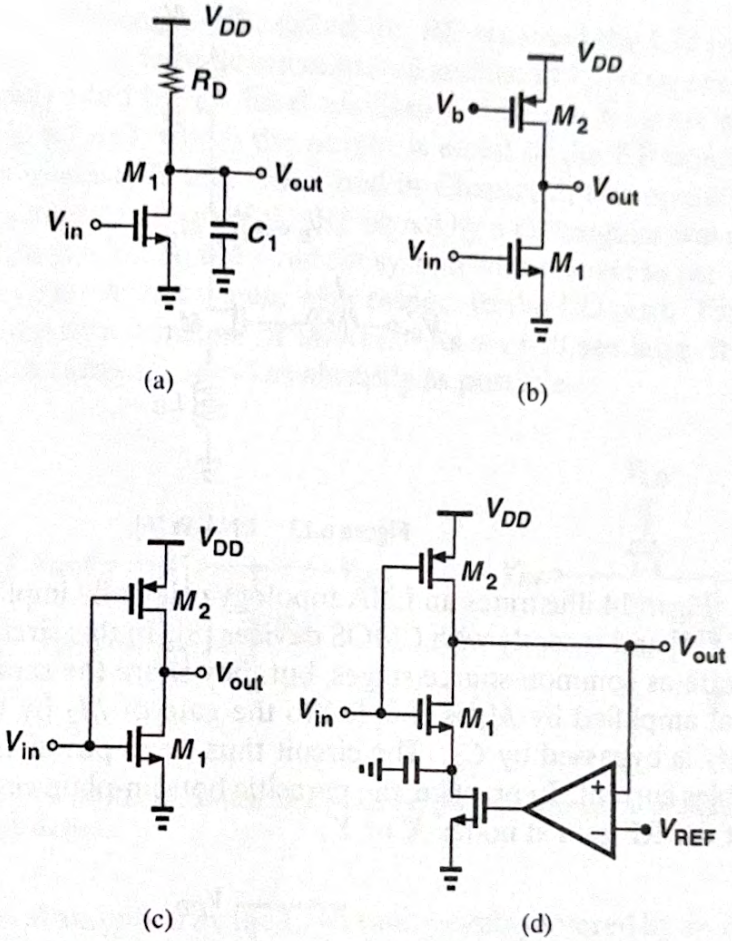


Figure 6.12 (a) Common-source stage with resistive load, (b) conversion of load to current source, (c) use of load as amplifying device, (d) LNA in [5].

Shown in Fig. 6.13 is a 1.5-GHz CMOS LNA employing on-chip and off-chip inductors [6]. In a manner similar to that described for the circuit of Fig. 6.7, this LNA incorporates L_S and L_1 to create conjugate matching at the input. At 1.5 GHz, the on-chip inductor L_D provides significant voltage gain even though its Q is less than 4. By contrast, a load resistor would require a large voltage drop to provide a comparable gain.

The common-gate transistor, M_2, plays two important roles by increasing the reverse isolation of the LNA: (1) it lowers the LO leakage produced by the following mixer, and (2) it improves the stability of the circuit by minimizing the feedback from the output to the input. Note that the same circuit with no cascode device would be prone to oscillation.

The LNA of Fig. 6.13 is followed by another cascode stage so as to drive a 50-Ω load, with each stage drawing 10 mA. Fabricated in a 0.6-μm CMOS technology and operating from a 1.5-V supply, the circuit achieves a noise figure of 3 dB, a gain of 20 dB, and an input IP_3 of -10 dBm.

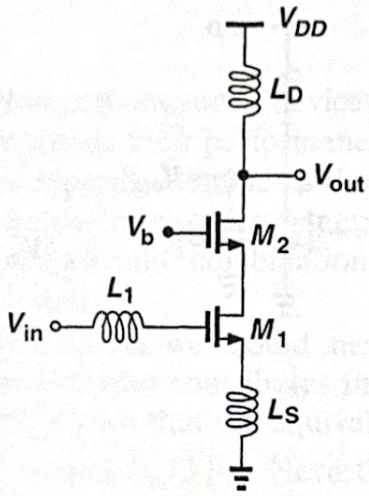


Figure 6.13 LNA in [6].

Fig. 6.14 illustrates an LNA topology originally implemented with MESFETs [7] and recently with CMOS devices [8]. In this circuit, both M_1 and M_2 operate as common-source stages, but they share the same bias current. The signal amplified by M_1 is coupled to the gate of M_2 by C_1 while the source of M_2 is bypassed by C_2. The circuit thus saves power through the reuse of the bias current. In practice, the parasitic bottom-plate capacitance of C_1 may limit the RF gain at nodes X or Y.

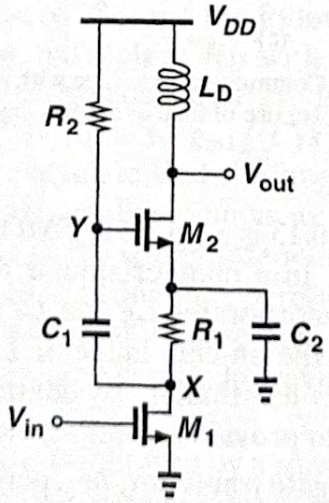


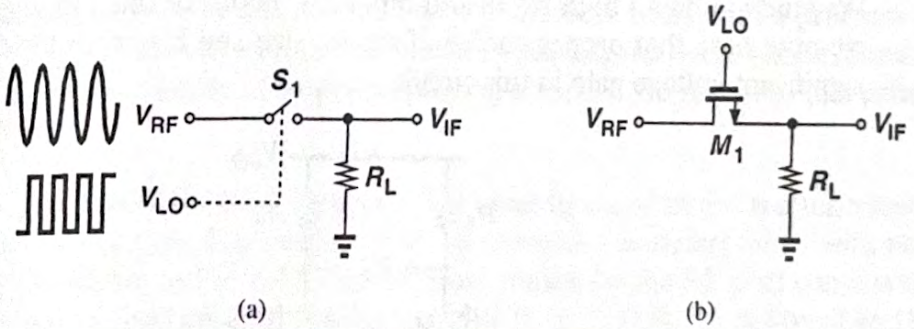
Figure 6.14 LNA in [7].

6.2 DOWNCONVERSION MIXERS

6.2.1 General Considerations

Mixers perform frequency translation by multiplying two signals (and possibly their harmonics). Downconversion mixers employed in the receive path have

two distinctly different inputs, called the RF port and the LO port. The RF port senses the signal to be downconverted and the LO port senses the periodic waveform generated by the local oscillator. This can be seen in the simple circuit of Fig. 6.15(a), where the output is equal to the RF input when S_1 is on and zero when S_1 is off. Described in Chapter 2, this operation can also be viewed as multiplication of the RF signal by a rectangular waveform. Note that the circuit is a linear, time-variant system with respect to the RF port and a nonlinear, time-variant system with respect to the LO port. This is true for most downconversion mixers of interest. As we will see later, it is desirable that the switch turn on and off as abruptly as possible.



(a) (b)

Figure 6.15 (a) Simple switch used as mixer, (b) implementation of switch with an NMOS device.

The signal amplified by the LNA (and possibly filtered by an image-reject filter) is applied to the RF port of the mixer. Thus, this port must exhibit sufficiently low noise and high linearity, the latter because nearby interferers are amplified by the LNA and hence can produce stronger intermodulation products. If the circuit of Fig. 6.15(a) incorporates a MOS switch [Fig. 6.15(b)], then the on-resistance of the transistor contributes noise. Furthermore, as the RF input signal varies, the gate-source overdrive voltage of M_1 and hence its on-resistance change, introducing nonlinearity in the voltage division between M_1 and R_L.

Listed in Table 6.2 are performance parameters of typical downconversion mixers. With a noise figure of 12 dB and an IIP_3 of +5 dBm, a mixer can be preceded by an LNA having a gain of approximately 15 dB with acceptable degradation in the overall noise and nonlinearity (Chapter 2).

TABLE 6.2 Typical mixer characteristics.

NF	12 dB
IIP_3	+5 dBm
Gain	10 dB
Input Impedance (Heterodyne)	50 Ω
Port-to-Port Isolation	10–20 dB

Passive and Active Mixers The circuit of Fig. 6.15(b) is an example of "passive" mixers because it does not provide any gain. The loss of the circuit can be calculated by noting that, if the LO signal has a 50% duty cycle, then the RF input is multiplied by a dimensionless square wave toggling between 0 and 1. Such a waveform has a fundamental at ω_{LO} with an amplitude equal to $\sin(\pi/2)/\pi = 1/\pi$. Since the IF signal results from convolving the input spectrum with this fundamental, the voltage gain of the circuit is equal to $1/\pi$.[1]

Active mixers, by contrast, generally provide gain. Shown in Fig. 6.16 is an example, where the RF input varies the drain current of M_1, and M_2 and M_3 function as a switching pair driven by the LO. Thus, the drain current of M_1 is in essence multiplied by a square wave as it is routed to R_1 and R_2 alternately. We study in detail both MOS and bipolar versions of this topology later, but we note here that proper choice of device size and bias currents can provide significant voltage gain in this circuit.

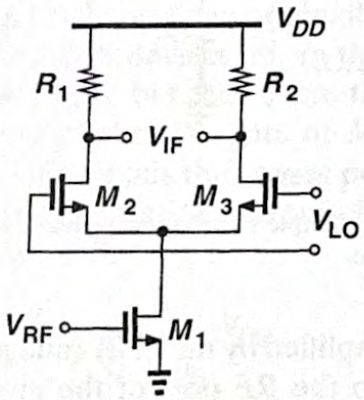


Figure 6.16 Active mixer.

By virtue of their gain, active mixers reduce the noise contributed by subsequent stages and are widely used in RF systems. Passive mixers, on the other hand, typically achieve a higher linearity and speed and find application in microwave and base station circuits.

Conversion Gain The gain of mixers must be carefully defined to avoid confusion. The "voltage conversion gain" of a mixer is defined as the ratio of the rms voltage of the IF signal to the rms voltage of the RF signal. Note that these two signals are centered around two different frequencies. The voltage conversion gain can be measured by applying a sinusoid at ω_{RF} and examining the amplitude of the downconverted component at ω_{IF}.

The "power conversion gain" of a mixer is defined as the IF power delivered to the load divided by the available RF power from the source. If the input impedance and the load impedance of the mixer are both equal to the

[1] This calculation assumes the on-resistance of the switch is much less than the impedance of the load.

source impedance, for example, 50 Ω, then the voltage conversion gain and power conversion gain of the mixer are equal when expressed in decibels.

Conjugate matching at the input of the mixers is necessary in the first downconversion stage of heterodyne receivers that employ image-reject filters. As mentioned earlier, the transfer function of these filters is usually characterized for only a standard termination impedance and may exhibit ripples if other impedance levels are used. The load impedance of the mixer, on the other hand, is typically *not* equal to 50 Ω because most passive IF filters have an input impedance of 500 to 1000 Ω.[2] In architectures such as homodyne topologies, the load seen by the mixer may be even higher to maximize the voltage gain.

From the above observation, we note that the voltage and power conversion gains of a mixer may not be equal in decibels. While not a problem per se, this difference can cause confusion in calculating the overall noise, linearity, and gain of a cascade of stages employing a mixer. We return to this issue in Section 6.3.

SSB and DSB Noise Figures The noise figure of mixers is often a source of great confusion. For simplicity, let us consider a *noiseless* mixer with unity gain. As shown in Fig. 6.17, the spectrum sensed by the RF port consists of a signal component and the thermal noise of R_S in both the signal band and the image band. Upon downconversion, the signal, the noise in the signal band, and the noise in the image band are translated to ω_{IF}. Thus, the output SNR is half the input SNR if the input frequency response of the mixer is the same for the signal band and the image band. In other words, the noise figure of a noiseless mixer is equal to 3 dB.

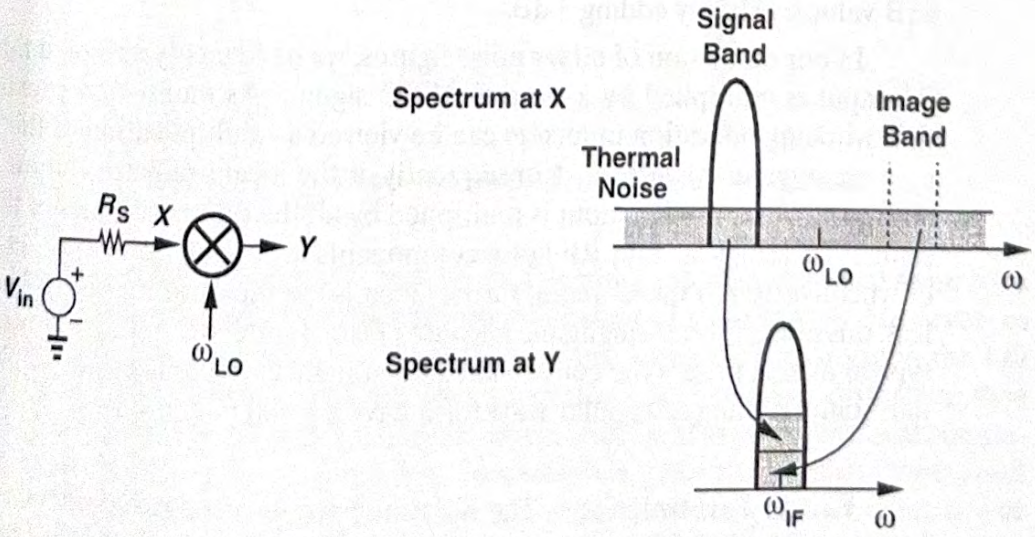


Figure 6.17 Folding of RF and image noise into the IF band.

[2] An exception is when the IF is quite high, for example, above 100 MHz.

The above measurement provides the "single-sideband" noise figure (SSB NF) of the mixer. The term SSB indicates that the desired signal spectrum resides on only one side of the LO frequency, a common case in heterodyne systems. Now, consider the homodyne downconversion of an AM signal by means of a single noiseless mixer (Fig. 6.18). In this case, the input and output signal-to-noise ratios are equal, giving a noise figure of 0 dB. This is called the "double-sideband" noise figure (DSB NF) so as to emphasize that the input signal spetrum resides on both sides of ω_{LO}.

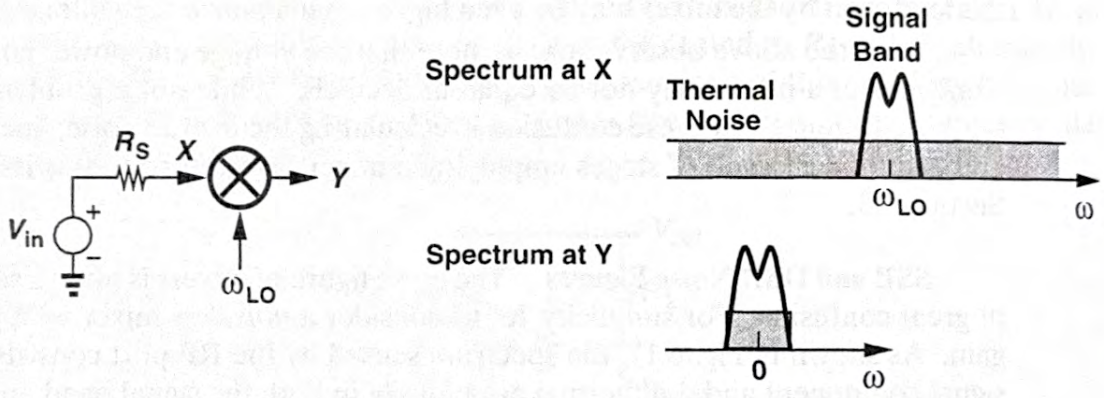


Figure 6.18 Downconversion of an AM signal.

In summary, the SSB noise figure of a mixer is 3 dB higher than the DSB noise figure if the signal and image bands experience equal gains at the RF port of a mixer. Typical noise figure meters measure the DSB NF and predict the SSB value by simply adding 3 dB.

In our discussion of mixer noise figures, we have tacitly assumed that the RF input is multiplied by a *sinusoidal* LO signal. As mentioned previously, the switching operation in mixers can be viewed as multiplication of the input by a *rectangular* waveform. Consequently, if the local oscillator output has a 50% duty cycle, the RF input is multiplied by all the odd harmonics of the LO signal. This suggests that RF noise components around $3\omega_{RF}$, $5\omega_{RF}$, etc., are downconverted to the IF band, further increasing the output noise. Nonetheless, this effect is often negligible because (1) the limited RF input bandwidth of typical mixers lowers the conversion gain at higher frequencies and (2) higher harmonics of the rectangular waveform have a small magnitude.

Port-to-Port Isolation The isolation between each two ports of a mixer is critical. The LO-RF feedthrough results in LO leakage to the LNA and eventually the antenna, whereas the RF-LO feedthrough allows strong interferers in the RF path to interact with the local oscillator driving the mixer. The LO-IF feedthrough is important because if substantial LO signal exists at the IF out-

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put even after low-pass filtering, then the following stage may be desensitized. Finally, the RF-IF isolation determines what fraction of the signal in the RF path directly appears in the IF, a critical issue with respect to the even-order distortion problem in homodyne receivers (Chapter 5).

The required isolation levels greatly depend on the environment in which the mixer is utilized. If the isolation provided by the mixer is inadequate, the preceding or following circuits may be modified to remedy the problem.

Single-Balanced and Double-Balanced Mixers If a mixer accommodates a differential LO signal but a single-ended RF signal, it is called "single-balanced," an example being the topology shown in Fig. 6.19(a). If a mixer operates with both differential LO and RF inputs, then it is called "double balanced," the active version of which assumes the form of a Gilbert cell [Fig. 6.19(b)].

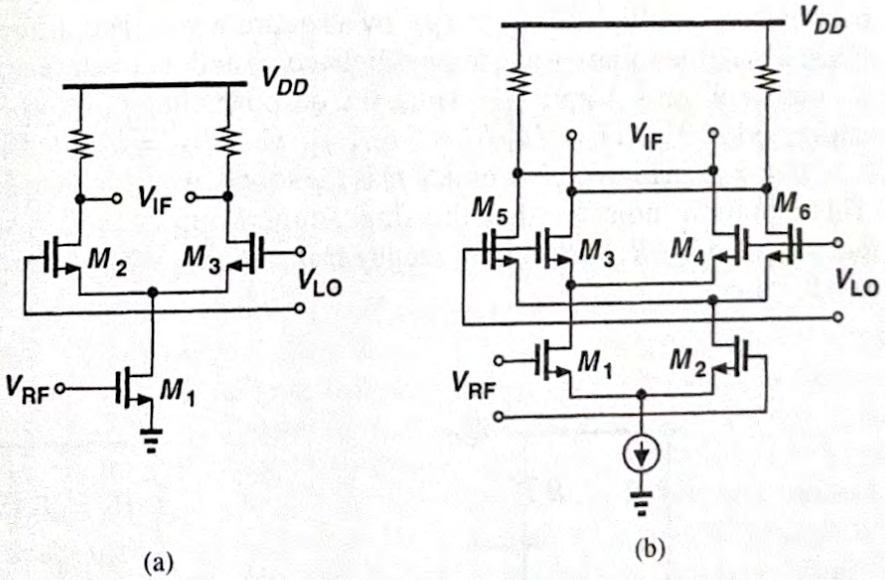


Figure 6.19 (a) Single-balanced mixer, (b) double-balanced mixer.

The single-balanced configuration exhibits less input-referred noise for a given power dissipation than the double-balanced counterpart. However, as explained in Section 6.2.4, the circuit is more susceptible to noise in the LO signal. The double-balanced mixer generates less even-order distortion, thus relaxing the half-IF issue in heterodyne receivers and lowering the beat components in homodyne architectures. Nevertheless, since the RF signal processed by the LNA (and possibly the image-reject filter) is usually single ended, one of the input terminals of the double-balanced mixer is simply connected to a bias voltage. This in turn creates different propagation times—i.e., phase shifts—for the two signal phases amplified by M_1 and M_2 in Fig. 6.19(b), leading to finite even-order distortion.

A drawback of the single-balanced mixer shown in Fig. 6.19(a) is the LO-IF feedthrough. Note that M_2 and M_3 operate as a differential pair, thus amplifying the LO signal. If the IF is not much lower than the LO frequency, then a first-order low-pass filter following the mixer may not adequately suppress the LO feedthrough without attenuating the IF signal. Thus, the large LO content may desensitize the IF amplifier. In the case of the double-balanced mixer of Fig. 6.19(b), on the other hand, the differential pairs M_3–M_4 and M_5–M_6 add the amplified LO signal with opposite phases, thereby providing a first-order cancellation. In general, the LO-IF feedthrough must be carefully studied in conjunction with the nonlinearities of the stages following the mixer.

In both mixer topologies of Fig. 6.19, the output can be sensed as either a differential or a single-ended signal. In addition to higher conversion gain, a differential output provides much more immunity to feedthrough of the RF signal to the IF output. To understand this effect, consider the simplified single-balanced mixers shown in Fig. 6.20, where the operation of both circuits can be viewed as multiplication of I_{RF} by a square wave. The difference is that in Fig. 6.20(a), the square wave toggles between 0 and +1, whereas in Fig. 6.20(b), it does between −1 and +1. Thus, the output voltage of both mixers can be expressed as $V_{out}(t) = I_{RF}R[a + bS(t)]$, where $a = b = 0.5$ in Fig. 6.20(a), $a = 0, b = 1$ in Fig. 6.20(b), and $S(t)$ is the square wave depicted in Fig. 6.20(b). This equation indicates that the single-ended output contains a component equal to $0.5I_{RF}R$, with no frequency translation. We call this effect "direct feedthrough."

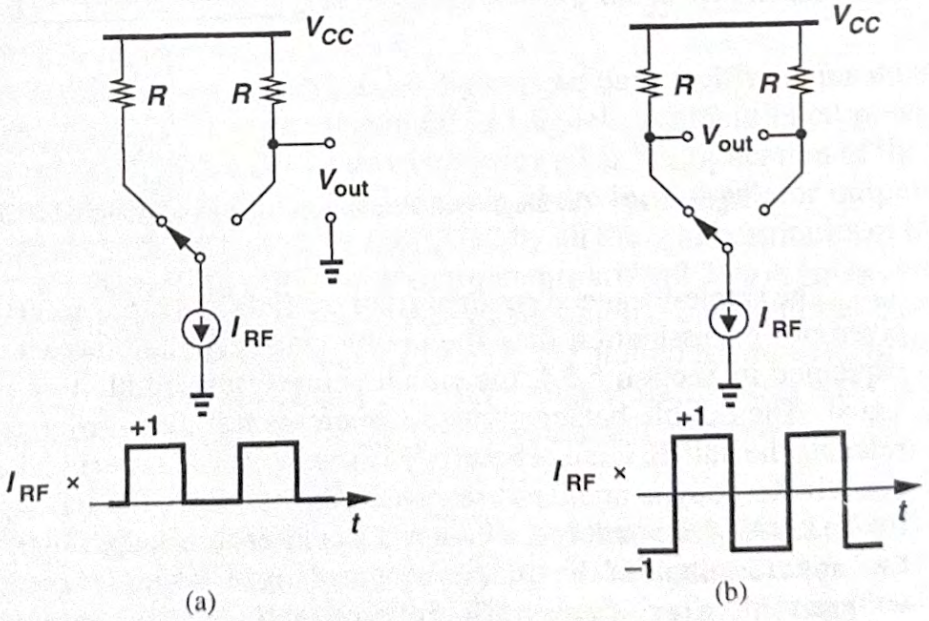


Figure 6.20 Simple mixers with (a) single-ended and (b) differential outputs.

Direct feedthrough of high-frequency components in I_{RF} is generally unimportant owing to the suppression provided by the low-pass filter at the IF output. Low-frequency components in I_{RF}, on the other hand, appear at the output without attenuation. Recall from our discussion of homodyne architectures in Chapter 5 that even-order distortion in the RF path (e.g., in the LNA) creates low-frequency beat or demodulated signals. Such signals directly appear in the single-ended output of the mixer, possibly corrupting the downconverted spectrum. In heterodyne receivers, this effect is negligible because, for two interferers to beat at IF, one usually falls out of the receive band and is therefore attenuated by the front-end filter.

Direct feedthrough of I_{RF} to V_{out} in Fig. 6.20(a) may also increase the noise figure of the mixer. This is because I_{RF} usually contains noise components in the vicinity of the intermediate frequency. In fact, the conversion gain of the mixer may be quite higher for such components than for the RF signal due to bandwidth limitations. As a result, the single-ended IF output carries the noise in I_{RF}.

By contrast, if the output is sensed differentially, the effect of direct feedthrough is much less significant. In Fig. 6.20(b), a finite feedthrough may exist because of mismatch-induced asymmetries as well as deviation of the LO duty cycle from 50%. Nonetheless, with typical mismatches in ICs, the feedthrough remains below a few percent.

Despite the advantages of differential output sensing, most mixers have been required to provide single-ended outputs, primarily because IF SAW filters have been available as single-ended devices. To reduce the effect of direct feedthrough and achieve the maximum gain, these applications often convert the differential output of the mixer to single-ended form by means of an external LC network [9]. Figure 6.21 depicts an example [10], where the network consisting of L_1, L_2, and C_1 converts the differential output current of the mixer to a single-ended current, I_{out}. Nevertheless, as differential SAW devices become available, the differential output of the mixer can directly drive the IF filter.

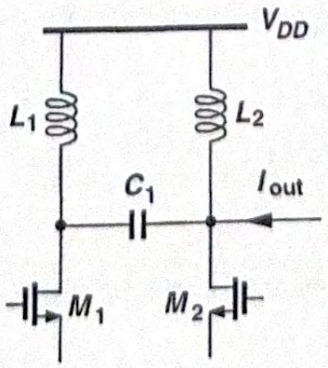


Figure 6.21 Conversion of differential currents to single-ended output.

Mixer Spurious Response In general, a mixer generates various cross-products of the RF and LO signals and their harmonics. The frequency of the resulting components can be expressed as $|m\omega_{RF} \pm n\omega_{LO}|$, where m and n are integers. A difficult task in receiver design is to ensure that, except for $|\omega_{LO} - \omega_{RF}|$, such components do not fall in the IF band. Owing to nonlinearities in the RF path, it is possible that harmonics of the interferers beat with harmonics of the LO, corrupting the downconverted signal. The spurious response for various combinations of m and n is usually analyzed with the aid of computer programs.

6.2.2 Bipolar Mixers

Single-balanced active bipolar mixers can be implemented as shown in Fig. 6.22, where emitter degeneration is utilized to achieve reasonable linearity. In each circuit, the RF input varies the collector current of Q_1, and the switching operation of Q_2–Q_3 multiplies this variation by a square wave. The circuit of Fig. 6.22(a) exhibits a relatively high input impedance and is not suited to heterodyne receivers where the image-reject filter must be terminated with a 50-Ω impedance. In Fig. 6.22(b), on the other hand, $R_E + 1/g_{m1}$ is chosen to be approximately equal to 50 Ω [2]. As mentioned in the context of common-base amplifiers (Section 6.1.3), the source impedance, R_S, linearizes the RF port of Fig. 6.22(b) to a much greater extent than it does in Fig. 6.22(a) while contributing the same amount of noise.

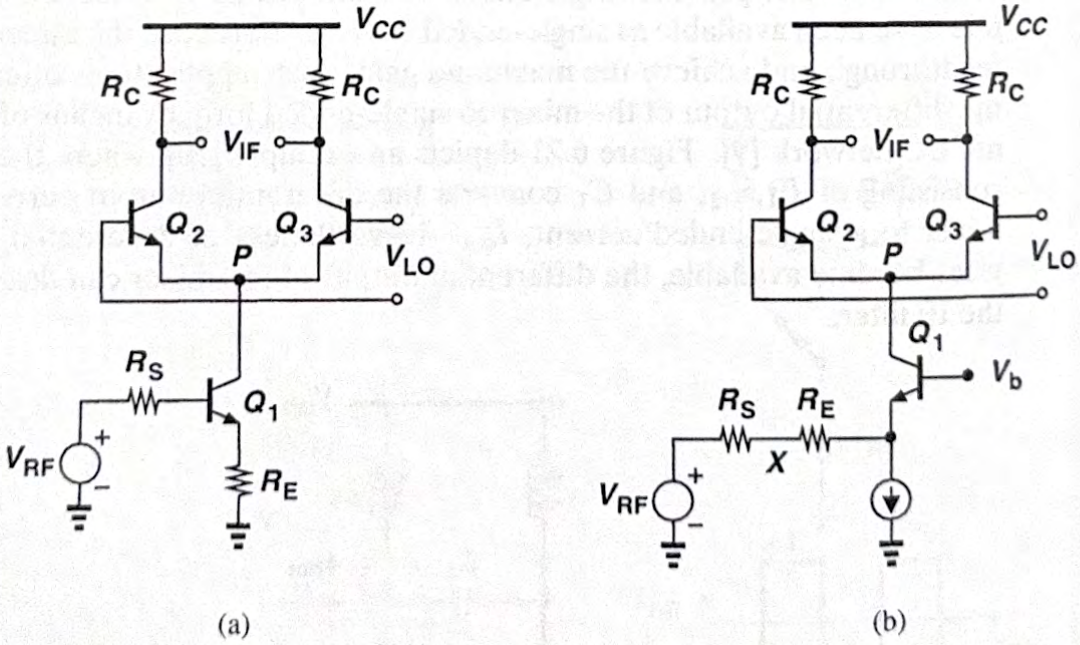


Figure 6.22 Bipolar mixers with RF signal applied to (a) base, (b) emitter of input device.

It is instructive to calculate the low-frequency voltage and power conversion gains of the mixer in Fig. 6.22(b) with the assumption that the Q_2–Q_3 pair experiences complete, instantaneous switching at each zero-crossing

point of V_{LO}. The small-signal collector current of Q_1 is equal to $I_{c1}(t) = V_{RF}(t)/(R_S + R_E + 1/g_{m1})$. If the LO waveform has a 50% duty cycle, then I_{c2}–I_{c3} is equal to the product of I_{c1} and a squarewave toggling between -1 and $+1$, yielding

$$V_{\text{out}}(t) = \frac{V_{RF}(t)R_C}{R_S + R_E + 1/g_{m1}} \cdot \frac{4}{\pi} \cos \omega_{LO} t, \tag{6.22}$$

where higher LO harmonics are neglected. Since multiplication of $V_{RF}(t)$ by $\cos \omega_{LO} t$ is equivalent to shifting $V_{RF}(\omega)$ by $\pm\omega_{LO}$ and dividing the result by a factor 2, the IF output in the frequency domain is equal to

$$V_{IF}(\omega) = \frac{V_{RF}(\omega - \omega_{LO})}{R_S + R_E + 1/g_{m1}} \frac{2R_C}{\pi}. \tag{6.23}$$

The voltage conversion gain is equal to the output IF voltage, V_{IF}, divided by the input RF voltage (at node X),

$$A_V = \frac{(2R_C/\pi)/(R_S + R_E + 1/g_{m1})}{(R_E + 1/g_{m1})/(R_S + R_E + 1/g_{m1})} \tag{6.24}$$

$$= \frac{2}{\pi} \frac{R_C}{R_E + 1/g_{m1}}, \tag{6.25}$$

which, for matched input, $R_S = R_E + 1/g_{m1}$, reduces to

$$A_V = \frac{1}{\pi} \frac{2R_C}{R_S}. \tag{6.26}$$

To calculate the power conversion gain, we note that the average IF power delivered to the load is equal to

$$P_{IF} = \frac{V_{IF,rms}^2}{2R_C}, \tag{6.27}$$

where the factor 2 in the denominator signifies the fact that $V_{IF,rms}$ appears across $2R_C$. From (6.23), we have

$$P_{IF} = \frac{V_{RF,rms}^2 R_C^2}{(R_S + R_E + 1/g_{m1})^2} \frac{4}{\pi^2} \frac{1}{2R_C} \tag{6.28}$$

$$= \frac{V_{RF,rms}^2 R_C}{(R_S + R_E + 1/g_{m1})^2} \frac{2}{\pi^2}. \tag{6.29}$$

The available source power is

$$P_{\text{in}} = \frac{V_{RF,rms}^2}{4R_S}, \tag{6.30}$$

The power gain is therefore given by

$$A_p = \frac{P_{IF}}{P_{\text{in}}} \tag{6.31}$$

$$= \frac{8}{\pi^2} \frac{R_S \cdot R_C}{(R_S + R_E + 1/g_{m1})^2}, \tag{6.32}$$

which, for $R_S = R_E + 1/g_{m1}$, reduces to

$$A_p = \frac{1}{\pi^2} \frac{2R_C}{R_S}. \tag{6.33}$$

From Eqs. (6.26) and (6.33), we note that, in general, $A_P \neq A_V^2$, and hence the voltage and power conversion gains are not equal if expressed in decibels. In the special, but rare, case where the differential load resistance, $2R_C$, is equal to the source resistance, R_S, we have $A_P = A_V^2$.

The contrast between voltage and power conversion gains can also be seen by expressing the latter as

$$A_P = \frac{V_{\text{out}}^2/R_L}{V_{\text{in}}^2/R_S} \tag{6.34}$$

$$= A_V^2 \frac{R_S}{R_L}, \tag{6.35}$$

indicating a difference of $10\log(R_S/R_L)$.

In reality, the conversion gains of the circuit are somewhat lower than those calculated above because of parasitic capacitances in the signal path. More accurate values must be obtained by careful simulations.

Defering the calculation of the noise figure to Section 6.2.4, we now consider the nonlinear behavior of the mixers in Fig. 6.22. The principal source of distortion in active mixers is the nonlinearity of the input voltage-to-current converter, for example, the network comprising Q_1, R_E, and R_S in Figs. 6.22(a) and (b). The high IIP_3 required of mixers usually mandates the use of substantial resistive degeneration at the input, creating trade-offs among noise, nonlinearity, and power dissipation.

Another type of nonlinearity in the mixers of Fig. 6.22 stems from the variation of the base-emitter diffusion capacitance of Q_2–Q_3 with the collector current of Q_1 [11]. Since in practice the LO signal is close to a sinusoid and hence the differential pair does not switch abruptly, Q_2 and Q_3 are simultaneously on for a fraction of the period. During this time, the base-emitter capacitance of Q_2–Q_3 acts as a nonlinear shunt for the collector current of Q_1, distorting the collector currents of Q_2 and Q_3. This effect can be lowered by increasing the LO slew rate or decreasing the base resistance of the differential pair [11].

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It is also interesting to examine the LO-RF feedthrough in Figs. 6.22(a) and (b). In both cases, if the LO signal is fully differential and Q_2 and Q_3 are perfectly matched, the waveform at node P experiences *two* full excursions in each period of the LO, thus exhibiting frequency components equal to $2\omega_{LO}$ and above. In Fig. 6.22(a) this waveform is coupled to the RF input through the base-collector junction capacitance of Q_1, and in Fig. 6.22(b) it is greatly attenuated by the high reverse isolation of the common-base stage. The key point here is that the leakage signal contains frequency components that are far from the band of interest and hence less problematic than direct feedthrough of ω_{LO}.

In practice, however, the mixer suffers from a finite feedthrough at ω_{LO}. The primary reason is that in most cases the LO signal is single ended and provided externally, thus coupling through bond wires and the substrate to the RF input. For example, in an actual implementation of the circuit shown in Fig. 6.22(b), the single-ended LO feedthrough to the RF port is approximately equal to -33 dB [2] even though Q_1 effectively isolates the input from the waveform at node P.

While exhibiting a lower LO-RF isolation than its counterpart in Fig. 6.22(b), the circuit of Fig. 6.22(a) has a higher input impedance and is therefore better suited to architectures where the LNA and the mixer must interface directly, i.e., if no image-reject filter is necessary.

Double-balanced bipolar mixers in the form of Gilbert cell have also been used extensively. In addition to lower LO-IF feedthrough, the Gilbert cell allows further linearization of the RF port by Schmook's technique [12]. To understand this technique, first note that if, as shown in Fig. 6.23(a), a bipolar differential pair employs two transistors with different emitter areas, A and nA, then its input-output characteristic is shifted horizontally by $V_T \ln n$. Now if two such differential pairs are cross connected [Fig. 6.23(b)], then the overall characteristic tends to be "smoother." Plotted in Fig. 6.23(c) is the equivalent transconductance, G_m, of the compound differential pair as a function of the input voltage, revealing that G_m exhibits a flat portion for $n \approx 4$ [12].

In practice, to achieve acceptable linearity, the cross-coupled differential pairs of Fig. 6.23(b) may still incorporate some resistive degeneration. Nonetheless, the combination of the two linearization methods can yield a lower noise figure for a given IIP_3 than a single resistively degenerated differential pair.

Another double-balanced bipolar mixer is shown in Fig. 6.24 [3]. Here, an on-chip transformer both operates as a single-ended to differential converter and provides input matching. The bias current of the switching quad is established by I_{EE}, and capacitors C_1–C_3 effect resonance at the primary and secondary of the transformer. A 1.9-GHz implementation of this configuration in an 11-GHz bipolar technology exhibits an SSB NF of 10.9 dB with an IIP_3 of +2.3 dBm while dissipating 5 mW from a 1.9-V supply [3].

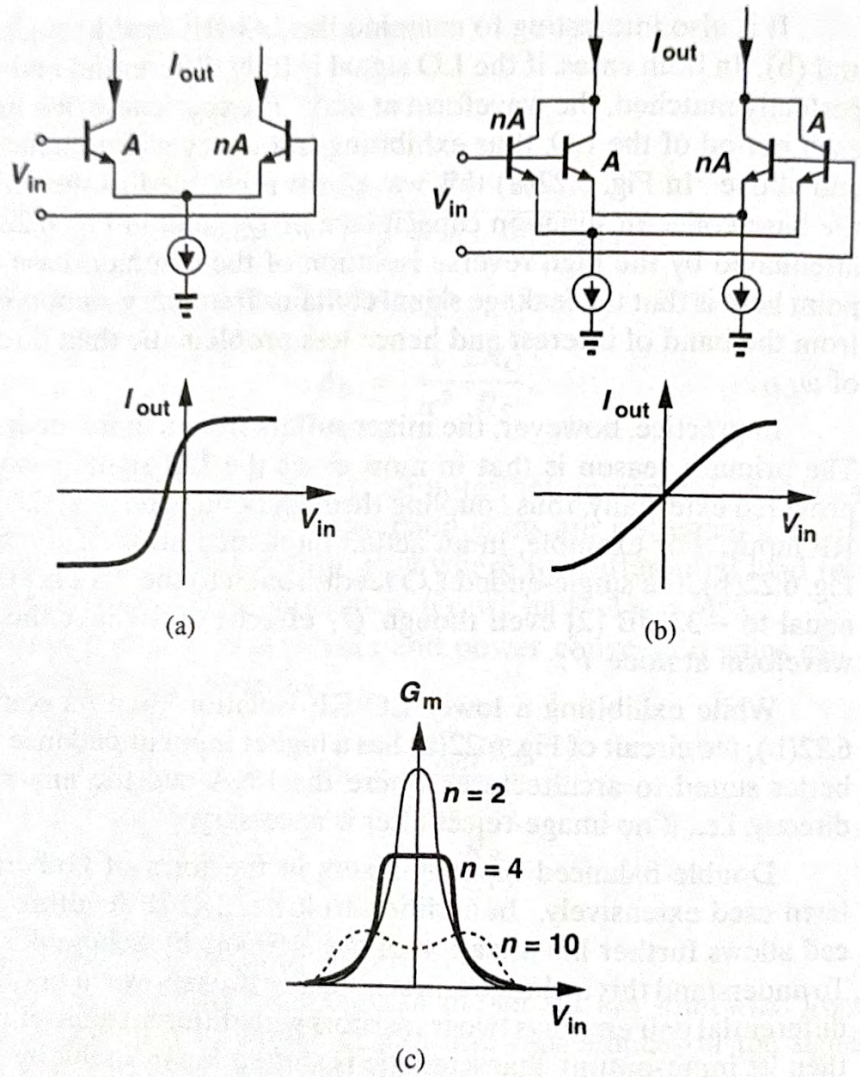


Figure 6.23 (a) Asymmetric differential pair, (b) Schmook's linearized pair, (c) variation of equivalent G_m with input level.

Other linearization techniques are described in [13, 14].

6.2.3 CMOS Mixers

Active CMOS mixers can be implemented as the single-balanced and double-balanced topologies shown in Fig. 6.19. Most of the design considerations described above for bipolar mixers apply to the CMOS counterparts as well. For example, the trade-offs among noise, nonlinearity, and power dissipation, especially in the RF voltage-to-current converter, typically lead to a compromise in the design.

Consider the single-balanced mixer of Fig. 6.25. The LO voltage swing in this circuit directly affects the conversion gain and the noise. This is because the MOS switching pair, M_2–M_3, typically requires much greater swings to experience complete switching than does a bipolar counterpart. If M_2 and M_3

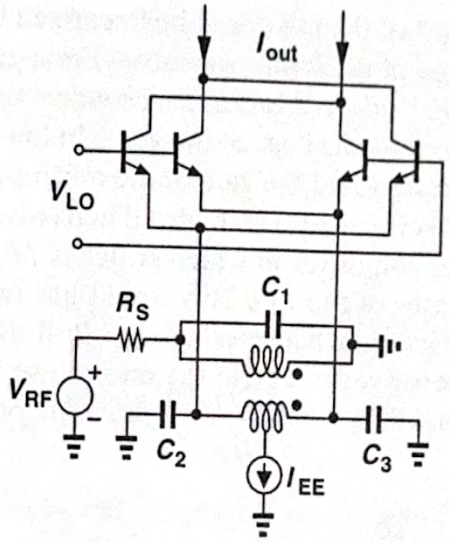


Figure 6.24 Mixer using transformer at RF input.

are simultaneously on for a significant part of the period, then some of the RF current generated by M_1 is "wasted" as a common-mode signal during this time. This lowers the conversion gain and, as we will see in Section 6.2.4, increases the noise contributed by M_2 and M_3.

For a given LO drive, the switching of M_2 and M_3 can be made more abrupt by increasing their width or decreasing their drain current. The first remedy increases the capacitance seen at node P, shunting the RF current.[3] The second approach decreases the transconductance of M_2 and M_3, raising the impedance seen looking into the source terminals of these devices and hence allowing more RF current to flow through the capacitance at node P. For these reasons, the total bias current and the width of M_2 and M_3 must be chosen with the available LO swing in mind.

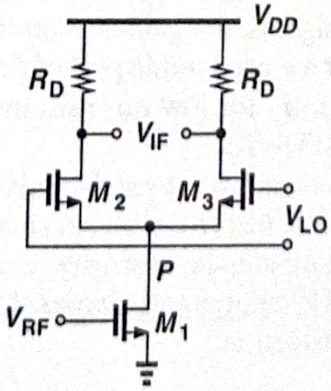


Figure 6.25 CMOS active mixer.

[3] The transconductance of M_2 and M_3 also increases but more slowly than the capacitance at node P.

The RF port of the mixer can be linearized by increasing the gate-source overdrive voltage of the input transistor. For a given bias current, however, a higher overdrive leads to a lower transconductance, thus increasing the noise figure and decreasing the conversion gain. In low-voltage design, the trade-off between the linearity and the gain of the mixer often becomes problematic.

CMOS mixers can also be realized in passive form. Shown in Fig. 6.26(a) is a downconversion mixer in which switches M_1 and M_2 are driven by complementary phases of the LO. This circuit has two advantages over its active counterparts. First, it achieves a higher IP_3 if M_1 and M_2 experience a large gate-source overdrive voltage in the on state so that V_{RF} does not vary their on-resistance significantly. Second, it draws no power from the supply voltage.

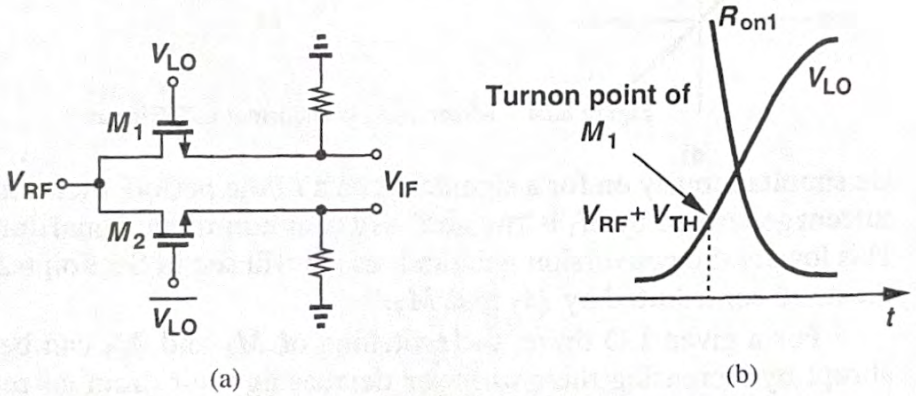


Figure 6.26 (a) Passive CMOS mixer, (b) variation of switch on-resistance.

The passive mixer of Fig. 6.26(a) nonetheless suffers from a number of severe drawbacks. First, because the gain of the circuit is less than unity, the noise of the stage following the mixer is "magnified" when referred to V_{RF}. Calculations similar to those in Section 6.2.2 show that the voltage gain of the mixer in the ideal case of instantaneous switching is equal to $2/\pi (\approx -4$ dB). For sinusoidal LO signals, the gain is even lower because M_1 and M_2 are simultaneously on for a considerable part of the period. Second, the large width required of M_1 and M_2 for low on-resistance leads to substantial capacitive feedthrough from LO to IF.

The linearity advantage of passive mixers diminishes at low supply voltages. As shown in Fig. 6.26(b), with sinusoidal LO signals, the switches have a relatively small gate-source overdrive voltage for a significant part of the period. Thus, the RF input greatly varies the switch on-resistance during this time, introducing distortion.

6.2.4 Noise in Mixers

The time variance and frequency translation in mixers make it difficult to calculate the noise figure. As illustrated conceptually in Fig. 6.27, the noise components of interest lie in the RF range before downconversion and in the IF

range after downconversion. The translation of the RF noise components by the switching stage prohibits the direct use of small-signal ac and noise analysis in SPICE, mandating simulations in the time domain. However, most present versions of SPICE do not provide time-domain noise analysis. Another difficulty is that the noise contributed by the switching stage exhibits time-varying statistics.

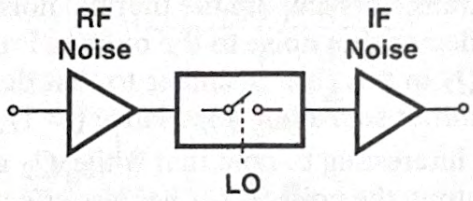


Figure 6.27 Conceptual view of a mixer.

Qualitative Analysis Before calculating noise of mixers, we make some qualitative observations regarding the single-balanced topology of Fig. 6.28(a). What are the sources of noise in this circuit? In the RF path, the thermal noise due to the base resistance of Q_1 and the emitter resistor, R_E, and the collector shot noise of Q_1 constitute the principal components. In the IF path, resistors R_{C1} and R_{C2} introduce thermal noise.

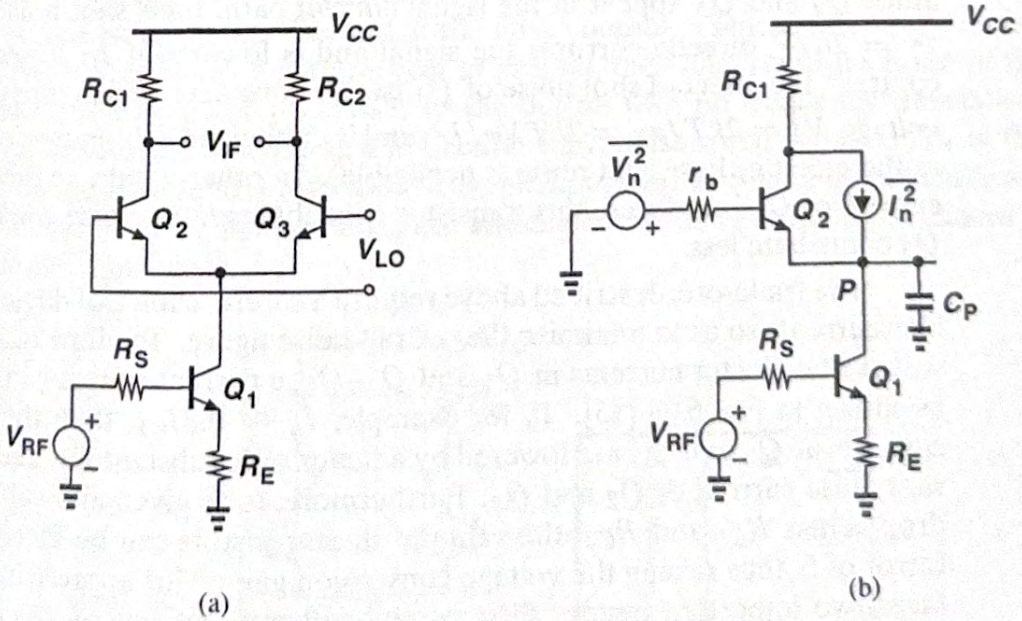


Figure 6.28 (a) Single-balanced mixer, (b) noise contribution of Q_2 when Q_3 is off.

The noise contributed by Q_2 and Q_3 requires more attention. First, let us assume these transistors switch instantaneously. Then, as shown in Fig. 6.28(b), each device is on for approximately half of the LO period, pumping noise to the output because the parasitic capacitance at node P, C_P, provides a finite impedance to ground. Arising from the base-emitter junction of Q_2 and Q_3

and collector-base and collector-substrate junctions of Q_1, this capacitance can be substantial if the transistors are large structures so as to minimize their base resistance. Thus, the RF noise due to the base resistance and collector current of Q_2 is translated to IF by the switching action of this transistor.

Now consider a more realistic case where the LO signal is not a square wave and Q_2 and Q_3 are simultaneously on for part of the period. During this time, the two transistors amplify the thermal noise of their base resistance and inject their collector shot noise to the output. From another point of view, the operation of Q_2 in this case is similar to that depicted in Fig. 6.28(b), except that here its emitter sees a low impedance ($\approx 1/g_{m3}$) to ground.

It is also interesting to note that while Q_2 and Q_3 are on, both injecting noise to the output, the noise in I_{C1} has less effect because it appears primarily as a common-mode component. In other words, when the noise of Q_2 and Q_3 is most substantial, the noise in I_{C1} is not and vice versa.

From the above observations, we infer that the contribution of thermal and shot noise of Q_2 and Q_3 can be minimized by (1) employing large LO swings (without saturating Q_2 and Q_3); (2) lowering C_P, which translates to smaller sizes for Q_1–Q_3 and hence higher base resistance noise; (3) reducing the base resistance of Q_2 and Q_3, which leads to higher C_P; and (4) decreasing the collector currents of Q_2 and Q_3. The last remedy merits some explanation. Since Q_2 and Q_3 appear in the signal *current* path, their shot noise *current*, $\overline{I_n^2} = 2qI_C$, directly corrupts the signal and is lowered if I_C *decreases*. By contrast, the effect of shot noise of Q_1 can be considered as an input-referred *voltage*, $\overline{V_n^2} = 2kT/g_m = 2kTV_T/I_C$, and is minimized if I_C *increases* (so long as the effect of base shot noise is negligible). In other words, as the collector current of Q_1 is reduced, this transistor contributes more noise while Q_2 and Q_3 contribute less.

The trade-offs described above require a careful choice of device size and bias currents so as to minimize the overall noise figure. To allow independent values of collector currents in Q_1 and Q_2–Q_3, a current source can be added as shown in Fig. 6.29 [15]. If, for example, $I_S \approx 0.8I_{C1}$, then the collector currents of Q_2 and Q_3 are lowered by a factor of 5, substantially reducing the shot noise current of Q_2 and Q_3. Furthermore, for a given allowable voltage drop across R_{C1} and R_{C2}, the value of these resistors can be increased by a factor of 5, thus raising the voltage conversion gain. This approach, however, faces two important issues. First, as the collector current of Q_2 and Q_3 is lowered, the impedance seen looking into their emitters rises, allowing more RF current provided by Q_1 to be shunted to ground through C_P. Second, the noise current arising from I_S itself directly adds to the RF signal. For these reasons, the addition of I_S to the mixer may decrease the noise figure by only a small amount.

It is important to make two other observations regarding the mixer of Fig. 6.28(a). First, the thermal noise generated by the output resistance of the LO

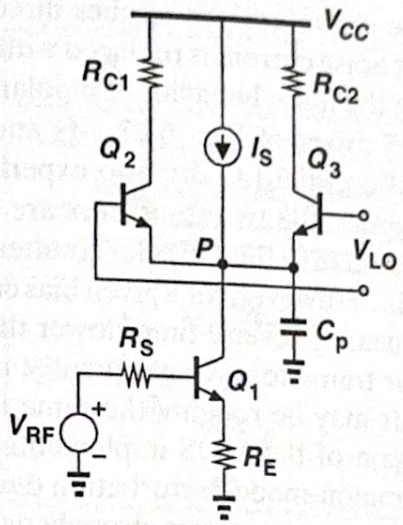


Figure 6.29 Addition of current source I_S to lower the collector current of Q_3 and Q_4.

circuitry also raises the noise figure, often requiring high power dissipation in the LO output buffer. For example, as depicted in Fig. 6.30, if a differential pair precedes the LO port, the noise produced by such a stage may be much higher than that due to Q_2 and Q_3. This effect is intensified by the high noise floor of typical oscillators. Note that double-balanced mixers are much more immune to LO noise. Second, if the mixer output is sensed in a single-ended form, e.g., at node X with respect to ground, then *low-frequency* noise in the collector current of Q_1 passes to the output with no frequency translation. This is because, as explained in Section 6.2.1, noise components in I_{C1} in the IF range appear in V_X as well. This phenomenon is usually quite significant because low-frequency noise is not attenuated by the parasitic capacitances in the RF signal path.

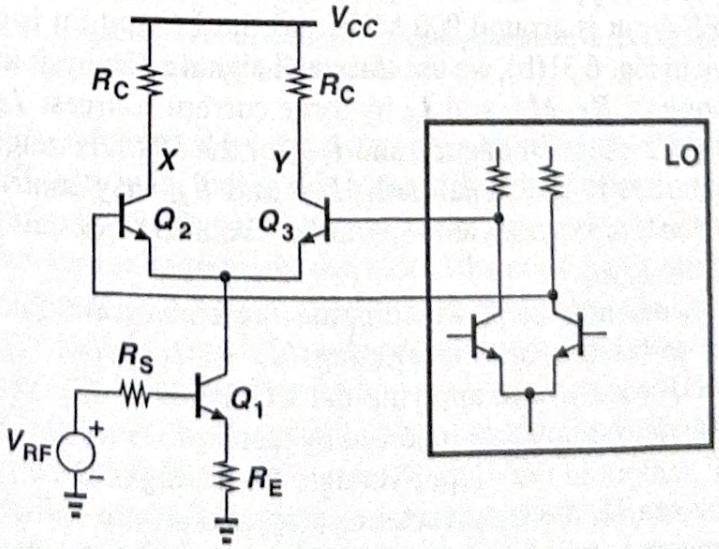


Figure 6.30 Inclusion of LO output noise in a mixer.

Most of the above analysis applies directly to MOS implementations if the collector shot noise current is replaced with channel thermal noise. Some of the differences in the noise behavior of bipolar and MOS mixers are as follows.

In the MOS mixer of Fig. 6.25, M_2 and M_3 typically require approximately 1 V of differential LO drive to experience complete switching. With sinusoidal LO signals, the two transistors are simultaneously on for a greater fraction of the period than their bipolar counterparts, potentially injecting more noise to the output. However, for a given bias current, the channel noise current of MOSFETs is usually several times lower than than the collector shot noise current of bipolar transistors. Consequently, the overall noise contribution of the switching pair may be roughly the same in both technologies. However, the conversion gain of the MOS implementation may be lower because the RF signal is a common-mode perturbation during the time M_2 and M_3 are on simultaneously. These parameters strongly depend on the specific design and the available LO swings.

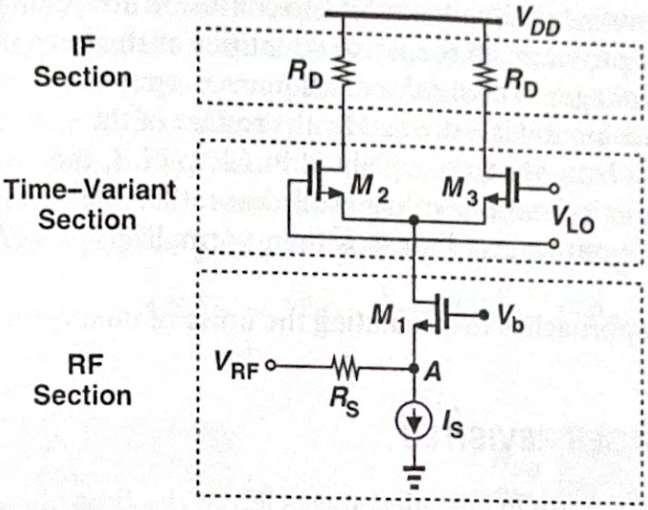
Another difference is that, for comparable device sizes and parasitic capacitances, the gate resistance of MOSFETs is much less than the base resistance of bipolar transistors.

Quantitative Analysis Consider the single-balanced mixer shown in Fig. 6.31(a). From our qualitative analysis, we can identify three sections in the circuit: the RF section, the time-variant section, and the IF section. To arrive at an estimate of the noise figure, we apply the following procedure: (1) for each source of noise, calculate a "conversion gain" to the IF output; (2) multiply the magnitude of each noise by the corresponding gain and add up all the resulting powers, thus obtaining the total noise at the IF output; (3) divide the output noise by the overall conversion gain to find the input-referred noise voltage, $\overline{V_{ni}^2}$; and (4) calculate $NF = \overline{V_{ni}^2}/(4kTR_S)$.

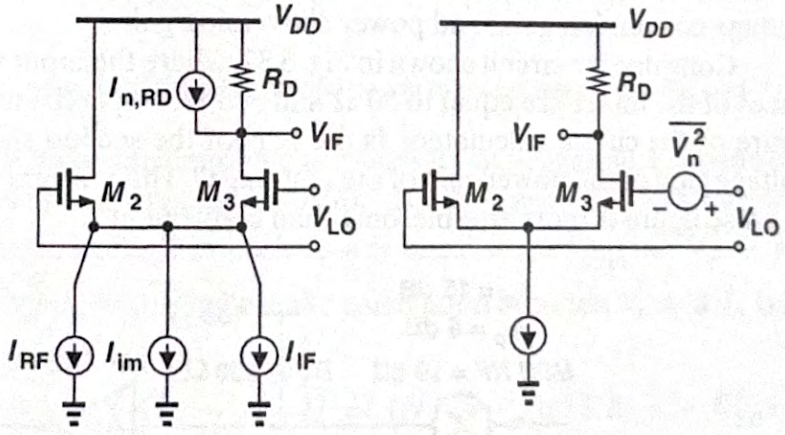
Let us apply the above procedure to the circuit of Fig. 6.31(a), assuming the RF input is around 900 MHz and the LO output is around 50 MHz. As shown in Fig. 6.31(b), we use the small-signal ac analysis in SPICE to represent the noise of R_S, M_1, and I_S by three current sources: I_{RF} for the RF range, I_{im} for the image frequency, and I_{IF} for the 50 MHz range. Owing to parasitic capacitances in the signal path, I_{RF} and I_{im} may contribute differently and must therfore be modeled separately. We also represent the IF thermal noise of R_D by $I_{n,RD}$.

In the next step, we compute the conversion gain from each current source to the output. Substituting $I_{RF} = I_1 \cos \omega_1 t$, $I_{im} = I_2 \cos \omega_2 t$, and $I_{IF} = I_3 \cos \omega_3 t$ and applying the LO signal to M_2 and M_3, we perform a time-domain simulation followed by fast Fourier transform (FFT) to calculate the IF content in the output voltage. To distinguish the relative contributions of each source, the frequencies ω_1, ω_2, and ω_3 are chosen such that their corresponding components at the IF output do not coincide. The contribution of $I_{n,RD}$ can be included easily.

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(a)



(b) (c)

Figure 6.31 (a) Sections of a mixer, (b) modeling the noise in the RF section, (c) modeling the noise in time-variant section.

The noise contributed by the switching pair must also be taken into account. The difficulty in including this noise is that the drain currents of M_2 and M_3 vary periodically, making the noise statistics also periodic functions of time. As a first-order approximation, we can model the noise with a voltage source in series with each gate [Fig. 6.31(c)] and choose the magnitude according to the transconductance of M_2 and M_3 under equilibrium conditions ($I_{D2} = I_{D3}$). The IF noise is then calculated by finding the conversion gain for each source (while the LO signal is also applied). Alternatively, the noise can be made a function of the drain current of the transistors [16].

With the above calculations, the output noise in the IF range can be found by multiplying each noise source by its respective conversion gain and adding up the noise powers. In this computation, the different levels of impedance at

different points in the circuit may lead to confusion in defining power quantities. To avoid this problem, all the noise quantities at the output can be expressed in terms of voltages. The total mean square output noise voltage can then be referred to the input if it is divided by the square of the voltage conversion gain of the mixer. Note that, as explained in Chapter 3, the voltage gain used in this calculation is from the voltage source—rather than from node A—to the output. The input-referred noise is then normalized to $4kTR_S$ to obtain the noise figure.

Other approaches to calculating the noise of mixers are described in [17].

6.3 CASCADED STAGES REVISITED

Our analysis of noise in cascaded stages led to the Friis equation in Chapter 2. In practice, a great deal of confusion may arise if this equation is applied to a cascade of stages where the impedance levels vary from one block to the next. In this section, we study two cases so as to reinforce the concepts of noise, loss, voltage conversion gain, and power conversion gain.

Consider the circuit shown in Fig. 6.32, where the input and output impedances of the mixer are equal to 50 Ω and 500 Ω, respectively. How is the noise figure of the circuit calculated: Is the NF of the second stage divided by the voltage gain or the power gain of the first stage? This is a case where the concept of noise figure is more troublesome than convenient.

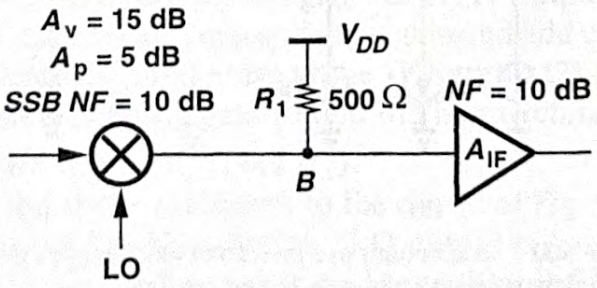


Figure 6.32 Cascade of a mixer and an IF amplifier.

To find the overall noise figure, we can take two different approaches: (1) Avoid defining an NF for A_{IF}, simply consider A_{IF} as part of the mixer, and follow the noise calculations outlined in Section 6.2.4. From an "analog" point of view, A_{IF} can be fully characterized by an input noise voltage and an input noise current, with no need for calculating its noise figure. (2) Return to the derivation of the Friis formula with particular attention to the definition of NF.

While approach (1) seems conducive to IC design, approach (2) becomes inevitable if the mixer and the IF amplifier are stand-alone circuits characterized by only their noise figures and gains. For this reason, we must still find out if the noise figure of A_{IF} is divided by the voltage gain or the power gain of the mixer. The first cause of confusion here is the definition of the NF of A_{IF}.

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In Fig. 6.32 the NF of the second stage must be calculated for $R_S = 500\ \Omega$, but manufacturers' data sheets typically give the NF for a source impedance of 50 Ω. How are these two quantities related? If the amplifier input-referred noise can be modeled with only a voltage source, i.e., if the input noise current is negligible (Fig. 6.33), then the noise figures corresponding to two different source impedances R_{SA} and R_{SB} are, respectively, given by $NF_A = 1 + \overline{V_n^2}/(4kTR_{SA})$ and $NF_B = 1 + \overline{V_n^2}/(4kTR_{SB})$, yielding:

$$(NF_A - 1)R_{SA} = (NF_B - 1)R_{SB}. \tag{6.36}$$

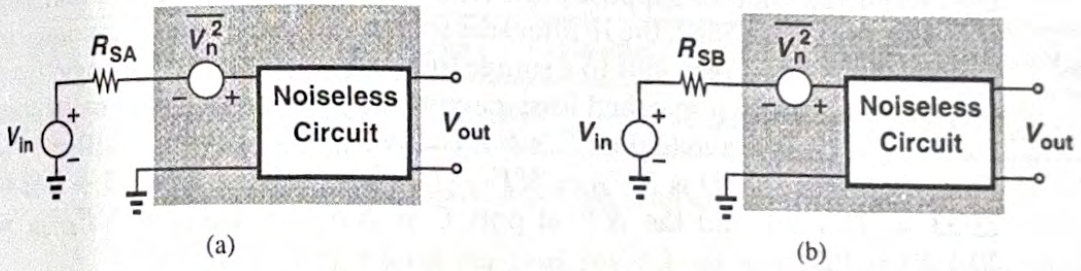


Figure 6.33 Calculation of noise figure with respect to source resistances R_{SA} and R_{SB}.

If the input noise current of the amplifier is not negligible, the two noise figures are generally not related by (6.36). As shown in Fig. 6.34, the total input-referred noise voltage in each case is equal to: $\overline{V_{nA,\text{tot}}^2} = \overline{V_n^2} + R_{SA}^2\overline{I_n^2}$ and $\overline{V_{nB,\text{tot}}^2} = \overline{V_n^2} + R_{SB}^2\overline{I_n^2}$, where the correlation between V_n and I_n is neglected. Thus,

$$(NF_A - 1)4kTR_{SA} - R_{SA}^2\overline{I_n^2} = (NF_B - 1)4kTR_{SB} - R_{SB}^2\overline{I_n^2}, \tag{6.37}$$

indicating that one NF cannot be calculated in terms of the other if $\overline{I_n^2}$ is unknown. For IF amplifiers operating above roughly 50 MHz, the contribution of $\overline{I_n^2}$ may be significant and (6.36) may not provide an accurate conversion. Nevertheless, we continue our derivation by neglecting $\overline{I_n^2}$ because the effect of this current is ultimately suppressed by the overall gain of the stages preceding the amplifier.

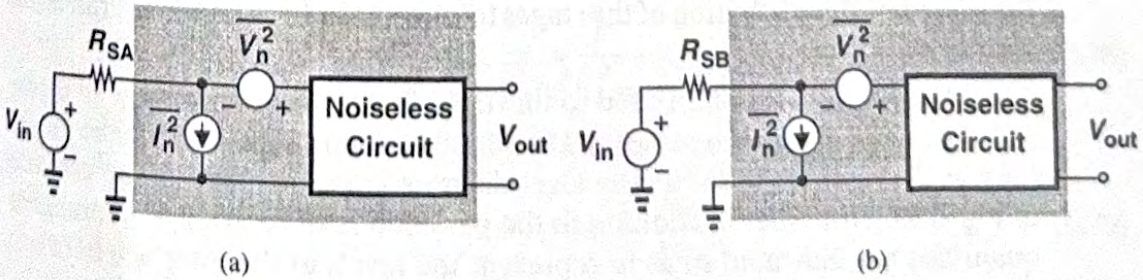


Figure 6.34 Calculation of noise figure with finite input noise current.

The second source of confusion is the Friis equation with different interstage impedance levels. Recall from Chapter 2 that in the Friis equation, $NF_2 - 1$ is divided by the available power gain of the preceding stage only if NF_2 is calculated with respect to R_{out1}. Thus, in Fig. 6.32 if the noise figure of the IF amplifier corresponds to a source impedance of 500 Ω, then $NF_{IF} - 1$ must be divided by the power conversion gain of the mixer. If, on the other hand, the noise figure of the IF amplifier is available for only a source impedance of 50 Ω and the input noise current is negligible, then $NF_{IF} - 1$ must be divided by the square of the voltage conversion gain of the mixer.

We now study a typical heterodyne receive path, Fig. 6.35, and compute the overall noise figure. Suppose ports A, B, C, and D are conjugate-matched for an impedance of 50 Ω, the IF filter sees source and load impedances equal to 500 Ω, and NF_6 corresponds to a source impedance of 500 Ω. We begin from the last stage. Since a matched lossy circuit raises the noise figure by its loss, the noise figure referred to port E is $NF_E = NF_6|_{dB} + L_5|_{dB} = 15$ dB$= 31.6$. Thus, the NF at port D is $NF_D = NF_4 + (NF_E - 1)/A_{P4} = 15.85 + 9.68 \approx 25.53 = 14.1$ dB, and the NF at port C is $NF_C = L_3|_{dB} + NF_D|_{dB} = 20.1$ dB $= 102.3$.

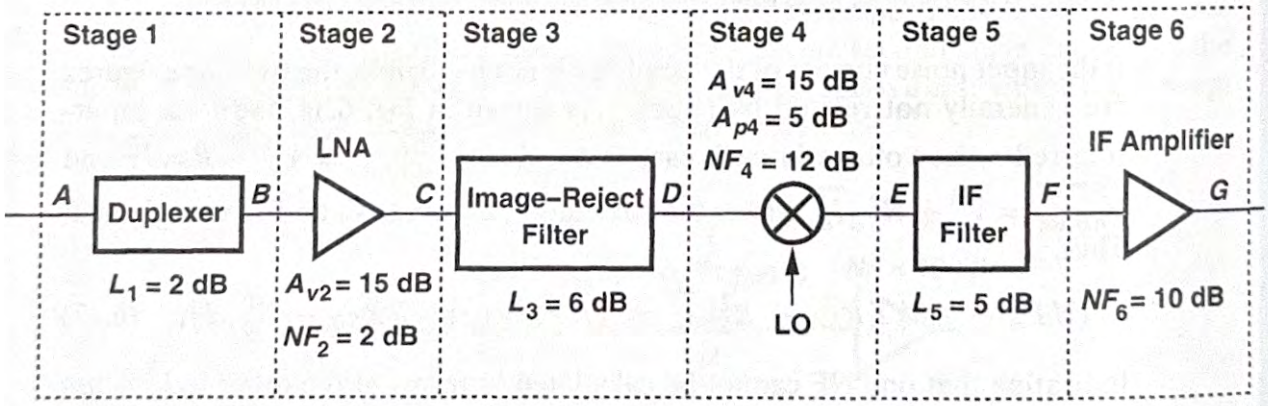


Figure 6.35 Calculation of noise figure in a cascade of stages.

It follows that the equivalent NF at the input of the LNA is given by $NF_B = NF_2 + (NF_C - 1)/A_{V2}^2 = 1.58 + 3.2 = 4.78 \approx 6.79$ dB. As a result, the overall noise figure is equal to $NF_{tot} = L_1|_{dB} + NF_B|_{dB} \approx 8.79$ dB. Note the substantial contribution of the stages following the LNA to the overall noise figure.

A powerful tool often used to illustrate the effect of each stage in a cascade upon the signal, the noise, and the intermodulation products is the "level diagram." Figure 6.36 shows the level diagram corresponding to the cascade of Fig. 6.35. Note that in addition to the parameters of each stage, cumulative quantities are indicated so as to represent the levels at the interface between consecutive stages.

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	A	Duplexer	B	LNA	C	Image-Reject Filter	D	Mixer	E	IF Filter	F	IF Amplifier
Stage Gain (dB)												
Voltage		−2		15		−6		15		−5		
Power		−2		15		−6		5				
Cumulative Voltage Gain (dB)				−2		13		7		22		17
Stage NF (dB)		2		2		6		12		5		10
Cumulative NF (dB)		8.79		6.79		20.1		14.1		15		10
Stage IP_3		+100 dBm		−12 dBm		+100 dBm		+5 dBm		1000 V_{rms}		700 mV_{rms}
Cumulative IP_3		−10.6 dBm		−12.6 dBm		+11 dBm		+5 dBm		22.1 V_{rms}		700 mV_{rms}

Figure 6.36 Level diagram corresponding to the cascade of Fig. 6.35.

In constructing a level diagram, several points must be observed. First, calculation of the cumulative gain proceeds from the *first* stage, whereas calculation of the cumulative noise figure and IP_3 begins from the *last* stage. Second, the IP_3 of passive filters is usually assumed to be a large number, for example, +100 dBm. Third, since the IF filter suppresses adjacent channel interferers to some extent, the cumulative IP_3 at the input of the IF filter is proportionally higher than the value predicted by the simple relationship derived in Chapter 2 for the IP_3 of cascaded stages. Fourth, because the impedance levels after the first mixer are not necessarily equal to 50 Ω, the IP_3 of the subsequent stages must be specified in volts or dBV. Also, if expressed in volts, the IP_3 of each stage is divided by the *loaded* voltage gain preceding that stage. Thus, the level diagram must indicate both the power gain (for NF calculations) and the voltage gain of each stage.

Using the stage IP_3 values shown in the diagram, we calculate the cumulative IP_3 of the cascade. Suppose the IF filter lowers the interferers by 30 dB while attenuating the desired channel by 5 dB. What is the equivalent IP_3 at point E? As shown in Fig. 6.37, since the interferers sensed by the IF amplifier are 30 dB lower than those at E, we have

$$\frac{1}{IP_{3,E}^2} = \frac{1}{IP_{3,\text{filt}}^2} + \frac{M^2}{IP_{3,\text{amp}}^2}, \tag{6.38}$$

where $M = 1/31.6 (= -30 \text{ dB})$. With the filter assumed highly linear,

$$IP_{3,E} = \frac{IP_{3,\text{amp}}}{M} \tag{6.39}$$

$$= 22.1 \text{ V}_{rms} \tag{6.40}$$

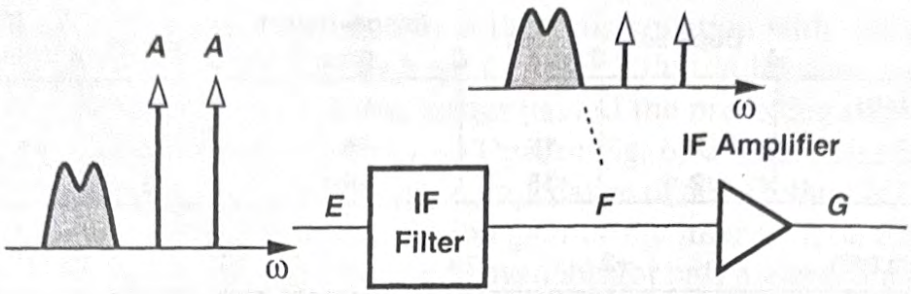


Figure 6.37 Suppression of adjacent channels by IF filter.

The cumulative IP_3 at point D is given by

$$\frac{1}{IP_{3,D}^2} = \frac{1}{IP_{3,\text{mix}}^2} + \frac{A_{v4}^2}{IP_{3,E}^2}, \tag{6.41}$$

and hence $IP_{3,D} \approx 398\ \text{mV}_{rms} \approx +5$ dBm. Note that $IP_{3,D}$ is dominated by the mixer nonlinearity. Similarly, $IP_{3,C} \approx +11$ dBm, $IP_{3,B} \approx -12.6$ dBm, and $IP_{3,A} \approx -10.6$ dBm.

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