
Murata – JMD Meeting

April 2, 2007



Agenda

- ❑ JMD today & the future
- ❑ Packaging technologies
 - Comparison to MLO
- ❑ JMD Supply chain
- ❑ JMD process & design roadmap
- ❑ Murata's interest in JMD (what is the expectation)
 - Short term
 - Long term
 - Other
- ❑ LTCC roadmap (Murata)
- ❑ Open discussion



Shrinking Form Factors

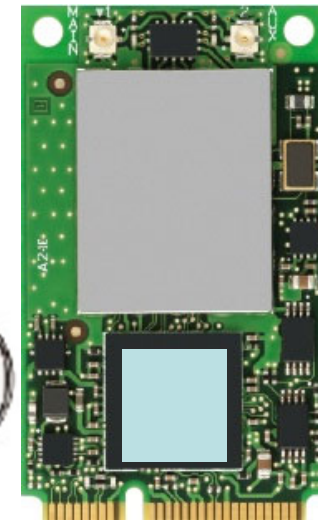
- ❑ Complexity Increasing
- ❑ Size Decreasing
- ❑ Mult-Standard Devices in Demand



- ❑ WLAN
- ❑ UMTS/EvDO
- ❑ WiMax
- ❑ Bluetooth
- ❑ UWB
- ❑ DVB/DMB/DARS
- ❑ GPS



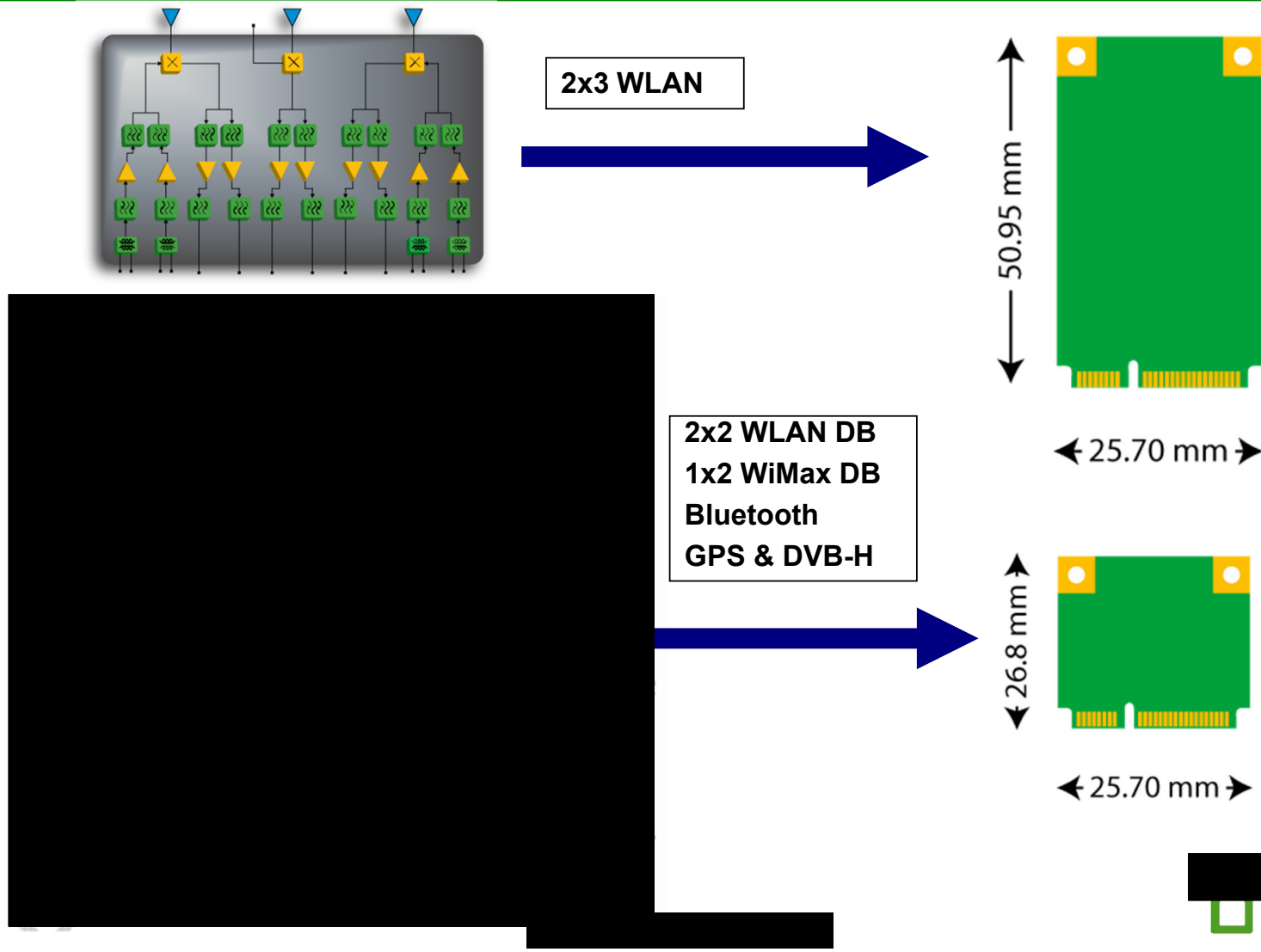
PCI Express Half Card



PCI Express Card



Much more in less space.....



Size & Performance Differentiation

□ Now.....

➤ Reduce size of current products:

- [REDACTED]



[REDACTED]

□ In the near future....

➤ Architectural efficiency

- Optimizing active & passive components
- Programmable/configurable FE's - multiband
- Higher Power out w/lower loss

➤ Integrated antenna

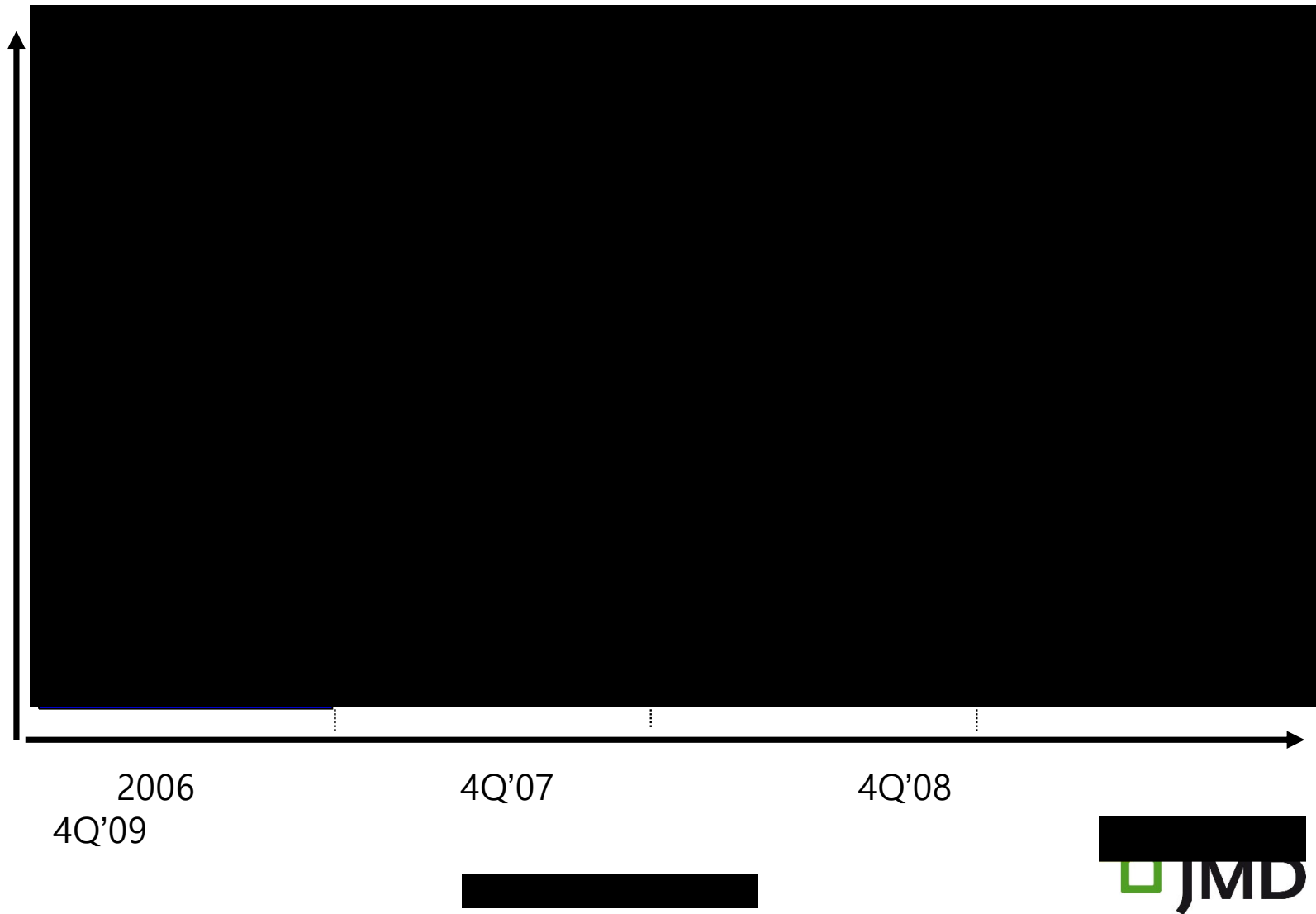
➤ “Card is module” – ½ card

- Fully integrated packaging – FEM, BB, TR

[REDACTED]



JMD today and the future



Packaging Technologies

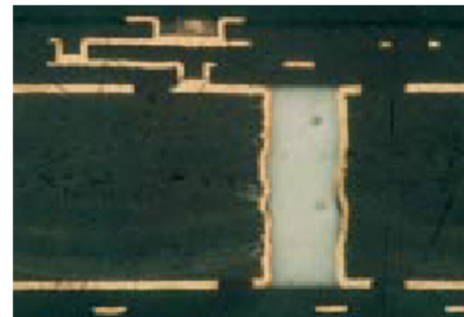
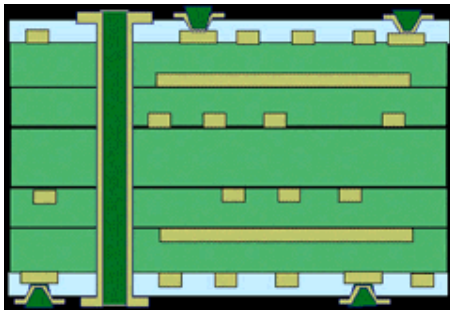


IBM Surface Laminar Circuitry (SLC) Technology

- Thin Film Sequential Build-up on Laminate
- Film/Liquid PhotoVia Process
- PTH & Microvia Plating

SLC Design Rules

Minimums (microns)	Typical	Available	Limited Availability
Line Width	75	75	50
Line Spacing	125	75	75
PhotoVia Diameter	125	125	100
Photo Via Land	300	250	150
PTH Diameter	350	250	200
PTH Land	600	450	350



Typical SLC Construction

Comparison to JMD MLO

- Original Sequential Build-up Technology
- Practiced widely in many substrate fabricators worldwide (BT/FR-4 Core)
- Mainly used for high density IC packaging, uses epoxy dielectric leading to low Qs

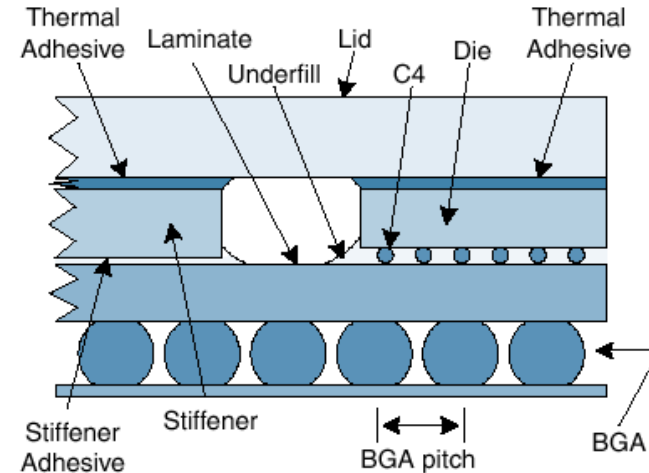
Courtesy: IBM Microelectronics



Endicott Interconnect HyberBGA™ Laminate for High Speed Applications

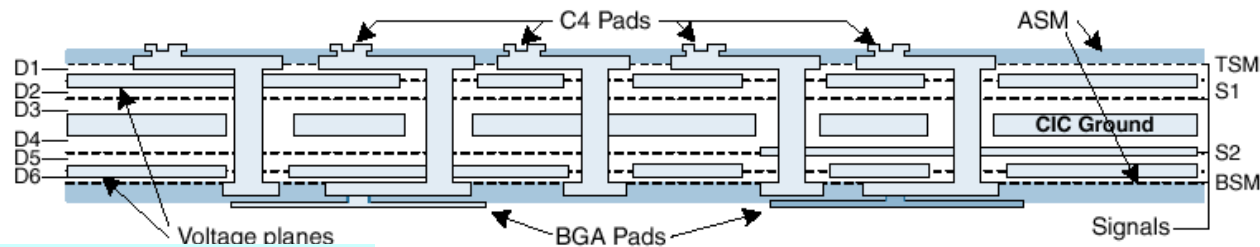
- ❑ Flipchip (C4) BGA Construction
- ❑ Copper-Invar-Copper (CIC) Core
- ❑ Low-k PTFE Laminate Layers
- ❑ 2 mil (50 μ m) Through Vias

	HyperBGA	Alumina Ceramic
Layers	9	17
Substrate Thickness (μ m)	500	2,550
Dielectric Constant	2.8	9.5
Nom. Line Width (μ m)	25	90
Nom. Line Height (μ m)	12	30
Nom. Impedance, Z0 (W)	54	37
Capacitance (pF/mm)	0.11	0.27
Delay (ps/mm)	5.6	11.5
Coupled Noise (mV/mm @1V/ns)	0.55	0.75



HyperBGA Package Cross-Section Schematic

HyperBGA Circuitized Laminate Schematic



* PTFE Substrate used by Anaren

Courtesy: Endicott Interconnect

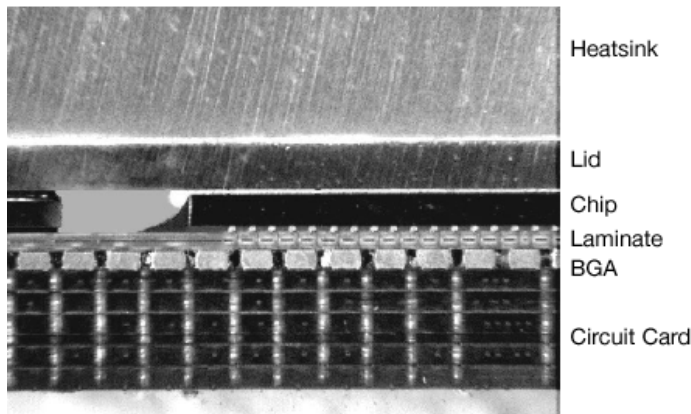


EI HyperBGA: Multilayer PTFE Substrate

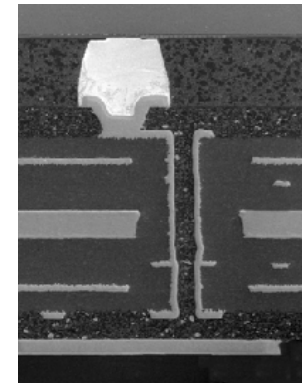


Courtesy:
Endicott Interconnect

HyperBGA Circuitized Laminate



Assembled HyperBGA Package Cross-Section



Solder Bump after Reflow on
HyperBGA Laminate

Comparison to JMD MLO

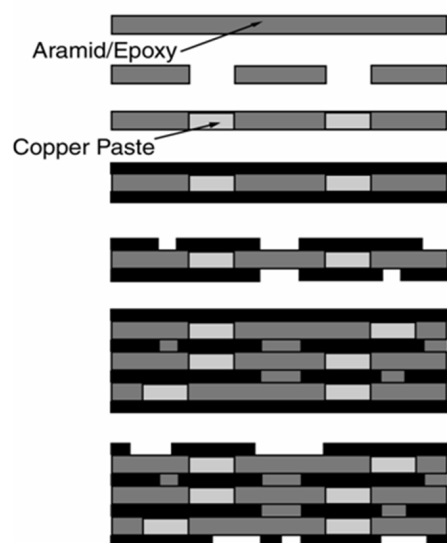
- Equivalent Q due to low loss PTFE
- Much lower component density due to low K of PTFE
- Much higher cost process due to the fusion bonding process



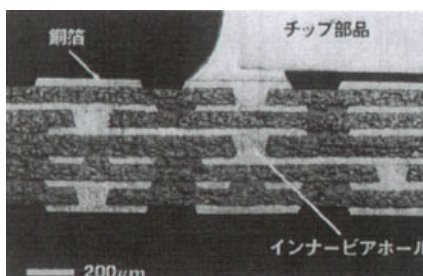
Matsushita ALIVH Substrate Technology (Any Layer Interstitial Via Hole)

ALIVH Technology (Matsushita)

(All Layer Internal Via Hole)



Process Flow



ALIVH Substrate with Conductive Epoxy Paste Fill

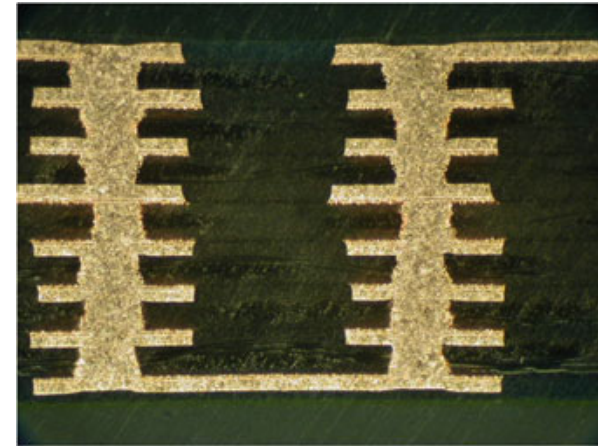
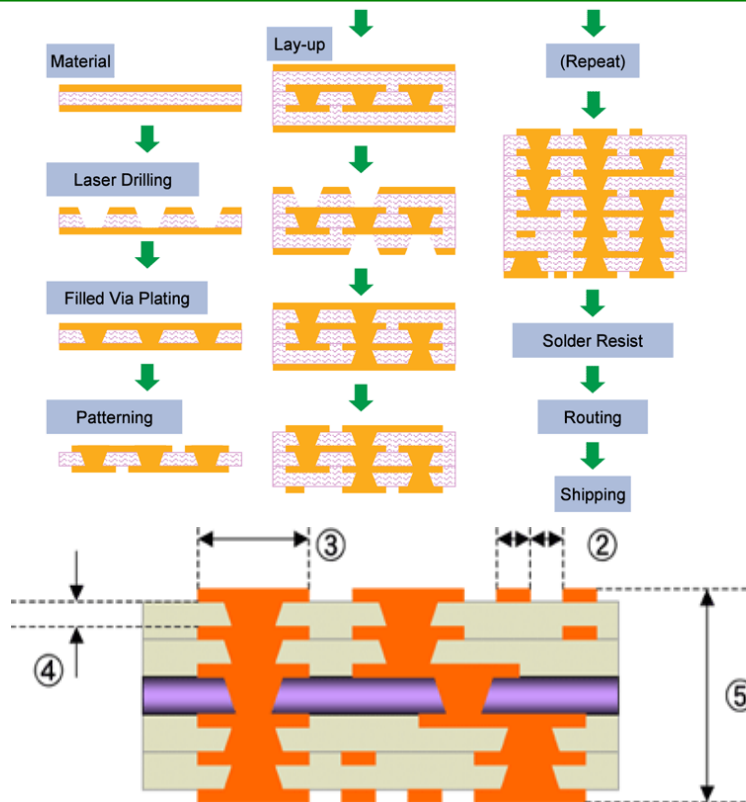
■ Properties

Item		ALIVH™	ALIVH™ G-Type
Base Material		Non-woven aramid fabric-epoxy resin	Glass-epoxy resin
Thickness of Board (standard) mm	8 Layer	0.75 to 0.95	0.60 to 1.00
Via Hole Size	μm	min. 150	
Via Pad Size	μm	min. 300	
Line/Space	μm	min. 60/70	
Dielectric Constant (1GHz)	—	3.7	4.6
Density	g/mL	1.4	2.0

Comparison to JMD MLO

- Much Lower Q due to higher loss thermoset dielectrics
- Paste filled vias leads to higher interconnect resistivity limiting high frequency performance
- Parallel process comparable in cost to MLO
- Layer to layer mis-registration seriously limits embedded component density and tolerance

Ibiden FVSS (Free Via Stacked-up Structure) Substrate Technology



Item		Spec
1.	layer count	>6 layers
2.	Line/Space	75/75 (50/50)um
3.	Land ø	150-275um
4.	HDI Dielectric thickness	60-80um
5.	Board thickness	>0.5mm

Comparison to JMD MLO

- Much Lower Q due to higher loss thermoset dielectrics
- Low K dielectrics used limits capacitor density
- Sequential build-up process leading to higher cost
- High Wiring Density Capabilit

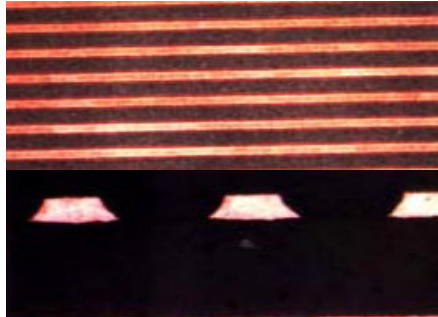


Limitations of Subtractive Process and Benefits of Additive Process

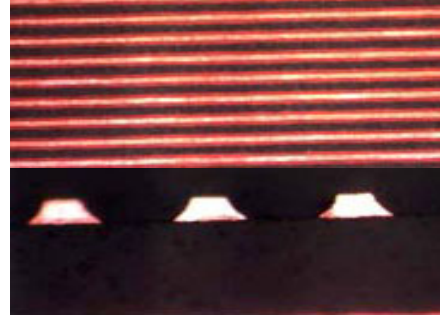
High Volume Production – Fine Line and Space Patterning

Subtractive Method

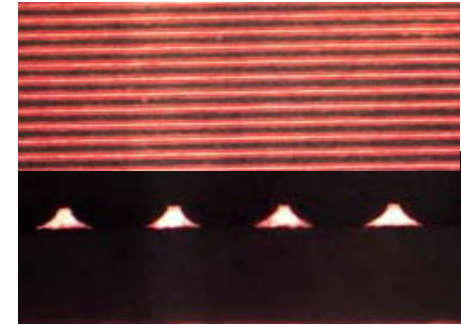
L/S=25/25 μ m



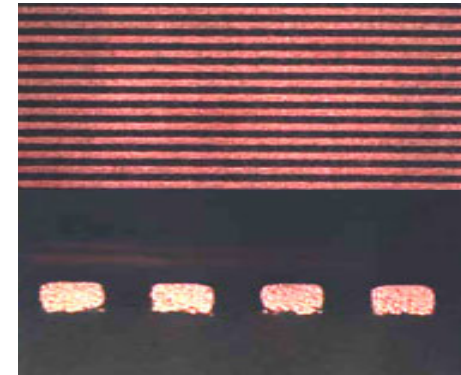
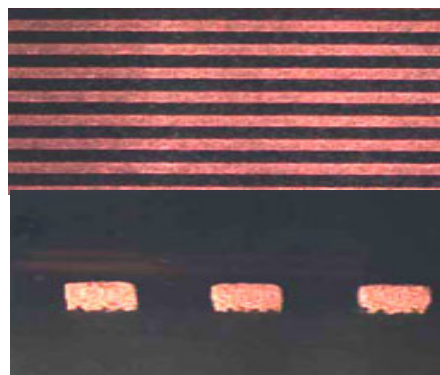
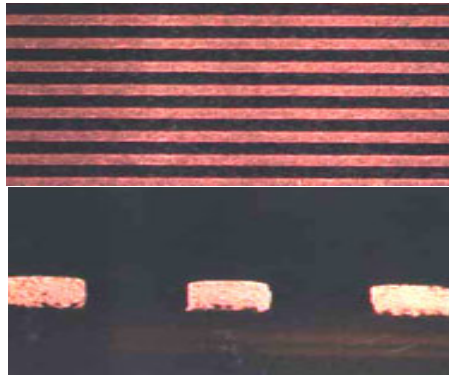
L/S=20/20 μ m



L/S=15/15 μ m



Semi-Additive Method



JMD MLO Technology can leverage Semi-Additive Process for much tighter embedded passive RF component tolerances in future designs

Source: Jun Sasaki, Toppan



Benchmarking of MLO & Other Module Substrate Technologies

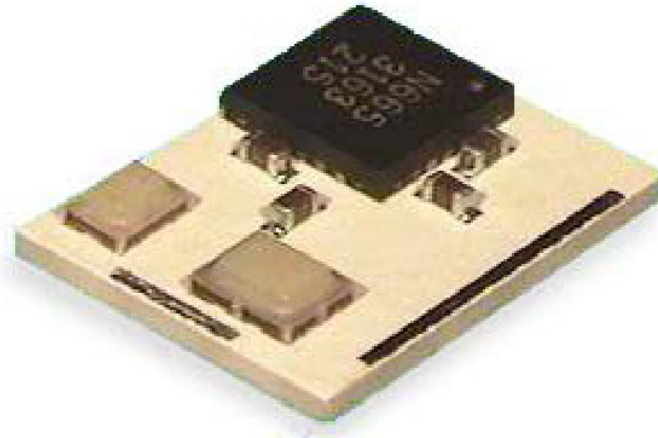
Factor	Measure	MLO	LTCC	PTFE/ Anaren	ALIV	BT/ FR-4	FVSS	Lead frame	SoIC
Inductor Q's			<70	>100	< 20	< 20	<20	Achievable on die <40	<40
Circuit density	devices/ cm ²		<200	Very limited routing.	400- 1000	<50	400- 1000	N/A	
Layers	#		16-18	6-8	6-8	6-12	6-12	N/A	
Thickness (Z)	mm		>0.85	.35	0.75- 1.00	.5	.5		
Size LxW	mm		12x12 mm or less	No Limit	No Limit	"No limit"	"No Limit"		
CTE	ppm/°C		5-7	13-16	14-16	16	16		
Process			Multilayer build-up w/hi temp firing			Std PCB			
Comment				Primarily IC packages & IPD's. Not used as substrate	Dk 3.7- 4.6			Low cost single die solution	



Embedded Passives (L and C) in LTCC RF Modules (TDK, Epcos, Murata, Hitachi Metals and others)

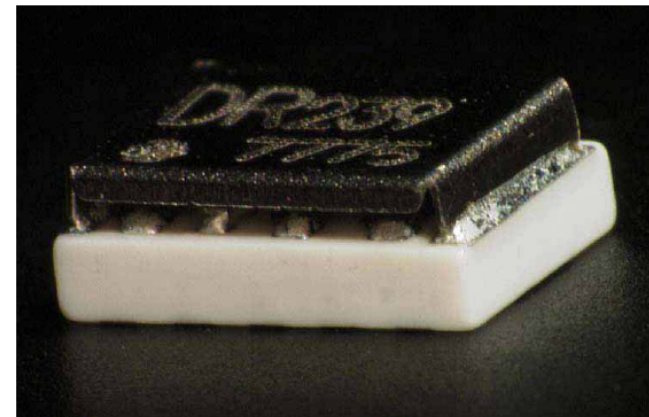
❑ TDK GSM/WCDMA Front End Module

- 15-17 Metal Layer LTCC Substrate
- >25 L and C Embedded in Substrate for Filters, Duplexers, Matching



❑ Hitachi Metals Antenna Switch Module

- 17 metal layer LTCC substrate
- Integrates 50 C and L



LTCC Companies in Japan Looking to Migrate to Organic Substrates

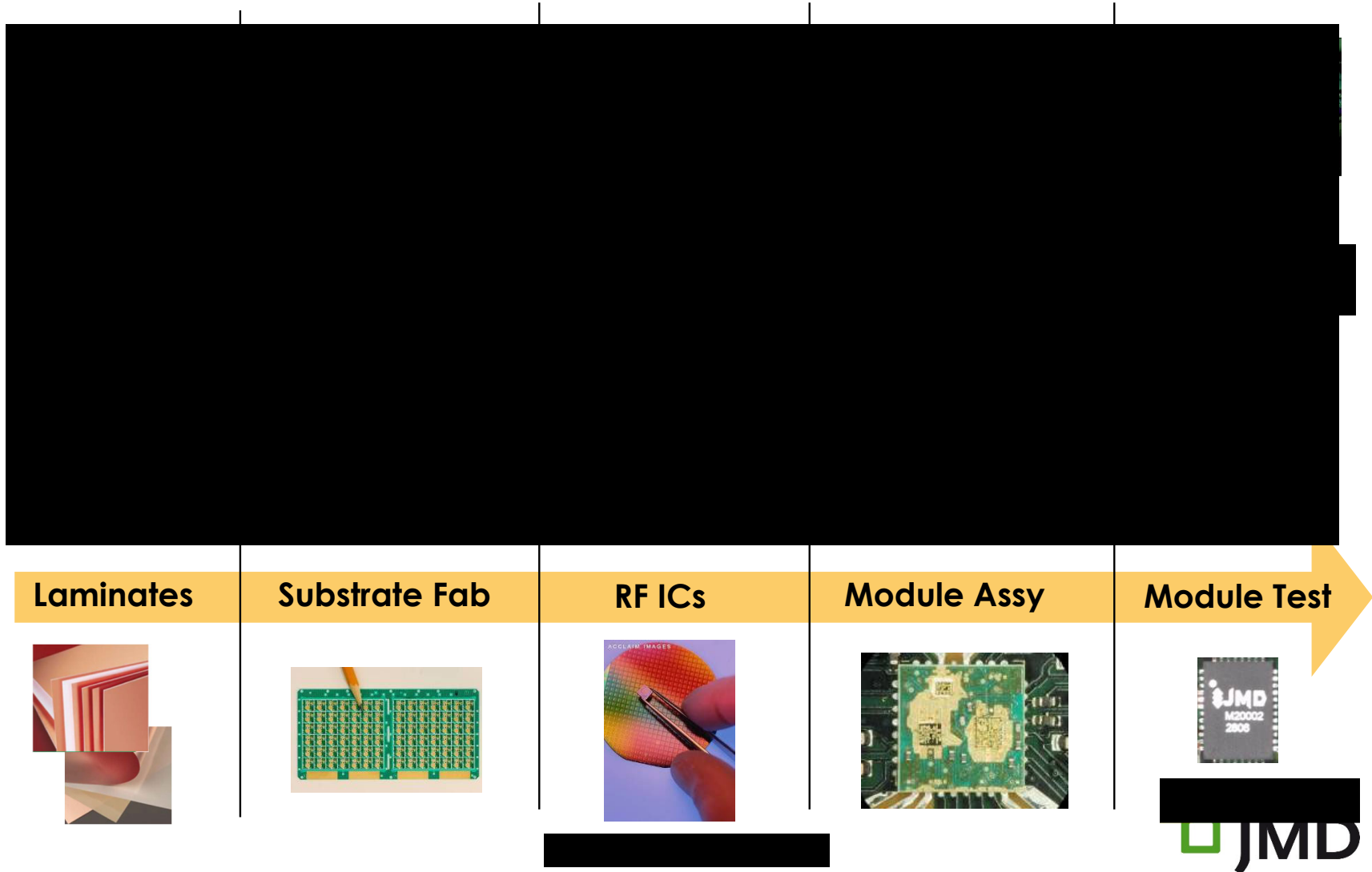
1. Kyocera acquired IBM-Yasu Organic Build-up Substrate Technology
Kyocera setting up new factory in Japan for Organic HDI Substrates
2. Murata developing organic substrate based modules since 2002



JMD Supply Chain



JMD Supply Chain - Overview



Process & Design Roadmap



JMD and MLOSM

Displaces Passive RF Components

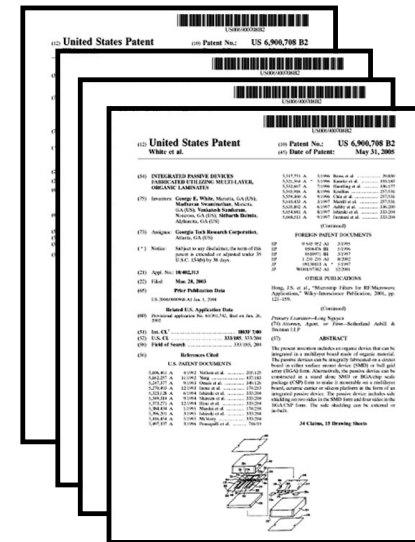
- [REDACTED]
- Goal in 2009 to eliminate modules completely with fully integrated cards

Competitive Advantage

- Simplicity in design
 - Achieving component density with 6-8 metal layers
- 25% - 50% size reduction compared to discretes and current modules
- C_{TE} matching with PCB prevents cracking of modules and devices when size increases or thickness decreases

Patented Multi-Layer Organic Processes

- 26 Issued/pending patents covering innovative fabrication techniques, component geometries & MLO process technology



JMD Design and Differentiation

□ Better Performance

- [Redacted]
- [Redacted]
- [Redacted]
- [Redacted]

□ Smaller Size and lower thickness

- Photolithography enables smaller line geometries
- As shown JMD will engage in sub 25um lines and spacing for all products by 2008-2009. Currently JMD uses 50um lines and spacing.

□ Scalability

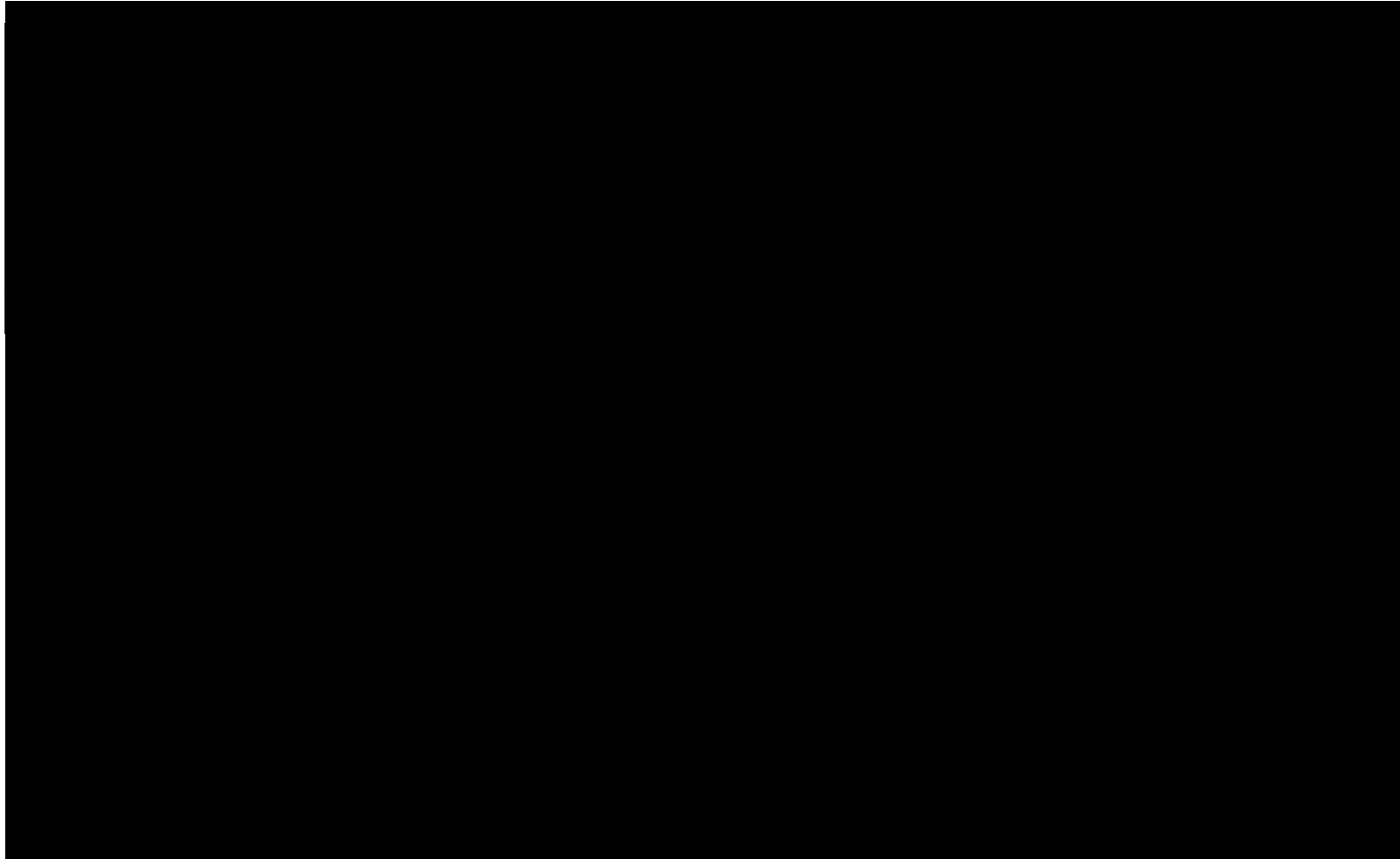
- Design libraries are used successfully for different products enabling scalability

□ Time to Market

- Standard design library and DFM reduces DCT
- Fewer layers simplifies design and gives excellent model-to-hardware



Process Flow

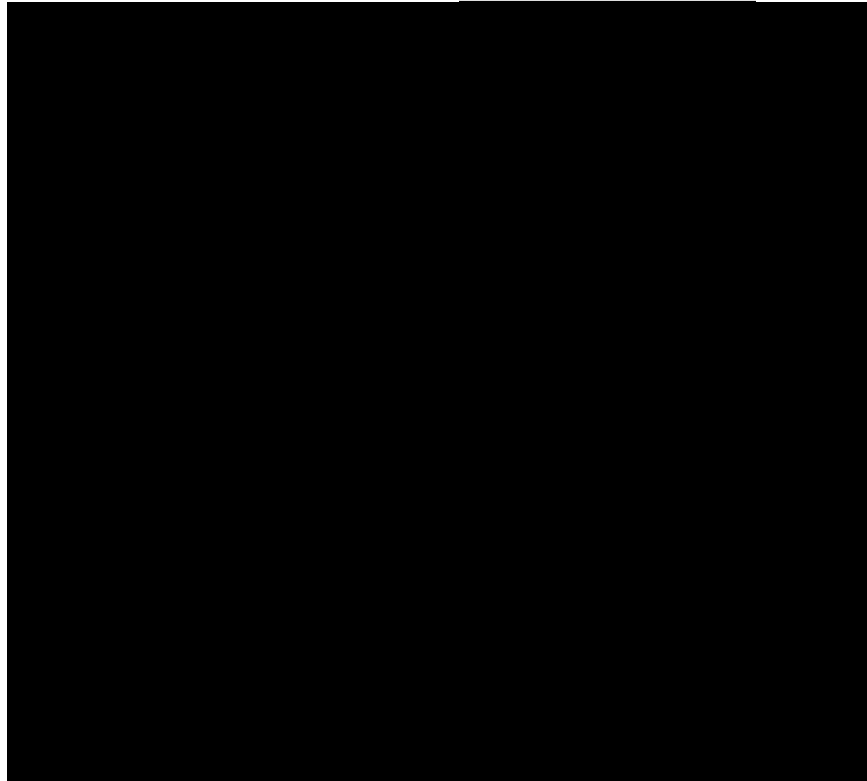


 JMD

Drive towards MultiBand



Primary Goal for Design and Process: Multi Radio Front End



☐ Performance

- [Redacted]
- [Redacted]

☐ Integration Challenges

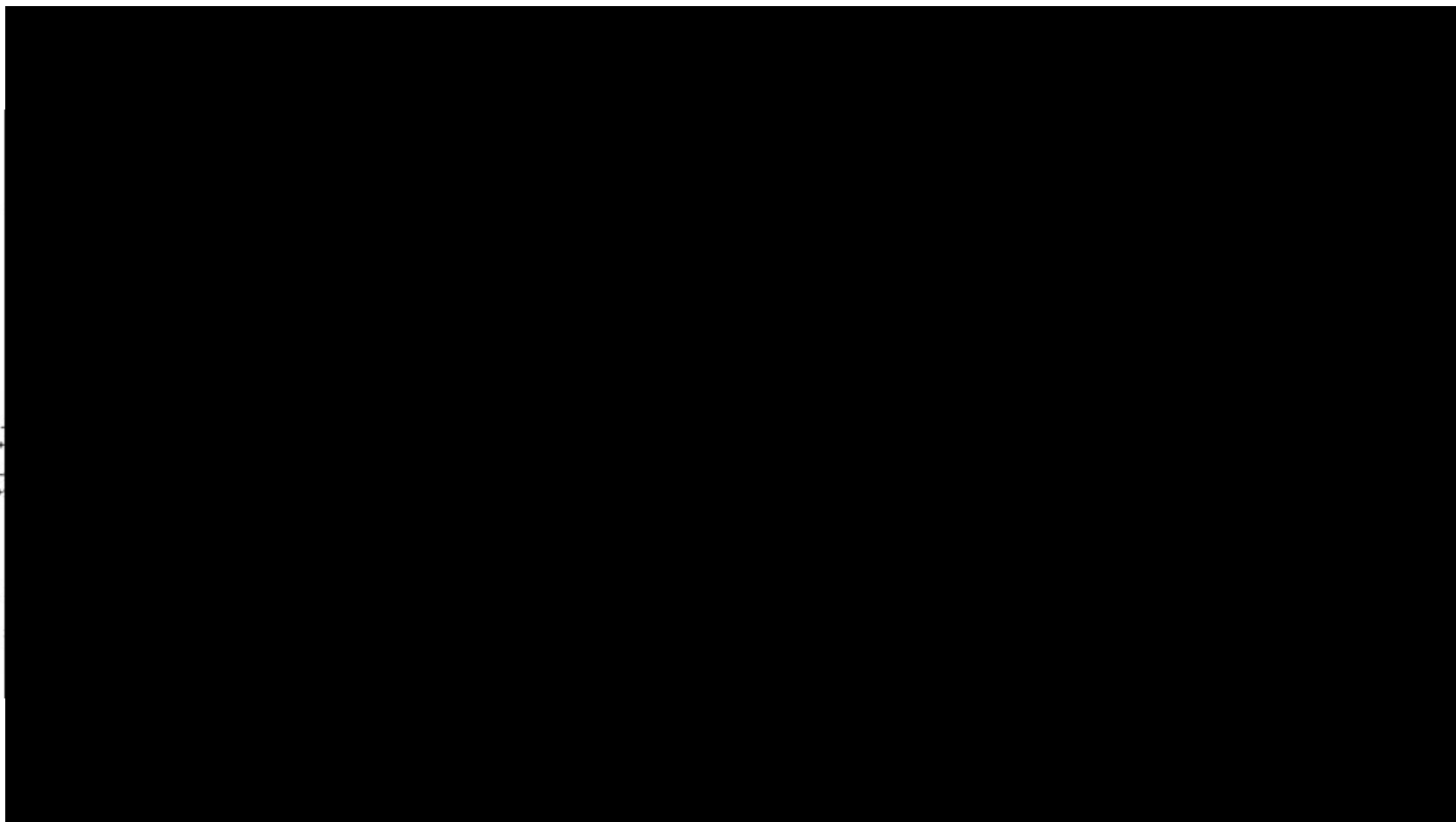
- [Redacted]
- Versatile packaging solution is imperative

☐ Further Integration

- [Redacted]
- [Redacted]

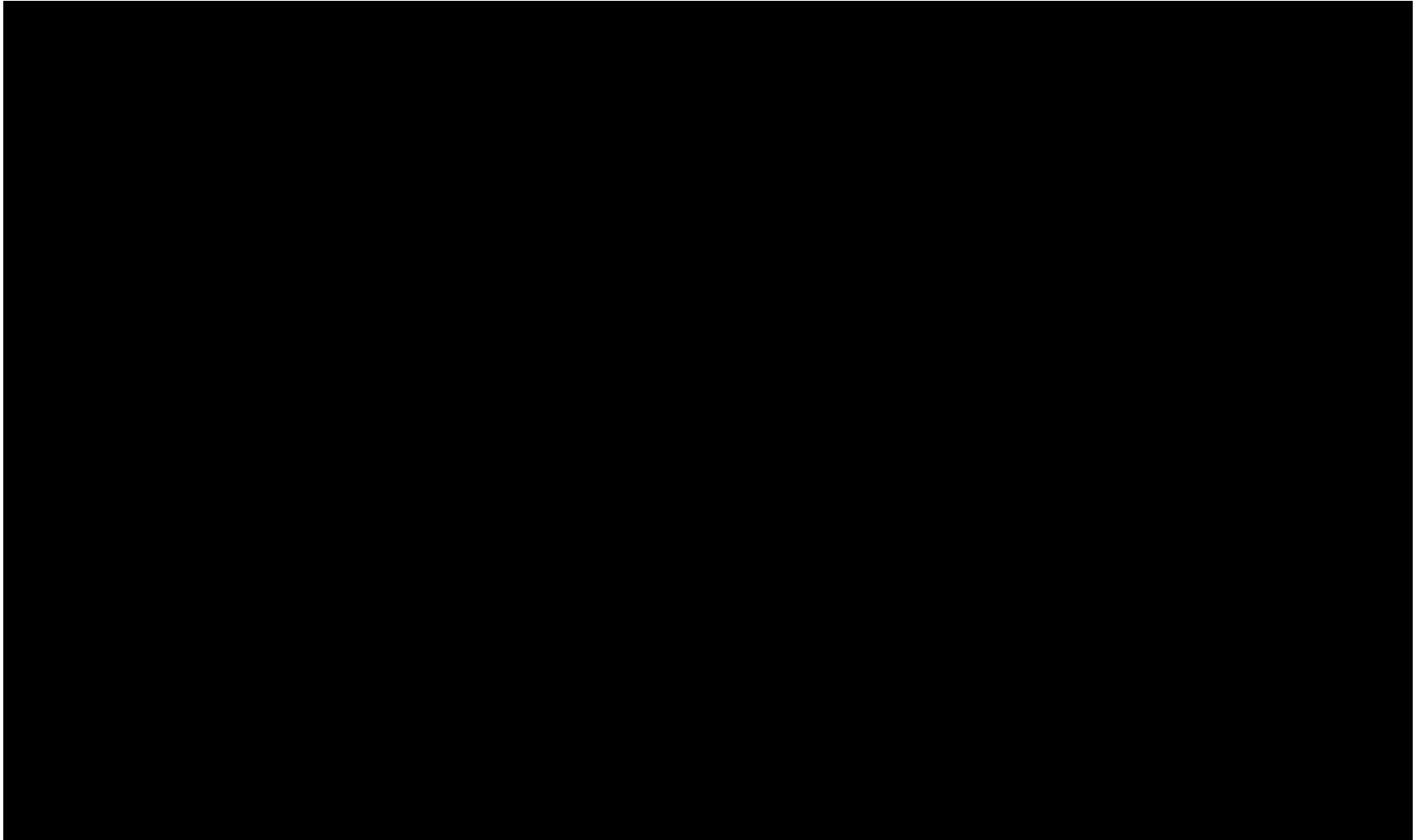


Building Blocks toward Multiband Mercury v1.1 (2x2)



 JMD

MCT Substrate Supplier Qualification and Development



Intellectual Property Update

Title	Filing Status	Key Claims
Packaged Tunable MEMS on Organic PCBs -JMD	U.S. Provisional	MEMs capacitors and switches on organic materials
System and method for integrated antenna structures in MLO PCB Devices) - JMD	U.S. Provisional	Integrated antennas in JMD Substrate. Embodiments include flex antennae, and antennas on sides of devices; Key for miniaturization in laptops, handhelds etc
Methods for fabricating 3D all organic interconnect structures (GT)	U.S. Non Provisional And PCT – All Claims Allowed	All LCP stackup with any layer via interconnections. Key to realizing smallest form factors and highest density. Similar to LTCC fab techniques. Very important to suppliers who have LTCC and looking to leverage organics
Filters with Inductors on Multiple Levels and Methods of Fabrication	Disclosure being finalized; Will file as a U.S. Non Provisional	Design centric patent that discloses fabrication of filters using multiple layers of low loss dielectrics
Methods and Apparatuses for High Performing Multilayer Inductor	U.S. Non-provisional (11/426,923)	Design centric patent, with process know how on multilayering of inductor structures to achieve high Q factors. Q factors in excess of 300 have been demonstrated
Low Cost, Low Noise Integrated Amp, Switch and LNA	Disclosure being finalized. Expect to file before 2Q07	IC design application that combines switch and LNA on single IC
Systems, Methods, and Apparatuses for Integration Using Package Stacking for Global Universal Radio Units	U.S. Provisional	Multiple radios in a module; GURU concept
Various Methods for Tuning Filter Performance	Disclosure being rewritten to encompass new learning; Expect to file by 3Q07	In-situ tuning of filter elements to enhance device and substrate yield



Intellectual Property Update

Title	Filing Status	Key Claims
Integrated passive devices fabricated utilizing multilayer organic laminates (GT)	Issued U.S. patents (6,900,708 and 7,068,124) Filed in EU, Japan and Korea	Inductors and capacitors on any organic material connected by micro-vias in substrates or components
Stand alone organic based passive devices (GT)	Issued U.S. patent (6,987,307) Filed in EU, Japan and Korea	Inductors in stand-alone components or in substrates or components
Methods for fabricating 3D all organic interconnect structures (GT)	Utility patent filed (10/402,315). Filed in EU, Japan and Korea. Office action pending.	All LCP stackup with any interconnects
Liquid crystalline polymer and multilayer polymer based RF components for multi-band ...	PCT - All Claims Allowed	Baluns, diplexers, couplers, etc. in multi-layer organics
Heterogeneous organic laminate stack up for HF applications (JMD)	U.S. Non-provisional (60/586,200)	Cavities, antennas, resistors and overmolding
Methods for fabricating three-dimensional all organic interconnect structures (JMD)	U.S. Non-provisional (10/402,315) PCT Non-provisional	Specific JMD stackups such as 246
Multi-band RF transceiver with passive re-use in organic substrates (JMD)	U.S. Non-provisional	Multi-frequency operation of VCOs, PAs, LNAs etc. in organic packages
Low-profile wide-band transformer balun in MLO for multi-band applications (JMD)	U.S. Non-provisional	JMD specific device
High Q Inductors (JMD)	U.S. Non-provisional	Fabrication of inductors with $Q_s > 100$ in organic materials
MEMs on Polymer material (JMD)	U.S. Provisional	MEMs capacitors and switches on organic materials



Murata's interest in JMD



Murata – JMD Synergies

□ Murata:

- Manufacturing scope
- Production process
- Materials science
- Market presence
- Financial strength

□ JMD:

- Leading packaging technology
- Packaging IP
- RF Design capability
- Connection to PRC



□ Open Discussion - Next steps

[REDACTED]

[REDACTED]

[REDACTED]
JMD

SoP vs SoC

- ❑ Single chip silicon solutions are mature for baseband and transceiver components
- ❑ Increase in complexity readily met (albeit at considerable increase in design cost) by new nodes in CMOS
- ❑ Single chip RF solutions are performance limited
- ❑ SoP approach for FEMs has legs

Hans Stork, CTO of Silicon Technology Development:

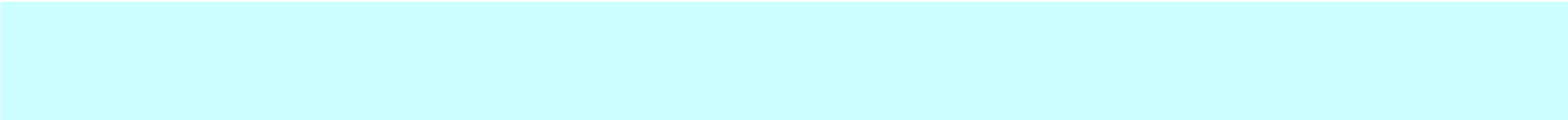
"... I am surprised at how important packaging is becoming in new IC markets. The need for chip-package co-design is growing rapidly. In the RF space especially we are challenged by the fact that the space required for an inductor (on a transceiver die for example) could be used instead for over 1 million transistors. Deep sub micron silicon is going to be an excellent solution for digital and low power analog and a bad solution for high powered analog and RF."

Behrooz Abdi - SVP, GM CDMA Technology, Qualcomm:

When asked by the moderator what areas he would advise semiconductor start-ups to focus on, he said:

"...RF miniaturization including antennas and switches."





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