

THIRD-PARTY SUBMISSION UNDER 37 CFR 1.290	Application Number	14748623

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1	7808434		2010-10-05	George White		
2	6987307		2006-01-17	George White		
3	8345433		2013-01-01	George White		
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NON-PATENT PUBLICATIONS (e.g., journal article, Office action)						

THIRD-PARTY SUBMISSION UNDER 37 CFR 1.290	Application Number	14748623

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STATEMENTS
The party making the submission is not an individual who has a duty to disclose information with respect to the above-identified application under 37 CFR 1.56. This submission complies with the requirements of 35 U.S.C. 122(e) and 37 CFR 1.290. ☐ The fee set forth in 37 CFR 1.290(f) has been submitted herewith. ☒ The fee set forth in 37 CFR 1.290(f) is not required because this submission lists three or fewer total items and, to the knowledge of the person signing the statement after making reasonable inquiry, this submission is the first and the only submission under 35 U.S.C 122(e) filed in the above-identified application by the party making the submission or by a party in privity with the party. ☐ This resubmission is being made responsive to a notification of non-compliance issued for an earlier filed third-party submission. The corrections in this resubmission are limited to addressing the non-compliance. As such, the party making this resubmission: (1) requests that the Office apply the previously-paid fee set forth in 37 CFR 1.290(f), or (2) states that no fee is required to accompany this resubmission as the undersigned is again making the fee exemption statement set forth in 37 CFR 1.290(g).

THIRD-PARTY SUBMISSION UNDER 37 CFR 1.290	Application Number	14748623

Signature	/Richard M. Moose/			
Name/Print	RICHARD M. MOOSE		Registration Number (if applicable)	31 226
Examiner Signature			Date Considered	
*EXAMINER: Signature indicates all documents listed above have been considered,except for citations through which a line is drawn. Draw line through citation if not considered. Include a copy of this form with next communication to applicant. 1. If known, enter kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16. See MPEP 901.04(a). 2. Enter the country or patent office that issued the document, by two-letter code under WIPO standard ST.3. See MPEP 1851. 3. For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 4. If known, enter the kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 . See MPEP 901.04(a). 5. Check mark indicates translation attached. 6. Check mark indicates evidence of publication attached.				

THIRD-PARTY SUBMISSION UNDER 37 CFR 1.290 CONCISE DESCRIPTION OF RELEVANCE		
Application Number	14748623	
U.S. PATENTS		
Cite No	Patent Number	Concise Description of Relevance
1	8345433	See Attached
2	6987307	See Attached
3	7808434	See Attached

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U.S. PATENT APPLICATION PUBLICATION

Cite No	Publication Number	Concise Description of Relevance

FOREIGN PATENT DOCUMENTS

CiteNo	Foreign Document Number	Concise Description of Relevance

NON-PATENT PUBLICATIONS

Cite No	Reference	Concise Description of Relevance

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Document 1

Patent No.: US Patent 7,808,434
Inventor: White, et al.
Application No.: 11/836,670
Filed: August 9, 2007
Issue Date: October 5, 2010

Concise Description:

Document 1 was published prior to the earliest possible priority date of February 15, 2013 for the subject Application USSN 14/748,623.

The subject Application USSN 14/748,623 is entitled "LAMINATED CIRCUIT SUBSTRATE." It relates in pertinent part to laminated circuits formed of thermoplastic resin layers laminated with conductor patterns and with selected internal surfaces subjected to roughening processes (etching), to form laminated capacitor and/or inductor circuit elements. See, for example, application Abstract, and paragraphs [0068] and [0074] in pertinent part, as follows (emphasis added):

Abstract

Sheets are laminated on each other and pressure bonded with fixtures from upper and lower directions of a lamination direction while being heated to produce **a laminated circuit substrate including therein a capacitor and a coil**. The capacitor is defined by a first conductor pattern and a second conductor pattern that face each other across thermoplastic resin layers. In the laminated circuit substrate, the first conductor pattern includes a first principal surface, the second conductor pattern includes a second principal surface, the first principal surface faces the second conductor pattern, the second principal surface faces the first conductor pattern, and the first principal surface and the second principal surface are subject to a roughening process.

...

[0068] Subsequently, as shown in FIG. 3B, the metal films 31 to 35 of the sheets 11 to 15 are **patterned mainly by etching**. As a result, the mounting lands 121, 122, 131, 132, and 133, the external connection terminals 31A and 31B, the **first conductor pattern 32A and the second conductor pattern 33A that define the capacitor C1**, and **conductor patterns 33B, 33C, 33D, 33E, 34A, 34B, 34C, and 34D that define the coil L1** are provided.

...

[0074] However, in the laminated circuit substrate 101, **the roughening process is performed to the first principal surface** that faces the second conductor pattern 33A in the first conductor pattern 32A (see FIG. 5A). Moreover, in the laminated circuit substrate 101, **the roughening process is performed also to the second principal surface 92** that faces the first conductor pattern 32A in the second conductor pattern 33A (see FIG. 5A). **The roughening process includes etching, for example.**

The subject Application USSN 14/748,623 makes seventeen references to “roughening process” but the only explanatory sentence is the one above that: “The roughening process includes etching, for example.” Then, dependent claim 17 states in pertinent part that “the roughened surfaces ... are etched surfaces.”

Sole pending independent claim 2 as published of the subject Application USSN 14/748,623 recites in pertinent part:

2. A laminated circuit substrate comprising:
 - a plurality of thermoplastic resin layers laminated on top of each other;
 - a first conductor pattern including a first principal surface;
 - and
 - a second conductor pattern including a second principal surface; wherein the first conductor pattern and the second conductor pattern face each other across at least one layer of the plurality of thermoplastic resin layers;

the first principal surface and the second principal surface are roughened surfaces.

FIG. 38

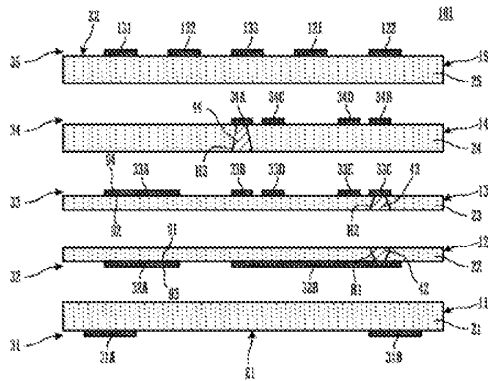
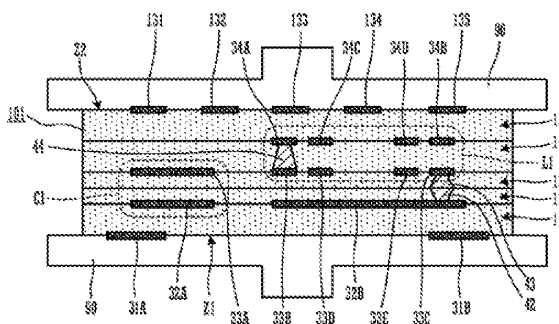


FIG. 4A



10. The laminated circuit substrate according to claim 2, wherein the first conductor pattern and the second conductor pattern define an inductor.

12. The laminated circuit substrate according to claim 2, wherein an inductor and a capacitor are defined by the first and second conductor and other conductors.

13. The laminated circuit substrate according to claim 12, wherein the coil is defined by linear conductor patterns and a via hole.

17. The laminated circuit substrate according to claim 2, wherein the roughened surfaces of the first principal surface and the second principal surface are etched surfaces.

Document 1 (D1) relates to integrated structures in multilayer organic-based printed circuit devices and is therefore concerned with certain aspects of the subject Application USSN 14/748,623.

For example, D1 discloses how coupling may be achieved using in part a resonator formed of inductor and capacitor elements in a multilayer device. In particular, multilayer thermoplastic substrates may be formed using in part selectively etched layers, to form included elements such as inductors and/or capacitors and vias. See, D1, Abstract in pertinent part; emphasis added:

Abstract

Embodiments of the invention may provide for a variety of antennae structures, including the following: ... e) antennae structures printed directly on the dielectric layers adjacent to thin film wiring and embedded passive elements such as filters, diplexers and couplers.

See, also, D1, Col 3, lines 10-18, in pertinent part as follows (emphasis added):

FIG. 1 illustrates a multilayer organic stackup that may be utilized with the antennae structures, according to example embodiments of the invention.

...

FIG. 2B illustrates a front view of the multilayer substrate of FIG. 2A, according to an example embodiment of the invention.

...

See, also, D1, Col 4, line 37 – Col. 6, line 7, in pertinent part as follows (emphasis added):

With reference to FIG. 1, the **multilayer organic stackup** in accordance with an embodiment of the invention **may include inductors 12 and 14**, which are meandering inductors formed close to each other on an organic dielectric layer 36 (which can be a thin laminate such as LCP or PPE, but is not limited to these) and may be configured as either a shorted hybrid CPW-stripline (where lines that form meandering inductors 12 and 14 are connected to a coplanar ground, that is, in-built shielding 30), or a stripline in the presence of coplanar in-built shielding 30 and **additional grounds in metallization/conductive layers 48 and 50 that are connected to the plated through holes 32 (e.g., vias)** and/or external shield electrodes 34.

Since these inductors 12 and 14 are very close to each other, the magnetic coupling between these resulting filters can increase the pass bandwidth, thereby decreasing its performance. However, **an inter-resonator parallel plate coupling capacitor 24**, (with or without the coplanar in-built shielding 30) **formed using two disconnected metal plates (one plate formed using patterning conductive layer 38 and the other plate formed using patterned conductive layer 40) and shown as capacitor plates 24a, 24b is provided**. The capacitor plates 24a, 24b may sandwich the first organic dielectric layer 36 in such a manner that each plate of the inter-resonator coupling capacitor electrode may be connected to separate resonators which helps compensate the effect of the magnetic coupling and helps make very compact filters. ... Additionally, **capacitor 24 in parallel with the mutual inductance equivalent** gives a pole in the lower band or upper band.

The bottom plate formed by the conductive layer 40 connects to inductor 12 using one or more microvias in the organic dielectric layer 36, such as the vias 44 with pads 46 for landing and capturing the via. First and second metallization/conductive layers 48, 50, which may

operate at least in part as shield electrodes, are formed respectively on the organic layers 52, 54, **where the organic layers 52 and 54 are disposed so as to sandwich the organic dielectric layer 36 there between.** A **first resonator 60 formed by inductor 12 and capacitor 16** and a **second resonator 62 formed by inductor 14 and capacitor 18** are electrically coupled to each other through the parallel plate capacitor 24, whereby an inter-resonator coupling is effected in combination with said magnetic coupling and electric coupling.

It will be appreciated that where the inductors do not provide the needed capacitance in the desired length, the inductors 12, 14 can be connected in similar fashion as the capacitor 24 to separate grounded/shunted parallel plates 16a and 18a, respectively, of capacitors 16 and 18, respectively, using the same first organic dielectric layer 36 as the sandwiched dielectric, which then together form the resonator pairs 60, 62.

...

The first organic dielectric layer 36 can comprise single side copper LCP laminate or the like, such as PPE, N6000, epoxy based N4000-13, or any other suitable low loss dielectric. In the multilayer stackup of FIG. 1, an initial step to making a connection between devices using vias 44 is done by drilling through holes (as small in diameters as the thickness of the dielectric used) through the LCP layer (or any other appropriate organic dielectric) and copper layer. Then both sides of LCP copper laminate may metallized, such as by electroless or vacuum deposited copper. Copper is then electroplated on both sides of laminate to form the metallized patterns 38, 40 on the organic dielectric layer 36. **The copper is then printed and etched to define the desired components.**

In FIG. 1, the dielectric layers 52, 54 can be laminate LCP or appropriate dielectric with generally larger thickness than the first substrate and aluminum, copper, Molybdenum metal (for high power applications) on both sides of filter to a given thickness to encapsulate components. **All metals are may be electroplated, etched, and patterned** on top and bottom of the device to leave space for signal input and output.

See, also, D1, Col 7 line 39 - Col. 8 line 11, in pertinent part as follows (emphasis added):

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During fabrication of the multilayer stackup 200, the antennae structures 202 may be fabricated using standard fabrication techniques known to those of ordinary skill in the art, **including print and etch techniques**.

...

FIG. 2B illustrates a front view of the multilayer substrate 200, according to an example embodiment of the invention. As more particularly shown in FIG. 2B, the **multilayer substrate 200 may include a plurality of organic layers such as organic layers 205a-e. The organic layers 205a-e may be formed of thermoplastic** or thermoset materials, including Rogers 4350 or Rogers 4003, liquid crystalline polymer (LCP), polyphenyl ether (PPE), hydrocarbon, Teflon, epoxy, polyamide, polyimide, and acrylate. ...

D1 exemplary arrangements per Figures 1 and 2B thereof, appear as follows:

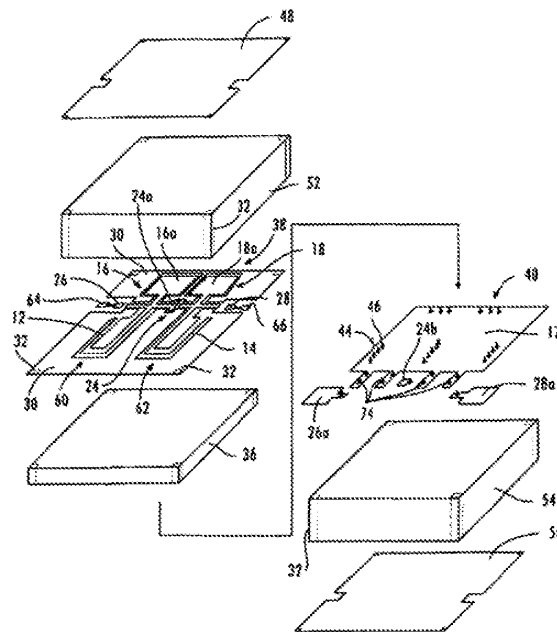


FIG. 1

Document 2

Patent No.: US Patent 6,987,307
Inventor: White, et al.
Application No.: 10/405,024
Filed: March 28, 2003
Issue Date: January 17, 2006

Concise Description:

Document 2 was published prior to the earliest possible priority date of February 15, 2013 for the subject Application USSN 14/748,623.

The subject Application USSN 14/748,623 is entitled "LAMINATED CIRCUIT SUBSTRATE." It relates in pertinent part to laminated circuits formed of thermoplastic resin layers laminated with conductor patterns and with selected internal surfaces subjected to roughening processes (etching), to form laminated capacitor and/or inductor circuit elements. See, for example, application Abstract, and paragraphs [0068] and [0074] in pertinent part, as follows (emphasis added):

Abstract

Sheets are laminated on each other and pressure bonded with fixtures from upper and lower directions of a lamination direction while being heated to produce **a laminated circuit substrate including therein a capacitor and a coil**. The capacitor is defined by a first conductor pattern and a second conductor pattern that face each other across thermoplastic resin layers. In the laminated circuit substrate, the first conductor pattern includes a first principal surface, the second conductor pattern includes a second principal surface, the first principal surface faces the second conductor pattern, the second principal surface faces the first conductor pattern, and the first principal surface and the second principal surface are subject to a roughening process.

...

[0068] Subsequently, as shown in FIG. 3B, the metal films 31 to 35 of the sheets 11 to 15 are **patterned mainly by etching**. As a result, the mounting lands 121, 122, 131, 132, and 133, the external connection terminals 31A and 31B, the **first conductor pattern 32A and the second conductor pattern 33A that define the capacitor C1**, and **conductor patterns 33B, 33C, 33D, 33E, 34A, 34B, 34C, and 34D that define the coil L1** are provided.

...

[0074] However, in the laminated circuit substrate 101, **the roughening process is performed to the first principal surface** that faces the second conductor pattern 33A in the first conductor pattern 32A (see FIG. 5A). Moreover, in the laminated circuit substrate 101, **the roughening process is performed also to the second principal surface 92** that faces the first conductor pattern 32A in the second conductor pattern 33A (see FIG. 5A). **The roughening process includes etching, for example.**

The subject Application USSN 14/748,623 makes seventeen references to “roughening process” but the only explanatory sentence is the one above that: “The roughening process includes etching, for example.” Then, dependent claim 17 states in pertinent part that “the roughened surfaces ... are etched surfaces.”

Sole pending independent claim 2 as published of the subject Application USSN 14/748,623 recites in pertinent part:

2. A laminated circuit substrate comprising:
 - a plurality of thermoplastic resin layers laminated on top of each other;
 - a first conductor pattern including a first principal surface;
 - and
 - a second conductor pattern including a second principal surface; wherein the first conductor pattern and the second conductor pattern face each other across at least one layer of the plurality of thermoplastic resin layers;

the first principal surface and the second principal surface are roughened surfaces.

FIG. 38

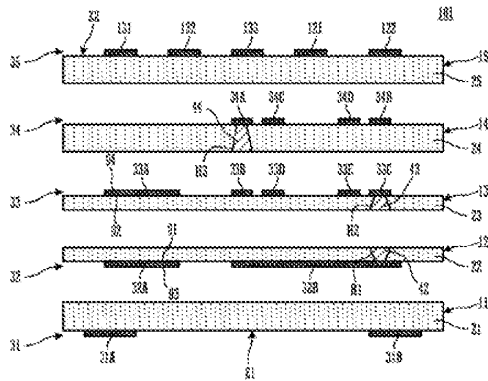
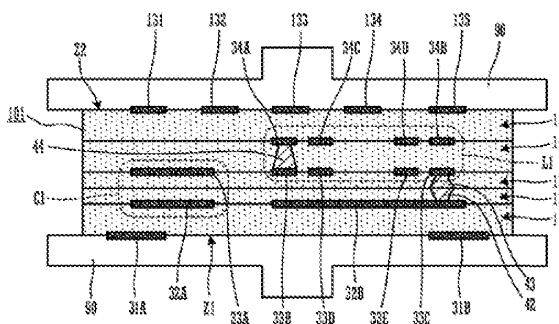


FIG. 4A



10. The laminated circuit substrate according to claim 2, wherein the first conductor pattern and the second conductor pattern define an inductor.

12. The laminated circuit substrate according to claim 2, wherein an inductor and a capacitor are defined by the first and second conductor and other conductors.

13. The laminated circuit substrate according to claim 12, wherein the coil is defined by linear conductor patterns and a via hole.

17. The laminated circuit substrate according to claim 2, wherein the roughened surfaces of the first principal surface and the second principal surface are etched surfaces.

Document 2 (D2) relates to stand-alone organic-based passive devices, and is concerned with certain aspects of the subject Application USSN 14/748,623.

For example, D2 discloses how multilayer thermoplastic substrates may be formed using in part selectively etched layers, to form included elements such as inductors and/or capacitors and vias. See, D2, Abstract in pertinent part; emphasis added:

Abstract

The present invention provides for low cost discrete inductor devices in an all organic platform. The inductor devices can utilize virtually any organic material that provides the desired properties, such as liquid crystalline polymer (LCP) or polyphenyl ether (PPE), in a multilayer structure, wherein the organic materials have low moisture uptake and **good temperature stability**. Each layer may be metalized and **selectively interconnected by vias formed in respective layers so as to form winding or coiled inductors**. The inductor devices may advantageously include external shielding formed by metalizing the side walls and top surface of the inductor devices on in-built shielding achieved by the utilization of the hybrid co-planar waveguide topologies....

See, also, D2, Col 6, lines 29-32, in pertinent part as follows (emphasis added):

FIGS. 2A-C are cross-sectional views of three illustrative embodiments of the packaging of a **multi-layer organic structure** according to an embodiment of the present invention.

...

See, also, D2, Col 8, line 1 – Col. 9, line 4, in pertinent part as follows (emphasis added):

FIG. 2A illustrates a cross-sectional view of an embodiment of a multilayer all organic device 200 in accordance with the present invention. The device 200 comprises a device component 202 sandwiched between two shielding and packaging components 204. The **device component 202 comprises a metalized organic dielectric layer 208 and two bond ply layers 210. The bond ply layers 210** (also referred to as prepreg) may comprise Speedboard from W. L. Gore & Associates, Inc. or Roger 4350 from Rogers Corporation. While the device component 202 only shows one metalized organic substrate layer, **the device component may comprise multiple metalized layers, which can be metalized on one or both sides, that are stacked with bonding material interposed between the metalized layers as needed for bonding the layers together.** For example, thermoset materials, like bond ply or prepreg, can be utilized. Alternatively, one could alternate **layers of high and low temperature thermoplastics, or utilize a combination of thermosets and thermoplastics.** The device 200 is particularly well suited for mounting to a circuit board using surface mount device (SMD) techniques, as discussed in more detail below. The shielding and packaging components 204 comprise relatively thicker organic core layers 212, and as desired, shielding on one or more external surfaces of the device.

...

The **bond ply layers 210 sandwich the metalized dielectric layer 208 and facilitate a bond between the dielectric layer 208 and the core layer 212.** The core layers 212 preferably comprise a 36 mils thick layer of a hydrocarbon composite. Suitable materials for the bond ply layers 210 include any uncured organics such as epoxy/glass composites, PPE, hydrocarbon composites, and prepreg, and other suitable materials for the core layers 212 include cured organics such as epoxy/glass composites, PPE, hydrocarbon composites and prepreg. It should be noted that the

organic materials comprising the various layers of the multilayer device 200 may all be a thermostat or thermoplastic, or they may be a combination of the two as described above. The organic materials selected may be chosen advantageously to thermally match or closely match adjacent material layer and/or the outer layer of the device 200 to the substrate on which it is mounted.

See, also, D2, Col. 13 line 55 - Col. 14 line 21, in pertinent part as follows (emphasis added):

II. Illustrative Methods for Fabricating Stand-Alone Inductors

An illustrative process for fabricating an LCP based integrated passive device (IPD), such as the inductor illustrated in FIG. 6, configured as a surface mount device (SMD) in accordance with an embodiment of the present invention is now described with reference generally to FIG. 12A. Initially, a starting material is selected, which is preferably a reinforced or non-reinforced LCP laminate that can be unclad, or clad with copper on one or both sides of the LCP, as illustrated in Step 1. ... Next, vias are drilled through the LCP or other laminate and the layers of copper, as illustrated in Step 2. ...

Steps 3 and 4, involve the metallization of the vias and laminate. In additive, semi-additive, or subtractive processes starting with unclad or copper clad LCP or other laminates, both sides of the LCP or other laminate and the vias are seeded using electroless plated, vacuum deposited copper or another deposition method for forming a continuous copper film. To achieve the target metal thickness for the device, electrolytic plating is done to build the copper on both sides of the laminate and in the vias in a single step. The circuit definition for the inductor component can be done using subtractive, semi-additive or fully additive processes with panel or pattern electroplating of copper followed by print and etch steps to define the inductor component of the device layer, as illustrated in Step 5.

The fabricated device circuits are then packaged.... The added layers on either side of the inductor component are often referred to as core layers. The internal and external metal layers are connected, as needed, using plated through holes that can be drilled mechanically or with

laser, photo, or plasma processes to provide signal and ground connections and SMD terminals, as illustrated in Step 7. The two edges of the device without the through hole are also slotted using mechanical drill/rout/mill, laser cutting, or sawing processes to provide for additional shielding of the device during subsequent metallization. ...

With reference to Steps 9, 10, and 11, the final metal thickness for the outer layers is built up by electroplated copper in the through holes, shielding slots, and on the top and bottom surfaces. Subtractive, semi-additive, or additive processes may be used to define the outerlayer ground circuits and SMD terminals for **connection with print and etch processing of the copper, as described above in connection with Steps 4 and 5.** The device is then finished with terminal metals....

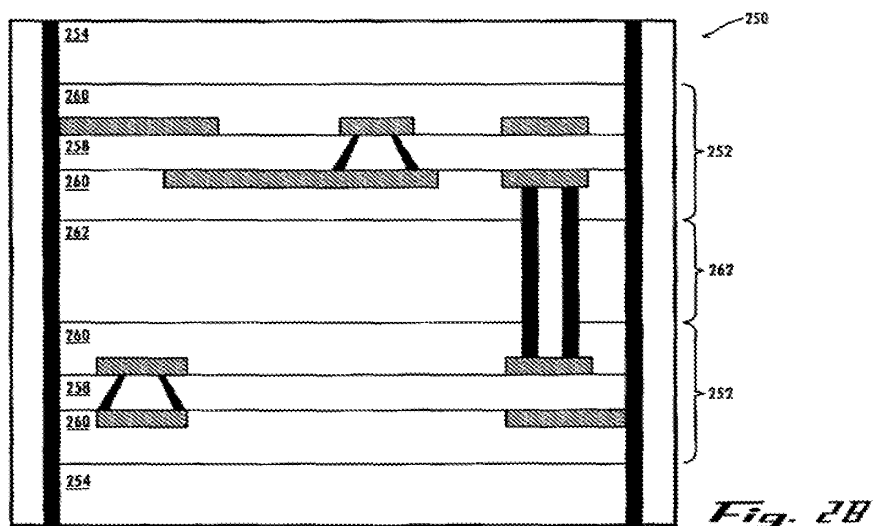
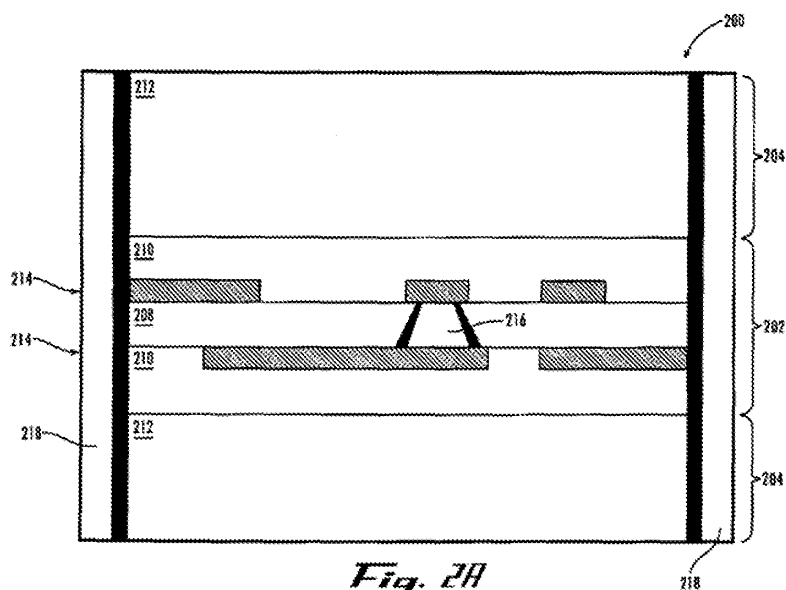
The fully fabricated wafer (also referred to as panel) is then singulated into individual inductor devices. ...

...

See, also, D2, Col 18, lines 62-67, in pertinent part as follows (emphasis added):

Regardless of the manner in which inductor device design/optimization system 610 is initiated, at block 702, inductor device design/optimization system 610 may receive one or more design parameters **for a substrate structure in which a design component, such as an inductor, capacitor, etc., is to be fabricated**....

D2 exemplary arrangements per Figures 2A and 2B thereof, appear as follows:



Thus, per the foregoing, at least the exemplary above-indicated disclosure of Document 2 subject matter as relates to multilayer thermoplastic substrates with selected etched surfaces and included inductor and/or capacitor elements, is pertinent to at least such aspects of the independent and selected dependent claims of the subject Application USSN 14/748,623.

Document 3

Patent No.: US Patent 8,345,433
Inventor: White, et al.
Application No.: 11/177,508
Filed: July 8, 2005
Issue Date: January 1, 2013

Concise Description:

Document 3 was published prior to the earliest possible priority date of February 15, 2013 for the subject Application USSN 14/748,623.

The subject Application USSN 14/748,623 is entitled "LAMINATED CIRCUIT SUBSTRATE." It relates in pertinent part to laminated circuits formed of thermoplastic resin layers laminated with conductor patterns and with selected internal surfaces subjected to roughening processes (etching), to form laminated capacitor and/or inductor circuit elements. See, for example, application Abstract, and paragraphs [0068] and [0074] in pertinent part, as follows (emphasis added):

Abstract

Sheets are laminated on each other and pressure bonded with fixtures from upper and lower directions of a lamination direction while being heated to produce **a laminated circuit substrate including therein a capacitor and a coil**. The capacitor is defined by a first conductor pattern and a second conductor pattern that face each other across thermoplastic resin layers. In the laminated circuit substrate, the first conductor pattern includes a first principal surface, the second conductor pattern includes a second principal surface, the first principal surface faces the second conductor pattern, the second principal surface faces the first conductor pattern, and the first principal surface and the second principal surface are subject to a roughening process.

...

[0068] Subsequently, as shown in FIG. 3B, the metal films 31 to 35 of the sheets 11 to 15 are **patterned mainly by etching**. As a result, the mounting lands 121, 122, 131, 132, and 133, the external connection terminals 31A and 31B, the **first conductor pattern 32A and the second conductor pattern 33A that define the capacitor C1**, and **conductor patterns 33B, 33C, 33D, 33E, 34A, 34B, 34C, and 34D that define the coil L1** are provided.

...

[0074] However, in the laminated circuit substrate 101, **the roughening process is performed to the first principal surface** that faces the second conductor pattern 33A in the first conductor pattern 32A (see FIG. 5A). Moreover, in the laminated circuit substrate 101, **the roughening process is performed also to the second principal surface 92** that faces the first conductor pattern 32A in the second conductor pattern 33A (see FIG. 5A). **The roughening process includes etching, for example.**

The subject Application USSN 14/748,623 makes seventeen references to “roughening process” but the only explanatory sentence is the one above that: “The roughening process includes etching, for example.” Then, dependent claim 17 states in pertinent part that “the roughened surfaces ... are etched surfaces.”

Sole pending independent claim 2 as published of the subject Application USSN 14/748,623 recites in pertinent part:

2. A laminated circuit substrate comprising:
 - a plurality of thermoplastic resin layers laminated on top of each other;
 - a first conductor pattern including a first principal surface;
 - and
 - a second conductor pattern including a second principal surface; wherein the first conductor pattern and the second conductor pattern face each other across at least one layer of the plurality of thermoplastic resin layers;

the first principal surface and the second principal surface are roughened surfaces.

FIG. 3B

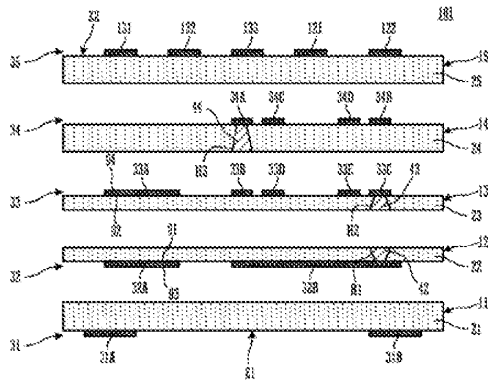
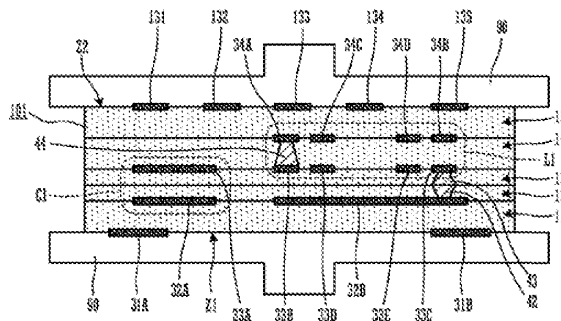


FIG. 4A



10. The laminated circuit substrate according to claim 2, wherein the first conductor pattern and the second conductor pattern define an inductor.

12. The laminated circuit substrate according to claim 2, wherein an inductor and a capacitor are defined by the first and second conductor and other conductors.

13. The laminated circuit substrate according to claim 12, wherein the coil is defined by linear conductor patterns and a via hole.

17. The laminated circuit substrate according to claim 2, wherein the roughened surfaces of the first principal surface and the second principal surface are etched surfaces.

Document 3 (D3) relates to heterogeneous organic laminate stack ups for high frequency applications, and is therefore concerned with certain aspects of the subject Application USSN 14/748,623.

For example, D3 discloses how thermoplastic substrates may be formed using in part selectively etched layers, to form included elements such as inductors and/or capacitors and vias. See, D3, Abstract in pertinent part; emphasis added:

Abstract

Organic laminate stack ups are disclosed for a variety of applications, including high frequency RF applications. One or more inner core layers may be disposed between outer layers **along with bondply or prepreg layers as needed**. Discrete devices, including surface mount components and flip chips, may be embedded within the organic laminate stack up structures. The embedding of the discrete devices, which may be active or passive devices, may be in the form of a layer of bondply or prepreg encapsulating the discrete devices. ... Further, shielding may be provided for the organic laminate stack up structure, including through a wall of vias or a plated trench cut along at least one side of the stack up structure. ...

See, also, D3, Col. 2, lines 44-48, in pertinent part as follows (emphasis added):

FIGS. 1A-1D illustrate exemplary stack up structures according to embodiments of the present invention.

FIG. 2 illustrates the attachment of surface mount components via solder, alloy, or conductive paste on an inner layer of organic metal clad laminate material. ...

See, also, D3, Col. 3, line 28 – Col. 4, line 21, in pertinent part as follows (emphasis added):

According to an embodiment of the invention, an exemplary heterogeneous organic materials structure will now be described with reference to FIG. 1A. **The outer layers 102, 104 of the stack up 100 may include thermoplastics** such as Rogers 4350 or Rogers 4003, liquid crystalline polymer (LCP), or other organic material such as hydrocarbon, Teflon, epoxy, or polyimide. ... In addition, the outer layers 102, 104 may be other low dielectric constant, low-loss glass, ceramic, or fiber reinforced organic material. ... Further, the outer layers 102, 104 may form the packaging of the RF device and include several metal layers.

Still referring to FIG. 1A, the one or more inner core layers 106 positioned between the outer layers 102, 104 may include one or more layers of liquid crystalline polymers (LCP) In alternative embodiments, **the inner core layers 106 may also include thermoplastics such as Rogers 4350 or Rogers 4003 material. Other thermoplastic inner core layer 106 materials other than those described above may be utilized....**

The **inner core layers 106**, which may be metal (e.g., copper, aluminum, silver, gold, or other high conductivity material) clad or unclad, **may serve as a basis for the fabrication of passive elements such as the inductors, capacitors**, and matching network structures that serve to make up the baluns, diplexers, duplexers, filters (e.g., high, low pass, and/or bandpass), and the like when the metal layers 108, 110 are circuitized. According to an exemplary embodiment, the photo lithographic techniques may be utilized to circuitize metal layers 108, 110. The photolithographic techniques can be additive, semi-additive, subtractive in

nature, or a combination thereof. The inductors and capacitors may be fabricated by defining circuitry on the top and bottom metal layers 108, 110 of the diclad (e.g., double sided metal such as copper) inner core layer 106 and then interconnected by means of a z-axis connection which can be fabricated by means of laser ablation, mechanical drilling, mechanical punching, plasma drilling, or wet etching followed by metal deposition either by plating, screen printing of conductive paste or vacuum deposition of an appropriate conductor metal such as copper, aluminum, silver, gold, and the like.

See, also, D3, Col. 4, line 62 - Col. 5, line 6, in pertinent part as follows (emphasis added):

In another alternative embodiment, a rigid core may be utilized as illustrated in FIG. 1D. In FIG. 1D, the inner core layers 174, 176, 178 are disposed between the outer layers 170, 172. The one or more of the inner core layers (e.g., layers 174, 178) may be LCP while the one or more inner core layer (e.g., layer 176) may be of a rigid core material such as Rogers 4350, Rogers 4003, or other thermoplastics. The outer layers 170, 172 may be materials such as Rogers 4350, Rogers 4003, or other thermoplastics. In addition, adhesive layers 188, 190, 192, 194, 196 of bond ply or prepreg (e.g., Rogers 4450 prepreg) may be disposed between the inner core layers 174, 176, 178 and outer layers 170, 172 as shown in FIG. 1D.

...

See, also, D3, Col. 5, lines 15-43, in pertinent part as follows (emphasis added):

Multi-Layer Stack Ups Incorporating Discrete Devices and/or Components

Using any of the embodiments described above and other possible stack up combinations as described, the multi-layer organic laminates may be used to embed discrete active and passive devices. The discrete devices may include oscillators, amplifiers, capacitors, and other devices including

RF devices. These discrete devices may be embedded within the organic laminate structures as described below.

A. Embedded Devices

Surface mount devices, which may also include flip chips, are embedded in a module stack up via the following exemplary process. Referring to FIG. 2, a inner core layer 202 with metal layers 204, 206 on each side is illustrated. **One or more vias 216 may also be disposed within core layer 202 to connect metal layers 204 and 206.** According to an exemplary embodiment, the inner core layer 202 is a film of LCP and the metal layers 204, 206 are copper such that a copper clad LCP film is formed. **The copper clad LCP film may be circuitized using a print and etch process** or any of the other processes described previously. Upon circuitization, the devices can be mounted on the copper clad LCP film either via solder, alloy attach, or other conductive adhesive attach. Referring to FIG. 2, the leads 220 of surface mount devices 208, 209 may be connected to the metal layers 204 and 206, respectively, using solder, alloy attach, or other conductive adhesive attach 210. Likewise, a flip chip 212 may also may be attached to metal layer 204 (or metal layer 206) through solder balls, alloy attach, or other conductive adhesive attach 214.

...

D3 exemplary arrangements per Figures 1A, 1D, and 2 thereof, appear as follows:

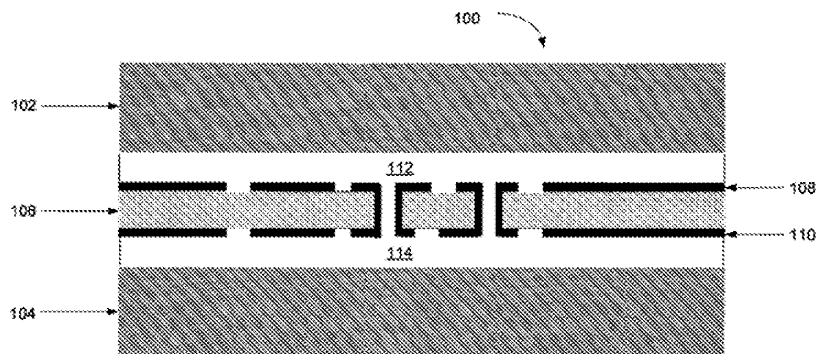


FIG. 1A

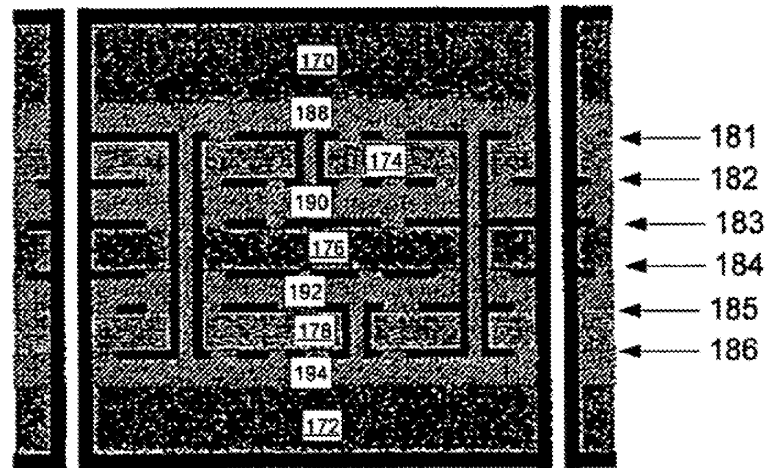


FIG. 1D

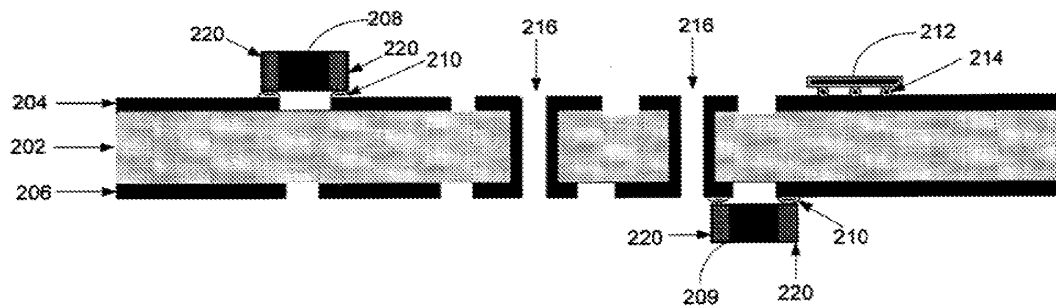


FIG. 2

Thus, per the foregoing, at least the exemplary above-indicated disclosure of Document 3 subject matter as relates to multilayer thermoplastic substrates with selected etched surfaces and included inductor and/or capacitor elements, is pertinent to at least such aspects of the independent and selected dependent claims of the subject Application USSN 14/748,623.



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A third-party submission under 37 CFR 1.290 has been filed on April 11, 2016, and is being entered in the above-identified application. Please allow a few days for the submission to be visible in the Patent Application Information Retrieval (PAIR) system.

/Vei-Chung Liang/
TQAS TC2800

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