UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,489,914 B2
APPLICATION NO. : 11/114733
DATED : February 10, 2009
INVENTOR(S) : Govind et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1, line 17, insert the following paragraph:

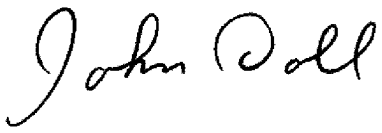
--STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

This invention was made with U.S. Government support under agreement no. DMI-0120308, awarded by the national Science Foundation. The Government has certain rights in this invention.

This invention was further made with U.S. Government support under agreement no. DAAH01-99-D-R002-00, awarded by the United States Army. The Government has certain rights in this invention.--

Signed and Sealed this

Fourth Day of August, 2009



JOHN DOLL
Acting Director of the United States Patent and Trademark Office

Practitioner's Docket No. **062020-1950**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Number: **7,489,914**

Issued: **February 10, 2009**

Name of Patentee: **Govind, et al.**

Title of Invention: **Multi-Band RF Transceiver with Passige Reuse in Organic Substrates**

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Attention: Decision and Certificate of Correction
Branch of the Patent Issue Division

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR APPLICANT'S MISTAKE (37 C.F.R. § 1.323)

1. It is noted that an error appears in this patent of a

☒ clerical

☒ typographical

☒ minor

nature or character, as more fully described below. It occurred in good faith. Correction thereof does not involve such changes in the patent as would constitute new matter or would require re-examination. A certificate of correction is requested.

2. Attached, in duplicate, is Form PTO-1050, with at least one copy being suitable for printing.

NOTE: Form PTO-1050, using the column and line number in the printed patent, should be used exclusively regardless of the length or complexity of the subject matter. M.P.E.P. § 1485.

NOTE: The patent grant should be retained by the patentee. The PTO does not attach the certificate of correction to the patentee's copy of the patent. The patent grant will be returned to the patentee if submitted. M.P.E.P. § 1485.

3. The exact page and line number where the error occurs in the application file are:

NOTE: This information should be identified in this request, however, on Form PTO-1050, only the column and line number in the printed patent should be used. MPEP §1485.

Column 1, line 17, insert the following paragraph:

--STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

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This invention was further made with U.S. Government support under agreement no. DAAH01-99-D-R002-00, awarded by the United States Army. The Government has certain rights in this invention.--

4. Please send the Certificate to:

Name: **Scott A. Horstemeyer**

Address: **Thomas, Kayden, Horstemeyer & Risley, LLP**

600 Galleria Parkway, N.W., Suite 1500, Atlanta, GA 30339

5. Please pay the fee of **$100.00**, as required by 37 CFR 1.20(a), as follows:

☐ Enclosed is a check for **$** .

☒ Charge the Deposit Account 20-0778 the sum of **$100.00**. A duplicate of this request is attached.

Scott A. Horstemeyer, Reg. No. 34,183

Tel. No.: (770) 933-9500

Thomas, Kayden, Horstemeyer & Risley, LLP
600 Galleria Parkway, N.W., Suite 1500
Atlanta, GA 30339-5948

Customer No.: 24504

NOTE: The certificate of correction for applicant's mistake may be signed by the attorney of record, unlike that for PTO mistake where the patentee or an owner of an interest in the invention must make the request.

PTO/SB/44 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,489,914

APPLICATION NO.: 11/114,733

ISSUE DATE : 02/10/2009

INVENTOR(S) : Govind, et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1, line 17, insert the following paragraph:

--STATEMENT REGARDING FEDERALLY SPONSORED
RESEARCH OR DEVELOPMENT

This invention was made with U.S. Government support under agreement no. DMI-0120308, awarded by the national Science Foundation. The Government has certain rights in this invention.

This invention was further made with U.S. Government support under agreement no. DAAH01-99-D-R002-00, awarded by the United States Army. The Government has certain rights in this invention.--

MAILING ADDRESS OF SENDER (Please do not use customer number below):

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.
600 Galleria Parkway, Suite 1500
Atlanta, Georgia 30339

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal

Application Number:	11114733
Filing Date:	25-Apr-2005
Title of Invention:	MULTI-BAND RF TRANSCEIVER WITH PASSIVE REUSE IN ORGANIC SUBSTRATES
First Named Inventor/Applicant Name:	Vinu Govind
Filer:	Scott A. Horstemeyer/Julie Campbell
Attorney Docket Number:	062020-1950

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Certificate of correction	1811	1	100	100
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
		Total in USD ($)		**100**

Electronic Acknowledgement Receipt

EFS ID:	5578366
Application Number:	11114733
International Application Number:	
Confirmation Number:	1270
Title of Invention:	MULTI-BAND RF TRANSCEIVER WITH PASSIVE REUSE IN ORGANIC SUBSTRATES
First Named Inventor/Applicant Name:	Vinu Govind
Customer Number:	24504
Filer:	Scott A. Horstemeyer/Julie Campbell
Filer Authorized By:	Scott A. Horstemeyer
Attorney Docket Number:	062020-1950
Receipt Date:	24-JUN-2009
Filing Date:	25-APR-2005
Time Stamp:	14:34:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$100
RAM confirmation Number	710
Deposit Account	200778
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	00933761.PDF	69063 0092ffaf734e5d273e7c91c7986cf35a61b4fcfd	no	3
Warnings:					
Information:					
2	Miscellaneous Incoming Letter	00933759.PDF	40365 e89f1cddd2c72e697c9fdc14395d36e0170b22d4	no	1
Warnings:					
Information:					
3	Fee Worksheet (PTO-875)	fee-info.pdf	30581 3499fead5a1688e8e317024aca57a8c0639e658e	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	140009		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
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www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/114,733	02/10/2009	7489914	062020-1950	1270

24504 7590 01/21/2009

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
600 GALLERIA PARKWAY, S.E.
STE 1500
ATLANTA, GA 30339-5994

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 487 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Vinu Govind, Decatur, GA;
Sidharth Dalmia, Norcross, GA;
Amit Bavisi, Atlanta, GA;
Venkatesh Sundraram, Norcross, GA;
Madhavan Swaminathan, Marietta, GA;
George White, Marietta, GA;

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/114,733	04/25/2005	Vinu Govind	062020-1950	1270

24504 7590 01/09/2009

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
600 GALLERIA PARKWAY, S.E.
STE 1500
ATLANTA, GA 30339-5994

EXAMINER	
PHU, SANH D	

ART UNIT	PAPER NUMBER
2618	

MAIL DATE	DELIVERY MODE
01/09/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Response to Rule 312 Communication	Application No.	Applicant(s)
	11/114,733	GOVIND ET AL.
	Examiner	**Art Unit**
	SANH D. PHU	2618

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

1. ☒ The amendment filed on *19 December 2008* under 37 CFR 1.312 has been considered, and has been:

   a) ☒ entered.

   b) ☐ entered as directed to matters of form not affecting the scope of the invention.

   c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
   Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

   d) ☐ disapproved. See explanation below.

   e) ☐ entered in part. See explanation below.

/Sanh D Phu/
Primary Examiner
Art Unit: 2618

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

24504 7590 09/23/2008

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
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STE 1500
ATLANTA, GA 30339-5994

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Mary Meegan	(Depositor's name)
Mary Meegan	(Signature)
12-19-08	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/114,733	04/25/2005	Vinu Govind	062020-1950	1270

TITLE OF INVENTION: MULTI-BAND RF TRANSCEIVER WITH PASSIVE REUSE IN ORGANIC SUBSTRATES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	~~$720~~ $755.00	$300	$0	~~$1020~~ $1,055.00	12/23/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHU, SANH D	2618	455-168100

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Thomas, Kayden,
2 Horstemeyer & Risley, LLP
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Georgia Tech Research Corporation Atlanta, GA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☒ Payment by credit card.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 20-0778

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date 12-19-08

Typed or printed name Scott A. Horstemeyer Registration No. 34,183

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Govind, et al.

Group Art Unit: 2618

Examiner: Phu, Sanh D.

Serial No.: 11/114,733

Docket No.: 62020-1950

Filed: April 25, 2005

For: Multi-Band Transceiver with Passive Reuse in Organic Substrates

AMENDMENT AFTER ALLOWANCE

Mail Stop: Issue Fee
P.O. Box 1450
Commissioner for Patents
Alexandria, Virginia 22313-1450

Sir:

Pursuant to 37 C.F.R. 1.312, please enter the following amendments. Applicants respectfully submit that the amendments herein merely embody the correction of formal matters and do not alter the scope or substance of the application.

DEPOSIT ACCOUNT AUTHORIZATION

It is not believed that extensions of time are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefore are hereby authorized to be charged to our Deposit Account No. 20-0778.

AMENDMENTS TO THE SPECIFICATION

The following is a marked-up version of the specification with the language that is underlined ("___") being added and the language that contains strikethrough ("~~~") being deleted:

In the BACKGROUND OF THE INVENTION section:

(paragraph 0004):

Designing multi-band, multi-mode devices such as RF transceivers ~~present~~presents some difficulties in power consumption, compatibility, interference, and integration. For example, the need for the additional design components to support such multi-band, multi-mode capabilities oftentimes presents challenges with power consumption. This may be especially problematic in a portable multi-band, multi-mode device such as a cell phone operating on a battery. The battery life of the cell phone would decrease as the power consumption requirements of the components within the cell phone increase. Further, as many devices continue to decrease in size, the inclusion of additional components becomes ~~increasing~~increasingly difficult due to problems such as routing, interference, etc. Achieving the required quality factors (Qs) of these components may become more difficult with these size constraints. In addition, the components may have to conform to improved performance characteristics such as high clock speed, low noise, wide bandwidth, and high temperature tolerance.

In the SUMMARY OF THE INVENTION section:

(paragraph 0006):

The present invention overcomes the difficulties above by describing multi-band, multimode integrated RF transceiver topologies, ~~comprising~~comprised of on-chip actives and in-package embedded high-Q passives in organic substrates that, in certain circumstances, can be reused at different frequency ranges, thereby reducing the number of components required. Two components of such an RF transceiver include voltage controlled oscillators (VCOs) and low noise amplifiers (LNAs). According to an embodiment, high-performance LNAs with low noise figures (NF) and VCOs with low phase noise may be formed from high-Q passive components embedded in organic substrates such as LCP (liquid crystalline polymer).

(paragraph 0010):

According to yet another embodiment of the present invention, ~~A~~an oscillator for use in an RF transceiver includes a first organic layer with a top surface and a bottom surface opposite the top surface, a first conductive layer positioned on the top surface of the first organic layer, a second conductive layer positioned on the bottom surface of the

first organic layer, a second organic layer positioned opposite the second conductive layer, a plurality of passive devices patterned on at least one of the first conductive layer and the second conductive layer, and at least one discrete active device positioned on the first conductive layer and in communication with at least a portion of the plurality of passive devices, wherein a feedback network for the active device is created such that the discrete active device becomes unstable and generates at least one signal at a particular frequency.

In the BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS section:

(paragraph 0034):

FIGs. 21 and 22 ~~illustrates~~illustrate alternative circuit diagrams of oscillators that can be implemented in accordance with an embodiment of the present invention.

(paragraph 0037):

~~FIG.~~FIGS. 24A, 24B, and 25 show measured ~~characteristic~~characteristics of the oscillator of FIGs. 23A and 23B.

(paragraph 0049):

FIG. 35 shows ~~and~~an exemplary circuit diagram of a low noise amplifier in accordance with an embodiment of the present invention.

(paragraph 0052):

FIGS. 38A-38F ~~illustrates~~illustrate substrate variations according to an embodiment of the present invention.

In the DETAILED DESCRIPTION section:

(paragraph 0060):

Since these inductors are very close to each other, the magnetic coupling between these filters, represented by M in FIG. 1A, can increase the pass bandwidth of the filter, thereby decreasing its performance. However, an inter-resonator parallel plate coupling capacitor 224, (with or without the coplanar in-built shielding 230) formed using two disconnected metal plates (one plate formed using patterning conductive layer 238 and the other plate formed using patterned conductive layer 240) and shown as capacitor plates 224a, 224b is provided. The capacitor plates 224a, 224b sandwich the first organic dielectric layer 236 in such a manner that ~~the~~ each plate of the inter-resonator coupling capacitor electrode is connected to separate resonators which helps compensate the effect of the magnetic coupling and helps make very compact filters. The center capacitance can be as small as femptoFarads or as large as picoFarads for achieving the specified bandwidths. The smaller capacitance helps reduce the

bandwidth. Additionally, capacitor 224 in parallel with the mutual inductance equivalent gives a pole in the lower band or upper band.

(paragraph 0061):

The bottom plate formed by the conductive layer 240 connects to inductor 212 using one or more microvias in the organic dielectric layer 236, such as the vias 244 with pads 246 for landing and capturing the via. First and second shield electrodes 248, 250 formed respectively on the organic core layers 252, 254, wherein the core ~~layer~~layers 252 and 254 are disposed so as to sandwich the organic dielectric layer 236 there between. A first resonator 260 formed by inductor 212 and capacitor 216 and a second resonator 262 formed by inductor 214 and capacitor 218 are electrically coupled to each other through the parallel plate capacitor 224, whereby an inter-resonator coupling is effected in combination with said magnetic coupling and electric coupling.

(paragraph 0073):

In a dielectric filter according to the embodiment illustrated in FIGS. 2A-2C, the side wall ground shield electrodes 232, 234 can be fabricated, if desired, by single or multiple connected drilled and plated through holes or using a saw cutting device and then connected via electroless or sputter seeded copper in the through hole. The copper can be electroplated in the through hole and on the surface. The copper can then be printed and etched to form SMD connection. The process flow for a two layer plus the packaging of the SMD device is explained in greater detail in connection with FIG. 5.

(paragraph 0078):

The following are examples of various embodiments of the present invention, wherein each illustrative ~~embodiments~~embodiment discloses several aspects of the invention.

(paragraph 0080):

Steps 3 and 4 involve the metallization of the through vias and laminate. In additive, semi-additive, or subtractive processes starting with unclad or copper clad LCP or other laminates, both sides of the LCP or other laminate and the vias are seeded using electroless plated, vacuum deposited copper or another deposition ~~methods~~method to form a continuous copper film. To achieve the target metal thickness for the device, electrolytic plating is done to build the copper on both sides of the laminate and in the vias in a single step. The circuit definition for the filter component can be done using subtractive, semi-additive or fully additive processes with panel or pattern electroplating of the copper followed by print and etch steps to define the filter circuitry, as illustrated in Step 5.

(paragraph 0081):

The fabricated device circuits are then packaged using vacuum or non-vacuum lamination of LCP or alternate laminate materials as detailed above in connection with Step 1, and/or Al, Cu, Mo metal (for high power applications) on both sides of the filter to provide sufficient thickness to encapsulate components, as illustrated in Step 6. The internal and external metal layers are connected, as needed, using plated through holes that can be drilled mechanically or with laser, photo, or plasma processes to provide signal and ground connections and SMD terminals, as illustrated in Step 7. The two edges of the device without the through hole can also be slotted using mechanical drill/rout/mill, laser cutting, or sawing processes to provide for additional shielding of the device during subsequent metallization. The drilled through holes and shielding slots are seeded with electroless plated or sputter/vacuum deposited copper to provide a bus layer in substantially the same manner as described above in connection with Step 3, as illustrated in Step 8.

(paragraph 0092):

The bandpass filter 500 further comprise ~~at~~ two external ground shield electrodes 534 respectively formed on different side surfaces of a laminated body comprising said first through three or more dielectric layers and connected to said shield electrodes. Additionally these provide the connection for the shorted inductors/ resonators and capacitors. Moreover, the presence of these external electrodes makes it a CPW/stripline topology, where the reference ~~is~~ on the same first dielectric layer provides the shielding internally, and also provides for the ground connectivity to the resonators/inductors and capacitors.

(paragraph 0124):

The layout for the passive networks shown in FIG. 16A was designed to achieve unloaded Qs of approximately 100 for the passive components in order to obtain near minimum phase noise performance for the oscillator. Increase in the unloaded Q of the resonant tank formed by inductor L 1012 and capacitors 1014 and 1016 beyond a certain point (e.g., 300) may have a diminishing effect on the phase noise performance of the oscillator. Hence, the use of organic substrates such as LCP as shown in FIG. 16B or polyphenyl ether may be used since they may provide Qs of over 100 for capacitors. In order to make the designs more compact, a two-layer cross-section was utilized for the substrate as shown in FIG. 16B. According to FIG. 16B, the layout includes metal layers 1050, 1052, and 1054. Metal layers 1050 and 1052 may be approximately 9μm thick while metal layer 1054 may be approximately 5μm thick. In addition, the layout includes LCP and bondply layers 1056 and 1058 along with hydrocarbon layer 1060. The LCP and bondply layers 1056 and 1058 may ~~be~~ comprise LCP that is approximately 25μm thick. The hydrocarbon layer 1060 ~~that~~ may be approximately 32 mils thick. It will be appreciated by one of ordinary skill in the art that the cross-section in FIG. 16B is for illustrative purposes only. Many other variations are possible, including varying the thickness of the metal layers and organic layers. In

addition, the numbers of metal layers and organic layers may change depending on the number of components to be included and the specification of the components. Further, the hydrocarbon layer 1060 may be a PCB (printed circuit board) or even replaced by another material that provides for sufficient rigidity.

(paragraph 0130):

Oscillator designs similar to those shown in FIGs. 16B and 16C can be implemented using other organic substrates besides LCP. For instance, epoxy-based substrates such as FR-4 epoxy can be utilized. FIGs. 19 and 20 show the measured performance for a 3.3 GHz and a 5.2 GHz oscillator, respectively, that were fabricated using the epoxy substrate. While fabricated oscillators utilizing LCP-based substrates generally have lower phase noise figures, the 5.2GHz oscillator fabricated using the epoxy substrate still meets the phase noise figure specifications of the IEEE 802.11a protocol.

(paragraph 0156):

FIG. 38C illustrates the layers shown in FIG. 38B, except that high K layers have been substituted as for the laminate layers. When compared to the laminate layers, the high K layers increase the separation and increase the capacitance for capacitor components that may be placed on the high K layers. Generally, the non-critical, lower-performing components would be placed on the high K layers. FIG. 38D illustrates three LCP layers that are separated by two prepreg layers. An aspect of the stackup shown in FIG. 38D compared to the previous ~~stickups~~stackups in FIGS. 17A-C is that this is an extremely thin stackup which may be on the order of a 0.3mm thick substrate. Four metal layers are shown in FIG. 38D, which may contain components such as capacitors and inductors, providing for excellent density. FIG. 38D may be known as a high performance substrate. One of ordinary skill would recognize that the stackup in FIG. 38D is not limited to 3 LCP layers, but could contain additional layers, including another LCP layer that is separated from the other LCP layer by a prepreg layer.

REMARKS

Applicants request that minor corrections for typographical errors to the specification be entered. In addition, Applicants note that replacement drawings for FIGS. 12, 16D, 19, 31C, 33, and 35 in compliance with 37 C.F.R. 1.84 and 37 C.F.R. 1.21(d) are submitted herewith. Applicants respectfully assert that the foregoing amendments are not being submitted for the purpose of delay and do not involve new matter. If, in the opinion of the Examiner, a telephonic conference would expedite entry of the foregoing amendments, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

By: _____

Scott A. Horstemeyer, Reg. No. 34,183

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.
600 Galleria Parkway, SE
Suite 1500
Atlanta, Georgia 30339-5948
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Fax: (770) 951-0933

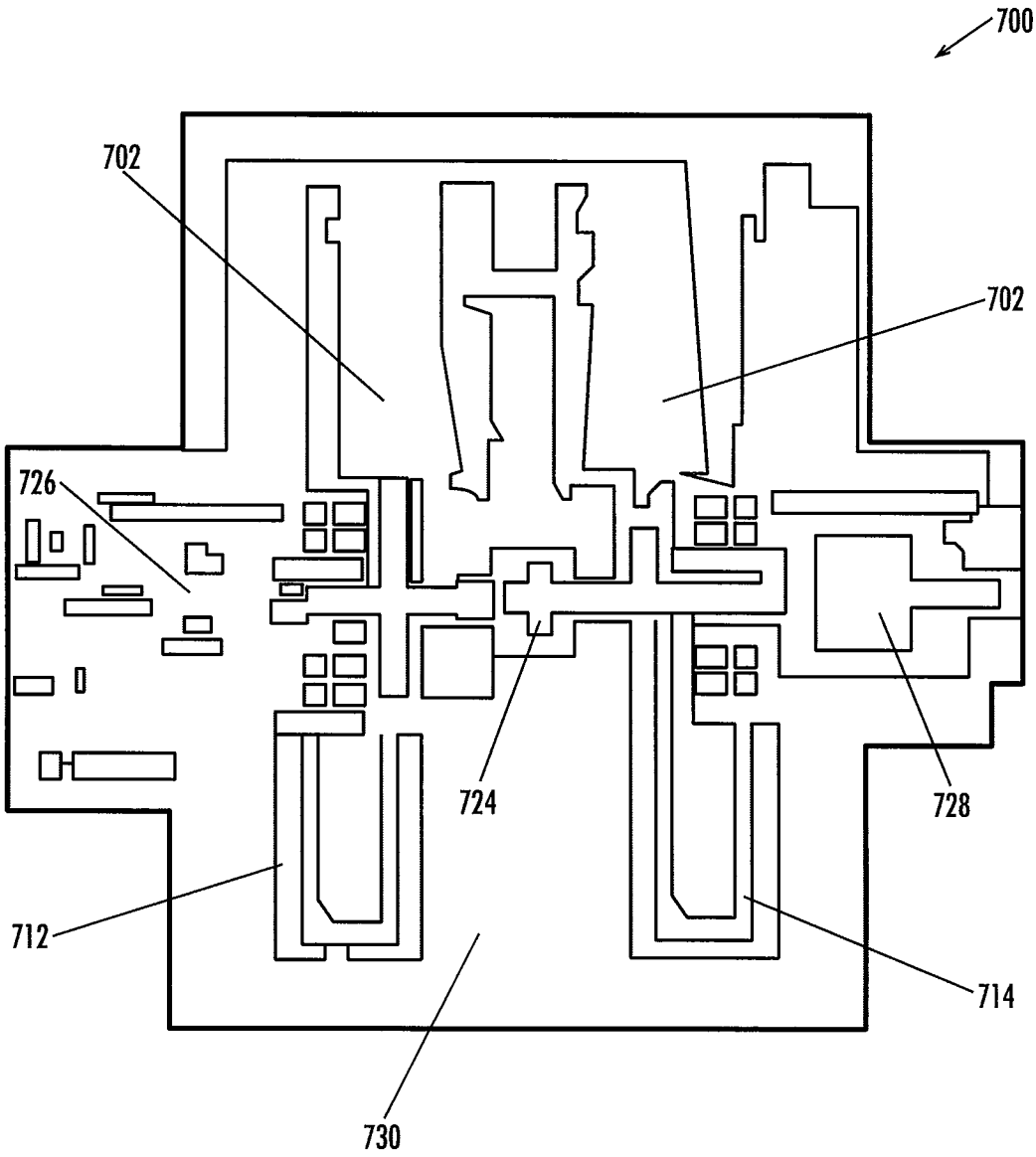


Fig. 12

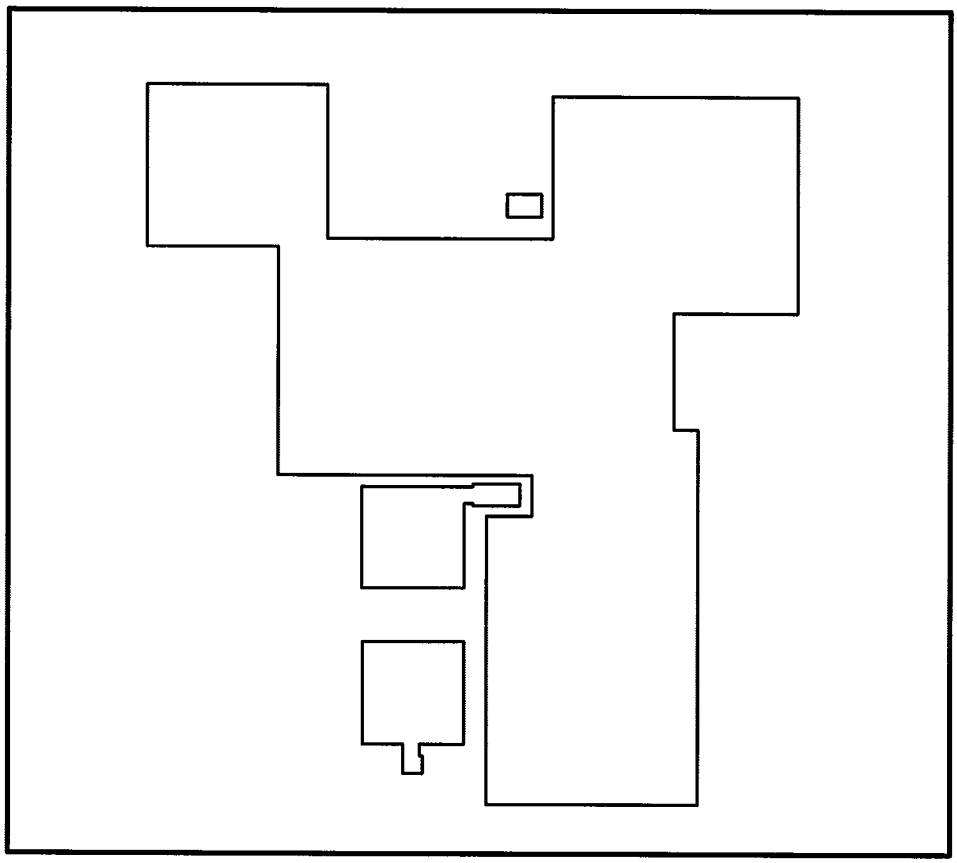


Fig. 16D

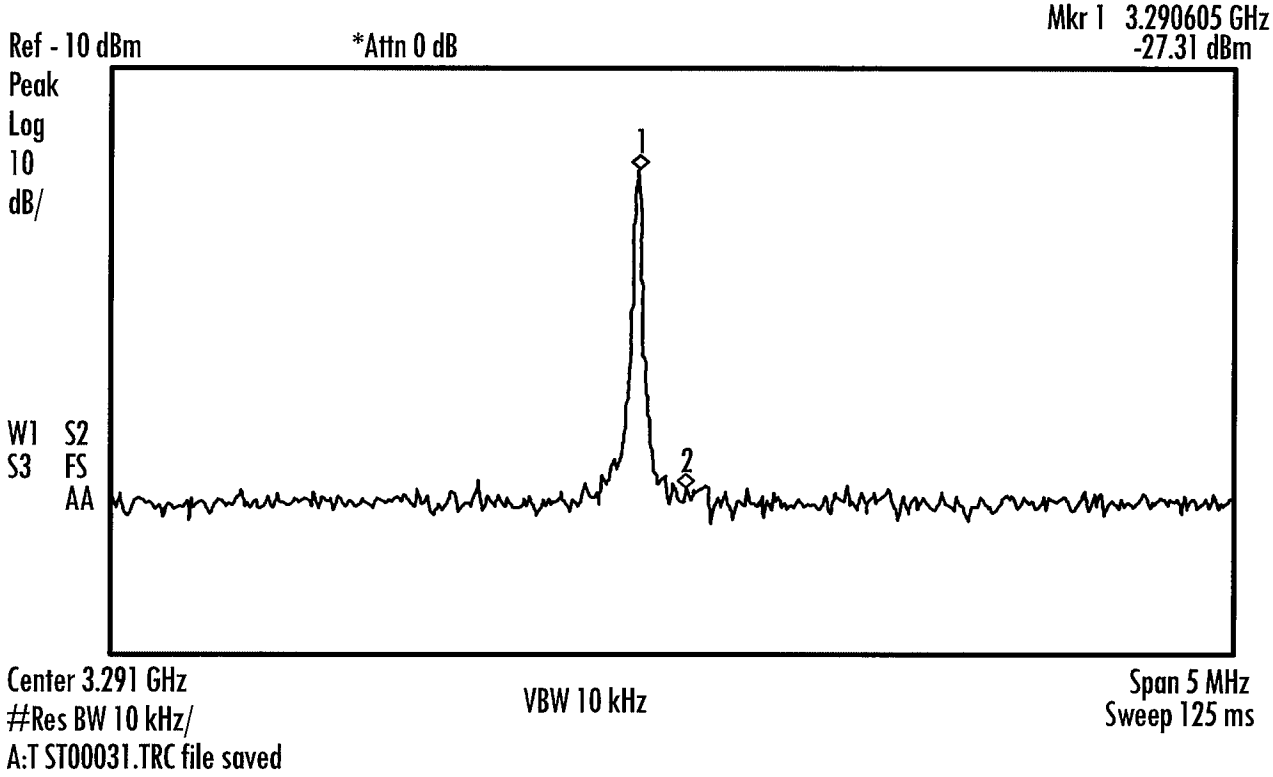


Fig. 19

EX1002 / Page 23 of 416
Murata Manufacturing Co., Ltd.

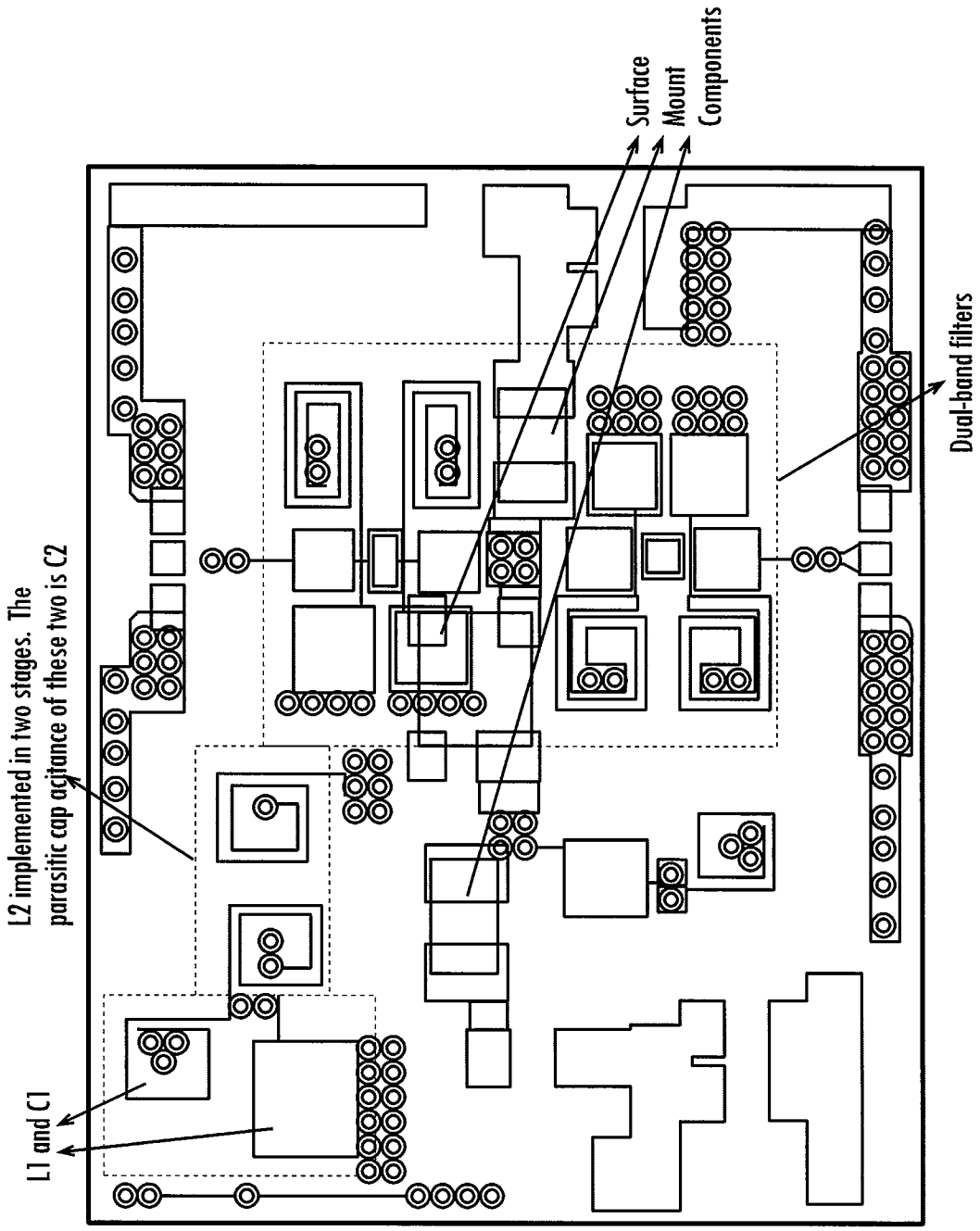

Surface Mount Components
Dual-band filters
L2 implemented in two stages. The parasitic cap acitance of these two is C2
L1 and C1

Fig. 31C

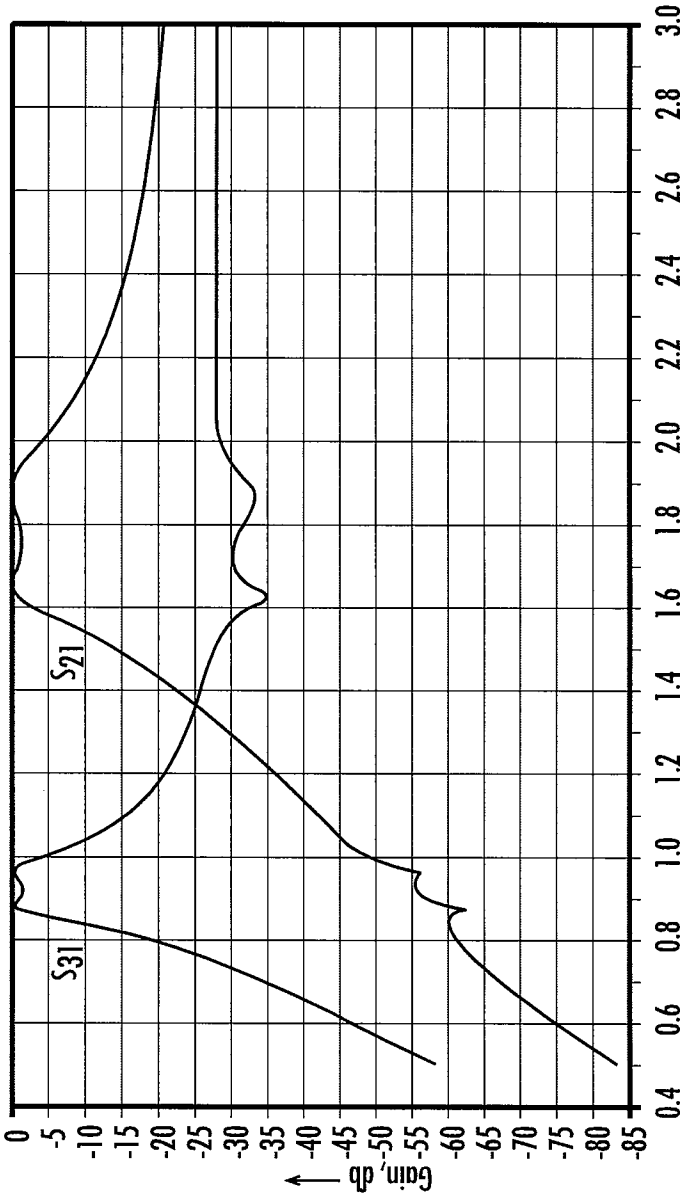

Gain, db
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50
-55
-60
-65
-70
-75
-80
-85
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2
2.4
2.6
2.8
3.0
freq GHz
S21
S31

Fig. 33

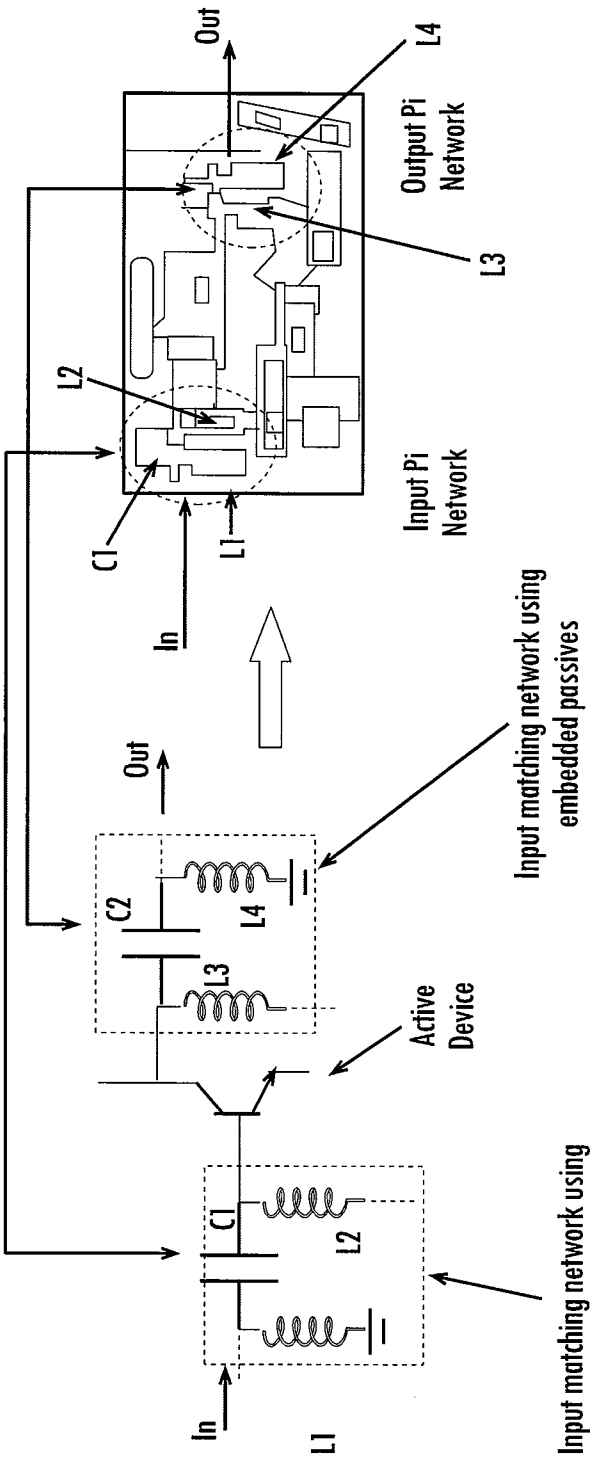

Out
L4
Output Pi Network
L3
L2
Input Pi Network
C1
L1
In
Out
Input matching network using embedded passives
C2
L4
L3
Active Device
C1
L2
In
L1
Input matching network using embedded passives

Fig. 35

Electronic Patent Application Fee Transmittal

Application Number:	11114733
Filing Date:	25-Apr-2005
Title of Invention:	MULTI-BAND RF TRANSCEIVER WITH PASSIVE REUSE IN ORGANIC SUBSTRATES
First Named Inventor/Applicant Name:	Vinu Govind
Filer:	Scott A. Horstemeyer/mary meegan
Attorney Docket Number:	062020-1950

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	2501	1	755	755
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1055**

Electronic Acknowledgement Receipt

EFS ID:	4489444
Application Number:	11114733
International Application Number:	
Confirmation Number:	1270
Title of Invention:	MULTI-BAND RF TRANSCEIVER WITH PASSIVE REUSE IN ORGANIC SUBSTRATES
First Named Inventor/Applicant Name:	Vinu Govind
Customer Number:	24504
Filer:	Scott A. Horstemeyer/mary meegan
Filer Authorized By:	Scott A. Horstemeyer
Attorney Docket Number:	062020-1950
Receipt Date:	19-DEC-2008
Filing Date:	25-APR-2005
Time Stamp:	10:28:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1055
RAM confirmation Number	8382
Deposit Account	200778
Authorized User	HORSTEMEYER,SCOTT A.

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	00834926.PDF	100412 adf77d4e6648781617b182368c085acc667af563	no	1
Warnings:					
Information:					
2	Amendment after Notice of Allowance (Rule 312)	00834929.PDF	355561 54c5b5bd519f451015b7e37949c5ea879468291b	no	7
Warnings:					
Information:					
3	Drawings-only black and white line drawings	00834930.PDF	85185 563da3418b03cee82e0c52b7ee562ddacb122d51	no	6
Warnings:					
Information:					
4	Fee Worksheet (PTO-06)	fee-info.pdf	31882 bcc14ed21a0fa63cfcb025986e00f9aec2dfe336	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	573040		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

24504 7590 09/23/2008

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
600 GALLERIA PARKWAY, S.E.
STE 1500
ATLANTA, GA 30339-5994

EXAMINER	
PHU, SANH D	
ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 09/23/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/114,733	04/25/2005	Vinu Govind	062020-1950	1270

TITLE OF INVENTION: MULTI-BAND RF TRANSCEIVER WITH PASSIVE REUSE IN ORGANIC SUBSTRATES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$720	$300	$0	$1020	12/23/2008

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

24504 7590 09/23/2008

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
600 GALLERIA PARKWAY, S.E.
STE 1500
ATLANTA, GA 30339-5994

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/114,733	04/25/2005	Vinu Govind	062020-1950	1270

TITLE OF INVENTION: MULTI-BAND RF TRANSCEIVER WITH PASSIVE REUSE IN ORGANIC SUBSTRATES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$720	$300	$0	$1020	12/23/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHU, SANH D	2618	455-168100

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/114,733	04/25/2005	Vinu Govind	062020-1950	1270

24504 7590 09/23/2008

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
600 GALLERIA PARKWAY, S.E.
STE 1500
ATLANTA, GA 30339-5994

EXAMINER	
PHU, SANH D	
ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 09/23/2008

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 541 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 541 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	11/114,733	GOVIND ET AL.	
	Examiner	Art Unit	
	SANH D. PHU	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Amendment filed on 8/1/08*.

2. ☒ The allowed claim(s) is/are *1-3,5,16-21 and 33-42*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

1. This Office Action is responsive to the Amendment filed on 8/1/2008.

REASONS FOR ALLOWANCE

2. Claims 1-3, 5, 16-21, 33-42 are allowed.

3. The following is an examiner's statement of reasons for allowance:

Claims 1-3, 5, 16-21, 33-42 are allowable over the prior art of record for the reason as stated in the Applicant's Remark dated on 8/1/2008 pages 6-7 and the reasons as below:

Regarding to claim 1, none of the prior art of record teaches or suggests a multi-band RF device operable at a first frequency and a second frequency different from the first frequency, comprising: an active device; a first passive network in communication with the active device, the first passive network being a first matching network at an input of the active device; a second passive network in communication with the active device, the second passive network being a second matching network at an output of the active device; and an organic-based substrate having at least two metal layers, wherein the two metal layers are patterned to form at least a portion of the first passive network and the second passive network, wherein impedances of the first and second passive networks are different at the first frequency than the second frequency. It would not have been obvious for a person skilled in the art to combine other prior arts of record in order to arrive at the claimed invention.

Regarding to claim 16, none of the prior art of record teaches or suggests a multi-band low noise amplifier for use in an RF application, comprising: an active

device; a first matching network, wherein an impedance of the first matching network at a first frequency is different than the impedance of the first matching network at a second frequency; a second matching network, wherein an impedance of the second matching network at the first frequency is different than the impedance of the second matching network at the second frequency; and a multi-layer organic-based substrate having at least one metal layer, wherein the first matching network and the second matching network are formed on the at least one metal layer and wherein the active device is mounted on the multi-layer organic substrate, thereby allowing the an output of the multi-band low noise amplifier to have desired power gains at the first frequency and the second frequency based at least in part on each of the first and second matching networks having the different reactance at the first frequency and the second frequency. It would not have been obvious for a person skilled in the art to combine other prior arts of record in order to arrive at the claimed invention.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sanh D. Phu whose telephone number is (571)272-7857. The examiner can normally be reached on M-Fr from 8:00-16:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on (571) 272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sanh D Phu/
Primary Examiner
Art Unit 2618

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11114733	GOVIND ET AL.
	Examiner	Art Unit
	SANH D PHU	2618

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	04/02/2008	09/06/2008							
1	1	✓	=							
2	2	✓	=							
3	3	✓	=							
	4	O	-							
4	5	O	=							
	6	N	-							
	7	N	-							
	8	N	-							
	9	N	-							
	10	N	-							
	11	N	-							
	12	N	-							
	13	N	-							
	14	N	-							
	15	N	-							
5	16	=	=							
6	17	=	=							
7	18	=	=							
8	19	=	=							
9	20	=	=							
10	21	=	=							
	22	N	-							
	23	N	-							
	24	N	-							
	25	N	-							
	26	N	-							
	27	N	-							
	28	N	-							
	29	N	-							
	30	N	-							
	31	N	-							
	32	N	-							
11	33		=							
12	34		=							
13	35		=							
14	36		=							

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11114733	GOVIND ET AL.
	Examiner	Art Unit
	SANH D PHU	2618

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	04/02/2008	09/06/2008							
15	37		=							
16	38		=							
17	39		=							
18	40		=							
19	41		=							
20	42		=							

Issue Classification

Application/Control No.	Applicant(s)/Patent Under Reexamination
11114733	GOVIND ET AL.
Examiner	**Art Unit**
SANH D PHU	2618

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
455	168.1	H 0 4 B 1 / 18 (2006.01)	

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
455	252.1	73	552.1		
257	723	724			

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	6	17	11	33										
2	2	7	18	12	34										
3	3	8	19	13	35										
	4	9	20	14	36										
4	5	10	21	15	37										
	6		22	16	38										
	7		23	17	39										
	8		24	18	40										
	9		25	19	41										
	10		26	20	42										
	11		27												
	12		28												
	13		29												
	14		30												
	15		31												
5	16		32												

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	19	
/SANH D PHU/ Primary Examiner.Art Unit 2618	9/6/08	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	35

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11114733	GOVIND ET AL.
	Examiner	**Art Unit**
	/Sanh D Phu/	2618

SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
455	168.1, 252.1, 73, 552.1	4/2/08	SP
257	723,724	4/2/08	SP
	Above Updated	9/6/08	SP

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
EAST (Text Search)	4/2/08	SP
EAST (Text Search)	9/6/08	SP
Checking co-pending application double patenting	9/6/08	SP

INTERFERENCE SEARCH			
Class	**Subclass**	**Date**	**Examiner**
455	168.1	9/6/08	SP
	PG-Pub text Search	9/6/08	SP

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	744588	amplifier or amplifiers	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 14:45
L2	552522	matching	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 14:46
L3	2712290	input	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 14:46
L4	42448	2 with 3	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 14:46
L5	3272371	output	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 14:46
L6	44844	2 with 5	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 14:46
L7	1987615	substrate or subtrates	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 14:47
L8	2871	1 and 4 and 6 and 7	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 14:48
L9	287420	1.ab.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 14:48
L10	914	8 and 9	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 14:48
L11	3531707	layer or layers	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 14:49
L12	444	10 and 11	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 14:49
L13	565379	hydrocarbon	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 14:49
L14	399819	crystalline	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 14:50

EAST Search History

L15	1	12 and 13	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 14:50
L16	22	12 and 14	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 14:50
L17	21	16 not 15	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 14:50
L18	10	("2003/0017683").URPN.	USPAT	OR	OFF	2008/09/08 15:18
L19	4	("6646293").URPN.	USPAT	OR	OFF	2008/09/08 15:20
L23	933446	7.clm. or 11.clm.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 15:24
L24	258	23 and 12	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 15:25
L25	238	24 not 16	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 15:25
L26	227031	Vinu.in. or Govind.in. or Sidharth.in. or Dalmia.in. or Amit.in. or Bavisi.in. or Venkatesh.in. or Sundraram.in. or Madhavan.in. or Swaminathan.in. or George.in. or White.in.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 17:05
L27	798	"georgia tech research".as.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 17:06
L28	227799	26 or 27	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 17:06
L29	1	28 and 24	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 17:06
L30	3	28 and 12	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/09/08 17:07

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Confirmation No.: **1270**
Govind *et al.*	Group Art Unit: **2618**
Serial No.: **11/114,733**	Examiner: **Phu, Sanh D**
Filed: **April 25, 2005**	Docket No.: **062020-1950**

For: **MULTI-BAND RF TRANSCEIVER WITH PASSIVE REUSE IN ORGANIC SUBSTRATES**

RESPONSE TO NON-FINAL OFFICE ACTION

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit the following amendments and remarks to the non-final Office Action mailed from the United States Patent and Trademark Office on May 5, 2008 (Paper No. 20080401).

AUTHORIZATION TO DEBIT ACCOUNT

It is not believed that additional fees are required, beyond those which may otherwise be provided for in the documents accompanying this paper. However, in the event that additional fees are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. §1.136(a), and any fees required (including fees for net additions of claims) are hereby authorized to be charged to 20-0778.

STATUS OF THE CLAIMS

1. (Currently Amended) A multi-band RF device operable at a first frequency and a second frequency different from the first frequency, comprising:

an active device;

a first passive network in communication with the active device, the first passive network comprising a first matching network at an input of the active device;

a second passive network in communication with the active device, the second passive network comprising a second matching network at an output of the active device; and

an organic-based substrate having at least two metal layers, wherein the two metal layers are patterned to form at least a portion of the first passive network and the second passive network, wherein impedances of the first and second passive networks are different at the first frequency than the second frequency.

2. (Original) The multi-band RF device of claim 1, wherein the first and second passive networks comprise resonant circuits, and wherein the impedances of the first and second networks comprise reactance.

3. (Original) The multi-band RF device of claim 2, wherein the active device is a bipolar junction transistor, wherein the multi-band RF device is an oscillator, and wherein a first oscillation signal at the first frequency and a second oscillation signal at the second frequency are simultaneously generated.

4. (Canceled).

5. (Currently Amended) The multi-band RF device of claim 1 ~~claim 4~~, wherein the active device is a bipolar junction transistor and wherein the multi-band device is a low noise amplifier operable for providing power gain at the first frequency and the second frequency.

6-15. (Canceled).

16. (Currently Amended) A multi-band low noise amplifier for use in an RF application, comprising:

an active device;

a first matching network in communication with the active device, wherein an impedance of the first matching network at a first frequency is different than the impedance of the first matching network at a second frequency;

a second matching network in communication with the active device, wherein an impedance of the second matching network at the first frequency is different than the impedance of the second matching network at the second frequency; and

a multi-layer organic-based substrate having at least one metal layer, wherein the first matching network and the second matching network are formed on the at least one metal layer and wherein the active device is mounted on the multi-layer organic substrate, thereby allowing the an output of the multi-band low noise amplifier to have desired power gains at the first frequency and the second frequency based at least in part on each of the first and second matching networks having the different reactance at the first frequency and the second frequency.

17. (Original) The multi-band amplifier of claim 16, wherein the active device is a bipolar junction transistor.

18. (Original) The multi-band amplifier of claim 16, wherein the multi-layer organic-based substrate comprises at least one of hydrocarbon and liquid crystalline polymer.

19. (Original) The multi-band amplifier of claim 18, wherein the first matching network is positioned at an input of the multi-band amplifier and the second matching network is positioned at an output of the multi-band amplifier.

20. (Original) The multi-band amplifier of claim 19, wherein the first matching network minimizes the noise figure for the multi-band amplifier at the input at both the first frequency and the second frequency.

21. (Original) The multi-band amplifier of claim 20, wherein the second matching network maximizes the desired power gains for the multi-band amplifier at the output at both the first frequency and the second frequency.

22-32. (Canceled).

33. (New) The multi-band RF device of claim 1, wherein the organic-based substrate comprises liquid crystalline polymer.

34. (New) The multi-band RF device of claim 1, wherein the active device is a field effect transistor.

35. (New) The multi-band RF device of claim 1, wherein the first passive network comprises a component embedded in the organic-based substrate.

36. (New) The multi-band RF device of claim 1, wherein at least one of the metal layers is patterned to form at least a portion of a component included in the first passive network.

37. (New) The multi-band RF device of claim 1, wherein the second passive network comprises a component embedded in the organic-based substrate.

38. (New) The multi-band RF device of claim 1, wherein at least one of the metal layers is patterned to form at least a portion of a component included in the second passive network.

39. (New) The multi-band amplifier of claim 16, wherein the first matching network comprises a component embedded in the organic-based substrate.

40. (New) The multi-band amplifier of claim 16, wherein at least one of the metal layers is patterned to form at least a portion of a component included in the first matching network.

41. (New) The multi-band amplifier of claim 16, wherein the second matching network comprises a component embedded in the organic-based substrate.

42. (New) The multi-band amplifier of claim 16, wherein at least one of the metal layers is patterned to form at least a portion of a component included in the second matching network.

REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed on May 5, 2008 (Paper No. 20080401). Upon entry of this response, claims 1-3, 5, 16-21, and 33-42 are pending in the application. In this response, claims 1, 5, and 16 have been amended and claims 4, 6-15, and 22-32 have been canceled without prejudice, waiver, or disclaimer. Claims 33-42 have been added. Applicants respectfully request that the amendments being filed herewith be entered and request reconsideration and allowance of all pending claims.

I. Allowable Subject Matter

Applicants appreciate the Examiner's allowance of claims 16-21. Applicants also acknowledge the Examiner's indication in the Office Action that claims 4 and 5 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims. Independent claim 1 is amended to include the limitations of dependent claim 4, such that claim 4 is now an independent claim including all of the limitations of its base claim. Dependent claim 5 is amended to depend from amended independent claim 1, and is therefore allowable as a matter of law for at least the reason that the dependent claim 5 contains all features of independent claim 1. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Accordingly, the Examiner is respectfully requested to place claims 1 and 5 in condition for allowance.

Applicants wish to clarify that the amendments to claim 1 are made for purposes of presenting claim 4 in an independent claim format as requested by the Examiner, and not in response to any rejections made based on cited art. Because a dependent claim as a matter of law inherently contains all of the limitations of its respective parent independent claim, and any intervening claims, the amendments to claim 1 do not narrow the scope of claims 4 and 5 as originally filed.

Applicants have also amended independent claim 16 to correct a typographical error, specifically, to add the word "network" after "the second matching". Applicants respectfully submit that the application is in condition for allowance.

II. Claim Rejections under 35 U.S.C. §102(e)

Claims 1-3 have been rejected under 35 U.S.C. § 102(e) as allegedly anticipated by *Jensen* (U.S. Patent No. 6,075,995, hereafter "*Jensen*"). As noted above, claim 1 has been amended to include the allowable limitations of dependent claim 4. Since amended claim 1 is allowable, Applicants submit that claims 2-3 are allowable for at least the reason that each depends from an allowable claim. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q. 2d 1596, 1598 (Fed. Cir. 1988). Therefore, Applicants request that the rejection of claims 1-3 be withdrawn.

III. Newly Added Claims

New claims 33-42 are based on subject matter that is explicit and/or inherent within the description of the specification and/or the drawings. Applicants submit that no new matter has been added in the new claims 33-42, and that new claims 33-42 are allowable over the cited references. Furthermore, Applicants respectfully submit that claims 33-38 and 39-42, which depend either directly or indirectly from independent claim 1 and 16, respectively, are allowable for at least the reason that each depends from an allowable independent claim. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). Therefore, Applicants request the Examiner to enter and allow the above new claims.

CONCLUSION

Applicants respectfully request that all outstanding objections and rejections be withdrawn and that this application and presently pending claims 1-3, 5, 16-21, and 33-42 be allowed to issue. Any statements in the Office Action that are not explicitly addressed herein are not intended to be admitted. If the Examiner has any questions or comments regarding Applicants' response, the Examiner is encouraged to telephone Applicants' undersigned counsel.

Respectfully submitted,

By: _____
Randy R. Schoen, Reg. No. 62,440

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.
600 Galleria Parkway, SE
Suite 1500
Atlanta, Georgia 30339-5948
Tel: (770) 933-9500
Fax: (770) 951-0933

Electronic Acknowledgement Receipt

EFS ID:	3714694
Application Number:	11114733
International Application Number:	
Confirmation Number:	1270
Title of Invention:	Multi-band RF transceiver with passive reuse in organic substrates
First Named Inventor/Applicant Name:	Vinu Govind
Customer Number:	24504
Filer:	Randy Richard Schoen
Filer Authorized By:	
Attorney Docket Number:	062020-1950
Receipt Date:	01-AUG-2008
Filing Date:	25-APR-2005
Time Stamp:	11:15:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment - After Non-Final Rejection	00755498.PDF	250324 bb92c39ba2e6d0572e308aead00b6fad144cb413	no	8

Warnings:	
Information:	

Total Files Size (in bytes):	250324

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/114,733	04/25/2005	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☒ RATE ($)	SMALL ENTITY ☒ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 08/01/2008	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 20	Minus	** 32	= 0	X $25 =	0	OR	X $ =	
Independent (37 CFR 1.16(h))	* 2	Minus	***4	= 0	X $105 =	0	OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE	

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/DENISE HOPKINS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/114,733	04/25/2005	Vinu Govind	062020-1950	1270

24504 7590 05/05/2008

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
600 GALLERIA PARKWAY, S.E.
STE 1500
ATLANTA, GA 30339-5994

EXAMINER	
PHU, SANH D	

ART UNIT	PAPER NUMBER
2618	

MAIL DATE	DELIVERY MODE
05/05/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/114,733	GOVIND ET AL.	
	Examiner	Art Unit	
	/Sanh D. Phu/	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *the Amendment filed on 1/18/2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 16-21* is/are pending in the application.

4a) Of the above claim(s) *6-15 and 22-32* is/are withdrawn from consideration.

5)☒ Claim(s) *16-21* is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☒ Claim(s) *4 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/8/05,3/16/06,11/2/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The IDS filed 8/8/05, 3/16/06 and 11/2/06 have been considered and recorded in the file.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Jensen (6,075,995).

Regarding to claim 1, Jensen teaches a multi-band RF device (3, fig.1)operable at a first frequency (900MHz, GSM) and a second frequency different (1800MHZ, DCS) from the first frequency, comprising: an active device (1, Fig. 1); a first passive network (L1, L2, C3, C4, C5)(fig. 3) in communication with the active device (1, Fig. 2); a second passive network (L3, L4, C15 and C16)(Fig. 4) in communication with the active device (1, Fig. 2); and an organic-based substrate having at least two metal layers (two layers substrate, see col. 1, lines 50-64), wherein the two metal layers are patterned to form at least a portion of the first passive network and the second passive network (see col. 1, lines 50-64), wherein impedances of the first and second passive networks are different at the first frequency than the second frequency (see fig. 3,4 and col. 5, line 13 to col. 7, line 45).

Regarding to claim 2, Jensen teaches the multi-band RF device wherein the first and second passive networks comprise resonant circuits (LC network), and wherein the impedances of the first and second networks comprise reactance (see fig. 3,4 and col. 5, line 13 to col. 7, line 45).

Regarding to claim 3, Jensen teaches the multi-band RF device wherein the active device is a bipolar junction transistor (T1, T2, T3, T4 and etc...)(Fig. 2A and text portion), wherein the multi-band RF device is an oscillator, and wherein a first oscillation signal at the first frequency and a second oscillation signal at the second frequency are simultaneously generated (amplifier 4 and 6 in fig. 2 operates at two different frequency simultaneously)(see col. Line 29).

Allowable Subject Matter

4. 16-21 are allowed.

5. Claim 4 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sanh D Phu whose telephone number (571)272-7857. The examiner can normally be reached on 8:00-16:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on 571-272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sanh D. Phu/
Primary Examiner
Division 2618

SP

Notice of References Cited	Application/Control No. 11/114,733	Applicant(s)/Patent Under Reexamination GOVIND ET AL.	
	Examiner /Sanh D. Phu/	Art Unit 2618	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,075,995	06-2000	Jensen, Niels J.	455/552.1
*	B	US-7,253,681	08-2007	Ichitsubo et al.	330/140
*	C	US-7,224,232	05-2007	Paul et al.	330/307
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

OIPE IAP28
NOV 0 2 2006
PATENT & TRADEMARK OFFICE

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Govind, et al.

Serial No.: 11/114,733

Filed: 04/25/2005

For: Multi-Bamd RF Receiver with Passive Reuse in Organic Substrates

Confirmation No.: 1270

Group Art Unit: 2681

Examiner:

Docket No.: 062020-1950

SECOND SUPPLEMENTAL
INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

This information disclosure statement is filed in accordance with 37 C.F.R. §§ 1.56, 1.97, and 1.98, and specifically:

☒ under 37 CFR 1.97(b), or
(within Three months of filing national application; or date of entry of international application; or before mailing date of first office action on the merits; whichever occurs last)

☐ under 37 CFR 1.97(c) together with either a:
- ☐ Statement Under 37 C.F.R. 1.97(e), or
- ☐ a $180.00 fee under 37 CFR 1.17(p), or

(After the CFR 1.97(b) time period, but before the final office action or notice of allowance, whichever occurs first)

☐ under 37 CFR 1.97(d) together with a:
- ☐ Statement under 37 CFR 1.97(e), and
- ☐ a $180.00 petition fee set forth in 37 CFR 1.17(p).

(Filed after final office action or notice of allowance, whichever occurs first, but before payment of the issue fee)

Enclosed is a check in the amount of $.

Enclosed is Credit Card Payment Form (PTO-2038) in the amount of $.

Please charge $ to deposit account . At any time during the pendency of this application, please charge any fees required to Deposit Account 20-0778 pursuant to 37 CFR 1.25. The Commissioner is hereby requested to credit any overpayment to Deposit Account No. 20-0778.

☒ Applicant(s) submit herewith *Form PTO 1449A - Information Disclosure Statement by Applicant* together with copies (where required) of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may or may not be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56. As required by 37 C.F.R. §1.98(a), a legible copy of each document is provided.

☐ A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individual(s) designated in 37 CFR 1.56(c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on the form PTO 1449 and is enclosed herewith.

The following rights are reserved by the Applicant(s): the right to establish the patentability of the claimed invention over any of the listed documents should they be applied as reference, and/or the right to prove that some of these documents may not be prior art, and/or the right to prove that some of these documents may not be enabling for the teachings they purport to offer.

This statement should not be construed as a representation that an exhaustive search has been made, or that information more material to the examination of the present application does not exist. Any statements or identifications regarding the relevance of any portion(s) of cited references should not be construed as a representation that the most relevant portion(s) have been identified, and the absence of such statements or identifications should not be construed as representations that there are no relevant portion(s). The Examiner is specifically requested not to rely solely on the materials submitted herewith. The Examiner is requested to conduct an independent and thorough review of the documents, and to form independent opinions as to their significance.

It is requested that the information disclosed herein be made of record in this application and that the Examiner initial and return a copy of the enclosed PTO-1449 to indicate the documents have been considered.

Respectfully Submitted,

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.

By: _____

Scott A. Horstemeyer, Reg. No. 34,183

100 Galleria Parkway, Suite 1750
Atlanta, Georgia 30339-5948
770-933-9500

CERTIFIED MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as **"First Class Mail,"** in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 10-31-06

_____
Signature

OIPE IAP28 NOV 02 2006 PATENT & TRADEMARK OFFICE

PTO/SB/08A (07-05)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	11/114,733
Filing Date	04/25/05
First Named Inventor	Govind
Art Unit	2681
Examiner Name	
Attorney Docket Number	062020-1950

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/S.P./	1	US- 4,745,215	0517/1988	Cox, et al.	
/S.P./	2	US- 5,450,290	09/12/1995	Boyko, et al.	
/S.P./	3	US- 6,079,100	06/27/2000	Farquhar, et al.	
/S.P./	4	US- 2002/0157864 A1	10/31/2002	Koyama, et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature	/Sanh Phu/	Date Considered	03/18/2008

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11114733	GOVIND ET AL.
	Examiner	**Art Unit**
	/Sanh D Phu/	2618

SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
455	168.1, 252.1, 73, 552.1	4/2/08	SP
257	723,724	4/2/08	SP

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
EAST (Text Search)	4/2/08	SP

INTERFERENCE SEARCH			
Class	**Subclass**	**Date**	**Examiner**

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 1270

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/114,733	04/25/2005 RULE	455	2618	062020-1950

APPLICANTS

Vinu Govind, Decatur, GA;
Sidharth Dalmia, Norcross, GA;
Amit Bavisi, Atlanta, GA;
Venkatesh Sundraram, Norcross, GA;
Madhavan Swaminathan, Marietta, GA;
George White, Marietta, GA;

**** CONTINUING DATA ***************************

This appln claims benefit of 60/565,254 04/23/2004
and is a CIP of 10/402,313 03/28/2003 PAT 6,900,708

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **
05/19/2005

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
❑ Yes ☑ No	❑ Yes ☑ No	/SANH D PHU/ Examiner's Signature	❑ Initials	GA	49	32	4

ADDRESS

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
600 GALLERIA PARKWAY, S.E.
STE 1500
ATLANTA, GA 30339-5994
UNITED STATES

TITLE

Multi-band RF transceiver with passive reuse in organic substrates

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
965	No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	❑ All Fees ❑ 1.16 Fees (Filing) ❑ 1.17 Fees (Processing Ext. of time) ❑ 1.18 Fees (Issue) ❑ Other _____ ❑ Credit

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11114733	GOVIND ET AL.
	Examiner	Art Unit
	/Sanh D Phu/	2618

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	04/02/2008								
	1	✓								
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	32	N								

OIPE MAR 16 2006 PATENT & TRADEMARK OFFICE

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Govind, et al.

Serial No.: 11/114,733

Filed: 04/25/2005

For: Multi-Bamd RF Receiver with Passive Reuse in Organic Substrates

Confirmation No.: 1270

Group Art Unit: 2681

Examiner:

Docket No.: 062020-1950

SUPPLEMENTAL
INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

This information disclosure statement is filed in accordance with 37 C.F.R. §§ 1.56, 1.97, and 1.98, and specifically:

☒ under 37 CFR 1.97(b), or
(within Three months of filing national application; or date of entry of international application; or before mailing date of first office action on the merits; whichever occurs last)

☐ under 37 CFR 1.97(c) together with either a:
- ☐ Statement Under 37 C.F.R. 1.97(e), or
- ☐ a $180.00 fee under 37 CFR 1.17(p), or

(After the CFR 1.97(b) time period, but before the final office action or notice of allowance, whichever occurs first)

☐ under 37 CFR 1.97(d) together with a:
- ☐ Statement under 37 CFR 1.97(e), and
- ☐ a $180.00 petition fee set forth in 37 CFR 1.17(p).

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Enclosed is Credit Card Payment Form (PTO-2038) in the amount of $.

Please charge $ to deposit account . At any time during the pendency of this application, please charge any fees required to Deposit Account 20-0778 pursuant to 37 CFR 1.25. The Commissioner is hereby requested to credit any overpayment to Deposit Account No. 20-0778.

☒ Applicant(s) submit herewith *Form PTO 1449A - Information Disclosure Statement by Applicant* together with copies (where required) of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may or may not be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56. As required by 37 C.F.R. §1.98(a), a legible copy of each document is provided.

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Respectfully Submitted,

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.

By: _____

Scott A. Horstemeyer, Reg. No. 34,183

100 Galleria Parkway, Suite 1750
Atlanta, Georgia 30339-5948
770-933-9500

CERTIFIED MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as **"First Class Mail,"** in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 3-13-06

_____
Signature

OIPE IAP17 MAR 16 2006 PATENT & TRADEMARK OFFICE

PTO/SB/08A (07-05)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	11/114,733
Filing Date	04/25/05
First Named Inventor	Govind
Art Unit	2681
Examiner Name	
Attorney Docket Number	062020-1950

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/S.P./	1	US- 5,401,913	03/1995	Gerber, et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature	/Sanh Phu/	Date Considered	03/18/2008

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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OIPE JC56
AUG 0 8 2005
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IFW

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Govind, et al.

Serial No.: 11/114,733

Filed: 04/25/2005

For: Multi-Bamd RF Receiver with Passive Reuse in Organic Substrates

Confirmation No.: 1270

Group Art Unit: 2681

Examiner:

Docket No.: 062020-1950

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

This information disclosure statement is filed in accordance with 37 C.F.R. §§ 1.56, 1.97, and 1.98, and specifically:

☒ under 37 CFR 1.97(b), or
(within Three months of filing national application; or date of entry of international application; or before mailing date of first office action on the merits; whichever occurs last)

☐ under 37 CFR 1.97(c) together with either a:
- ☐ Statement Under 37 C.F.R. 1.97(e), or
- ☐ a $180.00 fee under 37 CFR 1.17(p), or

(After the CFR 1.97(b) time period, but before the final office action or notice of allowance, whichever occurs first)

☐ under 37 CFR 1.97(d) together with a:
- ☐ Statement under 37 CFR 1.97(e), and
- ☐ a $180.00 petition fee set forth in 37 CFR 1.17(p).

(Filed after final office action or notice of allowance, whichever occurs first, but before payment of the issue fee)

Enclosed is a check in the amount of $.

Enclosed is Credit Card Payment Form (PTO-2038) in the amount of $.

Please charge $ to deposit account . At any time during the pendency of this application, please charge any fees required to Deposit Account pursuant to 37 CFR 1.25. The Commissioner is hereby requested to credit any overpayment to Deposit Account No. .

☒ Applicant(s) submit herewith *Form PTO 1449A - Information Disclosure Statement by Applicant* together with copies (where required) of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may or may not be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56. As required by 37 C.F.R. §1.98(a), a legible copy of each document is provided.

☐ A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individual(s) designated in 37 CFR 1.56(c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on the form PTO 1449 and is enclosed herewith.

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The following rights are reserved by the Applicant(s): the right to establish the patentability of the claimed invention over any of the listed documents should they be applied as reference, and/or the right to prove that some of these documents may not be prior art, and/or the right to prove that some of these documents may not be enabling for the teachings they purport to offer.

This statement should not be construed as a representation that an exhaustive search has been made, or that information more material to the examination of the present application does not exist. Any statements or identifications regarding the relevance of any portion(s) of cited references should not be construed as a representation that the most relevant portion(s) have been identified, and the absence of such statements or identifications should not be construed as representations that there are no relevant portion(s). The Examiner is specifically requested not to rely solely on the materials submitted herewith. The Examiner is requested to conduct an independent and thorough review of the documents, and to form independent opinions as to their significance.

It is requested that the information disclosed herein be made of record in this application and that the Examiner initial and return a copy of the enclosed PTO-1449 to indicate the documents have been considered.

Respectfully Submitted,

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.

By: _____

Scott A. Horstemeyer, Reg. No. 34,183

100 Galleria Parkway, Suite 1750
Atlanta, Georgia 30339-5948
770-933-9500

CERTIFIED MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as **"First Class Mail,"** in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 8-5-05

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 7

Complete if Known	
Application Number	11/114,733
Filing Date	04/25/05
First Named Inventor	Govind
Art Unit	2681
Examiner Name	
Attorney Docket Number	062020-1950

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US- 5,106,461	04/21/1992	Volfson,e t al.	
	2	US- 5,247,377	09/21/1993	Omeis, et al.	
	3	US- 5,323,128	06/21/1994	Ishizaki, et al.	
	4	US- 5,349,314	09/20/1994	Shimizu, et al.	
	5	US- 5,373,271	12/13/1994	Hirai, et al.	
	6	US- 5,396,201	03/07/1995	Ishizaki, et al.	
	7	US- 5,416,454	05/16/1995	McVeety	
	8	US- 5,497,337	03/05/1996	Ponnapalli, et al.	
	9	US- 5,517,751	05/21/1996	Bross, et al.	
	10	US- 5,545,916	08/13/1996	Koullias	
	11	US- 5,559,360	09/24/1996	Chiu, et al.	
	12	US- 5,635,892	06/03/1997	Ashby, et al.	
	13	US- 5,654,681	09/05/1997	Ishizaki, et al.	
	14	US- 5,668,511	09/16/1997	Furutani, et al.	
	15	US- 5,79,414	10/211997	Akashi, et al.	
	16	US- 5,716,663	02/10/1998	Capote, et al.	
	17	US- 5,719,354	02/17/1998	Jester, et al.	
	18	US- 5,719,539	02/17/1998	Ishizaki, et al.	
	19	US- 5,720,898	02/24/1998	Nohira, et al.	

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	20	WO 01/97582 A1	12/20/01	Shimokoshi, et al.		
	21	EP 0 506 476 B1	03/27/92	NGK Insulators Ltd.		✓
	22	EP 0 510 971 B1	04/23/92	Matsushita Electric Ind.		✓
	23	JP 09 130103 A	10/31/95	Endo, Toshiyuki		
	24	EP 1 235 235 A1	02/22/02	TDK Corporation		✓
	25	EP 0 645 952 A1	09/08/94	Rogers Corporation		✓

Examiner Signature		Date Considered	

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(Use as many sheets as necessary)

Sheet 2 of 7

Complete if Known	
Application Number	11/114,733
Filing Date	04/25/05
First Named Inventor	Govind
Art Unit	2681
Examiner Name	
Attorney Docket Number	062020-1950

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	26	US- 5,770,986	06/23/1998	Tonegawa, et al.	
	27	US- 5,801,100	10/01/1998	Lee, et al.	
	28	US- 5,818,313	10/06/1998	Estes, et al.	
	29	US- 5,844,299	12/01/1998	Merrill, et al.	
	30	US- 5,917,244	06/29/1999	Lee, et al.	
	31	US- 5,999,243	12/07/1999	Kameyama, et al.	
	32	US- 6,008,102	12/28/1999	Alford, et al.	
	33	US- 6,026,286	02/15/2000	Long	
	34	US- 6,040,226	03/21/2000	Wojnarowski, et al.	
	35	US- 6,051,289	04/18/2000	Tsujimoto, et al.	
	36	US- 6,093,599	06/25/2000	Lee, et al.	
	37	US- 6,114,925	09/05/2000	Lo	
	38	US- 6,127,905	10/03/2000	Horie	
	39	US- 6,166,799	12/26/2000	Kameyama, et al.	
	40	US- 6,177,853 B1	01/2320/01	Nagatomi, et al.	
	41	US- 6,191,666 B1	02/20/2001	Sheen	
	42	US- 6,191,669 B1	02/20/2001	Shigemura	
	43	US- 6,225,696 B1	05/01/2001	Hathaway, et al.	
	44	US- 6,255,714 B1	07/03/2001	Kossives, et al.	

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	45	EP 1 411 553 A1	04/21/2004	Hitachi, Ltd.		✓
	46	JP Abstract - JP 07161583	06/26/1995	Murata Mfg Co. Ltd	Abstract Only	✓
	47	WO 01/95679 A1	12/13/2001	Bluetronics AB		✓

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Sheet 3 of 7

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	48	US- 5,739,193	04/14/1998	Walpita, et al.	
	49	US- 6,380,608	04/30/2002	Bentley	
	50	US- 6,259,148 B1	07/10/2001	Bartush, et al.	
	51	US- 6,261,872 B1	07/17/2001	Hathaway, et al.	
	52	US- 6,281,430 B1	08/28/2001	Lupo, et al.	
	53	US- 6,287,931 B1	09/11/2001	Chen	
	54	US- 6,303,423 B1	10/16/2001	Lin	
	55	US- 6,395,374 B1	05/28/2002	McAndrew, et al.	
	56	US- 6,445,266 B1	09/03/2002	Nagatomi, et al.	
	57	US- 2001/0004228 A1	06/21/2001	Hirai, et al.	
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	60	US- 2002/0048930 A1	04/25/2002	Lin	
	61	US- 2002/0064701	05/30/2002	Hand et al.	
	62	US- 2002/0064922 A1	05/30/2002	Lin	
	63	US- 2002/0074158 A1	06/20/2002	St. Lawrence et al.	
	64	US- 2002-0076538 A1	06/20/2002	St. Lawrence et al.	
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Sheet 4 of 7

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First Named Inventor	Govind
Art Unit	2681
Examiner Name	
Attorney Docket Number	062020-1950

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	67	US- 6,583,687 B2	06/24/2003	Nosaka	
	68	US- 5,521,564	05/28/1996	Kaneko, et al.	
	69	US- 6,528,732 B1	03/04/2003	Okubora, et al.	
	70	US- 2002/0172021 A1	11/21/2002	Seri, et al.	
	71	US- 6,421,225 B2	07/16/2002	Bergstedt	
	72	US- 2001/0016980 A1	08/30/2001	Bergstedt	
	73	US- 6,259,037 B1	07/10/2001	Feilchenfeld, et al.	
	74	US- 6,249,962	06/26/2001	Bergstedt	
	75	US- 6,171,716	01/09/2001	Sasaki, et al.	
	76	US- 5,955,931	09/21/1999	Kaneko, et al.	
	77	US- 5,703,544	12/30/1997	Hays III	
	78	US- 5,610,433	03/11/1999	Merrill, et al.	
	79	US- 5,162,257	11/10/1992	Yung	
	80	US- 5,532,667	07/02/1996	Haertling, et al.	
	81	US- 6,492,886 B1	12/10/2002	Kushitani, et al.	
	82	US- 6,021,050	02/01/2000	Ehman, et al.	
	83	US- 6,625,037 B2	09/23/2003	Nakatani, et al.	
	84	US- 6,031,727	02/29/2000	Deusman, et al.	
	85	US- 5,270,493	12/14/1993	Inoue, et al.	

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	86	US- 6,153,290	11/28/2000	Sunahara	
	87	US- 5,384,434	01/24/1995	Mandai,e t al.	
	88	US- 6,005,197	12/21/1999	Kola, et al.	
	89	US- 6,713,162	03/30/2004	Takaya, et al.	
	90	US- 2004/0000425 A1	01/01/2004	White, et al.	
	91	US- 2004/0034489 A1	02/19/2004	Ogino, et al.	
	92	US- 2002/0195270 A1	12/26/2002	Okubora, et al.	
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Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.P./

PTO/SB/08B (07-05)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 6 of 7

Complete if Known	
Application Number	11/114,733
Filing Date	04/25/05
First Named Inventor	Govind
Art Unit	2681
Examiner Name	
Attorney Docket Number	062020-1950

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	93	http://sbir.gsfc.nasa.gov/SBIR/successes/ss/110text.html; Liquid Crystal Polymers for Printed Wiring Boards.	✓
	94	www.yamaichi.us/yflex.html; Flexible Printed Circuit - YFLEX	✓
	95	www.stneasy.org.tmp; Display from INSPEC; Taoka, M., Kanetaka, T., December 4, 2002	✓
	95	HONG, J.S., et al., "Microstrip Filters for RF/Microwave Applications", Wiley-Interscience PUblication, 2001, pp. 121-159.	✓
	97	SON, M.H., et al., "Low-Cost Realization of ISM Band Pass Filters Using Integrated Combine Structures," 2000, (4 pages).	✓
	98	MATIJASEVIC, G., et al., "MCM-L Substrates Fabricated Using Patterned TLPS Conductive Composites," 1997 International Conference on Multichip Modules, April 2, 1997, pp. 64-69	✓
	99	CHARLES, H.K., "Packaging with Multichip Modules", 1992 IEEE/CHMT International Electronics Manufacturing Technology Symposium, pp. 206-210.	✓
	100	MIN., S.H., et al., "Design, Fabrication, Measurement and Modeling of Embedded Inductors in Laminate Technology", ASME Int'l Elect. Pkg. Technical Conf, 2001 pp1-5	✓
	101	DALMIA, S., et al. "Modeling RF Passive Circuits Using Coupled LInes and Scable Modles, 2001 ECTC, pp. 816-823.	✓
	102	ALVIN, L.S. Loke, et al. "Evaluation of Copper Penetration in Low-K Polymer Dielectrics by Bias-Temperature Stress", MRS Spring Meeting, Symp. N/O, Paper 04.4, 04/07/1999.	✓

Examiner Signature		Date Considered	

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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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PTO/SB/08B (07-05)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 7 of 7

Complete if Known	
Application Number	11/114,733
Filing Date	04/25/05
First Named Inventor	Govind
Art Unit	2681
Examiner Name	
Attorney Docket Number	062020-1950

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	103	WANG, et al., "A Full-Wave Analysis Model for Uniplanar Circuits with Lumped Elements", IEEE Transactions on Microwave Theory and Techniques, Vol. 51, NO. 1., Jan. 2003	✓
		.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.P./

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:		Confirmation No.:	**1270**
	Govind *et al.*	Group Art Unit:	**2618**
Serial No.:	**11/114,733**	Examiner:	**Phu, Sanh D**
Filed:	**April 25, 2005**	Docket No.:	**062020-1950**

For: **Multi-Band RF Transceiver with Passive Reuse in Organic Substrates**

RESPONSE TO RESTRICTION REQUIREMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit the following amendments and remarks to the non-final Office Action mailed from the United States Patent and Trademark Office on December 18, 2007 (Paper No. 20071206).

AUTHORIZATION TO DEBIT ACCOUNT

It is not believed that additional fees are required, beyond those which may otherwise be provided for in the documents accompanying this paper. However, in the event that additional fees are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. §1.136(a), and any fees required (including fees for net additions of claims) are hereby authorized to be charged to 20-0778.

STATUS OF THE CLAIMS

1. (Original) A multi-band RF device operable at a first frequency and a second frequency different from the first frequency, comprising:

an active device;

a first passive network in communication with the active device;

a second passive network in communication with the active device; and

an organic-based substrate having at least two metal layers, wherein the two metal layers are patterned to form at least a portion of the first passive network and the second passive network, wherein impedances of the first and second passive networks are different at the first frequency than the second frequency.

2. (Original) The multi-band RF device of claim 1, wherein the first and second passive networks comprise resonant circuits, and wherein the impedances of the first and second networks comprise reactance.

3. (Original) The multi-band RF device of claim 2, wherein the active device is a bipolar junction transistor, wherein the multi-band RF device is an oscillator, and wherein a first oscillation signal at the first frequency and a second oscillation signal at the second frequency are simultaneously generated.

4. (Original) The multi-band RF device of claim 1, wherein the first passive network comprises a first matching network at an input of the active device and wherein the second passive network comprises a second matching network at an output of the active device.

5. (Original) The multi-band RF device of claim 4, wherein the active device is a bipolar junction transistor and wherein the multi-band device is a low noise amplifier operable for providing power gain at the first frequency and the second frequency.

6. (Original) An RF multi-band oscillator for simultaneously generating oscillation signals at a first frequency and a second frequency for a multi-band transceiver, comprising:

an organic layer having a top surface and a bottom surface;

a first metal layer opposite the top surface;

a second metal layer opposite the bottom surface, wherein the first metal layer and the second metal layer are patterned to form a first resonator and a second resonator, wherein a reactance of the first resonator at the first frequency differs from a reactance at the second frequency and wherein a reactance of the second resonator at the first frequency differs from a reactance at the second frequency; and

an active device in communication with the first resonator and the second resonator to form a feedback network, thereby simultaneously generating oscillation signals at the first frequency and the second frequency.

7. (Original) The multi-band oscillator of claim 6, wherein the organic layer comprises liquid crystalline polymer.

8. (Original) The multi-band oscillator of claim 6, wherein the reactance of each of the first resonator and second resonator is substantially constant at the first frequency and the second frequency.

9. (Original) The multi-band oscillator of claim 8, wherein the reactance of at least one of the first resonator and second resonator at the first frequency is inversely proportional to the reactance at the second frequency.

10. (Original) The multi-band oscillator of claim 9, wherein the first and second resonators comprise at least one inductor and at least one capacitor.

11. (Original) The multi-band oscillator of claim 10, wherein the first resonator is a parallel resonator and the second resonator is a series resonator.

12. (Original) The multi-band oscillator of claim 8, wherein the active device is a transistor.

13. (Original) The multi-band oscillator of claim 12, wherein the transistor is a bipolar junction transistor.

14. (Original) The multi-band oscillator of claim 6, further comprising a filter formed on at least one of the first patterned metal layer and the second patterned metal layer, wherein the filter separates the generated oscillation signals into distinct oscillation signals at the first frequency and the second frequency.

15. (Original) The multi-band oscillator of claim 14, wherein the filter is an inductively-coupled dual resonator type filter.

16. (Original) A multi-band low noise amplifier for use in an RF application, comprising:

an active device; a first matching network in communication with the active device, wherein an impedance of the first matching network at a first frequency is different than the impedance of the first matching network at a second frequency;

a second matching network in communication with the active device, wherein an impedance of the second matching network at the first frequency is different than the impedance of the second matching network at the second frequency; and

a multi-layer organic-based substrate having at least one metal layer, wherein the first matching network and the second matching are formed on the at least one metal layer and wherein the active device is mounted on the multi-layer organic substrate, thereby allowing the an output of the multi-band low noise amplifier to have desired power gains at the first frequency and the second frequency based at least in part on each of the first and second matching networks having the different reactance at the first frequency and the second frequency.

17. (Original) The multi-band amplifier of claim 16, wherein the active device is a bipolar junction transistor.

18. (Original) The multi-band amplifier of claim 16, wherein the multi-layer organic-based substrate comprises at least one of hydrocarbon and liquid crystalline polymer.

19. (Original) The multi-band amplifier of claim 18, wherein the first matching network is positioned at an input of the multi-band amplifier and the second matching network is positioned at an output of the multi-band amplifier.

20. (Original) The multi-band amplifier of claim 19, wherein the first matching network minimizes the noise figure for the multi-band amplifier at the input at both the first frequency and the second frequency.

21. (Original) The multi-band amplifier of claim 20, wherein the second matching network maximizes the desired power gains for the multi-band amplifier at the output at both the first frequency and the second frequency.

22. (Original) An oscillator for use in an RF transceiver, comprising:

a first organic layer with a top surface and a bottom surface opposite the top surface;

a first conductive layer positioned on the top surface of the first organic layer;

a second conductive layer positioned on the bottom surface of the first organic layer;

a second organic layer positioned opposite the second conductive layer;

a plurality of passive devices patterned on at least one of the first conductive layer and the second conductive layer; and

at least one discrete active device positioned on the first conductive layer and in communication with at least a portion the plurality of passive devices, wherein a feedback network for the active device is created such the discrete active device becomes unstable and generates at least one signal at a particular frequency.

23. (Original) The oscillator of claim 22, wherein the first organic layer and the second organic layer comprise liquid crystalline polymer.

24. (Original) The oscillator of claim 23, wherein the first organic layer comprise polyphenyl ether.

25. (Original) The oscillator of claim 23, wherein the discrete active device a transistor.

26. (Original) The oscillator of claim 25, wherein the transistor is a field effect transistor.

27. (Original) The oscillator of claim 25, wherein the transistor is a bipolar junction transistor.

28. (Original) The oscillator of claim 25, wherein at least a portion of the plurality of passive devices comprise inductors and capacitors.

29. (Original) The oscillator of claim 28, wherein the portion of the plurality of passive devices comprise resistors.

30. (Original) The oscillator of claim 29, wherein the feedback network forms a resonant tank.

31. (Original) The oscillator of claim 25, wherein the first conductive layer comprises a coplanar ground.

32. (Original) The oscillator of claim 25, wherein at least a portion of the plurality of passive devices comprise a network for matching to a load.

REMARKS

This is a full and timely response to the outstanding non-final Office action of December 18, 2007 (Paper No. 20071206). The Examiner has required the Applicants to elect to prosecute one of two groups of claims identified in the Office Action. In response to the restriction requirement, Applicants respectfully elect to prosecute the claims of Group I, corresponding to claims 1-5 and 16-21, drawn to a multi-band low noise amplifier using an active device for use in an RF application, classified in class 455, subclass 921, without traverse.

Applicants respectfully request the Examiner to examine the claims of Group I. Applicants expressly reserve the right to present the non-elected claims, or variants thereof, in continuing applications to be filed subsequent to the present application. If the Examiner has any questions or comments regarding Applicants' response, the Examiner is encouraged to telephone Applicants' undersigned counsel.

Respectfully submitted,

By: _____
Scott A. Horstemeyer, Reg. No. 34,183

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.
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Fax: (770) 951-0933

Electronic Acknowledgement Receipt

EFS ID:	2735652
Application Number:	11114733
International Application Number:	
Confirmation Number:	1270
Title of Invention:	Multi-band RF transceiver with passive reuse in organic substrates
First Named Inventor/Applicant Name:	Vinu Govind
Customer Number:	24504
Filer:	Scott A. Horstemeyer/Cathy Allred
Filer Authorized By:	Scott A. Horstemeyer
Attorney Docket Number:	062020-1950
Receipt Date:	18-JAN-2008
Filing Date:	25-APR-2005
Time Stamp:	10:16:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	00643622.pdf	245057 9282f4b2602d7b68be983d9c893307042fca9c4e	no	8

Warnings:	
Information:	

Total Files Size (in bytes):	245057

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/114,733	04/25/2005	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☒ RATE ($)	SMALL ENTITY ☒ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 01/18/2008	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 32	Minus	** 32	= 0	X $25 =	0	OR	X $ =	
Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X $105 =	0	OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE	

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/THERESA I. OKON/

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/114,733	04/25/2005	Vinu Govind	062020-1950	1270

24504 7590 12/18/2007

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
600 GALLERIA PARKWAY, S.E.
STE 1500
ATLANTA, GA 30339-5994

EXAMINER	
PHU, SANH D	

ART UNIT	PAPER NUMBER
2618	

MAIL DATE	DELIVERY MODE
12/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/114,733	GOVIND ET AL.	
	Examiner	Art Unit	
	Sanh D. Phu	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2005*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-32* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-5, 16-21, drawn to multi-band low noise amplifier using active device for use in an RF application, illustrated by Fig. 35, classified in class 455, subclass 291.

II. Claims 6-15 and 22-32, drawn to multi-band oscillator for use in an RF transceiver, illustrated by Fig. 16A and 27, classified in class 455, subclass 318.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions [I] and [II] are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention

[II] has separate utility such as low noise amplifier using with active device and having desired power gains at the difference frequency. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement is traversed (37 CFR 1.143).

3. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sanh D. Phu whose telephone number

is (571)272-7857. The examiner can normally be reached on M-Fr from 8:00-16:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on (571) 272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Sanh D Phu
Primary Examiner
Art Unit 2618

12/05/07

SP

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
11/114,733	GOVIND ET AL.
Examiner	**Art Unit**
Sanh D. Phu	2618

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
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Claim		Date
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BIB DATA SHEET

CONFIRMATION NO. 1270

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/114,733	04/25/2005 RULE	455	2618	062020-1950

APPLICANTS

Vinu Govind, Decatur, GA;
Sidharth Dalmia, Norcross, GA;
Amit Bavisi, Atlanta, GA;
Venkatesh Sundraram, Norcross, GA;
Madhavan Swaminathan, Marietta, GA;
George White, Marietta, GA;

** **CONTINUING DATA** *************************

This appln claims benefit of 60/565,254 04/23/2004
and is a CIP of 10/402,313 03/28/2003 PAT 6,900,708

** **FOREIGN APPLICATIONS** *************************

** **IF REQUIRED, FOREIGN FILING LICENSE GRANTED** ** ** SMALL ENTITY **
05/19/2005

Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged ___ Examiner's Signature	☐ Met after Allowance ___ Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		GA	49	32	4

ADDRESS

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
600 GALLERIA PARKWAY
STE 1500
ATLANTA, GA 30339
UNITED STATES

TITLE

Multi-band RF transceiver with passive reuse in organic substrates

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
965	No.___________ to charge/credit DEPOSIT ACCOUNT No.___________ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other ___________ ☐ Credit

BIB (Rev. 05/07).

OIPE IAP28
NOV 0 2 2006
PATENT & TRADEMARK OFFICE

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Govind, et al.

Serial No.: 11/114,733

Filed: 04/25/2005

For: Multi-Bamd RF Receiver with Passive Reuse in Organic Substrates

Confirmation No.: 1270

Group Art Unit: 2681

Examiner:

Docket No.: 062020-1950

SECOND SUPPLEMENTAL
INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

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(within Three months of filing national application; or date of entry of international application; or before mailing date of first office action on the merits; whichever occurs last)

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Respectfully Submitted,

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.

By: _____

Scott A. Horstemeyer, Reg. No. 34,183

100 Galleria Parkway, Suite 1750
Atlanta, Georgia 30339-5948
770-933-9500

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(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	11/114,733
Filing Date	04/25/05
First Named Inventor	Govind
Art Unit	2681
Examiner Name	
Attorney Docket Number	062020-1950

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US- 4,745,215	0517/1988	Cox, et al.	
	2	US- 5,450,290	09/12/1995	Boyko, et al.	
	3	US- 6,079,100	06/27/2000	Farquhar, et al.	
	4	US- 2002/0157864 A1	10/31/2002	Koyama, et al.	
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Examiner Signature		Date Considered	

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Govind, et al.

Serial No.: 11/114,733

Filed: 04/25/2005

For: Multi-Bamd RF Receiver with Passive Reuse in Organic Substrates

Confirmation No.: 1270

Group Art Unit: 2681

Examiner:

Docket No.: 062020-1950

SUPPLEMENTAL
INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

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By: _____

Scott A. Horstemeyer, Reg. No. 34,183

100 Galleria Parkway, Suite 1750
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EX1002 / Page 104 of 416
Murata Manufacturing Co., Ltd.

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(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	11/114,733
Filing Date	04/25/05
First Named Inventor	Govind
Art Unit	2681
Examiner Name	
Attorney Docket Number	062020-1950

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Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US- 5,401,913	03/1995	Gerber, et al.	
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AUG 0 8 2005
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Govind, et al.

Serial No.: 11/114,733

Filed: 04/25/2005

For: Multi-Bamd RF Receiver with Passive Reuse in Organic Substrates

Confirmation No.: 1270

Group Art Unit: 2681

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OIPE JC99
AUG 0 8 2005
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By: _____

Scott A. Horstemeyer, Reg. No. 34,183

100 Galleria Parkway, Suite 1750
Atlanta, Georgia 30339-5948
770-933-9500

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AUG 0 8 2005
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PTO/SB/08A (07-05)
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Examiner Name	
Attorney Docket Number	062020-1950

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Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US- 5,106,461	04/21/1992	Volfson,e t al.	
	2	US- 5,247,377	09/21/1993	Omeis, et al.	
	3	US- 5,323,128	06/21/1994	Ishizaki, et al.	
	4	US- 5,349,314	09/20/1994	Shimizu, et al.	
	5	US- 5,373,271	12/13/1994	Hirai, et al.	
	6	US- 5,396,201	03/07/1995	Ishizaki, et al.	
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	11	US- 5,559,360	09/24/1996	Chiu, et al.	
	12	US- 5,635,892	06/03/1997	Ashby, et al.	
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	20	WO 01/97582 A1	12/20/01	Shimokoshi, et al.		
	21	EP 0 506 476 B1	03/27/92	NGK Insulators Ltd.		✓
	22	EP 0 510 971 B1	04/23/92	Matsushita Electric Ind.		✓
	23	JP 09 130103 A	10/31/95	Endo, Toshiyuki		
	24	EP 1 235 235 A1	02/22/02	TDK Corporation		✓
	25	EP 0 645 952 A1	09/08/94	Rogers Corporation		✓

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 2 of 7

Complete if Known	
Application Number	11/114,733
Filing Date	04/25/05
First Named Inventor	Govind
Art Unit	2681
Examiner Name	
Attorney Docket Number	062020-1950

U. S. PATENT DOCUMENTS

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	26	US- 5,770,986	06/23/1998	Tonegawa, et al.	
	27	US- 5,801,100	10/01/1998	Lee, et al.	
	28	US- 5,818,313	10/06/1998	Estes, et al.	
	29	US- 5,844,299	12/01/1998	Merrill, et al.	
	30	US- 5,917,244	06/29/1999	Lee, et al.	
	31	US- 5,999,243	12/07/1999	Kameyama, et al.	
	32	US- 6,008,102	12/28/1999	Alford, et al.	
	33	US- 6,026,286	02/15/2000	Long	
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	45	EP 1 411 553 A1	04/21/2004	Hitachi, Ltd.		✓
	46	JP Abstract - JP 07161583	06/26/1995	Murata Mfg Co. Ltd	Abstract Only	✓
	47	WO 01/95679 A1	12/13/2001	Bluetronics AB		✓

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Attorney Docket Number	062020-1950

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NON PATENT LITERATURE DOCUMENTS

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	102	ALVIN, L.S. Loke, et al. "Evaluation of Copper Penetration in Low-K Polymer Dielectrics by Bias-Temperature Stress", MRS Spring Meeting, Symp. N/O, Paper 04.4, 04/07/1999.	✓

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(54) Title: ADHESIVE FILM AND METHOD FOR MANUFACTURING MULTILAYER PRINTED WIRING BOARD COMPRISING THE SAME

(54) 発明の名称: 接着フィルム及びこれを用いた多層プリント配線板の製造法

(57) Abstract: An adhesive film for a multilayer printed wiring board, characterized in that the film has at least a layer A and a layer B both specified below and formed adjacently to each other and a heat-curing resin composition constituting the layer B contains 10 weight% of resin having a softening point lower than the laminating temperature and can be placed in a through hole and/or a via hole simultaneously with the lamination on a circuit board. An insulating layer excellent in mechanical strength can be readily introduced into a multilayer printed wiring board by a build-up method by using such an adhesive film, and a multilayer printed wiring board excellent in mechanical strength can be provided. Layer A: A heat-resistant resin layer made of at least one of the heat-resistant resins selected from among the group consisting of a polyimide, a liquid crystal polymer, an aramid resin, and polyphenylene sulfide and having a thickness of 2 to 30 μm. Layer B: A heat-curing resin composition layer containing an epoxy resin (component (a)) having two or more epoxy resin groups in a molecule and an epoxy curing agent (component (b)) and solid at normal temperature.

[続葉有]

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(57) 要約:

この出願には、 少なくとも下記のＡ層及びＢ層を隣接して有し、Ｂ層を構成する熱硬化性樹脂組成物が、ラミネート温度より軟化点の低い樹脂を１０重量％以上含有し、回路基板へのラミネートと同時にスルホール及び／又はビアホール内の樹脂充填を行うことが可能な熱硬化性樹脂組成物であることを特徴とする多層プリント配線板用の接着フィルムが開示されている。そして、このような接着フィルムを使用することによりビルドアップ工法による多層プリント配線板において機械強度に優れる絶縁層を簡便に導入することが可能となり、また機械強度に優れる多層プリント配線板を提供することが可能となる。

Ａ層：ポリイミド、液晶ポリマー、アラミド樹脂及びポリフェニレンスルフィドからなる群より選択される耐熱樹脂の少なくとも１種からなる厚さ２乃至３０μｍの耐熱樹脂層、

Ｂ層：少なくとも１分子中に２以上のエポキシ基を有するエポキシ樹脂（成分（ａ））及びエポキシ硬化剤（成分（ｂ））を含有する常温で固形状の熱硬化性樹脂組成物層。

明細書

接着フィルム及びこれを用いた多層プリント配線板の製造法

（技術分野）

本発明は、回路形成された導体層と絶縁層とを交互に積み上げたビルドアップ方式の多層プリント配線板において、絶縁層を導入するための接着フィルムに関する。

（背景技術）

近年、回路形成された導体層と絶縁層を交互に積み上げていくビルドアップ方式の多層プリント配線板の製造技術が注目されている。ビルドアップ方式により多層プリント配線板を製造する際、絶縁層を形成する方法としては、例えば特開平１１－８７９２７公報に開示されているように、特定の樹脂組成物層を有する接着フィルムを用いて樹脂組成物を回路基板上に真空ラミネートにより積層する方法などが報告されている。

さて、携帯電話を始めとする電子機器においては今後も小型化、高性能化が進み、それに伴い多層プリント配線板も更に薄型化が要求されると考えられる。その際、多層プリント配線板の機械的強度を維持しながら薄型化を図る必要がある。従来の回路基板に使用されているエポキシ樹脂を含浸させたガラスクロス等により製造されるプリプレグ等は機械強度は優れるものの薄型化に限界がある。また、前記特開平１１－８７９２７公報に開示されているような絶縁層を形成させるための接着フィルムを用いただけでは十分な機械的強度が得られない。他方、熱可塑性ポリイミドなどを使用した耐熱樹脂付き銅箔を使用して多層プリント配線板を製造する方法も知られているが、耐熱樹脂のガラス転移点が高すぎるため、ラ

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ミネートに必要な温度が高温となり、一般的な多層プリント配線板における使用は困難であった。

（発明の開示）

［発明が解決しようとする課題］

本発明は、ビルトアップ工法により多層プリント配線板を製造する際に、機械的強度に優れる絶縁層を簡便に導入することが可能な接着フィルムを提供することを目的し、更には機械的強度に優れる多層プリント配線板を簡便に製造する方法を提供することを目的とする。

［課題を解決するための手段］

本発明者等は前記課題を解決すべく鋭意検討した結果、特定の耐熱樹脂の層及び特定の熱硬化性樹脂組成物の層を有する接着フィルムを用いることにより、多層プリント配線板の製造において簡便に機械的強度に優れる絶縁層を導入でき、機械的強度に優れた多層プリント配線板が簡便に得られることを見いだし、このような知見に基いて本発明を完成した。

すなわち、本発明は以下の態様を含むものである。

（１）少なくとも下記のＡ層及びＢ層を隣接して有し、Ｂ層を構成する熱硬化性樹脂組成物が、ラミネート温度より軟化点の低い樹脂を１０重量％以上含有し、回路基板へのラミネートと同時にスルホール及び／又はビアホール内の樹脂充填を行うことが可能な熱硬化性樹脂組成物であることを特徴とする多層プリント配線板用の接着フィルム。

Ａ層：ポリイミド、液晶ポリマー、アラミド樹脂及びポリフェニレンスルフィドからなる群より選択される耐熱樹脂の少なくとも１種からなる厚さ２乃至３０

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μmの耐熱樹脂層、

B層：少なくとも1分子中に2以上のエポキシ基を有するエポキシ樹脂（成分（a））及びエポキシ硬化剤（成分（b））を含有する常温で固形状の熱硬化性樹脂組成物層。

（2）上記態様（1）の多層プリント配線板用の接着フィルムであって、B層を構成する熱硬化性樹脂組成物が、ラミネート温度より軟化点の低い樹脂を10重量%以上含有し、温度70乃至140℃、圧力1乃至20kgf／cm^{2}及び気圧20mmHg以下のラミネート条件において回路基板へのラミネートと同時にスルホール及び／又はビアホール内の樹脂充填を行うことが可能な熱硬化性樹脂組成物であることを特徴とするもの。

（3）前記態様（1）の多層プリント配線板用の接着フィルムであって、B層を構成する熱硬化性樹脂組成物が、更に重量平均分子量が5，000乃至100，000である高分子化合物（成分（c））を5乃至50重量%の割合で含有し、ラミネート温度より軟化点の低い樹脂の含有割合が10重量%以上であり、かつ常温で液状の成分の含有割合が5乃至55重量%であって、回路基板へのラミネートと同時にスルホール及び／又はビアホール内の樹脂充填を行うことが可能な熱硬化性樹脂組成物であることを特徴とするもの。

（4）前記態様（3）の多層プリント配線板用の接着フィルムであって、B層を構成する熱硬化性樹脂組成物が、更に重量平均分子量が5，000乃至100，000である高分子化合物（成分（c））を5乃至50重量%で含有し、ラミネート温度より軟化点の低い樹脂の含有割合が10重量%以上であり、かつ常温で液状の成分の含有割合が5乃至55重量%であって、温度70乃至140℃、圧力1乃至20kgf／cm^{2}及び気圧20mmHg以下のラミネート条件において回路基板へのラミネートと同時にスルホール及び／又はビアホール内の樹脂充填を行うことが可能な熱硬化性樹脂組成物であることを特徴とするもの。

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（５）前記態様（１）の多層プリント配線板用の接着フィルムであって、Ｂ層を構成する熱硬化性樹脂組成物が、測定開始温度６０℃、昇温速度５℃／分で加熱した場合の溶融粘度が、９０℃で４，０００乃至５０，０００ポイズ、１００℃で２，０００乃至２１，０００ポイズ、１１０℃で９００乃至１２，０００ポイズ、１２０℃で５００乃至９，０００ポイズ、そして１３０℃で３００乃至１５，０００である熱硬化性樹脂組成物であることを特徴とするもの。

（６）前記態様（１）乃至（５）のいずれかの多層プリント配線板用の接着フィルムであって、耐熱樹脂層（Ａ層）及び熱硬化性樹脂組成物層（Ｂ層）が剥離性支持フィルム層（Ｃ層）上に形成されており、かつＢ層、Ａ層、そしてＣ層の順の層構成を有することを特徴とするもの。

（７）前記態様（１）乃至（５）のいずれかの多層プリント配線板用の接着フィルムであって、耐熱樹脂層（Ａ層）及び熱硬化性樹脂組成物層（Ｂ層）が剥離性支持フィルム層（Ｃ層）上に形成されており、かつＡ層、Ｂ層、そしてＣ層の順の層構成を有することを特徴とするもの。

（８）前記態様（１）乃至（５）のいずれかの多層プリント配線板用の接着フィルムであって、耐熱樹脂層（Ａ層）及び熱硬化性樹脂組成物層（Ｂ層）が剥離性支持フィルム層（Ｃ層）上に形成されており、Ｂ層、Ａ層、Ｂ層、そしてＣ層の順の層構成を有し、かつ少なくともＣ層に隣接するＢ層が酸化剤による粗化が可能であるものであることを特徴とするもの。

（９）上記態様（６）又は（８）のいずれかの多層プリント配線板用の接着フィルムであって、熱硬化性樹脂組成物層（Ｂ層）のＡ層と隣接しない面が保護フィルム層（Ｄ層）又は剥離性支持フィルム層（Ｃ層）で保護されていることを特徴とするもの。

（10）上記態様（１）乃至（９）のいずれかの多層プリント配線板用の接着フィルムを使用して製造されたことを特徴とする多層プリント配線板。

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(11) 下記の工程（ｉ）乃至（viii）を含むことを特徴とする多層プリント配線板の製造方法。

（ｉ）態様（１）乃至（９）のいずれかの接着フィルムを、ラミネートの際に回路基板側に位置する熱硬化性樹脂組成物層（Ｂ層）が保護フィルム層（Ｄ層）又は剥離性支持フィルム層（Ｃ層）で保護されている場合はこれらの層を剥離した後、Ｂ層を回路基板側にして回路基板の片面又は両面にラミネートする工程、

（ii）剥離性支持フィルム層（Ｃ層）が存在する場合に必要により該Ｃ層を剥離する工程、

（iii）回路基板上にラミネートされた接着フィルムの熱硬化性樹脂組成物層（Ｂ層）を熱硬化し絶縁層を形成する工程、

（iv）剥離性支持フィルム層（Ｃ層）が存在する場合に該Ｃ層を剥離する工程、

（ｖ）絶縁層が形成された回路基板に穴あけする工程、

（vi）絶縁層の表面を粗化処理する工程、

（vii）粗化された絶縁層の表面にメッキにより導体層を形成させる工程、そして

（viii）導体層に回路形成する工程。

［発明の実施の形態］

以下に、本発明を詳細に説明する。

本発明の多層プリント配線板用の接着フィルムは、Ａ層として「ポリイミド、液晶ポリマー、アラミド樹脂及びポリフェニレンスルフィドからなる群より選択される耐熱樹脂の少なくとも１種からなる厚さ２乃至３０μｍの耐熱樹脂層」（以下、「耐熱樹脂層」と略称することがある）を有する。

耐熱樹脂層を構成する耐熱樹脂は、ポリイミド、液晶ポリマー、アラミド樹脂

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又はポリフェニレンスルフィドの少なくとも１種からなる。特に、ポリイミド又はアラミド樹脂が好ましい。これらの樹脂は２種以上を組み合わせて用いてもよい。これらの耐熱樹脂はガラス転移点が２００℃以上であるか、または分解温度が３００℃以上であり、多層プリント配線板の製造において要求される半田耐熱性を満たすものである。耐熱樹脂層の厚さが２μｍ未満では絶縁層や多層プリント配線板の機械強度が十分でない場合があり、一方、３０μｍを超えるとコスト高となる上、必要以上に絶縁層が厚くなり、ビアホールを形成する際の微細化が困難となる場合があるなど好ましくない。

本発明における耐熱樹脂はフィルム状で市販されているものを用いることができ、例えば、宇部興産（株）製ポリイミドフィルム「ユーピ レックスーＳ」、東レ・デュポン（株）製ポリイミドフィルム「カプトン」、鐘淵化学工業（株）製ポリイミドフィルム「アピカル」、旭化成工業（株）製アラミドフィルム「アラミカ」、（株）クラレ製液晶ポリマーフィルム「ベクスター」等のフィルム状の耐熱樹脂を用いることができる。

また、本発明の接着フィルムが剥離性支持フィルム層（Ｃ層）有する場合は、該剥離性支持フィルム層（Ｃ層）上に、あるいはＣ層上に更に熱硬化性樹脂組成物層（Ｂ層）形成する等必要に応じ任意の層を形成した後これら層上に、耐熱樹脂ワニスを塗工し、乾燥させ耐熱樹脂層（Ａ層）形成させフィルム状とすることもできる。耐熱樹脂ワニスとしては、例えば、丸善石油化学（株）製の溶剤可溶型ポリイミド「ＰＩ－１００シリーズ」、新日本理化（株）製のポリイミドワニス「リカコート」シリーズ、日本ＧＥプラスチックス（株）製のポリイミド「ウルテム」を有機溶剤に溶解し樹脂ワニスとしたもの、信越化学工業（株）製のポリイミドシリコーン等を用いることができる。これらの耐熱樹脂ワニスはそのまま、或いは適当な有機溶剤に溶解して使用することができる。また、これらの樹脂ワニスは２種以上組み合わせて使用してもよく、適当な熱硬化性樹脂や樹脂添加剤

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を混練して使用することもできる。これらの耐熱樹脂ワニスを用いた耐熱樹脂層の形成は、後述する熱硬化性樹脂組成物層を形成する条件と同様の条件で容易に行うことができる。

なお、本発明における耐熱樹脂層（Ａ層）については、本発明における熱硬化性樹脂組成物層（Ｂ層）と接する面（隣接する面）が化学的粗化処理、プラズマ処理、機械研磨等の処理がなされている方が、Ｂ層との接着強度を増加させる上で好ましい。

本発明の接着フィルムはＢ層として「少なくとも１分子中に２以上のエポキシ基を有するエポキシ樹脂（成分（ａ））及びエポキシ硬化剤（成分（ｂ））を含有する常温で固形状の熱硬化性樹脂組成物層。」（以下、「熱硬化性樹脂組成物層」と略称することがある）を有する。

成分（ａ）である「１分子中に２以上のエポキシ基を有するエポキシ樹脂」としては、ビスフェノールＡ型エポキシ樹脂、ビスフェノールＦ型エポキシ樹脂、フェノールノボラック型エポキシ樹脂、ビスフェノールＳ型エポキシ樹脂、アルキルフェノールノボラック型エポキシ樹脂、ビフェノール型エポキシ樹脂、ナフタレン型エポキシ樹脂、ジシクロペンタジエン型エポキシ樹脂、フェノール類とフェノール性水酸基を有する芳香族アルデヒドとの縮合物のエポキシ化物、トリグリシジルイソシアヌレート、脂環式エポキシ樹脂等であって１分子中に２以上のエポキシ基を有するエポキシ樹脂を挙げることができる。また、難燃性を付与するために上記エポキシ樹脂を臭素化等したものでもよい。

成分（ａ）のエポキシ樹脂としては分子中に芳香環骨格を有する芳香族系エポキシ樹脂が好ましい。また、成分（ａ）のエポキシ樹脂は常温で固体状のエポキシ樹脂又は常温で液状のエポキシ樹脂のいずれを用いてもよいが、好ましくは液状のものが用いられる。

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なお、本発明における常温とは２０℃～３０℃の温度範囲とすることができる。

成分（ｂ）である「エポキシ硬化剤」としては、アミン系硬化剤、グアニジン系硬化剤、イミダゾール系硬化剤、フェノール系硬化剤、酸無水物系硬化剤又はこれらのエポキシアダクトやマイクロカプセル化したもの等を挙げることができる。また、これらの硬化剤はポットライフが長いものが好ましい。エポキシ硬化剤は２種以上を組み合わせて用いることもできる。

エポキシ硬化剤の具体例としては、例えば、ジシアンジアミド、２－フェニル－４－メチル－５－ヒドロキシメチルイミダゾール、２－フェニル－４，５－ビス（ヒドロキシメチル）イミダゾール、２，４－ジアミノ－６－（２－メチル－１－イミダゾリルエチル）－１，３，５－トリアジン・イソシアヌル酸付加物、２，４－ジアミノ－６－（２－ウンデシル－１－イミダゾリルエチル）－１，３，５－トリアジン等を挙げることができる。

エポキシ硬化剤としては、特に窒素原子を有するフェノール系硬化剤が好ましい。窒素原子を有するフェノール系硬化剤を用いた場合、絶縁層の耐熱性、難燃性、接着性等を向上させる効果が得られる。このようなエポキシ硬化剤としては、例えば、トリアジン構造含有ノボラック樹脂（例えば、「フェノライト７０５０」シリーズ：大日本インキ化学工業（株）製）、メラミン変性フェノールノボラック樹脂（例えば、ジャパンエポキシレジン（株）製「ＹＬＨ８２８」）などがある。

熱硬化性樹脂組成物における、これらエポキシ硬化剤は、アミン系硬化剤、グアニジン系硬化剤又はイミダゾール系硬化剤の場合、通常２乃至１２重量％の範囲で用いられ、フェノール系硬化剤又は酸無水物系硬化剤の場合は熱硬化性樹脂組成物に含まれるエポキシ樹脂のエポキシ基１当量に対して、フェノール性水酸基当量、または酸無水物当量が通常０．５乃至１．３当量の範囲で用いられる。

また、エポキシ硬化剤に加え、硬化促進剤を添加することもできる。このような硬化促進剤としては、イミダゾール系化合物、有機ホスフィン系化合物等を挙

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げることができる。硬化促進剤を用いる場合、好ましくは熱硬化性樹脂組成物に含まれるエポキシ樹脂に対して０．５乃至２重量％の範囲で用いることができる。

本発明における熱硬化性樹脂組成物層（Ｂ層）を構成する熱硬化性樹脂組成物は、回路基板へのラミネートと同時にスルホール及び／又はビアホール内の樹脂充填を行うことが可能な熱硬化性樹脂組成物として調製される。本発明における熱硬化性樹脂組成物は、長時間の真空式熱プレスを必要とせず真空ラミネートにより回路基板上に容易にラミネートが可能であり、更に回路基板がビアホールあるいはスルーホールを有する場合にも、ラミネート条件下で軟化し、回路基板に存在するスルーホールやビアホールを同時に一括して充填できる流動性（樹脂流れ性）を有するものである。多層プリント配線板において樹脂充填されるスルーホールは通常０．１乃至２ｍｍであり、この範囲で樹脂充填を可能とする熱硬化性樹脂組成物は本発明における熱硬化性樹脂組成物に含まれる。例えば、回路基板の両面をラミネートする場合はラミネート温度（通常７０乃至１４０℃）においてスルーホールの１／２を充填可能な流動性を有していればよい。

本発明における熱硬化性樹脂組成物は、真空ラミネートにより回路基板に熱硬化性樹脂組成物層をラミネートすることができ、また回路基板に存在するスルーホールやビアホールを同時に一括して樹脂充填できるため、回路基板上に簡便に絶縁層を形成することを可能とする。真空ラミネートの条件は通常、温度７０乃至１４０℃、圧力１乃至２０ｋｇｆ／ｃｍ^{2}及び気圧２０ｍｍＨｇ以下とすることができる。また、温度８０乃至１２０℃、圧力３乃至１０ｋｇｆ／ｃｍ^{2}及び気圧１０ｍｍＨｇ以下とするのが更に好ましい。

本発明における熱硬化性樹脂組成物は、ラミネート温度より軟化点の低い樹脂を１０重量％以上含有する。ラミネート温度は上述したように通常７０乃至１４０℃とすることができる。１０重量％未満ではラミネートの際の樹脂流れが十分でなく、スルーホールまたはビアホールに樹脂をボイド（void）なく充填するこ

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とが困難となる。好ましくはラミネート温度より軟化点の低い樹脂を１０乃至９０重量％の範囲で含有するよう調製される。９０重量％を越えると流動性が高すぎる傾向にあり、真空ラミネートにより均一な絶縁層の形成が困難となる場合が生じる。

本発明における熱硬化性樹脂組成物は、更に常温で液状の成分の含有割合が５乃至５５重量％であるのが好ましい。常温で液状の成分とは、熱硬化性樹脂組成物に任意に含まれる常温で液状の成分のことであり、常温で液状の樹脂、有機溶剤等を挙げることができる。

成分（ａ）である「１分子中に２以上のエポキシ基を有するエポキシ樹脂」が液状である場合は、ここにいう常温で液状の樹脂に含まれる。また、例えば任意に含まれることがある１分子中に１つのエポキシ基を有するエポキシ樹脂もここにいう常温で液状の樹脂に含まれる。また、前述したエポキシ硬化剤が常温で液状の樹脂である場合もここにいう常温で液状の樹脂に含まれる。任意に含まれることがあるその他の常温で液状の樹脂もここにいう常温で液状の樹脂含まれる。

有機溶剤は後述するように、熱硬化性樹脂組成物層を形成する際に通常用いられる。このような有機溶剤の例としては、アセトン、メチルエチルケトン、シクロヘキサノン等のケトン類、酢酸エチル、酢酸ブチル、セロソルブアセテート、プロピレングリコールモノメチルエーテルアセテート、カルビトールアセテート等の酢酸エステル類、セロソルブ、ブチルカルビトール等のカルビトール類、トルエン、キシレン等の芳香族炭化水素類、ジメチルホルムアミド、ジメチルアセトアミド、Ｎ－メチルピロリドン等を挙げることができる。これらの有機溶剤は２種以上が含まれていても良い。

熱硬化性樹脂組成物にこれら有機溶剤が含まれる場合、その含有割合は通常１０重量％以下、好ましくは５重量％以下である。

常温で液状の成分が１０重量％未満では、接着フィルムの可とう性や切断加工

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性が十分でなく、接着フィルムの取扱性上あまり好ましくない。一方、５５重量％を越える場合は、室温での流動性が高く接着フィルムの製造の際のロール巻き取り時に切断面からの樹脂の浸みだしが起こったり、剥離性支持フィルムや保護フィルムとの剥離性が悪くなる傾向にある。

本発明における熱硬化性樹脂組成物は、更に成分（ｃ）である「重量平均分子量が５，０００乃至１００，０００である高分子化合物」を５乃至５０重量％の割合で含有することが好ましい。例えば、本発明の多層プリント配線板用の接着フィルムを比較的高温でラミネートする場合に、樹脂の流動性が高くなりすぎる傾向にあるが、該高分子化合物を添加することにより、ラミネート時の樹脂流れを抑制し、好ましい流動性が得られるように調製することが容易となる。

なお、重量平均分子量が５，０００未満である場合、流動性の抑制効果が十分でなく、一方、１００，０００を越える場合、熱硬化性樹脂組成物を有機溶剤が配合された樹脂ワニスとし熱硬化性樹脂組成物層を形成する際において、有機溶剤への溶解性が悪くなる場合が生じる。

「重量平均分子量が５，０００乃至１００，０００である高分子化合物」としては、フェノキシ樹脂、ポリアクリル樹脂、ポリイミド樹脂、ポリアミドイミド樹脂、ポリシアネート樹脂、ポリエステル樹脂、熱硬化型ポリフェニレンエーテル樹脂等であって重量平均分子量が５，０００乃至１００，０００であるものを挙げることができる。

高分子化合物としては特にフェノキシ樹脂が好ましい。フェノキシ樹脂としては、例えば「フェノトートＹＰ５０」（東都化成（株）製）、「Ｅ－１２５６」（ジャパンエポキシレジン（株）製）等のフェノキシ樹脂、「ＹＰＢ－４０－ＰＸＭ４０」（東都化成（株）製）等の臭素化フェノキシ樹脂、「ＹＬ６７４７Ｈ３０」（ジャパンエポキシレジン（株）製、ビスフェノールＡ型エポキシ樹脂「エピコート８２８」とビスフェノールＳからなるフェノキシ樹脂のシクロヘキサノンワニス：

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不揮発分３０重量%、重量平均分子量４７，０００）等のビスフェノールＳ骨格を有するフェノキシ樹脂等が挙げられる。

本発明における熱硬化性樹脂組成物が粗化成分を含む場合、本発明の接着フィルムにより回路基板にラミネートされ加熱硬化された後に形成される絶縁層において、該絶縁層表面を酸化剤により化学処理し、表面の粗化を行うことにより、メッキによりピール強度に優れた導体層を絶縁層表面に容易に形成可能となる。

また、本発明における熱硬化性樹脂組成物が、エポキシ硬化剤（成分（ｂ））としてフェノール系硬化剤を使用し、かつ重量平均分子量が５，０００乃至１００，０００である高分子化合物（成分（ｃ））としてビスフェノールＳ骨格を有する重量平均分子量が５，０００乃至１００，０００であるフェノキシ樹脂を含有する場合、粗化成分を含有しなくても酸化剤による粗化が可能である。

粗化成分としては、ゴム成分、アミノ樹脂、無機フィラー、有機フィラーなどを挙げることができる。

そして、ゴム成分としては、ポリブタジエンゴム、エポキシ変性ポリブタジエンゴム、ウレタン変性ポリブタジエンゴム、アクリロニトリル変性ポリブタジエンゴム、メタクリロニトリル変性ポリブタジエンゴム、カルボキシル基を有するアクリロニトリル・ブタジエンゴム、カルボキシル基を有するメタクリロニトリル・ブタジエンゴム、アクリルゴム分散型エポキシ樹脂等を挙げることができる。

アミノ樹脂としては、メラミン樹脂、グアナミン樹脂、尿素樹脂等のアミノ樹脂又はこれらアミノ樹脂をアルキルエーテル化したもの等を挙げることができる。

無機フィラーとしては、炭酸カルシウム、炭酸マグネシウム、酸化マグネシウム、水酸化アルミニウム等を挙げることができる。

有機フィラーとしては、粉体エポキシ樹脂、架橋アクリルポリマー、上記アミノ樹脂を熱硬化させ微粉砕したもの等を挙げることができる。

本発明の熱硬化性樹脂組成物において、粗化成分を有する場合の粗化成分の含

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有割合は好ましくは５乃至４０重量％、更には１０乃至３０重量％であるのが好ましい。５重量％未満であると、粗化が十分でない場合があり、一方、４０重量％を越えると硬化後における絶縁層の絶縁性、耐薬品性、耐熱性等が悪くなる傾向にある。

なお、熱硬化性樹脂組成物（Ｂ層）においては、諸機能を付与するため、上述した粗化成分として用いる無機フィラー以外の無機フィラーを含有せしめることもできる。このように添加剤として用いる無機フィラーとしては、例えば、硫酸バリウム、チタン酸バリウム、酸化ケイ素粉、無定型シリカ、タルク、クレー、雲母粉等を挙げることができる。これらの粗化成分以外の無機フィラーは必要に応じて熱硬化性樹脂組成物中１０乃至８０重量％の範囲で用いることができる。

また、本発明の熱硬化性樹脂組成物（Ｂ層）は必要によりまたは所望によりその他の各種の樹脂添加剤を含むことができる。このような添加剤としては、増粘剤、消泡剤、レベリング剤、密着性付与剤、着色剤、難燃助剤、無機フィラー、有機フィラー等を挙げることができる。

本発明における熱硬化性樹脂組成物層（Ｂ層）を構成する熱硬化性樹脂組成物は、真空ラミネートにより回路基板へのラミネートと同時にスルホール及び／又はビアホール内の樹脂充填を行うことが可能とするものである。このような熱硬化性樹脂組成物は真空ラミネートにおける温度条件（通常７０℃～１４０℃）で軟化し、好ましい流動性（樹脂流れ）を示し、ビアホール或いはスルーホールが存在する場合には、これらホールへの樹脂充填を同時に一括して行うことができるものである。このような物性は、熱硬化性樹脂組成物の動的粘弾性率の測定による温度－溶融粘度曲線によって特徴づけることができる。

後掲実施例１で得られた熱硬化性樹脂組成物に基づいた動的粘弾性率を測定することにより、本発明における熱硬化性樹脂組成物として好ましい温度－溶融粘

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度（η）の関係の例を図１に示す。測定開始温度を６０℃とし、５℃／分の昇温速度で加熱していったときの熱硬化性樹脂組成物の溶融粘度を曲線図として表したものである。この図から、本発明に好ましい熱硬化性樹脂組成物の特性として、同条件で温度－溶融粘度の相関を測定した場合に、各温度における溶融粘度が下記第１表に示す範囲にあるものを、更に好ましくは第２表に示す範囲にあるものを、本発明に好ましい熱硬化性樹脂組成物とすることができる。

第１表

温度（℃）	溶融粘度（poise）
９０	４，０００～ ５０，０００
１００	２，０００～ ２１，０００
１１０	９００～ １２，０００
１２０	５００～ ９，０００
１３０	３００～ １５，０００

第２表

温度（℃）	溶融粘度（poise）
９０	１０，０００～ ２５，０００
１００	５，０００～ １０，０００
１１０	２，０００～ ６，０００
１２０	１，０００～ ５，０００
１３０	６００～ ３，０００

ラミネートの際、回路基板面に直接接する熱硬化性樹脂組成物層（Ｂ層）の厚さは、導体層の厚さ以上とするの通常である。回路基板が有する導体層の厚さは通常５～７０μｍの範囲であるが、Ｂ層の厚さはこの導体層の厚さにに加え更に５乃至１００μｍの厚みを有するのが好ましい。

また、導体層の被覆（及びビアホールまたはスルーホールの充填）に寄与しな

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い熱硬化性樹脂組成物層（Ｂ層)、すなわち専ら熱硬化後に表面に導体層を形成するために用いられる酸化剤により粗化可能な熱硬化性樹脂組成物層（Ｂ層）においては、厚さを２乃至２０μｍとするのが好ましい。例えば、本発明の接着フィルムが、「（１）熱硬化性樹脂組成物層（Ｂ層）／（２）耐熱樹脂層（Ａ層）／（３）酸化剤により粗化可能な熱硬化性樹脂組成物層（Ｂ層)」の層構成を有するものであれば、回路基板への接着フィルムのラミネートにおいて熱硬化性樹脂組成物層（１）を導体層の被覆に用い、そして酸化剤により粗化可能な熱硬化性樹脂組成物層（３）は熱硬化後にメッキにより導体層を形成させる絶縁層表面として用いることができる。

このような場合、酸化剤により粗化可能な熱硬化性樹脂組成物層の厚さが２μｍ未満では粗化処理後の好ましい凹凸面が得られない傾向にあり、一方、２０μｍを超えると必要以上の絶縁層の厚さを増すことになり、薄型化する上で好ましくない。

なお、導体層の被覆（及びビアホールまたはスルーホールの充填）に寄与しない熱硬化性樹脂組成物層（Ｂ層）は、真空ラミネートにおいて導体層の被覆に必要な特定の流動性を有している必要はない。

熱硬化性樹脂組成物層（Ｂ層）を形成する方法としては、先に例示したような有機溶剤に熱硬化性樹脂組成物を溶解した樹脂ワニスを調製し、耐熱樹脂層（Ａ層）又は剥離性支持フィルム層（Ｃ層）を支持体として、この樹脂ワニスを塗布し、加熱あるいは熱風吹きつけ等により有機溶剤を乾燥させて層形成させればよい。有機溶剤は必要に応じて２種以上を組み合わせて用いることができる。

本発明における剥離性支持フィルムは、通常、耐熱樹脂ワニスから耐熱樹脂層を形成する場合の支持体として、又は熱硬化性樹脂組成物の樹脂ワニスから熱硬化性樹脂組成物層を形成する際の支持体として使用されるものである。

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本発明の多層プリント配線板用の接着フィルムが剥離性支持フィルム層(C層)を有する場合、C層に使用する剥離性支持フィルムとしては、ポリエチレンテレフタレート等のポリエステル、ポリカーボネート、離型紙などのフィルム状のものを用いることができる。剥離性支持フィルムの厚さとしては10～150μmが一般的であり、好ましくは25～50μmの範囲で用られる。なお、剥離性支持フィルムにはマット(mat)処理、コロナ処理、離型処理等が施してあってもよい。

本発明における剥離性支持フィルムは、本発明の接着フィルムを回路基板にラミネートした後に、或いは加熱硬化することにより絶縁層を形成した後に、剥離される。接着フィルムを加熱硬化した後に剥離性支持フィルムを剥離すれば、硬化工程でのゴミ等の付着を防ぐことができる。硬化後に剥離する場合、剥離性支持フィルムには予め離型処理が施される。

なお、熱硬化性樹脂組成物を剥離性支持フィルム又は耐熱樹脂組成物上に形成する場合、熱硬化性樹脂組成物層の面積が剥離性支持フィルムの面積より小さくなるように形成するのが好ましい。

本発明の多層プリント配線板用の接着フィルムにおける保護フィルムは、接着フィルムへのゴミ等の付着を防止したり、キズ防止のため、主として熱硬化性樹脂組成物層を保護するために使用されるものである。従って、保護フィルムは通常、接着フィルムを回路基板にラミネートする前に剥離される。なお、例えば、剥離性支持フィルム上に熱硬化性樹脂組成物層や耐熱樹脂層を層形成したものを張り合わせて接着フィルムを作成する場合、剥離性支持フィルム層が保護フィルム層の役割を果たす場合がある。

本発明の接着フィルムが保護フィルム層(D層)を有する場合、D層としては、フィルム状の、ポリエチレン、ポリプロピレン、ポリエチレンテレフタレート等

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を用いることができる。保護フィルム層の厚さは通常１～４０μmの範囲で用いられる。

本発明による多層プリント配線板用の接着フィルムの好ましい層構成としては以下の例を挙げることができる。

層構成例（１）　保護フィルム層（Ｄ層）又は剥離性支持フィルム層（Ｃ層）／熱硬化性樹脂組成物層（Ｂ層）／耐熱樹脂層（Ａ層）／酸化剤による粗化が可能な熱硬化樹脂組成物層（Ｂ層）／剥離性支持フィルム層（Ｃ層)、

層構成例（２）　Ｄ層又はＣ層／Ｂ層／Ａ層、そして

層構成例（３）　Ｄ層又はＣ層／Ｂ層／Ａ層／Ｃ層。

なお、層構成例（１）において、双方の熱硬化性樹脂組成物（Ｂ層）が酸化剤により粗化が可能であっても構わない。

層構成例（１）の層構成を有する接着フィルムにおいて、保護フィルム層（又は剥離性支持フィルム層）を剥離し、剥離後の熱硬化性樹脂組成物層側を回路基板に接触するようラミネートし、更に熱硬化することにより絶縁層が形成される。ラミネート時に存在する剥離性支持フィルム層はラミネート後、又は熱硬化後に剥離される。

このようにして形成された絶縁層は耐熱樹脂層を有することにより、機械強度、層間絶縁性、加熱時の寸法安定性等に優れたものとなる。絶縁層の表面側に酸化剤により粗化が可能な熱硬化性樹脂組成物層（Ｂ層）が形成されている場合は、絶縁層表面を容易に粗化することができ、メッキにより導体層を容易に形成することが可能となる。

酸化剤（特にアルカリ性過マンガン酸溶液）による粗化処理は、ビルトアップ工法による多層プリント配線板の製造において導体層を形成する手段として汎用されている。従って、本発明の接着フィルムにおいて、絶縁層の表面側に位置す

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る熱硬化性樹脂組成物層が酸化剤により粗化可能な層構成とすれば、より簡便に多層プリント配線板を製造することが可能となる。

層構成例（１）の層構成を有する接着フィルムの製造方法の例としては、次のものを挙げることができる。すなわち、

（１）耐熱樹脂からなるフィルム上に熱硬化性樹脂組成物の樹脂ワニスを塗工し、乾燥させ、さらに熱硬化性樹脂組成物表面に保護フィルムを貼り合わせる(フィルム１：Ｄ層／Ｂ層／Ａ層)。別途、剥離性支持フィルムに酸化剤で粗化可能な熱硬化性樹脂組成物の樹脂ワニスを塗工し、乾燥させる（フィルム２：Ｂ層／Ｃ層)。次いで、フィルム２の熱硬化性樹脂組成物面をフィルム１の耐熱樹脂組成物面に貼り合わせる（Ｄ層／Ｂ層／Ａ層／酸化剤で粗化可能なＢ層／Ｃ層)、

（２）耐熱樹脂からなるフィルム上に酸化剤で粗化可能な熱硬化性樹脂組成物の樹脂ワニスを塗工し、乾燥させ該樹脂組成物層表面に剥離性支持フィルムを貼り合わせる（フィルム１：Ｃ層／酸化剤で粗化可能なＢ層／Ａ層)。ついで、フィルム１のＡ層側表面に熱硬化性樹脂組成物の樹脂ワニスを塗工し、乾燥させ、さらに該熱硬化性樹脂組成物表面に剥離性支持フィルムを貼り合わせる（Ｃ層／酸化剤で粗化可能なＢ層／Ａ層／Ｂ層／Ｃ層)、

（３）剥離性支持フィルムに酸化剤で粗化可能な熱硬化性樹脂組成物の樹脂ワニスを塗工し、乾燥させ、次いで、耐熱樹脂ワニスを熱硬化性樹脂組成物層上に塗工し、乾燥させる（Ａ層／酸化剤で粗化可能なＢ層／Ｃ層)。さらに、その耐熱樹脂層表面に熱硬化性樹脂組成物の樹脂ワニスを塗工し、乾燥させ、熱硬化性樹脂組成物表面に保護フィルムを貼り合わせる（Ｄ層／Ｂ層／Ａ層／酸化剤で粗化可能なＢ層／Ｃ層)、そして

（４）剥離性支持フィルムに酸化剤で粗化可能な熱硬化性樹脂組成物の樹脂ワニスを塗工し、乾燥させる（フィルム１：酸化剤で粗化可能なＢ層／Ｃ層)。別途剥離性支持フィルムに熱硬化性樹脂組成物の樹脂ワニスを塗工し、乾燥させる

（フィルム２：Ｂ層／Ｃ層）。フィルム１および２の熱硬化性樹脂組成物面を耐熱樹脂からなるフィルムの両面に貼り合わせる（Ｃ層／Ｂ層／Ａ層／酸化剤で粗化可能なＢ層／Ｃ層）。

層構成例（２）及び（３）の層構成を有する接着フィルムは、保護フィルム層（又は剥離性支持フィルム層）を剥離し、剥離後の熱硬化性樹脂組成物層側を回路基板に接触するようラミネートし、更に熱硬化することにより絶縁層が形成される。層構成例（３）の場合、ラミネート時に存在する剥離性支持フィルム層はラミネート後、又は熱硬化後に剥離される。また、絶縁層の表面側にある耐熱樹脂層の表面を粗化処理することにより、メッキにより導体層を形成することが可能である。

なお、層構成例（２）及び（３）の層構成を有する接着フィルムは、既述した層構成例（１）の層構成を有する接着フィルムに準じて製造することが可能である。

本発明の接着フィルムは、これをロール状に巻き取って保存または貯蔵することもできる。

本発明の多層プリント配線板用の接着フィルムを用いて多層プリント配線板を製造する方法としては、例えば、先に言及した以下の工程（ｉ）乃至（ⅷ）を含む方法を典型例として挙げることができる。

（ｉ）接着フィルムを、ラミネートの際に回路基板側に位置する熱硬化性樹脂組成物層（Ｂ層）が保護フィルム層（Ｄ層）又は剥離性支持フィルム層（Ｃ層）で保護されている場合はこれらの層を剥離した後、Ｂ層を回路基板側にして回路基板の片面又は両面にラミネートする工程、

（ⅱ）剥離性支持フィルム層（Ｃ層）が存在する場合に、必要により該Ｃ層を剥離する工程、

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（iii）回路基板上にラミネートされた接着フィルムの熱硬化性樹脂組成物層（B層）を熱硬化させ絶縁層を形成する工程、

（iv）剥離性支持フィルム層（C層）が存在する場合に該C層を剥離する工程、

（v）絶縁層が形成された回路基板に穴あけする工程、

（vi）絶縁層の表面を粗化処理する工程、

（vii）粗化された絶縁層の表面にメッキにより導体層を形成させる工程、そして

（viii）導体層に回路形成する工程。

詳述すると、本発明の多層プリント配線板用の接着フィルムを回路基板にラミネートする際において、ラミネートの際に回路基板側に位置する熱硬化性樹脂組成物層（B層）が保護フィルム層（D層）又は剥離性支持フィルム層（C層）で保護されている場合はこれらの層を剥離した後、B層を回路基板側にして回路基板の片面又は両面にラミネートする。本発明の接着フィルムにおいては真空ラミネートにより回路基板にラミネートする方法が好適に用いられる。

ラミネートの方法はバッチ式であってもロールでの連続式であってもよい。また、ラミネートを行う前に接着フィルム及び回路基板を必要によりプレヒートしておいてもよい。ラミネートの条件は前述した通りである。

真空ラミネートは市販の真空ラミネーターを使用して行うことができる。市販の真空ラミネーターとしては、例えば、ニチゴー・モートン（株）製「バキュームアップリケーター」、（株）名機製作所製「真空加圧式ラミネーター」、日立テクノエンジニアリング（株）製「ロール式ドライコータ」、日立エーアイーシー（株）製「真空ラミネータ」等を挙げることができる。

本発明における回路基板とは、主として、ガラスエポキシ、金属基板、ポリエステル基板、ポリイミド基板、ＢＴレジン基板、熱硬化型ポリフェニレンエーテル基板等の基板の片面又は両面にパターン加工された導体層（回路）が形成され

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たものをいう。また、導体層と絶縁層が交互に層形成してなる多層プリント配線板において、該多層プリント配線板の最外層の片面又は両面がパターン加工された導体層（回路）となっているものも本発明にいう回路基板に含まれる。なお、導体回路層表面は黒化処理等により予め粗化処理が施されていた方が絶縁層の回路基板への密着性の観点から好ましい。

なお、剥離性支持フィルム層（C層）が存在する場合に、ラミネート後に該C層を剥離してもよい。

熱硬化の条件は樹脂によっても異なるが硬化温度が通常１００～２００℃、そして硬化時間が通常１０～９０分の範囲で選択される。比較的低い硬化温度から高い硬化温度へ上昇させながら硬化した方が形成される絶縁層表面のしわや、ホール等へのボイド発生を防止する観点から好ましい。

なお、硬化後において剥離性支持フィルム層（C層）が存在する場合に該C層を剥離する。

次に、回路基板上に形成された絶縁層を必要に応じて穴開けを行いビアホール、スルーホールを形成する。穴あけは、例えば、ドリル、レーザー、プラズマ等の公知の方法により、また必要によりこれらの方法を組み合わせて行うことができる。

次いで、絶縁層表面の粗化処理を行う。粗化処理は、表面を乾式法、湿式法又はこれらの方法を組み合わせた方法で行うことができる。

乾式法としては、バフ、サンドブラスト等の機械研磨による粗化処理やプラズマエッチングによる粗化処理などを挙げることができる。

湿式法としては、アルカリ性過マンガン酸溶液、重クロム酸塩、オゾン、過酸化水素／硫酸、硝酸等の酸化剤溶液、または強アルカリ溶液など、化学薬品による粗化処理を挙げることができる。

粗化処理を行う絶縁層表面が耐熱樹脂層である場合は、メッキにより形成され

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る導体層のピール強度等の観点から乾式法で粗化するのが好ましい。一方、粗化処理を行う絶縁層表面が熱硬化性樹脂組成物層である場合、酸化剤を用いた湿式法による粗化処理により粗化が可能な熱硬化性樹脂組成物層とするのが好ましい。酸化剤による粗化処理は、ビルトアップ工法による多層プリント配線板の製造において導体層を形成する手段として汎用されており、より簡便に多層プリント配線板を製造することが可能となる。

酸化剤としては特にアルカリ性過マンガン酸溶液が好ましく、アルカリ性過マンガン酸溶液としては、例えば、過マンガン酸カリウム、過マンガン酸ナトリウムの水酸化ナトリウム水溶液を挙げることができる。

次に、粗化処理された絶縁層表面にメッキにより導体層を形成する。メッキ方法としては乾式メッキ法、湿式メッキ法等を挙げることができる。

乾式メッキ法としては、例えば、蒸着、スパッタリング、イオンプレーティング等の公知の方法を使用することができる。

湿式メッキ法の場合は、まずアルカリ性過マンガン溶液等の酸化剤で樹脂組成物層（絶縁層）の表面を粗化処理し、凸凹のアンカーを形成する。次いで、無電解メッキと電解メッキを組み合わせた方法で導体層を形成する。また、導体層とは逆パターンのメッキレジストを形成し、無電解メッキのみで導体層を形成することもできる。なお、導体層形成後、１５０～２００℃で２０～９０分アニール（anneal）処理することにより、導体層のピール（peel）強度を向上させ、安定化させることができる。

また、導体層をパターン加工し回路形成する方法としては、例えば当業者に公知のサブトラクティブ法、セミアディディブ法などを用いることができる。

（図面の簡単な説明）

第１図は、実施例１で調製された熱硬化性樹脂組成物を異なる２種類の乾燥条

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件で処理したものについて動的粘弾性率を測定した結果を示す。

第２図は、実施例１における熱硬化性樹脂組成物を更に異なる３種類の乾燥条件で処理したものにつて動的粘弾性率を測定した結果を示す。

第３図は、実施例１における熱硬化性樹脂組成物をなお更に異なる３種類の乾燥条件で処理したものについて動的粘弾性率を測定した結果を示す。

第４図は、実施例４の接着フィルムにおける熱硬化性樹脂組成物層についての動的粘弾性率を測定した結果を示す。

なお、図中、ηは溶融粘度を示す。

（発明を実施するための最良の形態）

以下、施例を示して本発明を具体的に説明するが、本発明はこれら実施例に限定されるものではない。

実施例１

液状ビスフエノールＡ型エポキシ樹脂（エポキシ当量１８５、油化シエルエポキシ（株）製「エピコート８２８ＥＬ」）２０部、臭素化ビスフエノールＡ型エポキシ樹脂（エポキシ当量５００、東都化成（株）製「ＹＤ－５００」）２０部、クレゾールノボラック型エポキシ樹脂(エポキシ当量２１５、大日本インキ化学(株)製「エピクロンＮ－６７３」）２０部、および末端エポキシ化ポリブタジエンゴム（ナガセ化成工業（株）製「デナレックスＲ－４５ＥＰＴ」）１５部をメチルエチルケトンに撹拌しながら加熱溶解させた。そこへ臭素化フェノキシ樹脂ワニス(不揮発分４０重量％、溶剤組成キシレン：メトキシプロパノール：メチルエチルケトン＝５：２：８、東都化成（株）製「ＹＰＢ－４０－ＰＸＭ４０」）５０部、エポキシ硬化剤として２，４－ジアミノ－６－（２－メチル－１－イミダゾリルエチル）－１，３，５－トリアジン・イソシアヌル酸付加物４部、さらに微粉砕シ

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リカ２部、三酸化アンチモン４部、および炭酸カルシウム５部を添加し熱硬化性樹脂組成物の樹脂ワニスを作製した。

この樹脂ワニスを両面プラズマ処理のポリイミドフィルム((株)宇部興産製「ユーピレックスＳ」(厚さ１２．５μｍ、ガラス転移点５００℃以上)) 上に、乾燥後の樹脂厚みが６０μｍとなるようにダイコーターにて塗布し、８０～１２０℃(平均１００℃) で約８分間乾燥し (残留溶媒量約２重量%)、乾燥後の熱硬化性樹脂組成物の表面に厚さ１５μｍのポリプロピレンフィルムを貼り合わせながらロール状に巻き取った。ロール状の接着フィルムを幅５０７ｍｍにスリット (slit) し、これより５０７×３３６ｍｍサイズのシート状の接着フィルムを得た。得られた接着フィルムの層構成はポリプロピレンフィルム層 (保護フィルム層) ／熱硬化性樹脂組成物層／ポリイミドフィルム層 (耐熱樹脂層) である。

ここで得られた熱硬化性樹脂組成物につき、動的粘弾性率を測定した結果を第１および第２図に示す。なお、測定は (株) ユービーエム製「動的粘弾性測定装置Ｒｈｅｏｓｏｌ－Ｇ３０００」を用いて行った。

第１図において、上の動的粘弾性率曲線 (１) は、熱硬化性樹脂組成物の樹脂ワニスを塗工した後、平均乾燥温度１００℃で１０分間加熱乾燥して得られた熱硬化性樹脂組成物層について測定したものである。また、下の動的粘弾性率曲線 (２) は、熱硬化性樹脂組成物の樹脂ワニスを塗工した後、平均乾燥温度１００℃で３．５分間加熱処理して得られた熱硬化性樹脂組成物層について測定したものである。なお、測定時の昇温速度を５℃／分とし、測定開始温度を６０℃、測定温度間隔を２．５℃、そして振動１Ｈｚ／ｄｅｇで測定された。測定値の一部を下記第３表に示す。

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第３表

温度（℃）	溶融粘度（poise）
７０	３５，０００～２６５，０００
８０	１２，９００～１１４，５００
９０	４，９００～ ４６，４００
１００	２，０００～ ２０，４００
１１０	９００～ １１，１００
１２０	４７０～ ８，８００
１３０	３００～ １４，２００
１４０	２８０～ ４６，８００

第２図は、同じ熱硬化性樹脂組成物の樹脂ワニスを塗工した後、平均乾燥温度１００℃で５分間加熱処理して得られた熱硬化性樹脂組成物層についての動的粘弾性率曲線を示している。曲線Ｉが昇温速度２０℃／分で測定したもの、曲線IIが昇温速度１０℃／分で測定したもの、そして曲線IIIが昇温速度５℃／分で測定したものである。なお、測定開始温度を６０℃、測定温度間隔を２．５℃、そして振動１Ｈｚ／ｄｅｇとして測定された。

第３図は、同じ熱硬化性樹脂組成物の樹脂ワニスを塗工した後、平均乾燥温度１００℃で２分間乾燥させたもの（曲線Ａ、比較例２で使用の接着フィルム）、８分間乾燥させたもの（曲線Ｂ、実施例５および８で使用の接着フィルム）、および１５分間乾燥させたもの（曲線Ｃ、比較例３で使用の接着フィルム）の動的粘弾性率曲線を示している。なお、測定開始温度を６０℃、測定温度間隔を２．５℃、そして振動１Ｈｚ／ｄｅｇとして測定された。測定値の一部を下記第４表に示す。

第４表

曲線Ａ

温度（℃）	溶融粘度（poise）
７０	１９，３００
８０	７，５００
９０	３，１００
１００	１，４００
１１０	６９０
１２０	３９０
１３０	２６０
１４０	２２０

曲線Ｂ

温度（℃）	溶融粘度（poise）
７０	８０，０００
８０	３６，０００
９０	１４，６００
１００	６，３００
１１０	３，２００
１２０	２，１００
１３０	１，９００
１４０	２，７００

曲線Ｃ

温度（℃）	溶融粘度（poise）
７０	３４８，０００
８０	２３４，０００
９０	１２１，０００
１００	７２，０００
１１０	５４，０００
１２０	９２，０００

実施例２

厚さ３８μｍのポリエチレンテレフタレートフィルムの離型処理面上に、丸善

石油化学（株）製「溶剤可溶型ポリイミドＰＩ－１００（ガラス転移点３００℃）」をＮ，Ｎ－ジメチルホルムアミドで溶解させたワニスを塗工し、８０～１４５℃（平均１２０℃）で乾燥させ、厚さ５μｍのポリイミドフィルム層を形成した。

そのポリイミドフィルム層上に実施例１で得られた熱硬化性樹脂組成物の樹脂ワニスを、乾燥後の樹脂の厚みが４０μｍとなるようにダイコーターにて塗布し、８０～１２０℃（平均１００℃）で乾燥し（残留溶媒量約２重量％）、乾燥後の熱硬化性樹脂組成物の表面に厚さ１５μｍのポリプロピレンフィルムを貼り合わせながらロール状に巻き取った。ロール状の接着フィルムを幅５０７ｍｍにスリット（slit）し、これより５０７×３３６ｍｍサイズのシート状の接着フィルムを得た。

得られた接着フィルムの層構成はポリプロピレンフィルム層(保護フィルム層)／熱硬化性樹脂組成物層／ポリイミドフィルム層（耐熱樹脂層）／ポリエチレンテレフタレートフィルム（剥離性支持フィルム層）である。

実施例３

臭素化ビスフエノールム型エポキシ樹脂（東都化成（株）製「ＹＤＢ－５００」）５０部、クレゾールノボラック型エポキシ樹脂（エポキシ当量２１５、軟化点７８℃、大日本インキ化学（株）製「エピクロンＮ－６７３」）２０部、および末端エポキシ化ポリブタジエンゴム（ナガセ化成工業（株）製「デナレックスＲ－４５ＥＰＴ」）１５部をメチルエチルケトン／トルエン混合溶媒に撹伴しながら加熱溶解させ、そこへエポキシ硬化剤として２，４－ジアミノ－６－（２－メチル－１－イミダゾリル）－エチル－１，３，５－トリアジン４部を加え、さらに微粉砕シリカ２部および炭酸カルシウム１０部を添加して熱硬化性樹脂組成物の樹脂ワニスを調製した。

この樹脂ワニスを実施例１におけると同様にポリイミドフィルム上に塗工し、

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８０～１２０℃（平均１００℃）で乾燥し、厚さ５μｍの熱硬化性樹脂組成物層を形成し、その上に厚さ２５μｍの離型処理ポリエチレンテレフタレートフィルムを貼り合わせた。その後、ポリイミドフィルムの該熱硬化性樹脂組成物層形成面とは逆の面に、実施例１と全く同様にして熱硬化性樹脂組成物層６０μｍを形成し、乾燥後の熱硬化性樹脂組成物の表面に厚さ３８μｍの離型処理ポリエチレンテレフタレートフィルムを貼り合わせながらロール状に巻き取った。ロール状の接着フィルムを幅５０７ｍｍにスリット（slit）し、これより５０７×３３６ｍｍサイズのシート状の接着フィルムを得た。

得られた接着フィルムの層構成はポリエチレンテレフタレートフィルム（剥離性支持フィルム層）／酸化剤で粗化可能な熱硬化性樹脂組成物層／ポリイミドフィルム層（耐熱樹脂層）／熱硬化性樹脂組成物層／ポリエチレンテレフタレートフィルム（剥離性支持フィルム層）である。

実施例４

ビスフェノールＡ型エポキシ樹脂（油化シェルエポキシ（株）製「エピコート８２８」）２０部、およびクレゾールノボラック型エポキシ樹脂（エポキシ当量２１５、軟化点７８℃、大日本インキ化学（株）製「エピクロンＮ－６７３」）３５部をＭＥＫに撹拌しながら加熱溶解させ室温まで冷却した後、そこへトリアジン構造含有フェノールノボラック樹脂のＭＥＫワニス（大日本インキ化学工業（株）製「フェノライトＬＡ－７０５２」、不揮発分６０％、不揮発分のフェノール性水酸基当量１２０）４５部、テトラメチルタイプのビフェノール型エポキシ樹脂（油化シェルエポキシ（株）製「ＹＸ－４０００」）とビスフェノールＳからなるフェノキシ樹脂のシクロヘキサノンワニス（油化シェルエポキシ（株）製「ＹＬ６７４６Ｈ３０」、不揮発分３０重量％、そして重量平均分子量３０，０００）７０部、さらに球型シリカ１８部および微粉砕シリカ２部を添加しエポキシ樹脂組成物を

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作製した。

そのワニス状のエポキシ樹脂組成物を厚さ３８μmのポリエチレンテレフタレートフィルムの離型処理面上に塗工し、８０～１２０℃（平均１００℃）で乾燥させ（残留溶媒量約２重量％）、厚さ１０μmと４５μmの２種類の膜厚で熱硬化性樹脂組成物層を形成し、それぞれロール状に巻き取った。次いで、厚さ４．５μmのアラミドフィルム（旭化成工業（株）製「アラミカ」、両面プラズマ処理）の両面に、上記２種類の膜厚の熱硬化性樹脂組成物面を同時に貼り合わせて得たロール状の接着フィルムを幅５０７mmにスリット（slit）し、これより５０７×３３６mmサイズのシート状の接着フィルムを得た。

得られた接着フィルムの層構成はポリエチレンテレフタレートフィルム（剥離性支持フィルム層）／熱硬化性樹脂組成物層／ポリイミドフィルム層（耐熱樹脂層）／酸化剤で粗化可能な熱硬化性樹脂組成物層／ポリエチレンテレフタレートフィルム（剥離性支持フィルム層）である。

ここで得られた４５μm厚の、回路基板へのラミネート側の熱硬化性樹脂組成物につき、動的粘弾性率を測定した結果を第４図に示す。なお、測定は実施例１におけると同じ「Ｒｈｅｏｓｏｌ－Ｇ３０００」を用いて行った。測定条件は、昇温速度が５℃／分、測定開始温度が６０℃、測定温度間隔が２．５℃、そして振動１Ｈｚ／ｄｅｇである。測定値の一部を下記第５表に示す。

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第５表

温度（℃）	溶融粘度（poise）
７０	１１６，０００
８０	３７，０００
９０	１３，０００
１００	５，３００
１１０	２，７００
１２０	２，１００
１３０	１，８００
１４０	１，８００

比較例１

ポリイミドフィルムを厚さ３８μmのポリエチレンテレフタレートフィルムに変更する以外は実施例１におけると全く同様にして接着フィルムを得た。接着フィルムの層構成はポリプロピレンフィルム／熱流動性樹脂組成物／ポリエチレンテレフタレートフィルムである。

実施例５

厚さ０．４mm、サイズ５１０×３４０mmのガラスエポキシ回路基板（導体厚３５μm）に、実施例１で得られた接着フィルムのポリプロピレンフィルムを剥離し、熱硬化性樹脂組成物面を回路側として基板両面に枚葉した。次に、（株）名機製作所製「真空ラミネーターＭＶＬＰ」により、真空度１ミリバール（０．７５mmHg）、温度１００℃、そして圧力６kg／cm^{2}の条件で１５秒間プレスし、両面同時にラミネートした後、積層回路板を１２０℃で３０分、さらに１７０℃で３０分熱硬化させた。その後、所定のスルーホールおよびビアホール部にドリル及びレーザーにより穴開けを行い、次いで酸素ガスによるプラズマエッチングし、さらにスパッタリング装置によりニッケル、クロムおよび銅と常法に

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従って導体層を形成した。次に、導体層とは逆パターンのメッキレジストを形成させ電解銅メッキを行い、セミアディティブ法に従って多層プリント配線板を得た。

得られた多層プリント配線板の導体のピール強度は０．９ｋｇ／ｃｍであった。また、絶縁層部分のユニバーサル硬度計（(株) フィッシャー・インストルメンツ製「ＦＩＳＣＨＥＲＳＣＯＰＥ　Ｈ１００」）から求められた弾性率は、室温で６．７ＧＰａ、そして１５０℃で５．２ＧＰａであった。

実施例６

実施例５におけると同様に、厚さ０．２ｍｍ、サイズ５１０×３４０ｍｍのガラスエポキシ回路基板（導体厚１８μｍ）に、実施例２で得られた接着フィルムのポリプロピレンフィルムを剥離し、熱硬化性樹脂組成物面を回路側として基板両面に枚葉した。次に、(株) 名機製作所製「真空ラミネーターＭＶＬＰ」により、真空度１ミリバール（０．７５ｍｍＨｇ)、温度１００℃、そして圧力６ｋｇ／ｃｍ^{2}の条件で１５秒間プレスし両面同時にラミネートした後、１２０℃で３０分、さらに１７０℃で３０分熱硬化させた。その後、ポリエチレンテレフタレートフィルムを剥離し、所定のスルーホールおよびビアホール部にドリル及びレーザーにより穴開けを行い、次いでアルゴンガスによるプラズマエッチングし、さらにスパッタリング装置によりニッケル、クロムおよび銅と常法に従って導体層を形成した。次に、導体層とは逆パターンのメッキレジストを形成させ電解銅メッキを行い、セミアディティブ法に従って多層プリント配線板を得た。

得られた多層プリント配線板は１７０℃で６０分間アニール処理した後の導体ピール強度が０．９ｋｇ／ｃｍであった。また、絶縁層部分のユニバーサル硬度計から求められた弾性率は、室温で６．０ＧＰａ、そして１５０℃で４．６ＧＰａであった。

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実施例７

実施例５におけると同様に、厚さ０．４ｍｍ、サイズ５１０×３４０ｍｍのガラスエポキシ回路基板（導体厚３５μｍ）に、実施例３で得られた接着フィルムの熱硬化性樹脂組成物面を回路側として基板両面に枚葉した。次に、(株)名機製作所製「真空ラミネーターＭＶＬＰ」により、真空度１ミリバール（０．７５ｍｍＨｇ)、温度１００℃、そして圧力６ｋｇ／ｃｍ^{2}の条件で１５秒間プレスし、両面同時にラミネートした後、１２０℃で３０分、さらに１７０℃で３０分熱硬化させた。その後、ポリエチレンテレフタレートフィルムを剥離し、所定のスルーホールおよびビアホール部にドリル及びレーザーにより穴開けを行い、次いで過マンガン酸塩のアルカリ性酸化剤で熱硬化樹脂組成物層表面を粗化処理し、さらに導体層とは逆パターンのメッキレジストを形成させ、アディティブ法に従って多層プリント配線板を得た。

得られた多層プリント配線板は、１７０℃で６０分間アニール処理した後の導体ピール強度が１．１ｋｇ／ｃｍであった。また、絶縁層部分のユニバーサル硬度計から求められた弾性率は、室温で６．３ＧＰａ、そして１５０℃で４．８ＧＰａであった。

実施例８

実施例５におけると同様に、パターン加工された厚さ０．４ｍｍ、サイズ１０×３４０ｍｍのガラスエポキシ内層回路基板（導体厚３５μｍ）に、実施例１で得られた接着フィルムのポリプロピレンフィルムを剥離し、熱流動性樹脂組成物面を回路側として基板両面に枚葉した。次に、(株)名機製作所製「真空ラミネーターＭＶＬＰ」により、真空度１ミリバール（０．７５ｍｍＨｇ)、温度１００℃、そして圧力６ｋｇ／ｃｍ^{2}の条件で１５秒間プレスし、両面同時にラミネートし

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た後、１２０℃で３０分熱硬化させた。次に、実施例３で調製した熱硬化性樹脂組成物の樹脂ワニスを耐熱樹脂フィルム両面にロールコーティングし７０℃で２０分、さらに１５０℃で３０分熱硬化させた。得られた熱硬化粗化性樹脂組成物層の厚さは１０μｍであった。その後、所定のスルーホールおよびビアホール部にドリル及びレーザーにより穴開けを行い、次いで、過マンガン酸塩のアルカリ性酸化剤で熱硬化粗化性樹脂組成物層表面を粗化処理し、全面に無電解及び電解メッキにより導体層を形成した後、サブトラクティブ法に従って多層プリント配線板を得た。

得られた多層プリント配線板は、１７０℃で６０分間アニール処理した後の導体ピール強度は１．２ｋｇ／ｃｍであった。また、絶縁層部分のユニバーサル硬度計から求められた弾性率は、室温で６．２ＧＰａ、そして１５０℃で４．６ＧＰａであった。

実施例９

実施例５におけると同様に、厚さ０．４ｍｍ、サイズ５１０×３４０ｍｍのガラスエポキシ回路基板（導体厚３５μｍ）に、実施例４で得られた接着フィルムの４５μｍ厚熱硬化性樹脂組成物面の剥離性支持ベースフィルムを剥離し、熱硬化性樹脂組成物面を回路側として基板両面に枚葉した。次に、（株）名機製作所製「真空ラミネーターＭＶＬＰ」により、真空度１ミリバール（０．７５ｍｍＨｇ）、温度１１０℃、そして圧力６ｋｇ／ｃｍ^{2}の条件で１５秒間プレスし、両面同時にラミネートした後、１２０℃で３０分、さらに１７０℃で３０分熱硬化させた。その後、ポリエチレンテレフタレートフィルムを剥離し、所定のスルーホールおよびビアホール部にドリル及びレーザーにより穴開けを行い、次いで過マンガン酸塩のアルカリ性酸化剤で熱硬化樹脂組成物層表面を粗化処理し、さらに導体層とは逆パターンのメッキレジストを形成させ、アディティブ法に従って多層プリ

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ント配線板を得た。

この多層プリント配線板は、１７０℃で６０分間アニール処理した後の導体ピール強度は１．０ｋｇ／ｃｍであった。また、絶縁層部分のユニバーサル硬度計から求められた弾性率は、室温で５．６ＧＰａ、そして１５０℃で４．９ＧＰａであった。

比較例２

厚さ０．４ｍｍ、サイズ５１０×３４０ｍｍのガラスエポキシ回路基板（導体厚３５μｍ）に、比較例１で得られた接着フィルムのポリプロピレンフィルムを剥離し、熱硬化性樹脂組成物面を回路側として基板両面に枚葉した。次に、（株）名機製作所製「真空プレス機ＭＶＬＰ」により、真空度１ミリバール、温度１００℃、そして圧力６ｋｇ／ｃｍ^{2}の条件で１５秒間プレスし、両面同時にラミネートした。その後、支持ベースフィルムを剥離し、１７０℃で３０分熱硬化させた。その後、所定のスルーホールおよびビアホール部にドリル及びレーザーにより穴開けを行い、次いで過マンガン酸塩のアルカリ性酸化剤で粗化性樹脂組成物表面を粗化処理し、全面に無電解及び電解メッキにより導体層を形成した後、サブトラクティブ法に従って多層プリント配線板を得た。

この多層プリント配線板は、１７０℃で６０分でアニール処理した後の導体ピール強度は１．０ｋｇ／ｃｍであった。また、絶縁層部分のユニバーサル硬度計から求められた弾性率は、室温で４．８ＧＰａ、そして１５０℃で３．１ＧＰａであった。

比較例３

実施例１における樹脂ワニスを、実施例１におけると同様に両面プラズマ処理のポリイミドフィルム（（株）宇部興産製「ユーピレックスＳ」（厚さ１２．５μ

m)) 上に、乾燥後の樹脂厚みが６０μmとなるようにダイコーターにて塗布し、８０～１２０℃（平均１００℃）で２分間乾燥し（残留溶媒量約１０重量%)、乾燥後の熱硬化性樹脂組成物の表面に厚さ１５μmのポリプロピレンフィルムを貼り合わせながらロール状に巻き取った。ロール状の接着フィルムを幅５０７mmにスリット(slit)し、これより５０７×３３６mmサイズのシート状の接着フィルムを得た。

得られた接着フィルムの層構成はポリプロピレンフィルム層(保護フィルム層)／熱硬化性樹脂組成物層／ポリイミドフィルム層（耐熱樹脂層）である。

この熱硬化性樹脂組成物層を有する接着フィルムを実施例５におけると同様、厚さ０．４mm、サイズ５１０×３４０mmのガラスエポキシ回路基板（導体厚３５μm）に、熱硬化性樹脂組成物面を回路側として基板両面に枚葉した。次に、（株）名機製作所製「真空ラミネーターＭＶＬＰ」により、真空度１ミリバール（０．７５mmHg)、温度１００℃、そして圧力６kg／cm^{2}の条件で１５秒間プレスし、両面同時にラミネートした後、積層回路板を１２０℃で３０分、さらに１７０℃で３０分熱硬化させた。

しかしながら、この場合、熱硬化性樹脂組成物層の厚みが不均一となる上に、熱硬化性樹脂組成物中に気泡が発生してしまい、良好な絶縁層を形成することができなかった。

比較例４

実施例１における樹脂ワニスを、実施例１におけると同様に両面プラズマ処理のポリイミドフィルム（(株）宇部興産製「ユーピレックスＳ」(厚さ１２．５μm)）上に、乾燥後の樹脂厚みが６０μmとなるようにダイコーターにて塗布し、８０～１２０℃（平均１００℃）で１５分間乾燥し（残留溶媒量１重量%以下)、乾燥後の熱硬化性樹脂組成物の表面に厚さ１５μmのポリプロピレンフィルムを

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貼り合わせながらロール状に巻き取った。ロール状の接着フィルムを幅５０７ｍｍにスリット（slit）し、これより５０７×３３６ｍｍサイズのシート状の接着フィルムを得た。

得られた接着フィルムの層構成はポリプロピレンフィルム層(保護フィルム層)／熱硬化性樹脂組成物層／ポリイミドフィルム層（耐熱樹脂層）である。

この熱硬化性樹脂組成物層を有する接着フィルムを実施例５におけると同様、厚さ０．４ｍｍ、サイズ５１０×３４０ｍｍのガラスエポキシ回路基板（導体厚３５μｍ）に、熱硬化性樹脂組成物面を回路側として基板両面に枚葉した。次に、（株）名機製作所製「真空ラミネーターＭＶＬＰ」により、真空度１ミリバール（０．７５ｍｍＨｇ)、温度１００℃、そして圧力６ｋｇ／ｃｍ^{2}の条件で１５秒間プレスし、両面同時にラミネートした後、積層回路板を１２０℃で３０分、さらに１７０℃で３０分熱硬化させた。

しかしながら、この場合、回路間に熱硬化性樹脂の埋め込み不足による気泡が発生してしまい、良好な絶縁層を形成することができなかった。

（産業上の利用可能性）

本発明によれば、ビルトアップ工法により多層プリント配線板を製造する際に、機械強度に優れる絶縁層を簡便に導入することが可能な接着フィルムを得ることができ、更には機械強度に優れる多層プリント配線板を簡便に得ることができる。

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請求の範囲

1．少なくとも下記のA層及びB層を隣接して有し、B層を構成する熱硬化性樹脂組成物が、ラミネート温度より軟化点の低い樹脂を１０重量％以上含有し、回路基板へのラミネートと同時にスルホール及び／又はビアホール内の樹脂充填を行うことが可能な熱硬化性樹脂組成物であることを特徴とする多層プリント配線板用の接着フィルム。

A層：ポリイミド、液晶ポリマー、アラミド樹脂及びポリフェニレンスルフィドからなる群より選択される耐熱樹脂の少なくとも１種からなる厚さ２乃至３０μmの耐熱樹脂層、

B層：少なくとも１分子中に２以上のエポキシ基を有するエポキシ樹脂（成分（a））及びエポキシ硬化剤（成分（b））を含有する常温で固形状の熱硬化性樹脂組成物層。

2．少なくとも上記のA層及びB層を隣接して有し、B層を構成する熱硬化性樹脂組成物が、ラミネート温度より軟化点の低い樹脂を１０重量％以上含有し、温度７０乃至１４０℃、圧力１乃至２０kgf／cm^{2}及び気圧２０mmHg以下のラミネート条件において回路基板へのラミネートと同時にスルホール及び／又はビアホール内の樹脂充填を行うことが可能な熱硬化性樹脂組成物であることを特徴とする請求項１に記載の多層プリント配線板用の接着フィルム。

3．少なくとも前記のA層及びB層を隣接して有し、B層を構成する熱硬化性樹脂組成物が、更に重量平均分子量が５，０００乃至１００，０００である高分子化合物（成分（c））を５乃至５０重量％の割合で含有し、ラミネート温度より軟化点の低い樹脂の含有割合が１０重量％以上であり、かつ常温で液状の成分の含有割合が５乃至５５重量％であって、回路基板へのラミネートと同時にスルホール及び／又はビアホール内の樹脂充填を行うことが可能な熱硬化性樹脂組成

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物であることを特徴とする請求項１に記載の多層プリント配線板用の接着フィルム。

４．少なくとも前記のＡ層及びＢ層を隣接して有し、Ｂ層を構成する熱硬化性樹脂組成物が、更に重量平均分子量が５，０００乃至１００，０００である高分子化合物（成分（ｃ））を５乃至５０重量％で含有し、ラミネート温度より軟化点の低い樹脂の含有割合が１０重量％以上であり、かつ常温で液状の成分の含有割合が５乃至５５重量％であって、温度７０乃至１４０℃、圧力１乃至２０ｋｇｆ／ｃｍ^{2}及び気圧２０ｍｍＨｇ以下のラミネート条件において回路基板へのラミネートと同時にスルホール及び／又はビアホール内の樹脂充填を行うことが可能な熱硬化性樹脂組成物であることを特徴とする請求項３に記載の多層プリント配線板用の接着フィルム。

５．少なくとも前記のＡ層及びＢ層を隣接して有し、Ｂ層を構成する熱硬化性樹脂組成物が、測定開始温度６０℃、昇温速度５℃／分で加熱した場合の溶融粘度が、９０℃で４，０００乃至５０，０００ポイズ、１００℃で２，０００乃至２１，０００ポイズ、１１０℃で９００乃至１２，０００ポイズ、１２０℃で５００乃至９，０００ポイズ、そして１３０℃で３００乃至１５，０００である熱硬化性樹脂組成物であることを特徴とする請求項１に記載の多層プリント配線板用の接着フィルム。

６．耐熱樹脂層（Ａ層）及び熱硬化性樹脂組成物層（Ｂ層）が剥離性支持フィルム層（Ｃ層）上に形成されており、かつＢ層、Ａ層、そしてＣ層の順の層構成を有することを特徴とする請求項１乃至５のいずれかに記載の多層プリント配線板用の接着フィルム。

７．耐熱樹脂層（Ａ層）及び熱硬化性樹脂組成物層（Ｂ層）が剥離性支持フィルム層（Ｃ層）上に形成されており、かつＡ層、Ｂ層、そしてＣ層の順の層構成を有することを特徴とする請求項１乃至５のいずれかに記載の多層プリント配線

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板用の接着フィルム。

8．耐熱樹脂層（A層）及び熱硬化性樹脂組成物層（B層）が剥離性支持フィルム層（C層）上に形成されており、B層、A層、B層、そしてC層の順の層構成を有し、かつ少なくともC層に隣接するB層が酸化剤による粗化が可能であるものであることを特徴とする請求項1乃至5のいずれかに記載の多層プリント配線板用の接着フィルム。

9．熱硬化性樹脂組成物層（B層）のA層と隣接しない面が保護フィルム層（D層）又は剥離性支持フィルム層（C層）で保護されていることを特徴とする請求項6又は8のいずれかに記載の多層プリント配線板用の接着フィルム。

10．請求項1乃至9のいずれかに記載の多層プリント配線板用の接着フィルムを使用して製造されたことを特徴とする多層プリント配線板。

11．下記の工程（i）乃至（viii）を含むことを特徴とする多層プリント配線板の製造方法。

（i）請求項1乃至9のいずれかに記載の接着フィルムを、ラミネートの際に回路基板側に位置する熱硬化性樹脂組成物層（B層）が保護フィルム層（D層）又は剥離性支持フィルム層（C層）で保護されている場合はこれらの層を剥離した後、B層を回路基板側にして回路基板の片面又は両面にラミネートする工程、

（ii）剥離性支持フィルム層（C層）が存在する場合に必要により該C層を剥離する工程、

（iii）回路基板上にラミネートされた接着フィルムの熱硬化性樹脂組成物層（B層）を熱硬化し絶縁層を形成する工程、

（iv）剥離性支持フィルム層（C層）が存在する場合に該C層を剥離する工程、

（v）絶縁層が形成された回路基板に穴あけする工程、

（vi）絶縁層の表面を粗化処理する工程、

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（vii）粗化された絶縁層の表面にメッキにより導体層を形成させる工程、そして

（viii）導体層に回路形成する工程。

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図 1

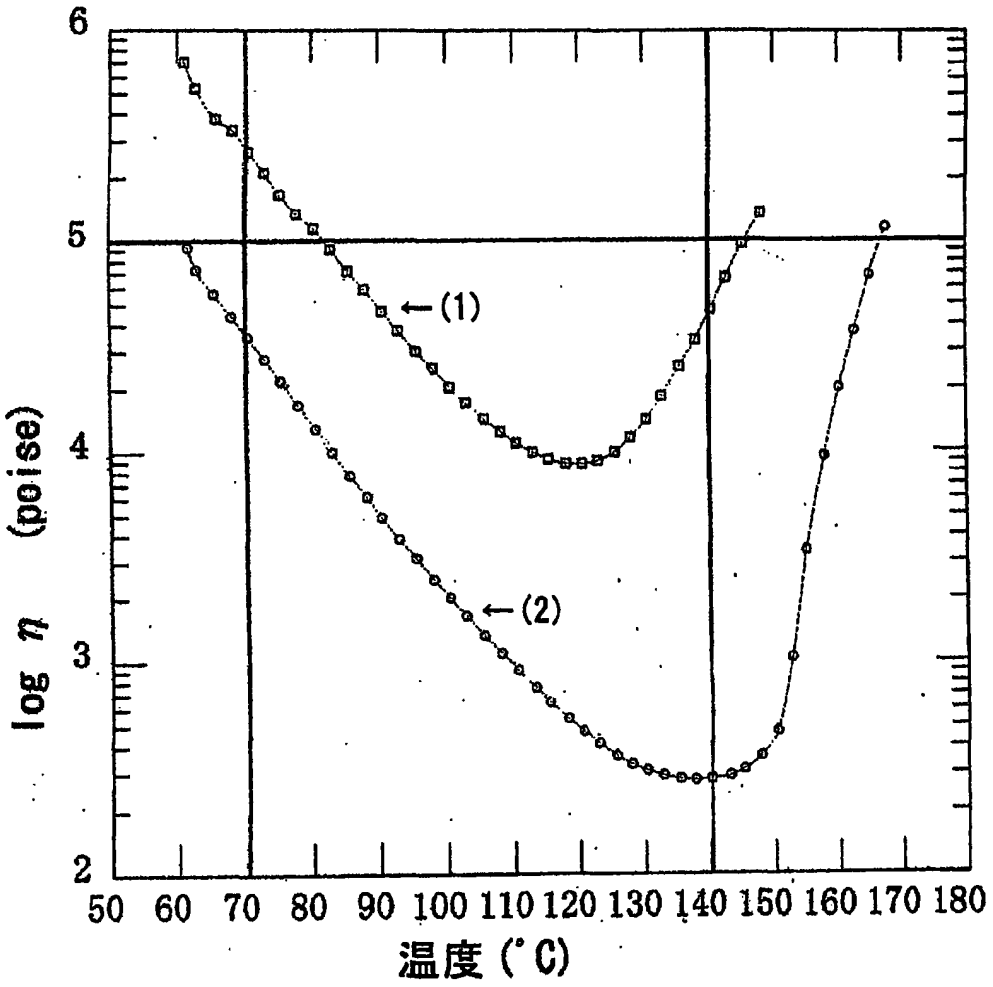

6
5
4
3
2
log η (poise)
←(1)
←(2)
50 60 70 80 90 100 110 120 130 140 150 160 170 180
温度 (°C)

図2

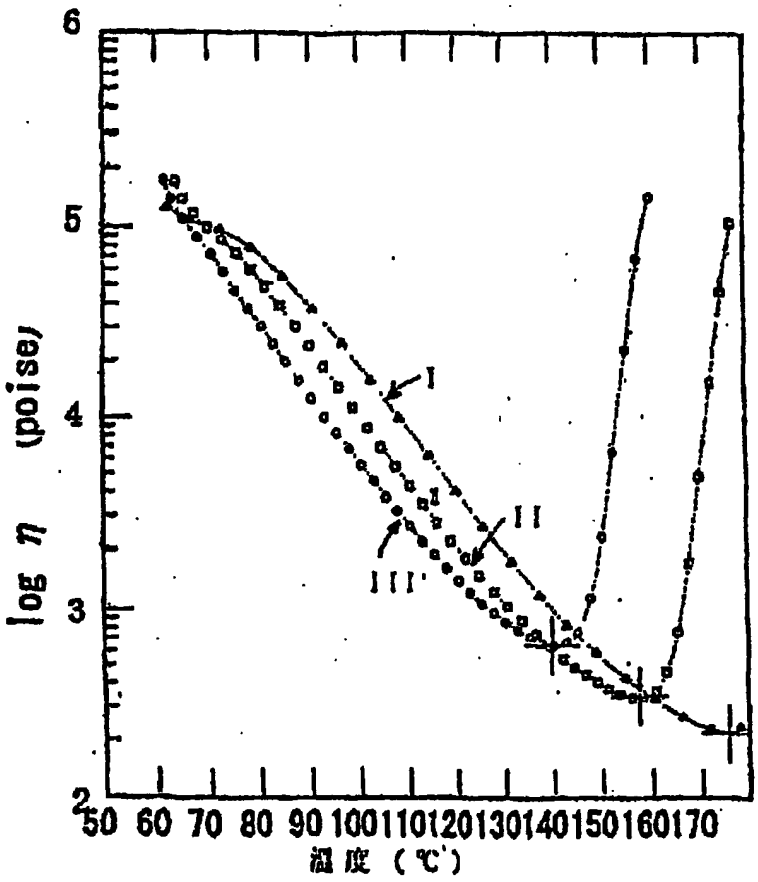

6
5
4
3
2
log η (poise)
I
II
III
50 60 70 80 90 100 110 120 130 140 150 160 170
温度 (℃)

図3

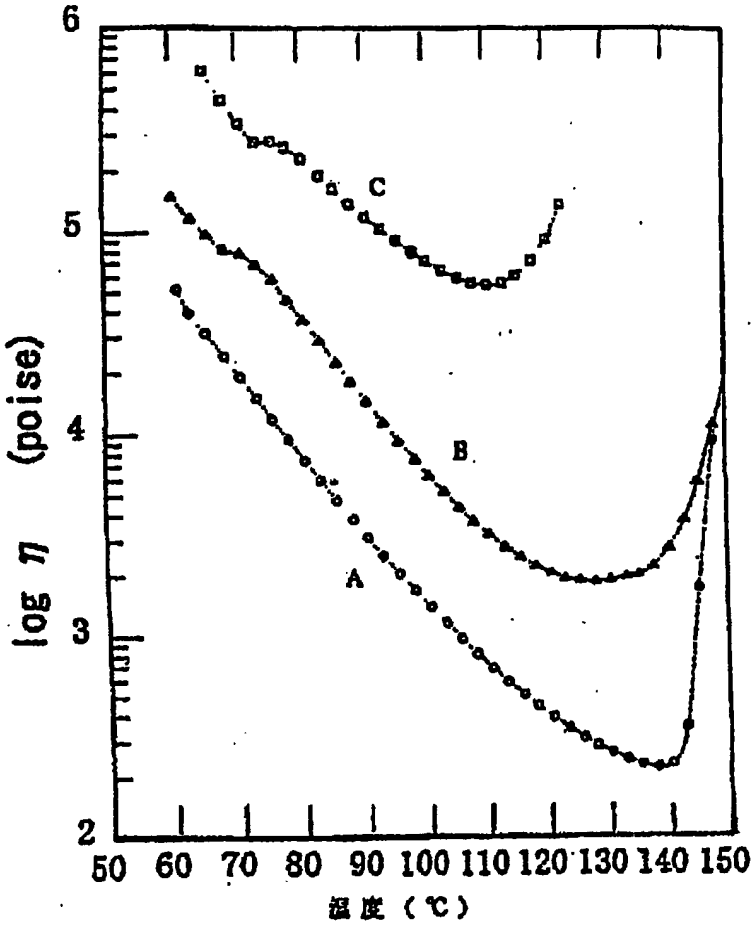
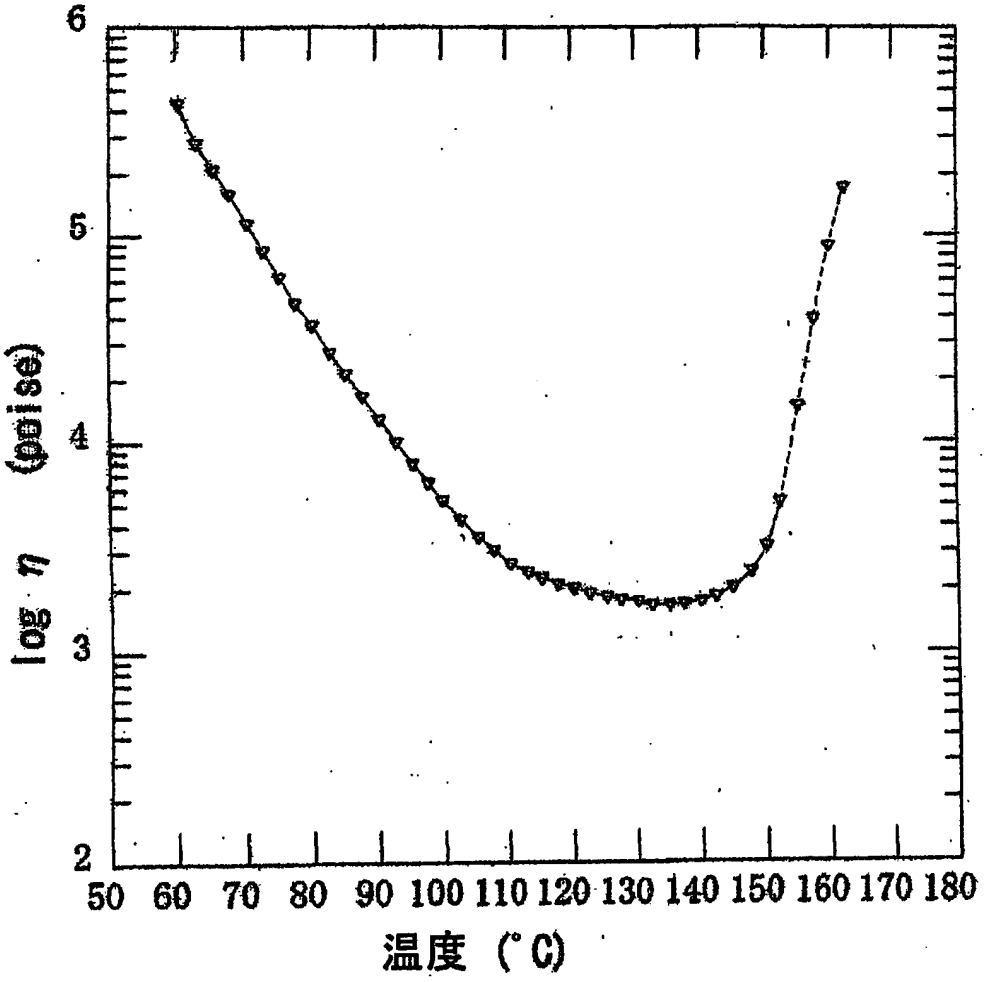


図4


6
5
4
3
2
log η (poise)
50 60 70 80 90 100 110 120 130 140 150 160 170 180
温度 (°C)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP01/04899

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H05K3/46, H05K3/38

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H05K3/46, H05K3/38

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926-1996 Toroku Jitsuyo Shinan Koho 1994-2001
Kokai Jitsuyo Shinan Koho 1971-2001 Jitsuyo Shinan Toroku Koho 1996-2001

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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A	JP 5-3388 A (Fujitsu Limited), 08 January, 1993 (08.01.93) (Family: none)	1-11
A	JP 7-202433 A (Ibiden Co., Ltd.), 04 August, 1995 (04.08.95) (Family: none)	1-11
A	JP 11-340625 A (Ajinomoto Co., Inc.), 10 December, 1999 (10.12.99) (Family: none)	1-11
A	JP 2000-104033 A (Sumitomo Bakelite Company, Limited), 11 April, 2000 (11.04.00) (Family: none)	1-11

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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24 August, 2001 (24.08.01)	04 September, 2001 (04.09.01)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
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Form PCT/ISA/210 (second sheet) (July 1992)

国際調査報告	国際出願番号 PCT／JP01／04899

A. 発明の属する分野の分類（国際特許分類（IPC））
Int. Cl' H05K3／46
H05K3／38

B. 調査を行った分野
調査を行った最小限資料（国際特許分類（IPC））
Int. Cl' H05K3／46
H05K3／38

最小限資料以外の資料で調査を行った分野に含まれるもの
日本国実用新案公報 1926－1996年
日本国公開実用新案公報 1971－2001年
日本国登録実用新案公報 1994－2001年
日本国実用新案登録公報 1996－2001年

国際調査で使用した電子データベース（データベースの名称、調査に使用した用語）

C. 関連すると認められる文献

引用文献のカテゴリー＊	引用文献名 及び一部の箇所が関連するときは、その関連する箇所の表示	関連する請求の範囲の番号
A	EP 851726 A2 (AJINOMOTO CO., INC.,) 1. 7月. 1998 (01. 07. 98) & JP 11－87927 A	1－11
A	JP 5－3388 A (富士通株式会社) 8. 1月. 1993 (08. 01. 93) (ファミリーなし)	1－11
A	JP 7－202433 A (イビデン株式会社) 4. 8月. 1995 (04. 08. 95) (ファミリーなし)	1－11

☒ C欄の続きにも文献が列挙されている。 ☐ パテントファミリーに関する別紙を参照。

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「&」同一パテントファミリー文献

国際調査を完了した日	国際調査報告の発送日
24. 08. 01	04.09.01

国際調査機関の名称及びあて先	特許庁審査官（権限のある職員）	3S	8509
日本国特許庁（ISA／JP） 郵便番号100－8915 東京都千代田区霞が関三丁目4番3号	中川 隆司 電話番号 03－3581－1101 内線 3390		

様式PCT／ISA／210（第2ページ）（1998年7月）

国際調査報告	国際出願番号　ＰＣＴ／ＪＰ０１／０４８９９

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Ａ	ＪＰ　２０００－１０４０３３　Ａ（住友ベークライト株式会社）１１．４月．２０００（１１．０４．００）（ファミリーなし）	１－１１

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(19) Europäisches Patentamt
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(11) EP 0 506 476 B1

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(22) Date of filing: **27.03.1992**

(54) Dielectric filter having coupling electrodes for connecting resonator electrodes, and method of adjusting frequency characteristic of the filter

Dielektrische Filter mit Koppelelektroden um Resonatoren oder Elektroden zu Verbinden, und Verfahren zur Einstellung der Frequenzcharakteristik des Filters

Filtre diélectrique avec des électrodes de couplage pour relier des résonateurs ou des électrodes, et méthode pour ajuster la caractéristique de fréquence du filtre

(84) Designated Contracting States:
DE FR GB IT

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(43) Date of publication of application:
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US-A- 4 673 902	**US-A- 4 963 843**

- **PATENT ABSTRACTS OF JAPAN vol. 12, no. 3 (E-570)(2850) 7 January 1988 & JP-A-62 164 301**
- **PATENT ABSTRACTS OF JAPAN vol. 12, no. 367 (E-664)(3214) 30 September 1988 & JP-A-63 119 302**

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EP 0 506 476 B1

Description

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates in general to a dielectric filter for the microwave spectrum of frequency and a method of adjusting the frequency characteristic of the dielectric filter. More particularly, the present invention is concerned with a small-sized dielectric filter constructed for excellent filtering properties, and a method by which the frequency characteristic of such dielectric filter can be easily adjusted.

Discussion of the Prior Art

In a microwave telecommunication system of modern vintage such as a portable or automobile telephone system, various filters using dielectric ceramics are used for minimizing the transmission loss. A known dielectric filter has a plurality of coaxial type resonators connected to each other. Each resonator is a dielectric block which has a central through-hole whose cylindrical surface is metallized to provide a central conductor serving as a resonating element. However, the central through-holes of the resonators have been a limiting factor to an effort to reduce the thickness and size of this type of dielectric filter. Further, this dielectric filter has a relatively large number of parts, and accordingly requires a cumbersome or complex fabrication process.

On the other hand, a three-layered or so-called tri-plate type dielectric filter as disclosed in laid-open Publication No. 59-51606 of unexamined Japanese Patent Application, for example, is free from such drawbacks. Namely, it is recognized in the art that the tri-plate type dielectric filter can be comparatively easily fabricated, with a considerably reduced thickness. An example of the dielectric filter of the tri-plate construction is illustrated in Figs. 12 and 13. This dielectric filter, which is indicated generally at 2 in Fig. 12, has a dielectric substrate 6 in which there is embedded a patterned array of an input and an output electrode 3 and a plurality of stripline resonator electrodes 4 (three electrodes 4 in this specific example). The outer surfaces of the dielectric substrate 6 are coated with a ground conductor 8 (respective conductive films 8), except certain areas on a pair of opposed side surfaces, on which an input and an output contact 10 are formed, respectively. Thus, the dielectric filter 2 is fabricated to be considerably compact and thin.

In the known tri-plate type dielectric filter 2 shown in Fig. 13, the resonator electrodes 4 are formed so as to provide a comb-shaped or interdigital structure, and the desired filtering properties are obtained by adjusting the spacing between the adjacent resonator electrodes 4. That is, the dielectric filter 2 does not have a circuit for electrically connecting the resonator electrodes 4. However, the applicants recognized a need for providing such an electrically connecting circuit so as to provide capacitors between the adjacent electrodes 4, in order to meet recent stringent requirements for improved properties of the dielectric filter for the microwave frequencies, which cannot be dealt with by the mere provision of a simple comb-shaped or interdigital structure of the resonator electrodes.

Conventionally, the final fine adjustment to obtain the desired frequency characteristic of the dielectric filter 2 is accomplished by trimming a portion of the ground conductor 8 which corresponds to the resonator electrodes 4, or by trimming the short-circuited ends of the electrodes 4 that are electrically connected to the conductor 8. However, the positions of the electrodes 4 embedded in the dielectric substrate 6 cannot be accurately detected, and the trimming is difficult to achieve the desired frequency characteristic of the filter.

SUMMARY OF THE INVENTION

The present invention was developed to solve the problem encountered in the prior art as described above. It is therefore a first object of this invention to provide a tri-plate type dielectric filter which exhibits improved filtering properties, without an increase in the size and the number of parts, as defined in claim 1.

A filter with the features of the preamble of claim 1 is known from patent document EP-A-0 414 619. Further advantageous embodiments are defined in claims 2 to 8.

A second object of the invention is to provide a method suitable for facilitating adjustment of the frequency characteristic of such dielectric filter, as defined in claim 9.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and optional objects, features and advantages of the present invention will be better understood by reading the following detailed description of presently preferred embodiments of the invention, when considered in connection with the accompanying drawings, in which:

Fig. 1 is a perspective view showing one embodiment of a dielectric filter of the present invention;
Fig. 2 is a cross sectional view taken along line 2-2 of Fig. 1;
Fig. 3 is a perspective view showing another embodiment of the dielectric filter of the invention;
Fig. 4 is a plan view of a first dielectric plate of the dielectric filter of Fig. 3;
Fig. 5 is a plan view of a second dielectric plate of the dielectric filter of Fig. 3;
Fig. 6 is a cross sectional view taken in a cutting plane indicated in dashed line in Figs. 4 and 5;
Fig. 7 is a view showing an equivalent circuit of the

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dielectric filter of Fig. 3;

Fig. 8 is a perspective view showing a further embodiment of the dielectric filter of this invention;

Fig. 9 is an exploded perspective view of the dielectric filter of Fig. 8;

Fig. 10 is a view showing an equivalent circuit of the dielectric filter of Fig. 8;

Fig. 11 is a graph indicating a relationship between the frequency and the damping effect of the filter of Figs. 8-10;

Fig. 12 is a perspective view showing a known dielectric filter; and

Fig. 13 is a cross sectional view taken along line 13-13 of Fig. 12.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring first to Figs. 1 and 2, there is shown one example of a three-layered or tri-plate type dielectric filter constructed according to the principle of the present invention. The dielectric filter, as indicated generally at 12 in Fig. 1, is a generally rectangular structure whose six surfaces include two opposite major surfaces and four side surfaces. All of these six surfaces are coated with a ground conductor 14, namely, with respective six conductive films 14. However, small areas on the opposite two longer side surfaces are left uncovered with the conductive films 14, so that respective two input and output contacts 16, 16 are formed on those areas, as shown in Figs. 1 and 2, such that the contacts 16 are electrically insulated from the ground conductor 14 (conductive films). Within the mass of the dielectric filter 12, there are embedded a plurality of resonator electrodes 18, an input and an output electrode 20, and a plurality of coupling electrodes 22, 26, as described below.

The dielectric filter 12 is a laminar structure fabricated by a common laminating method. The laminar structure includes a dielectric substrate 24 as shown in Fig. 2. On one major surface of this dielectric substrate 24, there is formed a patterned array of three parallel equi-spaced elongate strips 18 as the resonator electrodes. Further, the input and an output electrode 20 are formed on the same surface, such that these input and output electrodes 20 are electrically connected to the input and output contacts 16. These two electrodes 20 are positioned on the opposite sides of the array of the elongate strips 18. The three elongate strips 18 are formed in a comb-shaped pattern, so as to provide the respective resonators. The strips 18 have short-circuited first ends which are electrically connected to each other by means of the conductive film 14 formed on one of the opposite shorter side surfaces of the dielectric substrate 24. The other or second ends of the elongate strips 18 are located at a suitable distance inward of the other shorter side surface of the substrate 24. It will be understood that the parallel elongate strips 18 extend along the longer side surfaces of the substrate 24, and are spaced apart from each other in the direction parallel to the shorter side surfaces of the substrate 24.

The coupling electrodes 22 are formed integrally with the second ends of the elongate strips 18, such that each electrode 22 extends toward the second ends of the adjacent strips 18. As shown in Fig. 2, the coupling electrodes 22 formed with the strips 18 are spaced apart from each other in the direction perpendicular to the direction of extension of the strips 18, for capacitively connecting the elongate strips 18 at their second ends. The thus patterned array of the coupling electrodes 22 provides capacitors between the second ends of the adjacent strips 18. The capacitance values of these capacitors can be adjusted by suitably patterning the array of the electrodes 22, whereby the desired filtering property of the filter 12 can be obtained. This adjustment is not possible on the known dielectric filter.

Between the patterned array of the coupling electrodes 22 and the shorter side surface of the substrate 24 opposite to the shorter side surface at which the first ends of the elongate strips 18 are connected to each other by the conductive strip 14, there is formed a generally U-shaped coupling electrode 26 for capacitively connecting the two outer elongate strips 18 at their second ends. Namely, two capacitors are provided, one between one end of the coupling electrode 26 and one of the two outer strips 18, and the other between the other end of the electrode 26 and the other outer strip 18. The capacitance values of these capacitors can also be adjusted by suitably patterning the coupling electrode 26, whereby the frequency characteristic of the dielectric filter can be improved.

The provision of the coupling electrodes 22, 26 makes it possible to meet stringent requirements for improved characteristic of the filter 12, while maintaining the filter 12 sufficiently thin and small-sized, with the electrodes 22, 26 as well as the elongate strips (resonator electrodes) 18 being embedded in the mass of the dielectric filter 12. Thus, the improved dielectric filter 12 can be obtained without increasing the size or the number of process steps. It is to be noted that the coupling electrode 26 for capacitively connecting the two outer elongate strips 18 is not essential according to the principle of this invention.

Referring next to Figs. 3-7, there will be described another example of the tri-plate type dielectric filter, which is indicated generally at 28 in Fig. 3. The dielectric filter 28 is coated with the ground conductor 14, except for one of the opposite shorter side surfaces, on which the second ends of the elongate strips 18 (resonator electrodes) are exposed, as shown in Fig. 3. As in the first embodiment of Figs. 1 and 2, the first ends of the strips 18 are short-circuited, i.e., electrically connected to each other by the conductive film 14 on the other of the opposite short side surfaces of the filter 28. Unlike the input and output contacts 16 in the first embodiment, the contacts 16 in the present embodiment are formed

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on corner portions provided by the top surface and the opposite long side surfaces of the filter 28, which are adjacent to the opposite ends of the short side surface on which the second ends of the strips 18 are exposed. These input and output contacts 16 are electrically insulated from the conductive films 14 on the top and long side surfaces of the filter 28. Namely, the corner portions indicated above are left uncovered by the conductive films 14.

The dielectric filter 28 uses two dielectric substrates 30, 32 as shown in Figs. 4 and 5, respectively. The patterned array of equi-spaced parallel elongate strips 18 is formed on the first dielectric substrate 30, while the three coupling electrodes 22 for capacitively connecting the adjacent elongate strips 18 are formed on the second dielectric substrate 32. The first ends of the strips 18 are short-circuited on one of the opposite shorter side surfaces of the first substrate 30, while the second ends of the strips 18 are exposed on one of the opposite shorter side surfaces of the second substrate 32, which is opposite to the above-indicated one shorter side surface of the first substrate 30. The three coupling electrodes 22 are patterned such that these electrodes 22 are positioned right above and spaced apart from the second ends of the corresponding strips 18 when the first and second substrates 30, 32 are superposed on each other. A green laminar structure consisting of the superposed first and second substrates 30, 32 is fired into a blank for the dielectric filter 28.

The thus prepared blank for the dielectric filter 28 is trimmed at a suitable position as indicated in dashed lines in Figs. 4 and 5, which indicate a trimming plane which corresponds to the shorter side surface of the filter 28 on which the second ends of the strips 18 and the corresponding coupling electrodes 22 are exposed, as shown in Fig. 6.

Reference is now made to Fig. 7 showing an equivalent circuit of the dielectric filter 28. The equivalent circuit includes three resonators 34 corresponding to the three elongate strips 18, three capacitors 36 provided between the strips 18 and the coupling electrodes 22, and two capacitors 38 provided between the adjacent electrodes 22. The capacitance values of these capacitors 36, 38 can be adjusted as desired by suitably patterning the coupling electrodes 22, whereby the desired filtering property can be obtained, without increasing the size and complexity of the filter 28, with the coupling electrodes 22 embedded within the first and second dielectric substrate 30, 32.

In the present second embodiment, the coupling electrodes 22 are provided on the second dielectric substrate 32 and are spaced apart from the second ends of the elongate strips or resonator electrodes 18. Accordingly, the coupling electrodes 22 have a higher degree of freedom of patterning, without a design limitation by the second ends of the strips 18 as existing in the first embodiment. Thus, the present arrangement permits a relatively complicated circuit for capacitive connection of the second ends of the elongate strips 18 by the coupling electrodes 22.

In the second embodiment, the two outer coupling electrodes 22 serve also as the input and output electrodes (20), which are exclusively provided in the first embodiment. As shown in Fig. 7, these two outer coupling electrodes 22 provide respective capacitors 40 associated with the input and output contacts 16. The capacitance values of these input and output capacitors 40 can also be adjusted by suitably patterning the two outer coupling electrodes 22.

As described above, the dielectric filter 28 is trimmed at the second ends of the elongate strips 18 and the corresponding coupling electrodes 22, for fine adjustment of the frequency characteristic of the filter. The trimming operation for this adjustment is simple and easy, contributing to improved efficiency of fabrication of the filter 28.

Referring further to Figs. 8-11, there will be described a further example of the tri-plate type dielectric filter, which is indicated generally at 42 in Fig. 8. The dielectric filter 42 is coated with the ground conductor 14, except for some areas of one of the opposite short side surfaces, on which the second ends of the respective elongate strips 18 are exposed, as shown in Fig. 8. That is, parallel spaced-apart elongate conductive strips 14a are formed on the above-indicated one short side surface of the dielectric filter 42, such that these conductive strips 14a define areas on which the respective elongate strips 18 of the resonator electrodes are exposed.

As in the first and second embodiments of Figs. 1-7, the first ends of the strips 18 are short-circuited by the conductive film 14 on the other of the opposite short side surfaces of the filter 42. As in the first embodiment of Fig. 1-2, the contacts 16 in this embodiment are formed on the opposite long side surfaces of the filter 42, and are electrically insulated from the conductive films 14 on the long side surfaces of the filter 42.

More specifically, four substrates 44, 46, 48, 50 as shown in Fig. 9 are superposed on each other so as to form the dielectric filter 42 in which are embedded the coupling electrodes 22, elongate strips 18 and input and output electrodes 20. As shown in Fig. 9, the elongate strips 18 are formed on the third dielectric substrate 48 whose first ends are short-circuited by the conductive film 14 and whose seconds ends are exposed between the adjacent conductive strips 14a on one of the opposite short side surfaces of the filter 42, as described above. Further, the two coupling electrodes 22 for capacitively connecting the elongate strips 18 are formed on the second dielectric substrate 46 such that the coupling electrodes 22 are positioned right above and spaced apart from the second ends of the elongate strips 18. A green laminar structure consisting of the superposed four substrates 44, 46, 48, 50 is fired into a blank for the dielectric filter 42.

There is illustrated in Fig. 10 an equivalent circuit of

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the dielectric filter 42, which includes three resonators 34 corresponding to the three elongate strips 18, and four capacitors 36 provided between the strips 18 and the coupling electrodes 22. The adjacent resonators 34 are electrically connected to each other through the capacitors 36 and the coupling electrodes 22. The capacitance values of the capacitors 36 can be adjusted as desired by suitably patterning the coupling electrodes 22 so as to obtain the desired filtering property.

Further, the elongate conductive strips 14a of the conductor 14 effectively eliminate a difference in potential between the conductive films 14 on the opposite top and bottom surfaces of the dielectric filter 42, thereby assuring improved stability of the filtering characteristics of the filter 42.

The equivalent circuit also includes three capacitors 52 between the exposed or second end portions of the elongate strips 18 and the elongate conductive strips 14a on the corresponding short side surface of the dielectric filter 42, as indicated in Fig. 10. In the presence of these capacitors 52, the elongate strips 18 serving as the resonator electrodes are made inductive with respect to the resonance frequency, whereby there are provided an inductor M between the adjacent resonators 34. Thus, each resonator 34 is provided with a capacitor 36 and an inductor M, and the effect of damping by the instant dielectric filter on the input microwave spectrum is smaller in a frequency band of the spectrum lower than the pass band, than the effect of damping by the known dielectric filter, as indicated in the graph of Fig. 11. This means improved capability of filtering the desired frequency band. In addition, the provision of the capacitors 52 makes it possible to reduce the length of the resonators 34, for the same resonance frequency, thereby contributing to reduction in the size of the dielectric filter 42.

According to the present invention, the resonator electrodes 18 in the form of the elongate strips and the coupling electrodes 22 which are entirely embedded within the dielectric substrate (24) or substrates (30, 32; 44, 46, 48, 50) are preferably formed of an electrically conductive material whose resistivity is relatively small, whose major component or components is/are Au, Ag and/or Cu, for example. Since the loss at the electrodes 18, 22 increases the loss of the filter in the pass band, it is desired that the resistivity of the connecting circuit be sufficiently low, particularly where the filter deals with the electromagnetic wavelengths in the microwave spectrum.

Where a Ag- or Cu-based electrically conductive material is used for the electrodes 18, 22, it is necessary to use a dielectric material (for the dielectric substrate or substrates 24, 30, 32) which can be fired or sintered at a temperature lower than the melting point (1100°C or lower) of such electrically conductive material, since the melting point of the Ag- or Cu-based conductive material is too low to permit co-firing of the conductive material with an ordinary dielectric material. Where the dielectric filter is used as a microwave filter, it is desirable that the dielectric material is selected to assure that the temperature coefficient of the resonance frequency of resonance circuits corresponding to the resonator electrodes 18 be held not higher than ±50ppm/°C. Examples of the preferred dielectric material include: a glass composition consisting of a mixture of a cordierite glass powder, a TiO_2 powder and a $Nd_2Ti_2O_7$ powder; and a mixture consisting of a BaO-TiO_2-RE_2O_3-Bi_2O_3 composition (RE: rare earth component) and a small amount of a glass forming component or a glass powder.

To further clarify the present invention, there will be described some examples of the present invention. However, it is to be understood that the invention is not limited to the details of the following examples, but may be embodied with various changes, modifications and improvements, which may occur to those skilled in the art, without departing from the spirit of the invention.

Example 1

A powder mixture was prepared by sufficiently mixing 73 wt.% of a glass powder, 17wt.% of a TiO_2 powder and 10 wt.% of an $Nd_2Ti_2O_7$ powder. The glass powder consists of 18 wt.% of MgO, 37 wt.% of Al_2O_3, 37 wt.% of SiO_2, 5 wt.% of B_2O_3 and 3 wt.% of TiO_2. The $Nd_2Ti_2O_7$ powder was obtained by mixing Nd_2O_3 powder and TiO_2 powder, calcining the mixture at 1200°C, and milling the calcined powder mass. To the prepared powder mixture, there were added an acrylic-based organic binder , a plasticizer, toluene and alcohol solvents. The powder mixture and these additives were well mixed by alumina balls, whereby a slurry was obtained. Using the slurry, green tapes having a thickness of 0.2-0.5mm were formed by a doctor-blade method.

On the other hand, a Ag powder, an acrylic-based organic binder and a terpineol-based organic solvent were sufficiently kneaded by a three-roll method, whereby an electrically conductive printing paste was prepared. Using the printing paste, a pattern of electrically conductive material corresponding to the electrodes 18, 20, 22, 26 as shown in Fig. 2 was formed on some of the green tapes, while a conductive layer corresponding to the ground conductive films 14 was formed on one surface of the other green tapes. One green tape having the pattern of electrodes and two green tapes each having the conductive layer were superposed on each other so that the pattern of electrodes are interposed by the two green tapes having the conductive layers, such that the two conductive layers form the opposite surfaces of the obtained laminar green tape. The laminar green tape was compacted at 100°C under 100kg/cm^2. The compacted laminar green tape was cut into pieces each corresponding to the dielectric filter 12 of Fig. 1. Then, the printing paste was applied to the four side surfaces of each piece, to form conductive pads corresponding to the input and output contacts, and conductive layers corresponding to the conductive films 14 on the four side

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surfaces of the filter 12. Thus, a plurality of precursors for the dielectric filter 12 were prepared. These precursors were fired in the atmosphere, for 30 minutes at 900°C, whereby thin microwave filters having a total thickness of 2mm were produced.

These filters had a band width of 20MHz and an insertion loss of 3dB, where the nominal frequency was 900MHz. A sintered test piece was prepared by using the powder mixture described above. The test piece was ground to predetermined dimensions, and its temperature coefficient of the resonance frequency in the microwave spectrum was measured according to Hakki & Coleman method, over a temperature range from -25°C to +75°C. The measured temperature coefficient was +10ppm/°C.

Example 2

A powder mixture was prepared by sufficiently mixing 73 wt.% of a glass powder, 17wt.% of a TiO_2 powder and 10 wt.% of an $Nd_2Ti_2O_7$ powder. The glass powder consists of 17 wt.% of MgO, 37 wt.% of Al_2O_3, 37 wt.% of SiO_2, 5 wt.% of B_2O_3, 3 wt.% of TiO_2 and 1 wt.% of MnO. The TiO_2 powder was obtained by mixing commercially available TiO_2 and MnO powders, calcining the mixture at 1200°C, and milling the calcined powder mass. The $Nd_2Ti_2O_7$ powder was obtained by Nd_2O_3 powder, TiO_2 powder and MnO powder, calcining the mixture at 1200°C, and milling the calcined powder mass.

To the prepared powder mixture, there were added an acrylic-based organic binder , a plasticizer, toluene and alcohol solvents. The powder mixture and these additives were mixed by alumina balls, whereby a slurry was obtained. Using the slurry, green tapes having a thickness of 0.2-0.5mm were formed by a doctor-blade method.

On the other hand, a Cu powder, an acrylic-based organic binder and a terpineol-based organic solvent were sufficiently kneaded by a three-roll method, whereby an electrically conductive printing paste was prepared. Using the printing paste, a pattern of electrodes and a conductive layer were printed on the green tapes, and compacted laminar green tapes for the filter 12 of Fig. 1 were prepared, as in Example 1. Then, precursors for the dielectric filter 12 were prepared by applying the printing paste to the laminar green tapes, as in Example 1. The precursors were fired in a nitrogen atmosphere, for 30 minutes at 950°C, whereby thin microwave filters having a total thickness of 2mm were produced. These filters had a band width of 30MHz and an insertion loss of 3.5dB, where the nominal frequency was 900MHz.

Example 3

A pattern of electrically conductive material corresponding to the resonator electrodes 18, 20, 22, 26 was printed on the green tapes as prepared in Example 1, by using a Ag paste, and compacted laminar green tapes for the filter 12 were prepared. Then, a commercially available Cu paste was applied to form conductive films and pads corresponding to the ground conductive films 14 and input and output contacts 16, whereby precursors for the filter 12 of Fig. 1 were obtained. The precursors were fired in the atmosphere, for 30 minutes at 600°C, into 2-mm thick microwave filters. These filters had a band width of 20 MHz and an insertion loss of 3dB, where the nominal frequency was 900MHz.

Example 4

A powder mixture was prepared by adding a total of 8 wt.% of a low-melting point glass powder and a low-melting point metal oxide powder, to 92 wt.% of a powdered BaO-TiO_2-Nd_2O_3-Bi_2O_3 composition. To the prepared powder mixture, there were added an acrylic-based organic binder , a plasticizer, toluene and alcohol solvents. The powder mixture and these additives were well mixed by alumina balls, whereby a slurry was obtained. Using the slurry, green tapes having a thickness of 0.2-0.5mm were formed by a doctor-blade method.

On the other hand, a Ag powder, an acrylic-based organic binder and a terpineol-based organic solvent were sufficiently kneaded by a three-roll method, whereby an electrically conductive printing paste was prepared. Using the printing paste, a pattern of electrically conductive material corresponding to the resonator electrodes 18 as shown in Fig. 4 was formed on some of the green tapes, while a pattern of electrically conductive material corresponding to the coupling electrodes 22 were formed on the other green tapes. Further, a conductive layer corresponding to the ground conductive film 14 and conductive pads corresponding to the input and output contacts 16 as shown in Fig. 3 were formed on one surface of the yet other green tapes. The following four green tapes were superposed on each other in the order of description: one green tape having the conductive layer and the two conductive pads; two green tapes one having the pattern for the resonant electrodes 18 and the other having the pattern for the coupling electrodes 22; and one green tape having the conductive layer. The prepared laminar green tape was compacted at 100°C under 100kg/cm^2. The compacted laminar green tape was cut into pieces each corresponding to the dielectric filter 28 of Fig. 3. Then, the printing paste was applied to the four side surfaces of each piece, to form conductive layers corresponding to the conductive films 14 on the four side surfaces of the filter 28. Thus, a plurality of precursors for the dielectric filter 28 were prepared. These precursors were fired in the atmosphere, for 30 minutes at 900°C, whereby thin microwave filters having a total thickness of 2mm were produced.

These filters 28 had a band width of 20MHz and an insertion loss of 3dB, where the nominal frequency was 900MHz. A sintered test piece was prepared by using

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the powder mixture used for producing the filters 28. The test piece was ground to predetermined dimensions, and its temperature coefficient of the resonance frequency in the microwave spectrum was measured according to Hakki & Coleman method, over a temperature range from -25°C to +75°C. The measured temperature coefficient was +15ppm/°C. Before the measurement, a fine adjustment of the frequency characteristic of the test piece was made by trimming the second ends of the resonator electrodes 18 and the coupling electrodes 22.

Example 5

A powder mixture was prepared by adding a total of 8 wt.% of a low-melting point glass powder and a low-melting point metal oxide powder, to 92 wt.% of a powdered BaO-TiO_2-Nd_2O_3-Bi_2O_3 composition. To the prepared powder mixture, there were added an acrylic-based organic binder , a plasticizer, toluene and alcohol solvents. The powder mixture and these additives were well mixed by alumina balls, whereby a slurry was obtained. Using the slurry, green tapes having a thickness of 0.2-0.5mm were formed by a doctor-blade method.

On the other hand, a Ag powder, an acrylic-based organic binder and a terpineol-based organic solvent were sufficiently kneaded by a three-roll method, whereby an electrically conductive printing paste was prepared. Using the printing paste, patterns of electrically conductive material corresponding to the resonator electrodes 18, input and output electrodes 20 and coupling electrodes 22 as shown in Fig. 9 were formed on respective green tapes for the third, fourth and second dielectric substrates 48, 50 and 46. Further, conductive films corresponding to the top and bottom conductor films 14 were formed on the appropriate green tapes. The green tapes having the conductive patterns and films were superposed on each other in the appropriate order. The thus prepared laminar green tape was compacted at 100°C under 100kg/cm^2. The compacted laminar green tape was cut into pieces each corresponding to the dielectric filter 42 of Fig. 8. Then, the printing paste was applied to the four side surfaces of each piece, to form conductive layers corresponding to the conductive films 14 and strips 14a on the four side surfaces of the filter 42. Thus, a plurality of precursors for the dielectric filter 42 were prepared. These precursors were fired in the atmosphere, for 30 minutes at 900°C, whereby thin microwave filters having a total thickness of 2mm were produced.

These filters 42 had a band width of 20MHz and an insertion loss of 3dB, where the nominal frequency was 900MHz. A sintered test piece was prepared by using the powder mixture used for producing the filters 42. The test piece was ground to predetermined dimensions, and its temperature coefficient of the resonance frequency in the microwave spectrum was measured according to Hakki & Coleman method, over a temperature range from -25°C to +75°C. The measured temperature coefficient was +15ppm/°C. Before the measurement, a fine adjustment of the frequency characteristic of the test piece was made by trimming the second ends of the resonator electrodes 18 and the coupling electrodes 22.

Claims

1. A tri-plate type dielectric filter having a dielectric substrate (24;30,32;44,46,48,50) and a plurality of resonator electrodes (18) embedded in said substrate, characterized in that coupling electrodes (22,26) are formed within said dielectric substrate spaced from said resonator electrodes, for capacitively coupling said plurality of resonator electrodes, so as to provide capacitors (36,38) each between adjacent ones of said resonator electrodes.

2. A tri-plate type dielectric filter according to claim 1, wherein a ground conductor (14,14a) is provided on a first outer surface of said dielectric substrate (24; 30,32;44,46,48,50), and said plurality of resonator electrodes (18) have short-circuited first ends connected to each other by said ground conductor.

3. A tri-plate type dielectric filter according to claim 2, wherein said plurality of resonator electrodes (18) consist of a plurality of elongate strips, respectively, said elongate strips being formed substantially in parallel with each other.

4. A tri-plate type dielectric filter according to claim 2 or claim 3, wherein each of said resonator electrodes (18) has a second end opposite to said short-circuit first end thereof, further coupling electrodes (22) being formed integrally with said second ends of said resonator electrodes.

5. A tri-plate type dielectric filter according to any one of the preceding claims, wherein said coupling electrodes (22,26) include a coupling electrode (26) for capacitively coupling the two outermost electrodes of said resonator electrodes (18).

6. A tri-plate type dielectric filter according to any one of claims 2 to 5, wherein each of said resonator electrodes (18) provides a stripline type $\lambda/4$ or $\lambda/2$ TEM mode resonance circuit, and has a second end which is exposed on a second outer surface of said dielectric substrate (30,32;44,46,48,50).

7. A tri-plate type dielectric filter according to claim 6, wherein said coupling electrodes (22) correspond to said resonator electrodes (18), respectively, said exposed second end of each said resonator electrodes (18) being spaced from a corresponding one of said coupling electrodes (22), in a direction of thickness of said dielectric substrate (30,32;

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44,46,48,50).

8. A tri-plate type dielectric filter according to claim 6 or claim 7, wherein said ground conductor (14,14a) includes a top and a bottom conductive films (14) formed on opposite top and bottom surfaces as said first outer surface of said dielectric substrate (44,46,48,50), respectively, and a plurality of conductive strips (14a) formed on a side surface as said second outer surface of said dielectric substrate, so as to electrically connect said top and bottom conductive films (14), such that said second ends of said resonator electrodes (18) are electrically insulated from said conductive strips (14a).

9. A method of adjusting a frequency characteristic of a tri-plate type dielectric filter as defined in any one of claims 6 to 8, characterized by comprising the step of trimming said second end of each said resonator electrodes (18), to thereby adjust a resonance frequency of the corresponding resonance circuit.

Patentansprüche

1. Dielektrisches Filter vom Dreiplatten-Typ mit einem dielektrischen Substrat (24;30, 32; 44, 46, 48, 50) und einer Vielzahl von im Substrat eingebetteten Resonatorelektroden (18), dadurch gekennzeichnet, daß Kopplungselektroden (22, 26) innerhalb des dielektrischen Substrats im Abstand von den Resonatorelektroden ausgebildet sind, um die Vielzahl von Resonatorelektroden kapazitiv zu koppeln, um Kondensatoren bzw. Kapazitäten (36, 38) jeweils zwischen benachbarten Resonatorelektroden bereitzustellen bzw. vorzusehen.

2. Dielektrisches Filter vom Dreiplatten-Typ nach Anspruch 1, worin ein Masseleiter (14, 14a) an einer ersten Außenfläche des dielektrischen Substrats (24; 30, 32; 44, 46, 48, 50) vorgesehen ist und die Vielzahl von Resonatorelektroden (18) kurzgeschlossene erste Enden aufweist, die durch den Masseleiter miteinander verbunden sind.

3. Dielektrisches Filter vom Dreiplatten-Typ nach Anspruch 2, worin die Vielzahl von Resonatorelektroden (18) aus einer Vielzahl jeweiliger länglicher Streifen besteht, wobei die länglichen Streifen im wesentlichen parallel zueinander ausgebildet sind.

4. Dielektrisches Filter vom Dreiplatten-Typ nach Anspruch 2 oder 3, worin jede der Resonatorelektroden (18) ein zweites Ende gegenüber seinem kurzgeschlossenen ersten Ende aufweist, wobei weiters Kopplungselektroden (22) einstückig mit den zweiten Enden der Resonatorelektroden ausgebildet sind.

5. Dielektrisches Filter vom Dreiplatten-Typ nach einem der vorangegangenen Ansprüche, worin die Kopplungselektroden (22, 26) eine Kopplungselektrode (26) zum kapazitiven Koppeln der beiden äußersten Elektroden der Resonatorelektroden (18) umfassen.

6. Dielektrisches Filter vom Dreiplatten-Typ nach einem der Ansprüche 2 bis 5, worin jede der Resonatorelektroden (18) eine Streifenleitungsresonanzschaltung vom $\lambda/4$- oder $\lambda/2$ TEM-Mode bereitstellt und ein zweites Ende aufweist, das auf einer zweiten Außenfläche des dielektrischen Substrats (30, 32; 44, 46, 48, 50) freiliegt.

7. Dielektrisches Filter vom Dreiplatten-Typ nach Anspruch 6, worin die Kopplungselektroden (22) den Resonatorelektroden (18) jeweils entsprechend und das freiliegende zweite Ende einer jeden der Resonatorelektroden (18) von einer entsprechenden der Kopplungselektroden (22) in einer Dikkerichtung des dielektrischen Substrats (30, 32; 44, 46, 48, 50) beabstandet ist.

8. Dielektrisches Filter vom Dreiplatten-Typ nach Anspruch 6 oder 7, worin der Masseleiter (14, 14a) einen obersten und einen untersten leitenden Film (14) umfaßt, die auf gegenüberliegenden Deck- bzw. Bodenflächen als der ersten Außenfläche des dielektrischen Substrats (44, 46, 48, 50) ausgebildet sind, sowie eine Vielzahl leitender Streifen (14a), die auf einer Seitenfläche als der zweiten Außenfläche des dielektrischen Substrats ausgebildet sind, um den obersten und untersten leitenden Film (14) elektrisch zu verbinden, sodaß die zweiten Enden der Resonatorelektroden (18) elektrisch von den leitenden Streifen (14a) isoliert sind.

9. Verfahren zum Einstellen einer Frequenzcharakteristik eines dielektrischen Filters vom Dreiplatten-Typ, wie nach einem der Ansprüche 6 bis 8 definiert, dadurch gekennzeichnet, daß es den Schritt des Trimmens des zweiten Endes einer jeden Resonatorelektrode (18) umfaßt, um dadurch eine Resonanzfrequenz der entsprechenden Resonanzschaltung bzw. des entsprechenden Resonanzkreises einzustellen.

Revendications

1. Filtre diélectrique du type à trois plaques ayant un substrat diélectrique (24;30,32;44,46,48,50) et un certain nombre d'électrodes de résonateur (18) enfouies dans ledit substrat, caractérisé en ce que des électrodes de couplage (22,26) sont formées

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dans ledit substrat diélectrique espacées desdites électrodes de résonateur, pour coupler capacitivement ladite pluralité d'électrodes de résonateur, afin de réaliser les condensateurs (36,38) chacun entre les électrodes adjacentes des électrodes de résonateur.

2. Filtre diélectrique du type à trois plaques selon la revendication 1, dans lequel un conducteur de masse (14, 14a) est prévu sur une première surface externe du substrat diélectrique précité (24;50,52; 44,56,48,50) et la pluralité précitée d'électrodes de résonateur (18) ont des premières extrémités court-circuitées reliées les unes aux autres par le conducteur de masse.

3. Filtre diélectrique du type à trois plaques selon la revendication 2, dans lequel la pluralité précitée d'électrodes de résonateur (18) consistent en un certain nombre de bandes allongées, respectivement, lesdites bandes allongées étant formées sensiblement parallèles les unes aux autres.

4. Filtre diélectrique du type à trois plaques selon la revendication 2 ou la revendication 3, dans lequel chacune des électrodes de résonateur précitées (18) a une seconde extrémité opposée à la première extrémité court-circuitée précitée de celles-ci, des électrodes de couplage (22) étant de plus formées intégralement avec lesdites secondes extrémités desdites électrodes de résonateur.

5. Filtre diélectrique du type à trois plaques selon l'une quelconque des revendications précédentes, dans lequel les électrodes de couplage précitées (22,26) comprennent une électrode de couplage (26) pour coupler capacitivement les deux électrodes les plus externes des électrodes de résonateur précitées (18).

6. Filtre diélectrique du type à trois plaques selon l'une quelconque des revendications 2 à 5, dans lequel chacune des électrodes de résonateur précitées (18) réalise un circuit de résonance en mode TEM $\lambda/4$ ou $\lambda/2$ du type à ligne de bande, et a une seconde extrémité qui est exposée sur une seconde surface externe du substrat diélectrique précité (30,32;44,46, 48,50).

7. Filtre diélectrique du type à trois plaques selon la revendication 6, dans lequel les électrodes de couplage précitées (22) correspondent respectivement aux électrodes de résonateur précitées (18), la seconde extrémité exposée précitée de chacune desdites électrodes de résonateur (18) étant espacée de l'une correspondante desdites électrodes de couplage (22), dans une direction d'épaisseur dudit substrat diélectrique (30,32;44,46,48,50).

8. Filtre diélectrique du type à trois plaques selon la revendication 6 ou la revendication 7, dans lequel le conducteur de masse précité (14,14a) comprend un film conducteur supérieur et un film conducteur inférieur (14) formés sur des surfaces supérieure et inférieure opposées comme première surface externe précitée du substrat diélectrique précité (44,46,48,50), respectivement, et un certain nombre de bandes conductrices (14a) formées sur une surface latérale comme la seconde surface externe précitée dudit substrat diélectrique, afin de relier électriquement lesdits films conducteurs supérieur et inférieur (14), de sorte que les secondes extrémités précitées des électrodes de résonateur précitées (18) sont isolées électriquement desdites bandes conductrices (14a).

9. Procédé de réglage d'une caractéristique de fréquence d'un filtre diélectrique du type à trois plaques comme défini dans l'une quelconque des revendications 6 à 8, caractérisé en ce qu'il comprend l'étape d'ajuster la seconde extrémité précitée de chacune des électrodes de résonateur précitées (18), pour régler de la sorte une fréquence de résonance du circuit de résonance correspondant.

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FIG. 1

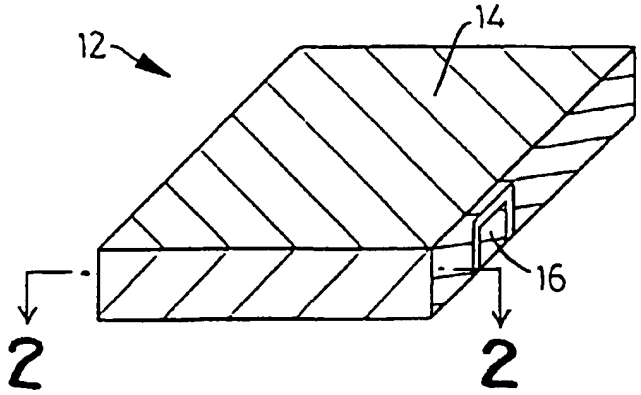
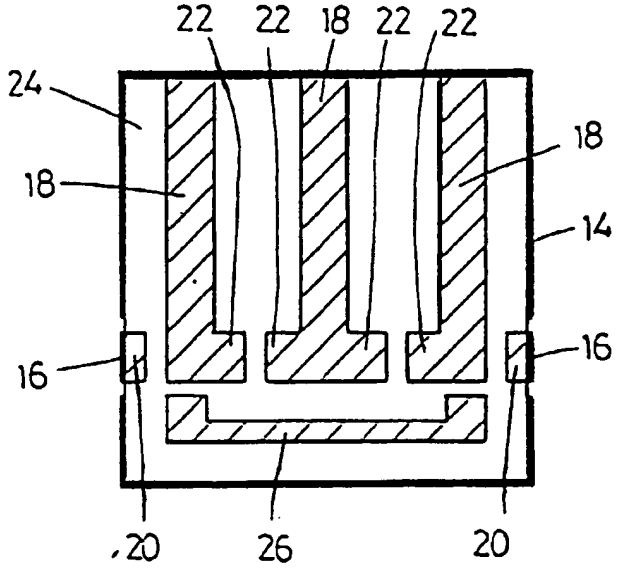


FIG. 2



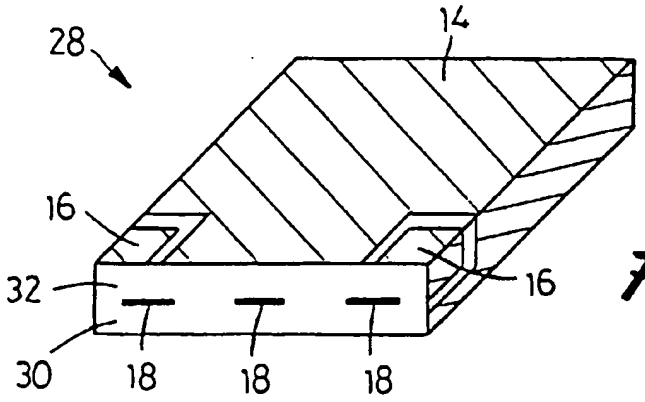


FIG. 3

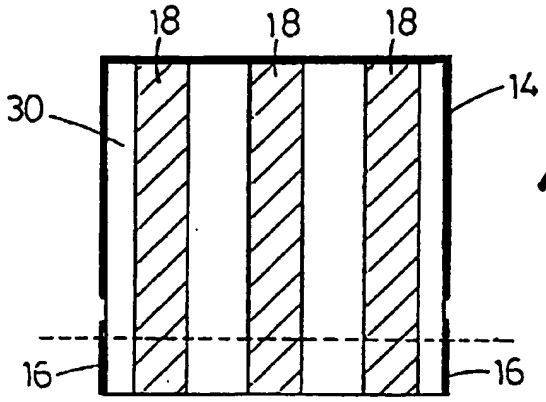


FIG. 4

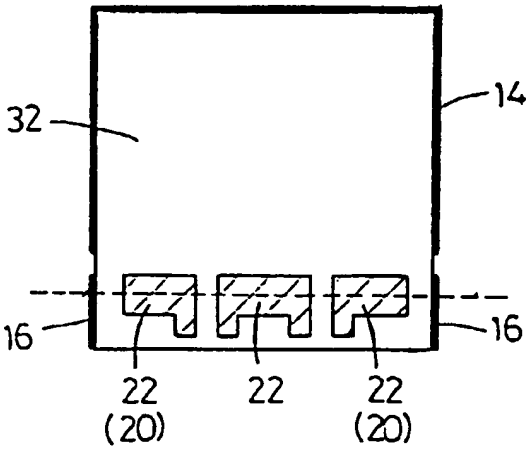


FIG. 5

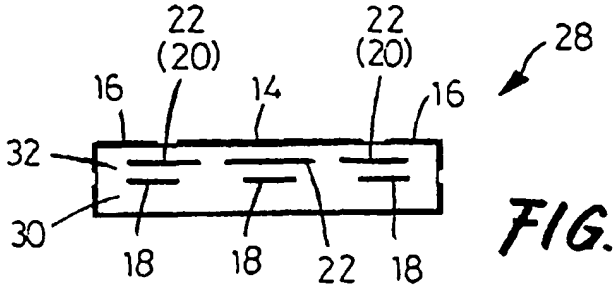


FIG. 6

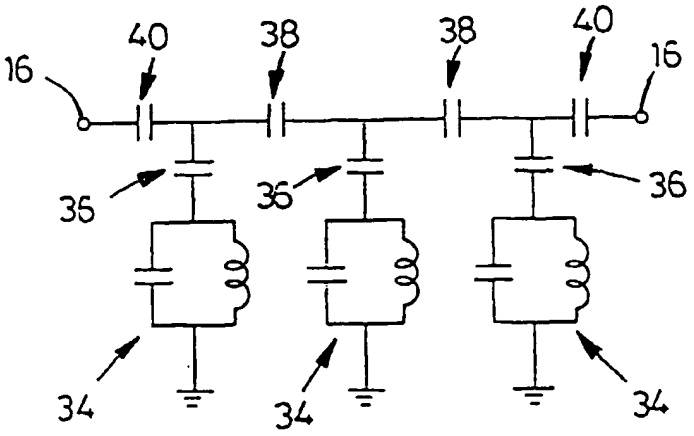


FIG. 7

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FIG. 8

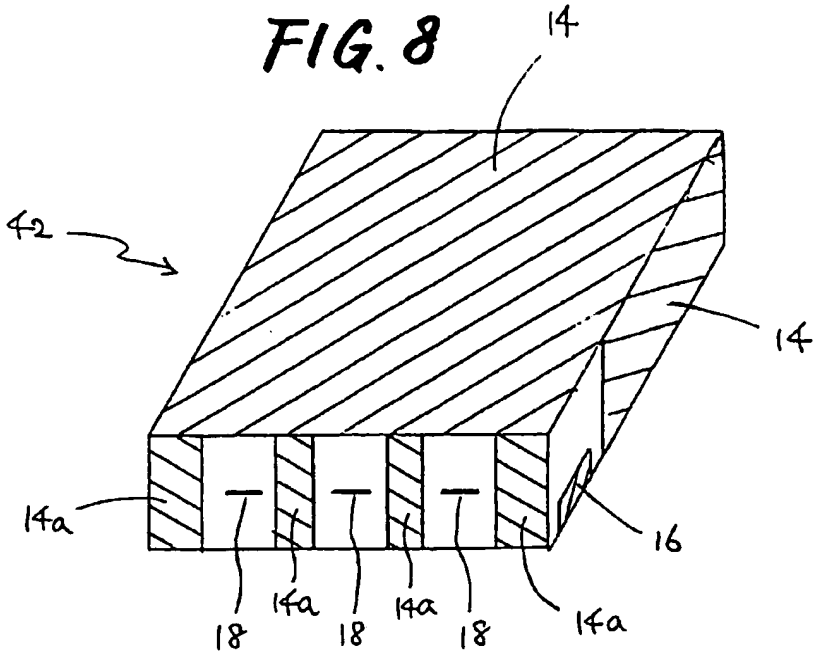

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FIG. 10

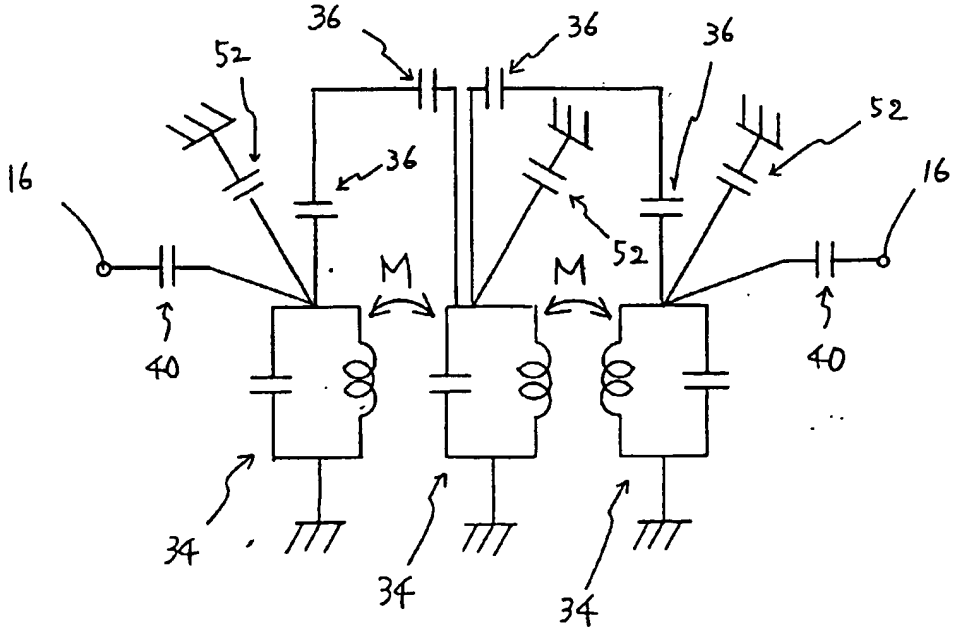

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FIG. 9

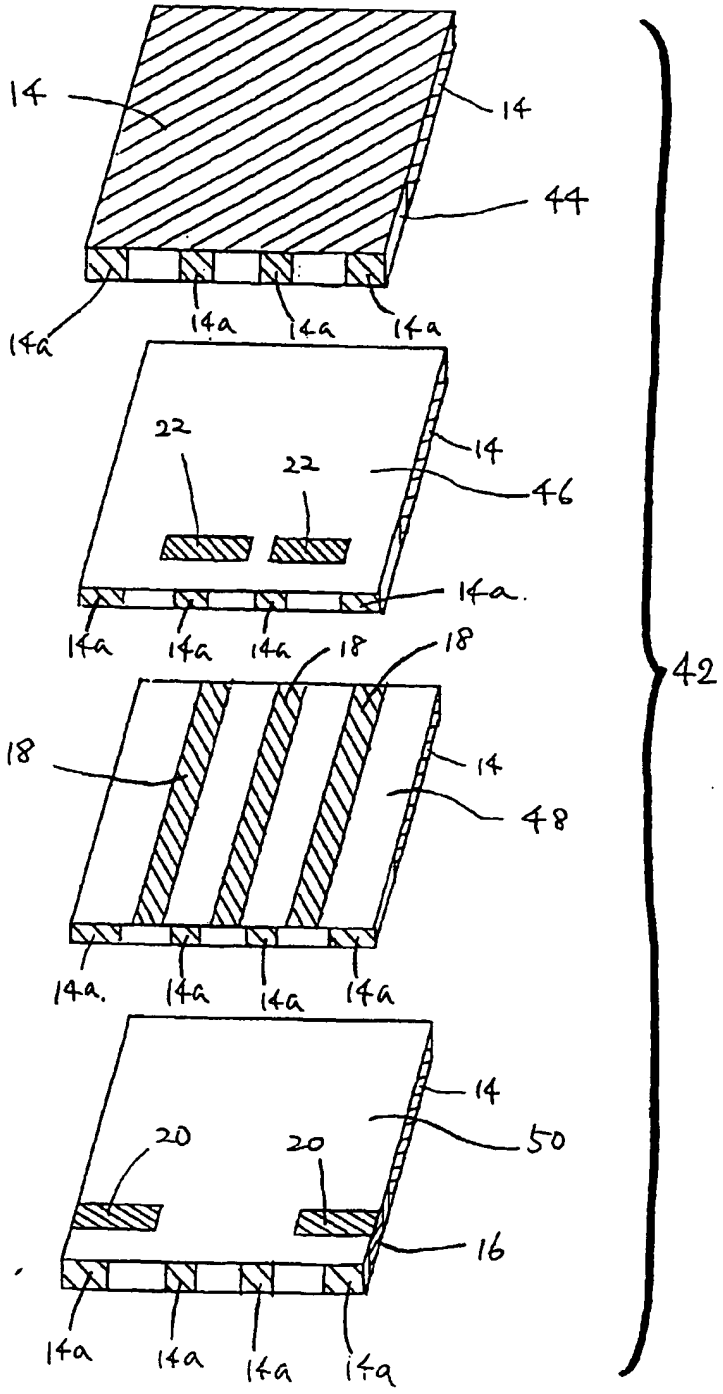
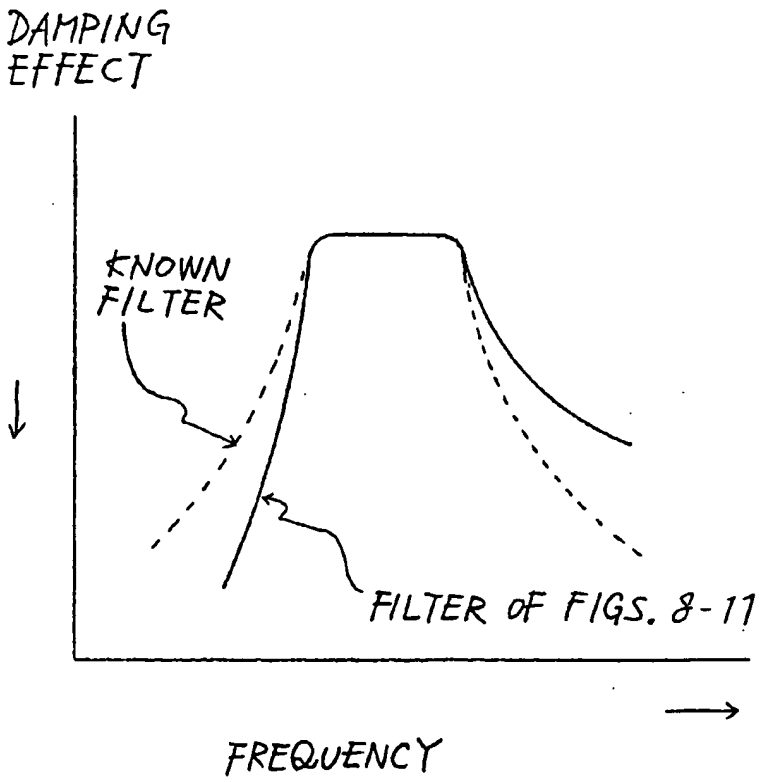
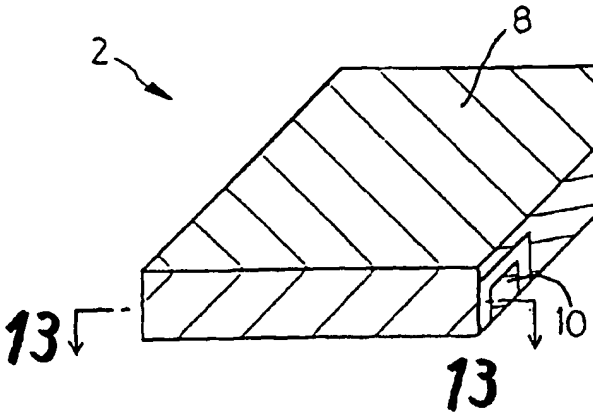

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FIG. 11





PRIOR ART
FIG. 12

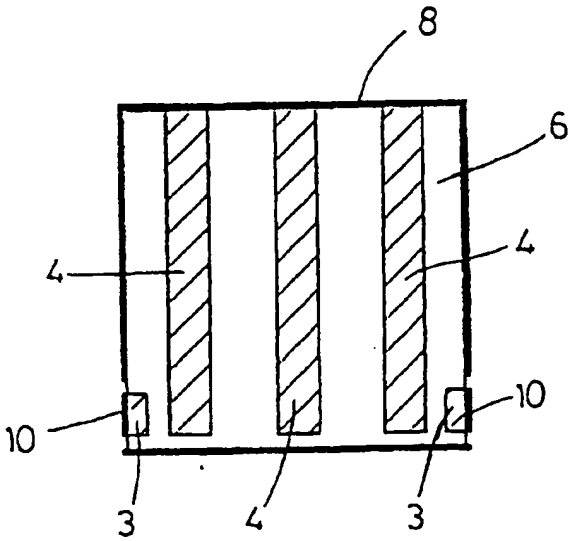


FIG. 13 PRIOR ART

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Filtre diélectrique

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- **PATENT ABSTRACTS OF JAPAN vol. 11, no. 110 (E-496)(2557) 7 April 1987 & JP-A-61 258 503 (MURATA MANUFACTORING CO LTD) 15 November 1986**
- **PATENT ABSTRACTS OF JAPAN vol. 7, no. 208 (E-198)(1353) 14 September 1983 & JP-A-58 103 202 (FUJITSU K.K.) 20 June 1983**

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a compact planar type dielectric filter to be mainly used in a high frequency radio equipment such as a portable telephone set and the like.

2. Description of the Prior Art

Recently, there is an increasingly growing demand for further down-sizing a planar type dielectric filter which can be made thinner in structure as compared with a coaxial type one being widely used for portable telephone sets.

Explanations will be made below on the operation of a conventional dielectric filter of a laminated planar type as an example. A conventional planar dielectric filter comprises two thick dielectric layers, a first dielectric sheet on which two coil electrodes are formed, a second dielectric sheet on which one-side electrodes of two parallel plane capacitors are formed, a third dielectric sheet on which the other side electrodes of the two parallel plane capacitors are formed, a fourth dielectric sheet on which a shield electrode is formed, and a dielectric sheet which serves to protect the electrodes, which are laminated from the bottom in the order of the fourth dielectric sheet, one of the two thick dielectric layers, the first dielectric sheet, the other of the two thick dielectric layers, the second dielectric sheet, the third dielectric sheet and the dielectric sheet for electrode protection. In the dielectric filter constructed as above, the parallel plane capacitors are formed respectively between the capacitor electrodes confronted to each other. The parallel plane capacitors thus formed are connected through respective side electrodes to the coil electrodes in series to serve to act as a resonance circuit. The two coils are magnetically coupled to each other, and the input/output terminals are taken intermediately of the coil electrodes, thus forming a band-pass filter. (See, for example, Japanese Laid-Open Patent Publication NO. 3-72706.)

With the conventional dielectric filter structured as above, if the coil electrodes are disposed close to each other to decrease the distance therebetween for down-sizing, such a problem has been arisen that a good band-pass characteristic of a narrow band is difficult to be realized due to the fact that the magnetic coupling between the resonance circuits becomes too large.

US-A-4 418 324 discloses an interdigital filter comprising two dielectric layers, one of which comprising a plurality of electromagnetically coupled conductive strips, and the other acting as a set of capacitors arranged to operate on alternate strips to give transmission zero at a certain frequency.

An object of this invention is to provide a compact planar type dielectric filter capable of providing superior narrow-band band-pass characteristic.

In order to attain the above-mentioned object, a dielectric filter of this invention comprises:

a first dielectric sheet (60c) having formed thereon a plurality of end short-circuited strip line resonators respectively composed of a plurality of strip lines (61a,61b) each of which has a length of about quarter-wavelength and which are formed in parallel; and

a second dielectric sheet (60d) having formed thereon a capacitor electrode (62a),

first and second dielectric sheets being laminated such that said capacitor electrode partially confronts at least one of said strip lines of said strip line resonators through said first or second dielectric sheet to constitute a parallel plane capacitor, wherein

said plurality of strip lines (61a,61b) are formed closely to each other so that each adjacent two of said strip line resonators are directly magnetically coupled to each other, and wherein said first and second dielectric sheets being laminated such that said capacitor electrode (62a) partially confronts all of the electrodes of said strip line resonators (61a, 61b) to constitute a plurality of parallel plane capacitors such that said strip line resonators are electrically coupled to each other through said parallel plane capacitors whereby an inter-resonator coupling is performed in combination with said magnetic coupling and electric coupling;

characterized by further comprising third and fourth dielectric sheets (60e,60f) each having formed thereon a shield electrode (63a,63b), said third and fourth dielectric sheet being disposed so as to sandwich therebetween said first and second dielectric sheets (60c,60d) to shield said strip line resonators and said parallel plane capacitor with said shield electrodes.

With the structure as explained above, an equivalent coupling inductance between the end short-circuited strip line resonators becomes relatively larger than that between the coil electrodes of lumped constant elements, so that the inter-resonator coupling can be reduced. In addition, the coupling inductance component can be easily cancelled by the capacitance component of the parallel plane capacitors inserted in parallel, so that the inter-resonator coupling can be further reduced. As a result, a compact planar type dielectric filter having superior narrow-band band-pass characteristic can be realized.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1(a) is an exploded perspective view of a dielectric filter.

Fig. 1(b) is a perspective view showing a first surface of a second dielectric substrate shown in Fig. 1(a).

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Fig. 1(c) is a perspective view showing a ground electrode on the back surface of the first dielectric substrate shown in Fig. 1(a).

Fig. 2(a) is an equivalent circuit diagram for explaining the operation of the dielectric filter shown in Fig. 1(a).

Fig. 2(b) is another equivalent circuit of the circuit shown in Fig. 2 (a) expressed by using lumped constant elements.

Fig. 2(c) is still another equivalent circuit obtained by further equivalently changing the circuit shown in Fig. 2(b).

Fig. 3 is a diagram showing a coupling characteristic of an end short-circuited parallel strip line resonator for explaining the operation of the dielectric filter shown in Fig. 1(a).

Fig. 4(a) is an exploded perspective view of a second dielectric filter.

Fig. 4(b) is a perspective view showing electrodes of strip line resonators formed on a first dielectric substrate shown in Fig. 4(a).

Fig. 4(c) is a perspective view showing a second surface of a second dielectric substrate shown in Fig. 4 (a).

Fig. 5 is a cross-sectioned view of the dielectric filter shown in Fig. 4(a).

Fig. 6 is an exploded perspective view of a lamination-type dielectric filter according to this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A dielectric filter operating in the same manner as that of the present invention will be described below while referring to the accompanying drawings.

Fig. 1 is an exploded perspective view of a dielectric filter having a two-pole structure according to the first embodiment. In Fig. 1(a), 10a is a first dielectric substrate, 11a and 11b are end short-circuited strip line resonators of substantially a quarter-wavelength and 11c is a ground electrode. In addition, 10b is a second dielectric substrate to be laminated onto the first dielectric substrate 10a. Fig. 1(b) shows a first surface of the second dielectric substrate 10b for contacting with the first dielectric substrate 10a. In this first surface, first electrodes 12a and 12b of parallel plane capacitors the number of which is the same as the number of the resonators are formed so as to partially overlap the open-circuited ends of respective electrode patterns of the strip line resonators 11a and 11b. Fig. 1(a) shows a second surface of the second dielectric substrate 10b. On this second surface is formed a second electrode 12c of the parallel plane capacitors so as to be partially confronted to all the first electrodes of the parallel plane capacitors and to constitute one area as the whole. In addition, third electrodes 12d and 12e of the parallel plane capacitors are partially formed on the second surface of the second dielectric substrate in such areas that are confronted to the first electrodes thereof and that the second electrode is not formed, and grounded through connecting electrode terminals 13a and 13b. In addition, fourth electrodes 12f and 12g of the parallel plane capacitors are partially formed on the second surface of the second dielectric substrate in such areas that are confronted to the first electrodes thereof and that the second and third electrodes are not formed, thus being electrically connected to an external circuit through the capacitors formed by the fourth electrodes and first electrodes. The strip line resonator electrodes and ground electrode on the first dielectric substrate, and capacitor electrodes on the second dielectric substrate are all formed by a thick film printing method. The first and second dielectric substrates 10a and 10b are bonded to each other by applying a solder by a soldering method in respective areas where the open-circuited ends of electrode patterns of the strip line resonators 11a and 11b are overlapped with the first electrodes 12a and 12b of the parallel plane capacitors. Fig. 1(c) shows the ground electrode on the back side of the first dielectric substrate 10a, in which 11d and 11e are controlling slits for controlling the coupling between the resonators.

With the dielectric filter structured as above, the operation will be explained below by referring to Figs. 2 and 3. Fig. 2(a) is an equivalent circuit diagram of a dielectric filter of the first embodiment, Fig. 2(b) is another equivalent circuit of the circuit shown in Fig. 2(a) expressed by using lumped constant elements, and Fig. 2 (c) is still another equivalent circuit by further equivalently changing the circuit shown in Fig. 2(b). In Fig. 2 (a), strip line resonators 20a and 20b correspond respectively to the strip line resonators 11a and 11b shown in Fig. 1, capacitors C11a and C11b correspond respectively to the capacitors formed by the third electrodes 12d and 12e and the first electrodes 12a and 12b shown in Fig. 1, capacitors C12a and C12b correspond respectively to the capacitors formed by the second electrode 12c and the first electrodes 12a and 12b shown in Fig. 1, and capacitors 13a and 13b correspond respectively to the capacitors formed by the fourth electrodes 12f and 12g and the first electrodes 12a and 12b shown in Fig. 1. In addition, M shows a magnetic coupling between the strip line resonators 20a and 20b.

In Fig. 2(b), inductances L21a and L21b respectively represent equivalent inductance components of the strip line resonators 20a and 20b, capacitances C21a and C21b represent capacitance components of the strip line resonators 20a and 20b, respectively, and a parallel connection of the capacitances C11a and C11b shown in Fig. 2(a). A capacitance C22 represents a series connection of the capacitances C12a and C12b.

In Fig. 2(c), a coupling inductance L32, inductances L31a and L31b respectively represent inductances obtained by circuit-changing equivalently the inductances L21a and L21b and the magnetic coupling M shown in Fig. 2(b). Here, when the coupling inductance L32 is large, an impedance to be inserted in series between the resonators becomes large, so that the inter-resona-

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tor coupling becomes small.

When the inductances L21a and L21b are supposed to be equal to each other and expressed as L21, the coupling inductance L32 can be expressed as follows;

$$L32 = (L21+M) * (L21/M-1).$$

From this equation, it can be made clear that when L21 is constant, L32 increases with a decrease in M, and when the ratio of L32 to M is constant, L32 increases with an increase in M. The former case corresponds to the case when the space between the strip lines of the resonators is expanded and the latter case corresponds to the case when the line lengths thereof are made large or when the dielectric constant of the first dielectric substrate 10a is made large.

Fig. 3 shows the degree of the inter-resonator coupling of the end short-circuited strip line resonators having a length of quarter-wavelength disposed in parallel. In case of coil resonators, the inter-resonator coupling increases with an increase in the length of the parallel portions. In case of strip line resonators, the inter-resonator coupling becomes zero when the length thereof becomes just a quarter-wavelength, and small in the vicinity of such a length as above. As a result, in case of using strip line resonators, a desired inter-resonator coupling can be realized by appropriately designing the length thereof.

In addition, the magnetic coupling M can be controlled by providing controlling slit 11d or 11e on the grounding electrode of the back surface of the strip line resonators. The controlling slit 11d parallel to the strip line resonators makes large the odd-mode impedance only without changing the even-mode impedance between the parallel strip lines, so that the difference between the two impedances becomes small, and the magnetic coupling M becomes small equivalently to the loose coupling of resonators. The controlling slit 11e perpendicular to the strip line resonators causes the electric current on the grounding electrode to be bypassed, resulting in the insertion of an inductance component between the resonators. As a result, the magnetic coupling M becomes large equivalently to the tight coupling of resonators.

In addition, with the filter constructed according to this embodiment, the capacitance C22 which is a serial combination of the capacitance C12a and C12b of the parallel plate capacitors inserted between the strip line resonators is connected to the coupling inductance L32 in parallel thereby to offset the inductance component. The capacitance C22 and the coupling inductance L32 constitutes a parallel resonance circuit, and the impedance becomes infinite with the resonance frequency, resulting in forming the attenuation pole in the transfer characteristic.

As explained above, according to this arrangement, a plurality of end short-circuited strip line resonators having a length of about quarter-wavelength are formed parallel and closely to each other on the first dielectric substrate, the resonators thus adjacently disposed to each other are directly magnetically coupled to each other, the electrodes of the parallel plane capacitors formed on the second dielectric substrate and the strip line electrodes are bonded by applying solder by a soldering method in an area where they overlap each other, so that the strip line resonators are electrically coupled to each other through the parallel plane capacitors, and the inter-resonator coupling can be made in combination of magnetic coupling and electric coupling, thus allowing the inter-resonator coupling to be reduced. As a result, such a small and planar type dielectric filter can be realized that has a small inter-resonator coupling and the attenuation pole as well as exhibits good narrow-band band-pass characteristic.

In addition, according to this arrangement all the capacitor electrodes necessary for making a filter can be formed on the second dielectric substrate, so that it can be made simple in structure, thus being capable of reducing the product variation of the dielectric filters that are produced.

In addition, in the explanations of this arrangement all the electrodes to be formed on the strip line resonators and capacitors were formed by the thick film printing technique, but not limited thereto, all of them may be formed thereon by means of a plating and etching method.

Further in addition, in this arrangement, the explanations were made on a dielectric filter having a two-pole structure, but not limited thereto, such a dielectric filter as to have a more than two-pole structure can be made in the same method, which is the same in the explanations of the following preferred embodiments.

A second dielectric filter similar to that of the present invention will be described below while referring to the drawings. Fig. 4 is an exploded perspective view of a dielectric filter according to this embodiment, and Fig. 5 is a cross-sectioned view of the dielectric filter of this embodiment taken along a line A - A' in Fig. 4(a).

In Fig. 4(a), 43 is a resin carrier, 40b is a second dielectric substrate, and 40a is a first dielectric substrate, which are laminated in this order. In addition, 41c is a ground electrode, and 41d and 41e are controlling slits for controlling the inter-resonator coupling. Fig. 4 (a) shows a first surface of the second dielectric substrate 40b. On this first surface, first electrodes 42a and 42b of parallel plane capacitors the number of which is the same as the number of the resonators, are formed so as to partially overlap the open-circuited ends of respective electrode patterns of strip line resonators. Fig. 4(b) shows the surface of the first dielectric substrate 40a on which the electrodes of the strip line resonators are formed, in which 41a and 41b are strip line resonators having a folded structure. Fig. 4(c) shows a second surface of the second dielectric substrate 40b. On this

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second surface, a second electrode 42c of the parallel plane capacitors is formed so as to be partially confronted to all the first electrodes of the parallel plane capacitors and to constitute one area as the whole. In addition, a third electrode 42d of the parallel plane capacitors is partially formed on the second surface thereof so as to be confronted to the first electrodes thereof in such an area that the second electrode is not formed. The third electrode 42d is such an electrode that the electrodes 12d and 12e shown in Fig. 1 are formed in one united body and grounded through a metal terminal 432a for ground electrode use. Also, fourth electrodes 42f and 42g of the parallel plane capacitors are partially formed on the second surface thereof to be confronted respectively to the first electrodes thereof in such an area that the second and third electrodes are not formed, and connected to an external circuit through capacitors to be respectively formed by the fourth electrodes 42f and 42g and the first electrodes 42a and 42b. In addition, the first and second dielectric substrates 40a and 40b are bonded to each other by applying a solder by a soldering method in such areas that the open-circuited ends of the electrode patterns of the strip line resonators 41a and 41b and the first electrodes 42a and 42b of the parallel plane capacitors are superposed, respectively.

The dielectric filter of this embodiment is different in structure from that of the first arrangement in (1) that the strip line resonators 41a and 41b having a folded structure are introduced as a resonator, (2) that the bonded substrate body is mounted onto the resin carrier 43, and (3) that the strip line resonators of a groove type are formed on the first dielectric substrate. The structure of the other component parts is substantially the same as that shown in Fig. 1.

With the dielectric filter structured as above, the operation will be explained while emphasizing the different points from that of the first arrangement.

The first different point is that the strip line resonators 41a and 41b each having a folded structure respectively have the line widths changed from wide width portions 411a and 411b to narrow width portions 412a to 412b of the strip line shorter than a quarter-wavelength, and connected to respective ground electrodes on the back surface thereof through band-shaped electrodes 413a and 413b each having the same width as that of the narrow width portion formed on the side of the first dielectric substrate 40a. The ground electrodes can be extended in the line length equivalently by providing notched slits 414a and 414b at respective connecting points, and the resonance frequency can be controlled by changing the lengths of the notched slits. The strip line resonator of the folded structure as shown above can be small-sized without degrading the value of Q-factor so much. A best combination of the value of Q-factor and the size of the resonator can be obtained when the line widths of the band-shaped electrodes 413a and 413b are equal to the widths of the narrow width portions 412a and 412b of the strip line resonators 41a and 41b. When the line widths of the band-shaped electrodes are smaller than the widths of the narrow width portions, the value of Q-factor will be sacrificed and when the former are larger than the latter, the size of the resonator will be sacrificed.

The second point is that the resin carrier 43 has an integral structure of a resin 433 with a metal terminal 431 for input/output electrode use and a metal terminal 432a for ground electrode use. This means that an improvement in terminal strength to be used as a surface mounted device (SMD) can be realized. In addition, for the purpose of shielding the filter, a shield plate 434 which is connected to the metal terminal 432b for ground electrode use is insertedly provided into the bottom surface of the resin carrier 43. The metal terminal 432b for ground electrode use is connected to the ground electrode 41c of the first dielectric substrate 40a to shield the upper portion of the filter. In order to reduce the filter loss to minimize the degradation of filter characteristic, it is effective to provide a concave groove 435 on the upper surface of the resin carrier 43 so as to form an air layer between the shield plate 434 and the bonded substrates body of the first and second dielectric substrates 40a and 40b.

The third point is that the strip line resonators 41a and 41b to be formed in a groove form on the first dielectric substrate 40a are made in such a manner that the grooves to form the resonators are pressure-molded and fired in the process of producing the first dielectric substrate, a thick film electrode material is applied on the entire surface of the substrate, and thereafter, the electrode material applied in the area where the grooves are not formed are removed by a polishing method thereby forming the electrodes of the strip line resonators. This method is superior in mass-production to the thick film printing method. In this method, the substrate may be entirely immersed into a solution of a thick film electrode material to adhere an electrode material onto the entire surface of the substrate and then fired, or an electrode material may be plated on the entire surface of the substrate by an electroless plating method, so that strong adhesion of the electrode material onto the ceramic substrate can be obtained. As a result, the adhesion of the electrodes and the substrate can be outstandingly improved especially in such an area that the strip line resonators at the edge of the substrate are connected to the respective band-shaped electrodes. Consequently, the electrode resistance to a high-frequency current can be reduced and the loss of resonators can be decreased. In addition, with the groove-type strip line resonator, the high-frequency current can be concentrated in the area where the bottom surface and side surface of the groove are to be in contact to each other. On the other hand, with a general planar type strip line resonator, the high frequency current will be concentrated in a rugged area peripherally of the strip line, thus a greater part of the loss of the resonator being generated at such area. On the other hand, with the groove-type

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strip line resonator, the electrode in the area where the bottom surface and the side surface thereof are contacted each other does not have such a ragged area that the side area has. Accordingly, the electrode resistance to high-frequency current in the contacting area becomes smaller than in the side area. As a result, the groove-type strip line resonator can be made small in resonator loss as compared with the plane-type strip line resonator.

As explained above, the dielectric filter according to this arrangement makes it possible to realize a compact size without degrading the filter characteristic by using a strip line resonator having a folded-type structure. In addition, by using a carrier made of a resin, the terminal electrode strength and shielding property of the filter can be outstandingly improved. Further in addition, by using a groove-type strip line resonator, the loss of the filter can be decreased and the productivity can be outstandingly improved.

Also, similar to the first arrangement, it is needless to say that the inter-resonator coupling can be controlled by providing a controlling slit 41d or 41e on the grounding electrode 41c on the back surface thereof. In addition, in combination with the frequency controlling method by using the notched slits 414a and 414b of the strip line resonators having a folded structure, the filter characteristic can be controlled only on the back surface of the resonator. This fact is very important for the dielectric filter of this embodiment in which the component parts other than the ground electrode on the back surface are substantially covered with the resin carrier.

A dielectric filter according to the present invention will be described below while referring to the drawings.

Fig. 6 is a perspective view of a dielectric filter of this embodiment, in which 60a and 60b are thick dielectric layers. A dielectric sheet 60c has strip line resonator electrodes 61a and 61b formed thereon, and a dielectric sheet 60d has a second electrode 62a, a third electrode 62b and fourth electrodes 62c and 62d of parallel plane capacitors formed thereon. The strip line resonator electrodes 61a and 61b have the strip lines whose short-circuited ends are narrowed in width of the strip line, that is, narrowed from a wide width portion to a narrow width portion, resulting in realizing down-sizing. In addition, a shield electrode 63a is formed on a dielectric sheet 60e, and a shield electrode 63d is formed on a dielectric sheet 60f. These dielectric sheets, dielectric layers and an electrode protective dielectric sheet 60g are laminated to obtain a lamination body.

With the dielectric filter structured as explained above, the operation will be explained below.

First, the strip line resonator electrodes 61a and 61b and the second electrode 62a, third electrode 62b and fourth electrodes 62c and 62d which are confronted to the electrodes 61a and 61b respectively form parallel plane capacitors therebetween. The second electrode 62a of the parallel plane capacitors serves to act as an interresonator coupling capacitor. The third electrode 62b serves to act as a parallel capacitor for lowering the resonance frequency of the strip line resonators. The fourth electrodes 62c and 62d serve to act as input/output coupling capacitors. The fourth electrodes 62c and 62d are connected respectively to the side electrodes 64a and 64b to be used as input/output terminals. The lower shield electrode 63a and the upper shield electrode 63b are connected to side electrodes 65a, 65b, and 65c respectively to be used as ground terminals.

The dielectric filter of this embodiment is different from that of the first arrangement in that lamination is made so that the first electrodes of the parallel plane capacitor are used in common with the electrodes of the strip line resonators. The lamination structure according to the present invention makes it possible to be simple in structure and small in size as well as to realize a shield. In addition, according to the present invention, all the electrodes of the strip line resonators are formed on the dielectric sheet 60c and all the capacitor electrodes are formed on the dielectric sheet 60d by a printing method, so that the electrode printing may be applied only for two dielectric sheets and two shield electrodes. This means that the number of printing processes can be made small and yet, the variation of filter characteristic can be reduced.

Claims

1. A dielectric filter comprising:

a first dielectric sheet (60c) having formed thereon a plurality of end short-circuited strip line resonators respectively composed of a plurality of strip lines (61a,61b) each of which has a length of about quarter-wavelength and which are formed in parallel; and
a second dielectric sheet (60d) having formed thereon a capacitor electrode (62a),
first and second dielectric sheets being laminated such that said capacitor electrode partially confronts at least one of said strip lines of said strip line resonators through said first or second dielectric sheet to constitute a parallel plane capacitor, wherein
said plurality of strip lines (61a,61b) are formed closely to each other so that each adjacent two of said strip line resonators are directly magnetically coupled to each other, and wherein said first and second dielectric sheets being laminated such that said capacitor electrode (62a) partially confronts all of the electrodes of said strip line resonators (61a,61b) to constitute a plurality of parallel plane capacitors such that said strip line resonators are electrically coupled to each other through said parallel plane capacitors whereby an inter-resonator coupling is performed in combination with said magnetic cou-

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pling and electric coupling;

characterized by further comprising third and fourth dielectric sheets (60e,60f) each having formed thereon a shield electrode (63a,63b), said third and fourth dielectric sheet being disposed so as to sandwich therebetween said first and second dielectric sheets (60c,60d) to shield said strip line resonators and said parallel plane capacitor with said shield electrodes.

2. A dielectric filter according to claim 1, further comprising a second capacitor electrode (62b) formed on said second dielectric sheet so as to partially confront said strip lines of said strip line resonators to thereby constitute second parallel plane capacitors, said second capacitor electrode being adapted to be connected to a ground.

3. A dielectric filter according to any preceding claim, further comprising a third capacitor electrode (62c) formed on said second dielectric sheet so as to partially confront one of said strip lines of said strip line resonators to thereby constitute a third parallel plane capacitor, and a fourth capacitor electrode (62d) formed on said second dielectric sheet so as to partially confront another of said strip lines of said strip line resonators to thereby constitute a fourth parallel plane capacitor, said third and fourth capacitor electrodes being adapted to be connected to input and output lines, respectively.

4. A dielectric filter according to any preceding claim, further comprising an additional dielectric sheet (60g) provided on an outermost one of the shield electrodes to protect the outermost shield electrode.

5. A dielectric filter according to any preceding claim, wherein said first through fourth dielectric sheets are laminated in the order of said third, first, second and fourth dielectric sheets with a first thick dielectric plate (60a) disposed between said third and first dielectric sheets and with a second thick dielectric plate (60b) disposed between said second and fourth dielectric sheets so that each of a distance between said shield electrode on said third dielectric sheet and said strip lines of said strip line resonators and a distance between said shield electrode on said fourth dielectric sheet and said capacitor electrode is larger than a distance between said strip lines of said strip line resonators and said capacitor electrode.

6. A dielectric filter according to any preceding claim, further comprising at least two ground electrodes (65a, 65b,65c) respectively formed on different side surfaces of each of said first through fourth dielectric sheets and connected to said shield electrode.

7. A dielectric filter according to any preceding claim, further comprising at least two ground electrodes (65a, 65b,65c) respectively formed on opposite side surfaces of each of said first through fourth dielectric sheets and connected to said shield electrode, a pattern of said ground electrodes on one of said opposite side surfaces being different from a pattern of said ground electrodes on the other of said opposite side surfaces.

8. A dielectric filter according to any preceding claim, wherein short-circuited ends of all of said strip line resonators extends to a same side surface of said first dielectric sheet and connected to a ground electrode (65a, 65b) formed on said side surface.

9. A dielectric filter according to claim 8, wherein another ground electrode (65c) is formed on a side surface of said first dielectric sheet closer to open-circuited ends of said strip line resonators.

10. A dielectric filter according to any preceding claim, further comprising an input terminal electrode (64a) and an output terminal electrode (64b) which are formed on one side surface of said first dielectric sheet, and a ground electrode (65c) formed between said input and output terminal electrodes on said side surface.

11. A dielectric filter according to any preceding claim, wherein said shield electrode on each of said third and fourth dielectric sheets is formed to leave a margin along the periphery of the corresponding dielectric sheet.

12. A dielectric filter according to any preceding claim, wherein said shield electrodes formed on said third and fourth dielectric sheets are the same in shape.

13. A dielectric filter according to any preceding claim, wherein a line width of a short-circuited end of a strip line of each of said strip line resonators is narrower than a line width of an open-circuited end of said strip line.

Patentansprüche

1. Ein dielektrisches Filter, umfassend:

eine erste, dielektrische Lamelle (60c), auf der eine Mehrzahl von am Ende kurzgeschlossenen Streifenleitungsresonatoren jeweils aus einer Mehrzahl von Streifenleitungen (61a, 61b) gebildet ist, von denen jede eine Länge von ungefähr einer Viertelwellenlänge hat und die par-

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allel gebildet sind; und

eine zweite, dielektrische Lamelle (60d), auf der eine Kondensatorelektrode (62a) gebildet ist,

die erste und die zweite, dielektrische Lamelle sind so geschichtet, daß die genannte Kondensatorelektrode teilweise wenigstens einer der genannten Streifenleitungen der genannten Streifenleitungsresonatoren durch die genannte erste oder zweite, dielektrische Lamelle hindurch gegenüberstehen, um einen parallelen, ebenen Kondensator zu bilden, worin

die genannte Mehrzahl von Streifenleitungen (61a, 61b) nahe beieinander gebildet ist, so daß jeweils zwei benachbarte der genannten Streifenleitungsresonatoren unmittelbar magnetisch miteinander gekoppelt sind, und worin die genannte erste und zweite, dielektrische Lamelle so geschichtet sind, daß die genannte Kondensatorelektrode (62a) teilweise allen Elektroden der genannten Streifenleitungsresonatoren (61a, 61b) gegenübersteht, um eine Mehrzahl von parallelen, ebenen Kondensatoren zu bilden, so daß die genannten Streifenleitungsresonatoren elektrisch miteinander durch die genannten parallelen, ebenen Kondensatoren gekoppelt sind, wodurch eine Zwischenresonatorkopplung in Kombination mit der genannten magnetischen Kopplung und der elektrischen Kopplung ausgeführt wird;

dadurch gekennzeichnet, daß es des weiteren eine dritte und eine vierte, dielektrische Lamelle (60e, 60f) umfaßt, auf denen jeweils eine Abschirmelektrode (63a, 63b) gebildet ist, wobei die genannte dritte und vierte, dielektrische Lamelle so angeordnet sind, daß dazwischen die genannte erste und die genannte zweite, dielektrische Lamelle (60c, 60d) eingefügt sind, um die genannten Streifenleitungsresonatoren und den genannten parallelen, ebenen Kondensator mit den genannten Abschirmelektroden abzuschirmen.

2. Ein dielektrisches Filter gemäß Anspruch 1, das des weiteren eine zweite Kondensatorelektrode (62b) umfaßt, die auf der genannten zweiten, dielektrischen Lamelle so gebildet ist, daß sie teilweise den genannten Streifenleitungen der genannten Streifenleitungsresonatoren gegenübersteht, und dadurch zweite, parallele, ebene Kondensatoren zu bilden, wobei die genannte zweite Kondensatorelektrode geeignet ist, mit Masse verbunden zu werden.

3. Ein dielektrisches Filter, gemäß irgendeinem vorhergehenden Anspruch, das des weiteren eine dritte Kondensatorelektrode (62c) umfaßt, die auf der genannten zweiten, dielektrischen Lamelle so gebildet ist, daß sie teilweise einer der genannten Streifenleitungen der genannten Streifenleitungsresonatoren gegenüber steht, um dadurch einen dritten, parallelen, ebenen Kondensator zu bilden, und eine vierte Kondensatorelektrode (62d), die auf der genannten zweiten, dielektrischen Lamelle so gebildet ist, daß sie teilweise einer anderen der genannten Streifenleitungen der genannten Streifenleitungsresonatoren gegenüber steht, um dadurch einen vierten, parallelen, ebenen Kondensator zu bilden, wobei die Elektroden des genannten dritten und vierten Kondensators mit einer Eingangs- bzw. Ausgangsleitung verbunden werden können.

4. Ein dielektrisches Filter, gemäß irgendeinem vorhergehenden Anspruch, das des weiteren eine zusätzliche, dielektrische Lamelle (60g) umfaßt, die auf einer äußersten der Abschirmelektroden vorgesehen ist, um die äußerste Abschirmelektrode zu schützen.

5. Ein dielektrisches Filter, gemäß irgendeinem vorhergehenden Anspruch, worin die genannte erste bis vierte, dielektrische Lamelle in der Reihenfolge der genannten dritten, ersten, zweiten und vierten, dielektrischen Lamelle aufeinander geschichtet sind, wobei einer erste, dicke, dielektrische Platte (60a) zwischen der genannten dritten und ersten, dielektrischen Lamelle angeordnet ist, und wobei eine zweite, dicke, dielektrische Platte (60b) zwischen der genannten zweiten und vierten, dielektrischen Lamelle so angeordnet ist, daß jeweils der Abstand zwischen der genannten Abschirmelektrode auf der genannten dritten, dielektrischen Lamelle und den genannten Streifen leitungen der genannten Streifenleitungsresonatoren und der Abstand zwischen der genannten Abschirmelektrode auf der genannten vierten, dielektrischen Lamelle und der genannten Kondensatorelektrode größer als ein Abstand zwischen den genannten Streifenleitungen der genannten Streifenleitungsresonatoren und der genannten Kondensatorelektrode ist.

6. Ein dielektrisches Filter, gemäß irgendeinem vorhergehenden Anspruch, das des weiteren wenigstens zwei Masselektroden (65a, 65b, 65c) umfaßt, die jeweils auf unterschiedlichen Seitenoberfläche von jeder der genannten ersten bis vierten, dielektrischen Lamelle gebildet sind und mit der genannten Abschirmelektrode verbunden sind.

7. Ein dielektrisches Filter, gemäß irgendeinem vorhergehenden Anspruch, das des weiteren wenigstens zwei Masseelektroden (65a, 65b, 65c) umfaßt, die jeweils auf gegenüberliegenden Seiten-

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oberflächen von jeder der genannten ersten bis vierten, dielektrischen Lamelle gebildet und mit der genannten Abschirmelektrode verbunden sind, wobei ein Muster der genannten Masselektroden auf einer der genannten gegenüberstehenden Seitenoberflächen von einem Muster der genannten Masseelektroden auf der anderen der genannten gegenüberstehenden Seitenoberflächen verschieden ist.

8. Ein dielektrisches Filter, gemäß irgendeinem vorhergehenden Anspruch, worin sich die kurzgeschlossenen Enden von allen der genannten Streifenleitungsresonatoren zu derselben Seitenoberfläche der genannten ersten, dielektrischen Lamelle erstrecken und mit einer Masseelektrode (65a, 65b) verbunden sind, die auf der genannten Seitenoberfläche gebildet ist.

9. Ein dielektrisches Filter, gemäß Anspruch 8, worin eine weitere Masseelektrode (65c) auf einer Seitenoberfläche der genannten ersten dielektrischen Lamelle näher zu den offenen Enden der genannten Streifenleitungsresonatoren gebildet sind.

10. Ein dielektrisches Filter, gemäß irgendeinem vorhergehenden Anspruch, das des weiteren eine Eingangsanschlußelektrode (64a) und eine Ausgangsanschlußelektrode (64b) umfaßt, die auf einer Seitenoberfläche der genannten ersten dielektrischen Lamelle gebildet sind, und eine Masseelektrode (65c), die zwischen der genannten Eingangs- und Ausgangsanschlußelektrode auf der genannten Seitenoberfläche gebildet ist.

11. Ein dielektrisches Filter, gemäß irgendeinem vorhergehenden Anspruch, worin die genannte Abschirmelektrode auf jeder der genannten dritten und vierten, dielektrischen Lamellen gebildet ist, einen Rand entlang dem Umfang der entsprechenden dielektrischen Lamelle zu lassen.

12. Ein dielektrisches Filter gemäß irgendeinem vorhergehenden Anspruch, worin die genannten Abschirmelektroden, die auf der genannten dritten und vierten dielektrischen Lamelle gebildet sind, die gleiche Form haben.

13. Ein dielektrisches Filter, gemäß irgendeinem vorhergehenden Anspruch, worin die Leitungsweite am kurzgeschlossenen Ende einer Streifenleitung von jedem der genannten Streifenleitungsresonatoren schmaler als die Leitungsweite an einem offenen Ende der genannten Streifenleitung ist.

Revendications

1. Filtre de diélectrique comprenant :

   - une première feuille de diélectrique (60c) possédant une pluralité de résonateurs en ligne en bandes à extrémités en court-circuit respectivement composés d'une pluralité de lignes en bandes (61a, 61b) possédant chacune une longueur d'environ un quart de longueur d'onde et formées en parallèle; et
   - une seconde feuille de diélectrique (60d) possédant une électrode de condensateur (62a) formée dessus;

   les première et seconde feuilles de diélectrique étant déposées en couches de telle façon que ladite électrode de condensateur soit partiellement en face d'au moins une desdites lignes en bande desdits résonateurs en ligne en bandes, via ladite première ou seconde feuille de diélectrique, pour constituer un condensateur plan en parallèle;
   filtre dans lequel ladite pluralité de lignes en bandes (61a, 61b) sont formées proches l'une de l'autre de telle façon que chaque paire adjacente desdits résonateurs en ligne en bandes soient directement couplées, de façon magnétique, l'une à l'autre et dans lequel lesdites première et seconde feuilles de diélectrique sont déposées en couches de telle façon que ladite électrode de condensateur (62a) sont partiellement en face de toutes les électrodes desdits résonateurs en ligne en bandes (61a, 61b) pour constituer une pluralité de condensateurs plans en parallèle de telle façon que lesdits résonateurs en ligne en bandes soient couplés, de façon électrique, l'un à l'autre via lesdits condensateurs plans en parallèles, un couplage entre résonateur étant effectué en combinaison avec ledit couplage magnétique et ledit couplage électrique;
   filtre caractérisé en ce qu'il comprend, de plus, des troisième et quatrième feuilles de diélectrique (60e, 60f) possédant chacune une électrode de blindage (63a, 63b), lesdites troisième et quatrième feuilles de diélectrique étant disposées de façon à prendre en sandwich lesdites première et seconde feuilles de diélectrique (60c, 60d) afin d'isoler lesdits résonateurs en ligne en bandes et ledit condensateur plan en parallèle desdites électrodes de blindage.

2. Filtre de diélectrique selon la revendication 1, comprenant, de plus, une seconde électrode de condensateur (62b) formée sur ladite seconde feuille de diélectrique de façon à faire face, de façon partielle, auxdites lignes en bandes desdits résona-

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teurs en ligne en bandes pour constituer ainsi des seconds condensateurs plans en parallèle, ladite seconde électrode de condensateur étant prévue pour être raccordée à une masse.

3. Filtre de diélectrique selon l'une quelconque des revendications précédentes, comprenant, de plus, une troisième électrode de condensateur (62c) formée sur ladite seconde feuille de diélectrique de façon à être partiellement en face d'une desdites lignes en bandes desdits résonateurs en ligne en bande pour constituer ainsi un troisième condensateur plan en parallèle, et une quatrième électrode de condensateur (62d) formée sur ladite seconde feuille de diélectrique de façon à être partiellement en face d'une autre desdites lignes en bande desdits résonateurs en ligne en bande pour constituer ainsi un quatrième condensateur plan en parallèle, lesdites troisième et quatrième électrodes de condensateur étant prévues pour être raccordées à des lignes respectives d'entrée et de sortie.

4. Filtre de diélectrique selon l'une quelconque des revendications précédentes, comprenant, de plus, une feuille additionnelle de diélectrique (60g) prévue sur une électrode la plus externe des électrodes de blindage pour protéger l'électrode de blindage la plus externe.

5. Filtre de diélectrique selon l'une quelconque des revendications précédentes, dans lequel lesdites première à quatrième feuilles de diélectrique sont déposées dans l'ordre selon lesdites troisième, première, seconde et quatrième feuilles de diélectrique avec interposition d'une première plaque épaisse de diélectrique (60a) entre lesdites troisième et première feuilles de diélectrique et avec interposition d'une seconde plaque épaisse de diélectrique (60b) entre lesdites seconde et quatrième feuilles de diélectrique de telle façon que chaque distance entre ladite électrode blindage sur ladite troisième couche de diélectrique et lesdites lignes en bande desdits résonateurs en ligne en bande et une distance entre ladite électrode de blindage sur ladite quatrième feuille de diélectrique et ladite électrode de condensateur soit plus grande qu'une distance séparant lesdites lignes en bandes desdits résonateurs en lignes en bandes et ladite électrode de condensateur.

6. Filtre de diélectrique selon l'une quelconque des revendications précédentes, comprenant, de plus, au moins deux électrodes de masse (65a, 65b, 65c) respectivement formées sur des surfaces latérales différentes de chacune desdites première à quatrième feuilles de diélectrique et raccordées à ladite électrode de blindage.

7. Filtre de diélectrique selon l'une quelconque des revendications précédentes comprenant, de plus, au moins deux électrodes de masse (65a, 65b, 65c) respectivement formées sur des surfaces latérales opposées de chacune desdites première à quatrième feuille de diélectrique et raccordées à ladite électrode de blindage, une configuration desdites électrodes de masse sur une desdites surfaces latérales opposées étant différente de celle desdites électrodes de masse sur l'autre desdites surfaces latérales opposées.

8. Filtre de diélectrique selon l'une quelconque des revendications précédentes, dans lequel les extrémités en court-circuit de tous lesdits résonateurs en ligne en bande s'étendent sur une même surface latérale de ladite première feuille de diélectrique et sont raccordées à une électrode de masse (65a, 65b) formée sur ladite surface latérale.

9. Filtre de diélectrique selon la revendication 8, dans lequel une autre électrode de masse (65c) est formée sur une surface latérale de ladite première couche de diélectrique plus proche des extrémités en court-circuit desdits résonateurs en ligne en bandes.

10. Filtre de diélectrique selon l'une quelconque des revendications précédentes, comprenant, de plus, une électrode de borne d'entrée (64a) et une électrode de borne de sortie (64b) qui sont formées sur une surface latérale de ladite première feuille de diélectrique, et une électrode de masse (65c) formée entre lesdites électrodes de borne d'entrée et de sortie sur ladite surface latérale.

11. Filtre de diélectrique selon l'une quelconque des revendications précédentes, dans lequel ladite électrode de blindage sur chacune desdites troisième et quatrième feuilles de diélectrique est formée pour laisser une marge le long de la périphérie de la feuille de diélectrique correspondante.

12. Filtre de diélectrique selon l'une quelconque des revendications précédentes, dans lequel lesdites électrodes de blindage formées sur lesdites troisième et quatrième feuilles de diélectrique ont la même forme.

13. Filtre de diélectrique selon l'une quelconque des revendications précédentes, dans lequel une largeur de ligne d'une extrémité en court-circuit d'une ligne en bandes de chacun desdits résonateurs en ligne en bandes est plus étroite qu'une largeur de ligne d'une extrémité en circuit ouvert de ladite ligne en bande.

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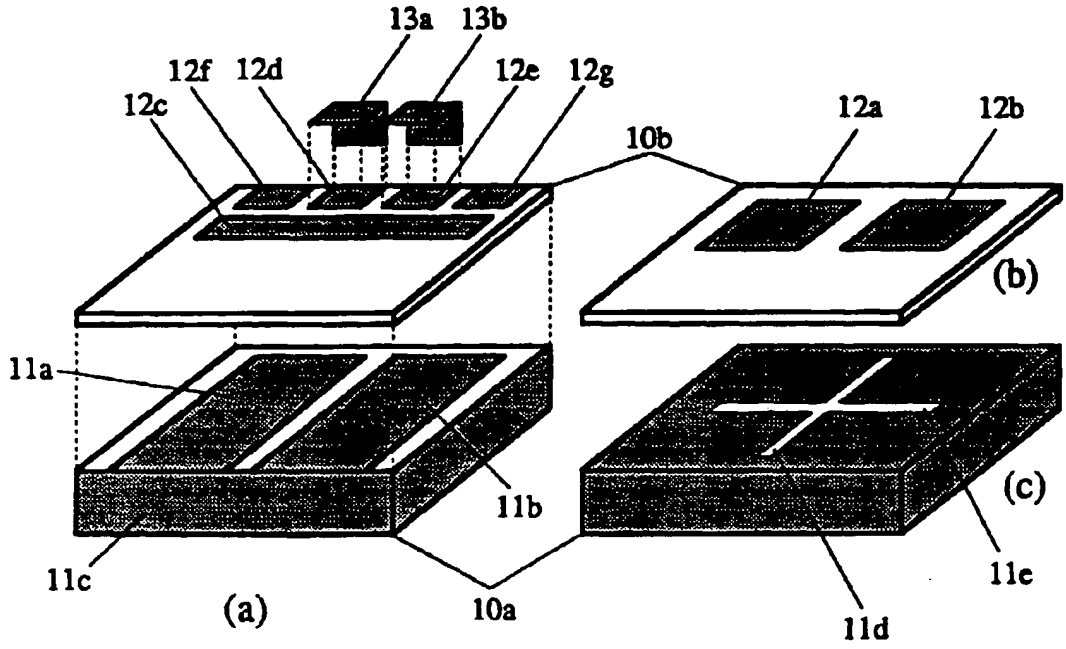

13a
13b
12f
12d
12e
12g
12c
12a
12b
10b
(b)
11a
11b
(c)
11c
11e
(a)
10a
11d

Fig.1

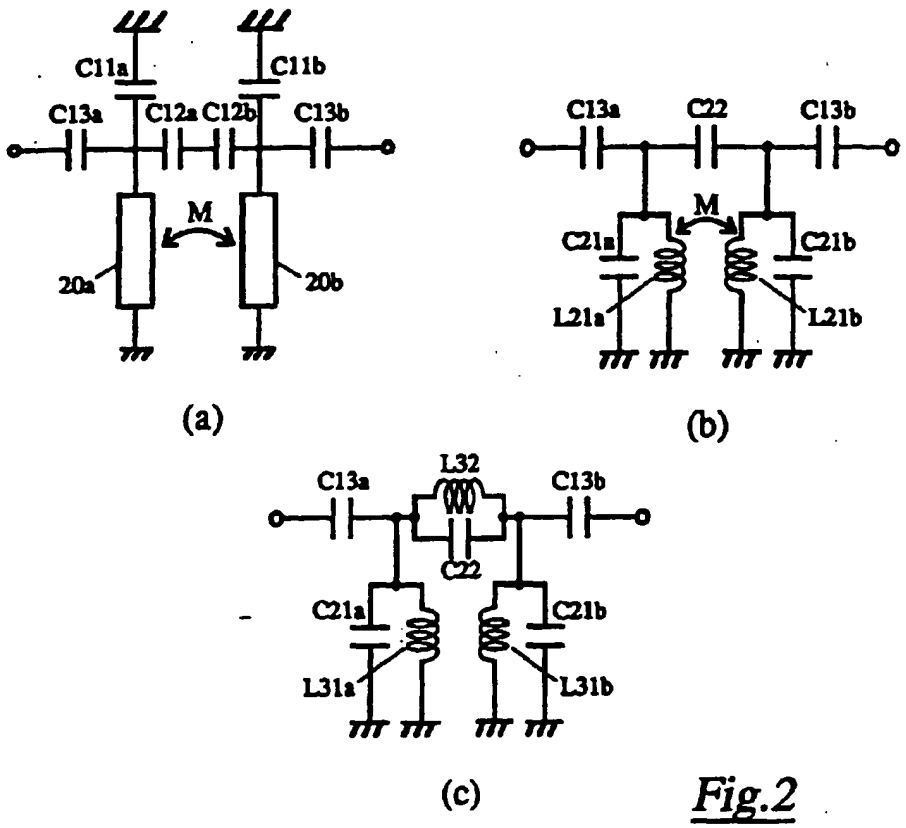


Fig.2

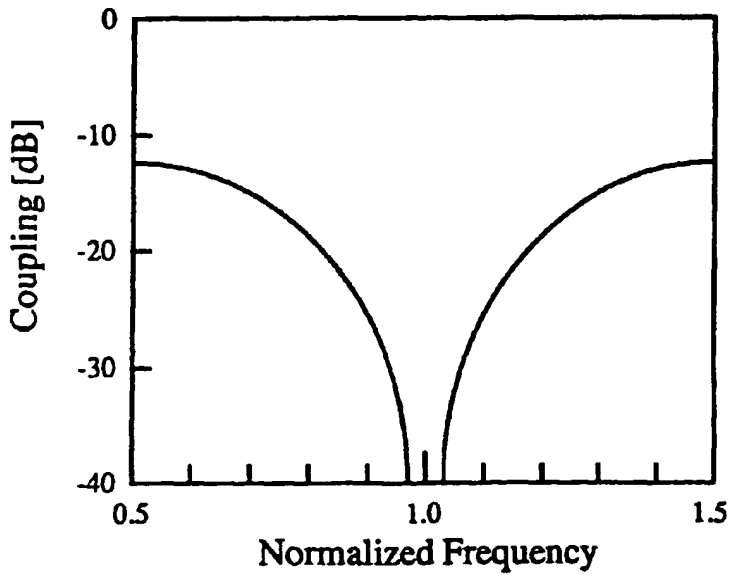


Fig.3

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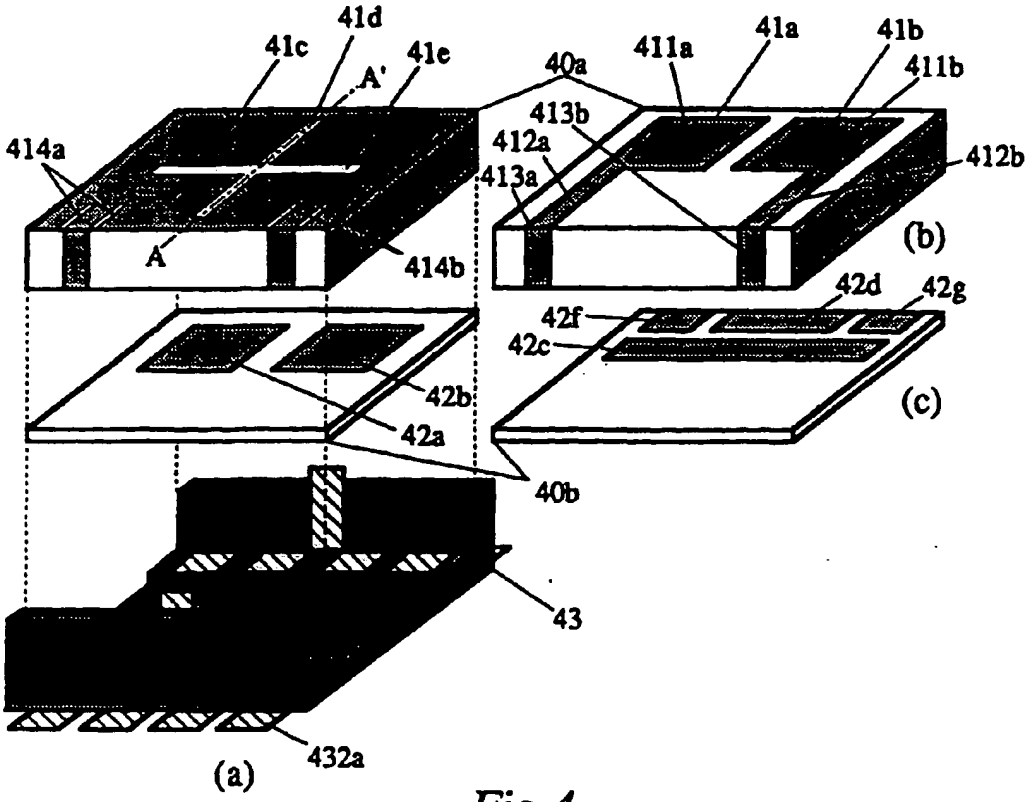

41d
41c
41e
A'
40a
411a
41a
41b
411b
414a
413b
412a
413a
412b
A
414b
(b)
42d
42g
42f
42c
42b
42a
(c)
40b
43
(a)
432a

Fig.4

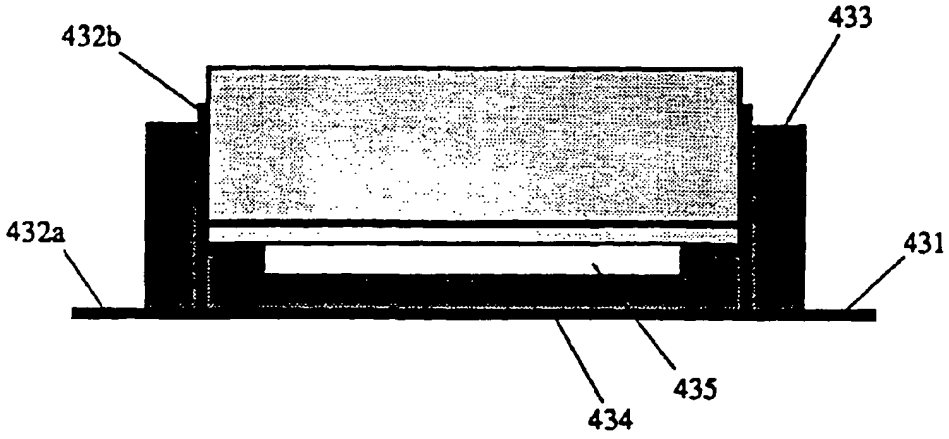

432b
433
432a
431
435
434

Fig.5

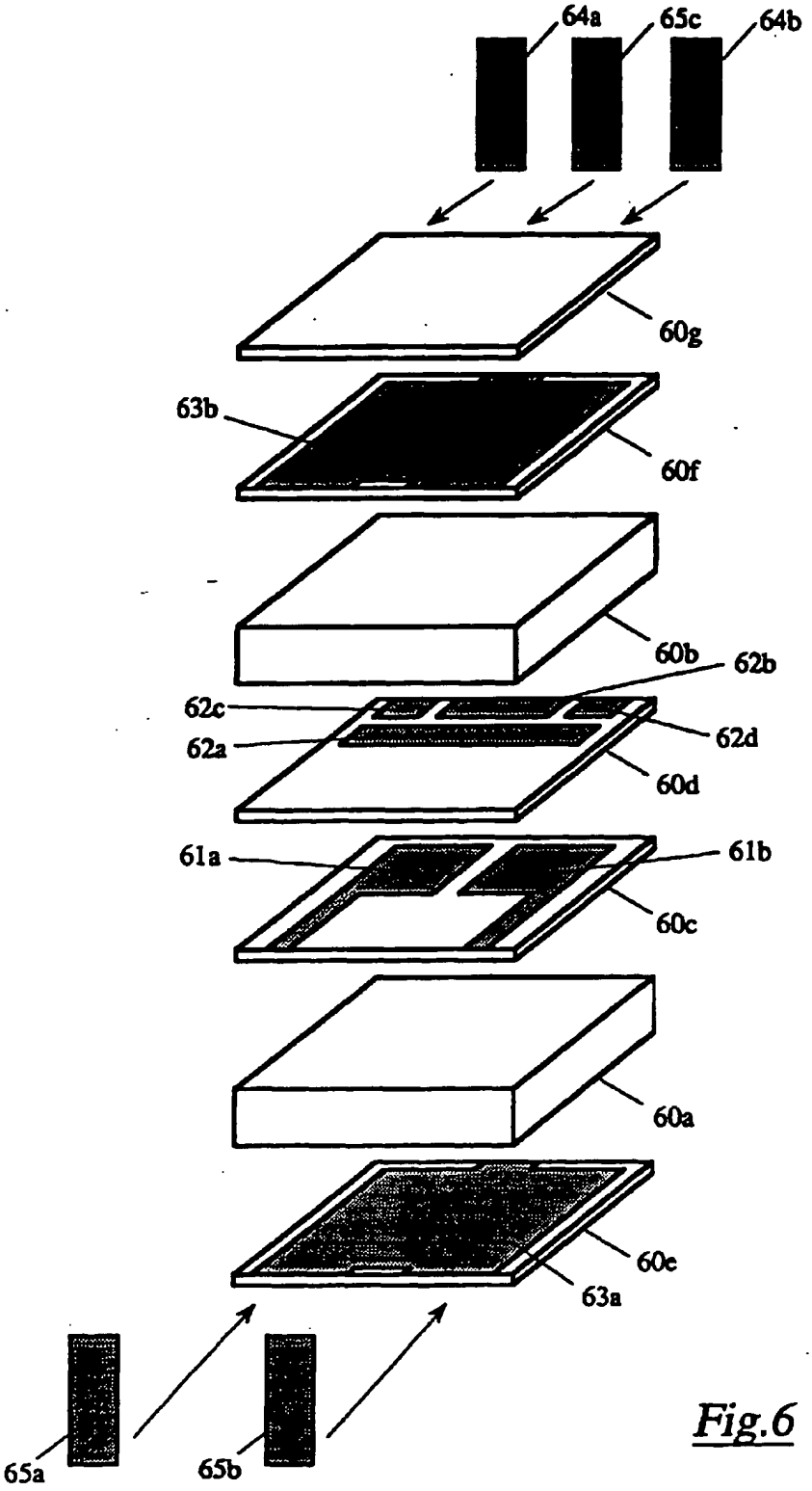

64a
65c
64b
60g
63b
60f
60b
62b
62c
62a
62d
60d
61a
61b
60c
60a
60e
63a
65a
65b

Fig.6

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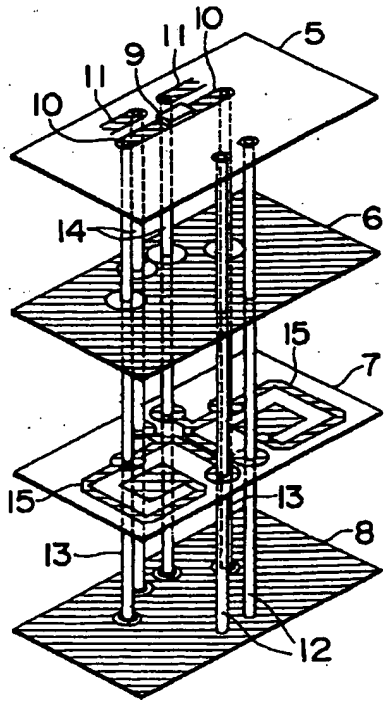
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(54)【発明の名称】　多層基板内層型トラップ付きバンドパスフィルタ

(57)【要約】
【課題】　標準的な有機系多層基板と市販のコンデンサチップを使用して、安価で小型の８００ＭＨｚ～２ＧＨｚ帯のトラップ付きバンドパスフィルタを提供する。
【解決手段】　導体層５～８と有機系誘電体層１６と多層基板と、該多層基板の上に表面実装されたコンデンサチップ９とを含み、該コンデンサ９と入出力端子１１以外のフィルタの構成要素を内部の導体層に設けた、８００ＭＨｚ～２ＧＨｚ帯のトラップ付きバンドパスフィルタを提供する。さらに、このトラップ付きバンドパスフィルタにおいて、フィルタを構成する導体層５～８を貫通スルーホール１２～１４により電気的に接続したフィルタを提供する。



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【特許請求の範囲】

【請求項１】　複数の導体層と複数の有機系誘電体層とを含む多層基板と、該多層基板の上に表面実装されたコンデンサチップとからなり、該コンデンサと入出力端子以外のフィルタの構成要素を該多層基板内部の導体層に設けた！８００ＭＨｚ～２ＧＨｚ帯のトラップ付きバンドパスフィルタ。

【請求項２】　フィルタを構成する導体層を貫通スルーホールにより電気的に接続したことを特徴とする請求項１記載の８００ＭＨｚ～２ＧＨｚ帯のトラップ付きバンドパスフィルタ。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、携帯電話や、ＰＨＳ（ｐｅｒｓｏｎａｌ　ｈａｎｄｙ　ｐｈｏｎｅｓｙｓｔｅｍ）用の携帯用無線機等に用いられる８００ＭＨｚ～２ＧＨｚ帯の高周波バンドパスフィルタに関し、より具体的には、有機系多層基板の内層に構成した多層基板内層型トラップ付きバンドパスフィルタに関する。

【０００２】

【従来の技術】携帯電話や、ＰＨＳの急速な普及により、携帯用無線機の性能の向上と小型化が強く求められている。一般的な電子回路については、より多くの回路素子がワンチップに納められるなどして小型化が進む中、特に８００ＭＨｚ～２ＧＨｚ帯の高周波バンドパスフィルタの小型化が強く望まれている。また、製造コストの引き下げ、全体的な製造工程の簡略化などの既存の課題に対する解決がより緊急に求められている。

【０００３】従来、コンデンサやコイルなどのバンドパスフィルタの構成要素をセラミックスの多層基板に作り込む技術はよく知られている。このようなバンドパスフィルタは、他の回路要素と一緒にセラミックス基板内に納めることができるので、バンドパスフィルタだけのための別個の製造工程を必要とせず、回路の小型化も可能であるという利点を有していた。

【０００４】しかし、セラミックス製の多層基板は、一般的に、（１）強度が低く割れやすいため、取り扱いが難しく、（２）誘電率が高いため、設計が難しい、（３）焼成という工程が必要なため、製造コストが大変高く、また、納期に時間がかかる、といった問題があり、未だに製品としては少ない例しかない。セラミックスを使用したバンドパスフィルタは、フィルタチップとして携帯電話用に既に販売されているが、このようなチップ部品の実装領域の大きさは相当なものであり、それを使用した回路全体の小型化の妨げとなっている。そして、上記のような、セラミックス多層基板が一般に有する問題点を持っている。

【０００５】

【発明が解決しようとする課題】本発明の目的は、標準的な有機系多層基板と市販のコンデンサチップを使用して、安価で小型の８００ＭＨｚ～２ＧＨｚ帯のトラップ付きバンドパスフィルタを提供することを目的とする。

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【０００６】

【課題を解決するための手段】本発明は、複数の導体層と複数の有機系誘電体層とを含む多層基板と、該多層基板の上に表面実装されたコンデンサチップとからなり、該コンデンサと入出力端子以外のフィルタの構成要素を内部の導体層に設けた、８００ＭＨｚ～２ＧＨｚ帯のトラップ付きバンドパスフィルタを提供する。さらに、本発明は、上記トラップ付きバンドパスフィルタにおいて、フィルタを構成する導体層を貫通スルーホールにより電気的に接続したフィルタを提供する。

【０００７】

【発明の実施の形態】本発明において用いられるコンデンサチップは、広く市販されているコンデンサチップを使用することができる。コンデンサの容量としては、約０．５ｐＦから約３ｐＦ程度である。現在市販されているコンデンサチップの大きさは、約１ｍｍから約２ｍｍ程度の大きさである。このように、コンデンサチップ自体の大きさが小さいので、バンドパスフィルタ全体の大きさも小さいものとすることができ、回路の小型化が図れる利点が本発明にはある。また、コンデンサチップを使用したことにより、有機系基板材料の誘電損失の影響が少なくなるという利点がある。

【０００８】本発明における導体層は、チップコンデンサを表面実装するための導体部分を１層と数えて、フィルタ回路の要部を構成するストリップラインとあわせて最低でも２層必要である。通常は、２層のシールド用導体膜とあわせて、少なくとも４層必要である。しかし、誘電体層の数も同様であるが、それ以上の任意の数の導体層があってよい。

【０００９】本発明のバンドパスフィルタにおいて用いられる基板用の有機系誘電体としては、特に限定はされないが、ガラスエポキシ樹脂などを好適に用いることができる。また誘電体層の数は、特に限定されない。上記のようにシールド層２層を加えて４層の導体層がある場合には、誘電体層の数は、３以上であればよく、上限は特にない。

【００１０】特に、本発明のバンドパスフィルタは、一般的に広く利用されている有機系誘電体を基板材料として使用しているので、フィルタ以外の、例えば、ローノイズアンプやミキサ回路とともに一つの多層基板中に構成することができることを特徴としている。このような場合には、４以上の誘電体層を用いることが有利な場合がある。

【００１１】入出力のためのＩ／Ｏ端子を構成する部分は、例えば、チップコンデンサが表面実装される表面に設けることができるが、その他の構成も可能である。例えば、他の回路と同一の多層基板に本発明のバンドパスフィルタを設ける場合には、入出力を多層基板の表面で

はなく、その内部で行うことが好ましい場合がある。また、導体層間の電気的な接続は、スルーホールにより行うことができるが、本発明の場合には、層構成が簡素化できるので、ブラインドスルーホールではなく、貫通スルーホールによりこの接続を行うことができる。貫通スルーホールにより電気的接続を行う場合には、導体層と誘電体各層を貫通する穴を開けて、その後メッキ処理等によりその穴を導体で満たすことにより、ブラインドスルーホールの場合に較べて製造工程がより簡易になる。

【００１２】

【実施例】以下に具体的な回路構成を参照しながら、本発明のバンドパスフィルタの構成と特性をより詳細に説明する。しかし、下記の実施例は、単に例として示したものであり、特許請求の範囲に記載された発明の範囲を限定するものではない。図１には、本発明の一実施例である通過帯域の上下にトラップを入れたバンドパスフィルタの回路構成を示す。この回路は、ＰＨＳ用に設計されたものである。本実施例においては、コンデンサ１の容量Ｃｍを、１ｐＦとし、１００５チップとして広く市販されているものを用いた。主要なストリップライン２、３が示されており、ストリップライン３同士の結合定数はＭである。入出力用の端子４がある。

【００１３】また、図２には、図１の回路構成を実現するための導体層５～８のパターンを示す。図２において、導体層４層５～８のパターンとそれを電気的に接続するための貫通スルーホール１２～１４のみが示されている。表面を構成する第１層５には、チップコンデンサ９が置かれ、このコンデンサ接続用の端子部分１０と入出力用の導体部分１１が設けられている。この第１層５の表面にはすべてのスルーホール１２～１４が見える。第２層６はグラウンドのシールド層をなす内層であり、コンデンサチップ用端子１０と入出力用端子１１にそれぞれ接続するスルーホール１３と１４は、このシールド層とは電気的に接続していない。しかし、グラウンド用のスルーホール１２が、この第２層６に電気的に接続している。さらに、もう一つの内層である第３層７には、本発明のフィルタのコンデンサ以外の回路要素となるストリップライン１５が導体膜により形成されている。３組６本のスルーホール１２～１４のすべてが、この第３層の導体と何らかの形で電気的に接続している。第４層８の導体は、裏面に当たるシールド層を形成している。このシールド用導体膜に電気的に接続しているのは、グラウンド用スルーホール１２のみであり、他のスルーホール１３、１４は、裏面の表面に出ているものの、このシールド用導体膜に電気的に接続していない。

【００１４】なお、図２においては導体のパターンとスルーホールのみを示した。現実の回路を構成するためには、この導体層間に有機系誘電体の層を配置する。この誘電体層の材質としては、本実施例においては、三菱ガス化学製ＥＬ２４０を用い、層厚としては、１層当たり約０．３ｍｍを採用した。導体層の厚さは約１８μｍであった。

【００１５】図３には、この導体パターンの平面図とその大きさを示す。パターンの縦と横の大きさは、それぞれ、約５．５ｍｍと約９ｍｍとした。パターン中の各要素大きさは、縦横の辺の長さにほぼ縮尺して示してある。

【００１６】図４には、積層した誘電体層１６と導体層の断面を模式的に示す。この図においては、貫通スルーホール１２と１３が貫通して表面と裏面に出ている様子が看取できる。

【００１７】図５と図６には、本実施例のトラップ付きバンドパスフィルタの特性について、実際に測定した結果を示す。図５には、通過特性を周波数の関数として示す。図６には、リターンロス特性を同じく周波数の関数として示す。

【００１８】

【発明の効果】上述のように、本発明によれば、導体層の構成を簡素化できる。したがって、例えば、４層の導体と貫通スルーホールのみでトラップ付きバンドパスフィルタを構成することができる。また、チップコンデンサを用いるため、フィルタ回路の小型化を図ることができる。さらに、一般的な回路に用いられる有機系多層基板を使用しているので、他の回路、アンプ回路やミキサー回路などを本発明のフィルタと同じ基板中に構成できるので、通信機に必要な回路全体の小型化に役立つ。

【図面の簡単な説明】

【図１】本発明の実施例の回路図を示す。

【図２】図１の実施例の回路を実現するための導体層のパターンと貫通スルーホールを示す。

【図３】図１の実施例の回路を実現するための導体層のパターンを示す。

【図４】積層した上記実施例にかかるフィルタの断面の模式図を示す。

【図５】上記実施例のフィルタの周波数通過特性を示す。

【図６】上記実施例のフィルタの周波数リターンロス特性を示す。

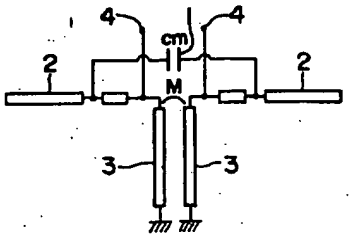
【符号の説明】

１　コンデンサ
２、３　ストリップライン
４　入出力端子
５　第１導体層（表面）
６　第２導体層
７　第３導体層
８　第４導体層（裏面）
９　コンデンサチップ
１０　コンデンサチップ用導体
１１　入出力端子導体
１２　グラウンド用貫通スルーホール

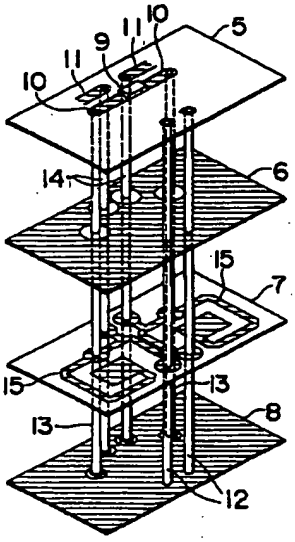
5　　6

13、14　貫通スルーホール
15　ストリップライン導体
16　誘電体層

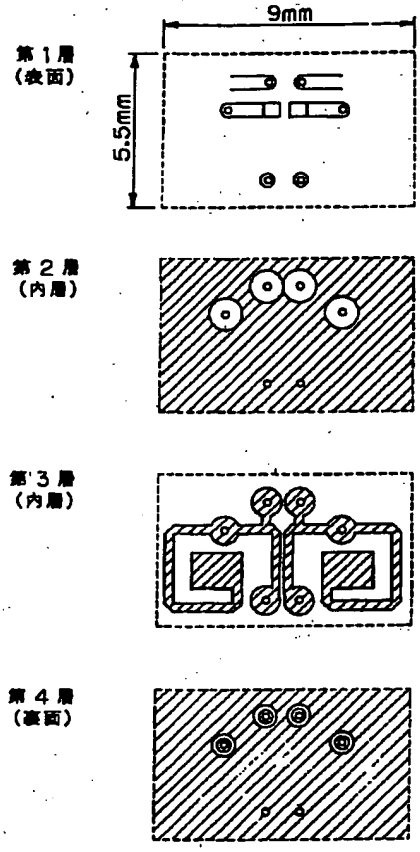
【図1】



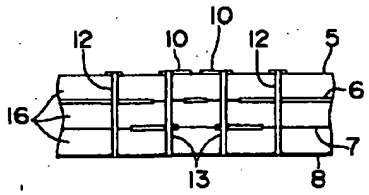
【図2】



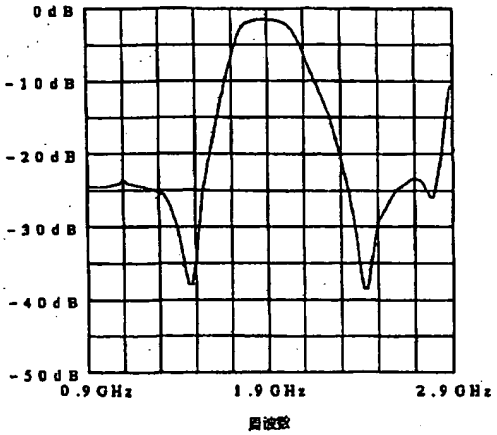
【図3】



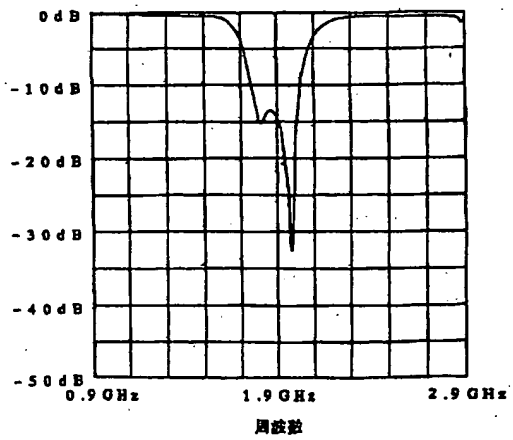
【図4】



【図5】



【図6】



PAT-NO: JP409130103A

DOCUMENT-IDENTIFIER: JP 09130103 A

TITLE: BAND PASS FILTER PROVIDED WITH MULTI-LAYERED SUBSTRATE-INCORPORATED TRAP

PUBN-DATE: May 16, 1997

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APPL-NO: JP07283017

APPL-DATE: October 31, 1995

INT-CL (IPC): H01P001/203, H01P001/205

ABSTRACT:

PROBLEM TO BE SOLVED: To provide an inexpensive and compact band pass filter provided with trap of 800MHz to 2GHz band by using a standard organic multilayered substrate and a capacitor ship on the market.

SOLUTION: This band pass filter provided with trap of 800MHz to 2GHz band consists of conductor layers 5 to 8, an organic dielectric layer, a multilayered substrate, and a capacitor chip 9 mounted on the multilayered substrate, and components of the filter other than the capacitor 9 and an input/ output terminal 11 are provided on internal

conductor layers. Conductor layers 5 to 8 constituting the filter are electrically connected to each other via through hole 12 to 14.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] More specifically, this invention relates to the band pass filter with a multilayer substrate inner layer mold trap constituted in the inner layer of an organic system multilayer substrate about the high frequency band pass filter of the 800MHz - 2GHz band used for a cellular phone, the portable walkie-talkie for PHS (personal handy phonesystem), etc.
[0002]
[Description of the Prior Art] Improvement and a miniaturization of the engine performance of a portable walkie-talkie are strongly called for by the cellular phone and the rapid spread of PHS. About the general electronic circuitry, while more circuit elements are dedicated to a one chip and a miniaturization progresses, a miniaturization of the high frequency band pass filter of a 800MHz - 2GHz band is desired especially strongly. Moreover, the solution to the existing technical problems, such as reduction in a manufacturing cost and simplification of an overall production process, is called for more nearly immediately.
[0003] Conventionally, the technique which makes the component of band pass filters, such as a capacitor and a coil, to the multilayer substrate of the ceramics is known well. Since such a band pass filter was dedicated in the ceramic substrate together with other circuit elements, the separate production process only for a band pass filter was not needed, but it had the advantage that the miniaturization of a circuit was also possible.
[0004] However, the multilayer substrate made from the ceramics has the problem that handling is generally difficult since (1) reinforcement tends to break low, a manufacturing cost is very high since (2) dielectric constants are high and the process of (3) baking with a difficult design is required, and time for delivery takes time amount, and has only few [still] examples as a product. Although the band pass filter which used the ceramics is already sold to cellular phones as a filter chip, the mounting area size of such a chip is considerable, and serves as hindrance of a miniaturization of the whole circuit which used it. And the above ceramic multilayer substrates have the trouble which it generally has.
[0005]
[Problem(s) to be Solved by the Invention] The purpose of this invention uses a standard organic system multilayer substrate and a commercial capacitor chip,

and aims at offering the band pass filter with a trap of a cheap and small 800MHz - 2GHz band.

[0006]

[Means for Solving the Problem] This invention offers the band pass filter with a trap of the 800MHz - 2GHz band which consisted of a capacitor chip by which the surface mount was carried out, and prepared the component of this capacitor and filters other than an input/output terminal at the internal conductor layer on the multilayer substrate containing two or more conductor layers and two or more organic system dielectric layers, and this multilayer substrate. Furthermore, this invention offers the filter which connected electrically the conductor layer which constitutes a filter by the penetration through hole in the above-mentioned band pass filter with a trap.

[0007]

[Embodiment of the Invention] The capacitor chip used in this invention can use the capacitor chip marketed widely. As a capacity of a capacitor, it is about 0.5pF to about 3pF. The capacitor chip size by which current marketing is carried out is about 1 to about 2mm in magnitude. Thus, since the magnitude of the capacitor chip itself is small, it can consider as what also has the small magnitude of the whole band pass filter, and the advantage which can attain the miniaturization of a circuit is in this invention. Moreover, there is an advantage that the effect of the dielectric loss of an organic system substrate ingredient decreases, by having used the capacitor chip.

[0008] a conductor for the conductor layer in this invention to carry out the surface mount of the chip capacitor -- also at the lowest in accordance with the stripline which counts a part with one layer and constitutes the important section of a filter circuit, it is the two-layer need. usually, the two-layer object for shielding -- a conductor -- in accordance with the film, at least four layers are required. However, although the same is said of the number of dielectric layers, there may be a conductor layer of the number of the arbitration beyond it.

[0009] As an organic system dielectric for substrates used in the band pass filter of this invention, although especially limitation is not carried out, it can use a glass epoxy resin etc. suitably. Moreover, especially the number of dielectric layers is not limited. When shielding layer two-layer is added as mentioned above and there is a conductor layer of four layers, there is especially no upper limit that the number of dielectric layers should just be three or more.

[0010] Since the organic system dielectric generally used widely is being used especially for the band pass filter of this invention as a substrate ingredient, it is characterized by the ability to constitute in one multilayer substrate with for example, the low noise amplifier and mixer circuits other than a filter. In such a case, it may be advantageous to use four or more dielectric layers.

[0011] Other configurations are also possible although the part which constitutes the I/O terminal for I/O can be prepared in the front face on which the surface mount of the chip capacitor is carried out. For example, when preparing the band pass filter of this invention in the same multilayer substrate as other circuits, it may be desirable to output and input not in the front face of a multilayer substrate but in the interior. Moreover, in the case of this invention, although electric

connection between conductor layers can be made by the through hole, since lamination can be simplified, this connection can be made not by the blind through hole but by the penetration through hole. When a penetration through hole performs electrical installation, compared with the case of a blind through hole, a production process becomes simpler by making the hole which penetrates a conductor layer and dielectric each class, and filling the hole with a conductor by plating processing etc. after that.

[0012]

[Example] The configuration and property of a band pass filter of this invention are explained more to a detail, referring to concrete circuitry below. However, the following example is only shown as an example and does not limit the range of invention indicated by the claim. The circuitry of the band pass filter of the passband which is one example of this invention into which the trap was put up and down is shown in drawing 1 . This circuit is designed for PHS. In this example, capacity Cm of a capacitor 1 was set to 1pF, and what is widely marketed as 1005 chips was used. The main striplines 2 and 3 are shown and the coupling constant of stripline 3 comrades is M. There is a terminal 4 for I/O.

[0013] Moreover, the pattern of the conductor layers 5-8 for realizing the circuitry of drawing 1 is shown in drawing 2 . In drawing 2 , only the penetration through holes 12-14 for connecting it with the pattern of 5-8 electrically four layers of conductor layers are shown. a front face is constituted -- a chip capacitor 9 puts the 1st layer on 5 -- having -- the conductor a part for a terminal area 10, and for the I/O for this capacitor connection -- the part 11 is formed. All the through holes 12-14 are visible to the front face of this 1st layer 5. 6 is a inner layer which makes the shielding layer of a ground, and the 2nd layer of this shielding layer has not connected electrically the through holes 13 and 14 connected to the terminal 10 for a capacitor chip, and the terminal 11 for I/O, respectively. however, the through hole 12 for grounds -- this -- the 2nd layer has connected with 6 electrically. furthermore, the stripline 15 which is another inner layer and which serves as circuit elements other than the capacitor of the filter of this invention the 3rd layer 7 -- a conductor -- it is formed with the film. All the 3-set six through holes 12-14 have connected with the conductor of this 3rd layer electrically in a certain form. The conductor of 8 forms the 4th layer of the shielding layer which hits a rear face. this object for shielding -- a conductor -- although it is only the through hole 12 for grounds which is electrically connected to the film and has come out of other through holes 13 and 14 on the surface of the rear face -- this object for shielding -- a conductor -- it has not connected with the film electrically.

[0014] In addition, only the pattern and through hole of a conductor were shown in drawing 2 . In order to constitute an actual circuit, the layer of an organic system dielectric is arranged between this conductor layer. As the quality of the material of this dielectric layer, about 0.3mm per layer was adopted as thickness in this example using Mitsubishi Gas Chemical EL240. The thickness of a conductor layer was about 18 micrometers.

[0015] The top view and magnitude of this conductor pattern are shown in drawing 3 . Length of a pattern and horizontal magnitude were set to about

5.5mm and about 9mm, respectively. Each element magnitude in a pattern is mostly reduced to the die length of the side in every direction, and is shown in it.
[0016] The cross section of the dielectric layer 16 which carried out the laminating, and a conductor layer is typically shown in drawing 4 . In this drawing, signs that the penetration through holes 12 and 13 penetrated and it has come out to the front face and the rear face can be ****(ed).
[0017] The actually measured result is shown in drawing 5 and drawing 6 about the property of the band pass filter with a trap of this example. A passage property is shown in drawing 5 as a function of a frequency. Similarly a return loss property is shown in drawing 6 as a function of a frequency.
[0018]
[Effect of the Invention] As mentioned above, according to this invention, the configuration of a conductor layer can be simplified. It can follow, for example, a band pass filter with a trap can consist of only a conductor of four layers, and a penetration through hole. Moreover, since a chip capacitor is used, the miniaturization of a filter circuit can be attained. Furthermore, since the organic system multilayer substrate used for a general circuit is used and other circuits, amplifier circuits, mixer circuits, etc. can be constituted in the same substrate as the filter of this invention, it is useful to the miniaturization of the whole circuit required for a transmitter.

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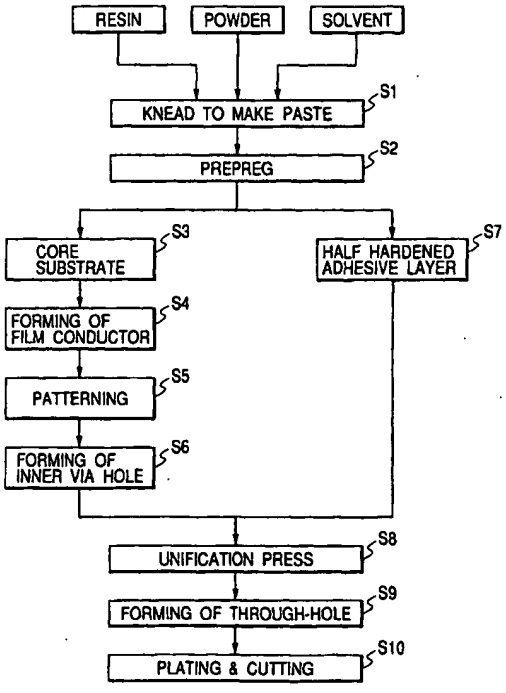
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(54) Electronic parts and method producing the same

(57) The invention is to offer electronic parts and a method of producing the same in which a producing time is shortened, crack or warp are hard to occur, and cost-down can be attained. Core substrates are made by forming a resin or a compound material made by mixing powder-like functional materials with this resin into thin plates, and hardening them. Conductor patterns are formed on at least any of front and back surfaces of the core substrates through any of an evaporation process, an ion plating process, an ion beam process, a sputtering process, and a vapor deposition process, followed by patterning. Half-hardened prepregs are produced by forming the resin or the compound material made by mixing powder-like functional materials with this resin into the thin plates. The prepregs and the core substrates are alternately laminated and laminated layers are made by unifying through a hot pressing.

FIG. 1



EP 1 235 235 A1

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Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates to electronic parts formed in a multilayer structure by use of a resin or a compound material made by mixing powder functional material into this resin, and to a method of producing the same.

[0002] As a method of producing multilayer electronic parts by use of thin film conductors, JP-A-5-267063 discloses a method in Fig. 5 of the drawings attached herewith. As shown in the same, for instance, in case of producing an inductor, powders of raw material are mixed for providing desired functions as ferrite (Step S1), and granulating and pulverizing are carried out (Step S2). Then, the substances mixed and regulated in predetermined grain diameter are turned out to be enamels by use of binder and solvent (Step S3).

[0003] Laminating and baking steps carry out a screen printing (Step S4) of the ferrite paste, a pre-baking (Step S5) by rising temperature in a drying furnace, installation of inductor electrodes (Step S6) by forming the film through any of an evaporation, a spattering and an ion plating, and a screen printing (Step S7) of the ferrite paste. These steps are repeated several times until obtaining patterns of desired number. The forming of the electrode patterns is carried out simultaneously for many pieces of inductors.

[0004] Thereafter, products are cut per each of chips (Step S8), and the chips are formed on sides with external electrodes by coating, evaporation or spattering (Step S9). Subsequently, other areas than the external electrodes are subjected to a silicone impregnation so that pores in the chip surface are impregnated with a synthetic (silicone) resin (Step S10). IF necessary, the external electrodes are subjected to an electroplating (Step S11).

[0005] For producing the multiplayer electronic parts using a resin or a compound material made by mixing functional materials (dielectric powder or magnetic powder) with this resin and thin film conductor formed by the evaporation or the like, the multilayer electronic parts are produced by repeating the printing of the compound material paste, the thermosetting and the forming of the thin film conductor.

[0006] In case of producing the electronic parts by the procedure of repeating the printing and the hardening as seen in the conventional examples, there have been problems that production cost is high, and a period till production is very long.

[0007] In addition, in the case of ceramics, for printing or forming the thin film conductor after baking, influences of fragility of a prime body are easy to appear, or as stress is loaded thereon, problems about cracks or warp easily occur. Laminated layers are baked for hours by nature, and when the number of layer increases, a long production time and cost are consumed.

[0008] Also in the case of the resin or the compound material, since the thermosetting and the printing are repeated to cause large stress loading thereon, the printed faces are roughened and when the number of layer increases, it becomes difficult to produce.

SUMMARY OF THE INVENITON

[0009] In view of the above mentioned problems, it is an object of the invention to provide electronic parts and a method of producing the same in which the producing time is shortened, and crack or warp are hard to occur, reduction of cost can be attained, and the production can be performed even if the number of layer is many.

[0010] A method of producing electronic parts of a first aspect of the invention is characterized by comprising: forming a resin or a compound material made by mixing powder-like functional materials with this resin into thin plate, hardening it to be core substrates; forming thin film conductor on at least any of front and back surfaces of the core substrate through any of an evaporation process, an ion plating process, an ion beam process, a vapor deposition process, and a sputtering process, followed by patterning; forming the resin or the compound material made by mixing powder-like functional materials with this resin into the prepregs like thin plates, alternately laminating half-hardened prepregs and the core substrates, and subsequently hot-pressing and unifying into multilayer parts.

[0011] As seeing, if the core substrate and the prepreg are separately produced, and lamination and hardening are carried out concurrently, the production time can be shortened and the cost is lowered. Since the whole is once hardened by hot-pressing, crack or warp are hard to occur, and the production is possible even though the number of layer is many.

[0012] Further, the thin film conductor can be made thin, so that it is possible to firstly make parts thin (in particular, this effect is remarkably in a capacitor), secondly heighten patterning precision and accuracy inlayer-to-layer, and thirdly avoid migration because the thin film conductor is thin so that the resin is buried around its periphery. In this application, the term "powder-like" includes grain form, flake form, needle form, spike form, or the like. .

[0013] An electronic part of a second aspect of the invention is characterized by comprising: a core substrate made by forming the resin or the compound material made by mixing the powder functional materials with this resin into thin plates, and hardening it; a thin film conductor formed on at least any of front and back surfaces of the core substrate through the film forming technique and carried out with the patterning; and an adhesive layer formed with the resin or the compound material made by mixing the powder-like functional material with this resin, and interposed among core substrates formed with the thin film conductors; wherein laminated layers made of the core substrates and the

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prepregs for the adhesive layers are unified by hot-pressing.

[0014] If the electronic parts are composed of such a laminated structure, as mentioned in the first aspect, the production time can be shortened, the cost is lowered and crack or warp are avoided from occurrence.

[0015] The electronic part of a third aspect of the invention is, in the second aspect, that the thin film conductor has thickness less than 5 μm.

[0016] When the thickness is more than 5 μm, time is taken too much for forming the thin film, and it is difficult to shorten the production time. Because the thickness restricted less than 5 μm, it is possible to avoid the manufacturing time from becoming long. In case of the thickness is less than 1 μm, a conductor resistance becomes large. Therefore, in order to maintain a Q value at a predetermined level, thickness of the thin film conductor preferably has more than 1μm. However, in case of capacitor or noise removing circuit which allows large loss, thickness of the thin thin film conductor may be less than 1μm, but more than 0.3μm.

[0017] Moreover, according to the electronic part of the present invention, as a resin, at least one thermosetting resin selected from a group consisting of epoxy resin, phenol resin, unsaturated polyester resin, vinyl ester resin, polyimde resin, bismaleimidotriazine (cyanate ester) resin, polyphenyle ether (oxide) resin, fumarate resin, polybutadiene resin, and vinylbenzyl resin, or at least one thermoplastic resin selected from a group consisting of aromatic polyester resin, polyphenylene sulfide resin, polyethylene terephtharate resin, polybutylene terephtalate resin, polyethylene sulfide resin, polyethyl ehter ketone resin, polytetrafluoroethylene resin, polyarylate resin and graft resin, or a composite resin composed of at least one of the thermosetting resin and at least one of the thermoplastic resin may be used.

[0018] . Moreover, according to the electronic part of the present invention, as the powder-like functional material, at least one ferrite magnetic material selected from a group consisting of Mn-Mg-Znbasedmagnetic material, Ni-Zn based magnetic material, and Mn-Zn based magnetic material, or at least one ferromagnetic metallic magnetic material selected from a group consisting of carbonyl iron, iron-silicon based alloy, iron-aluminum-silicon based alloy, iron-nickel based alloy, and amorphous (iron based or cobalt based) alloy, or at least one dielectric material selected from a group consisting of $BaO\text{-}TiO_2\text{-}Nd_2O_3$ based dielectric material, $BaO\text{-}TiO_2\text{-}SnO_2$ based dielectric material, PbO-CaO based dielectric material, TiO_2 based dielectric material, $BaTiO_3$ based dielectric material, $PbTiO_3$ based dielectric material, $SrTiO_3$ based dielectric material, $CaTiO_3$ dielectric material, Al_2O_3 based dielectric material, $BiTiO_4$ based dielectric material, $MgTiO_3$ based dielectric material, $(Ba, Sr)TiO_3$ based dielectric material, $Ba(Ti, Zr)O_3$ based dielectric material, $BaTiO_3\text{-}SiO_2$ based dielectric material, $BaO\text{-}SiO_2$ based dielectric material, $CaWO_4$ based dielectric material, $Ba(Mg, Nb)O_3$ based dielectric material, $Ba(Mg, Ta)O_3$ based dielectric material, $Ba(Co, Mg, Nb)O_3$ based dielectric material, $Ba(Co, Mg, Ta)O_3$ based dielectric material, Mg_2SiO_4 based dielectric material, $ZnTiO_3$ based dielectric material, $SrZrO_3$ based dielectric material, $ZrTiO_4$ based dielectric material, $(Zr, Sn)TiO_4$ based dielectric material, $BaO\text{-}TiO_2\text{-}Sm_2O_3$ based dielectric material, $PbO\text{-}BaO\text{-}Nd_2O_3\text{-}TiO_2$ based dielectric material, $(Bi_2O_3, PbO)\text{-}BaO\text{-}TiO_2$ based dielectric material, $La_2Ti_2O_7$ based dielectric material, $Nd_2Ti_2O_7$ based dielectric material, $(Li, Sm)TiO_3$ based dielectric material, $Ba(Zn, Ta)O_3$ based dielectric material, $Ba(Zn, Nb)O_3$ based dielectric material and $Sr(Zn, Nb)O_3$ based dielectric material, or composite functional material composed of at least two of the above mentioned ferrite magnetic materials, ferromagnetic metallic magnetic materials, and dielectric materials may be used.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019]

Fig. 1 is a processing diagram showing one embodiment of the production method of the electronic parts according to the invention;
Figs. 2A to 2E are explanatory views of procedures of one parts practicing the production method of the electronic part according to the invention;
Figs. 3A to 3E are explanatory views of procedures of remaining parts practicing the production method of the electronic part according to the invention;
Fig. 4A is a cross sectional view showing one example of the electronic part according to the invention, and Fig. 4B is a view of layer-structure; and
Fig. 5 is a procedure showing the conventional production method of the electronic part.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0020] Fig. 1 is a processing diagram showing one embodiment of the production method of the electronic parts according to the invention, and Figs. 2 and 3 are explaining views illustrating respective steps.

[0021] In the Step S1 of Fig. 1, for producing the compound material, the resin is added with the powder-like functional material (magnetic material powder or dielectric material powder) and a solvent such as toluene, and kneaded to make a paste. Herein, as the resins, at least one thermosetting resin selected from a group consisting of epoxy resin, phenol resin, unsaturated polyester resin, vinyl ester resin, polyimde resin, bismaleimidotriazine (cyanate ester) resin, polyphenyle ether (oxide) resin, fumarate resin, polybutadiene resin, and vinilbenzyl resin, or at least one thermoplastic resin selected from a group consisting of aromatic polyester resin, polyphenylene sulfide resin, polyethylene terephtharate

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resin, polybutylene terephtalate resin, polyethylene sulfide resin, polyethyl ehter ketone resin, polytetrafluoroethylene resin, polyarylate resin and graft resin, or a composite resin composed of at least one of the thermosetting resin and at least one of the thermoplastic resin may be used.

[0022] . The powder-like functional material to be mixed with these resin is at least one ferrite magnetic material selected from a group consisting of Mn-Mg-Zn based magnetic material, Ni-Zn based magnetic material, and Mn-Zn based magnetic material, or at least one ferromagnetic metallic magnetic material selected from a group consisting of carbonyl iron, iron-silicon based alloy, iron-aluminum-silicon based alloy, iron-nickel based alloy, and amorphous (iron based or cobalt based) alloy, or at least one dielectric material selected from a group consisting of $BaO\text{-}TiO_2\text{-}Nd_2O_3$ based dielectric material, $BaO\text{-}TiO_2\text{-}SnO_2$ based dielectric material, PbO-CaO based dielectric material, TiO_2 based dielectric material $BaTiO_3$ based dielectric material, $PbTiO_3$ based dielectric material, $SrTiO_3$ based dielectric material, $CaTiO_3$ based dielectric material, Al_2O_3 based dielectric material, $BiTiO_4$ based dielectric material, $MgTiO_3$ based dielectric material, (Ba, Sr)TiO_3 based dielectric material, Ba(Ti, Zr)O_3 based dielectric material, $BaTiO_3\text{-}SiO_2$ based dielectric material, $BaO\text{-}SiO_2$ based dielectric material, $CaWO_4$ based dielectric material, Ba (Mg, Nb)O_3 based dielectric material, Ba(Mg, Ta)O_3 based dielectric material, Ba(Co, Mg, Nb)O_3 based dielectric material, Ba(Co, Mg, Ta)O_3 based dielectric material, Mg_2SiO_4 based dielectric material, $ZnTiO_3$ based dielectric material, $SrZrO_3$ based dielectric material, $ZrTiO_4$ based dielectric material, (Zr, Sn) TiO_4 based dielectric material, $BaO\text{-}TiO_2\text{-}Sm_2O_3$ based dielectric material, $PbO\text{-}BaO\text{-}Nd_2O_3\text{-}TiO_2$ based dielectric material, (Bi_2O_3, PbO)-BaO-TiO_2 based dielectric material, $La_2Ti_2O_7$ based dielectric material, $Nd_2Ti_2O_7$ based dielectric material, (Li, Sm) TiO_3 based dielectric material, Ba (Zn, Ta) O_3 based dielectric material, Ba (Zn, Nb) O_3 based dielectric material and Sr (Zn, Nb) O_3 based dielectric material, or composite functional material composed of at least two of the above mentioned ferrite magnetic materials, ferromagnetic metallic magnetic materials, and dielectric materials may be used.

[0023] For reducing the invention to practice, other resin, magnetic powder and dielectric powder may be of course served.

[0024] In the Step S2 of Fig. 1, the prepreg is made as shown in Fig. 2A. That is, a glass cloth wound on a reel 3 is drawn out into a container 1 supporting the paste 2 of the compound material, and is immersed in the paste 2. Subsequently, the paste coated on the glass cloth 4 is dried by passing the glass cloth 4 through a dryer 5, and a blank material 7 is wound on a reel 6. Then, this blank material 7 is cut by a cutter 8 into desired sizes as shown in Fig. 2B, and glass-cloth-contained prepregs 9 are produced.

[0025] The thus produced prepregs are divided into left-side Steps S3 to S6 of Fig. 1 and a right-side Step S7, and utilized as the core substrate 9a (see Fig. 2C) or as the prepreg 9b as a half hardened adhesive layer (see Fig. 2F). For forming the core substrate (Step S3), in case, e.g., the vinyl benzyl resin is used to the compound material paste, it is carried out at 200°C for 2 hours.

[0026] As to the half-hardening of the prepreg 9b of Step S7, in case of using, for example, vinyl benzyl resin in the compound material 2, it is practiced at 110°C for 1 hour.

[0027] In the thin film conductor forming process in Step S4, as shown in Fig. 2D, the thin film conductor 10 is formed on the front and back surfaces of the core substrate 9a through the thin film forming technique such as the evaporation process, the ion plating process, the ion beam process, the sputtering process, and the vapor deposition process. In this case, as the thin film conductor 10, copper, silver, nickel, tin, zinc, or aluminum may be used.

[0028] In the patterning process of Step S5, a resist film is formed on the core substrate 9a, and passing through exposure for forming patterns of conductor layer thereafter, partial removal of the resist film, thin film conductor etching on the removed areas, and resist film removing process, the patterned thin film conductors 11 are formed in Fig. 2E. The thin film conductors 11 are many on one sheet of core substrate 9a, and a plurality of the same patterns are arranged longitudinally and laterally. There is also the method of forming a thin film conductor pattern through a mask as methods other than the above patterning process.

[0029] In an inner via forming process of Step S6, as shown in Fig. 3A, via holes 12 are formed by drilling, punching or laser applying, and the inner wall thereof is plated with the conductor 13, and the patterns 11, 11 on the both surfaces of the core substrate 9a are connected each other. Thus, when plating conductor 13 in the inner wall of a via hole 12, proper masking, such as a resist film coating, is performed to thin film conductor 11 so as to not thicken the thickness of the conductor 11.

[0030] In a unification press of Step S8, as shown in Fig. 3B, the core substrate 9a and the prepreg 9b as the adhesive layer are alternately laminated, and subjected to hot-pressing at substantially hardening temperatures and for time therefor, whereby the layer of the prepreg 9b is also substantially hardened. Thus, the unified and laminated layers 14 are produced as shown in Fig. 3C.

[0031] In forming through-holes of Step S9, as shown in Fig. 3D, the through-holes 15 are formed by the drilling, punching or laser applying and the inner walls thereof are plated with the conductor 16, and the pattern 11-to-the pattern 11 on the both surfaces of the core substrate 9a or these inner patterns-to-the patterns 11, otherwise the inner pattern 11-to-the inner pattern 11 are connected each other.

[0032] In the plating process and cutting process in

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Step S10, the required plating as solder-plating is performed, followed by cutting into chips in pieces. As shown in Fig. 3E, when mounting parts 17, these parts 17 are soldered before or after cutting into pieces of chips.

[0033] The core substrate 9a and the prepreg 9b are separately made and laminated, and hardening are concurrently carried out, whereby the production time is shortened and the reduction of cost can be attained. In addition, as the whole is once hardened by the hot pressing, crack or warp are hard to occur. If the pattern 11 is formed by use of copper foil as conventionally, it is generally used a foil having thickness around 18 μm. On the other hand, when the pattern is formed with the thin film conductor 11 as the invention, a thin film of lower than 9 μm can be easily produced. Therefore, the laminated layers are less rugged by the thickness of the conductor 11, and properties when forming capacitors or inductors are little in dispersion.

[0034] The thickness of the thin film conductor 10 is preferably less than 5 μm. When the thickness of the thin film conductor 10 is more than 5 μm, time is taken too much for forming the thin film, and it is difficult to shorten the production time. Because the thickness restricted less than 5 μm, it is possible to avoid the manufacturing time from becoming long. In case of the thickness is less than 1 μm, a conductor resistance becomes large. Therefore, in order to maintain a Q value at a predetermined level, thickness of the thin film conductor preferably has more than 1μm. However, in case of capacitor or noise removing circuit which allows large loss, thickness of the thin film conductor may be less than 1μm, but more than 0.3μm.

[0035] Fig. 4A is a cross sectional view showing one example of the electronic part according to the invention, and Fig. 4B is a view of layer-structure. This example is a voltage controlled oscillator (VCO), and 9a is the core substrate, 9b is the prepreg or a prepreg hardened and adhered to the core substrate 9a. Reference numeral 19 is a surface land pattern, 20 is capacitor electrodes, 21 is ground electrodes holding strip lines 22 composing a resonator therebetween. Reference numeral 17 is parts of semi-conductor such as transistors or variable capacitance diode, or mounted parts comprising capacitor of large capacitance, inductor chip, or chip resistor.

[0036] The invention can be realized, other than the above mentioned examples, as a capacitor, inductor, LC filter, LCR filter or various kinds of modules in which semiconductor devices and passive parts (circuit) are combined, that is, hybrid integrated. For reducing the invention to practice, it is possible to realize such a structure of forming the thin film conductor 11 only one side of the front and back surfaces of the core substrate 9a at a part or whole of the electronic part.

[0037] According to the present invention, in comparison with the conventional art in that copper foil is used, the thin film conductor of the present invention realizes to make electronic parts thin. Specifically, when the conventional electronic part include eight layers of 18μm copper foil which is generally used as conductor pattern and seven resin layers as insulation layer each having 60μm thickness, the thickness of the electonic part is 564μm (60μm x 7 + 18μm x 8 = 564μm).

[0038] On the other hand, in the example of the invention, when the thin film conductor 11 has 3μm thickness, and the other conditions (thickness of the resin layer and numbers of resin layers and conductor layers) are the same, the thickness of the electronic part of the present invention is 444μm (60μm x 7 + 3μm x 8 = 444μm). Thus, according to the invention, the electronic part thinner 120μm than the conventional can be obtained.

[0039] Further, according to the conventional art, minimum conductor pattern width is about 50μm and minimum distance betweenpatterns is also about 50μm. On the other hand, according to the present invention, minimum conductor pattern width is about 10μm and minimum distance between patterns is also about 10μm. Thus, the conductor pattern can be fine and pattern accuracy also can be improved.

[0040] According to the invention, as the core substrate and the prepreg are separately formed, alternately laminated, and hardened at the same time to produce the electronic part, the production time is shortened and the cost-down can be attained. As the whole is once hardened by the hot pressing, crack or warp are hard to occur. By making the conductor thin, it is possible to make the patterns fine and parts thin, heighten patterning precision and accuracy in layer-to-layer, and avoid migration.

[0041] According to the invention, the thin film conductor is made less than 5 μm in thickness, so that the conductor thickness is not large, it is possible to avoid the time from becoming long.

Claims

1. An electronic part, comprising

a core substrate which is made by forming a resin or a compound material made by mixing powder-like functional material with a resin into a thin plate, and hardening it;

thin film conductor formed on at least one of front and back surfaces of the core substrate through a thin film forming technique and carried out with a patterning; and

adhesive layer formed with a resin or a compound material made by mixing powder-like functional material with a resin, and interposed between core substrates formed with the thin film conductor,

wherein laminated layers made of the core substrates and prepregs provided between the core substrates as the adhesive layers are unified by hot-pressing.

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2. The electronic part as claimed in claim 1, wherein the thin film conductor has thickness less than 5 μm.

3. The electronic part as claimed in claim 1, wherein said resin comprises at least one thermosetting resin selected from a group consisting of epoxy resin, phenol resin, unsaturated polyester resin, vinyl ester resin, polyimde resin, bismaleimidotriazine (cyanate ester) resin, polyphenyle ether (oxide) resin, fumarate resin, polybutadiene resin, and vinylbenzyl resin.

4. The electronic part as claimed in claim 1, wherein said resin comprises at least one thermoplastic resin selected from a group consisting of aromatic polyester resin, polyphenylene sulfide resin, polyethylene terephtharate resin, polybutylene terephtalate resin, polyethylene sulfide resin, polyethyl ehter ketone resin, polytetrafluoroethylene resin, polyarylate resin and graft resin.

5. The electronic part as claimed in claim 1, wherein said resin comprises composite resin composed of at least one of the thermosetting resin and at least one of the thermoplastic resin,

said thermosetting resin is selected from a group consisting of epoxy resin, phenol resin, unsaturated polyester resin, vinyl ester resin, polyimde resin, bismaleimidotriazine (cyanate ester) resin, polyphenyle ether (oxide) resin, fumarate resin, polybutadiene resin, and vinylbenzyl resin, and

said thermoplastic resin is selected from a group consisting of aromatic polyester resin, polyphenylene sulfide resin, polyethylene terephtharate resin, polybutylene terephtalate resin, polyethylene sulfide resin, polyethyl ehter ketone resin, polytetrafluoroethylene resin, polyarylate resin and graft resin.

6. The electronic part as claimed in claim 1, wherein said powder-like functional material comprises at least one ferrite magnetic material selected from a group consisting of Mn-Mg-Zn based magnetic material, Ni-Zn based magnetic material, and Mn-Zn based magnetic material.

7. The electronic part as claimed in claim 1, wherein said powder-like functional material comprises at least one ferromagnetic metallic magnetic material selected from a group consisting of carbonyl iron, iron-silicon based alloy, iron-aluminum-silicon based alloy, iron-nickel based alloy, and amorphous (iron based or cobalt based) alloy.

8. The electronic part as claimed in claim 1, wherein said powder-like functional material comprises at least one dielectric material selected from a group consisting of $BaO\text{-}TiO_2\text{-}Nd_2O_3$ based dielectric material, $BaO\text{-}TiO_2\text{-}SnO_2$ based dielectric material, PbO-CaO based dielectric material, TiO_2 based dielectric material, $BaTiO_3$ based dielectric material, $PbTiO_3$ based dielectric material, $SrTiO_3$ based dielectric material, $CaTiO_3$ based dielectric material, Al_2O_3 based dielectric material, $BiTiO_4$ based dielectric material, $MgTiO_3$ based dielectric material, $(Ba, Sr)TiO_3$ based dielectric material, $Ba(Ti, Zr)O_3$ based dielectric material, $BaTiO_3\text{-}SiO_2$ based dielectric material, $BaO\text{-}SiO_2$ based dielectric material, $CaWO_4$ based dielectric material, $Ba(Mg, Nb)O_3$ based dielectric material, $Ba(Mg, Ta)O_3$ based dielectric material, $Ba(Co, Mg, Nb)O_3$ based dielectric material, $Ba(Co, Mg, Ta)O_3$ based dielectric material, Mg_2SiO_4 based dielectric material, $ZnTiO_3$ based dielectric material, $SrZrO_3$ based dielectric material, $ZrTiO_4$ based dielectric material, $(Zr, Sn)TiO_4$ based dielectric material, $BaO\text{-}TiO_2\text{-}Sm_2O_3$ based dielectric material, $PbO\text{-}BaO\text{-}Nd_2O_3\text{-}TiO_2$ based dielectric material, $(Bi_2O_3, PbO)\text{-}BaO\text{-}TiO_2$ based dielectric material, $La_2Ti_2O_7$ based dielectric material, $Nd_2Ti_2O_7$ based dielectric material, $(Li, Sm)TiO_3$ based dielectric material, $Ba(Zn, Ta)O_3$ based dielectric material, $Ba(Zn, Nb)O_3$ based dielectric material and $Sr(Zn, Nb)O_3$ based dielectric material.

9. The electronic part as claimed in claim 1, wherein said powder-like functional material comprises composite functional material composed of at least two of mentioned ferrite magnetic materials, ferromagnetic metal lie magnetic materials, and dielectric materials,

said ferrite magnetic material is selected from a group consisting of Mn-Mg-Zn based magnetic material, Ni-Zn based magnetic material, and Mn-Zn based magnetic material,

ferromagnetic metallic magnetic material is selected from a group consisting of carbonyl iron, iron-silicon based alloy, iron-aluminum-silicon based alloy, iron-nickel based alloy, and amorphous (iron based or cobalt based) alloy, and

dielectric material selected from a group consisting of $BaO\text{-}TiO_2\text{-}Nd_2O_3$ based dielectric material, $BaO\text{-}TiO_2\text{-}SnO_2$ based dielectric material, PbO-CaO based dielectric material, TiO_2 based dielectric material, $BaTiO_3$ based dielectric material, $PbTiO_3$ based dielectric material, $SrTiO_3$ based dielectric material, $CaTiO_3$ based dielectric material, Al_2O_3 based dielectric material, $BiTiO_4$ based dielectric material, $MgTiO_3$ based dielectric material, $(Ba, Sr)TiO_3$ based dielectric material, $Ba(Ti, Zr)O_3$ based dielectric material, $BaTiO_3\text{-}SiO_2$ based dielectric material, $BaO\text{-}SiO_2$ based dielectric material, $CaWO_4$ based dielectric material, $Ba(Mg, Nb)O_3$ based dielectric material, $Ba(Mg, Ta)O_3$ based dielectric material, $Ba(Co, Mg, Nb)O_3$ based dielectric material, $Ba(Co, Mg, Ta)O_3$ based dielectric ma-

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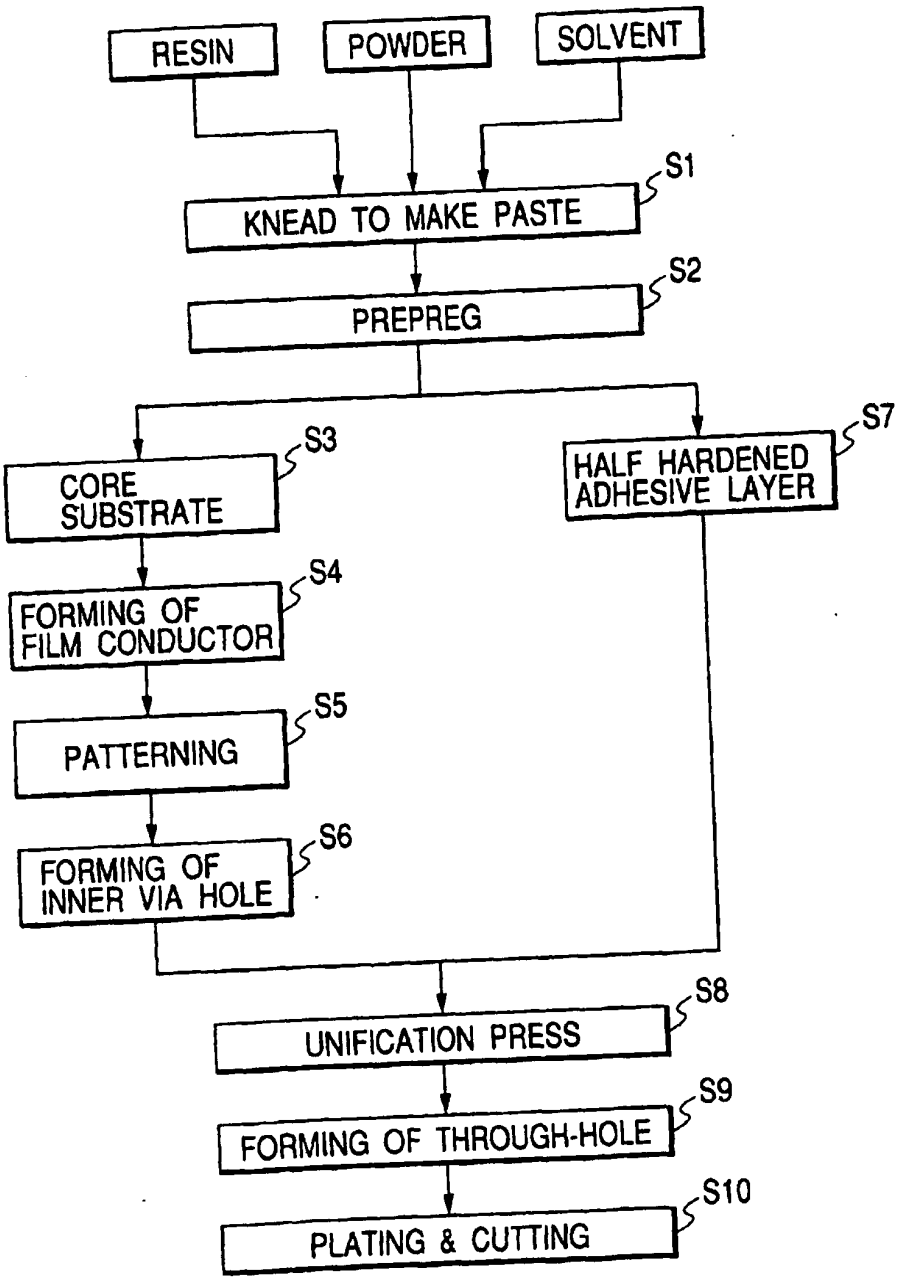
terial, Mg_2SiO_4 based dielectric material, $ZnTiO_3$ based dielectric material, $SrZrO_3$ based dielectric material, $ZrTiO_4$ based dielectric material, (Zr, Sn) TiO_4 based dielectric material, $BaO\text{-}TiO_2\text{-}Sm_2O_3$ based dielectric material, $PbO\text{-}BaO\text{-}Nd_2O_3\text{-}TiO_2$ based dielectric material, (Bi_2O_3, PbO)-$BaO\text{-}TiO_2$ based dielectric material, $La_2Ti_2O_7$ based dielectric material, $Nd_2Ti_2O_7$ based dielectric material, (Li, Sm) TiO_3 based dielectric material, Ba(Zn, Ta)O_3 based dielectric material, Ba (Zn, Nb) O_3 based dielectric material and Sr (Zn, Nb) O_3 based dielectric material.

10. A method of producing electronic parts, comprising the steps of:

forming a resin or a compound material made by mixing powder-like functional materials with said resin into thinpiates, and hardening it to be core substrate,
forming thin film conductors on at least one of front and back surfaces of the core substrates through any of an evaporation process, an ion plating process, an ion beam process, a vapor deposition process, and a sputtering process, followed by patterning,
forming the resin or the compound material made by mixing powder-like functional materials with the resin into prepreg like thin plates,
alternately laminating half-hardenedprepregs and the core substrates, and
subsequently hot-pressing and unifying into laminated parts.

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FIG. 1


RESIN
POWDER
SOLVENT
S1
KNEAD TO MAKE PASTE
S2
PREPREG
S3
CORE SUBSTRATE
S4
FORMING OF FILM CONDUCTOR
S5
PATTERNING
S6
FORMING OF INNER VIA HOLE
S7
HALF HARDENED ADHESIVE LAYER
S8
UNIFICATION PRESS
S9
FORMING OF THROUGH-HOLE
S10
PLATING & CUTTING

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FIG. 2A

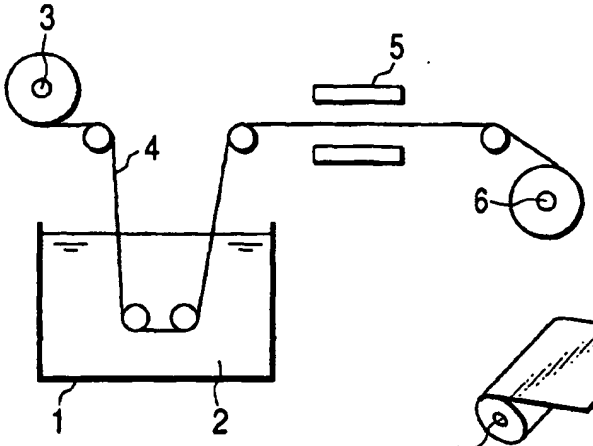


FIG. 2B

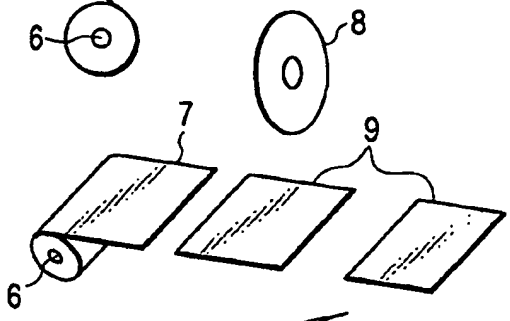


FIG. 2C

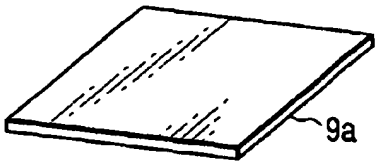


FIG. 2F

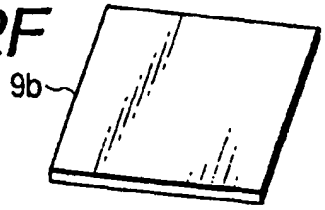


FIG. 2D

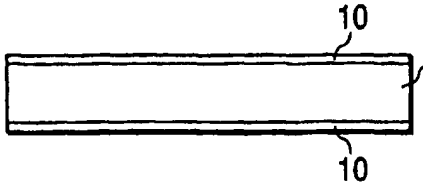
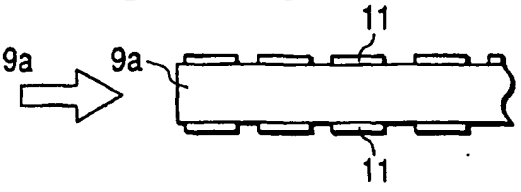


FIG. 2E



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FIG. 3A

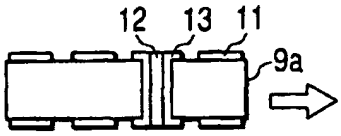


FIG. 3B

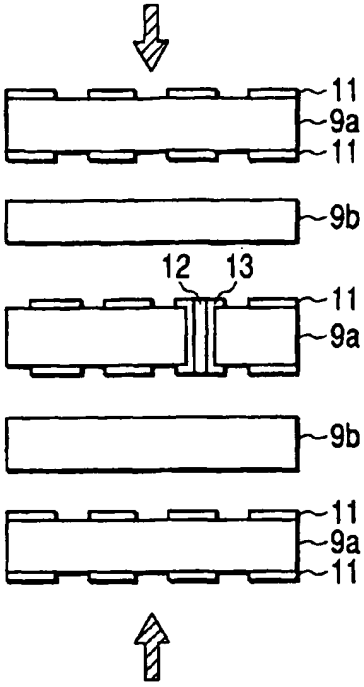


FIG. 3C

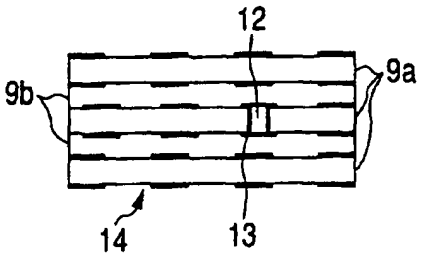


FIG. 3D

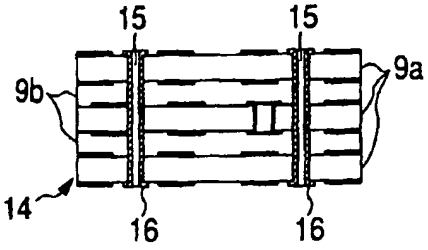
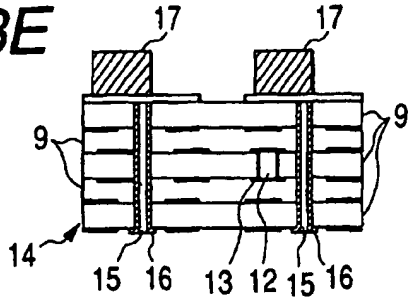


FIG. 3E



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FIG. 4A

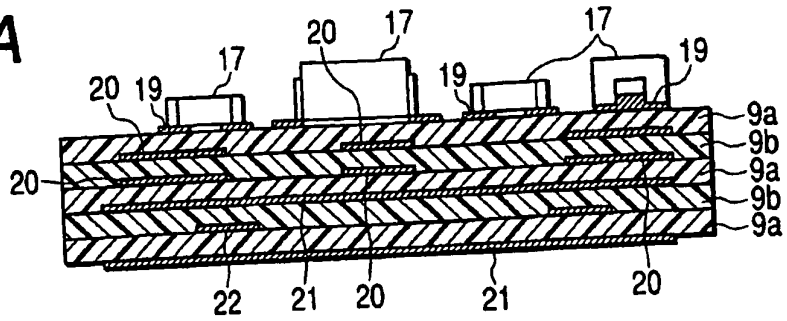
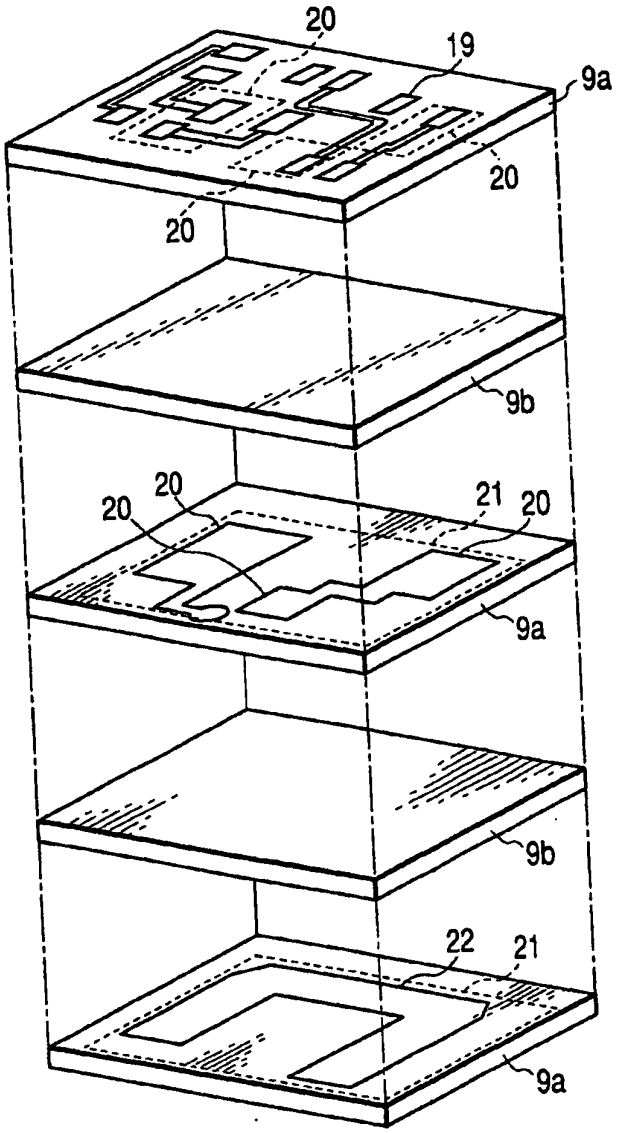
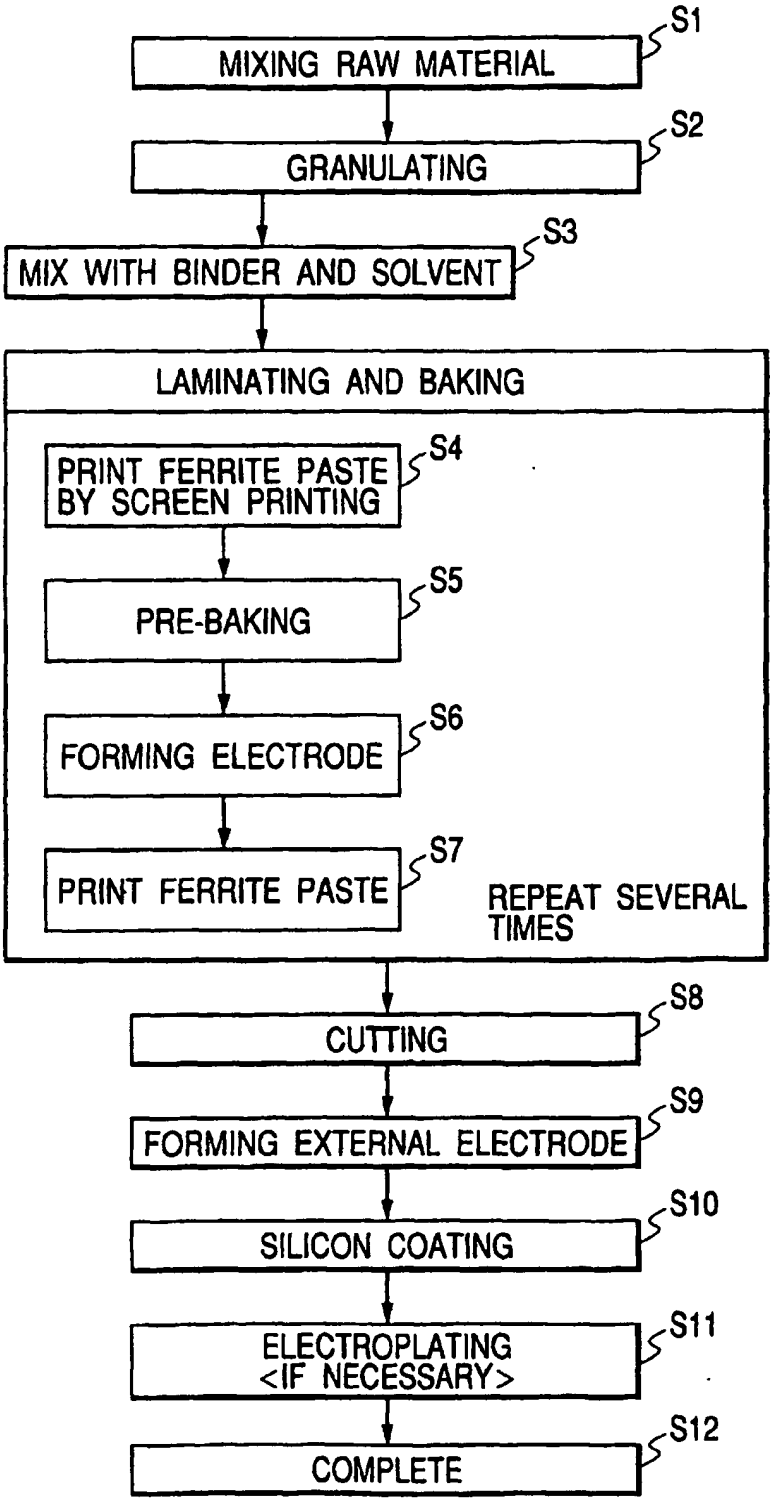


FIG. 4B



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FIG. 5



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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 00 4036

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X A	US 5 652 561 A (INOH KIYOHARU ET AL) 29 July 1997 (1997-07-29) * claims 1,6,12 * * column 1, line 62 - column 2, line 15 * * column 3, line 15 - line 32 * * figure 11 *	1,3,10 5	H01F41/04 H01F17/00 H01G4/30 H01G4/40
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A	EP 0 918 340 A (TDK CORP) 26 May 1999 (1999-05-26) * claims 1,2,4,5 * * paragraphs '0043!,'0064! * * paragraph '0077! * * paragraph '0088! *	1,3-7,9	
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H01F H01G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	24 May 2002	Stichauer, L

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
O : non-written disclosure
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
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& : member of the same patent family, corresponding document

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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 02 00 4036

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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24-05-2002

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(54) Method of manufacturing a multilayer circuit.

(57) In accordance with the present invention, a circuit assembly is manufactured in an additive process using at least one layer of a fluoropolymer composite material and a conductive material. The conductive layers are plated, and the fluoropolymer composite layers are laminated. The use of the filled fluoropolymeric composite eliminates the need for a barrier metal layer between the insulation and the conductors. A plurality of these circuit assemblies are stacked, one on top of the other. At least, selected exposed locations of the conductive material comprise a diffusible conductive material (e.g., gold). Once stacked the circuit assemblies are subjected to lamination under heat and pressure to simultaneously fuse adjacent fluoropolymer composite material and diffuse adjacent diffusible conductive material together to form an integral multilayer circuit having solid conductive interconnects.

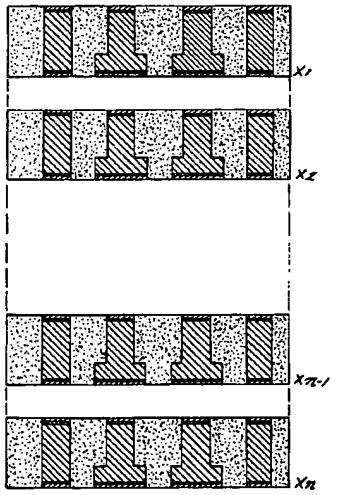


FIG. 12

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This invention relates generally to methods of manufacturing multilayer circuit boards and multichip modules, referred to collectively herein as circuits. More particularly, this invention relates to new and improved methods of manufacturing multilayer circuits wherein interconnections between multichip module assemblies (circuit assemblies) is accomplished in a single lamination step utilizing a fluoropolymer composite material and diffusible conductive material (e.g. a noble metal).

The need for and desirability of substrates for MCM's is well known in the electronic industry. The need for increased density in I/C packaging, increased interconnection capacity, and improved interconnection performance is well known among those involved in VLSI packaging and elsewhere in the electronics industry.

A multichip module can be viewed as a packaging technique in which several I/C chips, which may include complex microprocessor chips, memory chips, etc., are interconnected by a high density substrate. Although substrates for MCMs have been known in general for several years, these known prior art substrates for MCMs typically use thin film polyimide based material systems, and those systems have known deficiencies. Polyimide dielectric materials suffer from poor thermo-mechanical reliability and stability and electrical performance limitations. The polyimide materials usually are thermosetting, and have high elastic modulus, and there is a significant mismatch, i.e., difference, between the coefficient of thermal expansion (CTE) of the polyimide and the copper-conductors and/or other elements of the circuit structures. That all results in high stresses in the polyimide material and in surrounding materials and interfaces during thermal excursions in either or both the manufacturing process for or during use of the MCM substrate. Those stresses can lead to dimensional instabilities, cracking, delamination and other thermo-mechanically related problems. Also, the chemical bond between the polyimide and the copper conductors may be weak and is usually sensitive to the presence of water, thus leading to poor reliability of the copper-polyimide interface.

In some manufacturing processes for polyimide-based substrates for MCMs, a liquid form polyimide precursor is applied and then cured; in other processes, a sheet form polyimide prepreg is used. In either case, it is difficult to keep water out of the MCM substrate structure made with polyimides. Water is often generated during the polyimide cure, and the polyimide equilibrium water absorption is substantial, often in excess of 1%, and the rate of water uptake can be high. Also, water diffusion rates in polyimides are often high, so any water in a polyimide MCM substrate structure can diffuse quickly to the polyimide-conductor interface to corrode or otherwise degrade the interface. To combat this interface problem, a layer of metal, usually chromium is used as a barrier layer between the polyimide and the copper conductors. While this use of a barrier layer can be successful, it adds significant and expensive processing steps and costs to the manufacture of the MCM substrate structure.

Another point to note about polyimide based substrates for MCMs is that they are thin film structures. The layers of polyimide are typically in the range of 5 to 12 microns in thickness, with conductor line thickness in the range of 2 to 7 microns. Those relatively thin conductor lines mean relatively high resistance and relatively high loss; and both the nature of the polyimide material, per se, and the relatively thin layers used, result in poor electrical insulation characteristics.

Multilayer circuits are also well known and comprise a plurality of stacked substrate/circuit trace assemblies with interconnections between selected locations on the spaced circuit traces. Conventional manufacturing techniques for multilayer circuits generally do not yield multiple levels of interconnect, i.e. easy interconnection from one layer to any other layer without significant loss of density and/or major increases in processing costs. This limits the circuit density and the number of substrates. When multiple interconnect levels are required, step intensive sequential process techniques are usually utilized with much reduced yields.

U.S. Patent No. 4,788,766 attempts to overcome these problems. This prior patent discloses a method wherein a multilayer assembly is made up of a number of individual circuit boards and each board has a substrate on which a first conductive layer is formed on one surface while a second conductive layer is formed on the opposite surface. The substrate is a dielectric material which insulates the conductive layers. Via holes are formed through the first conductive layer, the substrate and the second conductive layer at various locations. An outer conductive material, such as copper, is applied over the first and second conductive layers and onto the side walls of the holes. A conductive bonding material is then deposited onto the outer conductive material in the area around the holes. Once the individual boards have been fabricated, they are stacked in a predetermined order and orientation with a suitable low temperature dielectric bonding ply (meaning that the bonding ply has a lower softening temperature than the circuit substrate material) positioned between each pair of layers. The dielectric bonding ply requires registered apertures therethrough which correspond to areas where the conductive layer of one substrate

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is to make an electrically conductive connection with the conductive layer of an adjacent substrate. Thus, the dielectric bonding ply integrally bonds adjacent boards together while providing electrical isolation and/or electrical connections between conductive layers of different boards. The assembly of the boards is then subjected to a cycle of heat and pressure to effect a bond between the various board layers.

While the method of U.S. Patent No. 4,788,766 overcomes some of the problems in the prior art, this prior method has certain disadvantages including the requirement for a substrate which has a melting temperature above the melting temperature of the bonding ply. In other words, the prior patent necessitates the use of a low temperature bond ply which limits the thermal rating of the multi-layer circuit. In addition, this prior method necessitates registered apertures in the bonding ply (leading to alignment problems) and is limited to multilayer circuits having plated through holes.

U.S. Patent No. 5,046,238 attempts to overcome these problems. This prior patent discloses a method wherein a plurality of circuit layers comprised of a dielectric substrate having a circuit formed thereon are stacked, one on top of the other. The dielectric substrate is composed of a polymeric material capable of undergoing fusion bonding such as a fluoropolymeric based substrate. Fusible conductive bonding material (e.g., solder) is applied on selected exposed circuit traces (prior to the stacking step) whereupon the entire stack is subjected to lamination under heat and pressure to simultaneously fuse all of the substrate and conductive layers together to form an integral multilayer circuit having solid conductive interconnects.

In the first embodiment of U.S. Patent No. 5,046,238, the discrete circuit layers are each prepared by (1) forming traces and pads on a removable mandrel; (2) laminating a layer of dielectric to the circuit and mandrel; (3) forming an access opening at selected locations through the dielectric layer (using laser, plasma, ion etch or mechanical drilling techniques) to expose selected circuit locations; (4) forming conductive posts in the access openings to a level below the top of the access openings; and (5) providing a fusible conductive material in the access opening. Thereafter, a stack-up is made of a plurality of these discrete circuit layers so that the exposed fusible conductive material contacts selected locations on an adjacent circuit. This stack-up is then subjected to heat and pressure to simultaneously fuse both the several layers of dielectric substrate and fusible conductive material to provide a cohesive fused multilayer circuit board.

In the second embodiment of U.S. Patent No. 5,046,238, at least one discrete circuit board is made using any suitable technique to define a fusible dielectric substrate having a circuit pattern thereon. Next, a layer of fusible dielectric material having openings through selected locations is placed on the circuit board so that selected locations on the circuit pattern are exposed. Thereafter, a plug of fusible conductive material (e.g., solder) is placed in the openings (using manual, mechanical or like techniques). Next, a second circuit board is stacked on the first board so that the plugs of fusible conductive material align with and contact selected locations on the circuit pattern of the second circuit board. This stack-up is then subjected to heat and pressure to simultaneously fuse both the layers of fusible dielectric and the fusible conductive material to provide a cohesive fused multilayer circuit board.

While the method of U.S. Patent No. 5,046,238 overcomes some of the problems in the prior art, this prior art method has certain disadvantages including problems commonly encountered with spreading of the solder mass during lamination, and evolution of the flux medium necessary to deoxidize the solder. Further, spreading of the solder mass is dependent on the low viscosity of the solder, the amount of solder and the proximity of other circuit features. Also, it is difficult to evolve all of the flux compound from the internal layers of the printed circuit board thereby presenting a potential long-term reliability problem from residual organics. With continued microminiaturization of circuit features, it was desired to produce circuit boards with feature sizes smaller than that possible using solder.

Temperatures and pressures used for practical solid state bonding processes are typically well in excess of 300 °C and 69 bar (1000 psi) . Therefore, it is necessary for any dielectric material used to be stable at temperatures above 300 °C. It will be appreciated that thermoplastic materials are generally not useful for fabricating very dense circuits with these harsh bonding conditions.

Fluoropolymers dielectric materials are often used for high frequency applications (>1 GHz) due to their low loss and tight dielectric constant control. Fluoropolymers such as polytetrafluoroethylene (PTFE), a copolymer of tetrafluorethylene and perfluoroalkyl vinyl ether (PFA) and a copolymer of hexafluoropropylene and tetrafluoroethylene (FEP) are also excellent circuit substrates due to their good thermal stability up to 400 °C and their good self-adhesion characteristics above their melt point. However, these materials generally have poor creep characteristics and yield poor dimensional stability when circuitized.

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To register dense circuit features (traces <150 μm and vias <200 μm), it is essential that the dielectric material be dimensionally stable. This requires the tailoring of x-y thermal expansion to closely match the metallurgy (in most cases copper) of the circuit features. This must be accomplished without jeopardizing dielectric self-adhesion characteristics, adhesion to conductors or producing unacceptably high porosity.

Thermal compression bonding processes can be practiced at relatively low, temperatures and moderate pressures as described in U.S. Patent No. 3,923,231. However, the time required for bonding is extremely long (22-30 days) so these processes are generally not practical for printed circuit board or multichip module applications. To yield practical bonding times (< 5 hour soak times), it is necessary to use relatively high temperatures (>300°C) and pressures (>69 bar (1000 psi)). U.S. Patent No. 4,874,721 describes a gold bonding process with pressures of about 2 kg/mm^2 (193 bar (2800 psi)) and 400°C in 1 hour.

With fluoropolymers, these high temperatures and pressures can produce flow which distorts circuits and produces severe misregistration of individual circuit layers. This problem increases greatly as the density of circuit features increases. It is an object of the present invention to overcome or alleviate at least some of the problems of the prior art. According to the present invention, a method of forming a multilayer circuit is proposed which comprises the steps of:

providing at least one first circuit assembly formed by the steps of,

(1) selecting a planar platform having opposed mutually parallel surfaces,

(2) forming first sites for a first part of a conductive circuit on a first of said surfaces of said platform,

(3) plating in said first sites to form said first part of said conductive circuit in said first sites,

(4) forming second sites for a second part of said conductive circuit on selected locations of said first part of said conductive circuit,

(5) plating in said second sites to form said second part of said conductive circuit in said second sites,

(6) laminating a layer of filled fluoropolymeric composite material onto said conductive circuit to define a laminated conductive circuit,

(7) planarizing said laminated conductive circuit to expose selected locations of said conductive circuit and define a planarized surface, and

wherein conductive circuit includes a layer of a diffusible conductive material on at least one selected location thereof;

providing at least one second circuit assembly comprising a substrate of fusible dielectric material and a conductive circuit formed thereon and wherein said conductive circuit includes a layer of a diffusible conductive material on at least one selected location thereof;

stacking said at least one first and at least one second assemblies one on top of the other so that said at least one selected location of diffusible conductive material of said at least one first assembly aligns with said at least one selected location of diffusible conductive material of said at least one second assembly; and

laminating said stacked assemblies under heat and pressure effective to both fuse said filled fluoropolymeric composite material with said fusible dielectric material and diffuse said diffusible conductive material so as to form a cohesive multilayer substrate having a solid conductive interconnect between said first and second assemblies, said solid conductive interconnect being defined by said diffusible conductive material.

A circuit assembly is manufactured in an additive process using at least one layer of a fluoropolymer composite material and a conductive material. The conductive layers are plated, and the fluoropolymer composite layers are laminated. The use of the filled fluoropolymer composite eliminates the need for a barrier layer between the insulation and the conductors.

A plurality of these circuit assemblies are stacked, one on top of the other. A diffusible conductive material (e.g., nobel metal) is applied at lead lines (or circuit traces) and vias wherever electrical connections are desired. Once stacked the circuits are subjected to lamination under heat and pressure to fuse adjacent fluoropolymer composite material and diffuse adjacent diffusible conductive material together to form an integral multilayer circuit having solid conductive interconnects. It may also be necessary, depending on conductive metal and noble metal combinations, to include a barrier metallization (i.e., nickel) to prevent diffusion of the conductive metal into the noble metal. Barrier metals are not required if both lead lines and vias are comprised of noble metal, as in the alternative embodiment.

The fluoropolymer composite dielectric material used in the MCM substrate of the present invention is preferably the material known as RO2800, available from Rogers Corporation, Rogers, Connecticut, the assignee of the present invention. That material is a thermoplastic polytetrafluoroethylene material with silane coated ceramic filler. That fluoropolymer material is set forth in more detail in commonly assigned U.S. Patent Nos. 4,849,284 and 5,061,548. The thermoplastic nature of the material combined with a high filler content (preferably greater than 50 vol. % and most preferably greater than 60 vol. %) imparts a

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high viscosity at the melt temperature. Therefore, the material can be repeatedly remelted without losing dimensional stability during sequential manufacturing steps. Also, the dielectric material has a low modulus of elasticity (7 - 8 Kbar (100 - 120 Kpsi)) and a low CTE, thus resulting in low stress both during the manufacturing process and in the use of the resulting structure. Also, the material is characterized by low moisture absorption on the order of less 0.13%.

Dimensional stability of fluoropolymers can be greatly improved by incorporating high volume fractions of ceramic powder to reduce the thermal expansion of the composite so that it approximates that of the conductor metallurgy. High filler loadings also reduce dielectric flow. This is an important feature for the high temperature and pressure bonding processes required for practical thermal compression bonding processes. However, adding excessive amounts of filler will significantly degrade dielectric bond strength and yield a porous composite with poor circuit processing characteristics. A narrow window of fluoropolymer composite filler contents has been identified which provides acceptable dimensional stability and self-adhesion for application of practical solid state diffusion processes.

Fused amorphous silica contents between 55 vol% and 70 vol% in PTFE have been found to yield good dimensional stability with copper or gold conductors. The precise filler content for good dimensional stability does vary somewhat with particle size distribution and filler.

Other features and advantages of the present invention will be understood by those skilled in the art from the following detailed description and drawings.

Referring now to the drawings, wherein like elements are numbered alike in the several FIGURES:

FIGURES 1 - 11 show various stages in the process of manufacture of a circuit assembly of the present invention;

FIGURE 12 is an exploded view depicting a stack-up of the circuit assemblies of the type shown in FIGURE 11; and

FIGURE 13 is a cross-sectional elevation view of a final multilayer circuit made in accordance with the method of the present invention.

It will be understood that FIGURES 1 through 13 show part of a circuit in its process of manufacture. In these drawings, only one, or a few, of each type of via, lead lines, and/or voltage and ground planes is shown for purposes of illustration. It will, however, be understood that the number and type of lead lines, vias and/or voltage and ground planes will be determined by the specific design and function of any particular circuit.

Referring to FIGURE 1, the process of the present invention starts with a flat platform 10 on which one or more layers of the MCM substrate (or circuit assembly) is to be built, and which may form a part of the finished MCM substrate structure. This process may be the same as described in U.S. Patent Application Serial No. 847,859 entitled Multichip Module Substrate and Method of Manufacture Thereof filed March 9, 1992, the entire contents of which are incorporated herein by reference. The copper surface of platform 10, on which the MCM substrate is to be built, must be as flat as possible. Platform 10 can be a copper sheet, preferably of 50,8 micron (2 mil) thick copper foil with parallel flat opposed top and bottom surfaces. The platform could also be other material that is dimensionally stable in the x (horizontally in the plane of the drawing paper), y (into the plane of the paper) and z (vertically along the plane of the paper) directions; is flat; has a CTE approximately equal to or slightly less than that of copper, and can be etched or otherwise removed (e.g. laser ablation) at the point in the process where the copper foil is etched off. Platform 10 could also be a flat, rigid ceramic element, either featureless or cofired. Such a platform would end up as the outer layer in the final multilayer structure. In this example, platform 10 comprises a 50,8 micron (2 mil) thick treated copper foil having flat and parallel top and bottom surfaces.

Both surfaces of the platform 10 are coated with a layer 12 of photoresist material, preferably a dry film photoresist 25,4 micron (1 mil) thick. The photoresist layer 12 on the upper treated surface of the platform 10 is imaged and developed to define via sites 14 and lead line sites 16 (in this example, the portion of the lead line site 16 shown is in the "Y" direction), see FIGURE 2. The photoresist layer 12 on the untreated bottom surface of the platform 10 is completely exposed (i.e., hardened) to form a protective layer during electroplating of the circuit features.

Next, referring to FIGURE 3, a thin layer 18 of nickel is plated on platform 10 in the via sites 14 and lead line sites 16. Then a layer 20 of a noble metal (e.g., gold) or other suitable diffusible conductive material is electroplated on the layer 18 of nickel. Layer 18 of nickel prevents the diffusion of the copper of platform 10 into the gold of layer 20. This diffusion would otherwise degrade the later bondability of the gold. Alternatively, a thin layer of nickel may be deposited on platform 10 prior to coating with photoresist material 12, and then gold only would be plated into the via sites 14 and lead line sites 16. This embodiment may be preferred since it will ensure a more planar surface when the copper platform 10 and nickel layer 18 are etched, as described hereinafter.

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Referring to FIGURE 4, the remaining thickness of the via sites 14 and lead line sites 16 are then electroplated with a layer 22 of copper, after plating another thin nickel (barrier) layer 24 on the gold layer 20. The copper plating of layer 22 is controlled so that the height of the plated features is equal to the height of the photoresist layer 12, see FIGURE 4. Care must be taken so that the electroplated features do not 'mushroom' over the top surface of the photoresist layer 12. Layers 18, 20, 24 and 22 in via sites 14 form vias 23 and in lead line sites 16 form lead lines 25.

Next, another layer 26 of 50,8- 76,2 micron (2-3 mil) photoresist is coated over the plated features (i.e., layer 22) and imaged and developed to produce via sites 28, see FIGURE 5. The bottoms of the via sites 28 are argon/oxygen plasma cleaned to ensure that the subsequent via plating will adhere well to the surfaces of the copper of layer 22 below them.

The via sites 28 are then plated up with a layer 30 of copper to form vias 31. The plating of copper layer 30 is controlled so that the tops of vias 31 are at or just below the top surface 33 of the photoresist layer 26. Again, care is taken so that the electroplated features (i.e., layer 30) do not mushroom over the surface of the photoresist, see FIGURE 6.

After the vias 31 have been formed (i.e., layer 30 has been plated up), all layers 26 and 12 of photoresist are removed to leave plated features 32 standing on the platform 10, see FIGURE 7. Plated features 32 comprise nickel layer 18, gold layer 20, nickel layer 24, and copper layers 22 and 30. Any residual photoresist is removed preferably using an argon/oxygen plasma etch. It will be appreciated that this plasma etching step is used through the method of the present invention to remove residual photoresist.

Next, referring to FIGURE 8, a layer 34 of a fluoropolymeric material (e.g. Rogers Corporation RO2800 fluoropolymer) is deposited on top of the vias and lead lines 32 and laminated thereto. Fluoropolymer layer 34 may be from 50,8-254 micron (2-10 mil) thick, preferably 127-254 (5-10 mil) thick. It will be appreciated that the thinner the final dielectric thickness after flycutting, described below, the thinner the dielectric thickness needed in lamination. The fluoropolymer material preferably has a thin (e.g., 25,4 micron (1 mil)) top layer 36 of copper which services as a release layer during lamination. The fluoropolymer layer 34 is laminated to platform 10, with plated features 32 by a heat and pressure lamination process. In this lamination process, release layer 36 prevents the fluoropolymer layer 34 from sticking to a press pad, which in turn, is in contact with the press plate. The lamination process densifies the fluoropolymer layer 34 in the z direction. However, the material is a highly filled and viscous polymer which does not flow laterally (x or y directions) under heat and pressure. Thus, the positioning and alignment of the vias and lead lines are not disturbed by lateral flow of the fluoropolymer of layer 34 during the lamination step.

The preferred process for effecting the lamination is as follows:

(a) Place the assembly (platform, vias, traces, fluoropolymer layer) in the press, close the press and apply a low pressure (about 7 bar (100 psi)) as heat is applied;
(b) ramp the temperature up to 371 • C (700 • F);
(c) increase the pressure to 117 bar (1700 psi);
(d) soak at 371 • C (700 • F) and 117 bar (1700 psi) for one hour;
(e) while maintaining 117 bar (1700 psi), reduce temperature to 204 • C (400 • F);
(f) at 204 • C (400 • F), reduce the pressure to 7 bar (100 psi);
(g) cool to below 38 • C (100 • F) (or room temperature) at to 7 bar (100 psi);
(h) remove the assembly from the press.

After the laminated subassembly (see, FIGURE 8) is removed from the press, copper release layer 36 is removed by etching. Platform 10 is protected from the etch during this etching step by, e.g., being coated with a photoresist which is removed after the etching step.

Next, the upper surface of the assembly is planarized by flycutting to (a) ensure general planarity (i.e., parallelism) with the upper surface of platform 10, and (b) to provide an upper surface 38 of the assembly where the vias 31 are exposed and are generally coplanar with each other and with the exposed upper surface 38 of laminated fluoropolymer layer 34, see FIGURE 9.

The flycutting is performed as described in U.S. Patent Application Serial No. 847,895. The subassembly is then removed from the flycutting machine and cleaned with a Freon or other degreasing material.

Next, a thin layer of barrier nickel 40 is plated on the exposed vias followed by the plating of another noble metal (e.g., gold) layer 42, see FIGURE 10. It will be appreciated that during the flycutting step the fluoropolymer layer 34 tends to compress, such that after flycutting the via heights are actually slightly recessed. Therefore, when layers 40 and 42 are added the end result is very close to a planar surface and in some instances the gold may exceed the height of the fluoropolymer layer by a very small amount. Prior to these platings (a) the tops of the vias 31 are plasma cleaned to remove any fluoropolymer debris produced during flycutting, and (b) the bottom surface of the platform 10 is again coated with a layer of photoresist (not shown) to prevent plating on the

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backside of the platform, which is removed after the gold plating and prior to the etching (i.e., removal) of the platform 10 in the next step.

The final step to produce the individual circuit layer is to etch off the copper platform 10 and the nickel layer 18 beneath it. The resulting circuit 44, shown in FIGURE 11, comprises fluoropolymeric dielectric layer 34 of a uniform thickness, with copper vias and lead lines 23, 25 and 31, the exposed surfaces of which are plated with fusible gold layers 20 and 42 (with nickel barrier layers 24 and 40, respectively) and are essentially flush with the surfaces of the dielectric layer 34. While circuit 44 has been described as a single layer circuit, the circuit may comprise more than one layer, as described in U.S. Patent Application Serial No. 847,895.

A variation of the preceding circuit fabrication process is one in which, after plating the thin layer 18 of barrier nickel, see FIGURE 3, the vias and lead lines are entirely built of a plated noble metal (e.g., gold), thereby eliminating all copper plating and subsequent nickel platings and the numerous metallic interfaces resulting from the multiple plating steps.

Turning now to FIGURE 12, a plurality of circuit layers which have been fabricated in accordance with the techniques shown in Figures 1 - 11 are stacked one on top of the other in the manner shown. Of course, any number (Xn) of circuits may be stacked and registered with one another such that selected areas of the noble metal layers from adjacent circuits align. Prior to stacking these circuit layers for lamination, all surfaces to be diffusion bonded are argon plasma cleaned.

After the circuits have been stacked up as shown in FIGURE 12, the stack up is subjected to lamination under sufficient heat (preferably less than 400°C) and pressure, as described in U.S. Patent Application Serial No. 939,105 entitled Method of Manufacturing a Multilayer Circuit Board filed September 1, 1992, so as to fuse adjacent dielectric material and diffuse adjacent noble metal and thereby provide an integral and cohesive multilayer circuit assembly 46, as shown in FIGURE 13 having solid conductive interconnects. By way of example, circuits were manufactured using the process of FIGURES 1 - 11 where: the diffusible conductive material was gold; the vias and traces were 50mm and 25mm wide, respectively; and the fluoropolymer was polytetrafluoroethylene (PTFE) filled with 60 volume percent 1mm fused amorphous silica. These circuits were stacked as described above, thereafter the adjacent gold layers were diffused and adjacent dielectric layers were fused at 370- and 117 bar (1700 psi) with a 1 hour soak time. This resulted in peel strengths which exceeded a 8 pli for both dielectric to dielectric and gold to gold bonds. Further, the 50mm vias were well registered to each other.

In another embodiment, individual circuit layers made in the heretofore described embodiment may be alternated in a stack with double sided, plated-through-hole printed circuits made from the copper clad R02800 dielectric by e.g. conventional, low cost subtractive printed circuit fabrication processes. The double sided circuits would, of course, have gold or other diffusible metallurgy on the outer surfaces where diffused conductive interconnects are to be made during the stack lamination. The stack lamination could be effected in the same manner as described earlier in U.S. Patent Application Serial No. 939,105.

Claims

1. A method of forming a multilayer circuit comprising the steps of:

providing at least one first circuit assembly formed by the steps of,

(1) selecting a planar platform having opposed mutually parallel surfaces,

(2) forming first sites for a first part of a conductive circuit on a first of said surfaces of said platform,

(3) plating in said first sites to form said first part of said conductive circuit in said first sites,

(4) forming second sites for a second part of said conductive circuit on selected locations of said first part of said conductive circuit,

(5) plating in said second sites to form said second part of said conductive circuit in said second sites,

(6) laminating a layer of filled fluoropolymeric composite material onto said conductive circuit to define a laminated conductive circuit,

(7) planarizing said laminated conductive circuit to expose selected locations of said conductive circuit and define a planarized surface, and

wherein conductive circuit includes a layer of a diffusible conductive material on at least one selected location thereof;

providing at least one second circuit assembly comprising a substrate of fusible dielectric material and a conductive circuit formed thereon and wherein said conductive circuit includes a layer of a diffusible conductive material on at least one selected location thereof;

stacking said at least one first and at least one second assemblies one on top of the other so that said at least one selected location of

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diffusible conductive material of said at least one first assembly aligns with said at least one selected location of diffusible conductive material of said at least one second assembly; and

laminating said stacked assemblies under heat and pressure effective to both fuse said filled fluoropolymeric composite material with said fusible dielectric material and diffuse said diffusible conductive material so as to form a cohesive multi layer substrate having a solid conductive interconnect between said first and second assemblies, said solid conductive interconnect being defined by said diffusible conductive material.

2. The method of claim 1 characterized in that said steps of forming said first and second sites include the steps of:

selectively depositing photoresist material;

imaging said deposited photoresist material; and

developing said imaged photoresist material to define said sites.

3. The method according to claim 1 or 2 characterized in that said steps of plating said first and second parts of said conductive circuit include the step of:

controlling the height of the conductive circuit to be about the same as the height of the photoresist.

4. The method according to any of the claims 1 to 3 characterized in that said layer of filled fluoropolymeric composite material includes a thin release layer on a top surface thereof.

5. The method according to any of the claims 1 to 4 characterized in that said filled fluoropolymeric composite material comprises:

silane coated silica filled polytetrafluoroethylene.

6. The method according to any of the claims 1 to 5 characterized in that said step of laminating said layer of filled fluoropolymeric composite material comprises:

(a) at a low pressure, ramping of the laminating temperature up to about 371 °C (700 °F);

(b) increasing the pressure to 117 bar (1700 p.s.i.);

(c) soaking at about 371 °C (700 ° F) and 117 bar (1700 p.s.i.);

(d) reducing the temperature to about 204 °C (400 °F) while maintaining a pressure of 117 bar (1700 p.s.i.);

(e) reducing the pressure to about 7 bar (100 p.s.i.) while maintaining the temperature of 204 °C (400 °F); and

(f) cooling to below 38 °C (100 °F) at a pressure of about 7 bar (100 p.s.i.).

7. The method according to any of the claims 1 to 6 characterized in that said step of planarizing said laminated conductive circuit comprises:

a flycutting process.

8. The method of claim 7 characterized in that:

said flycutting process utilizes a diamond cutting tool operated at a positive rake angle.

9. The method of claim 8 characterized in that:

said positive rake angle is about 4 °.

10. The method according to any of the claims 1 to 8 characterized in that said diffusible conductive material comprises a noble metal.

11. The method of claim 10 characterized in that said noble metal comprises gold.

12. The method according to any of the claims 1 to 11 characterized in that said planar platform comprises:

a layer of copper; and

a layer of nickel deposited on said layer of copper.

13. The method according to any of the claims 1 to 12 characterized in that the step of forming said first and second assemblies further comprises the step of:

(8) removing said planar platform from said planarized laminated conductive circuit.

14. The method according to any of the claims 1 to 13 characterized in that said conductive circuit comprises diffusible conductive material.

15. The method of claim 14 characterized in that said diffusible conductive material comprises a noble metal.

16. The method of claim 15 characterized in that said noble metal comprises gold.

17. The method of claim 1 characterized in that:

said step of plating said first sites comprises,

plating a first layer of nickel on said planar platform within said first sites,

plating a layer of gold on said first layer of

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nickel,

plating a third layer of nickel on said second layer, and

plating a fourth layer of copper of said third layer;

said step of plating said second sites comprises,

plating a fifth layer of copper on said fourth layer within said second sites; and

said step of forming said first and second assemblies further comprises the step of,

plating a sixth layer of nickel on said fifth layer after planarizing said laminated conductive circuit, and

plating a seventh layer of gold on said sixth layer.

18. The method of claim 1 characterized in that said step of laminating said stacked assemblies under heat and pressure comprises a heat of less than 400 • C.

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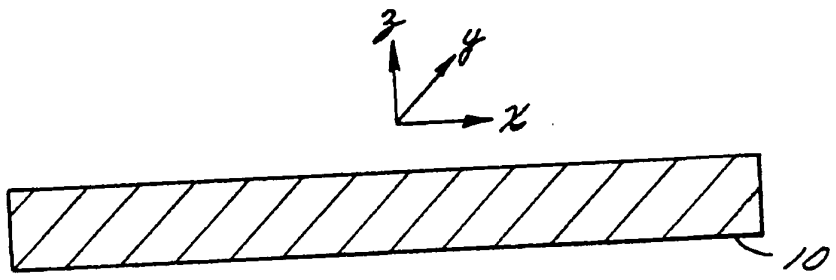


FIG. 1

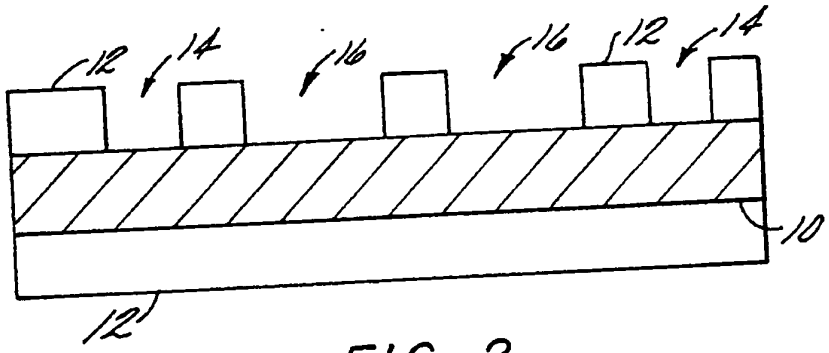


FIG. 2

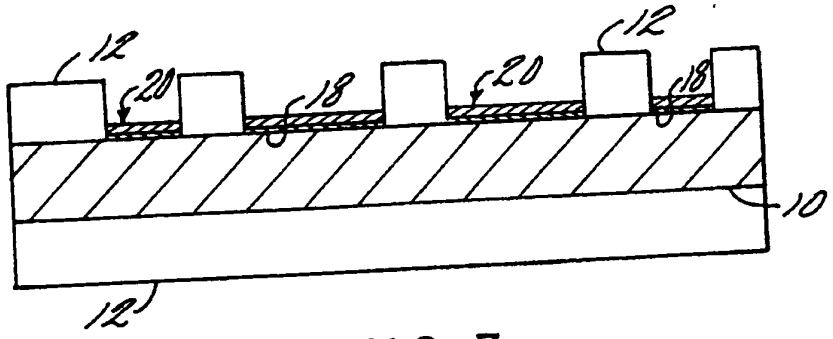


FIG. 3

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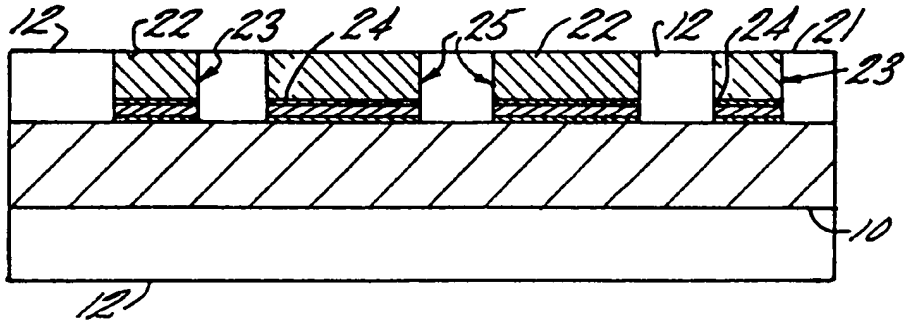


FIG. 4

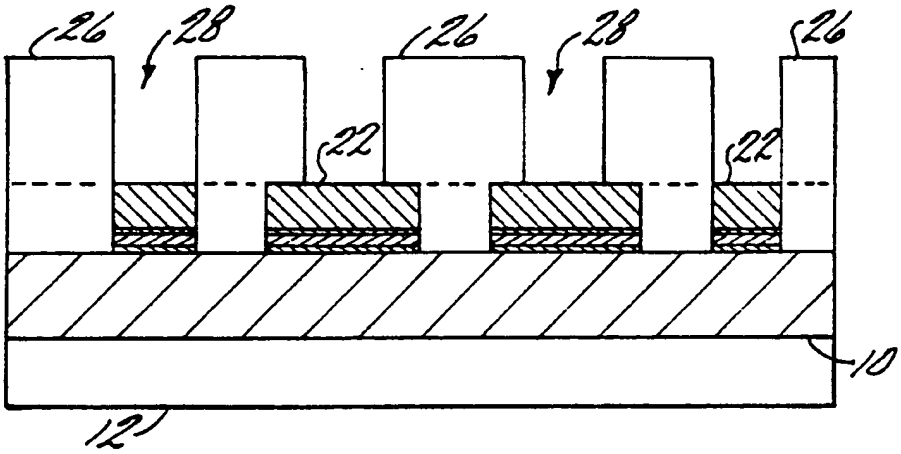


FIG. 5

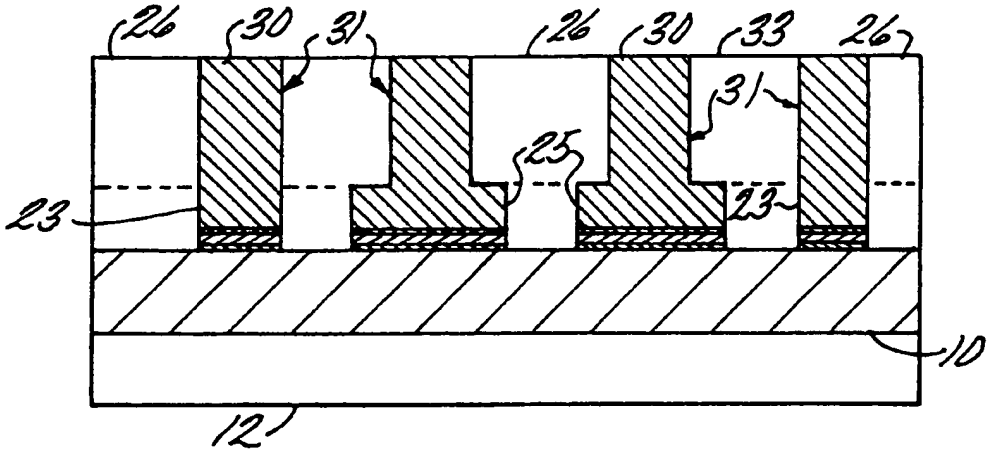


FIG. 6

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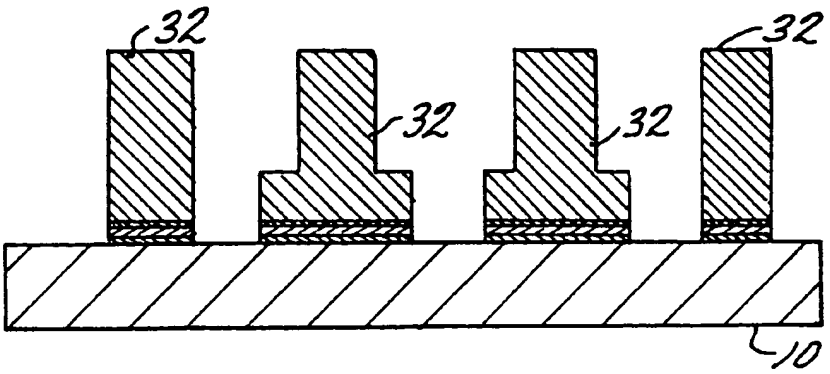


FIG. 7

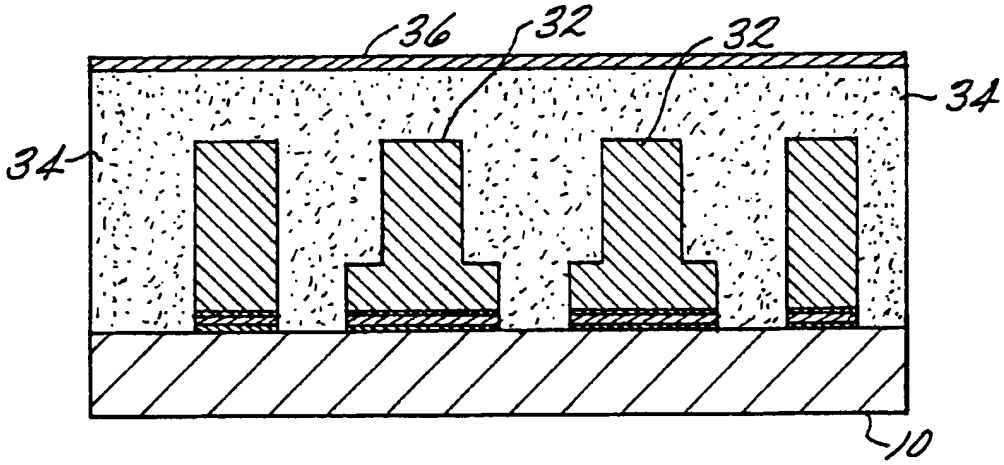


FIG. 8

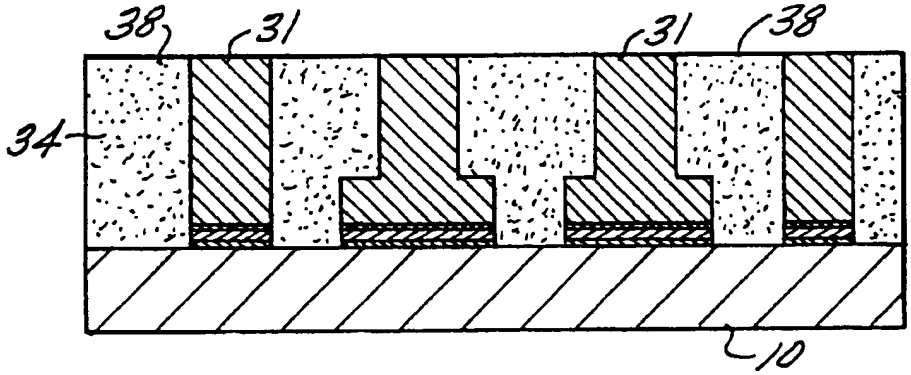


FIG. 9

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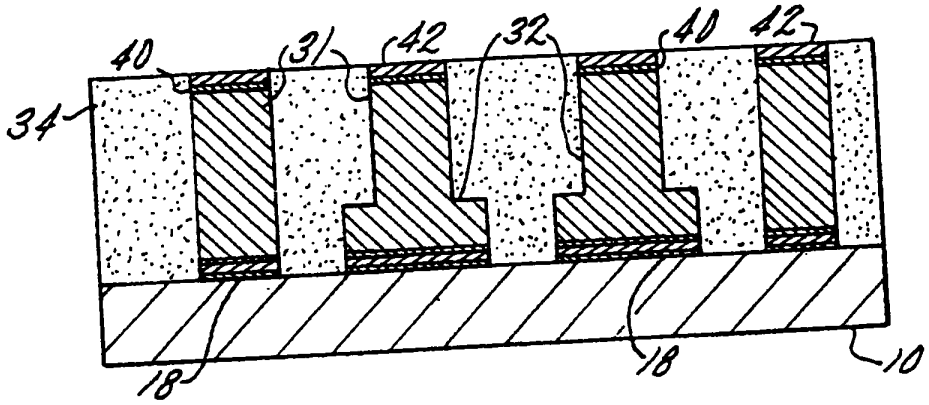


FIG. 10

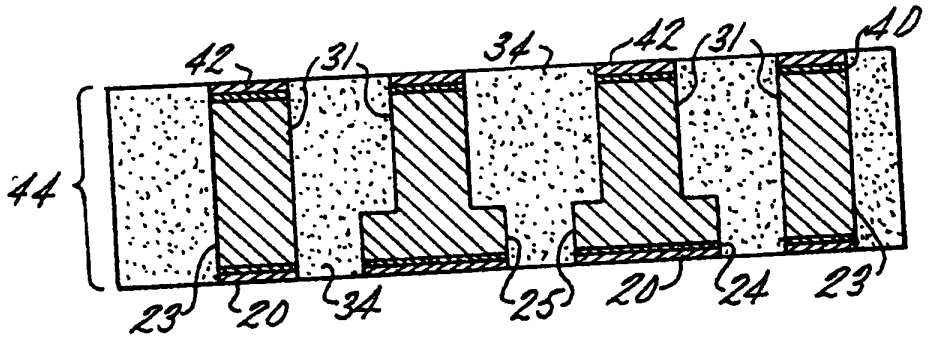


FIG. 11

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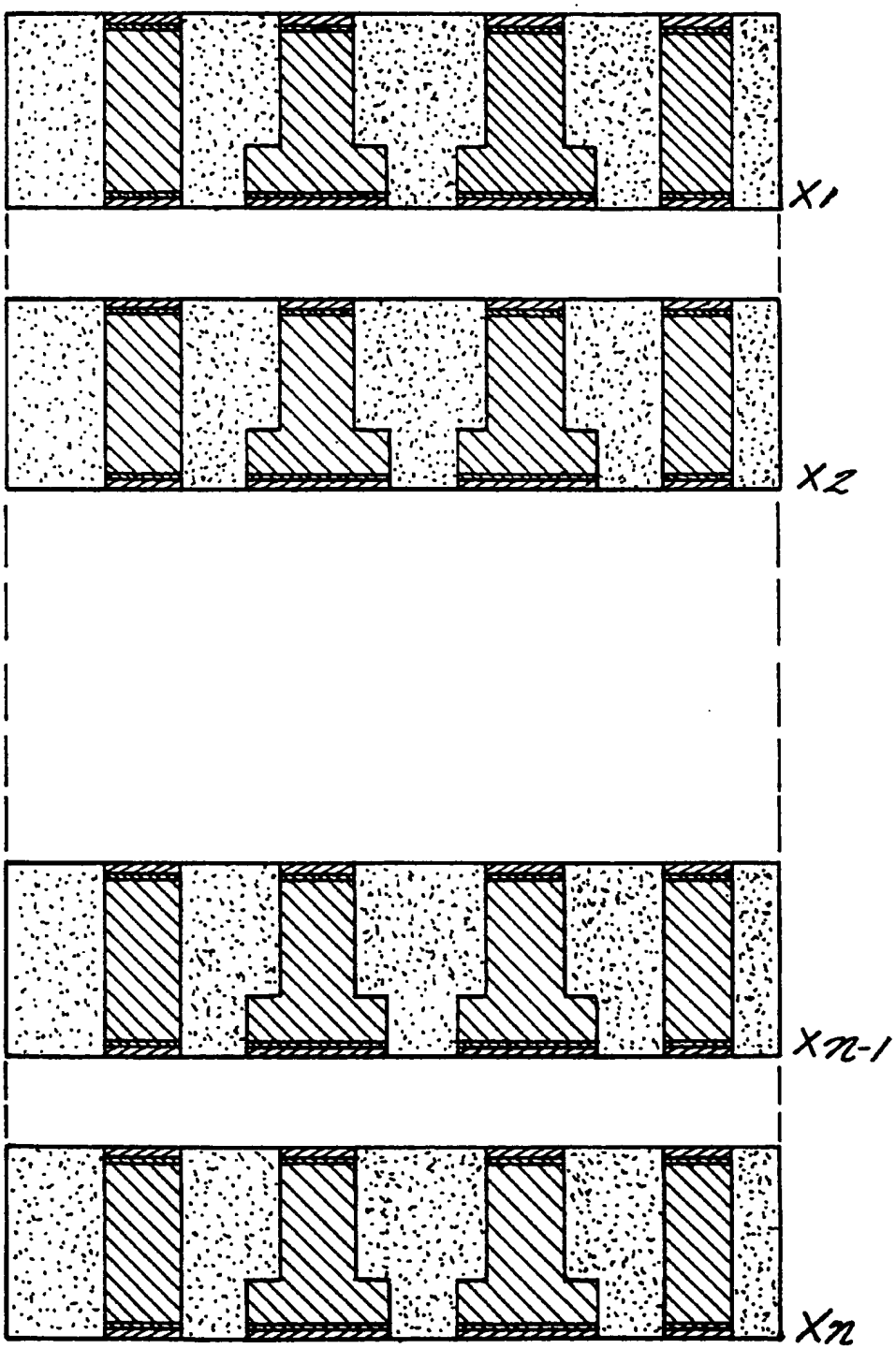


FIG. 12

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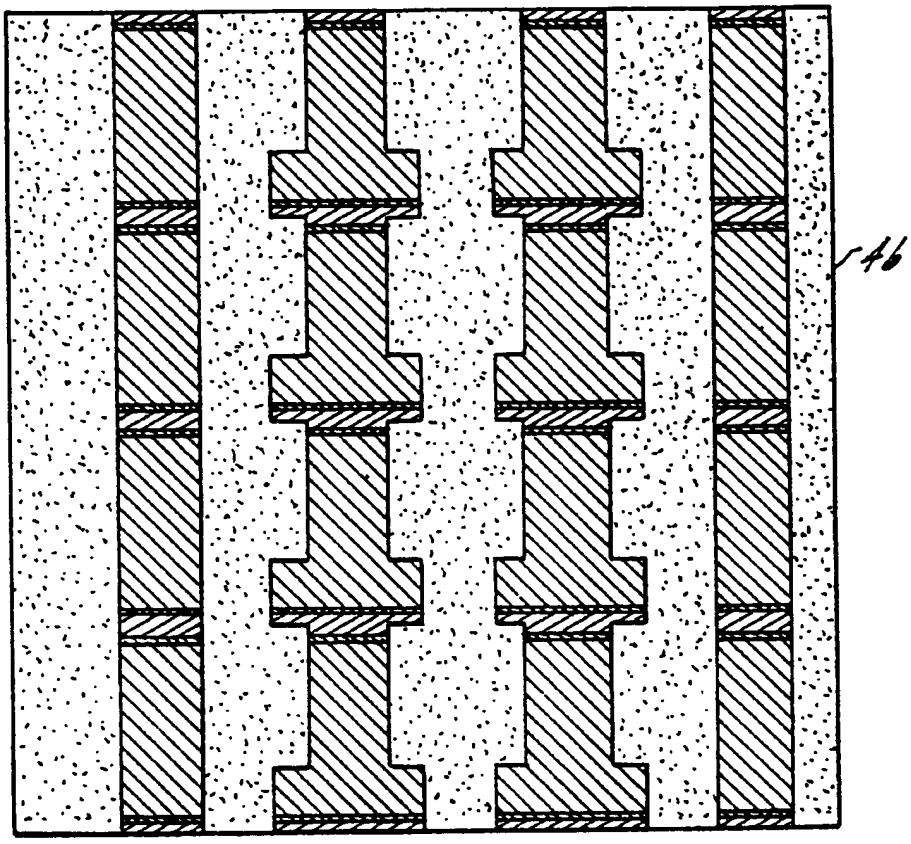


FIG. 13

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 11 4083

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	INTERNATIONAL JOURNAL OF MICROCIRCUITS AND ELECTRONIC PACKAGING, vol.16, no.2, Second Quarter 1993, RESTON VA US pages 109 - 116, XP000349287 G.S. SWEI ET AL. 'Ultra thin fluoropolymer dielectrics for MCM-L' * page 110 - page 112 *	1-3, 10-16,18	H05K3/46 H01L21/48
Y		4-9	
D,A	EP-A-0 560 077 (ROGERS CORP.) * column 5, line 19 - column 7, line 45 *	1-3	
Y		4-9	
A	EP-A-0 446 656 (ROGERS CORP.) * claims; figures * & US-A-5 046 238 (DAIGLE ET AL.)	1,12,13, 18	
A	GB-A-2 049 297 (PACTEL CORP.) * figures 1-5 *	1-3, 10-12, 14-16	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H05K H01L
A	US-A-4 685 210 (KING ET AL.) * claims *	10,11, 14-16	
A	IBM TECHNICAL DISCLOSURE BULLETIN., vol.11, no.12, May 1969, NEW YORK US pages 1676 - 1677 K.F. GREENE 'Producing printed circuit boards' * the whole document *	1,2,12, 13	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	2 January 1995	Mes, L

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
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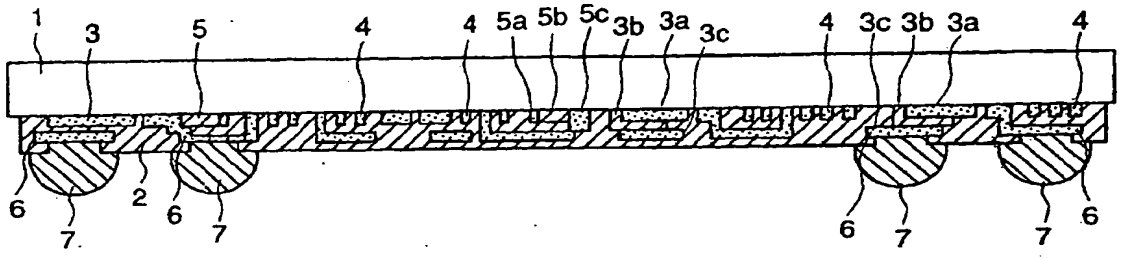
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Maximilianstrasse 54
80538 München (DE)

(54) ELECTRONIC CIRCUIT COMPONENT

(57) Through an improvement of module size increase due to mounting a single passive element on a substrate and an increase in the mounting cost, to provide a highly reliable, high performance and small sized electronic circuit component which permits to integrate a variety of electronic parts such as capacitors, inductors and resistors in a high density with low cost.

The electronic circuit component comprises an insulator substrate, a plurality of electrodes having different areas provided on the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a metal wiring connecting the elements, a metal terminal part of a part of the metal wiring and an organic insulator material covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion.

FIG. 1



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Description

FIELD OF THE INVENTION

[0001] The present invention relates to an electronic part and the manufacturing method thereof, in particular, relates to a technology which is effective when being applied to an electronic part using glass for the substrate and a manufacturing method therefore.

BACKGROUND ART

[0002] JP-A-8-255981 discloses a technology in which, by using an exposing process for a photo sensitive material with ultraviolet light, microscopic via holes and wirings are formed on a glass substrate. In the document, through forming a light shielding film of a metal constituting of such as Ti, Cr, Al, Ni, W, Mo, Ta and Cu on the glass substrate, multiple reflection of ultraviolet between the upper and lower faces of the glass substrate is prevented at the time of the exposing process of the photo sensitive material. Further, through forming the film thickness of the light shielding film constituted by one of the above metals more than 3μm, the heat conductivity of the glass substrate is enhanced.

[0003] JP-A-9-321184 discloses a connection substrate for connecting a semiconductor chip having a high wiring density with a printed wire substrate having a low wiring density and manufacturing method thereof. The connection substrate is constituted by a photosensitive glass substrate and on the upper face thereof one layer wiring is formed to which a bump for the chip is connected. Further, on the lower face of the substrate a plurality of bumps are formed, which are connected to electrodes on the printed wire substrate. The wirings on the upper face of the substrate and the bump on the lower face are electrically connected through holes penetrating between the upper and lower faces of the substrate. These penetrating holes are formed through a photolithography and the insides thereof conductors are buried through plating.

[0004] JP-A-2000-124358 discloses a technology of a high frequency integrated circuit mounting an active element in which an MIM type capacitor, a spiral inductor, a thin film resistor and metal wirings for connecting these are arranged on a silicon substrate and further, a flip chip is mounted thereon. Further, the claims thereof cover the use of a glass substrate, although the details thereof and the advantages thereof are not disclosed.

[0005] JP-A-10-284694 discloses a technology of constituting an electronic circuit on a poly crystal silicon substrate having a resistivity of more than 200 Q cm.

[0006] As the wiring substrate for mounting an electronic parts, one in which Cu wirings are formed on a resin substrate constituted such as epoxy resin containing glass fibers (glass epoxy) and polyimide resin or one in which W wirings are formed on a ceramics substrate such as AIN and SiC are broadly used.

[0007] However the warp and size variation of the wiring materials such as the resin and the ceramics are large in comparison with those of silicon substrate which is used in the manufacture of the semiconductor integrated circuits and the formation of microscopic wirings and through holes of the order of μm by using a photolithography is impossible, therefore, it was difficult to mount the electronic parts in high density.

[0008] On the other hand, as the wiring substrate for mounting electronics parts, the general use property of the silicon substrate, which is suitable for forming the microscopic wirings is low in comparison with such as the glass epoxy substrate, and it's usage is limited. Further, since the single crystal silicon substrate is a semiconductor, the substrate operates to reduce the efficiency of the electronic parts such as a capacitor and inductor formed thereon. On the other hand, the poly crystal silicon substrate can prevent in some extent the efficiency reduction, however, the poly crystal silicon substrate is more expensive than the single crystal silicon and the general use property thereof as the wiring substrate for mounting electronic parts is low and the usage thereof is limited.

[0009] Since the glass shows characteristics that the warp and the size variation are small in comparison with such as the resin and ceramics and the cost thereof is inexpensive in comparison with the silicon, it is considered that glass is a suitable substrate material for mounting electronic parts in high density. Further, the glass substrate is a desirable insulator, therefore the elements such as the inductors formed thereon show a high efficiency.

[0010] However, since the heat conductivity of the ordinal glass substrate as disclosed on JP-A-2000-124358 is low and is likely broken, such as cracks and damages are frequently caused due to difference of the thermal expansion coefficients between the glass substrate and other materials (Si), as a result, yield thereof reduces and the reliability thereof also reduces.

[0011] Further, in order to mount electronic parts on the glass substrate in high density as well as to use the glass substrate in a broad usage, it is necessary to lead out electrodes to be used as external connection terminals from t he back face of the substrate (opposite side face from the mounting face of the electronic parts) as being practiced in the wiring substrate of such as resin and ceramics.

[0012] In order to lead out the external connection terminals from the back face of the substrate, it is necessary to form through holes in the glass substrate in high accuracy, however, if a special photosensitive glass as, for example, disclosed in JP-A-9-321184 is used, the manufacturing cost of the substrate increases and it's usage is limited as the substrate for mounting the electronic parts.

[0013] Further, as disclosed in JP-A-2000-124358 when all of the variety of the electronic parts such as the capacitor, inductor and resistor are arranged on the sub-

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strate, the size of the integrated electronic parts become comparatively large.

[0014] Further, in the above document, since the respective constituting elements formed on the glass substrate are structured to be exposed at the end face of the substrate, when a large mechanical stress is applied at the interface regions of the respective layers constituting the electronic circuit component at the time of cutting out such as by dicing from the glass substrate larger than the electronic part, and when a large thermal stress is applied at the interfaces of the respective layers in connection with sudden temperature variation caused at the time of mounting the electronic circuit component, these stresses are concentratedly applied on the substrate exposed at the end faces of the electronic circuit component and the interface regions of the respective layers, thereby, the interface regions of the respective layers may be peeled off and the electronic circuit component may be damaged.

[0015] Accordingly, these already known electronic circuit components do not necessarily show a high reliability, in addition, it was not necessarily easy to obtain a high manufacturing yield.

[0016] An object of the present invention is to provide an electronic circuit component, which integrates a variety of electronic parts such as a capacitor, inductor and resistor in a high performance and in a high density.

DISCLOSURE OF THE INVENTION

[0017] In order to achieve the above object, an electronic circuit component comprises an insulator substrate, a plurality of electrodes having different areas provided on the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a metal wiring connecting the elemen ts, a metal terminal part of a part of the metal wiring and an organic insulator material covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion, with the above provision an electronic circuit component, which shows a desirable manufacturing yield and permits to integrate in a high density a variety of electronic parts such as the capacitor, inductor and resistor can be obtained.

[0018] Further, in order to achieve the above object, an electronic circuit component comprises an insulator substrate, a plurality of electrodes provided on the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a connecting portion provide at portions other than end portions of the electrodes, a metal wiring connecting the elements and the connecting portion, a metal terminal part of a part of the metal wiring and an organic insulator material covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion, with the above provision a n electronic circuit component , which shows a desirable manufacturing yield and permits to integrate in a high density a variety of electronic parts such as the capacitor, inductor and resistor can be obtained.

[0019] Further, in order to achieve the above object, an electronic circuit component comprises an insulator substrate, a plurality of electrodes provided on the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a metal wiring connecting the elements, a metal terminal part of a part of the metal wiring and being arranged in a grid shape and an organic insulator material covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion, with the above provision an electronic circuit component, which shows a desirable manufacturing yield and permits to integrate in a high density a variety of electronic parts such as the capacitor, inductor and resistor can be obtained and to ease connection with other parts such as a connection substrate.

[0020] Further, in order to achieve the above object, an electronic circuit component comprises an insulator substrate, a plurality of electrodes provided on the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a metal wiring connecting the elements, a metal terminal part of a part of the metal wiring and a plurality of organic insulator materials covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion, with the above provision an electronic circuit component, which shows a desirable manufacturing yield and permits to integrate in a high density and in a high performance a variety of electronic parts such as the capacitor, inductor and resistor through selection of the organic insulator materials suitable for the necessary high frequency characteristics of the respective elements can be obtained.

[0021] In order to achieve the above object, an electronic circuit component comprises an insulator substrate at predetermined position of which through holes are provided, a plurality of electrodes having different areas provided on both faces of the main face and the sub-main face or one of the faces of the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a metal wiring connecting the elements, a conductor portions formed inside the through holes for electrically connecting the metal wiring, a metal terminal part of a part of the metal wiring and an organic insulator material covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion, with the above provision an electronic circuit component , which shows a desirable manufacturing yield and permits to integrate in a high density a variety of electronic

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parts such as the capacitor, inductor and resistor can be obtained.

[0022] In order to achieve the above object, an electronic circuit component comprises an insulator substrate at predetermined position of which through holes are provided, a plurality of electrodes having different areas provided on both faces of the main face and the sub-main face or one of the faces of the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, connecting portions provided at portions other than end portions of the electrodes, a metal wiring connecting the elements and the connecting portions, a conductor portions formed inside the through holes for electrically connecting the metal wiring, a metal terminal part of a part of the metal wiring and an organic insulator material covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion, with the above provision an electronic circuit component , which shows a desirable manufacturing yield and permits to integrate in a high density a variety of electronic parts such as the capacitor, inductor and resistor can be obtained.

[0023] In order to achieve the above object, an electronic circuit component comprises an insulator substrate at predetermined position of which through holes are provided, a plurality of electrodes having different areas provided on both faces of the main face and the sub-main face or one of the faces of the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a metal wiring connecting the elements, a conductor portions formed inside the through holes for electrically connecting the metal wiring, a metal terminal part of a part of the metal wiring and being arranged in a grid shape and an organic insulator material covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion, with the above provision an electronic circuit component, which shows a desirable manufacturing yield and permits to integrate in a high density a variety of electronic parts such as the capacitor, inductor and resistor and to ease connection with other parts such as a connection substrate can be obtained.

[0024] Further, in order to achieve the above object, an electronic circuit component comprises an insulator substrate at predetermined position of which through holes are provided, a plurality of electrodes provided on both faces of the main face and the sub-main face or one of the faces of the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a metal wiring connecting the elements, a conductor portions formed inside the through holes for electrically connecting the metal wiring, a metal terminal part of a part of the metal wiring and a plurality of organic insulator materials covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion, with the above provision an electronic circuit component, which shows a desirable manufacturing yield and permits to integrate in a high density and in a high performance a variety of electronic parts such as the capacitor, inductor and resistor through selection of the organic insulator materials suitable for the necessary frequency characteristics of the respective elements can be obtained.

[0025] Further, in order to achieve the above object, an electronic circuit component comprises an insulator substrate at predetermined position of which through holes are provided, a plurality of electrodes provided on both faces of the main face and the sub-main face or one of the faces of the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a metal wiring connecting the elements, a conductor portions formed inside the through holes for electrically connecting the metal wiring, a metal terminal part of a part of the metal wiring, a first organic insulator material covering the elements provided on the main face of the insulator substrate and the circumference of the metal wiring portion excluding the metal terminal portion and a second organic insulator material covering the elements provided on the sub-main of the insulator substrate and the circumference of the metal wiring portion excluding the metal terminal portion, with the above provision an electronic circuit component , which shows a desirable manufacturing yield and permits to integrate in a high density and in a high performance a variety of electronic parts such as the capacitor, inductor and resistor through selection of the organic insulator materials suitable for the necessary frequency characteristics of the respective elements can be obtained.

[0026] Further, in order to achieve the above object, an electronic circuit component comprises an insulator substrate at predetermined position of which through holes are provided, a plurality of electrodes provided on both faces of the main face and the sub-main face or one of the faces of the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a metal wiring connecting the elements, a conductor portions formed inside the through holes for electrically connecting the metal wiring, a metal terminal part of a part of the metal wiring and being provided on the other face where the inductor element is provided and an organic insulator material covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion, with the above provision an electronic circuit component, which shows a desirable manufacturing yield, reduces an influence to the inductor element from electronic parts mounted on the substrate and permits

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to integrate in a high density and in a high performance a variety of electronic parts such as the capacitor, inductor and resistor can be obtained.

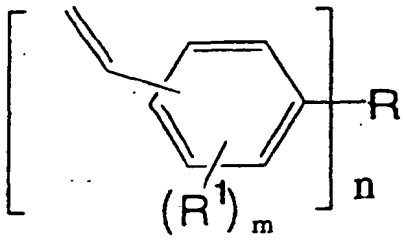
[0027] Further, in order to achieve the above object, an electronic circuit component comprises an insulator substrate at predetermined position of which through holes are provided, a plurality of electrodes provided on both faces of the main face and the sub-main face or one of the faces of the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a metal wiring connecting the elements, a conductor portions constituted of a conductive material, core forming material and glass and formed inside the through holes for electrically connecting the metal wiring, a metal terminal part of a part of the metal wiring and an organic insulator material covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion, with the above provision an electronic circuit component, which shows a desirable manufacturing yield, ensures electrical conduction between both faces of the substrate and permits to integrate in a high density and in a high performance a variety of electronic parts such as the capacitor, inductor and resistor can be obtained.

[0028] Further, in order to achieve the above object, since distances of the electrodes, the capacitor element of a dielectric material formed being sandwiched between the electrodes, the inductor element and the resistor element with respect to the insulator substrate are differentiated, the capacitor, inductor and resistor elements can be integrated in a further high density.

[0029] Still further, in order to achieve the above object, through the use of the glass substrate for the insulator substrate, a further low cost and high performance electronic circuit component can be obtained because of the low cost property, high flatness, high insulation property and low dielectric loss tangent of the glass substrate.

[0030] Still further, in order to achieve the above object, through the use of the photosensitive organic insulation material for the organic insulator, a further low cost electronic circuit component can be obtained because the number of the process steps during the manufacture is reduced and the manufacturing cost thereof is reduced.

[0031] Still further, in order to achieve the above object, as the organic insulator since a low dielectric loss tangent resin composition is used which includes a bridging component having a plurality of styrene groups as expressed by the following general chemical formula and contains polymers having average molecular weight of more than 5000, a further high performance and high efficiency electronic circuit component can be obtained with a low cost because of the low cost property, low dielectric constant and low dielectric loss tangent of the low dielectric loss tangent resin compositions.



(Wherein, R represents a hydrocarbon skeleton, which may include a subst ituent, R^1 represents one of hydrogen, methyl and ethyl, m represents 1 from 4 and n represents an integer more than 1). Still further, in order to achieve the above object, when the organic insulator is polyimide resin, a highly reliable electronic circuit component can be obtained because of high thermal stability of polyimide.

[0032] Further, in order to achieve the above object, when the organic insulator is BCB (Benzo Cyclo Butene), a further high performance and high efficiency electronic circuit component can be obtained because of low dielectric constant and low dielectric loss tangent of BCB.

[0033] Further, in order to achieve the above object, when the dielectric material is an oxide of any of Ta, Mg and Sr, a low cost, high reliability and high performance electronic circuit component can be obtained because of low cost and high stability property of Ta, Mg and Sr. further, when the oxide of Ta is used for the dielectric material, the dielectric strength thereof can be enhanced, when the oxide of Mg is used, Q value can be enhanced and when the oxide of Sr is used, a high ε can be obtained. Wherein Q value represents a sharpness of resonance (frequency selectivity) and is defined according to the following equation; $Q = \omega$(accumulated energy)/(loss)=Im(Z)/Re(Z) Wherein, Im(Z) and Re(Z) are impedances in an imaginary part and real part one port (a terminal pair) of the respective elements.

[0034] The capacitor elements of the present invention are constituted by one or more of capacitor elements having a structure in which an inorganic dielectric material is sandwiched by two metal electrodes and one or more capacitor elements having a structure in which an organic dielectric material is sandwiched by two electrodes. Further, the end portion of the metal electrode adjacent the glass substrate of the capacitor element is preferably covered by an insulator other than the dielectric material.

[0035] The metal electrode is preferably to be a low electrical resistance conductive material. More specifically, such as gold, copper, nickel, aluminum, platinum, tungsten, molybdenum, iron, niobium, titanium, nickel/chromium alloy, iron/nickel/chromium alloy and tantalum nitride are enumerated for the material. In particular, copper is preferable because of it's low electric resistance. Further, the surface of the metal electrode is re-

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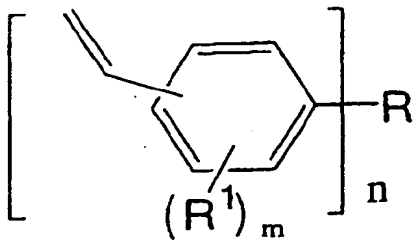
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quired to be flat and the unevenness of the surface is preferable to be below 1/25 of the thickness of the dielectric body. Further, when a metal having a high melting p oint is used for a lower electrode, a laser processing or a high temperature burning can be applied during the dielectric layer formation and a high performance (due to applicability of a high ε dielectric material) and an enhancement of manufacturing yield can be realized. As methods of forming the metal electrode, other than one in which after forming the conductive material in a film having a predetermined film thickness, a resist pattern is formed and the electrode is formed by dry or wet etching, after forming the resist pattern, the electrode can be formed by electro or electro less plating. With regard to forming methods of the metal electrodes and other wirings, when a plating method is used, a resistance reduction, high efficiency and high performance can be achieved, because a thick film wiring can be realized. Further, when a spattering method is used, a minuting, size reduction and high performance can be achieved, because a formation of a minute pattern can be realized.

[0036] The inorganic material is not limited, if the material is used commonly as a capacitor use dielectric material, for example, oxides of Ta, Mg and Sr are enumerated. Specifically, other than oxides such as Ta_2O_5, BsT (Ba(x)Sr(1-x)TiO(3), 0 x 1), $SrTiO_3$, TiO_2, MnO_2, Y_2O_3, SnO_2 and $MgTiO_3$, barium titanium oxide, compound formed by doping zirconium and tin into barium titanium oxide, WO_3, SrO, mixed barium/strontium oxide, $BaWO_4$, and CeO_2 are enumerated. The method of forming the dielectric layer is not limited and a spattering method, a dry method such as plasma CVD method and a wet method such as anodic oxidation method can be used. A dielectric layer formation with dry method such as spattering method and etching me thod enables a minute pattern, which is effective for minuting, size reduction and high performance. Further, a dielectric layer formation with wet methods such as sol-gel method and anodic oxidation method can simplify the processing steps, which is effective for reducing the cost.

[0037] Further, the organic material is not limited, if such is an organic material commonly used for semiconductor whether such is thermo setting or thermo plastic. For example, polyimide, polycarbonate, polyester, poly tetra fluoro ethylene, polystylene, polypropylene, poly vinylidene fluoride, cellulose acetate, polysulfone, polyacrylonitrile, polyamide, polyamideimide, epoxy, maleimide, phenol, isocyanate, polyolefin, polyurethane and compounds thereof can be used. Mixture formed by adding a rubber component such as acrylic rubber silicone rubber and nitrylbutadiene rubber, an organic compound filler such as polyimide filler and an inorganic filler such as silica to any of the above compounds. Further, the organic material can be formed by a photosensitive material containing any of the compounds above. When a photosensitive insulator material is used, the process of forming a resist on the insulator material can be eliminated, thereby, the manufacturing yield can be enhanced. Further, a microfabrication is enabled, which can realize size reduction.

[0038] In particular, polyimide resin is preferable because of it's excellent heat resistance and chemical resistance, and further, the polyimide provided with photosensitivity is preferable because of it' excellent workability. Further, benzo cyclo butene is preferable because of it's low dielectric loss tangent, when the capacitor of the present invention is used for a high frequency parts. Likely, resin composition having low dielectric loss tangent as expressed by the following general chemical formula which includes a bridging component having a plurality of styrene groups and further, includes polymers having weight average molecular weight of more than 5000 is also preferable, because the transmission loss can be reduced. For skeletons connecting the styrene groups of the above resin composition, hydrocarbon skeletons containing alkylene groups such as methylene and ethylene. Specifically, 1,2-bis (p-biphenyl) ethane, 1,2-bis (m-biphenyl) ethane and their equivalents, homopolymer of divinyl benzene having vinyl group at the side chains and oligomers of copolymers such as with styrene are enumerated.



(Wherein, R represents a hydrocarbon skeleton, which may include a substituent, R^1 represents one of hydrogen, methyl and ethyl, m represents 1 from 4 and n represents an integer more than 1).

[0039] Further, a function as a stress buffer can be provided for the above organic insulator material. Specifically, such as fluoro rubber silicone rubber, fluoro silicone rubber, aklyle rubber, hydronitryl rubber, ethylene propylene rubber, chloro sulfonated polyethylene, epichlorhydline rubber, butyl rubber, urethane rubber, polycarbonate/aklylonitril butadiene styrene alloy,polysiloxane dimethylene terephthalate /polyethylene terephthalate copolymer polybutylene terephthalate/polycarbonate alloy, polytetrafluoroethylene, florinated ethylene propylene, polyarylate, polyamide/aklylonitril butadiene styrene alloy, denaturated epoxy, denaturated polyolefin and siloxane denaturated poly amideimide can be enumerated.

[0040] As the formation methods thereof include a pattern printing method such as a printing method, an ink jet method and an electro photography method, a method such as a film pasting method and spin coating

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method in which after forming organic insulation material , patterns are formed such as by photo process and laser and combination thereof.

[0041] Other than the above, a variety of thermosetting resins such as epoxy resin, unsaturated polyester resin, epoxy isocyanate resin, maleimide resin, maleimide epoxy resin, cyanic acid ester resin, cyanic acid ester epoxy resin, cyanic acid ester maleimide resin, phenol resin, diallyl phthalate resin, urethane resin, cyanamide resin and maleimide cyanamide resin, materials formed by combining two or more resins above and materials mixing inorganic filler therein can be used. Further, by providing a photosensitivity to the above resin and through a predetermined exposure and developing process the shape of the stress buffering layer can be controlled.

[0042] Further, as the organic insulators, different insulation materials can be used between layers. When different insulation materials are used between layers, a proper material depending on the re quired property for the particular portion such as low loss and chemical resistance can be selected, which help to achieve high performance. Further, when organic insulators are formed on both sides of the insulator substrate while sandwiching the same, if different organic materials are used, the same advantage as above can be obtained.

[0043] The inductor element of the present invention is not in particular limited, if the same is an inductive circuit element, for example, such as a spiral type formed on a plane, one formed by laminating the spiral type, and a solenoid type can be used. Further, the inductance thereof is preferable to be in a range of 10nH/ mm^2~100nH/ mm^2.

[0044] Further, the inductor element and the metal wiring can be either a same material or different material and the material therefor is selected properly according to electrical conductivity, adhesive property with the surrounding materials and formation method. Further, the formation method therefor is not in particular limited. For example, Cu film can be formed by making use of spattering method and such as Ti and Cr films can be formed at the interface thereof in view of adhesive property with the surrounding materials. Further, after forming a thin film operating as a seed film with Cu through spattering method, the inductor element can be formed by electrolytic plating. Further, as patterning methods of the wiring and the inductor element, common wire patterning methods such as etching method and lift off method can be used. Further, the wiring and the inductor element can also be formed through printing method by making use of resin paste containing metal such as Ag. Still further, when the forming temperature of the inorganic dielectric layer is high, a metal having oxidation resistant and heat resistant property such as Pt can be used. When forming the inductor, if the distance between the wirings constituting the inductor is shortened with respect to the wiring width of the inductor, the space at the center portion of the inductor can be enlarged, which enhances efficiency and performance thereof.

[0045] The resistance element of the present invention is structured by sandwiching a resistance material between two metal electrodes and the resistance material is not limited in particular, if a common resistor material is used therefor, and for example, such as CrSi and TiN can be used therefor. The formation method therefor is also not limited in particular and for example, such as spattering method and plasma CVD method can be used. Further, the resistance element is formed at the lowest layer, the burning thereof at a higher temperature than the curing temperature of the insulation material is permit ted, which is effective for enhancing the manufacturing yield and the cost reduction.

[0046] The insulator substrate of the present invention is not in particular limited, if the same does not reduce the efficiency of the respective elements and shows a high insulation property. Further, the glass substrate of the present invention is also not in particular limited, if the same does not reduce the efficiency of the respective elements and shows a high insulation property and is selected in view of strength and workability thereof. Specifically, glasses containing at least one rare earth element selected among the group including Sc, Y, La, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu are in particular preferable. Further, it is preferable that the rare earth element is contained in a range of 0.5~20 weight% with respect to the entire glass components when converted based on oxide of Ln_2O_3 (Ln is a rare earth element) and as the other components it is preferable that SiO_2:40~80 weight%, B_2O_3:0~20 weight%, R_2O (R_2 is alkali metal):0~20 Weight%, RO (R is alkaline earth metal):0~20 weight% and Al_2O_3: 0~17 weight% are contained, and it is preferable that R_2O + RO are contained in an amount of 10~30 eight%, thereby, the strength of the glass substrate is greatly en hanced and the workability is significantly improved.

[0047] With regard to the configuration of the through holes of the present invention, it is preferable to satisfy the following relationship between the two opening diameters R1 and R2 of the through holes and the thickness t of the glass substrate;

$$70 \leqq \tan^{-1}(t/(R1-R2)) \leqq 80$$

wherein, the opening diameters R1 and R2,the arrangement thereof and the thickness of the substrate can be properly selected depending on the sizes of the elements and wirings to be mounted or integrated.

[0048] Further, the forming method thereof is not limited, if the same does not cause any large physical or chemical damage on the glass substrate. Any already known boring technology can be applied. For example, micro sand blasting method, chemical etching method, laser processing method and photosensitive processing method using photosensitive glass are enumerated. Regardless to the method used, it is important that the

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method used does not cause any physical or chemical damages such as chippings and cracks at the opening portions and the inside of the through holes as referred to the above.

[0049] Further, even if physical or chemical damages such as chippings and cracks are caused with any of the above through hole forming methods, such can be recovered and the substrate can be used. For the recovering, such as a method of removing the damages by etching with hydrofluoric acid of the glass surface where the chippings or cracks are caused, a method of burying such as cracks with sol-gel liquid of the glass and a method of performing a heattreatment near at the softening point of the glass substrate material are enumerated. Of course, the methods are not limited to the above, if the method can remove or seal the damages.

[0050] Further, the conductive portions of the present invention formed inside the through holes provided at the insulator substrate is not in particular limited, if such can electrically connect the metal wirings and the elements provided on the main and sub-main faces of the substrate, for example, a conductive material constituted of a conductive material, core forming material and glass can be used. Further, such is not in particular limited, if the same can electrically connect the circuit portions on both sides of the glass substrate and is properly selected according to the electrical conductivity, adhesiveness with the circumference materials and the forming method thereof. Further, the forming method thereof is not in particular limited. For example, a conductive layer of such as Cu can be formed on the walls of the through holes with spattering method and in view of adhesiveness with the surrounding materials Ti or Cr can be formed at the interface thereof. Further, after forming a thin film of such as Cu serving as a seed film with spattering method, the conductive layer can be formed with electrolytic plating method. Further, electroless plating method can also be used. Still further, a resin past containing a metal such as Ag can be buried inside the through holes.

[0051] The connecting portions of the present invention provided at portions other than the end portions of the electrodes are not in particular limited, if such are electrically connected with the upper metal wiring portions, after boring through holes at the organic insulator covering the electrodes with etching method, the connecting portions can be formed together with the upper wiring layers by plating. As another through hole forming method, the through holes can be formed with photomask method by using photosensitive organic insulator material such as photosensitive polyimide and BCB as the organic insulator.

[0052] The arrangement of the respective elements of the present invention is not in particular limited, however, it is necessary to design the arrangement of the respective elements in view of the performance reduction due to a parasitic capacity caused by coupling between the respective elements and an integration rate depending on the desired size of the electronic circuit component.

[0053] For example, the electronic circuit component does not require much size reduction, it is necessary to reduce an influence between the respective elements by arranging the respective elements on the same plane or to enlarge the distance between the layers. Further, a provision of a grounded plane, namely, a grounde d layer is another method.

[0054] Further, if the size reduction is desired, through forming the respective elements on both sides of the substrate, the integration rate is increased and the size is further reduced.

[0055] In order to further reduce the size, when the respective elements are formed on multiple faces in a layer lamination structure, the size is further reduced.

[0056] Further, by arranging the respective elements separately, while sandwiching the glass substrate there between, the production process is simplified and a low cost electronic circuit component can be obtained. Further, since large distances between the respective elements can be ensured, an increase of parasitic capacity due to the coupling can be prevented.

[0057] In the electronic circuit component of the present invention, it is not necessarily required that the external electrodes for electrical connection with the externals are formed on the metal end portions, however, if necessary, such can be formed thereon.

[0058] The external electrode is a conductive body for electrically connecting with the substrate on which the electronic circuit component of the present invention and the semiconductors, and specifically, a ball shaped body of solder alloy containing tin, zinc and lead, silver, copper, gold or one coated by gold are used. Further, other than the above an alloy formed by combining one or more of such as molybdenum, nickel, copper, platinum and titanium or a terminal having multi layered structure can be used. Further, as the forming method thereof, any conventional methods such as a method of transfer printing the ball shaped electrodes by using masks and a method of pattern printing can be used.

BRIEF DESCRIPTION OF THE DRAWINGS

[0059]

Fig.1 is a schematic cross sectional view representing first ~ fourth embodiments of the present invention;

Fig.2 is a schematic cross sectional view representing fifth embodiment of the present invention;

Fig.3 is a schematic cross sectional view representing sixth embodiment of the present invention;

Fig.4 is a view showing a capacitor element in the sixth embodiment of the present invention;

Fig.5 is a circuit diagram of the electronic circuit component representing a seventh embodiment of the present invention;

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Fig.6 is a schematic cross sectional view of the seventh embodiment of the present invention;
Fig.7 is an exploded view of the seventh embodiment of the present invention;
Figs.8 through 14 are plane pattern diagrams of respective layers in the seventh embodiment of th e present invention;
Fig.15 is a schematic cross sectional view representing eighth embodiment of the present invention;
Fig. 16 is a schematic cross sectional view representing ninth embodiment of the present invention;
Fig. 17 is a schematic cross sectional view representing tenth embodiment of the present invention;
Fig.18 is a schematic cross sectional view representing eleventh embodiment of the present invention;
Fig.19 is a schematic cross sectional view representing twelfth embodiment of the present invention;
Fig.20 is a schematic cross sectional view representing thirteenth embodiment of the present invention; and
Fig.21 is a schematic cross sectional view representing fourteenth embodiment of the present invention.

BEST MODES FOR CARRYING OUT THE INVENTION

[0060] Hereinbelow, the present invention will be explained further specifically with reference to the embodiments. Further, in all the drawings for explaining the present invention, ones having the same functions are designated by the same reference numerals and repetitive explanation thereof is omitted.

(Embodiment 1)

[0061] Fig.1 is a cross sectional view of an electronic circuit component representing one embodiment of the present invention. In Fig.1, 1 is a glass substrate (product of Nippon Electric Glass Co., Ltd.,BLC), and the thickness of which is 0.5mm.

[0062] In Fig.1, 2 is an organic insulator and photosensitive polyimide (product of Hitachi Chemical Co., Ltd., HD-6000) is used therefor.

[0063] A capacitor element 3 formed inside the organic insulator 2 is in a three layer structure constituted by a lower electrode 3a, a dielectric body 3b and an upper electrode 3c. The lower electrode 3a is composed by Cu, the dielectric body 3b by oxide of Ta and the upper electrode 3c by Cu.

[0064] An inductor element 4 is a spiral type inductor and is formed on the same plane as the upper electrode 3c of the capacitor element 3 and the material thereof is Cu.

[0065] A resistor 5 is constituted by a resistance body 5b and electrodes 5a and 5 c. The resistance body 5b is a compound of Ta and Ti and the electrodes 5a and 5c are composed of Cu.

[0066] In Fig.1, 6 is a metal terminal portion used for connection with a mounting substrate such as a print substrate and in the drawing a solder ball 7 is mounted on the metal terminal portion 6.

[0067] The manufacturing method of the electronic circuit component as shown in Fig.1 will be explained.

[0068] A Cr film of 50nm was formed on a glass substrate of 0.5 mm thickness with spattering method and further, a Cu film of 500nm was formed thereon, which was used for current feeding use seed film for Cu plating. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10 μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the lower electrode was formed.

[0069] Subsequently, as a barrier film a Cr film of 50nm is formed with spattering method.

[0070] Then, Ta_2O_5 film having thickness of 500nm was formed on the lower electrode by spattering method. On the Ta_2O_5 film positive type liquid resist OFPR800, 500cp(product of Tokyo Ohka) was coated and after performing drying, exposing and developing process a resist mask for a dielectric layer was formed. Subsequently, dry etch was performed by making use of CF_4 to remove unnecessary portion thereof and further, unnecessary portion of the barrier layer was removed with Cr etching liquid of permanganic acid, then, the resist mask was removed and the dielectric layer was formed.

[0071] Subsequently, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the dielectric layer over the lower electrode was exposed. In this instance the polyimide having an opening is hardened at 250° C/2 hours under nitrogen atmosphere and the organic insulator of 10μm was formed so that the polyimide covering portion comes inside by 80 μ m from the scribe area used for cutting into pieces as the electronic circuit components.

[0072] Then, a TaN film of 500nm was formed with spattering method. On the film positive type liquid state resist OFPR 800,100cp was spin-coated and prebaked, thereafter, a resist pattern mask was formed through exposure and development. By using the mask The TaN film was dry etched with CF_4. Then, a plurality of resistor elements were formed by peeling off the resist.

[0073] A Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed ther-

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eon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the upper electrode, electrodes for the resistors and the inductor were formed.

[0074] On the plane where the upper electrode, the electrodes for the resistor and the inductor were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portion for interlayer connection was formed. In this instance the polyimide having an opening is hardened at 250° C/1 hour under nitrogen atmosphere and the organic insulator was formed so that the polyimide covering portion comes inside by 80 μm from the scribe area used for cutting into pieces as the electronic circuit components.

[0075] In order to form the metal terminal portion on the organic insulator surface the electrolytic plating use seed films Cr:50nm, Cu:500nm were formed. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated and prebaked, thereafter, a resist mask for plating was formed through exposure and development, then a plating film of 10μm was formed by Cu electrolytic plating and further, an electrolytic nickel plating film of 2μm was formed. Finally, after peeling off the resist and the electrolytic plating seed film, the wirings and the metal terminal portions were formed.

[0076] On the plane where the metal terminal portions were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portions for forming the solder balls were formed. In this instance the polyimide having an opening is hardened at 250° C/1 hour under nitrogen atmosphere and the organic insulator was formed so that the polyimide covering portion comes inside by 80 μm from the scribe area used for cutting into pieces as the electronic circuit components.

[0077] After applying electroless gold plating on the surface of the metal terminal portion and then coating solder flux on a predetermined portion with a metal mask, the external electrodes were formed by arranging the lead free solder balls having a diameter of 200μm and performing reflow processing.

[0078] Finally, the product was separated by a dicing machine to form the electronic circuit components.

[0079] As has been explained above, by integrating the passive elements such as the inductors, capacitors and resistors, which were conventionally mounted in single parts, the mounting area can be halved and the size thereof is further reduced. Further, since a glass having a high insulation property is used for the substrate, a possible efficiency reduction of the respective elements can be prevented and efficiency of about five times in comparison with ones using the conventional silicon substrate can be obtained. Still further, the manufacturing cost is also halved in comparison with the ones using the conventional silicon substrate.

[0080] Still further, by forming the passive elements such as the capacitors, inductors and resistors at the inside from the end portion of the glass substrate, the structural portions where stresses concentratedly applied at the time of cutting out the electronic circuit components and at the time of mounting the same are designed to withstand the stresses and a possible damage on the electronic circuit components due to the applied stresses can be greatly reduced, thereby, a highly reliable electronic circuit components of a desirable manufacturing yield can be obtained.

[0081] Further, Fig. 1 structure is one embodiment of the present invention, and the arrangement of the respective elements is not limited to that shown.

(Embodiment 2)

[0082] In embodiment 2, in place of the glass substrate 1 used in embodiment 1 in Fig.1, the following glass substrate was used. The composition of the glass substrate of the present embodiment contains at least one rare earth element selected among the group including Sc, Y, La, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu in an amount of 0.5~20 weight% with respect to the entire glass components when converted based on oxide of Ln_2O_3 (Ln is a rare earth element) and as the other components contains SiO_2:40~80 weight%, B_2O_3:0~20 weight%, R_2O (R_2 is alkali metal): 0~20 weight%, RO (R is alkaline earth metal):0~20 weight% and Al_2O_3:0~17 weight%, and it is preferable that R_2O + RO are contained in an amount of 10~30 weight%. Further, the thickness thereof was 0.5mm like embodiment 1.

[0083] Further, the portions other than the glass substrate 1 in the present embodiment are the same as those in embodiment 1.

[0084] Further, the manufacturing method of the electronic circuit components of the present embodiment is the same as that of embodiment 1.

[0085] The bending resistances of the glass substrate (product of Nippon Electric Glass Co., Ltd.) used in embodiment 1 and of the glass substrate used in embodiment 2 were respectively 200Mpa and 300Mpa. The bending resistances were the values measured with a four point bending meter and the shape of the samples was 10mm x 36mm x0.5mm. As will be apparent from the above, the strength of the glass substrate used in

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embodiment 2 is about two times larger than that of the glass substrate in embodiment 1.

[0086] Accordingly, the electronic circuit component of embodiment 2 shows a high reliability such as in connection with impact resistance.

[0087] Through the use of such glass substrate containing at least one rare earth element selected among the group including Sc, Y, La, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu in an amount of 0.5~20 weight% with respect to the entire glass components when converted based on oxide of Ln_2O_3 (Ln is a rare earth element) and as the other components contains SiO_2:40~80 weight%, B_2O_3:0~20 weight%, R_2O (R_2 is alkali metal):0~20 weight%, RO (R is alkaline earth metal):0~20 weight% and Al_2O_3:0~17 weight%, and it is preferable that R_2O + RO are contained in an amount of 10~30 weight%, a further highly reliable electronic circuit component in addition to the advantages in embodiment 1 can be obtained.

(Embodiment 3)

[0088] In embodiment 3, in place of the photosensitive polyimide used in embodiment 1, BCB (product of Dow Chemical, Cycloten 4026) was used as the organic insulator 2.

[0089] Further, the portions other than the organic insulator 2 in the present embodiment are the same as those in embodiment 1.

[0090] Further, the manufacturing method of the electronic circuit component of the present embodiment is the same as that of embodiment 1.

[0091] The dielectric constant and dielectric loss tangent of BCB are respectively 2.65 and 0.003, which are respectively smaller than 3.5 and 0.01 of the photosensitive polyimide.

[0092] Accordingly, by using BCB as an insulator layer which covers the circumference of the electronic parts, the conductive loss and dielectric loss are reduced, thereby, loss of signals passing through the electronic parts can be reduced.

[0093] Through the use of BCB for the organic insulator in the present embodiment, the conductive loss and dielectric loss are reduced, thereby, an electronic circuit component having a small signal passing loss in addition to the advantages in embodiment 1 can be obtained.

[0094] Further, through the use of the glass used in embodiment 2, the electronic circuit component of course shows a high reliability such as in connection with impact resistance.

(Embodiment 4)

[0095] In embodiment 4, in place of the photosensitive polyimide used in embodiment 1, the low dielectric loss tangent resin composition as shown in the above chemical formula which includes a bridging component having a plurality of styrene groups as expressed by the following general chemical formula and contains polymers having average molecular weight of more than 5000 was used as the organic insulator 2.

[0096] Further, the portions other than the organic insulator 2 in the present embodiment are the same as those in embodiment 1.

[0097] Further, the manufacturing method of the electronic circuit component of the present embodiment is the same as that of embodiment 1 except for the formation method of the low dielectric loss tangent resin composition which will be explained below.

[0098] The above low dielectric loss tangent resin composition was formed in the following manner. Three kinds of raw materials of synthesized 1,2-bis (vinyl phenyl) ethane of 30 weight parts, cyclic poly olefin (product of Nihon Zeon, Zeonex 480) of 70 weight parts and curing catalyst per hexyne 25B of 0.3 weight part were resolved in xylene solvent so as to assume the solid component to be of 38% to prepare a varnish.

[0099] The varnish was coated by spin coating and baked on a hot plate under 120°C/2min, thereafter, a step curing under 200°C/5min was performed to form the insulator of 10 μm. On the insulator positive type liquid resist OFPR800, 500cp(product of Tokyo Ohka) was spin-coated and dried, thereafter, through exposing and developing process a resist mask having an opening portion was formed so that the end of the opening portion comes inside the end portion of the lower electrode by 20 μm. Subsequently, the low dielectric loss tangent resin composition was dry etched by making use of CF_4 and the dielectric body above the lower electrode was exposed. Finally, the resist was peeled off.

[0100] The dielectric constant and dielectric loss tangent of the low dielectric loss tangent resin composition are respectively 2.45 and 0.0015, which are respectively smaller than 3.5 and 0.002 of the photosensitive polyimide and likely smaller than 2.65 and 0.003 of BCB.

[0101] Further, the cost of the resin composition is 20000 yen/kg, which is inexpensive about 1/10 in comparison with BCB, which is 230000 yen/kg.

[0102] Accordingly, by using the low dielectric loss tangent resin composition as an insulator layer which covers the circumference of the electronic parts, the conductive loss and dielectric loss are reduced, thereby, loss of signals transmission through the electronic circuits can be reduced with the low cost material.

[0103] Through the use of the low dielectric loss tangent resin composition for the organic insulator in the present embodiment, the conductive loss and dielectric loss are reduced, thereby, a low cost electronic circuit component having a small signal transmission loss in addition to the advantages in embodiment 1 can be obtained.

[0104] Further, through the use of the glass used in embodiment 2, the electronic circuit component of course shows a high reliability such as in connection with impact resistance.

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(Embodiment 5)

[0105] Fig.2 is a cross sectional view of an electronic circuit component representing one embodiment of the present invention. In Fig.2, 1 is a glass substrate (product of Nippon Electric Glass Co., Ltd.,BLC), and the thickness of which is 0.5mm.

[0106] In Fig.2, 2 is an organic insulator and photosensitive polyimide (product of Hitachi Chemical Co., Ltd., HD-6000) is used therefor.

[0107] Capacitor elements formed inside the organic insulator 2 are constituted by a capacitor 3 in a three layer structure constituted by a lower electrode 3a of Cu, a dielectric body 3b of oxide of Ta and an upper electrode 3c of Cu and a capacitor 3' in a three layer structure constituted by a lower electrode 3'a of Cu, a dielectric body 3'b of polyimide and an upper electrode 3'c of Cu.

[0108] An inductor element 4 is a spiral type inductor and is formed of Cu.

[0109] A resistor 5 is constituted by a resistance body 5b and electrodes 5a and 5 c. The resistance body 5b is a compound of Ta and Ti and the electrodes 5a and 5c are composed of Cu.

[0110] In Fig.2, 6 is a metal terminal portion used for connection with a mounting substrate such as a print substrate and in the drawing a solder ball 7 is mount ed on the metal terminal portion 6.

[0111] The manufacturing method of the electronic circuit component as shown in Fig.2 will be explained.

[0112] A sand blast use film resist material(product of Tokyo Ohka, Odale)of 100μ m was laminated on the glass substrate having thickness of 0.5mm through exposure and development process and an etching use resist was formed. Subsequently, through holes were formed in the glass substrate with micro sand blasting method. Then, the resist film was peeled off, electrolytic pl ating use seed films Cr:50nm, Cu:500nm were formed on the surface of the glass substrate and walls of the via holes with spattering method. Thereafter, on the Cu film, a plating use film resist(product of Hitachi Chemical Co., Ltd., HN 920) was laminated and a resist mask was formed through exposure and development, then, conductive layers were formed inside the via holes by Cu electrolytic plating . Subsequently, the resist and the electrolytic plating seed film were peeled off.

[0113] A Cr film of 50nm was formed on a glass substrate of 0.5 mm thickness with spattering method and further, a Cu film of 500nm was formed thereon, which was used for current feeding use seed film for Cu plating. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10 μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the lower electrode was formed.

[0114] Subsequently, as a barrier film, a Cr film of 50nm is formed with spattering method.

[0115] Then, Ta_2O_5 film having thickness of 500nm was formed on the lower electrode 3a by spattering method. On the Ta_2O_5 film positive type liquid resist OFPR800, 500cp(product of Tokyo Ohka) was coated and after performing drying, exposing and developing process a resist mask for a dielectric layer was formed. Subsequently, a dry etch was performed by making use of CF_4 to remove unnecessary portion thereof and further, unnecessary portion of the barrier layer was removed with Cr etching liquid of permanganic acid, then, the resist mask was removed and the dielectric layer was formed.

[0116] Subsequently, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the dielectric layer over the lower electrode 3a was exposed. In this instance the polyimide having an opening is hardened at 250° C/2 hours under nitrogen atmosphere and the organic insulator of 10μm was formed so that the polyimide covering portion comes inside by 80 μ m from the scribe area used for cutting into pieces as the electronic circuit components. The organic insulator formed above the lower electrode 3'a according to the above process is the dielectric body 3'b.

[0117] Then, a TaN film of 500nm was formed with spattering method. On the film positive type liquid state resist OFPR800,100cp was spin-coated and prebaked, thereafter, a resist pattern mask was formed through exposure and development. By using the mask The TaN film was dry etched with CF_4. Then plural resistor elements were formed by peeling off the resist.

[0118] A Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the upper electrode, electrodes for the resistors and the inductor were formed.

[0119] On the plane where the upper electrode, the electrodes for the resistor and the inductor were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and devel-

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oping process the opening portion for interlayer connection was formed. In this instance the polyimide having an opening is hardened at 250° C/1 hour under nitrogen atmosphere and the organic insulator was formed so that the polyimide covering portion comes inside by 80 μm from the scribe area used for cutting into pieces as the electronic circuit components.

[0120] In order to form the metal terminal portion on the organic insulator surface the electrolytic plating use seed films Cr:50nm, Cu:500nm were formed. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated and prebaked, thereafter, a resist mask for plating was formed through exposure and development, then, a plating film of 10μm was formed by Cu electrolytic plating and further, an electrolytic nickel plating film of 2μm was formed. Finally, after peeling off the resist and the electrolytic plating seed film, the wirings and the metal terminal portions were formed.

[0121] On the plane where the metal terminal portions were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portions for forming the solder balls were formed. In this instance the polyimide having an opening is hardened at 250 ° C/1 hour and the organic insulator was formed so that the polyimide covering portion comes inside by 80μm from the scribe area used for cutting into pieces as the electronic circuit components.

[0122] After applying electroless gold plating on the surface of the metal terminal portion and then coating solder flux on a predetermined portion with a metal mask, the external electrodes were formed by arranging the lead free solder balls having a diameter of 200 μm and performing reflow processing.

[0123] Finally, the product was separated by a dicing machine to form the electronic circuit components.

[0124] In the present embodiment, through the use of the inorganic material having a high dielectric constant such as the oxide of Ta as well as the organic material having a low dielectric constant such as the polyimide as the dielectric body material, capacitors having a small capacitance can be formed accurately, which enhances reliability of the circuits and expands available capacitance range. Further, through the use of the same material for the dielectric body as the insulator material, which covers the circumference of the elements, the semiconductor connection substrate can be manufactured in further simplified and low cost processes in addition to the advantages obtained in embodiment 1.

[0125] Further, through the use of the glass used in embodiment 2, the electronic circuit component of course shows a high reliability such as in connection with impact resistance.

[0126] Through the use of BCB organic insulator used in embodiment 3 for the organic insulator in the present embodiment, the conductive loss and dielectric loss are reduced, thereby the signal transmission loss in the electronic circuit can be reduced.

[0127] Further, by using the low dielectric loss tangent resin composition as used in embodiment 4 as the insulator layer, the conductive loss and dielectric loss are reduced, thereby, loss of signals transmitting through the electronic circuits can be reduced with the low cost material.

[0128] Further, Fig.2 structure is one embodiment of the present invention, and the arrangement of the respective elements is not limited to that shown.

(Embodiment 6)

[0129] Fig.3 is a cross sectional view of a semiconductor connection substrate representing one embodiment of the present invention. In Fig.3, 1 is a glass substrate (product of Nippon Electric Glass Co., Ltd.,BLC), and the thickness of which is 0.5mm.

[0130] In Fig.3, 2 is an organic insulator and photosensitive polyimide (product of Hitachi Chemical Co., Ltd., HD-6000) is used therefor.

[0131] Capacitor elements formed inside the organic insulator 2 are constituted by a capacitor 3 in a three layer structure constituted by a lower electrode 3a of Cu, a dielectric body 3b of oxide of Ta and an upper electrode 3c of Cu and a capacitor 3' in a three layer structure constituted by a lower electrode 3 'a of Cu, a dielectric body 3'b of polyimide and an upper electrode 3'c of Cu. Further, on the upper electrodes connecting portions 8 for connecting the same with wirings on the upper layer are provided.

[0132] An inductor element 4 is a spiral type inductor and is formed of Cu.

[0133] A resistor 5 is constituted by a resistance body 5b and electrodes 5a and 5 c. The resistance body 5b is a compound of Ta and Ti and the electrodes 5a and 5c are composed of Cu.

[0134] In Fig.3, 6 is a metal terminal portion used for connection with a mounting substrate such as a print substrate and in the drawing a solder ball 7 is mounted on the metal terminal portion 6.

[0135] Further, Fig.4 shows parts of the capacitor element in Fig.3. In the capacitor in Fig.4, the dielectric body 3b is formed so as to cover the side faces of the lower electrode 3c and a reduction of defects due to current leakage between the upper and lower electrodes is achieved. Since the area of the upper electrode is formed smaller than that of the lower electrode, the capacitance of the capacitor is determined based on the area of the upper electrode. For the connection between the upper electrode 3c and the wirings on the upper layer, as shown in Fig.4, from a portion other than the end portion of the upper electrode 3c a wiring is lead out through a via hole in the organic insulator 2 to the upper layer to complete the connection. However, when the connection is performed by leading out the wiring from the side face of the upper electrode, the area of the led

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out portion of the wiring facing the lower electrode operates to form a part of the capacitance, therefore, when forming the capacitor, a high level of accuracy is required. In contrast, when the connecting portions 8 are used, the connecting portions do not affect the capacitance of the capacitor, thus, a highly accurate capacitor can be formed.

[0136] The manufacturing method of the electronic circuit component as shown in Fig.3 will be explained.

[0137] A sand blast use film resist material (product of Tokyo Ohka, Odale)of 100μ m was laminated on the glass substrate having thickness of 0.5mm through exposure and development process and an etching use resist was formed. Subsequently, through holes were formed in the glass substrate with micro sand blasting method. Then, the resist fil m was peeled off, electrolytic plating use seed films Cr:50nm, Cu:500nm were formed on the surface of the glass substrate and walls of the via holes with spattering method. Thereafter, on the Cu film, a plating use film resist(product of Hitachi Chemical Co., Ltd., HN 920) was laminated and a resist mask was formed through exposure and development, then, conductive layers were formed inside the via holes by Cu electrolytic plating . Subsequently, the resist and the electrolytic plating seed film were peeled off.

[0138] A Cr film of 50nm was formed on a glass substrate of 0.5 mm thickness with spattering method and further, a Cu film of 500nm was formed thereon, which was used for current feeding use seed film for Cu plating. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10 μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the lower electrode was formed.

[0139] Subsequently, as a barrier film, a Cr film of 50nm is formed with spattering method.

[0140] Then, Ta_2O_5 film having thickness of 500nm was formed on the lower electrode by spattering method. On the Ta_2O_5 film positive type liquid resist OFPR800, 500cp(product of Tokyo Ohka) was coated and after performing drying, exposing and developing process a resist mask for a dielectric layer was formed. Subsequently, a dry etch was performed by making use of CF_4 to remove unnecessary portion thereof and further, unnecessary portion of the barrier layer was removed with Cr etching liquid of permanganic acid, then, the resist mask was removed and the dielectric layer was formed.

[0141] Subsequently, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the dielectric layer over the lower electrode was exposed. In this instance, the polyimide layer was opened so that the end portion of the opening was located at the inner side from the end of the lower electrode by 20 μm. The polyimide is hardened at 250° C/2 hours under nitrogen atmosphere to form the organic insulator of 10 μm.

[0142] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the upper electrodes were formed.

[0143] On the plane where the upper electrodes were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portion for interlayer connection was formed and the polyimide was hardened at 250° C/1 hour to form the organic insulator.

[0144] Then, a TaN film of 500nm was formed with spattering method. On the film positive type liquid state resist OFPR 800,100cp was spin-coated and prebaked, thereafter, a resist pattern mask was formed through exposure and development. By using the mask The TaN film was dry etched with CF_4. Then, a plurality of resistor elements were formed by peeling off the resist.

[0145] A Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the electrodes for the resistors were formed.

[0146] On the plane where the electrodes for the resistor were formed, photosensitive polyimide HD 6000 (product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portion for interlayer connection was formed and the polyimide was hardened at 250° C/1 hour to form the organic insulator.

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[0147] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the inductor elements, wirings and metal terminal portions were formed.

[0148] On the plane where the metal terminal portions, inductor elements and wirings were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portions for forming the solder balls were formed and the polyimide was hardened at 250° C/1 hour to form the organic insulator.

[0149] After applying electroless gold plating on the surface of the metal terminal portion and then coating solder flux on a predetermined portion with a metal mask, the external electrodes were formed by arranging the lead free solder balls having a diameter of 200 μm and performing reflow processing.

[0150] Finally, the product was separated by a dicing machine to form the electronic circuit components.

[0151] In the present embodiment, since the capacitor elements, inductor elements and resistor elements are respectively arranged at a plurality of different distances from the surface of the glass substrate, the respective elements can be integrated in further high density, therefore, a further small sized electronic circuit component can be obtained in addition to the advantages obtained in embodiment 5.

[0152] Further, through the use of the glass used in embodiment 2, the electronic circuit component of course shows a high reliability such as in connection with impact resistance.

[0153] Through the use of BCB organic insulator used in embodiment 3 for the organic insulator in the present embodiment, the conductive loss and dielectric loss are reduced, thereby, an electronic circuit component having a small signal transmission loss can be obtained.

[0154] Further, by using the low dielectric loss tangent resin composition as used in embodiment 4 as the insulator layer, the conductive loss and dielectric loss are reduced, thereby, loss of signals transmitting through the electronic circuits can be reduced with the low cost material.

[0155] Further, Fig.3 structure is one embodiment of the present invention, and the arrangement of the respective elements is not limited to that shown.

(Embodiment 7)

[0156] As the seventh embodiment, an example of an electronic circuit component in which an LC filter circuit as shown in Fig.5 is formed in one chip. Fig.6 is a cross sectional view of the electronic circuit component representing an embodiment of the present invention. Fig. 7 is an exploded view of the electronic circuit component according to the present embodiment. Further, Figs.8 through 14 are plane views of the respective layers as shown in the exploded view of Fig.7. Still further, the cross sectional view in Fig.6 shows one being taken along the dotted line A-A' in Figs.8 through14.

[0157] In Figs.6 and 7, 26 is a glass substrate (product of Nihon Denki Glass, BLC) and of which thickness was 0.5mm and size was 2mm x 2mm. 27 is a lower electrode layer made of Cu and of which plane view is shown in Fig.8. 28 is a dielectric body layer made of oxide of Ta and of which plane view is shown in Fig.9. 29 is an organic insulator layer and of which plane view is shown in Fig.10. 30 is a layer serving as an inductor layer and an upper electrode and of which plane view is shown in Fig.11. 31 is another organic insulator and of which plane view is shown in Fig.12. 32 is an electrode layer for connecting between a wiring and an external terminal and of which plane view is shown in Fig.13. 33 is a surface protective layer made of an organic insulator a nd of which plane view is shown in Fig.14. 34 is an external electrode for a solder ball. The lower electrode 27 made of Cu, the layer 30 serving as the inductor layer and the upper electrode and the electrode layer 32 connecting the wiring and the external terminal are connected through via holes formed in the organic insulator layers 29 and 31 provided in the respective interlayers.

[0158] The manufacturing method of the electronic circuit component will be explained.

[0159] A Cr film of 50nm was formed on a glas s substrate 26 of 0.5 mm thickness with spattering method and further, a Cu film of 500nm was formed thereon, which was used for current feeding use seed film for Cu plating. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10 μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the lower electrode 27 was formed. The lower electrode layer 27 serves as a lower electrode and a wiring for a capacitor element.

[0160] Subsequently, as a barrier film, a Cr film of 50nm is formed with spattering method.

[0161] Then, Ta_2O_5 film having thickness of 500nm was formed on the lower electrode by spattering meth-

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od. On the Ta_2O_5 film positive type liquid resist OFPR800, 500cp(product of Tokyo Ohka) was coated and after performing drying, exposing and developing process a resist mask for a dielectric layer was formed. Subsequently, a dry etch was performed by making use of CF_4 to remove unnecessary portion thereof and further, unnecessary portion of the barrier layer was removed with Cr etching liquid of permanganic acid, then, the resist mask was removed and the dielectric layer 28 was formed. In this instance, the dielectric layer 28 was formed so as to cover the side face of the lower electrode.

[0162] Subsequently, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the dielectric layer over the lower electrode was exposed. In this instance, the polyimide layer was opened so that the end portion of the opening was located at the inner side from the end of the lower electrode by 20μm. The polyimide is hardened at 250° C/2 hours under nitrogen atmosphere to form the organic insulator layer 29 of 10μm. Further, in the organic insulator layer 29 via holes are formed for connecting the lower electrode layer 27 and a wiring on the upper layer thereof.

[0163] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the upper electrode and the inductor element 30 were formed. Herein, through forming the upper electrode and the inductor element on the same layer, the distance between the inductor element and the capacitor element is shortened, thereby, the size and noise reduction of the electronic circuit component is achieved with a high efficiency and a high performance. Further, in the present embodiment, as shown in the plane view of Fig. 11, a capacitor element is formed even in the area of the inductor element. Through such arrangement, the distance between the inductor element and the capacitor element is shortened and the occupying area of the capacitor element is saved which permits size reduction of the electronic circuits.

[0164] On the plane where the upper electrode and the inductor element 30 were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portion for interlayer connection was formed and the polyimide was hardened at 250° C/1 hour to form the organic insulator layer 31. Herein, since the opening portion for performing the interlayer connection between the upper electrode and the upper layer thereof is formed so as to locate in the face where the upper electrode is formed, the area of the upper electrode for the capacitor element can be easily controlled, which enhances accuracy of the capacitor element.

[0165] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the wirings and external electrode layer 32 were formed.

[0166] On the plane where the wiring and external electrode layer 32 metal end portions were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portion for solder balls were formed and the polyimide was hardened at 250° C/1 hour to form the organic insulator layer 33.

[0167] After applying electroless gold plating on the surface of the wiring and external electrode and then coating solder flux on a predetermined portion with a metal mask, the external electrodes 34 were formed by arranging the lead free solder balls having a diameter of 200 μm and performing reflow processing. The external electrode 34 is arranged in a grid shape as shown in Fig.7 so as to ease mounting such as on an external wiring substrate.

[0168] Finally, the product was separated by a dicing machine to form the electronic circuit components.

[0169] In the present embodiment, since the LC filter circuit, which was conventionally formed as a single discrete component is integrated on a substrate, the size, resistance, inductance and noise of the electronic circuit component can be realized.

[0170] Further, through the use of the glass used in embodiment 2, the electronic circuit component of course shows a high reliability such as in connection with impact resistance.

[0171] Through the use of BCB organic insulator used in embodiment 3 for the organic insulator in the present embodiment, the conductive loss and dielectric loss are reduced, thereby, an electronic circuit component having a small signal transmission loss can be obtained.

[0172] Further, by using the low dielectric loss tangent

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resin composition as used in embodiment 4 as the insulator layer, the conductive loss and dielectric loss are reduced, thereby. loss of signals transmitting through the electronic circuits can be reduced with the low cost material.

[0173] Further, Fig.5 structure is one embodiment of the present invention, and the arrangement of the respective elements is not limited to that shown.

(Embodiment 8)

[0174] Fig.15 is a cross sectional view of an electronic circuit component representing one embodiment of the present invention. In Fig.15, 1 is a glass substrate (product of Nippon Electric Glass Co., Ltd.,BLC), and the thickness of which is 0.5mm.

[0175] In Fig.15, 2 is an organic insulator and photosensitive polyimide (product of Hitachi Chemical Co., Ltd., HD-6000) is used therefor.

[0176] Capacitor elements formed inside the organic insulator 2 are constituted by a capacitor 3 in a three layer structure constituted by a lower electrode 3a of Cu, a dielectric body 3b of oxide of Ta and an upper electrode 3c of Cu and a capacitor 3' in a three layer structure constituted by a lower electrode 3'a of Cu, a dielectric body 3'b of polyimide and an upper electrode 3'c of Cu. Further, on the upper electrodes connecting portions 8 for connecting the same with the upper wirings are provided.

[0177] An inductor element 4 is a spiral type inductor and is formed of Cu.

[0178] A resistor 5 is constituted by a resistance body 5b and electrodes 5a and 5 c. The resistance body 5b is a compound of Ta and Ti and the electrodes 5a and 5c are composed of Cu.

[0179] In Fig.15, 9 is an organic insulator having a function of buffering stress. For the organic insulator having the stress buffering function, a liquid polyimide material in which polyimide fine particles are dispersed (product of Hitachi Chemical Co., Ltd., GH-P500) was used.

[0180] In Fig.15, 6 is a metal terminal portion used for connection with a mounting substrate such as a print substrate and in the drawing a solder ball 7 is mounted on the metal terminal portion 6.

[0181] The manufacturing method of the electronic circuit component as shown in Fig. 15 will be explained.

[0182] A Cr film of 50nm was formed on a glass substrate of 0.5 mm thickness with spattering method and further, a Cu film of 500nm was formed thereon, which was used for current feeding use seed film for Cu plating. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10 μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the lower electrode was formed.

[0183] Subsequently, as a barrier film, a Cr film of 50nm is formed with spattering method.

[0184] Then, Ta_2O_5 film having thickness of 500nm was formed on the lower electrode by spattering method. On the Ta_2O_5 film positive type liquid resist OFPR800, 500cp(product of Tokyo Ohka) was coated and after performing drying, exposing and developing process a resist mask for a dielectric layer was formed. Subsequently, a dry etch was performed by making use of CF_4 to remove unnecessary portion thereof and further, unnecessary portion of the barrier layer was removed with Cr etching liquid of permanganic acid, then, the resist mask was removed and the dielectric layer was formed.

[0185] Subsequently, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the dielectric layer over the lower electrode was exposed. In this instance, the polyimide layer was opened so that the end portion of the opening was located at the inner side from the end of the lower electrode by 20μm. The polyimide is hardened at 250° C/2 hours under nitrogen atmosphere to form the organic insulator of 10μm.

[0186] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMEF3-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the upper electrodes were formed.

[0187] On the plane where the upper electrodes were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portion for interlayer connection was formed and the polyimide was hardened at 250° C/1 hour to form the organic insulator.

[0188] Then, a TaN film of 500nm was formed with spattering method. On the film, positive type liquid state resist OFPR800, 100cp was spin-coated and prebaked, thereafter, a resist pattern mask was formed through exposure and development. By using the mask The TaN film was dry etched with CF_4. Then, a plurality of resistor elements were formed by peeling off the resist.

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[0189] A Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the electrodes for the resistors were formed.

[0190] On the plane where the electrodes for the resistor were formed, photosensitive polyimide HD 6000 (product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portion for interlayer connection was formed and the polyimide was hardened at 250° C/1 hour to form the organic insulator.

[0191] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the inductor elements and wirings were formed.

[0192] Thereafter, the liquid polyimide material GH-P 500 in which polyimide fine particles are dispersed (product of Hitachi Chemical Co., Ltd.) was print coated by using a mask, heated on a hot plate at 200°C/25min and hardened in a constant temperature bath at 250°C/60min to form the organic insulator having stress buffering function.

[0193] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, wh ich was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the wirings and metal end portions were formed.

[0194] On the plane where the wiring and metal end portions were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portion for solder balls were formed and the polyimide was hardened at 250° C/1 hour to form the organic insulator.

[0195] After applying electroless gold plating on the surface of the metal terminal portion and then coating solder flux on a predetermined portion with a metal mask, the external electrodes were formed by arranging the lead free solder balls having a diameter of 200μm and performing reflow processing.

[0196] Finally, the product was separated by a dicing machine to form the electronic circuit components.

[0197] In the present embodiment, since the organic insulator having stress buffering function is formed immediately below the metal terminal portion 6, when being connected to a mounting substrate such as a print substrate, a thermal stress applied to the metal terminal portion 6 and the solder ball 7 due to difference of thermal expansion coefficients between the semiconductor connection substrate and the mounting substrate can be relaxed. Thereby, a semiconductor connection substrate having excellent heart resistance cycle can be obtained in addition to the advantages obtained in embodiment 6.

[0198] Further, through the use of the glass used in embodiment 2, the electronic circuit component of course shows a high reliability such as in connection with impact resistance.

[0199] Through the use of BCB organic insulator used in embodiment 3 for the organic insulator in the present embodiment, the conductive loss and di electric loss are reduced, thereby, an electronic circuit component having a small signal transmission loss can be obtained.

[0200] Further, by using the low dielectric loss tangent resin composition as used in embodiment 4 as the insulator layer, the conductive loss and dielectric loss are reduced, thereby, loss of signals transmitting through the electronic circuits can be reduced with the low cost material.

[0201] Further, Fig. 15 structure is one embodiment of the present invention, and the arrangement of the respective elements is not limited to that shown.

(Embodiment 9)

[0202] Fig.16 is a cross sectional view of an electronic circuit component representing one embodiment of the present invention. In Fig.16, 1 is a glass substrate (product of Nippon Electric Glass Co., Ltd.,BLC), and the thickness of which is 0.5mm.

[0203] In Fig.16, 2 is an organic insulator and photosensitive polyimide (product of Hitachi Chemical Co., Ltd.,HD-6000) is used therefor.

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[0204] All of capacitor elements 3 formed inside the org anic insulator 2 are in a three layer structure constituted by a lower electrode 3a, a dielectric body 3b and an upper electrode 3c. The lower electrode 3a is constituted of Cu, the dielectric body 3b of oxide of Ta and the upper electrode 3c of Cu.

[0205] An inductor element 4 is a spiral type inductor and is formed on the same plane as the upper electrode 3c of the capacitor element 3 and the material thereof is Cu.

[0206] A resistor 5 is constituted by a resistance body 5b and electrodes 5a and 5 c. The resistance body 5b is a compound of Ta and Ti and the electrodes 5a and 5c are composed of Cu.

[0207] In Fig. 16, 12 is another insulator using photosensitive polyimide (product of Hitachi Chemical Co., Ltd., HD-6000).

[0208] All of capacitor elements 13 formed inside the organic insulator 12 are in a three layer structure constituted by a lower electrode 13a, a dielectric body 13b and an upper electrode 13c. The lower electrode 13a is constituted of Cu, the dielectric body 13b of oxide of Ta and the upper electrode 13c of Cu.

[0209] An inductor element 14 is a spiral type inductor and is formed on the same plane as the upper electrode 13c of the capacitor element 13 and the material thereof is Cu.

[0210] A resistor 15 is constituted by a resistance body 15b and electrodes 15a and 15 c. The resistance body 15b is a compound of Ta and Ti and the electrodes 15a and 15c are composed of Cu.

[0211] In Fig.16, the respective elements formed inside the organic insulators 2 and 12 are electrically connected via conductor portions filled in through holes 20 formed in the glass substrate so as to provide a predetermined functions.

[0212] In Fig.16, 6 is a metal terminal portion used for connection with a mounting substrate such as a print substrate and in the drawing a solder ball 7 is mounted on the metal terminal portion 6.

[0213] The manufacturing method of the electronic circuit component as shown in Fig.16 will be explained.

[0214] A sand blast use film resist material(product of Tokyo Ohka, Odale)of 100μ m was laminated on the glass substrate having thickness of 0.5mm through exposure and development process and an etching use resist was formed. Subsequently, through holes were formed in the glass substrate with micro sand blasting method. Then, the resist film was peeled off, electrolytic plating use seed films Cr: 50nm, Cu: 500nm were formed on the surface of the glass substrate and walls of the via-holes with spattering method. Thereafter, on the Cu film, a plating use film resist (product of Hitachi Chemical Co., Ltd., HN 920) was laminated and a resist mask was formed through exposure and development, then, conductive layers were formed inside the via holes by Cu electrolytic plating. Subsequently, the resist and the electrolytic plating seed film were peeled off.

[0215] A Cr film of 50nm was formed on the main surface of a glass substrate spattering method and further, a Cu film of 500nm was formed thereon, which was used for current feeding use seed film for Cu plating. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10 μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the lower electrode was formed.

[0216] Subsequently, as a barrier film, a Cr film of 50nm is formed with spattering method.

[0217] Then, Ta_2O_5 film having thickness of 500nm was formed on the lower electrode by spattering method. On the Ta_2O_5 film positive type liquid resist OFPR800, 500cp(product of Tokyo Ohka) was coated and after performing drying, exposing and developing process a resist mask for a dielectric layer was formed. Subsequently, dry etch was performed by making use of CF_4 to remove unnecessary portion thereof and further, unnecessary portion of the barrier layer was removed with Cr etching liquid of permanganic acid, then, the resist mask was removed and the dielectric layer was formed.

[0218] Subsequently, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the dielectric layer over the lower electrode was exposed. In this instance a covering portion of the polyimide was opened inside from the scribe area by 80μm used for cutting into pieces as the electronic circuit components. The ployimide was hardened at 250°C/2hours under nitrogen atmosphere to form the organic insulator of 10μm.

[0219] Then, a TaN film of 500nm was formed with spattering method. On the film positive type liquid state resist OFPR 800,100cp was spin-coated and prebaked, thereafter, a resist pattern mask was formed through exposure and development. By using the mask The TaN film was dry etched with CF_4. Then, a plurality of resistor elements were formed by peeling off the resist.

[0220] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with cop-

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per etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the upper electrode, electrodes for the resistors and the inductor element were formed.

[0221] On the plane where the upper electrode, the electrodes for the resistor and the inductor were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, the same was exposed and developed. In this instance the polyimide covering portion was opened so that the polyimide covering portion comes inside by 80μm from the scribe area used for cutting into pieces as the semiconductor connection substrates. The polyimide having the opening was hardened at 250 ° C/1 hour under nitrogen atmosphere and the organic insulator was formed.

[0222] A Cr film of 50nm was formed on the back surface of the glass substrate with spattering method and further, a Cu film of 500nm was formed thereon, which was used for current feeding use seed film for Cu plating. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10 μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the lower electrode was formed.

[0223] Subsequently, as a barrier film, a Cr film of 50nm is formed with spattering method.

[0224] Then, Ta_2O_5 film having thickness of 500nm was formed on the lower electrode by spattering method. On the Ta_2O_5 film positive type liquid resist OFPR800, 500cp(product of Tokyo Ohka) was coated and after performing drying, exposing and developing process a resist mask for a dielectric layer was formed. Subsequently, dry etch was performed by making use of CF_4 to remove unnecessary portion thereof and further, unnecessary portion of the barrier layer was removed with Cr etching liquid of permanganic acid, then, the resist mask was removed and the dielectric layer was formed.

[0225] Subsequently, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the dielectric layer over the lower electrode was exposed. In this instance the polyimide having an opening is hardened at 250° C/2 hours under nitrogen atmosphere and the organic insulator of 10μm was formed so that the polyimide covering portion comes inside by 80 μ m from the scribe area used for cutting into pieces as the electronic circuit components.

[0226] Then, a TaN film of 500nm was formed with spattering method. On the film positive type liquid state resist OFPR 800,100cp was spin-coated and prebaked, thereafter, a resist pattern mask was formed through exposure and development. By using the mask The TaN film was dry etched with CF_4. Then, a plurality of resistor elements were formed by peeling off the resist.

[0227] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the upper electrode, electrodes for the resistors and the inductor element were formed.

[0228] On the plane where the upper electrode, the electrodes for the resistor and the inductor were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portion for interlayer connection was formed. In this instance the polyimide having an opening is hardened at 250° C/1 hour under nitrogen atmosphere and the organic insulator was formed so that the polyimide covering portion comes inside by 80 μm from the scribe area used for cutting into pieces as the electronic circuit components.

[0229] In order to form the metal terminal portion on the organic insulator surface the electrolytic plating use seed films Cr:50nm, Cu:500nm were formed. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated and prebaked, thereafter, a resist mask for plating was formed through exposure and development then, a plating film of 10 μm was formed by Cu electrolytic plating and further, an electrolytic nickel plating film of 2μm was formed. Finally, after peeling off the resist and the electrolytic plating seed film, the wirings and the metal terminal portions were formed.

[0230] On the plane where the metal terminal portions were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portions for forming the solder balls were formed. In this instance the polyimide having an opening is hardened at 250° C/1 hour under nitrogen atmosphere and the organic insulator was formed so that the polyimide covering portion comes inside by 80 μm from the scribe area used for cutting into pieces as the semiconductor connection

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substrates.

[0231] After applying electroless gold plating on the surface of the metal terminal portion and then coating solder flux on a predetermined portion with a metal mask, the external electrodes were formed by arranging the lead free solder balls having a diameter of 200 μm and performing reflow processing.

[0232] Finally, the product was separated by a dicing machine to form the electronic circuit components.

[0233] According to the present embodiment, in addition to the advantages obtained in embodiment 1, since the elements were integrated on both surfaces of the glass substrate having the through holes, the integration rate was doubled in comparison with the conventional ones in which the elements were integrated on one face of the substrate, which further reduces the size of the electronic circuit component.

[0234] Further, through the use of the glass used in embodiment 2, the electronic circuit component of course shows a high reliability such as in connection with impact resistance.

[0235] Through the use of BCB organic insulator used in embodiment 3 for the organic insulator in the present embodiment, the conductive loss and dielectric loss are reduced, thereby, an electronic circuit component having a small signal transmission loss can be obtained.

[0236] Further, by using the low dielectric loss tangent resin composition as used in embodiment 4 as the insulator layer, the conductive loss and dielectric loss are reduced, thereby, loss of signals transmitting through the electronic circuits can be reduced with the low cost material.

[0237] Further, Fig. 16 structure is one embodiment of the present invention, and the arrangement of the respective elements is not limited to that shown.

(Embodiment 10)

[0238] Fig.17 is a cross sectional view of an electronic circuit component representing an embodiment of the present invention. In Fig.17, 22 is a photosensitive glass substrate, 23 a through hole and 24 a conductive portion formed inside the through hole. Further, in Fig.17, portions other than the photosensitive glass substrate 22, through hole 23 and conductive portion 24 are the same as those in embodiment 9.

[0239] Further, the manufacturing method of the electronic circuit compon ent as shown in Fig.17 is the same as that of embodiment 9 except for the through hole formation method which will be explained below.

[0240] For the photosensitive glass substrate a photosensitive glass series of Li_2-Al_2O_3-SiO_2 (Au,Ce) is used. On the main face of the photosensitive glass substrate a mask on which a through hole pattern was drawn by Cr was closely contacted and was exposed by using an Hg-Xe lamp. Thereafter, being developed and crystallized and a glass substrate having through holes were obtained.

[0241] When the photosensitive glass is used, the wall face of the through hole becomes more vertical, in other words, the taper angle thereof is enlarged in comparison with other through hole formation methods such as the sand blasting method, which permits formation of further fine through holes. Accordingly, in the present embodiment, the elements can be integrated in further high integration degree, thereby, an equivalent integration degree can be achieved with about halved area in comparison with embodiment 7 or 8.

[0242] As will be seen from the above, when the photosensitive glass substrate is used, an electronic circuit component of a high integration degree can be obtained with a low cost in addition to the advantages of embodiment 9.

[0243] Further, Fig.17 structure is one embodiment of the present invention, and the arrangement of the respective elements is not limited to that shown.

(Embodiment 11)

[0244] Fig.18 is a cross sectional view of a semiconductor connection substrate representing one embodiment of the present invention. In Fig. 18, 1 is a glass substrate (product of Nippon Electric Glass Co., Ltd., BLC), and the thickness of which is 0.5mm.

[0245] In Fig.18, 2 is an organic insulator and photosensitive polyimide (product of Hitachi Chemical Co., Ltd.,HD-6000) is used therefor.

[0246] Capacitor elements formed inside the organic insulator 2 are constituted by a capacitor 3 in a three layer structure constituted by a lower electrode 3a of Cu, a dielectric body 3b of oxide of Ta and an upper e lectrode 3c of Cu and a capacitor 3' in a three layer structure constituted by a lower electrode 3 'a of Cu, a dielectric body 3'b of polyimide and an upper electrode 3'c of Cu.

[0247] An inductor element 4 is a spiral type inductor and the material thereof is Cu.

[0248] A resistor 5 is constituted by a resistance body 5b and electrodes 5a and 5 c. The resistance body 5b is a compound of Ta and T i and the electrodes 5a and 5c are composed of Cu.

[0249] In Fig. 18, 12 is another insulator using photosensitive polyimide (product of Hitachi Chemical Co., Ltd., HD-6000).

[0250] Capacitor elements formed inside the organic insulator 12 are constituted by a capacitor 13 in a three layer structure constituted by a lower electrode 13a of Cu, a dielectric body 13b of oxide of Ta and an upper electrode 13c of Cu and a capacitor 13' in a three layer structure constituted by a lower electrode 13'a of Cu, a dielectric body 13'b of polyimide and an upper electrode 13'c of Cu.

[0251] An inductor element 14 is a spiral type inductor and the material thereof is Cu.

[0252] A resistor 15 is constituted by a resistance body 15b and electrodes 15a and 15 c. The resistance

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body 15b is a compound of Ta and Ti and the electrodes 15a and 15c are composed of Cu.

[0253] In Fig.18, the respective elements formed inside the organic insulators 2 and 12 are electrically connected via conductor portions filled in through holes 20 formed in the glass substrate so as to provide a predetermined functions.

[0254] In Fig. 18, 6 is a metal terminal portion used for connection with an external terminal and in the drawing a solder ball 7 is mounted on the metal terminal portion 6.

[0255] The manufacturing method of the electronic circuit component as shown in Fig.18 will be explained.

[0256] A sand blast use film resist (product of Tokyo Ohka, Odale)of 100μm was laminated on the glass substrate having thickness of 0.5mm through exposure and development process and an etching use resist was formed. Subsequently, through holes were formed in the glass substrate with micro sand blasting method. Then, the resist film was peeled off, electrolytic plating use seed films Cr:50nm, Cu:500nm were formed on the surface of the glass substrate and walls of the via holes with spattering method. Thereafter, on the Cu film a plating use fi lm resist (product of Hitachi Chemical Co., Ltd., HN 920) was laminated and a resist mask was formed through exposure and development, then, conductive layers were formed inside the via holes by Cu electrolytic plating . Subsequently, the resist and the electrolytic plating seed film were peeled off.

[0257] A Cr film of 50nm was formed on the main surface of a glass substrate spattering method and further, a Cu film of 500nm was formed thereon, which was used for current feeding use seed film for Cu plating. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10 μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the lower electrode was formed.

[0258] Subsequently, as a barrier film, a Cr film of 50nm is formed with spattering method.

[0259] Then, Ta_2O_5 film having thickness of 500nm was formed on the lower electrode by spattering method. On the Ta_2O_5 film positive type liquid resist OFPR800, 500cp(product of Tokyo Ohka) was coated and after performing drying, exposing and developing process a resist mask for a dielectric layer was formed. Subsequently, dry etch was performed by making use of CF_4 to remove unnecessary portion thereof and further, unnecessary portion of the barrier layer was removed with Cr etching liquid of permanganic acid, then, the resist mask was removed and the dielectric layer was formed.

[0260] Subsequently, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the dielectric layer over the lower electrode was exposed. In this instance a covering portion of the polyimide was opened inside from the scribe area by 80μm used for cutting into pieces as the electronic circuit components. The ployimide was hardened at 250°C/2hours under nitrogen atmosphere to form the organic insulator of 10μm.

[0261] Then, a TaN film of 500nm was formed with spattering method. On the film positive type liquid state resist OFPR 800,100cp was spin-coated and prebaked, thereafter, a resist pattern mask was formed through exposure and development. By using the mask The TaN film was dry etched with CF_4. Then, a plurality of resistor elements were formed by peeling off the resist.

[0262] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist openi ng portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the upper electrode, electrodes for the resistors and the inductor element were formed.

[0263] On the plane where the upper electrode, the electrodes for the resistor and the inductor element were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, the same was exposed and developed. In this instance the polyimide having an opening is hardened at 250° C/1 hour under nitrogen atmosphere and the organic insulator was formed so that the polyimide covering portion comes inside by 80μm from the scribe area used for cutting into pieces as the electronic circuit components.

[0264] A Cr film of 50nm was formed on the back surface of the glass substrate with spattering method and further, a Cu film of 500nm was formed thereon, which was used for current feeding use seed film for Cu plating. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10 μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Den-

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san). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the lower electrode was formed.

[0265] Subsequently, as a barrier film, a Cr film of 50nm is formed with spattering method.

[0266] Then, Ta_2O_5 film having thickness of 500nm was formed on the lower electrode by spattering method. On the Ta_2O_5 film positive type liquid resist OFPR800, 500cp(product of Tokyo Ohka) was coated and after performing drying, exposing and developing process a resist mask for a dielectric layer was formed. Subsequently, dry etch was performed by making use of CF_4 to remove unnecessary portion thereof and further, unnecessary portion of the barrier layer was removed with Cr etching liquid of permanganic acid, then, the resist mask was removed and the dielectric layer was formed.

[0267] Subsequently, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the dielectric layer over the lower electrode was exposed. In this instance the polyimide having an opening is hardened at 250° C/2 hours under nitrogen atmosphere and the organic insulator of 10μm was formed so that the polyimide covering portion comes inside by 80 μ m from the scribe area used for cutting into pieces as the electronic circuit components.

[0268] Then, a TaN film of 500nm was formed with spattering method. On the film positive type liquid state resist OFPR 800,100cp was spin-coated and prebaked, thereafter, a resist pattern mask was formed through exposure and development. By using the mask The TaN film was dry etched with CF_4. Then, a plurality of resistor elements were formed by peeling off the resist.

[0269] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, whi ch was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the upper electrode, electrodes for the resistors and the inductor element were formed.

[0270] On the plane where the upper electrode, the electrodes for the resistor and the inductor element were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portion for interlayer connection was formed. In this instance the polyimide having an opening is hardened at 250° C/1 hour under nitrogen atmosphere and the organic insulator was formed so that the polyimide covering portion comes inside by 80 μ m from the scribe area used for cutting into pieces as the electronic circuit components.

[0271] In order to form the metal terminal portion on the organic insulator surface the electrolytic plating use seed films Cr:50nm, Cu:500nm were formed. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated and prebaked, thereafter, a resist mask for plating was formed through exposure and development then, a plating film of 10μm was formed by Cu electrolytic plating and further, an electrolytic nickel plating film of 2μm was formed. Finally, after peeling off the resist and the electrolytic plating seed film, the wirings and the metal terminal portions were formed.

[0272] On the plane where the metal terminal portions were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portions for forming the solder balls were formed. In this instance the polyimide having an opening is hardened at 250° C/1 hour under nitrogen atmosphere and the organic insulator was formed so that the polyimide covering portion comes inside by 80 μm from the scribe area used for cutting into pieces as the electronic circuit components.

[0273] After applying electroless gold plating on the surface of the metal terminal portion and then coating solder flux on a predetermined portion with a metal mask, the external electrodes were formed by arranging the lead free solder balls having a diameter of 200 μm and performing reflow processing.

[0274] Finally, the product was separated by a dicing machine to form the electronic circuit components.

[0275] In the present embodiment, through the use of the inorganic material having a high dielectric constant such as the oxide of Ta as well as the organic material having a low dielectric constant such as the polyimide as the dielectric body material, capacitors having a small capacitance can be formed accurately, which enhances reliability of the circuits and expands available capacitance range. Further, through the use of the same material for the dielectric body as the insulator material, which covers the circumference of the elements, the electronic circuit component can be manufactured in further simplified and low cost processes in addition to the advantages obtained in embodiment 9.

[0276] Further, through the use of the glass used in embodiment 2, the electronic circuit component of course shows a high reliability such as in connection with impact resistance.

[0277] Further, through the use of the photosensitive glass substrate as used in embodiment 10 a low cost electronic circuit component having further high integration degree can be of course obtained.

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[0278] Through the use of BCB organic insulator used in embodiment 3 for the organic insulator in the present embodiment, the conductive loss and dielectric loss are reduced, thereby, an electronic circuit component having a small signal transmission loss can be obtained.

[0279] Further, by using the low dielectric loss tangent resin composition as used in embodiment 4 as the insulator layer, the conductive loss and dielectric loss are reduced, thereby, loss of signals transmitting through the electronic circuits can be reduced with the low cost material.

[0280] Further, Fig.18 structure is one embodiment of the present invention, and the arrangement of the respective elements is not limited to that shown.

(Embodiment 12)

[0281] Fig.19 is a cross sectional view of a semiconductor connection substrate representing one embodiment of the present invention. In Fig. 19, 1 is a glass substrate (product of Nippon Electric Glass Co., Ltd., BLC), and the thickness of which is 0.5mm.

[0282] In Fig.19, 2 is an organic insulator and photosensitive polyimide (product of Hitachi Chemical Co., Ltd., HD-6000) is used therefor.

[0283] Capacitor elements formed inside the organic insulator 2 are constituted by a capacitor 3 in a three layer structure constituted by a lower electrode 3a of Cu, a dielectric body 3b of oxide of Ta and an upper electrode 3c of Cu and a capacitor 3' in a three layer structure constituted by a lower electrode 3'a of Cu, a dielectric body 3'b of polyimide and an upper electrode 3'c of Cu.

[0284] In Fig.19, 12 is another insulator using photosensitive polyimide(product of Hitachi Chemical Co., Ltd., HD-6000).

[0285] An inductor element 14 is a spiral type inductor and the material thereof is Cu.

[0286] A resistor 15 is constituted by a resistance body 15b and electrodes 15a and 15 c. The resistance body 15b is a compound of Ta and Ti and the electrodes 15a and 15c are composed of Cu.

[0287] In Fig.19, the respective elements formed inside the organic insulators 2 and 12 are electrically connected via conductor portions filled in through holes 20 formed in the glass substrate so as to provide a predetermined functions.

[0288] In Fig.19, 6 is a metal terminal portion used for connection with a n external terminal and in the drawing a solder ball 7 is mounted on the metal terminal portion 6.

[0289] The manufacturing method of the elecronic circuit component as shown in Fig.19 will be explained.

[0290] A sand blast use film resist (product of Tokyo Ohka, Odale)of 100μm was laminated on the glass substrate having thickness of 0.5mm through exposure and development process and an etching use resist was formed. Subsequently, through holes were formed in the glass substrate with micro sand blasting method. Then, the resist film was peeled off, electrolytic plating use seed films Cr:50nm, Cu:500nm were formed on the surface of the glass substrate and walls of the via holes with spattering method. Thereafter, on the Cu film a plating use film resist (product of Hitachi Chemical Co., Ltd., HN 920) was laminated and a resist mask was formed through exposure and development, then, conductive layers were formed inside the via holes by Cu electrolytic plating. Subsequently, the resist and the electrolytic plating seed film were peeled off.

[0291] A Cr film of 50nm was formed on the main surface of a glass substrate spattering method and further, a Cu film of 500nm was formed thereon, which was used for current feeding use seed film for Cu plating. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10 μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the lower electrode was formed.

[0292] Subsequently, as a barrier film, a Cr film of 50nm is formed with spattering method.

[0293] Then, Ta_2O_5 film having thickness of 500nm was formed on the lower electrode by spattering method. On the Ta_2O_5 film positive type liquid resist OFPR800, 500cp(product of Tokyo Ohka) was coated and after performing drying, exposing and developing process a resist mask for a dielectric layer was formed. Subsequently, dry etch was performed by making use of CF_4 to remove unnecessary portion thereof and further, unnecessary portion of the barrier layer was removed with Cr etching liquid of permanganic acid, then, the resist mask was removed and the dielectric layer was formed.

[0294] Subsequently, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the dielectric layer over the lower electrode was exposed. In this instance a covering portion of the polyimide was opened inside from the scribe area by 80μm used for cutting into pieces as the electronic circuit components. The ployimide was hardened at 250°C/2hours under nitrogen atmosphere to form the organic insulator of 10μm.

[0295] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and develop-

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ment steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the upper electrodes were formed.

[0296] On the plane where the upper electrodes were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, the same was exposed and developed. In this instance the polyimide having an opening is hardened at 250 ° C/1 hour under nitrogen atmosphere and the organic insulator was formed so that the polyimide covering portion comes inside by 80 μm from the scribe area used for cutting into pieces as the electronic circuit components.

[0297] Then, on the back face of the glass substrate a TaN film of 500nm was formed with spattering method. On the film positive type liquid state resist OFPR 800,100cp was spin-coated and prebaked, thereafter, a resist pattern mask was formed through exposure and development. By using the mask The TaN film was dry etched with CF_4. Then, a plurality of resistor elements were formed by peeling off the resist.

[0298] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the electrodes for the resistors and the inductor element were formed.

[0299] On the plane where the electrodes for the resistor and the inductor element were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portion for interlayer connection was formed. In this instance the polyimide having an opening is hardened at 250° C/1 hour under nitrogen atmosphere and the organic insulator was formed so that the polyimide covering portion comes inside by 80μm from the scribe area used for cutting into pieces as the electronic circuit components.

[0300] In order to form the metal terminal portion on the organic insulator surface the electrolytic plating use seed films Cr:50nm, Cu:500nm were formed. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated and prebaked, thereafter, a resist mask for plating was formed through exposure and development then, a plating film of 10μm was formed by Cu electrolytic plating and further, an electrolytic nickel plating film of 2μm was formed. Finally, after peeling off the resist and the electrolytic plating seed film, the wirings and the metal terminal portions were formed.

[0301] On the plane where the metal terminal portions were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portions for forming the solder balls were formed. In thi s instance the polyimide having an opening is hardened at 250 ° C/1 hour and the organic insulator was formed so that the polyimide covering portion comes inside by 80μm from the scribe area used for cutting into pieces as the electronic circuit components.

[0302] After applying electroless gold plating on the surface of the metal terminal portion and then coating solder flux on a predetermined portion with a metal mask, the external electrodes were formed by arranging the lead free solder balls having a diameter of 200 μm and performing reflow processing.

[0303] Finally, the product was separated by a dicing machine to form the electronic circuit components.

[0304] In the present embodiment, as will be apparent from the above, since the respective elements are arranged on different faces, a possible influence of coupling between the respective elements can be reduced, thereby, the parasitic capacitance can be suppressed small and self oscillation frequencies of the respective elements can be increased, thus, in addition to the advantages obtained in embodiments 9 and 11 a high performance electronic circuit component can be obtained.

[0305] Further, through the use of the glass used in embodiment 2, the electronic circuit component of course shows a high reliability such as in connection with impact resistance.

[0306] Further, through the use of the photosensitive glass substrate as used in embodiment 10 a low cost electronic circuit component having further high integration degree can be of course obtained.

[0307] Through the use of BCB organic insulator used in embodiment 3 for the organic insulator in the present embodiment, the conductive loss and dielectric loss are reduced, thereby, an electronic circuit component having a small signal transmission loss can be obtained.

[0308] Further, by using the low dielectric loss tangent resin composition as used in embodiment 4 as the insulator layer, the conductive loss and dielectric loss are reduced, thereby, loss of signals transmitting through the electronic circuits can be reduced with the low cost material.

[0309] Further, Fig. 19 structure is one embodiment of the present invention, and the arrangement of the respective elements is not limited to that shown.

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(Embodiment 13)

[0310] Fig.20 is a cross sectional view of an electronic circuit component representing one embodiment of the present invention. In Fig.20, 1 is a glass substrate (product of Nippon Electric Glass Co., Ltd.,BLC), and the thickness of which is 0.5mm.

[0311] In Fig.20, 2 is an organic insulator and photosensitive polyimide (product of Hitachi Chemical Co., Ltd., HD-6000) is used therefor.

[0312] Capacitor elements formed inside the organic insulator 2 are constituted by a capacitor 3 in a three layer structure constituted by a lower electrode 3a of Cu, a dielectric body 3b of oxide of Ta and an upper electrode 3c of Cu and a capacitor 3' in a three layer structure constituted by a lower electrode 3'a of Cu, a dielectric body 3'b of polyimide and an upper electrode 3'c of Cu.

[0313] An inductor element 4 is a spiral type inductor and the material thereof is Cu.

[0314] A resistor 5 is constituted by a resistance body 5b and electrodes 5a and 5 c. The resistance body 5b is a compound of Ta and Ti and the electrodes 5a and 5c are composed of Cu.

[0315] In Fig.20, 12 is another insulator using photosensitive polyimide(product of Hitachi Chemical Co., Ltd., HD-6000).

[0316] Capacitor elements formed inside the organic insulator 12 are constituted by a capacitor 13 in a three layer structure constituted by a lower electrode 13a of Cu, a dielectric body 13b of oxide of Ta and an upper electrode 13c of Cu and a capacitor 13' in a three layer structure constituted by a lower electrode 13'a of Cu, a dielectric body 13'b of polyimide and an upper electrode 13'c of Cu.

[0317] An inductor element 14 is a spiral type inductor and the material thereof is Cu.

[0318] A resistor 15 is constituted by a resistance body 15b and electrodes 15a and 15 c. The resistance body 15b is a compound of Ta and Ti and the electrodes 15a and 15c are composed of Cu.

[0319] In Fig.20, the respective elements formed inside the organic insulators 2 and 12 are electrically connected via conductor portions filled in through holes 20 formed in the glass substrate so as to provide a predetermined functions.

[0320] In Fig.20, 6 is a metal terminal portion used for connection with a n external terminal and in the drawing a solder ball 7 is mounted on the metal terminal portion 6.

[0321] The manufacturing method of the electronic circuit component as shown in Fig.20 will be explained.

[0322] A sand blast use film resist (product of Tokyo Ohka, Odale)of 100μm was laminated on the glass substrate having thickness of 0.5mm through exposure and development process and an etching use resist was formed. Subsequently, through holes were formed in the glass substrate with micro sand blasting method. Then, the resist film was peeled off, electrolytic plating use seed films Cr: 50nm, Cu: 500nm were formed on the surface of the glass substrate and walls of the via-holes with spattering method. Thereafter, on the Cu film a plating use film resist (product of Hitachi Chemical Co., Ltd., HN 920) was laminated and a resist mask was formed through exposure and development, then, conductive layers were formed inside the via holes by Cu electrolytic plating. Subsequently, the resist and the electrolytic plating seed film were peeled off.

[0323] A Cr film of 50nm was formed on the main surface of a glass substrate spattering method and further, a Cu film of 500nm was formed thereon, which was used for current feeding use seed film for Cu plating. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10 μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the lower electrode was formed.

[0324] Subsequently, as a barrier film, a Cr film of 50nm is formed with spattering method.

[0325] Then, Ta_2O_5 film having thickness of 500nm was formed on the lower electrode by spattering method. On the Ta_2O_5 film positive type liquid resist OFPR800, 500cp(product of Tokyo Ohka) was coated and after performing drying, exposing and developing process a resist mask for a dielectric layer was formed. Subsequently, dry etch was performed by making use of CF_4 to remove unnecessary portion thereof and further, unnecessary portion of the barrier layer was removed with Cr etching liquid of permanganic acid, then, the resist mask was removed and the dielectric layer was formed.

[0326] Subsequently, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the dielectric layer over the lower electrode was exposed. In this instance, the polyimide layer was opened so that the end portion of the opening was located at the inner side from the end of the lower electrode by 20μm. The polyimide is hardened at 250° C/2 hours under nitrogen atmosphere to form the organic insulator of 10μm.

[0327] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic

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copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the upper electrodes were formed.

[0328] On the plane where the upper electrodes were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portion for interlayer connection was formed and the polyimide was hardened at 250° C/1 hour to form the organic insulator.

[0329] Then, a TaN film of 500nm was formed with spattering method. On the film positive type liquid state resist OFPR 800,100cp was spin-coated and prebaked, thereafter, a resist pattern mask was formed through exposure and development. By using the mask The TaN film was dry etched with CF_4. Then, a plurality of resistor elements were formed by peeling off the resist.

[0330] A Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the electrodes for the resistors were formed.

[0331] On the plane where the electrodes for the resistor were formed, photosensitive polyimide HD 6000 (product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portion for interlayer connection was formed and the polyimide was hardened at 250° C/1 hour to form the organic insulator.

[0332] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the inductor elements were formed.

[0333] On the plane where the inductor elements were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process of the same the polyimide was hardened at 250° C/1 hour to form the organic insulator.

[0334] A Cr film of 50nm was formed on the back surface of a glass substrate spattering method and further, a Cu film of 500nm was formed thereon, which was used for current feeding use seed film for Cu plating. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10 μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the lower electrode was formed.

[0335] Subsequently, as a barrier film, a Cr film of 50nm is formed with spattering method.

[0336] Then, Ta_2O_5 film having thickness of 500nm was formed on the lower electrode by spattering method. On the Ta_2O_5 film positive type liquid resist OFPR800, 500cp(product of Tokyo Ohka) was coated and after performing drying, exposing and developing process a resist mask for a dielectric layer was formed. Subsequently, dry etch was performed by making use of CF_4 to remove unnecessary portion thereof and further, unnecessary portion of the barrier layer was removed with Cr etching liquid of permanganic acid, then, the resist mask was removed and the dielectric layer was formed.

[0337] Subsequently, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the dielectric layer over the lower electrode was exposed. In this instance, the polyimide layer was opened so that the end portion of the opening was located at the inner side from the end of the lower electrode by 20μm. The polyimide is hardened at 250° C/2 hours under nitrogen atmosphere to form the organic insulator of 10 μm.

[0338] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10 μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with cop-

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per etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the upper electrodes were formed.

[0339] On the plane where the upper electrodes were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portion for interlayer connection was formed and the polyimide was hardened at 250° C/1 hour to form the organic insulator.

[0340] Then, a TaN film of 500nm was formed with spattering method. On the film positive type liquid state resist OFPR 800,100cp was spin-coated and prebaked, thereafter, a resist pattern mask was formed through exposure and development. By using the mask The TaN film was dry etched with CF_4. Then, a plurality of resistor elements were formed by peeling off the resist.

[0341] A Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the electrodes for the resistors were formed.

[0342] On the plane where the electrodes for the resistor were formed, photosensitive polyimide HD 6000 (product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portion for interlayer connection was formed and the polyimide was hardened at 250° C/1 hour to form the organic insulator.

[0343] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series, Cr seed film was removed and the inductor elements, the wirings and the metal terminal portions were formed.

[0344] On the plane where the inductor elements, the wirings and the metal terminal portions were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin-coating and after prebaking with a hot plate, through exposing and developing process the opening portions for forming the solder balls were formed and the polyimide was hardened at 250° C/1 hour to form the organic insulator.

[0345] After applying electroless gold plating on the surface of the metal terminal portion and then coating solder flux on a predetermined portion with a metal mask, the external electrodes were formed by arranging the lead free solder balls having a diameter of 200μm and performing reflow processing.

[0346] Finally, the product was separated by a dicing machine to form the electronic circuit components.

[0347] In the present embodiment, since the capacitor elements, inductor elements and resistor elements are respectively arranged at a plurality of different distances from the surface of the glass substrate, the respective elements can be integrated in further high density, therefore, a further small sized electronic circuit component can be obtained in addition to the advantages obtained in embodiments 9 and 11.

[0348] Further, through the use of the glass used in embodiment 2, the electronic circuit component of course shows a high reliability such as in connection with impact resistance.

[0349] Further, through the use of the photosensitive glass substrate as used in embodiment 10 a low cost electronic circuit component having further high integration degree can be of course obtained.

[0350] Through the use of BCB organic insulator used in embodiment 3 for the organic insulator in the present embodiment, the conductive loss and dielectric loss are reduced, thereby, an electronic circuit component having a small signal transmission loss can be obtained.

[0351] Further, by using the low dielectric loss tangent resin composition as used in embodiment 4 as the insulator layer, the conductive loss and dielectric loss are reduced, thereby, loss of signals transmitting through the electronic circuits can be reduced with the low cost material.

[0352] Further, Fig.20 structure is one embodiment of the present invention, and the arrangement of the respective elements is not limited to that shown.

(Embodiment 14)

[0353] Fig.21 is a cross sectional view of an electronic circuit component representing one embodiment of the present invention. In Fig.21, 1 is a glass substrate (product of Nippon Electric Glass Co., Ltd.,BLC), and the thickness of which is 0.5mm.

[0354] In Fig.21, 2 and 12 are an organic insulator and photosensitive polyimide (product of Hitachi Chemical Co., Ltd., HD-6000) is used therefor.

[0355] Capacitor elements formed inside the organic insulators 2 and 12 are constituted by capacitors 3 and 13 in a three layer structure constituted by lower elec-

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trodes 3a and 13a of Cu, a dielectric bodies 3b and 13b of oxide of Ta and upper electrodes 3c and 13c of Cu and capacitors 3' and 13' in a three layer structure constituted by lower electrode 3'a 13'a of Cu, dielectric bodies 3'b and 13'b of polyimide and upper electrode 3'c and 13'c of Cu. Further, on the upper electrode connecting portions 8 for connecting with upper wirings are provided

[0356] An inductor element 4 and 14 are spiral type inductors and the material thereof is Cu.

[0357] Resistors 5 and 15 are constituted by resistance bodies 5b and 15 and electrodes 5a 15a and 5 c and 15c. The resistance bodies 5b and 15b are a compound of Ta and Ti and the electrodes 5a and 15a and 5c and 15c are composed of Cu.

[0358] In Fig.21, the respective elements formed inside the organic insulators 2 and 12 are electrically connected via conductor portions filled in through holes 20 formed in the glass substrate so as to provide a predetermined functions.

[0359] In the semiconductor connection substrate as shown in Fig.21, an organic insulator 9 having a function of buffering stress is provided. For the organic insulator having the stress buffering function, a liquid polyimide material in which polyimide fine particles are dispersed (product of Hitachi Chemical Co., Ltd., GH-P500) was used.

[0360] In Fig.21, 6 is a metal terminal portion used for connectio n with an external terminal and in the drawing a solder ball 7 is mounted on the metal terminal portion 6.

[0361] The manufacturing method of the electronic circuit component as shown in Fig.21 will be explained.

[0362] A sand blast use film resist (product of Tokyo Ohka, Odale)of 100μm was laminated on the glass substrate having thickness of 0.5mm through exposure and development process and an etching use resist was formed. Subsequently, through holes were formed in the glass substrate with micro sand blasing method. Then, the resist film was peeled off, electrolytic plating use seed films Cr:50nm, Cu:500nm were formed on the surface of the glass substrate and walls of the via holes with spattering method. Thereafter, on the Cu film a plating use film resist (product of Hitachi Chemical Co., Ltd., HN 920) was laminated and a resist mask was formed through exposure and development, then, conductive layers were formed inside the via holes by Cu electrolytic plating. Subsequently, the resist and the electrolytic plating seed film were peeled off.

[0363] A Cr film of 50nm was formed on the main surface of a glass substrate spattering method and further, a Cu film of 500nm was formed thereon, which was used for current feeding use seed film for Cu plating. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10 μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of perma nganic acid series Cr seed film was removed and the lower electrode was formed.

[0364] Subsequently, as a barrier film, a Cr film of 50nm is formed with spattering method.

[0365] Then, Ta_2O_5 film having thickness of 500nm was formed on the lower electrode by spattering method. On the Ta_2O_5 film positive type liquid resist OFPR800, 500cp(product of Tokyo Ohka) was coated and after performing drying, exposing and developing process a resist mask for a dielectric layer was formed. Subsequently, dry etch was performed by making use of CF_4 to remove unnecessary portion thereof and further, unnecessary portion of the barrier layer was removed with Cr etching liquid of permanganic acid, then, the resist mask was removed and the dielectric layer was formed.

[0366] Subsequently, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the dielectric layer over the lower electrode was exposed. In this instance, the polyimide layer was opened so that the end portion of the opening was located at the inner side from the end of the lower electrode by 20μm. The polyimide is hardened at 250° C/2 hours under nitrogen atmosphere to form the organic insulator of 10μm.

[0367] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the upper electrodes were formed.

[0368] On the plane where the upper electrodes were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portion for interlayer connection was formed and the polyimide was hardened at 250° C/1 hour to form the organic insulator.

[0369] Then, a TaN film of 500nm was formed with spattering method. On the film positive type liquid state resist OFPR 800,100cp was spin-coated and prebaked, thereafter, a resist pattern mask was formed through exposure and development. By using the mask The TaN

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film was dry etched with CF_4. Then, a plurality of resistor elements were formed by peeling off the resist.

[0370] A Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the electrodes for the resistors were formed.

[0371] On the plane where the electrodes for the resistor were formed, photosensitive polyimide HD 6000 (product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portion for interlayer connection was formed and the polyimide was hardened at 250° C/1 hour to form the organic insulator.

[0372] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the inductor elements were formed.

[0373] On the plane where the inductor elements were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot.plate, through exposing and developing process the same, the polyimide was hardened at 250° C/1 hour to form the organic insulator.

[0374] A Cr film of 50nm was formed on the back surface of a glass substrate spattering method and further, a Cu film of 500nm was formed thereon, which was used for current feeding use seed film for Cu plating. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10 μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the lower electrode was formed.

[0375] Subsequently, as a barrier film, a Cr film of 50nm is formed with spattering method.

[0376] Then, Ta_2O_5 film having thickness of 500nm was formed on the lower electrode by spattering method. On the Ta_2O_5 film positive type liquid resist OFPR800, 500cp(product of Tokyo Ohka) was coated and after performing drying, exposing and developing process a resist mask for a dielectric layer was formed. Subsequently, dry etch was performed by making use of CF_4 to remove unnecessary portion thereof and further, unnecessary portion of the barrier layer was removed with Cr etching liquid of permanganic acid, then, the resist mask was removed and the dielectric layer was formed.

[0377] Subsequently, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the dielectric layer over the lower electrode was exposed. In this instance, the polyimide layer was opened so that the end portion of the opening was located at the inner side from the end of the lower electrode by 20μm. The polyimide is hardened at 250 ° C/2 hours under nitrogen atmosphere to form the organic insulator of 10μm.

[0378] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the upper electrodes were formed.

[0379] On the plane where the upper electrodes were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portion for interlayer connection was formed and the polyimide was hardened at 250° C/1 hour to form the organic insulator.

[0380] Then, a TaN film of 500nm was formed with spattering method. On the film positive type liquid state resist OFPR 800,100cp was spin-coated and prebaked, thereafter, a resist pattern mask was formed through exposure and development. By using the mask The TaN film was dry etched with CF_4. Then, a plurality of resistor elements were formed by peeling off the resist.

[0381] A Cr film of 50nm was formed with spattering

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method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the electrodes for the resistors were formed.

[0382] On the plane where the electrodes for the resistor were formed, photosensitive polyimide HD 6000 (product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portion for interlayer connection was formed and the polyimide was hardened at 250° C/1 hour to form the organic insulator.

[0383] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, which was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the inductor elements and the wirings were formed.

[0384] Thereafter, the liquid polyimide material GH-P 500 in which polyimide fine particles are dispersed (product of Hitachi Chemical Co., Ltd.) was print coated by using a mask, heated on a hot plate at 200°C/25min and hardened in a constant temperature bath at 250°C/60min to form the organic insulator having stress buffering function.

[0385] Subsequently, a Cr film of 50nm was formed with spattering method and further, a Cu film of 500nm was formed thereon, wh ich was used as a seed film. On the Cu film negative type liquid state resist PMER-N-CA1000 (product of Tokyo Ohka) was spin-coated, after prebaking the same with a hot plate, a resist mask was formed through exposure and development steps. At the resist opening portions electrolytic copper plating of 10μm was performed with current density of 1A/dm. Subsequently, the resist mask was removed and the copper seed film was removed with copper etching liquid Cobra etch (product of Ebara Densan). Further, by making use of Cr etching liquid of permanganic acid series Cr seed film was removed and the wirings and the metal terminal portions were formed.

[0386] On the plane where the wirings and the metal terminal portions were formed, photosensitive polyimide HD 6000(product of Hitachi Chemical Co., Ltd.) was coated by spin coating and after prebaking with a hot plate, through exposing and developing process the opening portions for forming the solder balls were formed and the polyimide was hardened at 250° C/1 hour to form the organic insulator.

[0387] After applying electroless gold plating on the surface of the metal terminal portion and then coating solder flux on a predetermined portion with a metal mask, the external electrodes were formed by arranging the lead free solder balls having a diameter of 200μm and performing reflow processing.

[0388] Finally, the product was separated by a dicing machine to form the electronic circuit components.

[0389] In the present embodiment, since the organic insulator having stress buffering function is formed immediately below the metal terminal portion 6, when being connected to a mounting substrate such as a print substrate, a thermal stress applied to the metal terminal portion 6 and the solder ball 7 due to difference of thermal expansion coefficients between the semiconductor connection substrate and the mounting substrate can be relaxed. Thereby, a semiconductor connection substrate having excellent heart resistance cycle can be obtained in addition to the advantages obtained in embodiment 13.

[0390] Further, through the use of the glass used in embodiment 2, the electronic circuit component of course shows a high reliability such as in connection with impact resistance.

[0391] Further, through the use of the photosensitive glass substrate as used in embodiment 10 a low cost electronic circuit component having further high integration degree can be of course obtained.

[0392] Through the use of BCB organic insulator used in embodiment 3 for the organic insulator in the present embodiment, the conductive loss and dielectric loss are reduced, thereby, an electronic circuit component having a small signal transmission loss can be obtained.

[0393] Further, by using the low dielectric loss tangent resin composition as used in embodiment 4 as the insulator layer, the conductive loss and dielectric loss are reduced, thereby, loss of signals transmitting through the electronic circuits can be reduced with the low cost material.

[0394] Further, Fig.21 structure is one embodiment of the present invention, and the arrangement of the respective elements is not limited to that shown.

[0395] In the followings, other embodiments of the present invention will be explained.

[0396] Through provision of (1) a glass substrate, (2) one or a plurality of elements selected from a capacitor element, an inductor element and resistor element each provided on the glass substrate,(3) a metal wiring provided on the glass substrate for connecting the elements, (4) a metal terminal portion which is a part of the

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metal wiring provided on the glass substrate and (5) an organic insulator which covers the elements and the circumference of the metal wiring portion except for the metal terminal portion, an electronic circuit component which permits to integrate a variety of electronic parts such as a capacitor, inductor and resistor in a high performance and in a high density can be obtained.

[0397] Through provision of (1) a glass substrate at predetermined positions of which through holes are provided, (2) one or a plurality of elements selected from a capacitor element, inductor element and resistor element each provided on one or both sides of the glass substrate, (3) a metal wiring provided on both sides of the glass substrate for connecting the elements, (4) conductive portions formed inside the through holes for electrically connecting the metal wiring, (5) a metal terminal portion which is a part of the metal wiring provided on one or both of the glass substrate and (6) an organic insulator which covers the elements and the circumference of the metal wiring portion except for the metal terminal portion, a n electronic circuit component which permits to integrate a variety of electronic parts such as a capacitor, inductor and resistor in a high performance and in a high density can be obtained.

[0398] By forming one or the plurality of elements selected from the capacitor elements, inductor elements and resistor elements, the metal wiring, the metal terminal portion and the organic insul ator at the inside from the end portion of the glass substrate, the structural portions where stresses concentratedly applied at the time of cutting out the electronic circuit component and at the time of mounting the same are designed to withstand the stresses and a possible damage on the electronic circuit component due to the applied stresses can be greatly reduced, thereby, a highly reliable electronic circuit component of a desirable manufacturing yield which permits to integrate a variety of electronic parts such as a capacitor, inductor and resistor in a high performance and in a high density can be obtained.

[0399] Since the capacitor elements are constituted by one or more of capacitor elements having a structure in which an inorganic dielectric material is sandwiched by two metal electrodes and one or more capacitor elements having a structure in which an organic dielectric material is sandwiched by two electrodes , through a proper use of dielectric materials of organic or inorganic or both, a small sized electronic circuit component of a high performance and a high integration degree can be obtained.

[0400] Since the inorganic dielectric material is an oxide of any of Ta, Mg and Sr and the organic dielectric material is polyimide, a highly reliable and high performance electronic circuit component of low cost can be obtained because of low cost and high stability property of Ta, Mg and Sr and of high thermal stability of polyimide.

[0401] Since the inorganic dielectric material is an oxide of any of Ta, Mg and Sr and the organic dielectric material is BCB (Benzo Cyclo Butene), a highly reliable and high performance electronic circuit component of low cost can be obtained because of low cost and high stability property of Ta, Mg and Sr and of low dielectric constant and dielectric loss tangent of BCB.

[0402] Since the inorganic dielectric material is an oxide of any of Ta, Mg and Sr and the organic dielectric material is a low dielectric loss tangent resin composition which includes a bridging component having a plurality of sty rene groups as expressed by the above referred to general chemical formula and contains polymers having average molecular weight of more than 5000, a highly reliable and high performance electronic circuit component of low cost can be obtained because of low cost and high stability property of Ta, Mg and Sr and of low dielectric constant and dielectric loss tangent of the low dielectric loss tangent resin composition of low cost.

[0403] Since the end portion of the metal electrode of the capacitor element at the side of the glass substrate is covered by an insulator other than the dielectric insulator, a short circuiting between the electrodes and reduction of dielectric strength are prevented and a highly reliable capacitor element with a low defective rate can be provided without reducing design freedom, thus, a low defective rate and highly reliable electronic circuit component having a plurality of built-in capacitor elements can be obtained.

[0404] Through the use of the electronic circuit component a high performance, highly reliable and small sized wireless terminal device of low cost can be obtained.

[0405] Through the use of the electronic circuit component a high performance, highly reliable and small sized wireless base station device of low cost can be obtained.

[0406] Through the use of the electronic circuit component a high performance, highly reliable and small sized wireless measurement device of low cost can be obtained.

[0407] Since the following relationship between the two opening diameters R1 and R2 (R1 ≧ R2)of the through holes and the thickness t of the glass substrate is satisfied;

$$70 \leqq \tan^{-1}(t/(R1-R2)) \leqq 80$$

a further small size electronic circuit component can be obtained, because the circuits are integrated in a further high density.

[0408] Since any of the capacitor elements, inductor elements and resistor elements are arranged on one face of the glass substrate and the remaining elements are arranged on the other face of the substrate, a possible influence between the respective elements can be reduced and the self oscillation frequencies of the elements can be increased because of reduced parasitic capacitance.

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[0409] With the above embodiments, the structural portions where stresses concentratedly applied at the time of cutting out the electronic circuit component and at the time of mounting the same are designed to withstand the stresses and a possible damage on the electronic circuit component due to the applied stresses can be greatly reduced, and thereby, a highly reliable electronic circuit component of a desirable manufacturing yield which permits to integrate a variety of electronic parts such as a capacitor, inductor and resistor in a high performance and in a high density can be obtained.

Claims

1. An electronic circuit component comprising an insulator substrate, a plurality of electrodes having different areas provided on the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a metal wiring connecting the elements, a metal terminal part of a part of the metal wiring and an organic insulator material covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion.

2. An electronic circuit component comprising an insulator substrate, a plurality of electrodes provided on the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a connecting portion provide at portions other than end portions of the electrodes, a metal wiring connecting the elements and the connecting portion, a metal terminal part of a part of the metal wiring and an organic insulator material covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion.

3. An electronic circuit component comprising an insulator substrate, a plurality of electrodes provided on the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a metal wiring connecting the elements, a metal terminal part of a part of the metal wiring and being arranged in a grid shape and an organic insulator material covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion.

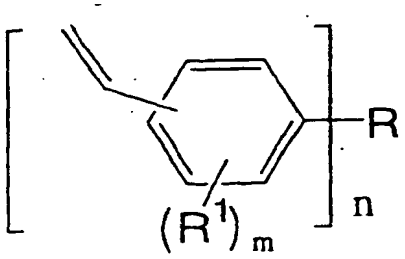
4. An electronic circuit component comprising an insulator substrate, a plurality of electrodes provided on the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a metal wiring connecting the elements, a metal terminal part of a part of the metal wiring and a plurality of organic insulator material s covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion.

5. An electronic circuit component according to any one of claims 1 through 4, wherein the distances between the capacitance element constituted by the plurality of the electrodes and the dielectric material sandwiched therebetween, the inductor element and the resistor element and the insulator substrate are differentiated.

6. An electronic circuit component according to any one of claims 1 through 5, wherein the insulator substrate is a glass substrate.

7. An electronic circuit component according to any one of claims 1 through 6, wherein the organic insulator material is a photosensitive organic insulator material.

8. An electronic circuit component according to any one of claims 1 through 6, wherein the organic insulator material is a low dielectric loss tangent resin composition which includes a bridging component having a plurality of styrene groups as expressed by the following general chemical formula and contains polymers having average molecular weight of more than 5000,



(Wherein, R represents a hydrocarbon skeleton, which may include a substituent, R^1 represents one of hydrogen, methyl and ethyl, m represents 1 from 4 and n represents an integer more than 1).

9. An electronic circuit component according to any one of claims 1 through 6, wherein the organic insulator material is polyimide.

10. An electronic circuit component according to any one of claims 1 through 6, wherein the organic insulator material is BCB (Benzo Cyclo Butene).

11. An electronic circuit component according to any

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one of claims 1 through 10, wherein the dielectric material is an organic insulator material or an oxide of any one of Ta, Mg and Sr.

12. An electronic circuit component comprising an insulator substrate at predetermined position of which through holes are provided, a plurality of electrodes having different areas provided on both faces of the main face and the sub-main face or one of the faces of the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a metal wiring connecting the elements, a conductor portions formed inside the through holes for electrically connecting the metal wiring, a metal terminal part of a part of the metal wiring and an organic insulator material covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion.

13. An electronic circuit component comprising an insulator substrate at predetermined position of which through holes are provided, a plurality of electrodes having different areas provided on both faces of the main face and the sub-main face or one of the faces of the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, connecting portions provided at portions other than end portions of the electrodes, a metal wiring connecting the elements and the connecting portions, a conductor portions formed inside the through holes for electrically connecting the metal wiring, a metal terminal part of a part of the metal wiring and an organic insulator material covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion.

14. An electronic circuit component comprising an insulator substrate at predetermined position of which through holes are provided, a plurality of electrodes having different areas provided on both faces of the main face and the sub-main face or one of the faces of the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a metal wiring connecting the elements, a conductor portions formed inside the through holes for electrically connecting the metal wiring, a metal terminal part of a part of the metal wiring and being arranged in a grid shape and an organic insulator material covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion.

15. An electronic circuit component comprising an insulator substrate at predetermined position of which through holes are provided, a plurality of electrodes provided on both faces of the main face and the sub-main face or one of the faces of the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a metal wiring connecting the elements, a conductor portions formed inside the through holes for electrically connecting the metal wiring, a metal terminal part of a part of the metal wiring and a plurality of organic insulator materials covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion.

16. An electronic circuit component comprising an insulator substrate at predetermined position of which through holes are provided, a plurality of electrodes provided on both faces of the main face and the sub-main face or one of the faces of the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a metal wiring connecting the elements, a conductor portions formed inside the through holes for electrically connecting the metal wiring, a metal terminal part of a part of the metal wiring, a first organic insulator material covering the elements provided on the main face of the insulator substrate and the circumference of the metal wiring portion excluding the metal terminal portion and a second organic insulator material covering the elements provided on the sub-main of the insulator substrate and the circumference of the metal wiring portion excluding the metal terminal portion.

17. An electronic circuit component comprising an insulator substrate at predetermined position of which through holes are provided, a plurality of electrodes provided on both faces of the main face and the sub-main face or one of the faces of the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a metal wiring connecting the elements, a conductor portions formed inside the through holes for electrically connecting the metal wiring, a metal terminal part of a part of the metal wiring and being provided on the other face where the inductor element is provided and an organic insulator material covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion.

18. An electronic circuit component comprising an insulator substrate at predetermined position of which through holes are provided, a plurality of electrodes

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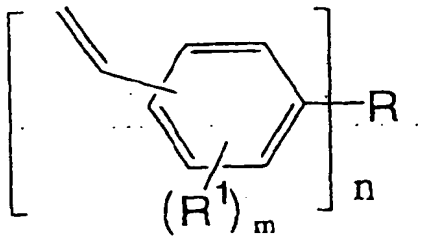
provided on both faces of the main face and the sub-main face or one of the faces of the insulator substrate, one or more elements selected from a capacitor element of dielectric material sandwiched between the electrodes, an inductor element and resistor element, a metal wiring connecting the elements, a conductor portions constituted of a conductive material, core forming material and glass and formed inside the through holes for electrically connecting the metal wiring, a metal terminal part of a part of the metal wiring and an organic insulator material covering the elements and the circumference of the metal wiring portion excluding the metal terminal portion.

19. An electronic circuit component according to any one of claims 12 through 18, wherein the distances between the capacitance element constituted by the plurality of the electrodes and the dielectric material sandwiched therebetween, the inductor element and the resistor element and the insulator substrate are differentiated.

20. An electronic circuit component according to any one of claims 12 through 19, wherein the insulator substrate is a glass substrate.

21. An electronic circuit component according to any one of claims 12 through 20, wherein the organic insulator material is a photosensitive organic insulator material.

22. An electronic circuit component according to any one of claims 12 through 20, wherein the organic insulator material is a low dielectric loss tangent resin composition which includes a bridging component having a plurality of styrene groups as expressed by the following general chemical formula and contains polymers having average molecular weight of more than 5000,



(Wherein, R represents a hydrocarbon skeleton, which may include a substituent, R^1 represents one of hydrogen, methyl and ethyl, m represents 1 from 4 and n represents an integer more than 1).

23. An electronic circuit component according to any one of claims 12 through 20, wherein the organic insulator material is polyimide.

24. An electronic circuit component according to any one of claims 12 through 20, wherein the organic insulator material is BCB (Benzo Cyclo Butene).

25. An electronic circuit component according to any one of claims 12 through 20, wherein the dielectric material is an organic insulator material or an oxide of any one of Ta, Mg and Sr.

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FIG. 1

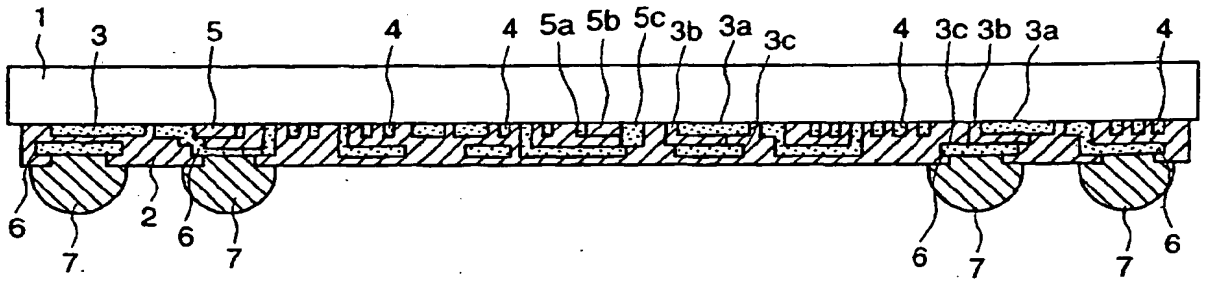


FIG. 2

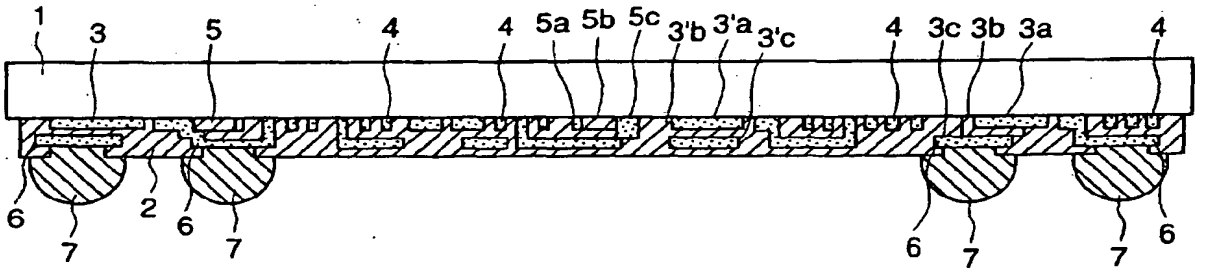
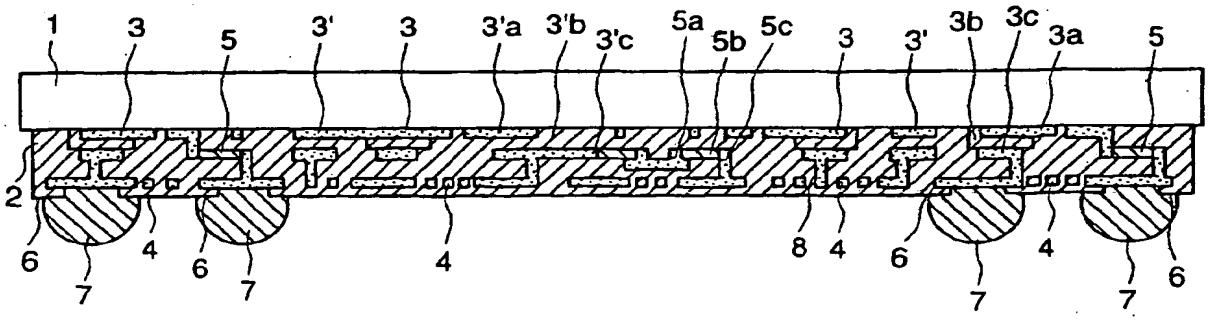


FIG. 3



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FIG. 4

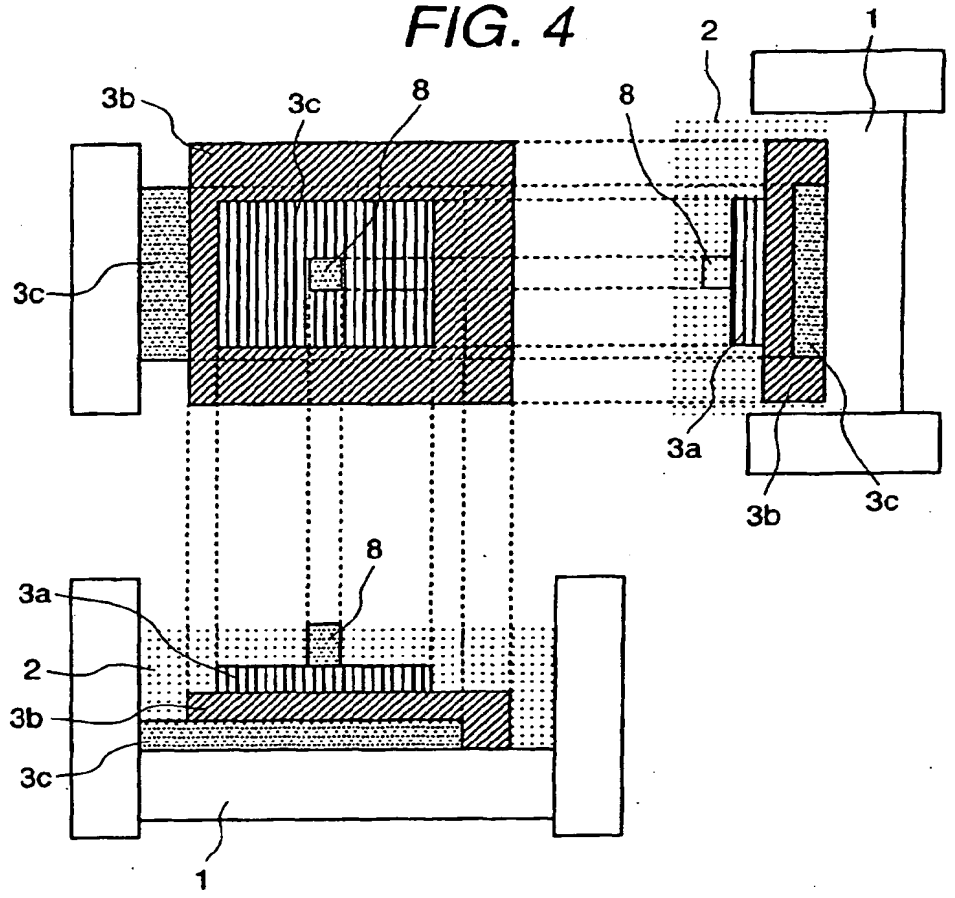
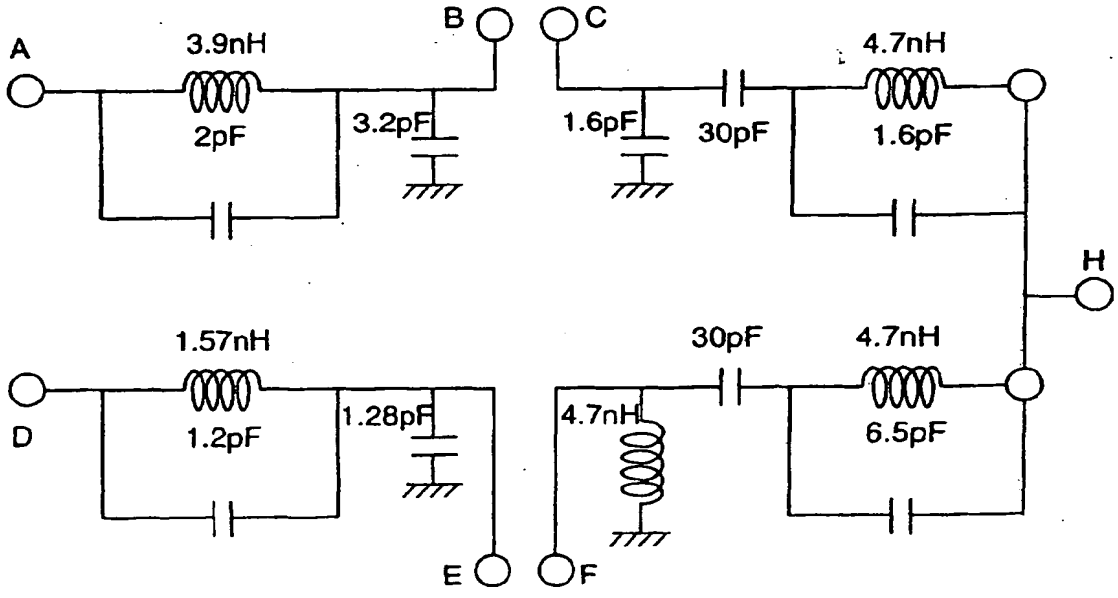
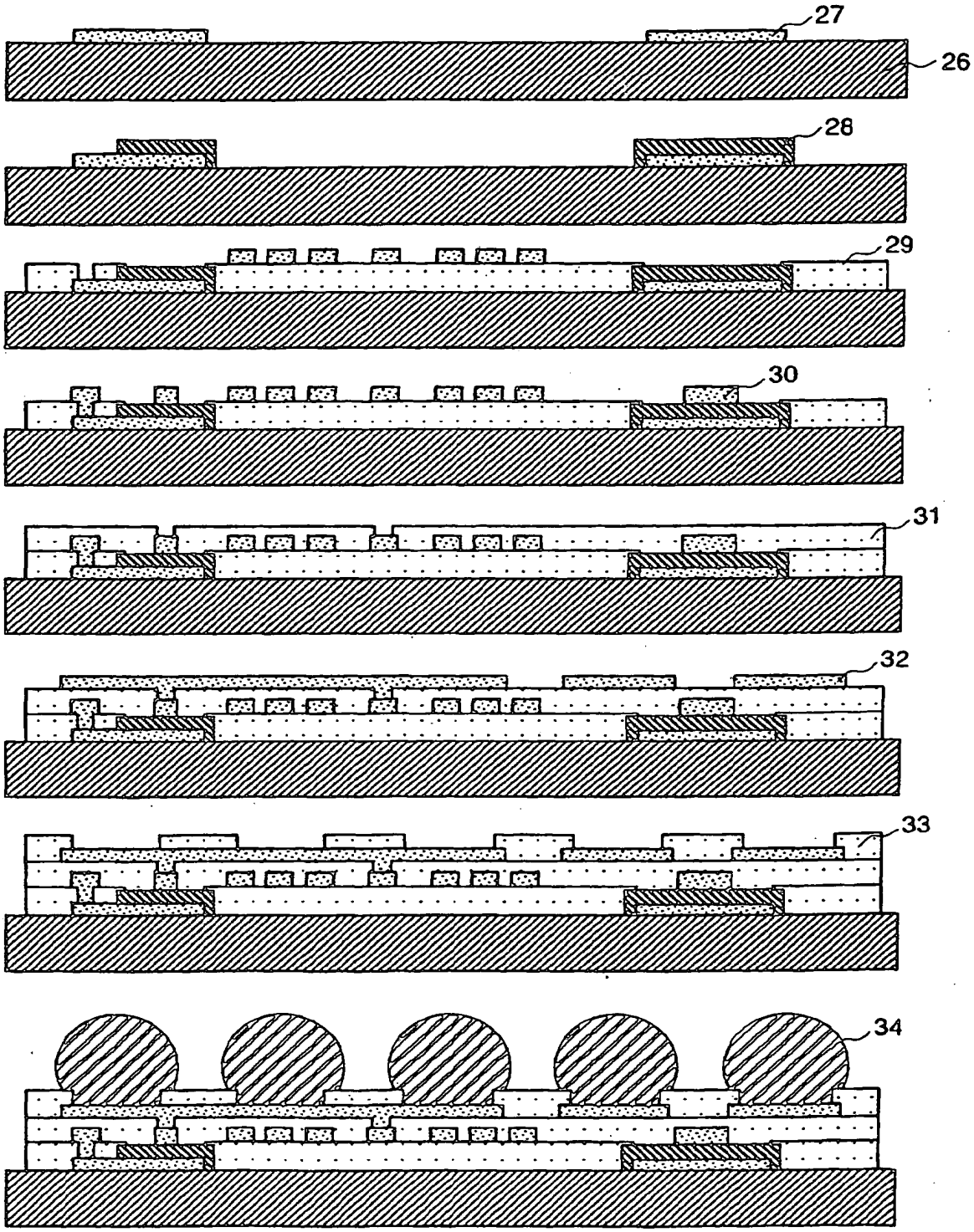


FIG. 5



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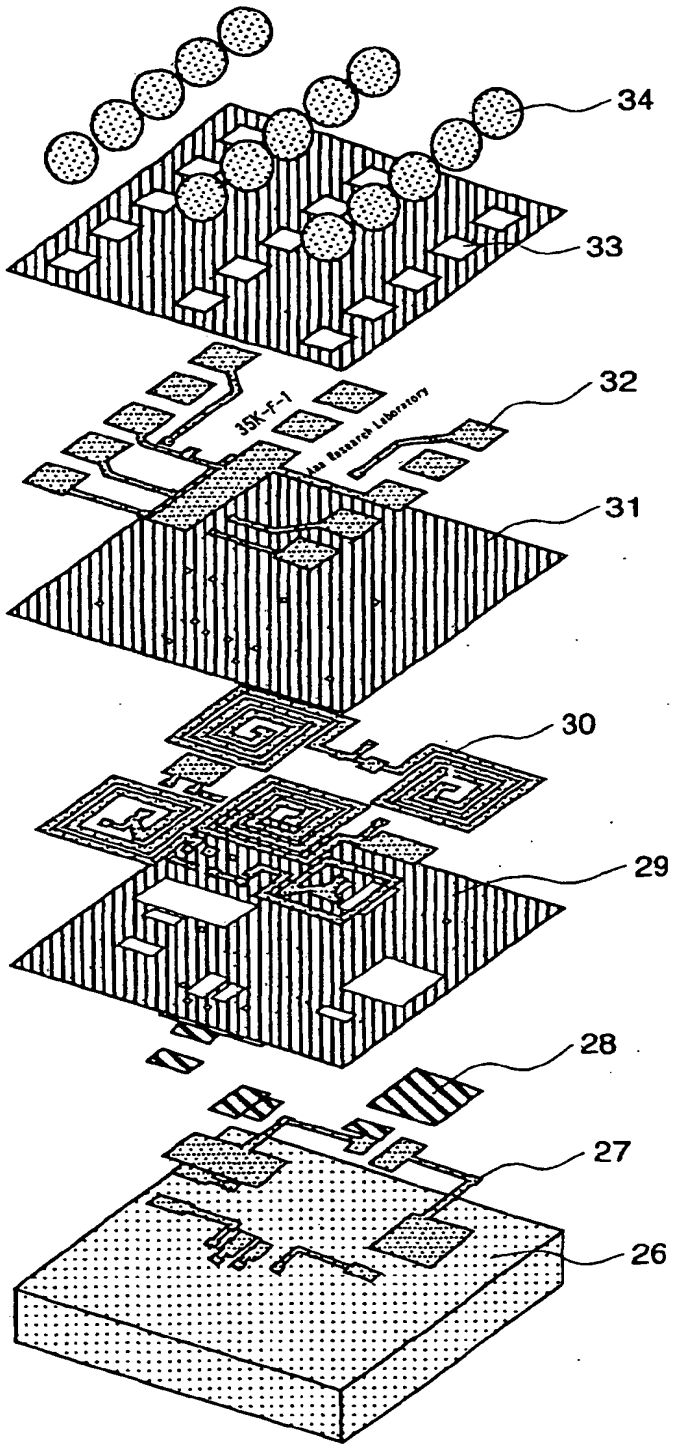
FIG. 6



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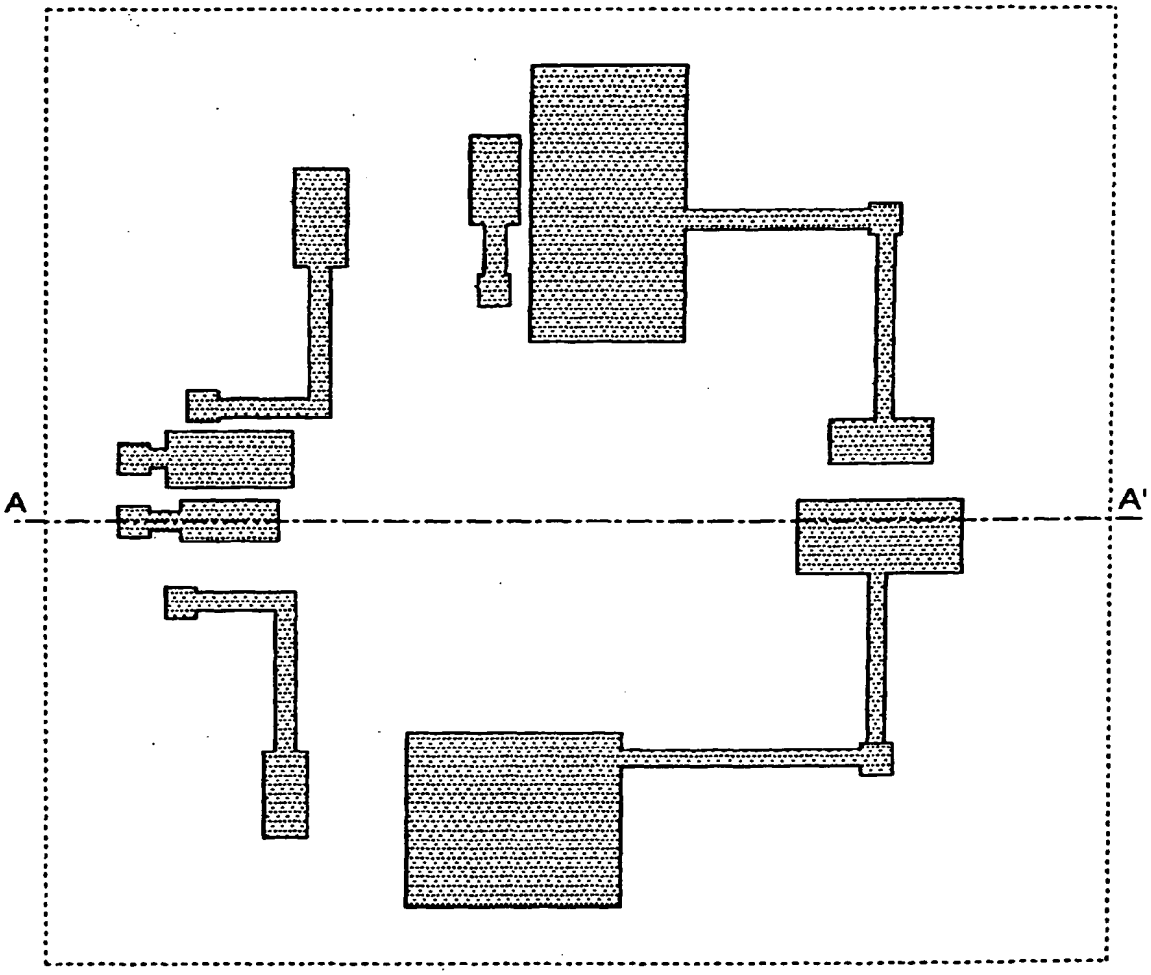
FIG. 7



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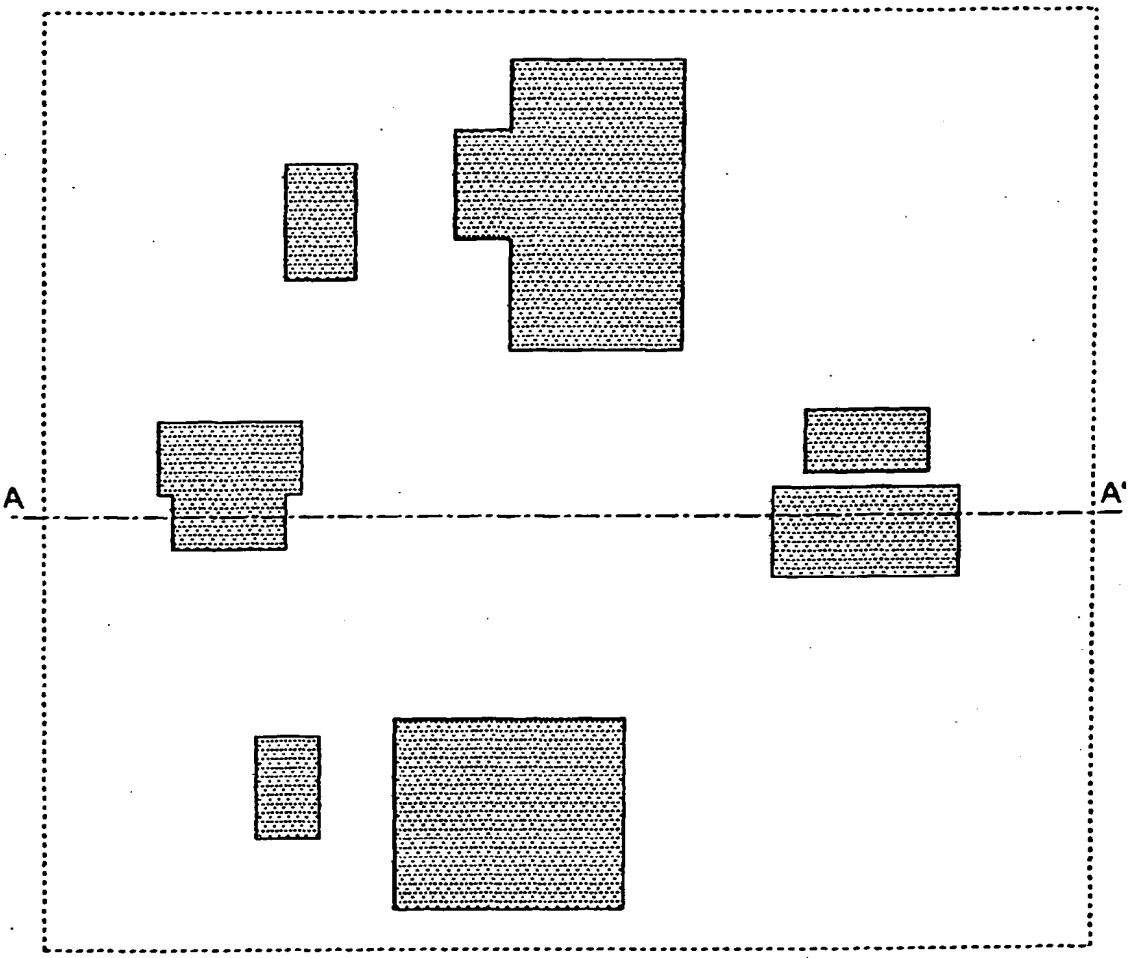
FIG. 8



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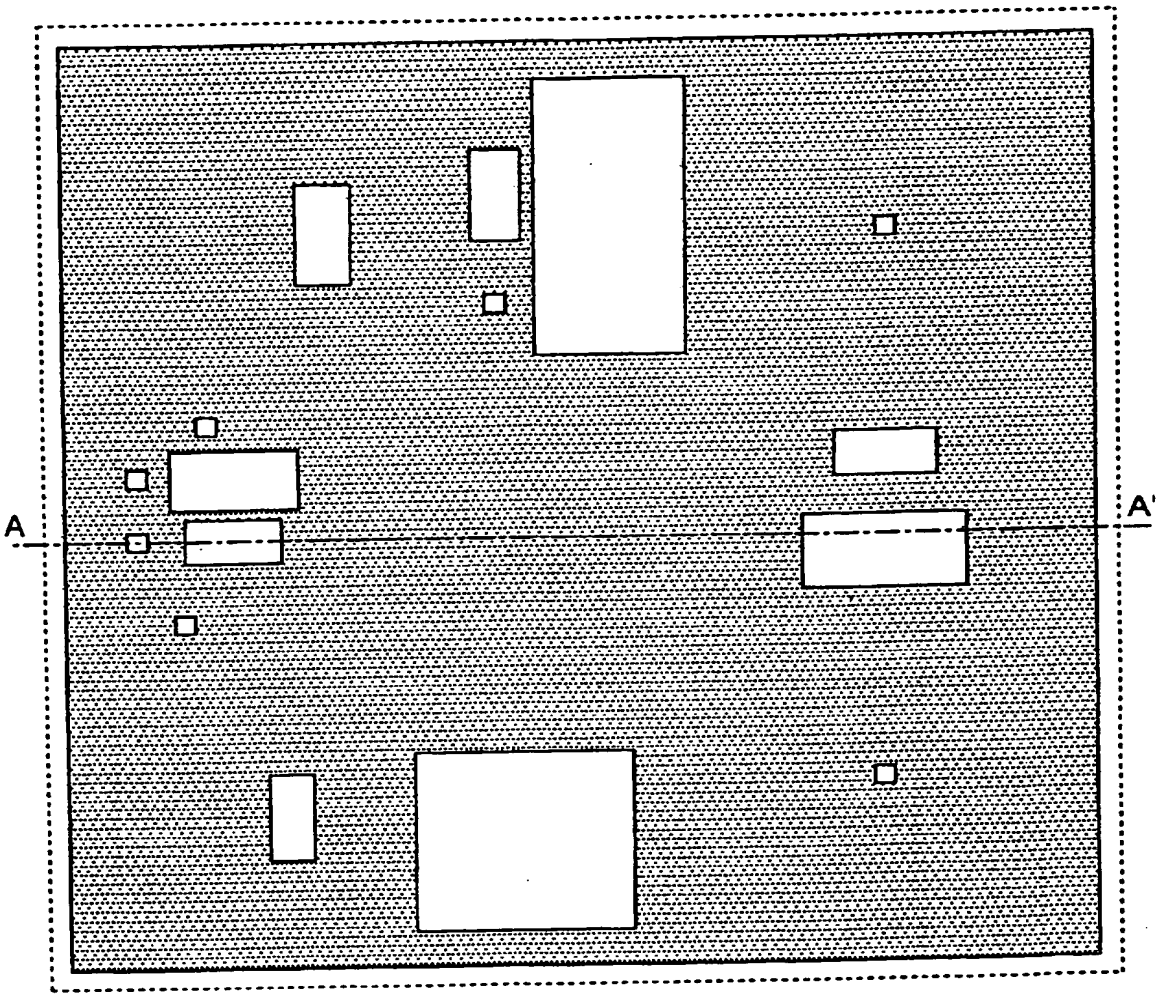
FIG. 9



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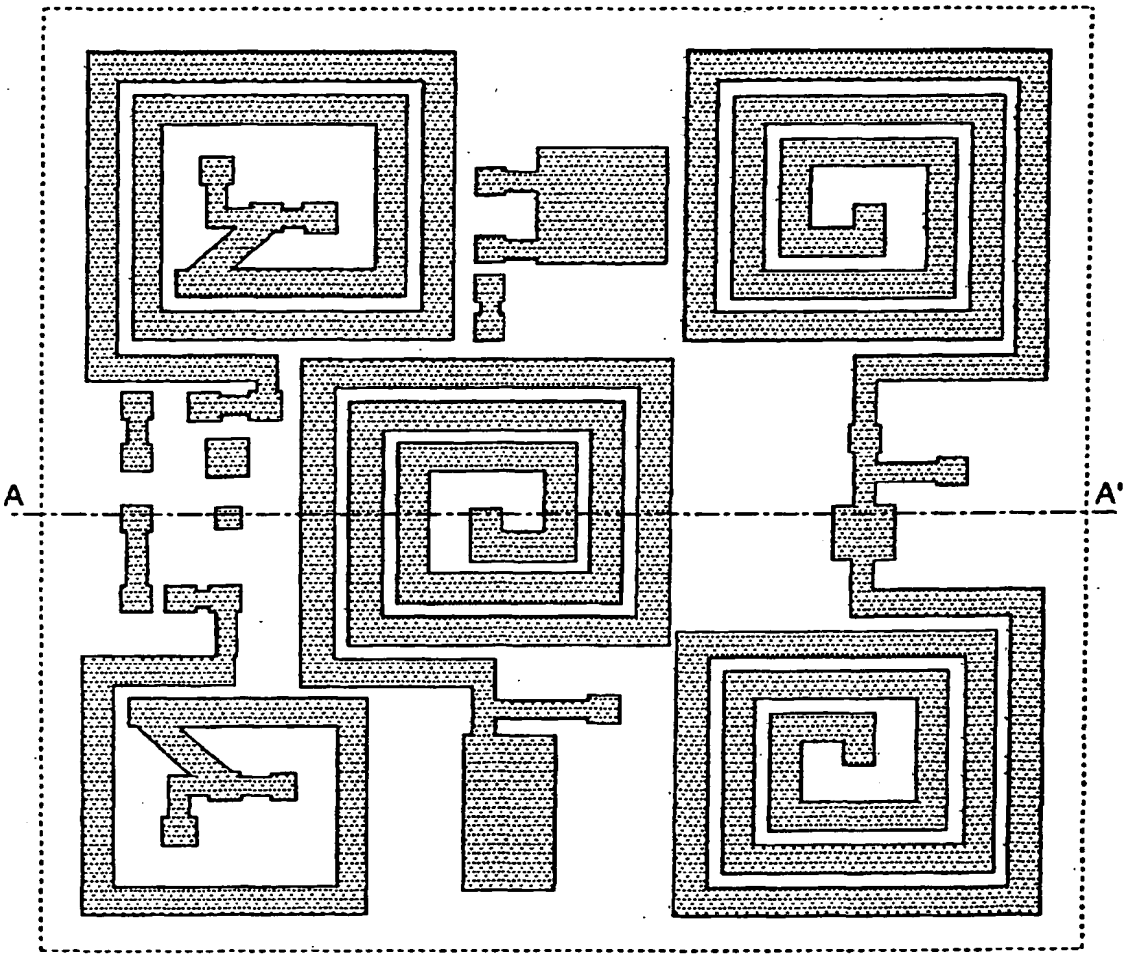
FIG. 10



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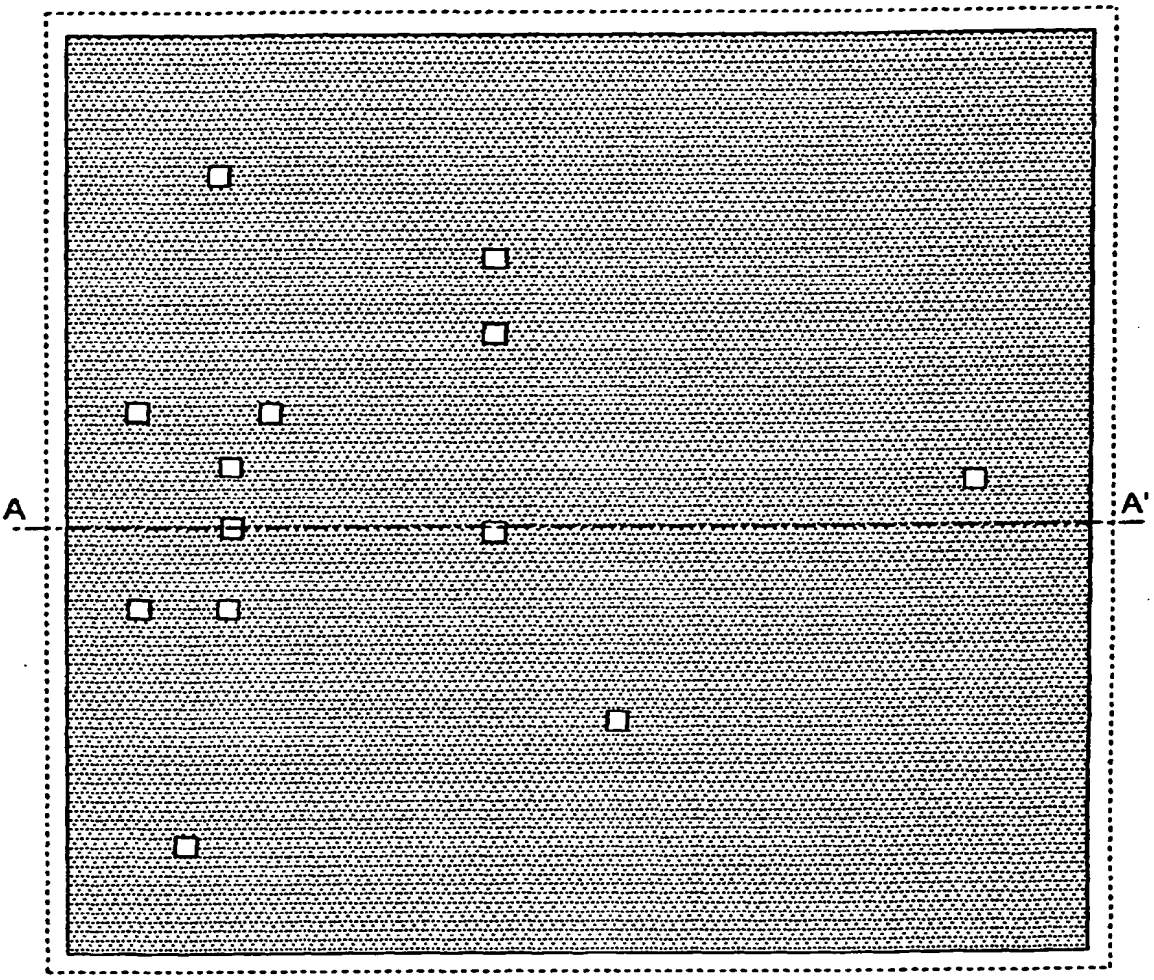
FIG. 11



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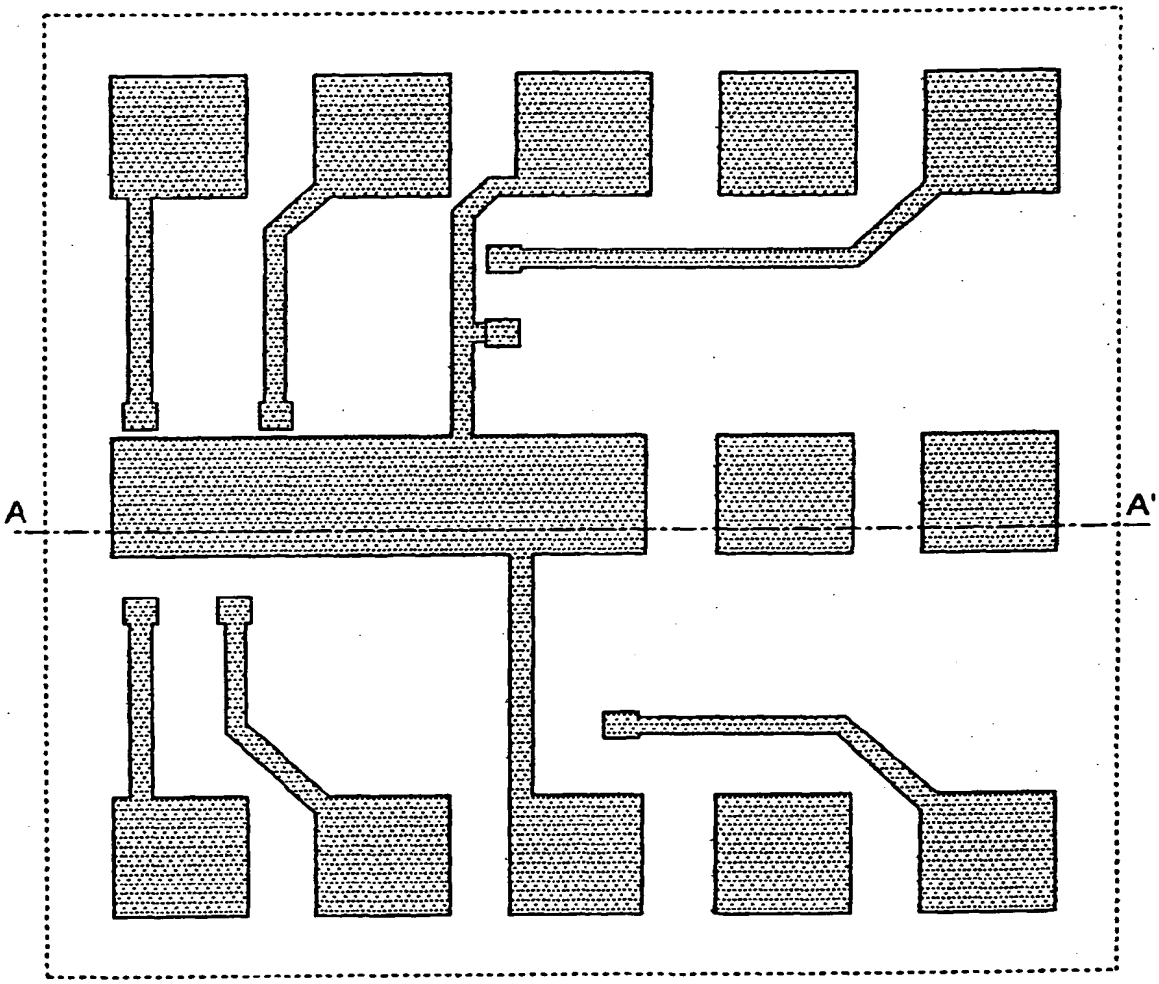
FIG. 12



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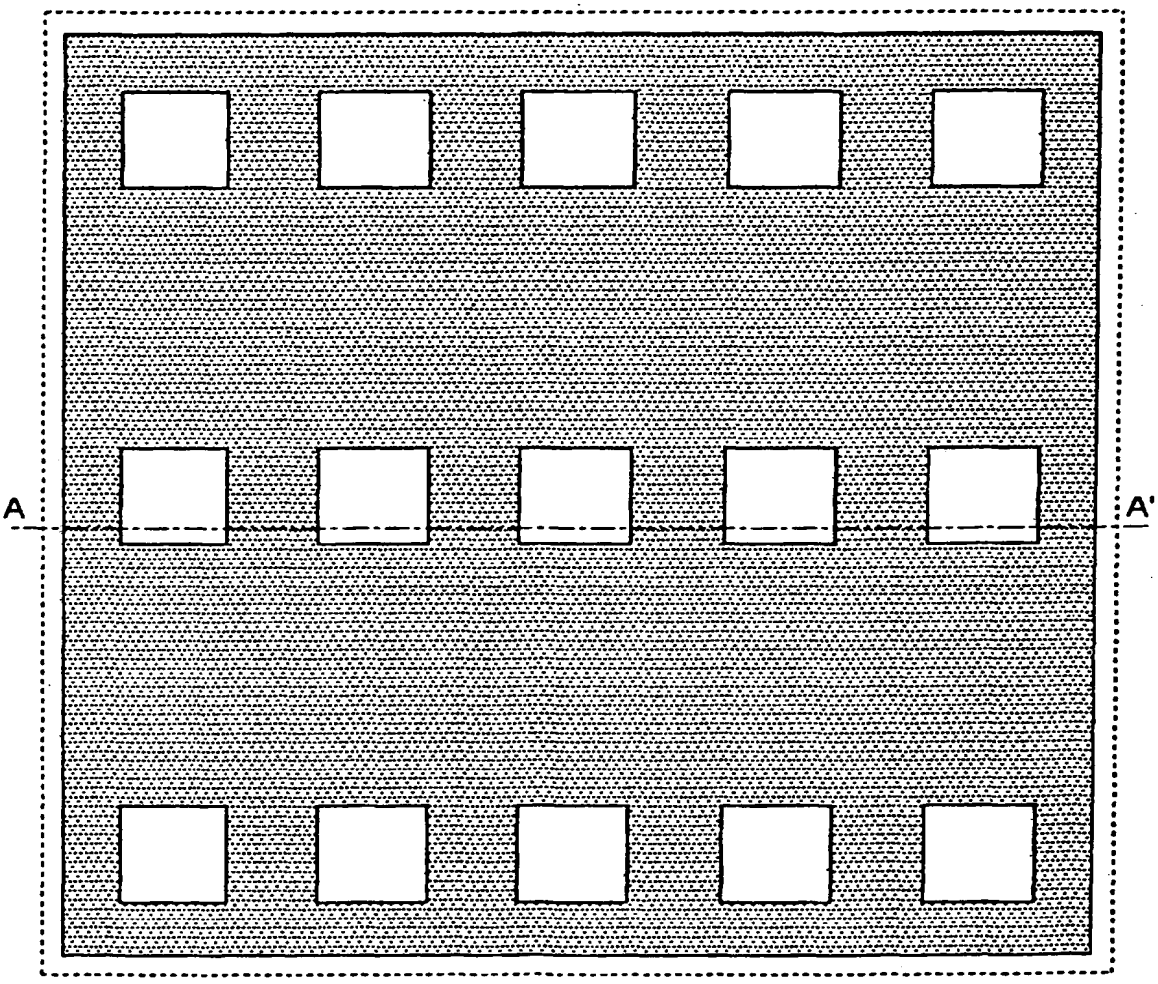
FIG. 13



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FIG. 14



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FIG. 15

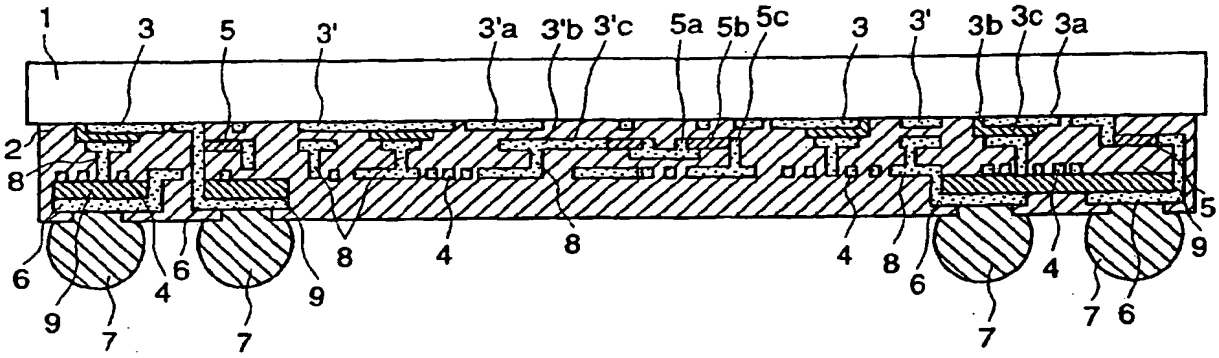
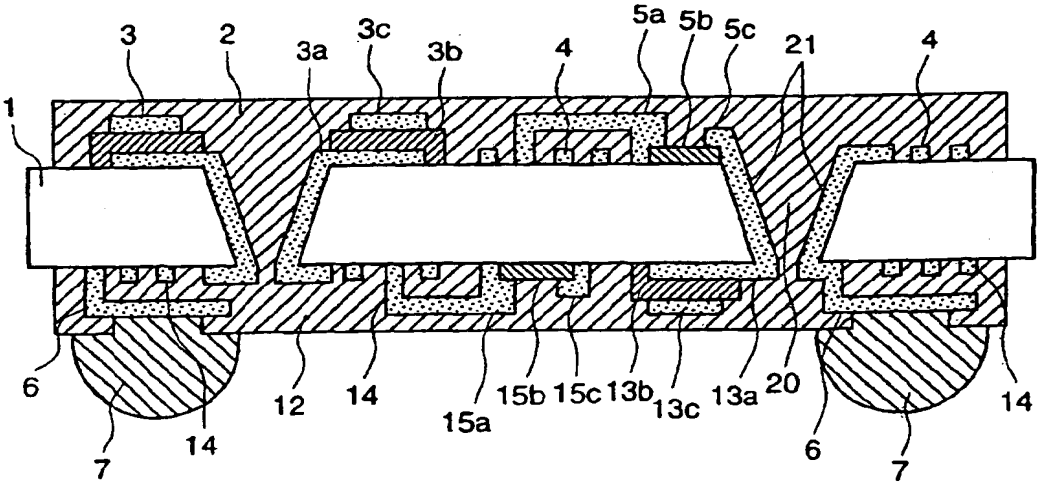


FIG. 16



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FIG. 17

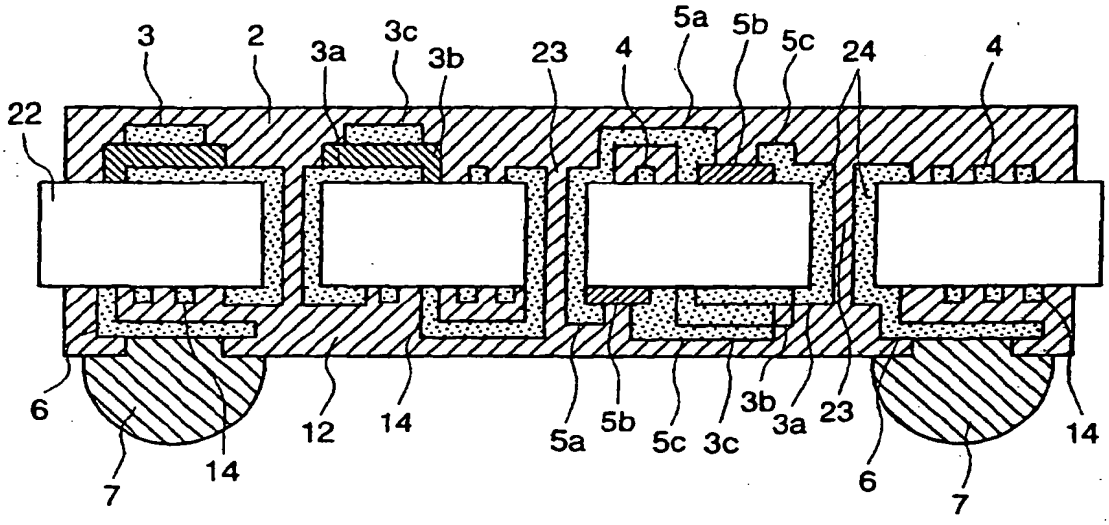
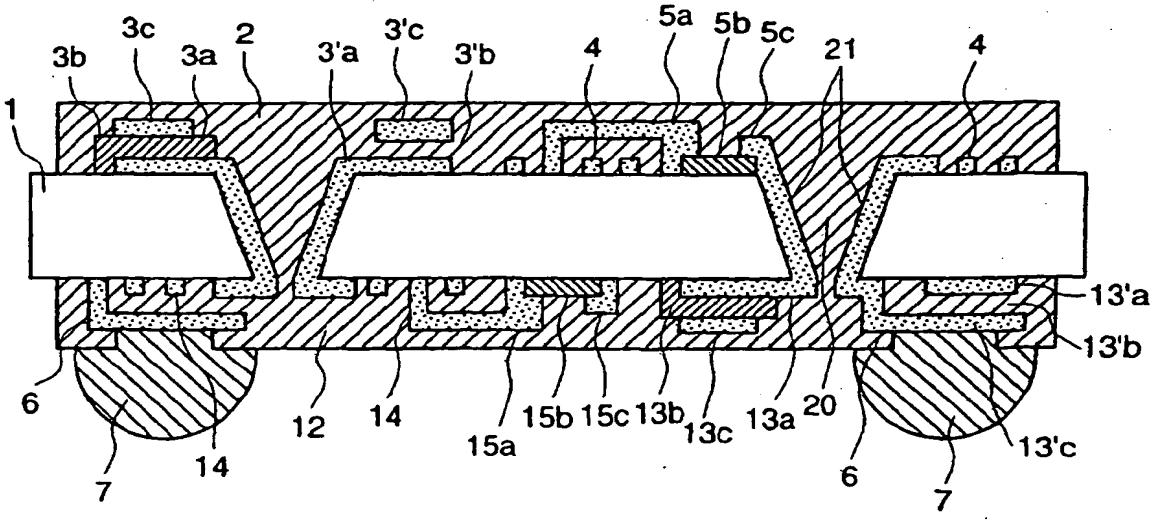


FIG. 18



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FIG. 19

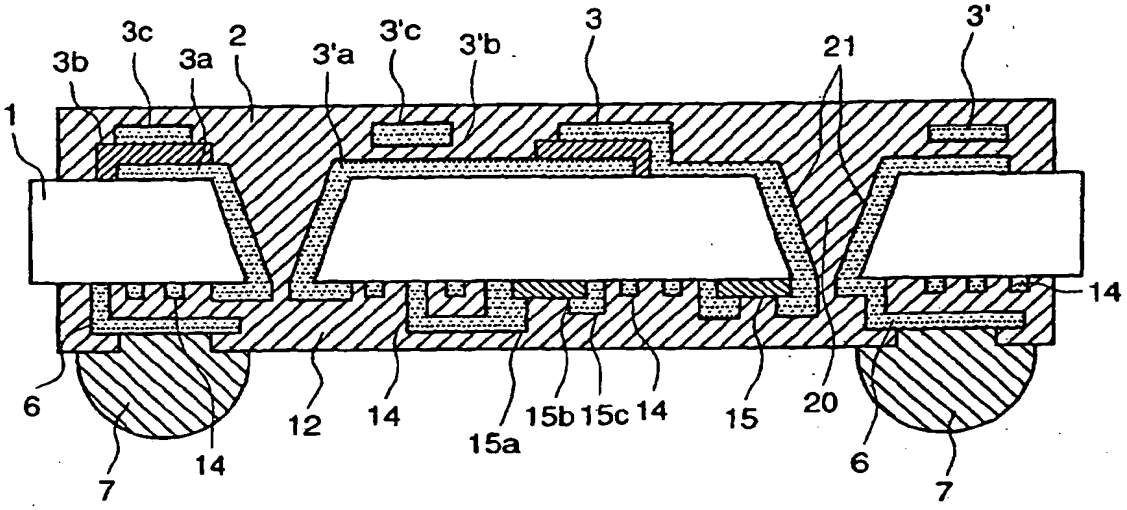
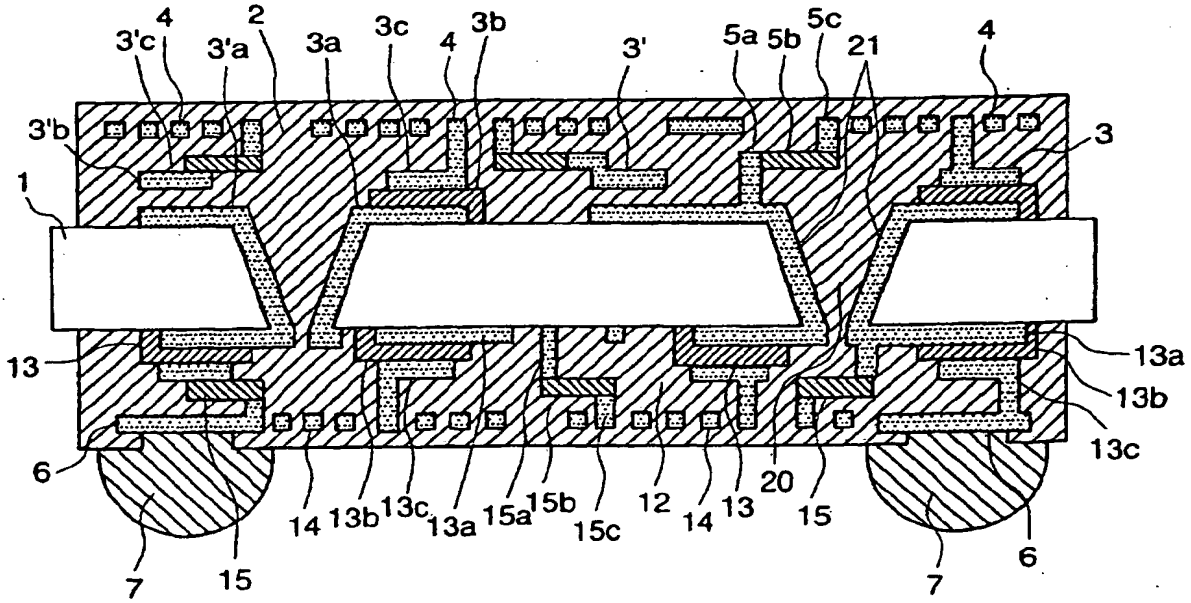


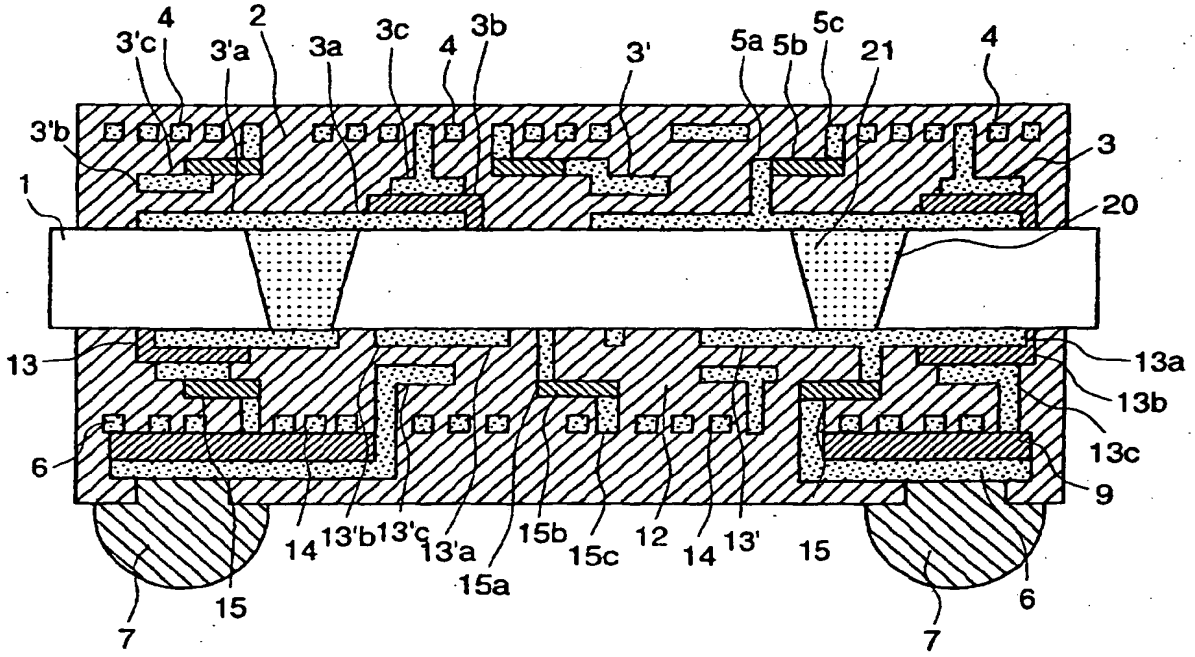
FIG. 20



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FIG. 21



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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP02/07092

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H01L27/01, H01G4/40, H01F17/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H01L27/01, H01L23/12, H01G4/40, H01F17/00, H05K1/16

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1922-1996	Toroku Jitsuyo Shinan Koho	1994-2002
Kokai Jitsuyo Shinan Koho	1971-2002	Jitsuyo Shinan Toroku Koho	1996-2002

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2000-286111 A (Kyocera Corp.), 13 October, 2000 (13.10.00), Full text; Figs. 1 to 4 (Family: none)	1-25
Y	JP 2000-124358 A (Matsushita Electric Industrial Co., Ltd.), 28 April, 2000 (28.04.00), Full text; Figs. 1 to 7 (Family: none)	1-25
Y	JP 4-26184 A (NEC Corp.), 29 January, 1992 (29.01.92), Full text; Figs. 1 to 3 (Family: none)	12-25

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Date of the actual completion of the international search	Date of mailing of the international search report
11 October, 2002 (11.10.02)	29 October, 2002 (29.10.02)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

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INTERNATIONAL SEARCH REPORT

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Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2001-44075 A (Sharp Corp.), 16 February, 2001 (16.02.01), Full text; Figs. 1 to 8 (Family: none)	12-25
Y A	JP 7-106133 A (Kyocera Corp.), 21 April, 1995 (21.04.95), Full text; Figs. 1 to 19 (Family: none)	11,25 1-10,12-24
Y A	JP 7-106134 A (Kyocera Corp.), 21 April, 1995 (21.04.95), Full text; Figs. 1 to 27 (Family: none)	11,25 1-10,12-24
A	JP 10-41632 A (Kyocera Corp.), 13 February, 1998 (13.02.98), Full text; Figs. 1 to 19 (Family: none)	1-25
A	JP 6-125180 A (NGK Spark Plug Co., Ltd.), 06 May, 1994 (06.05.94), Full text; Figs. 1 to 3 (Family: none)	1-25
A	JP 6-181119 A (Takashi IKEDA), 28 June, 1994 (28.06.94), Full text; Figs. 1 to 6 (Family: none)	1-25

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PUBLICATION NUMBER : 07161583
PUBLICATION DATE : 23-06-95

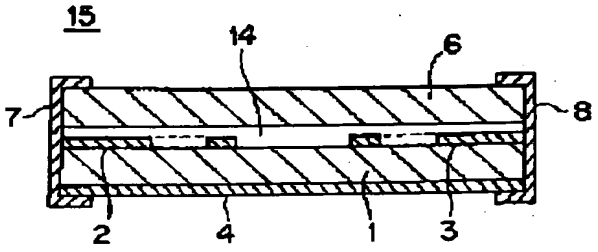
APPLICATION DATE : 03-12-93
APPLICATION NUMBER : 05303968

APPLICANT : MURATA MFG CO LTD;

INVENTOR : HIROSE TOMONORI;

INT.CL. : H01G 4/40 H01F 17/00 H01G 4/30 // H05K 3/46

TITLE : LAMINATED-TYPE ELECTRONIC PART



ABSTRACT : PURPOSE: To manufacture the laminated-type electronic part, wherein the dispersion of the bonding strength between substrates is small, and the reliability of the bonding strength is improved.

CONSTITUTION: On a ceramic substrate I, on the surface of which strip lines 2 and 3 are provided, a ceramic substrate 6 is bonded through a highly heat resistant, and thermoplastic. polyimide bonding agent layer 14. At this time, the thickness of the polyimide bonding agent layer 14 is set at the value, which is twice or more of the thickness of the strip lines 2 and 3.

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0001943-0 7 June 2000 (07.06.2000) SE

(71) Applicant *(for all designated States except US)*: **BLUETRONICS AB** [SE/SE]; S:t Petersgatan 19, S-601 86 Norrköping (SE).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **GONG, Shaofang** [MY/SE]; Åselstadsvägen 140, S-603 66 Norrköping (SE). **NILSSON, Johan** [SE/SE]; Sandgatan 22A, S-602 21 Norrköping (SE).

(74) Agents: **ÖRTENBLAD, Bertil** et al.; Noréns Patentbyrå AB, P.O. Box 10198, S-100 55 Stockholm (SE).

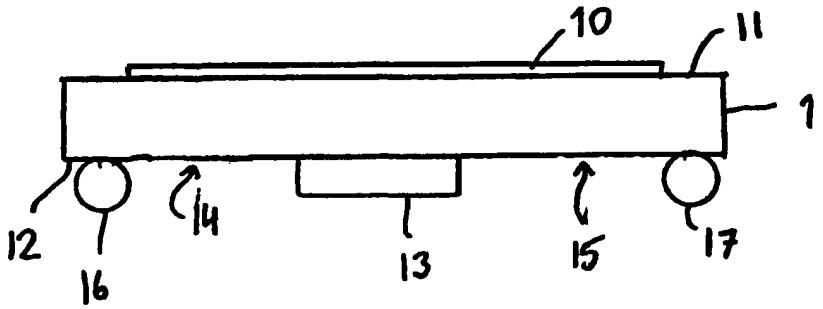
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(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

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(54) Title: MODULE FOR RADIO COMMUNICATION



(57) Abstract: A module for radio communication in accordance with the Blue Tooth concept and/or in accordance with the wireless-LAN concept, wherein the module comprises a transmitter-and-receiver circuit and an antenna. The invention is characterised in that the module comprises a carrier in the form of a laminated PCB-card (1) (Printed Circuit Board) that includes a number of electrically conductive metal layers (M1-M5) and so-called microvias; in that a first side (11) of the card (1) has an integrated antenna (10) formed in the metal layer (M5) on said side and connected to the remainder of the module; in that a radio frequency chip (13) is surface-mounted on the PCB-card (1) on other side (12) of said card; in that passive components (14, 15), such as filters, Baluns, inductors and capacitors, are integrated in the PCB-card (1) and connected to different microvias; and in that terminals in the form of BGA balls (16, 17) (Ball Grid Array) are provided on said second side (12) of the card.

WO 01/95679 A1

MODULE FOR RADIO COMMUNICATION

The present invention relates to a radio communications module and more specifically to a module for communication in accordance with the Blue Tooth concept and the Wireless LAN (WLAN) concept.

The main purpose of the Blue Tooth concept is to replace cables with radio signals when the range required is relatively short. The main purpose of WLAN is to obtain wireless access to the Internet.

Both techniques use the ISM (Industrial, Scientific and Medical) frequency band. Blue Tooth will operate at 2.4 GHz, whereas WLAN will operate at both 2.4 and 5.7 GHz.

In coming years, hundreds of millions of modules for these techniques will be required when the techniques are introduced onto the market.

Consequently, it is a desire that modules for these techniques will be small and can be produced in large numbers at low cost.

The present invention satisfies these desiderata.

Accordingly, the present invention relates to a module for radio communication in accordance with the Blue Tooth concept and/or in accordance with the wireless LAN concept, said module comprising a transmitter and receiver circuit and an antenna, wherein the module is characterised in that it comprises a carrier in the form of a laminated PCB – card (Printed Circuit Board) that includes a plurality of electrically conductive metal layers and so called microvias; in that a first side of the board carries an integrated antenna formed in the metal layer on said side and connected to the remainder of the module; in that the other side, of the card carries a surface-mounted radio frequency chip; in that passive components, such as filters, Baluns, inductors and capacitors, are integrated in the PCB-card and connected to different microvias; and in that terminals in the form of BGA balls (Ball Grid Array) are disposed on said other side of the card.

The invention will now be described in more detail partly with reference to an exemplifying embodiment of the invention illustrated in the accompanying drawing, in which

- Figure 1 is a side view of an inventive module;
- Figure 2 is a sectioned view through a PCB-card that includes so called microvias and a through-penetrating via;
- Figure 3 shows an integrated capacitor from above; and
- Figure 4 shows an integrated coil from above.

According to known technology, passive radio frequency components are mounted on a typical PCB-card (Printed Circuit Board) as discrete components together with semiconductor chips. More advanced technology uses thin films and ceramic multilayers to integrate certain passive components, such as filters and inductances. However, such technologies result in higher production costs than conventional PCB technology.

The present invention relates to a module that is fully integrated for Blue Tooth or WLAN.

Accordingly, the invention relates to a module for radio communication in accordance with the Blue Tooth concept and/or in accordance with the wireless LAN concept, comprising a transmitter and receiver circuit and an antenna.

In accordance with the invention, the module includes a carrier in the form of a laminated PCB-card (Printed Circuit Board) 1 that has a number of electrically conductive layers interconnected with so-called microvias. Figure 2 illustrates microvias 2, 3, 4. The reference signs M1, M2, M3, M4 and M5 identify metal layers that are separated by dielectric material 6, 7, 8 and 9. The dielectric layer 6 suitably has a thickness of 0.8 to 1.5 mm, whereas the layers 7, 8 and 9 have a thickness of 0.05 mm.

The microvias function to connect the various metal layers together and also to connect components to the board 1.

M5 in Figure 2 is used to pattern and form the antenna 10. The layers M1-M4 are used as transmission conductors and integrated passive components, such as filters, Baluns, inductances and capacitances.

According to the invention, the antenna 10 is provided on a first side 11 of the card 1 and is connected to the layer M1 through a through-penetrating via 18. The thickness of the antenna in Figure 1 has been exaggerated. The antenna is conveniently a so-called patch antenna of a quarter wavelength. However, other types of antenna may be used, such as a so-called microstrip antenna or a loop antenna.

A radio frequency chip 13 is surface-mounted on the other side 12 of the card. Passive components 14, 15, such as filters, Baluns, inductors and capacitors are integrated in the Printed Circuit Board.

According to the invention, said other side 12 of the card carries terminals in the form of BGA balls 16, 17 (Ball Grid Array).

There is therewith formed a fully integrated communications module, which is connected to a circuit card through the medium of the BGA balls.

It will be understood that the number of metal layers may be greater or smaller than the number described above.

According to one preferred embodiment, one or more passive components of the aforesaid kind are integrated in the card 1 and formed by means of said metal layers M1-M4. Figure 2 shows in the central part 18 of the figure a capacitor formed by means of the metal layers. Figure 3 shows the capacitor from above as formed in the metal layers M1-M4.

The arrows in Figure 1 show the capacitor 14 and the coil 15 situated within the PCB-card.

Figure 4 shows from above a coil formed in the metal layer M1 or M2 in the right-hand part 19 of Figure 2.

The present invention provides a number of significant advantages over known technology. One significant advantage is that the module can be made very small. With a quarter-wavelength antenna, the external measurements of the module may be 16x18x2.5 millimetres. There is also obtained a high radio quality owing to the absence of parasitic capacitances and inductances in electrical connections. Another advantage resides in the high sensitivity of the module, owing to the fact that requisite filters and Baluns are integrated in the structure. The cost of manufacture is also low.

Although the invention has been described above with reference to a number of exemplifying embodiments, it will be understood that the structural details of the module can be modified in accordance with the construction desired and desired performance.

Consequently, the present invention shall not be considered to be limited to the aforedescribed exemplifying embodiments thereof, since variations can be made within the scope of the accompanying Claims.

CLAIMS

1. A module for radio communication in accordance with the Blue Tooth concept and/or in accordance with the wireless-LAN concept, wherein the module comprises a transmitter-and-receiver circuit and an antenna, **characterised** in that the module comprises a carrier in the form of a laminated PCB-card (1) (Printed Circuit Board) that includes a number of electrically conductive metal layers (M1-M5) and so-called microvias; in that a first side (11) of the card (1) has an integrated antenna (10) formed in the metal layer (M5) on said side and connected to the remainder of the module; in that a radio frequency chip (13) is surface-mounted on the PCB-card (1) on the other side (12) of said card, and in that passive components (14, 15), such as filters, Baluns, inductors and capacitors, are integrated in the PCB-card (1) and connected to different microvias; and in that terminals in the form of BGA balls (16, 17) (Ball Grid Array) are provided on said second side (12) of the card.

2. A module according to Claim 1, **characterised** in that passive components of the aforesaid kind are integrated in the card (1) and formed by means of said metal layers (M1-M4).

3. A module according to Claim 1 or Claim 2, **characterised** in that said antenna (10) is connected to the metal layer (M1) located on said second side (12), by means of a through-passing via (18).

Fig 1

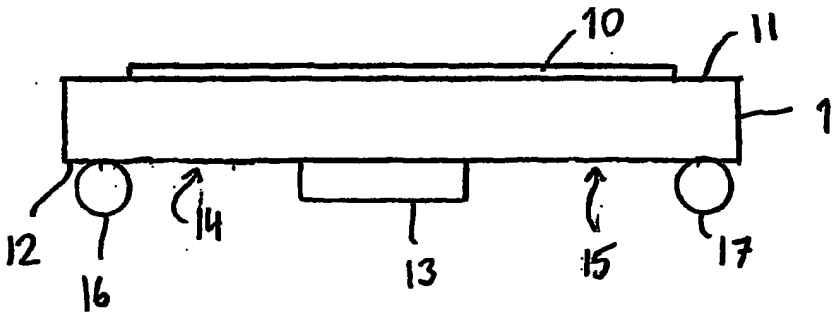
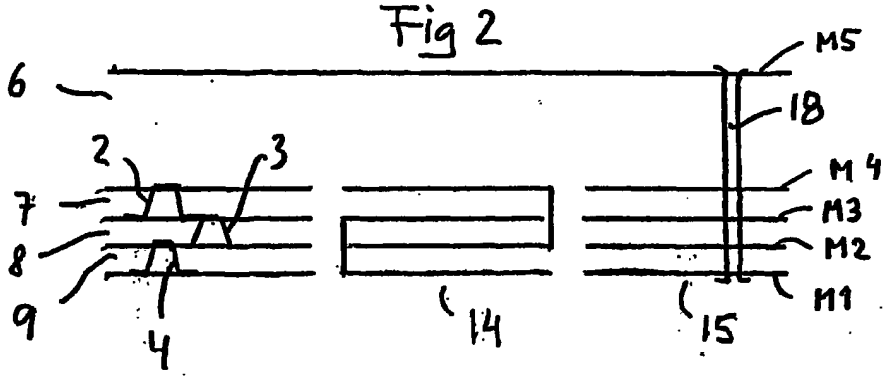


Fig 2



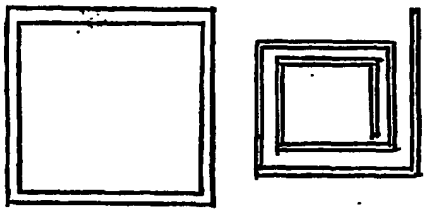


Fig 3 Fig 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 01/00949

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: H05K 1/16
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: H05K, H01L, H01Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-INTERNAL, WPI-DATA, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	DE 19813767 A1 (KABUSHIKI KAISHA TOSHIBA, KAWASAKI), 8 October 1998 (08.10.98), column 8, line 9 - column 9, line 43, abstract --	1-3
Y	US 6021050 A (MICHAEL F. EHMAN ET AL), 1 February 2000 (01.02.00), column 1, line 50 - column 2, line 25; column 2, line 60 - column 5, line 42 --	1,2
Y	GB 2321787 A (NOKIA MOBILE PHONES LIMITED), 5 August 1998 (05.08.98), page 1, line 1 - line 16; page 3, line 5 - line 10 --	1,3

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents:
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Date of the actual completion of the international search	Date of mailing of the international search report
8 August 2001	13 -08- 2001
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Antonio Farieta/mj Telephone No. +46 8 782 25 00

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 01/00949

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6060954 A (CHIA-WEI LIU ET AL), 9 May 2000 (09.05.00), column 1, line 26 - line 67 --	1-3
A	EP 0962968 A2 (MURATA MANUFACTURING CO., LTD.), 8 December 1999 (08.12.99), column 4, line 12 - column 14, line 44 -- --------	1-3

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INTERNATIONAL SEARCH REPORT

Information on patent family members

02/07/01

International application No.
PCT/SE 01/00949

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE 19813767 A1	08/10/98	JP 10276113 A	13/10/98
US 6021050 A	01/02/00	AU 1926900 A	19/06/00
		WO 0033626 A	08/06/00
GB 2321787 A	05/08/98	EP 0951629 A	27/10/99
		GB 2335736 A	29/09/99
		GB 9702010 D	00/00/00
		GB 9915426 D	00/00/00
US 6060954 A	09/05/00	DE 29808363 U	30/07/98
EP 0962968 A2	08/12/99	JP 11354924 A	24/12/99
		US 6228196 B	08/05/01
		JP 2000036665 A	02/02/00

Form PCT/ISA/210 (patent family annex) (July 1998)

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APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/114,733	04/25/2005	Govind	19667-0012

CONFIRMATION NO. 1270

29052
SUTHERLAND ASBILL & BRENNAN LLP
999 PEACHTREE STREET, N.E.
ATLANTA, GA 30309

FORMALITIES LETTER

OC000000016085736

Date Mailed: 05/20/2005

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

07/26/2005 MBERHE 00000074 11114733

01 FC:2051 65.00 OP

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing. *A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.*
  Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(f) of $65 for a small entity in compliance with 37 CFR 1.27, must be submitted with the missing items identified in this letter.

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121(d) are required. The drawings submitted are not acceptable because:
  - The drawings have a line quality that is too light to be reproduced (weight of all lines and letters must be heavy enough to permit adequate reproduction) or text that is illegible (reference characters, sheet numbers, and view numbers must be plain and legible) see 37 CFR 1.84(l) and (p)(1)); See Figure(s) 33.
  - The drawings submitted to the Office are not electronically reproducible. Drawing sheets must be submitted on paper, which is flexible, strong, white, smooth, non-shiny, and durable (see 37 CFR 1.84(e)). See Figure(s) 12, 16D, 19, 31C, 35.

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to

exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$65** for a Small Entity

- **$65** Late oath or declaration Surcharge.

Replies should be mailed to: Mail Stop Missing Parts
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A copy of this notice MUST be returned with the reply.

Tina Jones

Office of Initial Patent Examination (703) 308-1202

PART 2 - COPY TO BE RETURNED WITH RESPONSE

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CERTIFICATE OF MAILING

I hereby certify that the below listed items are being deposited with the U.S. Postal Service as first class mail in an envelope addressed to:

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on July 22, 2005.

Julie Campbell

Julie Campbell

In Re Application Of: Govind, et al.

Group No.: 2681

Serial No.: 11/114,733

Docket No. 062020-1950

Filed: 04/25/2005

Confirmation No.: 1270

For: **Multi-Band Transceiver with Passive Reuse in Organic Substrates**

The following is a list of documents enclosed:

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Response to Missing Parts
Copy of Notice of Missing Parts – Filing Date Granted
Change of Correspondence Address
Petition for Extension of Time (1 Month)
Credit Card Payment for $125.00

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JUL 25 2005
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application Of: Govind, et al.

Group No.: 2681

Serial No.: 11/114,733

Docket No. 062020-1950

Filed: 04/25/2005

Confirmation No.: 1270

For: **Multi-Band Transceiver with Passive Reuse in Organic Substrates**

RESPONSE TO MISSING PARTS NOTICE

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

In response to the Notice to File Missing Parts of Application, Filing Date Granted, dated May 20, 2005, please find enclosed:

1. Declaration and Power of Attorney;
2. Change of Attorney's Correspondence Address;
2. A copy of the Notice to File Missing Parts of Application, Filing Date Granted; and
3. Government fee in the amount of $65.00 to cover the additional surcharge fee for filing this Response to the Missing Parts Notice, plus $60.00 for one month Extension of Time to file the Missing Parts Notice.

The Commissioner is authorized to charge Deposit Account 20-0778 for any deficiencies or credit any over payments.

Respectfully Submitted,

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.

By: _____
Scott A. Horstemeyer, Reg. No. 34,183

Suite 1750, 100 Galleria Parkway
Atlanta, Georgia 30339-5948
(770) 933-9500

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JUL 25 2005
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DECLARATION FOR PATENT APPLICATION

Attorney Docket No: **062020-1950**

As the below named inventor(s), I/we hereby declare that:

Our residences, post office addresses and citizenships are as stated below next to our names.
We believe we are the original, first, and joint inventors of the subject matter which is claimed and for which a patent is sought on the invention entitled , the specification of which:

- ☐ is attached hereto.
- ☒ was filed on **April 25, 2005** as Application Serial No. **11/114,733**.
- ☐ was filed on _____ under U.S. Express Mail No. _____.
- ☐ is set forth in PCT International Application No. _____; filed on _____ and as amended Under PCT Article 19 on _____ (if any).

I/we hereby state that I/we have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I/we acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I/we hereby claim foreign priority benefits under Title 35, United States Code, 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America listed below and have also identified below any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed. **NOT APPLICABLE.**

I/we hereby appoint all attorneys and agents of Thomas, Kayden, Horstemeyer & Risley, LLP, who are listed under the USPTO Customer Number shown below as my/our attorneys and agents to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith, recognizing that the specific attorneys and agents listed under that Customer Number may be changed from time to time at the sole discretion of Thomas, Kayden, Horstemeyer & Risley, LLP, and request that all correspondence be addressed to the address filed under the same USTPO Customer Number.

24504

Please address all telephone calls, in the first instance, to **Scott A. Horstemeyer** at telephone number: **(770) 933-9500.**

Address all correspondence to:

Scott A. Horstemeyer
THOMAS, KAYDEN, HORSTEMEYER
& RISLEY, L.L.P.
100 Galleria Parkway, N.W., Suite 1750
Atlanta, Georgia 30339-5948

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I/we hereby declare that all statements made herein of my/our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statement and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First Inventor: **Vinu Govind**
Residence: 4201 Pace's Park Dr. Decatur GA 30033 Citizenship: India
Post Office Address: **Same as Residence**

Inventor's Signature: _____ Date: 7/20/05

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Full Name of First Inventor: **Sidharth Dalmia**
Residence: **3206, Greenwood Oak Drive, Norcross, GA 30092** Citizenship: **India**
Post Office Address: **Same as Residence**

Inventor's Signature: _____ Date: 7/20/05

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Full Name of Second Inventor: Amit Bavisi
Residence: 1280 West Peachtree Street, Apt 3703, Atlanta, Ga 30309 Citizenship: India

Post Office Address: Same as Residence

Inventor's Signature: A. D. Bavisi Date: 07/20/05.

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Full Name of Third Inventor: Venkatesh Sundraram
Residence: 5362 Medlock Corners Drive, Norcross, GA 30092 Citizenship: India
Post Office Address: Same as Residence

Inventor's Signature: S. Venkatesh Date: 7-20-05

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Full Name of Third Inventor: **Madhavan Swaminathan**
Residence: **1458 Grovehurst Drive, Marietta, GA 30062** Citizenship: **India**
Post Office Address: **Same as Residence**

Inventor's Signature: S. Madhavan Date: 7/2-/05

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Full Name of Third Inventor: George White
Residence: 2836 Saddlebrook Drive, Marietta, GA 30064 Citizenship: USA
Post Office Address: Same as Residence

Inventor's Signature: George White Date: 7/20/05

OIPE JC131 JUL 25 2005 PATENT & TRADEMARK OFFICE

PTO/SB/122(06-03)
Approved for use through 10/31/02. OMB 0651-0035
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CHANGE OF CORRESPONDENCE ADDRESS

APPLICATION

Address to:
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Alexandria, VA 22313-1450

Application Number	11/114,733
Filing Date	04/25/2005
First Named Inventor	Govind
Art Unit	2681
Examiner Name	To Be Assigned
Attorney Docket Number	062020-1950

Please change the Correspondence Address for the above-identified patent to:

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Address	**Suite 1750**				
City	**Atlanta**	State	**GA**	ZIP	**30152**
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I am the:

- ☐ Applicant/Inventor
- ☐ Assignee of record of the entire interest. See 37 CFR 3.71
  Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☒ Attorney or agent of record
- ☐ Registered practitioner named in the application transmittal letter in an application without an executed oath or declaration. See 37 CFR 1.33(a)(1). Registration Number _____.

Type or Printed Name	**Scott A. Horstemeyer, Reg. No. 34,183**
Signature	Scott Horstemeyer
Date	07/22/05

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representatives(s) are required. Submit multiple forms if more than one signature is required, see below.*

☐ * Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.13. The collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Office, U.S. Patent and Trademark Office, P.O. Box 1450, Arlington, Virginia 22313-1450 DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. Send Fees and Completed Forms to the following address: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450

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JUL 25 2005 PATENT & TRADEMARK OFFICE

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a) FY 2005 *(Fees pursuant to the Consolidated Appropriations act, 2005 (H.R. 4818).)*	Docket No. **062020-1950**
Application Number: **11/114,733**	Filed: **04/25/2005**
For: **Multi-Band RF Transceiver with Passive Reuse in Organic Substrates**	
Art Unit: **2681**	Examiner: **To be Assigned**

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

		Fees	Small Entity Fees	
☒	One month (37 CFR 1.17(a)(1))	$120	$60	$**60.00**
☐	Two months (37 CFR 1.17(a)(2))	$450	$225	$
☐	Three months (37 CFR 1.17(a)(3))	$1020	$510	$
☐	Four months (37 CFR 1.17(a)(4))	$1590	$795	$
☐	Five months (37 CFR 1.17(a)(5))	$2160	$1080	$

☒ Applicant claims small entity status. See 37 CFR 1.27

☐ A check in the amount of the fee is enclosed.

☒ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☒ The Commissioner is hereby authorized to charge any deficiencies in fees which any be required, or credit any overpayment to Deposit Account No. 20-0778. A duplicate copy is enclosed.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96).

☒ attorney or agent of record. Registration Number 34,183

☐ attorney or agent under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

Scott A. Horstemeyer, Reg. No. 34,183	**July 22, 2005** Date
	770-933-9500 Telephone Number

☐ Total of forms are submitted.

The collection of information is required by CFR 1.136(a). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 USC 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, US Patent and Trademark Office, US Department of Commerce, PO Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES RO COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, PO Box 1450 Alexandria, VA 22313-1450.

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PTO/SB/05 (09-04)

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	**19667-0012**
Named Inventor(s)	**Govind et al.**
Title	**Multi-band RF Transceiver With Passive Reuse In Organic Substrates**
Express Mail Label No.	**EV 416352332 US**

112963 U.S.PTO
11/114733
042505

APPLICATION ELEMENTS

ADDRESS TO: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

1. ☒ **Fee Transmittal Form** (e.g., PTO/SB/17)
(Submit an original, and a duplicate for fee processing)
2. ☒ **Applicant claims small entity status.**
See 37 CFR 1.27.
3. ☒ **Specification** Total Pages: **48**
Both the claims and abstract must start on a new page
(For information on the preferred arrangement, see MPEP 608.01(a))
4. ☒ **Drawing(s)** (35 U.S.C. 113)Total Sheets **49**
5. **Oath or Declaration** Total Pages
   a. ☐ Newly executed (original or copy)
   b. ☐ A copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 18 completed)
   (i) ☐ DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. ☐ **Application Data Sheet.** See 37 CFR 1.76
7. ☐ **CD-ROM or CD-R** in duplicate, large table or Computer Program (Appendix).
   ☐ Landscape Table on CD
8. ☐ **Nucleotide and/or Amino Acid Sequence Submission**
(if applicable, items a. - c. are required)
   a. ☐ Computer Readable Form (CRF)
   b. ☐ Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ paper
   c. ☐ Statement verifying identity of above copies.

ACCOMPANYING APPLICATION PARTS

9. ☐ **Assignment Papers** (cover sheet & documents(s))
Name of Assignee_____
10. ☐ **37 CFR 3.73(b) Statement**
(when there is an assignee)
☐ **Power of Attorney**
11. ☐ **English Translation Document** (*if applicable*)
12. ☐ **Information Disclosure Statement**
(PTO/SB/08 or PTO-1449)
☐ Copies of citations attached
13. ☐ **Preliminary Amendment**
14. ☒ **Return Receipt Postcard** (MPEP 503)
(*Should be specifically itemized*)
15. ☐ **Certified Copy of Priority Document(s)**
(*if foreign priority is claimed*)
16. ☐ **Nonpublication Request** Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.
17. ☐ Other: _____

18. If a **CONTINUING APPLICATION**, *check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:*
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No:
Prior application information: Examiner: Group Art Unit:

19. CUSTOMER NUMBER: **29052**

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AO 1304246.1

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PTO/SB/17 (12-04)

FEE TRANSMITTAL Attorney Docket No. **19667-0012**

This sheet accompanies a patent application transmittal for the following application:

Inventor(s): **Govind et al.**
Filing Date: **April 25, 2005**
Title: **Multi-band RF Transceiver With Passive Reuse In Organic Substates**

The filing fee is calculated as shown below:

1. FILING FEE:

APPLICATION TYPE	FILING FEES FEE	FILING FEES SMALL ENTITY FEE	SEARCH FEES FEE	SEARCH FEES SMALL ENTITY FEE	EXAMINATION FEES FEE	EXAMINATION FEES SMALL ENTITY FEE	FEE(S) PAID
Utility	**300**	150	**500**	250	**200**	100	**$500**
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. CLAIMS:

FOR:	NO. FILED	NO. EXTRA	SMALL ENTITY RATE	SMALL ENTITY FEE	LARGE ENTITY RATE	LARGE ENTITY FEE
TOTAL CLAIMS	32 - 20 or HP*=	12	**x 25 =**	**300**	**x 50 =**	
INDEP. CLAIMS	4 - 3 or HP*=	1	**x 100 =**	**100**	**x 200 =**	
☐ MULTIPLE DEPENDENT CLAIM PRESENTED			**+180 =**	**0**	**+360 =**	
*HP = Highest number paid for			**FEE(S) PAID:**	400		**$**

3. APPLICATION SIZE FEE: If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(g) and 37 CFR 1.16(s).

TOTAL SHEETS		EXTRA SHEETS	NUMBER OF EACH ADDITIONAL 50 SHEETS OR FRACTION THEREOF (round up to a whole number)	SMALL ENTITY RATE	SMALL ENTITY FEE	LARGE ENTITY RATE	LARGE ENTITY FEE
97	- 100 =	0	**0**	**x 125 =**	**0**	**x 250 =**	
				FEE(S) PAID:	**$0**		**$**

4. ADDITIONAL FEES:

FOR:	SMALL ENTITY FEE	SMALL ENTITY FEE PAID	LARGE ENTITY FEE	LARGE ENTITY FEE PAID
☐ LATE FILING, FEE OR OATH	**$65**		**$130**	
☐ NON-ENGLISH SPECIFICATION	**$130**		**$130**	
☐ OTHER:				
	FEE(S) PAID:	**$**		**$**

TOTAL FILING FEES: $900

A check is enclosed for the total amount:

☐ The Director is hereby authorized to charge any additional fee(s) or underpayment of fee(s) required under 37 C.F.R. 1.16 or 1.17 and credit any overpayments to Deposit Account 19-5029.

☒ The Director is hereby authorized to charge the fee(s) indicated above to Deposit Account 19-5029.

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By: Malvern U. Griffin III - Reg. No. 38,899
Attorney for Applicant

Date: April 25, 2005

AO 1304250.1

MULTI-BAND RF TRANSCEIVER WITH PASSIVE REUSE IN ORGANIC SUBSTRATES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims benefit of U.S. Provisional Application No. 60/565,254, filed April 23, 2004, entitled "Digitally Tunable Compact Multiband Low Noise Amplifiers Through Passive Re-use." This application is also a continuation-in-part of U.S. Patent Application No. 10/402,313, filed March 28, 2003, entitled "Integrated Passive Devices Fabricated Utilizing Multi-Layer, Organic Laminates." All of the foregoing applications are incorporated herein by reference.

BACKGROUND OF THE INVENTION

I. Field of the Invention

[0002] The present invention generally relates to passive components, and more particularly to the chip-package co-design of RF single-band and multi-band transceivers using high quality embedded passive components in organic substrates for use in radio frequency (RF) applications.

II. Description of Related Art

[0003] With a proliferation of wireless standards and applications operating at various frequencies, the need for radio frequency (RF) front-ends and interfaces that support multiple bands ("multi-band") and multiple protocols ("multimode") becomes necessary. As an example, a wireless LAN ("WLAN") device may support IEEE 802.11a/b/g protocols operating at 2.4 GHz or 5.2 GHz. Likewise, a cell phone supporting GSM900, DCS1800 and PCS1900 protocols may operate at 900 MHz, 1800 MHz, or 1900 MHz. Further, with the advent of MIMO (multiple-input multiple-output) based systems, optimization for high data rates and high data ranges using spatial and frequency diversity becomes necessary. Thus, there has been an increasing need for devices that are operable with a variety of wireless

protocols. Such a need may occur for example, in a situation where voice, video (in the cellular band), and data must be handled by the same cellular device.

[0004] Designing multi-band, multi-mode devices such as RF transceivers present some difficulties in power consumption, compatibility, interference, and integration. For example, the need for the additional design components to support such multi-band, multi-mode capabilities oftentimes presents challenges with power consumption. This may be especially problematic in a portable multi-band, multi-mode device such as a cell phone operating on a battery. The battery life of the cell phone would decrease as the power consumption requirements of the components within the cell phone increase. Further, as many devices continue to decrease in size, the inclusion of additional components becomes increasing difficult due to problems such as routing, interference, etc. Achieving the required quality factors (Qs) of these components may become more difficult with these size constraints. In addition, the components may have to conform to improved performance characteristics such as high clock speed, low noise, wide bandwidth, and high temperature tolerance.

[0005] Therefore, there is a need in the industry for multi-band, multimode RF transceivers that may satisfy one or more of these issues of power consumption, compatibility, interference, and integration.

SUMMARY OF THE INVENTION

[0006] The present invention overcomes the difficulties above by describing multi-band, multimode integrated RF transceiver topologies, comprising of on-chip actives and in-package embedded high-Q passives in organic substrates that, in certain circumstances, can be reused at different frequency ranges, thereby reducing the number of components required. Two components of such an RF transceiver include voltage controlled oscillators (VCOs) and low noise amplifiers (LNAs). According to an embodiment, high-performance LNAs with low noise figures (NF) and VCOs with low phase noise may be formed from high-Q passive components embedded in organic substrates such as LCP (liquid crystalline polymer).

[0007] According to an embodiment of the present invention, a multi-band RF device operable at a first frequency and a second frequency different from the first frequency includes an active device, a first passive network in communication with the active device, a second passive network in communication with the active device, and an organic-based substrate having at least two metal layers, wherein the two metal layers are patterned to form at least a portion of the first passive network and the second passive network, wherein impedances of the first and second passive networks are different at the first frequency than the second frequency.

[0008] According to another embodiment of the present invention, an RF multi-band oscillator for simultaneously generating oscillation signals at a first frequency and a second frequency for a multi-band transceiver includes an organic layer having a top surface and a bottom surface, a first metal layer opposite the top surface, a second metal layer opposite the bottom surface, wherein the first metal layer and the second metal layer are patterned to form a first resonator and a second resonator, wherein a reactance of the first resonator at the first frequency differs from a reactance at the second frequency and wherein a reactance of the second resonator at the first frequency differs from a reactance at the second frequency, and an active device in communication with the first resonator and the second resonator to form a feedback network, thereby simultaneously generating oscillation signals at the first frequency and the second frequency.

[0009] According to another embodiment of the present invention, a multi-band low noise amplifier for use in an RF application includes an active device, a first matching network in communication with the active device, wherein an impedance of the first matching network at a first frequency is different than the impedance of the first matching network at a second frequency, a second matching network in communication with the active device, wherein an impedance of the second matching network at the first frequency is different than the impedance of the second matching network at the second frequency, and a multi-layer organic-based substrate having at least one metal layer, wherein the first matching network and the second matching are formed on the at least one metal layer and wherein the active device is mounted on the multi-layer organic substrate, thereby allowing

the an output of the multi-band low noise amplifier to have desired power gains at the first frequency and the second frequency based at least in part on each of the first and second matching networks having the different reactance at the first frequency and the second frequency.

[0010] According to yet another embodiment of the present invention, An oscillator for use in an RF transceiver includes a first organic layer with a top surface and a bottom surface opposite the top surface, a first conductive layer positioned on the top surface of the first organic layer, a second conductive layer positioned on the bottom surface of the first organic layer, a second organic layer positioned opposite the second conductive layer, a plurality of passive devices patterned on at least one of the first conductive layer and the second conductive layer, and at least one discrete active device positioned on the first conductive layer and in communication with at least a portion the plurality of passive devices, wherein a feedback network for the active device is created such the discrete active device becomes unstable and generates at least one signal at a particular frequency.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0011] Having thus described the invention in general terms, reference will now be made to the accompanying drawings, which are not necessarily drawn to scale, and wherein:

[0012] FIG. 1A is a first equivalent circuit diagram for explaining the operation of the dielectric filters shown in FIGS. 2, 3 and 4.

[0013] FIG. 1B is a second equivalent circuit diagram for explaining the operation of the dielectric filter of FIG. 1A using transmission lines or inductor resonator elements.

[0014] FIGS. 2A-2C show several views of a first organic dielectric filter according to an embodiment of the present invention.

[0015] FIGS. 3A-3C show several views of a second organic dielectric filter according to an embodiment of the present invention.

[0016] FIGS. 4A-4B show several views of a third organic dielectric filter according to an embodiment of the present invention.

[0017] FIG. 5 illustrates a fabrication methodology for an organic dielectric filter according to the present invention, such as the first organic dielectric filter of FIGS. 2A-2C.

[0018] FIG. 6 illustrates a fabrication methodology for an organic dielectric filter according to the present invention, such as the organic dielectric filter of FIGS. 3A-3C.

[0019] FIG. 7 is an X-ray from a top plan view of an organic bandpass filter in accordance with an embodiment of the present invention.

[0020] FIG. 8 is an X-ray from a side perspective view of the organic bandpass filter of FIG. 7.

[0021] FIG. 9 is a graphical representation of a model to hardware correlation for the organic bandpass filter of FIG. 7.

[0022] FIG. 10 is a picture from a top plan view of a BGA style organic filter, in accordance with an embodiment of the present invention.

[0023] FIG. 11 is a graphical representation of measured and modeled data for the BGA style organic filter in FIG. 10.

[0024] FIG. 12 is a picture from a top plan view of an organic dielectric filter that includes SMD capacitors in accordance with an embodiment of the present invention.

[0025] FIG 13 is a graphical representation of a model to hardware correlation for the organic dielectric filter in FIG.12.

[0026] FIG. 14 illustrates an exemplary multi-band receiver portion of a transceiver in accordance with an embodiment of the present invention.

[0027] FIG. 15 illustrates another exemplary multi-band receiver portion of a transceiver.

[0028] FIG. 16A illustrates a circuit diagram of an oscillator that can be implemented using high-Q passive components fabricated on organic substrates in accordance with an embodiment of the present invention.

[0029] FIG. 16B illustrates an exemplary stackup for implementing the circuit diagram in FIG. 16A in accordance with an embodiment of the present invention.

[0030] FIGs. 16C and 16D illustrate exemplary layouts corresponding to metal layers in FIG. 16B in accordance with an embodiment of the present invention.

[0031] FIG. 17 is a simulated waveform for the exemplary circuit diagram of FIG. 16A.

[0032] FIG. 18 is a measured output power for the fabricated oscillator of FIGs. 16A-D in accordance with an embodiment of the present invention.

[0033] FIGs. 19 and 20 show the measured performance of the oscillator of FIG. 16A at 3.3 GHz and 5.2 GHz, respectively, when fabricated using an epoxy substrate in accordance with an embodiment of the present invention.

[0034] FIGs. 21 and 22 illustrates alternative circuit diagrams of oscillators that can be implemented in accordance with an embodiment of the present invention.

[0035] FIG. 23A illustrates another exemplary oscillator that can be implemented according to an embodiment of the present invention.

[0036] FIG. 23B illustrates an exemplary stackup for the oscillator shown in FIG. 23A in accordance with an embodiment of the present invention.

[0037] FIG. 24A, 24B, and 25 show measured characteristic of the oscillator of FIGs. 23A and 23B.

[0038] FIG. 26 illustrates a comparison of voltage controlled oscillators fabricated with various technologies.

[0039] FIG. 27 illustrates an exemplary concurrent, multi-band oscillator in accordance with an embodiment of the present invention.

[0040] FIG. 28 illustrates a multi-band filter in accordance with an embodiment of the present invention.

[0041] FIG. 29 shows a broad-band simulated response of a dual-band filter in accordance with an embodiment of the present invention.

[0042] FIG. 30 shows a transient simulation of the oscillator of FIG. 27 in accordance with an embodiment of the present invention.

[0043] FIG. 31A shows another exemplary circuit of a concurrent, multi-band oscillator in accordance with an embodiment of the present invention.

[0044] FIG. 31B illustrates an exemplary stackup for the oscillator of FIG. 31A in accordance with an embodiment of the present invention.

[0045] FIG. 31C shows a top view of a layout for the oscillator of FIG. 31A in accordance with an embodiment of the present invention.

[0046] FIG. 32 shows the loop gain and the loop gain criterion of the oscillator of FIG. 31A.

[0047] FIG. 33 shows a simulated response of a filter in accordance with an embodiment of the present invention.

[0048] FIG. 34 shows a transient response of the concurrent, multi-band oscillator of FIG. 28A.

[0049] FIG. 35 shows and exemplary circuit diagram of a low noise amplifier in accordance with an embodiment of the present invention.

[0050] FIG. 36 shows the measured gain and input match for the low noise amplifier of FIG. 35.

[0051] FIG. 37 shows the measured gain and input match for the low noise amplifier of FIG. 35.

[0052] FIGS. 38A-38F illustrates substrate variations according to an embodiment of the present invention.

DETAILED DESCRIPTION

[0053] The present inventions now will be described more fully hereinafter with reference to the accompanying drawings, in which some, but not all embodiments of the invention are shown. Indeed, these inventions may be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will satisfy applicable legal requirements. Like numbers refer to like elements throughout.

I. Filters

[0054] The operation of a filter in accordance with the present invention is explained below with reference to the bandpass filter 10 of FIG. 1A. However, it will be appreciated by those of ordinary skill in the art that the teachings of the present invention readily apply to other integrated passive devices. Accordingly, the scope of the present invention is not limited to bandpass filters, but is inclusive of other devices such as but not limited to diplexer, duplexer, multiplexer, baluns, power combiner, band-stop/band elimination filter, power divider, low-pass filter, high-pass filter, voltage controlled oscillators (VCOs), and low noise amplifiers (LNAs).

[0055] With reference to the figures, FIG. 1A is an equivalent circuit diagram of a dielectric bandpass filter 10 in accordance with the present invention. In FIG. 1A, inductors

12, 14 cooperate with their corresponding capacitor 16, 18, respectively, to form resonators 20, 22, respectively. The inductors 12, 14 correspond to the stripline or CPW/strip-line or CPW/microstrip inductors discussed below with reference to FIGS. 2-4. The capacitors 16 and 18, respectively, correspond to the capacitors formed on the same layer as inductors 12 and 14 or by using discrete capacitors. The capacitor 24 corresponds to the capacitor formed for the purposes of inter-resonator coupling. In FIG. 1A, capacitors 26 and 28, respectively, provide matching to the desired impedances at the input and output. In addition, M is the magnetic coupling between the inductors 12 and 14. The inductances of inductors 12 and 14 could also represent equivalent inductance components of the resonators, and capacitances of capacitors 16 and 18 could represent capacitance components of the resonators. While the circuit topology shown in FIG. 1A depicts one embodiment of a two pole filter, and an additional pole can be attained by the mutual inductance between inductors 12, 14 and the capacitor 24. In addition, resonators may be added with the required coupling elements by adding more inductors and capacitors in various configurations to achieve transfer characteristics that emulate such responses as first order, second order to nth order butterworth, chebychev, elliptic, blinkoff, symmetric, asymmetric, notch added filters using topologies such as nodal capacitor coupled, nodal-inductor coupled, shunt-input geometry, input geometry or mesh capacitor coupled.

[0056] The stopband characteristics of a filter is a prime factor in determining the isolation between the transmitting and receiving paths in duplexer designs. It is well known that the stopband rejection may be enhanced, either by increasing the number of resonators as mentioned earlier, or by adding transmission zeros.

[0057] FIG. 1B is an alternative equivalent circuit diagram 10 of a dielectric filter using transmission lines or inductor resonator elements, wherein the inductors 112 resonate at a desired center frequency. The physical parameters of the circuit 110, such as the number of turns, length of conductor, outer and inner diameter, can be altered to resonate the inductor 112 at the desired frequency. This reduces the number of components required to achieve a filtering function by removing the need for capacitors of the resonators. However, a disadvantage is the increase in length of the metallization to increase the capacitance, though

the increased inductance could increase loss in the circuit. If the inductor element becomes too large or too lossy, then it may be desirable to use an alternative circuit design, such as that illustrated in FIG. 1A. It should be noted that in the circuits of FIG. 1A and FIG. 1B, the coupling between the components can be achieved by magnetic coupling, electric coupling or a combination thereof.

[0058] Illustrative physical layouts of dielectric filters in accordance with the equivalent circuit diagram of FIG. 1A are depicted in FIGS. 2-4. The dielectric filters of FIGS. 2-4 have a two-pole structure and an additional pole attained by the mutual inductance and the capacitor 24 according to the equivalent circuit diagram shown in FIG. 1A.

[0059] With general reference to FIGS. 2A-2C, illustrated is a surface mounted device (SMD) embodiment of the filter illustrated by the circuit of FIG. 1A in accordance with the present invention. Specifically, the organic bandpass filter 200 comprises inductors 212 and 214, which are meandering inductors formed close to each other on an organic dielectric layer 236 (which can be a thin laminate such as LCP or PPE, but is not limited to these) and is preferably configured as either a shorted hybrid CPW-stripline (where lines that form meandering inductors 212 and 214 are connected to a coplanar ground, that is, in-built shielding 230), or a stripline in the presence of coplanar in-built shielding 230 and additional grounds 248 and 250 that are connected to the plated through holes 232 and/or external shield electrodes 234.

[0060] Since these inductors are very close to each other, the magnetic coupling between these filters, represented by M in FIG. 1A, can increase the pass bandwidth of the filter, thereby decreasing its performance. However, an inter-resonator parallel plate coupling capacitor 224, (with or without the coplanar in-built shielding 230) formed using two disconnected metal plates (one plate formed using patterning conductive layer 238 and the other plate formed using patterned conductive layer 240) and shown as capacitor plates 224a, 224b is provided. The capacitor plates 224a, 224b sandwich the first organic dielectric layer 236 in such a manner that the each plate of the inter-resonator coupling capacitor electrode is connected to separate resonators which helps compensate the effect of the

magnetic coupling and helps make very compact filters. The center capacitance can be as small as femptoFarads or as large as picoFarads for achieving the specified bandwidths. The smaller capacitance helps reduce the bandwidth. Additionally, capacitor 224 in parallel with the mutual inductance equivalent gives a pole in the lower band or upper band.

[0061] The bottom plate formed by the conductive layer 240 connects to inductor 212 using one or more microvias in the organic dielectric layer 236, such as the vias 244 with pads 246 for landing and capturing the via. First and second shield electrodes 248, 250 formed respectively on the organic core layers 252, 254, wherein the core layer 252 and 254 are disposed so as to sandwich the organic dielectric layer 236 there between. A first resonator 260 formed by inductor 212 and capacitor 216 and a second resonator 262 formed by inductor 214 and capacitor 218 are electrically coupled to each other through the parallel plate capacitor 224, whereby an inter-resonator coupling is effected in combination with said magnetic coupling and electric coupling.

[0062] In a dielectric filter according to the present invention, where the inductors do not provide the needed capacitance in the desired length, the inductors 212, 214 can be connected in similar fashion as the capacitor 224 to separate grounded/shunted parallel plates 216a and 218a, respectively, of capacitors 216 and 218, respectively, using the same first organic dielectric layer 236 as the sandwiched dielectric, which then together form the resonator pairs 260, 262.

[0063] The equivalent inductance L obtained with one of the meander inductors, 212, 214, and the equivalent capacitance C due to one of the capacitors 216, 218, resonates approximately at frequency Fo, the center frequency of the filter, as defined by Equation (1) below:

$$\text{whereby} \quad Fo \sim \sqrt{1/(LC)} \qquad (1)$$

[0064] The capacitor plates 216a and 218a have a corresponding ground plate 217 on the opposite surface of the organic dielectric layer 236. Having a common plate does cause coupling between the capacitors which has to be accounted for during the design by including it as the mutual inductance between the parasitic inductance of each capacitor 216, 218. This coupling can be used to achieve further poles; however if the coupling causes problems in the passband during the synthesis stage it could be reduced by either dividing plate 217 into separate plates or by adding several vias on pads 274 that connect plate 217 to in-built shielding 230 on the side of the inductors 212 and 214, thereby helping excess currents to sink and thereby reducing coupling between components.

[0065] In addition, parallel plate/interdigital capacitors 226 and 228, can be used on either side of the first and last resonator elements 260, 262 at the input and output terminals of the device for impedance matching purposes. Alternatively, inductors or transmission lines or a combination of capacitor(s), inductor(s) and transmission line(s) can be utilized, as desired. If capacitors 226, 228 are used for matching purposes, it follows the center capacitance is that of capacitor 224 in terms of the nominal capacitances required, that is, the capacitance from capacitor 226 and capacitor 228 are proportional to capacitor 224.

[0066] A dielectric filter according to the embodiment of the present invention illustrated in FIGS. 2A-2C can comprise at least two external shield electrodes 234 respectively formed on different side surfaces of the laminated structure, which comprises at least the organic dielectric layer 252, 236, 254, and that are connected to the shield electrodes 248 and 250. This may or may not be desired for shielding purposes in a CPW topology, wherein the use of plated through holes 232 on the four corners is sufficient. Utilizing the plated through holes 232 may save additional room required for the external shield electrodes 234 and also may save the processing cost involved. However, in stripline and microstrip filter topologies, plated through holes 232 and external shield electrodes 234 together provide the connection for the shorted inductors/resonators and capacitors at any point along the respective sides. Alternatively, the CPW topology with coplanar in-built shielding 230 on the same plane of the first dielectric layer provides the shielding internally, and provides for

the ground connectivity to the resonators/inductors and capacitors. However, in general, in more noisy environments it may be preferred to also have the external ground electrodes.

[0067] The dielectric filter 200 also comprises an external input terminal electrode 264 and an external output terminal electrode 266 which are formed on one side surface of a laminated body comprising at least dielectric sheets 252, 236, 254, and an external ground electrode, (such as shield electrodes 248, 250, through holes 232 or side shield electrodes 234) formed between said external input and output terminal electrodes 264, 266 on one side surface.

[0068] The shield electrodes 248 and 250 formed on the dielectric core layers 252 and 254, respectively, are preferably of the shape and patterned to leave room for the landing terminals of input and output terminal electrodes 264 and 266. For purposes of illustrating the present invention, the shield electrodes 248, 250 are shown in FIGS. 2B and 2C, but not 2A.

[0069] The first organic dielectric layer 236 can comprise single side copper LCP laminate or the like, such as PPE, N6000, epoxy based N4000-13, or any other suitable low loss dielectric.

[0070] The protective layers 270, 272 are formed on shield electrodes 248, 250 opposite dielectric core layers 252, 254, respectively, to protect the structure from environmental affects such as oxidation and also to create a pattern for solder to flow on to the input output terminals 264 and 266 and ground pads formed by plated through holes 232. The protective layers 270, 272 may comprise a solder mask, or in more demanding applications, with higher tolerances, other materials such as prepreg or LCP may be desired. For purposes of illustrating the present invention, the protective layers 270, 272 are shown in FIGS. 2A and 2B, but not 2C.

[0071] In the dielectric filter according to the present invention, as illustrated in FIGS. 2A-2C, an initial step to making a connection between devices using vias 244 is done by drilling through holes (as small in diameters as the thickness of the dielectric used) through the LCP layer (or any other appropriate organic dielectric) and copper layer. Then both sides of LCP copper laminate are metallized, such as by electroless or vacuum deposited copper. Copper is then electroplated on both sides of laminate to form the metallized patterns 238, 240 on the organic dielectric layer 236. The copper is then printed and etched to define the key filter components.

[0072] In the dielectric filter according to the embodiment illustrated in FIGS. 2A-2C, the dielectric core layers 252, 254 can be laminate LCP or appropriate dielectric with generally larger thickness than the first substrate and aluminum, copper, Molybenum metal (for high power applications) on both sides of filter to a given thickness to encapsulate components. All metals are preferably electroplate and etched and patterned on top and bottom of the device to leave space for signal input and output.

[0073] In a dielectric filter according to the embodiment illustrated in FIGS. 2A-2C, the side wall ground shield electrodes 232, 234 can be fabricated, if desired, by single or multiple connected drilled and plated through holes or using a saw cutting device and then connected via electroless or sputter seeded copper in through hole. The copper can be electroplated in the through hole and on the surface. The copper can then be printed and etched to form SMD connection. The process flow for a two layer plus the packaging of the SMD device is explained in greater detail in connection with FIG. 5.

[0074] With reference to FIGS. 3A-3C, illustrated, is a BGA/CSP embodiment of an organic bandpass filter 300 in accordance with the present invention. Essentially, all of the internal structure in the filter depicted in FIGS. 2A-2C and FIGS. 3A-3C are similar except the packaging is different, and thereby, the means by which you package it. For example, in FIGS. 3A-3C the thin laminate (e.g., the organic dielectric layer 336) is not packaged between two thick cores, but is packaged with one core layer 354 on one side and a first protective layer 370 on the opposite side substrate 336. The opposite side of the thicker core

354 is metallized to form a shield electrode 350, and a second protective layer 372 is disposed over the shield electrode 350. The protective layers may comprise a solder mask, or in more demanding applications, with higher tolerances, other materials such as prepreg or LCP may be desired.

[0075] This packaging of filter 300 renders a microstrip or CPW/microstrip filter device with only shield electrode 350. Instead of using through holes to connect the device input/output and ground terminals, solder balls 380 are utilized. Side wall ground shield electrodes 334 are used to connect the in-built shielding electrodes 330 and shield electrode 350 and, if desired, to solder balls 380.

[0076] Alternatively, this could be done by plated through holes, if provided. As discussed above, having both plated through holes 332 and side wall shield electrodes 334 is not typically necessary, and generally they can be utilized in the alternative of one another. For purposes of illustrating the present invention, side wall grounded shield electrodes 334 are shown in FIG. 3A-3C. The solder balls 382 connect the input and output terminals to the bandpass filter. The solder balls and the packaging is constructed using the methodology provided below in connection with FIG. 6. The protective layer 370 (also known as a passivation layer mask, solder mask, bondply layer or low temperature thermoset, thermopolymer material compound to inner laminate) may be utilized to provide openings for the solder balls, as well known in the art.

[0077] With reference to FIGS. 4A-4B, illustrated is an embodiment of a filter device 400 in accordance with the present invention, which utilizes discrete capacitors 402 and external shielded formed by a metallic case or cap 404. Essentially, all internal structure in FIGS. 2A-2C and FIG. 3A-3C are similar except the packaging is different in the embodiment of FIGS. 4A-4B, and thereby the means by which you package it. For example, in FIGS. 4A-4C, an organic dielectric layer 436 (e.g., a thin laminate substrate) is not packaged between two thick cores, but only one core layer 454 on one side, wherein a shielding electrode 450 is metallized on the opposite side of the core layer 454. On the other side of the organic dielectric layer 436 is a metallic cap 404 with the appropriate height,

which is used to provide a second ground reference. The organic dielectric layer 436 is metallized on opposing surfaces by patterned conductive layers 438 and 440, which are electrically connected by at least microvias in layer 436, as discussed with regard to the embodiments of FIGS. 2 and 3. Instead of using a thicker core on both sides of the substrate 436, this embodiment uses a core layer on one side and air as a dielectric on the other. This renders itself into a stripline or CPW/stripline device. Through holes are used to connect only the core metal to the internal metallic structure whereas the metallic cap 404 is connected using solder connections to the relative terminals. The metallic cap 404 can have openings where needed for the input and output terminals. It is important to note that the embodiment is not restricted to using discrete capacitors. The capacitors shown in FIGS. 4A-4B can also be embedded in the substrate, if needed, as discussed previously.

[0078] The following are examples of various embodiments of the present invention, wherein each illustrative embodiments discloses several aspects of the invention.

II. Illustrative Methods for Fabricating Stand Alone Filters

[0079] An illustrative process for fabricating an LCP based IPD, such as the filter illustrated in FIGS. 2A-2C, configured as a surface mount device (SMD) in accordance with an embodiment of the present invention is now described with reference generally to FIG. 5. Initially, a starting material is selected, which is preferably a reinforced or non-reinforced LCP laminate that can be unclad, or cladded with copper foil on one or both sides of the LCP, as illustrated in Step 1. Alternate materials include other low loss organic laminates like PPE, PTFE composites, hydrocarbon ceramic composites, BT resin composites (e.g., Speedboard C), and thermosets (e.g., Hitachi MCL-LX-67F). Next, through vias are drilled through the LCP or other laminate and the layers of copper, as illustrated in Step 2. These microvias can be drilled with mechanical drilling, laser drilling or other suitable methods known to those skilled in the art.

[0080] Steps 3 and 4 involve the metallization of the through vias and laminate. In additive, semi-additive, or subtractive processes starting with unclad or copper clad LCP or other laminates, both sides of the LCP or other laminate and the vias are seeded using

electroless plated, vacuum deposited copper or another deposition methods to form a continuous copper film. To achieve the target metal thickness for the device, electrolytic plating is done to build the copper on both sides of the laminate and in the vias in a single step. The circuit definition for the filter component can be done using subtractive, semi-additive or fully additive processes with panel or pattern electroplating of the copper followed by print and etch steps to define the filter circuitry, as illustrated in Step 5.

[0081] The fabricated device circuits are then packaged using vacuum or non-vacuum lamination of LCP or alternate laminate materials as detailed above in connection with Step 1, and/or Al, Cu, Mo metal (for high power applications) on both sides of the filter to provide sufficient thickness to encapsulate components, as illustrated in Step 6. The internal and external metal layers are connected, as needed, using plated through holes that can be drilled mechanically or with laser, photo, or plasma processes to provide signal and ground connections and SMD terminals, as illustrated in Step 7. The two edges of the device without the through hole can also slotted using mechanical drill/rout/mill, laser cutting, or sawing processes to provide for additional shielding of the device during subsequent metallization. The drilled through holes and shielding slots are seeded with electroless plated or sputter/vacuum deposited copper to provide a bus layer in substantially the same manner as described above in connection with Step 3, as illustrated in Step 8.

[0082] With reference to Steps 9, 10, and 11, the final metal thickness for the outer layers is built up by electroplated copper in the through holes, shielding slots, and on the top and bottom surfaces. Subtractive, semi-additive, or additive processes may be used to define the outerlayer ground circuits and SMD terminals for connection, with print and etch processing of the copper, as described above in connection with Steps 4 and 5. The device is then finished with the addition of terminal metals appropriate for SMD assembly and soldering processes. These finishing metals on the device terminals are common plated metals or alloys like electroless Ni-Au, immersion tin, immersion silver, electroplated Ni-Au, solder (HASL), or organic finishes (OSPs) and the choice depends on the intended application.

[0083] The fully fabricated wafer is then singulated into individual filter components. The singulation can be done using high speed dicing saws or alternate methods such as punching or routing/milling. An advantage of this fabrication process is the ability to fully electrical test the components either before or after singulation.

[0084] Another illustrative process for fabricating an LCP based IPD, such as the filter illustrated in FIGS. 3A-3C, configured as a ball grid array (BGA) or chip scale package (CSP) in accordance with an embodiment of the present invention is now described with reference generally to FIG. 6. Initially, a starting material is selected, preferably a reinforced or non-reinforced LCP laminate that can be unclad, or cladded with copper foil on one or both sides of the LCP, as illustrated in Step 1. Alternate materials include other low loss organic laminates like PPE, PTFE composites, hydrocarbon ceramic composites, BT resin composites (e.g., Speedboard C), and thermosets (e.g., Hitachi MCL-LX-67F). Next, through vias are drilled through the LCP or other laminate and the layers of copper, as illustrated in Step 2. The microvias can be drilled with mechanical drilling, laser drilling or other suitable methods known to those skilled in the art.

[0085] Steps 3 and 4 involve the metallization of the through vias and laminate. In additive, semi-additive, or subtractive processes starting with unclad or copper clad LCP or other laminates, both sides of the LCP or other laminate and the vias are seeded using electroless plated, vacuum deposited copper or other common deposition methods to form a continuous copper film. To achieve the target metal thickness for the device, electrolytic plating is done to build the copper on both sides of the laminate and in the vias in a single step. The circuit definition for the filter component can be done using subtractive, semi-additive or fully additive processes with panel or pattern electroplating of copper followed by print and etch steps to define the filter circuitry, as illustrated in Step 5.

[0086] The fabricated device circuits are then packaged using vacuum or non-vacuum lamination of LCP or alternate laminate materials detailed above in connection with Step 1, and/or Al, Cu, Mo metal (for high power applications) on both sides of the filter to a given thickness to encapsulate components, as illustrated in Step 6.

[0087] On the other side of the filter component, a cover coat material, liquid photo imagable (LPI), or dry film solder mask is deposited using standard processes such as spin coating, curtain or roller coating, dry film lamination, spray coating and others, as illustrated in Steps 7, 8 and 9. This layer acts as a barrier to solder flow between terminals during subsequent reflow and component assembly. The component terminals are defined by opening windows in the cover coat / soldermask material to open the BGA pads for board level interconnection. This is done with processes such as photolithography or laser ablation. The device is then finished with the addition of terminal metals appropriate for BGA assembly and soldering processes. These finishing metals on the device terminals are common plated metals or alloys like electroless Ni-Au, immersion tin, immersion silver, electroplated Ni-Au, solder (HASL), or organic finishes (OSPs) and the choice depends on the intended application and compatibility with the solder or other alloy used for device-to-module/ PWB interconnection.

[0088] With general reference to Steps 10, 11, 12, the interconnects are formed in the windows in the manner defined in Step 8 using Pb/Sn solder, or other lead free solders and metal alloys. Processes such as screen or stencil printing of solder paste and reflow, or plating processes can be used to form the bumps for interconnection. The BGA/CSP format of the filter components enables the testing of the components on the large area board prior to singulation. The testing can be done, for example, with probing techniques or using test sockets or fixtures.

[0089] The fully fabricated wafer is then singulated into individual filter components. The singulation can be done using high speed dicing saws or alternate methods such as punching or routing/milling. An advantage of this fabrication process is the ability to fully electrical test the components either before or after singulation.

III. Actual Devices

Example I

[0090] An X-ray photograph of an organic bandpass filter 500 in accordance with an embodiment of the present invention is provided in FIGS. 7 and 8. The filter 500 comprises

shorted hybrid CPW-stripline meander transmission line inductors 512, 514 formed close to each other on a first organic dielectric layer, which is a 50 μm thick layer of LCP, wherein the inductors 512, 514 are directly magnetically coupled to each other. Each inductor is connected to separate parallel plate capacitors 516, 518 by sandwiching the same dielectric sheet. An inter-resonator parallel plate coupling capacitor 524, is formed using two disconnected metal plates that sandwich the same organic dielectric sheet in such a manner that the each plate of the inter-resonator coupling capacitor electrode connects to separate inductors. In addition, a second organic dielectric layer and a third organic dielectric layer sandwich the first organic dielectric layer, and comprise a high frequency hydrocarbon material with a thickness of 30-40 mils, which are disposed so as to sandwich said first dielectric sheets there between.

[0091] The bandpass filter 500 further comprises an additional dielectric layer, in this case solder mask, provided on an outermost one of the shield electrodes to protect the outermost shield electrodes. The inductors 512, 514 did not provide the needed capacitance in the desired length, and therefore each are connected to a separate grounded/shunted parallel plate using the same first organic layer as the sandwiched dielectric, which then together form the resonator pairs 560, 562, as illustrated. In the illustrated device, parallel plate capacitors 526, 528 are utilized on either side of the first and last resonator elements at the input and output terminals of the device for impedance matching purposes. If greater density is desired multiple thin layers such as the first dielectric layer can be used to form multi (>2) plate capacitors.

[0092] The bandpass filter 500 further comprise at two external ground shield electrodes 534 respectively formed on different side surfaces of a laminated body comprising said first through three or more dielectric layers and connected to said shield electrodes. Additionally these provide the connection for the shorted inductors/ resonators and capacitors. Moreover, the presence of these external electrodes makes it a CPW/stripline topology, where the reference is on the same first dielectric layer provides the shielding internally, and also provides for the ground connectivity to the resonators/inductors and capacitors.

[0093] The bandpass filter further comprises an external input terminal electrode 564 and an external output terminal electrode 566 which are formed on one side surface of a laminated body comprising said first through three or more dielectric sheets. External side wall shield electrodes 534 (FIG. 7) are provided between said external input and output terminal electrodes on the side surfaces of the laminated body and external ground shield electrodes 548 are provided on opposing top and bottom surfaces of the laminated body and are electrically connected to the side wall shield electrodes 534.

[0094] The patterning of the external ground shields electrodes 548 on the top and bottom surfaces is required for leaving space for the signal input output as shown in FIGS. 7 and 8.

[0095] In the organic bandpass filter 500, the first step to making connection between devices is done by drilling through holes as small as 2 mils with pads as big as three times the size of the via through LCP and copper. Both sides of LCP copper laminate are then metalized via electroless. The copper on both sides of laminate is then electroplated, and the copper layer is printed and etched to define filter component.

[0096] The second and third organic dielectric layers are Rogers 4350 from Rogers Corporation with a generally larger thickness than the first organic dielectric layer, such as approximately 35 mils, with copper metal (for high power applications) on both sides of filter to a given thickness to encapsulate components. All metals are electroplate and etched and patterned on top and bottom of the device to leave space for signal input and output.

[0097] The side wall grounded shield electrodes 534 can be obtained by single or multiple connected drilled plated through holes and then connected via electroless or sputter seeded copper in through hole. Electroplate copper in through hole and on surface. Print and etch copper to form SMD connection. The copper electrodes may be electroless NiAu plate to prevent excess oxidation.

[0098] FIG. 9 shows model to hardware correlation for the organic bandpass filter 500 in FIGS. 7 and 8. The filter was measured using an HP 8720ES Vector Network Analyzer after performing a SOLT calibration. The measured data for the fabricated filter and simulated data is shown. As evident from FIG. 9, there is excellent correlation between measured data and simulated data. The organic bandpass filter 500 was fabricated using LCP for the first organic dielectric layer, and shows an insertion loss of only 1.88dB at 3 GHz and a 1dB bandwidth of 200 MHz. Such a filter would be suitable for IF frequency use in fixed wireless type receivers where the carriers frequency of the incoming signal is approximately 14 GHz and has to be down-converted to several lower frequency signals.

[0099] The organic bandpass filter 500 utilizes a CPW/stripline topology with only two metallization levels and all embedded passives in an organic substrate, which resulted in better performance than non-standardized multilayer (>5) ceramic processes, as seen in FIG. 9.

[00100] It is worth noting that while the Q of the capacitors for filter 500 was measured as high as 200 at 3 GHz using LCP, the Q for the inductor was kept at the required level of approximately 100 at 3 GHz. This was done to understand the advantages of using a material such as LCP without optimizing the design for the inductors. However, Qs exceeding 200 are also attainable for inductors on organic substrates. A resimulation for the filter circuit shown, but with Qs of 200 for the inductors, showed an insertion loss of 1.15dB when simulated. A filter with a loss of 1.15dB at the frequency and bandwidth can be alternatively achieved only by using the bulkier and costlier ceramic cavity and monoblock filters.

Example II

[00101] Another organic bandpass filter 600 in accordance with an embodiment of the present invention is shown in the picture of FIG. 10. The filter 600 comprises shorted hybrid CPW-microstrip, meander inductors 612, 614 formed close to each other on a first organic dielectric layer, which is a layer of LCP, directly magnetically coupled to each other. The term "shorted" refers to one end of each inductor connected to the large metallic area, which

in this case serves as the in-built shield 630 (also referred to as a coplanar ground ring). In addition, the filter 600 includes an inter-resonator parallel plate coupling capacitor electrode 624 with in-built shield 630 formed using two disconnected metal plates that sandwich the first organic dielectric layer in such a manner that the each plate of the inter-resonator coupling capacitor electrode connects to separate resonators. Yet further, the filter 600 includes a first shield electrode formed respectively on a second organic dielectric layer, which in this case is Rogers 4350 from Rogers Corporation, and which is disposed over the circuitry described above, so as to sandwich and substantially completely shield one surface of the filter.

[00102] The filter may further comprise a third organic dielectric sheet, if needed, provided on the outside of the shield electrode to protect the outermost shield electrode. In this filter, the inductors 612, 614 did not provide the needed capacitance in the desired length, and therefore each is connected to a separate grounded/shunted parallel plate (two plate) using the same first organic layer as the sandwiched dielectric, which then together form the resonator pairs. In addition, parallel plate/interdigital capacitors 626, 628 are utilized on either side of the first and last resonator elements at the input and output terminals of the device for impedance matching purposes. If greater density is desired, then multiple thin layers such as the first dielectric layer can be used to form multi (>2) plate capacitors. In addition, another dielectric layer such as lower temperature melt LCP compare to the higher melt temp LCP used as the first dielectric is laminated on the other side of the first substrate (not the same side as the second substrate), and then solder bump openings are made where ground and input output connections are required to connect the device to corresponding terminals on the board.

[00103] The CPW topology, where the reference is on the same first dielectric layer provides the shielding internally, provides for the ground connectivity to the resonators/inductors and capacitors. However in more noisy environments the external electrodes, such as those in Example I, could be added for added shielding.

[00104] In the second bandpass filter, the openings in the third substrate allow for the ground connection connected to the CPW ground and two other openings not connected to each other or the ground serving for input and output terminals.

[00105] The first step to making connection between devices is by drilling through holes (as small in diameters as the thickness of the dielectric used) through the first organic dielectric layer of LCP and copper. Then both sides of LCP copper laminate are metalized via electroless copper. Copper is then electroplated on both sides of laminate. The copper is then printed and etched to define filter component.

[00106] The second organic dielectric layer can be laminate LCP or another appropriate dielectric with generally larger thickness than the first organic dielectric layer with copper metal (for high power applications) plated on top of the filter to a given thickness of approximately 20-30 μm to encapsulate components. The third organic dielectric layer is laminate LCP or another appropriate dielectric with generally larger or smaller thickness than the first organic dielectric layer with copper plated in the openings to a given thickness to provide for solder landing pads. The openings in the third substrate are filled with screen solder paste and reflowed to form bumps.

[00107] FIG. 11 shows model to hardware correlation for the organic bandpass filter 600 in FIG. 10. In summary, the filter utilizes a CPW topology with only two metallization levels and all embedded passives in an organic substrate, which resulted in better performance than of non-standardized multilayer (>5) ceramic processes. As the adoption of lower loss materials, such as LCP, becomes more common, this design shows the feasibility of integrating very low loss filters for applications such as Bluetooth/WLAN in compact boards and packages.

[00108] The measured data for the filter 600 and simulated data is shown in FIG. 11. As seen there is excellent correlation between measured data and simulated data. The filter 600 has an insertion loss of only 2.22dB.

[00109] It is worth noting that while the Q of capacitors may be as high as 300 using LCP, the Q for the inductor was kept at the required level of approximately 130. The insertion loss was 0.6dB lower than the MLC filters with similar footprint. A resimulation for the filter circuit shown, but with Qs of 200 for the inductors, showed an insertion loss of 1.65dB when simulated. A filter with a loss of 1.65dB at the frequency and bandwidth desired of the Bluetooth/WLAN filter can be alternatively achieved only by using the bulkier and costlier ceramic cavity and monoblock filters.

Example III

[00110] Yet another organic bandpass filter 700 in accordance with an embodiment of the present invention is shown in the picture of FIG. 12. The organic bandpass filter 700 comprises shorted hybrid CPW-microstrip meander inductors formed close to each other on a first organic dielectric substrate, such as epoxy based Vialux by E.I. du Pont de Nemours and Company, directly magnetically coupled to each other. In addition, the third bandpass filter comprises an inter-resonator parallel plate coupling capacitor electrode 724, with ground ring, formed using two disconnected metal plates that sandwich the same organic dielectric sheet in such a manner that the each plate of the inter-resonator coupling capacitor electrode connects to separate resonators.

[00111] The transmission line inductors 712, 714 did not provide the needed capacitance in the desired length. Since the dielectric is lossy for the capacitor application, each is replaced by a separate discrete capacitor 702, such as a chip capacitor or ceramic capacitor with one terminal of one capacitor connected to one resonator and the other shorted to the in-built shielding electrode 730. The same can be done for the other capacitor 724 where one terminal is grounded, i.e., connected to a CPW ground electrode 730 and the other terminal is connected to the resonator section. In addition, a parallel plate/interdigital capacitors 726, 728 are utilized on either side of the first and last resonator elements at the input and output terminals of the device for impedance matching purposes. If greater density is desired multiple thin layers such as the first dielectric layer can be used to form multi (>2) plate capacitors.

[00112] The organic bandpass filter 700 may further comprise another monoclad second organic dielectric layer that is laminated on the one side of the first organic dielectric layer (opposite the side of the discrete capacitors). In addition, it may further comprise multiple plate through holes going through first and second organic dielectric layer connected to the in-built shielding electrode 730 and metal sheet of the monoclad dielectric. This may or may not be desired for cost saving purposes, though adding these vias makes it a true CPW/microstrip hybrid device. The CPW topology, where the reference is on the same first organic dielectric layer, provides the shielding internally, and also provides for the ground connectivity to the resonators/inductors and capacitors. However in more noisy environments the external through holes can be added for added shielding.

[00113] The organic bandpass filter 700 may further comprise a third organic dielectric layer on the same side as the discrete capacitors 702 providing for protection of the circuits and seal the device from moisture uptake and corrosion. This material could be the same as solder mask materials, which would be used by the board manufacturers to protect other circuits on the board. In addition, the bandpass filter 700 may further comprise a metallic lid or cap/electromagnetic shield which encloses the device on the top surface and prevents EMI interference and radiation effects from affecting the performance of the filter.

[00114] FIG. 13 shows model to hardware correlation for the organic bandpass filter 700 in FIG. 12. In particular, FIG. 13 shows a model to hardware correlation for the filter with all embedded components, except the two discrete capacitors. As shown, there is very good agreement between measured and predicted results. The measured filter has a center frequency = 1.9 GHz, a 1dB passband of 60 MHz, and a 3dB bandwidth of 120 MHz. The attenuation at 1.5 GHz is ~ 40dB, as desired. The insertion loss is approximately 3.8dB at 1.9 GHz, which is greater than the specification of 3dB for such applications. This is due to the use of center and matching capacitors with Qs of 40 in Vialux rather than the required Q of 60 needed to achieve a lesser loss of 3dB. This insertion loss can be lowered by using A-PPE™ or LCP™ from Rogers Corporation dielectric materials for the organic dielectric layer. Such a filter would be applicable in cellular phones as the intermediate RF filter or in cordless phones as the front-end RF filter.

[00115] As seen in FIG. 13, there is a discrepancy in the measured and predicted results beyond 2.5 GHz for S_{21}. This discrepancy is due to the coupling between the two discrete capacitors. The simulations were done for individual components and for optimizing the spacing between the inductors. The discrete capacitors were measured as individual components without any coupling between them. The tight spacing between the capacitors could have resulted in unwanted coupling effects which show up at frequencies greater than 2.5 GHz. After including a mutual coupling term between the two discrete capacitors, the results show better agreement with measurements.

[00116] Thus, the organic bandpass filter 700 utilizes a CPW topology with only two metallization levels and an epoxy based substrate along with discrete capacitors, which achieves the performance of non-standardized multilayer (>5) ceramic processes. Additionally, the MLC filters cannot be integrated with other components in the same layers of the ceramic package due to several reasons, a few of which include: firstly, because of the use of a filter-specific dielectric which is incompatible with other dielectrics; secondly, because of the specificity of certain attributes such as 100 μm thick aluminium conductor lines required to lower the attenuation present due to standard 5 μm lines used in ceramic processes. The design discussed in this section was fabricated using standard design rules pertinent to multilayer laminate boards and can be directly implemented on the board without the need for a separate surface mount device. Furthermore, the model to hardware correlation shows validity of the design tecchnique used.

IV. RF Transceivers

[00117] FIGs. 14 and 15 are illustrative of two respective approaches in which multi-band transceivers can be implemented according to an embodiment of the present invention. In particular FIG. 14 illustrates an exemplary multi-band receiver portion of a transceiver that uses multiple single-band paths, each of which may be selectable using switches. Referring to FIG. 14, two parallel paths 802 and 818 are provided for a multi-band receiver in which each path operates in a different frequency range (or band). In particular, path 802, which operates for a first frequency range, includes a single-band antenna 804 for receiving signals in the first frequency range, a bandpass filter 806, a balun / matching network 808, an RF

integrated circuit 810 that is operable with a first voltage controlled oscillator 812. The RF integrated circuit 810 may include a single-band low noise amplifier (LNA), a mixer, one or more intermediate frequency (IF) filters, and perhaps a frequency downconverter. After processing by the RF integrated circuit 810, a common baseband signal 814 is received by baseband processor 816, which may include components such as flash RAM, an analog-to-digital converter (or a digital-to-analog converter in the case of a RF transmitter), and power management capabilities. Similarly, path 818, which operates for a second frequency range, includes a single-band antenna 820 for receiving signals in the second frequency range, a bandpass filter 822, a balun / matching network 824, an RF integrated circuit 826 that is operable with a first voltage controlled oscillator 828. The RF integrated circuit may include a single-band low noise amplifier (LNA), a mixer, one or more IF filters, and a frequency downconverter. After processing by the RF integrated circuit 826, a common baseband signal 814 is received by baseband processor 816.

[00118] FIG. 15 illustrates an exemplary multi-band receiver portion of a multi-band transceiver that uses only a single multi-band path 902. The multi-band transceiver may utilize narrow-band devices operational at specific multiple frequency bands and/or wide-band devices, with the range of frequencies covering multiple frequency bands. Referring to FIG. 15, path 902, which may operate for two or more frequency ranges, includes a multi-band antenna 904 for receiving signals in various frequency ranges, a multi-band bandpass filter 906, a multi-band balun / matching network 908, an RF integrated circuit 910 that is operable with a multi-band voltage controlled oscillator 912. The RF integrated circuit 910 may include a multi-band low noise amplifier (LNA), mixer, and frequency downconverter. After processing by the RF integrated circuit 910, a common baseband signal 914 is received by baseband processor 916, which may include components such as flash RAM, an analog-to-digital converter (or a digital-to-analog converter in the case of a RF transmitter), and power management capabilities.

[00119] Note that FIGs. 14 and 15 are exemplary in nature only and that many variations would be known to one of ordinary skill in the art. For example, a combination of the approaches shown in FIGs. 14 and 15 are possible, where there may be one single band

path and another multi-band path. In addition, with respect to FIGs. 14 and 15, there may also be multiple filters along the signal paths and more than one mixer present. Likewise, there may be additional intermediate frequency stages utilized, which may not be shown in FIGs. 14 and 15. Further, the above approaches are applicable to the multi-band transmitter portion of the transceiver and would be readily recognized by one of ordinary skill in the art. For example, a digital-to-analog converter may be used to generate a signal that is filtered, amplified, upconverted by a frequency upconverter, and additionally amplified by a high power amplifier before transmission.

[00120] With respect to the choice between the exemplary approaches illustrated in FIGs. 14 and 15, or a combination thereof, several design considerations may be evaluated. In particular, frequency bands may be designated as either concurrent or non-concurrent based on the functionality required. In addition, multi-band devices may be designed for paths that are specified to be concurrent by using chip-package co-design methodologies. Many modifications to the above embodiments would be known to one of ordinary skill in the art.

Voltage Controlled Oscillators

[00121] High performance voltage controlled oscillators (VCOs) as shown in FIG. 14 may be utilized for the generation and regulation of carrier waves in an RF transceiver. The phase noise of an oscillator in an RF transceiver may determine the noise floor and interference issues. More particularly, the phase noise of the oscillator may degrade the receiver selectivity due to spreading of the transmitted signal and degrade the receiver sensitivity or receiver noise floor. Further, a high VCO phase noise may cause spurious emissions from a communications system. Therefore, it may be preferable to control certain specifications of the oscillator including reducing the phase noise.

[00122] The phase noise figure of an oscillator is inversely proportional to the quality factor (Q) of the oscillator's resonator and the power consumption of the oscillator. Because system power requirements oftentimes specify the power consumption of the VCO, it is not always possible nor desirable to increase the power consumption of the oscillator in order to

reduce the phase noise. However, the Q of the resonator in the oscillator may be increased according to an embodiment of the present invention, thereby reducing the phase noise of the VCO. In particular, embodiments of the present invention may use high-Q passive components fabricated on organic substrates for the VCO that result in integrated devices with a low phase noise.

[00123] FIG. 16A illustrates a circuit diagram of a Colpitt's oscillator that can be implemented using high-Q passive components fabricated on organic substrates to achieve a high-performance oscillator according to an exemplary embodiment of the present invention. The Colpitt's oscillator in FIG. 16A was designed to operate at 2.2 GHz. Referring to FIG. 16A, the oscillator is packaged with a BJT 1002 (bipolar junction transistor) and high-Q inductors and capacitors fabricated on an organic substrate such as LCP (liquid crystalline polymer). The BJT 1002 may be, for example, a discrete BJT HBFP-0420 (SOT-343 packaging) from Agilent. The output of the BJT 1002 is matched to 50Ω load (RL 1008) by using a capacitor Cmatch 1006. The output match increases the output power of the oscillator, which helps improve the phase noise performance of the oscillator. The frequency of oscillation can be determined by the parallel combination of the inductor L 1012 and capacitors C1 1014 and C2 1016. According to an embodiment of the present invention, at least a portion of the passive components in the oscillator circuit may be fabricated on an LCP-based substrate. Alternatively, in other embodiments, some of the passive components, including the resistors Rb 1004 and Re 1005 and capacitor Cb 1003, may be fabricated as discrete components such as surface mount components.

[00124] The layout for the passive networks shown in FIG. 16A was designed to achieve unloaded Qs of approximately 100 for the passive components in order to obtain near minimum phase noise performance for the oscillator. Increase in the unloaded Q of the resonant tank formed by inductor L 1012 and capacitors 1014 and 1016 beyond a certain point (e.g., 300) may have a diminishing effect on the phase noise performance of the oscillator. Hence, the use of organic substrates such as LCP as shown in FIG. 16B or polyphenyl ether may be used since they may provide Qs of over 100 for capacitors. In order to make the designs more compact, a two-layer cross-section was utilized for the substrate as

shown in FIG. 16B. According to FIG. 16B, the layout includes metal layers 1050, 1052, and 1054. Metal layers 1050 and 1052 may be approximately 9μm thick while metal layer 1054 may be approximately 5μm thick. In addition, the layout includes LCP and bondply layers 1056 and 1058 along with hydrocarbon layer 1060. The LCP and bondply layers 1056 and 1058 may be comprise LCP that is approximately 25μm thick. The hydrocarbon layer 1060 that may be approximately 32 mils thick. It will be appreciated by one of ordinary skill in the art that the cross-section in FIG. 16B is for illustrative purposes only. Many other variations are possible, including varying the thickness of the metal layers and organic layers. In addition, the numbers of metal layers and organic layers may change depending on the number of components to be included and the specification of the components. Further, the hydrocarbon layer 1060 may be a PCB (printed circuit board) or even replaced by another material that provides for sufficient rigidity.

[00125] A layout for the circuit diagram shown in FIG. 16A is shown in FIG. 16C. The layout shown in FIG. 16C utilized a CPW (coplanar waveguide) topology where the ground is coplanar for all the devices. The discrete components used for biasing and decoupling (Rb, Re, and C) are also shown in FIG. 16C. In this particular case, Rb was 22KΩ, Re was 100Ω, and decoupling capacitor C (not shown in FIG. 16A) was 1000pF. The layout shown in FIG. 16C corresponds to metal layer 1050 in FIG. 16B. FIG. 16D shows a layout for the metal layer 1052 in FIG. 16B. The layout in FIG. 16D includes the bottom metal plates (shown in the gray portion) corresponding to the top metal plates of the parallel plate capacitors in FIG. 16C.

[00126] It will be noted however that the layout corresponding to metal layer 1052 is not shown, but will be understood to contain other components, including the corresponding plates of the capacitors shown in FIG. 16C. One of ordinary skill would readily recognize that alternative topologies besides CPW shown in FIG. 16C are possible, including microstrip, stripline, or a combination of the foregoing.

[00127] The oscillator described above was simulated in Agilent's ADS (advanced design system) after including all the parasitics of the package as well the embedded passive

components and the active device (e.g., the BJT). The biasing resistors (Rb and Re) were adjusted to provide a current of approximately 4 mA for which the BJT parameters are optimized. The total power dissipation in the device was approximately 10.8mW. The output power delivered to the load was approximately -6dBm. The waveform from that simulation is shown in FIG. 17 and indicated that there was no distortion in the sine wave nature of the output power. The output power decreased significantly as the load value was changed or the frequency was varied, which indicated a narrow band of frequency matching. This was due to the matching element, however, which was limited to a single capacitor Cmatch 1006 for compactness. Should a wider bandwidth of frequency matching be needed, the matching circuit could be modified to be an "L" or "PI" network to increase the bandwidth.

[00128] The oscillator was fabricated according to the layouts shown in FIGs. 16B and 16C. The output power of the fabricated oscillator was then measured using Hewlett Packard's 4407b series Spectrum Analyzer. As shown in FIG. 18, the frequency of oscillations was maintained at 2.25 GHz with a measured output power of approximately -6dBm. When the DC supply voltage was varied from 2.7V to 4.0V, the frequency of oscillation changed from 3.25 GHz to 3.18 GHz with a measured output power of +3dBm.

[00129] As an aside, the quality factor (Q) of the resonant tank circuit on the LCP substrate may be sufficiently high—perhaps in the range of 120-130. The sensitivity of an oscillator to the changes in the Q of the passive components can be analyzed as follows: The phase noise of -80dBc/Hz is measured with a capacitor Q of approximately 300 and the inductor Q of around 100. So the equivalent Q of the resonant tank circuit is close to the Q of the inductor. When a high loss element such as a varactor diode (with Q of approximately 5-10 at 2 GHz) is added to the tank circuit the effective Q capacitive network becomes approximately 60. This Q is then raised to a higher value due to the high Q inductor. When the resonant circuit is replaced by a crystal with a Q of 10000 in series with a varactor diode of Q approximately 5-10, the change in the phase noise of the oscillator was trivial when compared to the obtained phase noise on the LCP substrate. This calculation rationalizes the capacitor Q of 300 to be sufficient for a high performing oscillator.

[00130] Oscillator designs similar to those shown in FIGs. 16B and 16C can implemented using other organic substrates besides LCP. For instance, epoxy-based substrates such as FR-4 epoxy can be utilized. FIGs. 19 and 20 show the measured performance for a 3.3 GHz and a 5.2 GHz oscillator, respectively, that were fabricated using the epoxy substrate. While fabricated oscillators utilizing LCP-based substrates generally have lower phase noise figures, the 5.2GHz oscillator fabricated using the epoxy substrate still meets the phase noise figure specifications of the IEEE 802.11a protocol.

[00131] In addition to the Colpitt's oscillator discussed above, other oscillators may be implemented in accordance with embodiments of the present invention. For example, FIG. 21 shows a schematic diagram of a Hartley's oscillator. A Hartley's oscillator includes two inductors L1 1102 and L2 1104 and a capacitor C 1106 that provides amplitude control, frequency selection, and feedback. For simplicity, the bias and decoupling circuitry are not shown in FIG. 21. In FIG. 21, the inductors L1 1102, L2 1104, and capacitor C 1106 provide positive feedback from the collector of the transistor 1108 to the base. The inductors L1 1102 and L2 1104 and the capacitor C 1106 are utilized to provided a feedback network such that the circuit becomes unstable and oscillates. The output of the oscillator may be input into a buffer amplifier that isolates the circuit as well as matches it to the load. Some or all of passive components shown in 1110 may be fabricated on an organic substrate such as LCP according to an embodiment of the invention. Another alternative oscillator that may be implemented according to an embodiment of the present invention is a cross-coupled oscillator as shown in FIG. 22. In FIG. 22, only one inductor is shown, but it is possible to use two inductors to maintain symmetry of the layout. The passive components shown in 1150 may be fabricated on an organic substrate such as LCP according to an embodiment of the present invention.

[00132] FIG. 23A illustrates another exemplary oscillator designed for 1.8 GHz that may be implemented according to an embodiment of the present invention. The active device 1160 in FIG. 23A may be a surface mountable BJT. FIG. 23B illustrates an exemplary stackup for the oscillator shown in FIG. 23A. Referring to FIG. 23B, six metal layers are shown, which include M1 1160, M2 1162, M3 1164, M4 1166, M5 1168, and

microstrip ground 1170. In addition, organic layers 1161, 1163, 1165, 1167, and 1169 are shown. Organic layers 1161, 1165, and 1169 may comprise LCP. Organic layers 1163 and 1167 may be core layers with a thickness of approximately 12 mils and a dielectric constant of approximately 3.35. The passive components shown in FIG. 23A may be formed on one or more of metal layers M1 1160, M2 1162, M3 1164, M4 1166, and M5 1168. Micro-vias 1172 may be provided for connecting the metal layers and thruhole 1173 provides for connections to the microstrip ground.

[00133] FIGs. 24A, 24B, and 25 show the measured characteristics of the oscillator shown in FIGs. 23A and 23B. According to FIG. 24A, the center frequency measurement corresponds to 1.8 GHz. FIG. 24B shows that the harmonic rejection is greater than 25dB. FIG. 25 shows the phase noise measurements obtained from an E 4407B spectrum analyzer.

[00134] FIG. 26 shows a comparison of VCOs fabricated with various technologies. Referring to FIG. 26, the VCOs fabricated with LCP according to embodiments of the present invention, which include the oscillator shown in FIGs. 23A and 23B (see 1190), were among the best performers in at least size and power consumption.

Multi-band Voltage Controlled Oscillators

[00135] As shown in FIG. 14, multi-band transceivers can use a single oscillator for each frequency band of interest such as VCOs 812 and 828. As shown in FIG. 14, each receiver for the a frequency band in interest may have a separate signal path from the antenna to the baseband processor (see e.g., signal paths 802 and 818). However, because the RF / analog blocks in a transceiver may occupy a major portion of the system, the multi-band transceiver with multiple single band paths as shown in FIG. 14 may be less efficient in size and power consumption compared to the multi-band transceiver with only a single multi-band path as shown in FIG. 15.

[00136] As discussed previously with regard to FIG. 15, using a single concurrent, multi-band VCO 912 instead of individual oscillators for the frequency bands of interest may reduce board design time and the size of a multi-band transceiver when compared to the one

in FIG. 14. In FIG. 15, the individual oscillators have been replaced with a single concurrent, multi-band VCO 912 until the first down conversion stage after which individual intermediate frequency (IF) signals (e.g., baseband signal 914) are processed by the baseband processor 916.

[00137] Concurrent multi-band VCOs, including those shown in FIG. 15, can also be implemented by fabricating passive components on organic substrates as described above. These passive components include high-Q passive components found in multi-resonant configurations, narrow band filters, and matching networks. Active components such as the discrete BJT and components for biasing the BJT are not necessarily embedded in the organic substrate.

[00138] In a simple form, the concurrent, multi-band VCO can generate signals at two or more different frequencies by using an oscillator with a feedback network satisfying the Barkhausen/Nyquist criterion at two or more different frequencies. According to a preferred embodiment, such a feedback network can have dual-band characteristic by making use of the dual network properties of such a passive network at different frequencies. With respect to the passive network, an inductor at one frequency may act more like a capacitor at a different frequency, and vice versa. For example, the capacitive feedback of the Colpitt's oscillator shown in FIG. 16A at 2.5 GHz is transformed into inductive feedback at 5.2 GHz. This may allow the same passive network to be reused in an oscillator in generating two signals at different frequencies.

[00139] Aspects of such an approach described above may include one or more of a) simultaneous optimization of space and power requirements to achieve desired phase noise performance, b) reduced power consumption by using the power consumed for a single oscillator to generate two unrelated distinct frequencies without the use of fractional multipliers, c) lower phase noise reducing the loop-bandwidth and hence lock-in time of PLLs (phase-locked loops), d) lower costs by using customizable embedded bandpass filters, and e) high Q passive components in organic packages.

[00140] As an example, a multiple-signal generator circuit of a concurrent, multi-band VCO is shown in FIG. 27. The active device 1200 may be Agilent's HBFP 0420 (SOT-343 package) surface-mount BJT with a gain-bandwidth product (f_t) of 18 GHz at 4mA and a forward emission coefficient (NF) of 1.3dB at 2.5GHz and 1.9dB at 5 GHz with an available gain of 14dB. With such feedback-type oscillators, it may be necessary to control the resonance of the passive components forming the feedback network since they determine the feedback factor, which may control the RF output power, phase noise, and figure of merit (FOM). As shown in FIG. 27, at 2.45 GHz, the series resonators (C1 1201, L1 1202 and C2 1203, L2 1204) provide capacitive reactance (see chart 1205) whereas the parallel resonator at the collector of the BJT (Cc 1206 and Lc 1207) provides inductive reactance (see chart 1208). Thus, at 2.45 GHz, the circuit in FIG. 27 functions as a Colpitt's oscillator with capacitive feedback from the collector to the emitter (similar to FIG. 16A). At a higher frequency such as 5.2 GHz, the series resonators (C1 1201, L1 1202 and C2 1203, L2 1204) provide inductive reactance (see chart 1205) whereas the parallel resonator at the collector of the BJT (Cc 1206 and Lc 1207) provides capacitive reactance (see chart 1208). Thus, at 5.2 GHz, the circuit functions as Hartley's oscillator (see FIG. 21) due to resonance and anti-resonance of the series (C1 1201, L1 1202 and C2 1202, L2 1204) and parallel resonators (Cc 1206 and Lc 1207), respectively. While implementing the series and parallel resonators, some of the components may be explicitly found in the corresponding layouts, but it is also possible that one or more of C1 1201, L1 1202 and C2 1202, L2 1204, Cc 1206 and Lc 1207 may be represented as parasitics of another component.

[00141] The C1 1201, L1 1202 combination provides an equivalent capacitance of approximately 0.85 pF at 2.45 GHz and the C2 1203, L2 1204 combination provides an equivalent capacitance of approximately 2.3 pF at 2.45GHz. Likewise, the parallel resonator (Cc 1206 and Lc 1207) at the collector of the BJT 1200 provides an inductance of approximately 3.9nH at 2.5 GHz and a capacitance of 0.05pF at approximately 5.2 GHz. When designing the series and parallel resonators, the reactance may be designed to be substantially constant at the frequency of interest. The constant reactance enables the oscillator design to be narrow-band and the specifications for the subsequent filter 1210 to be relaxed. The large signal loop-gain was determined using Agilent's Advanced Design

System (ADS) simulator. The circuit was biased at 4 mA from a 2.7 V DC supply. The loop-gain was adjusted to be 1.4 at 2.4 GHz and 1.5 at 5.2 GHz.

[00142] For a high f_t (e.g., >30 GHz) transistor, the trans-conductance (G_m) remains almost constant at the concerned design frequencies. Hence the 2.4 GHz and 5.2 GHz signals have similar characteristics and amplitude. In such a multi-signal, non-linear circuit, issues such as inter-modulation distortion and harmonic distortion may be prevalent and may affect the output signal purity. For example the first harmonic of the 2.45 GHz signal, which may occur at 4.9 GHz, must be significantly attenuated (e.g., perhaps >40 dB) to avoid distortion at the 5.2 GHz output. Thus, a traditional T or Pi-type matching network cannot be used in such a circuit with multi-band characteristics. If power consumption is a concern, purely passive matching may be used over active buffers. For a concurrent, multi-signal VCO, narrow band (e.g., 100 MHz), low loss, high out-of-band attenuation, and multiple transmission zeros type filters may be desirable. The design of the filters involves sufficient attenuation of the inter-modulation products and less than 0.5 dB ripple in the pass band. In addition, each filter should provide at least a transmission zero in the pass-band of the other designed filter.

[00143] The multi-band filter 1210 following the core circuit may be inductively-coupled dual resonator-type as shown in FIG. 28 according to an illustrative embodiment of the present invention. The filters in FIG. 28 are Chebychev type with transmission zeros providing sufficient isolation between bands. Each filter is designed to match the core circuit at its pass-band frequency while providing very low insertion loss. The filters provide a rejection greater than 40 dB at the pass band of the other filter. An additional zero is provided at 8 GHz which is the intermodulation product of the two frequencies (2.4 and 5.5 GHz). Such a response is desirable to meet the isolation requirements from other modules, such as the antenna, power amplifiers, in a multi-band environment.

[00144] FIG. 29 shows the broad-band simulated response of the dual-band filter 1210 for 50Ω input and output impedances. FIG. 30 shows the transient simulation of the complete 2.53 GHz and 5.2 GHz concurrent multi-band oscillator shown in FIGs. 27 and 28.

[00145] According to another embodiment, a concurrent signal generator for producing signals at 900MHz and 1900MHz will be described. Fig. 31A shows the schematic of a base-type concurrent oscillator that uses multiple resonance of passive components. The bias network is not shown for simplicity. FIG. 31A uses the same active device as used for the 2.4/5.2 GHz oscillator (i.e., Agilent's HBFP 0420 (SOT-343 package) surface-mount BJT) described with respect to FIG. 27.

[00146] FIG. 31B illustrates an exemplary stackup for the base-type concurrent oscillator of FIG. 31A. The stackup includes a 1 mil thick LCP layer 1350 that is laminated on a 32 mil lower melt adhesive (core) layer 1352. FIG. 31B also shows three metal layers, M1 1354, M2 1356, and M3 1358, which may be copper. The LCP layer 1350 may be an LCP with a dielectric constant of 2.95 and a loss tangent of 0.002. The adhesive layer 1352 may have a loss tangent of 0.0035 with a dielectric constant of 3.38. Further, high density inter-metal micro-vias 1360, perhaps with diameters < 100 μm, may be formed with high yield. The micro-vias 1360 enable the passive components to be closely packed together. Additionally, through-holes 1362 may be employed for connection with the microstrip ground metal layer 1358. The surface mount device 1364 in FIG. 31B can be Agilent's HBFP 0420 (SOT-343 package) surface-mount BJT. FIG. 31C shows a top view of a layout for the oscillator of FIG. 31A. Note that not all of the components $L_1L_2C_1C_2$ network 1302 are implemented as separate components in the layout of FIG. 31C. For example, referring to FIG. 31C, inductor L2 is implemented in two stages, and the parasitic capacitance of L2 is C2.

[00147] The circuit in FIG. 31A may be biased at 10mA from a -1V and 2V supply. The base-type oscillator may operate in a multiple reflection mode. Reflections ($S_{11} > 1$) may occur at the emitter and collector of the BJT due to negative resistance. The frequency at which the reflections occur may be controlled by the value of base inductance ($L_1L_2C_1C_2$ network 1302). The $L_1L_2C_1C_2$ network 1302 may provide an inductance of 14nH at 2 GHz and 20nH at 900 MHz. The loop-gain can be determined using large signal S-parameters as shown in FIG. 32. The loop gain criterion ($1\angle 0°$) is satisfied at 890 MHz and 1.92 GHz. The phase of the large signal loop gain is zero at 2.3 GHz, but the magnitude of loop-gain is

less than 1 so oscillations are avoided at 2.3 GHz. The filter of the 900 MHz and 1.9 GHz concurrent signal generator is similar to the one shown in FIG. 28, but without the mutual inductive coupling (M12 and M34). The simulated response of such a filter is shown in FIG. 33. The concurrent multi-band oscillator in FIG. 31A was simulated in the time domain to provide output signal at 892.8 MHz and 1.92 GHz. FIG. 34 shows the transient response of concurrent multi-band oscillator of FIG. 28A.

Low Noise Amplifiers

[00148] Several aspects may be evaluated in the design of a low noise amplifier (LNA) for an RF application, including reasonable gain, a good input impedance match, high linearity, and the lowest possible noise figure (NF). If the LNA is to be used in a portable device, such as a cell phone, the need for low power consumption also becomes important. The NF of an LNA is a measure of the amount of noise added by the circuit to the incoming signal, and is defined as the ratio of Signal-to-Noise Ratio (SNR) at the input of the device to the SNR at the output as shown below:

$$NF = \frac{(SNR)_{in}}{(SNR)_{out}}$$

[00149] In a simplified form, the LNA includes an active device with passive matching networks at its input and output. These matching networks provide impedance transformation for minimum NF at the input and maximum power gain at the output. The use of high-Q embedded passives in organic substrates for implementing these matching networks results in lower NF and higher gain for the LNAs. Additionally, like the VCOs described above, the passives can also be used for implementing multi-frequency resonant circuits, thereby making the LNAs operational at multiple frequencies.

[00150] FIG. 35 shows a circuit diagram of an exemplary low noise amplifier and a corresponding photograph of the fabricated device. In particular, FIG. 35 illustrates an LNA circuit with an active device (e.g., a bipolar junction transistor) and the matching networks that will be embedded in an organic substrate. FIG. 35 also shows a photograph of the

fabricated LNA with the transistor and bias circuit soldered on. FIG. 36 shows the measured gain and input match for the LNA of FIG. 35.

[00151] One of ordinary skill in the art would recognize that many other embodiments of the LNA are also possible. For instance, instead of an explicit matching network at the input, the capacitance looking into the base/gate of the transistor may be made part of the matching network. Depending on the size and performance requirements, some of the passives can be placed on-chip, leading to a design-segmentation. As indicated previously, with the design of the LNA, the passive Q-factor affects the NF and gain of the LNA.

Implementing Circuits in Low Form Factor Modules

[00152] With the drive towards embedding wireless functionality in consumer devices (flat-panel displays, PDAs, etc.), implementation of the above multi-band multi-mode RF transceivers in low-profile ultra thin modules may also be desirable. According to an embodiment of the present invention, the topology and circuits discussed previously may be implemented in low-profile modules (e.g., a maximum thickness of 1.1mm).

[00153] FIG. 37 is illustrative of three embodiments of low form factor modules according to embodiments of the present invention. The term "substrate" in each of the above diagrams consists of a multilayer stackup, including Hydrocarbons like Rogers 4350B, single or multiple layers of LCP, single or multiple layers of high-K materials or any combination of the above. Several different types of ICs may be supported by the substrate, including wire-bonded IC die, flip-chip IC die, and packaged IC (e.g., a surface mount). In addition, discrete components may be supported by the substrate, including resistors. An overmold may also be used for encapsulating the ICs and discrete components as shown in FIG. 37. According to alternative embodiments of the present invention, an even smaller version of the low form factor may be obtained by embedding the IC and the discrete component within the substrate. In this alternative embodiment, an overmold may not be needed, thereby further reducing the form factor.

[00154] FIGs. 38A – 38F provide exemplary multi-layer stackups according to an embodiment of the present invention. The embedded passives can be of microstrip, stripline, co-planar waveguide (CPW) topology, or a hybrid thereof. Depending on size and performance requirements, the devices can be designed such that they are optimized for high performance or for small size.

[00155] Specifically, FIG. 38A discloses six metal layers (metal being denoted by the dark lines). Both the top and bottom metal layers may function as ground shields. The metal layers on each surface of the LCP layer may contain inductors and parallel plate capacitors. The metal layers on the laminate layers adjacent the prepreg layers are optional and may contain additional components if desired, such as for added density. In accordance with an embodiment of the present invention, the inductors are preferably formed on the LCP layers and the capacitors are formed on either the LCP layer or the Laminate layers. FIG. 38B is an extension of FIG. 38A, in which an additional LCP layer with metal layers on opposite sides thereof has been added. More components, including parallel plate capacitors and inductors can be placed on this additional LCP layer. This additional LCP layer is separated from the other LCP layer by an additional prepreg layer, though the layer may be electrically connected by microvias.

[00156] FIG. 38C illustrates the layers shown in FIG. 38B, except that high K layers have been substituted as for the laminate layers. When compared to the laminate layers, the high K layers increase the separation and increase the capacitance for capacitor components that may be placed on the high K layers. Generally, the non-critical, lower-performing components would be placed on the high K layers. FIG. 38D illustrates three LCP layers that are separated by two prepreg layers. An aspect of the stackup shown in FIG. 38D compared to the previous stickups in FIGS. 17A-C is that this is an extremely thin stackup which may be on the order of a 0.3mm thick substrate. Four metal layers are shown in FIG. 38D, which may contain components such as capacitors and inductors, providing for excellent density. FIG. 38D may be known as a high performance substrate. One of ordinary skill would recognize that the stackup in FIG. 38D is not limited to 3 LCP layers, but could contain

additional layers, including another LCP layer that is separated from the other LCP layer by a prepreg layer.

[00157] FIG. 38E illustrates an inner high K layer that is positioned between two laminate, LCP, or high K layers. In particular, the high K layer is separated from each laminate, LCP, or high K layer by prepreg layers on opposite sides of the high K layer. The high K layer and each of the laminate, LCP, or high K layers may contain metal layers on each surface to provide for integrated components such as inductor and capacitors. The stackup shown in FIG. 38E may be suitable for a baluns which may have a more relaxed performance specification. In such a case, the high K middle layer does not have to be fabricated with such stringent requirements (e.g., thickness), and is appropriate for use as an inner layer. FIG. 38F discloses a stackup similar to that shown in FIG. 38A, with the addition of exterior RCF (resin coated foil) layers. RCF (resin coated foil) allows for the same densities for lines and spacing and microvias but at a lower cost compared to high K and LCP. In addition, in FIG. 38F, the laminate layers could also be substituted with high K or LCP layers.

[00158] When working with hybrid CPW-stripline topology, the higher performance components will typically need to be further away from ground while the lower performance components may be closer to ground. For example, in FIG. 38B, inductors may be placed in the inner LCP layers while parallel plate capacitors may be placed on the laminate layers. However, parallel plate capacitors could also be placed on the inner LCP layers as well.

[00159] Accordingly, embodiments of the VCO and LNAs described above can be implemented in accordance with FIGs. 37 and 38A-F.

[00160] Many modifications and other embodiments of the inventions set forth herein will come to mind to one skilled in the art to which these inventions pertain having the benefit of the teachings presented in the foregoing descriptions and the associated drawings. Therefore, it is to be understood that the inventions are not to be limited to the specific

embodiments disclosed and that modifications and other embodiments are intended to be included within the scope of the appended claims. Although specific terms are employed herein, they are used in a generic and descriptive sense only and not for purposes of limitation.

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THAT WHICH IS CLAIMED:

1. A multi-band RF device operable at a first frequency and a second frequency different from the first frequency, comprising:

an active device;

a first passive network in communication with the active device;

a second passive network in communication with the active device; and

an organic-based substrate having at least two metal layers, wherein the two metal layers are patterned to form at least a portion of the first passive network and the second passive network, wherein impedances of the first and second passive networks are different at the first frequency than the second frequency.

2. The multi-band RF device of Claim 1, wherein the first and second passive networks comprise resonant circuits, and wherein the impedances of the first and second networks comprise reactance.

3. The multi-band RF device of Claim 2, wherein the active device is a bipolar junction transistor, wherein the multi-band RF device is an oscillator, and wherein a first oscillation signal at the first frequency and a second oscillation signal at the second frequency are simultaneously generated.

4. The multi-band RF device of Claim 1, wherein the first passive network comprises a first matching network at an input of the active device and wherein the second passive network comprises a second matching network at an output of the active device.

5. The multi-band RF device of Claim 4, wherein the active device is a bipolar junction transistor and wherein the multi-band device is a low noise amplifier operable for providing power gain at the first frequency and the second frequency.

6. An RF multi-band oscillator for simultaneously generating oscillation signals at a first frequency and a second frequency for a multi-band transceiver, comprising:

an organic layer having a top surface and a bottom surface;

a first metal layer opposite the top surface;

a second metal layer opposite the bottom surface, wherein the first metal layer and the second metal layer are patterned to form a first resonator and a second resonator, wherein a reactance of the first resonator at the first frequency differs from a reactance at the second frequency and wherein a reactance of the second resonator at the first frequency differs from a reactance at the second frequency; and

an active device in communication with the first resonator and the second resonator to form a feedback network, thereby simultaneously generating oscillation signals at the first frequency and the second frequency.

7. The multi-band oscillator of Claim 6, wherein the organic layer comprises liquid crystalline polymer.

8. The multi-band oscillator of Claim 6, wherein the reactance of each of the first resonator and second resonator is substantially constant at the first frequency and the second frequency.

9. The multi-band oscillator of Claim 8, wherein the reactance of at least one of the first resonator and second resonator at the first frequency is inversely proportional to the reactance at the second frequency.

10. The multi-band oscillator of Claim 9, wherein the first and second resonators comprise at least one inductor and at least one capacitor.

11. The multi-band oscillator of Claim 10, wherein the first resonator is a parallel resonator and the second resonator is a series resonator.

12. The multi-band oscillator of Claim 8, wherein the active device is a transistor.

13. The multi-band oscillator of Claim 12, wherein the transistor is a bipolar junction transistor.

14. The multi-band oscillator of Claim 6, further comprising a filter formed on at least one of the first patterned metal layer and the second patterned metal layer, wherein the filter separates the generated oscillation signals into distinct oscillation signals at the first frequency and the second frequency.

15. The multi-band oscillator of Claim 14, wherein the filter is an inductively-coupled dual resonator type filter.

16. A multi-band low noise amplifier for use in an RF application, comprising:

an active device;

a first matching network in communication with the active device, wherein an impedance of the first matching network at a first frequency is different than the impedance of the first matching network at a second frequency;

a second matching network in communication with the active device, wherein an impedance of the second matching network at the first frequency is different than the impedance of the second matching network at the second frequency; and

a multi-layer organic-based substrate having at least one metal layer, wherein the first matching network and the second matching are formed on the at least one metal layer and wherein the active device is mounted on the multi-layer organic substrate, thereby allowing the an output of the multi-band low noise amplifier to have desired power gains at the first frequency and the second frequency based at least in part on each of the first and second matching networks having the different reactance at the first frequency and the second frequency.

17. The multi-band amplifier of Claim 16, wherein the active device is a bipolar junction transistor.

18. The multi-band amplifier of Claim 16, wherein the multi-layer organic-based substrate comprises at least one of hydrocarbon and liquid crystalline polymer.

19. The multi-band amplifier of Claim 18, wherein the first matching network is positioned at an input of the multi-band amplifier and the second matching network is positioned at an output of the multi-band amplifier.

20. The multi-band amplifier of Claim 19, wherein the first matching network minimizes the noise figure for the multi-band amplifier at the input at both the first frequency and the second frequency.

21. The multi-band amplifier of Claim 20, wherein the second matching network maximizes the desired power gains for the multi-band amplifier at the output at both the first frequency and the second frequency.

22. An oscillator for use in an RF transceiver, comprising:

a first organic layer with a top surface and a bottom surface opposite the top surface;

a first conductive layer positioned on the top surface of the first organic layer;

a second conductive layer positioned on the bottom surface of the first organic layer;

a second organic layer positioned opposite the second conductive layer;

a plurality of passive devices patterned on at least one of the first conductive layer and the second conductive layer; and

at least one discrete active device positioned on the first conductive layer and in communication with at least a portion the plurality of passive devices, wherein a feedback network for the active device is created such the discrete active device becomes unstable and generates at least one signal at a particular frequency.

23. The oscillator of Claim 22, wherein the first organic layer and the second organic layer comprise liquid crystalline polymer.

24. The oscillator of Claim 23, wherein the first organic layer comprise polyphenyl ether.

25. The oscillator of Claim 23, wherein the discrete active device a transistor.

26. The oscillator of Claim 25, wherein the transistor is a field effect transistor.

27. The oscillator of Claim 25, wherein the transistor is a bipolar junction transistor.

28. The oscillator of Claim 25, wherein at least a portion of the plurality of passive devices comprise inductors and capacitors.

29. The oscillator of Claim 28, wherein the portion of the plurality of passive devices comprise resistors.

30. The oscillator of Claim 29, wherein the feedback network forms a resonant tank.

31. The oscillator of Claim 25, wherein the first conductive layer comprises a coplanar ground.

32. The oscillator of Claim 25, wherein at least a portion of the plurality of passive devices comprise a network for matching to a load.

Abstract

The present invention allows for the use of chip-package co-design of RF transceivers and their components by using discrete active devices in conjunction with passive components. Two particular components are described, including voltage controlled oscillators (VCOs) and low noise amplifiers (LNAs). The high quality passive components for use in the VCOs and LNAs may be obtained by the use of embedded passives in organic substrates. Further, the embedded passives may have multi-band characteristics, thereby allowing multi-band VCOs and LNAs to be implemented with fewer components. In situations where size is a concern, the active devices and passive components utilized in an RF transceiver may be implemented in a low form factor module of less than 1.1mm thick according to an embodiment of the invention.

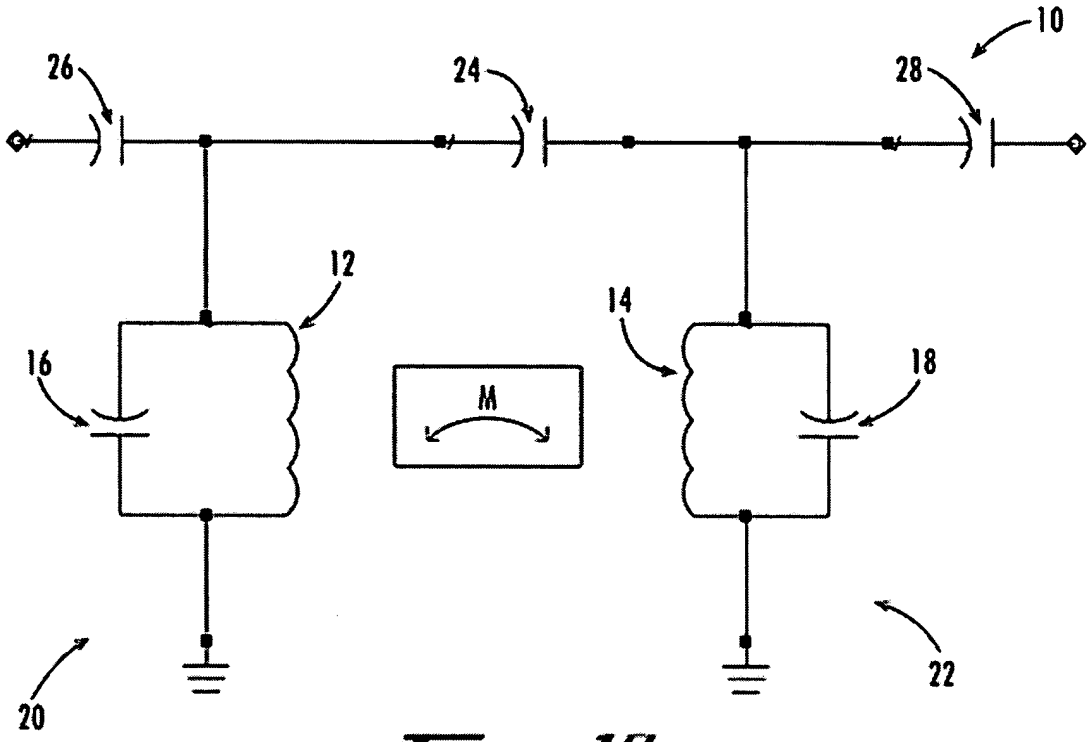


Fig. 1A

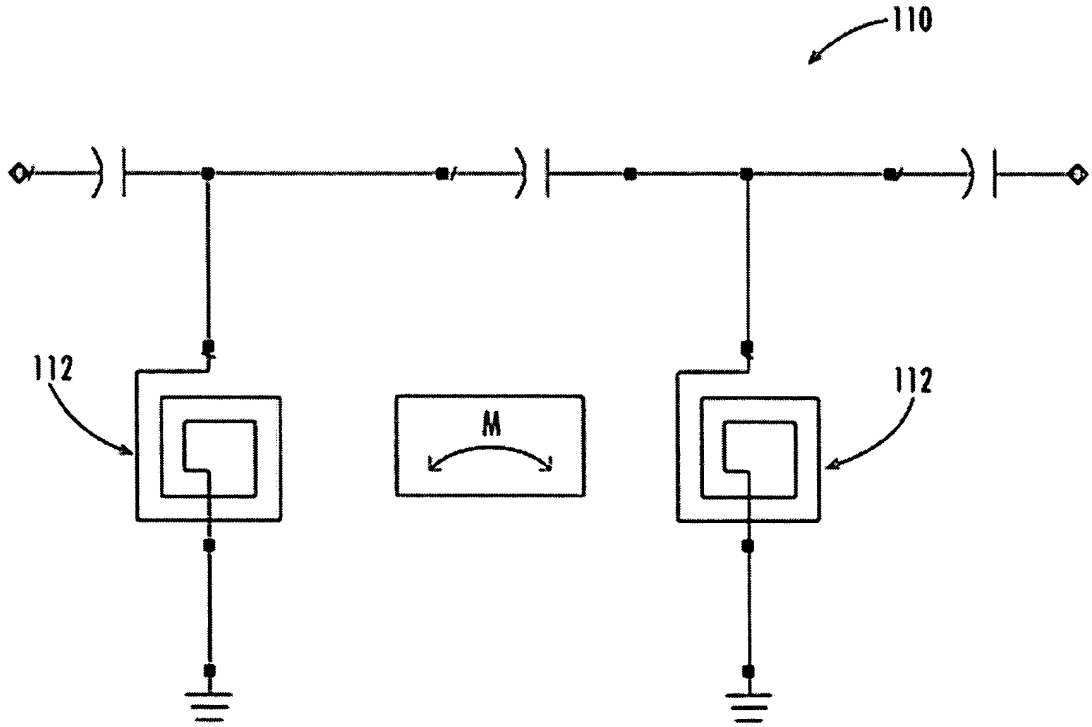


Fig. 1B

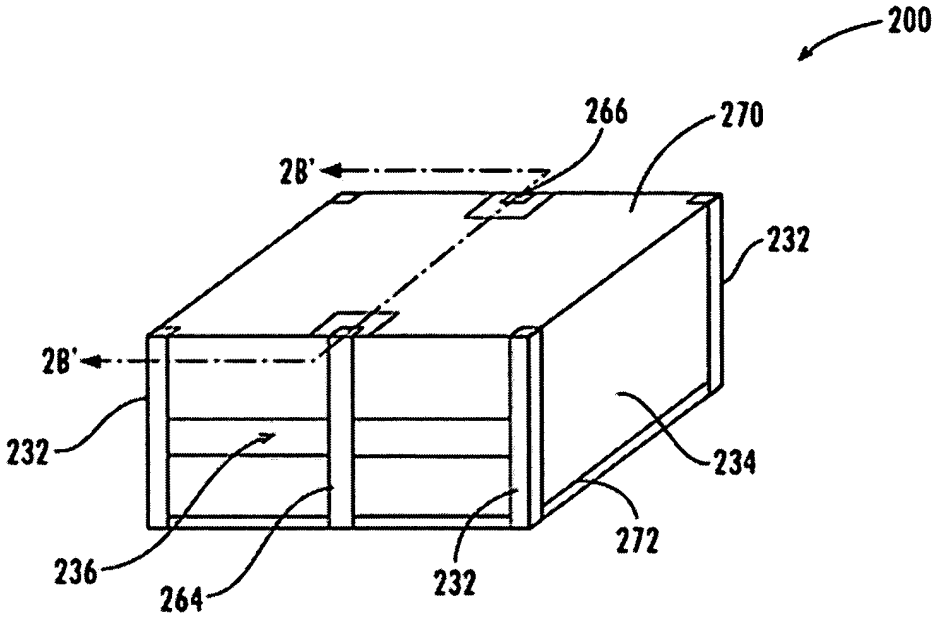

200
266
270
28'
232
28'
232
234
236
264
232
272

Fig. 2A

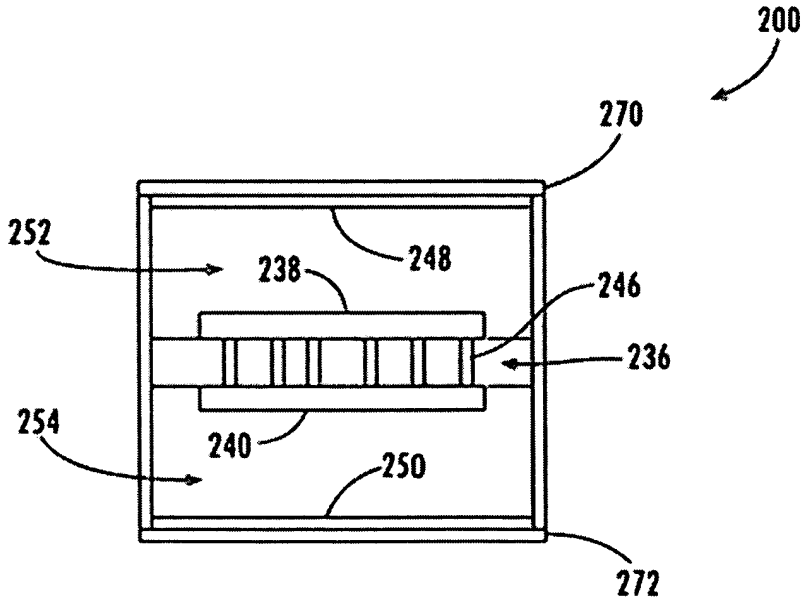

200
270
252
248
238
246
236
254
240
250
272

Fig. 2B

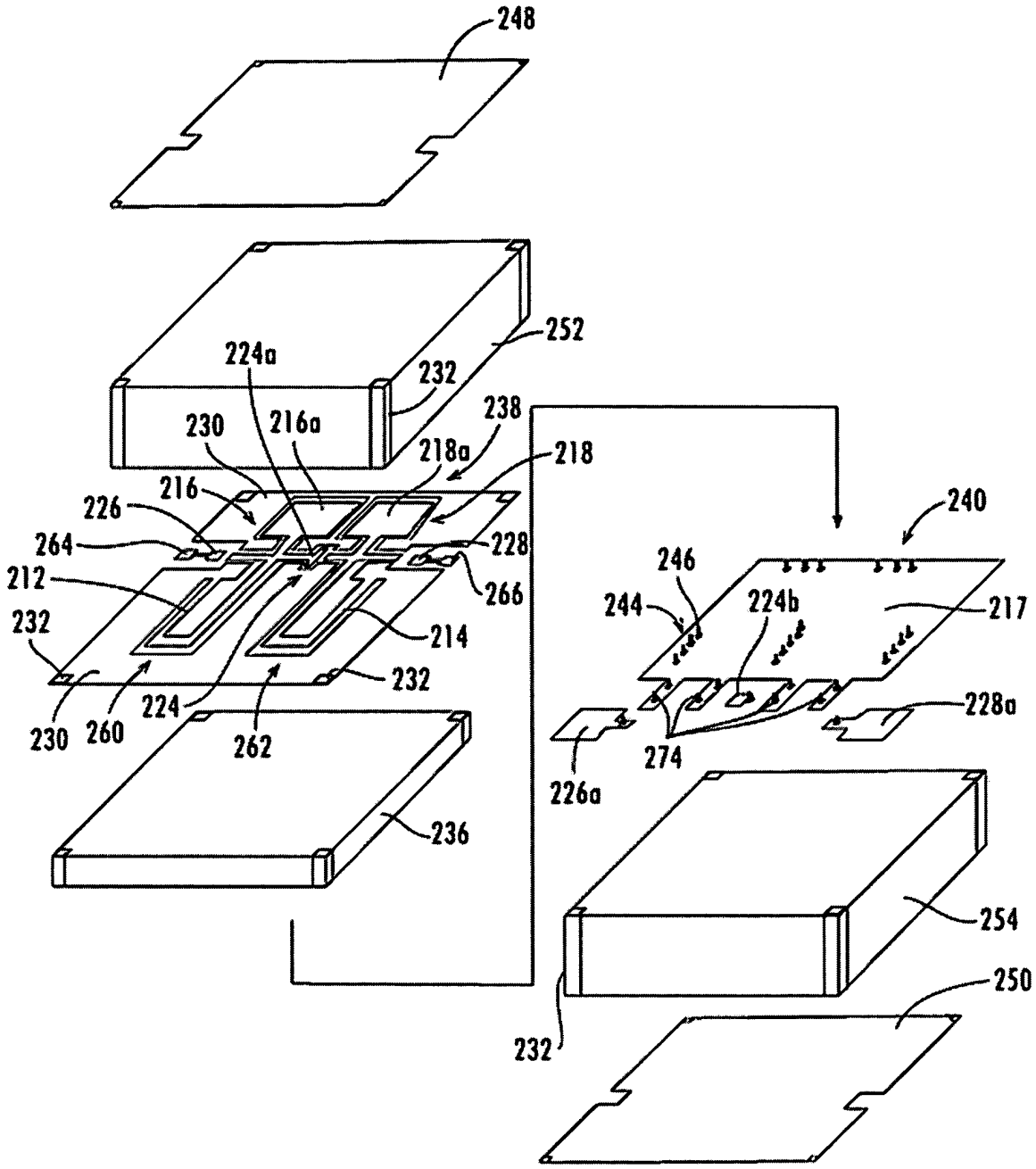

248
252
224a
232
230
216a
238
218a
218
216
226
264
228
212
266
214
232
232
230
260
224
262
236
240
246
244
224b
217
228a
274
226a
254
250
232

Fig. 2C

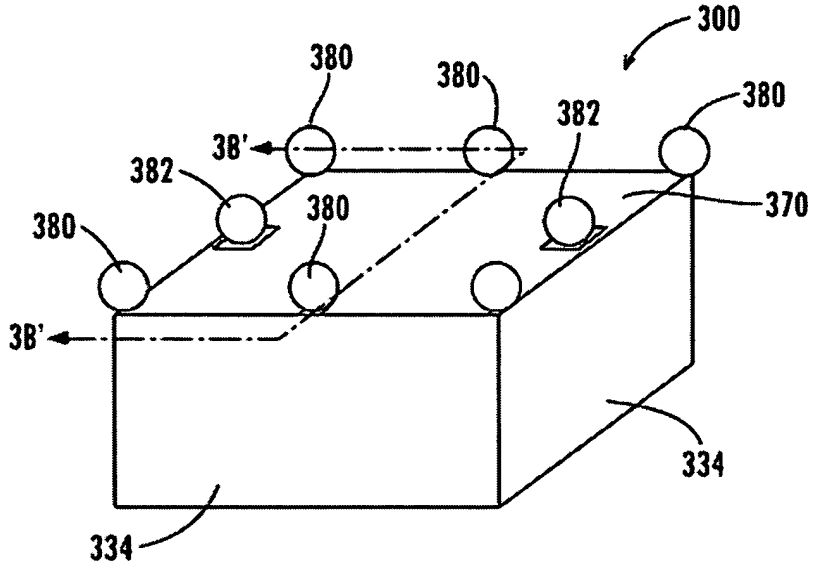

300
380
380
380
382
382
38'
380
380
370
3B'
334
334

Fig. 3A

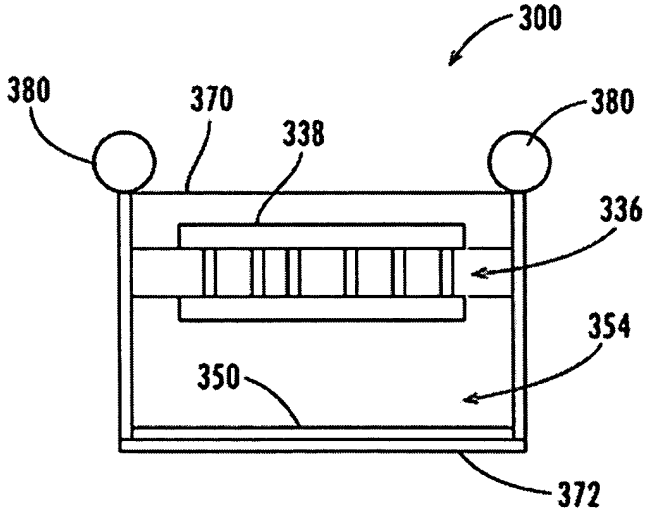

300
380
370
338
380
336
354
350
372

Fig. 3B

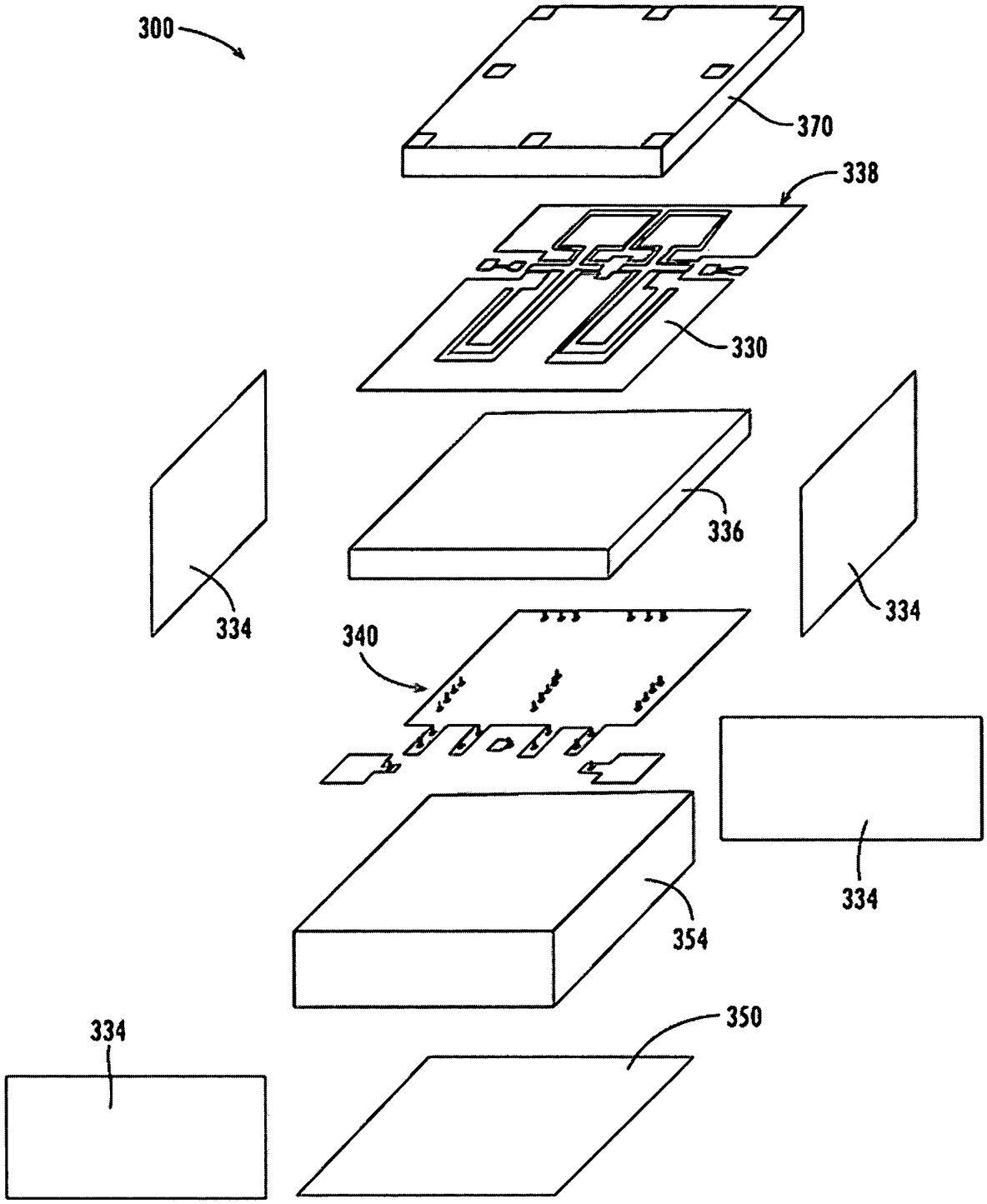


Fig. 3C

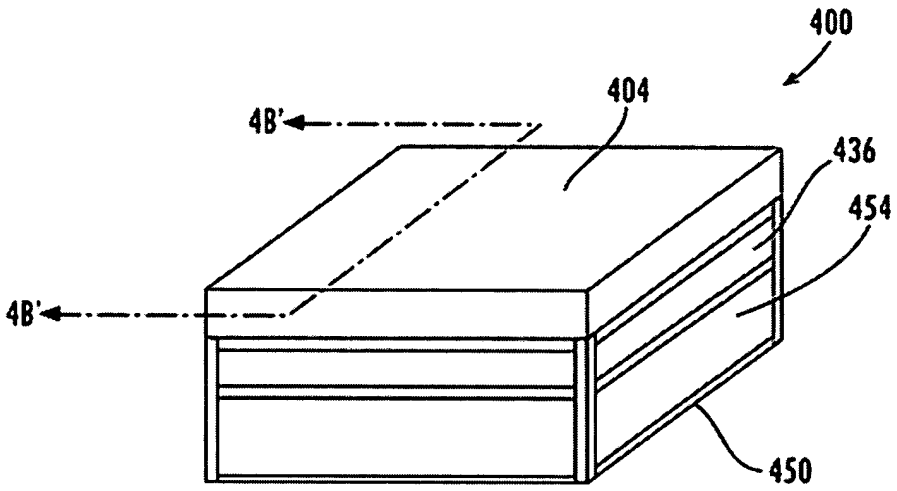


Fig. 4A

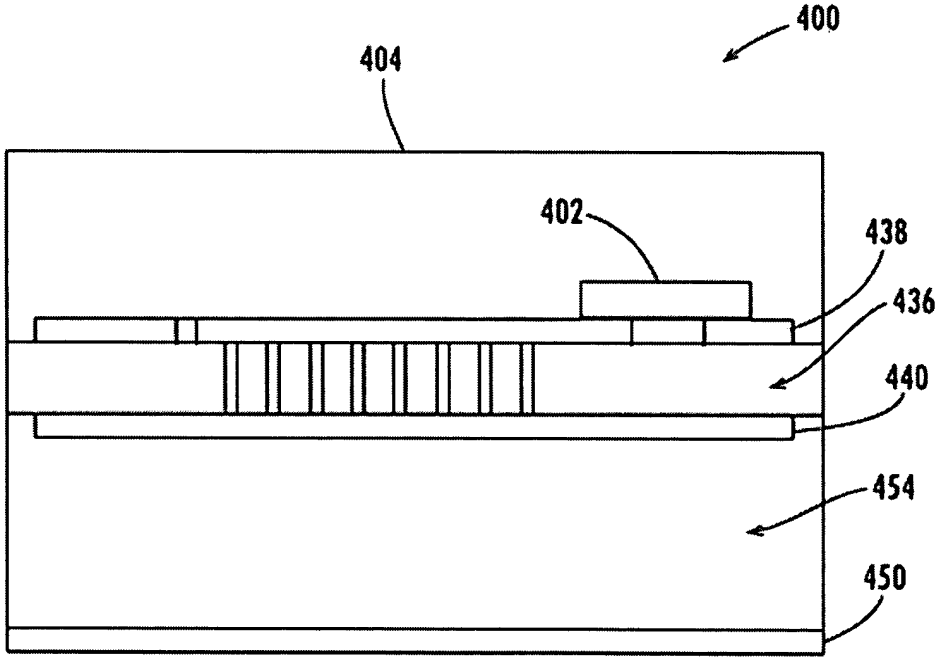


Fig. 4B

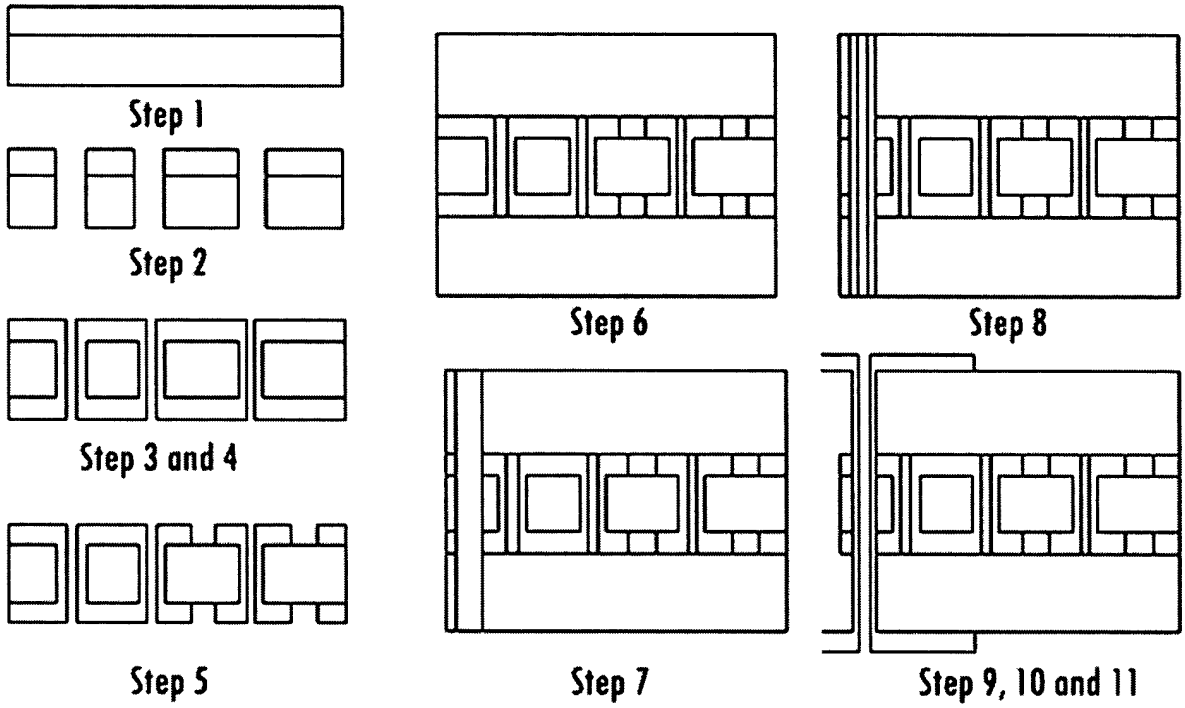

Step 1
Step 2
Step 3 and 4
Step 5
Step 6
Step 7
Step 8
Step 9, 10 and 11

Fig. 5

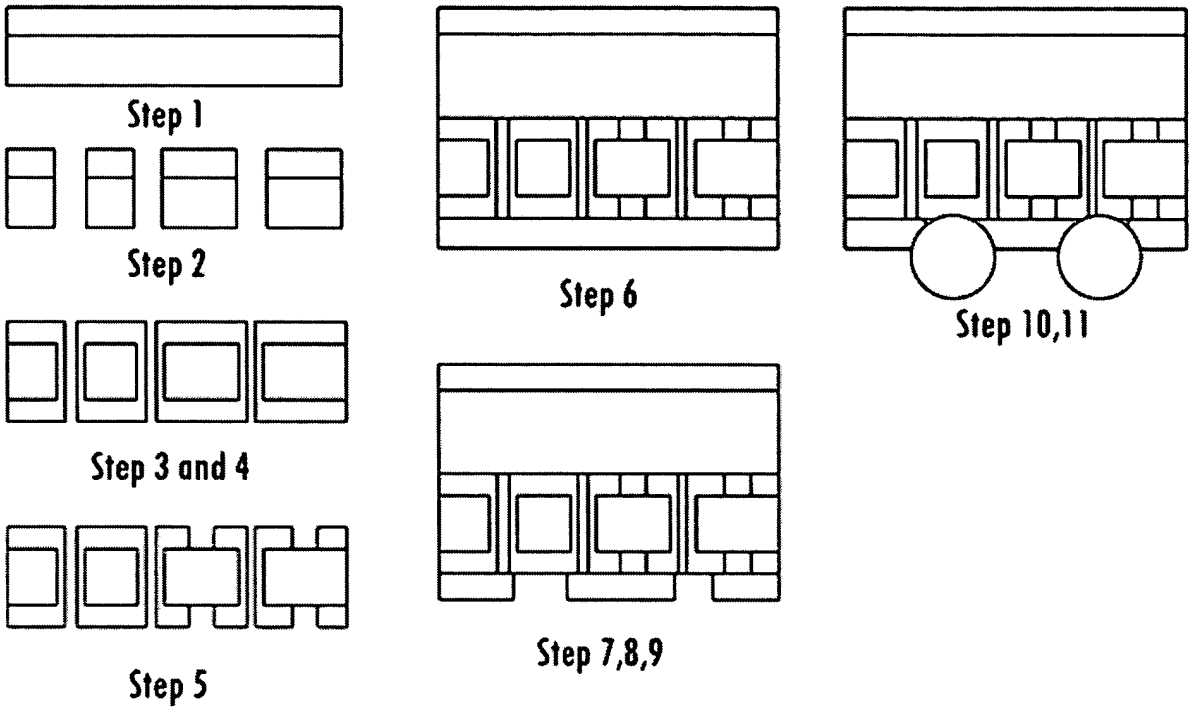


Fig. 6

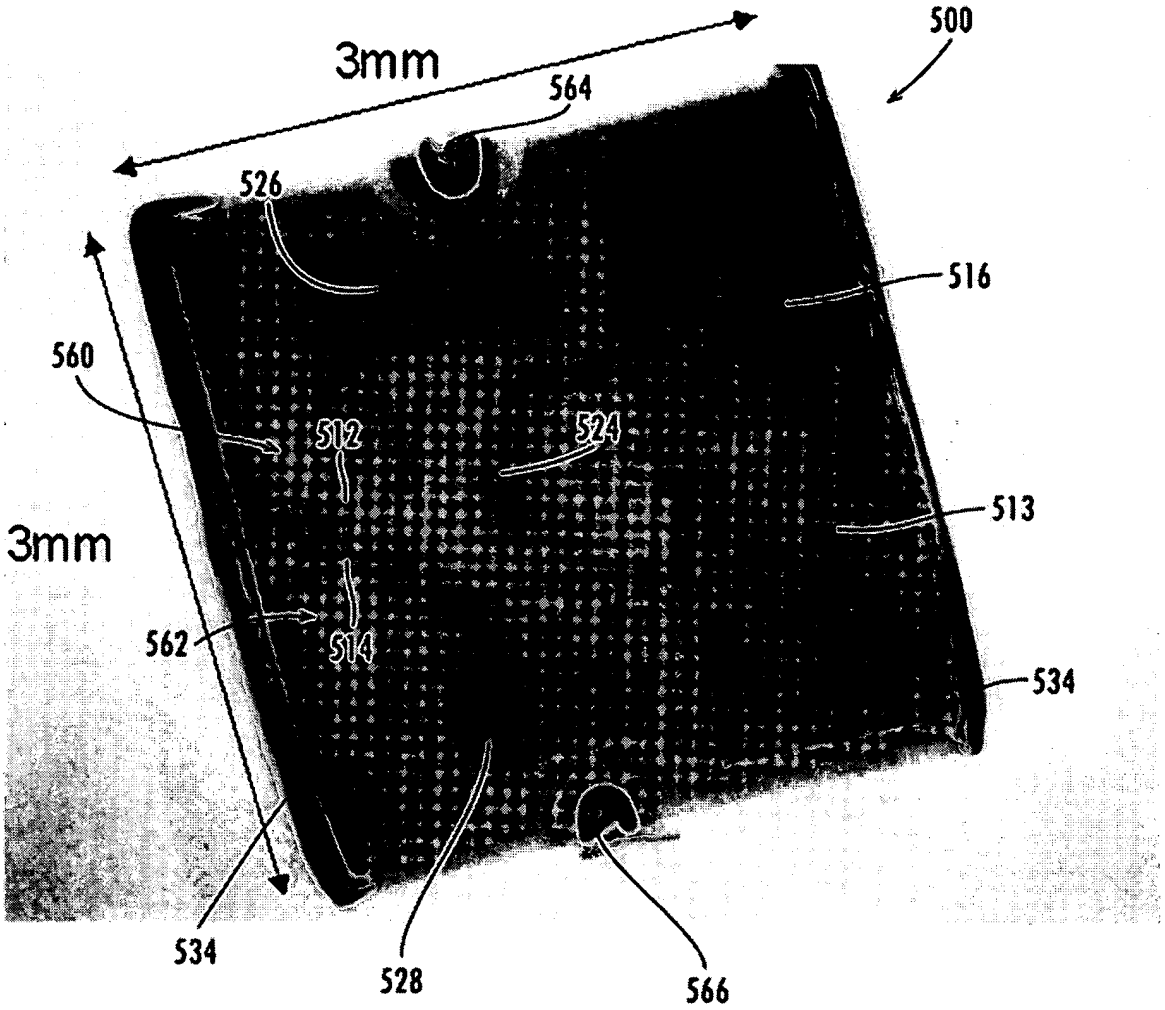


Fig. 1

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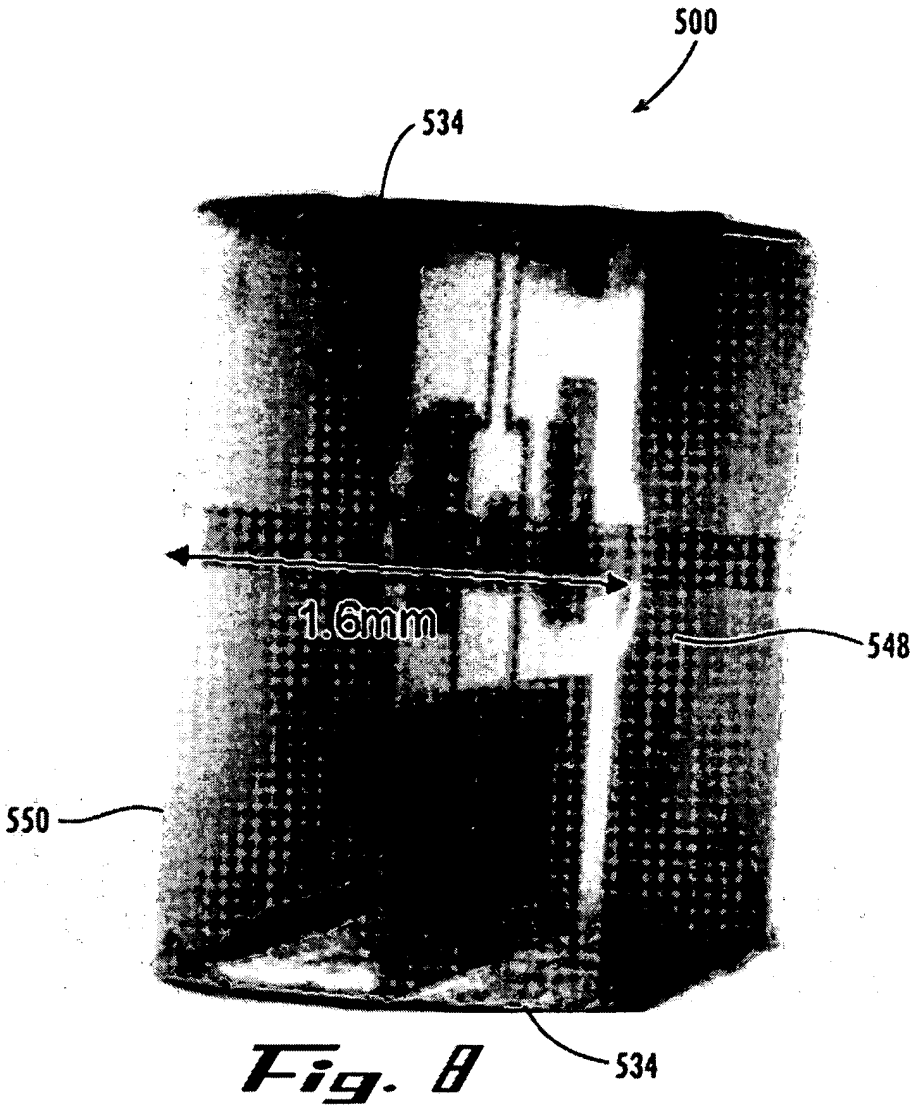


Fig. 8

BEST AVAILABLE COPY

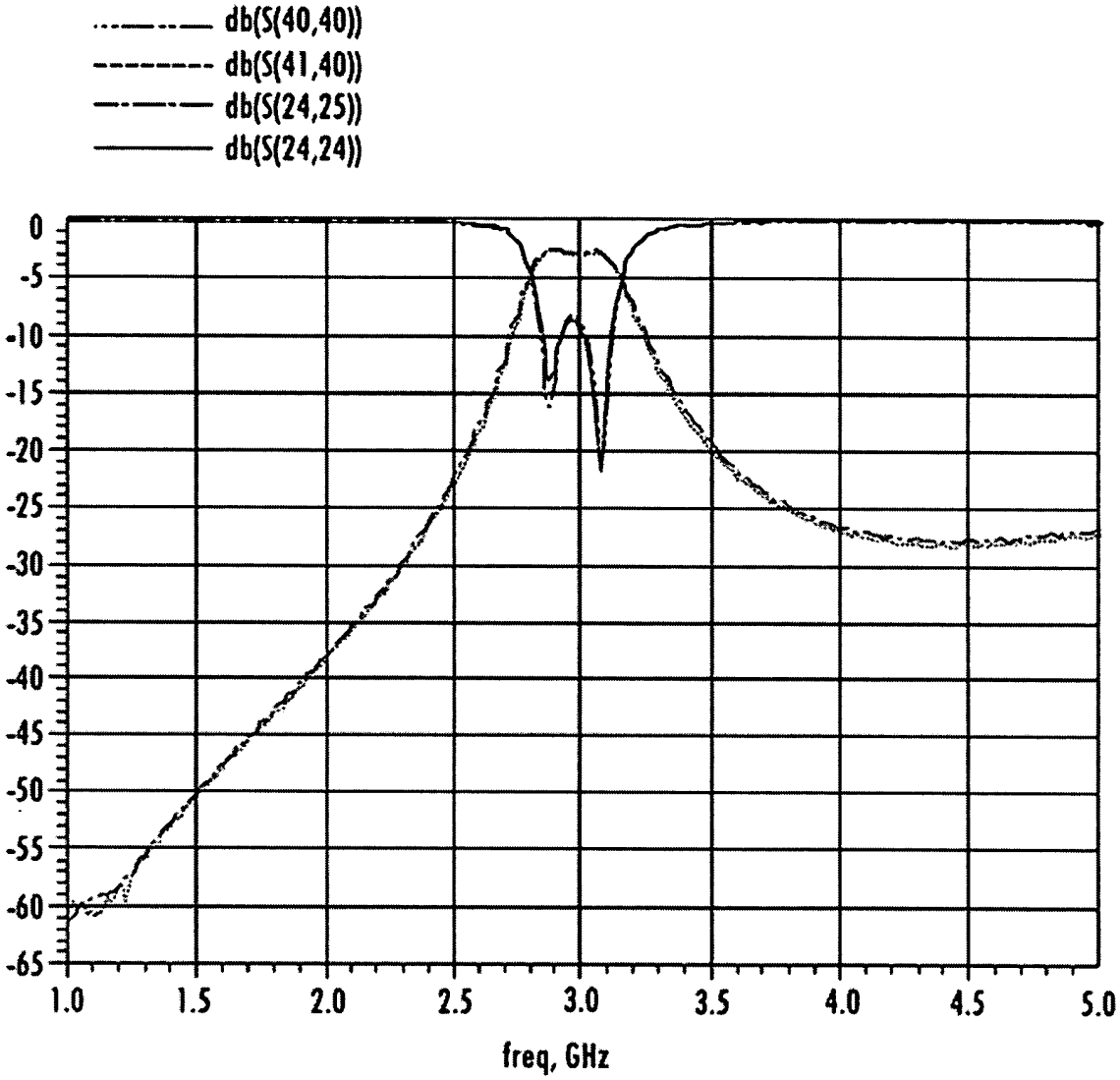

db(S(40,40))
db(S(41,40))
db(S(24,25))
db(S(24,24))
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50
-55
-60
-65
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
freq, GHz

Fig. 9

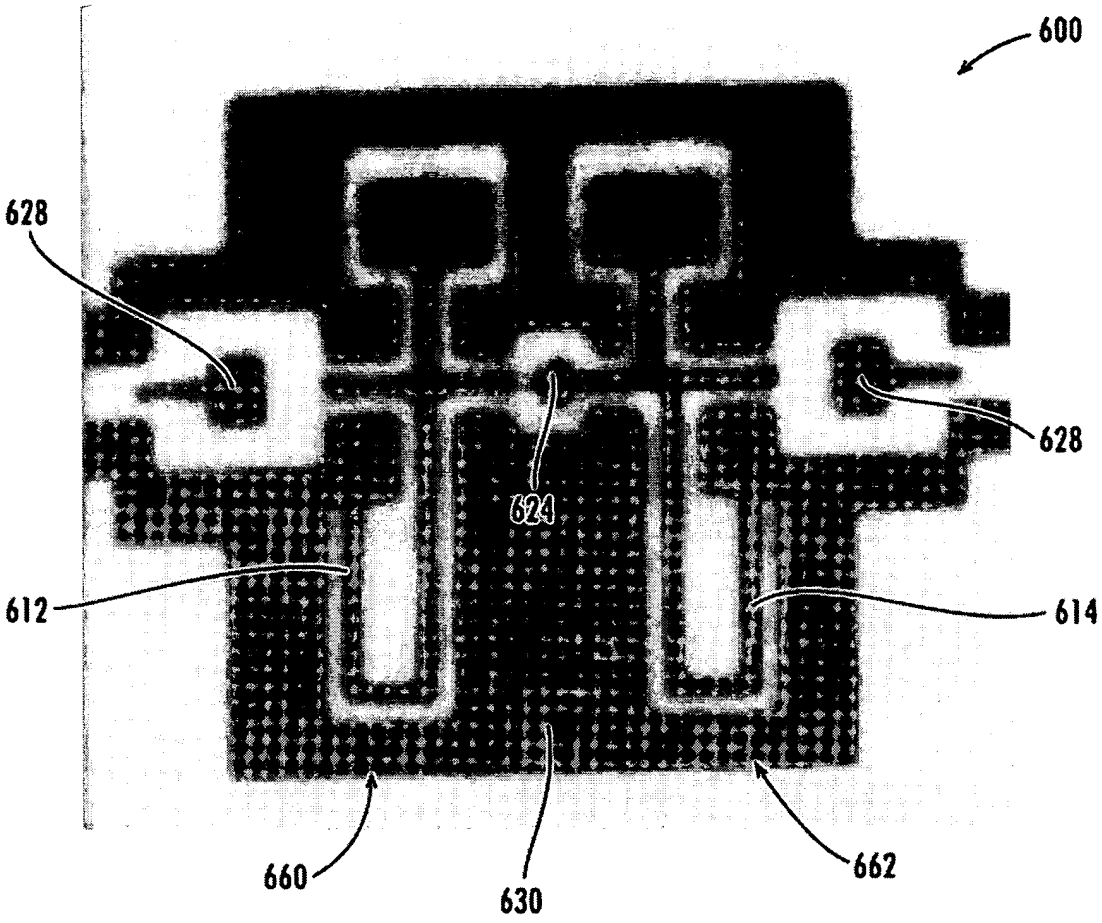


Fig. 10

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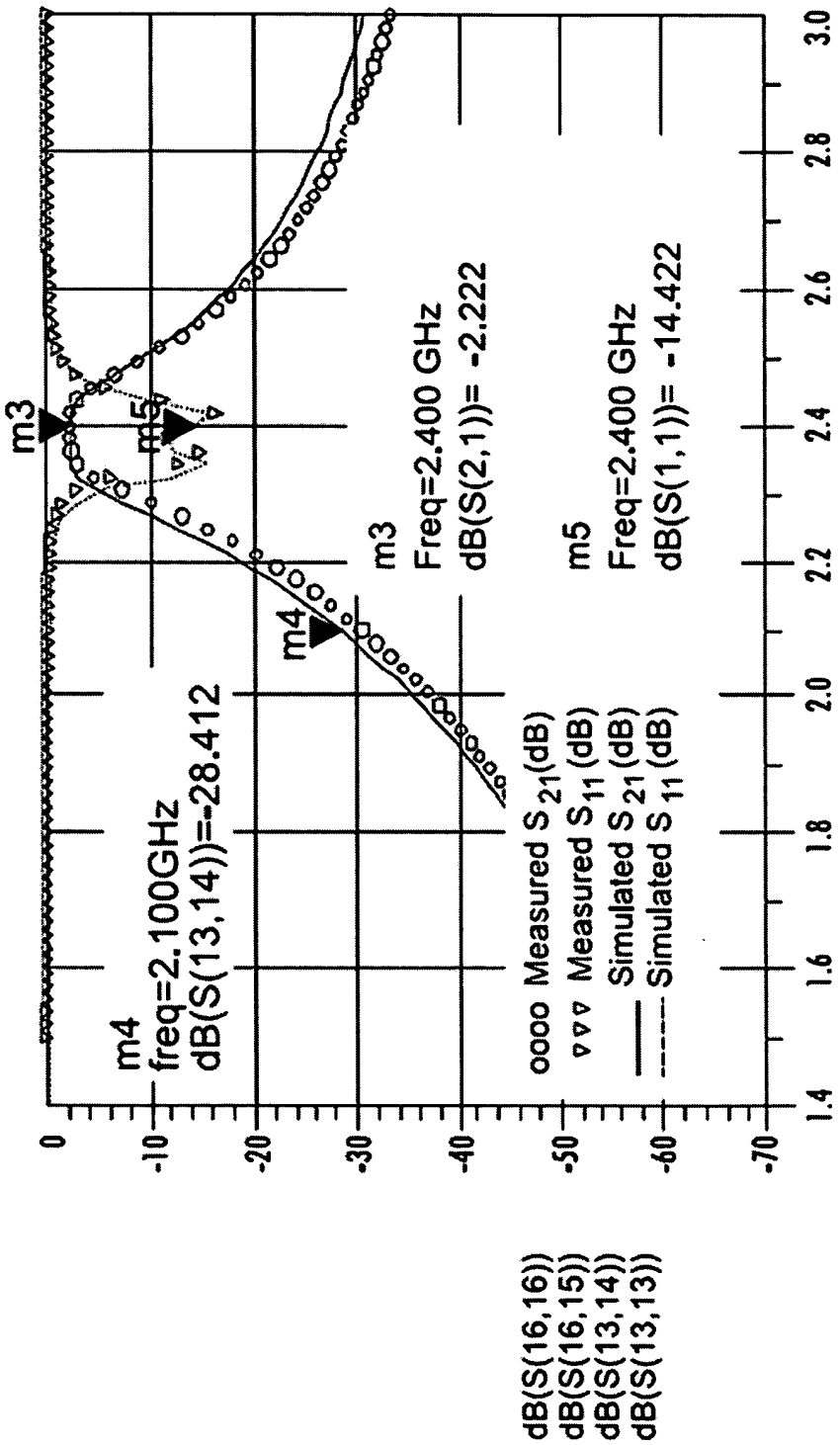

m3
m5
m4
freq=2.100GHz
dB(S(13,14))=-28.412
m3
Freq=2.400 GHz
dB(S(2,1))= -2.222
m5
Freq=2.400 GHz
dB(S(1,1))= -14.422
oooo Measured S21(dB)
vvv Measured S11 (dB)
Simulated S21 (dB)
Simulated S11 (dB)
dB(S(16,16))
dB(S(16,15))
dB(S(13,14))
dB(S(13,13))
freq, GHz
0
-10
-20
-30
-40
-50
-60
-70
1.4
1.6
1.8
2.0
2.2
2.4
2.6
2.8
3.0

Fig. 11

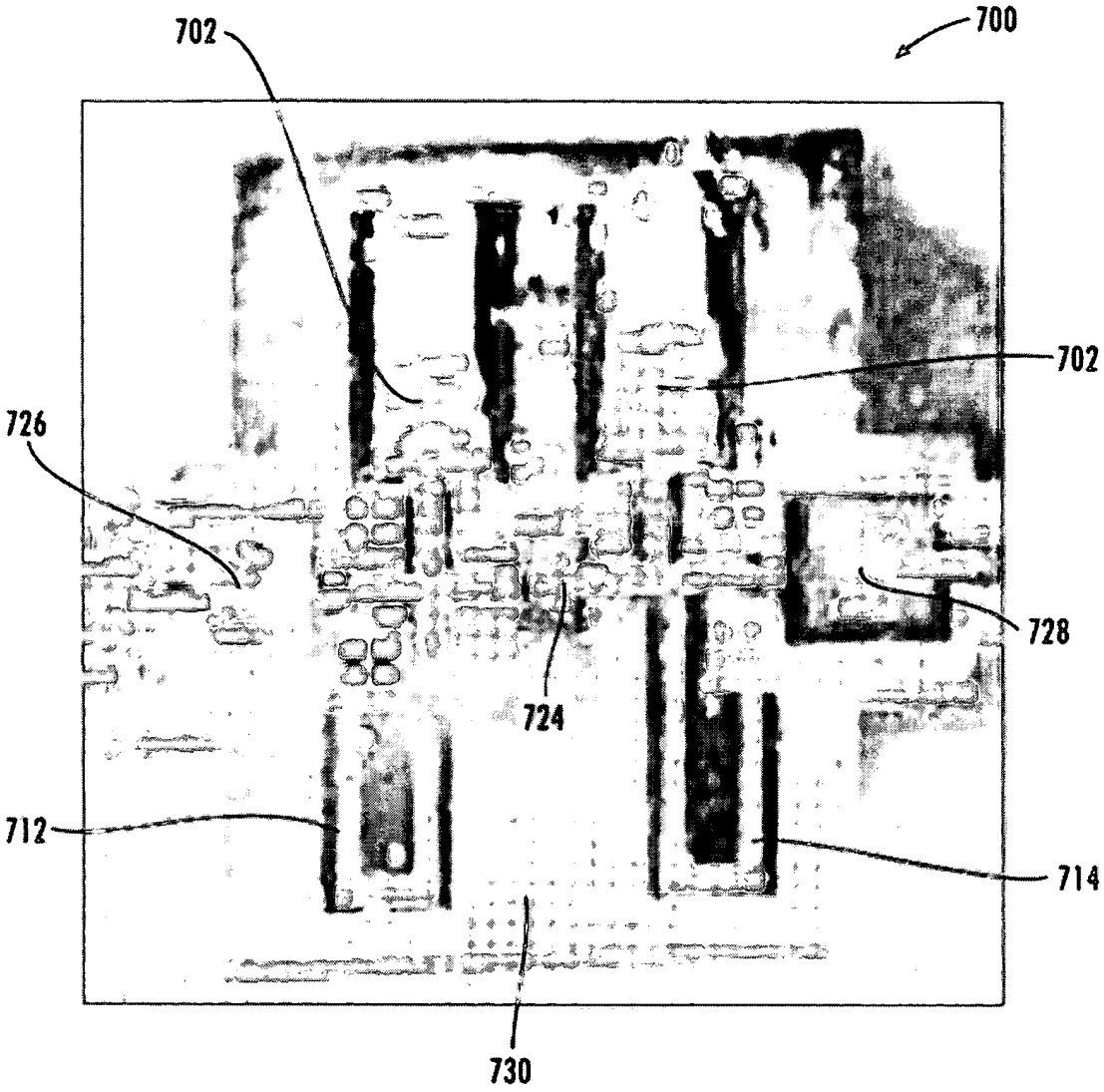


Fig. 12

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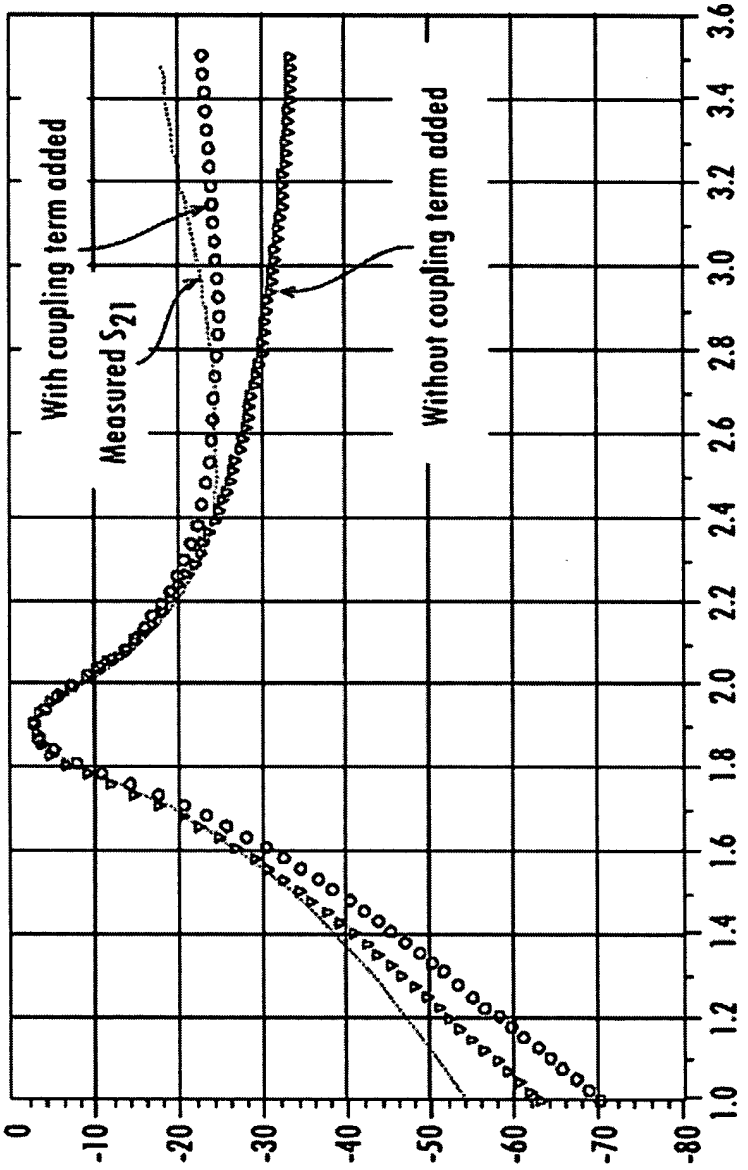

With coupling term added
Measured S_{21}
Without coupling term added
0
-10
-20
-30
-40
-50
-60
-70
-80
1.0
1.2
1.4
1.6
1.8
2.0
2.2
2.4
2.6
2.8
3.0
3.2
3.4
3.6
freq, GHz

Fig. 13

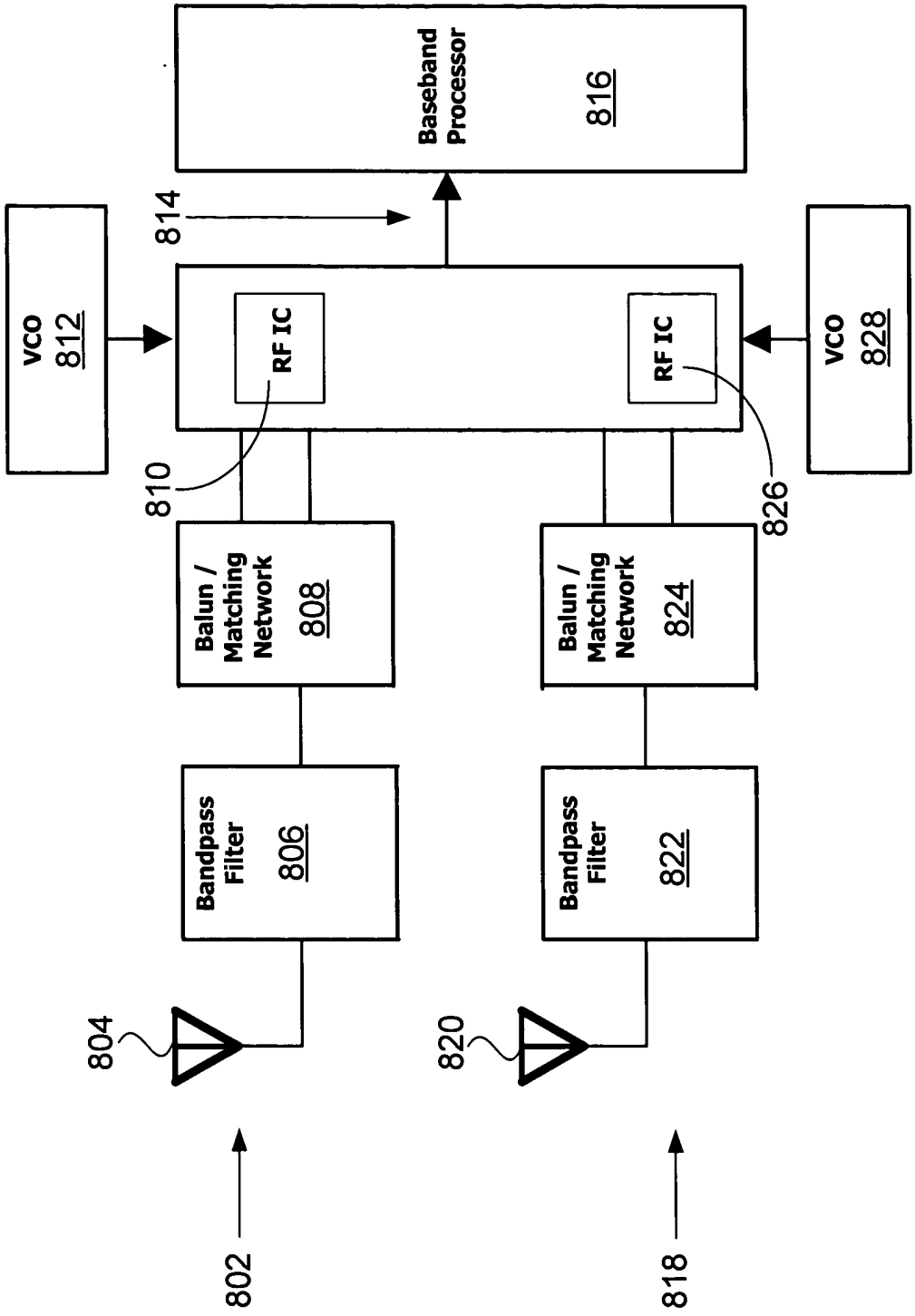

Baseband Processor
816
814
VCO
812
RF IC
RF IC
VCO
828
810
826
Balun / Matching Network
808
Balun / Matching Network
824
Bandpass Filter
806
Bandpass Filter
822
804
820
802
818

FIG. 14

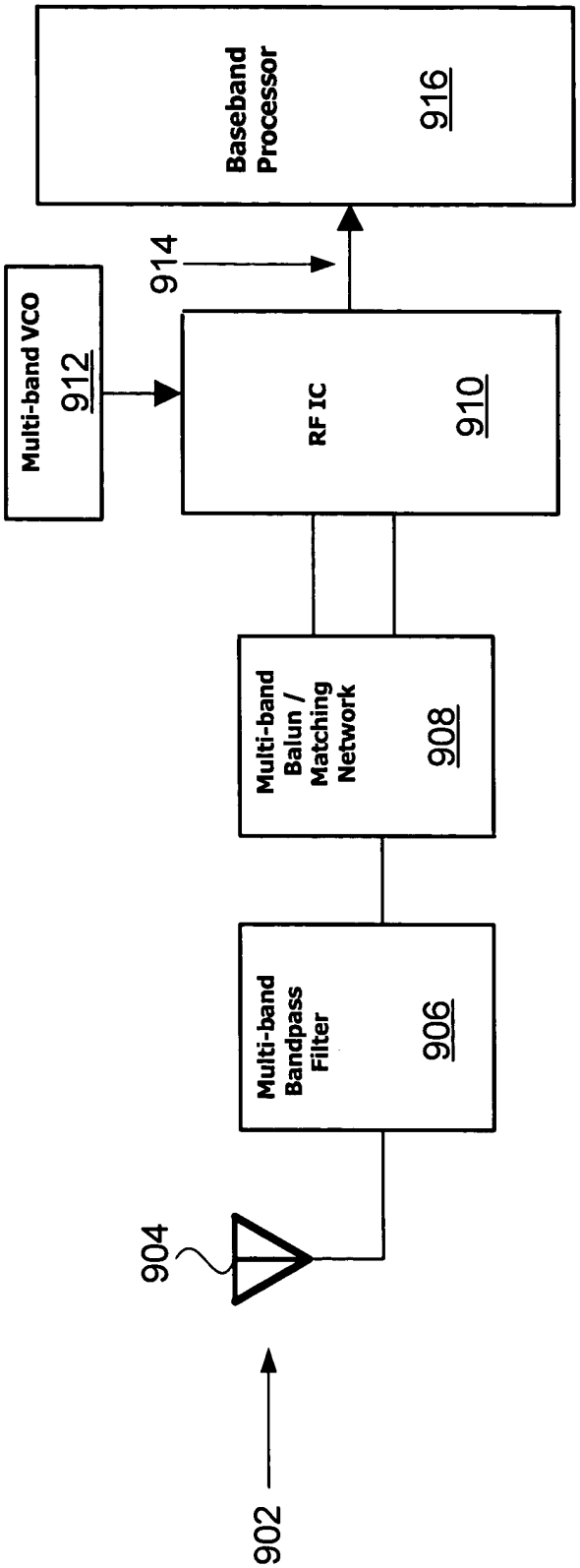

902
904
Multi-band Bandpass Filter
906
Multi-band Balun / Matching Network
908
RF IC
910
Multi-band VCO
912
914
Baseband Processor
916

FIG. 15

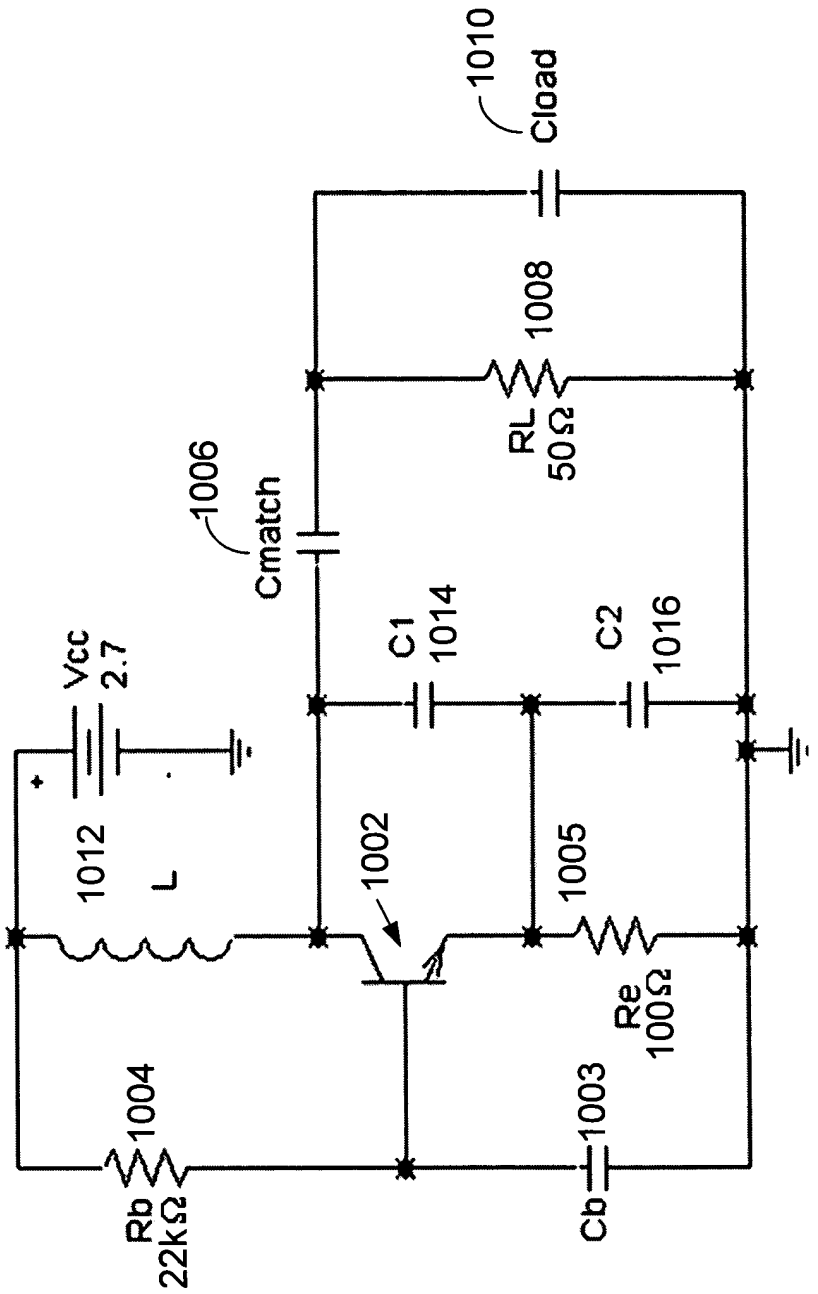

1010
Cload
1008
RL
50Ω
1006
Cmatch
C1
1014
C2
1016
Vcc
2.7
1012
L
1002
1005
Re
100Ω
1004
Rb
22kΩ
1003
Cb

FIG. 16A

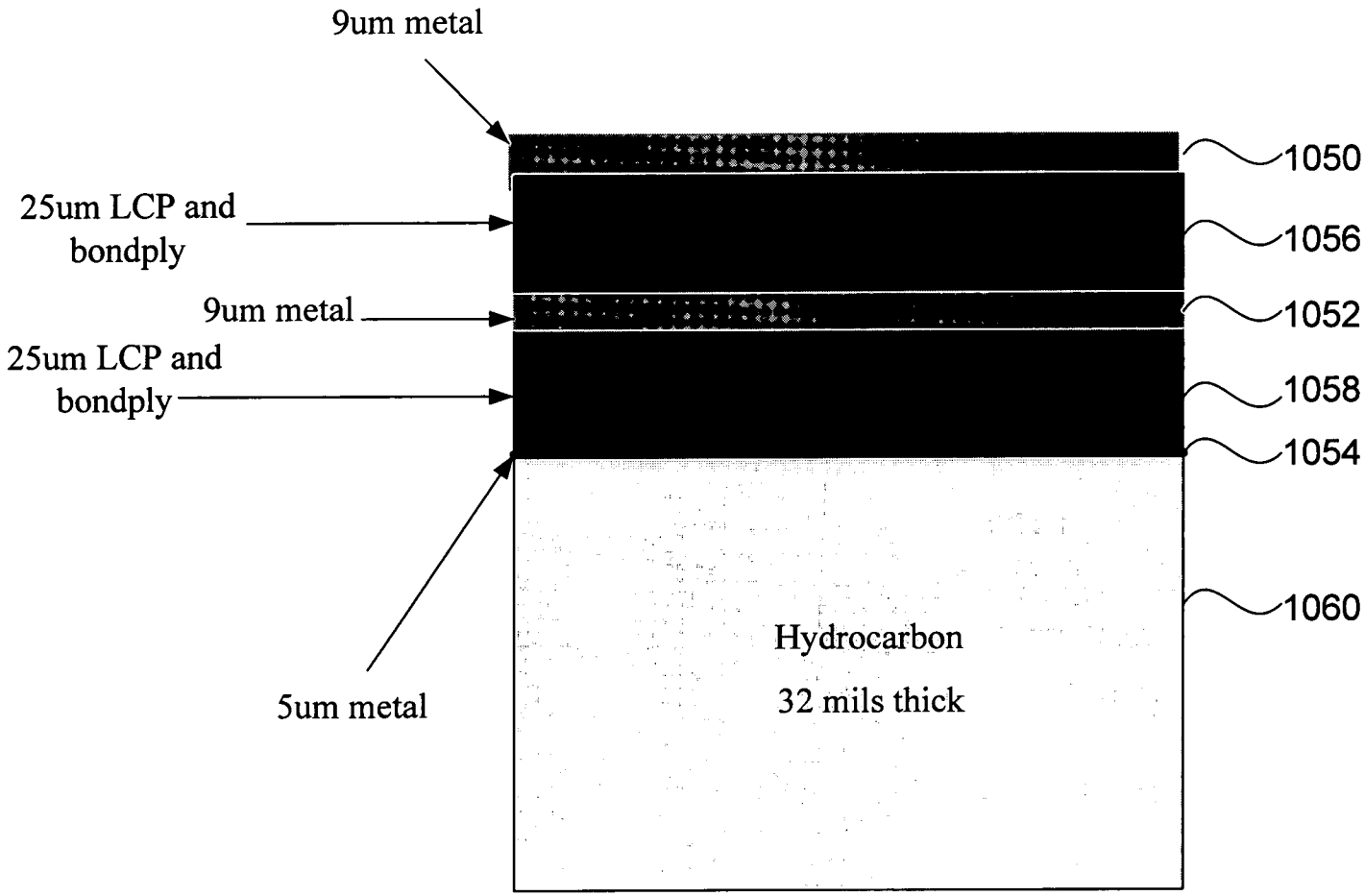


FIG. 16B

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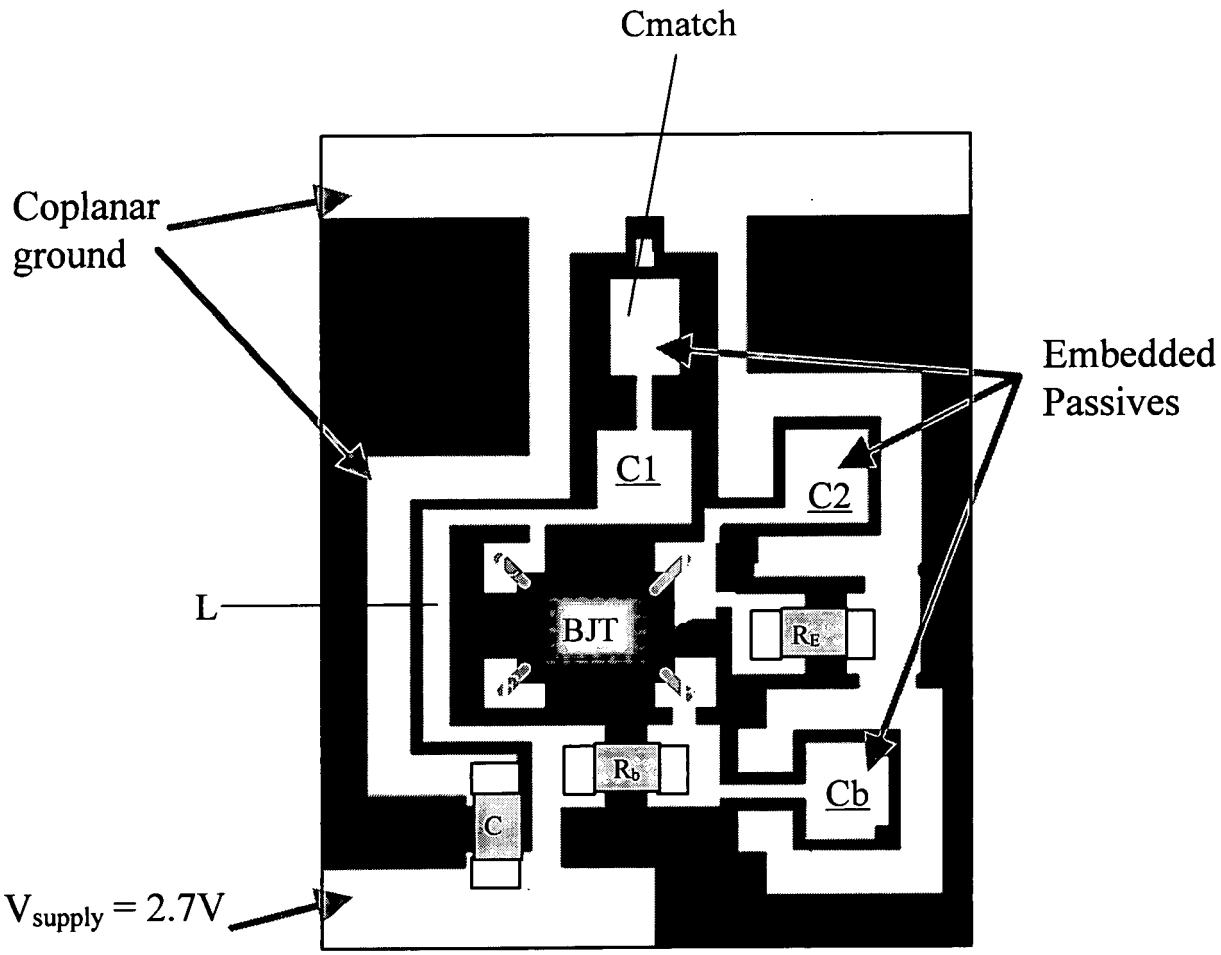


FIG. 16C

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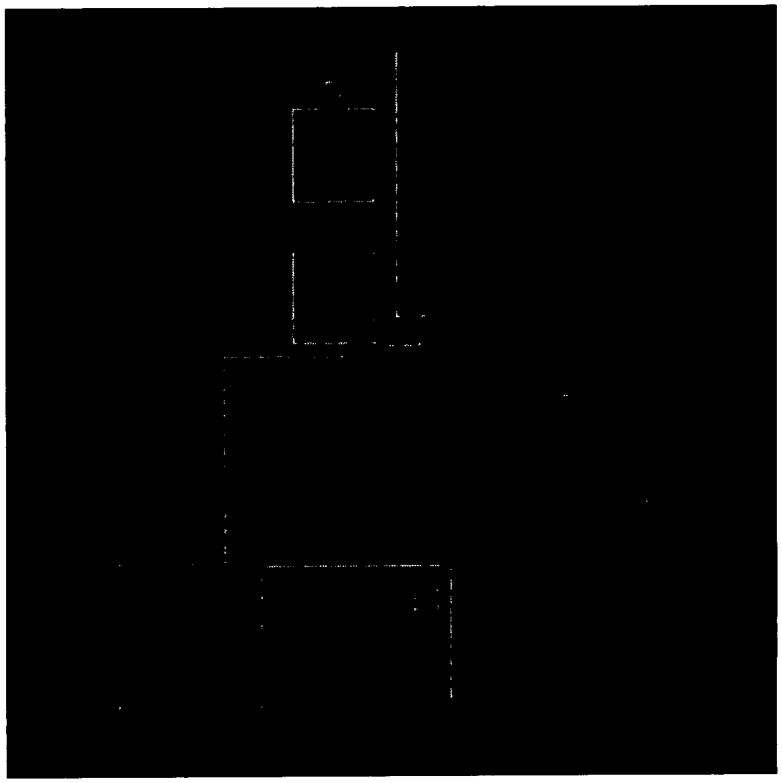


FIG. 16D

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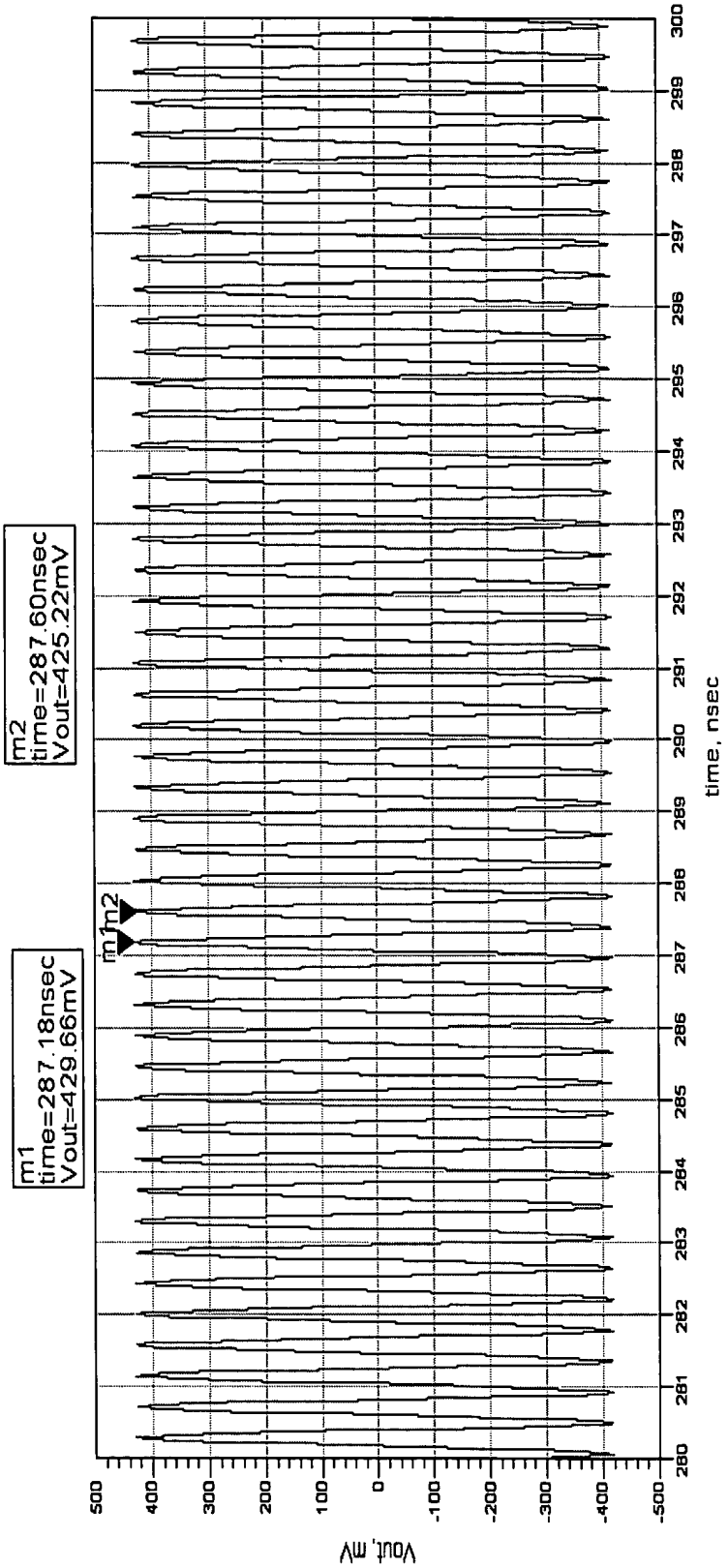

m1
time=287.18nsec
Vout=429.66mV
m2
time=287.60nsec
Vout=425.22mV
m1m2
Vout, mV
time, nsec
500
400
300
200
100
0
-100
-200
-300
-400
-500
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300

FIG. 17

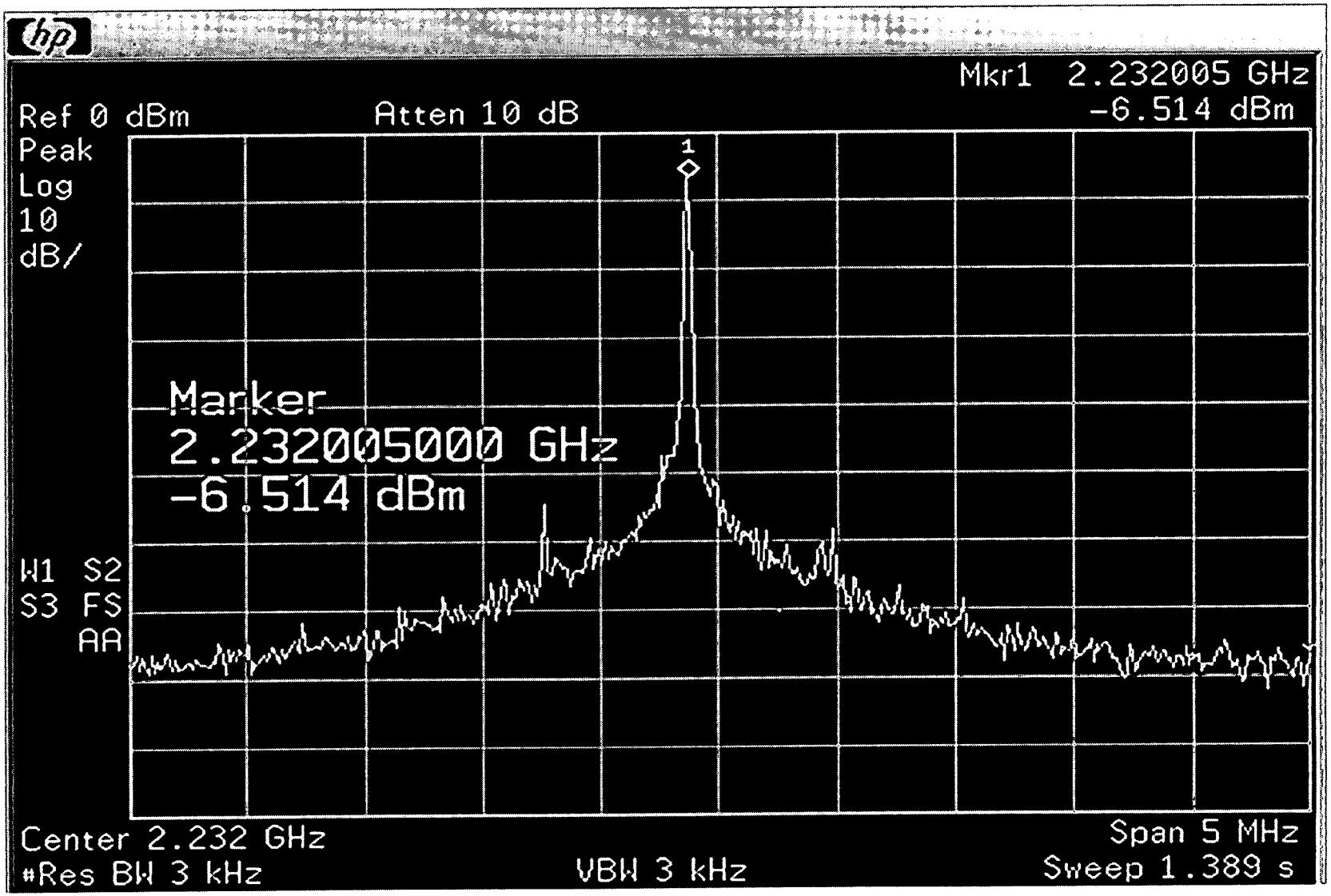


FIG. 18

BEST AVAILABLE COPY

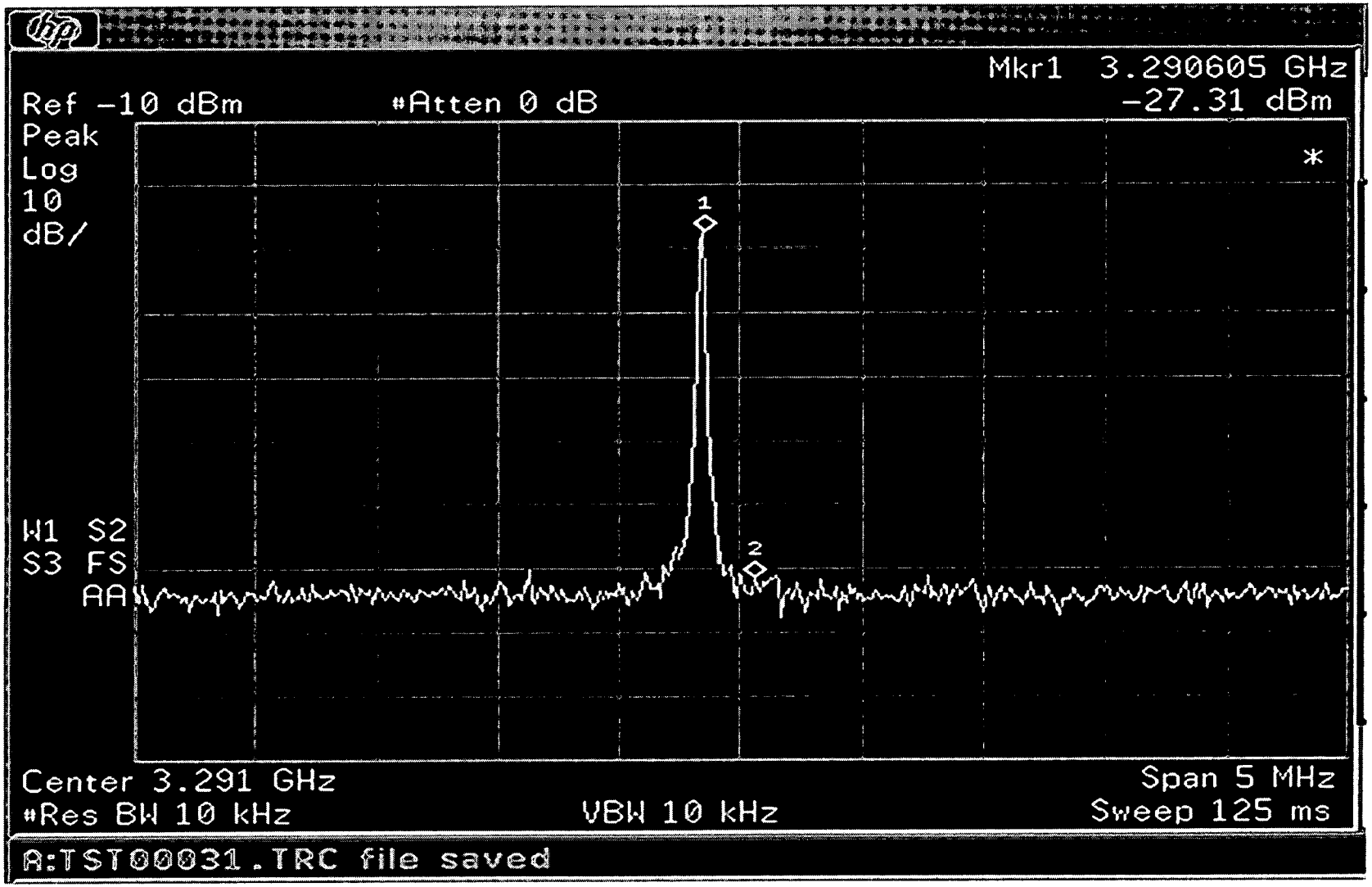


FIG. 19

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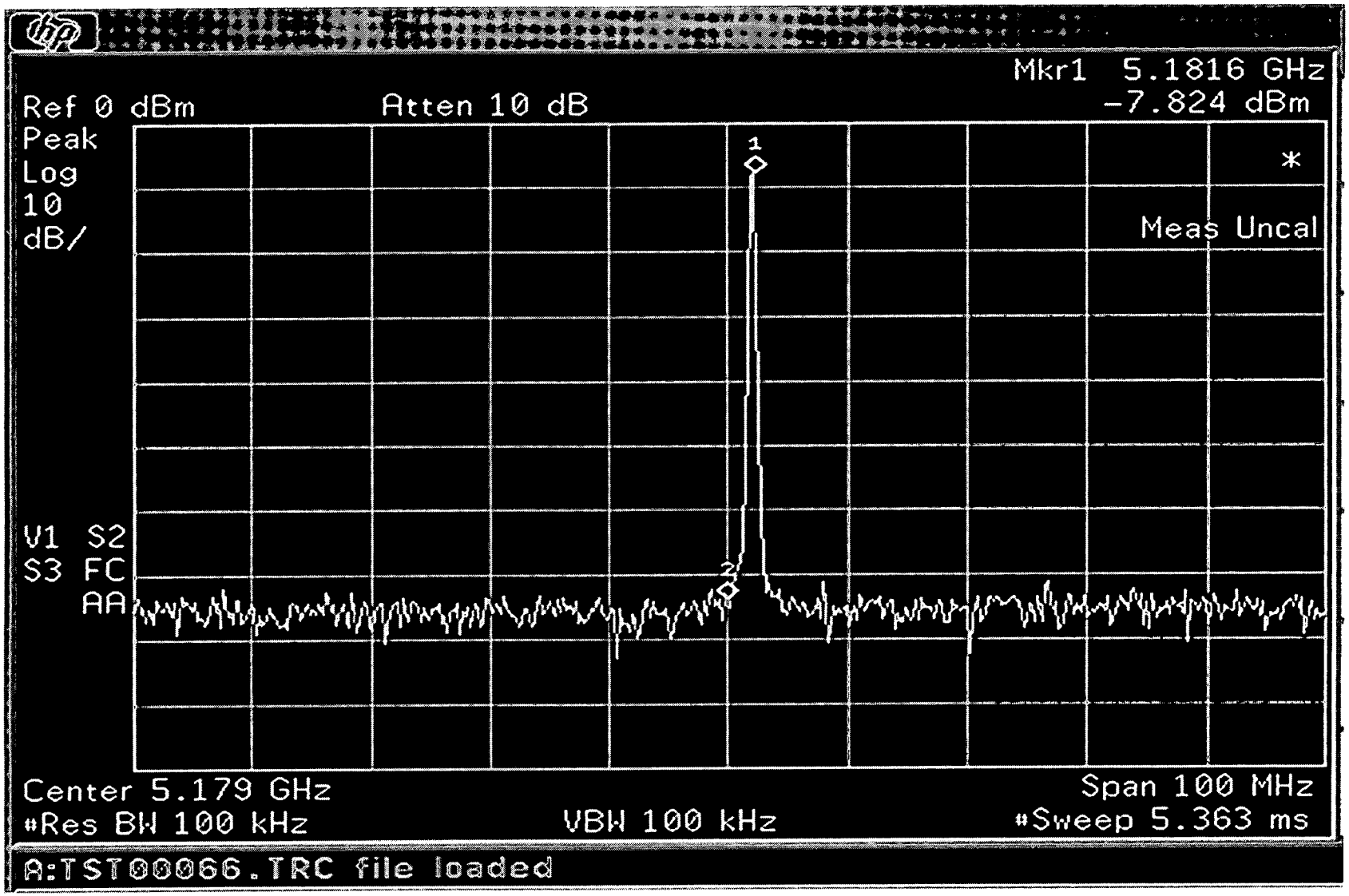


FIG. 20

BEST AVAILABLE COPY

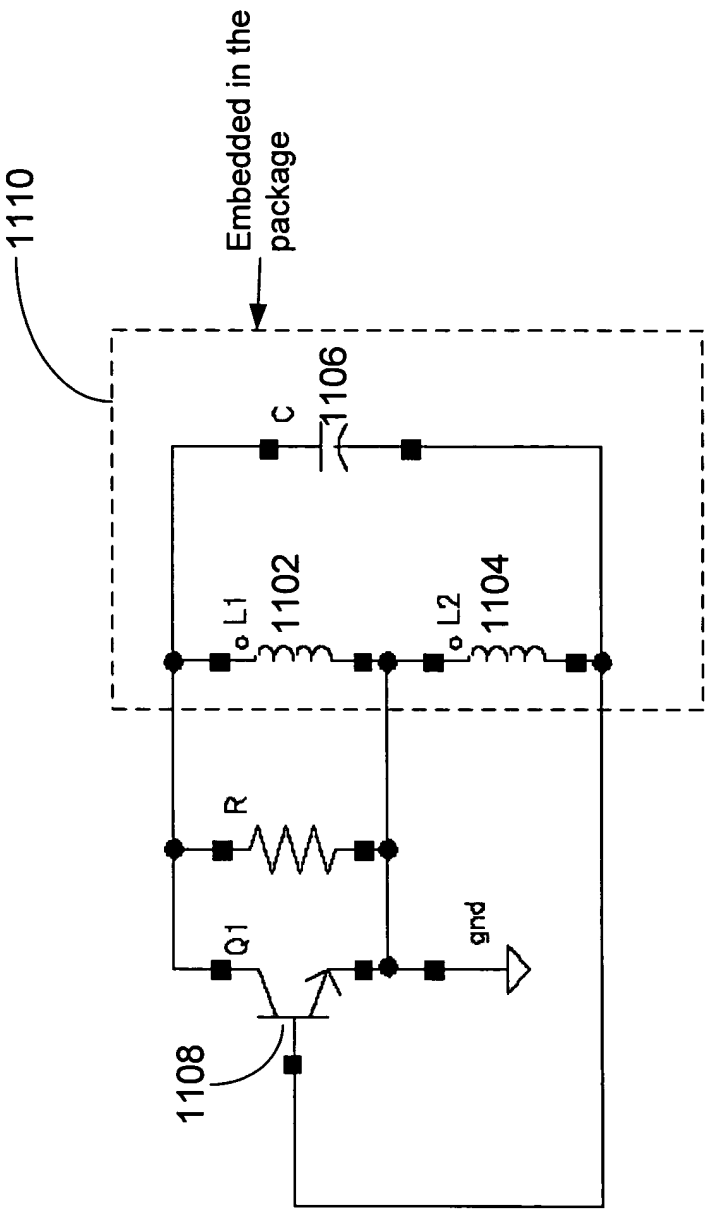

1110
Embedded in the package
C
1106
L1
1102
L2
1104
R
Q1
gnd
1108

FIG. 21

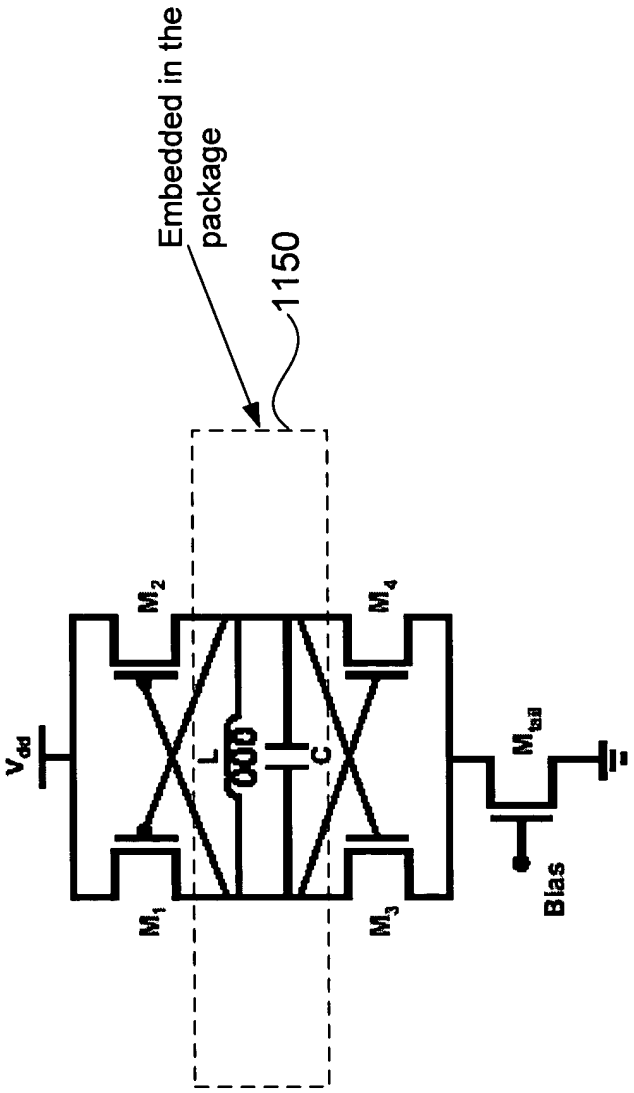


FIG. 22

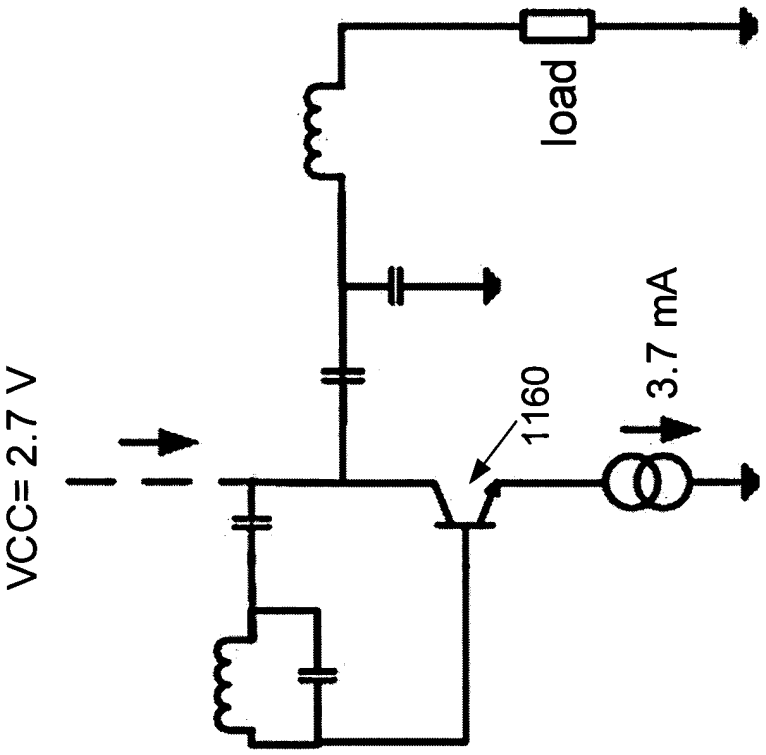


FIG. 23A

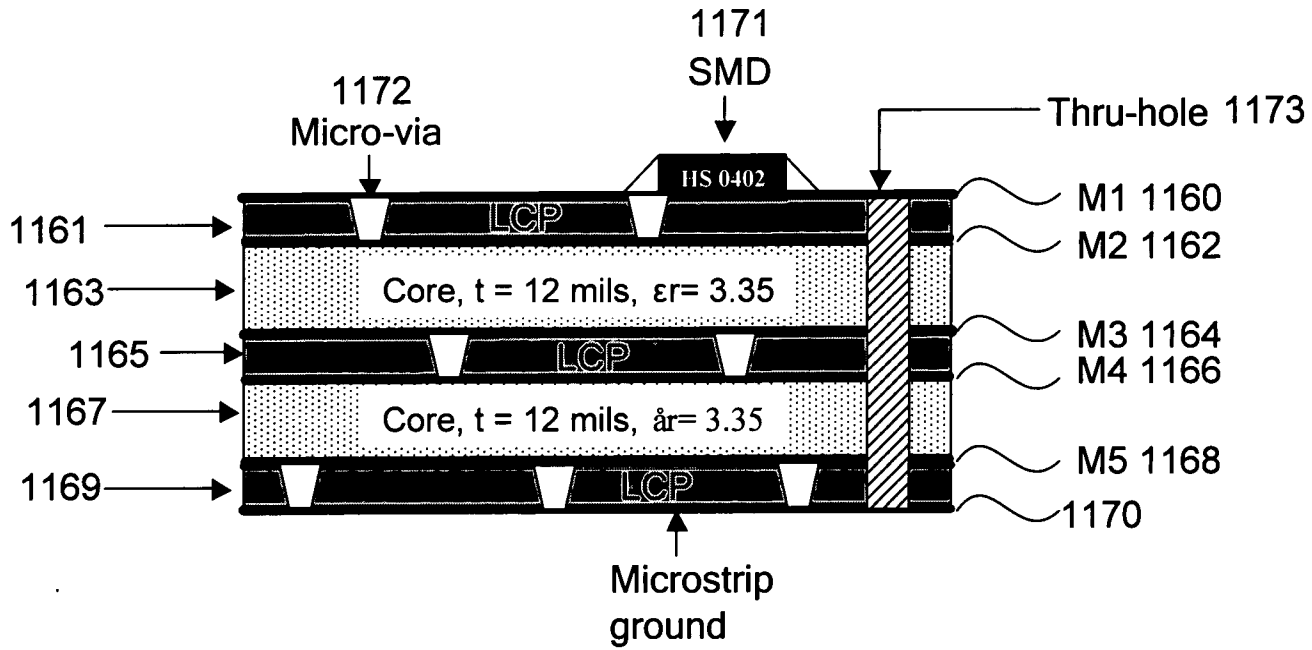


FIG. 23B

BEST AVAILABLE COPY

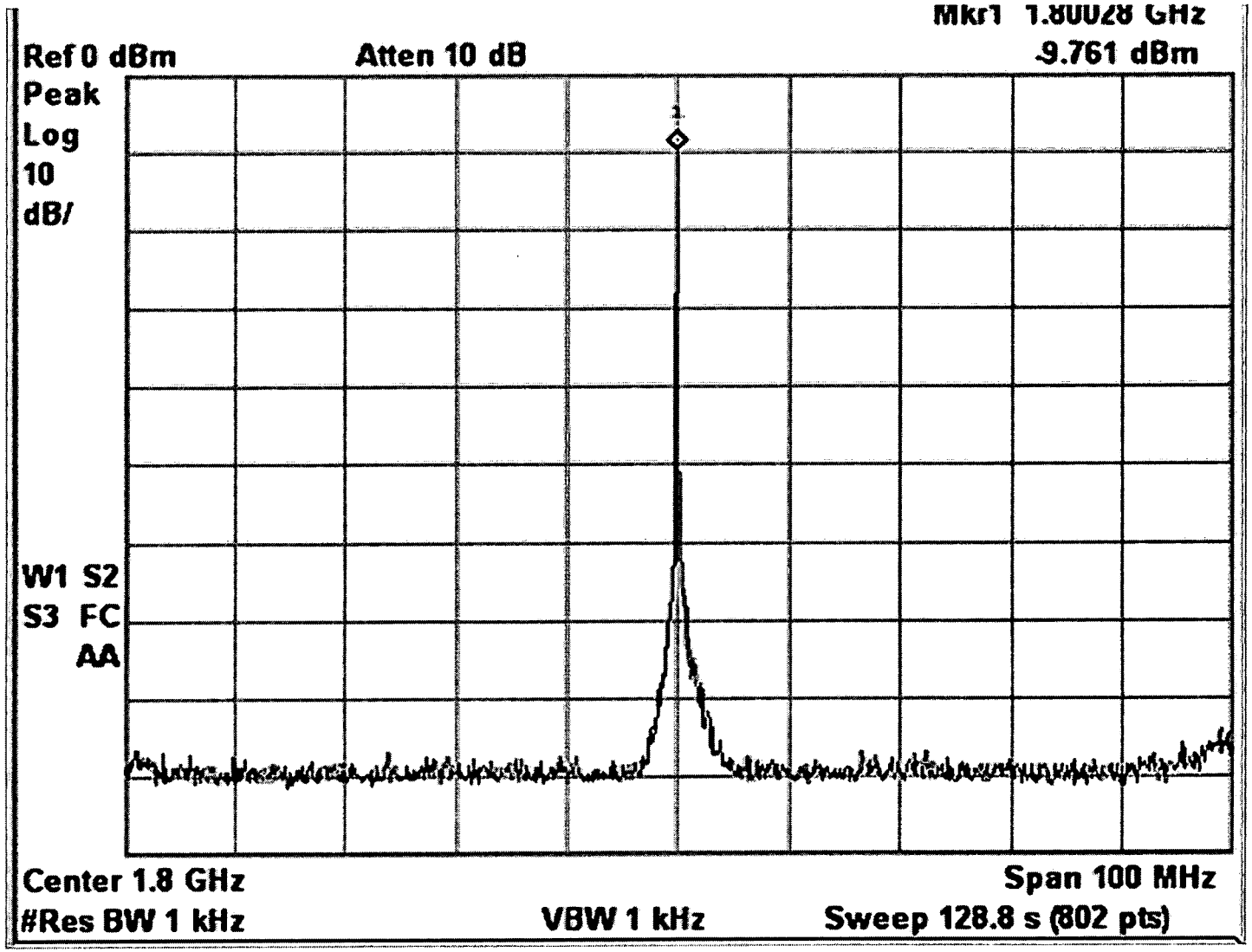

Mkr1 1.80028 GHz
Ref 0 dBm
Atten 10 dB
-9.761 dBm
Peak
Log
10
dB/
W1 S2
S3 FC
AA
Center 1.8 GHz
Span 100 MHz
#Res BW 1 kHz
VBW 1 kHz
Sweep 128.8 s (802 pts)

FIG. 24A

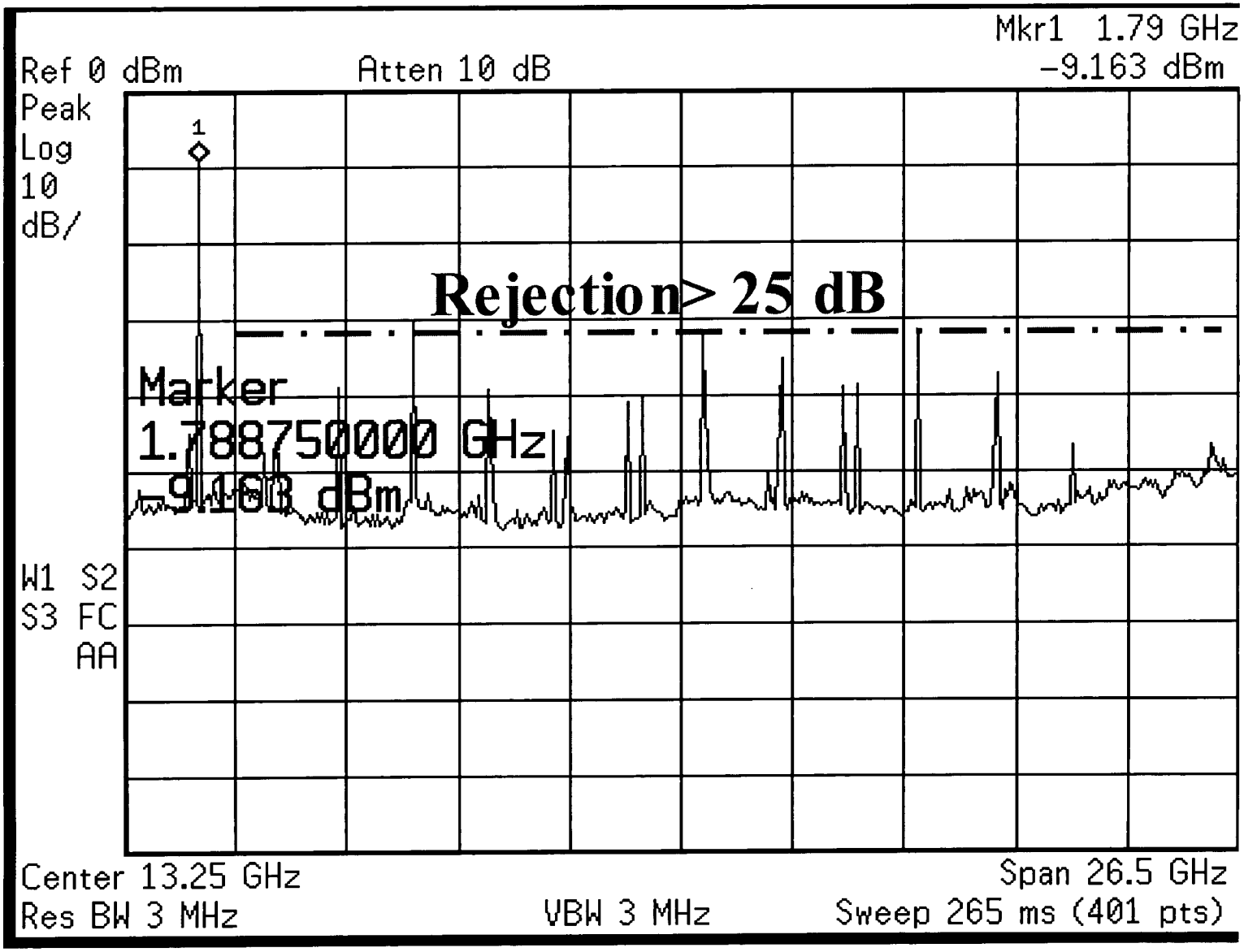

Mkr1 1.79 GHz
-9.163 dBm
Ref 0 dBm
Atten 10 dB
Peak
Log
10
dB/
1
Rejection> 25 dB
Marker
1.788750000 GHz
-9.163 dBm
W1 S2
S3 FC
AA
Center 13.25 GHz
Res BW 3 MHz
VBW 3 MHz
Span 26.5 GHz
Sweep 265 ms (401 pts)

FIG. 24B

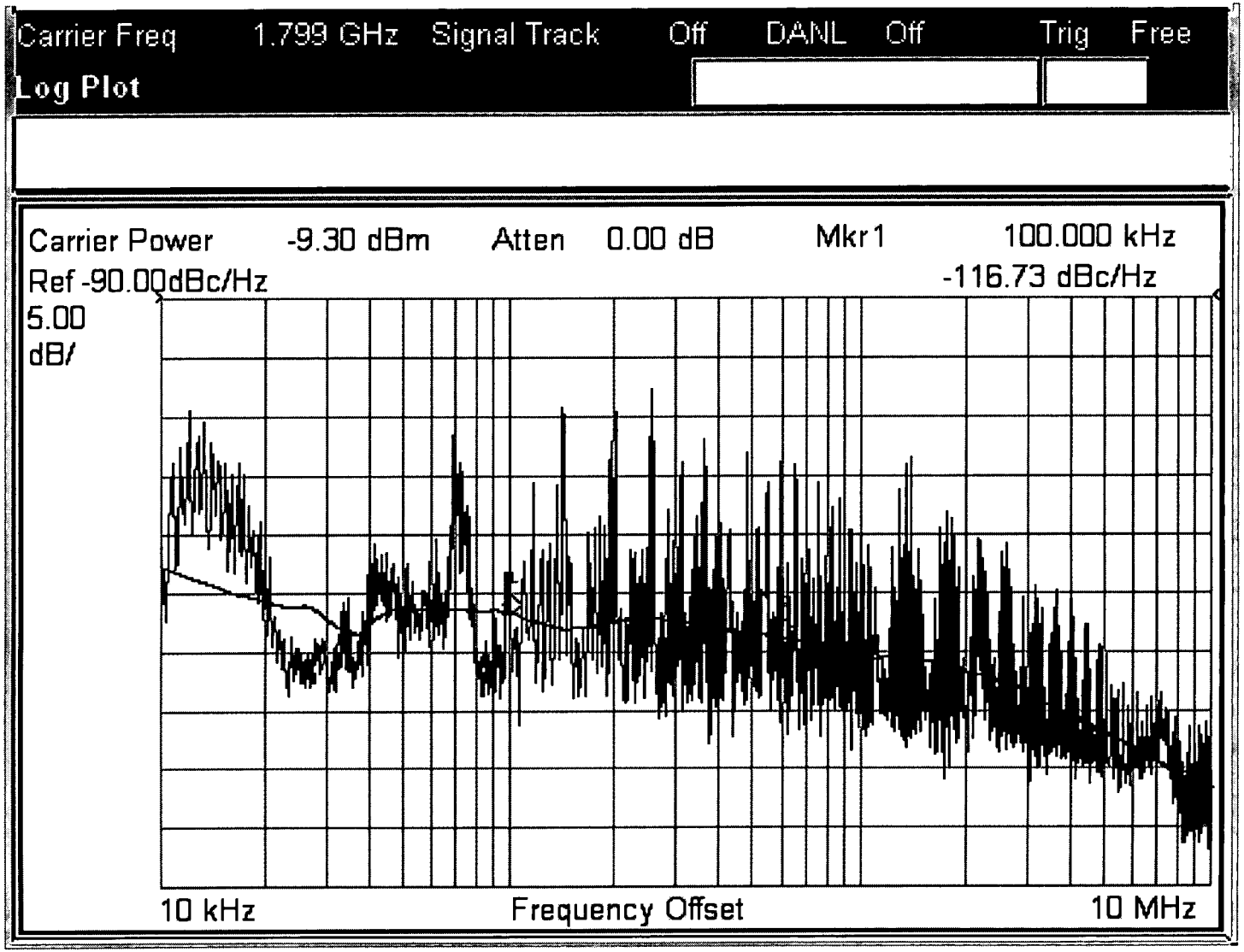


FIG. 25

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1190

Technology And References	Center Frequency (GHz)	Size, mm² and # of metal layers	Power Consumption (mW)	Phase Noise (dBc/Hz) @ offset Freq	Figure of Merit (dB)
LCP	1.80	5 x 5.6, five metal layers plus SMDs	10	-117 @ 100 KHz	192.1
LCP	1.86	6 x 7, Two metal layers plus SMDs	1.8	-103 @ 100 KHz	186.5
LTCC	2.2	12 x 11, >10	39	-120 @ 100 KHz	190.9
Thick Film	1.75	12 x 11, >10	35	-133 @ 100 KHz	202.4
Murata	1.92	5.5 x 4.8, >10	94	-112 @ 60 KHz	183

FIG. 26

EX1002 / Page 398 of 416
Murata Manufacturing Co., Ltd.

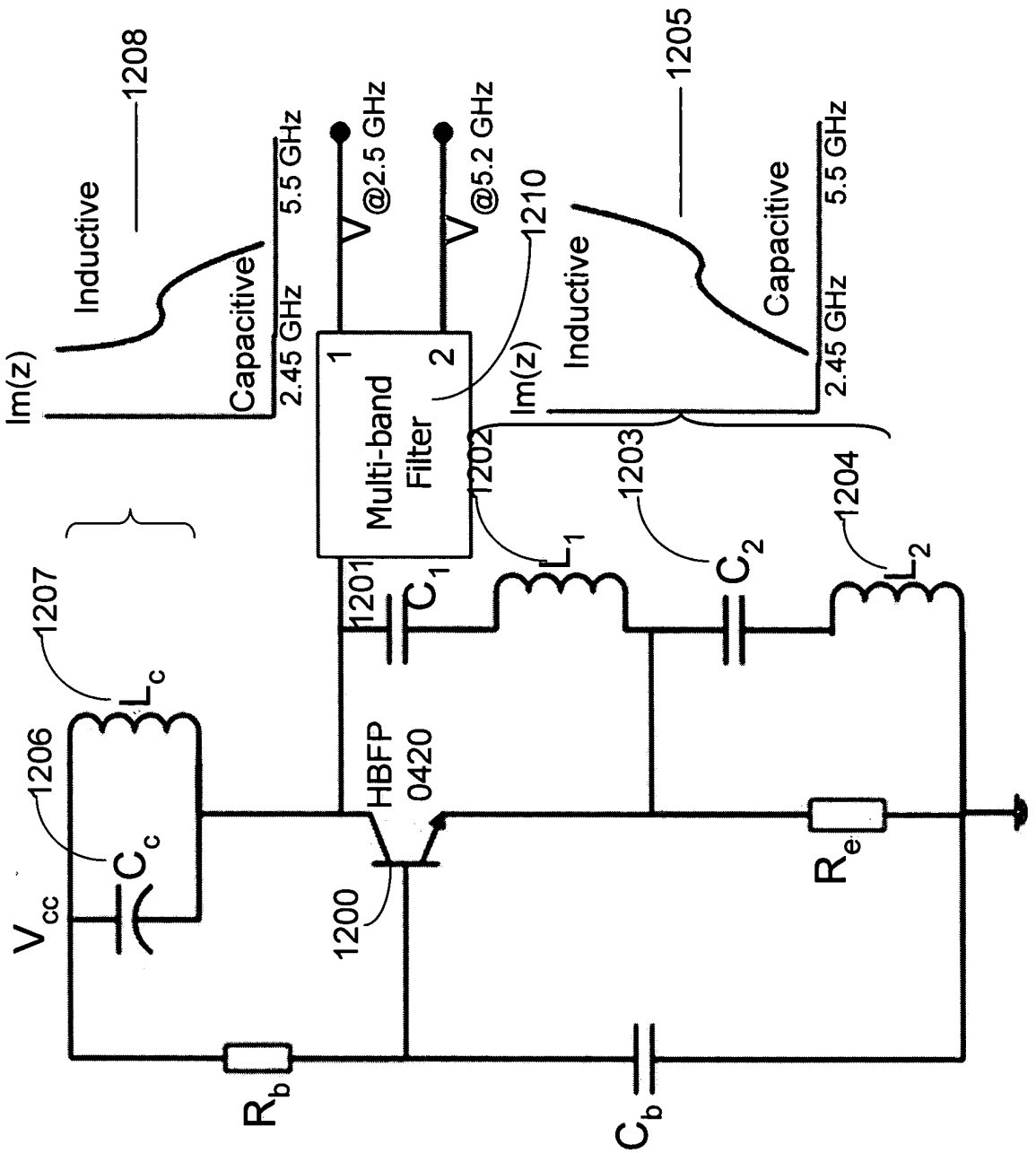

Im(z)
Inductive
1208
Capacitive
2.45 GHz
5.5 GHz
@2.5 GHz
@5.2 GHz
1
2
Multi-band
Filter
1210
1205
Im(z)
Inductive
Capacitive
2.45 GHz
5.5 GHz
1202
1203
1204
1207
1201
L_1
C_1
C_2
L_2
L_c
1206
HBFP
0420
C_c
V_{cc}
1200
R_e
R_b
C_b

FIG. 27

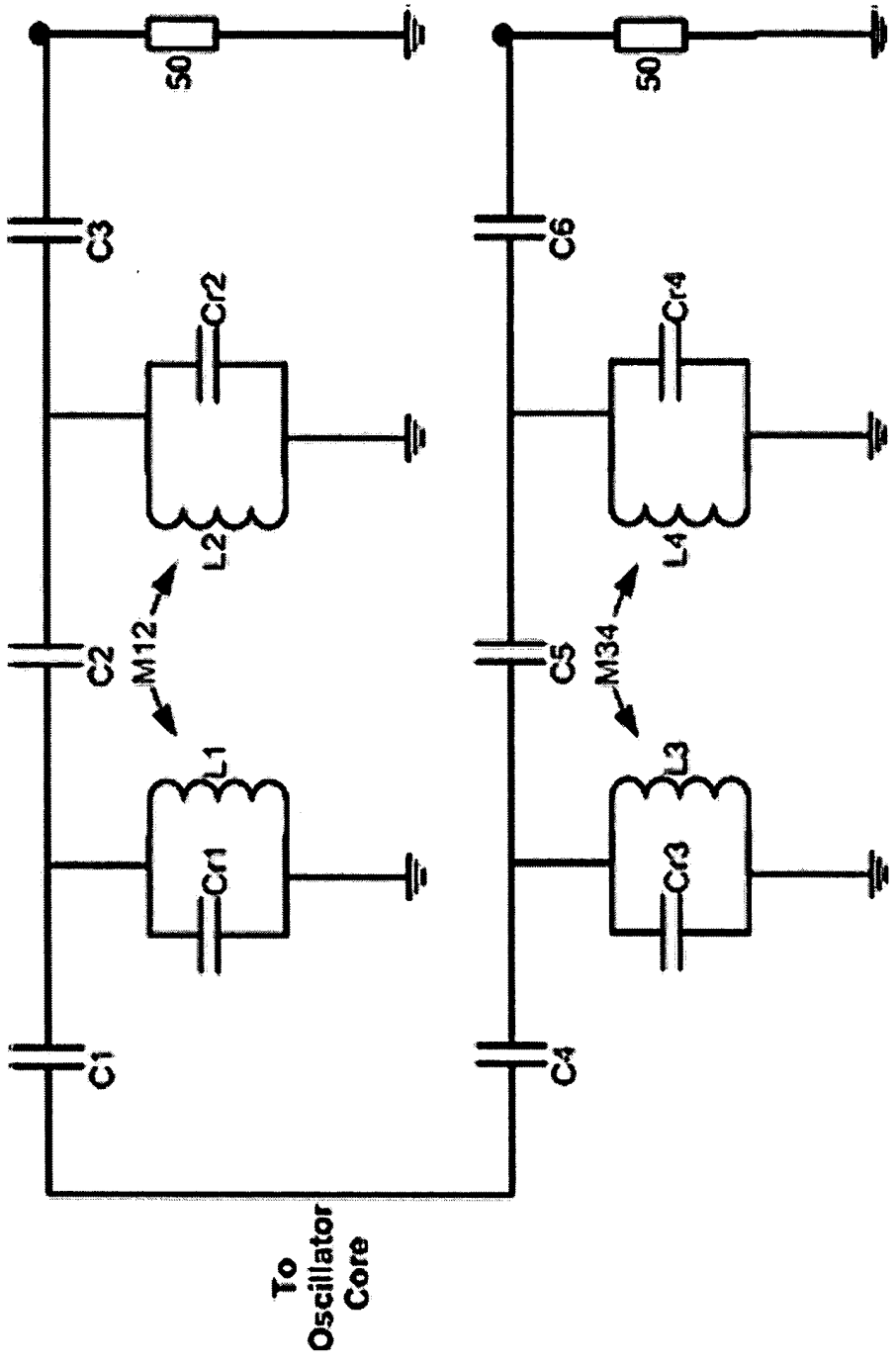

50
50
C3
C6
Cr2
Cr4
L2
L4
M12
M34
C2
C5
L1
L3
Cr1
Cr3
C1
C4
To
Oscillator
Core

FIG. 28

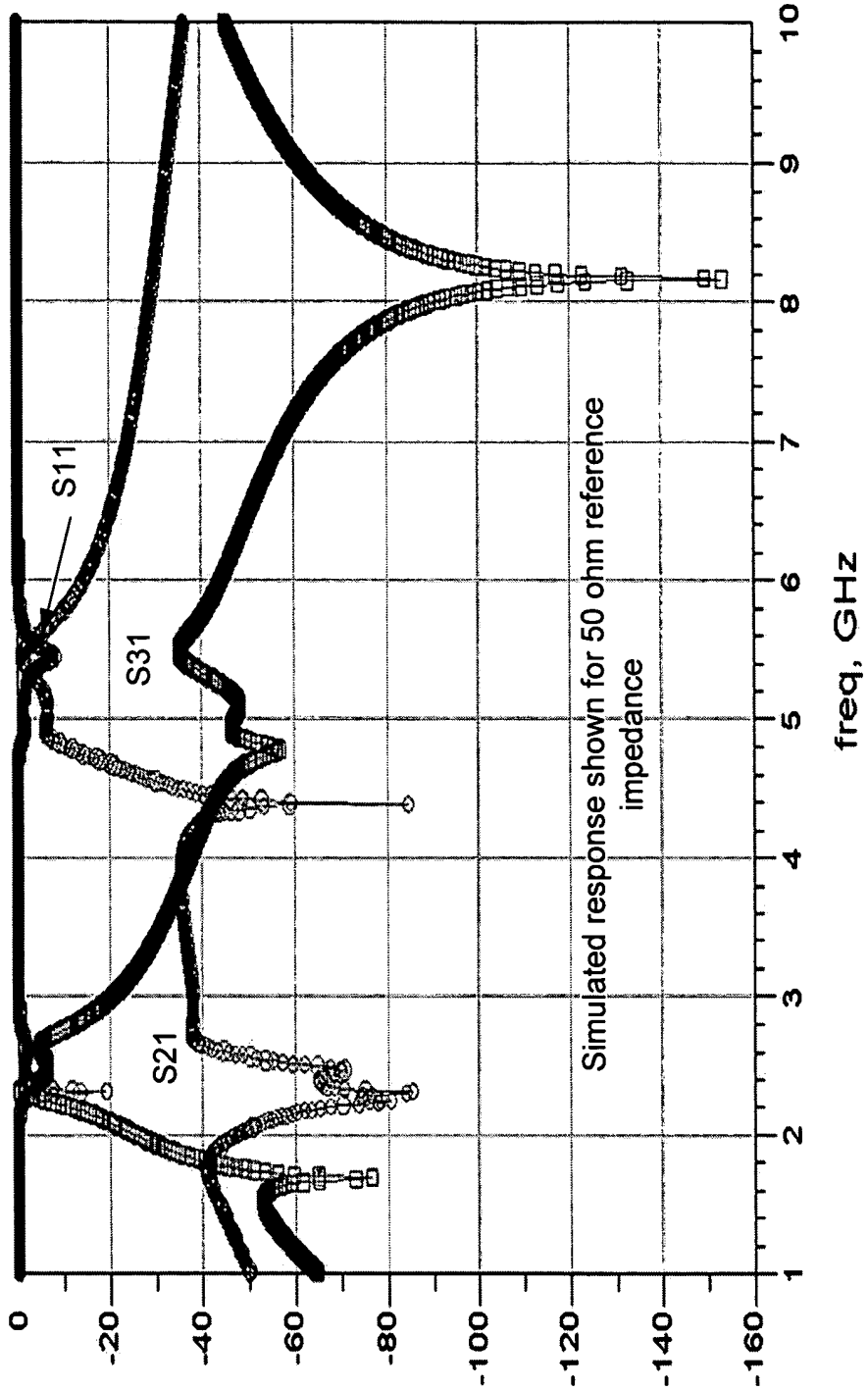

S11
S31
S21
Simulated response shown for 50 ohm reference impedance
freq, GHz
0
-20
-40
-60
-80
-100
-120
-140
-160
1
2
3
4
5
6
7
8
9
10

FIG. 29

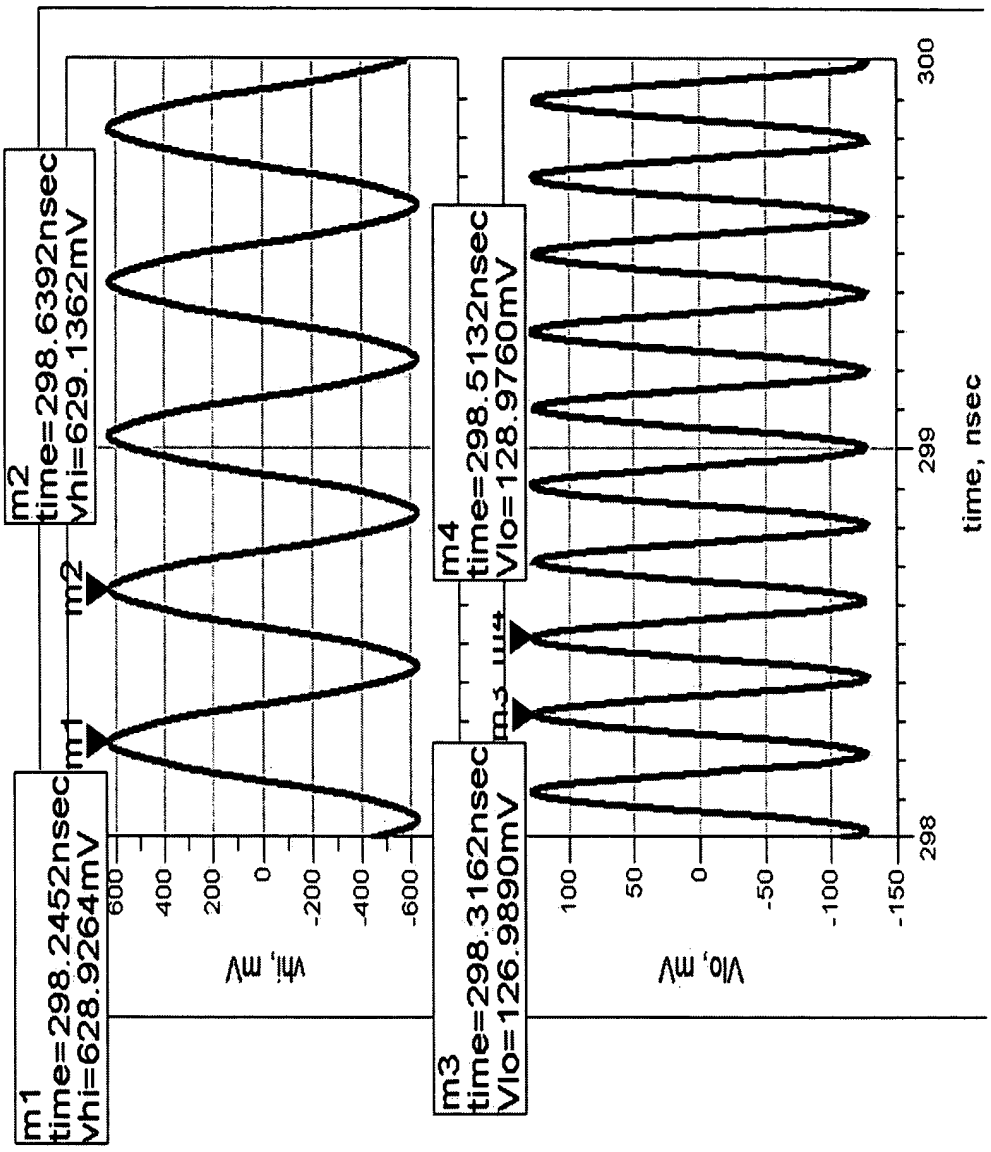

m1
time=298.2452nsec
Vhi=628.9264mV
m2
time=298.6392nsec
Vhi=629.1362mV
m3
time=298.3162nsec
Vlo=126.9890mV
m4
time=298.5132nsec
Vlo=128.9760mV
Vhi, mV
Vlo, mV
time, nsec
600
400
200
0
-200
-400
-600
100
50
0
-50
-100
-150
298
299
300

FIG. 30

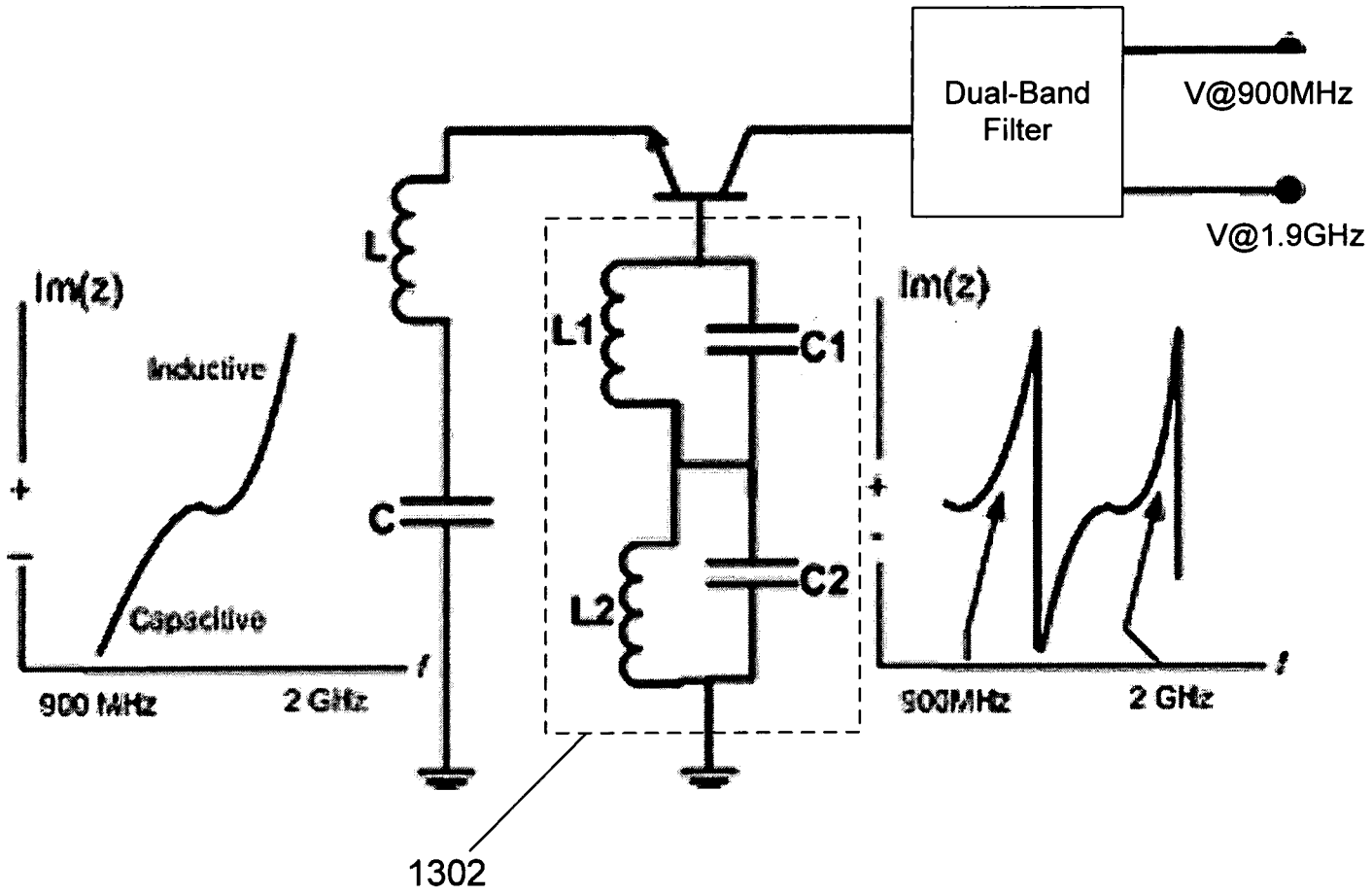


FIG. 31A

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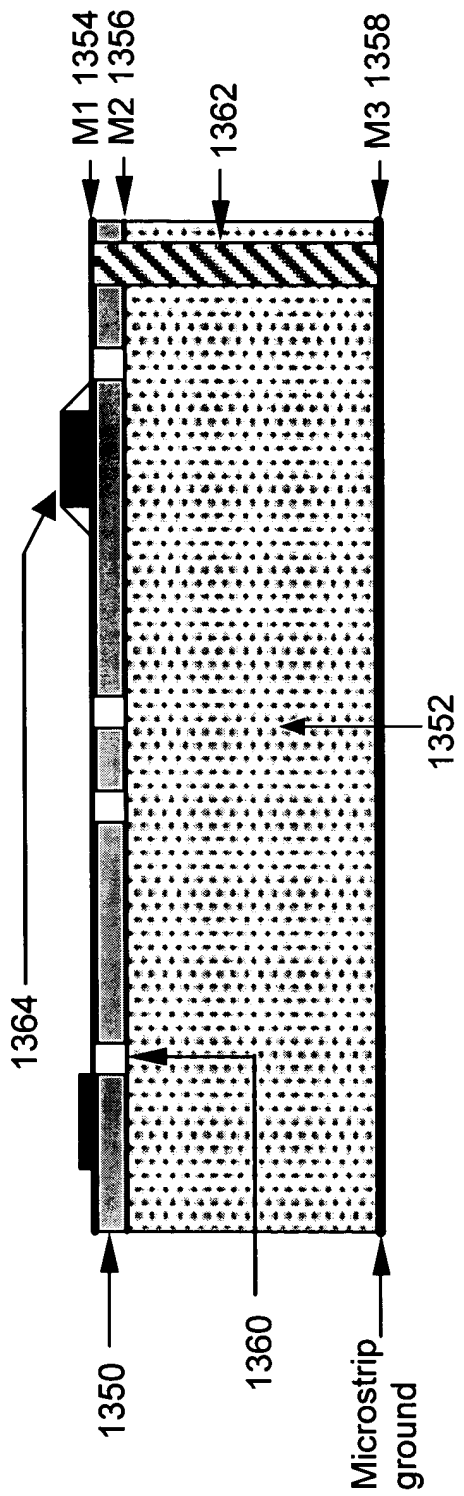

M1 1354
M2 1356
1362
M3 1358
1364
1352
1350
1360
Microstrip ground

FIG. 31B

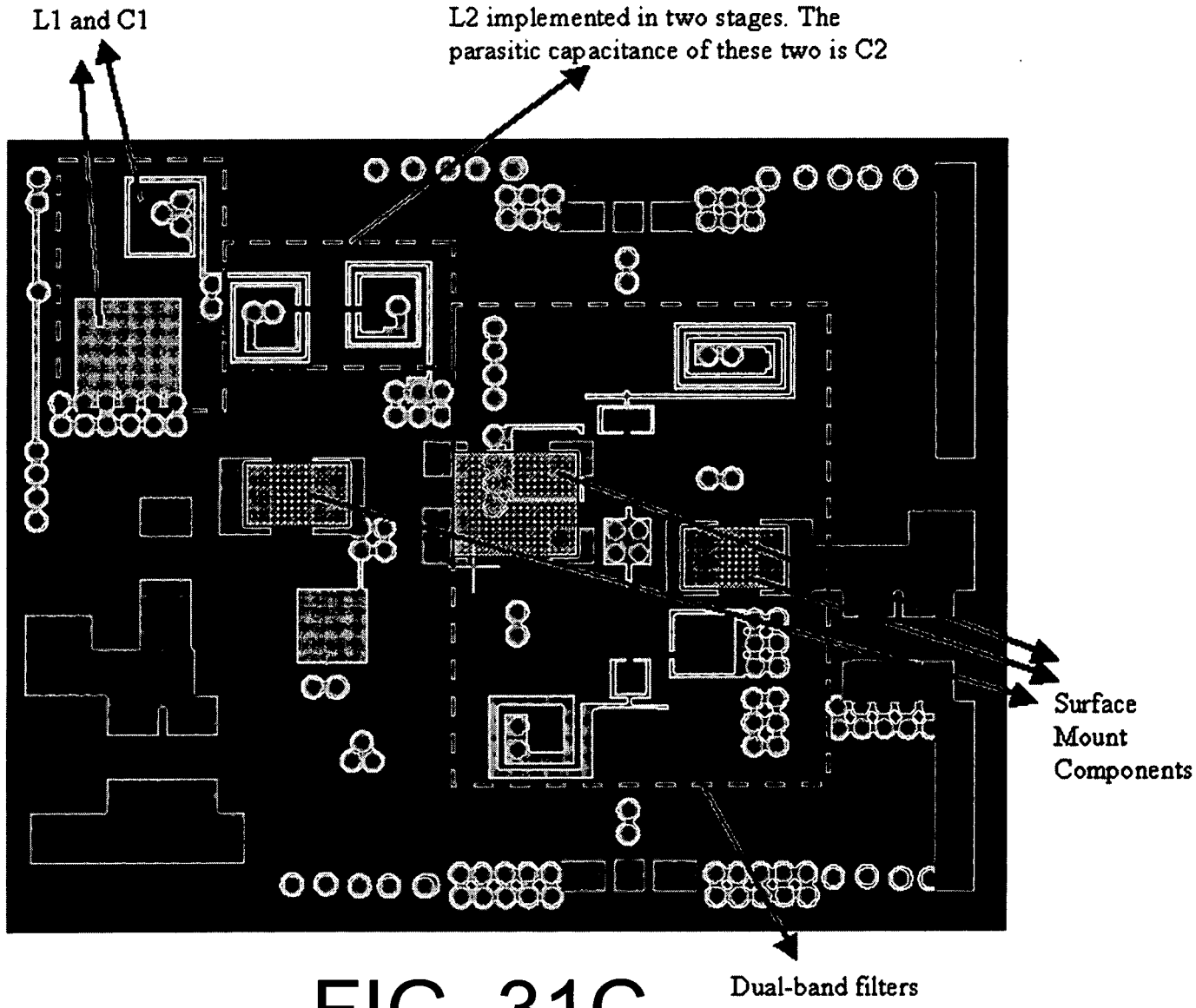


FIG. 31C

BEST AVAILABLE COPY

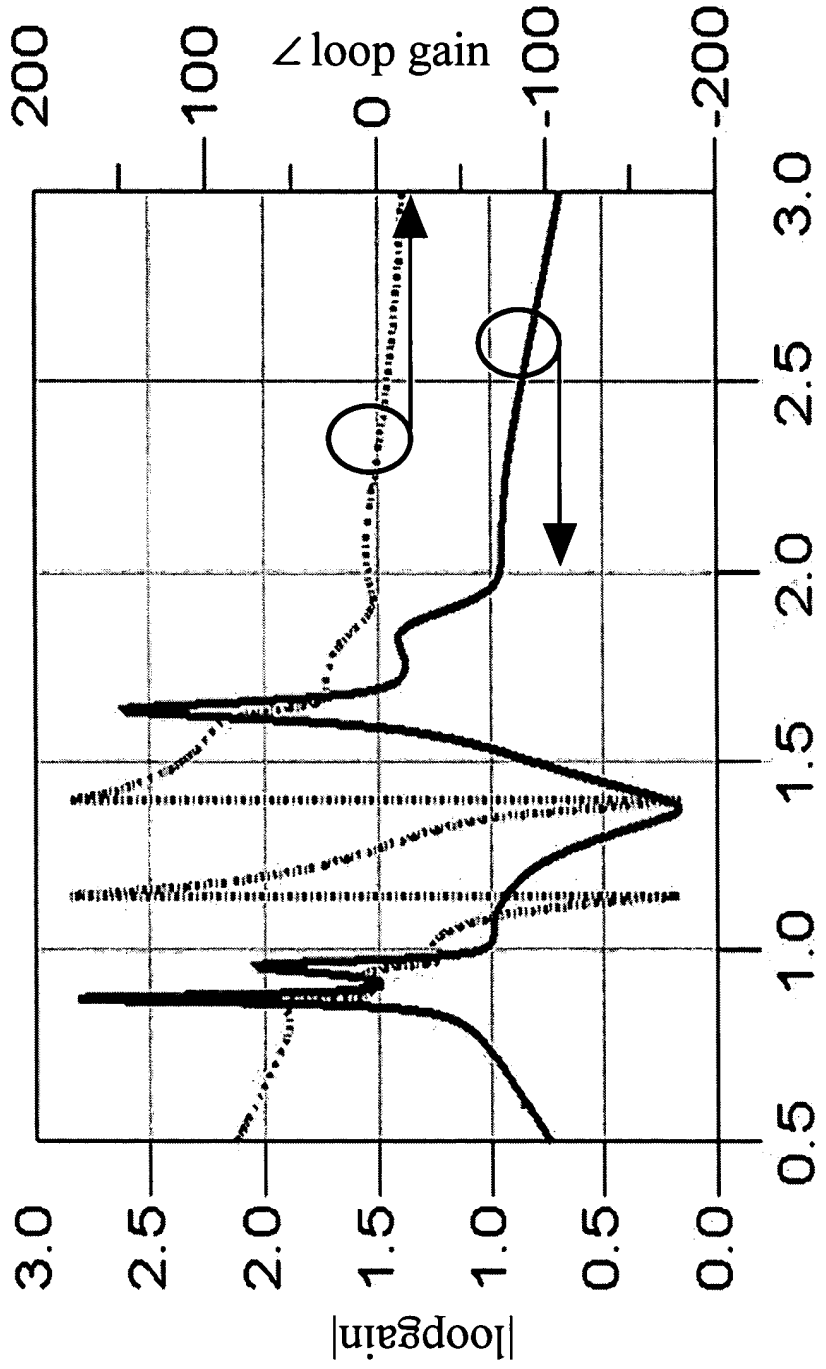

∠loop gain
200
100
0
-100
-200
|loopgain|
3.0
2.5
2.0
1.5
1.0
0.5
0.0
freq, GHz
0.5
1.0
1.5
2.0
2.5
3.0

FIG. 32

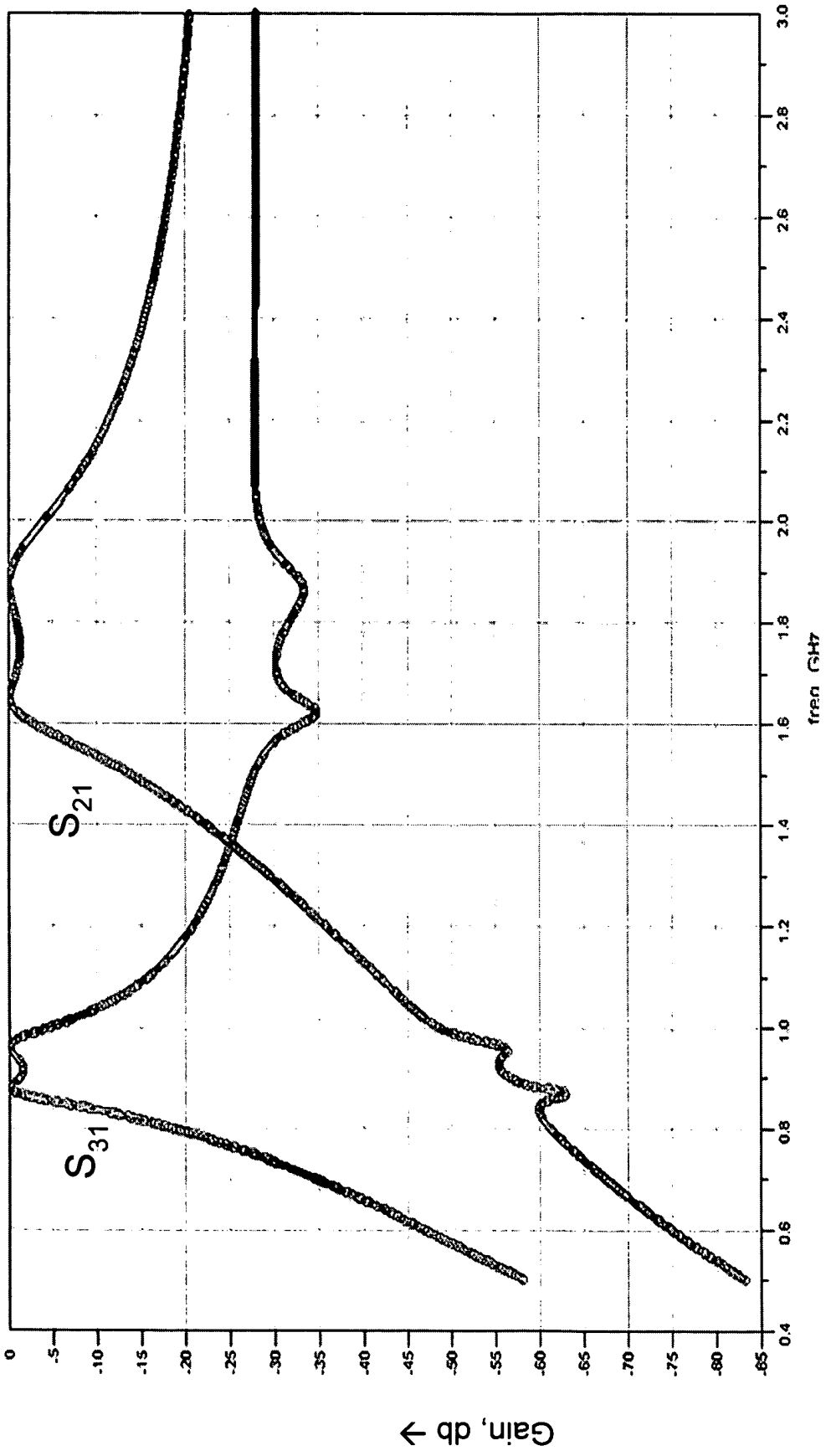


FIG. 33

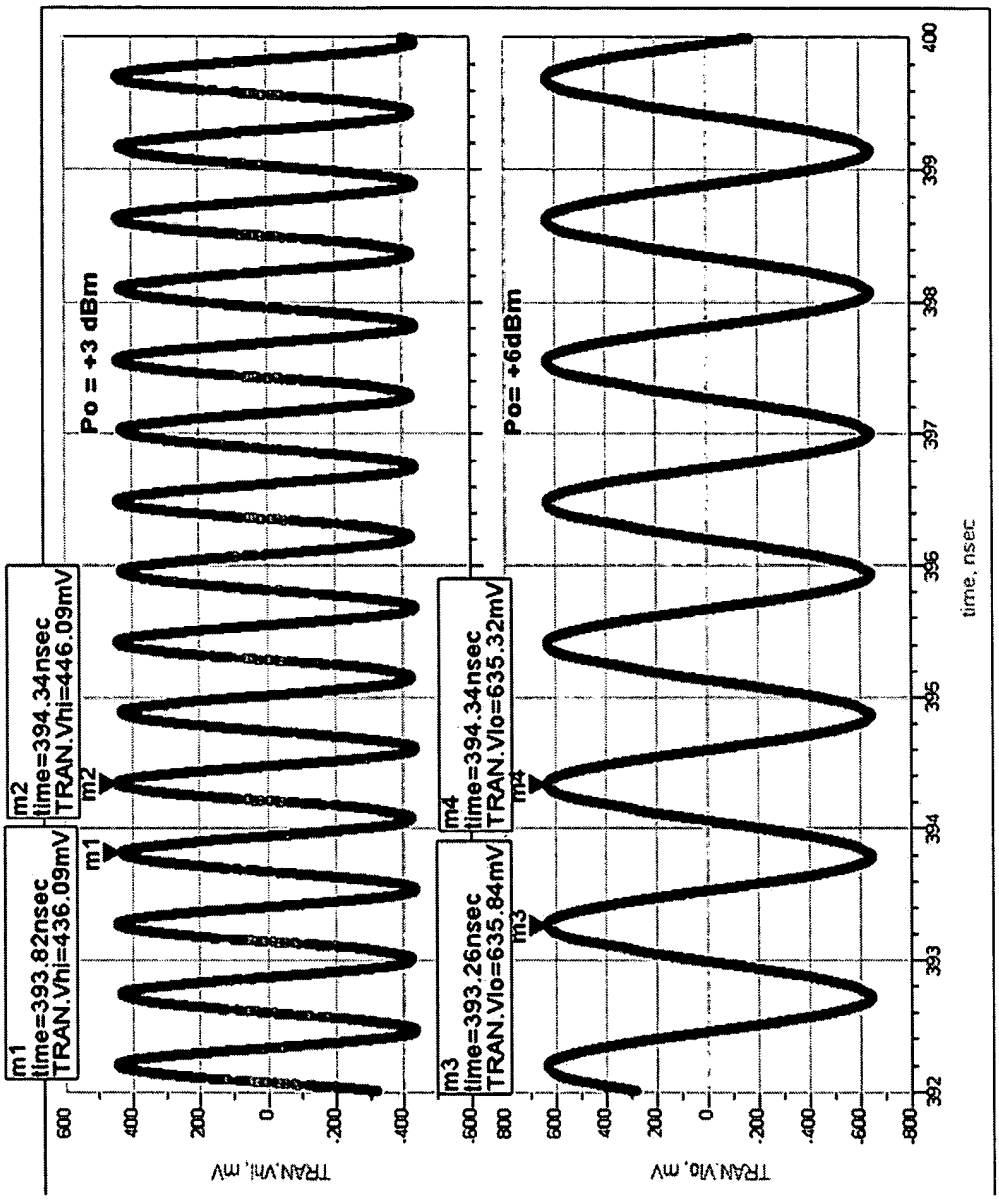

m1
time=393.82nsec
TRAN.Vhi=436.09mV
m2
time=394.34nsec
TRAN.Vhi=446.09mV
m3
time=393.26nsec
TRAN.Vlo=635.84mV
m4
time=394.34nsec
TRAN.Vlo=635.32mV
Po = +3 dBm
Po= +6dBm
TRAN.Vhi, mV
TRAN.Vlo, mV
time, nsec

FIG. 34

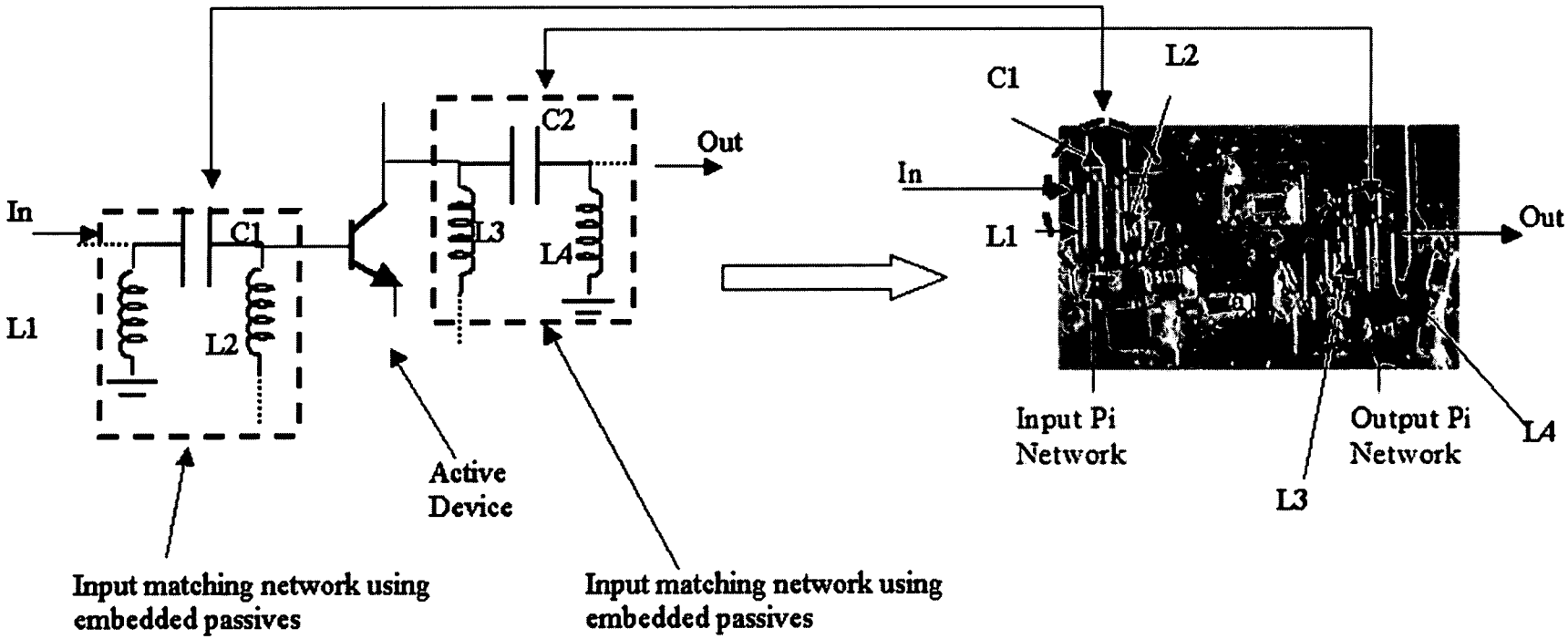


FIG. 35

BEST AVAILABLE COPY

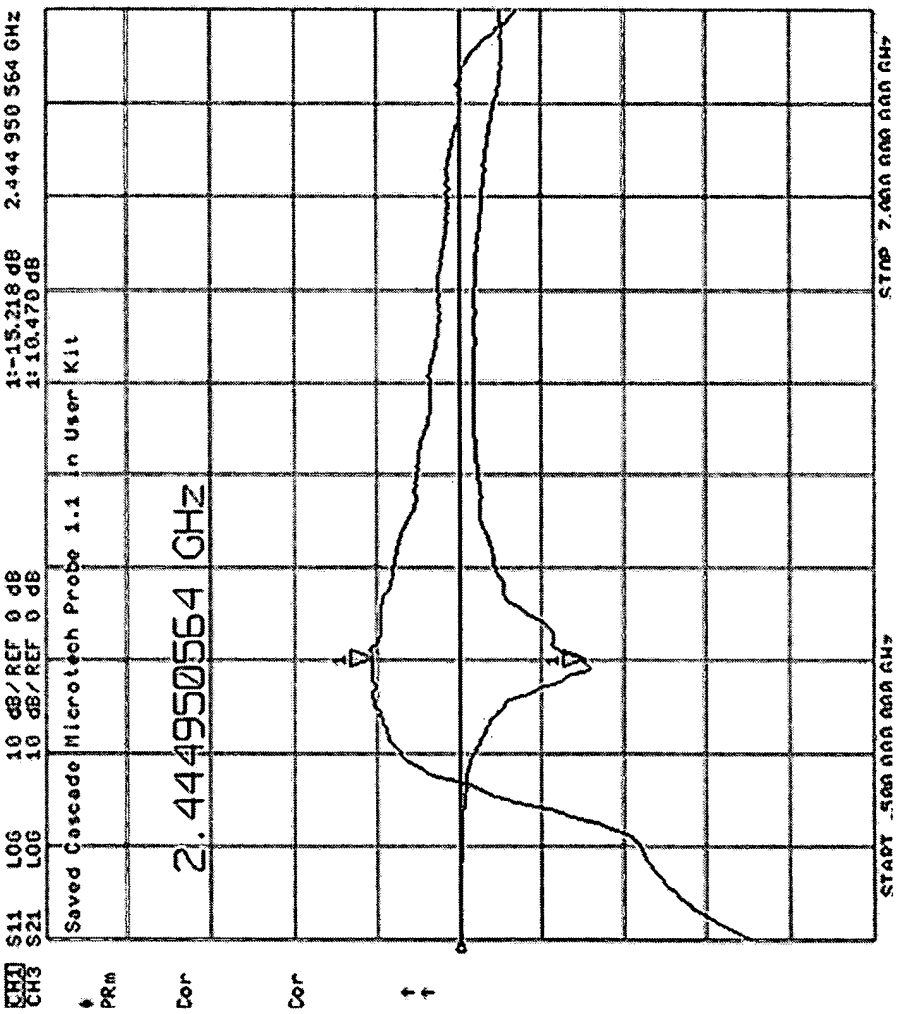

CH1 S11 LOG 10 dB/ REF 0 dB
CH3 S21 LOG 10 dB/ REF 0 dB
1:-15.218 dB 2.444 950 564 GHz
1: 10.470 dB
Saved Cascade Microtech Probe 1.1 in User Kit
2.444950564 GHz
START .500 000 000 GHz
STOP 7.000 000 000 GHz

FIG. 36

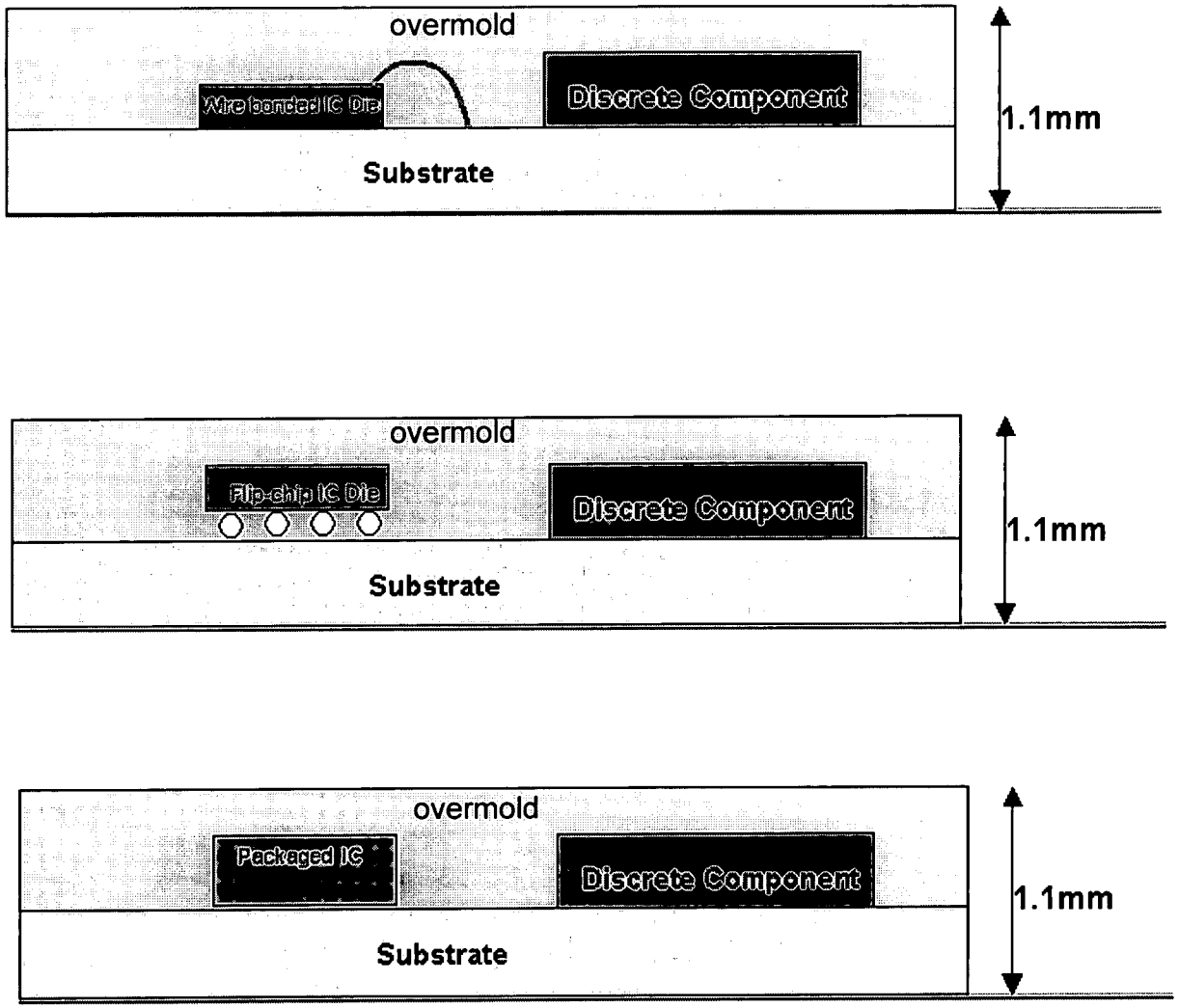


FIG. 37

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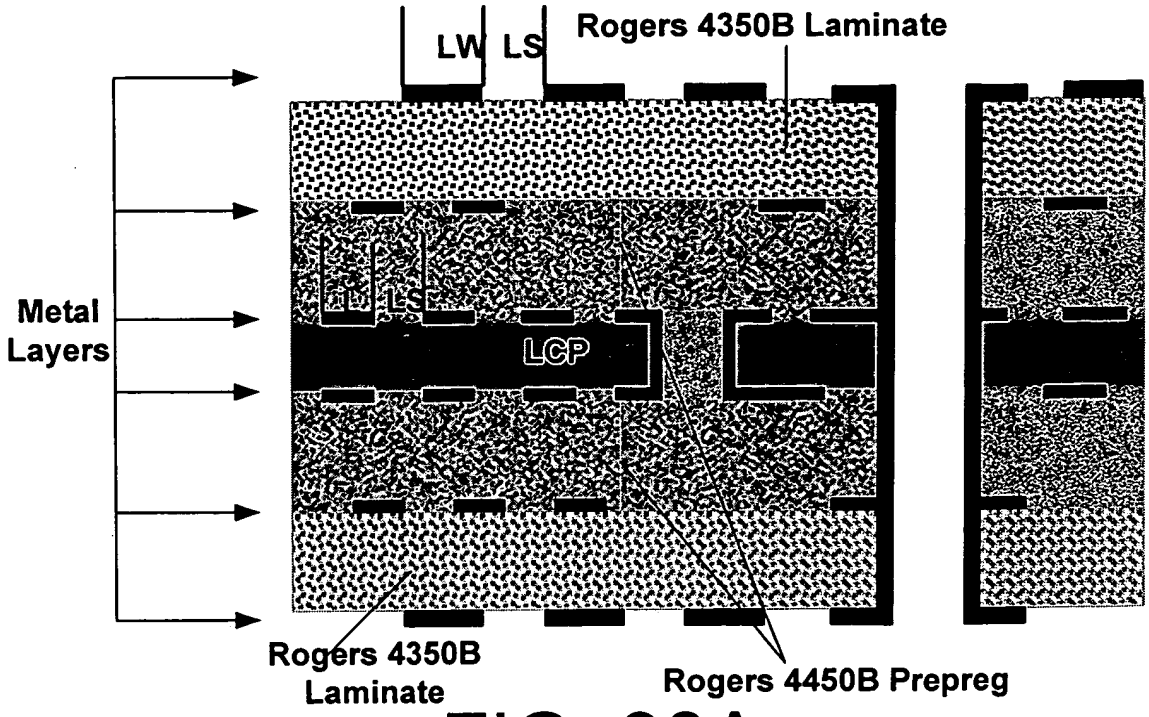


FIG. 38A

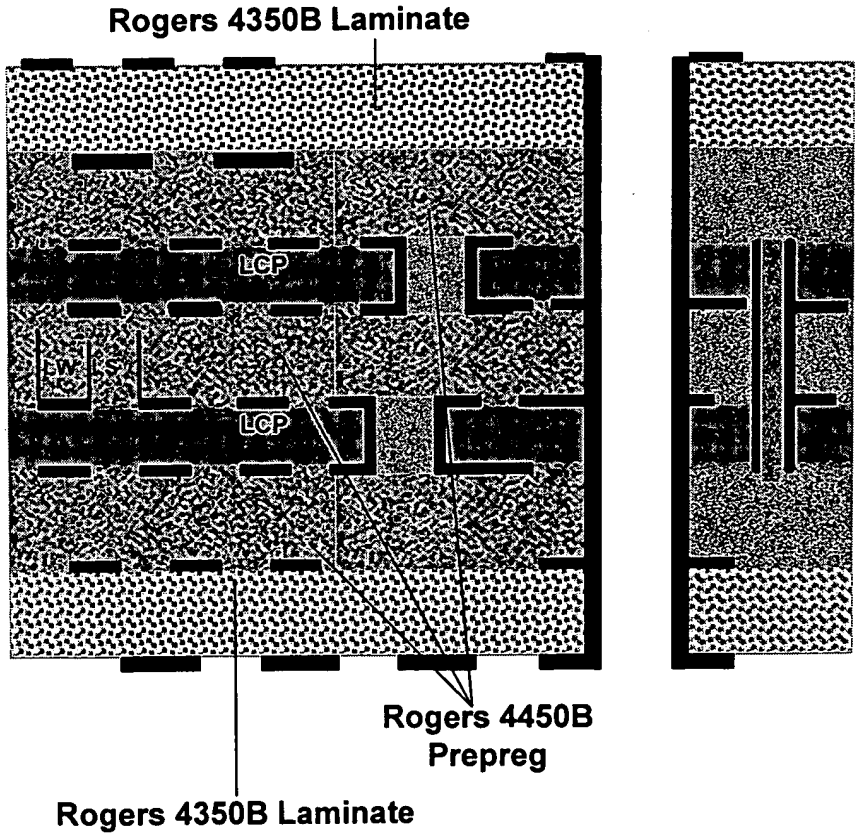


FIG. 38B

BEST AVAILABLE COPY

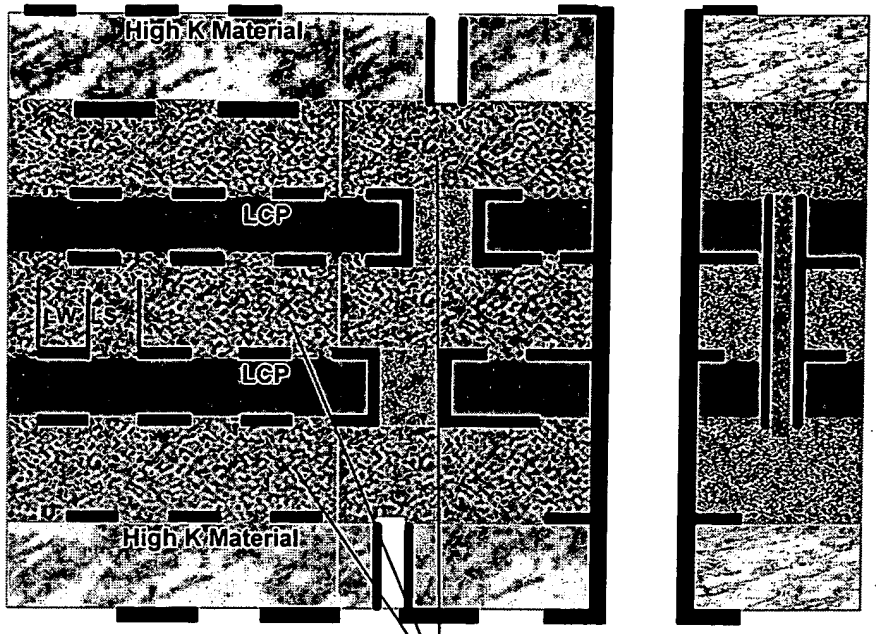


FIG. 38C

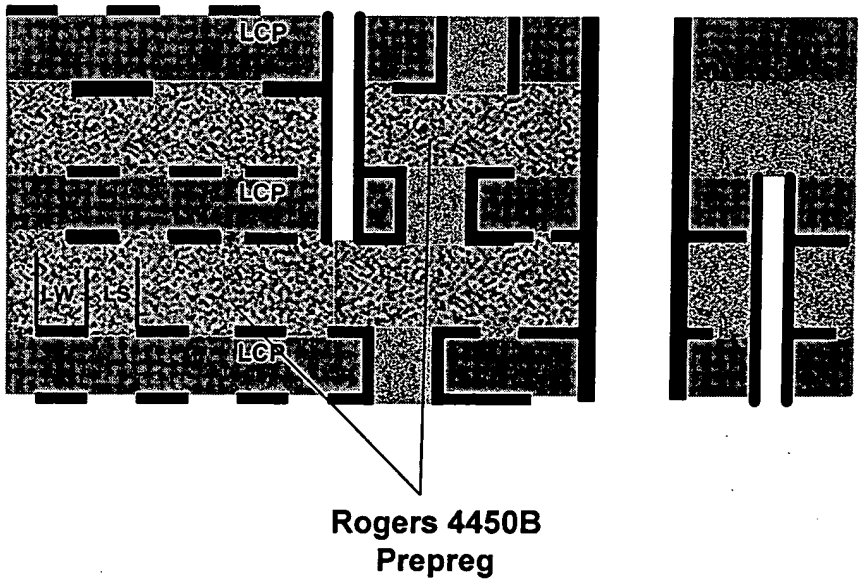


FIG. 38D

BEST AVAILABLE COPY

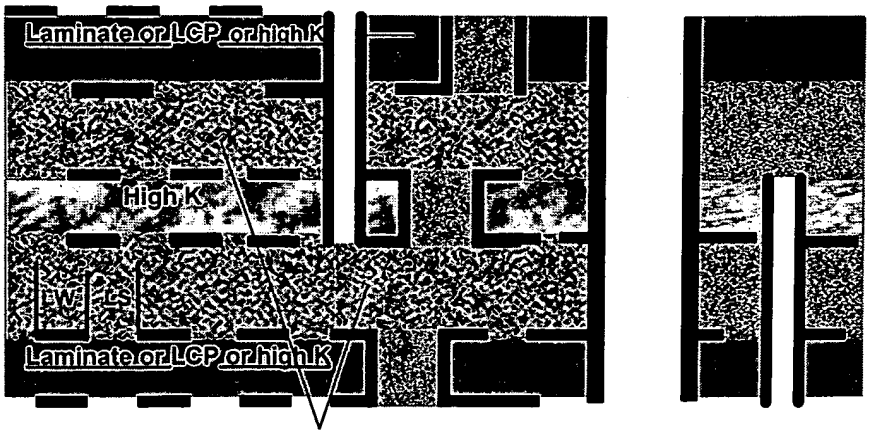


FIG. 38E

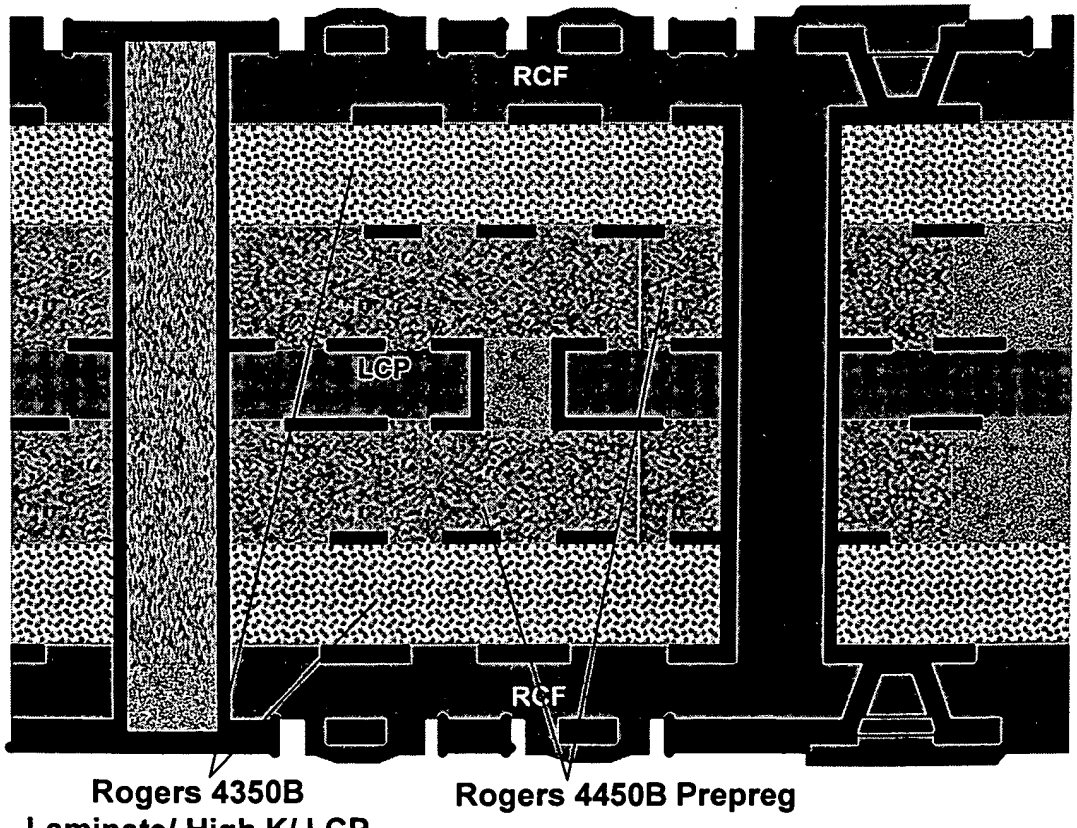


FIG. 38F

BEST AVAILABLE COPY

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

04/28/2005 FFANAEIA 00000023 195029 11114733

01 FC:2011 150.00 DA
02 FC:2111 250.00 DA
03 FC:2311 100.00 DA
04 FC:2201 100.00 DA
05 FC:2202 300.00 DA

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 490-267/69033

PATENT APPLICATION FEE DETERMINATION RECORD
Effective December 8, 2004

11114783

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	32	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	32 minus 20=	* 12
INDEPENDENT CLAIMS	4 minus 3 =	* 1
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	150.00	OR	BASIC FEE	300.00
X$ 25=	300	OR	X$50=	
X100=	100	OR	X200=	
+180=		OR	+360=	
TOTAL	550	OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

1-6-16-22

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 25=		OR	X$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.