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(54) **High frequency module device and method for its preparation**

(57) A high frequency module device of a thin type, high precision and high functions in which the size and the cost of the package may be diminished. The module device includes a base substrate (2) and a high frequency device layer (4). The base substrate (2) is formed by forming a patterned wiring layer (9) on a first major surface (5a) of a core substrate (5) molded of an organic material exhibiting thermal resistance and high frequency characteristics. The uppermost layer of the base substrate (2) is planarized to form a high frequency device layer forming surface (3). The high frequency device layer portion (4) is formed on the high frequency device layer forming surface (3) by a thin film or thick film forming technique and includes intra-layer passive elements, made up of a resistor (27) and a capacitor (26). The passive elements are supplied with power or signals from the side base substrate.

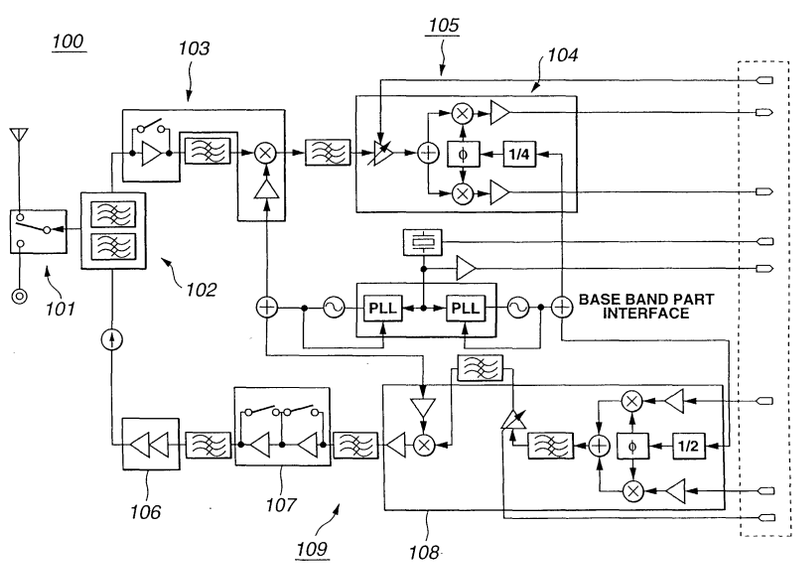

FIG.1

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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates to a high frequency module device and a method for producing the device. Embodiments of this invention relate to a high frequency module device loaded in a variety of electronic equipment, such as personal computers, a portable telephone set or audio equipment to form an ultra-small-sized communication function module having e.g., an information communication function or an information storage function.

Description of Related Art

[0002] The information of various sorts, such as music, speech or pictures, has come to be handled readily by a personal computer or a mobile computer in recent years with the advent of data digitizing technique. Moreover, the above information may be compressed in bands by speech codec or picture codec techniques and has come to be distributed readily and efficiently to a variety of communication terminal equipment by digital communication or digital broadcast. For example, the audio video data (AV data) can be received outdoors by portable telephone sets.

[0003] Meanwhile, as a network system convenient for a small territory, including homes, has now been proposed, variable utilization of transmission/reception systems for e.g., data has become possible. As such network system, a variety of next-generation wireless systems, such as a narrow band radio communication system of the 5 GHz band, as proposed in IEEE 802.1a, radio LAN system of 2.45 band, as proposed in IEEE 802.1b, or the short range radio communication system, termed Bluetooth, are stirring up notice. In a transmission/reception system for e.g., data, such wireless network systems are effectively utilized to exchange a variety of data, to access the Internet or to transmit/receive data in households or outdoors in a handy manner without using e.g., relaying devices.

[0004] Meanwhile, in a communication terminal equipment, it is necessary to modulate/demodulate analog high frequency signals in the transmission/reception unit. So, a high frequency transmission/reception circuit 100 of a superheterodyne system, in which the transmission/reception signals are first converted into signals of an intermediate frequency, as shown in Fig. 1, is routinely used.

[0005] A high frequency transmission/reception circuit 100 includes an antenna unit 10 provided with an antenna or with a changeover switch for transmitting or receiving information signals, and a transmission/reception switching unit 102 for switching between transmission and reception. The high frequency transmission/reception circuit 100 also includes a receipt circuit unit 105 made up e.g., of a frequency conversion circuit unit 103 or with a demodulation circuit unit 104. The high frequency transmission/reception circuit 100 also includes a transmission circuit unit 109 made up e.g., of a power amplifier 106, a driving amplifier 107 and a modulation circuit unit 108. The high frequency transmission/reception circuit 100 also includes a reference frequency generating circuit for supplying a reference frequency to the receipt circuit unit 105 or to the transmission circuit unit 109.

[0006] The high frequency transmission/reception circuit 100 has an extremely large number of component parts, such as large-sized functional components, interposed between respective stages, such as a variety of filters, local oscillators (VCO) or SAW filters, or passive components, such as inductors, resistors or capacitors, proper to the high frequency analog circuits; such as matching circuits or bias circuits. With the high frequency transmission/reception circuit 100, each circuit part is designed as an IC, however, the filter interposed between the respective stages cannot be built into the IC. Moreover, a matching circuit is necessary to provide as an exterior type circuit. Thus, the high frequency transmission/reception circuit 100 is generally bulky in size to present obstacles in reducing the size and weight of the communication terminal equipment.

[0007] On the other hand, a high frequency transmission/reception circuit 110 of the direct conversion system, designed to transmit/receive information signals without conversion into an intermediate frequency, as shown in Fig.2, is also used in the communication terminal equipment. In this high frequency transmission/reception circuit 110, information signals, generated in a source, are directly modulated in a modulation circuit unit 114 to the preset frequency range, without conversion to the intermediate frequency, and transmitted over an antenna 111 through an amplifier 115 and a transmission/reception switching unit 112.

[0008] In such high frequency transmission/reception circuit 110, in which the information signals are transmitted/received by direct detection without conversion of the intermediate frequency of the information signals, the number of component parts, such as filters, is reduced to simplify the overall structure so that expectation may be made of a structure closer to a one-chip structure. However, in the high frequency transmission/reception circuit 110, the filters or matching circuits, arranged on the downstream side, need to be coped with. Moreover, with the high frequency transmission/reception circuit 110, in which the information signals are amplified once and for all in the high frequency stage, it becomes difficult to realize a sufficient gain such that it is necessary to perform amplification in the baseband portion. Thus, the high frequency transmission/reception circuit 110 is in need of a DC offset cancelling circuit or a redundant low-pass filter, while the overall power consumption is increased.

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[0009] In the conventional high frequency transmission/reception circuit, requirements for reduction in size or weight of the communication terminal equipment cannot be met satisfactorily for the superheterodyne system or the direct conversion system. For this reason, a variety of attempts have been made in designing the high frequency transmission/reception circuit as a small-sized module by a simplified structure based on e.g., a Si-CMOS circuit. That is, one of the attempts is to form an active device of high properties on an Si substrate and to build filter circuits or resonators on an LSI as well as to form the logic LSI of the baseband portion as an integrated circuit to produce a so-called one-chip high frequency transmission/reception module.

[0010] However, in such high frequency transmission/reception module, how an inductor of high performance is to be formed on an LSI is crucial. In a high frequency transmission/reception circuit 120, a large-sized recess 124 is formed in register with an inductor forming site 123 of an Si substrate 121 and an SiO_2 insulating layer 122, as shown in Fig.3. In the high frequency transmission/reception circuit 120, a first wiring layer 125 is formed facing the recess 124, while a second wiring layer 126 closing the recess 124 is formed to form an inductor 127. In another type of the high frequency transmission/reception module, the wiring pattern is segmented and raised from the substrate surface to float in air to form an inductor. However, in such high frequency transmission/reception module, the process of forming the inductor is extremely labor-consuming such that the production cost is raised due to the increased number of process steps.

[0011] On the other hand, in a one-chip high frequency transmission/reception module, electrical interference of an Si substrate interposed between the high frequency circuit portion of an analog circuit and a baseband circuit portion of a digital circuit poses a serious problem. As for the high frequency transmission/reception module, an Si substrate high frequency transmission/reception module 130 shown in Fig.4 or a glass substrate high frequency transmission/reception module 140 shown in Fig. 5 has been proposed. In the high frequency transmission/reception module 130, an SiO_2 layer 132 is formed on an Si substrate, after which a passive elements forming layer 133 is formed by a lithographic technique.

[0012] In the passive elements forming layer 133, there are formed passive elements, such as inductors, resistors or capacitors to a multi-layer structure by a thin film forming technique or by a thick film forming technique, along with a wiring pattern, although details are not shown. In the high frequency transmission/reception module 130, a terminal unit connected to an internal wiring pattern is formed on the passive elements forming layer 133 through e.g., a via-hole (relaying through-hole) and a circuit device 134, such as a high frequency IC or LSI, is directly mounted on the passive elements forming layer 133 by e.g., a flip-chip mounting method.

[0013] The high frequency transmission/reception module 130 may be mounted on e.g., a motherboard to isolate the high frequency circuit portion and the baseband circuit portion from each other to suppress electrical interference therebetween. Meanwhile, in such high frequency transmission/reception module 130, there is presented a problem that the electrically conductive Si substrate 131, operating when forming each passive elements in the passive elements forming layer 133, is obstructive for optimum high frequency characteristics of the respective passive elements.

[0014] In a high frequency transmission/reception module 140, a glass substrate 141 is used as a base substrate to overcome the aforementioned problem concerning the Si substrate 131 of the frequency transmission/reception module 130. In the high frequency transmission/reception module 140, a passive elements forming layer 142 is similarly formed on the glass substrate 141 by the lithographic technique. In the passive elements forming layer 142, there are formed passive elements, such as inductors, resistors or capacitors by a thin film forming technique or by a thick film forming technique, to form a multi-layer structure, along with a wiring pattern, although not shown in detail. In the high frequency transmission/reception module 140, a terminal unit connected to an internal wiring pattern is formed on the passive elements forming layer 142, through e.g., a via-hole (relaying through-hole), and a circuit device 133, such as a high frequency IC or LSI, is directly mounted on the passive elements forming layer 133 by e.g., a flip-chip mounting method.

[0015] In the high frequency transmission/reception module 140, employing an electrically non-conductive glass substrate 141, the degree of capacitative coupling across the glass substrate 141 and the passive elements forming layer 142 can be suppressed to form a passive elements exhibiting superior high frequency characteristics within the passive elements forming layer 142. However, in mounting the high frequency transmission/reception module140 on e.g., a motherboard, a terminal pattern is formed on a surface of the passive elements forming layer 142, as shown at 150, and the high frequency transmission/reception module140 then is mounted, such as by wire bonding, to a mother board 151, after which it is connected to the motherboard. So, with the high frequency transmission/reception module 140, a terminal pattern forming step and a wire-bonding step are necessitated.

[0016] In the above-described high frequency transmission/reception module, a highly precise passive elements forming layer is formed on the base substrate, as described above. In forming the passive elements forming layer on the base substrate by a thin film forming technique, the base substrate is required to exhibit thermal resistance against rise in the surface temperature at the time of sputtering, retention of depth of focus at the time of lithography and contact alignment characteristics at the time of masking. So, the base substrate is

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required to exhibit high planarity, insulating properties, thermal resistance properties and resistance against chemicals.

[0017] The Si substrate 131 and the glass substrate 141 exhibit these properties to enable passive elements of low cost and low loss by a process different from the LSI process. Moreover, as compared to the pattern forming method by printing, as used in a conventional ceramic module technique or to the wet etching method used in forming a wiring pattern on a printed wiring board, the Si substrate 131 and the glass substrate 141 permit passive elements to be formed thereon to a high precision, while permitting the device size to be reduced to approximately one-hundredth of that achieved with the above-mentioned conventional methods. In addition, with the Si substrate 131 and the glass substrate 141, the marginal usable frequency band of the passive elements can be raised to 200 GHz by comminution.

[0018] However, in the above-described high frequency transmission/reception module, high frequency signal pattern formation, wiring to supply the power source or the grounding or the wiring of the control signals are made through a wiring layer formed on the Si substrate 131 or on the glass substrate 141. In the high frequency transmission/reception module, electrical interference is produced across respective wirings, while the problem of cost due to forming the wiring layer as a multi-layer wiring is also raised.

[0019] Moreover, the high frequency transmission/reception modules 130, 140 are packaged as shown in Fig.6. On one major surface of an interposer substrate 151 of a package 150 is mounted a high frequency transmission/reception module 130, with the entire assembly being encapsulated in an insulating resin 156. On the front and reverse surfaces of the interposer substrate 151 are formed pattern wiring layers 152, 153, respectively. Around the loading area for the high frequency transmission/ reception module 130 are formed numerous lands 154.

[0020] As the high frequency transmission/reception module 130 is loaded on the interposer substrate 151 of the package 150, this high frequency transmission/ reception module 130 and the lands 154 are electrically connected together by wire bonding 155 to enable power supply or signal transmission/reception. So, there is formed, on a surface layer of the high frequency transmission/reception module 130, having mounted thereon a high frequency IC 134 or a chip component 135, a wiring pattern 136 interconnecting these mounted components and connection terminals 137 to the wire bonding 155. The high frequency transmission/reception module 140 is also packaged in a similar manner.

[0021] Since the high frequency transmission/reception modules 130, 140 are packaged through the interposer substrate 151 as described above, there are presented problems that the package 150 is increased in thickness or size, while the cost of the package is raised.

[0022] In the Si substrate or in the glass substrate high frequency transmission/reception module, a shield cover is provided for overlying the high frequency IC or circuit devices, such as LSIs. However, there is raised a problem that the module becomes bulky depending on the heat radiating structure for the heat generated from these circuit devices. In addition, the production cost tends to be raised due to use of the relatively expensive Si substrate 121 or glass substrate 131.

SUMMARY OF THE INVENTION

[0023] Aspects of the present invention are set out in the claims to which attention is invited.

[0024] An embodiment of the invention seeks to provide a high frequency module device in which a high precision passive elements or a high density wiring layer is formed on a base substrate formed of inexpensive organic resin to improve the function, as well as to reduce the thickness and size and to lower the production cost. One aspect of the present invention seeks to provide a method for the preparation of a high frequency module device.

[0025] The high frequency module device according to an embodiment of the present invention includes a base substrate and a high frequency device layer deposited on this base substrate. The base substrate is made up of a core substrate formed of an organic material exhibiting thermal resistance and high frequency characteristics, and a patterned wiring layer formed on its first major surface. The uppermost layer is flattened out to form a high frequency device layer forming surface. The high frequency device layer, formed on the high frequency device layer forming surface of the base substrate by a thin film forming technique or a thick film forming technique, includes intra-layer passive elements, made up of a resistor, a capacitor or a patterned wiring, supplied with power or signals from the side base substrate through a dielectric insulating layer.

[0026] With the high frequency module device of an embodiment of the present invention, the high frequency device layer is directly formed, by the a thin film forming technique or by the thick film forming technique, on the high frequency device layer forming surface of the base substrate, exhibiting insulating properties and presenting a high precision flattened surface, so that passive elements or wiring layers of high precision and optimum high frequency characteristics may be formed within the bulk of the high frequency device layer. The overall cost of the high frequency device layer may be diminished because the base substrate is formed at a low cost on the core substrate of an inexpensive material in the same way as the conventional multi-layer substrate process. In the high frequency module device, in which the wiring for the power source or the grounding or the wiring of the control system is built in the base substrate and a high frequency signal circuit is formed in the high frequency device layer, electrical isolation may be achieved to suppress electrical interference to

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improve characteristics. With the high frequency module device, in which a power source of a sufficient area and the grounding wiring may be provided on the base substrate, power source supply with high regulation can be achieved.

[0027] An embodiment of the present invention also provides a method for the preparation of a high frequency module device comprised of a base substrate forming step and a high frequency device layer forming step. The base substrate forming step includes a first step of forming a core substrate from an organic material exhibiting thermal resistance and high frequency characteristics, a second step of forming a multi-layer wiring pattern layer on the first major surface of the core substrate and a third step of flattening out the uppermost layer to form a high frequency device layer forming surface. The high frequency device layer forming step includes a step of forming intra-layer passive elements by forming multiple layers comprised of a resistor, a capacitor or a wiring pattern supplied with power or signals from the side base substrate by a thin or thick film forming technique.

[0028] With the method for the preparation of the high frequency module device, according to an embodiment of the present invention, a high frequency device layer is directly formed by a thin or thick film forming technique on a high frequency device layer forming surface, designed as a high precision insulating planar surface, to provide a thin type high precision high frequency module device having high precision passive elements of optimum high frequency characteristics in the layers of the high frequency device layer. With the present method for the preparation of the high frequency module device, the wiring for the power source or the grounding or the wiring for the control system are provided on the base substrate, while a high frequency signal circuit is provided on the high frequency device layer, whereby the base substrate and the high frequency device layer are electrically separated from each other to suppress electrical interference to improve the characteristics of the high frequency module device. With the present method for the preparation of the high frequency module device, a high frequency module device may be produced in which the power source with a sufficient area for the base substrate and the grounding wiring may be formed in the base substrate to assure power supply with high regulation properties.

[0029] According to an embodiment of the present invention, the major surface of the core substrate formed of an insulating inexpensive organic material is flattened out to high precision to form a high frequency device layer forming surface, on which a high frequency device layer formed by a thin or thick film forming technique is directly formed to produce passive elements of high precision exhibiting superior high frequency characteristics by a simplified process. According to an embodiment of the present invention, in which the base substrate may be formed at a low cost by forming a multi-layer wiring layer on the core substrate of an inexpensive material by a process similar to the conventional multi-layer substrate process, a high frequency module device may be produced which is reduced in overall cost. With the present method for the preparation of the high frequency module device, the wiring for the power source or the grounding and the wiring for the control system are provided on the base substrate, while a high frequency signal circuit is provided on the high frequency device layer, whereby the base substrate and the high frequency device layer may be electrically isolated from each other to suppress electrical interference to improve the characteristics of the high frequency module device. According to an embodiment of the present invention, a high frequency module device may be produced in which the power source with a sufficient area for the base substrate and the grounding wiring may be formed in the base substrate to assure power supply with high regulation properties.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] The invention will now be described by way of example with reference to the accompanying drawings, throughout which like parts are referred to by like references, and in which:

Fig. 1 is a structural view of a high frequency transmission/reception circuit by the superheterodyne system.

Fig.2 is a structural view of a high frequency transmission/reception circuit by the direct conversion system.

Figs.3A and 3B illustrate an inductor provided in a conventional high frequency transmission/reception module, where Fig.3A is a perspective view showing essential portions thereof and Fig.3B is a longitudinal cross-sectional view showing essential portions thereof:

Fig.4 is a longitudinal cross-sectional view showing a conventional high frequency transmission/reception module employing a silicon substrate.

Fig.5 is a longitudinal cross-sectional view showing a conventional high frequency transmission/reception module employing a glass substrate.

Fig.6 is a longitudinal cross-sectional view showing a package obtained on mounting a conventional high frequency transmission/reception module on an interposer substrate.

Fig.7 is a longitudinal cross-sectional view showing high frequency transmission/reception module according to an embodiment of the present invention.

Fig.8 illustrates the production process for the high frequency transmission/reception module shown in Fig.7.

Fig.9 is a longitudinal cross-sectional view showing a core substrate employed in the high frequency transmission/reception module shown in Fig.7.

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Fig.10 illustrates a patterning process for a core substrate.

Fig.11 illustrates a process of bonding a copper wire carrying a first resin and another copper wire carrying a second resin.

Fig. 12 illustrates a process of forming a via-hole.

Fig. 13 illustrates a process of forming a first pattern wiring layer and a second pattern wiring layer.

Fig.14 illustrates a process of bonding a copper wire carrying a third resin and another copper wire carrying a fourth resin.

Fig.15 illustrates a process in which the copper wire carrying the third resin and the other copper wire carrying the fourth resin are bonded together.

Fig.16 illustrates a process of polishing the copper wire carrying the third resin and the other copper wire carrying the fourth resin.

Fig.17 illustrates a process of forming a process of forming the first resin layer.

Fig.18 illustrates a process of forming a wiring layer.

Fig.19 illustrates a process of forming a passive elements.

Fig.20 illustrates a process of forming the second resin layer.

Fig.21 illustrates a process of forming the wiring layer.

Fig.22 illustrates a process of forming a resist layer.

Fig.23 is a longitudinal cross-sectional view of a high frequency module device.

Figs.24A-24F illustrate another process of forming a base substrate.

Figs.25A-25D illustrate a process of producing a base substrate by a dip coating method.

Fig.26 is a longitudinal cross-sectional view of a high frequency module device having a heat radiating structure.

Fig.27 is a longitudinal cross-sectional view of a high frequency module device having another heat radiating structure.

Fig.28 is a longitudinal cross-sectional view of a high frequency module device having yet another heat radiating structure.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0031] Referring to the drawings, preferred embodiments of the present invention will be explained in detail. In a high frequency module device 1, shown as an embodiment in Fig.7, a base substrate 2, the uppermost layer of which is formed as a high frequency device layer forming surface 3 of high planarity, is prepared by a base substrate producing step which will be explained subsequently. Using this base substrate 2 as a base, a high frequency device layer portion 4 is formed on the high frequency device layer forming surface 3 by a high frequency device layer forming step which will also be explained subsequently. In the high frequency module device 1, the base substrate 2 forms a wiring portion of a power source system for the high frequency device layer portion 4 formed as an upper layer, while also forming a wiring portion for the control system or a ground surface. On the upper surface of the high frequency device layer portion 4 of the high frequency module device 1, a high frequency IC 90 or a chip component 91 is mounted on an upper surface of the high frequency device layer portion 4, and a shield cover 92 is applied for sealing, as shown in Fig.7. The high frequency module device 1 is mounted as a so-called one-chip component on a motherboard 93.

[0032] The base substrate 2 is made up of a core substrate 5, comprised of a double-sided substrate, a first pattern wiring layer 6, formed on one major surface 5a of the core substrate 5, as a core, and a second pattern wiring layer 7, formed on the other major surface of the core substrate 5. On the core substrate 5 of the base substrate 2 are bonded first to fourth resin coated copper foils 8 to 11, as will be explained subsequently. The first resin-coated copper foil 8 is bonded to the first major surface 5a of the core substrate 5 to form the two-layered first pattern wiring layer 6 along with the core substrate 5. The second resin-coated copper foil 9 is bonded to the second major surface 5b of the core substrate 5 to form the two-layered second pattern wiring layer 7 along with the core substrate 5.

[0033] The structure and the process for the preparation of the base substrate 2 are now explained in detail with reference to manufacture process diagrams of Figs. 8 to 16. Referring to Fig.8, the manufacture process for the base substrate 2 includes a first pattern wiring layer forming process s-1 for forming a first pattern wiring layer 12 and a second pattern wiring layer 13 on front and reverse major surfaces 5a, 5b of the core substrate 5, and for forming plural via-holes 14 therein, a first copper foil bonding process s-2 for bonding the first resin-coated copper foil 8 and the second resin-coated copper foil 9 to the front and reverse major surfaces 5a, 5b of the core substrate 5, and a via-forming process s-3 of forming via-holes 15, 16 in these resin-coated copper foils 8, 9. In the manufacture process of the base substrate 2, a base substrate intermediate product 19 is prepared through the above processes and a second pattern wiring layer forming process s-4 of forming a third pattern wiring layer 17 and a fourth pattern wiring layer 18 on the so bonded resin-coated copper foils 8, 9.

[0034] The manufacture process for the base substrate 2 includes a second copper foil bonding process a-5 of bonding a third resin-coated copper foil 10 and a fourth resincoated copper foil 11 on the base substrate intermediate product 19 for coating the third pattern wiring layer 17 and the fourth pattern wiring layer 18. In the manufacture process for the base substrate 2, the base substrate 2 is prepared through a polishing step s-6 of polishing the third resin-coated copper foil 10 and the fourth resin-coated copper foil 11 to form the high frequency device layer forming surface 3 as the uppermost

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layer on the side major surface 5a.

[0035] The core substrate 5 is comprised of a substrate material of low dielectric constant and low tanδ, that is of superior high frequency characteristics, such as polyphenylethylene (PPE), bis maleido triazine (BT-resin), polytetrafluoroethylene (trade mark: Teflon), polyimide, liquid crystal polymer (LCP), polynorbornene (PNB), ceramics or a mixture of ceramics with an organic substrate. As the core substrate 5, an epoxy-based substrate FR-5, having thermal resistance and resistance to chemicals, in addition to mechanical strength, and which is less costly than the aforementioned substrates, is also used. The core substrate 5, formed by the aforementioned substrate, is less costly than the Si substrate or the glass substrate which is rather expensive due to its characteristic high precision, thereby reducing the materials cost.

[0036] The first and second major surfaces 5a, 5b of the core substrate 5 are lined in their entirety with copper foil layers 20a, 20b, as shown in Fig.9. The core substrate 5 is subjected to the first pattern wiring layer forming process s-1. The core substrate 5 is subjected to a punching processing by a drill or laser to form via-holes 14 at preset positions. After burying an electrically conductive paste in the via-holes 14 of the core substrate 5, the inner wall surfaces of which are rendered electrically conductive by e.g., plating, a lid is formed by a plating method. The copper foil layers 20a, 20b of the core substrate 5 are subjected to photolithographic processing to form the first pattern wiring layer 12 and the second pattern wiring layer 13 on the first and second major surfaces 5a, 5b, as shown in Fig.10.

[0037] The first and second pattern wiring layers 12, 13 then are applied to the core substrate 5 from the above process, by the first copper foil bonding process s-2, to affix the first and second resin-coated copper foils 8, 9 to the first and second major surfaces 5a, 5b, as shown in Fig.11. As the first and second resin-coated copper foils 8, 9, resin-coated copper foils, obtained on lining resin layers 8b, 9b on one major surfaces of copper foil layers 8a, 9a in their entirety, are used.

[0038] The first and second resin-coated copper foils 8, 9 are bonded to the first and second major surfaces 5a, 5b of the core substrate 5, using a bonding resin (pre-preg), with the resin layers 8b, 9b as bonding surfaces. If the resin layers 8b, 9b are formed of thermoplastic resins, the first and second resin-coated copper foils 8, 9 are bonded to the core substrate 5, with the bonding resin being then unnecessary. With the first and second resin-coated copper foils 8, 9 remaining bonded to the core substrate 5, the first and second resin-coated copper foils 8, 9 are subjected to the via-forming process s-3. Thus, the sites thereof in register with the via-holes 14 to be formed are subjected to the photolithographic processing to form via-holes 15, 16. In the via-forming process s-3, the sites of the first and second resin-coated copper foils 8, 9, in which to form via-holes, are subjected to the photolithographic processing followed by wet etching to form openings 22a, 22b in the first and second resin-coated copper foils 8, 9, and laser processing then is carried out with these openings 22a, 22b as masks to form the via-holes 15, 16, with the land of the first pattern wiring layer 12 or the second pattern wiring layer 13 serving as supports.

[0039] The inner wall surfaces of the via-holes 15, 16 of the first and second resin-coated copper foils 8, 9 are rendered electrically conductive by e.g., via-hole plating. These via-holes 15, 16 are charged with electrically conductive materials 23a, 23b by embedding an electrically conductive paste or a plating method. By the second pattern wiring layer forming process s-4, the copper foil layers 8a, 9a of the first and second resin-coated copper foils 8, 9 are patterned in a preset fashion to form the third pattern wiring layer 17 and the fourth pattern wiring layer 18, as shown in Fig.13. Similarly to the first pattern wiring layer forming process s-1, the second pattern wiring layer forming process s-4 performs photolithographic processing on the copper foil layers 8a, 9a to form the third pattern wiring layer 17 and the fourth pattern wiring layer 18 on the resin layers 8b, 9b to form the base substrate intermediate product 19.

[0040] In the base substrate forming process, the high frequency device layer forming surface 3 exhibiting high planarity is formed on the base substrate intermediate product 19, in order to form the high frequency device layer portion 4, as later explained, on the base substrate intennediate product 19. By a second copper foil bonding process s-5, the base substrate intermediate product 19 is coated with the third pattern wiring layer 17 and the fourth pattern wiring layer 18 as shown in Fig.14 to bond the third resin-coated copper foil 10 and the fourth resin-coated copper foil 11 to the front and reverse major surfaces 5a, 5b, respectively.

[0041] Similarly to the aforementioned first and second resin-coated copper foils 8, 9, the third resin-coated copper foil 10 and the fourth resin-coated copper foil 11 are fonned by having one entire major surfaces of copper foil layers 10a, 11a lined with resin layers 10b, 1 1b, respectively. The third resin-coated copper foil 10 fourth resin-coated copper foil 11 are bonded with a prepreg (bond resin) on the front and reverse major surfaces ofthe base substrate intermediate product 19, with the resin layers 10b, 11b as the bond surfaces, as shown in Fig.15. If the resin layers 10b, 11b are formed by thermoplastic resins, the third resin-coated copper foil 10 fourth resin-coated copper foil 11 are bonded to the base substrate intermediate product 19, with the bond resin being then unnecessary.

[0042] The third resin-coated copper foil 10 and the fourth resin-coated copper foil 11, bonded to the base substrate intermediate product 19, are polished by a polishing process s-6. In this polishing process s-6, the entire surfaces of the third and fourth resin-coated copper foil 10, 11 are polished with a grinding liquid mixture composed of, for example, alumina and silica, to polish both sides of the base substrate intermediate product

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19 into highly planar surfaces. In the polishing process s-6, the side third resin-coated copper foil 10, in other words, the high frequency device layer forming surface 3, is polished until the third pattern wiring layer 17 is exposed, as shown in Fig.16. Moreover, in the polishing process s-6, the side fourth resin-coated copper foil 11 is polished so that the resin layer 1 1b has a preset thickness Δx, without allowing the fourth pattern wiring layer 18 to be exposed.

[0043] In the base substrate forming process, a base substrate 2, carrying the high frequency device layer forming surface 3 exhibiting the optimum precision planarity, is formed by the above process steps from the stage of the core substrate 5 through the stage of the base substrate intermediate product 19. In the base substrate forming process, the process of forming the base substrate intermediate product 19 similar to the manufacture process for the conventional multi-layered substrate is used to enable the manufacture process for the preparation of the multi-layered substrate may directly be applied, as high mass-producibility is kept. It should be noted that the manufacture process for the base substrate is not limited to the above process such that a variety of manufacture processes for the multi-layered substrate may be used.

[0044] On the base substrate 2, the second pattern wiring layer 13 is formed by the second resin-coated copper foil 9 bonded to the second major surface 5b of the core substrate 5, as described above. In the base substrate 2, this second pattern wiring layer 13 is not exposed by limiting the polishing amounts of the resin layer 1 1b of the fourth resin-coated copper foil 11. By this configuration, the second pattern wiring layer 13 of the base substrate 2 is protected against chemicals, mechanical load or thermal load by the resin layer 11b (dielectric layer), which is left over, in the high frequency device layer forming processing, which will be explained subsequently. After forming the high frequency device layer portion 4, the resin layer 11b is removed by cutting to expose the second pattern wiring layer 13 to form an input/output terminal 24.

[0045] On the base substrate 2, prepared as described above, the high frequency device layer portion 4 is layered on the high frequency device layer forming surface 3, through a high frequency device layer forming process, which will be explained subsequently. The high frequency device layer portion 4 is comprised of the high frequency device layer forming surface 3 of the planarized base substrate 2 on which are formed a device forming layer portion 28 and a wiring layer portion 29. The device forming layer portion 28 has enclosed therein passive elements, such as an inductor 25, a capacitor 26 or a resistor 27, produced using a thin film forming technique or a thick film forming technique. The high frequency device layer portion 4, on the wiring layer portion 29 of which a high frequency IC 90 or a chip component 91 is mounted, is coated in its entirety with a shield cover 92.

[0046] Meanwhile, in the base substrate forming process, the fourth resin-coated copper foil 11 bonded to the base substrate 5 via second resin-coated copper foil 9 polishes the copper foil layer 11a. In the base substrate forming process, the respective components, bonded together, are pressed into one unit by a press. In the base substrate forming process, the metal press surface has high affinity with respect to the fourth resin-coated copper foil 11 to assure high precision press working. Thus, in the fourth resin-coated copper foil 11, in which the copper foil does not form the wiring layer, other resin-coated metal foils, other than copper foils, may be used.

[0047] The structure and the. manufacture process for the high frequency device layer portion 4 is explained in detail by referring to manufacture process diagrams of Figs.8 and 17 through 23. The manufacture process for the high frequency device layer portion 4 includes a first insulating layer forming step s-7 of forming a first insulating layer 30 on the planarized high frequency device layer forming surface 3 of the base substrate 2, prepared as described above, an underlayer processing step s-8 of applying underlayer processing for forming the device forming layer portion 28 on the first insulating layer 30 and a passive element forming step s-9 of forming each passive element in the device forming layer portion 28. The manufacture process for the high frequency device layer portion 4 prepares the high frequency module device 1 through a second insulating layer forming step s-10 of forming a second insulating layer 31 for coating the device forming layer portion 28 and for forming the wiring layer portion 29, a wiring layer forming step s-11 of forming a preset pattern 32 and passive elements on the wiring layer portion 29 and a resist layer fonning step s-12 of forming resist layers 33a, 33b coating the front and reverse major surfaces.

[0048] In the first insulating layer forming step s-7, an insulating dielectric material is fed to the high frequency device layer forming surface 3 of the base substrate 2 to form the first insulating layer 30. As the insulating dielectric material, such a material which is low in dielectric constant and in tans, that is such a material which is superior in high frequency characteristics, thermal resistance and in resistance against chemicals, is used. As the insulating dielectric material, benzocyclobutene (BCB), polyimide, polynorbornene (PNB), liquid crystal polymers (LCP), epoxy resins or acrylic resins, may be used. As the film forming method, such a method which is able to maintain coating uniformity or thickness controllability, such as a spin coating method, a roll coating method or a dip coating method, may be used.

[0049] In the first insulating layer forming step s-7, a large number of via-holes 34 are formed in the first insulating layer 30 formed on the base substrate 2, as shown in Fig.7. The respective via-holes 34 are formed in register with the preset lands 17a of the third pattern wiring layer 17 exposed to the high frequency device layer forming surface 3 to expose the lands 17a to outside. If the photosensitive resin is used as the insulating

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dielectric material, a mask formed by preset patterning is placed on the first insulating layer 30 and formed by the photolithographic method. The via-holes 34 may be formed by any other suitable methods.

[0050] In the underlayer processing step s-8, a wiring layer 35, comprised of a nickel layer and a copper layer, is formed on the entire surface of the first insulating layer 30, inclusive of the via-holes 34, such as with a sputtering method. The wiring layer 35 is formed so that the thicknesses of the nickel layer and a copper layer will each be 50 to 500 nm or thereabouts. In the underlayer processing step s-8, the wiring layer 35 is removed by etching using a liquid etchant composed of a liquid mixture of nitric acid, sulfuric acid and acetic acid, as the resister forming site of the wiring layer 35 is masked with the resist.

[0051] The wiring layer 35 is subjected to the passive element forming step s-9 to form a resistor 27 and a capacitor 28. In the removed site of the wiring layer 35 is formed a tantalum nitride layer 36, by a lift-off method, as shown in Fig.18. This tantalum nitride layer 36 is formed only in the site of the wiring layer 35 in register with the resister 27 by sputtering tantalum nitride (TaN) on the entire resist-processed surface of the wiring layer 35 and by subsequently removing tantalum nitride of the resist layer portion.

[0052] On a site of the wiring layer 35 in which to form the capacitor 26, there is also formed a tantalum nitride layer 37, as shown in Fig.18. As the entire surface of the wiring layer 35 excluding the capacitor forming site is coated with a resist, an electrical field is applied to the wiring layer 35 so that tantalum nitride becomes an anode in an electrolytic solution such as ammonium borate, by way of so-called anodic oxidation. This anodic oxidation is carried out by applying an electrical field on the order of 100V and 30 minutes to oxidize the tantalum nitride layer 37 to form a tantalum oxide (TaO_2) layer 38.

[0053] The wiring layer 35 is subjected to resist patterning by photolithographic processing so that only the necessary wiring pattern will be left. After removing the resist, the tantalum oxide layer 38 is masked, and an upper electrode 39 composed of the nickel and copper layers is formed by, for example, a lift-off method. In the high frequency device layer forming process, a high frequency transmission/reception module substrate intermediate product 41, comprised of a first device forming layer 40 on the base substrate 2 shown in Fig.19, is prepared by the above process.

[0054] In the high frequency device layer forming process, the second insulating layer 31 is formed by the second insulating layer forming step s-10 on the high frequency transmission/reception module substrate intermediate product 41, prepared by the above process, as shown in Fig.20. In the second insulating layer forming step s-10, the second insulating layer 31 is formed by a method similar to that used for preparing the first insulating layer 30, while plural via-holes 42 are formed in the second insulating layer 31 for exposing the preset pattern formed in the wiring layer 35 or the upper electrode 39 of the capacitor 26 to outside.

[0055] In the high frequency device layer forming process, a pattern wiring 32 is formed on the second insulating layer 31 by the wiring layer forming step s-11. In more detail, in the wiring layer forming step s-11, a sputtering layer composed of a nickel layer and a copper layer is formed by sputtering on the second insulating layer 31 and subjected to a photolithographic processing by way of performing preset patterning. In the wiring layer forming step s-11, the sputtering layer is subjected to selective copper plating by electrical field plating to form a copper plating layer having a thickness approximately several μm. The resist for plating then is removed and the sputtering layer is etched in its entirety to form the wiring layer portion 29 as shown in Fig.21.

[0056] An inductor 25 is formed at this time in an area of the wiring layer portion 29. The serial resistance value of the inductor 25 is then at issue. However, the inductor 29 may be formed to a sufficient thickness by employing a thick film forming technique of applying electrolytic plating to the sputtering layer, as described above, thereby minimizing the lowering in the loss.

[0057] In the high frequency device layer forming process, the high frequency device layer portion 4 is formed on the base substrate 2 by the above process steps, whereby the resin layer 11b, used to protect the second pattern wiring layer 13 from chemicals, mechanical load or the thermal load, is unnecessary. In the high frequency device layer forming process, the resin layer 11b is subjected to polishing to expose the second pattern wiring layer 13.

[0058] In the high frequency device layer forming process, permanent resist layers 33a, 33b are coated on the entire surface of the high frequency device layer portion 4 and on the second pattern wiring layer 13, respectively, the by resist layer forming step s-12. In the high frequency device layer forming process, these resist layers 33 are subjected to photolithographic processing through a mask pattern to form openings 42a, 42b at preset sites, as shown in Fig.22. In the high frequency device layer forming process, these openings 42a, 42b are subjected to electroless nickel plating/copper plating to form electrode terminals 43a, 43b to prepare the high frequency module device 1 shown in Fig. 23.

[0059] In the high frequency module device 1, the electrode terminal 43a, provided on the high frequency device layer portion 4, and carrying the high frequency IC 90 or a chip component 91, forms a connection terminal. In the high frequency module device 1, the electrode terminal 43b, provided on the second wiring pattern layer 13 of the base substrate 2, forms a connection terminal and an input/output terminal 24 in loading the device on e.g., the motherboard 99. The high frequency IC 90 is mounted by e.g., a flip chip method through a solder bump 94.

[0060] In the above-described high frequency module

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device 1, the process of bonding the first to fourth resin coated copper foils 8 to 11 to the first major surface 5a and the second major surface 5b of the core substrate 5, comprised of a double-sided substrate, to form the four layer base substrate 2. Of course, the present invention is not limited to this manufacture process for the base substrate 2. In a base substrate manufacture process, shown as a second embodiment in Figs.24A-24F, a base substrate 50 similar to the base substrate 2 described above is prepared using two double-sided substrates 51a, 51b. Since the base substrate manufacture process is similar as to respective steps to the manufacture process for the base substrate 2 described above, it is not explained here specifically.

[0061] In the base substrate manufacture process, the electrically conductive portions 52a, 52b on the front and reverse major surfaces 5a, 5b of the double-sided substrate 51 shown in Fig.24A is subjected to photolithographic processing, by way of preset patterning, to form preset circuit patterns 53a, 53b by etching, as shown in Fig.24B. In the base substrate forming process, the two double-sided substrates 51a, 51b are bonded together, with e.g., an intermediate resin material 54 in-between, as shown in Fig.24C. In the base substrate forming process, the circuit patterns 53a, 53b of the double-sided substrates 51a, 51b are interconnected through via-holes, as shown in Fig.24D, to form a base substrate intermediate product 55.

[0062] In the base substrate forming process, a first resin-coated copper foil 56 and a second resin-coated copper foil 57 are bonded by heat press on the front and reverse major surfaces of the base substrate intermediate product 55, as shown in Fig.24E. In the base substrate forming process, as shown in Fig.24F, the first resin-coated copper foil 56 and the second resin-coated copper foil 57 are subjected to polishing. In the base substrate forming process, the first resin-coated copper foil 56 is subjected to polishing so that the circuit pattern 53a will be exposed to outside, insofar as the first double-sided substrate 51a is concerned, to form a highly planarized high frequency device layer forming surface 58. In the base substrate forming process, the second resin-coated copper foil 57 is subjected, to polishing so that the circuit pattern 53b will not be exposed to outside, insofar as the first double-sided substrate 51b is concerned. In the base substrate forming process, the base substrate 50 is prepared through the above processing steps, as shown in Fig.24G.

[0063] The base substrate forming process, shown in Figs.25A-25D as a third embodiment, includes a process of coating a liquid resin material 60 by a dip coating method on the base substrate intermediate product 55, shown in Fig.25A, produced by e.g., the above-described second embodiment. That is, in the base substrate forming process, a liquid resin material 60, dissolved with a suitable solvent, is accumulated in a dip tank 61, in which the base substrate intermediate product 55 is immersed, as shown in Fig.25B.

[0064] In the base substrate forming process, the base substrate intermediate product 55 is taken out from the dip tank 61 after a proper dipping time at a proper lift speed. In the base substrate forming process, resin layers 62a, 62b of the liquid resin material 60 are formed simultaneously on the front and reverse major surfaces of the base substrate intermediate product 55, as shown in Fig.25C. In the base substrate forming process, the base substrate intermediate product 55, now carrying the resin layers 62, is subjected to baking, as the base substrate intermediate product 55 is kept in a horizontal position, to vaporize excess organic components off. In the base substrate forming process, the base substrate intermediate product 55 is subjected to the aforementioned polishing, whereby the resin layers 62a, 62b are polished in preset amounts to produce a base substrate 63 shown in Fig.25D.

[0065] In the base substrate forming process, the concentration of the liquid resin material 60, dip time or the lift speed is controlled to realize the film thickness accuracy of the resin layers 62. Meanwhile, the resin layers 62 may be planarized by dry etching methods, such as reactive ion etching (RIE) or plasma etching (PE).

[0066] Meanwhile, in the high frequency module device 1, a high frequency IC 90 or a chip component 91 is loaded by a flip chip method on the surface of the high frequency device layer forming surface 3, with the entire device being covered by the shield cover 92, as shown in Fig.7. So, with the high frequency module device 1, heat evolved from the high frequency IC 90 or the chip component 91 is accumulated in the shield cover 92. Therefore, it is desirable to provide a heat radiating structure.

[0067] In the high frequency module device 1, a heat conductive resin material 70 is charged into a space defined between the upper surface of the high frequency IC 90 having a large heat generating volume and the inner surface of the shield cover 92, as shown in Fig.26. In the high frequency module device 1, the heat evolved from the high frequency IC 90 is transmitted through the heat conductive resin material 70 to the shield cover 92 and then radiated to outside. Meanwhile, since the high frequency IC 90 of a larger size is held by the heat conductive resin material 70 and by the shield cover 92, the high frequency module device 1 is also improved in mechanical strength.

[0068] In the high frequency module device 1, a large number of cooling via-holes 71, for establishing communication between the base substrate 2 and the high frequency device layer portion 4, may be provided in register with the loading area of the high frequency IC 90, as shown in Fig.27. These cooling via-holes 71 are formed at the time of forming the interconnecting via-holes in the base substrate 2 or in the high frequency device layer portion 4 by a similar process. In the high frequency module device 1, the heat from the high frequency IC 90 is transmitted through the cooling via-holes 71 to the bottom surface of the base substrate 2

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and then radiated to outside. If the high frequency module device 1 is used simultaneously as the heat-radiating electrically conductive resin material 70, described above as shown in Fig.27, heat radiation occurs from above and below to improve the heat radiation.

[0069] In the high frequency module device 1, a copper foil portion 72, formed in the base substrate 5, may be increased in thickness to e.g., 50 nm, as shown in Fig.27. In the high frequency module device 1, heat radiation may occur from the base substrate 5 by connecting the cooling via-holes 71 to the copper foil portion 72.

[0070] In the high frequency module device 1, a core substrate 73, forming the base substrate 2, may be formed of an electrically conductive material, as shown in Fig.28. The core substrate 72 may be formed by a metal core of high electrically conductivity, such as copper or 42-alloy, to interconnect the numerous cooling via-holes 71. In the high frequency module device I, heat radiation occurs not only from the heat-radiating electrically conductive resin material 70 and from the cooling via-holes 71, but from the core substrate 73, thus assuring efficient heat radiation to improve the operational reliability.

Claims

1. A high frequency module device comprising:

a base substrate including a core substrate formed of an organic material having thermal resistance and high frequency characteristics, and a pattern wiring layer formed on a first major surface of said core substrate and a base substrate, an uppermost layer of said pattern wiring layer being planarized to form a high frequency device layer forming surface; and
a high frequency device layer formed on said high frequency device layer forming surface of said base substrate;

wherein passive elements are formed the high frequency device layer passive elements by a thin film forming technique or by a thick film forming technique, said passive elements including resistors, capacitors and pattern wiring portions supplied with power or signals from said base substrate through a dielectric insulating layer.

2. The high frequency module device according to claim 1 wherein said core substrate is a double-sided substrate or an epoxy-based double-sided substrate formed of one or more materials selected from the group consisting of polyphenyl ethylene, bismaleidotriazine, polyimide, liquid crystal polymer, polynorbornene, ceramics and mixtures of ceramics and organic materials.

3. The high frequency module device according to claim 1 or 2 wherein said core substrate has a patterned input/output terminals on a second major surface of said core substrate facing said high frequency device layer forming surface so as to serve as a power source or as a signal input/output surface, and wherein said second major surface being directly mounted on a motherboard through said input/output terminals.

4. The high frequency module device according to claim 1, 2 or 3 wherein said dielectric insulating layer forming said high frequency device layer is formed as multiple layers on said high frequency device layer forming surface of said base substrate from an organic material, such as benzocyclobutene, polyimide, polynorbornene or liquid crystal polymer, epoxy-based resin or acrylic resin exhibiting high frequency characteristics, thermal resistance, resistance against chemicals, uniform coating characteristics and thickness controlling characteristics.

5. The high frequency module device according to any preceding claim wherein a pattern wiring layer is formed on the dielectric insulating layer formed as the uppermost layer of said high frequency device layer, wherein a coating layer is formed by exposing a preset land of a pattern wiring, and wherein at least one high frequency IC device directly connected to said land is directly loaded on said coating layer.

6. The high frequency module device according to claim 5 wherein a shield cover covering an entire surface including said high frequency IC device is mounted on said high frequency device layer.

7. The high frequency module device according to claim 6 wherein a resin material exhibiting heat conduction properties is charged into a space between said high frequency IC device and an inner surface of said shield cover.

8. The high frequency module device according to claim 6 or 7 wherein a large number of heat-radiating via-holes communicating with said base substrate are formed in said high frequency device layer in register with a loading area for said high frequency IC device.

9. The high frequency module device according to claim 8 wherein a large number of heat-radiating via-holes communicating with respective heat-radiating via-holes of said high frequency device layer are formed in said base substrate and wherein a heat radiating plate is formed in said core substrate.

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10. The high frequency module device according to claim 8 or 9 wherein said heat-radiating via-holes are connected to a portion of the pattern wiring layer formed on said first major surface of said core substrate, and wherein said pattern wiring layer has a thickness not less than 50 μm.

11. A method for preparing a high frequency module device comprising:

a base substrate forming step for producing a base substrate through a first step of forming a core substrate from an organic material exhibiting thermal resistance and high frequency characteristics, a second step of forming a multi-layer pattern wiring layer on a first major surface of said core substrate and a third step of planarizing an uppermost layer so as to form a high frequency device layer forming surface; and

a high frequency device layer forming step of forming passive elements in said high frequency device layer, composed of resistors, capacitors or pattern wiring units, on said high frequency device layer forming surface of said base substrate, by a thin-film or thick-film technique, said passive elements being fed with power or signals from the side base substrate through a dielectric insulating layer.

12. The method for preparing the high frequency module device according to claim 11 wherein said first step of forming said core substrate is a step of forming a double-sided substrate from a material selected from the group consisting of polyphenol ethylene, bismaleidotriazine, polyimide, liquid crystal polymer, polynorbornene, ceramics, mixtures of ceramics and organic materials and epoxy-based resins.

13. The method for preparing the high frequency module device according to claim 11 or 12 wherein said base substrate forming step includes a coating resin layer forming step of forming a first coating layer coating a wiring pattern layer formed as an uppermost layer of said first major surface and a second coating resin layer coating a second major surface facing said first major surface;

said first coating resin layer being polished along with the wiring pattern layer of said uppermost layer in said third step previous to said high frequency device layer forming step so that said first coating resin layer will be flattened with said wiring pattern layer;

said second coating resin layer being polished as a step following said high frequency device layer forming step so as to expose the wiring pattern layer formed on said second major surface to form an input/output terminal.

14. The method for preparing the high frequency module device according to claim 13 wherein said input/output terminal formed on the second major surface of said core substrate is connected to the input/output terminal formed in a motherboard, so that said input/output terminal is mounted directly on said motherboard.

15. The method for preparing the high frequency module device according to claim 11, 12, 13, or 14 wherein at least two of said dielectric insulating layers which form said high frequency device layer is formed on the high frequency device layer forming surface of said base substrate, said dielectric insulating layers being formed of organic materials, such as benzocyclobutene, polyimide, polynorbornene or liquid crystal polymers, epoxy resins or acrylic resins, exhibiting high frequency characteristics, thermal resistance, resistance against chemicals, uniform coating properties and thickness controlling characteristics.

16. The method for preparing the high frequency module device according to any one of claims 11 to 15 wherein said high frequency device layer forming step includes:

a first dielectric insulating layer forming step of forming said first dielectric insulating layer on said high frequency device layer forming surface and a first layer forming step of forming a first wiring layer on said first dielectric insulating layer and of forming a resistor and a capacitance by patterning; and

a second dielectric insulating layer forming step of forming said second dielectric insulating layer on said first insulating layer and a second layer forming step of forming a second wiring layer on said second dielectric insulating layer on said second dielectric insulating layer and also forming an inductor and a wiring.

17. The method for the preparation of a high frequency module device according to claim 16 wherein in said first layer forming step, after a thin film metal layer formed by sputtering or chemical vapor deposition on said first wiring layer is patterned, a site for forming said resistor is subjected to anodic oxidation to form said resistor comprised of a high dielectric layer.

18. The method for preparing the high frequency module device according to any one of claims 11 to 18 wherein said high frequency device layer forming step includes a step of forming a pattern wiring layer

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on said dielectric insulating layer fonned as the uppermost layer of said high frequency device layer, and forming a coating layer by exposing a preset land of a pattern wiring, and wherein at least one high frequency IC device directly connected to said land is directly loaded on said coating layer.

19. The method for preparing the high frequency module device according to claim 18 further comprising a step of mounting a shield cover covering an entire surface including said high frequency IC device on said high frequency device layer.

20. The method for preparing the high frequency module device according to claim 19 further comprising a step of charging a resin material exhibiting heat conduction properties into a space between said high frequency IC device and an inner surface of said shield cover.

21. The method for preparing the high frequency module device according to any one of claims 11-20 wherein said high frequency device layer forming step includes a step of forming a large number of heat-radiating via-holes communicating with said base substrate in said high frequency device layer in register with the loading area for said high frequency IC device.

22. The method for preparing the high frequency module device according to claim 21 wherein a large number of heat-radiating via-holes communicating with respective heat-radiating via-holes of said high frequency device layer are formed in said base substrate and wherein a heat radiating plate is formed in said core substrate.

23. The method for preparing the high frequency module device according to claim 22 wherein said pattern wiring layer which is pattern-formed on said base substrate and is connected to said heat-radiating via-holes is formed to have thickness of not less than 50 μm.

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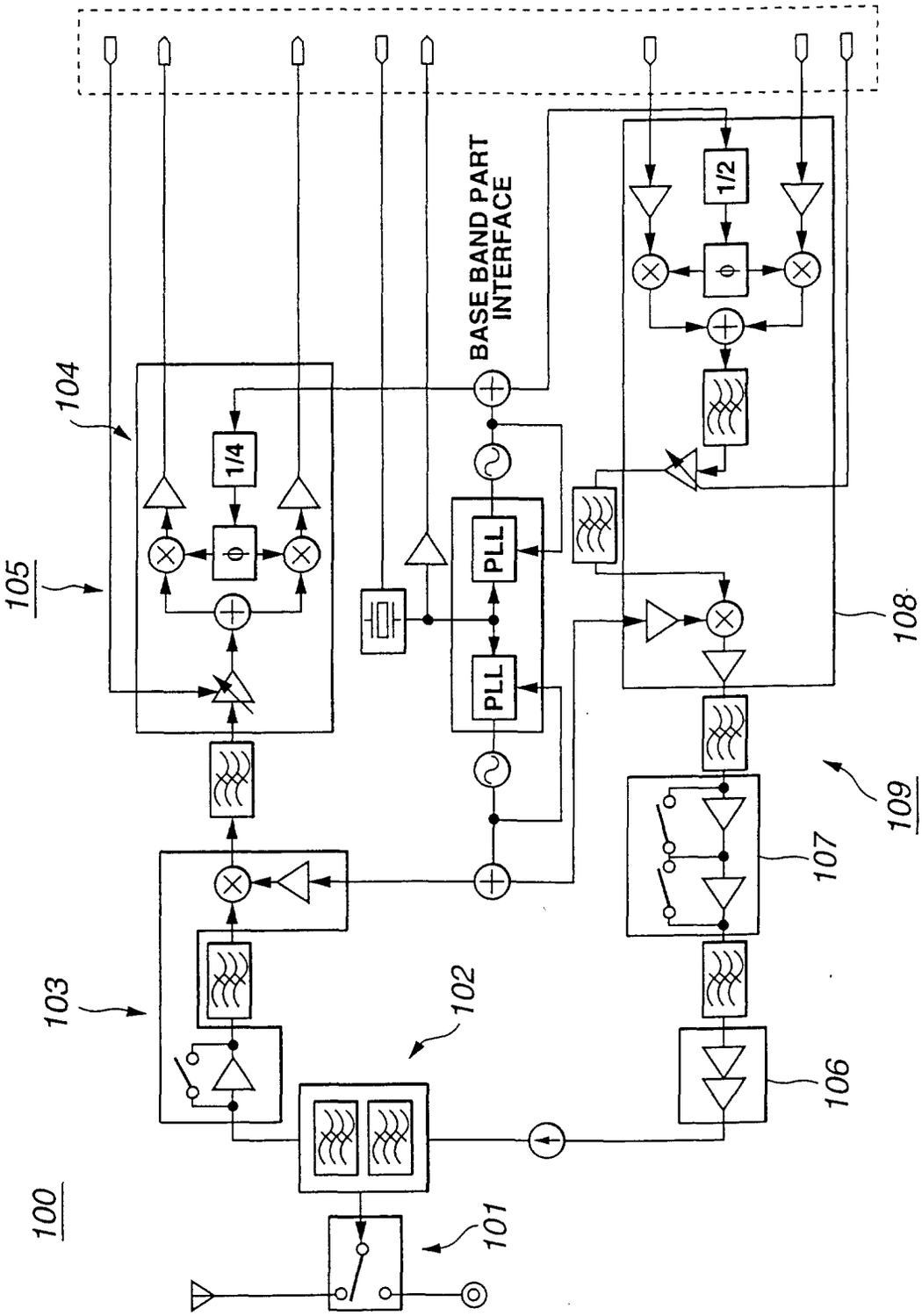

BASE BAND PART INTERFACE
PLL
PLL
1/4
1/2
100
101
102
103
104
105
106
107
108
109

FIG.1

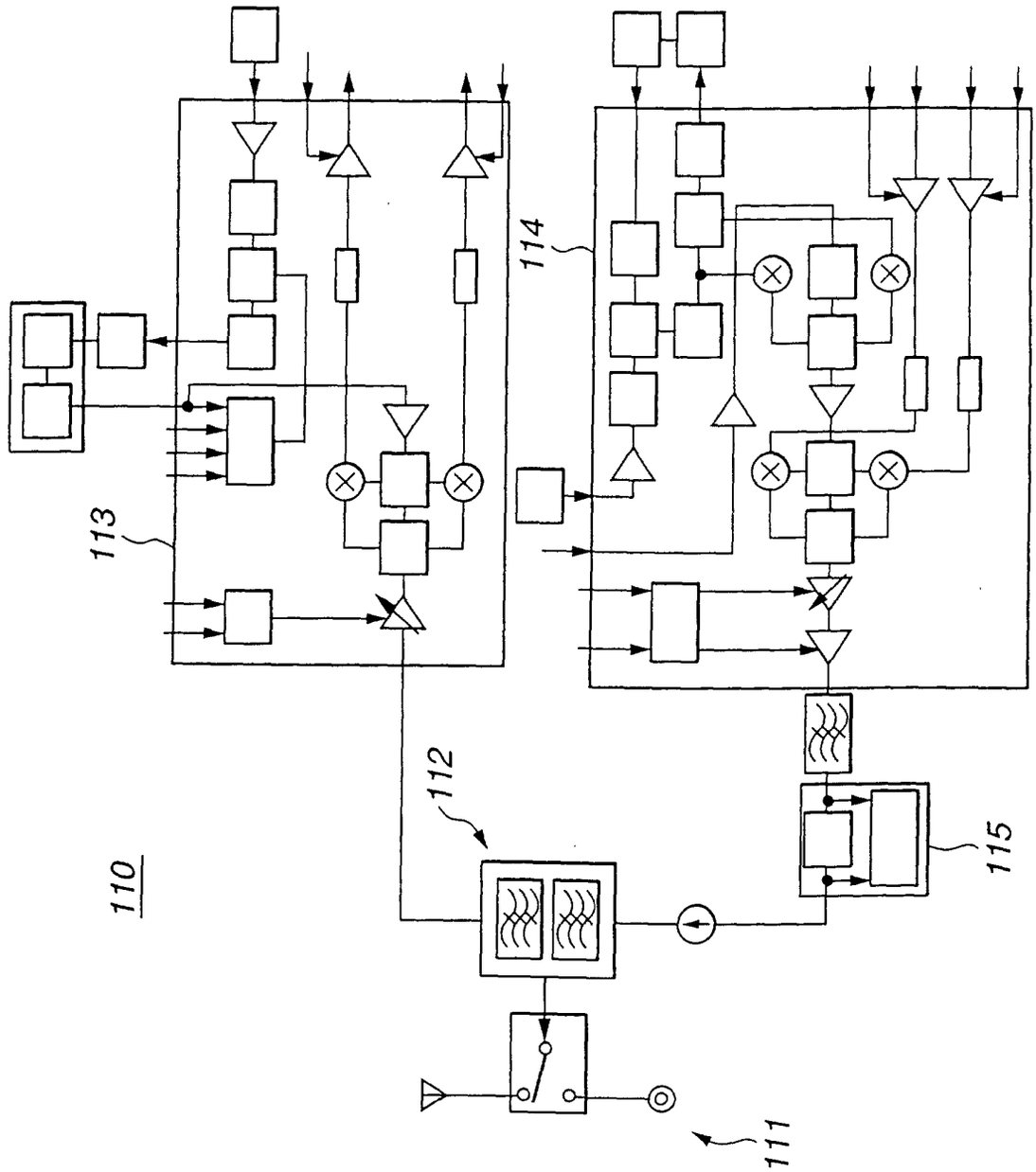


FIG.2

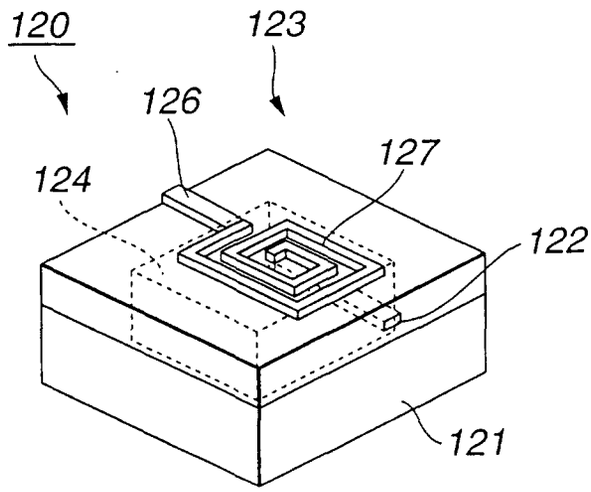


FIG.3A

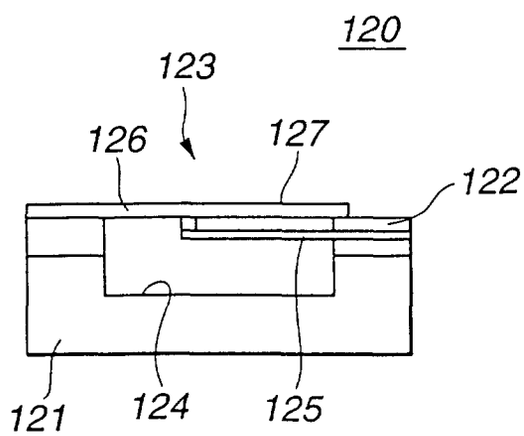


FIG.3B

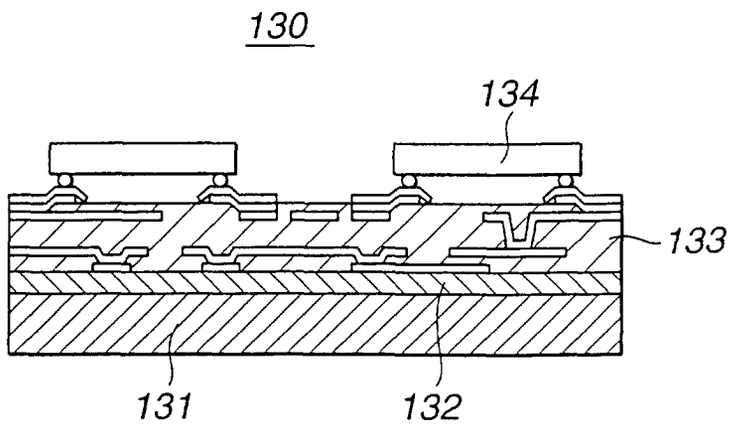


FIG.4

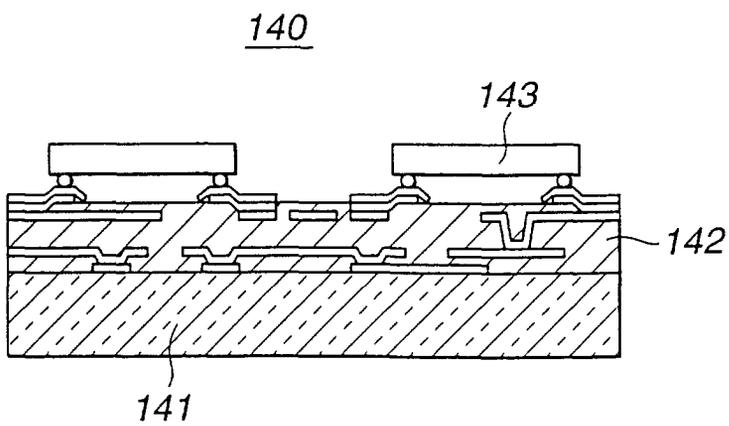


FIG.5

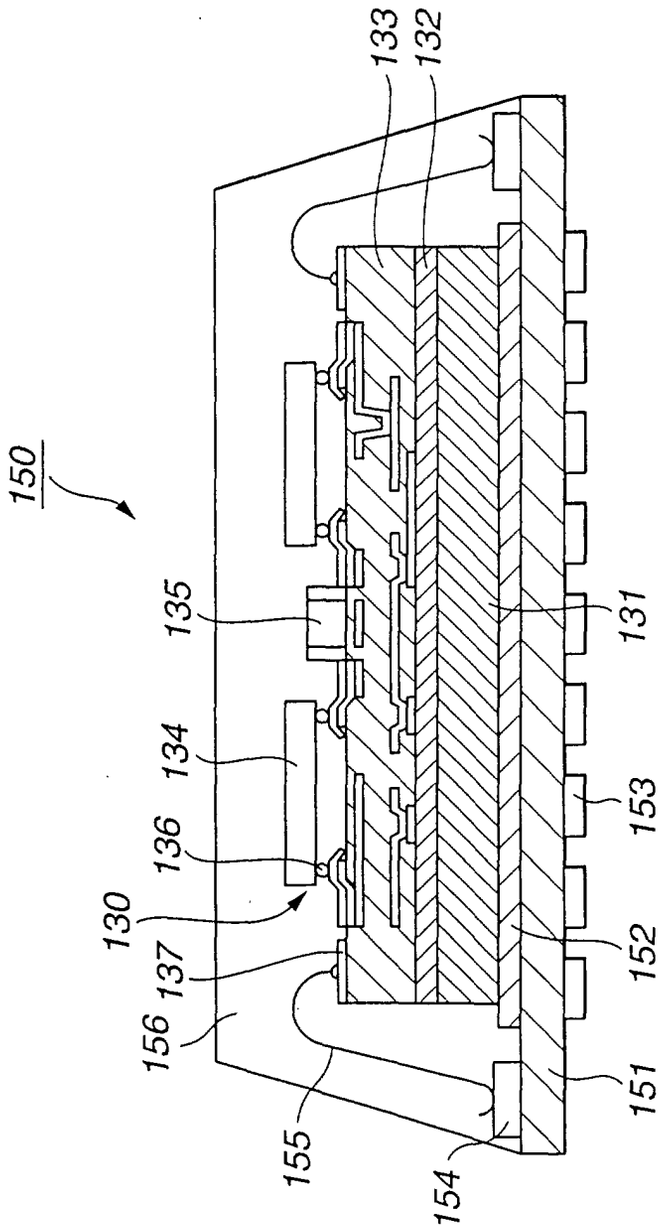
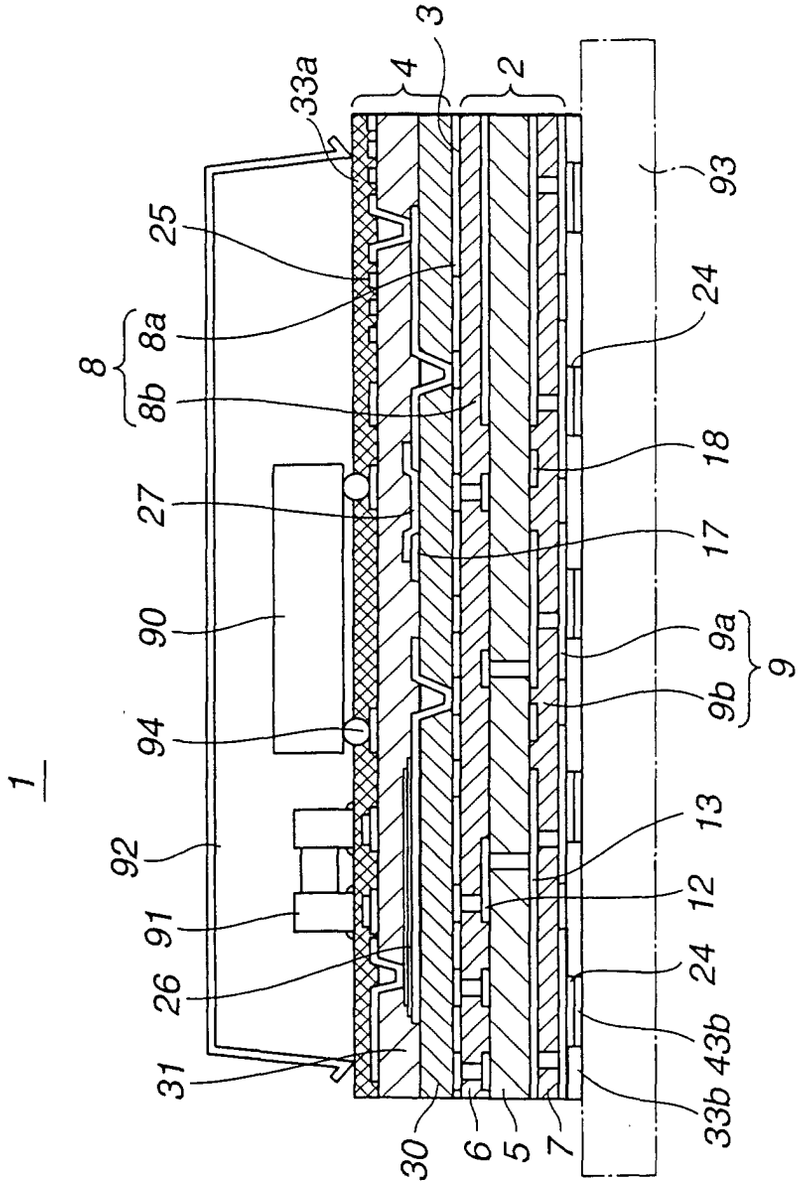


FIG.6


1
92
91
26
31
94
90
27
8
8b
8a
25
33a
4
3
2
93
24
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17
9a
9b
9
13
12
24
43b
33b
7
5
6
30

FIG.7

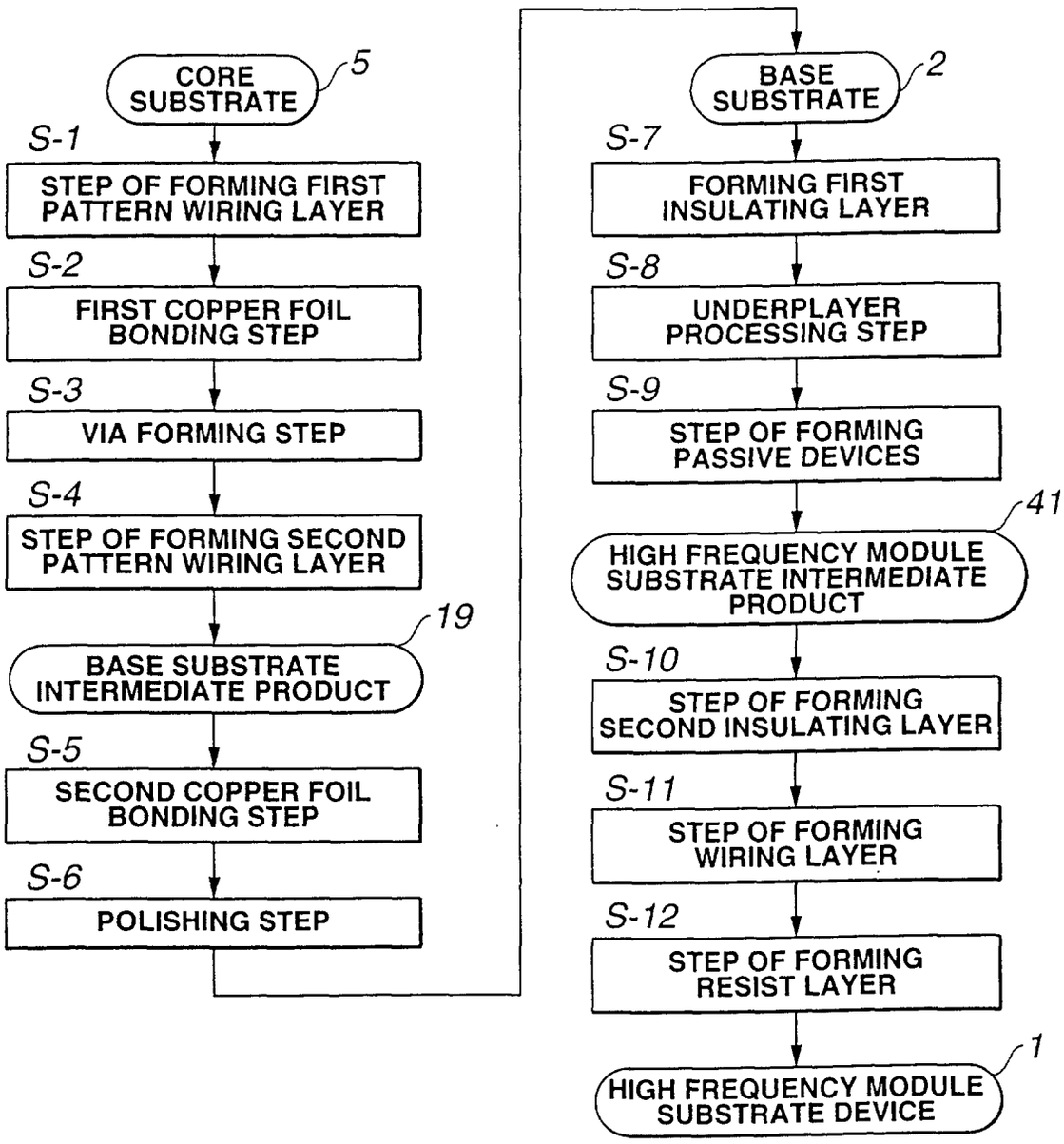
CORE SUBSTRATE
5
S-1
STEP OF FORMING FIRST PATTERN WIRING LAYER
S-2
FIRST COPPER FOIL BONDING STEP
S-3
VIA FORMING STEP
S-4
STEP OF FORMING SECOND PATTERN WIRING LAYER
19
BASE SUBSTRATE INTERMEDIATE PRODUCT
S-5
SECOND COPPER FOIL BONDING STEP
S-6
POLISHING STEP
BASE SUBSTRATE
2
S-7
FORMING FIRST INSULATING LAYER
S-8
UNDERPLAYER PROCESSING STEP
S-9
STEP OF FORMING PASSIVE DEVICES
41
HIGH FREQUENCY MODULE SUBSTRATE INTERMEDIATE PRODUCT
S-10
STEP OF FORMING SECOND INSULATING LAYER
S-11
STEP OF FORMING WIRING LAYER
S-12
STEP OF FORMING RESIST LAYER
1
HIGH FREQUENCY MODULE SUBSTRATE DEVICE

FIG.8

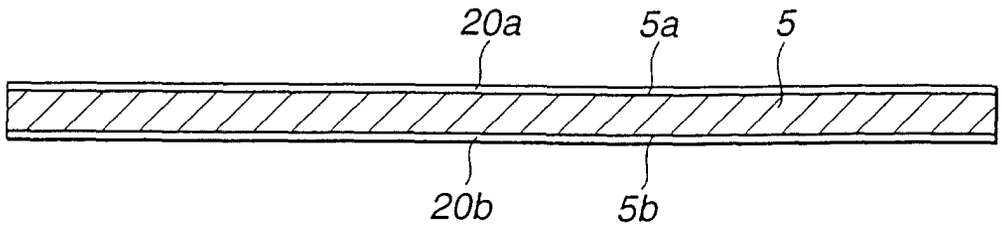

FIG.9

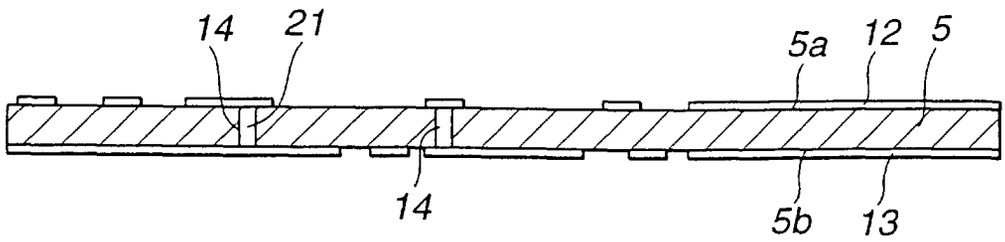

FIG.10

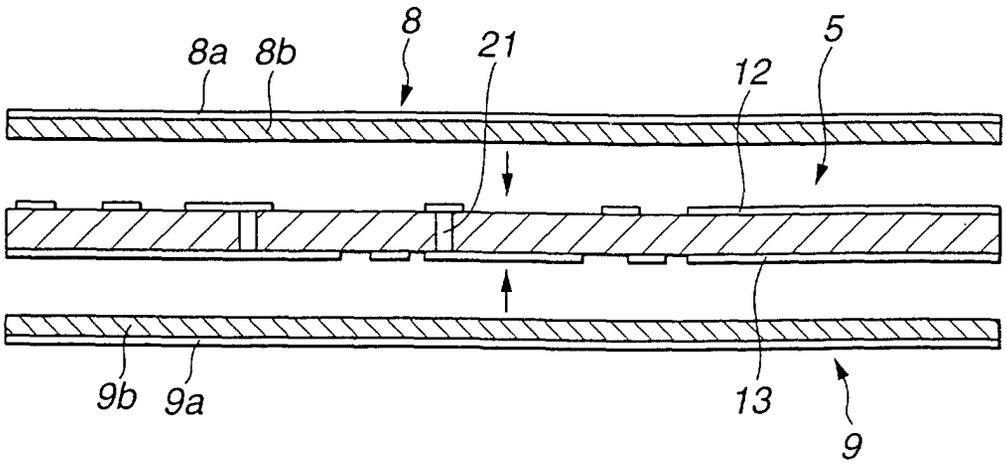

FIG.11

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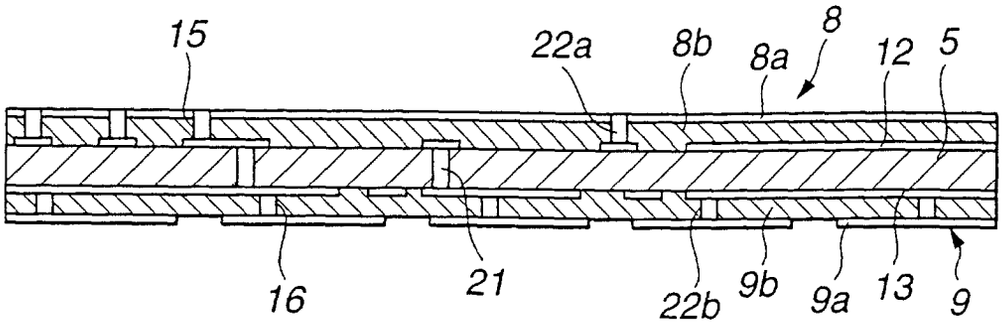

FIG.12

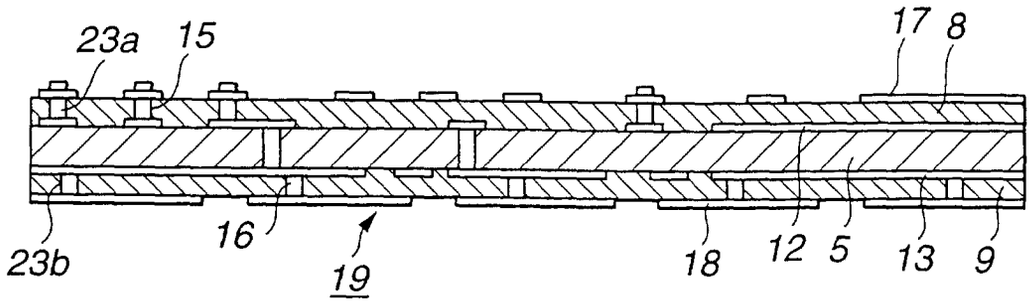

FIG.13

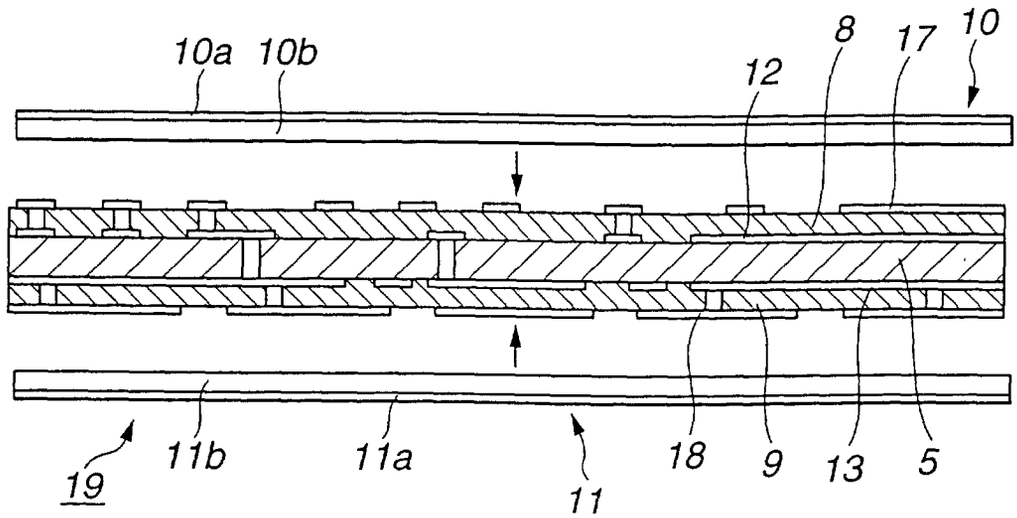

FIG.14

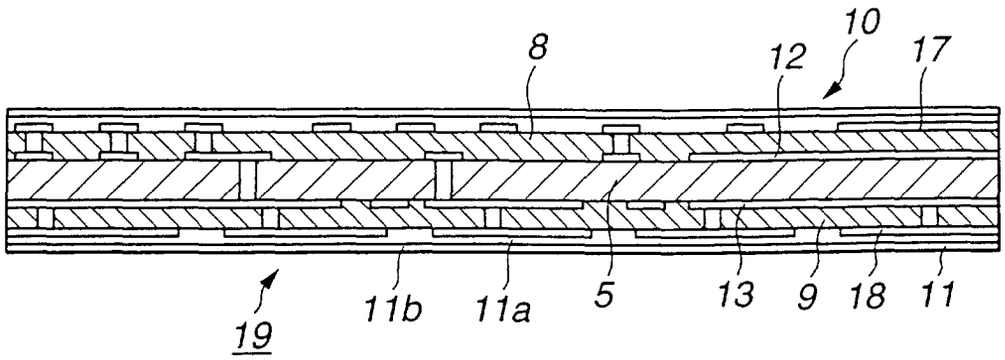

FIG.15

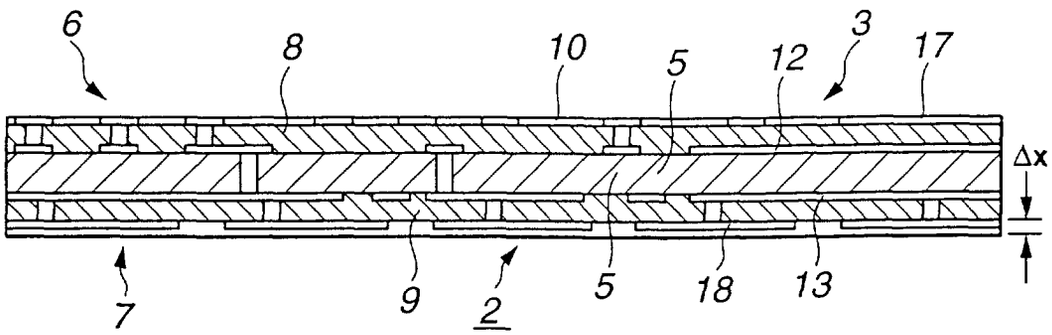

FIG.16

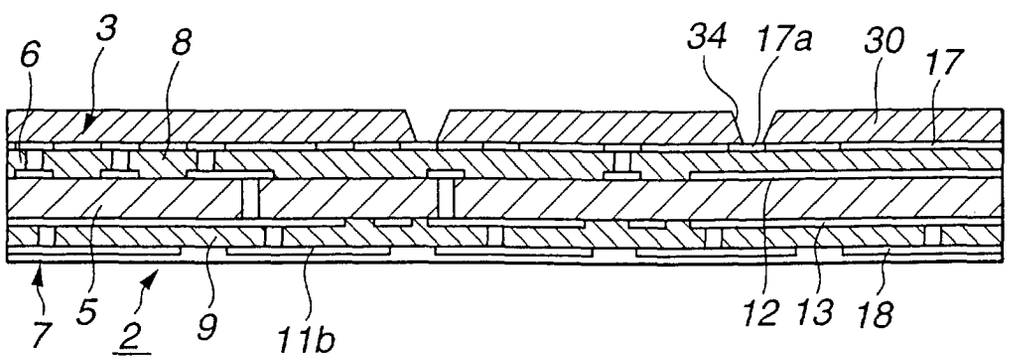

FIG.17

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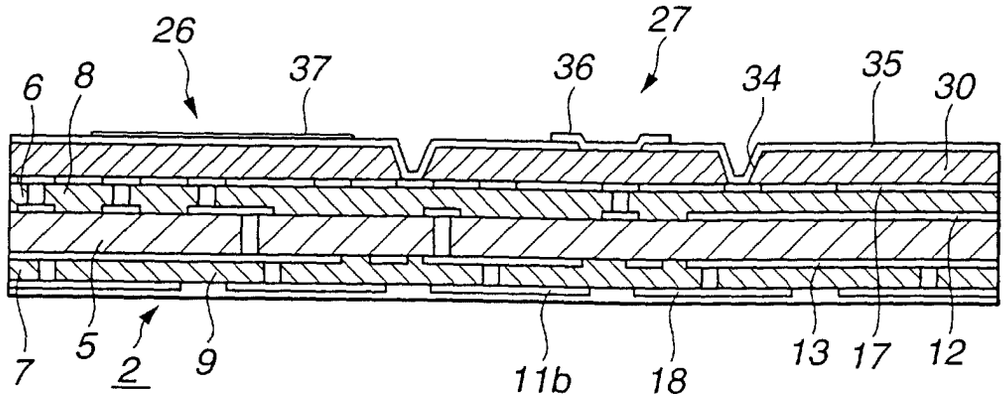
26
27
6
8
37
36
34
35
30
7
5
2
9
11b
18
13
17
12

FIG.18

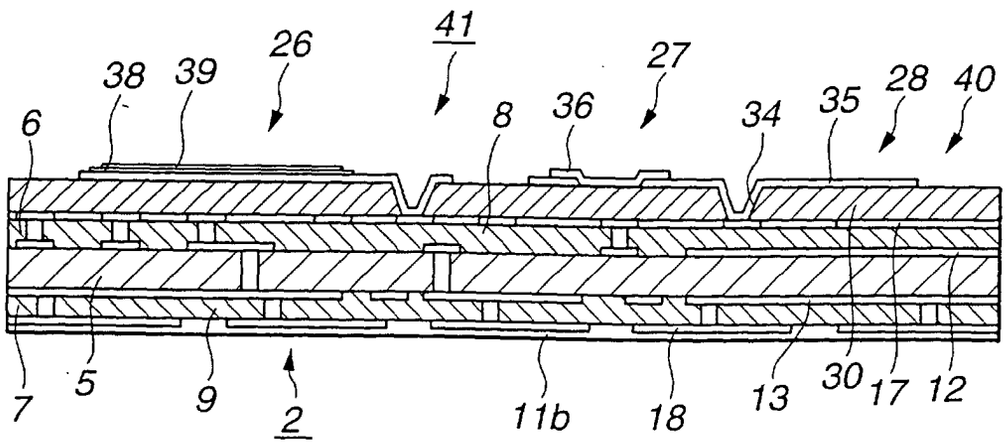
41
26
27
38
39
6
8
36
34
35
28
40
7
5
9
2
11b
18
13
30
17
12

FIG.19

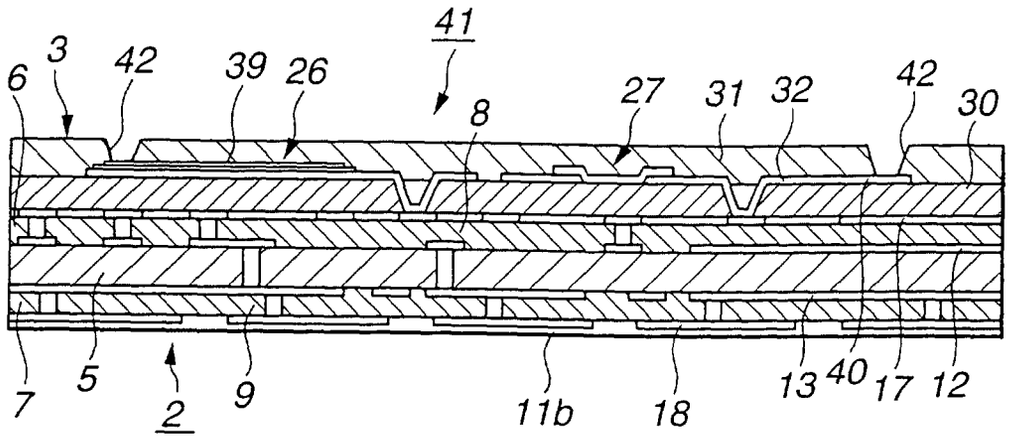

FIG.20

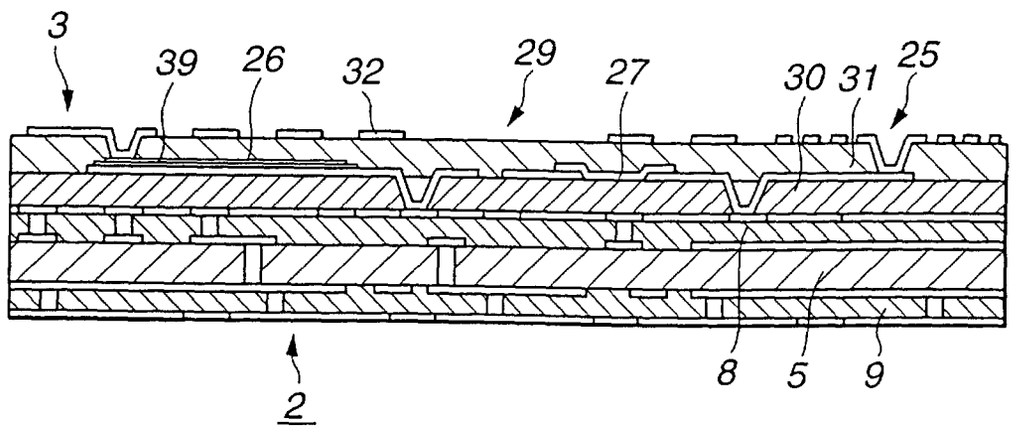

FIG.21

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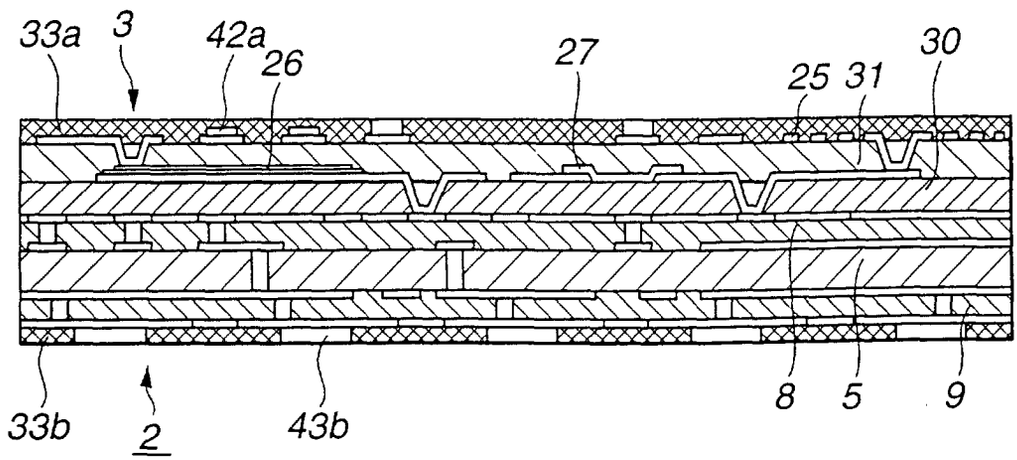
33a
3
42a
26
27
25
31
30
33b
2
43b
8
5
9

FIG.22

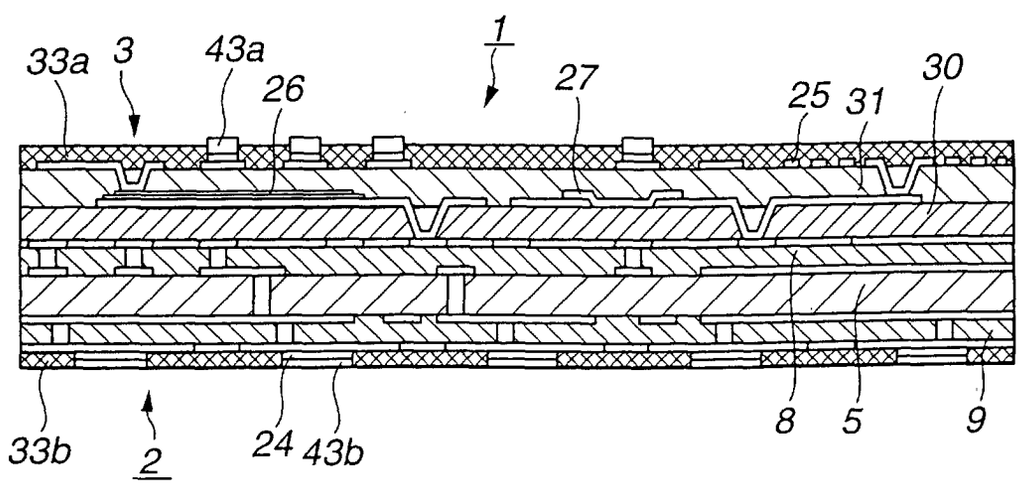
1
33a
3
43a
26
27
25
31
30
33b
2
24
43b
8
5
9

FIG.23

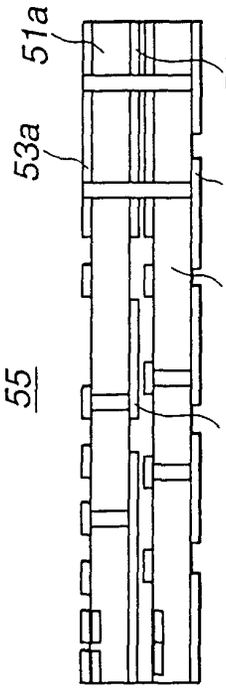

FIG.24D

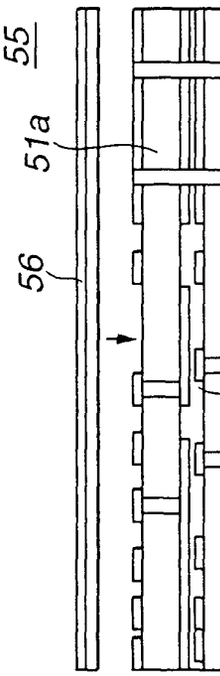

FIG.24E

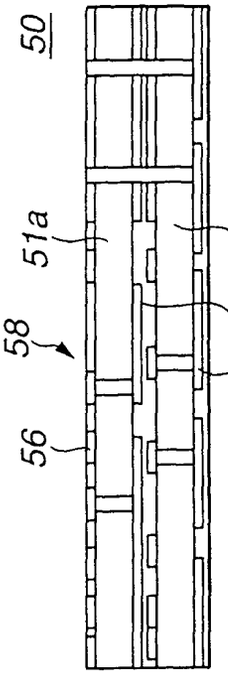

FIG.24F

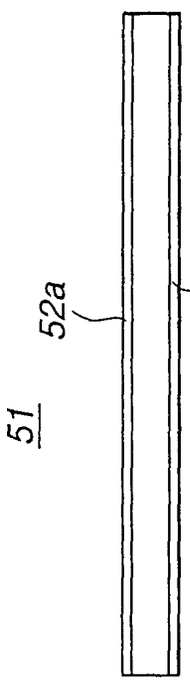

FIG.24A

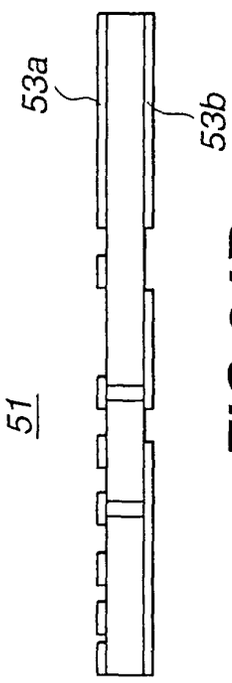

FIG.24B

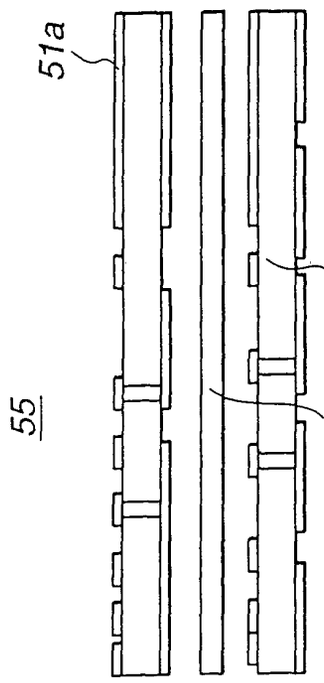

FIG.24C

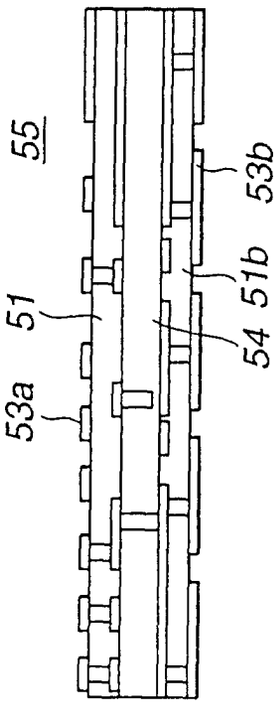

FIG.25A

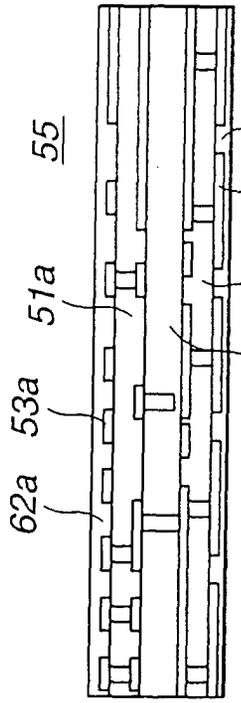

FIG.25C

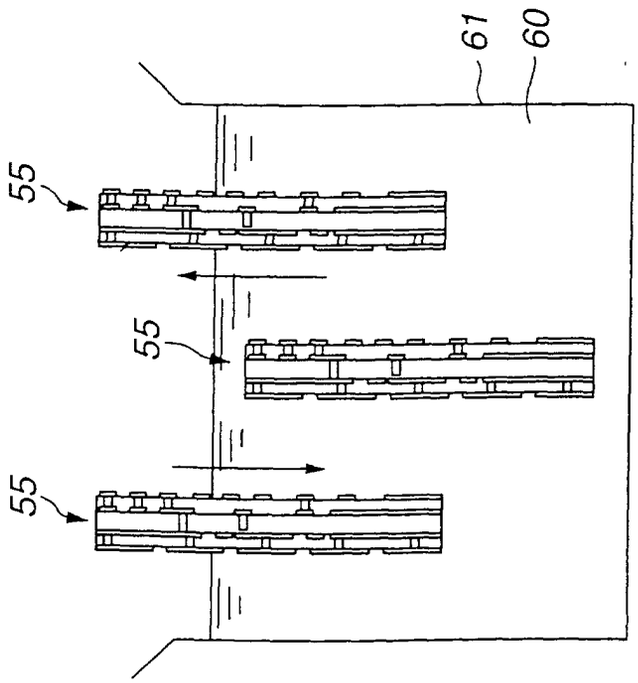

FIG.25B

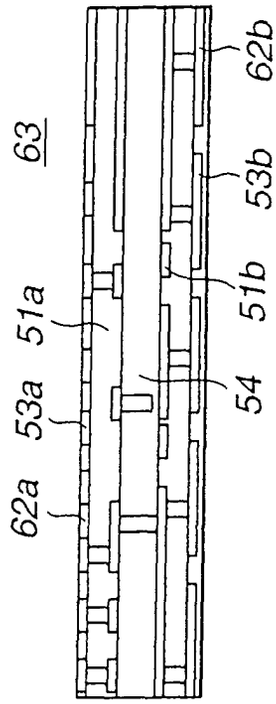

FIG.25D

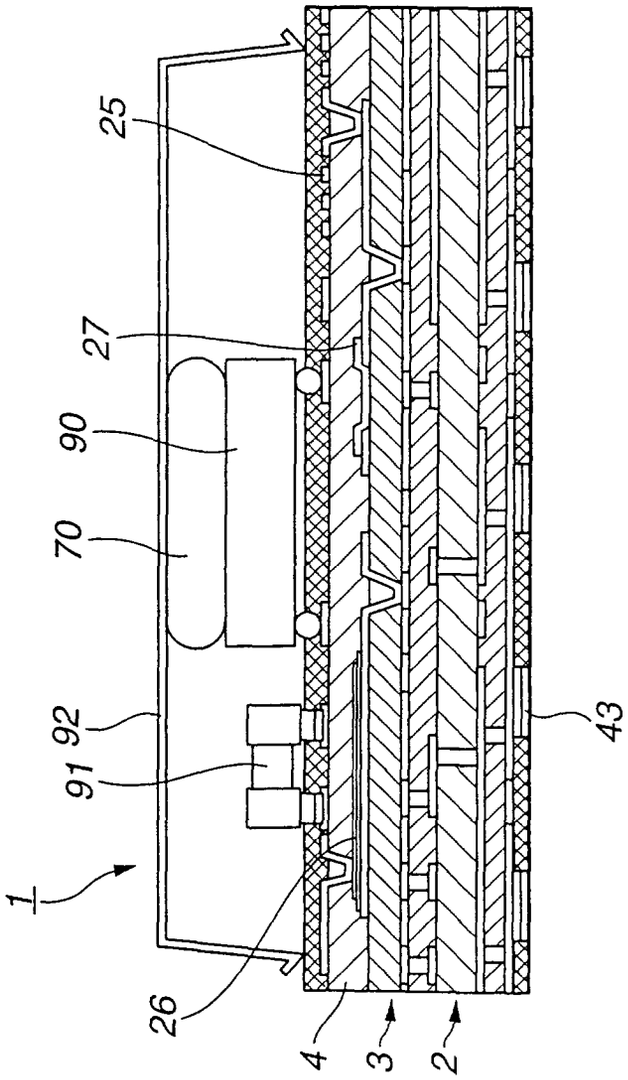

FIG.26

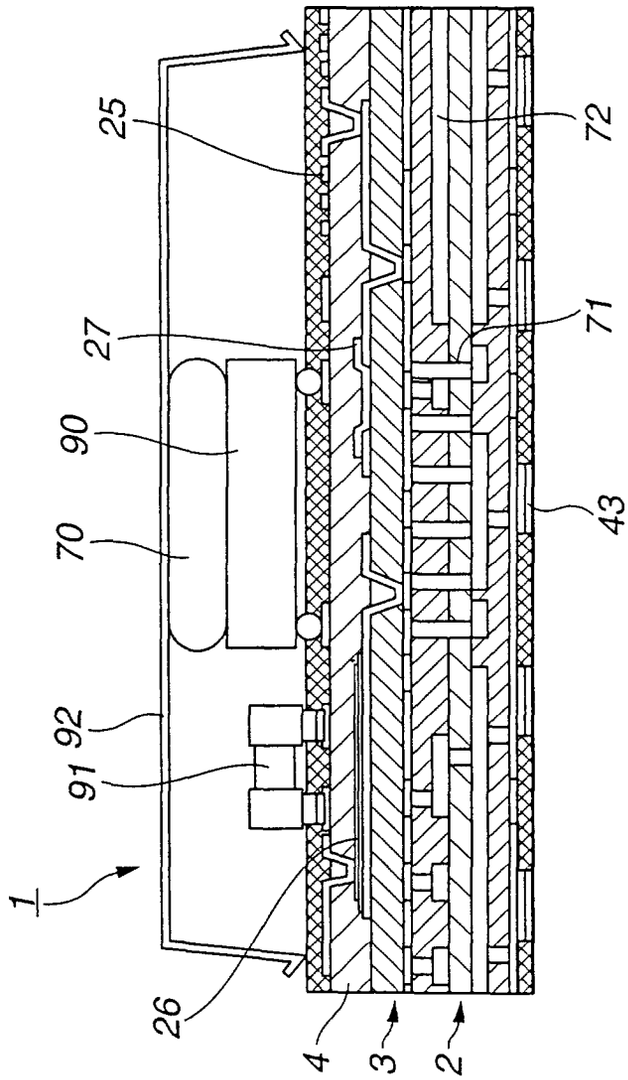

FIG.27

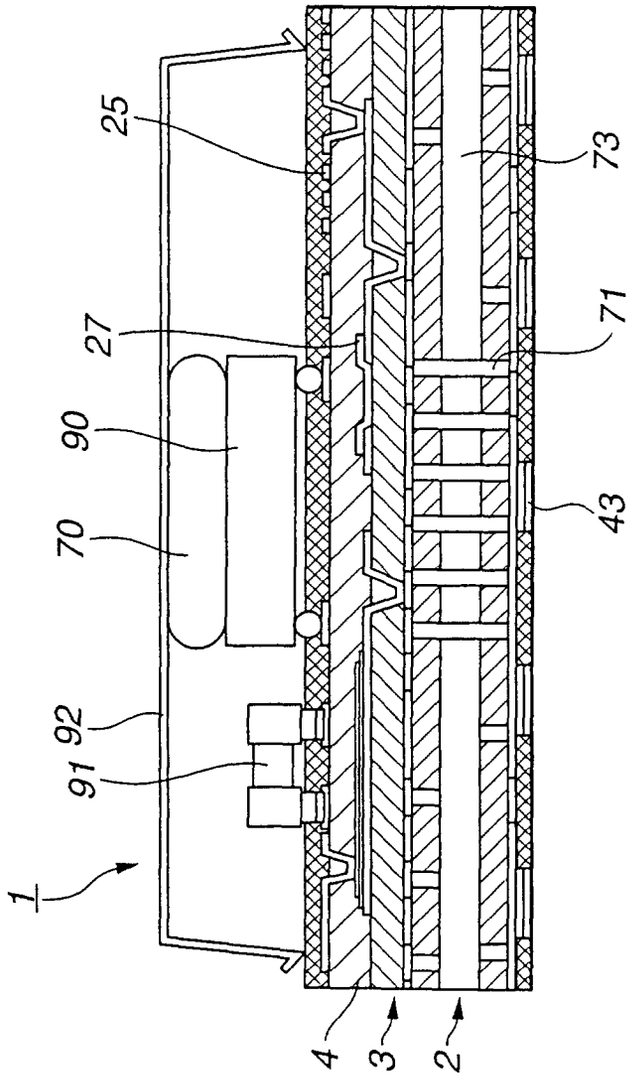

FIG.28