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DESIGN AND IMPLEMENTATION OF HIGH-Q PASSIVE DEVICES FOR WIRELESS APPLICATIONS USING SYSTEM-ON-PACKAGE (SOP) BASED ORGANIC TECHNOLOGIES

A Thesis

Presented to

The Academic Faculty

By

Sidharth Dalmia

In Partial Fulfillment

of the Requirements for the Degree of

Doctor of Philosophy

In Electrical and Computer Engineering

Georgia Institute of Technology

September 2002

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DESIGN AND IMPLEMENTATION OF HIGH-Q PASSIVE DEVICES FOR WIRELESS APPLICATIONS USING SYSTEM-ON-PACKAGE (SOP) BASED ORGANIC TECHNOLOGIES

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DEDICATION

To my parents, and grandmother, and the Fatehpuria, Dalmia, Poddar,

Khemka, Bubna, Kataria, Hobbs and Agarwal families for their

Love, Support, Dedication, and Friendship

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ACKNOWLEDGMENT

I wish to thank God for all His love and blessings. I would also like to thank Him for this opportunity and for the courage to hold on to it.

I will be forever grateful to my advisor, Dr. Swaminathan, not only for his guidance and support, but also for his confidence in me to accomplish the tasks at hand. I would also like to thank Dr. Ayazi for his advice and interest in this work. Gratitude is extended to my committee: Dr. Tummala, Dr. Peterson, Dr. C. P. Wong, and Dr. Sung-Kyu Lim. I appreciate their time and effort in serving on my committee.

I want to thank all the members of the Epsilon group and the Packaging Research Center for their contributions to my successful stay at Georgia Tech. I especially want to thank the following people: Sung Hwan Min, Jinwoo Choi, Nanju Na, Jifeng Mao, Woopoung Kim, Erdem Matoglu, Dr. Bhattacharya, Amit Bavisi, and Orfi Sanchez.

It is with the sincerest gratitude that I thank the next set of people, not just for their help but also for their friendship. Dr. White, Dr. Joseph Hobbs, Venky Sundaram, and Vinu Govind thank you for your kindness, generosity and indescribable support.

Finally would like to thank my entire family. Thank you to my parents, Mr. Subhash Dalmia and Mrs. Sita Dalmia, who have provided me with invaluable love, inspiration, and support through out my life. They have always taught me to be to kind, respectful, honest and thankful. Thank you to all masis and masas, chachas and chachis, especially Sharda masi, for making me a part of their families. Thank you to the Katarias for having faith and confidence in me. I also wish to thank my friends for their love and support.

Finally, I wish to thank Lopa for being a part of my life. She has taught me to enjoy what I have and not keep wanting more. I will be forever grateful to you.

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SUMMARY

Ceramic and silicon substrate interconnection and packaging technologies have been used for many years in many different types of applications such as integrated passive devices and modularization. This is especially true for the wireless handheld market segments. Although more cost-effective, there is an inherent inertia that has built up towards using organics for similar applications and remains a technology of choice primarily for circuit boards, IC packaging and flex applications. There is a perception that organic technology is inadequate and lower in performance compared to ceramics and silicon technologies for RF and mixed signal integration. This research discusses the feasibility of obtaining high Q embedded passive components for standards such as the Bluetooth (2.45GHz) and PCS (1.9GHz) using organic substrates. A system-on-package (SOP) approach has been taken at the heart of which is a low-cost, low-temperature, multi-layer organic sequential build-up (SBU) technology. Inductors and capacitors greater than 1nH and 1pF, respectively, with Q-factors in the range of 60-400 have been implemented for frequencies from 1-10 GHz. Robust methods to characterize the materials and process have been developed. Fast and accurate methods have been devloped to model and optimize embedded passives such as inductors, capacitors, filters and resonators. Bandpass filters for several different applications that perform similar to or better than ceramic filters have been implemented for various applications. The filters are smaller compared to the cavity filters and much easier to construct and fabricate. Devices such as oscillators and amplifiers with all embedded passive devices have been implemented which helps achieve the noise specifications for various wireless communication standards.

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CHAPTER I

1. INTRODUCTION

The trend in the communications industry is to combine digital and radio frequency (RF) circuits into compact, low-cost, mixed signal modules which support high-speed communication channels and sustain the demand for increased bandwidth of data and information that flows through these channels.

The single most important architecture being pursued worldwide towards this endeavor is system-on-chip (SoC), also known as a single chip radio in the communications industry. The base band sections of current products have benefited from the SoC levels of monolithic silicon integration, while the RF/analog sections have continued to require a range of active device technologies combined with high performance passive components to provide matching, filtering and biasing circuitry. This need to combine different technologies in RF/analog functions has continued to be driven by exacting performance requirements, where a purely monolithic approach can involve too many performance compromises even with very exotic and revolutionary processing techniques.

Another area of concern besides active integration on the chip is the physical layer, which includes the chip, chip to package transitions, package, discrete components and the board. The package is the housing for the devices, a means by which devices communicate with the external world. Discrete components such as RF filters work together with the active components for enhanced communication. Other discrete components such as high quality passive devices form an integral part of oscillators and

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low-noise amplifiers, which form part of RF sub-systems. As the carrier frequency of modulated signals in wireless communications and the speed for digital communications increase, current and future devices present very demanding packaging requirements. The key performance requirements must be satisfied without compromising the fundamental and overriding need for low cost solutions. The selected package must also present the lowest possible electrical parasitics, and inherently linked to this, a large silicon efficiency [1]. A package for high bandwidth digital applications must also support a large number of input-output signals (I/Os) and ensure the lowest possible overall parasitic inductances. While RF package I/O counts may be small when compared to digital packages, these packages have stringent requirements on matched impedances, which imply minimal return losses and smooth RF transitions. The encapsulation materials employed in the package construction must be carefully selected to minimize any capacitance loading effects or unacceptable dielectric losses. The chip, package and discrete components must be compatible with standard surface mount assembly methods and provide good board level reliability. Lastly, the minimal number of package style variants should be employed for the ease and scalability of package design, manufacturing and business management and, for very high volume applications, should be available in industry standard formats from multiple sources to ensure security of supply and ready customer acceptance. Similar to SoC, the interconnection of chips with embedded functions in the package or the board is referred to as the system-on-package (SoP) architecture.

Although the packaging and semiconductor industry were projected to grow hand-in-hand towards producing highly integrated mixed signal systems, the single most actively

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pursued technology today is based on the SoC architecture. The reason for this can be attributed to the poor packaging efficiency of only 10-20% available in todays board level technology. (Packaging efficiency is defined as the ratio of silicon area to the total package area at the systems level. [1]) Since the 1970's, packaging has evolved from dual-in-line, wire-bond, and pin through-hole technologies to ball grid array, chip scale, and surface mount technologies in the 1990's. In parallel, the discrete components have shrunk in size with the smallest discrete capacitors and inductors measuring $1.2mm^2$ in size [2]. However, these advances in packaging which includes discrete components have not been able to compliment the growth in the semiconductor markets. Since a large fraction of the board area is occupied by discrete components in RF and mixed signal systems, a method for improving packaging efficiency is to eliminate the discrete components on the board.

1.2 Discrete and embedded passive components

Discrete passive components such as inductors, resistors, capacitors, filters, and resonators currently dominate the component count in most RF and mixed signal electronic products. While the cost of discrete passive components may be low, the cost of all the components on total product cost can be significant. In addition discrete components increase the board area. For example a typical cellular phone product may include well over one hundred passive components, with less than 20 active devices [3]. The passive components can occupy up to 80 per cent of the printed circuit board area and contribute up to 70 per cent of the product assembly costs. In addition, discrete components have large tolerances and parasitics and there is a constant need for the

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development of design rules for a multitude of packaging styles such as surface mount devices (SMD), chip-scale packages (CSP), land-grid arrays (LGA) and ball grid array (BGA). These packages are common methods for packaging discrete components.

A method for eliminating the surface mount discrete components is by embedding the passive components into the layers of the package or board as shown in Figure 1.1.

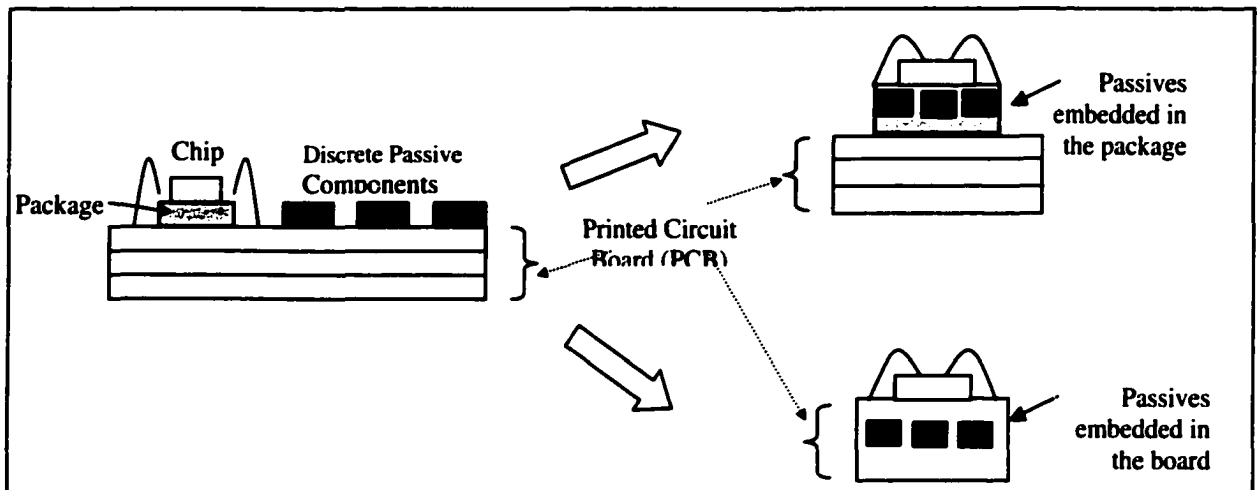

Figure 1.1. Passive component integration in the package and the board

Technologies that enable the integration of passive components therefore have a potential for the:

1. Reduction in circuit board area and weight
2. Increase in functionality for a given product size
3. Increase in the manufacturing line throughput
4. Reduction in the inventory and improvement of product reliability
5. Reduction in the functional block and system level costs
6. Enhanced design ease by eliminating the problems associated with lead and pad parasitics, matched impedances, higher tolerances for devices and reduction in the number of packaging style variants

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These integrated packaging technologies can serve as a highly functional platform on which the optimal set of active devices for the required RF and digital functions can be attached for the realization of future micro-systems.

However, different systems and sub-systems place varying constraints on the passive devices in terms of tolerance, quality, value, size and operating frequency. Table 1.1 shows an example of the different requirements for inductors and capacitors for various applications.

Application	Required range for capacitors and inductors	Desired unloaded Q Factor	Tolerance	Frequency	Comments
Filter & Matching Circuitry	$0.01 \leq C \leq 100pF$ $0.5 \leq L \leq 100nH$	>150	<2%	0.01-8GHz	• High Self Resonant Frequency • High unloaded q-factors • Tight Tolerance Required
RF Bypass Caps.	$0.001 \leq C \leq 0.1\mu F$	>50	<15%	DC-8GHz	• Low impedance (<<1 Ω)
Decoupling Caps.	$0.001 \leq C \leq 1uF$	N/A	<15%	N/A	• Low inductance, low impedance
RF Choke L	$0.1 \leq L \leq 1uH$	>15	<10%	0.01-10GHz	• Low resistance (<<1 Ω)

In Table 1.1, the unloaded quality factor (Q) is a measure of the performance of a passive device and is the ratio of the stored energy to the loss in the device. In Table 1.1, the passives with high Q and low tolerances are the most difficult to implement using standard semiconductor and packaging or board level technologies. Section 1.5.4 of this chapter further expands on the need for high quality factor passive devices in current and future wireless standards. Since the push for SoC has always been historically greater than SoP, the first attempt towards integration was to integrate passive devices on silicon. The primary disadvantage with this approach is that passive devices such as inductors consume a major part of the expensive silicon area. In addition, the losses in the silicon substrate and the thin aluminum metallization limit the performance of inductors and

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capacitors. An unloaded quality factor in the range 5-15 for spiral inductors and an unloaded quality factor of 20-30 for capacitors have been reported for devices integrated on silicon [4]. Currently technologies are being developed to integrate passive devices such as inductors on silicon using non-standard materials and process technologies that use thicker aluminum, copper metalization, high-resistivity silicon and sapphire substrates. However, the increase in Q for inductors has not scaled with the increase in processing complexity. An alternate approach, as suggested earlier and shown in Figure 1.1, is to embed inductors and capacitors requiring high unloaded Q in the package or in the printed circuit board (PCB).

Low-temperature co-fired ceramic (LTCC), thin-film deposition on glass/silicon/ceramic (also called multi-chip module deposition, MCM-D) and laminate multi-chip module (MCM-L) technologies have become the most prevalent choice for integration of passives into the package. The advantages and disadvantages of these technologies for integrating passives are discussed in the following sections.

1.3 Low-temperature co-fired ceramic technology (LTCC)

LTCC technology [5] is a multi-layer ceramic process. The ceramic layers are tape-cast in their pre-fired "green-state" and the tape is cut to the required size. Registration holes, via holes and cavities are then punched or drilled into the different tape layers. The via holes are normally filled, often with silver, and then thick film processing is used to print metalization patterns on each, or selected tapes. When the common thick film processing is used, the minimum line width/gap is around 100μm. The different layers are then inspected, registered and laminated and then co-fired at around 850°C.

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Electrically LTCC has a number of advantages, namely:

- Lower loss dielectric ($0.003<\tan\delta<0.009$ from 1-10 GHz)
- Better controlled dielectric properties (ε_r, $\tan\delta$ and thickness)
- Assembly of bare dies on LTCC modules
- Mixed dielectrics that allow for the integration of different product specifications on a single module
- Possibility for a large number of layers (>50)
- LTCC processes allow for the integration of passive devices such as inductors and capacitors. For example,
    - Inductors from 1nH-25nH have been fabricated and tested by companies such as National Semiconductor using 20 layer processes [5]. The highest Q obtained for the 20 layer process is ~150 using straight "resonators" for inductors in the range of 1nH–3nH [5]. Typical Q's are ~ 50, with a tolerance of 20% [6].
    - Interdigitated capacitors or dual plate structures have been fabricated with capacitance < 1 pF and multiple plate capacitors with high dielectric constant ceramic material have been fabricated with capacitances up to 30 pF for filter applications. The tolerance is ± 5%. The unloaded Q's are in the range of 50 – 200 [5].

A conceptual 3D integrated transceiver module functioning at 5.8 GHz, which uses a 20-layer LTCC process from National Semiconductor, has been discussed in [5]. The cross-section of the integrated module is shown in Figure 1.2a. Three different layers for transceiever, filter and antenna are vertically stacked and connected through vertical vias.

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The antenna and filter are directly fabricated in the module using LTCC technology for reducing the size and interconnection losses. The antenna, filter and transceiver utilize 8, 12 and 2 layers respectively. The filter uses two coupled embedded inductors and five parallel plate capacitors. The total size of the module is 14 x 19 x 2mm^2. A photograph of the integrated module is shown in Figure 1.2b.

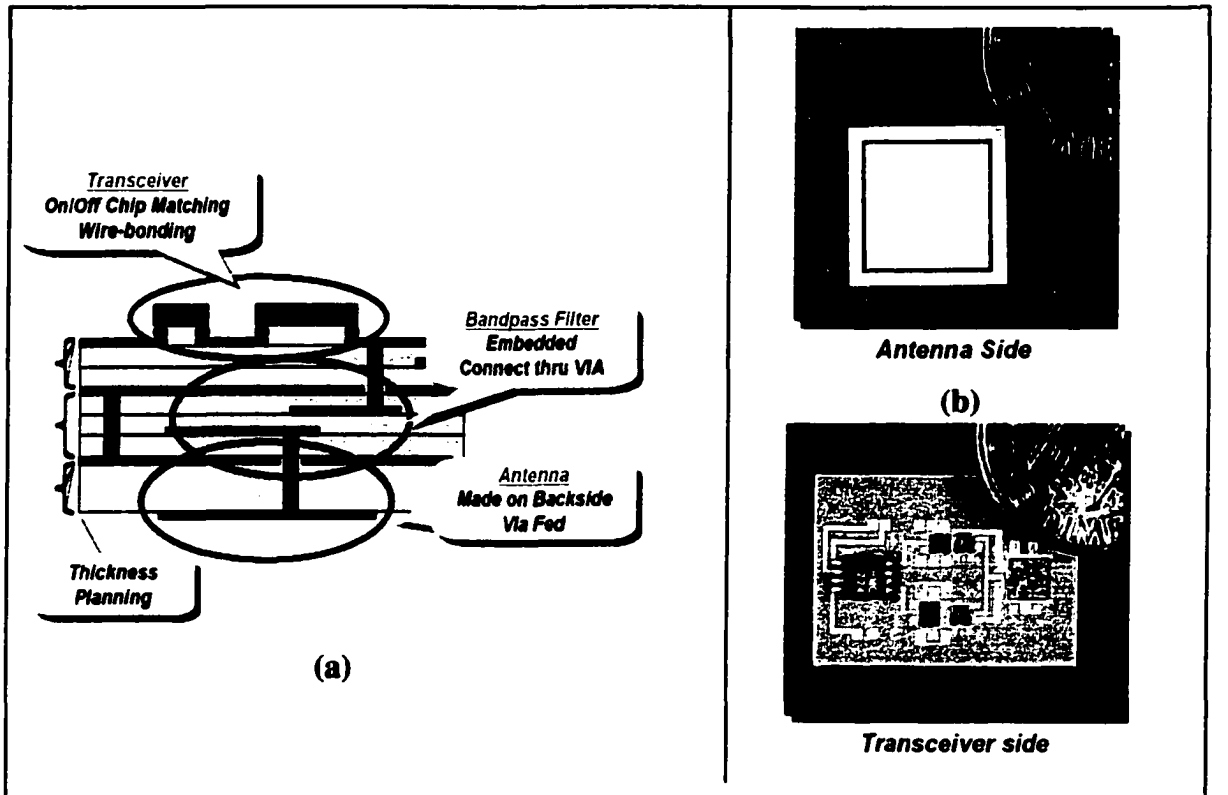

Figure 1.2. a) 3D integrated LTCC module with cavity backed antenna and bandpass filter b) Photograph of the integrated transceiver module for 5.8 GHz

Though LTCC has many advantages some of the disadvantages are:

- RF characterization data, for both the integral passive components and the material, are not often available
- During the firing process there is tape shrinkage of between 12% and 16% in the X and Y dimensions and a larger amount in the Z direction

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- The high temperatures associated with the processing adds process complexity and thereby increases cost
- Commercial manufactures can currently have an automated system for 5" x 5" parts [6]. Athough the use of LTCC substrates for packages with embedded components and attached chips is justified, it currently cannot be used for the replacement of an entire board for commercial wireless applications. All LTCC modules are almost always mounted on a larger carrier which is generally processed using laminate technology, which is currently automated for 18" x 24" panels.
- Medium to high dielectric constant material (>7.8 [6]) prevents the realization of high speed digital interconnects. The high dielectric constant also increases the parasitic capacitance for devices such as inductors limiting the Q for inductors to 150 [5].
- Although the limit on Q from dielectric loss for capacitors is as high as 300, the Q realized is only 200 due to the following reasons:
    - Thin metallization levels of 2-5um increases the conductor losses in the devices
    - When using parallel plate capacitors the use of vias which are typically 4mils in diameter and 3.8mils in height adds to the inductance and reduces the effective capacitance
- Solid ground-planes are difficult to fabricate due to warpage issues

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- The minimum tape thickness available in production is 3.8 mils (fired) while the thickest tape is approximately 8 mils fired. Multiple dielectric layers would therefore have to be used to provide for thicker fired layer dimension.
- Smallest via size in a typical process is limited to 4 mils, which may be insufficient for high density requirements in the future. In addition, larger vias through a thicker dielectric adds to the parasitics of interconnects.

1.4 Polymer Thin film or Multi-chip module deposition (MCM-D)

In this technology, thin (<15um) polymer dielectric films are deposited on a stable base substrate such as silicon/glass or alumina. Thin (2-5um) conductor film, usually copper, is then deposited and processed photolithographically. The lower dielectric constant of the polymers (Polyimide) and 5um-15um thick dielectrics make 50 Ohm lines more practical. In [7] the authors have presented a MCM-D module for embedded passive devices. The technology in [7] consists of sputtered metal layers (3 um thick) separated by thin spun-on layers of BCB (5um thick), which has a dielectric constant of 2.65 and a loss tangent of 0.0008. The BCB is stacked on a glass carrier substrate, which

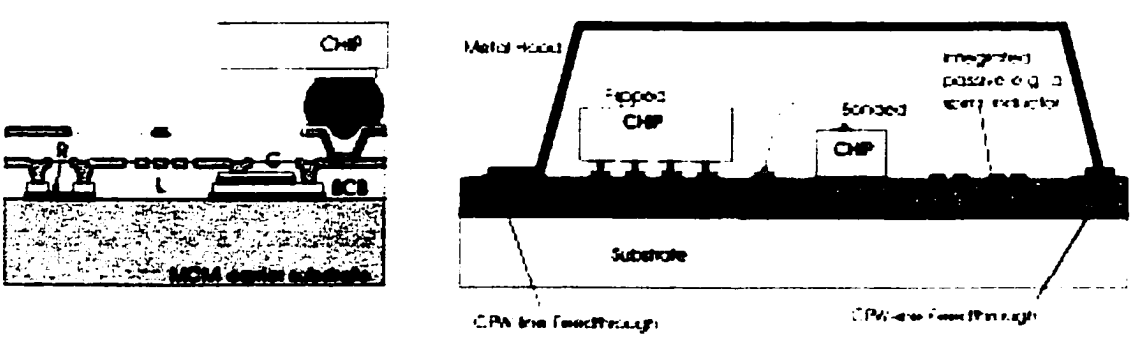

Figure 1.3. Cross-section of a MCM-D substrate and a schematic of possible mounting solutions [7]

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has a dielectric constant of 6.2 and a loss tangent of 0.0009. The cross-section of the substrate and supported assemblies are shown in Figure 1.3 [7].

The advantages of MCM-D technology are the following:

- Narrow line widths are possible (~10um)
- Small to medium via holes can be fabricated (10-50um).
- The process interlayer polymer dielectric material can be employed for achieving small capacitors with capacitance density of ~ 5pF/mm^2 for typical layer thicknesses. These capacitors have a very high Q >200 because of the low loss properties of the substrate. Intermediate capacitance values can be realized with plasma deposited silicon nitride films that have very good RF performance. Higher value capacitor components, principally for RF decoupling functions, can be realised with anodized aluminium oxide or tantalum oxide films with capacitance density of 500pF/mm^2 and above [8].
- Through careful inductor design optimization and prudent choice of materials, inductor quality factors from 40 to 100 in the frequency range of interest can be achieved for inductor values between 0.5nH-20nH with self resonant frequencies between 2.5 and 15GHz [7].
- High self-resonant frequencies for capacitors and inductors can be achieved due to small form factor of the devices.

Though MCM-D has several integration and size advantages, the disadvantages of MCM-D technology are as follows:

- No through-holes which limits the possible packaging formats to CSPs, BGAs and wire-bonded devices.

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- It is difficult to fabricate beyond two metal layers, which limits the design of inductors and transmission line interconnects to a coplanar waveguide topology. In [7] the authors have indicated that the CPW topology allows for greater freedom compared to a microstrip and stripline configuration due to the variable spacing the between the ground and signal lines. However, the thin metallization level of 2-5um increases losses significantly in a CPW topology, lowering the Q of inductors.
- The limit on Q from dielectric loss for capacitors is ~ 400 with standard dielectrics but conductor losses reduce the Q to ~200.
- This is a high cost, high temperature process (400 °C < T< 600 °C)
- The manufacturing is currently limited to 4-6 inch wafers compared to 18" x 24" panels in standard laminate technology.
- It requires a glass core for realizing high Q passive devices, which adds further to the cost and processing complexity.

The next section discusses laminated multi-chip module (MCM-L) technology, which is the focus of this research. It is a technology, which has been disregarded as a choice for embedded passive devices for RF applications due to the inadequacies of the materials used in the past. However, the next section introduces recent advances in laminate technology with an emphasis on density and dielectric materials.

1.5 Laminated Multi-chip module Technology (MCM-L)

MCM-L technology is currently the technology of choice for the fabrication of printed circuit boards. A thick copper-cladded (9um-35um) FR-4 organic substrate (epoxy-glass fiber composite) is used as the core laminate. Etching copper, which is

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cladded on the laminates or using electroplating baths, forms the line patterns. Each copper level is insulated from the other using thin-film epoxy-glass composites (25um-100um). The layers of conductors and organic dielectrics are laminated together using vacuum pressure type laminators and then heat cured. Appendix A discusses the process steps in more detail.

Some of the processing and electrical advantages of MCM-L technology are as follows:

- Lowest cost due to the inherent low cost of the materials and lower temperatures of processing (<250°C) compared to 800°C (LTCC) and 450°C (MCM-D)
- Large area (12" x 18", 18" x 24") processing further reduces cost compared to the smaller area LTCC and MCM-D processes due to the economies of scale involved
- Recently standardized higher packaging densities allow for 1mil wide lines with 1mil spacing with 1mil diameter vias for dielectrics as thin as 1 mil which exceeds the densities in ceramic technology and compares well with MCM-D technology
- Arbitrary layer thicknesses (10um to 1mm) allows for realizing mixed signal modules that combine RF and digital functions
- High conductivity copper metalization 10um-35um helps reduce DC losses in transmission lines and passive devices compared to the losses in deposition and ceramic processes
- Through vias are possible for direct backside connection
- Organic/polymer dielectrics offer the benefits of low dielectric constant (ε_r = 2.0-4.0), leading to higher signal propagation speeds, as shown in Figure 1.4 [8,9].

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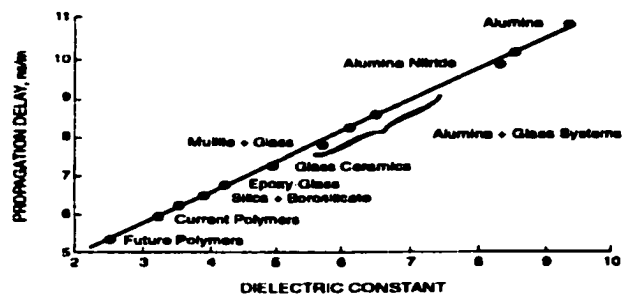

Figure 1.4. Propagation Delay vs. Dielectric Constant for Various Dielectric Materials [9]

The primary disadvantage with the MCM-L technology when using low-cost epoxy based laminates are as follows:

- Epoxy-glass laminate are the lowest cost materials and consequently hold a large market share in package substrates and PWBs. However, traditionally the relatively high loss tangent (0.015-0.025) of epoxy laminates and films limits their use to digital systems operating below 1 GHz.
- The highest Q achievable for capacitors using these dielectrics is on the order of 60 at 1GHz and degrades at higher frequencies.
- These epoxy based dielectrics also exhibit frequency dependent electrical behavior which is not suitable for integrating passive devices for RF applications.

A new breed of polymer laminate dielectrics are emerging to fill the gap between low-cost epoxy dielectrics and high-end, expensive materials like polytetrafluoroethylene (PTFE). These include polyphenyl ether (PPE) based materials, liquid crystalline polymers (LCP), and lower cost polymer and ceramic filled composites. Table 1.2 lists these new dielectric polymers along with their dielectric properties at high frequencies. The research program at the Packaging Research Center (PRC) at the Georgia Insititute of Technology (GIT) is evaluating

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these new materials for use in mixed signal SOP applications at frequencies up to 20GHz and beyond.

Table 1.2. Common Low Dielectric Polymers and their Electrical Properties

Material	ε_r *(1 GHz)*	*Tanδ @ 1 GHz*
Dupont Vialux™(epoxy-glass based))	3.3-3.7	0.015-0.025
Asahi A-PPE™ (PPE based)	3.5	0.007
Rogers Zyvex™ (LCP based)	2.95	0.002
Polymer ceramic composites	10.75	0.08-0.1

When considering materials such as A-PPE™ and Zyvex™, the possibilities for integration are immense because of the comparable low loss nature with materials used in LTCC and MCM-D. A maximum unloaded quality factor for capacitors as high as 110 for A-PPE™ and 500 for Zyvex™ can be achieved unlike MCM-D and LTCC processed capacitors where conductor losses reduce the maximum available Q's significantly. The capacitance densities when using the available thicknesses of the laminates is ~1pF/mm^2 which is again comparable to LTCC and MCM-D processes.

However, the commonly associated process variations with MCM-L processes (such as varying dielectric thicknesses during lamination, heating and curing, non-uniform conductor profiles and uneven metallization levels) have detered the RF industry from even suggesting the use of the newer laminate materials like A-PPE™ and Zyvex™ for embedded passive devices, despite the fcat that these materials have low losses and stable dielectric behavior.

However, if a design for manufacturability (DFM) approach is adopted ensuring controlled and predictable process attributes, materials such as Zyvex™ and A-PPE™ can

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provide replacements for ceramic and deposition technologies for many applications where epoxy-based materials have failed. These solutions can result in a lower-cost alternative to LTCC and MCM-D technologies for RF systems. Moreover, the materials used in laminate technology and shown in Table 1.2 have an inherent lower dielectric constant compared to all the materials used in ceramic technology making them also a better choice for high-speed digital applications. Though high Q passive devices associated with Zyvex™ and A-PPE™ are needed for some RF systems, other applications may not require such specifications. Materials such as Vialux™ which can provide Q's ~ 60 can be used as an even lower cost alternative to Zyvex™ and A-PPE™ for integrating passive devices.

The earlier sections have discussed the state of the art LTCC and MCM-D technologies, which can provide unloaded Q's for inductors and capacitors as high as 150 and 200, respectively. This serves as a good starting point for the specification for the inductors and capacitors in MCM-L technology. However, these Q factors may not be adequate for current and future RF applications. The next section discusses the specific demands that wireless systems place on passive devices and elaborates on the issues that need to be addressed.

1.6 Systems and Sub-systems for Wireless Applications

For digital applications, the performance of the substrate is judged based on delay, attenuation, and noise that signals experience when traveling from chip-to-chip over electrically long distances. However, the performance criteria for substrates used in RF applications change based on the system, architecture, and standards used. In this

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dissertation, the requirements for passive devices have been limited to front-end wireless receiver architectures.

Heterodyne and image-reject receivers are front-end architectures that are currently used in wireless products [10]. Digital IF and sub-sampling receivers are a few of the other architectures being investigated by the telecommunications industry [10]. The following sections provide a comparison of the heterodyne, homodyne and image-reject receiver architectures.

1.6.1 Heterodyne Receivers

A heterodyne receiver is perhaps the most traditional design for a receiver. It is primarily used to relax the need for an extremely high Q channel select filter. This is done by translating the high frequencies to lower frequencies using a mixer, which in its simplest form is an analog multiplier. A typical heterodyne architecture is shown in Figure 1.5 [11].

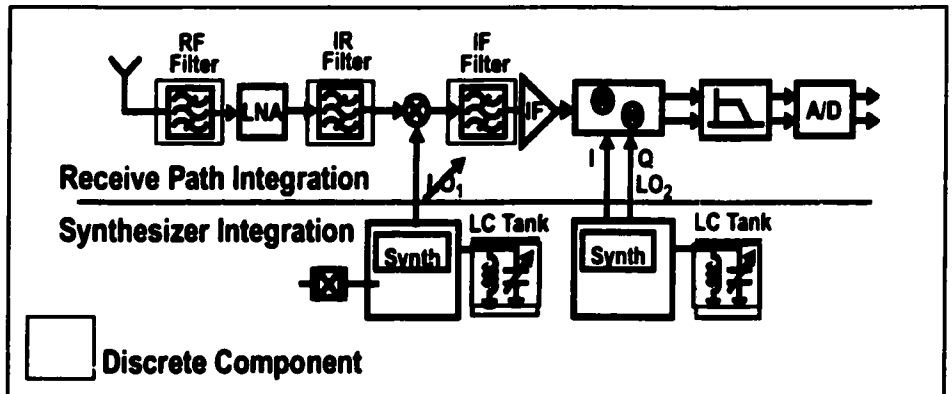

Figure 1.5. Super-heterodyne wireless receiver architecture

The RF front-end filter helps remove the out-of-band energy and performs rejection of image-band signals. The noise or image-rejection filter (IR filter), which follows the

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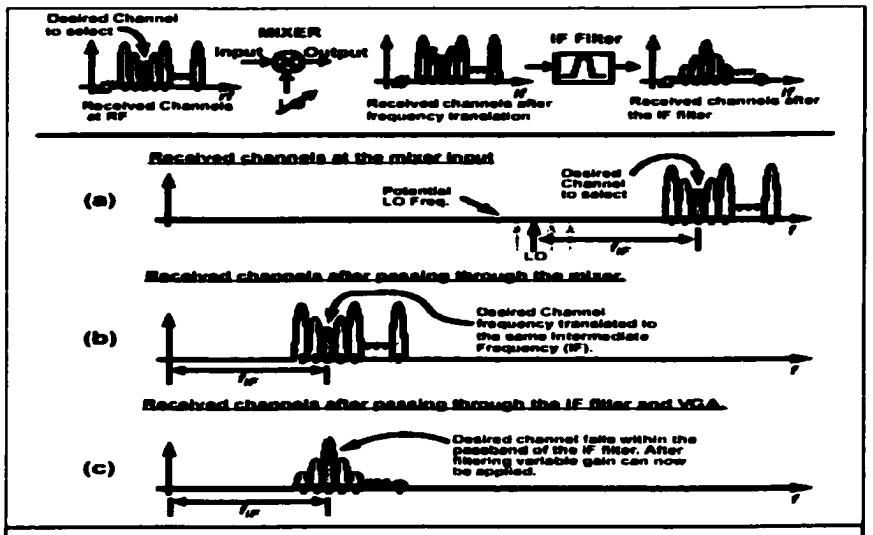

Figure 1.6. Signal Spectrum through a super-heterodyne [11].

low-noise amplifier (LNA), further attenuates the undesired signals present at the image frequencies. An RF channel-select frequency synthesizer tunes the desired band to a fixed intermediate frequency where a filter performs a first order attenuation of out-of-channel energy. This translation is explained in Figure 1.6.

The following are some of the advantages of the heterodyne architecture:

1. Relaxed loaded Q (loaded Q for a filter = Center frequency + 3dB Bandwidth) on channel-select filters by having more than one band-select filter. Relaxing the loaded Q helps reduce the insertion loss of the filter as given by equation 1.1. Ignoring radiation and mismatch loss, for a single resonator bandpass filter,

$$\text{Insertion Loss (dB)} = 20 \times \log [Q_U + (Q_U - Q_L)] \qquad (1.1)$$

Where, Q_L and Q_U are the loaded Q of the filter and the unloaded Q of the resonator, respectively.

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Since, the Noise Figure (NF) for a filter is its insertion loss in dB, reducing the insertion loss helps reduce the overall NF of the system.

2. The frequency at which I and Q phases are separated is about one or two orders lower than in the homodyne counterparts. This makes the two paths much less sensitive to mismatches.
3. Careful selection ensures maximum selectivity and sensitivity compared to any other architecture [10].
4. Each component can be used as a stand alone component and scaled to other architectures and system needs. This reduces time to market for subsequent designs and architectures.

The following are some of the disadvantages of this architecture:

1. Since the gain and NF of each stage depend on those of the previous stage, careful iteration is necessary. For example: the gain of the LNA is degraded due to the 50ohm input impedance of the filter in the next stage. Ideally, infinite output impedance is desired.
2. This architecture requires too many external components such as the RF, IF and IR filters.

The challenge of fully integrating a receiver is to replace the functions traditionally implemented by high performance, high-Q discrete components with integrated on-chip or off-chip solutions.

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1.6.2 Direct-Conversion or Homodyne Receivers

The direct-conversion receiver eliminates many of the discrete components because all of the in-band channels are frequency translated from the carrier directly to base-band using a single mixer stage. Energy from undesired channels is removed with on-chip filtering at baseband. In a direct conversion receiver, the IF stage is eliminated as is the need for image-rejection filtering. Although ideally suited for monolithic integration homodyne receivers, suffer from various problems, which are listed below:

1. Since the front-end band-pass filter and a low-pass active filter accomplish the rejection of all out-of-channel interferers, there is added pressure on the design and specifications of these devices. The front-end filter requires a high loaded Q and also very high attenuation of the unwanted signals, which is currently accomplished using bulky ceramic resonators (>1000mm^3) coupled to each other.
2. DC offsets due to coupling of "LO leakage" through substrate and capacitive coupling from mixer to LNA.
3. I/Q mismatch is one of the most severe problems in this architecture since the I and Q components have to be separated at the carrier frequency.

1.6.3 Image-Reject Receivers

An architecture that alleviates many of the DC offset problems that plague direct conversion receivers is the Low-IF receiver architecture, shown in Figure 1.7 [11]. Similar to direct conversion, a single mixer stage is used to frequency translate all of the desired channels to a low intermediate frequency (IF) which is on the order of one or two

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channel bandwidths. The primary advantage of a low IF system is that the desired channel is offset from DC. Therefore, the typical problems arising from DC offsets may be bypassed [11]. This architecture is one of the most widely used architectures in present CMOS processes. It offers the advantage of complete integration, which ties well with the goal for a SOC architecture. However, it does suffer from a few disadvantages and design constraints. In the low IF receiver some method of image-rejection must be performed because the desired carrier is down-converted to a low IF. This is accomplished by using some variant of an image-rejection mixer, which are most commonly the Weaver and Hartley mixers. A major problem that the Hartley and Weaver architectures share is incomplete image rejection due to gain and phase mismatch [10].

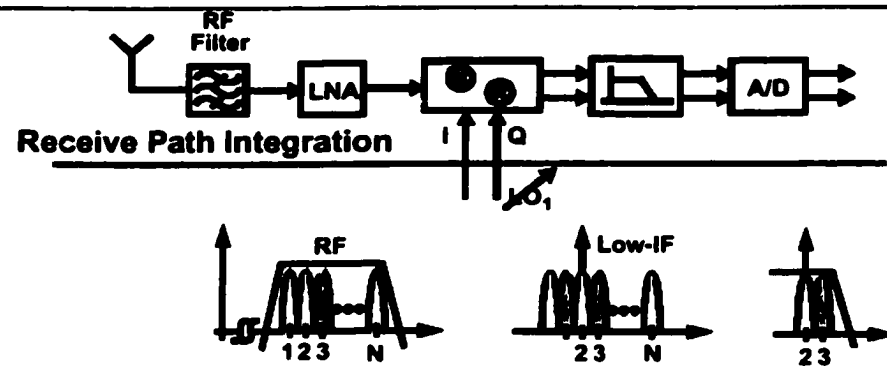

Figure 1.7. Low-IF Receiver System and Spectrum Flow [11]

Although ideally suited for monolithic integration, low IF receivers suffer from various problems, which are listed below:

1. Since the IF is on the order of the channel bandwidth, all of the image band attenuation must be performed by an on-chip image-rejection mixer where the image rejection is limited by matching considerations to ~30dB.

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2. Any additional image frequency attenuation needs to be accomplished by the front-end filter. This is accomplished by adding extra resonator elements to the filter, which adds to the loss of the filter and also increases the size of the device significantly (>1000mm^3).
3. The major problem is the performance compromise due to the reduction in the number of external components in a homodyne or image reject architecture. Key design considerations need to be made to minimize external components while maximizing the signal to noise ratio. For the LNA an external input and output matching network is almost always used which provides the lowest input noise figure. Having external circuitry is crucial at the input and output of the LNA. Noise figures close to the minimum possible noise figure can only be achieved with stand alone components with unloaded Q-factors greater than 50 [12]. However, when using on-chip passives with Q's as low as 5-10 the noise figure increases by a factor of 2 to 3. All other circuitry such as bias, interstage and output matching can be integrated into the device [13]. High-quality, low phase-noise voltage controlled oscillators (VCOs) are typically realized with discrete-component high-Q inductors, crystals, ceramic resonators and varactor diodes. Even using other technologies such as Gallium Arsenide (GaAs) and Silicon Germanium (SiGe) does not solve the problem of low quality passives as they provide Q's only as high as 30.

It is also important to note that the design of filters in all architectures required at the front end is becoming a major problem since center frequencies are scaling towards the

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multi-gigahertz range for most RF standards. This drives the loaded Q for filters higher, which increases the need for higher unloaded Qs for maintaining low insertion losses.

1.6.4 Common design issues in wireless receivers

Based on the discussions in the previous sections, some of the issues that need to be addressed for current and future wireless receivers are:

1.6.4.1 Integration of the front-end RF bandpass filter

Currently the most prominent technology of choice for front-end RF filters are multi-layer ceramic filters and ceramic cavity filters. Ceramic cavity filters provide very high attenuation, low insertion losses and narrow bandwidths. However, the form factors associated with cavity filters are extremely large. Multilayer planar filters can have a volume 1/40th that of ceramic cavity filters and are being developed for cellular telephones, data communication equipments, and digital cordless telephones, where narrow bandwidths and large roll-offs are not required [14]. Shown below in Table 1.3 is a comparison of filters in ceramic technology with a few examples of products currently available:

Table 1.3. Comparison of Ceramic Cavity and Multilayer Ceramic Technology

Type	*Center Freq (f_o). (Application)*	*1dB and 3dB Bandwidth (BW)*	*Insertion loss in 1dB band*	*Size*	*Attenuation*
1) 5 layer ceramic filter	1.9 GHz (W-CDMA)	60 MHz and 120 MHz	3.0dB	18mm^3	40dB at f_o-400 MHz
2) 3 section ceramic cavity filter	2.4 GHz (IEEE 802.11b)	60 MHz and 90 MHz	1.6dB → 2.4dB →	700mm^3 300mm^3	40dB at f_o±200 MHz
3) 5 layer ceramic filter	2.4 GHz (Bluetooth)	100 MHz and 300 MHz	2.5dB	18mm^3	30 dB at f_o-300 MHz

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As seen in Table 1.3, the attenuation achieved with the ceramic filter is large at the undesired frequencies compared to the multilayer filter. However, the size of the cavity filter can be 50 times larger than the multilayer filter if very low loss is desired.

The filters shown in Table 1.3 represent state of the art filters available in ceramic technology, but come with the disadvantage of higher costs due to the processes used in making multilayer ceramic packages or cavity based structures. Examples of filters implemented in MCM-D technologies compare well with multilayer ceramic filters with slightly higher losses, but cannot provide the combination of low loss and roll-off available in the cavity filters.

Equation 1.1 provides an estimation of the unloaded Q required for a single resonator bandpass filter to achieve the desired loaded Q with a specific insertion loss. Front-end RF filters which require more than one resonator section such as those discussed in Table 1.3 can be simulated to provide an estimate of the required unloaded Q of individual components to attain the necessary loaded Q. For example, the loaded Q for filter #3 in Table 1.3 is $f_o/BW=8.0$. Figure 1.8 is an example of a coupled-resonator filter, which meets the specifications of filter #3 in Table 3 for Bluetooth applications operating at 2GHz. The inductors and capacitors have been simulated as non-ideal components in Agilent's Advanced Design Suite (ADS) [15]. Figure 1.9 shows the simulated S_{21} (insertion loss) and S_{11} (return loss) for the filter in Figure 1.8. As seen, a maximum unloaded Q-factor of ~150 is required for inductors with inductance values greater than 1nH,

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and a maximum unloaded Q-factor of ~100 is needed for capacitors with capacitances greater than 1pF. As mentioned in [5,6] and also in section 1.2 these are also approximately the highest unloaded Q reported for capacitors and inductors in ceramic processes. For any filter or device, which requires higher performance, current multilayer ceramic process would prove to be inadequate and the use of larger ceramic cavity resonators would be necessary.

Combline RF bandpass filters integrated into the FR4/epoxy based multilayer MCM-L substrates have been realized in [16] and satisfy the low-cost and compact realization requirements. Since the epoxy-based material exhibits high loss, the design required the use of two discrete ceramic capacitors. However, due to lack of proper characterization of the discrete capacitors the performance of the filters deviated significantly from the predicted results. Although the sizes of the devices in [16] are comparable to multilayer ceramic filters, the 3dB bandwidth for the filters are rather large (>450 MHz) and the roll-off is insufficient. In [17] the authors use coupled-inductive resonator filters, and eliminate the need for discrete capacitors. However, due to the long length of the inductor coils the loss in the filter was greater than 4dB for 3dB bandwidths greater than 400 MHz at ~2.45 GHz. While these results show promise for using laminate technology along with novel design ideas for filter applications, key design changes need to be explored to push the performance limits of epoxy-based laminates further that emulate or better the multi-layer ceramic filters. Another option would be to use the newer materials like Zyvex™ which could potentially provide Q's as high as 500 and serve as a replacement for the bulky ceramic cavity filters.

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While the Q's required for filter type applications are fairly high, other applications may not need such high performance from the passive devices. Examples of these circuits are LNAs and VCOs.

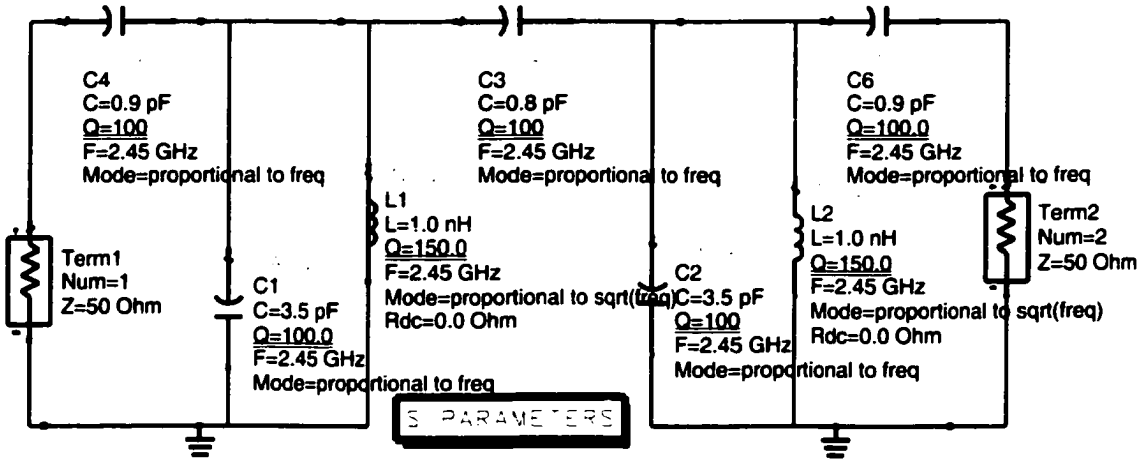

Figure 1.8. Schematic of coupled-resonator filter with non-ideal components.

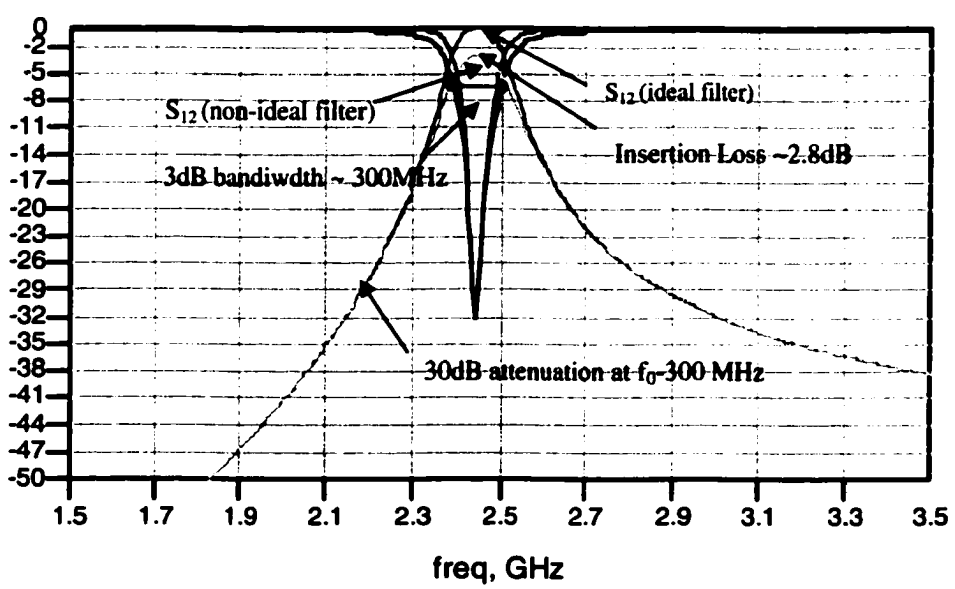

Figure 1.9. Simulation results for ideal and non-ideal filter. Simulations done in ADS

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1.6.4.2 Integration of the Low-Noise Amplifier

Low-noise amplifiers (LNAs) are internally biased devices, eliminating the need for external bias resistors and chokes. In a typical application as shown in Figure 1.10, the external components needed are the input and output matching networks; input and output blocking capacitors, and a V_{CC} bypass capacitor [13].

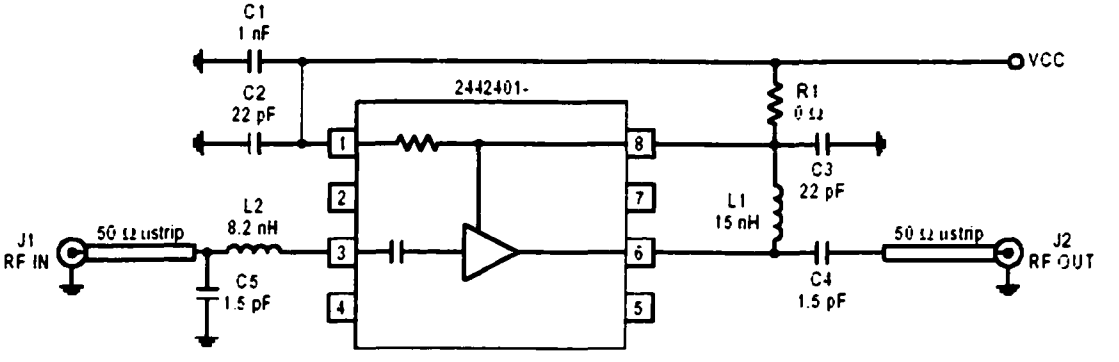

Figure 1.10. Schematic of a 900 MHz LNA application from RFMD showing the external components required for minimum NF [13]

Traditionally the input and output matching networks, blocking capacitors and bypass capacitors are implemented using discrete components. Similar to filters, most of the integration of these passive devices has been demonstrated using multilayer LTCC technologies and MCM-D technologies while little has been done to explore the fabrication of such devices using MCM-L technologies. The reason for using off-chip integration is because the NF of a LNA with inductor and capacitor Q's ~ 50 is 2-3 times lower than the NF obtained using on-chip passives where the Q's can be as low as 5 [12]. This decrease in NF is crucial to the success of long-range highly sensitive communication standards. However, it has also been shown in [12] that an unloaded Q greater than 50 for the passive

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devices decreases the NF only marginally. Since the unloaded Q's for the components that comprise the input and output matching circuits need to be ~ 50 the use of very low cost epoxy-based Vialux™ dielectric material which provide Q~60 is also a possibility. This can reduce the cost of implementing the devices significantly. Moreover, since the Q's required are not as high as those required for filters, design optimizations are possible for achieving the desired reactances and Q factors in very small form factors which are comparable to the smallest discrete passive components (~1.2mm^2).

Additionally, the gain of the LNA, which ideally requires infinite output impedance, is usually degraded due to the following 50 ohm input impedance of the IR filter in the following stage of a heterodyne architecture. By modifying the conventionally used L or Pi matching networks at the input and output of the LNA into bandpass networks while maintaining the matching conditions can help eliminate the need for the IR filter and also reduce the number of components. In an image-reject architecture, this would reduce the strain on the image-reject mixers which otherwise would only have ~30dB image rejection as the upper limit.

1.6.4.3 Integration of Oscillators

High-quality, low phase-noise oscillators are typically realized with discrete-component high-Q inductors, crystals, ceramic resonators and varactor diodes. Similar to the LNA, the authors in [18] show that the reduction in phase noise of an oscillator beyond a Q=80 for inductors is marginal. Once again little work has

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been done to explore the possibilities of using MCM-L technology with embedded passives for integrating the oscillator into the package or the board.

The other issue in realizing integrated passive devices, and always overlooked, is that there is no fast way to accurately model the embedded passive structures. Although empirical models found in advanced RF/microwave simulators may be fast, they are only limited to certain fixed geometries for simple embedded components. Moreover, they are available for mature technologies and are not relevant for new processes. Only EM solvers are suitable for a wide range of complex structures. However, even with today's rapid advancement in computer processors, currently EM tools are still very slow.

A fast and accurate technique is needed to model the parasitics related to embedded passive devices and then use the same technique to optimize their performance for the desired specifications and sub-systems.

1.7 Accomplished Research

Given the technical challenges arising in the use of multilayer MCM-L technology for the integration of wireless receivers, the following research work has been accomplished in this dissertation:

1. *Development of a method to characterize thin-film organic dielectric materials*
   This method uses a combination of parallel plate capacitors and transmission lines for characterizing dielectric materials as a function of frequency. These material properties are required for the design of embedded passive devices.
2. *Development of a method to model integral passives*

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This technique involves the segmentation of a complex passive device into multiple-coupled line sections and discontinuities, which can be individually modeled using a hybrid of quasi-static and full-wave techniques. This method works well in the frequency range 50MHz – 10 GHz for the structures studied. The modeling technique enables the incorporation of process variations such as non-uniform signal lines, conductor roughness, and dielectric constant variation as a function of frequency. This method works well for passives configured in a microstrip, stripline or coplanar waveguide topology. The method enables the development of models that include frequency dependent loss effects such as skin-effect, current-crowding, and loss tangent through interpolation techniques.

3. *Demonstration of very high-Q embedded inductors in epoxy based organic substrates*

   The inductors use aggressive features such as 2 mil microvias and 2 mil lines with 2 mil spaces. This ensures small device sizes ideally suited for integration with other devices. The results also show that the performance of inductors is weakly dependent on the loss of the materials and strongly dependent on the conductor type and conductor thicknesses. Using the information from the fabricated inductors, design rules have been developed for the implementation of high-Q inductors for RF communication standards such as GSM (900 MHz and 1800 MHz), Bluetooth (2.4 GHz) and Hyperlan (5.1-5.8 GHz).

4. *Demonstrated the need for newer organic materials for embebbed capacitor applications*

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Capacitors require much lower loss tangent dielectric materials as compared to inductors for achieving similar Q-factors.

5. *Comparison of dielectric materials for integral passive devices*

   The dielectric materials, Dupont Vialux™, Rogers Zyvex™ and Asahi PPE™ were compared based on loss tangent, dielectric thickness and dielectric constant for inductors, capacitors and filters. The Rogers Zyvex material evaluation was done as a result of a contract between Georgia Tech and the Army Missile Command (AMCOM). This particular research effort was led by Dr. White at the Packaging Research Center, Georgia Tech.

6. *Demonstration of RF filters*

   Filters with integral passives in organic substrates have been implemented for standards such as Bluetooth, IEEE 802.11b and W-CDMA applications as mentioned in Table 3.

7. *Design of integrated sub-systems*

   Integration of filters and low noise amplifiers can result in significant reduction in number of components. The impedance matching networks required for a discrete LNA can be integrated into the filter, thereby effecting a 30% reduction in the total number of embedded components. An example of an integrated bandpass filter and amplifier has been presented. In addition, the use of integrated passives in the design of active circuits such as oscillators and amplifiers have been studied for operation in the 2 GHz range.

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1.8 Dissertation Outline

The remainder of this dissertation is organized as follows. As the first step towards re-evaluating this technology for embedded RF passive applications, process parameters such as signal line profiles, conductor thickness, dielectric thickness variations, etc. were studied using several test vehicles processed under different conditions. Design rules were established which ensure low tolerances, repeatability and manufacturability. Next, the primary materials under consideration were characterized using different techniques. The processes, development of design rules and the characterization of materials, such as Dupont Vialux™, Rogers Zyvex™ and Asahi PPE™, are discussed in Chapter 2. In Chapter 3, the modeling of inductors and capacitors using a combination of fullwave and quasi-TEM techniques is presented. The design and comparison of inductors and capacitors on different substrates is discussed in Chapter 4 followed by the design and comparison of RF and IF filters on different substrates in Chapter 5. The section on filters will also include the analysis of key interconnects and the construction of equivalent circuits for filters which include several passives and interconnects. The design of low-noise amplifiers and oscillators is discussed in Chapter 6. Finally Chapter 7 concludes this dissertation and recommends future work.

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CHAPTER II

2. MATERIAL CHARACTERIZATION

Introduction

The design of devices and modules using new technologies requires the availability of electrical properties of the dielectric material used. A characterization method is therefore required to obtain the frequency dependent properties of the dielectrics, which includes both the permittivity and dielectric loss.

A popular and widely used characterization technique is the utilization of transmission line and waveguide resonators [19]. The major problem with this method is that the dielectric constant and loss tangent can be estimated only at discrete frequency points where the structures resonate. Moreover, if the resonant frequency is not close to the designed frequency (f_o), the shift in resonant frequency ($\Delta f_o/f_o$) is related to the error in the measurement of the dielectric constant using the relation, $\Delta\varepsilon_r/\varepsilon_r=(\Delta f_o/f_o)^2$, because f_o is proportional to $1/\sqrt{\varepsilon_r}$, where ε_r is the relative permittivity of the dielectric [19].

Unlike the method in [19], the dielectric can be characterized as a continuous function of frequency using the method discussed in [20] and no assumptions are made regarding the permittivity of the material. This chapter discusses the method presented in [20] in detail along with its application to the structures and dielectric materials used in this dissertation. In addition, a few more characterization methods have been discussed which have been used to verify the results.

2.1 Characterization method for MCM-L dielectrics

In [20], two transmission lines with the same characteristic impedance are used, where the characteristic impedance can be different from 50 ohms. One line is longer than the other by

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a distance Δd. For both lines the measured two port parameters, M expressed in ABCD matrix form can be considered as a product of three parts: an input matrix X including the probe-to-line transition, transmission line T and an output matrix Y including the line-to-probe transition:

$$M_1 = XT_1Y \tag{2.1}$$

$$M_2 = XT_2Y \tag{2.2}$$

where M_i, X, T_i and Y are ABCD matrices for the corresponding sections, shown in Figure 2.1, for the two different line lengths.

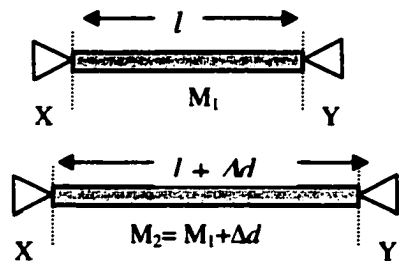

Figure 2.1 Two transmission line technique used to characterize materials

Multiplying the matrix M_1 by the inverse of M_2, and assuming X=Y, the following equation is obtained

$$M_1 M_2^{-1} = XT_1T_2^{-1} X^{-1} \tag{2.3}$$

Since (2.3) is a similar transformation,

$$Tr\,(M_1 M_2^{-1}) = Tr\,(T_1 T_2^{-1}) = 2\cosh(\gamma_{meas}\Delta d) \tag{2.4}$$

where, γ_{meas} is the complex propagation constant of the transmission line and Δd is the length difference in the two transmission lines. Although the method described in this section can be used to extract γ_{meas} using (2.4), a suitable structure is required. In the next section, the rationale for choosing the grounded coplanar waveguide (GCPW) transmission line or hybrid

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coplanar waveguide microstrip (CPWM) transmission line for material characterization is discussed.

2.2 Grounded CPW transmission line

Since ground-signal-ground (GSG) probes are considered most suitable for high frequency signal launches, it is appropriate to have coplanar waveguide (CPW) transmission lines for characterization in order to eliminate pad-to-line discontinuities. These discontinuities produce errors, which would require de-embedding if microstrip or stripline transmission lines are used. A CPW transmission line is one where the ground is coplanar with the signal lines as shown in Figure 2.2 with dielectrics above and below the transmission line.

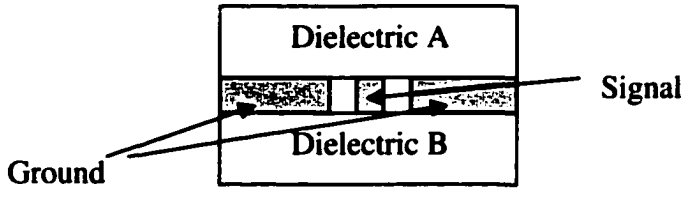

Figure 2.2 CPW transmission line

However, a pure CPW line without conductor backing introduces another interface between the build up material and the core that could cause errors in the interpretation of measurements. A core dielectric is a requirement for MCM-L processes and is used for rigidity, as explained in Appendix A. However, a conductor backed CPW line is problematic because of the higher order parallel plate modes that can be introduced between the ground and the conductor backing. The use of the CPW-microstrip (CPWM) or grounded-CPW structures (conductor backing connected to the coplanar ground with the use of vias as shown in Figures 2.3a and 2.3b), alleviates this problem, especially for thin dielectrics, leading to smooth transitions and improved signal launches. By using this hybrid design, there is no

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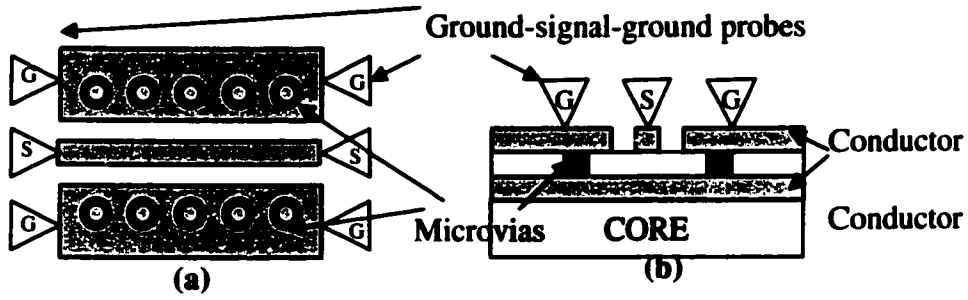

Figure 2.3 a) Top view of characterization CPWM structure
b) Cross-section of characterization CPWM structure

need to have a separate calibration structure for the pad to line discontinuity and the only interface that needs consideration is the probe tip to pad transition, which can be eliminated using the equations 2.1-2.4. The measurement setup is calibrated up to the probe tips using 2-port short-open-load-thru calibration structures available on impedance standard substrates (ISS) from Cascade Microtech.

2.3 Model to Hardware Correlation

The next step in the characterization procedure is to use ANSOFT 2D [21] to simulate the cross-sections of the grounded-CPW line. ANSOFT2D [21] is a 2D finite element method (FEM) based tool, which can be used to obtain the inductance (L), capacitance (C), resistance (R), and conductance (G) per unit length for the transmission line as a function of frequency. The R, L, G, C parameters can then be used to find the propagation constant from simulations:

$$\gamma_{sim} = \sqrt{(R + j\omega L)(G + j\omega C)} = \alpha_{sim} + j\beta_{sim} \qquad (2.5)$$

where ω is the angular frequency, α_{sim} is the attenuation per unit length and β_{sim} represents the wave propagation constant.

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At high frequencies, using the low-loss approximation R << ωL and G << ωC, equation 2.5 can be simplified to estimate the propogation constant β_{sim} in the form:

$$\beta_{sim} = \omega\sqrt{LC}$$

For extracting the dielectric constant, the relative permittivity of the dielectric is changed until β_{sim} equals β_{meas}. The use of ANSOFT2D for estimating the dielectric constant rather than using an empirical equation makes it possible to analyze non-uniform conductor profiles, large metal thickness and conductor roughness in the simulations. However, at lower frequencies and for lossy materials, the *R* and *G* values will influence the derived results for γ and β.

At lower frequencies, capacitors with large areas (each dimension much greater than the thickness of dielectric) have been used for the characterization of the material. Large area capacitors have small fringing effects and small conductor resistances due to the large size of the plates used. Additionally, small area capacitors (high self-resonant frequency) have been used to characterize the dielectric loss as a function of frequency. The unloaded Q and reactance of 1-port capacitors have been measured using a network analyzer. The unloaded Q factor of a capacitor is primarily affected by the dielectric loss of the material, which makes up the capacitor. The capacitors are then simulated in Advanced Design Suite (ADS) [15] with the relative permittivity extracted using the transmission line technique, whereby the loss in the material is altered until the measured and simulated unloaded Q for capacitors match.

The next section discusses the characterization of Asahi's A-PPE™ material using multiple structures, which includes the use of transmission lines, large area capacitors, and small area capacitors.

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2.4 Test vehicle for extracting dielectric constant

Table 2.1 shows low frequency capacitance measurements for several parallel plate capacitors fabricated using A-PPE™ as the dielectric. The measurements were done on various substrates and repeated at different times to include possible variations due to moisture absorption, and changes in temperature and humidity. One such substrate is shown in Figure 2.4. The capacitor measurements were done at 120 kHz using a standard LCR meter from Hewlett Packard with the setup shown in Figure 2.4 after performing cable and open-short corrections. The results indicate very good correlation in the low frequency range. The capacitor measurements give an average dielectric constant of about 3.48. The thickness of the Asahi A-PPE™ film measured at different points was found to be 30±1um. The

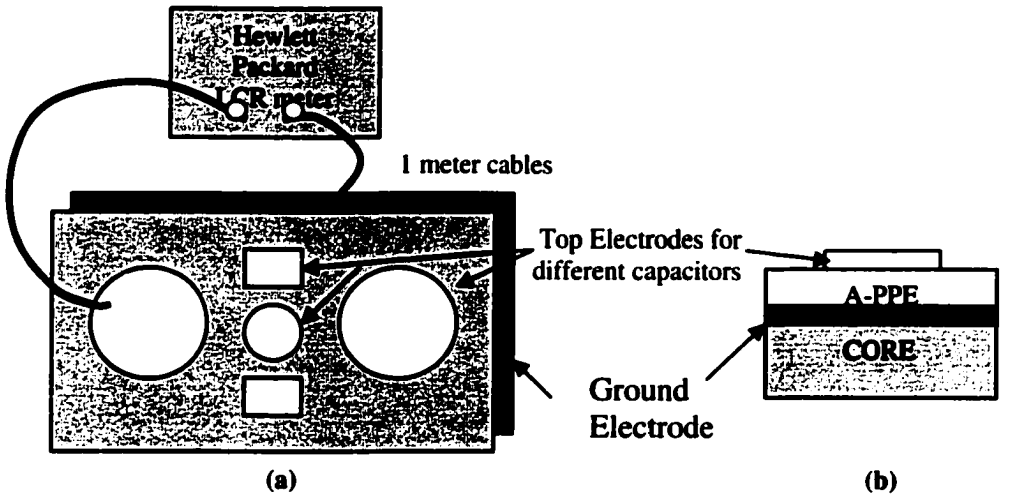

Figure 2.4 a) Top view of test vehicle for low frequency characterization
b) Cross-section of testbed for low frequency characterization

Table 2.1 Dielectric Constant from Capacitor Measurements at 120 kHz.

	Length (mils)	Width (mils)	Diameter (mils)	Area (mil^2)	Capacitance	Thickness (um)	E_r
Cap1			8.78	60.5	6.25E-11	30	3.48
Cap2			6.68	35	3.64E-11	29	3.48
Cap3(rectangle)	6.46	4.77		31	3.22E-11	29	3.48
Cap4			8.78	61	6.14E-11	31	3.48
Cap5 (rectangle)	6.47	4.75		31	3.10E-11	31	3.48
					Average Dielectric	30±1	3.48

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substrates were processed using the steps outlined in Appendix A.

Having characterized the material at low frequencies the next step is to characterize the material at higher frequencies. Figure 2.5a shows the cross-section of the CPWM lines used in the characterization of the A-PPE™ material while Figure 2.5b shows the top view of the CPWM structure. The spacing (*d2, Figure 2.5a*) was chosen so that the signal and ground are as far apart as possible and at the same time complies with the dimensions of wide-pitch probes such as the Cascade GSG 500um pitch probes. This ensures that *d (thickness of dielectric) much lesser than d2 (pitch of probe).* With this relationship, the return currents for

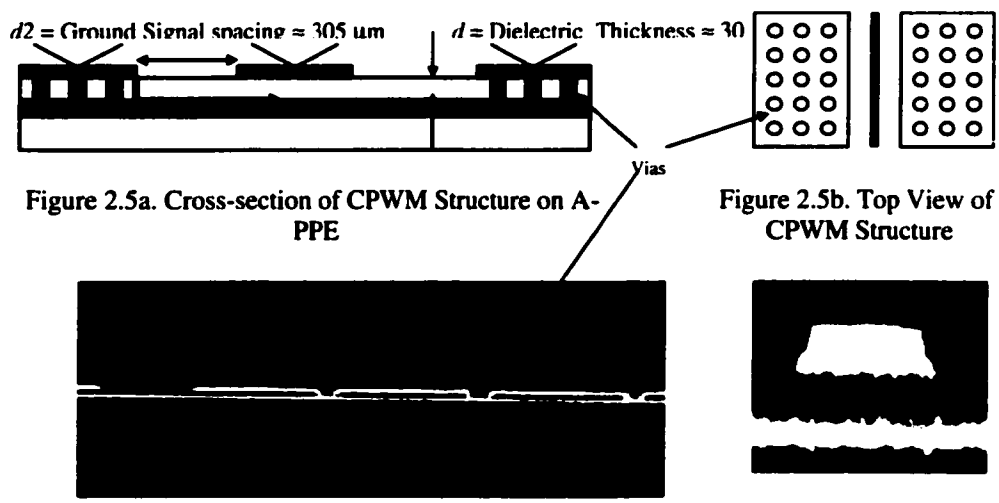

Figure 2.5a. Cross-section of CPWM Structure on A-PPE

Figure 2.5b. Top View of CPWM Structure

Figure 2.5c. Cross-section of 100 μm Microvias

Figure 2.5d Cross-section of Signal Line

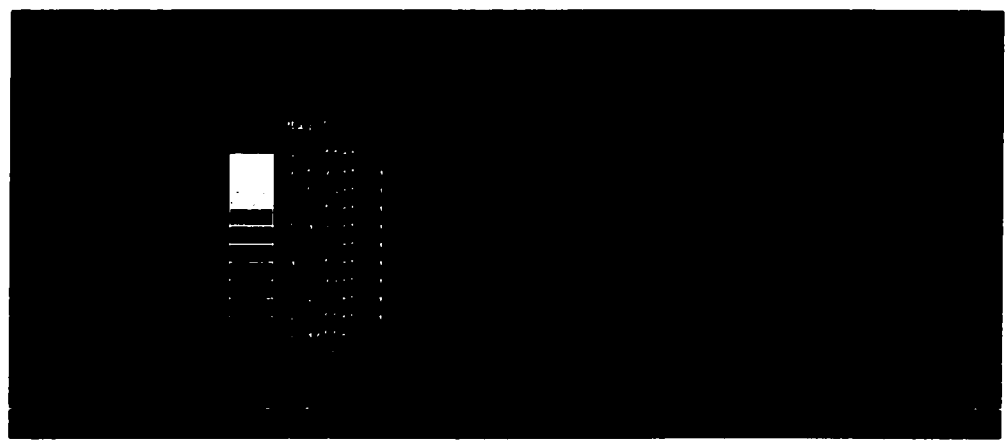

Figure 2.6 Electric fields at 1 GHz for the CPWM structure showing concentration of energy directly underneath the signal

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the signal line will be concentrated in the ground plane directly below the signal line. This can be verified with a simulation of the CPWM line in ANSOFT2D [21], as shown in Figure 2.6. This figure shows the E-field distribution at 1 GHz over the cross-section of the transmission line. As can be seen, all the fields are concentrated directly underneath the signal line.

Since the current flows entirely on the ground below the signal line, the coplanar ground connected to the ground underneath with vias can be ignored in the simulation. Reducing the number of metallic conductors/surfaces in the simulation helps decrease simulation time in FEM based solvers significantly and helps prevent memory overflow. No capacitance is observed between the CPW grounds and the backplane ground because they were connected to each other through multiple vias, as can be seen from Figure 2.5a, 2.5b, and 2.5c. The attenuation (α_{meas} in dB/m) and $\varepsilon_{eff,meas} = (\beta_{vacuum}/\beta_{meas})^2$ are derived using equations (2.1-2.4) where α_{meas}=Real(γ_{meas}) and β_{meas}=Imag(γ_{meas}) and are shown in Figure 2.7a and 2.7b, respectively. To obtain good model to hardware correlation, the microstrip structure with the trapezoidal profile from Figure 2.5d was simulated in ANSOFT 2D. The cross-section was simulated using the profile at different points, and then the dielectric constant was varied in the simulation until the measured effective dielectric constant, $\varepsilon_{eff,meas}$ agreed with the simulated effective dielectric constant. Since, the CPWM transmission line has air on one side and the dielectric on the other side, ε_{eff} is in between the permittivity of air and the dielectric. Figure 2.7b also shows the relative dielectric constant simulated at different frequencies, which correspond to the measured ε_{eff}. The dielectric constant at low frequencies as seen in Figure 2.7b for the A-PPE™ material shows good correlation with the data shown

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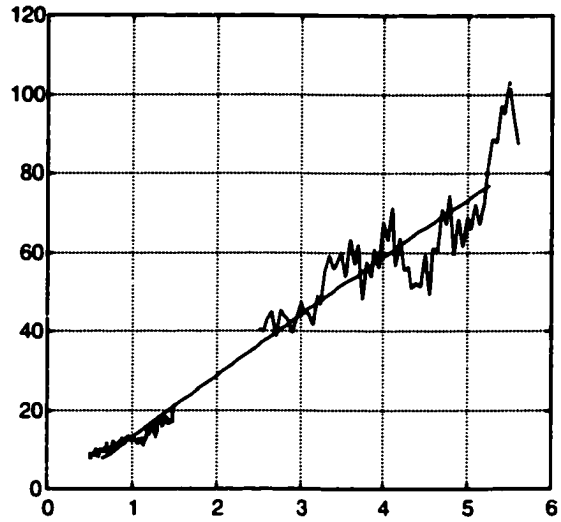

Figure 2.7a. Attenuation (dB/m) Vs. Freq (GHz) for A-PPE™

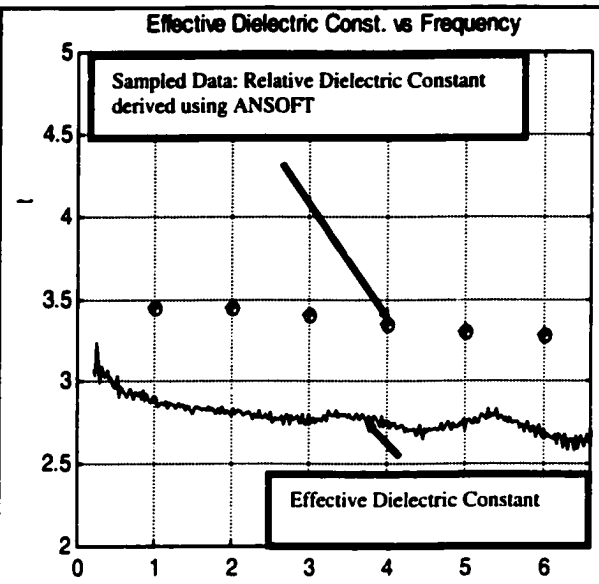

Figure 2.7b. Effective Dielectric Const. Vs Freq (GHz) for A-PPE™

in Table 2.1. The attenuation for the lines shown in Figure 2.7a correlates well with data for other laminates such as polyimide [22] which is currently used in high frequency applications. The dielectric constant is stable over a broad frequency range. Asahi's A-PPE™ is a relatively new laminate material and characterization of this material was the first step towards evaluating the feasibility of using this material at higher frequencies.

The dielectric constant for Dupont Vialux™ and Rogers Zyvex™ materials were also extracted using the transmission line method and then verified using small 1-port capacitors with high self resonant frequencies. The results are shown in Figure 2.8.

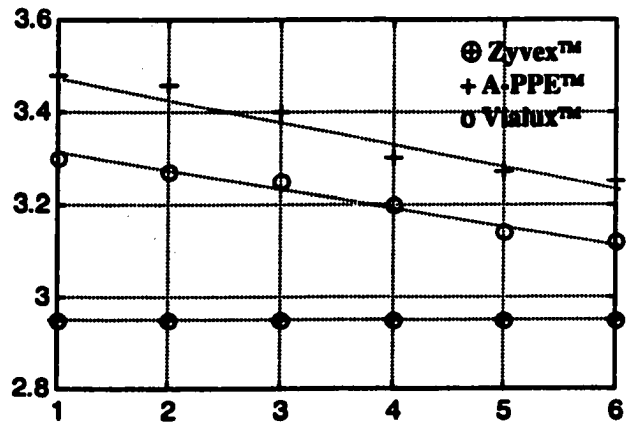

Figure 2.8 Relative Permittivity of three laminate materials vs. Frequency (GHz)

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The CPWM line technique is a fast, robust and accurate technique for characterizing materials up to high frequencies. With the present method, dielectric materials have been charactized upto 6 GHz in this dissertation.

2.5 Verification of transmission line method

Several small capacitors were also fabricated on A-PPE™ substrate. These capacitors were then measured using 1-port Short-Open-Load (SOL) calibration on Agilent's 8720ES Vector Network Analyzer. The measurements were done with an averaging factor of 36 and 1601 points for the frequency range: 100 MHz to 6 GHz. The capacitors were then simulated in Agilent's Advanced Design Suite (ADS) [15] for the same frequency range. The schematics for the capacitors on A-PPE™ are shown in Figure 2.9; the schematics include the discontinuities in the layout that come about because of the differences in the size of the probe pads compared to the device under test. The discontinuities are shown in the dotted boxes in Figure 2.9. The electrical properties of the substrate used in the simulations in ADS are the same as that obtained from the transmission line technique. The roughness and

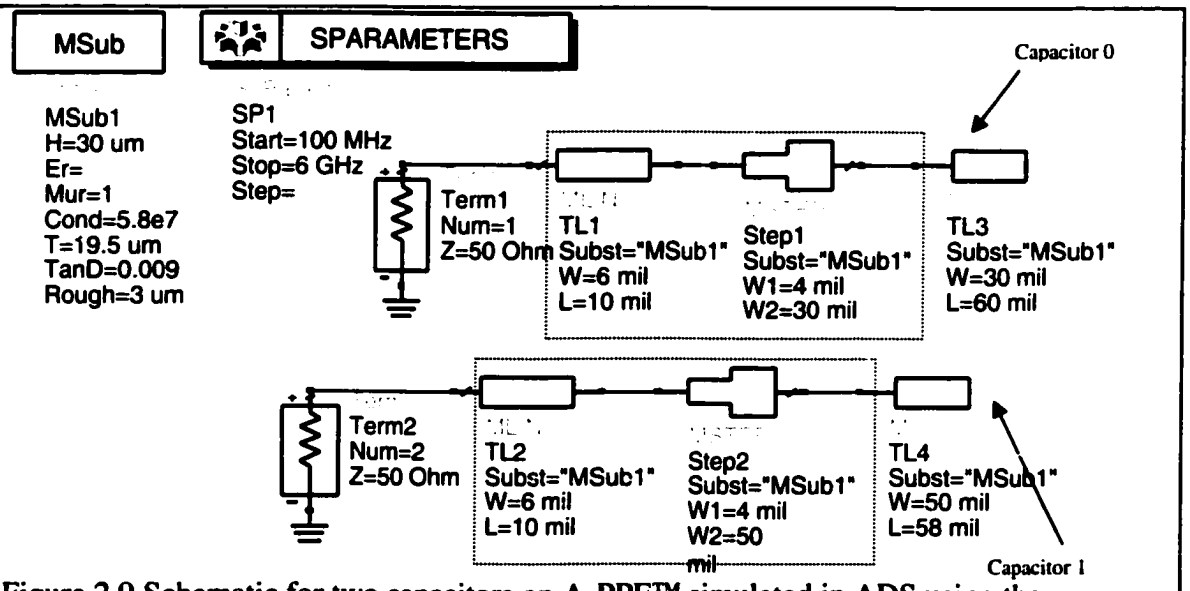

Figure 2.9 Schematic for two capacitors on A-PPE™ simulated in ADS using the characterization data from the transmission line technique.

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thickness of the conductor were obtained by cutting and polishing a section of the substrate. The simulated and measured data for effective capacitance is shown in Figure 2.10. As seen, there is very good correlation between simulated and measured data. These results show the validity of the two techniques, namely CPWM transmission line technique and small parallel plate capacitors, for extracting the dielectric constant.

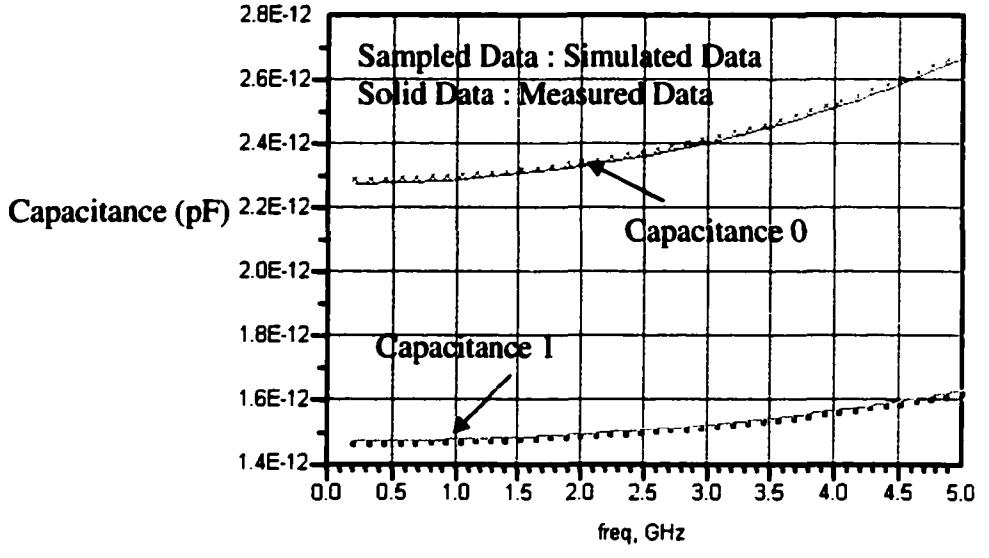

Figure 2.10 Measured and Simulated Effective Capacitance

2.6 Extraction of Dielectric Loss

The loss tangent for the material can be extracted by matching the measured Qs for the capacitors and simulated Qs for the 1-port capacitors such as those shown in Figure 2.9. However, care should be taken to include parameters such as conductor roughness and correct conductor thickness in order to include all losses in the device and not overestimate or underestimate the loss in the dielectric. The loss tangent for A-PPE™ material, Vialux™ and Zyvex™ was extracted after taking these parameters into account. As can be seen in the circuit schematic in Figure 2.8, the data used for the conductor roughness for A-PPE™

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substrate is 3 um and the metal thickness is 19.5 um. Figure 2.11 shows the measured and modeled Q factors for the capacitors represented in Figure 2.8. The model shows good model to hardware correlation. This method enables the characterization of material loss as a continuous function of frequency. The results have been verified with vendor-supplied data in the next section.

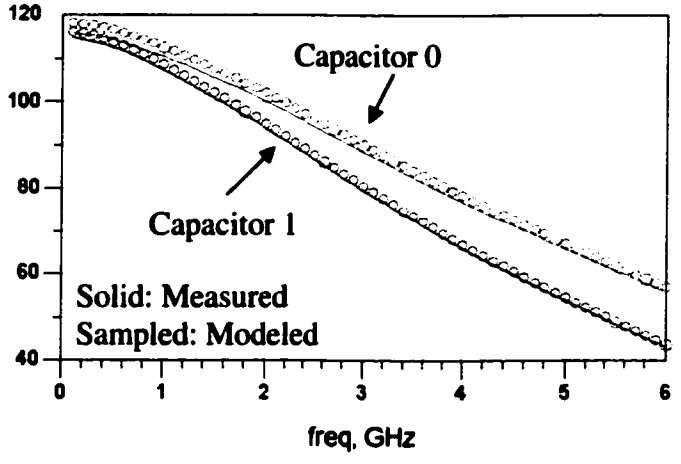

Figure 2.11 Modeled and measured Q factor vs. Freq (GHz) for capacitors in Figure 2.8

The loss tangent of Vialux™ and Zyvex™ was characterized using the same method. A 20um Vialux™ laminate and 50um Zyvex™ laminate were used for the respective testbeds. Figure 2.12 shows the loss tangent of the three different materials evaluated in this dissertation.

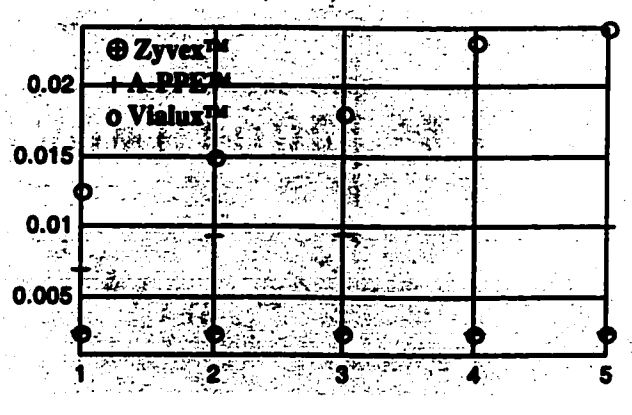

Figure 2.12 Loss of three laminate materials vs. Freq (GHz)

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2.7 Comparison between vendor data and extracted data

The comparison between the vendor supplied data for the three materials at 2 GHz has been shown in Table 2.2. As seen from Table 2.2, there is good correlation between vendor supplied data and extracted data for all numbers except the dielectric constant of A-PPE™ material. This is probably because A-PPE™ is a relatively new material in the industry and the material composition of the laminate is not standardized currently.

Table 2.2. Comparison of vendor supplied and extracted data for Asahi A-PPE™, Dupont Vialux™ and Rogers Zyvex™ at 2 GHz

Material	Dielectric Constant @ 2 GHz		Loss Tangent @ 2 GHz	
	Vendor Data	Extracted Data	Vendor Data	Extracted Data
Asahi A-PPE™	2.9	3.49	0.009	0.009
Dupont Vialux™	3.3	3.27	0.015	0.015
Rogers Zyvex™	2.95	2.95	0.002	0.0025

2.8 Summary

In conclusion, three different materials were evaluated and characterized to obtain the frequency dependent loss and relative permittivity of the materials. While materials such as Vialux™ exhibit strong dependence of the electrical properties over frequency, materials such as Zyvex™ show very stable properties, which is similar to materials used in LTCC and MCM-D processes. The next chapter discusses the modeling of passive devices such as inductors and capacitors, whereby a method to include the frequency dependent losses and electrical properties of the materials is discussed.

The primary difference between the three materials is the loss characteristics. While the strong dependence of the loss tangent on the Q of capacitors has been used in this chapter for

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extracting the loss of the material, the influence of loss on inductor performance has not been evaluated. Chapter 4 discusses in detail the design of inductors and capacitors and shows the importance of parameters such as dielectric loss and dielectric thickness on their performance. The three materials characterized in this chapter have also been used to fabricate filters and active modules, which are discussed in later chapters.

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CHAPTER III

3. MODELING OF EMBEDDED RF PASSIVE DEVICES

Introduction

Design of embedded passive devices requires accurate models for predicting the frequency response of the device. For example, the design of embedded inductors requires models for optimizing the layout to ensure that the device meets the specification for inductance, Q-factor and self-resonant frequency (SRF).

Various authors have modeled embedded inductors and capacitors in the past using a number of numerical methods. For example, commercial 3D electromagnetic solvers using finite elements (FEM) [23] and method of moments (MOM) [24] are currently available for modeling inductors and capacitors. Tools based on finite elements are accurate but the simulations sometimes take hours based on the design complexity. MOM based tools are faster and compute the reactance and SRF accurately for most configurations of inductors and capacitors. However, MOM based tools sometimes produce erroneous results in the computation of the Q-factor. For the inductor topologies discussed in this dissertation, the commercial tools under predicted the Q factor by ~ 100% in most cases. This could be due to a variety of approximations for modeling loss such as 1) conductors being represented as zero-thickness strips with the loss effect corrected using a surface impedance, 2) modeling the cross-section using four equivalent surfaces [25] and 3) modeling the thickness using parallel plates [24], to name a few. An alternate approach for obtaining accurate Q-factor is through empirical models available in RF design systems such as Libra and Advanced Design Suite (ADS by Agilent). These empirical models are however valid for specific technologies and do not scale well for

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new technologies. In addition, the empirical models seldom account for losses due to current crowding and proximity effects, which sometimes require a higher order approximation. Moreover, none of these tools provide any intuition on the kind of topology best suited for a particular process. Since the passives in this dissertation are specifically targeted for 1-5 GHz wireless applications, the modeling methods can be simplified as compared to commercial full-wave, three-dimensional electromagnetic tools. In addition, methods can be developed that are comparable in computational speed but have better accuracy than the empirical models. Fast computational methods allow for iterations in a design whereby the layout in a multi-layered process can be optimized to meet specifications.

Embedded passives such as spiral inductors, filters, couplers, and inter-digital capacitors consist of coupled line sections connected to each other through discontinuities. A method is presented in this chapter for simulating n-port embedded RF devices using coupled line parameters obtained using quasi-TEM and quasi-static approximations. In the case of two symmetric coupled lines, these parameters are the even-mode and odd-mode characteristic impedances and propagation constants. The coupled line approach uses a distributed model, which relates the voltages and currents at the start and end of a multiple coupled line section using impedance and admittance matrices [26, 27]. The solution is not limited to symmetric lines and can be applied to asymmetric lines as well. The discontinuities in the circuit, such as bends, vias and steps in width are modeled using scalable models [28]. These scalable models provide a mapping between the physical and electrical parameters of the discontinuity, which are represented using rational functions. The system response for the complete passive structure is obtained by enforcing the continuity of voltages and currents

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at the ports [26]. This method enables the segmentation of the structure, computation of the impedance matrix of the individual segments and reconstruction of the entire device response. This method has been found to be valid for frequencies up to 8 GHz for devices considered in this dissertation.

Predicting coupling between components is also important in the design of compact mixed signal devices. The magnetic coupling of two integrated inductors, which can affect the performance of active circuits such as amplifiers, has been studied in [29]. A Bluetooth filter, which utilizes the coupling of inductors, is discussed in [30] and has been simulated using partial-element-equivalent circuit (PEEC) and MOM based techniques. In this chapter, the modeling method discussed has been extended for extracting the coupling between devices.

This chapter has been organized as follows: section 3.1 provides details on the segmentation of inductors; in section 3.2, the Z-matrices for coupled line sections are derived; in section 3.3 a method for deriving scalable models for discontinuities such as bends, vias and cross-overs is presented; section 3.4 explains the segmentation method that is used to cascade the matrices; in section 3.5 the modeling technique is applied to multi-mode structures such as inductors and the results are compared with a full wave electromagnetic solver such as SONNET [24]; in section 3.6 the modeling results have been compared to several inductors fabricated using MCM-L technology; in section 3.7 the modeling method has been applied for modeling inter-digital capacitors and the results have been compared with measured data and SONNET data; the coupling between inductors is predicted using the modeling technique and compared with the results from a

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full wave electromagnetic solver (SONNET) in section 3.8 followed by a summary in section 3.9.

3.1. Segmentation of Planar and Multi-layer structures

Coupled lines represent an integral part of embedded passives such as coupled-line filters, line couplers, etc. However, coupled lines also represent an integral part of passive devices such as spiral inductors, loop inductors and inter-digital capacitors. For example, a 1 ¾ turn inductor above a ground plane is shown in Figure 3.1 and is made of several coupled line sections cascaded with each other through vias, bends and cross-overs.

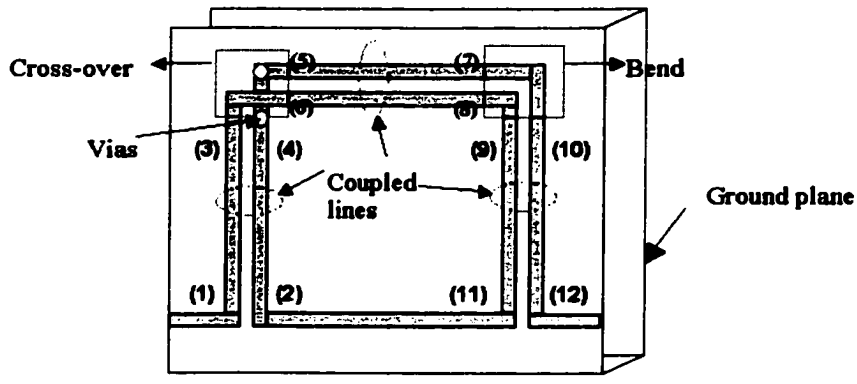

Figure 3.1 1 ¾ turn inductor

Figure 3.2 shows the inductor in Figure 3.1, which can be unfolded into a cascaded structure of coupled lines and discontinuities. The larger gray blocks in Figure 3.2

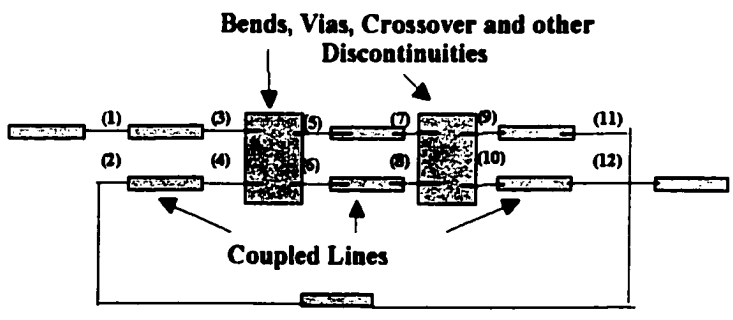

Figure 3.2. Segmentation of 1 ¾ turn inductor

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represent the discontinuities between the coupled line sections of the inductor in Figure 3.1. For example the block between ports 3, 4 and 5, 6 is a crossover and that between 7, 8 and 9, 10 are coupled bends. These discontinuities in the circuit, which are electrically short structures at RF frequencies, can be modeled using scalable models discussed in section 3.3. The gray line segments represent the multiple coupled line or single uncoupled line sections, which are modeled using the methods presented in section 3.2.

Hence, a multi-mode structure such as spiral inductors can be segmented as shown in Figure 3.2. The next section discusses the modeling of coupled segments in the frequency domain.

3.2. Z-matrices for Coupled Line Sections

A set of 'n' coupled lines can support 'n' independent modes of propagation called normal modes. This section explains the method used to capture the responses of coupled lines using the quasi-TEM modes of propagation. The accuracy of this approach improves as the ratio of the wavelength to the thickness of the dielectric increases. A 2D electromagnetic solver such as ANSOFT 2D provides characteristic mode impedances and propagation constants for lossy and lossless lines. The mode impedances and propagation constants can be used to create a distributed model for the multi-line coupled line sections. The advantage of using a distributed model is that it prevents artificial ringing induced by lumped circuit equivalents of the same structure. As an example, consider the symmetric coupled line structure shown in Figure 3.3. The voltages and currents on a set of 2 symmetric lossless coupled lines of length, l, shown in Figure 3.3, can be obtained from the even-mode impedance (Z_{oe}), odd-mode impedance (Z_{oo}), even-mode propagation constant (β_e) and odd-mode propagation constant (β_o) as follows [26]:

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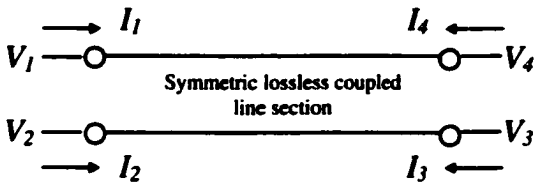

Figure 3.3. Voltage and Currents on Symmetric lossless coupled lines

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} \tag{3.1}$$

where,

$$\begin{aligned} Z_{11} = Z_{22} = Z_{33} = Z_{44} &= -j(Z_{oe}\cot(\beta_e l) + Z_{oo}\cot(\beta_o l))/2 \\ Z_{12} = Z_{21} = Z_{34} = Z_{43} &= -j(Z_{oe}\cot(\beta_e l) - Z_{oo}\cot(\beta_o l))/2 \\ Z_{13} = Z_{24} = Z_{31} = Z_{42} &= -j(Z_{oe}\csc(\beta_e l) + Z_{oo}\csc(\beta_o l))/2 \\ Z_{14} = Z_{23} = Z_{32} = Z_{41} &= -j(Z_{oe}\cot(\beta_e l) - Z_{oo}\csc(\beta_o l))/2 \end{aligned} \tag{3.2}$$

In equation 3.1, I_1, I_2, I_3 and I_4 are the port current and V_1, V_2, V_3 and V_4 are the corresponding port voltages. For structures like the inductor in figure 3.1 where only adjacent lines are coupled to one another, equations 3.1 and 3.2 are sufficient to obtain the z-parameters for the lines. However, for structures where multiple (>2) asymmetric lossy lines may be coupled, the eigen-value approach discussed ahead can be used.

The voltage and current vectors, V and I, on a multi-conductor coupled line, which propagate energy in the $\pm z$ direction, can be written as

$$-\frac{\partial^2}{\partial z^2} V = ZYV \tag{3.3}$$

$$-\frac{\partial^2}{\partial z^2} I = YZI \tag{3.4}$$

where

$$Z = (R(f) + j\omega[L]) \tag{3.5}$$

$$Y = (G(f) + j\omega[C_e]) \tag{3.6}$$

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In equations (3.5) and (3.6), R(f) and G(f) represent the conductor loss and dielectric loss respectively. Both these parameters are frequency dependent. For RF and microwave applications, where the current penetration depth in the conductor is of the order of micrometers, the frequency dependence of the resistance matrix, **R**, conductance matrix, **G**, and inductance matrix, **L**, can be written in the form:

$$R(\mathrm{f}) = R_{DC} + R_{AC}\sqrt{\mathrm{f}} \quad , L = L_e + L_i \frac{1}{\sqrt{\mathrm{f}}} \text{ and } G(\mathrm{f}) = \mathrm{G_1} \times \mathrm{f} / \mathrm{f_1} \qquad (3.7)$$

In the above equations, L_e and C_e represent the external inductance and capacitance matrices respectively; $\omega = 2\pi f$ is the angular frequency. Equation (3.7) can be used to capture the frequency effects in the inductor. R_{DC} and R_{AC} are computed by solving for the total resistance matrix, R, at two different frequencies using commercial tools such as ANSOFT2D. Similarly L_i and L_e are computed by solving for the inductance matrix, L, at two different frequencies. The conductance matrix, G_1, is computed at a particular frequency (f_1) and then computed at other frequencies (f) using equation (3.7). C_e is assumed to be constant with frequency. Equation 3.7 ignores the dependence of the dielectric constant on frequency, which is typical for dielectric substrates such as Vialux™ and A-PPE™ used in MCM-L processes.

The variations in dielectric constant can be introduced in the computation of the R, G and C matrices by observing the emperical equations for the lines under consideration. For example, in the quasi-TEM range, the effective dielectric constant, ε_{eff} of CPW lines (introduced in chapter 2 and shown in Figure 2.1) is proportional to $\sqrt{(\varepsilon_{ru1}(f_u) + \varepsilon_{ru2}(f_u))/2}$ [31] where ε_{ru1} and ε_{ru2} are the dielectric constants for

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Dielectric A and Dielectric B at a particular frequency f_u. Assuming one of the dielectrics to be air or vaccuum simplifies the relation to:

$$C_u(f_u) \ \alpha \ \varepsilon_{eff}(f_u) \alpha \sqrt{(\varepsilon_{ru}(f_u)+1)/2} \tag{3.8}$$

After computing the capacitance matrix C_u at a frequency f_u, with a dielectric constant of ε_{ru}, using ANSOFT2D, the C matrices at other frequencies can be obtained by using the quasi-TEM relationship described in equation 3.8. The capacitance matrix C_l at frequency f_l, where the dielectric constant is ε_{rl} for CPW lines can be computed by using the following relationship:

$$C_l(f_l) = C_u \times \sqrt{(\varepsilon_{rl} + 1)/(\varepsilon_{ru} + 1)} \tag{3.9}$$

The L matrix is independent of the dielectric constant. The G matrix at different frequencies can be computed using G α C.

For any transmission line, $R(f_u)$ is inversely proportional to $Zo(f_u)$ where $Zo(f_u)$ is the characteristic impedance of the line at frequency f_u. Since, $Zo(f_u)$ is also inversely proportional to $\sqrt{C_u}$, the R matrix becomes directly proportional to $\sqrt{C_u}$ as shown in equation 3.10. The relationship between R and C, shown in equation 3.10, along with equation 3.9 can be used to capture the effect of varying dielectric constant on the R matrix.

$$R(f_u)\alpha\frac{1}{Z_o}\alpha\sqrt{C_u} \tag{3.10}$$

The R matrix not only depends on the dielectric constant but also depends on skineffect and current-crowding effects. Current crowding is when the current distribution in lines, under the influence of an external time varying magnetic field, begins to

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concentrate along the edges of the lines. However, as expected current crowding is prominent only in very closely spaced turns of an inductor or closely spaced fingers of a capacitor. The inductors and capacitors evaluated as part of this work were designed using the design rules in Appendix B, one of which is to use a minimum spacing of 3 mils between lines. This ground rule reduces current crowding and therefore skin effect becomes the dominant effect. As mentioned earlier skin effect has been taken into account in the modeling using the $\sqrt{f}$ dependence as shown in (3.7). Section 3.6 and 3.8 verify the hypothesis and conclusions made above with model-to-hardware correlation for several inductors and capacitors.

Once the frequency dependant **Z** and **Y** matrices are obtained over the desired frequency range, for a wave propagating in the 'z' direction, the coupled equations, 3.3 and 3.4 can be partially de-coupled by solving the eigenvalue equation shown below:

$$(ZY - \lambda U).V = 0 \tag{3.11}$$

$$\textit{and} \quad (YZ - \lambda U).I = 0 \tag{3.12}$$

where, $-\lambda = \gamma^2$, U is the Identity Matrix and $\gamma = \alpha + j\beta$ is the complex propagation constant.

The n eigenvalues for n lines and n corresponding eigen modal voltage and current vectors can be obtained by solving equations (3.6) and (3.7) respectively. These can be used to define the behavior of the n lines completely. Let $\mathbf{M_V}$ and $\mathbf{M_I}$ be the complex eigenvector matrix associated with the matrices **ZY** and **YZ** respectively. All normal voltages and currents on the line can be written as a linear combination of vectors, $\hat{V}$ and $\hat{I}$ as follows:

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$$V = M_V \hat{V} \quad and \quad I = M_I \hat{I} \tag{3.13}$$

Substitution of (3.13) into (3.3) and (3.4) yields:

$$\begin{aligned} -\frac{\partial^2}{\partial z^2}\hat{V} &= (M_V^{-1} ZYM_V)\hat{V} \\ -\frac{\partial^2}{\partial z^2}\hat{I} &= (M_I^{-1} YZM_I)\hat{I} \\ (M_V^{-1} ZYM_V) &= (M_I^{-1} YZM_I) = \gamma^2 \end{aligned} \tag{3.14}$$

Since this is an eigenvalue problem a normalization procedure is required. In this paper the following normalization is used:

$$(M_V^{-1})^t = M_I \tag{3.15}$$

The computation of eigenvectors in 3.12 requires care, because of the properties of the **ZY** product. This product results in a diagonal dominant matrix, which has very closely spaced eigenvalues, which may give rise to difficulties and inaccuracies in the numerical computation. To avoid this difficulty an eigenvalue-shifting technique has been used. The shift is done by subtracting from **ZY** a scalar diagonal matrix with elements equal to the trace of **ZY** divided by n [26]:

$$(ZY)' = ZY - \gamma_{av}^2 E, \qquad \gamma_{av}^2 = \frac{1}{n}\sum_{i=1}^{n} (ZY)_{ii} \tag{3.16}$$

The resulting matrix **(ZY)'** is then diagonalized, yielding a set of adequately spaced eigenvalues $\gamma'_1, \ldots, \gamma'_k, \ldots \gamma'_n$ and a corresponding set of eigenvectors. The eigenvectors of **ZY** are exactly equal to those of **(ZY)'**. The eigenvalues of the original product **ZY** can be obtained by shifting back the eigenvalues as follow [26]:

$$\gamma_k'^2 = \gamma_{av}^2 + \lambda_k \qquad (k = 1, \ldots, n) \tag{3.17}$$

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This analysis is based on the diagonalization of the matrix **ZY**, whose solution enables the computation of the propagation modes traveling along the structure.

By solving for the voltages, V(0) and V(l) and currents, I(0) and I(l) at the ends of the multiple coupled line section, the impedance matrix can be derived as [26]:

$$\begin{bmatrix} V(0) \\ V(l) \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I(0) \\ I(l) \end{bmatrix}$$

$$Z_{11} = Z_{22} = COTH\ (\Gamma l) Z_w\ ;$$

$$Z_{12} = Z_{21} = CSCH\ (\Gamma l) Z_w$$

where,

$$COTH\ (\Gamma l) = M_V\ (coth\ \gamma l) M_V^{-1}$$

$$CSCH\ (\Gamma l) = M_V\ (csch\ \gamma l) M_V^{-1}$$

$$Z_w = M_V\ \gamma\ M_V^{-1} Y^{-1}$$

The above representation enables the designer to optimize the performance of RF passives by varying parameters such as line width, length and spacing for different coupled line sections using a 2D electromagnetic solver.

3.3. Scalable Models for Multi-Bend Structure

Quasi-static analysis is often performed to characterize strip discontinuities when the dimensions of the discontinuities are much smaller than the wavelength. When designing high-Q structures it is important to include all these effects into one model. Macromodeling is an efficient approach for these structures, which can be extended to scalable models explained in this section. The bends, crossovers and microstrip-via transitions and other discontinuities can be modeled using scalable models. The data for constructing the models can be obtained from measurements or from full-wave electromagnetic solvers.

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The purpose of a scalable function is to capture the mapping between the frequency response and the critical physical parameters of the structure. The mapping is developed using interpolation functions. The interpolation functions enable the minimization of the required number of sampled data points. In this section, rational functions have been used. Through selective sampling, the number of sampled data points has been minimized.

Using rational functions, the frequency response of any device can be represented as:

$$H(s) = \frac{\sum_{ns=0}^{NS} a_{ns} s^{ns}}{\sum_{ds=0}^{DS} b_{ds} s^{ds}}, \quad where \quad s = j\omega \tag{3.18}$$

where, s = $j\omega$, 'ω' is the angular frequency in radians per second and a_{ns}, b_{ds} are unknown coefficients. In (3.18), H(s) can either be S, Y or Z parameters. Using the research done by Hwan, *et al* in [28], this representation can be extended to multiple variables to develop scalable models in the form:

$$H(s, p_1, p_2, \ldots, p_n) = H_s(s) H_{p_1}(p_1) H_{p_2}(p_2) \cdots H_{p_n}(p_n) \tag{3.19}$$

$$H(s, p_1, p_2, \ldots, p_n) = \left(\frac{\sum_{ns=0}^{NS} a(0)_{ns} s^{ns}}{\sum_{ds=0}^{DS} b(0)_{ds} s^{ds}} \right) \left(\frac{\sum_{n1=0}^{N1} a(1)_{n1} p_1^{n1}}{\sum_{d1=0}^{D1} b(1)_{d1} p_1^{d1}} \right) \cdots \left(\frac{\sum_{nn=0}^{NN} a(n)_{nn} p_n^{nn}}{\sum_{dn=0}^{DN} b(n)_{dn} p_n^{dn}} \right)$$

where, p_1, p_2, ..., p_n are physical parameters of the device. For example, for a bend shown in Figure 3.4, the physical parameters are p_1 = *width* and p_2= *spacing*. The cross-section of a bend structure fabricated on a 10 mil core is shown in Figure 3.5 with the corresponding scalable parameters. The multi-dimensional function in (3.19) provides a mapping between the physical parameters, frequency and the frequency response of the

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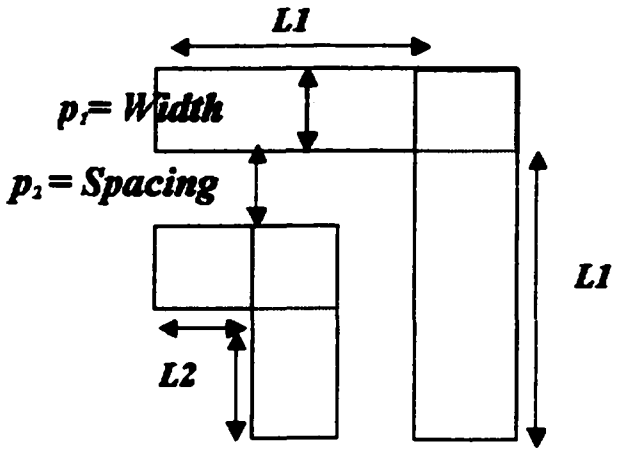

Figure 3.4. Coupled bends modeled as scalable functions

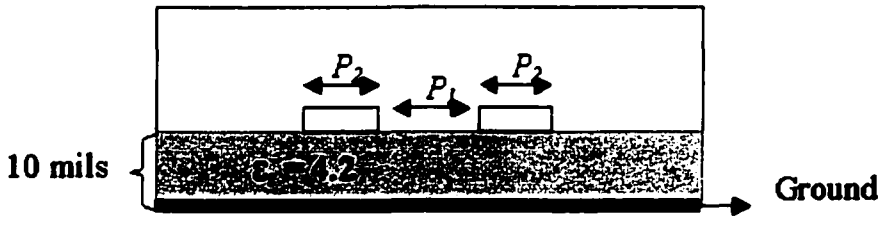

Figure 3.5 Cross-section of coupled bend structure

device. Once the scalable model in (3.19) is constructed, the function $H(s, p_1, p_2, \ldots, p_n)$ can be used to model multiple discontinuities by varying the physical parameters. However, L1 and L2 shown in figure 3.4, which are the lengths of the larger and smaller bend, are not chosen as scalable parameters. The larger length, L1 has to be a minimum length, which guarantees that the higher order electromagnetic modes within the bend die out at that length L1 from the corners of the bend structure, which in turn guarantees uniform current distribution. The length is determined after performing simulations for the coupled bend structure in SONNET. The current densities for the bend in Figure 3.4 on the substrate in Figure 3.5 at 1 GHz, 10 GHz and 15 GHz are shown in Figure 3.6 a, b, and c respectively. At 10 GHz length L1 can be chosen as the distance from the corner where the current density is uniform as seen in Figure 3.6b. However, scalable models cannot be used at 15 GHz because the bend behaves as a electrically long structure as

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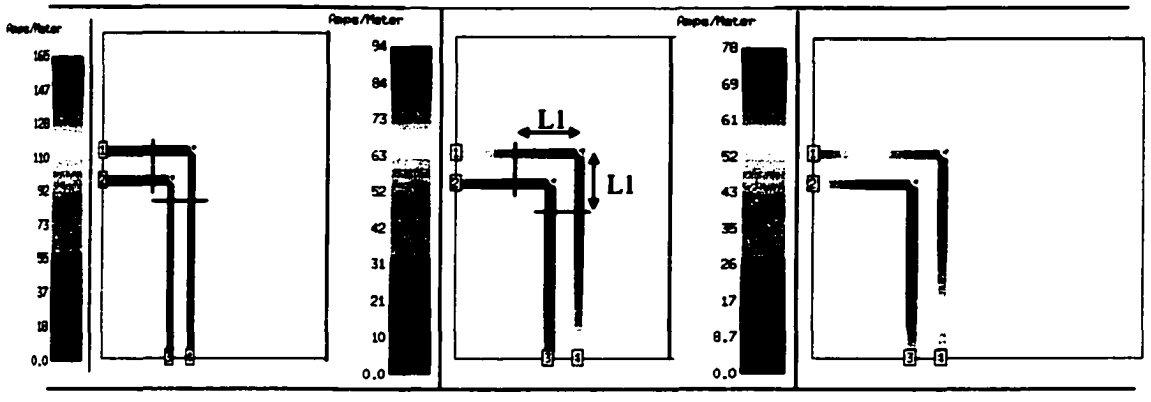
seen in Figure 3.6c where current densities are not uniform at any distance away from the corner.



(a) (b) (c)

Figure 3.6 a) Simulation of coupled bend structure in SONNET at 1 GHz
b) Simulation of coupled bend structure in SONNET at 10 GHz
c) Simulation of coupled bend structure in SONNET at 15 GHz

To extract the coefficients in (3.15) requires sampled input data and the solution to a matrix equation. To obtain the coefficients $\boldsymbol{a}$, and $\boldsymbol{b}$ the following matrix equation is solved:

$$N - H(s, p_1, p_2, \ldots, p_n)D = 0, \qquad (3.20)$$

where

$$N = \sum_{ns=0}^{NS} \sum_{n1=0}^{N1} \sum_{n2=0}^{N2} \cdots \sum_{nn=0}^{NN} a(0)_{ns} a(1)_{n1} a(2)_{n2} \cdots a(n)_{nn} s^{ns} p_1^{n1} p_2^{n2} \cdots p_n^{nn}$$

$$D = \sum_{ds=0}^{DS} \sum_{d1=0}^{D1} \sum_{d2=0}^{D2} \cdots \sum_{dn=0}^{DN} b(0)_{ns} b(1)_{n1} b(2)_{n2} \cdots b(n)_{nn} s^{ns} p_1^{n1} p_2^{n2} \cdots p_n^{nn}$$

Equation (3.20) can be written as:

$$(\boldsymbol{A}^*)^T \boldsymbol{A}\boldsymbol{x} = 0 \Leftrightarrow \boldsymbol{A}^H \boldsymbol{A}\boldsymbol{x} = \lambda_{\min} \boldsymbol{x} \qquad (3.21)$$

where, $\boldsymbol{A}$ contains the elements of the matrix, $\boldsymbol{A}^H$ is the Hermitian transpose and $\boldsymbol{x}$ contains the unknown coefficients. The above equation is solved as an eigenvalue

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problem by computing the minimum eigenvalue, λ_{min} as the order of the function is changed.

A major problem in implementing (3.20) is the number of sampling points required. The time required to construct the scalable model is a function of the number of sample points and the time required by the electromagnetic solver to generate each sampled data. Instead, Hwan, et al, have implemented an adaptive algorithm in [28], which has been used in this section.

The adaptive algorithm [28] begins with two groups of data with two separate functions. These two functions use the minimum number of sampled data points to construct the function. As a starting point, each function uses a small number of points, which represents the minimum samples required to construct the function. The response of these functions is then computed over a uniform grid across the domain of the solution space. The point at which the maximum deviation occurs is chosen as the next sample, which is then used to modify the two functions. The procedure is repeated until the error across the entire solution space is minimized.

3.4. Theory of Segmentation

Although fundamental mode equivalent circuits have proven to be very useful in simulating RF and microwave structures, they suffer from a number of limitations as structures that excite multiple modes are placed in close proximity to each other. The underlying basis of the segmentation approach is the transformation of the field matching (electric and magnetic fields) along the interface between two regions with higher mode excitations into an equivalent network connection problem using S-, Z-, or Y-matrices.

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Consider two multi-port segments with $n+q$ and $r+m$ ports respectively with q ports from the first segment connected to r ports from the second segment as shown in Figure 3.7.

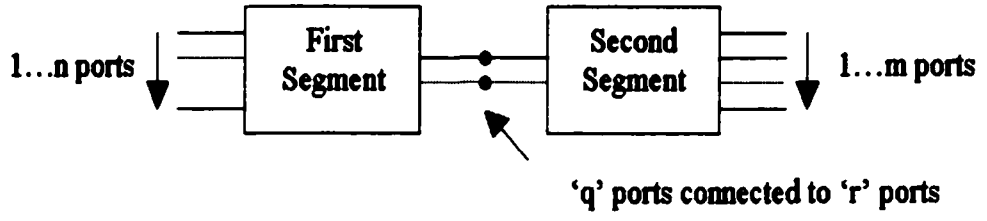

Figure 3.7 Segementation of different segments

The Z-matrices of the first and second segments can be written together as

$$\begin{bmatrix} V_p \\ V_q \\ V_r \end{bmatrix} = \begin{bmatrix} Z_{pp} & Z_{pq} & Z_{pr} \\ Z_{qp} & Z_{qq} & Z_{qr} \\ Z_{rp} & Z_{rq} & Z_{rr} \end{bmatrix} \begin{bmatrix} I_p \\ I_q \\ I_r \end{bmatrix} \tag{3.22}$$

where

$$\begin{bmatrix} V_p \end{bmatrix} = \begin{bmatrix} V_n \\ V_m \end{bmatrix}, \begin{bmatrix} I_p \end{bmatrix} = \begin{bmatrix} I_n \\ I_m \end{bmatrix} \text{ and } V_q = V_r \text{ and } I_q + I_r = 0 \tag{3.23}$$

Substituting equation (3.23) into (3.22) the Z-matrix for the overall network can be computed as:

$$Z_p = Z_{pp} + (Z_{pq} - Z_{pr})(Z_{qq} - Z_{qr} - Z_{rq} + Z_{rr})^{-1}(Z_{rp} - Z_{qp}) \tag{3.24}$$

Using the Z-matrices for the coupled line sections and discontinuities, equation (3.24) can be used to construct the response of the entire circuit.

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3.5. Validation of the Segmentation Method

To validate the segmentation method for simulating multi-mode structures, embedded inductors with repeated coupled line sections and discontinuities were chosen. Figure 3.8 shows a 2-turn and 3-turn lossless microstrip inductor simulated in SONNET, which is a commercial software that simulates microwave planar structures using the Method of Moments (MOM) technique. The segmentation of the 2-turn and 3-turn microstrip inductor structure is shown as a cascade of varying lengths of coupled line sections (2 line and 3 line coupled line sections), and coupled and single bend discontinuities (shown in dotted boxes). The microstrip substrate (ground below signal lines) was chosen as FR4 type material with ε_r=4.2 and a thickness of 10 mils. An example of the cross-section simulated in ANSOFT 2D to obtain the L, C matrices for the two lossless coupled line section, which represents segments for the 2 turn inductor, is shown in Figure 3.9.

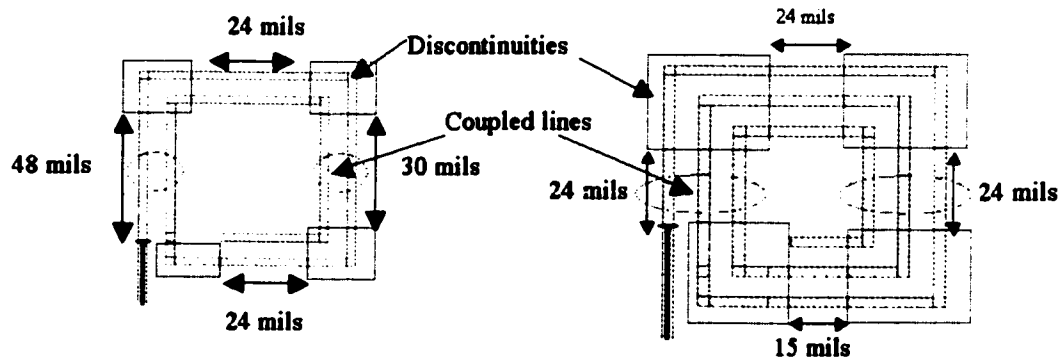

Figure 3.8 Segmentation technique for 3-turn and 2-turn inductors

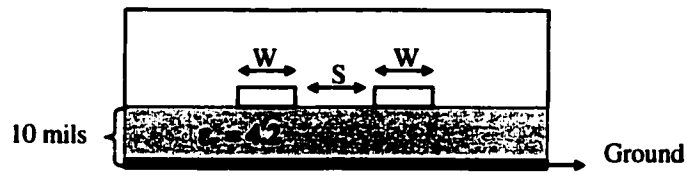

Figure 3.9 Cross-section of 2 coupled lines in ANSOFT 2D used to model 2 turn inductor

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The data for the bend discontinuities was obtained using SONNET, and then scalable models were developed based on Section 3.3 using adaptive sampling. For the 2-turn inductor the bend shown in Figure 3.4 was modeled as a scalable model with the physical parameters being $p_1 = w$ and $p_2 = s$. The model was developed for $1\text{mil} < p_1 < 6\text{mils}$ and $1\text{mil} < p_2 < 6$ mils and 1 GHz < f < 8 GHz. If p1 and p2 were both sampled at 1 mil intervals and f sampled in 400 MHz intervals, a total of 648 sampled points would be required. This requires SONNET simulation at 648 frequency points. Using the adaptive sampling technique, the number of sampled points required for the bend was 36 compared to 648 samples, which reduced the time significantly. For the bend structure, the error between the two functions is shown in Figure 3.10, where the x-axis is the number of loops required to construct the multivariable functions. Figure 3.11 shows a comparison between SONNET and Multi-dimensional Rational Function (MRF) data for varying physical parameters, which shows good correlation. The order of the polynomial for the final MRF were as follows: NS=1, DS=1, N1=2, D1=2, N2=2, and D2=1.

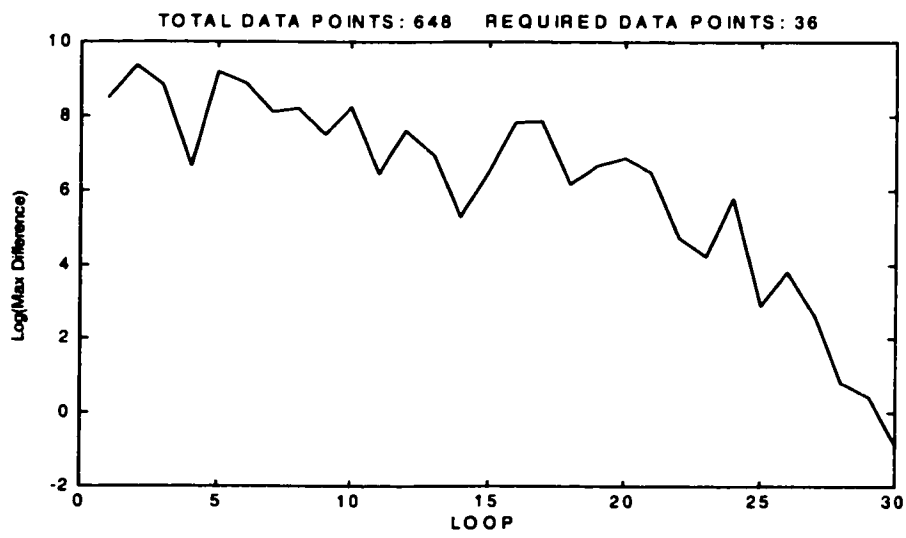

Figure 3.10 Maximum Deviation of the two rational functions vs. number of samples

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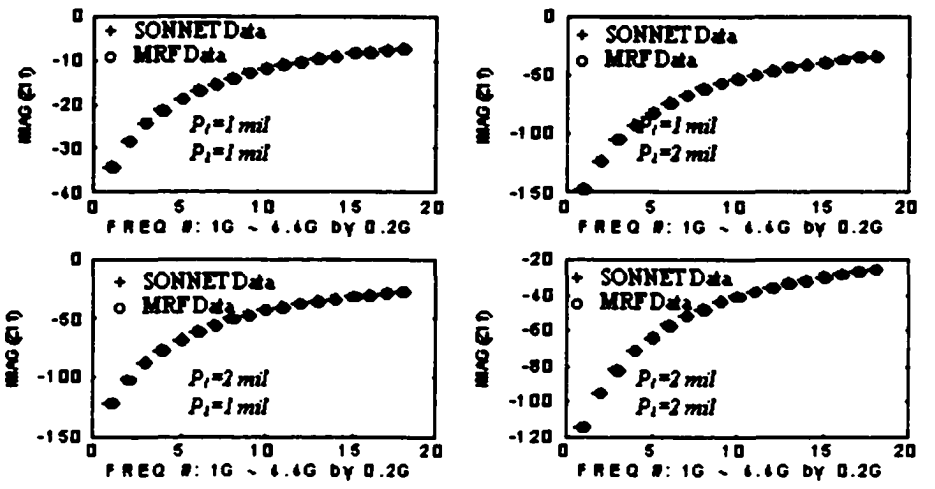

Figure 3.11 SONNET and MRF data results for coupled bend structure

Figure 3.12 and Figure 3.13 show the computed reactances for the structures in Figure 3.8, from SONNET and the proposed method. As clear from the figures, the two show good correlation up until 8 GHz.

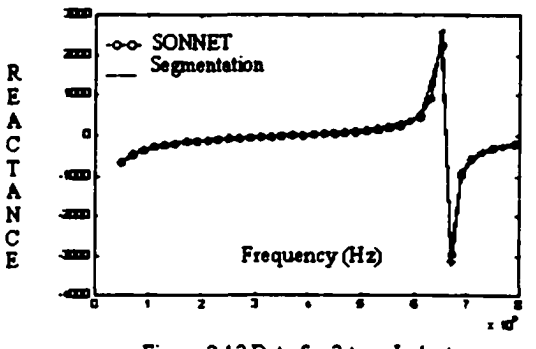

Figure 3.12 Data for 2-turn Inductor

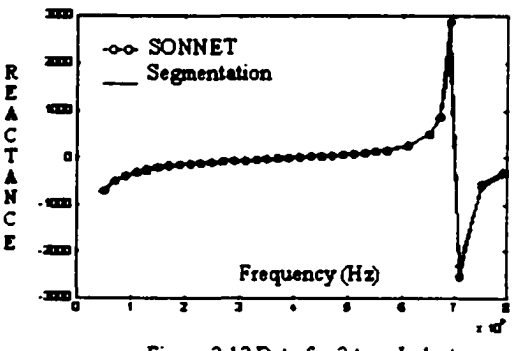

Figure 3.13 Data for 3-turn Inductor

In conclusion, once the electrical behavior of discontinuities is extracted using 3D electromagnetic solvers and represented using scalable models, these can be combined with the per unit length parameters of the coupled line sections (extracted using 2D solvers) to compute the overall electrical response of the device. The main advantage with this approach is that it provides scalability in the design process whereby all the

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physical parameters are scalable. In addition it provides computational speed and accuracy. The accuracy is maintained for lossless structures, such as those in this section where the computed reactances were compared to results from SONNET. In addition, the accuracy is also maintained for lossy structures such as those in the next section where tools such as SONNET fail due to reasons mentioned in the introduction section.

3.6. Model to Hardware Corelation

The cross section of the test vehicle, fabricated using the steps outlined in Appendix A, is shown in Figure 3.14. The shaded areas represent the conductor layers; Metal 3A was formed by electroplating and pattering copper to a height of 18um. The design rules in Appendix B require metal 2A, buried under the dielectric, to be < 1/3rd the height of the dielectric (18-20um) in order to achieve uniform dielectric thickness. However, it is not possible to plate copper uniformly below the height of the photo-resist (15um) being used. An obvious step would be to use thicker dielectric or thinner photo-resist, but due to the lack of availability of thicker laminates such as A-PPE™ and Zyvex™ or thinner resist at that moment, Vialux™ had to be used. As a result, the height of Metal 2A varied from 6-9um across the extent of the testbed. This did not cause a problem in the fabrication and

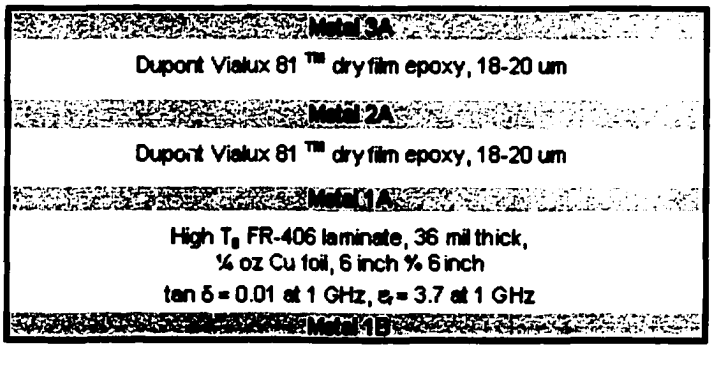

Figure 3.14 Cross-section for Multi-layer Substrate

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design of inductors, since Metal 2A was solely used for under-routing and connectivity of devices and the variance in the dielectric height contributed little to the overall response of the devices. The core substrate was standard FR4 which has a $\tan\delta=0.01$ and $\varepsilon_r=3.7$ at 1GHz. The dielectric, Dupont Vialux™, has a $\tan\delta=0.015$ and $\varepsilon_r=3.4$ at 1GHz and $\tan\delta=0.015$ and $\varepsilon_r=3.27$ at 2GHz. This data was obtained using the characterization methods discussed in chapter 2. The use of epoxy-based laminates such as Vialux™ was also made for the first testbed in order to understand the performance limits of the epoxy materials. Several embedded passives were designed on this substrate to characterize its performance. Figure 3.15 shows the top-view of the three cascaded loop microstrip inductors. These were fabricated on the top metal layer (Metal 3A) with Metal (1B) as the ground reference. This provided a ground plane separation of approximately 38 mils.

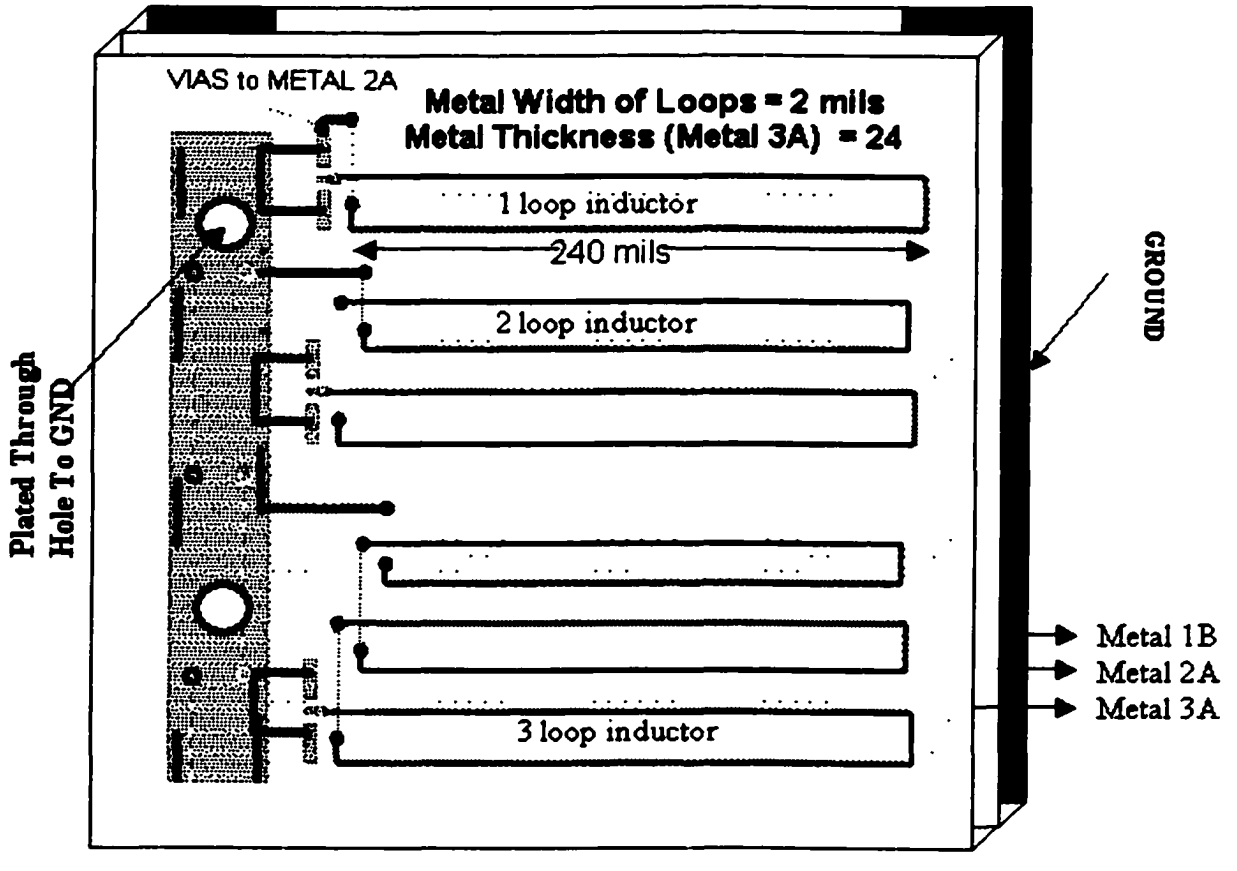

Figure 3.15 Microstrip loop inductors on the multilayer organic substrate

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Figure 3.16a, Figure 3.17a and Figure 3.18a show the measured and computed reactances of the microstrip loop inductors of Figure 3.15. Figure 3.16b, Figure 3.17b and Figure 3.18b show the measured and computed Q-factors for the corresponding inductors. The modeling results are based on the segmentation method described earlier. An example of the RLGC matrices for 4 lines at 1 GHz which represents the four line section of the 2-loop inductor is shown below:

$$L=\begin{bmatrix} 9.79 & 3.67 & 2.4627 & 1.77 \\ 3.676 & 9.648 & 3.748 & 2.335 \\ 2.4627 & 3.748 & 9.649 & 3.3997 \\ 1.770 & 2.3354 & 3.3997 & 9.835 \end{bmatrix} \frac{10^{-7}H}{m}, \quad G=\begin{bmatrix} 0.1402 & -0.035236 & -0.009378 & -0.003049 \\ -0.0352 & 0.1575 & -0.03429 & -0.0083599 \\ -0.0093783 & -0.034299 & 0.15584 & -0.030808 \\ -0.003048 & -0.0083599 & -0.030808 & 0.13536; \end{bmatrix} \frac{10^{-2}}{\Omega m}$$

$$C=\begin{bmatrix} 2.926 & -0.8069 & -0.238 & -0.11102 \\ -8.0696 & 3.2647 & -0.7933 & -0.2161 \\ -2.3807 & -0.7933 & 3.2224 & -0.70863 \\ -1.11 & -0.21611 & -0.70886 & 2.834 \end{bmatrix} \frac{pF}{m}, \quad R=\begin{bmatrix} 74.579 & 3.3349 & 2.6902 & 2.6501 \\ 3.3349 & 74.66 & 3.1719 & 2.7571 \\ 2.6902 & 3.1719 & 74.373 & 3.345 \\ 2.6501 & 2.7571 & 3.345 & 74.513 \end{bmatrix} \frac{\Omega}{m}$$

The frequency response of the microstrip bends in the devices were modeled as excess capacitances and characterized using scalable models discussed in Section 3.4. The capacitance of the bends in this configuration is the dominant behavior compared to the inductance of the bends. However, it is worth mentioning that in some other devices the inductance could dominate or play an equal role compared to the excess capacitance in similar discontinuities. In all these scenarios the use of scalable models would be an efficient method to characterize the frequency response of such discontinuities as a function of physical parameters.

The measurements were made using an Agilent Vector Network Analyzer using 1-port short-open-load-thru (SOLT) calibration. Chapter 4 provides further details on the procedure used to make measurements for the high Q passive devices. The results show good correlation with measured data. The disparity between the modeled Q and measured Q for the 1 loop inductor can be explained due to the uneven metallization, which is a

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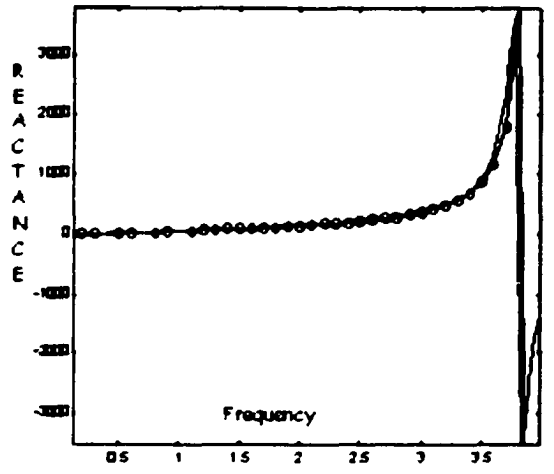

Figure 3.16a. Reactance of 1 loop inductor

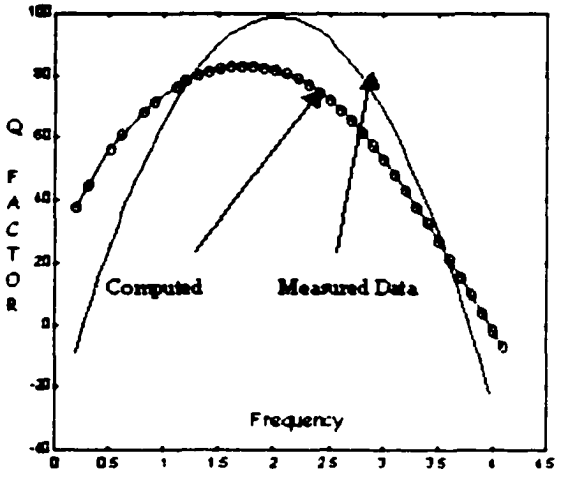

Figure 3.16b. Q-factor of 1 loop Inductor

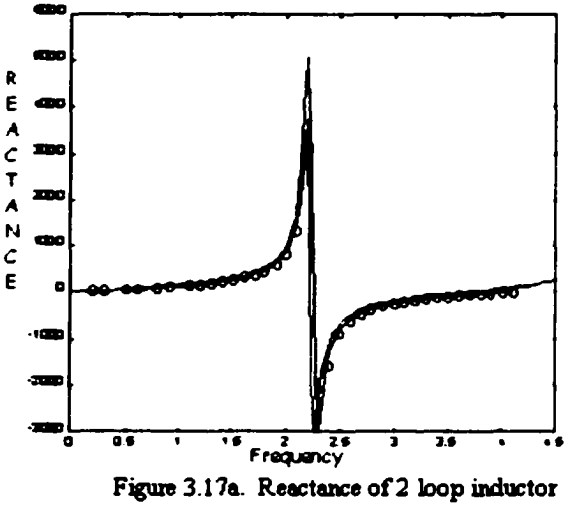

Figure 3.17a. Reactance of 2 loop inductor

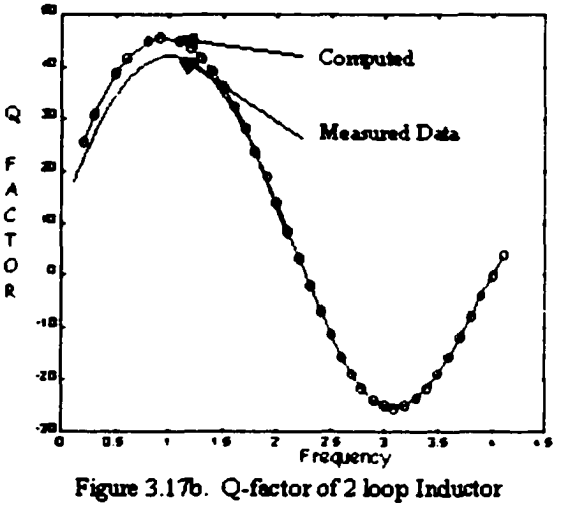

Figure 3.17b. Q-factor of 2 loop Inductor

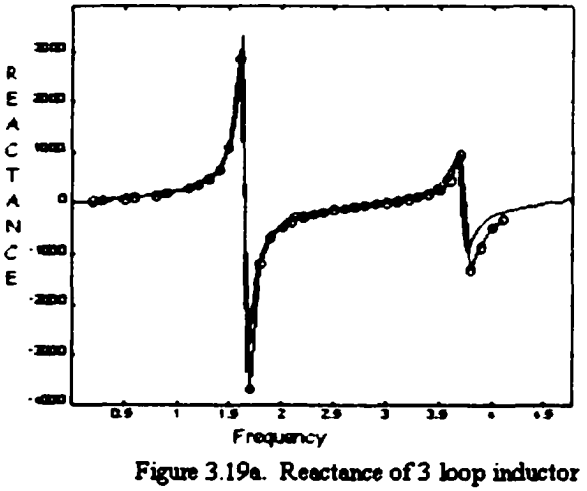

Figure 3.19a. Reactance of 3 loop inductor

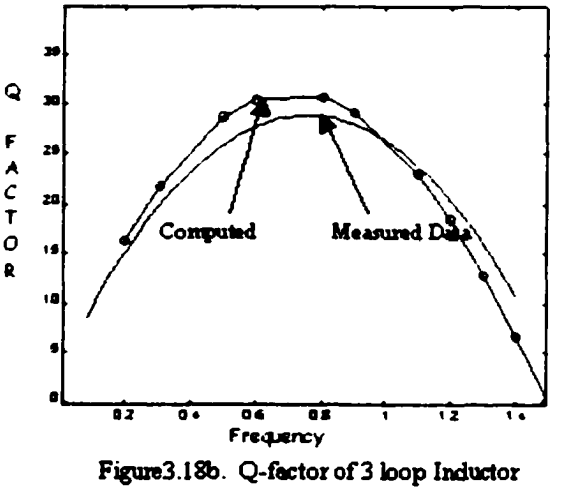

Figure3.18b. Q-factor of 3 loop Inductor

random effect on plated up metal layers in MCM-L processes. This can be prevented by using an etch back method instead of using the plate-up method. Both these techniques have been discussed in detail in Appendix A. The high Q-factors of the inductors despite an inherently lossy substrate show the lack of influence of dielectric loss on the overall

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loss of passive devices over the frequency range of interest. These high Q-inductors in inexpensive MCM-L technology using the lowest cost material set proved to be a good alternative to expensive Low-temperature-cofired-ceramic (LTCC) technology for high performance RF passive circuit design.

It is important to note that the modeling technique captured the response of structures with multiple resonance, as is evident from 3.18a.

Table 3.1, shows the tabulated data for the inductors shown in Figure 3.12. A max Q-factor of 99 was obtained for the one loop inductor. Max Q-factors of 41 and 25 were obtained for the 2-loop and 3-loop microstrip inductors, respectively.

Type	Qmax		L(nH)		Area	SRF(GHz)	
	Meas.	Model	Meas.	Model	(mils^2)	Meas.	Model
1 loop microstrip	99	81	11	10.9	240 * 21	3.6	3.6
	Measured at 2.2 GHz						
2 loop microstrip	41	44	20.5	20.6	240 * 60	2.2	2.2
	Measured at 1.2 GHz						
3 loop microstrip	25	29	29	28.92	240 * 86	1.6	1.6
	Measured at 0.65 GHz						

Table 3.1. Tabulated data for Microstrip Loop Inductors

The preceding work is a fast and accurate technique for simulating complex electromagnetic structures such as 1-port inductors. The structures were also simulated in SONNET for the purposes of comparison. Although the inductance and SRF were predicted

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accurately by SONNET, the loss was overestimated by ~100%. The next section shows the application of the method for modeling capacitor devices.

3.7 Model to Hardware Corelation for Capacitors

Several inter-digital capacitors such as the one shown in Figure 3.19 were processed on the same base organic technology used to process the inductors. Due to the unevenness of the dielectric thickness for reasons mentioned earlier, parallel plate capacitors were used only after thicker laminates were available. Initially, only inter-digital capacitors were fabricated on the FR-4 substrate itself. The capacitors were configured in a coplanar-waveguide (CPW) topology as shown in Figure 3.19. The capacitors were then measured as two port devices using a Vector Network Analyzer (HP 8720) after using SOLT calibration. The capacitors were also modeled using the segmentation method to show model to hardware correlation. In order to demonstrate the advantage of the modeling technique, the capacitors were modeled in SONNET and then simulations were compared in terms of computational time and accuracy in predicting loss and capacitance.

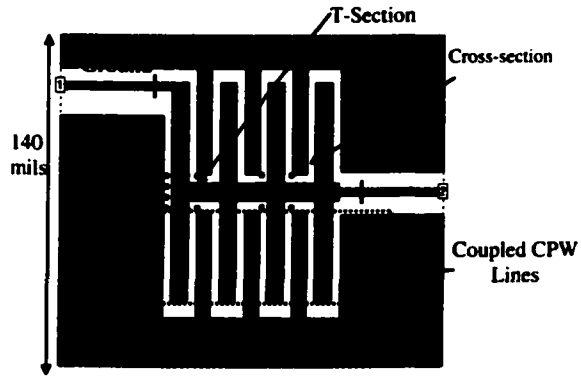

Figure 3.19 Inter-Digital Capacitor

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The dotted areas in Figure 3.19 represent the major blocks that were used to construct the electrical model for the capacitors. The seven coupled coplanar waveguides (CPWs) referenced to the ground constitute the fingers of the capacitor, which were modeled as coupled lines using the approach mentioned earlier. The discontinuities, which are critical to the performance of the capacitor, are the cross-sections and T-sections also shown in Figure 3.19.

The cross-section for the coupled lines in Figure 3.20 was used to obtain the coupled line R, L, G, C matrices from ANSOFT 2D. The spacing (S) between the lines is 3 mils and the width (W) of the lines is 6 mils. The thickness of the lines is ~18 microns. The 3 mil spacing is the minimum line spacing allowed in the design process and the 6 mil line width is the minimum line width that prevents the influence of the line profile on the performance of the device. (A detailed list of design rules are available in Appendix B). The dotted lines in figure 3.20 are the lines that were connected to ground and the filled

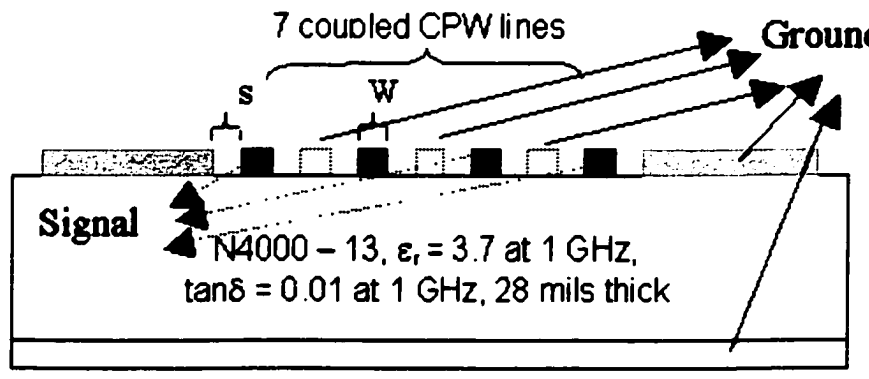

Figure 3.20 Cross-section for the Coupled CPWs used in the inter-digital capacitor in figure 3.19

lines represent the signal carrying lines of the capacitor, which are connected to each other via the cross-sections and T-sections. Since the capacitor in Figure 3.19 is a shunt capacitor, Z_{11} is a good measure of its performance. Figures 3.21a and 3.21b show the

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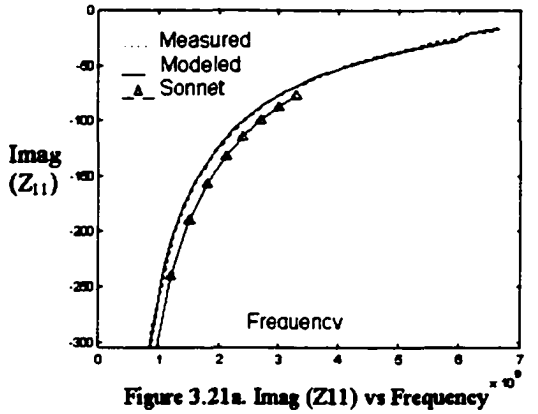

Figure 3.21a. Imag (Z11) vs Frequency

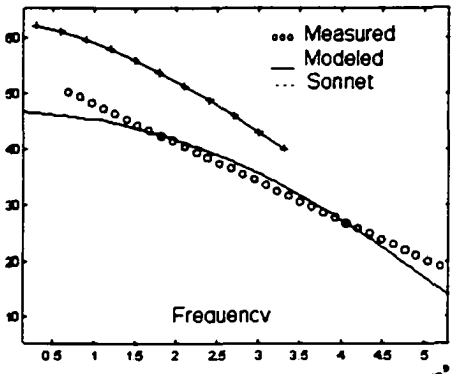

Figure 3.21b. Imag (Z_{11}) / Real (Z_{11}) vs. Frequency

modeled and measured reactance (imag(Z_{11})), and the Q-factor (imag(Z_{11})/real(Z_{11})), for the capacitor, respectively. The modeled data shows good correlation with measured data for both the reactance and Q-factor. The reason for a small disparity between SONNET data and measured data can be attributed to the modified geometry of the capacitor that was modeled in SONNET since the original geometry resulted in a mesh that was too large in SONNET. However, this is not a limitation of the modeling technique discussed in this chapter. Even with the modified geometry, SONNET took about 1.5 hours to simulate the response for nine frequency points on an Ultra 30 Sparc Station, whereas the modeling technique including the time to obtain the R, L, G, C parameters from ANSOFT 2D on a 600 MHz Celeron Processor took about 23 minutes.

The next section discusses the application of the segmentation method for modeling the coupling between devices.

3.8 Coupling between Inductors

Several 1-port microstrip loop inductors, processed on organic substrate, were measured and characterized in the last section. The results showed good agreement

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between measured and modeled data. Based on the results in modeling individual inductors, the method was applied to model the coupling between inductors. Figure 3.22 shows two 1-port inductors (with ports 1 and 2 as the input ports of the two inductors) modeled in SONNET on the same multi-layered lossy substrate. The structure was modeled using the technique mentioned in the previous section; however, in this instance the result was obtained as a 2 port response instead of a 1-port inductor response. The 2 port response captured the coupling of two 1-port inductors. The comparison of the responses obtained from SONNET and the modeling technique is shown in Figure 3.23.

The results show good correlation and capture the coupling effect ($Z_{12} = Z_{21}$) between the two inductors. It is important to note that the coupling is a function of the distance between the inductors and also the cross-sectional configuration of the two inductors. Optimization of the coupling and isolation parameters based on a full-wave tool such as SONNET can get very tedious. SONNET took about 26 minutes to simulate the response

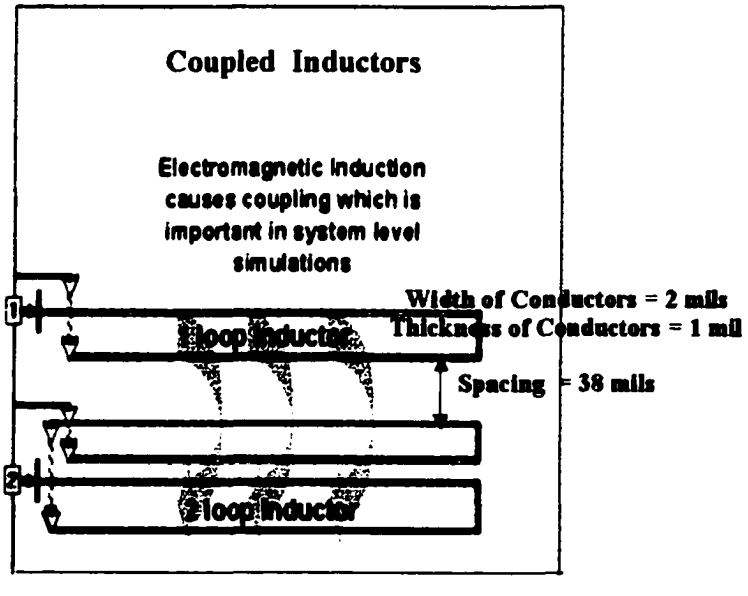

Figure 3.22 Two 1-port loop inductors coupled due to close proximity

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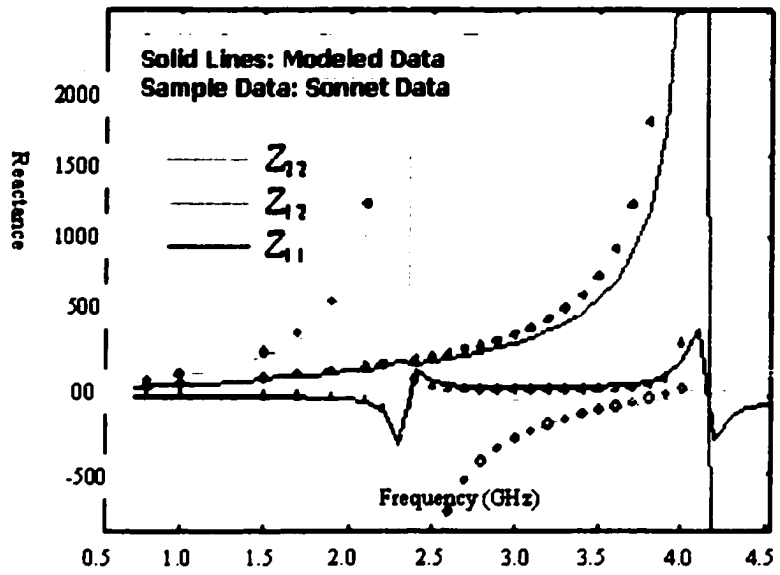

2 port parameters for coupled inductors

Figure 3.23 Coupling between inductors

for twenty four frequency points on Ultra 30 Sparc Station, whereas the modeling technique including the time to obtain the R, L, G, C parameters from ANSOFT 2D on a 600 MHz Celeron Processor took about 12 minutes. Tools such as the Advanced Design Suite (ADS) by Agilent can model the coupling of ideal inductors or model lossy inductors as a function of frequency with the aid of design equations but cannot model the coupling of lossy inductors. The technique discussed in this paper is a hybrid technique, which is circuit based and is more adaptable for the optimization of embedded RF circuits. This is primarily due to the use of 2D analysis for electrically large structures, use of 3D analysis for electrically short structures and the ability to combine these results through the segmentation method.

3.9 Summary

In this chapter, a method for modeling passive devices integrated in organic substrates has been presented. This method provides a fast and accurate way to optimize and model the performance of passive circuits consisting of multiple-coupled line sections cascaded to one another using multiple coupled line parameters and scalable models. This is useful for

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new processes where models are currently unavailable and predictive modeling can sometimes get very tedious. It also provides independence from full wave simulators, which are computationally expensive to use and sometimes use assumptions, which might be inappropriate for a particular process. The modeling technique discussed in this chapter can be used to incorporate different topologies such as CPW and microstrip (ground reference below the signal layers) along with important process parameters such as varying dielectric constant and non-uniform conductor profiles.

In conclusion, the initial data for the inductors demonstrates the possibilities of using a completely organic low-cost technology with epoxy-based substrates to achieve Q's as high as 100 for inductors greater than 10nH at frequencies above 1 GHz in an area less than $3mm^2$. If the inductance were to be reduced by using smaller loops, the nominal resistance due to the decreased lengths of loops would decrease and provide Q's (> 150) sufficient for applications such as front-end filters discussed in Chapter 1. The data for the capacitors was not very promising as far as the capacitance density (pF/mm^2) and Q-factor were concerned. The capacitance density using interdigital fingers is restricted to $0.1pF/mm^2$ due to a minimum line-to-line spacing of just 3mils. The use of parallel plate capacitors, which can provide densities of $1pF/mm^2$, is imperative but only with the use of thicker dielectrics or uniform metalization to achieve uniformity in dielectric thickness. Chapter 4 discusses the design, optimization and comparison of different topologies for inductors and parallel-plate capacitors suited for performance in different frequency bands. The use of newer laminate materials like PPE™ and Zyvex™ with lower loss and greater thickness compared to Vialux has also been evaluated for embedded passive applications in Chapter 4.

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CHAPTER IV

4. DESIGN OF INDUCTORS AND CAPACITORS IN LAMINATE TECHNOLOGY

Introduction

Commercially available thin-film ceramic-chip capacitors and inductors for RF and power applications from AVX, Kyocera and Murata, to name a few, have provided needed miniaturization of devices with sizes down to 2mm by 1mm. Inductors and capacitors with high enough Q's for filter applications have been demonstrated. However, as mentioned earlier, some of the disadvantages with discrete passive devices are the: 1) lead time of 4-6 weeks when buying high performance passives, 2) costs of assembly, 3) unpredictability and degradation of performance after assembly.

This chapter discusses the design of high Q inductors and capacitors in organic substrates. Inductors with maximum quality factors in the range of 60-180 were obtained at frequencies in the 1-5 GHz band for inductances in the range of 1nH - 20nH. This is the first demonstration of such high Q inductors in organic substrates.

Capacitors with maximum quality factors in the range of 50-250 were obtained at frequencies greater than 1 GHz depending on the dielectric material used. The dimensions of all inductors and capacitors were comparable to a LTCC process and well suited for integration in a variety of applications. The various inductor and capacitor designs, and trade-offs between different topologies, have been discussed in this chapter.

Using the modeling approach described in Chapter 3, several microstrip loop inductors and microstrip spiral inductors were designed and implemented for optimal performance in the bands of interest. The measured quality factor for all microstrip inductors was sufficient for applications such as front-end filters mentioned in Chapter 1. However, a major problem

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in a microstrip inductor topology is the reference to the ground plane, which requires plated through holes or a post-process drilling technique. Another major problem in the design of microstrip inductors is current crowding on the ground plane, which increases the loss of the device, thereby decreasing the unloaded quality factor (Q). However, coplanar waveguide (CPW) inductors with a hollow-ground plane reduce the current crowding effect in microstrip inductors by forcing the current to flow on the larger coplanar ground on the same layer. The Q factor increases by 20-30% with a CPW type topology compared to the microstrip topology.

This chapter is organized as follows: section 4.1 discusses the different inductor topologies that were explored in this dissertation. In section 4.2 the details of the organic process and testbed have been discussed. Various design parameters such as parasitic capacitances and higher order losses of inductors are discussed in section 4.3. The measurement technique used for characterizing the inductors is discussed in section 4.4. This is followed by section 4.5 that provides details on the design of microstrip spiral inductors. In section 4.6, microstrip loop inductors have been discussed for the specified bands of interest and compared to the traditional microstrip spiral inductors. The design of CPW/hollow-ground inductors is introduced in section 4.7. A comparison between the different topologies is discussed in section 4.8. Section 4.9 discusses the construction of equivalent circuit models for the inductors. The design and comparison of capacitors in different substrates is discussed in section 4.10. Finally section 4.11 discusses the construction of equivalent circuits for capacitors.

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4.1 Inductor Topologies

The commonly used topologies for the design of inductors are shown in Figure 4.1. They consist of multi-turn spirals and multi-turn loops. Using a ground plane, the structures in Figure 4.1 can be implemented as a microstrip or coplanar waveguide (CPW) configuration. For the microstrip configuration, the ground plane is implemented as a solid metal sheet below the current carrying conductors of the device as was shown in Chapter 3. Unlike the microstrip inductor, the CPW inductor is implemented by having a wide ground ring around the device with or without any backside metallization.

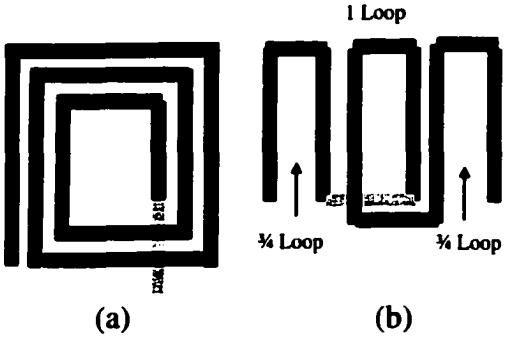

Figure 4.1 a) 3 turn Spiral b) 2½ loop

The trade-offs between the topologies in Figure 4.1 are explained in this chapter. The parameters of interest for the design of an inductor are its inductance, Q-factor and self resonant frequency (SRF). Amongst the three parameters, a high Q factor is the most difficult to achieve for the inductors. This is because the Q factor is affected by the losses in the device, which largely depend on the inductor topology and physical parameters such as line widths, line thickness, line spacing, etc. Though the number of inductor topologies and physical dimensions that can be implemented are endless, this chapter discusses only three topologies with appropriate dimensions based on the process. The three topologies as mentioned are the microstrip loop, microstrip spiral and CPW inductors.

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4.2 Inductor Testbed

Figure 4.2 shows the fabricated samples of microstrip spiral (Figure 4.2a), microstrip loop (Figure 4.2b) and CPW loop (Figure 4.2c) inductors.

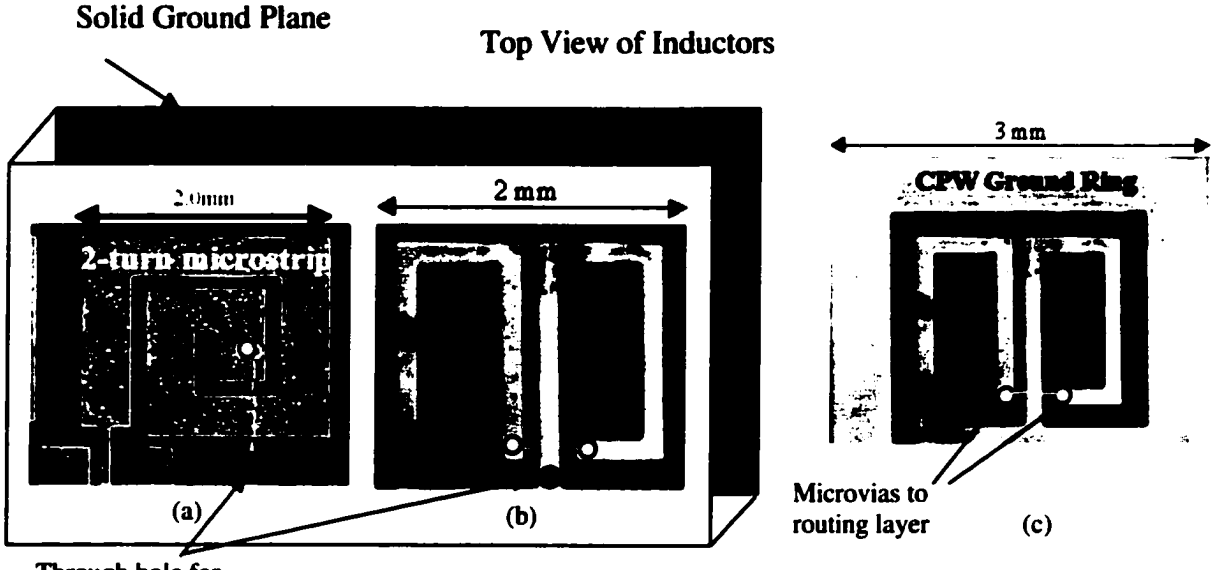

Figure 4.2. Fabricated inductor topologies
a) 2 turn Spiral b) 1 ¾ loop c) 1 ¾ CPW loop

The initial testbed for fabricating these inductors was obtained by laminating Vialux™ on a conventional 28 mil (~700um) printed wiring board FR-4 core. The reason for choosing a thinner core compared to the substrate shown in Chapter 3, was to reduce the tolerances due to a thicker core. Using one build up layer ensured maximum yield by eliminating via registration and alignment problems for multi-layered processes. For under-routing and connectivity between devices one build-up layer with microvias was sufficient. The cross-section of the test vehicle is shown in Figure 4.3. The design rules mentioned in Appendix B were used for the inductors. Since plated through holes (PTH) add processing complexity, no PTH were used for backside connections. All backside connections for microstrip type

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topologies were made using post-process mechanical drilling techniques with 20 mil diameter holes. These holes were then filled with silver paste for via connectivity.

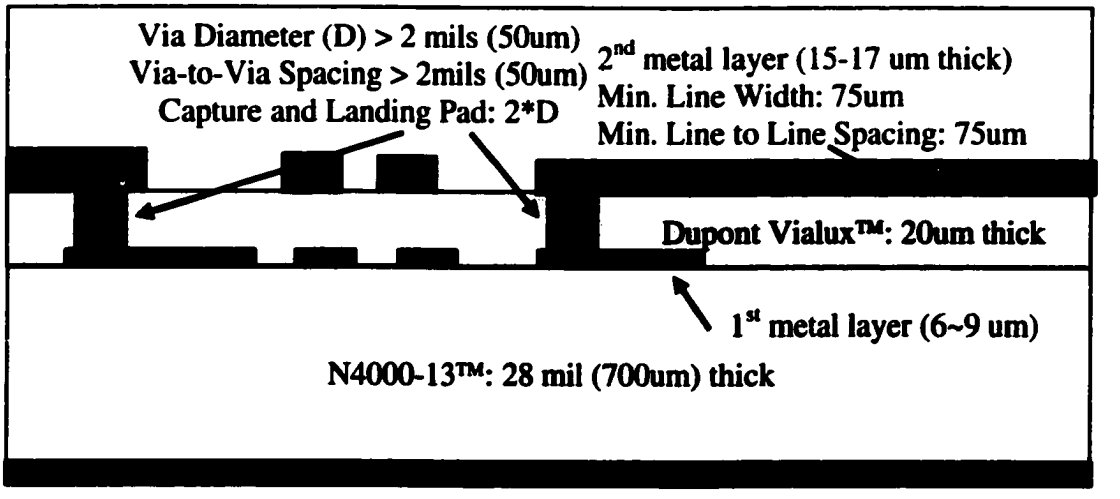

Figure 4.3. Cross-section of Testbed

4.3 Design and Optimization of inductors

The embedding of inductors in multi-layered substrates enables the reduction in surface area and volume occupied by the discrete inductor components. Hence, an important criterion in the design of inductors is the surface area and the volume occupied by the inductor in the substrate. In this paper all the microstrip inductors, spiral and loop, were limited to an area of $4.5mm^2$, a height of 0.7mm, and a volume of $3mm^3$. This constraint ensured the small size of inductors ideal for integration in communication devices.

For the minimization of losses in the device, a clear understanding of the contribution of conductor loss and dielectric loss in the device is required. By modeling the structure with a perfect conductor or perfect dielectric, the effect of conductor loss and dielectric loss on the total loss of the structure could be separated from each other. A "sqrt(f)" and "f" frequency dependence were assumed for the conductor and dielectric loss respectively, while modeling

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the device. Figure 4.4 and Figure 4.5 show the contributions of dielectric loss and conductor loss to the total loss in the device for the 1-port 1.75 loop inductor and the CPW inductor, respectively. The total loss in Figures 4.4 and 4.5 represents the real part of the impedance for the 1-port inductors. As seen in Figure 4.6, the Q for the 1.75 loop microstrip inductor reaches its maximum value at ~1.3 GHz, where the total loss in the device is dominated by the conductor loss. Additionally, as seen in Figure 4.6, the Q for the 1.75 loop CPW inductor

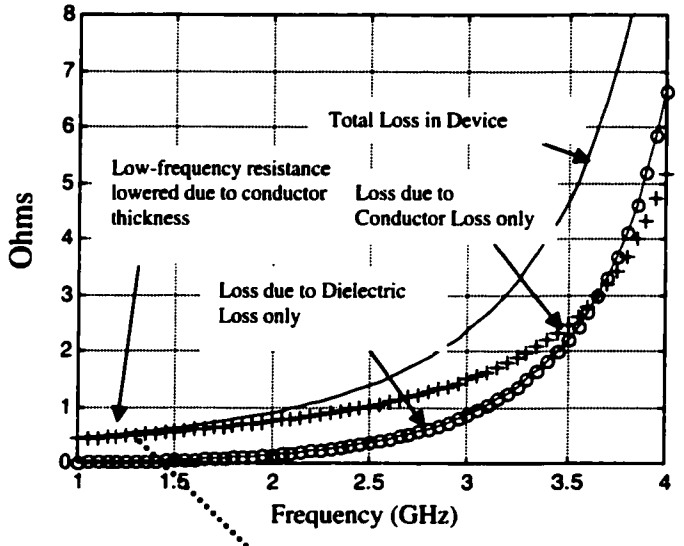

Figure 4.4. Losses in 1.75 loop Microstrip inductor

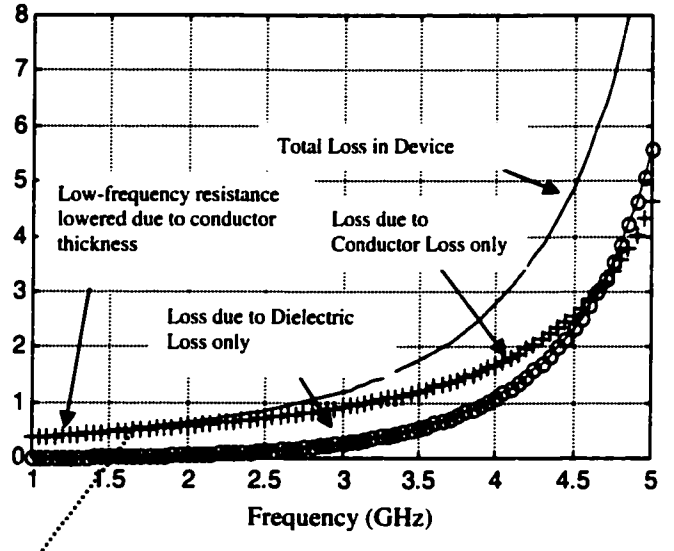

Figure 4.5. Losses in 1.75 loop CPW inductor

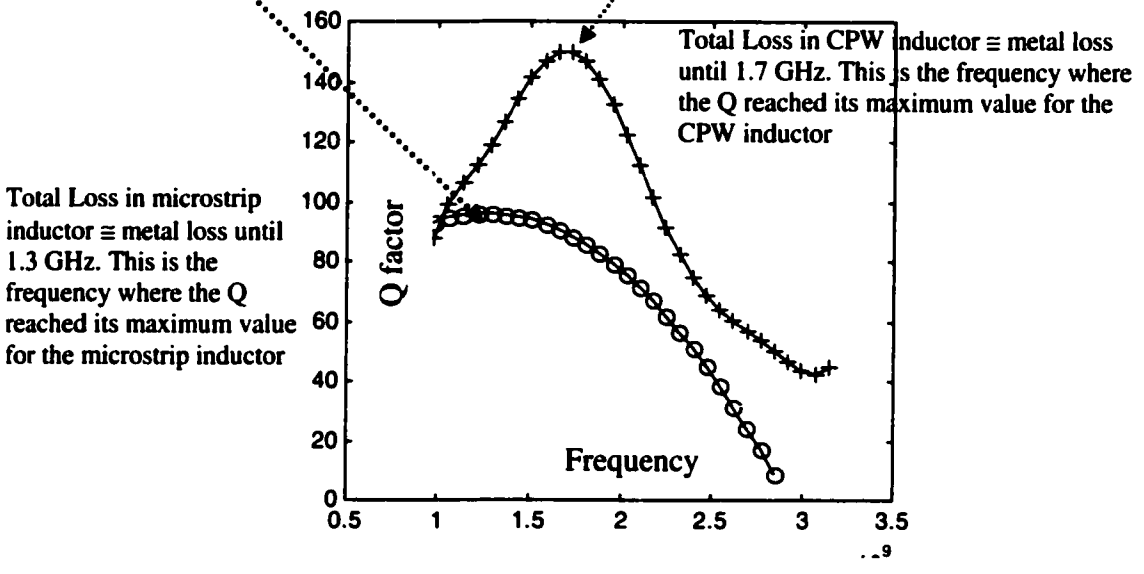

Figure 4.6 Measured Q vs. Frequency for the microstrip inductor and CPW inductor

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reaches its maximum value at ~1.7 GHz, where the total loss in the device is dominated by the conductor loss. Beyond this frequency, the dielectric loss begins to come into play and reduces the Q of the device.

From Figure 4.4, the dielectric loss begins to dominate the loss at 3.7 GHz for the microstrip loop inductor. This crossover point is increased to 4.7 GHz for the CPW inductor. Since conductor loss is the dominant loss for the inductors over the frequency bandwidth (1-3 GHz) of interest the conductor thickness can be suitably increased to obtain the desired Q. Conductor thickness of 15~17um was used to lower the DC resistance of the device which increased the Q by compensating for the loss in the epoxy-based dielectric materials. Another important observation from these two examples is that the frequency (f_d) at which the dielectric loss is larger than the conductor loss scales inversely with the inductance of the device. As an example, for the loop inductor with a low-frequency inductance of 6.4nH, f_d = 3.7 GHz; for the CPW inductor with a lower inductance of 5.0nH, f_d = 4.7 GHz. Assuming the loss tangent of the material is similar at higher frequencies, lower value inductors with high Q can be implemented at higher frequencies. One implementation is for HyperLAN applications (5.2-5.8 GHz) which require inductances less than 5nH.

Besides dielectric losses, other parasitics that influence the behavior of inductors are current crowding effects and parasitic capacitance. Parasitic capacitance can be separated into the series capacitance and the substrate shunt capacitance of the interconnects in the inductor structure. Based on the inductor's physical structure, both the coupling between adjacent turns and that between the inductor and the under-routing contribute to the series capacitance. However, since adjacent lines are almost of the same potential, the effect of cross coupling is negligible. Use of very thin lines for underpasses can minimize the

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capacitance between the inductor and the under-routing signals. The organic process used in this research allows the fabrication of 2mil (50um) lines, which enables the reduction of the series capacitance. Using 28 mil thick cores such as the FR-4 core in Figure 4.3, the substrate shunt capacitance can be greatly reduced. A larger separation between the signal and ground plane also increases the characteristic impedance, Z_o, of the lines for the same width. This reduces the signal attenuation due to conductor losses, which are inversely proportional to the characteristic impedance of the lines.

Finally current crowding related losses due to eddy currents, skin effect and edge effects can together reduce the Q of inductors significantly. A plot of the current distribution at 2.5 GHz for the loop inductor and spiral inductor is shown in Figure 4.7.

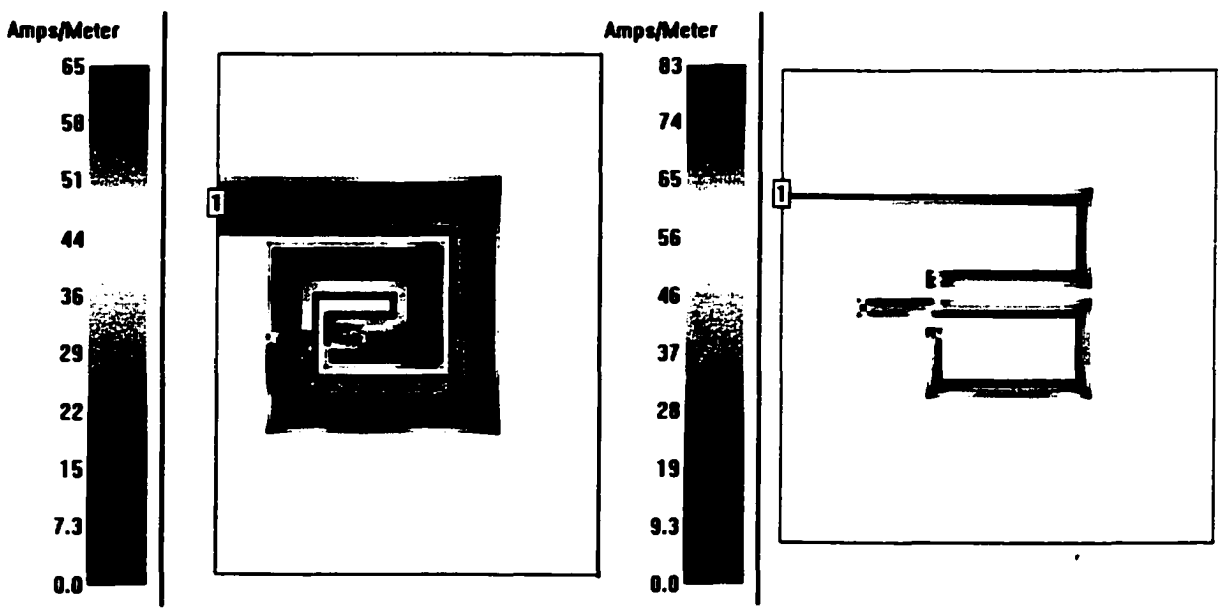

Figure 4.7 Current Distribution for Loop Inductor and Spiral Inductor

These results were obtained using SONNET. From the figure, current crowding is more prevalent in the spiral inductor. The wider conductors of the spiral have a smaller DC resistance as compared to the narrow conductors of the loop inductor in Figure 4.7. Since

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both topologies are microstrip type inductors, the edge effects (where the current crowds on the edges of the conductors at higher frequencies) are similar for the outer conductors of the two structures. However, the current crowding seen in the inner turn of the spiral due to eddy current effects is much more than the inner conductors of the loop. Hence, the microstrip loop inductor will have a smaller conductor loss. However, the increase in conductor loss in the spiral is compensated by the increased inductance due to the larger number of positively coupled conductors. Hence, the Q, which is defined as the ratio of reactance to resistance remains unchanged for the two inductors in Figure 4.7.

4.4 Measurement of High Q Devices

The fabricated inductors on a 4" by 4" test vehicle are shown in Figure 4.8.

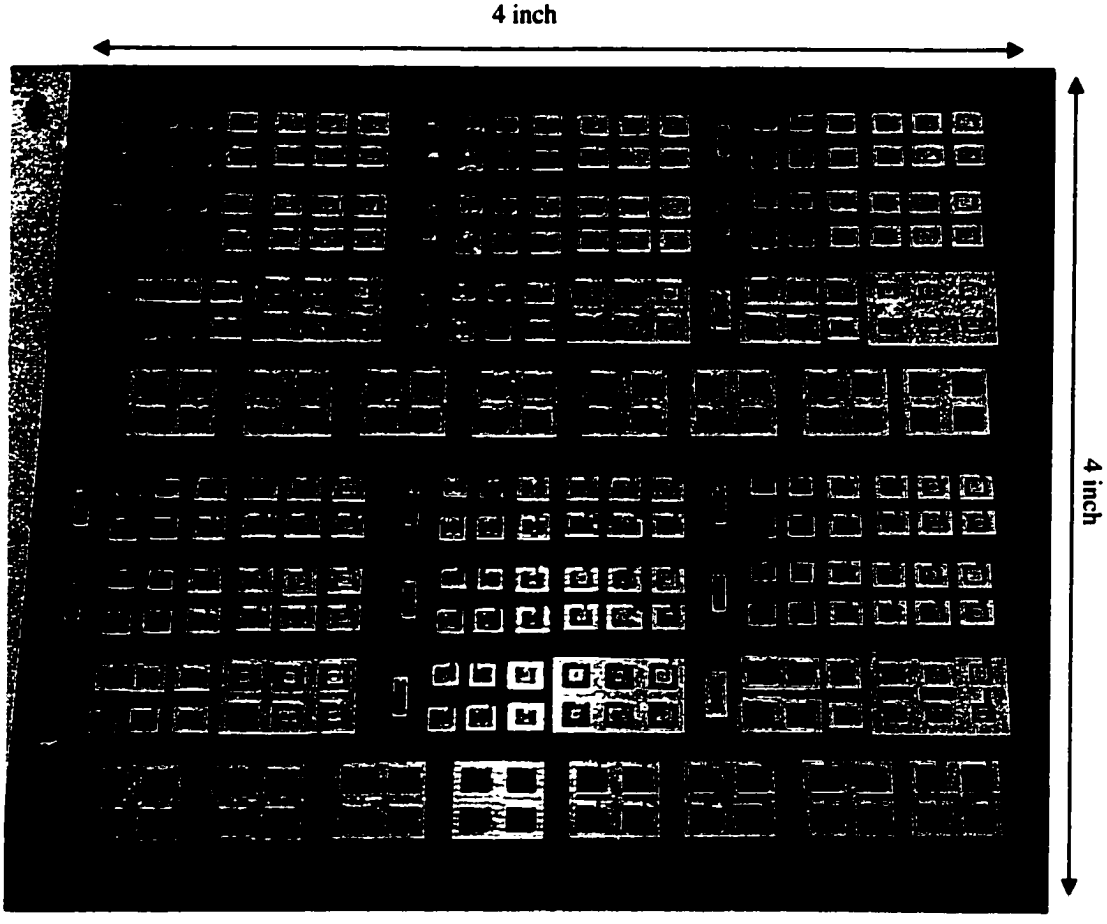

Figure 4.8 Top View of 4" * 4" quadrant of testbed. Substrate shown in Figure 4.3

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A good measurement setup and an accurate calibration procedure for the characterization of high Q inductors is required. In this chapter, a 1-port Short-Open-Load (SOL) calibration was used with Agilent's 8720ES vector network analyzer (VNA). The 1-port SOL calibration for inductors is available in all commercial VNAs and is simpler than 2-port standards such as thru-reflect-line (TRL) and line-reflect-reflect-match (LRRM). Since the parasitic values of the inductors are largely dependent on the probe contact with the standards, all standards must be contacted appropriately [31]. A 1-port calibration enables correct alignment and placement during calibration than 2-port calibration procedures. In addition, the SOL standards are well characterized using lumped circuit elements such as open-circuit capacitance, short-circuit inductance and load, all of which are available from Cascade Microtech [32]. In this chapter, 150um and 500um pitch air coplanar (ACP40) probes from Cascade Microtech were used for making measurements. Since the DC resistance for all inductors measured with a standard LCR meter was on the order of 0.05Ω~ 0.1Ω, it was important to calibrate to within 5mΩ-10mΩ of accuracy and repeatability using the VNA. A good measure for ensuring accuracy of measurements for high Q inductors is the measurement of the short standard after calibration. The measured short standard resistance after calibration should be stable and smaller than the DC resistance of the inductor to be measured. In this paper, the short calibration standards for the 150um and 500um pitch probes measured 5mΩ, which is lower than the DC resistance of the inductors. To enable stable measurements an averaging factor of 64 was used with 400-800 sampling points.

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4.5 Microstrip Spiral Inductors

As mentioned earlier all the microstrip inductors (spiral and loop) were limited to an area of 4.5mm^2, a height of 0.7mm, and a volume of 3mm^3. This constraint ensured the small size of inductors ideal for integration in communication devices.

The most conventional design for inductors is the multi-turn spiral with smaller turns embedded inside larger loops. With the given organic process, as mentioned earlier, it is possible to have minimum line widths of 3 mils (75um) with a ground to signal separation of 28 mil (700um) using FR-4 plus 1mil (25um) of Dupont Vialux™ dielectric.

However, in [32], line widths as high as 20 mils were used in a multi-layer LTCC process for inductors with performance in the 1.8GHz band although the technology allows for line widths down to 4-5 mils. For inductors with thinner lines the shunt capacitance to ground is reduced compared to those with wider lines. However, due to the reduced shunt capacitance the SRF becomes higher and correspondingly the Q reaches its peak value at a higher frequency. While higher SRFs are optimal for broadband circuits, most wireless devices are narrowband and require high Q in the desired band at the cost of lower SRF. By having larger line widths in [33], the smaller inductances (<3nH) were optimized to achieve maximum Q's at lower frequencies (1 GHz -3 GHz). The distance to the ground plane in [32] for some of the wide strip inductors is 22mils, which is comparable to the separation available in the organic process. Figure 4.9 shows five different spiral inductors with line widths varying from 7 mils to 34 mils with a maximum spacing of 4 mils implemented using the cross-section in Figure 4.3. A large conductor width of 34 mils proved optimal for a 1.5nH inductor (inductor #5) with a max Q factor of 180 at 2.4 GHz. The tight spacing of 4 mils ensured that every inductor area was less than or equal to 4.5mm^2 and inductor volume

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was less than or equal to $3mm^3$. Table 4.1 shows the measured data for the spiral inductors.

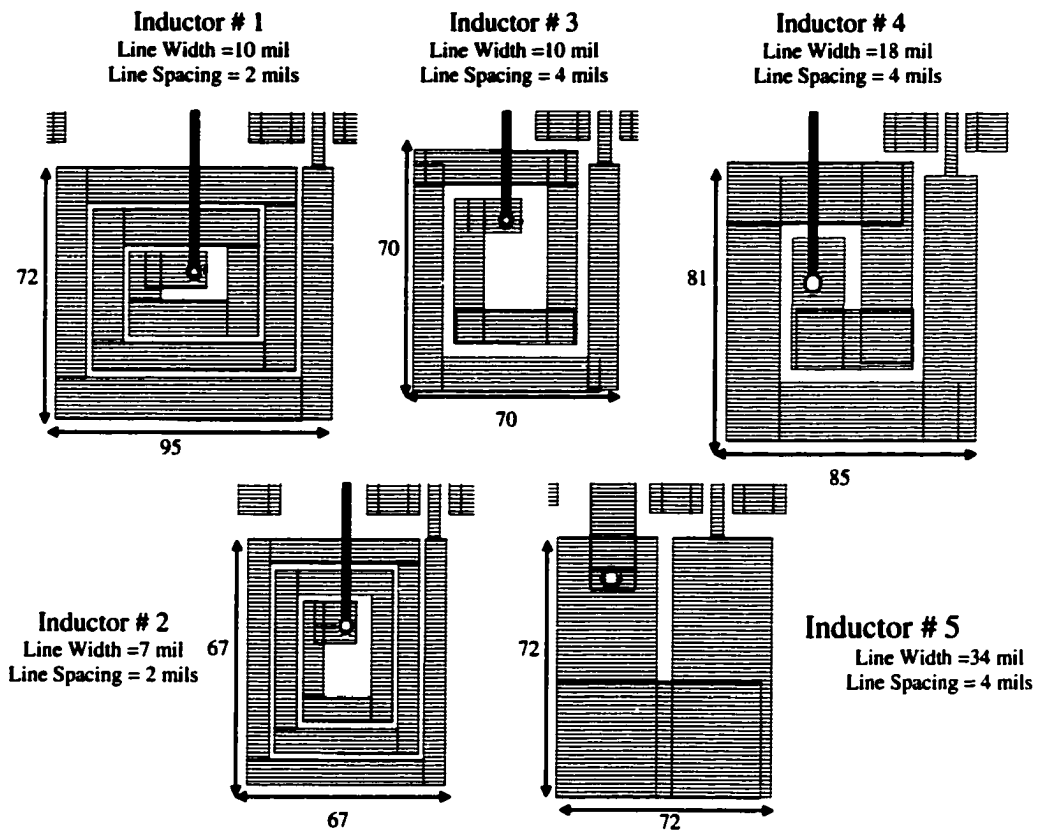

Figure 4.9. Microstrip Spiral Inductors

Table 4.1. Measured data for Wide-strip Narrow-spacing Microstrip Spiral Inductors shown in Figure 4.9

Inductor	Max Q (Peak Q Frequency)	Effective Inductance	Area	SRF (GHz)
Inductor 1	80 at 1.5 GHz	12nH at 1.5 GHz	$4.4mm^2$	3.9
Inductor 2	100 at 1.0 GHz	12nH at 1.0 GHz	$3.1mm^2$	3.2
Inductor 3	100 at 2.0 GHz	7nH at 2 GHz	$3.2mm^2$	6.8
Inductor 4	110 at 2.0 GHz	5.2nH at 2 GHz	$4.5mm^2$	7
Inductor 5	170 at 2.4 GHz	1.5nH at 2.4 GHz	$3.2mm^2$	8.5

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As an example, Figure 4.10 and Figure 4.11 show the measured effective inductance and Q as a function of frequency for inductors #2, #4 and #5. The measurements were done using the methods discussed in section 4.4.

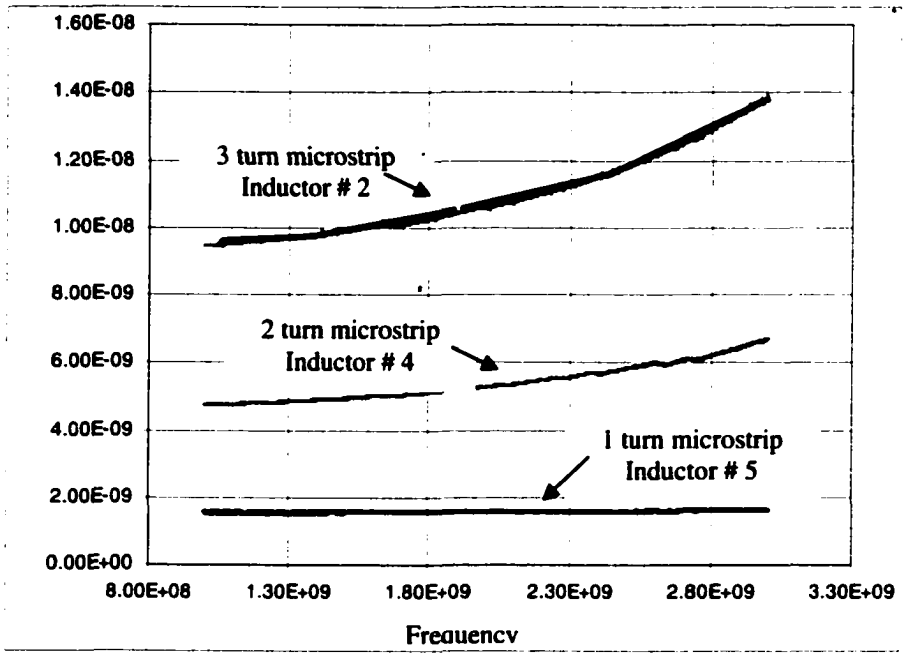

Figure 4.10 Measured inductance vs. Frequency for inductors #2, #4 and #5 of Figure 4.8.

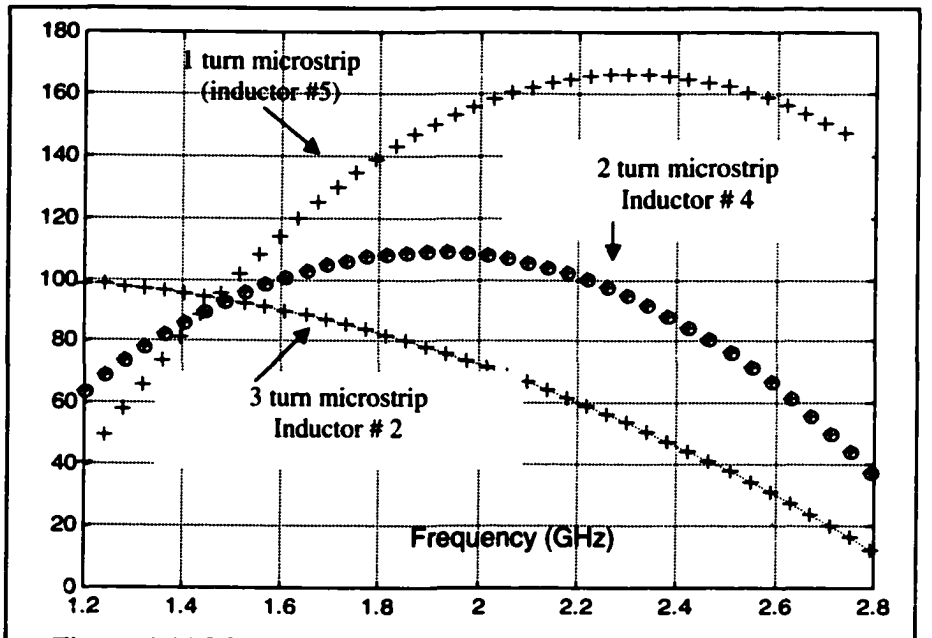

Figure 4.11 Measured Qs for Inductor # 2, # 4, and # 5 of Fig 4.8

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4.6 Microstrip Loop Inductors

Unlike spiral inductors, loop inductors are inductors in which current carrying loops are cascaded in series and not embedded inside larger outside loops. The primary difference between the spiral and loop topology with the same line widths is that the spiral has a higher inductance compared to the loop due to the larger number of positively coupled current carrying segments. In the previous section narrow-width spirals were modified to wide-strip spirals to obtain the best performance in the 1GHz and 1.8GHz-2.4GHz bands. The advantage with topologies that have narrower lines is that the discontinuities such as bends can be treated as ideal shorts and crossovers between narrower lines have negligible parasitic effects. Narrower lines, however, have a higher low frequency resistance, but the eddy current losses

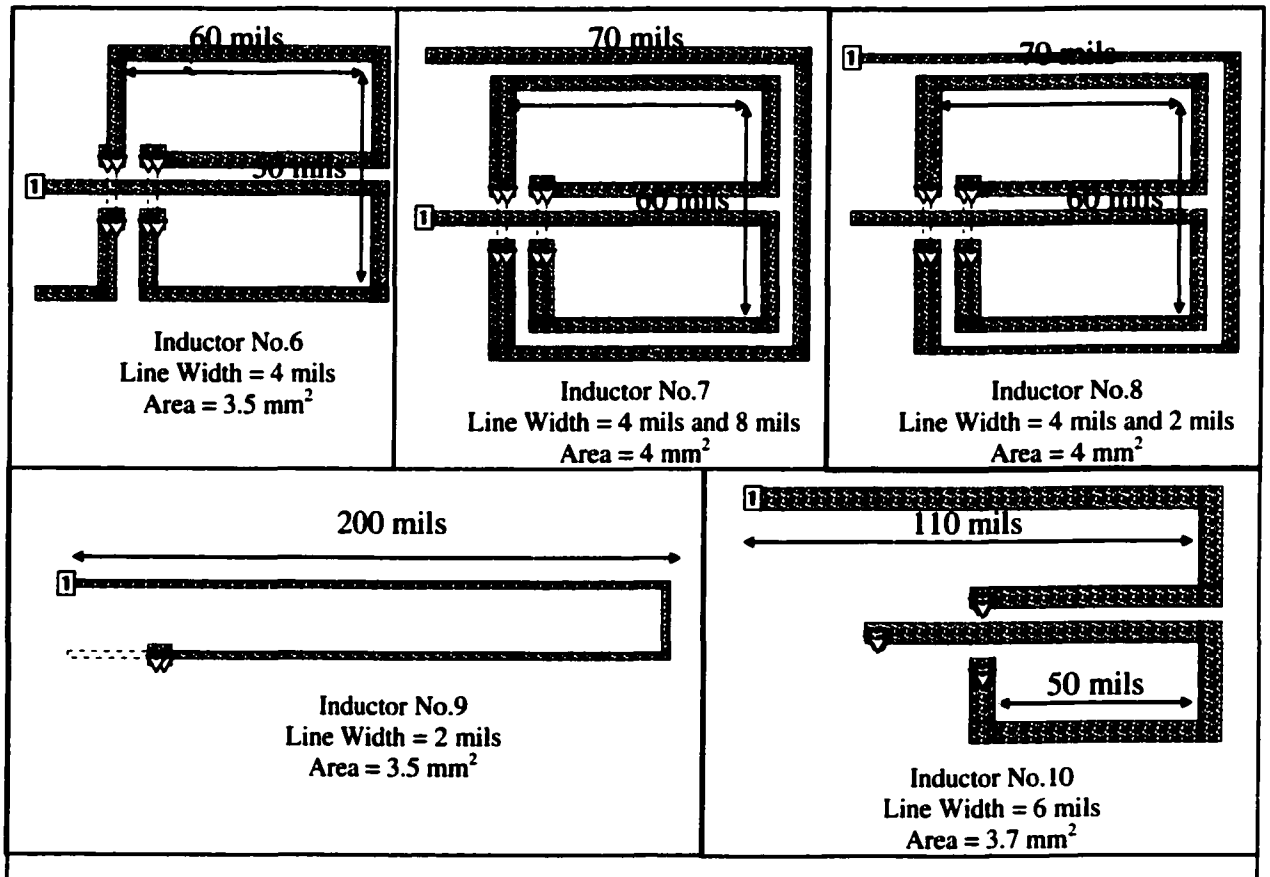

Figure 4.12 Microstrip loop inductors fabricated on substrate shown in Figure 4.3

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in loop inductors are less than in wide-strip and narrow-strip spirals. All designs were configured to have adjacent lines carry current in the same direction to maximize inductance. Figure 4.12 shows several microstrip loop inductors with a common separation of 29 mils (28 mils of FR-4 and 1 mil of Vialux™) below the signal lines. Table 4.2 shows the measured data for the loop inductors in Figure 4.10. The data was collected using the methods discussed in section 4.5. From the table, inductors #6, #9 and #10 are well suited for applications around 2 GHz and inductors #7 and #8 are well suited for applications around 1 GHz. Although both the loop and spiral inductors provided high Q factors with the required inductances, both topologies require a connection to the backside metal due to the presence of the ground plane beneath the spiral and the loop. This is a disadvantage since it adds parasitics due to vias. Another disadvantage with the microstrip topology at higher frequencies is the current crowding on the ground plane beneath the device, which decreases the Q of the inductors.

Table 4.2. Measured data for Microstrip Loop Inductors shown in Figure 4.12

Inductor	Max Q (Peak Q Frequency)	Effective Inductance	Area	SRF
Inductor 6	Q=85 at 1.2 GHz	L=10.2 nH	3.5 mm^2	3.9 GHz
Inductor 7	Q=80 at 1 GHz	L=15 nH	4 mm^2	3.2 GHz
Inductor 8	Q=70 at 1 GHz	L=17 nH	4 mm^2	3 GHz
Inductor 9	Q=90 at 2.4	L=7.68 nH	3.5 mm^2	7.2 GHz
Inductor 10	Q=110 at 2.1	L=7.8 nH	3.7 mm^2	6 GHz

As an example, Figure 4.13 and Figure 4.14 show the measured effective inductance and Q as a function of frequency for inductors #6, #7 and #9. The measurements were done using the methods discussed in section 4.4.

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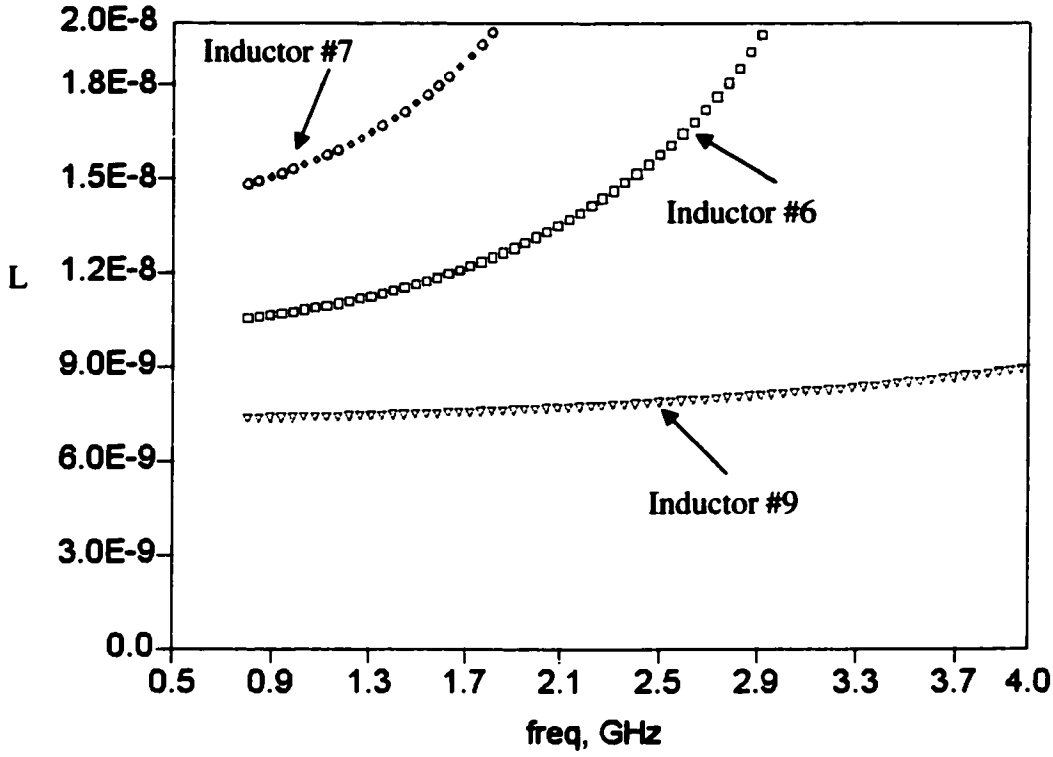

Figure 4.13. Measured inductance vs. Frequency for inductors #6, #7 and #9 of Fig 4.12

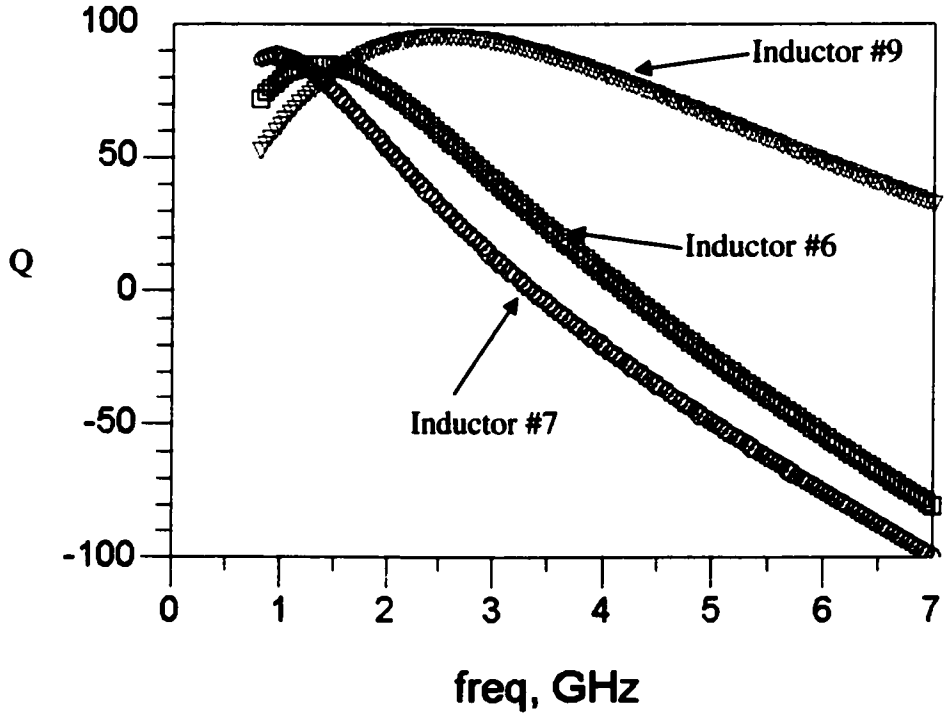

Figure 4.14 Measured Qs for Inductor # 6, # 7, and # 9 of 4.12

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4.7 CPW/Hollow-Ground Inductors

Figure 4.15 shows several CPW inductors that were also implemented on the substrate shown in Figure 4.3. Unlike the microstrip inductors, the ground or the reference for the devices are the wide ground rings around the devices as shown in Figure 4.15. Although this eliminates the need for backside connections, it does increase the area of the device. The CPW topology ensures the proximity of the ground since the interconnections and ground plane are co-planar on the same layer. This prevents the current crowding on the ground planes by forcing the currents to flow around the device on the larger area coplanar ground. The CPW topology does not use the large separation between the ground and signal lines as the microstrip topology does, but the shunt capacitance is significantly lower and effective inductance is much larger. For this reason a CPW or hollow-ground topology was also investigated.

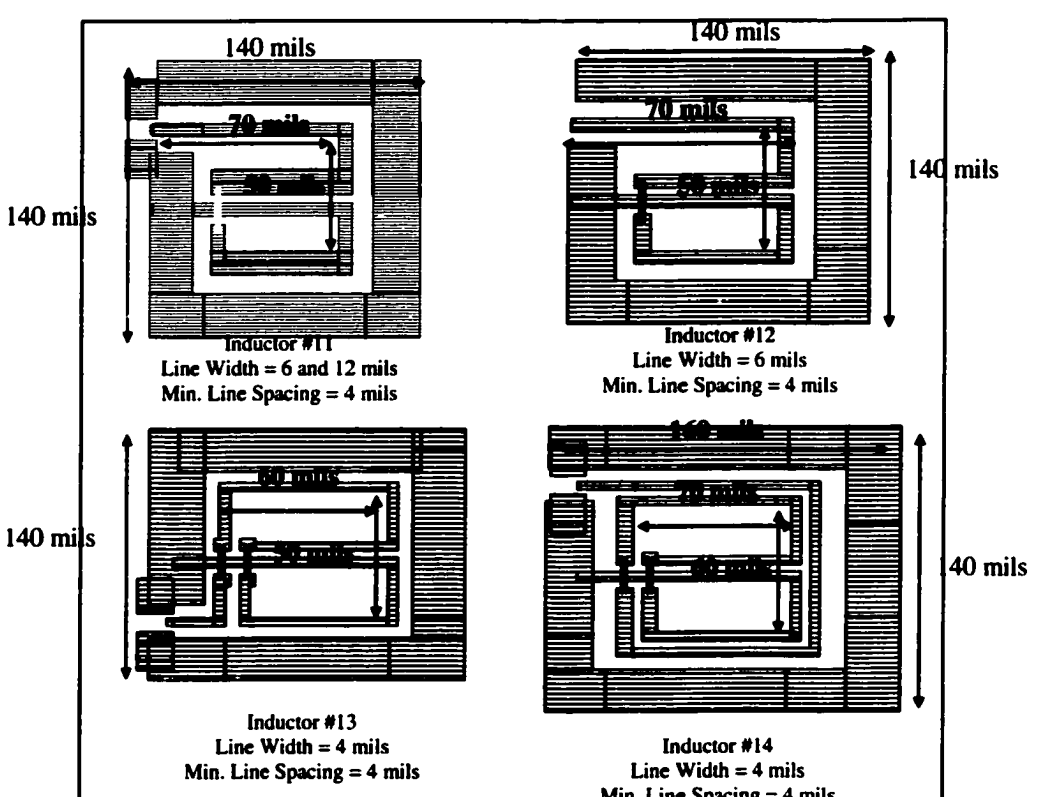

Figure 4.15. CPW or Hollow Ground Inductors

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Table 4.3 shows CPW inductor results measured using the same procedure outlined for the spiral and loop inductors. The achievable Q factors in CPW topology are significantly higher than either of the microstrip topologies. For example, inductor #11 implemented on a 2D area of 9mm^2 measured a maximum Q of 180 at 2.2 GHz with an effective inductance of 4.8nH, which is far more than what is achievable for similar spiral and loop inductors such as #4 and #10 with similar inductances.

Table 4.3. Measured data for CPW Loop Inductors shown in Figure 4.15

Inductor	Max Q (at Freq [GHz])	Effective Inductance (nH)	Area mm^2	SRF GHz
Inductor 11	Q=180 at 2.2	L = 4.8	9	5.5
Inductor 12	Q=140 at 1.9	L = 5.8	9	5.2
Inductor 13	Q=120 at 1.8	L = 8.8	9.5	5
Inductor 14	Q=70 at 1.8	L = 14	9.5	5

As an example, Figure 4.16 and Figure 4.17 show the measured effective inductance and Q as a function of frequency for inductors #11, #12 and #13. The measurements were done using the methods discussed in section 4.4.

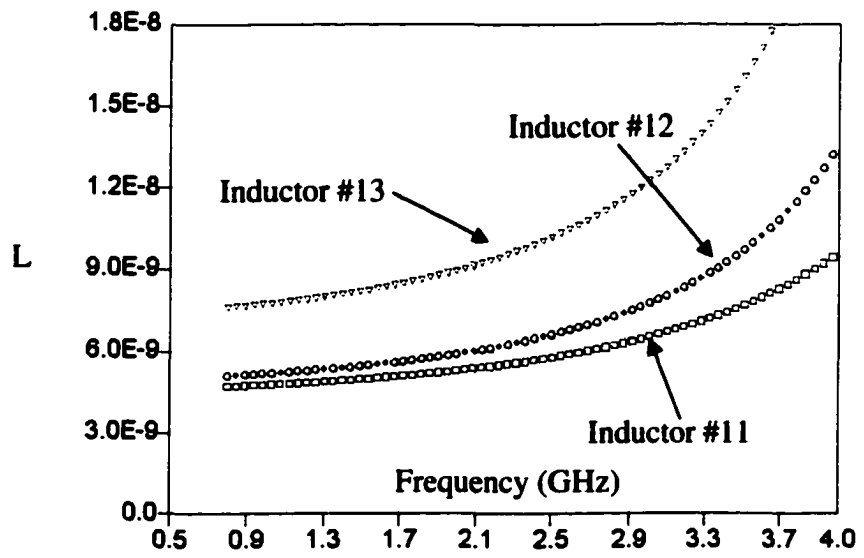

Figure 4.16. Measured inductance vs. Frequency (GHz) for inductors 11, 12 and 13 of 4.15.

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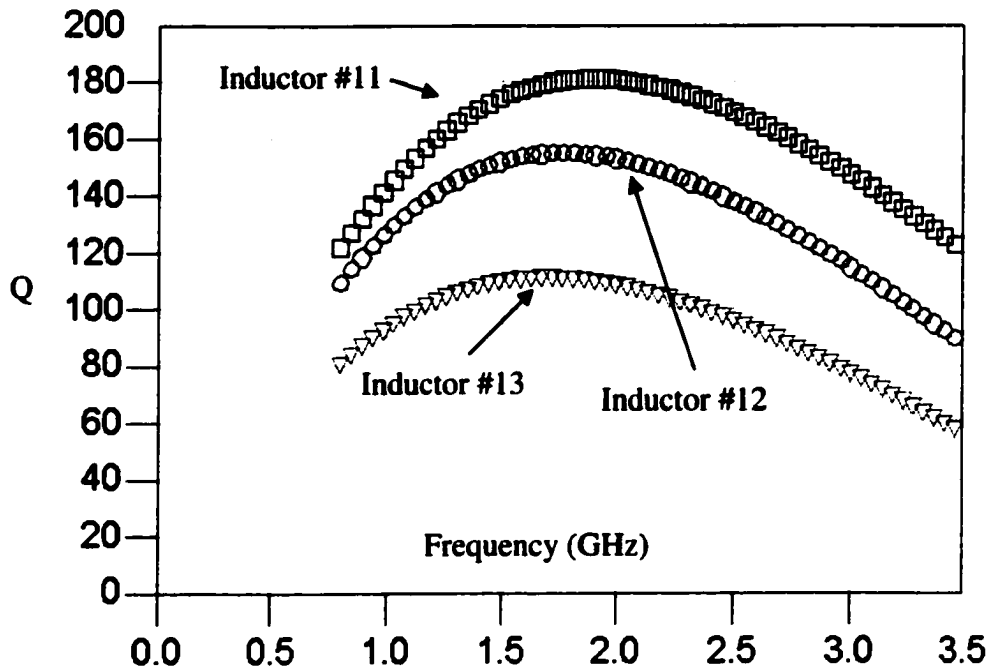

Figure 4.17. Measured Q vs. Frequency (GHz) for inductors #11, #12 and #13 of Fig 4.15.

4.8 Comparisons between different topologies and comparison with other technologies

Inductors with maximum quality factors in the range of 60-180 were obtained at frequencies in the 1-5 GHz band for inductances in the range of 1nH to 20nH. This is the first demonstration of high Q inductors in organic substrates. Aggressive feature sizes of 3 mil lines with 3 mil spacings and 2 mil microvias available in the organic process help keep the size of all microstrip inductors small. The microstrip loop and spiral inductors with sizes less than 4.5mm^2 and a volume less than 3mm^3 are ideally suited for integration in compact microwave circuits. The CPW inductors, though larger in planar size, offer the advantage of higher Q factors and access to a ground reference on the same layer (which makes it easier to add shunt elements without the need for additional through holes). In a CPW topology, the ground to signal spacing can be as large as required, which is another added advantage compared to the microstrip inductor. In conclusion, all topologies meet the requirements for

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high Q and reasonably high SRF for use in filters, low-noise amplifiers and low-phase noise oscillator applications in the GSM900, GSM1800 and Bluetooth frequency bands.

Based on the results and arguments in the previous sections, various comparisons between the different topologies for inductors have been summarized in Table 4.4.

Table 4.4. Comparison Between Various Inductor Topologies.

	WIDE-STRIP NARROW-SPACING SPIRAL TOPOLOGY	NARROW-WIDTH LOOPS TOPOLOGY	CPW/HOLLOW-GROUND TOPOLOGY
Power handling capability	*Medium Q*	*Medium Q*	*High Q*
Adding Elements in Series	*Easy*	*Easy*	*Easy*
Adding Shunt Elements	*Hard*	*Hard*	*Easy*
Topology	*3D*	*3D*	*2D - planar*
Ground spacing	*Limited to core thickness*	*Limited to core thickness*	*Arbitrary*
Ease of Modeling	*Accuracy higher with full-wave solvers. Segmentation technique well suited for three or lesser turn spirals.*	*Very accurate and fast results using segmentation*	*Higher order modes reasonably captured using full-wave solvers or segmentation*
Planar Area and Volume	*Small*	*Small*	*Large*

4.8.1 Comparison between Laminate Technology and MCM-D and LTCC technology for inductor design

The thickness of the core ~ 28 mils, an extremely important requirement for the optimized performance of all microstrip devices. Ensuring a large separation of the ground and signal lines in both microstrip and CPW topology helps increase the inductance, reduce the conductor attenuation and reduce the parasitic capacitance. The

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dimensions and performance of all microstrip inductors are comparable to inductors fabricated using LTCC processes and MCM-D processes and are well suited for integration in a variety of applications. However, in both LTCC and MCM-D processes the thick cores needed for microstrip inductors can only be fabricated by stacking up several layers, thereby increasing the process steps. The use of CPW topologies in LTCC and MCM-D is not feasible due to the constraint on the maximum size of substrates for both LTCC and MCM-D (which is 6"x 6" compared to 18" x 12" sizes for laminate technology).

All designs have been optimized and are well suited for the organic process which helps lower the resistive loss for a given inductance per unit area, the dominant loss in the inductors. The same designs were implemented on lower loss substrates such as A-PPE™ and Zyvex™, but showed negligible change in the maximum Q of the devices, showing the independence of the electrical performance from the loss in the dielectric material. The difference in using lower loss materials is that the Q does not drop as significantly as with a lossier material where dielectric loss ultimately becomes larger than the conductor loss at higher frequencies.

Finally, one build up layer, with microvias, provides the necessary means for under-routing and connectivity between devices. These results advocate the use of low-temperature organic processes as an attractive alternative to LTCC and MCM-D technologies for integral passive applications.

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4.9 Equivalent circuits for embedded inductors

The predictive modeling of inductors with the ability to identify the relevant parasitics and their effects was presented in Chapter 3. The optimization, design and comparison of inductors have been presented in the earlier sections of this chapter. However, a physical lumped circuit model, which captures the frequency response of a device, is important to estimate the effect of non-idealities such as parasitic capacitance and resistance on the behavior of the overall system or sub-systems such as amplifiers and filters. which use that particular device. Lumped model equivalents for a 2-port and 1-port inductor fabricated using the organic process are shown in Figure 4.18 and Figure 4.19, respectively. The series inductance, Ls, and the series resistance, Rs, represent the inductance and resistance of the inductor and under-routings respectively. The overlap between the inductor and the underpass allows direct capacitive coupling between the two terminals of the inductor. This feed-through path is represented by the series capacitance Cs. Components Cp and Rp capture the shunt capacitance and conductance between the inductor and the ground reference, respectively.

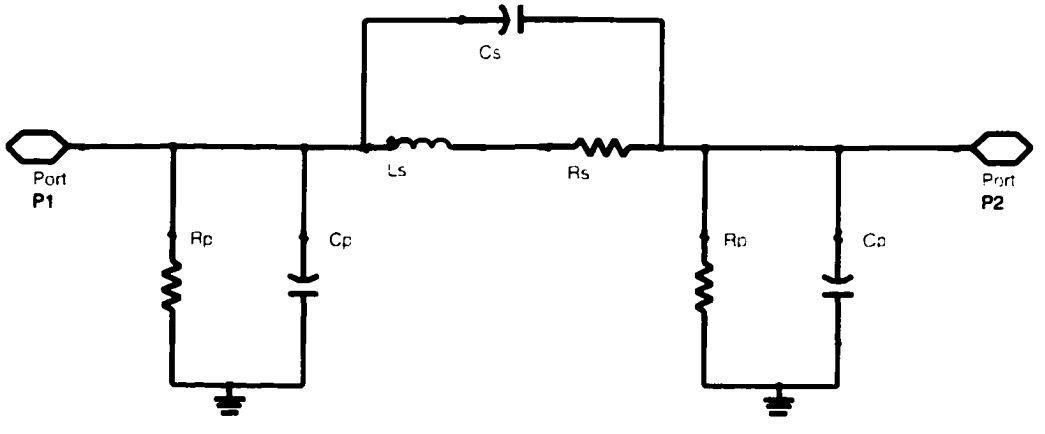

Figure 4.18 Lumped element model for 2-port embedded inductor

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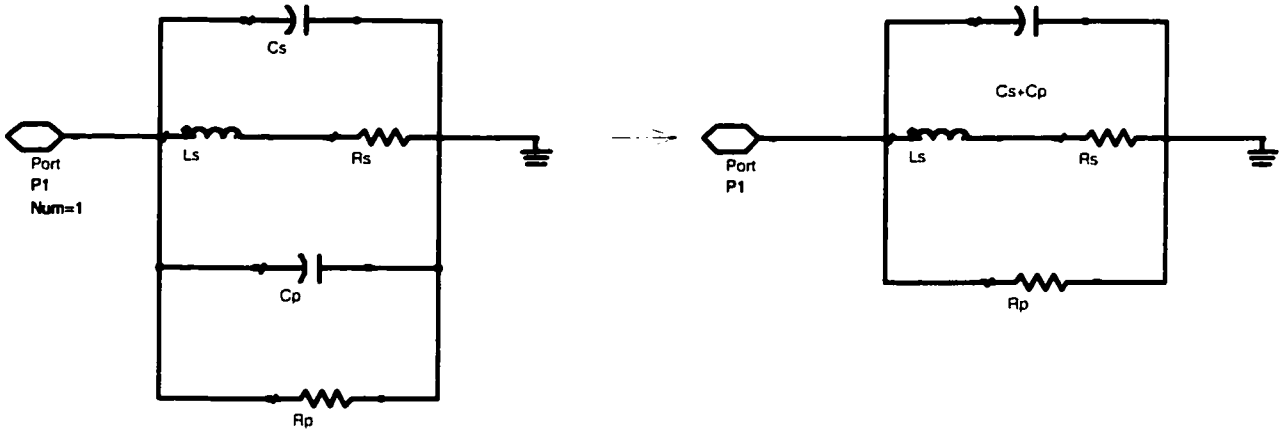

Figure 4.19 Lumped element model for 1-port embedded inductor

The values of Ls, Rs, Rp and Cs+Cp for inductors #1 - #14 (discussed earlier) are shown in Table 4.5. The values were obtained after optimizing each element to match the measured inductance, SRF and Q for the 1-port inductors.

Table 4.5 Summary of lumped model values for inductors #1 - #14

Type	Number	Ls(nH)	Rs(ohms)	Cp+Cs(pF)	Rp(kohms)
Microstrip Spiral Inductors (Figure 4.9)	#1	9.5	0.7	0.2	19
	#2	8.8	0.34	0.22	18
	#3	6.2	0.37	0.09	24
	#4	4.5	0.23	0.18	18
	#5	1.6	0.07	0.19	8.6
Microstrip Loop Inductors (Figure 4.12)	#6	10	0.5	0.2	19
	#7	14	0.5	0.17	18.8
	#8	15	0.7	0.18	19
	#9	7.3	0.65	0.04	28
	#10	7.4	0.45	0.04	23
CPW Loop Inductors (Figure 4.13)	#11	4.1	0.15	0.2	27
	#12	5	0.2	0.2	27
	#13	7.4	0.4	0.15	27
	#14	13	0.9	0.06	23

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As an example to show the validity of these models, Figure 4.20 shows the measured and modeled inductance for 1-port microstrip spiral inductors #2, #4 and #5 from Figure 4.8. Their corresponding measured and modeled Q-factors have been shown in Figure 4.21. As is evident the correlation between the measured and modeled values is very good over the frequency bandwidth of interest.

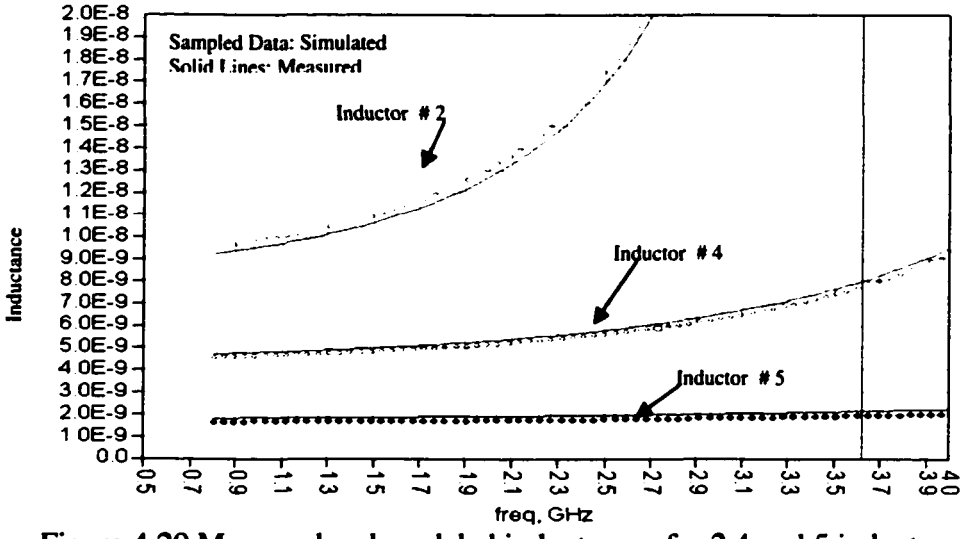

Figure 4.20 Measured and modeled inductances for 2,4 and 5 inductors

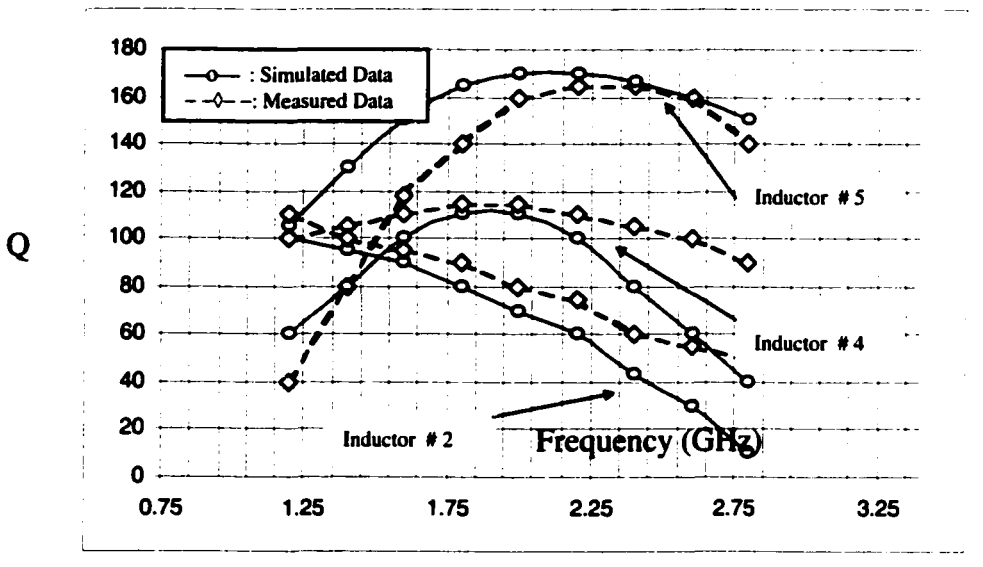

Figure 4.21 Measured and modeled Q-factors for 2,4 and 5 inductors

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4.10 Design and Optimization of Capacitors

Figure 4.22 shows various parallel capacitors implemented using the testbed in Figure 4.3. In the testbed, the 2nd metal layer serves as the feed / signal layer and the 1st metal layer acts as the ground plane. Three different dielectric materials were evaluated, namely, Vialux™, A-PPE™ amd Zyvex™. The testbeds provides for 20 um of Vialux™ as the dielectric medium between the plates of the capacitor for the first testbed, 30um of A-PPE™ for the second testbed and 50um of Zyvex™ for the third testbed. The upper limit for the Q factor for any size capacitor implemented on this substrate at a particular frequency (f), ignoring conductor loss, can be approximated using $1/\tan\delta$, where $\tan\delta$ is the loss tangent of the material at a particular frequency. Though this represents the upper limit, the Q factor is reduced by the conductor loss. Since from Chapter 2 the extracted dielectric loss tangent for Dupont Vialux™ is 0.015 at 1 GHz and 2 GHz, the upper limit for the Q of the capacitors is 66 at 1 GHz and 2 GHz, respectively. Similarly, since the loss tangent for the A-PPE™ is 0.007 at 1 GHz and 0.0095 at 2 GHz, this sets the upper limit for the Q of the capacitors for A-PPE™ at 140 at 1 GHz and 105 at 2 GHz. For Zyvex™, the upper limit for the Q of the capacitors is ~1/0.0025=400. Conductor thicknesses on the order of 20 um help reduce conductor losses and make it possible to reach these upper limits for Q factors. The above stated arguments are supported by the results shown in Table 4.6. The measurements for the capacitors was done using the same setup that was used to measure the inductors and is described in detail in section 4.4.

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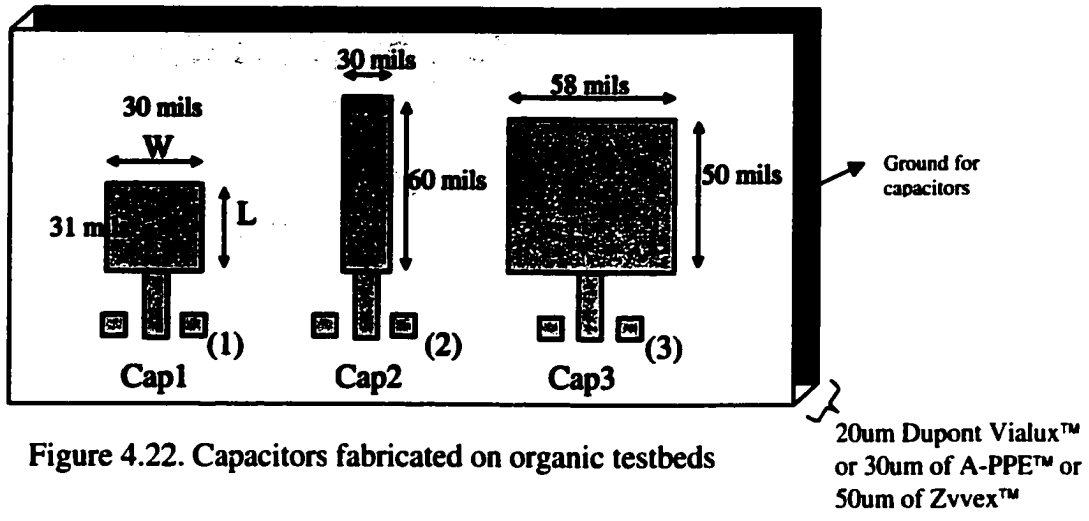

Figure 4.22. Capacitors fabricated on organic testbeds

Table 4.6. Measured Data for capacitors shown in Figure 4.22

Capacitor	Capacitance (pF) in the range of 1 GHz to 2 GHz			Q at 1 GHz			Q at 2 GHz			SRF (GHz)	
	Vialux	PPE	Zyvex	Vialux	PPE	Zyvex	Vialux	PPE	Zyvex	Vialux/ PPE	Zyvex
Cap 1	0.92	0.71	0.60	49	135	380	33	90	350	>9	>6
Cap 2	1.78	1.40	1.14	42	122	330	30	88	300	>9	>6
Cap 3	2.72	1.98	1.75	36	110	300	28	84	260	>8	>5

The performance for Cap2 and Cap3 fabricated using A-PPE™ compares well with the performance of capacitors with similar capacitances implemented in 20 layer ceramic processes and could be potentially used to replace the multi-layer ceramic filters. A Q of 90 at 1 GHz and 60 at 2 GHz has been reported for a 1.4 pF using LTCC capacitor in [5] compared to 100 at 1 GHz and 80 at 2 GHz for the capacitor fabricated using A-PPE™. Although the loss in the PPE material at 2 GHz is higher than that in ceramic material (tan δ=0.004 at 2 GHz) used in [5], the increased copper metallization of 15-20um and lower dielectric thicknesses in the organic process helps lower the resistive losses and inductive effects, respectively. In [5], 5um thick aluminum metallization and 4mil thick dielectrics have been used. The Q factors for capacitors, however, fabricated using Zyvex™ exceed the unloaded Q's attained using either MCM-D or LTCC processes and,

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as mentioned in Chapter 1 and discussed in Chapter 5, are sufficient to achieve the performances of the bulky ceramic cavity filters.

It can also be seen that the materials with lower thicknesses such as Vialux™ and A-PPE™ compared to Zyvex™ have higher SRFs due to the lower parasitic inductance. However, when using thinner dielectrics such as Vialux™ the tolerances associated with capacitances due to the dielectric thickness variation is greater than 10% when the thickness of the buried metal layers (~9um) is comparable to the thickness of the dielectric (~20um). The tolerance is ~ 2% when using materials such as Zyvex™ which are twice as thick for the same metal thickness. For devices such as filters and matching circuits for amplifiers, where tolerances less than 2% are desired, the metal thickness of the buried metal layers should be uniform and 1/3rd the thickness of the dielectric. As discussed in Chapter 2, Advanced Design Suite (ADS) from Agilent or the techniques in Chapter 3 can be used to physically model capacitors such as the ones in Figure 4.18 to identify the relevant parasitics and their effects.

The next section discusses the construction of 2-port and 1-port equivalent lumped circuit models which can be used to capture the effective capacitance, SRF and unloaded Q of an embedded capacitor to estimate their effect in sub-systems such as filters and amplifiers.

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4.11 Equivalent circuit for embedded capacitors

The 2-port and 1-port lumped element models for embedded capacitors are shown in Figure 4.23a and Figure 4.23b, respectively. They include a capacitor C in series with a resistance Rs to model the conductor loss and a resistor Rp in parallel with C to model the dielectric loss. The capacitor C_1 and C_2 and the inductor L in the schematic represent the shunt capacitances to ground and the series inductance, respectively. The lumped model values, C, Rs, Rp, L, and C_1, for capacitors 1 and 2 fabricated (shown in Figure 4.22) using Zyvex™, A-PPE™ and Vialux™ are shown in Table 4.7. The values for these elements were optimized to match the measured effective capacitance and unloaded Qs for the capacitors. Figures 4.24a and 4.24b show model to hardware correlation for capacitors fabricated using Zyvex.

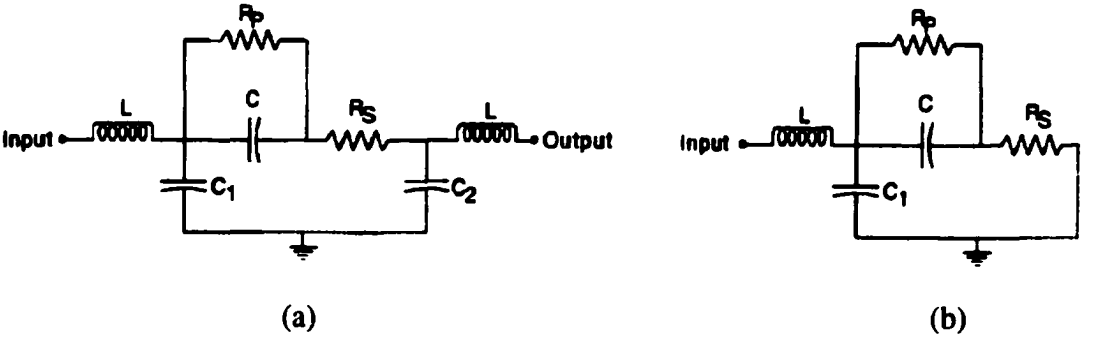

Figure 4.23. a) Equivalent circuit model for 2-port capacitors
b) Equivalent circuit model for 1-port capacitor

Table 4.7 Summary of lumped model values capacitors 1 and 2

Material	Capacitor	C(pF)	C_1(pF)	L(nH)	Rs(ohms)	Rp(kohms)
Zyvex™	1	0.45	0.25pF	0.1	0.5	120
	2	0.72	0.35	0.22	0.42	100
	3	1.3	0.3	0.26	0.3	100
A-PPE™	1	0.7	0.06	0.15	0.55	70
	2	1.3	0.1	0.22	0.49	65
	3	2.1	0.1	0.26	0.62	65
Vialux™	1	0.9	0.0	0.1	1.9	30
	2	1.6	0.1	0.2	1.7	30
	3	2.4	0.2	0.2	2	30

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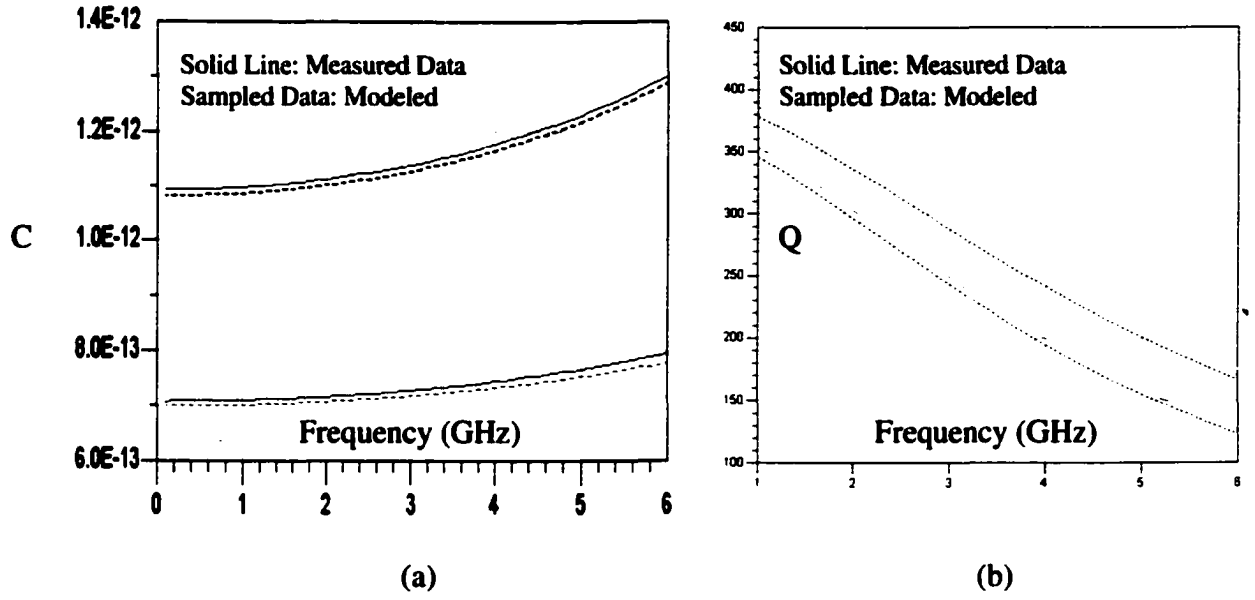

Figure 4.24 a) Effective capacitance for capacitors 1 and 2 fabricated using Zyvex
b) Q-factor for capacitors 1 and 2 fabricated using Zyvex
(Solid lines represent measured data and dotted lines represent modeled data)

4.12 Summary

The inductors shown in this chapter use aggressive features such as 2 mil microvias and 2 mil lines with 2 mil spaces. This ensures small device sizes ideally suited for integration with other devices. The results also show that the performance of inductors is weakly dependent on the loss of the materials and strongly dependent on the conductor type and conductor thicknesses. Using the information from the fabricated inductors, design rules have been developed for the implementation of high-Q inductors for RF communication standards such as GSM (900 MHz and 1800 MHz), Bluetooth (2.4 GHz) and Hyperlan (5.1-5.8 GHz).

Unlike inductors, capacitors require much lower loss dielectric materials as compared to inductors for achieving similar Q-factors. Q's as high as 300, similar to inductors, at

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gigahertz frequencies can only be obtained when using materials such as Zyvex™ with a loss tangent ~0.002.

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CHAPTER V

5. DESIGN AND IMPLEMENTATION OF FILTERS IN ORGANIC SUBSTRATES

Introduction

The previous chapter showed the feasibility of obtaining unloaded Q's for inductors in the range of 50-200 for inductances greater than 1nH and unloaded Q's for capacitors in the range of 50-380 for capacitances greater than 1pF. This chapter discusses the use of these inductors and capacitors for the construction of bandpass filters such as those described in Chapter 1.

Figure 5.1 shows a front-end section in receiver architectures such as heterodyne, homodyne or image-reject receivers.

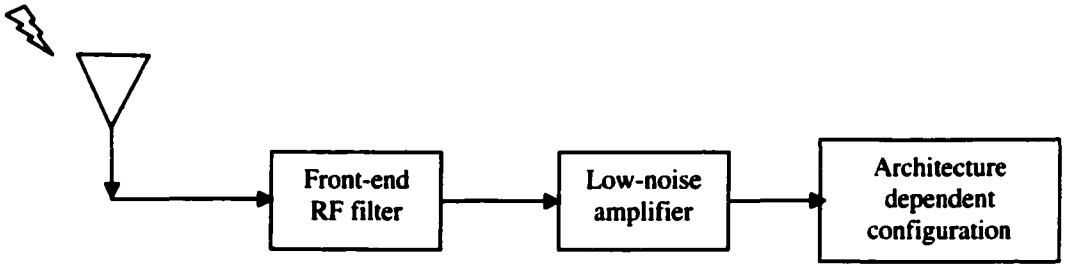

Figure 5.1 Common front-end for wireless receivers

The RF front-end filter helps remove the out-of-band energy and performs rejection of image-band signals. The design of front-end RF filters in all architectures is becoming a major problem since center frequencies are scaling towards the multi-gigahertz range for most RF standards. As the carrier frequency becomes higher, the loaded Q (carrier frequency ÷ 3dB bandwidth) for filters becomes higher, which places higher demand on the unloaded quality factor for components such as inductors, capacitors and resonators that make up the filter device. Coaxial cavity or monoblock type filters have become very popular in commercial applications, especially in portable communication equipment,

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due to their high performance. Low loss is achieved with transmission line sections that are rounded such as coax lines or by avoiding sharp corners. However, there are several disadvantages to these ceramic coaxial cavity or monoblock filters. First, the mold for these filters is expensive and each design usually needs a new mold. Second, when fabricating coaxial type ceramic filters, different coaxial resonators are sintered and coated separately, and then connected to each other by soldering the connecting wires by hand. Further, they must be fastened to some mounting support in a mechanically reliable manner. Therefore, the manufacturing process can be difficult and costly. Moreover, size reduction is achieved by using special high dielectric constant ceramics, resulting in a reduction of the effective wavelength in the medium.

Multilayer planar filters, fabricated using multilayer ceramic (MLC) technology based on LTCC, can have a volume $1/40^{th}$ that of ceramic cavity filters and are being developed for data communication equipments and digital cordless telephones, where unlike cellular applications, narrow bandwidths and large roll-offs are not required [14]. These filters use non-traditional metallization techniques used in ceramic technology to achieve metal thicknesses ~100um to lower higher frequency losses. Shown below in Table 5.1 is a comparison of filters in ceramic technology with a few examples of products currently available. The multi-layer ceramic filters come with the disadvantage of higher costs due to the non-traditional processes used in making the multilayer ceramic filters. These filters, however, do meet the demands for communication standards such as Bluetooth and Personal communication systems (PCS).

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Table 5.1. Comparison of Ceramic Cavity and Multilayer Ceramic Technology

Type	*Center Freq (f_o). (Application)*	*1dB and 3dB Bandwidth (BW)*	*Insertion loss in 1dB band*	*Size*	*Attenuation*
1) 5 layer ceramic filter	1.9 GHz (PCS)	60 MHz and 120 MHz	3.0dB	18mm^3	40dB at f_o-400 MHz
2) 5 layer ceramic filter	2.4 GHz (Bluetooth)	100 MHz and 300 MHz	2.8dB	18mm^3	30 dB at f_o-300 MHz
2) 3 section ceramic cavity filter	2.4 GHz (IEEE 802.11b)	60 MHz and 90 MHz	2.5dB	300mm^3	40dB at f_o±200 MHz

From Table 5.1, the attenuation achieved with the ceramic cavity filter is larger throughout the stopband and its insertion loss is lower compared to the multilayer ceramic filter. Hence, in spite of the disadvantages with the cavity filter discussed earlier with a size that is 40 times larger than the multilayer filter, the cavity filter is still the common choice for higher performance systems such as cellular phones. This chapter discusses the implementation of bandpass filters in organic substrates that meet the performance of ceramic cavity filters but with a significant size advantage. This chapter also discusses the implementation of bandpass filters in organic substrates that meet the performance of MLC filters but with a cost advantage. The next section helps understand the unloaded Qs associated with the resonator elements needed to achieve the desired specifications and explains why even MLC filters have not been able to replace bulky cavity filters.

5.1 Bandpass Filter Circuits

Figure 5.2 shows a typical topology used for bandpass filters implemented using MLC processing or ceramic coaxial cavities. Elements 20a and 20b in Figure 5.2 represent shorted transmission line resonator elements. The reason for choosing this

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particular topology is the higher relative permittivity (20<εr<90) of materials available in ceramic technology. The higher relative permittivity decreases the effective wavelength in the dielectric medium; thereby, the physical length required for the transmission line resonator elements decreases. However, the incompatibility of different ceramic materials during processing causes problems towards integration. Materials used for the construction of these filters may not be integrated with lower permittivity (εr<9) ceramic materials, some of which may be required for high speed applications or in another instance for an embedded inductor requiring high SRF.

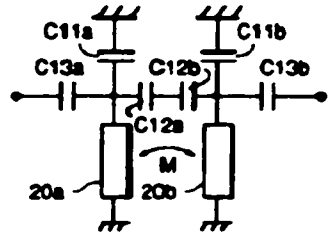

Figure 5.2 Schematic for filter with transmission line resonators

Since organics have an inherently lower dielectric constant (2.2<εr<4.5) they do offer themselves as a better candidate for applications such as high speed transmission and high SRF embedded inductors compared to ceramic substrates. However, for filter applications with all passives embedded in the organic package or board, the topology in Figure 5.2 needs modification because of the larger length of transmission line resonators as a result of lower dielectric constant. The topology used in this dissertation is shown in Figure 5.3. Front-end RF filters with the topology shown in Figure 5.3 can be simulated to provide an estimate of the required unloaded Q of individual components to attain the necessary loaded Q.

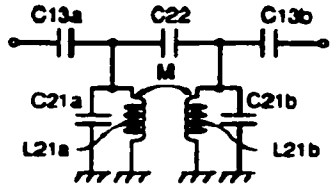

Figure 5.3 Bandpass filter with coupled resonators sections

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The circuit in Figure 5.4a is an example of a coupled-resonator filter, which meets the specifications of the multilayer ceramic filter described as Filter 1 in Table 5.1. The inductors and capacitors have been simulated as non-ideal components in Agilent's Advanced Design Suite (ADS) [15]. Figure 5.4b shows the simulated S_{21} (insertion loss) and S_{11} (return loss) for the filter in Figure 5.4a. A maximum unloaded Q-factor of ~110 at 1.9 GHz is required for inductors and capacitors connected in parallel which form the resonator tanks. The unloaded Qs for the center capacitance and the matching capacitors need to be approximately 60 at 1.9 GHz.

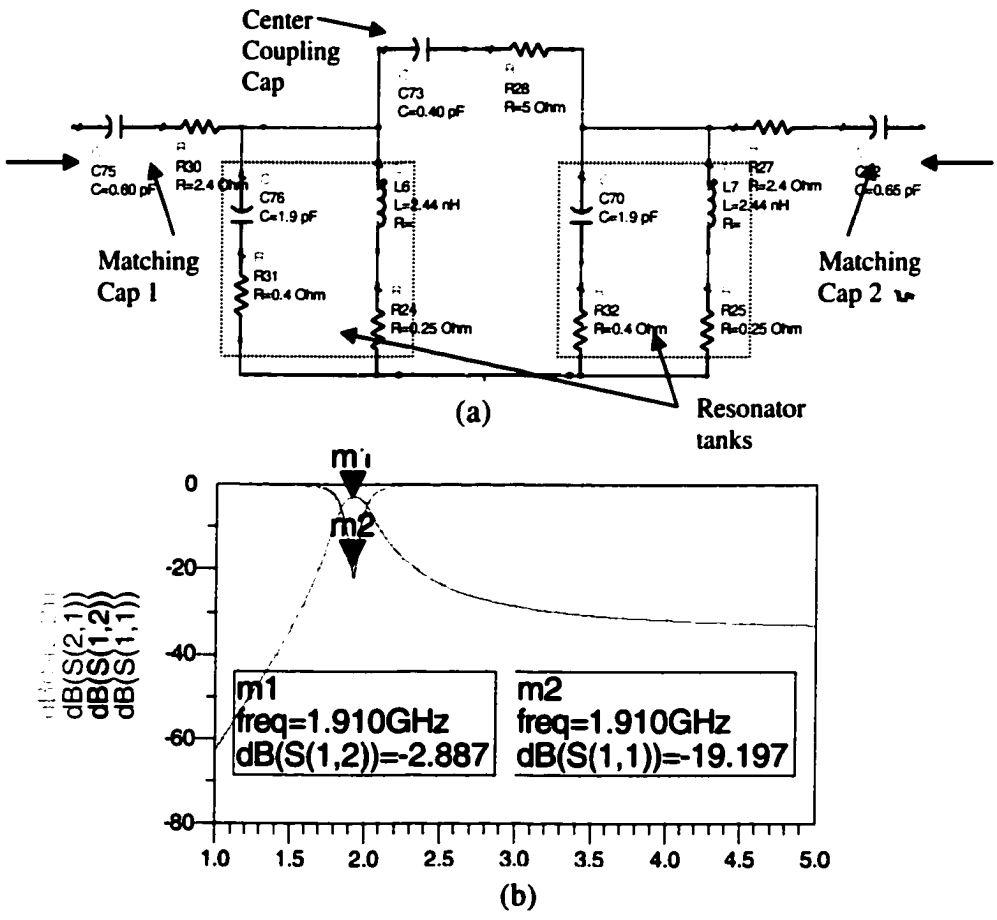

Figure 5.4 a) Schematic of a coupled resonator for PCS applications
b) Simulated return loss and insertion loss for filter using ADS

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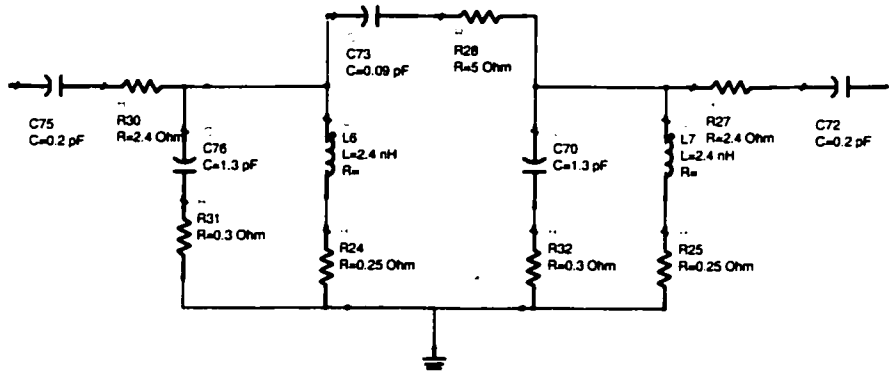
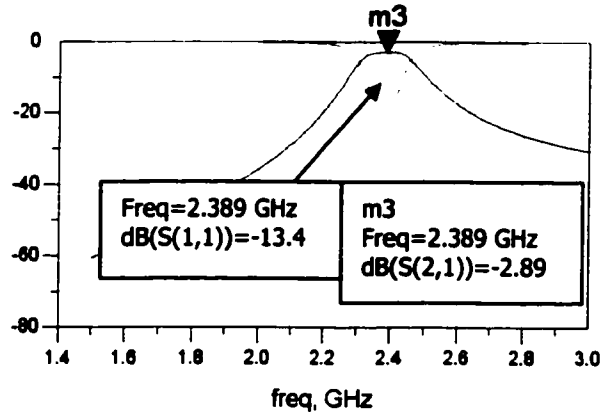
The circuit in Figure 5.5a is an example of a coupled-resonator filter, which meets the specifications of the multilayer ceramic filter described as Filter 2 in Table 5.1. The inductors and capacitors have again been simulated as non-ideal components in Agilent's Advanced Design Suite (ADS) [15]. Figure 5.5b shows the simulated S_{21} (insertion loss) and S_{11} (return loss) for the filter in Figure 5.4a. A maximum unloaded Q-factor of 130 at 2.4 GHz is required for inductors and capacitors connected in parallel, which form the resonator tanks. The unloaded Qs for the center capacitance and the matching capacitors need to be approximately 100 at 2.4 GHz.



(a)



(b)

Figure 5.5 a) Schematic of a coupled resonator for Bluetooth applications
b) Simulated return loss and insertion loss for filter using ADS

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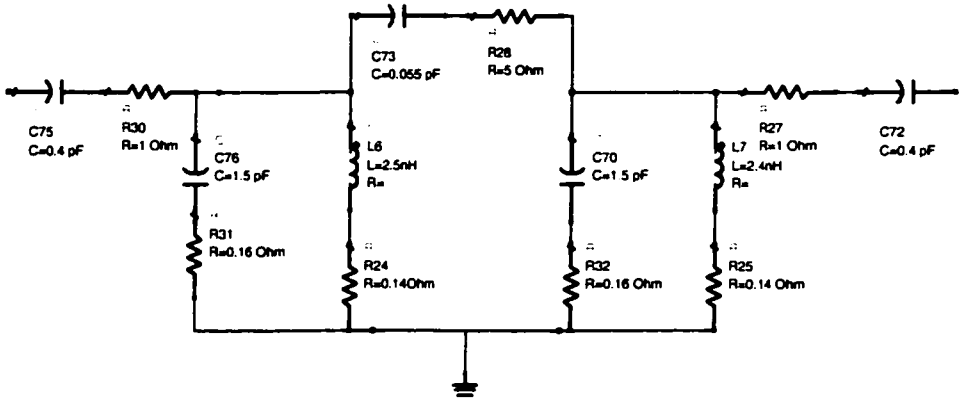
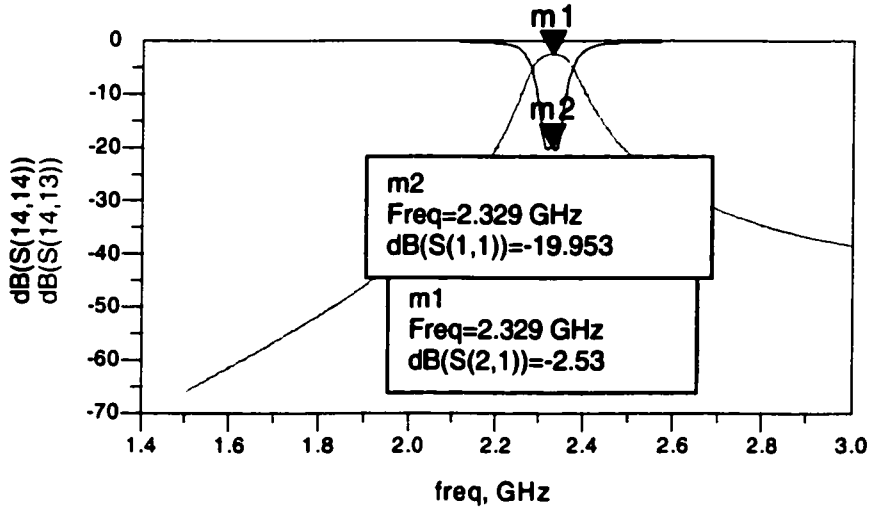
Similar to the previous two circuits, Figure 5.6a is an example of a coupled-resonator filter, which meets the specifications of the ceramic cavity filter described as Filter 3 in Table 5.1. Figure 5.6b shows the simulated S_{21} (insertion loss) and S_{11} (return loss) for the filter in Figure 5.6a. A maximum unloaded Q-factor of 210 at 2.4 GHz is required for inductors and capacitors connected in parallel, which form the resonator tanks. The unloaded Qs for the center capacitance and the matching capacitors need to be approximately 200 at 2.4 GHz



(a)



(b)

Figure 5.6 a) Schematic of a coupled resonator for IEEE 802.11 applications
b) Simulated return loss and insertion loss for filter using ADS

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As seen, a maximum unloaded Q-factor of ~130 is required for inductors greater than 1nH, and a maximum unloaded Q-factor of ~130 is needed for capacitors greater than 1pF to achieve the performances of the MLC filters. As mentioned in [5,6] and also in section 1.2 these are also approximately the highest unloaded Q reported for capacitors and inductors in ceramic processes. For any filter or device, which requires higher performance, the current multilayer ceramic process would prove to be inadequate and the use of larger ceramic cavity resonators would therefore be necessary.

In this chapter, filters with integral passive devices in organic substrates have been implemented for standards such as Bluetooth, IEEE 802.11b and PCS (Table 5.1) to show a feasible replacement for MLC and cavity filters. Unlike inductors, the unloaded Q for capacitors is heavily dependent on the dielectric loss, as shown in Chapter 4. The unloaded Qs for capacitors needed to achieve the specifications of different kind of filters, namely Filters 1, 2 and 3, constrain the dielectric medium for the implementation of these filters. For example, for Filters 2 and 3, Zyvex™, which can provide Qs as high as 200 at 2 GHz for capacitors, is appropriate. For Filter 1, A-PPE™, which can provide Qs as high as 110 at 2 GHz, is a fitting choice. Another approach that has been taken up in the past to explore the possibilities of "low-cost realization of ISM band filters" in MCM-L technology [16], which uses low-cost epoxy substrates, is the use of discrete high Q capacitors for applications where the loss tangent of dielectric makes it unusable.

This chapter is organized as follows: section 5.2 discusses the realization of filters for the PCS communication standard using the lowest cost epoxy-based dielectric along with discrete capacitors. Sections 5.3 and 5.4 discuss the realization of completely integrated

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filters in Zyvex™ for the Bluetooth and IEEE 802.11b standards. Finally, section 5.5 summarizes the differences between the filter implementations in different substrates.

5.2 Realization of Bandpass Filters for PCS applications in Organic Substrates

A ceramic filter suggested for the PCS communication standard, shown as Filter 1 in Table 5.1 has the following characteristics: center frequency (f_o) equal to 1.9 GHz, and 3dB bandwidth (BW) equal to 120 MHz, and a loaded Q of 17.5. The insertion loss at f_o is 3dB with 40dB rejection at 1.5 GHz. The schematic in Figure 5.4a emulates the performance of this filter. While the unloaded Q for inductors is independent of the dielectric as shown in Chapter 4, the Q for the capacitors is heavily dependent on the substrate used. As seen in the previous chapter the ideal choice of material for this application would be A-PPE™ which can provide unloaded Q's as high as 110 for capacitors ~1pF at 2 GHz, which is the requirement for this filter. However, due to the lack of availability of processing equipment for A-PPE™ at the time of the conception of the device, Vialux™ was used for fabricating the device along with the use of discrete capacitors. Vialux™, which can provide a Q of ~40 at 2 GHz, would barely suffice for integrating the center and matching capacitors which need a Q of 60, whereas the other capacitors that need a Q of 110 at 1.9 GHz can be implemented using discrete capacitors.

In [16], the use of discrete high Q capacitors is made for applications where the loss tangent of dielectric makes the dielectric unusable. This approach is still lower cost than using multilayer ceramic filters [16]. However, the 3dB bandwidths realized in [16] were on the order of 500 MHz, which does not meet the requirements for PCS applications. Furthermore the authors in [16] have made use of very aggressive design rules, which

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include line widths down to 10um. Additionally, the model to hardware correlation for the filters showed more than 10% deviation in the passband. In [17] the authors use coupled-inductive resonator filters, and eliminate the need for discrete capacitors. However, due to the long length of the inductor coils the loss in the filter was greater than 4dB for 3dB bandwidths greater than 400 MHz at 2.45 GHz.

The rest of this section discusses a novel methodology and topology for realizing filters with Vialux™ dielectric for applications such as PCS. Using a combination of discrete capacitors, embedded capacitors and embedded inductors, the filter circuit has been implemented with design rules described in Appendix B. The substrate was processed using the methods discussed in Appendix A.

AVX Corp's 0603 size discrete capacitors were chosen for their small size and associated unloaded Q factors to implement the larger capacitors with higher Q requirements. The rest of the devices including the inductors, coupling and matching capacitors and interconnections were implemented directly on the Vialux™ substrate. The layout for the filter, which represents element values shown in Figure 5.4a, is shown in Figure 5.7a and the cross-section of the testbed is shown in Figure 5.7b. The buried metal layer was limited to 5um to achieve uniformity in dielectric thickness. The drawing in Figure 5.7c shows the layout of a test structure that was used to measure the discrete capacitors. Since the performance of discrete components such as chip capacitors changes depending upon the pad dimensions used and type of topology (CPW or microstrip) from substrate-to-substrate, the documented data for discrete components from manufacturers such as AVX cannot be relied upon and needs re-characterization. One way to account for these effects is to model the pad structure with the appropriate substrate using a tool

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such as SONNET and then build an equivalent circuit for the pads, which can be superimposed on the model for the discrete capacitor to estimate the net capacitance. This is true for any other discrete component such as inductors or resistors. Another approach, which is faster and was used in this work, is to measure different discrete capacitors with the pads intended for their use and choose the one that provides the desired capacitance. The topology used for the implementation of this filter was a CPW topology, which can be clearly seen in Figure 5.7a. The discrete capacitors were measured separately before incorporating them in the filter device. The pads used in the filter and used for characterizing the capacitors are shown in Figure 5.7c. A 1pF capacitor listed under AVX's Accu-F/Accu-P 0603 series provided an effective capacitance of 1.7pF with a series resistance of 0.36 ohms in the configuration shown in Figure 5.7c.

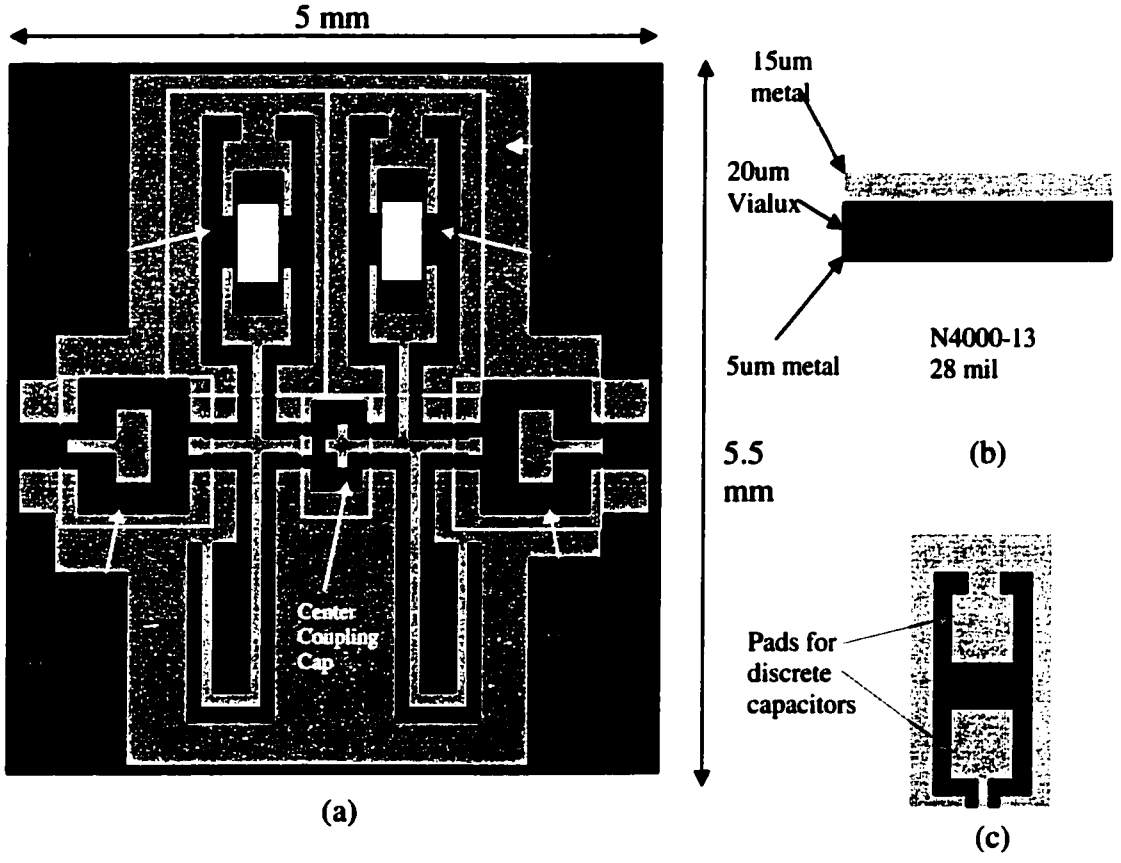

Figure 5.7 a) Layout for PCS application with discrete capacitors
b) Cross-section of the testbed
c) Layout for test structure to measure the discrete capacitors

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The equivalent circuit for the filter, which is in essence a combination of the equivalent circuits for the individual components, is shown in Figure 5.8. The matching capacitors were designed in such a way that the shunt capacitance was 0.2pF. As seen, the shunt capacitance of the matching capacitors together with the 1.7pF effective capacitance of the discrete capacitor provide the desired 1.9pF for the PCS filter. The inductors were designed and optimized to provide an equivalent inductance of 2.44nH and a series resistance less than 0.25ohms. As seen in Figure 5.7a, the spacing between the inductors is quite large. Based on simulations in SONNET, the spacing between the inductors in Figure 5.7a was the minimum spacing required, which provided the needed isolation between the inductors.

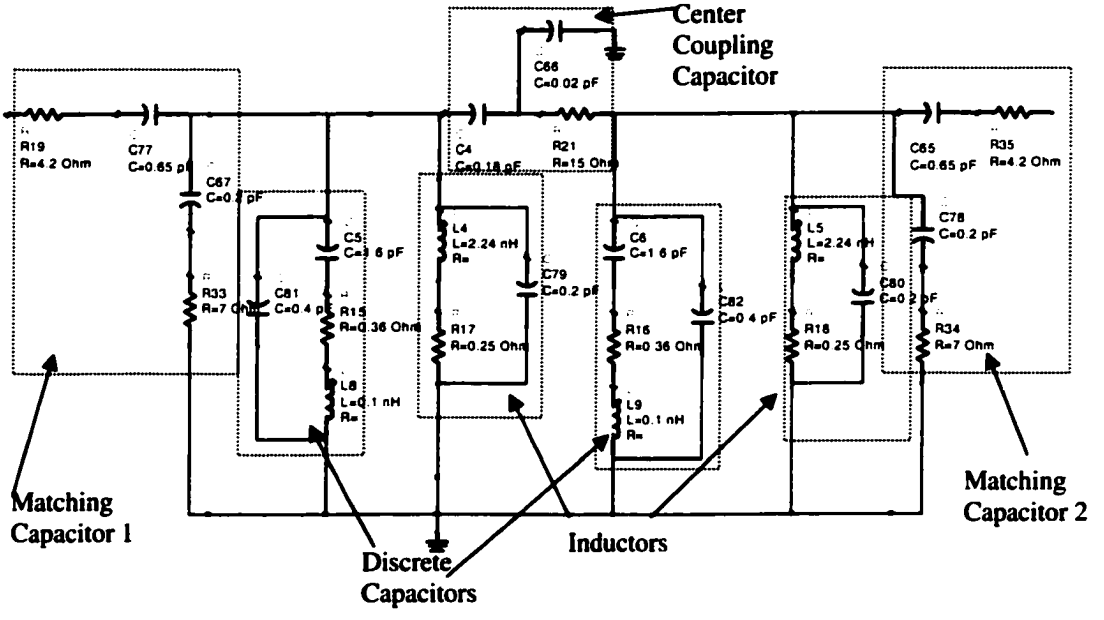

Figure 5.8 Equivalent circuit for PCS filters implemented using Vialux and two discrete capacitors

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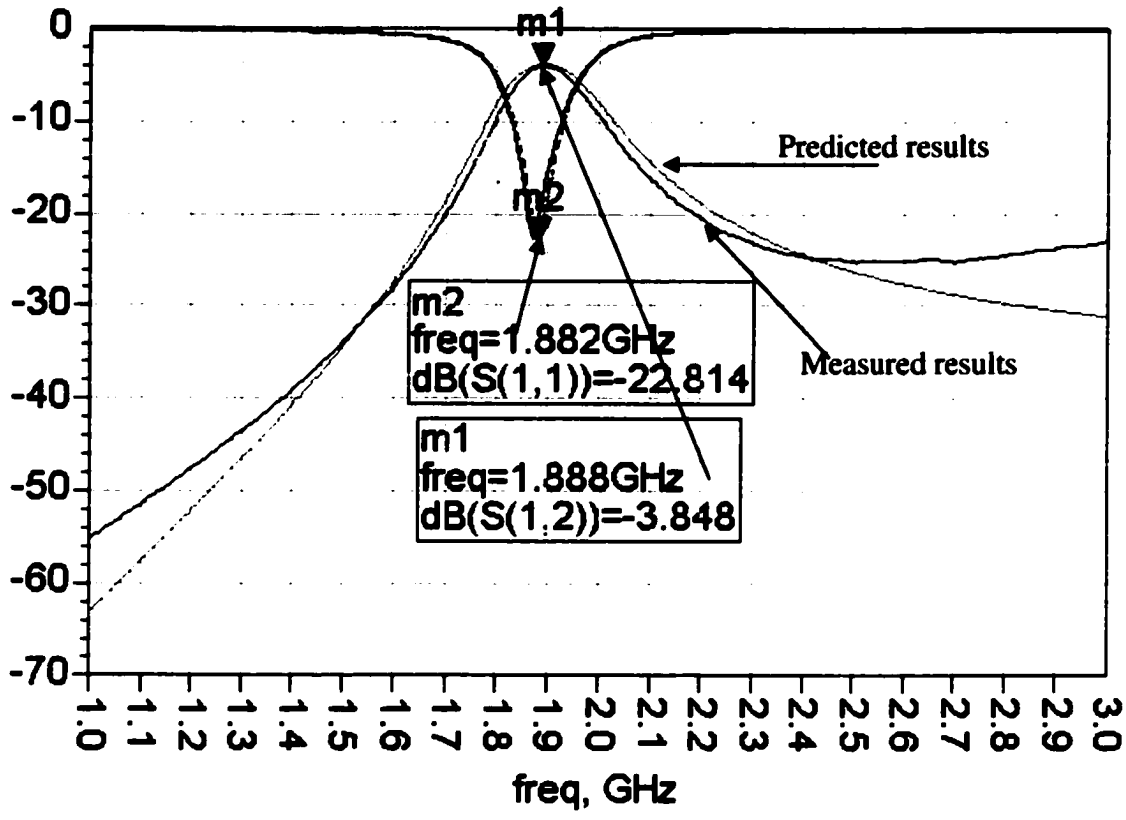

Figure 5.9. Model to hardware correlation for PCS filter

Figure 5.9 shows model to hardware correlation for the filter with all embedded components, except the two discrete capacitors. There is very good agreement between measured and predicted results. The measured filter has a center frequency = 1.9 GHz, a 1dB passband of 60 MHz, and a 3dB bandwidth of 120 MHz. The attenuation at 1.5 GHz is ~ 40dB, as desired. The insertion loss is ~ 3.8dB at 1.9 GHz, which is greater than the specification. This is due to the use of center and matching capacitors with Qs of 40 in Vialux rather than the required Q of 60 needed to achieve a lesser loss of 3dB. This insertion loss can be lowered by using A-PPE™ or Zyvex™ dielectric materials.

Although the filter meets the attenuation needed for PCS applications at 1.5 GHz as specified in Table 5.1, there is a discrepancy in the measured and predicted results beyond 2.5 GHz for S_{21}. This discrepancy is due to the coupling between the two discrete capacitors. The simulations in SONNET were done for individual components and for

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optimizing the spacing between the inductors. The discrete capacitors were measured as individual components without any coupling between them. The tight spacing between the capacitors could have resulted in unwanted coupling effects which show up at frequencies greater than 2.5 GHz. Figure 5.10 shows a comparison between modeled and measurement data for the filter, after including a mutual coupling term between the two discrete capacitors. As can be seen from the figure, the results show better agreement with measurements.

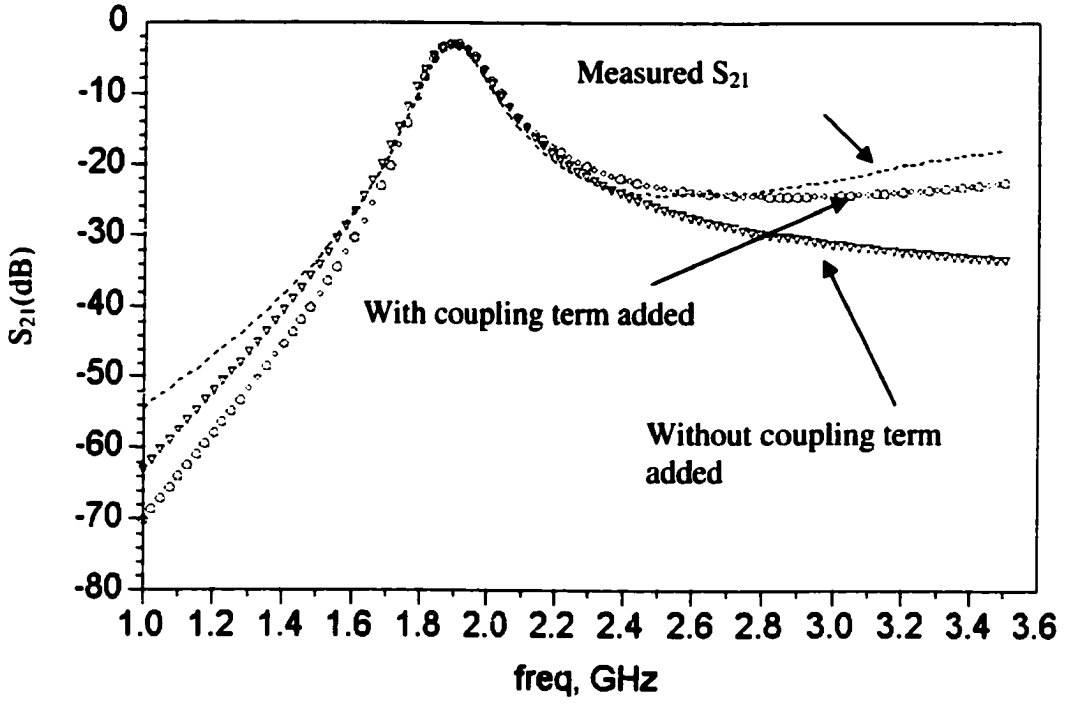

Figure 5.10 The comparison of measured S_{21} for PCS filter with modeled results with and without coupling term included between discrete capacitors

In summary, the filter shown here is a new CPW topology that uses only two metallization levels and an epoxy based substrate along with discrete capacitors to achieve the performance of non-standardized multilayer (>5) ceramic processes. Additionally, the MLC filters cannot be integrated with other components in the same layers of the ceramic package due to the following reasons: firstly, because of the use of a

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filter-specific dielectric which is incompatible with other dielectrics; secondly, because of the specificity of certain attributes such as 100um thick aluminium conductor lines required to lower the attenuation present due to standard 5um lines used in ceramic processes. The design discussed in this section was fabricated using standard design rules pertinent to multilayer laminate boards and can be directly implemented on the board without the need for a separate surface mount device. Furthermore, the model to hardware correlation shows validity of the design technique used. Figure 5.11 shows an example of the fabricated PCS filter in Vialux™.

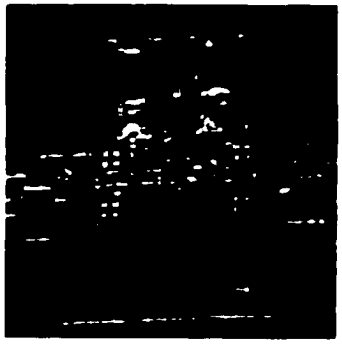

Figure 5.11 Fabricated PCS filter in Vialux™

On another note, applications such as PCS, although narrowband, are lower frequency standards (1.9 GHz) compared to the higher frequency Bluetooth and IEEE 802.11b standards which are centered at 2.4 GHz. The higher frequency (2.4 GHz) applications raises the requirements on the unloaded Q of the components compared to lower frequency PCS standard, which operates at 1.9 GHz for devices such as bandpass filters. The next section discusses the realization of a front-end filter using all embedded passives fabricated using Zyvex™. In this scenario, the entire device simulation was performed using SONNET to better understand all coupling effects and methods for removing the coupling effects if needed.

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5.3 Realization of bandpass filters for Bluetooth applications

A ceramic filter suggested for the Bluetooth communication standard, shown as Filter 2 in Table 5.1, has the following characteristics: center frequency (f_o) equal to 2.4 GHz, a 1dB bandwidth (BW) equal to 100 MHz with a minimum insertion loss of 2.8dB, and 30dB rejection at 2.1 GHz. The schematic in Figure 5.5a emulates the performance of this filter. While the unloaded Q for inductors is independent of the dielectric (shown in Chapter 4), the Q for the capacitors is largely dependent on the substrate used. In this case, a Q of 130 at 2.4 GHz is required for the capacitors. As seen in the previous chapter the ideal choice of material for this application would be Zyvex™, which can provide unloaded Q's as high as 200 for capacitors around1pF at ~2 GHz. As expected, higher Q for the capacitors as a result of the lower loss dielectric material should decrease the insertion loss as compared to the multialyer ceramic filter.

In this section, a novel topology for realizing filters on organic substrates has been used. The design uses all embedded passives fabricated using standard design rules used in multi-layer boards, as described in Appendix B. The substrate was processed using the methods discussed in Appendix A. Similar to the filter for PCS application, described in the previous section, the integrated filter was also fabricated using a two metal layer process.

The layout for the filter, which represents element values shown in Figure 5.5a, is shown in Figure 5.12a with the cross-section of the testbed shown in 5.12b.

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(a)

Figure 5.12 a) Layout for Bluetooth application with all embedded passives
b) Cross-section of the bandpass filter

The buried metal layer and the top metal layer thicknesses are ~ 15um. The topology used for the implementation of this filter is a CPW topology, which can be clearly seen in Figure 5.12a where the ground reference is coplanar for all devices. The initial dimensions for all the individual components were extracted using the modeling and optimization methods explained in Chapters 3 and 4. However, SONNET was used to simulate the entire device, to understand the effects of discontinuities like T-sections, bends and also optimize the spacing between the inductors and capacitors to ensure minimal coupling. Figure 5.13 shows results from SONNET for the filter layout shown in Figure 5.12. The conductor losses were ignored in the simulations, since SONNET overestimates conductor losses by almost 100% as discussed in Chapter 3. As seen in Figure 5.13, the simulated result meets the specifications with a center frequency of 2.4 GHz, 1dB passband of 100 MHz, and 40dB rejection at 2.1 GHz. The insertion loss, which includes the dielectric loss effect and ignores conductor losses, is ~ 0.8dB.

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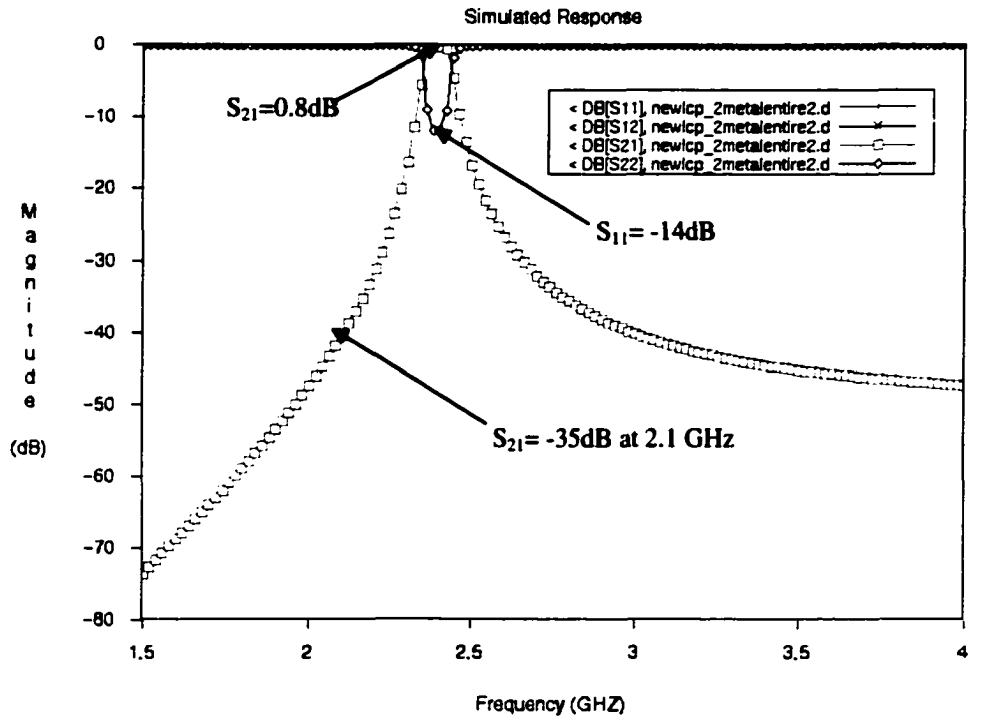

Figure 5.13 Simulated data for Bluetooth filter from SONNET showing S_{21}(dB) and S_{11}(dB) vs. Frequency

An equivalent circuit model for the filter layout is shown in Figure 5.14. The measured data for the fabricated filter and simulated data using the equivalent circuit in Figure 5.14, is shown in Figure 5.15. As seen there is excellent correlation between measured data and simulated data. Since the Q achieved for the capacitors is greater than what is needed to

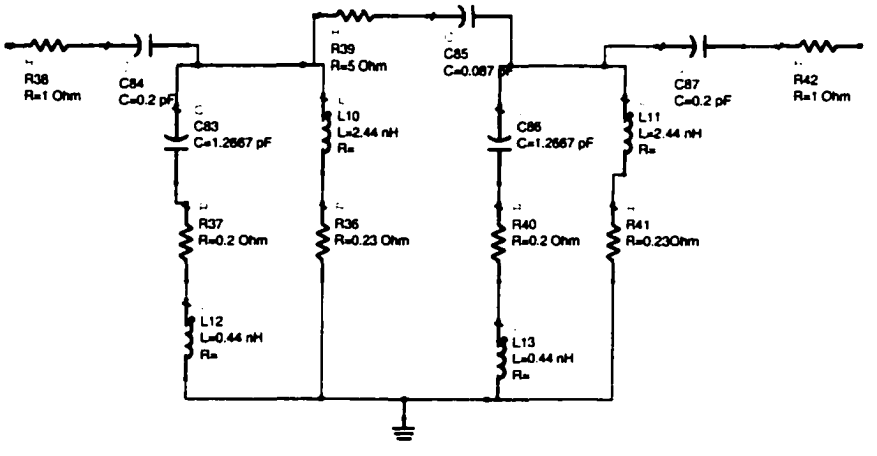

Figure 5.14. Equivalent circuit for Bluetooth filter implemented using all embedded passives in Zyvex™

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attain an insertion loss of 2.8dB, which is the insertion loss measured for the MLC filter, the filter implemented using Zyvex™ shows an insertion loss of only 2.22dB.

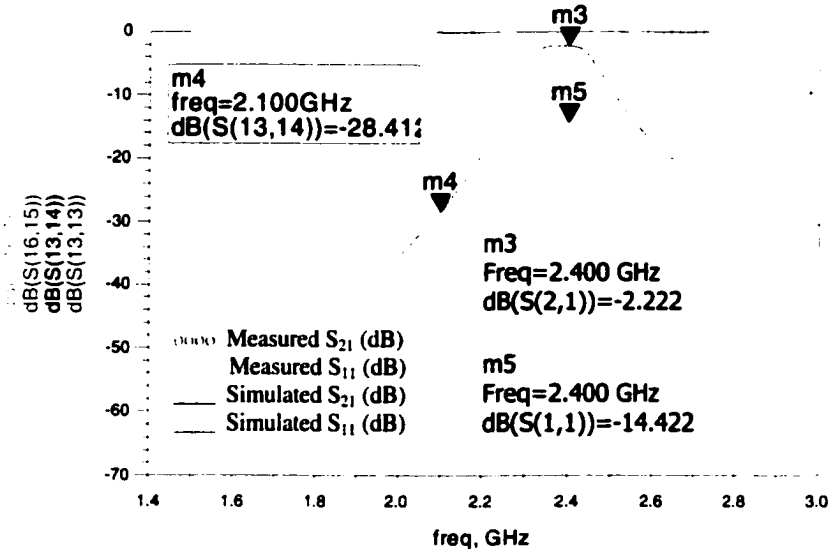

Figure 5.15 Model to hardware correlation for Bluetooth filter

Figure 5.16 shows an actual Bluetooth filter fabricated using Zyvex™ as the dielectric material.

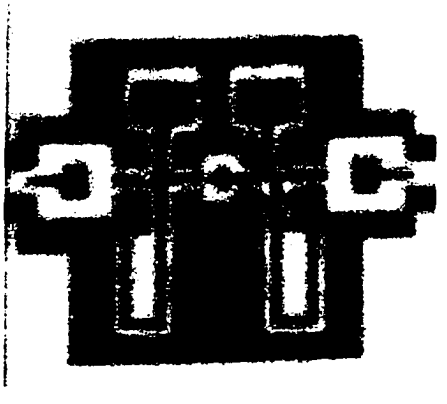

Figure 5.16 Bluetooth filter fabricated using Zyvex™

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In summary, the filter described here is a new CPW topology that uses only two metallization levels and all embedded passives in an organic substrate and betters the performance of non-standardized multilayer (>5) ceramic processes. As the adoption of lower loss materials such as Zyvex™ is becoming popular, this design shows the feasibility of integrating very low loss filters for applications such as Bluetooth in compact boards and packages without the need for any surface mount devices.

Another point worth noting is that while the Q of capacitors is as high as 200 using Zyvex, the Q for the inductor is kept at the required level of ~130. This was done to understand the advantages of using a material such as Zyvex without optimizing the design for the inductors. The insertion loss was 0.6dB lower than the MLC filters. However, Qs exceeding 200 are also attainable for inductors on organic substrates, as shown in chapter 4. A resimulation for the filter circuit shown in Figure 5.14, but with Qs of 200 for the inductors, showed an insertion loss of 1.65dB when simulated in ADS. A filter with a loss of 1.65dB at the frequency and bandwidth desired of the Bluetooth filter can be alternatively achieved only by using the bulkier and costlier ceramic cavity filters.

The next section discusses the design of a filter using very high Q inductors and capacitors to emulate the performance of Filter 3 in Table 5.1. For this filter implementation, the size of the cavity filter is $300mm^3$ while the filter proposed here measures $30mm^3$.

5.4 Realization of bandpass filters for IEEE 802.11b applications

A ceramic cavity filter suggested for the IEEE 802.11b communication standard, shown as Filter 3 in Table 5.1, has the following characteristics: center frequency (f_o)

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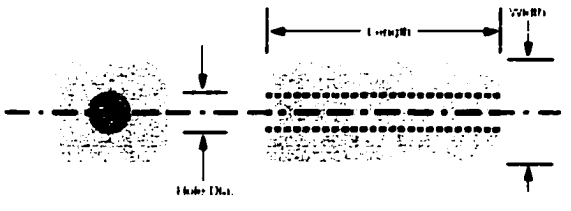
euqal to 2.4 GHz, 3dB bandwidth (BW) euqal to 90 MHz, and a loaded Q of 27. The insertion loss at f_o is 2.4dB with 40dB rejection at f_o±200 MHz. The schematic in Figure 5.6a emulates the performance of this filter and shows that a Q of 210 at 2.4 GHz is needed for inductors and capacitors. The Q factor of 210 required at 2.4 GHz is also the Q associated with a 2mm ceramic cavity resonator, which is the smallest available cavity resonator. The dimensions of individual cavity resonators, 2mm-12mm with different hole diameters, is shown in Figure 5.17. The length of the resonator is dependent on the dielectric material used. The smallest possible resonator usable at 2.4 GHz would then be the 2mm resonator fabricated using a ceramic material with a relative permittivity of 90. The length for a quarter wavelength resonator at 2.4 GHz would then be 314.6/2400 inches = 6.5mm with a height of 3mm. The number of sections required to achieve the desired attenuation at f_o±200 MHz is three. After packaging this filter as a surface mount device, the resulting size would be ~300mm^3.

Mechanical Specifications



Profile (mm)	Width in.(mm)	Hole Dia. in.(mm)
2	.083 (2.11)	.031 (0.78)
4	.152 (3.86)	.045 (1.14)
6	.230 (5.84)	.087 (2.21)
8	.316 (8.03)	.110 (2.79)
10	.394 (10.01)	.118 (3.00)
12	.472 (11.99)	.128 (3.25)

The approximate length of the resonator in inches can be obtained from the following formula where the frequency is in MHz

	Quarter wave	Half wave
Material 1 (k=20)	ℓ=659.8/f_o	ℓ=1319.6/f_o
Material 2 (k=37)	ℓ=485.1/f_o	ℓ=970.2/f_o
Material 3 (k=90)	ℓ=314.6/f_o	ℓ=629.1/f_o

Figure 5.17 Mechanical specifications for ceramic cavity resonators

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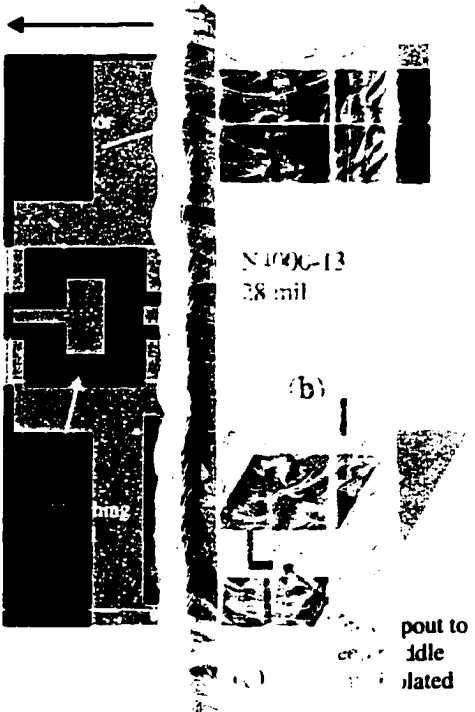

Figure 5 [illegible]

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In this section, a filter similar to the CPW topology in section 5.3 has been discussed for the IEEE 802.11b standard. The substrate was processed using the methods discussed in Appendix A. Although the filter can be designed using two metal layers, the filter discussed here uses three metal layers to show the size reduction possible by going to more than two layers.

The layout for the filter, which represents element values shown in Figure 5.6a, is shown in Figure 5.18a and the cross-section of the testbed shown in 5.18b. The capacitors are implemented as three plate vertically inter-digitated capacitors, as shown in Figure 5.18c. The inductors have been modified to provide Qs of ~200 at 2.4 GHz. With the three layer design, the size of the components reduces to 5 by 4=20mm^2 compared to the filter in the last section which was ~30mm^2. The buried metal layers and the top metal

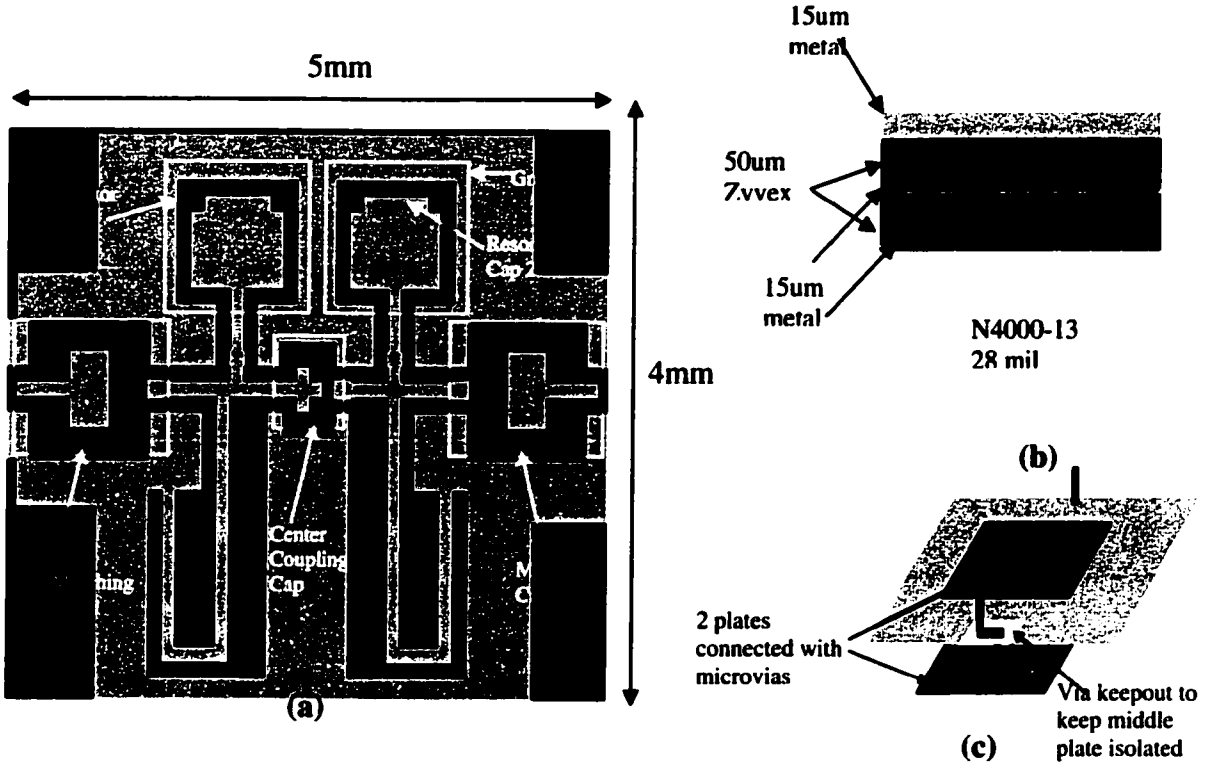

Figure 5.18 a) Layout for 802.11b application with all embedded passives
b) Cross-section of the testbed
c) Vertically inter-digitated capacitor

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layer thicknesses are ~ 15um. The topology used for the implementation of this filter is a CPW topology, which can be clearly seen in Figure 5.18a where the ground reference is coplanar for all devices. Figure 5.19 shows the simulated data obtained using SONNET. By including the dielectric loss and ignoring the conductor loss the filter exhibits a loss of ~1.1dB. The initial dimensions for all the individual components were extracted using the modeling and optimization methods explained in Chapters 3 and 4. However, SONNET was used to simulate the entire device, to understand the effects of discontinuities like T-sections and bends and also to optimize the spacing between the inductors and capacitors to ensure minimal coupling. An equivalent circuit for the filter was extracted and the loss in the filter is expected to increase to ~2.4dB due to the conductor losses in the filter device. The conductor loss can be estimated for the inductors using the modeling methods in Chapter 3. Adding conductor to the equivalent circuit models for the filters helps predict the total loss in the device which in this instance is ~2.4dB.

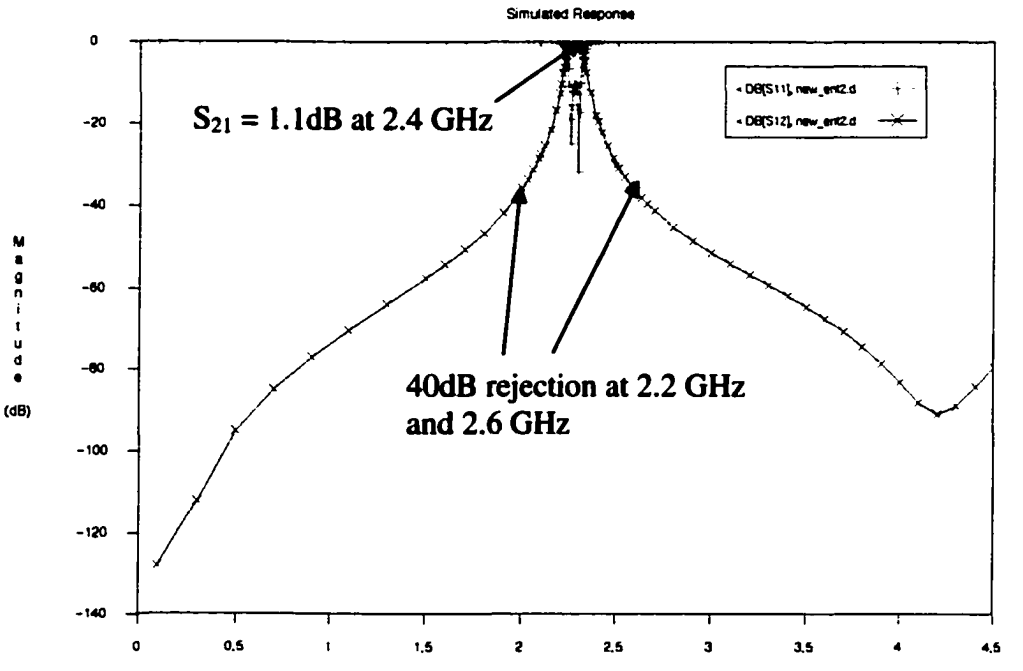

Figure 5.19 Simulated data for IEEE 802.11b filter from SONNET showing S_{21}(dB) and S_{11}(dB) vs. Frequency (GHz)

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The filter meets all the specifications of the cavity filter and IEEE 802.11b standard, namely a 3dB bandwidth of 90 MHz with 40 dB rejection at 2.2 and 2.6 GHz. The fabrication of the filter is currently in progress.

In summary, this filter showed ~15X reduction in volume compared to the ceramic cavity filter and 3X reduction in surface area. The filter would therefore be useful for applications requiring low profiles and compact sizes. Additionally, with the advent of thinner materials such as 1mil (25um) Zyvex™, the filter size can potentially reduce by another 30-40% with a resulting size of 3mm by 3mm and a volume of $9mm^3$, showing an attractive alternative to ceramic cavity filters with significant cost and size advantages.

5.5 Summary

In this chapter, filters have been discussed with all passives embedded in the organic package or board, using a novel CPW topology that uses just two metallization levels. For more compactness, a design with three layers has also been shown. In another instance, the use of two discrete capacitors has been made to adjust for the losses in the material. All filters emulate the performance of MLC filters and ceramic cavity filters and have been realized using standard multi-layer board fabrication design rules. Table 5.2 shows a comparison of filters fabricated using organic substrates and ceramic processes.

Table 5.2 Comparison of filters fabricated using organic substrates and ceramic processes

Type and Size		S_{21}(dB)		f_0	BW	Applications
Organic	Ceramic	Organic	Ceramic	GHz	MHz	PCS
Vialux™: $17mm^3$	$16mm^3$	3.8	3	1.9	120	
Zyvex™: $21mm^3$	$16mm^3$	2.22	2.8	2.4	300	Bluetooth
Zyvex™: $14mm^3$	$300mm^3$	2.4	2.5	2.4	90	IEEE 802.11a

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CHAPTER VI

6. DESIGN OF ACTIVE MODULES FOR MULTIBAND APPLICATIONS WITH EMBEDDED PASSIVES IN ORGANIC SUBSTRATES

Introduction

With advancements in IC processing technology, be it CMOS, GaAs or SiGe technologies, keen interest lies in integrating active circuitry such as amplifiers and oscillators at RF frequencies with embedded passives on the chip. In recent years, several publications have reported RF circuits designed for CMOS processes ([34]-[35]). However, the lack of high-Q inductors (Q~5 at 2GHz in CMOS, Q~30 at 5 GHz on GaAs and SiGe) as well as the poor Q of ~30 for on-chip capacitors has prevented complete integration. Many of these circuits use external devices to meet impedance matching and Noise Figure requirements for low noise amplifiers (LNAs) ([34], [35]). For oscillator type applications external resonator tanks are used to achieve the desired the phase-noise performance of the devices. The use of high-Q passives embedded in the package substrate presents an opportunity to have a completely integrated low cost device, at the same time meeting impedance matching and NF requirements.

In a typical low-noise amplifier application as shown in Figure 6.1 (shown as Figure 1.9 in Chapter 1), the external components needed are the input and output matching networks; input and output blocking capacitors, and a V_{CC} bypass capacitor [13]. The device shown in Figure 6.1 is a GaAs HBT device, and with the given layout in Figure 6.1 recommended by RFMD for 900 MHz applications, shows a minimal noise-figure of 1.6dB and a gain of ~18dB. The noise figure of 1.6dB is attained using chip inductors and chip capacitors, both with unloaded Q~50 at 900 MHz.

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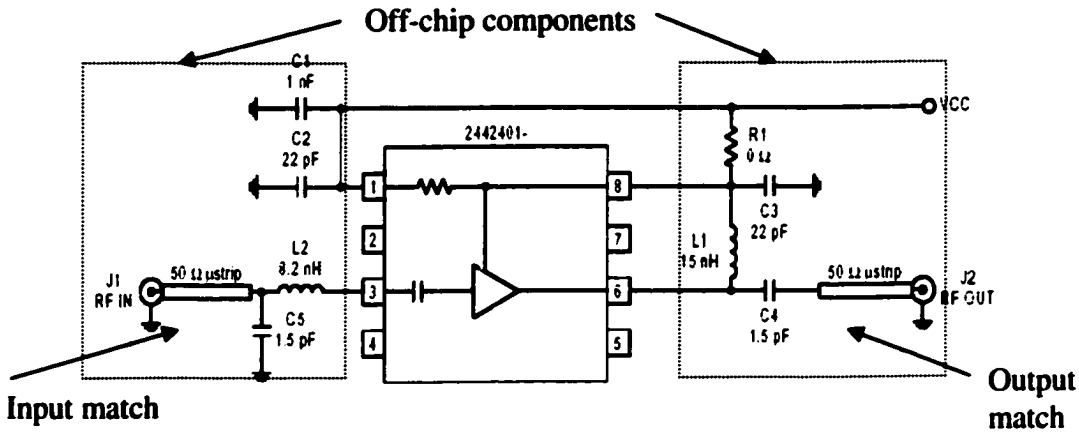

Figure 6.1. Schematic of a 900 MHz LNA application from RFMD showing the components required for low NF [13]

Similarly, in a typical low-phase noise oscillator application as shown in Figure 6.2, optimum performance is achieved with an off-chip resonator tank. The IC from RFMD in Figure 6.2 is designed to oscillate into a resonator with Q greater than 10. The performance of the oscillator is measured with an off-chip inductor, which serves as the resonator, and is connected at pin 2. A phase noise of –104dBc at 100KHz offset is measured when an inductor with a Q~50 is used. Changing the effective inductance, either physically or with a varactor-tuned circuit, will change the frequency of operation.

Traditionally, as mentioned, the input and output matching networks, resonator tanks,

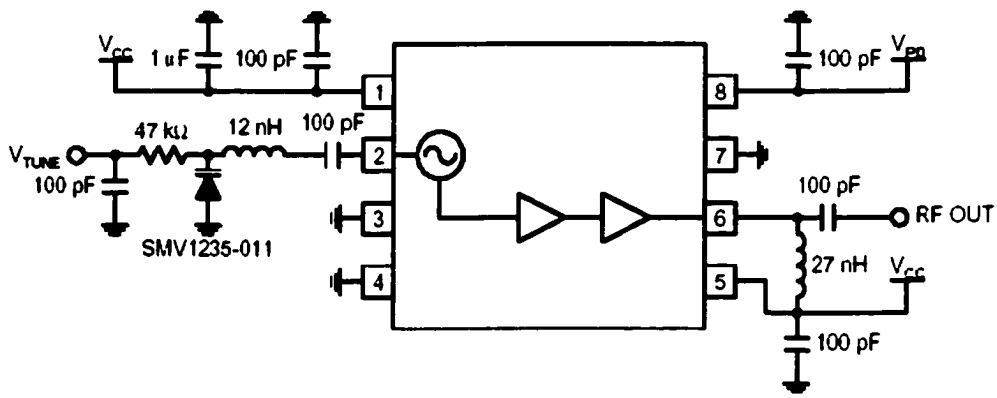

Figure 6.2. Schematic of a 900 MHz VCO application from RFMD showing the external components required for minimal phase noise

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blocking capacitors and bypass capacitors were implemented using discrete components. Similar to filters, most of the integration of these passive devices has been demonstrated using multilayer LTCC technologies and MCM-D technologies while little has been done to explore the fabrication of such devices using MCM-L technologies.

The work done in this chapter shows the feasibility of using embedded inductors and capacitors such as those fabricated in previous chapters for their use in LNA and oscillator applications using organic technology.

The chapter is organized as follows: section 6.1 briefly introduces the essentials of LNA design. This is followed by the design and modeling of integrated LNAs for PCS (1.9GHz) applications in sections 6.2. The designs use high Q passives embedded in the organic substrates for the input and matching circuitry similar to those mentioned in previous chapters. The bias resistors and decoupling capacitors have been implemented as discrete components. Integration of filters, such as those presented in Chapter 5, and low noise amplifiers can result in significant reduction in number of components. The impedance matching networks required for a LNA can be integrated into the filter, thereby effecting a 30%-70% reduction in the total number of embedded components. An example of an integrated bandpass filter and amplifier has been presented in section 6.3. Finally, the design and modeling of oscillators, which also use embedded passives, is presented in section 6.4.

6.1 Low Noise Amplifier Design

In any wireless architecture, the first active device of the RF frontend is the LNA. This amplifier circuit needs to be extremely sensitive to detect the incoming signal, as well as having a good input impedance matching circuit. The NF of an LNA is a measure of the

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amount of noise added by the circuit to the incoming signal, and is defined as the ratio of Signal-to-Noise Ratio (SNR) at the input of the device to the SNR at the output (6.1). It quantifies the amount of noise power added by the device, or the degradation of the SNR.

$$NF = \frac{(SNR)_{in}}{(SNR)_{out}} \tag{6.1}$$

The basic LNA architecture consists of an active device with impedance transformation networks at the input and output. The input impedance transformation network transforms 50Ω (from the band pass filter) to the optimum impedance required for minimum NF. If the output of the amplifier has to be connected to an external component (for example, a filter), an output impedance transformation network is also required, to transform the impedance at the collector/drain to 50Ω.

The Q factor of a passive device used in the input or output match can be modeled as a resistance placed in series with a lossless capacitor or inductor. Resistors act as white noise sources and contribute to increasing the NF of the device. Hence, high Q passives are required in the design of LNAs. Typically, Qs of on-chip inductors vary from 5-10, and this leads to an increase in the noise figure of the LNA. The alternative of using a discrete high Q inductor defeats the goal of integration and miniaturization. Embedded passives in the package substrate offer a third choice to designers, by incorporating very high Q factor as well as a higher level of integration than the use of discrete passives.

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V. Govind, et al. have derived the noise figure in [12] for an inductively degenerated CMOS LNA. The variation of the NF with respect to the Qs of the inductors is shown in Figure 6.3. In [12], the circuit was designed for the AMI 0.5u process, with a standard source resistance of 50Ω and an operating frequency of 1.9 GHz; leading to inductance values of L_g=11 nH and L_s=0.7 nH, which are present at the gate and source of the active device, respectively. Since accurate short channel data for α, β, γ and c values were not available in [12], they had to be assumed from long channel approximations. The NF decreases from about 4.1 dB to 2 dB as the Q of the gate inductor is increased from 10 (on chip) to 150 (off chip). In practice, on-chip inductors have Qs significantly lower than 10 at high inductance values, and the degradation in NF is much more.

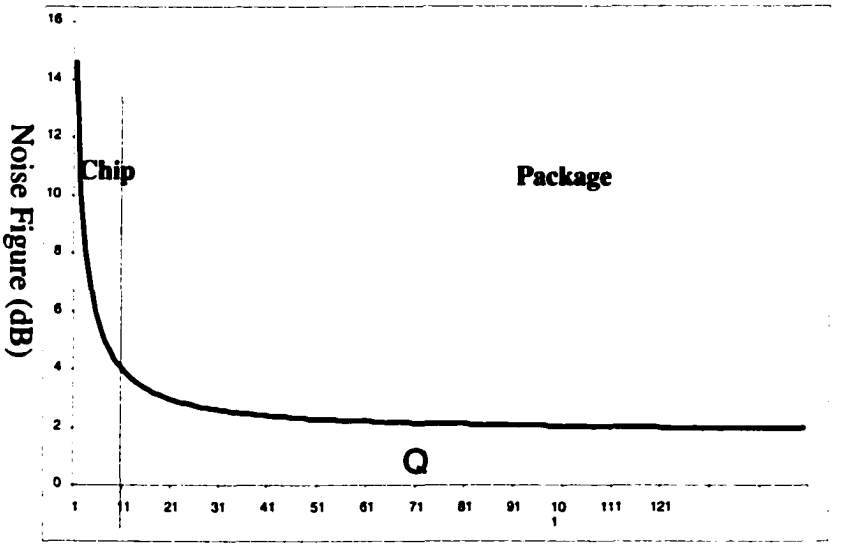

Figure 6.3 Variation in Noise Figure with respect to gate inductor Q for a Low Noise Amplifier [12]

However, the improvement in NF decreases as Q is increased. The change in NF is very small beyond a Q of 50. Coincidently, this is also the Q that is available with standard chip inductors from manufacturers like AVX, and hence used by IC manufacturers such

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as RFMD for validation of their IC technology for LNA type applications. Nonetheless, the usage of discrete passives suffer from disadvantages like lead time of 4-6 weeks, degradation of performance after assembly and assembly costs. The best method for achieving an integrated solution with reasonable NF and tolerance to variations during fabrication is to embed the inductance off-chip, in the package or in the board itself.

The work presented so far in this dissertation has shown embedded inductors and capacitors with Qs greater than 100. However, a Q of 50 is all that is desired for achieving next to minimum NF in LNA type topologies as shown in [12]. This leads to the possibility that the embedded inductors (which currently have a Q > 100) can be reduced in size (leading to lower Qs), resulting in a reduction of the total size of the packaged LNA. Moreover, the use of lower cost epoxy based substrates like Vialux™ is sufficient since it provides Qs of 50 for capacitors as seen in Chapter 4.

6.2 Design of a PCS Low-noise amplifier

Figure 6.4 shows the design of a hybrid LNA, using a discrete HBFP-0420 dual emitter transistor in a SOT-343 package and high Q embedded inductors and capacitors. In the figure, the bias circuit has been omitted. V. Govind at the Georgia Institute of Technology, a graduate research assistant in Prof. Swaminathan's research group, was the primary designer of the circuit schematic in Figure 6.4a. It consists of the transistor biased in the common emitter configuration. The input and output of the transistor are matched to 50Ω by using L-C "pi" networks, which are entirely embedded in the package (the use of "pi" networks instead of "L" networks results in improved bandwidth for the circuit). The output pi is designed for maximum power transfer, and thus performs

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impedance transformation from the complex conjugate of the collector impedance to 50Ω. The input pi is designed for minimum noise figure, and presents the minimum NF to the gate of the transistor.

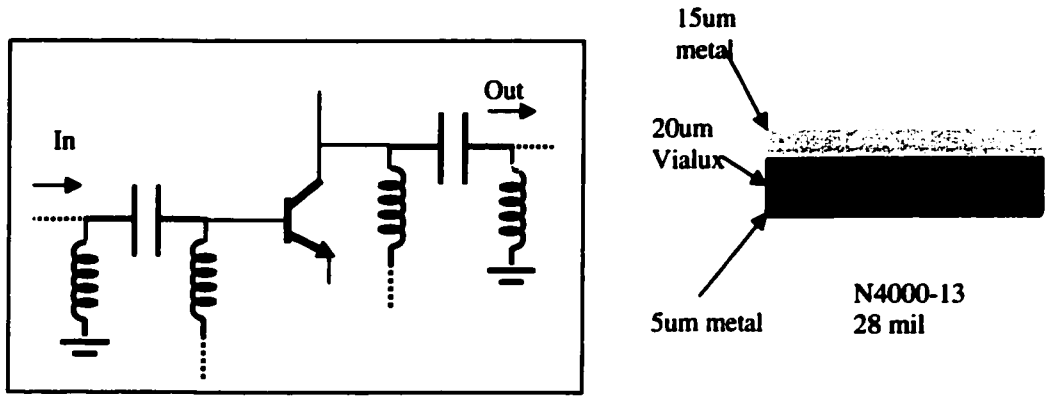

Fig 6.4. a) Integrated LNA, with impedance transformation networks
b) Cross-section of testbed

The pi networks were designed using SONNET using the cross-section in Figure 6.4b. As shown earlier, unloaded Q's ~ 50 for the passives was enough to attain near minimum noise figure. Although Q's greater than 150 were achieved in Chapter 4, the designs occupied greater than $9mm^2$ of the surface area. The design of inductors for the purposes of this work was constrained to a maximum surface area of $2mm^2$ and the overall pi matching networks were limited to $6mm^2$. The device was designed using a CPW topology where the ground is coplanar for all the devices as shown in Figure 6.5. The discrete components used for biasing, decoupling and noise sinks are also shown in Figure 6.5. The layout of the circuit, which includes the design of the pi networks, was done as a part of this dissertation to show the feasibility of embedded passives fabricated using organic materials and laminate technology for integrating active modules.

Simulations using ADS showed a gain of 14.6 dB and a NF of 2.22 dB at 1.9 GHz as seen in Figure 6.6.

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R1=65 ohms, R2=50 ohms, C1=1000pF decoupling cap,
C2=C3=noise sink=10pF, R3=16 Kohms, R4=50ohms, R5=13ohms
All components are reference size 0603 for discrete components

Figure 6.5 Top view of PCS LNA layout

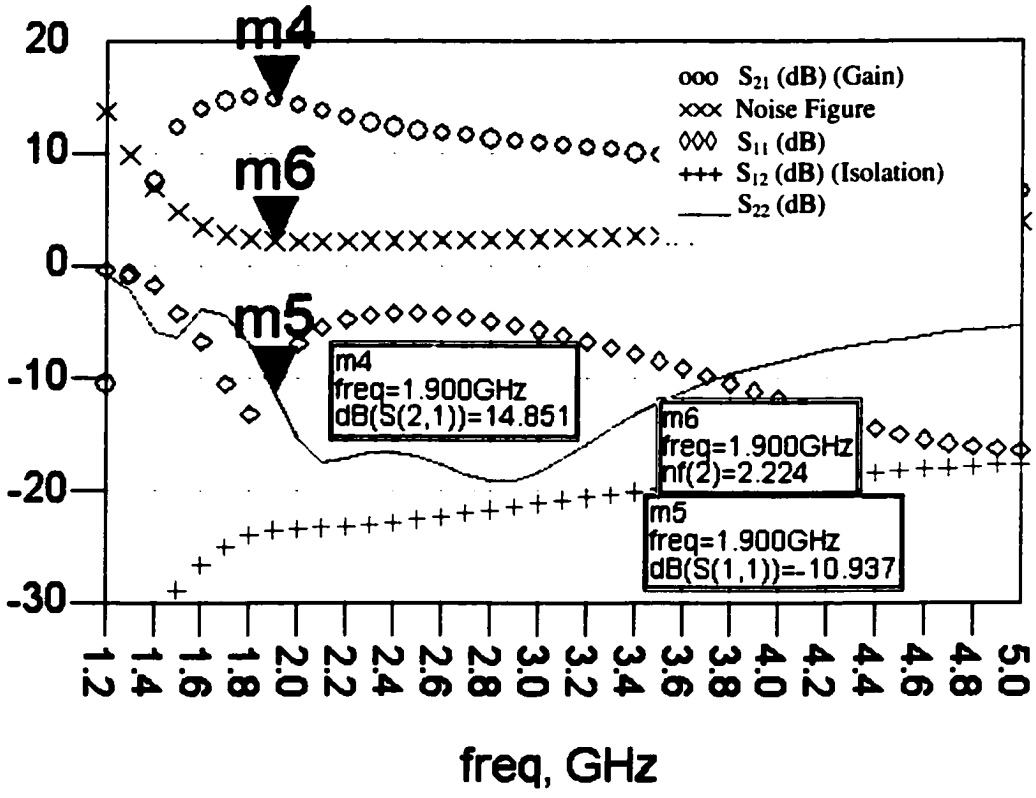

Figure 6.6 Simulated data for PCS LNA using ADS

However, after the device was fabricated and all discretes including the IC were soldered, the measurement showed no gain and showed instability at ~1.1 GHz. Upon revisiting the simulations done in ADS and including all possible parasitics, it was seen that the 10pF discrete capacitor, originally assumed to be in the bias network, was affecting the small signal equivalent circuit. The 0603 sized 10pF capacitor which resonated at 400 MHz was replaced by a smaller valued 2pF capacitor with a resonant frequency of 3GHz. At 1.9 GHz, the 2pF capacitor provided only 4pF equivalent capacitance. However, the circuit was then stable and the measurement showed a gain of ~10dB at 1.9 GHz and a match of ~ -6dB at 1.9 GHz. Figure 6.7 shows preliminary data and model to hardware correlation for the modified circuit of the LNA showing proof of concept. An approximate equivalent circuit for the 2pF discrete capacitor was used for obtaining the simulated response.

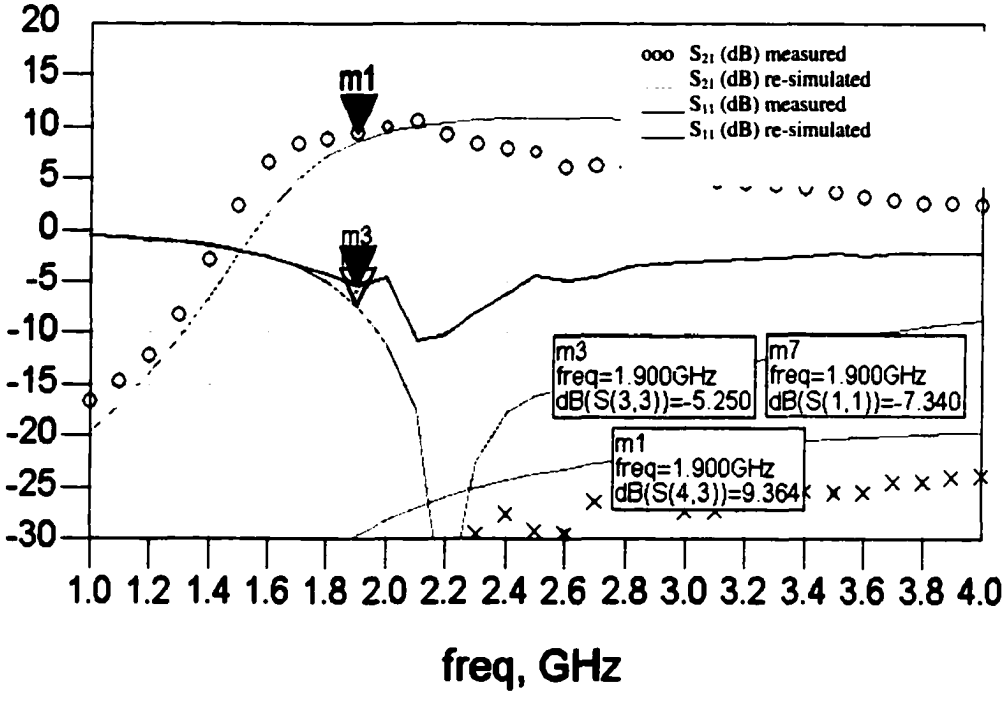

Figure 6.7 Model to hardware correlation for modified circuit of LNA used as a proof of concept device

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Since the measured and modeled S_{11} show discrepancy in Figure 6.7, for the purposes of verification, the input PI network was measured as a stand-alone network and compared with the lumped circuit model. As seen from Figure 6.8, there is good model to hardware correlation for the PI networks. The discrepancy in Figure 6.7 can be explained due to the lack of characterization data available for the 2pF capacitors.

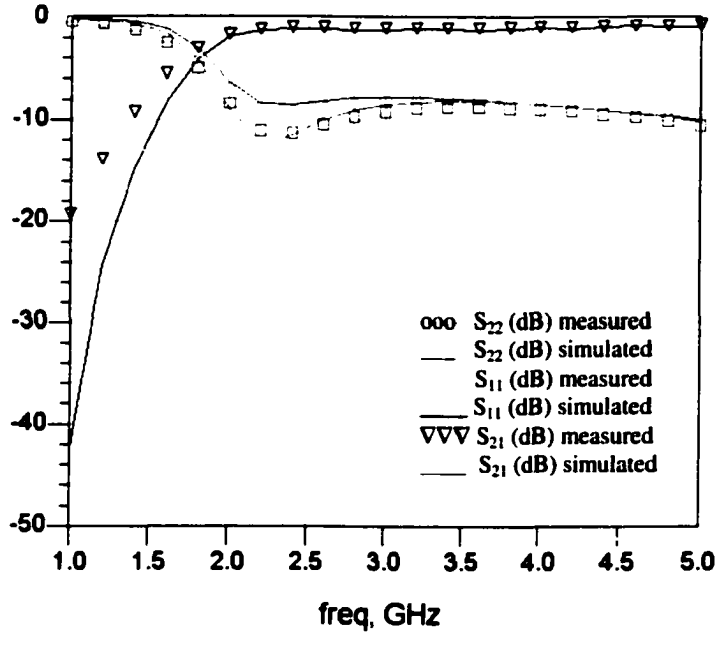

Figure 6.8 Model to hardware correlation for input PI network

In summary, pending some minor re-designs (fabrication and design of a new LNA is in progress at the time of this writing), it was shown that high-Q passives embedded in the package substrate provide a good alternative to using low-Q on-chip inductors or discrete inductors and capacitors. The feasibility of using embedded passives has been demonstrated by the design of an integrated LNA, using 6 embedded passives.

Figure 6.9 shows a fabricated LNA with embedded passives, discrete passives and a discrete BJT.

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Figure 6.9 LNA fabricated on Vialux™

Designing stand alone LNAs with embedded passives in the package or board, as shown in this section, is one of the key elements towards integration as well as achieving maximum performance the IC technology offers by leveraging the higher Q's of embedded passives. Additionally, the filter designs in the previous chapter, which use all embedded passives in the package or board, show the feasibility of even higher integration. The PI or L networks used for matching the input and output of the LNA can be transformed to bandpass networks, as shown in next section, possibly removing the need for pre-LNA and post-LNA filtering and achieving lower component count.

6.3 Design of integrated bandpass filters and LNA

An example of a typical front-end for a heterodyne type receiver, discussed in Chapter 1, includes the front-end filter followed by the LNA followed by the image-reject filter as shown in Figure 6.9. The respective topologies used in this work are also shown in the filter. With this particular topology for the frontend, a total of 20 passive components (7 for each filter, plus an additional 6 for the LNA) would be required. However, if a newer topology shown in Figure 6.10 is used where the components in the PI and L networks

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are transformed into resonator tanks, the functionality of the bandpass filters can be embedded inside the PI networks, thereby reducing the number of passives required from 20 to 8.

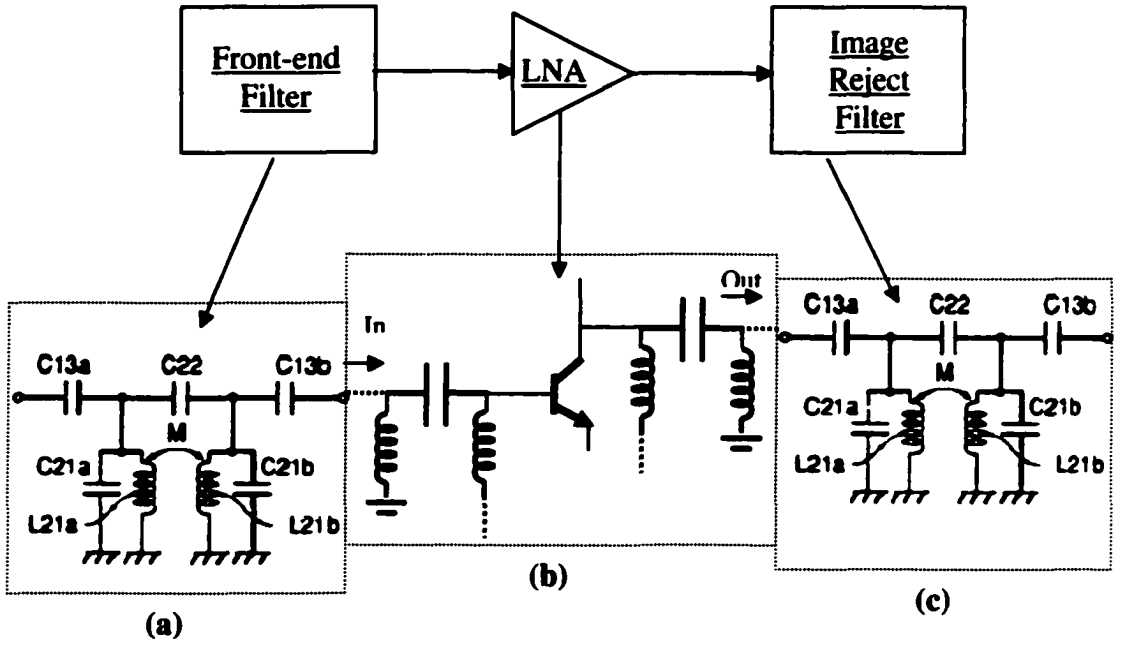

Fig 6.10. a) Front-end filter topology
b) LNA topology
c) Image reject filter topology

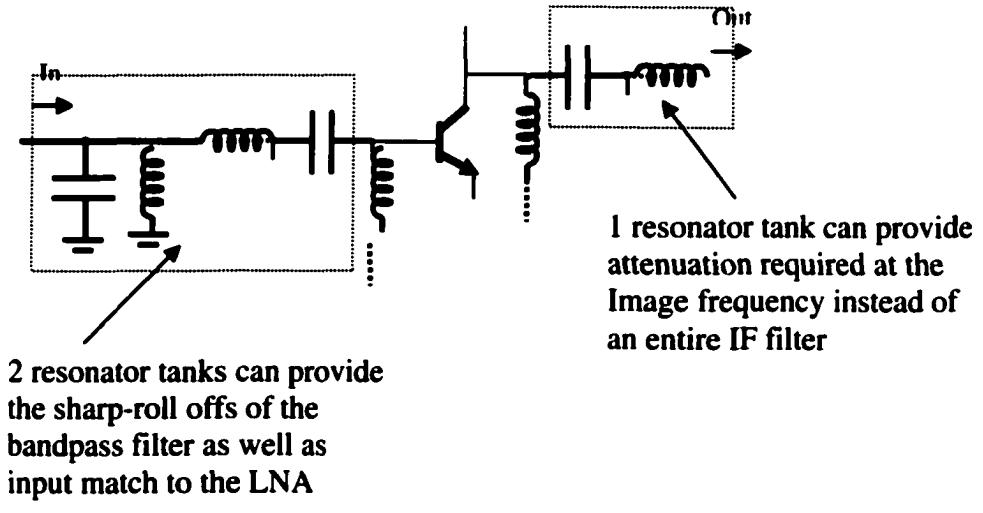

Figure 6.11 Modified topology for integrated bandpass filters and LNA

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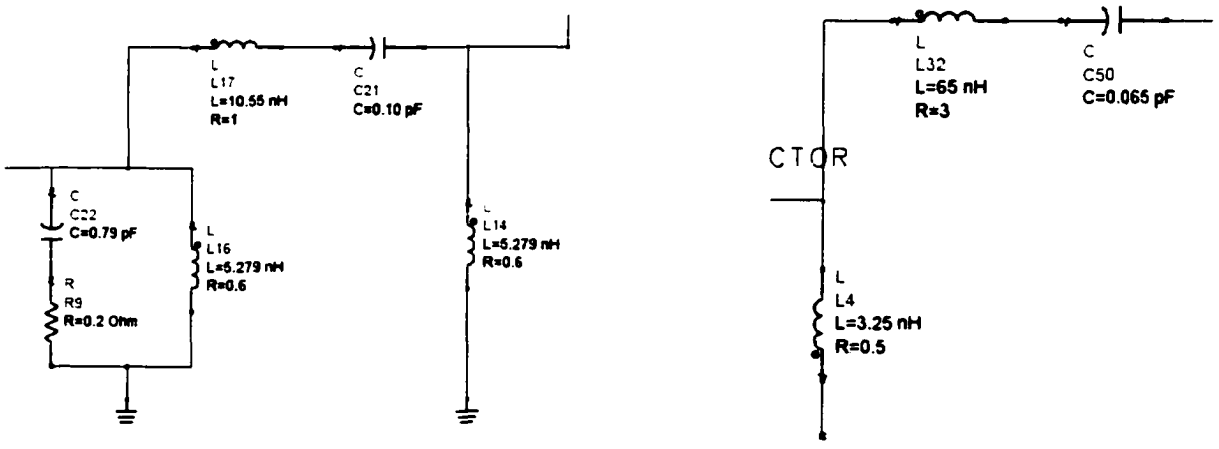
Figure 6.12 shows examples of modified input and output networks for use with the discrete HBFP-0420 dual emitter transistor in a SOT-343 package, (used in the previous section for PCS band LNA), designed here for operation at 2.45 GHz for Bluetooth applications. The simulated data obtained using the topologies from Figure 6.12 for the integrated LNA bandpass filter design is shown in Figure 6.13. The device achieves the required attenuation levels of ~25dB at 1.9 GHz and ~45dB at 5.2 GHz.



(a) (b)

Figure 6.12 a) Input PI designed for 2.4 GHz integrated bandpass filter and LNA
b) Output PI designed for 2.4 GHz integrated bandpass filter and LNA

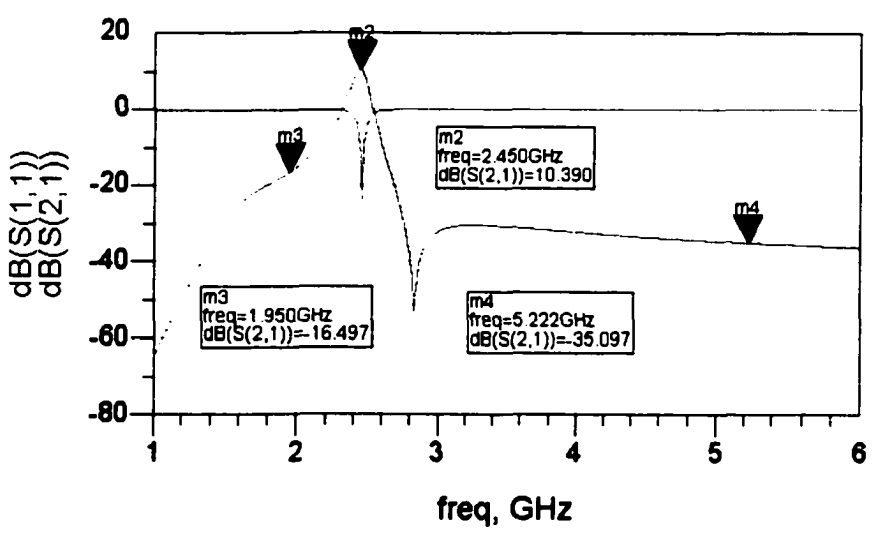


Figure 6.13 Simulation data from ADS for 2.45 GHz integrated BPF LNA

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6.4 Design of an integrated oscillator

Figure 6.14 shows the design of a hybrid oscillator, using a discrete HBFP-0420 dual emitter transistor in a SOT-343 package and high Q embedded inductors and capacitors. The figure includes two discrete resistors, R_B and R_E, for biasing. A. Bavisi at the Georgia Institute of Technology, a graduate research assistant in Prof. Swaminathan's research group and co-advised by Prof. Ayazi, was a co-designer of the circuit schematic in Figure 6.14.

The basic necessity for an oscillator is a feedback from the output to the input that increases the input signal, which in this case is noise required to start the oscillations. The tank being in the collector of the active device, the signal to be fed must be at the base or the emitter. The topology has a signal fed back to the emitter. The basic problem of feeding the signal to the emitter is that the input resistance looking into the emitter is $1/g_m$

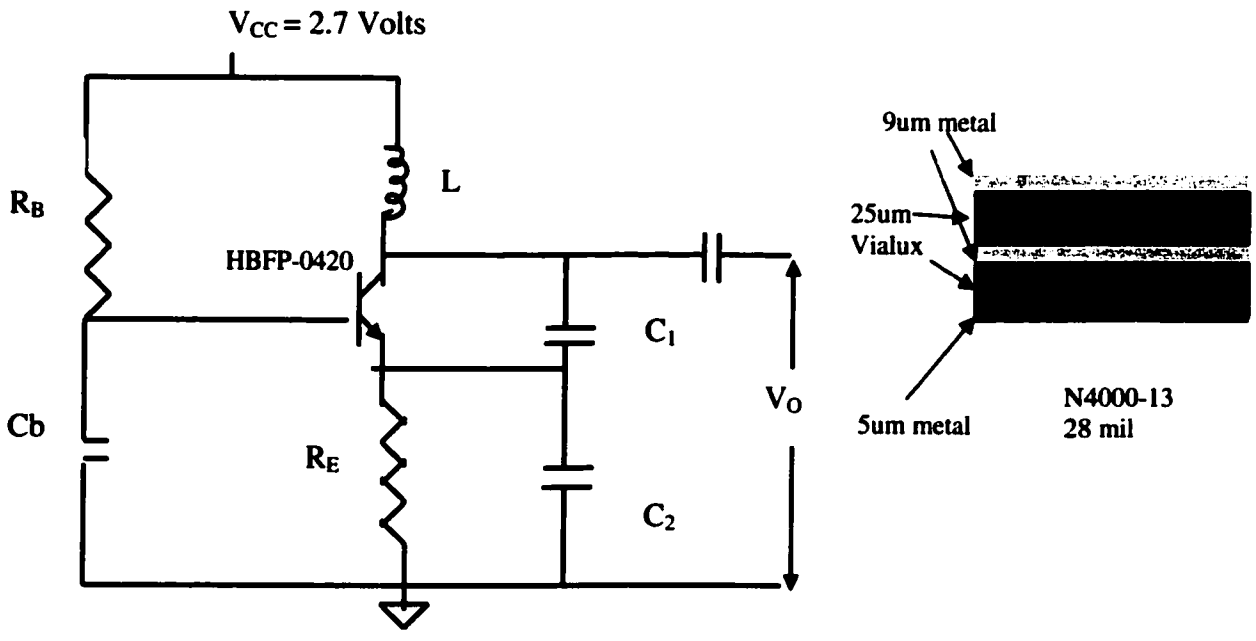

Figure 6.14 a) Colpitts oscillator designed for operation at 2.4 GHZ
b) Cross-section of testbed for integrating oscillator with embedded passives

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where g_m is the trans-conductance of the device at a particular bias current. So a transformer is necessary to increase the resistance to a sufficiently large value that does not reduce the Q of the tank formed by L and C_1. As can be seen in the figure, the capacitors C_1 and C_2 perform the function of a capacitive transformer. The impedance across the inductor is $(1+C1/C2)^2 / g_m$. Thus by adjusting the values of C1 and C2 the impedance across the tank can be adjusted. In order to get realistic values for the capacitors C_1 and C_2 a capacitor C_B is added in series with the capacitors.

The output of the transistor is matched to 50Ω by using a capacitor. All elements in the circuit are embedded except the two resistors and the IC itself. The output match is imperative to increase the output power of the oscillator, which helps better the phase noise performance of the oscillator.

The layout for the passive networks was designed using SONNET. Similar to the LNA, unloaded Qs of about 50 for the passives is enough to attain near minimum phase noise performance for the oscillator. Hence, the use of lower cost epoxy based substrates like Vialux™ is sufficient since it provides Qs of 50 for capacitors as seen in Chapter 4. In order to make the designs more compact, a two-layer cross-section was proposed for the substrate as shown in Figure 6.14b. The added layer of Vialux™ was proposed to decrease the capacitor areas by using the vertically inter-digitated topology used for filters in Chapter 5. The layout of the device is shown in Figure 6.15. The device was designed using a CPW topology where the ground is coplanar for all the devices as shown in Figure 6.15. The discrete components used for biasing and decoupling are also shown in Figure 6.15. The layout of the circuit, which includes the design of the passive networks, was done as a part of this dissertation to show the feasibility of embedded

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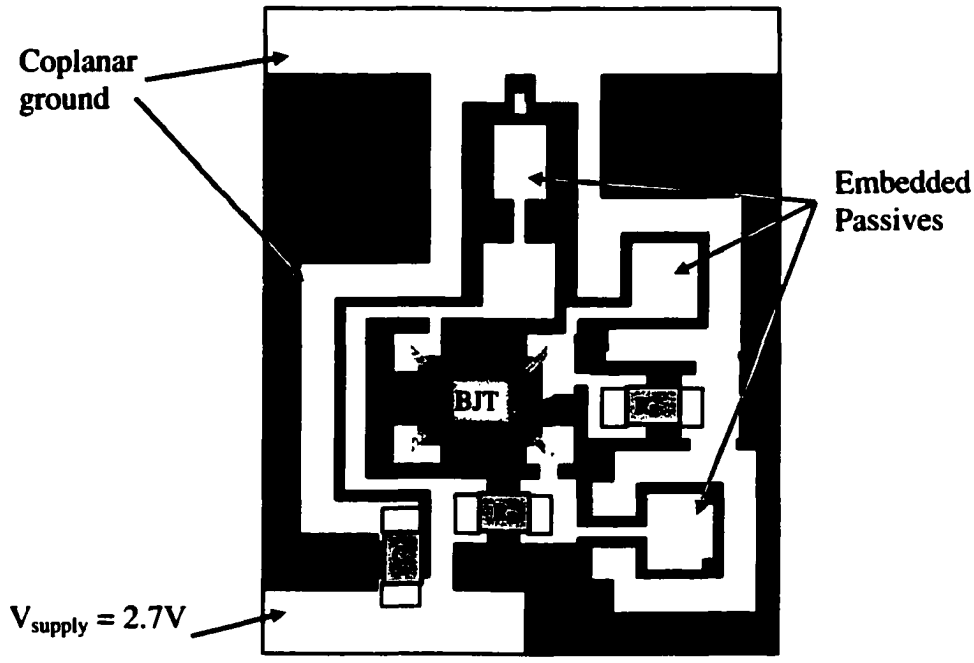
passives fabricated using organic materials and laminate technology for integrating active modules.



R_B=22K ohms, R_E=100 ohms, C=1000pF decoupling cap,
Reference size 0603 for discrete components

Figure 6.15 Top view of 2.4GHz oscillator layout

The oscillator was simulated in ADS after including all the parasitics of the package as well the passives and the active device. The biasing resistors were adjusted to provide a current of 4.2mA for which the transistor parameters are optimized. The total power dissipation in the device is approximately 12.6mW. The output waveform for the oscillator with a matched load of 50 ohms is shown in Figure 6.16.

The output power delivered to the load is 1.84mW or 3dBm. From the waveform it is very clear that the there is no distortion in the sine wave nature of the wave. The output power decreases significantly as soon as the load value is changed or the frequency is varied which indicates a very narrow band of frequency matching. This is due to the

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matching element, which was limited to a single capacitor for compactness. However, the matching circuit could be modified to a L or PI network, as was done for the LNA, to increase the bandwidth of the matching circuits. As the frequency is varied by the variation in the capacitance the load power falls to almost zero. The time period of the waveform is 0.42nsec, as shown in Figure 6.16, which gives frequency of 2.38GHz close to the desired frequency of 2.4GHz.

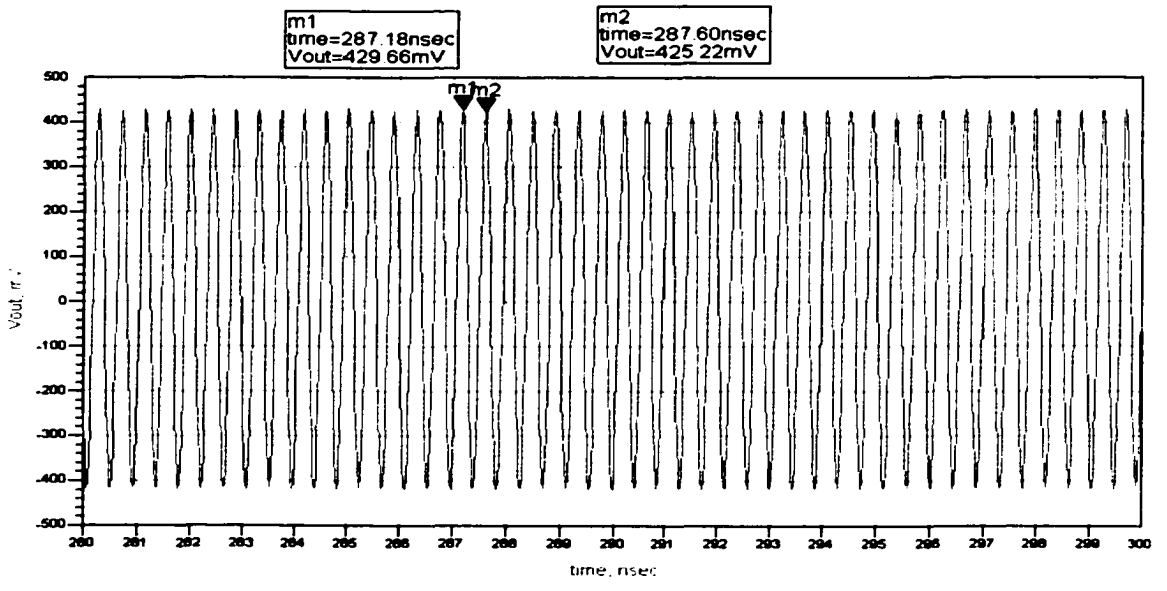

Figure 6.16 Output waveform for the 2.4 GHz oscillator using ADS

The design was meant for a 2-layer Vialux substrate and measured only 5mm by 5mm. However, due to several problems while processing the two layer substrate, just one layer of Vialux was used, i.e. two metal layers instead of three metal layers were fabricated. As a result the capacitors, designed as three plate capacitors, were reduced to half their capacitance. Nonetheless, the device was assembled and measured using Hewlett Packard's 4407b series Spectrum Analyzer. Initially, the device showed no response. Upon careful debugging, it was realized that the matching capacitor was not

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connected due to an open via. As such the device was directly probed at the collector. The measured spectrum from the output of the device is shown in Figure 6.17.

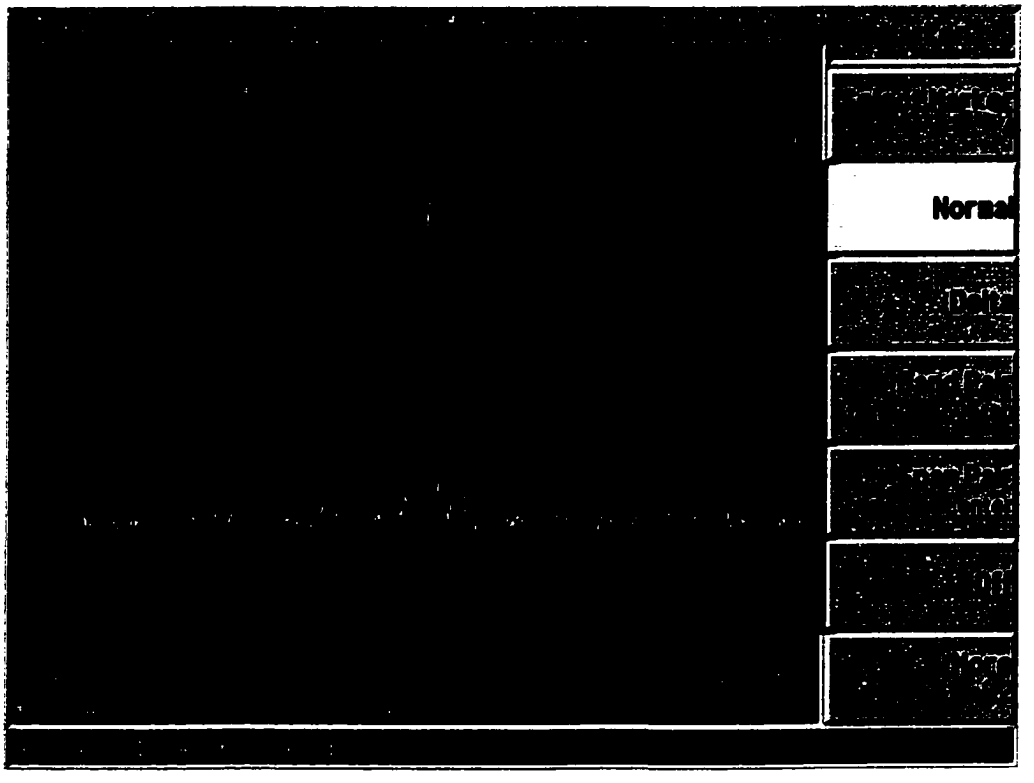

Figure 6.17. Measured spectrum of the oscillator device

As shown in Figure 6.17, the frequency of oscillations shifted to 3.29 GHz and the output power is reduced to –37dbm. The frequency shift can be explained due to the decrease in capacitor values by half due to the fewer metal layers processed, which increases the oscillating frequency by a factor of $\sqrt{2}$ which equatred to the designed frequency of 2.4 times 1.414 ~ 3.3 GHz. This also corresponds to the oscillating frequency measured by the spectrum analyzer. The reduction in power output level can be explained due to the unavailability of the matching capacitor, which was not connected to the device due to process problems.

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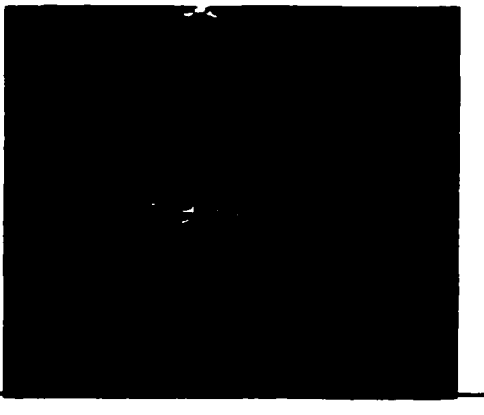
In summary, pending some minor re-designs (fabrication and design of a new oscillator is in progress), it was shown that high-Q passives embedded in the package substrate provide a good alternative to using low-Q on-chip inductors or discrete inductors and capacitors for oscillator applications. The phase noise performance of the device will be measured when the appropriate measurement system is available. Hence, phase noise testing is also in progress. The feasibility of using embedded passives has been demonstrated by the design of an integrated oscillator, using 5 embedded passives with the complete device occupying only 5mm by 5mm.

Figure 6.18 shows a fabricated oscillator with embedded passives, discrete passives and a discrete BJT.

Figure 6.18 Oscillator fabricated using Vialux



6.5 Summary

In summary, pending some re-designs (fabrication and design of new amplifiers and oscillators is in progress at the time of this writing), it was shown that high-Q passives embedded in the package substrate provide a good alternative to using low-Q on-chip inductors and capacitors or discrete inductors and capacitors for active module integration.

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CHAPTER VII

7. CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

The purpose of this section is to summarize the main contributions of this work. The most important contribution is demonstrating the feasibility of using low-cost organic materials and low-temperature large area laminate processing (PWB processing) as an alternative to LTCC, MLC and MCM-D technologies for the design of high Q embedded passive devices for wireless applications. For similar applications, the devices presented in this dissertation are comparable to or smaller than devices manufactured using ceramic or deposition technology. Similarly, in terms of performance, the devices are equivalent to or superior than devices manufactured using other technologies.

However, there were several intermediate steps that helped arrive at the conclusion mentioned above. These include the following:

1. Extension of an existent transmission-line characterization method for the extraction of the dielectric constant and loss tangent of materials as a function of frequency. Several other methods were also used to verify the results obtained using the transmission line method.
2. Characterization of Dupont's Vialux™, Asahi's A-PPE™ and Rogers' Zyvex™ up to 6 GHz through the extraction of the dielectric constant and loss tangent data.
3. Development of a method for modeling and optimizing the performance of passive devices that included frequency dependent dielectric properties. This was verified with measurements up to 8 GHz. The method also included other frequency-related effects such as skin-effect and proximity effect.

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4. Verification, through several testbeds, of the relative independence of unloaded Q's for inductors from the dielectric loss of the materials and obtained Q's as high as 200 for inductances in the range of 1-20nH with SRFs as high as 15 GHz on low-cost epoxy based substrates such as Vialux.
5. Demonstration, through several testbeds, of the importance of dielectric loss on the performance of capacitors. Using newer materials such as Zyvex, obtained Q's exceeding 200 for capacitors in the range of 1-5pF.
6. Construction of bandpass filters for several different applications that perform similar to or better than the performance of MLC, LTCC and cavity filters. The filters are smaller compared to the cavity filters and much easier to construct and fabricate.
7. Validating, through several examples, the feasibility of integrating devices such as oscillators and amplifiers with all embedded passive devices which helps achieve near minimum noise specifications of the relevant IC technology.

7.2 Future Work

The investigation of thinner laminates should be performed for applications such as those mentioned in this dissertation to further reduce sizes of components. Furthermore, the re-design of the active modules, such as those suggested in this dissertation with the topologies mentioned, is imperative to complete the study of passive devices embedded in organic substrates for integration with ICs to achieve functions such as amplification and oscillations.

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7.3 Inventions and Publications Generated

[1] Nanju Na, **Sidharth Dalmia** and Madhavan Swaminathan, "S-parameter based Macromodeling of Resonance in High Speed Packages," 16th General Assembly of the International Union of Radio Science, January 1999.

[2] **Sidharth Dalmia**, Sung-Hwan Min and Madhavan Swaminathan, "Modeling RF passives using coupled theory and scalable functions," *IEEE Electronics Components and Technology Conference*, Orlando, FL, pp. 816-823, May 2001.

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[4] Woopoung Kim, **Sidharth Dalmia** and Madhavan Swaminathan, "Characterization of Embedded Passives using TDR Measurements," *5th IEEE Workshop on Signal Propagation on Interconnects*, Venice, Italy, May 2001.

[5] Sung Hwan Min, et al, "Design, Modeling and Measurement of Scalable Embedded Inductors," *ASME/ IEEE Interpack*, May 2001.

[6] Sung Hwan Min, **Sidharth Dalmia** and Madhavan Swaminathan, "Scalable Embedded Passive Design, Modeling and Characterization," *5th IEEE Workshop on Signal Propagation on Interconnects*, Venice, Italy, May 2001.

[7] **Sidharth Dalmia**, Sung Hwan Min and Madhavan Swaminathan, "Design and Optimization of Embedded RF Filters," *IEEE Radio and Wireless Conference*, Boston, MA, pp. 145-148, August 2001.

[8] Venky Sundaram*, Fuhan Liu, **Sidharth Dalmia**, George E. White, Rao R. Tummala, "Process Integration for Low-Cost System on a Package (SOP)

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Substrate," *IEEE Electronics Components and Technology Conference,* Orlando, FL, pp. 535-540, May 2001.

[9] Sung Jun Chun, Jinseong Choi, **Sidharth Dalmia**, Madhavan Swaminathan, "Capturing Via Effects in Simultaneous Switching Noise Systems," *2001 IEEE International Symposium on Electromagnetic Compatibility*, vol. 2, pp. 1221-1226, August 2001.

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[11] **Sidharth Dalmia**, et al, "CPW High Q Inductors on Organic Substrates," *2001 IEEE Conference on Electrical Performance of Electronic Packaging*, Scottsdale, AZ, pp. 105-108, October 2001.

[12] **Sidharth Dalmia,** et al, "Design of Integral Inductors in Organic Substrates for 1-3 GHz Applications," accepted for publication in *IEEE Journal on Advanced Packaging*, January 2002.

[13] **Sidharth Dalmia,** et al, "Design and Optimization of High Q RF Passives on SOP-based Organic Substrates," *52nd IEEE Electronics Components and Technology Conference,* San Diego, CA, pp. 495-503, May 2002.

[14] **Sidharth Dalmia,** et al, "Design of Inductors for 1-3 GHz Wireless Applications in Organic Substrates," *2002 IEEE International Microwave Symposium*, Seattle, WA, vol. 3, pp. 1405-1408, June 2002.

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[15] S. H. Lee, et al, "High performance spiral inductors embedded on organic substrates for SOP applications," *2002 IEEE International Microwave Symposium*, Seattle, WA, vol. 3, pp. 2229-2232, June 2002.

[16] J. M. Hobbs, et al, "Development and characterization of embedded thin-film capacitors for mixed signal applications on fully organic system-on-package technology," 2002 IEEE Radio and Wireless Conference, Boston, MA, pp. 201-204, August 2002.

[17] V. Govind, **Sidharth Dalmia** and Madhavan Swaminathan, "Design of an Integrated Low Noise Amplifier with Embedded Passives in Organic Substrates," accepted for publication in *2002 IEEE Conference on Electrical Performance of Electronic Packaging*, Monterey, CA, October 2002.

The following inventions were generated based on the completed work:

[1] **Sidharth Dalmia**, M. Swaminathan, G. White, V. Sundaram, S. H. Lee, S. H. Min, W. Kim, F. Ayaazi, "Organic Substrates Having Integrated Passives," Georgia Tech Invention Disclosure # 2409, November 2000. Utility patent application submitted November 2001.

[2] **Sidharth Dalmia**, J. M. Hobbs, V. Sundaram, M. Swaminathan, G. White, "Characterization of Thin Film Polymer Dielectrics," Georgia Tech Invention Disclosure # 2560, September 2001.

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APPENDIX A: PROCESS FLOW

Figure A.1 [11] shows the fabrication process flow for two metal layer organic-based System-on-Package (SOP) lamination technology at the Packaging Research Center (PRC), Georgia Tech. A 40 mil or 28 mil thick, copper-cladded (9μm or 18μm) FR-4 organic substrate (epoxy-glass fiber composite) is used in this process. A 15μm thick photoresist dry film (Du Pont, Riston 206) is laminated on the substrate (@75°C) using vacuum pressure type laminator and patterned. The first conductor layer is then patterned by selectively etching the copper layer in ammonium hydroxide. The photoresist is then stripped off and a thin dielectric laminate dry film is laminated using the same method to insulate the conductor layers; the following films were chosen for this work: DuPont's Vialux™, Asahi PPE™ and Rogers Zyvex™. For photodefinable materials like Vialux™, photo-via openings were then formed through exposure to UV light, pre-baking in oven at 110°C for 1hr, developing in gamma-butyro lactone (GBL), and curing the dielectric polymer at 150°C (the maximum temperature used in this process) for 1.5hr. When processing materials like PPE™ and Zyvex™ that are not photo-sensitive, the vias are laser ablated. The vias and the 17μm-20μm thick upper conductor lines are then formed through electroless plating of copper seed layer followed by electrolytic copper plating into a 15μm thick photoresist mold made through lamination. The thickness of the copper on all layers is significantly larger than that in a standard silicon process, MCM-D process or LTCC process. This increased thickness helps decrease the series resistance in components such as transmission lines, inductors, and capacitors. For electroless copper plating, the surface of dielectric polymer is catalyzed through such process steps as swell, etch, neutralize, pre-catalyst, and catalyst. After plating, the photoresist is stripped off

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and the copper seed layer was wet-etched in micro-etch solution. Conductor profiles that are common in the SBU process are shown in Figure A.20 and Figure A.3. Having knowledge of the conductor profiles is imperative in almost all aspects of design. One also needs to characterize the variations in the thickness of the dry film across the extent of the boards. As seen in Figure A.2 and Figure A.3 the planarization of the film after all processes is very uniform; however, as seen in Figure A.2 the film sandwiched between two metal layers is much thinner than where it not sandwiched. If the metal density on the lower metal layer is not uniform and the film is thinner than a certain minimum [12], then these two thicknesses can vary across the extent of large area panels. If this parameter is not controlled or well characterized, it can lead to erroneous models and faulty simulation results.

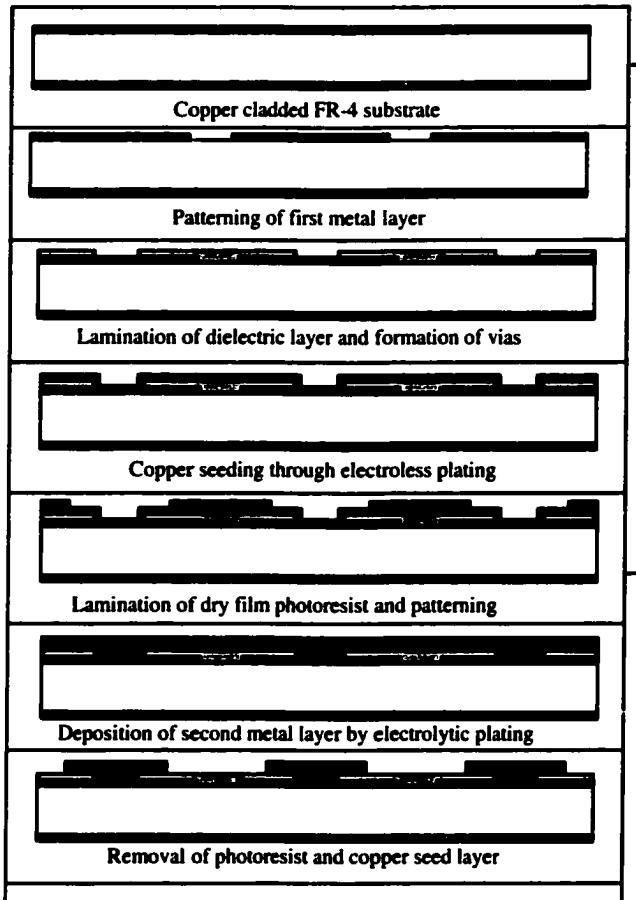

Figure A.1: Process flow for the low-temperature laminate SOP process.

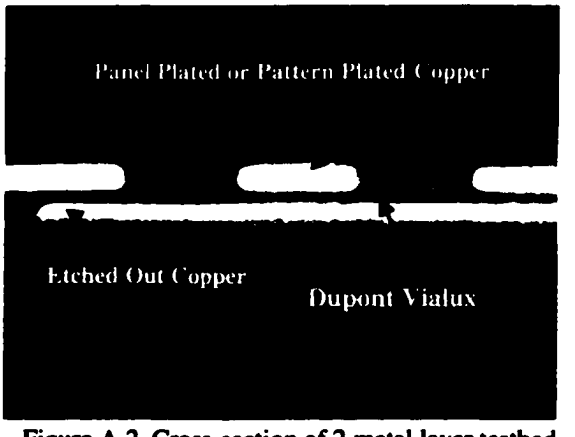

Figure A.2. Cross-section of 2 metal layer testbed (The core is Fr4 and the thin film is Vialux™)

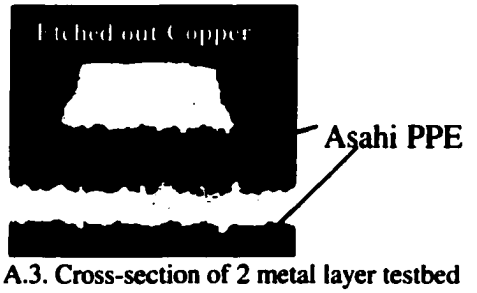

Figure A.3. Cross-section of 2 metal layer testbed (The core is Fr4 and the thin film is PPE™)

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APPENDIX B: DESIGN RULES

Having developed a good understanding of the process and possible variations, the first step taken was to establish design rules that ensure low tolerances, repeatability and manufacturability followed by the electrical characterization of each laminate.

1. Line Widths and Line-to-Line Spacing: A minimum line width of 3 mils with 3 mils line-to-line spacing was allowed for each metal layer.
2. Conductor Thickness: A maximum metal thickness equal to the thickness of the photo-resist used guarantees uniform conductor profiles. The width at the top and bottom is seen to differ by less than or equal to 0.3mils for plated or etched copper lines. For designs, which require less than 2 % tolerances, having line widths greater than 6 mils ensures little or no effect of line profiles on the inductance or capacitance of that line up to high frequencies. This rule was established after simulations of various configurations in ANSOFT2D [13], which is a 2D finite element (FEM) based electromagnetic (EM) tool.
3. Via Sizes: A minimum diameter size for the microvias equal to twice the build-up layer thickness ensures good via reliability. Since the maximum thickness of the dielectric films used in this work is 2 mils, the vias are all less than or equal to 4mils. When simulated in SONNET [14], which is a method-of-moments (MOM) based commercial tool, it is seen that the parasitic inductance added by the microvias is less than or equal to 0.1nH.
4. Metal Patterning on Buried Layers: The metal density for the buried layers determines the flow and fill of the build-up material. For characterization of materials, it is essential that the dielectric thickness is uniform over the extent of

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the board. The easiest way to this is to come up with characterization structures that do not require any patterning on the metal layer below the build-up layer. For devices, which may have one or more capacitive elements and require uniform and predictable dielectric thickness, a maximum metal thickness for the buried metal layers of 1/3rd the dielectric layer thickness is allowable.

5. Designs, which required less than 2% tolerances for all sub-components such as inductors, capacitors and transmission lines, e.g. filters, should be implemented using just two metal layers.

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