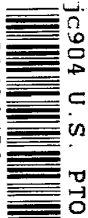


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UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR 1.53(b))	Attorney Docket No.	17625-0038
	Named Inventor(s)	White, et al.
	Title	Integrated Passive Devices Fabricated Utilizing Multi-Layer, Organic Laminates
	Express Mail Label No.	EV048621803US

APPLICATION ELEMENTS	ADDRESS TO: Assistant Commissioner for Patents Box Patent Application Washington, DC 20231
1. ☒ Fee Transmittal Form <i>(Submit an original, and a duplicate for fee processing)</i> 2. ☒ Applicant claims small entity status. See 37 CFR 1.27. 3. ☒ Specification, Claims, and Abstract Total Pages 37 4. ☒ Drawings Total Sheets 12 5. Oath or Declaration Total Pages 3 a. ☒ Newly executed (original or copy) b. ☐ Copy from prior application (37 CFR 1.63(d)). <i>(for continuation/divisional with Box 19 completed)</i> (i) ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b). 6. ☐ Incorporation by Reference <i>(usable if Box 5b is checked)</i> The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 5b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein. 7. ☐ Nonpublication Request Under 35 U.S.C. 122(b)(2)(B)(i). ☐ Form PTO/SB/35 8. ☐ Application Data Sheet. See 37 CFR 1.76 9. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix)	10. ☐ Nucleotide and/or Amino Acid Sequence Submission <i>(if applicable, all necessary)</i> a. ☐ Computer Readable Form (CRF) b. ☐ Specification Sequence Listing on: i. ☐ CD-ROM or CD-R (2 copies); or ii. ☐ paper c. ☐ Statement verifying identity of above copies 11. ☒ Assignment: a. ☒ Assignment Papers (cover sheet & document(s)) b. ☐ Assignment is of record in parent application No. 12. ☐ 37 CFR 3.73(b) Statement <i>(when there is an assignee)</i> ☐ Power of Attorney by assignee 13. ☐ English Translation Document <i>(if applicable)</i> 14. ☒ Information Disclosure Statement (IDS) PTO- 1449 ☒ Copies of IDS Citations (62 references) 15. ☐ Preliminary Amendment 16. ☒ Return Receipt Postcard (MPEP 503) <i>(Should be specifically itemized)</i> 17. ☐ Certified Copy of Priority Document(s) 18. ☐ Other:
19. If a CONTINUING APPLICATION , check appropriate box and supply the requisite information and in a preliminary amendment, or in an Application Date Sheet under 37 CFR 1.76: ☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: Prior application information: Examiner: Group Art Unit: Recite complete dependency back to first parent application:	
20. CORRESPONDENCE ADDRESS: Malvern U. Griffin III SUTHERLAND ASBILL & BRENNAN LLP 999 Peachtree Street, NE Atlanta, Georgia 30309-3996 By: <u>Malvern U. Griffin III</u> Reg. No. 38,899 Date: March 28, 2003 Telephone: 404-853-8000 Facsimile: 404-853-8233	

I hereby certify that this correspondence is being deposited with the United States Postal Service in an Express Mail envelope
(EV048621803US) addressed to: Assistant Commissioner for Patents, Washington, D.C. this 28th day of March 2003.

Malvern U. Griffin III
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PATENT TRADEMARK OFFICE

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EX1040 / Page 2 of 165
Murata Manufacturing Co., Ltd.

FEE TRANSMITTAL

Attorney Docket No. 17625-0038

This sheet accompanies a patent application transmittal for the following application:

Inventor(s): White, et al.

Filing Date: March 28, 2003

Serial No.:

Title: Integrated Passive Devices Fabricated Utilizing Multi-Layer, Organic Laminates

The filing fee is calculated as shown below:

1. FILING FEE:

FOR:	SMALL ENTITY		LARGE ENTITY	
	FEE	FEE PAID	FEE	FEE PAID
☒ UTILITY FILING FEE	\$375	\$375	\$750	
☐ DESIGN FILING FEE	\$165		\$330	
☐ PLANT FILING FEE	\$260		\$520	
☐ REISSUE FILING FEE	\$375		\$750	
☐ PROVISIONAL FILING FEE	\$80		\$160	
SUBTOTAL (1)		\$375		

2. CLAIMS:

SMALL ENTITY				LARGE ENTITY		
FOR:	NO. FILED	NO. EXTRA	RATE	FEE	RATE	FEE
TOTAL CLAIMS	36 - 20 =	16	x 9 =	\$144	x 18 =	
INDEP. CLAIMS	4 - 3 =	1	x 42 =	42	x 84 =	
☐ MULTIPLE DEPENDENT CLAIM PRESENTED			+140 =		+280 =	
SUBTOTAL ()				\$186		

3. ADDITIONAL FEES:

FOR:	SMALL ENTITY		LARGE ENTITY	
	FEE	FEE PAID	FEE	FEE PAID
☐ LATE FILING, FEE OR OATH	\$65		\$130	
☐ NON-ENGLISH SPECIFICATION	\$130		\$130	
☐ OTHER				
SUBTOTAL (3)		0		

TOTAL FILING FEES: \$561

A check is enclosed for the total amount: \$561

☒ Charge any additional fees required to Deposit Account 19-5029.

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10 INTEGRATED PASSIVE DEVICES FABRICATED
UTILIZING MULTI-LAYER, ORGANIC LAMINATES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims benefit of co-pending U.S. Provisional
15 Application No. 60/391,742, filed June 26, 2002, which is entirely incorporated herein
by reference. In addition, this application is related to the following co-pending,
commonly assigned U.S. applications, each of which is entirely incorporated herein
by reference: "Methods for Fabricating Three-Dimensional All Organic Interconnect
Structures" filed March 28, 2003, and accorded Application No. _____; and
20 "Stand-Alone Organic-Based Passive Devices" filed March 28, 2003, and accorded
Application No. _____.

BACKGROUND OF THE INVENTION

25 I. Field of the Invention

[0002] The present invention generally relates to the fabrication of integrated
passive devices, and more particularly, to topologies for passive filters fabricated
utilizing organic laminates.

30 II. Description of Related Art

[0003] Radio frequency (RF) filters are generally used to remove the out-of-
band energy and perform rejection of image-band signals. The design of RF filters in

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Additionally, the multilayer ceramic filters come with the disadvantage of higher costs due to the non-traditional processes used in making the multilayer ceramic filters. An example of higher costs is in the inherent higher temperatures of processing (e.g., >800°C) compared to organic laminate processing (e.g., <230°C).

- 5 Additionally, one can leverage the economies of scale when using organic laminate processing which can handle batch processing of 18"x12" panels as compared to a nominal maximum of 8"x8" for LTCC and 6"x6" for MLC technologies.

- [0006] While realizing the problems with ceramic and advantages with
10 organic laminate processing in terms of costs, filters fabricated in organic substrates generally have not delivered the performance of cavity filters or multilayer ceramic filters. The bandwidths realized by the organic filters have not been small enough and the insertion loss too high for even large bandwidth applications. See, for example, Son, M.H., Kim, Y.J., Lee, S.S., "Low-Cost Realization of ISM Band Pass Filters
15 Using Integrated Compline Structures," *2000 Asia-Pacific Microwave Conference*, pp. 1294 –1297. [2] G. Hong and M. Lancaster, *Microstrip Filtes for RF/Microwave Applications Design*, Wiley, June 2001.

- [0007] Thus, there is an unsatisfied need in the industry for a high frequency,
20 low loss, inexpensive bandpass filter having a relatively small footprint.

SUMMARY OF THE INVENTION

- [0008] The present invention comprises integrated passive devices incorporating topologies suitable for organic processes and that perform filtering
25 using lower-cost, lower-temperature, higher performing organic processing. These filters can meet the specifications of cavity filters, MLC and LTCC filters with equivalent or better performance in smaller or similar footprints. In particular, the present invention comprises methods and topologies of making devices that can be directly integrated in multilayer boards or packaged as a surface mount device (SMD)
30 or ball grid array (BGA)/ chip scale package (CSP) device.

[0009] In accordance with an embodiment of the present invention, a small, thin plane type narrow-band bandpass filter to be used for a portable telephone, cell phones, wireless infrastructure, WLAN, and the like, includes a plurality of end short-circuited hybrid CPW/stripline/microstrip meander/straight inductors or transmission line resonators formed close to one another on a first organic dielectric substrate or on multiple dielectric substrates interconnected by via connections, and in proximity to one another in order to be directly magnetically coupled to each other.

[0010] In circumstances where the inductors do not provide the desired parasitic capacitance, each inductor may be connected to separate shunted parallel plate (i.e., two or more plates) open-ended microstrip stub capacitors, which together form the resonators. In circumstances where the magnetic coupling between the inductors does not provide the desired coupling, the resonators can be electrically coupled further using a series parallel plate/inter-digital capacitor and/or an inductor. The resonators can also be coupled magnetically and capacitively. In addition, a parallel plate/inter-digital capacitor, an inductor or a transmission line can be used on either side of the two resonators at the input and output terminals of the device for impedance matching purposes.

[0011] In accordance with an aspect of the present invention, the dielectric material(s) used to achieve capacitance is virtually any low cost, high performance organic, such as liquid crystalline polymer (LCP) or polyphenyl ether (PPE), in a laminate or thin film. The dielectric constant, loss and thickness of the organic laminate is imperative to achieve the range of capacitances, and density needed for such applications. For example, the dielectric constant should be between approximately 2 and 100, the loss should be less than approximately 0.01, and the thickness should be between approximately 10 microns and 1000 microns. The present invention is capable of providing a range(s) of capacitances by sandwiching thin organic dielectrics (e.g., approximately less than 50 microns in thickness) with reasonable relative dielectric constants (e.g., approximately 2 to 100). The capacitance range available is from picofarads to femptofarads.

[0012] If the dielectric is too lossy for the purposes of integrating capacitors, then discrete capacitors can be used to compensate for the loss in the dielectric. This can be a cost-effective solution when compared to using multilayer ceramic, LTCC or cavity filters. The performance, however, may be dependent on the performance of the discrete capacitors.

[0013] The present invention further comprises co-planar waveguide (CPW)-type topologies, which make it easy to add grounded/shunted elements. The use of CPW topologies provides for additional paths for excess currents to sink from areas of current concentration, thereby reducing coupling of devices magnetically and electrically. Additionally, CPW topologies allow for a reference voltage in proximity to the signal carrying elements, which enables components like diplexers and duplexers that need many more inductors and capacitors than what is required in a bandpass filter, low pass filter and high pass filter.

[0014] In accordance with an aspect of the present invention, an all organic filter in accordance with the present invention can be integrated in a multilayer board because both use organic technology. A board typically is used as a carrier of such devices, which are mounted on the board in SMD or BGA/CSP configuration. However, if desired, a filter in accordance with the present invention using organic materials can be constructed in a stand alone SMD or BGA/CSP form to make it mountable on a multilayer board.

[0015] The design of the filters is accomplished in such a way that the final packaging of the device in stand-alone form or as an integrated device is done by sandwiching one or more thicker organic cores with metal on one or more sides to provide shielding from interferes and radiation.

[0016] In accordance with the present invention, multi-layer filters using any suitable low cost, high performance organic (e.g., LCP and PPE) with the topology

and layouts described herein can achieve the performance of not only the multilayer ceramic filters with the same form factors, but they also emulate the performance of cavity filter components in about one-tenth the volume and monoblock filters in about half the volume. Although such filter designs can be achieved in two layers, the process and design of the present invention allows for multiple layer (>2 layer) capacitors and inductors integrated to form even more compact devices having higher integration.

[0017] For example, a two pole filter constructed in accordance with the present invention using two metal layers on two sides of a thin laminate substrate and then shielded on both sides has a footprint of 3x3mm, a height of 1.5mm and emulates the performance of a 4x5mm monoblock filter having a height of 1.8mm. On a 12"x12" substrate, it is possible to fabricate approximately 6500 such components with filter-to-filter spacing included, which illustrates its cost effectiveness. A filter according to the present invention requires just two patterned metal layers because of the CPW-type topology, as compared to the multi-layers in ceramic filters or molded cavity filters. This also reduces design time, processing time, and fabrication cost as compared to ceramic filters or molded cavity filters.

[0018] While the present invention is disclosed in the context of filters and resonator elements, the teaching of the present invention can be readily applied to other integrated passive devices (IPDs) such as diplexers, duplexers, baluns, power combiners, band-stop/band elimination filters and power dividers, low-pass filters and high-pass filters. All of these different components only comprise inductors, capacitors and/or transmission lines in topologies only slightly different from the bandpass filters disclosed herein.

[0019] Other systems, methods, features, and advantages of the present invention will be or become apparent to one with skill in the art upon examination of the following drawings and detailed description. It is intended that all such additional systems, methods, features, and advantages be included within this description, be

within the scope of the present invention, and be protected by the accompanying claims.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S)

- 5 [0020] Having thus described the invention in general terms, reference will now be made to the accompanying drawings, which are not necessarily drawn to scale, and wherein:
- [0021] FIG. 1A is a first equivalent circuit diagram for explaining the operation of the dielectric filters shown in FIGS. 2, 3 and 4.
- 10 [0022] FIG. 1B is a second equivalent circuit diagram for explaining the operation of the dielectric filter of FIG. 1A using transmission lines or inductor resonator elements.
- [0023] FIGS. 2A-2C show several views of a first organic dielectric filter according to an embodiment of the present invention.
- 15 [0024] FIGS. 3A-3C show several views of a second organic dielectric filter according to an embodiment of the present invention.
- [0025] FIGS. 4A-4B show several views of a third organic dielectric filter according to an embodiment of the present invention.
- [0026] FIG. 5 illustrates a fabrication methodology for an organic dielectric
20 filter according to the present invention, such as the first organic dielectric filter of FIGS. 2A-2C.
- [0027] FIG. 6 illustrates a fabrication methodology for an organic dielectric filter according to the present invention, such as the organic dielectric filter of FIGS. 3A-3C.
- 25 [0028] FIG. 7 is an X-ray from a top plan view of an organic bandpass filter in accordance with an embodiment of the present invention.

[0029] FIG. 8 is an X-ray from a side perspective view of the organic bandpass filter of FIG. 7.

[0030] FIG. 9 is a graphical representation of a model to hardware correlation for the organic bandpass filter of FIG. 7.

5 [0031] FIG. 10 is a picture from a top plan view of a BGA style organic filter, in accordance with an embodiment of the present invention.

[0032] FIG. 11 is a graphical representation of measured and modeled data for the BGA style organic filter in FIG. 10.

10 [0033] FIG. 12 is a picture from a top plan view of an organic dielectric filter that includes SMD capacitors in accordance with an embodiment of the present invention.

[0034] FIG 13 is a graphical representation of a model to hardware correlation for the organic dielectric filter in FIG.12.

15 DETAILED DESCRIPTION

[0035] The present inventions now will be described more fully hereinafter with reference to the accompanying drawings, in which some, but not all embodiments of the invention are shown. Indeed, these inventions may be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will satisfy applicable legal requirements. Like numbers refer to like elements throughout.

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[0036] The operation of a filter in accordance with the present invention is explained below with reference to the bandpass filter 10 of FIG. 1A. However, it will be appreciated by those of ordinary skill in the art that the teachings of the present invention readily apply to other integrated passive devices. Accordingly, the scope of the present invention is not limited to bandpass filters, but is inclusive of other devices such as but not limited to diplexer, duplexer, multiplexer, baluns, power

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combiner, band-stop/band elimination filter and power divider low-pass filter and high-pass filter.

[0037] With reference to the figures, FIG. 1A is an equivalent circuit diagram of a dielectric bandpass filter 10 in accordance with the present invention. In FIG. 1A, inductors 12, 14 cooperate with their corresponding capacitor 16, 18, respectively, to form resonators 20, 22, respectively. The inductors 12, 14 correspond to the stripline or CPW/strip-line or CPW/microstrip inductors discussed below with reference to FIGS. 2-4. The capacitors 16 and 18, respectively, correspond to the capacitors formed on the same layer as inductors 12 and 14 or by using discrete capacitors. The capacitor 24 corresponds to the capacitor formed for the purposes of inter-resonator coupling. In FIG. 1A, capacitors 26 and 28, respectively, provide matching to the desired impedances at the input and output. In addition, M is the magnetic coupling between the inductors 12 and 14. The inductances of inductors 12 and 14 could also represent equivalent inductance components of the resonators, and capacitances of capacitors 16 and 18 could represent capacitance components of the resonators. While the circuit topology shown in FIG. 1A depicts one embodiment of a two pole filter, and an additional pole can be attained by the mutual inductance between inductors 12, 14 and the capacitor 24. In additional, resonators may be added with the required coupling elements by adding more inductors and capacitors in various configurations to achieve transfer characteristics that emulate such responses as first order, second order to nth order butterworth, chebychev, elliptic, blinkoff, symmetric, asymmetric, notch added filters using topologies such as nodal capacitor coupled, nodal-inductor coupled, shunt-input geometry, input geometry or mesh capacitor coupled.

[0038] The stopband characteristics of a filter is a prime factor in determining the isolation between the transmitting and receiving paths in duplexer designs. It is well known that the stopband rejection may be enhanced, either by increasing the number of resonators as mentioned earlier, or by adding transmission zeros.

[0039] FIG. 1B is an alternative equivalent circuit diagram 10 of a dielectric filter using transmission lines or inductor resonator elements, wherein the inductors 112 resonate at a desired center frequency. The physical parameters of the circuit 110, such as the number of turns, length of conductor, outer and inner diameter, can be altered to resonate the inductor 112 at the desired frequency. This reduces the number of components required to achieve a filtering function by removing the need for capacitors of the resonators. However, a disadvantage is the increase in length of the metallization to increase the capacitance, though the increased inductance could increase loss in the circuit. If the inductor element becomes too large or too lossy, then it may be desirable to use an alternative circuit design, such as that illustrated in FIG. 1A. It should be noted that in the circuits of FIG. 1A and FIG. 1B, the coupling between the components can be achieved by magnetic coupling, electric coupling or a combination thereof.

[0040] Illustrative physical layouts of dielectric filters in accordance with the equivalent circuit diagram of FIG. 1A are depicted in FIGS. 2-4. The dielectric filters of FIGS. 2-4 have a two-pole structure and an additional pole attained by the mutual inductance and the capacitor 24 according to the equivalent circuit diagram shown in FIG. 1A.

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[0041] With general reference to FIGS. 2A-2C, illustrated is a surface mounted device (SMD) embodiment of the filter illustrated by the circuit of FIG. 1A in accordance with the present invention. Specifically, the organic bandpass filter 200 comprises inductors 212 and 214, which are meandering inductors formed close to each other on an organic dielectric layer 236 (which can be a thin laminate such as LCP or PPE, but is not limited to these) and is preferably configured as either a shorted hybrid CPW-stripline (where lines that form meandering inductors 212 and 214 are connected to a coplanar ground, that is, in-built shielding 230), or a stripline in the presence of coplanar in-built shielding 230 and additional grounds 248 and 250

that are connected to the plated through holes 232 and/or external shield electrodes 234.

[0042] Since these inductors are very close to each other, the magnetic coupling between these filters, represented by M in FIG. 1A, can increase the pass bandwidth of the filter, thereby decreasing its performance. However, an inter-resonator parallel plate coupling capacitor 224, (with or without the coplanar in-built shielding 230) formed using two disconnected metal plates (one plate formed using patterning conductive layer 238 and the other plate formed using patterned conductive layer 240) and shown as capacitor plates 224a, 224b is provided. The capacitor plates 224a, 224b sandwich the first organic dielectric layer 236 in such a manner that the each plate of the inter-resonator coupling capacitor electrode is connected to separate resonators which helps compensate the effect of the magnetic coupling and helps make very compact filters. The center capacitance can be as small as femptoFarads or as large as picoFarads for achieving the specified bandwidths. The smaller capacitance helps reduce the bandwidth. Additionally, capacitor 224 in parallel with the mutual inductance equivalent gives a pole in the lower band or upper band.

[0043] The bottom plate formed by the conductive layer 240 connects to inductor 212 using one or more microvias in the organic dielectric layer 236, such as the vias 244 with pads 246 for landing and capturing the via. First and second shield electrodes 248, 250 formed respectively on the organic core layers 252, 254, wherein the core layer 252 and 254 are disposed so as to sandwich the organic dielectric layer 236 there between. A first resonator 260 formed by inductor 212 and capacitor 216 and a second resonator 262 formed by inductor 214 and capacitor 218 are electrically coupled to each other through the parallel plate capacitor 224, whereby an inter-resonator coupling is effected in combination with said magnetic coupling and electric coupling.

[0044] In a dielectric filter according to the present invention, where the inductors do not provide the needed capacitance in the desired length, the inductors

212, 214 can be connected in similar fashion as the capacitor 224 to separate grounded/shunted parallel plates 216a and 218a, respectively, of capacitors 216 and 218, respectively, using the same first organic dielectric layer 236 as the sandwiched dielectric, which then together form the resonator pairs 260, 262.

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[0045] The equivalent inductance L obtained with one of the meander inductors, 212, 214, and the equivalent capacitance C due to one of the capacitors 216, 218, resonates approximately at frequency Fo, the center frequency of the filter, as defined by Equation (1) below:

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$$\text{whereby } F_o \sim \sqrt{1/(LC)} \quad (1)$$

The capacitor plates 216a and 218a have a corresponding ground plate 217 on the opposite surface of the organic dielectric layer 236. Having a common plate does
15 cause coupling between the capacitors which has to be accounted for during the design by including it as the mutual inductance between the parasitic inductance of each capacitor 216, 218. This coupling can be used to achieve further poles; however if the coupling causes problems in the passband during the synthesis stage it could be reduced by either dividing plate 217 into separate plates or by adding several vias on
20 pads 274 that connect plate 217 to in-built shielding 230 on the side of the inductors 212 and 214, thereby helping excess currents to sink and thereby reducing coupling between components.

[0046] In addition, parallel plate/interdigital capacitors 226 and 228, can be
25 used on either side of the first and last resonator elements 260, 262 at the input and output terminals of the device for impedance matching purposes. Alternatively, inductors or transmission lines or a combination of capacitor(s), inductor(s) and transmission line(s) can be utilized, as desired. If capacitors 226, 228 are used for matching purposes, it follows the center capacitance is that of capacitor 224 in terms

of the nominal capacitances required, that is, the capacitance from capacitor 226 and capacitor 228 are proportional to capacitor 224.

[0047] A dielectric filter according to the embodiment of the present invention
 5 illustrated in FIGS. 2A-2C can comprise at least two external shield electrodes 234 respectively formed on different side surfaces of the laminated structure, which comprises at least the organic dielectric layer 252, 236, 254, and that are connected to the shield electrodes 248 and 250. This may or may not be desired for shielding purposes in a CPW topology, wherein the use of plated through holes 232 on the four
 10 corners is sufficient. Utilizing the plated through holes 232 may save additional room required for the external shield electrodes 234 and also may save the processing cost involved. However, in stripline and microstrip filter topologies, plated through holes 232 and external shield electrodes 234 together provide the connection for the shorted inductors/resonators and capacitors at any point along the respective sides.
 15 Alternatively, the CPW topology with coplanar in-built shielding 230 on the same plane of the first dielectric layer provides the shielding internally, and provides for the ground connectivity to the resonators/inductors and capacitors. However, in general, in more noisy environments it may be preferred to also have the external ground electrodes.

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[0048] The dielectric filter 200 also comprises an external input terminal electrode 264 and an external output terminal electrode 266 which are formed on one side surface of a laminated body comprising at least dielectric sheets 252, 236, 254, and an external ground electrode, (such as shield electrodes 248, 250, through holes
 25 232 or side shield electrodes 234) formed between said external input and output terminal electrodes 264, 266 on one side surface.

[0049] The shield electrodes 248 and 250 formed on the dielectric core layers 252 and 254, respectively, are preferably of the shape and patterned to leave room for
 30 the landing terminals of input and output terminal electrodes 264 and 266. For

purposes of illustrating the present invention, the shield electrodes 248, 250 are shown in FIGS. 2B and 2C, but not 2A.

[0050] The first organic dielectric layer 236 can comprise single side copper LCP laminate or the like, such as PPE, N6000, epoxy based N4000-13, or any other suitable low loss dielectric.

[0051] The protective layers 270, 272 are formed on shield electrodes 248, 250 opposite dielectric core layers 252, 254, respectively, to protect the structure from environmental affects such as oxidation and also to create a pattern for solder to flow on to the input output terminals 264 and 266 and ground pads formed by plated through holes 232. The protective layers 270, 272 may comprise a solder mask, or in more demanding applications, with higher tolerances, other materials such as prepreg or LCP may be desired. For purposes of illustrating the present invention, the protective layers 270, 272 are shown in FIGS. 2A and 2B, but not 2C.

[0052] In the dielectric filter according to the present invention, as illustrated in FIGS. 2A-2C, an initial step to making a connection between devices using vias 244 is done by drilling through holes (as small in diameters as the thickness of the dielectric used) through the LCP layer (or any other appropriate organic dielectric) and copper layer. Then both sides of LCP copper laminate are metallized, such as by electroless or vacuum deposited copper. Copper is then electroplated on both sides of laminate to form the metallized patterns 238, 240 on the organic dielectric layer 236. The copper is then printed and etched to define the key filter components.

[0053] In the dielectric filter according to the embodiment illustrated in FIGS. 2A-2C, the dielectric core layers 252, 254 can be laminate LCP or appropriate dielectric with generally larger thickness than the first substrate and aluminum, copper, Molybdenum metal (for high power applications) on both sides of filter to a given thickness to encapsulate components. All metals are preferably electroplate and

etched and patterned on top and bottom of the device to leave space for signal input and output.

[0054] In a dielectric filter according to the embodiment illustrated in FIGS. 2A-2C, the side wall ground shield electrodes 232, 234 can be fabricated, if desired, by single or multiple connected drilled and plated through holes or using a saw cutting device and then connected via electroless or sputter seeded copper in through hole. The copper can be electroplated in the through hole and on the surface. The copper can then be printed and etched to form SMD connection. The process flow for a two layer plus the packaging of the SMD device is explained in greater detail in connection with FIG. 5.

[0055] With reference to FIGS. 3A-3C, illustrated, is a BGA/CSP embodiment of an organic bandpass filter 300 in accordance with the present invention. Essentially, all of the internal structure in the filter depicted in FIGS. 2A-2C and FIGS. 3A-3C are similar except the packaging is different, and thereby, the means by which you package it. For example, in FIGS. 3A-3C the thin laminate (e.g., the organic dielectric layer 336) is not packaged between two thick cores, but is packaged with one core layer 354 on one side and a first protective layer 370 on the opposite side substrate 336. The opposite side of the thicker core 354 is metallized to form a shield electrode 350, and a second protective layer 372 is disposed over the shield electrode 350. The protective layers may comprise a solder mask, or in more demanding applications, with higher tolerances, other materials such as prepreg or LCP may be desired.

[0056] This packaging of filter 300 renders a microstrip or CPW/microstrip filter device with only shield electrode 350. Instead of using through holes to connect the device input/output and ground terminals, solder balls 380 are utilized. Side wall ground shield electrodes 334 are used to connect the in-built shielding electrodes 330 and shield electrode 350 and, if desired, to solder balls 380.

[0057] Alternatively, this could be done by plated through holes, if provided. As discussed above, having both plated through holes 332 and side wall shield electrodes 334 is not typically necessary, and generally they can be utilized in the alternative of one another. For purposes of illustrating the present invention, side wall grounded shield electrodes 334 are shown in FIG. 3A-3C. The solder balls 382 connect the input and output terminals to the bandpass filter. The solder balls and the packaging is constructed using the methodology provided below in connection with FIG. 6. The protective layer 370 (also known as a passivation layer mask, solder mask, bondply layer or low temperature thermoset, thermopolymer material compound to inner laminate) may be utilized to provide openings for the solder balls, as well known in the art.

[0058] With reference to FIGS. 4A-4B, illustrated is an embodiment of a filter device 400 in accordance with the present invention, which utilizes discrete capacitors 402 and external shielded formed by a metallic case or cap 404. Essentially, all internal structure in FIGS. 2A-2C and FIG. 3A-3C are similar except the packaging is different in the embodiment of FIGS. 4A-4B, and thereby the means by which you package it. For example, in FIGS. 4A-4C, an organic dielectric layer 436 (e.g., a thin laminate substrate) is not packaged between two thick cores, but only one core layer 454 on one side, wherein a shielding electrode 450 is metallized on the opposite side of the core layer 454. On the other side of the organic dielectric layer 436 is a metallic cap 404 with the appropriate height, which is used to provide a second ground reference. The organic dielectric layer 436 is metallized on opposing surfaces by patterned conductive layers 438 and 440, which are electrically connected by at least microvias in layer 436, as discussed with regard to the embodiments of FIGS. 2 and 3. Instead of using a thicker core on both sides of the substrate 436, this embodiment uses a core layer on one side and air as a dielectric on the other. This renders itself into a stripline or CPW/stripline device. Through holes are used to connect only the core metal to the internal metallic structure whereas the metallic cap 404 is connected using solder connections to the relative terminals. The metallic cap 404 can have openings where needed for the input and output terminals. It is

important to note that the embodiment is not restricted to using discrete capacitors. The capacitors shown in FIGS. 4A-4B can also be embedded in the substrate, if needed, as discussed previously.

5 [0059] The following are examples of various embodiments of the present invention, wherein each illustrative embodiments discloses several aspects of the invention.

II. Illustrative Methods for Fabricating Stand Alone Filters

10 [0060] An illustrative process for fabricating an LCP based IPD, such as the filter illustrated in FIGS. 2A-2C, configured as a surface mount device (SMD) in accordance with an embodiment of the present invention is now described with reference generally to FIG. 5. Initially, a starting material is selected, which is preferably a reinforced or non-reinforced LCP laminate that can be unclad, or clad

15 with copper foil on one or both sides of the LCP, as illustrated in Step 1. Alternate materials include other low loss organic laminates like PPE, PTFE composites, hydrocarbon ceramic composites, BT resin composites (e.g., Speedboard C), and thermosets (e.g., Hitachi MCL-LX-67F). Next, through vias are drilled through the LCP or other laminate and the layers of copper, as illustrated in Step 2. These

20 microvias can be drilled with mechanical drilling, laser drilling or other suitable methods known to those skilled in the art.

[0061] Steps 3 and 4 involve the metallization of the through vias and laminate. In additive, semi-additive, or subtractive processes starting with unclad or

25 copper clad LCP or other laminates, both sides of the LCP or other laminate and the vias are seeded using electroless plated, vacuum deposited copper or another deposition methods to form a continuous copper film. To achieve the target metal thickness for the device, electrolytic plating is done to build the copper on both sides of the laminate and in the vias in a single step. The circuit definition for the filter

30 component can be done using subtractive, semi-additive or fully additive processes

with panel or pattern electroplating of the copper followed by print and etch steps to define the filter circuitry, as illustrated in Step 5.

[0062] The fabricated device circuits are then packaged using vacuum or non-
5 vacuum lamination of LCP or alternate laminate materials as detailed above in
connection with Step 1, and/or Al, Cu, Mo metal (for high power applications) on
both sides of the filter to provide sufficient thickness to encapsulate components, as
illustrated in Step 6. The internal and external metal layers are connected, as needed,
using plated through holes that can be drilled mechanically or with laser, photo, or
10 plasma processes to provide signal and ground connections and SMD terminals, as
illustrated in Step 7. The two edges of the device without the through hole can also
slotted using mechanical drill/rout/mill, laser cutting, or sawing processes to provide
for additional shielding of the device during subsequent metallization. The drilled
through holes and shielding slots are seeded with electroless plated or sputter/vacuum
15 deposited copper to provide a bus layer in substantially the same manner as described
above in connection with Step 3, as illustrated in Step 8.

[0063] With reference to Steps 9, 10, and 11, the final metal thickness for the
outer layers is built up by electroplated copper in the through holes, shielding slots,
20 and on the top and bottom surfaces. Subtractive, semi-additive, or additive processes
may be used to define the outerlayer ground circuits and SMD terminals for
connection, with print and etch processing of the copper, as described above in
connection with Steps 4 and 5. The device is then finished with the addition of
terminal metals appropriate for SMD assembly and soldering processes. These
25 finishing metals on the device terminals are common plated metals or alloys like
electroless Ni-Au, immersion tin, immersion silver, electroplated Ni-Au, solder
(HASL), or organic finishes (OSPs) and the choice depends on the intended
application.

30 [0064] The fully fabricated wafer is then singulated into individual filter
components. The singulation can be done using high speed dicing saws or alternate

methods such as punching or routing/milling. An advantage of this fabrication process is the ability to fully electrical test the components either before or after singulation.

5 [0065] Another illustrative process for fabricating an LCP based IPD, such as the filter illustrated in FIGS. 3A-3C, configured as a ball grid array (BGA) or chip scale package (CSP) in accordance with an embodiment of the present invention is now described with reference generally to FIG. 6. Initially, a starting material is selected, preferably a reinforced or non-reinforced LCP laminate that can be unclad, or clad with copper foil on one or both sides of the LCP, as illustrated in Step 1. Alternate materials include other low loss organic laminates like PPE, PTFE composites, hydrocarbon ceramic composites, BT resin composites (e.g., Speedboard C), and thermosets (e.g., Hitachi MCL-LX-67F). Next, through vias are drilled through the LCP or other laminate and the layers of copper, as illustrated in Step 2. 10 The microvias can be drilled with mechanical drilling, laser drilling or other suitable methods known to those skilled in the art.

[0066] Steps 3 and 4 involve the metallization of the through vias and laminate. In additive, semi-additive, or subtractive processes starting with unclad or copper clad LCP or other laminates, both sides of the LCP or other laminate and the vias are seeded using electroless plated, vacuum deposited copper or other common deposition methods to form a continuous copper film. To achieve the target metal thickness for the device, electrolytic plating is done to build the copper on both sides of the laminate and in the vias in a single step. The circuit definition for the filter component can be done using subtractive, semi-additive or fully additive processes with panel or pattern electroplating of copper followed by print and etch steps to define the filter circuitry, as illustrated in Step 5.

[0067] The fabricated device circuits are then packaged using vacuum or non-
vacuum lamination of LCP or alternate laminate materials detailed above in
connection with Step 1, and/or Al, Cu, Mo metal (for high power applications) on

both sides of the filter to a given thickness to encapsulate components, as illustrated in Step 6.

[0068] On the other side of the filter component, a cover coat material, liquid
5 photo imagable (LPI), or dry film solder mask is deposited using standard processes
such as spin coating, curtain or roller coating, dry film lamination, spray coating and
others, as illustrated in Steps 7, 8 and 9. This layer acts as a barrier to solder flow
between terminals during subsequent reflow and component assembly. The
component terminals are defined by opening windows in the cover coat / soldermask
10 material to open the BGA pads for board level interconnection. This is done with
processes such as photolithography or laser ablation. The device is then finished with
the addition of terminal metals appropriate for BGA assembly and soldering
processes. These finishing metals on the device terminals are common plated metals
or alloys like electroless Ni-Au, immersion tin, immersion silver, electroplated Ni-Au,
15 solder (HASL), or organic finishes (OSPs) and the choice depends on the intended
application and compatibility with the solder or other alloy used for device-to-
module/ PWB interconnection.

[0069] With general reference to Steps 10, 11, 12, the interconnects are
20 formed in the windows in the manner defined in Step 8 using Pb/Sn solder, or other
lead free solders and metal alloys. Processes such as screen or stencil printing of
solder paste and reflow, or plating processes can be used to form the bumps for
interconnection. The BGA/CSP format of the filter components enables the testing of
the components on the large area board prior to singulation. The testing can be done,
25 for example, with probing techniques or using test sockets or fixtures.

[0070] The fully fabricated wafer is then singulated into individual filter
components. The singulation can be done using high speed dicing saws or alternate
methods such as punching or routing/milling. An advantage of this fabrication
30 process is the ability to fully electrical test the components either before or after
singulation.

III. Actual Devices

Example I

[0071] An X-ray photograph of an organic bandpass filter 500 in accordance
 5 with an embodiment of the present invention is provided in FIGS. 7 and 8. The filter
 500 comprises shorted hybrid CPW-stripline meander transmission line inductors 512,
 514 formed close to each other on a first organic dielectric layer, which is a 50 μm
 thick layer of LCP, wherein the inductors 512, 514 are directly magnetically coupled
 to each other. Each inductor is connected to separate parallel plate capacitors 516,
 10 518 by sandwiching the same dielectric sheet. An inter-resonator parallel plate
 coupling capacitor 524, is formed using two disconnected metal plates that sandwich
 the same organic dielectric sheet in such a manner that the each plate of the inter-
 resonator coupling capacitor electrode connects to separate inductors. In addition, a
 second organic dielectric layer and a third organic dielectric layer sandwich the first
 15 organic dielectric layer, and comprise a high frequency hydrocarbon material with a
 thickness of 30-40 mils, which are disposed so as to sandwich said first dielectric
 sheets there between.

[0072] The bandpass filter 500 further comprises an additional dielectric layer,
 20 in this case solder mask, provided on an outermost one of the shield electrodes to
 protect the outermost shield electrodes. The inductors 512, 514 did not provide the
 needed capacitance in the desired length, and therefore each are connected to a
 separate grounded/shunted parallel plate using the same first organic layer as the
 sandwiched dielectric, which then together form the resonator pairs 560, 562, as
 25 illustrated. In the illustrated device, parallel plate capacitors 526, 528 are utilized on
 either side of the first and last resonator elements at the input and output terminals of
 the device for impedance matching purposes. If greater density is desired multiple
 thin layers such as the first dielectric layer can be used to form multi (>2) plate
 capacitors.

30

[0073] The bandpass filter 500 further comprise at two external ground shield electrodes 534 respectively formed on different side surfaces of a laminated body comprising said first through three or more dielectric layers and connected to said shield electrodes. Additionally these provide the connection for the shorted inductors/
5 resonators and capacitors. Moreover, the presence of these external electrodes makes it a CPW/stripline topology, where the reference is on the same first dielectric layer provides the shielding internally, and also provides for the ground connectivity to the resonators/inductors and capacitors.

10 [0074] The bandpass filter further comprises an external input terminal electrode 564 and an external output terminal electrode 566 which are formed on one side surface of a laminated body comprising said first through three or more dielectric sheets. External side wall shield electrodes 534 (FIG. 7) are provided between said external input and output terminal electrodes on the side surfaces of the laminated
15 body and external ground shield electrodes 548 are provided on opposing top and bottom surfaces of the laminated body and are electrically connected to the side wall shield electrodes 534.

[0075] The patterning of the external ground shields electrodes 548 on the top
20 and bottom surfaces is required for leaving space for the signal input output as shown in FIGS. 7 and 8.

[0076] In the organic bandpass filter 500, the first step to making connection between devices is done by drilling through holes as small as 2 mils with pads as big
25 as three times the size of the via through LCP and copper. Both sides of LCP copper laminate are then metalized via electroless. The copper on both sides of laminate is then electroplated, and the copper layer is printed and etched to define filter component.

30 [0077] The second and third organic dielectric layers are Rogers 4350 from Rogers Corporation with a generally larger thickness than the first organic dielectric

layer, such as approximately 35 mils, with copper metal (for high power applications) on both sides of filter to a given thickness to encapsulate components. All metals are electroplate and etched and patterned on top and bottom of the device to leave space for signal input and output.

5

[0078] The side wall grounded shield electrodes 534 can be obtained by single or multiple connected drilled plated through holes and then connected via electroless or sputter seeded copper in through hole. Electroplate copper in through hole and on surface. Print and etch copper to form SMD connection. The copper electrodes may be electroless NiAu plate to prevent excess oxidation.

10

[0079] FIG. 9 shows model to hardware correlation for the organic bandpass filter 500 in FIGS. 7 and 8. The filter was measured using an HP 8720ES Vector Network Analyzer after performing a SOLT calibration. The measured data for the fabricated filter and simulated data is shown. As evident from FIG. 9, there is excellent correlation between measured data and simulated data. The organic bandpass filter 500 was fabricated using LCP for the first organic dielectric layer, and shows an insertion loss of only 1.88dB at 3 GHz and a 1dB bandwidth of 200 MHz. Such a filter would be suitable for IF frequency use in fixed wireless type receivers where the carriers frequency of the incoming signal is approximately 14 GHz and has to be down-converted to several lower frequency signals.

15

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[0080] The organic bandpass filter 500 utilizes a CPW/stripline topology with only two metallization levels and all embedded passives in an organic substrate, which resulted in better performance than non-standardized multilayer (>5) ceramic processes, as seen in FIG. 9.

25

[0081] It is worth noting that while the Q of the capacitors for filter 500 was measured as high as 200 at 3 GHz using LCP, the Q for the inductor was kept at the required level of approximately 100 at 3 GHz. This was done to understand the advantages of using a material such as LCP without optimizing the design for the

30

inductors. However, Qs exceeding 200 are also attainable for inductors on organic substrates. A resimulation for the filter circuit shown, but with Qs of 200 for the inductors, showed an insertion loss of 1.15dB when simulated. A filter with a loss of 1.15dB at the frequency and bandwidth can be alternatively achieved only by using the bulkier and costlier ceramic cavity and monoblock filters.

Example II

[0082] Another organic bandpass filter 600 in accordance with an embodiment of the present invention is shown in the picture of FIG. 10. The filter 600 comprises shorted hybrid CPW-microstrip, meander inductors 612, 614 formed close to each other on a first organic dielectric layer, which is a layer of LCP, directly magnetically coupled to each other. The term "shorted" refers to one end of each inductor connected to the large metallic area, which in this case serves as the in-built shield 630 (also referred to as a coplanar ground ring). In addition, the filter 600 includes an inter-resonator parallel plate coupling capacitor electrode 624 with in-built shield 630 formed using two disconnected metal plates that sandwich the first organic dielectric layer in such a manner that the each plate of the inter-resonator coupling capacitor electrode connects to separate resonators. Yet further, the filter 600 includes a first shield electrode formed respectively on a second organic dielectric layer, which in this case is Rogers 4350 from Rogers Corporation, and which is disposed over the circuitry described above, so as to sandwich and substantially completely shield one surface of the filter.

[0083] The filter may further comprise a third organic dielectric sheet, if needed, provided on the outside of the shield electrode to protect the outermost shield electrode. In this filter, the inductors 612, 614 did not provide the needed capacitance in the desired length, and therefore each is connected to a separate grounded/shunted parallel plate (two plate) using the same first organic layer as the sandwiched dielectric, which then together form the resonator pairs. In addition, parallel plate/interdigital capacitors 626, 628 are utilized on either side of the first and last resonator elements at the input and output terminals of the device for impedance

matching purposes. If greater density is desired, then multiple thin layers such as the first dielectric layer can be used to form multi (>2) plate capacitors. In addition, another dielectric layer such as lower temperature melt LCP compare to the higher melt temp LCP used as the first dielectric is laminated on the other side of the first substrate (not the same side as the second substrate), and then solder bump openings are made where ground and input output connections are required to connect the device to corresponding terminals on the board.

[0084] The CPW topology, where the reference is on the same first dielectric layer provides the shielding internally, provides for the ground connectivity to the resonators/inductors and capacitors. However in more noisy environments the external electrodes, such as those in Example I, could be added for added shielding.

[0085] In the second bandpass filter, the openings in the third substrate allow for the ground connection connected to the CPW ground and two other openings not connected to each other or the ground serving for input and output terminals.

[0086] The first step to making connection between devices is by drilling through holes (as small in diameters as the thickness of the dielectric used) through the first organic dielectric layer of LCP and copper. Then both sides of LCP copper laminate are metalized via electroless copper. Copper is then electroplated on both sides of laminate. The copper is then printed and etched to define filter component.

[0087] The second organic dielectric layer can be laminate LCP or another appropriate dielectric with generally larger thickness than the first organic dielectric layer with copper metal (for high power applications) plated on top of the filter to a given thickness of approximately 20-30 μm to encapsulate components. The third organic dielectric layer is laminate LCP or another appropriate dielectric with generally larger or smaller thickness than the first organic dielectric layer with copper plated in the openings to a given thickness to provide for solder landing pads. The

openings in the third substrate are filled with screen solder paste and reflowed to form bumps.

[0088] FIG. 11 shows model to hardware correlation for the organic bandpass
 5 filter 600 in FIG. 10. In summary, the filter utilizes a CPW topology with only two
 metallization levels and all embedded passives in an organic substrate, which resulted
 in better performance than of non-standardized multilayer (>5) ceramic processes. As
 the adoption of lower loss materials, such as LCP, becomes more common, this
 design shows the feasibility of integrating very low loss filters for applications such as
 10 Bluetooth/WLAN in compact boards and packages.

[0089] The measured data for the filter 600 and simulated data is shown in
 FIG. 11. As seen there is excellent correlation between measured data and simulated
 data. The filter 600 has an insertion loss of only 2.22dB.

15 [0090] It is worth noting that while the Q of capacitors may be as high as 300
 using LCP, the Q for the inductor was kept at the required level of approximately 130.
 The insertion loss was 0.6dB lower than the MLC filters with similar footprint. A
 resimulation for the filter circuit shown, but with Qs of 200 for the inductors, showed
 20 an insertion loss of 1.65dB when simulated. A filter with a loss of 1.65dB at the
 frequency and bandwidth desired of the Bluetooth/WLAN filter can be alternatively
 achieved only by using the bulkier and costlier ceramic cavity and monoblock filters.

Example III

25 [0091] Yet another organic bandpass filter 700 in accordance with an
 embodiment of the present invention is shown in the picture of FIG. 12. The organic
 bandpass filter 700 comprises shorted hybrid CPW-microstrip meander inductors
 formed close to each other on a first organic dielectric substrate, such as epoxy based
 Vialux by E.I. du Pont de Nemours and Company, directly magnetically coupled to
 30 each other. In addition, the third bandpass filter comprises an inter-resonator parallel
 plate coupling capacitor electrode 724, with ground ring, formed using two

disconnected metal plates that sandwich the same organic dielectric sheet in such a manner that the each plate of the inter-resonator coupling capacitor electrode connects to separate resonators.

5 [0092] The transmission line inductors 712, 714 did not provide the needed capacitance in the desired length. Since the dielectric is lossy for the capacitor application, each is replaced by a separate discrete capacitor 702, such as a chip capacitor or ceramic capacitor with one terminal of one capacitor connected to one resonator and the other shorted to the in-built shielding electrode 730. The same can
10 be done for the other capacitor 724 where one terminal is grounded, i.e., connected to a CPW ground electrode 730 and the other terminal is connected to the resonator section. In addition, a parallel plate/interdigital capacitors 726, 728 are utilized on either side of the first and last resonator elements at the input and output terminals of the device for impedance matching purposes. If greater density is desired multiple
15 thin layers such as the first dielectric layer can be used to form multi (>2) plate capacitors.

[0093] The organic bandpass filter 700 may further comprise another monolayer second organic dielectric layer that is laminated on the one side of the first
20 organic dielectric layer (opposite the side of the discrete capacitors). In addition, it may further comprise multiple plate through holes going through first and second organic dielectric layer connected to the in-built shielding electrode 730 and metal sheet of the monolayer dielectric. This may or may not be desired for cost saving purposes, though adding these vias makes it a true CPW/microstrip hybrid device.
25 The CPW topology, where the reference is on the same first organic dielectric layer, provides the shielding internally, and also provides for the ground connectivity to the resonators/inductors and capacitors. However in more noisy environments the external through holes can be added for added shielding.

30 [0094] The organic bandpass filter 700 may further comprise a third organic dielectric layer on the same side as the discrete capacitors 702 providing for

protection of the circuits and seal the device from moisture uptake and corrosion.

This material could be the same as solder mask materials, which would be used by the board manufacturers to protect other circuits on the board. In addition, the bandpass filter 700 may further comprise a metallic lid or cap/electromagnetic shield which
 5 encloses the device on the top surface and prevents EMI interference and radiation effects from affecting the performance of the filter.

[0095] FIG. 13 shows model to hardware correlation for the organic bandpass filter 700 in FIG. 12. In particular, FIG. 13 shows a model to hardware correlation for
 10 the filter with all embedded components, except the two discrete capacitors. As shown, there is very good agreement between measured and predicted results. The measured filter has a center frequency = 1.9 GHz, a 1dB passband of 60 MHz, and a 3dB bandwidth of 120 MHz. The attenuation at 1.5 GHz is ~ 40dB, as desired. The insertion loss is approximately 3.8dB at 1.9 GHz, which is greater than the
 15 specification of 3dB for such applications. This is due to the use of center and matching capacitors with Qs of 40 in Vialux rather than the required Q of 60 needed to achieve a lesser loss of 3dB. This insertion loss can be lowered by using A-PPE™ or LCP™ from Rogers Corporation dielectric materials for the organic dielectric layer. Such a filter would be applicable in cellular phones as the intermediate RF filter or in
 20 cordless phones as the front-end RF filter.

[0096] As seen in FIG. 13, there is a discrepancy in the measured and predicted results beyond 2.5 GHz for S_{21} . This discrepancy is due to the coupling between the two discrete capacitors. The simulations were done for individual
 25 components and for optimizing the spacing between the inductors. The discrete capacitors were measured as individual components without any coupling between them. The tight spacing between the capacitors could have resulted in unwanted coupling effects which show up at frequencies greater than 2.5 GHz. After including a mutual coupling term between the two discrete capacitors, the results show better
 30 agreement with measurements.

[0097] In summary, the organic bandpass filter 700 utilizes a CPW topology with only two metallization levels and an epoxy based substrate along with discrete capacitors, which achieves the performance of non-standardized multilayer (>5) ceramic processes. Additionally, the MLC filters cannot be integrated with other components in the same layers of the ceramic package due to several reasons, a few of which include: firstly, because of the use of a filter-specific dielectric which is incompatible with other dielectrics; secondly, because of the specificity of certain attributes such as 100 μm thick aluminium conductor lines required to lower the attenuation present due to standard 5 μm lines used in ceramic processes. The design discussed in this section was fabricated using standard design rules pertinent to multilayer laminate boards and can be directly implemented on the board without the need for a separate surface mount device. Furthermore, the model to hardware correlation shows validity of the design technique used.

15 [0098] Many modifications and other embodiments of the inventions set forth herein will come to mind to one skilled in the art to which these inventions pertain having the benefit of the teachings presented in the foregoing descriptions and the associated drawings. Therefore, it is to be understood that the inventions are not to be limited to the specific embodiments disclosed and that modifications and other
20 embodiments are intended to be included within the scope of the appended claims. Although specific terms are employed herein, they are used in a generic and descriptive sense only and not for purposes of limitation.

THAT WHICH IS CLAIMED:

1. An organic bandpass filter, comprising:
 - a first core layer having an upper surface and a lower surface;
 - 5 a second core layer having an upper surface and a lower surface, wherein the first core layer and the second core layer are positioned opposite one another so that the lower surface of the first core layer is facing the upper surface of the second core layer;
 - an organic dielectric layer having at least two resonators, wherein two of the resonators are coupled to each other, the organic dielectric layer being arranged
 - 10 between the first core layer and the second core layer;
 - a first shield electrode on the upper surface of the first core layer opposite the organic dielectric layer;
 - a second shield electrode on the lower surface of the second core layer
 - 15 opposite the organic dielectric layer; and
 - a side shield electrode in electrical contact with the first and second shield electrodes.
2. The bandpass filter of Claim 1, wherein the resonators are coupled
- 20 magnetically, electrically or a combination thereof.
3. The bandpass filter of Claim 1, wherein the resonators comprise a combination of transmission lines, inductors and capacitors.
- 25 4. The bandpass filter of Claim 1, wherein the resonators are formed by transmission line.
5. The bandpass filter of Claim 1, wherein the resonators are formed by inductors.
- 30

6. The bandpass filter of Claim 1, wherein each of the resonators comprises an inductor connected to a parallel plate capacitor, wherein the capacitors include disconnected plates sandwiching the organic dielectric layer.

5 7. The bandpass filter of Claim 1, further comprising an external input terminal electrode and an external output terminal electrode formed on opposite side surfaces of the filter, and the side shield electrode being disposed on other opposite sides of the filter.

10. 8. The bandpass filter of Claim 7, wherein the organic dielectric layer includes a circuit matching device connected to the external input terminal electrode and a second circuit matching device connected to the external output terminal electrode, wherein the first and second circuit matching devices are selected from the group consisting of a capacitor, inductor, transmission line and a combination thereof.

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9. The bandpass filter of Claim 1, wherein both the first and second core layers include a bondply layer.

10. The bandpass filter of Claim 1, wherein the organic dielectric layer
20 comprises multiple layers of organic material, and wherein at least a portion of a
passive device is formed on each respective layer of the multiple layers of organic
material.

11. The bandpass filter of Claim 1, wherein the organic dielectric layer
25 comprises a first patterned metal layer and a second patterned metal layer formed on
opposite surfaces thereof, and further comprises at least one via electrically
connecting the first patterned metal layer and the second patterned metal layer.

12. The bandpass filter of Claim 1, further comprising a first protective
30 layer formed on the first shield electrode and a second protective layer formed on the
second shield electrode.

13. The bandpass filter of Claim 1, wherein the side shield electrode comprises a third shield electrode and fourth shield electrode formed on opposite side surfaces of the filter.

5

14. The bandpass filter of Claim 1, wherein the side shield electrode comprises an in-built shield electrode on the organic dielectric layer that is coplanar with at least a portion of the resonators.

10

15. The bandpass filter of Claim 14, wherein at least one resonator includes a capacitor, and the capacitor includes a first plate on a first surface of the organic dielectric layer and a corresponding ground plate on the opposite surface of the organic dielectric layer, and wherein the in-built shield is disposed on the first surface in proximity of the first plates and is electrically connected to the second plates by vias in the organic dielectric layer.

15

16. The bandpass filter of Claim 1, further comprising an additional resonator formed by one of an inductor, transmission line, capacitor or a combination thereof.

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17. The bandpass filter of Claim 1, further comprising a plurality of poles formed by one of an inductor, transmission line, capacitor or a combination thereof.

18. An organic bandpass filter, comprising:

25 a protective layer having an upper surface and a lower surface;

a core layer having an upper surface and a lower surface, wherein the core layer and the protective layer are position opposite one another so that the lower surface of the protective layer is facing the upper surface of the core layer;

30 an organic dielectric layer having at least two resonators, wherein two of the resonators are coupled to each other, the organic dielectric layer being arranged between the core layer and the protective layer;

a first shield electrode on the lower surface of the core layer opposite the organic dielectric layer;

a side shield electrode in electrical contact with the first shield electrode;

a plurality of solder balls on the protective layer; and

5 through holes that electrically connect at least one solder ball to the first shield electrode.

10 19. The bandpass filter of Claim 18, wherein the resonators are coupled magnetically, electrically or a combination thereof.

20. The bandpass filter of Claim 18, wherein the resonators comprise a combination of transmission lines, inductors and capacitors.

15 21. The bandpass filter of Claim 18, wherein the resonators are formed by transmission line.

22. The bandpass filter of Claim 18, wherein the resonators are formed by inductors.

20 23. The bandpass filter of Claim 18, wherein each of the resonators comprises an inductor connected to a parallel plate capacitor, wherein the capacitors include disconnected plates sandwiching the organic dielectric layer.

25 24. The bandpass filter of Claim 18, further comprising an external input terminal electrode and an external output terminal electrode formed on the protective layer, wherein the terminal electrodes are connected to separate solder balls.

30 25. The bandpass filter of Claim 24, wherein the organic dielectric layer includes a circuit matching device connected to the external input terminal electrode and a second circuit matching device connected to the external output terminal

electrode, wherein the first and second circuit matching devices are selected from the group consisting of a capacitor, inductor, transmission line and a combination thereof.

26. The bandpass filter of Claim 18, wherein the core layers include a
5 bondply layer.

27. The bandpass filter of Claim 18, wherein the organic dielectric layer
comprises multiple layers of organic material, and wherein at least a portion of a
passive device is formed on each respective layer of the multiple layers of organic
10 material.

28. The bandpass filter of Claim 18, wherein the organic dielectric layer
comprises a first patterned metal layer and a second patterned metal layer formed on
opposite surfaces thereof, and further comprises at least one via electrically
15 connecting the first patterned metal layer and the second patterned metal layer.

29. The bandpass filter of Claim 18, wherein the protective layer
comprises an organic material.

20 30. The bandpass filter of Claim 18, wherein the side shield electrode
comprises a second shield electrode and third shield electrode formed on opposite side
surfaces of the filter.

31. The bandpass filter of Claim 18, wherein the side shield electrode
25 comprises an in-built shield electrode on the organic dielectric layer that is coplanar
with at least a portion of the resonators.

32. The bandpass filter of Claim 31, wherein at least one resonator
includes a capacitor, and the capacitor includes a first plate on a first surface of the
30 organic dielectric layer and a corresponding ground plate on the opposite surface of
the organic dielectric layer, and wherein the in-built shield is disposed on the first

surface of the organic dielectric layer in proximity of the first plates and is electrically connected to the second plates by vias in the organic dielectric layer.

33. The bandpass filter of Claim 18, further comprising an additional
5 resonator formed by one of an inductor, transmission line, capacitor or a combination thereof.

34. The bandpass filter of Claim 18, further comprising a plurality of poles
10 formed by one of an inductor, transmission line, capacitor or a combination thereof.

35. A stand-alone organic passive device, comprising:
a first core layer having an upper surface and a lower surface;
a second core layer having an upper surface and a lower surface, wherein the
first core layer and the second core layer are position opposite one another so that the
15 lower surface of the first core layer is facing the upper surface of the second core
layer;
an organic dielectric layer having at least on passive device, the organic
dielectric layer being arranged between the first core layer and the second core layer;
a first shield electrode on the upper surface of the first core layer opposite the
20 organic dielectric layer;
a second shield electrode on the lower surface of the second core layer
opposite the organic dielectric layer; and
a side shield electrode in electrical contact with the first and second shield
electrodes.

36. A stand-alone organic passive device, comprising:
a protective layer having an upper surface and a lower surface;
a core layer having an upper surface and a lower surface, wherein the core
layer and the protective layer are position opposite one another so that the lower
25 surface of the protective layer is facing the upper surface of the core layer;

an organic dielectric layer having at least one passive device, the organic dielectric layer being arranged between the core layer and the protective layer;

a first shield electrode on the lower surface of the core layer opposite the organic dielectric layer;

5 a side shield electrode in electrical contact with the first shield electrode;

a plurality of solder balls on the protective layer; and

through holes that electrically connect at least one solder ball to the first shield electrode.

10

INTEGRATED PASSIVE DEVICES FABRICATED
UTILIZING MULTI-LAYER, ORGANIC LAMINATES

5

ABSTRACT

The present invention includes an organic device that can be integrated in a multilayer board made of organic material. The passive devices can be integrally fabricated on a circuit board in either surface mount device (SMD) or ball grid array (BGA) form. Alternatively, the passive device can be constructed in a stand alone
10 SMD or BGA/chip scale package (CSP) form to make it mountable on a multilayer board, ceramic carrier or silicon platform in the form of an integrated passive device. The passive device includes side shielding on two sides in the SMD form and four sides in the BGA/CSP form. The side shielding can be external or in-built.

15

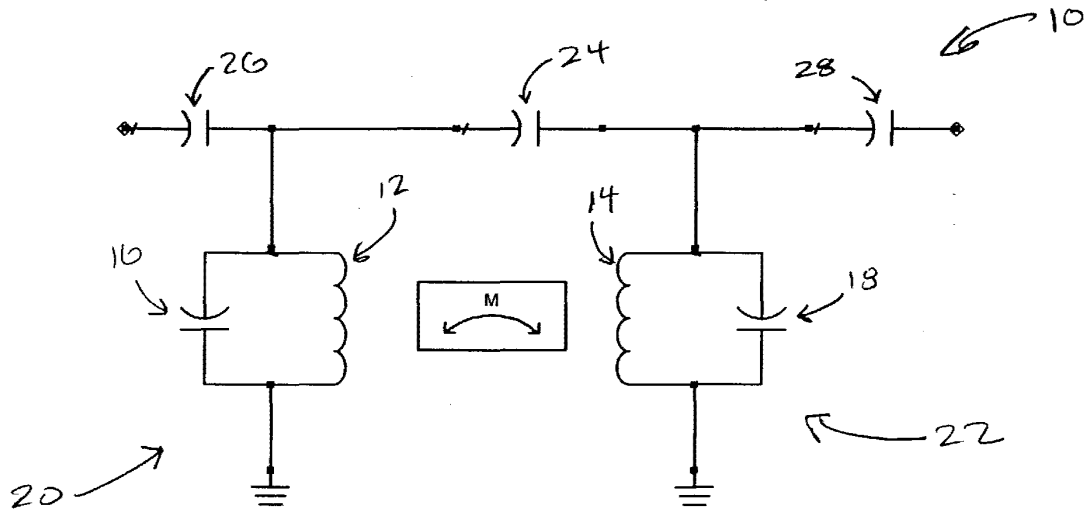


FIG. 1A

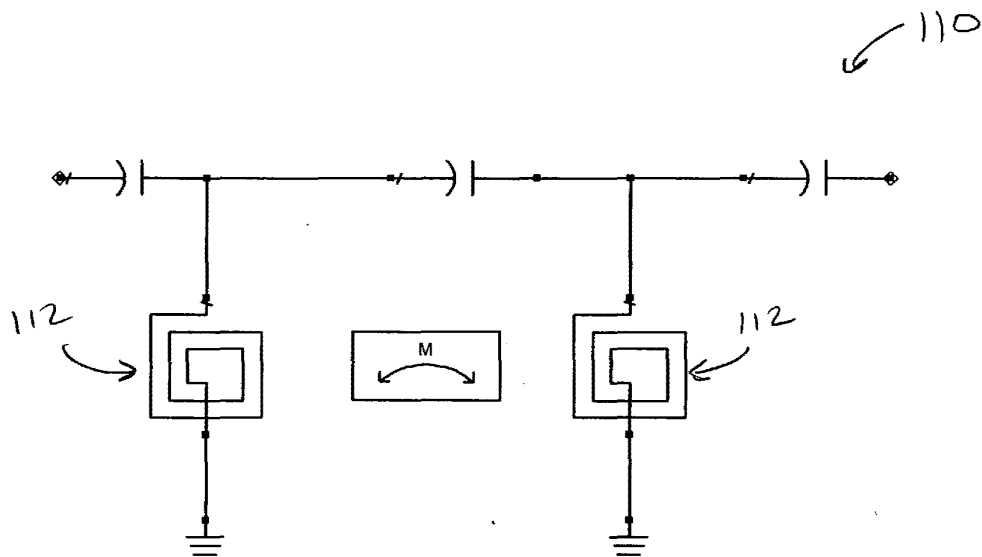


FIG. 1B

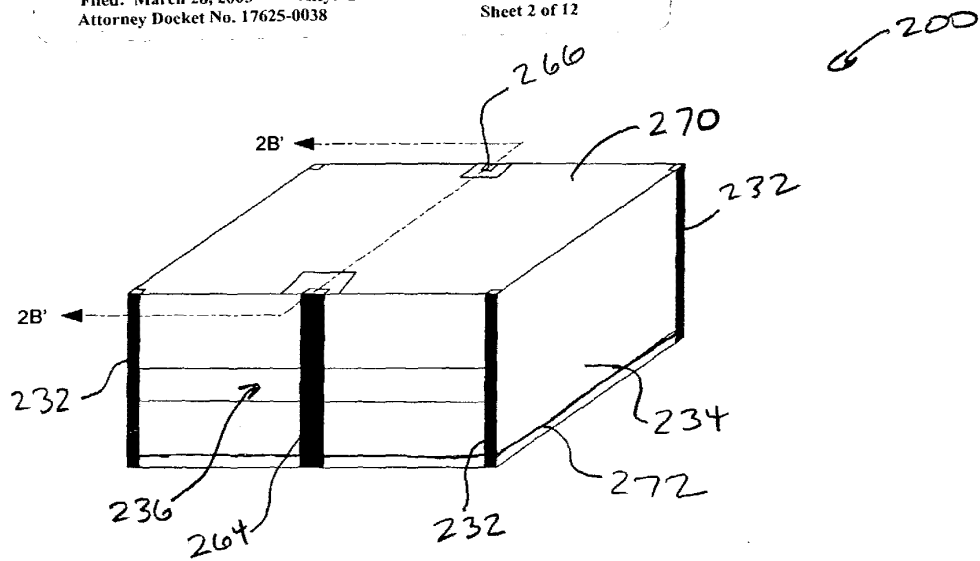


FIG. 2A

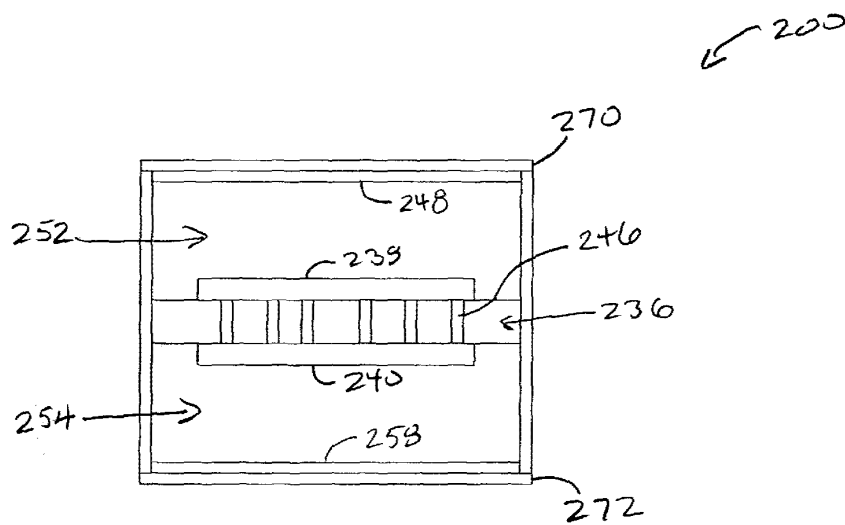


FIG. 2B

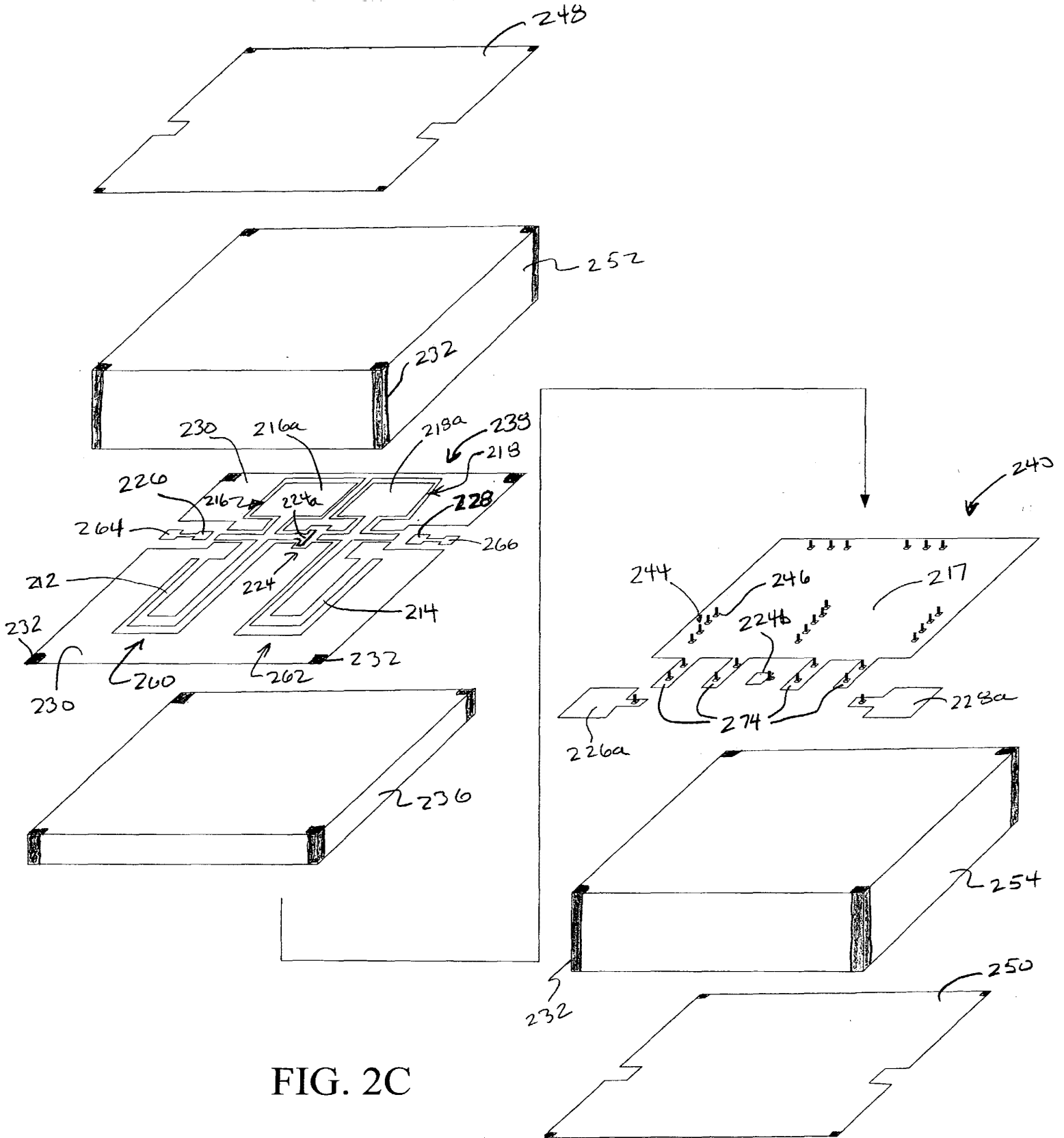


FIG. 2C

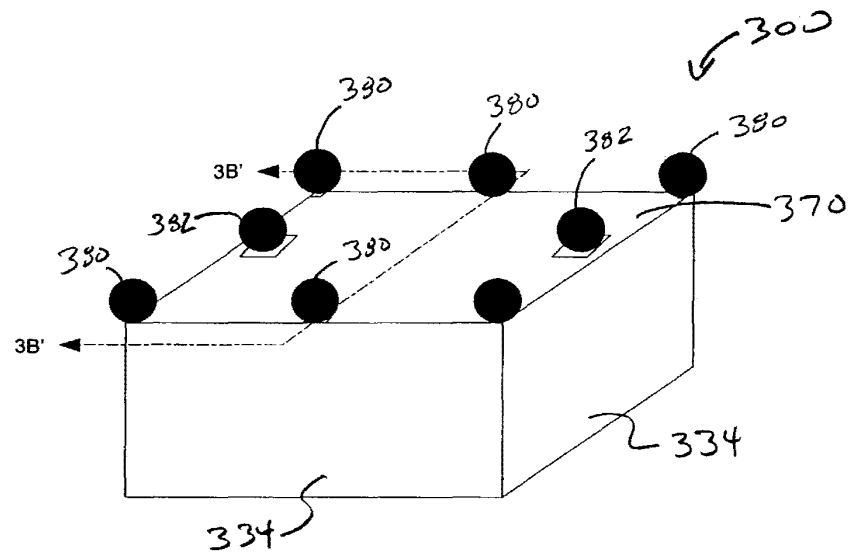


FIG. 3A

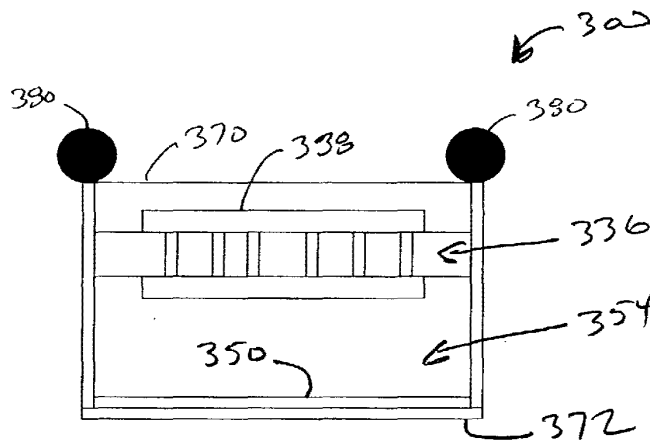


FIG. 3B

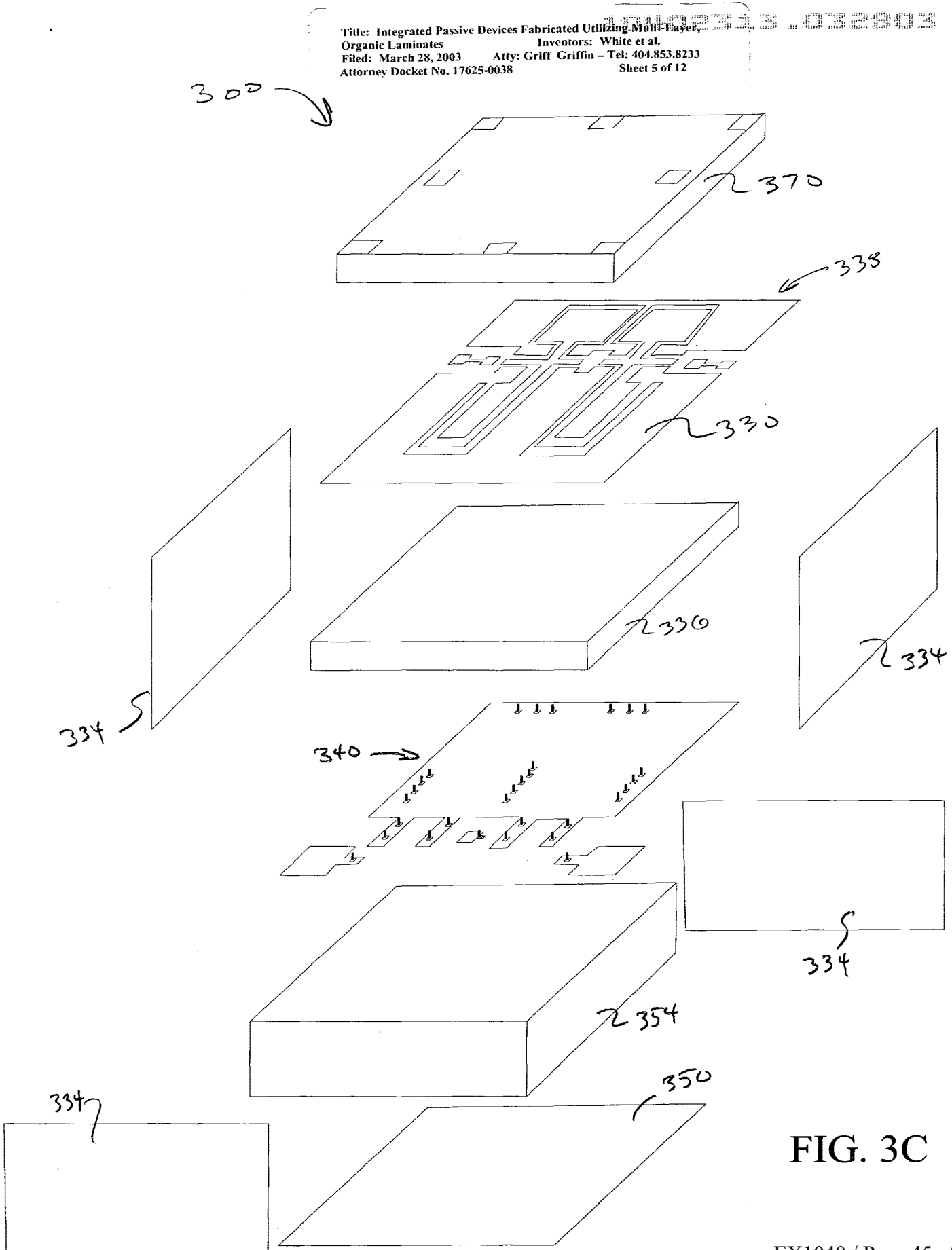


FIG. 3C

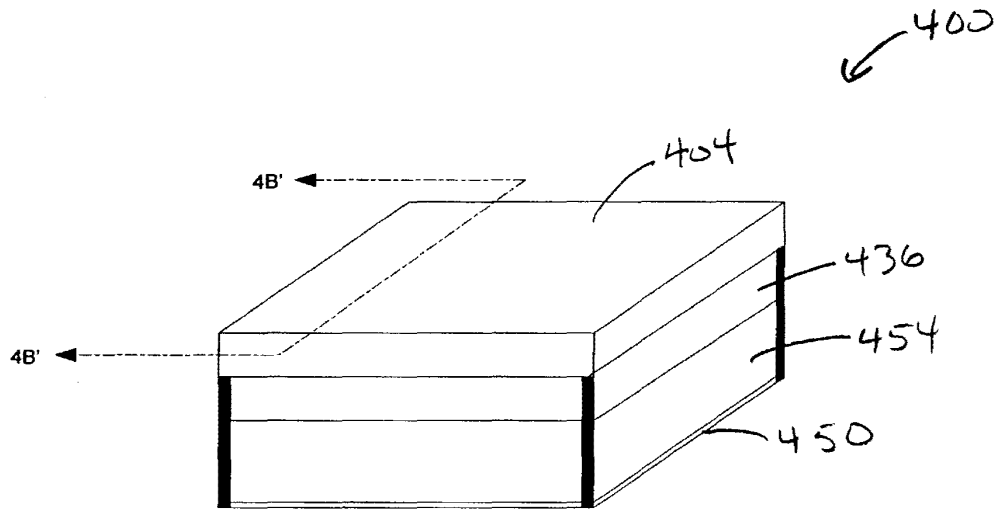


FIG. 4A

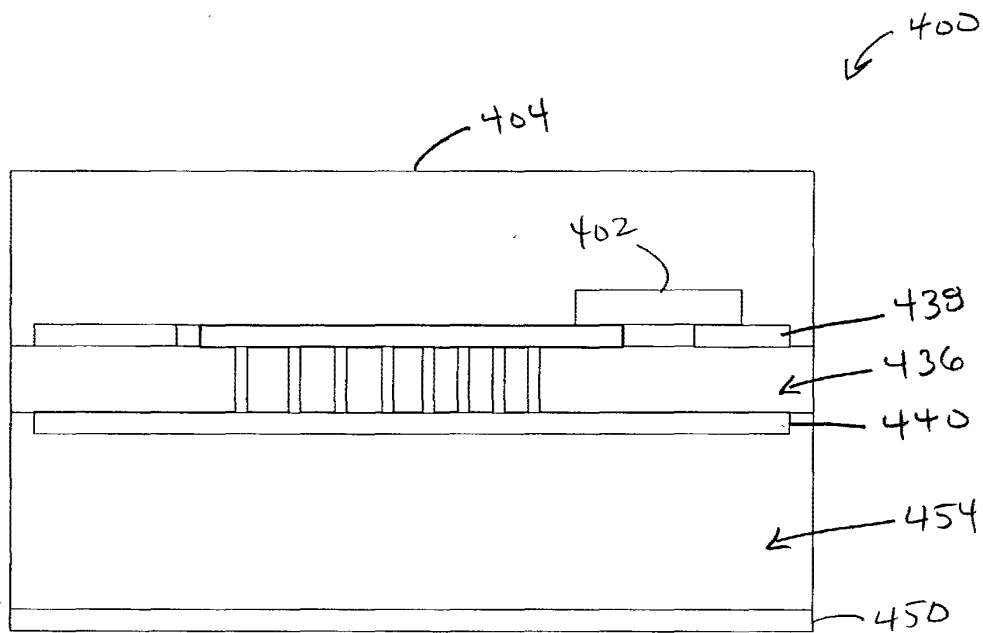


FIG. 4B

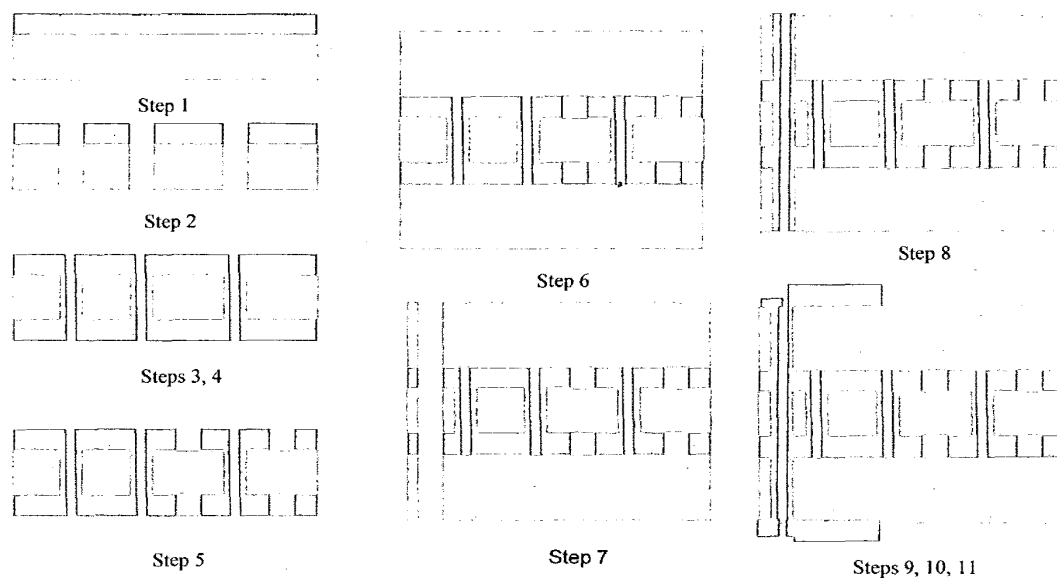


FIG. 5

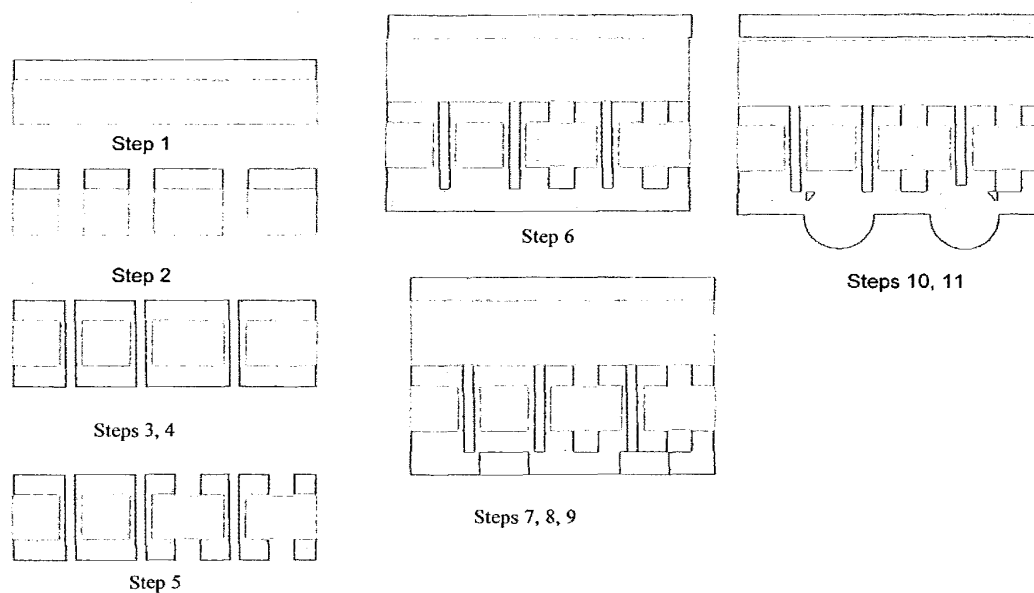


FIG. 6

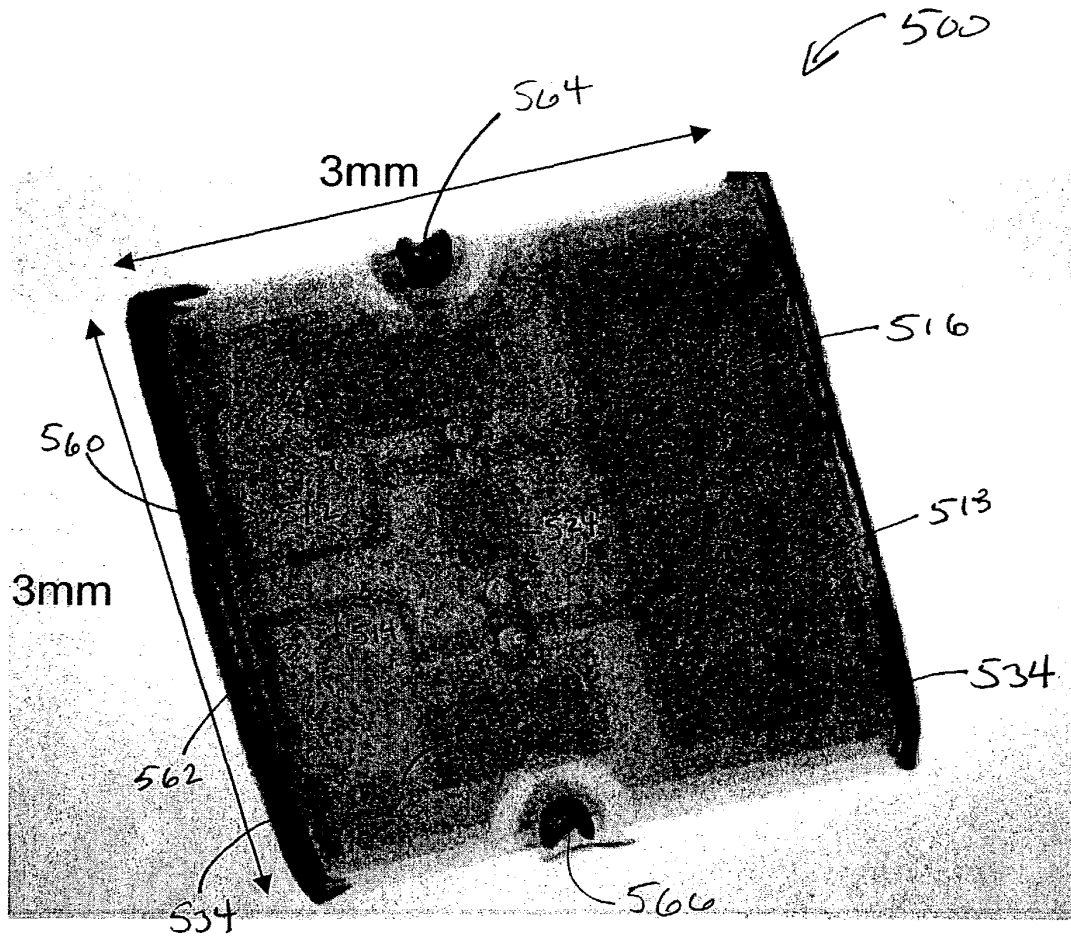


FIG. 7

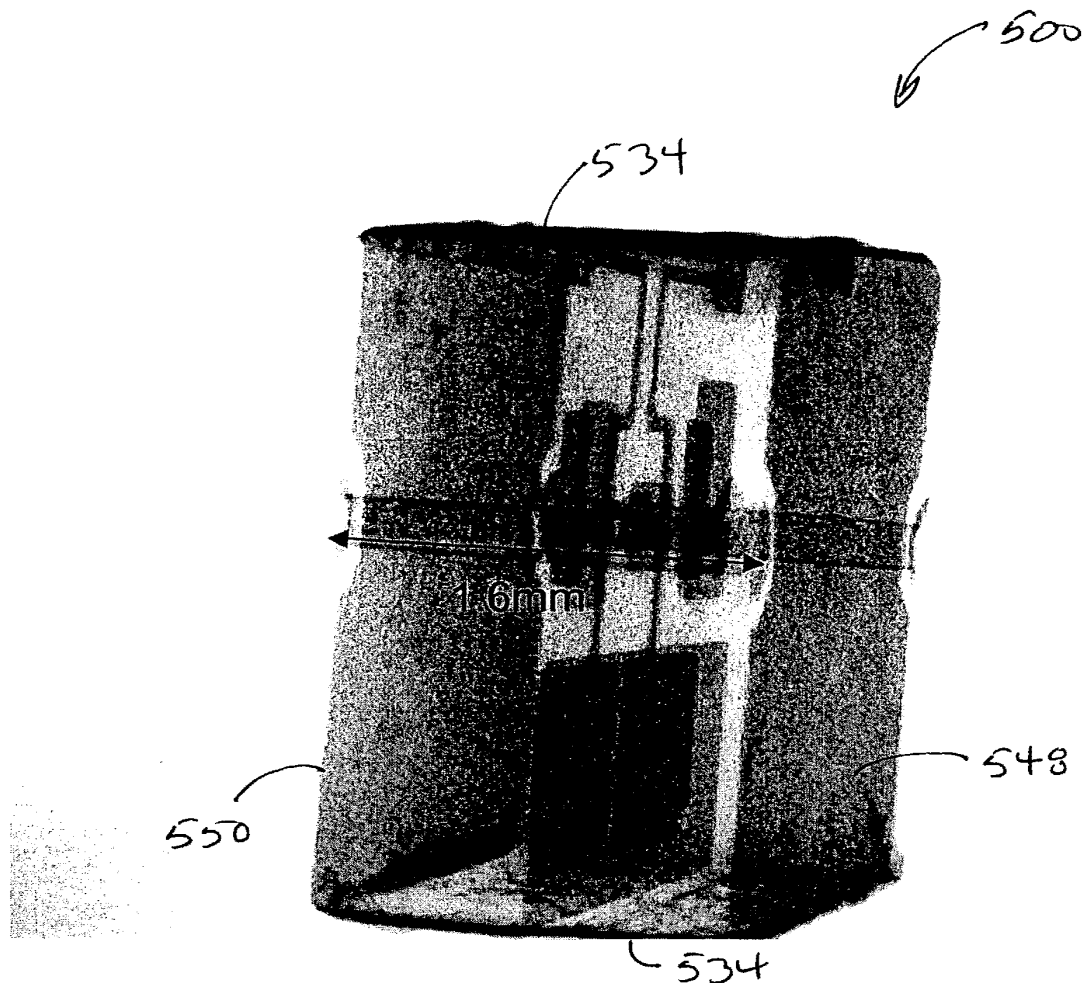


FIG. 8

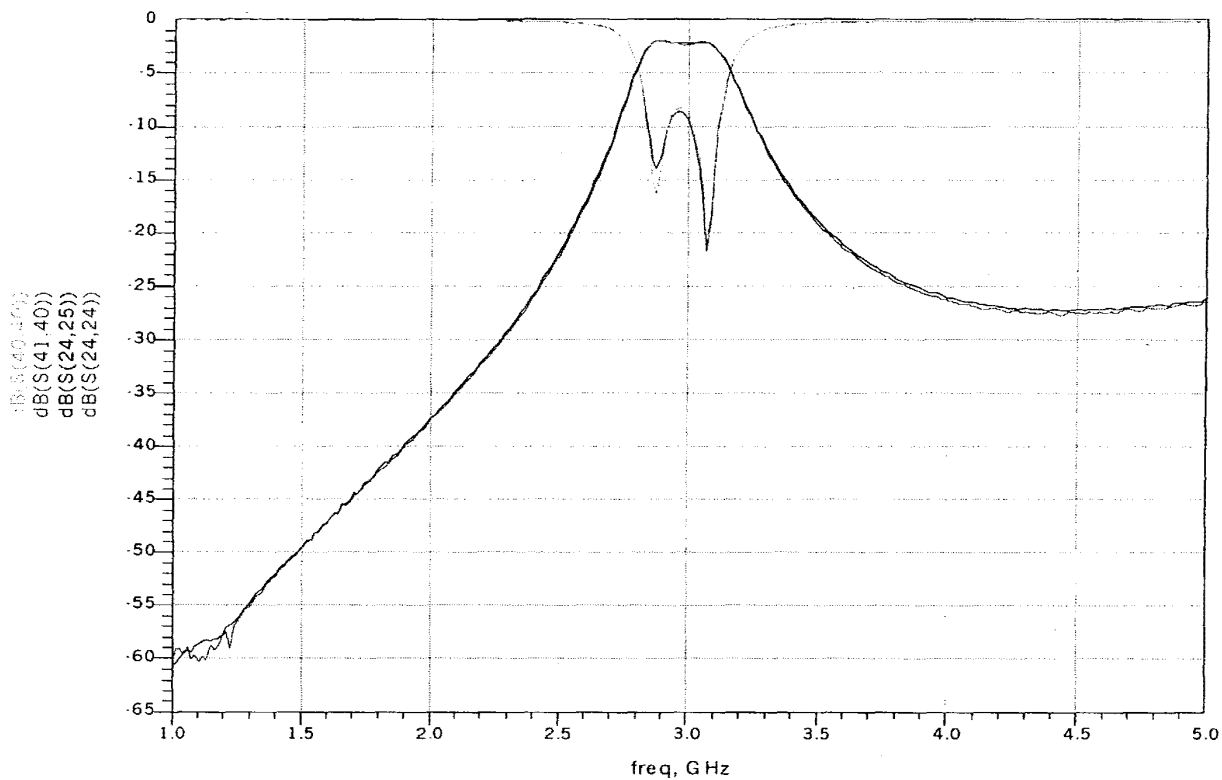


FIG. 9

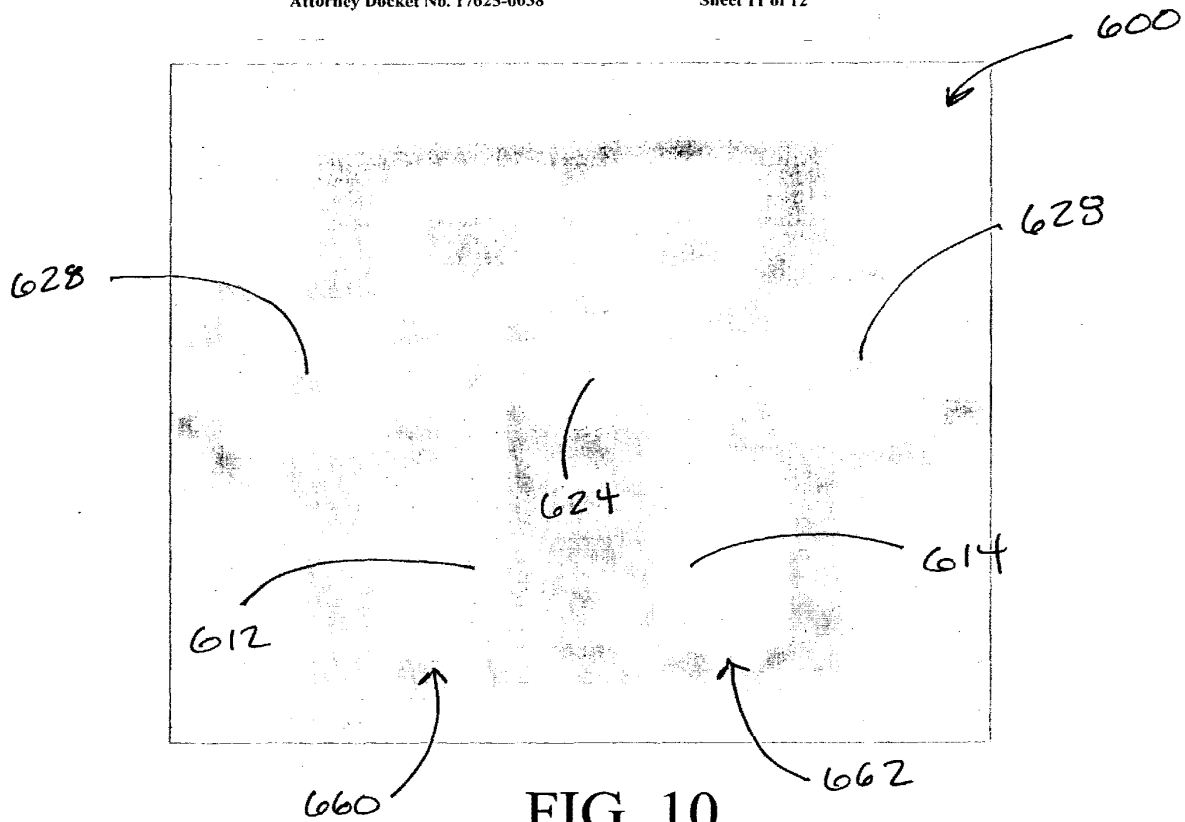


FIG. 10

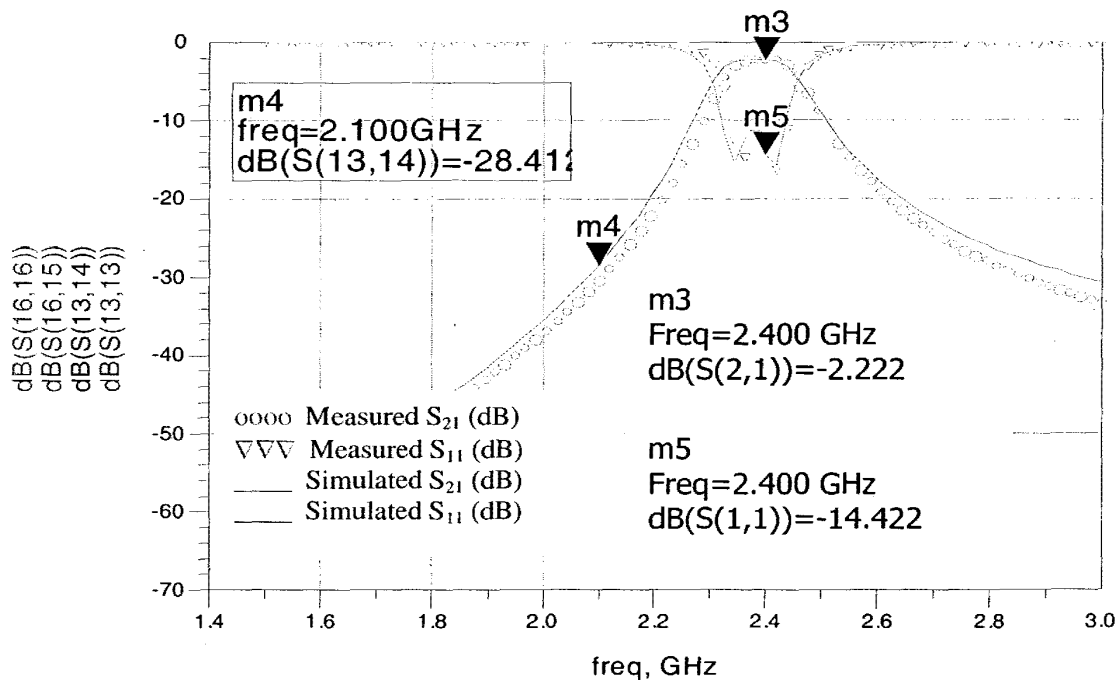


FIG. 11

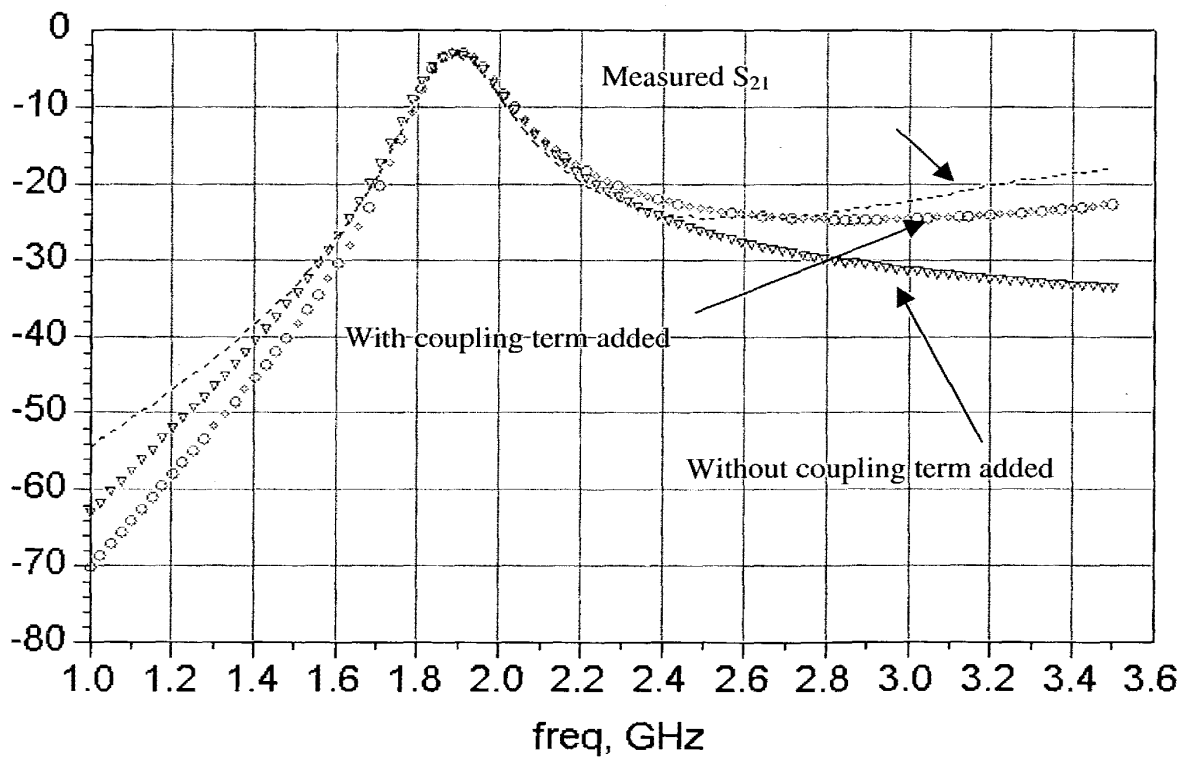
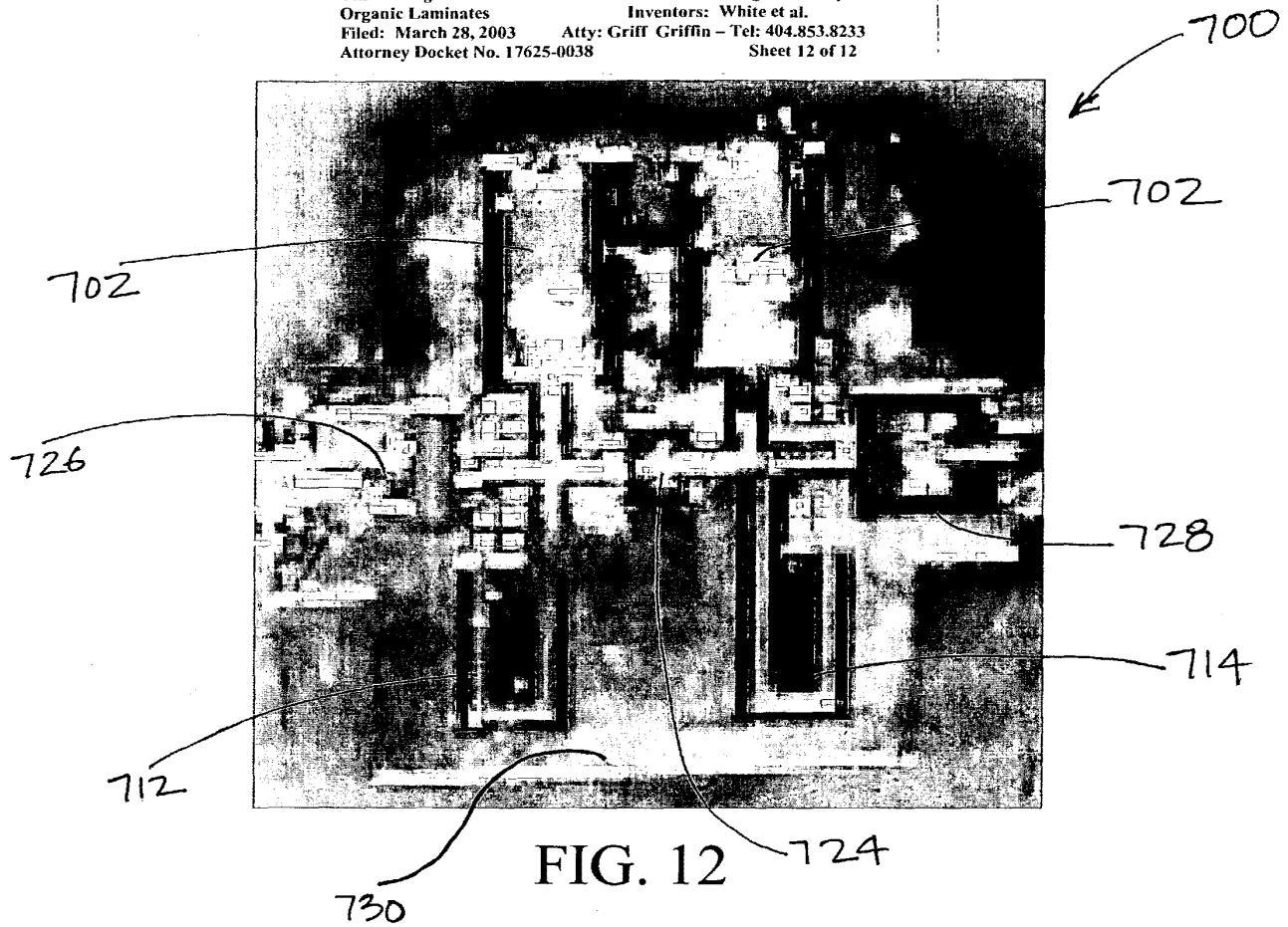
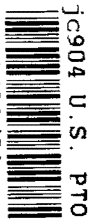


FIG. 13

**U.S. Application No.
10/402,315 filed 3-28-2003**

03/28/03



jc904 U.S. PTO

UTILITY
PATENT APPLICATION
TRANSMITTAL(Only for new nonprovisional applications
under 37 CFR 1.53(b))

Attorney Docket No.

17625-0039

Named Inventor(s)

White, et al.

Title

Methods For Fabricating Three-Dimensional All
Organic Interconnect Structures

Express Mail Label No.

EV048621785US

1050 U.S. PTO
10/402315

03/28/03

APPLICATION ELEMENTS

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)
2. ☒ Applicant claims small entity status.
See 37 CFR 1.27.
3. ☒ Specification, Claims,
and Abstract Total Pages 17
4. ☒ Drawings Total Sheets 8
5. Oath or Declaration Total Pages 3
- a. ☒ Newly executed (original or copy)
- b. ☐ Copy from prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 19
completed)
- (i) ☐ **DELETION OF INVENTOR(S)**
Signed statement attached deleting
inventor(s) named in the prior
application, see 37 CFR 1.63(d)(2)
and 1.33(b).
6. ☐ Incorporation by Reference
(usable if Box 5b is checked)
The entire disclosure of the prior application, from which
a copy of the oath or declaration is supplied under Box
5b, is considered as being part of the disclosure of the
accompanying application and is hereby incorporated
by reference therein.
7. ☐ Nonpublication Request Under 35 U.S.C.
122(b)(2)(B)(i).
☐ Form PTO/SB/35
8. ☐ Application Data Sheet. See 37 CFR 1.76
9. ☐ CD-ROM or CD-R in duplicate, large table or
Computer Program (Appendix)

10. ☐ Nucleotide and/or Amino Acid Sequence
Submission (if applicable, all necessary)
- a. ☐ Computer Readable Form (CRF)
- b. ☐ Specification Sequence Listing on:
- i. ☐ CD-ROM or CD-R (2 copies); or
- ii. ☐ paper
- c. ☐ Statement verifying identity of above
copies
11. ☒ Assignment:
- a. ☒ Assignment Papers (cover sheet &
document(s))
- b. ☐ Assignment is of record in parent
application No.
12. ☐ 37 CFR 3.73(b) Statement
(when there is an assignee)
☐ Power of Attorney by assignee
13. ☐ English Translation Document (if applicable)
14. ☒ Information Disclosure Statement (IDS) PTO-
1449
☒ Copies of IDS Citations (62 references)
15. ☐ Preliminary Amendment
16. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
17. ☐ Certified Copy of Priority Document(s)
18. ☐ Other:

19. If a **CONTINUING APPLICATION**, check appropriate box and supply the requisite information and in a preliminary
amendment, or in an Application Data Sheet under 37 CFR 1.76:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No:
Prior application information: Examiner: Group Art Unit:
Recite complete dependency back to first parent application:

20. CORRESPONDENCE ADDRESS:
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Date: March 28, 2003

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Reg. No. 38,899

I hereby certify that this correspondence is being deposited with the United States Postal Service in an Express Mail envelope
(EV048621785US) addressed to: Assistant Commissioner for Patents, Washington, D.C. this 28th day of March, 2003.

Malvern U. Griffin III

ATTACH CUSTOMER BAR CODE LABEL BELOW



29052

PATENT TRADEMARK OFFICE

AO 885527.1

EX1040 / Page 54 of 165
Murata Manufacturing Co., Ltd.

FEE TRANSMITTAL

Attorney Docket No. 17625-0039

This sheet accompanies a patent application transmittal for the following application:

Inventor(s): White, et al.

Filing Date: March 28, 2003

Serial No.:

Title: Methods For Fabricating Three-Dimensional
All Organic Interconnect Structures

The filing fee is calculated as shown below:

1. FILING FEE:

SMALL ENTITY			LARGE ENTITY	
FOR:	FEE	FEE PAID	FEE	FEE PAID
☒ UTILITY FILING FEE	\$375	\$375	\$750	
☐ DESIGN FILING FEE	\$165		\$330	
☐ PLANT FILING FEE	\$260		\$520	
☐ REISSUE FILING FEE	\$375		\$750	
☐ PROVISIONAL FILING FEE	\$80		\$160	
SUBTOTAL (1)		\$375		

2. CLAIMS:

SMALL ENTITY				LARGE ENTITY		
FOR:	NO. FILED	NO. EXTRA	RATE	FEE	RATE	FEE
TOTAL CLAIMS	21 - 20 =	1	x 9 =	\$9	x 18 =	
INDEP. CLAIMS	2 - 3 =	0	x 42 =		x 84 =	
☐ MULTIPLE DEPENDENT CLAIM PRESENTED			+140 =		+280 =	
SUBTOTAL ()				\$9		

3. ADDITIONAL FEES:

SMALL ENTITY			LARGE ENTITY	
FOR:	FEE	FEE PAID	FEE	FEE PAID
☐ LATE FILING, FEE OR OATH	\$65		\$130	
☐ NON-ENGLISH SPECIFICATION	\$130		\$130	
☐ OTHER				
SUBTOTAL (3)		0		

TOTAL FILING FEES: \$384A check is enclosed for the total amount: **\$384**☒ Charge any additional fees required to Deposit Account 19-5029.

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Reg. No. 38,899

Date: March 28, 2003

5

METHODS FOR FABRICATING THREE-DIMENSIONAL
ALL ORGANIC INTERCONNECT STRUCTURES

10

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims benefit of co-pending U.S. Provisional
Application No. 60/391,742, filed June 26, 2002, which is entirely incorporated herein
by reference. In addition, this application is related to the following co-pending,
15 commonly assigned U.S. applications, each of which is entirely incorporated herein
by reference: "Integrated Passive Devices Fabricated Utilizing Multilayer, Organic
Laminates" filed March 28, 2003, and accorded Application No. _____; and
"Stand-Alone Organic-Based Passive Devices" filed March 28, 2003, and accorded
Application No. _____.

20

BACKGROUND OF THE INVENTION

I. Field of the Invention

[0002] The present invention generally relates to three-dimensional all organic
structures, and more particularly to three-dimensional organic interconnect structures
25 for use in radio frequency and mixed signal module substrates and multilayer high-
speed printed circuit boards.

II. Description of Related Art

[0003] Multilayer circuits typically comprise at least one conductive circuit
30 layer bonded or laminated to a dielectric layer. The conductive circuit layer is
generally a conductive metal such as copper, and the dielectric layer generally

comprises a polymer resin such as epoxy. Depending on the selection of the dielectric layer and its thickness, the circuit can be either stiff or flexible.

[0003] Multilayer organic circuits incorporating thin film technologies are typically fabricated by parallel processing using dielad or monolad layers that are sandwiched between bond ply materials to form a multilayer circuit construction. The number of metal layers can be as few as two and as many as sixty or more. The requirements for multilayer circuits in high density, high performance applications are becoming ever more demanding for high frequency applications. As a result there exists an unresolved need for a low cost multilayer process that can support both high frequency and high density (e.g., fine line and spaces, small via sizes) multilayer circuit constructions.

SUMMARY OF THE INVENTION

[0004] The present invention comprises three-dimensional (3-D) multilayer circuit structures and methods of fabricating same wherein the circuit structures comprise uncladded high and low temperature organic material, such as liquid crystalline polymers (LCPs), teflon or polyphenyl ether (PPE) based materials, that have equivalent electrical and mechanical properties but differing melt temperatures, which enable a uniform homogeneous electrical circuit that can support high frequency and high bandwidth applications. The two different melt points allow for the stacking and lamination of individual circuitized layers to form multilayer construction, which when combined with a higher temperature metallic alloy provides for a reliable metal to metal joining that occurs at a temperature slightly above that at which the fusion bonding of the dielectric to dielectric and dielectric to metal occurs. Incorporation of resistive and high k particles or deposition resistive and high k films into or onto the high melt point and/or low melt point organic layers allows for the ability to integrate buried passives structures, (e.g., bias, decoupling and filter elements) in a 3-D multilayer construction.

[0005] The incorporation or deposition of the resistive materials into or on the organic layers provides for the ability to form single resistor elements and arrays when combined with a standardized lithographical process for circuit formation. Similarly, the incorporation of high dielectric constant materials or deposition of the same having dielectric constants from 8 to 20,000 provides for single capacitor elements and arrays when combined with standardized lithographical processes for circuit formation. This enables the fabrication of parallel plate capacitors, interdigitated (comb) capacitors and distributed capacitance layers with capacitance densities well beyond 1 nf/cm².

[0006] The use of uncladded high temperature and low temperature organic layers allow for the fabrication of fine line geometries down to five micron lines and spaces using build up processes that involve depositing a thin metal conductive layer by electroless plating or vacuum deposition, which could be any one of copper, Ni, Au, Pd, Pt. A photoresist is then deposited, lithographically exposed and then developed. A conductor metal layer is then electroplating through the patterned resist, wherein the conductor metal could be any one of Cu, Ni, Au, Pd, or Pt. While the resist is still in place, an adhesive metal is plated on the previous conductor metal layer. The adhesive metal may be any one of a number of high temperature alloys that will bond at temperatures exceeding the softening point of the organic layers. Such alloys may include, AuSn, PdSn, NiSn.

[0007] The various layers can be selectively interconnected by small via (also referred to herein as z-axis interconnects or studs) formed in the organic layers at the dimensions down to ten micron using laser or reactive ion etch techniques. Single side copper formation on the underside of the LCP layer serves as a stop during via formation using a laser or mechanical drill. The underside copper also serves as a cathode or bus layer to provide for the formation of the z-axis interconnect or metallic stud to form a 3-D interconnect structure. The studs or z-axis interconnects are formed by electroplating either copper, nickel, gold, silver or similar conductive

metal. The use of electroplating allows for solid via stud formation for improved conductivity.

[0008] After fabrication of the conductive metal stud within an organic layer,
5 the top of the stud is capped with high melting point metallic alloy that bonds to copper (or other metallic conductor material used) to form 3-D interconnection upon lamination of high temperature and low temperature metallized organic layer, such as an LCP or similar organic material layer.

10 BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S)

[0009] Having thus described the invention in general terms, reference will now be made to the accompanying drawings, which are not necessarily drawn to scale, and wherein:

15 [0010] FIGS. 1A-1E are schematic representations of the incremental steps in the fabrication of a multilayer structure in accordance with an embodiment of the present invention.

20 [0011] FIG. 2 is a schematic representation of multiple circuitized layers stacked in an alternating sequence of high and low temperature dielectrics.

[0012] FIG. 3 is a schematic representation of a multilayer circuitized structure including an expansion matched rigidizer embodiment of the present
25 invention.

[0013] FIG. 4 is a schematic representation of a multilayer circuitized structure including high k ceramic particles incorporated into an organic layer, or deposited as a film, in accordance with an embodiment of the present invention.
30

[0014] FIG. 5 is a schematic representation of a multilayer circuitized structure including resistive particles incorporated into an organic layer, or deposited as a resistive film, in accordance with an embodiment of the present invention.

5 [0015] FIG. 6 is a schematic representation of a metalized circuitized structure including high k ceramic particles incorporated into the organic layer or deposited as a film on the organic layer, and a second organic layer including resistive particles incorporated into the second organic layer or deposited as a film on the second organic layer in accordance with an embodiment of the present invention.

10

[0016] FIG. 7 is a schematic representation of a multilayer circuitized structure including layers filled with high k ceramic and resistive particles and/or films deposited with high k ceramic and resistive particles, and a rigidizer layer in accordance with an embodiment of the present invention.

15

[0017] FIG. 8 is a schematic representation of a multilayer circuitized structure illustrating various packaging formats compatible with the present invention.

DETAILED DESCRIPTION

20 [0018] The present inventions now will be described more fully hereinafter with reference to the accompanying drawings, in which some, but not all embodiments of the invention are shown. Indeed, these inventions may be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will
25 satisfy applicable legal requirements. Like numbers refer to like elements throughout.

[0019] The present invention comprises three-dimensional (3-D) multilayer structures having at least one low temperature organic layer and at least one high temperature organic layer that are processed in a parallel fashion that provides for
30 individual layers to be independently fabricated and tested prior to lamination into a multilayer 3-D circuit. Metal to metal bonding is formed by incorporating a high

temperature alloy that melts at a temperature slightly above the fusion point of the low temperature organic layer, but lower in temperature than the high melt point organic layer.

5 [0020] For purposes of the present invention, the organic layer or material may comprise any low cost, high performance organic material, such as polyphenyl ether (PPE) based materials, such as LD621 from Polyclad and N6000 series from Park/Nelco Corporation, Teflon organic from Rogers Corporation, or liquid crystalline polymer (LCP), such as LCP from Rogers Corporation or W.L. Gore &
10 Associates, Inc. These materials provide excellent hermicity and temperature independence, which emulates the performance of ceramic substrates used to construct multilayer ceramic structures.

[0021] Advantageously, the construction of the circuits of the present
15 invention does not require an adhesive or lower melting point dielectric to form the 3-D interconnect. As is known to those skilled in the art, adhesives (which are typically epoxies or polyimides) have dissimilar electrical and mechanical properties that are susceptible to moisture uptake, which degrades performance. In addition, the multilayer 3-D circuits of the present invention are homogeneous (e.g., where the two
20 organic materials have the same thickness, dielectric constant, loss tangent, volume resistivity, matching coefficient of thermal expansion (CTE), and modulus) which is highly desirable for improved performance and design ease in high speed digital and high frequency RF/wireless applications both from an electrical standpoint and mechanical standpoint (e.g., to minimize warpage). From an electrical standpoint, the
25 homogeneous construction provides smoother transitions and signal propagation in the z-axis direction, and facilitates the design of matched impedance networks since the dielectric constant and loss are the same, layer to layer.

[0022] The present invention includes the incorporation of high k and resistive
30 particles in the organic layers and/or the deposition of high k and resistive films, which represents additional advantages in design flexibility in realizing RF circuits

that require RC, LC, and RLC networks. Thus, filters, couplers, duplexers, baluns, mixers, etc. can be integrally fabricated. Such structures are possible because the host matrix material (e.g., filled LCP) is the same as the insulating low temperature and high temperature dielectrics. The low and/or high temperature LCP layer either can

5 be filled with high k dielectric particles or incorporate a high k deposited thin film, which then can be incorporated into the circuit to form embedded decoupling, bandpass filters, low pass filters, baluns, couplers, etc., and baseband circuits such as capacitors, blocking filters, etc. Incorporation of the high k particles may be achieved by introducing a surfactant onto high k particles, such as Barium titanate, lead

10 magnesium nitrate or titanium dioxide to minimize particle clustering, followed by drying and then subsequent introduction in the organic melt prior to drawing and pressing the clad organic layer into finished sheets. The resultant high k layers sandwiched between copper sheets or planes can serve as embedded decoupling layers that can be processed in the multilayer stack for noise suppression and other

15 benefits. The amount of high k particle incorporated into the organic layer will determine the resultant dielectric constant values and mechanical integrity. Typical volume fraction will vary from 10% to 50%. Additionally, high k organic layers that are either deposited or filled enable passive components and arrays that can support applications beyond 6 GHz, and are process compatible for the 3-D multilayer build

20 up described herein. This is achieved, at least in part, by lithographically defining the top and bottom conductor layers to form a parallel plate construction. The filled organic as well as the non-filled organic is sandwich between the lithographically defined top and bottom conductor layers.

25 [0023] The present invention also provides for the incorporation of resistive particles in the organic laminates or the deposition of resistive thin films on organic laminates, which enables passive components and arrays that provide for the formation of RC, and RLC networks. The resistive particles may include, for example, carbon, silicon carbide, ruthenium oxide, copper, silver, or combinations

30 thereof, that can be incorporated into the organic melt up to 50% volume, while resistive thin films could include NiP, TaN, NiCr, NiWP, ZnO, etc. A resistive circuit

is completed upon deposition and circuitization of metal contacts to form terminals, thereby forming planar and annular resistors and resistor networks. In addition, resistor networks are formed by plating, sputtering, evaporating or chemical vapor deposition of metals and/or metallic alloys on finished organic laminates to form low and high value resistors and resistor networks upon circuitization of metallic terminals to form planar and annular resistors and resistor networks. The resistor devices or elements can also be fabricated by laminating, electroplating, vacuum deposition, or printing of resistive films on the organic laminates. Upon putting down the resistive film, a metallic layer is deposited on the resistive film and the resistor and/or resistor networks are defined via a print and etch technique. In defining resistors or resistive networks using filled resistive organic layers, the filled organic layers are metallized either by plating, lamination or vacuum deposition. The conductors can then be lithographically defined to form the metallic terminals of the resistors.

[0024] The thin film of high k or resistive material can be fabricated on an organic layer using known techniques. For example, a layer of high k material can be deposited by CVD or sputtering and then lithographically defined into a desired design. Likewise, a layer of resistive material can be deposited by evaporation, CVS or sputtering and then lithographically defined. In either case, the thickness of the thin film will vary based upon the desired performance characteristics sought.

[0025] A 3-D multilayer circuit in accordance with the present invention can be fabricated in either sequential mode or reel to reel. In a sequential mode, a high temperature uncladded or single sided organic laminate from 1-10 mils in thickness is initially obtained. For the uncladded example, one side is metallized by, for example, sputtering or chemical-electro deposition of a thin conductive film, such as copper, nickel or gold. The other side is then drilled to form a via that terminates at the polymer-metal interface. Upon appropriate surface treatment (e.g., by plasma or chemical etching), the via is then metallized by electroless plating and capped with an adhesive metal, such as gold-tin. The bottom layer, which served as the conductive layer or bus layer, is then circuitized to form a single metal layer circuit. Upon

completion of the circuit, other layers (e.g., alternating layers of high and low melting point material) are combined so that 3-D connections are formed by the vias h/l stackup. The layers are stacked in a lamination press, whose temperature and pressure conditions will vary due to a number of known factors, such as the number of
5 layers and the adhesive metal composition. As an example, the layers may be laminated together in a press applying 75-500 psi at 270-280°C for 5-20 minutes. Within this stack could be one or more high k dielectric layers and resistive layers. The stack is taken up in temperature and pressure and laminated to fuse the low temperature dielectric to the high temperature dielectric, the low temperature
10 dielectric to the metal, and the metal alloy to the trace metal on the organic layer.

[0026] The 3-D metal layer circuit can also be processed onto an expansion matched CTE (coefficient of thermal expansion) core or substrate. The core material and the dielectric material can be tailored to have the same thermal expansivity, which
15 provides for little to no warpage for improved reliability. In addition, the CTE match of core and dielectric can be tailored to that of silicon devices, which can be subsequently joined to the 3-D interconnect in the absence of underfill.

Illustrative Embodiments

20 [0027] The following is an illustrative embodiment of a method of fabricating a multilayer organic structure according to the present invention utilizing LCP as the organic material, followed by several alternative embodiments.

[0028] FIG. 1A is a schematic representation of an uncladded high
25 temperature or low temperature LCP dielectric film 12, in accordance with an embodiment of the present invention. In a preferred embodiment, the high and low temperature LCP film has a CTE between 2 and 20 ppm/°C.

[0029] Next, as illustrated in FIG. 1B, a metalized layer 14 has been
30 fabricated on the high temperature or low temperature LCP dielectric film 12, in accordance with an embodiment of the present invention. Metallization of the LCP

film 12 can be accomplished by electroless and electroplating, sputtering, evaporation, or chemical vapor deposition. Metallization can be an adhesive metal such as copper, chromium, titanium, or platinum, followed by deposition of either copper, nickel, gold, or palladium. The thickness is preferably between 0.5 microns to 200 microns.

[0030] Next, as illustrated in FIG. 1C, the high temperature or low temperature LCP dielectric film 12 that has been drilled either by laser, mechanical, punch, etch, reactive ion etch to form vias 16 down to the underside of the metallization. Suitable lasers include UV, CO₂, excimer, or YAG, and the drilling can be accomplished using computer numeric control (CNC) or using a patterned mask for image transfer.

[0031] As illustrated in FIG. 1D, the metallized vias 16 have been plated, sputtered, or filled with conductive paste or evaporated, to form a conductive via stud 18 within the via 16, followed by the fabrication of an adhesive capping layer 20, which comprises a high melting point alloy that forms metal to metal joining. The solid via studs 18 form the z-axis interconnect between the layer of the stack up, while the adhesive caps 20 serve to form the reliable metal to interconnect bond. The cap is preferably a metallic solder of a binary alloy that melts at a temperature above that of the fusion point of the high temperature and low temperature LCP layers.

[0032] Next, as illustrated in FIG. 1E, the metalized layer 14 fabricated (e.g., printed and etched to form a single sided circuit layer) on either a high temperature or low temperature LCP dielectric film 12 is circuitized (e.g., etched). Circuitization of the LCP sheets can also be accomplished in an additive or semi additive method, where the defined circuit layer is formed by plating through a patterned photoresist. Followed by stripping of the resist and removal of the conductive bus layer used for the electroplating.

[0033] FIG. 2 is a schematic representation of multiple circuitized layers that have been stacked in an alternating sequences of aligned high temperature circuitized dielectric layers 24 and low temperature circuitized dielectric layers 26, which are fusion bonded at temperatures and pressures sufficient enough to form a multilayer flex circuit construction, in accordance with an embodiment of the present invention.

[0034] FIG. 3 is a schematic representation of circuitized layers that have been stacked in alternating sequences of high temperature circuitized dielectric layers 24 and low temperature circuitized dielectric layers 26 with a matched coefficient of thermal expansion (CTE) rigidizer 30, which can be either metallic or other inorganic, and which is fusion bonded to form a multilayer rigid circuit construction. The rigidizer can be disposed above or below the circuitized layers, as shown, or alternatively, the rigidizer can be aligned and placed between circuitized layers, where the circuit layers are stacked on either side of the rigidizer, followed by lamination of the entire stack up to form a multilayer rigidized circuit construction. Depending on the material comprising the rigidizer, it can also serve as a heat sink, ground or power plane, or EMI shielding. Examples of suitable materials include copper-invar-copper (CIC) or aluminum silicon carbide.

[0035] FIG. 4A is a schematic representation of circuitized layers that have been stacked in alternating sequences of high temperature circuitized dielectric layers 24 and low temperature circuitized dielectric layers 26 with an LCP layer 40 filled with high k ceramic particles. Alternatively, a high k film 40' can be deposited on LCP layer, as shown in FIG. 4B. The LCP layer 40 is fusion bonded in the multilayer stackup and circuitized to form a multilayer flex circuit construction with embedded inductors and capacitors in accordance with an embodiment of the present invention.

[0036] FIG. 5A is a schematic representation of circuitized layers that have been stacked in alternating sequences of high temperature circuitized dielectric layers 24 and low temperature circuitized dielectric layers 26 with an LCP film 42 filled with resistive particles. Alternatively, a resistive films 42' (such as NiCr, TaN, NiP,

or NiWP) can be deposited on the LCP layer as illustrated in FIG. 5B. The LCP layer is fusion bonded to form a multilayer flex circuit construction with embedded resistors (R), inductors (L) and capacitors (C).

5 [0037] FIG. 6 is a schematic representation of circuitized layers that have been stacked in alternating sequences of high temperature circuitized dielectric layers 24 and low temperature circuitized dielectric layers 26 that includes a layer 44 that includes a deposited high k dielectric film or is LCP filled with high k ceramic particles, and in a separate discrete level of the stack, a layer 46 that includes a
10 deposited resistive film 46 or is filled LCP with resistive particles, wherein the stack is fusion bonded to form a multilayer flex circuit construction with embedded R, L and C's.

[0038] FIG. 7 is a schematic representation of a rigid multilayer circuit of
15 FIG. 6 with a metallic, inorganic or organic rigidizer 50. The rigidizer 50 can be located on either side of the multilayer circuit stackup or within the multilayer stack up to form a rigid multilayer circuit construction with embedded components such as R, L, and C's. Through vias that are filled with plated copper or conductor paste can be used to connect circuit layers on opposite sides of the rigidizer. The multilayer
20 substrate or module can be used for interconnecting a vast array of active and passive components either through direct attached methods or surface mount technologies.

[0039] The multilayer 3D interconnect structure described herein can support the packaging and interconnection of various active and passive components in
25 addition to the passive components embedded in the structure to form functional modules or system boards for digital, RF/wireless, or mixed signal modules. The ability to tailor the expansion of the multilayer circuit, described above, enables the packaging of different active chips such as silicon CMOS, SoI, SiGe, GaAs, and surface mount passive components in a highly reliable platform. For example, FIG. 8
30 is a schematic representation of a multilayer circuitized structure including various illustrative packaging formats supported by the present invention. Suitable packaging

formats include, but are not limited to, flip-chip, wafer level packages (WLP), chip scale packages (CSP), ball grid array (BGA), wire bonded devices and various surface mount devices (SMD or SMT).

5 [0040] The formats illustrated in FIG. 8 include cavity flip chip or wirebond
70, flip chip wafer level packaging 72, BGA/CSP 74, SMD/SMT 76 and wire bond
78. The chips and/or package components 80 can be attached on a top surface of the
multilayer circuit or within cavities formed inside the multilayer circuit using routing,
10 punching, laser machining or other standard processes known to those skilled in the
art. These cavities can be single level or multilevel and can be interconnected to other
circuit layers using microvias or plated through holes. Using microvias 82 and plated
through holes 84, the packaged components 80 on the top side of the module or in
cavities can be interconnected to each other, to the embedded passive layers that
15 include capacitors, inductors, resistors, etc., or to the BGA pads 80 on the bottom side
of the module. The side walls of the module substrate can be covered with conductor
like Cu, Ni, Au or other absorbing materials to provide shielding from EMI and other
external radiation. This shielding can be formed with electroless and electroplating,
vacuum deposition, lamination or other deposition methods known to those skilled in
the art. The assembled multilayer module substrate can form a system board for a
20 system or can be terminated with ball grid array on the bottom side or wirebonded
from the top side for further interconnection to other components on a system board.

[0041] Many modifications and other embodiments of the inventions set forth
herein will come to mind to one skilled in the art to which these inventions pertain
25 having the benefit of the teachings presented in the foregoing descriptions and the
associated drawings. Therefore, it is to be understood that the inventions are not to be
limited to the specific embodiments disclosed and that modifications and other
embodiments are intended to be included within the scope of the appended claims.
Although specific terms are employed herein, they are used in a generic and
30 descriptive sense only and not for purposes of limitation.

THAT WHICH IS CLAIMED:

1. A method of fabricating 3-D multilayer interconnect structures,
comprising;
5 providing a first single sided circuitized layer of a first melting point having a
first conductive layer;
providing a second single sided circuitized layer of a second melting point
including at least one metal filled z-axis via connection stud;
capping the z-axis stud of the second organic layer with a high temperature
10 bonding material; and
bonding the low temperature organic layer to the high temperature organic
layer;
wherein the first organic layer forms a fusion bond with the second organic
layer, and the cap on the second organic layer forms a metal to metal bond with the
15 conductive layer first organic layer.
2. The method of claim 1, wherein the conductive layer comprises at least
one of copper, aluminum, gold, nickel, iron, silver, zinc, chromium and a combination
thereof.
20
3. The method of claim 1, wherein at least one conductive layer on one of
the low temperature and high temperature organic layers serves as a bus layer prior to
the z-axis via stud formation.
- 25 4. The method of claim 1, wherein the first melting point is less than the
second melting point.
5. The method of claim 1, wherein the first melting point is greater than
the second melting point.
30

6. The method of claim 1, wherein the cap on the vias of the second organic LCP layer is a metallic solder of a binary alloy that melts above a fusion point of the first and second organic layers.

5 7. The method of claim 1, wherein the first conductive layer has a thickness from approximately 0.5 microns to 200 microns.

8. The method of claim 1, wherein the first and second organic layers are laminated together in a stack to form a three-dimensional (3-D) circuit.

10

9. The method of claim 8, wherein the 3-D circuit is a flexible circuit.

10. The method of claim 8, wherein the 3-D circuit is a rigid circuit.

15 11. The method of claim 8, wherein the coefficient of thermal expansion of the completed 3-D circuit in the x and y directions are substantially matched.

12. The method of claim 8, wherein the coefficient of thermal expansion of the first and second organic layers is between 2 and 20 ppm/°C.

20

13. The method of claim 1, wherein the second organic layer is sufficiently filled with high k dielectric constant particles to achieve a suitable high k film for high value capacitors and resonator structures.

25 14. The method of claim 1, wherein the second organic layer includes a thin film of high k dielectric constant material.

15. The method of claim 1, wherein the second organic layer is sufficiently filled with resistive particles and circuitized to form a resistor or a resistor network.

30

16. The method of claim 1, wherein the second organic layer includes a thin film of resistive material.

17. The method of claim 1, further comprising an expansion matched core
5 that is bonded to one of the first or second organic layers to provide expansion matching to one of an organic, ceramic and metal substrates.

18. The method of claim 1, wherein the expansion matched core is metallic, and performs thermal and electrical functions.

10

19. A multilayer liquid crystalline polymer circuit; comprising
low temperature liquid crystalline polymer layer (LCP) having a single
circuitized surface;
high temperature liquid crystalline polymer layer having a single circuitized
15 surface;
at least one z-axis interconnect structure interconnecting the circuitized
surfaces of the low temperature and high temperature LCP layers.

20. The circuit of claim 19, wherein at least one of the low temperature
20 and high temperature LCP layers comprises at least one of high k particles and resistive particles.

21. The circuit of claim 19, wherein one of the low temperature and high
temperature LCP layers includes a z-axis via aligned in the z-axis with one of the z-
25 axis interconnect structure.

METHODS FOR FABRICATING THREE-DIMENSIONAL ALL ORGANIC INTERCONNECT STRUCTURES

ABSTRACT

5 The present invention comprises methods for making three-dimensional (3-D)
liquid crystalline polymer (LCP) interconnect structures using a high temperature
single sided liquid crystalline polymer, and low temperature single sided liquid
crystalline polymer, whereas both the high temperature LCP and the low temperature
LCP are drilled using a laser or mechanical drill or mechanically punch to form a z-
10 axis connection. The single sided Conductive layer is used as a bus layer to form z
axis conductive stud conductive stud within the high temperature and low
temperature LCP, followed by deposition of a metallic capping layer of the stud that
serves as the bonding metal between the conductive interconnects to form the z-axis
electrical connection. High temperature and low temperature LCP circuit layers are
15 etched or built up to form circuit patterns and subsequently bonded together to form
final 3-D multilayer circuit pattern whereas the low temperature LCP melts to form
both dielectric to dielectric bond to high temperature LCP circuit layer, and dielectric
to conductive bond, whereas, metal to metal bonding occurs with high temperature
metal capping layer bonding to conductive metal layer. The resultant structure is then
20 packaged using two metallized organic cores that are laminated onto either side of the
device using a low temperature adhesive with similar electrical properties and
subsequently metallized to form the input output terminals and EM shielding.

25

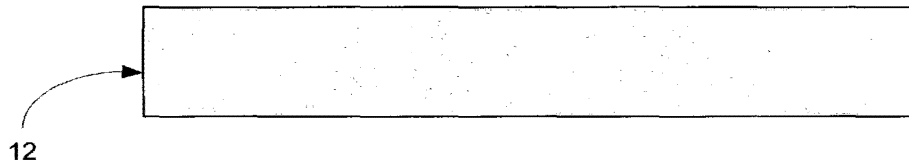


FIG. 1A

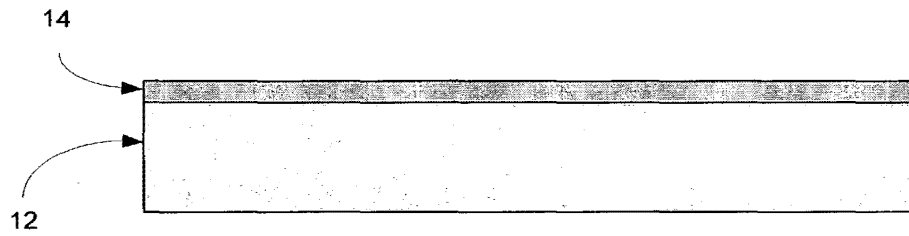


FIG. 1B

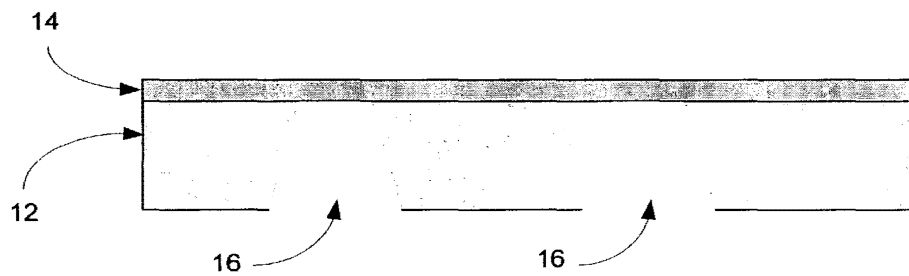


FIG. 1C

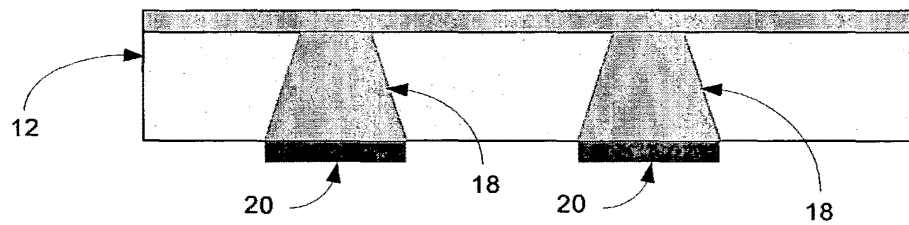


FIG. 1D

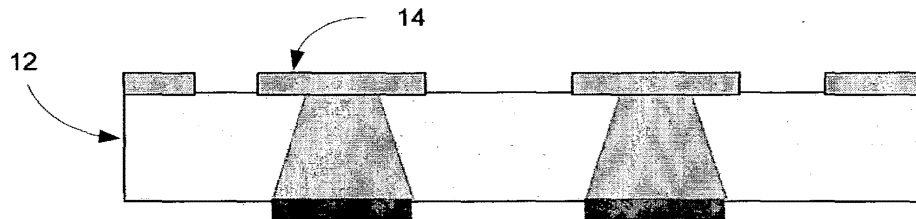


FIG. 1E

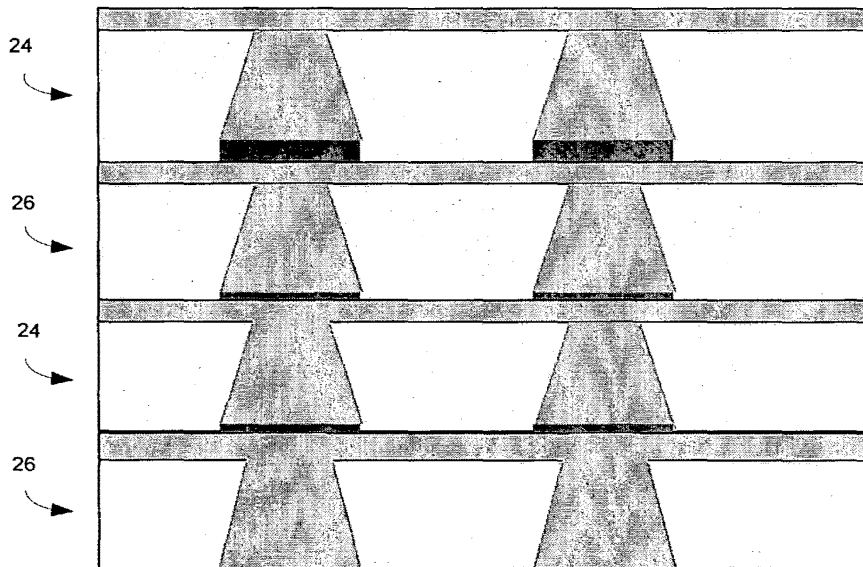


FIG. 2

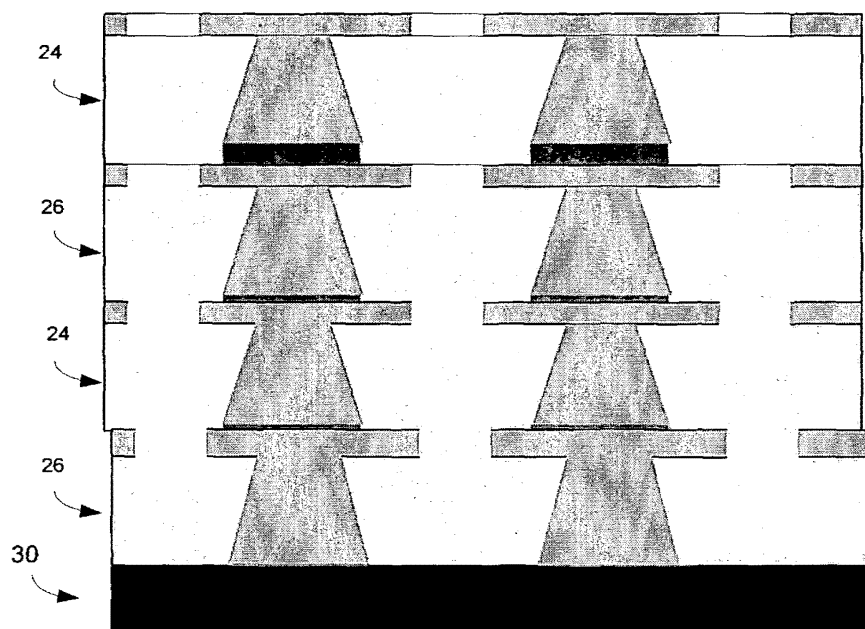


FIG. 3

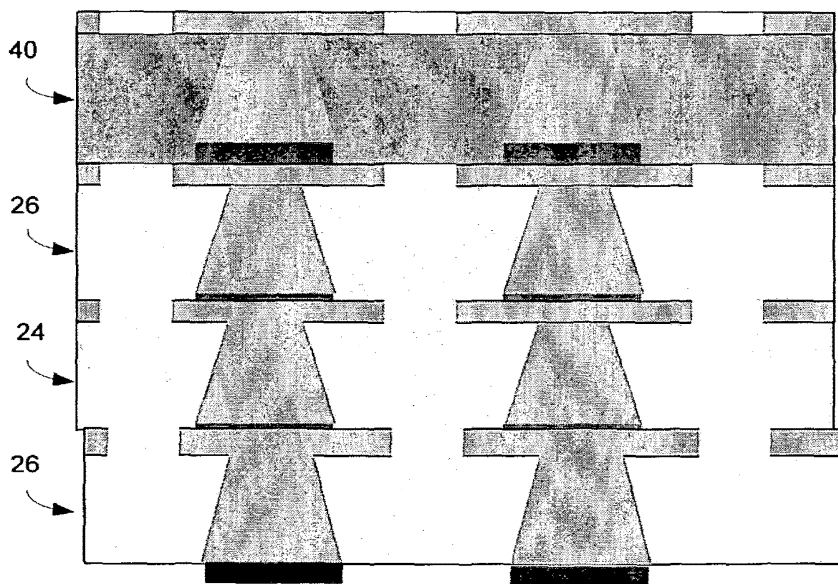


FIG. 4A

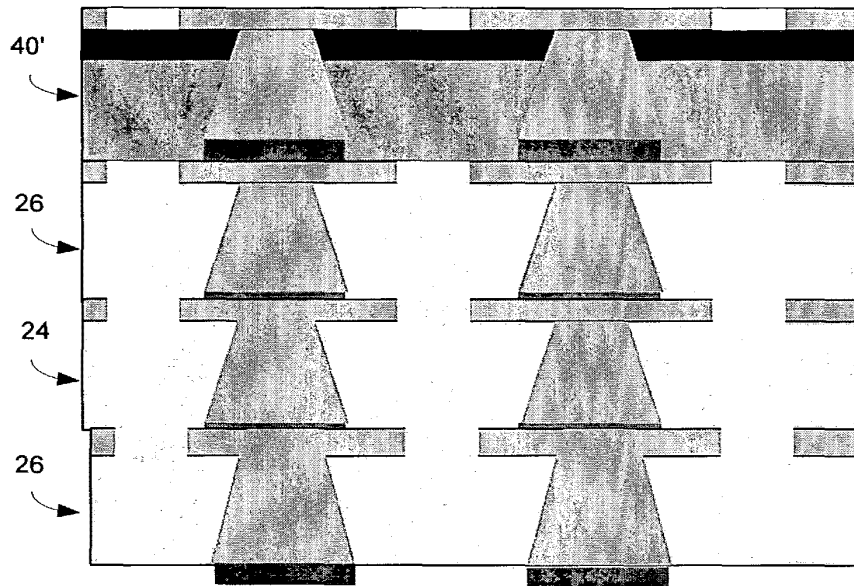


FIG. 4B

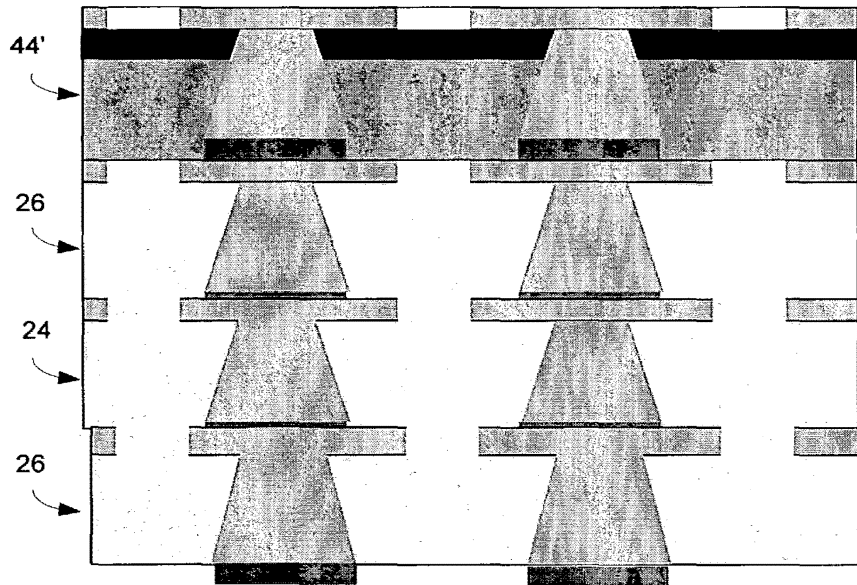


FIG. 5B

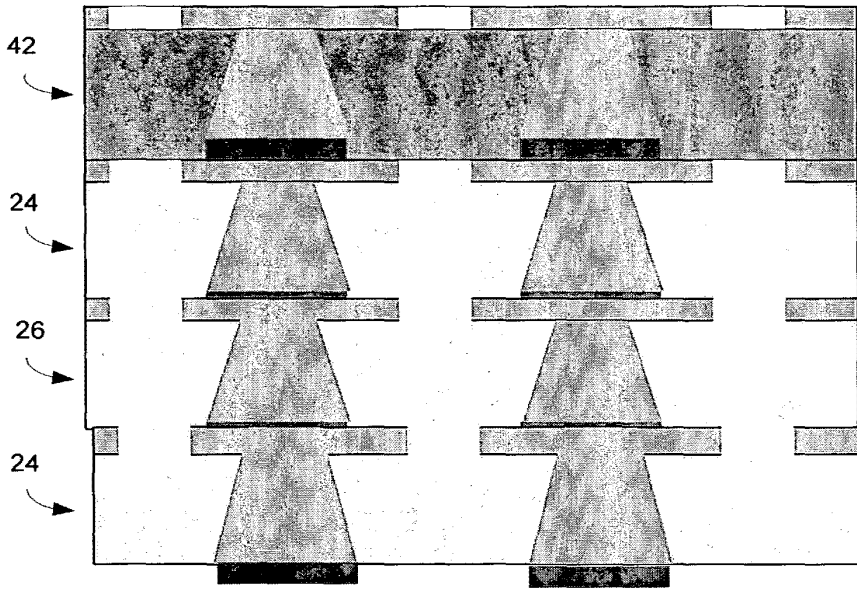


FIG. 5

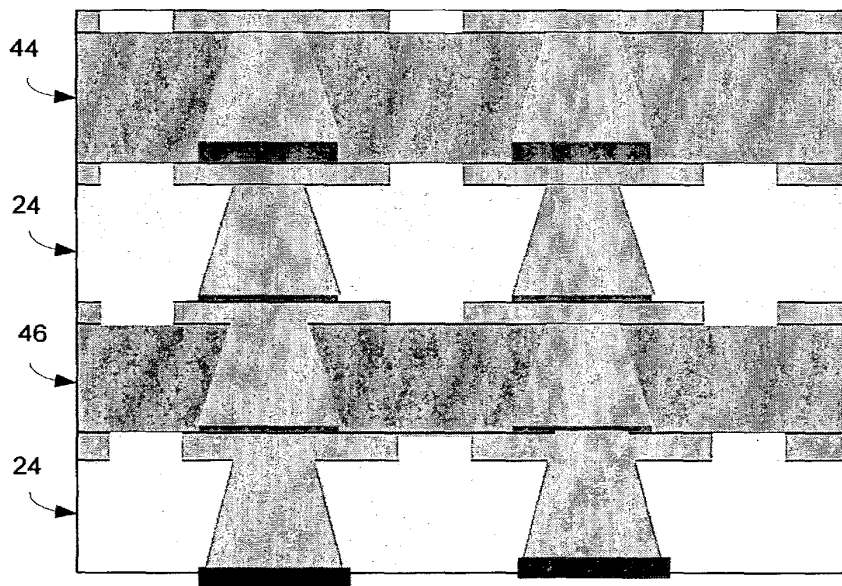


FIG. 6

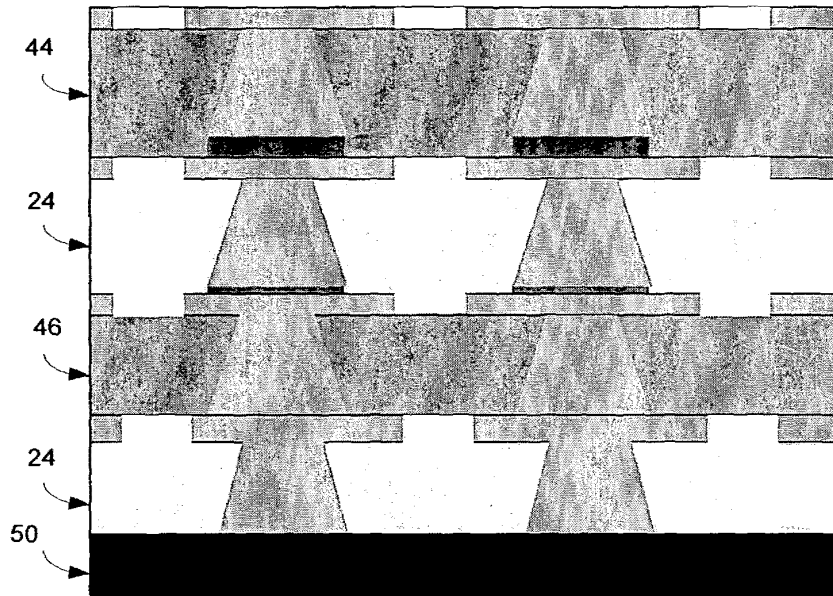


FIG. 7

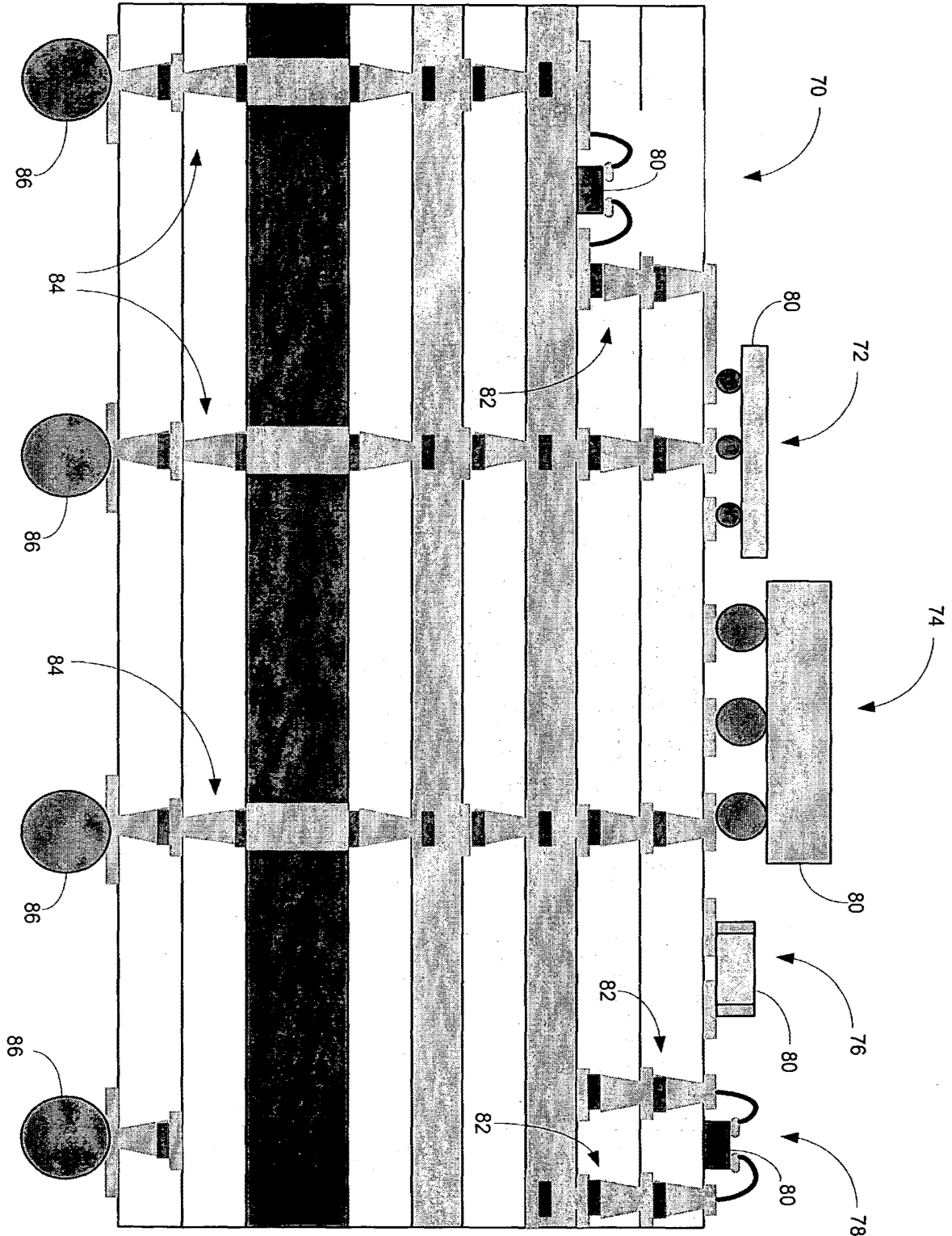


FIG. 8

**U.S. Application No.
10/405,024 filed 3-28-2003**

03/28/03



JC904 U.S. PTO

03-31-03 10405024 032803

UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR 1.53(b))	Attorney Docket No.	17625-0040
	Named Inventor(s)	White, et al.
	Title	Stand-Alone Organic-Based Passive Devices
	Express Mail Label No.	EV048621794US

APPLICATION ELEMENTS	ADDRESS TO: Assistant Commissioner for Patents Box Patent Application Washington, DC 20231
1. ☒ Fee Transmittal Form <i>(Submit an original, and a duplicate for fee processing)</i> 2. ☒ Applicant claims small entity status. See 37 CFR 1.27. 3. ☒ Specification, Claims, and Abstract Total Pages 52 4. ☒ Drawings Total Sheets 20 5. Oath or Declaration Total Pages 3 a. ☒ Newly executed (original or copy) b. ☐ Copy from prior application (37 CFR 1.63(d)) <i>(for continuation/divisional with Box 19 completed)</i> (i) ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b). 6. ☐ Incorporation by Reference <i>(usable if Box 5b is checked)</i> The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 5b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein. 7. ☐ Nonpublication Request Under 35 U.S.C. 122(b)(2)(B)(i). ☐ Form PTO/SB/35 8. ☐ Application Data Sheet. See 37 CFR 1.76 9. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix)	10. ☐ Nucleotide and/or Amino Acid Sequence Submission <i>(if applicable, all necessary)</i> a. ☐ Computer Readable Form (CRF) b. ☐ Specification Sequence Listing on: i. ☐ CD-ROM or CD-R (2 copies); or ii. ☐ paper c. ☐ Statement verifying identity of above copies 11. ☒ Assignment: a. ☒ Assignment Papers (cover sheet & document(s)) b. ☐ Assignment is of record in parent application No. 12. ☐ 37 CFR 3.73(b) Statement <i>(when there is an assignee)</i> ☐ Power of Attorney by assignee 13. ☐ English Translation Document <i>(if applicable)</i> 14. ☒ Information Disclosure Statement (IDS) PTO-1449 ☒ Copies of IDS Citations (62 references) 15. ☐ Preliminary Amendment 16. ☒ Return Receipt Postcard (MPEP 503) <i>(Should be specifically itemized)</i> 17. ☐ Certified Copy of Priority Document(s) 18. ☐ Other:
19. If a CONTINUING APPLICATION , check appropriate box and supply the requisite information and in a preliminary amendment, or in an Application Date Sheet under 37 CFR 1.76: ☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: Prior application information: Examiner: Group Art Unit: Recite complete dependency back to first parent application:	
20. CORRESPONDENCE ADDRESS: Malvern U. Griffin III SUTHERLAND ASBILL & BRENNAN LLP 999 Peachtree Street, NE Atlanta, Georgia 30309-3996 By: <u>Malvern U. Griffin III</u> Reg. No. 38,899 Date: March 28, 2003 Telephone: 404-853-8000 Facsimile: 404-853-8233	

I hereby certify that this correspondence is being deposited with the United States Postal Service in an Express Mail envelope (EV048621794US) addressed to: Assistant Commissioner for Patents, Washington, D.C. this 28th day of March 2003.

Malvern U. Griffin III

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PATENT TRADEMARK OFFICE

AO 885815.1

EX1040 / Page 82 of 165
Murata Manufacturing Co., Ltd.

JC857 U.S. PTO
10/405024
03/28/03

FEE TRANSMITTAL

Attorney Docket No. 17625-0040

This sheet accompanies a patent application transmittal for the following application:

Inventor(s): White, et al.

Filing Date: March 28, 2003

Serial No.:

Title: Stand-Alone Organic-Based Passive Devices

The filing fee is calculated as shown below:

1. FILING FEE:

SMALL ENTITY			LARGE ENTITY	
FOR:	FEE	FEE PAID	FEE	FEE PAID
☒ UTILITY FILING FEE	\$375	\$375	\$750	
☐ DESIGN FILING FEE	\$165		\$330	
☐ PLANT FILING FEE	\$260		\$520	
☐ REISSUE FILING FEE	\$375		\$750	
☐ PROVISIONAL FILING FEE	\$80		\$160	
SUBTOTAL (1)		\$375		

2. CLAIMS:

SMALL ENTITY				LARGE ENTITY		
FOR:	NO. FILED	NO. EXTRA	RATE	FEE	RATE	FEE
TOTAL CLAIMS	35 - 20 =	15	x 9 =	\$135	x 18 =	
INDEP. CLAIMS	5 - 3 =	2	x 42 =	84	x 84 =	
☐ MULTIPLE DEPENDENT CLAIM PRESENTED			+140 =		+280 =	
SUBTOTAL ()				\$219		

3. ADDITIONAL FEES:

SMALL ENTITY			LARGE ENTITY	
FOR:	FEE	FEE PAID	FEE	FEE PAID
☐ LATE FILING, FEE OR OATH	\$65		\$130	
☐ NON-ENGLISH SPECIFICATION	\$130		\$130	
☐ OTHER				
SUBTOTAL (3)		0		

TOTAL FILING FEES: \$594

A check is enclosed for the total amount: \$594

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Date: March 28, 2003

5

10 STAND-ALONE ORGANIC-BASED PASSIVE DEVICES

CROSS-REFERENCE TO RELATED APPLICATION

15 [0001] This application claims benefit of co-pending U.S. Provisional Application No. 60/391,742, filed June 26, 2002, which is entirely incorporated herein by reference. In addition, this application is related to the following co-pending, commonly assigned U.S. applications, each of which is entirely incorporated herein by reference: "Methods for Fabricating Three-Dimensional All Organic Interconnect Structures" filed March 28, 20 2003, and accorded Application No. _____; and "Integrated Passive Devices Fabricated Utilizing Multi-Layer, Organic Laminates" filed March 28, 2003, and accorded Application No. _____.

25

TECHNICAL FIELD

[0002] The present invention is generally related to integrated passive devices formed as discrete components for use on circuit boards and, more particularly, is related to multilayer organic passive devices, such as inductors, for use in broadband

applications.

BACKGROUND OF THE INVENTION

5 [0003] Integrated circuit technology is very advanced in the area of discrete surface mount passive components (i.e., resistors, capacitors, and inductors). For example, this technology is very popular in mixed signal designs, such as, for portable wireless electronics and other devices in which digital and radio frequency (RF) circuits are combined into mixed signal modules. However, as the size of electronic devices
10 decreases, it has become increasingly important for designers to optimize the available real estate on mixed signal chip modules. For instance, in some mixed signal designs, off-chip passive components use more real estate on the boards than the analog and digital signal processing units. By providing smaller passive components, designers may more efficiently use available real estate on boards or reduce the size of the boards
15 themselves. Therefore, the development of relatively smaller passive components suitable for mounting to printed wiring boards has become increasingly important.

[0004] The use of existing systems and methods for implementing integrated passive components, however, may be problematic for several reasons. It is important to
20 model the behavior of passive components, which are constituents in critical components such as filters, couplers, phase locked loops, etc., extremely accurately and in a reasonable processing time. The trade off of speed versus accuracy is one that has always plagued designers. Accordingly, it is a goal of the design community to develop solutions that are fast and accurate for modeling integrated components. Besides the
25 difficulty in modeling integrated passives, the presence of severe parasitic effects in silicon-based RF IC's makes the design of high Q reactive components difficult. Q factor refers to the measure of "quality" of a particular frequency response. Therefore, it is advantageous to design integrated passive components having a high Q. Low temperature co-fired ceramic (LTCC) technology for multi-chip modules (MCMs) used

in RF and wireless systems is one solution to this design problem of designing high Q integrated passive components. However, LTCC is an extremely expensive process to implement for consumer applications because of the complexity of the high-temperature fabrication process and/or the expense of the ceramic materials used in the substrates.

5

[0005] With specific regard to inductors, they form an integral part of filters, resonators, baluns, matching networks and bias networks. Inductors are commercially available as off-chip discrete components fabricated using multilayer ceramic substrates. Their construction generally has been limited to multilayer ceramic substrates because the ceramic materials used are resilient to moisture and temperature and show little variation with these parameters, which is imperative for inductors used in high frequency applications. There are essentially three types of ceramic inductors that are available in discrete form: winding internal construction, multilayer ceramic, thin film. The general properties of these inductors are provided below in Table 1.

10
15

Structure	Features	Suitable applications	Sizes
Winding Internal Construction	High Q; Large current capacity (750mA); low tolerance (>25% variance), low yield; Physically large	IF Impedance matching; RF Oscillation circuit; IF Choke; Circuits where large currents flow; Circuits where high Q characteristics	(2.0x1.5mm) to (3.2x1.6mm)
Multilayer Ceramic	Low current capacity (450mA); Inexpensive; Good high-frequency-range characteristics	RF/IF impedance matching; RF oscillation circuit; RF choke	(1.0x0.5mm) to (1.6x1.8mm)
Thin Film	Physically small and thin; low current capacity (450mA); Low L deviation; Good high-frequency-range characteristics; high tolerance (2- 5% variance); high yield; Expensive	RF/IF Impedance matching; RF Oscillation circuit; RF Choke; Circuits requiring tight inductance tolerance	(0.6x0.3mm) to (1.0x0.5mm)

Table 1: Prior Art Ceramic Inductors

[0006] None of the above-noted inductor designs provides a suitable combination
5 of low cost, high yield, and high current. In addition, these designs do not provide in-
built shielding, and therefore, if shielding is desired it must be added once mounted to the
circuit board, typically in the form of a can or by adding references adjacent or below the
device, which adds to the complexity of modeling the device (e.g., reduces quality
factor). Alternatively, modeling the component and then modeling the circuit board with
10 the component is very complex, as discussed in Wang et al., "A Full-Wave Analysis
Model for Uniplanar Circuits With Lumped Elements," IEEE Transactions on
Microwave Theory and Techniques, Vol. 51, No. 1, pp. 207-215, January 2003.

[0007] Additionally, the high temperatures associated with the processing of ceramic-based inductors adds process complexity and thereby increases cost.

Commercial manufactures currently utilize an automated system for a 5" x 5" wafer.

5 Although the use of ceramic substrates for packages with embedded components and attached chips has been performed, it currently cannot be used for the replacement of an entire board for commercial wireless applications. LTCC modules are almost always mounted on a larger ceramic carrier, which is generally processed using organic thin-film laminate technology, which is currently automated for 18" x 24" wafers. This involves
10 three levels of packaging, which is relatively expensive compared to other prior art inductors.

[0008] As an alternative to ceramic-based designs, organic materials have been utilized with varying degrees of success. The loss tangent for the dielectrics used in

15 organic processes is typically anywhere from 0.02 for epoxy-based materials to as low as 0.0005 for teflon-based materials. Cost is crucial for widespread acceptance of a material, and epoxy-glass laminate is the lowest cost material and consequently holds a large market share in package substrates and printed wiring boards. However, these organic dielectrics exhibit frequency dependent electrical behavior that is not suitable for
20 broadband applications. Additionally, they have high moisture uptake and show high variance with temperature. On the other hand, materials such as teflon based composites, which exhibit resilience to temperature and moisture, are expensive and difficult to process. For example, currently the hardness of the teflon based composites, such as polytetra flouroethylene (PTFE), makes it difficult to fabricate small vias and through
25 holes for selectively defining intra-layer connectivity because the PTFE melts from the high concentration of heat generated by the mechanical drill and then shatters. In addition, it is currently difficult to make multilayer structures out of PTFE because of its inertness. Those multilayer structures that comprise PTFE do not include layer-to-layer

selective interconnectivity, but rather, are limited to through holes that extend from the top layer to the bottom layer.

[0009] Thus, there is a need in the industry for low-cost, high performance
5 inductors for use in broadband applications.

SUMMARY OF THE INVENTION

[0010] The present invention provides for low cost, and if desired high
10 performance, discrete inductor devices in an all organic platform. The integrated passive devices (IPDs) of the present invention utilize a low cost organic material such as liquid crystalline polymer (LCP) or polyphenyl ether (PPE) in a multilayer structure, wherein the organic materials have low moisture uptake and good temperature stability. Each layer may be metalized on one or both sides and selectively interconnected by vias
15 formed in the respective layers so as to form winding or coiled inductors. Utilizing photolithographic techniques, tolerances within 2% can be obtained, with inductances of 0.1 nH and greater can be achieved with unloaded Qs from 30-700 at frequencies in the megahertz to multiple gigahertz range. The passive devices may advantageously utilize novel hybrid topologies (e.g., coplanar waveguide (CPW)/stripline or CPW/microstrip),
20 which reduce the number of processing steps, can be sealed to an 18" x 24" wafer, and provide in-built shielding. In certain embodiments, external shielding formed by metalizing the side walls is utilized. The passive devices can be configured for either ball grid array (BGA)/chip scale package (CSP) or surface mount device (SMD) mounting to circuit boards.

25

[0011] Briefly described, an embodiment of the present invention as a stand-alone inductor device for mounting to a circuit board comprises a first conductive layer, a first substrate layer comprising an organic material formed on a first surface of the first conductive layer, a second conductive layer formed on a first surface of the first substrate

layer and comprising an inductor, which exposes portions of the first substrate layer, a bond ply layer formed on the second conductive layer and exposed portions of the first substrate layer, a second substrate layer comprising a second organic material formed on the bond ply layer opposite the second conductive layer and first substrate layer, and a
5 third conductive layer formed on a first surface of the second substrate layer opposite the second conductive layer.

[0012] The inductor can be configured in a hybrid coplanar waveguide/stripline topology. The first conductive layer and third conductive layer can operate as ground
10 references for the transmission line, and the inductor may comprises shielding on at least two opposite sides of the inductor, wherein the side shielding is in-built or external. The first organic material and the second organic material can comprise one of liquid crystalline polymers, polyphenyl ether-based materials and hydrocarbon composites, and epoxy/glass composites. Further, the second conductive layer comprises a layer of
15 conductive material having a substantially uniform thickness greater or equal to 5 microns, and the total thicknesses of the first and second substrate layers can be greater than approximately 5 mils.

[0013] In accordance with another embodiment of the present invention, a
20 discrete inductor device for mounting to a circuit board comprises a first conductive layer, a first substrate layer comprising an organic material formed on a first surface of the first conductive layer, a second conductive layer formed on a first surface of the first substrate layer and comprising an inductor, which exposes portions of the first substrate layer, a bond ply layer formed on the second conductive layer and exposed portions of
25 the first substrate layer, a second substrate layer comprising a second organic material formed on the bond ply layer opposite the second conductive layer and first substrate layer, shielding on at least two opposite sides of the inductor device, and wherein the inductor is configured in a coplanar waveguide/microstrip topology. The side shielding can be in-built or external, and the first conductive layer and third conductive layer

operate as ground references for the transmission line. The first organic material and second organic material can comprise one of liquid crystalline polymers, polyphenyl ether-based materials and hydrocarbon composites, and epoxy/glass composites. The second conductive layer can comprise a layer of conductive material having a substantially uniform thickness of between 15 microns to 50 microns, and the thicknesses of the first and second substrate layers can be greater than approximately 20 mils. Lastly, the first conductive layer and shielding can operate as ground references for the transmission line.

10 [0014] In accordance with another embodiment of the present invention, a stand-alone inductor device comprises a device component comprising a first organic substrate on which at least one inductor is formed, a first core layer of organic material adjacent the device component, and side shielding on at least two sides of the inductor to provide a single ground reference. The stand-alone inductor can further comprise a second core layer disposed adjacent the device component, opposite the first core layer. The device component layer can comprise a plurality of organic substrates bonded together, wherein each organic substrate includes at least one inductor, wherein at least two of the plurality of organic substrates are electrically interconnected by a via. The stand-alone inductor can further comprise a second device component comprising a second organic substrate on which at least a second inductor is formed, the second device component is disposed adjacent the core layer, opposite the device layer. The device component and second device component can be electrically connected by a via in the core layer. The side shielding can comprise external layers of conductive material, or alternatively, the side shielding can comprise in-built layers of conductive material fabricated on the same plane as the inductor.

[0015] In accordance with another embodiment of the present invention, a method for fabricating a stand-alone inductor device comprises fabricating a wafer comprising a plurality of all organic inductor devices, at least one inductor device

comprising a device component including a first organic substrate on which at least one inductor is formed, and a first core layer of organic material adjacent the device component. The method further comprise forming trenches along two opposing sides of at least one inductor device integrated in the wafer, metalizing the trenches, and
5 singulating the inductor devices so as to form stand-alone inductor devices with external side shielding formed from the metallization of the trenches.

[0016] In accordance with another embodiment of the present invention, a method for fabricating a stand-alone inductor device comprises fabricating a wafer
10 comprising a plurality of all organic inductor devices, at least one inductor device comprising a device component including a first organic substrate on which at least one inductor is formed, in-built side shielding on at least two sides of an inductor integral the inductor device. The method further comprises a first core layer of organic material adjacent the device component, forming trenches along two opposing sides of at least one
15 inductor device integrated in the wafer, and singulating the inductor devices so as to form stand-alone inductor devices.

[0017] Other systems, methods, features, and advantages of the present invention will be or become apparent to one with skill in the art upon examination of the following
20 drawings and detailed description. It is intended that all such additional systems, methods, features, and advantages be included within this description, be within the scope of the present invention, and be protected by the accompanying claims.

25 BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The invention can be better understood with reference to the following drawings. The components in the drawings are not necessarily to scale, emphasis instead being placed upon clearly illustrating the principles of the present invention. Moreover, in the drawings, like reference numerals designate corresponding parts throughout the

several views.

[0019] FIG. 1 is a schematic illustration of an embodiment of an all organic integrated passive device according to an embodiment of the present invention.

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[0020] FIGS. 2A-C are cross-sectional views of three illustrative embodiments of the packaging of a multi-layer organic structure according to an embodiment of the present invention.

10 [0021] FIGS. 3A-3D are cross-sectional views of hybrid topologies of a multi-layer structure according to the present invention.

[0022] FIG. 4 is a cross-sectional view of an inductor device in accordance with an embodiment of the present invention.

15

[0023] FIG. 5 is a top plan view of a wafer having a plurality of inductor devices in accordance with an embodiment of the present invention integrally formed therein, said inductor devices configured for surface mounting to a circuit board.

20 [0024] FIG. 6 is a stand-alone inductor device in accordance with an embodiment of the present invention, which may have been singulated from the wafer of FIG. 5.

[0025] FIG. 7 is an exploded view of the inductor device of FIG. 6.

25 [0026] FIG 8 is a top plan view of a wafer having a plurality of inductor devices in accordance with an embodiment of the present invention that are integrally formed therein, said inductor devices configured for BGA/CSP mounting to a circuit board.

[0027] FIG. 9 is a stand-alone inductor device in accordance with an embodiment of the present invention, which may have been singulated from the wafer of FIG. 8.

[0028] FIG. 10A-10B are exploded views of the inductor device of FIG. 9 with
5 external shielding and in-built shielding, respectively.

[0029] FIGS. 11A-11D are illustrative conductor configurations suitable for incorporation in an inductor device according to the present invention.

10 [0030] FIGS. 12A-12B are process flow diagrams illustrating low-cost, all organic fabrication processes according to the present invention.

[0031] FIG. 13 is a block diagram illustrating an implementation of an embodiment of an integrated passive components design/optimization system according
15 to an embodiment of the present invention for designing, modeling, and/or optimizing integrated passive components.

[0032] FIG. 14 is a flow chart illustrating an example of the architecture, operation, and/or functionality of the integrated passive components design/optimization
20 system of FIG. 13.

[0033] FIG. 15 illustrates an example of an integrated passive component which may be designed, modeled, and/or optimized using the integrated passive components design/optimization system of FIGS. 13 and 14.
25

[0034] FIG. 16 illustrates a coupled-line representation of the integrated passive component of FIG. 15.

[0035] FIG. 17 illustrates a mathematical representation of two symmetric,

lossless, coupled lines for the integrated passive component represented in FIGS. 15 and 16.

[0036] FIG. 18 is a schematic illustration of the coupling of two one-port loop
5 inductors.

[0037] FIG. 19 is a graphical illustration of the modeling responses obtained for the two 1-port loop inductors of FIG. 18 as a two-port response.

10

DETAILED DESCRIPTION

I. Organic Substrate for Integrated Passive Components

[0038] FIG. 1 is a schematic illustration of an embodiment of an all organic
15 integrated passive device 100 packaged in a stand-alone configuration in accordance with an embodiment of the present invention. The device 100 comprises a device component 102 sandwiched between two shielding and packaging components 104. The device component 102 may comprise a single layer or multiple layers of low cost, high performance organic material metalized on one or both sides to form one or more passive
20 devices, such as inductors, as discussed in more detail below. The shielding and packaging components 104 may comprise external shielding, particularly if the device component 102 does not provide in-built shielding, and/or one or more relatively thick and rigid structural layers, also referred to as core layers. The shielding and packaging layer 104 may comprise a single layer or multiple layers of material, as discussed in more
25 detail below.

[0039] As will be understood with reference to the description that follows, the all-organic device 100 enables the design and fabrication of very low-cost stand-alone passive devices, such as inductors having a high Q factor. As described in more detail

below, the integrated passive device or devices of the device component 102 are preferably configured in a hybrid topology, such as a coplanar waveguide (CPW) microstrip, or a CPW stripline, in accordance with the present invention.

5 [0040] The organic material utilized in at least some of the layers of the device component 102 may comprise any low cost organic material, though preferably a low cost, high performance organic material. By way of example, the layers may comprise any of the following types of organic materials: polyphenyl ether (PPE) based materials, such as LD621 from Polyclad and N6000 series from Park/Nelco Corporation, liquid
10 crystalline polymer (LCP), such as LCP from Rogers Corporation or W.L. Gore & Associates, Inc., hydrocarbon composites, such as 4000 series from Rogers Corporation., and epoxy-based laminates, such as N4000 series from Park/Nelco Corp. These materials provide excellent hermiticity and temperature independence, which emulates the performance of ceramic substrates used to construct multilayer ceramic components such
15 as the inductors mentioned in Table 1.

[0041] FIG. 2A illustrates a cross-sectional view of an embodiment of a multilayer all organic device 200 in accordance with the present invention. The device 200 comprises a device component 202 sandwiched between two shielding and
20 packaging components 204. The device component 202 comprises a metalized organic dielectric layer 208 and two bond ply layers 210. The bond ply layers 210 (also referred to as prepreg) may comprise Speedboard from W.L. Gore & Associates, Inc. or Roger 4350 from Rogers Corporation. While the device component 202 only shows one metalized organic substrate layer, the device component may comprise multiple
25 metalized layers, which can be metalized on one or both sides, that are stacked with bonding material interposed between the metalized layers as needed for bonding the layers together. For example, thermoset materials, like bond ply or prepreg, can be utilized. Alternatively, one could alternate layers of high and low temperature thermoplastics, or utilize a combination of thermosets and thermoplastics. The device

200 is particularly well suited for mounting to a circuit board using surface mount device (SMD) techniques, as discussed in more detail below. The shielding and packaging components 204 comprise relatively thicker organic core layers 212, and as desired, shielding on one or more external surfaces of the device.

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[0042] The metalized organic dielectric layer 208 of the device component 202 preferably comprises a 25 μm thick layer of LCP or another suitable organic material, wherein the LCP layer comprises a patterned electroplated conductor layer 214 on both sides to form the conductor of the inductor. The conductor layers 214 may comprise
10 electroplated copper metal fabricated on the underlying substrate layer. While the conductor layers 214 in FIG. 2A are shown in a simple pattern in order to illustrate the invention, the present invention is not limited to any particular conductor design, though it is preferred that the conductor take one or a combination of the designs discussed in pending patent application, Application No. 09/995,161, filed on November 26, 2001, the
15 entire disclosure of which is incorporated by reference, or one of the designs illustrated in FIGS. 11A-D discussed below.

[0043] In an embodiment, conductor layers 214 comprise a layer of 25 μm electroplated copper metal. One of ordinary skill in the art will appreciate that the
20 thickness of the conductor layers may vary depending on design constraints. Furthermore, conductor layers 214 may comprise other types of metals and/or other types of conducting materials and may be fabricated on the substrate layers in various alternative ways. The conductor layers 214 on the opposing sides of the organic dielectric layer 208 may be interconnected by one or more vias 216, which can be formed
25 by a drill, laser or etch solution. Plated through holes 218 can be placed along the outer edge of the stand-alone device so that the singulation of the device dissects the through holes to form input/output ports for the device.

[0044] The bond ply layers 210 sandwich the metalized dielectric layer 208 and facilitate a bond between the dielectric layer 208 and the core layer 212. The core layers 212 preferably comprise a 36 mils thick layer of a hydrocarbon composite. Suitable materials for the bond ply layers 210 include any uncured organics such as epoxy/glass composites, PPE, hydrocarbon composites, and prepreg, and other suitable materials for the core layers 212 include cured organics such as epoxy/glass composites, PPE, hydrocarbon composites and prepreg. It should be noted that the organic materials comprising the various layers of the multilayer device 200 may all be a thermostat or thermoplastic, or they may be a combination of the two as described above. The organic materials selected may be chosen advantageously to thermally match or closely match adjacent material layer and/or the outer layer of the device 200 to the substrate on which it is mounted.

[0045] With reference to FIG. 2B, an alternative configuration of a multilayer all-organic device 250 is illustrated in a cross-sectional view. In this embodiment, the device component comprises two device components 252 that are sandwiching a relatively thick core layer 262, which provides the structural rigidity for the device 250. Additional structural rigidity and packaging is provided by shielding and packaging components 254. The device components 252 may comprise one or more metalized organic dielectric 258 sandwiched between two bond ply layers 260. This embodiment is particularly well-suited for a stand-alone device mounted using SMD techniques, as discussed in more detail below.

[0046] With reference to FIG. 2C, yet another alternative configuration of a multilayer all-organic device 280 is illustrated in a cross-sectional view. In this embodiment, a device component 282 is sandwiched between two core layers 284 that comprise the shielding and packaging. In this embodiment, the device component layer comprises bond ply and the component layer inductor comprises a patterned metallized layer 288 formed in a single plane (as opposed to having conductor elements on multiple

planes) on one of the core layers comprising the packaging component. The two core layers are bonded together by the bond ply layer, which is generally noted as the device component 282. Through holes 286 provide for connectivity to other layers or to the external bump pads on which solder bumps can be formed. This embodiment is particularly well-suited for a stand-alone device mounted using BGA/CSP techniques, as discussed in more detail below.

[0047] It should be noted that the embodiments of FIGS. 2A-2C are merely illustrative, and should not be viewed as limiting the present invention. The particular configuration of the device component 102 as a one or multiple layers, sandwiching or being sandwiched by core layers, should not be limited by the examples of FIGS. 2A-2C.

[0048] In accordance with an aspect of the present invention, the low cost organic materials (such as PPE and LCP) utilized to fabricate the inductors include thick copper metallization (e.g., greater than 10 μm) to sustain high current flow. Utilizing photolithography techniques, tolerances within 2% for inductances upwards of 0.1 nH can be achieved with unloaded Qs ranging from as low as 30 to as high as 700 at frequencies from hundreds of megahertz to multiple gigahertz. Additionally, the inductor devices are configured in novel topologies such as hybrid coplanar waveguide (CPW)/stripline and CPW/microstrip, which provides in-built shielding, as illustrated in FIGS. 3A-3D and discussed in greater detail below. In general, the hybrid topologies define the configuration of the inductors which leverages the organic process using the lower cost organic materials that can be processed using fewer steps, and can be automated for at least an 18"x24" wafer to leverage the economies of scale.

25

[0049] The quality determining component of an inductor is the characteristic impedance, Z_0 , of the lines used to comprise the inductor. The conductor loss in an inductor is inversely proportional to Z_0 of the line, and represents the dominant loss in the device provided the loss in the dielectric used in the construction is below a certain

threshold value of about 0.02. The characteristic impedance of these lines can be determined based on the inductance and capacitance per unit length, which can be computed based on the distance from the reference plane. Since voltage is not an absolute term like charge or current, it has to be referenced to a standard which is commonly called the ground plane. For the prior art ceramic inductors described in Table 1, the performance is determined by assuming the ground to be infinitely far away, which being impractical in most applications, has to be re-determined for realistic situations where the ground/reference is a finite distance away. This results in additional design time and interference due to the presence of other components which might be present in the electrical vicinity of the device.

[0050] The present invention avoids the problems associated with modeling ground for a discrete stand-alone inductor mounted to a circuit board of tens to hundreds of other passive and active electrical components by providing internal or external shielding, thereby defining ground independent of the inductor's surroundings. An inductor in accordance with the present invention includes a ground reference by having a multi (>2) terminal device, wherein two terminals can be the ground layer and the other two terminals can be the input and output terminals. This helps alleviate the concerns when using a standard two terminal device, such as those described in Table 1. The hybrid topologies of FIGS. 3A-3D also allow for additional shielding on the sides of the device to help restrict the energy within the device.

[0051] With reference to FIGS. 3A-3D, various hybrid topologies in accordance with aspects of the present invention are illustrated. FIGS. 3A and 3B illustrate CPW/stripline configurations, wherein FIG. 3A includes in-built side shielding and FIG. 3B includes external side shielding. The CPW/stripline topologies are particularly well-suited for mounting to a substrate or circuit board by SMD techniques. In each, the conductor 300 is substantially surrounded by shielding, such as by in-built side shielding 302 or external side shielding 304 and ground layers 306, 308. For illustrative purposes,

the conductor 300 is formed on an organic core 310. The organic core 310 and a core layer 312 sandwich a bond ply layer 314. FIGS. 3C and 3D illustrate CPW/microstrip configurations, wherein FIG. 3C includes in-built side shielding and FIG. 3D includes external side shielding. The CPW/microstrip topologies are particularly well-suited for mounting to a substrate or circuit board by BGA or CSP techniques. In each, the conductor 350 is surrounded on five sides by a reference ground, and the sixth side is shielded by the substrate to which it is mounted. As with the CPW/stripline topologies, side shielding is provided by in-built side shielding 352 in FIG. 3C and external side shielding 354 in FIG. 3D. The side shields are electrically connected with a ground layer 356. An organic core 360, on which the conductor is formed, and a core layer 358 sandwich a bond ply layer 362.

[0052] For an inductor, performance is often measured by the Q factor. The further apart the signal from the ground, the higher the impedance, which lends itself to a higher current carrying capability and a higher Q. In the hybrid topologies of the present invention, the separation between the coplanar ground and signal line (Hg) is arbitrary and can be chosen to be as large as required. However, Hs and Hm are not arbitrary and both need to be greater than or equal to Hg. To achieve Q's > 500, Hg is required to be approximately 30 mils with conductor widths greater than 10 mils, which implies Hs or Hm is to be greater than or equal to 30 mils. In a multilayer ceramic process, this thickness is can be achieved by stacking up several layers which are typically less than 8 mils. In an organic process, such thick cores are available with typical cores being 20 mils, 28 mils, 40 mils, etc. Moreover, organics have an intrinsically lower permittivity that helps reduce the capacitance and increase impedance of the lines. Lastly, conductor thicknesses of 35 μm are easily achievable in organic processes, as compared to 5 μm in ceramic processing. The relative thick conductor of the inductors of the present invention contributes to an increased quality factor by lowering resistive losses and advantageously allows the device to carry currents as high as the winding internal construction inductors in Table 1.

[0053] FIG. 4 is a cross-sectional view of an inductor 400 taken along lines 4'-4' of FIG. 5 in accordance with an embodiment of the present invention. The cross-sectional view shows the construction of an inductor formed on a wafer for singulation into discrete stand-alone inductor device. The inductor 400 comprises a ground plane conductive layer 408 on which an organic substrate layer 410 is disposed. A diclad organic layer 412 comprising conductive layers 414 and 416 is disposed on the upper surface of the organic substrate layer 410. The conductive layers 414, 416 are patterned to form conductive elements of a meandering coil conductor 418. In alternative embodiments, the diclad organic layer 412 may comprise a single clad layer, multiple single clad layers or multiple diclad layers, so as to form a single inductor or multiple inductors and other passive devices. A third organic substrate layer 420 is disposed on the diclad organic 412. While not illustrated in FIG. 4, each of organic substrate layers 410 and 420 includes a prepreg layer to facilitate bonding between the organic substrate layers 410, 420 and the diclad organic layer 412. A conductive layer 422 is disposed on the third organic substrate, and may operate as a ground plane if desired.

[0054] The conductive elements formed in conductive layers 414, 416 are interconnected by one or more vias 424 in the second organic substrate. The vias 424 can be formed by etching or drilling a void and then plating or filling the void with a conductive material such as copper/nickel-gold. The via is preferably formed prior to lamination of the substrates, and during lamination the dielectric to metal and dielectric to dielectric fusion bonds are formed in a single step, and then the metal to metal melting bonds are formed in a subsequent heating.

[0055] The inductor and other passive devices formed by the conductive layers are connected to two or more terminals formed by plated through holes 426. The cut lines 430 for singulating the inductor 400 pass through the through holes, as illustrated. Such plated through holes may be fabricated with a laser or mechanical drill.

[0056] Although the dimensions of the conductive layers and substrate layers may vary depending on the performance desired, intended use, materials utilized, etc., a particular embodiment will be described with reference to FIG. 4. For example, in cross-section, the conductive layers 408, 414, 416 and 422 may each comprise a layer of electroplated copper metal having a thickness greater than or equal to 20 μm . The organic substrate layers 410, 412 and 420 may each comprise a layer of LCP or other organic material having a thickness of 1 mil, and the core layer that may comprise at least a layer of hydrocarbon composite, epoxy/glass composite or PPE having a thickness greater than or equal to 20 mil. The vias and through holes are preferably copper plated.

[0057] In production, inductors 400 can be fabricated by the lot on a single substrate and then singulated. For example, a wafer 452 comprising a plurality of inductors 400, as illustrated in FIG. 5, can be singulated into stand-alone inductor devices 400, as illustrated in FIG. 6. Initially, the wafer is fabricated by adhering, preferably by lamination, a plurality of metalized organic substrates with patterned metalized layers with x-axis interconnecting vias and through holes formed therein. Next, parallel trenches 454 are formed to define the opposing side walls of the inductors. The trenches can be routed using a drill bit or cut out using a laser or saw. In one embodiment, the trenches are plated to form a side shielding layer 456 on opposing sides of the inductors. The inductors can then be singulated by cutting (e.g., with a saw or router) the wafer along lines 430, thereby intersecting the trenches 454 and through holes 426, thereby individually releasing the inductors from the wafer. Advantageously, the plated side walls and top conductive layers 458 provide external shielding for the inductor 400. This not only confines the electrical energy of the inductor 400, thereby preventing interference with other circuit bound components, it shields the inductor from external electrical noise. As previously discussed, this drastically reduces the processing required to model the performance of the inductor when mounted to a circuit board. The stand-

alone inductor 400 released from wafer 452, as illustrated in FIG. 6, can be mounted to a circuit board, for example, utilizing SMD technology.

[0058] FIG. 7 is an exploded view of a stand-alone inductor device, such as the one of FIG. 6. While metallization is only viewable on the upper surface of the organic layer 462, it is noted that the organic substrate layer 462 may be metalized on one or both planar surfaces and/or comprise multiple stacked metalized organic substrate layers that form one or more inductors and other passive components, as desired. If desired, vias can be formed in the organic substrate layer 462 to selectively interconnect the conductive elements formed on opposite surfaces or between the layers, providing for the fabrication of multiple passive devices. The passive devices are connected to the portion of the metalized through hole 464 that remains after singulation, which forms the terminals of the stand-alone device. Shielding 466 provides a ground reference and electrically isolates the operation of the enclosed passive device(s). While not illustrated in FIG. 7, each of the organic substrate layers 470, 472 may include a prepreg layer to facilitate the bonding of the organic substrate layers 470, 471 to the organic substrate layer 462.

[0059] In an alternative embodiment, inductors can be fabricated into a stand-alone device particularly well suited for mounting to a circuit board using BGA/CSP technology. For example, a plurality of inductors 500 can be fabricated by the lot on a wafer 502, as illustrated in FIG. 8. The construction of the inductors 500 will be similar to that of inductor 400 of FIG. 4 with several exceptions including, for example, the relative location of the through holes to the cut line and the addition of a solder mask layer of the top conductive layer. Parallel trenches 506 are formed to define opposite side walls of the inductor. If desired, the side walls formed by the trenches can be plated to form a shielding layer 510. To facilitate BGA/CSP mounting, the top surface of the wafer includes solder balls 530, 532 (also known as solder bumps). In order to form the solder balls 530, 532, a desired underbump metallurgy (UBM) is formed on the top

surface of the wafer, and then contact pads and the solder bumps (which are in the form of solder pads prior to reflow) are formed on the underbump metallurgy. See, for example, U.S. Patent No. 5,162,257. On the top surface of the wafer, over a top shielding layer, is a non-wattable solder mask to electrically isolate the solder balls 530, 532 from one another and the underlying shielding layer. The inductors 500 can be singulated by cutting the wafer along lines 520, intersecting trenches 504 to individually release the inductors from the wafer. FIG. 9 shows a stand-alone inductor 500 released from wafer 502. The shielding layer 510, 522 provide shielding to the integrated passive device imbedded within the stand-alone device. The solder balls 530, 532 provide for mechanical and electrical connection to a circuit board using well known flip-chip techniques (e.g., BGA and CSP), and in addition, solder balls 532 provide interconnection to the integrated passive device(s) of the inductor 500.

[0060] FIG. 10A is an exploded view of the stand-alone inductor device, such as the one of FIG. 9. As with the previous embodiment of FIG. 7, the device component layer 540 may be metalized on one or both planar surfaces and/or comprise multiple stacked metalized layers to form one or more inductors and other passive components, as desired. In the illustrated embodiment, the inductor 542 is electrically connected to the circuit board to which the stand-alone device is mounted by vias 544 and solder bumps 532. The solder balls 530 are electrically connected to the side shielding 546 by pads 548. A top shielding layer 550 is partially covered by a solder mask 552. While not illustrated in FIG. 10A, each of the organic substrate layers 570, 572 includes a prepreg layer to facilitate the bonding of the organic substrate layers 570, 572 to the device component layer 540.

[0061] FIG. 10B is an exploded view of an alternative embodiment to that of FIG. 10A, wherein the side shielding is in-built rather external. In particular, the external side shielding is not needed because of the patterned in-built ground ring 556 that is coplanar with the inductor. Additional vias 560 are formed in the core layer 574 to

facilitate connectivity between the solder balls 530 and the ground ring 556. Thus, for each plane on which passive devices or portions thereof are formed, a ground is fabricated about the periphery of the substrate. While not illustrated in FIG. 10B, each of the organic substrate layers 574, 576 may include a prepreg layer to facilitate the bonding
5 of the organic substrate layers 574, 576 to the device component layer 576.

[0062] The inductor configurations illustrated thus far have merely been illustrative of the numerous configurations available. Because of the ability to interconnect multiple conductive layers to form spiral and loop inductors in both the x-y
10 plane and z plane, as desired. For example, FIGS. 11A-11D provide illustrative alternative embodiments for the conductor configuration of an inductor in accordance with the present invention. For purposes of clarification, the inductors shown in FIGS. 11A-11D are represented in different widths to denote a different plane on which the inductors resided. That is, the inductors can be fabricated in either a single substrate
15 configuration (i.e., metallization on both sides of the organic substrate) or a multi-substrate configuration (i.e., metallization on one side of each adjacent substrate). With reference to the figures, FIG. 11A shows a three conductor residing on three discrete planes, thereby forming a vertically spiral or loop inductor in the z plane. FIG. 11B shows two spiraling conductors and two discrete planes, FIG. 11C shows a spiral or loop
20 in the x-y plane, and FIG. 11D shows a meandering spiral on a single plane.

II. Illustrative Methods for Fabricating Stand-Alone Inductors

[0063] An illustrative process for fabricating an LCP based integrated passive device (IPD), such as the inductor illustrated in FIG. 6, configured as a surface mount
25 device (SMD) in accordance with an embodiment of the present invention is now described with reference generally to FIG. 12A. Initially, a starting material is selected, which is preferably a reinforced or non-reinforced LCP laminate that can be unclad, or clad with copper on one or both sides of the LCP, as illustrated in Step 1. Alternate materials include other low loss organic laminates like PPE, PTFE composites,

hydrocarbon ceramic composites, BT resin composites (e.g., Speedboard C), and thermosets (e.g., Hitachi MCL-LX-67F). Next, vias are drilled through the LCP or other laminate and the layers of copper, as illustrated in Step 2. These microvias can be drilled with mechanical drilling, laser drilling or other suitable methods known to those skilled in the art.

[0064] Steps 3 and 4, involve the metallization of the vias and laminate. In additive, semi-additive, or subtractive processes starting with unclad or copper clad LCP or other laminates, both sides of the LCP or other laminate and the vias are seeded using electroless plated, vacuum deposited copper or another deposition method for forming a continuous copper film. To achieve the target metal thickness for the device, electrolytic plating is done to build the copper on both sides of the laminate and in the vias in a single step. The circuit definition for the inductor component can be done using subtractive, semi-additive or fully additive processes with panel or pattern electroplating of copper followed by print and etch steps to define the inductor component of the device layer, as illustrated in Step 5.

[0065] The fabricated device circuits are then packaged using vacuum or non-vacuum lamination of LCP or alternate dielectric laminate materials, such as those detailed above in connection with Step 1, and/or Al, Cu, Mo metal (for high power applications) on both sides of the inductor component to a given thickness to encapsulate components, as illustrated in Step 6. The added layers on either side of the inductor component are often referred to as core layers. The internal and external metal layers are connected, as needed, using plated through holes that can be drilled mechanically or with laser, photo, or plasma processes to provide signal and ground connections and SMD terminals, as illustrated in Step 7. The two edges of the device without the through hole are also slotted using mechanical drill/rout/mill, laser cutting, or sawing processes to provide for additional shielding of the device during subsequent metallization. The drilled through holes and shielding slots are seeded with electroless plated or

sputter/vacuum deposited copper to provide a bus layer in substantially the same manner as described above in connection with Step 3, as illustrated in Step 8.

[0066] With reference to Steps 9, 10, and 11, the final metal thickness for the outer layers is built up by electroplated copper in the through holes, shielding slots, and on the top and bottom surfaces. Subtractive, semi-additive, or additive processes may be used to define the outerlayer ground circuits and SMD terminals for connection with print and etch processing of the copper, as described above in connection with Steps 4 and 5. The device is then finished with terminal metals appropriate for SMD assembly and soldering processes. The finishing metals on the device terminals are common plated metals or alloys like electroless Ni-Au, immersion tin, immersion silver, electroplated Ni-Au, solder (HASL), or organic finishes (OSPs), wherein the choice depends on the intended application.

[0067] The fully fabricated wafer (also referred to as panel) is then singulated into individual inductor devices. The singulation can be done using high speed dicing saws or alternate methods such as punching or routing/milling. An advantage of this fabrication process is the ability to fully electrical test the components either before or after singulation.

[0068] Another illustrative process for fabricating an LCP based IPD, such as the inductor illustrated in FIG. 9, configured as a ball grid array (BGA) or chip scale package (CSP) in accordance with an embodiment of the present invention is now described with reference generally to FIG. 12B. Initially, a starting material is selected, preferably a reinforced or non-reinforced LCP laminate that can be unclad, or clad with copper foil on one or both sides of the LCP, as illustrated in Step 1. Alternate materials include other low loss organic laminates like PPE, PTFE composites, hydrocarbon ceramic composites, BT resin composites (e.g., Speedboard C), and thermosets (e.g., Hitachi MCL-LX-67F). Next, through vias are drilled through the LCP or other laminate and the layers of copper,

as illustrated in Step 2. These microvias can be drilled with mechanical drilling, laser drilling or other suitable methods known to those skilled in the art.

[0069] Steps 3 and 4 involve the metallization of the vias and laminate. In
5 additive, semi-additive, or subtractive processes starting with unclad or copper clad LCP or other laminates, both sides of the LCP or other laminate and the vias are seeded using electroless plated, vacuum deposited copper or another deposition method to form a continuous copper film. To achieve the target metal thickness for the device, electrolytic plating is done to build the copper on both sides of the laminate and in the vias in a single
10 step. The circuit definition for the inductor component can be done using subtractive, semi-additive or fully additive processes with panel or pattern electroplating of copper followed by print and etch steps to define the filter circuitry, as illustrated in Step 5.

[0070] The fabricated device circuits are then packaged using vacuum or non-
15 vacuum lamination of LCP or alternate dielectric laminate materials, such as those detailed above in connection with Step 1, and/or Al, Cu, Mo metal (for high power applications) on both sides of the inductor component to a given thickness to encapsulate components, as illustrated in Step 6.

[0071] On the other side of the inductor component, a cover coat material, liquid
20 photo imagable (LPI) or dry film solder mask is deposited using standard processes such as spin coating, curtain or roller coating, dry film lamination, spray coating and others, as illustrated in Steps 7, 8 and 9. This layer acts as a barrier to solder flow between terminals during subsequent reflow and component assembly. The component terminals
25 are defined by opening windows in the cover coat / solder mask material to open the BGA pads for board level interconnection. This is done with processes such as photolithography or laser ablation. The device is then finished with the deposition of terminal metals appropriate for BGA assembly and soldering processes. The finishing metals on the device terminals are common plated metals or alloys like electroless Ni-Au,

immersion tin, immersion silver, electroplated Ni-Au, solder (HASL), or organic finishes (OSPs) and the choice depends on the intended application and compatibility with the solder or other alloy used for device-to-module/ PWB interconnection.

5 [0072] With general reference to Steps 10, 11, 12, the interconnects are then formed in the windows defined in Step 8 using Pb/Sn solder, or other lead free solders and metal alloys. Processes such as screen or stencil printing of solder paste and reflow, or plating processes can be used to form the bumps for interconnection. The BGA/CSP format of the filter components enables the testing of the components on the large area
10 board prior to singulation. The testing can be done, for example, with probing techniques or using test sockets or fixtures.

[0073] The fabricated wafer is then singulated into individual inductor devices. The singulation can be done using high speed dicing saws or alternate methods such as
15 punching or routing/milling. An advantage of this fabrication process is the ability to fully electrical test the components either before or after singulation.

III. Integrated Passive Component Design/Optimization System

[0074] As stated above, the present invention enables the design of very low-cost,
20 integrated substrates with integrated inductors having a high Q factor. FIG. 13 illustrates a representative computing system 600 in which an embodiment of an inductor device design/optimization system 610 according to the present invention may be implemented. As described in more detail below, in general, inductor device design/optimization system 610 enables a user to design, model, and/or optimize inductors for mounting to
25 circuit boards using SMD or BGA/CSP techniques.

[0075] In general, inductor device design/optimization system 610 employs a coupled-line model to model integrated inductors, a segmentation approach to segment the integrated inductor into coupled-line segments and discontinuities, and a simulation

tool to compute the impedance matrix of the individual segments and reconstruction of the entire circuit response. Significantly, inductor device design/optimization system 610 enables a designer of integrated components to incorporate imperfections, such as non-uniform signal line profiles, varying dielectric constant, surface roughness in different topologies (i.e., CPW, microstrips, and striplines, etc.), and also maintain the frequency dependence of the models. Furthermore, inductor component design/optimization system also provides designers of inductor devices with layouts for specific passive components on a particular substrate, given certain process parameters and specifications.

10 [0076] Inductor component design/optimization system 610 may be implemented in software, firmware, hardware, or a combination thereof. In the embodiment illustrated in FIG. 13, inductor device design/optimization system 610 is implemented in software, as an executable program, which is executed by a processing device 602. Generally, in terms of hardware architecture, as shown in FIG. 13, computing system 600 comprises a
15 processing device 602, memory 604, one or more network interface devices 612, and one or more input and/or output (I/O) devices 614 interconnected via a local interface 620. System 600 may further comprise additional components not illustrated in FIG. 13.

[0077] Referring again to FIG. 13, the various components of system 600 will be
20 described. Local interface 620 may be, for example but not limited to, one or more buses or other wired or wireless connections. The local interface 620 may have additional elements, which are omitted for simplicity, such as controllers, buffers (caches), drivers, repeaters, and receivers, to enable communications. Furthermore, the local interface 420 may include address, control, and/or data connections to enable appropriate
25 communications among the aforementioned components.

[0078] Processing device 602 is a hardware device for executing software, particularly that stored in memory 604. Processing device 602 may be any custom-made or commercially-available processor, a central processing unit (CPU), an auxiliary

processor among several processors associated with system 600, a semiconductor based microprocessor (in the form of a microchip or chip set), a macroprocessor, or generally any device for executing software instructions.

5 [0079] As illustrated in FIG. 13, memory 604 may comprise an operating system 606, one or more applications 608, and inductor device design/optimization system 610. The architecture, operation, and/or functionality of inductor device design/optimization system 610 will be described in detail below. Memory 604 may include any one or combination of volatile memory elements (e.g., random access memory (RAM, such as
10 DRAM, SRAM, SDRAM, etc.)) and nonvolatile memory elements (e.g., ROM, hard drive, tape, CDROM, etc.). Memory 604 may incorporate electronic, magnetic, optical, and/or other types of storage media. Furthermore, memory 604 may have a distributed architecture, in which various components are situated remote from one another, but can be accessed by processing device 602.

15

[0080] The software in memory 604 may include one or more separate programs, each of which comprises executable instructions for implementing logical functions. In the example of FIG. 13, the software in memory 604 includes inductor device design/optimization system 610 according to the present invention. Memory 604 may
20 further comprise a suitable operating system 606 that controls the execution of other computer programs, such as one or more applications 608 and inductor device design/optimization system 610, and provides scheduling, input-output control, file and data management, memory management, and communication control and related services.

25

[0081] Inductor device design/optimization system 610 may be a source program, executable program (object code), script, or any other entity comprising a set of instructions to be performed. When implemented as a source program, then the program needs to be translated via a compiler, assembler, interpreter, or the like, which may or

may not be included within the memory 604, so as to operate properly in connection with operating system 606. Furthermore, inductor device design/optimization system 610 may be written as (a) an object oriented programming language, which has classes of data and methods, or (b) a procedure programming language, which has routines, subroutines,
5 and/or functions, for example but not limited to, C, C++, Pascal, Basic, Fortran, Cobol, Perl, Java, and Ada. In one embodiment, inductor device design/optimization system 610 is written as C code and implements commercial mathematical software, such as Matlab®

10 [0082] Network interface device(s) 612 may be any device configured to facilitate communication between system 600 and a communication network, such as a public or private packet-switched or other data network including the Internet, a circuit switched network, such as the public switched telephone network, a wireless network, an optical network, or any other desired communications infrastructure.

15 [0083] Input/output devices 614 may comprise any device configured to communicate with local interface 620. One of ordinary skill in the art will appreciate that, depending on the configuration of system 600, input/output devices 614 may include any of the following, or other, devices: a user interface device 616 (i.e., a keyboard, a
20 mouse, etc.), a display device 618, such a computer monitor, etc., a serial port, a parallel port, a printer, speakers, a microphone, etc. During operation of system 600, a user may interact with inductor device design/optimization system 610 via display device 618 and user interface devices 616.

25 [0084] During operation of system 600, the processing device 602 is configured to execute logic stored within the memory 604, to communicate data to and from the memory 604, and to generally control operations of the system 600 pursuant to the software. Inductor device design/optimization system 610 and operating system 606, in whole or in part, but typically the latter, are read by the processing device 602, perhaps

buffered within the processing device 602, and then executed.

[0085] In embodiments where inductor device design/optimization system 610 is implemented in software, as is shown in FIG. 13, inductor device design/optimization

5 system 610 may be stored on any computer-readable medium for use by or in connection with any computer related system or method. In the context of this document, a computer-readable medium may be an electronic, magnetic, optical, or other physical device or means that may contain or store a computer program for use by or in connection with a computer-related system or method. Inductor device

10 design/optimization system 610 may be embodied in any computer-readable medium for use by or in connection with an instruction execution system, apparatus, or device, such as a computer-based system, processor-containing system, or other system that can fetch the instructions from the instruction execution system, apparatus, or device and execute the instructions. In the context of this document, a "computer-readable medium" can be
15 any means that can store, communicate, propagate, or transport the program for use by or in connection with the instruction execution system, apparatus, or device. The computer-readable medium can be, for example but not limited to, an electronic, magnetic, optical, electromagnetic, infrared, or semiconductor system, apparatus, device, or propagation medium. More specific examples (a nonexhaustive list) of the computer-readable
20 medium would include the following: an electrical connection (electronic) having one or more wires, a portable computer diskette (magnetic), a random access memory (RAM) (electronic), a read-only memory (ROM) (electronic), an erasable programmable read-only memory (EPROM, EEPROM, or Flash memory) (electronic), an optical fiber (optical), and a portable compact disc read-only memory (CDROM) (optical). Note that
25 the computer-readable medium could even be paper or another suitable medium upon which the program is printed, as the program can be electronically captured, via for instance optical scanning of the paper or other medium, then compiled, interpreted or otherwise processed in a suitable manner if necessary, and then stored in a computer memory.

[0086] In alternative embodiments where inductor device design/optimization system 610 is implemented in hardware, inductor device design/optimization system 610 may be implemented with any or a combination of the following, or other, technologies: a
5 discrete logic circuit(s) having logic gates for implementing logic functions upon data signals, an application specific integrated circuit (ASIC) having appropriate combinational logic gates, a programmable gate array(s) (PGA), a field programmable gate array (FPGA), etc.

10 [0087] FIG. 14 is a flow chart illustrating the architecture, functionality, and/or operation of an embodiment of inductor device design/optimization system 610. Inductor device design/optimization system 610 begins at block 700. Inductor device design/optimization system 610 may be initiated by a user via an I/O device 614. In
15 alternative embodiments, inductor device design/optimization system 610 may be implemented as a function that may be called by operating system 606 and/or an application 608. In alternative embodiments, the functionality of inductor device design/optimization system 610 may be seamlessly implemented within an application 608.

20 [0088] Regardless of the manner in which inductor device design/optimization system 610 is initiated, at block 702, inductor device design/optimization system 610 may receive one or more design parameters for a substrate structure in which a design component, such as an inductor, capacitor, etc., is to be fabricated. One of ordinary skill
25 in the art will appreciate that the design parameters may vary depending on various design constraints. For example, the design parameters may specify various characteristics of the substrate structure, such as material characteristics, physical characteristics, (i.e., conductor thickness, etc.) and electrical characteristics of the substrate layers and the conductor layers. At block 704, inductor device design/optimization system 610 may receive one or more process parameters (i.e., surface

roughness, signal line profile, etc.) associated with a predetermined type of integrated circuit package in which the substrate structure is to be implemented.

[0089] Inductor device design/optimization system 610 may be configured to
5 receive the information represented at blocks 702 and 704 in a number of ways. In one embodiment, the information is received via an input/output device 614, for example, by a user via a user interface device 616. The information may also be received via a network interface, device 612 or may be accessed directly from memory 604.

10 [0090] At block 706, inductor device design/optimization system 610 generates a coupled-line model for a plurality of configurations for an inductor. The coupled-line model of the inductor may comprise one or more coupled lines and one or more discontinuities, such as bends, vias, and steps in width of the trace line. In general, inductor device design/optimization system 610 estimates the amount of coupling
15 between integrated passives on the substrate. Inductor device design/optimization system 610 models passive structures with the aid of common multi-line parameters. Inductor device design/optimization system 610 uses a distributed model, which relates the voltages and currents at the start and end of a multiple coupled line section using impedance and admittance matrices.

20

[0091] Inductor device design/optimization system 610 may be used to model symmetric lines, as well as asymmetric lines. For example, the discontinuities in the integrated inductor, such as bends, vias, cross-overs, and steps in width may be modeled using scalable models or analytical equations. Various scalable models are described in
25 S. H. Min, et al., "Design, Fabrication, Measurement and Modeling of Embedded Inductors in Laminate Technology," Proc. Of IPACK, July 2001, which is hereby incorporated by reference in its entirety. Scalable models may be used to provide a mapping between the physical and electrical parameters of the discontinuity, which may be represented using rational functions. In general, the mapping may employ

interpolation functions. The use of interpolation functions may minimize the number of sampled data points that are required.

[0092] One of ordinary skill in the art will appreciate that the response of integrated passives is dictated by unwanted parasitic effects, which need to be modeled accurately. Coupled lines represent an integral part of integrated passives such as filters, couplers, baluns, etc. However, they also represent an integral part of other passives such as spiral and loop inductors and inter-digital capacitors. For purposes of demonstrating the coupled-line model, FIG. 15 illustrates a 1-3/4 turn spiral inductor. As shown in FIG. 15, the spiral inductor comprises several coupled line sections cascaded with each other through vias, bends, and cross-overs.

[0093] FIG. 16 illustrates a cascaded structure representation of the inductor of FIG. 15, which may be derived using a segmentation approach. The segmentation approach is described in S. Dalmia, et al., "Modeling of Embedded RF Passives Using Coupled Lines and Scalable Modes," IEEE Electronics, Components and Technology Conference (ECTC), May 2001.

[0094] The cascaded structure representation comprises a series of coupled lines and discontinuities. The blocks in FIG. 16 represent the discontinuities between the coupled line sections of the inductor. For example, the block between ports 3, 4 and 5, 6 is a crossover and that between 7, 8 and 9, 10 are coupled bends. These discontinuities in the circuit, which may be modeled as electrically short structures at high frequencies, can be modeled using the scalable models described above. The line segments in FIG. 16 represent the multiple coupled line or single uncoupled line sections, which are modeled using the multi-line parameters. One of ordinary skill in the art will appreciate that a multi-mode structure, such as spiral inductors, microstrip loop inductors, and CPW loop inductors, may be segmented as shown in FIG. 16, which enables scalability in the design process. It is worth mentioning that the segmentation approach may be extended to other

devices, such as inter-digital capacitors, helical inductors, etc.

[0095] Referring again to FIG. 14, at block 708, inductor device design/optimization system 610 simulates the frequency response of the coupled-line models based on the design parameters and process parameters. For instance, a set of `n` coupled lines may support `n` independent modes of propagation (called normal modes). Inductor device design/optimization system 610 may be configured to simulate the responses of the coupled lines using quasi-transverse electromagnetic (TEM) lines modes of propagation. The accuracy of this approach improves as the ratio of the wavelength to the thickness of the dielectric increases. For example, a two-dimensional electromagnetic solver, such as ANSOFT 2D.RTM. provides characteristic mode impedances and propagation constants for lossy and lossless lines. The mode impedances and propagation constants may be used to create a distributed model for the multi-line coupled line sections. At least one advantage of using a distributed model is that it prevents artificial ringing induced by lumped circuit equivalents of the multi-coupled lines and may include frequency dependant parameters.

[0096] FIG. 17 illustrates a mathematical representation of two symmetric, lossless, coupled lines, which may be implemented by inductor device design/optimization system 610 to simulate the frequency response of the coupled-line models. One of ordinary skill in the art will appreciate that voltages and currents on a set of 2 symmetric lossless coupled lines of length, l , shown in FIG. 17 may be obtained from the even-mode impedance (Z_{0e}), odd-mode impedance (Z_{0o}), even-mode propagation constant (β_e) and odd-mode propagation constant (β_o) using Equation (1), which follows:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} \quad (1)$$

$$\begin{aligned} \text{where, } Z_{11} &= Z_{22} = Z_{33} = Z_{44} = -j(Z_{oe} \cot(\beta_e l) + Z_{oo} \cot(\beta_o l)) / 2 \\ Z_{12} &= Z_{21} = Z_{34} = Z_{43} = -j(Z_{oe} \cot(\beta_e l) - Z_{oo} \cot(\beta_o l)) / 2 \\ Z_{13} &= Z_{24} = Z_{31} = Z_{42} = -j(Z_{oe} \csc(\beta_e l) + Z_{oo} \csc(\beta_o l)) / 2 \\ Z_{14} &= Z_{23} = Z_{32} = Z_{41} = -j(Z_{oe} \cot(\beta_e l) - Z_{oo} \csc(\beta_o l)) / 2 \end{aligned}$$

5

[0097] One of ordinary skill in the art will appreciate that this approach may also be used to model more than a pair of coupled lines. Accordingly, inductor device design/optimization system 610 may incorporate the corresponding systems of alternative equations to model more than a pair of coupled lines. One of ordinary skill in the art will further appreciate that inductor device design/optimization system 610 may be used to model and simulate frequency responses for asymmetric multi-line lossy-coupled line sections, as described in S. Dalmia, et al., "Modeling of Embedded RF Passives Using Coupled Lines and Scalable Models," IEEE Electronics, Components and Technology Conference (ECTC), May 2001.

[0098] Furthermore, inductor device design/optimization system 610 is not limited to homogenous substrates and may be used for multi-layered dielectric substrates. Significantly, inductor device design/optimization system 610 enables a designer to optimize the performance of RF passives by varying parameters, such as line width and spacing, for different coupled line sections in the passive design. An example of such an optimization would be in the case of spiral inductors where wider outer turns and narrower inner turns helps reduce ohmic losses in the outer turns and eddy current losses

in the inner turns, respectively.

[0099] Moreover, inductor device design/optimization system 610 may be configured to include other variables, such as the surface roughness of the signal lines, the effect of varying dielectric constants, and non-uniform cross-section in the analysis of the coupled transmission lines. For instance, these variations are typical in laminate technology and/or organic technology, which use a sequential build up process. Tools such as ANSOFT HFSS®. may be used to model these non-uniformities, but such tools may be computationally expensive. Tools that utilize empirical equations, such as Agilent's ADS®, reduce computation time, but are limited in terms of bandwidth and need constant revision for new processes and new topologies. Tools such as SONNET, which is a method-of-moments tool, considered optimal for simulating planar components such as inductors, overestimate the loss in the device in components with thick conductors.

[0100] The voltage and current vectors, V and I , on a multi-conductor coupled line, which propagate energy in the $\pm z$ direction, can be written as

$$-\frac{\partial^2}{\partial z^2}V = ZYV \quad (2)$$

$$-\frac{\partial^2}{\partial z^2}I = YZI \quad (3)$$

where

$$Z = (R(f) + j\omega[L]) \quad (4)$$

$$Y = (G(f) + j\omega[C_e]) \quad (5)$$

[0101] In Equations (4) and (5), $R(f)$ and $G(f)$ represent the conductor loss and dielectric loss respectively. Both these parameters are frequency dependent. For RF and microwave applications, where the current penetration depth in the conductor is of the

order of micrometers, the frequency dependence of the resistance matrix, R, conductance matrix, G, and inductance matrix, L, can be written in the form Equation (6)-(8) below:

$$R(f) = R_{DC} + R_{AC} \sqrt{f}, L = L_e + L_i \frac{1}{\sqrt{f}} \text{ and } G(f) = G_1 \times f \quad f_1 \quad (6), (7), (8)$$

5 [0102] In the above equations, L_e and C_e represent the external inductance and capacitance matrices respectively; $\omega = 2\pi f$ is the angular frequency. Equations (6)-(8) can be used to capture the frequency effects in the inductor. R_{DC} and R_{AC} are computed by solving for the total resistance matrix, R, at two different frequencies using commercial tools such as ANSOFT2D. Similarly, L_i and L_e are computed by solving for
10 the inductance matrix, L, at two different frequencies. The conductance matrix, G_1 , is computed at a particular frequency (f_1) and then computed at other frequencies (f) using Equations (6)-(8). C_e is assumed to be constant with frequency. Equations (6)-(8) ignore the dependence of the dielectric constant on frequency, which is typical for dielectric substrates such as Vialux and PPE used in MCM-L processes.

15 [0103] The variations in dielectric constant can be introduced in the computation of the R, G and C matrices by observing the empirical equations for the lines under consideration. For example, in the quasi-TEM range, the effective dielectric constant, ϵ_{eff} of CPW lines is proportional to $\sqrt{(\epsilon_{ru1}(f_u) + \epsilon_{ru2}(f_u))/2}$ where ϵ_{ru1} and ϵ_{ru2} are the
20 dielectric constants for Dielectric A and Dielectric B at a particular frequency f_u . Assuming one of the dielectrics to be air or vacuum simplifies the Equation to:

$$C_u(f_u) \propto \epsilon_{eff}(f_u) \propto \sqrt{(\epsilon_{ru}(f_u) + 1)/2} \quad (9)$$

[0104] After computing the capacitance matrix C_u at a frequency f_u , with a dielectric constant of ϵ_{ru} , using ANSOFT2D, the C matrices at other frequencies can be obtained by using the quasi-TEM relationship described in Equation (9). The capacitance matrix C_l at frequency f_l , where the dielectric constant is ϵ_{rl} for CPW lines can be
 5 computed by using the following equation:

$$C_l(f_l) = C_u \times \sqrt{(\epsilon_{rl} + 1)/(\epsilon_{ru} + 1)} \quad (10)$$

[0105] The L matrix is independent of the dielectric constant. The G matrix at different frequencies can be computed using $G \propto C$.

10

[0106] For any transmission line, $R(f_u)$ is inversely proportional to $Z_o(f_u)$ where $Z_o(f_u)$ is the characteristic impedance of the line at frequency f_u . Since, $Z_o(f_u)$ is also inversely proportional to $\sqrt{C_u}$, the R matrix becomes directly proportional to $\sqrt{C_u}$ as shown in Equation (11), below:

15

$$R(f_u) \propto \frac{1}{Z_o} \propto \sqrt{C_u} \quad (11)$$

The relationship between R and C, shown in Equation (11), along with Equation (10) can be used to capture the effect of varying dielectric constant on the R matrix.

[0107] The R matrix not only depends on the dielectric constant but also depends
 20 on skin effect and current-crowding effects. Current crowding is when the current distribution in lines, under the influence of an external time varying magnetic field, begins to concentrate along the edges of the lines. However, as expected current crowding is prominent only in very closely spaced turns of an inductor or closely spaced fingers of a capacitor. A reduction in current crowding and therefore skin effect becomes the
 25 dominant effect. As mentioned earlier skin effect has been taken into account in the modeling using the $\sqrt{f}$ dependence as shown in Equations (6)-(8).

[0108] Once the frequency dependant Z and Y matrices are obtained over the desired frequency range, for a wave propagating in the 'z' direction, the coupled Equations (2) and (3) can be partially de-coupled by solving the eigenvalue equation
5 shown below:

(12)

$$(ZY - \lambda U).V = 0 \quad (13)$$

$$\text{and } (YZ - \lambda U).I = 0$$

where, $-\lambda = \gamma^2$, U is the Identity Matrix and $\gamma = \alpha + j\beta$ is the complex propagation
10 constant.

[0109] The n eigenvalues for n lines and n corresponding eigen modal voltage and current vectors can be obtained by solving Equations (5) and (6)-(8) respectively. These can be used to define the behavior of the n lines completely. Let M_V and M_I be the
15 complex eigenvector matrix associated with the matrices ZY and YZ respectively. All normal voltages and currents on the line can be written as a linear combination of vectors, $\hat{V}$ and $\hat{I}$ as follows:

$$V = M_V \hat{V} \quad \text{and} \quad I = M_I \hat{I} \quad (14)$$

20

Substitution of Equation (13) into (2) and (3) yields:

$$\begin{aligned} -\frac{\partial^2}{\partial z^2} \hat{V} &= (M_V^{-1} Z Y M_V) \hat{V} \\ -\frac{\partial^2}{\partial z^2} \hat{I} &= (M_I^{-1} Y Z M_I) \hat{I} \\ (M_V^{-1} Z Y M_V) &= (M_I^{-1} Y Z M_I) = \gamma^2 \end{aligned} \quad (15)$$

- 5 [0110] Since this is an eigenvalue problem a normalization procedure is required. In this paper the following normalization is used:

$$(M_V^{-1})^t = M_I \quad (16)$$

- 10 [0111] The computation of eigenvectors in Equation (13) requires care, because of the properties of the ZY product. This product results in a diagonal dominant matrix, which has very closely spaced eigenvalues, which may give rise to difficulties and inaccuracies in the numerical computation. To avoid this difficulty an eigenvalue-shifting technique has been used. The shift is done by subtracting from ZY a scalar diagonal matrix with elements equal to the trace of ZY divided by n :

15

$$(ZY)' = ZY - \gamma_{av}^2 E, \quad \gamma_{av}^2 = \frac{1}{n} \sum_{i=1}^n (ZY)_{ii} \quad (17)$$

- [0112] The resulting matrix $(ZY)'$ is then diagonalized, yielding a set of adequately spaced eigenvalues $\gamma'_1, \dots, \gamma'_k, \dots, \gamma'_n$ and a corresponding set of eigenvectors.
- 20 The eigenvectors of ZY are exactly equal to those of $(ZY)'$. The eigenvalues of the original product ZY can be obtained by shifting back the eigenvalues as follow:

$$\gamma_k'^2 = \gamma_{av}^2 + \lambda_k \quad (k = 1, \dots, n) \quad (18)$$

[0113] This analysis is based on the diagonalization of the matrix ZY, whose solution enables the computation of the propagation modes traveling along the structure.

5

[0114] By solving for the voltages, V(0) and V(l) and currents, I(0) and I(l) at the ends of the multiple coupled line section, the impedance matrix can be derived as:

$$\begin{bmatrix} V(0) \\ V(l) \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I(0) \\ I(l) \end{bmatrix}$$

$$Z_{11} = Z_{22} = \text{COTH}(\Gamma l) Z_w;$$

$$Z_{12} = Z_{21} = \text{CSCH}(\Gamma l) Z_w \quad (19)$$

where,

$$\begin{aligned} \text{COTH}(\Gamma l) &= M_V (\coth \gamma l) M_V^{-1} \\ \text{CSCH}(\Gamma l) &= M_V (\text{csch } \gamma l) M_V^{-1} \\ Z_w &= M_V \gamma M_V^{-1} Y^{-1} \end{aligned}$$

10

The above representation enables the designer to optimize the performance of RF passives by varying parameters such as line width, length and spacing for different coupled line sections using a 2D electromagnetic solver.

15 [0115] Accordingly, inductor device design/optimization system 610 may be configured to incorporate the variations mentioned above for different topologies, such as CPW, microstrip, etc. Once the matrices for the coupled lines and for the scalable functions are obtained they can be cascaded using the segmentation approach described above.

[0116] The underlying basis of the segmentation approach is the transformation of the field matching (electric and magnetic fields) along the interface between two regions with higher mode excitations into an equivalent network connection problem using S-, Z-, or Y-matrices. Because Z-matrix characterizations of multiple-coupled lines and planar discontinuities can be obtained as solutions of ordinary differential equations, it becomes computationally efficient to develop a segmentation procedure in terms of Z-parameters.

[0117] Referring again to FIG. 14, after simulating the frequency response of the coupled-line models, at block 710, inductor device design/optimization system 610 determines one or more optimal configurations for the inductor to be designed, which satisfies the design parameters and process parameters. Inductor device design/optimization system 610 may be further configured to provide the optimal configurations to the user via an input/output device 614 and a network interface device 612. Inductor device design/optimization system 610 terminates at block 712.

[0118] Another very important element that this optimization enables is the addition of the shield effect as well as the capability to model hybrid devices such as CPW/stripline. This attribute of the optimization is imperative to understand whether or not the shield, thought of as a short between, for example, upper and bottom ground planes of a stripline configuration degrades the performance of the device.

IV. Coupling between Inductors

[0119] The modeling technique discussed above for individual inductors is now applied to modeling the coupling between multiple inductors. FIG. 18 shows two 1-port inductors (with ports 1 and 2 as the input ports of the two inductors) modeled in SONNET on the same multi-layered lossy substrate. The structure was modeled using

the technique mentioned above; however, the result was obtained as a 2 port response instead of a 1-port inductor response. The 2 port response captured the coupling of two 1-port inductors. The comparison of the responses obtained from SONNET and the modeling technique is shown in FIG. 19.

5 [0120] The results show good correlation and capture the coupling effect (Z_{12}
= Z_{21}) between the two inductors. It is important to note that the coupling is a function of
the distance between the inductors and also the cross-sectional configuration of the two
inductors. Optimization of the coupling and isolation parameters based on a full-wave
tool such as SONNET can get very tedious. For example, SONNET took approximately
10 26 minutes to simulate the response for twenty four frequency points on an Ultra 30
Sparc Station, whereas the modeling technique of the present invention, including the
time to obtain the R, L, G, C parameters from ANSOFT 2D on a 600 MHz Celeron
Processor, took approximately 12 minutes. Tools such as the Advanced Design Suite
15 (ADS) by Agilent can model the coupling of ideal inductors or model lossy inductors as
a function of frequency with the aid of design equations but cannot model the coupling
of lossy inductors. The technique discussed herein is a hybrid technique, which is circuit
based and is more adaptable for the optimization of embedded RF circuits. This is
primarily due to the use of 2D analysis for electrically large structures, use of 3D
analysis for electrically short structures and the ability to combine these results through
20 the segmentation method.

[0121] The coupling of inductors becomes an important design parameter in the
design of devices with multiple inductors such as baluns, filters, etc. The coupling if not
modeled leads to parasitic behavior whereas if properly predicted can help achieve
additional functionality in the circuits.

25 [0122] Many modifications and other embodiments of the inventions set forth
herein will come to mind to one skilled in the art to which these inventions pertain
having the benefit of the teachings presented in the foregoing descriptions and the

associated drawings. Therefore, it is to be understood that the inventions are not to be limited to the specific embodiments disclosed and that modifications and other embodiments are intended to be included within the scope of the appended claims. Although specific terms are employed herein, they are used in a generic and descriptive
5 sense only and not for purposes of limitation.

THAT WHICH IS CLAIMED:

1. An organic stand-alone inductor device for mounting to a circuit board, comprising:
 - 5 a first conductive layer;
 - a first substrate layer comprising an organic material formed on a first surface of the first conductive layer;
 - a second conductive layer formed on a first surface of the first substrate layer and comprising an inductor, which exposes portions of the first substrate layer;
 - 10 a bond ply layer formed on the second conductive layer and exposed portions of the first substrate layer;
 - a second substrate layer comprising a second organic material formed on the bond ply layer opposite the second conductive layer and first substrate layer; and
 - a third conductive layer formed on a first surface of the second substrate layer
 - 15 opposite the second conductive layer.
2. The inductor device of Claim 1, wherein the inductor is configured in a hybrid coplanar waveguide/stripline topology.
- 20 3. The inductor device of Claim 2, further comprising shielding on at least two opposite sides of the inductor.
4. The inductor device of Claim 3, wherein the side shielding is in-built.
- 25 5. The inductor device of Claim 3, wherein the side shielding is external.
6. The inductor device of Claim 1, wherein the first conductive layer and third conductive layer operate as ground references for the transmission line.

7. The inductor device of Claim 1, wherein the first organic material comprises one of liquid crystalline polymers, polyphenyl ether-based materials and hydrocarbon composites, and epoxy/glass composites.

5 8. The inductor device of Claim 1, wherein the second organic material comprises one of liquid crystalline polymers, polyphenyl ether-based materials and hydrocarbon composites, and epoxy/glass composites.

9. The inductor device of Claim 1, wherein the second conductive layer
10 comprises a layer of conductive material having a substantially uniform thickness greater or equal to 5 microns.

10. The inductor device of Claim 1, wherein the total thicknesses of the first and second substrate layers is greater than approximately 5 mils.

15

11. The inductor device of Claim 1, wherein the inductor device includes at least two terminals, and further comprising a via connecting the inductor to at least one of the terminals.

20 12. An organic inductor device for mounting to a circuit board, comprising:
a first conductive layer;
a first substrate layer comprising an organic material formed on a first surface of the first conductive layer;
a second conductive layer formed on a first surface of the first substrate layer and
25 comprising an inductor, which exposes portions of the first substrate layer;
a bond ply layer formed on the second conductive layer and exposed portions of the first substrate layer;
a second substrate layer comprising a second organic material formed on the bond ply layer opposite the second conductive layer and first substrate layer;

shielding on at least two opposite sides of the inductor device; and
wherein the inductor is configured in a coplanar waveguide/microstrip topology.

13. The inductor device of Claim 12, wherein the side shielding is in-built.

5

14. The inductor device of Claim 12, wherein the side shielding is external.

15. The inductor device of Claim 12, wherein the first conductive layer and
third conductive layer operate as ground references for the transmission line.

10

16. The inductor device of Claim 12, wherein the first organic material
comprises one of liquid crystalline polymers, polyphenyl ether-based materials and
hydrocarbon composites, and epoxy/glass composites.

15

17. The inductor device of Claim 12, wherein the second organic material
comprises one of liquid crystalline polymers, polyphenyl ether-based materials and
hydrocarbon composites, and epoxy/glass composites.

20

18. The inductor device of Claim 12, wherein the second conductive layer
comprises a layer of conductive material having a substantially uniform thickness of
between 15 microns to 50 microns.

25

19. The inductor device of Claim 12, wherein the thicknesses of the first and
second substrate layers are greater than approximately 20 mils.

20. The inductor device of Claim 12, wherein the inductor device includes at
least two terminals, and further comprising a via connecting the inductor to at least one of
the terminals.

21. The inductor device of Claim 12, wherein the first conductive layer and shielding operate as ground references for the transmission line.

22. The inductor device of Claim 21, wherein the side shielding is electrically
5 connected to the first conductive layer.

23. The inductor device of Claim 22, wherein a through hole connects the side shielding and first conductive layer.

10 24. An organic stand-alone inductor device, comprising:
a device component comprising a first organic substrate on which at least one inductor is formed;
a first core layer of organic material adjacent the device component; and
side shielding on at least two sides of the inductor to provide a single
15 ground reference.

25. The stand-alone inductor of Claim 24, further comprising a second core layer disposed adjacent the device component, opposite the first core layer.

20 26. The stand-alone inductor of Claim 24, wherein the device component layer comprises a plurality of organic substrates bonded together, wherein each organic substrate includes at least one inductor.

27. The stand-alone inductor of Claim 26, wherein at least two of the plurality
25 of organic substrates are electrically interconnected by a via.

28. The stand-alone inductor of Claim 24, wherein the inductor device includes at least two terminal, and the inductor is electrically connected to one of the terminals.

29. The stand-alone inductor of Claim 24, further comprising a second device component comprising a second organic substrate on which at least a second inductor is formed, the second device component is disposed adjacent the core layer, opposite the device layer.

30. The stand-alone inductor of Claim 29, wherein the device component and second device component are electrically connected by a via in the core layer.

31. The stand-alone inductor of Claim 24, wherein the side shielding comprising external layers of conductive material.

32. The stand-alone inductor of Claim 24, wherein the side shielding comprising in-built layers of conductive material fabricated on the same plane as the inductor.

33. The stand-alone inductor of Claim 24, wherein the device component comprises two bond ply layers that sandwich the first organic substrate.

34. A method for fabricating a stand-alone inductor device, comprising:
fabricating a wafer comprising a plurality of all organic inductor devices,
at least one inductor device comprising:

a device component including a first organic substrate on which at least one inductor is formed, and

a first core layer of organic material adjacent the device component;

forming trenches along two opposing sides of at least one inductor device integrated in the wafer;

metalizing the trenches; and

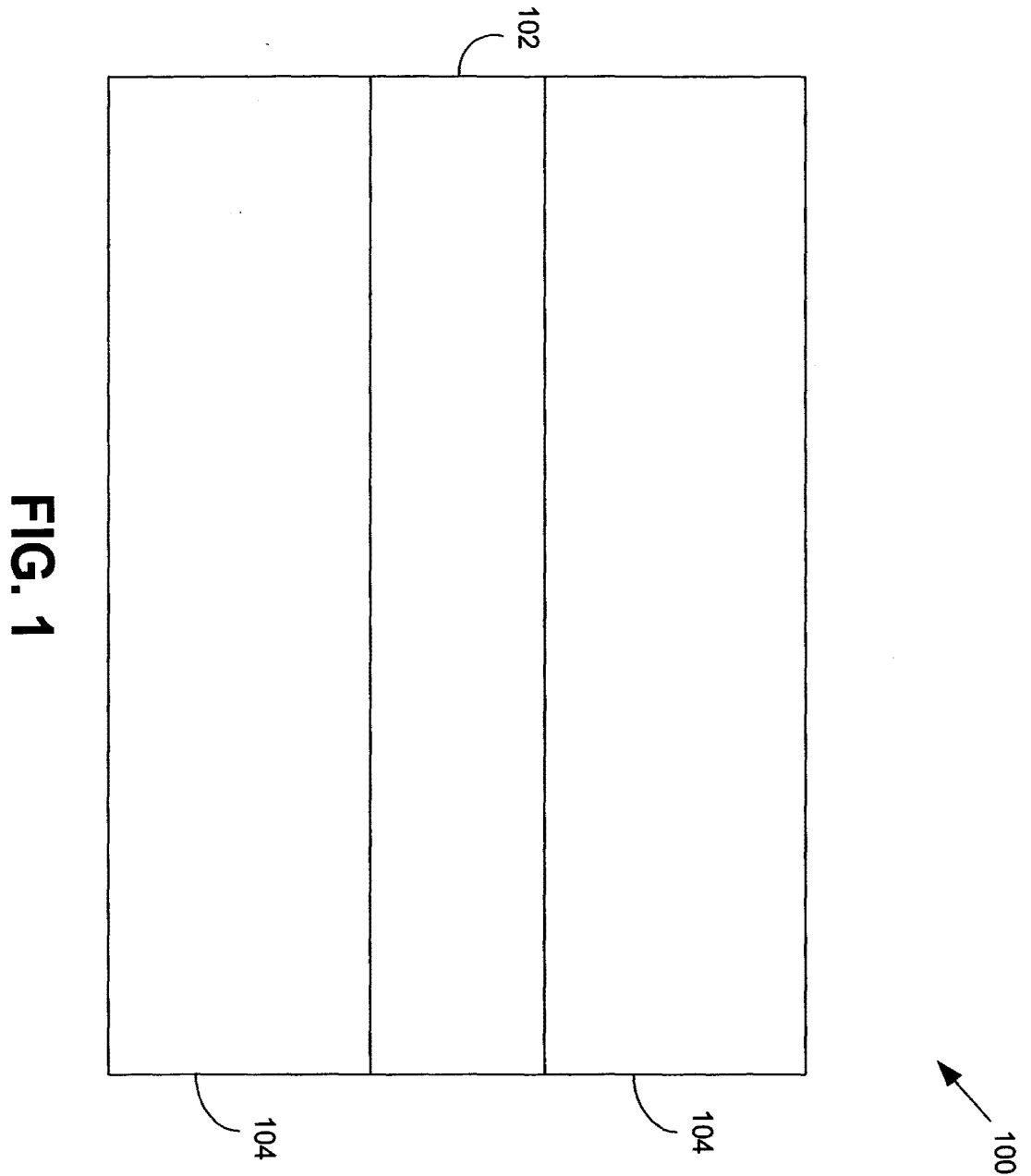
singulating the inductor devices so as to form stand-alone inductor devices with external side shielding formed from the metallization of the trenches.

35. A method for fabricating a stand-alone inductor device, comprising:
 fabricating a wafer comprising a plurality of all organic inductor devices,
 at least one inductor device comprising:
 a device component including a first organic substrate on which at
 least one inductor is formed,
 in-built side shielding on at least two sides of an inductor integral
 the inductor device; and
 a first core layer of organic material adjacent the device
 component;
 forming trenches along two opposing sides of at least one inductor device
 integrated in the wafer; and
 singulating the inductor devices so as to form stand-alone inductor
 devices.

STAND-ALONE ORGANIC-BASED PASSIVE DEVICES

ABSTRACT

5 The present invention provides for low cost discrete inductor devices in an all
organic platform. The inductor devices can utilize virtually any organic material that
provides the desired properties, such as liquid crystalline polymer (LCP) or polyphenyl
ether (PPE), in a multilayer structure, wherein the organic materials have low moisture
uptake and good temperature stability. Each layer may be metalized and selectively
10 interconnected by vias formed in respective layers so as to form winding or coiled
inductors. The inductor devices may advantageously include external shielding formed
by metalizing the side walls and top surface of the inductor devices on in-built shielding
achieved by the utilization of the hybrid co-planar waveguide topologies. The inductor
devices can be configured for either ball grid array (BGA)/chip scale package (CSP) or
15 surface mount device (SMD) mounting to circuit boards.



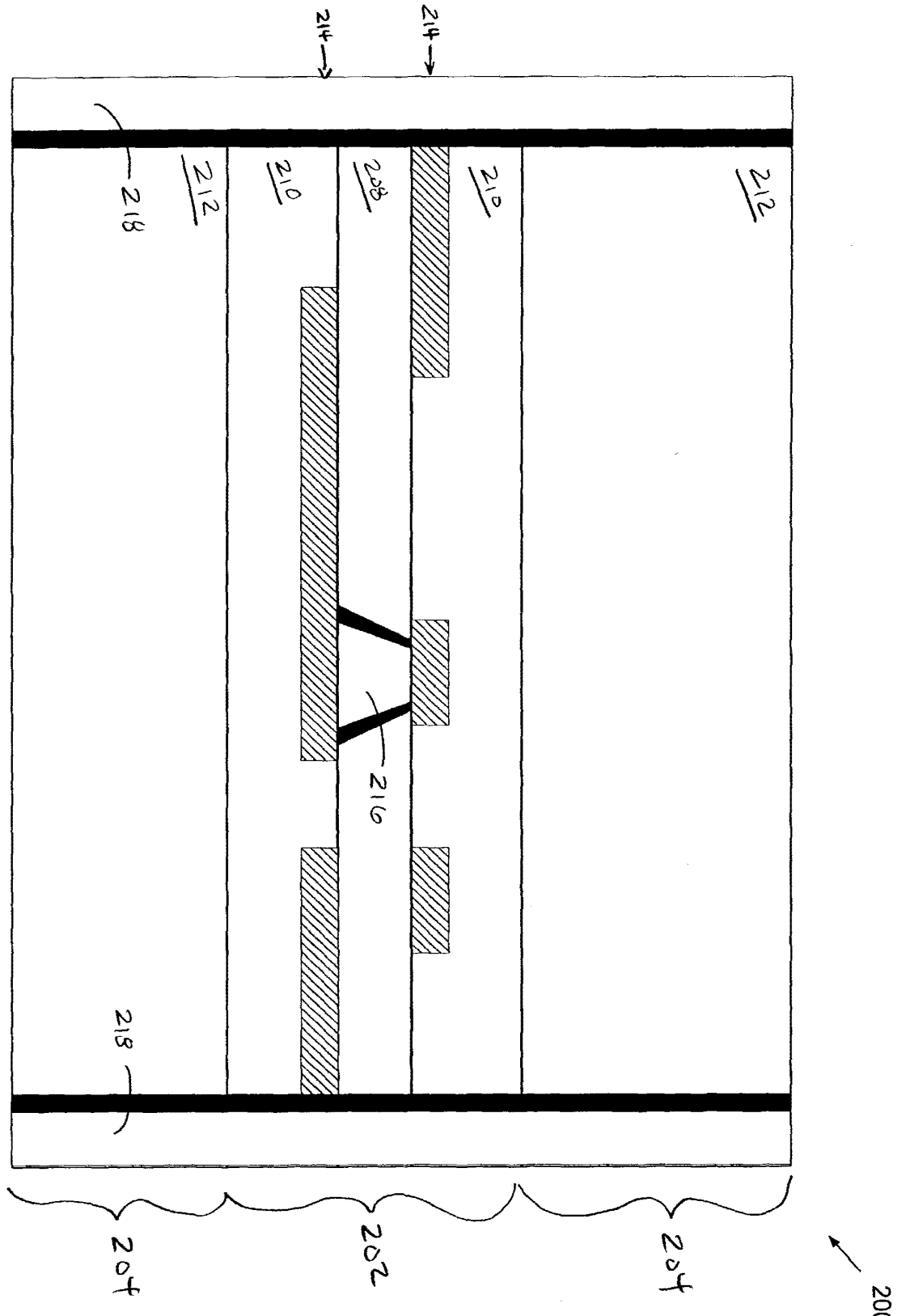


FIG. 2A

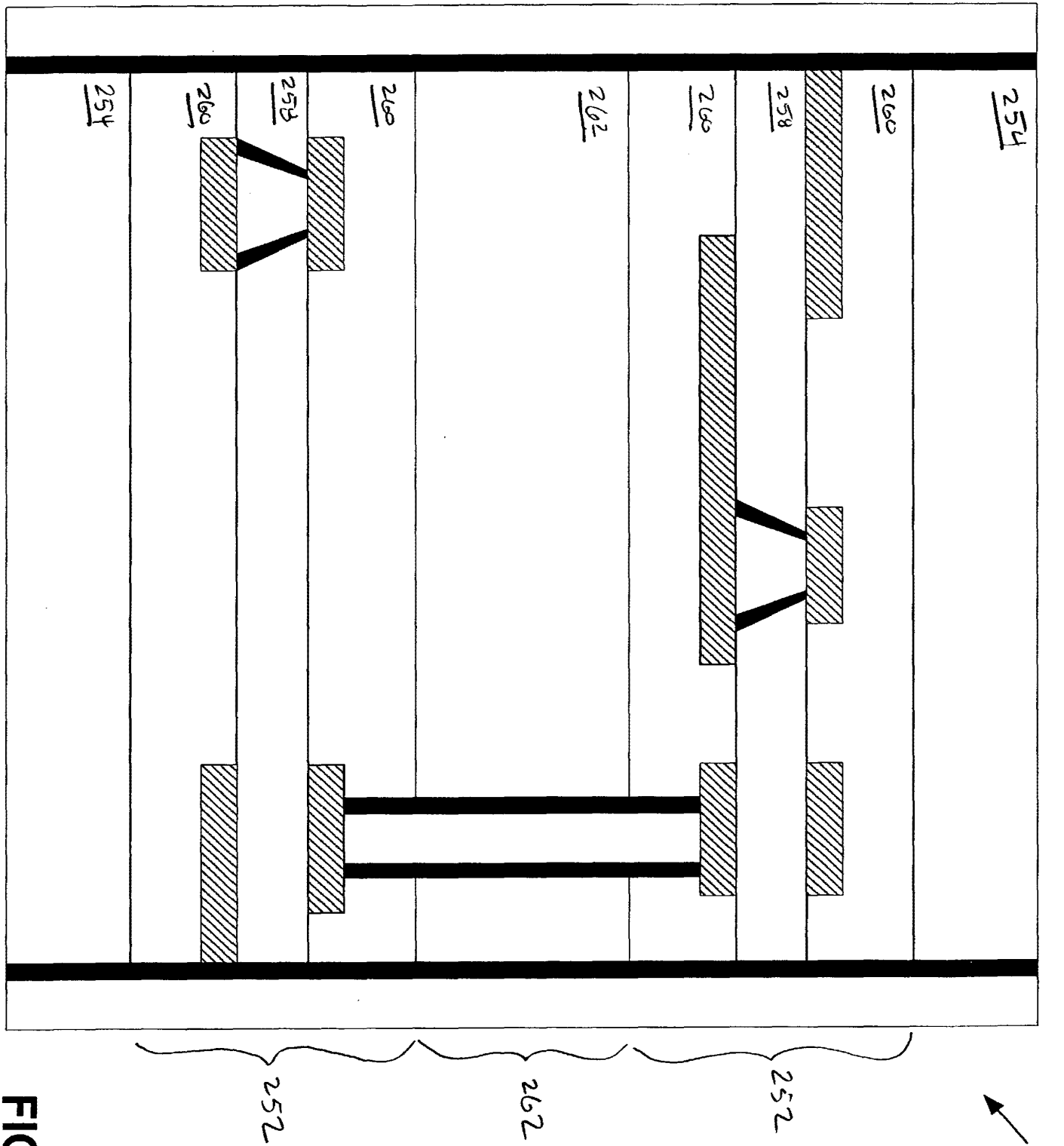
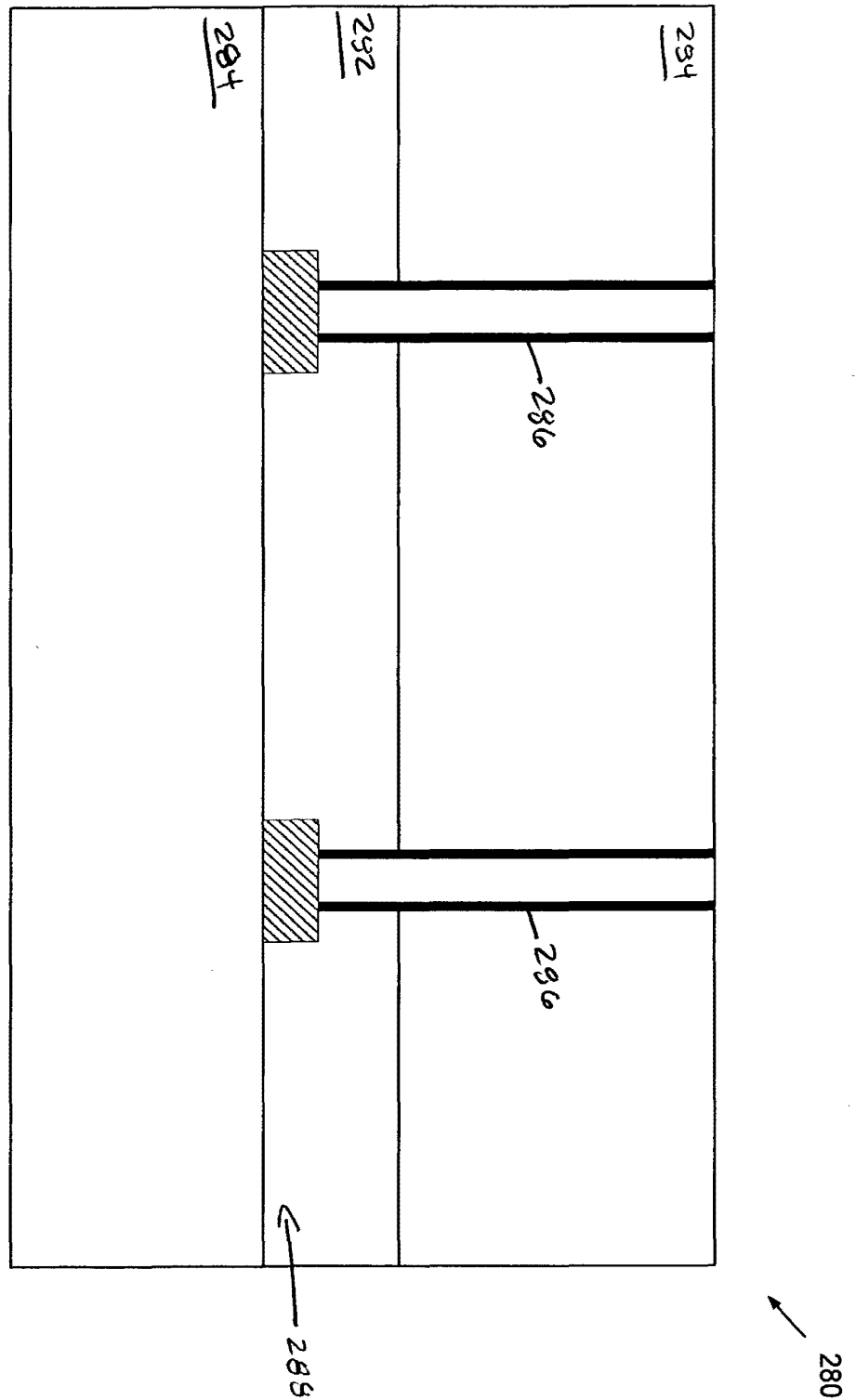


FIG. 2B

FIG. 2C



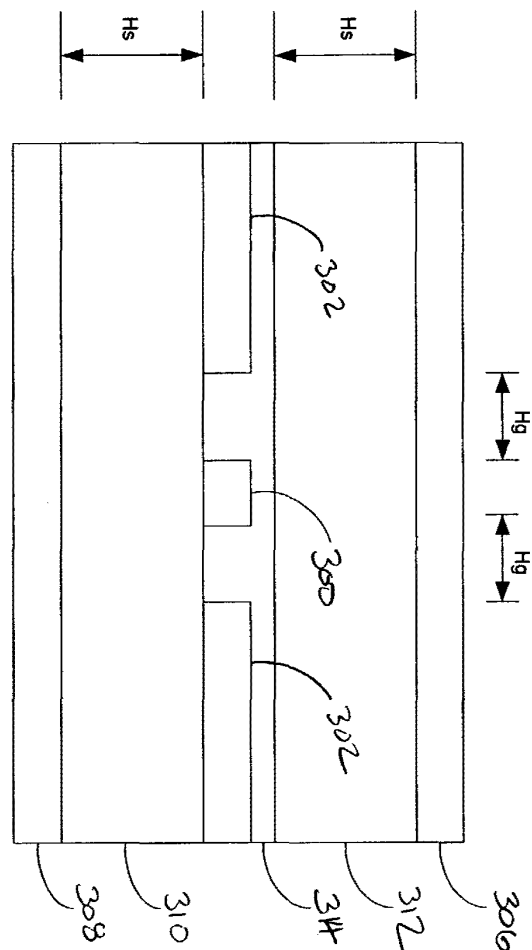


FIG. 3A

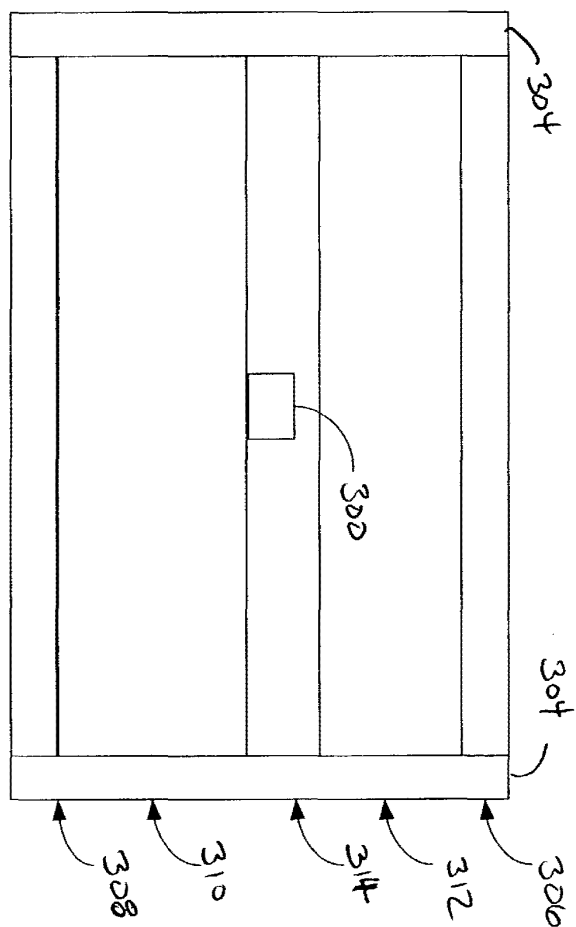


FIG. 3B

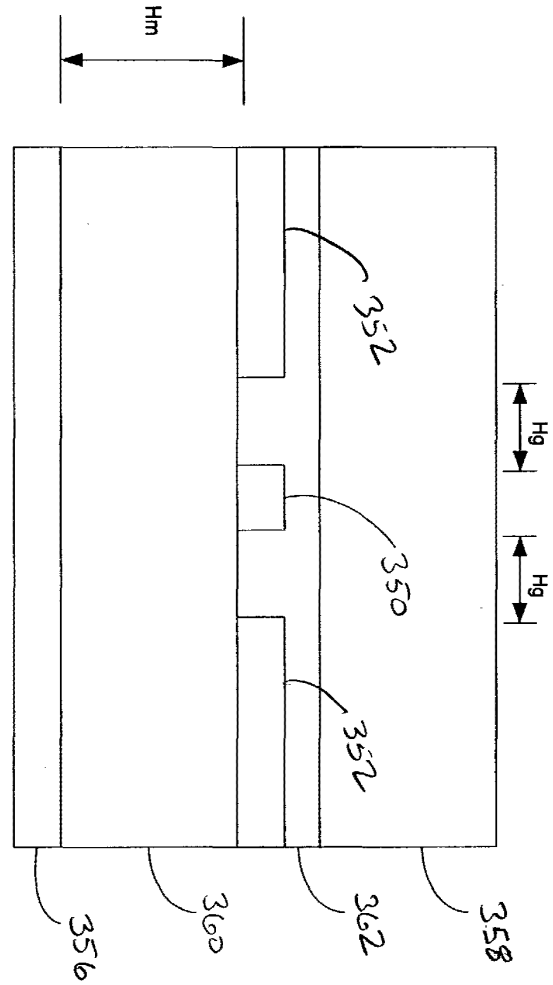


FIG. 3C

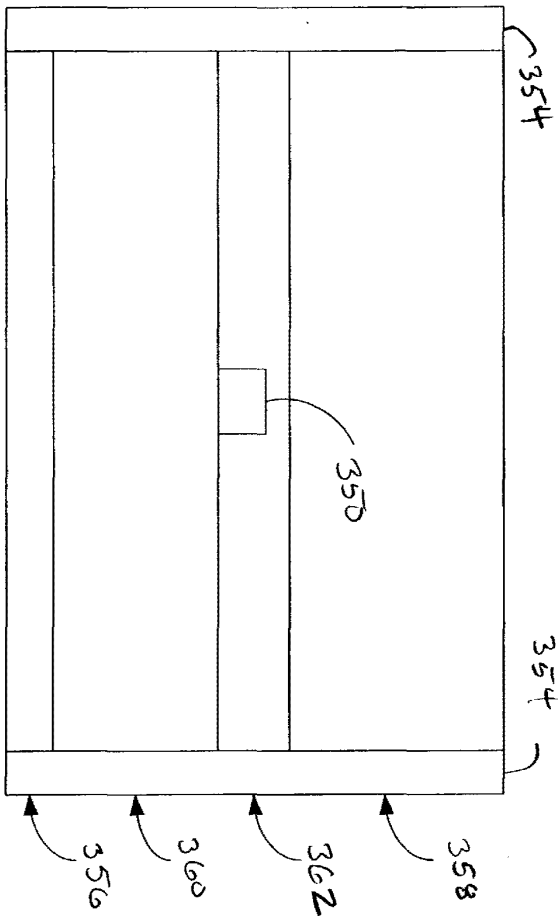
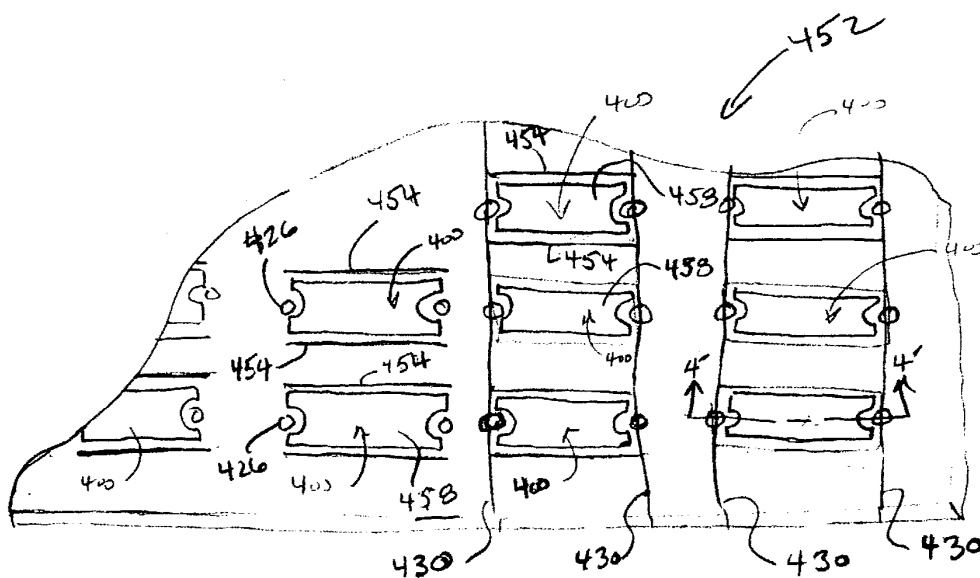
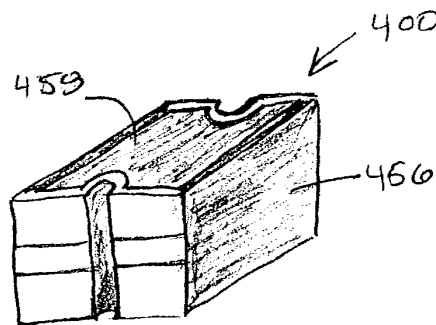
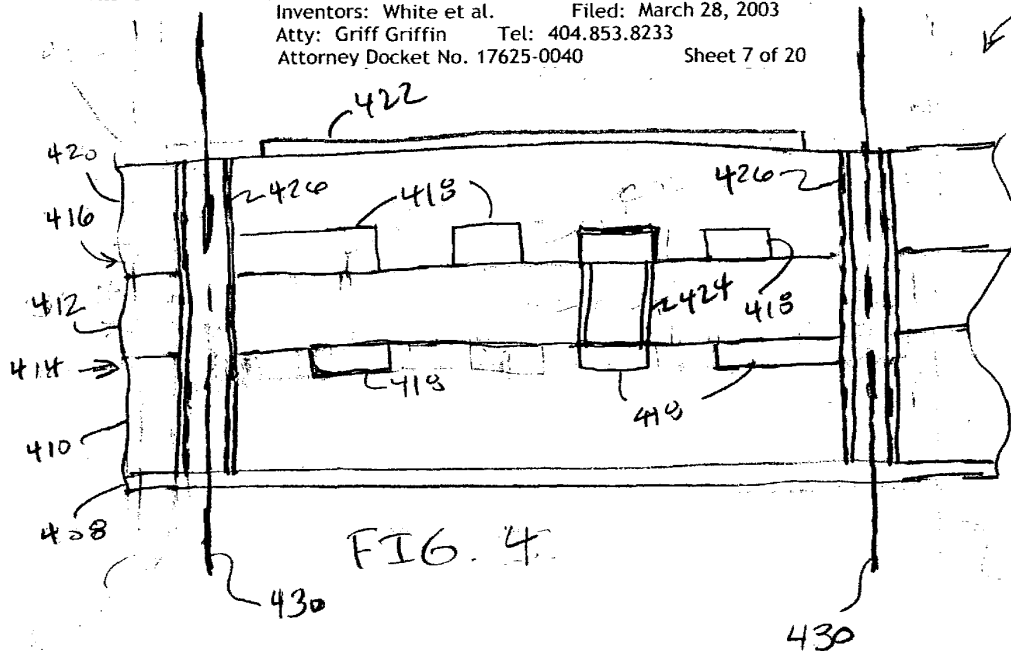


FIG. 3D



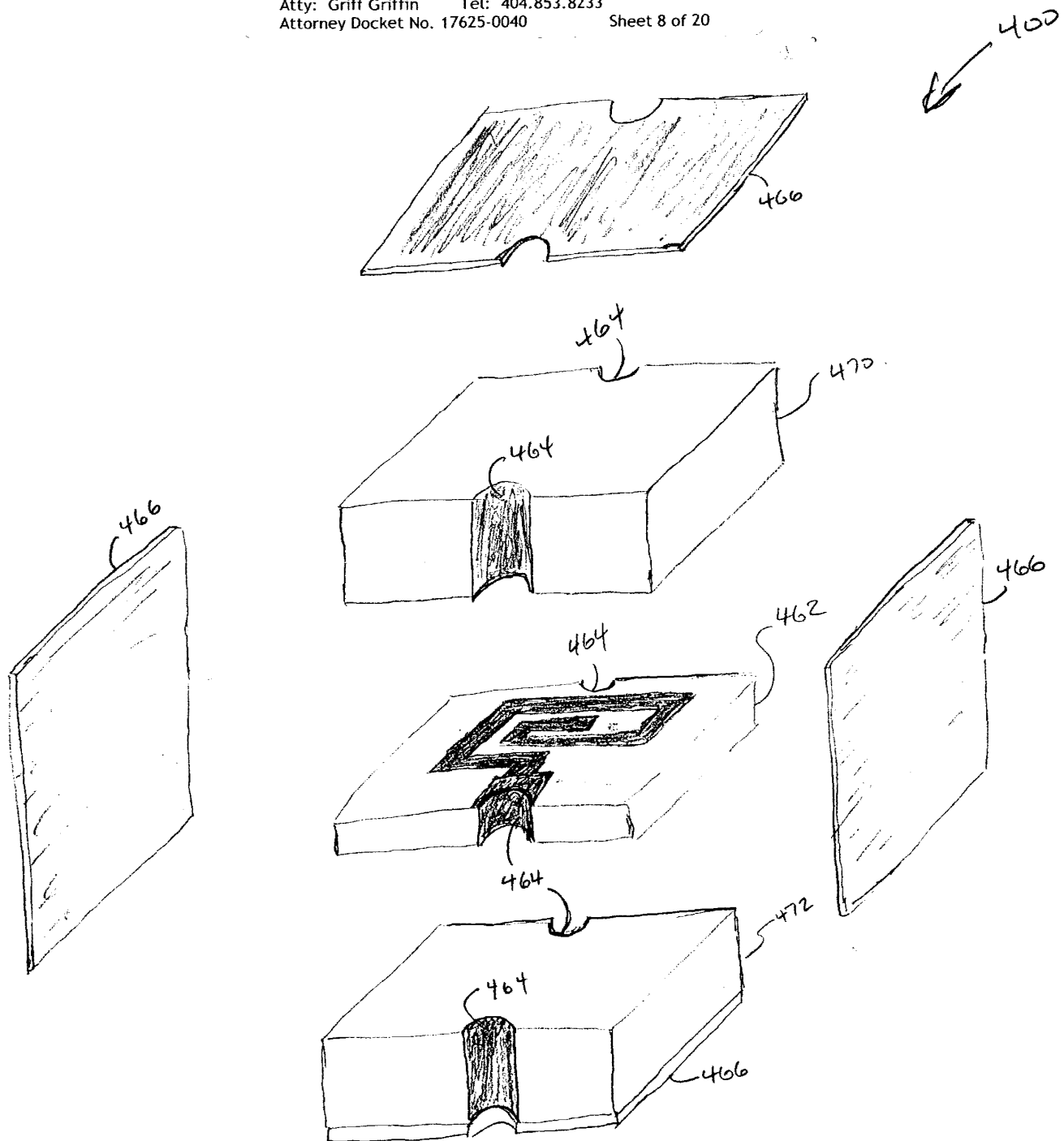
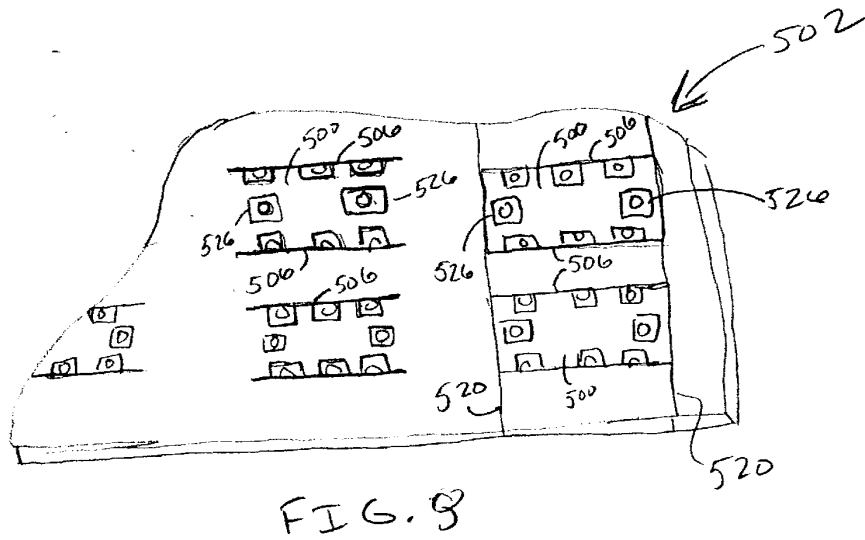
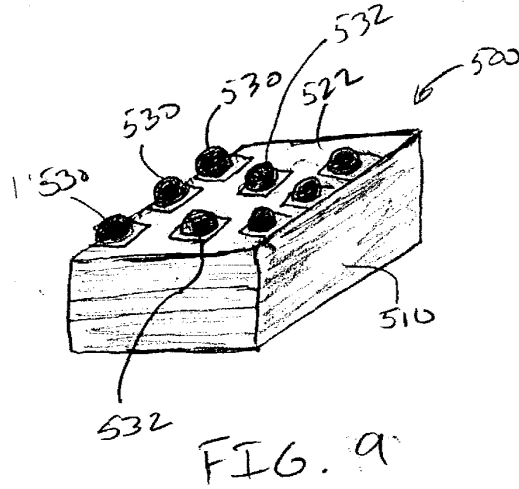
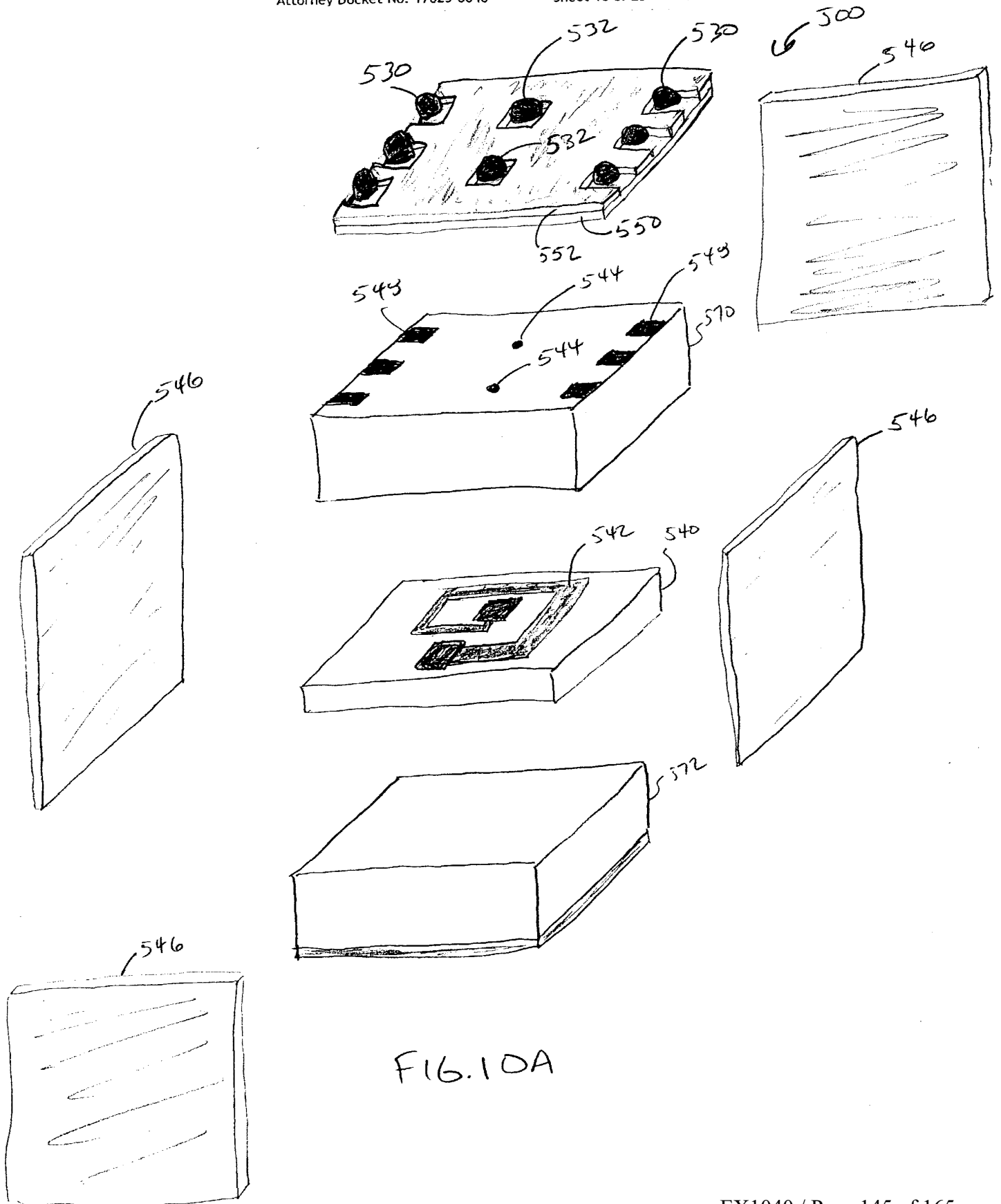


FIG. 7





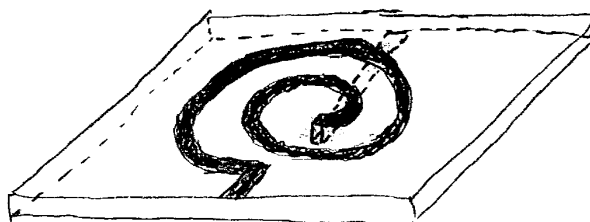
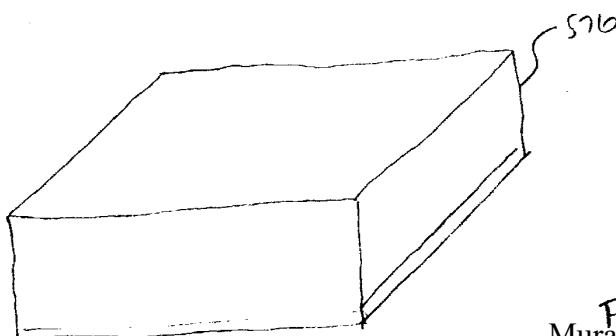
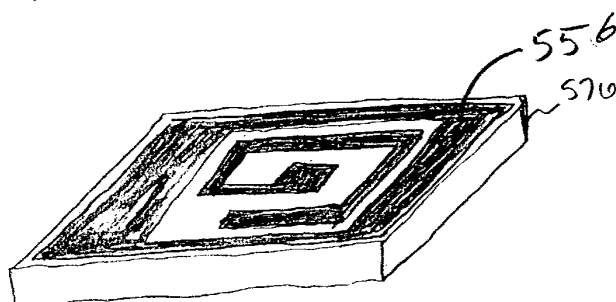
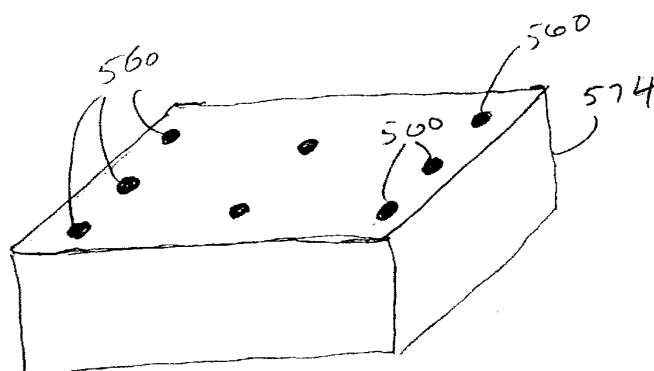
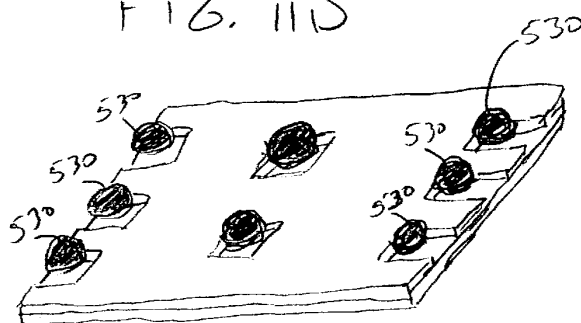
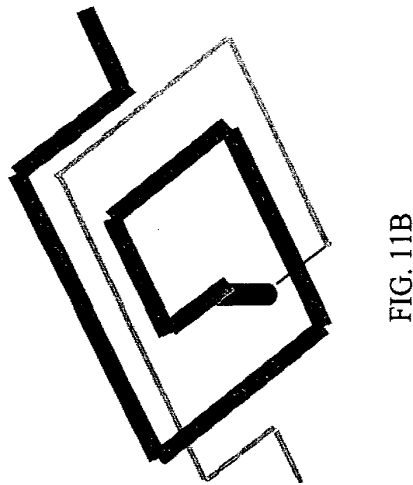
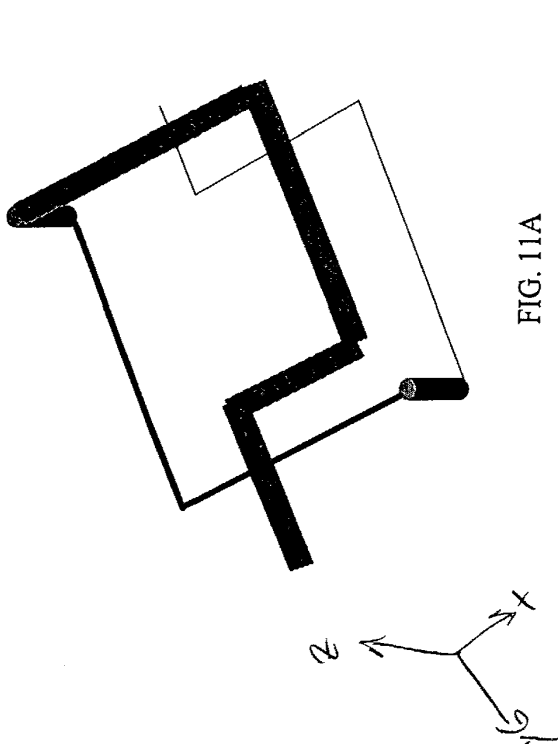
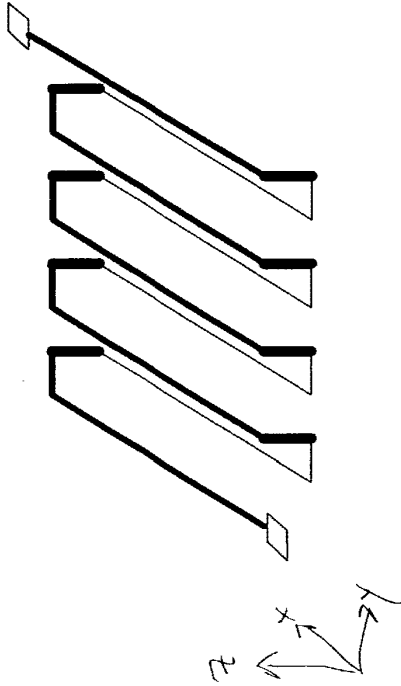


FIG. 11D





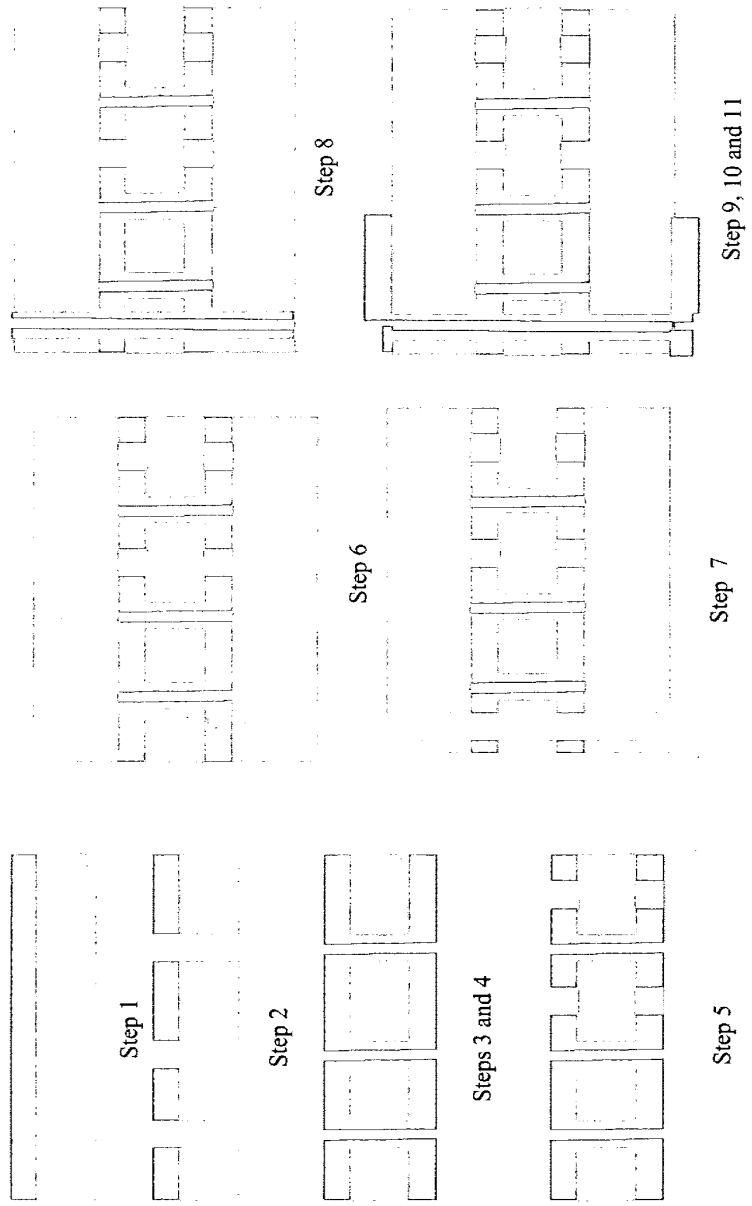


FIG. 12A

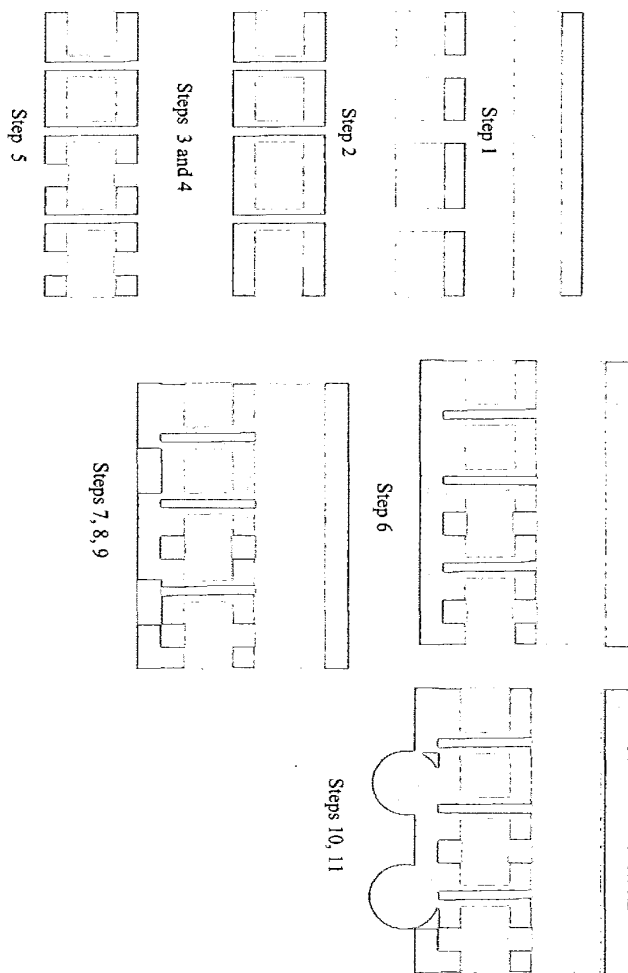


FIG. 12B

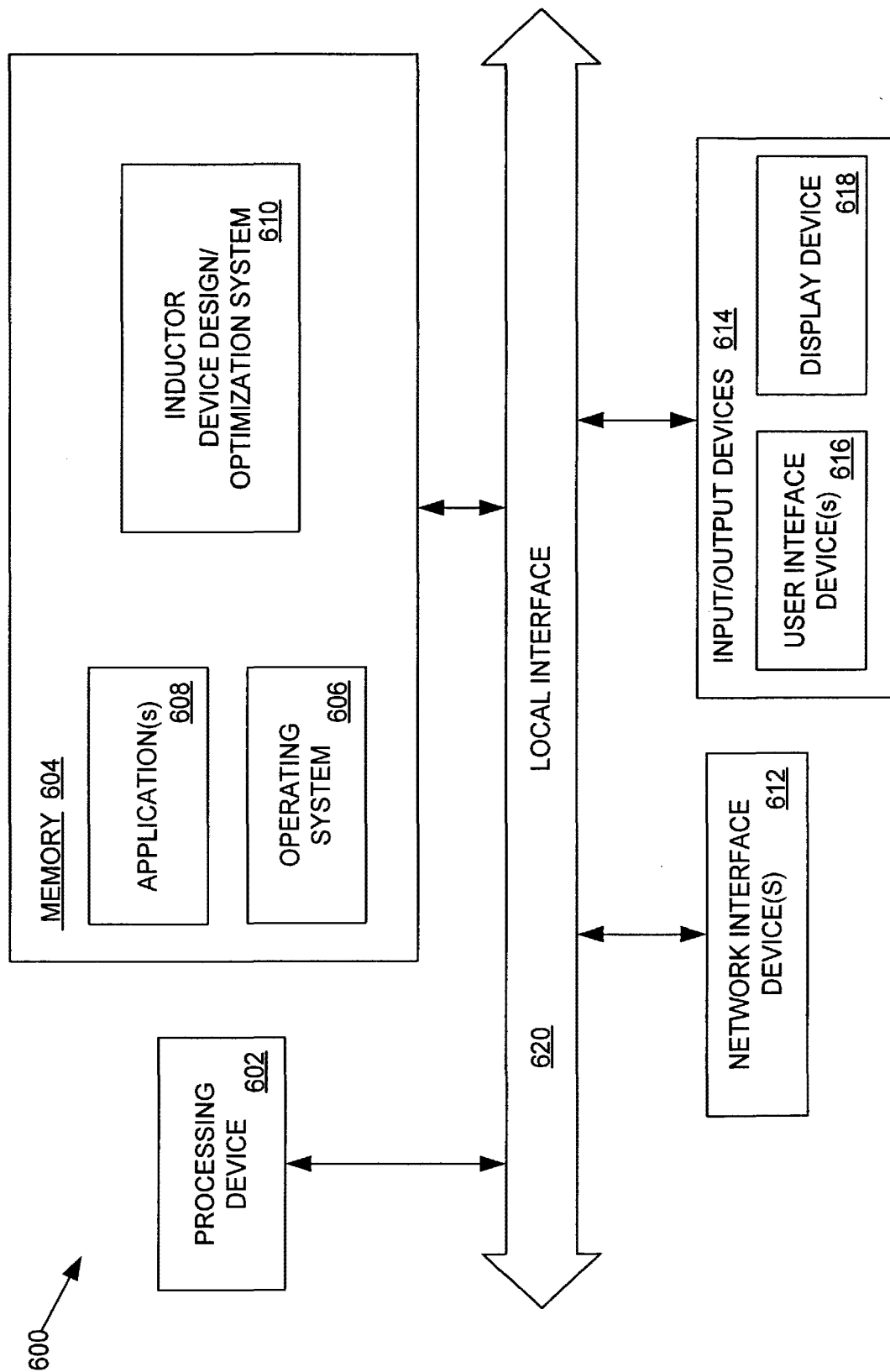


FIG. 13

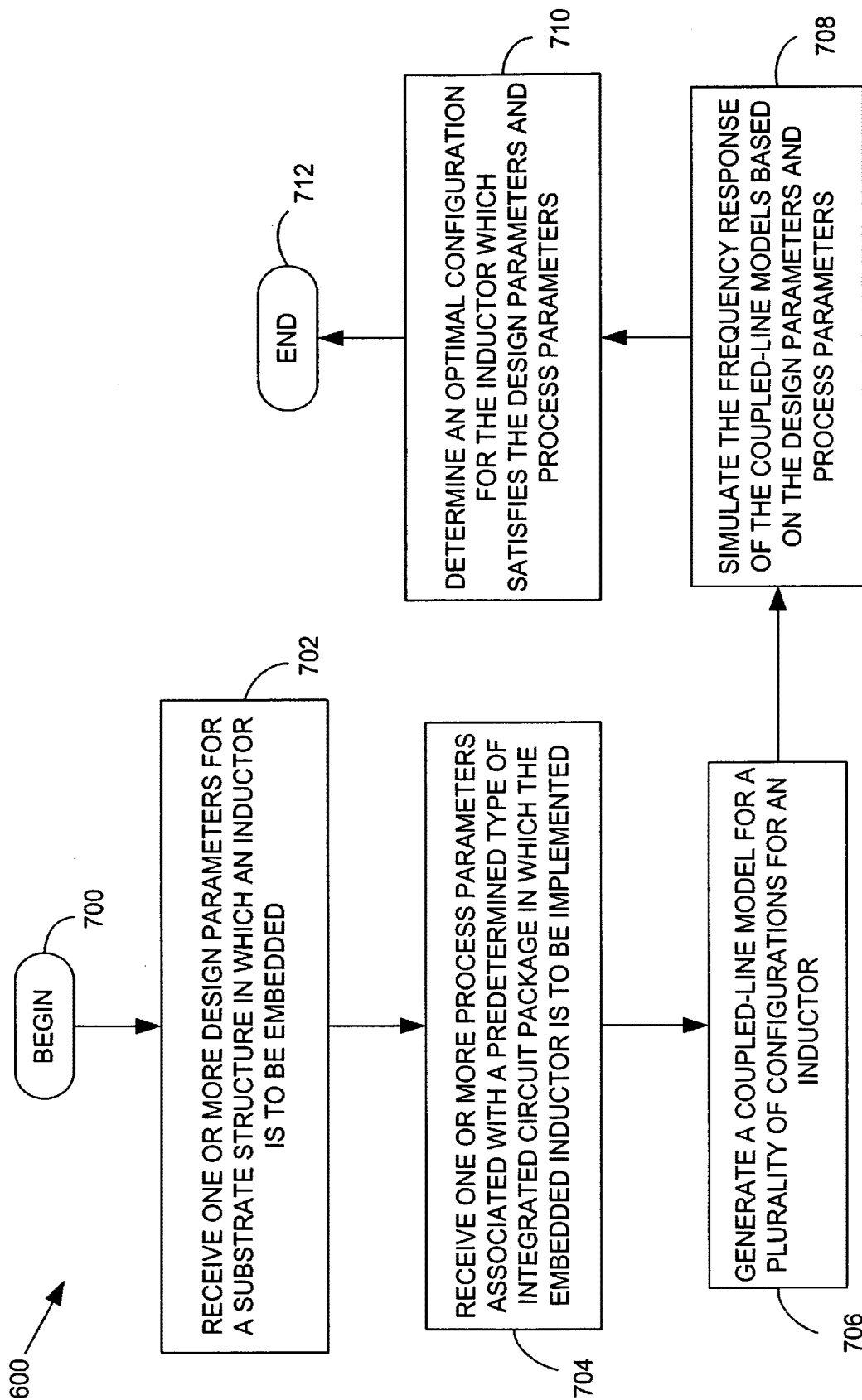


FIG. 14

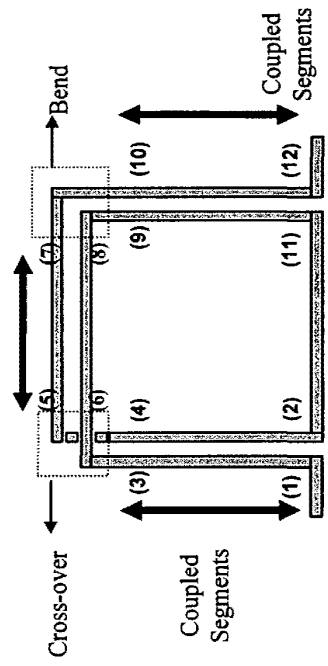


FIG. 15

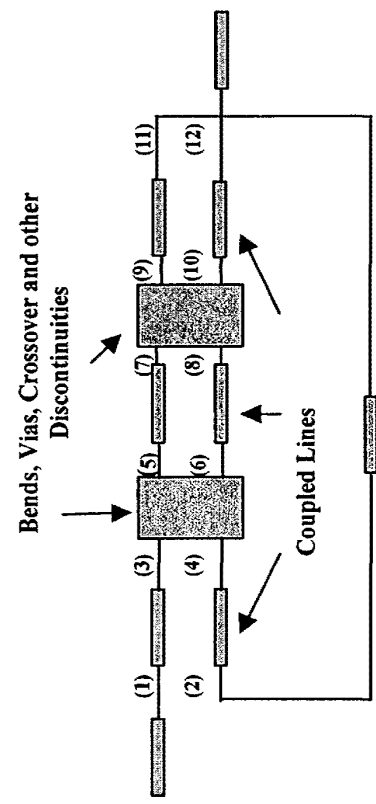


FIG. 16

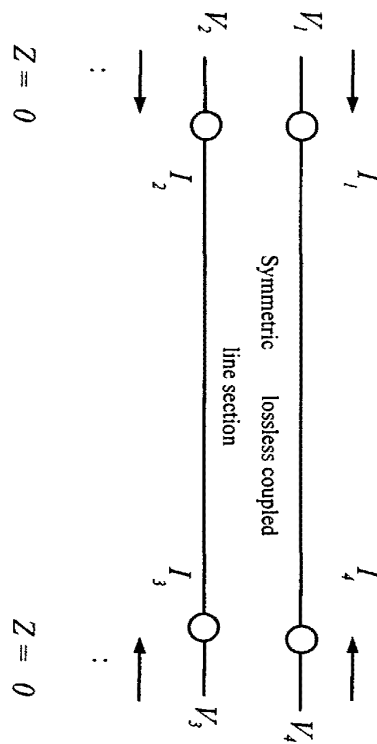


FIG. 17

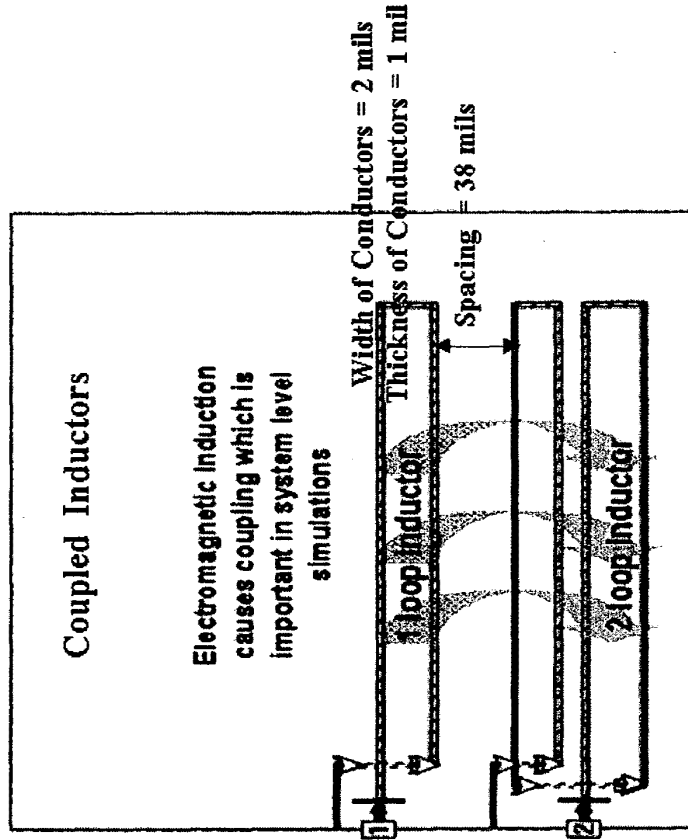


FIG. 18

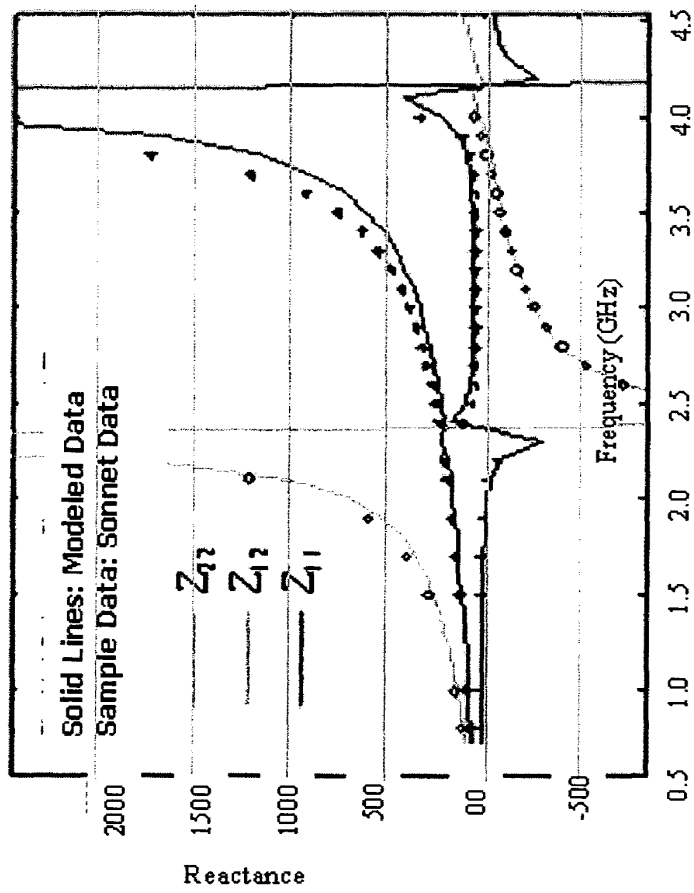


FIG. 19

U.S. Provisional Application
No. 60/391,742 filed 6-26-2002

06 - 27 - 02 062606 AP20V

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Express Mail Label No.: EL 681042906 US

INVENTOR(S)

Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
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GEORGE	WHITE	MARIETTA, GEORGIA USA
MADHAVAN	SWAMINATHAN	MARIETTA, GEORGIA USA

☐ Additional Inventors are being named on the 1 separately numbered sheets attached hereto.

TITLE OF THE INVENTION (280 characters max)
**PASSIVE COMPONENT ARCHITECTURES IN MULTI-LAYER
LIQUID CRYSTALLINE POLYMER (LCP) SUBSTRATES**

CORRESPONDENCE ADDRESS

☐ Customer Number or Bar Code Label	(Insert Customer No. or Attach bar code label here)	Or ☒ Correspondence address below
NAME	Office of Technology Licensing Georgia Tech Research Corporation Attention: Director	
ADDRESS	505 Tenth Street, NW	
CITY	Atlanta	STATE Georgia
COUNTRY	U.S.A.	ZIP CODE 30332-0415
	TELEPHONE 404-894-6287	FAX 404-894-9728

ENCLOSED APPLICATION PARTS (check all that apply)

- ☒ Specification Number of Pages 7 ☐ CD(s), Number
- ☐ Drawing(s) Number of Pages ☒ Other (Specify) Return postcard
- ☒ Application Data Sheet. See 37 CFR 1.76.

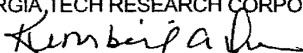
METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

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This invention was made by an agency of the United States government or under a contract with an agency of the United States Government.

- ☐ No.
- ☒ Yes, the name of the U.S. Government agency and the Government contact number are: **U.S. Army Missile Command-
Contract No. DAAH01-99-D-R002-0032**

Respectfully submitted,
GEORGIA TECH RESEARCH CORPORATION

SIGNATURE: 

TYPE or PRINTED NAME: Kimberly A. Dunn,
Patent Coordinator

Date: 6/26/02

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **DALMIA, et al.**

For: **PASSIVE COMPONENT ARCHITECTURES IN MULTI-LAYER LIQUID CRYSTALLINE POLYMER (LCP) SUBSTRATES**

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FOR PROVISIONAL APPLICATION**

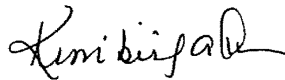
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Kimberly A. Dunn
Patent Coordinator

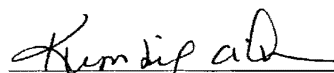
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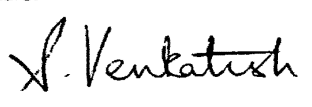

Kimberly A. Dunn

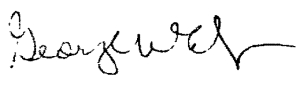
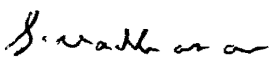
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Short Title: Integrated passive architectures in LCP based substrates	
Previous Invention	
Is this invention related to a previous invention disclosed to the OTL? ☐ Yes ☐ No	
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Phone: (404) 894-7892	Home Address: 115 N. Clublands Ct, Alpharetta, GA 30022
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Email: dalmia@ee.gatech.edu	Fax: (404) 894-9959
	Email: dalmia@ee.gatech.edu
Execution by Inventor(s): I/We inventor(s) hereby solemnly swear and affirm under oath that I/we am/are the only inventor(s) of this invention and that I/we have not knowingly omitted the inclusion of any other inventor(s) besides me/us, and that the information provided in this disclosure is, to the best of my/our knowledge, true and accurate.	Signature: 
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Invention Description			
Brief Description: (please attach more detailed descriptions, any support materials, reports) Novel compact passive architectures to be used for a portable telephone, data and internet access and the like, which can include several multilevel or planar inductors(Ls), a plurality of short-circuited and open-circuited transmission line resonators(Ts), and several metal-insulator-metal capacitors(Cs) in a stripline, microstrip or coplanar waveguide (CPW) topology constructed using metal patterning on several layers of LCP. The invention utilizes novel design ideas and novel processing techniques for integrated passives for high frequency applications. The material, liquid crystalline polymer, which has been around in production for a few years has excellent electrical, thermal and mechanical properties, but its use for passive architectures has not been explored. The invention discloses a novel method for the fabrication of high density multilayer structure using alternate layers of low and high temperature LCP. The invention also discloses novel design ideas which together with the electrical properties of LCP provides for extremely high quality compact passive devices. The proposed new technology impacts not only inductors, capacitors and resonator elements, but also provides for passive architectures such as bandpass filters, diplexers, baluns, power combiners and power dividers, low-pass filters and high-pass filters which all use various configurations of Ls, Cs and Ts. The increased quality, reduced cost compared to ceramic and thin-film on silicon/glass technologies used for passive integration and small sizes are well placed to make a huge impact in the current and future markets. However, the requirements such as frequency of interest, insertion losses, size allocation, cut-off frequencies, etc are almost always dependent on the customers particular needs. As an example, the design of bandpass filters for a commercial communications standard, Bluetooth (2.45 GHz), has been explained with circuit details, topological and implementation details.(Attached Appendix A for description, schematics and topology of front-end bluetooth filter)			

Source of SupportDid this invention result from sponsored research? ☒ Yes ☐ No

If NO, how was this work funded, including salaries, charges of time, materials, supplies, equipment?

If YES, please provide information on all:

Sponsor:

GIT Project Number:

Sponsor:

GIT Project Number:

Was this project conducted through or associated with a Georgia Tech Center?

☐ Yes ☐ No

If YES, list name of Center.

Did you use any material obtained from another party in developing this technology?

☐ Yes ☐ No

If YES, please list source: (attach copy of material transfer agreement if applicable)

Establishment of Invention History

Please provide your best estimate for the date when the following occurred (will occur):

Date(s):

A. Conception of Invention

B. First written description (please attach a copy if available)

C. First oral disclosure

To whom:

D. First disclosure outside of Georgia Tech (e.g. abstract, proposal, paper submission, talk, or meeting with industry – please attach a copy if available)

To whom:

E. Completion of model or prototype

F. First successful operational test:

G. Is a publication or other disclosure planned within 6 months? ☒ Yes ☐ No

If YES, Disclosure Date:

Type of disclosure:

Prior ArtInventors are highly encouraged to conduct a literature and patent search. Two useful sites are: 1) www.uspto.gov and 2) www.surfip.gov.sgA. Has a patent or literature been conducted? ☒ Yes ☐ NoB. Are there any related patents or publications known to you? ☐ Yes ☐ No

If Yes, please attach copies or reference list.

Commercialization Potential**A. What are the immediate and/or future applications for the invention?**

Multi-layer organic build-up technology capable of being processed on large areas (18"x12") at lower temperatures compared to competing smaller area (4"x4") higher temperature ceramic and thin-film deposition technologies for integrated passive devices (IPDs) and passive architectures offers a cost effective solution for the applications mentioned earlier. We have the advantage of having first-hand processing knowledge of an organic laminate such as liquid crystalline polymer (LCP) with enhanced electrical, thermal and mechanical properties that address the emerging needs for low cost high frequency materials that can support mixed signal applications up to 20 GHz. An IPD made using LCP has the potential to save space, through use of various wire-bonded, ball-grid-array (BGA) and flip-chip (FC) implementations, which is particularly good for designs operating from the low GHz to 15 GHz range. Moreover, the advantages of lower cost, lower temperatures and large area processing capabilities make it possible to use LCP technology as cost effective solution over ceramic and silicon based IPD's that currently dominate the market. The electrical attribute of a few prototypes such as stand alone inductors, capacitors and bandpass filters seem to rival or better the performance of similar sized ceramic and TFOS packages.

B. What are the limitations that must be overcome prior to practical application?

The electrical design techniques for electrical circuit synthesis, physical layout and electromagnetic simulation are in place and we have excellent model-to-hardware correlation for pre-packaged passive components such as inductors, capacitors, resonators, and filters. Low cost fab techniques have been realized using techniques similar to PWB fabrication with some notable exceptions. These exceptions (details available if required) involve plasma pretreatments, high temperature vacuum lamination, and laser drilling. To date we have shown the feasibility of metallization, stacking, lamination, drilling both electrically and circuitization. We are developing technologies, both electrical design rules and processing techniques that will allow us to package elements in BGA, CSP and micro BGA formats in an all LCP construction. These formats will allow for the continuing drive to realize smaller, and low profile construction for portable and consumer products, even though this technology can be utilized for high performance applications such as base stations and servers. Extensive reliability testing will be performed in the end to ensure high quality manufacturing processes and meet current product specifications. We do not foresee any limitations to be overcome before application of this idea.

C. What are the advantages of the invention versus present technologies?

Novel design structures which can be designed for two metal layer will significantly reduce fabrication costs and make this product much more competitive than any ceramic based filter currently on the market. Couple the design with the fact that IPS will develop their fabrication process on 12" x 18" substrates as compared to existing technologies which fabricate their structures on 4" x 4" ceramic substrates, a 25x increase in productivity will be realized. Surface mount IPDs are typically singulated and then metallized first by sputtering and then solder plated. IPS will package its components in a large area format by screening solder paste over the terminals of the large area substrate, reflow to form the BGA/CSP balls and then singulate. Again this offers a significant benefit in terms of cost and flexibility over conventional practices. We will have a distinct advantage with electrical testing of the components. Since the first set of designs are two layer designs testing and design becomes very easy compared to ceramic components which typically used several layers (>5 layers typical). However, we recognize the need for multilayer implementation in the near future. We already have novel process capability for multilayer configurations if the need arises and have also initiated building an extensive Integrated Passive Component Design Library for multilayer configurations to reduce design time. Unlike the LCP and ceramic processing which allows for multilevels of metalization, it is very hard to implement more than two metal levels in thin film technology.

D. Please provide any available data or information on market potential/size.

The IPD market is poised for a change. The Multilayer Ceramic IPD market is expected to grow to \$3.8 Billion and the TFOS market to \$2 billion by 2004, which adds to ~\$6 Billion growing at an annual rate of 4-7%. We believe the proposed technology can firstly capture a big chunk of this market and also provide a huge impetus towards the move for sub-systems such as modules (VCOs, LNAs, etc) which also use a combination of Ls, Cs and Ts for matching and biasing circuits, and ultimately lead to the intergration of entire systems.

E. Is work on the invention continuing? ☒ Yes ☐ No**F. Do you know of any appropriate industrial organizations that may be interested in licensing this technology? (Please attach additional sheet if more space is required.)**

Company Name	Contact Person	Contact Information
Rogers		
AMCOM		

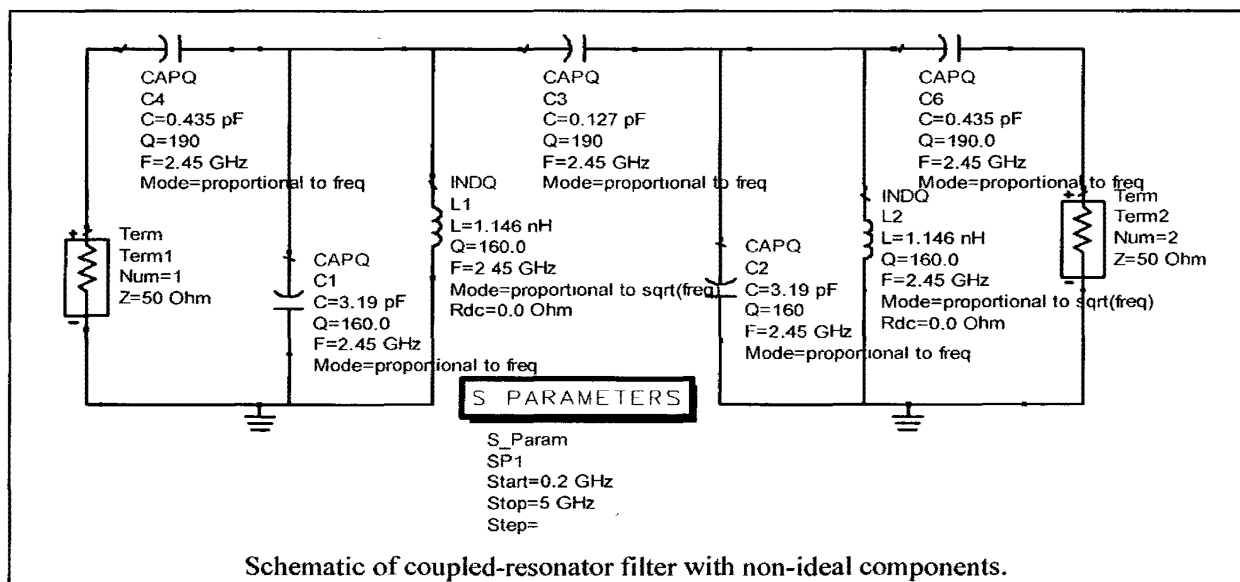
Execution by Witnesses

This disclosure should be witnessed by two individuals who are not co-inventors and who are technically qualified to understand the subject matter.

	Print Name	Signature	Date
I have read this invention disclosure (including attached pages, if any) and understand its subject matter	DEAN A. SUTTER	<i>Dean A. Sutter</i>	6/17/02
I have read this invention disclosure (including attached pages, if any) and understand its subject matter	Michael E. Toole	<i>Michael E. Toole</i>	6/17/02

Application 1: Band-pass filters Specific standards were targeted so that the frequency of application and the requirements of each IPD can be estimated. The Bluetooth (2.45 GHz) standard is a popular IEEE standardized protocol for short-range wireless mobile communications. The currently released standard, v1.1, supports 79 adjacent channels with a channel spacing of 1 MHz. The FCC allocated spectrum for this application is 2402 MHz - 2480 MHz. The nominal characteristics of a commercial available front-end RF filter (volume: 12mm³ and height: 1.4 mm) using multi-layer ceramic technology from Murata, for this application are as follows: impedance of 50 ohms; center-frequency $f_0 = 2.45$ GHz; passband (BW) $f_0 \pm 50$ MHz; maximum insertion loss in bandwidth ~ 2.7 dB; suppression of GSM900 and GSM1800 frequencies is excellent; and the maximum ripple in bandwidth is 1.5 dB. Currently IPD's such as the filter discussed here can sell for \$3-\$5 based on volume purchased. When comparing our LCP IPD substrate to those typically used for ceramic based IPD, the LCP will yield more than 6x the number of components than ceramic using a fewer number of layers to achieve similar or better performances. **We understands the high impact of the proposed technology not only for filters and resonator elements, but also for other IPDs such as Diplexers, Baluns, Power combiners and power dividers, low-pass filters and high-pass filters in the near future. However, to show high impact has chosen to prototype front-end RF filters as its first products for 2.45 and 5-5.8 GHz applications.**

The filter currently designed has a volume of 12mm³ with a nominal height of 0.7mm. It comprises of two-coupled resonator tanks with high attenuation, shielding and isolation. Given the current process it is possible to fabricate ~ 2000 such IPD's (allowing a net area 50 mm² for each filter which includes filter-to-filter spacing) on the typical 18"x12" boards which illustrates its cost effectiveness. Compared to the ceramic filter, the novel design betters the performance with a nominal loss of ~ 1.6 dB and a ripple of ~ 1 dB. With the flexibility of the proprietary process, novel electrical design techniques, and technical know how, ASIP™ has shown that the design time for IPDs such as the bandpass filter for various other standards is extremely short and extremely scalable. For example, the current design which requires just 2 metal layer patterning compared to the multi-layers in ceramic filters helps reduced design time and processing time.



WHAT IS CLAIMED:

1. An apparatus as described herein and as shown in the Figures, including each and every limitation and embodiment; and
2. A method of operation as described herein and as shown in the Figures, including each and every limitation and embodiment.

