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[54] **LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME**

[75] Inventor: **Woo Sup Shin**, Kyungsangbuk-do, Rep. of Korea

[73] Assignee: **LG Electronics, Inc.**, Seoul, Rep. of Korea

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[30] Foreign Application Priority Data

Aug. 19, 1995 [KR] Rep. of Korea 25538/1995

[51] **Int. Cl.⁶** **G02F 1/136; G02F 1/1343; G02F 1/1345**

[52] **U.S. Cl.** **349/148; 349/149; 349/43**

[58] **Field of Search** 349/149, 148, 349/43, 139, 152, 147

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Primary Examiner—William L. Sikes

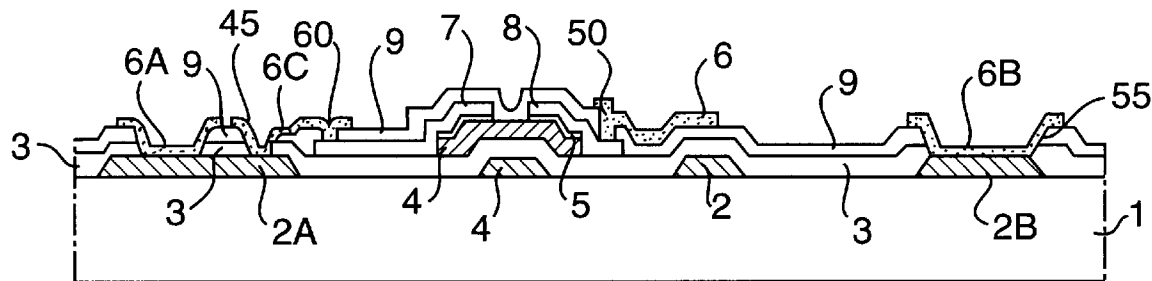
Assistant Examiner—Tiep H. Nguyen

Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.

[57] ABSTRACT

A method for fabricating a liquid crystal display is disclosed whereby a source and gate are exposed after the step of forming a passivation layer. As a result, the number of processing steps is reduced and yield is improved.

11 Claims, 5 Drawing Sheets



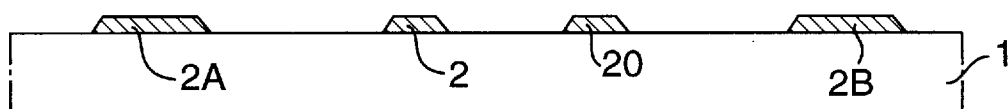


FIG. 1a
PRIOR ART

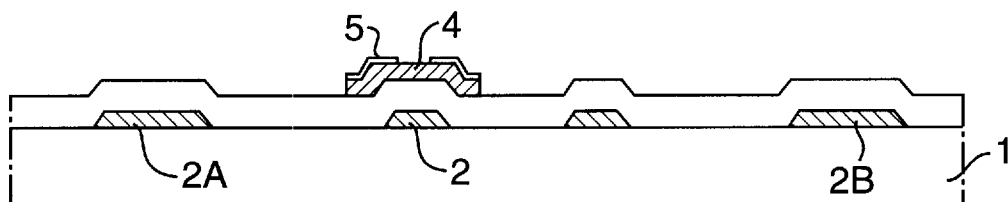


FIG. 1b
PRIOR ART

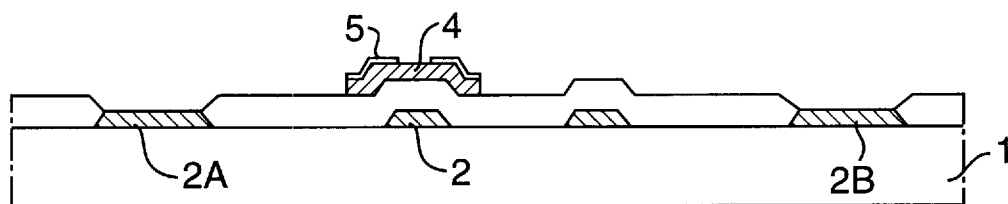


FIG. 1c
PRIOR ART

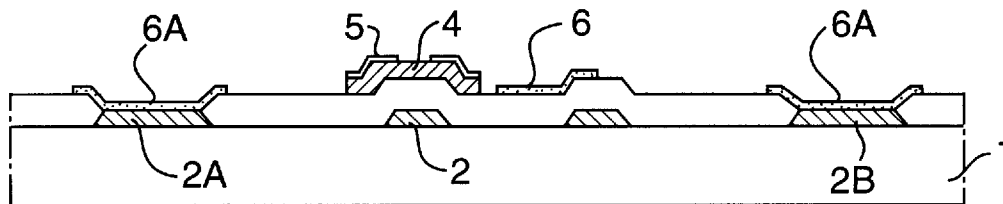


FIG. 1d
PRIOR ART

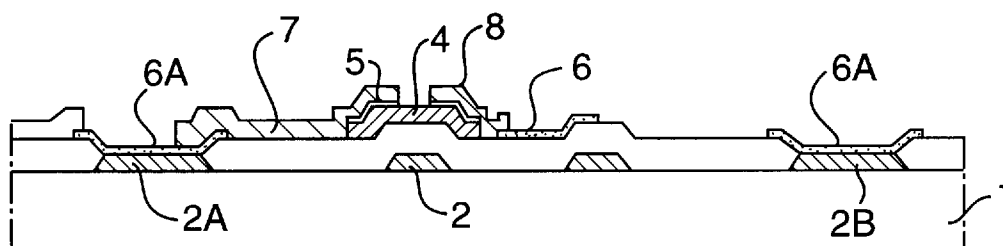


FIG. 1e
PRIOR ART

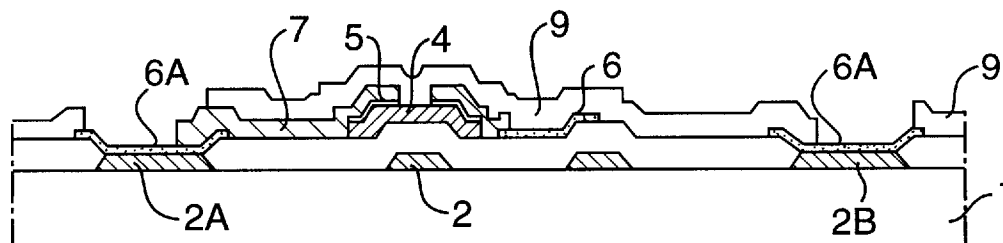


FIG. 1f
PRIOR ART

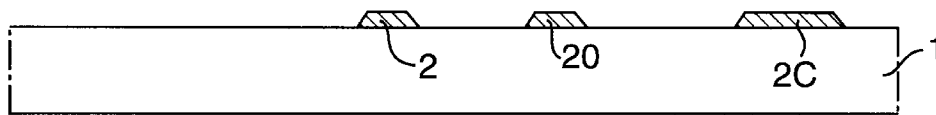


FIG. 2a

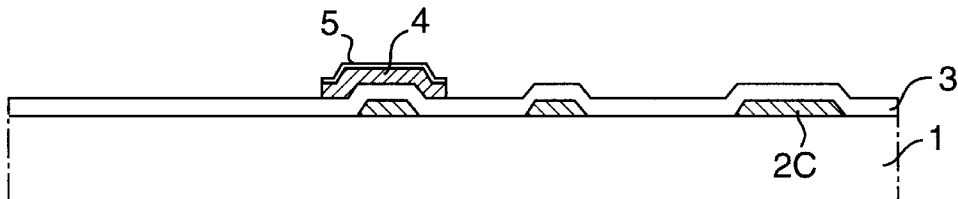


FIG. 2b

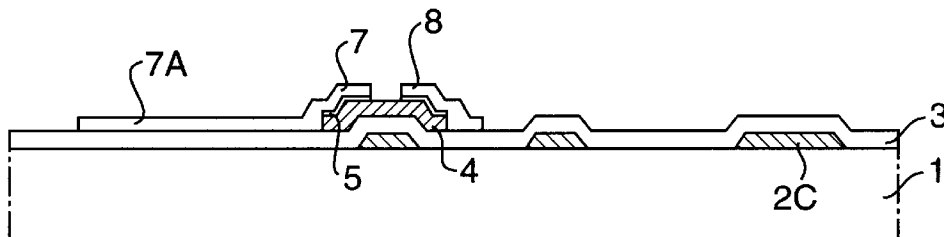


FIG. 2c

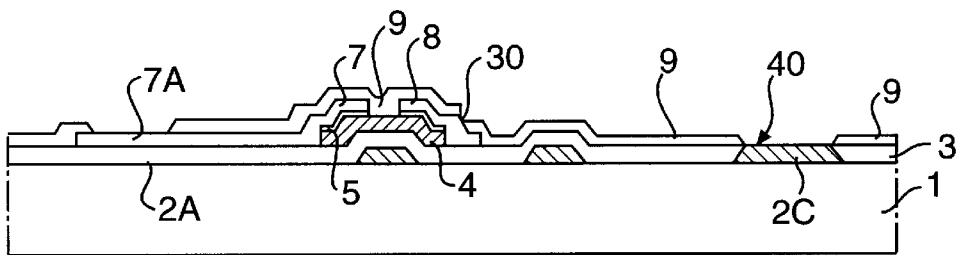


FIG. 2d

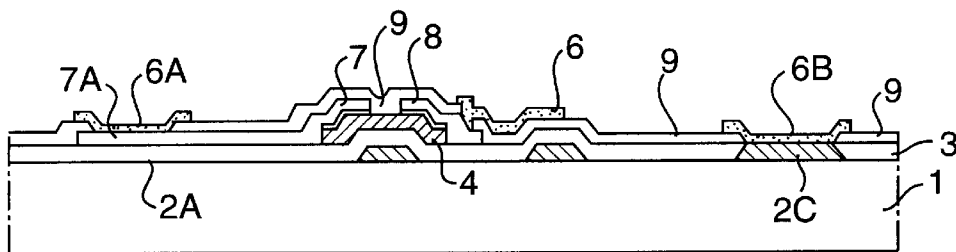


FIG. 2e

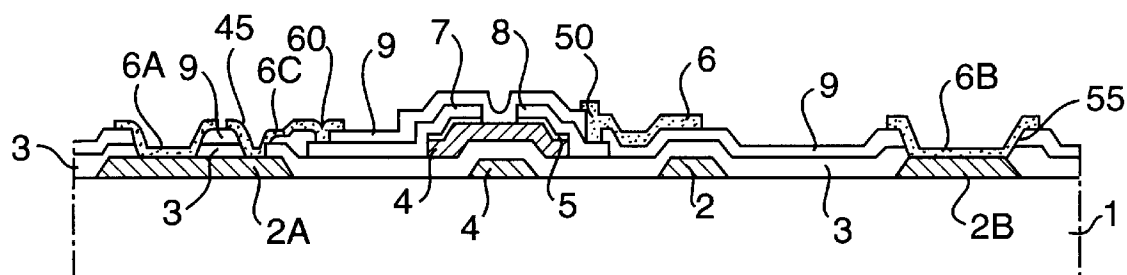


FIG. 3

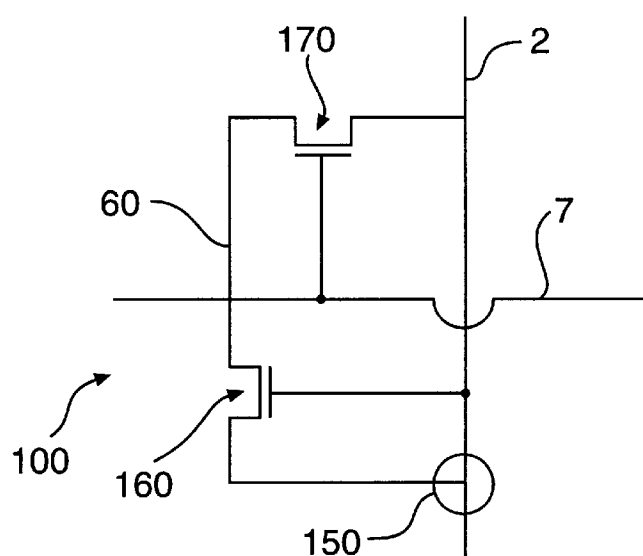


FIG. 4

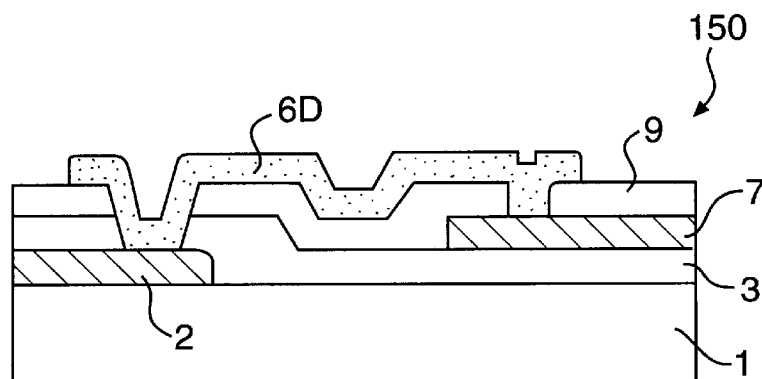


FIG. 5

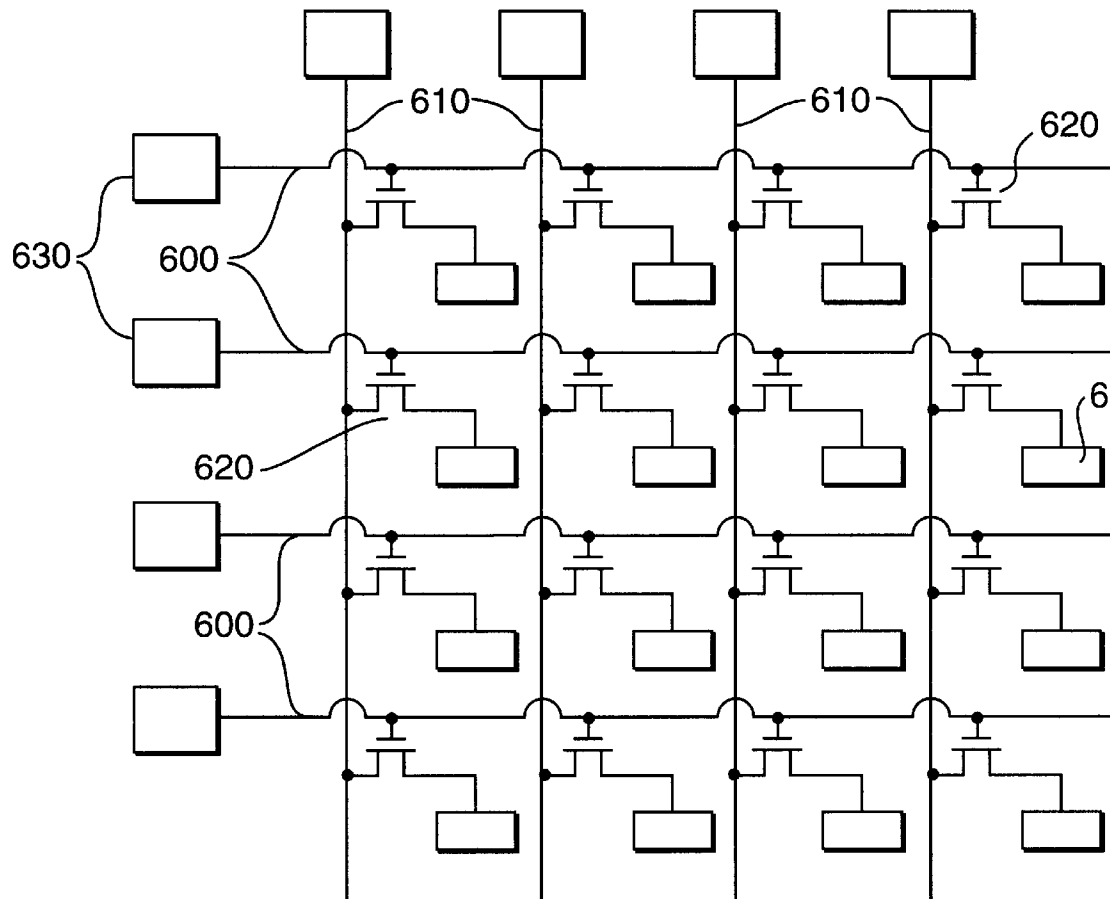


FIG. 6
PRIOR ART

LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME

This is a continuation of application Ser. No. 08/616,291, Filed Mar. 15, 1996.

BACKGROUND OF THE INVENTION

The present invention relates to a liquid crystal display (LCD) device and a method of manufacturing the same, and more particularly, to a liquid crystal display device having a combined source electrode and source pad structure.

Active matrix thin film displays include thin film transistors (TFTs) for driving the liquid crystal material in individual pixels of the display. As shown in FIG. 6, a conventional LCD includes an array of pixels each having liquid crystal material (not shown) sandwiched between a common electrode provided on a top plate (not shown) and a pixel electrode 6 disposed on a bottom plate. The bottom plate further includes a plurality of gate lines 600 intersecting a plurality of data lines 610.

Thin film transistors 620, serving as active devices, are located at intersecting portions of gate lines 600 and data lines 610. Gate lines 600 and data lines 610 are connected to the gates and sources, respectively of thin film transistors 620. In addition, pixel electrodes 6 are connected to respective drain electrodes of thin film transistors 620. Gate Pads 630 and Data Pads 640 are connected to the gate lines and data lines to receive datas from gate driver and data driver respectively.

A conventional method of manufacturing a liquid crystal display device including TFT driving elements will be described with reference to FIGS. 1a-1f.

As shown in FIG. 1a, a conductive layer is formed on a transparent glass substrate 1 and patterned to form gate 2, storage capacitor electrode 2D, source pad 2A, and gate pad 2B. Gate pad 2B is used for receiving a voltage to drive and active layer in the completed TFT device.

As shown in FIG. 1b, a gate insulating film 3, such as a nitride film or an oxide film, is formed on the entire surface of the substrate in order to electrically insulate gate 2. An amorphous silicon active layer 4 is formed on a portion of gate insulating film 3 overlying gate 2. Then, in order to reduce the contact resistance between the active layer and the source/drain regions in the completed device, and appropriately doped semiconductor layer 5 is formed on amorphous silicon layer 4 as an ohmic contact layer. Doped semiconductor layer 5 and amorphous silicon layer 4 are then etched in accordance with a predetermined active layer pattern.

Since a pad wiring layer is necessary in order to communicate information from an external driving circuit to the gate and source, a gate insulating film 3 is selectively etched to expose source pad 2A and gate pad 2B (see FIG. 1c). Next, as shown in FIG. 1d, a transparent conductive layer (ITO) is deposited on the entire surface of the substrate and patterned to form a pixel electrode 6, which is formed on a portion of the display pixel, while ITO patterns 6A and 6B are formed on source pad 2A and gate pad 2B, respectively.

As shown in FIG. 1e, the TFT is formed on the active layer and includes a conductive layer deposited on the substrate and simultaneously patterned to form source and drain electrodes 7 and 8, respectively. Source electrode 7 is connected to source pad 2A, and drain electrode 8 is contact with impurity-doped semiconductor layer 5 and pixel electrode 6. In the completed device structure, source electrode

7 conducts a data signal, received from a data wiring layer and drain electrode 8, to pixel electrode 6. The signal is stored in the form of charge on pixel electrode 6, thereby driving the liquid crystal.

As shown in FIG. 1f, a nitride film is deposited on the entire surface of the substrate as a passivation layer 9 in order to seal the underlying device from moisture and to prevent absorption of impurities. Passivation layer 9 is selectively etched to expose source-pad 2A and gate pad 2B, thereby completing the TFT.

In the conventional method described above, The source electrode 7 and pixel electrode 6 provided on the same surface of gate insulating film 3. Accordingly, processing errors can cause these electrodes to contact each other. As a result, shorts can occur, thereby reducing yields.

Further, since the source pad for the source wiring is composed of the same material as the gate, its contact resistance with the underlying source electrode can be high. In addition, at least six masking steps are required as follows: patterning the gate, storage capacitor electrode, source pad and gate pad; forming the active layer pattern; patterning the gate insulating film for exposing the pad part; forming the pixel electrode; forming the source and drain electrode; and patterning the passivation film for exposing the pad part. Thus, the conventional process requires an excessive number of fabrication steps which increase cost and further reduce yield.

SUMMARY OF THE INVENTION

In order to solve the aforementioned problems, it is an objective of the present invention to provide a liquid crystal display device and a method of manufacturing the same, in which processing errors can be prevented and the Yield can be increased by etching the gate insulating film after the step of forming the passivation layer.

To accomplish this objective of the present invention, there is provided a liquid crystal display device comprising a substrate; a gate electrode; a gate pad and a source pad formed on the substrate as a first conductive layer; a gate insulating film formed on the entire surface of the substrate; a semiconductor layer and an impurity-doped semiconductor layer formed on the gate insulating film above the gate electrode; a source electrode and a drain electrode formed on the semiconductor layer; a passivation layer formed on the entire surface of the substrate; a first contact hole exposing the source pad; a second contact hole exposing a portion of the drain electrode; a third contact hole exposing the gate pad portion; and a fourth contact hole exposing the source electrode, the contact holes being formed by etching the passivation layer and gate insulating film; a pixel electrode connected with the drain electrode through the second contact hole; and a transparent conductive layer connecting the source pad with the source electrode through the first contact hole and fourth contact hole.

To further accomplish the objective of the present invention, there is also provided a method of manufacturing a liquid crystal display device, comprising the steps of forming a first conductive layer on a substrate; patterning the first conductive layer to respectively form a gate electrode, a gate pad and a source pad; sequentially forming an insulating film, a semiconductor layer and an impurity-doped semiconductor layer on the entire surface of the substrate; patterning the impurity-doped semiconductor layer and semiconductor layer to an active pattern; forming a second conductive layer on the entire surface of the substrate; patterning the second conductive layer to form a

source electrode and a drain electrode; forming a passivation film on the entire surface of the substrate; Selectively etching the passivation film and insulating film to respectively form a first contact hole exposing the source pad, a second contact hole exposing a portion of the drain electrode, a third contact hole exposing a gate pad portion, and a fourth contact hole exposing a portion of the source electrode; forming a transparent conductive layer on the entire surface of the substrate; and patterning a pixel electrode connected with the drain electrode through the second contact hole, a transparent conductive layer connected with the gate pad through the third contact hole, and a transparent conductive layer connecting the source pad with the source electrode through the first and fourth contact holes.

BRIEF DESCRIPTION OF THE ATTACHED DRAWINGS

FIG. 1a to 1f are cross-sectional views illustrating steps of a conventional method for manufacturing a liquid crystal display device;

FIGS. 2a to 2e are cross-sectional views illustrating steps of a method for manufacturing a liquid crystal display according to a preferred embodiment of the present invention;

FIG. 3 is a cross-sectional view illustrating a liquid crystal display device structure according to a second embodiment of the present invention;

FIG. 4 is a circuit diagram of one example of a liquid crystal display device in which a gate material is connected with a source material in accordance with a third embodiment of the present invention; and

FIG. 5 is a vertical-cross-sectional view of the device shown in FIG. 4.

FIG. 6 is a plan view schematic representation of one prior embodiment of a matrix display.

DETAILED DESCRIPTION OF THE INVENTION

Hereinafter, preferred embodiments of the present invention will be described with reference to the attached drawings.

Referring first to FIG. 2a, a conductive layer is formed on a transparent glass substrate 1 and patterned to form a gate electrode 2, a storage capacitor electrode 2D, and a gate pad 2C, all of the same material. The gate electrode is used for applying a voltage in order to drive the active layer in the completed TFT device.

As shown in FIG. 2b, a gate insulating film 3 such as a nitride film or an oxide film is formed on the entire surface of the substrate in order to electrically insulate gate 2. Semiconductor active layer 4 is then formed on insulating gate 2. Active layer 4 is preferably made of amorphous silicon layer deposited by a chemical vapor deposition (CVD) process. Then, in order to reduce the contact resistance between the active layer and the subsequently formed source and drain, an impurity-doped semiconductor layer 5 is formed on amorphous silicon layer 4, as an ohmic contact layer. Impurity-doped semiconductor layer 5 and amorphous silicon layer 4 are etched according to a predetermined active layer pattern.

As shown in FIG. 2c, a conductive layer for forming source electrode 7 and drain electrode 8 is deposited on the substrate by patterning a sputtered layer of conductive material. Using the source and drain electrodes as masks, portions of the impurity-doped semiconductor layer 5 are

exposed and then etched. Source electrode 7 thus forms part of a transistor region and serves as source pad 7A above the gate insulating film so that the same conductive layer constitutes part of the source wiring and the source electrode of the TFT.

As shown in FIG. 2d, a passivation layer 9, e.g., a nitride film, is deposited on the entire surface of the substrate by a CVD process. Then, a predetermined portion of passivation layer 9 and gate insulating film 3 are selectively etched to form first, second and third contact holes 20, 30 and 40, thereby exposing a predetermined region of source pad 7A above gate insulating film 3, a predetermined region of drain electrode 8, and a predetermined region of gate pad 2C. For external electrical connections It is necessary to expose pads 7A and 2C.

As shown in FIG. 2e, an indium tin oxide (ITO) layer is next deposited on the substrate by sputtering or a CVD process and etched according to a predetermined pattern to form a pixel electrode 6. As further shown in FIG. 2e, pixel electrode 6 is connected to the upper portion of drain electrode 8. At the same time, ITO pattern 6B is formed on gate pad 2C. In addition, ITO pattern 6A is provided on source pad 2A, which is part of a data electrode of the LCD. The TFT of the present invention having electrical contacts or wiring structures including gate pad 2C, layer 6B and layer 6A, source pad 7A is thus completed.

As described above, the pixel electrode 6 is formed after the passivation process in the present invention. In contrast, pixel electrode 6 is formed after the pad process or the source/drain formation process in the conventional method. Thus, the passivation layer is interposed between the source/drain formation material and the pixel electrode, thereby effectively isolating these layers and preventing shorts.

Further, unlike the conventional process, the method in accordance with the present invention does not require the step of exposing the pad directly after depositing the gate insulating film, and the source and gate pads are exposed by etching during the passivation process. Thus, the pixel electrode, which is made of ITO, is formed on the source and gate pads. In addition, the source pad is not formed of gate material, but is formed from the source formation material, while the source and drain are deposited. Thus, the problem of high contact resistance between the source pad and the source, caused by forming the source pad from the gate material, can be avoided.

FIG. 3 illustrates a second embodiment of the present invention in which the step of etching the gate insulating layer and the step of etching the passivation layer to expose the pads are preformed in only one mask step. In particular, source pad 2A is composed of gate material, as in the conventional method, and is formed at the same time as gate 2, storage capacitor electrode 2D and gate pad 2B. After forming first, second, third and fourth contact holes 45, 50, 55 and 60, material for forming the pixel electrode is then deposited. As a result, since both the first (45) and fourth (60) contact holes are formed over source pad 2A (formed of the same material as the gate) and source electrode 7, respectively, the source electrode 7 and source pad 2A may be connected to each other in the same step that the pixel electrode is formed. Thus, after patterning, a first transparent conductive layer 6C connects source electrode 7 with source pad 2A, and a second transparent conductive layer 6 (i.e., the pixel electrode) is connected to drain electrode 8.

In other words, a conductive layer is formed on a transparent glass substrate 1 and patterned to form gate 2, a storage capacitor electrode 2D, a source pad 2A and a gate

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pad 2B. After forming a gate insulating film 3 on the entire surface of the substrate, an amorphous silicon layer 4 and an impurity-doped semiconductor layer 5 are sequentially formed thereon. These layers are then etched in accordance with a predetermined active layer pattern.

Then, a conductive layer is formed on the substrate and etched in accordance with a predetermined pattern, thereby forming a source electrode 7 and a drain electrode 8. After forming a passivation layer 9 on the entire surface of the substrate, passivation layer 9 and gate insulating film 3 are selectively etched, thereby forming a first contact hole exposing the source pad 2A and a third contact hole exposing the gate pad 2B. Since the passivation layer 9 and gate insulating film 3 are preferably etched in a single step, the sidewalls of the first and second contact holes are planar and smooth.

ITO is then deposited on the entire surface of the substrate and patterned to form a pixel electrode 6 connected to drain electrode 8 through the contact hole overlying drain electrode 8 in the pixel part. At the same time, ITO patterns 6A, 6B and 6C are formed to contact source pad 2A and gate pad 2B through the contact holes formed at gate insulating film 3 and passivation layer 9.

Further, in accordance with an additional embodiment of the present invention, a repair line or static electricity protection circuit can also be provided during deposition of the pixel electrode layer. FIG.4 is a schematic diagram of static electricity protection circuit 100, and FIG.5 is an enlarged cross-sectional view of a portion 150 of the circuit.

In the circuit shown in FIG.4, if a high potential due to an electrostatic discharge is present on source electrode 7, for example, transistor 170 is rendered conductive to discharge source electrode 7 to gate line 2. Similarly, gate line 2 can discharge to source electrode 7 via transistor 160. As shown in FIG.5, the connection between gate line 2 and source electrode 7 is achieved by forming contact holes in insulative films 3 and 9 and then depositing conductive material (preferably ITO) into these holes while forming the pixel electrode.

According to the present invention as described above, the manufacture of the TFT of the liquid crystal display device can be accomplished using five mask steps (step of forming the gate, step of forming the active layer, step of forming the source and drain, step of etching the passivation layer and gate insulating film, and step of forming the pixel electrode), while the conventional process requires six or more mask steps. Thus, manufacturing cost can be reduced.

Further, when the source pad is formed from the same material as the source electrode, the contact resistance problem caused when the source pad is in contact with the source electrode can be solved. In addition, since the pixel electrode is formed after forming the passivation layer, processing errors resulting in the pixel electrode contacting the source and drain can be prevented.

Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

What is claimed is:

1. A wiring structure comprising:

- a substrate;
- a first conductive layer formed on a first portion of said substrate;
- a first insulative layer formed on a second portion of said substrate and on said first conductive layer;

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a second conductive layer formed on a first portion of said first insulative layer;

a second insulative layer formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer;

an indium tin oxide layer formed on said second insulative layer,

wherein a first contact hole is provided through said first and second insulative layers to expose part of said first conductive layer and a second contact hole is provided through said second insulative layer to expose part of said second conductive layer, said indium tin oxide layer extends through said first and second contact holes to electrically connect said first conductive layer with said second conductive layer, and

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

2. A wiring structure comprising:

- a substrate;
- a first conductive layer formed on a portion of said substrate;
- a first insulative layer having a first via hole exposing a portion of said first conductive layer;
- a second conductive layer formed on a portion of said first insulative layer;
- a second insulative layer having a second via hole exposing said exposed portion of the first conductive layer and having a third via hole exposing a portion of the second conductive layer;
- a third conductive layer formed on said second insulative layer and electrically connecting said first conductive layer to said second conductive layer through said first, second, and third via holes,

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

3. A wiring structure in accordance with claim 2, wherein said third conductive layer includes indium tin oxide.

4. A wiring structure in accordance with claim 2, wherein said first and second via holes constitute a common hole exposing said exposed portion of said first conductive layer, a sidewall of said common hole being substantially smooth.

5. A wiring structure in accordance with claim 2, wherein said second via hole is aligned with said first via hole.

6. A liquid crystal display device comprising:

- a substrate having a primary surface;
- a first conductive layer disposed on a predetermined region of said primary surface;
- a first insulating layer formed overlying said primary surface including said first conductive layer, said first insulating layer including a first contact hole exposing a predetermined portion of said first conductive layer;
- a second conductive layer formed on a predetermined region of said first insulating layer;
- a second insulating layer formed overlying said primary surface including said second conductive layer, said second insulating layer having a second contact hole exposing a predetermined portion of said second conductive layer and said first contact hole region; and
- a third conductive layer formed on said second insulating layer and electrically connected to said first and second conductive layers via said first and second contact holes,

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wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

7. A liquid crystal display device in accordance with claim 6, wherein said third conductive layer includes material 5 suitable for forming a pixel electrode.

8. A method of manufacturing a liquid crystal display device, comprising the steps of:

forming a first conductive layer pattern on a substrate, said first conductive layer pattern being connected to a first terminal of a thin film transistor; 10

forming a first insulating layer overlying a surface of said substrate including said first conductive layer pattern;

forming a second conductive layer pattern on said first insulating layer, said second conductive layer pattern being connected to a second terminal of the thin film transistor; 15

forming a second insulating layer overlying said substrate including said second conductive layer pattern; 20

selectively etching said first and second insulating layers to form a first contact hole and a second contact hole exposing said first conductive layer pattern and said second conductive layer pattern, respectively; and

forming a third conductive layer on said second insulating layer, said third conductive layer electrically connected to said first and second conductive layer patterns via said first and second contact holes, respectively. 25

9. A method of manufacturing a liquid crystal display device in accordance with claim 8, wherein said selective etching step is performed in a single etch step and said third conductive layer includes indium tin oxide. 30

10. A liquid crystal display device comprising:

a substrate;

a first conductive layer on said substrate including: 35
a gate electrode,
a gate pad, and
a source pad;

a gate insulating film on said surface of said substrate, a portion of said gate insulating film overlying said gate electrode; 40

a semiconductor layer on said portion of said gate insulating film;

an impurity-doped semiconductor layer on said semiconductor layer; 45

a source electrode and a drain electrode on said semiconductor layer;

a passivation layer overlying said source pad, said drain electrode, said gate pad, and said source electrode; 50

a first contact hole provided through said passivation layer and said gate insulating film exposing said source pad;

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a second contact hole provided through said passivation layer exposing said drain electrode;

a third contact hole provided through said passivation layer and said gate insulating film exposing said gate pad;

a fourth contact hole provided through said passivation layer exposing said source electrode;

a pixel electrode electrically connected with said drain electrode via said second contact hole; and

a transparent conductive layer electrically connecting said source pad with said source electrode via said first contact hole and said fourth contact hole.

11. A method of manufacturing a liquid crystal display device, comprising the steps of:

forming a first conductive layer on a substrate;

patterning said first conductive layer to form a gate electrode, a gate pad and a source pad;

forming an insulating film on said substrate including said patterned conductive layer;

forming a semiconductor layer on said insulating film;

forming an impurity-doped semiconductor layer on said semiconductor layer;

patterning said impurity-doped semiconductor layer and said semiconductor layer to form an active layer;

forming a second conductive layer overlying said substrate including said active layer; 30

patterning said second conductive layer to form source electrode and a drain electrode on said active layer;

forming a passivation film overlying said substrate including said source pad, a portion of said drain electrode, said gate pad portion, and a portion of said source electrode; 35

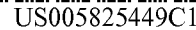
selectively etching said passivation film and said insulating film to form a first contact hole exposing said source pad, a second contact hole exposing said portion of said drain electrode, a third contact hole exposing said gate pad portion, and a fourth contact hole exposing said portion of said source electrode;

patterning a pixel electrode electrically connected to said drain electrode via said second contact hole;

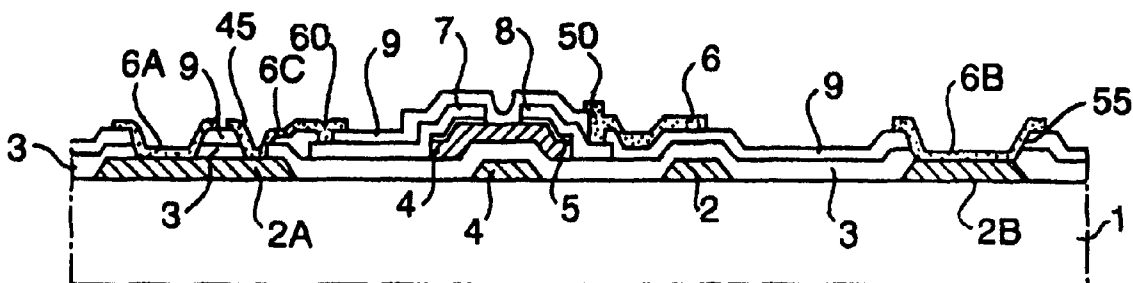
patterning a first transparent conductive layer electrically connected to said gate pad through said third contact hole; and

patterning second transparent conductive layer electrically connecting said source pad to said source electrode via said first and fourth contact holes.

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(10) **Number:** US 5,825,449 C1
(45) **Certificate Issued:** Oct. 20, 2009



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EX PARTE
REEXAMINATION CERTIFICATE
ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS
INDICATED BELOW.

Matter enclosed in heavy brackets [] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claims 10 and 11 is confirmed.

Claims 1, 2, 6, 8 and 9 are determined to be patentable as amended.

Claims 3, 4, 5 and 7, dependent on an amended claim, are determined to be patentable.

New claims 12–21 and 22 are added and determined to be patentable.

1. A wiring structure comprising:

a substrate;

a first conductive layer *including a gate electrode* formed on a first portion of said substrate;

a first insulative layer formed on a second portion of said substrate and on said first conductive layer;

a second conductive layer formed on a first portion of said first insulative layer;

a second insulative layer formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer;

an indium tin oxide layer formed on said second insulative layer,

wherein a first contact hole is provided through said first and second insulative layers to expose part of said first conductive layer and a second contact hole is provided through said second insulative layer to expose part of said second conductive layer, said indium tin oxide layer extends through said first and second contact holes to electrically connect said first conductive layer with said second conductive layer, and

wherein *only* one of said first and second conductive layers is *directly* connected to one of a plurality of terminals of a thin film transistor.

2. A wiring structure comprising:

a substrate;

a first conductive layer *including a gate electrode* formed on a portion of said substrate;

a first insulative layer having a first via hole exposing a portion of said first conductive layer;

a second conductive layer formed on a portion of said first insulative layer;

a second insulative layer having a second via hole exposing said exposed portion of the first conductive layer and having a third via hole exposing a portion of the second conductive layer;

a third conductive layer formed on said second insulative layer and electrically connecting said first conductive

layer to said second conductive layer through said first, second, and third via holes,

wherein *only* one of said first and second conductive layers is *directly* connected to one of a plurality of terminals of a thin film transistor.

6. A liquid crystal display device comprising:

a substrate having a primary surface;

a first conductive layer *including a gate electrode* disposed on a predetermined region of said primary surface;

a first insulating layer formed overlying said primary surface including said first conductive layer, said first insulating layer including a first contact hole exposing a predetermined portion of said first conductive layer;

a second conductive layer formed on a predetermined region of said first insulating layer;

a second insulating layer formed overlying said primary surface including said second conductive layer, said second insulating layer having a second contact hole exposing a predetermined portion of said second conductive layer and said first contact hole region; and

a third conductive layer formed on said second insulating layer and electrically connected to said first and second conductive layers via said first and second contact holes,

wherein *only* one of said first and second conductive layers is *directly* connected to one of a plurality of terminals of a thin film transistor.

8. A method of manufacturing a liquid crystal display device *having an array of pixels*, comprising the steps of:

forming a first conductive layer pattern on a substrate, *said first conductive layer pattern including a gate line and a conductive element*, said first conductive layer pattern *except said conductive element* being connected to a [first] gate terminal of a thin film transistor;

forming a first insulating layer overlying a surface of said substrate including said first conductive layer pattern;

forming a second conductive layer pattern on said first insulating layer, *said second conductive layer pattern including a source wiring, said source wiring of said second conductive layer pattern being connected to a [second] source terminal of the thin film transistor, wherein said conductive element of the first conductive layer pattern is outside said array of pixels*;

forming a second insulating layer overlying said substrate including said second conductive layer pattern;

selectively etching said first and second insulating layers to form a first contact hole and a second contact hole exposing said *conductive element of the first conductive layer pattern* and said second conductive layer pattern, respectively; and

forming a third conductive layer pattern on said second insulating layer, said third conductive layer pattern electrically connected to said *conductive element of the first conductive layer pattern* and said second conductive layer [patterns] pattern via said first and second contact holes, respectively, *wherein said conductive element of the first conductive layer pattern is electrically connected to said second conductive layer pattern through said third conductive layer pattern*.

9. A method of manufacturing a liquid crystal display device in accordance with claim 8, wherein said selective etching step is performed in a single etch step and said third conductive layer pattern includes indium tin oxide.

12. A method of manufacturing a liquid crystal display device in accordance with claim 8, wherein the conductive element is a source pad.

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13. A method of manufacturing a liquid crystal display device in accordance with claim 8, wherein the first conductive layer pattern includes a plurality of conductive elements and the second conductive layer pattern includes a plurality of source wirings, each of said plurality of conductive elements being electrically connected to one of the plurality of source wirings through the third conductive layer pattern.

14. A method of manufacturing a liquid crystal display device in accordance with claim 8, wherein the first conductive layer pattern further includes a gate pad connected to the gate line.

15. A method of manufacturing a liquid crystal display device in accordance with claim 12, wherein the source wiring does not overlap with the source pad.

16. A method of manufacturing a liquid crystal display device in accordance with claim 8, wherein the third conductive layer pattern contacts the first insulating layer, the second insulating layer, the source wiring and the conductive element.

17. A method of manufacturing a liquid crystal display device in accordance with claim 8, wherein the third conduc-

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tive layer pattern contacts at least two different areas of the conductive element.

18. A method of manufacturing a liquid crystal display device in accordance with claim 8, wherein the first insulating layer is directly on the first conductive layer pattern.

19. A method of manufacturing a liquid crystal display device in accordance with claim 8, wherein the second insulating layer is directly on the second conductive layer pattern.

20. A wiring structure according to claim 1, wherein the substrate includes glass and the first conductive layer including the gate electrode is directly on the glass.

21. A wiring structure according to claim 2, wherein the substrate includes glass and the first conductive layer including the gate electrode is directly on the glass.

22. A wiring structure according to claim 6, wherein the substrate includes glass and the first conductive layer including the gate electrode is directly on the glass.

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Claims 1, 2, 6 and 8 are determined to be patentable as amended.

Claims 3-5, 7, 9 and 12-22, dependent on an amended claim, are determined to be patentable.

1. A wiring structure comprising:

a substrate;

a first conductive layer [including] *and a gate electrode on said substrate, the first conductive layer being formed on a first portion of said substrate;*

a first insulative layer formed on a second portion of said substrate and on said first conductive layer;

a second conductive layer formed on a first portion of said first insulative layer;

a second insulative layer formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer;

an indium tin oxide layer formed on said second insulative layer,

wherein a first contact hole is provided through said first and second insulative layers to expose part of said first conductive layer and a second contact hole is provided through said second insulative layer to expose part of said second conductive layer, said indium tin oxide layer extends through said first and second contact holes to electrically connect said first conductive layer with said second conductive layer, and

wherein only one of said first and second conductive layers is directly connected to one of a plurality of terminals of a thin film transistor.

2. A wiring structure comprising:

a substrate;

a first conductive layer [including] *and a gate electrode on the substrate, the first conductive layer being formed on a portion of said substrate;*

a first insulative layer having a first via hole exposing a portion of said first conductive layer;

a second conductive layer formed on a portion of said first insulative layer;

a second insulative layer having a second via hole exposing said exposed portion of the first conductive layer and having a third via hole exposing a portion of the second conductive layer;

a third conductive layer *of a transparent conductive material* formed on said second insulative layer and electrically connecting said first conductive layer to said sec-

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ond conductive layer through said first, second, and third via holes,

wherein only one of said first conductive and second conductive layers is directly connected to one of a plurality of terminals of a thin film transistor.

6. A liquid crystal display device comprising:

a substrate having a primary surface;

a first conductive layer [including] *and a gate electrode on the substrate, the first conductive layer being disposed on a predetermined region of said primary surface;*

a first insulating layer formed overlying said primary surface including said first conductive layer, said first insulating layer including a first contact hole exposing a predetermined portion of said first conductive layer;

a second conductive layer formed on a predetermined region of said first insulating layer;

a second insulating layer formed overlying said primary surface including said second conductive layer, said second insulating layer having a second contact hole exposing a predetermined portion of said second conductive layer and said first contact hole region; and

a third conductive layer *of a transparent conductive material* formed on said second insulating layer and electrically connected to said first *conductive layer* and second conductive [layers] *layer* via said first and second contact holes,

wherein only one of said first conductive and second conductive layers is directly connected to one of a plurality of terminals of a thin film transistor.

8. A method of manufacturing a liquid crystal display device having an array of pixels, comprising the steps of:

forming a first conductive layer pattern on a substrate, said first conductive layer pattern including a gate line and a conductive element, said first conductive layer pattern except said conductive element being connected to a gate terminal of a thin film transistor;

forming a first insulating layer overlying a surface of said substrate including said first conductive layer pattern;

forming a second conductive layer pattern on said first insulating layer, said second conductive layer pattern including a source wiring, said source wiring of said second conductive layer pattern being connected to a source terminal of the thin film transistor, wherein said conductive element of the first conductive layer pattern is outside said array of pixels;

forming a second insulating layer overlying said substrate including said second conductive layer pattern;

selectively etching said first and second insulating layers to form a first contact hole and a second contact hole exposing said conductive element of the first conductive layer pattern and said second conductive layer pattern, respectively; and

forming a third conductive layer pattern *of a transparent conductive material* on said second insulating layer, said third conductive layer pattern electrically connected to said conductive element of the first conductive layer pattern and said second conductive layer pattern via said first and second contact holes, respectively, wherein said conductive element of the first conductive layer pattern is electrically connected to said second conductive layer pattern through said third conductive layer pattern.

* * * * *