IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

Valtrus Innovations Ltd. and Key Patent Innovations Ltd.,	§	
Plaintiffs	§	
v.	§	**CIVIL ACTION NO. 2:24-CV-00021-JRG**
SAP America, Inc. and SAP, SE.	§	**JURY TRIAL DEMANDED**
Defendants.	§	

JOINT CLAIM CONSTRUCTION CHART

Pursuant to P.R. 4-5(d) of the Rules of Practice for Patent Cases before the United States District Court for the Eastern District of Texas, and the Court's Second Amended Docket Control Order (Dkt. No. 109), Plaintiffs Valtrus Innovations Ltd. and Key Patent Innovations Ltd. (collectively, "Plaintiffs") and Defendants SAP America, Inc. and SAP, SE (collectively, "Defendants") hereby submit Appendix A (Claim Terms and Constructions) and Appendix B (List of Complete Language of Disputed Claims).

The patents asserted in this case are U.S. Patent No. 6,823,409 ("the '409 Patent"), U.S. Patent No. 6,871,264 ("the '264 Patent"), U.S. Patent No. 6,889,244 ("the '244 Patent"), U.S. Patent No. 7,313,575 ("the '575 Patent"), U.S. Patent No. 6,691,139 ("the '139 Patent"), U.S. Patent No. 7,936,738 ("the '738 Patent"), and U.S. Patent No. 7,152,182 ("the '182 Patent").

Date: February 28, 2025

By: */s/ Matthew G. Berkowitz by permission Andrea L. Fair*

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system pursuant to Local Rule CV-5(a)(3) on February 28, 2025

/s/ Andrea L. Fair
Andrea L. Fair

Term	Asserted Patents, Claims	Plaintiffs' Proposed Construction	Defendants' Proposed Construction	Court's Construction
as set for the in	'409 Patent, claim 9	**[AGREED]**[1]	**[AGREED]**	as set forth in
a plurality of cache memory blocks, allocable cache memory block, allocable upper level cache memory blocks	'264 Patent, claims 1, 3, 5, 9	**[AGREED]**	**[AGREED]**	Plain and ordinary meaning, where the blocks are composed of memory cache rather than disk cache
non-allocable cache memory blocks	'264 Patent, claims 8	**[AGREED]**	**[AGREED]**	Plain and ordinary meaning, where the blocks are composed of memory cache rather than disk cache
transmitting the send message to from the FTSS to a service on the second node	'244 Patent, claim 4	**[AGREED]**	**[AGREED]**	transmitting the send message [] from the FTSS to a service on the second node
Claim 1 Preamble	'139 Patent, claim 1	**[AGREED]**	**[AGREED]**	Limiting
Claim 5 Preamble	'139 Patent, claim 5	**[AGREED]**	**[AGREED]**	Limiting
Claim 12 Preamble	'738 Patent, claim 12	**[AGREED]**	**[AGREED]**	Limiting
wherein the outgoing message is sent from the node is to a remote node across a network	'738 Patent, claim 3	**[AGREED]**	**[AGREED]**	wherein the outgoing message [] sent from the node is to a remote node across a network
Claim 1 Preamble	'738 Patent, claim 1	**[AGREED]**	**[AGREED]**	Limiting

[1] The parties identified this term as agreed after submitting the Joint Claim Construction and Prehearing Statement.

Term	Asserted Patents, Claims	Plaintiffs' Proposed Construction	Defendants' Proposed Construction	Court's Construction
Claim 33 Preamble	'738 Patent, claim 33	**[AGREED]**	**[AGREED]**	Limiting
"assembler" and "disassembler"	'575 Patent, claims 1, 4, 36	**[AGREED]**[2]	**[AGREED]**	Plain and ordinary meaning.
the RTID that … create at least one assembler defined according to the polymorphic metadata …	'575 Patent, claims 28	**[AGREED]** [3]	**[AGREED]**	the RTID that … create[s] at least one assembler defined according to the polymorphic metadata …
context information	'738 Patent, claims 1, 2, 5, 6, 10, 33	**[AGREED]**[4]	**[AGREED]**	Plain and ordinary meaning.
coherency control module	'409 Patent, claims 1, 4	Plain and ordinary meaning. Not indefinite.	Indefinite	
request module	'409 Patent, claims 1, 7	Plain and ordinary meaning. Not indefinite.	Indefinite	
static RAM interface module	'409 Patent, claims 1, 7, 9	Plain and ordinary meaning. Not indefinite.	Indefinite	
high-speed interconnect coupling	'264 Patent, claim 1	Plain and ordinary meaning. Not indefinite.	Indefinite	
accessing determining which nodes should receive the broadcast message based on the broadcast message	'244 Patent, claim 10	[] determining which nodes should receive the broadcast message based on the broadcast message	Indefinite	

[2] This term was originally disputed but the parties are now in agreement.
[3] This term was originally disputed but the parties are now in agreement.
[4] This term was originally disputed but the parties are now in agreement.

Term	Asserted Patents, Claims	Plaintiffs' Proposed Construction	Defendants' Proposed Construction	Court's Construction
the first and second nodes are each coupled to a fault tolerant storage system (FTSS)	'244 Patent, claim 1, preamble	Plain and ordinary meaning. Not indefinite.	Plain and ordinary meaning, where the coupling to the FTSS provides for transmitting messages by a store-and-forward method (i.e., not through a conventional computer network such as a local area network (Ethernet) or wide area network (Internet))	
highly reliable fault-tolerant storage media	'244 Patent, claims 1, 2, 3, 6, 9, 10	Plain and ordinary meaning. Not indefinite.	Indefinite	
polymorphic metadata	'575 Patent, claims 1, 4, 28[5]	Plain and ordinary meaning. Not indefinite.	Indefinite	
potentially inaccurate or incomplete	'738 Patent, claim 10	Plain and ordinary meaning. Not indefinite.	Indefinite	

[5] Valtrus's opening claim construction brief inadvertently listed claim 33 as including the disputed term, and SAP's response brief inadvertently excluded claim 28.

Valtrus Innovations Ltd., et. al. v. SAP Am., Inc., et. al., Civil Action No. 2:24-cv-00021-JRG (E.D. Tex.)

I. <u>'409 Patent (Claims 1, 4, 7, 9)</u>

Claim 1. A computer system comprising:

a host controller;

a first processor bus coupled between the host controller and a first processor;

a second processor bus coupled between the host controller and a second processor;

a random access memory (RAM) coupled to the host controller via a memory bus, the RAM comprising a portion of static memory and a portion of dynamic memory; and

a **coherency control module** operably coupled to the first processor bus and the second processor bus and comprising:

a **request module** configured to receive requests from the first processor bus and the second processor bus and to maintain proper ordering of the requests from each processor bus;

an active snoop queue (ASQ) module coupled to the **request module** and configured to maintain a list of requests currently being processed and to prevent simultaneous multiple accesses to a single address in the static portion of the RAM; and

a **static RAM interface module** configured to access an address look-up table corresponding to data stored in the static portion of the RAM.

Claim 4. The computer system, as set forth in claim 1, wherein the **coherency control module** comprises a plurality of list structures corresponding to the first processor bus and the second processor bus.

Claim 7. The computer system, as set forth in claim 4, wherein the **request module** comprises a plurality of bypass paths configured to provide a direct request path from the first and second processor buses to the **static RAM interface module**, thereby bypassing the list structures.

Claim 9. The computer system, as set for the in claim 1, wherein the **static RAM interface module** comprises a plurality of static RAM interfaces, each static RAM interface corresponding to a segment of the static portion of the RAM.

II. <u>'264 Patent (Claim 1)</u>

Claim 1. A processor integrated circuit capable of executing more than one instruction stream comprising:

a first processor, coupled to fetch instructions and access data through a first cache controller;

a second processor, coupled to fetch instructions and access data through a second cache controller;

a plurality of cache memory blocks;

a **high-speed interconnect coupling** the plurality of cache memory blocks to the first and second cache controllers such that at least one allocable cache memory block is capable of being used by the first and second cache controllers; and

a resource allocation controller coupled to determine an accessing cache memory controller selected from the group consisting of the first and second cache memory controllers, whereby the accessing cache memory controller is allowed to access the allocable cache memory block,

wherein the cache memory blocks are usable by the cache controllers to store data and instructions fetched from a random-access memory.

III. <u>'244 Patent (Claims 1, 2, 3, 6, 9, 10)</u>

Claim 1. A method of transmitting messages between a first node and a second node, wherein **the first and second nodes are each coupled to a fault tolerant storage system (FTSS)**, the method comprising:

transmitting a message from the first node to a communication agent in the FTSS;

storing the message in a data structure in **highly reliable fault-tolerant storage media** of the FTSS;

processing the message at the FTSS in accordance with a messaging paradigm; and

transmitting the message from the FTSS to the second node.

Claim 2. The method of claim 1 wherein the messaging paradigm is a request/reply communication paradigm, and:

transmitting a message from the first node to a communication agent in the FTSS comprises:

transmitting a request message from the first node to a request/reply communication agent in the FTSS;

storing the message in a data structure in **highly reliable fault-tolerant storage media** of the FTSS comprises:

storing the request message in a request queue in **highly reliable fault-tolerant storage media** of the FTSS;

processing the message at the FTSS in accordance with a messaging paradigm comprises:

retrieving the request message from the request queue; and

transmitting the message from the FTSS to the second node comprises:

transmitting the request message from the FTSS to a service on the second node;

and the method further comprises:

executing the service on the second node using the request message as an input

and providing a reply message as an output; transmitting the reply message from the second node to the request/reply communication agent in the FTSS;

storing the reply message in a reply queue in **highly reliable fault-tolerant storage media** of the FTSS;

retrieving the reply message from the reply queue; and

transmitting the reply message from the FTSS to the first node.

Claim 3. The method of claim 1 wherein the messaging paradigm is a conversational communication paradigm, and:

transmitting a message from the first node to a communication agent in the FTSS comprises:

transmitting a connect message from the first node to a conversational communication agent in the FTSS;

processing the message at the FTSS in accordance with a messaging paradigm comprises:

opening a conversation queue in highly reliable fault-tolerant storage media of the FTSS;

storing the message in a data structure in **highly reliable fault-tolerant storage media** of the FTSS comprises:

storing the connect message in the conversation queue; and

transmitting the message from the FTSS to the second node comprises:

transmitting the connect message from the FTSS to the second node.

Claim 6. The method of claim 1 wherein the messaging paradigm is an event-based communication paradigm, and:

transmitting a message from the first node to a communication agent in the FTSS comprises:

transmitting a post message from the first node to an event-based communication agent in the FTSS;

processing the message at the FTSS in accordance with a messaging paradigm comprises:

accessing a subscription manager to determine whether any nodes have subscribed to receive the event represented by the post message;

storing the message in a data structure in **highly reliable fault-tolerant storage media** of the FTSS comprises:

storing the post message in an event queue in **highly reliable fault-tolerant storage media** of the FTSS; and

transmitting the message from the FTSS to the second node comprises:

transmitting the post message from the FTSS to the second node if the second node has subscribed to receive the event represented by the post message.

Claim 9. The method of claim 1 wherein the messaging paradigm is a queue-based communication paradigm, and:

transmitting a message from the first node to a communication agent in the FTSS comprises:

transmitting an enqueue message from the first node to a queue-based communication agent in the FTSS;

storing the message in a data structure in **highly reliable fault-tolerant storage media** of the FTSS comprises:

storing the enqueue message in a queue space in **highly reliable fault tolerant storage media** of the FTSS;

processing the message at the FTSS in accordance with a messaging paradigm comprises:

retrieving the enqueue message from the queue space only if the second node is available; and

transmitting the message from the FTSS to the second node comprises:

transmitting the enqueue message from the FTSS to a service on the second node only if the second node is available;

and the method further comprises:

executing the service on the second node using the enqueue message as an input and providing a dequeue message as an output; transmitting the dequeue message from the second node to the queue-based communication agent in the FTSS;

storing the dequeue message in the queue space;

retrieving the dequeue message from the queue space; and

transmitting the dequeue message from the FTSS to the first node.

Claim 10. The method of claim 1 wherein the messaging paradigm is an unsolicited communication paradigm, and:

transmitting a message from the first node to a communication agent in the FTSS comprises:

transmitting a broadcast message from the first node to an unsolicited communication agent in the FTSS;

processing the message at the FTSS in accordance with a messaging paradigm comprises:

accessing determining which nodes should receive the broadcast message based on the broadcast message;

storing the message in a data structure in **highly reliable fault-tolerant storage media** of the FTSS comprises:

storing the broadcast message in an unsolicited message queue in **highly reliable fault-tolerant storage media** of the FTSS; and

transmitting the message from the FTSS to the second node comprises:

transmitting the post message from the FTSS to all nodes that should receive the broadcast message.

IV. <u>'575 Patent (Claims 1, 4, 28)</u>

Claim 1. A data services handler for execution on a computing system comprising:

an interface executing on the computing system for communicating between a data store and applications that supply and consume data; and

a real time information director (RTID) executing on the computing system that transforms data for supply, consumption, or both by the applications under direction of **polymorphic metadata** that defines a security model and data integrity rules for application to the data, the RTID to dynamically instantiate, create, and cache for reuse disassemblers and assemblers according to demand, the RTID further comprising:

at least one disassembler defined according to the **polymorphic metadata** that disassembles inbound data documents into multiple records in preparation for insertion into metadata tables; and

at least one assembler defined according to the **polymorphic metadata** that assembles outbound data documents from at least one record selected from at least one metadata-selected table whereby data is transformed for supply, consumption or both.

Claim 4. The data services handler according to claim 1 wherein the real time information director further comprises:

the RTID using a same descriptive **polymorphic metadata** to build both assemblers and disassemblers for a same document class.

Claim 28. An enterprise system comprising:

a plurality of interlinked computer servers and networks enabling multiple users to access applications and data on the servers; and

a real time information director (RTID) executing on at least one of the interlinked servers that manages information flow between a data store and applications that supply and consume data and dynamically instantiates, creates, and caches for reuse disassemblers and assemblers according to demand,

the RTID that creates at least one disassembler defined according to the **polymorphic metadata** that disassembles inbound data documents into multiple records in preparation for insertion into metadata tables and create at least one assembler defined according to **the polymorphic metadata** that assembles outbound data documents from at least one record selected from at least one metadata-selected table whereby data is transformed for supply, consumption, or both.

V. <u>'738 Patent (Claim 10)</u>

Claim 10. The method of claim 1, further comprising adding, to the message, an indication associated with the obtained context information where it is determined that the obtained context information is **potentially inaccurate or incomplete**.