BRUCE L. JACOB
Cyber Science Department
United States Naval Academy

Fall/Winter 2024

FIELDS
Hardware-Based Security *(Side-Channel Analysis, Robust Computer Architectures & Operating Systems)*
Memory Systems *(Caches, DRAM, Flash & Other Non-Volatile Technologies — from Devices to Systems)*
Technology Innovation *(Start-Up Companies, Entrepreneurship, High Tech, Electric Guitars)*

In 2022, Bruce Jacob joined the U.S. Naval Academy's Department of Cyber Science, where he studies the intersection between hardware and security, including the following:

- the security and protection of memory devices and memory systems
- side-channel exploits and their mitigation
- the development of robust computer architectures and operating systems, a pursuit that combines his knowledge of memory systems and operating systems with methodologies derived from the side-channel experiments

He continues to do research in the design of novel memory architectures and systems that exploit them.

In 2020, Jacob was named a Fellow of the IEEE "for contributions to computer memory design and analysis." He has designed computer-system architectures and computer memory-system architectures for both industry and government, national and international, focusing on highly efficient designs at the High-Performance Computing level, as well as at the high-performance embedded-systems level. For instance, he helped Micron design their new *Hybrid Memory Cube* DRAM architecture, he redesigned Cray's memory controller for their *Black Widow* memory system, he helped Northrop Grumman design a system interconnect for their experimental ultra-low-power datacenter, he designed a high-performance memory system for the 1024-core *Teraflux* chip funded by the European Commission, he has collaborated with researchers at the Department of Energy on the design of their next-generation supercomputers, and with collaborators at the University of Maryland, he currently works on the design of monolithic computer systems that integrate high-capacity restive RAMs directly into CMOS logic chips for high-performance, low power, single-chip systems.

Recognized internationally as a leading expert on computer memory systems, Jacob founded the annual *International Symposium on Memory Systems* and is regularly invited to give keynote speeches and high-level briefings on the topic of memory systems around the world. He has been the keynote speaker at meetings including EMS, MCC, MCHPC, ModSim, SAMOS, Multicore World, and Computing Frontiers. In 2007, he was one of fifteen members of academia and industry invited to brief a National Academies panel on the then-current state of computing, resulting in the highly-cited NRC exascale report *The Future of Computing Performance — Game Over or Next Level?* In 2012, he was one of twenty members of academia and industry asked to brief the Secretary of Energy, Steven Chu, on the state of computing relative to the Department of Energy's plans to achieve exascale-class computer performance. In 2016, he was one of a dozen members of academia and industry invited to participate with DOE in creating a roadmap for computer science and applied mathematics research at DOE in the coming decades. In 2020, he was one of four members of academia and two dozen members of industry and national labs invited to work with Semiconductor Research Corp., Semiconductor Industry Assoc., and DOE to develop a roadmap for memory devices and systems in the coming decade.

In addition to his academic credentials, Jacob has significant industry experience. Between college and graduate school, he worked in the start-up industry in Boston for two different telecommunications companies, serving as a software engineer at Boston Technology and then as the chief engineer and system architect at Priority Call Management. Both of these start-up companies were successful — in particular, Priority Call Management, for which Jacob designed and developed the product's system-level architecture, its distributed middleware code, and its object-oriented applications framework, was purchased for $162M in the late 1990s.

Jacob has written two textbooks on computer memory systems and over one hundred articles covering memory systems, computer design, embedded systems, operating system design, astrophysics, and algorithmic composition. He holds two patents in memory-systems design and three patents in the circuit design of electric guitars. In 2009, the electric guitars were featured on Washington DC local television and radio stations; in articles appearing in *The Washington Post*, *Los Angeles Times*, and *The Chronicle of Higher Education*; and on National Public Radio (Jacob and his graduate student were interviewed by Robert Siegel on *All Things Considered* on July 10, 2009).

I. EDUCATION AND EMPLOYMENT

A. EDUCATION

1997 *Ph.D.* **Computer Science & Engineering** **University of Michigan–Ann Arbor**
Dissertation: *Software-Oriented Memory-Management Design*
Results published in *HPCA 1997*; *IEEE Computer,* June 1998; *IEEE Micro,* July/August 1998

1995 *M.S.* **Computer Science & Engineering** **University of Michigan–Ann Arbor**
Thesis: *Optimization of Storage Hierarchies*
Results published in *IEEE Transactions on Computers*, October 1996

1988 *A.B.* **Mathematics** *(cum laude)* **Harvard University**
Senior Project: *A Radio Study of the Galactic Center*
Results published in *Interstellar Matter*, Gordon & Breach NY, 1987
Starting PK on 1987 Ivy League Championship football team (yes, I have a ring)

B. PROFESSIONAL EXPERIENCE

2022–present **Professor**, Department of Cyber Science, United States Naval Academy, Annapolis MD

2021–2022 **Professor/Chair**, Department of Electrical & Computer Engineering, Florida Polytechnic University

2020 Named **Fellow**, *Institute of Electrical and Electronics Engineers (IEEE)*

The IEEE Board of Directors, at its November 2020 meeting, elevated Jacob to IEEE Fellow, effective as of 1 January 2021, with the following citation:

for contributions to computer memory design and analysis

2015 **Founder**, International Symposium on Memory Systems *(published by ACM)*

First meeting held October 2015; every year sees over 100 attendees, ~30% international, who come for a 3-day technical meeting that has now become the world's preeminent forum for research in memory systems

2014 **Visiting Professor**, Foundation for Research & Technology – Hellas (FORTH), Heraklion Greece

Two-month research collaboration on EC-sponsored datacenter project ***EuroServer****, designing nonvolatile main memories for improved system-level power dissipation*

2014 **Visiting Professor**, University of Cyprus, Nicosia Cyprus

One-month research collaboration on EC-sponsored supercomputer project ***Teraflux****, studying dataflow issues within single-chip multiprocessors*

2012–2013 **Visiting Professor**, University of Siena, Siena Italy

Fourteen-month research collaboration on EC-sponsored supercomputer project ***Teraflux****, designing a memory system for their 1024-core CPU chip*

2011–2021 **Professor (Full)**, Department of Electrical & Computer Engineering, University of Maryland, College Park MD

Helped design Micron's ***Hybrid Memory Cube*** *(revolutionary DRAM architecture announced in 2012); designed a system interconnect for Northrop Grumman's experimental ultra-low-power datacenter*

2007–2010 **Director of Computer Engineering**, Department of Electrical & Computer Engineering, University of Maryland, College Park MD

Updated the curriculum of the undergraduate degree program and increased the program's visibility and enrollment (applications were up 25% the year after changes were made)

2006–2010 **Founder**, Coil Guitars, College Park MD

Patented three circuit-design technologies and served as public relations emissary for the University of Maryland; featured in ***The Washington Post****,* ***Los Angeles Times****, and on* ***National Public Radio***

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2006	Named **Keystone Professor**, University of Maryland's Clark School of Engineering
	Honorific for teaching excellence; helped to redesign the Clark School's introductory engineering class to become more interdisciplinary and to use more relevant projects
2003–2011	**Associate Professor**, Department of Electrical & Computer Engineering, University of Maryland, College Park MD
	Redesigned Cray's memory controller, significantly improving their system's sustained memory bandwidth; wrote and published Memory Systems: Cache, DRAM, Disk (1000-page reference work)
1997–2003	**Assistant Professor**, Department of Electrical & Computer Engineering, University of Maryland, College Park MD
	*Received National Science Foundation **CAREER Award** for work on DRAM devices and architectures*
1992–1997	**Graduate Student Research Assistant**, University of Michigan, Ann Arbor MI
	Designed the memory-management architecture for the PUMA processor
1991–1992	**System Architect/Chief Engineer**, Priority Call Management, Wilmington MA
	Employee #2; designed the company's real-time distributed telecommunications system; developed the first system prototype used to attract seed funding; designed, developed, and installed into the Dallas Convention Center the company's first real product
1989–1991	**Software Engineer**, Boston Technology, Cambridge MA
	Developed real-time telecommunications applications
1988–1989	**Mathematics Teacher**, Thayer Academy, Braintree MA

II. RESEARCH, SCHOLARLY, AND CREATIVE ACTIVITIES

A. Contracts and Grants

Department of Defense
RRAM Architecture Exploration; 9/2023–8/2028; $6,700,000. US Naval Academy as subcontractor to University of Maryland with Yeung (PI) and Peckerar.

Army Research Office & Intelligence Advanced Research Projects Activity
AGILE Honeycomb; 6/2024–. Consultant for Qualcomm (PI) and Extreme Scale Solutions.

Office of Naval Research
Investigating "Complex" Instruction-Set Design and Multicore Processors for Improved Computer Security; Summer 2023; $46,000. PI.

Department of Defense
E-VERIFY: ReRAM Architecture Exploration; 8/2022–2/2024; $420,000. Co-PI, with Yeung (PI) and Peckerar.

Department of Defense
E-VERIFY: Advanced Memory Modeling, Simulation, and Architectural Studies — Task 8; 8/2022–12/2025; $400,000. PI.

Department of Defense
E-VERIFY: High Bandwidth Memory System Development; 8/2021–8/2022; $420,000. Co-PI, with Yeung (PI).

Department of Defense
E-VERIFY: Advanced Memory Modeling, Simulation, and Architectural Studies — Task 8; 8/2021–8/2022; $210,000. PI.

Department of Defense
E-VERIFY: High Bandwidth Memory System Development; 5/2020–5/2021; $270,000. Co-PI, with Yeung (PI).

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Department of Defense
E-VERIFY: High Bandwidth Memory Model/Simulation Development; 5/2020–5/2021; $175,000. PI.

Semiconductor Research Corporation
Monolithic Integration of CPU and Main Memory Systems; 1/2020–12/2022; $270,000. Co-PI, with Yeung (PI).

Department of Defense
Memory Modeling and Simulation; 5/2019–5/2020; $300,000. PI.

Department of Defense
Emerging Memory Technologies; 5/2019–5/2020; $200,000. Co-PI, with Yeung (PI).

Department of Defense
Memory Modeling: Infrastructure Extension and RRAM Plug-In; 5/2018–5/2019; $175,000. PI.

Department of Defense
Using RRAM to Build CPUs with On-Chip Memory Systems; 5/2018–5/2019; $275,000. Co-PI, with Yeung (PI).

Department of Defense
High Bandwidth Memory Modeling and Simulation; 2/2018–2/2020; $500,000. PI.

National Science Foundation
3DSIM: A Unified Framework for 3D CPU Co-Simulation; 9/2016–9/2019; $500,000. Co-PI, with Srivastava (PI).

Northrop Grumman Corporation
Memory-System Design for Cold Logic Program; 9/2015–12/2015; $625,000. PI.

Department of Energy Office of Science
Data Movement Dominates II: Advanced Memory Technology to Address the Real Exascale Power Problem (Extension); 10/2013–9/2015; $5,100,000. Co-PI, with investigators at Sandia National Laboratories (Lead Institution), Lawrence Berkeley National Laboratory, Micron Technology, and Columbia University.

Sandia National Laboratories
E-VERIFY: High Performance Memory Systems Design and Optimization; 2/2012–2/2013; $150,000. PI.

Defense Advanced Research Projects Agency
X-caliber Ubiquitous High Performance Computing (UHPC) Proposal; 10/2010–9/2014; $25,800,000. Academic Subcontractor, on team including Sandia National Laboratories (Lead Institution), FTL Systems, Micron Technologies, LexisNexis Special Services, Indiana Integrated Circuits LLC, Georgia Institute of Technology, Louisiana State University, North Carolina State University, Stanford University, University of Illinois, University of Notre Dame, and University of Southern California.

Department of Energy Office of Science
Data Movement Dominates: Advanced Memory Technology to Address the Real Exascale Power Problem; 10/2010–9/2013; $5,100,000. Co-PI, with investigators at Sandia National Laboratories (Lead Institution), Lawrence Berkeley National Laboratory, Micron Technology, and Columbia University.

Intel Corporation
Novel Applications of Persistent Memory; 10/2010–9/2013; $440,000. PI.

Sandia National Laboratories
Non-Volatile Memory Systems; 10/2010– 9/2013; $200,000. PI.

Maryland Industrial Partnerships
Novel Signal-Processing Prototypes II; 1/2010–12/2010; $135,000. PI.

Intel Corporation
Memory Hierarchy Architecture Research; 11/2009 [Foundation gift]; $120,000. PI.

Cypress Semiconductor Corporation
Memory-System Modeling; 11/2009–7/2010; $200,000. PI.

Maryland Industrial Partnerships
Novel Signal-Processing Prototypes; 1/2009–12/2009; $135,000. PI.

Department of Defense
Next-Generation DRAM-System Architectures and Optimizations; 11/2008–10/2013; $500,000. PI.

Note: *this contract covered the collaborative design and development of Micron's Hybrid Memory Cube DRAM architecture ("HMC"), announced as a commercial product in 2012.*

Sandia National Laboratories
High Performance Memory-Systems Design and Optimization; 6/2008–12/2010; $255,000. PI.

National Institute of Standards and Technology
Integration Methodologies and Full System Verification for Heterogeneous Systems on Chip; 1/2007–1/2009; $150,000. PI.

Office of the Secretary of Defense
Focused Logistics Transformation and Sense & Respond Support; 9/2005–12/2007; $120,000 (my portion). Associated Researcher, on team including investigators from the School of Public Policy (Lead Institution); the College of Computer, Mathematical, and Natural Sciences; and the College of Engineering.

National Science Foundation, MRI Award
MRI: Development of Energy-Efficient Embedded Systems for Wireless Sensor Networks; 8/2005–7/2008; $400,000. Co-PI, with Ephremides (PI), Abshire, Barua, Petrov, Qu, Ulukus, and Vishkin. Equipment grant.

Cray Computer Corporation
High-Bandwidth Controller and System Design; 5/2005–11/2005; $60,000. PI.

IBM Corporation, SUR Award
DRAM Device Configuration and Performance Scalability; 2/2005; $25,000 in equipment. PI.

National Institute of Standards and Technology
System-on-Chip Integration of Microcontroller with Gas Sensor VC; 1/2005–1/2007; $140,000. PI.

Cray Computer Corporation
DDR3 Memory-System Configuration Sensitivity; 4/2004–9/2004; $50,000. PI.

National Institute of Standards and Technology
Embedded Sensor System-on-Chip Microcontroller Core and System Architecture Design; 8/2003–5/2004; $30,000. PI.

National Science Foundation, ITR Award
ITR: Parallel Random-Access Model (PRAM)-On-Chip; 9/2003–9/2008; $750,000. Co-PI, with Vishkin (PI), Barua, Franklin, and Qu.

Department of Defense — Maryland Procurement Office
Joint Program for Advanced Electronic Materials; 6/2003–5/2006; $2,400,000. Associated Researcher, with Lee (PI), Goldsman, and Yang.

Air Force Office of Scientific Research, MURI Award
Basic Studies of the Effect of Microwave Pulses on Electronics; 5/2001–4/2006; $3,300,000. Co-PI, with Granatstein (PI), Anlage, Antonsen, Baker, Carmel, Goldsman, Iliadis, Melngailis, O'Shea, Ott, Ramahi, and Rodgers.

National Science Foundation
Hardware-Software Co-Design of Real-Time Operating Systems and Embedded Microprocessors; 3/2001–3/2005; $1,400,000. PI, with Stewart (subcontractor).

National Science Foundation, CAREER Award
Architecture Issues in DRAM Devices and Systems; 1/2000–1/2004; $230,000. PI.

Compaq Computer Corporation
Evaluation of EV6 with Contemporary DRAM Architectures; 8/1999; $40,000 in equipment. PI.

IBM Corporation
The Study of Design Parameters for DDR DRAM and DDRII DRAM; 11/1999–1/2003; joint study agreement with access to IBM proprietary mainframe memory traces. PI.

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National Science Foundation
Hardware-Software Co-Design of an Experimental Real-Time Operating System and a Microcontroller Architecture; 9/1998–9/2000; $280,000. Co-PI, with Stewart (PI).

UNIVERSITY OF MARYLAND INTERNAL

UMD Minta Martin Aeronautical Research Fund
Microarchitecture Support for Real-Time Embedded Systems; 5/1998–10/1999; $35,000.

UMD General Research Board Summer Research
A Better Simulation Environment for Computer Architecture; 6/1998–9/1998; $6,000.

Note: *In the following sections on publications, lead author is first; student advisees are in* ***bold****; number of citations is given only for works whose citation count is notable (e.g., double digits). Citation counts come from Google Scholar and include self-citations.*

Total number of citations > 8500; ***mean citations*** *per work ~85;* ***i1000-index*** *of citations = 2 (works with 1000+ citations);* ***i100-index*** *of citations = 25 (works with 100+ citations);* ***i10-index*** *of citations = 70 (works with 10+ citations)*

B. BOOKS

B. Jacob, W. Casey, and A. Melaragno. Cybersecurity Architecture: The Design and Security of Modern Computing Systems. Springer/Nature, forthcoming 2025.

B. Jacob, with contributions by **S. Srinivasan** and **D. T. Wang**. The Memory System (You Can't Avoid It; You Can't Ignore It; You Can't Fake It). ISBN 978-1598295870. Morgan & Claypool Publishers: San Rafael CA, 2009.

Citations: 100

B. Jacob, S. Ng, and **D. Wang**, with contributions by **S. Rodriguez**. Memory Systems: Cache, DRAM, Disk. ISBN 978-0123797513. Morgan Kaufmann: San Francisco CA, 2007.

Citations: 1,209

➡ ~500,000 words, 950 pages. An authored work, not an edited work.

C. REFEREED WORK (JOURNAL ARTICLES AND CONFERENCE PAPERS)

J. E. Hill, T. O. Walker, J. A. Blanco, R. W. Ives, R. Rakvic and B. Jacob, "Ransomware classification using hardware performance counters on a non-virtualized system." *IEEE Access*, vol. 12, pp. 63865–63884, April 2024.

B. Jacob and T. Mudge. "RETROSPECTIVE: A performance comparison of contemporary DRAM architectures (ISCA 1999)." In *ISCA@50 25-Year Retrospective: 1996–2020*, J. F. Martínez and L. K. John, Eds. ACM SIGARCH and IEEE TCCA, June 2023.

➡ Invited retrospective on our 1999 memory-systems paper selected for inclusion in *ISCA@50 25-Year Retrospective: 1996–2020*. The paper was one of 98 chosen to represent the computer architecture field on the 50-year anniversary of the conference.

B. Jacob. "Thoughts on merging the file system and virtual memory system — Design decisions and their ramifications in developing the Osprey kernel." In *Proc. ACM/IEEE International Symposium on Memory Systems (MEMSYS 2023)*, pp. 173–179. Washington DC, October 2023.

M. Peckerar, P.-C. Huang, R. A. Jamil, B. Jacob, and D. Yeung. "Critical issues in advanced ReRAM development." In *Proc. ACM/IEEE International Symposium on Memory Systems (MEMSYS 2023)*, p. 285. Washington DC, October 2023.

L. Kang, Y. Xue, W. Jia, X. Wang, J. Kim, C. Youn, M. Kang, H. Lim, B. Jacob, J. Huang. "IceClave: A trusted execution environment for in-storage computing." In *Proc. 54th International Symposium on Microarchitecture (MICRO 2021),* pp. 199–211. Athens Greece, October 2021.

Citations: 28

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L. Kang and B. Jacob. "Zoned FTL: Achieve resource isolation via hardware virtualization." In *Proc. ACM/IEEE International Symposium on Memory Systems (MEMSYS 2021)*, pp. 1–8. Washington DC, October 2021.

C. Walden, D. Singh, **M. Jagasivamani**, **S. Li**, **L. Kang**, M. Asnaashari, S. Dubois, B. Jacob, and D. Yeung. "Monolithically integrating non-volatile main memory over the last-level cache." *ACM Transactions on Architecture and Code Optimization*, vol. 18, no. 4, article 48. July 2021.

M. Jagasivamani, C. Walden, D. Singh, **L. Kang**, M. Asnaashari, S. Dubois, B. Jacob, D. Yeung. "Tileable monolithic ReRAM memory design," In *Proc. IEEE Symposium in Low-Power and High-Speed Chips (COOL CHIPS 2020)*, pp. 1–3. Kokubunji Japan, April 2020.

S. Li, Z. Yang, **D. Reddy**, A. Srivastava, B. Jacob. "DRAMsim3: A cycle-accurate, thermal-capable DRAM simulator." *IEEE Computer Architecture Letters*, vol. 19 , no. 2 , pp. 106–109. July–December 2020. Published on-line February 2020.

Citations: 168

M. Jagasivamani, C. Walden, D. Singh, **L. Kang**, **S. Li**, M. Asnaashari, S. Dubois, D. Yeung, and B. Jacob. "Analyzing the monolithic integration of a ReRAM-based main memory into a CPU's die." *IEEE Micro*, vol. 39, no. 6, pp. 64–72. November/December 2019. (Special Issue on Monolithic 3D Architectures)

S. Li, R.S. Verdejo, P. Radojković, and B. Jacob. "Rethinking cycle accurate DRAM simulation." In *Proc. ACM/IEEE International Symposium on Memory Systems (MEMSYS 2019)*, pp. 184–194. Washington DC, October 2019.

Citations: 16

M. Jagasivamani, C. Walden, D. Singh, **L. Kang**, **S. Li**, M. Asnaashari, S. Dubois, D. Yeung, and B. Jacob. "Design for ReRAM-based main-memory architectures." In *Proc. ACM/IEEE International Symposium on Memory Systems (MEMSYS 2019)*, pp. 342–350. Washington DC, October 2019.

Citations: 15

S. Li and B. Jacob. "Statistical DRAM modeling." In *Proc. ACM/IEEE International Symposium on Memory Systems (MEMSYS 2019)*, pp. 521–530. Washington DC, October 2019.

Citations: 10

M. Radulovic, R. Verdejo, P. Carpenter, P. Radojković, B. Jacob, and E. Ayguadé. "PROFET: Modeling system performance and energy without simulating the CPU." *Proceedings of the ACM on Measurement and Analysis of Computing Systems (POMACS)*, vol. 3, no. 2, pp. 34:1–33. June 2019.

Citations: 11

S. Li, **D. Reddy**, and B. Jacob. "A performance & power comparison of modern high-speed DRAM architectures." In *Proc. IEEE International Symposium on Memory Systems (MEMSYS 2018)*, pp. 331–343. Washington DC, October 2018.

Citations: 42

R.S. Verdejo, K. Asifuzzaman, M. Radulovic, P. Radojković, E. Ayguade, and B. Jacob. "Main memory latency simulation: The missing link." In *Proc. IEEE International Symposium on Memory Systems (MEMSYS 2018)*, pp. 107–116. Washington DC, October 2018.

Citations: 18

M. Jagasivamani, C. Walden, D. Singh, **L. Kang**, **S. Li**, M. Asnaashari, S. Dubois, B. Jacob, and D. Yeung. "Memory-system design challenges in realizing monolithic computers." In *Proc. IEEE International Symposium on Memory Systems (MEMSYS 2018)*, pp. 98–104. Washington DC, October 2018.

Citations: 12

S. Li, **P.-C. Huang**, and B. Jacob. "Exascale interconnect topology characterization and parameter exploration." In *Proc. 20th IEEE International Conference on High Performance Computing and Communications (HPCC 2018)*. Exeter UK, June 2018.

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D. M. Mathew, E. F. Zulian, M. Jung, K. Kraft, C. Weis, B. Jacob, N. Wehn. "Using run-time reverse-engineering to optimize DRAM refresh." In *Proc. International Symposium on Memory Systems (MEMSYS 2017)*, pp. 115–124. Washington DC, October 2017.

Citations: 11

S. Li, **P.-C. Huang**, **D. Banks**, **M. DePalma**, **A. Elshaarany**, S. Hemmert, A. Rodrigues, **E. Ruppel**, **Y. Wang**, J. Ang, and B. Jacob. "Low latency, high bisection-bandwidth networks for exascale memory systems." In *Proc. 2016 International Symposium on Memory Systems (MEMSYS 2016),* pp. 62–73. Washington DC, October 2016.

P. Tschirhart, **J. Stevens**, Z. Chishti, and B. Jacob. "The case for associative DRAM caches." In *Proc. 2016 International Symposium on Memory Systems (MEMSYS 2016),* pp. 211–219. Washington DC, October 2016.

I. Bhati, M.-T. Chang, Z. Chishti, S.-L. Lu, and B. Jacob. "DRAM refresh mechanisms, penalties, and trade-offs." *IEEE Transactions on Computers*, vol. 65, no. 1, pp. 108–121. January 2016.

Citations: 156

P. Tschirhart, **J. Stevens**, Z. Chishti, S.-L. Lu, and B. Jacob. "Bringing modern hierarchical memory systems into focus: A study of architecture and workload factors on system performance." In *Proc. 2015 International Symposium on Memory Systems (MEMSYS 2015),* pp. 179–190. Washington DC, October 2015.

J. Stevens, P. Tschirhart, and B. Jacob. "The semantic gap between software and the memory system." In *Proc. 2015 International Symposium on Memory Systems (MEMSYS 2015),* pp. 43–46. Washington DC, October 2015.

I. Bhati, Z. Chishti, S.-L. Lu, and B. Jacob. "Flexible Auto-Refresh: Enabling scalable and energy-efficient DRAM refresh reductions." In *Proc. 42nd International Symposium on Computer Architecture (ISCA 2015)*, pp. 235–246. Portland OR, June 2015.

Citations: 126

B. Jacob. "The 2 petaflop, 3 petabyte, 9 TB/s, 90 kW cabinet: A system architecture for Exascale and Big Data." *IEEE Computer Architecture Letters*, vol. 15 , no. 2 , pp. 125–128. July–December 2016. Published on-line June 2015.

B. Jacob. "The case for VLIW-CMP as a building block for Exascale." *IEEE Computer Architecture Letters*, vol. 15 , no. 1, pp. 54–57. January–June 2016. Published on-line April 2015.

I. Bhati, Z. Chishti, and B. Jacob. "Coordinated Refresh: Energy-efficient techniques for DRAM refresh scheduling." In *Proc. 2013 International Symposium on Low Power Electronics and Design (ISLPED 2013)*, pp. 205–210. Beijing China, September 2013.

Citations: 32

J. Stevens, P. Tschirhart, M.-T. Chang, I. Bhati, P. Enns, J. Greensky, Z. Chishti, S.-L. Lu, and B. Jacob. "An integrated simulation infrastructure for the entire memory hierarchy: Cache, DRAM, nonvolatile memory, and disk." *Intel Technology Journal*, vol. 17, no. 1, pp. 184–200. April 2013.

Citations: 28

B. Jacob. "Forward ... A Foreword." Foreword to Special Issue on Memory Systems, *Intel Technology Journal*, vol. 17, no. 1. April 2013.

M.-T. Chang, **P. Rosenfeld**, S.-L. Lu, and B. Jacob. "Technology comparison for Large Last-Level Caches (L3Cs): Low-leakage SRAM, low write-energy STT-RAM, and refresh-optimized eDRAM." In *Proc. 19th International Symposium on High Performance Computer Architecture (HPCA 2013)*, pp. 143–154. Shenzhen China, February 2013.

Citations: 297

E. Cooper-Balis, **P. Rosenfeld**, and B. Jacob. "Buffer On Board memory systems." In *Proc. 39th International Symposium on Computer Architecture (ISCA 2012)*, pp. 392–403. Portland OR, June 2012.

Citations: 68

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K. Bergman, G. Hendry, P. Hargrove, J. Shalf, B. Jacob, K. S. Hemmert, A. Rodrigues, and D. Resnick. "Let there be light! The future of memory systems is photonics and 3D stacking." In *Proc. ACM SIGPLAN Workshop on Memory Systems Performance and Correctness (MSPC 2011)*, pp. 43–48. San Jose CA, June 2011.

Citations: 15

P. Rosenfeld, **E. Cooper-Balis**, and B. Jacob. "DRAMsim2: A cycle-accurate memory-system simulator." *Computer Architecture Letters*, vol. 10, no. 1, pp. 16–19. January 2011.

Citations: 1,138

A. Rodrigues, K. Hemmert, B. Barrett, C. Kersey, R. Oldfield, M. Weston, R. Risen, J. Cook, **P. Rosenfeld**, **E. Cooper-Balls**, and B. Jacob. "The Structural Simulation Toolkit." *ACM SIGMETRICS Performance Evaluation Review*, vol. 38, no. 4, pp. 37–42. March 2011.

Citations: 397

E. Cooper-Balis and B. Jacob. "Fine-grained activation for power reduction in DRAM." *IEEE Micro*, vol. 30, no. 3, pp. 34–47. May/June 2010.

Citations: 88

C. Dirik and B. Jacob. "The performance of PC solid-state disks (SSDs) as a function of bandwidth, concurrency, device architecture, and system organization." In *Proc. 36th International Symposium on Computer Architecture (ISCA 2009)*, pp. 279–289. Austin TX, June 2009.

Citations: 294

S. Srinivasan, L. Zhao, **B. Ganesh**, B. Jacob, M. Espig, and R. Iyer. "CMP memory modeling: How much does accuracy matter?" In *Proc. Fifth Annual Workshop on Modeling, Benchmarking and Simulation (MoBS 2009)*, pp. 24–33. Austin TX, June 2009.

Citations: 31

A. Jaleel, R. S. Cohn, C.-K. Luk, and B. Jacob. "CMP$im: A Pin-based on-the-fly multi-core cache simulator." In *Proc. Fourth Annual Workshop on Modeling, Benchmarking and Simulation (MoBS 2008)*, pp. 28–36. Beijing China, June 2008.

Citations: 246

A. Varma, E. Debes, I. Kozintsev, P. Klein, and B. Jacob. "Accurate and fast system-level power modeling: An XScale-based case study." *ACM Transactions on Embedded Computing Systems*, vol. 7, no. 3, pp. 25:1–20. April 2008.

Citations: 43

➡ Identical to September 2007 article of same title; reason for reprinting unknown; reason for reordering author list also unknown.

A. Varma, B. Jacob, E. Debes, I. Kozintsev, and P. Klein. "Accurate and fast system-level power modeling: An XScale-based case study." *ACM Transactions on Embedded Computing Systems*, vol. 6, no. 4, pp. 26:1–20. September 2007.

Citations: *see April 2008 printing of article, above*

B. Ganesh, **A. Jaleel**, **D. Wang**, and B. Jacob. "Fully-Buffered DIMM memory architectures: Understanding mechanisms, overheads and scaling." In *Proc. 13th International Symposium on High Performance Computer Architecture (HPCA 2007)*, pp. 109–120. Phoenix AZ, February 2007.

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J. Teller, C. Silio, and B. Jacob. "Performance characteristics of MAUI: an intelligent memory system architecture." In *Proc. Workshop on Memory System Performance (MSP 2005)*, pp. 44–53. Chicago IL, June 2005.

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A. Jaleel and B. Jacob. "Using virtual load/store queues (VLSQs) to reduce the negative effects of reordered memory instructions." In *Proc. 11th IEEE International Symposium on High Performance Computer Architecture (HPCA 2005)*, pp. 191–200. San Francisco CA, February 2005.

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➡ Aamer Jaleel won the *Best Paper Presentation* award for his talk presenting this paper (*International Symposium on High Performance Computer Architecture*, February 2005).

A. Varma, E. Debes, I. Kozintsev, and B. Jacob. "Instruction-level power dissipation in the Intel XScale embedded microprocessor." In *Proc. SPIE's 17th Annual Symposium on Electronic Imaging Science & Technology*, vol. 5683, pp. 1–8. San Jose CA, January 2005.

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H. Wang, **S. V. Rodriguez**, **C. Dirik**, **A. Gole**, **V. Chan**, and B. Jacob. "TERPS: The Embedded Reliable Processing System." A finalist in the University LSI Design Contest. *Asia and South Pacific Design Automation Conference 2005 (ASP-DAC 2005)*. Shanghai China, January 2005.

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B. Iyer, **S. Srinivasan**, and B. Jacob. "Extended Split-Issue: Enabling flexibility in the hardware implementation of NUAL VLIW DSPs." In *Proc. 31st Annual ACM/IEEE International Symposium on Computer Architecture (ISCA 2004)*, pp. 364–375. München Germany, June 2004.

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V. Cuppu, B. Jacob, B. Davis, and T. Mudge. "High performance DRAMs in workstation environments." *IEEE Transactions on Computers*, vol. 50, no. 11, pp. 1133–1153. November 2001. (Special Issue on High-Performance Memory Systems)

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K. Baynes, **C. Collins**, **E. Fiterman**, **B. Ganesh**, **P. Kohout**, **C. Smit**, **T. Zhang**, and B. Jacob. "The performance and energy consumption of three embedded real-time operating systems." In *Proc. International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2001)*, pp. 203–210. Atlanta GA, November 2001.

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S. Srinivasan, **V. Cuppu**, and B. Jacob. "Transparent data-memory organizations for digital signal processors." In *Proc. International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2001)*, pp. 44–48. Atlanta GA, November 2001.

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B. Davis, T. Mudge, **V. Cuppu**, and B. Jacob. "DDR2 and low-latency variants." In *Proc. Workshop on Solving the Memory Wall Problem*, pp. 15–29. Vancouver, British Columbia, June 2000.

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B. Davis, T. Mudge, and B. Jacob. "The new DRAM interfaces: SDRAM, RDRAM and variants." In *High Performance Computing, Lecture Notes in Computer Science*, Vol. 1940, pp. 26–31. M. Valero, K. Joe, M. Kitsuregawa, and H. Tanaka, Editors. Springer Publishing: Tokyo, Japan, 2000.

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D. Stewart and B. Jacob. "Hardware/software co-design of I/O interfacing hardware and real-time device drivers for embedded systems." In *Proc. International Conference on Compiler and Architecture Support for Embedded Systems (CASES 1999)*, pp. 115–119. Washington DC, October 1999.

B. Jacob. "Cache design for embedded real-time systems." In *Proc. Embedded Systems Conference–Summer*. Danvers MA, June 1999. CD-ROM proceedings.

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B. Jacob and T. Mudge. "Virtual memory in contemporary microprocessors." *IEEE Micro*, vol. 18, no. 4, pp. 60–75. July/August 1998.

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B. Jacob and T. Mudge. "Software-managed address translation." In *Proc. Third IEEE International Symposium on High Performance Computer Architecture (HPCA 1997)*, pp. 156–167. San Antonio TX, February 1997.

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B. Jacob, P. Chen, S. Silverman, and T. Mudge. "An analytical model for designing storage hierarchies." *IEEE Transactions on Computers*, vol. 45, no. 10, pp. 1180–1194. October 1996.

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B. Jacob. "Service Discovery: Access to local resources in a nomadic environment." *OOPSLA 1996 Workshop on Object Replication and Mobile Computing*. San Jose CA, October 1996. **Note:** The original extended abstract submitted to the conference was entitled "Support for nomadism in a global environment," which is the title given on some websites.

B. Jacob and T. Mudge. "The trading function in action." In *Proc. 1996 ACM SIGOPS European Workshop*, pp. 241–247. Connemara, Ireland, September 1996.

B. Jacob. "Composing with genetic algorithms." In *Proc. 1995 International Computer Music Conference (ICMC 1995)*, pp. 452–455. Banff Alberta, September 1995.

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B. Jacob. "The use of distributed objects and dynamic interfaces in a wide-area transaction environment." *SIGCOMM 1995 Workshop on Middleware*. Cambridge MA, August 1995.

D. Chapters in Books

B. Jacob. "Reward: How to Foster a Technology-Innovation Culture within a Large Organization (What You Can Learn from Startup Companies)." In The Handbook of Technology Management, pp. 1:964–1:977. H. Bidgoli, Editor. John Wiley & Sons: Hoboken NJ, 2009.

B. Jacob. "Virtual Memory." In Computer Sciences. R. Flynn, Editor. Macmillan Reference USA: Farmington Hills MI, 2002.

B. Jacob. "Virtual Memory Systems and TLB Structures." In The Computer Engineering Handbook, pp. 5:55–5:65. V. Oklobdzija, Editor. CRC Press: Boca Raton FL, 2002.

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➡ In February, 2003, The Computer Engineering Handbook was honored as an Outstanding Academic Title for 2002 by *Choice Magazine*, a publication of the American Library Association.

B. Jacob, J. Szczepanski, and P. Ho. "SiO J=1–0 Emission Near the Galactic Center: Tidal Stripping and Shocks?" In Interstellar Matter. Gordon and Breach: New York NY, 1987.

E. Technical Reports & White Papers

Y. Xue, **L. Kang**, W. Jia, X. Wang, J. Kim, C. Youn, M. J. Kang, H. J. Lim, B. Jacob, J. Huang. "Building a trusted execution environment for in-storage computing." *arXiv preprint* arXiv:2205.06361. May 2022.

P. Rosenfeld, **E. Cooper-Balis**, T. Farrell, D. Resnick, and B. Jacob. "Peering over the memory wall: Design space and performance analysis of the Hybrid Memory Cube." Tech. Rep. UMD-SCA-2012-10-01, University of Maryland Systems & Computer Architecture Group. October 2012.

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A. Rodrigues, K. Bergman, D. Bunde, **E. Cooper-Balis**, K. Ferreira, K.S. Hemmert, B. Barrett, C. Versaggi, R. Hendry, B. Jacob, H. Kim, V. Leung, M. Levenhagen, M. Rasquinha, R. Riesen, **P. Rosenfeld**, M. Varela, S. Yalamanchili. "Improvements to the Structural Simulation Toolkit." Tech. Rep. SAND2012-2185C, Sandia National Lab. March 2012.

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A. Jaleel, R. S. Cohn, C-K. Luk, and B. Jacob. "CMP$im: A binary instrumentation approach to modeling memory behavior of workloads on CMPs." Tech. Rep. UMD-SCA-2006-01, University of Maryland Systems & Computer Architecture Group. June 2006.

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B. Jacob. *Synchronous DRAM Architectures, Organizations, and Alternative Technologies*. Technical Report, University of Maryland. December 2002.

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B. Jacob. *The RiSC-16 Instruction-Set Architecture*. ENEE 446: Digital Computer Design, University of Maryland. Fall 2000.

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➡ This is a description of a teaching architecture that I developed at the University of Maryland and which has been used as a teaching aid in numerous other universities around the world and realized in silicon by my own research group and several others as well.

B. Jacob and S. Bhattacharyya. "Real-time memory management: Compile-time techniques and run-time mechanisms that enable the use of caches in real-time systems." Tech. Rep. UMIACS-TR-2000-60, University of Maryland Institute for Advanced Computer Studies (UMIACS). September 2000.

C. Collins, **E. Fiterman**, **T. Zhang**, and B. Jacob. "SimBed: Accurate microarchitecture-level simulation of embedded real-time operating systems." Tech. Rep. UMD-SCA-2000-1, University of Maryland Systems & Computer Architecture Group. April 2000.

V. Cuppu and B. Jacob. "Organizational design trade-offs at the DRAM, memory bus, and memory controller level: Initial results." Tech. Rep. UMD-SCA-1999-2, University of Maryland Systems & Computer Architecture Group. November 1999.

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E. Berkovich, J. Nuzman, M. Franklin, B. Jacob, and U. Vishkin. "XMT-M: A scalable decentralized processor." Tech. Rep. UMIACS-TR-99-55. University of Maryland Institute for Advanced Computer Studies (UMIACS). October 1999.

B. Jacob. "Segmented addressing solves the virtual cache synonym problem." Tech. Rep. UMD-SCA-1997-1, University of Maryland Systems & Computer Architecture Group. December 1997.

B. Jacob. *Software-Oriented Memory-Management Design*. PhD thesis, The University of Michigan. July 1997.

B. Jacob. "Notes on calculating computer performance." Tech. Rep. CSE-TR-231-95, University of Michigan. March 1995.

Citations: 14

B. Jacob. *Optimization of Mass Storage Hierarchies*. M.S. thesis, Tech. Rep. CSE-TR-228-95, The University of Michigan. May 1994.

F. Editorial Work

B. Jacob and S. Bhattacharyya, Editors. Embedded Systems: The Memory Resource. Special (and inaugural) issue of *ACM Transactions on Embedded Computing Systems*, vol. 1, no. 1, September 2002.

G. Keynotes, Special Seminars, and High-Level Briefings

"Ridiculously Simple Computers (& simulation thereof)," **Invited Talk**, *Modeling & Simulation of Systems and Applications (ModSim)*, Seattle WA. Fall 2024.

"All Tomorrow's Memories (and Kernels)." **Keynote,** *HiPEAC Memory-Centric Computing for Data-Intensive Workloads (MCC)*. München Germany, Winter 2024.

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"Whither External Memory?" **Panelist Talk**, *SRC/SIA/DOE Decadal Plan for Semiconductors: New Trajectories for Memory and Storage Technologies*. Fall 2020.

One of roughly thirty members of academia, government labs, and industry invited to participate with SRC in creating a roadmap for memory devices and systems in the coming decade.

"DRAMsimL — Current Issues in Its Development." **Invited Talk**, *DOE Brainstorming Workshop on Machine Learning for Modeling and Simulation.* Fall 2020.

"Machine Learning is the Holy Grail of Memory-System Modeling & Simulation." **Panelist Talk**, *Modeling & Simulation of Systems and Applications (ModSim).* Fall 2020.

"All Tomorrow's Memories ... for Multicore." **Keynote**, *Multicore World 2020.* Wellington NZ, Winter 2019/20.

"Faster and Accurater — The Future of Memory-System Modeling and Simulation." **Invited Talk**, *Modeling & Simulation of Systems and Applications (ModSim)*, Seattle WA. Fall 2019.

"All Tomorrow's Memories." **Invited Talk**, *University of Texas at Austin Electrical & Computer Engineering Department.* Austin TX, Winter 2018/19.

"Tomorrow's [High-Performance] Memory Systems, Rev. 2018." **Keynote,** *Supercomputing 2018 Memory-Centric HPC Workshop (MCHPC 2018)*. Dallas TX, Fall 2018.

"Modeling Tomorrow's Memory Systems." **Invited Talk**, *Modeling & Simulation of Systems and Applications (ModSim).* Seattle WA, Fall 2018.

"All Tomorrow's Memory Systems." **Panelist Talk**, *ICCD Special Panel — Non-Volatile Memory: will it be memory, storage, or neither of them? (ICCD 2018).* Orlando FL, Fall 2018.

"All Tomorrow's Memories." **Panelist Talk**, *18th IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing (CCGrid 2018).* Washington DC, Spring 2018.

"Tomorrow's Memory Systems and What They Enable." **Invited Talk,** *Chesapeake Large-Scale Analytics Conference.* Annapolis MD, Fall 2017.

CLSAC is an annual limited-attendance DOE conference on analytics in high-performance computing. Attendance is by invitation only, and all talks are invited (e.g., no talks are contributed; all are solicited by the program committee).

"What needs to happen to restore balance and performance efficiency as we approach exascale?" **Panelist Talk**, *International Supercomputing Conference.* Frankfurt Germany, Fall 2017.

"Modeling Tomorrow's Memory Systems." **Invited Talk**, *Modeling & Simulation of Systems and Applications (ModSim).* Seattle WA, Fall 2017.

"Tomorrow's Memory Systems, Rev. 2017." **Chaired Professorship Talk**, *Texas A&M University Computer Science & Engineering Department*. College Station TX, Spring 2017.

"Tomorrow's Memory Systems, Rev. 2017." **Keynote**, *DATE Workshop on Emerging Memory Solutions.* Dresden Germany, Spring 2017.

"A Couple Decades of (accidental) Hardware/Software Co-Optimization." Computer Engineering **Eminent Scholar Seminar Series**, *Texas A&M University Electrical & Computer Engineering Department*. College Station TX, Fall 2016.

"Highly Efficient Systems from Embedded to Exascale — All Begin with Memory." **Keynote**, *FutureWorld.tech.* London Great Britain, Fall 2016. Conference postponed to 2017.

"Execution Models and the Memory System." **Invited Talk**, *Computing 2025 and Beyond: DOE round table held at Argonne National Laboratory*. Lemont IL, Summer 2016.

One of roughly a dozen members of academia and industry invited to participate with DOE in creating a roadmap for computer science and applied mathematics research at DOE in the coming decades.

"Exascale Begins at the Memory System." **Invited Talk**, *Salishan Conference on High-Speed Computing.* Gleneden Beach OR, Spring 2016.

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Salishan is an annual limited-attendance DOE conference on high-performance computing. Attendance is by invitation only, and all talks are invited (e.g., no talks are contributed; all are solicited by the program committee).

"Exascale Begins at the Memory System." **Keynote**, *DATE Workshop on Emerging Memory Solutions.* Dresden Germany, Spring 2016.

"Tomorrow's High-Bandwidth, High-Capacity, Low-Power Memory Systems." **Invited Talk**, *High-End Computing Inter-Agency Workgroup (HEC IWG), Networking and Information Technology Research and Development (NITRD).* Washington DC, Fall 2015.

Briefing to an inter-agency workgroup interested in high-performance computing and comprised of division directors at DARPA, DOE, NASA, and NSA.

"Tomorrow's High-Bandwidth, High-Capacity, Low-Power Memory Systems." **Keynote**, *Modeling & Simulation of Systems and Applications (ModSim).* Seattle WA, Fall 2015.

"Next-Generation Memory Systems." **Keynote**, *International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS).* Samos Island Greece, Summer 2014.

"High-Bandwidth, High-Capacity, Low-Power Memory Systems." **Keynote**, *ACM International Conference on Computing Frontiers.* Cagliari Italy, Spring 2014 .

"Data Access, Data Movement, Data Integrity." ***Briefing*** *to Secretary Steven Chu*. Spring 2012.

One of roughly twenty members of academia, industry, and the national laboratories who were asked to brief US Energy Secretary Steven Chu on the status of supercomputing today and what is required to achieve exascale computing performance in the near future.

"Big Memories." **Keynote**, *Session on Large Memory Systems & Challenges at International Supercomputing Conference.* Hamburg Germany, Spring 2012.

"Memory Systems: Then, Now, and To Come." **Keynote**, *Session on Memory Systems at International Supercomputing Conference.* Hamburg Germany, Spring 2010.

"Wealth, Innovation, Design, & Entrepreneurship." **Invited Talk**, *Advisory Board to the University of Maryland Department of Electrical & Computer Engineering.* College Park MD, Fall 2009.

"Memory Systems." *National Academies CSTB* ***Briefing****: Trends in Computing Performance.* Mountain View CA, Fall 2007.

One of roughly fifteen people across all areas of computing (including sub-disciplines of Storage, Power, Programming, and Applications) invited to brief a National Academies committee on the state of affairs in our various sub-disciplines. Briefers were asked to inform the committee on the technical issues and present/future trends that can hinder or aid the continued growth of computer performance. The resulting NRC report, *The Future of Computing Performance — Game Over or Next Level?*, can be found online at http://www.nap.edu/catalog/12980/the-future-of-computing-performance-game-over-or-next-level.

H. Other Invited Talks and Presentations

"Careers in (Computer) Engineering." *University of Maryland ECE TA Training and Development Program Workshop*. College Park MD, Spring 2019.

"All Tomorrow's Memory Systems (2018 version)." *DOE ASCR Workshop on Extreme Heterogeneity*. Gaithersburg MD. Winter/Spring 2018.

"Tomorrow's Memory Systems and Monolithic Processors." *National Energy Research Scientific Computing Center*. Berkeley CA, Fall 2017.

"Tomorrow's Memory Systems, Rev. 2017." *Barcelona Supercomputing Center*. Barcelona Spain, Spring 2017.

"A Couple Decades of (accidental) Hardware/Software Co-Optimization." *University of Michigan Department of Electrical Engineering & Computer Science*. Ann Arbor MI, Winter 2016.

"A Bad Talk, A Good Talk, A Bad Talk, A Good Talk, Some Thoughts (or: How Not To Suck)." *University of Maryland ECEGSA Seminar Series.* College Park MD, Fall 2016.

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"Some of Our Work on Hybrid Memory Cube." Invited Talk, *Workshop on Hybrid Memory Cube.* Fort Meade MD, Fall 2015.

"Tomorrow's High-Bandwidth, High-Capacity, Low-Power Memory Systems." *Department of Energy*. Washington DC, Fall 2015.

"Wealth, Innovation, Design, & Economic Growth, and How it Begins with Entrepreneurship." *University of Cyprus*. Nicosia Cyprus, Spring 2014.

"(Exascale) Data Movement." *Foundation for Research and Technology (FORTH).* Heraklion (Crete) Greece, Winter 2013.

"(Exascale) Data Movement." *University of Cyprus.* Nicosia Cyprus, Winter 2013.

"Research and Development in Electrical & Computer Engineering." Invited talk, *Career Day at Baltimore Polytechnic Institute.* Baltimore MD, Spring 2010.

"Trends in Memory Systems." *Sun-DARPA UNIC Architecture Workshop.* Menlo Park CA, Winter 2010.

"Innovation & Design ... and Modern Engineering Entrepreneurship." *University of Maryland Clark School Board of Visitors.* College Park MD, Fall 2009.

"High-Tech Design as Modern Engineering Entrepreneurship." *University of Maryland ECEGSA Seminar Series.* College Park MD, Fall 2009.

"Embedded Systems, Memory Systems, and Embedded Memory Systems." *ACACES 2009 Fifth International Summer School on Advanced Computer Architecture and Compilation for Embedded Systems.* Terrassa Spain, Summer 2009.

"R&D in Electrical & Computer Engineering." *National Student Leadership Conference.* College Park MD, Summer 2009.

"The Memory System and You: A Love/Hate Relationship." Invited Talk, *SOS-13 Workshop on Distributed Supercomputing.* Hilton Head SC, Spring 2009.

"R&D in Electrical & Computer Engineering." *National Student Leadership Conference.* College Park MD, Summer 2008.

"Engineering Entrepreneurship: Towards a High-Tech Cottage Industry." *University of Maryland Inventis Lecture Series on Professional Concepts in Engineering*. College Park MD, Spring 2008.

"Design as Modern Engineering Entrepreneurship." Invited lecture. *UNIV 100, The Student and the University.* College Park MD, Fall 2007.

"Embedded and Non-Classical Systems." *Dialogue with the Dean lecture series, University of Maryland College of Engineering*. College Park MD, Spring 2006.

"A Holistic Approach to DRAM (and Systems)." *North Carolina State University Electrical & Computer Engineering Department.* Raleigh NC, Spring 2006.

"A Holistic Approach to DRAM-System Design." *IBM T.J. Watson Research Center.* Yorktown Heights NY, Winter 2004.

"A Bad Talk, A Good Talk, A Bad Talk, A Good Talk, Some Thoughts (or: How Not To Suck)." First presented at *University of Maryland ECEGSA Seminar Series.* College Park MD, Spring 2004.

"Research Issues in Embedded Systems." *Dialogue with the Dean lecture series, University of Maryland College of Engineering*. College Park MD, Fall 2003.

"Embedded Systems at Maryland." *University of Maryland College of Engineering, Department of Electrical Engineering, Department of Computer Science, Institute for Advanced Computer Studies, and Institute for Systems Research Research Review Day.* College Park MD, Spring 2003.

"How To Do Research (Well)." First presented at *University of Maryland ECEGSA Seminar Series.* College Park MD, Spring 2003.

"DRAM: Architectures, Interfaces, and Systems: A Tutorial." Full-day tutorial presented with David Wang at the *International Symposium on Computer Architecture (ISCA)*. Anchorage AK, Spring 2002.

"Computers and Memory Systems." *Dialogue with the Dean lecture series, University of Maryland College of Engineering*. College Park MD, Fall 2001.

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"Career Paths in Computer Engineering, or So What Are You Going To Do With Your Life?" *University of Maryland IEEE Student-Professional Awareness Conference (S-PAC).* College Park MD, Spring 2001.

"How Not to Configure Your DRAM System." *Compaq Systems Research Group.* Marlborough MA, Fall 2000.

"High-Performance DRAM Systems." *Compaq Alpha Group.* Shrewsbury MA, Fall 2000.

"Contemporary DRAM Architectures and Beyond." *Compaq Systems Research Center.* Palo Alto CA, Fall 1999.

"Cache Design for Embedded Real-Time Systems." *Embedded Systems Conference.* Danvers MA, Spring 1999.

"DRAM Memory Systems." *IBM T.J. Watson Research Center.* Yorktown Heights NY, Spring 1999.

"The Top 10 Lessons I Learned as a Grad Student." First presented at *University of Maryland Electrical & Computer Engineering Department.* College Park MD, Fall 1998.

"Software-Managed Memory Systems." *University of Wisconsin Electrical & Computer Engineering Department.* Madison WI, Spring 1998.

"The IA-64 Architecture." *University of Maryland IEEE Chapter.* College Park MD, Fall 1997.

I. Conference-Paper Presentations

"Thoughts on Merging the File System and Virtual Memory System." Presented at *The 9th ACM/IEEE International Symposium on Memory Systems (MEMSYS 2023)*. Washington DC, October 2023.

"Exascale Interconnect Topology Characterization and Parameter Exploration." Presented at *The 20th IEEE International Conference on High Performance Computing and Communications (HPCC 2018)*. Exeter United Kingdom, June 2018.

"Energy/Power Breakdown of Pipelined Nanometer Caches (90nm/65nm/45nm/32nm)." Presented at *The International Symposium on Low Power Electronics and Design (ISLPED 2006)*. Tegernsee Germany, October 2006.

"Concurrency, Latency, or System Overhead: Which Has the Largest Impact on Uniprocessor DRAM-System Performance?" Presented at *The 28th International Symposium on Computer Architecture (ISCA 2001).* Göteborg Sweden, June 2001.

"Hardware/Software Architectures for Real-Time Caching." Presented at *The Second International Workshop on Compiler and Architecture Support for Embedded Systems (CASES 1999)*. Washington DC, December 1999.

"A Performance Comparison of Contemporary DRAM Architectures." Presented at *The 26th Annual ACM/IEEE International Symposium on Computer Architecture (ISCA 1999).* Atlanta GA, May 1999.

"Software-Managed Caches: Architectural Support for Real-Time Embedded Systems." Presented at *The First International Workshop on Compiler and Architecture Support for Embedded Systems (CASES 1998).* Washington DC, December 1998.

"A Look at Several Memory Management Units, TLB-Refill Mechanisms, and Page Table Organizations." Presented at *The Eighth ACM/IEEE International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 1998).* San Jose CA, October 1998.

"Software-Managed Address Translation." Presented at *The Third IEEE International Symposium on High Performance Computer Architecture (HPCA 1997).* San Antonio TX, February 1997.

"Method Invocation in the Face of Anarchy." Presented at *The 1996 OOPSLA Workshop on Object Replication and Mobile Computing (ORMC 1996).* San Jose CA, October 1996.

"Composing with Genetic Algorithms." Presented at *The 1995 International Computer Music Conference (ICMC 1995).* Banff Alberta, September 1995.

J. Patents Issued

Integrating a Resistive Memory System into a Multicore CPU Die to Achieve Massive Memory Parallelism. US Patent 11,126,550; issued September 21, 2021; filed September 4, 2018. Donald Yeung, Bruce L. Jacob, Mehdi Asnaashari, and Sylvain Dubois, Crossbar Inc. and University of Maryland at College Park.

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Programmable Switch for Configuring Circuit Topologies. US Patent 8,445,770, issued May 21, 2013; filed September 21, 2008; claiming priority to provisional patent filed June 14, 2008. Bruce Jacob.

Citations: 20

Volume-Adjustment Circuit for Equilibrating Pickup Settings. US Patent 8,324,495, issued December 4, 2012; filed February 13, 2009. Bruce Jacob.

Citations: 11

Electronic Guitar Harness Component Connector. US Patent 7,915,506, issued March 29, 2011; filed August 10, 2010. Bruce Jacob.

System and Method for Performing Multi-Rank Command Scheduling in DDR SDRAM Memory Systems. US Patent 7,543,102, issued June 2, 2009; filed April 17, 2006; claiming priority to provisional patent filed April 18, 2005. Bruce Jacob and Dave Wang, University of Maryland.

Citations: 89

K. Cited Patent Applications

NVMM: An Extremely Large, Logically Unified, Sequentially Consistent Main-Memory System. US Patent Application 2016/0253123, filed March 18, 2015; published September 1, 2016. Bruce Jacob.

Citations: 10

L. Computational Artifacts

DRAMsimL, developed 2019–present (ongoing)
A machine-learning-based memory-system simulation framework that can be used in place of traditional cycle-accurate simulation, for early experimental results. The framework is described in the following publications:

S. Li, R.S. Verdejo, P. Radojković, and B. Jacob. "Rethinking cycle accurate DRAM simulation." In Proc. ACM/IEEE International Symposium on Memory Systems (MEMSYS 2019), pp. 184–194. Washington DC, October 2019.

S. Li and B. Jacob. "Statistical DRAM modeling." In Proc. ACM/IEEE International Symposium on Memory Systems (MEMSYS 2019), pp. 521–530. Washington DC, October 2019.

The framework relies upon the results of cycle-accurate simulators, which are used to create the statistical models.

NVsim, developed 2009–present (ongoing)
A framework for simulating non-volatile memories of all types (including NAND flash, NOR flash, PCM, and SST-RAM). It has been developed by my graduate students and is described in the following publication:

J. Stevens, P. Tschirhart, M.-T. Chang, I. Bhati, P. Enns, J. Greensky, Z. Chishti, S.-L. Lu, and B. Jacob. "An integrated simulation infrastructure for the entire memory hierarchy: Cache, DRAM, nonvolatile memory, and disk." *Intel Technology Journal*, vol. 17, no. 1. April 2013.

The framework accurately models configurations of non-volatile memories in SSD architectures as well as in standalone configurations such as hybrid main memories.

DRAMsim, developed 1999–present (ongoing)
A memory-system simulation framework that interacts with popular CPU simulators such as MARSSx86, SST, GEMS, MASE, and SimAlpha. It has been developed by my graduate students and represents many student-decades of development effort. The framework is described in the following publications:

D. Wang, B. Ganesh, N. Tuaycharoen, K. Baynes, A. Jaleel, and B. Jacob. "DRAMsim: A memory-system simulator." *SIGARCH Computer Architecture News*, vol. 33, no. 4, pp. 100–107. September 2005.

P. Rosenfeld, E. Cooper-Balis, and B. Jacob. "DRAMsim2: A cycle-accurate memory-system simulator." *Computer Architecture Letters*, vol. 10, no. 1, pp. 16–19. January 2011.

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S. Li, Z. Yang, D. Reddy, A. Srivastava, B. Jacob. "DRAMsim3: A cycle-accurate, thermal-capable DRAM simulator." IEEE Computer Architecture Letters, published on-line February 2020.

The software has been released to the community under the GNU Public License and can be found at github.com/dramninjasUMD/DRAMSim2.

BioBench/BioParallel, developed 2004–2005

A collection of benchmarks, each a different application area within the larger domain of bioinformatics and data mining. BioBench, a suite of workloads collected by students and faculty at the University of Maryland, was released in 2005. The suite expanded in 2006 with the addition of parallel workloads collected by researchers at Intel (distinguished from the original *BioBench* suite as the *BioParallel* suite). Described in the following publications:

K. Albayraktaroglu, **A. Jaleel**, X. Wu, M. Franklin, B Jacob, C. Tseng, and D. Yeung. "BioBench: A benchmark suite of bioinformatics applications." In *Proc. ISPASS 2005*, pp. 2–9. Austin TX, March 2005.

A. Jaleel, M. Mattina, and B. Jacob. "Last-level cache (LLC) performance of data-mining workloads on a CMP — A case study of parallel bioinformatics workloads." In *Proc. HPCA 2006*, pp. 88–98. Austin TX, February 2006.

The benchmark suites have been released to the community and can be found at www.ece.umd.edu/biobench.

Variations, developed 1994–1996

A music composition system that uses genetic algorithms to generate and organize complex tonal and microtonal music for orchestral organizations. The software is described in the following publications:

B. Jacob. "Composing with genetic algorithms." In *Proc. 1995 International Computer Music Conference*, pp. 452–455. Banff Alberta, September 1995.

B. Jacob. "Algorithmic composition as a model of creativity." *Organised Sound*, vol. 1, no. 3, pp. 157–165. December 1996.

High-fidelity audio examples of the system's output (in MP3 format) as well as the software itself can be found at www.ece.umd.edu/~blj/algorithmic_composition.

Telecom Services Architecture, developed 1991–1996

A distributed system of active network objects whose service methods are invoked transparently via a service broker. The software is described in the following publications:

B. Jacob. "The use of distributed objects and dynamic interfaces in a wide-area transaction environment." *SIGCOMM 1995 Workshop on Middleware*. Cambridge MA, August 1995.

B. Jacob and T. Mudge. "The trading function in action." In *Proc. 1996 ACM SIGOPS European Workshop*, pp. 241–247. Connemara Ireland, September 1996.

This architecture was created for the telecommunications startup Priority Call Management. The software forms the core technology in Priority Call's product line, and the architecture was still in use as late as 1999.

M. Honors and Awards

Named Fellow, Institute of Electrical and Electronics Engineers (2020, effective 2021)

The IEEE Board of Directors, at its November 2020 meeting, elevated to IEEE Fellow, effective 1 January 2021, with the following citation:

for contributions to computer memory design and analysis

Invited to serve on ACM/IEEE CS George Michael Memorial HPC Fellowship Committee (2018–2020)

Served on the international Fellowship Committee for three years. The Fellowship "honors exceptional PhD students throughout the world whose research focus is on high-performance computing applications, networking, storage, or large-scale data analysis using the most powerful computers that are currently available.
The award committee is selected by the two societies and includes past winners as well as leaders in the field."

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University of Maryland "Research Leader" (2017)
Recognized by the University of Maryland's Division of Research as "having made significant contributions to the University of Maryland College Park research program."

University of Maryland "Research Leader" (2016)
Recognized by the University of Maryland's Division of Research as "having made significant contributions to the University of Maryland College Park research program."

University of Maryland "Research Leader" (2012)
Recognized by the University of Maryland's Division of Research as "having made significant contributions to the University of Maryland College Park research program."

University of Maryland "Research Leader" (2010)
Recognized by the University of Maryland's Division of Research as "having made significant contributions to the University of Maryland College Park research program."

Philip Merrill Presidential Scholar Faculty Mentor (2009)
Recognized as the faculty mentor who has made the most impact on the academic achievement of one of the University of Maryland's Philip Merrill Presidential Scholars.

Clark School of Engineering Keystone Professor (2006)
One of six professors named to Keystone: The Clark School Academy of Distinguished Professors.

University of Maryland "Research Leader" (2006)
Recognized by the Office of Research and Graduate Studies for being one of the top 100 researchers in the University of Maryland, as measured by research funding. Was previously called the University's "Rainmaker" award.

University of Maryland "Rainmaker" (2005)
Recognized by the Office of Research and Graduate Studies for being one of the top 100 researchers in the University of Maryland, as measured by research funding.

Best Paper Presentation (HPCA 2005)
My student, Aamer Jaleel, won the Award for Best Paper Presentation for our paper in the *11th Int'l Symposium on High Performance Computer Architecture (HPCA 2005)*, February 2005.

Award for Teaching Excellence (2004)
Recognized by the University of Maryland (campus-wide) for excellence in teaching at the undergraduate level.

University of Maryland "Rainmaker" (2001)
Recognized by the Office of Research and Graduate Studies for being one of the top 100 researchers in the University of Maryland, as measured by research funding.

National Science Foundation CAREER Award (1999)
Project Title: "Architecture Issues in DRAM Devices and Systems."

George Corcoran Memorial Award (1998–9 Academic Year)
"In recognition of teaching and educational leadership at the University of Maryland, College Park campus, effective contribution at the national level, and creative and other scholarly activities related to Electrical and Computer Engineering education."

N. Professional Memberships

1993–	Member, ACM
1994–	Member, IEEE
1993–1998	Member, USENIX
1999–	USENIX Campus Liaison at University of Maryland

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III. TEACHING AND ADVISING

A. Course Instruction

Teaching evaluation scores are often in the top half dozen scores in the department (out of roughly 70 faculty); they have been the highest-ranking score in the department on numerous occasions.

Academic Year	Course Number	Course Title	No. of Students	Teaching Eval. Total	Average for Similar
1997/1998	ENEE 350H	Computer Organization (Honors)	12	3.81	3.36
	ENEE 759M	Advanced Topics in Microarchitecture	15	3.71	3.37
1998/1999	ENEE 350H	Computer Organization (Honors)	15	4.92 (of 5)	4.20 (of 5)
	ENEE 698b	Computer Engineering Seminar	17		
	ENEE 647	Design of Distributed Systems	50	3.58	3.25
1999/2000	ENEE 350	Computer Organization	45	3.73	3.33
	ENEE 759M	Advanced Topics in Microarchitecture	18	3.87	3.28
2000/2001	ENEE 446	Design of Digital Computers (undergrad)	27	3.74	3.25
	ENEE 350	Computer Organization	20	3.62	3.34
2001/2002	ENEE 646	Design of Digital Computers (grad)	70	3.50	3.14
	ENEE 759M	Advanced Topics in Microarchitecture	45	3.60	3.20
2002/2003	ENEE 646	Design of Digital Computers (grad)	66	3.56	3.24
	ENES 100	Introduction to Engineering Design	36	3.17	2.99
	ENEE 759H	High-Speed Memory Systems	17	3.98	3.23
2003/2004		**On sabbatical**			
2004/2005	ENEE 302H	Digital Electronics (Honors)	24	3.57	3.09
	ENEE 759H	High-Speed Memory Systems	12		
	HONR 218V	Digital Sound and Fury on Mac OSX: Desktop Publishing, Music, Photography, and Video (University Honors)	24		
2005/2006	ENEE 302H	Digital Electronics (Honors)	11	3.52	3.29
	ENEE 446	Design of Digital Computers (undergrad)	23	3.40	3.34
2006/2007	ENEE 646	Design of Digital Computers (grad)	27	3.70	3.30
	ENES 100	Introduction to Engineering Design	36		
	ENEE 359A	Digital VLSI Circuits	15	3.50	3.16
	ENES 100	Introduction to Engineering Design	36		
2007/2008	ENEE 759H	High-Speed Memory Systems	12	3.43	3.11
	ENES 100	Introduction to Engineering Design	40	3.50	3.24
	ENEE 359A	Digital VLSI Circuits	12	3.82	3.24

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Academic Year	Course Number	Course Title	No. of Students	Teaching Eval. Total	Average for Similar
	ENEE 159B	Start-Up 101: Electric Guitar Design	12	3.65	3.39
	ENES 100	Introduction to Engineering Design	40	3.40	3.32
2008/2009	ENEE 646	Design of Digital Computers (grad)	21	3.63	3.31
	ENES 100	Introduction to Engineering Design	41	3.57	3.10
	ENEE 159B	Start-Up 101: Electric Guitar Design	12	3.71	3.29
	ENEE 459J	Start-Up 101: Consumer Electronics	12	3.70	3.34
	ENES 100	Introduction to Engineering Design	40	3.67	3.25
2009/2010	ENEE 350H	Computer Organization (Honors)	25	3.79	3.24
	ENES 100	Introduction to Engineering Design	40	3.55	3.02
	ENEE 359R	Reverse Engineering (Supervisor)	11	3.90	3.24
	ENEE 159B	Start-Up 101: Electric Guitar Design	12	3.71	3.22
	ENES 100	Introduction to Engineering Design	40	3.68	3.21
2010/2011		**On sabbatical**			
2011/2012	ENEE 646	Design of Digital Computers (grad)	25	3.47	3.29
	ENEE 446	Design of Digital Computers (undergrad)	30		
2012/2013	**Visiting at University of Siena (Italy), working on EC-funded TERAFLUX project**				
	PHD-SEM	Advanced Memory Systems (25-hour grad seminar at University of Siena)	7	n/a	n/a
2013/2014	**Visiting at University of Siena, FORTH (Crete, Greece), and University of Cyprus, working on EU-funded TERAFLUX and EuroServer projects**				
	CS-590.26	High-Speed Memory Systems (30-hour grad seminar at University of Crete)	15	n/a	n/a
2014/2015	ENEE 646	Design of Digital Computers (grad)	42	3.63	3.27
	ENEE 245	Digital Circuits & Systems Lab	45	3.11	3.18
	ENEE 245	Digital Circuits & Systems Lab	36	3.59	3.10
2015/2016	ENEE 447	Operating Systems	34	3.33	3.16
2016/2017	ENEE 245	Digital Circuits & Systems Lab	112	3.37	3.18
2017/2018	ENEE 646	Design of Digital Computers (grad)	16	3.38	3.30
	ENEE 408L	Capstone Design: Electric Guitars	12	3.75	3.24
	ENEE 446	Design of Digital Computers (undergrad)	46	3.62	3.18
2018/2019	ENEE 408L	Capstone Design: Electric Guitars	13	3.26	3.23
	ENEE 447	Operating Systems	60	3.74	3.24
2019/2020		**On sabbatical**			

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Academic Year	Course Number	Course Title	No. of Students	Teaching Eval. Total	Average for Similar
2020/2021	ENEE 646	Design of Digital Computers (grad)	16		
	ENEE 447	Operating Systems			
2021/2022	CompSci 2271	Introduction to Computation and Programming	96		
	CompEng 4930	The Design of Modern Computer Systems			
2022/2023	SY110	Introduction to Cyber Security	60		
	SY204	Cyber Systems Programming & OS Fundamentals	20		

B. Undergraduate Independent Study

ENEE499 Spring 2010 *On-Board Low-Power Audio Electronics*, with Rob Brisentine, Noel Cervino, and Matt Wienke. Development of low-power signal-processing electronics to mix synthetic and real-time audio, all run on 9V batteries.

ENEE499 Spring 2010 *A Comparison of Preamps: Transistor-based versus OpAmp-based*, with Ilia Kobrinsky. A comparison of the fidelity and power requirements of two different audio preamp designs.

ENEE 499L Summer 2008 *High-Resolution Low-Power A/D Conversion on an Electric Guitar*, with Spencer Black. Development of analog-to-USB and analog-to-firewire DSP units to go on-board an electric guitar.

ENEE 499 Fall 2007 *Analog Circuit Design for Electric Guitars*, with Justin Ahmanson and Timothy Babich. Design and development of a novel preamp and variable EQ circuit for electric guitar, to be used on-board the guitar and powered by 9V battery.

ENEE 499 Fall 2007 *Applications Engineering*, with Garrett Lang, Han Dao, and Jason Borrero. Design and development of web-based application software. One step in the development of a new course to be called *Start-Up 101: Applications Engineering*.

ENEE 499 Fall 2001 *Verilog Modeling of Real-Time Embedded Systems*, with Vincent Chan, Lei Zong, and David Xia. Development of a Verilog ARM core with support for precise interrupts and programmable I/O controllers.

ENEE499 Spring 2000 *Development of an Embedded-System Simulation Environment*, with Eric Fiterman. Design and development of an embedded-system simulation environment that emulates the embedded CPU and peripheral IO devices as well as a real-time operating system.

ENEE499 Fall 2000 *A Pipelined Microprocessor on an FPGA*, with Andrew Ripple. Implementation of a high-performance pipelined processor on programmable hardware, including timing specifications and performance measurements.

ENEE499 Spring 1999 *Full Computer-System Emulation*, with Aamer Jaleel, Jiwanjot Tulsi, and Yun Hua Wang. Design and development of a simulation environment that emulates both a full workstation (including CPU and peripheral IO devices) and a sophisticated operating system (including support for virtual memory, a file system, and multitasking).

ENEE 499 Spring 1999 *Implementing the Ridiculously Simple Computer*, with Julian Requejo. Design and development of a small digital computer from IC components on circuit bread-boards. The computer will be able to run simple applications stored in memory.

C. Educational Development at the University of Maryland

New courses introduced into the regular curriculum

Developed and introduced *ENEE 759M: Advanced Topics in Microarchitecture*

Developed and introduced *ENEE 759H: High-Speed Memory Systems*

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Developed and introduced *ENEE 447: Operating Systems*

Developed and introduced *ENEE 408L: Electric Guitar Design Capstone*

Developed and introduced *ENEE 359A: Digital VLSI Circuits*

Developed and introduced *ENEE 159B: Electric Guitar Design (Start-Up 101)*

Course development — ENEE 408L: Electric Guitar Capstone Design

At the Department's request, developed a Capstone Design course on electric guitars. The course uses a popular topic (electric guitars) to motivate students to learn about and do research in the fundamentals of electrical & computer engineering, and express their understanding through their design project.

Modern electric guitars contain both EE and CE components; the fundamentals are EE-based, but an increasing number of current designs incorporate CE-based concepts such as active digital control circuits, digital signal processors, and many embedded digital effects units. The course builds upon previous disciplines and development skills students have learned, such as circuit design & test and working with analog and digital circuit components, as well as the interaction between magnetic fields and electric currents. It also introduces skills such as PCB design, fabrication, and assembly, for those students who have not already learned them previously.

The students first start with an assigned experiment: using the guitars, amplifiers, and guitar parts provided to them, they develop and validate an electrical-engineering model for how the guitar's pickup works. Many models exist, but they are often simplistic and overlook critical elements, such as the fact that the bridge must be grounded; the strings are an integral part of the circuit; and the pickup's inductors are not actually necessary: one could (and the students do) put alligator clips on the ends of the strings and send the signal to an amplifier, produced only by the string's vibration over a fixed magnet. The second project is for the students to spend a class period experimenting with different "tone" circuits that have appeared in guitars, to see how the various filtering functions interact with the pickups' inductors and their resonance properties. After coming to a better understanding of the components involved and how they interact, the students then propose their design and spend the rest of the semester implementing and characterizing it.

Course development — ENEE 447: Operating Systems

Asked by department chair to develop and teach an Operating Systems course for the Computer Engineering degree program. Developed a treatment of Operating Systems specifically targeted to Computer Engineers, presenting a deep look at the hardware and how the OS interacts with it. In this course, students build a rudimentary but fully complete operating system from scratch on actual hardware, because, in most Engineering courses, the best way for one to learn how something works is to build it for oneself. The material is covered much in the way that CE and EE courses cover their material: as a sequence of problems, each followed by a range of solutions, proofs of their correctness (in this case, primarily intuitive rather than formal or mathematical proofs), and the advantages and disadvantages of each solution. Topics given special emphasis include multicore processors and nonvolatile memories, both of which call for a shake-up in operating systems design.

In particular, multicore is here to stay, and therefore scheduling, coherence, control, and basic operating-system design all need to be reevaluated. Non-volatile main memory will be here tomorrow, which means that separate virtual memory systems and file systems will become a thing of the past. Issues such as security, reliability, and power/energy efficiency are extremely important today but were less important (in some cases not at all important) when today's operating systems were designed; these warrant reevaluation of existing design choices. Thus, it made sense to address these issues specifically in the course.

The resulting course can serve as a template for how Operating Systems is taught to Computer Engineering students everywhere, as Computer Engineering students have needs and learning styles that are very distinct and different from those of Computer Science students.

Formal course revision & improvement

As Director of Computer Engineering, restructured and reoriented the program's curriculum to address its age and concerns by students, faculty, and graduates that the curriculum needed better structure, cohesiveness, and topical

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focus. In 2007/8 brought together faculty, current students, and recent graduates to work on the program over numerous focus groups and meetings. The new proposed curriculum strengthened the program's focus on hardware, circuits, and electronics and was informally adopted by the Computer Engineering group via vote in the Fall of 2008. The computer group is working on a formal transition and implementation plan.

Member of a Dean's committee appointed to review and revise *ENES 100 — Introduction to Engineering Design*, charged with the task of making the class more attractive to freshmen and more relevant in general. The committee's recommendations resulted in, among other things, the formation by the Dean of a cadre of faculty called *Keystone: The Clark School Academy of Distinguished Professors*, the members chosen by the Dean for their proven teaching skills and ability to reach students, and then charged with realizing the committee's vision. The course is now taught by Keystone professors and has undergone a significant overhaul for the better.

New courses offered on a trial basis

Developed and introduced several pilot courses that are aimed at educating students on the technical aspects of building real-world artifacts. Due to the confluence of several economic factors, now is an ideal time for students and recent graduates to start up medium- and high-tech companies on their own. However, most entrepreneurship classes, workshops, and seminars focus on the business aspects of startups (e.g., funding, attracting venture capitalists, writing business plans, etc.), which ignores the technical/design aspects of entrepreneurship. This group of classes is an attempt to bring into the classroom real-world design & development skills — skills that, unlike manufacturing and construction, are *not* being out-sourced.

Start-Up 101: Electric Guitar Design (ENEE 159B). Design and development of circuits in electric guitars, such as analog switches, volume, and EQ; basic skills and knowledge such as wiring, soldering, electromagnetism, the physics of sound; printed circuit-board design, construction, and assembly. Offered Spring 2008. Note: at the Department's request, this became *ENEE 408L: Capstone Design*.

Start-Up 101: Consumer Electronics (ENEE 459J). Design and development of hardware/software systems, focusing on issues in real-time operating systems, firmware development, circuit-board design and construction, and correctness of design. Offered Spring 2009.

Start-Up 101: Applications Engineering (as ENEE 499). Design and development of large, industrial-strength software applications, 10–100x the size of those typically developed in the classroom. Offered Fall 2007.

Informal course revision & improvement — ENEE 350

Revised ENEE 350 (computer organization) to become a project-oriented course, which is very different from the way it had been taught previously, both in content and in instructional delivery. This approach was successful in both the honors-level course and the regular version of ENEE 350. The approach was introduced to the regular section in the Fall of 1999, and now the projects are used by other faculty in the ECE department and CS department as well.

Informal course revision & improvement — ENEE 446/646

ENEE 446 (computer architecture) focuses on the implementation of microprocessors and systems; the class projects were revised to reflect how industrial-strength designs work and how commercial hardware development is done. To begin with, students implement a microprocessor (the "RiSC-16," designed by me) in the Verilog hardware description language; Verilog is a language used in industry that represents hardware in its VLSI implementation, as opposed to a C-language emulation as is used in 350 and was previously used in 446. To this Verilog implementation students add the necessary hardware constructs to allow an operating system to run on the microprocessor: namely, facilities for precise interrupts and virtual memory. Lastly, the students write the rudiments of an operating system, in assembly code, to run on their Verilog microprocessor.

The projects are used by other faculty in the ECE department. Even more interesting is the response from outside the university. For instance, the RiSC-16 architecture has been used in universities all around the world, such as the University of Illinois at Urbana-Champaign, Université Libre de Bruxelles (Belgium), and Universidad Pontificia Comillas (Spain); the various design documents posted on the class website show up in on-line databases as cited works; numerous developers have contacted me over the years to help them build VLSI implementations of the

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processor design (google "RiSC-16 maryland" to see examples); and the implementation of precise interrupts, an extremely important mechanism that had previously been neglected in *all* computer-systems textbooks — despite the fact that it is nearly impossible to build a working microprocessor without precise interrupts — began to show up in undergraduate texts several years after the RiSC-16 design documents were first posted.

D. Advising at the University of Maryland

Graduated Ph.D. Students

Jennie Hill, Ph.D. 2023. *Evaluation of Selected Side-Channel Analysis Methods for Ransomware Classification and Detection*. (Unites States Naval Academy)

Luyi Kang, Ph.D. 2022. *Tackling Performance and Security Issues for Cloud Storage Systems*. (Intel)

Meenatchi Jagasivamani, Ph.D. 2020. *Resistive RAM Based Main-Memory Systems: Understanding the Opportunities, Limitations, and Tradeoffs*. (Northrop Grumman)

Shang Li, Ph.D. 2019. *Scalable and Accurate Memory System Simulation*. (Cadence Design Systems)

Paul Tschirhart, Ph.D. 2015. *Bringing Modern Multi-Level Main Memory Systems Into Focus*. (Northrop Grumman)

Ishwar Bhati, Ph.D. 2014. *Scalable and Energy-Efficient DRAM Refresh Techniques*. (Oracle)

Paul Rosenfeld, Ph.D. 2014. *Performance Exploration of the Hybrid Memory Cube*. (Micron)

Mu-Tien Chang, Ph.D. 2013. *Technology Choices for Large Last-Level Caches*. (Samsung)

Elliott Cooper-Balis, Ph.D. 2012. *Buffer-on-Board Memory Systems*. (Micron)

Cagdas Dirik, Ph.D. 2009. *Performance and Analysis of NAND Flash Memory Solid-State Disks*. (SanDisk)

Sadagopan Srinivasan, Ph.D. 2007. *Prefetching vs. the Memory System: Optimizations for Multi-core Server Platforms*. (Intel)

Brinda Ganesh, Ph.D. 2007. *Understanding and Optimizing High-Speed Serial Memory-System Protocols*. (Intel)

Ankush Varma, Ph.D. 2007. *High-Speed Performance, Power, and Thermal Co-Simulation for SoC Design*. (Intel)

Nuengwong (Ohm) Tuaycharoen, Ph.D. 2006. *Disk Design-Space Exploration in Terms of System-Level Performance, Power, and Energy Consumption*. (Dhurakijpundit University, Thailand)

Samuel Rodriguez, Ph.D. 2006. *myCACTI: A New Cache-Design Tool for Pipelined Nanometer Caches*. (AMD)

Aamer Jaleel, Ph.D. 2005. *The Effects of Out-of-Order Execution on the Memory System*. (Intel)

David Tawei Wang, Ph.D. 2005. *Modern DRAM Memory Systems: Performance Analysis and a High Performance, Power-Constrained DRAM-Scheduling Algorithm*. (MetaRAM, a Silicon Valley start-up)

Brian Davis, Ph.D. 2000. *Modern DRAM Architectures*. Davis was a doctoral student at the University of Michigan; I was his thesis co-chair with Trevor Mudge. (Michigan Technological University)

Graduated M.S. Students
(only MS with theses listed)

Dhiraj Reddy Nallapa Yoge, M.S. 2018. *Performance Study of Various Modern DRAM Architectures*.

Jeffrey Scott Smith, M.S. 2006. *Distributed Two-Dimensional Fourier Transforms on DSPs with Applications for Phase Retrieval*. (NASA)

Rami Nasr, M.S. 2005. *FBsim and the Fully Buffered DIMM Memory System Architecture*. (Lutron)

Amol Gole, M.S. 2003. *TERPS: The Embedded Reliable Processing System*. (U.S. Patent Office)

Bharath Iyer, M.S. 2003. *Extended Split-Issue Mechanism in VLIW DSPs to Support SMT and Hardware-ISA Decoupling*. (AMD)

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Nuengwong Tuaycharoen, M.S. 2003. *RTOS-Based Dynamic Voltage Scaling*. (continued as U. Maryland Ph.D. student)

Lei Zong, M.S. 2003. *Nanoprocessors: Configurable Hardware Accelerators for Embedded Systems*. (Army Research Lab)

Brinda Ganesh, M.S. 2002. *Architectural Support for Embedded Operating Systems*. (continued as U. Maryland Ph.D. student)

Aamer Jaleel, M.S. 2002. *In-Line Interrupt Handling and Lockup-Free TLBs*. (continued as U. Maryland Ph.D. student)

Paul Kohout, M.S. 2002. *Hardware Support for Real-Time Operating Systems*. (EVI Technology)

Tiebing Zhang, M.S. 2001. *RTOS Performance and Energy Consumption Analysis Based on an Embedded System Testbed*. (Aeptec Microsystems)

Christopher Collins, M.S. 2000. *Emulation of Embedded Microcontrollers and Real-Time Operating Systems*. (Intel)

Undergraduate Research

Emily Ruppel (2015–2016). *Modeling High-Performance Memory Systems.*

Spencer Black (as part of ENEE 499L, Summer 2008). *High-Resolution Low-Power A/D Conversion on an Electric Guitar*.

Paul Rosenfeld (Summer 2007). *Modeling High-Performance DRAM Systems.*

James Shen (Summer 2007). *Embedded Wireless Networks.*

Brian Davis (as part of the MERIT/ICE program, Summer 2002). *Direct-DRAM-to-DRAM-Access to Support High-Level Data Movement.*

Kevin Ghozati (Summer 2002). *Nanoprocessor Modeling for Real-Time Embedded Systems.*

Sandy Klemm (as part of the MERIT/ICE program, Summer 2002). *Applying Control Theory to Dynamic Voltage Scaling.*

Jeremy Monaldo (Spring/Summer 2002). *Nanoprocessor Modeling for Real-Time Embedded Systems.*

Vincent Chan (as part of ENEE 499, Fall 2001). *Verilog Modeling of Real-Time Embedded Systems.*

David Xia (as part of ENEE 499, Fall 2001). *Verilog Modeling of Real-Time Embedded Systems.*

Lei Zong (as part of ENEE 499, Fall 2001). *Verilog Modeling of Real-Time Embedded Systems.*

Daniel O'Brien (as part of the MERIT/ICE program, Summer 2001). *High-Performance Benchmarks for Real-Time Embedded Systems.*

Lei Zong (as part of the MERIT/ICE program, Summer 2001). *High-Performance Benchmarks for Real-Time Embedded Systems.*

Kathleen Baynes (as part of the MERIT/ICE program, Summer 2000). *Power Modeling of Embedded Systems.*

Christine Smit (as part of the MERIT/ICE program, Summer 2000). *Power Modeling of Embedded Systems.*

Aamer Jaleel (1999–2000). *A Performance Study of Several Virtual Memory Mechanisms.*

Eric Fiterman (Summer 1999). *Microarchitecture-Level Emulation of Real-Time Embedded Systems.*

Ken Powers (Summer 1999). *A Study of DRAM Architectures and Organizations.*

Jiwanjot Tulsi (as part of ENEE 499, Spring 1999). *Design of a Provably Correct Operating System.*

Yun Hua Wang (as part of ENEE 499, Spring 1999). *Design of a Provably Correct Operating System.*

Aamer Jaleel (as part of ENEE 499, Spring 1999). *Design of a Provably Correct Operating System.*

Benjamin Garrett (Fall 1998). *A Speculative Architecture for Handling Precise Interrupts.*

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Benjamin Garrett (as part of ENEE 759M, Spring 1998). *Miss Handling in Software-Managed TLBs.*

Joe Nuzman (as part of ENEE 759M, Spring 1998). *A Simulation of Explicit Multi-Threading.*

High-School Student Research

Rachel Fallon (research intern from River Hill High School, Summer 2016). *Network Design for Supercomputer Memory Systems.*

Kevin Hu (high-school research internship for the Science, Mathematics, and Computer Science program at Poolesville High School, Summer 2016). *Processor Design for High-Performance Memory Systems.*

Demetri Wolfe (high-school research internship for the School Without Walls Senior High School in Washington, DC, Spring 2016). *Building an Electric Guitar out of Cardboard.*

Andrea Ng (high-school research internship for the Magnet Program at Montgomery Blair High School, Summer 2009). *Hardware Validation of Simulators.*

Colin Schmidt (high-school research internship for the Magnet Program at Montgomery Blair High School, Summer 2008). *Validating a DRAM-System Simulator.*

Ben Li (high-school research internship for the Magnet Program at Montgomery Blair High School, Summer 2006). *Performance Modeling of Advanced DRAM Systems.*

E. Advising (non-research)

Undergraduate Cyber Mentoring — United States Naval Academy. The Cyber Science department has a formal advising/mentoring program in which students are assigned to faculty. Currently advise roughly ten Cyber Science undergraduates.

Inventis Mentoring — University of Maryland. The Inventis mentoring program spans the Engineering College; the mentors are selected by the program organizers. Advised roughly a dozen students in this program.

Undergraduate ECE Mentoring — University of Maryland. The ECE department has a formal advising/mentoring program in which students are assigned to faculty; students cannot register for classes without meeting with their faculty advisor. Advised roughly fifteen ECE undergraduates at a time.

F. Education-Related Honors and Awards

Asked to serve as the Moderator of the 9th Annual ECEGSA Academic Careers Panel, an all-day event held November 4, 2016. The discussion topic was "Careers in Academia — Is Academia for Me? and How Do I Get An Academic Job?" Featured Guests included Professor Nicole McFarlane from the University of Tennessee, and Professor Aswin Sankaranarayanan from Carnegie Mellon.

Invited to speak at the *National Student Leadership Conference*, a week-long seminar for high-school students who have shown academic talent. Summer 2008, and again Summer 2009.

Named *Clark School of Engineering Keystone Professor*. One of six professors named to Keystone: The Clark School Academy of Distinguished Professors, 2006.

Received the *Award for Teaching Excellence*, University of Maryland (campus-wide), in recognition of excellence in teaching at the undergraduate level, May 2004.

In February, 2003, The Computer Engineering Handbook (a title to which I contributed the following chapter) was honored as an Outstanding Academic Title for 2002 by *Choice Magazine*, a publication of the American Library Association.

> B. Jacob. "Virtual Memory Systems and TLB Structures." In The Computer Engineering Handbook, pp. 5:55–5:65. V. Oklobdzija, Editor. CRC Press: Boca Raton FL, 2002.

Selections for this honor are made based upon "their excellence in scholarship and presentation, the significance of their contribution to the field, and their value as important — often the first — treatment of their subject."

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General Co-Chair for 5th Workshop on Computer Architecture Education, January 1999.

Received the *George Corcoran Memorial Award*, 1998/9 academic year, "[i]n recognition of teaching and educational leadership at the University of Maryland, College Park campus, effective contribution at the national level, and creative and other scholarly activities related to Electrical and Computer Engineering education."

IV. SERVICE

A. Professional Service

Award/Honors Committees

Member, *ACM/IEEE CS George Michael Memorial HPC Fellowship Committee*, 2018–2020

Editorial Service

Associate Editor, *IEEE Computer Architecture Letters (CAL)*, 2007–2011

Associate Editor, *ACM Transactions on Embedded Computing Systems (TECS)*, 2006–2009

Co-Editor, Special Inaugural Issue of *ACM Transactions on Embedded Computing Systems (TECS)*, vol. 1, no. 1. December 2002

Proposal-Review Panels

Panelist, Department of Energy, July 2018

Panelist, Department of Energy, April–May 2018

Panelist, National Science Foundation, February 2017

Panelist, National Science Foundation, March 2008

Panelist, National Science Foundation, October 2003

Panelist, National Science Foundation, November 2003

Panelist, National Science Foundation, February 2002

Organizing Committees

General Chair, *10th International Symposium on Memory Systems (MEMSYS 2024)*, October 2024

General Chair, 9*th International Symposium on Memory Systems (MEMSYS 2023)*, October 2023

General & Program Chair, 8*th International Symposium on Memory Systems (MEMSYS 2022)*, October 2022 (virtual)

General & Program Chair, 7*th International Symposium on Memory Systems (MEMSYS 2021)*, October 2021 (virtual)

General & Program Chair, 6*th International Symposium on Memory Systems (MEMSYS 2020)*, October 2020 (virtual)

General & Program Chair, *5th International Symposium on Memory Systems (MEMSYS 2019)*, October 2019

General & Program Chair, *4th International Symposium on Memory Systems (MEMSYS 2018)*, October 2018

Organizing Committee Member, *DOE Workshop on Modeling & Simulation of Systems and Applications (ModSim 2018),* August 2018

Moderator/Panel Chair, *2018 Symposia on VLSI Technology and Circuits*, June 2018

General & Program Chair, *3rd International Symposium on Memory Systems (MEMSYS 2017)*, October 2017

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General & Program Chair, *2nd International Symposium on Memory Systems (MEMSYS 2016)*, October 2016

General & Program Chair, *1st International Symposium on Memory Systems (MEMSYS 2015)*, October 2015

Panel Discussion Coordinator: *Memory Systems — What's the Real Problem? What's the Next Solution?* Held at the *Workshop on Memory System Performance and Correctness (MSPC 2008)*, March 2008

Session Chair, *13th International Symposium on High-Performance Computer Architecture (HPCA 2007)*, February 2007

Session Chair, *International Symposium on Low Power Electronics and Design (ISLPED 2006)*, October 2006

Workshops Chair, *8th International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2005)*, September 2005

Local Arrangements Chair, *7th International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2004)*, November 2004

Coordination Vice-Chair, *5th International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2002)*, November 2002

Publicity Chair, *2nd Workshop on Compiler and Architecture Support for Embedded Systems (CASES 1999)*, October 1999

General Co-Chair, *5th Workshop on Computer Architecture Education (WCAE 1999)*, January 1999

Local Arrangements Chair, *3rd IEEE Symposium on High-Assurance Systems Engineering (HASE 1998)*, November 1998

Program Committees

Program Committee Member, *The 48th International Symposium on Computer Architecture (ISCA 2021)*, May 2021

Program Committee Member, *The 27th International Symposium on High-Performance Computer Architecture (HPCA-27)*, February 2021

Program Committee Member, *The 45th International Symposium on Computer Architecture (ISCA 2018)*, June 2018

Program Committee Member, *Supercomputing — Architectures & Networks (SC17)*, November 2017

Program Committee Member, *14th International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2011)*, October 2011

Program Committee Member, *43rd International Symposium on Microarchitecture (MICRO 2010)*, December 2010

Program Committee Member, *13th International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2010)*, October 2010

Program Committee Member, *41st International Symposium on Microarchitecture (MICRO 2008)*, November 2008

Program Committee Member, *11th International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2008)*, November 2008

Program Committee Member, *International Conference on Computer Design (ICCD 2008)*, October 2008

Program Committee Member, *Workshop on Memory System Performance and Correctness (MSPC 2008)*, March 2008

Program Committee Member, *13th International Symposium on High-Performance Computer Architecture (HPCA 2007)*, February 2007

Program Committee Member, *39th International Symposium on Microarchitecture (MICRO 2006)*, December 2006

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Program Committee Member, *9th International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2006)*, October 2006

Program Committee Member, *International Conference on Computer Design (ICCD 2006)*, October 2006

Program Committee Member, *8th International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2005)*, September 2005

Program Committee Member, *Memory Systems Performance Workshop (MSP 2005)*, June 2005

Program Committee Member, *7th International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2004)*, November 2004

Program Committee Member, *6th International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2003)*, November 2003

Program Committee Member, *4th International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2001),* November 2001

Program Committee Member, *Workshop on Memory Performance Issues,* June 2001

Program Committee Member, *4th IEEE Symposium on High-Assurance Systems Engineering (HASE 1999),* November 1999

General Reviewing

Reviewer for papers in the following journals:

IEEE Transactions on Computers
IEEE Transactions on Parallel and Distributed Systems
IEEE Transactions on Very Large Scale Integration Systems
IEEE Computer
ACM Transactions on Embedded Computing Systems
ACM Transactions on Architecture and Code Optimization
ACM Computing Surveys
IBM Journal of Research and Development
The Computer Journal

Reviewer for papers in the following annual meetings:

ACM/IEEE International Symposium on Computer Architecture (ISCA)
ACM/IEEE International Symposium on Microarchitecture (MICRO)
ACM International Conference on Supercomputing (ICS)
IEEE International Symposium on High-Performance Computer Architecture (HPCA)
IEEE International Symposium on High-Assurance Systems Engineering (HASE)
IEEE International Conference on Computer Design (ICCD)
Int'l Conf. on Compilers, Architectures, and Synthesis for Embedded Systems (CASES)
Workshop on Computer Architecture Education (WCAE)

B. University Service at the Naval Academy

2023–present Chair, Cyber Science Faculty-Search Committee

C. University Service at Maryland

Departmental

Winter 2020 Speaker at the ECE Department's TA Teaching and Development (TATD) event

Fall 2018 Member, ECE APT Committee

Spring 2017 Keynote speaker at the ECE Department's TA Teaching and Development Fellowship event

Spring 2017 Member, ECE Faculty Search Sub-Committee for Computer Engineering

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Fall 2016	Member, ECE Faculty Search Committee for Microelectronics
Fall 2016	Served as the Moderator of the 9th Annual ECEGSA Academic Careers Panel, an all-day event held November 4, 2016
Fall 2016	Invited by ECEGSA to speak to the ECE Department's graduate students on how to give a good research presentation
2015–2016	Developed from scratch and taught *ENEE 447: Operating Systems* at Dept. Chair's request, to improve the Computer Engineering program
2015–2017	Member, ECE Faculty Search Committee
2014–2015	Brought in to teach and overhaul the laboratories of *ENEE 245: Digital Circuits & Systems Lab* at Dept. Chair's request, to improve the Computer Engineering program
2013–2014	Chair, ECE Promotion and Tenure Subcommittee
2013–2016	Member, ECE Promotion and Tenure Committee
2007–2010	Director, Computer Engineering Program — first faculty to hold the position; charged by Dept. Chair to overhaul the curriculum (in particular, improve the curriculum's consistency across topics), increase the program's external visibility, and increase enrollment; all tasks completed successfully before sabbatical in 2010
2006–2011	Member, ECE PhD Qualifying Exam Committee
2006–2007	Prepared accreditation materials for Middle States Commission on Higher Education
2005–2007	Member, ECE Faculty Search Committee
2005–2006	Prepared materials for ABET accreditation process
Spring 2005	ECE search committee for *Chairperson of the ECE Department*
2004–2007	Member, ECE Promotion and Tenure Committee
Spring 2004	ECE search committee for *Director of Computing Facilities* position
2002–2004	Member, ECE Department Council
Spring 2001	ECE search committee for *Chairperson of the ECE Department*
2000–2002	Member, ECE Facilities and Services Committee
1999–2000	Member, ECE Undergraduate Affairs Committee
1998–1999	Chair, ECE Undergraduate Affairs Committee
1998–2000	Organized the weekly *Research in Computer Engineering Colloquium*
1998–2000	Member, ECE General Academic Affairs Committee
1998–2000	Member, ECE Curriculum Revision Committee
1998–2000	Computer Engineering representative for ABET transition
Spring 1998	ECE search committee for Personnel and *Research Coordinator* position
Spring 1998	ECE search committee for *Systems Analyst* position
1997–1998	Organized a weekly Microarchitecture Seminar Series

College

2005–2008	Member, Engineering College Promotion and Tenure Committee
2004–2005	Member, Dean's committee formed to review and revise the college-wide *ENES 100 — Introduction to Engineering Design*

1999–2001	Member, ECE College of Engineering Council

University

Fall 2018	Invited to present Tech+Music seminar to Technica/Hackathon
Winter 2017	Guest speaker at *Foundations of Entrepreneurship & Innovation (HEIP143)* course
Fall 2017	Invited to present Innovation & Design seminar to Mtech Startup Hours/Shell Talk
2017–2019	Faculty consultant for the EIP/NIST Technology Market Assessment (T-Map) Project
2006–2007	ECE representative/member of CS Department Curriculum Review Committee
1999–2003	Faculty advisor for university chapter of Eta Kappa Nu (EE Honor Society)

➡ The Maryland chapter received the Certificate of Merit from the national Eta Kappa Nu Association for Outstanding Chapter Activities, 1999–2000 academic year. The two other chapters receiving the same award were from Carnegie Mellon and MIT.

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V. RESEARCH, TESTIMONY, AND DEPOSITION AS EXPERT WITNESS

Dr. Jacob has written numerous expert reports, has testified in court, has been deposed, has performed prior-art searches, has done claims construction and patent-validity analysis. He has worked on roughly fifty cases in the past twenty-five years and has worked for most semiconductor memory manufacturers, many systems manufacturers, and several general semiconductor manufacturers. He has served on the side of the plaintiff/complainant/petitioner as well as on the side of the defendant/respondent/patent owner.

He is a leading expert in memory systems and has served as a testifying expert in that and related fields.

The following are his appearances at trial and deposition (out of respect for client confidentiality and protective orders, only publicly available information is provided here):

U.S. Patent and Trademark Office Inter Partes Review No. IPR2023-01286, February 2023–present
Provided technical opinions to Patent Owner and performed validity analysis regarding output buffers/drivers in semiconductor devices.

Deposition of August 20, 2024

U.S. Patent and Trademark Office Inter Partes Review No. IPR2023-01200, February 2023–present
Provided technical opinions to Patent Owner and performed validity analysis regarding synchronous interfaces in semiconductor memory devices.

Deposition of June 27, 2024

U.S. Patent and Trademark Office Inter Partes Review No. IPR2023-01230, February 2023–present
Provided technical opinions to Patent Owner and performed validity analysis regarding voltage-boosting circuitry in semiconductor memory devices.

Deposition of June 21, 2024

U.S. District Court for the Western District of Texas, Case No. 6:20-cv-00636-ADA, June 2023–February 2024
Provided technical opinions to Plaintiff, and generated performance analyses, on the relationship between transistor delay and memory performance in DRAM products.

Trial testimony of February 13, 2024
Deposition of November 8, 2023

U.S. District Court for the Central District of California, Case No. 8:23-cv-00039-JWH-DFM, February 2023–present
Provided technical opinions to Plaintiff on claim-term constructions regarding memory arrays and devices, and their I/O subsystems both volatile and non-volatile, planar and 3D.

(Markman) Deposition of January 3, 2024

U.S. Patent and Trademark Office Inter Partes Review No. IPR2021-01064, March 2022
Petitioner submitted a public declaration of mine from a previous case, to institute the IPR, and I agreed to a deposition to defend the analysis in the declaration.

Deposition of March 31, 2022

U.S. District Court for the Western District of Texas, Case No. 6:20-cv-501-ADA, July 2020–February 2021
Provided technical opinions to Plaintiff on claim-term constructions, and performed technical analysis regarding the management of flash-based memory arrays and devices, the design of flash translation layers (FTLs), and the internals of solid-state drives (SSDs).

(Markman) Deposition of February 8, 2021

U.S. Patent and Trademark Office Inter Partes Review No. IPR2020-00533, July 2019–November 2020
Provided technical opinions to Petitioner, performed prior-art search, helped with legal strategy, and performed detailed validity analysis regarding processor-cache hierarchies and memory-coherence protocols within them.

Deposition of November 2, 2020

U.S. Patent and Trademark Office Inter Partes Review No. IPR2019-00104, June 2018–November 2019
Provided technical opinions to Petitioner, performed prior-art search, helped with legal strategy, and performed detailed validity analysis regarding voltage boosting circuits.

Deposition of November 21, 2019

U.S. Patent and Trademark Office Inter Partes Review No. IPR2019-00102, June 2018–November 2019
Provided technical opinions to Petitioner, performed prior-art search, helped with legal strategy, and performed detailed validity analysis regarding memory-array sense amplifier design.

Deposition of November 21, 2019

U.S. Patent and Trademark Office Inter Partes Review No. IPR2018-01794, June 2018–November 2019
Provided technical opinions to Petitioner, performed prior-art search, helped with legal strategy, and performed detailed validity analysis regarding leakage techniques for memory arrays.

Deposition of November 20, 2019

U.S. Patent and Trademark Office Inter Partes Review No. IPR2018-01784, June 2018–November 2019
Provided technical opinions to Petitioner, performed prior-art search, helped with legal strategy, and performed detailed validity analysis regarding memory-array sense amplifier design.

Deposition of November 20, 2019

U.S. International Trade Commission Investigation No. 337-TA-1097, October 2017–April 2019
Provided technical opinions to Complainants, helped with legal strategy, and performed detailed schematics- and firmware-based infringement analysis on SSD and stacked memory architectures.

Deposition of December 17 and 18, 2018

U.S. Patent and Trademark Office Inter Partes Review No. IPR2017-00381, September 2016–January 2018
Provided technical opinions to Petitioner, performed prior-art search, helped with legal strategy, and performed detailed validity analysis regarding memory-system and memory-device signaling interfaces.

Deposition of January 23, 2018
Deposition of September 11, 2017

U.S. Patent and Trademark Office Inter Partes Review No. IPR2015-01068, January 2015–April 2016
Provided technical opinions to Petitioner, helped with legal strategy, and performed detailed, schematics-based non-infringement and validity analysis regarding memory-system and memory-device signaling interfaces.

Deposition of January 7, 2016

U.S. International Trade Commission Investigation No. 337-TA-941, January 2015–August 2015
Provided technical opinions to Respondents, helped with legal strategy, and performed detailed, schematics-based non-infringement and validity analysis regarding memory-system and memory-device signaling interfaces.

Trial testimony of August 20, 2015
Deposition of July 2, 2015

U.S. International Trade Commission Investigation No. 337-TA-909, April 2014–October 2014
Provided technical opinions to Complainants, helped with legal strategy, and performed detailed, schematics-based infringement analysis on NOR and NROM flash-device architectures.

Trial testimony of October 21, 22, and 27, 2014
Deposition of September 5, 2014

U.S. International Trade Commission Investigation No. 337-TA-803, November 2011–September 2012
Provided technical opinions to Respondents, helped with legal strategy, and performed research on prior art regarding memory-system and memory-device architectures.

Deposition of June 7, 2012
Markman-Hearing testimony of April 17, 2012
(Markman) Deposition of April 9, 2012

U.S. International Trade Commission Investigation No. 337-TA-753, March 2011–October 2011

Provided technical opinions to Respondents, helped with legal strategy, and performed research on prior art regarding high-speed memory-system architectures.

Trial testimony of October 14, 2011
Deposition of August 23 and 24, 2011

Rambus vs. Nanya USA, May 2007–March 2008

Provided technical opinions to Nanya USA regarding DDR2 SDRAM interfaces and alternative technologies.

Deposition of October 26, 2007

U.S. Federal Trade Commission vs. Rambus, Docket No. 9302, July 2002–July 2003

Provided technical opinions to the FTC regarding SDRAM interfaces, Rambus intellectual property, infringement of Rambus patents, and alternative technologies.

Trial testimony of June 16 and 17, 2003
Deposition of March 19, 2003