
BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAP AMERICA, INC.,
Petitioner

v.

VALTRUS INNOVATIONS LTD.,
Patent Owner

Case No. IPR2025-00418
Patent No. 6,871,264

**PATENT OWNER'S BRIEF THAT INSTITUTION OF THE PETITION
SHOULD BE DENIED ON DISCRETIONARY GROUNDS**

PATENT OWNER’S EXHIBIT LIST

No.	Exhibit Description
2001	Memorandum for Interim Processes for PTAB Workload Management, dated March 26, 2025
2002	Joint Claim Construction and Prehearing Statement in <i>Valtrus Innovations Ltd. v. SAP America, Inc.</i> , No. 2:24-cv-00021-JRG, Dkt. No. 96 (E.D. Tex. Dec. 20, 2024)
2003	Joint Claim Construction Chart in <i>Valtrus Innovations Ltd. v. SAP America, Inc.</i> , No. 2:24-cv-00021-JRG, Dkt. No. 123 (E.D. Tex. Feb. 28, 2025)
2004	Opening Claim Construction Brief in <i>Valtrus Innovations Ltd. v. SAP America, Inc.</i> , No. 2:24-cv-00021-JRG, Dkt. No. 110 (E.D. Tex. Jan. 31, 2025)
2005	Responsive Claim Construction Brief in <i>Valtrus Innovations Ltd. v. SAP America, Inc.</i> , No. 2:24-cv-00021-JRG, Dkt. No. 117 (E.D. Tex. Feb. 14, 2025)
2006	Reply Claim Construction Brief in <i>Valtrus Innovations Ltd. v. SAP America, Inc.</i> , No. 2:24-cv-00021-JRG, Dkt. No. 118 (E.D. Tex. Feb. 21, 2025)
2007	Order in <i>Valtrus Innovations Ltd. v. SAP America, Inc. et al.</i> , No. 2:24-cv-00021-JRG, Dkt. No. 146 (E.D. Tex. Apr. 26, 2025)

Pursuant to the Memorandum titled “*Interim Processes for PTAB Workload Management*,” dated March 26, 2025 (“the Interim Processes Memo”; EX2001) and the Notice Extending Deadline for Discretion Briefing (Paper 6), Patent Owner respectfully submits this brief explaining why the Director, in consultation with a Board panel, should exercise her discretion to deny institution of Petitioner’s Petition for *Inter Partes* Review (Paper 1).

In the Interim Processes Memo, the Director identified several considerations, including, among others, “[t]he strength of the unpatentability challenge,” “[t]he extent of the petition’s reliance on expert testimony,” “[s]ettled expectations of the parties, such as the length of time the claims have been in force,” and “[a]ny other considerations bearing on the Director’s discretion.” EX2001, 2-3.¹ In accordance with the memo, the Director will also consider “its statutory deadlines for AIA proceedings, and other workload needs.” EX2001, 3.

Against this backdrop, Patent Owner submits that discretionary denial is warranted.

¹ With the exception of any patents (cited by column and line number) and the expert declaration (cited by paragraph number), Patent Owner uses the exhibit page numbering in the lower righthand corner of the Exhibits.

First, the '264 Patent was filed on March 6, 2002, issued on March 22, 2005, and expired on September 16, 2022. EX1001, Cover Page. It was in full force for its entire term (20 years, 194 days). All maintenance fees were timely paid (including those paid prior to the enactment of the America Invents Act that created *inter partes* reviews). Although Patent Owner appreciates that pre-AIA patents are not, as a matter of law, immune from *inter partes* review proceedings, Patent Owner respectfully submits that the Director should exercise her discretion under the circumstances, based on the settled expectations of when the '264 Patent was filed (in 2002) and that the '264 Patent already ran its full term. Nonetheless, as the Supreme Court has stated, “[e]lementary considerations of fairness dictate that individuals should have an opportunity to know what the law is and to conform their conduct accordingly; settled expectations should not be lightly disrupted.” *Landgraf v. USI Film Prods.*, 511 U.S. 244, 265 (1994). That is why “[r]etroactivity is not favored by the law” and “congressional enactments and administrative rules will not be construed to have retroactive effect unless their language requires this result.” *Bowen v. Georgetown Univ. Hosp.*, 488 U.S. 204, 208 (1988). This is particularly so for patents, where “fundamental alterations ... risk destroying the legitimate expectations of inventors in their property.” *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 535 U.S. 722, 739 (2002). Here, those settled expectations—

especially when considered in view of the circumstances discussed below and the Board's finite resources—counsel toward discretionary denial.

Second, Patent Owner is no longer asserting the '264 Patent against Petitioner in the underlying district court action, having recently dismissed with prejudice its claims pertaining to the patent. EX2007, 1. Thus, Patent Owner is not (and cannot in the future) assert this patent against Petitioner. Patent Owner also is not asserting the '264 Patent in any other case. Patent Owner respectfully submits that it is not worth the Board's finite resources to address a 13,946-word Petition (with an accompanying 221-page expert declaration that the Petition extensively relies upon throughout its Grounds), filed three days before Petitioner's 35 U.S.C. §315(b) one-year bar, over an expired patent, when Petitioner no longer faces any risk of the patent being asserted against it. Indeed, if this IPR Petition is instituted, by the time of any final written decision (which would be due August 27, 2026), the '264 Patent will have been expired for nearly four years (3 years, 11 months, 11 days to be exact).

Third, although the district court case no longer involves the '264 Patent, Petitioner previously took inconsistent positions in district court and in its IPR Petition, which hobbles its merits position. For example, prior to filing the Petition, Petitioner argued in the district court action that the term “high-speed interconnect coupling” in independent claim 1 is indefinite. EX2002, 25; *see also* EX2003, 6. Petitioner continued this argument in its claim construction briefing (without any

expert reliance), EX2005, 22-26, to which Patent Owner disagreed, EX2004, 32-34; EX2006, 12.² However, in the IPR Petition, Petitioner argues (as does its expert) the *opposite*, contending that the term has a “plain and ordinary meaning”: “Because a POSITA would find the challenged claims unpatentable under any interpretation consistent with their plain and ordinary meaning in the context of the ’264 Patent, the Board need not expressly construe the claim terms.” Petition (Paper 1), 17. Neither Petitioner, nor its expert, mentions or attempts to reconcile these contradictory positions, when applying the prior art to the challenged claims. *See* Petition (Paper 1), 25, 30-33; EX1005 ¶¶96-98.³ Nor do they actually explain what constitutes the “plain and ordinary meaning” of a “high-speed interconnect coupling.” *See* Petition (Paper 1), 25, 30-33; EX1005 ¶¶95-98.

Petitioner’s omissions are significant. For example, Petitioner asserts that “as depicted in Figure 4 [of the *Cherabuddi* reference], a POSITA would understand

² For the parties’ claim construction briefing, Patent Owner again cites to the exhibit page numbering (*e.g.*, exhibit page number 22 corresponds to labeled page 16 of the brief in EX2005).

³ Petitioner also ignores the constructions it agreed to for certain claim terms in the district court, EX2003, 5, failing in its Petition to address or explain how they are met in the prior art.

that ‘*a high-speed interconnect*’ is shown based on the wires that connect the first cache controller 42a and the second cache controller 42b to the cache memory partition 23a and the cache memory partition 23b, respectively over the cache access circuit 22.” Petition (Paper 1), 31 (emphasis in original & citing EX1005 ¶¶95, 29; EX1002, Fig. 4, 3:40-42).

However, neither Paragraph 95 nor Paragraph 29 of the expert declaration (EX1005) provides any analysis as to what constitutes a “high-speed interconnect” (or “high-speed interconnect coupling”). Paragraph 95 simply refers back to the expert’s “Technical Background” section, and states “on a cache miss, data is fetched and transmitted back to the cache,” which “is done over wires.” EX1005 ¶95. Paragraph 29 (part of the “Technical Background” section) describes a cache but contains no explanation as to how that may apply to a “high-speed interconnect,” “high-speed interconnect coupling,” or “a POSITA’s understanding” of the terms (as the Petition alleges). Paragraph 29 recites, in full:

A cache is a relatively small memory structure that holds copies of data, whether that data is a set of instructions to perform, or the numbers (data) on which the instructions operate. This leads to caches specialized for holding instructions (“instruction caches” or “i-caches”) and those specialized for holding data (“data caches” or “d-caches”). Caches of both types are connected to processor cores across busses, which are groups of wires that carry the requests and also carry the data involved in

those requests. One can see, for example, in the illustration above from Hammond, the dark black lines connecting the various caches to the CPUs, and to the right is an indication that those black wires make up the “system bus” of the single-chip microprocessor. Each of those wires is a bus that carries data between the caches and the processor cores, and each is a separate segment of the larger “system bus” connecting the caches and processor cores of the chip.

EX1005 ¶29.

The Petition also points to Paragraph 90 of the expert declaration (EX1005), asserting that: “Figure 4 also depicts a dynamically allocated cache memory 23 (dynamically allocable cache unit) and a high-speed interconnect, as shown in claim [1.4].” Petition (Paper 1), 25 (citing EX1002, 3:2-5 & EX1005 ¶90). But Paragraph 90 of the expert declaration is simply a block quote from a different portion of *Cherabuddi* (EX1002, 4:66-5:14), without any independent analysis or explanation:

Cherabuddi describes this as follows:

FIG. 4 shows an MPU 40 that is one embodiment of MPU 20, and includes CPUs 21a-21b, cache access circuit 22, and cache memory partitions 23a-23b. *Each CPU 21 is shown to include a CPU core 41 and a cache controller 42. Each cache controller 42, which may be of conventional architecture, transfers address and*

data between its associated CPU core 41 and cache access

circuit 22, and includes (or is associated with) a memory element 43.

Memory element 43 may be any suitable memory device including, for example, a register or memory cell. Although shown in FIG. 4 as being internal to cache controller 42, memory element 43 may be external to cache controller 42. CPU core 41 includes other well-known elements of CPU 21 including, for instance, L1 cache memory, instruction units, fetch and decode units, execution units, register files, write cache(s), and so on. [Cherabuddi, 4:66–5:14, emphasis added]

EX1005 ¶90.

Nor does Petitioner’s expert, in his “high-speed interconnect” limitation discussion, explain what a “high-speed interconnect” or “high-speed interconnect coupling” is, or what makes it qualify as such. EX1005 ¶¶95-98. Instead, Petitioner’s expert concludes, without explanation, that the green highlighting in his annotated figure corresponds to the “high-speed interconnect.” EX1005 ¶¶96-98. In his concluding paragraph (Paragraph 98) for the limitation, Petitioner’s expert asserts that:

Cherabuddi’s description above confirms the understanding that, in the preceding figure, the high-speed interconnect is highlighted in green. In the figure is shown the wires that directly connect the plurality of cache memory blocks to the first and second cache controllers. The figure illustrates, and the text explains, that the high-speed interconnect couples the cache memory blocks to the cache controllers via MUXes such that both controllers have access to all of the cache memory

blocks, depending on the address comparisons that drive the MUX select signals.

EX1005 ¶98.

An examination of the expert’s “Cherabuddi’s description above” reveals it is an extended block quote from *Cherabuddi*, EX1005 ¶97, and provides *no* analysis or explanation as to a POSITA’s alleged understanding of the reference or claim.

Having argued in district court that the “high-speed interconnect coupling” limitation is indefinite, and provided in the IPR Petition no actual analysis or explanation as how *Cherabuddi* meets the claim limitations under its unexplained “plain and ordinary meaning,” Petitioner has failed to show a reasonable likelihood of prevailing. *See Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9, 15-16 (PTAB Aug. 24, 2022) (precedential) (denying institution where petitioner’s expert did not provide any supporting evidence or technical reasoning). Regardless, the inconsistent positions cannot be reconciled and counsel toward discretionary denial. *C.f. Cambridge Mobile Telematics, Inc. v. Sfara, Inc.*, IPR2024-00952, Paper 12, 6-9 (PTAB Dec. 13, 2024) (informative as to the majority) (denying institution where petitioner asserted in district court a term was means-plus-function but plain and ordinary meaning in its IPR petition).

In sum, with Petitioner having failed to address its district-court claim construction positions—or inform the Board of the same—Patent Owner

respectfully submits that discretionary denial is warranted for this additional reason. There is simply no reason for the Board to expend resources to address these inconsistent positions over an expired patent that is not being asserted (and will not be asserted in the future) against Petitioner.

Accordingly, for the reasons explained above, Patent Owner respectfully submits that the Director should exercise her discretion to deny the Petition.

Dated: May 9, 2025

Respectfully submitted,

/Patrick Colsher/

Patrick Colsher (Reg. No. 74,955)
Counsel for Patent Owner

CERTIFICATE OF COMPLIANCE

I hereby certify that this paper complies with the type-volume limitation of 37 C.F.R. §42.24 and the Interim Processes Memo (as determined by the Microsoft Word word-processing system used to prepare this paper) because it contains 1706 words, excluding the parts of the paper exempted by 37 C.F.R. §42.24(a).

Dated: May 9, 2025

Respectfully submitted,

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Counsel for Patent Owner

CERTIFICATE OF SERVICE

I hereby certify that the foregoing Patent Owner's Brief that Institution of the Petition Should be Denied on Discretionary Grounds and Exhibits listed on the List of Exhibits were served on May 9, 2025, via electronic mail upon counsel of record for Petitioner at the following email addresses:

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