

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

**Valtrus Innovations Ltd. and
Key Patent Innovations Ltd.,**

Plaintiffs

v.

SAP America, Inc. and SAP, SE.

Defendants.

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CIVIL ACTION NO. 2:24-CV-00021-JRG

JURY TRIAL DEMANDED

**PLAINTIFFS VALTRUS INNOVATIONS LTD. AND
KEY PATENT INNOVATIONS LTD.'S
REPLY CLAIM CONSTRUCTION BRIEF**

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I. INTRODUCTION

SAP has failed to meet its burden to show indefiniteness by clear and convincing evidence, and to show a “clear and unmistakable” disclaimer during prosecution of the ’244 patent. As it concerns indefiniteness, SAP largely relies on attorney argument, without any evidentiary or even specification support, and mostly ignores the intrinsic evidence as a whole and undisputed testimony from Valtrus’s experts.¹ As it concerns the prosecution history disclaimer of the ’244 patent, SAP has the argument and the background facts wrong—the Utter reference at issue did *not* disclose messages passing *through* a fault tolerant storage system, just the messages passing *over* Ethernet. Moreover, the applicant never said anything about the “Internet”; SAP simply includes it in the alleged disavowal, notwithstanding the fact that neither the applicant nor the Examiner ever mentioned it. SAP’s positions should be rejected.

II. ARGUMENT

A. Disputed Terms of U.S. Patent No. 7,936,738

1. “potentially inaccurate or incomplete” (claim 10)

SAP’s argument ignores the context of the claim language around “potentially inaccurate or incomplete.” Claim 10 does not require drawing a line between, on the one hand, context information that is *definitely* inaccurate or incomplete, and, on the other hand, context information that is *potentially* inaccurate or incomplete. Rather, the claim just requires adding an indication to the message according to whatever determination is made. All that matters is that the user determined that the context information is “potentially inaccurate or incomplete” (regardless of whether that determination was correct) and added an indication to that effect. *See* Pl. Opening Claim Construction Br., Dkt. 110 (“Op. Br.”) at 6. There is nothing indefinite about this type of

¹ Errata to the depositions of Valtrus’s Experts are attached hereto as Exhibits 23 and 24.

limitation. *SB IP Holdings, LLC v. Vivint Smart Home, Inc.*, Case No. 4:20-CV-886, 2021 WL 5804286, at *19 (E.D. Tex. Dec. 7, 2021) (“irregular activity” not indefinite because “it is irrelevant what criteria are used...what matters is that some criteria are used to categorize an activity and then some action is taken.”).

B. Disputed Terms of U.S. Patent No. 6,889,244

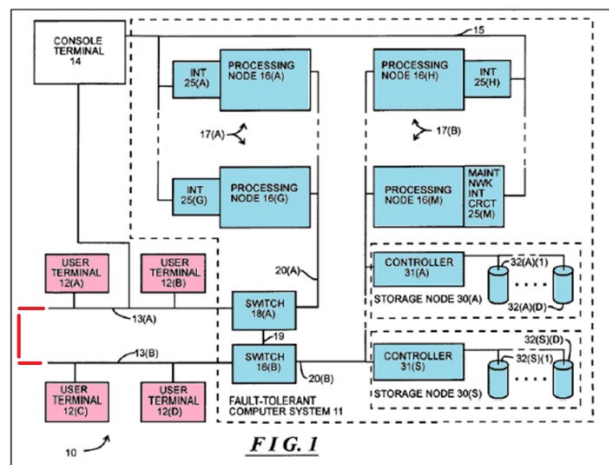
1. “the first and second nodes are each coupled to a fault tolerant storage system (FTSS)”

SAP’s disavowal argument is based on an exchange that the applicant had with the Examiner during prosecution concerning an anticipation rejection over the Utter reference. Per SAP, “a message from one user terminal to two of the other user terminals [in Utter] necessarily requires the message to pass through the FTSS as there is no path between these terminals which do not go through the FTSS.” Def. Resp. Claim Construction Br., Dkt. 117 (“Resp. Br.”) at 3. Based on this, SAP concludes that the applicant’s argument to the contrary must have disclaimed Ethernet (and by some implied extension, the Internet). But SAP’s entire premise is wrong.

First, prosecution history disclaimer applies only when an applicant’s statements constitute “a clear and unmistakable surrender of subject matter.” *Ecolab, Inc. v. FMC Corp.*, 569 F.3d 1335, 1342 (Fed. Cir. 2009). Here, there was no “clear and unmistakable surrender” because the applicant never stated anything about passing a message from “terminal 12(A) to 12(C) or 12(D)” as SAP asserts. Resp. Br. at 3. Instead, all the applicant argued was that, when two nodes (such as Terminals 12A and 12B) are connected directly via an ethernet connection (such as 13(A)), there was no reason for the Examiner to conclude that a message between them would necessarily go through Utter’s “Fault-tolerant Computer System.” SAP’s contrary interpretation ignores the applicant’s repeated and clear statements. *See, e.g.*, Op. Br. Ex. 18 at 43 (applicant arguing that there is “no indication whatsoever” that Utter’s terminals communicate

“through the FTSS”); *Id.* at 20 (applicant arguing that it “cannot find a single teaching” in Utter of messages passed from “a first user terminal through the fault-tolerant computer system to a second user terminal”). As the applicant argued, Utter disclosed passing a message *over* Ethernet, but the claims required the message to also go *through* the FTSS, which Utter did not disclose. *See* Op. Br. at 11. This was the applicant’s point, and all of the cited passages are consistent with that explanation.

Moreover, SAP’s reading of Utter is wrong. Figure 1 of Utter shows ethernet networks 13(A) and 13(B) extending out to the left of the diagram, suggesting that a message could pass from 12(A) to 12(C) via a connection located elsewhere, as annotated in red on the left side of the figure.² This tracks the applicant’s repeated explanation that passing a message over a standard Ethernet connection was not, by itself, the same as passing a message through an FTSS. *See, e.g.,* Op. Br. Ex. 18 at 20, 43.



Op. Br. at 10 (annotation added).

Further, SAP has no basis to assert that the applicant also intended to disclaim the Internet as a means of connecting the nodes and the FTSS. If the applicant intended a disavowal of this

² Moreover, Utter labels Storage Nodes 30 separately from the Fault-Tolerant Computer System 11.

magnitude that is so divorced from the actual claim language (as SAP suggests), then the applicant would have likely said as much, and the Examiner would have likely noted it in reasons for withdrawing the rejection. Nothing of this sort exists in the record (for good reason—there was no disavowal of any “coupling” between the nodes and the FTSS, Ethernet, Internet or, for that matter, “store and forward”).

2. “highly reliable fault-tolerant storage media” (claim 1, 2, 3, 6, 9, 10)

“[H]ighly reliable fault tolerant storage media” is not indefinite. SAP attempts to inject ambiguity where there is none: claim 1 recites “A method of transmitting messages between a first node and a second node, wherein the first and second nodes are each coupled to **a fault tolerant storage system (FTSS)**, the method comprising . . . storing the message in a data structure in **highly reliable fault-tolerant storage media of the FTSS.**” “[H]ighly reliable fault-tolerant storage media” thus plainly refers to the storage media of the FTSS. This is further reflected in the prosecution history, which shows that the applicant and Examiner both understood the FTSS to also be highly reliable. For example, the applicant distinguished the prior art because claim 1 required messages to be “stored in highly reliable FTSS data storage.” Op. Br. Ex. 18 at 44. And the Examiner’s Notice of Allowance states specifically that “message storage within a **highly reliable fault-tolerant storage system**...was not suitably taught or suggested by the prior art of record.” Op. Br. Ex. 18 at 68; *see also Tinnus Enterprises, LLC v. Telebrands Corp.*, 733 F. App’x 1011, 1020 (Fed. Cir. 2018) (“The examiner’s own remarks confirm that the claim language informs a person of ordinary skill of the objective boundaries of the claim term.”).

Dr. Farach-Colton explained at length how “highly reliable fault tolerant” would have been readily understood by a POSITA given its common usage in the prior art. *See* Op. Br. at 12; *id.* Ex. 15, ¶¶ 66-73. Highly reliable and fault tolerant are used “to generally describe systems with additional indications or guarantees of reliability beyond non-redundant, single point of

failure systems.” *Id.* Ex. 15, ¶¶ 69. While “individual pieces of the media” are not necessarily fault tolerant by themselves, when “[y]ou take storage media and you combine it using a set of techniques that make it fault tolerant...a POSITA would classify that as highly reliable and fault tolerant.” Resp. Br. Ex. B at 37:13; 36:6-12.³ This is because “fault tolerant is one kind of...high reliability.” *Id.* Ex. B at 42:16. The specification is replete with descriptions of “highly reliable fault tolerant” and gives a specific example for an FTSS—the SureStore(R) XP512. *See* Op. Br. Ex. 17 at 6:50-67.

Accordingly, SAP’s cited case, *In re Taasera Licensing LLC, Pat. Litig.*, is inapposite. Case No. 2:22-MD-03042-JRG, 2023 WL 8628323, at *19–20 (E.D. Tex. Dec. 13, 2023) (“substantially real-time” indefinite where expert testimony regarding the term was merely conclusory and no examples of “substantially real-time” were given in the specification to explain its scope). Same, too, with the laundry list of “term of degree” cases SAP cites where the intrinsic and extrinsic evidence failed to give sufficient context. None of SAP’s cited cases found indefiniteness where, as here for “highly reliable fault-tolerant storage media,” the intrinsic evidence and un rebutted expert testimony gave clear examples of how a POSITA would understand the disputed term.

Lastly, SAP argues (without citation to any case law) that the term is indefinite because “highly reliable” could be considered superfluous in the term “highly reliable fault tolerant.” Resp. Br. at 9. But even if it is superfluous, the presence or lack of superfluous terms is not the standard for definiteness, which requires merely that “a patent’s claims, viewed in light of the specification and prosecution history, inform those skilled in the art about the scope of the

³ *See also* Resp Br. Ex. B at 50:16-20 (“It is tautological to say that a fault tolerant storage system would have fault tolerant storage media because the meaning of fault tolerant storage media is the media used in a fault tolerant storage system.”).

invention with reasonable certainty.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 910 (2014); *see also Uniloc 2017 LLC v. Apple Inc.*, 843 F. App'x 305, 312 (Fed. Cir. 2021) (“The preference for giving meaning to all terms is not an inflexible rule that supersedes all other principles of claim construction.”) (quotation omitted). Because “highly reliable fault tolerant storage media” would be understood by a POSITA, the term is not indefinite.

3. “accessing determining which nodes should receive the broadcast message based on the broadcast message” (Claim 10)

SAP admits that there is a clear language error such that “accessing determining” is nonsensical, as well as that, as Valtrus described in its opening brief, the court need look only at the structurally parallel claims 6 and 10 and their underlying messaging paradigms. *See* Resp. Br. at 10. But SAP nevertheless argues that “accessing” cannot be deleted because it is possible that the claim was meant to require “accessing a list of recipients.” *Id.* at 11. SAP’s hypothetical contradicts the specification. The entire discussion of the unsolicited messaging paradigm never once references accessing any list of recipients, and the only use of the verb “accessing” is in “the client can access unsolicited message manager 142 to retrieve any relevant unsolicited messages.” Op. Br. Ex. 16 at 11:10-25. Moreover, altering the claim as SAP suggests—to recite “accessing [an unsolicited message manager to] determining which nodes should receive the broadcast message”—makes no grammatical sense. This Court should adopt Valtrus’s construction. *See Ollnova Techs. Ltd. v. ecobee Techs., ULC*, Case No. 2:22-CV-00072-JRG, 2023 WL 2871051, at *5 (E.D. Tex. Apr. 10, 2023).

C. Disputed Terms of U.S. Patent No. 7,313,575

1. “polymorphic metadata” (Claims 1, 4)

SAP admits that polymorphism and metadata were well known concepts in the prior art, admits that the patent describes the use of hierarchy to implement polymorphism, quotes a portion

of the patent describing how “polymorphic metadata” is metadata that uses polymorphism, and quotes a description of how polymorphic metadata is implemented using hierarchy (*i.e.*, “an individual metadata class can be used to represent a different common pattern, defined with attributes that are specific to the pattern”). Resp. Br. at 12-13. Nevertheless, SAP argues that “Plaintiffs identify nothing in the specification or the extrinsic record from which a POSITA would understand with reasonable certainty how metadata is ‘defined using a polymorphic mechanism.’” *Id.* at 12.

SAP’s argument is both incorrect and improperly attempts to shift the burden to Valtrus to prove definiteness. The specification gives numerous examples of how polymorphic metadata is implemented using hierarchy. *See* Op. Br. at 14-15. And it is SAP who must prove indefiniteness by clear and convincing evidence. *See BASF Corp. v. Johnson Matthey Inc.*, 875 F.3d 1360, 1365 (Fed. Cir. 2017). SAP has not done so, and “polymorphic metadata” is not indefinite.

D. Disputed Terms of U.S. Patent No. 6,823,409

Section 112, ¶ 6 does not apply to the “coherency control module,” “request module,” and “static RAM interface module” terms. Each of these terms are presumed not to be means-plus-function terms because they do not recite the word “means,” and SAP has not met its burden to rebut this presumption (let alone its burden of showing indefiniteness). *See Dyfan, LLC v. Target Corp.*, 28 F.4th 1360, 1365–66 (Fed. Cir. 2022); *BASF*, 875 F.3d at 1365.

The unrebutted evidence shows that a POSITA would understand the disputed terms of the ’409 patent to refer to classes of structures generally known in the art. *See* Op. Br. at 21–26. As Dr. Brogioli explained, a POSITA would understand that “coherency control module” and its variants are generally recognized as specific structures in microprocessors implemented in hardware architecture, specifically, “the structural component in a multiprocessor that contains

the circuitry and logic that maintains coherency in cache memory.” *Id.* at 21–22 (citing *id.*, Ex. 3, ¶¶ 91–98). A POSITA would also understand that “request module” refers to “the structural component in a multiprocessor that contains the circuitry and logic that receives requests to access data.” *Id.* at 23–24 (citing *id.*, Ex. 3, ¶¶ 116–128). Finally, a POSITA would understand that “static RAM interface module” refers to “the structural component in a multiprocessor that contains the circuitry and logic that accesses static RAM (e.g., cache memory).” *Id.* at 25 (citing *id.*, Ex. 3, ¶¶ 133–146).

Consistent with a POSITA’s understanding, the ’409 patent claims and specification explain how the coherency control module interacts with other claimed components and how it operates as a whole. Op. Br. at 17–25 (citing *id.*, Ex. 1; *id.*, Ex. 3, ¶¶ 99–111, 118–128, 145–151). Specifically, the specification describes in detail the cache coherency problem and how an exemplary embodiment of the coherency control module, the tag control (TCON) module 40,⁴ operates in a multi-processor, multi-processor bus computing system to maintain cache coherency—first at a high level in reference to Figure 2 and then in terms of its architecture, including physical components used in circuitry, in reference to Figure 3. *Id.* at 17–21; *see also id.*, Ex. 1 at 5:13–11:65. This includes details regarding the structure and operation of the request module 42 and the tag RAM interface module 46, which a POSITA would understand to refer to the claimed request module and static RAM interface module, respectively.

SAP’s cited cases are inapposite because, in each case, the record lacked unrebutted intrinsic and extrinsic evidence demonstrating that the disputed term had a commonly understood meaning and is generally understood by a POSITA to connote structure. *See Williamson v. Citrix*

⁴ A POSITA would understand that the TCON module 40 is an embodiment of the coherency control module. *See* Op. Br., Ex. 3, ¶ 108; *id.*, Ex. 1 at 4:62–65, 5:13–24, 7:13–15 *id.*, Ex. 2 at VAL-SAP00004452–4453. Moreover, there is no requirement that the words in the claim must match those used in the specification disclosure. MPEP § 2173.05(e)(II).

Online, LLC, 792 F.3d 1339, 1350–1351 (Fed. Cir. 2015) (the specification and expert declaration do not describe how a “distributed learning control module” is understood as the name for structure); *Rain Computing, Inc. v. Samsung Elecs. Am., Inc.*, 989 F.3d 1002, 1006 (Fed. Cir. 2021) (the parties *agreed* that “user identification module” has no commonly understood meaning and is not generally viewed by one skilled in the art to connote structure); *Grecia v. Samsung Elecs. Am., Inc.*, 780 F. App’x 912, 914–16 (Fed. Cir. 2019) (nothing in the record suggested that the term would have been understood by persons of skill in the art to have a sufficiently definite meaning as the name for structure.); *Media Rights Techs., Inc. v. Cap. One Fin. Corp.*, 800 F.3d 1366, 1372–73 (Fed. Cir. 2015) (no dispute that the disputed term “compliance mechanism” has no commonly understood meaning and is not generally viewed by one skilled in the art to connote a particular structure and holding that the specification does not disclose how the mechanism and its components operated as a circuit).

Even if Section 112, ¶ 6 were to apply to these terms, the specification provides extensive disclosure about the architecture, structure, and operation of the cache coherency module, the TCON module 40, and its components the request module, request module 42, and the static RAM interface module, the tag RAM interface module 46/46a and 46b⁵. Op. Br. at 17–21; *id.*, Ex. 1 at 5:13–11:65; *id.*, Ex. 3, ¶¶ 91, 108–113, 116, 126–130, 133, 149–153. SAP argues that these claims lack structure corresponding to their purported functions without citing any record evidence, or explaining in any detail why it believes Valtrus’s and Dr. Brogioli’s specification

⁵ SAP asserts (without evidentiary support) that the disclosure regarding the request module 42 and ASQ 44, embodiments of the claimed request module and active snoop queue (ASQ) module cannot be attributed to the claimed coherency control module. Resp. Br. at 24. This is wrong. The request module, ASQ module, and static RAM interface module are subcomponents of the coherency control module and work together to contribute to its overall operation. See Op. Br. at 17–21; *id.*, Ex. 1, 5:13–11:65, Figs. 2, 3; *id.*, Ex. 3, ¶¶ 99–111.

citations (including Figures with circuitry) are wrong.⁶ SAP cannot meet its burden to prove indefiniteness by clear and convincing evidence. *See BASF*, 875 F.3d at 1365.

E. Disputed Term of U.S. Patent No. 6,871,264

SAP concedes that a POSITA would understand, based on the intrinsic record, that the high-speed interconnect couples cache memory to one or more processors through their cache controllers and that cache memory is commonly understood in the art to be “high-speed” memory. Op. Br. at 27–28 (citing Ex. 6 at 3:22–25, 4:10–21; *id.* at 2:11–13 (“Modern processor integrated circuits are frequently fabricated with cache memory. Cache memory offers substantially faster access than main memory[.]”); Op. Br., Ex. 3, ¶¶ 160–168; Exs. 7–13). As Dr. Brogioli explained, a POSITA would have no difficulty determining the scope of the invention because the high speeds at which cache memories operate—that thus need to be supported by the high-speed interconnect—and cache memory’s relative speed compared to, for example, main memory, are well within the knowledge of a POSITA. *See* Op. Br., Ex. 3, ¶¶ 163–167; *Nautilus*, 572 U.S. at 910. SAP’s unsupported arguments to the contrary cannot meet their burden to show indefiniteness by clear and convincing evidence. *See BASF*, at 1365.

III. CONCLUSION

For the foregoing reasons, Plaintiffs respectfully request that the Court enter an order adopting Plaintiffs’ proposed constructions and rejecting the positions SAP advances in its constructions.

⁶ SAP cites no evidence that the specification’s description of the operation of the tag RAM interface module 46 is “functionally based”. When read as a whole, the specification describes in detail how the tag RAM interface module 46 “checks” (*i.e.*, accesses) cache state data stored in the look-up table of tag RAM 29 and uses the data make efficient use of cache memory. *See* Op. Br., Ex. 1, 6:3–7:12, 10:20–11:8; *id.*, Ex. 3, ¶¶ 152–153. Moreover, even a lay person, let alone a POSITA, would understand that data transmission, including the tag RAM interface module checking data in the tag RAM, occurs via an electrical connection. *See* Op. Br., Ex. 1 at 6:25–65, Fig. 2; *id.*, Ex. 3, ¶ 144 (citing Exs. 19–27 thereto).

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Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that, on February 21, 2025 the foregoing document was served on all counsel of record who have consented to electronic service.

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