IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

VALTRUS INNOVATIONS LTD., **Plaintiff,** **vs.** **SAP AMERICA, INC. AND SAP SE,** **Defendants.**	**Civil Action No. 2:24-cv-21** **JURY TRIAL DEMANDED**

DEFENDANTS' INVALIDITY CONTENTIONS

Contents

I. RESERVATIONS 1
A. General Reservations 1
B. Ongoing Discovery 2
C. Claim Construction 4
D. Valtrus's Infringement Contentions 5
E. The Intrinsic Record 6
F. Rebuttal Evidence 6
G. Contextual Evidence 7
H. Invalidity Under Section 102(f) Prior Art 7
I. Priority and Effective Filing Date 8
J. No Patentable Weight 8
II. IDENTIFICATION OF PRIOR ART 9
A. Prior Art Patents and Published Applications 10
B. Prior Art Non-Patent References 15
C. Prior Art Offered For Sale and/or Publicly Used or Known 18
D. Admitted Prior Art 27
III. PRIOR ART CLAIM CHARTS 50
IV. PRIOR ART UNDER 35 U.S.C. § 102 THAT ANTICIPATES THE ASSERTED CLAIMS OF THE ASSERTED PATENTS 51
V. PRIOR ART UNDER 35 U.S.C. § 103 THAT RENDERS OBVIOUS THE ASSERTED CLAIMS OF THE ASSERTED PATENTS 55
VI. MOTIVATION FOR COMBINING IDENTIFIED PRIOR ART 61
VII. INVALIDITY UNDER 35 U.S.C. § 112(¶1/a) 69
VIII. INVALIDITY UNDER 35 U.S.C. § 112(2/b) 84
IX. INVALIDITY UNDER 35 U.S.C. § 101 (JUDGE GILSTRAP'S STANDING ORDER REGARDING SUBJECT MATTER ELIGIBILITY CONTENTIONS) 93
X. ACCOMPANYING DOCUMENT PRODUCTION 96

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 2 of 101

Pursuant to Rule 3-3 of the Local Patent Rules of the Eastern District of Texas and the Court's Docket Control Order (Dkt. No. 32), SAP America, Inc. and SAP SE (collectively, "Defendants" or "SAP") provide Valtrus Innovations Ltd.'s ("Plaintiff" or "Valtrus") with notice of its Invalidity Contentions (the "Invalidity Contentions") with respect to those claims asserted against them by Valtrus in its March 11, 2024 Initial Disclosure of Asserted Claims and Infringement Contentions, collectively being claims 1-17 of U.S. Patent No. 6,823,409 (the "'409 Patent"); claims 1-10 of U.S. Patent No. 6,889,244 (the "'244 Patent"); claims 1-7 and 9-18 of U.S. Patent No. 7,152,182 (the "'182 Patent"); claims 1-14, 16-28, and 30-36 of U.S. Patent No. 7,313,575 (the "'575 Patent"); claims 1-4, 5, 7-12, and 14-18 of U.S. Patent No. 6,691,139 (the "'139 Patent"); claims 1-6, 10, and 33 of U.S. Patent No. 7,936,738 (the "'738 Patent"), and claims 1-5 and 8-11 of U.S. Patent No. 6,871,264 (the "'264 Patent") (collectively and respectively, the "Asserted Patents" and the "Asserted Claims").

I. RESERVATIONS

A. General Reservations

SAP relies on and incorporates by reference, as if originally set forth herein, all invalidity or unenforceability positions, and all associated prior art and arguments, raised during the prosecution of the Asserted Patents. Moreover, SAP reserves the right, to the extent permitted by the Court and the applicable statutes and rules, to supplement these Invalidity Contentions based on prior art currently known to Valtrus, including documents responsive to the mandatory disclosures contained in the Court's Discovery Order (Dkt. No. 33) and prior art identified or provided to Valtrus by any third party.

Consistent with Patent Rule 3-6, SAP reserves the right to amend these Invalidity Contentions. SAP reserves the right to amend or supplement these disclosures and the corresponding document production should Valtrus: 1) provide any information that it failed to

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 3 of 101

provide in its Patent Rule 3-1 and 3-2 disclosures; 2) amend its Patent Rule 3-1 or 3-2 disclosures in any way; or 3) attempt to rely on any information at trial, in a hearing or during a deposition that it failed to provide in its Patent Rule 3-1 and 3-2 disclosures.

SAP provides the information below, as well as the accompanying production of documents, for the sole purpose of complying with Patent Rules 3-3 and 3-4. The information provided shall not be deemed an admission regarding the scope of any claims or the proper construction of those claims or any terms contained therein. Nothing contained in these Invalidity Contentions should be understood or deemed to be an express or implied admission or contention with respect to the proper construction of any terms in the Asserted Claim, or with respect to the alleged infringement of that claim.

B. Ongoing Discovery

Furthermore, because only limited discovery has occurred and because SAP continues its search for and analysis of relevant prior art, SAP reserves the right to revise, amend, and/or supplement the information provided herein, including identifying, charting, and relying on additional references, should SAP's further search and analysis yield additional information or references, consistent with the Local Patent Rules and the Federal Rules of Civil Procedure.

SAP's Invalidity Contentions are based on information reasonably available to it as of the date of these contentions. Because discovery is ongoing SAP expressly reserves the right to clarify, alter, amend, modify, or supplement these Invalidity Contentions, to identify additional prior art, and to rely on additional information, documents, tangible things, and testimony obtained during discovery, including discovery obtained from third parties. For example, prior art not included in these contentions whether or not known to SAP at this time, may become relevant depending on the positions Valtrus asserts and the claim constructions the Court adopts.

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 4 of 101

Discovery is in its infancy and is ongoing, and SAP's prior art investigation and third-party discovery is therefore not yet complete. SAP reserves the right to present additional items of prior art under 35 U.S.C. §§ 102(a), (b), (e), and/or (g), and/or 103 located during the course of discovery or further investigation. For example, SAP has issued and may issue additional subpoenas to third parties believed to have knowledge, documentation, and/or corroborating evidence concerning some of the prior art listed herein and/or additional prior art. These third parties include without limitation the authors, inventors, or assignees of the references listed in these disclosures. For example, for any given company's commercial products, SAP anticipates that additional documentation relating to these products will be discovered, and SAP reserves the right to rely on such documentation to further support these Invalidity Contentions. In addition, SAP reserves the right to assert invalidity under 35 U.S.C. § 102(c), (d), or (f) to the extent that discovery or further investigation yield information forming the basis for such invalidity.

Similarly, SAP has not had the opportunity to take any depositions of the inventors named on the face of the Asserted Patents or other persons having relevant information. SAP reserves the right to revise, amend or supplement these Invalidity Contentions pursuant to Federal Rule of Civil Procedure 26(e) and the Local Rules to the extent appropriate in light of further investigation and discovery regarding the defenses, the review and analysis of expert witnesses, or supplemental disclosures or contentions by Valtrus.

SAP accordingly reserves the right to modify these Invalidity Contentions by adding or withdrawing prior art and/or modifying any of the referenced claim charts in light of the Court's claim construction ruling, any amended or supplemental infringement contentions by Valtrus, any party admissions or admissions by any named inventor concerning the scope of the claims or teachings of the prior art, or any positions taken by Valtrus in this or related litigation, covered-

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 5 of 101

business method review, reexamination, or other proceeding, or to avoid unfair prejudice from Valtrus's failure to timely comply with its disclosure obligations. Furthermore, additional obviousness combinations of the references identified in these Invalidity Contentions are possible, and SAP reserves the right to use any such combination(s) in this case. In particular, SAP is currently unaware of the extent, if any, to which Valtrus will contend that limitations of the claims at issue are not disclosed in the art identified by SAP as anticipatory, and the extent to which Valtrus will contend that elements not disclosed in the specifications of the Asserted Patents and related applications would have been known to persons of ordinary skill in the art at the relevant time. To the extent that an issue arises with any such limitations, SAP reserves the right to identify other references that would have made such limitations obvious in view of the relevant disclosures.

SAP also reserves the right to revise its ultimate contentions concerning the invalidity of the Asserted Claims of the Asserted Patents, which may change depending on any findings as to the priority date of those claims and/or positions that Valtrus or expert witness(es) may take concerning infringement and/or invalidity issues.

C. Claim Construction

SAP does not waive the right to contest any claim constructions or to take positions during claim construction proceedings that have yet to occur that may be inconsistent with the Invalidity Contentions herein. Consequently, SAP also reserves the right to amend or supplement these Invalidity Contentions in the event that the claims are construed differently at some point in the future, in accordance with Patent Rule 3-6.

SAP does not necessarily adopt Valtrus's positions on the scope or construction of the claims. In certain instances, SAP has applied the claims to the prior art in view of Valtrus's allegations, admissions, or positions for purposes of these contentions only. As such, SAP's Invalidity Contentions are not adoptions or admissions by SAP as to the accuracy of Valtrus's

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 6 of 101

allegations, admissions, or positions. Accordingly, these contentions are made in the alternative, are not necessarily intended to be consistent with each other or other contentions, and should not be otherwise construed.

SAP expressly reserves the right to take positions with respect to future claim construction or infringement issues that are inconsistent with, or even contradictory to, the claim construction or infringement positions expressed or implied in the Invalidity Contentions set forth herein.

D. Valtrus's Infringement Contentions

Valtrus's disclosures under Patent Rules 3-1 and 3-2 are incomplete or deficient in numerous respects. For example, Valtrus has not yet specifically identified where each software element of each claim is found within each Accused Instrumentality as required by Patent Rule 3-1 and paragraph 3(a)(i) of this Court's Discovery Order (Dkt. No. 33). The lack of detail in Valtrus's Infringement Contentions has impaired SAP's ability to prepare these Invalidity Contentions by forcing it to speculate as to Valtrus's actual position on SAP's alleged infringement. Therefore, these Invalidity Contentions are based in whole or in part on the present understanding of the Asserted Claims and Valtrus's apparent positions as to the scope of the Asserted Claims as applied in its P.R. 3-1 disclosures. SAP further reserves the right to modify or add additional contentions in light of any amendment made by Valtrus under Local Patent Rule 3-6 or paragraph 3(a)(i) of this Court's Discovery Order. Furthermore, any such amendment may lead to further grounds for invalidity, SAP specifically reserves the right to modify, amend, or supplement its Invalidity Contentions as Valtrus modifies, amends, or supplements its disclosures under Patent Rules 3-1, 3-2, and/or 3-6, produces documents in discovery, or amend its contentions under paragraph 3(a)(i) of this Court's Discovery Order.

Additionally, Valtrus has presented insufficient contentions for indirect infringement, i.e., active inducement or contributory infringement. Valtrus has not, for example, provided detailed

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 7 of 101

contentions that identify how SAP allegedly induces direct infringement of the Asserted Patents by a third party, or how SAP allegedly contributes to the infringement of the Asserted Patents by a third party. Nor has Valtrus provided detailed contentions regarding any alleged infringement by multiple parties pursuant to 35 U.S.C. § 271(a) (i.e., joint infringement). Nor has Valtrus provided detailed contentions of any alleged infringement under the doctrine of equivalents. If Valtrus is permitted to provide this and other information relating to alleged indirect or joint infringement or infringement pursuant to the doctrine of equivalents, SAP will amend and supplement these Invalidity Contentions as appropriate.

E. The Intrinsic Record

SAP further reserves the right to rely on applicable industry standards and prior art cited or discussed in the specifications and file histories of the Asserted Patents, and any related U.S. and foreign patent applications as invalidating references or to show the state of the art. SAP further reserves the right to rely on the patent applicants' admissions concerning the scope of the prior art relevant to the Asserted Patents found in, *inter alia*: the specifications; the patent prosecution history for the Asserted Patents and any related patents and/or patent applications or reexaminations; any deposition testimony of the named patent applicants on the Asserted Patents; and the papers filed and any evidence submitted by Valtrus in connection with this litigation.

F. Rebuttal Evidence

Prior art not included in these Invalidity Contentions, whether known or not known to SAP, may become relevant. In particular, SAP is currently unaware of the extent, if any, to which Valtrus will contend that limitations of the Asserted Claims of the Asserted Patents are not disclosed in the prior art identified herein. To the extent that such an issue arises, SAP reserves the right to

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 8 of 101

identify other references that would render obvious the allegedly missing limitation(s) or the disclosed device or method.

G. Contextual Evidence

SAP's claim charts cite particular teachings and disclosures of the prior art as applied to the limitation of each of the Asserted Claims. Persons having ordinary skill in the art, however, may generally view an item of prior art in the context of his or her experience and training, other publications, literature, products, and understanding. As such, the cited portions are only examples, and SAP reserves the right to rely on uncited portions of the prior art references and on other publications and expert testimony as aids in understanding and interpreting the cited portions, as providing context thereto, and as additional evidence that the prior art discloses a claim limitation or the claimed subject matter as a whole. SAP further reserves the right to rely on uncited portions of the prior art references, other publications, and testimony, including expert testimony, to establish bases for combinations of certain cited references that render the Asserted Claims obvious. The references discussed in the claim charts may disclose the elements of the Asserted Claims explicitly and/or inherently, and/or they may be relied on to show the state of the art in the relevant time frame. The suggested obviousness combinations are provided in the alternative to anticipation contentions and are not to be construed to suggest that any reference included in the combinations is not by itself anticipatory.

H. Invalidity Under Section 102(f) Prior Art

SAP reserves the right to assert that the Asserted Claims of the Asserted Patents are invalid under 35 U.S.C. § 102(f) in the event SAP obtains evidence that the inventors named on the Asserted Patents or related patents, did not themselves "invent" the subject matter claimed. Should

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 9 of 101

SAP obtain such evidence, it will provide the name of the person(s) from whom and the circumstances under which the claimed subject matter or any part of it was derived.

I. Priority and Effective Filing Date

SAP reserves the right to amend these contentions on the Court's determination of the priority date(s) of the Asserted Claims. SAP further reserves the right to use related patents in the alleged chain of priority of the Asserted Patents as prior art on the Court's determination of the priority date(s) of the Asserted Claims.

J. No Patentable Weight

SAP reserves the right to argue that various portions of the Asserted Claims, such as an intended use or result, non-functional descriptive material, and certain preamble language, are entitled to no patentable weight. Mapping of a portion of an Asserted Claim to a prior art reference does not represent that such portion of the claim is entitled to patentable weight when comparing the claimed subject matter to the prior art.

K. Inequitable Conduct

SAP reserves the right to contend that the Asserted Patents are unenforceable due to inequitable conduct by Valtrus or the applicant, including but not limited to inequitable conduct by failure to disclose any of the references identified below to the extent that Valtrus or the applicant was aware of the reference during prosecution of an Asserted Patent but did not disclose it to the reviewing agency.

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 10 of 101

II. IDENTIFICATION OF PRIOR ART

At least the prior art listed below, individually or in combination, invalidates the Asserted Claims. *See* Patent Rule 3-3(a). The attached Exhibits provide detailed claim charts showing where each claim element may be found in the particular reference being charted.

SAP identifies the following items of prior art that anticipate or render obvious the Asserted Claims. The identification of prior art below is not exclusive, and SAP's production pursuant to Patent Rule 3-3 contains additional references that render the Asserted Claims invalid. SAP reserves the right to rely on both the listed and unlisted references produced pursuant to Patent Rule 3-3, as well as other art that may become known and/or relevant during the course of this or related litigation.

For those references for which detailed claim charts are not provided in the attached Exhibits, those additional prior art references are otherwise pertinent to the invalidity of the Asserted Patents, either alone or in combination with other references. At this time, SAP is not providing claim charts for each of these additional references, either because they are cited in conjunction with primary references for which charts have already been provided and are cited therein, and/or because these references have similar disclosure to the prior art references for which invalidity charts have been provided and/or may be used to show the state of the art.

SAP also incorporates as if fully set forth herein the complete file histories for the Asserted Patents, including any prior art or supporting documents cited therein.

SAP not only relies on the prior art disclosed herein, but also relies on any commercial embodiments and accompanying literature of the various assignees that correspond to the respective disclosures found within the prior art disclosed herein. The assignees' various and respective commercial embodiments and/or corresponding literature anticipate and/or render obvious the claims of the Asserted Patents for at least the reasons disclosed in these Invalidity

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 11 of 101

Contentions and claim charts, as well as for other independent reasons found within the commercial embodiments and corresponding literature. SAP also reserves the right to rely on related patents, published applications, foreign patents or publications, and other patent documents as necessary to establish prior art status or clarify the disclosures cited.

SAP reserves the right to revise its claim charts to rely on any of these references to prove the invalidity of the claims of the Asserted Patents in a manner consistent with the Federal Rules of Civil Procedure, the Court's Local Rules, and this Court's Orders.

A. Prior Art Patents and Published Applications

- U.S. Patent No. 5,109,384 to Tseung, issued Apr. 28, 1992
- U.S. Patent No. 5,239,640 to Froemke, issued Aug. 24, 1993
- U.S. Patent No. 5,440,726 to Fuchs, issued Aug. 8, 1995
- U.S. Patent No. 5,455,946 to Mohan, issued Oct. 3, 1995
- U.S. Patent No. 5,504,861 to Crockett, issued Apr. 2, 1996
- U.S. Patent No. 5,588,147 to Neeman, issued Dec. 24, 1996
- U.S. Patent No. 5,634,052 to Morris, issued May 27, 1997
- U.S. Patent No. 5,678,026 to Vartti, issued Oct. 14, 1997
- U.S. Patent No. 5,790,789 to Suarez, issued Aug. 4, 1998
- U.S. Patent No. 5,805,798 to Kearns, issued Sep. 8, 1998
- U.S. Patent No. 5,809,537 to Itskin, issued Sep. 15, 1998
- U.S. Patent No. 5,815,649 to Utter, issued Sep. 29, 1998
- U.S. Patent No. 5,819,272 to Benson, issued Oct. 6, 1998
- U.S. Patent No. 5,822,611 to Donley, issued Oct. 13, 1998
- U.S. Patent No. 5,829,025 to Mittal, issued Oct. 27, 1998
- U.S. Patent No. 5,845,061 to Miyamoto, issued Dec. 1, 1998

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 12 of 101

- U.S. Patent No. 5,860,101 to Arimilli, issued Jan. 12, 1999
- U.S. Patent No. 5,889,935 to Ofek, issued Mar. 30, 1999
- U.S. Patent No. 5,890,165 to Boudrie, issued Mar. 30, 1999
- U.S. Patent No. 5,893,151 to Merchant, issued Apr. 6, 1999
- U.S. Patent No. 5,938,775 to Damani, issued Aug. 17, 1999
- U.S. Patent No. 5,958,031 to Kim, issued Sep. 28, 1999
- U.S. Patent No. 5,983,259 Campbell, issued Nov. 9, 1999
- U.S. Patent No. 6,018,747 to Burns, issued Jan. 25, 2000
- U.S. Patent No. 6,029,178 to Martin, issued Feb. 22, 2000
- U.S. Patent No. 6,035,412 to Tamer, issued Mar. 7, 2000
- U.S. Patent No. 6,070,251 to Chong, issued May 30, 2000
- U.S. Patent No. 6,085,276 to VanDoren, issued Jul. 4, 2000
- U.S. Patent No. 6,088,717 to Reed, issued Jul. 11, 2000
- U.S. Patent No. 6,105,122 to Muller, issued Aug. 15, 2000
- U.S. Patent No. 6,173,367 Aleksic, issued Jan. 9, 2001
- U.S. Patent No. 6,173,377 to Yanai, issued Jan. 9, 2001
- U.S. Patent No. 6,178,427 to Parker, issued Jan. 23, 2001
- U.S. Patent No. 6,199,179 to Kaufmann, issued Mar. 6, 2001
- U.S. Patent No. 6,205,449 to Rastogi, issued Mar. 20, 2001
- U.S. Patent No. 6,253,295 to Beal, issued Jun. 26, 2001
- U.S. Patent No. 6,279,084 to VanDoren, issued Aug. 21, 2001
- U.S. Patent No. 6,320,949 to Kim, issued Nov. 20, 2001
- U.S. Patent No. 6,321,259 to Ouellette, issued Nov. 20, 2001
- U.S. Patent No. 6,321,284 to Shinohara, issued Nov. 20, 2001

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 13 of 101

- U.S. Patent No. 6,381,682 to Noel, issued Apr. 30, 2002
- U.S. Patent No. 6,397,273 to Chilton, issued May 28, 2002
- U.S. Patent No. 6,438,538 to Goldring, issued Aug. 20, 2002
- U.S. Patent No. 6,438,658 to Akashi, issued Aug. 20, 2002
- U.S. Patent No. 6,442,706 to Wah, issued Aug. 27, 2002
- U.S. Patent No. 6,449,671 to Patkar, issued Sep. 10, 2002
- U.S. Patent No. 6,460,122 to Otterness, issued Oct. 1, 2002
- U.S. Patent No. 6,487,643 to Khare, issued Nov. 26, 2002
- U.S. Patent No. 6,516,393 to Fee, issued Feb. 4, 2003
- U.S. Patent No. 6,546,413 to Northrup, issued Apr. 8, 2003
- U.S. Patent No. 6,553,391 to Goldring, issued Apr. 22, 2003
- U.S. Patent No. 6,560,593 to Kosciuszko, issued May 6, 2003
- U.S. Patent No. 6,560,617 to Winger, issued May 6, 2003
- U.S. Patent No. 6,604,174 to Dean, issued Aug. 5, 2003
- U.S. Patent No. 6,615,225 to Cannon, issued Sep. 2, 2003
- U.S. Patent No. 6,615,253 to Bowman, issued Sep. 2, 2003
- U.S. Patent No. 6,622,152 to Sinn, issued Sep. 16, 2003
- U.S. Patent No. 6,662,195 to Langseth, issued Dec. 9, 2003
- U.S. Patent No. 6,681,296 to Liao, issued Jan. 20, 2004
- U.S. Patent No. 6,684,301 to Martin, issued Jan. 27, 2004
- U.S. Patent No. 6,694,447 to Leach, issued Feb. 17, 2004
- U.S. Patent No. 6,775,239 to Akita, issued Aug. 10, 2004
- U.S. Patent No. 6,789,114 to Garg, issued Sep. 7, 2004
- U.S. Patent No. 6,826,757 to Steele, issued Nov. 30, 2004

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 14 of 101

- U.S. Patent No. 6,907,011 to Miller, issued Jun. 14, 2005
- U.S. Patent No. 6,910,148 to Ho, issued Jun. 21, 2005
- U.S. Patent No. 7,210,061 to Anderson, issued Apr. 24, 2007
- U.S. Patent No. 7,318,133 to Yagawa, issued Jan. 8, 2008
- U.S. Patent No. 7,412,492 to Waldspurger, issued Aug. 12, 2008
- Korean Patent No. 100289686 to Lee, issued May 15, 2001
- U.S. Patent Application No. 2001/0047372 to Gorelik, published Nov. 29, 2001
- U.S. Patent Application No. 2001/0049771 to Tischler, published Dec. 6, 2001
- U.S. Patent Application No. 2001/0056420 to Steele, published Dec. 27, 2001
- U.S. Patent Application No. 2002/0004799 to Gorelik, published Jan. 10, 2002
- U.S. Patent Application No. 2002/0049950 to Loaiza, published Apr. 25, 2002
- U.S. Patent Application No. 2002/0083281 to Carteau, published Jun. 27, 2002
- U.S. Patent Application No. 2002/0091718 to Bohannon, published Ju1. 11, 2002
- U.S. Patent Application No. 2002/0116576 to Keshava, published Aug. 22, 2002
- U.S. Patent Application No. 2002/0129208 to Barroso, published Sep. 12, 2002
- U.S. Patent Application No. 2002/0184445 to Cherabuddi, published Dec. 5, 2002
- U.S. Patent Application No. 2002/0196778 to Colmant, published Dec. 26, 2002
- U.S. Patent Application No. 2002/0198858 to Stanley, published Dec. 26, 2002
- U.S. Patent Application No. 2002/0198902 to Sankaran, published Dec. 26, 2002
- U.S. Patent Application No. 2003/0014397 to Chau, published Jan. 16, 2003
- U.S. Patent Application No. 2003/0014433 to Teloh, published Jan. 16, 2003
- U.S. Patent Application No. 2003/0018808 to Brouk, published Jan. 23, 2003
- U.S. Patent Application No. 2003/0046604 to Lau, published Mar. 6, 2003
- U.S. Patent Application No. 2003/0093575 to Upton, published May 15, 2003

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 15 of 101

- U.S. Patent Application No. 2003/0093638 to Margerie, published May 15, 2003
- U.S. Patent Application No. 2003/0096592 to Moreau, published May 22, 2003
- U.S. Patent Application No. 2003/0126107 to Yamagami, published Jul. 3, 2003
- U.S. Patent Application No. 2003/0126282 to Sarkar, published Jul 3, 2003
- U.S. Patent Application No. 2003/0200397 to McAllister, published Oct. 23, 2003
- U.S. Patent Application No. 2003/0225760 to Ruuth, published Dec. 4, 2003
- U.S. Patent Application No. 2003/0229529 to Mui, published Dec. 11, 2003
- U.S. Patent Application No. 2004/0010502 to Bomfim, published Jan. 15, 2004
- U.S. Patent Application No. 2004/0015898 to Tewksbary, published Jan. 22, 2004
- U.S. Patent Application No. 2004/0078619 to Vasavada, published Apr. 22, 2004
- U.S. Patent Application No. 2004/0088418 to Iyer, published May 6, 2004
- U.S. Patent Application No. 2004/0139322 to Kaler, published Jul. 15, 2004
- U.S. Patent Application No. 2005/0021354 to Brendle, published Jan. 27, 2005
- U.S. Patent Application No. 2005/0096950 to Caplan, published May 5, 2005
- PCT Application No. WO 2001/013232A2 to Frey, published Feb. 22, 2001
- PCT Application No. WO 2003/009157 to Halpern, published Jan. 30, 2003.
- PCT Application No. WO 2003/017022 to Nahum, published Feb. 27, 2003
- PCT Application No. WO 2003/032181 to Messinger, published Apr. 17, 2003
- PCT Application No. WO 2003/102722 to Blevins, published Dec. 11, 2003
- European Patent Application No.008111122, filed Nov. 2000.
- Japanese Patent Application No. JPH 06103092A to Imada, published Apr. 15, 1994
- Japanese Patent Application No. JPH 10333974A to Shigegaki, published Dec. 18, 1998.
- Korean Patent Application No. 2002/ 0062483 to Cho, published July, 26, 2002

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 16 of 101

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SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 17 of 101

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- IBM, “IBM Gekko RISC Microprocessor User’s Manual,” (May 2000)
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- IBM, “Technical Information Manual / PC 300GL Types 6563, 6564, 6574 / PC 300PL Type 6565,” (Mar. 2000)
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- Lamont, Judith, “Data warehousing from end to end,” KM World (May 1999)
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SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 18 of 101

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- Olokotun, Kunle, “ChipMultiprocessor Architecture: Techniques to Improve Throughput and Latency,” Synthesis Lectures on Computer Architecture (2007)
- Polyzois, Christos, “Evaluation of Remote Backup Algorithms for Transaction Processing Systems,” ACM SIGMOD (J,un. 1997)
- Powers, Susan, “AS/400 Disk Storage Topics and Tools,” IBM (Apr. 2000)
- Ramani, Srinivasan, “Building a Reliable Message Delivery System Using the CORBA Event Service,” IPDPS 2000 Workshops, LNCS 1800 (Jan. 2000)
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- Steffan, Gregory, “A Scalable Approach to Thread-Level Speculation,” Carnegie Mellon Univ. (1997)
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- Suh, Ed, “Analytical Cache Models with Applications to Cache Partitioning,” CSAIL (Feb. 2001)
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- Tremblay, Marc, "The MAJC Architecture," IEEE (2000)
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- Wade, Will, "Sun unveils first MAJC chip," EE Times (Oct. 1999)
- Wright, Gregory, "A single-chip multiprocessor architecture with hardware thread support," Univ. of Manchester (Jan 2001)

C. Prior Art Offered For Sale and/or Publicly Used or Known

Pursuant to Local Patent Rule 3-3(a), SAP provides the following information regarding prior art which was the subject of a commercial offer of sale and/or in public use prior to the earliest permissible priority date of the Asserted Patents. To the extent necessary, SAP has or will serve subpoenas and/or otherwise request further information pertaining to the products and/or software programs (and/or obtain the actual products and/or software programs themselves). For example, SAP may issue subpoenas in short order to the following third parties who have knowledge, documentation, and/or corroborating evidence regarding the system art this section:

To the extent necessary, SAP will amend and/or supplement these Invalidity Contentions based on information received in response.

- ActaWorks / Business Object ETL Tool
    - On information and belief, this product package was invented, purchased, evaluated, compared, tested, implemented, made, used (publicly and/or

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 20 of 101

commercially), disclosed, offered for sale, and/or sold by Acta Technology and later Business Object in the United States at least as early as 1997.

- SAP's current understanding of the design, implementation, and capabilities of the ActaWorks / Business Object ETLTool system is charted in (at least) the following references:
  - Gorelik 372 App
  - Gorelik 799 App
  - Bloor Research, "Data Integrator version 6.5 from Business Objects."
  - Business Objects "End-to-End Business Intelligence with BusinessObjects Data Integrator"
  - Business Objects "What's New in Data Integrator 6.5"
  - Nucleus Research, "BusinessObjects releases Data Integrator 6.5"
  - Lamont, Judith, "Data warehousing from end to end."
  - HPC Wire, "Acta Leads ETL Industry In Performance On Benchmark Tests."
  - FHC, "Acta first to integrate Web services and ETL."
  - CBR, "Acta Offers to Warehouse SAP Data."

- Sybase ASE High Availability
  - On information and belief, this product package was invented, purchased, evaluated, compared, tested, implemented, made, used (publicly and/or commercially), disclosed, offered for sale, and/or sold by Sybase in the United States at least as early as 2001.
  - SAP's current understanding of the design, implementation, and capabilities of the Sybase ASE High Availability system is charted in (at least) the following references:
    - ASE, "What's New in Sybase Adaptive Server Enterprise?" (Jun. 2001).
    - ASE, "The Official Guide Sybase ASE 12.5 High Availability," (2002).

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 21 of 101

        - ASE, “Taming the Downtime: High Availability in Sybase ASE 12” (Feb. 2000).

- HP ServiceGuard

    - On information and belief, this product package was invented, purchased, evaluated, compared, tested, implemented, made, used (publicly and/or commercially), disclosed, offered for sale, and/or sold by HP in the United States at least as early as June 2002.

    - SAP’s current understanding of the design, implementation, and capabilities of the HP ServiceGuard system is charted in (at least) the following references:

        - Hewlett Packard, “Managing MC/ServiceGuard,” (Mar. 2002).

- IBM Database Replication

    - On information and belief, this product package was invented, purchased, evaluated, compared, tested, implemented, made, used (publicly and/or commercially), disclosed, offered for sale, and/or sold by IBM in the United States at least as early as 2000.

    - SAP’s current understanding of the design, implementation, and capabilities of the IBM Database Replicaiton system is charted in (at least) the following references:

        - Goldring ’391
        - Goldring ’538
        - Morris ’052
        - Sinn ’152
        - Mohan ’946
        - Cannon ’225
        - Burns ’747
        - Ruuth ’760 App
        - Beal ’295
        - Crocket ’861

- Oracle Database Replication

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 22 of 101

- On information and belief, this product package was invented, purchased, evaluated, compared, tested, implemented, made, used (publicly and/or commercially), disclosed, offered for sale, and/or sold by Oracle in the United States at least as early as 2000.

- SAP's current understanding of the design, implementation, and capabilities of the Oracle Database Replication system is charted in (at least) the following references:

  - To, Oracle8i Standby Database

  - Leach '447

  - Loaiza '950 App

  - Chong '251

  - Teloh '433

- EMC Database Replication

  - On information and belief, this product package was invented, purchased, evaluated, compared, tested, implemented, made, used (publicly and/or commercially), disclosed, offered for sale, and/or sold by EMC in the United States at least as early as 2000.

  - SAP's current understanding of the design, implementation, and capabilities of the EMC Database Replication system is charted in (at least) the following references:

    - Boudrie '165

    - Yanai '377

    - Winger '617

    - Ofek '935

- IBM Processors

  - On information and belief, this product package, including but not limited to the IBM's Power4 CPU and IBM Sysem, was invented, purchased, evaluated, compared, tested, implemented, made, used (publicly and/or commercially), disclosed, offered for sale, and/or sold by IBM in the United States at least as early as 2000.

  - SAP's current understanding of the design, implementation, and capabilities of the IBM Processors are charted in (at least) the following references:

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 23 of 101

        - Fee ’393
        - Arimilli ’101
        - Itskin ’537
        - Otterness ’122
        - IBM, “The IBM Power4”
        - Tender, “IBM eServer Power 4 System Microarchitecture”
        - Powers, Susan, “AS/400 Disk Storage Topics and Tools”
        - IBM, “IBM Gekko RISC Microprocessor User’s Manual”
        - IBM, “Technical Information Manual PC 300PL”
        - IBM, “Technical Information Manual / PC 300GL Types 6563, 6564, 6574 / PC 300PL Type 6565”
        - IBM, “Technical Information Manual PC 730 (Type 6877) and PC 750 (Type 6887)”

- MIT M-Machine
    - On information and belief, this product package was invented, purchased, evaluated, compared, tested, implemented, made, used (publicly and/or commercially), disclosed, offered for sale, and/or sold by MIT in the United States at least as early as 1995.
    - SAP’s current understanding of the design, implementation, and capabilities of the MIT M-Machine are charted in (at least) the following references:
        - Schiltz, Andrew, “Advances in the M-Machine Runtime System”
        - Costlow, Terry, “Arpa funds development of parallel-supercomputer IC”
        - Gupta, Parag, “Design and Implementation of the Integer Unit Datapath of the MAP Cluster of the M-Machine”
        - Fillo, Marco, “Instruction Scheduling on the M-Machine Multicomputer”
        - MIT, “M-Machine Project Page“
        - Fillo, Marco, “The M-Machine Multicomputer”

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 24 of 101

        - Gurevich, Yevgeny, "The M-Machine Operating System"

- Stanford Hydra CMP

    - On information and belief, this product package was invented, purchased, evaluated, compared, tested, implemented, made, used (publicly and/or commercially), disclosed, offered for sale, and/or sold by Stanford in the United States at least as early as 1997.

    - SAP's current understanding of the design, implementation, and capabilities of the Stanford Hydra CMP are charted in (at least) the following references:

        - Hammond, "A Single-Chip Multiprocessor"

        - Hammond, "Data Speculation Support for a Chip Multiprocessor"

        - Hammond, "The Standford Hydra CMP"

        - Hammond, Lance, "Considerations in the Design of Hydra"

        - Olokotun, Kunle, "ChipMultiprocessor Architecture: Techniques to Improve Throughput and Latency"

- Sun Microsystems's MAJC

    - On information and belief, this product package was invented, purchased, evaluated, compared, tested, implemented, made, used (publicly and/or commercially), disclosed, offered for sale, and/or sold by Sun Microsystem in the United States at least as early as 1999.

    - SAP's current understanding of the design, implementation, and capabilities of the MAJC are charted in (at least) the following references:

        - Wade, "Sun unveils first MAJC chip"

        - Tremblay, "The MAJC Architecture"

- CMU Stampede

    - On information and belief, this product package was invented, purchased, evaluated, compared, tested, implemented, made, used (publicly and/or commercially), disclosed, offered for sale, and/or sold by Carnegie Mellon in the United States at least as early as 1997.

    - SAP's current understanding of the design, implementation, and capabilities of the CMU Stampede are charted in (at least) the following references:

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 25 of 101

        - Steffan, Gregory, "A Scalable Approach to Thread-Level Speculation."
        - Steffan, Gregory, "The Potential for Using Thread-Level Data Speculation to Facilitate Automatic Parallelization."
        - Steffan, Gregory, "The Potential for Thread-Level Data Speculation in Tightly Coupled Multiprocessors."
        - Steffan, Gregory, "Architectural Support for Thread-Level Data Speculation."
        - Steffan, Gregory, "Extending Cache Coherence to Support Thread-Level Data Speculation on a Single Chip and Beyond."

- Wisconsin Multiscalar
    - On information and belief, this product package was invented, purchased, evaluated, compared, tested, implemented, made, used (publicly and/or commercially), disclosed, offered for sale, and/or sold by the University of Wisconsin in the United States at least as early as 1993.
    - SAP's current understanding of the design, implementation, and capabilities of the Wisconsin Multiscalar are charted in (at least) the following references:
        - Wright, Gregory, "A single-chip multiprocessor architecture with hardware thread support"
        - Burger, Doug, "DataScalar Architectures"
        - Steffan, Gregory, "Hardware Support for Thread-Level Speculation"
        - Hiraki, Kei, "Speculative execution model with duplication"
        - Franklin, Manoj, "The Multiscalar Architecture"

- Intel Processors
    - On information and belief, this product package was invented, purchased, evaluated, compared, tested, implemented, made, used (publicly and/or commercially), disclosed, offered for sale, and/or sold by IBM in the United States at least as early as 2000.
    - SAP's current understanding of the design, implementation, and capabilities of the Intel Processors are charted in (at least) the following references:

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 26 of 101

        - Khare ’643
        - Keshava ’576 App.
        - Merchant ’151
        - Mittal ’025
        - Akashi ’658

- Java Messaging Service

    - On information and belief, this product package was invented, purchased, evaluated, compared, tested, implemented, made, used (publicly and/or commercially), disclosed, offered for sale, and/or sold by Sun Microsystems in the United States at least as early as 2002.

    - SAP’s current understanding of the design, implementation, and capabilities of the Java Messaging Service are charted in (at least) the following references:

        - Java Message Service Specification v1.1, Sun Microsystems

- Alcatel Fault Tolerant Systems

    - On information and belief, this product package was invented, purchased, evaluated, compared, tested, implemented, made, used (publicly and/or commercially), disclosed, offered for sale, and/or sold by Alcatel in the United States at least as early as 2000.

    - SAP’s current understanding of the design, implementation, and capabilities of the Alcatel Fault Tolerant Systems are charted in (at least) the following references:

        - Garg ’114
        - Utter ’649
        - Moreau ’592

- IBM Fault Tolerant Systems

    - On information and belief, this product package was invented, purchased, evaluated, compared, tested, implemented, made, used (publicly and/or commercially), disclosed, offered for sale, and/or sold by IBM in the United States at least as early as 2000.

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 27 of 101

- SAP's current understanding of the design, implementation, and capabilities of the IBM Fault Tolerant Systems are charted in (at least) the following references:
    - Miller '011
    - Campbell '259

- AT&T Fault Tolerant Systems
    - On information and belief, this product package was invented, purchased, evaluated, compared, tested, implemented, made, used (publicly and/or commercially), disclosed, offered for sale, and/or sold by AT&T in the United States at least as early as 2000.
    - SAP's current understanding of the design, implementation, and capabilities of the AT&T Fault Tolerant Systems are charted in (at least) the following references:
        - Fuchs '726
        - Damani '775

- IBM DB2 UDB
    - On information and belief, this product package was invented, purchased, evaluated, compared, tested, implemented, made, used (publicly and/or commercially), disclosed, offered for sale, and/or sold by IBM in the United States at least as early as 2003.
    - SAP's current understanding of the design, implementation, and capabilities of the IBM DB2 UDB are charted in (at least) the following references:
        - Chen, "DB2 UDB Evaluation Guide for Linux and Windows"
        - Chen, "DB2 UDB Exploitation of the Windows Environment"

- IBM DB2 UDB
    - On information and belief, this product package was invented, purchased, evaluated, compared, tested, implemented, made, used (publicly and/or commercially), disclosed, offered for sale, and/or sold by IBM in the United States at least as early as 2003.
    - SAP's current understanding of the design, implementation, and capabilities of the IBM DB2 UDB are charted in (at least) the following references:
        - Chen, "DB2 UDB Evaluation Guide for Linux and Windows"

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 28 of 101

        - Chen, "DB2 UDB Exploitation of the Windows Environment"

- Oracle 9i XML

    - On information and belief, this product package was invented, purchased, evaluated, compared, tested, implemented, made, used (publicly and/or commercially), disclosed, offered for sale, and/or sold by Oracle in the United States at least as early as 2001.

    - SAP's current understanding of the design, implementation, and capabilities of the IBM DB2 UDB are charted in (at least) the following references:

        - Melnick, Jack, "Oracle9i XML Developer's Kits Guide - XDK, Release 2 (9.2)"

        - Upton '575 App.

D. Admitted Prior Art

The applicant expressly or implicitly admitted that certain elements recited in Asserted Claims of the Asserted Patents were known in the prior art and thus part of the state of the art. These admissions include, but are not limited to, the following prior art concepts. SAP reserves the right to identify additional examples of admitted prior art and to further support the admissions identified below by relying on additional portions of the patent specification, statements made during the prosecution history of the Asserted Patents and the prosecution history of any related applications, and any statements by the Valtrus or the patent applicants.

Patent	Admissions by Applicant
'409 Patent	The '409 Patent admits in its Background section that "with the advent of standardized architectures and operating systems, computers soon became virtually indispensable tools for a wide variety of business applications." '409 Patent at 1:26-29. The '409 Patent further admits in its Background section that "user interfaces" were known. '409 Patent at 1:30-31. The '409 Patent further admits in its Background section that both "standalone" and "mainframe" systems were known, including mainframe systems in which "users utilized 'dumb' terminals to provide input to and to receive output from the

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 29 of 101

Patent	Admissions by Applicant
	mainframe computer while all processing was done centrally by the mainframe computer." '409 Patent at 1:34-42. The '409 Patent further admits in its Background section that "personal computers" and "servers" were known, including servers that were "multi-processor computers that couple numerous personal computers together in a network." '409 Patent at 1:46-50. The '409 Patent further admits in its Background section that computers and servers "rely on microprocessors, associated chip sets, and memory chips to perform most of their processing functions," and that these "devices are integrated circuits formed on semi-conducting substrates." '409 Patent at 1:51-56. The '409 Patent further admits in its Background section that "mass data storage devices" were known. '409 Patent at 1:58-65. The '409 Patent further admits in its Background section that "a variety of different memory devices available for use in microprocessor-based systems" were known, including "Dynamic Random Access Memory (DRAM) devices" and "Static Random Access Memory (SRAM) devices." '409 Patent at 1:65-2:12. The '409 Patent further admits in its Background section that "cache memory," "special high-speed Storage mechanism which may be provided as a reserved section of the main memory or as an independent high-speed storage device," was known and could be "a portion of the memory which is made of the high speed SRAM rather than the slower and cheaper DRAM which is used for the remainder of the main memory" and was "effective since most computer systems implement the same programs and request access to the same data or instructions repeatedly." '409 Patent at 2:12-24. The '409 Patent further admits in its Background section that memory caches could be "built into the architecture of the microprocessor themselves, such as the Intel 80486 microprocessor and the Pentium processor," and that such "internal caches are often called level 1 (L1) caches." '409 Patent at 2:25-28. The '409 Patent further admits in its Background section that "many computer systems also include external cache memory or level 2 (L2) caches," which "sit between the central processing unit (CPU) and the DRAM," and are "a separate [c]hip residing externally with respect to the microprocessor." '409 Patent at 2:28-33. The '409 Patent further admits in its Background section that known memory caches were "an area of memory which is made of Static RAM to facilitate rapid access to often used information." '409 Patent at 2:33-39.

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 30 of 101

Patent	Admissions by Applicant
	The ’409 Patent further admits in its Background section that in known systems “frequently accessed data may be stored in the cache memory area of main memory,” and “the portion of the system which is accessing the main memory should be able to identify what area of main memory it must access to retrieve the required information.” ’409 Patent at 2:40-44. The ’409 Patent further admits in its Background section that in known systems “a ‘tag RAM’ identifies which data from the main memory is currently stored in each cache line,” that “data is stored in the cache,” that “the values stored in the tag RAM determine whether the actual data can be retrieved quickly from the cache or if the requesting device will have to access the slower DRAM portion of the main memory,” that “[t]he size of the data store determines how much data the cache can hold at any one time,” that “[t]he size of the tag RAM determines what range of main memory can be cached,” and that “[m]any [known] computer systems, for example, are configured with a 256k L2 cache and tag RAM that is 8 bits wide,” which is “sufficient for caching up to 64 MB of main memory.” ’409 Patent at 2:45-56. The ’409 Patent further admits in its Background section that in a known “multi-processor system, each processor may have a corresponding main memory, with each main memory reserving a portion for cache memory,” hat “cache coherence” could be use “for managing the caches of a multi-processor system so that no data is lost or over-written before the data is transferred from a cache to a requesting or target memory, that “each processor may have its own memory cache that is separate from a larger shared RAM that the individual processors will access” and “[w]hen these multi-processors with separate caches share a common memory, it is necessary to keep the caches in a state of coherence by insuring that any shared operand that has changed in any cache is changed throughout the entire system.” ’409 Patent at 2:56-3:4. The ’409 Patent further admits in its Background section that in known systems “[c]ache coherency is generally maintained through either a directory based or a snooping system,” that (1) in “directory based system, the data being shared is placed in a common directory that maintains the coherence between the caches,” that “the directory acts as a filter through which the processor must ask permission to load an entry from the primary memory to its cache” and “[when an entry is changed, the directory either updates or invalidates the other caches with that entry,” which “disadvantageously . . . add[s] to the cycle time (previously reduced by the implementation of cache memory) by requiring that each access to the cache memory go through the common directory,” and that (2) in “snooping systems, all caches on a bus monitor (or snoop) the bus to determine if they have a copy of the block of data that is requested on the bus” and “[e]very cache has a copy of the sharing status of every block of physical memory it has.” ’409 Patent at 3:5-20.

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 31 of 101

Patent	Admissions by Applicant
	The ’409 Patent further admits in its Background section that known “cache coherence aims at solving problems associated with sharing data in a multi-processor computer system which maintains separate caches,” and that “[i]n a multi-processor-bus shared memory system, a host controller must maintain memory coherency throughout all the processor caches,” which “requires snoop cycles to be run on buses other than the originating bus.” ’409 Patent at 3:21-28. The ’409 Patent further admits in its Background section that a “[s]noop filter may be implemented to minimize the amount of snoop cycles on other buses, “ and “[t]o maintain efficiency, the snoop filter should facilitate data look up from the tag RAMs as quickly as possible to determine the proper snoop response on the processor bus in a minimal number of clock cycles.” ’409 Patent at 3:28-34. The ’409 Patent further admits that the components and arrangement of the exemplary multiprocessor-bus computer system in Figure 1 were known, including “one or more processors or CPUs,” “a split bus configuration in which [some] processors are coupled to a first bus, whereas [other] processors are coupled to a second bus,” known processors “available from Intel, AMD, or Motorola,” “individual bus” arrangements,” “Intel Pentium III processors,” buses that “operate at 100/133 MHz,” buses “coupled to a chip set which includes a host controller and a data controller,” in which “the data controller is effectively a data cross bar slave device controlled by the host controller,” “memory controllers” coupled to the data/host controllers and “a segment of main memory designated,” “dual inline memory modules (DIMMs),” a “a single memory cartridge which may be removable,” “a “4+1 parity striping pattern wherein one of the memory cartridges is used to provide redundancy, “an area of cache memory,” “bridges,” which may be “a variety of suitable [known] types such as PCI, PCI-X, EISA, AGP, etc,” and “an input/output (I/O) bus.” ’409 Patent at 4:3-53. The ’409 Patent further admits that “content addressable memory (CAM)” and READ and WRITE requests into memory were known, and it was further known that “a CAM request is issued to insure that the READ and WRITE requests are performed only when necessary and according to proper dependencies.” ’409 Patent at 5:37-46. The ’409 Patent further admits that those skilled in the art would appreciate that “basic cache protocol dictates that data be one of the four types: modified, exclusive, shared, or invalid (MESI)” and that owned data “refers to data that is either modified or exclusive.” ’409 Patent at 6:59-63. The ’409 Patent further admits that a “first-in-first-out (FIFO)” list structure “such that requests are processed in the order in which they were received, thereby fulfilling the ordering requirements for the WRITE requests” was “simple

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 32 of 101

Patent	Admissions by Applicant
	processing scheme is generally adequate for the WRITE requests since they are generally less time critical than the READ requests." '409 Patent at 8:19-25.
'244 Patent	The '244 Patent admits in its Related Art section that in the known art of computing "a distributed application is an application that is separated into two or more parts, such as a client application on a first computer system and a server application on a second computer system, with the two computers coupled together via a network," that the known term "'client'" refers to an entity that requests a service, and the [known] term 'server' refers to the entity that fulfills the request," that these entities "can be a an application, i.e., a client application or a server application," or "can be a computer system coupled to a network, i.e., a client computer system or a server computer system," and that it is know that a "computer systems coupled to a network may also be referred to as 'nodes.'" '244 Patent at 1:25-39. The '244 Patent further admits in its Related Art section that a known example of a distributed application would be "a distributed application that allows a customer to order a product over the Internet from an on-line retailer," where "[the customer accesses the distributed application using a web browser," "[t]he web browser communicates over the Internet with a web server, which provides the customer with a catalog of products that can be ordered, and provides a 'shopping basket' that allows the customer to select the products that the customer wishes to purchase," and if "the customer decides to complete the order, and pay for the order with a credit card," [t]he web server must communicate as a client with a server application that verifies that the credit card is valid, and posts the purchase to the customer's credit card account," next "the web server must also communicate with an application that delivers the order to the warehouse so the order can be shipped," and "the web server may communicate with an inventory control application to verify that the products ordered are in stock, and to order replacement inventory from the vendor, and finally "[i]f the customer checks back latter to view the status of the order, the web server may communicate with an application maintained by the shipping company to provide the customer with a tracking number." '244 Patent at 1:40-63. The '244 Patent further admits in its Related Art section it was known that "[t]o ensure that all applications communicate seamlessly and reliably in a distributed application, the application designer may use a middleware product that distributes applications across multiple platforms, databases, and operating systems using message-based communications and, if desired, distributed transaction processing," and that such "[m]iddleware products are used with client server applications to distribute processing among multiple servers, manage distributed transactions, and integrate multiple database platforms." '244 Patent at 2:4-13. The '244 Patent further admits in its Related Art section that "[m]iddleware systems are sometimes known in the art as 'on-line transaction processing' (OLTP)

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 33 of 101

Patent	Admissions by Applicant
	systems, and that "[o]ne such system is Bea Tuxedo, which is a product of BEA Systems, Inc.," which "provides an application designer with a series of messaging paradigms" including "conversational communication, event-based communication, queue-based communication, request/reply communication, and unsolicited communication." '244 Patent at 2:13-22. The '244 Patent further admits in its Related Art section that the known conversational communication paradigm "allows messages to be exchanged between clients and servers in a manner analogous to human conversation," and is "implemented using [known] inter-process communication (IPC) message queues," which are "typically implemented in transient memory areas, and are typically provided by the underlying operating system and are used for communication between clients and servers" and "can be used to pass messages between client and server applications operating on the same computer system or on separate computer systems coupled by a network." '244 Patent at 2:22-33. The '244 Patent further admits in its Related Art section that in the known conversational communication paradigm "a number of messages pass back and forth between the client and server until a conclusion is reached," that "[o]ver the course of the communication, both sides 'remember the point (or state) of the conversation so that relatively long operations, such as ad hoc queries, reports, and file transfers, can be supported," and that "the context of any particular message is interpreted in view the previous messages comprising the conversation." '244 Patent at 2:34-42. The '244 Patent further admits in its Related Art section that the known event-based communication paradigm "uses an event broker to transfer messages," where "[t]he event broker provides a communication paradigm in which message suppliers can post messages for message subscribers" and "acts like a newspaper delivery person who delivers newspapers only to customers who have paid for a subscription." In addition, "[e]vent generators inform the event broker of events (such as changes and problems) as they occur," which "is called posting an event." "The event broker then matches the name of the event to an event name associated with a list of subscribers, and notifies each subscriber on the list of the event by passing a message to the subscriber," and "[c]ommunication between the suppliers, subscribers, and event broker is provided by IPC message queues." In addition, "[b]ecause client and server processes that use the event broker communicate with one another based on a set of subscriptions, this paradigm is also known in the art as publish-and-subscribe communication." '244 Patent at 2:42-59. The '244 Patent further admits in its Related Art section that the known queue-based communication paradigm "requires persistent storage of data" and "allows any client or server to store messages in queues, and guarantees that any stored message will be delivered to the destination." It was also known that

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 34 of 101

Patent	Admissions by Applicant
	"[q]ueues can be ordered as last-in first-out (LIFO) or first-in first-out (FIFO), or on the basis of time or priority" and that a "collection of queues is administered and referred to as a single entity known as a queue space." '244 Patent at 2:60-67. The '244 Patent further admits in its Related Art section that is was known that "[q]ueue-based communication is appropriate when communication can occur in a time-independent fashion, " which "is a characteristic of programs that operate independently from one another and do not need to synchronize their communications." It was also known that "[t]ime independent programs synchronize with each other by leaving messages in application queues," and "[b]ecause queued messages are stored using persistent media, such as a hard disk drive, queue-based communication is highly reliable and messages can even be delivered after failures, such as power outages or network interruptions." It was further known that "[e]ven though queue-based messages pass through persistent storage, server applications and client applications enqueue and dequeue messages by sending the messages to a queue administrator," which "can reside on the same computer as either the server or client application, or can reside on a third server." '244 Patent at 3:1-17. The '244 Patent further admits in its Related Art section that the known request/reply communication is "implemented using inter-process communication (IPC) message queues," where "[e]ach server is assigned an IPC message queue called a request queue, and each client is assigned an IPC message queue called a reply queue." It was further known that "a client application can send requests to the server by putting those requests on the server's queue, and then check and retrieve messages from the server by retrieving messages from its own reply queue." It was further known that "[r]equest/reply communication is typically carried out in either a synchronous mode or an asynchronous mode," that in "a synchronous mode, a client sends a request to a server, which performs the requested action while the client waits," then the server "sends the reply to the client, which receives the reply," and that in "asynchronous mode, the client does not wait for a server to complete a service request before the client undertakes other tasks, but rather "after issuing a request, the client performs additional tasks (which may include issuing more requests to the server)" and "[w]hen a reply to the first request is available, the client retrieves it from its reply queue." '244 Patent at 3:17-36. The '244 Patent further admits in its Related Art section that the known unsolicited communication "is a type of communication that allows a client or server to receive a message that it never requested, thereby making it possible for applications to receive notification of application-specific events as they occur without having to request notification." It was further known that "[u]nsolicited messages can be sent to a single server node or client node, or be broadcast to a group of nodes," e.g., "a server may alert a single client that the account about which the client is inquiring

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 35 of 101

Patent	Admissions by Applicant
	has been closed, or a server may send a message to all the clients to notifying the clients that the server will be shut down for maintenance at a specific time." It was further known that "unsolicited messages can be sent either with or without guaranteed delivery" and are "[s]ent using IPC message queues." '244 Patent at 3:37-50. The '244 Patent further admits in its Related Art section it was known that some messaging paradigms "use transient media, such as network connections and system memory, to pass messages between clients and servers," while other use "persistent media, such as a hard disk drive." '244 Patent at 3:51-57. The '244 Patent further admits in its Related Art section it was known that "[t]o ensure that a distributed application has a high rate of availability, it is important to make each component that hosts the distributed application as reliable and fault-tolerant as possible" because "messaging is critical in a distributed application, and two components critical in the communication of messages are the persistent storage media, such as the hard drives, and the transient communication network." Thus, it was known that "a designer of a distributed application will often specify that the application be implemented using highly reliable and fault tolerant interconnection fabrics and storage systems." '244 Patent at 3:65:4:9. The '244 Patent further admits in its Related Art section that it was known "[s]everal interconnection fabrics are available to provide guaranteed delivery of packets," such as ServerNet, which is "a system interconnect architecture available from Compaq Computer Corporation." It was known that "ServerNet hardware ensures data integrity using multiple techniques," e.g., "command link integrity isolates single-bit errors, cyclic redundancy checks maintain both data and control integrity of transfers crossing the interconnect fabric, and hardware protocol acknowledgments ensure that end-to-end reliable data transfer has occurred." In addition, it was known that "ServerNet is capable of providing a high level of availability by incorporating spare alternate paths within a primary interconnection fabric, and providing a fully redundant secondary interconnect fabric with redundant Secondary attachments to network nodes." It was also known that "[s]imilar interconnection fabrics are available from other vendors, such as the Coupling Facility provided by IBM Corporation." '244 Patent at 4:9-27. The '244 Patent further admits in its Related Art section that "fault tolerant storage systems (FTSS), such as the SureStore(R) XP512 Disk Array, which is a product of Hewlett-Packard Company," were known and "guarantees the availability and integrity of files stored by the FTSS." It was also known that "[f]ault tolerant storage systems are also available from other companies, such as Hitachi Data Systems Corporation and EMC Corporation." '244 Patent at 4:27-34. The '244 Patent further admits in its Related Art section it was known that "an

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 36 of 101

Patent	Admissions by Applicant
	FTSS is coupled to a server using a high speed interface, such as an Ultra 160 SCSI interface, a fiber channel interface, or an enterprise system connectivity (ESCON) interface," and "[s]uch systems are highly reliable and fault tolerant." It was further known that "the SureStore(R) XP512 Disk Array uses a fault-tolerant, redundant architecture that ensures there is no single point-of-failure, and has a mean time between failure (MTBF) of 2.5 million hours, or alternatively 285 years." Such known systems are acknowledged by the patent to be "incredibly fast," such that a "single fiber channel port can support transfer rates of 100 megabytes per Second, and ports can be ganged together to increase transfer rates even further, and "the internal crossbar architecture of the XP512 has a bandwidth of 6.4 gigabytes per second." '244 Patent at 4:34-48 The '244 Patent further admits that the components and arrangement of the exemplary FTSS in Figure 1 were known, highly reliable. and could "be used to host a distributed application." The components of the known system include: "computer systems" coupled to a "fault tolerant storage system" via a "FTSS interconnection fabric," "to carry file transactions between the computer systems and FTSS." It was further known that this "interconnection fabric couples each computer system directly to the FTSS, but does not directly couple the computer systems to each other." It was also known that the computer systems 12, are coupled to together by highly reliable, fault tolerant network interconnection fabric to carry messages between the computer systems." '244 Patent at 4:49-61 The '244 Patent further admits that those skilled in the art "will recognize that other network nodes may be coupled to FTSS via fabric, such as printers, scanners, backup systems, and the like," and that "computer systems may be coupled to each other and to other computers via another interconnection fabric, such as an ethernet network, which in turn may be coupled to the Internet via a gateway." '244 Patent at 6:34-41. The '244 Patent further admits it was known that a "interconnection fabric will be comprised of high-speed interfaces and related cabling used to connect computer systems to storage systems, such as small computer system interfaces (SCSI), fiber channel interfaces, or enterprise system connectivity (ESCON) interfaces," and that in "a typical FTSS, these interfaces tend to connect each computer system directly to the FTSS, but do not connect the computer systems to each other." '244 Patent at 6:42-50. The '244 Patent further admits it was known that "a typical FTSS, such as the SureStore(R) XP512 Disk Array, which is a product of Hewlett-Packard Company," "has a battery-protected fully redundant nonvolatile write cache that can range in size from 2 gigabytes to 32 gigabytes." And it was known that in this system "as soon as a message is received by FTSS from a sending computer system, the message is committed to the nonvolatile write cache" and then "the

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 37 of 101

Patent	Admissions by Applicant
	message is written to a redundant array of independent disks (RAID) of FTSS, and processed by one of the message agents." '244 Patent at 6:58-67. The '244 Patent further admits that the components and arrangement of the prior art computer system in Figure 3 were known, including "client and server applications that use middleware messaging," which "pass messages to other nodes using an application to-transaction monitor interface (ATMI)" and is part of middleware product, such as Bea Tuxedo." It was also known that the "ATMI provides a series of functions that may be called by the client and server applications to pass messages." '244 Patent at 7:1-13. The '244 Patent further admits that the components and arrangement of the prior art computer system in Figure 3 were known including "the messaging paradigms supported by [a] middleware product." This would include a "conversational communication paradigm, a "event-based communication paradigm," a "queue-based communication paradigm," a "request/reply communication", and a "unsolicited communication paradigm," which "communicates with the I/O services of the operating system . . . to transmit messages" between nodes and thus "communicates with network I/O block to send and receive messages from other network nodes via network fabric." '244 Patent at 7:14-27.
'182 Patent	The '182 Patent admits in its Background section it was known that "[r]emote mirroring is a data redundancy technique for coping with storage system failures," in which "[a] copy of data, sometimes referred to as a primary or local copy, is updated, for example, as it is accessed by an application program" and "[a] redundant copy of the data, sometimes referred to as a secondary or slave copy of the data, usually at a remote site, is updated as well." In addition, it was known that "[w]hen a failure occurs that renders the primary copy unusable or inaccessible, the data can be restored from the secondary copy, or accessed directly from there." '182 Patent at 1:31-41. The '182 Patent further admits in its Background section that "[c]onventional techniques for remote mirroring tend to maintain the primary and secondary copies of the data synchronized." '182 Patent at 1:42-45. SAP further incorporates by reference the Background sections in applicant's related applications ('182 Patent at 1:1-25) as if fully set forth herein. The '182 Patent further admits that the invention could be implemented in known computers system, such as "any computer system in which a primary copy of data is backed up by data that is redundant of the primary copy." In such known systems, "the primary copy may be stored at a primary data storage facility, while redundant data may be stored at one or more secondary storage facilities." Known "data storage facilities can include any type of data storage, such as volatile or non-

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 38 of 101

Patent	Admissions by Applicant
	volatile memory, including random access memory, flash memory, magnetic tape or disk, an array of disk drives and so forth." In addition, the known storage facilities could be "are positioned at different locations, which are generally remote from one another," and thus be connected via known techniques, including "via a network or via a direct communication link," such as known "local area networks (LANs), metropolitan area networks (MANs), wide area networks (WANs), storage area networks (SANs), the Internet and so forth." '182 Patent at 3:10-25. The '182 Patent further admits that known "[a]dditional devices, such as one or more computer(s) (e.g., a host computer, a workstation or a server), may communicate with the primary data storage facility." '182 Patent at 3:31-35. The '182 Patent further admits that known or would have been readily apparent to one of skill in the part that "[o]ne or more applications operating at the computer may access the primary data storage facility for performing write or read transactions to or from data objects, such as files or storage volumes, stored at the facility," and that "[m]ore particularly, the computer may retrieve a copy of a data object by issuing a read request to the facility." In addition, it was known or readily apparent that "[w]hen a data object at the computer is ready for storage at the facility, the computer may issue a write request to the facility," e.g., "[t]he computer may request storage of a file undergoing modification by the computer." In addition, it was known or readily apparent that "[w]hile a single computer is illustrated in FIG. 1, it will be apparent that multiple computers may access the data storage facilities, " and that each "computer system may include any number of devices that retrieve, modify and/or generate data and any number of primary and secondary storage facilities." In addition, it was known or readily apparent that "a device, such as a workstation or server, may also function as a storage facility," and that "a storage facility may function as a primary storage facility for Some data and as a secondary storage facility for other data, and a storage facility may function as a computer system, generating storage requests (e.g., as part of a backup process)." '182 Patent at 3:41:63. The '182 Patent further admits various techniques for the storage of redundant data were known, including "a mirrored copy of the data," "a redundancy scheme in which redundant data is distributed among or striped across multiple storage devices or facilities," and "Redundant Array of Inexpensive Disks (RAID) techniques, such as RAID levels 2, 3, 4 or 5." It was also known or readily apparent to those of ordinary skill that "one or more additional secondary storage facilities may be provided, in which each stores only a portion of the data stored at the primary (thus, proving a distributed redundant copy) or where each stores a complete copy of the data (thus, providing multiple redundant copies)." '182 Patent at 4:1-16. The '182 Patent further admits that known or would have been readily apparent to

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 39 of 101

Patent	Admissions by Applicant
	one of skill in the part that "the appliances 202 and 204 may be implemented by (amongst other examples) appropriately configured hardware, software or firmware in disk arrays, storage devices, hosts (e.g., computer 108), in-host I/O bus adapters, network switches, network hubs, or combination thereof, which may be dedicated to perform the functions of the appliances 202 and 204 as described herein, or which may have shared functionality." '182 Patent at 4:34-41. The '182 Patent further admits the invention could leverage known technology such as "a dedicated storage device (e.g., a disk drive, disk array or section of non-volatile memory (NVRAM)) . . . accessible via a Storage Area Network (SAN), and may be shared with other uses." '182 Patent at 5:11-18. The '182 Patent further admits that known or would have been readily apparent to one of skill in the part that "[t]he primary and secondary storage controllers may be replicated, distributed, mirrored, or otherwise constructed using any of the techniques known in the art for building storage systems." '182 Patent at 5:45-48. The '182 Patent further admits the invention could leverage known technology such as a "first-in, first-out buffer (FIFO) for write transactions." '182 Patent at 5:58-60. The '182 Patent further admits the invention could leverage known technology such as "known techniques for data compression." '182 Patent at 15:30-33. The '182 Patent further admits the invention could leverage known technology to commits "batches to storage at approximately the same point in time," including "[w]ell-known techniques such as 'two-phase commit.'" '182 Patent at 25:15-20.
'575 Patent	The '575 Patent admits in its Background section it was known that "[o]ne aspect of real-time enterprises is a capability to materialize data from disjointed databases into an integrated data model," and "[m]any problems, such as synchronization of master data, cannot be solved effectively by a federated database approach alone." In addition, it was known that "[d]ata elements are deduplicated and merged into a common data model to create a semantic bridge between systems," and "[e]xisting tools and methods operate in batch mode to support business intelligence applications," and additional tools were "available to support real-time information integration." '575 Patent at 1:5-18. The '575 Patent further admits in its Background section it was known that "[l]atency, an inability to react immediately to business stimuli, can contribute to basically any deficiency in business performance, for example poor customer service, missed selling opportunities, failure to address consumer fraud, insufficiency in monitoring enterprise finances, and the like." It was further known that "[a] zero latency enterprise (ZLE) performance has been sought to enable enterprises to eliminate latency from operations so that business events that occur

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 40 of 101

Patent	Admissions by Applicant
	anywhere in an organization can immediately trigger appropriate actions across other parts of the enterprise and beyond" and that "[e]limination of operational inconsistency is sought to enable users to gain real-time consolidated performance and enable the enterprise to become more responsive and competitive." '575 Patent at 1:18-30. The '575 Patent further admits in its Background section it was known that "[o]ne technique that has been attempted to attain a low latency performance relies on standard applications to supply data services using a standard data model," "[a]nother technique attempts to customize a data model without recoding applications through usage of table-driven code," and "[a]nother attempted solution is usage of user-exits to evade limitations of table-driven approaches." '575 Patent at 34-45. The '575 Patent further admits that a known example "a real-time infrastructure is Supply Chain from Hewlett-Packard of Palo Alto, Calif., which operates in a distributed fashion, with geographies and business units having different business processes," and that to "respond to customers and suppliers more effectively, a real-time computing infrastructure is implemented which maps data from many of the hundreds of Systems, Applications, and Products (SAP) instances into a common data model, embodied in a real-time data store." It was further known that Defendant "SAP of Walldorf, Germany supplies enterprise systems," and that "[t]he result is a unified view of the Supply Chain, up to the current minute, that attains an ability to manage Supply globally, enabling more efficient pricing, supplier contracts, and inventory turns." '575 Patent at 2:45-59. The '575 Patent further admits that the invention could be implemented in a known "real-time computing architecture with a capability to supply a solution that makes an enterprise more adaptive as a business by supplying a capability to integrate disparate enterprise applications in real time, addressing business level flexibility and timeliness," and that a known "enterprise system [such as SAP] is a computing environment or model that includes multiple interlinked servers and networks in which multiple users access applications and data stored on a server." '575 Patent at 2:59-67. The '575 Patent further admits that a known "real-time infrastructure has one or more of several desirable characteristics including an extreme adaptability of the data model, allowing rapid customization," including "relationships between source data and a central data model, [which] are described as metadata . . . support for cleansing, enrichment, integration, and aggregation of data for use by subscribing applications, a capability for mapping and translating data and messages from numerous structures and database technologies into a common data model." Other known "characteristics include a simple and open subscription service, security and integrity of data in the real-time data store, and a capability for synchronous and asynchronous delivery of inbound and outbound data." '575

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 41 of 101

Patent	Admissions by Applicant
	Patent 3:1-22. The ’575 Patent further admits it was known that “[d]ata cleansing, which may otherwise be termed data scrubbing, is the process of amending or removing data in a database that is incomplete, incorrect, improperly formatted, or duplicated,” and that in “a data intensive application such as telecommunications, transportation, banking, insurance, or retailing, data cleansing is used to systematically examine data for flaws using rules, algorithms, data relationships, such as look-up tables, and the like.” ’575 Patent at 3:10-19. The ’575 Patent further admits that the invention utilizes known technology in which “[a]n integrated set of services called a real time information director (RTID) has been developed to address performance and functionality of a real-time enterprise,” in which the “real time information director is responsible for most or all data input and output to the real-time data store” and “receives and sends data in the form of eXtended Markup Language (XML) documents.” It was further known that “the real time information director is implemented in the Java language and runs through WebLogic ServerTM from BEA of San Jose, Calif.” and that “[t]he real time information director is accessed synchronously via HyperText Transport Protocol (HTTP) and asynchronously via Java Message Service (JMS).” It was further known that “Hewlett-Packard's Open ViewTM manages the real time information director through standard Java 2 Enterprise Edition (J2EE) and NonStop WebLogic Server (WLS) mechanisms” and the “real time information director interoperates with various Enterprise Application Integration (EAI) platforms and middleware, such as SAP Netweaver XITM from SAP of Walldorf, Germany, various programs from Web MethodsTM of Fairfax, Va., RendezvousTM from TIBCO Software, Inc. of Palo Alto, Calif., BEA eLinkTM and HP Service BusTM.” It was further known that the “EAI platforms supply adapters to many other applications that feed or consume data from the real-time data store.” ’575 Patent at 3:21-45. The ’575 Patent further admits that the invention utilizes known technology in which the “real time information director prepares and caches Java Database Connectivity (JDBC) statements for each inbound or outbound document class.” And that a “document disassembler contains prepared statements for inserting or updating various records related to a particular class of inbound documents into the data store,” and a “document assembler contains prepared statements for selecting various records related to a particular class of outbound documents from the data store.” In addition, the invention utilizes known technology to “instantiate and cache for reuse as many disassemblers and assemblers of each document class as is appropriate to handle peak concurrent demand.” ’575 Patent at 3:46-57. The ’575 Patent further admits that the invention utilizes known technology in which “[e]ach class of documents is defined through descriptive metadata,” and

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 42 of 101

Patent	Admissions by Applicant
	"[a]ssemblers and disassemblers are created on-the fly, based entirely on the descriptive metadata and on the schema of the tables read on demand from the database." In addition, it was known that "[b]ecause the metadata is descriptive rather than procedural, the same metadata is used to build both assemblers and disassemblers of the same document class." '575 Patent at 3:58-64. The '575 Patent further admits that the invention utilizes known technology in which "[m]etadata is expressed in Java, mainly with nested Java constructors," and "[n]ew Java metadata subclasses are created as appropriate to handle novel criteria. It was further known that "metadata classes extensively use polymorphism," that "[f]ormat metadata classes map documents from externally-defined representations, such as SAP IDocs, to a common data model," "content metadata classes describe the relationships between the various records and tables that contribute to a particular document, and other "metadata classes invoke various data services and cleanse or enrich the document, either before insertion into the real-time data store, or when assembling an outbound document." '575 Patent at 3:65-4:9. The '575 Patent further admits that the invention utilizes known technology in which "[d]escriptive metadata is typically very concise in comparison to procedural code," e.g., "real time information director (RTID) metadata for individual SAP IDocs is typically about one-tenth the size of the eXtensible Stylesheet Language Transformations (XSLT) style sheets that have been created to map the IDoc to the Real-Time Supply Chain (RTSC) data model." '575 Patent at 4:26-34. The '575 Patent further admits that the invention utilizes known technology in which "[p]olymorphic metadata can be used to enable extension of the real time information director to facilitate and address new functionality and behaviors." It was further known that "[p]olymorphic metadata is metadata that takes many forms, using polymorphism to flexibly represent different patterns economically and facilitate evolution of metadata as new circumstances arise," and "[g]enerally, an individual metadata class can be used to represent a different common pattern, defined with attributes that are specific to the pattern," e.g., "circles and rectangles can be assigned to different classes of shape with circle having a defining attribute called diameter, and rectangle having defining attributes called length and width." It was further known that "polymorphic representation is economical because specified attributes or parameters of metadata can be limited to those that are applicable to a specific pattern under consideration," and "[n]ew metadata classes can be rapidly generated to solve new problems outside of the patterns previously encountered." '575 Patent at 4:34-50. The '575 Patent further admits that the invention utilizes known technology in which "polymorphic metadata can be expressed in Java, enabling usage of descriptive language for new classes of metadata to be implemented at the same time as the behavior that carries out that metadata," and the "descriptive power of

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 43 of 101

Patent	Admissions by Applicant
	the metadata can be embodied in Java constructors." '575 Patent at 4:51-56. The '575 Patent further admits that the invention utilizes known technology in which "[i]n a Java implementation, individual classes of real time information director (RTID) metadata can be implemented as distinct Java classes." It was further known that "[p]arameters passed to the constructors for each metadata class serve to describe the metadata" and "[o]ther methods of metadata classes are called to carry out the functions of the metadata." It was further known that a "new class of metadata is most frequently created by creating a new subclass of an existing metadata class," in which the "subclass can be used in any context in which the superclass could be used," and "[a]dditional parameters can be defined for the sub-class, which can then be used within the implementation of any methods that override the inherited behaviors of the superclass." '575 Patent at 4:57-5:5. The '575 Patent further admits that "Siebel Systems, Inc., of San Mateo, Calif., supplies [known] Customer Relationship Management (CRM) and business intelligence systems." '575 Patent at 5:29-31. The '575 Patent further admits that a known "realtime information director [cound be] is supplied by Hewlett Packard Company of Palo Alto, Calif. Hewlett Packard Company", which "also has a ZLE Development Kit, familiarly known as the ZDK, used by HP professional services and partners to build custom ZLE applications that run on a NonStopTM Server platform." '575 Patent at 29:7-12. The '575 Patent further admits that the invention utilizes known technology including the use of "a Blaze Advisor rules engine, which can supply offers based on business rules that are written and tested in Blaze Advisor Builder" and that " Blaze Advisor can be licensed from Fair Isaac Corporation of San Rafael, Calif. Blaze Advisor is incorporated into the real time information director by adding appropriate JavaTM Archive (JAR) format files obtained from Fair Isaac to the real time information director class path." '575 Patent at 29:20-30.
'139 Patent	The '139 Patent admits in its Background section it was known that "the use of networked computer software and the Internet has brought about a significant increase in the amount of network traffic and transactions performed by software applications residing on remote servers." In addition, it was known that "[m]ore information is stored by these networked applications and in remote database applications than ever before," and that "[t]hese applications process a large number of purchase transactions, credit card transactions, electronic mailing lists, email functions, data distribution, batch processing, etc." It was also known that "[t]hese systems contain very critical data and it must be backed up so that the information is not lost" and "application end users also desire that networked applications and data should be available 24 hours a day and 7 days a week." '139 Patent at 1:12-25.

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 44 of 101

Patent	Admissions by Applicant
	The ’139 Patent further admits in its Background section it was known that “computer systems must have redundant backup systems,” because “[i]t is inevitable that the primary system will fail on occasion.” It was also known that “[w]hen the primary system fails, a backup System must be quickly available,” and that a “backup system can be located on-site with the primary system and then a secondary backup system can be located at a physically remote backup site.” It was also known that “having at least one backup system on-site is valuable because the networked application can immediately failover to that application, if the primary system becomes inoperative,” and that “[t]his fast failover will be transparent to the user because it is local.” ’139 Patent at 1:26-27. The ’139 Patent further admits in its Background section it was known that a “second backup system at a remote Site is desirable because it protects against catastrophic failure at the primary site,” which is “sometimes called the standby site.” It was known that “[i]f the primary site is disabled by an extended power outage, fire, or flood then the remote standby system will be activated,” and that while a “failover to an off-site Standby System is slower, … it provides a maximum amount of protection against total system failure.” It was known that “this type of fail safe system is valuable for applications that are connected to the Internet which need to be constantly available.” ’139 Patent at 1:39-48. The ’139 Patent further admits in its Background section it was known that “[m]any online, transaction based systems store more than one copy of their data, “ which “is another safeguard against system failure or data corruption.” It was known that “the first copy is an original copy and the second is an archival copy,” and that the “archival copy is a backup but other times it is used for error checking purposes.” It was also know that “[s]ome systems can even store multiple backup copies.” ’139 Patent at 1:49-55. The ’139 Patent further admits in its Background section it was known that for “certain transactional systems, such as a database, an active transaction log is kept which tracks recent transactions,” and that an “archive log is then kept to store information from the active log after the active log has been filled or a certain time period has passed.” It was also known that “[t]o be able to mirror a transactional system between the primary site and the standby site both the active logs and then the archive logs must be transferred to the standby system,” where the “active logs are then entered into or applied to the standby system which constantly keeps the standby system current.” ’139 Patent at 1:55-65. The ’139 Patent further admits in its Background section it was known that [i]n the event of a failure, the standby system is always ready to take over,” and that “[u]sually, the standby system is located in another building or in a geographically remote area.” It was known that this setup “requires the active logs, archive logs, or backups to be transferred across a wide area network (WAN), which is relatively

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 45 of 101

Patent	Admissions by Applicant
	slow in comparison to a local area network (LAN) or a high speed cluster connection," and so "the data sent from the primary site across the WAN to the standby site can cause a significant amount of network congestion," especially "where these files can contain hundreds of megabytes of data per file." '139 Patent at 1:65-2:10. The '139 Patent further admits that it was known the invention could be implemented using a known "communications link," which was typically a known "wide area network (WAN), but a WAN is typically not as fast as a local area network (LAN) or a fast cluster connection," and that communications link could also be a known "wireless link." '139 Patent at 3:12-16. The '139 Patent further admits that is was "well known by those skilled in the art" that "redo log files store all the information needed to perform database recovery and they record every change made to the database structure," and "[w]hen the online redo logs are filled they are then archived and transferred into the archive log areas (i.e., archive data file)." '139 Patent at 4:49-55. The '139 Patent further admits that it was known the invention could be implemented using a known "local high performance, quick recovery, file system 62 (e.g., VXFS)," or a known "special file system generally called the archive replicator file system." '139 Patent at 4:65-5:3. The '139 Patent further admits that it was known the invention could be implemented using a known "UNIX device driver" and known "remote procedure calls (RPC)." '139 Patent at 5:30-40.
'738 Patent	The '738 Patent admits it was known that "[m]any critical systems, such as telecommunications networks, have essential elements which are required to function twenty-four hours a day, three hundred and sixty five days a year," and "[f]or many such systems the amount of acceptable down time is in the order of no more than a few minutes per year." It was also know that to "achieve this, critical systems are often designed to be fault tolerant, such that a fault or failure of a system or component of a system does not cause significant disruption to the services provided thereby," and that such "systems are often also referred to as high-availability (HA) systems." '738 Patent at 1:6-16. The '738 Patent further admits it was known that a "system may be arranged to be high-availability in a number of different ways, for example, through use of an active and standby system, or using a cluster of servers, as is well known in the art." It was also known that "[w]ith an active/standby system, in the event of a fault being detected in the active system, a switchover of the active and standby systems occurs such that the standby system becomes the active system, and vice versa," and as a result "services which were available before the fault was detected should

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 46 of 101

Patent	Admissions by Applicant
	still be available, albeit, potentially, after a short delay, once the switchover has occurred." '738 Patent at 1:16-26. The '738 Patent further admits it was known that "[d]ifferent levels of high-availability exist which may be split into two broad categories, referred to herein as service continuity and task preservation." It was known that "[s]ervice continuity refers to the ability to continue to use the services provided by a system after a fault or switchover of a high-availability system, whereas task preservation, a higher level of high-availability, refers to the ability for tasks being processed when a fault or switchover occurs to be largely unaffected by the switchover." '738 Patent at 1:26-35. The '738 Patent further admits it was known that "in a telephone network, a service may be the ability to establish calls between parties, and a task may be a call currently in progress," and in "this context, service continuity generally means that any calls in progress when a fault occurs will typically be dropped, whereas calls placed after the fault has occurred will be established in the normal manner in other words, the provision of the service is preserved, albeit after a short delay." It was also known that in "a task preservation system active calls will be maintained even during a switchover of an active/standby system." '738 Patent at 1:36-45. The '738 Patent further admits it was known that "[i]n order to provide task preservation a common storage element is often provided in addition to a high-availability configuration." It was also known that "[c]ontext data relating to each task is stored in the common storage area, and may be used in the event of a switchover for reinitializing the new active system with the context of any tasks which were in progress when the switchover occurred." '738 Patent at 1:46-52. The '738 Patent further admits it was known that "[i]n a telephony network, this context information may relate to the state of different protocol layers of a protocol stack as well as any application specific data related to individual calls," and that "[u]pon a switchover to a standby system, the newly activated system can recover the stored context data from the common storage element and rebuild the protocol stack and application context for calls open at the time of the switchover." By using these known system "processing of calls open at the time of a switchover may continue on the new active system without significant interruption." '738 Patent at 1:53-62. The '738 Patent further admits it was known that "the requirement for a common storage area for storing context data adds to the complexity and cost of such systems." '738 Patent at 1:63-65. The '738 Patent further admits the invention could be implemented using a known "session initiation protocol (SIP) network, in which case the obtained context

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 47 of 101

Patent	Admissions by Applicant
	information may be appended to a SIPTAG field, or to a SIP extension header." '738 Patent at 2:20-25. The '738 Patent further admits that the components and arrangement of the fault tolerant or high availability system of Figure 1 were known referring to the figure as "a fault tolerant or high availability system according to the prior art." The known components or arrangements in Figure 1 include a "telephone switch" that "communicates with a high-availability network element over a network to provide value added services or to control access to a network resource," and the "network may, for example, be an SS7 network, in which case the network element may, for example, be a service control point (SCP)." '738 Patent at 3:65-4:5. The '738 Patent further admits that the known components or arrangements in Figure 1 include a "network element," which "comprises two similar peer systems which are arranged in a known fault tolerant, or high-availability, configuration, in which one of the systems is arranged in an active mode, whilst the other system is arranged in a standby mode," so that "[i]n the event of a fault being detected in the current active system, a switchover will occur such that the current active system becomes the standby system, and vice-versa" and "[c]all processing may thus continue on the new active server." It was also known that "[s]witchover may also be initiated manually, for example to enable maintenance to be carried out on an active server." '738 Patent at 4:6-17. The '738 Patent further admits that the known components or arrangements in Figure 1 include that "[e]ach of the peer systems comprise numerous elements, such as an application and a protocol stack," and that the "systems also have access to a common storage element, such as a database." Use of this known system would include that "when calls are processed on the active server the application may decide to store context data in the storage element" and the "context data may relate, for each call, to both application context data and context data relating to one or more layers of the protocol stack." So, it was known that "[i]n the event of a switchover from the active server to the standby server, the stored context data may be retrieved by the application on the new active server, and be used to rebuild, for each call, the context of the application and the protocol stack," which "helps ensure that processing of calls open at the time of the fault is continued once the new active server has been initialized." '738 Patent at 4:18-33. The '738 Patent further admits the invention could be implemented using a known elements such as a "SIP user agent" and "a SIP back-to-back user agent (B2BUA) of a session initiation protocol (SIP) network." '738 Patent 4:66-5:2. The '738 Patent further admits the invention could be implemented using a known elements such as a "SIP INVITE message." '738 Patent 5:25-33.

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 48 of 101

Patent	Admissions by Applicant
’264 Patent	The ’264 Patent admits in its Background section it was known that “[m]odern integrated processor circuits of high performance are fabricated with at least some cache memory on the processor integrated circuit,” and “[t]ypically cache is designed as multiple blocks of memory cells, together with control logic.” It was also known that “[s]ome of these circuits have been designed with bonding options such that a portion of cache may be disabled; a technique that permits product differentiation as well as sale of partially defective circuits.” It was also known that “[s]ome of these circuits also have spare blocks of memory that can be substituted for defective sections of cache,” and “[t]ypically cache is designed as multiple blocks of memory cells, together with control logic.” ’264 Patent at 1:19-30. The ’264 Patent further admits in its Background section it was known that “modern software is written to take advantage of multiple processor machines” and “typically is written to use multiple threads.” It was also known that “[e]ach thread has a sequence of instructions that can be independently scheduled for execution,” and “[t]ypically, at any given time some threads may be in a ‘wait’ mode, where execution is delayed until some other thread completes an action or an external event occurs, while other threads may be ready for execution.” ’264 Patent at 1:30-38. The ’264 Patent further admits in its Background section it was known that “[s]oftware is also frequently able to prioritize those threads, determining which thread should receive the most resources at a particular time.” It was known that “the Windows 2000 (trademark of Microsoft), VMS (trademark of Compaq Computer), and UNIX operating Systems all maintain thread priorities, which are often derived from an administrator-set base priority,” and that “[t]hese operating Systems use these priorities to determine which threads should execute, and to determine an amount of time each thread should execute before it is preempted by another thread.” ’264 Patent at 1:38-47. The ’264 Patent further admits in its Background section it was known that in “a multiple processor machine, each processor may be tasked with executing different threads from among those threads that are ready for execution,” that “[t]hese threads may belong to the same, or a different, application program, or may be associated with system tasks,” and that “[s]uch machines are often capable of doing more useful work than machines having a single processor.” ’264 Patent at 1:49-55. The ’264 Patent further admits in its Background section it was known that “[m]ultithreaded processors are those that have more than one instruction counter, typically have a register set associated with each instruction counter, and are capable of executing more than one instruction stream.” A known example was that “machines are known wherein a single pipelined execution unit is timeshared among several instruction streams, and because “the execution unit is timeshared, each instruction stream tends to execute somewhat slowly.” It was also known that

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 49 of 101

Patent	Admissions by Applicant
	"[m]ultithreaded machines with a timeshared, single, execution unit appear to software as multiple, independent, processors." '264 Patent at 1:55-65. The '264 Patent further admits in its Background section that "[m]achines of superscalar performance, having multiple processors on single integrated circuits, where each processor is capable of dispatching multiple instructions in some cycles, are known." In addition, known "[m]achines of this type include the IBM Power-4 and the PA 8800," where "[t]ypically, each processor on these integrated circuits has its own dedicated set of execution unit pipelines and cache." It was known that such machines' "die area, and therefore cost, for execution units is therefore typically much greater than with a timeshared multithreaded machine." It was also known that these "superscalar multiple-processor circuits are also capable of executing multiple threads and can be regarded as a form of high performance multithreaded machine." '264 Patent at 1:65-2:10. The '264 Patent further admits in its Background section it was known that "[m]odern processor integrated circuits are frequently fabricated with cache memory," which "offers substantially faster access than main memory; but offers that fast access only for information found in the cache." It was also known that "[m]emory references that are found in cache are called 'hits' in the cache, while references not found in cache are called cache 'misses,'" and the "ratio of cache hits to total memory references is the 'hit rate,' and is known to be a function of cache size, cache architecture including the number of ways of associativity of the cache, and the nature of the executing thread." '264 Patent at 2:11-20. The '264 Patent further admits in its Background section it was "known that cache hit rates can be measured by using counters to count cache hits and memory references," and such "counters can be read and a hit rate computed." It was also "known that a low hit rate can drastically impair system performance." '264 Patent at 2:21-26. The '264 Patent further admits in its Background section it was "known that some threads require larger cache size to achieve high hit rates than others." It was "also known that processor performance can be adversely affected, sometimes seriously, by a low hit rate in cache," and so it was "necessary to provide sufficient cache to support high hit rates for all or most threads if maximum processor performance is to be attained." It was also known that "[l]arge cache sizes are, however, expensive, and "[m]anufacturers therefore market integrated circuits having similar processors with different cache sizes to different markets where application programs, and cache requirements, are expected to differ." '264 Patent at 2:26-37. The '264 Patent further admits in its Background section it was known that "[c]ache of multiple processor integrated circuits is typically limited in size by processing costs," and that "[l]arge integrated circuits typically have fabrication

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 50 of 101

Patent	Admissions by Applicant
	cost that is an exponential function of their circuit area, and in some circuits as much as half of the integrated circuit area is cache and cache memory control circuitry." '264 Patent at 2:38-43.. The '264 Patent further admits in its Background section it was known that "[m]ultiple-processor integrated circuits typically have predetermined amounts of cache allocated to each processor, and these "circuits therefore typically require an amount of total cache equal to the number of processors multiplied by the cache required to achieve a high hit rate on the most cache intensive thread expected to run." '264 Patent at 2:44-49. The '264 Patent further admits in its Background section that "[m]ultiple-processor and multithreaded machines are known that are capable of simultaneously executing multiple operating systems," which "are partitionable machines." It was also known that "[t]ypically, each operating System is run on a partition, where a partition is assigned one or more processors, suitable sections of main memory, and other system resources" and "[e]ach partition is typically configured as a virtual machine, which may have dedicated disk space or may share disk space with other partitions." It was known that "[m]achines exist that are capable of running Windows NT (Trademark of Microsoft) in one partition, while running UNIX in another partition," and "[m]achines also exist that are capable of simultaneously running several copies of the same operating system with each copy running independently in a separate partition." It was known that "[t]hese machines are advantageous in that each partition may be dedicated to particular users and applications, and problems (including system crashes) that arise in one partition need not adversely affect operation in other partitions." '264 Patent at 2:50-67. The '264 Patent further admits in its Background section it was "known that execution time on multiple-processor and multithreaded machines may be billed according to the number of processors, the amount of memory, and the amount of disk space assigned to each partition" and it was "also known that one or more multiple-processor or multithreaded integrated circuits may be used as processors in partitionable machines." '264 Patent at 3:1-7.

E. The Applicant's Own Prior Patents and Published Applications

No Asserted Claim of any Asserted Patents is entitled to be backdated before the actual filing date of the application that issued as that patent. Accordingly, the applicant's patents filed prior to the filing of each Asserted Patent, and the related file histories, thus qualify as Sec. 102(b) and/or 102(d) prior art, and state of the art—including, but not limited:

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 51 of 101

- Kearns ’798
- VanDoren ’276
- Kaufmann ’179
- VanDoren ’084
- Noel ’682
- Anderson ’061

III. PRIOR ART CLAIM CHARTS

Pursuant to Patent Rule 3-3(c), the claim charts attached hereto as Exhibits A1-G14 and AO-GO identify specifically where each limitation of each claim is found in each prior art reference. SAP expressly reserves the right to supplement or amend these Invalidity Contentions pursuant to Patent Rule 3-6 after the Court’s *Markman* ruling or if Valtrus is permitted to amend or alter its infringement contentions or its position on claim construction in any way. Further, to the extent that SAP applies Valtrus’s constructions (and to the extent these constructions can be discerned), SAP does not concede in any way that those constructions are correct, and instead expressly reserves the right to oppose those constructions at the appropriate time specified in the Court’s Docket Control Order.

In the Invalidity Charts, SAP has referred to relevant, representative portions of the cited prior art. The absence of any specific or express reference to any claim term or claim element in these charts should not be construed as an admission that any corresponding limitation is lacking either expressly or inherently in the prior art reference. There may be additional support or other grounds for SAP’s Invalidity Contentions that such prior art satisfies a particular claim element, and SAP reserves the right to supplement these Invalidity Contentions with such information. For example, persons of ordinary skill in the art at the time of the filing of the Asserted Patents knew to read prior art references as a whole, and in the context of other publications and literature and

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 52 of 101

the general knowledge in the field. SAP may rely on all such information, including uncited portions of the prior art references listed herein, and on other publications and expert testimony, to provide context and as aids to understanding and interpreting the listed references, or to establish that a person of ordinary skill in the art would have been motivated to modify or combine any of the cited references so as to render the claims obvious. Additionally, citations to a particular figure in a prior art reference encompass all text relating to the figure, and citations to text encompass all figures relating to or referred to by that text.

Moreover, many of the prior art systems and apparatuses were sold prior to the earliest asserted priority dates and documentation regarding these prior art systems is not in the possession, custody, or control of SAP. Instead, these documents are currently or will be the subject of third-party discovery, including the subpoenas identified in Section II.C. SAP expressly reserves the right to supplement its Invalidity Contentions to include further information obtained in discovery.

IV. PRIOR ART UNDER 35 U.S.C. § 102 THAT ANTICIPATES THE ASSERTED CLAIMS OF THE ASSERTED PATENTS

The prior art listed above anticipates the Asserted Claims of the Asserted Patents either expressly or inherently as understood by a person having ordinary skill in the art. The specific anticipation assertions with respect to each claim are set forth in the accompanying claim charts, which are attached as Exhibits A1-G14 (as set forth below:)

Exhibit No.	Chart
A1	409 Patent vs. Donley
A2	409 Patent vs. Fee
A3	409 Patent vs. Khare
A4	409 Patent vs. Kim
A5	409 Patent vs. Lee

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 53 of 101

Exhibit No.	Chart
A6	409 Patent vs. Merchant
A7	409 Patent vs. Shinohara
A8	409 Patent vs. CMU Stampede
A9	409 Patent vs. Hydra
A10	409 Patent vs. IBM Power 4
A11	409 Patent vs. IBM System
A12	409 Patent vs. MAJC
A13	409 Patent vs. MIT M-Machine
A14	409 Patent vs. Wisconsin Multiscalar
B1	244 Patent vs. Bowman
B2	244 Patent vs. Frey
B3	244 Patent vs. Fuchs
B4	244 Patent vs. Garg
B5	244 Patent vs. Langseth
B6	244 Patent vs. Miyamoto
B7	244 Patent vs. Muller
C1	182 Patent vs. ASE
C2	182 Patent vs. Beal
C3	182 Patent vs. Margerie
C4	182 Patent vs. Ruuth
C5	182 Patent vs. ServiceGuard Manual
D1	575 Patent vs. Caplan

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 54 of 101

Exhibit No.	Chart
D2	575 Patent vs. Chau
D3	575 Patent vs. Chilton
D4	575 Patent vs. IBM UDB Evaluation
D5	575 Patent vs. IBM UDB Exploitation
D6	575 Patent vs. Kosciuszko
D7	575 Patent vs. Li
D8	575 Patent vs. Messinger
D9	575 Patent vs. Oracle 9i
D10	575 Patent vs. Ouellette
D11	575 Patent vs. Sankaran
D12	575 Patent vs. Stanley
D13	575 Patent vs. Upton
D14	575 Patent vs. Varlamis
D15	575 Patent vs. Actaworks
D16	575 Patent vs. Blevins
D17	575 Patent vs. Mui
D18	575 Patent vs. Tewksbary
E1	139 Patent vs. Goldring
E2	139 Patent vs. Morris
E3	139 Patent vs. Oracle8i Standby Database
F1	738 Patent vs. Akita
F2	738 Patent vs. Iyer
F3	738 Patent vs. Java Message Service

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 55 of 101

Exhibit No.	Chart
F4	738 Patent vs. Kaler
G1	264 Patent vs. Aleksic
G2	264 Patent vs. Arimilli
G3	264 Patent vs. Barroso
G4	264 Patent vs. Cherabuddi
G5	264 Patent vs. Keshava
G6	264 Patent vs. Patkar
G7	264 Patent vs. Tischler
G8	264 Patent vs. CMU Stampede
G9	264 Patent vs. Hydra
G10	264 Patent vs. IBM Power4
G11	264 Patent vs. IBM System
G12	264 Patent vs. MAJC
G13	264 Patent vs. MIT M-Machine
G14	264 Patent vs. Wisconsin Multiscalar

SAP has endeavored to identify the most relevant portions of identified references. The references may contain additional support, however, for a particular claim element. SAP may rely on uncited portions of the prior art references and/or other publications and fact or expert testimony to provide context and as aids to understanding and interpreting the portions that are cited. In instances of cumulative disclosure within a particular prior art reference, SAP may have cited a subset of those instances as opposed to citing each instance, and SAP reserves the right to rely on uncited instances of cumulative disclosure. Where SAP cites to a particular figure in a reference, the citation should be understood to encompass the caption and description of the figure and any

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 56 of 101

text relating to or discussing the figure. Conversely, where SAP cites to particular text referring to a figure, the citation should be understood to include the figure as well.

The references discussed in the claim charts may disclose the elements of the Asserted Claims explicitly and/or inherently, and/or they may be relied on to show the state of the art in the relevant time frame. The suggested obviousness combinations are provided in the alternative to SAP's anticipation contentions and are not to be construed to suggest that any reference included in any combination is not by itself anticipatory. Also, the suggested obviousness combinations are provided as examples, and it should be understood that other combinations of the prior art disclosed and cited herein could be used in such combinations.

V. PRIOR ART UNDER 35 U.S.C. § 103 THAT RENDERS OBVIOUS THE ASSERTED CLAIMS OF THE ASSERTED PATENTS

To the extent that the Asserted Claims are not rendered invalid purely on anticipatory grounds or are not obvious in light of the general knowledge in the field and of one skilled in the art, the primary prior art references charted in A1-G14 render obvious the Asserted Claims alone, in combination with other primary references, or in the combination with the additional art suggested in attached Exhibits AO-GO, as set forth below:

'409 Patent (*see* Exhibit AO)

Donley	Alone or in combination with	Fee, Khare, Kim, Lee, Merchant, CMU Stampede, Hydra, IBM Power4, IBM System, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit AO
Fee	Alone or in combination with	Donley, Khare, Kim, Lee, Merchant, CMU Stampede, Hydra, IBM Power4, IBM System, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit AO
Khare	Alone or in combination with	Donley, Fee, Kim, Lee Merchant, CMU Stampede, Hydra, IBM Power4, IBM System, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit AO

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 57 of 101

Kim	Alone or in combination with	Donley, Fee, Khare, Lee, Merchant, CMU Stampede, Hydra, IBM Power4, IBM System, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit AO
Lee	Alone or in combination with	Donley, Fee, Khare, Kim, Merchant, CMU Stampede, Hydra, IBM Power4, IBM System, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit AO
Merchant	Alone or in combination with	Donley, Fee, Khare, Kim, Lee, CMU Stampede, Hydra, IBM Power4, IBM System, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit AO
CMU Stampede	Alone or in combination with	Donley, Fee, Khare, Kim, Lee, Merchant, Hydra, IBM Power4, IBM System, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit AO
Hydra	Alone or in combination with	Donley, Fee, Khare, Kim, Lee, Merchant, CMU Stampede, IBM Power4, IBM System, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit AO
IBM Power4	Alone or in combination with	Donley, Fee, Khare, Kim, Lee, Merchant, CMU Stampede, Hydra, IBM System, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit AO
IBM System	Alone or in combination with	Donley, Fee, Khare, Kim, Lee, Merchant, CMU Stampede, Hydra, IBM Power4, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit AO
MAJC	Alone or in combination with	Donley, Fee, Khare, Kim, Lee, Merchant, CMU Stampede, Hydra, IBM Power4, IBM System, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit AO
MIT-M-Machine	Alone or in combination with	Donley, Fee, Khare, Kim, Lee, Merchant, CMU Stampede, Hydra, IBM Power4, IBM System, MAJC, Wisconsin Multiscalar, and/or the references in Exhibit AO
Wisc. Mutiscalar	Alone or in combination with	Donley, Fee, Khare, Kim, Lee, Merchant, CMU Stampede, Hydra, IBM Power4, IBM System, MAJC, MIT-M-Machine, and/or the references in Exhibit AO

’244 Patent (*see* Exhibit BO)

Bowman	Alone or in combination with	Frey, Fuchs, Garg, Langseth, Miyamoto, Muller and/or the references in Exhibit BO.

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 58 of 101

Frey	Alone or in combination with	Bowman, Fuchs, Garg, Langseth, Miyamoto, Muller and/or the references in Exhibit BO.
Fuchs	Alone or in combination with	Bowman, Frey, Garg, Langseth, Miyamoto, Muller and/or the references in Exhibit BO.
Garg	Alone or in combination with	Bowman, Frey, Fuchs, Langseth, Miyamoto, Muller and/or the references in Exhibit BO.
Langseth	Alone or in combination with	Bowman, Frey, Fuchs, Garg, Miyamoto, Muller and/or the references in Exhibit BO.
Miyamoto	Alone or in combination with	Bowman, Frey, Fuchs, Garg, Langseth, Muller and/or the references in Exhibit BO.
Muller	Alone or in combination with	Bowman, Frey, Fuchs, Garg, Langseth, Miyamoto and/or the references in Exhibit BO.

’182 Patent (*see* Exhibit CO)

ASE	Alone or in combination with	Beal, Margerie, Ruuth, ServiceGuard and/or the references in Exhibit CO.
Beal	Alone or in combination with	ASE, Margerie, Ruuth, ServiceGuard and/or the references in Exhibit CO.
Margerie	Alone or in combination with	ASE, Beal, Ruuth, ServiceGuard and/or the references in Exhibit CO.
Ruuth	Alone or in combination with	ASE, Beal, Margerie, ServiceGuard and/or the references in Exhibit CO.
ServiceGuard	Alone or in combination with	ASE, Beal, Margerie, Ruuth and/or the references in Exhibit CO.

’575 Patent (*see* Exhibit DO)

Caplan	Alone or in combination with	Chau, Chilton, IBM UDB, Kosciuszko, Li, Messinger, Oracle 9i, Ouellette, Sankaran, Stanley, Upton, Varlamis, Actaworks, Blevins, Mui, Tewksbary and/or the references in Exhibit DO.
Chau	Alone or in combination with	Caplan, Chilton, IBM UDB, Kosciuszko, Li, Messinger, Oracle 9i, Ouellette, Sankaran, Stanley, Upton, Varlamis, Actaworks, Blevins, Mui, Tewksbary and/or the references in Exhibit DO.
Chilton	Alone or in combination with	Caplan, Chau, IBM UDB, Kosciuszko, Li, Messinger, Oracle 9i, Ouellette, Sankaran, Stanley, Upton, Varlamis, Actaworks, Blevins, Mui, Tewksbary and/or the references in Exhibit DO.
IBM UDB	Alone or in combination with	Caplan, Chau, Chilton, Kosciuszko, Li, Messinger, Oracle 9i, Ouellette, Sankaran, Stanley, Upton, Varlamis, Actaworks, Blevins, Mui, Tewksbary and/or the references in Exhibit DO.

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 59 of 101

Kosciuszko	Alone or in combination with	Caplan, Chau, Chilton, IBM UDB, Li, Messinger, Oracle 9i, Ouellette, Sankaran, Stanley, Upton, Varlamis, Actaworks, Blevins, Mui, Tewksbary and/or the references in Exhibit DO.
Li	Alone or in combination with	Caplan, Chau, Chilton, IBM UDB, Kosciuszko, Messinger, Oracle 9i, Ouellette, Sankaran, Stanley, Upton, Varlamis, Actaworks, Blevins, Mui, Tewksbary and/or the references in Exhibit DO.
Messinger	Alone or in combination with	Caplan, Chau, Chilton, IBM UDB, Kosciuszko, Li, Oracle 9i, Ouellette, Sankaran, Stanley, Upton, Varlamis, Actaworks, Blevins, Mui, Tewksbary and/or the references in Exhibit DO.
Oracle 9i	Alone or in combination with	Caplan, Chau, Chilton, IBM UDB, Kosciuszko, Li, Messinger, Ouellette, Sankaran, Stanley, Upton, Varlamis, Actaworks, Blevins, Mui, Tewksbary and/or the references in Exhibit DO.
Ouellette	Alone or in combination with	Caplan, Chau, Chilton, IBM UDB, Kosciuszko, Li, Messinger, Oracle 9i, Sankaran, Stanley, Upton, Varlamis, Actaworks, Blevins, Mui, Tewksbary and/or the references in Exhibit DO.
Sankaran	Alone or in combination with	Caplan, Chau, Chilton, IBM UDB, Kosciuszko, Li, Messinger, Oracle 9i, Ouellette, Stanley, Upton, Varlamis, Actaworks, Blevins, Mui, Tewksbary and/or the references in Exhibit DO.
Stanley	Alone or in combination with	Caplan, Chau, Chilton, IBM UDB, Kosciuszko, Li, Messinger, Oracle 9i, Ouellette, Sankaran, Upton, Varlamis, Actaworks, Blevins, Mui, Tewksbary and/or the references in Exhibit DO.
Upton	Alone or in combination with	Caplan, Chau, Chilton, IBM UDB, Kosciuszko, Li, Messinger, Oracle 9i, Ouellette, Sankaran, Stanley, Varlamis, Actaworks, Blevins, Mui, Tewksbary and/or the references in Exhibit DO.
Varlamis	Alone or in combination with	Caplan, Chau, Chilton, IBM UDB, Kosciuszko, Li, Messinger, Oracle 9i, Ouellette, Sankaran, Stanley, Upton, Actaworks, Blevins, Mui, Tewksbary and/or the references in Exhibit DO.
Actaworks	Alone or in combination with	Caplan, Chau, Chilton, IBM UDB, Kosciuszko, Li, Messinger, Oracle 9i, Ouellette, Sankaran, Stanley, Upton, Varlamis, Blevins, Mui, Tewksbary and/or the references in Exhibit DO
Blevins	Alone or in combination with	Caplan, Chau, Chilton, IBM UDB, Kosciuszko, Li, Messinger, Oracle 9i, Ouellette, Sankaran, Stanley, Upton, Varlamis, Actaworks, Mui, Tewksbary and/or the references in Exhibit DO

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 60 of 101

Mui	Alone or in combination with	Caplan, Chau, Chilton, IBM UDB, Kosciuszko, Li, Messinger, Oracle 9i, Ouellette, Sankaran, Stanley, Upton, Varlamis, Actaworks, Blevins, Tewksbary and/or the references in Exhibit DO
Tewksbary	Alone or in combination with	Caplan, Chau, Chilton, IBM UDB, Kosciuszko, Li, Messinger, Oracle 9i, Ouellette, Sankaran, Stanley, Upton, Varlamis, Actaworks, Blevins, Mui, and/or the references in Exhibit DO

'139 Patent (*see* Exhibit EO)

Goldring	Alone or in combination with	Morris, Oracle 8i and/or the references in Exhibit EO.
Morris	Alone or in combination with	Goldring, Oracle 8i and/or the references in Exhibit EO.
Oracle8i	Alone or in combination with	Goldring, Morris and/or the references in Exhibit EO.

'738 Patent (*see* Exhibit FO)

Akita	Alone or in combination with	Akita, Iyer, Java, Kaler and/or the references in Exhibit FO.
Iyer	Alone or in combination with	Akita, Java, Kaler and/or the references in Exhibit FO.
Java	Alone or in combination with	Akita, Iyer, Kaler and/or the references in Exhibit FO.
Kaler	Alone or in combination with	Akita, Iyer, Java and/or the references in Exhibit FO.

'264 Patent (*see* Exhibit GO)

Aleksic	Alone or in combination with	Arimilli, Barroso, Cherabuddi, Keshava, Patkar, Tischler, CMU Stampede, Hydra, IBM Power4, IBM System, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit GO
Arimilli	Alone or in combination with	Aleksic, Barroso, Cherabuddi, Keshava, Patkar, Tischler, CMU Stampede, Hydra, IBM Power4, IBM System, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit GO
Barroso	Alone or in combination with	Aleksic, Arimilli, Cherabuddi, Keshava, Patkar, Tischler, CMU Stampede, Hydra, IBM Power4, IBM System, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit GO

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 61 of 101

Cherabuddi	Alone or in combination with	Aleksic, Arimilli, Barroso, Keshava, Patkar, Tischler, CMU Stampede, Hydra, IBM Power4, IBM System, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit GO
Keshava	Alone or in combination with	Aleksic, Arimilli, Barroso, Cherabuddi, Patkar, Tischler, CMU Stampede, Hydra, IBM Power4, IBM System, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit GO
Patkar	Alone or in combination with	Aleksic, Arimilli, Barroso, Cherabuddi, Keshava, Tischler, CMU Stampede, Hydra, IBM Power4, IBM System, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit GO
Tischler	Alone or in combination with	Aleksic, Arimilli, Barroso, Cherabuddi, Keshava, Patkar, CMU Stampede, Hydra, IBM Power4, IBM System, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit GO
CMU Stampede	Alone or in combination with	Aleksic, Arimilli, Barroso, Cherabuddi, Keshava, Patkar, Tischler, Hydra, IBM Power4, IBM System, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit GO
Hydra	Alone or in combination with	Aleksic, Arimilli, Barroso, Cherabuddi, Keshava, Patkar, Tischler, CMU Stampede, IBM Power4, IBM System, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit GO
IBM Power4	Alone or in combination with	Aleksic, Arimilli, Barroso, Cherabuddi, Keshava, Patkar, Tischler, CMU Stampede, Hydra, IBM System, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit GO
IBM System	Alone or in combination with	Aleksic, Arimilli, Barroso, Cherabuddi, Keshava, Patkar, Tischler, CMU Stampede, Hydra, IBM Power4, MAJC, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit GO
MAJC	Alone or in combination with	Aleksic, Arimilli, Barroso, Cherabuddi, Keshava, Patkar, Tischler, CMU Stampede, Hydra, IBM Power4, IBM System, MIT-M-Machine, Wisconsin Multiscalar, and/or the references in Exhibit GO
MIT-M-Machine	Alone or in combination with	Aleksic, Arimilli, Barroso, Cherabuddi, Keshava, Patkar, Tischler, CMU Stampede, Hydra, IBM Power4, IBM System, MAJC, Wisconsin Multiscalar, and/or the references in Exhibit GO
Wisc. Mutiscalar	Alone or in combination with	Aleksic, Arimilli, Barroso, Cherabuddi, Keshava, Patkar, Tischler, CMU Stampede, Hydra, IBM Power4, IBM System, MAJC, MIT-M-Machine, and/or the references in Exhibit GO

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 62 of 101

These combinations are not exclusive, and SAP reserves the right to supplement the obviousness arguments listed below, using any references listed above in Section II and any references that may become known to the SAP during the course of discovery. Further, the suggested obviousness combinations are in addition to SAP's anticipation contentions and are not to be construed to suggest that any reference included in the combinations is not anticipatory on its own.

VI. MOTIVATION FOR COMBINING IDENTIFIED PRIOR ART

Pursuant to Local Patent Rule 3-3, SAP has included this section discussing motivation to combine. The Supreme Court, however, has rejected the idea that a "teaching, suggestion, or motivation to combine" is a prerequisite for proving obviousness. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1739-40 (2007) (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, and instead espousing an "expansive and flexible" approach). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *Id.* at 1742.

Subject to the reservation of rights based on SAP's present understanding of the Asserted Claims of the Asserted Patents, and the apparent constructions Valtrus is asserting based on its Infringement Contentions, the prior art references identified above in Section II, which are charted in Exhibits A1-G14, each anticipate and/or individually render obvious the Asserted Claims of the Asserted Patents.

Should any individual prior art reference be deemed not to disclose, explicitly or inherently, any limitation of a claim, SAP contends in the alternative that such individual prior art references can be combined in the manner suggested the table in Section V above. These combinations are not exclusive, and SAP reserves the right to supplement the obviousness arguments listed below,

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 63 of 101

using any references listed above in Section II and any references that may become known to the SAP during the course of discovery.

The United States Supreme Court clarified the standard for what types of inventions are patentable. *KSR Int'l*, 127 S. Ct. 1727. In particular, the Supreme Court emphasized that inventions arising from ordinary innovation, ordinary skill, or common sense should not be patentable. *Id.* at 1732, 1738, 1742-1743, 1746. In that regard, a patent claim may be obvious if the combination of elements was obvious to try or there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. In addition, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, Section 103 bars its patentability. To that end, for the purposes of these Invalidity Contentions and this Section, the knowledge of a person of ordinary skill in the art is demonstrated by the full list of references in Section II and all prior art produced pursuant to Patent Rule 3-4(b).

"[T]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id.* at 1731. Because the Asserted Patents simply arrange old elements with each performing the same function it had been known to perform and yields no more than what one would expect from such an arrangement, the combination is obvious. *Id.* at 1742. The Asserted Claims are therefore invalid under 35 U.S.C. § 103 because they do nothing more than combine known techniques and apparatuses according to their known and ordinary uses to yield predictable results.

The Supreme Court further held that, "[w]hen a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 64 of 101

different one. If a person of ordinary skill can implement a predictable variation, § 103 bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill . . . ." *Id.* at 1740. Accordingly, a person of ordinary skill in the art at the time of the alleged invention would have been motivated to combine or adapt known or familiar methods in the art, especially where market forces prompt such variations. Thus, one of skill in the art would have thought to combine or modify references that described known methods that one of skill in the art would have recognized as offering improvements to solutions of that time. The references in Exhibits AO-GO further describe methods that were known to offer such improvements in the field of each Asserted Patent and, accordingly, one of skill in the art would have been motivated to combine or modify the references as indicated above and in Exhibits AO-GO.

Moreover, since there was a finite number of predictable solutions, a person of ordinary skill in the art had good reason to pursue the known options. *Id.* The primary references in Exhibits A1-G14 and the combination references in Exhibits AO-GO use familiar elements for their primary or well-known purposes in a manner well within the ordinary level of skill in the art. Accordingly, common sense and the knowledge of the prior art render the claims invalid under either Section 102 or Section 103.

A person of ordinary skill would have been motivated to combine the above prior art based on his/her knowledge, the nature of the problem to be solved, and the teachings of the prior art. The references in the exhibits for each Asserted Patent (e.g., all charts for the '409 Patent, which are Ex. A1-A7 and AO) address the same or similar technical issues and suggests the same or

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 65 of 101

similar solutions to those issues. Moreover, some of the prior art refer to or discuss other prior art, illustrating the close technical relationship among the prior art.

By way of further example, references in the exhibits for each Asserted Patent (e.g., all charts for the '409 Patent, which are Ex. A1-A7 and AO) are directed to the same or similar technology—namely, document processing on a mobile phone. Thus, for example, one of ordinary skill in the art would have been motivated to combine known prior art solutions described in these references relating to document processing using a mobile phone, including autocapture of documents and mobile check processing.

Moreover, as detailed above, many of the claim elements were already known as admitted by the applicant in the specifications of the Asserted Patents. These elements represented design choices available to a person of ordinary skill. When there is a design need or market pressure to solve a problem such as identified previously and/or described in the Asserted Patents, and there are a finite number of identified, predictable solutions, a person of ordinary skill would be motivated to combine the known options that are within his or her technical grasp. Here, one of ordinary skill in the art would have been motivated to combine known prior art solutions, including those in the combination references and those admitted by applicant to be known.

For each of the various "systems" or "products" that are discussed in Section II.C, to the extent that the collective references referenced in Section II.C are not considered to be the same reference for purposes of invalidity under 35 U.S.C. § 102, it would have been obvious to combine the references cited. For each such product/system, all of the listed references relate to the same technology and variations thereof. One of skill in the art would have been motivated to look at all of the available documentation for a particular product/system to understand the operation. One of skill in the art would have combined that knowledge from the various related references because

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 66 of 101

it would be clear that the references were related. For at least this reason, one of skill in the art could consider it obvious to combine the references that collectively teach a particular technology. The references were identified in the charts for each such system/product, and SAP intends to rely on the combination of references in each of the system/product charts.

One of skill in the art would have been motivated to combine the different publications and patents that were authored by employees of the same company or assigned to the same assignee and related to the same subject matter, particularly when that assignee was well-known to have experience and knowledge in the design and development of computer architectures and the patents are directed to improvements in the company's products. So, for example, for such companies one of skill in the art would have been motivated to look at the various patents assigned to the companies, as well as articles written about their products, and to combine the approaches taken in those patents and articles for such products. Likewise, employees at applicant HPE itself would have been motivated to combine the 102(d) different publication and patents authored by employees of their same company related to the same subject matter (*see* Section II.E).

One of skill in the art would have been motivated to combine different references that were authored, developed, or invented by the same individual(s) related to the same subject matter. The common inventor/author/architect references themselves demonstrate that they relate to continued work in a common field of effort and continued related developments in that field. One of skill in the art would, therefore, combine the references related to each individual.

Each of the references can be combined with the known prior art based on the statements made in the specification and during prosecution of the Asserted Patents. For example, the applicants acknowledged that many of the claimed features were well known in the art. *See* Section II.D, above. Thus, it would have been obvious for one of skill in the art to combine this knowledge

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 67 of 101

in the art (as the applicants did) with any of the charted references because the applicants acknowledged that the basic arrangement of elements was known in the art.

Additionally, beyond the elements acknowledged in the patent and prosecution history to be known in the art, to the extent that the Valtrus alleges that certain elements are missing from any of the charted references, those elements are known in the art or would be inherent in the relevant context. One of skill in the art would have understood that different approaches could be taken depending on the design needs and would have combined those approaches to meet the various design needs.

It would have been obvious to combine any references that expressly refer to each other or incorporate each other by reference. For example, one of skill in the art would have been motivated to combine different references from articles or papers that were known to be related and/or referenced within another related article or paper. So, for example, it would have been obvious to combine a paper referenced in an article with the paper that references the article. In addition, it would have been obvious to combine a patent (or patent application) incorporated by reference into another patent (or patent application). It likewise would have been obvious to combine patents and patent applications from the same patent family.

Exemplary combinations are identified in the table in Section V. above for purposes of explaining and exemplifying which references would be combined. In many instances, multiple different motivations would apply to a particular combination (for example, if multiple references were both authored by the same person and referred to the same product/system, then both of those motivations would apply).

In addition to the motivations set forth above, one or more combinations of the prior art references identified above and below pursuant to Patent Rule 3-3(a) would have been obvious

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 68 of 101

because these references would have been combined using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining the prior art references identified above pursuant to Patent Rule 3-3(a) because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. In addition, the combinations of the prior art references identified above pursuant to P.R. 3-3(a) would have been obvious because the combinations represent the known potential options with a reasonable expectation of success.

Notwithstanding the factors and motivations identified above, including the exemplary combinations above, and notwithstanding the nascent stage of discovery, and subject to the reservation of rights stated above, SAP contends that an analysis of secondary considerations further supports the view that each of the Asserted Claims is obvious. Secondary considerations that courts evaluate as objective indicia of obviousness or nonobviousness of an alleged invention include (1) commercial success of the claimed subject matter; (2) long felt but unresolved needs; (3) failure of others; (4) teaching away from the claimed subject matter by the prior art; (5) copying or acclamation by others; and (6) skepticism of experts. *See, e.g*., *Ruiz v. A.B. Chance Co.,* 357 F.3d 1270, 1274 (Fed. Cir. 2004); *Ecolochem, Inc. v. Southern Cal. Edison Co.*, 227 F.3d 1361, 1379 (Fed. Cir. 2000).

On information and belief, the Asserted Patents also were not directed to long felt, unresolved needs. On the contrary, the Asserted Patents addressed problems that had been handled successfully in the prior art.

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 69 of 101

Additionally, and as outlined herein and in the Exhibits, numerous prior art references anticipate the claims of the Asserted Patents, so failure by others cannot be cited as a secondary consideration in favor of nonobviousness. Numerous prior art references, including those identified above pursuant to Patent Rule 3-3(a), are directed to the same approach as the Asserted Patents. Importantly, none of the prior art teaches away from the claimed subject matter. In fact, just the opposite is true, and as shown in these Invalidity Contentions and the accompanying claim charts, the prior art teaches the claimed subject matter. Thus, Valtrus cannot rely on any teaching away in the prior art.

Valtrus has not presented any evidence to suggest that others in the industry copied or praised the alleged invention of the Asserted Patents. To the extent that others may have subsequently adopted a similar technique, SAP asserts that they were in fact copying well-known systems that predate the Asserted Patents. At the time of the alleged invention of the Asserted Patents, experts would not have been skeptical of the general approach or idea disclosed therein. The general idea of each Asserted Patent had already been in widespread use for a long time and was not patentable by the time the applicants filed their patent applications. Experts would have regarded the disclosures and matter claimed in the Asserted Patents as obvious.

Any reference or combination of references that anticipates or makes obvious an independent claim also makes obvious any claim dependent on that independent claim because every element of each dependent claim was known by a person of ordinary skill at the time of the alleged invention, and it would have been obvious to combine those known elements with the independent claim at least as a matter of common sense and routine innovation. Accordingly, SAP contends that each claim would have been obvious not only by the combinations explicitly defined in these contentions, but also by any combination of references that renders obvious that claim.

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 70 of 101

To the extent Valtrus contends that any reference contains multiple distinct embodiments, it would be obvious to combine elements of the distinct embodiments. A person would be motivated to make such a combination because the elements are found in the same reference and the reference as a whole is directed to the same topic or topics.

VII. INVALIDITY UNDER 35 U.S.C. § 112(¶1/a)

Pursuant to Patent Rule 3-3(d), SAP hereby identifies grounds of invalidity based on lack of written description and enablement under 35 U.S.C. § 112(¶1/a) (requiring "a written description of the [claimed] invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same."). SAP reserves the right to supplement or amend these contentions based on Valtrus's representations during the course of the litigation (including during claim construction) and following any claim construction rulings of the Court.

Valtrus has asserted in its Patent Rule 3-1(e) disclosures, for each Asserted Patent, that each Asserted Claim of the Asserted Patents is entitled to the filing date of the patent's earliest ancestor application as its priority date (hereinafter, "the Asserted Priority Application"). SAP denies that asserted entitlement but in view of such position of Valtrus in its Patent Rule 3-1(e) disclosure, that Asserted Priority Application is the application governing invalidity of the claims under Sec. 112(¶1/a), and therefore these Invalidity Contentions focus on the lack of support in the Asserted Priority Application for each claim.

Throughout these contentions, an assertion that an application did not "support" a claim or claim element means—unless otherwise noted—that the application did not provide as of the filing date sought:

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 71 of 101

(a) the required written description for the claim element and the claimed subject matter;

(b) the required written description for the full-scope of the claim element and the claim;

(c) the required enabling disclosure for the claim element and the claimed subject matter;

(d) the required enabling disclosure for the full-scope of the claim element and the claim;

(e) a description of the claimed "invention" understandable to a skilled artisan and showing that the applicant actually possessed such "invention";

(f) a description of the claimed "invention" that was express or necessarily present (inherent), complete, unambiguous, specific, and as broad as the claim; or

(g) a disclosure teaching a skilled artisan how, by following the steps set forth in the application, to make or carry out (use) the claimed "invention" without undue experimentation.

Throughout these contentions, an assertion that an application did not "support" an independent claim or language in an independent claim means—unless otherwise noted—that the application did not support that claim's asserted dependent claims either.

Each Asserted Claim of the Asserted Patents is invalid (or alternatively not entitled to the benefit of an earlier filed date) for failure of the Asserted Priority Application to support the claim. For each Asserted Claim, the Asserted Priority Application failed to support the claim and individual elements of the claim, as listed below.

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 72 of 101

The ’409 Patent

’409 Patent, Claim 1:

- a coherency control module operably coupled to the first processor bus and the second processor bus and comprising:
- a request module configured to receive requests from the first processor bus and the second processor bus and to maintain proper ordering of the requests from each processor bus,
- an active snoop queue (ASQ) module coupled to the request module and configured to maintain a list of requests currently being processed and to prevent simultaneous multiple accesses to a single address in the static portion of the RAM, and
- a static RAM interface module configured to access an address look-up table corresponding to data stored in the static portion of the RAM

’409 Patent, Claim 2:

- comprising an input/output (1/0) bus coupled between the host controller and a plurality of 1/0 devices, wherein the 1/0 bus is operably coupled to the coherency control module and wherein the request module is configured to receive requests from the I/O bus

’409 Patent, Claim 3:

- wherein the coherency control module is located within the host controller

’409 Patent, Claim 4:

- wherein the coherency control module comprises a plurality of list structures corresponding to the first processor bus and the second processor bus

’409 Patent, Claim 5:

- wherein the list structures comprise two-dimensional doubly-linked lists with head and tail pointers

’409 Patent, Claim 7:

- wherein the request module comprises a plurality of bypass paths configured to provide a direct request path from the first and second processor buses to the static RAM interface module, thereby bypassing the list structures

’409 Patent, Claim 8:

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 73 of 101

- wherein the active snoop queue module comprises a plurality of 10 active snoop queues, each active snoop queue configured to maintain a list of requests currently being processed and to function independently with respect to each other

'409 Patent, Claim 10

- A coherency control module configured to control access to cache memory in a computer system, the coherency control module comprising,

- a request module configured to receive requests from a plurality of buses in a computer system and to maintain proper ordering of the requests from each bus, and

- an active snoop queue (ASQ) module coupled to the request module and configured to maintain a list of requests from all of the buses currently being processed and to prevent multiple accesses to a single address in the cache memory simultaneously

'409 Patent, Claim 12

- wherein the coherency control module comprises a plurality of list structures corresponding to the first processor bus and the second processor bus

'409 Patent, Claim 13

- wherein the list structures comprise two-dimensional doubly-linked lists with head and tail pointers

'409 Patent, Claim 15

- wherein the request module comprises a plurality of bypass paths configured to provide a direct request path from the first and second processor buses to the static RAM interface module, thereby bypassing the list structures

'409 Patent, Claim 16

- wherein the active snoop queue module comprises a plurality of active snoop queues, each active snoop queue configured to maintain a list of requests currently being processed and to function independently with respect to each other

The '244 Patent

'244 Patent, Claim 1:

- storing the message in a data Structure in highly reliable fault-tolerant storage media of the FTSS, and

- processing the message at the FTSS in accordance with a messaging paradigm

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 74 of 101

’244 Patent, Claim 2:

- the messaging paradigm is a request/reply communication paradigm,
- transmitting a request message from the first node to a request/reply communication agent in the FTSS,
- storing the message in a data structure in highly reliable fault-tolerant storage media of the FTSS,
- storing the request message in a request queue in highly reliable fault-tolerant storage media of the FTSS,
- transmitting the reply message from the second node to the request/reply communication agent in the FTSS, and
- storing the reply message in a reply queue in highly reliable fault-tolerant storage media of the FTSS

’244 Patent, Claim 3:

- wherein the messaging paradigm is a conversational communication paradigm,
- transmitting a connect message from the first node to a conversational communication agent in the FTSS,
- opening a conversation queue in highly reliable fault-tolerant storage media of the FTSS, and
- storing the message in a data structure in highly reliable fault-tolerant storage media of the FTSS

’244 Patent, Claim 4:

- transmitting a send message from the first node to the conversational communication agent in the FTSS, and
- transmitting the receive message from the second node to the conversational communication agent in the FTSS

’244 Patent, Claim 5:

- transmitting a disconnect message from the first node to the conversational communication agent in the FTSS

’244 Patent, Claim 6:

- the messaging paradigm is an event-based communication paradigm,

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 75 of 101

- transmitting a post message from the first node to an event-based communication agent in the FTSS,

- accessing a subscription manager to determine whether any nodes have subscribed to receive the event represented by the post message,

- storing the message in a data structure in highly reliable fault-tolerant storage media of the FTSS comprises,

- storing the post message in an event queue in highly reliable fault-tolerant storage media of the FTSS,

’244 Patent, Claim 7:

- transmitting a subscribe message from the second node to the event-based communication manager in the FTSS, wherein the subscribe message includes an event

’244 Patent, Claim 8:

- transmitting an unsubscribe message from the second node to the event-based communication manager in the FTSS, wherein the unsubscribe message includes an event

’244 Patent, Claim 9:

- wherein the messaging paradigm is a queue-based communication paradigm,

- transmitting an enqueue message from the first node to a queue-based communication agent in the FTSS,

- storing the message in a data structure in highly reliable fault-tolerant storage media of the FTSS comprises,

- storing the enqueue message in a queue space in highly reliable fault tolerant storage media of the FTSS,

- retrieving the enqueue message from the queue space only if the second node is available,

- transmitting the enqueue message from the FTSS to a service on the second node only if the second node is available, and

- executing the service on the second node using the enqueue message as an input and providing a dequeue message as an output; transmitting the dequeue message from the second node to the queue-based communication agent in the FTSS,

’244 Patent, Claim 10:

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 76 of 101

- wherein the messaging paradigm is an unsolicited communication paradigm,
- transmitting a broadcast message from the first node to an unsolicited communication agent in the FTSS,
- accessing determining which nodes should receive the broadcast message based on the broadcast message,
- storing the message in a data structure in highly reliable fault-tolerant storage media of the FTSS comprises, and
- storing the broadcast message in an unsolicited message queue in highly reliable fault-tolerant storage media of the FTSS

The ’182 Patent

’182 Patent, Claim 1:

- a first redundancy appliance operable in a role for receiving a sequence of write requests and for storing data for the sequence of write requests in storage associated with the primary storage facility,
- a second redundancy appliance for shadowing the first redundancy appliance wherein the second redundancy appliance assumes the role of the first redundancy appliance,
- the secondary storage facility discrete from the primary storage facility,
- a third redundancy appliance operable in a role for storing redundant data for the sequence of write requests in storage associated with the secondary facility, and
- a fourth redundancy appliance for shadowing the third redundancy appliance wherein the fourth redundancy appliance assumes the role of the third redundancy appliance in the event of a fault at the third redundancy appliance.

’182 Patent, Claim 2:

- the failover event including a communication traffic condition having a greater portion of request traffic originating closer to the secondary storage facility than to the primary storage facility

’182 Patent, Claim 3:

- a failover event selected from the group consisting of a manually initiated event and an automatically initiated event

’182 Patent, Claim 4:

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 77 of 101

- the second redundancy appliance sending acknowledgements to the first redundancy appliance in batches in response to receiving write records

’182 Patent, Claim 6:

- wherein the first redundancy appliance is disjoint from the second redundancy appliance

’182 Patent, Claim 7:

- wherein the second redundancy appliance maintains a shadow copy of data stored by the first redundancy appliance wherein the second redundancy appliance accesses the shadow copy of the data when the second redundancy appliance assumes the role of the first redundancy appliance

’182 Patent, Claim 9:

- wherein the first redundancy appliance forwards redundant data to the secondary storage facility as send batches

’182 Patent, Claim 10:

- wherein a send batch size is determined according to either a time interval for collecting transactions into the send batch or a predetermined quantity of transactions to be included in the send batch

’182 Patent, Claim 11:

- wherein a send batch size is determined adaptively based on available communication bandwidth between the primary storage facility and the secondary storage facility

’182 Patent, Claim 14:

- wherein the third redundancy appliance stores a receive batch after the receive batch is determined safe to apply

’182 Patent, Claim 15:

- wherein a receive batch is determined safe to apply when a data integrity test is successfully performed

’182 Patent, Claim 17:

- forwarding the logged write requests as send batches to a second redundancy appliance at the secondary storage facility disjoint from the primary storage facility, the second storage facility batching the received write request as receive batches, and

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 78 of 101

- the second redundancy appliance acting as the first redundancy appliance in response to a failover event.

’182 Patent, Claim 18:

- at least one primary redundancy appliance for receiving a sequence of write requests and for storing data for the sequence of write requests in storage associated with the primary storage facility, the primary storage facility batching the write requests as send batches for transfer to a secondary storage facility,

- the secondary storage facility disjoint from the primary storage facility including at least one secondary redundancy appliance for receiving the sequence of write requests and for storing data for the sequence of write requests in storage associated with the secondary storage facility, and

- wherein a first write transaction in a receive batch at the second storage facility is replaced with a second write transaction where the second write transaction over writes data written by the first write transaction

The ’575 Patent

’575 Patent, Claim 1:

- an interface executing on the computing system for communicating between a data store and applications that supply and consume data,

- a real time information director (RTID) executing on the computing system that transforms data for supply, consumption, or both by the applications under direction of polymorphic metadata that defines a security model and data integrity rules for application to the data,

- the RTID to dynamically instantiate, create, and cache for reuse disassemblers and assemblers according to demand,

- at least one disassembler defined according to the polymorphic metadata that disassembles inbound data documents into multiple records in preparation for insertion into metadata tables, and

- at least one assembler defined according to the polymorphic metadata that assembles outbound data documents from at least one record selected from at least one metadata-selected table whereby data is transformed for supply, consumption or both.

’575 Patent, Claim 2:

- a data mapper collecting data from a plurality of diverse applications that can supply data in multiple diverse external document formats and mapping the

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 79 of 101

supplied data to a predetermined unified data model according to the polymorphic metadata

’575 Patent, Claim 3:

- a logic that cleanses and enriches the data, supplies data security, and insures data integrity

’575 Patent, Claim 4:

- a same descriptive polymorphic metadata to build both assemblers and disassemblers for a same document class

’575 Patent, Claim 5:

- specifies logic behaviors applicable to the individual data elements

’575 Patent, Claim 6:

- a logic that represents metadata as polymorphic objects, enabling individual metadata objects to have distinct numbers and types of attributes according to a predetermined object class, the behaviors and attributes being defined specific to object class

’575 Patent, Claim 7:

- a logic that represents metadata as stateless polymorphic objects that are permanent after initial construction, whereby methods of stateful metadata classes delegate operation to the stateless polymorphic metadata objects

’575 Patent, Claim 8:

- the constructors having parameters that specify metadata data elements and being nested to represent hierarchical relationships between the specified metadata data elements, the at least one metadata object including identifying information for deriving the hierarchical relationships

’575 Patent, Claim 11:

- a logic that automatically generates and caches prepare SQL statements from a content metadata portion of document metadata according to the schema

’575 Patent, Claim 16:

- the security manager enforces securities policies that are customized to identify specific agent and consumer relationships expressed in a business model

’575 Patent, Claim 18:

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 80 of 101

- a data cleanser that receives data elements identified by Document Metadata, normalizes the data elements, queues source and destination information for detection of duplicates, and cross-references duplicates in the data store

’575 Patent, Claim 21:

- a business rules engine that defines a business object model capable of enabling access to data described by Document Metadata, performing computations on data relevant to business rules specified by the business object model, concluding a decision based on computation results, and executing the decision

’575 Patent, Claim 22:

- a code causing the controller to transfer data among a data store and applications that supply and consume data,

- a code causing the controller to transform data for transfer using a representation of metadata as polymorphic objects, enabling individual metadata objects to have distinct numbers and types of attributes according to a predetermined object class, the behaviors and attributes being defined specific to object class,

- a code causing the controller to dynamically instantiate, create, and cache for reuse at least one disassembler and at least one assembler according to demand,

- a code dynamically created by the controller as defined by polymorphic metadata that disassembles inbound data documents into multiple records in preparation for insertion into metadata tables, and

- a code dynamically created by the controller as defined by polymorphic metadata that assembles outbound data documents from at least one record selected from at least one metadata-selected table

’575 Patent, Claim 23:

- a code causing the controller to transform data under direction of polymorphic metadata that defines a security model and data integrity rules for application to the data

’575 Patent, Claim 24:

- a code causing the controller to collect data from a plurality of diverse applications that can supply data in multiple diverse external document formats and mapping the supplied data to a predetermined unified data model according to the polymorphic metadata

’575 Patent, Claim 25:

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 81 of 101

- a code causing the controller to represent metadata as stateless polymorphic objects that are permanent after initial construction, whereby methods of stateful meta data classes delegate operation to the stateless poly morphic metadata objects

’575 Patent, Claim 26:

- a code causing the controller to construct at least one metadata object using constructors of multiple metadata classes

- a code causing the controller to use constructor parameters to specify metadata data elements and being nested to represent hierarchical relationships between the specified metadata data elements, the at least one metadata object including identifying information for deriving the hierarchical relationships

’575 Patent, Claim 27:

- a code causing the controller to use received data document mapping metadata to disassemble elements of inbound data documents into rows and columns to be inserted into inbound metadata-selected tables in a database, select rows and columns from outbound metadata-selected tables of the database and assemble elements from the outbound metadata-selected tables into an outbound data document, and generate a schema for documents that can be input or output using the received data document mapping metadata

’575 Patent, Claim 28:

- a real time information director (RTID) executing on at least one of the interlinked servers that manages information flow between a data store and applications that supply and consume data and dynamically instantiates, creates, and caches for reuse disassemblers and assemblers according to demand,

- the RTID that creates at least one disassembler defined according to the polymorphic metadata that disassembles inbound data documents into multiple records in preparation for insertion into metadata tables and create at least one assembler defined according to the polymorphic metadata that assembles outbound data documents from at least one record selected from at least one metadata-selected table whereby data is transformed for supply, consumption, or both

’575 Patent, Claim 31:

- the RTID represents metadata as polymorphic objects, enabling individual metadata objects to have distinct numbers and types of attributes according to a predetermined object class, the behaviors and attributes being defined specific to object class

’575 Patent, Claim 32:

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 82 of 101

- the RTID represents metadata as stateless polymorphic objects that are permanent after initial construction, whereby methods of stateful metadata classes delegate operation to the stateless polymorphic metadata objects

’575 Patent, Claim 33:

- the at least one disassembler, assembler, and generator that use a single descriptive polymorphic metadata

’575 Patent, Claim 36:

- transforming data for transfer using a representation of metadata as polymorphic objects, enabling individual metadata objects to have distinct numbers and types of attributes according to a predetermined object class, the behaviors and attributes being defined specific to object class

- dynamically instantiating, creating, and caching for reuse at least one disassembler and at least one assembler according to demand,

The ’139 Patent

’139 Patent, Claim 1:

- transmitting the active transaction redo log and the delta image, separately in time sequence, from the primary site to the standby site

’139 Patent, Claim 3:

- step of storing transactions in the standby active transaction redo log as they are trapped at the primary site

’139 Patent, Claim 5:

- trapping active log writes using a remote mirroring device that is capable of mirroring the log writes to a standby site, to create an online redo log at the standby site

’139 Patent, Claim 7:

- transmitting the delta image to a standby archive log replicator using a first remote mirroring device in the primary database and a second remote mirroring device in the standby database

’139 Patent, Claim 8:

- using replication handles to track the progress of mirror writes on the standby database as compared to the primary database

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 83 of 101

’139 Patent, Claim 10:

- shipping an entire archive redo log from the primary archive log replicator to the standby archive log replicator asynchronously after archiving becomes slow enough that there is a risk of primary database blocking

’139 Patent, Claim 11:

- shipping an entire archive redo log from the primary archive log replicator to the standby archive log replicator asynchronously when a spool buffer in a remote mirroring system has been filled

’139 Patent, Claim 12:

- trapping file system transactions to create an online redo log at the standby database

’139 Patent, Claim 14:

- transmitting the delta image to a standby archive log replicator using a first remote mirroring device in the primary database and a second remote mirroring device in the standby database.

’139 Patent, Claim 15:

- using replication handles to track the progress of mirror writes on the standby database as compared to the primary database

’139 Patent, Claim 17:

- shipping an entire archive redo log from the primary archive log replicator to the standby archive log replicator asynchronously after archiving becomes slow enough that there is a risk of the primary database blocking

’139 Patent, Claim 18:

- shipping the entire archive redo log from the primary archive log replicator to the standby archive log replicator asynchronously when a spool buffer in a remote mirroring system has been filled

The ’738 Patent

’738 Patent, Claim 1:

- selectively indicating to the layer of the protocol stack that context information is to be obtained for that layer

- obtaining, by the computing device, context information in accordance with the indication

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 84 of 101

- adding, by the computing device, the obtained context information to the outgoing message such that a response, received from the destination node, to the outgoing message contains the obtained context information

'738 Patent, Claim 2:

- adding context information obtained from a different protocol stack layer to the outgoing message

'738 Patent, Claim 5:

- obtaining context information obtains context information related to the outgoing message

'738 Patent, Claim 10:

- an indication associated with the obtained context information where it is determined that the obtained context information is potentially inaccurate or incomplete

'738 Patent, Claim 33:

- indicating to a layer that context information is to be obtained for that layer
- obtaining, by a computing device, context information in accordance with the indication
- adding, by the computing device, the obtained context information to the message, such that a response to the message contains the obtained context information needed to restore a pre-switchover context of the layer

The '264 Patent

'264 Patent, Claim 1:

- a high-speed interconnect coupling the plurality of cache memory blocks to the first and second cache controllers such that at least one allocable cache memory block is capable of being used by the first and second cache controllers
- a resource allocation controller coupled to determine an accessing cache memory controller selected from the group consisting of the first and second cache memory controllers, whereby the accessing cache memory controller is allowed to access the allocable cache memory block

'264 Patent, Claim 5:

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 85 of 101

- a plurality of allocable upper level cache memory blocks, interconnect apparatus for transmitting cache misses at each first level cache to upper level cache memory blocks assigned thereto

- allocation apparatus for assigning upper level cache memory blocks to processors

- repartitioning the system, the step of repartitioning the system including allocation of upper level cache blocks to processors of at least one of the multiple processor integrated circuits

'264 Patent, Claim 11:

- of stopping execution of operating systems in each partition, and restarting execution of operating systems in each partition, and wherein the system is capable of being repartitioned without rebooting each operating system

VIII. INVALIDITY UNDER 35 U.S.C. § 112(2/b)

Pursuant to Patent Rule 3-3(d), SAP hereby identify grounds of invalidity "based on indefiniteness" under 35 U.S.C. § 112(2/b) (requiring "claims particularly pointing out and distinctly claiming the" "invention"). SAP reserves the right to supplement or amend these contentions based on Valtrus's representations during the course of the litigation and any claim construction rulings of the Court. The Patent Rules do not require these contentions to include, and SAP does not include, contentions regarding invalidity under the additional "regards as the invention" requirement of Section 112(2/b).

Throughout these contentions, an assertion that a claim or claim language was unclear and imprecise means—unless otherwise noted—that the claim, each claim containing that claim language, and each dependent claim therefrom, read by a skilled artisan at the time of the patent application, in light of the application and its Patent Office prosecution history leading to issuance of the patent: (a) failed the statute's particular and distinct claiming mandate; (b) failed to inform, with reasonable certainty, those skilled in the art at the time of the patent application of the scope of the claimed invention; and (c) failed to clearly distinguish what is claimed from what went before in the art and clearly circumscribe what is foreclosed from future enterprise.

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 86 of 101

An assertion that a claim or claim language was unclear and imprecise does not necessarily mean that the claim or claim language is not now amenable to construction by the court.

'409 Patent

Based on SAP's present understanding of Valtrus's asserted scope of the claims of the '409 Patent, to the extent such positions can be understood from Valtrus's Infringement Contentions, SAP asserts that the Asserted Claims of the '409 Patent are invalid for reciting at least the following claim terms, phrases, or limitations:

- a coherency control module (claims 1-4, 10-17)
- maintain proper ordering (claims 1 and 10)
- active snoop queue (ASQ) (claims 1, 8, 10, 16)

These claim terms, phrases, and limitations, as apparently construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112.

Additionally, Claims 1-2, 7-8, 10, and 15-16 of the '409 Patent recites numerous limitations ("request module configured to," "active snoop queue (ASQ) module . . . configured to," "static RAM interface module configured to," "plurality of bypass paths configured to," and "coherency control module configured to"), which are subject to 35 U.S.C. § 112 paragraph 6 (pre-AIA). SAP asserts that each claim is invalid as indefinite for failure to recite sufficient structure.

Based on Defendants' present understanding of Plaintiff's Infringement Contentions, at least one or more of these claim terms, phrases, and limitations are indefinite because they are inconsistent with and broader than the alleged invention disclosed in the specification and during prosecution, and given Valtrus's apparent constructions of the claims, any person of ordinary skill in the art at the time of the invention would not understand what is claimed with reasonable certainty, even when the claims are read in light of the specification and prosecution history. Despite the indefiniteness of the claims, the prior art references described in these contentions,

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 87 of 101

alone or in combination with other prior art references, render the claims invalid under any reasonable interpretation of the claims.

’244 Patent

Based on SAP’s present understanding of Valtrus’s asserted scope of the claims of the ’244 Patent, to the extent such positions can be understood from Valtrus’s Infringement Contentions, SAP asserts that the Asserted Claims of the ’244 Patent are invalid for reciting at least the following claim terms, phrases, or limitations:

- highly reliable fault-tolerate storage media (claims 1-3, 6, 9-10)
- messaging paradigm (claims 1-3, 6, 9-10)
- request/reply communication paradigm (claim 2)
- request/reply communication agent (claim 2)
- reply queue (claim 2)
- conversational communication paradigm (claim 3)
- conversational communication agent (claims 3-5)
- conversation queue (claims 3-5)
- event-based communication paradigm (claim 6)
- event-based communication agent (claim 6)
- event queue (claim 6)
- event-based communication manager (claims 7-8)
- queue-based communication paradigm (claim 9)
- queue-based communication agent (claim 9)
- enqueue (claim 9)
- dequeue (claim 9)
- unsolicited message queue (claim 10)

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 88 of 101

These claim terms, phrases, and limitations, as apparently construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112.

Based on Defendants' present understanding of Plaintiff's Infringement Contentions, at least one or more of these claim terms, phrases, and limitations are indefinite because they are inconsistent with and broader than the alleged invention disclosed in the specification and during prosecution, and given Valtrus's apparent constructions of the claims, any person of ordinary skill in the art at the time of the invention would not understand what is claimed with reasonable certainty, even when the claims are read in light of the specification and prosecution history. Despite the indefiniteness of the claims, the prior art references described in these contentions, alone or in combination with other prior art references, render the claims invalid under any reasonable interpretation of the claims.

'182 Patent

Based on SAP's present understanding of Valtrus's asserted scope of the claims of the '182 Patent, to the extent such positions can be understood from Valtrus's Infringement Contentions, SAP asserts that the Asserted Claims of the '182 Patent are invalid for reciting at least the following claim terms, phrases, or limitations:

- communication traffic condition having a greater portion (claim 2)
- shadow copy (claim 7)
- send batch size is determined according to either a time interval for collecting transactions into the send batch or a predetermined quantity of transactions to be included in the send batch (claim 10)
- send batch size is determined adaptively based on available communication bandwidth between the primary storage facility and the secondary storage facility (claim 11)
- safe to apply (claims 14-15)
- a data integrity test is successfully performed (claim 15)

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 89 of 101

These claim terms, phrases, and limitations, as apparently construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112.

Additionally, Claims 1 and 18 of the ’182 Patent recites numerous limitations (“primary storage facility for,” “first redundancy appliance operable in a role for,” “second redundancy appliance for,” “secondary storage facility for,” “third redundancy appliance operable in a role for,” “fourth redundancy appliance for,” “a primary storage facility including at least one primary redundancy appliance for,” “secondary storage facility disjoint from the primary storage facility including at least one secondary redundancy appliance for”), which are subject to 35 U.S.C. § 112 paragraph 6 (pre-AIA). SAP asserts that each claim is invalid as indefinite for failure to recite sufficient structure.

Additionally, Claims 17 and 18 of the’182 Patent contain both apparatus and method steps of using the apparatus and are thus indefinite under 35 U.S.C. 112(b) or pre-AIA 35 U.S.C. 112, second paragraph. *See In re Katz Interactive Call Processing Patent Litigation*, 639 F.3d 1303, 1318, 97 USPQ2d 1737, 1748-49 (Fed. Cir. 2011).

Based on Defendants’ present understanding of Plaintiff’s Infringement Contentions, at least one or more of these claim terms, phrases, and limitations are indefinite because they are inconsistent with and broader than the alleged invention disclosed in the specification and during prosecution, and given Valtrus’s apparent constructions of the claims, any person of ordinary skill in the art at the time of the invention would not understand what is claimed with reasonable certainty, even when the claims are read in light of the specification and prosecution history. Despite the indefiniteness of the claims, the prior art references described in these contentions, alone or in combination with other prior art references, render the claims invalid under any reasonable interpretation of the claims.

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 90 of 101

’575 Patent

Based on SAP’s present understanding of Valtrus’s asserted scope of the claims of the ’575 Patent, to the extent such positions can be understood from Valtrus’s Infringement Contentions, SAP asserts that the Asserted Claims of the ’575 Patent are invalid for reciting at least the following claim terms, phrases, or limitations:

- transforms data for supply, consumption, or both (claim 1, 28)
- data is transformed for supply, consumption or both (claim 1, 28)
- applications under direction of polymorphic metadata (claim 1, 23)
- the RTID to dynamically instantiate, create, and cache (claim 1, 22, 28)
- multiple diverse external document formats (claim 2, 24)
- a predetermined unified data model (claim 2, 24)
- cleanses and enriches the data, supplies data security, and insures data integrity (claim 3)
- have distinct numbers and types of attributes according to a predetermined object class (claim 6, 22, 31, 36)
- metadata object constructed using constructors (claim 8, 26)
- upon registration (claim 14)
- normalizes the data elements (claim 18)

These claim terms, phrases, and limitations, as apparently construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112.

Additionally, Claims 1, 3, 5-7, 9, 11-15, 17-19, 21-28, 30, and 35 of the ’575 Patent recites numerous limitations (“an interface executing on the computing system for,” “real time information director (RTID) executing on the computing system that,” “disassembler . . . that disassembles,” “assembler . . . that assembles,” “logic that,” “servlet that,” “subscription handler that,” “a security manager that,” “audit log handler that,” “data cleanser that,” “aggregation engine

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 91 of 101

that," "business rules engine that," "code causing the controller," "s code . . . that disassembles," "a code . . . that assembles," "server platform . . . that," "one generator that . . . generates," "a query logic that queries,"), which are subject to 35 U.S.C. § 112 paragraph 6 (pre-AIA). SAP asserts that each claim is invalid as indefinite for failure to recite sufficient structure.

Based on Defendants' present understanding of Plaintiff's Infringement Contentions, at least one or more of these claim terms, phrases, and limitations are indefinite because they are inconsistent with and broader than the alleged invention disclosed in the specification and during prosecution, and given Valtrus's apparent constructions of the claims, any person of ordinary skill in the art at the time of the invention would not understand what is claimed with reasonable certainty, even when the claims are read in light of the specification and prosecution history. Despite the indefiniteness of the claims, the prior art references described in these contentions, alone or in combination with other prior art references, render the claims invalid under any reasonable interpretation of the claims.

'139 Patent

Based on SAP's present understanding of Valtrus's asserted scope of the claims of the '139 Patent, to the extent such positions can be understood from Valtrus's Infringement Contentions, SAP asserts that the Asserted Claims of the '139 Patent are invalid for reciting at least the following claim terms, phrases, or limitations:

- separately in time sequence (claim 1)
- the standby transaction processing system (claim 4)
- a remote mirroring device that is capable of mirroring (claim 5)
- to create an online redo log at the standby site (claim 5)
- computing a difference between ***an*** online redo log (claim 5)

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 92 of 101

- after archiving becomes slow enough that there is a risk of primary database blocking (claim 10, 17)
- the archive replicator (claim 16)
- the standby archive log replicator (claim 18)

These claim terms, phrases, and limitations, as apparently construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112.

Additionally, Claim 5 of the '139 Patent recites a limitation ("a remote mirroring device that is capable of mirroring") that is subject to 35 U.S.C. § 112 paragraph 6 (pre-AIA). SAP asserts that each claim is invalid as indefinite for failure to recite sufficient structure.

Based on Defendants' present understanding of Plaintiff's Infringement Contentions, at least one or more of these claim terms, phrases, and limitations are indefinite because they are inconsistent with and broader than the alleged invention disclosed in the specification and during prosecution, and given Valtrus's apparent constructions of the claims, any person of ordinary skill in the art at the time of the invention would not understand what is claimed with reasonable certainty, even when the claims are read in light of the specification and prosecution history. Despite the indefiniteness of the claims, the prior art references described in these contentions, alone or in combination with other prior art references, render the claims invalid under any reasonable interpretation of the claims.

'738 Patent

Based on SAP's present understanding of Valtrus's asserted scope of the claims of the '738 Patent, to the extent such positions can be understood from Valtrus's Infringement Contentions, SAP asserts that the Asserted Claims of the '738 Patent are invalid for reciting at least the following claim terms, phrases, or limitations:

- selectively indicating to the layer of the protocol stack (claim 1)

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 93 of 101

- context information obtained from a different protocol stack layer (claim 2)
- that the obtained context information is potentially inaccurate or incomplete (claim 10)

These claim terms, phrases, and limitations, as apparently construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112.

Based on Defendants' present understanding of Plaintiff's Infringement Contentions, at least one or more of these claim terms, phrases, and limitations are indefinite because they are inconsistent with and broader than the alleged invention disclosed in the specification and during prosecution, and given Valtrus's apparent constructions of the claims, any person of ordinary skill in the art at the time of the invention would not understand what is claimed with reasonable certainty, even when the claims are read in light of the specification and prosecution history. Despite the indefiniteness of the claims, the prior art references described in these contentions, alone or in combination with other prior art references, render the claims invalid under any reasonable interpretation of the claims.

'264 Patent

Based on SAP's present understanding of Valtrus's asserted scope of the claims of the '264 Patent, to the extent such positions can be understood from Valtrus's Infringement Contentions, SAP asserts that the Asserted Claims of the '264 Patent are invalid for reciting at least the following claim terms, phrases, or limitations:

- a high-speed interconnect (claim 1)
- resource allocation controller coupled to determine (claim 1)
- interconnect apparatus for transmitting (claim 5)
- determining desired processor to partition and upper level cache block allocations to processors (claim 5)

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 94 of 101

These claim terms, phrases, and limitations, as apparently construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112.

Additionally, Claims 1, 5, 9 of the '264 Patent recites numerous limitations ("resource allocation controller coupled to determine," "interconnect apparatus for," "allocation apparatus for," and "upper level cache controller is capable of controlling"), which are subject to 35 U.S.C. § 112 paragraph 6 (pre-AIA). SAP asserts that each claim is invalid as indefinite for failure to recite sufficient structure.

Additionally, all Asserted Claims of the'182 Patent contain both apparatus and method steps of using the apparatus and are thus indefinite under 35 U.S.C. 112(b) or pre-AIA 35 U.S.C. 112, second paragraph. *See In re Katz Interactive Call Processing Patent Litigation*, 639 F.3d 1303, 1318, 97 USPQ2d 1737, 1748-49 (Fed. Cir. 2011).

Based on Defendants' present understanding of Plaintiff's Infringement Contentions, at least one or more of these claim terms, phrases, and limitations are indefinite because they are inconsistent with and broader than the alleged invention disclosed in the specification and during prosecution, and given Valtrus's apparent constructions of the claims, any person of ordinary skill in the art at the time of the invention would not understand what is claimed with reasonable certainty, even when the claims are read in light of the specification and prosecution history. Despite the indefiniteness of the claims, the prior art references described in these contentions, alone or in combination with other prior art references, render the claims invalid under any reasonable interpretation of the claims.

IX. INVALIDITY UNDER 35 U.S.C. § 101 (JUDGE GILSTRAP'S STANDING ORDER REGARDING SUBJECT MATTER ELIGIBILITY CONTENTIONS)

In connection with these contentions, SAP has provided Exhibits SME-A to SME-G ("SM Contentions"), as set forth below:

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 95 of 101

Patent	SME Chart
’409 Patent	SME-A
’244 Patent	SME-B
’182 Patent	SME-C
’575 Patent	SME-D
’139 Patent	SME-E
’738 Patent	SME-F
’264 Patent	SME-G

These SM Contentions address only the Asserted Claims. SAP reserves the right to supplement these SM Contentions if Valtrus asserts infringement of any additional claims beyond the Asserted Claims. These SM Contentions are subject to revision and amendment pursuant to Federal Rule of Civil Procedure 26(e) and the Docket Control Order (Dkt. 32), to the extent appropriate, in light of further investigation and discovery regarding the defenses below, the Court’s construction of the claims at issue, and/or the review and analysis of expert witnesses.

Section 101 lists four broad categories of patent-eligible subject matter but is subject to “an important implicit exception” that “[l]aws of nature, natural phenomena, and abstract ideas,” which form the “basic tools of scientific and technological work,” are not eligible for patent protection. *Alice Corp. Pty. Ltd. v. CLS Bank Int’l*, 573 U.S. 208, 216 (2014) (internal quotation marks omitted). “The ‘abstract ideas’ category embodies ‘the longstanding rule that an idea of itself is not patentable.’” *Id.* at 209 (quoting Gottschalk v. Benson, 409 U.S. 63, 67 (1972)).

Alice set forth a two-step inquiry.

***Alice* step one**. The first step is to “determine whether the claims at issue are directed to one of those patent-ineligible concepts,” e.g., an abstract idea. *Id.* at 217. “*Alice* step one presents a legal question that can be answered based on the intrinsic evidence” and “does not require an

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 96 of 101

evaluation of the prior art or facts outside of the intrinsic record." *CardioNet, LLC v. InfoBionic*, Inc., 955 F.3d 1358, 1372 (Fed. Cir. 2020).

The step one analysis typically begins "with an examination of eligible and ineligible claims of a similar nature from past cases." *Amdocs (Israel) Ltd. v. Openet Telecom, Inc.*, 841 F.3d 1288, 1295 (Fed. Cir. 2016). "Under this inquiry, [courts] evaluate the focus of the claimed advance over the prior art to determine if the character of the claim as a whole, considered in light of the specification, is directed to excluded subject matter." *Trading Techs. Int'l, Inc. v. IBG LLC*, 921 F.3d 1378, 1384 (Fed. Cir. 2019) (quotation omitted).

Where a claim recites "a desired function or outcome, without providing any limiting detail that confines the claim to a particular solution to an identified problem," the "functional nature of the claim confirms that it is directed to an abstract idea." *Affinity Labs of Texas, LLC v. Amazon.com, Inc.*, 838 F.3d 1266, 1269 (Fed. Cir. 2016). The "essentially result-focused, functional character of claim language has been a frequent feature of claims held ineligible under § 101." *Elec. Power Group, LLC v. Alstom S.A.*, 830 F.3d 1350, 1356 (Fed. Cir. 2016)

***Alice* step two**. If a claim is directed to ineligible subject matter, the second step is to "determine whether [any] additional elements transform the nature of the claim into a patent-eligible application" by reciting "an inventive concept—i.e., an element or combination of elements that is sufficient to ensure that the patent in practice amounts to significantly more than a patent upon the ineligible concept itself." *Alice*, 573 U.S. at 217-18 (quotations omitted). "What is needed is an inventive concept in the non-abstract application realm." *SAP Am., Inc.*, 898 F.3d at 1168. Even if "the techniques claimed are groundbreaking, innovative, or even brilliant, [] that is not enough for eligibility" if "the advance lies entirely in the realm of abstract ideas." *Id.* at 1163.

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 97 of 101

To the extent claims include non-abstract elements, they are still ineligible if they recite "well-understood, routine, conventional activities previously known to the industry." *Alice*, 573 U.S. at 225 (quotation omitted). The "inquiry is not whether the claimed invention as a whole is unconventional or non-routine," but "whether the claim limitations other than the invention's use of the ineligible concept to which it was directed were well-understood, routine and conventional." *BSG Tech LLC v. BuySeasons, Inc.*, 899 F.3d 1281, 1290 (Fed. Cir. 2018).

Pursuant to Sections (a)(1)-(3) of the Court's Standing Order Regarding Subject Matter Eligibility Contentions, SAP has produced as SME-A to SME-G a chart for each of the Asserted Patents that identifies each exception to subject matter eligibility; describes the industry in which the challenged claims were well-understood, routine, and conventional at the relevant time; and identifies the factual and legal bases for how the challenged claims are otherwise ineligible for patent protection.

X. ACCOMPANYING DOCUMENT PRODUCTION

Pursuant to Patent Rule 3-4(a), SAP incorporates by reference its prior production SAP_VAL_0000001 - SAP_VAL_0014175 and is concurrently producing additional documents, including SAP_VAL_0014264 - SAP_VAL_ 0351031. In addition, SAP has identified relevant source code and is in the process of making it available for inspection on reasonable notice. SAP's investigation is ongoing. If and when any additional documents required to be disclosed under this rule are discovered, SAP will timely produce them.

In addition, SAP directs Valtrus to publicly available repositories or third parties from which relevant information related to the operation and functionality of the Accused Products may be access including but not limited to: (1) Intel, (2) Ampere, (3) AMD, (4) the Apache Kafka Project, (5) the Apache Camel project, and (6) the Apache Qpid project.

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 98 of 101

Pursuant to Patent Rule 3-4(b), SAP is concurrently producing copies of the identified prior art as SAP_VAL_0351032 - SAP_VAL_0360577 and SAP_VAL_0360578 - SAP_VAL_0360696. SAP's investigation is ongoing. SAP further identifies Actaworks documents produced within the ranges provided in the paragraphs above. If and when any additional documents required to be disclosed under this rule are discovered, including any documents received in response to the subpoenas listed in Section II.C., SAP will timely produce them.

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 99 of 101

DATED: May 20, 2024

Respectfully submitted,

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SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 100 of 101

CERTIFICATE OF SERVICE

The undersigned hereby certifies that a true and correct copy of the above and foregoing document has been served on May 20, 2014, via electronic mail to all counsel of record for Plaintiff.

/s/ Michael A. Bittner
Michael A. Bittner

SAP - Exhibit 1114
SAP v. Valtrus et al. - IPR2025-00419
Page 101 of 101