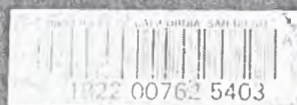


HANDBOOK OF ELECTRONIC PACKAGE DESIGN



**EDITED BY
MICHAEL PECHT**

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This back-side metallization is typically a diffused gold. The wafer is then diamond sawed into individual chips or dice.

2.9 PACKAGING STYLES

The transistor, one of the first semiconductor devices, was developed to replace the bulky vacuum tube. Semiconductors were initially packaged in cans, called to-cans, which are round capped packages with leads extending from the base. To-cans became difficult to work with as the number of I/O pins required by semiconductor devices began to rise. As a result, new forms of packages for semiconductor integrated circuits were developed. Some of the common package outlines are shown in Figure 2.27.

2.9.1 Dual In-Line Package Plastic Dual In-line Packages

One of the earliest packaging standards is the rectangular dual in-line package (DIP). The DIP has I/O leads which extend from two opposite sides of the package and are bent downward (Figure 2.28). DIPs have been a main stream of the microelectronics industry since 1968 and still account for some 80% of all packaging of integrated circuits. However, the application of DIPs has been reduced because of newly emerging packages such as chips carriers, small-outline integrated circuits (SOICs) and pin-grid arrays (PGAs).

DIPs were invented to overcome the difficulty associated with handling and inserting packages onto mounting boards, typically called printed wiring boards (PWBs). The leads of DIPs are inserted through holes in the PWB and soldered to the back of the board. With DIPs, it has become possible to service these boards in the field with standard hand tools and soldering irons.

Plastic DIPs consist of a lead frame typically made of kovar. The lead frame is punched out of sheet metal in the desired shape, which normally includes a small platform or pad at the center with the leads fanning out from this pad. The leads are formed so that they bend down for insertion onto the PWB. This lead frame is then plated with nickel as an underplate, or corrosion barrier, and tin or gold surface plating for wire bondability and/or solderability. The semiconductor die is then mounted to the center pad of the lead frame and the I/O pins of the die are wire bonded to the appropriate leads. The entire assembly is then molded in plastic, forming the plastic DIP body.

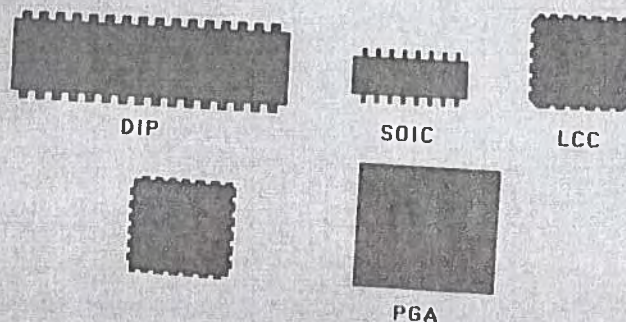


Figure 2.27 Common package outlines.

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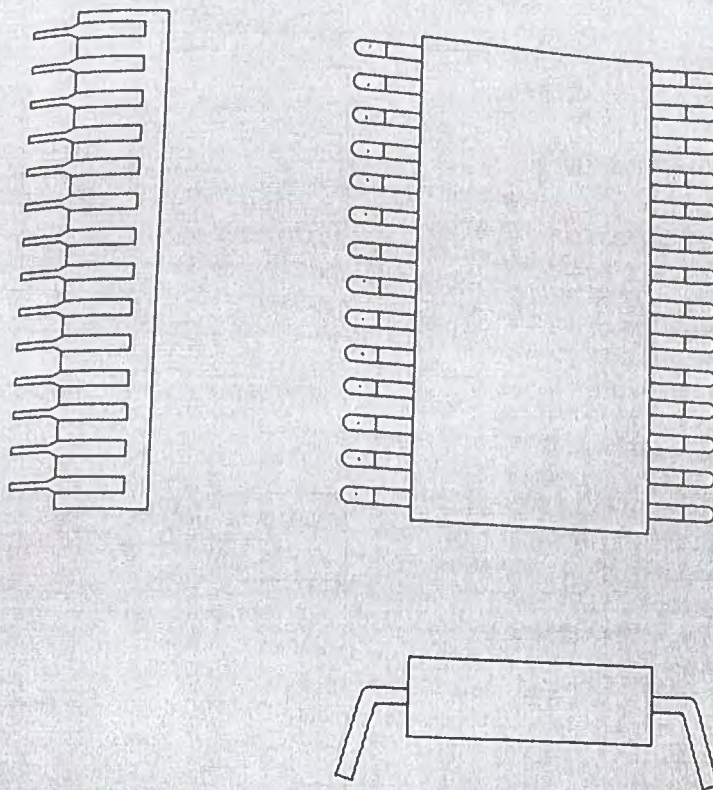


Figure 2.28 Dual in-line package.

Since 1972 most plastic packages have been made of Epoxy B or Novalac. Plastic packages are available with up to 68 leads. Above 68 leads, molding and lead frame problems limit the production of larger DIPs because of excessive costs. Up to 68 leads, the manufacture of chips in plastic packages is easily automated, which is one of the prime reasons for their popularity.

Environmental tests on a plastic-encased 4096-bit random access memory have been conducted by Texas Instruments. The test showed that most failures occurred in the pressure-cooker test, which is equivalent to putting the ICs in steam. Although the conditions are rarely found in actual operation, this test indicates that plastic DIPs are most vulnerable to moisture. Still, in the real world, plastic DIPs function reliably in most consumer, computer, and industrial applications where coupled high temperature and high humidity is not encountered.

The advantages of plastic DIPs are low cost and a predictable uniform factor. Furthermore, they have the fewest infant mortality failures of any packaging type. The cofired or multilayer alumina ceramic DIPs are the most reliable after screening and the most expensive insertion mount components.

Plastic-encapsulated ICs use an injection-molded epoxy or silicone encapsulant and are not suitable for high-temperature operation. Because most plastic encapsulants are susceptible to moisture ingress via permeation, they have not been recommended for use in high-temperature/moisture environments. Moisture provides a medium for electrolytic

corrosion at wire bonds or conductor tracks through any gaps or holes in the glassivation layer.

Ceramic Dual In-Line Packages

Plastic DIPs are typically used in commercial applications, whereas military systems typically utilize ceramic (alumina) DIP packages. In ceramic packages, the integrated circuit die is sandwiched between the two ceramic plate elements. The element on the bottom half of the sandwich holds the integrated circuit die. The ceramic section on the top of the sandwich protects the integrated circuit die from mechanical stress during sealing operations. Each of the ceramic elements is coated with low-melting-temperature glass for subsequent joining and sealing.

Ceramic packages are preferred for high-quality electronic systems, where increased reliability takes precedence over increased cost. Ceramic packages are typically made from either beryllia or alumina. Beryllia has better thermal characteristics than alumina; however, beryllia can be toxic if inhaled in a powdered form. For this reason, alumina is the most widely used ceramic material in packaging. Alumina is superior to epoxy in terms of heat transfer and hermeticity. Alumina packages are more expensive than epoxy because of higher material costs and higher manufacturing costs.

The leads of ceramic DIPs, like the leads on plastic DIPs typically have a pitch of 100 mils (1 mil equals 0.001 in.). The materials of the DIP lead frame are mainly kovar (high-nickel steel) or copper. The lead frame is stamped and bent into its final shape. The excessive material is intended to preserve pin alignment. The holes at each end are for the keying jig used in the final sealing operation. The lower half of the ceramic package is inserted into the lead frame. The die is mounted in the well and leads are attached. The top ceramic element is bonded to the bottom element, and the excess material is removed from the package.

The manufacture of multilayer ceramic DIPs, often called cer paks, is an elaborate process. The basic element is uncured (green) alumina tape. Screened onto the top of the tape are metalized patterns, which where necessary include vias (square holes filled with the screened-on metal) for connection to other layers. These metallized layers are then laminated together and fired in a furnace, creating a strong, monolithic structure. A lead frame is brazed to the top or side of the package, which can now be shipped to the user along with the metal lid. The user then mounts the desired die into the cavity of the cer pak and wire bonds the I/O pads of the die to the appropriate wire bond pads of the cer pak. These pads are connected through the multilayers of the package to the brazed-on leads. The first cer paks were design to be one-for-one replacements for DIPs. Thus, these first units were rectangular and had 100-mil centered leads extending from the two long sides of the package. However, the cofired process allowed for finer line resolution, so cer paks are now available in much smaller sizes and lead pitches. Development of the chip carrier soon followed that of the cer pak, so the use of cer paks never really caught on. For more information on the cofired ceramic process, see Chapter 3.

The cofired DIP can handle as many as 68 leads successfully and is at present the largest cofired DIP available. Since this unit is about 3.2 in. long by 0.9 in. wide, it is doubtful whether there will be too many packages made that are large. Other advantages of cofired ceramic DIPs are true hermeticity and superior heat dissipation. The ceramic DIPs are superior to plastic DIPs in lead strength, because the lead frames are brazed on.

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Designing a new package typically requires 10 to 18 weeks and \$5000 to \$35,000 for tooling costs. Ceramic is fragile, making it harder to ship and handle automatically than plastic packages.

DIPs have been used by the military and in industry for a long time; therefore, problems associated with DIPs and the failure mechanisms of through hole leads are well known and most of the problems have been solved. DIPs, however, have the limitation that as the number of the leads is increased, the DIPs take too much space on a printed circuit board. In particular, the smallest mounting hole that can be drilled on a circuit board is 40 mils. As the lead count of the die increases the area for mounting the DIPs increases at an even greater rate.

With the introduction of VLSI, the lower available pin counts of a rectangular DIP have become a limiting factor. With pins spaced 100 mils apart on only two sides of the package, the size and weight of the DIPs have become too great. Consequently, the cost of drilling holes for DIP insertion has also become a problem. For example, a DIP with 64 pins is 0.9 by 3.2 in. with 100-mil pin spacing. On the other hand, the size of the circuit elements has been reduced, which in turn has led to reduced power consumption and chip delay time due to greater circuit integration, thus reducing the cost per circuit function. As a result, DIP packages have become up to 50 times as big as the chips themselves, which defeats the objective of shrinking the size of the integrated circuits. Thus DIPs are not an effective packaging method for VLSI.

2.9.2 Flatpack Packages

With the increase in IC pin count, other methods of packaging and mounting have appeared. The emergence of surface- or planar-mounted components has overcome some of the space problems associated with through hole mounting and the high-pin-count DIP packages.

One of the earliest forms of surface-mounted (as opposed to through hole-mounted) components is the flatpack. The flatpack is similar to the DIP with the exception that the leads are bent outward to form a flat surface and are mounted on pads rather than inserted into holes in the board. Flatpacks are found in both dual in-line configurations called small outline integrated circuits (SOIC) and with leads which protrude on all four sides of the component package. SOICs typically have gull wing-type leads and are preferred for lead counts up to 20 pins.

2.9.3 Chip Carrier Package

The chip carrier is a package (often square) with I/O connections on all four sides. There are three main types of chip carriers: ceramic and plastic leaded chip carriers and leadless ceramic chip carriers (LCCCs often just called LCCs). Figures 2.29 shows a typical leadless chip carrier geometry. Figure 2.30 shows a leaded ceramic chip carrier before and after lead forming. In this case the leads are top brazed and are formed in a gull-winged (stepped) fashion for surface mounting. The chip carriers have notches in three corners to ensure proper mounting orientation.

Chip carriers offer higher packaging densities than their corresponding DIP packages. For comparison, a 28-pin DIP is 3.725 cm long and 1.475 cm wide and has a 0.5-cm² chip-mounting area. A 28-lead chip carrier is 1.125 cm on each side with a slightly larger chip capacity (Figure 2.31).

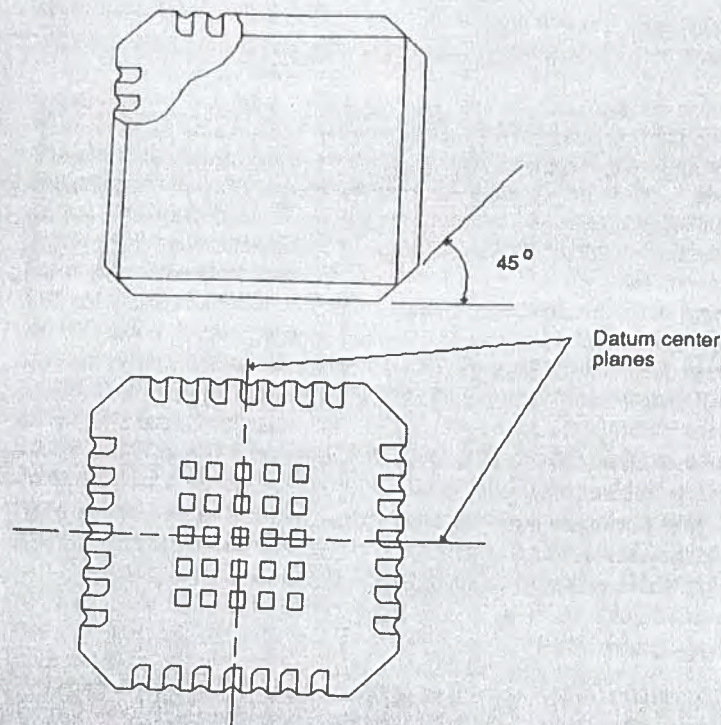


Figure 2.29 Leadless chip carrier geometry with thermal pads.

Chip carriers having 16 to 84 terminals meet the requirements of the Joint Electronic Device Engineering Council (JEDEC). The JEDEC standards include two families, 50 mils and 40 mils terminal pitch. Above 84 terminals there are as yet no generally accepted standards, although JEDEC has proposed certain terminal counts and configurations with up to 264 terminals and 25 and 20 mils pitch. Non-JEDEC chip carriers are available in single layer, multilayer, cavity up, cavity down, rectangular, and square configurations. Chip carriers are available in plastic, alumina, beryllia, and aluminum nitride, with thick-film, thin-film, and cofired metallizations. They are open tooled (meaning the tooling is open to the public for purchase) with lead counts over 300.

Plastic Chip Carriers

The plastic leadless chip carriers were developed in the early 1980s by Texas Instruments as a low-cost alternative to the leadless chip carriers. Plastic chip carriers are fabricated in the same manner as plastic DIPs. The leads on a plastic chip carrier can have the same configuration as the DIPs for insertion mounting. They can also be formed in a gull-winged DIP configuration or a J-lead configuration for surface mounting. Gull-winged chip carriers have the same lead configuration as flatpacks. J leads start off similar to DIP leads, but are bent up just below the package in the shape of a J.

Ceramic Chip Carriers

Single-layer leadless chip carriers, or SLAMs, have a conductor pad at the center of the chip carrier for mounting the die. Surrounding the die are wire bond pads. These pads are normally on 0.008-in. centers which match the bond pads of most dice. Conductor tracks fan out from these wire bond pads, connecting them to the I/O of the package. The dice are mounted and wire bonded prior to sealing the package by attaching a dome-shaped lid with a glass sealant.

Multilayered chip carriers (see Figure 2.32 for examples) are fabricated using cofired ceramic technology. They do not have leads, just conductors routed through the layers' central cavity. The die is secured in the package's contacts on the top side. The most common LCCs are designed by JEDEC. JEDEC type A has the contacts on the top side. Type B has the contacts on the edges as well as the top and bottom. Type C is different from type B in the way the corners are shaped. Figures 2.33 through 2.38 give examples of the different JEDEC chip carriers.

All ceramic chip carriers can be configured to be leadless or leadless. For leadless chip carriers, leads are brazed onto the I/O pads along the perimeter of the package. Type A chip carriers would have the leads brazed to the top of the case, hence the term top-brazed chip carrier. These top-brazed leads can be formed into gull-winged packages for surface mounting (see Figure 2.30). They are formed in a step-down shape to the PWB. These steps offer enough stress relief to handle the mismatch in coefficient of thermal expansion (CTE) of the chip carrier and the PWB. Figure 2.39 shows a leadless chip carrier mounted to a PWB. Types B and C can have the leads brazed to the top of the carrier, to the bottom, or along the side. The side braid configuration is similar to DIPs and is used for insertion mounting.

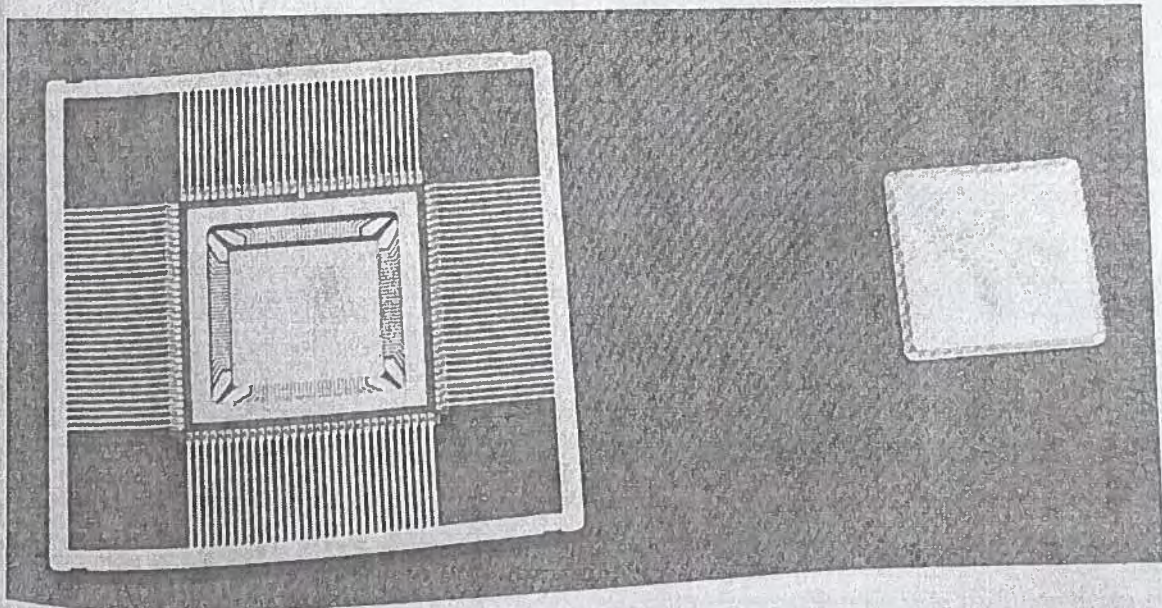


Figure 2.30(a) Leadless ceramic chip carrier.

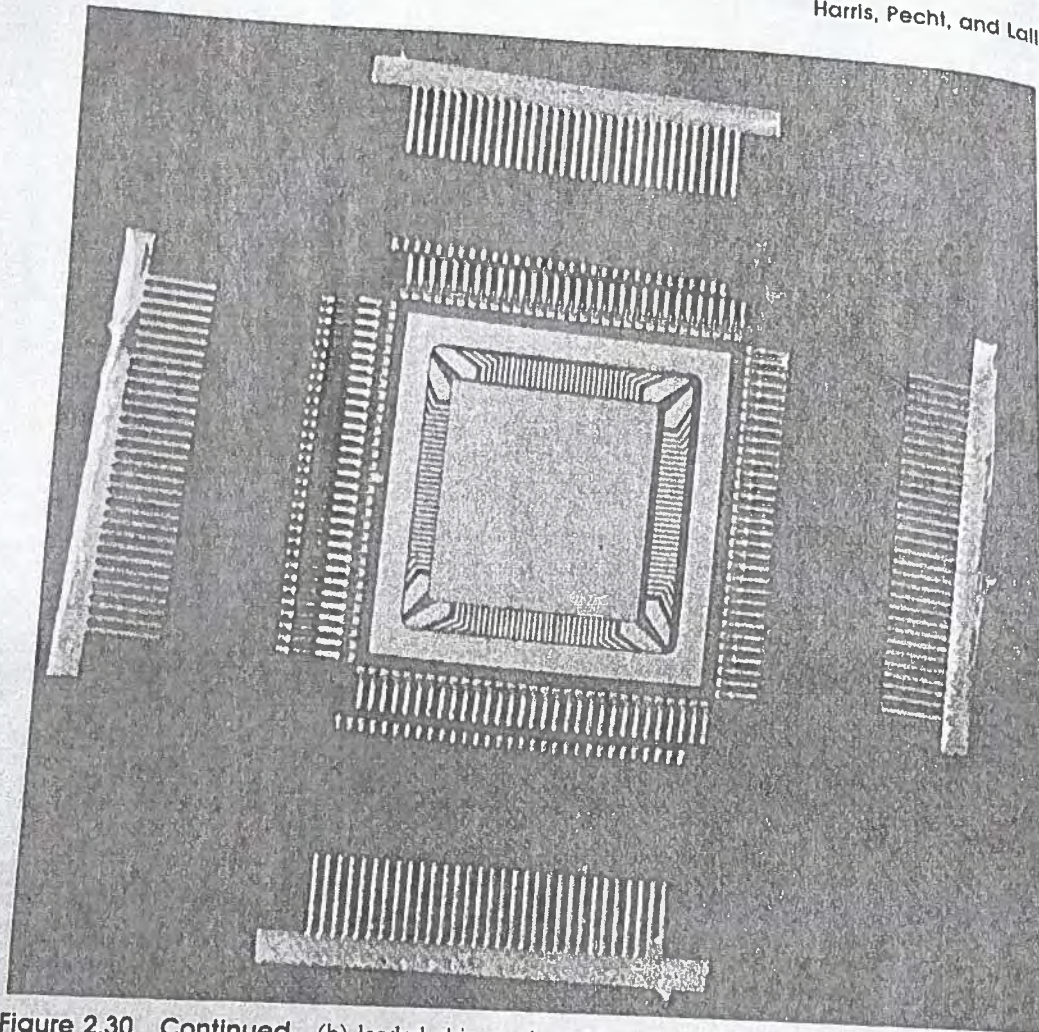


Figure 2.30 Continued (b) leaded chip carrier with gull-wing formed leads for surface mount. (Courtesy of Westinghouse ESG.)

Leadless chip carriers have "castellations" instead of leads. A semicylindrical column is cut out of the side of the chip carrier at every I/O. The insides of these columns are metallized the same way that vias between the layers are metallized. They are then plated as is all external metallization of the package. The plating used is typically nickel followed by gold. To attach LCCs to the board, solder in paste form is applied, components are placed, and joining is accomplished by heating (e.g., vapor phase or infrared reflow), which melts and solidifies the solder. During the reflow process, the molten solder wicks up the metallized columns to form the solder joints, as shown in Figure 2.40. Prevention of solder joint cracking under extremes of temperature requires closely matching the CTEs of the LCCs to the mounting boards. (See Chapter 4 for more details on the surface mount process and design considerations.) Leadless chip carriers can be reworked by reflowing

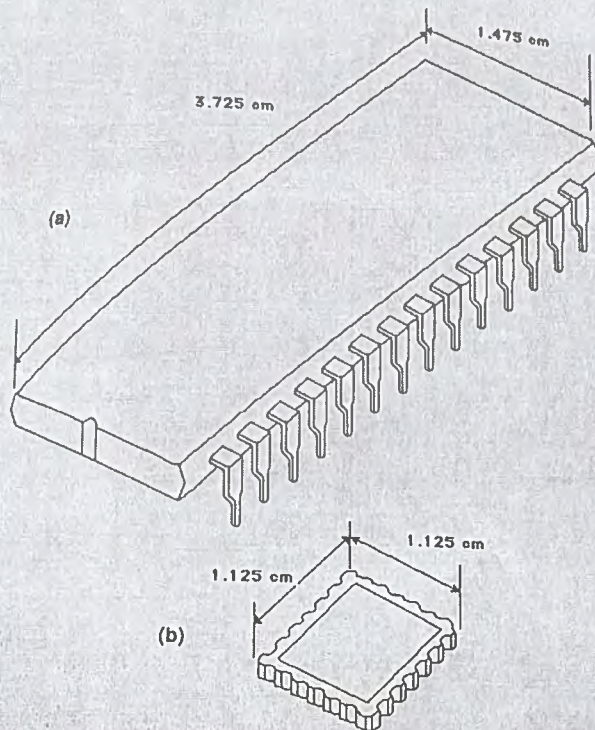


Figure 2.31 DIP versus LCC comparison.

the solder joints with the aid of an extractor, as shown in Figure 2.41. An extractor is nothing more than a soldering wand with an end effector in the shape of the chip carrier to be removed.

Inserting a type A leaded chip carrier face down in sockets puts the primary heat-dissipating surface away from the mounting surface, resulting in more effective cooling. Type B has notches for sockets, but the chip carriers can also be soldered directly to boards. Type C LCCs have beveled corners instead of notches, and they are meant to be soldered directly to boards.

LCCs with a typical pitch of 40 or 50 mils take up as little as 30% of the room required by DIPs that have the same lead count. Alumina LCCs typically have a much smaller coefficient of thermal expansion than the standard organic printed circuit boards they are soldered to. As a result, heat cycling in a system, which can cause repeated strain on the solder joint, will eventually cause fatigue failures. Therefore, it is recommended that only leaded chip carriers be mounted on organic PWBs. However, if a ceramic PWB is to be used, leadless ceramic chip carriers can be surface mounted with very high reliability.

Figure 2.42 shows the relationship between the wiring length of the package and the number of pins for various package types. TAB is the most efficient packaging technology with respect to wiring length. This is an important consideration, since the wire length determines the time for the signal to propagate from one chip to the next.

estate for such spacing may not be available. Since the current or charge travels on the surface, one way to increase spacing between two tracks without increasing the area needed for the design is to break up the substrate into different subassemblies. When this is done, the path of potential arcing must travel down the side of one substrate, across the floor of the case, and up the side of another substrate, as shown in Figure 4.12. Thus, without increasing the needed surface area, the spacing between two high voltage potentials is increased threefold.

4.2 CHIP CARRIER ASSEMBLIES

Chip carriers are plastic or ceramic packages that carry a single chip or die. Chapter 2 discussed the outline configuration of various chip carriers. The assembly processes used to make chip carriers are very similar to those used to make dual in-line packages (DIPs) for plastic chip carriers or ceramic packages (cer paks) for ceramic chip carriers.

4.2.1 Plastic Chip Carrier Fabrication and Design

The first step in fabricating a plastic chip carrier is to punch or etch a lead frame pattern into sheet metal, typically kovar that has been plated with nickel and gold. The die is epoxied to the center of the lead frame and then wire-bonded accordingly. The lead frame with die and wire bonds is then encapsulated within a plastic mold. In the case of plastic chip carriers, the leads that extend out of the molded body can have a gull-winged or DIP configuration or be shaped like the letter J, hence the name J-leaded chip carriers. (Plastic chip carriers are always leaded.)

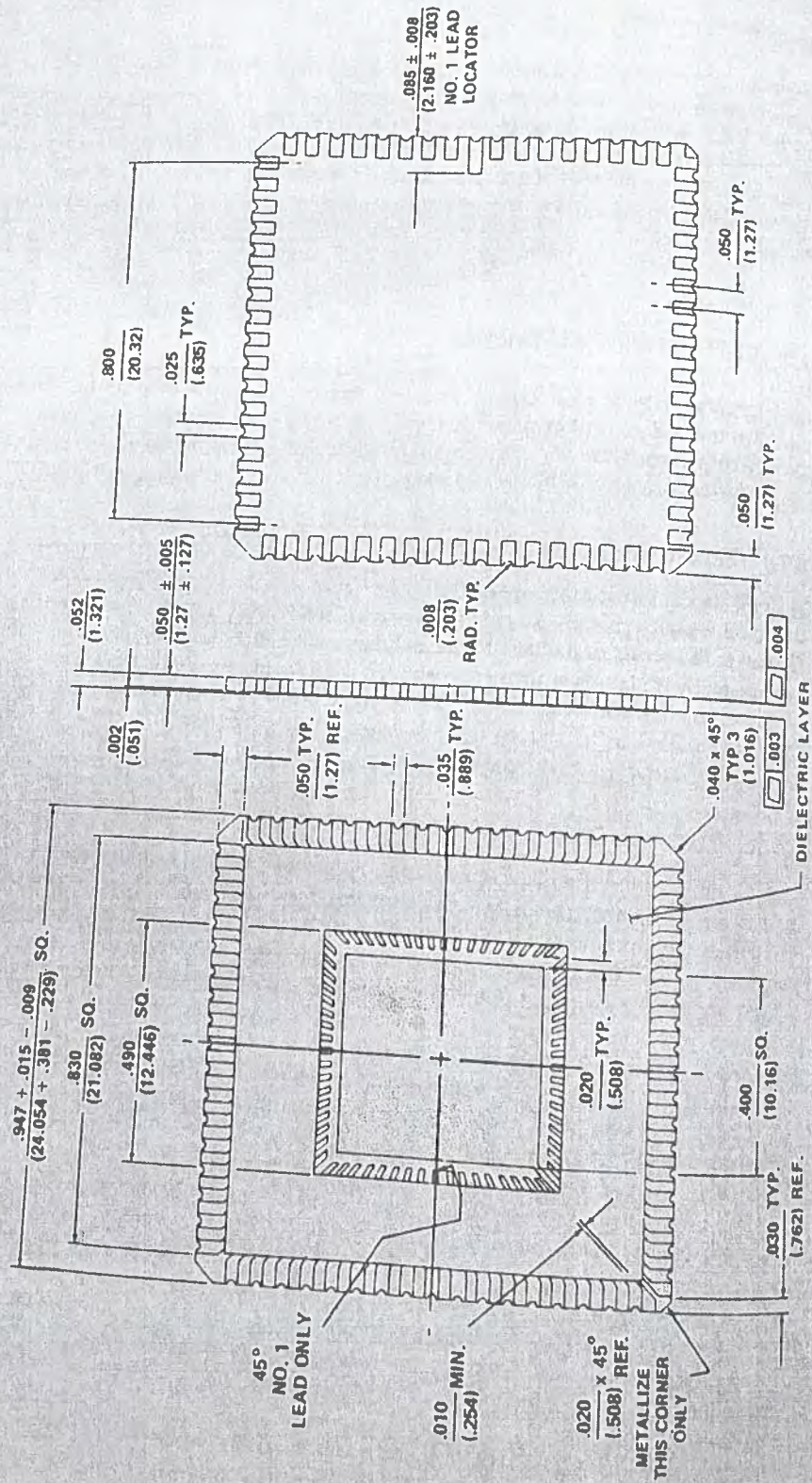
4.2.2 Ceramic Chip Carrier Fabrication and Design

Ceramic chip carriers are made of cofired ceramic with tungsten metallization. See Chapter 3 for a review of the cofired process. Any exposed tungsten is nickel and gold plated. The ceramic body is available in two styles, slam or flatpack, and multilayered with a cavity for the die. The slam chip carrier can be single or multilayered. The die mount pad is the center of the slam and is surrounded by the wire bond pads. These wire bond pads via down to the buried layer and/or fan out toward the edge of the chip carrier, where they either via up to the top of the castellation or via down to the solder mount pad/castellation, in the case of a multilayered design. On the surface of the chip carrier surrounding the wire bond pads is a ring frame of metallization used to solder mount a dome-shaped lid or has a domed lid glass mounted in the case of a single layer design. Figure 4.13a shows the configuration of a slam chip carrier.

Multilayered ceramic chip carriers are cofired ceramic layers with windows cut out in the top layers. When these layers are fired together the windows form a cavity. The bottom layers of the chip carrier form the bottom of the package. The next layers have small windows that form the lower cavity where the die is mounted. The third set of layers, with a slightly larger window, form the wire-bonding ledge within the chip carrier. The top layer has the metallization ring surrounding the window, which is used for solder sealing the lid onto the chip carrier. Figures 4.13b & 4.14 give examples of multilayered chip carriers.

Chip carriers are available in a cavity-up or cavity-down configuration. In a cavity-up design, the cavity faces up from the surface mount pads on the bottom of the package.

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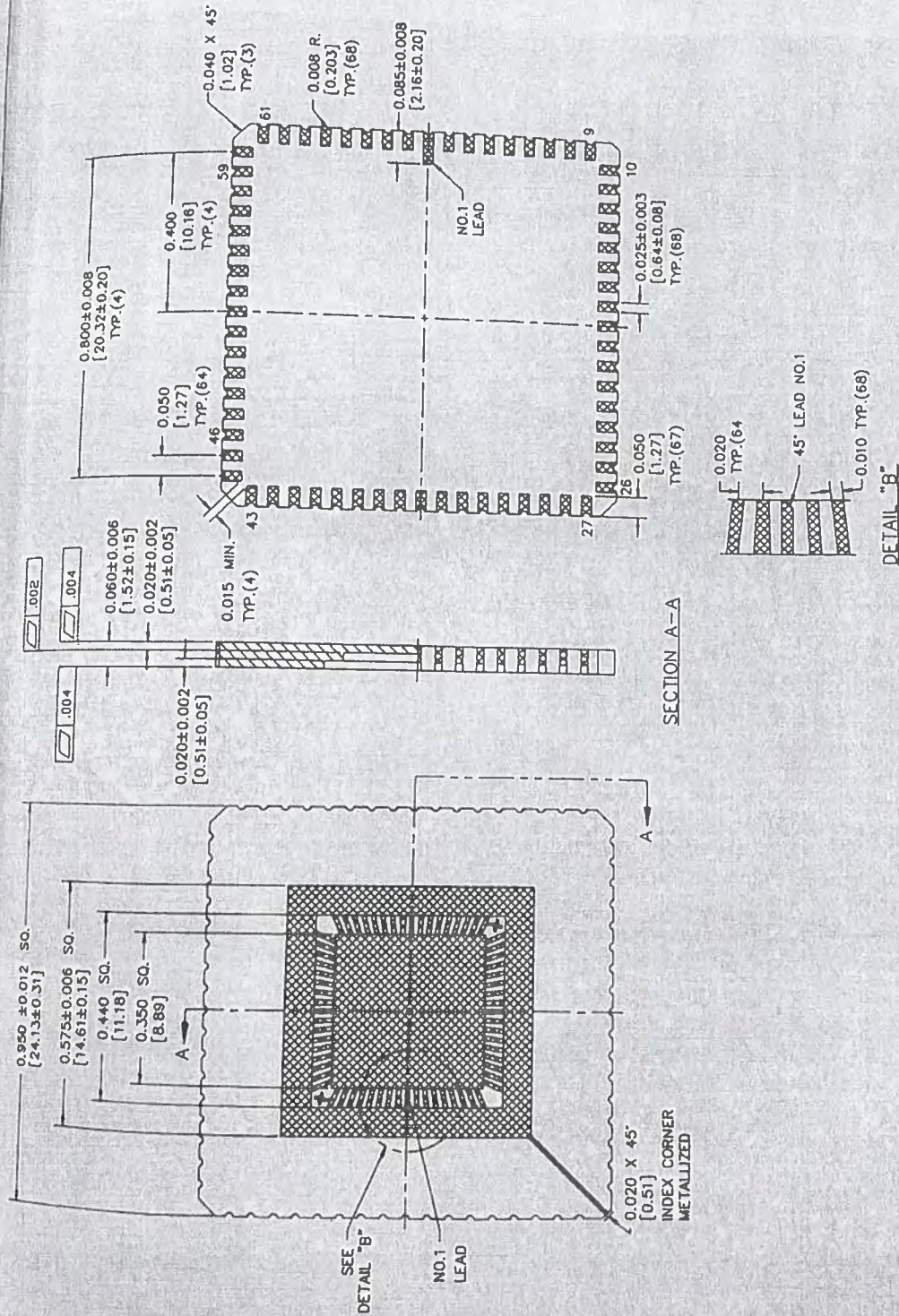


Figure 4.13 (Top) Slam ceramic chip carrier. Single-layer chip carrier requires domed lid. Example shown is an open tool 68 pin LCC. (Bottom) Multilayer ceramic chip carrier. Example shown is an open tool 68 pin LCC. (Courtesy of Kyocera America.)

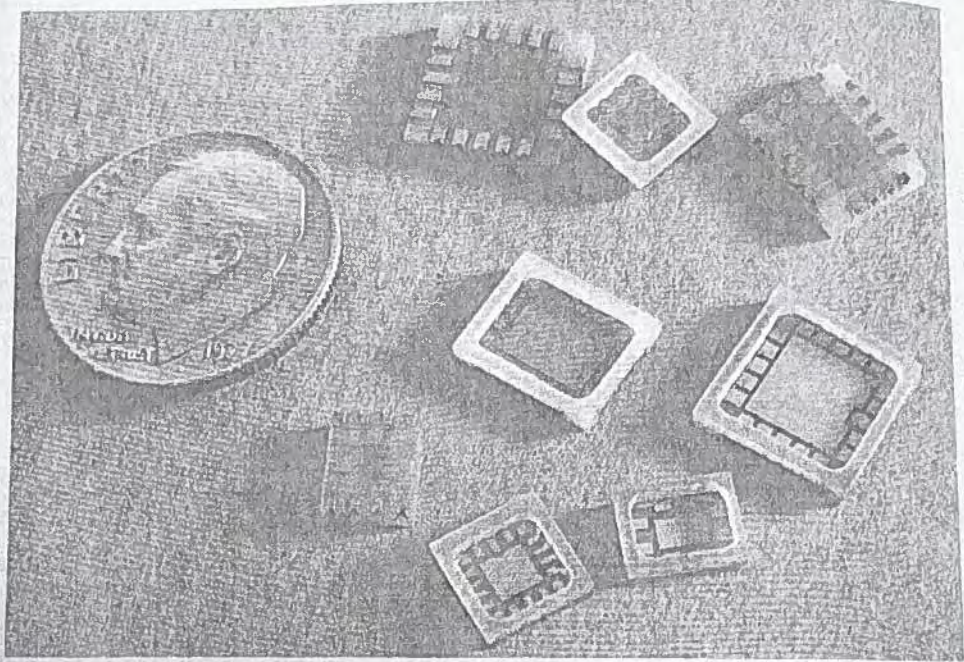


Figure 4.14 Examples of multilayered chip carriers. (Courtesy of Westinghouse ESG.)

In other words, the lid goes on the top of the package and the bottom of the package is mounted down to the PWB. In a cavity-down package the lid is on the bottom of the package and is placed down on the PWB. A cavity-up package is used in traditional mounting configurations in which both routing and thermal path are directed down through the PWB. A cavity-down package allows the routing to be directed down to the PWB, but the thermal path is directed toward the top of the package, away from the PWB. This thermal design is sometimes used in convection-cooled systems.

Ceramic chip carriers are available in a variety of lead configurations, as discussed in Chapter 2. Leadless chip carriers have castellations. When the chip carriers are fabricated, the green tape used to make them is larger than the desired package, even with consideration of the shrinkage of the tape during firing. Holes are punched into all the tape layers around the outer perimeter of the chip carrier. The edges of these holes are metallized with the tungsten. After the layers are laminated together, the prefired stack-up is cut to size. The outer ring of green tape is cut off. This cut runs through the holes, leaving evenly spaced semicircular columns around the outer perimeter of the chip carrier. These metallized half-circles form the castellations. The castellations provide a column of metal that allows the solder to flow up, forming the solder fillet during the surface-mounting process. Figure 4.15 shows a leadless chip carrier mounted to a board. Note the solder fillets that have formed in the castellations. Figure 4.16 shows a leaded chip carrier mounted to a board. Here the leads have been top brazed to the package to give the standard gull-winged

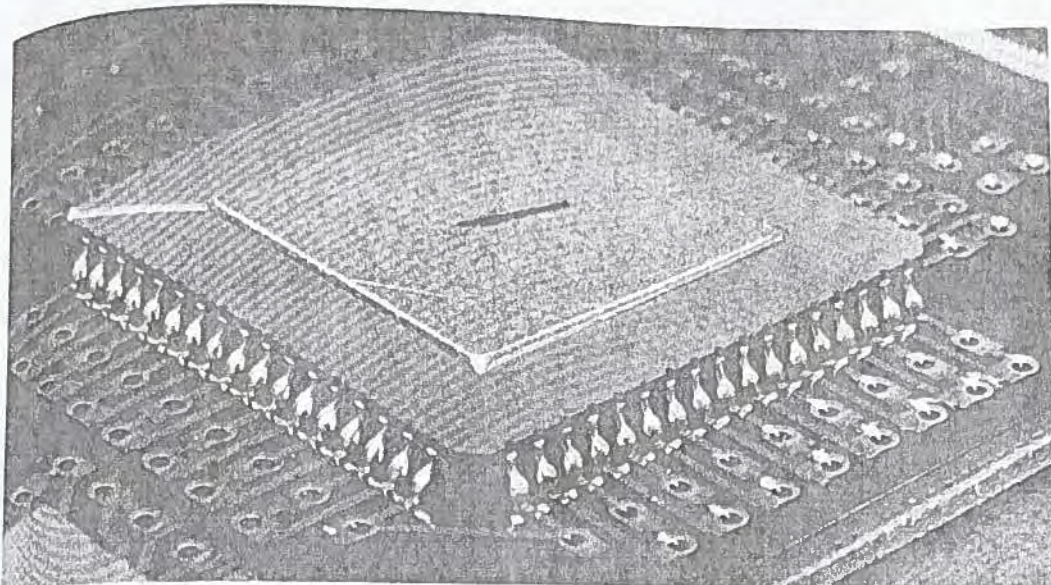


Figure 4.15 Leadless chip carrier (LCC) mounted to a PWB. (Courtesy of Westinghouse ESG.)

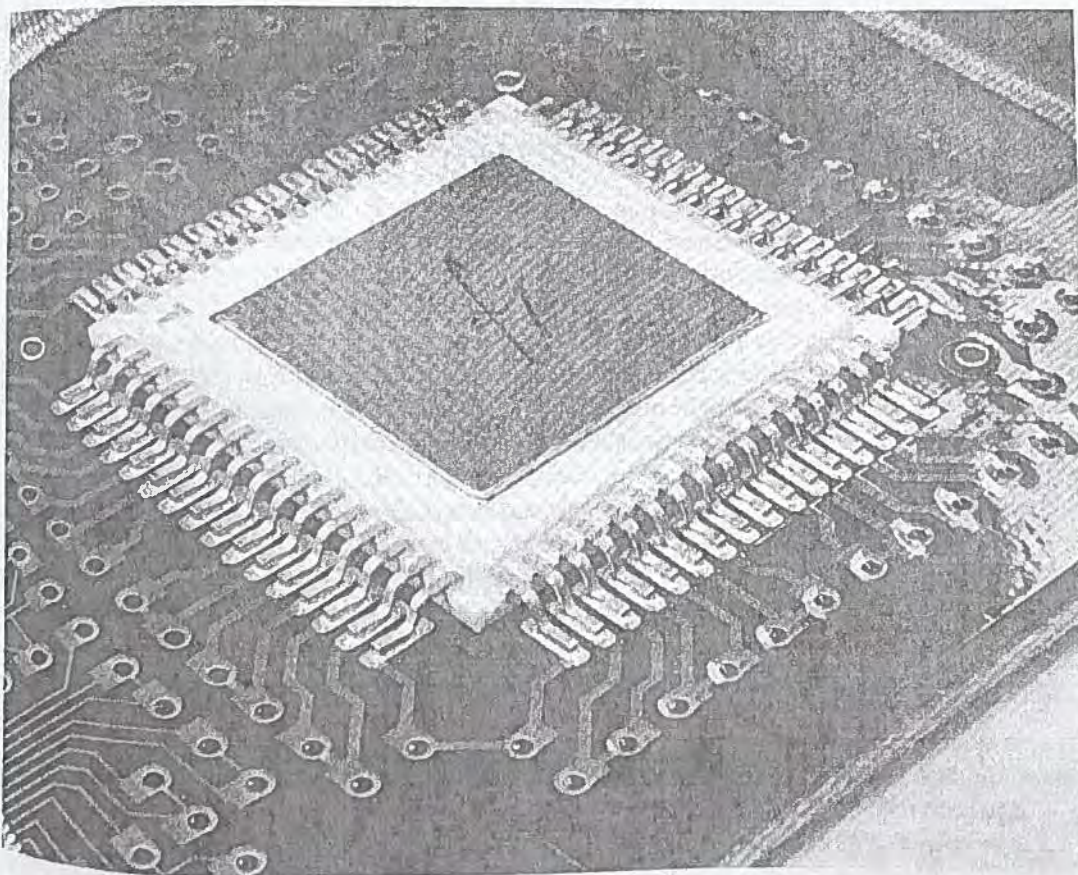


Figure 4.16 Gull winged chip carrier mounted to a PWB. (Courtesy of Westinghouse ESG.)

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Leaded chip carriers are fabricated in the same manner as leadless ones, with an additional step of brazing on leads after the plating of the exposed tungsten metallization. The leads are kovar (with nickel and gold plating). The leads are attached using a high-temperature braze, such as a eutectic copper-silver. As discussed in Chapter 2, the leads can be brazed to the top of the package, in a gull-winged configuration; to the bottom of the package; to the side of the package, for insertion mounting; or to the side of the package in a J-lead form for surface mounting.

4.2.3 Pin Grid Array Packaging

Pin grid array (PGA) packages are high-lead-count chip carriers. To accommodate the high lead count without increasing the perimeter of the chip carrier, the I/O is designed into an array of pads on the bottom of the package instead of a single row along the package perimeter. The leads are pedestals that are brazed onto the array of pads, yielding an array of pins for insertion mounting to the PWB. Likewise, to accommodate the high I/O count dual ledges for wire bonding are typically found inside a PGA. PGAs are available in both cavity-up and cavity-down configurations.

4.2.4 Chip Carrier Assembly Processing

Chip carrier processing is very simple. The die is mounted with epoxy or a solder preform. The die is then wire bonded by thermocompression or thermosonically. (These mounting and bonding methods are discussed in detail under Die Assembly Processing.) After a bake out within a dry nitrogen or vacuum oven to outgas all potential contaminants, the lid with preform is clamped on top of the seal ring of the chip carrier. The lid is ceramic with a metallized ring along the perimeter that matches the seal ring on the chip carrier, or is nickel- and gold-plated kovar with a ring-shaped solder preform tacked along its perimeter. The solder preform is eutectic gold-tin. The chip carriers with their clamped-on lids are run through a furnace programmed to reflow the gold-tin solder. After the chip carriers are removed from the furnace, they are tested. For military and space applications, this testing will include burn-in. The final product is available with the nickel/gold-plated finish or with a pretinned finish. Pretinning involves dipping the chip carrier into a solder pot of 60% tin-40% lead solder.

Dice can also be mounted inside the chip carrier with tape-assisted bonding (TAB) techniques. These techniques will be discussed in detail under Interconnection.

Chip carriers are sometimes customized during the assembly process. In this case, a pattern of separate mounting pads is laser scribed into the cavity. This permits mounting multiple components without shorting all the terminations and/or back planes together. The components are then mounted with epoxy, wire bonded, and sealed as before. These customized chip carrier assemblies are referred to as chip carrier hybrids.

testing, temperature extremes must be carefully chosen to avoid introducing nonrepresentative material behavior such as softening of the substrate epoxy.

Good fatigue data for solder in the open literature are scarce. Different investigators have used different test methods and test parameters, recorded different variables, and interpreted their answers in different (sometimes erroneous) ways. The data are confusing and conflicting at best and misleading and incorrect at worst. It is extremely important to realize that the fatigue behavior of most materials is different in axial and shear modes. Consequently, the experimental data must be chosen carefully to model the actual loading situation encountered in practice. In multiaxial situations, multiaxial fatigue analyses will be required. Some of the most useful information has been developed by Solomon [12, 38], who mechanically strained solder joints under different conditions of temperature and frequency. Most of his experiments were on lap shear specimens, and he presented a relationship between the plastic strain range (unlike Wild [42], who used the total strain range) and cycles to failure, in accordance with the classical Coffin-Manson law for low-cycle fatigue. Figures 8.11a and 8.25a and b show his data for eutectic tin-lead solder, showing that the number of mean cycles to failure for a given shear strain range increases with frequency and decreases with increasing temperature. Typical operating temperatures would fall within his temperature extremes of -50°C and 150°C , and his lowest test frequencies of 10^{-4} Hz are adequate for normal functional frequencies of about 4 cycles per hour. Other comprehensive fatigue studies may be found in Wild [42].

Other attempts at generating Coffin-type frequency-modified fatigue data for solders have met with limited success. The best results have come from corrections to c , the fatigue ductility exponent, and only minor corrections to ϵ_f , the fatigue ductility coefficient. Engelmaier [18] determined from Wild's experimental data for 63/37 and 60/40 SnPb solder [42] that the fatigue ductility exponent can be represented by

$$c = -0.442 - 6(10^{-4})T_s + 1.74(10^{-2}) \ln \left(1 + \frac{360}{t_D} \right) \quad (8.57)$$

where T_s is the mean cyclic solder joint temperature ($^{\circ}\text{C}$), t_D is the half-cycle dwell time (minutes), and the fatigue ductility coefficient is

$$2\epsilon_f = 0.65 \quad (8.58)$$

Besides temperature, loading frequency, and dwell time, there are other factors that drastically affect solder fatigue life. Impurities or contaminants can drastically reduce fatigue life. As an example, 6% gold added to a eutectic PbSn solder has been shown to reduce fatigue life by a factor of 4 due to embrittlement from the formation of AuSn intermetallics. Such phenomena are observed when gold from plating diffuses (termed "leaching") into the solder joint. Solder grain size is another parameter that can affect life. As the grain size becomes smaller, plastic strains decrease due to dislocation pile-ups at grain boundaries and anelastic strains decrease due to reduced grain boundary sliding and intergranular cracking. As a result, fatigue life improves with grain refinement. Surface finish, notches, and hostile chemical environments can also limit fatigue life because of local stress concentrations and stress-assisted corrosion.

8.3.3 Thermal Cycling Tests

Various testing methods are used to generate fatigue failure data for PCBs. Temperature cycling in environmental chambers produces first-order reliability results quickly and with

little effort. It should be clearly understood, however, that this method does not simulate the actual temperature distributions that components and interconnections in a PCB see in service. Some of the better-known specifications for temperature cycling and thermal shock tests are the military specifications MIL-STD-883, Methods 1010 and 1011. These methods define a thermal cycle or shock as the stress a device undergoes when it is temperature cycled in an environmental chamber or when it is alternately switched from a bath of hot liquid to a bath of cold liquid. These methods specify the temperature extremes for cycling and shock tests under several conditions: (1) condition A is between +100 and 0°C; (2) condition B, which was the most commonly adopted test until recently, is between +125 and -55°C; (3) condition C, which is currently most common, is between +65 and 100°C; and (4) condition F is between +22 and -195°C. For example, during screening tests, hybrid components are typically subjected to 10 temperature cycles (Method 1010) under condition C or 15 shock cycles (Method 1011) under condition A. On the other hand, qualification tests under MIL-STD-1772 require 100 temperature cycles (Method 1010) under condition C and 15 thermal shocks (Method 1011) under condition A.

These test conditions can be used in simple analytical models to predict fatigue failure. As an example, consider the solder joint of a leadless chip carrier. Because of the differences in expansion between the chip carrier and the substrate in a PCB, the solder joint is subjected to a cyclic strain. A first approximation of the cyclic strain can be obtained by considering only the deformations in the plane of the PCB. Figure 8.26a is a schematic of the chip carrier mounted on the PCB substrate with a solder joint of rectangular cross section and height h .

The shear strain in the deformed solder joint due to the differential expansion ΔL , as shown in Figure 8.26b, is

$$\gamma = \frac{\Delta L}{2h} \quad (8.59)$$

The factor of 2 in the denominator accounts for the fact that the expansion mismatch is shared equally by the solder joint at each end. Assuming that the chip carrier and the PCB are much stiffer than the solder joint and ignoring bending deformations (i.e., considering only in-plane displacements),

$$\Delta L = L[(\alpha_s - \alpha_{cc})T_{\max} - (\alpha_s - \alpha_{cc})T_{\min}] = L \Delta \alpha \Delta T \quad (8.60)$$

where $\Delta \alpha (= \alpha_s - \alpha_{cc})$ is the difference between the thermal coefficients of the PCB substrate and the chip carrier and $\Delta T (= T_{\max} - T_{\min})$ is the difference between the maximum and minimum temperatures in the cycle. Note that there is an underlying assumption that the dwell times at $T_{\max}$ and $T_{\min}$ are sufficient for complete stress relaxation to occur in the solder joint. Thus

$$\gamma = \frac{L \Delta \alpha \Delta T}{2h} \quad (8.61)$$

Assuming that the dwell times at $T_{\min}$ and at $T_{\max}$ are sufficient to allow complete stress relaxation in the solder during each cycle, the mean stress effects can be ignored (experimental evidence suggests that mean strains do not affect fatigue life). Further, ignoring elastic strains in low-cycle fatigue and assuming the anelastic and plastic strains to be equivalent in the context of fatigue damage (i.e., ignoring the frequency modifications to the Coffin-Manson relationship) as a first-order approximation,

Thermom

$$\frac{\Delta \gamma_p}{2}$$

Rearrang

$$N_f =$$

$$T_{cc} -$$

$$T_{s,u} -$$

$$T_s -$$

$$T_{s,l} -$$

(a)

$$T_{cc} -$$

$$T_s -$$

(b)

Figure 8
expansion
joint of r
(out-of-p

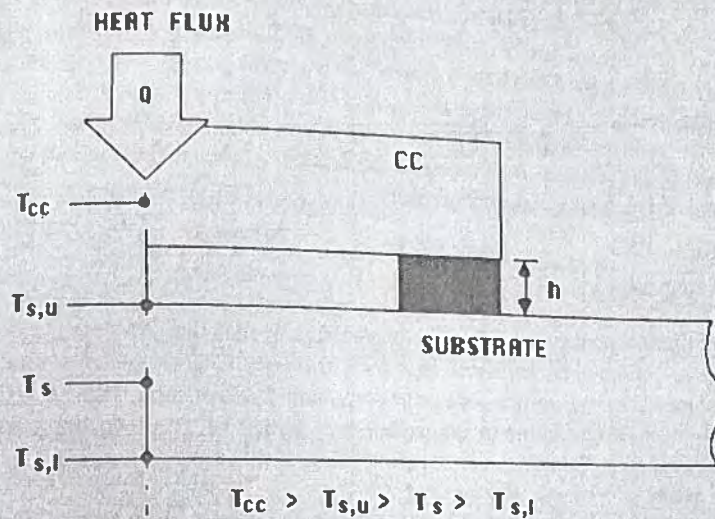
$$\frac{\Delta\gamma_p}{2} = \gamma_r(2N_r)^c$$

(8.62)

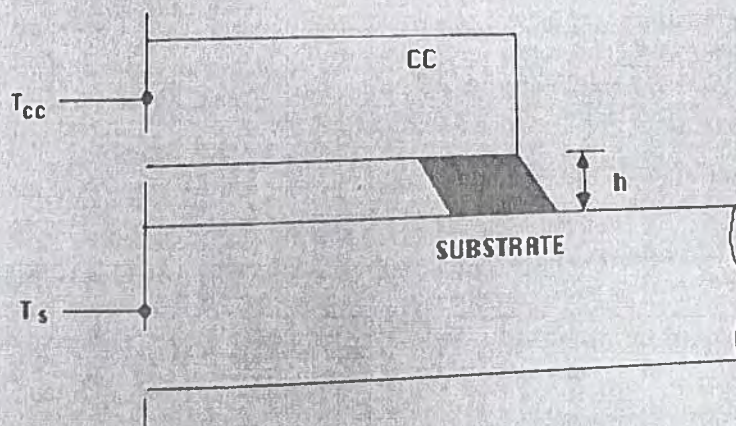
Rearranging Eq. (8.62) and substituting Eq. (8.59),

$$N_r = \frac{1}{2} \left(\frac{\Delta\gamma_p}{2\gamma_r} \right)^{1/c} = \frac{1}{2} \left(\frac{L \Delta\alpha \Delta T}{4h\gamma_r} \right)^{1/c}$$

(8.63)



(a)



(b)

Figure 8.26 Shear strain in a deformed solder joint due to differential expansion ΔL . (a) Schematic of a chip carrier mounted on a PCB with a solder joint of rectangular cross section and height h . (b) Pure shear deformation (out-of-plane deformations are ignored), $\alpha_s \Delta T_s > \alpha_{cc} \Delta T_{cc}$.