

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CAMBRIDGE INDUSTRIES USA INC.,
Petitioner

v.

APPLIED OPTOELECTRONICS, INC.,
Patent Owner

Case No. IPR2025-00435
U.S. Patent No. 10,042,116

**DECLARATION OF DR. ANDREW G. KIRK IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 10,042,116**

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TABLE OF EXHIBITS

Exhibit	Short Name	Description
Ex. 1001	'116 Patent	U.S. Patent No. 10,042,116
Ex. 1002	'116 File History	File History of U.S. Patent No. U.S. Patent No. 10,042,116
Ex. 1003	Kirk Declaration	Declaration of Dr. Andrew G. Kirk
Ex. 1004	Kirk CV	<i>Curriculum Vitae</i> of Dr. Kirk
Ex. 1005	Soldano	U.S. Patent No. 9,768,901
Ex. 1006	Lurie	U.S. Patent No. 5,351,327
Ex. 1007	Tomita	U.S. Patent No. 4,978,193
Ex. 1008	Shen	U.S. Patent Pub. No. US 2016/0349451
Ex. 1009	Shen provisional	U.S. prov. patent appln SN 62/166,015
Ex. 1010	Kanazawa	Japanese Patent Pub. JP 2012-034314A
Ex. 1011	—	Kanazawa English translation
Ex. 1012	Sasaki	Japanese Patent Pub. JP 2003-215371A
Ex. 1013	—	Sasaki English translation
Ex. 1014	Claim Terms	Joint Claim Construction And Pre-Hearing Statement in <i>Applied Optoelectronics, Inc. v. Cambridge Industries USA, Inc.</i> , No. 3:24-cv-01010-JD (N.D. Cal.)
Ex. 1015	Scheduling Order	Scheduling Order dated August 7, 2024, in <i>Applied Optoelectronics, Inc. v. Cambridge Industries USA, Inc.</i> , No. 3:24-cv-01010-JD (N.D. Cal.)
Ex. 1016	Excerpt from Infringement Claim Charts	Excerpt from Patent Owner's L.R. 3-1 & 3-2 Disclosures, June 6, 2024, in <i>Applied Optoelectronics, Inc. v. Cambridge Industries USA, Inc.</i> , No. 3:24-cv-01010-JD (N.D. Cal.)

DECLARATION OF DR. ANDREW G. KIRK

I, Andrew G. Kirk, do hereby declare and say as follows:

I. Introduction

1. My name is Dr. Andrew G. Kirk, and I have been retained as a technical expert by counsel for Petitioner Cambridge Industries USA Inc. (“CIG USA”) to address certain issues regarding U.S. Patent No. 10,042,116 (“the ’116 Patent”).

2. I have personal knowledge of the facts contained in this Declaration, am of legal age, and am otherwise competent to testify.

3. Unless otherwise stated, the matters contained in this Declaration are of my own personal knowledge and, if called as a witness, I could and would testify completely and truthfully with regard to the matters set forth herein.

4. My opinions are based on my years of education, research, and experience, as well as my study of the relevant materials. A list of materials I considered is included at the beginning of this Declaration.

5. I reserve all available rights to supplement this Declaration if further information becomes available, or if I am asked to consider additional information. This Declaration represents only those opinions I have formed to date.

6. Further, I reserve all available rights to consider and comment on any additional expert statements or testimony of Patent Owner’s expert(s) in this matter.

7. I am being compensated at my usual consulting rate of \$400 per hour

IPR2025-00435, Exhibit 1003

for my time spent working on issues in this matter. My compensation does not depend on the outcome of this matter or the opinions I express.

II. Qualifications

8. A true and correct copy of my curriculum vitae is submitted herewith as Ex. 1004.

9. I have over 30 years of experience in communications and signal processing. I am currently a Professor in the Department of Electrical & Computer Engineering, Photonics Systems Group, at McGill University in Montreal, Canada. I graduated with Honors from University of Bristol, United Kingdom in 1989 with an B.Sc. in Physics and went on to receive a Ph.D. from King's College, London, in 1992 in Physics. The title of my thesis was "Diffractive optical elements within parallel optical systems" I conducted Post-Doctoral research in reconfigurable optical interconnects for parallel processing applications at the University of Tokyo as a JGF Research Fellow and in design, analysis, and packaging of parallel optical interconnects in an HCM Fellowship at Vrije Universiteit Belgium, Brussels.

10. In 1996, I joined McGill University as an Assistant Professor in the Department of Electrical and Computer Engineering, and in 2002, I was promoted to Associate Professor.

11. In 2006, I became Associate Dean for Research and Graduate Education, Faculty of Engineering, and in 2011, was promoted to Professor in the

Department of Electrical and Computer Engineering. My teaching responsibilities include courses in fiber-optic communications, free-space optical systems, optoelectronics, quantum optics, thermodynamics and professional engineering.

12. I was awarded a William Dawson Scholar research chair by McGill in 2000, which was renewed in 2005. In 2011 I was appointed as a James McGill Professor (term ended in 2018). I was appointed as Department Chair in 2011 and again from 2013 to 2018, and served as Dean of the Faculty of Engineering (in an Interim position from 2011-2013). I have obtained academic appointments as a Visiting Researcher at the University of Glasgow (UK), University of Sydney (Australia), Universidad Politécnica de Valencia (Spain) and Lady Davis Institute of the Jewish General Hospital, Montreal.

13. My responsibilities as a member of the Photonics Systems Group included leading a \$800,000 research program involving approximately 5 faculty members and supervising 6 doctoral and post-doctoral students.

14. In addition to the activities, education, and professional experience listed above, I have been involved in several research projects that contribute to my expertise relating to fiber-optic communications.

15. I have received numerous awards such as James McGill Professor, the William and Reah Seath Award for Engineering Innovation and the NSERC Synergy Award (as part of a team). I am a Member of the SYTACom Research

Center. I have contributed to advances in the design of integrated optical wavelength demultiplexers and switches, to microelectromechanical optical systems, optical sensor devices and signal processing for optical sensors.

16. My research interests include passive and active components for fiber-optic communications systems, optical packaging techniques and optical sensor devices. I have extensive experience researching and teaching about optics and photonics, optical signal processing and packaging. I also have experience with optical transceiver modules, including pluggable-type modules.

17. To date, I have published book chapters on optical Interconnects and reviews in the area of fiber optic communications systems. In addition, I have published more than 150 papers in conference proceedings and more than 100 peer-reviewed journal papers. I am also a named inventor on three patents relating to fiber-optic components.

18. I have previously consulted for several major companies in the field of optical fiber communications technology, including Nortel, JDSU, Corning and Accelight Networks.

19. Through my work, I have earned the respect of the optical communication and electrical engineering community more broadly. I served as an Elected Member of the Board of Governors of the IEEE Photonics Society and as Chair of the IEEE Photonics Society Nanotechnology Committee. I have served as

Board Member for several technical organizations, including PROMPT-Quebec, CQRDA and CRIAQ.

III. Scope of the Engagement

20. I have been retained by Eversheds Sutherland (US) LLP on behalf of CIG USA to provide various analyses and opinions. Among other tasks, I have been asked to address the technology claimed in the '116 Patent and to evaluate whether certain claims of the '116 Patent would have been regarded as lacking novelty or would have been obvious to a person of ordinary skill in the art.

21. All of the opinions I express in this Declaration have been made from the standpoint of a person of ordinary skill in the relevant art at the time of the invention of the '116 Patent, which I am informed is, for purposes of the '116 Patent, is April 25, 2016.

22. I have been asked to identify the level of skill in the art pertinent to the '116 Patent. It is my opinion that a person of ordinary skill in the art ("POSITA") pertinent to the '116 Patent would have had at least a bachelor's degree in electrical engineering, computer engineering, networking, or similar discipline and had approximately two years of experience with optical data communications and networks or a similar field of work. Additional graduate education might substitute for experience. A person with a different degree but with additional relevant experience could still qualify if the additional experience compensates for the

different educational background. Such a POSITA would have had knowledge of design considerations known in the optical industry and would have been familiar with then-existing products and solutions and would have understood how to search available literature for relevant publications.

23. A POSITA in April 2016 would have been familiar with MSA optical modules, including SFP and XFP formats. The '116 Patent concerns itself with communications and networking in optical systems, particularly networking protocols such as Ethernet, and the technologies that enable it, as well as the miniaturization of those technologies into what are commonly known as Small Form-Factor Pluggable (SFP) module. Thus, a POSITA in April 2016 would have been familiar with both communications networking technology as well as optoelectronic devices.

24. I consider myself a person of ordinary skill in the art as of at least the earliest claimed priority date (April 25, 2016), and for many years earlier.

25. My opinions regarding the level of ordinary skill in the art are based on, among other things, my more than 30 years of experience in optical networks and components therefor, my understanding of the basic qualifications that would be relevant to an engineer or scientist tasked with investigating optical networks and components therefor, my knowledge and experience with the capabilities of such systems by 2016, and my familiarity with the backgrounds of colleagues, both past

and present. Although my qualifications and experience exceed those of the hypothetical person having ordinary skill in the art defined above, my analysis and opinions regarding the '116 Patent have been based on the perspective of a person of ordinary skill in the art as of around April 2016. I am able to take on that perspective based on my experience as I have worked with individuals who had this level of experience in the 2016-time frame and am familiar with their level of knowledge.

26. My opinions are also based on the information I have reviewed as of the date of this Declaration. In connection with my analysis, I have reviewed the exhibits listed in the above list of exhibits, as well as each of the items referenced herein. I attest that the foregoing exhibits are true and accurate copies that I downloaded. My opinions directed to the invalidity of the challenged claims are based, at least in part, on the following patents and publications:

- **“Soldano”** Ex. 1005, which is U.S. Patent No. 9,768,901, filed on February 12, 2015, and issued on September 19, 2017, claiming priority to U.S. Provisional Patent Application 62/082,529, filed November 20, 2014.
- **“Lurie”** Ex. 1006, which is U.S. Patent No. 5,351,327, filed on June 25, 1993, and issued on September 27, 1994.
- **“Tomita”** Ex. 1007, which is U.S. Patent No. 4,978,193, filed on August 24, 1989, and issued on December 18, 1990.

- **“Shen”** Ex. 1008, which is U.S. Patent Application Publication No. US 2016/0349451, filed on May 24, 2016, and published on December 1, 2016, which claims the priority to Shen U.S. Provisional Patent Application No. 62/166,015, Ex. 1009, filed May 25, 2015.

- **“Kanazawa”** Ex. 1010, which is Japanese Patent Publication JP 2012-034314A, filed August 3, 2010, and published on February 16, 2012, and its English language translation, Ex. 1011.

- **“Sasaki”** Ex. 1012, which is Japanese Patent Publication JP 2003-215371A, filed January 25, 2002, and published on August 30, 2003, and its English language translation, Ex. 1013.

IV. Legal Standards

27. For purposes of this Declaration, counsel for CIG USA have instructed me to make the following assumptions:

28. Claims are construed from the perspective of a POSITA as of the effective filing date of the patent application. POSITAs are deemed to read the claims in the context of the entire patent, including the specification and prosecution history. In other words, the terms are not considered in a vacuum.

29. It is my understanding that information that satisfies one of the categories of prior art set forth in 35 U.S.C. § 102 may be used in an invalidity analysis under §§ 102 or 103. If information is not properly classified as prior art

under one of the subsections of § 102 of the Patent Act, then it may not form the basis of an anticipation or obviousness determination. It is also my understanding that, for *inter partes* review, applicable prior art is limited to patents and printed publications.

30. I am informed and understand that a patent claim is invalid under 35 U.S.C. § 102 if a single item of prior art discloses all of the limitations set forth in a patent claim, arranged as set forth in the claim. I understand that a POSITA may take into account technical knowledge that would have been well known to those of skill in the relevant art when considering the disclosures of a patent and that applying such knowledge to the disclosure of a reference still qualifies as anticipation. I understand from counsel that this is sometimes referred to as “single reference obviousness,” but in this case the motivation to combine comes from the single reference itself when properly interpreted by those of skill in the art.

31. I am also informed that a patent claim is invalid under 35 U.S.C. § 103 if the differences between the claimed invention and the prior art are such that the subject matter as a whole would have been obvious at the time of the invention to a POSITA to which the subject matter pertains. Obviousness, I am informed, is determined based on the scope and content of the prior art, the differences between the prior art and the claim, the level of ordinary skill in the art, and secondary indications of non-obviousness to the extent they exist.

32. I understand that whether there are any relevant differences between the prior art and the claimed invention is to be analyzed from the view of a POSITA at the time of the invention. A POSITA is a hypothetical person who is presumed to be aware of all of the relevant art at the time of the invention. The POSITA is not an automaton and may be able to fit together the teachings of multiple patents (or other printed publications) by employing ordinary creativity and the common sense that familiar items may have obvious uses in another context or beyond their primary purposes.

33. In analyzing the relevance of the differences between the claimed invention and the prior art, I understand that I must consider the impact, if any, of such differences on the obviousness or non-obviousness of the invention as a whole, not merely some portion of it. The POSITA faced with a problem is able to apply his or her experience and ability to solve the problem and also look to any available prior art to help solve the problem.

34. I understand that an invention would have been obvious if a POSITA, facing the wide range of needs created by developments in the field, would have seen an obvious benefit to the solutions tried by the patent applicant. When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, it would have been obvious to a POSITA to try the known options. If a technique has been used to improve one device, and a

POSITA would recognize that it would improve similar devices in the same way, using the technique would have been obvious.

35. I understand that I do not need to look for precise teachings in the prior art directed to the subject matter of the claimed invention. I understand that I may consider the inferences and creative steps that a POSITA would have employed in reviewing the prior art at the time of the invention. For example, if the claimed invention combines elements that were known in the prior art and if the combination yields results that were predictable to a POSITA at the time of the invention, then this would make it more likely that the claim was obvious. On the other hand, if the combination of known elements yields unexpected or unpredictable results, or if the prior art teaches away from combining the known elements, then this would make it more likely that the claim that successfully combined those elements was not obvious. I understand that hindsight must not be used when comparing the prior art to the invention during an obviousness analysis.

36. I understand that obviousness may be shown by demonstrating that it would have been obvious to modify what is taught in a single piece of prior art to create the patented invention. Obviousness may also be shown by demonstrating that it would have been obvious to combine the teachings of more than one item of prior art. I understand that a claimed invention may be obvious if some teaching, suggestion, or motivation exists that would have led a POSITA to combine the

invalidating references. I also understand that this suggestion or motivation may come from sources such as explicit statements in the prior art, or from the knowledge of a POSITA. Alternatively, any need or problem known in the field at the time and addressed by the patent may provide a reason for combining elements of the prior art. I also understand that when there is a design need or market pressure, and there are a finite number of predictable solutions, persons of ordinary skill may be motivated to apply both their skill and common sense in trying to combine the known options in order to solve the problem.

37. I understand that absent evidence of an invention date prior to the filing date of a patent, the invention date of the patent is presumed to be its filing date. A prior invention requires a complete conception of the invention and a reduction to practice of that invention. The patent owner has the burden of establishing by clear and convincing evidence a date of conception earlier than the filing date of the patent.

V. Technical Background

38. In this technical background, I describe the pertinent technology as it existed as of April 2016, the earliest alleged priority date of the '116 Patent.

39. The '116 Patent generally relates to an optical transceiver module in which an optical demultiplexer, in the form of an arrayed waveguide grating ("AWG"), is coupled to photodetectors by an angled end portion of the AWG. Such

arrangements, and the use thereof, were well-known to POSITAs of photonics module and planar light circuit (“PLC”) design at the time the application that matured into the ’116 Patent was filed.

40. The ’116 Patent describes and claims an AWG chip (and photonics module containing same) having a first end that couples to an optical coupling receptable to receive an optical signal comprised of multiple channel wavelengths, a substrate, a PLC disposed on the substrate, a plurality of output waveguides coupled to the PLC to each receive a demultiplexed channel wavelength from the PLC, and a tapered region at a second end of the AWG chip to reflect light from the plurality of output waveguides towards an output interface region of the AWG chip. Ex. 1001, 3:66-4:25.

41. Claims 1-11 require that the output interface region emit light received from the AWG chip on the same side as the substrate on which the AWG was built, without passing the received light through the substrate. *Id.*, 12:23-13:20. Claims 12-19 are directed to an optical transceiver including an AWG having a tapered end region at one end, and an angled surface at the other that joins to the optical coupling receptable, thereby reducing back reflection along the input optical fiber. *Id.*, 3:58-65, 13:21-14:42.

42. As I will describe, all these ideas were well known to a POSITA at the time of the alleged invention.

a. Pluggable Optical Transceiver Modules

43. The optical-to-electrical interface is where electrical and fiber cables are connected to one another via an optical transceiver module. To allow the electrical and fiber cables to communicate with one another, the optical transceiver module converts between optical and electrical signals.

44. For example, a transceiver module includes an optical transmitter and optical receiver. The transmitter receives electrical signals and converts them to optical signals. The receiver receives optical signals and converts them to electrical signals. The transmitter and receiver, which together form the transceiver, thus send signals back and forth across the electrical-to-optical interface, allowing communication between the electrical components and optical fibers.

45. Traditionally, optical transceiver modules were bulky and mounted in a relatively fixed configuration, such as mounted on a circuit card located in a computer, peripheral device, or on a shelf in an equipment rack. But as optical networks garnered increased popularity, the market requirement to grow the capacity of network equipment required that the density of the network equipment improve. This requirement manifested itself in a need to improve the density of optical interfaces at a faceplate, which led to the creation of a new type of transceiver: a Small Form Factor (SFF) device.

46. The availability of SFF devices enabled high port densities in optical

transmission systems. However, while solving the density problem, the SFF package had to be soldered down to the board, making replacement and repair a difficult process. In order to resolve the drawbacks of the SFF device, it was desirable to produce a smaller hot-pluggable optical transceiver that was easily removable.

47. Thus, in the late 1990s and early 2000s, photonics module developers began to develop and design transceiver modules that could be inserted into and removed from a live circuit pack without disrupting service or impacting the performance of any other ports already in service, leading to the creation of Small Form-factor Pluggable (SFP) transceivers. The SFP modules were similar in size to the SFF devices, but were hot-pluggable, offering full flexibility and permitting a mix of various transceiver types on a single circuit pack and easing replacement in the case of transceiver failure.

48. In order to facilitate simple pluggable insertion and removal from the host device, these transceiver modules were constructed with a protective cage mounted at the front of the host device and an electrical interface realized through an electrical connector. The electrical interface provides all necessary input and output signals from the transceiver module to the host device.

49. In an effort to standardize the industry, system vendors supported Multi-Source Agreements (“MSA”), agreements between component suppliers to define and specify all the physical and electrical requirements for specific pluggable

form factors. With MSAs in place, system vendors could concentrate on system architecture and not optical research and development. Several MSA optical module types were known by 2003, including but not limited to:

- Small form-factor pluggable (SFP) (*see* INF-8074i Specification for SFP (Small Formfactor Pluggable) Transceiver, Rev. 1.0, May 12, 2001); and
- 10G small form factor pluggable (XFP) (initial publication in March 2002; 10 Gigabit Small Factor Pluggable Module, XFP Revision 4.5).

50. A POSITA in 2016 would have understood that the form factor used for the transceiver depends on the type of data, speed, and distance between communication devices.

b. Arrayed Waveguide Grating Devices (AWG)

51. An AWG employs optics that are capable of separating (or combining) light waves having different channel wavelengths. When employed as an optical de-multiplexer, an AWG can separate an inbound multiwavelength optical signal carried by a single optical fiber into a plurality of channel wavelengths for individual detection and processing. When employed as an optical multiplexer, an AWG can combine multiple channel wavelengths output by a plurality of lasers into a single multiwavelength optical signal for outbound transmission on a single optical fiber. Accordingly, AWGs may be used for both multiplexing and de-multiplexing optical signals. Ex. 1001, 2:15-27.

52. AWGs may be fabricated as a silica-based device using planar lightwave circuit techniques. In this regard, doped and undoped layers of silica are deposited on a substrate, such as silicon. *Id.*, 2:28-34. An AWG may be used as a demultiplexer in a receiving optical subassembly (“ROSA”), wherein the grating portions of the AWG separate out the individual channel wavelengths and guide the wavelengths to corresponding photodetectors for conversion to electrical signals.

VI. The ’116 Patent

53. The ’116 Patent is generally directed towards communication over an optical network using pluggable optical transceiver modules, and in particular the optoelectrical interface. Specifically, the ’116 Patent discloses a transceiver module for use in an optical network having a ROSA and a transmitting optical subassembly (“TOSA”). The ROSA employs an AWG to demultiplex an incoming multiwavelength optical signal received on a single input optical fiber to convert that signal to separate wavelength optical signals and then convert those separate optical signals to electrical signals for processing. The TOSA receives processed electrical signals and employs a laser assembly to generate separate corresponding optical signals and an AWG to multiplex those optical signals into a multiwavelength optical signal for transmission over a single optical output fiber. Ex. 1001, Abstract, FIG. 3 (reproduced below).

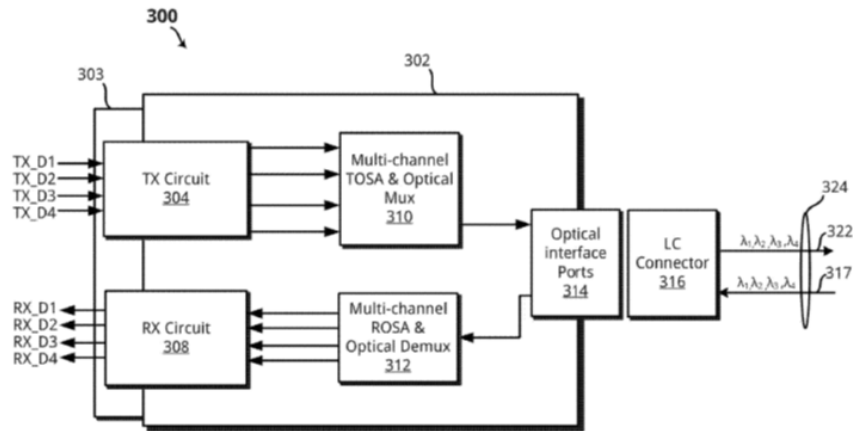


FIG. 3

54. The '116 Patent discloses an AWG chip 503, illustrated in FIG. 5A (below), in which the AWG is formed as a planar light circuit ("PLC") in which cladding and core are deposited on substrate 502. The alleged invention, recited in Claims 1-11 of the '116 Patent, is that optical signals transmitted through the AWG are reflected by polished angle surface 520 and exit from the AWG through direct coupling interface 517 on the same side as substrate 502. *See* Ex. 1001, 3:33-50, 3:66-4:28, 7:60-66, 9:21-61.

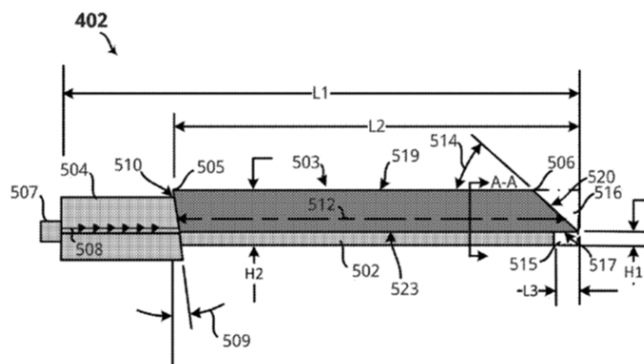


FIG. 5A

55. The '116 Patent further discloses an optical transceiver having a

ROSA and a TOSA including an AWG, wherein an input coupling region 504 of the AWG includes mounting surface 510 having an angle 509, preferably about 8 degrees, to reduce back reflection when launching light into AWG chip 503. This aspect of the '116 Patent is set forth in Claims 12-19. As I describe below, it was known in the art of optical communications—decades before the filing of the application that matured as the '116 patent—to provide angled junctions between optical components to reduce back reflection.

56. I have been asked to evaluate Claims 1-19 of the '116 Patent. I have reproduced these challenged claims below:

Claim	Recitation
[1a]	An arrayed waveguide grating (AWG) chip comprising:
[1b]	a first end for coupling to an optical coupling receptacle to receive an optical signal comprising a plurality of channel wavelengths;
[1c]	a substrate;
[1d]	a planar lightwave circuit (PLC) disposed on the substrate, the PLC coupled to the first end and configured to de-multiplex each channel wavelength of the plurality of channel wavelengths;
[1e]	a plurality of output waveguides coupled to the PLC, each of the output waveguides configured to receive light corresponding to an associated de-multiplexed channel wavelength launched from the PLC and provide the light along a first light path that extends towards a second end of the AWG chip; and
[1f]	a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an exposed output interface region of the AWG chip, wherein the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate.
2	The AWG chip of claim 1, wherein the exposed output interface region

Claim	Recitation
	is configured to pass the reflected light received via the plurality of output waveguides out of the AWG chip along a second light path that is substantially orthogonal to the first light path.
3	The AWG chip of claim 1, wherein the AWG chip defines a plurality of sidewalls extending longitudinally from the first end to the second end, and wherein the tapered region of the second end defines an angled surface that extends from a first sidewall of the plurality of sidewalls to a second sidewall of the plurality of sidewalls.
4	The AWG chip of claim 3, wherein the angled surface has an interior angle of about 41 to 45 degrees relative to the exposed output interface region.
5	The AWG chip of claim 3, wherein each of the output waveguides comprise a core material, and wherein a cladding material is disposed on the core material, the core material defining at least a portion of the plurality of sidewalls of the AWG chip.
6	The AWG chip of claim 5, wherein the core material of each of the plurality of output waveguides has a first index of refraction, and a medium external to and adjacent the tapered region has a second index of refraction, the first index of refraction being greater than the second index of refraction.
7	The AWG chip of claim 6, wherein the external medium comprises a material having an index of refraction of about 1.0.
8	The AWG chip of claim 5, wherein the core material of each of the plurality of output waveguides provide a portion of the angled surface, and wherein the angled surface is configured to reflect incident light based on at least an interior angle of the angled surface.
9	The AWG chip of claim 5, wherein the core material comprises doped silica (SiO ₂) having an index of refraction of about 1.45 to 1.50.
10	The AWG chip of claim 1, wherein the AWG chip is configured as a 1×N demultiplexer device whereby a single optical input signal is demultiplexed into N different channel wavelengths.
11	The AWG chip of claim 1, wherein the AWG chip is implemented in an AWG device package.
[12a]	An optical transceiver module comprising
[12b]	a transceiver housing;

Claim	Recitation
[12c]	a multi-channel receiver optical sub-assembly (ROSA) located in the transceiver housing and including an arrayed waveguide grating (AWG) chip, the AWG chip comprising:
[12d]	a first end for coupling to an optical coupling receptacle to receive an optical signal comprising a plurality of channel wavelengths, wherein the first end for coupling to the optical coupling receptacle includes an angled surface to reduce back reflections of an optical signal launched into the AWG chip;
[12e]	a planar lightwave circuit (PLC) coupled to the first end configured to de-multiplex each channel wavelength of the plurality of channel wavelengths;
[12f]	a plurality of output waveguides coupled to the PLC, each of the output waveguides configured to receive light corresponding to an associated de-multiplexed channel wavelength launched from the PLC and provide the light along a first light path that extends towards a second end of the AWG chip; and
[12g]	a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an output interface region of the AWG chip;
[12h]	an array of detector devices disposed adjacent to the output interface region of the AWG chip; and
[12i]	a multi-channel transmitter optical assembly (TOSA) including at least one laser package located in the transceiver housing for transmitting optical signals at different channel wavelengths.
13	The optical transceiver module of claim 12, wherein the output interface region of the AWG chip is an exposed region adjacent an air gap, and wherein the air gap separates the output interface region of the AWG chip and the array of detector devices.
14	The optical transceiver module of claim 12, wherein the output interface region of the AWG chip is separated from the array of detector devices by about 50 microns.
15	The optical transceiver module of claim 12, wherein the AWG chip defines a plurality of sidewalls extending longitudinally from the first end to the second end, and wherein the tapered region of the second end defines an angled surface that extends from a first sidewall of the plurality of sidewalls to a second sidewall of the plurality of sidewalls.

Claim	Recitation
16	The optical transceiver module of claim 15, wherein the angled surface has an interior angle of about 41 to 45 degrees relative to the output interface region.
17	The optical transceiver module of claim 15, wherein each of the output waveguides comprise a core material, and wherein a cladding material is disposed on the core material, the core material defining at least a portion of the plurality of sidewalls of the AWG chip.
18	The optical transceiver module of claim 17, wherein the core material of each of the plurality of output waveguides provide a portion of the angled surface, and wherein the angled surface is configured to reflect incident light based on at least an interior angle of the angled surface relative to the output interface of the AWG chip.
19	The optical transceiver of claim 12, wherein the transceiver is a Small Form-factor Pluggable (SFP) transceiver module and the ROSA is configured to receive at least four different channel wavelengths at transmission rates of at least about 25 Gbps per channel.

VII. Prosecution History

57. Patent Owner filed Application No. 15/137,823 (the “’823 Application”) on April 25, 2016, which matured as the ’116 Patent, on August 7, 2018. Ex. 1001, cover.

58. An Office action mailed June 7, 2017, imposed a restriction between Claims 1-19, drawn to an AWG chip, and Claim 20, drawn to a method of forming an AWG chip. *Id.*, pp. 110-114. A Response was filed August 7, 2017, electing Claims 1-19 for examination and withdrawing Claim 20. *Id.*, p. 104.

59. On August 21, 2017, a non-final Office action was mailed, rejecting Claims 1-11 as anticipated by Bai (U.S. Patent No. 7,532,783). *Id.*, pp. 82-85. Claims 12-19 were rejected as obvious over Dallesasse (U.S. Patent No. 7,941,053)

IPR2025-00435, Exhibit 1003

in view of Bai or Welch et al. (U.S. 7,058,263). *Id.*, pp. 85-90. An Amendment and Response was filed on January 29, 2018, in which independent Claim 1 was amended to recite “a substrate,” that the planar lightwave circuit was “disposed on the substrate” and that “the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate.” *Id.*, p. 43. Claim 12 was amended to recite that the first end “includes an angled surface to reduce back reflections of an optical signal launched into the AWG chip.” *Id.*, p. 45.

60. A Notice of Allowance and Notice of Allowability were mailed June 4, 2018. *Id.*, pp. 7-13. The Notice of Allowability recites that Claims 1-11 “are allowable because Bai (US Patent No. 7,532,783) fails to teach a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an exposed output interface region of the AWG chip, wherein the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate. *Id.*, p. 12.

61. The Notice of Allowability also recites that Claims 12-19 “are allowable because Dallesasse (US Patent No. 7,941,053) and Bai (US Patent No. 7,532,783) fails [sic] to teach a first end for coupling to an optical coupling receptacle to receive an optical signal comprising a plurality of channel

wavelengths, wherein the first end for coupling to the optical coupling receptacle includes an angled surface to reduce back reflections of an optical signal launched into the AWG chip.” *Id.*, pp. 12-13.

62. The Issue Fee was paid on July 5, 2018. *Id.*, p. 2. The ’116 patent issued on August 7, 2018. *Id.*, p. 1.

VIII. Claim Construction

63. I am informed by counsel for CIG USA that in an *Inter Partes Review*, claims should be construed “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. §282(b).” 37 C.F.R. §42.100(b) (Nov. 13, 2018). And unless otherwise specified in the patent under review, the terms should receive their respective plain and ordinary meaning as understood by a person of ordinary skill in the art under *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005).

64. In deciding this Petition, in view of the arguments made to the Patent Examiner to secure allowance of Claims 1-11, it is my opinion that the Board will need to construe the terms “substrate” and “disposed on the substrate” as used in those claims. As expressly described in the ’116 patent, the claimed AWG is formed by sequentially depositing cladding and core layers on a silicon or other silicon-based substrate. *See, e.g.*, Ex. 1001, 502 in FIG. 5A, 3:35-38 (“the AWG device is formed on a substrate such as a silicon wafer or any other suitable

substrate and may include depositing sequential layers of cladding and core material thereon”), 8:31-43.

65. As further described in the ’116 Patent, a portion of the substrate may be removed by cutting or etching to expose output interface region 517. *Id.*, FIG. 5A, 9:46-50. The patent explains that this process step is employed so that the “output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate” as recited in Claim 1. As discussed, this limitation that was added to Claim 1 to distinguish over the cited prior art. Ex. 1002, pp. 43, 48-49.

66. In my view, the proper construction of the term “substrate” of Claim 1 is “a silicon or silicon-based layer on which the cladding and core layers are deposited to form the PLC.” Ex. 1001, 3:35-38, 8:31-43. With the foregoing construction of “substrate,” the term “disposed on” in the second element of Claim 1, which requires a “planar lightwave circuit (PLC) disposed on the substrate,” which in my opinion should be construed to mean that the PLC is deposited on the substrate (e.g., as during manufacture of the AWG chip as described in the ’116 Patent specification). *Id.* Further, limiting the substrate to the material upon which the PLC is formed gives meaning to the final clause of Claim 1, “without passing the received light through the substrate”—the implementation of which in the patent is obtained by etching or otherwise removing a portion of the substrate underlying

the angled end face. *Id.*, FIG. 5A, 9:46-49 (“Formation of the AWG chip 503 can include removing a portion of the substrate generally indicated at 515 to expose the output interface region 517”).

67. Notwithstanding the foregoing, I am also informed that a claim term should be construed the same way for determining invalidity as for infringement. I understand that in pending litigation between the Patent Owner and CIG USA, the Patent Owner construes the term “substrate” more broadly than it did during prosecution of the ’116 Patent, arguing for a “plain and ordinary meaning.” Ex. 1014, p. 4. Specifically, in the pending litigation, the Patent Owner has urged the District Court to adopt a construction of “substrate” as “a supporting structure for an AWG device.” *Id.* In its infringement claim charts, Ex. 1016, the Patent Owner variously has identified the substrate as: (1) slab of grey-colored material underneath the PLC (Exhibit 3); (2) the printed circuit board (“PCB”) to which the AWG is affixed (Exhibit 4); and (3) a glue layer used to affix the PLC to the PCB (Exhibit 5). *See* Ex. 1016, pp. 3, 4, 5, 10-11, 12-13, 14-15.

68. Thus, as applied in Patent Owner’s infringement claim charts, despite amending the claims to identify the location of the “substrate” to distinguish over the prior art, Patent Owner attributes to the term “substrate” a plain and ordinary meaning of “a supporting structure for an AWG device.” Ex. 1014, p. 4. Consistent with the Patent Owner’s construction for “substrate,” for purposes of my invalidity

analyses, I adopt herein the construction of “substrate” urged by the Patent Owner in its infringement contentions.

IX. Prior Art References

a. Soldano Overview

69. U.S. Patent No. 9,768,901 (“Soldano”), Ex. 1005, titled “Planar Lightwave Circuit Active Connector,” was filed on February 12, 2015, and issued on September 19, 2017. Ex. 1005, cover. I understand from counsel for CIG USA that Soldano qualifies as prior art under 35 U.S.C. § 102(a). Soldano was cited by the Patent Owner in an Information Disclosure Statement (“IDS”) filed simultaneously with Patent Owner’s last Amendment filed during prosecution of the ’116 Patent. Ex. 1002, p. 52. Soldano was not applied in a prior art rejection by the Patent Examiner during prosecution of the ’116 Patent. *Id.*

70. Soldano teaches a photonics module having a receiving optical subassembly (“ROSA”) and a transmitter optical subassembly (“TOSA”), which uses an arrayed waveguide grating (“AWG”) demultiplexer (404) for receiving a multi-wavelength optical input (401) and a plurality of output channel waveguides (406) of a planar light circuit (“PLC”) (302) to transmit separate demultiplexed channel wavelengths to an array of photodetectors (505) using a polished angled end face (409) of the PLC. Ex. 1005, FIGS. 3-4, 7:63-8:24.

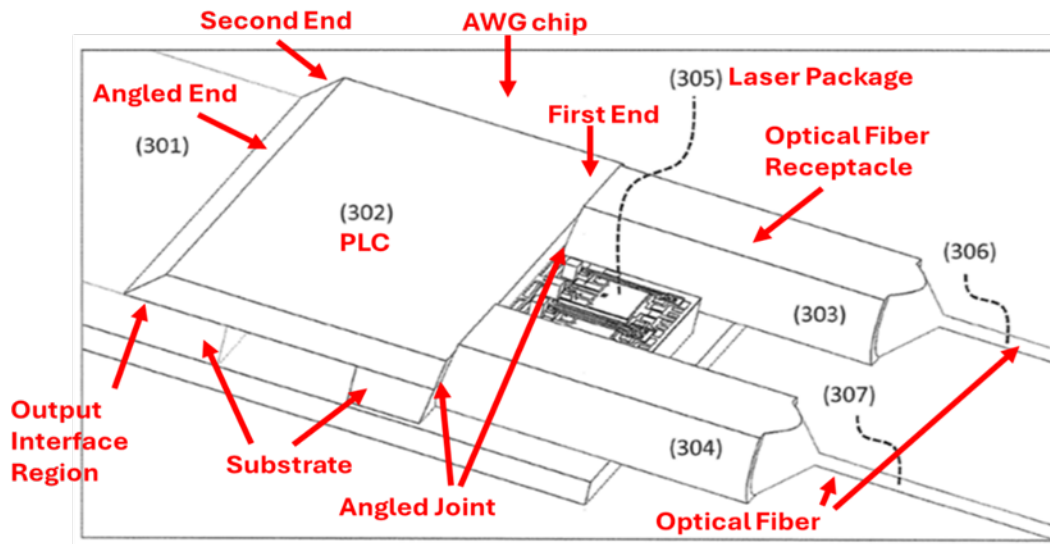


FIG. 3
(Annotated)

71. Soldano's PLC (302) includes a layer of core material (503) that extends between the first and second ends and includes a demultiplexer (404) for demultiplexing a multi-channel wavelength input optical signal (401) to four separate channel wavelength waveguides (406) which are redirected to the array of photodetectors (505) Ex. 1005, FIGS. 3-4, 7:63-8:24, 10:10-19.

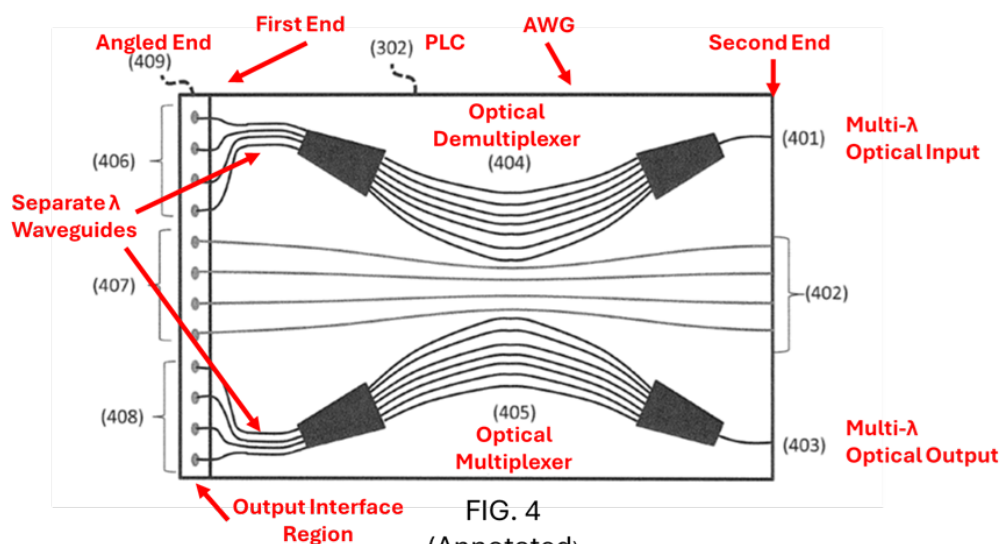


FIG. 4
(Annotated)

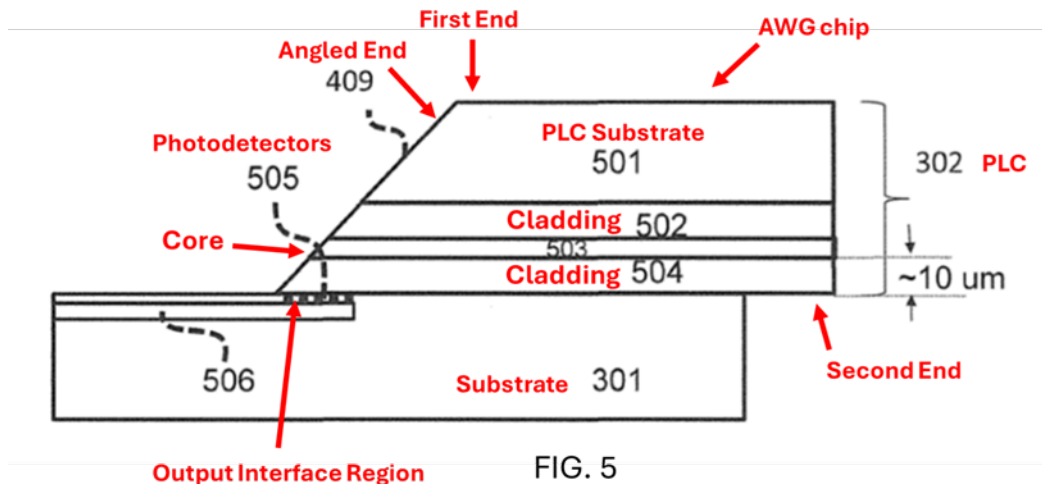


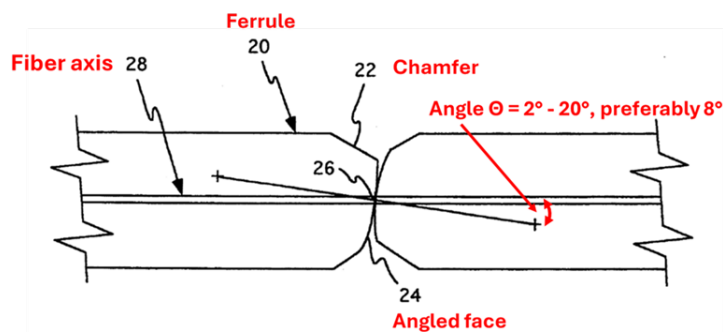
FIG. 5
(Annotated)

b. Lurie and Tomita Overview

72. U.S. Patent No. 5,351,327 (“Lurie et al.”), Exhibit 1006 issued September 27, 1994, and refers to U.S. Patent No. 4,978,193 (“Tomita”), Exhibit 1007, issued December 18, 1990. Both patents discuss what was commonly known to a POSITA regarding coupling of optical communication fibers more than two decades before the application for the ’116 Patent was filed, although neither was cited during prosecution of the ’116 Patent.

73. Lurie et al. is directed to a method of polishing ferrules used in optical fiber connectors to provide angled physical contact between pairs of interconnected fibers. Ex. 1006, Abstract. As explained in the Background of the Invention, “[t]he prior art further recognizes that signal transmission across a connector may be improved by imparting an angled finish to the end face of the fibers. This construction results in reduced internal reflections of the signals at the

end face.” Ex. 1006, 1:35-39.



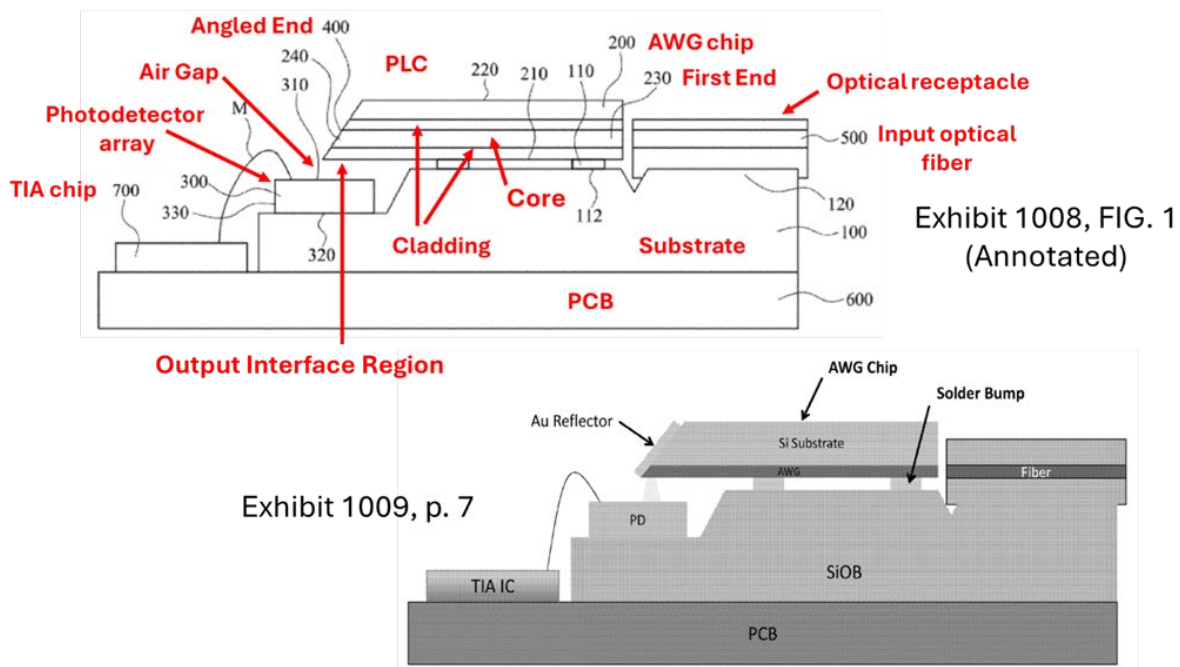
Ex. 1006, FIG. 2 (annotated)

74. As disclosed in the “Summary of the Invention” portion of Lurie, the desired angle of inclination of the abutting ends of the optical fibers is “usually about 8° .” See Ex. 1006, 3:16-18, 4:35-43 (citing Tomita U.S. Patent No. 4,978,193)(Ex. 1007); see also Ex. 1007, 2:58-68 (“An angle of inclination of the end face 22 relative to a plane 24 which is normal to the longitudinal axis [of the optical fiber] is preferably between 3° and 12° , more preferably between 5° and 10° , e.g. 8° , the precise angle to be used being governed by several design considerations, one of which is the minimum angle required so that substantially all reflected light from an end 28 of the fiber exceeds a critical acceptance angle of the fiber so that the reflected light is not guided by the fiber core in a back reflection direction but is rather refracted into the fiber cladding and dissipated thereby.”)

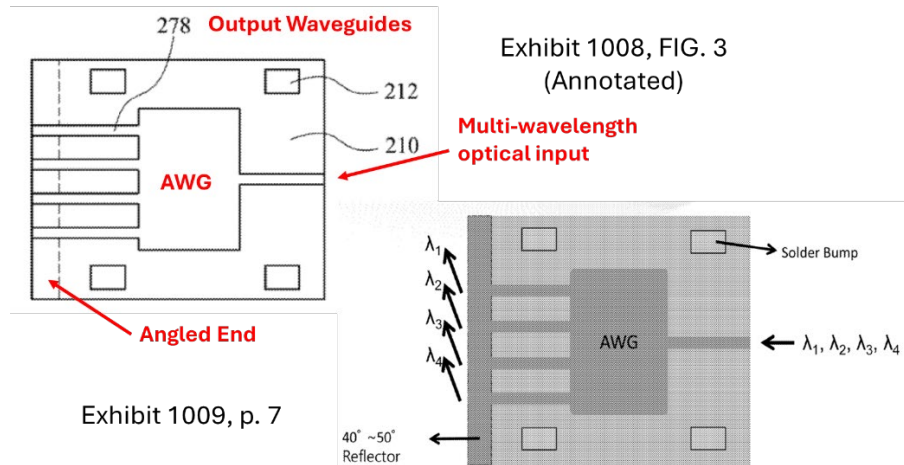
c. Shen Overview

75. U.S. Patent App. Pub. No. US 2016/0349451 (“Shen”), Exhibit 1008 filed on May 24, 2016, and published on December 1, 2016, claims priority to U.S. IPR2025-00435, Exhibit 1003

Provisional Patent Application 62/166,015, filed May 25, 2015, Exhibit 1009. I understand from counsel for CIG USA that the Shen provisional application and corresponding parts of the Shen non-provisional application qualify as prior art under at least 35 U.S.C. § 102(a)(2). Shen was cited by the Patent Owner in a January 29, 2018, IDS, but was not applied in a rejection by the Examiner during prosecution of the '116 Patent.



77. Shen discloses that the input multi-wavelength optical input signal is demultiplexed by the AWG and transmitted via separate channel wavelength waveguides (278) to the angled end (400), where the light is directed to the photodetector array (300).

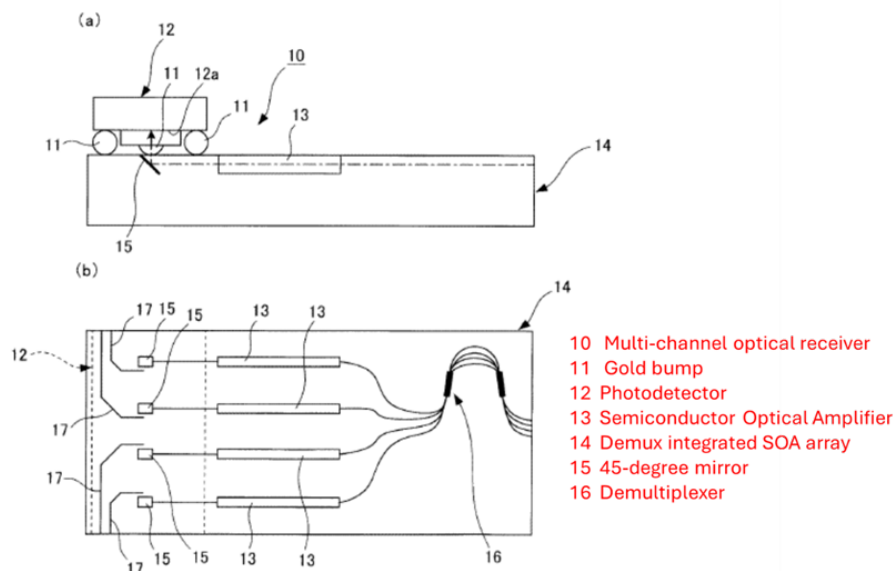


d. Kanazawa Overview

78. Japanese Patent Pub. JP 2012-034314A (“Kanazawa”), Exhibit 1010, and Exhibit 1011 (English translation), was filed on August 3, 2010, and published on April 2, 2014. I understand that it is prior art under at least 35 U.S.C. § 102(a)(1). It was not cited during prosecution of the ’116 Patent.

79. Kanazawa teaches a multi-channel optical receiver including a planar light circuit (PLC) (14) including a demultiplexer (16) for splitting a multiwavelength input signal into multiple channel wavelengths, which are then transmitted along corresponding waveguides (semiconductor optical amplifiers (13)). See Ex. 1010, FIGS. 1(a), 1(b); Ex. 1011, Abstract, ¶¶ [0006]-[0007].

80. Kanazawa discloses 45-degree mirrors (15) that redirect the channel wavelengths onto photodetectors (12) for conversion to electrical signals. *Id.*, See Ex. 1010, FIGS. 1(a), 1(b)(reproduced below with translated labels).

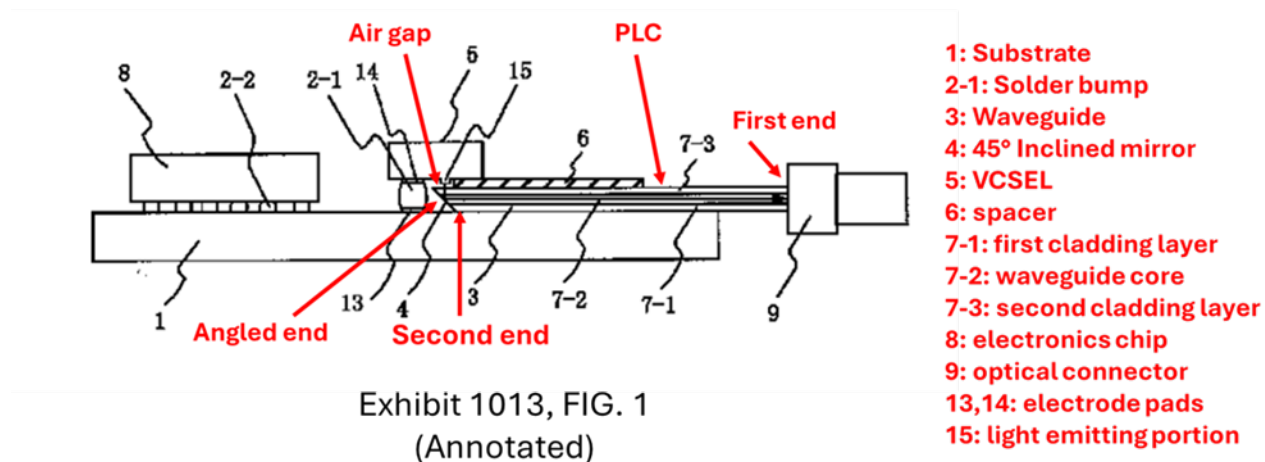


e. Sasaki Overview

81. Japanese Patent App. Pub. JP 2003-215371A (“Sasaki”), Exhibit 1012 and Exhibit 1013 (English translation), was filed on January 25, 2002, and published on July 30, 2003. I understand that it qualifies as prior art under at least 35 U.S.C. § 102(a)(1). It was not cited during prosecution of the ’116 Patent.

82. Sasaki discloses combination of a surface-type optical element (VCSEL or photodetector 15) and a planar light circuit (PLC) for use in a photonics module having a plurality of channel wavelength waveguides (3), wherein the PLC has an angled end (4) that redirects light from a light emitting unit to a channel waveguide (7-2) or from a channel waveguide (7-2) to a VCSEL or photodetector

(15). Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0018], [0023], [0032], [0042].



83. Sasaki discloses that the light emitting unit/photodiode (15) and optical waveguides (7-2) are aligned with to each other via the angled end (mirror 4) across and air gap. Ex. 1012, FIG. 1; Ex. 1013, Abstract, ¶ [0017].

X. Grounds

Ground	Reference Or Reference Combination	Claims
Ground 1	Soldano	1-11
Ground 2	Soldano + Lurie or Tomita	12-19
Ground 3	Shen	1-11
Ground 4	Shen + Soldano + Lurie or Tomita	12-19
Ground 5	Kanazawa + Sasaki	1-11
Ground 6	Kanazawa + Sasaki + Lurie or Tomita	12-19

Ground 1: Soldano anticipates Claims 1-11.

i. Claim 1: [1a] An arrayed waveguide grating (AWG) chip comprising:

84. Soldano discloses an optical transceiver module having a ROSA that includes an AWG. *See* Ex. 1005, FIGS. 3–5, 7:62-8:28.

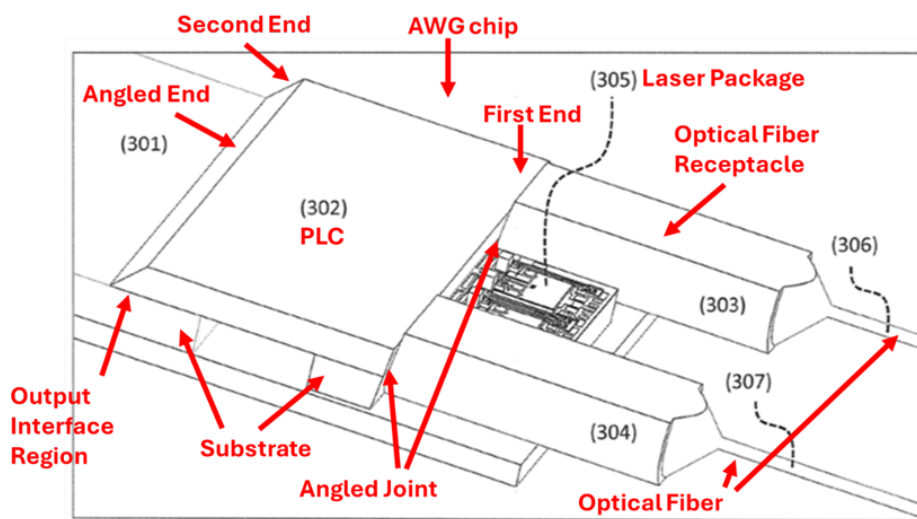


FIG. 3
(Annotated)

ii. Claim 1: [1b] a first end for coupling to an optical coupling receptacle to receive an optical signal comprising a plurality of channel wavelengths;

85. Soldano discloses the AWG chip has a first end for coupling to an optical coupling receptacle (303) to receive an optical signal including a plurality of channel wavelengths. *See* Ex. 1005, FIGS. 3-5, 7:62–8:8, 8:61-9:23.

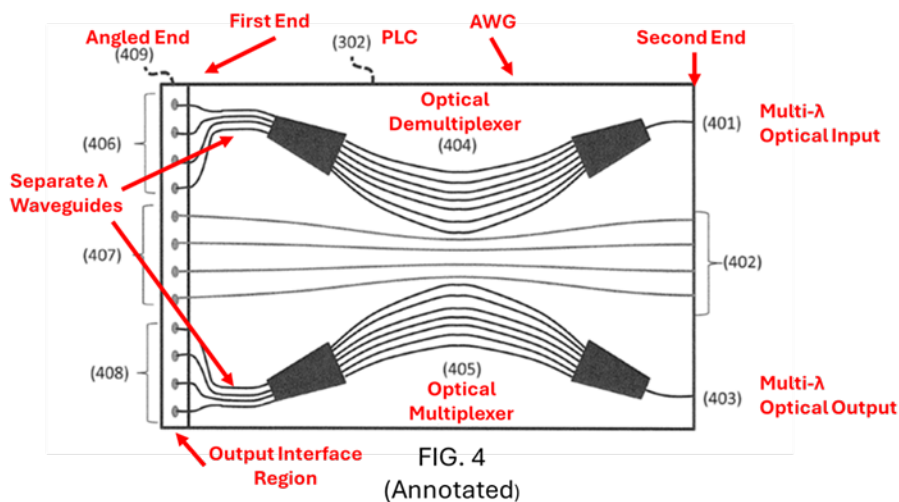
iii. Claim 1: [1c] a substrate;

86. Based on my understanding as to how the Patent Owner has construed the term “substrate” for purposes of alleging infringement in the pending litigation,

Soldano discloses that the AWG chip is supported atop the silicon photonics chip (301), which serves as a substrate. *See* Ex. 1005, FIG. 5, 8:62-9:10, 9:53-55.

iv. **Claim 1: [1d] a planar lightwave circuit (PLC) disposed on the substrate, the PLC coupled to the first end and configured to de-multiplex each channel wavelength of the plurality of channel wavelengths;**

87. Soldano discloses a planar lightwave circuit (PLC) (302) is disposed on the substrate (303). The PLC (302) is coupled to first end and de-multiplexes the incoming multi-wavelength optical signal (401) into a discrete plurality of channel wavelengths. *See* Ex. 1005, FIGS. 3-5, 4:15-39, 7:62-8:8, 8:61-9:10.



v. **Claim 1: [1e] a plurality of output waveguides coupled to the PLC, each of the output waveguides configured to receive light corresponding to an associated de-multiplexed channel wavelength launched from the PLC and provide the light along a first light path that extends towards a second end of the AWG chip; and**

88. In my opinion, Soldano discloses a plurality of output waveguides that are coupled to the PLC, with each of the output waveguides transmitting light of a channel wavelength launched from PLC along a first light path that extends towards the second end (409) of the AWG chip. *See* Ex. 1005, FIGS. 3-5, 8:61-9:23.

vi. Claim 1: [1f] a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an exposed output interface region of the AWG chip, wherein the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate.

89. Soldano discloses a tapered region (409) is located at second end of the AWG chip, which receives light via the plurality of output waveguides and reflects the light towards exposed output interface region of the AWG chip, such that exposed output interface region emits received light from the AWG chip on the same side as the substrate (301) without passing the received light through the substrate. *See* Ex. 1005, FIGS. 4, 5 (reproduced below), 9:52-10:25. Thus, in my opinion, a POSITA would understand that Soldano discloses all of the elements of, and therefore anticipates, Claim 1.

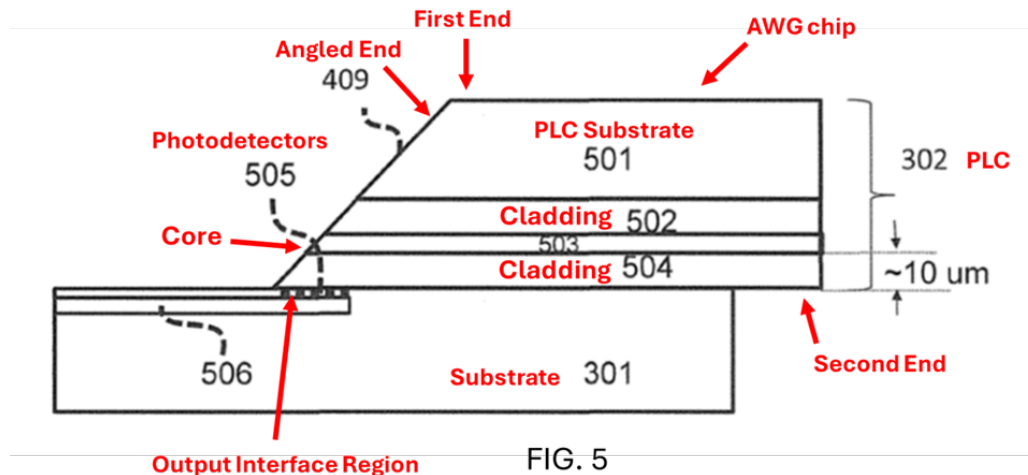


FIG. 5
(Annotated)

vii. **Claim 2:** The AWG chip of claim 1, wherein the exposed output interface region is configured to pass the reflected light received via the plurality of output waveguides out of the AWG chip along a second light path that is substantially orthogonal to the first light path.

90. It is my opinion that Soldano discloses that the exposed output interface region is configured to pass reflected light received via the plurality of waveguides (503) out of the AWG chip along a path that is substantially orthogonal to the first light path. *See* Ex. 1005, FIG. 5, 3:17-24, 9:52-10:17. For the device of Claim 1, *see supra*, Sections X.a.i-vi.

91. Accordingly, in my opinion, a POSITA would have understood that Soldano anticipates Claim 2.

viii. **Claim 3:** The AWG chip of claim 1, wherein the AWG chip defines a plurality of sidewalls extending longitudinally from the first end to the second end, and wherein the tapered region of the second end defines an angled surface that extends from a first sidewall of the plurality of sidewalls to a second sidewall of the plurality of sidewalls.

92. It is my opinion Soldano discloses an AWG chip defines a plurality of

sidewalls extending longitudinally from first end to second end, wherein a tapered region (409) of the second end defines an angled surface that extends from a first sidewall of the plurality of sidewalls to a second sidewall of the plurality of sidewalls. *See* Ex. 1005, FIGS. 4, 5, 9:23–37. For the device of Claim 1, *see supra*, Sections X.a.i-vi.

93. Accordingly, a POSITA would have understood that Soldano anticipates Claim 3.

ix. Claim 4: The AWG chip of claim 3, wherein the angled surface has an interior angle of about 41 to 45 degrees relative to the exposed output interface region.

94. It is my opinion that Soldano discloses that the AWG chip has an angled polish surface that redirects light from a horizontal orientation in the channel wavelength waveguides to vertical orientation exiting the PLC, which angle is within the claimed range of 41 to 45 degrees relative to the exposed output interface region. *See* Ex. 1005, FIGS. 4-5, 9:23-37. For the device of Claim 1, *see supra*, Sections X.a.i-vi.

95. Thus, a POSITA would have understood that Soldano anticipates Claim 4.

x. Claim 5: The AWG chip of claim 3, wherein each of the output waveguides comprise a core material, and wherein a cladding material is disposed on the core material, the core material defining at least a portion of the plurality of sidewalls of the AWG chip.

96. It is my opinion that Soldano discloses that the output waveguides of the AWG chip comprise a core material (503) and include a cladding material (502), (504) disposed on the core material (503), such that the core material defines at least a portion of the first and second sidewalls. *See* Ex. 1005, FIGS. 4-5, 9:56-66. For the device of Claim 1, *see supra*, Sections X.a.i-vi.

97. Thus, a POSITA would have understood that Soldano anticipates Claim 5.

xi. Claim 6: The AWG chip of claim 5, wherein the core material of each of the plurality of output waveguides has a first index of refraction, and a medium external to and adjacent the tapered region has a second index of refraction, the first index of refraction being greater than the second index of refraction.

98. Soldano discloses that the core material (503) of each of the plurality of waveguides has a first index of refraction (e.g., silica with n greater than 1.45) and that the medium external (e.g., air, $n \sim 1.0$) to and adjacent the tapered region (409) has a second index of refraction, such that the first index of refraction is greater than the second index of refraction. *See* Ex. 1005, FIGS. 4-5, 9:56-60. For the device of Claim 5, *see supra*, Section X.a.x.

99. A POSITA would have understood that Soldano anticipates Claim 6.

xii. Claim 7: The AWG chip of claim 6, wherein the external medium comprises a material having an index of refraction of about 1.0.

100. It is my opinion that a POSITA would have understood that the AWG chip described in Soldano typically would be enclosed within a module containing air or an inert gas to prevent the accumulation of dust. A POSITA therefore would have understood that the external medium adjacent to the tapered region (409) of the AWG chip would be air or similar gas having an index of refraction of about 1.0. For the device of Claim 6, *see supra*, Section X.a.xi.

101. Thus, a POSITA would have understood that Soldano anticipates Claim 7.

xiii. Claim 8: The AWG chip of claim 5, wherein the core material of each of the plurality of output waveguides provide a portion of the angled surface, and wherein the angled surface is configured to reflect incident light based on at least an interior angle of the angled surface.

102. It is my opinion that Soldano discloses that the core material (503) provides a portion of the angled surface (409) and that the angled surface is configured to reflect light based at least on the interior angle of the angled surface. *See* Ex. 1005, FIG. 5, 9:23-37, 52-66. For the device of Claim 5, *see supra*, Section X.a.x.

103. Accordingly, in my view, a POSITA would have understood that Soldano anticipates Claim 8.

xiv. Claim 9: The AWG chip of claim 5, wherein the core material comprises doped silica (SiO₂) having an index of refraction of about 1.45 to 1.50.

104. Soldano discloses that the PLC may be glass or one of a variety of materials typically used in making waveguides. *See* Ex. 1005, 9:45-51. Accordingly, a POSITA would have understood that core material of the AWG chip described in Soldano would be made of a material such as doped fused silica having n between 1.45 and 1.5. For the device of Claim 5, *see supra*, Section X.a.x.

105. Thus, a POSITA would have understood that Soldano anticipates Claim 9.

xv. Claim 10: The AWG chip of claim 1, wherein the AWG chip is configured as a 1×N demultiplexer device whereby a single optical input signal is de-multiplexed into N different channel wavelengths.

106. Soldano discloses an AWG chip having a 1xN demultiplexer, in which a single multi-wavelength optical input signal is demultiplexed into N different wavelengths, specifically 4 different wavelengths. *See* Ex. 1005, FIGS. 3-4, 7:29-37, 7:62-8:8. For the device of Claim 1, *see supra*, Sections X.a.i-vi.

107. A POSITA would have understood that Soldano anticipates Claim 10.

xvi. Claim 11: The AWG chip of claim 1, wherein the AWG chip is implemented in an AWG device package.

108. Soldano discloses an AWG chip that is implemented in an AWG device package. *See* Ex. 1005, FIG. 3, 7:24-8:60. For the device of Claim 1, *see*

supra, Sections X.a.i-vi.

109. Accordingly, in my view a POSITA would have understood that Soldano anticipates Claim 11.

b. Ground 2: The Combination Of Soldano And Lurie Or Tomita Renders Claims 12-19 Obvious.

i. Claim 12: [12a] An optical transceiver module comprising.

110. As discussed above for Claim 1, Soldano discloses an optical transceiver module. *See* Ex. 1005, FIGS. 3-5, 7:62-8:28.

ii. Claim 12: [12b] a transceiver housing;

111. In my opinion, a POSITA would have understood that the structure disclosed in Soldano would be housed in a transceiver housing configured in accordance with a relevant photonics module specification prescribed at the time the application for the Soldano patent was filed, e.g., SFF Committee Specification SFF - 8665 for QSFP + 28 Gb/s. 4x Pluggable Transceiver Solution (QSFP28) published May 10, 2013. *See* Ex. 1001, 5:35-41.

iii. Claim 12: [12c] a multi-channel receiver optical sub-assembly (ROSA) located in the transceiver housing and including an arrayed waveguide grating (AWG) chip, the AWG chip comprising:

112. Soldano discloses a multi-channel receiver optical subassembly (ROSA) that includes an AWG chip. *See* Ex. 1005, FIGS. 3-5, 7:24-37.

iv. Claim 12: [12d] a first end for coupling to an optical coupling receptacle to receive an optical signal comprising a plurality

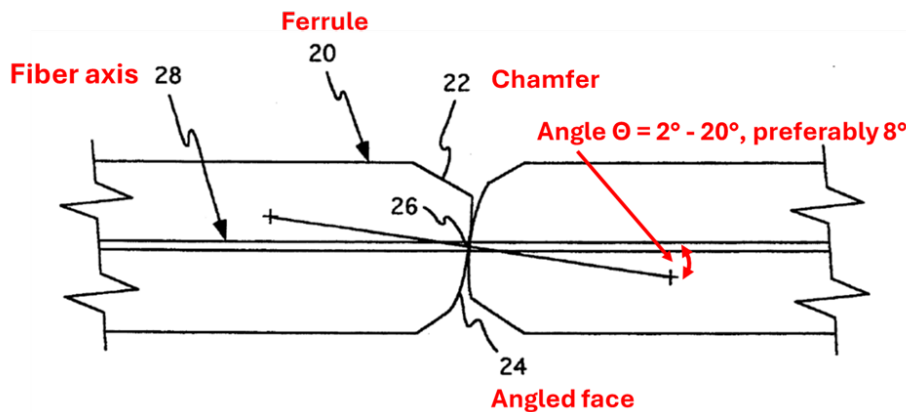
of channel wavelengths, wherein the first end for coupling to the optical coupling receptacle includes an angled surface to reduce back reflections of an optical signal launched into the AWG chip;

113. Soldano discloses an AWG chip having a first end coupled to an optical coupling receptacle (303) to receive an incoming optical signal comprising a plurality of channel wavelengths (401). As illustrated in FIG. 3, the first end of the PLC includes an angled surface where it joins the optical receptacle (303) to reduce back reflections of the optical signal launched into the AWG chip. *See* Ex. 1005, FIG. 3, 3:17-25, 4:15-39, 7:62-8:8, 8:61-9:10.

114. In my opinion a POSITA also would have understood that when coupling optical components, angled physical junctions should be used to reduce back-reflections. This concept was well-known in the optical communications field many years before the application for the '116 patent was filed. *See, e.g.*, U.S. Patent No. 5,351,327 to Lurie et al., Ex. 1006, which refers to U.S. Patent No. 4,978,193 to Tomita, Ex. 1007. Both patents describe employing an angled junction when coupling optical communication fibers to reduce back reflections.

115. Specifically, Lurie is directed to a method of polishing ferrules used in optical fiber connectors to provide angled physical contact between pairs of interconnected fibers. Ex. 1006, Abstract. As explained in the Background of the Invention of Lurie, “[t]he prior art further recognizes that signal transmission across a connector may be improved by imparting an angled finish to the end face of the

fibers. This construction results in reduced internal reflections of the signals at the end face.” Ex. 1006, 1:35-39.



Ex. 1006, FIG. 2 (annotated)

116. As further disclosed in the “Summary of the Invention” portion of Lurie, the desired angle of inclination of the abutting ends of the optical fibers is “usually about 8° .” See Ex. 1006, 3:16-18, 4:35-43, citing U.S. Patent No. 4,978,193 to Tomita, Ex. 1007.

117. Tomita describes that for coupling optical components, “An angle of inclination of the end face 22 relative to a plane 24 which is normal to the longitudinal axis [of the optical fiber] is preferably between 3° and 12° , more preferably between 5° and 10° , e.g. 8° , the precise angle to be used being governed by several design considerations, one of which is the minimum angle required so that substantially all reflected light from an end 28 of the fiber exceeds a critical acceptance angle of the fiber so that the reflected light is not guided by the fiber core in a back reflection direction but is rather refracted into the fiber cladding and

dissipated thereby.” *See* Ex. 1007, 2:58-68.

118. It is my opinion that it was common knowledge in the field of optical communications, decades before the application for the '116 Patent was filed, that optical components should be joined using an angled junction, and this knowledge was possessed by POSITAs. Accordingly, a POSITA would have had strong motivation to combine the angled junction of Lurie or Tomita where the optical fiber meets the AWG of Soldano, and indeed that appears what is depicted in the FIG. 3 of Soldano. In my view, it would have been obvious in Soldano to angle the surface where the PLC that couples to the optical coupling receptacle (303) and fiber (306) for the reasons described in Lurie and Tomita and this is depicted in FIG. 3 of Soldano, reproduced below.

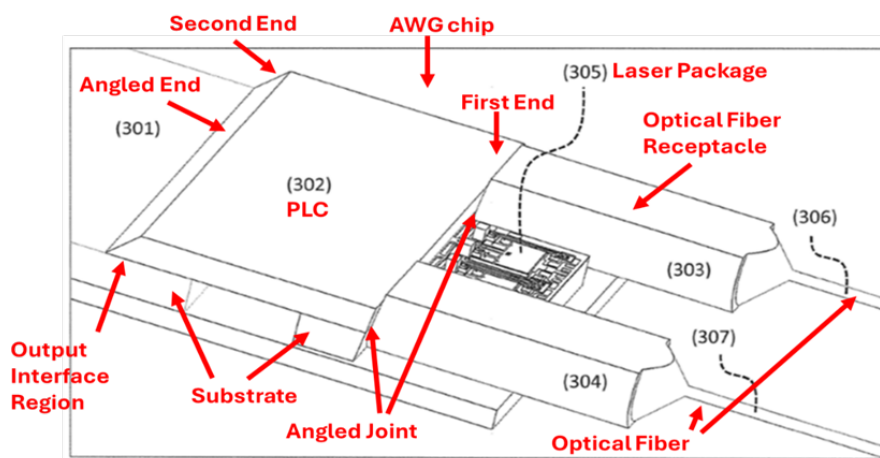


FIG. 3
(Annotated)

v. **Claim 12: [12e] a planar lightwave circuit (PLC) coupled to the first end configured to de-multiplex each channel wavelength of the plurality of channel wavelengths;**

119. Soldano discloses a PLC (302) coupled to the first end (401) configured to de-multiplex (404) each channel wavelength of the plurality of channel wavelengths. *See* Ex. 1005, FIGS. 4-5, 8:61-9:23.

vi. Claim 12: [12f] a plurality of output waveguides coupled to the PLC, each of the output waveguides configured to receive light corresponding to an associated de-multiplexed channel wavelength launched from the PLC and provide the light along a first light path that extends towards a second end of the AWG chip; and

120. In my opinion, Soldano discloses a plurality of output waveguides coupled to the PLC (302) configured to receive light corresponding to an associated de-multiplexed channel wavelength launched from PLC and transmit the light along a first light path towards a second end (409) of the AWG chip. *See* FIGS. 4-5, 9:5-10, 9:52-10:25.

vii. Claim 12: [12g] a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an output interface region of the AWG chip;

121. Soldano discloses a tapered region (409) at the second end of PLC (302) of the AWG chip to receive light via the plurality of output waveguides and reflects the light towards an output interface region of the AWG chip. *See* Ex. 1005, FIGS. 4, 5, 9:23-34, 9:52-65.

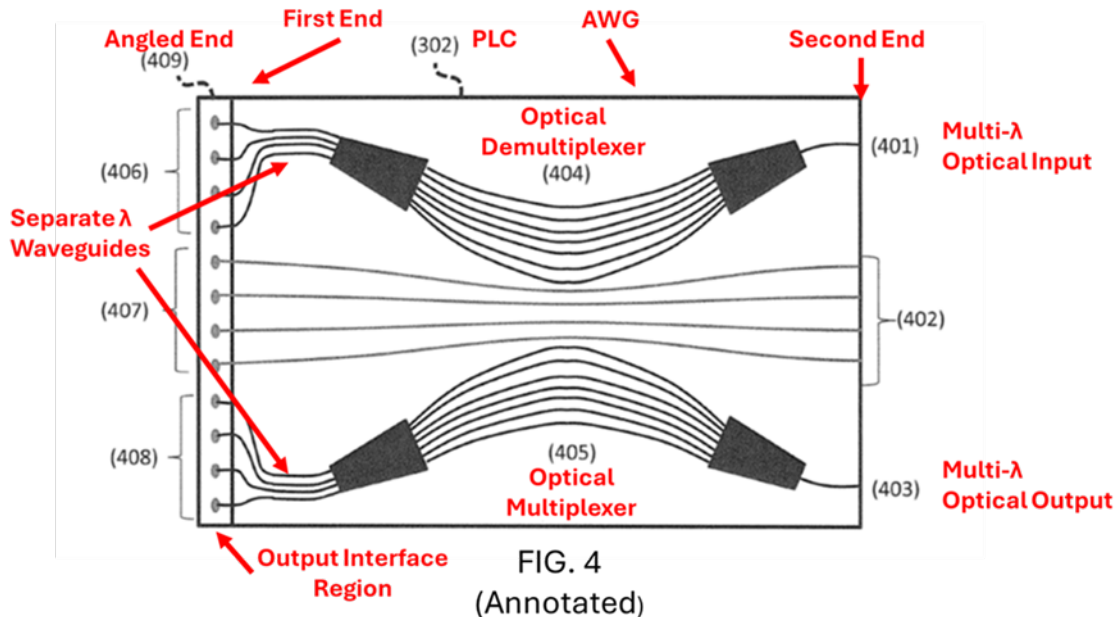
viii. Claim 12: [12h] an array of detector devices disposed adjacent to the output interface region of the AWG chip; and

122. Soldano describes that light directed to the silicon photonics chip 301

alternatively could pass through grating couplers 505 or directly to an array of photodetectors. *See* Ex. 1005, 10:10-19 (“On the receiver side, a grating coupler may not be necessary. Depending on the silicon technology, the light in the glass PLC 302 could be deflected down by the side polish 409 and instead of hitting a grating coupler 505 and entering a waveguide 506, could instead hit a photodetector that would be placed in lieu of the grating coupler 505. The photodetector would then be electrically connected to the transimpedance amplifier”). Accordingly, in my opinion, a POSITA would have understood that in the above-described embodiment of Soldano, individual optical wavelengths exiting the AWG would have been directly coupled to corresponding detector devices.

ix. Claim 12: [12i] a multi-channel transmitter optical assembly (TOSA) including at least one laser package located in the transceiver housing for transmitting optical signals at different channel wavelengths.;

123. In my opinion, Soldano discloses a multi-channel transmitter optical assembly (TOSA) including at least one laser package located in the transceiver housing for transmitting signals at different channel wavelengths. Specifically, Soldano discloses that separate channel wavelengths processed by silicon photonics chip (301) and modulated by lasers then are passed back via the angled end (409) to the multiplexer (405) of PLC (302). *See* Ex. 1005, FIGS. 3-5, 7:37-51, 8:20-28, 8:54-60, 9:10-15.



124. In view of the above, it is my opinion that a POSITA would have understood that Soldano fully anticipates Claim 12. However, to the extent that a POSITA could not rely on the angled connection between the AWG and the optical connector depicted in FIG. 3 of Soldano, a POSITA would have been readily aware that an angled junction should be used therebetween, as taught decades earlier by Lurie and Tomita.

x. Claim 13: The optical transceiver module of claim 12, wherein the output interface region of the AWG chip is an exposed region adjacent an air gap, and wherein the air gap separates the output interface region of the AWG chip and the array of detector devices.

125. In my opinion, a POSITA would have understood that when PLC (302) is aligned with silicon photonics chip (301), an air gap will exist between the output interface region of the angle polish (409) and grating couplers or

photodetectors (505), for example, to permit alignment of these pieces and to accommodate thermal expansion of the components. *See* Ex. 1005, FIG. 5, 8:29-60, *see also* Ex. 1008, FIG. 1, ¶ 43; Ex. 1009, pp. 6, 8. For the device of Claim 12, *see supra*, ¶¶ X.b.i-ix.

126. A POSITA would have understood that Soldano alone fully anticipates Claim 13, or alternatively, that the combination of Soldano and knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 13 obvious.

xi. Claim 14: The optical transceiver module of claim 12, wherein the output interface region of the AWG chip is separated from the array of detector devices by about 50 microns.

127. It is my opinion that a POSITA would have understood the benefit of not having the output interface region of the PLC (302) in intimate contact with the silicon photonics chip (301). For example, a POSITA would readily recognize the benefits of providing an offset between these structures to account for the effects of thermal expansion. I am therefore of the view that it would have been a simple design choice to leave an air gap of 50 microns between the PLC and the photodetectors, especially as I could find no specific advantage attributed to this feature in the '116 Patent. *See* Ex. 1001, 10:14-17. For the device of Claim 12, *see supra*, Sections X.b.i-ix.

128. Thus, a POSITA would have understood that Soldano alone fully anticipates Claim 14, or alternatively, that the combination of Soldano and

knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 14 obvious.

xii. Claim 15: The optical transceiver module of claim 12, wherein the AWG chip defines a plurality of sidewalls extending longitudinally from the first end to the second end, and wherein the tapered region of the second end defines an angled surface that extends from a first sidewall of the plurality of sidewalls to a second sidewall of the plurality of sidewalls.

129. It is my opinion that Soldano discloses AWG chip defines a plurality of sidewalls that extend longitudinally from the first end to the second end, wherein a tapered region (409) of the second end defines an angled surface that extends from a first sidewall of the plurality of sidewalls to a second sidewall of the plurality of sidewalls. *See* Ex. 1005, FIGS. 4, 5, 9:23–37. For the device of Claim 12, *see supra*, Sections X.b.i-ix.

130. Thus, a POSITA would have understood that Soldano alone fully anticipates Claim 15, or alternatively, that the combination of Soldano and knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 15 obvious.

xiii. Claim 16: The optical transceiver module of claim 15, wherein the angled surface has an interior angle of about 41 to 45 degrees relative to the output interface region.

131. Soldano discloses that the AWG chip has an angled end (409) that redirects light from a horizontal orientation in the channel wavelength waveguides

to vertical orientation exiting the PLC (302), which is within the claimed range of 41 to 45 degrees relative to the exposed output interface region. *See* Ex. 1005, FIGS. 4-5, 9:23-37. For the device of Claim 15, *see supra*, Section X.b.xii.

132. Thus, a POSITA would have understood that Soldano alone fully anticipates Claim 16, or alternatively, that the combination of Soldano and knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 16 obvious.

xiv. Claim 17: The optical transceiver module of claim 15, wherein each of the output waveguides comprise a core material, and wherein a cladding material is disposed on the core material, the core material defining at least a portion of the plurality of sidewalls of the AWG chip.

133. Soldano discloses that the output waveguides of the AWG chip comprise a core material (503) and include a cladding material (502), (504) disposed on the core material (503), such that the core material defines at least a portion of the first and second sidewalls. *See* FIGS. 4-5, 9:56-66. For the device of Claim 15, *see supra*, Section X.b.xii.

134. A POSITA would have understood that Soldano alone fully anticipates Claim 17, or alternatively, that the combination of Soldano and knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 17 obvious.

xv. Claim 18: The optical transceiver module of claim 17, wherein the core material of each of the plurality of output waveguides provide a portion of the angled surface, and wherein the angled surface

is configured to reflect incident light based on at least an interior angle of the angled surface relative to the output interface of the AWG chip.

135. It is my opinion that Soldano discloses that the core material (503) provides a portion of the angled surface (409) and that the angled surface (409) is configured to reflect light based at least on the interior angle of the angled surface relative to the output interface of the AWG chip. *See* Ex. 1005, FIG. 5, 9:23-37, 52-66. For the device of Claim 17, *see supra*, Section X.b.xiv.

136. A POSITA would have understood that Soldano alone fully anticipates Claim 18, or alternatively, that the combination of Soldano and knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 18 obvious.

xvi. Claim 19: The optical transceiver of claim 12, wherein the transceiver is a Small Form-factor Pluggable (SFP) transceiver module and the ROSA is configured to receive at least four different channel wavelengths at transmission rates of at least about 25 Gbps per channel.

137. It is my opinion that a POSITA would have understood that the photonics structure disclosed in Soldano could be used in any available module format that existed circa 2016 when the application for the '116 patent was filed. This includes the Quad Small Form-factor pluggable "QSFP" specification, released in 2013, discussed *supra*, element 12(b), which specified at least four different channel wavelengths of 25 Gbps per channel. For the device of Claim 12, *see supra*, Sections X.b.i-ix.

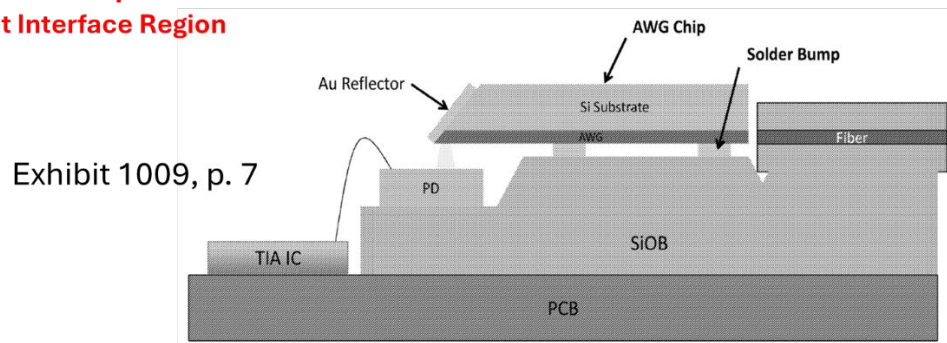
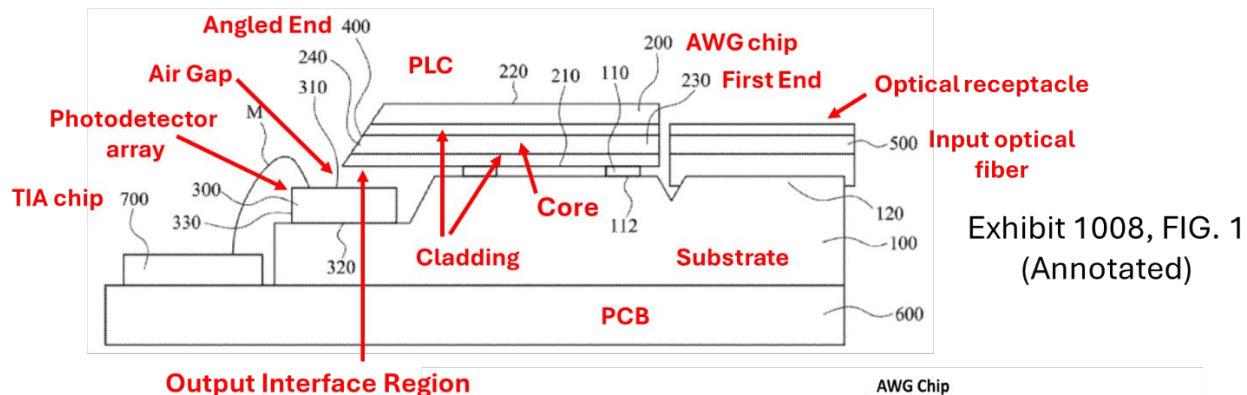
138. Thus, a POSITA would have understood that Soldano alone fully anticipates Claim 19, or alternatively, that the combination of Soldano and knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 19 obvious.

c. Ground 3: Claims 1-11 Are Unpatentable Under 35 U.S.C. §102 As Anticipated By Shen, Exhibits 1008 and 1009.

139. In the analyses below, I base my opinions on the disclosures of FIGS. 1-3 of the published Shen U.S. patent application, Ex. 1008, and the corresponding figures and supporting text of the Shen U.S. provisional patent application, Ex. 1009, which is incorporated by reference into Shen. *See* Ex. 1008, ¶ [0001].

i. Claim 1: [1a] An arrayed waveguide grating (AWG) chip comprising:

140. Shen discloses an arrayed waveguide grating (AWG) chip (200), which a POSITA would have understood had its intended use in an optical receiver or transceiver module. *See* Ex. 1008, FIGS. 1-3, ¶ [0033]; Ex. 1009, pp. 5-8.



ii. **Claim 1: [1b] a first end for coupling to an optical coupling receptacle to receive an optical signal comprising a plurality of channel wavelengths;**

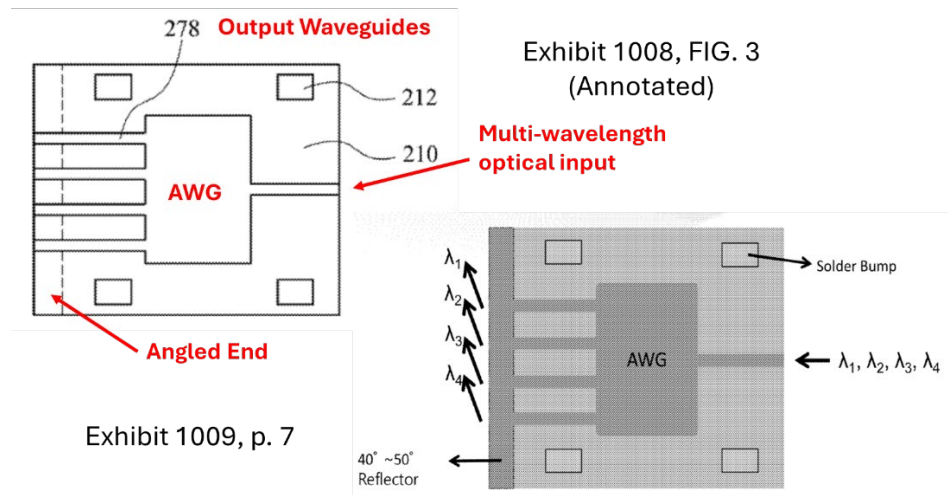
141. Shen discloses the AWG chip (200) has a first end (230) for coupling to an optical fiber (500) to receive an optical signal including a plurality of channel wavelengths. *See* Ex. 1008, FIG. 4, ¶ [0043]; Ex. 1009, p. 7.

iii. **Claim 1: [1c] a substrate;**

142. Based on my understanding as to how the Patent Owner has construed the term “substrate” for purposes of alleging infringement in the pending litigation, Shen discloses that the AWG chip (200) is supported atop a silicon optical bench (SiOB)(100), which serves as substrate. Ex. 1008, ¶¶ [0007], [0017]-[0020], [0033], [0036]-[0037], [0043]; Ex. 1009, pp. 6-8.

iv. **Claim 1: [1d] a planar lightwave circuit (PLC) disposed on the substrate, the PLC coupled to the first end and configured to de-multiplex each channel wavelength of the plurality of channel wavelengths;**

143. Shen discloses a planar lightwave circuit (PLC) is disposed on substrate (100). As illustrated in the figures above from Exs. 1008 and 1009, the PLC is coupled to the first end (230) and de-multiplexes the incoming multi-wavelength optical signal into a discrete plurality of channel wavelengths. See Ex. 1008, FIG. 4, ¶¶ [0035], [0043]; Ex. 1009, p. 7.



v. **Claim 1: [1e] a plurality of output waveguides coupled to the PLC, each of the output waveguides configured to receive light corresponding to an associated de-multiplexed channel wavelength launched from the PLC and provide the light along a first light path that extends towards a second end of the AWG chip; and**

144. In my opinion, Shen discloses a plurality of output waveguides (278) are coupled to PLC, with each of the output waveguides (278) designed to transmit light of a channel wavelength launched from PLC along first light path that extends

towards second end of the AWG chip (200). *See* Ex. 1008, FIGS. 1-3, ¶¶ [0038]-[0039], [0043]; Ex. 1009, pp. 6-8.

vi. Claim 1: [1f] a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an exposed output interface region of the AWG chip, wherein the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate.

145. Shen discloses a tapered region (400) located at second end of the AWG chip (200), which receives light via the plurality of output waveguides (278) and reflects the light towards exposed output interface region of AWG chip, such that exposed output interface region emits received light from the AWG chip on the same side as substrate (100) without passing the received light through the substrate. *See* Ex. 1008, FIGS. 1-3, ¶¶ [0038]-[0039], [0043]; Ex. 1009, pp. 6-8. Thus, in my opinion, a POSITA would understand that Shen anticipates Claim 1.

vii. Claim 2: The AWG chip of claim 1, wherein the exposed output interface region is configured to pass the reflected light received via the plurality of output waveguides out of the AWG chip along a second light path that is substantially orthogonal to the first light path.

146. It is my opinion that Shen discloses that the output interface region is configured to pass reflected light received via the plurality of waveguides (278) out of the AWG chip along a path that is substantially orthogonal to the first light path. *See* Ex. 1008, FIGS. 1-3, ¶¶ [0038]-[0039], [0043]; Ex. 1009, pp. 6-8. For the device of Claim 1, *see supra*, Sections X.c.i-vi.

147. Accordingly, in my opinion, a POSITA would have understood that Shen anticipates Claim 2.

viii. Claim 3: The AWG chip of claim 1, wherein the AWG chip defines a plurality of sidewalls extending longitudinally from the first end to the second end, and wherein the tapered region of the second end defines an angled surface that extends from a first sidewall of the plurality of sidewalls to a second sidewall of the plurality of sidewalls.

148. It is my opinion Shen discloses the AWG chip (200) defines a plurality of sidewalls extending longitudinally from first end to second end, wherein a tapered region of the second end defines an angled end (400) that extends from a first sidewall of the plurality of sidewalls to a second sidewall of the plurality of sidewalls. *See* Ex. 1008, FIGS. 1-2, ¶¶ [0038]-[0041]; Ex. 1009, pp. 6-8. For the device of Claim 1, *see supra*, Sections X.c.i-vi.

149. A POSITA would have understood that Shen anticipates Claim 3.

ix. Claim 4: The AWG chip of claim 3, wherein the angled surface has an interior angle of about 41 to 45 degrees relative to the exposed output interface region.

150. Shen discloses that the AWG chip (200) has an angled end (400) that redirects light from a horizontal orientation in the channel wavelength waveguides (278) to vertical orientation exiting the PLC, wherein the reflector angle is 40° to 50°, which encompasses the claimed range of 41 to 45 degrees relative to the output interface region. *See* Ex. 1008, FIGS. 1-2, ¶¶ [0038]-[0041]; Ex. 1009, pp. 6-8. For the device of Claim 3, *see supra*, Section X.c.viii.

151. Thus, in my view, a POSITA would have understood that Shen anticipates Claim 4.

x. Claim 5: The AWG chip of claim 3, wherein each of the output waveguides comprise a core material, and wherein a cladding material is disposed on the core material, the core material defining at least a portion of the plurality of sidewalls of the AWG chip.

152. Shen discloses that the output waveguides (278) of the AWG chip (200) comprise a core material (270) and cladding material (250), (260) disposed on either side of the core material (270), such that the core material defines at least a portion of the first and second sidewalls. *See* Ex. 1008, FIGS. 1-2, ¶¶ [0041]-[0042]; Ex. 1009, pp. 6-8. For the device of Claim 3, *see supra*, Section X.c.viii.

153. Thus, a POSITA would have understood that Shen anticipates Claim 5.

xi. Claim 6: The AWG chip of claim 5, wherein the core material of each of the plurality of output waveguides has a first index of refraction, and a medium external to and adjacent the tapered region has a second index of refraction, the first index of refraction being greater than the second index of refraction.

154. Shen discloses that the core material (270) of each of the plurality of waveguides (278) has a first index of refraction (e.g., silica with n greater than 1.45) and that the medium external (e.g., air, $n \sim 1.0$) to and adjacent the tapered region has a second of refraction, such that the first index of refraction is greater than the second index of refraction. *See* Ex. 1008, FIGS. 1-2, ¶¶ [0038]-[0041]; Ex. 1009,

pp. 6-8. For the device of Claim 5, *see supra*, Section X.c.x.

155. Thus, a POSITA would have understood that Shen anticipates Claim 6.

xii. Claim 7: The AWG chip of claim 6, wherein the external medium comprises a material having an index of refraction of about 1.0.

156. It is my opinion that a POSITA would have understood that the AWG chip described in Shen typically would be enclosed within a module containing air or an inert gas to prevent the accumulation of dust. A POSITA therefore would have understood the external medium adjacent to the tapered region of the AWG chip (200) would be air or similar gas having an index of refraction of about 1.0.

For the device of Claim 6, *see supra*, Section X.c.xi.

157. A POSITA would have understood that Shen anticipates Claim 7.

xiii. Claim 8: The AWG chip of claim 5, wherein the core material of each of the plurality of output waveguides provide a portion of the angled surface, and wherein the angled surface is configured to reflect incident light based on at least an interior angle of the angled surface.

158. It is my opinion that Shen discloses that the core material provides a portion of the angled end (400) configured to reflect light based at least on the interior angle of the angled surface. *See* Ex. 1008, FIGS. 1-2, ¶¶ [0038]-[0041]; Ex. 1009, pp. 6-8. For the device of Claim 5, *see supra*, Section X.c.x.

159. Accordingly, in my view, a POSITA would have understood that Shen

anticipates Claim 8.

xiv. Claim 9: The AWG chip of claim 5, wherein the core material comprises doped silica (SiO₂) having an index of refraction of about 1.45 to 1.50.

160. Shen discloses that the PLC comprises an optically suitable material typically used in making waveguides. *See* FIGS. 1-2, ¶¶ [0038]-[0041]. In my opinion, a POSITA would have understood that the core material of the AWG chip described in the '116 patent typically would comprise a material, such as doped fused silica, having *n* between 1.45 and 1.5. For the device of Claim 5, *see supra*, Section X.cx.

161. A POSITA would have understood that Shen anticipates Claim 9.

xv. Claim 10: The AWG chip of claim 1, wherein the AWG chip is configured as a 1×N demultiplexer device whereby a single optical input signal is de-multiplexed into N different channel wavelengths.

162. Shen discloses an AWG chip (200) that having a 1xN demultiplexer, in which a single multi-wavelength optical input signal is demultiplexed into N different wavelengths, specifically 4 different wavelengths. *See* Ex. 1008, FIG. 3, ¶ [0043]; Ex. 1009, p. 7. For the device of Claim 1, *see supra*, Sections X.c.i- vi.

163. A POSITA would have understood that Shen anticipates Claim 10.

xvi. Claim 11: The AWG chip of claim 1, wherein the AWG chip is implemented in an AWG device package.

164. It is my opinion that a POSITA would have understood that Shen

discloses an AWG chip that is employed in an AWG device package. *See* Ex. 1008, FIG. 1, ¶¶ [0033], [0035], [0044]; Ex. 1009, pp. 5-8. For the device of Claim 1, *see supra*, Sections X.c.i-vi.

165. Accordingly, in my view a POSITA would have understood that Shen anticipates Claim 11.

d. Ground 4: Claims 12-19 are Unpatentable As Obvious Over Shen And Soldano Further In View Of Lurie Or Tomita.

i. Motivation To Combine Shen With Soldano And Lurie Or Tomita.

166. As discussed above for Claim 1, Soldano discloses an optical transceiver module. *See* Ex. 1008, FIGS. 3-5, 7:62-8:28. Shen discloses an AWG arrangement for use in a photonics module for demultiplexing an incoming multi-wavelength optical signal and directing the resulting separate wavelength optical signals onto detectors to generate electrical signals for further processing. Both Soldano and Shen relate to the same field of endeavor, optical communications, and both are directed to increasing the density of the carried signals. Accordingly, in my opinion, a POSITA would have understood that the AWG of Shen could advantageously be used in the device of Soldano, that includes similar AWG structure to implement both ROSA and TOSA functionalities.

167. It is further my opinion that when coupling the AWG of Shen to an incoming optical fiber, a POSITA would have employed the angled junction

depicted in FIG. 3 of Soldano to reduce reflections, exactly as taught by Lurie and Tomita decades earlier. Because Lurie and Tomita also both are directed to the field of optical communications, it is my opinion that the common knowledge of using angled junctions for connection of optical fibers to other optical components, would have been known to and implemented by a POSITA in implementing the structure described in Shen.

ii. Claim 12: [12a] An optical transceiver module comprising.

168. As discussed above for Claim 1, Shen discloses an arrayed waveguide grating (AWG) chip (200), which a POSITA would have understood for use in an optical receiver (as described in Shen) or as part of a transceiver module (as described in Soldano). *See* Ex. 1008, FIGS. 1-3, ¶ [0033]; Ex. 1009, pp. 5-8; Ex. 1005, FIGS. 3-5, 7:62-8:28.

iii. Claim 12: [12b] a transceiver housing;

169. In my opinion, a POSITA would have understood that the AWG chip (200) disclosed in Shen would be located in a transceiver housing configured in accordance with a relevant photonics module specification prescribed at the time the Shen patent application was filed, e.g., SFF Committee Specification SFF - 8665 for QSFP + 28 Gb/s. 4x Pluggable Transceiver Solution (QSFP28) published May 10, 2013. *See* Ex. 1001, 5:35-41.

iv. Claim 12: [12c] a multi-channel receiver optical sub-assembly (ROSA) located in the transceiver housing and including an arrayed waveguide grating (AWG) chip, the AWG chip comprising:

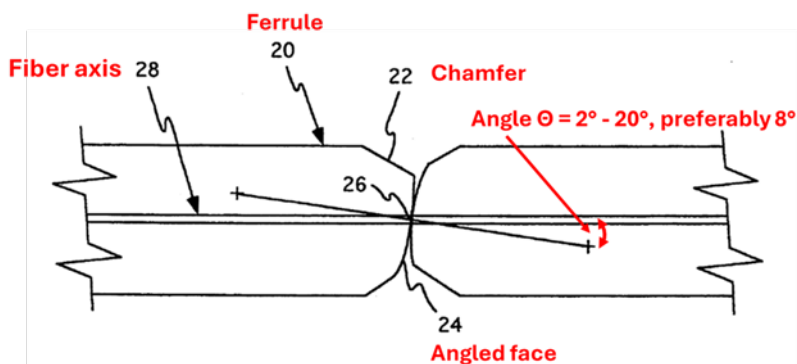
170. Shen discloses a multi-channel receiver optical subassembly (ROSA) 404 that includes an AWG chip (200). *See* Ex. 1008, FIG. 4, ¶ [0043]; Ex. 1009, pp. 5, 7.

v. Claim 12: [12d] a first end for coupling to an optical coupling receptacle to receive an optical signal comprising a plurality of channel wavelengths, wherein the first end for coupling to the optical coupling receptacle includes an angled surface to reduce back reflections of an optical signal launched into the AWG chip;

171. Shen discloses an AWG chip (200) having a first end (230) for coupling to an optical fiber to receive an incoming optical signal comprising a plurality of channel wavelengths. *See* Ex. 1008, FIG. 4, ¶ [0043]; Ex. 1009, pp. 5, 7. As discussed *supra*, a POSITA would have understood that when coupling optical components, an angled physical junction should be used to reduce back-reflections. This concept was well-known in the optical communications field many years before the application for the '116 patent was filed, as typified by Lurie, Ex. 1006 and Tomita, Ex. 1007. *See supra*, Section XI.b.

172. Specifically, Lurie is directed to a method of polishing ferrules used in optical fiber connectors to provide angled physical contact between pairs of interconnected fibers. Ex. 1006, Abstract. As explained in the Background of the Invention of Lurie, “[t]he prior art further recognizes that signal transmission across

a connector may be improved by imparting an angled finish to the end face of the fibers. This construction results in reduced internal reflections of the signals at the end face.” Ex. 1006, 1:35-39.



Ex. 1006, FIG. 2 (annotated)

173. As further disclosed in the “Summary of the Invention” portion of Lurie, the desired angle of inclination of the abutting ends of the optical fibers is “usually about 8° .” See Ex. 1006, 3:16-18, 4:35-43, citing U.S. Patent No. 4,978,193 to Tomita, Ex. 1007.

174. Tomita describes that for coupling optical components, “An angle of inclination of the end face 22 relative to a plane 24 which is normal to the longitudinal axis [of the optical fiber] is preferably between 3° and 12° , more preferably between 5° and 10° , e.g. 8° , the precise angle to be used being governed by several design considerations, one of which is the minimum angle required so that substantially all reflected light from an end 28 of the fiber exceeds a critical acceptance angle of the fiber so that the reflected light is not guided by the fiber

core in a back reflection direction but is rather refracted into the fiber cladding and dissipated thereby.” *See* Ex. 1007, 2:58-68

175. As discussed *supra*, it is my opinion that knowledge that optical components should be joined using an angled junction was common knowledge in the field of optical communications decades before the application for the ’116 Patent was filed and would have been understood and implemented by a POSITA. Accordingly, a POSITA there would have had strong motivation to combine the angled junction of Lurie or Tomita (or depicted in Soldano) where the optical fiber meets the AWG of Shen. In my view, it would have been obvious in Shen to angle the surface where the PLC that couples to the optical fiber for the reasons described in Lurie and Tomita.

vi. Claim 12: [12e] a planar lightwave circuit (PLC) coupled to the first end configured to de-multiplex each channel wavelength of the plurality of channel wavelengths;

176. Shen discloses a PLC coupled at its first end (230) and configured to de-multiplex each channel wavelength of the plurality of channel wavelengths. *See* Ex. 1008, FIG. 3, ¶ [0043]; Ex. 1009, pp. 5, 8.

vii. Claim 12: [12f] a plurality of output waveguides coupled to the PLC, each of the output waveguides configured to receive light corresponding to an associated de-multiplexed channel wavelength launched from the PLC and provide the light along a first light path that extends towards a second end of the AWG chip; and

177. In my opinion, Shen discloses a plurality of output waveguides (278)

coupled to the PLC configured to receive light corresponding to an associated demultiplexed channel wavelength launched from PLC and provide the light along a first light path towards a second end of the AWG chip. *See* Ex. 1008, FIGS. 1-3, ¶¶ [0038]-[0039], [0043]; Ex. 1009, pp. 6-8.

viii. Claim 12: [12g] a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an output interface region of the AWG chip;

178. Shen discloses a tapered region (409) at the second end of PLC of the AWG chip (200) to receive light via the plurality of output waveguides and reflect the light towards an output interface region of the AWG chip. *See* Ex. 1008, FIGS. 1-3, ¶¶ [0038]-[0039], [0043]; Ex. 1009, pp. 6-8.

ix. Claim 12: [12h] an array of detector devices disposed adjacent to the output interface region of the AWG chip; and

179. Shen has an array of photodetectors (300) disposed adjacent to the output interface region of the PLC to receive the separate channel wavelengths. *See* Ex. 1008, FIGS. 1-3, ¶¶ [0033]-[0037], [0043]; Ex. 1009, pp. 6-8.

x. Claim 12: [12i] a multi-channel transmitter optical assembly (TOSA) including at least one laser package located in the transceiver housing for transmitting optical signals at different channel wavelengths.

180. In my opinion, a POSITA would have understood that the AWG chip disclosed in Shen would be used in a transceiver module, such as disclosed in

Soldano, that includes a multi-channel transmitter optical assembly (TOSA) having at least one laser package located in the transceiver housing for transmitting signals at different channel wavelengths. *See* Ex. 1005, FIGS. 3-5, 7:37-51, 8:20-28, 8:54-60, 9:10-15.

181. For the foregoing reasons, it is my opinion that a POSITA would have been readily aware that an angled junction should be used where the optical input fiber is coupled to the AWG of Shen, as taught decades earlier in Lurie and Tomita, thus rendering Claim 12 obvious.

xi. Claim 13: The optical transceiver module of claim 12, wherein the output interface region of the AWG chip is an exposed region adjacent an air gap, and wherein the air gap separates the output interface region of the AWG chip and the array of detector devices.

182. In my opinion, Shen necessarily discloses that an air gap exists between the output interface region of the PLC and photodetectors (300), for example, as a result of affixing the AWG chip to the substrate (100) via the bonding pads (110). *See* Ex. 1008, FIG. 1, ¶ [0043]; Ex. 1009, pp. 6, 8. For the device of Claim 12, *see supra*, Sections X.d.ii-x.

183. Accordingly, a POSITA would have understood that Shen in combination with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 13 obvious.

xii. Claim 14: The optical transceiver module of claim 12, wherein the output interface region of the AWG chip is separated from the array of detector devices by about 50 microns.

184. It is my opinion that a POSITA would have understood the benefit of not having the AWG chip (200) in intimate contact with the underlying photodetector array (300). *See* Ex. 1008, FIG. 1, ¶ [0043]; Ex. 1009, pp. 6, 8; Ex. 1001, 10:14-17. For example, a POSITA would readily recognize the benefits of providing an offset between these structures to accommodate thermal expansion. I am therefore of the opinion that it would have been a simple design choice to leave an air gap of 50 microns between the PLC and the photodetectors, especially as I could find no specific advantage attributed to this feature in the '116 Patent. *See* Ex. 1001, 10:14-17. For the device of Claim 12, *see supra*, Sections X.d.ii-x.

185. Thus, a POSITA would have understood that Shen in combination with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 14 obvious.

xiii. Claim 15: The optical transceiver module of claim 12, wherein the AWG chip defines a plurality of sidewalls extending longitudinally from the first end to the second end, and wherein the tapered region of the second end defines an angled surface that extends from a first sidewall of the plurality of sidewalls to a second sidewall of the plurality of sidewalls.

186. Shen discloses AWG chip (200) that defines a plurality of sidewalls extending longitudinally from the first end (230) to the second end, wherein a

tapered region of the second end defines an angled end (409) that extends from a first sidewall of the plurality of sidewalls to a second sidewall of the plurality of sidewalls. *See* Ex. 1008, FIGS. 1-2, ¶¶ [0038]-[0041]; Ex. 1009, pp. 6-8. For the device of Claim 12, *see supra*, Sections X.d.ii-x.

187. Thus, a POSITA would have understood that Shen in combination with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 15 obvious.

xiv. Claim 16: The optical transceiver module of claim 15, wherein the angled surface has an interior angle of about 41 to 45 degrees relative to the output interface region.

188. Shen discloses that the AWG chip (200) has an angled end (400) that redirects light from a horizontal orientation in the channel wavelength waveguides (278) to vertical orientation exiting the PLC, wherein the reflector angle is 40° to 50°, which encompasses the claimed range of 41 to 45 degrees relative to the output interface region. *See* Ex. 1008, FIGS. 1-2, ¶¶ [0038]-[0041]; Ex. 1009, pp. 6-8. For the device of Claim 15, *see supra*, Section X.d.xiii.

189. Thus, a POSITA would have understood that Shen in combination with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 16 obvious.

xv. Claim 17: The optical transceiver module of claim 15, wherein each of the output waveguides comprise a core material, and wherein a cladding material is disposed on the core material, the core material defining at least a portion of the plurality of sidewalls of the AWG chip.

190. Shen discloses that the output waveguides (278) of the AWG chip (200) comprise a core material (270) and include a cladding material (250), (260) disposed on the core material (270), such that the core material defines at least a portion of the first and second sidewalls. *See* Ex. 1008, FIG. 2, ¶¶ [0041]-[0042]; Ex. 1009, pp. 6-8. For the device of Claim 15, *see supra*, Section X.d.xiii.

191. Thus, a POSITA would have understood that Shen in combination with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 17 obvious.

xvi. Claim 18: The optical transceiver module of claim 17, wherein the core material of each of the plurality of output waveguides provide a portion of the angled surface, and wherein the angled surface is configured to reflect incident light based on at least an interior angle of the angled surface relative to the output interface of the AWG chip.

192. Shen discloses that the core material (270) provides a portion of the angled end (400) and that the angled end is configured to reflect light based at least on the interior angle of the angled surface relative to the output interface of the AWG chip. *See* Ex. 1008, FIGS. 1-2, ¶¶ [0038]-[0041]; Ex. 1009, pp. 6-8. For the device of Claim 17, *see supra*, Section X.d.xv.

193. Accordingly, a POSITA would have understood that Shen in combination with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 18 obvious.

xvii. Claim 19: The optical transceiver of claim 12, wherein the transceiver is a Small Form-factor Pluggable (SFP) transceiver module and the ROSA is configured to receive at least four different channel wavelengths at transmission rates of at least about 25 Gbps per channel.

194. It is my opinion that a POSITA would have understood that the AWG chip (200) described in Shen typically would be used in any available module format that existed circa 2016 when the application for the '116 patent was filed, e.g., SFF Committee Specification SFF - 8665 for QSFP + 28 Gb/s. 4x Pluggable Transceiver Solution (QSFP28) published May 10, 2013, which specified at least four different channel wavelengths of 25 Gbps per channel. *See* Ex. 1001, 5:35-41. For the device of Claim 12, *see supra*, Sections X.d.ii-x.

195. Thus, a POSITA would have understood that Shen in combination with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 19 obvious.

i. Motivation To Combine Kanazawa with Sasaki.

Figure 1 consists of two schematic diagrams, (a) and (b), illustrating the proposed demultiplexer. Diagram (a) is a top view showing a multi-channel optical receiver (10) with gold bumps (11) and photodetectors (12) on a substrate (14). The receiver is connected to a demultiplexer (16) via a demux integrated SOA array (14). The receiver also includes semiconductor optical amplifiers (13) and 45-degree mirrors (15). Diagram (b) is a cross-sectional view showing the multi-channel optical receiver (10) with gold bumps (11) and photodetectors (12) on a substrate (14). The receiver is connected to a demultiplexer (16) via a demux integrated SOA array (14). The receiver also includes semiconductor optical amplifiers (13) and 45-degree mirrors (15).

Legend:

- 10 Multi-channel optical receiver
- 11 Gold bump
- 12 Photodetector
- 13 Semiconductor Optical Amplifier
- 14 Demux integrated SOA array
- 15 45-degree mirror
- 16 Demultiplexer

Exs. 1010, 1011 (annotated)

IPR2025-00435, Exhibit 1003

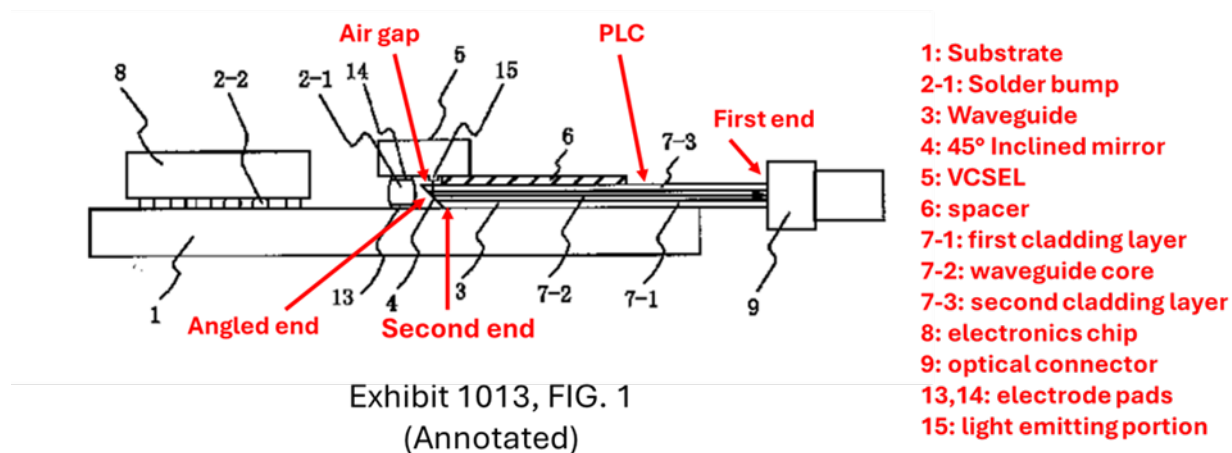


Exhibit 1013, FIG. 1
 (Annotated)

198. Both Kanazawa and Sasaki disclose structures for use in optical transceiver modules. Sasaki describes a PLC having an angled end for orthogonally redirecting light into or out of an adjacent waveguide carrying four separate wavelength optical signals. Kanazawa describes mirrors for redirecting separate optical wavelength signals coming from, or heading towards, an AWG that serves to de-multiplex (or multiplex) the signals. Both Kanazawa and Sasaki relate to the same field of endeavor, optical communications, and both are directed to increasing the density of the carried signals and compactness of the photonics module. Accordingly, in my opinion a POSITA would have been motivated to use the angled end of the PLC of Sasaki in the AWG device of Kanazawa to increase both signal density and compactness of a photonics module, while also employing the AWG structure of Kanazawa to implement both ROSA and TOSA functionalities.

ii. **Claim 1: [1a] An arrayed waveguide grating (AWG) chip comprising:**

199. Kanazawa discloses a multichannel optical receiver having an arrayed waveguide grating (AWG) chip (14) for demultiplexing an input light beam into multiple light beams (16), the number of which is the same as that of the channels. *See* Ex. 1010, FIG. 1; Ex. 1011, Abstract, ¶¶ [0001]-[0003], [0006], [0015]-[0018], [0022].

iii. Claim 1: [1b] a first end for coupling to an optical coupling receptacle to receive an optical signal comprising a plurality of channel wavelengths;

200. Kanazawa discloses the AWG chip (14) has a first end configured for coupling to an optical fiber to receive an input optical signal including a plurality of channel wavelengths. *See* Ex. 1010, FIG. 1; Ex. 1011, ¶¶ [0016]-[0018].

iv. Claim 1: [1c] a substrate;

201. Based on my understanding as to how the Patent Owner has construed the term “substrate” for purposes of alleging infringement in the pending litigation, Kanazawa discloses that the AWG chip (14) is disposed adjacent to a photodetector array (12) disposed on a substrate. *See* Ex. 1010, FIG. 1; Ex. 1011, ¶ [0017].

v. Claim 1: [1d] a planar lightwave circuit (PLC) disposed on the substrate, the PLC coupled to the first end and configured to demultiplex each channel wavelength of the plurality of channel wavelengths;

202. Kanazawa discloses that the AWG chip (14), which is a planar lightwave circuit (PLC), is disposed adjacent to the photodetector array 12. The

PLC is coupled to the first end and is designed to de-multiplex (16) an input multi-wavelength optical signal into a discrete plurality of channel wavelengths. *See* Ex. 1010, FIG. 1; Ex. 1011, Abstract, ¶¶ [0016]-[0018].

vi. Claim 1: [1e] a plurality of output waveguides coupled to the PLC, each of the output waveguides configured to receive light corresponding to an associated de-multiplexed channel wavelength launched from the PLC and provide the light along a first light path that extends towards a second end of the AWG chip; and

203. In my opinion, Kanazawa discloses a plurality of output waveguides (13) are coupled to the demultiplexer (16) of the PLC, with each of the output waveguides (13) designed to transmit light of a channel wavelength launched from PLC along first light path that extends towards second end of the AWG chip. *See* Ex. 1010, FIG. 1; Ex. 1011, Abstract, ¶¶ [0016]-[0017].

vii. Claim 1: [1f] a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an exposed output interface region of the AWG chip, wherein the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate.

204. Kanazawa discloses mirrors (15) angled at 45 degrees embedded in the AWG chip (14), at the output ends of the plurality of individual channel wavelength waveguides (13), to redirect light to the photodetector array (12). *See* Ex. 1010, FIG. 1; Ex. 1011, ¶¶ [0016], [0018]. Sasaki describes a PLC having an angled end (4) for redirecting light between a plurality of horizontal channel

wavelength waveguides (7-2) and vertically to photodetectors or light-emitting diodes (5, 15). *See* Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0017]-[0018], [0024]-[0025], [0052].

205. In my opinion, as discussed *supra*, a POSITA would have been motivated to substitute the angled end of Sasaki for the angled mirrors (15) embedded in the PLC of Kanazawa to simplify construction thereof. In this manner, configuring the second end of the AWG chip of Kanazawa to have an angled end, as taught in Sasaki, would result in directing light exiting the plurality of output waveguides towards adjacent photodetector array (12) without passing the received light through the substrate.

206. Both Kanazawa and Sasaki are directed to the field of reducing the size of photonics modules, simplifying assembly, and improving alignment accuracy. In my opinion such benefits would have been readily apparent to a POSITA making the optical receiver disclosed in Kanazawa and motivated the combination of the teachings of Kanazawa and Sasaki. Thus, in my opinion, a POSITA would have understood that Kanazawa in combination with Sasaki renders Claim 1 obvious.

viii. Claim 2: The AWG chip of claim 1, wherein the exposed output interface region is configured to pass the reflected light received via the plurality of output waveguides out of the AWG chip along a second light path that is substantially orthogonal to the first light path.

207. Sasaki discloses that the output interface region of the PLC is configured to pass reflected light received via the plurality of waveguides along a path that is substantially orthogonal to the first light path. *See* Ex. 1012, FIG. 1; Ex. 1013, Abstract, ¶¶ [0023]-[0026], [0052]. In my opinion, a POSITA would have been motivated to combine the angled end of Sasaki in the AWG chip of Kanazawa for the resulting increase in signal density, module compactness, and simplicity of manufacture and assembly. For the device of Claim 1, *see supra*, Sections X.e.ii-vii.

208. Accordingly, in my opinion, a POSITA would have understood that Kanazawa in combination with Sasaki renders Claim 2 obvious.

ix. Claim 3: The AWG chip of claim 1, wherein the AWG chip defines a plurality of sidewalls extending longitudinally from the first end to the second end, and wherein the tapered region of the second end defines an angled surface that extends from a first sidewall of the plurality of sidewalls to a second sidewall of the plurality of sidewalls.

209. Sasaki discloses that the PLC defines a plurality of sidewalls extending longitudinally from first end to second end, wherein a tapered region of the second end defines an angled surface (4) that extends from a first sidewall of the plurality of sidewalls to a second sidewall of the plurality of sidewalls. *See* Ex. 1012, FIG.

1; Ex. 1013, ¶¶ [0019], [0023]-[0026], [0052]. In my view, a POSITA would have been motivated to combine the angled end configuration (4) of Sasaki in the AWG chip of Kanazawa to obtain the resulting increase in signal density, module compactness, and for simplicity of manufacture and assembly. For the device of Claim 1, *see supra*, Sections X.e.ii-vii.

210. Accordingly, in my opinion, a POSITA would have understood that Kanazawa in combination with Sasaki renders Claim 3 obvious.

x. Claim 4: The AWG chip of claim 3, wherein the angled surface has an interior angle of about 41 to 45 degrees relative to the exposed output interface region.

211. It is my opinion that Sasaki discloses that the PLC has an angled 45-degree surface (4) that redirects light between horizontal orientation (in the channel wavelength waveguides) and vertical orientation (to/from the PLC), and further discloses that other angles such as 41 to 49 degrees relative to the output interface region may be desirable. *See* Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0025], [0052], [0057]. Accordingly, in my opinion a POSITA would have been motivated to combine such teachings of Sasaki in the AWG chip of Kanazawa for simplicity of manufacture and assembly. For the device of Claim 3, *see supra*, Section X.e.ix.

212. Thus, in my opinion, a POSITA would have understood that Kanazawa in combination with Sasaki renders Claim 4 obvious.

xi. Claim 5: The AWG chip of claim 3, wherein each of the output waveguides comprise a core material, and wherein a cladding material is disposed on the core material, the core material defining at least a portion of the plurality of sidewalls of the AWG chip.

213. Sasaki discloses that the output waveguides of the PLC comprise a core material (7-2) and include a cladding material (7-1, 7-3) disposed on the core material (7-2), such that the core material (7-2) defines at least a portion of the first and second sidewalls. *See* Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0023]-[0025], [0052], [0056]. In my opinion, a POSITA would have understood that optical waveguides generally employ a core sandwiched between cladding layers, and thus this configuration of Sasaki would be used in the AWG chip of Kanazawa. For the device of Claim 3, *see supra*, Section X.e.ix.

214. In my opinion, a POSITA would have understood that Kanazawa in combination with Sasaki renders Claim 5 obvious.

xii. Claim 6: The AWG chip of claim 5, wherein the core material of each of the plurality of output waveguides has a first index of refraction, and a medium external to and adjacent the tapered region has a second index of refraction, the first index of refraction being greater than the second index of refraction.

215. In my opinion, a POSITA would have understood that Sasaki discloses that the core material (7-2) of each of the plurality of waveguides has a first index of refraction (e.g., a siloxane polymer or glass with n generally above 1.5) and that the medium external (e.g., air, $n \sim 1.0$) to and adjacent to the tapered region has a

second of refraction, such that the first index of refraction is greater than the second index of refraction. *See* Ex. 1012, FIG. 1, Ex. 1013, Abstract ¶¶ [0023]-[0025], [0052], [0056]. In my opinion, a POSITA would have understood that these aspects of Sasaki were directly transferable to the AWG chip of Kanazawa. For the device of Claim 5, *see supra*, Section X.e.xi.

216. Accordingly, in my opinion, a POSITA would have understood that Kanazawa in combination with Sasaki renders Claim 6 obvious.

xiii. Claim 7: The AWG chip of claim 6, wherein the external medium comprises a material having an index of refraction of about 1.0.

217. It is my opinion that a POSITA would have understood that the AWG chip described in Kanazawa typically would be enclosed within a module containing air or an inert gas to prevent the accumulation of dust. A POSITA therefore would have understood the external medium adjacent to the tapered region of the AWG chip would be air or similar gas having an index of refraction of about 1.0. For the device of Claim 6, *see supra*, Section X.e.xii.

218. Thus, in my opinion, a POSITA would have understood that Kanazawa in combination with Sasaki renders Claim 7 obvious.

xiv. Claim 8: The AWG chip of claim 5, wherein the core material of each of the plurality of output waveguides provide a portion of the angled surface, and wherein the angled surface is configured to reflect incident light based on at least an interior angle of the angled surface.

219. In my opinion, Sasaki discloses that the core material (7-2) provides a portion of the angled surface that is configured to reflect light based at least on the interior angle of the angled surface. *See* Ex. 1012, FIG. 1; Ex. 1013, Abstract, ¶ [0025]. For the device of Claim 5, *see supra*, Section X.e.xi.

220. Accordingly, in my opinion, a POSITA would have understood that Kanazawa in combination with Sasaki renders Claim 8 obvious.

xv. Claim 9: The AWG chip of claim 5, wherein the core material comprises doped silica (SiO₂) having an index of refraction of about 1.45 to 1.50.

221. Sasaki discloses that the PLC may be made of a siloxane polymer, glass or other similar material used in waveguides. *See* Ex. 1012, FIG. 1; Ex. 1013, ¶ [0025]. Kanazawa generally describes that the AWG would be made from materials used to create optical waveguides. Accordingly, in my opinion, a POSITA would have understood that an AWG chip combining the teachings of Kanazawa and Sasaki should be made of a material which is commonly used in waveguides, such as doped fused silica, having n in the range of 1.45 and 1.5. For the device of Claim 5, *see supra*, Section X.e.xi.

222. Thus, in my opinion, a POSITA would have understood that Kanazawa in combination with Sasaki renders Claim 9 obvious.

xvi. Claim 10: The AWG chip of claim 1, wherein the AWG chip is configured as a 1×N demultiplexer device whereby a single optical input signal is de-multiplexed into N different channel

wavelengths.

223. Kanazawa discloses an AWG chip that having a 1xN demultiplexer, in which a single multi-wavelength optical input signal is demultiplexed into N different wavelengths, specifically 4 different wavelengths. *See* Ex. 1010, FIG. 1; Ex. 1011, ¶¶ [0006], [0015]-[0022]. Sasaki discloses a PLC that receives as its input four channel wavelengths. *See* Ex. 1012, FIG. 6; Ex. 1013, ¶ [0018]. In my opinion, a POSITA would have been motivated to combine the demultiplexer of Kanazawa with the PLC of Sasaki to reduce the four input channel waveguides of Sasaki to a single input multi-channel optical signal as in Kanazawa. For the device of Claim 1, *see supra*, Sections X.e.ii-vii.

224. In my opinion, a POSITA would have understood that Kanazawa in combination with Sasaki renders Claim 10 obvious.

xvii. Claim 11: The AWG chip of claim 1, wherein the AWG chip is implemented in an AWG device package.

225. Kanazawa discloses an AWG chip that is implemented in an AWG device package. *See* Ex. 1010, FIG. 1; Ex. 1011, Abstract, ¶¶ [0001]-[0003], [0005]-[0006], [0011]-[0012]. For the device of Claim 1, *see supra*, Sections X.e.ii-vii.

226. Accordingly, in my view, a POSITA would have understood that Kanazawa in combination with Sasaki renders Claim 11 obvious.

f. Ground 6: Claims 12-19 Are Unpatentable As Obvious Over Kanazawa In View Of Sasaki And Further In View Of Lurie Or Tomita.

i. Motivation To Combine Kanazawa and Sasaki further in view of Lurie or Tomita

227. My opinion discussing the motivation for a POSITA to combine the teachings of Kanazawa and Sasaki are described *supra* at Section X.e.i. In addition, of relevance to Claim 12 of the '116 Patent, Sasaki teaches that, when coupling a semiconductor optical component to a waveguide via a mirror, it is preferable to tilt the mirror about 8 degrees to prevent back reflection along the same optical path as the incident light. Ex. 1013, ¶ [0057].

228. It is further my opinion, as set forth, *supra*, that when coupling an incoming optical fiber such as in Kanazawa to an AWG, a POSITA would have employed an angled junction to reduce reflections, as taught by Lurie and Tomita decades earlier. Because Lurie and Tomita also both are directed to the same field of optical communications as Kanazawa and Sasaki, it is my opinion that the common knowledge of using angled junctions for connection of optical fibers to other optical components, would have been known to and implemented by a POSITA in implementing the structure described in Kanazawa.

ii. Claim 12: [12a] An optical transceiver module comprising.

229. As discussed above for Claim 1, Kanazawa discloses a multichannel optical receiver having an arrayed waveguide grating (AWG) chip (14) for

demultiplexing an input light beam into multiple light beams, the number of which is the same as that of the channels. *See* Ex. 1010, FIG. 1; Ex. 1011, Abstract, ¶¶ [0001]-[0003], [0006], [0015]-[0018], [0022].

iii. Claim 12: [12b] a transceiver housing;

230. In my opinion, a POSITA would have understood that the AWG chip (14) disclosed in Kanazawa would be embodied in a transceiver housing configured in accordance with a relevant photonics module specification prescribed at the time the Kanazawa patent application was filed, e.g., SFF Committee Specification SFF - 8665 for QSFP + 28 Gb/s. 4x Pluggable Transceiver Solution (QSFP28) published May 10, 2013. *See* Ex. 1001, 5:35-41; Ex. 1011, ¶ [0005].

iv. Claim 12: [12c] a multi-channel receiver optical sub-assembly (ROSA) located in the transceiver housing and including an arrayed waveguide grating (AWG) chip, the AWG chip comprising:

231. Kanazawa discloses a multi-channel receiver optical subassembly (ROSA) that includes the AWG chip (14). *See* Ex. 1010, FIG. 1; Ex. 1011, Abstract, ¶¶ [0005]-[0006], [0014]-[0022].

v. Claim 12: [12d] a first end for coupling to an optical coupling receptacle to receive an optical signal comprising a plurality of channel wavelengths, wherein the first end for coupling to the optical coupling receptacle includes an angled surface to reduce back reflections of an optical signal launched into the AWG chip;

232. Kanazawa discloses the AWG chip (14) has a first end for coupling to an optical fiber to receive an incoming optical signal comprising a plurality of

channel wavelengths. *See* Ex. 1010, FIG. 1; Ex. 1011, ¶¶ [0016]-[0018]. As discussed *supra*, Sasaki teaches that an 8-degree tilt should be used when coupling a waveguide to a semiconductor optical component to prevent back reflection. Moreover, a POSITA would have understood that it was common knowledge in the art to use an angled physical junction to reduce back-reflections when coupling optical components. This concept was well-known in the optical communications field many years before the application for the '116 patent was filed, as typified by U.S. Patent No. 5,351,327 to Lurie et al. (Ex. 1006) and U.S. Patent No. 4,978,193 to Tomita (Ex. 1007), discussed *supra*. *See* Exhibit 1006, 1:35-39, 3:16-18, 4:35-43; Ex. 1007, 2:58-68.

233. It is therefore my opinion that knowledge that optical components should be joined using an angled junction was common knowledge in the field of optical communications decades before the application for the '116 Patent was filed and such knowledge was possessed by POSITAs. A POSITA would have been motivated to combine the angled junction of Lurie or Tomita where the optical fiber meets the AWG of Kanazawa. Accordingly, in my view, it would have been obvious to angle the surface of the PLC of Kanazawa that couples to the optical fiber for the reasons described in Sasaki, Lurie and Tomita.

vi. Claim 12: [12e] a planar lightwave circuit (PLC) coupled to the first end configured to de-multiplex each channel wavelength of the plurality of channel wavelengths;

234. Kanazawa discloses a PLC coupled at its first end and configured to de-multiplex each channel wavelength of the plurality of channel wavelengths. *See* Ex. 1010, FIG. 1; Ex. 1011, Abstract, ¶¶ [0016]-[0018].

vii. Claim 12: [12f] a plurality of output waveguides coupled to the PLC, each of the output waveguides configured to receive light corresponding to an associated de-multiplexed channel wavelength launched from the PLC and provide the light along a first light path that extends towards a second end of the AWG chip; and

235. Kanazawa discloses a plurality of output waveguides (13) coupled to the demultiplexer (16) of the PLC. Each of the output waveguides (13) is configured to receive light of an associated de-multiplexed channel wavelength launched from PLC and provide the light along a first light path towards a second end of the AWG chip. *See* Ex. 1010, FIG. 1; Ex. 1011, Abstract, ¶¶ [0016]-[0017].

viii. Claim 12: [12g] a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an output interface region of the AWG chip;

236. Kanazawa discloses mirrors (15) angled at 45 degrees embedded in the AWG chip (14), at the output ends of the plurality of individual channel wavelength waveguides (13), to redirect light to the photodetector array (12). *See* Ex. 1010, FIG. 1; Ex. 1011, ¶¶ [0016], [0018]. Sasaki discloses a tapered region at the second end of a PLC to receive light via the plurality of output waveguides and reflect the light towards an output interface region of the PLC. *See* Ex. 1012, FIG.

1; Ex. 1013, ¶¶ [0017]-[0018], [0024]-[0025], [0052].

237. In my opinion, a POSITA would have been motivated to substitute the angled end of Sasaki for the angled mirrors (15) embedded in the PLC of Kanazawa to simplify construction thereof. In this manner, configuring the second end of the AWG chip of Kanazawa as an angled end, as taught in Sasaki, would direct light exiting the plurality of output waveguides towards adjacent photodetector array (12). Both Kanazawa and Sasaki are directed to the field of reducing the size of photonics modules, simplifying assembly, and improving alignment accuracy, which benefits would have been readily apparent to a POSITA making the optical receiver disclosed in Kanazawa.

ix. Claim 12: [12h] an array of detector devices disposed adjacent to the output interface region of the AWG chip; and

238. Kanazawa has an array of photodetectors (12) disposed adjacent to the output interface region of the PLC to receive the separate channel wavelengths. *See* Ex. 1010, FIG. 1; Ex. 1011, Abstract, ¶¶ [0016]-[0017].

x. Claim 12: [12i] a multi-channel transmitter optical assembly (TOSA) including at least one laser package located in the transceiver housing for transmitting optical signals at different channel wavelengths.

239. In my opinion, a POSITA would have understood that the AWG chip disclosed in Kanazawa would be used in a transceiver module and include a multi-channel transmitter optical assembly (TOSA) having at least one laser package

located in the transceiver housing for transmitting signals at different channel wavelengths, such as disclosed in Soldano. Ex. 1011, ¶¶ [0001], [0002]; *see also* Ex. 1005, FIGS. 3-5, 7:37-51, 8:20-28, 8:54-60, 9:10-15.

240. For the foregoing reasons, it is my opinion that a POSITA would have been readily aware that an angled junction should be used where the optical input fiber is coupled to the AWG of Kanazawa, as taught decades earlier in Lurie and Tomita, thus rendering Claim 12 obvious.

xi. Claim 13: The optical transceiver module of claim 12, wherein the output interface region of the AWG chip is an exposed region adjacent an air gap, and wherein the air gap separates the output interface region of the AWG chip and the array of detector devices.

241. Sasaki discloses that an air gap exists between the interface region of the PLC and the array of photodetectors (15), for example, as a result of affixing the AWG chip to the substrate (5) via solder bumps (2-1). *See* Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0010]-[0012], [0017]-[0018]. In my opinion, a POSITA would have understood and been motivated to use this feature of Sasaki in aligning and joining the PLC to the photodetector array (12) of Kanazawa. For the device of Claim 12, *see supra*, Sections X.f.ii-x.

242. Accordingly, a POSITA would have understood that the combination of Kanazawa and Sasaki, together with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 13 obvious.

xii. Claim 14: The optical transceiver module of claim 12, wherein the output interface region of the AWG chip is separated from the array of detector devices by about 50 microns.

243. It is my opinion that a POSITA would have understood that it would be a simple design choice to leave an air gap of 50 microns between the PLC of Sasaki and the adjacent photodetector array, as implemented for the AWG of Kanazawa. *See* Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0010]-[0012], [0017]-[0018]. Such an air gap between these structures would facilitate alignment and accommodate thermal expansion. I am therefore of the view that it would have been a simple design choice to leave an air gap of 50 microns between the AWG and the photodetectors, especially as I could find no specific advantage attributed to this distance in the '116 Patent. *See* Ex. 1001 at 10:14-17. For the device of Claim 12, *see supra*, Sections X.f.ii-x.

244. Thus, in my view a POSITA would have understood that the combination of Kanazawa and Sasaki, together with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 14 obvious.

xiii. Claim 15: The optical transceiver module of claim 12, wherein the AWG chip defines a plurality of sidewalls extending longitudinally from the first end to the second end, and wherein the tapered region of the second end defines an angled surface that extends from a first sidewall of the plurality of sidewalls to a second sidewall of the plurality of sidewalls.

245. Sasaki discloses the PLC defines a plurality of sidewalls extending

longitudinally from the first end to the second end of the PLC, wherein a tapered region of the second end defines an angled surface that extends from a first sidewall of the plurality of sidewalls to a second sidewall of the plurality of sidewalls. *See* Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0019], [0023]-[0026], [0052]. In my view, it would have been obvious to a POSITA to employ the angled end configuration of Sasaki in the AWG chip of Kanazawa to achieve increased signal density, module compactness, and for simplicity of manufacture and assembly. For the device of Claim 12, *see supra*, Section X.f.ii-x.

246. Accordingly, in my view, a POSITA would have understood that the combination of Kanazawa and Sasaki, together with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 15 obvious.

xiv. Claim 16: The optical transceiver module of claim 15, wherein the angled surface has an interior angle of about 41 to 45 degrees relative to the output interface region.

247. Sasaki discloses that the PLC has an angled 45-degree surface (4) that redirects light between horizontal orientation (in the channel wavelength waveguides) and vertical orientation (to/from the PLC), and further discloses that other angles such as 41 to 49 degrees relative to the output interface region may be desirable. *See* Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0025], [0052], [0057]. Accordingly, it is my opinion that a POSITA would have been motivated to combine such teachings of Sasaki in the AWG chip of Kanazawa to achieved the benefits

discussed *supra*. For the device of Claim 15, *see supra*, Section X.f.xiii.

248. Thus, a POSITA would have understood that the combination of Kanazawa and Sasaki, together with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 16 obvious.

xv. Claim 17: The optical transceiver module of claim 15, wherein each of the output waveguides comprise a core material, and wherein a cladding material is disposed on the core material, the core material defining at least a portion of the plurality of sidewalls of the AWG chip.

249. Sasaki discloses that the output waveguides of the PLC comprise a core material (7-2) and include a cladding material (7-1, 7-3) disposed on the core material, such that the core material (7-2) defines at least a portion of the first and second sidewalls. *See* Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0023]-[0025], [0052], [0056]. Accordingly, a POSITA would have understood that because optical waveguides generally employ a core sandwiched between cladding layers, this configuration of Sasaki would be used in the AWG chip of Kanazawa. For the device of Claim 15, *see supra*, Section X.f.xiii.

250. In my view, a POSITA would have understood that the combination of Kanazawa and Sasaki, together with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 17 obvious.

xvi. Claim 18: The optical transceiver module of claim 17, wherein the core material of each of the plurality of output waveguides provide a portion of the angled surface, and wherein the angled surface is configured to reflect incident light based on at least an interior angle of the angled surface relative to the output interface of the AWG chip.

251. Sasaki discloses that the core material (7-2) provides a portion of the angled surface and that the angled surface is configured to reflect light based at least on the interior angle of the angled surface relative to the output interface of the AWG chip. *See* Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0023]-[0025], [0052]. Accordingly, a POSITA would have been motivated to combine the teachings of Sasaki in the AWG chip of Kanazawa to obtain the benefits discussed *supra*. For the device of Claim 17, *see supra*, Section X.f.xv.

252. Accordingly, a POSITA would have understood that the combination of Kanazawa and Sasaki, together with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 18 obvious.

xvii. Claim 19: The optical transceiver of claim 12, wherein the transceiver is a Small Form-factor Pluggable (SFP) transceiver module and the ROSA is configured to receive at least four different channel wavelengths at transmission rates of at least about 25 Gbps per channel.

253. It is my opinion that a POSITA would have understood that the photonics structure disclosed in Kanazawa could be used in any available module format that existed circa 2016 when the application for the '116 patent was filed, e.g., SFF Committee Specification SFF - 8665 for QSFP + 28 Gb/s. 4x Pluggable

Transceiver Solution (QSFP28) published May 10, 2013. *See* Ex. 1001, 5:35-41.

For the device of Claim 12, *see supra*, Sections X.f.ii-x.

254. It is therefore my opinion that a POSITA would have understood that the combination of Kanazawa and Sasaki, together with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 19 obvious.

XI. Revision Or Supplementation

255. In this report, I have presented my opinions regarding the invalidity of the challenged claims of the '116 Patent based on the information available to me. My opinions are subject to change in view of opinions provided by the Patent Owner or its expert, or any additional information that I may receive. I reserve the right to supplement my opinions accordingly.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed January 14, 2025 at Montreal, Canada.



Dr. Andrew G. Kirk