

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CAMBRIDGE INDUSTRIES USA INC.,

Petitioner

v.

APPLIED OPTOELECTRONICS, INC.,

Patent Owner

Case: IPR2025-00435

U.S. Patent No. 10,042,116

**PETITION FOR *INTER PARTES* REVIEW UNDER 35 U.S.C. § 311-319
AND 37 C.F.R. § 42.104**

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Exhibit	Short Name	Description
Ex. 1001	'116 Patent	U.S. Patent No. 10,042,116
Ex. 1002	'116 File History	File History of U.S. Patent No. U.S. Patent No. 10,042,116
Ex. 1003	Kirk Declaration	Declaration of Dr. Andrew G. Kirk
Ex. 1004	Kirk CV	<i>Curriculum Vitae</i> of Dr. Kirk
Ex. 1005	Soldano	U.S. Patent No. 9,768,901
Ex. 1006	Lurie	U.S. Patent No. 5,351,327
Ex. 1007	Tomita	U.S. Patent No. 4,978,193
Ex. 1008	Shen	U.S. Patent Pub. No. US 2016/0349451
Ex. 1009	Shen provisional	U.S. Prov. Patent Appln. No. 62/166015
Ex. 1010	Kanazawa	Japanese Patent Pub. JP 2012-034314A
Ex. 1011	—	Kanazawa English translation
Ex. 1012	Sasaki	Japanese Patent Pub. JP 2003-215371A
Ex. 1013	—	Sasaki English translation
Ex. 1014	Claim Terms	Joint Claim Construction And Pre-Hearing Statement in <i>Applied Optoelectronics, Inc. v. Cambridge Industries USA, Inc.</i> , No. 3:24-cv-01010-JD (N.D. Cal.)
Ex. 1015	Scheduling Order	Scheduling Order dated August 7, 2024, in <i>Applied Optoelectronics, Inc. v. Cambridge Industries USA, Inc.</i> , No. 3:24-cv-01010-JD (N.D. Cal.)
Ex. 1016	Excerpt from Infringement Claim Charts	Excerpt from Patent Owner's L.R. 3-1 & 3-2 Disclosures, June 6, 2024, in <i>Applied Optoelectronics, Inc. v. Cambridge Industries USA, Inc.</i> , No. 3:24-cv-01010-JD (N.D. Cal.)

Cambridge Industries USA Inc. (“Petitioner”) petitions for *Inter Partes* Review (“IPR”) under 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42 of Claims 1-19 (“the Challenged Claims”) of U.S. Patent No. 10,042,116 (the “’116 Patent”). Petitioner requests cancellation of the Challenged Claims.

I. STANDING UNDER 37 C.F.R. § 42.104(a)

Petitioner certifies that the ’116 Patent is available for IPR, and that Petitioner is not barred or estopped from requesting IPR.

II. PAYMENT OF FEES

Petitioner authorizes Deposit Account No. 19-5029 to be charged for any applicable fees in connection with this submission.

III. OVERVIEW OF CHALLENGES AND RELIEF REQUESTED

Pursuant to 37 CFR § 42.22(a)(1) and 37 CFR § 42.104(b)(1)-(2), Petitioner requests cancellation of the Challenged Claims pursuant to the grounds below.

Ground 1: Claims 1-11 Are Unpatentable Under 35 U.S.C. § 102 as Anticipated by Soldano.

Ground 2: Claims 12-19 Are Unpatentable Under § 103 as Obvious over Soldano in View of Lurie or Tomita.

Ground 3: Claims 1-11 Are Unpatentable Under 35 U.S.C. § 102 as Anticipated by Shen.

Ground 4: Claims 12-19 Are Unpatentable Under § 103 as Obvious over Shen in View of Soldano and Further in View of Lurie or Tomita.

Ground 5: Claims 1-11 Are Unpatentable Under § 103 as Obvious over Kanazawa in view of Sasaki.

Ground 6: Claims 12-19 Are Unpatentable Under § 103 as Obvious over Kanazawa in View of Sasaki and Further in View of Lurie or Tomita.

IV. BACKGROUND

A. Overview of the '116 Patent

The '116 Patent is directed to an optical transceiver module in which an optical demultiplexer, in the form of an arrayed waveguide grating (“AWG”) is coupled to photodetectors by an angled end portion of the AWG. Ex. 1003, ¶ 39. Such arrangements, and the use thereof, were well-known to persons of skill in the art (POSITAs) of photonics module and planar light circuit (“PLC”) design at the time the application for the '116 Patent was filed. The references discussed herein demonstrate that the claimed inventions of the '116 Patent were well-known in the photonics industry many years earlier. Ex. 1003, ¶ 55.

The '116 Patent describes and claims an AWG chip (and photonics module containing same) having a first end that couples to an optical coupling receptacle to receive an optical signal comprised of multiple channel wavelengths, a substrate, a PLC disposed on the substrate, a plurality of output waveguides coupled to the PLC to each receive a demultiplexed channel wavelength from the PLC and a tapered region at a second end of the AWG chip to reflect light from

the plurality of output waveguides towards an output interface region of the AWG chip. Ex. 1001, 3:66-4:25. Claims 1-11 require that the output interface region emit light received from the AWG chip on the same side as the substrate without passing the received light through the substrate. *Id.*, 12:23-13:20; Ex. 1003, ¶¶ 40, 54. Claims 12-19 are directed to an optical transceiver including an AWG having a tapered end region at one end, and an angled surface at the other that joins to the optical coupling receptacle, thereby reducing back reflection along the input optical fiber. Ex. 1001, 3:58-65, 13:21-14:42; Ex. 1003, ¶ 55.

As demonstrated in this Petition, the '116 Patent merely describes standard applications of AWGs in optical transceivers. *Id.* Accordingly, the Board should institute review because there is a strong likelihood that Petitioner will prevail on at least one Challenged Claim.

B. Technical Background

Optical transceivers are fiber optical communications devices that include a receiver optical subassembly (“ROSA”) and a transmitter optical subassembly (“TOSA”). Ex. 1003, ¶¶ 43-45. The ROSA receives multiple channel wavelengths via an incoming optical fiber and demultiplexes those wavelengths into individual channels for conversion to electrical signals using photodetectors, so that the resulting electrical signals may be input to a digital processor. *Id.* The TOSA receives electrical signals output by the digital processor that are used to

drive lasers having multiple channel wavelengths, which then are combined for transmission using an outgoing optical fiber. An AWG may be used in a ROSA demultiplexing the inbound optical signal or in a TOSA for multiplexing the outbound optical signal. *Id.*

AWGs may be fabricated using planar lightwave circuit techniques, in which doped and undoped layers of silica are deposited on a substrate. For use as a demultiplexer in a ROSA, a grating portion separates out the individual channel wavelengths, which channel wavelengths then are guided to separate photodetectors for conversion to electrical signals. Ex. 1003, ¶¶ 51-52.

C. '116 Patent Prosecution History

Patent Owner filed Application No. 15/137,823 (the “’823 Application”) on April 25, 2016, which matured as the ’116 Patent, on August 7, 2018. Ex. 1001, cover. An Office action mailed June 7, 2017, imposed a restriction between claims 1-19, drawn to an AWG chip, and claim 20, drawn to a method of forming an AWG chip. Ex. 1002, pp. 110-114. A Response was filed August 7, 2017, electing claims 1-19 for examination and withdrawing claim 20. *Id.*, p. 104; Ex. 1003, ¶¶ 57-58.

On August 21, 2017, a Non-final office action was mailed, rejecting claims 1-11 as anticipated by Bai (U.S. Patent No. 7,532,783). Ex. 1002, pp. 82-85. Claims 12-19 were rejected as obvious over Dallesasse (U.S. Patent No. 7,941,053) in view of Bai or Welch et al. (U.S. 7,058,263). *Id.*, pp. 85-90. An Amendment

and Response was filed on January 29, 2018, in which independent claim 1 was amended to recite “a substrate,” that the planar lightwave circuit was “disposed on the substrate” and that “the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate.” *Id.*, p. 43. Claim 12 was amended to recite that the first end “included an angled surface to reduce back reflections of an optical signal launched into the AWG chip.” *Id.*, p. 45; Ex. 1003, ¶ 59.

A Notice of Allowance and Notice of Allowability were mailed June 4, 2018. Ex. 1002, pp. 7-13. The Notice of Allowability recites that claims 1-11 “are allowable because Bai (US Patent No. 7,532,783) fails to teach a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an exposed output interface region of the AWG chip, wherein the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate. *Id.*, p. 12. The Notice of Allowability also recites that claims 12-19 “are allowable because Dallesasse (US Patent No. 7,941,053) and Bai (US Patent No. 7,532,783) fails to teach a first end for coupling to an optical coupling receptacle to receive an optical signal comprising a plurality of channel wavelengths, wherein the first end for coupling to the optical coupling receptacle includes an angled surface to reduce back

reflections of an optical signal launched into the AWG chip.” *Id.*, pp. 12-13; Ex. 1003, ¶¶ 60-61.

The Issue Fee was paid on July 5, 2018. Ex. 1002, p. 2. The ’116 Patent issued on August 7, 2018. *Id.*, p. 1; Ex. 1003, ¶ 62.

D. Priority Date

The ’116 Patent does not claim the benefit of priority of any prior application and has an effective filing date of April 25, 2016.

E. Prior Decisions by District Courts and the Board

The ’116 Patent is currently asserted in a pending district court case in the Northern District of California: *Applied Optoelectronics, Inc. v. Cambridge Industries USA Inc.*, No. 3:24-cv-01010-JD. No dispositive judgments or claim construction orders have issued regarding the ’116 Patent. A claim construction hearing is currently set for April 10, 2025. Ex. 1015, p. 2. The dispositive motion deadline is currently set for January 28, 2026. *Id.* Jury selection is currently set for June 8, 2026. *Id.*

The ’116 Patent has not been the subject of prior decisions by the Board.

F. Claim Construction (37 C.F.R. § 42.104(b)(3))

The claims are construed herein “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b).” 37 C.F.R. § 42.100(b) (Nov. 13, 2018). Unless otherwise specified, the terms

should receive their respective plain and ordinary meaning as understood by a person of ordinary skill in the art under *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005).

In deciding this Petition, the Board may find it necessary to construe the terms “substrate” and “disposed on the substrate” as used in independent claim 1 of the ’116 Patent. Ex. 1003, ¶ 64. As described in the ’116 Patent, the claimed AWG is formed by sequentially depositing cladding and core layers on a silicon or other silicon-based substrate. *See, e.g.,* Ex. 1001, 502 in FIG. 5A, 3:35-38 (“the AWG device is formed on a substrate such as a silicon wafer or any other suitable substrate and may include depositing sequential layers of cladding and core material thereon”), 8:31-43; Ex. 1003, ¶ 64. As further described in the ’116 Patent, a portion of the substrate may be removed by cutting or etching to expose output interface region 517. Ex, 1001, FIG. 5A, 9:46-50; Ex. 1003, ¶ 65. This process step is employed so that the “output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate” as recited in claim 1 to distinguish over the prior art. Ex. 1002, pp. 43, 48-49; Ex. 1003, ¶ 65.

One possible construction of the term “substrate” of claim 1 is “a silicon or silicon-based” layer on which the cladding and core layers are deposited to form the PLC. Ex. 1001, 3:35-38, 8:31-43, Ex. 1003, ¶66. Petitioner submits that

consistent with this construction of “substrate,” the term “disposed on” in the second element of claim 1, which requires a “planar lightwave circuit (PLC) disposed on the substrate,” should be construed to mean that the PLC is deposited on the substrate during formation of the AWG chip, as described in the ’116 Patent specification. *Id.* Further, limiting the substrate to the material upon which the PLC is formed gives meaning to the final clause of claim 1, “without passing the received light through the substrate”—which limitation is described in the patent as etching or otherwise removing a portion of the substrate underlying the angled end face. Ex. 1001, FIG. 5A, 9:46-49 (“Formation of the AWG chip 503 can include removing a portion of the substrate generally indicated at 515 to expose the output interface region 517”). Ex. 1003, ¶ 66.

By contrast, in the pending litigation, Patent Owner has construed the term “substrate” in its infringement claim charts for both the accused products more broadly, arguing for a “plain and ordinary meaning” as “a supporting structure for an AWG device.” Ex. 1014, p. 4; Ex. 1003, ¶ 67. In the pending litigation, the Patent Owner variously has identified the substrate as: (1) slab of grey-colored material underneath the PLC (Exhibit 3); (2) the printed circuit board (“PCB”) to which the AWG is affixed (Exhibit 4); and (3) a glue layer used to affix the PLC to the PCB (Exhibit 5). *See* Ex. 1016, pp. 3, 4, 5, 10-11, 12-13, 14-15; Ex. 1003, ¶ 67.

As used in Patent Owner’s infringement claim charts, despite amending the claims to specifically identify the location of the “substrate” to distinguish over the prior art, Patent Owner urges a plain and ordinary meaning for substrate as “a supporting structure for an AWG device.” Ex. 1014, p. 4. This may be consistent with how district courts have construed the term “substrate” when it is *not* explicitly defined in the patent specification or prosecution history. *See, e.g., ShieldMark, Inc. v. Insite Solutions, LLC*, Case No. 1:12-CV-223, at *13 (N.D. Ohio Feb. 13, 2013); *Collins v. Western Digital Technologies, Inc.*, C.A. No. 2:09-cv-219-TJW, at *18 (E.D. Tex. Sep. 23, 2011). Patent Owner’s construction is improper in view of the prosecution history of the ’116 Patent.

However, because a claim term should have the same meaning for purposes of invalidity as for infringement, Petitioner and its expert adopt a plain and ordinary meaning for the term “substrate” in the unpatentability analyses presented herein. Ex. 1003, ¶ 68.

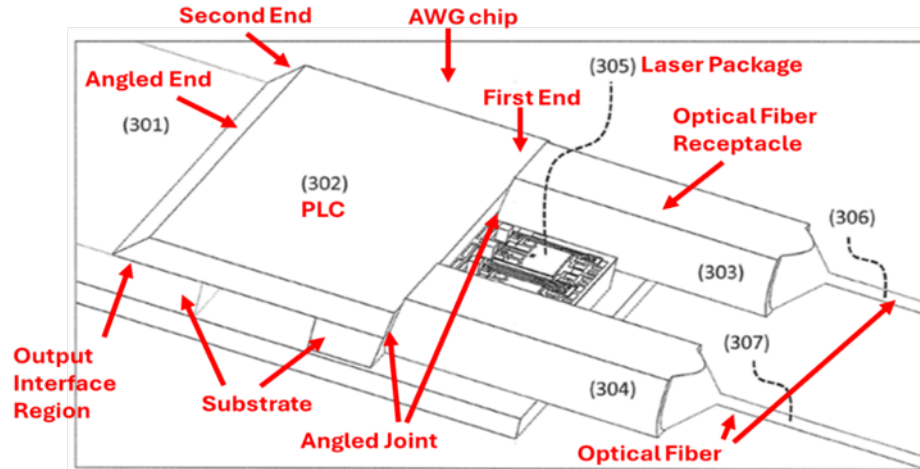
V. PRIOR ART REFERENCES

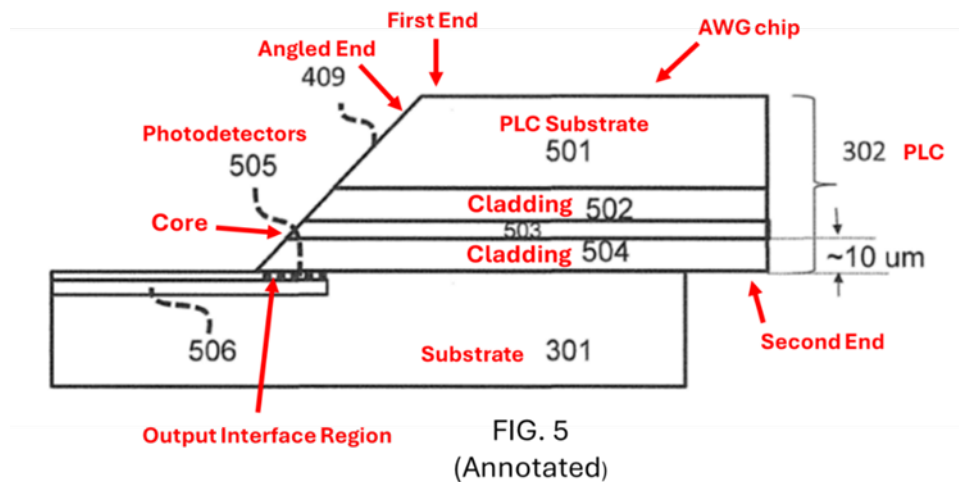
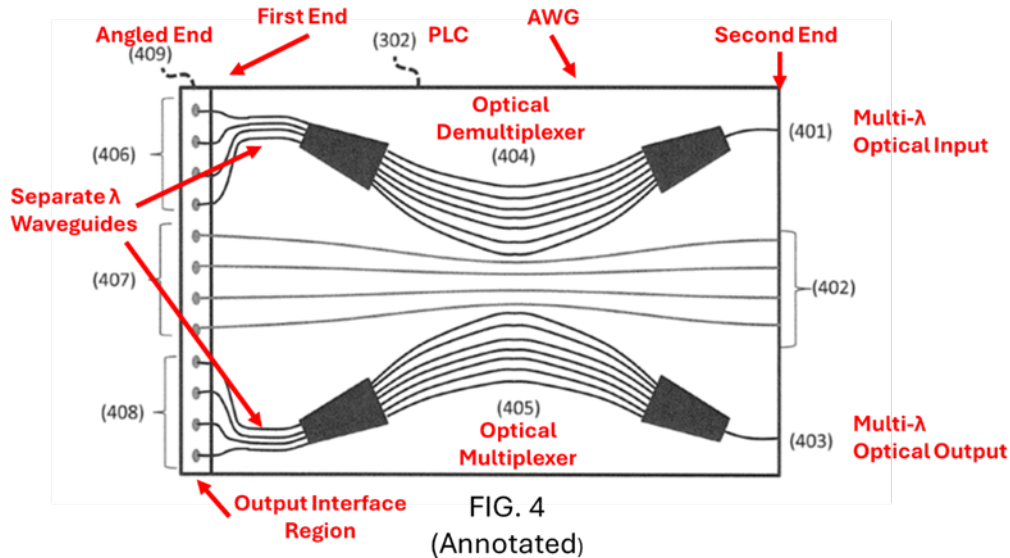
A. U.S. Patent No. 9,768,901 (“Soldano”), Exhibit 1005

Soldano was filed on February 12, 2015, and issued September 19, 2017, and claims priority to U.S. Provisional Patent Application 62/082,529, filed November 20, 2014. Ex. 1005, cover. Soldano qualifies as prior art under 35 U.S.C. § 102(a). Soldano was cited by the patentee in an Information Disclosure Statement (“IDS”)

filed simultaneously with patentee's last Amendment. Ex. 1002, p. 52. Soldano was not applied in a prior art rejection during prosecution of the '116 Patent. *Id.*; Ex. 1003, ¶ 69.

Soldano teaches a photonics module having a receiving optical subassembly ("ROSA") and a transmitter optical subassembly ("TOSA"), which uses an arrayed waveguide grating ("AWG") demultiplexer (404) for receiving a multi-wavelength optical input (401) and a plurality of output channel waveguides (406) of a planar light circuit ("PLC")(302) to transmit separate demultiplexed channel wavelengths to an array of photodetectors (505) using a polished angled end face (409) of the PLC. Ex. 1005, FIGS. 3-4, 7:63-8:24; Ex. 1003, ¶70.

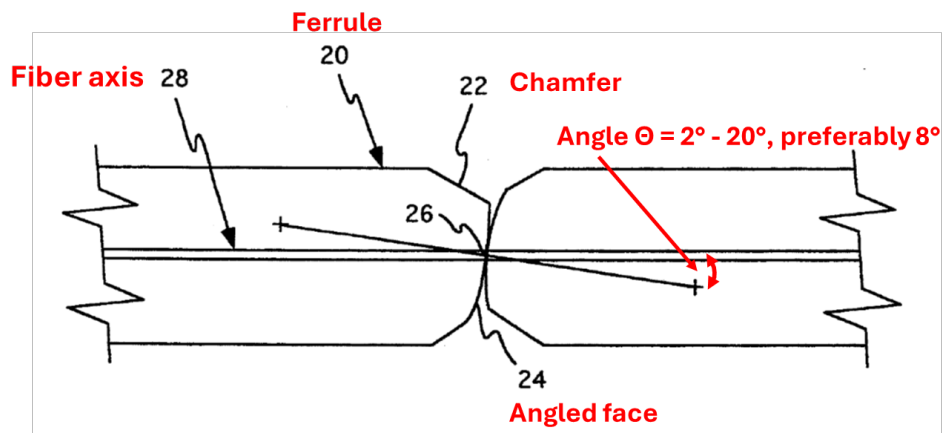




Soldano's PLC (302) includes a layer of core material (503) that extends between the first and second ends and includes a demultiplexer (404) for demultiplexing a multi-channel wavelength input optical signal (401) to four separate channel wavelength waveguides (406) which are redirected to the array of photodetectors (505). Ex. 1005, FIGS. 3-4, 7:63-8:24, 10:10-19; Ex. 1003, ¶ 70.

**B. U.S. Patent No. 5,351,327 (“Lurie et al.”), Exhibit 1006
U.S. Patent No. 4,978,193 (“Tomita”), Exhibit 1007**

Lurie et al. issued September 27, 1994, and is directed to a method of polishing ferrules used in optical fiber connectors to provide angled physical contact between pairs of interconnected fibers. Ex. 1006, Abstract. Lurie qualifies as prior art under 35 U.S.C. § 102(a). As explained in the Background of the Invention, “[t]he prior art further recognizes that signal transmission across a connector may be improved by imparting an angled finish to the end face of the fibers. This construction results in reduced internal reflections of the signals at the end face.” Ex. 1006, 1:35-39; Ex. 1003, ¶ 73.



Ex. 1006, FIG. 2 (annotated)

As further disclosed in the “Summary of the Invention” portion of Lurie, the desired angle of inclination of the abutting ends of the optical fibers is “usually about 8° .” See Ex. 1006, 3:16-18, 4:35-43, citing U.S. Patent No. 4,978,193 (Tomita, Ex. 1007; *see also* Ex. 1007, 2:58-68 (“An angle of inclination of the end face 22 relative to a plane 24 which is normal to the longitudinal axis [of the optical fiber] is

preferably between 3° and 12°, more preferably between 5° and 10°, e.g. 8°, the precise angle to be used being governed by several design considerations, one of which is the minimum angle required so that substantially all reflected light from an end 28 of the fiber exceeds a critical acceptance angle of the fiber so that the reflected light is not guided by the fiber core in a back reflection direction but is rather refracted into the fiber cladding and dissipated thereby.”); Ex. 1003, ¶ 74.

**C. U.S. Patent App. Pub. No. US 2016/0349451 (“Shen”), Exhibit 1008
U.S. Provisional Patent App. 62/166,015, Exhibit 1009**

Shen was filed on May 24, 2016, and published on December 1, 2016, claiming priority to U.S. provisional patent application 62/166,015, filed May 25, 2015 (Exhibit 1009). At least Figures 1-4 of Shen qualify as prior art under at least 35 U.S.C. § 102(a)(2). Shen was cited by the Patentee in its January 29, 2018, IDS, but was not applied in a rejection by the Examiner during prosecution of the ’116 Patent. Ex. 1003, ¶ 75.

Shen discloses an optical receiver module having an AWG chip (200) mounted on a substrate (100), in which a multi-wavelength light is demultiplexed and the resulting individual channel wavelengths transit corresponding waveguides and are redirected to photodetectors (300) by an angled surface end (400). Ex. 1008, Abstract, FIGS. 1-3; Ex. 1009, pp. 5-8; Ex. 1003, ¶ 76.

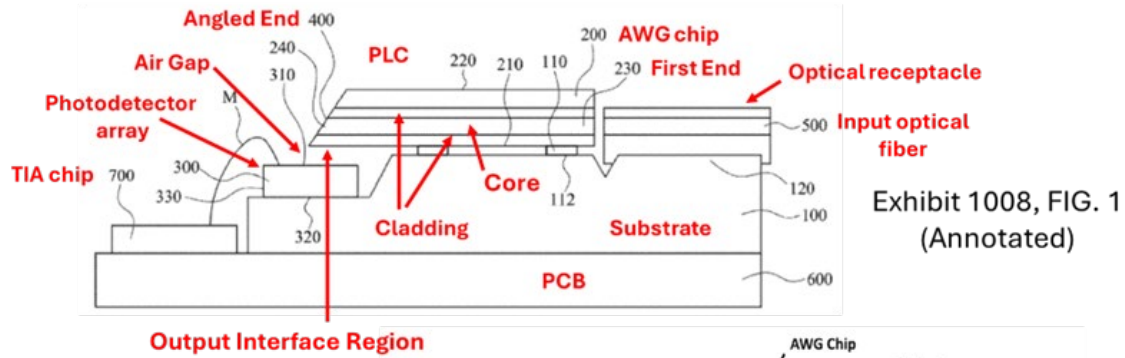
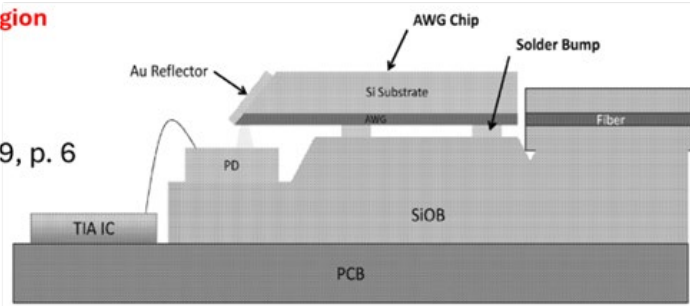
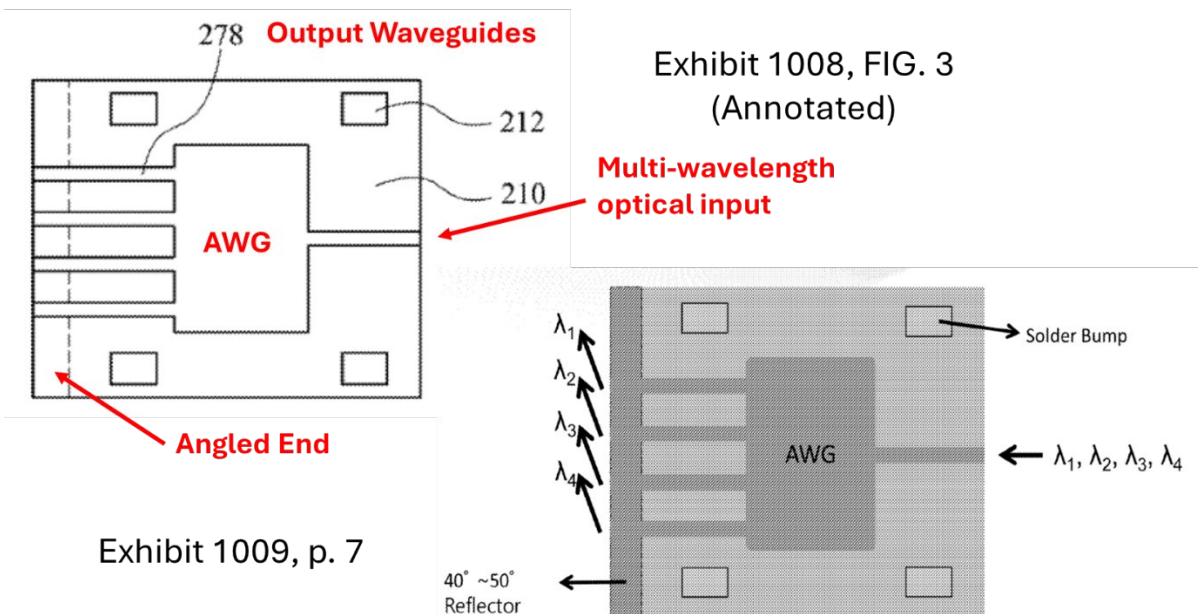


Exhibit 1009, p. 6



Shen discloses that the input multi-wavelength optical input signal is demultiplexed by the AWG and transmitted via separate channel wavelength waveguides (278) to the angled end (400), where the light is directed to the photodetector array (300). Ex. 1008, FIG. 3, ¶ [0043]; Ex. 1003, ¶ 77.



D. Japanese Patent Pub. JP 2012-034314A (“Kanazawa”) (Exhibit 1010) and Exhibit 1011 (English translation).

Kanazawa was filed on August 3, 2010, and published on April 2, 2014.

Kanazawa is prior art under at least 35 U.S.C. § 102(a)(1). Ex. 1003, ¶ 78.

Kanazawa teaches a multi-channel optical receiver including a planar light circuit (PLC) 14 including a demultiplexer (16) for splitting a multiwavelength input signal into multiple channel wavelengths, which are then transmitted along corresponding waveguides (13) to 45-degree mirrors (15) that redirect the channel wavelengths onto photodetectors (12) for conversion to electrical signals. *See* Exs. 1010, FIGS. 1(a), 1(b) (reproduced below); Ex. 1011, Abstract; ¶¶ [0006]-[0007]; Ex. 1003, ¶ 79.

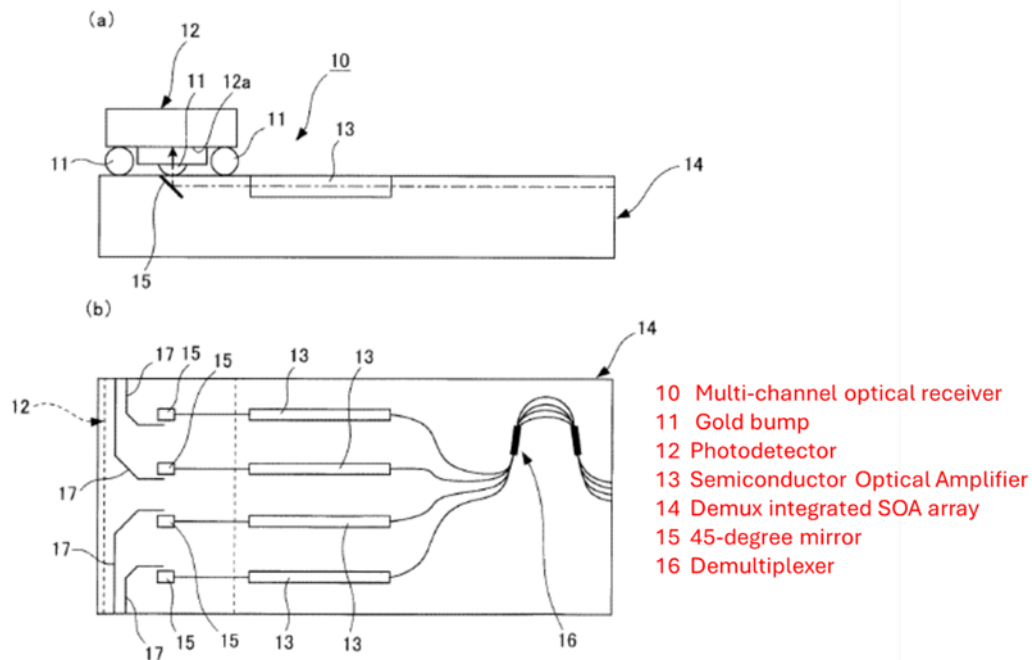
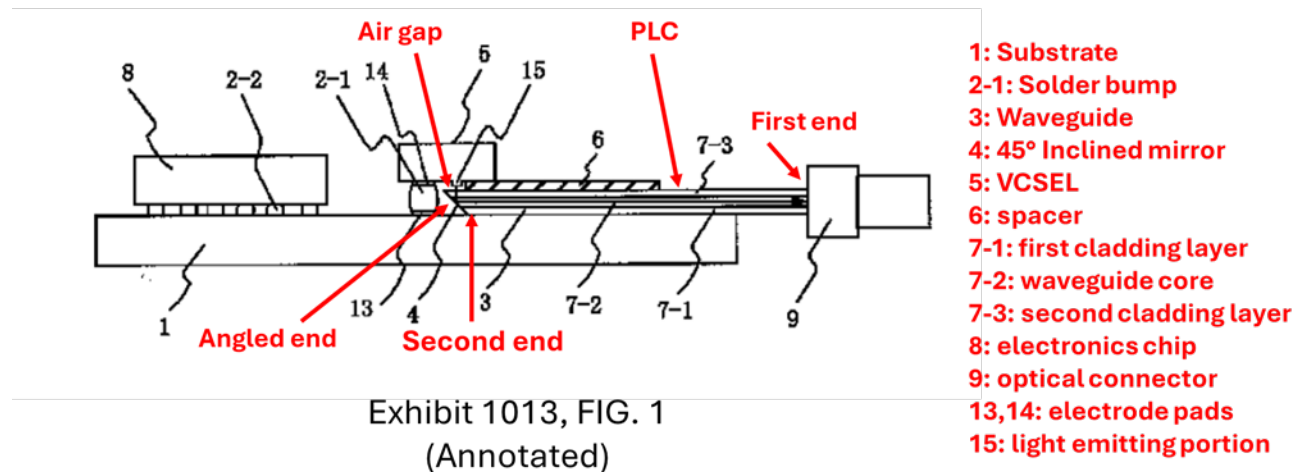


Exhibit 1010, FIGS. 1(a) and 1(b)

E. Japanese Patent App. Pub. JP 2003-215371A (“Sasaki”), Exhibit 1012; Exhibit 1013 (English translation).

Sasaki was filed on January 25, 2002, and published on July 30, 2003. Sasaki qualifies as prior art under at least 35 U.S.C. §102(a)(1). Ex. 1003, ¶ 81.

Sasaki discloses combination of a surface-type optical element (VCSEL or photodetector 15) and a planar light circuit (PLC) for use in a photonics module having a plurality of channel wavelength waveguides (3), wherein the PLC has an angled end (4) that redirects light from a light emitting unit to a channel waveguide (7-2) or from a channel waveguide (7-2) to a VCSEL or photodetector (15). Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0018], [0023], [0032], [0042]; Ex. 1003, ¶ 82.



Sasaki further discloses that the light emitting unit/photodiode (15) and optical waveguides (7-2) are aligned so as to be optically coupled to each other via the angled end (mirror 4) across an air gap. Ex. 1012, FIG. 1; Ex. 1013, Abstract, ¶ [0017]; Ex. 1003, ¶ 83.

VI. LEVEL OF SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) knowledgeable of the technical field of the ’116 Patent would have had at least (1) an undergraduate degree in electrical engineering, computer engineering, networking, or a comparable field of study and (2) at least two years of experience with optical data communications or a comparable field of work. Exhibit 1003, ¶¶ 22-23. Individuals with different education and additional experience also could be of ordinary skill in the art if that experience compensates for a deficit in their educational training as mentioned above. *Id.* Additional education might substitute for some experience, and vice versa.

VII. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Ground 1: Claims 1-11 Are Unpatentable Under 35 U.S.C. § 102 as Anticipated by Soldano.

Claim 1

[1a] Soldano discloses an arrayed waveguide grating AWG chip. *See* Ex. 1005, FIGS. 3-5; 7:62-8:28. Ex. 1003, ¶ 84.

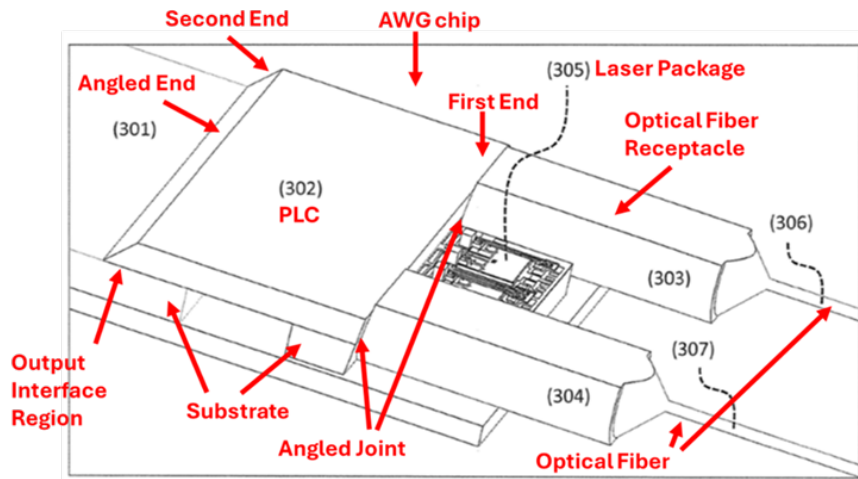
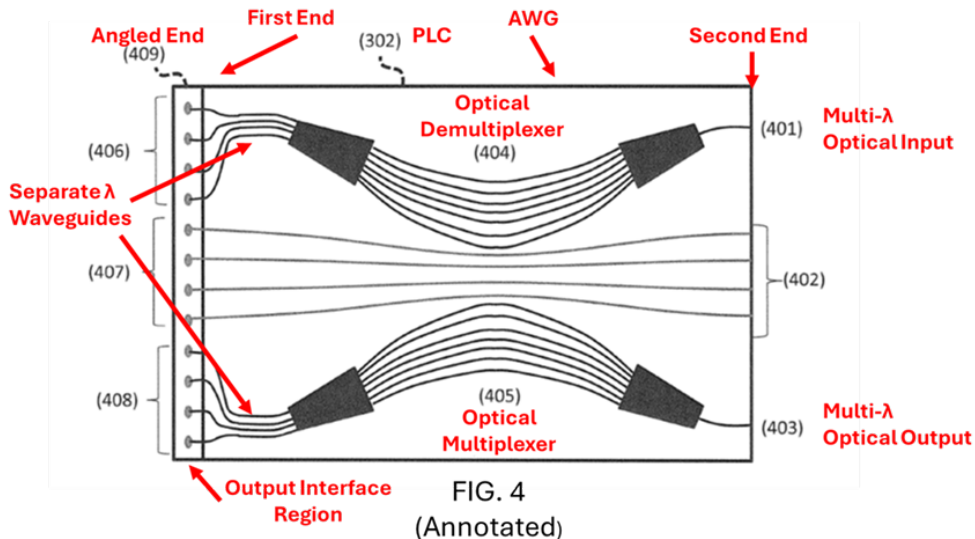


FIG. 3
(Annotated)

[1b] Soldano discloses the AWG chip has a first end for coupling to an optical coupling receptacle (303) to receive an optical signal including a plurality of channel wavelengths. *See* Ex. 1005, FIGS. 3-5; 7:62–8:8, 8:61–9:23; Ex. 1003, ¶ 85.

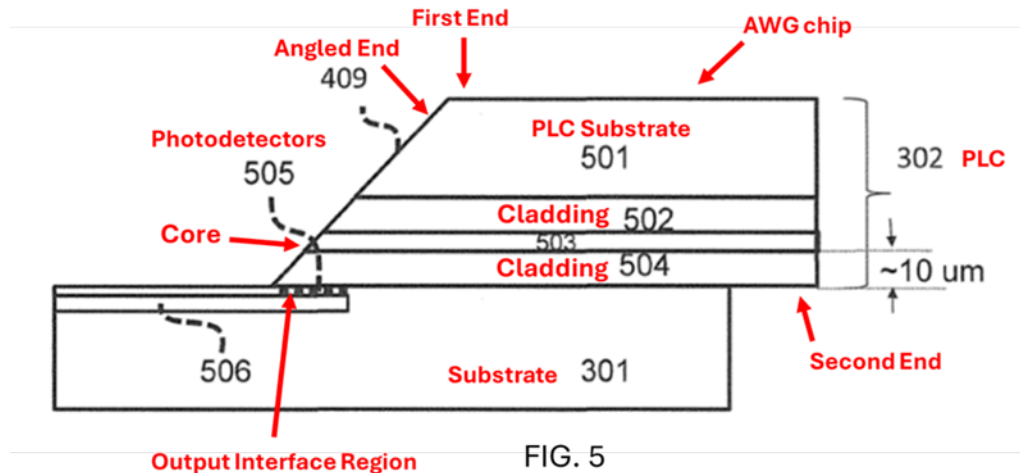
[1c] As construed by Patentee, Soldano discloses that the AWG chip is supported atop the silicon photonics chip (301), which serves as a substrate. *See* Ex. 1005, FIG. 5, 8:62-9:10, 9:53-55; Ex. 1003, ¶ 86.

[1d] Soldano discloses a planar lightwave circuit (PLC) (302) is disposed on the substrate (303). The PLC (302) is coupled to first end and is designed to de-multiplex the incoming multi-wavelength optical signal (401) into a discrete plurality of channel wavelengths. *See* Ex. 1005, FIGS. 3-5, 4:15-39, 7:62-8:8, 8:61-9:10; Ex. 1003, ¶ 87.



[1e] Soldano discloses a plurality of output waveguides are coupled to the PLC, each of the output waveguides designed to transmit light of a channel wavelength launched from PLC along a first light path that extends towards the second end (409) of the AWG chip. *See* Ex. 1005, FIGS. 3-5, 8:61-9:23; Ex. 1003, ¶ 88.

[1f] Soldano discloses a tapered region (409) is located at second end of the AWG chip, which receives light via the plurality of output waveguides and reflects the light towards exposed output interface region of the AWG chip, such that exposed output interface region emits received light from the AWG chip on the same side as the substrate (301) without passing the received light through the substrate. *See* Ex. 1005, FIGS. 4, 5, 9:52-10:25; Ex. 1003, ¶ 89.



Claim 2

Soldano discloses that the exposed output interface region is configured to pass reflected light received via the plurality of waveguides (503) out of the AWG chip along a path that is substantially orthogonal to the first light path. *See* Ex. 1005, FIG. 5, 3:17-24, 9-52-10:17; Ex. 1003, ¶¶ 90-91.

Claim 3

Soldano discloses AWG chip defines a plurality of sidewalls extending longitudinally from first end to second end, wherein a tapered region (409) of the second end defines an angled surface that extends from a first sidewall of the plurality of sidewalls to a second sidewall of the plurality of sidewalls. *See* Ex. 1005, FIGS. 4, 5, 9:23-37; Ex. 1003, ¶¶ 92-93.

Claim 4

Soldano discloses that the AWG chip has an angled polish surface that

redirects light from a horizontal orientation in the channel wavelength waveguides to vertical orientation exiting the PLC, which necessarily requires an angle within the claimed range of 41 to 45 degrees relative to the exposed output interface region. *See* Ex. 1005, FIGS. 4-5, 9:23-37; Ex. 1003, ¶¶ 94-95.

Claim 5

Soldano discloses that the output waveguides of the AWG chip comprise a core material (503) and include a cladding material (502), (504) disposed on the core material (503), such that the core material (503) defines at least a portion of the first and second sidewalls. *See* Ex. 1005, FIGS. 4-5, 9:56-66; Ex. 1003, ¶¶ 96-97.

Claim 6

Soldano discloses that the core material (503) of each of the plurality of waveguides has a first index of refraction (e.g., silica with n greater than 1.45) and that the medium external (e.g., air, $n \sim 1.0$) to and adjacent the tapered region (409) has a second of refraction, such that the first index of refraction is greater than the second index of refraction. *See* Ex. 1005, FIGS. 4-5, 9:56-60; Ex. 1003, ¶¶ 98-99.

Claim 7

A POSITA would have understood that the AWG chip described in Soldano typically would be enclosed within a module containing air or an inert gas to prevent the accumulation of dust. A POSITA therefore would have understood that the external medium adjacent to the tapered region (409) of the AWG chip would be air

or similar gas having an index of refraction of about 1.0. Ex. 1003, ¶¶ 100-101.

Claim 8

Soldano discloses that the core material (503) provides a portion of the angled surface (409) and that the angled surface is configured to reflect light based at least on the interior angle of the angled surface. *See* Ex. 1005, FIG. 5, 9:23-37, 9:52-66; Ex. 1003, ¶¶ 102-103.

Claim 9

Soldano discloses that the PLC may be glass or one of a variety of materials typically used in making waveguides. *See* Ex. 1005, 9:45-51. Accordingly, a POSITA would have understood that the AWG chip described in Soldano would be made of a material such as doped fused silica having n between 1.45 and 1.5. Ex. 1003, ¶¶ 104-105.

Claim 10

Soldano discloses an AWG chip that having a $1 \times N$ demultiplexer, in which a single multi-wavelength optical input signal is demultiplexed into N different wavelengths, specifically 4 different wavelengths. *See* Ex. 1005, FIGS. 3-4, 7:29-37, 7:62-8:8; Ex. 1003, ¶¶ 106-107.

Claim 11

Soldano discloses an AWG chip that is implemented in an AWG device package. *See* Ex. 1005, FIG. 3, 7:24-8:60; Ex. 1003, ¶¶ 108-109.

B. Ground 2: Claims 12-19 Are Unpatentable Under 35 U.S.C. § 103 as Obvious over Soldano in View of Lurie or Tomita.

Claim 12

[12a] Soldano discloses an optical transceiver module. *See* Ex. 1005, FIGS. 3-5, 7:62-8:28; Ex. 1003, ¶ 110.

[12b] A POSITA would have understood that the structure disclosed in Soldano would be housed in a transceiver housing configured in accordance with a relevant photonics module specification prescribed at the time the application for the Soldano patent was filed, e.g., SFF Committee Specification SFF - 8665 for QSFP + 28 Gb/s. 4x Pluggable Transceiver Solution (QSFP28) published May 10, 2013. *See* Ex. 1005, 12:62-13:15; Ex. 1001, 5:35-41; Ex. 1003, ¶ 111.

[12c] Soldano discloses a multi-channel receiver optical subassembly (ROSA) that includes an AWG chip. *See* Ex. 1005, FIGS. 3-5, 7:24-37; Ex. 1003, ¶ 112.

[12d] Soldano discloses an AWG chip having a first end coupled to an optical coupling receptacle (303) to receive an incoming optical signal comprising a plurality of channel wavelengths (401). As illustrated in FIG. 3, the first end of the PLC includes an angled surface where it joins the optical receptacle (303) to reduce back reflections of the optical signal launched into the AWG chip. *See* Ex. 1005, FIG. 3, 3:17-25, 4:15-39, 7:62-8:8, 8:61-9:10; Ex. 1003, ¶ 113.

A POSITA also would have understood that when coupling optical components, angled physical contact (“APC”) should be used to reduce back-reflections. This concept was well-known in the optical communications field many years before the application for the ’116 Patent was filed, as typified by U.S. Patent No. 5,351,327 to Lurie et al. (Ex. 1006) and U.S. Patent No. 4,978,193 to Tomita (Ex. 1007). *See, e.g.*, Ex. 1006, 1:35-39; Ex. 1007, 2:58-68; Ex. 1003, ¶ 114. It would have been obvious to angle the surface of the PLC that couples to the optical coupling receptacle (303) and fiber (306) for the reasons described in Lurie and Tomita. Figure 3 of Soldano depicts just such an angled junction. Ex. 1003, ¶¶ 115-118.

[12e] Soldano discloses a PLC (302) coupled to the first end (401) configured to de-multiplex (404) each channel wavelength of the plurality of channel wavelengths. *See* Ex. 1005, FIGS. 4-5, 8:61-9:23; Ex. 1003, ¶ 119.

[12f] Soldano discloses a plurality of output waveguides coupled to the PLC (302) configured to receive light corresponding to an associated de-multiplexed channel wavelength launched from PLC and transmit the light along a first light path towards a second end (409) of the AWG chip. *See* Ex. 1005, FIGS. 4-5, 9:5-10, 9:52-10:25; Ex. 1003, ¶ 120.

[12g] Soldano discloses a tapered region (409) at the second end of PLC (302) of the AWG chip to receive light via the plurality of output waveguides and reflects

the light towards an output interface region of the AWG chip. *See* Ex. 1005, FIGS. 4-5, 9:23-34, 9:52-65; Ex. 1003, ¶ 121.

[12h] Soldano discloses that light directed to the silicon photonics chip (301) alternatively could pass through grating couplers (505) or directly to an array of photodetectors. *See* Ex. 1005, 10:10-19 (“On the receiver side, a grating coupler may not be necessary. Depending on the silicon technology, the light in the glass PLC 302 could be deflected down by the side polish (409) and instead of hitting a grating coupler (505) and entering a waveguide (506), could instead hit a photodetector ... in lieu of the grating coupler (505). The photodetector would then be electrically connected to the transimpedance amplifier.”); Ex. 1003, ¶ 122.

[12i] Soldano discloses a multi-channel transmitter optical assembly (TOSA) including at least one laser package located in the transceiver housing for transmitting signals at different channel wavelengths. Specifically, Soldano discloses that separate channel wavelengths processed by silicon photonics chip (301) and modulated by lasers are then passed back via the angled end (409) to the multiplexer (405) of PLC (302). *See* Ex. 1005, FIGS. 3-5, 7:37-51, 8:20-28, 8:54-60, 9:10-15; Ex. 1003, ¶ 123. Additionally, to the extent that a POSITA could not rely on the angled connection between the optical connector and the AWG that is depicted in FIG. 3 of Soldano, a POSITA nevertheless would have readily known that an angled junction should be used therebetween, as taught decades earlier by

Lurie and Tomita. Ex. 1003, ¶ 124.

Claim 13

A POSITA would have understood that when PLC (302) is aligned with silicon photonics chip (301), an air gap will exist between the output interface region of the angle polish (409) and grating couplers or photodetectors (505), for example, to permit alignment of these pieces and for thermal expansion. *See* Ex. 1005, FIG. 5, 8:29-60; Ex. 1003, ¶ 125; *see also* Ex. 1008, FIG. 1, ¶ 43; Ex. 1009, pp. 6, 8. Therefore, Soldano fully anticipates Claim 13 on its own, or alternatively, when combined with knowledge of skill in the art, as typified by Lurie or Tomita, Soldano renders Claim 13 obvious. Ex. 1003, ¶ 126.

Claim 14

A POSITA would have understood the benefit of not having the output interface region of the PLC (302) in intimate contact with the silicon photonics chip (301), such as to provide an offset between these structures to account for the effects of thermal expansion. It would have been a simple design choice to leave an air gap of 50 microns between the PLC and the photodetectors, and no criticality is attributed to that distance in the '116 Patent. *See* Ex. 1001 at 10:14-17. Therefore, Soldano fully anticipates Claim 14 on its own, or alternatively, when combined with knowledge of skill in the art, as typified by Lurie or Tomita, Soldano renders Claim 14 obvious. Ex. 1003, ¶¶ 127-128.

Claim 15

Soldano discloses AWG chip defines a plurality of sidewalls that extend longitudinally from the first end to the second end, wherein a tapered region (409) of the second end defines an angled surface that extends from a first sidewall of the plurality of sidewalls to a second sidewall of the plurality of sidewalls. *See* Ex. 1005, FIGS. 4-5, 9:23–37; Ex. 1003, ¶ 129. Therefore, Soldano fully anticipates Claim 15 on its own, or alternatively, when combined with knowledge of skill in the art, as typified by Lurie or Tomita, Soldano renders Claim 15 obvious. Ex. 1003, ¶ 130.

Claim 16

Soldano discloses that the AWG chip has an angled end (409) that redirects light from a horizontal orientation in the channel wavelength waveguides to vertical orientation exiting the PLC (302), which necessarily requires an angle within the claimed range of 41 to 45 degrees relative to the exposed output interface region. *See* Ex. 1005, FIGS. 4-5, 9:23-37; Ex. 1003, ¶ 131. Therefore, Soldano fully anticipates Claim 16 on its own, or alternatively, when combined with knowledge of skill in the art, as typified by Lurie or Tomita, Soldano renders Claim 16 obvious. Ex. 1003, ¶ 132.

Claim 17

Soldano discloses that the output waveguides of the AWG chip comprise a core material (503) and include a cladding material (502), (504) disposed on the core

material (503), such that the core material (503) defines at least a portion of the first and second sidewalls. *See* Ex. 1005, FIGS. 4-5, 9:56-66; Ex. 1003, ¶ 133. Therefore, Soldano fully anticipates Claim 17 on its own, or alternatively, when combined with knowledge of skill in the art, as typified by Lurie or Tomita, Soldano renders Claim 17 obvious. Ex. 1003, ¶ 134.

Claim 18

Soldano discloses that the core material (503) provides a portion of the angled surface (409) and that the angled surface (409) is configured to reflect light based at least on the interior angle of the angled surface relative to the output interface of the AWG chip. *See* Ex. 1005, FIG. 5, 9:23-37, 9:52-66; Ex. 1003, ¶ 135. Therefore, Soldano fully anticipates Claim 18 on its own, or alternatively, when combined with knowledge of skill in the art, as typified by Lurie or Tomita, Soldano renders Claim 18 obvious. Ex. 1003, ¶ 136.

Claim 19

A POSITA would have understood that the photonics structure disclosed in Soldano could be used in any available module format that existed circa 2016 when the application for the '116 Patent was filed. This includes the Quad Small Form-factor pluggable “QSFP” specification, released in 2013, discussed *supra*, element 12(b), which specified at least four different channel wavelengths of 25 Gbps per channel. Ex. 1003, ¶ 137. Therefore, Soldano fully anticipates Claim 19 on its own,

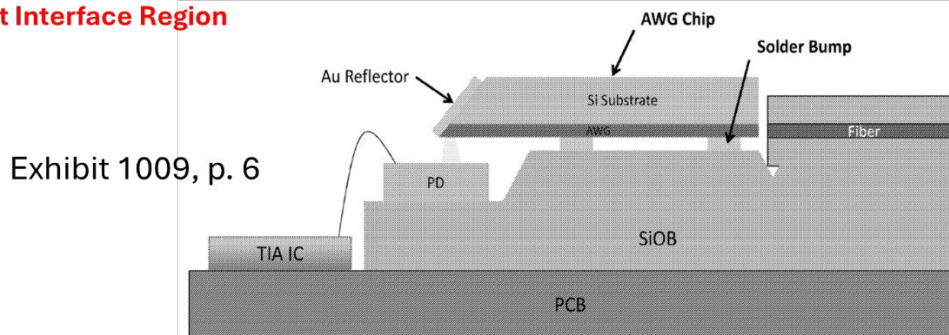
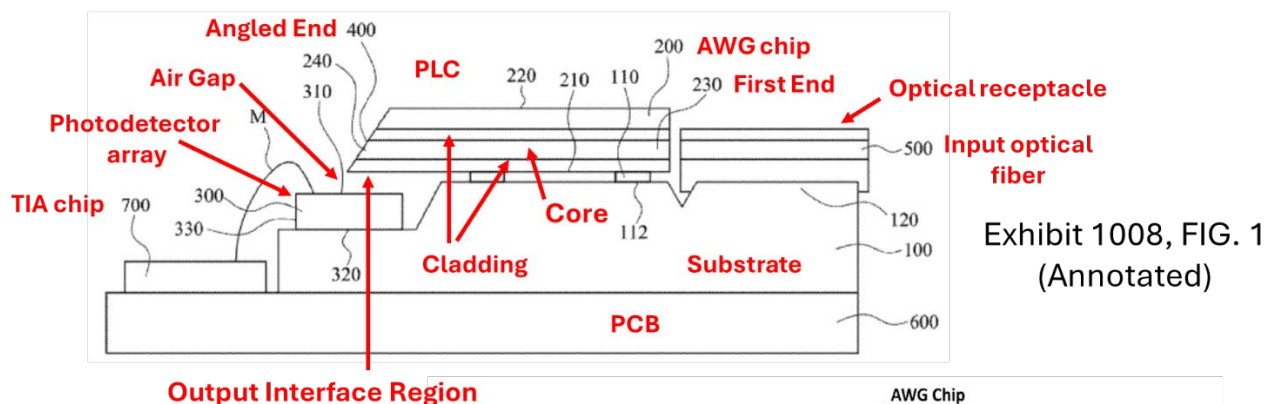
or alternatively, when combined with knowledge of skill in the art, as typified by Lurie or Tomita, Soldano renders Claim 19 obvious. Ex. 1003, ¶ 138.

C. Ground 3: Claims 1-11 Are Unpatentable Under 35 U.S.C. § 102 as Anticipated by Shen, Exhibits 1008 and 1009.

In the following analyses, Petitioner refers to the disclosure of Figures 1-3 of the published Shen U.S. Patent Application, Ex. 1008, and the corresponding figures and text supporting of the Shen U.S. Provisional Patent Application, Ex. 1009, which Shen incorporates by reference at paragraph [0001]. Ex. 1003, ¶ 139

Claim 1

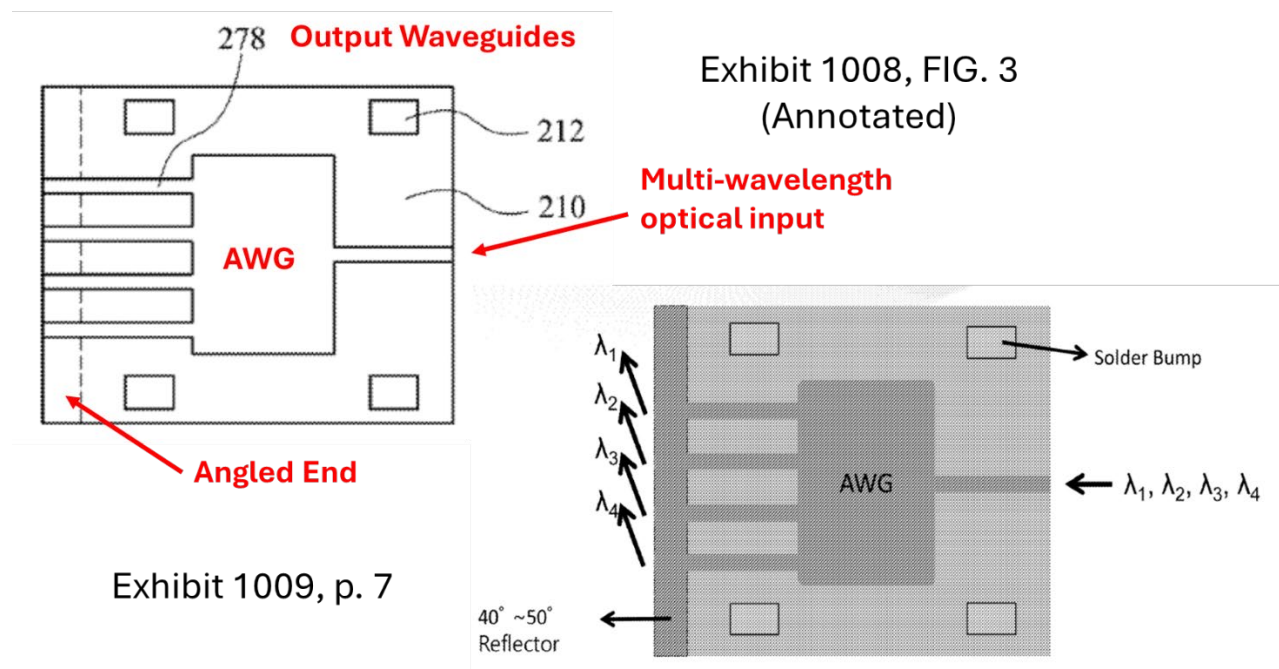
[1a] Shen discloses an arrayed waveguide grating (AWG) chip (200), which a POSITA would have understood for use in an optical receiver or transceiver module. *See* Ex. 1008, FIGS. 1-3, ¶ [0033]; Ex. 1009, pp. 5-8; Ex. 1003, ¶ 140.



[1b] Shen discloses the AWG chip (200) has a first end (230) for coupling to an optical fiber (500) to receive an optical signal including a plurality of channel wavelengths. *See* Ex. 1008, FIG. 4, ¶ [0043]; Ex. 1009, p. 7; Ex. 1003, ¶ 141.

[1c] As construed by Patentee, Shen discloses that the AWG chip (200) is supported atop a silicon optical bench (SiOB) (100), which serves as substrate. Ex. 1008, ¶¶ [0007], [0017]-[0020], [0033], [0036]-[0037], [0043]; Ex. 1009, pp. 6-8; Ex. 1003, ¶ 142.

[1d] Shen discloses a planar lightwave circuit (PLC) is disposed on substrate (100). The PLC is coupled to the first end (230) and is designed to demultiplex the incoming multi-wavelength optical signal into a discrete plurality of channel wavelengths. *See* Ex. 1008, FIG. 3, ¶ [0043]; Ex. 1009, p. 7; Ex. 1003, ¶ 143.



[1e] Shen discloses a plurality of output waveguides (278) are coupled to PLC, with each of the output waveguides (278) designed to transmit light of a channel wavelength launched from PLC along first light path that extends towards second end of the AWG chip (200). *See* Ex. 1008, FIGS. 1-3; ¶¶ [0038]-[0039], [0043]; Ex. 1009, pp. 6-8; Ex. 1003, ¶ 144.

[1f] Shen discloses a tapered region (400) located at second end of the AWG chip (200), which receives light via the plurality of output waveguides (278) and reflects the light towards exposed output interface region of AWG chip. Ex. 1008, FIGS. 1-3, ¶¶ [0038]-[0039], [0043]; Ex. 1009, pp. 6-8; Ex. 1003, ¶ 145. The exposed output interface region emits received light from the AWG chip on the same side as substrate (100) without passing it through the substrate. *Id.*

Claim 2

Shen discloses that the output interface region is configured to pass reflected light received via the plurality of waveguides (278) out of the AWG chip along a path that is substantially orthogonal to the first light path. *See* Ex. 1008, FIGS. 1-3, ¶¶ [0038]-[0039], [0043]; Ex. 1009, pp. 6-8; Ex. 1003, ¶¶ 146-147.

Claim 3

Shen discloses the AWG chip (200) defines a plurality of sidewalls extending longitudinally from first end to second end, wherein a tapered region of the second end defines an angled end (400) that extends from a first sidewall of the plurality

of sidewalls to a second sidewall of the plurality of sidewalls. *See* Ex. 1008, FIGS. 1-2, ¶¶ [0038]-[0041]; Ex. 1009, pp. 6-8; Ex. 1003, ¶¶ 148-149.

Claim 4

Shen discloses that the AWG chip (200) has an angled end (400) that redirects light from a horizontal orientation in the channel wavelength waveguides (278) to vertical orientation exiting the PLC, wherein the reflector angle is 40° to 50°, which encompasses the claimed range of 41 to 45 degrees relative to the output interface region. *See* Ex. 1008, FIGS. 1-3, ¶¶ [0038]-[0041], [0043]; Ex. 1009, pp. 6-8; Ex. 1003, ¶¶ 150-151.

Claim 5

Shen discloses that the output waveguides (278) of the AWG chip (200) comprise a core material (270) and include a cladding material (250), (260) disposed on either side of the core material (270), such that the core material defines at least a portion of the first and second sidewalls. *See* Ex. 1008, FIGS. 1-3, ¶¶ [0041]-[0042]; Ex. 1009, pp. 6-8; Ex. 1003, ¶¶ 152-153.

Claim 6

Shen discloses that the core material (270) of each of the plurality of waveguides (278) has a first index of refraction (e.g., silica with n greater than 1.45) and that the medium external (e.g., air, $n \sim 1.0$) to and adjacent the tapered region has a second of refraction, such that the first index of refraction is greater than the

second index of refraction. *See* Ex. 1008, FIGS. 1-3, ¶¶ [0038]-[0041], [0043]; Ex. 1009, pp. 6-8; Ex. 1003, ¶¶ 154-155.

Claim 7

A POSITA would have understood that the AWG chip described in Shen typically would be enclosed within a module containing air or an inert gas to prevent the accumulation of dust. A POSITA therefore would have understood the external medium adjacent to the tapered region of the AWG chip (200) would be air or similar gas having an index of refraction of about 1.0. Ex. 1003, ¶¶ 156-157.

Claim 8

Shen discloses that the core material provides a portion of the angled end (400) and that the angled end is configured to reflect light based at least on the interior angle of the angled surface. *See* Ex. 1008, FIGS. 1-2; ¶¶ [0038]-[0041]; Ex. 1009, pp. 6-8; Ex. 1003, ¶¶ 158-159.

Claim 9

Shen discloses that the PLC comprises an optically suitable material typically used in making waveguides. *See* Ex. 1008, FIGS. 1-2; ¶¶ [0038]-[0041]. A POSITA would have understood that the AWG chip described in the '116 Patent typically would be made of a material, such as doped fused silica, having n between 1.45 and 1.5. Ex. 1003, ¶¶ 160-161.

Claim 10

Shen discloses an AWG chip (200) that having a 1xN demultiplexer, in which a single multi-wavelength optical input signal is demultiplexed into N different wavelengths, specifically 4 different wavelengths. *See* Ex. 1008, FIGS. 3, ¶ [0043]; Ex. 1009, p. 7; Ex. 1003, ¶¶ 162, 163.

Claim 11

Shen discloses an AWG chip that is implemented in an AWG device package. *See* Ex. 1008, FIGS. 1, ¶¶ [0033], [0035], [0044]; Ex. 1009, pp. 5-8; Ex. 1003, ¶ 164, 165.

D. Ground 4: Claims 12-19 Are Unpatentable Under 35 U.S.C. § 103 as Obvious over Shen in View of Soldano and Further in view of Lurie or Tomita.

Motivation to Combine Shen with Soldano and Lurie or Tomita

Soldano discloses an optical transceiver module. *See* Ex. 1005, FIGS. 3-5, 7:62-8:28. Shen discloses an AWG arrangement that may be used in a photonics module for demultiplexing an incoming multi-wavelength optical signal and directing the resulting separate wavelength optical signals onto detectors to generate electrical signals for further processing. Ex. 1008, Abstract, ¶¶ [0033]-[0040]. Soldano and Shen both relate to the same field of endeavor, optical communications, and both are directed to increasing the density of the carried signals. Accordingly, a POSITA would have understood the advantages of using Shen in the device of

Soldano, which includes similar AWG structure to implement both ROSA and TOSA functionalities. Ex. 1003, ¶ 166.

Additionally, when coupling the AWG of Shen to an incoming optical fiber, a POSITA would have been motivated to employ the angled junction depicted in Figure 3 of Soldano to reduce reflections, exactly as taught decades earlier by Lurie and Tomita. Because both Lurie and Tomita are also directed to the field of optical communications, it would have been common knowledge for a POSITA to use angled junctions for connection of optical fibers to other optical components, and such a configuration would have been used by a POSITA in implementing the structure described in Shen. Ex. 1003, ¶ 167.

Claim 12

[12a] Shen discloses an arrayed waveguide grating (AWG) chip (200), which a POSITA would have understood for use in an optical receiver (as described in Shen) or as part of a transceiver module (as described in Soldano). *See* Ex. 1008, FIGS. 1-3, ¶ [0033]; Ex. 1009, pp. 5-8; Ex. 1005, FIGS. 3-5, 7:62-8:28; Ex. 1003, ¶ 168.

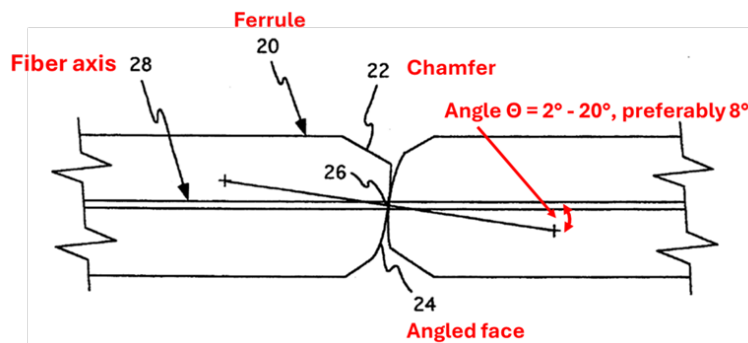
[12b] A POSITA would have understood that the AWG chip (200) disclosed in Shen would be located in a transceiver housing configured in accordance with a relevant photonics module specification prescribed at the time the Shen patent application was filed, e.g., SFF Committee Specification SFF - 8665 for QSFP +

28 Gb/s. 4x Pluggable Transceiver Solution (QSFP28) published May 10, 2013.

See Ex. 1001, 5:35-41; Ex. 1003, ¶ 169.

[12c] Shen discloses a multi-channel receiver optical subassembly (ROSA) 404 that includes an AWG chip (200). See Ex. 1008, FIG. 4, ¶ [0043]; Ex. 1009, pp. 5, 7; Ex. 1003, ¶ 170.

[12d] Shen discloses an AWG chip (200) having a first end (230) for coupling to an optical fiber to receive an incoming optical signal comprising a plurality of channel wavelengths. See Ex. 1008, FIG. 4, ¶ [0043]; Ex. 1009, pp. 5, 7. A POSITA would have understood that when coupling optical components, angled physical contact (“APC”) should be used to reduce back-reflections. This concept was well-known in the optical communications field many years before the application for the ’116 Patent was filed, as typified by Lurie and Tomita. See, e.g., Ex. 1006, 1:35-39; Ex. 1007, 2:58-68. It would have been obvious to angle the surface of the PLC of Shen that couples to the optical fiber for the reasons described in Lurie and Tomita. Ex. 1003, ¶¶ 171-176.



Ex. 1006, FIG. 2 (annotated)

[12e] Shen discloses a PLC coupled at its first end (230) and configured to de-multiplex each channel wavelength of the plurality of channel wavelengths. *See* Ex. 1008, FIG. 3, ¶ [0043]; Ex. 1009, pp. 5, 7; Ex. 1003, ¶ 177.

[12f] Shen discloses a plurality of output waveguides (278) coupled to the PLC configured to receive light corresponding to an associated de-multiplexed channel wavelength launched from PLC and provide the light along a first light path towards a second end of the AWG chip. *See* Ex. 1008, FIGS. 1-3, ¶¶ [0038]-[0039], [0043]; Ex. 1009, pp. 6-8; Ex. 1003, ¶ 178.

[12g] Shen discloses a tapered region (400) at the second end of PLC of the AWG chip (200) to receive light via the plurality of output waveguides and reflect the light towards an output interface region of the AWG chip. *See* Ex. 1008, FIGS. 1-2, ¶¶ [0038]-[0039]; Ex. 1009, pp. 6-8; Ex. 1003, ¶ 179.

[12h] Shen has an array of photodetectors (300) disposed adjacent to the output interface region of the PLC to receive the separate channel wavelengths. *See* Ex. 1008, FIGS. 1-3, ¶¶ [0033]-[0037], [0043]; Ex. 1009, pp. 6-8; Ex. 1003, ¶ 180.

[12i] A POSITA would have understood that the AWG chip of Shen would be used in a transceiver module, such as in Soldano, that includes a multi-channel transmitter optical assembly (TOSA) having at least one laser package located in the transceiver housing for transmitting signals at different channel wavelengths. *See* Ex. 1005, FIGS. 3-5, 7:37-51, 8:20-28, 8:54-60, 9:10-15; Ex. 1003, ¶¶ 181-182.

Claim 13

Shen discloses that an air gap exists between the output interface region of the PLC and photodetectors (300), for example, as a result of affixing the AWG chip to the substrate (100) via the bonding pads (110). *See* Ex. 1008, FIG. 1, ¶ [0043]; Ex. 1009, pp. 6-8; Ex. 1003, ¶ 183. A POSITA would have understood that Shen combined with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 13 obvious. Ex. 1003, ¶ 184.

Claim 14

A POSITA would have understood that it would be a simple design choice to leave an air gap of 50 microns between the AWG chip (200) and the underlying photodetector array (300) to provide benefits, such as providing an offset between these structures to account for the effects of thermal expansion, and no criticality is attributed to that distance in the '116 Patent. *See* Ex. 1008, FIG. 1, ¶ [0043]; Ex. 1009, pp. 6, 8; Ex. 1001, 10:14-17; Ex. 1003, ¶ 185. A POSITA would have understood that Shen combined with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 14 obvious. Ex. 1003, ¶ 186.

Claim 15

Shen discloses AWG chip (200) defines a plurality of sidewalls extending longitudinally from the first end (230) to the second end, wherein a tapered region of the second end defines an angled end (409) that extends from a first sidewall of

the plurality of sidewalls to a second sidewall of the plurality of sidewalls. *See* Ex. 1008, FIGS. 1-2, ¶¶ [0038]-[0041]; Ex. 1009, pp. 6-8; Ex. 1003, ¶ 187. A POSITA would have understood that Shen combined with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 15 obvious. Ex. 1003, ¶ 188.

Claim 16

Shen discloses that the AWG chip (200) has an angled end (400) that redirects light from a horizontal orientation in the channel wavelength waveguides (278) to vertical orientation exiting the PLC, wherein the reflector angle is 40° to 50°, which encompasses the claimed range of 41 to 45 degrees relative to the output interface region. *See* Ex. 1008, FIGS. 1-2, ¶¶ [0038]-[0041]; Ex. 1009, pp. 6-8; Ex. 1003, ¶ 189. A POSITA would have understood that Shen combined with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 16 obvious. Ex. 1003, ¶ 190.

Claim 17

Shen discloses that the output waveguides (278) of the AWG chip (200) comprise a core material (270) having cladding material (250), (260) disposed thereon, such that the core material defines at least a portion of the first and second sidewalls. *See* Ex. 1008, FIG. 2, ¶¶ [0041]-[0042]; Ex. 1009, pp. 6-8. A POSITA would have understood that Shen combined with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 17 obvious. Ex. 1003, ¶¶ 192-193.

Claim 18

Shen discloses that the core material (270) provides a portion of the angled end (400) and that the angled end is configured to reflect light based at least on the interior angle of the angled surface relative to the output interface of the AWG chip. *See* Ex. 1008, FIGS. 1-2, ¶¶ [0038]-[0041]; Ex. 1009, pp. 6-8; Ex. 1003, ¶ 193. A POSITA would have understood that Shen combined with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 18 obvious. Ex. 1003, ¶ 194.

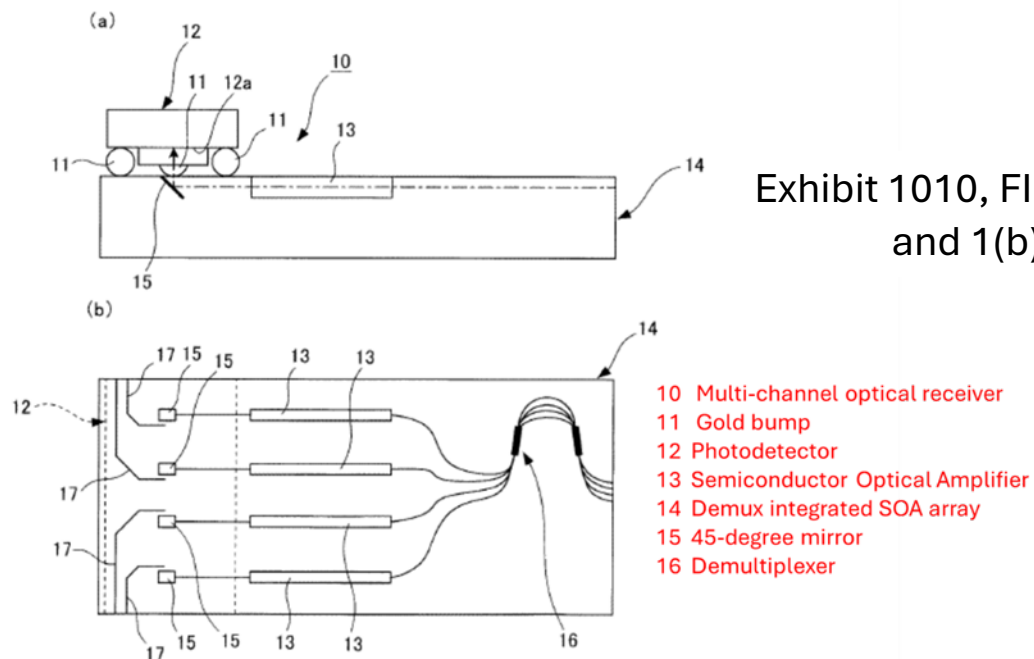
Claim 19

A POSITA would have understood that the AWG chip (200) described in Shen typically would be used in any available module format that existed circa 2016 when the application for the '116 Patent was filed, e.g., SFF Committee Specification SFF - 8665 for QSFP + 28 Gb/s. 4x Pluggable Transceiver Solution (QSFP28) published May 10, 2013, which specified at least four different channel wavelengths of 25 Gbps per channel. *See* Ex. 1001, 5:35-41; Ex. 1003, ¶ 195. A POSITA would have understood that Shen combined with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 19 obvious. Ex. 1003, ¶ 196.

E. Ground 5: Claims 1-11 Are Unpatentable Under 35 U.S.C. § 103 as Obvious over Kanazawa in View of Sasaki.

Motivation to Combine Kanazawa with Sasaki

Kanazawa discloses a multi-channel optical receiver module having a PLC including an AWG that demultiplexes a multi-wavelength input signal into separate wavelengths, which wavelengths pass through a corresponding plurality of waveguides to photodetectors in a semiconductor optical amplifier (“SOA”). Ex. 1010, FIGS. 1(a), 1(b); Ex. 1011, Abstract, ¶¶ [0006]-[0008]; Ex. 1003, ¶ 197.



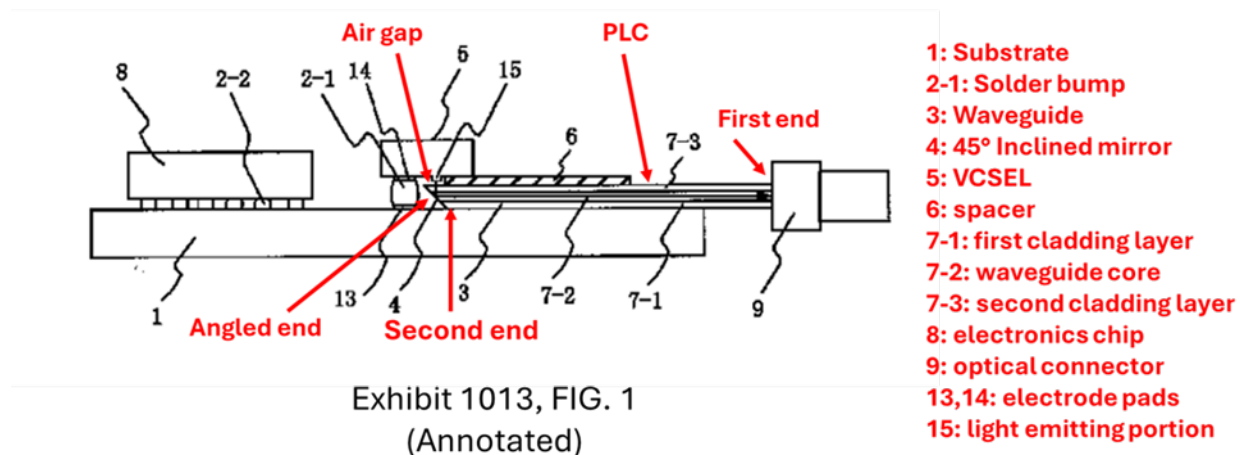
Sasaki discloses a PLC for use in an optical communication module in which a plurality of channel wavelengths in corresponding waveguides are directed orthogonally out of the plane of the waveguides to a plurality of photodetectors using an angled end of the PLC. Ex. 1012, FIGS. 1, 2, 6; Ex. 1013, ¶¶ [0017]-[0018]; Ex. 1003, ¶ 198.

Kanazawa and Sasaki both disclose structures for use in optical transceiver modules. Sasaki describes a PLC that has an angled end for orthogonally redirecting light into or out of an adjacent waveguide carrying four separate wavelength optical signals. Kanazawa describes mirrors that redirect separate optical wavelength signals coming from, or heading towards, an AWG that serves to de-multiplex (or multiplex) the signals. Kanazawa and Sasaki both relate to the same field of endeavor, optical communications, and both are directed to increasing the density of the carried signals and compactness of the photonics module. A POSITA would have been motivated to use the angled end of the PLC disclosed in Sasaki in the AWG device of Kanazawa to increase both signal density and compactness of a photonics module, while also employing the AWG structure of Kanazawa to implement both ROSA and TOSA functionalities. Ex. 1003, ¶ 199.

Neither Kanazawa nor Sasaki were cited during prosecution of the '116 Patent. Ex. 1003, ¶¶ 78, 81.

Claim 1

[1a] Kanazawa discloses a multichannel optical receiver having an arrayed waveguide grating (AWG) chip (14) for demultiplexing an input light beam into multiple light beams (16), the number of which is the same as that of the channels. *See* Ex. 1010, FIG. 1; Ex. 1011, Abstract, ¶¶ [0001]-[0003], [0006], [0015]-[0018], [0022]; Ex. 1003, ¶ 200.



[1b] Kanazawa discloses the AWG chip (14) has a first end configured for coupling to an optical fiber to receive an input optical signal including a plurality of channel wavelengths. *See* Ex. 1010, FIG. 1; Ex. 1011, ¶¶ [0016]-[0018]. Ex. 1003, ¶ 201.

[1c] As construed by Patentee, Kanazawa discloses that the AWG chip (14) is disposed adjacent to a photodetector array (12) that is disposed on a substrate. *See* Ex. 1010, FIG. 1; Ex. 1011, ¶ [0017]; Ex. 1003, ¶ 202.

[1d] Kanazawa discloses that the AWG chip (14), which is a planar lightwave circuit (PLC), is disposed adjacent to the photodetector array 12. The PLC is coupled to the first end and is designed to de-multiplex (16) an input multi-wavelength optical signal into a discrete plurality of channel wavelengths. *See* Ex. 1010, FIG. 1; Ex. 1011, Abstract, ¶¶ [0016]-[0018]; Ex. 1003, ¶ 203.

[1e] Kanazawa discloses a plurality of output waveguides (13) are coupled to the demultiplexer (16) of the PLC, with each of the output waveguides (13)

designed to transmit light of a channel wavelength launched from PLC along first light path that extends towards second end of the AWG chip. *See* Ex. 1010, FIG. 1; Ex. 1011, Abstract, ¶¶ [0016]-[0017]; Ex. 1003, ¶ 204.

[1f] Kanazawa discloses mirrors (15) angled at 45 degrees embedded in the AWG chip (14), at the output ends of the plurality of individual channel wavelength waveguides (13), to redirect light to the photodetector array (12). *See* Ex. 1010, FIG. 1; Ex. 1011, ¶¶ [0016], [0018]. Sasaki describes a PLC having an angled end (4) for redirecting light between a plurality of horizontal channel wavelength waveguides (7-2) and vertically to photodetectors or light-emitting diodes (5, 15). *See* Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0017]-[0018], [0024]-[0025], [0052]; Ex. 1003, ¶ 205. A POSITA would have been motivated to substitute the angled end of Sasaki for the angled mirrors (15) embedded in the PLC of Kanazawa to simplify construction thereof. In this manner, configuring the second end of the AWG chip of Kanazawa to have an angled end, as taught in Sasaki, would result in directing light exiting the plurality of output waveguides towards adjacent photodetector array (12) without passing the received light through the substrate. Both Kanazawa and Sasaki are directed to the field of reducing the size of photonics modules, simplifying assembly, and improving alignment accuracy, which benefits would have been readily apparent to a POSITA making the optical receiver disclosed in Kanazawa. Ex. 1003, ¶¶ 206-207.

Claim 2

Sasaki discloses that the output interface region of the PLC is configured to pass reflected light received via the plurality of waveguides along a path that is substantially orthogonal to the first light path. *See* Ex. 1012, FIG. 1; Ex. 1013, Abstract, ¶¶ [0023]-[0026], [0052]; Ex. 1003, ¶ 208. A POSITA would have been motivated to combine the angled end of Sasaki in the AWG chip of Kanazawa for simplicity of manufacture and assembly. Ex. 1003, ¶ 209.

Claim 3

Sasaki discloses that the PLC defines a plurality of sidewalls extending longitudinally from first end to second end, wherein a tapered region of the second end defines an angled surface (4) that extends from a first sidewall of the plurality of sidewalls to a second sidewall of the plurality of sidewalls. *See* Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0019], [0023]-[0026], [0052]; Ex. 1003, ¶ 210. A POSITA would have been motivated to combine the angled end configuration (4) of Sasaki in the AWG chip of Kanazawa for simplicity of manufacture and assembly. Ex. 1003, ¶ 211.

Claim 4

Sasaki discloses that the PLC has an angled 45-degree surface (4) that redirects light between horizontal orientation (in the channel wavelength waveguides) and vertical orientation (to/from the PLC), and further discloses that

other angles such as 41 to 49 degrees relative to the output interface region may be desirable. *See* Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0025], [0052], [0057]; Ex. 1003, ¶ 212. A POSITA would have been motivated to combine such teachings of Sasaki in the AWG chip of Kanazawa for simplicity of manufacture and assembly. Ex. 1003, ¶ 213.

Claim 5

Sasaki discloses that the output waveguides of the PLC comprise a core material (7-2) and include a cladding material (7-1, 7-3) disposed on the core material (7-2), such that the core material (7-2) defines at least a portion of the first and second sidewalls. *See* Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0023]-[0025], [0052], [0056]; Ex. 1003, ¶ 214. A POSITA would have understood that optical waveguides generally employ a core sandwiched between cladding layers, and thus this configuration of Sasaki would be used in the AWG chip of Kanazawa. Ex. 1003, ¶ 215.

Claim 6

Sasaki discloses that the core material (7-2) of each of the plurality of waveguides has a first index of refraction (e.g., a siloxane polymer or glass with n generally above 1.5) and that the medium external (e.g., air, $n \sim 1.0$) to and adjacent to the tapered region has a second index of refraction, such that the first index of refraction is greater than the second index of refraction. *See* Ex. 1012, FIG. 1; Ex. 1013,

Abstract ¶¶ [0023]-[0025], [0052], [0056]. A POSITA would have understood that these aspects of Sasaki were directly transferable to the AWG chip of Kanazawa. Ex. 1003, ¶¶ 216-217.

Claim 7

A POSITA would have understood that the AWG chip described in Kanazawa typically would be enclosed within a module containing air or an inert gas to prevent the accumulation of dust. A POSITA therefore would have understood the external medium adjacent to the tapered region of the AWG chip would be air or similar gas having an index of refraction of about 1.0. Ex. 1003, ¶¶ 218, 219.

Claim 8

Sasaki discloses that the core material (7-2) provides a portion of the angled surface and that the angled surface is configured to reflect light based at least on the interior angle of the angled surface. *See* Ex. 1012, FIG. 1; Ex. 1013, Abstract ¶ [0025]; Ex. 1003, ¶¶ 220-221.

Claim 9

Sasaki discloses that the PLC may be made of a siloxane polymer, glass or other similar material used in waveguides. *See* Ex. 1012, FIG. 1; Ex. 1013, ¶ [0025]. Kanazawa generally describes that the AWG would be made from materials used to create optical waveguides. Accordingly, a POSITA would have understood that the AWG chip combining the teachings of Kanazawa and Sasaki should be made of a

material which is commonly used in waveguides, such as doped fused silica, having n in the range of 1.45 and 1.5. Ex. 1003, ¶¶ 222-223.

Claim 10

Kanazawa discloses an AWG chip that having a $1 \times N$ demultiplexer, in which a single multi-wavelength optical input signal is demultiplexed into N different wavelengths, specifically 4 different wavelengths. *See* Ex. 1010, FIG. 1; Ex. 1011, ¶¶ [0006], [0015]-[0022]. Sasaki discloses a PLC having that receives as its input four channel wavelengths. A POSITA would have been motivated to combine the demultiplexer of Kanazawa with the PLC of Sasaki to reduce the four input channel waveguides of Sasaki to a single input multi-channel optical signal as in Kanazawa. *See* Ex. 1012, FIG. 6; Ex. 1013, ¶ [0018]; Ex. 1003, ¶¶ 224-225.

Claim 11

Kanazawa discloses an AWG chip that is implemented in an AWG device package. *See* Ex. 1010, FIG. 1; Ex. 1011, Abstract, ¶¶ [0001]-[0003], [0005]-[0006], [0011]-[0012]; Ex. 1003, ¶¶ 226-227.

F. Ground 6: Claims 12-19 Are Unpatentable Under 35 U.S.C. § 103 as Obvious over Kanazawa in View of Sasaki and Further in view of Lurie or Tomita

Motivation to Combine Kanazawa with Sasaki Further in View of Lurie or Tomita

Kanazawa discloses a multi-channel optical receiver module having a planar light circuit (“PLC”) including an arrayed waveguide grating. Motivation to

combine Kanazawa with Sasaki is provided above. *See* § VI(E). In addition, Sasaki itself teaches that, when coupling a semiconductor optical component to a waveguide via a mirror, it is preferable to tilt the mirror about 8 degrees to prevent back reflection along the same optical path as the incident light. Ex. 1013, ¶ [0057]; Ex. 1003, ¶ 228.

Additionally, when coupling an incoming optical fiber such as in Kanazawa to an AWG, a POSITA would have known to employ an angled junction to reduce reflections, as taught by Lurie and Tomita decades earlier. Because Lurie and Tomita also both are directed to the same field of optical communications as Kanazawa and Sasaki, it would have been common knowledge for a POSITA to use angled junctions for connection of optical fibers to other optical components, and a POSITA would have used such components in implementing the structure described in Kanazawa. Ex. 1003, ¶ 229.

Claim 12

[12a] Kanazawa discloses a multichannel optical receiver having an arrayed waveguide grating (AWG) chip (14) for demultiplexing an input light beam into multiple light beams, the number of which is the same as that of the channels. *See* Ex. 1010, FIG. 1; Ex. 1011, Abstract, ¶¶ [0001]-[0003], [0006], [0015]-[0018], [0022]; Ex. 1003, ¶ 230.

[12b] A POSITA would have understood that the AWG chip (14) disclosed in Kanazawa would be located in a transceiver housing configured in accordance with a relevant photonics module specification prescribed at the time the Kanazawa patent application was filed, e.g., SFF Committee Specification SFF - 8665 for QSFP + 28 Gb/s. 4x Pluggable Transceiver Solution (QSFP28) published May 10, 2013. *See* Ex. 1001, 5:35-41; Ex. 1011, ¶ [0005]; Ex. 1003, ¶ 231.

[12c] Kanazawa discloses a multi-channel receiver optical subassembly (ROSA) that includes the AWG chip (14). *See* Ex. 1010, FIG. 1; Ex. 1011, Abstract, ¶¶ [0005]-[0006], [0014]-[0022]; Ex. 1003, ¶ 232.

[12d] Kanazawa discloses the AWG chip (14) has a first end for coupling to an optical fiber to receive an incoming optical signal comprising a plurality of channel wavelengths. *See* Ex. 1010, FIG. 1; Ex. 1011, ¶¶ [0016]-[0018]; Ex. 1003, ¶ 233. As discussed *supra*, Sasaki teaches that an 8-degree tilt should be used when coupling a waveguide to a semiconductor optical component to prevent back reflection. Further, a POSITA would have understood that when coupling optical components, angled physical contact (“APC”) should be used to reduce back-reflections. This concept was well-known in the optical communications many years before the application for the ’116 Patent was filed, as typified by Lurie and Tomita. *See, e.g.*, Ex. 1006, 1:35-39; Ex. 1007, 2:58-68. It would have been obvious to angle the surface of the PLC of Kanazawa that couples to the optical

fiber for the reasons described in Sasaki, Lurie and Tomita. Ex. 1003, ¶ 234.

[12e] Kanazawa discloses a PLC coupled at its first end and configured to demultiplex each channel wavelength of the plurality of channel wavelengths. *See* Ex. 1010, FIG. 1; Ex. 1011, Abstract, ¶¶ [0016]-[0018]; Ex. 1003, ¶ 235.

[12f] Kanazawa discloses a plurality of output waveguides (13) coupled to the demultiplexer (16) of the PLC, with each of the output waveguides (13) configured to receive light corresponding to an associated de-multiplexed channel wavelength launched from PLC and provide the light along a first light path towards a second end of the AWG chip. *See* Ex. 1010, FIG. 1; Ex. 1011, Abstract, ¶¶ [0016]-[0017]; Ex. 1003, ¶ 236.

[12g] Kanazawa discloses mirrors (15) angled at 45 degrees embedded in the AWG chip (14), at the output ends of the plurality of individual channel wavelength waveguides (13), to redirect light to the photodetector array (12). *See* Ex. 1010, FIG. 1; Ex. 1011, ¶¶ [0016], [0018]. Sasaki discloses a tapered region at the second end of a PLC to receive light via the plurality of output waveguides and reflect the light towards an output interface region of the PLC. *See* Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0017]-[0018], [0024]-[0025], [0052]; Ex. 1003, ¶ 237. A POSITA would have been motivated to substitute the angled end of Sasaki for the angled mirrors (15) embedded in the PLC of Kanazawa to simplify construction thereof. In this manner, configuring the second end of the AWG chip of Kanazawa as an angled end, as

taught in Sasaki, would direct light exiting the plurality of output waveguides towards adjacent photodetector array (12). Both Kanazawa and Sasaki are directed to the field of reducing the size of photonics modules, simplifying assembly, and improving alignment accuracy, which benefits would have been readily apparent to a POSITA making the optical receiver disclosed in Kanazawa. Ex. 1003, ¶ 238.

[12h] Kanazawa has an array of photodetectors (12) disposed adjacent to the output interface region of the PLC to receive the separate channel wavelengths. *See* Ex. 1010, FIG. 1; Ex. 1011, Abstract, ¶¶ [0016]-[0017]; Ex. 1003, ¶ 239.

[12i] A POSITA would have understood that the AWG chip disclosed in Kanazawa would readily be of use in a transceiver module, such as disclosed in Soldano, that includes a multi-channel transmitter optical assembly (TOSA) having at least one laser package located in the transceiver housing for transmitting signals at different channel wavelengths. *See* Ex. 1011, ¶¶ [0001], [0002]; Ex. 1003, ¶ 240; *see also* Ex. 1005, FIGS. 3-5, 7:37-51, 8:20-28, 8:54-60, 9:10-15. A POSITA would have been readily aware that an angled junction should be used where the optical input fiber is coupled to the AWG of Kanazawa, as taught decades earlier in Lurie and Tomita, thus rendering Claim 12 obvious. Ex. 1003, ¶ 241.

Claim 13

Sasaki discloses that an air gap exists between the interface region of the PLC and the array of photodetectors (15), for example, as a result of affixing the AWG

chip to the substrate (5) via solder bumps (2-1). *See* Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0010]-[0012], [0017]-[0018]. A POSITA would have understood that it would be expedient to use this feature of Sasaki to align and join the PLC to the photodetector array (12) of Kanazawa. Ex. 1003, ¶ 242. A POSITA would have understood that the combination of Kanazawa and Sasaki, together with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 13 obvious. Ex. 1003, ¶ 243.

Claim 14

A POSITA would have understood that it would be a simple design choice to leave an air gap of 50 microns between the PLC of Sasaki and the adjacent photodetector array, as implemented for the AWG of Kanazawa, as an air gap between these structures would account for the effects of thermal expansion. Moreover, no criticality is attributed to that distance in the '116 patent. *See* Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0010]-[0012], [0017]-[0018]; Ex. 1003, ¶ 244. A POSITA would have understood that the combination of Kanazawa and Sasaki, together with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 14 obvious. Ex. 1003, ¶ 245.

Claim 15

Sasaki discloses the PLC defines a plurality of sidewalls extending longitudinally from the first end to the second end of the PLC, wherein a tapered region of the second end defines an angled surface that extends from a first

sidewall of the plurality of sidewalls to a second sidewall of the plurality of sidewalls. *See* Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0019], [0023]-[0026], [0052]. It would have been obvious to a POSITA to employ the angled end configuration of Sasaki in the AWG chip of Kanazawa for simplicity of manufacture and assembly. Ex. 1003, ¶ 246. A POSITA would have understood that the combination of Kanazawa and Sasaki, together with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 15 obvious. Ex. 1003, ¶ 247.

Claim 16

Sasaki discloses that the PLC has an angled 45-degree surface (4) that redirects light between horizontal orientation (in the channel wavelength waveguides) and vertical orientation (to/from the PLC), and further discloses that other angles such as 41 to 49 degrees relative to the output interface region may be desirable. *See* Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0025], [0052], [0057]. A POSITA would have been motivated to combine such teachings of Sasaki in the AWG chip of Kanazawa for simplicity of manufacture and assembly. Ex. 1003, ¶ 248. A POSITA would have understood that the combination of Kanazawa and Sasaki, together with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 16 obvious. Ex. 1003, ¶ 249.

Claim 17

Sasaki discloses that the output waveguides of the PLC comprise a core material (7-2) and include a cladding material (7-1, 7-3) disposed on the core material, such that the core material (7-2) defines at least a portion of the first and second sidewalls. *See* Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0023]-[0025], [0052], [0056]. A POSITA would have understood that optical waveguides generally employ a core sandwiched between cladding layers, and thus this configuration of output waveguides of Sasaki would be used in the AWG chip of Kanazawa. Ex. 1003, ¶ 250. A POSITA would have understood that the combination of Kanazawa and Sasaki, together with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 17 obvious. Ex. 1003, ¶ 251.

Claim 18

Sasaki discloses that the core material (7-2) provides a portion of the angled surface and that the angled surface is configured to reflect light based at least on the interior angle of the angled surface relative to the output interface of the AWG chip. *See* Ex. 1012, FIG. 1; Ex. 1013, ¶¶ [0023]-[0025], [0052]. A POSITA would have been motivated to combine the teachings of Sasaki in the AWG chip of Kanazawa for simplicity of manufacture and assembly. Ex. 1003, ¶ 252. A POSITA would have understood that the combination of Kanazawa and Sasaki, together with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 18

obvious. Ex. 1003, ¶ 253.

Claim 19

A POSITA would have understood that the photonics structure disclosed in Kanazawa could be used in any available module format that existed circa 2016 when the application for the '116 patent was filed, e.g., SFF Committee Specification SFF - 8665 for QSFP + 28 Gb/s. 4x Pluggable Transceiver Solution (QSFP28) published May 10, 2013. *See* Ex. 1001, 5:35-41; Ex. 1003, ¶ 254. A POSITA would have understood that the combination of Kanazawa and Sasaki, together with knowledge of skill in the art, as typified by Lurie or Tomita, renders Claim 19 obvious. Ex. 1003, ¶ 255.

VIII. DISCRETIONARY ISSUES

A. The Petition Does Not Present the Same References Addressed During Prosecution of the '116 Patent.

The Board should not deny institution under § 325(d). Under *Advanced Bionics*, the Board uses a two-part framework in determining whether to exercise its discretion under § 325(d). *Advanced Bionics, LLC v. MED-EL Elektromedizinische*, No. IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020).

The Board has held that the first prong of *Advanced Bionics* is not met where “neither [the combination references] nor similar prior art was before the examiner... the prosecution history does not include any overlapping arguments directed to this prior art.” *Godbersen-Smith Constr. Co. v. Guntert & Zimmerman*

Const. Div., Inc. No. IPR2021-00050, Paper 24 at 19–21 (PTAB May 7, 2021). And in such a case, the Board “need not address part two of the analysis.” *Id.* at 21.

This Petition does not include any prior art references that were consistently cited during the original prosecution and are not cumulative of the art considered by the Examiner during prosecution. Ex. 1003, ¶¶ 69, 72, 75, 78, 81.

Thus, the combination of references used in this petition cannot be cumulative of the art and/or arguments raised during prosecution as there are material differences between the grounds herein and what was previously presented. *Tianma Microelectronics Co., v. Japan Display Inc.*, IPR2021-01058, Paper 16 at 31 (PTAB Jan. 5, 2022). Because the first prong is not met, the Board need not move to the second prong. *Id.* at 21; *Oticon Med. AB v. Cochlear Ltd.*, IPR2019-00975, Paper 15 at 20 (PTAB Oct. 16, 2019).

B. The Board Should Not Deny Institution Under *Fintiv*.

The claims of the ’116 Patent have never been tested in view of the most relevant prior art. In view of these strong challenges and the nascent nature of the current district court proceedings, institution should not be discretionarily denied under § 314(a). *See NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 19-20 (PTAB Sept. 12, 2018) (precedential); *Apple v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 13-14 (PTAB Mar. 20, 2020) (precedential).

Factor 1—potential stay of the district court litigation—is neutral because no party has requested a stay. *VMWare, Inc. v. Intellectual Ventures I LLC*, IPR2020-00470, Paper 13 at 17 (PTAB Aug. 18, 2020) (finding in the absence of a stay motion that this factor “does not weigh for or against discretionary denial”).

Factor 2—district court trial date and the Board’s statutory deadline—should be considered neutral. The trial date set for this case according to the Court’s Scheduling Order is June 8, 2026. *See* Ex. 1015, p. 2. The current trial date does not support denial. *See Dish Network v. Broadband iTV*, IPR2020-01280, Paper 17 at 17-18 (PTAB Feb. 4, 2021).

Factor 3—investment in the district court proceedings—weighs heavily against discretionary denial. The associated district court case is still in the very early stages of litigation: discovery is still in the preliminary stages, the Defendants only recently filed their invalidity contentions, and Claim Construction is not scheduled until April 10, 2025. Ex. 1015, p. 2. Moreover, it is unlikely that a claim construction order will issue prior to the PTAB’s projected institution decision date. Accordingly, the district court will not invest significant resources or issue substantive orders related to the challenged patent prior to the issuance of an institution decision. *See Fintiv*, IPR2020-00019, Paper 11 at 9-12. Regardless, Petitioner filed well in advance of the statutory deadline, which weighs against denying institution.

Factor 4—overlap in the parallel proceedings—favors institution. Instituting trial will allow issues to be narrowed in the district court because, if instituted, Petitioner stipulates that it will not pursue invalidity against the asserted claims in the district court using the specific combination of prior art references set forth in the grounds presented in this Petition for purposes of establishing obviousness. *See Sand Revolution II LLC v. Continental Intermodal Group-Trucking LLC*, IPR2019-01393, Paper 24 at 11-12 (PTAB June 16, 2020) (holding a similar stipulation weighs against discretionary denial). Given the lack of overlap between the proceedings, this factor weighs against the Board exercising discretion to deny.

Factor 5—overlapping parties—is neutral as it is “far from an unusual circumstance that a petitioner in *inter partes* review and a defendant in a parallel district court proceeding are the same.” *Sand*, No. IPR2019-01393, Paper 24 at 12-13.

Factor 6—other considerations—weighs against discretionary denial. As explained, the merits of the Petition are strong, and the Challenged Claims are invalid. For example, none of the grounds asserted herein were previously considered by either the Office or the district courts. *Cf. Comcast Cable Commn’s, LLC v. Rovi Guides, Inc.*, IPR2019-00231, Paper 14 at 11 (PTAB May 20, 2019) (obviousness challenges not “previously considered by the Office or any court”

weigh in favor of not denying institution). Accordingly, the Board should decline to exercise its discretion under *Fintiv* and institute trial.

C. The Board Should Not Deny Institution Under *General Plastic*.

The *General Plastic* (*General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 (P.T.A.B. Sep. 6, 2017) factors do not apply because this is the first and only *inter partes* review (“IPR”) petition filed by Petitioner with respect to the ’116 Patent.

IX. CONCLUSION

Petitioner respectfully requests cancellation of the Challenged Claims.

X. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

A. Real Party in Interest (37 C.F.R. §42.8(b)(1))

The real parties-in-interest are Cambridge Industries USA, Inc, which is a named defendant in the associated district court proceeding, and its parent corporation, CIG Shanghai, Co. Ltd.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

Pursuant to 37 C.F.R. § 42.8(b)(2), Petitioner is aware of the following lawsuit or related matters involving the ’116 Patent:

- *Applied Optoelectronics, Inc. v. Cambridge Industries USA, Inc.*,
5:24-cv-01010 (N.D. Cal. filed Feb. 20, 2024)

- *Applied Optoelectronics, Inc. v. Accelight Technologies, Inc.*,
4:24-cv-09041 (N.D. Cal. filed Nov. 19, 2024)

C. Designation of Counsel (37 C.F.R. § 42.8(b)(3))

Petitioner provides the following designation of counsel.

Lead Counsel	Backup Counsel
Nicola A. Pisano Reg. No. 34,408 EVERSHEDS SUTHERLAND (US) LLP 12255 Camino Real, Suite 100 San Diego, California 92130-2071 Phone: (858) 252-2952 Fax: (858) 252-6503 Email: nicolapisano@eversheds-sutherland.com	Regis Worley Reg. No. 58,430 EVERSHEDS SUTHERLAND (US) LLP 12255 Camino Real, Suite 100 San Diego, California 92130-2071 Phone: (858) 252-2952 Fax: (858) 252-6503 Email: regisworley@eversheds-sutherland.com

Pursuant to 37 C.F.R. § 42.8(b)(4), counsel agrees to service by mail as detailed above, and to electronic service by email at the following addresses:

nicolapisano@eversheds-sutherland.com, and regisworley@eversheds-sutherland.com.

Pursuant to 37 C.F.R § 42.10(b), a Power of Attorney executed by Petitioner accompanies this Petition.

D. Service Information (37 C.F.R. § 42.8(b)(4))

Please address all correspondence and service to the addresses listed above.

Petitioner consents to electronic service directed to
nicolapisano@eversheds-sutherland.com and regisworley@eversheds-
sutherland.com.

Date: January 17, 2025

By: /Nicola A. Pisano /

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Claim	Recitation
[1a]	An arrayed waveguide grating (AWG) chip comprising:
[1b]	a first end for coupling to an optical coupling receptacle to receive an optical signal comprising a plurality of channel wavelengths;
[1c]	a substrate;
[1d]	a planar lightwave circuit (PLC) disposed on the substrate, the PLC coupled to the first end and configured to de-multiplex each channel wavelength of the plurality of channel wavelengths;
[1e]	a plurality of output waveguides coupled to the PLC, each of the output waveguides configured to receive light corresponding to an associated de-multiplexed channel wavelength launched from the PLC and provide the light along a first light path that extends towards a second end of the AWG chip; and
[1f]	a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an exposed output interface region of the AWG chip, wherein the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate.
2	The AWG chip of claim 1, wherein the exposed output interface region is configured to pass the reflected light received via the plurality of output waveguides out of the AWG chip along a second light path that is substantially orthogonal to the first light path.
3	The AWG chip of claim 1, wherein the AWG chip defines a plurality of sidewalls extending longitudinally from the first end to the second end, and wherein the tapered region of the second end defines an angled surface that extends from a first sidewall of the plurality of sidewalls to a second sidewall of the plurality of sidewalls.
4	The AWG chip of claim 3, wherein the angled surface has an interior angle of about 41 to 45 degrees relative to the exposed output interface region.
5	The AWG chip of claim 3, wherein each of the output waveguides comprise a core material, and wherein a cladding material is disposed on the core material, the core material defining at least a portion of the plurality of sidewalls of the AWG chip.

6	The AWG chip of claim 5, wherein the core material of each of the plurality of output waveguides has a first index of refraction, and a medium external to and adjacent the tapered region has a second index of refraction, the first index of refraction being greater than the second index of refraction.
7	The AWG chip of claim 6, wherein the external medium comprises a material having an index of refraction of about 1.0.
8	The AWG chip of claim 5, wherein the core material of each of the plurality of output waveguides provide a portion of the angled surface, and wherein the angled surface is configured to reflect incident light based on at least an interior angle of the angled surface.
9	The AWG chip of claim 5, wherein the core material comprises doped silica (SiO ₂) having an index of refraction of about 1.45 to 1.50.
10	The AWG chip of claim 1, wherein the AWG chip is configured as a 1×N demultiplexer device whereby a single optical input signal is demultiplexed into N different channel wavelengths.
11	The AWG chip of claim 1, wherein the AWG chip is implemented in an AWG device package.
[12a]	An optical transceiver module comprising
[12b]	a transceiver housing;
[12c]	a multi-channel receiver optical sub-assembly (ROSA) located in the transceiver housing and including an arrayed waveguide grating (AWG) chip, the AWG chip comprising:
[12d]	a first end for coupling to an optical coupling receptacle to receive an optical signal comprising a plurality of channel wavelengths, wherein the first end for coupling to the optical coupling receptacle includes an angled surface to reduce back reflections of an optical signal launched into the AWG chip;
[12e]	a planar lightwave circuit (PLC) coupled to the first end configured to de-multiplex each channel wavelength of the plurality of channel wavelengths;
[12f]	a plurality of output waveguides coupled to the PLC, each of the output waveguides configured to receive light corresponding to an associated de-multiplexed channel wavelength launched from the PLC and provide the light along a first light path that extends towards a second end of the AWG chip; and

[12g]	a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an output interface region of the AWG chip;
[12h]	an array of detector devices disposed adjacent to the output interface region of the AWG chip; and
[12i]	a multi-channel transmitter optical assembly (TOSA) including at least one laser package located in the transceiver housing for transmitting optical signals at different channel wavelengths.
13	The optical transceiver module of claim 12, wherein the output interface region of the AWG chip is an exposed region adjacent an air gap, and wherein the air gap separates the output interface region of the AWG chip and the array of detector devices.
14	The optical transceiver module of claim 12, wherein the output interface region of the AWG chip is separated from the array of detector devices by about 50 microns.
15	The optical transceiver module of claim 12, wherein the AWG chip defines a plurality of sidewalls extending longitudinally from the first end to the second end, and wherein the tapered region of the second end defines an angled surface that extends from a first sidewall of the plurality of sidewalls to a second sidewall of the plurality of sidewalls.
16	The optical transceiver module of claim 15, wherein the angled surface has an interior angle of about 41 to 45 degrees relative to the output interface region.
17	The optical transceiver module of claim 15, wherein each of the output waveguides comprise a core material, and wherein a cladding material is disposed on the core material, the core material defining at least a portion of the plurality of sidewalls of the AWG chip.
18	The optical transceiver module of claim 17, wherein the core material of each of the plurality of output waveguides provide a portion of the angled surface, and wherein the angled surface is configured to reflect incident light based on at least an interior angle of the angled surface relative to the output interface of the AWG chip.
19	The optical transceiver of claim 12, wherein the transceiver is a Small Form-factor Pluggable (SFP) transceiver module and the ROSA is configured to receive at least four different channel wavelengths at transmission rates of at least about 25 Gbps per channel.

CERTIFICATION UNDER 37 C.F.R. § 42.24

Petitioner certifies that the word count in this Petition is 12,200 words, as counted by the word-processing program (Microsoft Word for Office 365) used to generate this Petition, where such word count excludes the table of contents, table of authorities, mandatory notices, certificate of service, appendix of exhibits, and this certificate of word count. This Petition complies with the 14,000-word limit set in 37 C.F.R. § 42.24(a)(1)(i).

Date: January 17, 2025

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e), 42.105, the undersigned hereby certifies that true and correct copies of the above-captioned PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 10,379,116, all associated exhibits, and Petitioner's Power of Attorney were served in their entireties on January 17, 2025, upon the Patent Owner at the correspondence address of record for the subject patent as listed on the USPTO's Patent Center via Priority Mail Express®:

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Date: January 17, 2025

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