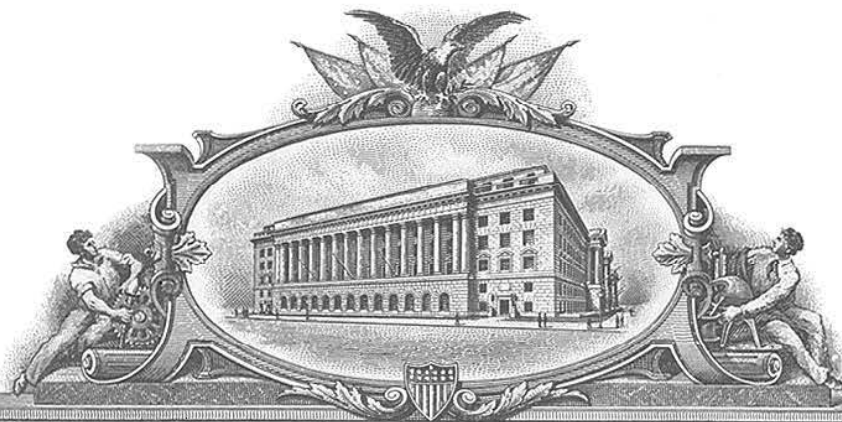


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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	C67508 1170US.1
		Application Number	
Title of Invention	A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE		
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	C67508 1170US.1
		Application Number	
Title of Invention	A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE		
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Title of the Invention	A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE		
Attorney Docket Number	C67508 1170US.1	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	5	Suggested Figure for Publication (if any)	

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	C67508 1170US.1
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Title of Invention	A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE		

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Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

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Phone Number		Fax Number	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	C67508 1170US.1
		Application Number	
Title of Invention	A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE		
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Signature	/Michael L. Gencarella/			Date (YYYY-MM-DD)	2013-12-06
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		Application Number	
Title of Invention	A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE		

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR LETTERS PATENT

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TITLE:

A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING
TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE

BACKGROUND OF THE INVENTION

Field of Invention

The present invention relates generally to the field of load distribution. More specifically, the present invention is related to a system and method for dividing and
5 synchronizing a processing task across multiple processing elements/processors in hardware.

Discussion of Related Art

In the prior art, the processing load (of a processing element) to determine what
10 command to issue is relatively high. The processing load to determine what command to issue can be partially or fully offloaded to a multiplicity of other processing elements (e.g. processors, processor cores, or custom processing circuitry). However, this distribution of load causes commands to be determined from multiple processing elements. It can become a challenge to ensure the module command queues (FIFOs) are not overfilled,
15 thus synchronization is required amongst the multiplicity of processing elements. In the prior art, such synchronization is performed using software techniques, such as semaphores and mutexes to a shared available space count variable in memory. However, this takes additional processing time, making this process non-optimal. To further compound the problem, there may be a need to keep the time from command issue to
20 execution minimized, which tends to keep the command queue shallow.

Embodiments of the present invention are an improvement over prior art systems and methods.

SUMMARY OF THE INVENTION

5 In one embodiment, the present invention provides a system for dividing and synchronizing a processing task across a plurality of processing elements comprising: an input queue implemented in hardware; an output queue implemented in hardware; a first processing element having access to the input queue and the output queue; at least one second processing element in communication with the first processing element; a reservation register implemented in hardware storing a value indicative of available space
10 in a command queue, the reservation register accessible by both the first processing element and the at least second processing element; computer storage storing instructions, which when executed by the at least one second processing element: accesses the reservation register and reads the stored value; determines when the read value indicates
15 available space in the input queue for the first processing element to issue a command; notifies the first processing element to issue the command to the input queue; and wherein the first processing element receives notification from the at least second processing element regarding issuing the command, issues the command to the input queue, and receives a response corresponding to the command from the output queue.

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In another embodiment, the present invention provides a system for dividing and synchronizing a processing task across a plurality of processing elements comprising: an input queue implemented in hardware; an output queue implemented in hardware; a first processing element having access to the input queue and the output queue; at least one
5 second processing element in communication with the input queue; a reservation register implemented in hardware storing a value indicative of available space in a command queue, the reservation register accessible by both the first processing element and the at least second processing element; computer storage storing instructions, which when executed by the at least one second processing element: accesses the reservation register
10 and reads the stored value; determines when the read value indicates available space in the input queue for the first processing element to issue a command; issue the command to the input queue; and wherein the first processing element receives a response corresponding to the command from the output queue.

15 In another embodiment, the present invention provides for a system for dividing and synchronizing a processing task across a plurality of processing elements comprising: an input queue implemented in hardware; an output queue implemented in hardware; a first processing element having access to the input queue and the output queue; at least one second processing element in communication with the input queue and the output
20 queue; a reservation register implemented in hardware storing a value indicative of available space in a command queue, the reservation register accessible by both the first

processing element and the at least second processing element; computer storage storing instructions, which when executed by the at least one second processing element: accesses the reservation register and reads the stored value; determines when the read value indicates available space in the input queue for the first processing element to issue
5 a command; issue the command to the input queue; and receives a response corresponding to the command from the output queue.

BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure, in accordance with one or more various examples, is described in detail with reference to the following figures. The drawings are provided for purposes of illustration only and merely depict examples of the disclosure. These
5 drawings are provided to facilitate the reader's understanding of the disclosure and should not be considered limiting of the breadth, scope, or applicability of the disclosure. It should be noted that for clarity and ease of illustration these drawings are not necessarily made to scale.

FIG. 1 depicts a non-limiting example of where the present invention's
10 "reservation" register is accessible by a plurality of processing elements.

FIG. 2 depicts another non-limiting example of where the present invention's reservation register is accessible by a plurality of processors.

FIG. 3 through FIG. 5 depict the various embodiments of the present invention for dividing and synchronizing a processing task across a plurality of processing elements.

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DESCRIPTION OF THE PREFERRED EMBODIMENTS

While this invention is illustrated and described in a preferred embodiment, the invention may be produced in many different configurations. There is depicted in the drawings, and will herein be described in detail, a preferred embodiment of the invention,
20 with the understanding that the present disclosure is to be considered as an exemplification of the principles of the invention and the associated functional

specifications for its construction and is not intended to limit the invention to the embodiment illustrated. Those skilled in the art will envision many other possible variations within the scope of the present invention.

5 Note that in this description, references to “one embodiment” or “an embodiment” mean that the feature being referred to is included in at least one embodiment of the invention. Further, separate references to “one embodiment” in this description do not necessarily refer to the same embodiment; however, neither are such embodiments mutually exclusive, unless so stated and except as will be readily apparent to those of
10 ordinary skill in the art. Thus, the present invention can include any variety of combinations and/or integrations of the embodiments described herein.

The invention considers the case where software must issue commands to a hardware module. In this case the processing load to determine what command to issue is
15 relatively high, and there may also be additional background tasks necessary. The processing load to determine what command to issue can be partially or fully offloaded to a multiplicity of other processing elements (e.g. processors, processor cores, or custom processing circuitry). However, this distribution of load causes commands to be determined from multiple processing elements. It can become a challenge to ensure the
20 module command queues (FIFOs) are not overfilled, thus synchronization is required amongst the multiplicity of processing elements. As noted above, in the prior art, this

synchronization is performed using software techniques, such as semaphores and mutexes to a shared available space count variable. However, this takes additional processing time. To further compound the problem there may be a need to keep the time from command issue to execution minimized, which tends to keep the command queue shallow.

5

The present invention provides a shared counter resource (e.g., a register) in the hardware representing how much free space there is in the command queue, accessible to one or more processing elements. FIG. 1 depicts a non-limiting example of where the present invention's "reservation" register **102** is accessible by a plurality of processing
10 elements 1 through n, **104** through **108**. It should be noted that while the discussion herein references processing elements, the teachings of the present invention equally applies to disparate processors as well. For example, FIG. 2 depicts another non-limiting example of where the present invention's reservation register **202** is accessible by a plurality of processors 1 through n, **204** through **208**.

15

When a processing element reads the "reservation" register, the hardware automatically decrements the available free space by a preconfigured amount (e.g., 1) and returns the value of the free space immediately prior to the read / reservation. If the read returns 0 (or a number less than the preconfigured amount), there is insufficient free space
20 to satisfy the request. In the event there is insufficient space to satisfy the request the reservation register may be configured to reserve however much space is available or to

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not reserve any space at all. At times there may exist a need to test if a reservation would succeed without actually making a reservation, a “peek” at the reservation register. This peek may be implemented via an alternate, mirrored, reservation register that mirrors the value of the reservation register that can be read by a processing element, but does not actually make a reservation, whereby the alternate register does not automatically modify the available free space. Any number of processing elements may read these registers (hardware synchronizes these reads internally to ensure they do not overlap using standard arbitration for multiple processing elements). Thus there is a guarantee of not “over subscribing” the command queue. When commands actually are issued to the queue following a reservation, they will remain there until the hardware module or entity consuming those commands is able to process them, removing them from the queue. Once they are removed from the queue, the reservation free space will be incremented automatically by the hardware. This reservation technique allows for a fixed or variable time delay between making the reservation for space in the queue and actually issuing the command to the queue, and allows for different processing elements to make the decision(s) and to then issue the command(s). The reservation free space is different from the actual real time free space in the command queue, since space is “reserved” prior to actually being consumed by an issued command.

20 The software, therefore, need only read a register and check its return value to make a reservation and know if it was successful or not. All arbitration and mutual

exclusion tasks between multiple processing elements are handled in hardware. There is no need for the software overhead of multiple processing elements handling the synchronization of a shared available space count variable in shared memory or otherwise.

5

In one embodiment there is a single processing element connected to the module's command queue. It is desired to have a single point of responsibility for this hardware module (such as a control interface to a storage processing element) to issue the commands and deal with the responses from the module. However, the processing load to determine all or a subset of commands to issue may be high. This processing load is placed on a separate processing element. The two processing elements communicate in some efficient way (such as through shared memory, etc.). Part of the processing load is to know that there is in fact available space for a command to be issued, thus this second processing element must have visibility to the available free command queue space in addition to the first processing element also having visibility. The second processing element may issue its commands directly or may return its decision back to the first processing element to be sequenced with any commands the first processing element is able to issue on its own, but even in such a scenario, the first processing element would have to make its own space reservations for those commands it is able to issue on its own. Therefore, any processing element that determines a command must first make a reservation prior to issuing the command or informing another processing element of the

20

decision to issue a command. The hardware will then automatically, without software intervention, update the reserved free space when the command is actually removed from the queue for consumption. In the event space is reserved but later it is determined that space is not to be used (e.g., decided to not issue the command after space had been reserved), there may be a mechanism available to a processing element to return reserved space back to the pool (via another register action) making it available space again.

This mechanism need not be a “command” queue but any resource shared among a plurality of processing elements. For example, the mechanism may be used to implement a hardware-based mutex or hardware-based semaphore. The shared resource itself may be implemented in hardware, software, or a combination of the two. Though the reservations in the embodiments discussed reserve one entry in the queue at a time, this is not necessary, as it could be some other number (e.g., a plurality of commands, the amount of queue space consumed by a command, or some other number relevant to the shared resource). Such other numbers are within the scope of the present invention.

In the event a reservation fails, it would be possible for the hardware to internally and automatically queue (e.g., post) the attempt and generate an interrupt to the requesting processor element at some later point in time to indicate it was then successful, alleviating the requesting processing element from having to poll for space to be available.

In one embodiment, as depicted in FIG. 3, the present invention provides a system for dividing and synchronizing a processing task across a plurality of processing elements comprising: an input queue **308** implemented in hardware **314**; an output queue **312** also
5 implemented in hardware **314**; a first processing element **302** having access to the input queue **308** (over communication link **316**) and the output queue **312** (over communication link **320**); one or more additional processing elements (e.g., processing element #2 - **304** through processing element #n - **306**) in communication with the first processing element **302** (depicted by inter-processor communication link **326** between
10 processing element #1 **302** and processing element #2 **304** and depicted by inter-processor communication link **328** between processing element #1 **302** and processing element #n **306**) (while FIG. 3 depicts a simplistic link **326** or **328** between two processing elements, it should be noted that there may be other components disposed along this path, where such components may not be used to limit the scope of the present
15 invention); a reservation register **310** implemented in hardware **314** storing a value indicative of available space in input queue **308**, the reservation register **310** accessible by both the first processing element **302** (over communication link **318**) and one or more additional processing elements (e.g., processing element #2 - **304** through processing element #n - **306**) (e.g., over communication links **322** and **324**); computer storage
20 storing instructions, which when executed by one of the additional processing elements

(e.g., processing element #2 - **304** through processing element #n - **306**): accesses the reservation register **310** and reads the stored value; the stored value automatically decremented in hardware by 1 in concert with the read to make a reservation of space **300**; determines when the read value indicates available space in the input queue **308** for the first processing element **302** to issue a command; notifies the first processing element **302** to issue the command to the input queue **308**; and wherein the first processing element **302** receives notification from one of the additional processing elements (e.g., processing element #2 - **304** through processing element #n - **306**) regarding issuing the command, issues the command to the input queue **308**, and receives a response corresponding to the command from the output queue **312**. In the event the first processing element **302** decides not to issue the command (e.g., overrides the decision to issue the command), it would return the space previously reserved for the command by writing to a reservation return register, depicted as the return mechanism **334**, the amount of space it wishes to return (i.e. increments the reservation register **310** by this amount).

Also shown in FIG. 3, another additional processing element **330** takes the command from the input queue **308** causing the reservation register to increase its available space automatically in hardware **332** by the amount of space now created based on the removal of the command from the input queue. The additional processing element **330** then executes the command and notifies the output queue **312** of the execution where it then issues the response to the first processing element **302**. In one non-limiting example, the

system is implemented as part of a storage area network (SAN) controller, providing the command queue for the commands the storage controller is to issue to a storage media device. In another non-limiting example, the system is implemented as part of a network attached storage (NAS) controller, providing the command queue for the commands the
5 storage controller is to issue to a storage media device.

In one embodiment, as depicted in FIG. 4, the present invention provides a system for dividing and synchronizing a processing task across a plurality of processing elements comprising: an input queue **408** implemented in hardware **414**; an output queue **412** also
10 implemented in hardware **414**; a first processing element **402** having access to the input queue **408** (over communication link **416**) and the output queue **412** (over communication link **420**); one or more additional processing elements (e.g., processing element #2 - **404** through processing element #n – **406**) optionally in communication with the first processing element **402** (depicted by inter-processor communication link **426**
15 between processing element #1 **402** and processing element #2 **404** and depicted by inter-processor communication link **428** between processing element #1 **402** and processing element #n **406**) (while FIG. 4 depicts a simplistic link **426** or **428** between two processing elements, it should be noted that there may be other components disposed along this path, where such components may not be used to limit the scope of the present
20 invention) and having access to the input queue **408** (over communication links **436** and **438**); a reservation register **410** implemented in hardware **414** storing a value indicative

of available space in input queue **408**, the reservation register **410** accessible by both the first processing element **402** (over communication link **418**) and one or more additional processing elements (e.g., processing element #2 - **404** through processing element #n - **406**) (e.g., over communication links **422** and **424**); computer storage storing instructions, which when executed by one of the additional processing elements (e.g., processing element #2 - **404** through processing element #n - **406**): accesses the reservation register **410** and reads the stored value; the stored value automatically decremented in hardware by 1 in concert with the read to make a reservation of space **400**; determines when the read value indicates available space in the input queue **408** to issue a command; issue the command to the input queue **408** (this may be optionally done on behalf of the first processing element **402** or the first processing element can issue the command (or another command) into the input queue **408** by itself over communication link **416**); and wherein the first processing element **402** receives a response corresponding to the command from the output queue **412**. In the event the additional processing element (e.g., processing element #2 - **404** through processing element #n - **406**) decides not to issue the command after reserving space, it would return the space previously reserved for the command by writing to a reservation return register, depicted as the return mechanism **434**, the amount of space it wishes to return (i.e. increments the reservation register **410** by this amount). Also shown in FIG. 4, another additional processing element **430** that takes the command from the input queue **408** causing the reservation register to increase its available space

automatically in hardware **432** by the amount of space now created based on the removal of the command from the input queue. The, the additional processing element **430** executes the command, and notifies the output queue **412** of the execution where it then issues the response to the first processing element **402**. In one non-limiting example, the
5 system is implemented as part of a storage area network (SAN) controller. In another non-limiting example, the system is implemented as part of a network attached storage (NAS) controller.

In one embodiment, as depicted in FIG. 5, the present invention provides a system
10 for dividing and synchronizing a processing task across a plurality of processing elements comprising: an input queue **508** implemented in hardware **514**; an output queue **512** also implemented in hardware **514**; a first processing element **502** having access to the input queue **508** (over communication link **516**) and the output queue **512** (over communication link **520**); one or more additional processing elements (e.g., processing
15 element #2 - **504** through processing element #n – **506**) optionally in communication with the first processing element **502** (depicted by inter-processor communication link **526** between processing element #1 **502** and processing element #2 **504** and depicted by inter-processor communication link **528** between processing element #1 **502** and processing element #n **506**) (while FIG. 5 depicts a simplistic link **526** or **528** between two
20 processing elements, it should be noted that there may be other components disposed along this path, where such components may not be used to limit the scope of the present

invention) and having access to the input queue **508** (over communication links **536** and **538**) and the output queue **512** (over communication links **540** and **542**); a reservation register **510** implemented in hardware **514** storing a value indicative of available space in input queue **508**, the reservation register **510** accessible by both the first processing
5 element **502** (over communication link **518**) and one or more additional processing elements (e.g., processing element #2 - **504** through processing element #n - **506**) (e.g., over communication links **522** and **524**); computer storage storing instructions, which when executed by one of the additional processing elements (e.g., processing element #2 - **504** through processing element #n - **506**): accesses the reservation register **510** and reads
10 the stored value; the stored value automatically decremented in hardware by 1 in concert with the read to make a reservation of space **500**; determines when the read value indicates available space in the input queue **508** to issue a command; issue the command to the input queue **508** (this may be optionally done on behalf of the first processing element **502** or the first processing element can issue the command (or another command)
15 into the input queue **508** by itself over communication link **516**); and wherein the first processing element **502**, or the one or more additional processing elements **504** or **506**, receives a response (over communication links **520**, **540** or **542**) corresponding to the command from the output queue **512**. In the event the additional processing element (e.g., processing element #2 - **504** through processing element #n - **506**) decides not to
20 issue the command after reserving space, it would return the space previously reserved for

the command by writing to a reservation return register, depicted as the return mechanism **534**, the amount of space it wishes to return (i.e. increments the reservation register **510** by this amount). Also shown in FIG. 5, another additional processing element **530** that takes the command from the input queue **508** causing the reservation register to increase
5 its available space automatically in hardware **532** by the amount of space now created based on the removal of the command from the input queue. The additional processing element **530** then executes the command, and notifies the output queue **512** of the execution where it then issues the response to the first processing element **502**. In one non-limiting example, the system is implemented as part of a storage area network (SAN)
10 controller. In another non-limiting example, the system is implemented as part of a network attached storage (NAS) controller.

The above-described features and applications can be implemented as software processes that are specified as a set of instructions recorded on a computer readable
15 storage medium (also referred to as computer readable medium). When these instructions are executed by one or more processing element(s) (e.g., one or more processors, cores of processors, or other processing elements), they cause the processing element(s) to perform the actions indicated in the instructions. Embodiments within the scope of the present disclosure may also include tangible and/or non-transitory computer-readable
20 storage media for carrying or having computer-executable instructions or data structures stored thereon. Such non-transitory computer-readable storage media can be any

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available media that can be accessed by a general purpose or special purpose computer, including the functional design of any special purpose processor. By way of example, and not limitation, such non-transitory computer-readable media can include flash memory, RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or
5 other magnetic storage devices, or any other medium which can be used to carry or store desired program code means in the form of computer-executable instructions, data structures, or processor chip design. The computer readable media does not include carrier waves and electronic signals passing wirelessly or over wired connections.

10 Computer-executable instructions include, for example, instructions and data which cause a general purpose computer, special purpose computer, or special purpose processing device to perform a certain function or group of functions. Computer-executable instructions also include program modules that are executed by computers in stand-alone or network environments. Generally, program modules include routines,
15 programs, components, data structures, objects, and the functions inherent in the design of special-purpose processors, etc. that perform particular tasks or implement particular abstract data types. Computer-executable instructions, associated data structures, and program modules represent examples of the program code means for executing steps of the methods disclosed herein. The particular sequence of such executable instructions or
20 associated data structures represents examples of corresponding acts for implementing the functions described in such steps.

5 A computer program (also known as a program, software, software application, script, or code) can be written in any form of programming language, including compiled or interpreted languages, declarative or procedural languages, and it can be deployed in any form, including as a stand-alone program or as a module, component, subroutine, object, or other unit suitable for use in a computing environment. A computer program may, but need not, correspond to a file in a file system. A program can be stored in a portion of a file that holds other programs or data (e.g., one or more scripts stored in a markup language document), in a single file dedicated to the program in question, or in
10 multiple coordinated files (e.g., files that store one or more modules, sub programs, or portions of code). A computer program can be deployed to be executed on one computer or on multiple computers that are located at one site or distributed across multiple sites and interconnected by a communication network.

15 These functions described above can be implemented in digital electronic circuitry, in computer software, firmware or hardware. The techniques can be implemented using one or more computer program products. The processes and logic flows can be performed by one or more programmable processors and by one or more programmable logic circuitry. General and special purpose computing devices and
20 storage devices can be interconnected through communication networks.

Some implementations include electronic components, for example microprocessors, storage and memory that store computer program instructions in a machine-readable or computer-readable medium (alternatively referred to as computer-readable storage media, machine-readable media, or machine-readable storage media).

5 Some examples of such computer-readable media include RAM, ROM, read-only compact discs (CD-ROM), recordable compact discs (CD-R), rewritable compact discs (CD-RW), read-only digital versatile discs (e.g., DVD-ROM, dual-layer DVD-ROM), a variety of recordable/rewritable DVDs (e.g., DVD-RAM, DVD-RW, DVD+RW, etc.), flash memory (e.g., SD cards, mini-SD cards, micro-SD cards, etc.), magnetic or solid

10 state hard drives, read-only and recordable Blu-Ray[®] discs, ultra density optical discs, any other optical or magnetic media, and floppy disks. The computer-readable media can store a computer program that is executable by at least one processing element and includes sets of instructions for performing various operations. Examples of computer programs or computer code include machine code, for example is produced by a

15 compiler, and files including higher-level code that are executed by a computer, an electronic component, or a microprocessor using an interpreter.

While the above discussion primarily refers to microprocessor or multi-core processors that execute software, some implementations are performed by one or more

20 integrated circuits, for example application specific integrated circuits (ASICs) or field programmable gate arrays (FPGAs). In some implementations, such integrated circuits

execute instructions that are stored on/within the circuit itself. In some implementations, such as with FPGAs, software may be used to describe hardware circuits, an example of which are FPGA programming files. Such FPGA programming files may also include computer programs, machine code, microcode, firmware, and other software. The FPGA programming files may be stored within an FPGA, ASIC, computer-readable storage media, machine-readable media, or machine-readable storage media.

As used in this specification and any claims of this application, the terms “computer”, “server”, “processor”, and “memory” all refer to electronic or other technological devices. These terms exclude people or groups of people. For the purposes of the specification, the terms display or displaying means displaying on an electronic device. As used in this specification and any claims of this application, the terms “computer readable medium” and “computer readable media” are entirely restricted to tangible, physical objects that store information in a form that is readable by a computer. These terms exclude any wireless signals, wired download signals, and any other ephemeral signals.

Those of skill in the art will appreciate that other embodiments of the disclosure may be practiced in network computing environments with many types of computer system configurations, including personal computers, hand-held devices, multi-processor systems, ASIC-based systems, FPGA-based systems, microprocessor-based or

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programmable consumer electronics, network PCs, minicomputers, mainframe computers, and the like. Embodiments may also be practiced in distributed computing environments where tasks are performed by local and remote processing devices that are linked (either by hardwired links, wireless links, or by a combination thereof) through a communications network. In a distributed computing environment, program modules may be located in both local and remote memory storage devices.

It is understood that any specific order or hierarchy of steps in the processes disclosed is an illustration of example approaches. Based upon design preferences, it is understood that the specific order or hierarchy of steps in the processes may be rearranged, or that all illustrated steps be performed. Some of the steps may be performed simultaneously. For example, in certain circumstances, multitasking and parallel processing may be advantageous. Moreover, the separation of various system components illustrated above should not be understood as requiring such separation, and it should be understood that the described program components and systems can generally be integrated together in a single software product or packaged into multiple software products.

Various modifications to these aspects will be readily apparent, and the generic principles defined herein may be applied to other aspects. Thus, the claims are not intended to be limited to the aspects shown herein, but is to be accorded the full scope

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consistent with the language claims, where reference to an element in the singular is not intended to mean “one and only one” unless specifically so stated, but rather “one or more.” Unless specifically stated otherwise, the term “some” refers to one or more. Pronouns in the masculine (e.g., his) include the feminine and neuter gender (e.g., her and
5 its) and vice versa. Headings and subheadings, if any, are used for convenience only and do not limit the subject technology.

A phrase, for example, an “aspect” does not imply that the aspect is essential to the subject technology or that the aspect applies to all configurations of the subject
10 technology. A disclosure relating to an aspect may apply to all configurations, or one or more configurations. A phrase, for example, an aspect may refer to one or more aspects and vice versa. A phrase, for example, a “configuration” does not imply that such configuration is essential to the subject technology or that such configuration applies to all configurations of the subject technology. A disclosure relating to a configuration may
15 apply to all configurations, or one or more configurations. A phrase, for example, a configuration may refer to one or more configurations and vice versa.

The various embodiments described above are provided by way of illustration only and should not be construed to limit the scope of the disclosure. Those skilled in the
20 art will readily recognize various modifications and changes that may be made to the principles described herein without following the example embodiments and applications

illustrated and described herein, and without departing from the spirit and scope of the disclosure.

While this specification contains many specific implementation details, these
5 should not be construed as limitations on the scope of any invention or of what may be
claimed, but rather as descriptions of features that may be specific to particular
embodiments of particular inventions. Certain features that are described in this
specification in the context of separate embodiments can also be implemented in
combination in a single embodiment. Conversely, various features that are described in
10 the context of a single embodiment can also be implemented in multiple embodiments
separately or in any suitable subcombination. Moreover, although features may be
described above as acting in certain combinations and even initially claimed as such, one
or more features from a claimed combination can in some cases be excised from the
combination, and the claimed combination may be directed to a subcombination or
15 variation of a subcombination.

Similarly, while operations are depicted in the drawings in a particular order, this
should not be understood as requiring that such operations be performed in the particular
order shown or in sequential order, or that all illustrated operations be performed, to
20 achieve desirable results. In certain circumstances, multitasking and parallel processing
may be advantageous. Moreover, the separation of various system components in the

embodiments described above should not be understood as requiring such separation in all embodiments, and it should be understood that the described program components and systems can generally be integrated together in a single software product or packaged into multiple software products.

5

As noted above, particular embodiments of the subject matter have been described, but other embodiments are within the scope of the following claims. For example, the actions recited in the claims can be performed in a different order and still achieve desirable results. As one example, the processes depicted in the accompanying
10 figures do not necessarily require the particular order shown, or sequential order, to achieve desirable results. In certain implementations, multitasking and parallel processing may be advantageous.

CONCLUSION

A system and method has been shown in the above embodiments for the effective implementation of a system and method for dividing and synchronizing a processing task across multiple processing elements/processors in hardware. While various preferred
5 embodiments have been shown and described, it will be understood that there is no intent to limit the invention by such disclosure, but rather, it is intended to cover all modifications falling within the spirit and scope of the invention, as defined in the appended claims. For example, the present invention should not be limited by software/program, computing environment, or specific computing hardware.

10

CLAIMS

1. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:
- an input queue implemented in hardware;
 - 5 an output queue implemented in hardware;
 - a first processing element having access to said input queue and said output queue;
 - at least one second processing element in communication with said first processing element;
 - 10 a reservation register implemented in hardware storing a value indicative of available space in a command queue, said reservation register accessible by both said first processing element and said at least second processing element;
 - computer storage storing instructions, which when executed by said at least one second processing element:
 - 15 accesses said reservation register and reads said stored value;
 - determines when said read value indicates available space in said input queue for said first processing element to issue a command;
 - notifies said first processing element to issue said command to said input queue; and
 - 20 wherein said first processing element receives notification from said at least second processing element regarding issuing the command, issues said command to said

input queue, and receives a response corresponding to said command from said output queue.

2. The system of claim 1, wherein said command queue is a FIFO buffer.

5

3. The system of claim 1, wherein said system is part of a storage area network (SAN) controller.

4. The system of claim 1, wherein said system is part of a network attached storage (NAS) controller.

10

5. The system of claim 1, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element.

15

6. The system of claim 1, wherein at least one third processing element executes said command and notifies said output queue to issue said response.

7. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

20

an input queue implemented in hardware;

an output queue implemented in hardware;

a first processing element having access to said input queue and said output queue;

at least one second processing element in communication with said input queue;

5 a reservation register implemented in hardware storing a value indicative of available space in a command queue, said reservation register accessible by both said first processing element and said at least second processing element;

computer storage storing instructions, which when executed by said at least one second processing element:

10 accesses said reservation register and reads said stored value;

determines when said read value indicates available space in said input queue for said first processing element to issue a command;

issue said command to said input queue; and

wherein said first processing element receives a response corresponding to said command from said output queue.

15

8. The system of claim 7, wherein said command queue is a FIFO buffer.

9. The system of claim 7, wherein said system is part of a storage area network (SAN) controller.

20

10. The system of claim 7, wherein said system is part of a network attached storage (NAS) controller.

11. The system of claim 7, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element.

12. The system of claim 7, wherein at least one third processing element executes said command and notifies said output queue to issue said response.

10

13. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

an input queue implemented in hardware;

an output queue implemented in hardware;

15 a first processing element having access to said input queue and said output queue;

at least one second processing element in communication with said input queue and said output queue;

20 a reservation register implemented in hardware storing a value indicative of available space in a command queue, said reservation register accessible by both said first processing element and said at least second processing element;

computer storage storing instructions, which when executed by said at least one second processing element:

accesses said reservation register and reads said stored value;

determines when said read value indicates available space in said

5 input queue for said first processing element to issue a command;

issue said command to said input queue; and

receives a response corresponding to said command from said output queue.

10 14. The system of claim 13, wherein said command queue is a FIFO buffer.

15 15. The system of claim 13, wherein said system is either part of a storage area network (SAN) controller.

16 16. The system of claim 13, wherein said system is part of a network attached storage (NAS) controller.

17. The system of claim 13, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing
20 element.

18. The system of claim 13, wherein at least one third processing element executes said command and notifies said output queue to issue said response.

ABSTRACT OF THE DISCLOSURE

A shared counter resource, such as a register, is disclosed in the hardware, where the register representing how much free space there is in the command queue is accessible to one or more processing elements. When a processing element reads the “reservation”
5 register, the hardware automatically decrements the available free space by a preconfigured amount (e.g., 1) and returns the value of the free space immediately prior to the read / reservation. If the read returns 0 (or a number less than the preconfigured amount), there was insufficient free space to satisfy the request. In the event there was insufficient space to satisfy the request the reservation register may be configured to
10 reserve however much space was available or to not reserve any space at all. Any number of processing elements may read these registers and various scenarios are described where the input and output queues are accessible via various processing elements.

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE
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As the below named inventor, I hereby declare that:

This declaration is directed to: ☒ The attached application, or☐ United States application or PCT international application number _____
filed on _____.

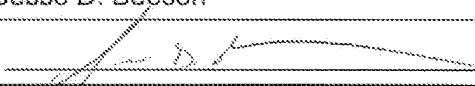
The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

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LEGAL NAME OF INVENTORInventor: Jesse D. Beeson Date (Optional): _____Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE
-------------------------------	--

As the below named inventor, I hereby declare that:

This declaration is directed to: ☒ The attached application, or
☐ United States application or PCT international application number _____
 filed on _____.

The above-identified application was made or authorized to be made by me.

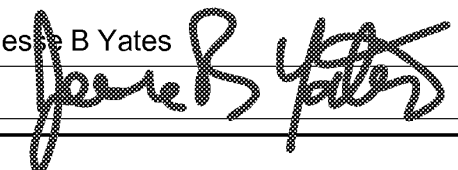
I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than **five (5)** years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Jesse B Yates Date (Optional) : _____
 Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form **or must have been previously filed**. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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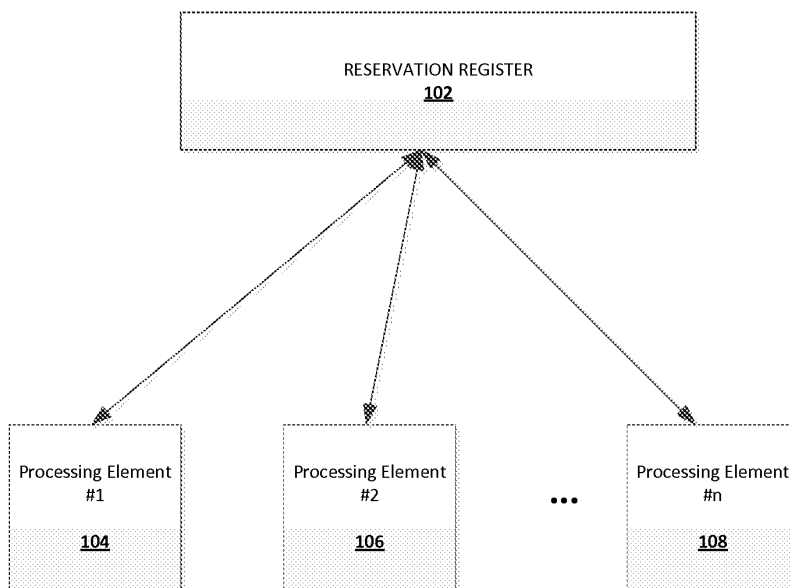


FIG. 1

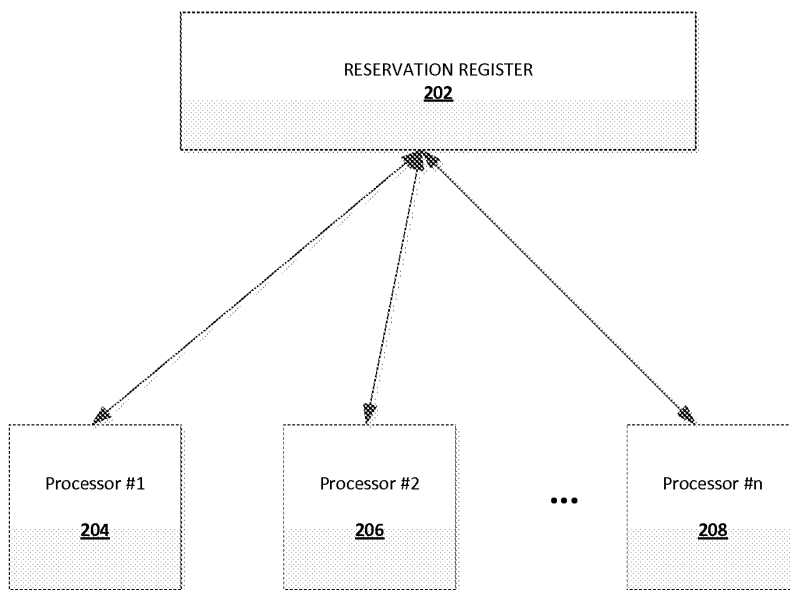


FIG. 2

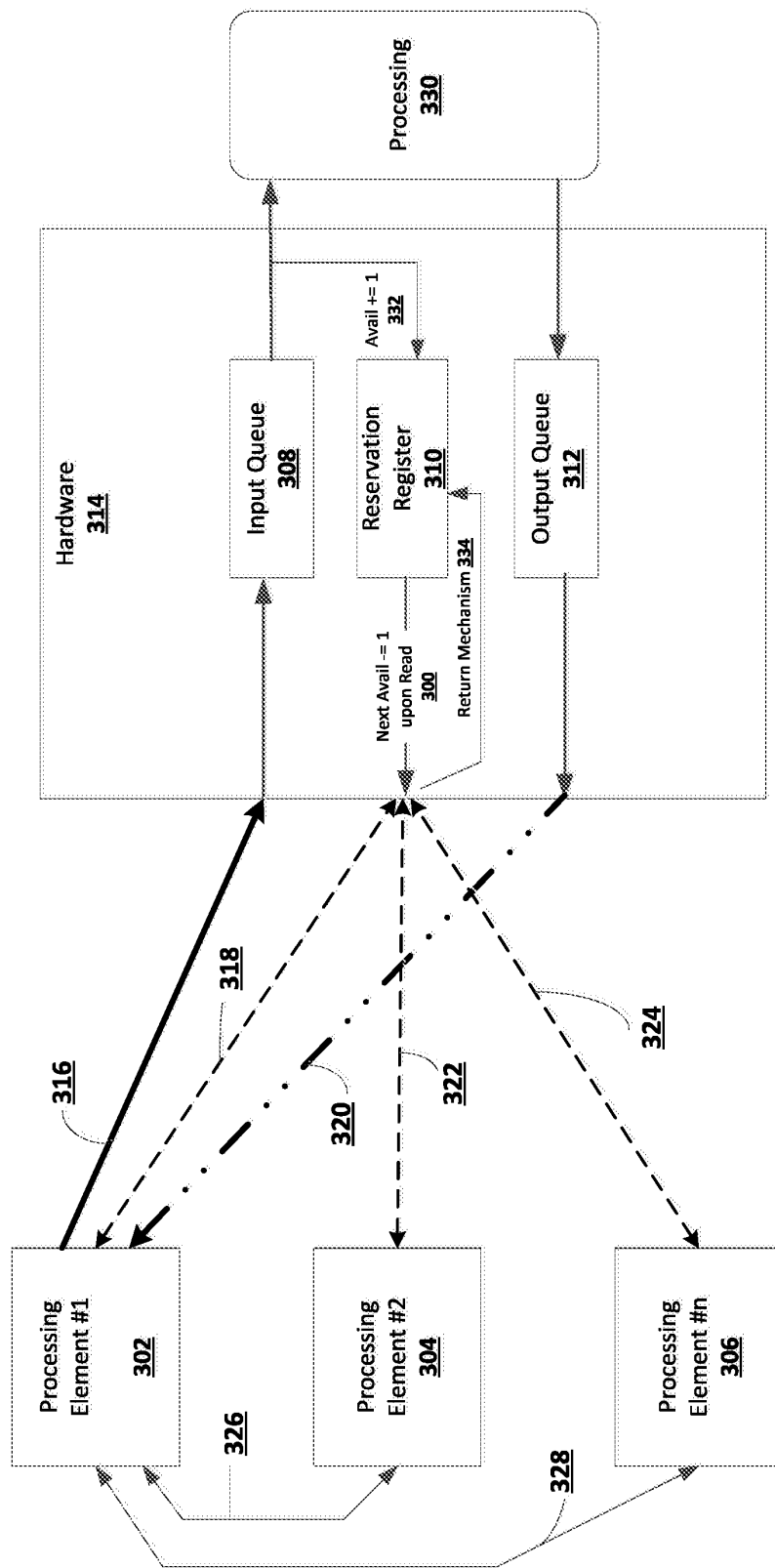


FIG. 3

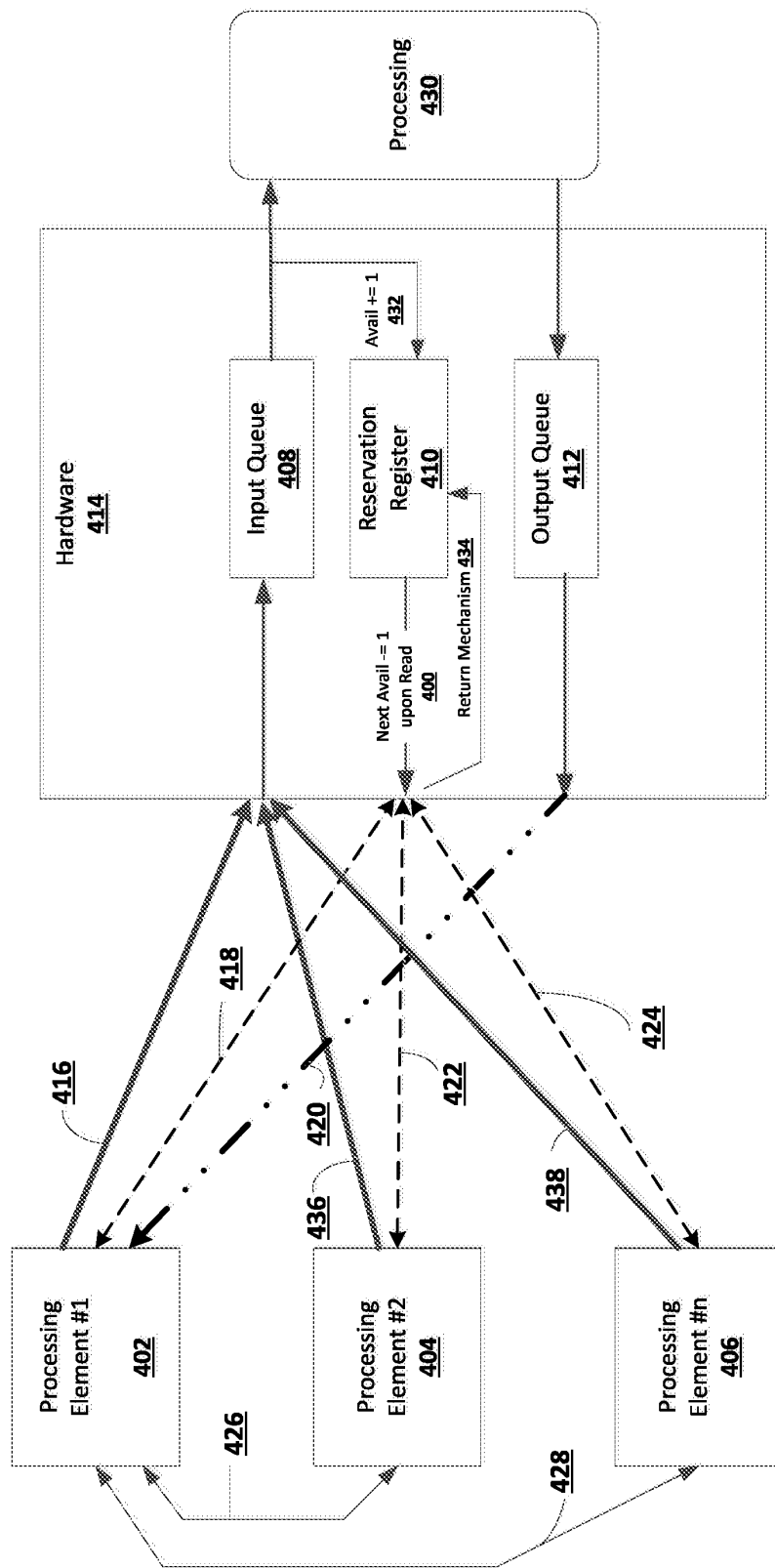


FIG. 4

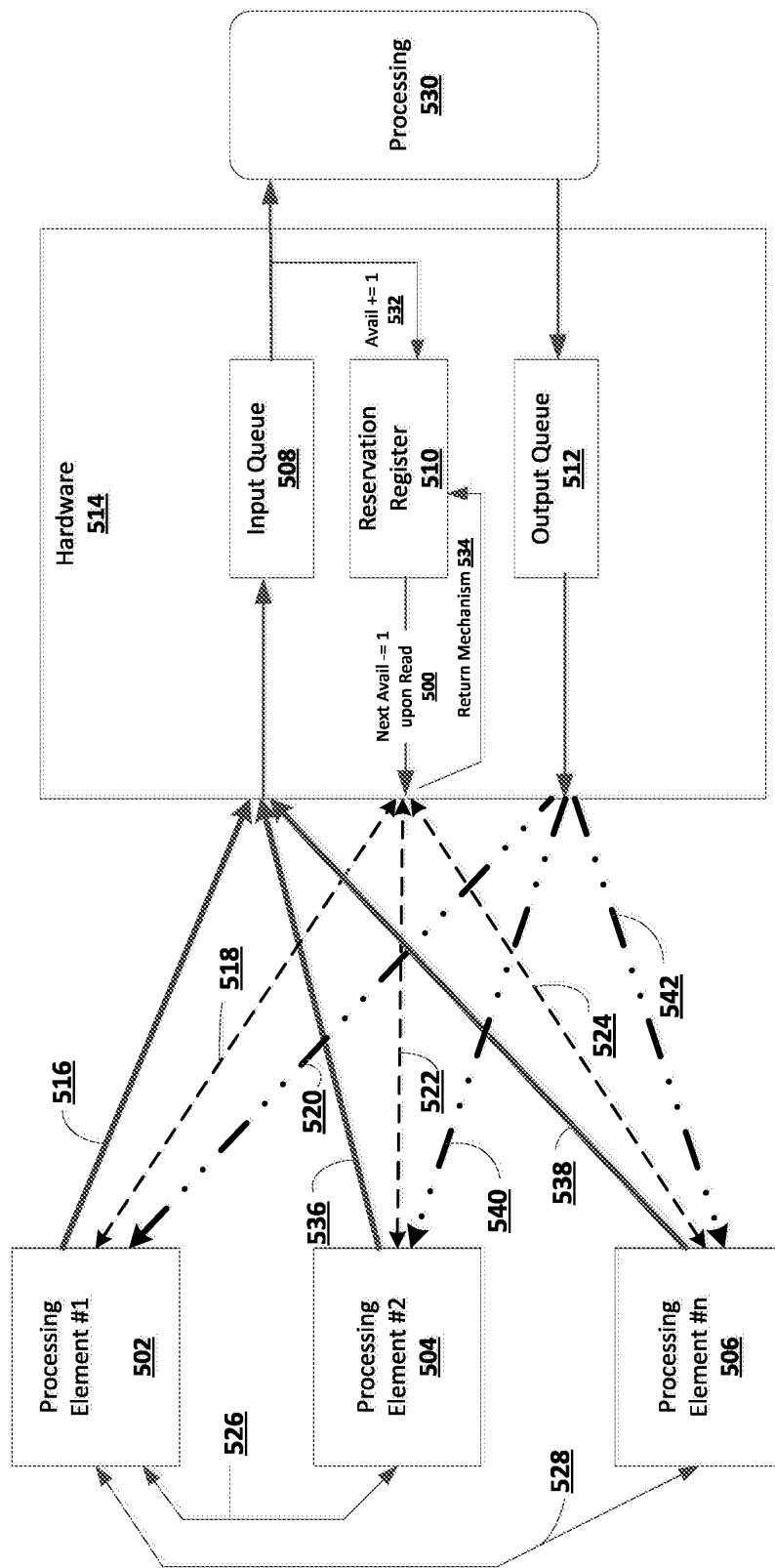


FIG. 5

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE		
First Named Inventor/Applicant Name:		Jesse D. Beeson		
Filer:		Michael L. Gencarella/Bindi Patel		
Attorney Docket Number:		C67508 1170US.1		
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility filing Fee (Electronic filing)	4011	1	70	70
Utility Search Fee	2111	1	300	300
Utility Examination Fee	2311	1	360	360
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				730

Electronic Acknowledgement Receipt	
EFS ID:	17595526
Application Number:	14099844
International Application Number:	
Confirmation Number:	3222
Title of Invention:	A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE
First Named Inventor/Applicant Name:	Jesse D. Beeson
Customer Number:	26158
Filer:	Michael L. Gencarella/Sheryl Bernardo
Filer Authorized By:	Michael L. Gencarella
Attorney Docket Number:	C67508 1170US.1
Receipt Date:	06-DEC-2013
Filing Date:	
Time Stamp:	20:47:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$730
RAM confirmation Number	7390
Deposit Account	090528
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
-----------------	----------------------	-----------	-------------------------------------	------------------	------------------

1	Application Data Sheet	ADS.pdf	1245832 dfde5e9e2052766eab0ab190e4b3244127a92a0b	no	7
Warnings:					
Information:					
2	Specification	App_CVP0020_12.pdf	182748 1324867d9eb05fc87b5e934b87e6365c0f36a8f3	no	34
Warnings:					
Information:					
3	Oath or Declaration filed	Dec.pdf	566395 29cd7b2ee2430f2a517af842d1b5f0fc7637f3e9	no	2
Warnings:					
Information:					
4	Drawings-only black and white line drawings	Dwg_CVP0020_12.pdf	541998 decac87eee1c31b4ac2b9182f17e5dc505214cd3	no	5
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	33295 bf37c8d851889063ceae1cd0894c59650bf18e6a	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			2570268		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

SCORE Placeholder Sheet for IFW Content

Application Number: 14099844

Document Date: 12/06/2013

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

- Drawings – Other than Black and White Line Drawings

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

To access the documents in the SCORE database, refer to instructions below.

At the time of document entry (noted above):

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- External customers may access SCORE content via the Public and Private PAIR interfaces.

Form Revision Date: September 30, 2013

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 14/099,844				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	70		N/A				
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	300		N/A				
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	360		N/A				
TOTAL CLAIMS (37 CFR 1.16(j))	18	minus 20 = *	x 40 =	0.00	OR					
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *	x 210 =	0.00						
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00						
				TOTAL		TOTAL				
* If the difference in column 1 is less than zero, enter "0" in column 2.				730						
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
14/099,844	12/06/2013	2189	730	C67508 1170US.1	18	3

CONFIRMATION NO. 3222

26158
WOMBLE CARLYLE SANDRIDGE & RICE, LLP
ATTN: IP DOCKETING
P.O. BOX 7037
ATLANTA, GA 30357-0037

FILING RECEIPT



OC000000065682699

Date Mailed: 01/02/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Jesse D. BEESON, Johns Creek, GA;
Jesse B. YATES, Atlanta, GA;

Applicant(s)

Concurrent Ventures, LLC, Johns Creek, GA

Assignment For Published Patent Application

Concurrent Ventures, LLC, Johns Creek, GA

Power of Attorney: None

Domestic Applications for which benefit is claimed - None.

A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the Patent Prosecution Highway program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 12/19/2013

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/099,844**

Projected Publication Date: Request for Non-Publication Acknowledged

page 1 of 3

Non-Publication Request: Yes

Early Publication Request: No

**** SMALL ENTITY ****

Title

SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS
MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
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Jan 02, 2014 05:35:14 AM

Dear PAIR Customer:

WOMBLE CARLYLE SANDRIDGE & RICE, LLP
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P.O. BOX 7037
ATLANTA, GA 30357-0037
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 26158 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

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Application	Document	Mailroom Date	Attorney Docket No.
14099844	APP.FILE.REC	01/02/2014	C67508 1170US.1

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Thank you for prompt attention to this notice,

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NOTICE OF ALLOWANCE AND FEE(S) DUE

26158 7590 08/19/2014
WOMBLE CARLYLE SANDRIDGE & RICE, LLP
ATTN: IP DOCKETING
P.O. BOX 7037
ATLANTA, GA 30357-0037

EXAMINER

SNYDER, STEVEN G

ART UNIT

PAPER NUMBER

2184

DATE MAILED: 08/19/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/099,844	12/06/2013	Jesse D. BEESON	C67508 1170US.1	3222

TITLE OF INVENTION: SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$480	\$0	\$0	\$480	11/19/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
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Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26158 7590 08/19/2014
WOMBLE CARLYLE SANDRIDGE & RICE, LLP
ATTN: IP DOCKETING
P.O. BOX 7037
ATLANTA, GA 30357-0037

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/099,844	12/06/2013	Jesse D. BEESON	C67508 1170US.1	3222

TITLE OF INVENTION: SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$480	\$0	\$0	\$480	11/19/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
SNYDER, STEVEN G	2184	710-005000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/099,844	12/06/2013	Jesse D. BEESON	C67508 1170US.1	3222
26158 7590 08/19/2014 WOMBLE CARLYLE SANDRIDGE & RICE, LLP ATTN: IP DOCKETING P.O. BOX 7037 ATLANTA, GA 30357-0037			EXAMINER SNYDER, STEVEN G	
			ART UNIT 2184	PAPER NUMBER

DATE MAILED: 08/19/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/099,844	Applicant(s) BEESON ET AL.	
	Examiner STEVEN SNYDER	Art Unit 2184	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the application filed December 6, 2013.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-18. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)	5. ☒ Examiner's Amendment/Comment
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____
4. ☒ Interview Summary (PTO-413), Paper No./Mail Date <u>20140813</u> .	

/STEVEN SNYDER/ Primary Examiner, Art Unit 2184	
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DETAILED ACTION

This is in response to the application filed on December 6, 2013 in which claims 1 – 18 are presented for examination.

Status of Claims

Claims 1 – 18 are pending, of which claims 1, 7, and 13 are in independent form.

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Michael Gencarella on 8/13/2014.

The application has been amended as follows:

Claims

1. (Currently Amended) A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

an input queue implemented in hardware;

an output queue implemented in hardware;

a first processing element having access to said input queue and said output queue;

at least one second processing element in communication with said first processing element;

a reservation register implemented in hardware storing a value indicative of available space in ~~a command queue~~ said input queue, said reservation register accessible by both said first processing element and said at least one second processing element;

computer storage storing instructions, which when executed by said at least one second processing element:

- accesses said reservation register and reads said stored value;
- determines when said read value indicates available space in said input queue for said first processing element to issue a command;
- notifies said first processing element to issue said command to said input queue; and

wherein said first processing element receives notification from said at least one second processing element regarding issuing the command, issues said command to said input queue, and receives a response corresponding to said command from said output queue.

2. (Currently Amended) The system of claim 1, wherein said ~~command queue~~ input queue is a first-in-first-out (FIFO) buffer.

3. (Previously Presented) The system of claim 1, wherein said system is part of a storage area network (SAN) controller.

4. (Previously Presented) The system of claim 1, wherein said system is part of a network attached storage (NAS) controller.

5. (Previously Presented) The system of claim 1, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element.

6. (Previously Presented) The system of claim 1, wherein at least one third processing element executes said command and notifies said output queue to issue said response.

7. (Currently Amended) A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

an input queue implemented in hardware;

an output queue implemented in hardware;

a first processing element having access to said input queue and said output

queue;

at least one second processing element in communication with said input queue;

a reservation register implemented in hardware storing a value indicative of available space in ~~a command queue~~ said input queue, said reservation register accessible by both said first processing element and said at least one second processing element;

computer storage storing instructions, which when executed by said at least one second processing element:

receives a command from said first processing element;

accesses said reservation register and reads said stored value;

determines when said read value indicates available space in said input queue ~~for said first processing element~~ to issue a said command;

~~issue~~ issues said command to said input queue on behalf of said first processing element; and

wherein said first processing element receives a response corresponding to said command from said output queue.

8. (Currently Amended) The system of claim 7, wherein ~~said command queue~~ input queue is a first-in-first-out (FIFO) buffer.

9. (Previously Presented) The system of claim 7, wherein said system is part of a storage area network (SAN) controller.

10. (Previously Presented) The system of claim 7, wherein said system is part of a network attached storage (NAS) controller.

11. (Previously Presented) The system of claim 7, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element.

12. (Previously Presented) The system of claim 7, wherein at least one third processing element executes said command and notifies said output queue to issue said response.

13. (Currently Amended) A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

- an input queue implemented in hardware;

- an output queue implemented in hardware;

- a first processing element having access to said input queue and said output queue;

- at least one second processing element in communication with said input queue and said output queue;

- a reservation register implemented in hardware storing a value indicative of available space in ~~a command queue~~ said input queue, said reservation register

accessible by both said first processing element and said at least one second processing element;

computer storage storing instructions, which when executed by said at least one second processing element:

receives a command from said first processing element;

accesses said reservation register and reads said stored value;

determines when said read value indicates available space in said

input queue ~~for said first processing element~~ to issue a said command;

~~issue~~ issues said command to said input queue on behalf of said first processing element; and

receives a response corresponding to said command from said output queue.

14. (Currently Amended) The system of claim 13, wherein ~~said command queue~~ input queue is a first-in-first-out (FIFO) buffer.

15. (Previously Presented) The system of claim 13, wherein said system is either part of a storage area network (SAN) controller.

16. (Previously Presented) The system of claim 13, wherein said system is part of a network attached storage (NAS) controller.

17. (Previously Presented) The system of claim 13, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element.

18. (Previously Presented) The system of claim 13, wherein at least one third processing element executes said command and notifies said output queue to issue said response.

Allowable Subject Matter

3. **Claims 1 – 18** are allowed.

4. The following is an examiner's statement of reasons for allowance: The primary reason for the allowance of the claims in this application is the inclusion of the specific details of a reservation register that is accessed by the second processing element and the feature of the second processing element notifying the first processing element to issue a command to the input queue if the reservation register value indicates that there is available space in the input queue, as are now included in independent claim 1, in combination with the other elements recited, which is not found in the prior art of record.

5. The primary reason for the allowance of the claims in this application is the inclusion of the specific details of a reservation register that is accessed by the second processing element and the feature of the second processing element receiving a command from the first processing element and the second processing element issuing said command to the input queue if the reservation register value indicates that there is

available space in the input queue, as are now included in independent claims 7 and 13, in combination with the other elements recited, which is not found in the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent Applications 2006/0221087 and 2010/0149195.

U.S. Patents 5,638,535 5,696,990 5,740,406 5,805,930 5,924,126 5,805,930 5,924,126 6,081,854 8,704,838 and 8,730,248.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **STEVEN SNYDER** whose telephone number is **(571)270-1971**. The examiner can normally be reached on Mon. - Fri. 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai can be reached on (571) 272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Steven G Snyder/
Primary Examiner, Art Unit 2184

Notice of References Cited	Application/Control No. 14/099,844	Applicant(s)/Patent Under Reexamination BEESON ET AL.	
	Examiner STEVEN SNYDER	Art Unit 2184	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2006/0221087	10-2006	Diard, Franck R.	345/505
*	B	US-2010/0149195	06-2010	Fernando et al.	345/505
*	C	US-5,638,535	06-1997	Rosenthal et al.	711/165
*	D	US-5,696,990	12-1997	Rosenthal et al.	710/29
*	E	US-5,740,406	04-1998	Rosenthal et al.	711/169
*	F	US-5,805,930	09-1998	Rosenthal et al.	710/57
*	G	US-5,924,126	07-1999	Rosenthal et al.	711/207
*	H	US-6,081,854	06-2000	Priem et al.	710/37
*	I	US-8,704,838	04-2014	Fernando et al.	345/505
*	J	US-8,730,248	05-2014	Sasaki et al.	345/503
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	14/099844	US-PGPUB; USPAT	ADJ	OFF	2014/08/04 09:22
S2	38	(command queue) WITH (overflow\$3 or overfill\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 10:31
S3	40	register WITH (empty or available) WITH space WITH (command NEAR3 (queue or fifo or buffer))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 10:32
S4	0	S2 and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 10:32
S5	271	(command NEAR3 (buffer or fifo or queue)) WITH (overflow\$3 or overfill\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 10:33
S6	6	S3 and S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 10:33
S7	811704	(second or multiple or other or another or plural\$5) NEAR4 (processor or (processing element) or microprocessor or controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 11:06
S8	17	S3 and S7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 11:07
S9	1834	distribut\$3 WITH load WITH S7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 11:12

S10	0	S5 and S9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 11:12
S11	1069807	(second or multiple or other or another or plural\$5) NEAR4 (processor or (processing element) or microprocessor or controller or core)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 11:26
S12	2067	distribut\$3 WITH load WITH S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 11:26
S13	0	S5 and S12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 11:26
S14	118	S5 and S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 11:27
S15	90482	(input NEAR3 (buffer or fifo or queue)) SAME (output NEAR3 (buffer or fifo or queue))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 11:27
S16	2963	S15 SAME S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 11:28
S17	4	(distribut\$3 WITH load) SAME S16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 11:28
S18	1073323	(second or multiple or other or another or plural\$5) NEAR4 (processor or (processing element) or microprocessor or controller or core or (execution unit))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 12:04
S19	2078	distribut\$3 WITH load WITH S18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 12:05

S20	0	S5 and S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 12:05
S21	2978	S15 SAME S18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 12:05
S22	4	(distribut\$3 WITH load) SAME S21	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 12:05
S23	32992	(buffer or fifo or queue) WITH (overflow\$3 or overfill\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 12:59
S24	230	S23 and S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 12:59
S25	721	register WITH (empty or available) WITH space WITH (queue or fifo or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 13:00
S26	0	S24 and S25	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 13:00
S27	2	S25 and S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 13:01
S28	4	S6 AND ((G06F5/06 OR G06F3/06 OR G06F13/12).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 13:19
S29	0	S2 AND ((G06F5/06 OR G06F3/06 OR G06F13/12).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 13:19

S30	4	S19 AND ((G06F5/06 OR G06F3/06 OR G06F13/12).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 13:22
S31	5	S2 and ((storage area network) or (network attached storage))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 13:27
S32	7	("20040223003" "20060192983" "20060221087" "20070159488" "5757385" "6222550" "6828985").PN.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2014/08/04 15:06
S33	154550	((divid\$3 or balanc\$3) NEAR4 load)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 15:13
S34	115	S25 and S33	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 15:14
S35	7070	(710/5 710/18 710/19 710/57 710/310).ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/04 15:14
S36	4589	(711/147 711/152).ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/04 15:14
S37	20323	((G06F3/0656 OR G06F3/0659 OR G06F3/067 OR G06F5/06 OR G06F13/1673).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 15:16
S38	2	S34 and (S35 or S36 or S37)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2014/08/04 15:16

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S39	27	(queue and ((available or empty) space) and command).clm.	US- PGPUB; USPAT;	ADJ	ON	2014/08/04 13:34

			UPAD			
S40	84	((queue or buffer or fifo) and ((available or empty) space) and command).clm.	US-PGPUB; USPAT; UPAD	ADJ	ON	2014/08/04 13:34
S41	374664	((second or multiple or other or another or plural\$5) NEAR4 (processor or (processing element) or microprocessor or controller or core or (execution unit))).clm.	US-PGPUB; USPAT; UPAD	ADJ	ON	2014/08/04 13:34
S42	20	S40 and S41	US-PGPUB; USPAT; UPAD	ADJ	ON	2014/08/04 13:35
S43	5	S40 AND ((G06F3/0659).CPC.)	US-PGPUB; USPAT; UPAD	ADJ	ON	2014/08/04 13:49
S44	11	S40 AND ((G06F3/0656 OR G06F3/0659 OR G06F3/067).CPC.)	US-PGPUB; USPAT; UPAD	ADJ	ON	2014/08/04 13:51
S45	17	S40 AND ((G06F3/0656 OR G06F3/0659 OR G06F5/06 OR G06F13/1673).CPC.)	US-PGPUB; USPAT; UPAD	ADJ	ON	2014/08/04 13:54
S46	2721	710/5.ccls.	US-PGPUB; USPAT; UPAD	ADJ	ON	2014/08/04 14:00
S47	1	S40 and S46	US-PGPUB; USPAT; UPAD	ADJ	ON	2014/08/04 14:00
S48	3439	(710/18 710/19 710/57 710/310).ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/04 14:05
S49	8	S40 and (S46 or S48)	US-PGPUB; USPAT; UPAD	ADJ	ON	2014/08/04 14:05
S50	3922	(711/147 711/152).ccls.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/04 14:07
S51	1	S40 and S50	US-PGPUB; USPAT; UPAD	ADJ	ON	2014/08/04 14:07
S52	12238	((divid\$3 or balanc\$3) NEAR4 load).clm.	US-PGPUB; USPAT; UPAD	ADJ	ON	2014/08/04 15:12
S53	3	S40 and S52	US-PGPUB; USPAT; UPAD	ADJ	ON	2014/08/04 15:12

8/13/2014 3:03:28 PM

C:\Users\ssnyder1\Documents\EAST\Workspaces\14_099844.wsp

Search Notes 	Application/Control No. 14099844	Applicant(s)/Patent Under Reexamination BEESON ET AL.
	Examiner STEVEN SNYDER	Art Unit 2184

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Inventor Name Search in PALM	8/4/2014	S. Snyder
Keyword Search in EAST (US and Foreign Databases)	8/4/2014	S. Snyder
Google Search	8/4/2014	S. Snyder
CPC keyword search in EAST	8/4/2014	S. Snyder

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
710	5, 18, 19, 57, 310	8/4/2014	S. Snyder
711	147, 152	8/4/2014	S. Snyder

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<i>Index of Claims</i> 	Application/Control No. 14099844	Applicant(s)/Patent Under Reexamination BEESON ET AL.
	Examiner STEVEN SNYDER	Art Unit 2184

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant
 ☐ CPA
 ☐ T.D.
 ☐ R.1.47

CLAIM		DATE									
Final	Original	08/13/2014									
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	2	=									
	3	=									
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	16	=									
	17	=									
	18	=									



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BIB DATA SHEET

CONFIRMATION NO. 3222

SERIAL NUMBER 14/099,844	FILING or 371(c) DATE 12/06/2013 RULE	CLASS 710	GROUP ART UNIT 2184	ATTORNEY DOCKET NO. C67508 1170US.1		
APPLICANTS Concurrent Ventures, LLC, Johns Creek, GA, Assignee (with 37 CFR 1.172 Interest); INVENTORS Jesse D. BEESON, Johns Creek, GA; Jesse B. YATES, Atlanta, GA; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** ** SMALL ENTITY ** 12/19/2013						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/STEVEN G SNYDER/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY GA	SHEETS DRAWINGS 5	TOTAL CLAIMS 18	INDEPENDENT CLAIMS 3
ADDRESS WOMBLE CARLYLE SANDRIDGE & RICE, LLP ATTN: IP DOCKETING P.O. BOX 7037 ATLANTA, GA 30357-0037 UNITED STATES						
TITLE SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE						
FILING FEE RECEIVED 730	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			

Issue Classification 	Application/Control No. 14099844	Applicant(s)/Patent Under Reexamination BEESON ET AL.	
	Examiner STEVEN SNYDER	Art Unit 2184	

CPC					
Symbol				Type	Version
G06F		3	0659	F	2013-01-01
G06F		3	067	I	2013-01-01
G06F		3	061	I	2013-01-01

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	18	
/STEVEN SNYDER/ Primary Examiner.Art Unit 2184	8/13/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3

Issue Classification 	Application/Control No. 14099844	Applicant(s)/Patent Under Reexamination BEESON ET AL.
	Examiner STEVEN SNYDER	Art Unit 2184

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION														
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED									
710		5				G	0	6	F	3 / 00 (2006.01.01)										
CROSS REFERENCE(S)																				
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																			
710	18	19	57	310																
711	147	152																		

NONE		Total Claims Allowed:	
		18	
(Assistant Examiner)	(Date)		
/STEVEN SNYDER/ Primary Examiner. Art Unit 2184	8/13/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3

Issue Classification 	Application/Control No. 14099844	Applicant(s)/Patent Under Reexamination BEESON ET AL.
	Examiner STEVEN SNYDER	Art Unit 2184

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17												
	2		18												
	3														
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	10														
	11														
	12														
	13														
	14														
	15														
	16														

NONE		Total Claims Allowed:	
(Assistant Examiner)		18	
(Date)			
/STEVEN SNYDER/ Primary Examiner. Art Unit 2184		8/13/2014	
(Primary Examiner)		(Date)	
		O.G. Print Claim(s)	O.G. Print Figure
		1	3

To: IPDocketing@WCSR.COM,,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
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Application	Document	Mailroom Date	Attorney Docket No.
14099844	NOA	08/19/2014	C67508 1170US.1
	INTV.SUM.EX	08/19/2014	C67508 1170US.1
	892	08/19/2014	C67508 1170US.1

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26158 7590 08/19/2014
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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/099,844	12/06/2013	Jesse D. BEESON	C67508 1170US.1	3222

TITLE OF INVENTION: SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$480	\$0	\$0	\$480	11/19/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
SNYDER, STEVEN G	2184	710-005000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Womble Carlyle Sandridge & Rice
LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.111. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Concurrent Ventures, LLC

Johns Creek, GA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
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5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29
☐ Applicant asserting small entity status. See 37 CFR 1.27
☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Michael L. Gencarella/

Date November 19, 2014

Typed or printed name Michael L. Gencarella

Registration No. 44,703

Electronic Patent Application Fee Transmittal				
Application Number:		14099844		
Filing Date:		06-Dec-2013		
Title of Invention:		SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE		
First Named Inventor/Applicant Name:		Jesse D. BEESON		
Filer:		Michael L. Gencarella/Sheryl Bernardo		
Attorney Docket Number:		C67508 1170US.1		
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	2501	1	480	480
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				480

Electronic Acknowledgement Receipt	
EFS ID:	20743118
Application Number:	14099844
International Application Number:	
Confirmation Number:	3222
Title of Invention:	SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE
First Named Inventor/Applicant Name:	Jesse D. BEESON
Customer Number:	26158
Filer:	Michael L. Gencarella/Sheryl Bernardo
Filer Authorized By:	Michael L. Gencarella
Attorney Docket Number:	C67508 1170US.1
Receipt Date:	19-NOV-2014
Filing Date:	06-DEC-2013
Time Stamp:	19:22:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$480
RAM confirmation Number	5221
Deposit Account	090528
Authorized User	
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Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	C67508_1170_Statement.pdf	82645	no	1
			ffa7bdcec2b7ec8a6046958072adc2c2a2aaecd9		
Warnings:					
Information:					
2	Issue Fee Payment (PTO-85B)	C67508_1170_Issue_Fee_Final.pdf	142270	no	1
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Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30677	no	2
			481ed51200d96cf9d0f28bcc72316cbefab9c438		
Warnings:					
Information:					
Total Files Size (in bytes):			255592		
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of)
Jesse D. BEESON) Examiner: SNYDER, STEVEN G.
Application No: 14/099,844)
Filed: 12-06-2013) Art Unit: 2184
For: SYSTEM AND METHOD FOR DIVIDING AND)
SYNCHRONIZING A PROCESSING TASK ACROSS)
MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN)
HARDWARE)
Atty. Docket No: C67508 1170US.1
Date: November 19, 2014

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop ISSUE FEE
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Reasons for allowance are warranted in instances in which “the record of the prosecution as a whole does not make clear his or her reasons for allowing a claim or claims” 37 CFR 1.104(c). In the above identified application, Applicants believe the record as a whole makes clear the reasons for allowance and therefore no statement by the Examiner is necessary or warranted.

Accordingly, Applicants assert that the record should be limited only by the terms utilized in the record. Applicants submit these comments to ensure that the claims are properly construed based upon the limitations that are present and/or to ensure that none of the claims is interpreted so as to include any additional claim limitations not found in respective claims.

Should the Examiner have any questions concerning this matter, please contact the undersigned.

Respectfully submitted,
WOMBLE CARLYLE SANDRIDGE & RICE, LLP

/Michael L. Gencarella/

Michael L. Gencarella, Esq.
Reg. No. 44,703

Customer Number 26158

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RESCISSION OF PREVIOUS NONPUBLICATION REQUEST

(35 U.S.C. 122(b)(2)(B)(ii))

AND, IF APPLICABLE,

NOTICE OF FOREIGN FILING

(35 U.S.C. 122(b)(2)(B)(iii))

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Mail Stop PG Pub

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

FAX: (571) 273-8300

Application Number	14/099,844
Filing Date	12-06-2013
First Named Inventor	Jesse D. BEESON
Title	SYSTEM AND METHOD FOR DIVIDING AND
Atty Docket Number	C67508 1170US.1
Art Unit	2184
Examiner	SNYDER, STEVEN G.

A request that the above-identified application not be published under 35 U.S.C. 122(b) (nonpublication request) was included with the above-identified application on filing pursuant to 35 U.S.C. 122(b)(2)(B)(i).

I hereby **rescind** the previous nonpublication request.

If a notice of foreign or international filing is or will be required by 35 U.S.C. 122(b)(2)(B)(iii) and 37 CFR 1.213(c), I hereby provide such notice. This notice is being provided no later than forty-five (45) days after the date of such foreign or international filing.

If a notice of subsequent foreign or international filing required by 35 U.S.C. 122(b)(2)(B)(iii) and 37 CFR 1.213(c) was not filed within forty-five (45) days after the date of filing of the foreign or international application, the application is ABANDONED, and a petition to revive under 37 CFR 1.137(b) is required. See 37 CFR 1.137(f).

/Michael L. Gencarella/

2014-12-10

Signature

Date

Michael L. Gencarella

44,703

Typed or printed name

Registration Number, if applicable

408-341-3015

Telephone Number

This request must be signed in compliance with 37 CFR 1.33(b).

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Name (Print/Type)

Date

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Electronic Acknowledgement Receipt	
EFS ID:	20923741
Application Number:	14099844
International Application Number:	
Confirmation Number:	3222
Title of Invention:	SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE
First Named Inventor/Applicant Name:	Jesse D. BEESON
Customer Number:	26158
Filer:	Michael L. Gencarella/Sheryl Bernardo
Filer Authorized By:	Michael L. Gencarella
Attorney Docket Number:	C67508 1170US.1
Receipt Date:	10-DEC-2014
Filing Date:	06-DEC-2013
Time Stamp:	16:22:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Rescind Nonpublication Request for Pre Grant Pub	1170_rescind.pdf	65963 f405e2a1ba5d2111e0d2eac8ebc6e83ef81e f627	no	1

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/099,844	12/30/2014	8924596	C67508 1170US.1	3222

26158 7590 12/10/2014
WOMBLE CARLYLE SANDRIDGE & RICE, LLP
ATTN: IP DOCKETING
P.O. BOX 7037
ATLANTA, GA 30357-0037

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Concurrent Ventures, LLC, Johns Creek, GA, Assignee (with 37 CFR 1.172 Interest);
Jesse D. BEESON, Johns Creek, GA;
Jesse B. YATES, Atlanta, GA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

To: IPDocketing@WCSR.COM,,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 26158

Dec 11, 2014 05:30:31 AM

Dear PAIR Customer:

WOMBLE CARLYLE SANDRIDGE & RICE, LLP
ATTN: IP DOCKETING
P.O. BOX 7037
ATLANTA, GA 30357-0037
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 26158 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

Disclaimer:

The list of documents shown below is provided as a courtesy and is not part of the official file wrapper. The content of the images shown in PAIR is the official record.

Application	Document	Mailroom Date	Attorney Docket No.
14099844	ISSUE.NTF	12/10/2014	C67508 1170US.1

To view your correspondence online or update your email addresses, please visit us anytime at <https://sportal.uspto.gov/secure/myportal/privatepair>.

If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov with 'e-Office Action' on the subject line or call 1-866-217-9197 during the following hours:

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/099,844	12/06/2013	Jesse D. BEESON	C67508 1170US.1

CONFIRMATION NO. 3222

26158
WOMBLE CARLYLE SANDRIDGE & RICE, LLP
ATTN: IP DOCKETING
P.O. BOX 7037
ATLANTA, GA 30357-0037

NONPUBLICATION RESCISSION
LETTER



Date Mailed: 12/15/2014

**Communication Regarding Rescission Of
Nonpublication Request and/or Notice of Foreign Filing**

Applicant's rescission of the previously-filed nonpublication request and/or notice of foreign filing is acknowledged. The paper has been reflected in the Patent and Trademark Office's (USPTO's) computer records so that the earliest possible projected publication date can be assigned.

The projected publication date is 06/11/2015.

If applicant rescinded the nonpublication request before or on the date of "foreign filing,"¹ then no notice of foreign filing is required.

If applicant foreign filed the application after filing the above application and before filing the rescission, and the rescission did not also include a notice of foreign filing, then a notice of foreign filing (not merely a rescission) is required to be filed within 45 days of the date of foreign filing. See 35 U.S.C. § 122(b)(2)(B)(iii), and Clarification of the United States Patent and Trademark Office's Interpretation of the Provisions of 35 U.S.C. § 122(b)(2)(B)(iii)-(iv), 1272 Off. Gaz. Pat. Office 22 (July 1, 2003).

If a notice of foreign filing is required and is not filed within 45 days of the date of foreign filing, then the application becomes abandoned pursuant to 35 U.S.C. § 122(b)(2)(B)(iii). In this situation, applicant should either file a petition to revive or notify the Office that the application is abandoned. See 37 CFR 1.137(f). Any such petition to revive will be forwarded to the Office of Petitions for a decision. Note that the filing of the petition will not operate to stay any period of reply that may be running against the application.

Questions regarding petitions to revive should be directed to the Office of Petitions at (571) 272-3282.

¹ Note, for purpose of this notice, that "foreign filing" means "filing an application directed to the same invention in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing".

/ctuazon/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

To: IPDocketing@WCSR.COM,,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 26158

Dec 15, 2014 05:25:12 AM

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WOMBLE CARLYLE SANDRIDGE & RICE, LLP
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P.O. BOX 7037
ATLANTA, GA 30357-0037
UNITED STATES

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Application	Document	Mailroom Date	Attorney Docket No.
14099844	M327	12/15/2014	C67508 1170US.1

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Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

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Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA/82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	14/099,844
Filing Date	12-06-2013
First Named Inventor	Jesse D. BEESON
Title	SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE
Art Unit	2184
Examiner Name	SNYDER, STEVEN G
Attorney Docket Number	C67508 1170US.1

SIGNATURE of Applicant or Patent Practitioner

Signature	/Michael L. Gencarella/	Date (Optional)	
Name	Michael L. Gencarella	Registration Number	44,703
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			
NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.			
☒ *Total of <u>1</u> forms are submitted.			

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:



Practitioners associated with Customer Number:

142922

OR



Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number

Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned, according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:



The address associated with Customer Number:

142922

OR

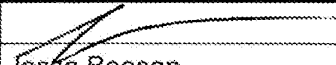
☐	Firm or Individual Name			
	Address			
	City	State	Zip	
	Country			
	Telephone			Email

Assignee Name and Address: Concurrent Ventures, LLC
240 Woodscape Court
Johns Creek, GA 30022-3244

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	15 Nov 2016
Name	Jesse Beeson	Telephone	678-823-2775
Title	Chief Executive Officer of Concurrent Ventures, LLC		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: Concurrent Ventures, LLCApplication No./Patent No.: 14/099,844Filed/Issue Date: 12-06-2013Titled: SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ...Concurrent Ventures, LLC, a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is ____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 031742, Frame 0809, or for which a copy thereof is attached.
- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

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5. From: _____ To: _____

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6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
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☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Michael L. Gencarella/

11-30-2016

Signature

Date

Michael L. Gencarella

44,703

Printed or Typed Name

Title or Registration Number

Electronic Acknowledgement Receipt	
EFS ID:	27657918
Application Number:	14099844
International Application Number:	
Confirmation Number:	3222
Title of Invention:	SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE
First Named Inventor/Applicant Name:	Jesse D. BEESON
Customer Number:	26158
Filer:	Michael L. Gencarella/Dana Beardsley
Filer Authorized By:	Michael L. Gencarella
Attorney Docket Number:	C67508 1170US.1
Receipt Date:	30-NOV-2016
Filing Date:	06-DEC-2013
Time Stamp:	18:30:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		C67508_1170US1_POA_asfiled.pdf	2634263	yes	4
			5ad0ac7a0815c0aaaccd0de918d88818df10443c		

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Power of Attorney	1	2
	Assignee showing of ownership per 37 CFR 3.73	3	4
Warnings:			
Information:			
Total Files Size (in bytes):		2634263	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/099,844	12/06/2013	Jesse D. BEESON	C67508 1170US.1

CONFIRMATION NO. 3222

POA ACCEPTANCE LETTER

142922
WOMBLE CARLYLE SANDRIDGE & RICE, LLP
P.O. Box 7037
Atlanta, GA 30357-0037



Date Mailed: 12/06/2016

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/30/2016.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/sleutchit/

To: IPDocketing@wcsr.com,MGencarella@wcsr.com,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 142922

Dec 06, 2016 03:43:45 AM

Dear PAIR Customer:

WOMBLE CARLYLE SANDRIDGE & RICE, LLP
P.O. Box 7037
Atlanta, GA 30357-0037
UNITED STATES

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Application	Document	Mailroom Date	Attorney Docket No.
14099844	N570	12/06/2016	C67508 1170US.1

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PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT6532618

SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
Name		Execution Date
CONCURRENT VENTURES, LLC		01/15/2021
RECEIVING PARTY DATA		
Name:	XTREAMEDGE, INC.	
Street Address:	240 WOODSCAPE CT	
City:	JOHNS CREEK	
State/Country:	GEORGIA	
Postal Code:	30022	
PROPERTY NUMBERS Total: 28		
Property Type	Number	
Patent Number:	9274722	
Patent Number:	8954614	
Patent Number:	8954615	
Patent Number:	8984172	
Patent Number:	8954616	
Patent Number:	8943243	
Patent Number:	8954617	
Patent Number:	9436404	
Patent Number:	10235096	
Patent Number:	10048895	
Patent Number:	10057346	
Patent Number:	10764618	
Patent Number:	9813313	
Patent Number:	9529767	
Patent Number:	10067904	
Patent Number:	10599605	
Patent Number:	9582455	
Patent Number:	8924596	
Patent Number:	9201597	
Patent Number:	9753658	

Property Type	Number
Patent Number:	10359956
Patent Number:	10873753
Application Number:	14099820
Application Number:	16035674
Application Number:	16035672
Application Number:	16035671
Application Number:	16035670
Application Number:	16035668

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 678-823-2775

Email: jesse.beeson@concurrent-ventures.com

Correspondent Name: JESSE BEESON

Address Line 1: 240 WOODSCAPE CT

Address Line 4: JOHNS CREEK, GEORGIA 30022

NAME OF SUBMITTER:	JESSE BEESON
SIGNATURE:	/Jesse Beeson/
DATE SIGNED:	02/03/2021
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 9

source=XtreamEdge - Patent Assignment (Concurrent) - v3 - signed#page1.tif
source=XtreamEdge - Patent Assignment (Concurrent) - v3 - signed#page2.tif
source=XtreamEdge - Patent Assignment (Concurrent) - v3 - signed#page3.tif
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source=XtreamEdge - Patent Assignment (Concurrent) - v3 - signed#page8.tif
source=XtreamEdge - Patent Assignment (Concurrent) - v3 - signed#page9.tif

PATENT ASSIGNMENT

This Patent Assignment ("Patent Assignment") is made as of January 15, 2021 (the "Effective Date") by and between Concurrent Ventures, LLC, a Georgia limited liability corporation ("Assignor") and XstreamEdge, Inc., a Delaware corporation ("Assignee").

WHEREAS, in connection with and pursuant to that certain Asset Purchase Agreement of even date herewith, by and between Assignor (as the seller) and Assignee (as the purchaser) (the "Purchase Agreement"), all right, title and interest in and to certain intellectual property owned by Assignor is to be transferred to Assignee, specifically the Transferred Patents (as defined in Section 1 below) and the inventions disclosed therein;

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, effective as of the Effective Date:

1. "Transferred Patents" means those patents and/or patent applications listed in Attachment A and any and all patents in the same Patent Family (as defined in Section 2 below) as any of the foregoing patents and/or patent applications, throughout the world.

2. "Patent Family" means a set comprised of all patents and applications that at any time are (a) linked or entitled to be linked through one or more claims of priority pursuant to 35 U.S.C. §§ 120 or 119(e) (the equivalent laws or regulation of any other patent authority) or by a disclaimer issue or (b) that are, or are entitled to be, international or foreign counterparts, reissues, divisionals, renewals, extensions, continuations or continuations-in-part with respect to any other patents and applications in such set.

3. Assignor hereby irrevocably assigns, transfers and sells to Assignee all of Assignor's rights, title and interest in and to the following:

a. Transferred Patents, and the inventions disclosed in any of the foregoing, and all issuances, divisions, continuations, continuations-in-part, reissues, extensions, reexaminations, and renewals thereof;

b. all rights of any kind whatsoever of Assignor accruing under any of the foregoing provided by applicable law of any jurisdiction, by international treaties and conventions, and otherwise throughout the world;

c. any and all royalties, fees, income, payments, and other proceeds now or hereafter due or payable with respect to any and all of the foregoing; and

d. all causes of action and enforcement rights, whether currently pending, filed, or otherwise, for the foregoing, including without limitation all rights to pursue damages, injunctive relief and other remedies for past, current and future infringement.

4. In the event that additional assignment documents are required to accomplish or record the assignment to Assignee of the Transferred Patents in any other country or jurisdiction, Assignor hereby agrees, without further consideration, to execute and deliver such assignments to Assignee.

5. Assignor irrevocably constitutes and appoints Assignee, with full power of substitution, to be its true and lawful attorney, and in its name, place or stead, to execute, acknowledge, swear to and file, all instruments, conveyances, certificates, agreements and other documents, and to take any action which shall be necessary, appropriate or desirable to effectuate the transfer of the Transferred Patents in

accordance with the terms of this Patent Assignment; provided, however, that such power shall be exercised by Assignee only in the event that Assignor fails to take the necessary actions required hereunder to affect or record such transfer, or prosecution of such Transferred Patents within thirty (30) days of Assignee's reasonable written request, or ten (10) days prior to the deadline for taking the required action if earlier. This power of attorney shall be deemed to be coupled with an interest and shall be irrevocable.

6. Assignee shall have the right to file or record this Patent Assignment, and any additional assignment documents as provided above, with the United States Patent and Trademark Office and any other equivalent authority anywhere else in the world.

7. In consideration of the assignments herein, Assignee agrees to pay and shall pay any outstanding amounts and costs currently owed by Assignor for the maintenance and/or prosecution of the Transferred Patents. Effective immediately upon the transfer of Transferred Patents to Assignee, Assignor has no continuing responsibility to pay maintenance costs of the Transferred Patents. Further, effective immediately upon the transfer of Transferred Patents to Assignee, any further fees billed or invoiced to the Assignor relating to the Transferred Patents shall, at the Assignor's discretion, be (a) billed to the Assignee by Assignor or (b) otherwise forwarded to the Assignee for payment.

8. This Patent Assignment shall be binding upon and shall inure to the benefit of the parties hereto and their respective successors and assigns.

9. This Patent Assignment and any claim, controversy, dispute, or cause of action (whether in contract, tort, or otherwise) based upon, arising out of, or relating to this Patent Assignment and the transactions contemplated hereby shall be governed by, and construed in accordance with, the laws of the United States and the State of Delaware, without giving effect to any choice or conflict of law provision or rule (whether of the State of Delaware or any other jurisdiction).

10. This Patent Assignment may be executed in two or more counterparts, each of which shall be deemed an original, but all of which together shall constitute one and the same instrument. The delivery of copies of this Patent Assignment or other documents to be delivered pursuant to this Patent Assignment, including executed signature pages where required, by electronic transmission will constitute effective execution and delivery of this Patent Assignment or such other document for all purposes. Signatures transmitted electronically will constitute original signatures for all purposes.

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IN WITNESS WHEREOF, Assignor and Assignee have executed this Patent Assignment as of the Effective Date.

ASSIGNOR

CONCURRENT VENTURES, LLC

By: Jesse D Beeson
Name: Jesse D. Beeson
Title: Chief Executive Officer & Manager

ASSIGNEE

XTREAMEDGE, INC.

By: Stacy Kenworthy
Name: Stacy Kenworthy
Title: Vice President

Attachment A

Transferred Patents

Ctry	Type	Status	Title	Application Number	Patent Number
US	PRI	Granted	System, method and article of manufacture for monitoring, controlling and improving storage media system performance	14/099,713	9,274,722
US	PRI	Granted	System, method and article of manufacture for monitoring, controlling and improving storage media system performance based on temperature	14/099,723	8,954,614
US	PRI	Granted	System, method and article of manufacture for monitoring, controlling and improving storage media system performance based on temperature ranges	14/099,740	8,954,615
US	PRI	Granted	System, method and article of manufacture for monitoring, controlling and improving storage media system performance based on storage media device fill percentage	14/099,752	8,984,172
US	PRI	Granted	System, method and article of manufacture for monitoring, controlling and improving storage media system performance based on storage media device write rate	14/099,767	8,954,616
US	PRI	Granted	System, method and article of manufacture for monitoring, controlling and improving storage media system performance based on storage media device read rate	14/099,811	8,943,243

US	PRI	Granted	System, method and article of manufacture for monitoring, controlling and improving storage media system performance based on data type	14/099,807	8,954,617
US	PRI	Published	System and method for dynamically load balancing storage media devices based on a minimum performance level	14/099,820	
US	PRI	Granted	System and method for dynamically load balancing across storage media devices having fast access rates	14/099,848	9,436,404
US	PRI	Granted	System and method for dynamically load balancing storage media devices based on an average or discounted average sustained performance level	14/099,846	10,235,096
CN	PCT	Granted	System and method for dynamically load balancing storage media devices based on a mid-range performance level	2014800749511	CN105981351
EP	PCT	Published	System and method for dynamically load balancing storage media devices based on a mid-range performance level	14867506.9	
US	PRI	Granted	System and method for dynamically load balancing storage media devices based on a mid-range performance level	14/099,845	10,048,895
WO	ORD	Expired	System and method for dynamically load balancing storage media devices based on a mid-range performance level	PCT/US2014/069143	
US	PRI	Granted	System, method and article of manufacture for automatic detection and storage/archival of network video	14/099,841	10,057,346

US	PRI	Granted	System, method and article of manufacture for automatic detection and storage/archival of network video in a video-on-demand scenario	14/099,837	10,764,618
US	PRI	Granted	System, method and article of manufacture for automatic detection and storage/archival of network video to offload the load of a video management system (VMS)	14/099,836	9,813,313
CN	PCT	Granted	A system and method for abstracting storage media devices via a full duplex queued command interface	2014800750720	CN105981001
EP	PCT	Published	A system and method for abstracting storage media devices via a full duplex queued command interface	14867130.8	
US	PRI	Granted	System and method for abstracting SATA and/or SAS storage media devices via a full duplex queued command interface to increase performance, lower host overhead, and simplify scaling storage media devices and systems	14/099,833	9,529,767
US	CON	Granted	System and method for abstracting SATA and/or SAS storage media devices via a full duplex queued command interface to increase performance, lower host overhead, and simplify scaling storage media devices and systems	15/388,970	10,067,904

US	CON	Granted	System and method for abstracting SATA and/or SAS storage media devices via a full duplex queued command interface to increase performance, lower host overhead, and simplify scaling storage media devices and systems	16/118,849	10,599,605
WO	ORD	Expired	A system and method for abstracting storage media devices via a full duplex queued command interface	PCT/US2014/069149	
US	PRI	Granted	System and method for abstracting SATA and/or SAS storage media devices via a full duplex queued command interface to increase performance, lower host overhead, and simplify scaling storage media devices and systems	14/099,830	9,582,455
CN	PCT	Granted	System and method for dividing and synchronizing a processing task across multiple processing elements/processors in hardware	2014800738485.00	CN105934744
EP	PCT	Published	System and method for dividing and synchronizing a processing task across multiple processing elements/processors in hardware	14867963.2	
US	PRI	Granted	System and method for dividing and synchronizing a processing task across multiple processing elements/processors in hardware	14/099,844	8,924,596
US	CON	Granted	System and method for dividing and synchronizing a processing task across multiple processing elements/processors in hardware	14/585,003	9,201,597

US	CON	Granted	System and method for dividing and synchronizing a processing task across multiple processing elements/processors in hardware	14/952,320	9,753,658
US	CON	Granted	System and method for dividing and synchronizing a processing task across multiple processing elements/processors in hardware	15/694,468	10,359,956
WO	ORD	Expired	System and method for dividing and synchronizing a processing task across multiple processing elements/processors in hardware	PCT/US2014/069153	
US	PRI	Granted	Hardware defined anything in a platform with swappable pods, message interface, sandboxes and memory superposition	16/035,675	10,873,753
US	PRI	Allowed	Hardware defined anything in a platform with swappable pods, message interface, sandboxes and memory superposition	16/035,674	
US	PRI	Allowed	Optimization for network connections	16/035,672	
US	PRI	Pending	Targeted advertising inserted into individual streaming media feeds or static images	16/035,671	
US	PRI	Allowed	Preprocessing data as it lands on storage media, in a hardware accelerated processing pipeline	16/035,670	
US	PRI	Pending	Hash-based file system	16/035,668	

Signature: *Jesse D Beeson*
Jesse D Beeson (Jan 15, 2021 09:48 EST)

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Stacy Kenworthy (Jan 15, 2021 08:47 EST)

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XtreamEdge - Patent Assignment (Concurrent) - v3

Final Audit Report

2021-01-15

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