



- (51) International Patent Classification:
G06F 9/46 (2006.01)
- (21) International Application Number:
PCT/US2014/069153
- (22) International Filing Date:
8 December 2014 (08.12.2014)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
14/099,844 6 December 2013 (06.12.2013) US
- (71) Applicant: **CONCURRENT VENTURES, LLC**
[US/US]; 240 Woodscape Court, Johns Creek, GA 30022-3244 (US).
- (72) Inventors: **BEESON, Jesse, D**; 240 Woodscape Court, Johns Creek, GA 30022-3244 (US). **YATES, Jesse, B**; 2451 Cumberland Parkway SE Suite 300 #3310, Atlanta, GA 30339 (US).
- (74) Agent: **GENCARELLA, Michael, L**; Womble Carlyle Sandridge & Rice LLP, PO Box 7037, Atlanta, GA 30357 (US).
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,

BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

Published:

- with international search report (Art. 21(3))

(54) Title: A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE

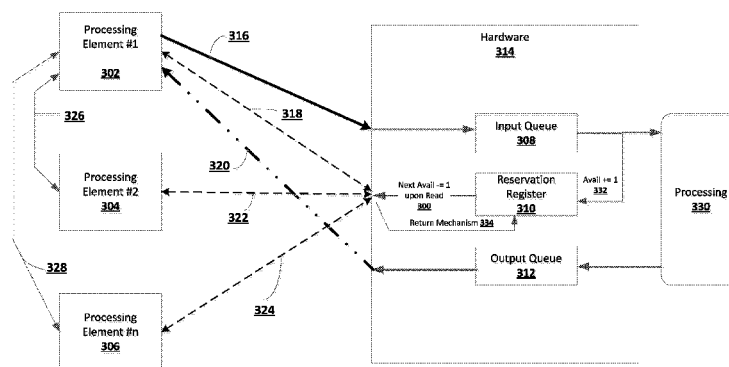


FIG. 3

(57) Abstract: A shared counter resource, such as a register, is disclosed in the hardware, where the register representing how much free space there is in the command queue is accessible to one or more processing elements. When a processing element reads the "reservation" register, the hardware automatically decrements the available free space by a preconfigured amount (e.g., 1) and returns the value of the free space immediately prior to the read / reservation. If the read returns 0 (or a number less than the preconfigured amount), there was insufficient free space to satisfy the request. In the event there was insufficient space to satisfy the request the reservation register may be configured to reserve however much space was available or to not reserve any space at all. Any number of processing elements may read these registers and various scenarios are described where the input and output queues are accessible via various processing elements.

**A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A
PROCESSING TASK ACROSS MULTIPLE PROCESSING
ELEMENTS/PROCESSORS IN HARDWARE**

BACKGROUND OF THE INVENTION

Field of Invention

The present invention relates generally to the field of load distribution. More specifically, the present invention is related to a system and method for dividing and synchronizing a processing task across multiple processing elements/processors in hardware.

Discussion of Related Art

In the prior art, the processing load (of a processing element) to determine what command to issue is relatively high. The processing load to determine what command to issue can be partially or fully offloaded to a multiplicity of other processing elements (e.g. processors, processor cores, or custom processing circuitry). However, this distribution of load causes commands to be determined from multiple processing elements. It can become a challenge to ensure the module command queues (FIFOs) are not overfilled, thus synchronization is required amongst the multiplicity of processing elements. In the prior art, such synchronization is performed using software techniques, such as semaphores and mutexes to a shared available space count variable in memory. However, this takes additional processing time, making this process non-optimal. To further compound the problem, there may be a need to keep the time from command issue to execution minimized, which tends to keep the command queue shallow.

Embodiments of the present invention are an improvement over prior art systems and methods.

SUMMARY OF THE INVENTION

In one embodiment, the present invention provides a system for dividing and synchronizing a processing task across a plurality of processing elements comprising: an input queue implemented in hardware; an output queue implemented in hardware; a first processing element having access to the input queue and the output queue; at least one second processing element in communication with the first processing element; a reservation register implemented in hardware storing a value indicative of available space in a command queue, the reservation register accessible by both the first processing element and the at least second processing element; computer storage storing instructions, which when executed by the at

least one second processing element: accesses the reservation register and reads the stored value; determines when the read value indicates available space in the input queue for the first processing element to issue a command; notifies the first processing element to issue the command to the input queue; and wherein the first processing element receives notification from the at least second processing element regarding issuing the command, issues the command to the input queue, and receives a response corresponding to the command from the output queue.

In another embodiment, the present invention provides a system for dividing and synchronizing a processing task across a plurality of processing elements comprising: an input queue implemented in hardware; an output queue implemented in hardware; a first processing element having access to the input queue and the output queue; at least one second processing element in communication with the input queue; a reservation register implemented in hardware storing a value indicative of available space in a command queue, the reservation register accessible by both the first processing element and the at least second processing element; computer storage storing instructions, which when executed by the at least one second processing element: accesses the reservation register and reads the stored value; determines when the read value indicates available space in the input queue for the first processing element to issue a command; issue the command to the input queue; and wherein the first processing element receives a response corresponding to the command from the output queue.

In another embodiment, the present invention provides for a system for dividing and synchronizing a processing task across a plurality of processing elements comprising: an input queue implemented in hardware; an output queue implemented in hardware; a first processing element having access to the input queue and the output queue; at least one second processing element in communication with the input queue and the output queue; a reservation register implemented in hardware storing a value indicative of available space in a command queue, the reservation register accessible by both the first processing element and the at least second processing element; computer storage storing instructions, which when executed by the at least one second processing element: accesses the reservation register and reads the stored value; determines when the read value indicates available space in the input queue for the first processing element to issue a command; issue the command to the input queue; and receives a response corresponding to the command from the output queue.

BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure, in accordance with one or more various examples, is described in detail with reference to the following figures. The drawings are provided for purposes of illustration only and merely depict examples of the disclosure. These drawings are provided to facilitate the reader's understanding of the disclosure and should not be considered limiting of the breadth, scope, or applicability of the disclosure. It should be noted that for clarity and ease of illustration these drawings are not necessarily made to scale.

FIG. 1 depicts a non-limiting example of where the present invention's "reservation" register is accessible by a plurality of processing elements.

FIG. 2 depicts another non-limiting example of where the present invention's reservation register is accessible by a plurality of processors.

FIG. 3 through FIG. 5 depict the various embodiments of the present invention for dividing and synchronizing a processing task across a plurality of processing elements.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

While this invention is illustrated and described in a preferred embodiment, the invention may be produced in many different configurations. There is depicted in the drawings, and will herein be described in detail, a preferred embodiment of the invention, with the understanding that the present disclosure is to be considered as an exemplification of the principles of the invention and the associated functional specifications for its construction and is not intended to limit the invention to the embodiment illustrated. Those skilled in the art will envision many other possible variations within the scope of the present invention.

Note that in this description, references to "one embodiment" or "an embodiment" mean that the feature being referred to is included in at least one embodiment of the invention. Further, separate references to "one embodiment" in this description do not necessarily refer to the same embodiment; however, neither are such embodiments mutually exclusive, unless so stated and except as will be readily apparent to those of ordinary skill in the art. Thus, the present invention can include any variety of combinations and/or integrations of the embodiments described herein.

The invention considers the case where software must issue commands to a hardware module. In this case the processing load to determine what command to issue is relatively high, and there may also be additional background tasks necessary. The processing load to determine what command to issue can be partially or fully offloaded to a multiplicity of other

processing elements (e.g. processors, processor cores, or custom processing circuitry). However, this distribution of load causes commands to be determined from multiple processing elements. It can become a challenge to ensure the module command queues (FIFOs) are not overfilled, thus synchronization is required amongst the multiplicity of processing elements. As noted above, in the prior art, this synchronization is performed using software techniques, such as semaphores and mutexes to a shared available space count variable. However, this takes additional processing time. To further compound the problem there may be a need to keep the time from command issue to execution minimized, which tends to keep the command queue shallow.

The present invention provides a shared counter resource (e.g., a register) in the hardware representing how much free space there is in the command queue, accessible to one or more processing elements. FIG. 1 depicts a non-limiting example of where the present invention's "reservation" register **102** is accessible by a plurality of processing elements 1 through n, **104** through **108**. It should be noted that while the discussion herein references processing elements, the teachings of the present invention equally applies to disparate processors as well. For example, FIG. 2 depicts another non-limiting example of where the present invention's reservation register **202** is accessible by a plurality of processors 1 through n, **204** through **208**.

When a processing element reads the "reservation" register, the hardware automatically decrements the available free space by a preconfigured amount (e.g., 1) and returns the value of the free space immediately prior to the read / reservation. If the read returns 0 (or a number less than the preconfigured amount), there is insufficient free space to satisfy the request. In the event there is insufficient space to satisfy the request the reservation register may be configured to reserve however much space is available or to not reserve any space at all. At times there may exist a need to test if a reservation would succeed without actually making a reservation, a "peek" at the reservation register. This peek may be implemented via an alternate, mirrored, reservation register that mirrors the value of the reservation register that can be read by a processing element, but does not actually make a reservation, whereby the alternate register does not automatically modify the available free space. Any number of processing elements may read these registers (hardware synchronizes these reads internally to ensure they do not overlap using standard arbitration for multiple processing elements). Thus there is a guarantee of not "over subscribing" the command queue. When commands actually are issued to the queue following a reservation, they will

remain there until the hardware module or entity consuming those commands is able to process them, removing them from the queue. Once they are removed from the queue, the reservation free space will be incremented automatically by the hardware. This reservation technique allows for a fixed or variable time delay between making the reservation for space in the queue and actually issuing the command to the queue, and allows for different processing elements to make the decision(s) and to then issue the command(s). The reservation free space is different from the actual real time free space in the command queue, since space is “reserved” prior to actually being consumed by an issued command.

The software, therefore, need only read a register and check its return value to make a reservation and know if it was successful or not. All arbitration and mutual exclusion tasks between multiple processing elements are handled in hardware. There is no need for the software overhead of multiple processing elements handling the synchronization of a shared available space count variable in shared memory or otherwise.

In one embodiment there is a single processing element connected to the module’s command queue. It is desired to have a single point of responsibility for this hardware module (such as a control interface to a storage processing element) to issue the commands and deal with the responses from the module. However, the processing load to determine all or a subset of commands to issue may be high. This processing load is placed on a separate processing element. The two processing elements communicate in some efficient way (such as through shared memory, etc.). Part of the processing load is to know that there is in fact available space for a command to be issued, thus this second processing element must have visibility to the available free command queue space in addition to the first processing element also having visibility. The second processing element may issue its commands directly or may return its decision back to the first processing element to be sequenced with any commands the first processing element is able to issue on its own, but even in such a scenario, the first processing element would have to make its own space reservations for those commands it is able to issue on its own. Therefore, any processing element that determines a command must first make a reservation prior to issuing the command or informing another processing element of the decision to issue a command. The hardware will then automatically, without software intervention, update the reserved free space when the command is actually removed from the queue for consumption. In the event space is reserved but later it is determined that space is not to be used (e.g., decided to not issue the command after space had been reserved), there may be a mechanism available to a processing element

to return reserved space back to the pool (via another register action) making it available space again.

This mechanism need not be a “command” queue but any resource shared among a plurality of processing elements. For example, the mechanism may be used to implement a hardware-based mutex or hardware-based semaphore. The shared resource itself may be implemented in hardware, software, or a combination of the two. Though the reservations in the embodiments discussed reserve one entry in the queue at a time, this is not necessary, as it could be some other number (e.g., a plurality of commands, the amount of queue space consumed by a command, or some other number relevant to the shared resource). Such other numbers are within the scope of the present invention.

In the event a reservation fails, it would be possible for the hardware to internally and automatically queue (e.g., post) the attempt and generate an interrupt to the requesting processor element at some later point in time to indicate it was then successful, alleviating the requesting processing element from having to poll for space to be available.

In one embodiment, as depicted in FIG. 3, the present invention provides a system for dividing and synchronizing a processing task across a plurality of processing elements comprising: an input queue **308** implemented in hardware **314**; an output queue **312** also implemented in hardware **314**; a first processing element **302** having access to the input queue **308** (over communication link **316**) and the output queue **312** (over communication link **320**); one or more additional processing elements (e.g., processing element #2 - **304** through processing element #n - **306**) in communication with the first processing element **302** (depicted by inter-processor communication link **326** between processing element #1 **302** and processing element #2 **304** and depicted by inter-processor communication link **328** between processing element #1 **302** and processing element #n **306**) (while FIG. 3 depicts a simplistic link **326** or **328** between two processing elements, it should be noted that there may be other components disposed along this path, where such components may not be used to limit the scope of the present invention); a reservation register **310** implemented in hardware **314** storing a value indicative of available space in input queue **308**, the reservation register **310** accessible by both the first processing element **302** (over communication link **318**) and one or more additional processing elements (e.g., processing element #2 - **304** through processing element #n - **306**) (e.g., over communication links **322** and **324**); computer storage storing instructions, which when executed by one of the additional processing

elements (e.g., processing element #2 - **304** through processing element #n - **306**): accesses the reservation register **310** and reads the stored value; the stored value automatically decremented in hardware by 1 in concert with the read to make a reservation of space **300**; determines when the read value indicates available space in the input queue **308** for the first processing element **302** to issue a command; notifies the first processing element **302** to issue the command to the input queue **308**; and wherein the first processing element **302** receives notification from one of the additional processing elements (e.g., processing element #2 - **304** through processing element #n - **306**) regarding issuing the command, issues the command to the input queue **308**, and receives a response corresponding to the command from the output queue **312**. In the event the first processing element **302** decides not to issue the command (e.g., overrides the decision to issue the command), it would return the space previously reserved for the command by writing to a reservation return register, depicted as the return mechanism **334**, the amount of space it wishes to return (i.e. increments the reservation register **310** by this amount). Also shown in FIG. 3, another additional processing element **330** takes the command from the input queue **308** causing the reservation register to increase its available space automatically in hardware **332** by the amount of space now created based on the removal of the command from the input queue. The additional processing element **330** then executes the command and notifies the output queue **312** of the execution where it then issues the response to the first processing element **302**. In one non-limiting example, the system is implemented as part of a storage area network (SAN) controller, providing the command queue for the commands the storage controller is to issue to a storage media device. In another non-limiting example, the system is implemented as part of a network attached storage (NAS) controller, providing the command queue for the commands the storage controller is to issue to a storage media device.

In one embodiment, as depicted in FIG. 4, the present invention provides a system for dividing and synchronizing a processing task across a plurality of processing elements comprising: an input queue **408** implemented in hardware **414**; an output queue **412** also implemented in hardware **414**; a first processing element **402** having access to the input queue **408** (over communication link **416**) and the output queue **412** (over communication link **420**); one or more additional processing elements (e.g., processing element #2 - **404** through processing element #n - **406**) optionally in communication with the first processing element **402** (depicted by inter-processor communication link **426** between processing element #1 **402** and processing element #2 **404** and depicted by inter-processor communication link **428** between processing element #1 **402** and processing element #n **406**)

(while FIG. 4 depicts a simplistic link **426** or **428** between two processing elements, it should be noted that there may be other components disposed along this path, where such components may not be used to limit the scope of the present invention) and having access to the input queue **408** (over communication links **436** and **438**); a reservation register **410** implemented in hardware **414** storing a value indicative of available space in input queue **408**, the reservation register **410** accessible by both the first processing element **402** (over communication link **418**) and one or more additional processing elements (e.g., processing element #2 - **404** through processing element #n - **406**) (e.g., over communication links **422** and **424**); computer storage storing instructions, which when executed by one of the additional processing elements (e.g., processing element #2 - **404** through processing element #n - **406**): accesses the reservation register **410** and reads the stored value; the stored value automatically decremented in hardware by 1 in concert with the read to make a reservation of space **400**; determines when the read value indicates available space in the input queue **408** to issue a command; issue the command to the input queue **408** (this may be optionally done on behalf of the first processing element **402** or the first processing element can issue the command (or another command) into the input queue **408** by itself over communication link **416**); and wherein the first processing element **402** receives a response corresponding to the command from the output queue **412**. In the event the additional processing element (e.g., processing element #2 - **404** through processing element #n - **406**) decides not to issue the command after reserving space, it would return the space previously reserved for the command by writing to a reservation return register, depicted as the return mechanism **434**, the amount of space it wishes to return (i.e. increments the reservation register **410** by this amount). Also shown in FIG. 4, another additional processing element **430** that takes the command from the input queue **408** causing the reservation register to increase its available space automatically in hardware **432** by the amount of space now created based on the removal of the command from the input queue. The, the additional processing element **430** executes the command, and notifies the output queue **412** of the execution where it then issues the response to the first processing element **402**. In one non-limiting example, the system is implemented as part of a storage area network (SAN) controller. In another non-limiting example, the system is implemented as part of a network attached storage (NAS) controller.

In one embodiment, as depicted in FIG. 5, the present invention provides a system for dividing and synchronizing a processing task across a plurality of processing elements comprising: an input queue **508** implemented in hardware **514**; an output queue **512** also

implemented in hardware **514**; a first processing element **502** having access to the input queue **508** (over communication link **516**) and the output queue **512** (over communication link **520**); one or more additional processing elements (e.g., processing element #2 - **504** through processing element #n - **506**) optionally in communication with the first processing element **502** (depicted by inter-processor communication link **526** between processing element #1 **502** and processing element #2 **504** and depicted by inter-processor communication link **528** between processing element #1 **502** and processing element #n **506**) (while FIG. 5 depicts a simplistic link **526** or **528** between two processing elements, it should be noted that there may be other components disposed along this path, where such components may not be used to limit the scope of the present invention) and having access to the input queue **508** (over communication links **536** and **538**) and the output queue **512** (over communication links **540** and **542**); a reservation register **510** implemented in hardware **514** storing a value indicative of available space in input queue **508**, the reservation register **510** accessible by both the first processing element **502** (over communication link **518**) and one or more additional processing elements (e.g., processing element #2 - **504** through processing element #n - **506**) (e.g., over communication links **522** and **524**); computer storage storing instructions, which when executed by one of the additional processing elements (e.g., processing element #2 - **504** through processing element #n - **506**): accesses the reservation register **510** and reads the stored value; the stored value automatically decremented in hardware by 1 in concert with the read to make a reservation of space **500**; determines when the read value indicates available space in the input queue **508** to issue a command; issue the command to the input queue **508** (this may be optionally done on behalf of the first processing element **502** or the first processing element can issue the command (or another command) into the input queue **508** by itself over communication link **516**); and wherein the first processing element **502**, or the one or more additional processing elements **504** or **506**, receives a response (over communication links **520**, **540** or **542**) corresponding to the command from the output queue **512**. In the event the additional processing element (e.g., processing element #2 - **504** through processing element #n - **506**) decides not to issue the command after reserving space, it would return the space previously reserved for the command by writing to a reservation return register, depicted as the return mechanism **534**, the amount of space it wishes to return (i.e. increments the reservation register **510** by this amount). Also shown in FIG. 5, another additional processing element **530** that takes the command from the input queue **508** causing the reservation register to increase its available space automatically in hardware **532** by the amount of space now created based on the removal of the command from the input queue. The additional processing element **530** then

executes the command, and notifies the output queue **512** of the execution where it then issues the response to the first processing element **502**. In one non-limiting example, the system is implemented as part of a storage area network (SAN) controller. In another non-limiting example, the system is implemented as part of a network attached storage (NAS) controller.

The above-described features and applications can be implemented as software processes that are specified as a set of instructions recorded on a computer readable storage medium (also referred to as computer readable medium). When these instructions are executed by one or more processing element(s) (e.g., one or more processors, cores of processors, or other processing elements), they cause the processing element(s) to perform the actions indicated in the instructions. Embodiments within the scope of the present disclosure may also include tangible and/or non-transitory computer-readable storage media for carrying or having computer-executable instructions or data structures stored thereon. Such non-transitory computer-readable storage media can be any available media that can be accessed by a general purpose or special purpose computer, including the functional design of any special purpose processor. By way of example, and not limitation, such non-transitory computer-readable media can include flash memory, RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium which can be used to carry or store desired program code means in the form of computer-executable instructions, data structures, or processor chip design. The computer readable media does not include carrier waves and electronic signals passing wirelessly or over wired connections.

Computer-executable instructions include, for example, instructions and data which cause a general purpose computer, special purpose computer, or special purpose processing device to perform a certain function or group of functions. Computer-executable instructions also include program modules that are executed by computers in stand-alone or network environments. Generally, program modules include routines, programs, components, data structures, objects, and the functions inherent in the design of special-purpose processors, etc. that perform particular tasks or implement particular abstract data types. Computer-executable instructions, associated data structures, and program modules represent examples of the program code means for executing steps of the methods disclosed herein. The particular sequence of such executable instructions or associated data structures represents examples of corresponding acts for implementing the functions described in such steps.

A computer program (also known as a program, software, software application, script, or code) can be written in any form of programming language, including compiled or interpreted languages, declarative or procedural languages, and it can be deployed in any form, including as a stand-alone program or as a module, component, subroutine, object, or other unit suitable for use in a computing environment. A computer program may, but need not, correspond to a file in a file system. A program can be stored in a portion of a file that holds other programs or data (e.g., one or more scripts stored in a markup language document), in a single file dedicated to the program in question, or in multiple coordinated files (e.g., files that store one or more modules, sub programs, or portions of code). A computer program can be deployed to be executed on one computer or on multiple computers that are located at one site or distributed across multiple sites and interconnected by a communication network.

These functions described above can be implemented in digital electronic circuitry, in computer software, firmware or hardware. The techniques can be implemented using one or more computer program products. The processes and logic flows can be performed by one or more programmable processors and by one or more programmable logic circuitry. General and special purpose computing devices and storage devices can be interconnected through communication networks.

Some implementations include electronic components, for example microprocessors, storage and memory that store computer program instructions in a machine-readable or computer-readable medium (alternatively referred to as computer-readable storage media, machine-readable media, or machine-readable storage media). Some examples of such computer-readable media include RAM, ROM, read-only compact discs (CD-ROM), recordable compact discs (CD-R), rewritable compact discs (CD-RW), read-only digital versatile discs (e.g., DVD-ROM, dual-layer DVD-ROM), a variety of recordable/rewritable DVDs (e.g., DVD-RAM, DVD-RW, DVD+RW, etc.), flash memory (e.g., SD cards, mini-SD cards, micro-SD cards, etc.), magnetic or solid state hard drives, read-only and recordable Blu-Ray[®] discs, ultra density optical discs, any other optical or magnetic media, and floppy disks. The computer-readable media can store a computer program that is executable by at least one processing element and includes sets of instructions for performing various operations. Examples of computer programs or computer code include machine code, for

example is produced by a compiler, and files including higher-level code that are executed by a computer, an electronic component, or a microprocessor using an interpreter.

While the above discussion primarily refers to microprocessor or multi-core processors that execute software, some implementations are performed by one or more integrated circuits, for example application specific integrated circuits (ASICs) or field programmable gate arrays (FPGAs). In some implementations, such integrated circuits execute instructions that are stored on/within the circuit itself. In some implementations, such as with FPGAs, software may be used to describe hardware circuits, an example of which are FPGA programming files. Such FPGA programming files may also include computer programs, machine code, microcode, firmware, and other software. The FPGA programming files may be stored within an FPGA, ASIC, computer-readable storage media, machine-readable media, or machine-readable storage media.

As used in this specification and any claims of this application, the terms “computer”, “server”, “processor”, and “memory” all refer to electronic or other technological devices. These terms exclude people or groups of people. For the purposes of the specification, the terms display or displaying means displaying on an electronic device. As used in this specification and any claims of this application, the terms “computer readable medium” and “computer readable media” are entirely restricted to tangible, physical objects that store information in a form that is readable by a computer. These terms exclude any wireless signals, wired download signals, and any other ephemeral signals.

Those of skill in the art will appreciate that other embodiments of the disclosure may be practiced in network computing environments with many types of computer system configurations, including personal computers, hand-held devices, multi-processor systems, ASIC-based systems, FPGA-based systems, microprocessor-based or programmable consumer electronics, network PCs, minicomputers, mainframe computers, and the like. Embodiments may also be practiced in distributed computing environments where tasks are performed by local and remote processing devices that are linked (either by hardwired links, wireless links, or by a combination thereof) through a communications network. In a distributed computing environment, program modules may be located in both local and remote memory storage devices.

It is understood that any specific order or hierarchy of steps in the processes disclosed is an illustration of example approaches. Based upon design preferences, it is understood that the specific order or hierarchy of steps in the processes may be rearranged, or that all illustrated steps be performed. Some of the steps may be performed simultaneously. For example, in certain circumstances, multitasking and parallel processing may be advantageous. Moreover, the separation of various system components illustrated above should not be understood as requiring such separation, and it should be understood that the described program components and systems can generally be integrated together in a single software product or packaged into multiple software products.

Various modifications to these aspects will be readily apparent, and the generic principles defined herein may be applied to other aspects. Thus, the claims are not intended to be limited to the aspects shown herein, but is to be accorded the full scope consistent with the language claims, where reference to an element in the singular is not intended to mean “one and only one” unless specifically so stated, but rather “one or more.” Unless specifically stated otherwise, the term “some” refers to one or more. Pronouns in the masculine (e.g., his) include the feminine and neuter gender (e.g., her and its) and vice versa. Headings and subheadings, if any, are used for convenience only and do not limit the subject technology.

A phrase, for example, an “aspect” does not imply that the aspect is essential to the subject technology or that the aspect applies to all configurations of the subject technology. A disclosure relating to an aspect may apply to all configurations, or one or more configurations. A phrase, for example, an aspect may refer to one or more aspects and vice versa. A phrase, for example, a “configuration” does not imply that such configuration is essential to the subject technology or that such configuration applies to all configurations of the subject technology. A disclosure relating to a configuration may apply to all configurations, or one or more configurations. A phrase, for example, a configuration may refer to one or more configurations and vice versa.

The various embodiments described above are provided by way of illustration only and should not be construed to limit the scope of the disclosure. Those skilled in the art will readily recognize various modifications and changes that may be made to the principles described herein without following the example embodiments and applications illustrated and described herein, and without departing from the spirit and scope of the disclosure.

While this specification contains many specific implementation details, these should not be construed as limitations on the scope of any invention or of what may be claimed, but rather as descriptions of features that may be specific to particular embodiments of particular inventions. Certain features that are described in this specification in the context of separate
5 embodiments can also be implemented in combination in a single embodiment. Conversely, various features that are described in the context of a single embodiment can also be implemented in multiple embodiments separately or in any suitable subcombination. Moreover, although features may be described above as acting in certain combinations and
10 even initially claimed as such, one or more features from a claimed combination can in some cases be excised from the combination, and the claimed combination may be directed to a subcombination or variation of a subcombination.

Similarly, while operations are depicted in the drawings in a particular order, this
15 should not be understood as requiring that such operations be performed in the particular order shown or in sequential order, or that all illustrated operations be performed, to achieve desirable results. In certain circumstances, multitasking and parallel processing may be advantageous. Moreover, the separation of various system components in the embodiments described above should not be understood as requiring such separation in all embodiments,
20 and it should be understood that the described program components and systems can generally be integrated together in a single software product or packaged into multiple software products.

As noted above, particular embodiments of the subject matter have been described,
25 but other embodiments are within the scope of the following claims. For example, the actions recited in the claims can be performed in a different order and still achieve desirable results. As one example, the processes depicted in the accompanying figures do not necessarily require the particular order shown, or sequential order, to achieve desirable results. In certain implementations, multitasking and parallel processing may be
30 advantageous.

CONCLUSION

A system and method has been shown in the above embodiments for the effective implementation of a system and method for dividing and synchronizing a processing task across multiple processing elements/processors in hardware. While various preferred
5 embodiments have been shown and described, it will be understood that there is no intent to limit the invention by such disclosure, but rather, it is intended to cover all modifications falling within the spirit and scope of the invention, as defined in the appended claims. For example, the present invention should not be limited by software/program, computing environment, or specific computing hardware.

10

CLAIMS

1. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

an input queue implemented in hardware;

5 an output queue implemented in hardware;

a first processing element having access to said input queue and said output queue;

at least one second processing element in communication with said first processing element;

10 a reservation register implemented in hardware storing a value indicative of available space in a command queue, said reservation register accessible by both said first processing element and said at least second processing element;

computer storage storing instructions, which when executed by said at least one second processing element:

accesses said reservation register and reads said stored value;

15 determines when said read value indicates available space in said input queue for said first processing element to issue a command;

notifies said first processing element to issue said command to said input queue; and

20 wherein said first processing element receives notification from said at least second processing element regarding issuing the command, issues said command to said input queue, and receives a response corresponding to said command from said output queue.

2. The system of claim 1, wherein said command queue is a FIFO buffer.

25 3. The system of claim 1, wherein said system is part of a storage area network (SAN) controller.

4. The system of claim 1, wherein said system is part of a network attached storage (NAS) controller.

30

5. The system of claim 1, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element.

35 6. The system of claim 1, wherein at least one third processing element executes said command and notifies said output queue to issue said response.

7. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

an input queue implemented in hardware;

5 an output queue implemented in hardware;

a first processing element having access to said input queue and said output queue;

at least one second processing element in communication with said input queue;

10 a reservation register implemented in hardware storing a value indicative of available space in a command queue, said reservation register accessible by both said first processing element and said at least second processing element;

computer storage storing instructions, which when executed by said at least one second processing element:

accesses said reservation register and reads said stored value;

15 determines when said read value indicates available space in said input queue for said first processing element to issue a command;

issue said command to said input queue; and

wherein said first processing element receives a response corresponding to said command from said output queue.

20 8. The system of claim 7, wherein said command queue is a FIFO buffer.

9. The system of claim 7, wherein said system is part of a storage area network (SAN) controller.

25 10. The system of claim 7, wherein said system is part of a network attached storage (NAS) controller.

11. The system of claim 7, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element.

30

12. The system of claim 7, wherein at least one third processing element executes said command and notifies said output queue to issue said response.

35 13. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

an input queue implemented in hardware;
an output queue implemented in hardware;
a first processing element having access to said input queue and said output queue;
at least one second processing element in communication with said input queue and

5 said output queue;

a reservation register implemented in hardware storing a value indicative of available space in a command queue, said reservation register accessible by both said first processing element and said at least second processing element;

10 computer storage storing instructions, which when executed by said at least one second processing element:

accesses said reservation register and reads said stored value;

determines when said read value indicates available space in said input queue for said first processing element to issue a command;

issue said command to said input queue; and

15 receives a response corresponding to said command from said output queue.

14. The system of claim 13, wherein said command queue is a FIFO buffer.

20 15. The system of claim 13, wherein said system is either part of a storage area network (SAN) controller.

16. The system of claim 13, wherein said system is part of a network attached storage (NAS) controller.

25

17. The system of claim 13, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element.

18. The system of claim 13, wherein at least one third processing element executes
30 said command and notifies said output queue to issue said response.

1/5

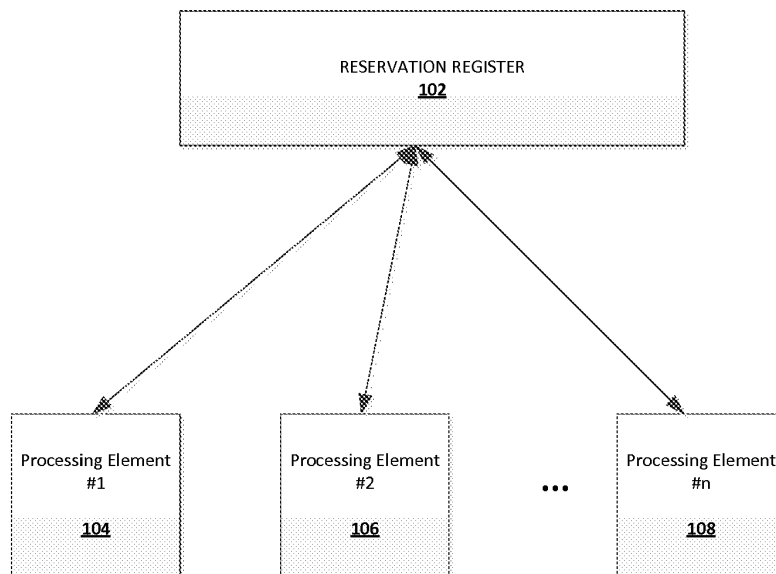


FIG. 1

2/5

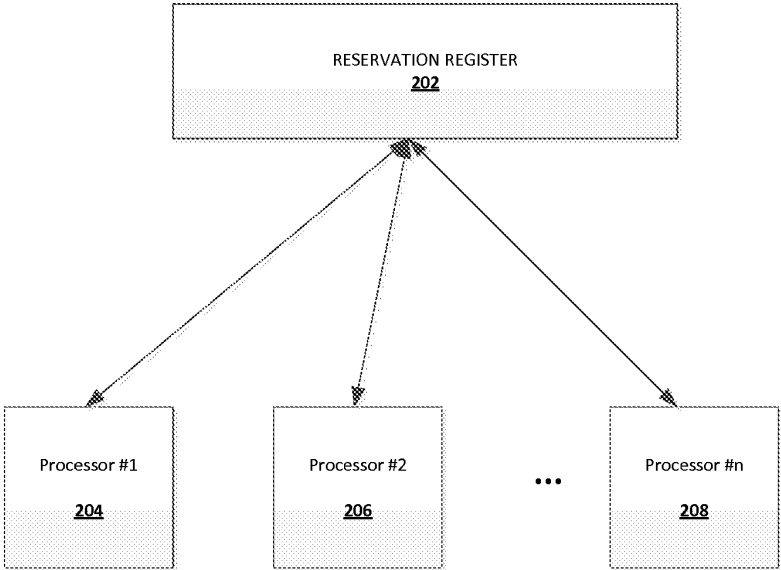


FIG. 2

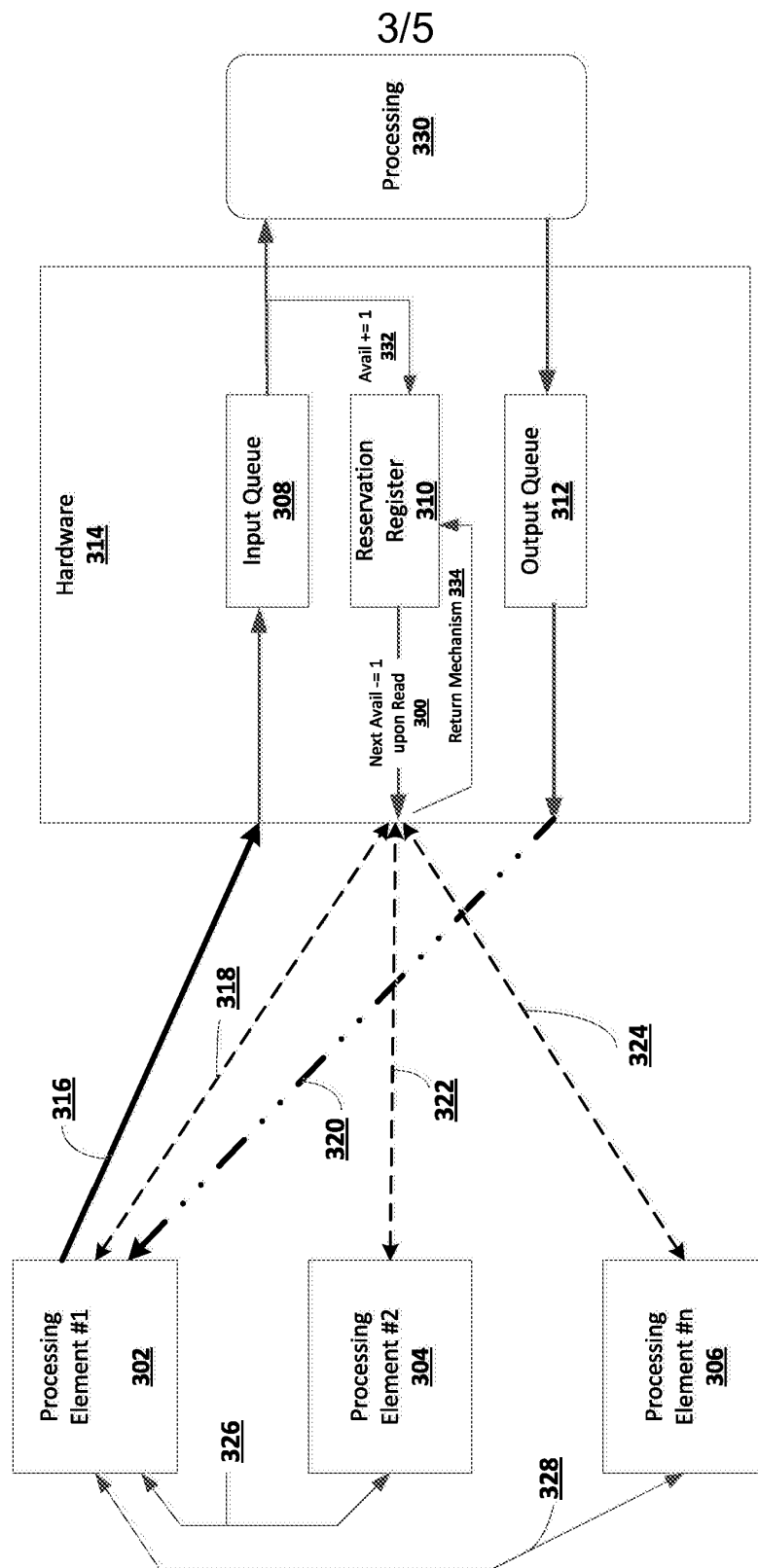


FIG. 3

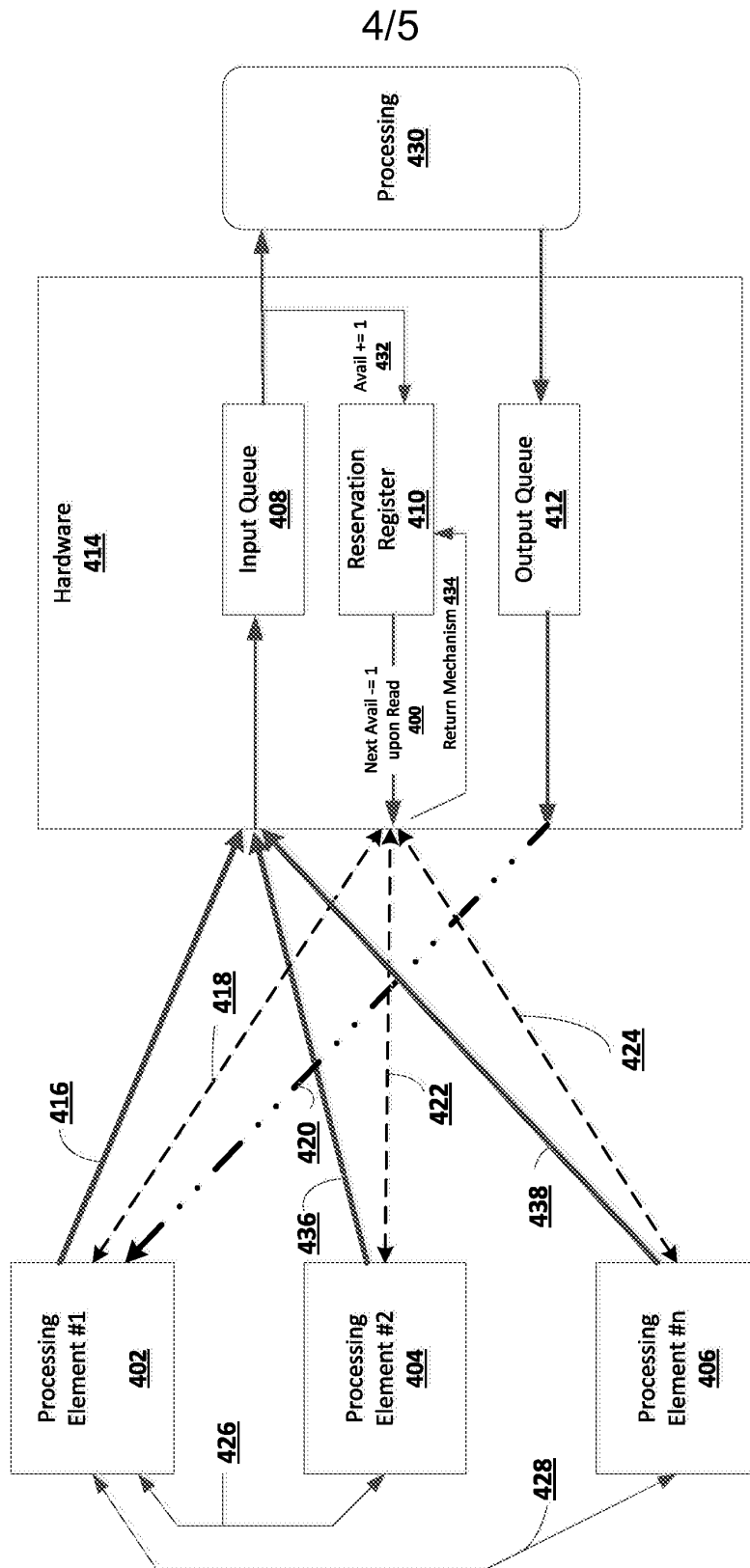


FIG. 4

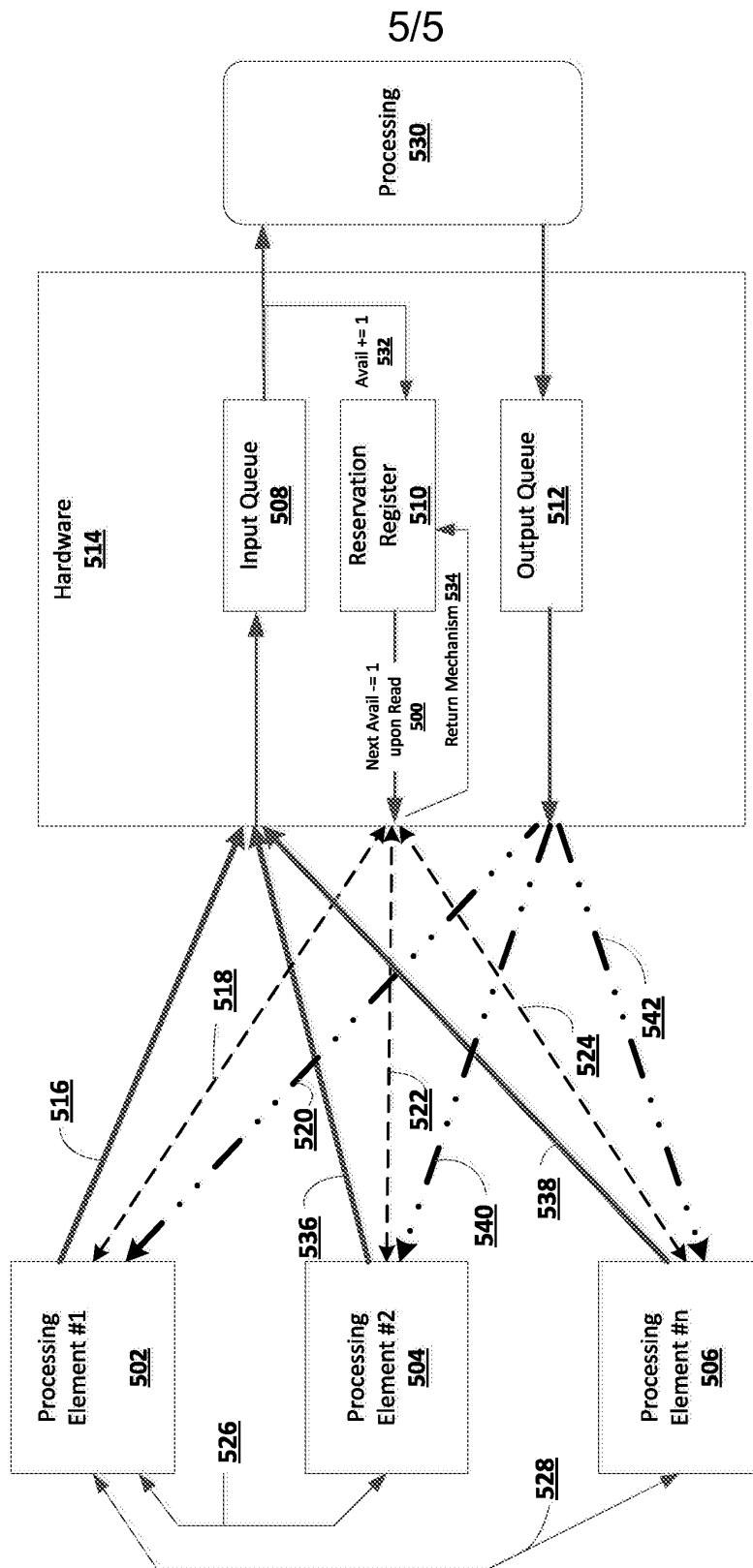


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/069153**A. CLASSIFICATION OF SUBJECT MATTER****G06F 9/46(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHEDMinimum documentation searched (classification system followed by classification symbols)
G06F 9/46Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: task, dispatch, command, queue, reservation**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2011-0078700 A1 (BLACKBURN, R. A. et al.) 31 March 2011 See abstract, paragraphs [0019]–[0028], and fig. 1.	1–18
A	US 2008-0301697 A1 (SOUTHGATE, T. J. et al.) 04 December 2008 See abstract, figs. 23 and 24, and claims 1–12.	1–18
A	US 2012-0102501 A1 (WADDINGTON, D. et al.) 26 April 2012 See abstract, paragraphs [0023]–[0032], and fig. 2.	1–18
A	US 2007-0016906 A1 (TRAUBEN, R. D. et al.) 18 January 2007 See abstract, paragraphs [0034]–[0039], and fig. 5.	1–18
A	US 2011-0055839 A1 (ALEXANDER, B. G. et al.) 03 March 2011 See abstract, paragraphs [0046]–[0053], and figs. 5 and 6.	1–18

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search
20 March 2015 (20.03.2015)Date of mailing of the international search report
23 March 2015 (23.03.2015)

Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701,
Republic of Korea

Facsimile No. ++82 42 472 7140

Authorized officer

YU, Jintae

Telephone No. +82-42-481-8530



Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2014/069153

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2011-0078700 A1	31/03/2011	None	
US 2008-0301697 A1	04/12/2008	US 2008-141279 A1 US 2008-301395 A1 US 2008-301418 A1 US 2008-301694 A1 US 8332829 B2 US 8438365 B2 US 8694757 B2	12/06/2008 04/12/2008 04/12/2008 04/12/2008 11/12/2012 07/05/2013 08/04/2014
US 2012-0102501 A1	26/04/2012	KR 10-2012-0042654 A US 2012-102500 A1 US 8640140 B2	03/05/2012 26/04/2012 28/01/2014
US 2007-0016906 A1	18/01/2007	None	
US 2011-0055839 A1	03/03/2011	CN 102004630 A CN 102004630 B JP 2011-054161 A JP 5650952 B2 KR 10-2011-0023832 A TW 201120754 A US 8056080 B2	06/04/2011 11/12/2013 17/03/2011 07/01/2015 08/03/2011 16/06/2011 08/11/2011

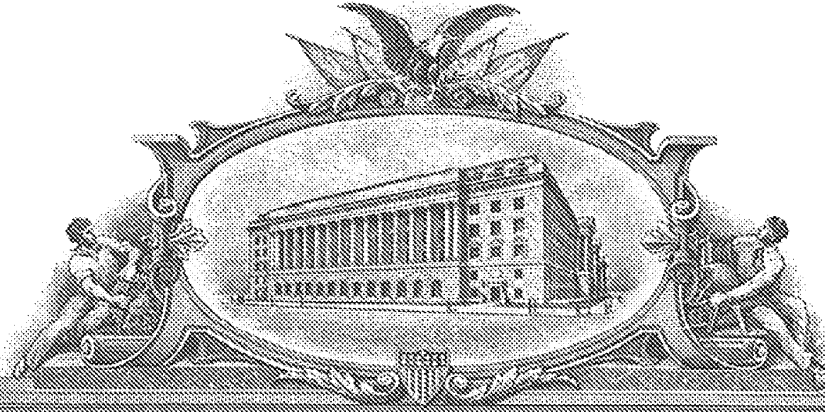
Form PCT/ISA/210 (patent family annex) (January 2015)

**DOCUMENT MADE AVAILABLE UNDER THE
PATENT COOPERATION TREATY (PCT)**

International application number:	PCT/US2014/069153
International filing date:	08 December 2014 (08.12.2014)
Document type:	Certified copy of priority document
Document details:	Country/Office: US
	Number: 14/099,844
	Filing date: 06 December 2013 (06.12.2013)
Date of receipt at the International Bureau:	02 January 2015 (02.01.2015)

Remark: Priority document submitted or transmitted to the International Bureau in compliance with Rule 17.1(a),(b) or (b-bis)

675022



THE UNITED STATES OF AMERICA

TO ALL TO WHOM THESE PRESENTS SHALL COME:

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

January 01, 2015

THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM THE RECORDS OF THE UNITED STATES PATENT AND TRADEMARK OFFICE OF THOSE PAPERS OF THE BELOW IDENTIFIED PATENT APPLICATION THAT MET THE REQUIREMENTS TO BE GRANTED A FILING DATE.

APPLICATION NUMBER: *14/099,844*

FILING DATE: *December 06, 2013*

RELATED PCT APPLICATION NUMBER: *PCT/US14/69153*

THE COUNTRY CODE AND NUMBER OF YOUR PRIORITY APPLICATION, TO BE USED FOR FILING ABROAD UNDER THE PARIS CONVENTION, IS *US14/099,844*



Certified by

David J. Kyros

Under Secretary of Commerce
for Intellectual Property
and Director of the United States
Patent and Trademark Office

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	C67508 1170US.1
		Application Number	
Title of Invention	A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Jesse D.		BEESON		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	Johns Creek	State/Province	GA	Country of Residence i	US
Mailing Address of Inventor:					
Address 1	240 Woodscape Court				
Address 2					
City	Johns Creek	State/Province	GA		
Postal Code	30022-3244	Country i	US		
Inventor 2					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Jesse B.		YATES		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	Atlanta	State/Province	GA	Country of Residence i	US
Mailing Address of Inventor:					
Address 1	2451 Cumberland Parkway SE, Ste. 300 #3310				
Address 2					
City	Atlanta	State/Province	GA		
Postal Code	30339	Country i	US		
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.					Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	C67508 1170US.1	
		Application Number		
Title of Invention	A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE			
☐ An Address is being provided for the correspondence information of this application.				
Customer Number	26158			
Email Address			Add Email	Remove Email

Application Information:

Title of the Invention	A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE		
Attorney Docket Number	C67508 1170US.1	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	5	Suggested Figure for Publication (if any)	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☒ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.			
Please Select One: ☒ Customer Number ☐ US Patent Practitioner ☐ Limited Recognition (37 CFR 11.9)			
Customer Number	26158		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.			
Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	C67508 1170US.1
		Application Number	
Title of Invention	A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE		

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove			
Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ^j (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013. ☐ NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.
--

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices
--

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	C67508 1170US.1
		Application Number	
Title of Invention	A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE		

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.			
Applicant 1			Remove
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.			
Clear			
☒ Assignee	☐ Legal Representative under 35 U.S.C. 117	☐ Joint Inventor	
☐ Person to whom the inventor is obligated to assign.		☐ Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor :			
If the Applicant is an Organization check here. ☒			
Organization Name	Concurrent Ventures, LLC		
Mailing Address Information:			
Address 1	240 Woodscape Court		
Address 2			
City	Johns Creek	State/Province	GA
Country	US	Postal Code	30022-3244
Phone Number		Fax Number	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	C67508 1170US.1
		Application Number	
Title of Invention	A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE		
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button.			Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1				
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
				Remove
If the Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information:				
Address 1				
Address 2				
City		State/Province		
Country i		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee Data may be generated within this form by selecting the Add button.				Add

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications					
Signature	/Michael L. Gencarella/			Date (YYYY-MM-DD)	2013-12-06
First Name	Michael L.	Last Name	Gencarella	Registration Number	44703
Additional Signature may be generated within this form by selecting the Add button.					Add

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	C67508 1170US.1
		Application Number	
Title of Invention	A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR LETTERS PATENT

INVENTOR(S):

Jesse D Beeson

240 Woodscape Ct

Johns Creek, GA 30022

Jesse B Yates

2451 Cumberland Parkway SE

Ste 300 #3310

Atlanta, GA 30339

TITLE:

A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING
TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE

BACKGROUND OF THE INVENTION

Field of Invention

The present invention relates generally to the field of load distribution. More specifically, the present invention is related to a system and method for dividing and
5 synchronizing a processing task across multiple processing elements/processors in hardware.

Discussion of Related Art

In the prior art, the processing load (of a processing element) to determine what
10 command to issue is relatively high. The processing load to determine what command to issue can be partially or fully offloaded to a multiplicity of other processing elements (e.g. processors, processor cores, or custom processing circuitry). However, this distribution of load causes commands to be determined from multiple processing elements. It can become a challenge to ensure the module command queues (FIFOs) are not overfilled,
15 thus synchronization is required amongst the multiplicity of processing elements. In the prior art, such synchronization is performed using software techniques, such as semaphores and mutexes to a shared available space count variable in memory. However, this takes additional processing time, making this process non-optimal. To further compound the problem, there may be a need to keep the time from command issue to
20 execution minimized, which tends to keep the command queue shallow.

Embodiments of the present invention are an improvement over prior art systems and methods.

SUMMARY OF THE INVENTION

5 In one embodiment, the present invention provides a system for dividing and synchronizing a processing task across a plurality of processing elements comprising: an input queue implemented in hardware; an output queue implemented in hardware; a first processing element having access to the input queue and the output queue; at least one second processing element in communication with the first processing element; a reservation register implemented in hardware storing a value indicative of available space in a command queue, the reservation register accessible by both the first processing element and the at least second processing element; computer storage storing instructions, which when executed by the at least one second processing element: accesses the reservation register and reads the stored value; determines when the read value indicates available space in the input queue for the first processing element to issue a command; 10 notifies the first processing element to issue the command to the input queue; and wherein the first processing element receives notification from the at least second processing element regarding issuing the command, issues the command to the input queue, and receives a response corresponding to the command from the output queue.

20

CONCURRENT VENTURES, LLC CONFIDENTIAL

In another embodiment, the present invention provides a system for dividing and synchronizing a processing task across a plurality of processing elements comprising: an input queue implemented in hardware; an output queue implemented in hardware; a first processing element having access to the input queue and the output queue; at least one
5 second processing element in communication with the input queue; a reservation register implemented in hardware storing a value indicative of available space in a command queue, the reservation register accessible by both the first processing element and the at least second processing element; computer storage storing instructions, which when executed by the at least one second processing element: accesses the reservation register
10 and reads the stored value; determines when the read value indicates available space in the input queue for the first processing element to issue a command; issue the command to the input queue; and wherein the first processing element receives a response corresponding to the command from the output queue.

15 In another embodiment, the present invention provides for a system for dividing and synchronizing a processing task across a plurality of processing elements comprising: an input queue implemented in hardware; an output queue implemented in hardware; a first processing element having access to the input queue and the output queue; at least one second processing element in communication with the input queue and the output
20 queue; a reservation register implemented in hardware storing a value indicative of available space in a command queue, the reservation register accessible by both the first

processing element and the at least second processing element; computer storage storing instructions, which when executed by the at least one second processing element: accesses the reservation register and reads the stored value; determines when the read value indicates available space in the input queue for the first processing element to issue
5 a command; issue the command to the input queue; and receives a response corresponding to the command from the output queue.

BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure, in accordance with one or more various examples, is described in detail with reference to the following figures. The drawings are provided for purposes of illustration only and merely depict examples of the disclosure. These
5 drawings are provided to facilitate the reader's understanding of the disclosure and should not be considered limiting of the breadth, scope, or applicability of the disclosure. It should be noted that for clarity and ease of illustration these drawings are not necessarily made to scale.

FIG. 1 depicts a non-limiting example of where the present invention's
10 "reservation" register is accessible by a plurality of processing elements.

FIG. 2 depicts another non-limiting example of where the present invention's reservation register is accessible by a plurality of processors.

FIG. 3 through FIG. 5 depict the various embodiments of the present invention for dividing and synchronizing a processing task across a plurality of processing elements.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

While this invention is illustrated and described in a preferred embodiment, the invention may be produced in many different configurations. There is depicted in the drawings, and will herein be described in detail, a preferred embodiment of the invention,
20 with the understanding that the present disclosure is to be considered as an exemplification of the principles of the invention and the associated functional

specifications for its construction and is not intended to limit the invention to the embodiment illustrated. Those skilled in the art will envision many other possible variations within the scope of the present invention.

5 Note that in this description, references to “one embodiment” or “an embodiment” mean that the feature being referred to is included in at least one embodiment of the invention. Further, separate references to “one embodiment” in this description do not necessarily refer to the same embodiment; however, neither are such embodiments mutually exclusive, unless so stated and except as will be readily apparent to those of
10 ordinary skill in the art. Thus, the present invention can include any variety of combinations and/or integrations of the embodiments described herein.

The invention considers the case where software must issue commands to a hardware module. In this case the processing load to determine what command to issue is
15 relatively high, and there may also be additional background tasks necessary. The processing load to determine what command to issue can be partially or fully offloaded to a multiplicity of other processing elements (e.g. processors, processor cores, or custom processing circuitry). However, this distribution of load causes commands to be determined from multiple processing elements. It can become a challenge to ensure the
20 module command queues (FIFOs) are not overfilled, thus synchronization is required amongst the multiplicity of processing elements. As noted above, in the prior art, this

synchronization is performed using software techniques, such as semaphores and mutexes to a shared available space count variable. However, this takes additional processing time. To further compound the problem there may be a need to keep the time from command issue to execution minimized, which tends to keep the command queue shallow.

5

The present invention provides a shared counter resource (e.g., a register) in the hardware representing how much free space there is in the command queue, accessible to one or more processing elements. FIG. 1 depicts a non-limiting example of where the present invention's "reservation" register **102** is accessible by a plurality of processing
10 elements 1 through n, **104** through **108**. It should be noted that while the discussion herein references processing elements, the teachings of the present invention equally applies to disparate processors as well. For example, FIG. 2 depicts another non-limiting example of where the present invention's reservation register **202** is accessible by a plurality of processors 1 through n, **204** through **208**.

15

When a processing element reads the "reservation" register, the hardware automatically decrements the available free space by a preconfigured amount (e.g., 1) and returns the value of the free space immediately prior to the read / reservation. If the read returns 0 (or a number less than the preconfigured amount), there is insufficient free space
20 to satisfy the request. In the event there is insufficient space to satisfy the request the reservation register may be configured to reserve however much space is available or to

CONCURRENT VENTURES, LLC CONFIDENTIAL

not reserve any space at all. At times there may exist a need to test if a reservation would succeed without actually making a reservation, a “peek” at the reservation register. This peek may be implemented via an alternate, mirrored, reservation register that mirrors the value of the reservation register that can be read by a processing element, but does not actually make a reservation, whereby the alternate register does not automatically modify the available free space. Any number of processing elements may read these registers (hardware synchronizes these reads internally to ensure they do not overlap using standard arbitration for multiple processing elements). Thus there is a guarantee of not “over subscribing” the command queue. When commands actually are issued to the queue following a reservation, they will remain there until the hardware module or entity consuming those commands is able to process them, removing them from the queue. Once they are removed from the queue, the reservation free space will be incremented automatically by the hardware. This reservation technique allows for a fixed or variable time delay between making the reservation for space in the queue and actually issuing the command to the queue, and allows for different processing elements to make the decision(s) and to then issue the command(s). The reservation free space is different from the actual real time free space in the command queue, since space is “reserved” prior to actually being consumed by an issued command.

The software, therefore, need only read a register and check its return value to make a reservation and know if it was successful or not. All arbitration and mutual

exclusion tasks between multiple processing elements are handled in hardware. There is no need for the software overhead of multiple processing elements handling the synchronization of a shared available space count variable in shared memory or otherwise.

5

In one embodiment there is a single processing element connected to the module's command queue. It is desired to have a single point of responsibility for this hardware module (such as a control interface to a storage processing element) to issue the commands and deal with the responses from the module. However, the processing load to determine all or a subset of commands to issue may be high. This processing load is placed on a separate processing element. The two processing elements communicate in some efficient way (such as through shared memory, etc.). Part of the processing load is to know that there is in fact available space for a command to be issued, thus this second processing element must have visibility to the available free command queue space in addition to the first processing element also having visibility. The second processing element may issue its commands directly or may return its decision back to the first processing element to be sequenced with any commands the first processing element is able to issue on its own, but even in such a scenario, the first processing element would have to make its own space reservations for those commands it is able to issue on its own. Therefore, any processing element that determines a command must first make a reservation prior to issuing the command or informing another processing element of the

20

decision to issue a command. The hardware will then automatically, without software intervention, update the reserved free space when the command is actually removed from the queue for consumption. In the event space is reserved but later it is determined that space is not to be used (e.g., decided to not issue the command after space had been reserved), there may be a mechanism available to a processing element to return reserved space back to the pool (via another register action) making it available space again.

This mechanism need not be a “command” queue but any resource shared among a plurality of processing elements. For example, the mechanism may be used to implement a hardware-based mutex or hardware-based semaphore. The shared resource itself may be implemented in hardware, software, or a combination of the two. Though the reservations in the embodiments discussed reserve one entry in the queue at a time, this is not necessary, as it could be some other number (e.g., a plurality of commands, the amount of queue space consumed by a command, or some other number relevant to the shared resource). Such other numbers are within the scope of the present invention.

In the event a reservation fails, it would be possible for the hardware to internally and automatically queue (e.g., post) the attempt and generate an interrupt to the requesting processor element at some later point in time to indicate it was then successful, alleviating the requesting processing element from having to poll for space to be available.

In one embodiment, as depicted in FIG. 3, the present invention provides a system for dividing and synchronizing a processing task across a plurality of processing elements comprising: an input queue **308** implemented in hardware **314**; an output queue **312** also
5 implemented in hardware **314**; a first processing element **302** having access to the input queue **308** (over communication link **316**) and the output queue **312** (over communication link **320**); one or more additional processing elements (e.g., processing element #2 - **304** through processing element #n - **306**) in communication with the first processing element **302** (depicted by inter-processor communication link **326** between
10 processing element #1 **302** and processing element #2 **304** and depicted by inter-processor communication link **328** between processing element #1 **302** and processing element #n **306**) (while FIG. 3 depicts a simplistic link **326** or **328** between two processing elements, it should be noted that there may be other components disposed along this path, where such components may not be used to limit the scope of the present
15 invention); a reservation register **310** implemented in hardware **314** storing a value indicative of available space in input queue **308**, the reservation register **310** accessible by both the first processing element **302** (over communication link **318**) and one or more additional processing elements (e.g., processing element #2 - **304** through processing element #n - **306**) (e.g., over communication links **322** and **324**); computer storage
20 storing instructions, which when executed by one of the additional processing elements

(e.g., processing element #2 - **304** through processing element #n - **306**): accesses the reservation register **310** and reads the stored value; the stored value automatically decremented in hardware by 1 in concert with the read to make a reservation of space **300**; determines when the read value indicates available space in the input queue **308** for the first processing element **302** to issue a command; notifies the first processing element **302** to issue the command to the input queue **308**; and wherein the first processing element **302** receives notification from one of the additional processing elements (e.g., processing element #2 - **304** through processing element #n - **306**) regarding issuing the command, issues the command to the input queue **308**, and receives a response corresponding to the command from the output queue **312**. In the event the first processing element **302** decides not to issue the command (e.g., overrides the decision to issue the command), it would return the space previously reserved for the command by writing to a reservation return register, depicted as the return mechanism **334**, the amount of space it wishes to return (i.e. increments the reservation register **310** by this amount). Also shown in FIG. 3, another additional processing element **330** takes the command from the input queue **308** causing the reservation register to increase its available space automatically in hardware **332** by the amount of space now created based on the removal of the command from the input queue. The additional processing element **330** then executes the command and notifies the output queue **312** of the execution where it then issues the response to the first processing element **302**. In one non-limiting example, the

system is implemented as part of a storage area network (SAN) controller, providing the command queue for the commands the storage controller is to issue to a storage media device. In another non-limiting example, the system is implemented as part of a network attached storage (NAS) controller, providing the command queue for the commands the storage controller is to issue to a storage media device.

In one embodiment, as depicted in FIG. 4, the present invention provides a system for dividing and synchronizing a processing task across a plurality of processing elements comprising: an input queue **408** implemented in hardware **414**; an output queue **412** also implemented in hardware **414**; a first processing element **402** having access to the input queue **408** (over communication link **416**) and the output queue **412** (over communication link **420**); one or more additional processing elements (e.g., processing element #2 - **404** through processing element #n - **406**) optionally in communication with the first processing element **402** (depicted by inter-processor communication link **426** between processing element #1 **402** and processing element #2 **404** and depicted by inter-processor communication link **428** between processing element #1 **402** and processing element #n **406**) (while FIG. 4 depicts a simplistic link **426** or **428** between two processing elements, it should be noted that there may be other components disposed along this path, where such components may not be used to limit the scope of the present invention) and having access to the input queue **408** (over communication links **436** and **438**); a reservation register **410** implemented in hardware **414** storing a value indicative

of available space in input queue **408**, the reservation register **410** accessible by both the first processing element **402** (over communication link **418**) and one or more additional processing elements (e.g., processing element #2 - **404** through processing element #n - **406**) (e.g., over communication links **422** and **424**); computer storage storing instructions, which when executed by one of the additional processing elements (e.g., processing element #2 - **404** through processing element #n - **406**): accesses the reservation register **410** and reads the stored value; the stored value automatically decremented in hardware by 1 in concert with the read to make a reservation of space **400**; determines when the read value indicates available space in the input queue **408** to issue a command; issue the command to the input queue **408** (this may be optionally done on behalf of the first processing element **402** or the first processing element can issue the command (or another command) into the input queue **408** by itself over communication link **416**); and wherein the first processing element **402** receives a response corresponding to the command from the output queue **412**. In the event the additional processing element (e.g., processing element #2 - **404** through processing element #n - **406**) decides not to issue the command after reserving space, it would return the space previously reserved for the command by writing to a reservation return register, depicted as the return mechanism **434**, the amount of space it wishes to return (i.e. increments the reservation register **410** by this amount). Also shown in FIG. 4, another additional processing element **430** that takes the command from the input queue **408** causing the reservation register to increase its available space

automatically in hardware **432** by the amount of space now created based on the removal of the command from the input queue. The, the additional processing element **430** executes the command, and notifies the output queue **412** of the execution where it then issues the response to the first processing element **402**. In one non-limiting example, the system is implemented as part of a storage area network (SAN) controller. In another non-limiting example, the system is implemented as part of a network attached storage (NAS) controller.

In one embodiment, as depicted in FIG. 5, the present invention provides a system for dividing and synchronizing a processing task across a plurality of processing elements comprising: an input queue **508** implemented in hardware **514**; an output queue **512** also implemented in hardware **514**; a first processing element **502** having access to the input queue **508** (over communication link **516**) and the output queue **512** (over communication link **520**); one or more additional processing elements (e.g., processing element #2 - **504** through processing element #n - **506**) optionally in communication with the first processing element **502** (depicted by inter-processor communication link **526** between processing element #1 **502** and processing element #2 **504** and depicted by inter-processor communication link **528** between processing element #1 **502** and processing element #n **506**) (while FIG. 5 depicts a simplistic link **526** or **528** between two processing elements, it should be noted that there may be other components disposed along this path, where such components may not be used to limit the scope of the present

invention) and having access to the input queue **508** (over communication links **536** and **538**) and the output queue **512** (over communication links **540** and **542**); a reservation register **510** implemented in hardware **514** storing a value indicative of available space in input queue **508**, the reservation register **510** accessible by both the first processing
5 element **502** (over communication link **518**) and one or more additional processing elements (e.g., processing element #2 - **504** through processing element #n - **506**) (e.g., over communication links **522** and **524**); computer storage storing instructions, which when executed by one of the additional processing elements (e.g., processing element #2 - **504** through processing element #n - **506**): accesses the reservation register **510** and reads
10 the stored value; the stored value automatically decremented in hardware by 1 in concert with the read to make a reservation of space **500**; determines when the read value indicates available space in the input queue **508** to issue a command; issue the command to the input queue **508** (this may be optionally done on behalf of the first processing element **502** or the first processing element can issue the command (or another command)
15 into the input queue **508** by itself over communication link **516**); and wherein the first processing element **502**, or the one or more additional processing elements **504** or **506**, receives a response (over communication links **520**, **540** or **542**) corresponding to the command from the output queue **512**. In the event the additional processing element (e.g., processing element #2 - **504** through processing element #n - **506**) decides not to
20 issue the command after reserving space, it would return the space previously reserved for

the command by writing to a reservation return register, depicted as the return mechanism **534**, the amount of space it wishes to return (i.e. increments the reservation register **510** by this amount). Also shown in FIG. 5, another additional processing element **530** that takes the command from the input queue **508** causing the reservation register to increase
5 its available space automatically in hardware **532** by the amount of space now created based on the removal of the command from the input queue. The additional processing element **530** then executes the command, and notifies the output queue **512** of the execution where it then issues the response to the first processing element **502**. In one non-limiting example, the system is implemented as part of a storage area network (SAN)
10 controller. In another non-limiting example, the system is implemented as part of a network attached storage (NAS) controller.

The above-described features and applications can be implemented as software processes that are specified as a set of instructions recorded on a computer readable
15 storage medium (also referred to as computer readable medium). When these instructions are executed by one or more processing element(s) (e.g., one or more processors, cores of processors, or other processing elements), they cause the processing element(s) to perform the actions indicated in the instructions. Embodiments within the scope of the present disclosure may also include tangible and/or non-transitory computer-readable
20 storage media for carrying or having computer-executable instructions or data structures stored thereon. Such non-transitory computer-readable storage media can be any

available media that can be accessed by a general purpose or special purpose computer, including the functional design of any special purpose processor. By way of example, and not limitation, such non-transitory computer-readable media can include flash memory, RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or
5 other magnetic storage devices, or any other medium which can be used to carry or store desired program code means in the form of computer-executable instructions, data structures, or processor chip design. The computer readable media does not include carrier waves and electronic signals passing wirelessly or over wired connections.

10 Computer-executable instructions include, for example, instructions and data which cause a general purpose computer, special purpose computer, or special purpose processing device to perform a certain function or group of functions. Computer-executable instructions also include program modules that are executed by computers in stand-alone or network environments. Generally, program modules include routines,
15 programs, components, data structures, objects, and the functions inherent in the design of special-purpose processors, etc. that perform particular tasks or implement particular abstract data types. Computer-executable instructions, associated data structures, and program modules represent examples of the program code means for executing steps of the methods disclosed herein. The particular sequence of such executable instructions or
20 associated data structures represents examples of corresponding acts for implementing the functions described in such steps.

A computer program (also known as a program, software, software application, script, or code) can be written in any form of programming language, including compiled or interpreted languages, declarative or procedural languages, and it can be deployed in
5 any form, including as a stand-alone program or as a module, component, subroutine, object, or other unit suitable for use in a computing environment. A computer program may, but need not, correspond to a file in a file system. A program can be stored in a portion of a file that holds other programs or data (e.g., one or more scripts stored in a markup language document), in a single file dedicated to the program in question, or in
10 multiple coordinated files (e.g., files that store one or more modules, sub programs, or portions of code). A computer program can be deployed to be executed on one computer or on multiple computers that are located at one site or distributed across multiple sites and interconnected by a communication network.

15 These functions described above can be implemented in digital electronic circuitry, in computer software, firmware or hardware. The techniques can be implemented using one or more computer program products. The processes and logic flows can be performed by one or more programmable processors and by one or more programmable logic circuitry. General and special purpose computing devices and
20 storage devices can be interconnected through communication networks.

CONCURRENT VENTURES, LLC CONFIDENTIAL

Some implementations include electronic components, for example microprocessors, storage and memory that store computer program instructions in a machine-readable or computer-readable medium (alternatively referred to as computer-readable storage media, machine-readable media, or machine-readable storage media).

5 Some examples of such computer-readable media include RAM, ROM, read-only compact discs (CD-ROM), recordable compact discs (CD-R), rewritable compact discs (CD-RW), read-only digital versatile discs (e.g., DVD-ROM, dual-layer DVD-ROM), a variety of recordable/rewritable DVDs (e.g., DVD-RAM, DVD-RW, DVD+RW, etc.), flash memory (e.g., SD cards, mini-SD cards, micro-SD cards, etc.), magnetic or solid
10 state hard drives, read-only and recordable Blu-Ray[®] discs, ultra density optical discs, any other optical or magnetic media, and floppy disks. The computer-readable media can store a computer program that is executable by at least one processing element and includes sets of instructions for performing various operations. Examples of computer programs or computer code include machine code, for example is produced by a
15 compiler, and files including higher-level code that are executed by a computer, an electronic component, or a microprocessor using an interpreter.

While the above discussion primarily refers to microprocessor or multi-core processors that execute software, some implementations are performed by one or more
20 integrated circuits, for example application specific integrated circuits (ASICs) or field programmable gate arrays (FPGAs). In some implementations, such integrated circuits

CONCURRENT VENTURES, LLC CONFIDENTIAL

execute instructions that are stored on/within the circuit itself. In some implementations, such as with FPGAs, software may be used to describe hardware circuits, an example of which are FPGA programming files. Such FPGA programming files may also include computer programs, machine code, microcode, firmware, and other software. The FPGA
5 programming files may be stored within an FPGA, ASIC, computer-readable storage media, machine-readable media, or machine-readable storage media.

As used in this specification and any claims of this application, the terms “computer”, “server”, “processor”, and “memory” all refer to electronic or other
10 technological devices. These terms exclude people or groups of people. For the purposes of the specification, the terms display or displaying means displaying on an electronic device. As used in this specification and any claims of this application, the terms “computer readable medium” and “computer readable media” are entirely restricted to tangible, physical objects that store information in a form that is readable by a computer.
15 These terms exclude any wireless signals, wired download signals, and any other ephemeral signals.

Those of skill in the art will appreciate that other embodiments of the disclosure may be practiced in network computing environments with many types of computer
20 system configurations, including personal computers, hand-held devices, multi-processor systems, ASIC-based systems, FPGA-based systems, microprocessor-based or

CONCURRENT VENTURES, LLC CONFIDENTIAL

programmable consumer electronics, network PCs, minicomputers, mainframe computers, and the like. Embodiments may also be practiced in distributed computing environments where tasks are performed by local and remote processing devices that are linked (either by hardwired links, wireless links, or by a combination thereof) through a communications network. In a distributed computing environment, program modules
5 may be located in both local and remote memory storage devices.

It is understood that any specific order or hierarchy of steps in the processes disclosed is an illustration of example approaches. Based upon design preferences, it is
10 understood that the specific order or hierarchy of steps in the processes may be rearranged, or that all illustrated steps be performed. Some of the steps may be performed simultaneously. For example, in certain circumstances, multitasking and parallel processing may be advantageous. Moreover, the separation of various system components illustrated above should not be understood as requiring such separation, and
15 it should be understood that the described program components and systems can generally be integrated together in a single software product or packaged into multiple software products.

Various modifications to these aspects will be readily apparent, and the generic
20 principles defined herein may be applied to other aspects. Thus, the claims are not intended to be limited to the aspects shown herein, but is to be accorded the full scope

CONCURRENT VENTURES, LLC CONFIDENTIAL

consistent with the language claims, where reference to an element in the singular is not intended to mean “one and only one” unless specifically so stated, but rather “one or more.” Unless specifically stated otherwise, the term “some” refers to one or more. Pronouns in the masculine (e.g., his) include the feminine and neuter gender (e.g., her and
5 its) and vice versa. Headings and subheadings, if any, are used for convenience only and do not limit the subject technology.

A phrase, for example, an “aspect” does not imply that the aspect is essential to the subject technology or that the aspect applies to all configurations of the subject
10 technology. A disclosure relating to an aspect may apply to all configurations, or one or more configurations. A phrase, for example, an aspect may refer to one or more aspects and vice versa. A phrase, for example, a “configuration” does not imply that such configuration is essential to the subject technology or that such configuration applies to all configurations of the subject technology. A disclosure relating to a configuration may
15 apply to all configurations, or one or more configurations. A phrase, for example, a configuration may refer to one or more configurations and vice versa.

The various embodiments described above are provided by way of illustration only and should not be construed to limit the scope of the disclosure. Those skilled in the
20 art will readily recognize various modifications and changes that may be made to the principles described herein without following the example embodiments and applications

illustrated and described herein, and without departing from the spirit and scope of the disclosure.

While this specification contains many specific implementation details, these
5 should not be construed as limitations on the scope of any invention or of what may be
claimed, but rather as descriptions of features that may be specific to particular
embodiments of particular inventions. Certain features that are described in this
specification in the context of separate embodiments can also be implemented in
combination in a single embodiment. Conversely, various features that are described in
10 the context of a single embodiment can also be implemented in multiple embodiments
separately or in any suitable subcombination. Moreover, although features may be
described above as acting in certain combinations and even initially claimed as such, one
or more features from a claimed combination can in some cases be excised from the
combination, and the claimed combination may be directed to a subcombination or
15 variation of a subcombination.

Similarly, while operations are depicted in the drawings in a particular order, this
should not be understood as requiring that such operations be performed in the particular
order shown or in sequential order, or that all illustrated operations be performed, to
20 achieve desirable results. In certain circumstances, multitasking and parallel processing
may be advantageous. Moreover, the separation of various system components in the

CONCURRENT VENTURES, LLC CONFIDENTIAL

embodiments described above should not be understood as requiring such separation in all embodiments, and it should be understood that the described program components and systems can generally be integrated together in a single software product or packaged into multiple software products.

5

As noted above, particular embodiments of the subject matter have been described, but other embodiments are within the scope of the following claims. For example, the actions recited in the claims can be performed in a different order and still achieve desirable results. As one example, the processes depicted in the accompanying
10 figures do not necessarily require the particular order shown, or sequential order, to achieve desirable results. In certain implementations, multitasking and parallel processing may be advantageous.

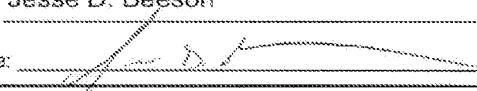
CONCLUSION

A system and method has been shown in the above embodiments for the effective implementation of a system and method for dividing and synchronizing a processing task across multiple processing elements/processors in hardware. While various preferred
5 embodiments have been shown and described, it will be understood that there is no intent to limit the invention by such disclosure, but rather, it is intended to cover all modifications falling within the spirit and scope of the invention, as defined in the appended claims. For example, the present invention should not be limited by software/program, computing environment, or specific computing hardware.

10

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of Invention	A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE
As the below named inventor, I hereby declare that:	
This declaration is directed to: ☒ The attached application, or ☐ United States application or PCT international application number _____ filed on _____	
The above-identified application was made or authorized to be made by me.	
I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.	
I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.	
WARNING: Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.	
LEGAL NAME OF INVENTOR	
Inventor: <u>Jesse D. Beeson</u> Date (Optional): _____	
Signature: <u></u>	
Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.	

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and
by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to
complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any
comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S.
Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO
THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-0199 and select option 2.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of Invention	A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE
-------------------------------	--

As the below named inventor, I hereby declare that:

This declaration is directed to: ☒ The attached application, or
☐ United States application or PCT international application number _____
filed on _____.

The above-identified application was made or authorized to be made by me.

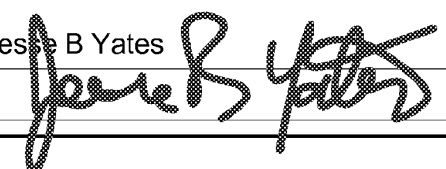
I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than **five (5)** years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Jesse B Yates Date (Optional) : _____
Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form **or must have been previously filed**. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

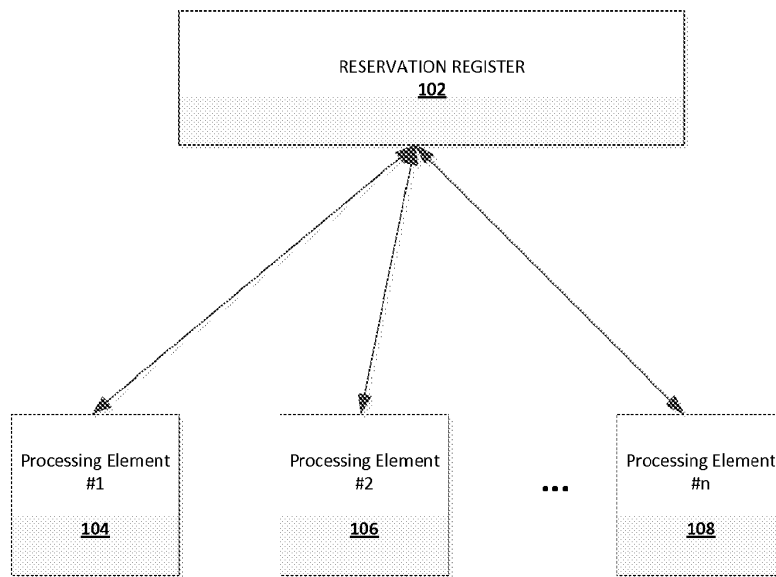


FIG. 1

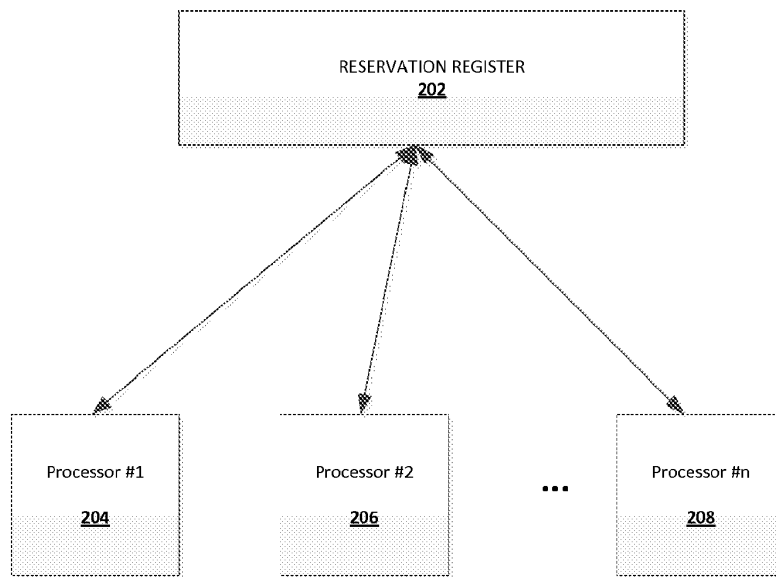


FIG. 2

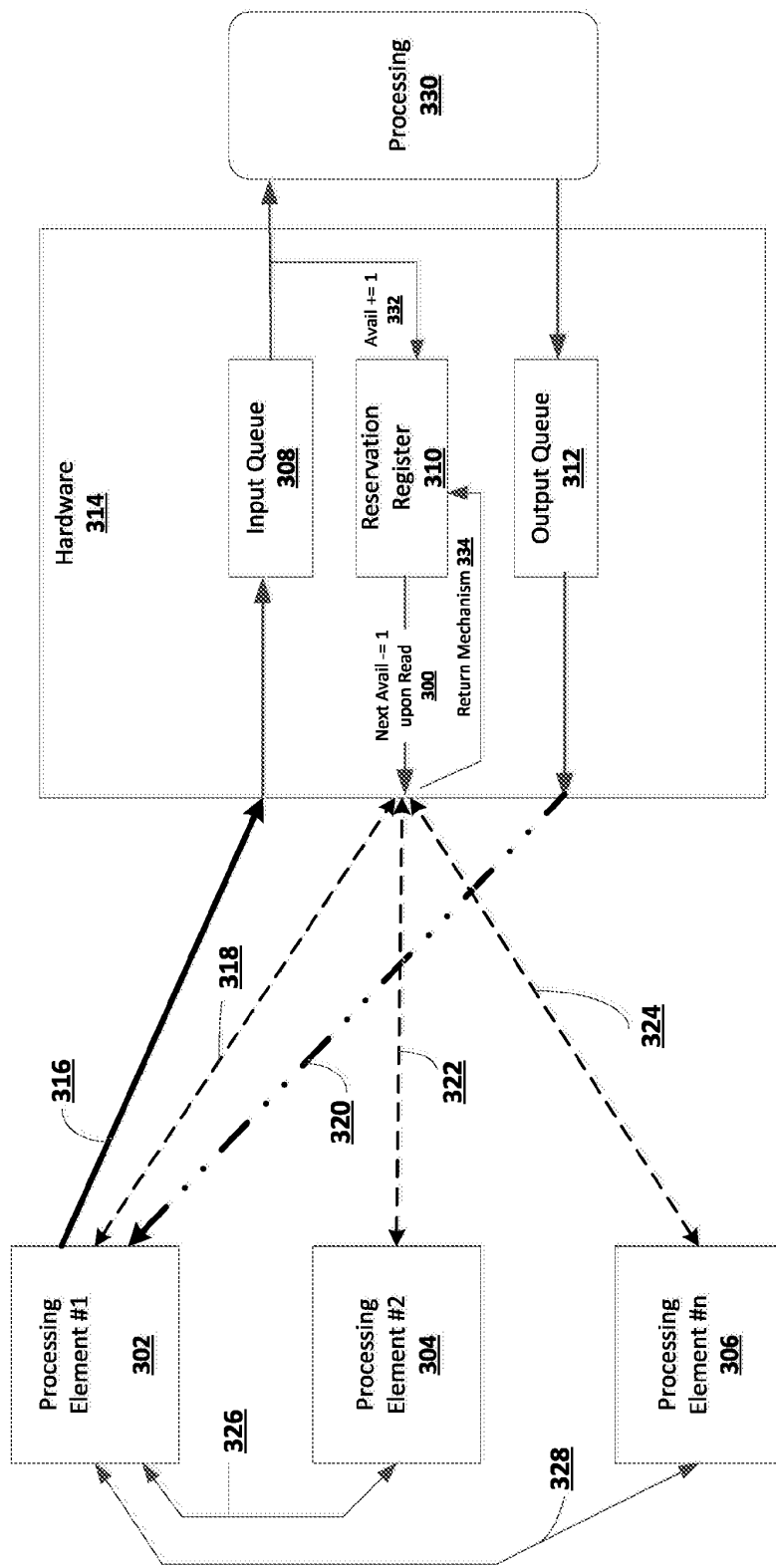


FIG. 3

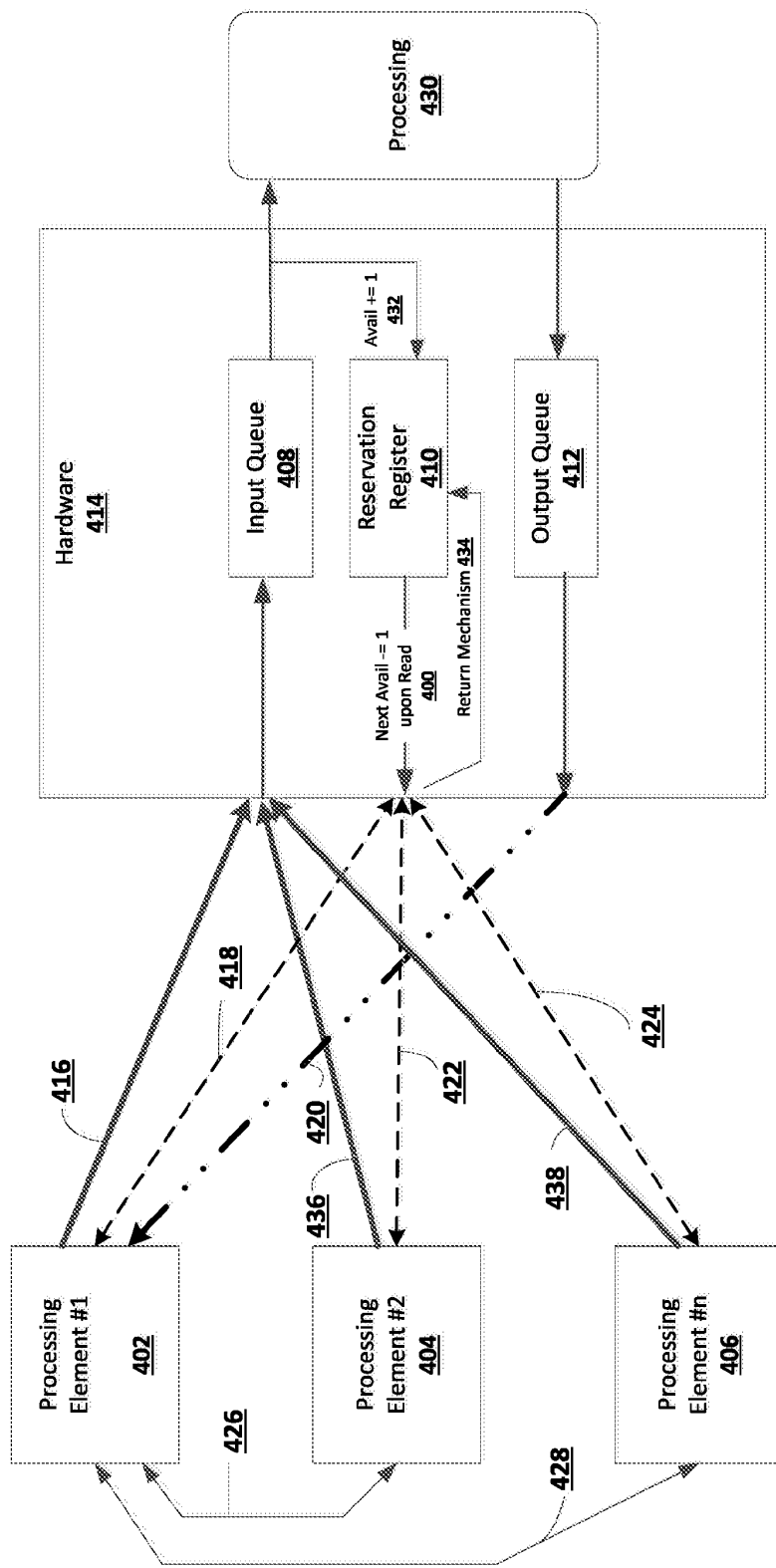


FIG. 4

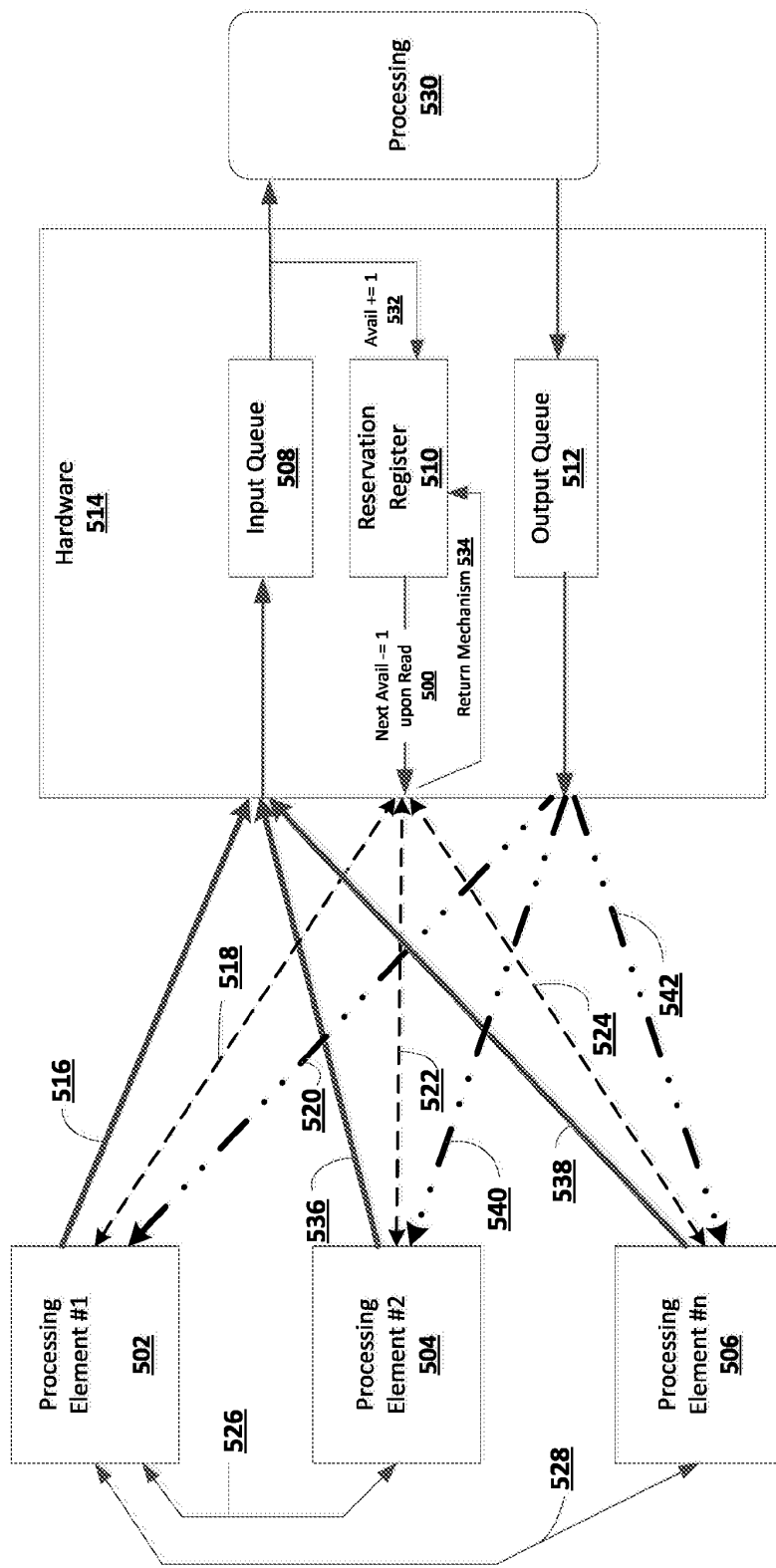


FIG. 5

Electronic Acknowledgement Receipt	
EFS ID:	17595526
Application Number:	14099844
International Application Number:	
Confirmation Number:	3222
Title of Invention:	A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE
First Named Inventor/Applicant Name:	Jesse D. Beeson
Customer Number:	26158
Filer:	Michael L. Gencarella/Sheryl Bernardo
Filer Authorized By:	Michael L. Gencarella
Attorney Docket Number:	C67508 1170US.1
Receipt Date:	06-DEC-2013
Filing Date:	
Time Stamp:	20:47:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$730
RAM confirmation Number	7390
Deposit Account	090528
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
-----------------	----------------------	-----------	-------------------------------------	------------------	------------------

1	Application Data Sheet	ADS.pdf	1245832 dfde5e9e2052766eab0ab190e4b324f1127a52a0b	no	7
Warnings:					
Information:					
2	Specification	App_CVP0020_12.pdf	182748 1324867d9eb05fc67b5e934b87e6365c0f36a8f3	no	34
Warnings:					
Information:					
3	Oath or Declaration filed	Dec.pdf	566395 29cd7b2ee2430f2a517af842d1b5f0c7637f3e9	no	2
Warnings:					
Information:					
4	Drawings-only black and white line drawings	Dwg_CVP0020_12.pdf	541998 decac87eee1c31b4ac2b9182f17e5dc505214cf3	no	5
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	33295 bf37c84851889063ceae1cd0894c59650bf18e6a	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			2570268		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

CLAIMS

1. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

an input queue implemented in hardware;

5 an output queue implemented in hardware;

a first processing element having access to said input queue and said output queue;

at least one second processing element in communication with said first processing element;

10 a reservation register implemented in hardware storing a value indicative of available space in a command queue, said reservation register accessible by both said first processing element and said at least second processing element;

computer storage storing instructions, which when executed by said at least one second processing element:

15 accesses said reservation register and reads said stored value;

determines when said read value indicates available space in said input queue for said first processing element to issue a command;

notifies said first processing element to issue said command to said input queue; and

20 wherein said first processing element receives notification from said at least second processing element regarding issuing the command, issues said command to said

input queue, and receives a response corresponding to said command from said output queue.

2. The system of claim 1, wherein said command queue is a FIFO buffer.

5

3. The system of claim 1, wherein said system is part of a storage area network (SAN) controller.

4. The system of claim 1, wherein said system is part of a network attached storage (NAS) controller.

10

5. The system of claim 1, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element.

15

6. The system of claim 1, wherein at least one third processing element executes said command and notifies said output queue to issue said response.

7. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

20

an input queue implemented in hardware;

CVP0020

Page 29 of 34

CONCURRENT VENTURES, LLC CONFIDENTIAL

an output queue implemented in hardware;

a first processing element having access to said input queue and said output queue;

at least one second processing element in communication with said input queue;

5 a reservation register implemented in hardware storing a value indicative of available space in a command queue, said reservation register accessible by both said first processing element and said at least second processing element;

computer storage storing instructions, which when executed by said at least one second processing element:

10 accesses said reservation register and reads said stored value;

determines when said read value indicates available space in said input queue for said first processing element to issue a command;

issue said command to said input queue; and

wherein said first processing element receives a response corresponding to said command from said output queue.

15

8. The system of claim 7, wherein said command queue is a FIFO buffer.

9. The system of claim 7, wherein said system is part of a storage area network (SAN) controller.

20

CONCURRENT VENTURES, LLC CONFIDENTIAL

10. The system of claim 7, wherein said system is part of a network attached storage (NAS) controller.

5 11. The system of claim 7, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element.

12. The system of claim 7, wherein at least one third processing element executes said command and notifies said output queue to issue said response.

10

13. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

an input queue implemented in hardware;

an output queue implemented in hardware;

15 a first processing element having access to said input queue and said output queue;

at least one second processing element in communication with said input queue and said output queue;

20 a reservation register implemented in hardware storing a value indicative of available space in a command queue, said reservation register accessible by both said first processing element and said at least second processing element;

CVP0020

Page 31 of 34

CONCURRENT VENTURES, LLC CONFIDENTIAL

computer storage storing instructions, which when executed by said at least one second processing element:

accesses said reservation register and reads said stored value;

determines when said read value indicates available space in said

5 input queue for said first processing element to issue a command;

issue said command to said input queue; and

receives a response corresponding to said command from said output queue.

10 14. The system of claim 13, wherein said command queue is a FIFO buffer.

15 15. The system of claim 13, wherein said system is either part of a storage area network (SAN) controller.

16. The system of claim 13, wherein said system is part of a network attached storage (NAS) controller.

17. The system of claim 13, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element.

20

18. The system of claim 13, wherein at least one third processing element executes said command and notifies said output queue to issue said response.

ABSTRACT OF THE DISCLOSURE

A shared counter resource, such as a register, is disclosed in the hardware, where the register representing how much free space there is in the command queue is accessible to one or more processing elements. When a processing element reads the “reservation” register, the hardware automatically decrements the available free space by a preconfigured amount (e.g., 1) and returns the value of the free space immediately prior to the read / reservation. If the read returns 0 (or a number less than the preconfigured amount), there was insufficient free space to satisfy the request. In the event there was insufficient space to satisfy the request the reservation register may be configured to reserve however much space was available or to not reserve any space at all. Any number of processing elements may read these registers and various scenarios are described where the input and output queues are accessible via various processing elements.

SCORE Placeholder Sheet for IFW Content

Application Number: 14099844

Document Date: 12/06/2013

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

- Drawings – Other than Black and White Line Drawings

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

To access the documents in the SCORE database, refer to instructions below.

At the time of document entry (noted above):

- Examiners may access SCORE content via the eDAN interface.
- Other USPTO employees can bookmark the current SCORE URL (<http://Score.uspto.gov/ScoreAccessWeb/>).
- External customers may access SCORE content via the Public and Private PAIR interfaces.

Form Revision Date: September 30, 2013



European Patent Office
80298 MUNICH
GERMANY

Questions about this communication ?

Contact Customer Services at www.epo.org/contact



GENCARELLA, Michael, L
Womble Carlyle Sandridge&Rice LLP
PO Box 7037
Atlanta, GA 30357
ETATS-UNIS D'AMERIQUE

Date

15.04.16

Reference	Application No./Patent No. 14867963.2 - 1957 PCT/US2014069153
Applicant/Proprietor Concurrent Ventures LLC	

Entry into the European phase before the European Patent Office

The following information describes the procedural steps required for entry into the European phase before the European Patent Office (EPO). You are advised to read it carefully because failure to take the necessary action in due time can lead to a loss of rights.

1. The above mentioned international patent application has been given the **European application No. 14867963.2**. This application number is to be used in correspondence with the EPO.
2. Applicants **without a residence or their principal place of business** in an EPC Contracting State may themselves initiate European processing of their international applications, provided they do so before expiry of the 31st month from the priority date.

During the European phase before the EPO as designated or elected Office, however, such applicants **must** be represented by a professional representative (Art. 133(2) and Art. 134(1) and (8) EPC).

Where, at the expiry of the time period laid down in Rule 163(5) EPC, the requirements of Article 133(2) EPC have not been complied with, the European patent application will be **refused**, pursuant to Rule 163(6) EPC.

Please note that a professional representative authorised to act before the EPO and who acted for the applicant during the international phase does not automatically become the representative for the European phase. Applicants are therefore strongly advised to appoint in good time any representative they wish to initiate the European phase for them; otherwise the EPO has to send all communications directly to the applicant.

3. Applicants **with a residence or their principal place of business** in an EPC Contracting State are not obliged to appoint for the European phase a professional representative authorised to act before the EPO. However, in view of the complexity of the procedure it is recommended that they do so.
4. Applicants and professional representatives are also strongly advised to initiate the European phase using **EPO Form 1200**. It is available free of charge from the EPO or via the EPO website at www.epo.org. Similarly, it can be generated with the Online Filing software, obtainable free of charge from the EPO (www.epoline.org) The use of the form is not compulsory.

-
5. Applicants wishing to use an address for correspondence which is different from the address of their seat or residence are advised to indicate this address in section 1 of EPO Form 1200. When acting as designated or elected Office, the EPO will accept an address for correspondence only if no professional representative must be or is appointed (Art. 133 and 134 EPC). This address must be the applicant's own address and must be located in an EPC Contracting State. Any address for correspondence accepted for the procedure in the international phase which does not fulfil those conditions will not be accepted in the procedure before the EPO in the European phase.
6. Where the EPO acts as designated or elected Office (Art. 22(1) and (3) and 39(1) PCT), to enter the European phase before the EPO, the **following acts** must be performed by the applicant within **31 months** from the date of filing of the international application or (where applicable) the earliest priority date:
- a) Supply a translation of the international application into an EPO official language, if the International Bureau did not publish the application in such language (Art. 22(1) PCT and R. 159(1)(a) EPC);
 - b) Specify the application documents, as originally filed or as amended, on which the European grant procedure is to be based (R. 159(1)(b) EPC);
 - c) Pay the filing fee and, where applicable, the additional fee for a European patent application comprising more than 35 pages (R. 159(1)(c) EPC, Art. 2, items 1, 1a Rules relating to Fees);
 - d) Pay the search fee where a supplementary European search report has to be drawn up (R. 159(1)(e) EPC);
 - e) Pay the designation fee if the time limit laid down in Rule 39(1) EPC (i.e. six months after publication of the international search report) has expired before the 31-month period pursuant to Rule 159(1) EPC (R. 159(1)(d) EPC);
 - f) File the written request for examination and pay the examination fee if the time limit laid down in Rule 70(1) EPC has expired before the 31-month period pursuant to Rule 159(1) EPC (R. 159(1)(f) EPC);
 - g) Pay the renewal fee in respect of the third year, if the fee has fallen due (see Rule 51(1) EPC) before expiry of the 31-month period pursuant to Rule 159(1) EPC (R. 159(1)(g) EPC);
 - h) File, where applicable, the certificate of exhibition referred to in Article 55(2) and Rule 25 EPC (R. 159(1)(h) EPC);
 - i) Pay the claims fees for the sixteenth and each subsequent claim when the application documents on which the European grant procedure is to be based comprise more than fifteen claims (R. 162(1) EPC). For applications entering the European phase on or after 1 April 2009, a higher amount is payable for the 51st and each subsequent claim (Decision of the Administrative Council of 14 December 2007 amending the Rules relating to Fees, OJ EPO 2008, 10).

If either the translation of the international application or the request for examination is not filed in time, or if the filing fee, the additional fee, the search fee, the designation fee or the examination fee is not paid in due time, the application shall be deemed to be withdrawn (R. 160(1) EPC).

7. Payment of fees

An up-to-date guidance for the payment of fees, expenses and prices and a list of the euro accounts of the European Patent Organisation are published in each issue of the Official Journal of the EPO. The guidance includes inter alia a reference to the latest version of the Schedule of fees and expenses where the amounts of fees are set out.

The Schedule of fees and expenses, published as a Supplementary publication to the Official Journal of the EPO, is also available on the EPO website (www.epo.org) and can be found under www.epo.org/schedule-of-fees, which allows the viewing, downloading and searching for individual fee amounts, both current and previous.

Applicants should always check the fee amounts applying at the time of payment.

Payments can be validly made by any person. Permissible methods of payment are laid down in Article 5 Rules relating to Fees. Please note that payment cannot be made by cheque sent to the EPO.

For information on the calculation of the additional fee for applications comprising more than 35 pages, see Notice from the European Patent Office dated 26 January 2009 concerning the 2009 fee structure (OJ EPO 2009, 118), Notice supplementing the notice from the European Patent Office dated 26 January 2009 concerning the 2009 fee structure (OJ EPO 2009, 338) and Guidelines for Examination in the EPO, A-III, 13.2.

For an overview of search and examination fees, see Notice from the European Patent Office dated 10 February 2014 (OJ EPO 2014, A31). Fee information is also published on the EPO website under www.epo.org/fees.

8. Restoration of priority right

Where the international application contains a priority claim to an earlier application and it has been filed within two months from the expiration of the 12-month priority period, a request for restoration before the EPO as designated Office (R. 49ter.2 PCT) applies under the following circumstances:

- a) No request for restoration filed before the receiving Office (RO) during the international phase (R. 26bis.3 PCT)
- b) Negative decision by the RO irrespective of the criterion applied (due care/unintentionality)
- c) Positive decision by the RO based on the unintentionality criterion.

For a request to be admissible, it must be filed and the requisite fee must be paid (R. 49ter.2(b)(iii) and R. 49ter.2(d) PCT). Attention is drawn to the one-month time limit under R. 49ter.2(b)(i) PCT for filing the request, which starts from the expiry of the 31-month time limit pursuant to Rule 159(1)EPC and Article 22(3) or 39(1)(b) PCT or, where applicable, from the date on which an effective request for early processing pursuant to Article 23(2) or 40(2) PCT is filed with the EPO as a designated/elected office ('Notice from the European Patent Office dated 21 February 2013 concerning the request for early processing', OJ EPO 2013, 158). The request for restoration also needs to state the reasons for the failure to file the international application within the priority period (Rule 49ter.2(b)(ii) PCT).

9. If the applicant had appointed a representative during the application's international phase, the present Form will be sent to the representative, asking him to inform the applicant accordingly. All subsequent communications will be sent to the applicant, or - if the EPO is informed of his appointment in time - to the applicant's European representative.
10. For more details about time limits and procedural acts before the EPO as designated or elected Office, see the EPO brochure "How to get an European patent", Guide for applicants - Part 2, PCT procedure before the EPO - "Euro-PCT" (EPO PCT Guide). This brochure, the list of professional representatives before the EPO, Form 1200 and details of the latest fees are available on the Internet under <http://www.epo.org>.

11. Programme for accelerated prosecution of European patent applications - "PACE"

Applicants wishing to accelerate proceedings before the EPO as designated or elected Office may request accelerated search and/or examination under the PACE programme (Notice from the European Patent Office dated 30 November 2015 concerning the programme for accelerated prosecution of European patent applications - "PACE", OJ EPO 2015, A93). To be as effective as possible, this should preferably be requested immediately on entry into the European phase.

Receiving Section



PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44bis)

Applicant's or agent's file reference C675081170WO	FOR FURTHER ACTION	See item 4 below
International application No. PCT/US2014/069153	International filing date (<i>day/month/year</i>) 08 December 2014 (08.12.2014)	Priority date (<i>day/month/year</i>) 06 December 2013 (06.12.2013)
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237		
Applicant CONCURRENT VENTURES, LLC		

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 bis.1(a).

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.

3. This report contains indications relating to the following items:

- | | | |
|-------------------------------------|--------------|---|
| ☒ | Box No. I | Basis of the report |
| ☐ | Box No. II | Priority |
| ☐ | Box No. III | Non-establishment of opinion with regard to novelty, inventive step and industrial applicability |
| ☐ | Box No. IV | Lack of unity of invention |
| ☒ | Box No. V | Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement |
| ☐ | Box No. VI | Certain documents cited |
| ☐ | Box No. VII | Certain defects in the international application |
| ☐ | Box No. VIII | Certain observations on the international application |

4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44bis.3(c) and 93bis.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44bis .2).

	Date of issuance of this report 07 June 2016 (07.06.2016)
The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland	Authorized officer Yukari Nakamura
Facsimile No. +41 22 338 82 70	e-mail: pt07.pct@wipo.int

Form PCT/IB/373 (January 2004)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

GENCARELLA, MICHAEL L

WOMBLE CARLYLE SANDRIDGE & RICE LLP PO BOX
7037 ATANTA GA 30357 USA

PCT

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

(PCT Rule 43bis.1)

Date of mailing
(day/month/year) **23 March 2015 (23.03.2015)**

Applicant's or agent's file reference
C675081170WO

FOR FURTHER ACTION
See paragraph 2 below

International application No.

PCT/US2014/069153

International filing date (day/month/year)

08 December 2014 (08.12.2014)

Priority date(day/month/year)

06 December 2013 (06.12.2013)

International Patent Classification (IPC) or both national classification and IPC

G06F 9/46(2006.01)i

Applicant

CONCURRENT VENTURES, LLC

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon
Metropolitan City, 302-701, Republic of Korea
Facsimile No. ++82 42 472 7140



Date of completion of this opinion

20 March 2015 (20.03.2015)

Authorized officer

YU, Jintae

Telephone No. +82-42-481-8530



**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US2014/069153

Box No. 1 Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of :
- ☒ the international application in the language in which it was filed
 - ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))
3. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:
- a. ☐ forming part of the international application as filed:
 - ☐ in the form of an Annex C/ST.25 text file.
 - ☐ on paper or in the form of an image file.
 - b. ☐ furnished together with the international application under PCT Rule 13*ter*.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.
 - c. ☐ furnished subsequent to the international filing date for the purposes of international search only:
 - ☐ in the form of an Annex C/ST.25 text file (Rule 13*ter*.1(a)).
 - ☐ on paper or in the form of an image file (Rule 13*ter*.1(b) and Administrative Instructions, Section 713).
4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.
5. Additional comments:

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US2014/069153

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	<u>1-18</u>	YES
	Claims	<u>NONE</u>	NO
Inventive step (IS)	Claims	<u>1-18</u>	YES
	Claims	<u>NONE</u>	NO
Industrial applicability (IA)	Claims	<u>1-18</u>	YES
	Claims	<u>NONE</u>	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 2011-0078700 A1 (BLACKBURN, R. A. et al.) 31 March 2011
D2: US 2008-0301697 A1 (SOUTHGATE, T. J. et al.) 04 December 2008
D3: US 2012-0102501 A1 (WADDINGTON, D. et al.) 26 April 2012
D4: US 2007-0016906 A1 (TRAUBEN, R. D. et al.) 18 January 2007
D5: US 2011-0055839 A1 (ALEXANDER, B. G. et al.) 03 March 2011

1. Novelty and Inventive Step

1.1 Claims 1-6

1.1.1 Independent Claim 1

The subject matter of claim 1 differs from the prior art documents D1 to D5 in that the subject matter of claim 1 discloses a system comprising a reservation register storing a value indicative of available space in a command queue and computer storage storing instructions which when executed by at least one second processing element: accesses the reservation register and reads the stored value, determines when the read value indicates available space in the input queue for the first processing element to issue a command, notifies the first processing element to issue the command, and wherein the first processing element receives notification from the at least second processing element regarding issuing the command, issues the command to the input queue and receives a response from the output queue. And, it is not obvious to a person skilled in the art by the documents, taken alone or in combination. Therefore, claim 1 meets the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

1.1.2 Dependent Claims 2-6

Claims 2-6 are dependent on claim 1 and therefore meet the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

1.2 Claims 7-12

Continued on Supplemental Box

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US2014/069153

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of : Box No. V

1.2.1 Independent Claim 7

The subject matter of claim 7 differs from the prior art documents D1 to D5 in that the subject matter of claim 7 discloses a system comprising a reservation register storing a value indicative of available space in a command queue and computer storage storing instructions which when executed by at least one second processing element: accesses the reservation register and reads the stored value, determines when the read value indicates available space in the input queue for the first processing element to issue a command, issues the command to the input queue, and wherein the first processing element receives a response corresponding the command from the output queue. And, it is not obvious to a person skilled in the art by the documents, taken alone or in combination. Therefore, claim 7 meets the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

1.2.2 Dependent Claims 8-12

Claims 8-12 are dependent on claim 7 and therefore meet the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

1.3 Claims 13-18

1.3.1 Independent Claim 13

The subject matter of claim 13 differs from the prior art documents D1 to D5 in that the subject matter of claim 13 discloses a system comprising a reservation register storing a value indicative of available space in a command queue and computer storage storing instructions which when executed by at least one second processing element: accesses the reservation register and reads the stored value, determines when the read value indicates available space in the input queue for the first processing element to issue a command, issues the command to the input queue, and receives a response corresponding the command from the output queue. And, it is not obvious to a person skilled in the art by the documents, taken alone or in combination. Therefore, claim 13 meets the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

1.3.2 Dependent Claims 14-18

Claims 14-18 are dependent on claim 13 and therefore meet the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

2. Industrial Applicability

Claims 1-18 are industrially applicable under PCT Article 33(4).



Entry into the European phase (EPO as designated or elected Office)

To the European Patent Office

European application number	EP14867963.2
PCT application number	PCT/US2014/069153
PCT publication number	WO2015085317
Applicant's or representative's reference	PE957775EP
International Filing Date	08.12.2014
International Searching Authority (ISA)	KR
International Preliminary Examining Authority (IPEA)	not applicable
1. Applicant Indications concerning the applicant(s) are contained in the international publication or were recorded by the International Bureau after the international publication. Changes which have not yet been recorded by the International Bureau are set out here:	☒ ☐
2. Representative Representative 1 This is the representative who will be listed in the European Patent Register and to whom notifications will be sent.	Name: HARGREAVES, Dr Timothy Edward Address of place of business: Marks & Clerk LLP Atholl Exchange 6 Canning Street Edinburgh, EH3 8EG United Kingdom Telephone: 0131 221 7000 Fax: 0131 221 7010 E-mail: thargreaves@marks-clerk.com
3. Authorisation Representative 1 An individual authorisation is attached. A general authorisation has been registered under No: A general authorisation has been filed, but not yet registered. The authorisation filed with the EPO as PCT receiving Office expressly includes the European phase.	☐ ☐ ☐ ☐
4. Request for examination Examination of the application under Art. 94 EPC is hereby requested. The examination fee is being (has been, will be) paid. Request for examination in an admissible non-EPO language: The applicant waives his right to be asked under Rule 70(2) EPC whether he wishes to proceed further with the application. The/Each applicant hereby declares that he is an entity or a natural person under Rule 6(4) EPC.	☒ ☐ ☐ ☐
5. Copies Additional copies of the documents cited in the supplementary European search report are requested. Number of additional sets of copies	☐
6. Documents intended for proceedings before the EPO Number of claims on entry into the European phase: 6.1 Proceedings before the EPO as designated Office (PCT I) are to be based on the following documents:	18

PE957775EP

the application documents published by the International Bureau (with all claims, description and drawings), where applicable with amended claims under Art. 19 PCT	☒
unless replaced by the amendments attached.	☐
<i>Where necessary, clarifications should be attached as 'Other documents'</i>	
6.2 Proceedings before the EPO as elected Office (PCT II) are to be based on the following documents:	
the documents on which the international preliminary examination report is based, including any annexes	☐
unless replaced by the amendments attached.	☐
<i>Where necessary, clarifications should be attached as 'Other documents'</i>	
If the EPO as International Preliminary Examining Authority has been supplied with test reports, these may be used as the basis of proceedings before the EPO.	☐
6.3 A copy of the results of the search carried out by the authority with which the previous application(s) whose priority is claimed was (were) filed is attached (R. 141(1) EPC).	☐
6.4 The applicant waives his right to the communication under Rules 161(1) or (2) and 162 EPC.	☐
7. Translations	
Translations in one of the official languages of the EPO (English, French, German) are attached as crossed below:	☐
<i>* In proceedings before the EPO as designated or elected Office (PCT I + II):</i>	
Translation of the international application (description, claims, any text in the drawings) as originally filed, of the abstract as published and of any indication under Rule 13bis.3 and 13bis.4 PCT regarding biological material	☐
Translation of the priority application(s) (to be filed only at the EPO's request, Rule 53(3) EPC)	☐
It is hereby declared that the international application as originally filed is a complete translation of the previous application (Rule 53(3) EPC)	☐
<i>* In addition, in proceedings before the EPO as designated Office (PCT I):</i>	
Translation of amended claims and any statement under Art. 19 PCT, if the claims as amended are to form the basis for the proceedings before the EPO (see Section 6).	☐
<i>* In addition, in proceedings before the EPO as elected Office (PCT II):</i>	
Translation of annexes to the international preliminary examination report	☐
8. Biological material	
The invention uses and/or relates to biological material deposited under Rule 31 EPC.	☐
The particulars referred to in Rule 31(1)(c) EPC (if not yet known, the depositary institution and the identification reference(s)) [number, symbols, etc.] of the depositor) are given in the international publication or in the translation submitted in Section 7 on:	☐
page(s) / line(s)	
The receipt(s) of deposit issued by the depositary institution	
is (are) enclosed.	☐
will be filed later.	☐
Waiver of the right to an undertaking from the requester pursuant to Rule 33(2) EPC attached.	☐
9. Nucleotide and amino acid sequences	
The international application discloses nucleotide and/or amino acid sequences.	☐
9.1 The sequence listing was filed under Rule 5.2(a) PCT, or furnished to the EPO as ISA under Rule 13ter.1(a) PCT, or is otherwise available to the EPO, in computer-readable format in accordance with WIPO ST.25.	☐
9.2	
The sequence listing is attached in computer-readable format in accordance with WIPO Standard ST.25	☐
The sequence listing is attached in PDF format.	☐

PE957775EP

The sequence listing does not include matter which goes beyond the content of the application as filed.	☐	
10. Designation of contracting states All the contracting states party to the EPC at the time of filing of the international patent application and designated in the international application are deemed to be designated (see Article 79(1) EPC).	☒	
11. Extension/Validation This application is deemed to be a request to extend the effects of the European patent application and the European patent granted in respect of it to all non-contracting states to the EPC designated in the international application with which extension or validation agreements were in force on the date on which the application was filed. However, the request is deemed withdrawn if the extension fee or the validation fee, whichever is applicable, is not paid within the prescribed time limit. 11.1 It is intended to pay the extension fee(s) for the following state(s): 11.2 It is intended to pay the validation fee(s) for the following state(s): Note: Under the automatic debiting procedure, extension and/or validation fees will be debited only for states indicated here unless the EPO is instructed otherwise before expiry of the period for payment.	☐	
12. List of enclosed documents		
	Original file name	Assigned file name
13. Mode of payment: Debit from deposit account Currency The European Patent Office is hereby authorised, to debit from the deposit account with the EPO any fees and costs indicated on the fees page. Deposit account number Account holder		
☒ EUR 28050604 Marks & Clerk LLP		
14. Any refunds should be made to the following EPO deposit account: Number and account holder		
☒ Marks & Clerk LLP, 28050604		
15. Fees		
	Factor/reducti on applied	Fee schedule
15-1	-190	1 300.00
15-2	1	585.00
15-3	1	1 635.00
15-4	0	235.00
15-5	0	585.00
15-6	1	120.00
15-7	0	15.00
Total:		EUR
		3 450.00
16. Annotations		
17. Signature(s) of applicant(s) or representative		
Place:	Edinburgh, UK	
Date:	23 June 2016	
Signed by:	Timothy Hargreaves 29477	
Representative name:	Timothy Edward HARGREAVES	
Capacity:	(Representative)	

PE957775EP

Table for section 6 of Form 1200.3

In accordance with the Notice from the European Patent Office dated 26 January 2009 concerning the 2009 fee structure (OJ EPO 2009, 118, and Guidelines for Examination in the EPO, April 2009, A-III, 13.2), the amount of the additional fee (Art. 2, item 1a, Rules relating to Fees) for the pages of this European patent application is calculated as follows:

Documents intended for proceedings before the EPO (R. 159 (1) (b) EPC) and for calculating the additional fee (Art. 2, item 1a, RFees):

	Page(s) from ... to ...	Number of pages
Description: International application as published	1 to 15	15
Claims: International application as published	16 to 18	3
Drawings: International application as published	1/5 to 5/5	5
Abstract: Default count: one page		1
Total number of pages		24
Fee-exempt pages (Art. 2, item 1a, RFees)		-35
Number of pages to be paid for		0
		(x 15 EUR per page)
Total amount payable	EUR	0

PE957775EP



Acknowledgement of receipt

We hereby acknowledge receipt of the form for entry into the European phase (EPO as designated or elected Office) as follows:

Submission number	4441326	
PCT application number	PCT/US2014/069153	
EP application number	14867963.2	
Date of receipt	23 June 2016	
Receiving Office	European Patent Office, The Hague	
Your reference	PE957775EP	
Applicant		
Country		
Documents submitted	package-data.xml application-body.xml	ep-euro-pct.xml epf1200.pdf (4 p.)
Submitted by	CN=Timothy Hargreaves 29477	
Method of submission	Online	
Date and time receipt generated	23 June 2016, 15:02 (CEST)	
Message Digest	49:8E:6A:B5:A3:AB:C9:4B:7B:38:38:63:AA:83:C1:56:17:5B:63:61	

Correction by the EPO of errors in debit instructions filed by eOLF

Errors in debit instructions filed by eOLF that are caused by the editing of Form 1038E entries or the continued use of outdated software (all forms) may be corrected automatically by the EPO, leaving the payment date unchanged (see decision T 152/82, OJ EPO 1984, 301 and point 6.3 ff ADA, Supplement to OJ EPO 10/2007).

/European Patent Office/



European Patent Office
80298 MUNICH
GERMANY

Questions about this communication ?

Contact Customer Services at www.epo.org/contact



BEESON, Jesse, D
240 Woodscape Court
Johns Creek, GA 30022-3244
ETATS-UNIS D'AMERIQUE

Date

22.07.16

Reference	Application No./Patent No. 14867963.2 - 1957 PCT/US2014069153
Applicant/Proprietor Concurrent Ventures LLC	

Notification of the data mentioned in Rule 19(3) EPC

In the above-identified patent application you are designated as inventor/co-inventor.
Pursuant to Rule 19(3) EPC the following data are notified herewith:

DATE OF FILING : 08.12.14

PRIORITY : US/06.12.13/ USA201314099844

TITLE : A SYSTEM AND METHOD FOR DIVIDING AND
SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE
PROCESSING ELEMENTS/PROCESSORS IN HARDWARE

DESIGNATED STATES : AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE
IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM
TR

Receiving Section





European Patent Office
80298 MUNICH
GERMANY

Questions about this communication ?

Contact Customer Services at www.epo.org/contact



YATES, Jesse B
2451 Cumberland Parkway SE Suite 300 3310
Atlanta, GA 30339
ETATS-UNIS D'AMERIQUE

Date

22.07.16

Reference	Application No./Patent No. 14867963.2 - 1957 PCT/US2014069153
Applicant/Proprietor Concurrent Ventures LLC	

Notification of the data mentioned in Rule 19(3) EPC

In the above-identified patent application you are designated as inventor/co-inventor.
Pursuant to Rule 19(3) EPC the following data are notified herewith:

DATE OF FILING : 08.12.14

PRIORITY : US/06.12.13/ USA201314099844

TITLE : A SYSTEM AND METHOD FOR DIVIDING AND
SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE
PROCESSING ELEMENTS/PROCESSORS IN HARDWARE

DESIGNATED STATES : AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE
IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM
TR

Receiving Section





European Patent Office
80298 MUNICH
GERMANY

Questions about this communication ?

Contact Customer Services at www.epo.org/contact



Hargreaves, Timothy Edward
Marks & Clerk LLP
Atholl Exchange
6 Canning Street
Edinburgh EH3 8EG
ROYAUME UNI

Date

26.07.16

Reference PE957775EP	Application No./Patent No. 14867963.2 - 1957 PCT/US2014069153
Applicant/Proprietor Concurrent Ventures LLC	

Communication pursuant to Rules 161(2) and 162 EPC

1. Amendment of the application (R. 161(2) EPC)

The above-mentioned international (Euro-PCT) application has entered the European phase.

Under Articles 28, 41 PCT and Rules 52, 78 PCT the application may be amended before a designated or elected Office.

In accordance with Rule 161(2) EPC, you may amend your application once within a **non-extendable period of six months** after notification of the present communication.

If filing amendments, you must identify them and indicate the basis for them in the application as filed. Failure to meet either requirement may lead to a communication from the Examining Division requesting that you correct this deficiency (R. 137(4) EPC).

The claims applicable on expiry of this period, i.e. those filed on entry into the European phase or in response to the present communication, will form the basis for the calculation of any claims fee to be paid (see page 2).

2 Claims fees under Rule 162 EPC

If the application documents on which the European grant procedure is to be based comprise more than fifteen claims, a claims fee shall be payable for the sixteenth and each subsequent claim within the period provided for in Rule 159(1) EPC.

- ☐ Based on the application documents currently on file, all necessary claims fees have already been paid (or the documents do not comprise more than 15 claims).
- ☐ All necessary fees will be debited automatically according to the automatic debit order.
- ☒ The claims fees due for the claims 16 to 18 were not paid within the above-mentioned period.

Registered letter

EPO Form 1226CC 06.15 (NFS) EUCL (18/07/16)

Page: 1 of 2

Any outstanding claims fee, either based on the current set of claims or on any amended claims to be filed pursuant to Rule 161 EPC (see page 1), may still be validly paid within a **non-extendable period of six months** after notification of this communication (R. 162(2) EPC).

If a payment is made for only some of the claims, you must indicate for which claims it is intended. If a claims fee is not paid in due time, the claim concerned is deemed to be abandoned (R. 162(4) EPC).

If claims fees have already been paid, but on expiry of the above-mentioned period there is a new set of claims containing fewer fee-incurring claims than before, the claims fees in excess of those due under Rule 162(2), second sentence EPC will be refunded (R. 162(3) EPC).

You are reminded that the supplementary search carried out according to Article 153(7) EPC will relate only to the last set of claims applicable on expiry of the above period AND will be confined to those fee-incurring claims for which fees have been paid in due time.

The claims fee is currently

EUR 235 for the 16th and each subsequent claim up to the limit of 50
EUR 585 for the 51st and each subsequent claim

Note to users of the automatic debiting procedure

Unless the EPO receives prior instructions to the contrary, the fees for all claims incurring fees will be debited on the last day of the period for payment. For further details see the Arrangements for the automatic debiting procedure, Annex A.1 to the ADA, Point 6.1(d), supplementary publication 3 - OJ EPO 2015.

Important information concerning fee amounts

Following any amendment to the Rules relating to Fees, the amount(s) mentioned in this communication may be different from the amount(s) **actually due on the date of payment**. The latest version of the Schedule of fees and expenses, published as a Supplement to the Official Journal of the EPO, is also available on the EPO website (www.epo.org) and can be found under www.epo.org/schedule-of-fees, which allows the viewing, downloading and searching for individual fee amounts, both current and previous.

Please note that procedural fees are usually adjusted every two years, on even years, with effect from 1 April.

Payments by cheque delivered or sent direct to the EPO are no longer accepted as from 1 April 2008 (see OJ EPO 2007, 626).

Receiving Section





European Patent Office
80298 MUNICH
GERMANY

Questions about this communication ?

Contact Customer Services at www.epo.org/contact



Hargreaves, Timothy Edward
Marks & Clerk LLP
Atholl Exchange
6 Canning Street
Edinburgh EH3 8EG
ROYAUME UNI

Date

14.09.16

Reference PE957775EP	Application No./Patent No. 14867963.2 - 1957 / 3077909 PCT/US2014069153
Applicant/Proprietor Concurrent Ventures LLC	

Communication of European publication number and information on the application of Article 67(3) EPC

Provisional protection under Article 67(1) and (2) EPC in the individual contracting states becomes effective when the conditions referred to in Article 67(3) EPC have been fulfilled. Provisional protection in the individual extension and validation states is governed by the national laws of the countries concerned. For more details, see Chapter III of the EPO brochure "National Law relating to the EPC" (www.epo.org/law-practice/legal-texts/national-law.html), which also contains information about the extension and validation system. Further information can also be found in the Official Journal of the European Patent Office.

Pursuant to Article 153(3) EPC the publication under Article 21 PCT of an international application for which the European Patent Office is a designated or elected Office takes the place of the publication of a European patent application.

The bibliographic data of the above-mentioned Euro-PCT application will be published on 12.10.16 in Section I.1 of the European Patent Bulletin. The European publication number is 3077909.

In all future communications to the European Patent Office, please quote the application number plus Directorate number.

Receiving Section





Letter accompanying subsequently filed items

Representative:

Dr Timothy Edward HARGREAVES
Marks & Clerk LLP
Atholl Exchange
6 Canning Street
Edinburgh EH3 8EG
United Kingdom

Phone: 0131 221 7000

Fax: 0131 221 7010

E-mail: edinburgh@marks-clerk.com

80298 Munich

Germany

Tel. +49(0)89 2399-0 | Fax -4465

P.O. Box 5818

2280 HV Rijswijk

Netherlands

Tel. +31(0)70 340-2040 | Fax -3016

10958 Berlin

Germany

Tel. +49(0)30 25901-0 | Fax -840

The document(s) listed below is (are) subsequently filed documents pertaining to the following application:

Application number

14867963.2

Applicant's or representative's reference

PE957775EP

	Description of document	Original file name	Assigned file name
1	Letter relating to the search and examination procedure	PE957775EP LETTER TO EPO 6.2.17.pdf	EPLETT-1.pdf
2	Amended claims (clean copy)	PE957775EP CLAIMS.pdf	CLMS-1.pdf
3	Amended claims with annotations	PE957775EP CLAIMS WITH ANNOTATIONS.pdf	CLMS-HWA-1.pdf

	Payment	
1	Mode of payment	Not specified

Signatures

Place: **Edinburgh, UK**
Date: **06 February 2017**
Signed by: **Timothy Hargreaves 29477**
Representative name: **Timothy Edward HARGREAVES**
Capacity: **(Representative)**

PE957775EP

Marks&Clerk LLP

Patent and Trade Mark Attorneys

Edinburgh Office

Atholl Exchange, 6 Canning Street, Edinburgh EH3 8EG

Tel: +44 (0)131 221 7000 Fax: +44 (0)131 221 7010

edinburgh@marks-clerk.com www.marks-clerk.com

European Patent Office

80298

Munich

Germany



Our Ref: TH/PE957775EP

Your Ref:

Date: 6 February 2017

By Online Filing

Dear Sirs

European Patent Application No 14867963.2 in the name of Concurrent Ventures, LLC

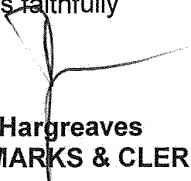
We hereby respond to the Communication pursuant to Rule 161(2) and 162 EPC. We replace the set of claims on file with the enclosed amended set of claims.

Various dependent claims have been combined as optional combinations (claims 11 and 12; claims 16, 17 and 18). Basis for the amendments is found in the set of claims as filed.

The claim set now consists of 15 claims and so no claims fees are payable.

No subject matter is abandoned. As a precaution, oral proceedings are requested in lieu of any adverse decision.

Yours faithfully


Tim Hargreaves
for MARKS & CLERK LLP

Encs. Amended set of claims
Marked-up version of amended set of claims.

CLAIMS

1. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

5 an input queue implemented in hardware;
 an output queue implemented in hardware;
 a first processing element having access to said input queue and said output queue;
 at least one second processing element in communication with said first processing element;

10 a reservation register implemented in hardware storing a value indicative of available space in a command queue, said reservation register accessible by both said first processing element and said at least second processing element;

 computer storage storing instructions, which when executed by said at least one second processing element:

15 accesses said reservation register and reads said stored value;
 determines when said read value indicates available space in said input queue for said first processing element to issue a command;
 notifies said first processing element to issue said command to said input queue; and

20 wherein said first processing element receives notification from said at least second processing element regarding issuing the command, issues said command to said input queue, and receives a response corresponding to said command from said output queue.

2. The system of claim 1, wherein said command queue is a FIFO buffer.

3. The system of claim 1, wherein said system is part of a storage area network (SAN) controller.

4. The system of claim 1, wherein said system is part of a network attached storage (NAS) controller.

5. The system of claim 1, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element.

6. The system of claim 1, wherein at least one third processing element executes said command and notifies said output queue to issue said response.

7. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

an input queue implemented in hardware;

an output queue implemented in hardware;

a first processing element having access to said input queue and said output queue;

at least one second processing element in communication with said input queue;

a reservation register implemented in hardware storing a value indicative of available space in a command queue, said reservation register accessible by both said first processing element and said at least second processing element;

computer storage storing instructions, which when executed by said at least one second processing element:

accesses said reservation register and reads said stored value;

determines when said read value indicates available space in said input queue for said first processing element to issue a command;

issue said command to said input queue; and

wherein said first processing element receives a response corresponding to said command from said output queue.

8. The system of claim 7, wherein said command queue is a FIFO buffer.

9. The system of claim 7, wherein said system is part of a storage area network (SAN) controller.

10. The system of claim 7, wherein said system is part of a network attached storage (NAS) controller.

11. The system of claim 7, wherein at least one of a) or b):

a) said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element;

~~b) 12. The system of claim 7, wherein at least one third processing element executes said command and notifies said output queue to issue said response.~~

Formatted: Indent: First line: 0 cm

~~1213. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:~~

~~an input queue implemented in hardware;~~

~~an output queue implemented in hardware;~~

~~a first processing element having access to said input queue and said output queue;~~

~~at least one second processing element in communication with said input queue and said output queue;~~

~~a reservation register implemented in hardware storing a value indicative of available space in a command queue, said reservation register accessible by both said first processing element and said at least second processing element;~~

~~computer storage storing instructions, which when executed by said at least one second processing element:~~

~~accesses said reservation register and reads said stored value;~~

~~determines when said read value indicates available space in said input queue for said first processing element to issue a command;~~

~~issue said command to said input queue; and~~

~~receives a response corresponding to said command from said output queue.~~

~~1314. The system of claim 1213, wherein said command queue is a FIFO buffer.~~

~~1415. The system of claim 1213, wherein said system is either part of a storage area network (SAN) controller.~~

~~1516. The system of claim 1312 wherein at least one of a), b) or c):~~

~~a) said system is part of a network attached storage (NAS) controller;~~

~~b)~~

~~17. The system of claim 13, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element;~~

~~c)~~

Formatted: Indent: First line: 0 cm

18. ~~The system of claim 13, wherein at least one third processing element executes~~
said command and notifies said output queue to issue said response.

CLAIMS

1. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

5 an input queue implemented in hardware;
 an output queue implemented in hardware;
 a first processing element having access to said input queue and said output queue;
 at least one second processing element in communication with said first processing element;

10 a reservation register implemented in hardware storing a value indicative of available space in a command queue, said reservation register accessible by both said first processing element and said at least second processing element;

 computer storage storing instructions, which when executed by said at least one second processing element:

15 accesses said reservation register and reads said stored value;
 determines when said read value indicates available space in said input queue for said first processing element to issue a command;
 notifies said first processing element to issue said command to said input queue; and

20 wherein said first processing element receives notification from said at least second processing element regarding issuing the command, issues said command to said input queue, and receives a response corresponding to said command from said output queue.

2. The system of claim 1, wherein said command queue is a FIFO buffer.

25 3. The system of claim 1, wherein said system is part of a storage area network (SAN) controller.

30 4. The system of claim 1, wherein said system is part of a network attached storage (NAS) controller.

5. The system of claim 1, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element.

6. The system of claim 1, wherein at least one third processing element executes said command and notifies said output queue to issue said response.

7. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

an input queue implemented in hardware;
an output queue implemented in hardware;
a first processing element having access to said input queue and said output queue;
at least one second processing element in communication with said input queue;
a reservation register implemented in hardware storing a value indicative of available space in a command queue, said reservation register accessible by both said first processing element and said at least second processing element;
computer storage storing instructions, which when executed by said at least one second processing element:

accesses said reservation register and reads said stored value;
determines when said read value indicates available space in said input queue for said first processing element to issue a command;
issue said command to said input queue; and
wherein said first processing element receives a response corresponding to said command from said output queue.

8. The system of claim 7, wherein said command queue is a FIFO buffer.

9. The system of claim 7, wherein said system is part of a storage area network (SAN) controller.

10. The system of claim 7, wherein said system is part of a network attached storage (NAS) controller.

11. The system of claim 7, wherein at least one of a) or b):
a) said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element;
b) at least one third processing element executes said command and notifies said output queue to issue said response.

12. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

an input queue implemented in hardware;
an output queue implemented in hardware;
a first processing element having access to said input queue and said output queue;
at least one second processing element in communication with said input queue and said output queue;

a reservation register implemented in hardware storing a value indicative of available space in a command queue, said reservation register accessible by both said first processing element and said at least second processing element;

computer storage storing instructions, which when executed by said at least one second processing element:

accesses said reservation register and reads said stored value;
determines when said read value indicates available space in said input queue for said first processing element to issue a command;
issue said command to said input queue; and
receives a response corresponding to said command from said output queue.

13. The system of claim 12, wherein said command queue is a FIFO buffer.

14. The system of claim 12, wherein said system is either part of a storage area network (SAN) controller.

15. The system of claim 12 wherein at least one of a), b) or c):

a) said system is part of a network attached storage (NAS) controller;
b) said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element;
c) at least one third processing element executes said command and notifies said output queue to issue said response.



Acknowledgement of receipt

We hereby acknowledge receipt of the following subsequently filed document(s):

Submission number	5013635	
Application number	EP14867963.2	
Date of receipt	06 February 2017	
Receiving Office	European Patent Office, The Hague	
Your reference	PE957775EP	
Applicant	All applicants as on file	
Documents submitted	package-data.xml epf1038.pdf (1 p.) CLMS-1.pdf\PE957775EP CLAIMS.pdf (4 p.)	ep-sfd-request.xml EPLTT-1.pdf\PE957775EP LETTER TO EPO 6.2.17.pdf (1 p.) CLMS-HWA-1.pdf\PE957775EP CLAIMS WITH ANNOTATIONS.pdf (4 p.)
Submitted by	CN=Timothy Hargreaves 29477	
Method of submission	Online	
Date and time receipt generated	06 February 2017, 12:38 (CET)	
Message Digest	0F:2B:F0:E0:B5:4D:9A:64:E6:9D:C4:CE:55:BC:3F:F0:09:17:CF:9A	

Correction by the EPO of errors in debit instructions filed by eOLF

Errors in debit instructions filed by eOLF that are caused by the editing of Form 1038E entries or the continued use of outdated software (all forms) may be corrected automatically by the EPO, leaving the payment date unchanged (see decision T 152/82, OJ EPO 1984, 301 and point 6.3 ff ADA, Supplement to OJ EPO 10/2007).

/European Patent Office/



Application No.: 14867963.2

The search has started on 07.04.17 (see Notice from the European Patent Office dated 03/2013, OJ EPO 2013, 153).

Receiving Section

**SUPPLEMENTARY
EUROPEAN SEARCH REPORT**

Application Number
EP 14 86 7963

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
Y	US 8 051 227 B1 (GEWIRTZ EVAN [US] ET AL) 1 November 2011 (2011-11-01) * column 1, line 39 - line 46 * * column 2, line 46 - column 3, line 7 * * column 4, line 51 - column 5, line 6 * * column 6, line 18 - line 22 * * column 9, line 22 - line 26 * -----	1-15	INV. G06F9/46 G06F9/52 G06F3/06
Y	US 2002/069245 A1 (KIM HAN-GY00 [KR]) 6 June 2002 (2002-06-06) * paragraph [0064] - paragraph [0067] * * paragraph [0083] - paragraph [0084] * -----	1-15	
A	US 7 631 122 B1 (WYATT DAVID [US]) 8 December 2009 (2009-12-08) * column 3, line 30 - line 48 * -----	1-15	
A	US 2004/181635 A1 (HURAS MATTHEW ALBERT [CA] ET AL) 16 September 2004 (2004-09-16) * the whole document * -----	1-15	
			TECHNICAL FIELDS SEARCHED (IPC)
			G06F
The supplementary search report has been based on the last set of claims valid and available at the start of the search.			
Place of search		Date of completion of the search	Examiner
The Hague		19 May 2017	García Gutiérrez, M
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

3
EPO FORM 1503 03.82 (P04C04)

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 14 86 7963

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

19-05-2017

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 8051227 B1	01-11-2011	EP 2386962 A1 US 8051227 B1	16-11-2011 01-11-2011
US 2002069245 A1	06-06-2002	US 2002069245 A1 US 2006010287 A1 US 2010138602 A1	06-06-2002 12-01-2006 03-06-2010
US 7631122 B1	08-12-2009	NONE	
US 2004181635 A1	16-09-2004	CA 2422252 A1 US 2004181635 A1	14-09-2004 16-09-2004

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

TITLE: A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE

APPLICANT: Concurrent Ventures LLC

IPC CLASSIFICATION: G06F9/46, G06F9/52, G06F3/06

EXAMINER: García Gutiérrez, M

CONSULTED DATABASES: WPI, EPDOC, DOSYS, NPL

CLASSIFICATION SYMBOLS DEFINING EXTENT OF THE SEARCH:

IPC:

CPC: G06F3/0601, G06F9/546, G06F9/50, G06F9/54, G06F9/52, G06F9/46, G06F9/466, G06F3/0659

FI/F-TERMS:

KEYWORDS OR OTHER ELEMENTS FEATURING THE INVENTION:

Hardware-assisted queue maintenance, multiple producers submit (enqueue) commands in parallel after obtaining a reservation by reading a hardware register (akin to memory location). Single consumer dequeues commands for processing. FIFO order. Possibility for a producer to cancel a reservation by writing to a hardware register. Responses to commands are placed on an output queue. Possibility to delegate issuing of command (ie, enqueueing).

The examination is being carried out on the **following application documents**

Description, Pages

1-15 as published

Claims, Numbers

1-15 filed on 06-02-2017

Drawings, Sheets

1/5-5/5 as published

Reference is made to the following documents; the numbering will be adhered to in the rest of the procedure.

D1 US 8 051 227 B1 (GEWIRTZ EVAN [US] ET AL) 1 November 2011 (2011-11-01)

D2 US 2002/069245 A1 (KIM HAN-GYOO [KR]) 6 June 2002 (2002-06-06)

1 The application does not meet the requirements of Article 84 EPC, because claims 1, 7, and 12 are not clear, as discussed next.

Clarity, claims 1, 7 and 12 (an input queue, a command queue)

2 Claim 1 defines "*an input queue implemented in hardware; an output queue implemented in hardware*" and "*a reservation register implemented in hardware storing a value indicative of available space in a command queue*", suggesting the presence of three queues (i.e., an input queue, an output queue, and a command queue) thus leading to an objection under Article 84 EPC.

2.1 However, the interpretation adopted in this opinion is that the aforementioned input queue and the aforementioned command queue are one and the same.

2.2 This interpretation is based on:

- 2.2.1 (page 6, lines 30-31 of the description) "a reservation register 310 implemented in hardware 314 storing a value indicative of available space in input queue 308"
- 2.2.2 (page 7, lines 14-17 of the description) "Also shown in FIG. 3, another additional processing element 330 takes the command from the input queue 308 causing the reservation register to increase its available space automatically in hardware 332 by the amount of space now created based on the removal of the command from the input queue."
- 2.3 Additionally, this interpretation is consistent with another feature in claim 1: "*notifies said first processing element to issue said command to said input queue*"
- 2.4 Objections similar to the above apply, mutatis mutandis, to claims 7 and 12.

Clarity, claims 1, 7 and 12 (decrement before fetch)

- 3 Claim 5 defines an essential feature (GL F-IV.4.5.2) that is missing in independent claim 1 (GL F-IV.4.5.1): "*said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element.*"
- 3.1 Since independent claim 1 does not contain this feature it does not meet the requirement following from Art. 84 EPC, taken in combination with Rule 43(1) and (3) EPC, that any independent claim must contain all the technical features essential to the definition of the invention.
- 3.2 Objections similar to the above apply, mutatis mutandis, to claim 11 defining an essential feature that is missing in independent claim 7.
- 3.3 Similarly for claim 15 defining an essential feature that is missing in independent claim 12.

Clarity, claims 1, 7 and 12 (command execution and response)

- 4 Claim 6 defines an essential feature (GL F-IV.4.5.2) that is missing in independent claim 1 (GL F-IV.4.5.1): "*at least one third processing element executes said command and notifies said output queue to issue said response.*"

- 4.1 Since independent claim 1 does not contain this feature it does not meet the requirement following from Art. 84 EPC, taken in combination with Rule 43(1) and (3) EPC, that any independent claim must contain all the technical features essential to the definition of the invention.
- 4.2 Objections similar to the above apply, mutatis mutandis, to claim 11 defining an essential feature that is missing in independent claim 7.
- 4.3 Similarly for claim 15 defining an essential feature that is missing in independent claim 12.

Independent claims 1, 7 and 12

- 5 The present application does not meet the requirements of Article 52(1) EPC, because the subject-matter of claim 1 is not inventive within the meaning of Article 56 EPC, lack of clarity notwithstanding (points 2 to 4.3).
- 5.1 D1 is considered to be the prior art closest to the subject-matter of claim 1.
- 5.2 Each feature of claim 1 (reproduced below, in italics) is followed by corresponding disclosure(s) in the prior art (inside square brackets, in normal font). Each distinguishing feature over the prior art (D1) appears in bold strikethrough. Additionally, terminology used in D1 instead of a distinguished feature appears (after that distinguished feature) between braces in a fixed font: {like this}.
- 5.3 *A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:*
[(column 1, lines 39-44 of D1) "According to one aspect of the invention, a command is received from a first agent via a first predetermined memory-mapped register, the first agent being one of multiple agents representing software processes, each being executed by one of multiple processor cores of a network processor in a network element."]
- 5.4 *an input queue implemented in hardware;*
~~**an output queue implemented in hardware;**~~
[(column 1, lines 44-46 of D1) "A first queue associated with the command is identified based on the first predetermined memory-mapped register, where the first queue was allocated in a memory."]

[(column 3, lines 3-7 of D1) "All maintenance of the queue state is done automatically in hardware, and will be atomically visible, along with the new queue entry (or the new head of the queue for a pop), to the next access."]

- 5.5 *a first processing element having access to said input queue ~~and said output queue~~;*
at least one second processing element in communication with said first processing element;
[(column 2, lines 55-58 of D1) "Once a queue is set up, it can be used concurrently by any number of agents in the system, both producers (e.g., agents to write to the queue) and consumers (e.g., agents to read from the queue)."]
- 5.6 *a reservation register implemented in hardware storing a value indicative of available space in a ~~command~~ queue,*
[(column 2, lines 59-66 of D1) "Another register (also referred to as a state register or status register) holds the dynamic state of the queue, including a read pointer and a write pointer, queue occupancy, and/or number of free writeable entries for flow control purposes. This register may be updated by hardware logic that manages the queues. Software can then perform queue operations by performing simple reads and writes to one or more data access registers (e.g., memory mapped registers)."]
- 5.7 *said reservation register accessible by both said first processing element and said at least second processing element;*
[(column 4, lines 56-61 of D1) "When an agent wants to write an element into the queue, it first reads the reservation register to see if an entry is available. An agent may be one of multiple agents representing software processes, each being executed by one of multiple processor cores of a network processor in a network element."]
- 5.8 *computer storage storing instructions, which when executed by said at least one second processing element:*
accesses said reservation register and reads said stored value;
determines when said read value indicates available space in said input queue for said first processing element
to ~~issue a command~~ {write an element onto the queue} ;

[(column 4, lines 51-61 of D1) "The queue hardware can return a pass/fail value to the agent in response to the read, depending on whether there is a reservation available, which may be specified via a reserved field (not shown) of state register 106. When an agent receives a pass value, it can perform a write to one of the data access registers. If it receives a fail value, it must attempt to obtain a reservation again. If the agent decides not to write an element on to the queue, the agent may be required to write the reservation register to free the credit for subsequent use."]

- 5.9 ~~**notifies said first processing element to issue said command to said input queue; and wherein said first processing element receives notification from said at least second processing element regarding issuing the command, issues said command to said input queue, and receives a response corresponding to said command from said output queue.**~~
- 5.10 The technical effect resulting from the distinguishing feature is increased combined throughput of the queuing system.
- 5.11 The objective technical problem consists in adapting the method of D1 to increase the combined throughput of the queuing system.
- 5.12 Faced with this objective technical problem and seeking solution in the appropriate technical field, the person skilled in the art would find D2 in the same technical field of D1 and of the application.
- 5.13 D2 discloses:
- 5.13.1 A command queue (points 5.6 and 5.8)
(paragraph 0065 of D2) "Each block device driver has an I/O request queue to store the I/O requests to the device."
- 5.13.2 Offloading the task of issuing a command to another thread (point 5.9):
(paragraph 0067 of D2) "FIG. 8 shows a situation where the request function 229, instead of directly issuing a command, activates a device accessing thread 230 so that the device accessing thread 230 can issue a command based on the information in the request queue. A thread refers to a single use of a program that can handle multiple users."

- 5.14 It is common general knowledge of the skilled person (GL G-VII.3.1) that an output queue (points 5.4 and 5.5) is an implementation choice for buffering request results from a storage device.
- 5.15 The skilled person would then adapt the method of D1 to incorporate the teachings above and so arrive at the teaching of claim 1 without exercising any inventive effort.
- 5.16 Therefore the subject matter of claim 1 is not inventive within the meaning of Article 56 EPC.
- 5.17 Objections similar to the above apply, mutatis mutandis, to claims 7 and 12, whose subject-matter is not inventive within the meaning of Article 56 EPC, given the ample similarity of said claims with claim 1.

Claims 2, 8 and 13

- 6 The subject-matter of claim 2 is not inventive within the meaning of Article 56 EPC, as discussed next.
- 6.1 As additional feature, claim 2 defines "*said command queue is a FIFO buffer.*"
- 6.2 This feature is disclosed in D1: (column 1, lines 14-16 of D1) "A queue is a data structure with FIFO properties where agents push elements onto the queue (writes) and pop elements off of the queue (reads)."
- 6.3 Objections similar to the above apply, mutatis mutandis, to claims 8 and 13, whose subject-matter is not inventive within the meaning of Article 56 EPC, given the ample similarity of said claims with claim 2.

Claims 3, 4, 9, 10 and 14

- 7 The subject-matter of claim 3 is not inventive within the meaning of Article 56 EPC, as discussed next.
- 7.1 As distinguishing feature, claim 3 defines "*said system is part of a storage area network (SAN) controller.*"

- 7.2 In D1, a hardware-based queue system constitutes an implementation choice strongly hinted at for a Storage Area Network (SAN) controller:
(column 9, lines 22-26 of D1) "FIG. 7 is a block diagram illustrating a network element according to one embodiment of the invention. Network element 700 may be implemented as any network element having queue systems as shown in FIGS. 1-2 and 5."
- 7.3 The presence of the additional feature in claim 3 is not inventive because the skilled person would follow the above disclosures in the context of the system of D1 without exercising any inventive skill.
- 7.4 Objections similar to the above apply, mutatis mutandis, to claims 4, 9, 10 and 14, whose subject-matter is not inventive within the meaning of Article 56 EPC, given the ample similarity of said claims with claim 3.

Claim 5

- 8 The subject-matter of claim 5 is not inventive within the meaning of Article 56 EPC, as discussed next.
- 8.1 As additional feature, claim 5 defines "*said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element.*"
- 8.2 This feature is disclosed in D1:
- 8.2.1 (column 5, lines 3-6 of D1) "The available reservation count is maintained by hardware: it is decremented when a successful reservation read request is processed, and incremented when either a reservation register write is seen, or when an element is popped off of the queue."
- 8.2.2 (column 6, lines 18-22 of D1) "In addition, the number of free entries field 113 may also be updated by hardware logic, for example, by decrementing field 113, since an entry has been pushed into the queue. These operations are performed atomically and controlled by hardware logic."

Claim 6

- 9 The subject-matter of claim 6 is not inventive within the meaning of Article 56 EPC, as discussed next.

- 9.1 As additional feature, claim 6 defines "*at least one third processing element executes said command and notifies said output queue to issue said response.*"
- 9.2 D1 discloses processing queue items using producers and consumers: (column 2, lines 55-58 of D1) "Once a queue is set up, it can be used concurrently by any number of agents in the system, both producers (e.g., agents to write to the queue) and consumers (e.g., agents to read from the queue)."

Claims 11 and 15

- 10 The subject-matter of claim 15 is not inventive within the meaning of Article 56 EPC, as discussed next.
- 10.1 Each feature of claim 15 (reproduced below, in italics) is followed by corresponding disclosure(s) in the prior art (inside square brackets, in normal font).
- 10.2 *The system of claim 12 wherein at least one of a), b) or c):*
a) said system is part of a network attached storage (NAS) controller;
[As discussed for claim 3 under points 7 ff., D1 discloses this feature.]
- 10.3 *b) said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element;*
[As discussed for claim 5 under points 8 ff., D1 discloses this feature.]
- 10.4 *c) at least one third processing element executes said command and notifies said output queue to issue said response.*
[As discussed for claim 6 under point 9 ff., D1 discloses this feature.]
- 10.5 Objections similar to the above apply, mutatis mutandis, to claim 11, whose subject-matter is not inventive within the meaning of Article 56 EPC, given the ample similarity of said claim with claim 15.

Typographical errors

11 Claim 14 has a typographical error: the word "either" appears without serving any grammatical function. The interpretation adopted in this opinion for claim 14 is as follows (text deletions shown in bold strikethrough):

"The system of claim 12, wherein said system is ~~either~~ part of a storage area network (SAN) controller."

Concluding remarks

Should the applicant regard some particular matter as patentable, independent claims should be filed taking account i.a. of Rule 43 EPC. The applicant should also indicate in the letter of reply:

- the difference of the subject-matter of any new claim vis-à-vis the state of the art (D1 and D2) and the technical significance thereof,
- the technical problem solved by this difference,
- how this technical problem is solved in a non-obvious manner by the features of all independent claims.

To meet the requirements of Rule 42 EPC, D1 and D2 should be identified in the description and the relevant contents should be discussed in a manner adequate to allow full understanding of the subject of protection and in order to ensure that it is clear from the description which features of the subject-matter of any new independent claim are known from D1 and D2.

If filing amended claims the applicant should at the same time bring the description into conformity with the amended claims. Care should be taken during revision, not to add subject-matter which extends beyond the content of the application as originally filed (Article 123(2) EPC).

In order to safeguard the well-established principle of legitimate expectations, it is reminded that the applicant does not have the benefit of the doubt in matters concerning Article 123(2) EPC.

Any possible extension of subject-matter must be assessed with respect to the content only of the application as filed; this content does not include the abstract and the content of priority documents.

In order to facilitate the examination of the conformity of the amended application with the requirements of Article 123(2) EPC, the applicant is requested to clearly identify (Rule 137(4) EPC) the amendments carried out, irrespective of whether they concern amendments by addition, replacement or deletion, and to indicate the passages of the application as filed on which these amendments are based.

These indications should preferably be submitted on a marked-up copy of the relevant parts of the application as filed.



European Patent Office
80298 MUNICH
GERMANY

Questions about this communication ?

Contact Customer Services at www.epo.org/contact



Hargreaves, Timothy Edward
Marks & Clerk LLP
Atholl Exchange
6 Canning Street
Edinburgh EH3 8EG
ROYAUME UNI

Date

13.06.17

Reference PE957775EP	Application No./Patent No. 14867963.2 - 1879 / 3077909 PCT/US2014069153
Applicant/Proprietor Concurrent Ventures LLC	

Communication

The extended European search report is enclosed.

The extended European search report includes, pursuant to Rule 62 EPC, the supplementary European search report (Art. 153(7) EPC) and the European search opinion.

Copies of documents cited in the European search report are attached.

☒ 0 additional set(s) of copies of such documents is (are) enclosed as well.

Refund of the search fee

If applicable under Article 9 Rules relating to fees, a separate communication from the Receiving Section on the refund of the search fee will be sent later.

Should you wish to further prosecute this application in the examination phase, your attention is drawn to the provisions of Rule 70a EPC. An invitation to respond to the extended European search report will be issued shortly (R. 70(2) EPC).





European Patent Office
80298 MUNICH
GERMANY

Questions about this communication ?

Contact Customer Services at www.epo.org/contact



Hargreaves, Timothy Edward
Marks & Clerk LLP
Atholl Exchange
6 Canning Street
Edinburgh EH3 8EG
ROYAUME UNI

Date

30.06.17

Reference PE957775EP	Application No./Patent No. 14867963.2 - 1879 / 3077909 PCT/US2014069153
Applicant/Proprietor Concurrent Ventures LLC	

Communication pursuant to Rules 70(2) and 70a(2) EPC

A supplementary European search report has been drawn up concerning the above-identified European patent application (publication number: 3077909).

Since the request for examination has been filed (R. 70(1), 159(1)(f), Art. 94(1) EPC) prior to the transmission of the supplementary European search report, you are hereby invited to indicate within

six months

of notification of this communication whether you wish to proceed further with the European patent application.

If you do not indicate in due time that you wish to proceed further with the European patent application, it **will be deemed to be withdrawn** (R. 70(3) EPC).

You are invited, within the above-mentioned six-month period, to comment on the objections raised in the opinion accompanying the European search report and/or to file any amendments to the description, claims and drawings correcting any deficiencies noted in the opinion (R. 70a(2), R. 137(2) EPC; Guidelines for Examination in the EPO, B-XI, 8).

If filing amendments, you must identify them and indicate the basis for them in the application as filed. Failure to meet either requirement may lead to a communication from the Examining Division requesting that you correct this deficiency (R. 137(4) EPC).

Should the reply to the invitation pursuant to Rule 70a(2) EPC be filed in an admissible non-EPO language, a translation is to be submitted within one month of its filing (R. 6(2) EPC).

Should you not comply with this invitation within the time limit, the application **will be deemed to be withdrawn** in accordance with Rule 70a(3) EPC.

Receiving Section



Registered letter

EPO Form 1224 11.12 (RTB/ESOP01=N) DMEX

page 1 of 1



European Patent Office
80298 MUNICH
GERMANY

Questions about this communication ?

Contact Customer Services at www.epo.org/contact



Hargreaves, Timothy Edward
Marks & Clerk LLP
Atholl Exchange
6 Canning Street
Edinburgh EH3 8EG
ROYAUME UNI

Date

16.02.2018

Reference PE957775EP	Application No./Patent No. 14867963.2 - 1221 / 3077909
Applicant/Proprietor Concurrent Ventures LLC	

Noting of loss of rights pursuant to Rule 112(1) EPC

The European patent application cited above is deemed to be withdrawn because

- ☒ no indication of the desire to proceed further with the application was furnished within the time limit specified in the communication (EPO Form 1082/1224) issued under Rule 70(2) EPC (R. 70(3) EPC).
- ☒ no response has been filed to the invitation to correct any deficiencies noted in the opinion accompanying the (supplementary) European search report within the time limit specified in the communication (EPO Form 1082/1224) issued under Rule 70a(2) EPC (R. 70a(3) EPC).

Means of redress

Request for a decision (R. 112(2) EPC)

If the applicant considers that the finding of the European Patent Office is inaccurate, he may, within a (non-extendable) period of **two months** after notification of this communication, apply in writing for a decision on the matter. The application can only lead to the finding being reversed if this does not actually correspond to the factual or legal situation.

Further processing (Art. 121 EPC)

The legal consequence of the failure to observe the time limit(s) shall be deemed not to have ensued if, within a (non-extendable) period of **two months** after notification of this communication, further processing is requested by payment of the fee(s) prescribed under Article 2(1)12 of the Rules relating to Fees and the omitted act(s) is (are) completed (R. 135(1) EPC).

The time limits under Rule 70(2) EPC and Rule 70a(2) EPC are legally independent from each other. Therefore, where both have been missed, further processing must be requested, and a further processing fee must be paid, in respect of each of them. In both cases, the flat-rate fee for further processing (Art. 2(1)12, third indent, RFees) is due.

Registered letter

EPO Form 1099 RTB 12.17 ADWI 11

page 1 of 2

Making payments

For payments made via deposit account, please note that as from 1 December 2017 debit orders will only be carried out if filed in an electronically processable format (xml), using an accepted means of filing as laid down in the Arrangements for deposit accounts (ADA), published in the Supplementary publication in the Official Journal.

All relevant information related to the modes of payment of fees to the EPO can be retrieved from the EPO website at "**Making Payments**".

Information concerning fee amounts

Procedural fees are usually adjusted every two years, on even years, with effect from 1 April. Therefore, before making a payment, parties should verify the amounts actually due on the date of payment using the applicable version of the Schedule of fees and expenses, published as a Supplement to the Official Journal of the EPO, available on the EPO website (www.epo.org) at www.epo.org/schedule-of-fees. The Schedule of fees table allows the viewing, downloading and searching of individual fee amounts, both current and previous.

Important note to users of the automatic debiting procedure

The fee for further processing will be debited automatically on the day on which the above-mentioned omitted act is completed.

Receiving Section



Letter accompanying subsequently filed items

Representative:

Dr Timothy Edward HARGREAVES
Marks & Clerk LLP
Atholl Exchange
6 Canning Street
Edinburgh EH3 8EG
United Kingdom

Phone: 0131 221 7000

Fax: 0131 221 7010

E-mail: edinburgh@marks-clerk.com

80298 Munich
Germany
Tel. +49(0)89 2399-0 | Fax -4465

P.O. Box 5818
2280 HV Rijswijk
Netherlands
Tel. +31(0)70 340-2040 | Fax -3016

10958 Berlin
Germany
Tel. +49(0)30 25901-0 | Fax -840

The document(s) listed below is (are) subsequently filed documents pertaining to the following application:

Application number

14867963.2

Applicant's or representative's reference

PE957775EP

	Description of document	Original file name	Assigned file name
1	Letter relating to the search and examination procedure	Response to European Search Opinion - PE957775EP.pdf	EPLETT-1.pdf
2	Amended claims (clean copy)	PE957775EP - Amended claims (clean).pdf	CLMS-1.pdf
3	Amended claims with annotations	PE957775EP - Amended claims (annotated).pdf	CLMS-HWA-1.pdf
4	Amended description with annotations	PE957775EP - Amended page 1 (annotated).pdf	DESC-HWA-1.pdf
5	Amended description (clean copy)	PE957775EP - Amended page 1 (clean).pdf	DESC-1.pdf

	Payment	
1	Method of payment	Not specified

Signatures

Place: **Glasgow, UK**
Date: **23 April 2018**
Signed by: **Timothy Hargreaves 29477**
Representative name: **Timothy Edward HARGREAVES**
Capacity: **(Representative)**

PE957775EP

Marks & Clerk LLP

Atholl Exchange, 6 Canning Street, Edinburgh EH3 8EG, UK
T +44 131 221 7000 | F +44 131 221 7010
edinburgh@marks-clerk.com | www.marks-clerk.com

European Patent Office
80298
Munich
Germany

Our Ref: TH/PE957775EP

Your Ref:

Date: 23 April 2018

VIA ONLINE FILING

Dear Sirs

European Patent Application No 14867963.2 in the name of Concurrent Ventures, LLC

We hereby respond to the Communication pursuant to Rules 70(2) and 70a(2) EPC, and we confirm that the applicant wishes to proceed further with the application.

We respond to the objections raised in the European search opinion as follows.

We also request further processing. The omitted act is completed by way of the present response. The further processing fees are being paid under separate cover.

Amendments

We replace the set of claims on file with the enclosed amended set of claims.

A marked-up version of the amended set of claims, showing amendments using underlining and strikeout, is enclosed in case it is of assistance to the examiner.

Claim 1 is amended to include the features of dependent claims 5 and 6, in view of the examiner's objection concerning lack of clarity set out in sections 3 and 4 of the search opinion. Basis for the amendment is found in the combination of claims 1, 5 and 6 of the application as filed.

Claim 1 is also amended to replace "a command queue" with "said input queue" in view of the examiner's objection under section 2 of the search opinion. Claim 1 now recites two queues (the input queue and the output queue) rather than three queues. Basis for the amendment is found in the passages cited by the examiner at page 6, lines 30 to 31 and page 7, lines 14 to 17 and the amendments provides internal consistency to claim 1 as noted by the examiner.

Amendments corresponding to those made to claim 1 are made to the other independent claims, claim 5 (previously claim 7) and claim 9 (previously claim 13).

Claims 5, 6 and 11 are deleted, and consequential amendments are made to the dependent claims.

This letter is sent on behalf of Marks & Clerk LLP, a limited liability partnership registered in England and Wales with registered number OC343273. The firm is regulated by the Intellectual Property Regulation Board (IPREG). A list of members' names is open to inspection at our registered office, 90 Long Acre, London WC2E 9RA, UK. Marks & Clerk is a trading name of Marks & Clerk LLP and other entities within the Marks & Clerk network of associated operating firms, each of which is a separately constituted entity. Marks & Clerk offices are located in Beijing and Hong Kong (China); Kuala Lumpur (Malaysia); Singapore; Ottawa (Canada); Paris and Sophia Antipolis (France); Luxembourg; Aberdeen, Birmingham, Cambridge, Edinburgh, Glasgow, London, Manchester and Oxford (UK).

53169097-1-THARGREAVES

We also replace page 1 of the description with the enclosed page 1, which has been amended to identify and discuss D1 and D2, and to clarify that aspects of the invention are in accordance with the claims.

Comments

D1 relates to programmable queue structures for multiprocessors. D1 describes the use of "agents" writing commands into a queue. These agents read a reservation register to see if an entry is available. The queue hardware can return a pass/fail value to the agent in response to the read, depending on whether reservation is available, which is specified by a reservation field of a state register.

If an agent receives a pass value, it can perform a write to a data access register. If the agent receives a fail value, it must attempt to obtain reservation again. If an agent decides not to write a command on to the queue, the agent is then required to write to the reservation register to free up space for subsequent use.

The examiner has conceded that D1 does not disclose an output queue. The examiner has also conceded that D1 does not disclose the feature of notifying *"...said first processing element to issue said command to said input queue; and wherein said first processing element receives notification from said at least second processing element regarding issuing the command, issues said command to said input queue, and receives a response corresponding to said command from said output queue"*.

D1 also does not disclose at least the newly included feature of claim 1 of upon determining when said read value indicates available space in said input queue, the second processing element notifies the first processing element to issue the command to the input queue.

By providing the novel features as outlined above, the offloading of processing load of a processing element in determining what command to issue may be obtained, thereby potentially ensuring that command queues are not overfilled whilst keeping processing time to a minimum and keeping the command queue to a desirable size.

A technical problem addressed by the claimed invention in view of D1 may be considered to be the provision of an improved, or at least alternative, system and method of performing a processing task.

The solution provided by the claimed invention is neither disclosed nor suggested in D1.

Turning to D2, this document relates to a disk system or interface that can be directly attached to a network. D2 seems merely to describe a method of issuing commands from an input queue (referred to as a "request" queue) to an NAD device using a thread, based on information in the request queue. This seems to be merely a method of outputting commands stored in the input queue to an external device.

The examiner cites paragraphs [0065] and [0067] of D2 in particular. These paragraphs describe the structure of a block device driver. Paragraph [0065] of D1 describes that each block driver has an I/O request queue to store I/O requests to the device. Paragraph [0067] describes a request function, which instead of directly issuing a command, activates a device accessing thread so that the device accessing thread can issue a command based on the information in the request queue.

It appears that the above-mentioned paragraphs of D2 refer to a process for controlling the output and execution of commands stored within the I/O request queue to an NAD device by using the thread (see Fig. 8 and paragraph [0066]).

In contrast, as described above, embodiments of the present claimed invention are directed to controlling the commands issued to the input command queue by offloading the processing load, to determine what command to issue, of a processing element.

Thus, D2 seems to be directed to controlling the output and execution of commands output from a request queue whereas the present invention is concerned primarily with management of the input to an input queue.

D2 and D1, whether considered alone or in combination, fail to disclose or suggest the claimed invention, and thus it is submitted that the invention of claim 1 is both novel and inventive. Similar comments apply to claims 5 and 9, which thus are also both novel and inventive.

Each of the objections raised by the examiner has been addressed and favourable reconsideration of the application is requested. If the examiner has further objections then it would be preferred if the proceedings could be continued in writing. Nevertheless, as a precaution, oral proceedings are requested in lieu of any adverse decision.

Amendments made in the course of this response are made without prejudice to the later reinstatement or dividing out of any subject matter deleted by way of the amendments and such subject matter should not be considered to have been abandoned.

Yours faithfully

Dr Tim Hargreaves
European Patent Attorney
for MARKS & CLERK LLP

Encs. Amended set of claims
Marked-up version of amended set of claims
Amended page 1
Marked-up version of amended page 1

A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE

BACKGROUND OF THE INVENTION

Field of Invention

The present invention relates generally to the field of load distribution. More specifically, the present invention is related to a system and method for dividing and synchronizing a processing task across multiple processing elements/processors in hardware.

Discussion of Related Art

In the prior art, the processing load (of a processing element) to determine what command to issue is relatively high. The processing load to determine what command to issue can be partially or fully offloaded to a multiplicity of other processing elements (e.g. processors, processor cores, or custom processing circuitry). However, this distribution of load causes commands to be determined from multiple processing elements. It can become a challenge to ensure the module command queues (FIFOs) are not overfilled, thus synchronization is required amongst the multiplicity of processing elements. In the prior art, such synchronization is performed using software techniques, such as semaphores and mutexes to a shared available space count variable in memory. However, this takes additional processing time, making this process non-optimal. To further compound the problem, there may be a need to keep the time from command issue to execution minimized, which tends to keep the command queue shallow.

US 8,051,227 describes programmable queue structures for multiprocessors. US 2002/069245 describes a network-attached disk system.

Embodiments of the present invention are an improvement over prior art systems and methods.

SUMMARY OF THE INVENTION

In one embodiment, the present invention provides a system for dividing and synchronizing a processing task across a plurality of processing elements comprising: an input queue implemented in hardware; an output queue implemented in hardware; a first processing element having access to the input queue and the output queue; at least one second processing element in communication with the first processing element; a reservation register implemented in hardware storing a value indicative of available space in a command queue, the reservation register accessible by both the first processing element and the at least second processing element; computer storage storing instructions, which when executed by the at

A SYSTEM AND METHOD FOR DIVIDING AND SYNCHRONIZING A PROCESSING TASK ACROSS MULTIPLE PROCESSING ELEMENTS/PROCESSORS IN HARDWARE

BACKGROUND OF THE INVENTION

Field of Invention

The present invention relates generally to the field of load distribution. More specifically, the present invention is related to a system and method for dividing and synchronizing a processing task across multiple processing elements/processors in hardware.

Discussion of Related Art

In the prior art, the processing load (of a processing element) to determine what command to issue is relatively high. The processing load to determine what command to issue can be partially or fully offloaded to a multiplicity of other processing elements (e.g. processors, processor cores, or custom processing circuitry). However, this distribution of load causes commands to be determined from multiple processing elements. It can become a challenge to ensure the module command queues (FIFOs) are not overfilled, thus synchronization is required amongst the multiplicity of processing elements. In the prior art, such synchronization is performed using software techniques, such as semaphores and mutexes to a shared available space count variable in memory. However, this takes additional processing time, making this process non-optimal. To further compound the problem, there may be a need to keep the time from command issue to execution minimized, which tends to keep the command queue shallow.

US 8,051,227 describes programmable queue structures for multiprocessors. US 2002/069245 describes a network-attached disk system.

Embodiments of the present invention are an improvement over prior art systems and methods.

SUMMARY OF THE INVENTION

In one embodiment, the present invention provides a system for dividing and synchronizing a processing task across a plurality of processing elements comprising: an input queue implemented in hardware; an output queue implemented in hardware; a first processing element having access to the input queue and the output queue; at least one second processing element in communication with the first processing element; a reservation register implemented in hardware storing a value indicative of available space in a command queue, the reservation register accessible by both the first processing element and the at least second processing element; computer storage storing instructions, which when executed by the at

CLAIMS

1. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

an input queue (308) implemented in hardware;

an output queue (312) implemented in hardware;

a first processing element (312) having access to said input queue (308) and said output queue (312);

at least one second processing element (304) in communication with said first processing element (302);

a reservation register (310) implemented in hardware storing a value indicative of available space in ~~a command~~ said input queue (308), said reservation register (310) accessible by both said first processing element (302) and said at least second processing element (304);

computer storage storing instructions, which when executed by said at least one second processing element (304):

accesses said reservation register (310) and reads said stored value;

determines when said read value indicates available space in said input queue (308) for said first processing element (302) to issue a command;

~~upon determining when said read value indicates available space in said input queue (308), notifies said first processing element (302) to issue said command to said input queue (308); and~~

wherein said first processing element (302) receives notification from said at least second processing element (304) regarding issuing the command, issues said command to said input queue (308), and receives a response corresponding to said command from said output queue (312);

~~wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element (304); and~~

~~wherein at least one third processing element (330) executes said command and notifies said output queue (312) to issue said response.~~

2. The system of claim 1, wherein said ~~command-input~~ queue (308) is a FIFO buffer.

3. The system of claim 1, wherein said system is part of a storage area network (SAN) controller.

4. The system of claim 1, wherein said system is part of a network attached storage (NAS) controller.

~~5. The system of claim 1, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element.~~

~~6. The system of claim 1, wherein at least one third processing element executes said command and notifies said output queue to issue said response.~~

75. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

an input queue (408) implemented in hardware (414);

an output queue (412) implemented in hardware (414);

a first processing element (402) having access to said input queue (408) and said output queue (412);

at least one second processing element (404) in communication with said input queue (408);

a reservation register (410) implemented in hardware (414) storing a value indicative of available space in ~~a command~~ said input queue (408), said reservation register (410) accessible by both said first processing element (402) and said at least second processing element (404);

computer storage storing instructions, which when executed by said at least one second processing element (404):

accesses said reservation register (410) and reads said stored value;

determines when said read value indicates available space in said input

queue (408) for said first processing element (402) to issue a command;

~~upon determining when said read value indicates available space in said input queue (408), issue said command to said input queue (408); and~~

wherein said first processing element (402) receives a response corresponding to said command from said output queue (412);-

wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element (404); and

wherein at least one third processing element (430) executes said command and notifies said output queue (412) to issue said response.

86. The system of claim 75, wherein said ~~command-input~~ queue (408) is a FIFO buffer.

97. The system of claim 75, wherein said system is part of a storage area network (SAN) controller.

408. The system of claim 75, wherein said system is part of a network attached storage (NAS) controller.

11. The system of claim 7, wherein ~~at least one of a) or b)~~:

~~a) said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element;~~

~~b) 12. The system of claim 7, wherein at least one third processing element executes said command and notifies said output queue to issue said response.~~

129. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

an input queue (508) implemented in hardware (514);

an output queue (512) implemented in hardware (514);

a first processing element (502) having access to said input queue (508) and said output queue (512);

at least one second processing element (504) in communication with said input queue (508) and said output queue (512);

a reservation register (510) implemented in hardware (514) storing a value indicative of available space in ~~a command~~ said input queue (508), said reservation register (510) accessible by both said first processing element (502) and said at least second processing element (504);

computer storage storing instructions, which when executed by said at least one second processing element (504):

accesses said reservation register (510) and reads said stored value;

determines when said read value indicates available space in said input queue (508) for said first processing element (502) to issue a command;

upon determining when said read value indicates available space in said input queue (508), issue said command to said input queue (508); and

receives a response corresponding to said command from said output queue (512);-

wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element (504); and

wherein at least one third processing element (530) executes said command and notifies said output queue (512) to issue said response.

1310. The system of claim 129, wherein said command input queue (508) is a FIFO buffer.

1411. The system of claim 129, wherein said system is either part of a storage area network (SAN) controller.

1512. The system of claim 129, wherein ~~at least one of a), b) or c):~~

~~a) said system is part of a network attached storage (NAS) controller;-~~

~~b) -~~

17. The system of claim 13, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element;-

~~c) -~~

18. The system of claim 13, wherein at least one third processing element executes said command and notifies said output queue to issue said response.

Formatted: Indent: Left: 0 cm

Formatted: Indent: First line: 0 cm

Formatted: Justified, None, Don't keep with next, Tab stops: 0.63 cm, Left

CLAIMS

1. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

5 an input queue (308) implemented in hardware;
 an output queue (312) implemented in hardware;
 a first processing element (312) having access to said input queue (308) and said output queue (312);

10 at least one second processing element (304) in communication with said first processing element (302);

 a reservation register (310) implemented in hardware storing a value indicative of available space in said input queue (308), said reservation register (310) accessible by both said first processing element (302) and said at least second processing element (304);

15 computer storage storing instructions, which when executed by said at least one second processing element (304):

 accesses said reservation register (310) and reads said stored value;

 determines when said read value indicates available space in said input queue (308) for said first processing element (302) to issue a command;

20 upon determining when said read value indicates available space in said input queue (308), notifies said first processing element (302) to issue said command to said input queue (308);

25 wherein said first processing element (302) receives notification from said at least second processing element (304) regarding issuing the command, issues said command to said input queue (308), and receives a response corresponding to said command from said output queue (312);

 wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element (304); and

 wherein at least one third processing element (330) executes said command and notifies said output queue (312) to issue said response.

30 2. The system of claim 1, wherein said input queue (308) is a FIFO buffer.

 3. The system of claim 1, wherein said system is part of a storage area network (SAN) controller.

4. The system of claim 1, wherein said system is part of a network attached storage (NAS) controller.

5

5. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

an input queue (408) implemented in hardware (414);

an output queue (412) implemented in hardware (414);

10 a first processing element (402) having access to said input queue (408) and said output queue (412);

at least one second processing element (404) in communication with said input queue (408);

15 a reservation register (410) implemented in hardware (414) storing a value indicative of available space in said input queue (408), said reservation register (410) accessible by both said first processing element (402) and said at least second processing element (404);

computer storage storing instructions, which when executed by said at least one second processing element (404):

accesses said reservation register (410) and reads said stored value;

20 determines when said read value indicates available space in said input queue (408) for said first processing element (402) to issue a command;

upon determining when said read value indicates available space in said input queue (408), issue said command to said input queue (408);

25 wherein said first processing element (402) receives a response corresponding to said command from said output queue (412);

wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element (404); and

wherein at least one third processing element (430) executes said command and notifies said output queue (412) to issue said response.

30

6. The system of claim 5, wherein said input queue (408) is a FIFO buffer.

7. The system of claim 5, wherein said system is part of a storage area network (SAN) controller.

8. The system of claim 5, wherein said system is part of a network attached storage (NAS) controller.

5

9. A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

an input queue (508) implemented in hardware (514);

an output queue (512) implemented in hardware (514);

10 a first processing element (502) having access to said input queue (508) and said output queue (512);

at least one second processing element (504) in communication with said input queue (508) and said output queue (512);

15 a reservation register (510) implemented in hardware (514) storing a value indicative of available space in said input queue (508), said reservation register (510) accessible by both said first processing element (502) and said at least second processing element (504);

computer storage storing instructions, which when executed by said at least one second processing element (504):

accesses said reservation register (510) and reads said stored value;

20 determines when said read value indicates available space in said input queue (508) for said first processing element (502) to issue a command;

upon determining when said read value indicates available space in said input queue (508), issue said command to said input queue (508);

25 receives a response corresponding to said command from said output queue (512);

wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element (504); and

wherein at least one third processing element (530) executes said command and notifies said output queue (512) to issue said response.

30

10. The system of claim 9, wherein said input queue (508) is a FIFO buffer.

11. The system of claim 9, wherein said system is part of a storage area network (SAN) controller.

5 12. The system of claim 9, wherein said system is part of a network attached storage (NAS) controller;



Acknowledgement of receipt

We hereby acknowledge receipt of the following subsequently filed document(s):

Submission number	6260056
Application number	EP14867963.2
Date of receipt	23 April 2018
Receiving Office	European Patent Office, The Hague
Your reference	PE957775EP
Applicant	All applicants as on file
Documents submitted	package-data.xml epf1038.pdf (1 p.) CLMS-1.pdfPE957775EP - Amended claims (clean).pdf (4 p.) DESC-HWA-1.pdfPE957775EP - Amended page 1 (annotated).pdf (1 p.) ep-sfd-request.xml EPLETT-1.pdfResponse to European Search Opinion - PE957775EP.pdf (3 p.) CLMS-HWA-1.pdfPE957775EP - Amended claims (annotated).pdf (5 p.) DESC-1.pdfPE957775EP - Amended page 1 (clean).pdf (1 p.)
Submitted by	CN=Timothy Hargreaves 29477
Method of submission	Online
Date and time receipt generated	23 April 2018, 16:34 (CEST)
Message Digest	D7:D7:24:1B:B8:37:F7:DA:F3:80:45:C3:2F:61:84:AC:75:1B:44:B2

Correction by the EPO of errors in debit instructions filed by eOLF

Errors in debit instructions filed by eOLF that are caused by the editing of Form 1038E entries or the continued use of outdated software (all forms) may be corrected automatically by the EPO, leaving the payment date unchanged (see decision T 152/82,

OJ EPO 1984, 301 and point 6.3 ff ADA, Supplement to OJ EPO 10/2007).

/European Patent Office/



Letter accompanying subsequently filed items

Representative:

Dr Timothy Edward HARGREAVES
Marks & Clerk LLP
Atholl Exchange
6 Canning Street
Edinburgh EH3 8EG
United Kingdom

Phone: 0131 221 7000

Fax: 0131 221 7010

E-mail: edinburgh@marks-clerk.com

80298 Munich

Germany

Tel. +49(0)89 2399-0 | Fax -4465

P.O. Box 5818

2280 HV Rijswijk

Netherlands

Tel. +31(0)70 340-2040 | Fax -3016

10958 Berlin

Germany

Tel. +49(0)30 25901-0 | Fax -840

The document(s) listed below is (are) subsequently filed documents pertaining to the following application:

Application number

14867963.2

Applicant's or representative's reference

TH/PE957775EP

	Description of document	Original file name	Assigned file name
--	-------------------------	--------------------	--------------------

	Fees	Factor applied	Fee schedule	Amount to be paid
15-1	122 Fee for further processing (non fee related cases)	2	255.00	510.00
	Total:		EUR	510.00

	Payment	
1	Method of payment	Debit from deposit account
	Currency:	EUR
	The European Patent Office is hereby authorised, to debit from the deposit account with the EPO any fees and costs indicated on the fees page.	
	Deposit account number:	28050604
	Account holder:	Marks & Clerk LLP
2	Refund/Reimbursement	
	Reimbursement (if any) to be made to EPO deposit account:	28050604
	Account holder:	Marks & Clerk LLP

Signatures

Place: **Glasgow, UK**
Date: **24 April 2018**
Signed by: **Timothy Hargreaves 29477**
Representative name: **Timothy Edward HARGREAVES**
Capacity: **(Representative)**

TH/PE957775EP



Acknowledgement of receipt

We hereby acknowledge receipt of the following subsequently filed document(s):

Submission number	6262817	
Application number	EP14867963.2	
Date of receipt	24 April 2018	
Receiving Office	European Patent Office, The Hague	
Your reference	TH/PE957775EP	
Applicant	All applicants as on file	
Documents submitted	package-data.xml epf1038.pdf (1 p.)	ep-sfd-request.xml
Submitted by	CN=Timothy Hargreaves 29477	
Method of submission	Online	
Date and time receipt generated	24 April 2018, 13:27 (CEST)	
Message Digest	44:61:03:C3:D3:75:FC:9B:3A:A1:53:D5:6A:3E:A1:92:B3:E3:59:E1	

Correction by the EPO of errors in debit instructions filed by eOLF

Errors in debit instructions filed by eOLF that are caused by the editing of Form 1038E entries or the continued use of outdated software (all forms) may be corrected automatically by the EPO, leaving the payment date unchanged (see decision T 152/82, OJ EPO 1984, 301 and point 6.3 ff ADA, Supplement to OJ EPO 10/2007).

/European Patent Office/



European Patent Office
80298 MUNICH
GERMANY

Questions about this communication ?

Contact Customer Services at www.epo.org/contact



Hargreaves, Timothy Edward
Marks & Clerk LLP
Atholl Exchange
6 Canning Street
Edinburgh EH3 8EG
ROYAUME UNI

Date
09.05.18

Reference PE957775EP	Application No./Patent No. 14867963.2 - 1221 / 3077909
Applicant/Proprietor Concurrent Ventures LLC	

Decision on the request for further processing under Rule 135(3) EPC

The request for further processing received on 24.04.18 has been granted (Art. 121(2) EPC).

- ☒ The legal consequence notified in the communication dated 16.02.18 that the application was deemed to be withdrawn shall not ensue.
- ☐ The legal consequence shall not ensue.
- ☐ The refusal of the application dated shall not ensue.
- ☐ The legal consequence notified in the communication dated that the particular loss of rights occurred shall not ensue.
- ☐ The time limit set in the communication dated is deemed to have been met.

The procedure shall be continued/the particular loss of rights shall not ensue (Art. 121(3) EPC).

Important information in case of a PACE request

If a PACE request has been validly filed for the application, the applicant is herewith informed that the application is removed from the PACE programme. A second PACE request for that application during the same stage of the procedure will not be processed (see OJ EPO 2015, A93, point 4).

For the Examining Division



Registered letter

EPO Form 2010 02.16 (NFS) (02/05/18)

page 1 of 1

Marks&Clerk LLP

Patent and Trade Mark Attorneys



Fax No:	00498923994465
To:	
Attn:	
From:	Edinburgh
Subject:	Letter to EPO - Change of address
Date:	10 May 2018 at 15:46
No. of pages:	4

FAX COVER SHEET

Atholl Exchange, 6 Canning Street, Edinburgh, EH3 8EG
Tel: +44 (0) 131 221 7000 Fax: +44 (0) 131 221 7010
Email: edinburgh@marks-clerk.com <http://www.marks-clerk.com>

Marks & Clerk LLP is a limited liability partnership and is registered in England and Wales with registered number OC343273. A list of members' names is open to inspection at our registered office, 90 Long Acre, London WC2E 9RA

Received at the EPO on May 10, 2018 16:48:40. Page 1 of 4

Duration: 05.10.2018 04:46:53 PM - 05.10.2018 04:48:40 PM. This page 1 of 4 was completed at 05.10.2018 04:47:32 PM

Advanced Micro Devices, Inc., Pensando Systems, Inc. - Ex. 1004, Page 000148

Dear Sirs,

Please find our letter attached.

Kind regards,

Anna Lechtanska | Formalities Team Leader
Certified CIPA Administrator and CITMA Paralegal
for **Marks & Clerk LLP**

T +44 131 221 7000 | F +44 131 221 7010
alechtanska@marks-clerk.com | Atholl Exchange, 6 Canning Street, Edinburgh EH3 8EG, UK

www.marks-clerk.com | [LinkedIn](#) | [Twitter](#)

 cid:image003.png@01D3CB53.E55A2290

Marks&Clerk



Marks & Clerk LLP

Atholl Exchange, 6 Canning Street, Edinburgh EH3 8EG, UK
T +44 131 221 7000 | F +44 131 221 7010
edinburgh@marks-clerk.com | www.marks-clerk.com

European Patent Office
80298
Munich
Germany

Date: 10 May 2018

By Fax +0049 89 23994465

Dear Sirs

We have changed our office address to:

**MARKS & CLERK LLP
40 Torphichen Street
Edinburgh
EH3 8JB**

Please update the address on your records.

Yours faithfully

Dr Paul Chapman
Office Managing Partner
for MARKS & CLERK LLP
Direct e-mail: pchapman@marks-clerk.com

This letter is sent on behalf of Marks & Clerk LLP, a limited liability partnership registered in England and Wales with registered number OC343273. The firm is regulated by the Intellectual Property Regulation Board (IPREG). A list of members' names is open to inspection at our registered office, 30 Long Acre, London WC2E 8PA, UK. Marks & Clerk is a trading name of Marks & Clerk LLP and other entities within the Marks & Clerk network of associated operating firms, each of which is a separately constituted entity. Marks & Clerk offices are located in Beijing and Hong Kong (China); Kuala Lumpur (Malaysia); Singapore; Ottawa (Canada); Paris and Sophia Antipolis (France); Luxembourg; Aberdeen, Birmingham, Cambridge, Edinburgh, Glasgow, London, Manchester and Oxford (UK).

53187690-1-ALECHTANSKA

Received at the EPO on May 10, 2018 16:48:40. Page 3 of 4

Duration: 05.10.2018 04:46:53 PM - 05.10.2018 04:48:40 PM. This page 3 of 4 was completed at 05.10.2018 04:48:25 PM

Advanced Micro Devices, Inc., Pensando Systems, Inc. - Ex. 1004, Page 000150

SCOTLAND PROSECUTION
FIRM 5th YEAR 2017 & 2018



European Patent Office
80298 MUNICH
GERMANY

Questions about this communication ?

Contact Customer Services at www.epo.org/contact



Hargreaves, Timothy Edward
Marks & Clerk LLP
40 Torphichen Street
Edinburgh EH3 8JB
ROYAUME UNI

Date

05.02.20

Reference PE957775EP	Application No./Patent No. 14867963.2 - 1203 / 3077909
Applicant/Proprietor Concurrent Ventures LLC	

**Notice drawing attention to Rule 51(2) EPC, Article 2 No. 5 of the Rules relating to Fees,
- Payment of the renewal fee plus additional fee -**

The renewal fee for the 06. year fell due on 31.12.19 unless this date falls within the period covered by an interruption of the proceedings in accordance with Rule 142(1) EPC, or a request for re-establishment of rights is pending (Art. 122, R. 51(4) EPC).

The current rate of the renewal fee amounts to **EUR 1050,00** (see current Schedule of fees and costs).

The renewal fee was not paid by the due date.

The renewal fee may still be validly paid **up to the last day of the sixth calendar month** following the due date, provided that the additional fee (50% of the renewal fee) is paid at the same time, see OJ EPO 2008, 5.

Within the above period, which cannot be extended, the following fees are to be paid:

Renewal fee for the 06. year:	EUR	1050,00
Additional fee:	EUR	525,00

TOTAL AMOUNT	EUR	1.575,00

If the renewal fee and the additional fee are not paid in due time, the European patent application shall be deemed to be withdrawn (Art. 86(1) EPC).

Note to users of the automatic debiting procedure

The basic time limit for payment of the above renewal fee had already expired when the automatic debit order was received. The renewal fee and the surcharge will be debited automatically on the last day of the six-month period.

Making payments

For payments made via deposit account, please note that as from 1 December 2017 debit orders will only be carried out if filed in an electronically processable format (xml), using an accepted means of filing as laid down in the Arrangements for deposit accounts (ADA), published in the Supplementary publication in the Official Journal.

All relevant information related to the modes of payment of fees to the EPO can be retrieved from the EPO website at **"Making Payments"**.

Information concerning fee amounts

Procedural fees are usually adjusted every two years, on even years, with effect from 1 April. Therefore, before making a payment, parties should verify the amounts actually due on the date of payment using the applicable version of the Schedule of fees and expenses, published as a Supplement to the Official Journal of the EPO, available on the EPO website (www.epo.org) at www.epo.org/schedule-of-fees. The "Schedule of fees" table allows the viewing, downloading and searching of individual fee amounts, both current and previous.

Important information in case of a PACE request

If, for an application being processed under the PACE programme the payment of the renewal fee has not been received by the due date stipulated in Rule 51(1) EPC, the accelerated prosecution of the application is suspended until the payment of the renewal fee with additional fee has been received (see OJ EPO 2015, A93, point 5).

For the Examining Division



Letter accompanying subsequently filed items

Representative:

Timothy Edward HARGREAVES
Marks & Clerk LLP
40 Torphichen Street
Edinburgh EH3 8JB
United Kingdom

Phone: +44-0131-221-7000

Fax: +44-0131-221-7010

E-mail: edinburgh@marks-clerk.com

80298 Munich
Germany
Tel. +49(0)89 2399-0 | Fax -4465

P.O. Box 5818
NL-2280 HV Rijswijk
Netherlands
Tel. +31(0)70 340-2040 | Fax -3016

10958 Berlin
Germany
Tel. +49(0)30 25901-0 | Fax -840

The document(s) listed below is (are) subsequently filed documents pertaining to the following application:

Application number and/or EP publication number	EP14867963.2
Reference	PE957775EP
Procedural phase	All procedures
Name of represented party	Concurrent Ventures, LLC

	Fees	Factor applied	Fee schedule	Amount to be paid
15-1	036 Renewal fee for the 6th year	1	1 090.00	1 090.00
15-2	096 Surcharge for renewal fee for 6th year	1	545.00	545.00
	Total:		EUR	1 635.00

	Payment	
1	Method of payment	Debit from deposit account
	Currency: EUR The European Patent Office is hereby authorised, to debit from the deposit account with the EPO any fees and costs indicated on the fees page. Deposit account number: 28050604 Account holder: Marks & Clerk LLP	
2	Refund/Reimbursement	
	Reimbursement (if any) to be made to EPO deposit account: 28050604 Account holder: Marks & Clerk LLP	

Signature 1

Place: **Edinburgh, UK**
Date: **08 June 2020**
Signed by: **/147280/**
Capacity: **Representative 1**

Smart card certificate 1

Common name:	Timothy Hargreaves 29477
EPO ID:	29477
Issued by:	European Patent Office CA G2



Acknowledgement of receipt

We hereby acknowledge receipt of the following subsequently filed document(s):

Submission number	8703513	
Application number	EP14867963.2	
Date of receipt	08 June 2020	
Filing Office	European Patent Office, The Hague	
Procedural phase	All procedures	
Your reference	PE957775EP	
Documents submitted	package-data.xml ep-cms-sfd-request.pdf (2 p.)	ep-cms-sfd-request.xml
Submitted by	CN=secure.epoline.org	
Method of submission	Online	
Date and time receipt generated	08 June 2020, 15:43 (CEST)	
Message Digest	07:F8:1B:C2:B4:9F:1D:E6:7D:D5:86:AD:C9:20:91:7C:A4:49:20:F9	

/European Patent Office/



European Patent Office
80298 MUNICH
GERMANY

Questions about this communication ?

Contact Customer Services at www.epo.org/contact



Hargreaves, Timothy Edward
Marks & Clerk LLP
40 Torphichen Street
Edinburgh EH3 8JB
ROYAUME UNI

Date

15.02.21

Reference PE957775EP	Application No./Patent No. 14867963.2 - 1203 / 3077909
Applicant/Proprietor Concurrent Ventures, LLC	

**Notice drawing attention to Rule 51(2) EPC, Article 2 No. 5 of the Rules relating to Fees,
- Payment of the renewal fee plus additional fee -**

The renewal fee for the 07. year fell due on 31.12.20 unless this date falls within the period covered by an interruption of the proceedings in accordance with Rule 142(1) EPC, or a request for re-establishment of rights is pending (Art. 122, R. 51(4) EPC).

The current rate of the renewal fee amounts to **EUR 1210,00** (see current Schedule of fees and costs).

The renewal fee was not paid by the due date.

The renewal fee may still be validly paid **up to the last day of the sixth calendar month** following the due date, provided that the additional fee (**50%** of the renewal fee) is paid at the same time, see OJ EPO 2008, 5.

Within the above period, which cannot be extended, the following fees are to be paid:

Renewal fee for the 07. year:	EUR	1210,00
Additional fee:	EUR	605,00

TOTAL AMOUNT	EUR	1.815,00

If the renewal fee and the additional fee are not paid in due time, the European patent application shall be deemed to be withdrawn (Art. 86(1) EPC).

Note to users of the automatic debiting procedure

The basic time limit for payment of the above renewal fee had already expired when the automatic debit order was received. The renewal fee and the surcharge will be debited automatically on the last day of the six-month period.

Making payments

For payments made via deposit account, please note that as from 1 December 2017 debit orders will only be carried out if filed in an electronically processable format (xml), using an accepted means of filing as laid down in the Arrangements for deposit accounts (ADA), published in the Supplementary publication in the Official Journal.

All relevant information related to the modes of payment of fees to the EPO can be retrieved from the EPO website at **"Making Payments"**.

Information concerning fee amounts

Procedural fees are usually adjusted every two years, on even years, with effect from 1 April. Therefore, before making a payment, parties should verify the amounts actually due on the date of payment using the applicable version of the Schedule of fees and expenses, published as a Supplement to the Official Journal of the EPO, available on the EPO website (www.epo.org) at www.epo.org/schedule-of-fees. The "Schedule of fees" table allows the viewing, downloading and searching of individual fee amounts, both current and previous.

Important information in case of a PACE request

If, for an application being processed under the PACE programme the payment of the renewal fee has not been received by the due date stipulated in Rule 51(1) EPC, the accelerated prosecution of the application is suspended until the payment of the renewal fee with additional fee has been received (see OJ EPO 2015, A93, point 5).

For the Examining Division



European Patent Office
80298 MUNICH
GERMANY



Hargreaves, Timothy Edward
Marks & Clerk LLP
40 Torphichen Street
Edinburgh EH3 8JB
ROYAUME UNI

Questions about this communication ?

Contact Customer Services at www.epo.org/contact

Formalities officer

Alevizou, Martina

Date
21-07-2021

Reference PE957775EP	Application No./Patent No. 14867963.2 - 1203 / 3077909
Applicant/Proprietor Concurrent Ventures, LLC	

Noting of loss of rights pursuant to Rule 112(1) EPC

The European Patent application is deemed to be withdrawn under Article 86(1) EPC.

The renewal fee for the 07. year and the additional fee have not been paid in due time / not been paid in full in due time.

Means of redress

Request for a decision (R. 112(2) EPC)

If the applicant considers that the finding of the European Patent Office is inaccurate, he may, within a (non-extendable) period of **two months** after notification of this communication, apply in writing for a decision on the matter. The application can only lead to the finding being reversed if this does not actually correspond to the factual or legal situation.

Re-establishment of rights (Art. 122 EPC)

The applicant who, in spite of all due care required by the circumstances having been taken, was unable to observe the time limit, shall have his rights re-established upon request, provided that the time limits and other requirements of Rule 136(1) and (2) EPC are met.

Request under Article 7(3) and (4) Rules relating to Fees

The fee is considered to have been paid in due time if, within a period of two months from notification of this communication and in accordance with the requirements under Article 7(3) and (4) Rules relating to Fees, evidence is provided to the EPO that the payment was effected in an EPC Contracting State within the period in which the payment should have been made.

For the Examining Division



Registered letter

EPO Form 2524 04.20 (13/07/21)

ADWI 9

page 1 of 1



European Patent Office
80298 MUNICH
GERMANY

Questions about this communication ?

Contact Customer Services at www.epo.org/contact



Hargreaves, Timothy Edward
Marks & Clerk LLP
40 Torphichen Street
Edinburgh EH3 8JB
ROYAUME UNI

Date

27.10.21

Reference PE957775EP	Application No./Patent No. 14867963.2 - 1203 / 3077909
Applicant/Proprietor Concurrent Ventures, LLC	

Refund of fees

The following fee has been paid in respect of application No. 14867963.2:

Fee	Reference	Voucher No.	Date	Currency	Amount
Examination fee	006	00953461	23.06.16	EUR	1 635,00

The fee was paid by Marks & Clerk LLP.

Amount refundable:	Reference	Currency	Amount	Voucher No.
	006	EUR	1.635,00	10183870

Refund order

1. Reason for refund: Application withdrawn, refused or deemed to be withdrawn before Examining Division has assumed responsibility (100 % of the examination fee refunded)

2. In accordance with the information on file, the refund:

(x) will be credited to EPO deposit account number 28050604

The authorising officer
Avilés Parrales

