THE ART OF ELECTRONICS

PAUL HOROWITZ
WINFIELD HILL

SECOND EDITION

Advanced Micro Devices, Inc., Pensando Systems, Inc. - Ex. 1019, Page 000001
IPR2025-00478 (Advanced Micro Devices, Inc., Pensando Systems, Inc. v. Concurrent Ventures, LLC, XtreamEdge, Inc.)

THE ART OF ELECTRONICS

Second Edition

Paul Horowitz HARVARD UNIVERSITY

Winfield Hill ROWLAND INSTITUTE FOR SCIENCE, CAMBRIDGE, MASSACHUSETTS

CAMBRIDGE
UNIVERSITY PRESS

Advanced Micro Devices, Inc., Pensando Systems, Inc. - Ex. 1019, Page 000002

Published by the Press Syndicate of the University of Cambridge
The Pitt Building, Trumpington Street, Cambridge CB2 1RP
40 West 20th Street, New York, NY 10011-4211, USA
10 Stamford Road, Oakleigh, Melbourne 3166, Australia

© Cambridge University Press 1980, 1989

First published 1980
Second edition 1989
Reprinted 1990 (twice), 1991, 1993, 1994 (twice), 1995

Printed in the United States of America

Library of Congress Cataloging-in-Publication Data is available.

A catalogue record for this book is available from the British Library.

ISBN 0-521-37095-7 hardback

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figure the abbreviation MSB is used to mean "most significant bit," and LSB means "least significant bit"; the curved arrows are used to indicate what causes what, to aid in understanding.

As you will see in Section 8.25, the counter is such a useful function that many versions are available integrated onto single chips, including 4-bit, BCD, and multidigit counting formats. By cascading several such counters and displaying the count on a numeric display device (e.g., an LED digital display) you can easily construct an event counter. If the input pulse train to such a counter is gated for exactly 1 second, you've got a frequency counter, which displays frequency (cycles per second) by actually counting the number of cycles in a second. Section 15.10 shows diagrams of this simple and highly useful scheme. In fact, single-chip frequency counters are available, complete with oscillator, counter, control, and display circuitry; see Figure 8.71 for an example.

In practice, the simple scheme of cascading counters by connecting each Q output to the next clock input has some interesting problems related to the cascaded delays as the signal "ripples" down through the chain of flip-flops, and a "synchronous" scheme (in which all clock inputs see the same clocking signal) is usually better. Let's look into this question of synchronous clocked systems.

8.18 Combining memory and gates: sequential logic

Having explored the properties of flip-flops, let's see what can be done when they are combined with the combinational (gate) logic we discussed earlier. Circuits made with gates and flip-flops constitute the most general form of digital logic.

Synchronously clocked systems

As we hinted in the last section, sequential logic circuits in which there is a common source of clock pulses driving all flip-flops have some very desirable properties. In such a *synchronous system* all action takes place just after each clocking pulse, based on the levels present just before each clock pulse. Figure 8.57 shows the general scheme.

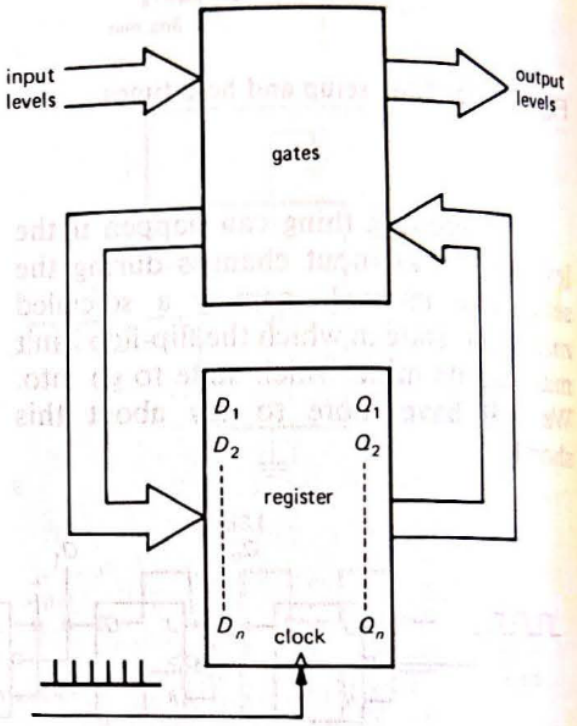


Figure 8.57. The classical sequential circuit: memory registers plus combinational logic. This scheme can be easily implemented with single-chip "registered PALs" (Section 8.27).

The flip-flops have all been combined into a single *register*, which is nothing more than a set of type D flip-flops with their clock inputs all tied together and their individual D inputs and Q outputs brought out; i.e., each clock pulse causes the levels present at the D inputs to be transferred to the respective Q outputs. The box full of gates looks at both the Q outputs and whatever input levels are applied to the circuit and generates a new set of D inputs and logic outputs. This simple-looking scheme is extremely powerful. Let's look at an example.

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