

DIGITAL DESIGN

PRINCIPLES & PRACTICES
SECOND EDITION

JOHN F. WAKERLY



Digital Design Principles and Practices

Second Edition

JOHN F. WAKERLY

Alantec Corporation

Stanford University



PRENTICE HALL, Englewood Cliffs, New Jersey 07632

Library of Congress Cataloging-in-Publication Data

Wakerly, John F.

Digital design: principles and practices. / John F. Wakerly. --2nd ed.

p. cm. -- (Prentice Hall series in computer engineering)

Includes bibliographical references and index

ISBN 0-13-211459-3

I. Digital integrated circuits--Design and construction.

1. Title. II. Series

TK7874.65.W34 1994

621.39'5--dc20

93-43333

CIP

Acquisitions editor: **Don Fowley**

Production editor: **Irwin Zucker**

Copy editor: **Brenda Melissaratos**

Production coordinator: **David Dickey**

Supplements editor: **Alice Dworkin**

Editorial assistant: **Jennifer Klein**

Cover design: **Glen Biren/Topdesk Pre-Press, Inc.**

Cover illustration: **Photo of circuit board, Bruce Forster/Allstock**

Background texture, Allstock



© 1994, 1990 by Prentice-Hall, Inc.

A Paramount Communications Company

Englewood Cliffs, New Jersey 07632

The author and publisher of this book have used their best efforts in preparing this book. These efforts include the development, research, and testing of the theories and programs to determine their effectiveness. The author and publisher make no warranty of any kind, expressed or implied, with regard to these programs or the documentation contained in this book. The author and publisher shall not be liable in any event for incidental or consequential damages in connection with, or arising out of, the furnishing, performance, or use of these programs.

All rights reserved. No part of this book may be reproduced, in any form or by any means, without permission in writing from the publisher.

TRADEMARK INFORMATION: PostScript is a trademark of Adobe Systems Incorporated. Macintosh is a trademark of Apple Computer, Inc. TRI-STATE is a trademark of National Semiconductor Corporation. PAL is a trademark of Advanced Micro Devices, Inc. ABEL is a trademark of Data I/O Corporation.

Printed in the United States of America

10 9 8 7 6 5 4 3 2 1

ISBN 0-13-211459-3

Prentice-Hall International (UK) Limited, *London*

Prentice-Hall of Australia Pty. Limited, *Sydney*

Prentice-Hall Canada Inc., *Toronto*

Prentice-Hall Hispanoamericana, S.A., *Mexico*

Prentice-Hall of India Private Limited, *New Delhi*

Prentice-Hall of Japan, Inc., *Tokyo*

Simon & Schuster Asia Pte. Ltd., *Singapore*

Editora Prentice-Hall do Brasil, Ltda., *Rio de Janeiro*

CONTENTS

FOREWORD xv

PREFACE xvii

1 INTRODUCTION 1

- 1.1 About Digital Design 2
- 1.2 Analog versus Digital 3
- 1.3 Digital Devices 6
- 1.4 Electronic Aspects of Digital Design 7
- 1.5 Software Aspects of Digital Design 8
- 1.6 Integrated Circuits 11
- 1.7 Application-Specific ICs 15
- 1.8 Printed-Circuit Boards 17
- 1.9 The Name of the Game 19
- 1.10 Going Forward 20
- Drill Problems 20

2 NUMBER SYSTEMS AND CODES 21

- 2.1 Positional Number Systems 22
- 2.2 Octal and Hexadecimal Numbers 23
- 2.3 General Positional Number System Conversions 25
- 2.4 Addition and Subtraction of Nondecimal Numbers 27
- 2.5 Representation of Negative Numbers 30
 - 2.5.1 Signed-Magnitude Representation
 - 2.5.2 Complement Number Systems
 - 2.5.3 Radix-Complement Representation
 - 2.5.4 Two's-Complement Representation
 - 2.5.5 Diminished Radix-Complement Representation
 - 2.5.6 Ones'-Complement Representation 2.5.7 Excess Representations
- 2.6 Two's-Complement Addition and Subtraction 35
 - 2.6.1 Addition Rules 2.6.2 A Graphical View 2.6.3 Overflow
 - 2.6.4 Subtraction Rules
 - 2.6.5 Two's-Complement and Unsigned Binary Numbers

2.7	Ones'-Complement Addition and Subtraction	40
2.8	Binary Multiplication	41
2.9	Binary Division	43
2.10	Binary Codes for Decimal Numbers	44
2.11	Gray Code	47
2.12	Character Codes	49
2.13	Codes for Actions, Conditions, and States	49
2.14	n -Cubes and Distance	53
2.15	Codes for Detecting and Correcting Errors	54
	2.15.1 Error-Detecting Codes	
	2.15.2 Error-Correcting and Multiple-Error-Detecting Codes	
	2.15.3 Hamming Codes	2.15.4 Two-Dimensional Codes
	2.15.5 Checksum Codes	2.15.6 m -out-of- n Codes
2.16	Codes for Serial Data Transmission and Storage	64
	2.16.1 Parallel and Serial Data	2.16.2 Serial Line Codes
	References	67
	Drill Problems	68
	Exercises	70

3 DIGITAL CIRCUITS 73

3.1	Logic Signals and Gates	74
3.2	Logic Families	78
3.3	CMOS Logic	79
	3.3.1 CMOS Logic Levels	3.3.2 MOS Transistors
	3.3.3 Basic CMOS Inverter Circuit	3.3.4 CMOS NAND and NOR Gates
	3.3.5 Fan-In	3.3.6 Noninverting Gates
	3.3.7 CMOS AND-OR-INVERT and OR-AND-INVERT Gates	
3.4	Electrical Behavior of CMOS Circuits	90
	3.4.1 Overview	3.4.2 A Real-World CMOS Data Sheet
3.5	CMOS Steady-State Electrical Behavior	95
	3.5.1 Logic Levels and Noise Margins	
	3.5.2 Circuit Behavior with Resistive Loads	
	3.5.3 Circuit Behavior with Nonideal Inputs	3.5.4 Fanout
	3.5.5 Effects of Loading	3.5.6 Unused Inputs
	3.5.7 Current Spikes and Decoupling Capacitors	
	3.5.8 How to Destroy a CMOS Device	
3.6	CMOS Dynamic Electrical Behavior	109
	3.6.1 Transition Time	3.6.2 Propagation Delay
	3.6.3 Power Consumption	
3.7	Other CMOS Input and Output Structures	119
	3.7.1 Schmitt-Trigger Inputs	3.7.2 Three-State Outputs
	3.7.3 Open-Drain Outputs	3.7.4 Driving LEDs
	3.7.6 Multisource Buses	3.7.7 Pull-Up Resistors
	3.7.8 Transmission Gates	
	3.7.5 Wired Logic	

3.8	CMOS Logic Families	132
3.8.1	HC and HCT	3.8.2 AC and ACT
3.8.3	HC, HCT, AC, and ACT Electrical Characteristics	
3.8.4	FCT and FCT-T	3.8.5 FCT and FCT-T Electrical Characteristics
3.9	Bipolar Logic	141
3.9.1	Diodes	3.9.2 Diode Logic
3.9.3	Bipolar Junction Transistors	
3.9.4	Transistor Logic Inverter	3.9.5 Schottky Transistors
3.10	Transistor-Transistor Logic	153
3.10.1	Basic TTL NAND Gate	3.10.2 Logic Levels and Noise Margins
3.10.3	Fanout	3.10.4 Unused Inputs
3.11	Additional TTL Gate Types	165
3.11.1	NOR Gates	3.11.2 AND-OR-INVERT Gates
3.11.3	Noninverting Gates	
3.11.4	Three-State and Open-Collector Outputs	
3.12	TTL Families	169
3.12.1	Early TTL Families	3.12.2 Schottky TTL Families
3.12.3	Characteristics of TTL Families	3.12.4 A TTL Data Sheet
3.13	CMOS/TTL Interfacing	173
3.14	Current-Mode Logic	175
3.14.1	Basic CML Circuit	3.14.2 ECL 10K Family
3.14.3	ECL 100K Family	
	References	181
	Drill Problems	182
	Exercises	187

4 COMBINATIONAL LOGIC DESIGN PRINCIPLES 193

4.1	Switching Algebra	194
4.1.1	Axioms	4.1.2 Single-Variable Theorems
4.1.3	Two- and Three-Variable Theorems	4.1.4 n-Variable Theorems
4.1.5	Duality	4.1.6 Standard Representations of Logic Functions
4.2	Combinational Circuit Analysis	210
4.3	Combinational Circuit Synthesis	215
4.3.1	Circuit Descriptions and Designs	4.3.2 Circuit Manipulations
4.3.3	Combinational Circuit Minimization	4.3.4 Karnaugh Maps
4.3.5	Minimizing Sums of Products	4.3.6 Simplifying Products of Sums
4.3.7	"Don't-Care" Input Combinations	
4.3.8	Multiple-Output Minimization	
4.4	Programmed Minimization Methods	239
4.4.1	Representation of Product Terms	
4.4.2	Finding Prime Implicants by Combining Product Terms	
4.4.3	Finding Prime Implicants by Iterative Consensus	
4.4.4	Finding a Minimal Cover Using Prime-Implicant Tables	
4.4.5	Finding a Minimal Cover Using Iterative Consensus	
4.4.6	Other Minimization Methods	
4.5	Timing Hazards	254
4.5.1	Static Hazards	4.5.2 Finding Static Hazards Using Maps
4.5.3	Dynamic Hazards	4.5.4 Designing Hazard-Free Circuits

References	259
Drill Problems	261
Exercises	264

5 COMBINATIONAL LOGIC DESIGN PRACTICES 271

5.1	Documentation Standards	272
5.1.1	Block Diagrams	5.1.2 Gate Symbols
5.1.3	Signal Names and Active Levels	5.1.4 Active Levels for Pins
5.1.5	Bubble-to-Bubble Logic Design	5.1.6 Drawing Layout
5.1.7	Buses	5.1.8 Additional Schematic Information
5.2	Circuit Timing	289
5.2.1	Timing Diagrams	5.2.2 Propagation Delay
5.3	Decoders	297
5.3.1	Binary Decoders	5.3.2 Logic Symbols for Larger-Scale Elements
5.3.3	The 74x139 Dual 2-to-4 Decoder	
5.3.4	The 74x138 3-to-8 Decoder	5.3.5 Cascading Binary Decoders
5.3.6	Binary Decoders as Minterm Generators	
5.3.7	Seven-Segment Decoders	
5.4	Three-State Buffers	311
5.4.1	Standard SSI and MSI Three-State Buffers	
5.5	Encoders	318
5.5.1	Priority Encoders	5.5.2 The 74x148 Priority Encoder
5.6	Multiplexers	323
5.6.1	Standard MSI Multiplexers	5.6.2 Expanding Multiplexers
5.6.3	Multiplexers, Demultiplexers, and Buses	
5.6.4	Multiplexers as Function Generators	
5.7	EXCLUSIVE OR Gates and Parity Circuits	336
5.7.1	EXCLUSIVE OR and EXCLUSIVE NOR Gates	5.7.2 Parity Circuits
5.7.3	The 74x280 9-Bit Parity Generator	
5.7.4	Parity-Checking Applications	
5.8	Comparators	342
5.8.1	Comparator Structure	5.8.2 Iterative Circuits
5.8.3	An Iterative Comparator Circuit	5.8.4 Standard MSI Comparators
5.9	Adders, Subtracters, and ALUs	349
5.9.1	Half Adders and Full Adders	5.9.2 Ripple Adders
5.9.3	Subtracters	5.9.4 Carry Lookahead Adders
5.9.5	MSI Adders	
5.9.6	MSI Arithmetic and Logic Units	5.9.7 Group-Carry Lookahead
5.10	Combinational Multipliers	364
5.11	Combinational Logic Design with MSI Functions	367
5.11.1	Using MSI Functions for "Random Logic"	
5.11.2	Almost-MSI Functions	
5.11.3	Finding the MSI Functions in Larger Problems	
References	377	
Drill Problems	378	
Exercises	381	

6	COMBINATIONAL LOGIC DESIGN WITH PLDS	391
6.1	Programmable Logic Arrays	392
6.2	PLD Circuit and Programming Technologies	396
6.2.1	Bipolar PLDs	
6.2.2	CMOS PLDs	
6.2.3	Programming and Testing	
6.3	Programmable Array Logic Devices	401
6.4	The ABEL PLD Programming Language	405
6.4.1	ABEL Program Structure	
6.5	ABEL Documentation	408
6.5.1	Program Listings	
6.5.2	Fuse Patterns	
6.5.3	Signal Polarity	
6.6	Two-Pass Logic	412
6.7	Combinational PLD Applications	413
6.7.1	Decoders	
6.7.2	Multiplexers	
6.8	ABEL Sets and Relations	421
6.9	Additional Combinational PLD Applications	423
6.10	Other Combinational PLDs and Applications	428
6.11	Three-State Output Control	431
6.11.1	Three-State Output Example	
6.11.2	Bidirectional I/O Pins	
6.12	Generic Array Logic Devices	435
	References	441
	Drill Problems	442
	Exercises	444
7	SEQUENTIAL LOGIC DESIGN PRINCIPLES	447
7.1	Bistable Elements	449
7.1.1	Digital Analysis	
7.1.2	Analog Analysis	
7.1.3	Metastable Behavior	
7.2	Latches and Flip-Flops	452
7.2.1	S-R Latch	
7.2.2	/S-/R Latch	
7.2.3	S-R Latch with Enable	
7.2.4	D Latch	
7.2.5	Edge-Triggered D Flip-Flop	
7.2.6	Master/Slave S-R Flip-Flop	
7.2.7	Master/Slave J-K Flip-Flop	
7.2.8	Edge-Triggered J-K Flip-Flop	
7.2.9	T Flip-Flop	
7.3	Clocked Synchronous State-Machine Analysis	467
7.3.1	State-Machine Structure	
7.3.2	Characteristic Equations	
7.3.3	Analysis of State Machines with D Flip-Flops	
7.3.4	Analysis of State Machines with J-K Flip-Flops	
7.4	Clocked Synchronous State-Machine Design	481
7.4.1	State-Table Design Example	
7.4.2	State Minimization	
7.4.3	State Assignment	
7.4.4	Synthesis Using D Flip-Flops	
7.4.5	Synthesis Using J-K Flip-Flops	
7.4.6	More Design Examples Using D Flip-Flops	
7.5	Feedback Sequential Circuits	503
7.5.1	Analysis	
7.5.2	Analyzing Circuits with Multiple Feedback Loops	
7.5.3	Races	
7.5.4	State Tables and Flow Tables	
7.5.5	Comments	

7.6	Feedback Sequential Circuit Design	514
7.6.1	Latches	
7.6.2	Designing Fundamental-Mode Flow Tables	
7.6.3	Flow-Table Minimization	
7.6.4	Race-Free State Assignment	
7.6.5	Excitation Equations	
7.6.6	Essential Hazards	
7.6.7	Summary	
	References	527
	Drill Problems	528
	Exercises	531

8 SYNCHRONOUS DESIGN WITH STATE MACHINES 539

8.1	Synchronous Design Methodology	540
8.1.1	Synchronous System Structure	
8.1.2	A Synchronous System Design Example	
8.2	Ad Hoc State-Machine Design	545
8.2.1	An Ad Hoc Example	
8.2.2	Finite-Memory Design	
8.3	Designing State Machines Using State Diagrams	550
8.4	Designing State Machines Using ASM Charts	557
8.4.1	ASM-Chart Examples	
8.4.2	ASM Transition Lists and Expressions	
8.5	Synthesizing State Machines from Transition Lists	562
8.5.1	Transition Equations	
8.5.2	Excitation Equations	
8.5.3	Variations on the Scheme	
8.5.4	Realizing the State Machine	
8.6	Another Example State Machine	566
8.6.1	The Guessing Game	
8.6.2	Unused States	
8.6.3	Output-Coded State Assignment	
8.6.4	"Don't-Care" State Codings	
8.7	Decomposing State Machines	574
	References	576
	Drill Problems	577
	Exercises	578

9 SEQUENTIAL LOGIC DESIGN PRACTICES 581

9.1	Sequential Circuit Documentation Standards	582
9.1.1	General Requirements	
9.1.2	Logic Symbols	
9.1.3	State-Machine Descriptions	
9.1.4	Timing Diagrams and Specifications	
9.2	Latches and Flip-Flops	586
9.2.1	SSI Latches and Flip-Flops	
9.2.2	Switch Debouncing	
9.2.3	The Simplest Switch Debouncer	
9.2.4	Multibit Registers and Latches	
9.3	Counters	593
9.3.1	Ripple Counters	
9.3.2	Synchronous Counters	
9.3.3	MSI Counters and Applications	
9.3.4	Decoding Binary-Counter States	
9.4	Shift Registers	606
9.4.1	Shift-Register Structure	
9.4.2	MSI Shift Registers	
9.4.3	The World's Biggest Shift-Register Application	
9.4.4	Serial/Parallel Conversion	
9.4.5	Shift-Register Counters	
9.4.6	Ring Counters	
9.4.7	Johnson Counters	
9.4.8	Linear Feedback Shift Register Counters	

9.5	Iterative versus Sequential Circuits	628
9.6	MSI Devices as State Machines	631
9.7	Impediments to Synchronous Design	634
	9.7.1 Clock Skew 9.7.2 Gating the Clock 9.7.3 Asynchronous Inputs	
9.8	Synchronizer Failure and Metastability Estimation	642
	9.8.1 Synchronizer Failure 9.8.2 Metastability Resolution Time	
	9.8.3 Reliable Synchronizer Design 9.8.4 Analysis of Metastable Timing	
	9.8.5 Better Synchronizers 9.8.6 Other Synchronizer Designs	
	9.8.7 Metastable-Hardened Flip-Flops	
	References	651
	Drill Problems	652
	Exercises	653
10	SEQUENTIAL LOGIC DESIGN WITH PLDS	659
10.1	Bipolar Sequential PLDs	660
10.2	Sequential GALs	664
10.3	PLD Timing Specifications	670
10.4	PLD Realizations of Sequential MSI Functions	672
	10.4.1 Edge-Triggered Registers 10.4.2 Shift Registers	
	10.4.3 Counters 10.4.4 Latches	
10.5	Counter Design With PLDs	681
	10.5.1 Counter Behavior 10.5.2 X-Series PLDs	
	10.5.3 Counter Design with X-Series PLDs	
	10.5.4 Cascading and Carry Outputs	
10.6	Sequential-PLD Applications	687
	10.6.1 Combining MSI Functions 10.6.2 Shift-Register Counters	
	10.6.3 X-Series Design Example	
10.7	State-Machine Design with Sequential PLDs	695
	10.7.1 Timing and Packaging of PLD-Based State Machines	
	10.7.2 Ad Hoc Design of PLD-Based State Machines	
	10.7.3 Synthesizing PLD-Based State Machines Using Transition Lists	
10.8	State-Machine Description Language for PLDs	705
	10.8.1 Simple State-Diagram Examples 10.8.2 T-Bird Tail Lights	
	10.8.3 Reinventing Traffic-Light Controllers	
	References	719
	Drill Problems	720
	Exercises	720
11	MEMORY	723
11.1	Read-Only Memory	724
	11.1.1 Using ROMs for "Random" Combinational Logic Functions	
	11.1.2 Internal ROM Structure 11.1.3 Two-Dimensional Decoding	
	11.1.4 Commercial ROM Types 11.1.5 ROM Control Inputs and Timing	
	11.1.6 ROM Applications	

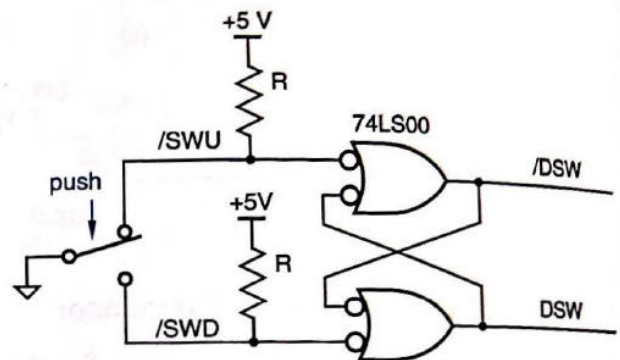
11.2	Read/Write Memory	746
11.3	Static RAM	747
	11.3.1 Static-RAM Inputs and Outputs	
	11.3.2 Static-RAM Internal Structure	11.3.3 Static-RAM Timing
	11.3.4 Standard Static RAMs	
11.4	Dynamic RAM	753
	11.4.1 Dynamic-RAM Structure	11.4.2 Dynamic-RAM Timing
	References	759
	Drill Problems	760
	Exercises	760
12	ADDITIONAL REAL-WORLD TOPICS	763
12.1	Computer-Aided Engineering Tools	763
	12.1.1 Schematic Capture	12.1.2 Circuit Analysis and Simulation
	12.1.3 Hardware Description Languages	
	12.1.4 Printed-Circuit-Board Layout	
12.2	Design for Testability	771
	12.2.1 Testing	12.2.2 Bed-of-Nails and In-Circuit Testing
	12.2.3 Scan Methods	
12.3	Estimating Digital System Reliability	777
	12.3.1 Failure Rates	12.3.2 Reliability and MTBF
	12.3.3 System Reliability	
12.4	Transmission Lines, Reflections, and Termination	782
	12.4.1 Basic Transmission-Line Theory	
	12.4.2 Logic-Signal Interconnections as Transmission Lines	
	References	789
A	IEEE STANDARD SYMBOLS	791
A.1	General Definitions	791
A.2	Decoders	793
A.3	Three-State Buffers	796
A.4	Priority Encoders	798
A.5	Multiplexers and Demultiplexers	800
A.6	EXCLUSIVE-OR and Parity Functions	802
A.7	Comparators	803
A.8	Adders	803
A.9	Latches, Flip-Flops, and Registers	804
A.10	Counters	806
A.11	Shift Registers	808
A.12	Pros and Cons of IEEE Standard Symbols	808
	Exercises	810
	INDEX	811

top inverter output is no longer shorted to ground, and feedback in the bistable maintains the logic 0 on /SW even if the wiper bounces off the bottom contact, as it does.

Advantages of this circuit compared to other debouncing approaches are that it has a low chip count (one-third of a 74LS04), no pull-up resistors are required, and both polarities of the input signal (active-high and active-low) are produced. In situations where momentarily shorting gate outputs must be avoided, a similar circuit can be designed using a /S-/R latch and pull-up resistors, as suggested in Figure 9-6.

Figure 9-6

Switch input using a /S-/R latch for debouncing.



9.2.4 Multibit Registers and Latches

register

A collection of two or more D flip-flops with a common clock input is called a *register*. Registers are often used to store a collection of related bits, such as a byte of data in a computer. However, a single register can also be used to store unrelated bits of data or control information; the only real constraint is that all of the bits are stored using the same clock signal.

74x175

74x174

Figure 9-7(a) and (b) shows the logic diagram and logic symbol for a commonly used MSI register, the 74x175. The 74x175 contains four edge-triggered D flip-flops and provides both active-high and active-low outputs at the external pins of the device. The 74x174, shown in (c), is similar, except that it eliminates the active-low outputs and provides two more flip-flops instead.

The individual flip-flops in a '175 are negative-edge triggered, as indicated by the inversion bubbles on their CLK inputs. However, the circuit also contains an inverter that makes the flip-flops positive-edge triggered with respect to the device's external CLK input pin. A common, active-low, clear signal (/CLR) is connected to the asynchronous clear inputs of all four flip-flops. Both CLK and /CLR are buffered before fanning out to the four flip-flops, so that a device driving one of these inputs sees only one unit load instead of four. This is especially important if a common clock or clear signal must drive many such registers.