

## **Exhibit A: Claim Chart for U.S. Patent 8,924,596**

### **U.S. Patent No. 8,924,596**

This claim chart is based on publicly available literature, the source code<sup>1</sup> Defendants have made available, and the documents currently produced by Defendants (AMD-CV-0000001–AMD-CV-00005452). Plaintiffs Concurrent Ventures, LLC and XstreamEdge, Inc. (“Plaintiffs” or “CV”) reserve the right to supplement and/or amend their positions based on discovery from Defendants Advanced Micro Devices, Inc. and Pensando Systems, Inc. (“AMD Pensando” or “Defendants”), including technical documentation such as schematics and datasheets, and source code. Plaintiffs reserve the right to amend these contentions for good cause with leave of the Court.

Defendants infringed and continue to infringe U.S. Patent No. 8,924,596 (the “’596 patent”) by having made, used, sold or offered for sale, and/or imported into the United States their Distributed Services Cards (“DSCs”) and Data Processing Units (“DPUs”) including at least Elba, Capri, Giglio, and Salina (including AMD DSC2-25G, AMD DSC2-100G, and AMD DSC2-200), as well as their DPU and DSC technology when implemented in other products, services, and offerings, for example the SmartSwitch or AMD Pensando Pollara 400<sup>2</sup> (collectively, the “Accused Products,” “Accused DPUs,” or “Accused DSCs”). For an example, Defendants directly infringe when they themselves implement, use, or test the Accused Products in the claimed manner discussed herein.

Additionally, Defendants also indirectly infringe the ’596 patent by having induced and/or contributed to third parties’ infringement, including the infringement of Defendants’ customers. In particular, Defendants, through their advertising, marketing, communications with customers and clients, troubleshooting, guidance, testing, setting of default settings, and helping, actively and knowingly aids and abets their customers’ and clients’ infringement, including their use of the Accused Products. Defendants also sold or offered to sell into the United States, or imported into the United States, their Accused Products, which are material components of the infringing implementation and not staple articles of commerce capable of substantial noninfringing use, as shown, for example, at least by Defendants’ own descriptions, guidance, and instructions to implement the Accused Products. Defendants have known of the patents, their infringement, and that the Accused Products are especially made for use in a manner that would infringe the patent when they sold, offered to sell, and/or imported the Accused Products. Further details are provided herein.

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<sup>1</sup> Due to the parties’ ongoing negotiations regarding the protective order and the time constraints inherent in the draft procedures for printing source code in the protective order, these contentions incorporate Plaintiffs’ review of the source code but do not explicitly refer to the source code.

<sup>2</sup> <https://www.tomshardware.com/networking/amd-unveils-industrys-first-ultra-ethernet-ready-network-card-for-ai-and-hpc>, CV-AMD0016365; CV-AMD0017532.

**Exhibit A: Claim Chart for U.S. Patent 8,924,596**

Theories exemplifying how the Accused Products infringe the asserted claims of the '596 patent are detailed herein. The products included are representative; on information and belief, all Accused Products function in substantially the same manner as one or more of the examples provided, and include generally the same components. For example, for purposes of infringement of the '596 patent, Defendants' Elba, Capri, Giglio, and Salina versions operate, in relevant part, in the same manner, and thus infringe in substantially the same way. *See* AMD-CV-0002195–AMD-CV-0002196; AMD-CV-0004986–AMD-CV-0005004 at AMD-CV-0004988; AMD-CV-0003945–AMD-CV-0004184 at AMD-CV-0003962; AMD-CV-0002195; AMD-CV-0004986; Defendants' Response to Interrogatory Nos. 1, 2. The following documents provide additional support for Plaintiffs' infringement theories documented herein: AMD-CV-0001962; AMD-CV-0000001; AMD-CV-0000608; AMD-CV-0000643; AMD-CV-0000935; AMD-CV-0000988; AMD-CV-0000994; AMD-CV-0001126; AMD-CV-0001155; AMD-CV-0002797; AMD-CV-0002200; AMD-CV-0004235; AMD-CV-0003945–AMD-CV-0004184; Defendants' Response to Interrogatory Nos. 1, 2. This is further shown by the evidence for the various versions cited herein.

| Claim Language                                                                                                         | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [1pre] A system for dividing and synchronizing a processing task across a plurality of processing elements comprising: | <p>To the extent the preamble is limiting, Defendants make, use, test, sell, and offer to sell the claimed system for dividing and synchronizing a processing task across a plurality of processing elements, including by making, using, testing, selling, and offering to sell the Accused Products; implementing and/or testing those Accused Products in their own platforms; and providing them to customers. <i>See, e.g.</i>, AMD-CV-0003945–AMD-CV-0004184.</p> <p>The AMD Pensando DSC is designed with multiple processing elements, including general-purpose cores (like ARM cores); specialized processing units, such as Match Processing Units (MPUs); processors in the P4 Pipelines, including in the DMA engines and P4 ingress and egress; and accelerators (for example SRAM, Crypto, CRC, and Comp/Decomp). The DSCs split the processing task (such as packet processing or protocol handling) across all of these multiple elements.</p> |

**Exhibit A: Claim Chart for U.S. Patent 8,924,596**

| Claim Language                               | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                              | <p><b>Hardware-assisted Functions</b></p> <ul style="list-style-type: none"><li>• SRAM controller can perform updates to table entries</li><li>• Before MPU starts processing them</li><li>• It can be used for read-modify-write operations</li></ul> <div><div>Policer</div><div>Counter</div></div> <ul style="list-style-type: none"><li>• Supported through <i>table properties</i></li></ul> <p><a href="https://opennetworking.org/wp-content/uploads/2020/11/2020-EuroP4-Mario-Baldi.pdf">https://opennetworking.org/wp-content/uploads/2020/11/2020-EuroP4-Mario-Baldi.pdf</a>, CV-AMD0016101.</p>                                                                              |
| [1a] an input queue implemented in hardware; | <p>The Accused Products includes input queues implemented in hardware.</p> <p>The Accused AMD Pensando DPU enabled systems such as AMD Pensando DSCs or SmartSwitch contain input and output queues implemented in hardware. For example, in AMD Pensando DPU architecture, there are many input queues to different processing elements or stages (e.g., P4 Ingress, P4 Egress, P4 RxDMA, etc.), implemented in the hardware to efficiently manage packet processing and traffic flow. These queues are located within the central Packet Buffer. Additionally, AMD Pensando DSCs include input queues implemented in hardware for each of the various processors discussed herein.</p> |

## Exhibit A: Claim Chart for U.S. Patent 8,924,596

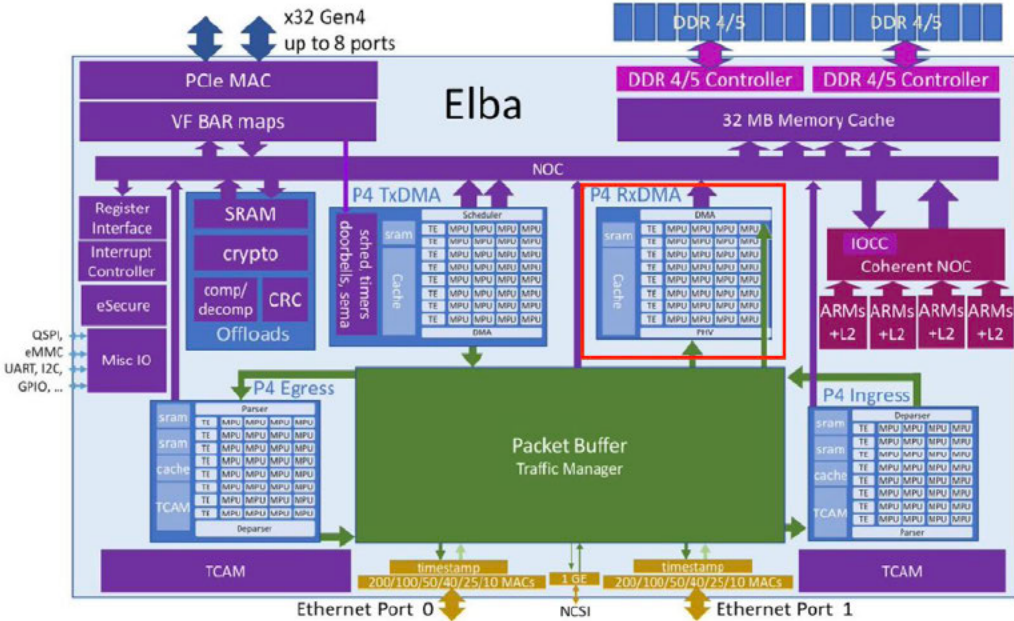
| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                |  <p>The diagram illustrates the Elba network processor architecture. At the top, it features a PCIe MAC connected to x32 Gen4 ports (up to 8 ports) and VF BAR maps. The central component is the Elba processor, which includes a 32 MB Memory Cache, a Coherent NOC, and four ARM cores with L2 caches. The architecture is divided into several functional blocks: P4 Tx/DMA, P4 Rx/DMA, P4 Egress, and P4 Ingress. These blocks are interconnected via a central Packet Buffer Traffic Manager. The P4 Tx/DMA block includes a scheduler, cache, and TCAM. The P4 Rx/DMA block includes a cache and TCAM. The P4 Egress and P4 Ingress blocks also include caches and TCAMs. The central Packet Buffer Traffic Manager is connected to Ethernet Port 0 and Ethernet Port 1 via NCSI. The diagram also shows various peripheral components like SRAM, crypto, comp/decomp, CRC, Offloads, Register Interface, Interrupt Controller, eSecure, Misc IO, and QSPI, eMMC, UART, I2C, GPIO, ...</p> <p><a href="https://www.servethehome.com/pensando-distributed-services-architecture-smartnic/">https://www.servethehome.com/pensando-distributed-services-architecture-smartnic/</a>, CV-AMD0015900.</p> |

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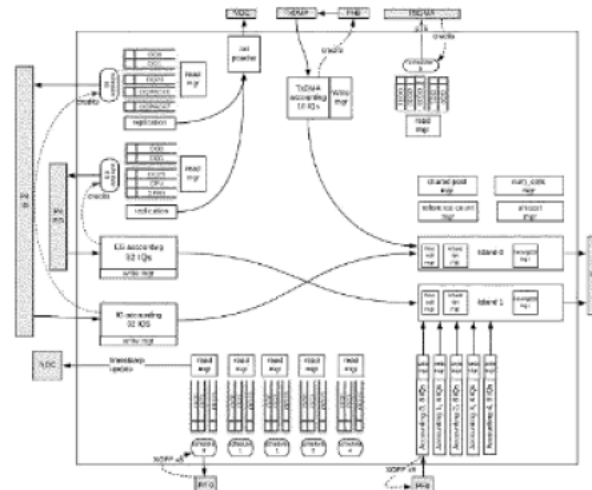
## Claim Language

## Infringement Contentions and Exemplary Evidence of Infringement

<https://www.amd.com/content/dam/amd/en/documents/pensando-technical-docs/white-papers/pensando-comparison-of-dpu-hardware-strategies.pdf>, p. 13, CV-AMD0015807.

AMD Pensando DSCs are designed with millions of hardware queues to manage and prioritize packet flows.

## Exhibit A: Claim Chart for U.S. Patent 8,924,596

| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <div> <p>[AMD Official Use Only - General]</p> <h3 style="text-align: center;">Packet Buffer</h3> <ul style="list-style-type: none"> <li>Shared memory switch <ul style="list-style-type: none"> <li>Multiple VOQs</li> <li>Multiple CoS</li> <li>Enhanced Tx Selection (ETS) Scheduling</li> <li>Replication (Multicast, SPAN)</li> <li>Network Pause Buffering</li> <li>Burst overflow regions at ingress</li> </ul> </li> <li>Ports: tm_iport, tm_oport <ul style="list-style-type: none"> <li>0.3 : ethernet 0.3, 16 queues each</li> <li>4: 1 Gb/s interface, 16 queues</li> <li>5: TxDMA/RxDMA, 16/32 queues</li> <li>6: P4 Egress, 32 queues</li> <li>7: P4 Ingress, 32 queues</li> </ul> </li> </ul>  <p style="text-align: center;">AMD-CV-0005079.</p> </div> <p>AMD Pensando DSCs have millions of hardware queues to manage and prioritize packet flows.</p> |

## Exhibit A: Claim Chart for U.S. Patent 8,924,596

| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <p style="text-align: center;"><b>SOC, NOC, &amp; hardware queues</b></p> <hr/> <ul style="list-style-type: none"> <li>• Network On Chip (NOC) connects CPUs, memory, P4 DMA, and offload engines in a cache-coherent domain</li> <li>• ARM A-72 CPUs run SMP Linux, DPDK supported</li> <li>• P4 programs can push packet headers and data structures directly into ARM L2 caches or the last level system cache</li> <li>• Doorbells for <u>16 million hardware queues</u> are mapped to host or ARM processes, initiates multi-level scheduler to inject P4 pipeline tokens</li> </ul> <div> </div> <p style="text-align: center;"><i>Hot Chips 32 Pensando SOC NOC And Hardware Queues</i></p> <p><a href="https://www.servethehome.com/pensando-distributed-services-architecture-smartnic">https://www.servethehome.com/pensando-distributed-services-architecture-smartnic</a>, CV-AMD0016001.</p> <p>The hardware queues use doorbell mechanisms to signal when space is available in the input queues. These doorbells trigger the multi-level scheduler, which assigns resources to the input queues and coordinates the dispatch of packets into the P4 pipeline. This ensures that the associated processing elements receive a steady stream of packets, allowing the DPU to process data efficiently and maintain high throughput.</p> |

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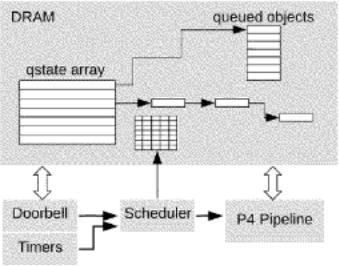
| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <div style="text-align: center; margin-bottom: 10px;"> <small>(AMD Official Use Only - General)</small> </div> <div style="text-align: center;"> <h3>Packet Buffer - Hardware Queues</h3> </div> <div style="display: flex; justify-content: space-around; align-items: flex-start;"> <div style="text-align: center;">  </div> <div> <ul style="list-style-type: none"> <li>• Upto 16M queues</li> <li>• Pkts from wire or internal placed in queues</li> <li>• Help manage Interfaces, Flows, Connections, other objects that need ordering, tracking and scheduling</li> <li>• Queue states maintained Qstate record               <ul style="list-style-type: none"> <li>• Enqueued objects count, linked-lists, connection state, process-id (memory protection)</li> </ul> </li> <li>• Events Enqueuing object(s) through Doorbells</li> <li>• HW timer markers set for periodic events to be scheduled, ex: TCP timers</li> <li>• Queues organized as Scheduling groups, Interface Groups and Class of Service (CoS) groups.</li> <li>• When a Queue is scheduled, a PHV token with QID and CoS is inserted into P4 pipeline</li> </ul> </div> </div> <div style="display: flex; justify-content: space-between; margin-top: 20px;"> <div style="text-align: center;"><small>12</small></div> <div style="text-align: right;">  </div> </div> <div style="text-align: center; margin-top: 20px;"> <h2>AMD-CV-0005080.</h2> </div> |

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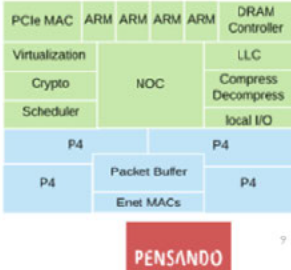
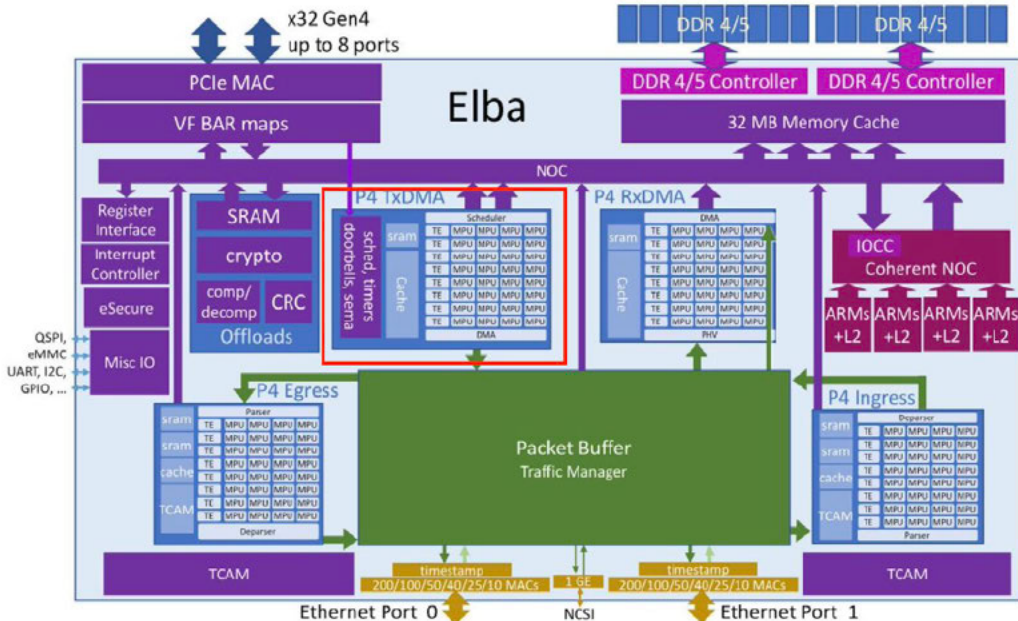
| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <p><b>SOC, NOC, &amp; Hardware Queues</b></p> <p>NOC connects P4 DMA, offload engines, ARM, PCIe, and DRAM in both coherent and non-coherent domains</p> <p>ARM CPUs run SMP Linux and interface to P4 with either a netDev or DPDK interface</p> <p>Doorbells for 16 million hardware queues are mapped to host or ARM processes and initiate multi-level scheduler to inject P4 pipeline tokens</p> <p>Ethernet and DPDK device drivers available for multiple host OSes</p>  <p><small>HotChips 2020   August 18, 2020</small></p> <p>Distributed Services Architecture by Francis Matus, HotChips (2020), CV-AMD0016381.</p> |

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| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <div> </div> <p>Michael Galles and Francis Matus, “Pensando Distributed Services Architecture” in Theme Article: Hot Chips (2021), CV-AMD0016134.</p> <p> <b>Life of a Packet</b><br/> Packets received through the network enter on one of the Ethernet MAC interfaces and are placed in the packet buffer according to L2 or L3 class of service (COS). The packet buffer provides pause absorption buffering and COS aware arbitration for the P4 ingress pipeline. Consistent with the P4 model, packets pass through the P4 ingress pipeline for flow classification, firewall, tunnel endpoint processing, and other ingress services; return to the packet buffer in case of multicast or span replication; then enter the P4 egress pipeline to apply, for example, network address translation, policers, and telemetry. Having completed network processing tasks, the packet can be sent back out an Ethernet MAC port or it can be passed up toward the ARM subsystem or local host. </p> <p>Michael Galles and Francis Matus, “Pensando Distributed Services Architecture” in Theme Article: Hot Chips (2021), CV-AMD0016133–CV-AMD0016134.</p> |

## Exhibit A: Claim Chart for U.S. Patent 8,924,596

| Claim Language                                       | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>[1b] an output queue implemented in hardware;</p> | <p>The Accused Products include output queues implemented in hardware.</p> <p>For example, in AMD Pensando's DPU architecture, there are many output queues implemented in the hardware, contained within the central Packet Buffer, to efficiently manage packet processing and traffic flow. These output queues contain post-processed packets or responses. Additionally, AMD Pensando DSCs include output queues implemented in hardware for each of the various processors discussed herein. <i>See generally</i> claim 1a.</p>  <p>The diagram illustrates the AMD Pensando DPU architecture. At the top, it shows connections for x32 Gen4 up to 8 ports to the PCIe MAC and VF BAR maps. The central Elba block connects to various components including a Register Interface, Interrupt Controller, eSecure, Misc IO, SRAM, crypto, comp/decomp, CRC, and Offloads. It also connects to P4 Tx/DMA and P4 Rx/DMA blocks, which contain schedulers, caches, and DMA engines. The P4 Egress and P4 Ingress blocks are connected to the central Packet Buffer Traffic Manager. The architecture includes multiple TCAMs, SRAMs, and caches, as well as various controllers like the DDR 4/5 Controller and IOCC Coherent NOC. The bottom of the diagram shows connections to Ethernet Port 0 and Ethernet Port 1 via NCSI, with timestamp and MAC address information.</p> <p><a href="https://www.servethehome.com/pensando-distributed-services-architecture-smartnic">https://www.servethehome.com/pensando-distributed-services-architecture-smartnic</a>, CV-AMD0016000.</p> |

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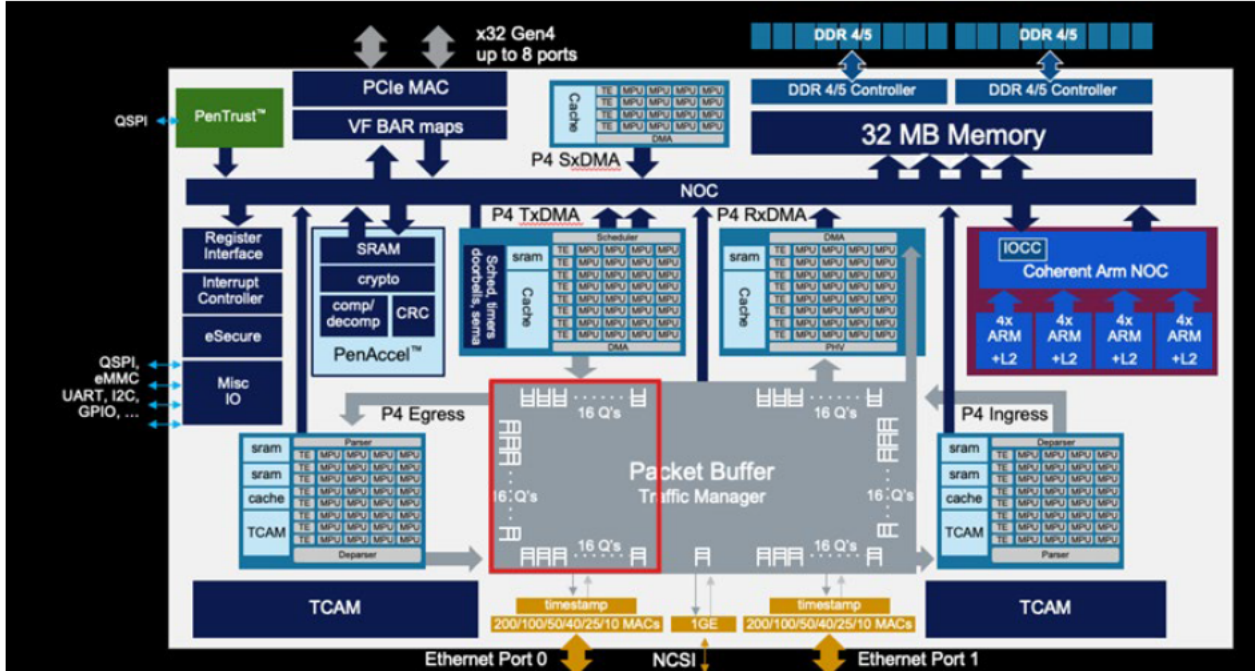
| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                |  <p>The diagram illustrates the Pensando P4 hardware architecture. At the top, it shows connections for x32 Gen4 up to 8 ports, DDR 4/5 memory (32 MB), and various controllers like PenTrust, PCIe MAC, and VF BAR maps. The central part features a Network-on-Chip (NOC) with P4 SxDMA, P4 TxDMA, and P4 RxDMA. Below the NOC is the Packet Buffer Traffic Manager, which includes a Scheduler, Cache, and various buffers (16 Q's). The architecture also includes a Coherent Arm NOC with 4x ARM + L2 processors, and various peripheral components like SRAM, PenAccel, TCAM, and Ethernet Port 0/1. The bottom of the diagram shows connections for Ethernet Port 0, NCSI, and Ethernet Port 1.</p> <p><a href="https://www.amd.com/content/dam/amd/en/documents/pensando-technical-docs/white-papers/pensando-comparison-of-dpu-hardware-strategies.pdf">https://www.amd.com/content/dam/amd/en/documents/pensando-technical-docs/white-papers/pensando-comparison-of-dpu-hardware-strategies.pdf</a>, CV-AMD0015807.</p> |

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| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <p><b>SOC, NOC, &amp; Hardware Queues</b></p> <p>NOC connects P4 DMA, offload engines, ARM, PCIe, and DRAM in both coherent and non-coherent domains</p> <p>ARM CPUs run SMP Linux and interface to P4 with either a netDev or DPDK interface</p> <p>Doorbells for 16 million hardware queues are mapped to host or ARM processes and initiate multi-level scheduler to inject P4 pipeline tokens</p> <p>Ethernet and DPDK device drivers available for multiple host OSes</p> <div> <p>The diagram illustrates the Distributed Services Architecture. It features a central green block labeled 'NOC' (Network On Chip). To the left of the NOC are several green blocks: 'PCIe MAC', 'Virtualization', 'Crypto', and 'Scheduler'. To the right of the NOC are 'ARM' (multiple instances), 'DRAM Controller', 'LLC', 'Compress Decompress', and 'local I/O'. Below the NOC and its associated blocks are blue blocks labeled 'P4'. At the bottom center, there is a red block labeled 'PENSANDO'.</p> </div> <p><small>HotChips 2020   August 18, 2020</small></p> <p>Distributed Services Architecture by Francis Matus, HotChips 2020, CV-AMD0016381.</p> |

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|------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                          | <p><b>Life of a Packet</b><br/>Packets received through the network enter on one of the Ethernet MAC interfaces and are placed in the packet buffer according to L2 or L3 class of service (COS). The packet buffer provides pause absorption buffering and COS aware arbitration for the P4 ingress pipeline. Consistent with the P4 model, packets pass through the P4 ingress pipeline for flow classification, firewall, tunnel endpoint processing, and other ingress services; return to the packet buffer in case of multicast or span replication; then enter the P4 egress pipeline to apply, for example, network address translation, policers, and telemetry. Having completed network processing tasks, the packet can be sent back out an Ethernet MAC port or it can be passed up toward the ARM subsystem or local host.</p> <p>Michael Galles and Francis Matus, “Pensando Distributed Services Architecture” in Theme Article: Hot Chips (2021), CV-AMD0016133–CV-AMD0016134.</p> |
| [1c] a first processing element having access to said input queue and said output queue; | <p>The Accused Products includes a first processing element having access to said input queue and said output queue.</p> <p>The AMD Pensando DSCs include many “first processing element[s]” having access to said input queue and said output queue. As a general matter, the “first processing element” in the AMD Pensando DSC are those processors that communicate with the above identified input and output queues. For example, the processors in the P4 Packet Processing Dataplane, including in the DMA engine, (e.g., the TE), are each a “first processing element” that, as shown in the below diagrams, have access to said input queue and said output queue. Similarly,</p>                                                                                                                                                                                                                                                                                                     |

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|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <p>the processors in the packet buffer, including in the P4 ingress and egress, (e.g., the TE) are each a “first processing element” that, as shown in the below diagrams, have access to said input queue and said output queue. The ARM cores and offloads/accelerators can also each serve as a “first processing element” when they communicate with the input and output queues. As another example, the DPU has first processing elements such as table engines or MPUs that have access to the input and output queues for scheduling operations performed by parts of the DPU.</p> <div> <p style="text-align: center;"><a href="https://www.youtube.com/watch?v=in7athW-PaQ">https://www.youtube.com/watch?v=in7athW-PaQ</a>,</p> </div> |

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| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <p>CV-AMD0016269.</p> <p><a href="https://www.servethehome.com/pensando-distributed-services-architecture-smartnic">https://www.servethehome.com/pensando-distributed-services-architecture-smartnic</a></p> <p>CV-AMD0016000.</p> <p>For another example, server processors and/or the host processors within the system and VMs running on a system containing AMD Pensando DSCs are each a “first processing element” that, as shown below, have access to the above-identified input queues and output queues.</p> |

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|                | <div> <p>The diagram illustrates the NVMeoF/TCP Offload architecture. It shows two main components: a Hypervisor and an OS/Container. The Hypervisor contains two VMs, each with an NVMe Initiator*. Below the VMs is the NVMe Emulation layer, which includes Emulated Local Storage, NVMeoF Initiator, and Remote Storage Management (NAPLES DSC). The OS/Container also contains an NVMe Initiator*, NVMe Emulation layer with Emulated Local Storage, NVMeoF Initiator, and Remote Storage Management (NAPLES DSC). Both NAPLES DSCs connect via NVMeoF (RDMA or TCP) to a network of nodes, which then connects to an NVMeoF Target.</p> </div> <p><a href="https://www.youtube.com/watch?v=in7athW-PaQ">https://www.youtube.com/watch?v=in7athW-PaQ</a>, CV-AMD0016269.</p> |

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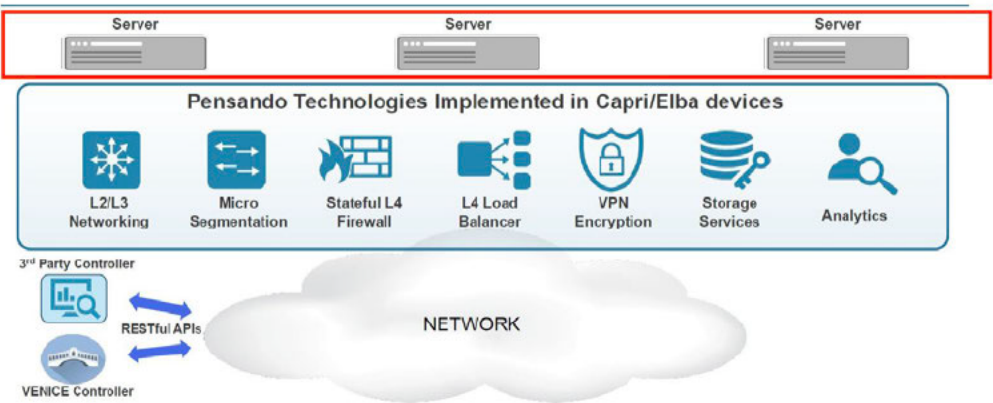
| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <p>Pensando: Distributed Services Architecture</p>  <p><a href="https://www.servethehome.com/pensando-distributed-services-architecture-smartnic">https://www.servethehome.com/pensando-distributed-services-architecture-smartnic</a>, CV-AMD0016000; <i>see</i> AMD-CV-0001083–AMD-CV-0001125; “White Paper: Creating a Distributed Services Architecture in Existing Data Center Environments,” AMD-CV-0004642–AMD-CV-0004651.</p> |

**Exhibit A: Claim Chart for U.S. Patent 8,924,596**

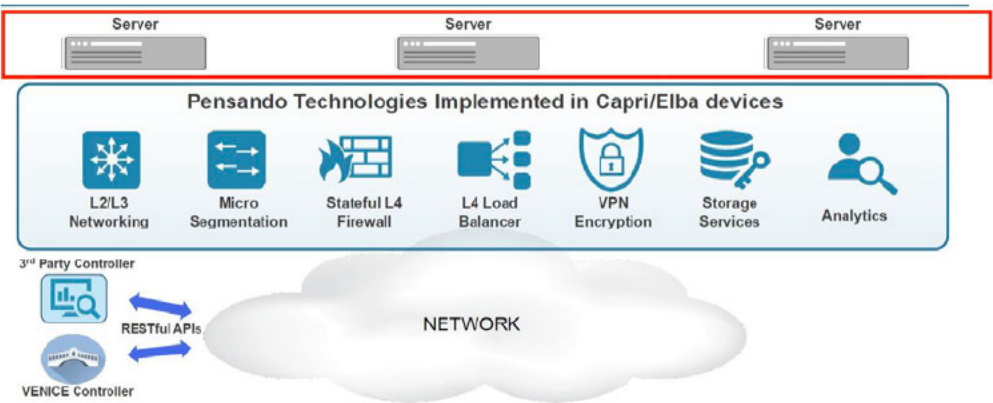
| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <p>Pensando: Distributed Services Architecture</p>  <p><a href="https://www.servethehome.com/pensando-distributed-services-architecture-smartnic">https://www.servethehome.com/pensando-distributed-services-architecture-smartnic</a>, CV-AMD0016000; <i>see</i> AMD-CV-0001083–AMD-CV-0001125; “White Paper: Creating a Distributed Services Architecture in Existing Data Center Environments,” AMD-CV-0004642–AMD-CV-0004651.</p> |

**Exhibit A: Claim Chart for U.S. Patent 8,924,596**

The diagram illustrates the Elba SoC architecture, centered around a Packet Buffer Traffic Manager. Key components and connections include:

- Top Interfaces:** x32 Gen4 up to 8 ports (PCIe MAC), DDR 4/5 (DDR 4/5 Controller), and 32 MB Memory Cache.
- Central Processing:** Elba core, P4 TxDMA, P4 RxDMA, and P4 Egress/P4 Ingress pipelines.
- Memory and Storage:** SRAM, crypto, comp/decomp, CRC, and Offloads.
- Control and Security:** Register Interface, Interrupt Controller, eSecure, and Misc IO.
- Network and I/O:** Ethernet Port 0, Ethernet Port 1, NCSI, and various peripheral interfaces (QSPI, eMMC, UART, I2C, GPIO, ...).
- Internal Structures:** TCAM, Parser, Scheduler, Cache, and various MPUs (MPU, MPU, MPU, MPU).

**Exhibit A: Claim Chart for U.S. Patent 8,924,596**

| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <p>Life of a Packet</p> <p>Packets received through the network enter on one of the Ethernet MAC interfaces and are placed in the packet buffer according to L2 or L3 class of service (COS). The packet buffer provides pause absorption buffering and COS aware arbitration for the P4 ingress pipeline. Consistent with the P4 model, packets pass through the P4 ingress pipeline for flow classification, firewall, tunnel endpoint processing, and other ingress services; return to the packet buffer in case of multicast or span replication; then enter the P4 egress pipeline to apply, for example, network address translation, policers, and telemetry. Having completed network processing tasks, the packet can be sent back out an Ethernet MAC port or it can be passed up toward the ARM subsystem or local host.</p> <p>Michael Galles and Francis Matus, “Pensando Distributed Services Architecture” in Theme Article: Hot Chips (2021), CV-AMD0016133–CV-AMD0016134.</p> |

# Exhibit A: Claim Chart for U.S. Patent 8,924,596

| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                        |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <p><a href="https://www.amd.com/content/dam/amd/en/documents/pensando-technical-docs/white-papers/pensando-comparison-of-dpu-hardware-strategies.pdf">https://www.amd.com/content/dam/amd/en/documents/pensando-technical-docs/white-papers/pensando-comparison-of-dpu-hardware-strategies.pdf</a>, CV-AMD0015807.</p> |

**Exhibit A: Claim Chart for U.S. Patent 8,924,596**

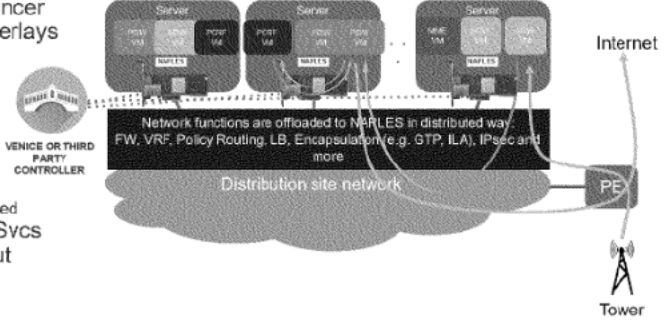
| Claim Language                                                                                          | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|---------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                         | <div> <p align="center"><b>Simplifying NFV for SP with Distributed Network Services</b></p> <ul style="list-style-type: none"> <li>• Pensando Solution <ul style="list-style-type: none"> <li>- Distributed Stateful L4 Firewall</li> <li>- Distributed Stateful L4 Load Balancer</li> <li>- Implementing routing/bridging/overlays <ul style="list-style-type: none"> <li>• Including GTP, ILA, VxLAN, SRv6</li> </ul> </li> <li>- Traffic encryption <ul style="list-style-type: none"> <li>• IPsec, TLS</li> </ul> </li> </ul> </li> <li>• Pensando Value <ul style="list-style-type: none"> <li>- Distributed consistent services <ul style="list-style-type: none"> <li>• Centrally reconfigurable, fully automated</li> </ul> </li> <li>- Scale-out Network and Security Svcs</li> <li>- Significant latency and throughput improvement</li> <li>- P4 programmable dataplane</li> <li>- CapEx and OpEx savings <ul style="list-style-type: none"> <li>• Network function consolidation</li> </ul> </li> </ul> </li> </ul>  <p align="center">VENICE OR THIRD PARTY CONTROLLER</p> <p align="center">Distribution site network</p> <p align="center">PE</p> <p align="center">Tower</p> <p align="center">Internet</p> <p align="right"><b>PENSANDO</b></p> <p align="center">© 2019 Pensando Confidential</p> </div> <p align="center">AMD-CV-0002236.</p> |
| <p>[1d] at least one second processing element in communication with said first processing element;</p> | <p>The Accused Products include at least one second processing element in communication with said first processing element.</p> <p>For example, AMD Pensando DSCs includes ARM cores and offloads (“Service Processing Offloads”) and accelerators), each of which are a “second processing unit,” and which are “in communication with the” first processing elements (including the processors in the P4 Packet Processing Dataplane, Packet Buffer, server processors and/or the host processors) via internal interconnects, PCIe interface, ethernet, and/or NVME-Over-</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

**Exhibit A: Claim Chart for U.S. Patent 8,924,596**

| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <p>Fabric. For another example, AMD Pensando DSCs include processors in the P4 Packet Processing Dataplane and Packet Buffer and in these processors are each a “second processing unit,” and are “in communication with the” first processing elements (including other processors in the P4 Packet Processing Dataplane and in the Packet Buffer as well as server processors and/or the host processors).</p> <div> <p><b>NVMeoF Offloading Support</b></p> <p>Host Interface</p> <p>(1) NVMe commands</p> <p>PCIe</p> <p>Memory</p> <p>Coherent Interconnect</p> <p>(2) NVMe commands translated into NVMeoF capsules</p> <p>P4 Packet Processing Dataplane</p> <p>ARM Cores</p> <p>Service Processing Offloads</p> <p>Packet Buffer Traffic Manager</p> <p>Ethernet Port</p> <p>Ethernet Port</p> <ul style="list-style-type: none"> <li>• Load balance across remote controllers</li> <li>• Encapsulation</li> <li>• TCP segmentation</li> </ul> </div> <p><a href="https://www.youtube.com/watch?v=in7athW-PaQ">https://www.youtube.com/watch?v=in7athW-PaQ</a>, CV-AMD0016269.</p> |

## Exhibit A: Claim Chart for U.S. Patent 8,924,596

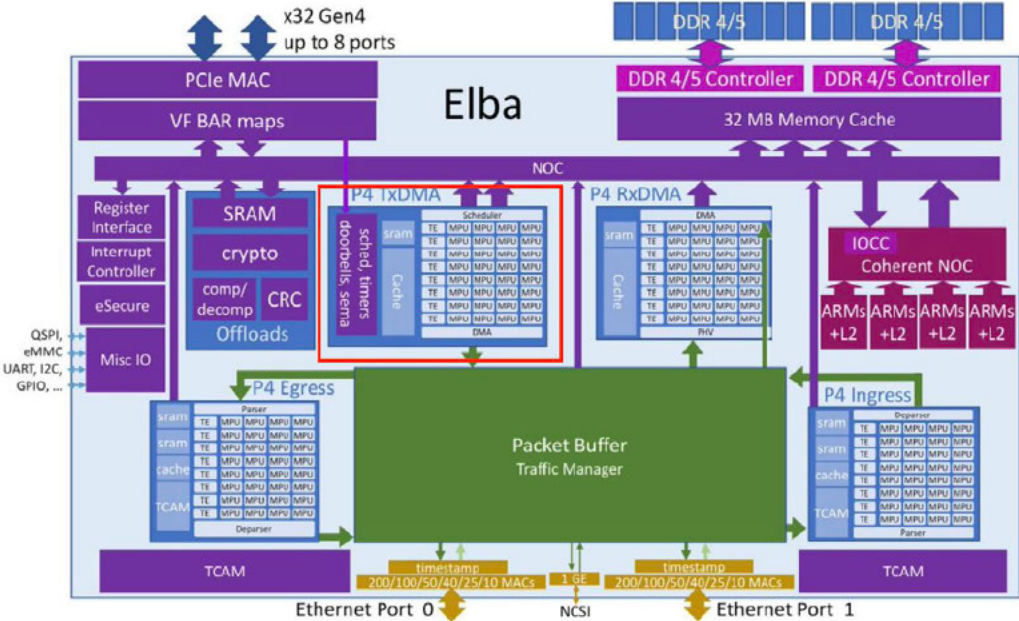
| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                               |
|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                |  <p style="text-align: center;"> <a href="https://www.servethehome.com/pensando-distributed-services-architecture-smartnic/">https://www.servethehome.com/pensando-distributed-services-architecture-smartnic/</a><br/> CV-AMD0016000. </p> |

**Exhibit A: Claim Chart for U.S. Patent 8,924,596**

| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <div><pre>graph TD     HI[Host Interface] &lt;--&gt; PCIe     PCIe &lt;--&gt; CI[Coherent Interconnect]     CI &lt;--&gt; P4[P4 Packet Processing Dataplane]     CI &lt;--&gt; AC[ARM Cores]     CI &lt;--&gt; SPO[Service Processing Offloads]     P4 &lt;--&gt; PTM[Packet Buffer Traffic Manager]     AC &lt;--&gt; PTM     SPO &lt;--&gt; PTM     PTM &lt;--&gt; EP1[Ethernet Port]     PTM &lt;--&gt; EP2[Ethernet Port]     EP1 &lt;--&gt; NI1[Network Interface]     EP2 &lt;--&gt; NI2[Network Interface]</pre></div> <p>Figure 2: Distributed Services Card Architecture.</p> <p><a href="https://opennetworking.org/news-and-events/blog/pensando-announces-p4-programmable-platform-and-joins-p4-community/">https://opennetworking.org/news-and-events/blog/pensando-announces-p4-programmable-platform-and-joins-p4-community/</a>, CV-AMD0016131.</p> |

**Exhibit A: Claim Chart for U.S. Patent 8,924,596**

| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <p>The number and organization of stages in various pipelines is key to ensure the capability of performing complex processing and versatility, respectively. If the number of stages that can be pipelined is not large enough for implementing a given functionality, packet recirculation is necessary, thus affecting achievable throughput. In the DSC, stages are organized in separate blocks of parallel pipelines. Since each pipeline has a maximum amount of packets per second it can process, the degree of parallelism in each block ensures wire rate operation capability. Different blocks can be dedicated to specific roles (such as input processing, output processing, etc.), as well as chained among themselves to create longer pipelines. Also, blocks can be chained with other processing modules (i.e., ARM Cores and Service Processing Offloads) to support more complex and efficient processing. As proven by the ability to execute various complex applications (including, but not limited to, SSL/TLS offload, NVMe-oF/TCP, stateful firewall) at wire speed, this design provides impressive scale and good granularity to alternate processing performed in a pipeline with processing performed by the other processing modules. Moreover, pipeline blocks can fetch and deliver packets from and to DSC memory, the host, and the Packet Buffer. In order to fully leverage the versatility of the specialized processors deployed in the pipeline and the tight integration with other components of the card, programming relies on an extension of the P4 language.</p> <p><a href="https://opennetworking.org/news-and-events/blog/pensando-announces-p4-programmable-platform-and-joins-p4-community/">https://opennetworking.org/news-and-events/blog/pensando-announces-p4-programmable-platform-and-joins-p4-community/</a>, CV-AMD0016131.</p> <p>ARM cores (an example of second processing elements) are connected to TE and MPUs (in that instance, examples of first processing elements) in the P4 processors via NOC or Coherent interconnect.</p> <p>The processors in the P4 DMA Pipelines (another example of second processing elements), second to the host interface (in that instance, another example of first processing elements) which it is communicative to via the Coherent Interconnect or NOC and the PCIe interface. Also, the processors in the P4 DMA Pipelines are an example of a second processing element, second to the P4 Ingress Pipeline (in that instance, another example of first processing elements) which it is communicative to via the Coherent Interconnect or NOC, and the central Packet Buffer.</p> |

# Exhibit A: Claim Chart for U.S. Patent 8,924,596

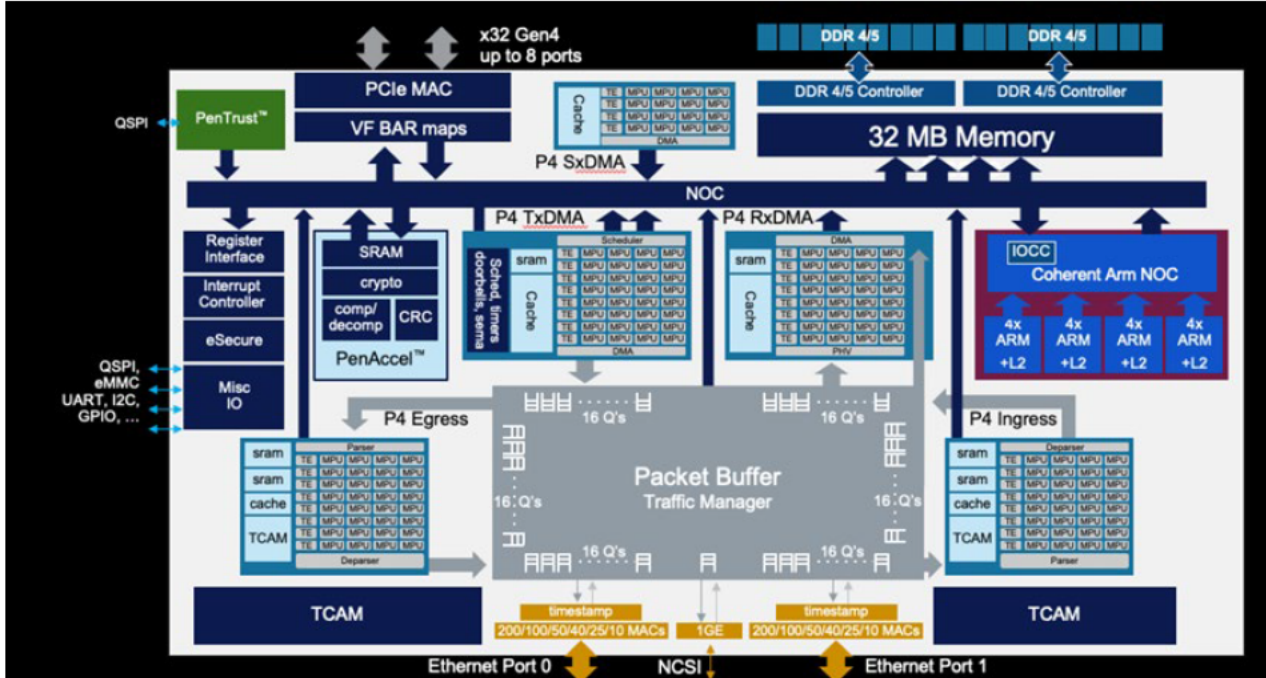
| Claim Language                                                                    | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                           |
|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                   |  <p><a href="https://www.amd.com/content/dam/amd/en/documents/pensando-technical-docs/white-papers/pensando-comparison-of-dpu-hardware-strategies.pdf">https://www.amd.com/content/dam/amd/en/documents/pensando-technical-docs/white-papers/pensando-comparison-of-dpu-hardware-strategies.pdf</a>, CV-AMD0015807.</p> |
| [1e] a reservation register implemented in hardware storing a value indicative of | The Accused Products have a reservation register implemented in hardware storing a value indicative of available space in said input queue, said reservation register is accessible by both said first processing element and said at least one second processing element.                                                                                                                                |

**Exhibit A: Claim Chart for U.S. Patent 8,924,596**

| <b>Claim Language</b>                                                                                                                                            | <b>Infringement Contentions and Exemplary Evidence of Infringement</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| available space in said input queue, said reservation register accessible by both said first processing element and said at least one second processing element; | AMD Pensando DSCs have a reservation register implemented in hardware to store a value indicative of available space in said input queue, for example, the “Register Interface,” “Scheduler,” “Doorbells” mechanism, and related functionality. The reservation register is implemented in hardware to enhance performance by optimizing the processor’s pipeline and resources, wherein the values are not accessible only by the originating software. The reservation register is accessible by both said first processing element and said at least one second processing element, for example, the ARM Cores, accelerators/offloads, P4 pipeline DMA engine processors, and Packet Buffer processors can access the register interface at least through the internal communications, for example NOC and Coherent Interconnect. The reservation register is accessible by the VM and host processors through the external communications between the DCSs and those processors, for example by PCIe interface, ethernet, and/or NVME-Over-Fabric. |

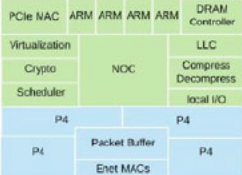
**Exhibit A: Claim Chart for U.S. Patent 8,924,596**

## Claim Language

## Infringement Contentions and Exemplary Evidence of Infringement

<https://www.servethehome.com/pensando-distributed-services-architecture-smartnic>, CV-AMD001600.

## Exhibit A: Claim Chart for U.S. Patent 8,924,596

| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <p style="text-align: center;">SOC, NOC, &amp; hardware queues</p> <hr/> <ul style="list-style-type: none"> <li>• Network On Chip (NOC) connects CPUs, memory, P4 DMA, and offload engines in a cache-coherent domain</li> <li>• ARM A-72 CPUs run SMP Linux, DPDK supported</li> <li>• P4 programs can push packet headers and data structures directly into ARM L2 caches or the last level system cache</li> <li>• Doorbells for <u>16 million hardware queues</u> are mapped to host or ARM processes, initiates <u>multi-level scheduler</u> to inject P4 pipeline tokens</li> </ul> <div style="text-align: right;">  </div> <p style="text-align: center;"><i>Hot Chips 32 Pensando SOC NOC And Hardware Queues</i></p> <p style="text-align: center;"><a href="https://www.servethehome.com/pensando-distributed-services-architecture-smartnic">https://www.servethehome.com/pensando-distributed-services-architecture-smartnic</a>,<br/>CV-AMD0016001.</p> |

## Exhibit A: Claim Chart for U.S. Patent 8,924,596

| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <p><b>New Constructs Required</b></p> <ul style="list-style-type: none"> <li>• Doorbell <ul style="list-style-type: none"> <li>◦ A register the driver can update to start a P4 program</li> <li>◦ A register a P4 program can update to notify completion</li> </ul> </li> <li>• DMA <ul style="list-style-type: none"> <li>◦ GSO <ul style="list-style-type: none"> <li>■ Copy header and segments to form multiple packets</li> </ul> </li> <li>◦ LRO <ul style="list-style-type: none"> <li>■ Copy payload from multiple packets to form a larger message</li> </ul> </li> </ul> </li> <li>• Timers</li> <li>• Stateful Memory <ul style="list-style-type: none"> <li>◦ To keep track of state</li> <li>◦ GSO : last segment offloaded; LRO : last segment received</li> </ul> </li> </ul> <p><small>© Systems, Inc. - All Rights Reserved</small> <span style="background-color: red; color: white; padding: 2px 5px; font-weight: bold;">PENSANDO</span></p> <p style="text-align: center;"><b>Use Cases for the Evolution of P4 and PSA in Programmable NICs by Mario Baldi and John Cruz, P4 Expert Roundtable Series (2020), CV-AMD0016429.</b></p> <p>All three processing modules (P4 Packet Processing Data Plane, ARM Cores, and Service Processing Offloads) can access the card Memory through a Coherent Interconnect. The Memory can also be mapped onto the PCIe space for I/O access from host software. Since the card Memory can be accessed by all processing modules, it can be used to keep state information required for stateful processing of packets, such as, for example, TCP offload. Moreover, it can be used to store full packets when their payload needs to be processed, which is key in application layer processing.</p> <p style="text-align: center;"><a href="https://opennetworking.org/news-and-events/blog/pensando-announces-p4-programmable-platform-and-joins-p4-community/">https://opennetworking.org/news-and-events/blog/pensando-announces-p4-programmable-platform-and-joins-p4-community/</a>, CV-AMD0016131.</p> |

**Exhibit A: Claim Chart for U.S. Patent 8,924,596**

| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <p><b>Doorbell</b></p> <ul style="list-style-type: none"><li>• P4 programs are traditionally triggered by an incoming packet on an interface</li><li>• Need capability to trigger P4 programs by driver after placing data in the TX descriptor ring</li><li>• Need capability to notify driver after appending an entry to the completion queue or RX descriptor ring</li></ul> <p>Required constructs:</p> <ul style="list-style-type: none"><li>• Start P4 program execution on doorbell</li><li>• Extern to ring doorbell</li></ul> <div><small> Pensando Systems, Inc. - All Rights Reserved</small></div> <div><b>PENSANDO</b></div> <p>Use Cases for the Evolution of P4 and PSA in Programmable NICs by Mario Baldi and John Cruz, P4 Expert Roundtable Series (2020), CV-AMD0016429.</p> |

**Exhibit A: Claim Chart for U.S. Patent 8,924,596**

| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <p>Events which enqueue new objects are signaled with a doorbell mechanism, allowing one or more objects to be added to any queue with a single doorbell action. Events which require processing in the future, such as TCP timers or activity checks, set hardware time markers for future scheduling. The queue scheduler organizes all 16 million queues into a DRAM array, tracking scheduling groups, interface groups, and COS groups. Priority scheduling, min/max data rates, and deficit weighted round robin scheduling are available across scheduling groups. When a queue is scheduled, a PHV token with the scheduled queue ID and COS is inserted into the assigned P4 pipeline for processing. The TE then accesses the qstate array, launching programs depending on queue type and state, which in turn fetch queued objects and descriptors as entries of tables in the P4 program.</p> <p>Michael Galles and Francis Matus, “Pensando Distributed Services Architecture” in Theme Article: Hot Chips (2021), CV-AMD0016136.</p> |

**Exhibit A: Claim Chart for U.S. Patent 8,924,596**

| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <p><b>Hardware Queue Management</b></p> <p>Packets which enter the P4 pipeline form the wire or which originate from internal events are placed in hardware queues. Hardware queues are used to manage interfaces, flows, connections, and any other objects which require ordered tracking and scheduling. Software can configure up to 16 million hardware queues (Figure 5). Each queue stores its current state in a DRAM-based qstate record, which includes a count of enqueued objects, pointers to arrays or linked lists of enqueued objects, connection state and peer information, and a process ID used for memory protection.</p> <p>Michael Galles and Francis Matus, “Pensando Distributed Services Architecture” in Theme Article: Hot Chips (2021), CV-AMD0016136.</p> <p>All three processing modules (P4 Packet Processing Data Plane, ARM Cores, and Service Processing Offloads) can access the card Memory through a Coherent Interconnect. The Memory can also be mapped onto the PCIe space for I/O access from host software. Since the card Memory can be accessed by all processing modules, it can be used to keep state information required for stateful processing of packets, such as, for example, TCP offload. Moreover, it can be used to store full packets when their payload needs to be processed, which is key in application layer processing.</p> <p><a href="https://opennetworking.org/news-and-events/blog/pensando-announces-p4-programmable-platform-and-joins-p4-community/">https://opennetworking.org/news-and-events/blog/pensando-announces-p4-programmable-platform-and-joins-p4-community/</a>, CV-ADM0016131.</p> |

**Exhibit A: Claim Chart for U.S. Patent 8,924,596**

| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <p>The MPU implements a domain-specific instruction set architecture with an emphasis on bit field manipulation and fast header updates. In particular, the MPU ISA focuses on rapid field extraction from multiple sources (tables, registers, or PHV) and forwards those fields directly to an ALU or straight to the PHV. MPU instruction types include register and field comparisons, branches, Boolean, and arithmetic ALU operations, and memory load and store operations. In addition to these familiar CPU instructions, the MPU includes PHV write operations, packet sequence number comparison and modification, queue state reduction, leading 0 and 1 detection, and other special protocol acceleration instructions. A general purpose, 64-bit-wide register file can be used to hold intermediate computational values, plus a domain-specific, 512-bit-wide table entry vector and a 512-bit-wide header field vector provide operands directly to ALU instructions.</p> <p><a href="https://sci-hub.se/downloads/2021-06-19/c1/galles2021.pdf">https://sci-hub.se/downloads/2021-06-19/c1/galles2021.pdf</a>, CV-ADM0016135.</p> |

**Exhibit A: Claim Chart for U.S. Patent 8,924,596**

| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <p><b>Writeback Table Fields</b></p> <ul style="list-style-type: none"><li>• Enable stateful processing</li><li>• E.g., stateful firewall with connection tracking</li><li>• In P4, table entries are read-only</li><li>• Register externs can be used to store state</li><li>• Indirection - additional stage required</li><li>• Limited resource</li><li>• Decreased code readability</li></ul> <p><i>Pensando processor supports writable table entries</i></p> <p><a href="https://opennetworking.org/wp-content/uploads/2020/11/2020-EuroP4-Mario-Baldi.pdf">https://opennetworking.org/wp-content/uploads/2020/11/2020-EuroP4-Mario-Baldi.pdf</a>, CV-AMD0016097.</p> |

**Exhibit A: Claim Chart for U.S. Patent 8,924,596**

| Claim Language | Infringement Contentions and Exemplary Evidence of Infringement                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
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|                | <p style="text-align: center;"><b>Hardware-assisted Functions</b></p> <ul style="list-style-type: none"><li>• SRAM controller can perform updates to table entries</li><li>• Before MPU starts processing them</li><li>• It can be used for read-modify-write operations</li></ul> <div style="display: flex; justify-content: space-around; align-items: center;"><div style="border: 1px solid black; background-color: red; color: white; padding: 10px; text-align: center; width: 100px;">Policer</div><div style="border: 1px solid black; background-color: darkblue; color: white; padding: 10px; text-align: center; width: 100px;">Counter</div></div> <ul style="list-style-type: none"><li>• Supported through <i>table properties</i></li></ul> <p><a href="https://opennetworking.org/wp-content/uploads/2020/11/2020-EuroP4-Mario-Baldi.pdf">https://opennetworking.org/wp-content/uploads/2020/11/2020-EuroP4-Mario-Baldi.pdf</a>, CV-AMD0016101.</p> <p>As an example, this reservation register can be a doorbell register stored on the accused product, that contains a p_index value. This stored value provides the producer index of the queue, which is indicative of available space in the input queue.</p> <p>Processing by the TxDMA P4+ pipeline is always triggered by the Scheduler mechanism. The scheduler selects a Queue for execution among those that have their corresponding scheduler bit set (//REV xref to scheduler description). Each QP has 2 scheduler bits, one for its Requester TX flow and one for its Responder TX flow. Whenever a Q has pending work, the corresponding scheduler bit is set. Upon scheduling into execution at the TxDMA P4+ pipeline, Requester TX flows are processed by the "Requester TX" P4+ program while Responder TX flows are processed by the "Responder TX" P4+ program.</p> <p>The setting of scheduler bits is done through the doorbell mechanism (//REV xref to doorbells). For both Requester TX flow and Responder TX flow the doorbell could be invoked by external or internal sources.</p> <p style="text-align: center;">AMD-CV-000055.</p> |