

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC. AND PENSANDO SYSTEMS, INC.,

Petitioners,

v.

CONCURRENT VENTURES, LLC AND XTREAMEDGE, INC.,

Patent Owners.

Case No. IPR2025-00478

U.S. Patent No. 8,924,596

**PATENT OWNERS' PRELIMINARY RESPONSE TO PETITION FOR
INTER PARTES REVIEW**

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PATENT OWNERS' EXHIBIT LIST

Exhibit	Description
2001	Text Order Denying AMD/Pensando's Motion to Stay Case (Judge Robert Pitman) in <i>Concurrent Ventures, LLC and XstreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)
2002	First Amended District Court Scheduling Order (Dkt. 77) in <i>Concurrent Ventures, LLC and XstreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)
2003	Webpage printouts of Docket Navigator Time to Trial regarding the District Court for the Western District of Texas and Judge Alan D. Albright
2004	Webpage printout of "AMD Reports Fourth Quarter and Full Year 2024 Financial Results" dated March 4, 2025 (https://ir.amd.com/news-events/press-releases/detail/1236/amd-reports-fourth-quarter-and-full-year-2024-financial-results)
2005	AMD/Pensando's Invalidity Contentions (Cover Pleading) in <i>Concurrent Ventures, LLC and XstreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)
2006	AMD/Pensando's Opening Claim Construction Brief in <i>Concurrent Ventures, LLC and XstreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)
2007	Declaration of Dr. R. Jacob Baker submitted by AMC/Pensando in support of AMD/Pensando's Opening Claim Construction Brief in <i>Concurrent Ventures, LLC and XstreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)
2008	Declaration of Darrell Long submitted by AMC/Pensando in support of AMD/Pensando's Opening Claim Construction Brief in <i>Concurrent Ventures, LLC and XstreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)

2009	Declaration of Bill Lin submitted by AMC/Pensando in support of AMD/Pensando's Opening Claim Construction Brief in <i>Concurrent Ventures, LLC and XtreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)
2010	Declaration of Kevin Jeffay submitted by AMC/Pensando in support of AMD/Pensando's Opening Claim Construction Brief in <i>Concurrent Ventures, LLC and XtreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)
2011	CV/XE's Responsive Claim Construction Brief in <i>Concurrent Ventures, LLC and XtreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)
2012	Declaration of Dr. Paul Min submitted by CV/XE in support of CV/XE's Responsive Claim Construction Brief in <i>Concurrent Ventures, LLC and XtreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)
2013	AMD/Pensando's Reply Claim Construction Brief in <i>Concurrent Ventures, LLC and XtreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)
2014	CV/XE's Objection to the Report and Recommendation of the U.S. Magistrate Judge in <i>Concurrent Ventures, LLC and XtreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)

Concurrent Ventures, LLC (“CV”) and XtreamEdge, Inc. (“XE”) (collectively “CV/XE” or “Patent Owners”) respectfully submit this Patent Owners’ Preliminary Response (POPR) to the Petition for *Inter Partes* Review (“IPR”) of U.S. Patent No. 8,924,596 (“the ’596 patent”) filed by Advanced Micro Devices, Inc. (“AMD”) and Pensando Systems, Inc. (“Pensando”) (collectively “AMD/Pensando” or “Petitioners”).

I. INTRODUCTION

Patent Owners submitted their Brief in Support of Patent Owners’ Request for Discretionary Denial of Institution of *Inter Partes* Review (Paper 6, “Discretionary Denial Brief”) on June 13, 2025. The Director and Board should deny institution of AMD/Pensando’s Petition against CV/XE’s ’596 patent for all the reasons stated therein—including Patent Owners’ settled expectations as to the validity of the ’596 patent, which issued almost 11 years ago and which, upon information and belief, at least one Petitioner has had actual knowledge of for a decade. Accordingly, the Board need not reach the merits of the Petition (except as relevant to the discretionary denial analysis). Even if the Board does reach the merits, however, institution should still be denied. As explained below, the Petition fails to identify how key claim terms should be construed and—to the extent the Petition can be understood to identify and apply a construction—fails to show that the prior art discloses those terms under that construction.

II. BACKGROUND

A. Overview of the '596 Patent

The inventors of the '596 patent identified a problem in the art of computer processing relating to “load distribution.” EX1001, 1:9-10. Specifically, “[i]n the prior art, the processing load (of a processing element) to determine what command to issue is relatively high.” *Id.*, 1:15-16. These high processing loads could be ameliorated in part by “partially or fully offload[ing] to a multiplicity of other processing elements (e.g. processors, processor cores, or custom processing circuitry),” but this created new problems with “synchronization...amongst the multiplicity of processing elements.” *Id.*, 1:17-25.

The prior art attempted to address the synchronization problem “using software techniques, such as semaphores and mutexes to a shared available space count variable in memory.” *Id.*, 1:25-27. These software techniques, however, “take[] additional processing time” and thus were “non-optimal,” particularly since “there may be a need to keep the time from command issue to execution minimized.” *Id.*, 1:27-32.

To address this problem in the art, the inventors of the '596 patent developed “a system for dividing and synchronizing a processing task across a plurality of processing elements” that utilized input and output queues and a reservation register

implemented in hardware, among other claim elements. *Id.*, 2:13-14. This innovation is reflected in the claims of the '596 patent.

B. The Claims of the '596 Patent

The language of independent claims 1, 7, and 13 of the '596 patent is reproduced below. For convenience, Patent Owners have included the limitation labels used by Petitioners.

Claim 1:

1[pre] A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

[1a] an input queue implemented in hardware;

[1b] an output queue implemented in hardware;

[1c] a first processing element having access to said input queue and said output queue;

[1d] at least one second processing element in communication with said first processing element;

[1e] a reservation register implemented in hardware storing a value indicative of available space in said input queue, said reservation register accessible by both said first processing element and said at least one second processing element;

[1f] computer storage storing instructions, which when executed by said at least one second processing element:

[1g] accesses said reservation register and reads said stored value;

[1h] determines when said read value indicates available space in said input queue for said first processing element to issue a command;

[1i] notifies said first processing element to issue said command to said input queue; and

[1j] wherein said first processing element receives notification from said at least one second processing element regarding issuing the command, issues said command to said input queue, and receives a response corresponding to said command from said output queue.

EX1001, claim 1; *see also* Pet., 92-93 (claim appendix).

Claim 7:

[7pre] A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

[7a] an input queue implemented in hardware;

[7b] an output queue implemented in hardware;

[7c] a first processing element having access to said input queue and said output queue;

[7d] at least one second processing element in communication with said input queue;

[7e] a reservation register implemented in hardware storing a value indicative of available space in said input queue, said reservation register accessible by both said first processing element and said at least one second processing element;

[7f] computer storage storing instructions, which when executed by said at least one second processing element:

[7g] receives a command from said first processing element;

[7h] accesses said reservation register and reads said stored value;

[7i] determines when said read value indicates available space in said input queue to issue said command;

[7j] issues said command to said input queue on behalf of said first processing element; and

[7k] wherein said first processing element receives a response corresponding to said command from said output queue.

EX1001, claim 7; *see also* Pet., 93-95 (claim appendix).

Claim 13:

13[pre] A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

- [13a] an input queue implemented in hardware;
- [13b] an output queue implemented in hardware;
- [13c] a first processing element having access to said input queue and said output queue;
- [13d] at least one second processing element in communication with said input queue and said output queue;
- [13e] a reservation register implemented in hardware storing a value indicative of available space in said input queue, said reservation register accessible by both said first processing element and said at least one second processing element;
- [13f] computer storage storing instructions, which when executed by said at least one second processing element:
 - [13g] receives a command from said first processing element;
 - [13h] accesses said reservation register and reads said stored value;
 - [13i] determines when said read value indicates available space in said input queue to issue said command;
 - [13j] issues said command to said input queue on behalf of said first processing element; and
 - [13k] receives a response corresponding to said command from said output queue.

EX1001, claim 13; *see also* Pet., 95-96 (claim appendix).

C. The Parallel Litigation

Patent Owners, CV/XE, are presently asserting the '596 patent in the following district court action: *Concurrent Ventures, LLC and XstreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.*, No. 1-24-cv-00335 (W.D. Tex. 2024).

D. The Petition's Principal Relied-Upon Prior Art References

1. U.S. Patent No. 8,559,439 ("Dongare") (EX1005)

Dongare is entitled "Method and Apparatus for Queue Ordering in a Multi-Engine Processing System." Dongare purports to disclose "[a] method and apparatus for queue-ordering commands in multi-engines, multi-queues and/or multi-flows environment." EX1005, Abstract. Dongare describes a buffer-based system in which "input queues," which Dongare describes as "sequentially ordered commands or segments to be processed by the plurality of engines," are "received and stored in input queue buffer[s]." EX1005, 5:3-12. Dongare is the primary reference used in Grounds 1 and 2.

2. U.S. Patent No. 8,051,227 ("Gewirtz") (EX1006)

Gewirtz is entitled "Programmable Queue Structures for Multiprocessors." Petitioner relies on Gewirtz primarily for its teachings regarding a "Queue State

Register.” Pet. 19-27. Petitioner uses Gewirtz as a secondary reference in Grounds 1 and 2.

3. U.S. Patent No. 7,398,528 (“Khawand”) (EX1008)

Khawand is entitled “Method And System For Efficient Multiprocessor Processing In A Mobile Wireless Communication Device.” Petitioner contends that Khawand teaches “a multiprocessor architecture that improves efficiency using delegation, queues, and flow control.” Pet., 44. Khawand is the primary reference for Grounds 3 and 4.

4. U.S. Patent No. 5,805,930 (“Rosenthal”) (EX1009)

Rosenthal is entitled “System for FIFO Informing the Availability of Stages to Store Commands Which Include Data and Virtual Address Sent Directly From Application Programs.” Petitioner relies on Rosenthal as a secondary reference in Grounds 3 and 4, principally for its teachings regarding FIFO methodologies. Pet. 57-60. Rosenthal was before the Patent Office during prosecution of the ’596 patent.

5. U.S. Patent No. 8,028,284 (“Ohkawa”) (EX1010)

Ohkawa is entitled “Data Processing System And Program For Transferring Data.” Petitioner relies on Ohkawa solely to supply the “output queue implemented in hardware” limitation in Ground 4. Pet. 74-79.

E. The IPR Petition’s Alleged Unpatentability Grounds

Grounds	Claims	Statutory Basis	Prior Art
1	1-2, 5-8, 11-14, 17-18	§103	Dongare in view of Gewirtz
2	7, 9-10	§103	Dongare in view of Gewirtz and Matsunami
3	1-2, 6-8, 12-14, 18	§103	Khawand in view of Rosenthal
4	1-2, 6-8, 12-14, 18	§103	Khawand in view of Rosenthal and Ohkawa
5	3-4, 9-10, 15-16	§103	Khawand in view of Rosenthal, Ohkawa, and Matsunami

F. Related IPR Matters

Petitioners have also filed three other petitions for *inter partes* review on three other patents asserted in the district court action: IPR2025-00223, IPR2025-00479, and IPR2025-00486.

III. CLAIM CONSTRUCTION

The claim construction portion of the Petition identifies one term that is subject to dispute in the district court litigation: “[input/output] queue implemented in hardware.”¹ Reproduced below is the totality of Petitioners’ discussion of this term in the claim construction section of the Petition:

¹ Patent Owners reserve the right to address the proper construction of this and other terms, and to address any substantive arguments provided by Petitioners, if this proceeding is instituted.

In district court, Petitioners proposed that these terms are “input/output queue implemented in physical circuits without software intervention.” The specification states: “the hardware will then automatically, **without software intervention**, update the reserved free space when the command is actually removed from the **queue for consumption**.” EX-1001, 4:43-46. This an example of how the ’596 patent explains what it means when it describes something as implemented in hardware. Ex-1003, ¶¶58-62.

PO proposed plain and ordinary meaning. Ex-1029, 000002.
Pet., 8-9 (emphasis in original).

Notably absent from this brief discussion is any statement as to what construction (or constructions) Petitioners are actually applying in the Petition. Also absent is any discussion of what the plain and ordinary meaning of the term is, much less how Petitioners’ district court construction differs from the plain meaning. As discussed in more detail below, this fails to satisfy Petitioners’ obligation to “identify...[h]ow the challenged claim is to be construed.” 37 CFR § 42.104(b)(3).

IV. PETITIONERS HAVE NOT SHOWN A REASONABLE LIKELIHOOD OF PREVAILING ON ANY CHALLENGED CLAIMS

A. All grounds fail because the Petition fails to meet its fundamental obligation to identify how the term “[input/output] queue implemented in hardware” should be construed.

As discussed above, in the “Claim Construction” section of the Petition, Petitioners note the existence of a live dispute as to the meaning of the terms

“[input/output] queue implemented in hardware” (limitations 1[a] and 1[b]).² Wholly absent from this discussion, however, is any statement identifying ***Petitioners’ position*** as to how the term should be construed or is being construed in the Petition. This is contrary to law.

PTAB regulations expressly require that an IPR petition “identify...[h]ow the challenged claim is to be construed.” 37 CFR § 42.104(b)(3). As the PTAB has stated, this express regulatory mandate “place[s] an affirmative burden on petitioners to set forth how the challenged claim is to be construed.” *OrthoPediatrics Corp. v. K2M, Inc.*, IPR2018-01548, Paper 9 at 10 (P.T.A.B. Mar. 1, 2019) (citation cleaned up; citing *Medicines Co. v. Mylan, Inc.*, 853 F.3d 1296, 1308 (Fed. Cir. 2017)). While this requirement does not necessitate “subjective agreement regarding correctness of its proffered claim constructions,” it does require that Petitioners actually identify the claim construction(s) that provide the basis for the Petition’s unpatentability theories. *W. Digital Corp. v. Spex Techs., Inc.*, No. IPR2018-00082, 2018 WL 1990246, at *5 (P.T.A.B. Apr. 25, 2018) (“Petitioner complies with our

² The terms “input queue implemented in hardware” and “output queue implemented in hardware” also appear in the other two independent claims (see limitations 7[a] and [7b] and limitations 13[a] and 13[b]) and thus appear in all challenged claims. Accordingly, Petitioners failure to meets its threshold obligation to identify how this term is to be construed dooms all grounds as to all claims.

rules by identifying claim constructions it proposes as the basis for requesting review of the challenged claims.”).

Here, Petitioners have not complied with this threshold requirement. Instead, they have done nothing more than identify, in truncated fashion, the parties’ competing district court positions as to the interpretation of key claims terms—without ever saying what claim construction or constructions they are adopting in this proceeding. Further muddying the waters, Petitioners also vaguely assert (without further explanation) that “[t]he Challenged Claims are invalid irrespective of whether these constructions are adopted.” Pet., 8. This vague and ambiguous approach to claim construction is deficient and lacks the particularity that PTAB regulations require. *See Tcl Commc’n Tech. Holdings Ltd. v. Dataquill Ltd.*, No. IPR2020-00746, 2020 WL 5592711, at *5 (P.T.A.B. Sept. 18, 2020) (stating that “[t]he Petition suffers various deficiencies with regard to claim construction” because “[o]n the one hand, Petitioner states that the claims need not be construed” yet “[o]n the other hand, Petitioner submits a table of terms with [district court] proposed constructions of various terms,” and holding that “Petitioner’s various failures as to claim construction contribute to our finding that the Petition lacks the requisite particularity to institute *inter partes* review”).

Petitioners’ attempts to map the prior art to the claim language do not change—and indeed confirm—the deficiencies of Petitioners’ claim construction

approach. When addressing limitations 1[a] and 1[b], Petitioner never expressly states what construction it is applying. *See* Pet. 14-17 (addressing limitations 1[a] and [b] for the Dongare/Gewirtz combination that underlies Grounds 1 and 2); 49-52 (addressing limitations 1[a] and [b] for the Khawand/Rosenthal combination that underlies Grounds 3-5); 74-75 (further addressing limitation 1[b] for Ground 4); 82-83 (relying on Ground 4 for all contentions regarding independent claims in Ground 5). To the extent its contentions can be understood to adopt any construction, moreover, they fail to show that proposed construction is met, as discussed below.

B. All grounds fail because Petitioners have not shown that the prior art discloses “[input/output] queue implemented in hardware” under any identified construction.

For each ground, when addressing limitations 1[a] and [1b], Petitioners include a conclusory, thinly supported statement suggesting that the limitations are satisfied under its own proposed district court construction that requires hardware

implementation “without software intervention.”³ Pet., 14-17; 49-52; 74-75.⁴ Thus, to the extent the Petition can be understood to adopt any construction, it is the narrow, negative construction Petitioners proffered in district court (“Petitioners’ District Court Construction”). The Petition does not come close, however, to showing that the art discloses Petitioners’ District Court Construction, which excludes any “software intervention” in the implementation of the “input queue” or “output queue.” Instead, for each reference that Petitioner uses to supply these limitations, Petitioner relies on generalized boilerplate statements—none of which are specific to input or output queues—that the disclosed system in general can be implemented in hardware or software.

The specific Grounds are discussed below. But ultimately, this discussion highlights the fundamental flaw with the Petition: it is insolubly unclear which

³ To be clear, Patent Owners do not adopt or concede the correctness of Petitioners’ District Court Construction, but merely discuss it here in light of Petitioners’ apparent application of it. Patent Owners show herein that the Petition does not have a reasonable likelihood of success on its own terms, under the construction it appears to apply. Patent Owners are not relying on Petitioners’ District Court Construction substantively to overcome the alleged prior art. Patent Owners explicitly state that they do not intend to surrender any claim scope falling outside of Petitioners’ District Court Construction.

⁴ For every Ground, Petitioners’ contentions for limitations 7[a] and 7[b] and 13[a] and 13[b] rely on Petitioners’ contentions for limitations 1[a] and 1[b] in that Ground. Pet. 37-39, 66, 70, 80, 82-83 (relying on Ground 4 for all contentions regarding independent claims in Ground 5). Accordingly, all of the analysis herein regarding limitations 1[a] and 1[b] applies equally to the Petitions contentions regarding limitations [a] and 7[b] and 13[a] and 13[b].

construction Petitioners applied. The closest Petitioners come to clearly identifying what they view as the proper claim construction is their implication that they applied Petitioners' District Court Construction. But the Petition does nothing to show that narrow construction is met. Nor does the Petition explicitly apply the plain and ordinary meaning of the term (i.e., not applying their own narrowed construction).⁵

Either way, the Petition fails: either Petitioners identified their own proposed construction as the proper claim construction—in which case they failed to show it was met—or they left it open what construction should apply—in which case they failed to identify the proper construction.

⁵ The closest Petitioners come is stating, for example, that “to the extent PO somehow argues that Dongare or Gerwitz use memory, PO alleged in district court that a queue implemented in memory using software is a queue implemented in hardware.” Pet. 16 (citing EX107, 000003-14), 17 (same). Petitioner includes an essentially identical statement in Ground 3. Pet. 50, 52. This unsupported characterization of an excerpt from Patent Owners' infringement contentions still does not identify *how Petitioner is interpreting the claims* and does not articulate an unpatentability theory. At the end of the day, the problem is the same: Petitioners do not identify what claim construction should apply. Moreover, it is Petitioner's burden to identify “with particularity, each claim challenged, the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge to each claim.” 35 U.S.C. § 312(a)(3). Simply declaring that Patent Owners' infringement contentions cover a particular configuration, without further analysis or expert support, cannot possibly meet this standard.

1. Grounds 1 and 2.

With respect to Grounds 1 and 2,⁶ for example, Petitioner states that “[t]he input queue is implemented in physical circuits, without software intervention, because Dongare teaches an implementation as a ‘hardware circuit.’” Pet., 15-16 (citing EX1005, 11:14-16, 2:55-58); *id.*, 17 (“The output queue is implemented in physical circuits, without software intervention, because Dongare teaches an implementation as a ‘hardware circuit.’” (citing EX1005, 11:14-16, 2:55-58)). The two brief passages of Dongare that Petitioners cite in support, however, say nothing about input queues. The first passage merely states that “elements of the multi-engine processing system 100 may be implemented as a software routine, hardware circuit, firmware, or a combination thereof.” EX1005, 11:14-16. And the second passage, apparently cited in error (although it is cited in multiple places) has no discernible relevance to the issue.⁷

None of this discloses Petitioners’ District Court Construction, which requires “input/output queue[s] implemented in physical circuits without software intervention” (which again, is relevant because that is the construction Petitioners’

⁶ Ground 2 relies exclusively on Ground 1 for its contentions regarding limitations 1[a] and 1[b].

⁷ The cited portion of Dongare covers several blank lines, the heading “Detailed Description,” and a fragment of the first sentence of Dongare’s discussion of the prior art. Patent Owners’ highlight the issue only because it is impossible to tell from context what portion of Dongare, if any, Petitioners intended to cite.

appear to apply). Pet. 8. The high-level language that Petitioner relies upon merely says that elements of the system may use software or hardware—it does not say that the input queue is implemented wholly without software intervention.⁸ In short, the Petition fails to make a threshold showing that Dongare discloses Petitioner’s proposed negative construction.

2. Grounds 3-5.⁹

The same is true of Petitioners’ contentions for the other grounds. In Ground 3, Petitioner relies on Khawand to supply the “input queue” limitation, and Rosenthal for its teachings regarding “hardware FIFO” methodology. Pet., 50. Petitioners’ only cited basis in Khawand for alleging that the alleged input queue is implemented “without software intervention” is—once again—a generic boilerplate statement that the disclosed systems can be implemented in either hardware or software. Pet. 50 (citing EX1008, 6:14-34); EX1008, 6:14-17 (“In light of the foregoing description, it should be recognized that embodiments in the present invention could be realized in hardware, software, or a combination of hardware and

⁸ Again, Patent Owners do not agree to or adopt Petitioners’ proposed “without software intervention” negative limitation, and are not substantively relying on it to overcome the alleged prior art. Instead, the issue is that, to the extent the Petition is applying that construction, it has not shown that it is disclosed by the art.

⁹ Ground 5 addresses only dependent claims and relies wholly on Ground 4 for its contentions regarding the independent claims. Pet. 82-83. Accordingly, it is not discussed independently herein.

software.”). As to Rosenthal, the cited language refers to a “hardware FIFO unit” but there is no indication from the cited language that this unit operates without software intervention. Nor does Petitioner explain how it could operate without software intervention.

Notably, Petitioner does not even contend that Khawand discloses the claimed *output* queue. Instead, in Ground 3, Petitioner relies on a European patent examiner’s statement about “common general knowledge” to supply the missing limitation. Pet. 51 (citing EX1004). Recognizing the frailty of this argument, in Ground 4, Petitioner provides a backup theory that relies upon Ohkawa to supply the missing limitation. Pet. 74-75. Once again, however, Petitioner’s only cited basis for asserting that Ohkawa’s alleged output queue is “implemented in physical circuits, without software intervention” is a generic statement that the described system and functions can be achieved through hardware or software. Pet. 74-75 (citing EX1010, 4:52-61). This does not come close to a disclosure of the narrow, negative limitation imposed by Petitioners’ District Court Construction, which requires a total absence of software intervention. Accordingly, for all of the foregoing reasons, Petitioner has failed to show that the prior art discloses limitations 1[a] and 1[b] under the only construction that it has even arguably adopted in the Petition.

V. CONCLUSION

For the foregoing reasons, to the extent the Director does not discretionarily deny the Petition and the Board reaches the merits, the Board should deny institution of the requested IPR.

Dated: July 15, 2025

By: /s/Michael Matulewicz-Crowley
Michael Matulewicz-Crowley
PTO Reg. No. 72,220

*Counsel for Patent Owners
Concurrent Ventures, LLC and
XtreamEdge, Inc.*

CERTIFICATE OF COMPLIANCE

The undersigned hereby certifies that CV/XE's Patent Owners' Preliminary Response to the Petition for IPR consists of 3,684 words, excluding the table of contents, table of authorities, certificate of service, this certificate of compliance, or table of exhibits. This Patent Owners' Preliminary Response to the Petition for IPR complies with the type-volume limitation of 14,000 words as mandated by the Memo. In preparing this certificate, counsel has relied on the word count of the word processing system used to prepare this paper (Microsoft Word).

Dated: July 15, 2025

By: /s/Michael Matulewicz-Crowley
Michael Matulewicz-Crowley
PTO Reg. No. 72,220

*Counsel for Patent Owners
Concurrent Ventures, LLC and
XtreamEdge, Inc.*

CERTIFICATE OF SERVICE

The undersigned hereby certifies that pursuant to 37 C.F.R. §42.6(e)(1), a copy of the foregoing **CV/XE's Patent Owners' Preliminary Response to the Petition for IPR** was served on July 15, 2025 by filing this document through the Patent Trial and Appeal Board's P-TACTS System as well as delivering a copy via electronic mail upon the following attorneys of record for Petitioners:

Dated: July 15, 2025

By: /s/Michael Matulewicz-Crowley
Michael Matulewicz-Crowley
PTO Reg. No. 72,220

*Counsel for Patent Owners
Concurrent Ventures, LLC and
XtreamEdge, Inc.*