

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC. and
PENSANDO SYSTEMS, INC.,
Petitioner,

v.

XTREAMEDGE, INC.,
Patent Owner.

IPR2025-00478
Patent 8,924,596 B1

Before KARL D. EASTHOM, JUSTIN T. ARBES, and
IFTIKHAR AHMED, *Administrative Patent Judges*.

AHMED, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Advanced Micro Devices, Inc. and Pensando Systems, Inc. (collectively, “Petitioner”) filed a Petition (Paper 2, “Pet.”) requesting *inter partes* review of claims 1–18 of U.S. Patent No. 8,924,596 B1 (Ex. 1001, “the ’596 patent”). XtreamEdge, Inc. (“Patent Owner”) filed a Preliminary Response (Paper 7, “Prelim. Resp.”). Patent Owner’s request for discretionary denial was denied and the Petition was referred to the Board. Paper 10.

We have authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2024). To institute an *inter partes* review, we must determine that the information presented in the Petition shows “a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). Based on the information presented in the Petition and the supporting evidence, we are persuaded that there is a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims. Accordingly, we institute an *inter partes* review of the challenged claims on the grounds set forth in the Petition.

B. *Real Parties in Interest*

Each party identifies itself as the real party in interest. Pet. 90; Paper 4, 2. Patent Owner also notes that “Concurrent Ventures, LLC is the exclusive licensee to U.S. Patent No. 8,924,596 and has all substantial rights to U.S. Patent No. 8,924,596.” Paper 4, 2.

C. Related Matters

The parties indicate that the '596 patent is the subject of *Concurrent Ventures, LLC and XtreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.*, No. 1:24-cv-00335 (W.D. Tex.) (“the district court case”). See Pet. 90; Paper 4, 2. Petitioner filed petitions challenging patents asserted in the district court case in IPR2025-00223, IPR2025-00479, and IPR2025-00486. Prelim. Resp. 9.

D. The '596 Patent

The '596 patent discloses a “System and Method for Dividing and Synchronizing a Processing Task Across Multiple Processing Elements/Processors in Hardware.” Ex. 1001, code (54). According to the '596 patent, the prior art offloaded high processing loads to a multiplicity of processing elements, but this solution was inadequate because it created a problem with synchronization amongst the processing elements, and using software techniques, such as semaphores and mutexes, to address this problem required additional processing time and was non-optimal. *Id.* at 1:15–29. The '596 patent purports to improve on those systems by “dividing and synchronizing a processing task across a plurality of processing elements” using input/output queues and a reservation register implemented in hardware. *Id.* at 2:13–20.

Figure 3 of the '596 patent is reproduced below.

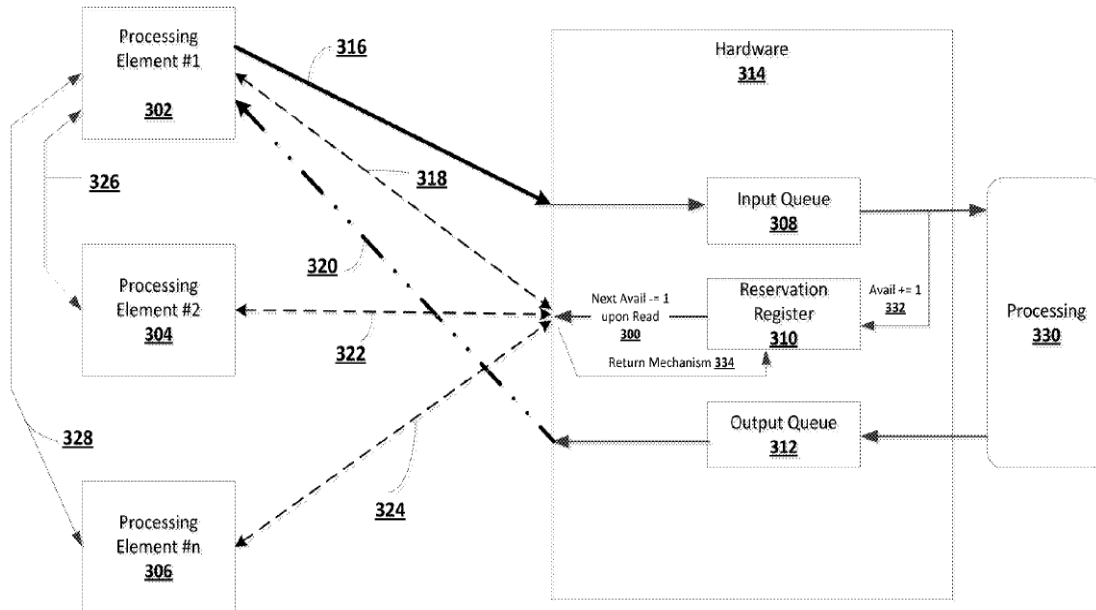


FIG. 3

Figure 3 depicts a system for dividing and synchronizing a processing task across a plurality of processing elements 302, 304, and 306, as well as input queue 308, register 310, and output queue 312 implemented in hardware, communicating with each other over various links. *Id.* at 2:50–52, 5:3–29. First processing element 302 accesses input queue 308 over communication link 316, output queue 312 over communication link 320, and second processing element 304 over communication link 326. *Id.* at 5:8–14. Reservation register 310 stores a value indicative of available space in input queue 308, and is accessible by both first processing element 302 over communication link 318 as well as by second processing element 304 over communication link 322. *Id.* at 5:23–29.

According to the '596 patent, computer storage stores instructions, which when executed by second processing element 304, accesses

reservation register 310 and reads the stored value. *Id.* at 5:29–33. “[T]he stored value [is] automatically decremented in hardware by 1 in concert with the read to make a reservation of space 300.” *Id.* at 5:33–35. The processing element “determines when the read value indicates available space in the input queue 308 for the first processing element 302 to issue a command,” and “notifies the first processing element 302 to issue the command to the input queue 308.” *Id.* at 5:35–39. First processing element 302 receives notification from one of processing elements 304, 306 “regarding issuing the command, issues the command to the input queue 308, and receives a response corresponding to the command from the output queue 312.” *Id.* at 5:39–45.

E. Illustrative Claim

Challenged claims 1, 7, and 13 of the ’596 patent are independent. Claims 2–6 depend from claim 1, claims 8–12 depend from claim 7, and claims 14–18 depend from claim 13. Claim 1 recites the following (with letter designations used in the Petition to refer to the various limitations):

1. [1pre] A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:

- [1a] an input queue implemented in hardware;
- [1b] an output queue implemented in hardware;
- [1c] a first processing element having access to said input queue and said output queue;
- [1d] at least one second processing element in communication with said first processing element;
- [1e] a reservation register implemented in hardware storing a value indicative of available space in said input queue, said reservation register accessible by both said first processing element and said at least one second processing element;

[1f] computer storage storing instructions, which when executed by said at least one second processing element:

[1g] accesses said reservation register and reads said stored value;

[1h] determines when said read value indicates available space in said input queue for said first processing element to issue a command;

[1i] notifies said first processing element to issue said command to said input queue; and

[1j] wherein said first processing element receives notification from said at least one second processing element regarding issuing the command, issues said command to said input queue, and receives a response corresponding to said command from said output queue.

F. Asserted Grounds of Unpatentability

Petitioner contends that the challenged claims are unpatentable as follows:¹

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 5–8, 11–14, 17, 18	103	Dongare, ² Gewirtz ³
3, 4, 9, 10, 15, 16	103	Dongare, Gewirtz, Matsunami ⁴
1, 2, 6–8, 12–14, 18	103	Khawand, ⁵ Rosenthal ⁶

¹ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. §§ 102, 103 effective March 16, 2013, which is before the ’596 patent’s effective filing date. *See* Ex. 1001, code (22). Therefore, the AIA version of § 103 applies.

² U.S. Patent No. 8,559,439 B1, issued Oct. 15, 2013 (Ex. 1005, “Dongare”).

³ U.S. Patent No. 8,051,227 B1, issued Nov. 1, 2011 (Ex. 1006, “Gewirtz”).

⁴ U.S. Patent No. 6,810,462 B2, issued Oct. 26, 2004 (Ex. 1007, “Matsunami”).

⁵ U.S. Patent No. 7,398,528 B2, issued July 8, 2008 (Ex. 1008, “Khawand”).

⁶ U.S. Patent No. 5,805,930, issued Sept. 8, 1998 (Ex. 1009, “Rosenthal”).

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 6–8, 12–14, 18	103	Khawand, Rosenthal, Ohkawa ⁷
3, 4, 9, 10, 15, 16	103	Khawand, Rosenthal, Ohkawa, Matsunami

II. ANALYSIS

A. Legal Standards – Obviousness

A claim is unpatentable if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. 35 U.S.C. § 103; *see KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations, including commercial success, long-felt but unsolved needs, failure of others, and unexpected results. *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17–18 (1966).

When evaluating a combination of teachings, we must also “determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). “[T]here must be some

⁷ U.S. Patent No. 8,028,284 B2, issued Sept. 27, 2011 (Ex. 1010, “Ohkawa”).

articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *Kahn*, 441 F.3d at 988. “[W]here a party argues a skilled artisan would have been motivated to combine references, it must show the artisan ‘would have had a reasonable expectation of success from doing so.’” *Arctic Cat Inc. v. Bombardier Recreational Prods. Inc.*, 876 F.3d 1350, 1360–61 (Fed. Cir. 2017) (quoting *In re Cyclobenzaprine Hydrochloride Extended-Release Capsule Patent Litig.*, 676 F.3d 1063, 1068–69 (Fed. Cir. 2012)).

B. Level of Ordinary Skill in the Art

We review Petitioner’s asserted obviousness grounds in view of the understanding of a person of ordinary skill in the art at the time of the invention. *Graham*, 383 U.S. at 17. The person of ordinary skill in the art is a hypothetical person who is presumed to have known the relevant art at the time of the invention. *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995).

Petitioner argues that at the time of the ’596 patent, a person of ordinary skill in the art would have had “a bachelor’s degree in electrical engineering, computer engineering, or comparable major with at least two years of experience in the field or a master’s degree in electrical engineering, computer engineering, or similar major with a specialization in the field,” where “[a] person with less education but more relevant practical experience may also meet this standard.” Pet. 8 (citing Ex. 1003 ¶¶ 55–57). Patent Owner does not address the level of ordinary skill in the art in its Preliminary Response. *See generally* Prelim. Resp.

We determine, on the current record, that Petitioner’s proposed level of ordinary skill is consistent with the ’596 patent and the asserted prior art.

See Okajima v. Bourdeau, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d at 1579. We adopt that level of ordinary skill in deciding whether to institute trial.

C. Claim Construction

In *inter partes* reviews, the Board interprets claim language using the same standard as the district courts, as described in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b) (2024). Under that standard, we generally give claim terms their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history. *See Phillips*, 415 F.3d at 1313–14.

1. [input/output] queue implemented in hardware

Petitioner notes that, in the district court case, Petitioner has proposed that the claim terms “[input/output] queue implemented in hardware” be construed as “input/output queue implemented in physical circuits without software intervention.” Pet. 8. In support of that construction, Petitioner points to the Specification’s statement that “the hardware will then automatically, without software intervention, update the reserved free space when the command is actually removed from the queue for consumption.” *Id.* at 8–9 (quoting Ex. 1001, 4:43–46) (emphasis omitted). According to Petitioner, “[t]his is an example of how the ’596 patent explains what it means when it describes something as implemented in hardware.” *Id.* at 9 (citing Ex. 1003 ¶¶ 58–62). Petitioner further notes that Patent Owner “proposed plain and ordinary meaning” for these terms in the district court case. *Id.* (citing Ex. 1029, 2). Petitioner contends that the “[c]hallenged

[c]laims are invalid irrespective of whether these constructions are adopted.”
Id. at 8.

Patent Owner argues that because Petitioner does not appear to be applying a specific construction for these terms in the Petition, Petitioner fails to satisfy its obligation to “identify . . . [h]ow the challenged claim is to be construed.” Prelim. Resp. 10 (citing 37 C.F.R. § 42.104(b)(3)). According to Patent Owner, Petitioner has “done nothing more than identify, in truncated fashion, the parties’ competing district court positions as to the interpretation of key claims terms—without ever saying what claim construction or constructions they are adopting in this proceeding.” *Id.* at 12. As a result, Patent Owner argues, the grounds asserted by Petitioner fail. *Id.* at 10–12.

Under the circumstances of this case and at this stage of the proceeding, we disagree with Patent Owner’s assertion that the applicable rules and guidance require Petitioner to do more. In pertinent part, Rule 42.104(b) requires that a petition set forth: “(3) How the challenged claim is to be construed. . . . [and] (4) How the construed claim is unpatentable.” 37 C.F.R. §§ 42.104(b)(3), (4). The Consolidated Trial Practice Guide⁸ explains:

If a petitioner *believes* that a claim term *requires an express construction*, the petitioner must include a statement identifying a proposed construction of the particular term and where the intrinsic and/or extrinsic evidence supports that meaning. On the

⁸ Consolidated Trial Practice Guide (November 2019), *available at* <https://www.uspto.gov/sites/default/files/documents/tpgnov.pdf>, hereinafter as “CTPG.”

other hand, a petitioner may include a statement that the claim terms require no express construction.

CTPG 44. Under the circumstances of this case, the applicable rule and our Practice Guide permit Petitioner to rely on the plain and ordinary meaning of these claim terms. After all, as Petitioner points out, that is the construction that Patent Owner proposes for these terms in the district court case.⁹ *See* Ex. 1029, 2. Moreover, Petitioner contends that even under Petitioner’s proposed construction from the district court case, the prior art teaches these claim limitations. Pet. 8, 15–17 (explaining how Dongare allegedly teaches implementation “in physical circuits, without software intervention”), 49–52 (similar arguments for Khawand and Rosenthal), 74–75 (similar arguments for Ohkawa). Because, as discussed below, we agree with Petitioner that, on the current record, Dongare teaches these claim limitations even under the construction that Petitioner proposes in the district court, we need not expressly construe these claim terms. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“Because we need only construe terms ‘that are in controversy, and *only to the extent necessary* to resolve the controversy,’ we need not construe [a particular claim limitation] where the construction is not ‘material to the . . . dispute.’” (citation omitted) (emphasis added)). If Patent Owner believes these terms should be construed differently, Patent Owner may propose a construction and identify where the intrinsic and/or extrinsic evidence supports its construction. *See* CTPG 44–45.

⁹ Patent Owner does not propose an express construction for these claim terms at this stage of this proceeding. *See generally* Prelim. Resp.

2. *Remaining Claim Terms*

On the present record, we do not discern a need to expressly construe any claim terms because doing so would have no effect on our analyses of Petitioner’s asserted grounds and will not assist in resolving the present controversy between the parties. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Obviousness Based on Dongare and Gewirtz

Petitioner contends that claims 1, 2, 5–8, 11–14, 17, and 18 are unpatentable over Dongare and Gewirtz under 35 U.S.C. § 103. Pet. 10–40 (Ground 1).

1. Dongare

Dongare discloses “queue ordering in a multi-engine processing system.” Ex. 1005, 1:16–17. Dongare states that in existing systems, “segments of one or more input streams are parallel processed in multiple processors to increase the processing efficiency or throughput of the system” but “out of order processing” may occur which results in “a loss of order in the sequence of the segments within the input stream and the resulting output stream may not correspond to the input stream.” *Id.* at 1:22–29. Dongare explains that this requires additional processing “to restore the order of the segments of the output stream relative to the input stream resulting in a compromise of the efficiencies gained by multi-processing.” *Id.* at 1:29–32. Dongare’s disclosed method includes “appending an identity

tag to the plurality of input segments in each input stream to produce a plurality of tagged input segments, the identity tag including information indicating the input stream and the relative order within the input stream of each of the plurality of input segments.” *Id.* at 1:43–48. The tagged input segments are assigned to “any one of the plurality of processing engines based on availability of the processing engines in the relative order of the tagged input segments within the respective input stream,” and a plurality of correspondingly tagged output segments are reordered to produce “output stream[s] having the same relative order as in the corresponding input stream.” *Id.* at 1:48–60.

Figure 1 of Dongare is reproduced below.

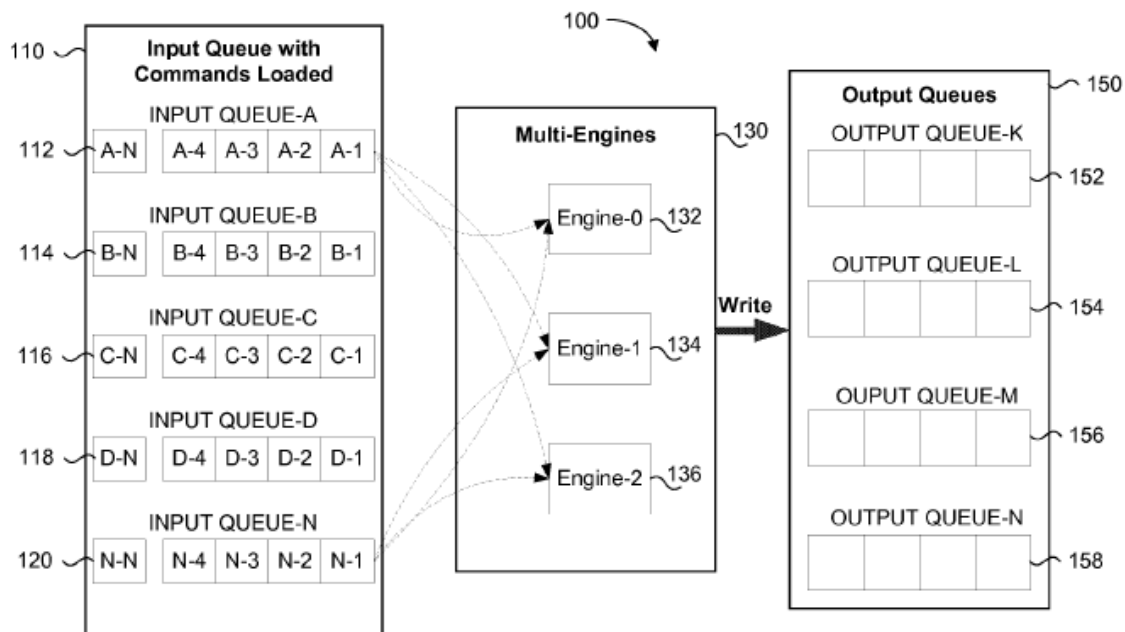


Figure 1 depicts a schematic representation of a multi-engine processing system. *Id.* at 2:38–39. Multi-engine processing system 100 is capable of handling a plurality of input queues or input streams 110, which are sequentially ordered commands or segments to be processed by the plurality of engines 130. *Id.* at 5:3–7. The processed commands are written out to

the plurality of output queues 150. *Id.* at 5:7–8. Dongare explains that “the elements of the multi-engine processing system 100 may be implemented as a software routine, hardware circuit, firmware, or a combination thereof.”

Id. at 11:14–16.

2. *Gewirtz*

Gewirtz, titled “Programmable Queue Structures for Multiprocessors,” discloses “a high performance hardware implementation is employed to manage logical queues with configuration registers which use queue element storage that is allocated in a normal memory.” Ex. 1006, code (54), 2:46–49. A state register or status register “holds the dynamic state of the queue, including a read pointer and a write pointer, queue occupancy, and/or number of free writeable entries for flow control purposes.” *Id.* at 2:59–62.

Figure 1 of Gewirtz is reproduced below.

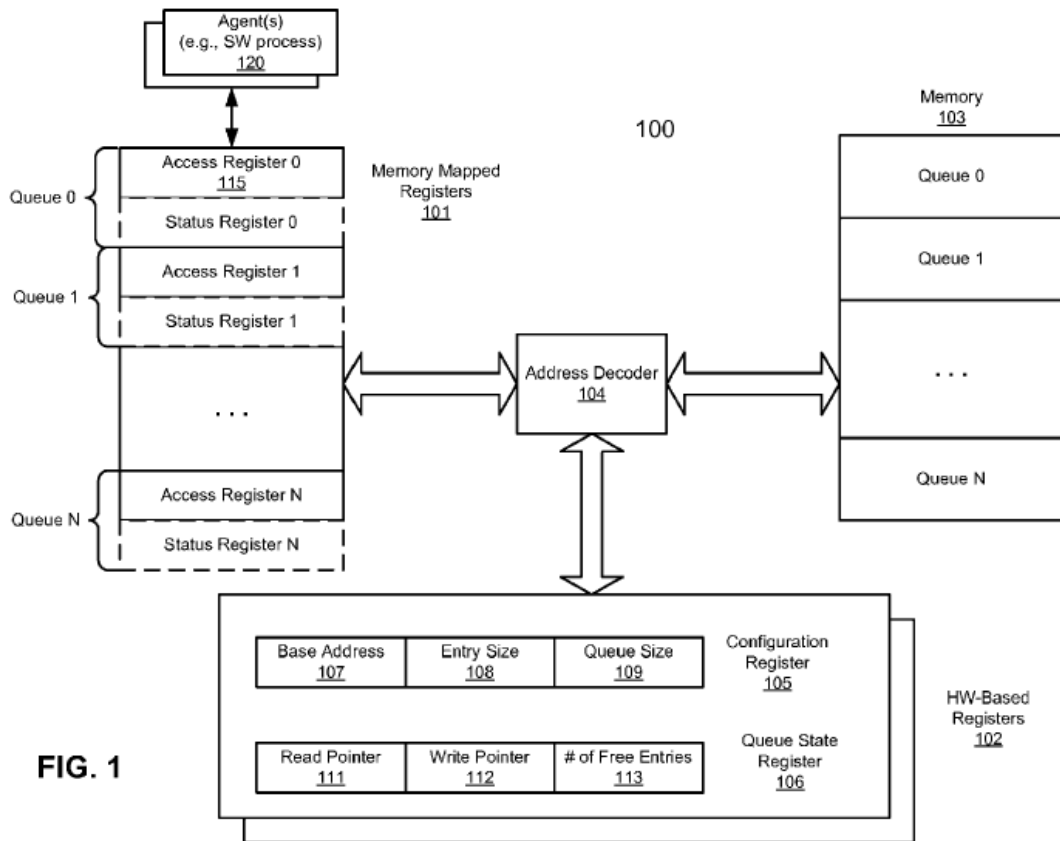


Figure 1 is a block diagram illustrating hardware-controlled queuing system 100. *Id.* at 3:8–9. System 100 includes memory mapped registers 101, hardware-based registers 102, and “a memory or memory section 103 (e.g., part of main memory) defining one or more queues (e.g., logical queues) coupled to each other via an address decoder 104.” *Id.* at 3:10–15. A programmable queue includes configuration register 105, queue state register 106, “storage that is allocated for the queue elements (e.g., corresponding memory segment of memory 103), and data access registers (e.g., corresponding memory mapped registers 101).” *Id.* at 3:43–47. Gewirtz explains that when a programmable queue is enabled and defined,

“agents 120 can perform reads and writes to the corresponding data access registers 101, which may cause queue operations to be performed atomically.” *Id.* at 4:16–20. This causes “the appropriate queue element to be read or written, and the queue state to be updated accordingly by hardware logic.” *Id.* at 4:20–22.

According to Gewirtz, “state register 106 includes an optional built-in credit counter represented by the number of free entries 113 which can be accessed via a status register of memory mapped registers 101 corresponding to the queue.” *Id.* at 4:51–54. “The credit counter originally contains the number of entries in the queue. When an agent wants to write an element into the queue, it first reads the reservation register to see if an entry is available.” *Id.* at 4:55–58.

3. *Claim 1*

Claim 1 recites a “system for dividing and synchronizing a processing task across a plurality of processing elements.” Ex. 1001, 11:25–51. In addition to the preamble, which Petitioner designates as element [1pre], claim 1 recites various limitations, which Petitioner designates as limitations [1a] through [1j]. We address each of these in turn.

(i) *Preamble [1pre]*

The preamble of claim 1 recites, “[a] system for dividing and synchronizing a processing task across a plurality of processing elements.” Ex. 1001, 11:25–26. Petitioner contends that Dongare teaches that multiple engines or processors are used to increase the throughput of a device or a network system as well as dividing processing tasks to enable parallel execution across a plurality of redundant array of independent disks (“RAID”) engines, and then synchronizing the output as necessary to

account for out-of-order execution. Pet. 12–14 (citing Ex. 1005, 1:21–32, 4:49–55, 14:31–55, Fig. 7; Ex. 1003 ¶ 83).

Patent Owner does not specifically respond to these arguments. *See* Prelim. Resp. Based on our review of the current record, at this stage of the proceeding, we determine that the information presented sufficiently supports Petitioner’s contentions relating to the preamble of claim 1.¹⁰

- (ii) *Limitation [1a]: an input queue implemented in hardware*
Limitation [1b]: an output queue implemented in hardware

Petitioner contends that Dongare teaches these limitations. Pet. 14–16. With regard to an input queue, Petitioner contends that Dongare teaches input queues in the RAID application-specific integrated circuit (ASIC) for holding commands from the host to the processing engines. *Id.* at 14 (citing Ex. 1005, 14:30–34, 5:3–36, 14:39–42; Ex. 1003 ¶¶ 84–87). Petitioner further contends Dongare teaches implementation of input queues as a “hardware circuit.” *Id.* at 15–16 (citing Ex. 1005, 11:14–16).

Similarly, with regard to an output queue, Petitioner contends that Dongare teaches at least one output queue in the RAID ASIC for processed commands. Pet. 16–17 (citing Ex. 1005, 5:3–20, 14:30–42, 14:46–49; Ex. 1003 ¶¶ 92–94). Petitioner contends Dongare teaches implementation of output queues as a “hardware circuit.” *Id.* at 17 (citing Ex. 1005, 11:14–16; Ex. 1003 ¶¶ 95, 97–98). As discussed above (*supra* section II.C.1), Petitioner contends that Dongare teaches these limitations under the plain and ordinary meaning of the claim limitations as well as under the

¹⁰ At this stage in the proceeding, we do not decide whether the preamble of claim 1 is limiting.

construction proposed by Petitioner in the district court: “input/output queue implemented in physical circuits without software intervention.” Pet. 8.

Patent Owner responds that Dongare does not teach limitations [1a] and [1b]. Prelim. Resp. 13–17. Patent Owner argues that Petitioner “relies on generalized boilerplate statements—none of which are specific to input or output queues—that the disclosed system in general can be implemented in hardware or software.” *Id.* at 14. Patent Owner argues that Petitioner’s cited portion of Dongare merely states “elements of the multi-engine processing system 100 may be implemented as a software routine, hardware circuit, firmware, or a combination thereof.” *Id.* at 16 (citing Ex. 1005, 11:14–16).¹¹ Patent Owner argues that this “high-level language that Petitioner relies upon merely says that elements of the system may use software or hardware—it does not say that the input queue is implemented wholly without software intervention.” *Id.* at 16–17. As such, Patent Owner argues, “the Petition fails to make a threshold showing that Dongare discloses Petitioner’s proposed negative construction.” *Id.* at 17.

Based on the current record and for the purposes of institution, Dongare sufficiently teaches limitations [1a] and [1b].

¹¹ Patent Owner also points out that another portion of Dongare cited by Petitioner is “apparently cited in error . . . [and] has no discernible relevance to the issue.” Prelim. Resp. 16 & n.7 (citing Ex. 1005, 2:55–58). We agree with Patent Owner that this citation appears to be incorrect.

Figure 7 of Dongare is reproduced below.

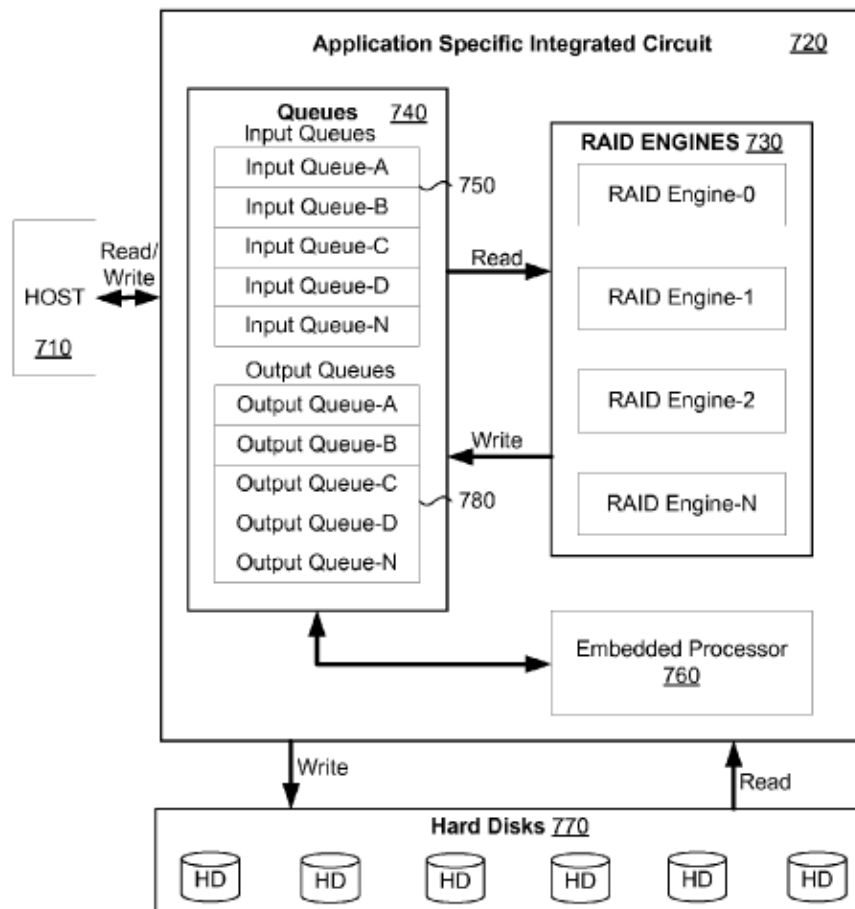


Figure 7 provides an illustration of an application of the apparatus of Figure 5 (not reproduced) in a multi-engine processing system. Ex. 1005, 14:30–31. As Petitioner points out, Dongare teaches input queues in the RAID Application Specific Integrated Circuit (“ASIC”). Pet. 14 (citing Ex. 1005, 14:30–34, 14:39–42). Dongare discloses that in “RAID controllers, the Host computer 710 is connected to a RAID ASIC 720 via a PCIe protocol bus,” and “[t]he queues 740 in the controller are classified as input queues 750 from the Host, and output queues from the RAID engines 730.” Ex. 1005, 14:33–36, 14:39–41. Dongare therefore discloses input/output queue[s] implemented as part of an Application Specific

Integrated Circuit. Dongare further discloses that the elements of its multi-engine processing system “may be implemented as a software routine, *hardware circuit*, firmware, or a combination thereof.” *Id.* at 11:14–16 (emphasis added).¹² Petitioner’s declarant, Samuel Russ, Ph.D., testifies that this disclosure “teaches implementing the input [and output] queues as hardware.” Ex. 1003 ¶¶ 88, 95. For the purposes of institution, we find Dr. Russ’s testimony supports Petitioner’s contentions, and determine that Dongare teaches these claim limitations under their plain and ordinary meaning as well as under the construction proposed by Petitioner in the district court.

(iii) *Limitation [1c]: a first processing element having access to said input queue and said output queue*

Petitioner contends that Dongare teaches this limitation. Pet. 17–18. Petitioner contends that “[t]he host processor is connected to the RAID ASIC using PCIe . . . and has access to the input queue because it writes commands to the input queues.” *Id.* at 17 (citing Ex. 1005, 14:31–34, 14:37–42; Ex. 1003 ¶¶ 99–100). Petitioner further contends that “Dongare’s host processor accesses the output queue, for example by reading the output queue, after it is signaled by the embedded processor that the host’s

¹² Patent Owner argues that Petitioner relies on “generalized boilerplate statements” and “high-level language” that does not specifically refer to the queues. Prelim. Resp. 14, 17. Patent Owner, however, does not explain why an ordinarily skilled artisan would have understood Dongare’s reference to an implementation in a *hardware circuit* as insufficient to teach the claimed queues. Moreover, Patent Owner does not address the specific disclosure of the RAID ASIC, i.e., integrated circuits, that Petitioner further relies on as teaching the claim limitations. See Pet. 14–15 (citing Ex. 1005, 14:30–34, 14:39–42, Fig. 7).

command has been completed.” *Id.* (citing Ex. 1005, 14:46–54, Fig. 7; Ex. 1003 ¶¶ 101–102).

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review of the current record, at this stage of the proceeding, we determine that the information presented sufficiently supports Petitioner’s assertions as to this limitation.

(iv) *Limitation [1d]: at least one second processing element in communication with said first processing element*

Petitioner contends that Dongare teaches this limitation. Pet. 18. Petitioner contends that Dongare’s “embedded processor communicates with the host processor over PCIe, using input and output queues,” and “signals and interrupts the host by writing to the outbound queue.” *Id.* (citing Ex. 1005, 14:31–44, 4:52–55, Fig. 7; Ex. 1003 ¶¶ 103–106).

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review of the current record, at this stage of the proceeding, we determine that the information presented sufficiently supports Petitioner’s assertions as to this limitation.

(v) *Limitation [1e]: a reservation register implemented in hardware storing a value indicative of available space in said input queue, said reservation register accessible by both said first processing element and said at least one second processing element*

Petitioner contends that the combination of Dongare and Gewirtz teaches this limitation. Pet. 19–24. Petitioner contends that Dongare’s embedded processor manages the input queues, e.g., through queue handling/scheduling, but Dongare leaves out implementation details. *Id.* at 19 (citing Ex. 1005, 10:50–11:30, Fig. 7; Ex. 1003 ¶¶ 101–102). Petitioner contends Gewirtz teaches queue management, including a queue

state register, which is “a reservation register that stores a value indicative of available space in the input queue (e.g., [the number] of free entries).” *Id.* (citing Ex. 1006, 2:59–64, 3:55–59, 4:5–15, 4:51–5:6; Ex. 1003 ¶¶ 107–108). Petitioner contends that Gewirtz discloses that the register is a hardware-based register, and on a successful read of the register, hardware auto-decrements the “available reservation count.” *Id.* at 20–22 (citing Ex. 1006, 1:30–64, 2:59–64, 4:5–15, 4:51–5:6, 6:18–25, 6:66–7:6, Fig. 1; Ex. 1003 ¶¶ 109–112). Petitioner contends that Gewirtz also teaches that the register is accessible by software agents running on multiple processor cores. *Id.* at 22 (citing Ex. 1006, 4:56–61; Ex. 1003 ¶ 113). Petitioner argues that a person of ordinary skill in the art would have understood from Gewirtz’s teaching, that the queue state register is accessible to Dongare’s host/embedded processors, because Gewirtz teaches it as a memory-mapped register. *Id.* at 22–24 (citing Ex. 1006, 3:10–27, 4:51–54, 4:51–54; Ex. 1003 ¶ 114).

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review of the current record, at this stage of the proceeding, we determine that the information presented sufficiently supports Petitioner’s assertions as to this limitation.

(vi) *Limitation [1f]: computer storage storing instructions, which when executed by said at least one second processing element*

Petitioner contends that both Dongare and Gewirtz teach this limitation. Pet. 27–28 (citing Ex. 1005, 15:27–47; Ex. 1006, 11:40–53, 11:14–16; Ex. 1003 ¶¶ 126–129). Petitioner argues that Dongare teaches using a computer program stored in a machine-readable medium, and given

how processors have worked, it would have been obvious for Dongare's embedded processor to access computer storage storing instructions. *Id.*

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review of the current record, at this stage of the proceeding, we determine that the information presented sufficiently supports Petitioner's assertions as to this limitation.

(vii) *Limitation [lg]: accesses said reservation register and reads said stored value*

Petitioner contends that the combination of Dongare and Gewirtz teaches this limitation. Pet. 28–30. Petitioner contends that Dongare's embedded processor manages the input queues. *Id.* at 28 (citing Ex. 1005, 10:50–11:30, 14:30–55, Figs. 5, 7). Petitioner contends that Gewirtz's queue status register contains the “available entries for reservation,” which enables a processor to track available space. *Id.* at 29 (citing Ex. 1006, 4:5–7; Ex. 1003 ¶¶ 130–131). Petitioner further contends that the combination of Dongare with Gewirtz teaches Dongare's embedded processor managing the input queue by first reading the number of available entries for reservation from the queue status register. *Id.* (citing Ex. 1005, 14:46–54, Fig. 7; Ex. 1006, 4:12–13; Ex. 1003 ¶¶ 101–102). Petitioner argues that it would have been obvious for Dongare's embedded processor to monitor the queue states via the reservation register and notify the host processor when there is space available for additional commands. *Id.* at 29–30 (citing Ex. 1006, 4:12–13, 4:56–58; Ex. 1003 ¶¶ 131–132).

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review of the current record, at this

stage of the proceeding, we determine that the information presented sufficiently supports Petitioner's assertions as to this limitation.

(viii) Limitation [1h]: determines when said read value indicates available space in said input queue for said first processing element to issue a command

Petitioner contends that the combination of Dongare and Gewirtz teaches this limitation. Pet. 30–31. Petitioner contends that Gewirtz teaches that, before entries are written to the queue, a processor “first reads the reservation register to see if an entry is available.” *Id.* at 30 (citing Ex. 1006, 4:12–13, 4:56–64; Ex. 1003 ¶¶ 133–134). In the proposed combination, Petitioner contends, it would have been obvious for Dongare's embedded processor to read the queue status register for the input queue and determine whether the reservation field indicates available space for a command to be issued. *Id.* at 30–31 (citing Ex. 1005, 14:30–55; Ex. 1006, 2:64–66; Ex. 1003 ¶ 135).

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review of the current record, at this stage of the proceeding, we determine that the information presented sufficiently supports Petitioner's assertions as to this limitation.

(ix) Limitation [1i]: notifies said first processing element to issue said command to said input queue

Petitioner contends that the combination of Dongare and Gewirtz teaches this limitation. Pet. 31–34. Petitioner contends that Dongare's embedded processor reads the reservation register and notifies the host processor when space is available for additional commands to be issued, and the host processor then writes the commands to the input queue. *Id.* at 31 (citing Ex. 1005, 14:41–49; Ex. 1003 ¶¶ 138–39). Petitioner further

contends that Gewirtz's queues generate interrupts to a programmable target based on queue status/events, including when queue space is available. *Id.* at 32 (citing Ex. 1006, 3:63–4:2). Petitioner contends that, in its proposed combination, Dongare's embedded processor notifies the host of space available in the input queue over the PCIe bus or by generating an interrupt to the host. *Id.* at 33 (citing Ex. 1005, 14:30–34, 14:52–55; Ex. 1006, 3:63–4:2; Ex. 1011, 10:3–26, 11:52–54; Ex. 1003 ¶¶ 141–142).

Petitioner contends that Gewirtz teaches that when an input queue is full, the embedded processor notifies the host after the input queue drains below a predetermined threshold, and the host processor can then issue commands to the input queue. *Id.* (citing Ex. 1006, 3:63–4:2, 14:41–42). Petitioner contends that the “combination of Dongare and Gewirtz takes advantage of Gewirtz's teachings to monitor queue status and leverages Dongare's embedded processor to notify the host processor of queue space availability.” *Id.* at 34 (citing Ex. 1003 ¶¶ 143–44).

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review of the current record, at this stage of the proceeding, we determine that the information presented sufficiently supports Petitioner's assertions as to this limitation.

(x) *Limitation [1j]: wherein said first processing element receives notification from said at least one second processing element regarding issuing the command, issues said command to said input queue, and receives a response corresponding to said command from said output queue.*

Petitioner contends that Dongare teaches this limitation. Pet. 17–18. Petitioner contends that Dongare discloses that after its host receives a notification that space is available in an input queue, the host issues

commands to the input queue. *Id.* (citing Ex. 1005, 14:41–42, 14:46–49; Ex. 1003 ¶¶ 145–146). Petitioner contends that Dongare also teaches that its embedded processor signals the host when the RAID engines have finished processing a command and the output is available in the output queue corresponding to the command from the output queue. *Id.* at 34–35 (citing Ex. 1005, 14:35–37, 14:41–42, 14:46–55). Petitioner further contends that Dongare discloses that the host processor then reads the output queue over the PCIe bus to receive the response corresponding to the command it submitted. *Id.* at 35 (citing Ex. 1005, 14:31–39; Ex. 1003 ¶¶ 148–149).

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review of the current record, at this stage of the proceeding, we determine that the information presented sufficiently supports Petitioner’s assertions as to this limitation.

(xi) *Motivation to Combine Dongare and Gewirtz*

Petitioner argues that a person of ordinary skill in the art would have been motivated to combine Dongare and Gewirtz because Dongare’s system uses many input and output queues, and Gewirtz teaches queue-management techniques for tracking queue space and flow control. Pet. 24–27 (citing Ex. 1005, 10:50–11:30; Ex. 1006, 1:12–35, 2:46–3:7, 4:16–50; Ex. 1003 ¶¶ 115–125). Petitioner contends that Dongare’s architecture creates a need for synchronization and flow control with its queues as tasks are scheduled and divided among multiple processing engines. *Id.* at 24–25 (citing Ex. 1005, code (57), 6:6–35, 6:28–42, 7:34–39; Ex. 1003 ¶ 116). According to Petitioner, Gewirtz teaches a queue management solution, including a register optimized for queue flow control, to this common problem of

variable-rate data flows. *Id.* at 25 (citing Ex. 1006, 2:46–3:7, 3:32–42, 8:7–17; Ex. 1003 ¶ 117).

Petitioner contends that a person of ordinary skill in the art would have been motivated to apply Gewirtz’s teachings to Dongare’s architecture. *Id.* Petitioner argues that “Gewirtz’s teachings provide several known benefits, including atomic hardware operations to avoid software spin locks . . . and flow control using a register,” and that “Gewirtz’s teachings prevent queue overflow and increase throughput/efficiency.” *Id.* at 25–26 (citing Ex. 1006, 1:30–64, 4:49–61, 6:8–7:14, 6:66–7:14; Ex. 1003 ¶¶ 118–120).

Petitioner also argues that a person of ordinary skill in the art would have had a reasonable expectation of success in combining the teachings of Dongare and Gewirtz because it would have been a straightforward application of known techniques and routine technologies like registers, queue management, and flow control to improve Dongare’s architecture. *Id.* at 26–27 (citing Ex. 1006, 1:12–35, 2:46–3:7, 4:16–50; Ex. 1003 ¶¶ 122–123).

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review of the current record, at this stage of the proceeding, we determine that Petitioner provides an adequate reason why one of ordinary skill in the art would have combined the teachings of Dongare and Gewirtz in the manner asserted by Petitioner, with a reasonable expectation of success.

(xii) *Summary as to Claim 1*

For the reasons discussed above with regard to claim 1, we determine that the information presented supports sufficiently, for purposes of institution, Petitioner’s assertions as to claim 1.

(xiii) Objective Indicia of Nonobviousness

In the record presently before us, neither Petitioner nor Patent Owner has presented any evidence of objective indicia of nonobviousness.

(xiv) Weighing the Graham Factors

“Once all relevant facts are found, the ultimate legal determination [of obviousness] involves the weighing of the fact findings to conclude whether the claimed combination would have been obvious to an ordinary artisan.” *Arctic Cat*, 876 F.3d at 1361. On balance, considering the record presently before us, Petitioner has established a reasonable likelihood that it would prevail in showing that the combination of Dongare and Gewirtz would have rendered the subject matter of claim 1 of the ’596 patent obvious to one of ordinary skill in the art at the time of the invention.

4. Independent Claims 7 and 13 and Dependent Claims 2, 5, 6, 8, 11, 12, 14, 17, and 18

Independent claims 7 and 13 recite limitations similar to those in claim 1. Ex. 1001, 11:64–12:21, 12:34–58. For these limitations, Petitioner relies on its contentions as to claim 1, discussed above. Pet. 37–40 (citing Ex. 1003 ¶¶ 161–164, 168–169, 173–74, 179, 183–186, 191–196). Petitioner contends that Dongare also teaches the additional limitations recited in claims 7 and 13. *Id.* at 38–40 (citing Ex. 1003 ¶¶ 165–167, 170–172, 175–178, 187–190, 197–199).

Claims 2, 5, and 6 depend from claim 1; claims 8, 11, and 12 depend from claim 7; and claims 14, 17, and 18 depend from claim 13. *See* Ex. 1001, 11:52–13:3. Each of claims 2, 8 and 14 recites, “wherein said input queue is a first-in-first-out (FIFO) buffer.” *Id.* Each of claims 5, 11, and 17 recites, “wherein said stored value is decremented by a predefined

value prior to returning said stored value to said at least one second processing element.” *Id.* Each of claims 6, 12, and 18 recites, “wherein at least one third processing element executes said command and notifies said output queue to issue said response.” *Id.* Petitioner contends that either Dongare or Gewirtz teach each of these limitations. Pet. 35–37 (citing Ex. 1003 ¶¶ 151–160).

Patent Owner does not specifically respond to Petitioner’s contentions as to these claims. *See generally* Prelim. Resp.

Based on our review of the current record, at this stage of the proceeding, we determine that Petitioner has established a reasonable likelihood that it would prevail in showing that the combination of Dongare and Gewirtz would have rendered the subject matter of claims 2, 5–8, 11–14, 17, and 18 of the ’596 patent obvious to one of ordinary skill in the art at the time of the invention.

E. Obviousness Based on Dongare, Gewirtz, and Matsunami

Petitioner contends that claims 3, 4, 9, 10, 15, and 16 are unpatentable over Dongare, Gewirtz, and Matsunami under 35 U.S.C. § 103. Pet. 40–44 (Ground 2).

1. Matsunami

Matsunami is titled “Storage System and Method Using Interface Control Devices of Different Types,” and discloses a system wherein “interface controllers of a plurality of types may include a block I/O interface controller having functions of a [storage area network (SAN)] and a file I/O interface controller having functions of a [network attached storage (NAS)].” Ex. 1007, 2:49–52.

2. *Claims 3, 4, 9, 10, 15, and 16*

Claims 3 and 4 depend from claim 1, claims 9 and 10 depend from claim 7, and claims 15 and 16 depend from claim 13. Ex. 1001, 11:54–57, 12:24–27, 12:61–64. Each of claims 3, 9, and 15 recites, “wherein said system is part of a storage area network (SAN) controller.” *Id.* Each of claims 4, 10, and 16 recites, “wherein said system is part of a network attached storage (NAS) controller.” *Id.*

Petitioner contends that Matsunami teaches the use of SAN/NAS controllers and using RAID for storage, and that it would have been obvious “to use RAID teachings from the Dongare-Gewirtz combination as part of Matsunami’s SAN/NAS controller.” Pet. 41–43 (citing Ex. 1007, code (57), 1:18–23, 1:30–34, 2:1–4, 2:13–27, 3:42–47, 3:66–4:20, 6:29–47, 7:1–17, Fig. 1; Ex. 1005, 14:30–55, Fig. 7; Ex. 1003 ¶¶ 209–213, 222–223). Petitioner further contends that a person of ordinary skill in the art would have been motivated to use Matsunami’s SAN/NAS teachings with Dongare’s RAID architecture because this would have been “a simple combination of prior art elements according to known methods to yield predictable results (a SAN/NAS storage controller using RAID).” *Id.* at 43–44 (citing Ex. 1003 ¶¶ 214–220).

Patent Owner does not separately address Petitioner’s showing for these claims. *See* Prelim. Resp. 16 (combining its arguments for Petitioner’s Grounds 1 and 2).

Based on our review and consideration of the current record, including the above disclosure of Matsunami, at this stage of the proceeding, we determine that Petitioner has established a reasonable likelihood that it would prevail in showing that Dongare, Gewirtz, and Matsunami would

have rendered the subject matter of claims 3, 4, 9, 10, 15, and 16 of the '596 patent obvious to one of ordinary skill in the art at the time of the invention.

*F. Obviousness Based on Khawand and Rosenthal;
Obviousness Based on Khawand, Rosenthal, and Ohkawa;
and Obviousness Based on Khawand, Rosenthal, Ohkawa,
and Matsunami*

Petitioner contends that claims 1, 2, 6–8, 12–14, and 18 would have been obvious over Khawand and Rosenthal. Pet. 44–72 (Ground 3). Petitioner also contends that claims 1–2, 6–8, 12–14, and 18 would have been obvious over Khawand, Rosenthal, and Ohkawa. Pet. 72–82 (Ground 4). Petitioner contends that claims 3, 4, 9, 10, 15, and 16 would have been obvious over Khawand, Rosenthal, Ohkawa, and Matsunami. Pet. 82–87 (Ground 5).

Patent Owner responds that Petitioner has failed to show that the prior art asserted in Grounds 3–5 discloses limitations 1[a] and 1[b] under the construction that Petitioner proposes in the district court. Prelim. Resp. 17–18.

Because we have determined above that, at this stage of the proceeding and on the present record, the information presented in the Petition shows that there is a reasonable likelihood that Petitioner will prevail with respect to its challenges based on Dongare, Gewirtz, and Matsunami (Grounds 1 and 2), we need not address, in this Decision, Petitioner's additional challenges (Grounds 3–5). *See* 35 U.S.C. § 314(a); *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1356 (2018) (“Section 314(a) does not require the Director to evaluate every claim individually. Instead, it simply requires him to decide whether the petitioner is likely to succeed on

‘at least 1’ claim. Once that single claim threshold is satisfied, it doesn’t matter whether the petitioner is likely to prevail on any *additional* claims; the Director need not even consider any other claim before instituting review”); 37 C.F.R. § 42.108(a).

III. CONCLUSION

Based on the arguments and evidence presented by the parties, we conclude that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to at least one claim of the ’596 patent challenged in the Petition. Our analysis is based on the preliminary record developed thus far and may change after the record is developed fully, during trial.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review is instituted for claims 1–18 of the ’596 patent on the unpatentability grounds asserted in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which commences on the entry date of this Decision.

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