

Invalidity of the '596 Patent by Rosenthal '930 and Other Prior Art

The asserted claims of U.S. Patent No. 8,924,596 are anticipated and/or rendered obvious in view of US5805930A ("Rosenthal '930") alone or in combination with knowledge of one of skill in the art or other prior art.

This claim chart is based on Defendants' present understanding of the asserted claims, Plaintiffs' vague and overbroad infringement contentions (and corresponding, implicit claim constructions), and Defendants' investigation to date. Defendants are not adopting Plaintiffs' apparent constructions, nor are Defendants admitting to the correctness of any particular construction. Defendants reserve all rights to amend this invalidity claim chart in light of any claim construction developments or any amendments to Plaintiffs' infringement contentions. Further, as discovery is ongoing and Defendants continue to seek discovery from third parties regarding the references identified in Defendants' invalidity contentions as well as other potential prior art, Defendants reserve the right to amend or supplement this claim chart in connection with Defendants' continuing investigation. At a minimum, Defendants intend to revise these invalidity contentions as appropriate based on discovery from third parties as discovery progresses.

The claim chart below identifies where each limitation of each asserted claim of the '596 patent can be found in Rosenthal '930. This analysis is based on Plaintiff's interpretation of the claims as indicated in their Infringement Contentions. The citations provided below are exemplary, rather than exhaustive, and Defendants reserve the right to rely upon any other portion of the cited references.

Claim Language	Exemplary Evidence of Anticipation and/or Obviousness
[1pre] A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:	<p>To the extent the preamble is considered a claim limitation, Rosenthal '930 teaches "[a] system for dividing and synchronizing a processing task across a plurality of processing elements," including at least the following exemplary citations.</p> <p>For example, Rosenthal '930 teaches a system for dividing and synchronizing processing tasks by disclosing, as non-limiting examples, a digital system with multiple parallel FIFO buffers for application programs that divide and synchronize a processing task. <i>See, e.g.:</i></p> <p>"A digital system which uses an arrangement of one or more parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available." Rosenthal '930 at Abstract.</p>

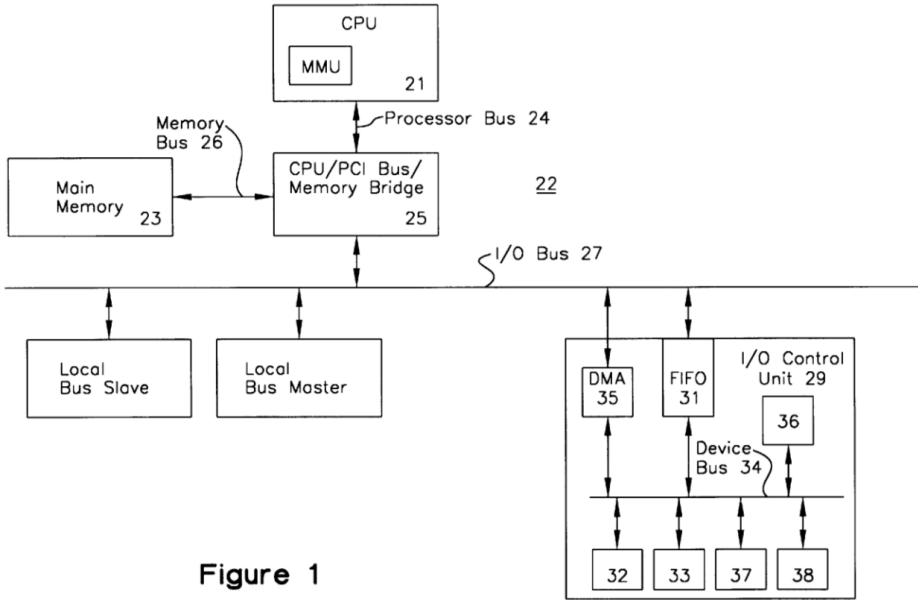
Claim Language	Exemplary Evidence of Anticipation and/or Obviousness
	<p style="text-align: center;">Figure 1</p> <p>Rosenthal '930 at Figure 1.</p> <p>“Since any practical input/output device will have limited FIFO buffer storage for holding data written to it over the input/output bus, any architecture for input/output devices must include some technique for controlling the flow of data so that this storage is not exhausted.</p> <p>It is desirable to provide a means for providing flow control for a computer system or similar system utilizing FIFO buffers to receive data so that the operation may proceed as rapidly as possible without loss of data.”</p> <p>Rosenthal '930 at col. 1, l. 66 – col. 2, l. 7.</p> <p>“It is another object of the present invention to provide a flow control system for an architecture which utilizes FIFO buffers for buffering write operations.</p> <p>These and other objects of the present invention are realized in a system which uses an arrangement of parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the central processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register</p>

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	<p>tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal ’930 at col. 2, ll. 15–33.</p> <p>“FIG. 1 is a block diagram of a computer system 22 which has been devised to overcome the problems of the prior art. The system 22 provides a new input/output architecture which cooperates with other components of present systems based on the PDP11 architecture, runs legacy code for those systems, yet is able to drastically increase the speed of input/output operations for new application programs. In order to accomplish this, the new architecture of the system allows read and write operations by application programs to be made directly to the input/output devices. This eliminates the cumbersome multi-step software processes invoked by prior art systems using the operating system and trusted code for every input/output access. In order to accomplish the process safely, the input/output architecture of the system 22 utilizes an input/output control unit 29 which provides its own virtual name-to-physical-device and context translation for all of the input/output devices associated with the new control unit 29 on its own device bus 34. By enforcing this translation, application programs can write directly to input/output devices without affecting assets of other application programs. Once this translation from virtual names furnished by the application programs to physical input/output devices on the device bus is accomplished and context has been furnished to the input/output devices, translation of addresses of input/output devices on the input/output bus into physical addresses on the device bus 34 is accomplished directly by hardware at the input/output control unit 29. This hardware also checks permissions; and, when an operation is known to be safe, it is performed by hardware. When a translation operation fails, the operating system software is invoked. Thus, rather than trapping every input/output operation to determine whether it is safe as is done in prior art computer systems based on the PDP11 architecture, the system 22 traps and sends to operating system software only unsafe operations allowing hardware to accomplish most translations and greatly speeding the access of input/output devices.” Rosenthal ’930 at col. 3, ll. 29–65.</p> <p>“Although the input/output architecture of system 22 may be used with systems utilizing a single input/output bus for all operations, the preferred embodiment of system 22 functions as well in a system utilizing a local bus 27 such as the Peripheral Component Interconnect (PCI) bus or the Video Electronics Standards Association (VESA) local bus which may be associated with other input/output buses. While the discussion of this specification will assume that bus 27 is a local bus, the local bus 27 is also referred to in this specification as the input/output bus 27 in order to emphasize its use. In arrangements utilizing local buses, the central processing unit 21 and main memory 23 are typically arranged on a processor bus 24 and a memory bus 26, respectively, and are joined to a bridge unit 25. The central processing unit 21 typically</p>

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	<p>includes a memory management unit. The bridge unit 25 provides write buffering for operations between the central processing unit 21 and the input/output bus 27, between the central processing unit 21 and main memory 23 on the processor bus 24 and the memory bus 26, and between the input/output bus 27 and main memory 23.” Rosenthal ’930 at col. 4, ll. 28–48.</p> <p>“Those skilled in the art will recognize that the use of 128 individual FIFO buffers 39 to receive commands written by the central processing unit is very expensive and probably not economically feasible for use with personal computers. In addition, it is expensive of system resources for an operating system to context switch the central processing unit from one application program to another. Thus, the operating system will try to ensure that once an application is given the central processing unit the application will retain control long enough to amortize the cost of the context switch. This means that typically in a one processor system at most one FIFO buffer will be active at a time. In a multi-processor system, typically at most as many FIFO buffers will be active as there are processors.” Rosenthal ’930 at col. 21, ll. 39–52.</p> <p>“One embodiment of the new architecture provides a means for attaining almost the same speed as is possible with 128 FIFO buffers but much more economically. Instead of 128 individual FIFO buffers 39, the described embodiment utilizes a smaller number of FIFO buffers 39 than the number of areas into which the input/output address space may be divided and thus the number of application programs which may be run. Utilizing a smaller number of FIFO buffers causes each FIFO buffer to function as a cache for commands which may be sent by any of the application programs. In the preferred embodiment, one FIFO buffer 39 is used for each processor which may be writing to the input/output control unit 29. For example, if the computer utilizes two processors arranged as symmetrical multi-processors, then two individual FIFO buffers are utilized. If, as is usually the case, only a single central processing unit is used, then a single FIFO buffer 39 may in the limit act as a cache for commands from all application programs which may be running on the central processing unit. Such an arrangement is illustrated in FIG. 6. Of course, in either case more FIFO buffers might be used.” Rosenthal ’930 at col. 21, l. 53 – col. 22, l. 6.</p>
<p>[1a] an input queue implemented in hardware;</p>	<p>Rosenthal ’930 teaches “an input queue implemented in hardware,” including at least the following exemplary citations.</p> <p>For example, Rosenthal ’930 teaches an input queue implemented in hardware, by disclosing, as non-limiting examples, FIFO queue for storing operations.</p> <p>Defendants have proposed a construction that “queue implemented in hardware” means “queue implemented in physical circuits without software intervention.” The input queue in Rosenthal ’930 meets Defendants’</p>

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	<p>construction because, for example, Rosenthal '930 teaches a hardware implementation of its teachings, which includes its teachings of queues. <i>See, e.g.</i>, Rosenthal '930 at 5:24–27 (“The control unit 29 includes a hardware FIFO unit 31 for receiving incoming commands addressed to the input/output devices on a device bus 34.”). <i>See, e.g.</i>:</p> <p>“A digital system which uses an arrangement of one or more parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available.” Rosenthal '930 at Abstract.</p>  <p style="text-align: center;">Figure 1 Rosenthal '930 at Figure 1.</p>

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	<div data-bbox="583 259 1459 820"><p>The diagram illustrates a system architecture. At the top, a horizontal line represents Bus 27. Below it, a large rectangular block represents the Input/Output Control Unit 29. Inside this unit, there is a 'Decode' block 30 connected to Bus 27. Below 'Decode' is a 'Pusher' block 53. To the left of the Pusher is a block containing 'MMU 50' and 'DMA 35'. Below the Pusher is a large grid-like structure with various numbered cells (7, 3, 11, 32, 39, 40, 45, etc.). To the right of this grid is a 'Resource Manager' block (dashed outline) and a 'Translation Table' block 38. Below the main unit, a horizontal line represents Bus 34. Connected to Bus 34 are three blocks: 'Disk Controller 32', 'Graphics Output Controller Memory 33', and 'Sound Generator 37'. Arrows indicate data flow between these components and the buses.</p></div> <p data-bbox="945 824 1071 857">Figure 3</p> <p data-bbox="583 860 934 893">Rosenthal '930 at Figure 3.</p>

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	<div data-bbox="583 261 1459 816"><p>The diagram illustrates a system architecture centered around an Input/Output Control Unit 29. At the top, a Decode block 30 is connected to Bus 27. Below it, a Pusher block 53 is connected to Bus 27 and a central processing area. This central area contains a grid of blocks labeled 3, 11, and 32, with a vertical stack of blocks labeled 7 and 36. To the left, an MMU block 50 contains a sub-block 52, and a DMA block 35 is connected to it. To the right, a Resource Manager block is connected to a Translation Table block 38. Below the central area, a Disk Controller 32, a Graphics Output Controller Memory 33, and a Sound Generator 37 are connected to Bus 34. A Translation Table block 38 is also connected to Bus 34. Various other blocks like 42, 45, 49, and 40 are shown with their respective connections.</p></div> <p data-bbox="949 824 1073 857">Figure 6</p> <p data-bbox="583 862 932 894">Rosenthal '930 at Figure 6.</p>

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	<p style="text-align: center;">Figure 7 Rosenthal '930 at Figure 7.</p> <p>“It is another object of the present invention to provide a flow control system for an architecture which utilizes FIFO buffers for buffering write operations.</p> <p>These and other objects of the present invention are realized in a system which uses an arrangement of parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the central processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal '930 at col. 2, ll. 15–33.</p> <p>“The architecture of the system 22 has been designed so that it eliminates almost all read operations of input/output devices by the central processing unit. In order to accomplish this, the input/output control unit 29 includes a first-in first-out (FIFO) unit 31 for storing write operations directed to the input/output control</p>

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	<p>unit. The FIFO unit 31 queues incoming write operations. Unlike FIFO units in prior art systems, it stores both addresses and data. This allows the write operations to the input/output control unit 29 to occur asynchronously so that both the central processing unit 21 and the input/output control unit 29 may be functioning independently of one another and neither need wait for operations of the other.” Rosenthal ’930 at col. 3, l. 66 – col. 4, l. 11.</p> <p>“In the architecture of system 22, an input/output control unit 29 is shown joined to the input/output bus 27. The control unit 29 includes a hardware FIFO unit 31 for receiving incoming commands addressed to the input/output devices on a device bus 34.” Rosenthal ’930 at col. 4, ll. 60–64.</p> <p>“In one embodiment, the FIFO unit 31 includes a plurality of FIFO buffers 39 (see FIG. 3). When an application program desires to write to an input/output device on the device bus 34, it addresses that device. Decoding circuitry decodes the address by reviewing a number of the highest order bits decoded by the chip sufficient to indicate a unique portion of the input/output address space assigned to an application program and places the command in the appropriate FIFO buffer 39 for that application program. Each FIFO buffer 39 handles commands only from the application program to which the address area has been mapped. An arrangement using a smaller number of FIFO buffers 39 than one buffer for each application program (as few as a single buffer 39) could also be utilized as long as the address of the FIFO buffer is mapped to only one application program at a time.” Rosenthal ’930 at col. 5, ll. 51–66.</p> <p>“The unit 29 receives physical addresses furnished by the memory management unit and virtual names furnished by application programs for operations to be performed which have been sent to the FIFO unit 31 and controls the translation of those virtual names for all input/output devices. The hardware unit 29 includes the device bus 34 to which the individual input/output devices such as a disk controller 32, a graphics output controller 33, and a sound generator 37 are shown joined. The unit 29 also includes a DMA unit 35 which is adapted to transfer data between the individual input/output devices and main memory for use by the central processing unit or other components of the system.” Rosenthal ’930 at col. 5, l. 67 – col. 6, l. 10.</p> <p>“Because the amount of space in each of the FIFO buffers is limited to thirty-two entries in the embodiment being described (and will be limited to some finite number in any embodiment), it is possible for a buffer 39 to fill with data and be unable to take more commands directed to the particular area. As discussed previously, this will occur when the central processing unit is writing a FIFO buffer 39 faster than the input/output control unit 29 is able to handle the commands placed in the FIFO unit 31. In such a case, the input/output control unit 29 issues a hold command on the bus 27 to stop additional commands from being sent by the application program. During the holdoff period, the puller circuit 40 may empty some of the</p>

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	<p>commands of the application program from the FIFO buffer 39 so that space will be available. Alternatively, when the bus holdoff expires, commands from the program may still fill the FIFO buffer 39; and the new commands may have to be otherwise dealt with or the data will be lost to the input/output control unit 29.” Rosenthal ’930 at col. 16, ll. 14–32.</p> <p>“In one embodiment of the new architecture, a flow control register 45 is included for each FIFO buffer 39 of the input/output control unit 29. The register 45 stores an indication of the number of available spaces for commands in the associated FIFO buffer 39. The use of this flow control register 45 allows a requirement to be placed on an application program attempting an access of the input/output control unit 29 that it first determine whether space is available in the FIFO unit 31 before it writes any command. Before writing any data, the application program must determine the amount of "free" space to which it may write. This it does by having the central processing unit read the value in the flow control register 45 associated with the FIFO buffer 39 being utilized. Once this value has been read, the application program may send up to that amount of data before it need test again to determine whether free space remains to which it may send more data.” Rosenthal ’930 at col. 16, ll. 33–49.</p> <p>“In one embodiment of the new architecture the individual buffers 39 are implemented utilizing an array of random access memory (RAM). In such an arrangement, the data comprising the commands is placed in the RAM and pointers are utilized to define the positions of the beginning and end of the individual FIFO buffers 39 and the beginning and end of the data. In such an embodiment, a simple subtraction of a pointer designating the last data placed in a particular RAM buffer from the pointer designating the end of the buffer provides the value to be held by the flow control register. In such a case, the flow control register itself may be a logical register whose contents are computed whenever it is read.” Rosenthal ’930 at col. 16, l. 58 – col. 17, l. 3.</p> <p>“The use of the flow control register 45 allows an application program presently using the resources of the input/output control unit 29 to proceed without causing the overflow of the FIFO unit 31. Whenever the application has written commands totaling the amount previously read from the register 45, it must read the register again. This is especially useful for application programs which may wish to transfer a series of commands in sequence, possibly using the burst transfer mode of operation provided by many of the modern buses. By ascertaining the space available in the FIFO buffer 39 before transferring a sequence of commands, the application can know that sufficient space will be available for the operation. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal ’930 at col. 17, ll. 4–18.</p>

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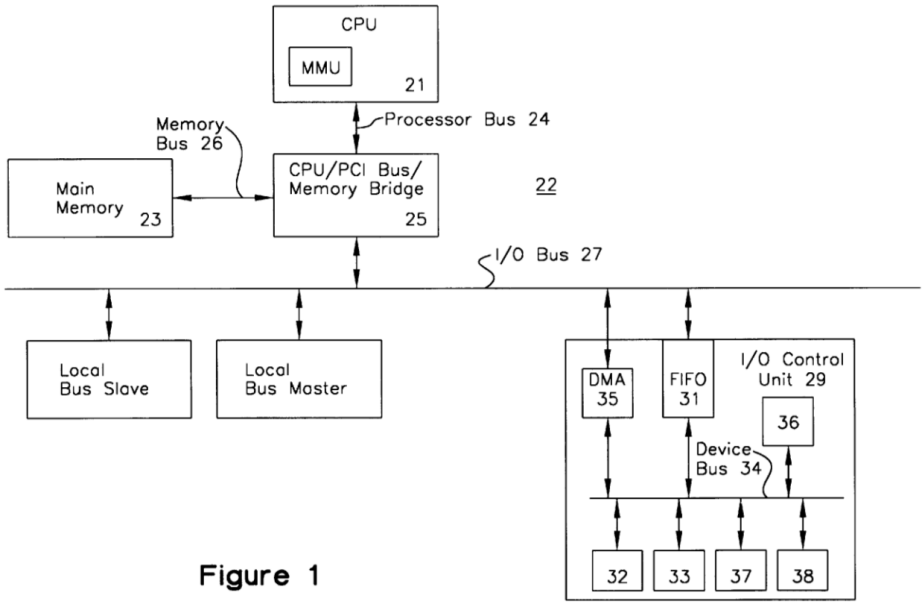
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	<p>“Various operating conditions can cause the flow control register 45 associated with a buffer 39 to store different values. If the central processing unit is writing at a rate faster than the input/output device can handle the commands, then a FIFO buffer 39 which is initially empty and provides a maximum free count value when read by the central processing unit will provide a lower free count number after the amount of data first indicated by the free count register has been sent. This will occur because the FIFO buffer 39 will empty more slowly than it is filled. In such a case, the next value read by the application program after sending the amount of data designated by the free count register will be a smaller number. The application program may again send this amount of data and be sure that the FIFO buffer will not overflow. On the other hand, if the central processing unit is writing at a rate slower than the input/output device can handle the commands, then a FIFO buffer which is initially empty and provides a maximum free count value when read by the central processing unit, will provide the same free count number after the amount of data first indicated by the flow control register has been sent. This will occur because the FIFO will empty more rapidly than it is filled and will always be empty when the register 45 is read by the central processing unit.” Rosenthal '930 at col. 17, ll. 19–42.</p> <p>“Those skilled in the art will recognize that the use of 128 individual FIFO buffers 39 to receive commands written by the central processing unit is very expensive and probably not economically feasible for use with personal computers. In addition, it is expensive of system resources for an operating system to context switch the central processing unit from one application program to another. Thus, the operating system will try to ensure that once an application is given the central processing unit the application will retain control long enough to amortize the cost of the context switch. This means that typically in a one processor system at most one FIFO buffer will be active at a time. In a multi-processor system, typically at most as many FIFO buffers will be active as there are processors.” Rosenthal '930 at col. 21, ll. 39–52.</p> <p>“One embodiment of the new architecture provides a means for attaining almost the same speed as is possible with 128 FIFO buffers but much more economically. Instead of 128 individual FIFO buffers 39, the described embodiment utilizes a smaller number of FIFO buffers 39 than the number of areas into which the input/output address space may be divided and thus the number of application programs which may be run. Utilizing a smaller number of FIFO buffers causes each FIFO buffer to function as a cache for commands which may be sent by any of the application programs. In the preferred embodiment, one FIFO buffer 39 is used for each processor which may be writing to the input/output control unit 29. For example, if the computer utilizes two processors arranged as symmetrical multi-processors, then two individual FIFO buffers are utilized. If, as is usually the case, only a single central processing unit is used, then a single FIFO buffer 39 may in the limit act as a cache for commands from all application programs which may be running on the</p>

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	<p>central processing unit. Such an arrangement is illustrated in FIG. 6. Of course, in either case more FIFO buffers might be used.” Rosenthal ’930 at col. 21, l. 53 – col. 22, l. 6.</p> <p>“As with the embodiments which use one FIFO buffer for each application area, a free count register 45 and a puller are included with each FIFO buffer 39 as a part of the input/output control unit 29. The register 45 stores an indication of the number of available entries in each FIFO buffer 39 of the FIFO unit 31 and allows a requirement to be placed on an application program attempting to access the input/output control unit 29 that it first determine whether space is available in the FIFO unit 31. It also allows an application presently using the resources of the input/output control unit 29 to proceed without overflowing the FIFO unit 31. The application program may obtain a boundary value indicating the number of free entries in the FIFO buffer by reading from a designated offset in any of the sub-areas of its mapped area. The application may write up to the amount of data designated by this boundary value without further testing and be certain that overflow of the FIFO unit will not occur. As with the multiple FIFO buffer embodiments, the FIFO buffer arrangements of the described embodiment make use of a memory runout area; such a memory runout area assures that a FIFO buffer may be used to cache commands from a plurality of application programs. The use of a memory runout area also allows the system to make use of lying in order to enhance the speed of transfer by reducing the number of read operations by the central processing unit of the free count register 45.” Rosenthal ’930 at col. 22, ll. 27–52.</p> <p>“9. A method for controlling the flow of data in a data transfer path of a computer having a first-in first-out (FIFO) buffer with a plurality of stages positioned between a computer input-output bus and input/output devices, each stage providing storage for both data and a virtual address which are translated to provide a physical address for commands decoupled from application programs originating the commands, comprising the steps of:</p> <p>detecting a value indicating an amount of space available for data in the FIFO buffer,</p> <p>transferring to the FIFO buffer an amount of data up to an amount determine from the value detected, and</p> <p>detecting another value indicating an amount of space available for data in the FIFO buffer before transferring additional data to the FIFO buffer.” Rosenthal ’930 at col. 24, ll. 51–65.</p>
[1b] an output queue implemented in hardware;	Rosenthal ’930 teaches “an output queue implemented in hardware,” including at least the following exemplary citations.

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	<p>For example, Rosenthal '930 teaches an output queue implemented in hardware, by disclosing, as non-limiting examples, a DMA device.</p> <p>Defendants have proposed a construction that “queue implemented in hardware” means “queue implemented in physical circuits without software intervention.” The output queue in Rosenthal '930 meets Defendants’ construction because, for example, Rosenthal '930 teaches a hardware implementation of its teachings, which includes its teachings of queues. <i>See, e.g.</i>, Rosenthal '930 at 4:54–57 (“The DMA device 35 includes its own memory management unit which allows writes from input/output devices to the virtual memory space of an application without involving the operating system in the translation process.”). <i>See, e.g.</i>:</p> <p>“To help maintain this asynchronous operating arrangement and to eliminate read operations to the extent possible, the input/output control unit also includes an advanced direct memory access (DMA) device 35 which provides direct memory access for operations conducted involving input/output devices. The DMA device 35 allows the results of input/output operations to be written from input/output devices to main memory 23 rather than requiring read operations by the central processing unit 21 to obtain these results. This eliminates almost all need for the central processing unit 21 to read input/output devices and drastically increases the overall speed of input/output operations. The DMA device 35 includes its own memory management unit which allows writes from input/output devices to the virtual memory space of an application without involving the operating system in the translation process.” Rosenthal '930 at col. 4, ll. 12–27.</p>
<p>[1c] a first processing element having access to said input queue and said output queue;</p>	<p>Rosenthal '930 teaches “a first processing element having access to said input queue and said output queue,” including at least the following exemplary citations.</p> <p>For example, Rosenthal '930 teaches a first processing element having access to said input queue and said output queue, by disclosing, as non-limiting examples, a CPU. The CPU has access to both the input queue and output queue. <i>See, e.g.</i>:</p> <p>“A digital system which uses an arrangement of one or more parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may</p>

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	<p>be written without running the risk of overflowing the data storage area which the input/output device has available.” Rosenthal '930 at Abstract.</p>  <p style="text-align: center;">Figure 1 Rosenthal '930 at Figure 1.</p>

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	<div data-bbox="583 259 1459 820"><p>The diagram illustrates a system architecture. At the top, a horizontal line represents Bus 27. Below it, a box labeled 'Decode 30' is connected to Bus 27. To the right, a box labeled 'Input/Output Control Unit 29' is connected to Bus 27. Below Bus 27, a large box contains several components: 'MMU 50' with a sub-box '52' and 'DMA 35' are on the left. In the center is a 'Pusher 53' box with a grid of cells (7, 3, 11, 32) and a '31' label. To the right of the pusher is a 'Resource Manager' box (dashed outline) and a 'Translation Table 38'. Below the pusher is a 'Disk Controller 32', 'Graphics Output Controller Memory 33', and 'Sound Generator 37'. A 'Bus 34' is at the bottom, connecting these components. Arrows indicate data flow between components and buses.</p></div> <p style="text-align: center;">Figure 3</p> <p>Rosenthal '930 at Figure 3.</p>

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	<p style="text-align: center;">Figure 7 Rosenthal '930 at Figure 7.</p> <p>“It is another object of the present invention to provide a flow control system for an architecture which utilizes FIFO buffers for buffering write operations.</p> <p>These and other objects of the present invention are realized in a system which uses an arrangement of parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the central processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal '930 at col. 2, ll. 15–33.</p> <p>“FIG. 1 is a block diagram of a computer system 22 which has been devised to overcome the problems of the prior art. The system 22 provides a new input/output architecture which cooperates with other components of present systems based on the PDP11 architecture, runs legacy code for those systems, yet is able to drastically</p>

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	<p>increase the speed of input/output operations for new application programs. In order to accomplish this, the new architecture of the system allows read and write operations by application programs to be made directly to the input/output devices. This eliminates the cumbersome multi-step software processes invoked by prior art systems using the operating system and trusted code for every input/output access. In order to accomplish the process safely, the input/output architecture of the system 22 utilizes an input/output control unit 29 which provides its own virtual name-to-physical-device and context translation for all of the input/output devices associated with the new control unit 29 on its own device bus 34. By enforcing this translation, application programs can write directly to input/output devices without affecting assets of other application programs. Once this translation from virtual names furnished by the application programs to physical input/output devices on the device bus is accomplished and context has been furnished to the input/output devices, translation of addresses of input/output devices on the input/output bus into physical addresses on the device bus 34 is accomplished directly by hardware at the input/output control unit 29. This hardware also checks permissions; and, when an operation is known to be safe, it is performed by hardware. When a translation operation fails, the operating system software is invoked. Thus, rather than trapping every input/output operation to determine whether it is safe as is done in prior art computer systems based on the PDP11 architecture, the system 22 traps and sends to operating system software only unsafe operations allowing hardware to accomplish most translations and greatly speeding the access of input/output devices.” Rosenthal ’930 at col. 3, ll. 29–65.</p> <p>“The architecture of the system 22 has been designed so that it eliminates almost all read operations of input/output devices by the central processing unit. In order to accomplish this, the input/output control unit 29 includes a first-in first-out (FIFO) unit 31 for storing write operations directed to the input/output control unit. The FIFO unit 31 queues incoming write operations. Unlike FIFO units in prior art systems, it stores both addresses and data. This allows the write operations to the input/output control unit 29 to occur asynchronously so that both the central processing unit 21 and the input/output control unit 29 may be functioning independently of one another and neither need wait for operations of the other.” Rosenthal ’930 at col. 3, l. 66 – col. 4, l. 11.</p> <p>“Although the input/output architecture of system 22 may be used with systems utilizing a single input/output bus for all operations, the preferred embodiment of system 22 functions as well in a system utilizing a local bus 27 such as the Peripheral Component Interconnect (PCI) bus or the Video Electronics Standards Association (VESA) local bus which may be associated with other input/output buses. While the discussion of this specification will assume that bus 27 is a local bus, the local bus 27 is also referred to in this specification as the input/output bus 27 in order to emphasize its use. In arrangements utilizing local buses,</p>

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	<p>the central processing unit 21 and main memory 23 are typically arranged on a processor bus 24 and a memory bus 26, respectively, and are joined to a bridge unit 25. The central processing unit 21 typically includes a memory management unit. The bridge unit 25 provides write buffering for operations between the central processing unit 21 and the input/output bus 27, between the central processing unit 21 and main memory 23 on the processor bus 24 and the memory bus 26, and between the input/output bus 27 and main memory 23.” Rosenthal ’930 at col. 4, ll. 28–48.</p> <p>“In the architecture of system 22, an input/output control unit 29 is shown joined to the input/output bus 27. The control unit 29 includes a hardware FIFO unit 31 for receiving incoming commands addressed to the input/output devices on a device bus 34.” Rosenthal ’930 at col. 4, ll. 60–64.</p> <p>“In one embodiment, the FIFO unit 31 includes a plurality of FIFO buffers 39 (see FIG. 3). When an application program desires to write to an input/output device on the device bus 34, it addresses that device. Decoding circuitry decodes the address by reviewing a number of the highest order bits decoded by the chip sufficient to indicate a unique portion of the input/output address space assigned to an application program and places the command in the appropriate FIFO buffer 39 for that application program. Each FIFO buffer 39 handles commands only from the application program to which the address area has been mapped. An arrangement using a smaller number of FIFO buffers 39 than one buffer for each application program (as few as a single buffer 39) could also be utilized as long as the address of the FIFO buffer is mapped to only one application program at a time.” Rosenthal ’930 at col. 5, ll. 51–66.</p> <p>“The unit 29 receives physical addresses furnished by the memory management unit and virtual names furnished by application programs for operations to be performed which have been sent to the FIFO unit 31 and controls the translation of those virtual names for all input/output devices. The hardware unit 29 includes the device bus 34 to which the individual input/output devices such as a disk controller 32, a graphics output controller 33, and a sound generator 37 are shown joined. The unit 29 also includes a DMA unit 35 which is adapted to transfer data between the individual input/output devices and main memory for use by the central processing unit or other components of the system.” Rosenthal ’930 at col. 5, l. 67 – col. 6, l. 10.</p> <p>“FIG. 3 is a block diagram illustrating details of the input/output control unit 29 including the device bus 34 and the input/output devices arranged on that bus. As described above, the input/output control unit 29 includes a decode unit 30 which receives commands directly from the input/output bus 27 and transfers the commands to a pusher circuit 53 which transfers the command to one of the FIFO buffers 39 of the FIFO unit 31. The FIFO unit 31 stores the data along with the addresses for each of the commands being transferred to all of the input/output devices associated with the input/output control unit 29. The buffers 39 of the FIFO</p>

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	<p>unit replace the individual data registers used by the input/output devices of the prior art. However, in contrast to the registers used by the prior art for communication on the input/output bus 27, the FIFO unit 31 allows a very much larger number of commands to be processed much more rapidly and facilitates the asynchronous operations of the input/output devices and the central processing unit. In one embodiment, the FIFO unit 31 includes 128 individual FIFO buffers 39 each of which has thirty-two stages. The use of 128 individual FIFO buffers 39 allows a FIFO buffer to be assigned to each of 128 different application programs which may be running on the central processing unit for the use of that application program alone. The thirty-two stages of each buffer 39 allow any FIFO buffer to hold thirty-two individual serially ordered commands at any time. Although each of the stages of the FIFO unit 31 holds (along with the address bits) the data held by an individual register of a typical prior art input/output device, a particular system has the ability to store commands for over 16 thousand 32 bit registers for each of 128 different application programs which may map different addresses decoded by the input/output control unit 29.” Rosenthal ’930 at col. 8, ll. 21–53.</p> <p>“The use of the flow control register 45 allows an application program presently using the resources of the input/output control unit 29 to proceed without causing the overflow of the FIFO unit 31. Whenever the application has written commands totaling the amount previously read from the register 45, it must read the register again. This is especially useful for application programs which may wish to transfer a series of commands in sequence, possibly using the burst transfer mode of operation provided by many of the modern buses. By ascertaining the space available in the FIFO buffer 39 before transferring a sequence of commands, the application can know that sufficient space will be available for the operation. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal ’930 at col. 17, ll. 4–18.</p> <p>“Various operating conditions can cause the flow control register 45 associated with a buffer 39 to store different values. If the central processing unit is writing at a rate faster than the input/output device can handle the commands, then a FIFO buffer 39 which is initially empty and provides a maximum free count value when read by the central processing unit will provide a lower free count number after the amount of data first indicated by the free count register has been sent. This will occur because the FIFO buffer 39 will empty more slowly than it is filled. In such a case, the next value read by the application program after sending the amount of data designated by the free count register will be a smaller number. The application program may again send this amount of data and be sure that the FIFO buffer will not overflow. On the other hand, if the central processing unit is writing at a rate slower than the input/output device can handle the commands, then a FIFO buffer which is initially empty and provides a maximum free count value when read by the central processing unit, will provide the same free count number after the amount of data first indicated by the flow</p>

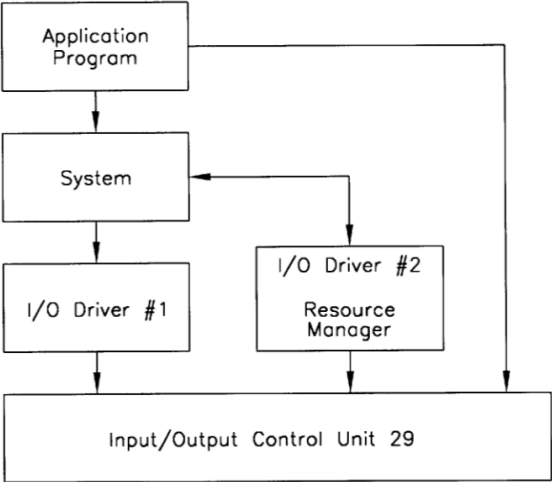
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	<p>control register has been sent. This will occur because the FIFO will empty more rapidly than it is filled and will always be empty when the register 45 is read by the central processing unit.” Rosenthal ’930 at col. 17, ll. 19–42.</p> <p>“Those skilled in the art will recognize that the use of 128 individual FIFO buffers 39 to receive commands written by the central processing unit is very expensive and probably not economically feasible for use with personal computers. In addition, it is expensive of system resources for an operating system to context switch the central processing unit from one application program to another. Thus, the operating system will try to ensure that once an application is given the central processing unit the application will retain control long enough to amortize the cost of the context switch. This means that typically in a one processor system at most one FIFO buffer will be active at a time. In a multi-processor system, typically at most as many FIFO buffers will be active as there are processors.” Rosenthal ’930 at col. 21, ll. 39–52.</p> <p>“One embodiment of the new architecture provides a means for attaining almost the same speed as is possible with 128 FIFO buffers but much more economically. Instead of 128 individual FIFO buffers 39, the described embodiment utilizes a smaller number of FIFO buffers 39 than the number of areas into which the input/output address space may be divided and thus the number of application programs which may be run. Utilizing a smaller number of FIFO buffers causes each FIFO buffer to function as a cache for commands which may be sent by any of the application programs. In the preferred embodiment, one FIFO buffer 39 is used for each processor which may be writing to the input/output control unit 29. For example, if the computer utilizes two processors arranged as symmetrical multi-processors, then two individual FIFO buffers are utilized. If, as is usually the case, only a single central processing unit is used, then a single FIFO buffer 39 may in the limit act as a cache for commands from all application programs which may be running on the central processing unit. Such an arrangement is illustrated in FIG. 6. Of course, in either case more FIFO buffers might be used.” Rosenthal ’930 at col. 21, l. 53 – col. 22, l. 6.</p> <p>“As with the embodiments which use one FIFO buffer for each application area, a free count register 45 and a puller are included with each FIFO buffer 39 as a part of the input/output control unit 29. The register 45 stores an indication of the number of available entries in each FIFO buffer 39 of the FIFO unit 31 and allows a requirement to be placed on an application program attempting to access the input/output control unit 29 that it first determine whether space is available in the FIFO unit 31. It also allows an application presently using the resources of the input/output control unit 29 to proceed without overflowing the FIFO unit 31. The application program may obtain a boundary value indicating the number of free entries in the FIFO buffer by reading from a designated offset in any of the sub-areas of its mapped area. The application may write up to</p>

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	<p>the amount of data designated by this boundary value without further testing and be certain that overflow of the FIFO unit will not occur. As with the multiple FIFO buffer embodiments, the FIFO buffer arrangements of the described embodiment make use of a memory runout area; such a memory runout area assures that a FIFO buffer may be used to cache commands from a plurality of application programs. The use of a memory runout area also allows the system to make use of lying in order to enhance the speed of transfer by reducing the number of read operations by the central processing unit of the free count register 45.” Rosenthal ’930 at col. 22, ll. 27–52.</p> <p>“9. A method for controlling the flow of data in a data transfer path of a computer having a first-in first-out (FIFO) buffer with a plurality of stages positioned between a computer input-output bus and input/output devices, each stage providing storage for both data and a virtual address which are translated to provide a physical address for commands decoupled from application programs originating the commands, comprising the steps of:</p> <p>detecting a value indicating an amount of space available for data in the FIFO buffer,</p> <p>transferring to the FIFO buffer an amount of data up to an amount determine from the value detected, and</p> <p>detecting another value indicating an amount of space available for data in the FIFO buffer before transferring additional data to the FIFO buffer.” Rosenthal ’930 at col. 24, ll. 51–65.</p>
<p>[1d] at least one second processing element in communication with said first processing element;</p>	<p>Rosenthal ’930 teaches “at least one second processing element in communication with said first processing element,” including at least the following exemplary citations.</p> <p>For example, Rosenthal ’930 teaches at least one second processing element in communication with said first processing element, by disclosing, as non-limiting examples, an I/O control unit. The I/O control unit, the second processing element is in communication with the first processing element. <i>See, e.g.:</i></p>

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	<div><p>Figure 1 Rosenthal '930 at Figure 1.</p></div>

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	 <pre>graph TD; AP[Application Program] --> S[System]; S --> ID1[I/O Driver #1]; S --> ID2[I/O Driver #2]; ID1 --> IOCU[Input/Output Control Unit 29]; ID2 --> IOCU; AP --> IOCU; RM[Resource Manager] --> ID2; RM --> S;</pre> <p data-bbox="583 821 934 894">Figure 2 Rosenthal '930 at Figure 2.</p>

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	<div data-bbox="583 259 1459 820"><p>The diagram illustrates a system architecture. At the top, a horizontal line represents Bus 27. Below it, a large rectangular block represents the Input/Output Control Unit 29. Inside this unit, at the top, is a 'Decode' block 30 connected to Bus 27. Below 'Decode' is a 'Pusher' block 53. To the left of the Pusher is a block containing 'MMU 50' and 'DMA 35'. Below the MMU/DMA block is a vertical stack of blocks labeled 36. To the right of the Pusher is a large grid-like structure with rows and columns, containing labels 7, 3, 11, 32, and 39. Below this grid is a block labeled 40. To the right of the grid is a block labeled 45. Below the grid is a dashed box labeled 'Resource Manager'. To the right of the Resource Manager is a 'Translation Table' block 38. Below the Translation Table is a horizontal line representing Bus 34. Below Bus 34 are three blocks: 'Disk Controller' 32, 'Graphics Output Controller Memory' 33, and 'Sound Generator' 37. Arrows indicate data flow: from Bus 27 to Decode 30; from Decode 30 to Pusher 53; from Pusher 53 to the grid; from the grid to DMA 35; from DMA 35 to Bus 34; from Bus 34 to Disk Controller 32, Graphics Output Controller Memory 33, and Sound Generator 37; from the grid to the Translation Table 38; and from the Translation Table 38 to Bus 34. There are also internal connections within the Input/Output Control Unit 29, including a connection from the Pusher 53 to the grid, and from the grid to the DMA 35 and the Translation Table 38.</p></div> <p data-bbox="945 824 1071 857">Figure 3</p> <p data-bbox="583 860 934 893">Rosenthal '930 at Figure 3.</p>

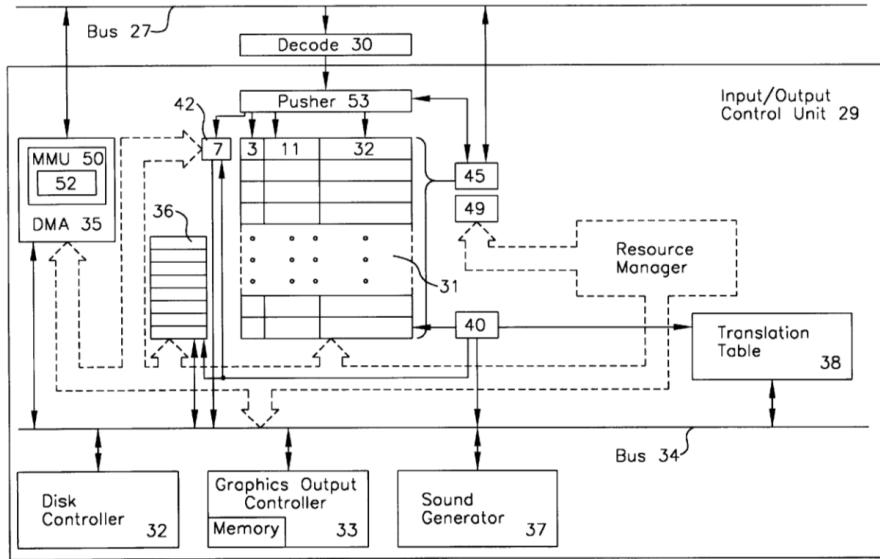
Claim Language	Exemplary Evidence of Anticipation and/or Obviousness
	 <p data-bbox="940 824 1073 857">Figure 6</p> <p data-bbox="583 862 932 894">Rosenthal '930 at Figure 6.</p> <p data-bbox="583 914 1896 987">“It is another object of the present invention to provide a flow control system for an architecture which utilizes FIFO buffers for buffering write operations.</p> <p data-bbox="583 1003 1986 1333">These and other objects of the present invention are realized in a system which uses an arrangement of parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the central processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal '930 at col. 2, ll. 15–33.</p> <p data-bbox="583 1349 1986 1455">“FIG. 1 is a block diagram of a computer system 22 which has been devised to overcome the problems of the prior art. The system 22 provides a new input/output architecture which cooperates with other components of present systems based on the PDP11 architecture, runs legacy code for those systems, yet is able to drastically</p>

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	<p>increase the speed of input/output operations for new application programs. In order to accomplish this, the new architecture of the system allows read and write operations by application programs to be made directly to the input/output devices. This eliminates the cumbersome multi-step software processes invoked by prior art systems using the operating system and trusted code for every input/output access. In order to accomplish the process safely, the input/output architecture of the system 22 utilizes an input/output control unit 29 which provides its own virtual name-to-physical-device and context translation for all of the input/output devices associated with the new control unit 29 on its own device bus 34. By enforcing this translation, application programs can write directly to input/output devices without affecting assets of other application programs. Once this translation from virtual names furnished by the application programs to physical input/output devices on the device bus is accomplished and context has been furnished to the input/output devices, translation of addresses of input/output devices on the input/output bus into physical addresses on the device bus 34 is accomplished directly by hardware at the input/output control unit 29. This hardware also checks permissions; and, when an operation is known to be safe, it is performed by hardware. When a translation operation fails, the operating system software is invoked. Thus, rather than trapping every input/output operation to determine whether it is safe as is done in prior art computer systems based on the PDP11 architecture, the system 22 traps and sends to operating system software only unsafe operations allowing hardware to accomplish most translations and greatly speeding the access of input/output devices.” Rosenthal ’930 at col. 3, ll. 29–65.</p> <p>“Although the input/output architecture of system 22 may be used with systems utilizing a single input/output bus for all operations, the preferred embodiment of system 22 functions as well in a system utilizing a local bus 27 such as the Peripheral Component Interconnect (PCI) bus or the Video Electronics Standards Association (VESA) local bus which may be associated with other input/output buses. While the discussion of this specification will assume that bus 27 is a local bus, the local bus 27 is also referred to in this specification as the input/output bus 27 in order to emphasize its use. In arrangements utilizing local buses, the central processing unit 21 and main memory 23 are typically arranged on a processor bus 24 and a memory bus 26, respectively, and are joined to a bridge unit 25. The central processing unit 21 typically includes a memory management unit. The bridge unit 25 provides write buffering for operations between the central processing unit 21 and the input/output bus 27, between the central processing unit 21 and main memory 23 on the processor bus 24 and the memory bus 26, and between the input/output bus 27 and main memory 23.” Rosenthal ’930 at col. 4, ll. 28–48.</p>

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	<p>“In the architecture of system 22, an input/output control unit 29 is shown joined to the input/output bus 27. The control unit 29 includes a hardware FIFO unit 31 for receiving incoming commands addressed to the input/output devices on a device bus 34.” Rosenthal ’930 at col. 4, ll. 60–64.</p> <p>“In one embodiment, the FIFO unit 31 includes a plurality of FIFO buffers 39 (see FIG. 3). When an application program desires to write to an input/output device on the device bus 34, it addresses that device. Decoding circuitry decodes the address by reviewing a number of the highest order bits decoded by the chip sufficient to indicate a unique portion of the input/output address space assigned to an application program and places the command in the appropriate FIFO buffer 39 for that application program. Each FIFO buffer 39 handles commands only from the application program to which the address area has been mapped. An arrangement using a smaller number of FIFO buffers 39 than one buffer for each application program (as few as a single buffer 39) could also be utilized as long as the address of the FIFO buffer is mapped to only one application program at a time.” Rosenthal ’930 at col. 5, ll. 51–66.</p> <p>“The unit 29 receives physical addresses furnished by the memory management unit and virtual names furnished by application programs for operations to be performed which have been sent to the FIFO unit 31 and controls the translation of those virtual names for all input/output devices. The hardware unit 29 includes the device bus 34 to which the individual input/output devices such as a disk controller 32, a graphics output controller 33, and a sound generator 37 are shown joined. The unit 29 also includes a DMA unit 35 which is adapted to transfer data between the individual input/output devices and main memory for use by the central processing unit or other components of the system.” Rosenthal ’930 at col. 5, l. 67 – col. 6, l. 10.</p> <p>“FIG. 3 is a block diagram illustrating details of the input/output control unit 29 including the device bus 34 and the input/output devices arranged on that bus. As described above, the input/output control unit 29 includes a decode unit 30 which receives commands directly from the input/output bus 27 and transfers the commands to a pusher circuit 53 which transfers the command to one of the FIFO buffers 39 of the FIFO unit 31. The FIFO unit 31 stores the data along with the addresses for each of the commands being transferred to all of the input/output devices associated with the input/output control unit 29. The buffers 39 of the FIFO unit replace the individual data registers used by the input/output devices of the prior art. However, in contrast to the registers used by the prior art for communication on the input/output bus 27, the FIFO unit 31 allows a very much larger number of commands to be processed much more rapidly and facilitates the asynchronous operations of the input/output devices and the central processing unit. In one embodiment, the FIFO unit 31 includes 128 individual FIFO buffers 39 each of which has thirty-two stages. The use of 128 individual FIFO buffers 39 allows a FIFO buffer to be assigned to each of 128 different application programs which may be</p>

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	<p>running on the central processing unit for the use of that application program alone. The thirty-two stages of each buffer 39 allow any FIFO buffer to hold thirty-two individual serially ordered commands at any time. Although each of the stages of the FIFO unit 31 holds (along with the address bits) the data held by an individual register of a typical prior art input/output device, a particular system has the ability to store commands for over 16 thousand 32 bit registers for each of 128 different application programs which may map different addresses decoded by the input/output control unit 29.” Rosenthal ’930 at col. 8, ll. 21–53.</p> <p>“Those skilled in the art will recognize that the use of 128 individual FIFO buffers 39 to receive commands written by the central processing unit is very expensive and probably not economically feasible for use with personal computers. In addition, it is expensive of system resources for an operating system to context switch the central processing unit from one application program to another. Thus, the operating system will try to ensure that once an application is given the central processing unit the application will retain control long enough to amortize the cost of the context switch. This means that typically in a one processor system at most one FIFO buffer will be active at a time. In a multi-processor system, typically at most as many FIFO buffers will be active as there are processors.” Rosenthal ’930 at col. 21, ll. 39–52.</p> <p>“One embodiment of the new architecture provides a means for attaining almost the same speed as is possible with 128 FIFO buffers but much more economically. Instead of 128 individual FIFO buffers 39, the described embodiment utilizes a smaller number of FIFO buffers 39 than the number of areas into which the input/output address space may be divided and thus the number of application programs which may be run. Utilizing a smaller number of FIFO buffers causes each FIFO buffer to function as a cache for commands which may be sent by any of the application programs. In the preferred embodiment, one FIFO buffer 39 is used for each processor which may be writing to the input/output control unit 29. For example, if the computer utilizes two processors arranged as symmetrical multi-processors, then two individual FIFO buffers are utilized. If, as is usually the case, only a single central processing unit is used, then a single FIFO buffer 39 may in the limit act as a cache for commands from all application programs which may be running on the central processing unit. Such an arrangement is illustrated in FIG. 6. Of course, in either case more FIFO buffers might be used.” Rosenthal ’930 at col. 21, l. 53 – col. 22, l. 6.</p> <p>“9. A method for controlling the flow of data in a data transfer path of a computer having a first-in first-out (FIFO) buffer with a plurality of stages positioned between a computer input-output bus and input/output devices, each stage providing storage for both data and a virtual address which are translated to provide a physical address for commands decoupled from application programs originating the commands, comprising the steps of:</p>

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	<p>detecting a value indicating an amount of space available for data in the FIFO buffer, transferring to the FIFO buffer an amount of data up to an amount determine from the value detected, and detecting another value indicating an amount of space available for data in the FIFO buffer before transferring additional data to the FIFO buffer.” Rosenthal ’930 at col. 24, ll. 51–65.</p>
<p>[1e] a reservation register implemented in hardware storing a value indicative of available space in said input queue, said reservation register accessible by both said first processing element and said at least one second processing element;</p>	<p>Rosenthal ’930 teaches “a reservation register implemented in hardware storing a value indicative of available space in said input queue, said reservation register accessible by both said first processing element and said at least one second processing element,” including at least the following exemplary citations.</p> <p>For example, Rosenthal ’930 teaches a reservation register implemented in hardware storing a value indicative of available space in said input queue, said reservation register accessible by both said first processing element and said at least one second processing element, by disclosing, as non-limiting examples, a flow control register. The flow control register stores a value of indicative space and is accessible by both the first and second processing elements discussed above.</p> <p>Defendants have proposed a construction that “register” means “set of flip–flops that store a set of related bits.” Rosenthal ’930 teaches a reservation register that is a set of flip–flops that store a set of related bits. <i>See, e.g.</i>, Rosenthal ’930 at 16:58–62 (“In one embodiment of the new architecture, a flow control register 45 is included for each FIFO buffer 39 of the input/output control unit 29. The register 45 stores an indication of the number of available spaces for commands in the associated FIFO buffer 39.”). For example, the flow control register identified above is explained and described as a register and the description of its behavior is consistent with a set of flip–flops that store a set of related bits. <i>See id.</i> Rosenthal ’930 is a multiprocessor system that uses registers. A POSITA reading Rosenthal ’930 would have understood the description of these registers to be a set of flip–flops that store a set of related bits in view of the relevant disclosures, and further because that is how hardware systems and registers in particular had been designed and implemented for decades. <i>See, e.g.</i>:</p> <p>“A digital system which uses an arrangement of one or more parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may</p>

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	<p>be written without running the risk of overflowing the data storage area which the input/output device has available.” Rosenthal ’930 at Abstract.</p> <p>“It is another object of the present invention to provide a flow control system for an architecture which utilizes FIFO buffers for buffering write operations.</p> <p>These and other objects of the present invention are realized in a system which uses an arrangement of parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the central processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal ’930 at col. 2, ll. 15–33.</p> <p>“In one embodiment of the new architecture, a flow control register 45 is included for each FIFO buffer 39 of the input/output control unit 29. The register 45 stores an indication of the number of available spaces for commands in the associated FIFO buffer 39. The use of this flow control register 45 allows a requirement to be placed on an application program attempting an access of the input/output control unit 29 that it first determine whether space is available in the FIFO unit 31 before it writes any command. Before writing any data, the application program must determine the amount of "free" space to which it may write. This it does by having the central processing unit read the value in the flow control register 45 associated with the FIFO buffer 39 being utilized. Once this value has been read, the application program may send up to that amount of data before it need test again to determine whether free space remains to which it may send more data.” Rosenthal ’930 at col. 16, ll. 33–49.</p> <p>“In one embodiment of the new architecture the individual buffers 39 are implemented utilizing an array of random access memory (RAM). In such an arrangement, the data comprising the commands is placed in the RAM and pointers are utilized to define the positions of the beginning and end of the individual FIFO buffers 39 and the beginning and end of the data. In such an embodiment, a simple subtraction of a pointer designating the last data placed in a particular RAM buffer from the pointer designating the end of the buffer provides the value to be held by the flow control register. In such a case, the flow control register itself may be a logical register whose contents are computed whenever it is read.” Rosenthal ’930 at col. 16, l. 58 – col. 17, l. 3.</p>

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	<p>“The use of the flow control register 45 allows an application program presently using the resources of the input/output control unit 29 to proceed without causing the overflow of the FIFO unit 31. Whenever the application has written commands totaling the amount previously read from the register 45, it must read the register again. This is especially useful for application programs which may wish to transfer a series of commands in sequence, possibly using the burst transfer mode of operation provided by many of the modern buses. By ascertaining the space available in the FIFO buffer 39 before transferring a sequence of commands, the application can know that sufficient space will be available for the operation. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal '930 at col. 17, ll. 4–18.</p> <p>“Various operating conditions can cause the flow control register 45 associated with a buffer 39 to store different values. If the central processing unit is writing at a rate faster than the input/output device can handle the commands, then a FIFO buffer 39 which is initially empty and provides a maximum free count value when read by the central processing unit will provide a lower free count number after the amount of data first indicated by the free count register has been sent. This will occur because the FIFO buffer 39 will empty more slowly than it is filled. In such a case, the next value read by the application program after sending the amount of data designated by the free count register will be a smaller number. The application program may again send this amount of data and be sure that the FIFO buffer will not overflow. On the other hand, if the central processing unit is writing at a rate slower than the input/output device can handle the commands, then a FIFO buffer which is initially empty and provides a maximum free count value when read by the central processing unit, will provide the same free count number after the amount of data first indicated by the flow control register has been sent. This will occur because the FIFO will empty more rapidly than it is filled and will always be empty when the register 45 is read by the central processing unit.” Rosenthal '930 at col. 17, ll. 19–42.</p> <p>“In utilizing the free count value, the application program should deduct the value of any data which it has already written before each new write operation commences. In this manner, the application program knows at any time the amount of data which it may still write to the input/output device before another read of the free count register will be required. This allows a number of write operations to occur before a read of the register 45 (which significantly slows operation of the overall system) need occur. This also assures that any writes which might be presently in the write channel on the input/output bus are accounted for in determining the actual value of the free count left. It should be noted that this read of the free count register is the only read necessary in dealing with the input/output control unit 29. It would be possible either to interrupt the central processing unit if a FIFO buffer 39 filled or to use the DMA unit 35 to transfer the value in the free</p>

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	<p>count register to the central processing unit instead of reading the value, but in the particular embodiment reading the free count register appears to be the fastest operation.” Rosenthal ’930 at col. 17, l. 52 – col. 18, l. 4.</p> <p>“In one embodiment, the application program may obtain a free count value indicating the number of free entries in a FIFO buffer 39 by reading from a designated method offset in any of the sub-areas of the area mapped to the application program. The value read is that stored in the flow control register 45 associated with the particular FIFO buffer 39. This value is then placed on the bus when the central processing unit provides the appropriate control signals to implement the read operation. The application may write up to the amount of data designated by this free count value without further testing and be certain that overflow of the FIFO buffer 39 will not occur.” Rosenthal ’930 at col. 18, ll. 16–27.</p> <p>“As with the embodiments which use one FIFO buffer for each application area, a free count register 45 and a puller are included with each FIFO buffer 39 as a part of the input/output control unit 29. The register 45 stores an indication of the number of available entries in each FIFO buffer 39 of the FIFO unit 31 and allows a requirement to be placed on an application program attempting to access the input/output control unit 29 that it first determine whether space is available in the FIFO unit 31. It also allows an application presently using the resources of the input/output control unit 29 to proceed without overflowing the FIFO unit 31. The application program may obtain a boundary value indicating the number of free entries in the FIFO buffer by reading from a designated offset in any of the sub-areas of its mapped area. The application may write up to the amount of data designated by this boundary value without further testing and be certain that overflow of the FIFO unit will not occur. As with the multiple FIFO buffer embodiments, the FIFO buffer arrangements of the described embodiment make use of a memory runout area; such a memory runout area assures that a FIFO buffer may be used to cache commands from a plurality of application programs. The use of a memory runout area also allows the system to make use of lying in order to enhance the speed of transfer by reducing the number of read operations by the central processing unit of the free count register 45.” Rosenthal ’930 at col. 22, ll. 27–52.</p> <p>“means for informing a source of data of stages of the FIFO circuit available to store data including a register for storing a value indicating the number of stages of the FIFO circuit which are available.</p> <p>2. A flow control circuit as claimed in claim 1 in which the means for informing a source of data of stages of the FIFO circuit available to store data includes means for furnishing the value in the register to an application program.” Rosenthal ’930 at col. 24, ll. 12–19.</p>

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Claim Language	Exemplary Evidence of Anticipation and/or Obviousness
	<p>“9. A method for controlling the flow of data in a data transfer path of a computer having a first-in first-out (FIFO) buffer with a plurality of stages positioned between a computer input-output bus and input/output devices, each stage providing storage for both data and a virtual address which are translated to provide a physical address for commands decoupled from application programs originating the commands, comprising the steps of:</p> <p>detecting a value indicating an amount of space available for data in the FIFO buffer,</p> <p>transferring to the FIFO buffer an amount of data up to an amount determine from the value detected, and</p> <p>detecting another value indicating an amount of space available for data in the FIFO buffer before transferring additional data to the FIFO buffer.” Rosenthal ’930 at col. 24, ll. 51–65.</p>
<p>[1f] computer storage storing instructions, which when executed by said at least one second processing element:</p>	<p>Rosenthal ’930 teaches computer storage storing instructions executed by said at least one second processing element, including at least the following exemplary citations.</p> <p>For example, Rosenthal ’930 teaches computer storage storing instructions that are executed by said at least one second processing element, by disclosing, as non-limiting examples, application programs, e.g. resource manager that are executed from computer storage. The processors execute those instructions stored in the computer storage. <i>See, e.g.:</i></p> <p>“A digital system which uses an arrangement of one or more parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available.” Rosenthal ’930 at Abstract.</p> <p>“It is another object of the present invention to provide a flow control system for an architecture which utilizes FIFO buffers for buffering write operations.</p> <p>These and other objects of the present invention are realized in a system which uses an arrangement of parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO</p>

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	<p>buffer, each FIFO buffer includes a flow control register which must be read by the central processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal ’930 at col. 2, ll. 15–33.</p> <p>“Thus, as may be seen, the resource manager is a piece of software which is associated with the input/output control unit 29 and determines that the input/output control unit 29 functions correctly. It maintains a database of data structures which represent the various input/output devices and the context that those devices require to function correctly. It fills the translation table 38, does the necessary context switching for initializing the physical devices, provides routines for less used input/output operations which input/output devices may invoke through interrupts, and does other things required to run the input/output control unit 29. The resource manager may be thought of as part of the operating system and takes the place of the device driver used in a conventional input/output system. The resource manager maps in a part of the physical hardware of the input/output control unit 29 called the privileged address space. This space is distinct from the FIFO unit. Unlike the application programs operating with input/output devices, the resource manager both reads and writes this address space to perform its various tasks such as context switching. Unlike all of the device drivers of the prior art, the resource manager accomplishes its functions after the hardware of the input/output control unit 29 has been directly addressed by an application program rather than before. Moreover, in the overall operation of the input/output control unit 29, the resource manager is used infrequently compared to the hardware portions of the input/output control unit 29 since the resource manager attends only to creation operations, the various software implementations of methods, and unsafe operations.” Rosenthal ’930 at col. 15, ll. 35–64.</p> <p>“The use of the flow control register 45 allows an application program presently using the resources of the input/output control unit 29 to proceed without causing the overflow of the FIFO unit 31. Whenever the application has written commands totaling the amount previously read from the register 45, it must read the register again. This is especially useful for application programs which may wish to transfer a series of commands in sequence, possibly using the burst transfer mode of operation provided by many of the modern buses. By ascertaining the space available in the FIFO buffer 39 before transferring a sequence of commands, the application can know that sufficient space will be available for the operation. Provided that no application</p>

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	<p>program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal ’930 at col. 17, ll. 4–18.</p> <p>“Various operating conditions can cause the flow control register 45 associated with a buffer 39 to store different values. If the central processing unit is writing at a rate faster than the input/output device can handle the commands, then a FIFO buffer 39 which is initially empty and provides a maximum free count value when read by the central processing unit will provide a lower free count number after the amount of data first indicated by the free count register has been sent. This will occur because the FIFO buffer 39 will empty more slowly than it is filled. In such a case, the next value read by the application program after sending the amount of data designated by the free count register will be a smaller number. The application program may again send this amount of data and be sure that the FIFO buffer will not overflow. On the other hand, if the central processing unit is writing at a rate slower than the input/output device can handle the commands, then a FIFO buffer which is initially empty and provides a maximum free count value when read by the central processing unit, will provide the same free count number after the amount of data first indicated by the flow control register has been sent. This will occur because the FIFO will empty more rapidly than it is filled and will always be empty when the register 45 is read by the central processing unit.” Rosenthal ’930 at col. 17, ll. 19–42.</p> <p>“In utilizing the free count value, the application program should deduct the value of any data which it has already written before each new write operation commences. In this manner, the application program knows at any time the amount of data which it may still write to the input/output device before another read of the free count register will be required. This allows a number of write operations to occur before a read of the register 45 (which significantly slows operation of the overall system) need occur. This also assures that any writes which might be presently in the write channel on the input/output bus are accounted for in determining the actual value of the free count left. It should be noted that this read of the free count register is the only read necessary in dealing with the input/output control unit 29. It would be possible either to interrupt the central processing unit if a FIFO buffer 39 filled or to use the DMA unit 35 to transfer the value in the free count register to the central processing unit instead of reading the value, but in the particular embodiment reading the free count register appears to be the fastest operation.” Rosenthal ’930 at col. 17, l. 52 – col. 18, l. 4.</p> <p>“In one embodiment, the application program may obtain a free count value indicating the number of free entries in a FIFO buffer 39 by reading from a designated method offset in any of the sub-areas of the area mapped to the application program. The value read is that stored in the flow control register 45 associated</p>

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	<p>with the particular FIFO buffer 39. This value is then placed on the bus when the central processing unit provides the appropriate control signals to implement the read operation. The application may write up to the amount of data designated by this free count value without further testing and be certain that overflow of the FIFO buffer 39 will not occur.” Rosenthal ’930 at col. 18, ll. 16–27.</p> <p>“As with the embodiments which use one FIFO buffer for each application area, a free count register 45 and a puller are included with each FIFO buffer 39 as a part of the input/output control unit 29. The register 45 stores an indication of the number of available entries in each FIFO buffer 39 of the FIFO unit 31 and allows a requirement to be placed on an application program attempting to access the input/output control unit 29 that it first determine whether space is available in the FIFO unit 31. It also allows an application presently using the resources of the input/output control unit 29 to proceed without overflowing the FIFO unit 31. The application program may obtain a boundary value indicating the number of free entries in the FIFO buffer by reading from a designated offset in any of the sub-areas of its mapped area. The application may write up to the amount of data designated by this boundary value without further testing and be certain that overflow of the FIFO unit will not occur. As with the multiple FIFO buffer embodiments, the FIFO buffer arrangements of the described embodiment make use of a memory runout area; such a memory runout area assures that a FIFO buffer may be used to cache commands from a plurality of application programs. The use of a memory runout area also allows the system to make use of lying in order to enhance the speed of transfer by reducing the number of read operations by the central processing unit of the free count register 45.” Rosenthal ’930 at col. 22, ll. 27–52.</p> <p>“9. A method for controlling the flow of data in a data transfer path of a computer having a first-in first-out (FIFO) buffer with a plurality of stages positioned between a computer input-output bus and input/output devices, each stage providing storage for both data and a virtual address which are translated to provide a physical address for commands decoupled from application programs originating the commands, comprising the steps of:</p> <p>detecting a value indicating an amount of space available for data in the FIFO buffer,</p> <p>transferring to the FIFO buffer an amount of data up to an amount determine from the value detected, and</p> <p>detecting another value indicating an amount of space available for data in the FIFO buffer before transferring additional data to the FIFO buffer.” Rosenthal ’930 at col. 24, ll. 51–65.</p>

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<p>[1g] accesses said reservation register and reads said stored value;</p>	<p>Rosenthal '930 teaches “accesses said reservation register and reads said stored value,” including at least the following exemplary citations.</p> <p>For example, Rosenthal '930 teaches that the second processing element executes instructions that causes it to access said reservation register and reads said stored value, by disclosing, as non-limiting examples, accessing the flow control register to determine if there is sufficient space. The processor that is running the application program accesses and reads the stored value in the reservation register. <i>See, e.g.:</i></p> <p>“A digital system which uses an arrangement of one or more parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available.” Rosenthal '930 at Abstract.</p> <p>“It is another object of the present invention to provide a flow control system for an architecture which utilizes FIFO buffers for buffering write operations.</p> <p>These and other objects of the present invention are realized in a system which uses an arrangement of parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the central processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal '930 at col. 2, ll. 15–33.</p> <p>“In one embodiment of the new architecture, a flow control register 45 is included for each FIFO buffer 39 of the input/output control unit 29. The register 45 stores an indication of the number of available spaces for commands in the associated FIFO buffer 39. The use of this flow control register 45 allows a requirement to be placed on an application program attempting an access of the input/output control unit 29 that it first determine whether space is available in the FIFO unit 31 before it writes any command. Before writing any data, the application program must determine the amount of "free" space to which it may write. This it does</p>

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	<p>by having the central processing unit read the value in the flow control register 45 associated with the FIFO buffer 39 being utilized. Once this value has been read, the application program may send up to that amount of data before it need test again to determine whether free space remains to which it may send more data.” Rosenthal ’930 at col. 16, ll. 33–49.</p> <p>“The use of the flow control register 45 allows an application program presently using the resources of the input/output control unit 29 to proceed without causing the overflow of the FIFO unit 31. Whenever the application has written commands totaling the amount previously read from the register 45, it must read the register again. This is especially useful for application programs which may wish to transfer a series of commands in sequence, possibly using the burst transfer mode of operation provided by many of the modern buses. By ascertaining the space available in the FIFO buffer 39 before transferring a sequence of commands, the application can know that sufficient space will be available for the operation. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal ’930 at col. 17, ll. 4–18.</p> <p>“Various operating conditions can cause the flow control register 45 associated with a buffer 39 to store different values. If the central processing unit is writing at a rate faster than the input/output device can handle the commands, then a FIFO buffer 39 which is initially empty and provides a maximum free count value when read by the central processing unit will provide a lower free count number after the amount of data first indicated by the free count register has been sent. This will occur because the FIFO buffer 39 will empty more slowly than it is filled. In such a case, the next value read by the application program after sending the amount of data designated by the free count register will be a smaller number. The application program may again send this amount of data and be sure that the FIFO buffer will not overflow. On the other hand, if the central processing unit is writing at a rate slower than the input/output device can handle the commands, then a FIFO buffer which is initially empty and provides a maximum free count value when read by the central processing unit, will provide the same free count number after the amount of data first indicated by the flow control register has been sent. This will occur because the FIFO will empty more rapidly than it is filled and will always be empty when the register 45 is read by the central processing unit.” Rosenthal ’930 at col. 17, ll. 19–42.</p> <p>“In utilizing the free count value, the application program should deduct the value of any data which it has already written before each new write operation commences. In this manner, the application program knows at any time the amount of data which it may still write to the input/output device before another read of the free count register will be required. This allows a number of write operations to occur before a read of the</p>

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	<p>register 45 (which significantly slows operation of the overall system) need occur. This also assures that any writes which might be presently in the write channel on the input/output bus are accounted for in determining the actual value of the free count left. It should be noted that this read of the free count register is the only read necessary in dealing with the input/output control unit 29. It would be possible either to interrupt the central processing unit if a FIFO buffer 39 filled or to use the DMA unit 35 to transfer the value in the free count register to the central processing unit instead of reading the value, but in the particular embodiment reading the free count register appears to be the fastest operation.” Rosenthal ’930 at col. 17, l. 52 – col. 18, l. 4.</p> <p>“In one embodiment, the application program may obtain a free count value indicating the number of free entries in a FIFO buffer 39 by reading from a designated method offset in any of the sub-areas of the area mapped to the application program. The value read is that stored in the flow control register 45 associated with the particular FIFO buffer 39. This value is then placed on the bus when the central processing unit provides the appropriate control signals to implement the read operation. The application may write up to the amount of data designated by this free count value without further testing and be certain that overflow of the FIFO buffer 39 will not occur.” Rosenthal ’930 at col. 18, ll. 16–27.</p> <p>“As with the embodiments which use one FIFO buffer for each application area, a free count register 45 and a puller are included with each FIFO buffer 39 as a part of the input/output control unit 29. The register 45 stores an indication of the number of available entries in each FIFO buffer 39 of the FIFO unit 31 and allows a requirement to be placed on an application program attempting to access the input/output control unit 29 that it first determine whether space is available in the FIFO unit 31. It also allows an application presently using the resources of the input/output control unit 29 to proceed without overflowing the FIFO unit 31. The application program may obtain a boundary value indicating the number of free entries in the FIFO buffer by reading from a designated offset in any of the sub-areas of its mapped area. The application may write up to the amount of data designated by this boundary value without further testing and be certain that overflow of the FIFO unit will not occur. As with the multiple FIFO buffer embodiments, the FIFO buffer arrangements of the described embodiment make use of a memory runout area; such a memory runout area assures that a FIFO buffer may be used to cache commands from a plurality of application programs. The use of a memory runout area also allows the system to make use of lying in order to enhance the speed of transfer by reducing the number of read operations by the central processing unit of the free count register 45.” Rosenthal ’930 at col. 22, ll. 27–52.</p>

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	<p>“means for informing a source of data of stages of the FIFO circuit available to store data including a register for storing a value indicating the number of stages of the FIFO circuit which are available.</p> <p>2. A flow control circuit as claimed in claim 1 in which the means for informing a source of data of stages of the FIFO circuit available to store data includes means for furnishing the value in the register to an application program.” Rosenthal ’930 at col. 24, ll. 12–19.</p> <p>“9. A method for controlling the flow of data in a data transfer path of a computer having a first-in first-out (FIFO) buffer with a plurality of stages positioned between a computer input-output bus and input/output devices, each stage providing storage for both data and a virtual address which are translated to provide a physical address for commands decoupled from application programs originating the commands, comprising the steps of:</p> <p>detecting a value indicating an amount of space available for data in the FIFO buffer,</p> <p>transferring to the FIFO buffer an amount of data up to an amount determine from the value detected, and</p> <p>detecting another value indicating an amount of space available for data in the FIFO buffer before transferring additional data to the FIFO buffer.” Rosenthal ’930 at col. 24, ll. 51–65.</p>
<p>[1h] determines when said read value indicates available space in said input queue for said first processing element to issue a command;</p>	<p>Rosenthal ’930 teaches “determines when said read value indicates available space in said input queue for said first processing element to issue a command,” including at least the following exemplary citations.</p> <p>For example, Rosenthal ’930 teaches that the second processing element executes instructions that causes it to determine when said read value indicates available space in said input queue for said first processing element to issue a command, by disclosing, as non-limiting examples, application programs that read the flow control register to determine if there is sufficient space before writing. The processor that is running the application program determines if the stored value indicates available space in the input queue for the first processing element to issue a command. <i>See, e.g.:</i></p> <p>“A digital system which uses an arrangement of one or more parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may</p>

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	<p>be written without running the risk of overflowing the data storage area which the input/output device has available.” Rosenthal ’930 at Abstract.</p> <p>“It is another object of the present invention to provide a flow control system for an architecture which utilizes FIFO buffers for buffering write operations.</p> <p>These and other objects of the present invention are realized in a system which uses an arrangement of parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the central processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal ’930 at col. 2, ll. 15–33.</p> <p>“In one embodiment of the new architecture, a flow control register 45 is included for each FIFO buffer 39 of the input/output control unit 29. The register 45 stores an indication of the number of available spaces for commands in the associated FIFO buffer 39. The use of this flow control register 45 allows a requirement to be placed on an application program attempting an access of the input/output control unit 29 that it first determine whether space is available in the FIFO unit 31 before it writes any command. Before writing any data, the application program must determine the amount of "free" space to which it may write. This it does by having the central processing unit read the value in the flow control register 45 associated with the FIFO buffer 39 being utilized. Once this value has been read, the application program may send up to that amount of data before it need test again to determine whether free space remains to which it may send more data.” Rosenthal ’930 at col. 16, ll. 33–49.</p> <p>“The use of the flow control register 45 allows an application program presently using the resources of the input/output control unit 29 to proceed without causing the overflow of the FIFO unit 31. Whenever the application has written commands totaling the amount previously read from the register 45, it must read the register again. This is especially useful for application programs which may wish to transfer a series of commands in sequence, possibly using the burst transfer mode of operation provided by many of the modern buses. By ascertaining the space available in the FIFO buffer 39 before transferring a sequence of commands, the application can know that sufficient space will be available for the operation. Provided that no application</p>

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	<p>program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal ’930 at col. 17, ll. 4–18.</p> <p>“Various operating conditions can cause the flow control register 45 associated with a buffer 39 to store different values. If the central processing unit is writing at a rate faster than the input/output device can handle the commands, then a FIFO buffer 39 which is initially empty and provides a maximum free count value when read by the central processing unit will provide a lower free count number after the amount of data first indicated by the free count register has been sent. This will occur because the FIFO buffer 39 will empty more slowly than it is filled. In such a case, the next value read by the application program after sending the amount of data designated by the free count register will be a smaller number. The application program may again send this amount of data and be sure that the FIFO buffer will not overflow. On the other hand, if the central processing unit is writing at a rate slower than the input/output device can handle the commands, then a FIFO buffer which is initially empty and provides a maximum free count value when read by the central processing unit, will provide the same free count number after the amount of data first indicated by the flow control register has been sent. This will occur because the FIFO will empty more rapidly than it is filled and will always be empty when the register 45 is read by the central processing unit.” Rosenthal ’930 at col. 17, ll. 19–42.</p> <p>“In utilizing the free count value, the application program should deduct the value of any data which it has already written before each new write operation commences. In this manner, the application program knows at any time the amount of data which it may still write to the input/output device before another read of the free count register will be required. This allows a number of write operations to occur before a read of the register 45 (which significantly slows operation of the overall system) need occur. This also assures that any writes which might be presently in the write channel on the input/output bus are accounted for in determining the actual value of the free count left. It should be noted that this read of the free count register is the only read necessary in dealing with the input/output control unit 29. It would be possible either to interrupt the central processing unit if a FIFO buffer 39 filled or to use the DMA unit 35 to transfer the value in the free count register to the central processing unit instead of reading the value, but in the particular embodiment reading the free count register appears to be the fastest operation.” Rosenthal ’930 at col. 17, l. 52 – col. 18, l. 4.</p> <p>“In one embodiment, the application program may obtain a free count value indicating the number of free entries in a FIFO buffer 39 by reading from a designated method offset in any of the sub-areas of the area mapped to the application program. The value read is that stored in the flow control register 45 associated</p>

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	<p>with the particular FIFO buffer 39. This value is then placed on the bus when the central processing unit provides the appropriate control signals to implement the read operation. The application may write up to the amount of data designated by this free count value without further testing and be certain that overflow of the FIFO buffer 39 will not occur.” Rosenthal ’930 at col. 18, ll. 16–27.</p> <p>“As with the embodiments which use one FIFO buffer for each application area, a free count register 45 and a puller are included with each FIFO buffer 39 as a part of the input/output control unit 29. The register 45 stores an indication of the number of available entries in each FIFO buffer 39 of the FIFO unit 31 and allows a requirement to be placed on an application program attempting to access the input/output control unit 29 that it first determine whether space is available in the FIFO unit 31. It also allows an application presently using the resources of the input/output control unit 29 to proceed without overflowing the FIFO unit 31. The application program may obtain a boundary value indicating the number of free entries in the FIFO buffer by reading from a designated offset in any of the sub-areas of its mapped area. The application may write up to the amount of data designated by this boundary value without further testing and be certain that overflow of the FIFO unit will not occur. As with the multiple FIFO buffer embodiments, the FIFO buffer arrangements of the described embodiment make use of a memory runout area; such a memory runout area assures that a FIFO buffer may be used to cache commands from a plurality of application programs. The use of a memory runout area also allows the system to make use of lying in order to enhance the speed of transfer by reducing the number of read operations by the central processing unit of the free count register 45.” Rosenthal ’930 at col. 22, ll. 27–52.</p> <p>“9. A method for controlling the flow of data in a data transfer path of a computer having a first-in first-out (FIFO) buffer with a plurality of stages positioned between a computer input-output bus and input/output devices, each stage providing storage for both data and a virtual address which are translated to provide a physical address for commands decoupled from application programs originating the commands, comprising the steps of:</p> <p>detecting a value indicating an amount of space available for data in the FIFO buffer,</p> <p>transferring to the FIFO buffer an amount of data up to an amount determine from the value detected, and</p> <p>detecting another value indicating an amount of space available for data in the FIFO buffer before transferring additional data to the FIFO buffer.” Rosenthal ’930 at col. 24, ll. 51–65.</p>

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<p>[1i] notifies said first processing element to issue said command to said input queue; and</p>	<p>Rosenthal '930 teaches “notifies said first processing element to issue said command to said input queue,” including at least the following exemplary citations.</p> <p>For example, Rosenthal '930 teaches that the second processing element executes instructions that causes it to notify said first processing element to issue said command to said input queue, by disclosing, as non-limiting examples, reading the flow control register and determining if there is enough space. The processor running the application program notifies the first processing element to issue the command to the input queue. <i>See, e.g.:</i></p> <p>“A digital system which uses an arrangement of one or more parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available.” Rosenthal '930 at Abstract.</p> <p>“It is another object of the present invention to provide a flow control system for an architecture which utilizes FIFO buffers for buffering write operations.</p> <p>These and other objects of the present invention are realized in a system which uses an arrangement of parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the central processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal '930 at col. 2, ll. 15–33.</p> <p>“In one embodiment of the new architecture, a flow control register 45 is included for each FIFO buffer 39 of the input/output control unit 29. The register 45 stores an indication of the number of available spaces for commands in the associated FIFO buffer 39. The use of this flow control register 45 allows a requirement to be placed on an application program attempting an access of the input/output control unit 29 that it first determine whether space is available in the FIFO unit 31 before it writes any command. Before writing any</p>

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	<p>data, the application program must determine the amount of "free" space to which it may write. This it does by having the central processing unit read the value in the flow control register 45 associated with the FIFO buffer 39 being utilized. Once this value has been read, the application program may send up to that amount of data before it need test again to determine whether free space remains to which it may send more data.” Rosenthal ’930 at col. 16, ll. 33–49.</p> <p>“The use of the flow control register 45 allows an application program presently using the resources of the input/output control unit 29 to proceed without causing the overflow of the FIFO unit 31. Whenever the application has written commands totaling the amount previously read from the register 45, it must read the register again. This is especially useful for application programs which may wish to transfer a series of commands in sequence, possibly using the burst transfer mode of operation provided by many of the modern buses. By ascertaining the space available in the FIFO buffer 39 before transferring a sequence of commands, the application can know that sufficient space will be available for the operation. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal ’930 at col. 17, ll. 4–18.</p> <p>“Various operating conditions can cause the flow control register 45 associated with a buffer 39 to store different values. If the central processing unit is writing at a rate faster than the input/output device can handle the commands, then a FIFO buffer 39 which is initially empty and provides a maximum free count value when read by the central processing unit will provide a lower free count number after the amount of data first indicated by the free count register has been sent. This will occur because the FIFO buffer 39 will empty more slowly than it is filled. In such a case, the next value read by the application program after sending the amount of data designated by the free count register will be a smaller number. The application program may again send this amount of data and be sure that the FIFO buffer will not overflow. On the other hand, if the central processing unit is writing at a rate slower than the input/output device can handle the commands, then a FIFO buffer which is initially empty and provides a maximum free count value when read by the central processing unit, will provide the same free count number after the amount of data first indicated by the flow control register has been sent. This will occur because the FIFO will empty more rapidly than it is filled and will always be empty when the register 45 is read by the central processing unit.” Rosenthal ’930 at col. 17, ll. 19–42.</p> <p>“In one embodiment, the application program may obtain a free count value indicating the number of free entries in a FIFO buffer 39 by reading from a designated method offset in any of the sub-areas of the area mapped to the application program. The value read is that stored in the flow control register 45 associated</p>

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	<p>with the particular FIFO buffer 39. This value is then placed on the bus when the central processing unit provides the appropriate control signals to implement the read operation. The application may write up to the amount of data designated by this free count value without further testing and be certain that overflow of the FIFO buffer 39 will not occur.” Rosenthal ’930 at col. 18, ll. 16–27.</p> <p>“As with the embodiments which use one FIFO buffer for each application area, a free count register 45 and a puller are included with each FIFO buffer 39 as a part of the input/output control unit 29. The register 45 stores an indication of the number of available entries in each FIFO buffer 39 of the FIFO unit 31 and allows a requirement to be placed on an application program attempting to access the input/output control unit 29 that it first determine whether space is available in the FIFO unit 31. It also allows an application presently using the resources of the input/output control unit 29 to proceed without overflowing the FIFO unit 31. The application program may obtain a boundary value indicating the number of free entries in the FIFO buffer by reading from a designated offset in any of the sub-areas of its mapped area. The application may write up to the amount of data designated by this boundary value without further testing and be certain that overflow of the FIFO unit will not occur. As with the multiple FIFO buffer embodiments, the FIFO buffer arrangements of the described embodiment make use of a memory runout area; such a memory runout area assures that a FIFO buffer may be used to cache commands from a plurality of application programs. The use of a memory runout area also allows the system to make use of lying in order to enhance the speed of transfer by reducing the number of read operations by the central processing unit of the free count register 45.” Rosenthal ’930 at col. 22, ll. 27–52.</p> <p>“9. A method for controlling the flow of data in a data transfer path of a computer having a first-in first-out (FIFO) buffer with a plurality of stages positioned between a computer input-output bus and input/output devices, each stage providing storage for both data and a virtual address which are translated to provide a physical address for commands decoupled from application programs originating the commands, comprising the steps of:</p> <p>detecting a value indicating an amount of space available for data in the FIFO buffer,</p> <p>transferring to the FIFO buffer an amount of data up to an amount determine from the value detected, and</p> <p>detecting another value indicating an amount of space available for data in the FIFO buffer before transferring additional data to the FIFO buffer.” Rosenthal ’930 at col. 24, ll. 51–65.</p>

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<p>[1j] wherein said first processing element receives notification from said at least one second processing element regarding issuing the command, issues said command to said input queue, and receives a response corresponding to said command from said output queue.</p>	<p>Rosenthal '930 teaches “wherein said first processing element receives notification from said at least one second processing element regarding issuing the command, issues said command to said input queue, and receives a response corresponding to said command from said output queue,” including at least the following exemplary citations.</p> <p>For example, Rosenthal '930 teaches wherein said first processing element receives notification from said at least one second processing element regarding issuing the command, issues said command to said input queue, and receives a response corresponding to said command from said output queue, by disclosing, as non-limiting examples, that the processor running the application program receives the notification, issues the command, and receives a corresponding response from the output queue. <i>See, e.g.:</i></p> <p>“A digital system which uses an arrangement of one or more parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available.” Rosenthal '930 at Abstract.</p> <p>“It is another object of the present invention to provide a flow control system for an architecture which utilizes FIFO buffers for buffering write operations.</p> <p>These and other objects of the present invention are realized in a system which uses an arrangement of parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the central processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal '930 at col. 2, ll. 15–33.</p> <p>“When the operation involves a device directly associated with the control unit 29 on its device bus 34, the commands after the first commands (creating the new data structure, attaching its new virtual name, providing any necessary device context, and creating the address translation) are sent by hardware directly to that device</p>

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	<p>for execution. If the command requires that data be transferred to or from the application, the input/output device performs the transfer using the DMA unit 35. Upon the return of data in response to a command, the DMA unit 35 of the control unit 29 responds by transferring the data to main memory and notifying the central processing unit in a separate DMA operation of the existence of the data so that no local bus read operation by the central processing unit 21 is necessary to ascertain the result of the operation or to receive the data provided.” Rosenthal ’930 at col. 7, ll. 30–45.</p> <p>“In one embodiment of the new architecture, a flow control register 45 is included for each FIFO buffer 39 of the input/output control unit 29. The register 45 stores an indication of the number of available spaces for commands in the associated FIFO buffer 39. The use of this flow control register 45 allows a requirement to be placed on an application program attempting an access of the input/output control unit 29 that it first determine whether space is available in the FIFO unit 31 before it writes any command. Before writing any data, the application program must determine the amount of "free" space to which it may write. This it does by having the central processing unit read the value in the flow control register 45 associated with the FIFO buffer 39 being utilized. Once this value has been read, the application program may send up to that amount of data before it need test again to determine whether free space remains to which it may send more data.” Rosenthal ’930 at col. 16, ll. 33–49.</p> <p>“The use of the flow control register 45 allows an application program presently using the resources of the input/output control unit 29 to proceed without causing the overflow of the FIFO unit 31. Whenever the application has written commands totaling the amount previously read from the register 45, it must read the register again. This is especially useful for application programs which may wish to transfer a series of commands in sequence, possibly using the burst transfer mode of operation provided by many of the modern buses. By ascertaining the space available in the FIFO buffer 39 before transferring a sequence of commands, the application can know that sufficient space will be available for the operation. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal ’930 at col. 17, ll. 4–18.</p> <p>“Various operating conditions can cause the flow control register 45 associated with a buffer 39 to store different values. If the central processing unit is writing at a rate faster than the input/output device can handle the commands, then a FIFO buffer 39 which is initially empty and provides a maximum free count value when read by the central processing unit will provide a lower free count number after the amount of data first indicated by the free count register has been sent. This will occur because the FIFO buffer 39 will empty more slowly than it is filled. In such a case, the next value read by the application program after sending the</p>

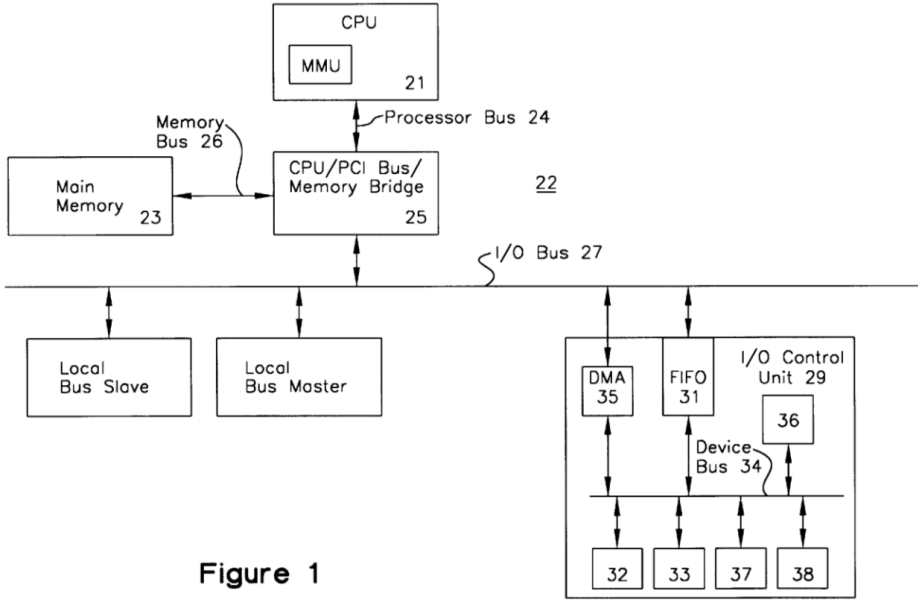
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	<p>amount of data designated by the free count register will be a smaller number. The application program may again send this amount of data and be sure that the FIFO buffer will not overflow. On the other hand, if the central processing unit is writing at a rate slower than the input/output device can handle the commands, then a FIFO buffer which is initially empty and provides a maximum free count value when read by the central processing unit, will provide the same free count number after the amount of data first indicated by the flow control register has been sent. This will occur because the FIFO will empty more rapidly than it is filled and will always be empty when the register 45 is read by the central processing unit.” Rosenthal ’930 at col. 17, ll. 19–42.</p> <p>“In one embodiment, the application program may obtain a free count value indicating the number of free entries in a FIFO buffer 39 by reading from a designated method offset in any of the sub-areas of the area mapped to the application program. The value read is that stored in the flow control register 45 associated with the particular FIFO buffer 39. This value is then placed on the bus when the central processing unit provides the appropriate control signals to implement the read operation. The application may write up to the amount of data designated by this free count value without further testing and be certain that overflow of the FIFO buffer 39 will not occur.” Rosenthal ’930 at col. 18, ll. 16–27.</p> <p>“As with the embodiments which use one FIFO buffer for each application area, a free count register 45 and a puller are included with each FIFO buffer 39 as a part of the input/output control unit 29. The register 45 stores an indication of the number of available entries in each FIFO buffer 39 of the FIFO unit 31 and allows a requirement to be placed on an application program attempting to access the input/output control unit 29 that it first determine whether space is available in the FIFO unit 31. It also allows an application presently using the resources of the input/output control unit 29 to proceed without overflowing the FIFO unit 31. The application program may obtain a boundary value indicating the number of free entries in the FIFO buffer by reading from a designated offset in any of the sub-areas of its mapped area. The application may write up to the amount of data designated by this boundary value without further testing and be certain that overflow of the FIFO unit will not occur. As with the multiple FIFO buffer embodiments, the FIFO buffer arrangements of the described embodiment make use of a memory runout area; such a memory runout area assures that a FIFO buffer may be used to cache commands from a plurality of application programs. The use of a memory runout area also allows the system to make use of lying in order to enhance the speed of transfer by reducing the number of read operations by the central processing unit of the free count register 45.” Rosenthal ’930 at col. 22, ll. 27–52.</p>

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	<p>“9. A method for controlling the flow of data in a data transfer path of a computer having a first-in first-out (FIFO) buffer with a plurality of stages positioned between a computer input-output bus and input/output devices, each stage providing storage for both data and a virtual address which are translated to provide a physical address for commands decoupled from application programs originating the commands, comprising the steps of:</p> <p>detecting a value indicating an amount of space available for data in the FIFO buffer,</p> <p>transferring to the FIFO buffer an amount of data up to an amount determine from the value detected, and</p> <p>detecting another value indicating an amount of space available for data in the FIFO buffer before transferring additional data to the FIFO buffer.” Rosenthal ’930 at col. 24, ll. 51–65.</p>
<p>2. The system of claim 1, wherein said input queue is a first-in-first-out (FIFO) buffer.</p>	<p>Rosenthal ’930 teaches “[t]he system of claim 1, wherein said input queue is a first-in-first-out (FIFO) buffer,” including at least the following exemplary citations.</p> <p>For example, Rosenthal ’930 teaches wherein said input queue is a first-in-first-out (FIFO) buffer, by disclosing, as non-limiting examples, a FIFO buffer. <i>See, e.g.:</i></p> <p>“A digital system which uses an arrangement of one or more parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available.” Rosenthal ’930 at Abstract.</p>

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	 <p data-bbox="772 813 905 846">Figure 1</p> <p data-bbox="583 862 932 894">Rosenthal '930 at Figure 1.</p>

Claim Language	Exemplary Evidence of Anticipation and/or Obviousness
	<div data-bbox="583 259 1459 820"><p>The diagram illustrates a system architecture. At the top, a horizontal line represents Bus 27. Below it, a box labeled 'Decode 30' is connected to Bus 27. To the right, a box labeled 'Input/Output Control Unit 29' is connected to Bus 27. Below Bus 27, a large box contains several components: 'MMU 50' with a sub-box '52' and 'DMA 35' are on the left. In the center is a 'Pusher 53' box with a grid of cells containing numbers 7, 3, 11, and 32. Below the pusher is a grid of dots labeled 39. To the right of the pusher is a box labeled 45. Below the pusher is a box labeled 40. A dashed box labeled 'Resource Manager' is to the right of the pusher. Below the Resource Manager is a box labeled 'Translation Table 38'. At the bottom, a horizontal line represents Bus 34. Below Bus 34 are three boxes: 'Disk Controller 32', 'Graphics Output Controller Memory 33', and 'Sound Generator 37'. Arrows indicate data flow between these components and the buses.</p></div> <p style="text-align: center;">Figure 3</p> <p>Rosenthal '930 at Figure 3.</p>

Claim Language	Exemplary Evidence of Anticipation and/or Obviousness
	<div data-bbox="585 261 1459 816"><p>The diagram illustrates a system architecture. At the top, a horizontal line represents Bus 27. Below it, a box labeled 'Decode 30' is connected to Bus 27. Below 'Decode 30' is a large box labeled 'Input/Output Control Unit 29'. Inside this unit, there is a 'Pusher 53' connected to Bus 27. To the left of 'Pusher 53' is a box labeled 'MMU 50' containing a sub-box '52'. Below 'MMU 50' is a box labeled 'DMA 35'. To the right of 'Pusher 53' is a grid of boxes labeled 3, 11, and 32. Below this grid is a box labeled 45, which is connected to a box labeled 49. Below 49 is a box labeled 40. To the right of 40 is a box labeled 'Translation Table 38'. Below the 'Input/Output Control Unit 29' is a horizontal line representing Bus 34. Below Bus 34 are three boxes: 'Disk Controller 32', 'Graphics Output Controller Memory 33', and 'Sound Generator 37'. A dashed box labeled 'Resource Manager' is connected to the 'Translation Table 38' and the 'Disk Controller 32'. A dashed box labeled 36 is connected to the 'DMA 35' and the 'Disk Controller 32'. A dashed box labeled 31 is connected to the 'Translation Table 38' and the 'Sound Generator 37'. A dashed box labeled 7 is connected to the 'MMU 50' and the 'Disk Controller 32'. A dashed box labeled 42 is connected to the 'Pusher 53' and the 'Disk Controller 32'.</p></div> <p style="text-align: center;">Figure 6</p> <p>Rosenthal '930 at Figure 6.</p>

Claim Language	Exemplary Evidence of Anticipation and/or Obviousness
	<div data-bbox="583 258 968 753"> <p>The flowchart in Figure 7 illustrates a data processing sequence. It begins with a 'From decode' input (71) leading to a 'Match area I.D.?' decision (73). If 'no', it proceeds to an 'Overflow' state. If 'yes', it goes to 'Area already in runout?' (75). If 'yes' here, it also leads to 'Overflow'. If 'no', it checks 'Space available?' (77). If 'no', it leads to 'Overflow'. If 'yes', it proceeds to a 'FIFO Unit 31'. The FIFO Unit 31 has inputs 3, 11, and 32, and an output 38. The output 38 leads to a 'Special value' decision (40). If 'yes', it leads to an 'Interrupt'. If 'no', it goes to a 'method' decision (41). The 'method' decision (41) has two paths: 'device add.' leading to 'Device Bus 34' and 'data' leading to another 'device add.' block, which then leads to 'Device Bus 34'. There are also feedback loops from the 'Overflow' states back to the 'From decode' input (71) and from the 'Special value' decision (40) back to the 'FIFO Unit 31'.</p> </div> <div data-bbox="583 834 930 891"> <p>Figure 7 Rosenthal '930 at Figure 7.</p> </div> <div data-bbox="583 914 1971 1128"> <p>“Since most central processing unit accesses to input/output devices are write operations, the designers of systems and input/output devices attempt to decouple the central processing unit and input/output devices as far as write operations are concerned by implementing write queues using first-in first-out (FIFO) write buffers. These buffers may appear at various places in a particular implementation: as a part of the central processing unit, as part of a bridge chip, or as part of an input/output device.” Rosenthal '930 at col. 1, ll. 45–53.</p> </div> <div data-bbox="583 1149 1971 1399"> <p>“One problem raised in systems using FIFO buffers is that an input/output device and the buffers supplying it must accept all information written to them over the input/output bus. Although some input/output buses allow devices to "hold off" writes, that is, delay the completion of the write operation until the device has enough resources available to store the data, there is always a limit to how long a write can be held off. If a write is held off too long the data will be lost. In the limit, the input/output device has no alternative but to store all data written to it. In a system utilizing FIFO buffers for storage of this data at the input/output device, the FIFO buffers must ultimately store the data.” Rosenthal '930 at col. 1, ll. 54–65.</p> </div>

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Claim Language	Exemplary Evidence of Anticipation and/or Obviousness
	<p>“It is another object of the present invention to provide a flow control system for an architecture which utilizes FIFO buffers for buffering write operations.</p> <p>These and other objects of the present invention are realized in a system which uses an arrangement of parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the central processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal ’930 at col. 2, ll. 15–33.</p> <p>“In the architecture of system 22, an input/output control unit 29 is shown joined to the input/output bus 27. The control unit 29 includes a hardware FIFO unit 31 for receiving incoming commands addressed to the input/output devices on a device bus 34.” Rosenthal ’930 at col. 4, ll. 60–64.</p> <p>“In one embodiment, the FIFO unit 31 includes a plurality of FIFO buffers 39 (see FIG. 3). When an application program desires to write to an input/output device on the device bus 34, it addresses that device. Decoding circuitry decodes the address by reviewing a number of the highest order bits decoded by the chip sufficient to indicate a unique portion of the input/output address space assigned to an application program and places the command in the appropriate FIFO buffer 39 for that application program. Each FIFO buffer 39 handles commands only from the application program to which the address area has been mapped. An arrangement using a smaller number of FIFO buffers 39 than one buffer for each application program (as few as a single buffer 39) could also be utilized as long as the address of the FIFO buffer is mapped to only one application program at a time.” Rosenthal ’930 at col. 5, ll. 51–66.</p> <p>“The unit 29 receives physical addresses furnished by the memory management unit and virtual names furnished by application programs for operations to be performed which have been sent to the FIFO unit 31 and controls the translation of those virtual names for all input/output devices. The hardware unit 29 includes the device bus 34 to which the individual input/output devices such as a disk controller 32, a graphics output controller 33, and a sound generator 37 are shown joined. The unit 29 also includes a DMA unit 35 which is adapted to transfer data between the individual input/output devices and main memory for use by the central processing unit or other components of the system.” Rosenthal ’930 at col. 5, l. 67 – col. 6, l. 10.</p>

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Claim Language	Exemplary Evidence of Anticipation and/or Obviousness
	<p>“FIG. 3 is a block diagram illustrating details of the input/output control unit 29 including the device bus 34 and the input/output devices arranged on that bus. As described above, the input/output control unit 29 includes a decode unit 30 which receives commands directly from the input/output bus 27 and transfers the commands to a pusher circuit 53 which transfers the command to one of the FIFO buffers 39 of the FIFO unit 31. The FIFO unit 31 stores the data along with the addresses for each of the commands being transferred to all of the input/output devices associated with the input/output control unit 29. The buffers 39 of the FIFO unit replace the individual data registers used by the input/output devices of the prior art. However, in contrast to the registers used by the prior art for communication on the input/output bus 27, the FIFO unit 31 allows a very much larger number of commands to be processed much more rapidly and facilitates the asynchronous operations of the input/output devices and the central processing unit. In one embodiment, the FIFO unit 31 includes 128 individual FIFO buffers 39 each of which has thirty-two stages. The use of 128 individual FIFO buffers 39 allows a FIFO buffer to be assigned to each of 128 different application programs which may be running on the central processing unit for the use of that application program alone. The thirty-two stages of each buffer 39 allow any FIFO buffer to hold thirty-two individual serially ordered commands at any time. Although each of the stages of the FIFO unit 31 holds (along with the address bits) the data held by an individual register of a typical prior art input/output device, a particular system has the ability to store commands for over 16 thousand 32 bit registers for each of 128 different application programs which may map different addresses decoded by the input/output control unit 29.” Rosenthal ’930 at col. 8, ll. 21–53.</p> <p>“Thus, as may be seen, the resource manager is a piece of software which is associated with the input/output control unit 29 and determines that the input/output control unit 29 functions correctly. It maintains a database of data structures which represent the various input/output devices and the context that those devices require to function correctly. It fills the translation table 38, does the necessary context switching for initializing the physical devices, provides routines for less used input/output operations which input/output devices may invoke through interrupts, and does other things required to run the input/output control unit 29. The resource manager may be thought of as part of the operating system and takes the place of the device driver used in a conventional input/output system. The resource manager maps in a part of the physical hardware of the input/output control unit 29 called the privileged address space. This space is distinct from the FIFO unit. Unlike the application programs operating with input/output devices, the resource manager both reads and writes this address space to perform its various tasks such as context switching. Unlike all of the device drivers of the prior art, the resource manager accomplishes its functions after the hardware of the input/output control unit 29 has been directly addressed by an application program rather than before. Moreover, in the overall operation of the input/output control unit 29, the resource manager is used infrequently compared to</p>

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	<p>the hardware portions of the input/output control unit 29 since the resource manager attends only to creation operations, the various software implementations of methods, and unsafe operations.” Rosenthal ’930 at col. 15, ll. 35–64.</p> <p>“The use of the flow control register 45 allows an application program presently using the resources of the input/output control unit 29 to proceed without causing the overflow of the FIFO unit 31. Whenever the application has written commands totaling the amount previously read from the register 45, it must read the register again. This is especially useful for application programs which may wish to transfer a series of commands in sequence, possibly using the burst transfer mode of operation provided by many of the modern buses. By ascertaining the space available in the FIFO buffer 39 before transferring a sequence of commands, the application can know that sufficient space will be available for the operation. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal ’930 at col. 17, ll. 4–18.</p> <p>“One embodiment of the new architecture provides a means for attaining almost the same speed as is possible with 128 FIFO buffers but much more economically. Instead of 128 individual FIFO buffers 39, the described embodiment utilizes a smaller number of FIFO buffers 39 than the number of areas into which the input/output address space may be divided and thus the number of application programs which may be run. Utilizing a smaller number of FIFO buffers causes each FIFO buffer to function as a cache for commands which may be sent by any of the application programs. In the preferred embodiment, one FIFO buffer 39 is used for each processor which may be writing to the input/output control unit 29. For example, if the computer utilizes two processors arranged as symmetrical multi-processors, then two individual FIFO buffers are utilized. If, as is usually the case, only a single central processing unit is used, then a single FIFO buffer 39 may in the limit act as a cache for commands from all application programs which may be running on the central processing unit. Such an arrangement is illustrated in FIG. 6. Of course, in either case more FIFO buffers might be used.” Rosenthal ’930 at col. 21, l. 53 – col. 22, l. 6.</p> <p>“As with the embodiments which use one FIFO buffer for each application area, a free count register 45 and a puller are included with each FIFO buffer 39 as a part of the input/output control unit 29. The register 45 stores an indication of the number of available entries in each FIFO buffer 39 of the FIFO unit 31 and allows a requirement to be placed on an application program attempting to access the input/output control unit 29 that it first determine whether space is available in the FIFO unit 31. It also allows an application presently using the resources of the input/output control unit 29 to proceed without overflowing the FIFO unit 31. The application program may obtain a boundary value indicating the number of free entries in the FIFO buffer by</p>

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	<p>reading from a designated offset in any of the sub-areas of its mapped area. The application may write up to the amount of data designated by this boundary value without further testing and be certain that overflow of the FIFO unit will not occur. As with the multiple FIFO buffer embodiments, the FIFO buffer arrangements of the described embodiment make use of a memory runout area; such a memory runout area assures that a FIFO buffer may be used to cache commands from a plurality of application programs. The use of a memory runout area also allows the system to make use of lying in order to enhance the speed of transfer by reducing the number of read operations by the central processing unit of the free count register 45.” Rosenthal ’930 at col. 22, ll. 27–52.</p> <p>“a first-in first-out (FIFO) circuit positioned between a computer input-output bus and input/output devices in the computer and having a plurality of stages, each stage providing storage for commands sent directly from application programs including both data and a virtual address for the data which together translate to provide a physical address for the command, and” Rosenthal ’930 at col. 24, ll. 5–11.</p> <p>“9. A method for controlling the flow of data in a data transfer path of a computer having a first-in first-out (FIFO) buffer with a plurality of stages positioned between a computer input-output bus and input/output devices, each stage providing storage for both data and a virtual address which are translated to provide a physical address for commands decoupled from application programs originating the commands, comprising the steps of:</p> <p>detecting a value indicating an amount of space available for data in the FIFO buffer,</p> <p>transferring to the FIFO buffer an amount of data up to an amount determine from the value detected, and</p> <p>detecting another value indicating an amount of space available for data in the FIFO buffer before transferring additional data to the FIFO buffer.” Rosenthal ’930 at col. 24, ll. 51–65.</p>
3. The system of claim 1, wherein said system is part of a storage area network (SAN) controller.	
4. The system of claim 1, wherein said system is part of a network attached storage (NAS) controller.	

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<p>5. The system of claim 1, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element.</p>	<p>Rosenthal '930 teaches “[t]he system of claim 1, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element,” including at least the following exemplary citations.</p> <p>For example, Rosenthal '930 teaches wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element by disclosing, as non-limiting examples, the application program deducting the number of writes it has performed before needing to read the flow control register again. The application program decrements the stored value by a predefined value. <i>See, e.g.:</i></p> <p>“Various operating conditions can cause the flow control register 45 associated with a buffer 39 to store different values. If the central processing unit is writing at a rate faster than the input/output device can handle the commands, then a FIFO buffer 39 which is initially empty and provides a maximum free count value when read by the central processing unit will provide a lower free count number after the amount of data first indicated by the free count register has been sent. This will occur because the FIFO buffer 39 will empty more slowly than it is filled. In such a case, the next value read by the application program after sending the amount of data designated by the free count register will be a smaller number. The application program may again send this amount of data and be sure that the FIFO buffer will not overflow. On the other hand, if the central processing unit is writing at a rate slower than the input/output device can handle the commands, then a FIFO buffer which is initially empty and provides a maximum free count value when read by the central processing unit, will provide the same free count number after the amount of data first indicated by the flow control register has been sent. This will occur because the FIFO will empty more rapidly than it is filled and will always be empty when the register 45 is read by the central processing unit.” Rosenthal '930 at col. 17, ll. 19–42.</p> <p>“In utilizing the free count value, the application program should deduct the value of any data which it has already written before each new write operation commences. In this manner, the application program knows at any time the amount of data which it may still write to the input/output device before another read of the free count register will be required. This allows a number of write operations to occur before a read of the register 45 (which significantly slows operation of the overall system) need occur. This also assures that any writes which might be presently in the write channel on the input/output bus are accounted for in determining the actual value of the free count left. It should be noted that this read of the free count register is the only read necessary in dealing with the input/output control unit 29. It would be possible either to interrupt the central processing unit if a FIFO buffer 39 filled or to use the DMA unit 35 to transfer the value in the free</p>

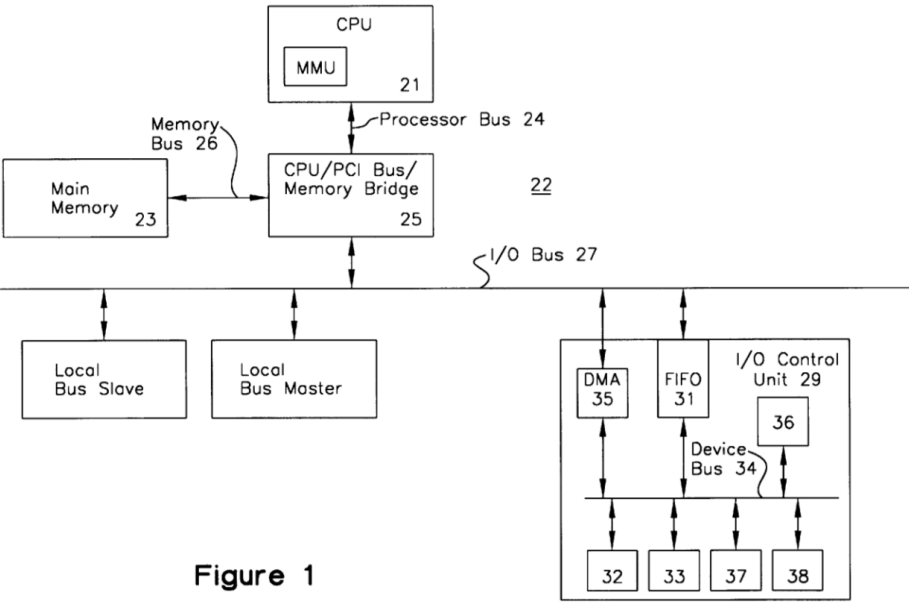
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	<p>count register to the central processing unit instead of reading the value, but in the particular embodiment reading the free count register appears to be the fastest operation.” Rosenthal ’930 at col. 17, l. 52 – col. 18, l. 4.</p>
<p>6. The system of claim 1, wherein at least one third processing element executes said command and notifies said output queue to issue said response.</p>	<p>Rosenthal ’930 teaches “[t]he system of claim 1, wherein at least one third processing element executes said command and notifies said output queue to issue said response,” including at least the following exemplary citations.</p> <p>For example, Rosenthal ’930 teaches wherein at least one third processing element executes said command and notifies said output queue to issue said response, by disclosing, as non-limiting examples, a DMA device. The DMA device executes the command and notifies the output queue to issue a response. <i>See, e.g.:</i></p> <p>“To help maintain this asynchronous operating arrangement and to eliminate read operations to the extent possible, the input/output control unit also includes an advanced direct memory access (DMA) device 35 which provides direct memory access for operations conducted involving input/output devices. The DMA device 35 allows the results of input/output operations to be written from input/output devices to main memory 23 rather than requiring read operations by the central processing unit 21 to obtain these results. This eliminates almost all need for the central processing unit 21 to read input/output devices and drastically increases the overall speed of input/output operations. The DMA device 35 includes its own memory management unit which allows writes from input/output devices to the virtual memory space of an application without involving the operating system in the translation process.” Rosenthal ’930 at col. 4, ll. 12–27.</p> <p>“When the operation involves a device directly associated with the control unit 29 on its device bus 34, the commands after the first commands (creating the new data structure, attaching its new virtual name, providing any necessary device context, and creating the address translation) are sent by hardware directly to that device for execution. If the command requires that data be transferred to or from the application, the input/output device performs the transfer using the DMA unit 35. Upon the return of data in response to a command, the DMA unit 35 of the control unit 29 responds by transferring the data to main memory and notifying the central processing unit in a separate DMA operation of the existence of the data so that no local bus read operation by the central processing unit 21 is necessary to ascertain the result of the operation or to receive the data provided.” Rosenthal ’930 at col. 7, ll. 30–45.</p>
<p>[7pre] A system for dividing and synchronizing a processing task</p>	<p>Rosenthal ’930 teaches “[a] system for dividing and synchronizing a processing task across a plurality of processing elements,” including at least the following exemplary citations.</p>

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across a plurality of processing elements comprising:	<i>See</i> above at row [1pre].
[7a] an input queue implemented in hardware;	Rosenthal '930 teaches “an input queue implemented in hardware,” including at least the following exemplary citations. <i>See</i> above at row [1a].
[7b] an output queue implemented in hardware;	Rosenthal '930 teaches “an output queue implemented in hardware,” including at least the following exemplary citations. <i>See</i> above at row [1b].
[7c] a first processing element having access to said input queue and said output queue;	Rosenthal '930 teaches “a first processing element having access to said input queue and said output queue,” including at least the following exemplary citations. <i>See</i> above at row [1c].
[7d] at least one second processing element in communication with said input queue;	Rosenthal '930 teaches “at least one second processing element in communication with said input queue,” including at least the following exemplary citations. For example, Rosenthal '930 teaches at least one second processing element in communication with said input queue, by disclosing, as non-limiting examples, an I/O control unit. The I/O control unit, the second processing element is in communication with the input queue. <i>See, e.g.:</i>

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	 <p style="text-align: center;">Figure 1 Rosenthal '930 at Figure 1.</p>

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	<div><pre>graph TD; AP[Application Program] --> S[System]; S --> ID1[I/O Driver #1]; ID1 --> IOCU[Input/Output Control Unit 29]; AP --> IOCU; S --> ID2[I/O Driver #2]; ID2 --> RM[I/O Driver #2 Resource Manager]; RM --> IOCU;</pre><p>The diagram illustrates a system architecture. At the top is a box labeled 'Application Program'. An arrow points down from it to a box labeled 'System'. From the 'System' box, an arrow points down to a box labeled 'I/O Driver #1'. From 'I/O Driver #1', an arrow points down to a wide box at the bottom labeled 'Input/Output Control Unit 29'. A second arrow points down from the 'Application Program' box directly to the 'Input/Output Control Unit 29' box. To the right of the 'System' box, there is a box labeled 'I/O Driver #2' with 'Resource Manager' written below it. An arrow points from the 'System' box to this box. From the 'I/O Driver #2' box, an arrow points down to the 'Input/Output Control Unit 29' box.</p></div> <p>Figure 2 Rosenthal '930 at Figure 2.</p>

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	<p style="text-align: center;">Figure 6</p> <p>Rosenthal '930 at Figure 6.</p>

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	<p style="text-align: center;">Figure 7 Rosenthal '930 at Figure 7.</p> <p>“It is another object of the present invention to provide a flow control system for an architecture which utilizes FIFO buffers for buffering write operations.</p> <p>These and other objects of the present invention are realized in a system which uses an arrangement of parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the central processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal '930 at col. 2, ll. 15–33.</p> <p>“The architecture of the system 22 has been designed so that it eliminates almost all read operations of input/output devices by the central processing unit. In order to accomplish this, the input/output control unit 29 includes a first-in first-out (FIFO) unit 31 for storing write operations directed to the input/output control</p>

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	<p>unit. The FIFO unit 31 queues incoming write operations. Unlike FIFO units in prior art systems, it stores both addresses and data. This allows the write operations to the input/output control unit 29 to occur asynchronously so that both the central processing unit 21 and the input/output control unit 29 may be functioning independently of one another and neither need wait for operations of the other.” Rosenthal ’930 at col. 3, l. 66 – col. 4, l. 11.</p> <p>“In one embodiment, the FIFO unit 31 includes a plurality of FIFO buffers 39 (see FIG. 3). When an application program desires to write to an input/output device on the device bus 34, it addresses that device. Decoding circuitry decodes the address by reviewing a number of the highest order bits decoded by the chip sufficient to indicate a unique portion of the input/output address space assigned to an application program and places the command in the appropriate FIFO buffer 39 for that application program. Each FIFO buffer 39 handles commands only from the application program to which the address area has been mapped. An arrangement using a smaller number of FIFO buffers 39 than one buffer for each application program (as few as a single buffer 39) could also be utilized as long as the address of the FIFO buffer is mapped to only one application program at a time.” Rosenthal ’930 at col. 5, ll. 51–66.</p> <p>“The unit 29 receives physical addresses furnished by the memory management unit and virtual names furnished by application programs for operations to be performed which have been sent to the FIFO unit 31 and controls the translation of those virtual names for all input/output devices. The hardware unit 29 includes the device bus 34 to which the individual input/output devices such as a disk controller 32, a graphics output controller 33, and a sound generator 37 are shown joined. The unit 29 also includes a DMA unit 35 which is adapted to transfer data between the individual input/output devices and main memory for use by the central processing unit or other components of the system.” Rosenthal ’930 at col. 5, l. 67 – col. 6, l. 10.</p> <p>“FIG. 3 is a block diagram illustrating details of the input/output control unit 29 including the device bus 34 and the input/output devices arranged on that bus. As described above, the input/output control unit 29 includes a decode unit 30 which receives commands directly from the input/output bus 27 and transfers the commands to a pusher circuit 53 which transfers the command to one of the FIFO buffers 39 of the FIFO unit 31. The FIFO unit 31 stores the data along with the addresses for each of the commands being transferred to all of the input/output devices associated with the input/output control unit 29. The buffers 39 of the FIFO unit replace the individual data registers used by the input/output devices of the prior art. However, in contrast to the registers used by the prior art for communication on the input/output bus 27, the FIFO unit 31 allows a very much larger number of commands to be processed much more rapidly and facilitates the asynchronous operations of the input/output devices and the central processing unit. In one embodiment, the FIFO unit 31</p>

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	<p>includes 128 individual FIFO buffers 39 each of which has thirty-two stages. The use of 128 individual FIFO buffers 39 allows a FIFO buffer to be assigned to each of 128 different application programs which may be running on the central processing unit for the use of that application program alone. The thirty-two stages of each buffer 39 allow any FIFO buffer to hold thirty-two individual serially ordered commands at any time. Although each of the stages of the FIFO unit 31 holds (along with the address bits) the data held by an individual register of a typical prior art input/output device, a particular system has the ability to store commands for over 16 thousand 32 bit registers for each of 128 different application programs which may map different addresses decoded by the input/output control unit 29.” Rosenthal ’930 at col. 8, ll. 21–53.</p> <p>“The use of the flow control register 45 allows an application program presently using the resources of the input/output control unit 29 to proceed without causing the overflow of the FIFO unit 31. Whenever the application has written commands totaling the amount previously read from the register 45, it must read the register again. This is especially useful for application programs which may wish to transfer a series of commands in sequence, possibly using the burst transfer mode of operation provided by many of the modern buses. By ascertaining the space available in the FIFO buffer 39 before transferring a sequence of commands, the application can know that sufficient space will be available for the operation. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal ’930 at col. 17, ll. 4–18.</p> <p>“Various operating conditions can cause the flow control register 45 associated with a buffer 39 to store different values. If the central processing unit is writing at a rate faster than the input/output device can handle the commands, then a FIFO buffer 39 which is initially empty and provides a maximum free count value when read by the central processing unit will provide a lower free count number after the amount of data first indicated by the free count register has been sent. This will occur because the FIFO buffer 39 will empty more slowly than it is filled. In such a case, the next value read by the application program after sending the amount of data designated by the free count register will be a smaller number. The application program may again send this amount of data and be sure that the FIFO buffer will not overflow. On the other hand, if the central processing unit is writing at a rate slower than the input/output device can handle the commands, then a FIFO buffer which is initially empty and provides a maximum free count value when read by the central processing unit, will provide the same free count number after the amount of data first indicated by the flow control register has been sent. This will occur because the FIFO will empty more rapidly than it is filled and will always be empty when the register 45 is read by the central processing unit.” Rosenthal ’930 at col. 17, ll. 19–42.</p>

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	<p>“Those skilled in the art will recognize that the use of 128 individual FIFO buffers 39 to receive commands written by the central processing unit is very expensive and probably not economically feasible for use with personal computers. In addition, it is expensive of system resources for an operating system to context switch the central processing unit from one application program to another. Thus, the operating system will try to ensure that once an application is given the central processing unit the application will retain control long enough to amortize the cost of the context switch. This means that typically in a one processor system at most one FIFO buffer will be active at a time. In a multi-processor system, typically at most as many FIFO buffers will be active as there are processors.” Rosenthal ’930 at col. 21, ll. 39–52.</p> <p>“One embodiment of the new architecture provides a means for attaining almost the same speed as is possible with 128 FIFO buffers but much more economically. Instead of 128 individual FIFO buffers 39, the described embodiment utilizes a smaller number of FIFO buffers 39 than the number of areas into which the input/output address space may be divided and thus the number of application programs which may be run. Utilizing a smaller number of FIFO buffers causes each FIFO buffer to function as a cache for commands which may be sent by any of the application programs. In the preferred embodiment, one FIFO buffer 39 is used for each processor which may be writing to the input/output control unit 29. For example, if the computer utilizes two processors arranged as symmetrical multi-processors, then two individual FIFO buffers are utilized. If, as is usually the case, only a single central processing unit is used, then a single FIFO buffer 39 may in the limit act as a cache for commands from all application programs which may be running on the central processing unit. Such an arrangement is illustrated in FIG. 6. Of course, in either case more FIFO buffers might be used.” Rosenthal ’930 at col. 21, l. 53 – col. 22, l. 6.</p> <p>“9. A method for controlling the flow of data in a data transfer path of a computer having a first-in first-out (FIFO) buffer with a plurality of stages positioned between a computer input-output bus and input/output devices, each stage providing storage for both data and a virtual address which are translated to provide a physical address for commands decoupled from application programs originating the commands, comprising the steps of:</p> <p>detecting a value indicating an amount of space available for data in the FIFO buffer,</p> <p>transferring to the FIFO buffer an amount of data up to an amount determine from the value detected, and</p> <p>detecting another value indicating an amount of space available for data in the FIFO buffer before transferring additional data to the FIFO buffer.” Rosenthal ’930 at col. 24, ll. 51–65.</p>

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<p>[7e] a reservation register implemented in hardware storing a value indicative of available space in said input queue, said reservation register accessible by both said first processing element and said at least one second processing element;</p>	<p>Rosenthal '930 teaches “a reservation register implemented in hardware storing a value indicative of available space in said input queue, said reservation register accessible by both said first processing element and said at least one second processing element,” including at least the following exemplary citations.</p> <p><i>See above at row [1e].</i></p>
<p>[7f] computer storage storing instructions, which when executed by said at least one second processing element:</p>	<p>Rosenthal '930 teaches computer storage storing instructions executed by said at least one second processing element, including at least the following exemplary citations.</p> <p><i>See above at row [1f].</i></p>
<p>[7g] receives a command from said first processing element;</p>	<p>Rosenthal '930 teaches “receives a command from said first processing element,” including at least the following exemplary citations.</p> <p>For example, Rosenthal '930 teaches that the second processing element executes instructions that causes it to receive a command from said first processing element, by disclosing, as non-limiting examples, the CPU sending commands to the I/O unit. The I/O unit, the second processing element receives a command from the first processing element. <i>See, e.g.:</i></p> <p>“A digital system which uses an arrangement of one or more parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available.” Rosenthal '930 at Abstract.</p> <p>“It is another object of the present invention to provide a flow control system for an architecture which utilizes FIFO buffers for buffering write operations.</p>

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	<p>These and other objects of the present invention are realized in a system which uses an arrangement of parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the central processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal ’930 at col. 2, ll. 15–33.</p> <p>“The use of the flow control register 45 allows an application program presently using the resources of the input/output control unit 29 to proceed without causing the overflow of the FIFO unit 31. Whenever the application has written commands totaling the amount previously read from the register 45, it must read the register again. This is especially useful for application programs which may wish to transfer a series of commands in sequence, possibly using the burst transfer mode of operation provided by many of the modern buses. By ascertaining the space available in the FIFO buffer 39 before transferring a sequence of commands, the application can know that sufficient space will be available for the operation. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal ’930 at col. 17, ll. 4–18.</p> <p>“In one embodiment, the application program may obtain a free count value indicating the number of free entries in a FIFO buffer 39 by reading from a designated method offset in any of the sub-areas of the area mapped to the application program. The value read is that stored in the flow control register 45 associated with the particular FIFO buffer 39. This value is then placed on the bus when the central processing unit provides the appropriate control signals to implement the read operation. The application may write up to the amount of data designated by this free count value without further testing and be certain that overflow of the FIFO buffer 39 will not occur.” Rosenthal ’930 at col. 18, ll. 16–27.</p> <p>“As with the embodiments which use one FIFO buffer for each application area, a free count register 45 and a puller are included with each FIFO buffer 39 as a part of the input/output control unit 29. The register 45 stores an indication of the number of available entries in each FIFO buffer 39 of the FIFO unit 31 and allows a requirement to be placed on an application program attempting to access the input/output control unit 29 that it first determine whether space is available in the FIFO unit 31. It also allows an application presently using the resources of the input/output control unit 29 to proceed without overflowing the FIFO unit 31. The</p>

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	<p>application program may obtain a boundary value indicating the number of free entries in the FIFO buffer by reading from a designated offset in any of the sub-areas of its mapped area. The application may write up to the amount of data designated by this boundary value without further testing and be certain that overflow of the FIFO unit will not occur. As with the multiple FIFO buffer embodiments, the FIFO buffer arrangements of the described embodiment make use of a memory runout area; such a memory runout area assures that a FIFO buffer may be used to cache commands from a plurality of application programs. The use of a memory runout area also allows the system to make use of lying in order to enhance the speed of transfer by reducing the number of read operations by the central processing unit of the free count register 45.” Rosenthal ’930 at col. 22, ll. 27–52.</p> <p>“9. A method for controlling the flow of data in a data transfer path of a computer having a first-in first-out (FIFO) buffer with a plurality of stages positioned between a computer input-output bus and input/output devices, each stage providing storage for both data and a virtual address which are translated to provide a physical address for commands decoupled from application programs originating the commands, comprising the steps of:</p> <p>detecting a value indicating an amount of space available for data in the FIFO buffer,</p> <p>transferring to the FIFO buffer an amount of data up to an amount determine from the value detected, and</p> <p>detecting another value indicating an amount of space available for data in the FIFO buffer before transferring additional data to the FIFO buffer.” Rosenthal ’930 at col. 24, ll. 51–65.</p>
[7h] accesses said reservation register and reads said stored value;	<p>Rosenthal ’930 teaches “accesses said reservation register and reads said stored value,” including at least the following exemplary citations.</p> <p><i>See above at row [1g].</i></p>
[7i] determines when said read value indicates available space in said input queue to issue said command;	<p>Rosenthal ’930 teaches “determines when said read value indicates available space in said input queue to issue said command,” including at least the following exemplary citations.</p> <p><i>See above at row [1h].</i></p>

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<p>[7j] issues said command to said input queue on behalf of said first processing element; and</p>	<p>Rosenthal '930 teaches “issues said command to said input queue on behalf of said first processing element,” including at least the following exemplary citations.</p> <p>For example, Rosenthal '930 teaches that the second processing element executes instructions that causes it to issue said command to said input queue on behalf of said first processing element, by disclosing, as non-limiting examples, an I/O control unit that issues the command. The I/O control unit issues the command to the input queue on behalf of the first processing element. <i>See, e.g.:</i></p> <p>“A digital system which uses an arrangement of one or more parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available.” Rosenthal '930 at Abstract.</p> <p>“It is another object of the present invention to provide a flow control system for an architecture which utilizes FIFO buffers for buffering write operations.</p> <p>These and other objects of the present invention are realized in a system which uses an arrangement of parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the central processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal '930 at col. 2, ll. 15–33.</p> <p>“In one embodiment of the new architecture, a flow control register 45 is included for each FIFO buffer 39 of the input/output control unit 29. The register 45 stores an indication of the number of available spaces for commands in the associated FIFO buffer 39. The use of this flow control register 45 allows a requirement to be placed on an application program attempting an access of the input/output control unit 29 that it first determine whether space is available in the FIFO unit 31 before it writes any command. Before writing any data, the application program must determine the amount of "free" space to which it may write. This it does</p>

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	<p>by having the central processing unit read the value in the flow control register 45 associated with the FIFO buffer 39 being utilized. Once this value has been read, the application program may send up to that amount of data before it need test again to determine whether free space remains to which it may send more data.” Rosenthal ’930 at col. 16, ll. 33–49.</p> <p>“The use of the flow control register 45 allows an application program presently using the resources of the input/output control unit 29 to proceed without causing the overflow of the FIFO unit 31. Whenever the application has written commands totaling the amount previously read from the register 45, it must read the register again. This is especially useful for application programs which may wish to transfer a series of commands in sequence, possibly using the burst transfer mode of operation provided by many of the modern buses. By ascertaining the space available in the FIFO buffer 39 before transferring a sequence of commands, the application can know that sufficient space will be available for the operation. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal ’930 at col. 17, ll. 4–18.</p> <p>“Various operating conditions can cause the flow control register 45 associated with a buffer 39 to store different values. If the central processing unit is writing at a rate faster than the input/output device can handle the commands, then a FIFO buffer 39 which is initially empty and provides a maximum free count value when read by the central processing unit will provide a lower free count number after the amount of data first indicated by the free count register has been sent. This will occur because the FIFO buffer 39 will empty more slowly than it is filled. In such a case, the next value read by the application program after sending the amount of data designated by the free count register will be a smaller number. The application program may again send this amount of data and be sure that the FIFO buffer will not overflow. On the other hand, if the central processing unit is writing at a rate slower than the input/output device can handle the commands, then a FIFO buffer which is initially empty and provides a maximum free count value when read by the central processing unit, will provide the same free count number after the amount of data first indicated by the flow control register has been sent. This will occur because the FIFO will empty more rapidly than it is filled and will always be empty when the register 45 is read by the central processing unit.” Rosenthal ’930 at col. 17, ll. 19–42.</p> <p>“In one embodiment, the application program may obtain a free count value indicating the number of free entries in a FIFO buffer 39 by reading from a designated method offset in any of the sub-areas of the area mapped to the application program. The value read is that stored in the flow control register 45 associated with the particular FIFO buffer 39. This value is then placed on the bus when the central processing unit</p>

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	<p>provides the appropriate control signals to implement the read operation. The application may write up to the amount of data designated by this free count value without further testing and be certain that overflow of the FIFO buffer 39 will not occur.” Rosenthal ’930 at col. 18, ll. 16–27.</p> <p>“As with the embodiments which use one FIFO buffer for each application area, a free count register 45 and a puller are included with each FIFO buffer 39 as a part of the input/output control unit 29. The register 45 stores an indication of the number of available entries in each FIFO buffer 39 of the FIFO unit 31 and allows a requirement to be placed on an application program attempting to access the input/output control unit 29 that it first determine whether space is available in the FIFO unit 31. It also allows an application presently using the resources of the input/output control unit 29 to proceed without overflowing the FIFO unit 31. The application program may obtain a boundary value indicating the number of free entries in the FIFO buffer by reading from a designated offset in any of the sub-areas of its mapped area. The application may write up to the amount of data designated by this boundary value without further testing and be certain that overflow of the FIFO unit will not occur. As with the multiple FIFO buffer embodiments, the FIFO buffer arrangements of the described embodiment make use of a memory runout area; such a memory runout area assures that a FIFO buffer may be used to cache commands from a plurality of application programs. The use of a memory runout area also allows the system to make use of lying in order to enhance the speed of transfer by reducing the number of read operations by the central processing unit of the free count register 45.” Rosenthal ’930 at col. 22, ll. 27–52.</p> <p>“9. A method for controlling the flow of data in a data transfer path of a computer having a first-in first-out (FIFO) buffer with a plurality of stages positioned between a computer input-output bus and input/output devices, each stage providing storage for both data and a virtual address which are translated to provide a physical address for commands decoupled from application programs originating the commands, comprising the steps of:</p> <p>detecting a value indicating an amount of space available for data in the FIFO buffer,</p> <p>transferring to the FIFO buffer an amount of data up to an amount determine from the value detected, and</p> <p>detecting another value indicating an amount of space available for data in the FIFO buffer before transferring additional data to the FIFO buffer.” Rosenthal ’930 at col. 24, ll. 51–65.</p>
[7k] wherein said first processing element receives a response	Rosenthal ’930 teaches “wherein said first processing element receives a response corresponding to said command from said output queue,” including at least the following exemplary citations.

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corresponding to said command from said output queue.	<p>For example, Rosenthal '930 teaches wherein said first processing element receives a response corresponding to said command from said output queue, by disclosing, as non-limiting examples, receiving a response from the DMA unit. The CPU receives a response from the output queue corresponding to the command. <i>See, e.g.:</i></p> <p>“When the operation involves a device directly associated with the control unit 29 on its device bus 34, the commands after the first commands (creating the new data structure, attaching its new virtual name, providing any necessary device context, and creating the address translation) are sent by hardware directly to that device for execution. If the command requires that data be transferred to or from the application, the input/output device performs the transfer using the DMA unit 35. Upon the return of data in response to a command, the DMA unit 35 of the control unit 29 responds by transferring the data to main memory and notifying the central processing unit in a separate DMA operation of the existence of the data so that no local bus read operation by the central processing unit 21 is necessary to ascertain the result of the operation or to receive the data provided.” Rosenthal '930 at col. 7, ll. 30–45.</p>
8. The system of claim 7, wherein said input queue is a first-in-first-out (FIFO) buffer.	<p>Rosenthal '930 teaches “[t]he system of claim 7, wherein said input queue is a first-in-first-out (FIFO) buffer,” including at least the following exemplary citations.</p> <p><i>See above at row 2.</i></p>
9. The system of claim 7, wherein said system is part of a storage area network (SAN) controller.	
10. The system of claim 7, wherein said system is part of a network attached storage (NAS) controller.	
11. The system of claim 7, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element.	<p>Rosenthal '930 teaches “[t]he system of claim 7, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element,” including at least the following exemplary citations.</p> <p><i>See above at row 5.</i></p>

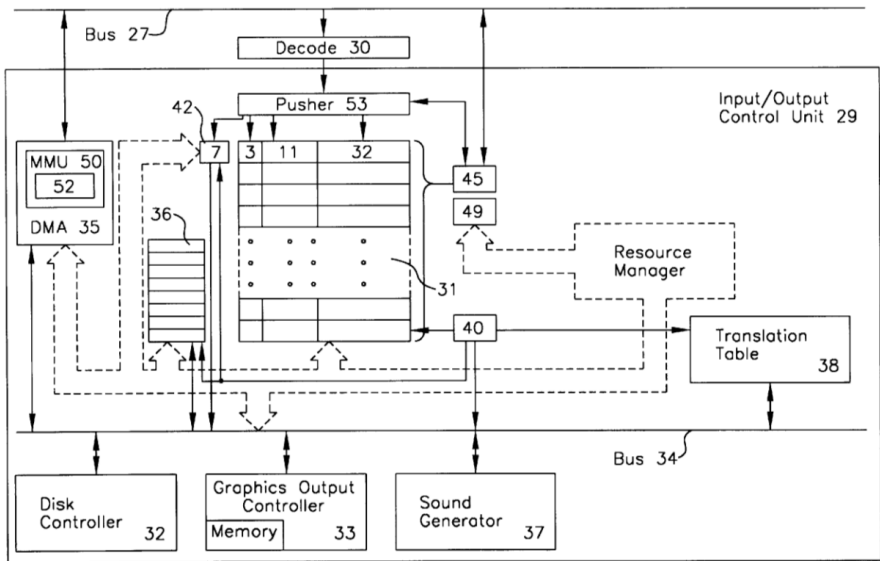
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12. The system of claim 7, wherein at least one third processing element executes said command and notifies said output queue to issue said response.	Rosenthal '930 teaches "[t]he system of claim 7, wherein at least one third processing element executes said command and notifies said output queue to issue said response," including at least the following exemplary citations. <i>See above at row 6.</i>
[13pre] A system for dividing and synchronizing a processing task across a plurality of processing elements comprising:	Rosenthal '930 teaches "[a] system for dividing and synchronizing a processing task across a plurality of processing elements," including at least the following exemplary citations. <i>See above at row [1pre].</i>
[13a] an input queue implemented in hardware;	Rosenthal '930 teaches "an input queue implemented in hardware," including at least the following exemplary citations. <i>See above at row [1a].</i>
[13b] an output queue implemented in hardware;	Rosenthal '930 teaches "an output queue implemented in hardware," including at least the following exemplary citations. <i>See above at row [1b].</i>
[13c] a first processing element having access to said input queue and said output queue;	Rosenthal '930 teaches "a first processing element having access to said input queue and said output queue," including at least the following exemplary citations. <i>See above at row [1c].</i>
[13d] at least one second processing element in communication with said input queue and said output queue;	Rosenthal '930 teaches "at least one second processing element in communication with said input queue and said output queue," including at least the following exemplary citations. For example, Rosenthal '930 teaches at least one second processing element in communication with said input queue and said output queue, by disclosing, as non-limiting examples, an I/O control unit. The I/O control unit, the second processing element is in communication with the input and output queue. <i>See, e.g.:</i>

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	<div><p>Figure 1 Rosenthal '930 at Figure 1.</p></div>

Claim Language	Exemplary Evidence of Anticipation and/or Obviousness
	<div><pre>graph TD; AP[Application Program] --> S[System]; S --> ID1[I/O Driver #1]; ID1 --> IOCU[Input/Output Control Unit 29]; AP --> IOCU; S --> ID2[I/O Driver #2]; ID2 --> RM[Resource Manager]; RM --> IOCU;</pre><p>Figure 2 Rosenthal '930 at Figure 2.</p></div>

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	<div data-bbox="583 259 1459 820"><p>The diagram illustrates a system architecture. At the top, a horizontal line represents Bus 27. Below it, an 'Input/Output Control Unit 29' is shown as a large rectangular block. Inside this unit, at the top, is a 'Decode 30' block connected to Bus 27. Below 'Decode 30' is a 'Pusher 53' block. To the left of 'Pusher 53' is a 'DMA 35' block containing an 'MMU 50' and a sub-block '52'. Below 'DMA 35' is a 'Disk Controller 32'. To the right of 'Pusher 53' is a large grid-like structure labeled '39' with various internal components like '7', '3', '11', '32', and '45'. Below this grid is a 'Graphics Output Controller Memory 33'. To the right of the grid is a 'Resource Manager' block (dashed outline) and a 'Translation Table 38'. Below the 'Resource Manager' is a 'Sound Generator 37'. A horizontal line at the bottom represents Bus 34. Arrows indicate data flow between these components and the buses.</p></div> <p style="text-align: center;">Figure 3</p> <p>Rosenthal '930 at Figure 3.</p>

Claim Language	Exemplary Evidence of Anticipation and/or Obviousness
	 <p>The diagram illustrates a system architecture centered around an Input/Output Control Unit 29. This unit is connected to a Bus 27 at the top and a Bus 34 at the bottom. Within the Input/Output Control Unit 29, several components are shown: a Decode block 30, a Pusher 53, an MMU 50 containing a sub-block 52, a DMA 35, a Resource Manager, and a Translation Table 38. A central processing area 31 contains a grid of blocks labeled 3, 11, 32, 42, 45, 49, and 51. A stack of blocks labeled 36 is also present. External components connected to Bus 34 include a Disk Controller 32, a Graphics Output Controller Memory 33, and a Sound Generator 37. Bidirectional arrows indicate data flow between the control unit and the buses, and between the control unit and its internal components.</p> <p style="text-align: center;">Figure 6</p> <p>Rosenthal '930 at Figure 6.</p>

Claim Language	Exemplary Evidence of Anticipation and/or Obviousness
	<p style="text-align: center;">Figure 7 Rosenthal '930 at Figure 7.</p> <p>“It is another object of the present invention to provide a flow control system for an architecture which utilizes FIFO buffers for buffering write operations.</p> <p>These and other objects of the present invention are realized in a system which uses an arrangement of parallel FIFO buffers in which each FIFO buffer handles data from only one application program at any time. In order to assure that no data written to a FIFO buffer by an application program will overflow the FIFO buffer, each FIFO buffer includes a flow control register which must be read by the central processing unit running the application before writing data to an input/output device. The register stores a value which indicates the amount of space available in the FIFO buffer to which data may be written. Reading this register tells the application program how much data may be written without running the risk of overflowing the data storage area which the input/output device has available. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal '930 at col. 2, ll. 15–33.</p> <p>“The architecture of the system 22 has been designed so that it eliminates almost all read operations of input/output devices by the central processing unit. In order to accomplish this, the input/output control unit 29 includes a first-in first-out (FIFO) unit 31 for storing write operations directed to the input/output control</p>

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	<p>unit. The FIFO unit 31 queues incoming write operations. Unlike FIFO units in prior art systems, it stores both addresses and data. This allows the write operations to the input/output control unit 29 to occur asynchronously so that both the central processing unit 21 and the input/output control unit 29 may be functioning independently of one another and neither need wait for operations of the other.” Rosenthal ’930 at col. 3, l. 66 – col. 4, l. 11.</p> <p>“In one embodiment, the FIFO unit 31 includes a plurality of FIFO buffers 39 (see FIG. 3). When an application program desires to write to an input/output device on the device bus 34, it addresses that device. Decoding circuitry decodes the address by reviewing a number of the highest order bits decoded by the chip sufficient to indicate a unique portion of the input/output address space assigned to an application program and places the command in the appropriate FIFO buffer 39 for that application program. Each FIFO buffer 39 handles commands only from the application program to which the address area has been mapped. An arrangement using a smaller number of FIFO buffers 39 than one buffer for each application program (as few as a single buffer 39) could also be utilized as long as the address of the FIFO buffer is mapped to only one application program at a time.” Rosenthal ’930 at col. 5, ll. 51–66.</p> <p>“The unit 29 receives physical addresses furnished by the memory management unit and virtual names furnished by application programs for operations to be performed which have been sent to the FIFO unit 31 and controls the translation of those virtual names for all input/output devices. The hardware unit 29 includes the device bus 34 to which the individual input/output devices such as a disk controller 32, a graphics output controller 33, and a sound generator 37 are shown joined. The unit 29 also includes a DMA unit 35 which is adapted to transfer data between the individual input/output devices and main memory for use by the central processing unit or other components of the system.” Rosenthal ’930 at col. 5, l. 67 – col. 6, l. 10.</p> <p>“FIG. 3 is a block diagram illustrating details of the input/output control unit 29 including the device bus 34 and the input/output devices arranged on that bus. As described above, the input/output control unit 29 includes a decode unit 30 which receives commands directly from the input/output bus 27 and transfers the commands to a pusher circuit 53 which transfers the command to one of the FIFO buffers 39 of the FIFO unit 31. The FIFO unit 31 stores the data along with the addresses for each of the commands being transferred to all of the input/output devices associated with the input/output control unit 29. The buffers 39 of the FIFO unit replace the individual data registers used by the input/output devices of the prior art. However, in contrast to the registers used by the prior art for communication on the input/output bus 27, the FIFO unit 31 allows a very much larger number of commands to be processed much more rapidly and facilitates the asynchronous operations of the input/output devices and the central processing unit. In one embodiment, the FIFO unit 31</p>

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	<p>includes 128 individual FIFO buffers 39 each of which has thirty-two stages. The use of 128 individual FIFO buffers 39 allows a FIFO buffer to be assigned to each of 128 different application programs which may be running on the central processing unit for the use of that application program alone. The thirty-two stages of each buffer 39 allow any FIFO buffer to hold thirty-two individual serially ordered commands at any time. Although each of the stages of the FIFO unit 31 holds (along with the address bits) the data held by an individual register of a typical prior art input/output device, a particular system has the ability to store commands for over 16 thousand 32 bit registers for each of 128 different application programs which may map different addresses decoded by the input/output control unit 29.” Rosenthal ’930 at col. 8, ll. 21–53.</p> <p>“The use of the flow control register 45 allows an application program presently using the resources of the input/output control unit 29 to proceed without causing the overflow of the FIFO unit 31. Whenever the application has written commands totaling the amount previously read from the register 45, it must read the register again. This is especially useful for application programs which may wish to transfer a series of commands in sequence, possibly using the burst transfer mode of operation provided by many of the modern buses. By ascertaining the space available in the FIFO buffer 39 before transferring a sequence of commands, the application can know that sufficient space will be available for the operation. Provided that no application program ever writes more than the data for which it has permission, no data will be lost.” Rosenthal ’930 at col. 17, ll. 4–18.</p> <p>“Various operating conditions can cause the flow control register 45 associated with a buffer 39 to store different values. If the central processing unit is writing at a rate faster than the input/output device can handle the commands, then a FIFO buffer 39 which is initially empty and provides a maximum free count value when read by the central processing unit will provide a lower free count number after the amount of data first indicated by the free count register has been sent. This will occur because the FIFO buffer 39 will empty more slowly than it is filled. In such a case, the next value read by the application program after sending the amount of data designated by the free count register will be a smaller number. The application program may again send this amount of data and be sure that the FIFO buffer will not overflow. On the other hand, if the central processing unit is writing at a rate slower than the input/output device can handle the commands, then a FIFO buffer which is initially empty and provides a maximum free count value when read by the central processing unit, will provide the same free count number after the amount of data first indicated by the flow control register has been sent. This will occur because the FIFO will empty more rapidly than it is filled and will always be empty when the register 45 is read by the central processing unit.” Rosenthal ’930 at col. 17, ll. 19–42.</p>

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	<p>“Those skilled in the art will recognize that the use of 128 individual FIFO buffers 39 to receive commands written by the central processing unit is very expensive and probably not economically feasible for use with personal computers. In addition, it is expensive of system resources for an operating system to context switch the central processing unit from one application program to another. Thus, the operating system will try to ensure that once an application is given the central processing unit the application will retain control long enough to amortize the cost of the context switch. This means that typically in a one processor system at most one FIFO buffer will be active at a time. In a multi-processor system, typically at most as many FIFO buffers will be active as there are processors.” Rosenthal ’930 at col. 21, ll. 39–52.</p> <p>“One embodiment of the new architecture provides a means for attaining almost the same speed as is possible with 128 FIFO buffers but much more economically. Instead of 128 individual FIFO buffers 39, the described embodiment utilizes a smaller number of FIFO buffers 39 than the number of areas into which the input/output address space may be divided and thus the number of application programs which may be run. Utilizing a smaller number of FIFO buffers causes each FIFO buffer to function as a cache for commands which may be sent by any of the application programs. In the preferred embodiment, one FIFO buffer 39 is used for each processor which may be writing to the input/output control unit 29. For example, if the computer utilizes two processors arranged as symmetrical multi-processors, then two individual FIFO buffers are utilized. If, as is usually the case, only a single central processing unit is used, then a single FIFO buffer 39 may in the limit act as a cache for commands from all application programs which may be running on the central processing unit. Such an arrangement is illustrated in FIG. 6. Of course, in either case more FIFO buffers might be used.” Rosenthal ’930 at col. 21, l. 53 – col. 22, l. 6.</p> <p>“9. A method for controlling the flow of data in a data transfer path of a computer having a first-in first-out (FIFO) buffer with a plurality of stages positioned between a computer input-output bus and input/output devices, each stage providing storage for both data and a virtual address which are translated to provide a physical address for commands decoupled from application programs originating the commands, comprising the steps of:</p> <p>detecting a value indicating an amount of space available for data in the FIFO buffer,</p> <p>transferring to the FIFO buffer an amount of data up to an amount determine from the value detected, and</p> <p>detecting another value indicating an amount of space available for data in the FIFO buffer before transferring additional data to the FIFO buffer.” Rosenthal ’930 at col. 24, ll. 51–65.</p>

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[13e] a reservation register implemented in hardware storing a value indicative of available space in said input queue, said reservation register accessible by both said first processing element and said at least one second processing element;	Rosenthal '930 teaches “a reservation register implemented in hardware storing a value indicative of available space in said input queue, said reservation register accessible by both said first processing element and said at least one second processing element,” including at least the following exemplary citations. <i>See above at row [1e].</i>
[13f] computer storage storing instructions, which when executed by said at least one second processing element:	Rosenthal '930 teaches computer storage storing instructions that are executed by said at least one second processing element including at least the following exemplary citations. <i>See above at row [1f].</i>
[13g] receives a command from said first processing element;	Rosenthal '930 teaches “receives a command from said first processing element,” including at least the following exemplary citations. <i>See above at row [7g].</i>
[13h] accesses said reservation register and reads said stored value;	Rosenthal '930 teaches “accesses said reservation register and reads said stored value,” including at least the following exemplary citations. <i>See above at row [1g].</i>
[13i] determines when said read value indicates available space in said input queue to issue said command;	Rosenthal '930 teaches “determines when said read value indicates available space in said input queue to issue said command,” including at least the following exemplary citations. <i>See above at row [1h].</i>
[13j] issues said command to said input queue on behalf of said first processing element; and	Rosenthal '930 teaches “issues said command to said input queue on behalf of said first processing element,” including at least the following exemplary citations. <i>See above at row [7j].</i>

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<p>[13k] receives a response corresponding to said command from said output queue.</p>	<p>Rosenthal '930 teaches “receives a response corresponding to said command from said output queue,” including at least the following exemplary citations.</p> <p>For example, Rosenthal '930 teaches that the second processing element executes instructions that causes it to receive a response corresponding to said command from said output queue, by disclosing, as non-limiting examples, receiving a response from the DMA unit. The I/O control unit receives a corresponding response from the output queue. <i>See, e.g.:</i></p> <p>“When the operation involves a device directly associated with the control unit 29 on its device bus 34, the commands after the first commands (creating the new data structure, attaching its new virtual name, providing any necessary device context, and creating the address translation) are sent by hardware directly to that device for execution. If the command requires that data be transferred to or from the application, the input/output device performs the transfer using the DMA unit 35. Upon the return of data in response to a command, the DMA unit 35 of the control unit 29 responds by transferring the data to main memory and notifying the central processing unit in a separate DMA operation of the existence of the data so that no local bus read operation by the central processing unit 21 is necessary to ascertain the result of the operation or to receive the data provided.” Rosenthal '930 at col. 7, ll. 30–45.</p>
<p>14. The system of claim 13, wherein said input queue is a first-in-first-out (FIFO) buffer.</p>	<p>Rosenthal '930 teaches “[t]he system of claim 13, wherein said input queue is a first-in-first-out (FIFO) buffer,” including at least the following exemplary citations.</p> <p><i>See</i> above at row 2.</p>
<p>15. The system of claim 13, wherein said system is either part of a storage area network (SAN) controller.</p>	<p>Rosenthal '930 teaches “[t]he system of claim 13, wherein said system is either part of a storage area network (SAN) controller,” including at least the following exemplary citations.</p>
<p>16. The system of claim 13, wherein said system is part of a network attached storage (NAS) controller.</p>	<p>Rosenthal '930 teaches “[t]he system of claim 13, wherein said system is part of a network attached storage (NAS) controller,” including at least the following exemplary citations.</p>

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17. The system of claim 13, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element.	Rosenthal '930 teaches “[t]he system of claim 13, wherein said stored value is decremented by a predefined value prior to returning said stored value to said at least one second processing element,” including at least the following exemplary citations. <i>See above at row 5.</i>
18. The system of claim 13, wherein at least one third processing element executes said command and notifies said output queue to issue said response.	Rosenthal '930 teaches “[t]he system of claim 13, wherein at least one third processing element executes said command and notifies said output queue to issue said response,” including at least the following exemplary citations. <i>See above at row 6.</i>