UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 8,549,339 B2
APPLICATION NO. : 12/713220
DATED : October 1, 2013
INVENTOR(S) : Wolfe et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title Page

In Item (56), under "OTHER PUBLICATIONS", in Column 2, Line 1, delete "al" and insert -- al., --, therefor.

In Item (56), under "OTHER PUBLICATIONS", in Column 2, Line 8, delete "al" and insert -- al., --, therefor.

In Item (56), under "OTHER PUBLICATIONS", in Column 2, Line 11, delete "al" and insert -- al., --, therefor.

In Item (56), under "OTHER PUBLICATIONS", in Column 2, Line 15, delete "Howlett-Packard" and insert -- Hewlett-Packard --, therefor.

In the Specifications

In Column 5, Line 61, delete "and or" and insert -- and/or --, therefor.

In the Claims

In Column 9, Line 7, in Claim 15, delete "for managing" and insert -- to manage --, therefor.

Signed and Sealed this
Sixth Day of May, 2014

Michelle K. Lee

Michelle K. Lee
Deputy Director of the United States Patent and Trademark Office

PTO/SB/44 (09-07)
Approved for use through 08/31/2013. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 8,549,339 B2

APPLICATION NO. : 12/713,220

ISSUE DATE : October 1, 2013

INVENTOR(S) : Wolfe, et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Face Page, in Field (56), under "OTHER PUBLICATIONS", in Column 2, Line 1, delete "al" and insert - - al., - -, therefor.

On the Face Page, in Field (56), under "OTHER PUBLICATIONS", in Column 2, Line 8, delete "al" and insert - - al., - -, therefor.

On the Face Page, in Field (56), under "OTHER PUBLICATIONS", in Column 2, Line 11, delete "al" and insert - - al., - -, therefor.

On the Face Page, in Field (56), under "OTHER PUBLICATIONS", in Column 2, Line 15, delete "Howlett-Packard" and insert - - Hewlett-Packard - -, therefor.

In Column 5, Line 61, delete "and or" and insert - - and/or - -, therefor.

In Column 9, Line 7, in Claim 15, delete "for managing" and insert - - to manage - -, therefor.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Maschoff Brennan
1389 Center Drive, Suite 300
Park City, Utah 84098, United States

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

PATENT NO.: 8,549,339

USPTO CONFIRMATION CODE: 4243

APPLICATION NO.: 12/713,220

FILED: February 26, 2010

EXAMINER: Dennis M. Butler

GROUP ART UNIT: 2115

FOR: PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR

37 CFR 1.322 & 37 CFR 1.323 REQUEST FOR CERTIFICATE OF CORRECTION FOR USPTO AND/OR APPLICANT MISTAKE

Commissioner for Patents
Office of Patent Publication
ATTN: Certificate of Correction Branch
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

A certificate of correction under 35 USC 254 is respectfully requested in the above-identified patent.

It is believed that all errors identified herein were the fault of both the applicant and USPTO and, accordingly, please charge **$100.00** to the credit card utilized for this certificate of correction filing. In the event that a further fee is required, please charge the amount to the same credit card.

The exact locations where the errors appear in the patent and patent application are as follows:

On the Face Page, in Field (56), under "OTHER PUBLICATIONS", in Column 2, Line 1, delete "al" and insert - - al., - -, therefor.
(LIST OF REFERENCES CITED BY APPLICANT AND CONSIDERED BY EXAMINER DATED JUNE 11, 2013, SHEET 2 (PAGE 28 OF FW), UNDER "NON-PATENT LITERATURE DOCUMENTS", ENTRY 1, LINE 1)

On the Face Page, in Field (56), under "OTHER PUBLICATIONS", in Column 2, Line 8, delete "al" and insert - - al., - -, therefor.
(LIST OF REFERENCES CITED BY APPLICANT AND CONSIDERED BY EXAMINER DATED JUNE 11, 2013, SHEET 2 (PAGE 28 OF FW), UNDER "NON-PATENT LITERATURE DOCUMENTS", ENTRY 3, LINE 1)

On the Face Page, in Field (56), under "OTHER PUBLICATIONS", in Column 2, Line 11, delete "al" and insert - - al., - -, therefor.
(LIST OF REFERENCES CITED BY APPLICANT AND CONSIDERED BY EXAMINER DATED JUNE 11, 2013, SHEET 2 (PAGE 28 OF FW), UNDER "NON-PATENT LITERATURE DOCUMENTS", ENTRY 4, LINE 1)

On the Face Page, in Field (56), under "OTHER PUBLICATIONS", in Column 2, Line 15, delete "Howlett-Packard" and insert - - Hewlett-Packard - -, therefor.
(LIST OF REFERENCES CITED BY APPLICANT AND CONSIDERED BY EXAMINER DATED JUNE 11, 2013, SHEET 2 (PAGE 28 OF FW), UNDER "NON-PATENT LITERATURE DOCUMENTS", ENTRY 5, LINE 1)

In Column 5, Line 61, delete "and or" and insert - - and/or - -, therefor.
(ORIGINALLY FILED SPECIFICATION DATED FEBRUARY 26, 2010, PAGE 10, LINE 1)

In Column 9, Line 7, in Claim 15, delete "for managing" and insert - - to manage - -, therefor.
(AMENDMENTS TO THE CLAIMS DATED AUGUST 13, 2013, PAGE 5, CLAIM 15, LINE 1)

The requested corrections are attached on Form PTO/SB/44.

Dated this 4th day of February, 2014.

Respectfully Submitted,

/R. Burns Israelsen/ Reg. # 42,685
R. BURNS ISRAELSEN
Acting in Representative Capacity
(37 CFR 1.34)
Registration No. 42,685
Telephone No. (435) 252-1360

Electronic Patent Application Fee Transmittal

Application Number:	12713220
Filing Date:	26-Feb-2010
Title of Invention:	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR
First Named Inventor/Applicant Name:	Andrew WOLFE
Filer:	Robert Burns Israelsen/Jeffrey Woodward
Attorney Docket Number:	121-0019-US-REG

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Certificate of Correction	1811	1	100	100
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**100**

Electronic Acknowledgement Receipt

EFS ID:	18105822
Application Number:	12713220
International Application Number:	
Confirmation Number:	4243
Title of Invention:	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR
First Named Inventor/Applicant Name:	Andrew WOLFE
Customer Number:	83446
Filer:	Robert Burns Israelsen/Jeffrey Woodward
Filer Authorized By:	Robert Burns Israelsen
Attorney Docket Number:	121-0019-US-REG
Receipt Date:	04-FEB-2014
Filing Date:	26-FEB-2010
Time Stamp:	12:13:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$100
RAM confirmation Number	10430
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if app.)

1	Request for Certificate of Correction	US-600189-01-US-REG_2014-02-04_CoC.pdf	254990 7662d7a73eede60445db0a52e137d1ffa756e38c	no	2
Warnings:					
Information:					
2	Request for Certificate of Correction	US-600189-01-US-REG_2014-02-04_Request_Letter.pdf	148834 be2caebb879383568a9cbb5ba48658dae831c199	no	3
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30063 11b8d44894d6b36a1e285b47417970a6a87c2a71	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	433887	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/713,220	10/01/2013	8549339	121-0019-US-REG	4243

83446 7590 09/11/2013
REN-SHENG INTERNATIONAL IP MANAGEMENT LTD.
GENE I. SU
7F, NO. 57, SEC. 2, DUN HUA S. ROAD
TAIPEI, 106
TAIWAN

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 524 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Andrew WOLFE, Los Gatos, CA;
Marc Elliot LEVITT, San Jose, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/713,220	02/26/2010	Andrew WOLFE	121-0019-US-REG	4243

83446 7590 09/05/2013
REN-SHENG INTERNATIONAL IP MANAGEMENT LTD.
GENE I. SU
7F, NO. 57, SEC. 2, DUN HUA S. ROAD
TAIPEI, 106
TAIWAN

EXAMINER
BUTLER, DENNIS

ART UNIT	PAPER NUMBER
2115	

NOTIFICATION DATE	DELIVERY MODE
09/05/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

gsu@suipconsulting.com
filing@suipconsulting.com
gene.i.su@gmail.com

Response to Rule 312 Communication	Application No.	Applicant(s)
	12/713,220	WOLFE ET AL.
	Examiner	**Art Unit**
	DENNIS M. BUTLER	2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ The amendment filed on *13 August 2013* under 37 CFR 1.312 has been considered, and has been:

a) ☐ entered.

b) ☒ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☒ entered in part. See explanation below.

The amendments to claims 2,3,16,18,19 and 20 have been entered because they are directed to matters of form not affecting the scope of the invention. The amendment to claim 15 has not been entered because it would add indefinite language into the method claim and there is no reason why it is necessary to add the indefinite language.

/DENNIS M BUTLER/
Primary Examiner, Art Unit 2115

ENTER IN PART: /D.B./

/D.B./ 08/26/2013

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Andrew WOLFE	§	
	§	Group Art Unit: 2115
Serial No.: 12/713,220	§	
Confirmation No.: 4243	§	Examiner: BUTLER, DENNIS
Filed: February 26, 2010	§	
For: PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR	§	

MAIL STOP ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

AMENDMENT AFTER ALLOWANCE UNDER 37 C.F.R. §1.312 AND ISSUE FEE TRANSMITTAL

The Examiner is thanked for issuing the Notice of Allowance and Fee Due mailed on June 11, 2013. Please enter the following amendment prior to issuing the present application as a patent under 37 C.F.R. §1.312.

Enclosed herewith please also find Issue Fee Transmittal Form PTOL-85(B).

The Issue Fee and the Publication Fee are being paid by credit card via EFS-Web.

It is respectfully noted that there may be additional reasons for allowance that have not been specifically cited, and which may apply to various of the allowed claims, in addition to or instead of the Examiner's Reasons for Allowance. It is respectfully suggested that notwithstanding the Examiner's Reasons for Allowance, each of the allowed claims is believed to be patentable in its own right and/or at least for other reasons raised during the prosecution and/or explained in the specification of this application.

To the extent that any statements regarding patentability of any claims allowed by the Examiner made in any document filed in this application are inconsistent with or not included in the Examiner's Reasons for Allowance, they are incorporated by reference herein.

Although it is believed that no additional fees are due in connection with this submission, the Commissioner is hereby authorized to charge Counsel's Deposit Account No. 50-4588/121-0019-US-REG for any fees required to make this submission timely and acceptable to the Office.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

83446 7590 06/11/2013
REN-SHENG INTERNATIONAL IP MANAGEMENT LTD.
GENE I. SU
7F, NO. 57, SEC. 2, DUN HUA S. ROAD
TAIPEI, 106
TAIWAN

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/713,220	02/26/2010	Andrew WOLFE	121-0019-US-REG	4243

TITLE OF INVENTION: PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	09/11/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
BUTLER, DENNIS	2115	713-322000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 REN-SHENG INTERNATIONAL
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: EMPIRE TECHNOLOGY DEVELOPMENT LLC

(B) RESIDENCE: (CITY and STATE OR COUNTRY): WILMINGTON, DELAWARE

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☒ Payment by credit card. ~~Form PTO-2038 is attached.~~
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29	NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
❑ Applicant asserting small entity status. See 37 CFR 1.27	NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
❑ Applicant changing to regular undiscounted fee status.	NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Gene Su/ Date August 13, 2013

Typed or printed name Gene Su Registration No. 45,140

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal

Application Number:	12713220
Filing Date:	26-Feb-2010
Title of Invention:	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR
First Named Inventor/Applicant Name:	Andrew WOLFE
Filer:	Gene I. Su
Attorney Docket Number:	121-0019-US-REG

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	1780	1780
Publ. Fee- Early, Voluntary, or Normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**2080**

Electronic Acknowledgement Receipt

EFS ID:	16570306
Application Number:	12713220
International Application Number:	
Confirmation Number:	4243
Title of Invention:	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR
First Named Inventor/Applicant Name:	Andrew WOLFE
Customer Number:	83446
Filer:	Gene I. Su
Filer Authorized By:	
Attorney Docket Number:	121-0019-US-REG
Receipt Date:	13-AUG-2013
Filing Date:	26-FEB-2010
Time Stamp:	03:24:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$2080
RAM confirmation Number	8367
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Amendment after Notice of Allowance (Rule 312)	121-0019-US-REG_312-Amendment_General-Transmittal.pdf	58853 7476264bf8baab0992ba2ab3d9692754717d5875	no	8
Warnings:					
Information:					
2	Issue Fee Payment (PTO-85B)	121-0019-US-REG_PTOL85.pdf	102098 73cdce04e986c3e884cfaed3aff2aca3feb50c04	no	2
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	31854 bac163000e3cedd4d1e40822d220cf2876d21e7b	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	192805		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Andrew WOLFE	§	
	§	Group Art Unit: 2115
Serial No.: 12/713,220	§	
Confirmation No.: 4243	§	Examiner: BUTLER, DENNIS
Filed: February 26, 2010	§	
For: PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR	§	

MAIL STOP ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

AMENDMENT AFTER ALLOWANCE UNDER 37 C.F.R. §1.312 AND ISSUE FEE TRANSMITTAL

The Examiner is thanked for issuing the Notice of Allowance and Fee Due mailed on June 11, 2013. Please enter the following amendment prior to issuing the present application as a patent under 37 C.F.R. §1.312.

Enclosed herewith please also find Issue Fee Transmittal Form PTOL-85(B).

The Issue Fee and the Publication Fee are being paid by credit card via EFS-Web.

It is respectfully noted that there may be additional reasons for allowance that have not been specifically cited, and which may apply to various of the allowed claims, in addition to or instead of the Examiner's Reasons for Allowance. It is respectfully suggested that notwithstanding the Examiner's Reasons for Allowance, each of the allowed claims is believed to be patentable in its own right and/or at least for other reasons raised during the prosecution and/or explained in the specification of this application.

To the extent that any statements regarding patentability of any claims allowed by the Examiner made in any document filed in this application are inconsistent with or not included in the Examiner's Reasons for Allowance, they are incorporated by reference herein.

Although it is believed that no additional fees are due in connection with this submission, the Commissioner is hereby authorized to charge Counsel's Deposit Account No. 50-4588/121-0019-US-REG for any fees required to make this submission timely and acceptable to the Office.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

IN THE CLAIMS:

The listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Previously Presented) A multi-core processor, comprising:

a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input;

a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and

an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.

2. (Currently Amended) The multi-core processor of claim 1, wherein the interface block further ~~comprising~~comprises a first level shifter that is referenced to the second supply voltage and adapted to translate first logic levels associated with the first set of processor cores to second logic levels associated with the second set of processor cores for a first signal traveling from the first set of processor cores to the second set of processor cores.

3. (Currently Amended) The multi-core processor of claim 1, wherein the interface block further ~~comprising~~comprises a second level shifter that is referenced to the first supply voltage and adapted to translate second logic levels associated with the second set of processor cores to first logic levels associated with the first set of processor cores for a second signal traveling from the second set of processor cores to the first set of processor cores.

4. (Original) The multi-core processor of claim 1, wherein the interface block further comprises a synchronizer configured to synchronize the first clock signal and the second clock

signal for communication between one or more processor cores of the first set of processor cores and one or more processor cores of the second set of processor cores.

5. (Original) The multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a periphery of the multi-core processor.

6. (Original) The multi-core processor of claim 1, wherein the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located in a second region of the multi-core processor.

7. (Original) The multi-core processor of claim 6, wherein the first region and the second region are overlapping regions of the multi-core processor.

8. (Original) The multi-core processor of claim 6, wherein the first region and the second region are non-overlapping regions of the multi-core processor.

9. (Original) The multi-core processor of claim 6, wherein the first region corresponds to a first row of the multi-core processor, and wherein the second region corresponds to a second row of the multi-core processor.

10. (Previously Presented) The multi-core processor of claim 1, wherein the interface block is configured to idle communications between the first set of processor cores and the second set of processor cores when one or more of the first output clock signal and/or the second output clock signal is determined to have changed.

11. (Previously Presented) The multi-core processor of claim 10, wherein the interface block is configured to resume communication between the first set of processor cores and the second set of processor cores after one or more of the first output clock signal and/or the second output clock signal is determined to have stabilized.

12. (Original) The multi-core processor of claim 5, wherein the first set of processor cores is adjacent to the second set of processor cores, and the one or more control blocks are

configured to select the first supply voltage and the second supply voltage to maintain a differential relationship between the first supply voltage and the second supply voltage.

13. (Original) The multi-core processor of claim 12, wherein the differential relationship is based on having an output voltage level associated with the first set of processor cores to be within an acceptable input voltage level associated with the second set of processor cores.

14. (Original) The multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a common region that is substantially central to the first set of processor cores and the second set of processor cores.

15. (Currently Amended) A method ~~for managing~~to manage communications in a multi-core processor that includes a plurality of processor cores having a first set of processor cores and a second set of processor cores, the method comprising:

idling communications between the first set of processor cores and the second set of processor cores in response to a clock frequency change request for the first set of processor cores; and

resuming communications between the first set of processor cores and the second set of processor cores after having determined that a first phase lock loop operation associated with a first clock signal for the first set of processor cores has acquired a first lock signal and a second phase lock loop operation associated with a second clock signal for the second set of processor cores has also acquired a second lock signal, wherein the first clock signal is independent from the second clock signal.

16. (Currently Amended) The method of claim 15, wherein resuming communications further ~~comprising~~comprises having determined that a third phase lock loop operation associated with a third set of processor cores in the multi-core processor has acquired a third lock signal, wherein the third set of processor cores is adjacent to the first set of processor cores.

17. (Original) The method of claim 16, wherein the second set of processor cores is adjacent to the first set of processor cores.

18. (Currently Amended) A ~~non-transistory~~non-transitory computer-readable medium containing a sequence of instructions ~~for managing~~to manage communications in a multi-core processor that includes a plurality of processor cores having a first set of processor cores and a second set of processor cores, which when executed by a computing device, causes the computing device to:

issue a first command to idle communications between the first set of processor cores and the second set of processor cores in response to a clock frequency change request for the first set of processor cores;

issue a second command to resume communications between the first set of processor cores and the second set of processor cores after having determined that a first phase lock loop operation associated with a first clock signal for the first set of processor cores has acquired a first lock signal and a second phase lock loop operation associated with a second clock signal for the second set of processor cores has also acquired a second lock signal, wherein the first clock signal is independent from the second clock signal.

19. (Currently Amended) The ~~non-transistory~~non-transitory computer-readable medium of claim 18, further including a sequence of instructions, which when executed by the computing device, causes the computing device to determine whether a third phase lock loop operation associated with a third set of processor cores in the multi-core processor has acquired a third lock signal before issuing the second command, wherein the third set of processor cores is adjacent to the first set of processor cores.

20. (Currently Amended) The ~~non-transistory~~non-transitory computer-readable medium of claim 19, wherein the second set of processor cores is adjacent to the first set of processor cores.

21. (Previously Presented) A multi-core processor, comprising:

a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage from a power control block and a first output clock signal from a first phase lock loop (PLL) having a first clock signal as input in a clock control block;

a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage from the power control block and a second output clock signal from a second PLL having a second clock signal as input in the clock control block, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and

an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.

22. (Previously Presented) The multi-core processor of claim 21, wherein the interface block is configured to idle communications between the first set of processor cores and the second set of processor cores when one or more of the first output clock signal and/or the second output clock signal is determined to have changed.

23. (Previously Presented) The multi-core processor of claim 22, wherein the interface block is configured to resume communication between the first set of processor cores and the second set of processor cores after one or more of the first output clock signal and/or the second output clock signal is determined to have stabilized.

REMARKS

Please enter the above amendment prior to issuing the present application as a patent. Specifically, claims 2 – 3, 15 – 16, and 18 – 20 have been amended to merely address formal matters in the claims without changing the scope thereof.

The amendments do not introduce any new matter or raise any new issues. If there are any questions about any of the foregoing, please contact the undersigned representative.

Respectfully submitted,

/Gene Su/
Gene Su
Registration No. 45,140

Telephone: (886) 2.2700.7882
Facsimile 1: (886) 2.2700.7856
Facsimile 2: (650) 644.3217
Email: filing@suipconsulting.com

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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NOTICE OF ALLOWANCE AND FEE(S) DUE

83446 7590 06/11/2013
REN-SHENG INTERNATIONAL IP MANAGEMENT LTD.
GENE I. SU
7F, NO. 57, SEC. 2, DUN HUA S. ROAD
TAIPEI, 106
TAIWAN

EXAMINER
BUTLER, DENNIS

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 06/11/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/713,220	02/26/2010	Andrew WOLFE	121-0019-US-REG	4243

TITLE OF INVENTION: PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	09/11/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

83446 7590 06/11/2013
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7F, NO. 57, SEC. 2, DUN HUA S. ROAD
TAIPEI, 106
TAIWAN

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/713,220	02/26/2010	Andrew WOLFE	121-0019-US-REG	4243

TITLE OF INVENTION: PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	09/11/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
BUTLER, DENNIS	2115	713-322000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee
❑ Publication Fee (No small entity discount permitted)
❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.
❑ Payment by credit card. Form PTO-2038 is attached.
❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29	NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
❑ Applicant asserting small entity status. See 37 CFR 1.27	NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
❑ Applicant changing to regular undiscounted fee status.	NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/713,220	02/26/2010	Andrew WOLFE	121-0019-US-REG	4243

83446 7590 06/11/2013
REN-SHENG INTERNATIONAL IP MANAGEMENT LTD.
GENE I. SU
7F, NO. 57, SEC. 2, DUN HUA S. ROAD
TAIPEI, 106
TAIWAN

EXAMINER
BUTLER, DENNIS

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 06/11/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 491 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 491 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 12/713,220	Applicant(s) WOLFE ET AL.	
	Examiner DENNIS M. BUTLER	Art Unit 2115	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the IDS filed on April 25, 2013*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-23*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

   Interim copies:

   a) ☐ All b) ☐ Some c) ☐ None of the: Interim copies of the priority documents have been received.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 4/25/2013
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/DENNIS M BUTLER/
Primary Examiner, Art Unit 2115

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12713220	WOLFE ET AL.
	Examiner	**Art Unit**
	DENNIS M BUTLER	2115

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/23/2012	02/06/2013	06/01/2013						
	1	✓	=	=						
	2	✓	=	=						
	3	✓	=	=						
	4	✓	=	=						
	5	✓	=	=						
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	20	✓	=	=						
	21	✓	=	=						
	22	✓	=	=						
	23	✓	=	=						

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	12713220
Filing Date	2010-02-26
First Named Inventor	Andrew WOLFE
Art Unit	2115
Examiner Name	Dennis BUTLER
Attorney Docket Number	121-0019-US-REG

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/D.B./	1	7219245	B1	2007-05-15	Raghuvanshi	
/D.B./	2	6711447	B1	2004-03-23	Saeed	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	12713220
	Filing Date	2010-02-26
	First Named Inventor	Andrew WOLFE
	Art Unit	2115
	Examiner Name	Dennis BUTLER
	Attorney Docket Number	121-0019-US-REG

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
/D.B./	1	JOONHO KONG et al., "Low-Cost Application-Aware DVFS for Multi-Core Architecture", Third 2008 International Conference on Convergence and Hybrid Information Technology, IEEE Computer Society, 2008, pages 106-111	☐
/D.B./	2	REINALDO BERGAMASCHI et al., "Exploring Power Management in Multi-Core Systems", IEEE, 2008, pages 708-713 (Downloaded on July 13, 2009 from IEEE Xplore)	☐
/D.B./	3	WAYNE H. CHENG et al., "Dynamic Voltage and Frequency Scaling Circuits with Two Supply Voltages", IEEE, 2008, pages 1236-1239 (Downloaded on July 14, 2009 from IEEE Xplore)	☐
/D.B./	4	WONYOUNG KIM et al., "System Level Analysis of Fast, Per-Core DVFS using On-Chip Switching Regulators", High Performance Computer Architecture, IEEE 14th International Symposium, Feb. 16-20, 2008, pages 123-134	☐
/D.B./	5	HOWLETT-PACKARD CORPORATION et al., "Advanced Configuration and Power Interface Specification", October 10, 2006, Pages 1-631 (represented by 4 different files), Revision 3.0b	☐
/D.B./	6	MICAH SCHMIDT, "Nehalem: Xeon Gets Core i7 Upgrade", 2CPU.com, Mar 29, 2009 <http://www.2cpu.com/review.php?id=117>	☐
/D.B./	7	"Third-Generation AMD Opteron Processor Key Architectural Features", WAYBACKMACHINE, October 20, 2007 <http://www.amd.com/us-en/Processors/ProductInformation/0,,30_118_8796_15224,00.html>	☐

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EXAMINER SIGNATURE

Examiner Signature	/Dennis Butler/	Date Considered	06/01/2013

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	12713220
	Filing Date	2010-02-26
	First Named Inventor	Andrew WOLFE
	Art Unit	2115
	Examiner Name	Dennis BUTLER
	Attorney Docket Number	121-0019-US-REG

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Gene Su/	Date (YYYY-MM-DD)	2013-04-25
Name/Print	Gene Su	Registration Number	45140

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12713220	WOLFE ET AL.
	Examiner	**Art Unit**
	DENNIS M BUTLER	2115

CPC- SEARCHED

Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED

Symbol	Date	Examiner

US CLASSIFICATION SEARCHED

Class	Subclass	Date	Examiner

SEARCH NOTES

Search Notes	Date	Examiner
EAST search attached.	8/22/2012	DB
EAST search attached.	2/6/2013	DB
EAST search attached.	6/1/2013	DB

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
713	320, 322, 501	2/6/2013	DB
713	320, 322, 501	6/1/2013	DB

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	("6711447" | "7219245").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/06/01 22:07
L2	59622	(plurality multi multiple) adj2 core	US-PGPUB; USPAT; USOCR	OR	ON	2013/06/01 22:14
L3	25595	2 near5 (processor microprocessor cpu mpu)	US-PGPUB; USPAT; USOCR	OR	ON	2013/06/01 22:15
L4	3546	2 near5 (set group$3)	US-PGPUB; USPAT; USOCR	OR	ON	2013/06/01 22:17
L5	2363	3 and 4	US-PGPUB; USPAT; USOCR	OR	ON	2013/06/01 22:17
L6	323	5 and voltage and (clock frequency)	US-PGPUB; USPAT; USOCR	OR	ON	2013/06/01 22:18
L7	1	1 and 6	US-PGPUB; USPAT; USOCR	OR	ON	2013/06/01 22:18
L8	2615	first adj2 pll	US-PGPUB; USPAT; USOCR	OR	ON	2013/06/01 22:26
L9	2784	second adj2 pll	US-PGPUB; USPAT; USOCR	OR	ON	2013/06/01 22:26
L10	2409	second adj2 (phase adj lock$2 adj loop)	US-PGPUB; USPAT; USOCR	OR	ON	2013/06/01 22:28
L11	2190	first adj2 (phase adj lock$2 adj loop)	US-PGPUB; USPAT; USOCR	OR	ON	2013/06/01 22:28
L12	4752	9 or 10	US-PGPUB; USPAT; USOCR	OR	ON	2013/06/01 22:28
L13	4228	8 or 11	US-PGPUB; USPAT; USOCR	OR	ON	2013/06/01 22:28
L14	2942	12 and 13	US-PGPUB; USPAT; USOCR	OR	ON	2013/06/01 22:29
L15	1	6 and 14	US-PGPUB; USPAT; USOCR	OR	ON	2013/06/01 22:29

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L16	56394	(plurality multi multiple) adj2 core	US-PGPUB; USPAT; UPAD	OR	ON	2013/06/01 22:33
L17	25976	16 near5 (processor microprocessor cpu mpu)	US-PGPUB; USPAT; UPAD	OR	ON	2013/06/01 22:33
L18	3394	16 near5 (set group$3)	US-PGPUB; USPAT; UPAD	OR	ON	2013/06/01 22:34
L19	2401	17 and 18	US-PGPUB; USPAT; UPAD	OR	ON	2013/06/01 22:34
L20	328	19 and voltage and (clock frequency)	US-PGPUB; USPAT; UPAD	OR	ON	2013/06/01 22:35

L21	2598	first adj2 pll	US-PGPUB; USPAT; UPAD	OR	ON	2013/06/01 22:35
L22	2163	first adj2 (phase adj lock$2 adj loop)	US-PGPUB; USPAT; UPAD	OR	ON	2013/06/01 22:35
L23	2777	second adj2 pll	US-PGPUB; USPAT; UPAD	OR	ON	2013/06/01 22:35
L24	2380	second adj2 (phase adj lock$2 adj loop)	US-PGPUB; USPAT; UPAD	OR	ON	2013/06/01 22:36
L25	4183	21 or 22	US-PGPUB; USPAT; UPAD	OR	ON	2013/06/01 22:36
L26	4715	23 or 24	US-PGPUB; USPAT; UPAD	OR	ON	2013/06/01 22:36
L27	2922	25 and 26	US-PGPUB; USPAT; UPAD	OR	ON	2013/06/01 22:37
L28	1	20 and 27	US-PGPUB; USPAT; UPAD	OR	ON	2013/06/01 22:37

6/1/2013 10:40:44 PM
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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12713220	WOLFE ET AL.
	Examiner	**Art Unit**
	DENNIS M BUTLER	2115

CPC

Symbol	Type	Version

CPC Combination Sets

Symbol	Type	Set	Ranking	Version

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
713	322	G	0	6	F	1 / 08 (2006.01.01)					
CROSS REFERENCE(S)		G	0	6	F	1 / 32 (2006.01.01)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)										
713	320 501										

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 23	
/DENNIS M BUTLER/ Primary Examiner.Art Unit 2115 (Primary Examiner)	6/1/2013 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
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/DENNIS M BUTLER/ Primary Examiner.Art Unit 2115 (Primary Examiner)	6/1/2013 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3

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☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17												
2	2	18	18												
3	3	19	19												
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15	15														
16	16														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 23	
/DENNIS M BUTLER/ Primary Examiner.Art Unit 2115 (Primary Examiner)	6/1/2013 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3

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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	12/713,220	Filing Date	2010-02-26	Docket Number (if applicable)	121-0019-US-REG	Art Unit	2115
First Named Inventor	Andrew WOLFE			Examiner Name	BUTLER, DENNIS		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☐ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☐ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No _____

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

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Signature of Registered U.S. Patent Practitioner			
Signature	/Gene Su/	Date (YYYY-MM-DD)	2013-04-25
Name	Gene Su	Registration Number	45140

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

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Filing Date	2010-02-26
First Named Inventor	Andrew WOLFE
Art Unit	2115
Examiner Name	Dennis BUTLER
Attorney Docket Number	121-0019-US-REG

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7219245	B1	2007-05-15	Raghuvanshi	
	2	6711447	B1	2004-03-23	Saeed	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

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NON-PATENT LITERATURE DOCUMENTS Remove

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	12713220
	Filing Date	2010-02-26
	First Named Inventor	Andrew WOLFE
	Art Unit	2115
	Examiner Name	Dennis BUTLER
	Attorney Docket Number	121-0019-US-REG

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	JOONHO KONG et al., "Low-Cost Application-Aware DVFS for Multi-Core Architecture", Third 2008 International Conference on Convergence and Hybrid Information Technology, IEEE Computer Society, 2008, pages 106-111	☐
	2	REINALDO BERGAMASCHI et al., "Exploring Power Management in Multi-Core Systems", IEEE, 2008, pages 708-713 (Downloaded on July 13, 2009 from IEEE Xplore)	☐
	3	WAYNE H. CHENG et al., "Dynamic Voltage and Frequency Scaling Circuits with Two Supply Voltages", IEEE, 2008, pages 1236-1239 (Downloaded on July 14, 2009 from IEEE Xplore)	☐
	4	WONYOUNG KIM et al., "System Level Analysis of Fast, Per-Core DVFS using On-Chip Switching Regulators", High Performance Computer Architecture, IEEE 14th International Symposium, Feb. 16-20, 2008, pages 123-134	☐
	5	HOWLETT-PACKARD CORPORATION et al., "Advanced Configuration and Power Interface Specification", October 10, 2006, Pages 1-631 (represented by 4 different files), Revision 3.0b	☐
	6	MICAH SCHMIDT, "Nehalem: Xeon Gets Core i7 Upgrade", 2CPU.com, Mar 29, 2009 <http://www.2cpu.com/review.php?id=117>	☐
	7	"Third-Generation AMD Opteron Processor Key Architectural Features", WAYBACKMACHINE, October 20, 2007 <http://www.amd.com/us-en/Processors/ProductInformation/0,,30_118_8796_15224,00.html>	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	12713220
	Filing Date	2010-02-26
	First Named Inventor	Andrew WOLFE
	Art Unit	2115
	Examiner Name	Dennis BUTLER
	Attorney Docket Number	121-0019-US-REG

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Gene Su/	Date (YYYY-MM-DD)	2013-04-25
Name/Print	Gene Su	Registration Number	45140

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	12713220
Filing Date:	26-Feb-2010
Title of Invention:	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR
First Named Inventor/Applicant Name:	Andrew WOLFE
Filer:	Gene I. Su
Attorney Docket Number:	121-0019-US-REG

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for Continued Examination	1801	1	1200	1200
		Total in USD ($)		**1200**

Electronic Acknowledgement Receipt

EFS ID:	15607313
Application Number:	12713220
International Application Number:	
Confirmation Number:	4243
Title of Invention:	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR
First Named Inventor/Applicant Name:	Andrew WOLFE
Customer Number:	83446
Filer:	Gene I. Su
Filer Authorized By:	
Attorney Docket Number:	121-0019-US-REG
Receipt Date:	25-APR-2013
Filing Date:	26-FEB-2010
Time Stamp:	05:45:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1200
RAM confirmation Number	7527
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if app.)

1	Request for Continued Examination (RCE)	121-0019-US-REG_RCE_2013-02-14.pdf	697381 5845421c7cc672bd45bd42fc06177c4023092c79	no	3
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	121-0019-US-REG_IDS.pdf	612976 14eb9979d7b8ce9933eeca3d4d5b9475991e18a8	no	4
Warnings:					
Information:					
3	Non Patent Literature	121-0019-US-REG_NPL1-Low-Cost.pdf	180854 e3d2d6b3b8c2323f1a4e45059af592134f5eb7eb	no	6
Warnings:					
Information:					
4	Non Patent Literature	121-0019-US-REG_NPL2-Exploring.pdf	669151 201e4bc86bc06d9a93e0f76f633523386c99a72a	no	6
Warnings:					
Information:					
5	Non Patent Literature	121-0019-US-REG_NPL3-Dynamic.pdf	219137 0db71b386319820b59a4b041f932fc262ef9ea40	no	4
Warnings:					
Information:					
6	Non Patent Literature	121-0019-US-REG_NPL4-System.pdf	1860305 da67e23313a6e862eeb07576f4ee6e2fad49ee63	no	14
Warnings:					
Information:					
7	Non Patent Literature	121-0019-US-REG_NPL5-Advanced_P1-157.pdf	1864456 859952ea29a1e8bec1a566193787c41af8217dc8	no	157
Warnings:					
Information:					
8	Non Patent Literature	121-0019-US-REG_NPL5-Advanced_P158-315.pdf	1734030 295dc4cc97d332cd1a3bd2fafca91bcfe25b57d6	no	158
Warnings:					
Information:					
9	Non Patent Literature	121-0019-US-REG_NPL5-Advanced_P316-515.pdf	1895228 7e419535a8fe72af4af827c5a48aa490976019c3	no	200
Warnings:					
Information:					

10	Non Patent Literature	121-0019-US-REG_NPL5-Advanced_P516-631.pdf	1275324 59787ff3000661c85261b2c2ed2d60c2f5aefd68	no	116
Warnings:					
Information:					
11	Non Patent Literature	121-0019-US-REG_NPL6-Nehalem.pdf	110376 69ddd5be04f3f45a44a83839fdb5a2959b288e44	no	2
Warnings:					
Information:					
12	Non Patent Literature	121-0019-US-REG_NPL7-Third-Generation-AMD.pdf	92566 f266135c326e6e8a9774cf66853fa9c23443fc3b	no	2
Warnings:					
Information:					
13	Fee Worksheet (SB06)	fee-info.pdf	30163 31ce48b5e602fb9a0d49d2c2957574e805b58299	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	11241947	

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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United States Patent and Trademark Office
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NOTICE OF ALLOWANCE AND FEE(S) DUE

83446 7590 02/14/2013
REN-SHENG INTERNATIONAL IP MANAGEMENT LTD.
GENE I. SU
7F, NO. 57, SEC. 2, DUN HUA S. ROAD
TAIPEI, 106
TAIWAN

EXAMINER
BUTLER, DENNIS

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 02/14/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/713,220	02/26/2010	Andrew WOLFE	121-0019-US-REG	4243

TITLE OF INVENTION: PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1770	$300	$0	$2070	05/14/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

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III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

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Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

83446 7590 02/14/2013
REN-SHENG INTERNATIONAL IP MANAGEMENT LTD.
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TAIPEI, 106
TAIWAN

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/713,220	02/26/2010	Andrew WOLFE	121-0019-US-REG	4243

TITLE OF INVENTION: PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1770	$300	$0	$2070	05/14/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
BUTLER, DENNIS	2115	713-322000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

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- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/713,220	02/26/2010	Andrew WOLFE	121-0019-US-REG	4243

83446 7590 02/14/2013
REN-SHENG INTERNATIONAL IP MANAGEMENT LTD.
GENE I. SU
7F, NO. 57, SEC. 2, DUN HUA S. ROAD
TAIPEI, 106
TAIWAN

EXAMINER
BUTLER, DENNIS

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 02/14/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 491 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 491 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/713,220	WOLFE ET AL.	
	Examiner	Art Unit	
	DENNIS M. BUTLER	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment and remarks received on November 29, 2012*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *1-23*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.

   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/DENNIS M BUTLER/
Primary Examiner, Art Unit 2115

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12713220	WOLFE ET AL.
	Examiner	**Art Unit**
	DENNIS M BUTLER	2115

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/23/2012	02/06/2013							
	1	✓	=							
	2	✓	=							
	3	✓	=							
	4	✓	=							
	5	✓	=							
	6	✓	=							
	7	✓	=							
	8	✓	=							
	9	✓	=							
	10	✓	=							
	11	✓	=							
	12	✓	=							
	13	✓	=							
	14	✓	=							
	15	✓	=							
	16	✓	=							
	17	✓	=							
	18	✓	=							
	19	✓	=							
	20	✓	=							
	21	✓	=							
	22	✓	=							
	23	✓	=							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12713220	WOLFE ET AL.
	Examiner	**Art Unit**
	DENNIS M BUTLER	2115

CPC- SEARCHED

Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED

Symbol	Date	Examiner

US CLASSIFICATION SEARCHED

Class	Subclass	Date	Examiner

SEARCH NOTES

Search Notes	Date	Examiner
EAST search attached.	8/22/2012	DB
EAST search attached.	2/6/2013	DB

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
713	320, 322, 501	2/6/2013	DB

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	51739	(plurality multi multiple) adj2 core	US-PGPUB; USPAT	OR	ON	2013/02/06 14:13
L2	22700	1 near5 (processor microprocessor cpu mpu)	US-PGPUB; USPAT	OR	ON	2013/02/06 14:14
L3	3095	1 near5 (set group$3)	US-PGPUB; USPAT	OR	ON	2013/02/06 14:15
L4	2162	2 and 3	US-PGPUB; USPAT	OR	ON	2013/02/06 14:16
L5	36	3 same (domain island)	US-PGPUB; USPAT	OR	ON	2013/02/06 14:20
L6	17	5 and voltage and (clock frequency)	US-PGPUB; USPAT	OR	ON	2013/02/06 14:21
L7	2544	first adj2 pll	US-PGPUB; USPAT	OR	ON	2013/02/06 14:43
L8	2714	second adj2 pll	US-PGPUB; USPAT	OR	ON	2013/02/06 14:44
L9	2354	second adj2 (phase adj lock$2 adj loop)	US-PGPUB; USPAT	OR	ON	2013/02/06 14:45
L10	2131	first adj2 (phase adj lock$2 adj loop)	US-PGPUB; USPAT	OR	ON	2013/02/06 14:46
L11	4110	7 or 10	US-PGPUB; USPAT	OR	ON	2013/02/06 14:46
L12	4631	8 or 9	US-PGPUB; USPAT	OR	ON	2013/02/06 14:46
L13	302	4 and voltage and (clock frequency)	US-PGPUB; USPAT	OR	ON	2013/02/06 14:47
L14	1	11 and 12 and 13	US-PGPUB; USPAT	OR	ON	2013/02/06 14:48

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L15	52331	(plurality multi multiple) adj2 core	US-PGPUB; USPAT; UPAD	OR	ON	2013/02/06 14:49
L16	23119	15 near5 (processor microprocessor cpu mpu)	US-PGPUB; USPAT; UPAD	OR	ON	2013/02/06 14:50
L17	3146	15 near5 (set group$3)	US-PGPUB; USPAT; UPAD	OR	ON	2013/02/06 14:51
L18	2202	16 and 17	US-PGPUB; USPAT; UPAD	OR	ON	2013/02/06 14:51
L19	2547	first adj2 pll	US-PGPUB; USPAT; UPAD	OR	ON	2013/02/06 14:56
L20	2133	first adj2 (phase adj lock$2 adj loop)	US-PGPUB; USPAT; UPAD	OR	ON	2013/02/06 14:56

L21	2720	second adj2 pll	US-PGPUB; USPAT; UPAD	OR	ON	2013/02/06 14:57
L22	2355	second adj2 (phase adj lock$2 adj loop)	US-PGPUB; USPAT; UPAD	OR	ON	2013/02/06 14:57
L23	4114	19 or 20	US-PGPUB; USPAT; UPAD	OR	ON	2013/02/06 14:59
L24	4637	21 or 22	US-PGPUB; USPAT; UPAD	OR	ON	2013/02/06 14:59
L25	308	18 and voltage and (clock frequency)	US-PGPUB; USPAT; UPAD	OR	ON	2013/02/06 15:01
L26	1	23 and 24 and 25	US-PGPUB; USPAT; UPAD	OR	ON	2013/02/06 15:02
L27	404378	(set group$3) near5 (communicat$3 exchang$3 pass$3)	US-PGPUB; USPAT; UPAD	OR	ON	2013/02/06 15:06
L28	1	18 and 24 and 25 and 27	US-PGPUB; USPAT; UPAD	OR	ON	2013/02/06 15:08

2/ 6/ 2013 3:10:23 PM
C:\ Users\ dbutler1\ Documents\ EAST\ Workspaces\ 502930.wsp

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12713220	WOLFE ET AL.
	Examiner	**Art Unit**
	DENNIS M BUTLER	2115

CPC

Symbol	Type	Version

CPC Combination Sets

Symbol	Type	Set	Ranking	Version

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
713	322	G	0	6	F	1 / 08 (2006.01.01)					
CROSS REFERENCE(S)		G	0	6	F	1 / 32 (2006.01.01)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)										
713	320 501										

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 23	
/DENNIS M BUTLER/ Primary Examiner.Art Unit 2115 (Primary Examiner)	2/6/2013 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12713220	WOLFE ET AL.
	Examiner	**Art Unit**
	DENNIS M BUTLER	2115

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 23	
/DENNIS M BUTLER/ Primary Examiner.Art Unit 2115 (Primary Examiner)	2/6/2013 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12713220	WOLFE ET AL.
	Examiner	**Art Unit**
	DENNIS M BUTLER	2115

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17												
2	2	18	18												
3	3	19	19												
4	4	20	20												
5	5	21	21												
8	6	22	22												
9	7	23	23												
10	8														
11	9														
12	10														
13	11														
6	12														
7	13														
14	14														
15	15														
16	16														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 23	
/DENNIS M BUTLER/ Primary Examiner.Art Unit 2115 (Primary Examiner)	2/6/2013 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/713,220	02/26/2010	Andrew WOLFE	121-0019-US-REG	4243

83446 7590 12/03/2012
REN-SHENG INTERNATIONAL IP MANAGEMENT LTD.
GENE I. SU
7F, NO. 57, SEC. 2, DUN HUA S. ROAD
TAIPEI, 106
TAIWAN

EXAMINER
BUTLER, DENNIS

ART UNIT	PAPER NUMBER
2115	

NOTIFICATION DATE	DELIVERY MODE
12/03/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

gsu@suipconsulting.com
filing@suipconsulting.com
gene.i.su@gmail.com

Applicant-Initiated Interview Summary	Application No.	Applicant(s)	
	12/713,220	WOLFE ET AL.	
	Examiner	Art Unit	
	DENNIS M. BUTLER	2115	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Dennis Butler (examiner 2115)*. (3)_____.

(2) *Gene Su (applicant's representative)*. (4)_____.

Date of Interview: *27 November 2012*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☒112 ☒102 ☒103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1,10-13,15 and 18*.

Identification of prior art discussed: *Jacobowitz (2009/0106576), Kim (2009/0138737) and von Kaenel (2010/0188115)*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Claims 15 and 18 were discussed regarding the 112, second paragraph rejection. Applicant's representative agreed to amend the claims to clarify that communication is between the first and second sets of processor cores. Claims 1, 10-13, 15 and 18 were discussed regarding the art rejections under 35 USC 102 and 103. Applicant's representative referred to figure 3 of the specification and stated that clock signals 1 through 3 were different/independent clock signals input to the PLLs while Jacobowitz disclosed using a single reference clock. The examiner agreed that Jacobowitz discloses using a single reference clock and that clock signals 1 through 3 of figure 3 are different than disclosed by Jacobowitz. However, the broadest reasonable interprtation of the recited claim language (i.e.,claim 1: first set of processor cores configured to dynamically receive a first clock signal) reads on the clock output of the local oscillators of Jacobowitz and also reads on the output of the PLLs shown in applicant's figure 3. Applicant's representative stated that he would discuss amends to the claims with applicant regarding clock signals 1 through 3 of figure 3.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/DENNIS M BUTLER/
Primary Examiner, Art Unit 2115

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Andrew WOLFE	§	
	§	Group Art Unit: 2115
Serial No.: 12/713,220	§	
Confirmation No.: 4243	§	
	§	Examiner: BUTLER, DENNIS
Filed: February 26, 2010	§	
For: PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR	§	

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

RESPONSE TO OFFICE ACTION DATED AUGUST 29, 2012

In response to the non-final Office Action dated August 29, 2012 having a shortened statutory period for response set to expire on November 29, 2012, please enter this response and reconsider the claims pending in the application for the reasons discussed below. Although Applicant believes that no fees are due in connection with this response, the Commissioner is hereby authorized to charge Counsel's Deposit Account No. 50-4588/121-0019-US-REG for any fees, including extension of time fees or excess claims fees, required to make this response timely and acceptable to the Office.

Amendments to the Specification are reflected on page 2 of this paper. **Amendments to the Claims** are reflected in the listing of claims which begins on page 3 of this paper. **Remarks** begin on page 8 of this paper.

IN THE SPECIFICATION:

The following paragraph will replace paragraph [0017] in the as filed application:

[0017] Processing for the transition processing routine [[300]]400 may begin at operation [[302]]402, "receive clock frequency change request." Operation [[302]]402 may be followed by operation [[304]]404, "idle communication between stripes." Operation [[304]]404 may be followed by operation [[306]]406, "examine PLL blocks of requesting stripe and adjacent stripe(s)." Operation [[306]]406 may be followed by operation [[308]]408, "does each of PLL blocks acquire a lock?" Operation [[308]]408 may be followed by either operation [[306]]406 when the decision logic tested at block [[308]]408 fails to be satisfied (NO), or operation [[310]]410, "determine whether to resume communication between stripes", when the decision logic tested at block [[308]]408 is satisfied (YES). Processing for the routine may terminate after block [[310]]410.

IN THE CLAIMS:

The listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A multi-core processor, comprising:

a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input;

a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and

an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.

2. (Original) The multi-core processor of claim 1, the interface block further comprising a first level shifter that is referenced to the second supply voltage and adapted to translate first logic levels associated with the first set of processor cores to second logic levels associated with the second set of processor cores for a first signal traveling from the first set of processor cores to the second set of processor cores.

3. (Original) The multi-core processor of claim 1, the interface block further comprising a second level shifter that is referenced to the first supply voltage and adapted to translate second logic levels associated with the second set of processor cores to first logic levels associated with the first set of processor cores for a second signal traveling from the second set of processor cores to the first set of processor cores.

4. (Original) The multi-core processor of claim 1, wherein the interface block further comprises a synchronizer configured to synchronize the first clock signal and the second clock

signal for communication between one or more processor cores of the first set of processor cores and one or more processor cores of the second set of processor cores.

5. (Original) The multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a periphery of the multi-core processor.

6. (Original) The multi-core processor of claim 1, wherein the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located in a second region of the multi-core processor.

7. (Original) The multi-core processor of claim 6, wherein the first region and the second region are overlapping regions of the multi-core processor.

8. (Original) The multi-core processor of claim 6, wherein the first region and the second region are non-overlapping regions of the multi-core processor.

9. (Original) The multi-core processor of claim 6, wherein the first region corresponds to a first row of the multi-core processor, and wherein the second region corresponds to a second row of the multi-core processor.

10. (Currently Amended) The multi-core processor of claim 1, wherein the interface block is configured to idle communications between the first set of processor cores and the second set of processor cores when one or more of the first <u>output</u> clock signal and/or the second <u>output</u> clock signal is determined to have changed.

11. (Currently Amended) The multi-core processor of claim 10, wherein the interface block is configured to resume communication between the first set of processor cores and the second set of processor cores after one or more of the first <u>output</u> clock signal and/or the second <u>output</u> clock signal is determined to have stabilized.

12. (Original) The multi-core processor of claim 5, wherein the first set of processor cores is adjacent to the second set of processor cores, and the one or more control blocks are

configured to select the first supply voltage and the second supply voltage to maintain a differential relationship between the first supply voltage and the second supply voltage.

13. (Original) The multi-core processor of claim 12, wherein the differential relationship is based on having an output voltage level associated with the first set of processor cores to be within an acceptable input voltage level associated with the second set of processor cores.

14. (Original) The multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a common region that is substantially central to the first set of processor cores and the second set of processor cores.

15. (Currently Amended) A method for managing communications in a multi-core processor that includes a plurality of processor cores having a first set of processor cores and a second set of processor cores, the method comprising:

idling communications ~~with one or more of the plurality of processor cores~~between the first set of processor cores and the second set of processor cores in response to a clock frequency change request for the first set of processor cores; and

resuming communications ~~with one or more of the plurality of processor cores~~between the first set of processor cores and the second set of processor cores after having determined that a first phase lock loop operation associated with a first clock signal for the first set of processor cores has acquired a first lock signal and a second phase lock loop operation associated with a second clock signal for the second set of processor cores has also acquired a second lock signal, wherein the first clock signal is independent from the second clock signal.

16. (Original) The method of claim 15, wherein resuming communications further comprising having determined that a third phase lock loop operation associated with a third set of processor cores in the multi-core processor has acquired a third lock signal, wherein the third set of processor cores is adjacent to the first set of processor cores.

17. (Original) The method of claim 16, wherein the second set of processor cores is adjacent to the first set of processor cores.

18. (Currently Amended) A non-transistory computer-readable medium containing a sequence of instructions for managing communications in a multi-core processor that includes a plurality of processor cores having a first set of processor cores and a second set of processor cores, which when executed by a computing device, causes the computing device to:

issue a first command to idle communications ~~with one or more of the plurality of processor cores~~between the first set of processor cores and the second set of processor cores in response to a clock frequency change request for the first set of processor cores;

issue a second command to resume communications ~~with one or more of the plurality of processor cores~~between the first set of processor cores and the second set of processor cores after having determined that a first phase lock loop operation associated with a first clock signal for the first set of processor cores has acquired a first lock signal and a second phase lock loop operation associated with a second clock signal for the second set of processor cores has also acquired a second lock signal, wherein the first clock signal is independent from the second clock signal.

19. (Currently Amended) The non-transistory computer-readable medium of claim 18, further including a sequence of instructions, which when executed by the computing device, causes the computing device to determine whether a third phase lock loop operation associated with a third set of processor cores in the multi-core processor has acquired a third lock signal before issuing the second command, wherein the third set of processor cores is adjacent to the first set of processor cores.

20. (Currently Amended) The non-transistory computer-readable medium of claim 19, wherein the second set of processor cores is adjacent to the first set of processor cores.

21. (Currently Amended) A multi-core processor, comprising:

a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage from a power control block and a first output clock signal from a first phase lock loop (PLL) having a first clock signal as input in a clock control block;

a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive

a second supply voltage from the power control block and a second output clock signal from a second PLL having a second clock signal as input in the clock control block, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and

an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.

22. (Currently Amended) The multi-core processor of claim [[1]]21, wherein the interface block is configured to idle communications between the first set of processor cores and the second set of processor cores when one or more of the first output clock signal and/or the second output clock signal is determined to have changed.

23. (Currently Amended) The multi-core processor of claim [[21]]22, wherein the interface block is configured to resume communication between the first set of processor cores and the second set of processor cores after one or more of the first output clock signal and/or the second output clock signal is determined to have stabilized.

REMARKS

This is intended as a full and complete response to the Office Action dated August 29, 2012, having a shortened statutory period for response set to expire on November 29, 2012. By way of this reply, Applicant is amending claims 1, 10-11, 15, and 18-23. Claims 1 – 23 are pending. Applicant is also amending paragraph [0017] in the as filed application, which describes FIG. 4, to correct typographical errors. No new matter has been added.

Examiner Interview

Applicant thanks Examiner Butler for the November 27, 2012 telephone interview. The interview included discussions of the 35 U.S.C. § 101 rejections, 35 U.S.C. § 112 rejections, 35 U.S.C. § 102, and 35 U.S.C. § 103 rejections in view of the references cited in the Office Action. An agreement was reached regarding the 35 U.S.C. § 101 rejections and the 35 U.S.C. § 112 rejections. Pending the Examiner's further searches, the Examiner acknowledges that the architecture shown and described in the present disclosure differs from the currently cited references.

Applicant respectfully submits that the claims as presented in this response substantially reflect the discussions during the interview.

Claim Objections

Claims 22 – 23 are objected to under 37 CFR 1.75 as allegedly being substantial duplicates of claims 10 and 11. Claims 22 – 23 have been amended to depend on claims 21 and 22, respectively. Claim 21 also recites different elements than claim 1 (e.g., a power control block and a clock control block). Applicant respectfully requests the withdrawal of the claim objections.

35 U.S.C. § 101 Rejection

Claims 18 – 20 are rejected under 35 U.S.C. §101, because the claimed invention is allegedly directed to non-statutory subject matter. The suggested "non-transitory" language has been added, and Applicant respectfully requests the withdrawal of the rejections under 35 U.S.C. §101.

35 U.S.C. § 112 Rejection

Claims 15 – 20 are rejected under 35 U.S.C. §112, second paragraph for being allegedly indefinite and failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. As discussed during the interview, Applicant has amended

independent claims 15 and 18 to clarify that the communication is "between the first set of processor cores and the second set of processor cores." The amendments are at least supported by paragraph [0018] and FIG. 1, FIG. 3, and FIG. 4 of the as filed application. Applicant respectfully requests the withdrawal of the rejections under 35 U.S.C. §112.

35 U.S.C. § 102 Rejections

Claims 1, 5 – 6, 8 – 9, 14 and 21 are rejected under 35 U.S.C. §102(e) as being allegedly anticipated by U.S. Patent Application Publication 2009/0106576 (hereinafter *Jacobowitz*).

Applicant does not concede that the above reference is prior art and reserves the right to challenge the reference at a later date. Further, Applicant respectfully submits that the rejections are overcome for at least the reasons stated below.

To anticipate a claim, the alleged reference must teach each and every element of the claim. Applicant respectfully submits that *Jacobowitz* does not teach or suggest one or more elements of the amended independent claims 1 and 21. Specifically, *Jacobowitz* does not teach or suggest at least the elements of "a first set of processor cores… configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (LLP) having a first clock signal as input," "a second set of processor cores… configured to dynamically received a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal." The claim amendments are at least supported by paragraph [0015] and FIG. 3 of the as filed application.

First, *Jacobowitz* fails to disclose or teach a first set of processor cores and second set of processor cores configured to dynamically receive a first supply voltage and a second supply voltage, respectively. In addition, the first supply voltage is <u>independent from</u> the second supply voltage, as required in the amended independent claims 1 and 21. Paragraph [0043] of *Jacobowitz* merely mentions that "[f]urther power management can be realized by controlling the power supply voltage (Vdd) to each core and/or chip." In other words, *Jacobowitz* is silent with respect to least the recited different <u>sets of processor cores</u> configured to receive <u>independent</u> supply voltages.

Second, FIG. 6 and all other figures of *Jacobowitz* clearly show that the microprocessor chip (e.g., 600) receives a system reference oscillator clock frequency (v_R) and distributes v_R to local oscillators 108. <u>See</u> *Jacobowitz*, paragraphs [0037]-[0038] and FIG. 6. *Jacobowitz* fails to

disclose or teach a first set of processor cores and second set of processor cores configured to dynamically receive a first output clock signal of a first PLL having a first clock signal as input and a second output clock signal of a second PLL having a second clock signal as input, respectively. In addition, the first clock signal is independent from the second clock signal, as required in the amended independent claims 1 and 21.

For at least the reasons set forth above, the amended independent claims 1 and 21 and the related dependent claims 2 – 14 and 22 – 23 are patentable over *Jacobowitz*. Applicant respectfully requests the withdrawal of the rejections under 35 U.S.C. §102.

35 U.S.C. § 103 Rejections

Claims 2 – 4, 7, 12 and 13 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over *Jacobowitz* in view of U.S. Patent Application Publication 2009/0138737 (hereinafter *Kim*).

Claims 10 – 11, 15 – 20 and 22 – 23 rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over *Jacobowitz* in view of Kim and further in view of U.S. Patent Application Publication 2010/0188115 (hereinafter *von Kaenel*).

Applicant does not concede that the aforementioned references are prior art and reserves the right to challenge these references at a later date. Further Applicant respectfully submits that these rejections are overcome for at least the reasons stated below.

To establish a *prima facie* case of obviousness required for a §103(a) rejection, the references must teach or suggest all the claim elements.

Claims 2 – 4, 7, 12 and 13

As discussed during the interview, *Kim* discloses a different architecture than the one recited in the present disclosure. Specifically, as shown in FIG. 1 and FIG. 2 of *Kim*, *Kim* fails to disclose or teach a first set of processor cores and second set of processor cores configured to dynamically receive a first supply voltage and a second supply voltage, which is independent from the first supply voltage, respectively. Instead, *Kim* discloses having each core, not a set of processor cores, received a V_{DD} (i.e., V_{DD1}, V_{DD2}, V_{DD3}, and V_{DD4}).

In addition, *Kim* also fails to disclose or teach a first set of processor cores and second set of processor cores configured to dynamically receive a first output clock signal of a first PLL having a first clock signal as input and a second output clock signal of a second PLL having a second clock signal, respectively. In addition, the first clock signal is independent from the second clock signal. Instead, *Kim* discloses the apparatus comprising a multi-core processor (i.e., 100 in FIG. 1 or 200 in FIG. 2) having a single clock source (i.e., 170 in FIG. 1 or 270 in

FIG. 2). The clock signal from this single clock source is then processed (i.e., divided or multiplied) and provided to each of the cores. See *Kim*, paragraphs [0024]-[0025] and FIGs 1 – 2.

Moreover, the Examiner acknowledges that *Jacobowitz* does not disclose the recited first and second level shifters in claims 2 and 3. See Office Action, page 7. *Kim* merely discloses a voltage level-translating communication transceiver 180 that is "configured to enable communications between each of the plurality of cores 110, 120, 130, and 140." See *Kim*, paragraph [0024]. *Kim* is silent with respect to the recited "first level shifter that is referenced to the second supply voltage" (which is independent from the first supply voltage) and "adapted to translate… for a first signal traveling from the first set of processor cores to the second set of processor cores" in claim 2. *Kim* is also silent with respect to the recited "second level shifter that is referenced to the first supply voltage" and "adapted to translate… for a second signal traveling from the second set of processor cores to the first set of processor cores."

For at least the reasons set forth above, *Kim* fails to cure the deficiencies of *Jacobowitz*.

Claims 10 – 11, 15, 18 and 22 – 23

The Examiner acknowledges neither *Jacobowitz* nor *Kim* discloses the recited operations of idling communications and resuming communications. See Office Action, page 8. Applicant respectfully submits that none of *Jacobowitz*, *Kim*, and *von Kaenel* discloses or teaches at least "resuming communications… after having determined that a first phase lock loop operation associated with a first clock signal for the first set of processor cores has acquired a first lock signal and a second phase lock loop operation associated with a second clock signal for the second set of processor cores has also acquired a second lock signal, wherein the first clock signal is independent from the second clock signal," as required in the amended independent claims 15 and 18.

As discussed above, neither *Jacobowitz* nor *Kim* discloses having sets of processor cores configured to receive multiple and independent clock signals. In conjunction with its FIG. 9, *von Kaenel* merely describes "wait[ing] for the clock generation circuit to lock to the new frequency (block 148)" in paragraph [0074]. *von Kaenel* is silent with respect to at least the recited elements of "idling communication… in response to a clock frequency change request" and "resuming communication" after having determined the acquisition of PLL lock signals associated with multiple independent clock signals.

For at least the reasons set forth above, *von Kaenel* fails to cure the deficiencies of *Jacobowitz* and *Kim*.

Thus, claims 2 – 4, 7, 10 – 13, 15 – 20, and 22 - 23 are patentable over *Jacobowitz*, *Kim*, and *von Kaenel*. Applicant respectfully requests the withdrawal of the rejections under 35 U.S.C. §103.

CONCLUSION

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that the claims be allowed. If there are any questions about any of the foregoing, please contact Applicant's undersigned representative.

Respectfully submitted,

/Gene Su/
Gene Su
Attorney for Applicant(s)
Registration No. 45,140

Telephone: (886) 2.2700.7882
Facsimile 1: (886) 2.2700.7856
Facsimile 2: (650) 644.3217
Email: filing@suipconsulting.com

Electronic Acknowledgement Receipt

EFS ID:	14346671
Application Number:	12713220
International Application Number:	
Confirmation Number:	4243
Title of Invention:	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR
First Named Inventor/Applicant Name:	Andrew WOLFE
Customer Number:	83446
Filer:	Gene I. Su
Filer Authorized By:	
Attorney Docket Number:	121-0019-US-REG
Receipt Date:	29-NOV-2012
Filing Date:	26-FEB-2010
Time Stamp:	22:23:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	121-0019-US-REG_ROA.pdf	96145 03109273c69e0784d954fcd6c734ea6d9110a82c	no	13

Warnings:

Information:

Total Files Size (in bytes):	96145

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/713,220	02/26/2010	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 11/29/2012	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 23	Minus	** 23	= 0	X $ =		OR	X $62=	0
Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X $ =		OR	X $250=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/ANTHONY WILLIAMS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/713,220	02/26/2010	Andrew WOLFE	121-0019-US-REG	4243

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TAIWAN

EXAMINER
BUTLER, DENNIS

ART UNIT	PAPER NUMBER
2115	

NOTIFICATION DATE	DELIVERY MODE
08/29/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

gsu@suipconsulting.com
filing@suipconsulting.com
gene.i.su@gmail.com

Office Action Summary	Application No.	Applicant(s)	
	12/713,220	WOLFE ET AL.	
	Examiner	Art Unit	
	DENNIS M. BUTLER	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-23* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-23* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *26 February 2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/2/2011*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

This action is in response to the application filed on February 26, 2010. Claims 1-23 are pending.

Claim Objections

Applicant is advised that should claims 10 and 11 be found allowable, claims 22 and 23 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 18-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The claims are directed to a medium that has been defined in the specification as a transmission type medium such as a wireless communication channel or link (at paragraph 22) that is a signal. Signals are not statutory under 35 USC 101 because they do not fit any of the four statutory categories. The

claim language would be improved if applicant amended the claims to recite " a non-transitory computer readable medium".

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 15-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 15 and 18, the claims are vague and indefinite as to the relationship between idling/resuming communications with one or more of the plurality of processor cores and the first and second sets of processor cores. The claims are unclear whether the communications are between one or more cores and some internal or external component, between cores of the same set or between cores of different sets.

Claims 16-17 and 19-20 are rejected because they incorporate the deficiencies of claims 15 and 18 respectively.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

.

Claims 1, 5-6, 8-9, 14 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Jacobowitz et al., U.S. Patent Application Publication 2009/0106576.

Per claim 1:

A) Jacobowitz et al teach the following claimed items:

1. a first set of processor cores of the multi-core processor configured to dynamically receive a first supply voltage and a first clock signal with the V0 cores 102 (top set) of figure 6 and paragraphs 32, 34, 37-38 and 43;

2. a second set of processor cores of the multi-core processor configured to dynamically receive a second supply voltage and a second clock signal with the V1 cores 102 (bottom set) of figure 6 and paragraphs 32, 34, 37-38 and 43;

3. an interface block coupled to the first and second sets of cores and configured to facilitate communication between the first and second sets of cores with internal cluster fabric 206, MCM fabric controller 208 and fabric 210 of figure 2 and paragraph 28.

Per claims 5-6, 8-9 and 14:

Jacobowitz discloses that the first and second sets of cores are configured to receive control signals from one or more control blocks located in a periphery of

the multi-core processor with the 2ND level distribution function block and/or the local store vData and distribution block. Jacobowitz discloses locating the first set of cores in a first region/row and the second set of cores in a second region/row, the regions are non-overlapping with figure 6. Jacobowitz discloses that the first and second sets of cores are configured to receive control signals from one or more control blocks located in a common region of the multi-core processor with the 2ND level distribution function block 502.

Per claim 21:

A) Jacobowitz et al teach the following claimed items:

1. a first set of processor cores of the multi-core processor configured to dynamically receive a first supply voltage from a power control block (local power grid controller) and a first clock signal from a clock control block (local core clock controller) with the V0 cores 102 (top set) of figure 6 and paragraphs 32, 34, 37-38 and 43;

2. a second set of processor cores of the multi-core processor configured to dynamically receive a second supply voltage from a power control block (local power grid controller) and a second clock signal from a clock control block (local core clock controller) with the V1 cores 102 (bottom set) of figure 6 and paragraphs 32, 34, 37-38 and 43;

3. an interface block coupled to the first and second sets of cores and configured to facilitate communication between the first and second sets of cores

with internal cluster fabric 206, MCM fabric controller 208 and fabric 210 of figure 2 and paragraph 28.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 2-4, 7, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobowitz et al., U.S. Patent Application Publication 2009/0106576 in view of Kim et al., U.S. Patent Application Publication 2009/0138737.

Per claims 2 and 3:

Jacobowitz discloses a multi-core processor including an interface block configured to facilitate communication as described above in connection to the rejection of claim 1. Jacobowitz does not disclose first and second level shifters adapted to translate logic levels as claimed. Kim teaches that it is known to include first and second level shifters adapted to translate logic levels in a multi-core processor with voltage level translating communication transceiver 180 of figure 1 and at paragraph 24. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include first and second level shifters adapted to translate logic levels in a multi-core processor, as taught by Kim, in order to enable communication between each of the cores that are operating at different voltage levels.

Per claims 4, 7, 12 and 13:

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include a synchronizer in the multi-core processor of Jacobowitz because Jacobowitz discloses providing dynamically programmable local oscillators for each set of cores and synchronizing the core clock signals would allow for synchronous communication of data between the cores. Jacobowitz discloses placing sets of cores in non-overlapping regions of the processor. However, placing sets of cores in overlapping regions of the processor is an obvious design choice and would have been obvious to one of ordinary skill in the art in view of Jacobowitz's disclosure of including a plurality of sets of cores in a multi-core processor. Kim discloses maintaining a differential

relationship between the first and second supply voltages with voltage level translating communication transceiver 180 of figure 1 and at paragraph 24.

Claims 10-11,15-20 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobowitz et al., U.S. Patent Application Publication 2009/0106576 in view of Kim et al., U.S. Patent Application Publication 2009/0138737 and further in view of von Kaenel, U.S. Patent Application Publication 2010/0188115.

Per claims 10-11,15, 18 and 22-23:

Jacobowitz discloses a multi-core processor including first and second sets of cores and an interface block configured to facilitate communication between cores as described above in connection to the rejection of claim 1. Jacobowitz does not disclose idling communications and resuming communications as claimed. Kim discloses that it is known to use first and second PLLs for managing communications in a multi-core processor with PLL1-4 of figure 2 and paragraph 25. While Kim does not explicitly disclose idling communications in response to a change in frequency request and resuming communications when the PLLs have locked/stabilized the requested clock, von Kaenel discloses that it is known to stop core activity when changing frequency and waiting until lock before resuming activity with figure 9 and paragraphs 73-76. It would have been obvious to one having ordinary skill in the art at the time the invention was made to idle communications with one or more of the plurality of cores in response to a clock frequency change request for the first set of cores and resume

communications with one or more of the plurality of cores after having determined that a first phase lock loop operation associated with the first set of cores has acquired a first lock signal and a second phase lock loop operation associated with the second set of cores has also acquired a second lock signal in order to avoid the unpredictable effects of communicating while the PLL is being programmed with the new frequency and has not locked on the new frequency.

Per claims 16-17 and 19-20:

It would have been obvious to one having ordinary skill in the art at the time the invention was made to add a third PLL for a third set of processor cores in order to gain the cumulative effect of increasing processing power and/or flexibility by increasing the number of sets of processor cores. Jacobowitz discloses locating sets of cores adjacent to each other with figures 2 and 6.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DENNIS M. BUTLER whose telephone number is (571)272-3663. The examiner can normally be reached on M-F from 9:00 to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee, can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://portal.uspto.gov/external/portal.

Should you have questions on access to the Private PAIR system, contact the

Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/DENNIS M BUTLER/
Primary Examiner, Art Unit 2115

DENNIS M BUTLER
Primary Examiner
Art Unit 2115

Notice of References Cited	Application/Control No. 12/713,220	Applicant(s)/Patent Under Reexamination WOLFE ET AL.	
	Examiner DENNIS M. BUTLER	Art Unit 2115	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2010/0188115	07-2010	von Kaenel, Vincent R.	326/16
*	B	US-2010/0162018	06-2010	SUBRAMANIAN et al.	713/322
*	C	US-2009/0106576	04-2009	Jacobowitz et al.	713/501
*	D	US-2009/0138737	05-2009	Kim et al.	713/322
*	E	US-7,248,838	07-2007	Goodnow et al.	455/70
*	F	US-8,225,315	07-2012	Cheng et al.	718/1
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	12713220
Filing Date	2010-02-26
First Named Inventor	Andrew WOLFE
Art Unit	2115
Examiner Name	LEE, THOMAS C
Attorney Docket Number	121-0019-US-REG

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/D.B./	1	7735037		2010-06-08	TELL	entire document, especially Abstract; para [0030], [0035], [0054], [0058], [0127], [0163]
/D.B./	2	7853808		2010-12-14	KIM et al.	entire document, especially Abstract; Fig.2; para [0004], [0005], [0006], [0011], [0032], [0034], [0035], [0043], [0044], [0048], [0054]
/D.B./	3	7263457		2007-08-28	WHITE et al.	entire document, especially Abstract; para [0004], [0006], [0009], [0010], [0017], [0032], [0033], [0037]

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

Receipt date: 08/02/2011	Application Number	12713220 12713220 - GAU: 2115
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2010-02-26
	First Named Inventor	Andrew WOLFE
	Art Unit	2115
	Examiner Name	LEE, THOMAS C
	Attorney Docket Number	121-0019-US-REG

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
/D.B./	1	NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, May 17, 2011	☐

If you wish to add additional non-patent literature document citation information please click the Add button **Add**

EXAMINER SIGNATURE

Examiner Signature	/Dennis Butler/	Date Considered	08/22/2012

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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BIB DATA SHEET

CONFIRMATION NO. 4243

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/713,220	02/26/2010 **RULE**	713	2115	121-0019-US-REG

APPLICANTS

Andrew WOLFE, Los Gatos, CA;
Marc Elliot LEVITT, San Jose, CA;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

03/04/2010

Foreign Priority claimed	☐ Yes ☑ No		STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
35 USC 119(a-d) conditions met	☐ Yes ☑ No	☐ Met after Allowance				
Verified and Acknowledged	/DENNIS BUTLER/ Examiner's Signature	Initials	CA	5	20	3

ADDRESS

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GENE I. SU
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TAIPEI, 106
TAIWAN

TITLE

PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR

FILING FEE RECEIVED		
1414	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12713220	WOLFE ET AL.
	Examiner	**Art Unit**
	DENNIS M BUTLER	2115

SEARCHED

Class	Subclass	Date	Examiner

SEARCH NOTES

Search Notes	Date	Examiner
EAST search attached.	8/22/2012	DB

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12713220	WOLFE ET AL.
	Examiner	**Art Unit**
	DENNIS M BUTLER	2115

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/23/2012								
	1	✓								
	2	✓								
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	5	✓								
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	18	✓								
	19	✓								
	20	✓								
	21	✓								
	22	✓								
	23	✓								

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3	("7263457" | "7735037" | "7853808").PN.	US-PGPUB; USPAT	OR	ON	2012/08/22 10:43
L2	5638	((plurality multi multiple) adj3 core) with (set group$3)	US-PGPUB; USPAT	OR	ON	2012/08/22 11:06
L3	76	2 same (domain island)	US-PGPUB; USPAT	OR	ON	2012/08/22 11:11
L4	20	3 and voltage and (clock frequency)	US-PGPUB; USPAT	OR	ON	2012/08/22 11:11
L5	11	4 and (interfac$3 near5 core)	US-PGPUB; USPAT	OR	ON	2012/08/22 11:12
L6	9	4 not 5	US-PGPUB; USPAT	OR	ON	2012/08/22 11:33
L7	76170	phase$1 adj lock$2 adj loop$2	US-PGPUB; USPAT	OR	ON	2012/08/22 12:04
L8	21563	lock$2 adj2 signal	US-PGPUB; USPAT	OR	ON	2012/08/22 12:05
L9	3681	7 same 8	US-PGPUB; USPAT	OR	ON	2012/08/22 12:05
L10	2567	7 with 8	US-PGPUB; USPAT	OR	ON	2012/08/22 12:05
L11	26	2 and 10	US-PGPUB; USPAT	OR	ON	2012/08/22 12:06
L12	2019	(core near3 (set group$3)) with (communicat$3 exchang$3 pass$3)	US-PGPUB; USPAT	OR	ON	2012/08/22 12:09
L13	1	11 and 12	US-PGPUB; USPAT	OR	ON	2012/08/22 12:09
L14	25	11 not 13	US-PGPUB; USPAT	OR	ON	2012/08/22 12:10
L15	1	10 and 12	US-PGPUB; USPAT	OR	ON	2012/08/22 12:16
L16	1	9 and 12	US-PGPUB; USPAT	OR	ON	2012/08/22 12:17
L17	126534	core with (communicat$3 exchang$3 pass$3)	US-PGPUB; USPAT	OR	ON	2012/08/22 12:18
L18	194	10 and 17	US-PGPUB; USPAT	OR	ON	2012/08/22 12:19
L19	8	18 and (chang$3 adj3 (clock frequency))	US-PGPUB; USPAT	OR	ON	2012/08/22 12:20
L20	286	9 and 17	US-PGPUB; USPAT	OR	ON	2012/08/22 12:42
L21	68	20 and (chang$3 adj3 (clock frequency))	US-PGPUB; USPAT	OR	ON	2012/08/22 12:42
L22	60	21 not 19	US-PGPUB; USPAT	OR	ON	2012/08/22 12:42

L23	2019	12 same 17	US-PGPUB; USPAT	OR	ON	2012/08/22 12:53
L24	1	9 and 23	US-PGPUB; USPAT	OR	ON	2012/08/22 12:54
L25	67	7 and 23	US-PGPUB; USPAT	OR	ON	2012/08/22 12:54
L26	1	8 and 23	US-PGPUB; USPAT	OR	ON	2012/08/22 12:54
L27	66	25 not (26 or 21)	US-PGPUB; USPAT	OR	ON	2012/08/22 12:58

8/22/2012 2:01:32 PM
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/713,220	02/26/2010	Andrew WOLFE	121-0019-US-REG

CONFIRMATION NO. 4243

PUBLICATION NOTICE

OC000000049630276

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TAIPEI, 106
TAIWAN

Title:PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR

Publication No.US-2011-0213991-A1
Publication Date:09/01/2011

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

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In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
GENE SU
REN-SHENG INTERNATIONAL IP
MANAGEMENT LTD.
7F, NO. 57, SEC. 2, DUN HUA S. ROAD
106 TAIPEI
TAIWAN, PROVINCE OF CHINA

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

	Date of mailing *(day/month/year)* 17 MAY 2011
Applicant's or agent's file reference 121-0019-PCT	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US 11/24477	International filing date *(day/month/year)* 11 February 2011 (11.02.2011)
Applicant EMPIRE TECHNOLOGY DEVELOPMENT LLC	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70

   For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 – 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. Following the expiration of 30 months from the priority date, these comments will also be made available to the public.

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90*bis*.1 and 90*bis*.3).

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

Name and mailing address of the ISA/ Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer Lee W. Young PCT Helpdesk: 571-272-4300 Telephone No. PCT OSP: 571-272-7774

Form PCT/ISA/220 (July 2010)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 121-0019-PCT	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US 11/24477	International filing date *(day/month/year)* 11 February 2011 (11.02.2011)	(Earliest) Priority Date *(day/month/year)* 26 February 2010 (26.02.2010)
Applicant EMPIRE TECHNOLOGY DEVELOPMENT LLC		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      ☒ the international application in the language in which it was filed.
      ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 2
      ☒ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figures is to be published with the abstract.

Form PCT/ISA/210 (first sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 11/24477

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G06F 13/36 (2011.01)
USPC - 710/306
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 710/306

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 710/1, 33, 56, 315; 370/351, 389, 402; 702/127, 130, 132; 714/699, 746, 752, 755; 711/E12.023 (keyword limited - see search terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWEST (PGPB, USPT, USOC, EPAB, JPAB); GOOGLE; Google Scholar
Terms: processors, multi, core, chip, die, cache, interface, communication, voltage, clock, shift, power, supply, synchronize, timing, shifter, differential.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2007/0174586 A1 (TELL) 26 July 2007 (26.07.2007) entire document, especially Abstract; para [0030], [0035], [0054], [0058], [0127], [0163]	1-20
Y	US 2008/0178023 A1 (KIM et al.) 24 July 2008 (24.07.2008) entire document, especially Abstract; Fig. 2; para [0004], [0005], [0006], [0011], [0032], [0034], [0035], [0043], [0044], [0048], [0054]	1-20
A	US 2007/0156370 A1 (WHITE et al.) 05 July 2007 (05.07.2007) entire document, especially Abstract; para [0004], [0006], [0009], [0010], [0017], [0032], [0033], [0037]	1-20

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
09 May 2011 (09.05.2011)	17 MAY 2011
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To: GENE SU
REN-SHENG INTERNATIONAL IP
MANAGEMENT LTD.
7F, NO. 57, SEC. 2, DUN HUA S. ROAD
106 TAIPEI
TAIWAN, PROVINCE OF CHINA

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	17 MAY 2011
Applicant's or agent's file reference 121-0019-PCT	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US 11/24477	11 February 2011 (11.02.2011)	26 February 2010 (26.02.2010)

International Patent Classification (IPC) or both national classification and IPC
IPC(8) - G06F 13/36 (2011.01)
USPC - 710/306

Applicant EMPIRE TECHNOLOGY DEVELOPMENT LLC

1. This opinion contains indications relating to the following items:

- [X] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [X] Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer:
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	09 May 2011 (09.05.2011)	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/237 (cover sheet) (July 2009)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 11/24477

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:
   - [X] the international application in the language in which it was filed.
   - [ ] a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. [ ] This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:
   a. (means)
   - [ ] on paper
   - [ ] in electronic form

   b. (time)
   - [ ] in the international application as filed
   - [ ] together with the international application in electronic form
   - [ ] subsequently to this Authority for the purposes of search

4. [ ] In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 11/24477

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-20	YES
	Claims	None	NO
Inventive step (IS)	Claims	None	YES
	Claims	1-20	NO
Industrial applicability (IA)	Claims	1-20	YES
	Claims	None	NO

2. Citations and explanations:

Claims 1-20 lack an inventive step under PCT Article 33(3) as being obvious over US 2007/0174586 A1 (Tell) in view of US 2008/0178023 A1 to Kim et al. (hereinafter, 'Kim').

Regarding claim 1, Tell teaches a multi-core processor (processor 54 may comprise any one of several alternative processing circuit cores capable of executing machine-readable instructions provided according to a programmable processing instruction set, para [0058]), comprising: a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first clock signal (processor 54 may at least in part control and/or adjust one or more timing characteristics and/or one or more voltage characteristics of signals 84 in multiple, independent closed feedback loops, para [0054]). Tell does not expressly teach a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second clock signal; and an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores. However Kim, in an analogous art, teaches a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second clock signal (on a multi-core processor system chip by supplying a nominal power supply voltage to a first processing core and a second core power supply voltage to a second processing core, the second core power supply voltage greater or lower than the nominal power supply voltage, para [0006]); and an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores (controlled by a controller 210. It is known that each of the individual processing cores 202, 204, 206, 208 may evidence divergent clock rates f.sub.CLK, k in response to similar operational inputs and operating environments. For example, in response to the same nominal power supply voltage V.sub.DDnom the first core 102 may exhibit an impermissibly slow clock rate relative to a minimum reference clock speed (f.sub.CLK, k,<f.sub.spec), the second core 104 may exhibit an impermissibly fast clock rate relative to a maximum clock speed, para [0032]; Fig.2). It would have been obvious to one skilled in the art to combine the teachings of Tell with those of Kim in order to more efficiently tailor individual operating environments in a multi core processor system (see Kim para [0004]-[0005]).

Regarding claim 2, Kim further teaches the interface block further comprising a first level shifter that is referenced to the second supply voltage and adapted to translate first logic levels associated with the first set of processor cores to second logic levels associated with the second set of processor cores for a first signal traveling from the first set of processor cores to the second set of processor cores (raise or lower each core supply voltage V.sub.DD, k as needed until each core meets specifications, thus enabling the MCP chip to pass both minimum and maximum core clock rate specifications in the present example, para [0043]).

Regarding claim 3, Kim further teaches the interface block further comprising a second level shifter that is referenced to the first supply voltage and adapted to translate second logic levels associated with the second set of processor cores to first logic levels associated with the first set of processor cores for a second signal traveling from the second set of processor cores to the first set of processor cores (repetitive lowering iterations in order to enable graduated and/or incremental voltage lowering of each supply voltage V.sub.DD, k (for example, at steps 310 and 312 above) by the controller, which may gradually lower a core supply voltage V.sub.DD, k for each core 202,204,206,208 to determine the lowest supply voltage at which each individual core will evidence a clock rate required by specifications, para [0044]).

Regarding claim 4, Kim further teaches wherein the interface block further comprises a synchronizer configured to synchronize the first clock signal and the second clock signal for communication between one or more processor cores of the first set of processor cores and one or more processor cores of the second set of processor cores (if individual cores are required to meet a maximum clock rate specification, then the present invention may provide a means for verifying that each core k meets said specification. Thus, in one example illustrated in FIG. 6, subsequent to determining each core's adjusted power supply voltage V.sub.Min, k at 316 or 318 as described above, the core clock rate f.sub.CLK, k at V.sub.Min, k is compared to a specified maximum rate, para [0048]).

Regarding claim 5, Tell further teaches wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a periphery of the multi-core processor (Comparator 480 compares the incoming data signals from lines 330 with a reference voltage level, V.sub.ref, which is adjusted by threshold control circuitry 490. Threshold control circuitry 490 may respond to an adjustment signal from processor 54 stored in threshold control register, para [0127]).

---continued in supplemental box---

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 11/24477

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:
Box No. V.2. Citations and explanations.

Regarding claim 6, Kim further teaches wherein the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located in a second region of the multi-core processor (first and second individual processing cores formed on a unitary chip structure, each core connected to first and second adjustable power supplies, para [0011]).

Regarding claim 7, Kim further teaches wherein the first region and the second region are overlapping regions of the multi-core processor (first and second individual processing cores formed on a unitary chip structure, each core connected to first and second adjustable power supplies, para [0011]; the MCP 712 can read and/or write data to/from memory 732, storage system 716, and/or I/O interface, para [0054]).

Regarding claim 8, Kim further teaches wherein the first region and the second region are non-overlapping regions of the multi-core processor (first and second individual processing cores formed on a unitary chip structure, each core connected to first and second adjustable power supplies, para [0011]; the MCP 712 can read and/or write data to/from memory 732, storage system 716, and/or I/O interface, para [0054]).

Regarding claim 9, Kim further teaches wherein the first region corresponds to a first row of the multi-core processor, and wherein the second region corresponds to a second row of the multi-core processor (Fig. 2, communication block 220 may be located between the controller 210 and the cores 202,204,206,208, para [0035]).

Regarding claim 10, Kim further teaches wherein the interface block is configured to idle communications between the first set of processor cores and the second set of processor cores when one or more of the first clock signal and/or the second clock signal is determined to have changed (raise the clock rate of cores that do not meet a minimum reference clock speed, thereby enabling an otherwise failing MCP chip 200 to pass a minimum reference clock specification, para [0043]).

Regarding claim 11, Kim further teaches wherein the interface block is configured to resume communication between the first set of processor cores and the second set of processor cores after one or more of the first clock signal and/or the second clock signal is determined to have stabilized (raise the clock rate of cores that do not meet a minimum reference clock speed, thereby enabling an otherwise failing MCP chip 200 to pass a minimum reference clock specification, para [0043]).

Regarding claim 12, Tell further teaches wherein the first set of processor cores is adjacent to the second set of processor cores, and the one or more control blocks are configured to select the first supply voltage and the second supply voltage to maintain a differential relationship between the first supply voltage and the second supply voltage (the interconnection between circuit elements or circuit blocks may be shown or described as multi-conductor or single conductor signal lines. Each of the multi-conductor signal lines may alternatively be single-conductor signal lines, and each of the single-conductor signal lines may alternatively be multi-conductor signal lines. Signals and signaling paths shown or described as being single-ended may also be differential, para [0163]).

Regarding claim 13, Kim further teaches wherein the differential relationship is based on having an output voltage level associated with the first set of processor cores to be within an acceptable input voltage level associated with the second set of processor cores (controller 210 means is configured to individually select and adjust a supply voltage V.sub.DD, k supplied to each core 202,204,206,208 by its respective adjustable power supply, para [0034]).

Regarding claim 14, Kim further teaches wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a common region that is substantially central to the first set of processor cores and the second set of processor cores (Comparator 480 compares the incoming data signals from lines 330 with a reference voltage level, V.sub.ref, which is adjusted by threshold control circuitry 490. Threshold control circuitry 490 may respond to an adjustment signal from processor 54 stored in threshold control register, para [0127]).

Regarding claim 15, Tell teaches a method for managing communications (a link may carry or communicate information in the form of a signal from a transmitting device to a receiving device, para [0030]) in a multi-core processor that includes a plurality of processor cores having a first set of processor cores and a second set of processor cores (processor 54 may comprise any one of several alternative processing circuit cores capable of executing machine-readable instructions provided according to a programmable processing instruction set, para [0058]), the method comprising: resuming communications with one or more of the plurality of processor cores after having determined that a first phase lock loop operation associated with the first set of processor cores has acquired a first lock signal and a second phase lock loop operation associated with the second set of processor cores has also acquired a second lock signal (a timing comparison signal may indicate a difference between a phase of an input signal and a phase of a reference signal, para [0035]). Tell does not expressly teach idling communications with one or more of the plurality of processor cores in response to a clock frequency change request for the first set of processor cores. However Kim, in an analogous art, teaches idling communications with one or more of the plurality of processor cores in response to a clock frequency change request for the first set of processor cores (raise the clock rate of cores that do not meet a minimum reference clock speed, thereby enabling an otherwise failing MCP chip 200 to pass a minimum reference clock specification, para [0043]). It would have been obvious to one skilled in the art to combine the teachings of Tell with those of Kim in order to more efficiently tailor individual operating environments in a multi core processor system (see Kim para [0004]-[0005]).

Regarding claim 16, Tell further teaches wherein resuming communications further comprising having determined that a third phase lock loop operation associated with a third set of processor cores in the multi-core processor has acquired a third lock signal, wherein the third set of processor cores is adjacent to the first set of processor cores (a timing comparison signal may indicate a difference between a phase of an input signal and a phase of a reference signal, para [0035]).

---continued in supplemental box---

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 11/24477

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:
Box No. V.2. Citations and explanations.

Regarding claim 17, Kim further teaches wherein the second set of processor cores is adjacent to the first set of processor cores (first and second individual processing cores formed on a unitary chip structure, each core connected to first and second adjustable power supplies, para [0011]; the MCP 712 can read and/or write data to/from memory 732, storage system 716, and/or I/O interface, para [0054]).

Regarding claim 18, Tell teaches a computer-readable medium containing a sequence of instructions for managing communications (a link may carry or communicate information in the form of a signal from a transmitting device to a receiving device, para [0030]) in a multi-core processor that includes a plurality of processor cores having a first set of processor cores and a second set of processor cores (processor 54 may comprise any one of several alternative processing circuit cores capable of executing machine-readable instructions provided according to a programmable processing instruction set, para [0058]), which when executed by a computing device, causes the computing device to: issue a second command to resume communications with one or more of the plurality of processor cores after having determined that a first phase lock loop operation associated with the first set of processor cores has acquired a first lock signal and a second phase lock loop operation associated with the second set of processor cores has also acquired a second lock signal (a timing comparison signal may indicate a difference between a phase of an input signal and a phase of a reference signal, para [0035]). Tell does not expressly teach issue a first command to idle communications with one or more of the plurality of processor cores in response to a clock frequency change request for the first set of processor cores. However Kim, in an analogous art, teaches issue a first command to idle communications with one or more of the plurality of processor cores in response to a clock frequency change request for the first set of processor cores (raise the clock rate of cores that do not meet a minimum reference clock speed, thereby enabling an otherwise failing MCP chip 200 to pass a minimum reference clock specification, para [0043]). It would have been obvious to one skilled in the art to combine the teachings of Tell with those of Kim in order to more efficiently tailor individual operating environments in a multi core processor system (see Kim para [0004]-[0005]).

Regarding claim 19, Tell further teaches a sequence of instructions, which when executed by the computing device, causes the computing device to determine whether a third phase lock loop operation associated with a third set of processor cores in the multi-core processor has acquired a third lock signal before issuing the second command, wherein the third set of processor cores is adjacent to the first set of processor cores (a timing comparison signal may indicate a difference between a phase of an input signal and a phase of a reference signal, para [0035]).

Regarding claim 20, Kim further teaches wherein the second set of processor cores is adjacent to the first set of processor cores (first and second individual processing cores formed on a unitary chip structure, each core connected to first and second adjustable power supplies, para [0011]; the MCP 712 can read and/or write data to/from memory 732, storage system 716, and/or I/O interface, para [0054]).

Claims 1-20 have industrial applicability as defined by PCT Article 33(4) because the subject matter can be made or used in industry.

SEARCH HISTORY

Application Number	PCT/US 11/24477
Search Conducted By	BOK
Search Approved By	RC/RLP

US/IPC Classifications Searched	USPC: 710/306
Date Conducted	09 May 2011 (09.05.2011)

Documentation Searched	USPC: 710/1, 33, 56, 315; 370/351, 389, 402; 702/127, 130, 132; 714/699, 746, 752, 755; 711/E12.023 (keyword limited; terms below)
Search Terms Used	processors multi core chip die cache interface communication voltage clock shift power supply synchronize timing shifter differential
Date Conducted	09 May 2011 (09.05.2011)

Electronic Database Searched	PubWEST
Files Searched	PGPB, USPT, EPAB, JPAB
Date Conducted	09 May 2011 (09.05.2011)
Search Logic:	

DATE: Monday, May 09, 2011 Purge Queries Printable Copy Create Case

Set Name Side by Side	Query	Hit Count	Set Name Result Set	Set Name Grid
	DB=PGPB,USPT,USOC,EPAB,JPAB; PLUR=NO; OP=ADJ			
L15	L12 and differential$1	1	L15	L15
L14	L12 and shifter$1	0	L14	L14

SEARCH HISTORY

L13	L12 and (synchroniz$3 near5 (clock$1 or tim$3))	2	L13	L13
L12	L8 and synchroniz$3	12	L12	L12
L11	L10 and (suppl$3 near5 volt$4)	2	L11	L11
L10	L8 and (power near5 suppl$3)	5	L10	L10
L9	L8 and (volt$4 near5 (shift$3 or adjust$3))	1	L9	L9
L8	L6 and clock$1	37	L8	L8
L7	L6 and voltage$1	9	L7	L7
L6	L5 and (communicat$4 or messag$3)	71	L6	L6
L5	L4 and interfac$3	75	L5	L5
L4	L3 and (chip$1 or die$1)	82	L4	L4
L3	L2 and (multi near4 (core$1 or processor$1))	119	L3	L3
L2	L1 and processors	501	L2	L2
L1	710/306[ccls]	1168	L1	L1

END OF SEARCH HISTORY

DATE: Monday, May 09, 2011 Purge Queries Printable Copy Create Case

Set Name Side by Side	Query	Hit Count	Set Name Result Set	Set Name Grid
	DB=PGPB,USPT,USOC,EPAB,JPAB; PLUR=NO; OP=ADJ			
L31	L29 and differential$1	8	L31	L31
L30	L29 and shifter$1	1	L30	L30
L29	L24 and (synchroniz$3 near5 (clock$1 or tim$3))	13	L29	L29
L28	L27 and synchroniz$3	1	L28	L28
L27	L26 and (suppl$3 near5 volt$4)	6	L27	L27
L26	L25 and (power near5 suppl$3)	6	L26	L26
L25	L24 and (volt$4 near5 (shift$3 or adjust$3))	7	L25	L25
L24	L23 and clock$1	35	L24	L24
L23	L22 and voltage$1	48	L23	L23
L22	L21 and (communicat$4 or messag$3)	267	L22	L22
L21	L20 and interfac$3	276	L21	L21
L20	L19 and cache$1	292	L20	L20
L19	L18 and (chip$1 or die$1)	496	L19	L19
L18	L17 and (multi near4 (core$1 or processor$1))	787	L18	L18
L17	L16 and processors	6144	L17	L17
L16	710/1[ccls] or 710/33[ccls] or 710/56[ccls] or	23991	L16	L16

SEARCH HISTORY

710/315[ccls] or 370/351[ccls] or 370/389[ccls] or
370/402[ccls] or 702/127[ccls] or 702/130[ccls] or
702/132[ccls] or 714/699[ccls] or 714/746[ccls] or
714/752[ccls] or 714/755[ccls] or 711/E12.023[ccls]

END OF SEARCH HISTORY

DATE: Monday, May 09, 2011 Purge Queries Printable Copy Create Case

Set Name Side by Side	Query	Hit Count	Set Name Result Set	Set Name Grid
	DB=PGPB,USPT,USOC,EPAB,JPAB; PLUR=NO; OP=ADJ			
L46	L45 and differential$1	0	L46	L46
L45	L44 and shifter$1	6	L45	L45
L44	L43 and (synchroniz$3 near5 (clock$1 or tim$3))	57	L44	L44
L43	L42 and synchroniz$3	95	L43	L43
L42	L41 and (suppl$3 near5 volt$4)	161	L42	L42
L41	L40 and (power near5 suppl$3)	180	L41	L41
L40	L39 and (volt$4 near5 (shift$3 or adjust$3))	229	L40	L40
L39	L38 and clock$1	1339	L39	L39
L38	L37 and voltage$1	1768	L38	L38
L37	L36 and (communicat$4 or messag$3)	9409	L37	L37
L36	L35 and interfac$3	9934	L36	L36
L35	L34 and cache$1	11077	L35	L35
L34	L33 and (chip$1 or die$1)	21552	L34	L34
L33	L32 and (multi near4 (core$1 or processor$1))	41711	L33	L33
L32	processors	409083	L32	L32

END OF SEARCH HISTORY

Electronic Database Searched	Google
Files Searched	Google
Date Conducted	09 May 2011 (09.05.2011)

SEARCH HISTORY

Search Logic:

Terms: processors multi core chip die cache interface communication voltage clock shift power supply synchronize timing shifter differential

About 5,110 results (0.36 seconds)

Electronic Database Searched	Google
Files Searched	Google Scholar
Date Conducted	09 May 2011 (09.05.2011)

Search Logic:

Terms: processors multi core chip die cache interface communication voltage clock shift power supply synchronize timing shifter differential

Results 1 - 10 of about 75. (0.23 sec)

Electronic Acknowledgement Receipt

EFS ID:	10653834
Application Number:	12713220
International Application Number:	
Confirmation Number:	4243
Title of Invention:	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR
First Named Inventor/Applicant Name:	Andrew WOLFE
Customer Number:	83446
Filer:	Gene I. Su
Filer Authorized By:	
Attorney Docket Number:	121-0019-US-REG
Receipt Date:	03-AUG-2011
Filing Date:	26-FEB-2010
Time Stamp:	03:56:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	121-0019-US-REG_NPL.pdf	609990 0dde9e651e5f5ca750f8fca68bcd98946910ded5	no	12

Warnings:

Information:

Total Files Size (in bytes):	609990

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: WOLFE, et al.	§	Group Art Unit: 2115
	§	
Serial No.: 12/713,220	§	Examiner: LEE, THOMAS C
	§	
	§	
Filed: February 26, 2010	§	Confirmation No.: 4243
	§	
For: PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR	§	
	§	
	§	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

PRELIMINARY AMENDMENT

Prior to examination, please amend the application as indicated on the following pages. Payment of US$324 pursuant to 37 CFR §1.16 for one newly added independent claim and two newly added dependent claims is also submitted with this Preliminary Amendment. **Amendments to the Claims** are reflected in the listing of claims which begins on page 2 of this paper. **Remarks** begin on page 6 of this paper.

IN THE CLAIMS:

The listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Original) A multi-core processor, comprising:

a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first clock signal;

a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second clock signal; and

an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.

2. (Original) The multi-core processor of claim 1, the interface block further comprising a first level shifter that is referenced to the second supply voltage and adapted to translate first logic levels associated with the first set of processor cores to second logic levels associated with the second set of processor cores for a first signal traveling from the first set of processor cores to the second set of processor cores.

3. (Original) The multi-core processor of claim 1, the interface block further comprising a second level shifter that is referenced to the first supply voltage and adapted to translate second logic levels associated with the second set of processor cores to first logic levels associated with the first set of processor cores for a second signal traveling from the second set of processor cores to the first set of processor cores.

4. (Original) The multi-core processor of claim 1, wherein the interface block further comprises a synchronizer configured to synchronize the first clock signal and the second clock signal for communication between one or more processor cores of the first set of processor cores and one or more processor cores of the second set of processor cores.

5. (Original) The multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a periphery of the multi-core processor.

6. (Original) The multi-core processor of claim 1, wherein the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located in a second region of the multi-core processor.

7. (Original) The multi-core processor of claim 6, wherein the first region and the second region are overlapping regions of the multi-core processor.

8. (Original) The multi-core processor of claim 6, wherein the first region and the second region are non-overlapping regions of the multi-core processor.

9. (Original) The multi-core processor of claim 6, wherein the first region corresponds to a first row of the multi-core processor, and wherein the second region corresponds to a second row of the multi-core processor.

10. (Original) The multi-core processor of claim 1, wherein the interface block is configured to idle communications between the first set of processor cores and the second set of processor cores when one or more of the first clock signal and/or the second clock signal is determined to have changed.

11. (Original) The multi-core processor of claim 10, wherein the interface block is configured to resume communication between the first set of processor cores and the second set of processor cores after one or more of the first clock signal and/or the second clock signal is determined to have stabilized.

12. (Original) The multi-core processor of claim 5, wherein the first set of processor cores is adjacent to the second set of processor cores, and the one or more control blocks are configured to select the first supply voltage and the second supply voltage to maintain a differential relationship between the first supply voltage and the second supply voltage.

13. (Original) The multi-core processor of claim 12, wherein the differential relationship is based on having an output voltage level associated with the first set of processor cores to be within an acceptable input voltage level associated with the second set of processor cores.

14. (Original) The multi-core processor of claim 1, wherein the first set of processor cores

and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a common region that is substantially central to the first set of processor cores and the second set of processor cores.

15. (Original) A method for managing communications in a multi-core processor that includes a plurality of processor cores having a first set of processor cores and a second set of processor cores, the method comprising:

idling communications with one or more of the plurality of processor cores in response to a clock frequency change request for the first set of processor cores; and

resuming communications with one or more of the plurality of processor cores after having determined that a first phase lock loop operation associated with the first set of processor cores has acquired a first lock signal and a second phase lock loop operation associated with the second set of processor cores has also acquired a second lock signal.

16. (Original) The method of claim 15, wherein resuming communications further comprising having determined that a third phase lock loop operation associated with a third set of processor cores in the multi-core processor has acquired a third lock signal, wherein the third set of processor cores is adjacent to the first set of processor cores.

17. (Original) The method of claim 16, wherein the second set of processor cores is adjacent to the first set of processor cores.

18. (Original) A computer-readable medium containing a sequence of instructions for managing communications in a multi-core processor that includes a plurality of processor cores having a first set of processor cores and a second set of processor cores, which when executed by a computing device, causes the computing device to:

issue a first command to idle communications with one or more of the plurality of processor cores in response to a clock frequency change request for the first set of processor cores;

issue a second command to resume communications with one or more of the plurality of processor cores after having determined that a first phase lock loop operation associated with the first set of processor cores has acquired a first lock signal and a second phase lock loop operation associated with the second set of processor cores has also acquired a second lock signal.

19. (Original) The computer-readable medium of claim 18, further including a sequence of instructions, which when executed by the computing device, causes the computing device to determine whether a third phase lock loop operation associated with a third set of processor cores in the multi-core processor has acquired a third lock signal before issuing the second command, wherein the third set of processor cores is adjacent to the first set of processor cores.

20. (Original) The computer-readable medium of claim 19, wherein the second set of processor cores is adjacent to the first set of processor cores.

21. (New) A multi-core processor, comprising:

a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage from a power control block and a first clock signal from a clock control block;

a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage from the power control block and a second clock signal from the clock control block; and

an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.

22. (New) The multi-core processor of claim 1, wherein the interface block is configured to idle communications between the first set of processor cores and the second set of processor cores when one or more of the first clock signal and/or the second clock signal is determined to have changed.

23. (New) The multi-core processor of claim 21, wherein the interface block is configured to resume communication between the first set of processor cores and the second set of processor cores after one or more of the first clock signal and/or the second clock signal is determined to have stabilized.

REMARKS

Claim 21 - 23 are being introduced. Claims 1-23 are pending. No new matter has been introduced.

If there are any questions, please contact the undersigned representative.

Respectfully submitted,

/Gene Su/
Gene I. Su
Attorney for Applicant(s)
Reg. No. 45,140
7F, NO. 57, SEC. 2, DUNHUA S. ROAD
TAIPEI, TAIWAN
Telephone: (886) 2.2700.7882
Facsimile: (650) 644.3217
Email: filing@suipconsulting.com

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Andrew WOLFE	§	Group Art Unit: 2115
	§	
Serial No.: 12/713,220	§	Examiner: LEE, THOMAS C
	§	
Filed: February 26, 2010	§	Confirmation No.: 4243
	§	
For: PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR	§	
	§	
	§	

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INFORMATION DISCLOSURE STATEMENT

Please consider the U.S. patents and the International Search Report and the Written Opinion listed on the enclosed PTO/SB/08a form. The cited non-patent literature document is enclosed.

This statement is being filed before the receipt of a first Office Action on the merits. Although applicant believes that no fees are due in connection with this filing, the Commissioner is hereby authorized to apply any charges or credits to Deposit Account No. 50-4588 to make this filing timely and acceptable to the Office.

Respectfully submitted,

/Gene Su/

Gene I. Su
Attorney for Applicant(s)
Reg. No. 45,140
7F, NO. 57, SEC. 2, DUN HUA S. ROAD
TAIPEI, TAIWAN
Telephone: (886) 2.2700.7882
Facsimile: (650) 644.3217

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	12713220
Filing Date	2010-02-26
First Named Inventor	Andrew WOLFE
Art Unit	2115
Examiner Name	LEE, THOMAS C
Attorney Docket Number	121-0019-US-REG

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7735037		2010-06-08	TELL	entire document, especially Abstract; para [0030], [0035], [0054], [0058], [0127], [0163]
	2	7853808		2010-12-14	KIM et al.	entire document, especially Abstract; Fig.2; para [0004], [0005], [0006], [0011], [0032], [0034], [0035], [0043], [0044], [0048], [0054]
	3	7263457		2007-08-28	WHITE et al.	entire document, especially Abstract; para [0004], [0006], [0009], [0010], [0017], [0032], [0033], [0037]

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	12713220
	Filing Date	2010-02-26
	First Named Inventor	Andrew WOLFE
	Art Unit	2115
	Examiner Name	LEE, THOMAS C
	Attorney Docket Number	121-0019-US-REG

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, May 17, 2011	☐

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	12713220
	Filing Date	2010-02-26
	First Named Inventor	Andrew WOLFE
	Art Unit	2115
	Examiner Name	LEE, THOMAS C
	Attorney Docket Number	121-0019-US-REG

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Gene Su/	Date (YYYY-MM-DD)	2011-08-02
Name/Print	Gene Su	Registration Number	45140

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	12713220
Filing Date:	26-Feb-2010
Title of Invention:	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR
First Named Inventor/Applicant Name:	Andrew WOLFE
Filer:	Gene I. Su
Attorney Docket Number:	121-0019-US-REG

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Claims in excess of 20	1202	2	52	104
Independent claims in excess of 3	1201	1	220	220
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**324**

Electronic Acknowledgement Receipt

EFS ID:	10643707
Application Number:	12713220
International Application Number:	
Confirmation Number:	4243
Title of Invention:	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR
First Named Inventor/Applicant Name:	Andrew WOLFE
Customer Number:	83446
Filer:	Gene I. Su
Filer Authorized By:	
Attorney Docket Number:	121-0019-US-REG
Receipt Date:	02-AUG-2011
Filing Date:	26-FEB-2010
Time Stamp:	06:31:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$324
RAM confirmation Number	6133
Deposit Account	504588
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Preliminary Amendment	121-0019-US-REG_Preliminary-Amendment.pdf	40321 7b224de193a9d4ee44aab34e8f22cf962e17fd83	no	6
Warnings:					
Information:					
2	Transmittal Letter	121-0019-US-REG_IDS-Letter.pdf	18945 f88cdaa657bf07718c5db0ded18a842c326c6393	no	1
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	121-0019-US-REG_IDS.pdf	612278 41578b8e622669460e8e008b17c612fd27831b9c	no	4
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	31699 5b47d605c3c6c459425217e1032df898fc1f7a85	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	703243		

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<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt

EFS ID:	10643707
Application Number:	12713220
International Application Number:	
Confirmation Number:	4243
Title of Invention:	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR
First Named Inventor/Applicant Name:	Andrew WOLFE
Customer Number:	83446
Filer:	Gene I. Su
Filer Authorized By:	
Attorney Docket Number:	121-0019-US-REG
Receipt Date:	02-AUG-2011
Filing Date:	26-FEB-2010
Time Stamp:	06:31:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$324
RAM confirmation Number	6133
Deposit Account	504588
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if app.)

1	Preliminary Amendment	121-0019-US-REG_Preliminary-Amendment.pdf	40321 7b224de193a9d4ee44aab34e8f22cf962e17fd83	no	6
Warnings:					
Information:					
2	Transmittal Letter	121-0019-US-REG_IDS-Letter.pdf	18945 f88cdaa657bf07718c5db0ded18a842c326c6393	no	1
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	121-0019-US-REG_IDS.pdf	612278 41578b8e622669460e8e008b17c612fd27831b9c	no	4
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	31699 5b47d605c3c6c459425217e1032df898fc1f7a85	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	703243		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	
12/713,220	02/26/2010	☐ To be Mailed

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 08/02/2011

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 23	Minus	** 20	= 3	X $ =		OR	X $52=	156
Independent (37 CFR 1.16(h))	* 4	Minus	***3	= 1	X $ =		OR	X $220=	220
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	376

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/POLIN ANG/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 12/18/2012

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01 FC : 1202 52.00 DA

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/713,220	02/26/2010	2189	1090	121-0019-US-REG	20	3

CONFIRMATION NO. 4243

83446
GENE I. SU
17F-1, NO. 151, SEC. 4, XINYI ROAD
TAIPEI,
TAIWAN

FILING RECEIPT

OC000000040441055

Date Mailed: 03/09/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Andrew WOLFE, Los Gatos, CA;
Marc Elliot LEVITT, San Jose, CA;

Assignment For Published Patent Application

EMPIRE TECHNOLOGY DEVELOPMENT LLC, Wilmington, DE

Power of Attorney: The patent practitioners associated with Customer Number 83446

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 03/04/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/713,220**

Projected Publication Date: 09/01/2011

Non-Publication Request: No

Early Publication Request: No

Title

PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR

Preliminary Class

711

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/713,220	02/26/2010	Andrew WOLFE	121-0019-US-REG

CONFIRMATION NO. 4243

POA ACCEPTANCE LETTER

83446
GENE I. SU
17F-1, NO. 151, SEC. 4, XINYI ROAD
TAIPEI,
TAIWAN

OC000000040440964

Date Mailed: 03/09/2010

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/26/2010.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/sibrahim/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

United States Patent Application

POWER OF ATTORNEY

I, the undersigned, as an authorized representative for EMPIRE TECHNOLOGY DEVELOPMENT LLC, of 2711 Centerville Road, Suite 400, Wilmington, New Castle County, Delaware 19808, U.S.A., hereby revoke all previous powers of attorney in the following application:

U.S. APPLICATION NUMBER	DATE OF FILING (day, month, year)	FIRST NAMED INVENTOR	TITLE
		Andrew Wolfe	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR

I hereby appoint the Practitioner ***Ren-Sheng International IP Management Ltd., 17F-1, No. 151, Sec. 4, XinYi Road, Taipei, Taiwan*** (s) associated with the following Customer Number as attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

83,446
U.S. PATENT & TRADEMARK OFFICE CUSTOMER NUMBER

Please direct all correspondence for the above-identified application to the address associated with the above-identified customer number.

For: EMPIRE TECHNOLOGY DEVELOPMENT LLC

By: ERIC BELL Title: AUTHORIZED PERSON

Signature: Date: 2/22/10

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR
First Named Inventor/Applicant Name:	ANDREW WOLFE
Filer:	Gene I. Su
Attorney Docket Number:	121-0019-US-REG

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1090**

Electronic Acknowledgement Receipt

EFS ID:	7093670
Application Number:	12713220
International Application Number:	
Confirmation Number:	4243
Title of Invention:	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR
First Named Inventor/Applicant Name:	ANDREW WOLFE
Customer Number:	83446
Filer:	Gene I. Su
Filer Authorized By:	
Attorney Docket Number:	121-0019-US-REG
Receipt Date:	26-FEB-2010
Filing Date:	
Time Stamp:	09:35:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	121-0019-US-REG_ADS.pdf	964796 99a0d44e83941bd6d3e61ebdaa33e84bd45c63ea	no	4

Warnings:

Information:

2	Oath or Declaration filed	121-0019-US-REG_Executed-DEC.pdf	213072 169e09eddf3d0e5eb5888954072e1976d3318dfa	no	4
Warnings:					
Information:					
3	Drawings-only black and white line drawings	121-0019-US-REG_Drawings.pdf	96755 b1df2a3d11a5622e08103b4531dd92a5b17b6f1b	no	5
Warnings:					
Information:					
4		121-0019-US-REG_Specification.pdf	919673 3ebd50710735a3b70cedb87f88e3fdef589d501f	yes	18

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	13
	Claims	14	17
	Abstract	18	18

Warnings:					
Information:					
5		121-0019-US-REG_373b-Statement.pdf	278285 b642b36bb1831647343185947 6ff1350d7391ba9	yes	7

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Assignee showing of ownership per 37 CFR 3.73(b).	1	6
	Power of Attorney	7	7

Warnings:					
Information:					
6	Fee Worksheet (PTO-875)	fee-info.pdf	32792 f36f198dba8ec129322b7b7a2d56cf8a6463792e	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2505373		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	121-0019-US-REG
	Application Number	
Title of Invention	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1 Remove

Applicant Authority ◉ Inventor ◯ Legal Representative under 35 U.S.C. 117 ◯ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Andrew		WOLFE	

Residence Information (Select One) ◉ US Residency ◯ Non US Residency ◯ Active US Military Service

City	Los Gatos	State/Province	CA	Country of Residence i	US

Citizenship under 37 CFR 1.41(b) i US

Mailing Address of Applicant:

Address 1	108 Leewood Ct.		
Address 2			
City	Los Gatos	State/Province	CA
Postal Code	95032	Country i	US

Applicant 2 Remove

Applicant Authority ◉ Inventor ◯ Legal Representative under 35 U.S.C. 117 ◯ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Marc	Elliot	LEVITT	

Residence Information (Select One) ◉ US Residency ◯ Non US Residency ◯ Active US Military Service

City	San Jose	State/Province	CA	Country of Residence i	US

Citizenship under 37 CFR 1.41(b) i US

Mailing Address of Applicant:

Address 1	5615 Brookhurst Ct.		
Address 2			
City	San Jose	State/Province	CA
Postal Code	95129	Country i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	121-0019-US-REG
	Application Number	
Title of Invention	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR	

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	83446		
Email Address	gsu@suipconsulting.com	Add Email	Remove Email

Application Information:

Title of the Invention	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR		
Attorney Docket Number	121-0019-US-REG	**Small Entity Status Claimed** ☐	
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	5	**Suggested Figure for Publication (if any)**	2

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	◯ US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	83446		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	121-0019-US-REG
	Application Number	
Title of Invention	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR	

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			○ Yes ◉ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1 Remove

If the Assignee is an Organization check here. ☒

Organization Name	Empire Technology Development LLC		
Mailing Address Information:			
Address 1	2711 Centerville Road, Suite 400		
Address 2			
City	Wilmington	**State/Province**	DE
Country [i]	US	Postal Code	19808
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the **Add** button. Add

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Gene Su/			Date (YYYY-MM-DD)	2010-02-25
First Name	Gene	Last Name	Su	Registration Number	45140

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

United States Patent Application

DECLARATION UNDER 37 C.F.R. § 1.63

As a below named inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR

The specification of which:

☒ is attached hereto
☐ was filed on _____ as United States Patent Application Serial No. or PCT International Application No. _____ and was amended on _____ (*if applicable*).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose all information which is material to patentability as defined in 37 C.F.R. § 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

PRIORITY CLAIMS

I hereby claim foreign priority benefits under Title 35 U.S.C. § 119(a)-(d) or (f) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application(s) which designated at least one country other than the United States of America listed below and have also identified, by checking the box, any foreign application(s) for patent or inventor's certificate or any PCT international application(s) having a filing date before that of the application(s) on which priority is claimed.

☒ no such applications have been filed.
☐ such applications have been filed as follows:

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER § 119 or § 365
			☐ YES ☐ NO
			☐ YES ☐ NO
			☐ YES ☐ NO
			☐ YES ☐ NO

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

☒ no such applications have been filed.
☐ such applications have been filed as follows:

U.S. APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

☒ no such applications have been filed.
☐ such applications have been filed as follows:

U.S. PROVISIONAL APPLICATION NUMBER	DATE OF FILING (day, month, year)

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Given Name:	Andrew Wolfe		
Inventor's Signature:		Date	2/10/10
Residence:	Los Gatos, CA, USA	Citizenship:	USA
Mailing Address:	108 Leewood Ct.		
	Los Gatos, CA 95032, US		

Given Name:	Marc Elliot Levitt		
Inventor's Signature:		Date	2-11-10
Residence:	San Jose, CA, USA	Citizenship:	USA
Mailing Address:	5616 Brookhurst Ct.,		
	San Jose, CA 95129, USA		

37 C.F.R. § 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

(e) In any continuation-in-part application, the duty under this section includes the duty to disclose to the Office all information known to the person to be material to patentability, as defined in paragraph (b) of this section, which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

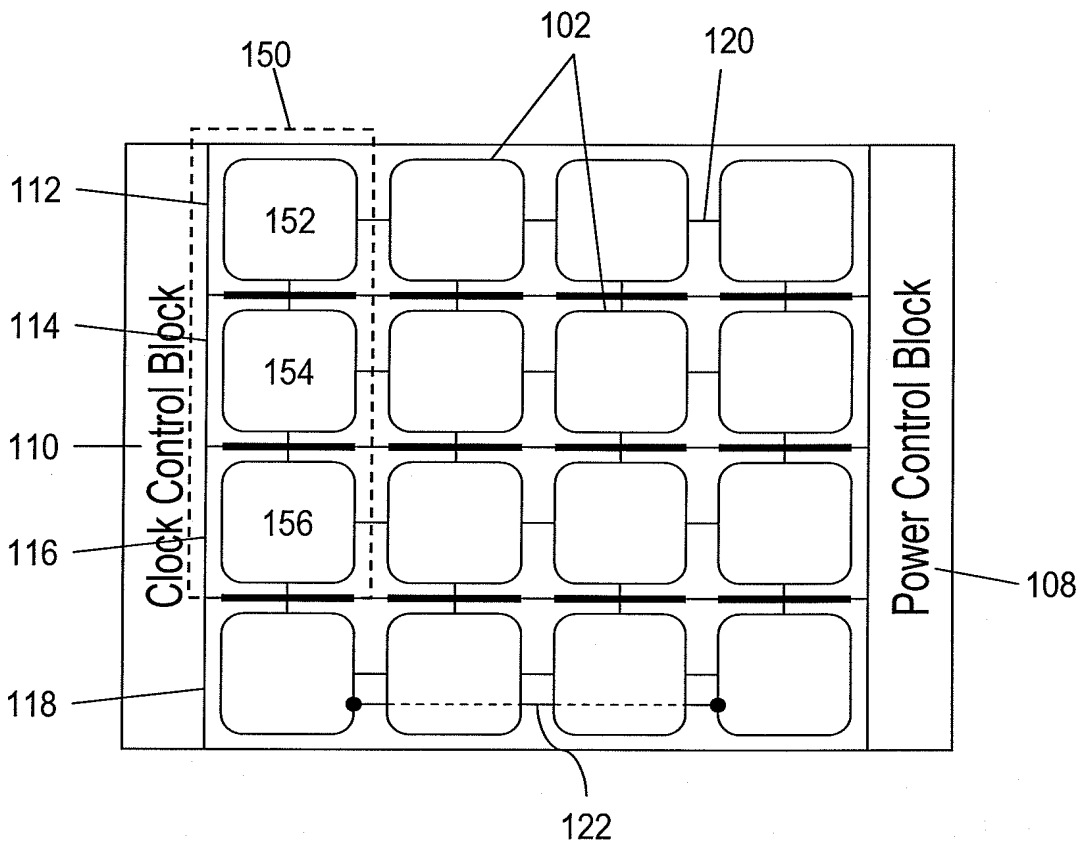
100
150
102
120
112
114
110
116
118
152
154
156
Clock Control Block
Power Control Block
108
122

FIG. 1

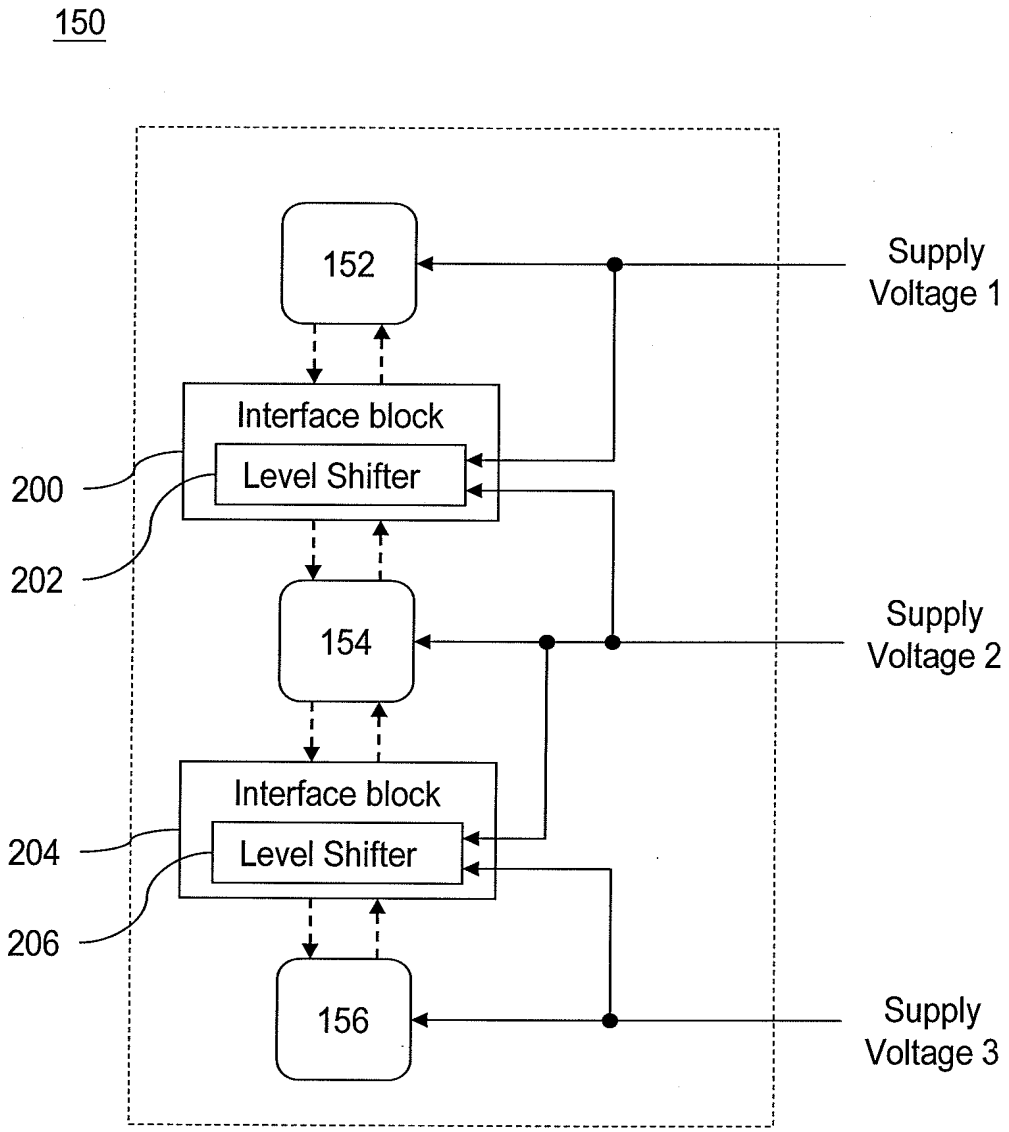
150
152
Supply Voltage 1
Interface block
Level Shifter
200
202
154
Supply Voltage 2
Interface block
Level Shifter
204
206
156
Supply Voltage 3

FIG. 2

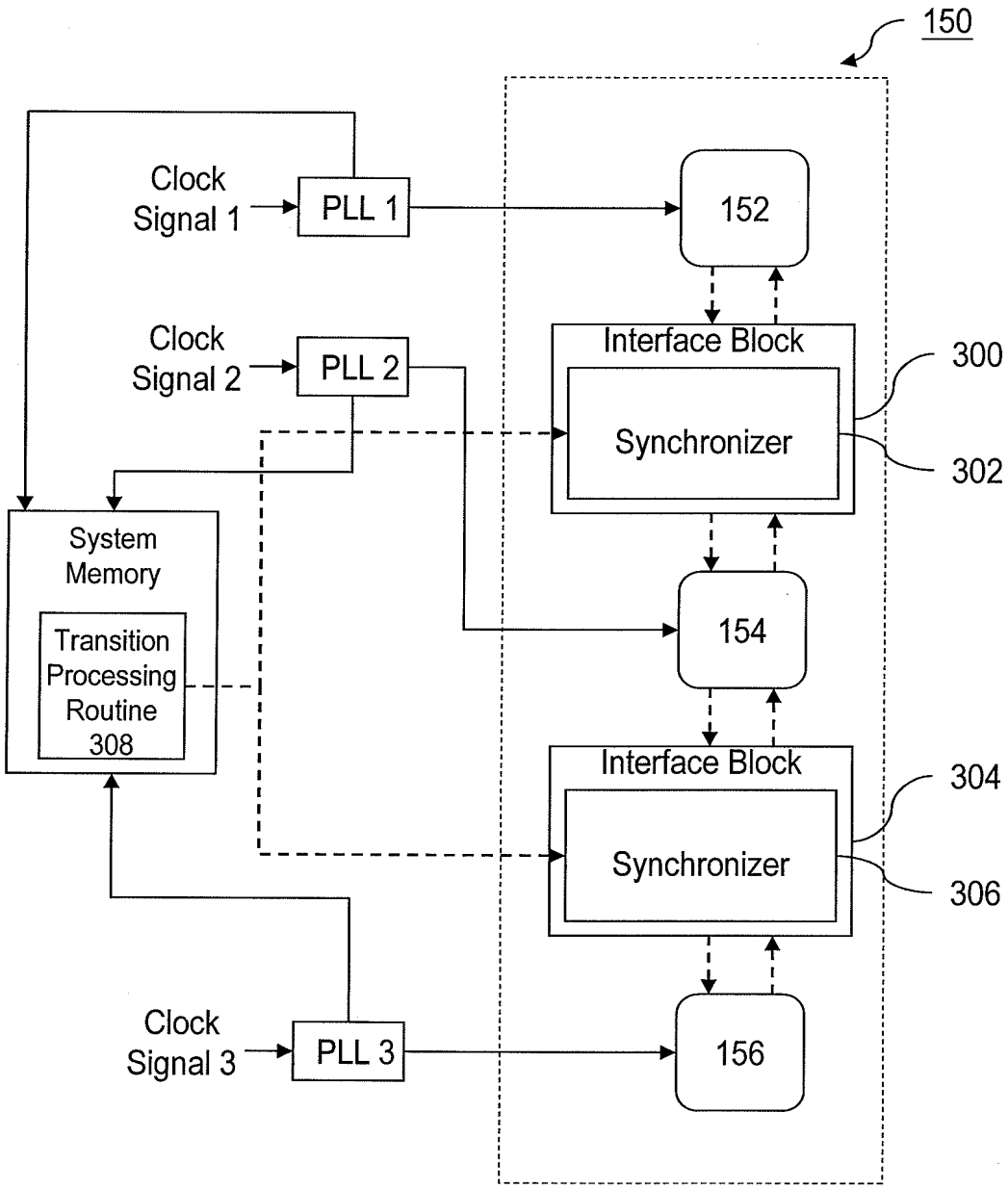
150
Clock Signal 1
PLL 1
152
Clock Signal 2
PLL 2
Interface Block
Synchronizer
300
302
System Memory
Transition Processing Routine 308
154
Interface Block
Synchronizer
304
306
Clock Signal 3
PLL 3
156

FIG. 3

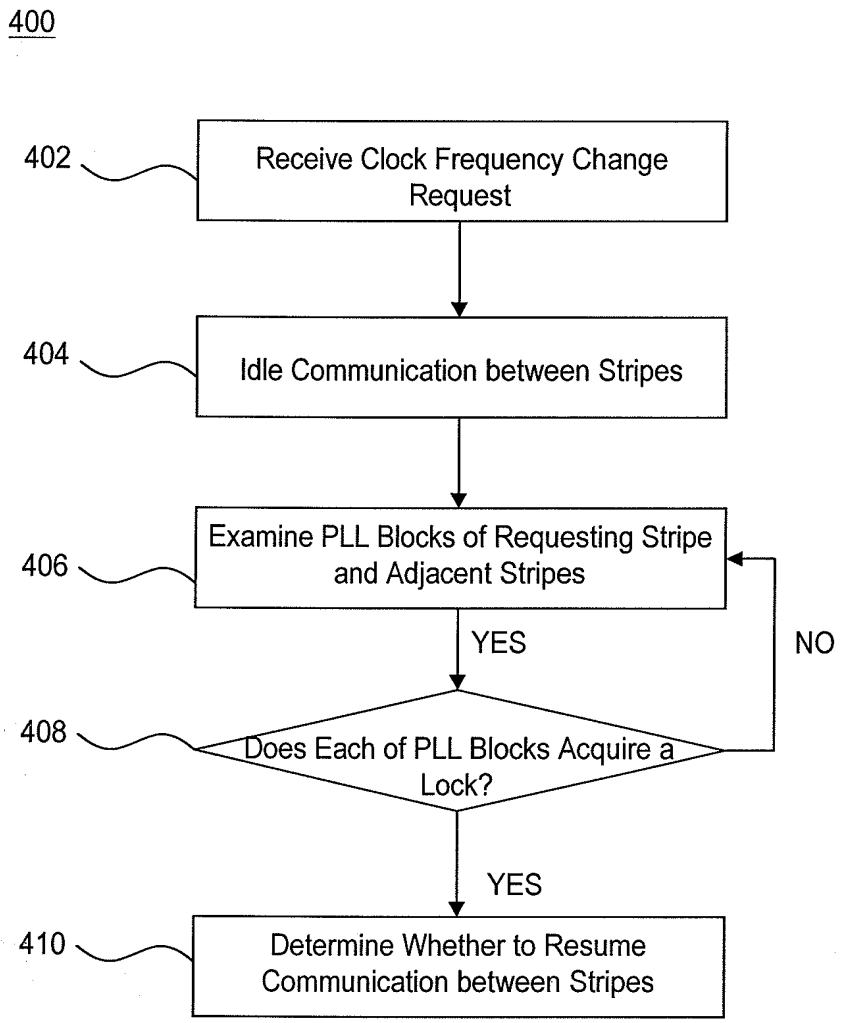
400
402
Receive Clock Frequency Change Request
404
Idle Communication between Stripes
406
Examine PLL Blocks of Requesting Stripe and Adjacent Stripes
YES
NO
408
Does Each of PLL Blocks Acquire a Lock?
YES
410
Determine Whether to Resume Communication between Stripes

FIG. 4

500 A computer program product

502 at least one of

one or more instructions for receiving a request of changing the clock frequency;

one or more instructions for issuing a command to idle communication with the first region;

one or more instructions for examining whether a first phase lock loop operation associated with the first region has acquired a first lock signal in response to the request; and/or

one or more instructions for examining whether a second phase lock loop operation associated with a second region of processor cores in the multi-core processor has acquired a second lock signal in response to the request, wherein the second region is adjacent to the first region

504 a signal bearing medium

506 a communication medium

508 a computer readable medium

510 a recordable medium

FIG. 5

PATENT APPLICATION FOR:

PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR

INVENTORS:

ANDREW WOLFE

MARC ELLIOT LEVITT

ATTORNEY DOCKET NUMBER: 121-0019-US-REG

PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR

BACKGROUND OF THE DISCLOSURE

[0001] A multi-core processor includes two or more independent processor cores arranged in an array. Each processor core in a conventional multi-core processor generally shares the same supply voltage and clock signal to simplify the interfaces between the processor cores. For power consumption management, dynamic supply voltage and clock speed control may be utilized, so that a multi-core processor may operate at high power and high clock frequency when needed and at low power when the computing requirements are reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] The foregoing and other features of the present disclosure will become more fully apparent from the following description and appended claims, taken in conjunction with the accompanying drawings. These drawings depict only several embodiments in accordance with the disclosure and are, therefore, not to be considered limiting of its scope. The disclosure will be described with additional specificity and detail through use of the accompanying drawings.

[0003] FIG. 1 illustrates an example configuration of a multi-core processor;

FIG. 2 is a block diagram illustrating an example set of processor cores with example interface blocks having level shifters;

FIG. 3 is another block diagram illustrating an example set of processor cores with example interface blocks having synchronizers;

FIG. 4 is a flow chart illustrating an example transition processing routine for managing a clock frequency change; and

FIG. 5 is a block diagram illustrating an example computer program product for handling processor core communication in a multi-core processor; all arranged in accordance with at least some embodiments of the present disclosure.

DETAILED DESCRIPTION

[0004] In the following detailed description, reference is made to the accompanying drawings, which form a part hereof. In the drawings, similar symbols typically identify similar components, unless context dictates otherwise. The illustrative embodiments described in the detailed description, drawings, and claims are not meant to be limiting. Other embodiments may be utilized, and other changes may be made, without departing from the spirit or scope of the subject matter presented here. It will be readily understood that the aspects of the present disclosure, as generally described herein, and illustrated in the Figures, can be arranged, substituted, combined, and designed in a wide variety of different configurations, all of which are explicitly contemplated and make part of this disclosure.

[0005] This disclosure is drawn, *inter alia*, to devices, methods, systems, and computer programs related to power management for a multi-core processor.

[0006] A multi-core processor may include multiple processor cores arranged in an array. A power profile associated with an individual processor core may be controlled through signals that may be received from control blocks that are located in the periphery of the multi-core processor. The power profile may include, without limitation, one or more power-supply voltages of the core processor, clock rates of the core processor, clock multipliers of the core processor, power throttling of the core processor, and/or sleep state cycles of the core processor.

[0007] FIG. 1 illustrates an example configuration of a multi-core processor 100 that is arranged in accordance with at least some embodiments of the present disclosure. The multi-core processor 100 may include multiple processor cores 102 arranged in rows and columns in a 2-dimensional array in an integrated circuit. A processor core may be coupled with adjacent processor cores through an interface circuit 120. In some implementations, the processor cores 102 may be horizontally coupled to one another, vertically coupled to one another, and/or diagonally coupled to one another by the interface circuit 120. In some example implementations, the processor core 102 located on one edge of the multi-core processor 100 may also be coupled to the processor core 102 on the opposite edge with a wrap-around

connection 122, which may be employed to ensure a continuous connection among the processor cores in the same row and/or column.

[0008] The multi-core processor 100 may be further divided into regions. In some implementations, the regions of multi-core processor 100 may correspond to rows of the two-dimensional array, and the regions may or may not be overlapping. Each row of processors may also be referred to as a "stripe." For example, the multi-core processor 100 may be divided into stripes 112, 114, 116, and 118. Each stripe may be associated with an independent power profile. For example, the stripe 112 may be powered by a supply voltage received from a power control block 108 and/or may be associated with an independent clock domain defined by a clock signal received from a clock control block 110. In some implementations, the power control block 108 and the clock control block 110 may be arranged at two different sides of the multi-core processor 100 as shown in FIG. 1. In some other implementations, the power control block 108 and the clock control block 110 may be arranged at the same side of the multi-core processor 100. In yet some other implementations, the power control block 108 and the clock control block 110 may be arranged in a common area located near the center of the multi-core processor 100.

[0009] The power profile associated with a stripe may be determined based on the computational requirements of the tasks assigned to the processor cores in the stripe. In some implementations, sensors placed at the input of each processor core may be configured to measure the supply voltage and the local temperature for the processor core. The measured supply voltage and local temperature may be maintained in the power control block 108. One or more performance counters associated with each processor core may also provide feedback to the power control block 108. Based on the measured operational information (e.g., supply voltage and local temperature) and the performance data, the power control block 108 may then be configured to select a supply voltage for each strip. For example, the tasks with the highest computational requirements may be scheduled into the topmost stripe, such as the stripe 112. The stripe 112 may be configured to operate at a high supply voltage. The tasks with lesser computational requirements may be

scheduled into the stripe 114 and so forth. The stripes 114, 116, and 118 thus may be configured to operate lower supply voltages.

[0010] In some implementations, supply voltages to the stripes may be selected such that the selected supply voltages for adjacent stripes may differ by a limited amount. This limited amount may be based on a relationship between the output voltage level associated with one stripe and the input voltage level associated with an adjacent stripe. For example, suppose the stripe with the higher supply voltage (e.g., the stripe 112) may be associated with an output voltage level (e.g., V_o). V_o needs to fall reliably within an acceptable input voltage level range (e.g., V_{i+} to V_{i-}) for an adjacent stripe (e.g., the stripe 114). In other words, the power control block 108 may be configured to select the supply voltages to the stripe 112 and the stripe 114, so that the aforementioned relationship between V_o and range V_{i+} to V_{i-} may be maintained.

[0011] To maintain the limited differential relationship discussed above, adjusting the supply voltage to one stripe may involve adjusting the supply voltages to the other stripes. To illustrate, suppose the power control block 108 may adjust the supply voltage to the stripe 112. To maintain the limited differential relationship, the power control block 108 may adjust the supply voltages to the stripes 118, 116, and 114 before adjusting the supply voltage to the stripe 112.

[0012] Although dynamically adjusting the power profile for a stripe in response to changes in computational requirements may reduce power consumption for a multi-core processor, such adjustments may take some period of time to stabilize. To further illustrate the interfaces that facilitate communication between two processor cores in the multi-core processor 100, a subset 150 of processor cores 152, 154, and 156 of FIG. 1 may be selected. The processor core 152 belongs to the stripe 112; the processor core 154 belongs to the stripe 114; and the processor core 156 belongs to the stripe 116.

[0013] FIG. 2 is a block diagram illustrating an example subset 150 of processor cores with example interface blocks having level shifters, arranged in accordance

with at least some embodiments of the present disclosure. The processor core 152 may be powered by a supply voltage 1 and coupled to an interface block 200 having a level shifter 202; the processor core 154 may be powered by a supply voltage 2 and coupled to the same interface block 200; and the processor core 156 may be powered by a supply voltage 3 and coupled to an interface block 204 having a level shifter 206. In some implementations, the inputs of the level shifter 202 may be the supply voltage 1 and the supply voltage 2, and the inputs of the level shifter 206 may be the supply voltage 2 and the supply voltage 3. The supply voltage 1, the supply voltage 2, and the supply voltage 3 may come from a power control block, such as the power control block 108 of FIG 1.

[0014] When the processor core 152 of the stripe 112 sends a signal to the processor core 154 of the stripe 114, in some implementations, the output voltage of the level shifter 202 may be tied to the supply voltage 2, and the input voltage of the level shifter 202 may be tied to the supply voltage 1. The level shifters are arranged to translate the signal levels such that each of the processor cores operates correctly (e.g., the processor cores properly interpret the voltages as valid logic levels even though processor cores are powered by different supply voltages). Here, the level shifter 202 may be adapted to translate first logic levels associated with the stripe 112 to second logic levels associated with the stripe 114, and the level shifter 202 may be referenced to the supply voltage 2. On the other hand, when the processor core 154 of the stripe 114 sends a signal to the processor core 152 of the stripe 112, the output voltage of the level shifter 202 may be tied to the supply voltage 1, and the input voltage of the level shifter 202 may be tied to the supply voltage 2. In other words, the level shifter 202 may be adapted to translate second logic levels associated with the stripe 114 to first logic levels associated with stripe 112, and the level shifter 202 may be referenced to the supply voltage 1. The relationships among the supply voltage 1, supply voltage 2, and the level shifter 202 described above similarly apply to the relationships among the supply voltage 2, supply voltage 3, and the level shifter 206.

[0015] FIG. 3 is another block diagram illustrating an example subset 150 of processor cores with example interface blocks having synchronizers, arranged in

accordance with at least some embodiments of the present disclosure. The processor core 152 may be driven by a clock signal 1 and coupled to an interface block 300 having a synchronizer 302; the processor core 154 may be driven by a clock signal 2 and coupled to the same interface block 300; and the processor core 156 may be driven by a clock signal 3 and coupled to an interface block 304 having a synchronizer 306. In some implementations, the clock signal 1, the clock signal 2, the clock signal 3, and the respective phase lock loops (PLLs) may be a part of a clock control block, such as the clock control block 110. The processing results of the PLL blocks may be fed back to a transition processing routine 308. Commands generated by the transition processing routine 308 may also be sent to the synchronizer 302 and/or the synchronizer 306.

[0016] As discussed above, when the power profile for a stripe changes, such as a change in clock frequency, the clock signal for the stripe may become unstable. To handle such a situation, FIG. 4 is a flow chart illustrating an example transition processing routine 400 for managing a clock frequency change, arranged in accordance with at least some embodiments of the present disclosure. For ease of description, the transition processing routine 400 is described in terms of a set of processor cores and interface blocks substantially similar to those described previously with respect to FIG. 3. The transition processing routine 400 may include one or more functions, operations, or actions as depicted by operations 402, 404, 406, 408, and/or 410. In some implementations, the various features of the illustrated operations for the transition processing routine 400 may be combined into fewer operations, divided into additional operations, or eliminated based on the desired result.

[0017] Processing for the transition processing routine 300 may begin at operation 302, "receive clock frequency change request." Operation 302 may be followed by operation 304, "idle communication between stripes." Operation 304 may be followed by operation 306, "examine PLL blocks of requesting stripe and adjacent stripe(s)." Operation 306 may be followed by operation 308, "does each of PLL blocks acquire a lock?" Operation 308 may be followed by either operation 306 when the decision logic tested at block 308 fails to be satisfied (NO), or operation

310, "determine whether to resume communication between stripes", when the decision logic tested at block 308 is satisfied (YES). Processing for the routine may terminate after block 310.

[0018] For illustration, suppose the processor core 154 of the stripe 114 in FIG. 3 is asked to change its clock frequency based on the tasks that are being assigned to the stripe 114 for processing. After having received the request in operation 402, the transition processing routine 400 may issue commands to the synchronizer 302 and the synchronizer 306 in operation 404 to idle the communications between the processor core 154 and the processor core 152 and between the processor core 154 and the processor core 156. Following operation 404, the outputs of the PLL blocks for the stripes that are adjacent to the stripe 114 may be examined in operation 406. Depending on whether the PLL blocks have acquired locks as determined in operation 408, the transition processing routine 400 may decide in operation 410 whether the transition sequence has occurred properly and the communication between the stripes may resume.

[0019] In some implementations, after each of the PLL block 1, PLL block 2, and PLL block 3 is determined to have acquired a lock of its respective clock signal in operation 408, a stable clock signal may be sent to the processor core 154 and also the synchronizer 302 and the synchronizer 306. Then, the synchronizer 302 may be configured to synchronize the clock signal 1 and the clock signal 2 for the communication between the processor core 152 and the processor core 154. Similarly, the synchronizer 306 may be configured to synchronize the clock signal 2 and the clock signal 3 for the communication between the processor core 154 and the processor core 156.

[0020] FIG. 5 is a block diagram illustrating a computer program product 500 for handling processor core communication in a multi-core processor in accordance with at least some embodiments of the present disclosure. Computer program product 500 may include one or more sets of executable instructions 502 for executing the transition processing routine described above and illustrated in FIG. 4. Computer program product 500 may be transmitted in a signal bearing medium 504

or another similar communication medium 506. Computer program product 500 may also be recorded in a computer readable medium 508 or another similar recordable medium 510.

[0021] There is little distinction left between hardware and software implementations of aspects of systems; the use of hardware or software is generally (but not always, in that in certain contexts the choice between hardware and software can become significant) a design choice representing cost vs. efficiency tradeoffs. There are various vehicles by which processes and/or systems and/or other technologies described herein can be effected (e.g., hardware, software, and/or firmware), and that the preferred vehicle will vary with the context in which the processes and/or systems and/or other technologies are deployed. For example, if an implementer determines that speed and accuracy are paramount, the implementer may opt for a mainly hardware and/or firmware vehicle; if flexibility is paramount, the implementer may opt for a mainly software implementation; or, yet again alternatively, the implementer may opt for some combination of hardware, software, and/or firmware.

[0022] The foregoing detailed description has set forth various embodiments of the devices and/or processes via the use of block diagrams, flowcharts, and/or examples. Insofar as such block diagrams, flowcharts, and/or examples contain one or more functions and/or operations, it will be understood by those within the art that each function and/or operation within such block diagrams, flowcharts, or examples can be implemented, individually and/or collectively, by a wide range of hardware, software, firmware, or virtually any combination thereof. In one embodiment, several portions of the subject matter described herein may be implemented via Application Specific Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs), digital signal processors (DSPs), or other integrated formats. However, those skilled in the art will recognize that some aspects of the embodiments disclosed herein, in whole or in part, can be equivalently implemented in integrated circuits, as one or more computer programs running on one or more computers (e.g., as one or more programs running on one or more computer systems), as one or more programs running on one or more processors (e.g., as one or more programs running on one or more microprocessors), as firmware, or as virtually any combination thereof, and

that designing the circuitry and/or writing the code for the software and or firmware would be well within the skill of one of skill in the art in light of this disclosure. In addition, those skilled in the art will appreciate that the mechanisms of the subject matter described herein are capable of being distributed as a program product in a variety of forms, and that an illustrative embodiment of the subject matter described herein applies regardless of the particular type of signal bearing medium used to actually carry out the distribution. Examples of a signal bearing medium include, but are not limited to, the following: a recordable type medium such as a floppy disk, a hard disk drive, a Compact Disc (CD), a Digital Video Disk (DVD), a digital tape, a computer memory, etc.; and a transmission type medium such as a digital and/or an analog communication medium (e.g., a fiber optic cable, a waveguide, a wired communications link and/or channel, a wireless communication link and/or channel, etc.).

[0023] Those skilled in the art will recognize that it is common within the art to describe devices and/or processes in the fashion set forth herein, and thereafter use engineering practices to integrate such described devices and/or processes into data processing systems. That is, at least a portion of the devices and/or processes described herein can be integrated into a data processing system via a reasonable amount of experimentation. Those having skill in the art will recognize that a typical data processing system generally includes one or more of a system unit housing, a video display device, a memory such as volatile and non-volatile memory, processors such as microprocessors and digital signal processors, computational entities such as operating systems, drivers, graphical user interfaces, and applications programs, one or more interaction devices, such as a touch pad or screen, and/or control systems including feedback loops and control motors (e.g., feedback for sensing position and/or velocity; control motors for moving and/or adjusting components and/or quantities). A typical data processing system may be implemented utilizing any suitable commercially available components, such as those typically found in data computing/communication and/or network computing/communication systems.

[0024] The herein described subject matter sometimes illustrates different components contained within, or connected with, different other components. It is to be understood that such depicted architectures are merely exemplary, and that in fact many other architectures can be implemented which achieve the same functionality. In a conceptual sense, any arrangement of components to achieve the same functionality is effectively "associated" such that the desired functionality is achieved. Hence, any two components herein combined to achieve a particular functionality can be seen as "associated with" each other such that the desired functionality is achieved, irrespective of architectures or intermedial components. Likewise, any two components so associated can also be viewed as being "operably connected", or "operably coupled", to each other to achieve the desired functionality, and any two components capable of being so associated can also be viewed as being "operably couplable", to each other to achieve the desired functionality. Specific examples of operably couplable include but are not limited to physically mateable and/or physically interacting components and/or wirelessly interactable and/or wirelessly interacting components and/or logically interacting and/or logically interactable components.

[0025] With respect to the use of substantially any plural and/or singular terms herein, those having skill in the art can translate from the plural to the singular and/or from the singular to the plural as is appropriate to the context and/or application. The various singular/plural permutations may be expressly set forth herein for sake of clarity.

[0026] It will be understood by those within the art that, in general, terms used herein, and especially in the appended claims (e.g., bodies of the appended claims) are generally intended as "open" terms (e.g., the term "including" should be interpreted as "including but not limited to," the term "having" should be interpreted as "having at least," the term "includes" should be interpreted as "includes but is not limited to," etc.). It will be further understood by those within the art that if a specific number of an introduced claim recitation is intended, such an intent will be explicitly recited in the claim, and in the absence of such recitation no such intent is present. For example, as an aid to understanding, the following appended claims may contain

usage of the introductory phrases "at least one" and "one or more" to introduce claim recitations. However, the use of such phrases should not be construed to imply that the introduction of a claim recitation by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim recitation to inventions containing only one such recitation, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an" (e.g., "a" and/or "an" should typically be interpreted to mean "at least one" or "one or more"); the same holds true for the use of definite articles used to introduce claim recitations. In addition, even if a specific number of an introduced claim recitation *is* explicitly recited, those skilled in the art will recognize that such recitation should typically be interpreted to mean *at least* the recited number (e.g., the bare recitation of "two recitations," without other modifiers, typically means *at least* two recitations, or *two or more* recitations). Furthermore, in those instances where a convention analogous to "at least one of A, B, and C, etc." is used, in general such a construction is intended in the sense one having skill in the art would understand the convention (e.g., "a system having at least one of A, B, and C" would include but not be limited to systems that have A alone, B alone, C alone, A and B together, A and C together, B and C together, and/or A, B, and C together, etc.). In those instances where a convention analogous to "at least one of A, B, or C, etc." is used, in general such a construction is intended in the sense one having skill in the art would understand the convention (e.g., "a system having at least one of A, B, or C" would include but not be limited to systems that have A alone, B alone, C alone, A and B together, A and C together, B and C together, and/or A, B, and C together, etc.). It will be further understood by those within the art that virtually any disjunctive word and/or phrase presenting two or more alternative terms, whether in the description, claims, or drawings, should be understood to contemplate the possibilities of including one of the terms, either of the terms, or both terms. For example, the phrase "A or B" will be understood to include the possibilities of "A" or "B" or "A and B."

[0027] While various aspects and embodiments have been disclosed herein, other aspects and embodiments will be apparent to those skilled in the art. The various

aspects and embodiments disclosed herein are for purposes of illustration and are not intended to be limiting, with the true scope and spirit being indicated by the following claims.

We Claim:

1. A multi-core processor, comprising:

a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first clock signal;

a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second clock signal; and

an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.

2. The multi-core processor of claim 1, the interface block further comprising a first level shifter that is referenced to the second supply voltage and adapted to translate first logic levels associated with the first set of processor cores to second logic levels associated with the second set of processor cores for a first signal traveling from the first set of processor cores to the second set of processor cores.

3. The multi-core processor of claim 1, the interface block further comprising a second level shifter that is referenced to the first supply voltage and adapted to translate second logic levels associated with the second set of processor cores to first logic levels associated with the first set of processor cores for a second signal traveling from the second set of processor cores to the first set of processor cores.

4. The multi-core processor of claim 1, wherein the interface block further comprises a synchronizer configured to synchronize the first clock signal and the second clock signal for communication between one or more processor cores of the first set of processor cores and one or more processor cores of the second set of processor cores.

5. The multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a periphery of the multi-core processor.

6. The multi-core processor of claim 1, wherein the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located in a second region of the multi-core processor.

7. The multi-core processor of claim 6, wherein the first region and the second region are overlapping regions of the multi-core processor.

8. The multi-core processor of claim 6, wherein the first region and the second region are non-overlapping regions of the multi-core processor.

9. The multi-core processor of claim 6, wherein the first region corresponds to a first row of the multi-core processor, and wherein the second region corresponds to a second row of the multi-core processor.

10. The multi-core processor of claim 1, wherein the interface block is configured to idle communications between the first set of processor cores and the second set of processor cores when one or more of the first clock signal and/or the second clock signal is determined to have changed.

11. The multi-core processor of claim 10, wherein the interface block is configured to resume communication between the first set of processor cores and the second set of processor cores after one or more of the first clock signal and/or the second clock signal is determined to have stabilized.

12. The multi-core processor of claim 5, wherein the first set of processor cores is adjacent to the second set of processor cores, and the one or more control blocks

are configured to select the first supply voltage and the second supply voltage to maintain a differential relationship between the first supply voltage and the second supply voltage.

13. The multi-core processor of claim 12, wherein the differential relationship is based on having an output voltage level associated with the first set of processor cores to be within an acceptable input voltage level associated with the second set of processor cores.

14. The multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a common region that is substantially central to the first set of processor cores and the second set of processor cores.

15. A method for managing communications in a multi-core processor that includes a plurality of processor cores having a first set of processor cores and a second set of processor cores, the method comprising:

idling communications with one or more of the plurality of processor cores in response to a clock frequency change request for the first set of processor cores; and

resuming communications with one or more of the plurality of processor cores after having determined that a first phase lock loop operation associated with the first set of processor cores has acquired a first lock signal and a second phase lock loop operation associated with the second set of processor cores has also acquired a second lock signal.

16. The method of claim 15, wherein resuming communications further comprising having determined that a third phase lock loop operation associated with a third set of processor cores in the multi-core processor has acquired a third lock signal, wherein the third set of processor cores is adjacent to the first set of processor cores.

17. The method of claim 16, wherein the second set of processor cores is adjacent to the first set of processor cores.

18. A computer-readable medium containing a sequence of instructions for managing communications in a multi-core processor that includes a plurality of processor cores having a first set of processor cores and a second set of processor cores, which when executed by a computing device, causes the computing device to:

issue a first command to idle communications with one or more of the plurality of processor cores in response to a clock frequency change request for the first set of processor cores;

issue a second command to resume communications with one or more of the plurality of processor cores after having determined that a first phase lock loop operation associated with the first set of processor cores has acquired a first lock signal and a second phase lock loop operation associated with the second set of processor cores has also acquired a second lock signal.

19. The computer-readable medium of claim 18, further including a sequence of instructions, which when executed by the computing device, causes the computing device to determine whether a third phase lock loop operation associated with a third set of processor cores in the multi-core processor has acquired a third lock signal before issuing the second command, wherein the third set of processor cores is adjacent to the first set of processor cores.

20. The computer-readable medium of claim 19, wherein the second set of processor cores is adjacent to the first set of processor cores.

ABSTRACT OF THE DISCLOSURE

Embodiments of the disclosure generally set forth techniques for handling communication between processor cores. Some example multi-core processors include a first set of processor cores in a first region of the multi-core processor configured to dynamically receive a first supply voltage and a first clock signal, a second set of processor cores in a second region of the multi-core processor configured to dynamically receive a second supply voltage and a second clock signal, and an interface block coupled to the first set of processor cores and the second set of processor cores, wherein the interface block is configured to facilitate communications between the first set of processor cores and the second set of processor cores.

Attorney Docket No. 121-0019-US-REG

United States Patent Application

STATEMENT UNDER 37 CFR § 3.73(b)

I, the undersigned, as an authorized representative for EMPIRE TECHNOLOGY DEVELOPMENT LLC, of 2711 Centerville Road, Suite 400, Wilmington, New Castle County, Delaware 19808, U.S.A., state that EMPIRE TECHNOLOGY DEVELOPMENT LLC is the assignee of the entire right, title, and interest in the following application:

U.S. APPLICATION NUMBER	DATE OF FILING (day, month, year)	FIRST NAMED INVENTOR	TITLE
		Andrew Wolfe	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR

Copies of the assignment agreement(s) establishing the chain of title is/are:

☒ attached hereto.

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For: EMPIRE TECHNOLOGY DEVELOPMENT LLC

By: ERIC BELL Title: AUTHORIZED PERSON

Signature: Date: 2/22/10

Page 1 of 1

Attorney Docket. No.
121-0019-US-REG

ASSIGNMENT OF PATENT RIGHTS

For valuable consideration, the receipt and sufficiency of which is hereby acknowledged, Andrew Wolfe of 108 Leewood Ct., Los Gatos, CA 95032, US, and Marc Elliot Levitt of 5615 Brookhurst Ct., San Jose, CA 95129, US, "**Assignors**" effective as of December 10, 2009, hereby sells, assigns, transfers, and conveys unto

(A) Empire Technology Development LLC, a Delaware limited liability company, with an address at 2711 Centerville Road, Suite 400, Wilmington, DE 19808 ("**U.S. Assignee**"), all rights, title, and interests that exist today and may exist in the future in and to any and all of the following items (1) through (8) below:

1. the inventions disclosed in the solution report/invention disclosure titled "***Controlled voltage gradients in an asynchronoous processor array***" and all inventions claimed and/or described in the Application (collectively, the "**Invention**");

2. the patent applications listed in the table below (the "**Application**");

Patent Application No.	Country	Filing Date	Title
	US		PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR

3. all rights with respect to the Invention, including all United States patents or other governmental grants or issuances that may be granted with respect to the Invention or from any direct or indirect divisionals, continuations, continuations-in-part, or other patent applications claiming priority rights from the Application ("**Potential Patents**");

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8. any and all other rights and interests arising out of, in connection with, or in relation to the Application, the Invention, Potential Patents, and the Foreign Rights.

As used in this Assignment, "Assignee" means, collectively, the U.S. Assignee and the Non-U.S. Assignee. Assignor will not sign any document or do any act conflicting with this Assignment, and, without further compensation, will sign all documents and do such additional acts as Assignee, its successors, legal representatives, and assigns deem necessary or desirable to perfect enjoyment of the Rights, conduct proceedings regarding the Rights (including any litigation or interference proceedings), or perfect or defend title to the Rights. Assignor requests the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models, or other governmental grants or issuances that may be granted upon any of the Rights in the name of the Assignee, as the assignee to the entire interest therein.

Assignor hereby authorizes and requests legal representative *Ren-Sheng International IP Management Ltd., 17F-1, No. 151, Sec. 4, XinYi Road, Taipe, Taiwan,* to insert on this Assignment the filing date and Patent Application Numbers in the table above when known.

The terms and conditions of this Assignment will inure to the benefit of Assignee, its successors, legal representatives, and assigns and will be binding upon Assignor, their successors, legal representatives and assigns.

[Signature Page(s) to Follow]

By: _____

Andrew Wolfe
108 Leewood Ct.,
Los Gatos, CA 95032 U.S.

NOTARIZATION

STATE OF CALIFORNIA)
) ss.
COUNTY OF SANTA CLARA)

On FEB. 11, 2010, before me, JOANNE VENEGAS, Notary Public, personally appeared Andrew Wolfe, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature(s) on the instrument the person(s) or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of CALIFORNIA that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

Signature Joanne Venegas

JOANNE VENEGAS
Commission # 1789670
Notary Public - California
Santa Clara County
My Comm. Expires Feb 21, 2012

By: _____

Marc Elliot Levitt
5615 Brookhurst Ct.,
San Jose, CA 95129 U.S.

NOTARIZATION

STATE OF _____)
) ss.
COUNTY OF _____)

See attached.

On _____, 20___, before me, _____, Notary Public, personally appeared Marc Elliot Levitt, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature(s) on the instrument the person(s) or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of _____ that the foregoing paragraph is true and correct.

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CALIFORNIA ALL-PURPOSE ACKNOWLEDGMENT

State of California
County of Santa Clara }

On February 11, 2010 (Date) before me, Mary Ann Walthers, Notary Public (Here Insert Name and Title of the Officer),
personally appeared Marc Elliott Levitt (Name(s) of Signer(s))

who proved to me on the basis of satisfactory evidence to be the person~~(s)~~ whose name~~(s)~~ is/~~are~~ subscribed to the within instrument and acknowledged to me that he/~~she/they~~ executed the same in his/~~her/their~~ authorized capacity~~(ies)~~, and that by his/~~her/their~~ signature~~(s)~~ on the instrument the person~~(s)~~, or the entity upon behalf of which the person~~(s)~~ acted, executed the instrument.

MARY ANN WALTHERS
Commission # 1773587
Notary Public - California
Santa Clara County
My Comm. Expires Oct 16, 2011

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

Signature Mary Ann Walthers (Signature of Notary Public)

Place Notary Seal Above

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Though the information below is not required by law, it may prove valuable to persons relying on the document and could prevent fraudulent removal and reattachment of this form to another document.

Description of Attached Document

Title or Type of Document: Assignment of Patent Rights

Document Date: December 10, 2009 Number of Pages: 4

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Electronic Patent Application Fee Transmittal

Application Number:	12713220
Filing Date:	
Title of Invention:	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR
First Named Inventor/Applicant Name:	Andrew WOLFE
Filer:	Gene I. Su
Attorney Docket Number:	121-0019-US-REG

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1090**

Electronic Acknowledgement Receipt

EFS ID:	7095537
Application Number:	12713220
International Application Number:	
Confirmation Number:	4243
Title of Invention:	PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR
First Named Inventor/Applicant Name:	Andrew WOLFE
Customer Number:	83446
Filer:	Gene I. Su
Filer Authorized By:	
Attorney Docket Number:	121-0019-US-REG
Receipt Date:	26-FEB-2010
Filing Date:	
Time Stamp:	12:21:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1090
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1	Fee Worksheet (PTO-875)	fee-info.pdf	32952 29c817e7692bd29f2aa26e2a4dd25898bb9099b1	no	2

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Information:

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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Filing Date: 02/26/2010

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number **12/713,220**

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	LARGE ENTITY RATE ($)	LARGE ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	12711517N/A	N/A	N/A			N/A	**330**
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	**540**
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	**220**
TOTAL CLAIMS (37 CFR 1.16(i))	**20** minus 20 =	**0**	X$ 26		OR	2X$52	**0**
INDEPENDENT CLAIMS (37 CFR 1.16(h))	**3** minus 3 =	**0**	X$110			1X$220	**0**
APPLICATION SIZE FEE (37 CFR 1.16(s))	135						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195			390	**0**
			TOTAL			TOTAL	**1090**

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDI-TIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDI-TIONAL FEE ($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDI-TIONAL FEE ($)	OR	RATE ($)	ADDI-TIONAL FEE ($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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