System Level Analysis of Fast, Per-Core DVFS using On-Chip Switching Regulators

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Abstract

Portable, embedded systems place ever-increasing demands on high-performance, low-power microprocessor design. Dynamic voltage and frequency scaling (DVFS) is a well-known technique to reduce energy in digital systems, but the effectiveness of DVFS is hampered by slow voltage transitions that occur on the order of tens of microseconds. In addition, the recent trend towards chip-multiprocessors (CMP) executing multi-threaded workloads with heterogeneous behavior motivates the need for per-core DVFS control mechanisms. Voltage regulators that are integrated onto the same chip as the microprocessor core provide the benefit of both nanosecond-scale voltage switching and per-core voltage control. We show that these characteristics provide significant energy-saving opportunities compared to traditional off-chip regulators. However, the implementation of on-chip regulators presents many challenges including regulator efficiency and output voltage transient characteristics, which are significantly impacted by the system-level application of the regulator. In this paper, we describe and model these costs, and perform a comprehensive analysis of a CMP system with on-chip integrated regulators. We conclude that on-chip regulators can significantly improve DVFS effectiveness and lead to overall system energy savings in a CMP, but architects must carefully account for overheads and costs when designing next-generation DVFS systems and algorithms.

1. Introduction

Dynamic voltage and frequency scaling (DVFS) was introduced in the 90's [19], offering great promise to dramatically reduce power consumption in large digital systems by adapting both voltage and frequency of the system with respect to changing workloads [16,28, 30,36]. Unfortunately, the full promise of DVFS has been hindered by slow off-chip voltage regulators that lack the ability to adjust to different voltages at small time scales. Modern implementations are limited to temporally coarse-grained adjustments governed by runtime software (i.e. the operating system) [1,31]. In recent years, researchers have turned to chip multiprocessor architectures as a way of maintaining performance scaling while staying within tight power constraints. There are several examples of processors that use a large number of simple tiles, demonstrating a trend towards many-core designs [6, 22, 26]. This trend, coupled with diverse workloads found in modern systems, motivates the need for fast, per-core DVFS control.

Voltage regulators are found in nearly all computing systems and are essential for delivering power from an energy source (e.g., battery) to multiple integrated circuits (e.g., microprocessor) at their respective, desired fixed or time-varying voltage levels. In order to achieve high energy-conversion efficiencies, inductor-based switching voltage regulators are commonly used. Conventional switching regulators operate at relatively low switching frequencies ($<$ 5MHz) and utilize bulky filter components (i.e. discrete inductors and capacitors) [21, 23, 37, 39]. Hence, voltage regulator modules (VRM) typically are separate, board-level components that, unfortunately, have slow voltage adjustment capabilities—limited to tens of microsecond timescales. The cost and bulk of these modules also preclude using these efficient regulators to implement multiple on-chip power domains.

In recent years, there has been a surge of interest to build on-chip integrated switching voltage regulators [5, 14, 27, 34]. These regulators offer the potential to provide multiple on-chip power domains in future CMP systems. An on-chip regulator, operating with high switching frequencies, can obviate bulky filter components (the filter inductor and capacitor), allow the filter capacitor to be integrated entirely on the chip, place smaller inductors on the package, and enable fast voltage transitions at nanosecond timescales. Moreover, an on-chip regulator can easily be divided into multiple parallel copies with little additional overhead, readily providing multiple on-chip power domains. Unfortunately, these potential benefits are tempered by lower energy-conversion efficiencies resulting from high switching frequencies and increased susceptibility to load current steps.

This paper explores the interplay of the promising characteristics and costs of employing on-chip regulator designs in modern CMP system architectures. While this study considers CMP designs comprising multiple low-power processor cores within the context of a mobile embedded system, the analysis described throughout this paper can be extended to higher-power processors as well.

Figure 1 illustrates three power-supply configurations that this paper studies. The first configuration (left) represents a conventional design scenario that only uses an off-chip voltage regulator. This voltage regulator directly steps the power supply voltage, assumed to be 3.7V provided by a Li-Ion battery, down to a processor voltage ranging from 0.6V to 1V. The second configuration (middle) implements a two-step voltage conversion scenario. Given an inherent degradation in conversion efficiencies for large step-down ratios, an off-chip regulator performs the initial step-down from 3.7V to 1.8V, which can be shared by other on-board components. The 1.8V supply then drives an on-chip voltage regulator that further steps the voltage down to a range of 0.6V to 1V as a single power supply domain distributed across a 4-core CMP. The third configuration (right) expands on the second configuration by providing four separate on-chip power domains via individual on-chip voltage regulators. These three configurations constitute the framework through which we compare the costs and benefits of fast, per-core DVFS enabled by on-chip regulators.

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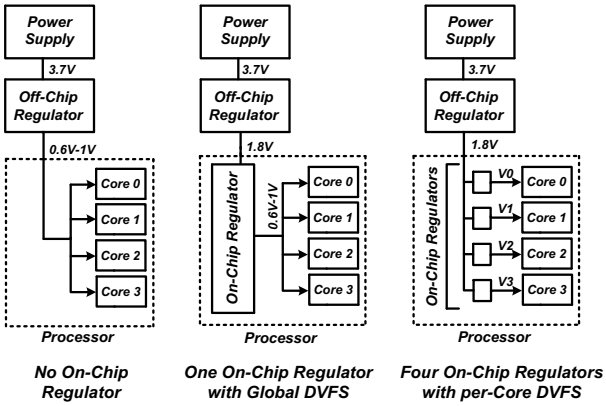

Figure 1. Three power-supply configurations for a 4-core CMP.

The main contributions of this work are as follows:

1. We explore the energy savings offered by implementing both temporally fine-grained and per-core DVFS in a 4-core CMP system using an offline DVFS algorithm (Section 2).
2. We present a detailed on-chip regulator model and design space analysis that considers key regulator characteristics—DVFS transition times and overheads, load current transient response, and regulator losses (Sections 3 and 4).
3. We combine the energy savings with the on-chip regulator cost models and come to several conclusions. For a single power domain, on-chip regulator losses offset the gains from fast DVFS for many workloads. In contrast, fast, per-core DVFS can achieve energy savings (>20%) when compared to conventional, single power domain, off-chip regulators with comparatively slow DVFS (Section 5).

2. Potential of Fast and Per-Core DVFS schemes

Dynamic voltage and frequency scaling can be an effective technique to reduce power consumption in processors. DVFS control algorithms can be implemented at different levels, such as in the processor microarchitecture [20], the operating system scheduler [17], or through compiler algorithms [15, 38]. Most previous work in the domain of DVFS control algorithms focus on coarse temporal granularity, e.g., voltage changes on the order of several microseconds, which is appropriate given slow response times of off-chip regulators. In contrast, on-chip regulators offer much faster voltage transitions as presented in Figure 2. This figure, a simulation of the on-chip regulator model described in a later section, shows voltage transitions can occur on the order of tens of nanoseconds, several orders of magnitude faster than off-chip regulators. DVFS algorithms implemented at the microarchitecture level provide the finest level of temporal control, hence, are good candidates for the fine-grained approach that we consider. In this section, we explore the benefits of fast DVFS with fine temporal resolution and also highlight the benefits of per-core voltage domains compared to chip-wide DVFS. To explore the benefits and tradeoffs associated with temporally fine-grained and per-core DVFS, we rely on an offline DVFS algorithm that can easily be applied across the wide range of DVFS transition times we consider. Section 2.1 provides a brief overview of the simulation framework used in our study, and the methodology of the offline DVFS algorithm is described in Section 2.2. We then discuss the effects of finer temporal granularity (Section 2.3), and the savings for per-core versus chip-wide DVFS schemes (Section 2.4).

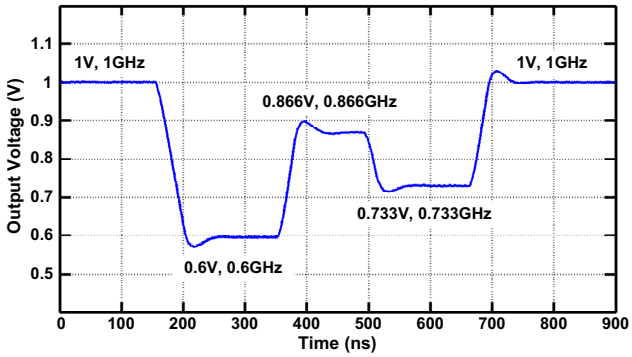

Figure 2. DVFS transition times with an on-chip regulator

Frequency	1GHz @ 65nm	**Vdd**	1 V
Core Area	16mm^2	**Fetch/Issue/Retire**	2/2/2
Branch Penalty	7 cycles Hybrid Branch Predictor	**Branch Predictor**	BTB (1K entries) RAS (32 entries)
Int registers	32	**FP registers**	32
IL1	32KB, 32-way, 32B block Hi/Miss latency 2/1 cycles	**DL1**	32KB, 32-way, 32B block Hi/Miss latency 2/1 cycles MESI-protocol
ITLB entries	64	**DTLB entries**	128
MSHR size	8	**Write Buffer size**	16
L2 size	512 KB	**MSHR size**	16

Table 1. Processor configuration and system parameters for SESC.

2.1 Simulation Framework

We employ an architectural power-performance simulator that generates realistic current traces. We use SESC [25], a multi-core simulator, integrated with power-models based on Wattch [7], Cacti [29], and Orion [32]. A simple in-order processor model represents configurations similar to embedded processors like Xscale [10]. The per-core current load is 400mA when fully active and 120mA when idle. We model a configuration with a shared-L2 configuration, private-L1 caches in each processor, and a MESI-based coherence protocol. Table 1 lists the details of the 4-core processor configuration and system parameters. The simulator was modified to obtain cycle-by-cycle current profiles for each core in the system.

In a CMP-based system, it is important to understand the interactions between the multiple cores. These interactions can be accurately characterized by analyzing a mix of multi-threaded and multi-programmed benchmarks. We use a composite benchmark suite composed of applications from SPEC2K, ALPBench [18], and SPLASH2 [35]. For multi-programmed scenarios, we consider several mixtures of a memory-bound benchmark (*mcf*) and a cpu-bound benchmark (*applu*) from SPEC2K. Table 2 lists the different benchmarks used in this study along with the ratio of memory cycles to total runtime of the application for each. All benchmarks are run for 400M instructions after fast forwarding through the initialization phase.

2.2 Offline DVFS Algorithm

The goal of any DVFS algorithm is to minimize energy consumption of the application within certain performance constraints. This can be done by exploiting the slack due to asynchronous memory events. Scaling down the frequency of the processor slows down cpu-bound operations, but does not affect the time taken by memory-bound operations. We exploit the presence of such memory-bound intervals to reduce the voltage and frequency of the processor. The effectiveness of such a DVFS scheme is directly related to the ratio of memory-bound cycles to cpu-bound cycles.

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Benchmarks	Description	Memory Cycles / Total Runtime
ocean-con	Large Scale Ocean Simulation	0.47
fft	Fast Fourier Transform	0.4
facerec	CSU Face Recognizer	0.22
cholesky	Cholesky Factorization	0.197
raytrace	Tachyon Ray Tracer	0.058
mcf4	4-high memory-bound (*mcf*)	0.697
mcf3, applu1	3-high memory-bound (*mcf*) and 1-high cpu-bound (*applu*)	0.697 (*mcf*) and 0.051 (*applu*)
mcf2, applu2	2-high memory-bound (*mcf*) and 2-high cpu-bound (*applu*)	
mcf1, applu3	1-high memory-bound (*mcf*) and 3-high cpu-bound (*applu*)	
applu4	4-high cpu-bound (*applu*)	0.051

Table 2. Benchmark Suite.

As this paper aims to study the potential system-wide benefits of using on-chip voltage regulators, the offline algorithm is applied to all configurations and it optimizes DVFS settings based on a global view of workload characteristics. We formulate the DVFS control problem as an integer linear programming (ILP) optimization problem, which seeks to reduce the total power consumption of the processor within specific performance constraints (δ). This approach is similar to the one proposed in [38]. We divide the application runtime into N intervals based on different temporal granularities of DVFS. A total of L = 4 voltage/frequency (V/F) levels are considered. For each runtime interval i and frequency j, the power consumption, P_{ij}, is calculated. The delay for each interval and V/F level, D_{ij}, is also calculated. Heuristics for the delay of individual intervals are obtained by calculating the relative memory-boundness of each interval through cache miss behavior. Equations 1- 3 specify the ILP formulation of our offline algorithm. The overheads associated with switching between different voltage/frequencies settings are not considered in the optimization, but are included later in Section 4.

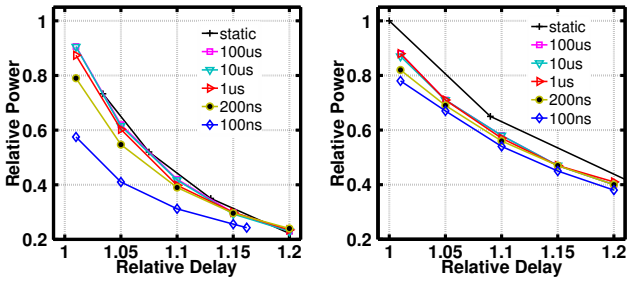
$$min(\sum_{i=1}^{N}\sum_{j=1}^{L} P_{ij}x_{ij}) \quad (1)$$

$$(\sum_{i=1}^{N}\sum_{j=1}^{L} D_{ij}x_{ij}) < \delta \quad (2)$$

$$\sum_{i=1}^{N}\sum_{j=1}^{L} x_{ij} = N \quad (3)$$

We consider an in-order processor with the capability of switching between four voltage settings: 1V, 0.866V, 0.733V, and 0.6V, with proportionally scaled frequencies from 1GHz down to 600MHz. As in Xscale [10], we assume the processor can operate through voltage transitions by quickly ramping down frequency before the voltage ramps down. Conversely, we ramp up the voltage and only switch the frequency after the voltage has settled to higher levels. Clock synthesis that combines finely-spaced edges out of a delay-locked loop can provide rapid frequency adjustment without PLL re-lock penalties [11].

The offline algorithm finds voltage/frequency settings at each interval to minimize power while maintaining a specified performance constraint. In this study, we consider performance constraints of 1%, 5%, 10%, 15%, and 20%. In order to keep the runtime overheads of the ILP algorithm tractable, we divide the simulation trace into smaller windows of 2M cycles each; finding optimal DVFS assignments within the windows, but not necessarily across the entire trace. The overall power savings presented in this paper represents the average power savings across all 2M-cycle windows for each application.



(a) *mcf* (b) *fft*

Figure 3. Benefits of fine-grained DVFS scheme for *mcf* and *fft*.

2.3 Effects of Finer Temporal Resolution

On-chip regulators allow voltage transitions to occur at a rate of tens of nanoseconds as compared to microseconds for off-chip regulators. The fast voltage-scaling capability of on-chip regulators provides the potential for applying DVFS at very fine-grained timescales. A fine-grained DVFS scheme can more closely track different cpu- and memory-bound phases than a coarse-grained scheme and, hence, reduce power consumption without performance degradation. However, the power-saving benefits of a fine-grained technique depend on the distribution of memory misses in the benchmark.

Figure 3(a) shows the impact of scaling temporal DVFS resolutions for *mcf* and *fft*. Resolutions in the range of 10-100μs represent the coarse-grained DVFS schemes and 100-200ns represent fine-grained, on-chip DVFS. We also consider a static voltage/frequency scaling scheme (representative of coarse-grained OS-level control) that fixes DVFS settings at one point for the entire benchmark for each performance target. In some cases, the ILP algorithm fails to match the performance constraint and data points may deviate from initial performance targets. As discussed previously, *mcf* is a memory-bound benchmark, with approximately 70% of its runtime spent servicing memory misses. The fine-grained approach can capture these memory-miss intervals and achieve as much as 60% power savings for only 5% performance degradation. In contrast, coarse-resolution windows fail to capture all of these intervals, achieving less power savings for the same performance constraint (between 35-40% savings for the same 5% performance loss). In general,we find that the benefits of fast DVFS depends heavily on the application. For example, fine-grained DVFS is not much better than the coarse-grained schemes for *fft* (Figure 3(b)), but show an 8% power benefit compared to static voltage/frequency scaling.

2.4 Per-Core vs. Chip-Wide DVFS

Chip multiprocessor systems running heterogeneous workloads add the dimension of benefiting from per-core DVFS. Isci et al. show multiple power domains offer power savings in CMP systems over a single power domain [16]. However, due to cost and system board area constraints, it may not be practical to implement multiple power domains using off-chip voltage regulators. On the other hand, on-chip regulators can easily be modified to accommodate multiple power-domains with little additional cost (explained in Section 4). We refer to chip-wide DVFS as a global setting for voltage/frequency of the entire chip based on the activity of the whole chip, as opposed to each core. In this section we compare per-core and chip-wide DVFS schemes with 100ns transition times for both multi-threaded and multi-programmed workloads.

Figure 4 plots the relative power savings for per-core DVFS and chip-wide DVFS schemes across a range of multi-threaded bench-

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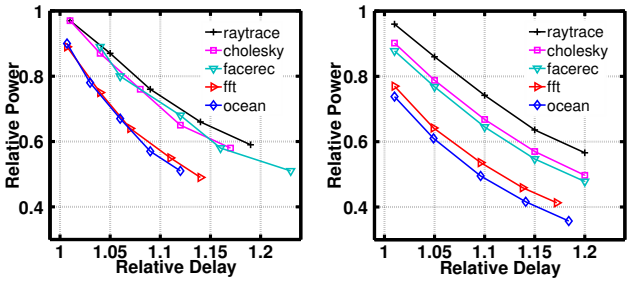
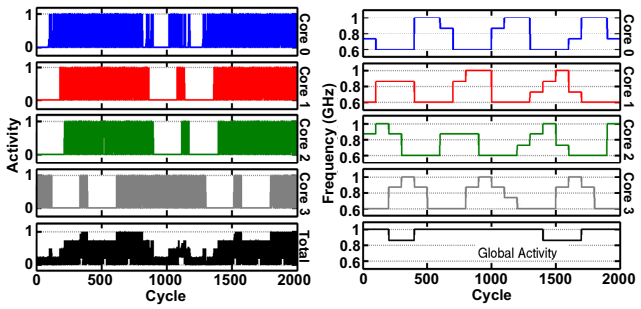


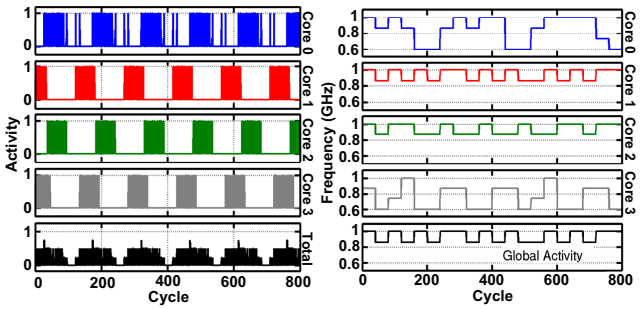
(a) Chip-Wide DVFS (b) Per-Core DVFS

Figure 4. Per-Core DVFS for multi-threaded applications.



(a) Activity profile of *ocean* (b) Frequency settings

Figure 5. Snapshot of *ocean* with per-core and chip-wide DVFS.

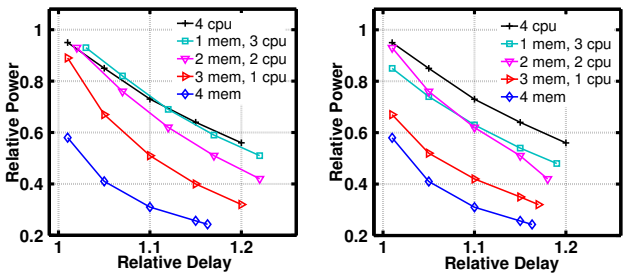


(a) Activity profile of *fft* (b) Frequency settings

Figure 6. Snapshot of *fft* with per-core and chip-wide DVFS.

marks and a significant difference can be observed for most of the benchmarks (e.g., *ocean, fft, facerec*). However, benchmarks like *raytrace* yield only slight differences between the two approaches. This can be attributed to the highly cpu-bound behavior of *raytrace*, which offers fewer frequency-scaling opportunities.

Multi-threaded applications can have similar phases (cpu- or memory-bound) of operation across the cores. Figure 5(a) shows a snapshot of activity on each core for a four-threaded version of *ocean*. We see similar behavior across all four threads, but there is a slight shift in the activity across the cores. While per-core DVFS is able to capture DVFS scaling opportunities in the individual threads, the time windows where the scaling is applied are different. Because of this, a chip-wide DVFS scheme, based on the combined activity of the four threads, finds fewer DVFS scaling opportunities as shown by the global scaling in Figure 5(b). In contrast, Figure 6(a) presents the activity snapshot for *fft*. We see that the activity profiles of core 0 and core 2 are synchronized in time, as are the activity profiles of core 1 and core 3. This leads to a more effective chip-wide DVFS schedule, demonstrated by the



(a) Chip-Wide DVFS (b) Per-Core DVFS

Figure 7. Per-core DVFS for multi-programming scenarios.

global scaling in Figure 6(b). As mentioned in Section 2.2, the offline algorithm relies on a global view of each 2M cycle window and, hence, the local voltage/frequency assignments for short intervals shown do not necessarily line up with local activities.

Figure 7 plots the relative power vs. delay for multi-programmed scenarios with per-core and chip-wide DVFS. The figure shows different combinations of *mcf* (a memory-bound application) and *applu* (a cpu-bound application), ranging from all four cores running *mcf* to all four cores running *applu*. Per-core DVFS achieves similar power savings as chip-wide DVFS for both extremes (all memory-bound or all cpu-bound) as there is little per-core variation to exploit. On the other hand, we observe an additional 18% of power savings for the per-core DVFS scheme over the chip-wide DVFS scheme at a performance degradation of 5% when one copy of *applu* and three copies of *mcf* are run on the 4-core machine.

These results show that depending on the heterogeneity of workload characteristics, per-core DVFS offers substantial additional savings compared to global DVFS schemes by better adapting to the different requirements of each core.

3. Switching Regulator Background and Modeling

While on-chip regulators facilitate fast, per-core DVFS, they also introduce various overheads. In order to understand these overheads, this section provides an overview of on-chip switching regulators and the model used for simulations. Switching regulators and linear regulators are two widely-used regulator topologies. Linear regulators offer several advantages: ease of on-chip integration, relatively small size, and good response to load current transients [13]. Unfortunately, the maximum achievable power-conversion efficiency of a linear regulator is constrained by the ratio of Vout (the output voltage of the regulator) to Vin (the input voltage to the regulator). For example, when stepping down a voltage from 1.1V to 1V, high power conversion efficiency (∼90%) is possible. However, when the output voltage is low compared to the input voltage, maximum efficiency degrades linearly. When delivering power to a processor using DVFS, the regulator has to deliver a wide range of output voltage levels, in which case the efficiency degradation of a linear regulator can be prohibitively high. In contrast, a switching regulator can regulate a wide range of output voltage levels with higher power-conversion efficiency that is less sensitive to the Vout/Vin ratio. Hence, switching regulators are better suited for loads employing DVFS [34]. This higher conversion efficiency stems from its reliance on inductors as low-loss energy-transfer devices (between Vin and Vout), but they can be bulky and consume large area. The next section introduces the basic operation of an inductor-based switching regulator that we employ for stepping down voltage, commonly referred to as buck converters.

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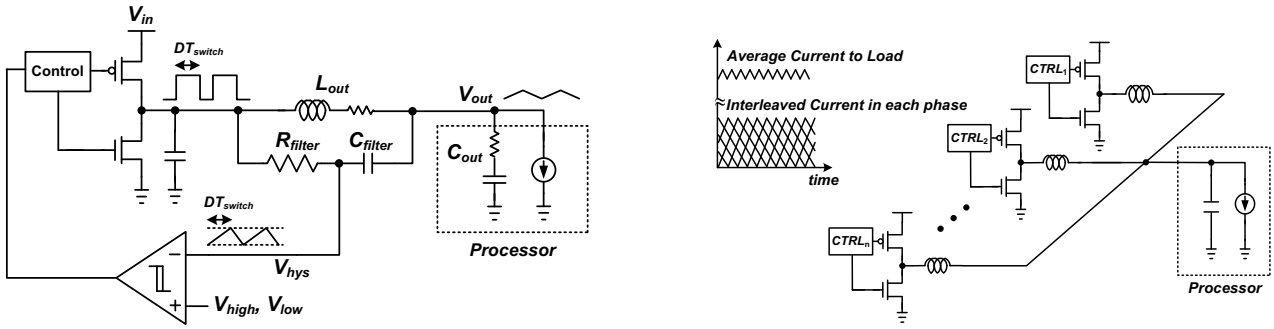

(a) Buck converter with hysteretic control

(b) Multiphase buck converter

Figure 8. Buck converter schematics

3.1 Background on Buck Converters

A typical buck regulator, shown in Figure 8(a), is comprised of three sets of components: switching power transistors, the output filter inductor (L_{out}) and capacitor (C_{out}), and the feedback control consisting of a hysteretic comparator and associated filter elements (C_{filter} and R_{filter}) that enhance loop stability. The power transistors can simply be viewed as an inverter that switches on and off at a switching frequency and provides a square wave to the low-pass output filter composed of L_{out} and C_{out}. The regulator output, V_{out}, powers the microprocessor load and its voltage is approximately set by the duty cycle of the square wave. This regulated voltage exhibits small ripples since the filter attenuates the high-frequency square wave. The feedback loop is closed by feeding V_{hys}, which is the output of the filter composed of C_{filter} and R_{filter}, to the hysteretic comparator. The duty cycle of the square-wave input to the power transistors is set by the hysteretic comparator output. As shown in Figure 8(a), the hysteretic comparator has a high threshold (V_{high}) and a low threshold voltage (V_{low}). The PMOS power switch turns on when V_{hys} drops below V_{low}, and the NMOS turns on when the V_{hys} increases above V_{high}. Since V_{out} directly affects V_{hys}, when V_{out} fluctuates in response to load current transients, hysteretic control can react very quickly. While there are several other feedback control schemes one can employ for a buck regulator, hysteretic control offers fast transient response characteristics while keeping design complexity low [21].

The power transistors and inductor shown in Figure 8(b) can be interleaved to form a multiphase buck converter. Multiphase converters have been proposed for high load current applications [23, 37, 39], since they can reduce the peak current in each inductor. Multiphase designs are also well-suited for on-chip regulators designs, because they allow for small filter inductor and capacitor sizes, and can achieve fast transient response. Parallel sets of power transistors and inductors are interleaved and connected to the same load such that current through each inductor is interleaved across even time intervals. Hence these interleaved inductor currents cancel out at the output node and result in an average current that has small ripple. Moreover, this interleaving accommodates the use of small output filter capacitance while meeting small voltage ripple constraints. However, more phases come with the overhead of consuming more on-die area. Since size of the power transistors scale with the current provided per phase, the total area of the power transistors depends on load current specifications and is largely independent of the number of phases. However, the area occupied by C_{filter}, R_{filter}, and the hysteretic comparator increases linearly with the number of phases.

3.2 Model and Simulation of Buck Regulator

This section describes how the off-chip and on-chip regulators are modeled and simulated in this work. Figure 9 illustrates the overall power delivery network of the example embedded system, from the Li-Ion battery to the processor load, for two regulator configurations—with and without an on-chip regulator. This is a more detailed version of Figure 1, adding in the parasitic elements associated with the power delivery network. This figure shows the parasitic inductors and resistors along the PCB trace and package, and decoupling capacitance added to mitigate voltage fluctuations. This model is derived from the Intel Pentium 4 package model, but scaled to be consistent with our assumptions of power draw in embedded processors [12]. The off-chip regulator is modeled as an ideal voltage source, but losses are accounted for by using power-conversion efficiencies extracted from published datasheets [4].

The on-chip regulator is modeled in greater detail with parasitics. We assume an on-chip regulator using a commercial 65nm CMOS process. Extensive SPICE simulations were run to extract parasitic values that can significantly affect regulator efficiency and performance. These parasitics include feedback control path delays, power MOSFET gate capacitance and on-state resistance, and on-chip decoupling capacitor losses. The inductors required by the on-chip regulators are assumed to be air-core surface-mount inductors [2] attached on-package [14, 27]. The inductors are connected via C4 bumps, which introduce series resistance. The total number of C4 bumps for power is assumed to be equal for both off-chip and on-chip regulators for fair comparisons. For the on-chip regulator, we use 60% of the C4 bumps to connect package-mounted inductors to the die. The remaining bumps are used to connect Vin of the on-chip regulator to the PCB. Since the off-chip scheme uses more C4 bumps to connect the processor to the package, it has lower package-to-chip impedance compared to the on-chip scheme. Careful modeling of parasitic losses is required to accurately estimate on-chip regulator efficiency, which is found to be consistent with published results [14, 27].

Transient response characteristics also impact the efficacy of using on-chip voltage regulators. Hence, we rely on a detailed Matlab-Simulink model of the on-chip regulator to thoroughly investigate the regulator's performance given load current transients and voltage transition demands of realistic workloads seen in Section 2. The model is built using the SimPowerSystems blockset [3] of Simulink. This Simulink model includes all of the parasitic elements described above since they also impact transient behavior in addition to efficiency.

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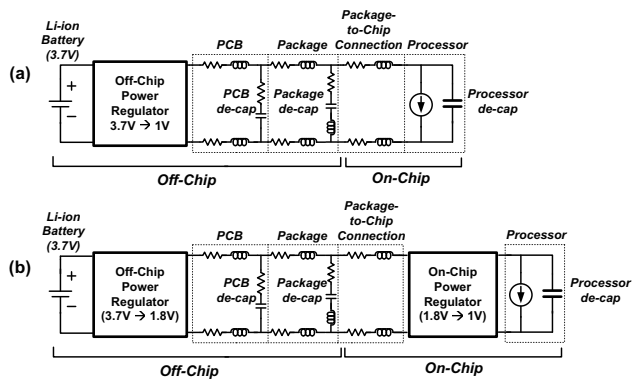


Figure 9. Power delivery network using (a) only off-chip and (b) both off-chip and on-chip regulators.

The next section studies the characteristics of on-chip regulators in more depth with simulation results based on the aforementioned model. The characteristics are presented in comparison to those for an off-chip regulator. We also study the tradeoffs associated with different regulator characteristics in order to minimize overheads.

4. Characteristics of On-Chip Regulators

Voltage regulators are typically off-chip devices [21,23,37,39] due to the large power transistors and output filter components that are required. However, this regulator module can occupy a significant portion of the PCB area, making it costly to utilize multiple regulators for per-core DVFS. Recently, on-chip regulators have been proposed, integrated on the same die as the processor load [5,14,27,34]. By using much higher switching frequencies, the bulky off-chip inductors and capacitors can be reduced in size and moved onto the package and die, respectively. Hence, on-chip regulators offer an interesting solution that can supply multiple power domains in CMPs with per-core DVFS.

In addition to reducing size, on-chip regulators are also capable of fast voltage switching, which again results from higher switching frequencies. The switching frequency of an off-chip regulator is typically on the order of hundreds of KHz to single-digit MHz, whereas on-chip regulator designs push switching frequency above 100MHz. Unfortunately, the higher frequency switching comes at the cost of degrading the conversion efficiency of on-chip regulators, lower than that of their off-chip counterparts. Hence, there are tradeoffs between regulator size, voltage switching speed, and conversion efficiency.

In order to design an on-chip regulator with minimum overheads, we study three important regulator characteristics: regulator efficiency, load transient response, and voltage switching time. Figure 10 summarizes the tradeoffs between these three characteristics. Each dot represents a regulator design with different parameters: output filter inductor and capacitor sizes, C_{filter}, R_{filter}, and switching frequency. Voltage variation is the percentage change of the output voltage droops during load transients. Regulator loss includes both switching power and resistive losses associated with the power transistors in addition to all components of resistive loss throughout the power delivery network. Different colors (or shades) of each dot correspond to how quickly the voltage can transition between 0.6V and 1V. The figure shows that different design parameters can shift regulator characteristics. Regulators with higher switching frequencies are capable of fast voltage scaling (i.e. short scaling times) and exhibit smaller voltage variations, but incur higher regulator loss. Conversely, regulators with lower switching frequencies have lower regulator loss, but exhibit larger voltage variations and slower voltage scaling capabilities. By understanding these characteristics, designers can exploit the tradeoffs to minimize overheads depending on the specific needs and attributes of the processor load. For example, if the load can leverage fast DVFS for significant power savings (seen for memory-bound applications), a regulator that prioritizes minimization of voltage scaling times may yield the best overall system-level solution. On the other hand, if the load is steady with small current transients, design parameters ought to be chosen to minimize regulator loss. To better understand how one can make appropriate design tradeoffs, the next subsections delve into the regulator characteristics in greater detail.

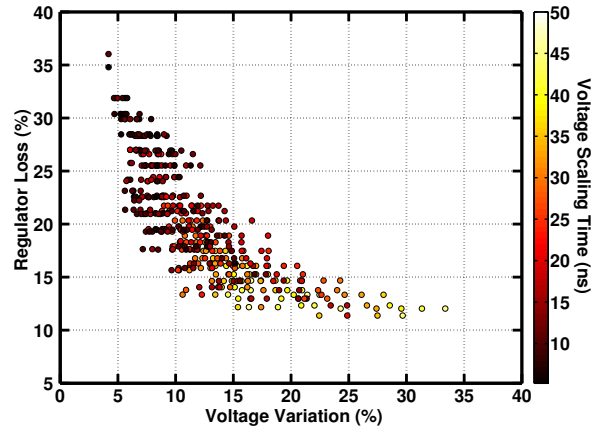
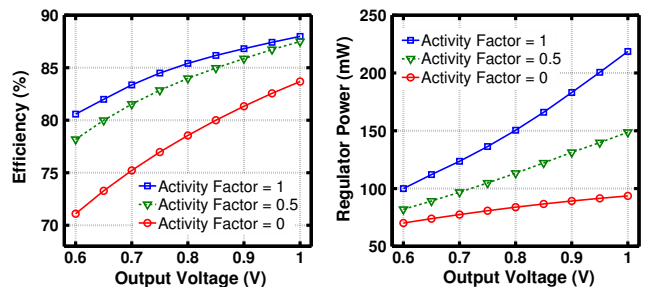


Figure 10. Regulator loss, voltage variation, and voltage scaling time of a regulator with different parameters.



(a) Efficiency (b) Power

Figure 11. Regulator efficiency and power vs. output voltage for different activity factors.

4.1 Regulator Efficiency

An ideal regulator delivers power from a power source (e.g., battery) to the load without any losses. Unfortunately, the regulator itself consumes power while delivering power to a load. Conversion efficiency is an important metric commonly used to evaluate regulator performance. It is the ratio of power delivered to the load by the regulator to the total power into the regulator. Regulator losses are dominated by switching power and resistive losses, which depend on the size of the switching power transistors, switching frequency, and load conditions (e.g., load current levels). Larger power devices reduce resistive losses at the expense of higher switching power. Higher switching frequencies lead to higher switching power, but can also reduce resistive loss. Hence, it is important to balance these two loss components with respect to different load conditions. Figure 11(a) shows that efficiency varies as a function of the output

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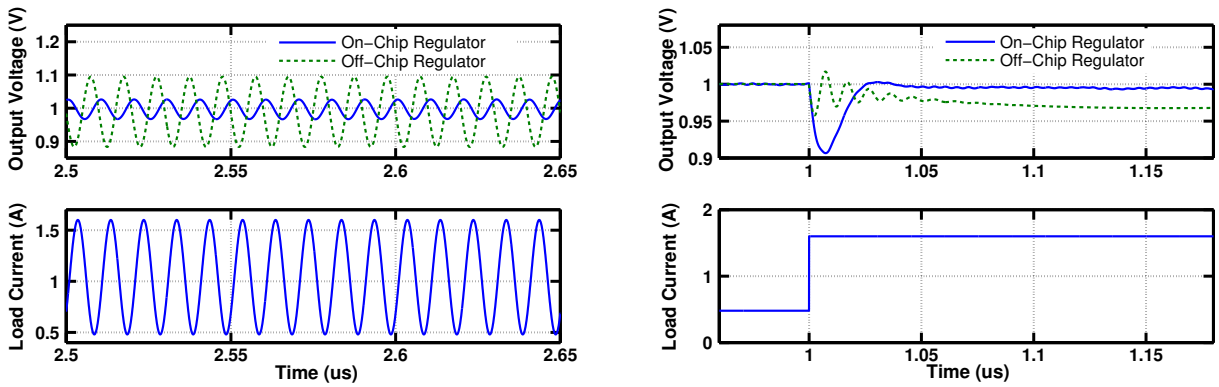

(a) Sine wave load current

(b) Step load current

Figure 12. Voltage fluctuation of off-chip and on-chip regulators during step and sine wave load current transient

voltage and processor activity, assuming a fixed input voltage. As output voltage scales down, load power scales down with CV^2f and regulator power also decreases (Figure 11(b)), but not as rapidly. Hence, the efficiency degrades at lower output voltages. Decreasing processor activity also degrades converter efficiency in a similar fashion. Since activity factors differ among benchmarks, regulator efficiency changes with benchmarks as well. However, the conversion efficiency metric alone does not appropriately capture the system-level costs and benefits of DVFS. When we later evaluate total system energy consumption and savings, it will be important to combine the on-chip and off-chip regulator losses along with DVFS-derived energy savings and overheads. Hence, this paper presents results in terms of energy (with detailed breakdowns of energy losses) instead of reporting efficiency numbers.

Although the model treats the off-chip regulator as an ideal voltage source, it includes regulator power (or loss) based on published efficiency plots found in commercial product datasheets [4]. Based on the peak efficiency values for different output voltages, we calculate the efficiency for our target input and output voltages. Efficiency of the off-chip regulator tends to be higher than that of the on-chip regulator since they have lower switching frequencies. Recalling Figure 9, (a) uses one off-chip regulator that converts 3.7V to 1V, and (b) uses an off-chip regulator that converts 3.7V to 1.8V and an on-chip regulator steps down the 1.8V input to 1V for the processor. Since conversion efficiency varies with output voltage, as shown in Figure 11, an off-chip regulator can step voltage down from 3.7V to 1.8V with higher efficiency than stepping down to 1V. Besides the losses associated with the regulator, we must also consider other losses associated with power delivery. As was observed in Figure 9, there are parasitic resistors between the battery and the processor that contribute to loss. Since higher currents flow through this resistive network when delivering power at 1V directly to the processor load from the off-chip regulator, I^2R losses are higher. In contrast, using an on-chip regulator that requires a 1.8V input permits lower current flow ($\sim$1/1.8) through the resistive network between the off-chip regulator and the chip. This difference in resistive loss is also included when accounting for on-chip and off-chip regulator losses.

4.2 Load Transient Response

In addition to conversion efficiency, load transient response is another important characteristic that impacts regulator performance. Simply put, a regulator's load transient response determines how much the voltage fluctuates in response to a change in current. Recalling Figure 9, it shows that there are parasitic inductors and resistors along the path between the off-chip regulator and the processor. Decoupling capacitors are typically added on the PCB, package, and chip in order to suppress voltage fluctuations. However, these capacitors and inductors can interact to create resonances in the power-delivery network. For a configuration that only relies on the off-chip regulator, a mid-frequency frequency resonance occurring in the 100MHz-200MHz range is commonly seen on the chip [12, 24]. Owing to this resonance, load current fluctuations that occur with a frequency near the resonance can lead to large on-chip voltage fluctuations. On the other hand, if the regulator is integrated on-chip, most of the parasitic elements fall between the power supply (i.e. battery) and the regulator input, as seen in Figure 9(b), suppressing this important mid-frequency resonance issue. This can be verified by applying step or sine wave load current patterns and observing how the processor voltage reacts. Figure 12 shows that a sinusoidal load current with a frequency at the mid-frequency resonance can cause large on-chip voltage fluctuations due to resonant buildup. In contrast, the on-chip regulator does not suffer this resonance problem and exhibits much smaller voltage fluctuations. Effects of this resonance can also be observed by applying a load current step. The voltage of the off-chip regulator rings before settling down, indicative of an under-damped response with resonance. In contrast, the output voltage of the on-chip regulator does not ring, but rather reveals a critically-damped system. However, the output voltage of the on-chip regulator suffers a different problem. It droops much more in response to the load current step than its off-chip regulator counterpart. This is because the on-chip regulator relies on the on-chip capacitor for both decoupling and to act as the output filter capacitor. Since this on-chip capacitor is much smaller than the total decoupling and filter capacitance used for off-chip regulators, large load current steps can rapidly drain out the limited charge stored on the capacitor before the regulator loop can respond, resulting in a large voltage droop. These plots suggest that the worst-case current trace for the off-chip regulator is a sine wave at the resonance frequency, whereas a step change is the worst-case load transient for the on-chip regulator.

In order to make a fair comparison between the on-chip and off-chip regulators, two important factors that affect load transient response are kept constant. The total on-chip decoupling capacitance is 40nF (10nF per core) and voltage margin is set to $\pm$10%. The 40nF decoupling capacitance is set such that with the conventional off-chip regulator scenario, voltage fluctuations stay within the $\pm$10% voltage margin under worst-case load conditions. This decoupling capacitance value also matches well with the Intel 80200 Processor based on the Xscale Architecture [9]. The 10% voltage

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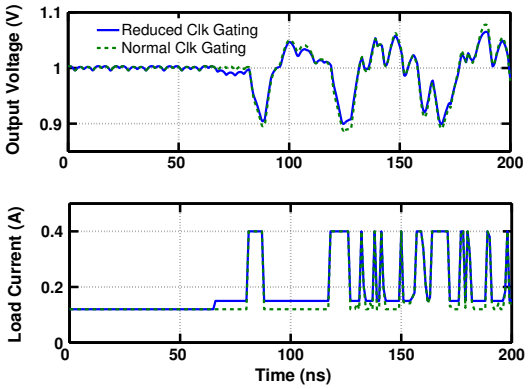

Figure 13. Example of reducing voltage fluctuations by selectively disabling clock gating.

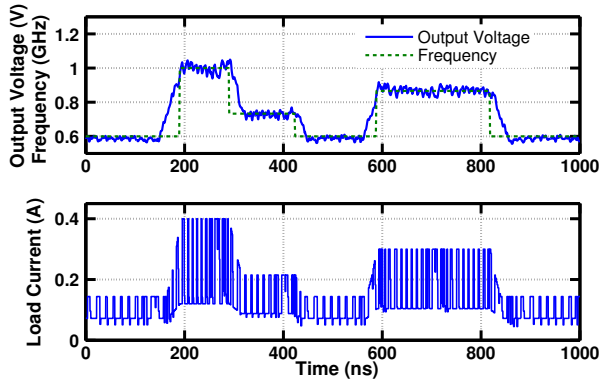

Figure 14. Snapshot of output voltage, frequency, and load current traces with DVFS.

margin is also a widely-used value in microprocessors [8, 33]. Unfortunately, the 40nF of on-chip decoupling cannot always guarantee voltage fluctuations stay within the $\pm 10\%$ margin for on-chip voltage regulators across all load transient conditions.

In order to prevent voltage emergencies, where the on-chip regulator's output voltage swings beyond $\pm 10\%$ due to sudden load current steps, we employ a simple architecture-driven mechanism that selectively disables clock gating. Since large load transients can largely be attributed to aggressive clock gating events, disabling some of the gating can reduce the magnitude of load current steps. Figure 13 shows voltage traces corresponding to load current transients for two clock gating scenarios. A sudden current increase that occurs after a long stall period causes a voltage emergency and large current steps following the first step also cause subsequent voltage emergencies. By appropriately disabling some of the clock gating (solid line), current transient magnitudes are reduced and the voltage droops can be suppressed to stay within the 10% margin. Since clock gating is used to reduce power consumption, disabling it leads to power overhead that must be accounted for. Hence, this technique is sparingly applied only when there are large current transients due to large fluctuations in processor activity.

4.3 Voltage Scaling Time

Voltage scaling time is another important characteristic that affects systems with DVFS. When the regulator voltage scales to a new voltage level, it cannot scale immediately, but scales gradually. Figure 14 shows voltage, frequency, and current traces for an on-chip regulator that drives a single processor core running *fft*. The frequency changes abruptly whereas the voltage scales across tens of nanoseconds. To ensure sufficient timing margins for the processor core, low-to-high frequency transitions are allowed after the voltage settles to the higher level. Similarly, high-to-low frequency transitions precede voltage changes. This difference between frequency and voltage transition times leads to energy overhead. We account for this wasted energy as DVFS overhead. Higher switching frequencies and/or smaller output filter component sizes can enable faster voltage scaling to reduce this DVFS overhead, but they introduce penalties of higher regulator loss and/or more sensitivity to load current transients.

4.4 On-Chip Regulators for Single and Multiple Power Domains

Given their small size compared to off-chip regulators, several on-chip regulators can be integrated on-chip to deliver power to multiple voltage domains. However, there is a tradeoff between using one voltage domain versus multiple voltages domains. For fair comparison, we assume that the total number of phases for the multiphase on-chip regulator we use is constant for single and multiple voltage domain configurations, matching the area overhead. In other words, an 8-phase regulator is used to power a single voltage domain, while four 2-phase regulators deliver power to four different voltage domains. Again, we assume that each core has 10nF of on-chip capacitance for each of the 2-phase regulators in the multiple voltage domain scenario and a total capacitance of 40nF for a single 8-phase on-chip regulator for the single voltage domain case.

There are several differences related to implementing single versus multiple power domains using on-chip regulators in a 4-core CMP. With four voltage domains, each regulator is only sensitive to current transients in its respective core. For a single power domain, the regulator sees current transients from all four cores, but also benefits from the larger on-chip capacitance. For a multi-threaded version of *facerec* running on a 4-core CMP, maximum current steps (between idle and full activity) occur over 125K times within 1M cycles for each core. In contrast, with a single voltage domain, the maximum current step (between all four cores idles and all four cores fully active) occurs much less frequently, only 350 times out of 1M cycles. These differences affect the appropriate tradeoffs a designer must make to minimize overheads and maximize energy savings. Given the higher potential for voltage emergencies with multiple power domains, the previously-described technique that disables clock gating may trigger frequently and incur high power penalties. Higher switching frequencies may improve load transient response to reduce overheads in spite of higher switching losses.

Given the tradeoffs between regulator loss, load transient response, and voltage scaling time, we can choose different regulator design parameters for both single and multiple voltage domains that minimize energy overhead. Figure 15 presents the regulator loss, DVFS overhead, and power overhead of disabling clock gating (labeled Clock Gating Loss) across different regulator design parameters for a 4-core CMP running *facerec* with one and four regulators. These plots are similar to Figure 10, but Figure 15 combines all of the losses into a total energy overhead represented by different colors for each dot. For both single and four voltage domains, configurations corresponding to dots in the bottom left corner offer the design point with the smallest total energy overheads and losses. Dots extending to the lower right have small regulator loss, but the low switching frequency leads to higher power overhead related to frequently disabling clock gating to limit current swings. Dots in the upper left corner suffer excessive regulator loss. Figure 15 also

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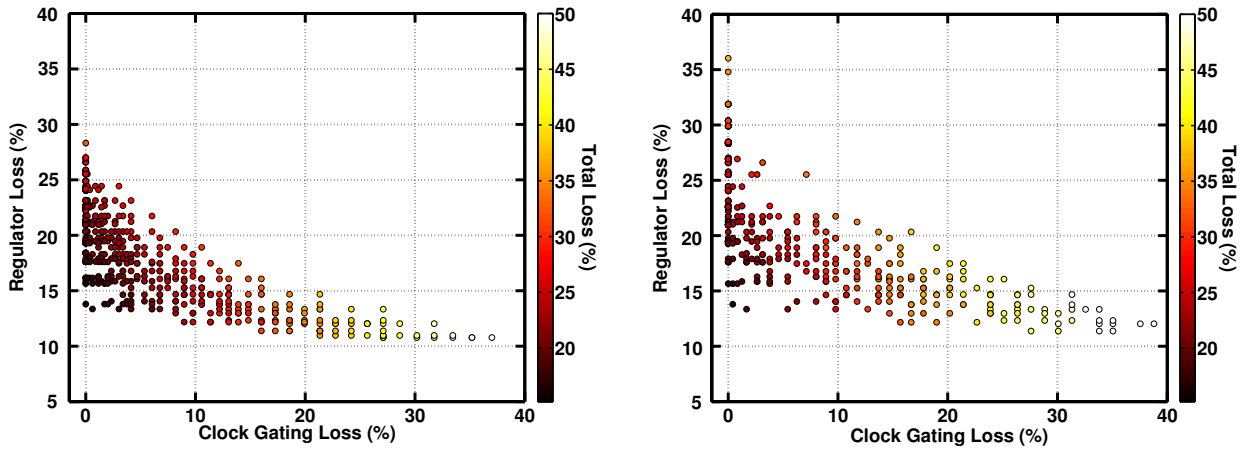

(a) 1 regulator

(b) 4 regulators

Figure 15. Total energy overhead with different regulator settings for *facerec*

	Single Power Domain	Four Power Domains
# of phases for on-chip regulator	8	2 per domain
On-chip regulator switching frequency (MHz)	100	125
Inductance per phase (nH)	13	9.6
Voltage scaling speed (mV/ns)	30	50
Total Energy Overhead (%)	15.49	17.32
Decoupling capacitance (nF)	40	10 per domain
Voltage margin (%)	± 10	

Table 3. Characteristics of the on-chip regulator (all percentage (%) numbers are relative to the processor energy with DVFS).

shows that the total loss for the single power domain tends to be smaller than that for four power domains. This can be attributed to the fact that the four power domains have to handle many more worst-case current steps as compared to the single-domain case, in which much of the current hash cancels out. Based on this analysis, the regulator design (or dot) that minimizes overhead is chosen for the single and four power domain scenarios. Details of these configuration are list Table 3, showing a single power domain scenario has around 2% smaller overhead than implementing four power domains. Similar trends are observed for other benchmarks and so we use the regulator design configurations based on the analysis above in subsequent sections of the paper.

5. Energy Savings for Per-Core and Chip-Wide DVFS using On-Chip Regulators

In previous sections, the major benefits (additional DVFS energy-saving opportunities) and overheads (DVFS overheads and regulator losses) of on-chip regulators were discussed in isolation. In this section, we return to Figure 1 and evaluate the overall benefits of on-chip regulators compared to traditional, off-chip regulators when considering all of these combined effects. We also extend our analysis to larger numbers of power domains (and on-chip regulators) to understand scalability constraints.

5.1 Comparison of Energy Savings

Figure 16 provides detailed breakdowns of the DVFS energy savings and the various overheads incurred within a 5% DVFS performance loss constraint. This analysis has been performed for four configurations: an off-chip regulator with no DVFS, an off-chip regulator with DVFS, an on-chip regulator with a single-power domain (global or per-chip DVFS), and an on-chip regulator with four power domains (local or per-core DVFS). In this figure, processor energy consumption with no DVFS is set to 100 and the other values are presented relative to this value. The reduced processor energy results achieved with DVFS represent the best selection of DVFS parameters for each configuration that maximize DVFS-energy savings while minimizing DVFS overheads: the on-chip regulator has a 100ns DVFS interval and the off-chip regulator has a 100 μs interval. To evaluate the energy savings offered by using on-chip regulators, Figure 17 presents a bar graph showing energy savings compared to the off-chip DVFS case for different benchmarks. For each benchmark, the bar on the right corresponds to how much energy savings is possible with fast DVFS, ignoring overheads. The bar on the left presents the relative savings with all of the overheads included. The gap between the left and right bars corresponds to the sum of overheads introduced by using on-chip regulators. Higher bars indicate larger relative energy savings.

These two figures represent several interesting trends in the design space which we discuss in detail below.

Off-chip DVFS vs. On-Chip, Single Power Domain: We first compare on-chip regulators with global DVFS to the off-chip regulator. At a high-level, we see that only *mcf4* achieves significant positive energy savings when compared to the off-chip regulator with DVFS. The reduction in processor energy, provided by fast DVFS, has the added benefit of reducing regulator losses. Seven of the ten benchmarks are approximately break-even (within $\pm 2\%$) between the two configurations, which means that the faster DVFS scaling can just offset the additional losses introduced by using an on-chip regulator. *Raytrace* and *cholesky* with few opportunities for DVFS, yet still suffering the impact of on-chip regulator loss, suffer significant energy overheads. One reason that off-chip DVFS performs well is that the the coarser DVFS intervals lead to less DVFS overhead compared to the on-chip regulator which may switch voltage/frequency settings more frequently.

Off-chip DVFS vs. On-Chip, Four Power Domains: The next comparison that we perform investigates the benefits of per-core DVFS scaling (on top of the fast voltage transition times) compared to the off-chip configuration which only provides a single voltage domain. This comparison provides very encouraging results for the on-chip regulator design: all of the benchmarks except *raytrace* achieve energy savings, and several by significant amounts with *ocean* achieving 21% savings. The multiple power domain config-

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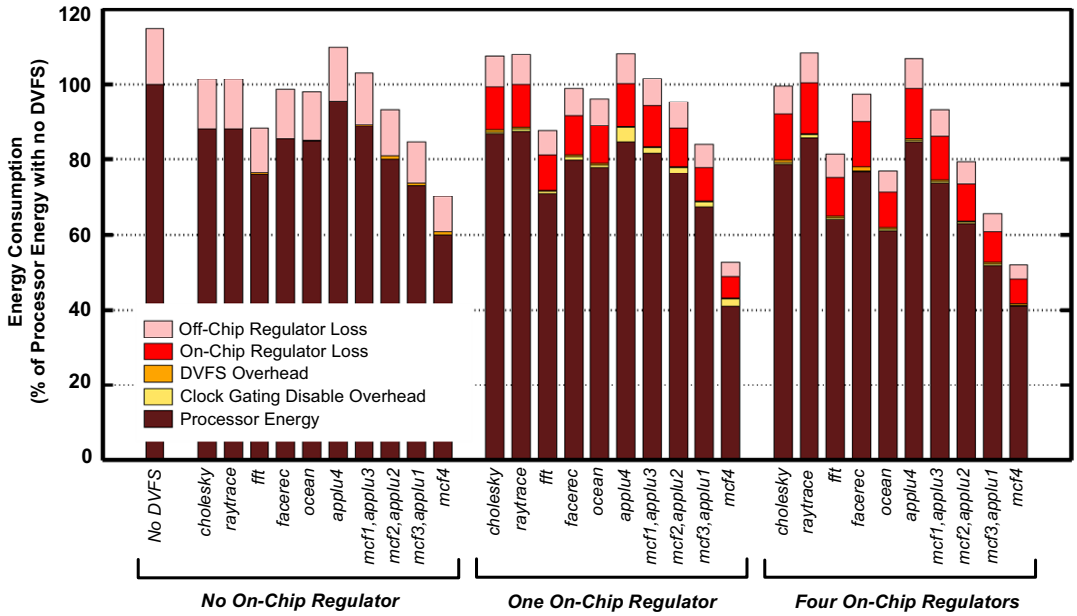

Figure 16. Detailed breakdown of energy consumption for the processor and regulator for single power domain (global) and multiple domains (per-core) DVFS.

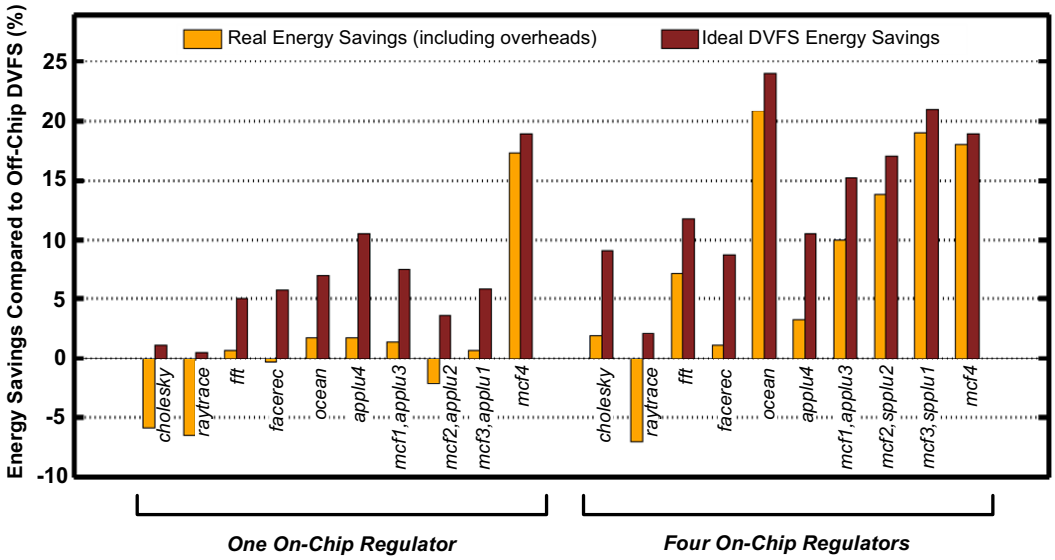

Figure 17. Relative energy consumption of on-chip regulator configurations compared to a off-chip regulator with DVFS.

uration allows even more savings through DVFS than the single domain, but needs more regulator power to deal with the additional load current hash that each core introduces. When we compare the two cases that both use on-chip regulators, Figure 16 shows that on-chip regulator loss is consistently higher by a small amount in the four domain case, but this is clearly overshadowed by the additional DVFS energy savings. There is another interesting effect that can be observed. Since regulator losses scale with load power, the gap between adjacent bars that correspond to total overheads reduces for several benchmarks, in Figure 17, since more energy savings is possible with fast, per-core DVFS. Thus, applications that significantly benefit from DVFS to reduce processor energy can also benefit from the synergistic reduction of regulator overheads.

From this analysis, we can form several conclusions regarding the impact of on-chip regulators on system design.

- Systems architects who plan to utilize on-chip voltage regulation must carefully account for energy-efficiency costs when calculating projected benefits. This requires a detailed understanding of many of the costs and overheads that on-chip regulators incur.
- DVFS scaling algorithms must adapt to take advantage of the fast, fine-grained nature of on-chip regulators. Future DVFS scaling algorithms will likely require significant microarchitectural control, rather than traditional OS-based control, and must carefully take into the DVFS scaling overheads.

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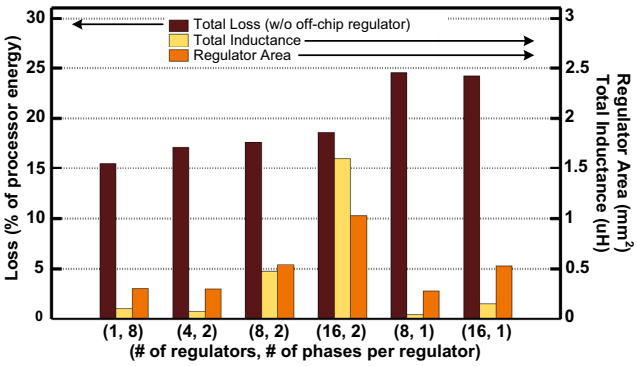

Figure 18. Loss, inductor size, and area of on-chip regulators for different numbers of power domains.

- On-chip regulators provide significant benefits to designers of CMP systems and we expect that future systems will be developed to capture this potential. The power scalability of on-chip regulators is a key future research question to extend this analysis to high-performance CMP systems with four to eight cores.

5.2 Power Domain Scalability

The previous analysis shows that multiple power domains using DVFS with finer granularity allow large energy savings. However, there is a limit to the number of on-chip power domains that can be implemented due to various overheads. This subsection compares different overheads related to implementing 1, 4, 8, and 16 power domains, equal to the total number of regulators since one regulator is used per power domain. Figure 18 shows simulation results for *facerec* with the energy loss, area overhead, and total inductance of on-chip regulators assuming these power domain scenarios in a 4-core CMP. With a total maximum power of 1.6W, 1, 4, 8, and 16 power domains consume 1.6W, 0.4W, 0.2W, and 0.1W per domain, respectively. The total loss corresponds to the sum of on-chip regulator loss, DVFS overhead, and power overhead from the architectural mechanism that disables clock gating to limit current swings, as a percentage of the processor energy. The chart also shows the total sum of inductance, indicating the number of inductors mounted onto the package scales up rapidly. The two main components that occupy significant on-die area are the power transistors and feedback circuits. Power transistor sizes are obtained using Simulink/Matlab simulations, and the values from a recently built on-chip regulator [14] are used for the feedback circuits including the hysteretic comparator, C_{filter}, and R_{filter}. This does not include the area consumed by on-chip decoupling capacitors. The total decoupling capacitance is again fixed to 40nF, which means more power domains get smaller, equally divided units of decoupling capacitance per domain. For each scenario, the regulator design is optimized to minimize energy overheads using design parameter sweeps similar to those shown in Figure 15.

The results in Figure 18 again suggest basic tradeoffs between the number of power domains and associated overheads. The first four sets of bars show that loss only increases slightly with the number of power domains. There is roughly a 3% difference between the loss for 1 domain and 16 domains. However, more power domains occupy significantly larger area, both on the package and on the die. The main reason for this is the increasing number of regulator phases. Since power transistor size scales with load current, power transistor area remains relatively constant. However, the area occupied by the feedback circuit grows proportionally with the number of phases used in the regulators. The area corresponding to 1 and 4 domains are the same, because the total number of phases used in the regulators are fixed to 8 for fair comparison as shown previously in Table 3. For 8 and 16 domains with 2-phase regulator designs, the area-increases are two- and four-fold over the 4 domain case, respectively. In addition to increases in on-die area, the total inductance increases rapidly because the number of inductors increase with more phases. Moreover, the inductance per phase increases in order to minimize energy loss associated with lower load currents. This increase in total inductance leads to higher costs and packaging complexity to mount all of the inductors. One can offset these increasing costs for 8 and 16 domains by implementing single-phase regulators at the expense of incurring more loss.

Systems that seek to use a large number of power domains with a multitude of on-chip regulators to implement DVFS with finer spatial granularity must carefully consider all of the related losses, overheads, and costs. The ideal benefits of very fine-grained DVFS may be lost or difficult to justify.

6. Related Work

There has been prior work that has focused on exploring the benefits of multiple frequency/power domains in microprocessors compared to a global frequency/voltage. In the area of CMP systems, per-core DVFS has been shown to offer larger energy savings than chip-wide DVFS using four different voltage and frequency levels [16], but this work considered relatively coarse DVFS time intervals and did not consider any of the issues related to power supply regulation. Other works explore multiple clock domain (MCD) architectures, which use globally asynchronous, locally synchronous(GALS) techniques to provide *within-core* energy control. These techniques have demonstrated 17% improvement in energy-delay product compared to using a single domain [28]. An adaptive reaction time scheme for multiple clock domain processors have been proposed [36]. These works focus on the energy savings of the processor using per-core DVFS, and the algorithms associated with it, but do not consider the practical overheads of integrating multiple on-chip regulators. As this paper shows, the practical overheads of on-chip regulators must be considered to argue that per-core DVFS actually has large energy savings. At the circuit-level, there have been many works demonstrating on-chip regulators [5, 14, 27, 34], but these works solely analyze the energy conversion efficiency of regulators. These works do not consider any of the system-level overheads (DVFS scaling and voltage transient analysis) or the system-level benefits of on-chip regulators. The contribution of this paper is the aggregation of ideal energy savings using per-core DVFS with the practical overheads of integrating on-chip regulators within each processor core.

7. Conclusion and Future Work

This paper explores the potential system-wide energy savings offered by implementing both fine-grained and per-core DVFS in a 4-core CMP system, and combines that with the practical overheads and advantages of using on-chip regulators. This is supported by a detailed model of an on-chip regulator design, which includes losses in the power delivery network. In the DVFS analysis, we show that per-core and chip-wide DVFS both offer energy savings with an offline DVFS algorithm. When we then include the regulator model and practical overheads, on-chip regulator losses and related overhead offset many of the ideal gains for a single power domain scenario. However, fast, per-core DVFS is shown to achieve up to 21% energy savings compared to conventional slow,

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chip-wide DVFS using off-chip regulators. Benchmarks that show large benefits from DVFS also gain from reductions of regulator loss, since regulator loss is directly correlated to processor power. This leads to even more gains for these benchmarks. In addition, we also show that on-chip regulators have the advantage of removing the mid-frequency resonance that is a significant problem for off-chip regulators. As the number of cores within a CMP increases, on-chip regulators offer an interesting solution to implement multiple power domains with aggressive DVFS to maximize the energy efficiency of future processors.

Acknowledgments

This work is supported by National Science Foundation grants CCF-0429782 and CSR-0720566 and Army Research Office grant W911NF-07-0331 (DARPA YFA). The findings expressed in this material are those of the authors and do not necessarily reflect the views of the funding agencies.

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