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Ishimi

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(45) **Date of Patent: Jun. 12, 2012**

(54) **MULTI-PROCESSOR DEVICE WITH GROUPS OF PROCESSORS CONSISTING OF RESPECTIVE SEPARATE EXTERNAL BUS INTERFACES**

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(51) **Int. Cl.**

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G06F 13/20	(2006.01)
G06F 15/00	(2006.01)
G06F 15/76	(2006.01)

(52) **U.S. Cl.** **710/306**; 710/307; 710/313; 710/315; 712/29

(58) **Field of Classification Search** 710/306, 710/307, 313, 315; 712/29

See application file for complete search history.

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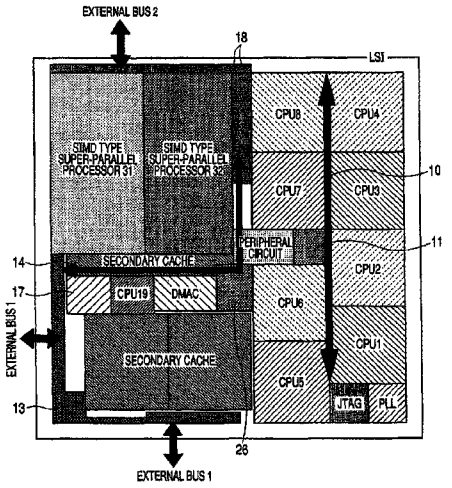
Primary Examiner — Faisal M Zaman
(74) *Attorney, Agent, or Firm* — Miles & Stockbridge P.C.

(57) **ABSTRACT**

The present invention intends to provide a high-performance multi-processor device in which independent buses and external bus interfaces are provided for each group of processors of different architectures, if a single chip includes a plurality of multi-processor groups. A multi-processor device of the present invention comprises a plurality of processors including first and second groups of processors of different architectures such as CPUs, SIMD type super-parallel processors, and DSPs, a first bus which is a CPU bus to which the first processor group is coupled, a second bus which is an internal peripheral bus to which the second processor group is coupled, independent of the first bus, a first external bus interface to which the first bus is coupled, and a second external bus interface to which the second bus is coupled, over a single semiconductor chip.

11 Claims, 11 Drawing Sheets



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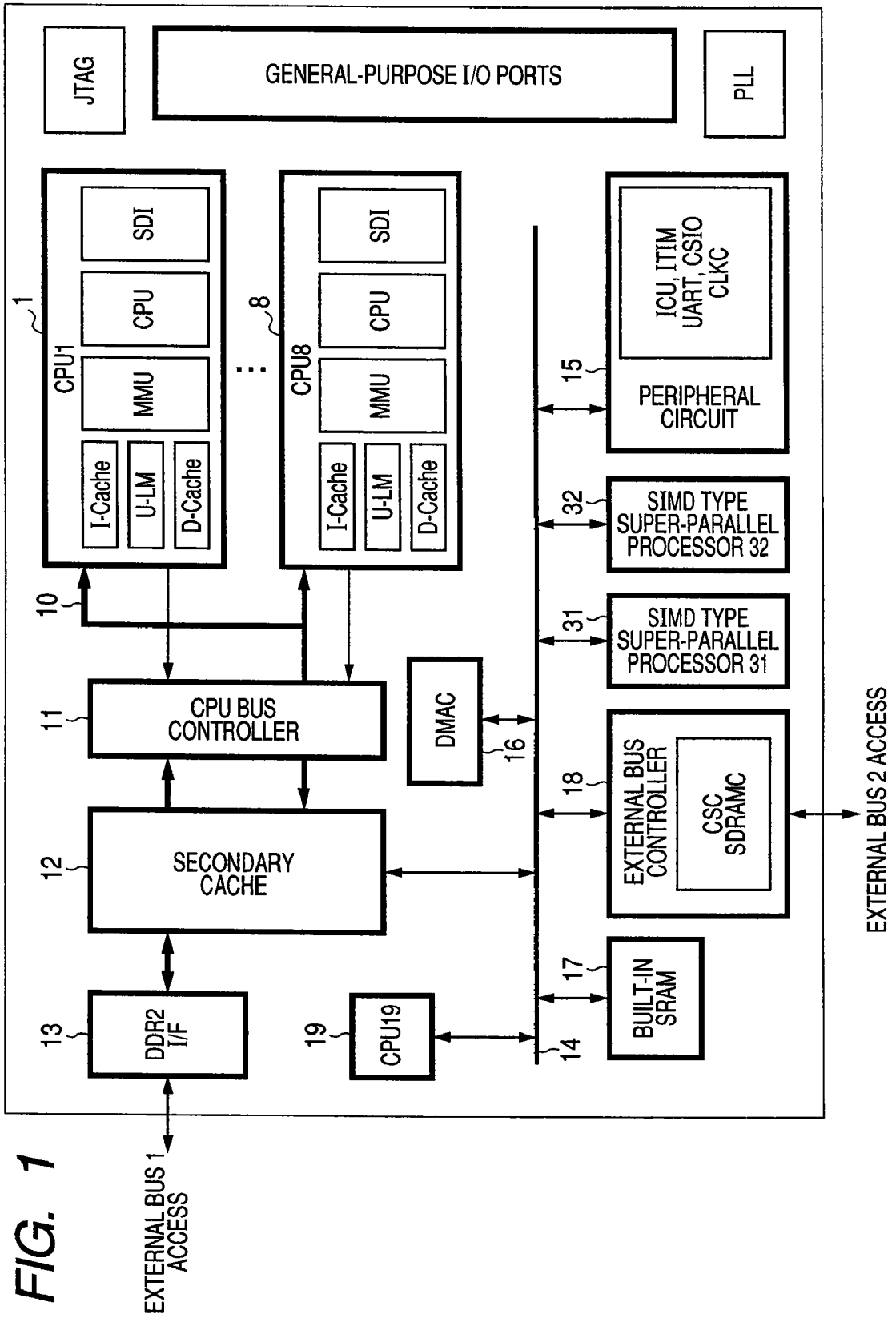
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GENERAL-PURPOSE I/O PORTS
PLL
1
CPU1
SDI
CPU
MMU
I-Cache
U-LM
D-Cache
8
CPU8
SDI
CPU
MMU
I-Cache
U-LM
D-Cache
10
11
CPU BUS CONTROLLER
12
SECONDARY CACHE
13
DDR2 I/F
EXTERNAL BUS 1 ACCESS
DMAC
16
19
CPU19
14
15
ICU, ITIM UART, CSIO CLKC
PERIPHERAL CIRCUIT
32
SIMD TYPE SUPER-PARALLEL PROCESSOR 32
31
SIMD TYPE SUPER-PARALLEL PROCESSOR 31
18
EXTERNAL BUS CONTROLLER
CSC SDRAMC
17
BUILT-IN SRAM
EXTERNAL BUS 2 ACCESS

FIG. 1

FIG. 2

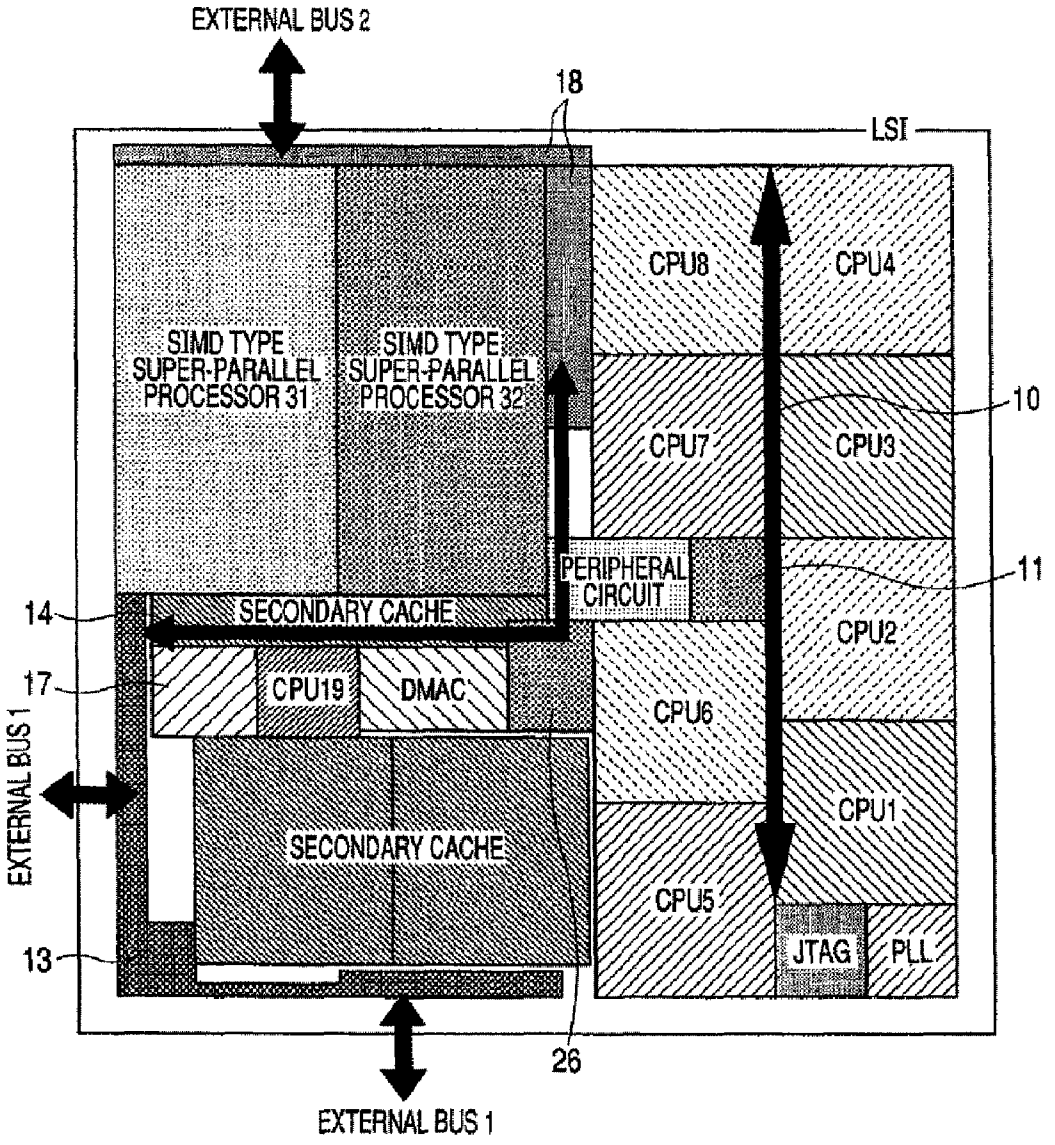
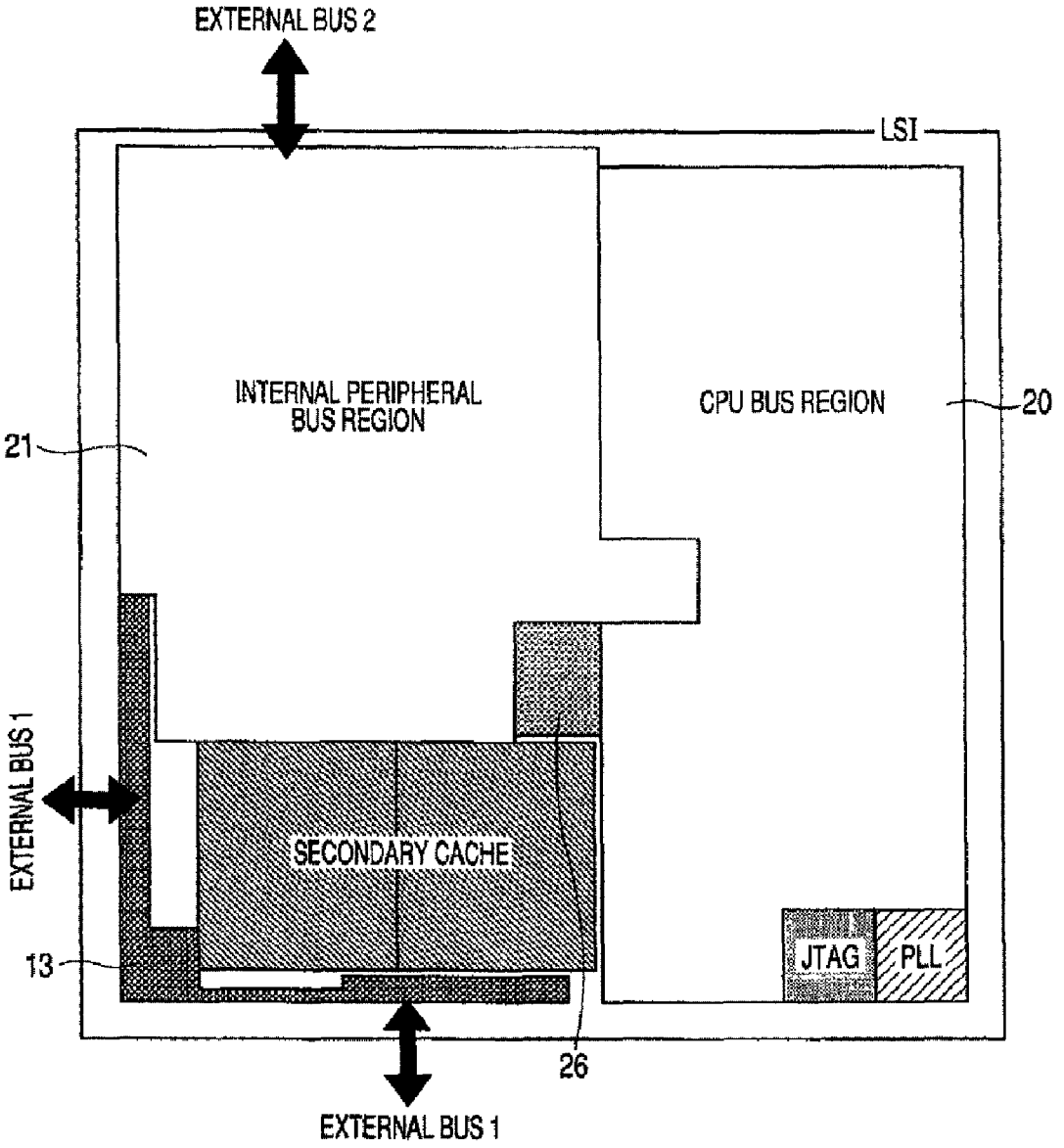

EXTERNAL BUS 2
18
LSI
SIMD TYPE SUPER-PARALLEL PROCESSOR 31
SIMD TYPE SUPER-PARALLEL PROCESSOR 32
CPU8
CPU4
CPU7
CPU3
10
PERIPHERAL CIRCUIT
11
14
SECONDARY CACHE
CPU2
17
CPU19
DMAC
CPU6
EXTERNAL BUS 1
CPU1
SECONDARY CACHE
CPU5
JTAG
PLL
13
26
EXTERNAL BUS 1

FIG. 3


EXTERNAL BUS 2
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INTERNAL PERIPHERAL BUS REGION
CPU BUS REGION
20
21
EXTERNAL BUS 1
SECONDARY CACHE
13
JTAG
PLL
26
EXTERNAL BUS 1

FIG. 4

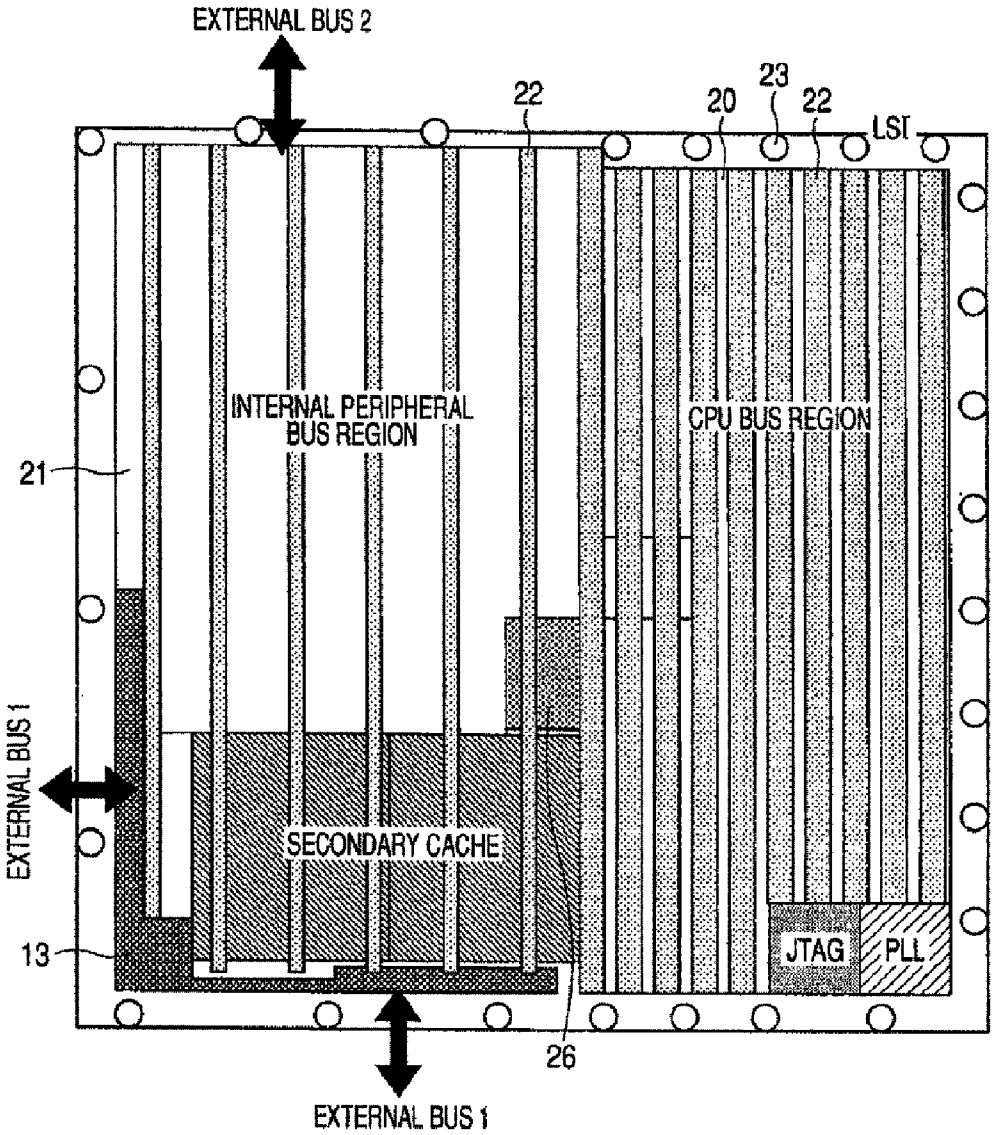
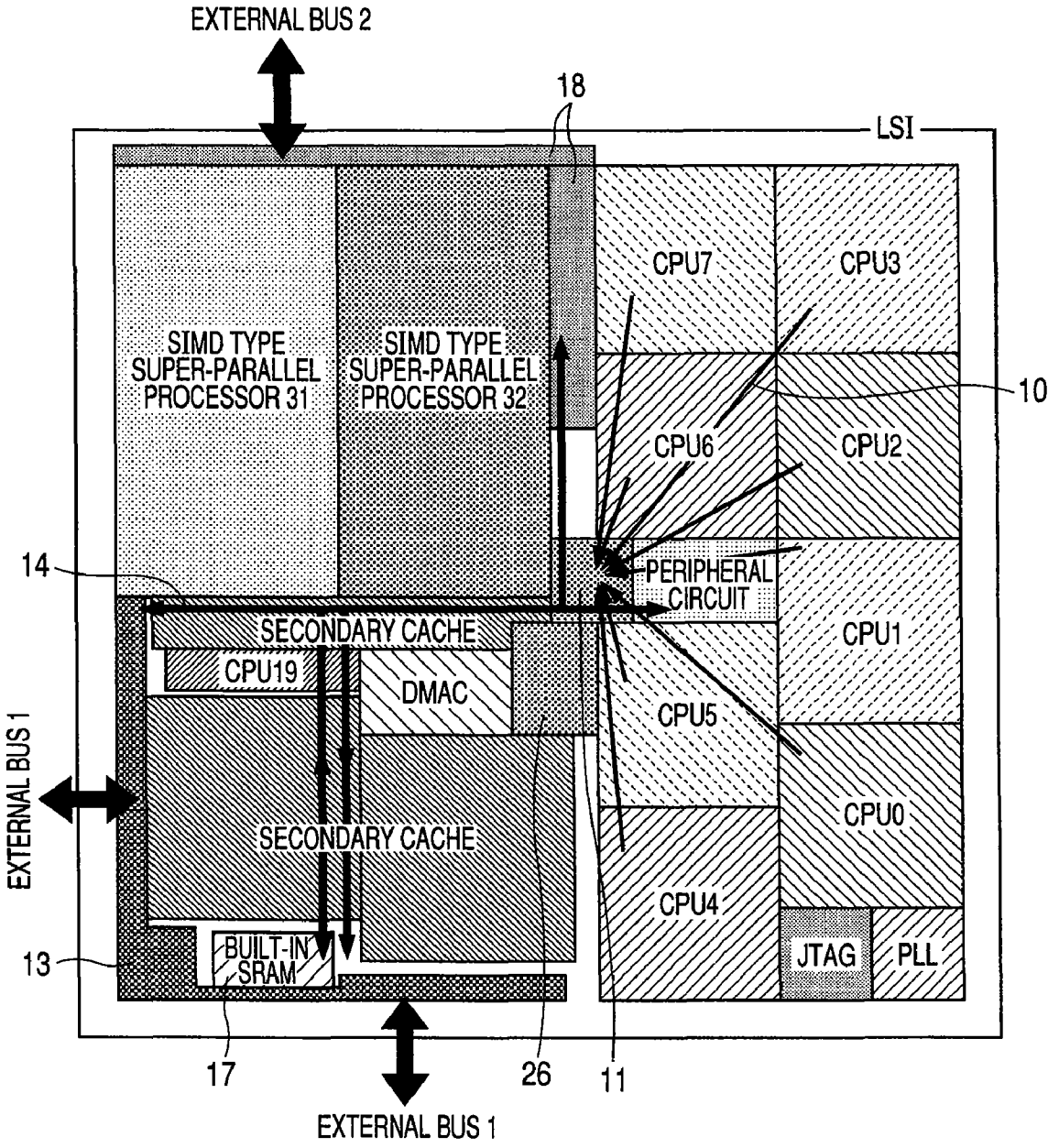

EXTERNAL BUS 2
22
20
23
22
LSI
INTERNAL PERIPHERAL BUS REGION
CPU BUS REGION
21
EXTERNAL BUS 1
SECONDARY CACHE
13
JTAG
PLL
26
EXTERNAL BUS 1

FIG. 5


EXTERNAL BUS 2
18
LSI
SIMD TYPE SUPER-PARALLEL PROCESSOR 31
SIMD TYPE SUPER-PARALLEL PROCESSOR 32
CPU7
CPU3
10
CPU6
CPU2
14
PERIPHERAL CIRCUIT
SECONDARY CACHE
CPU1
CPU19
DMAC
CPU5
EXTERNAL BUS 1
CPU0
SECONDARY CACHE
CPU4
13
BUILT-IN SRAM
JTAG
PLL
17
26
11
EXTERNAL BUS 1

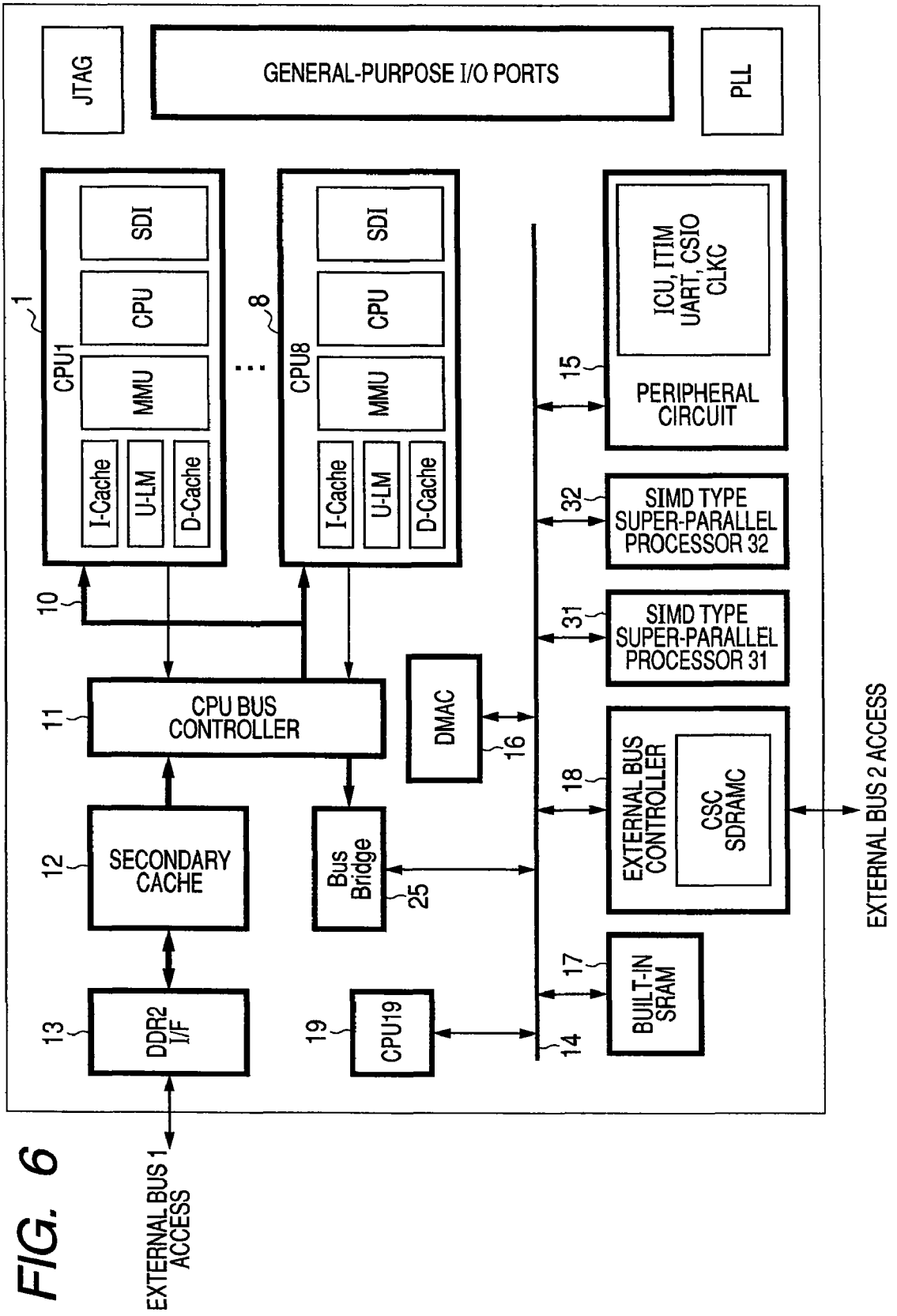

JTAG
GENERAL-PURPOSE I/O PORTS
PLL
1
CPU1
SDI
CPU
MMU
I-Cache
U-LM
D-Cache
8
CPU8
SDI
CPU
MMU
I-Cache
U-LM
D-Cache
10
11
CPU BUS CONTROLLER
12
SECONDARY CACHE
13
DDR2 I/F
EXTERNAL BUS 1 ACCESS
DMAC
16
Bus Bridge
25
19
CPU19
14
15
ICU, ITIM UART, CSIO CLKC
PERIPHERAL CIRCUIT
32
SIMD TYPE SUPER-PARALLEL PROCESSOR 32
31
SIMD TYPE SUPER-PARALLEL PROCESSOR 31
18
EXTERNAL BUS CONTROLLER
CSC SDRAMC
17
BUILT-IN SRAM
EXTERNAL BUS 2 ACCESS

FIG. 6

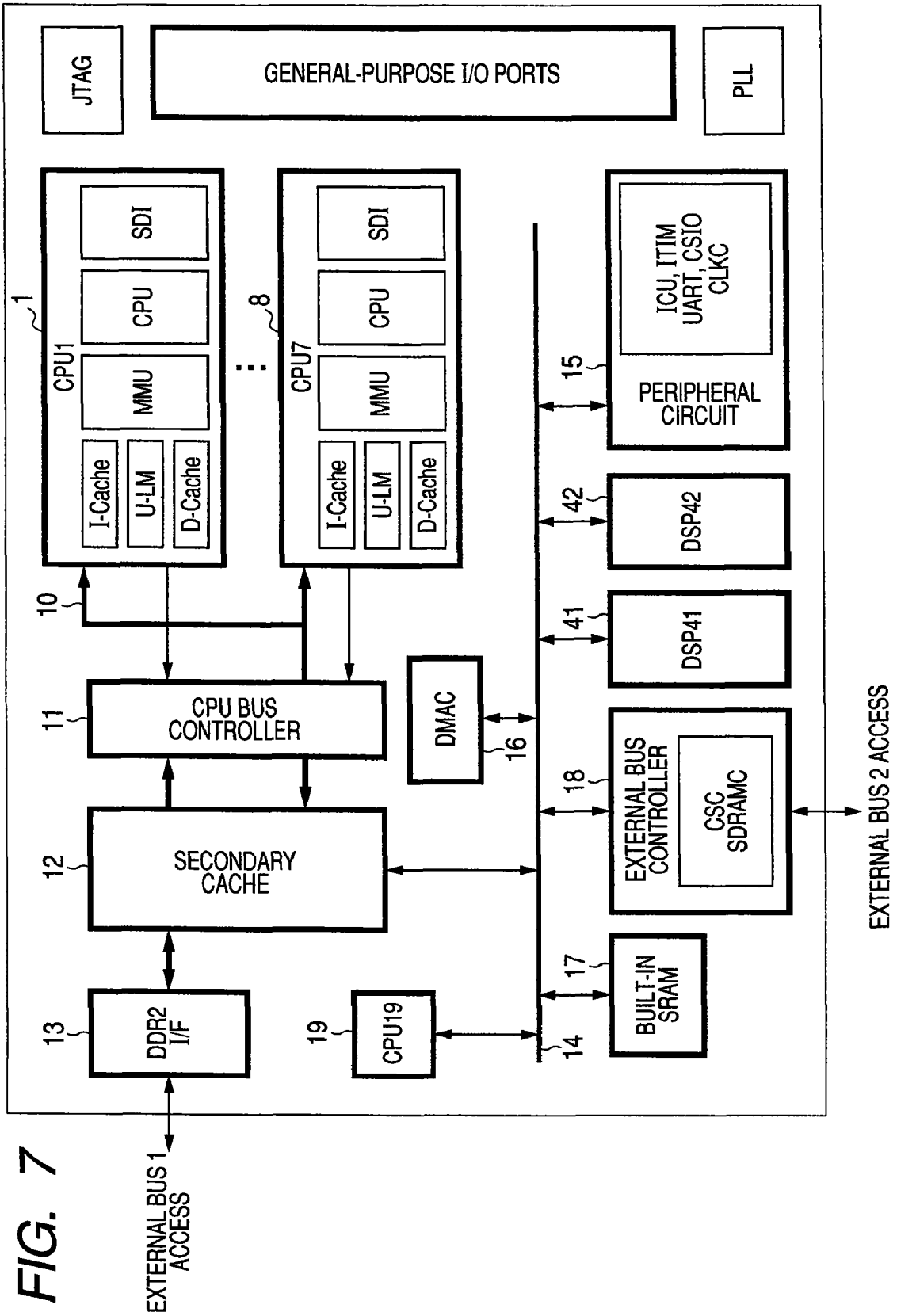

JTAG
GENERAL-PURPOSE I/O PORTS
PLL
1
CPU1
SDI
CPU
MMU
I-Cache
U-LM
D-Cache
8
CPU7
SDI
CPU
MMU
I-Cache
U-LM
D-Cache
10
11
CPU BUS CONTROLLER
12
SECONDARY CACHE
13
DDR2 I/F
EXTERNAL BUS 1 ACCESS
DMAC
16
19
CPU19
14
15
ICU, ITIM UART, CSIO CLKC
PERIPHERAL CIRCUIT
42
DSP42
41
DSP41
18
EXTERNAL BUS CONTROLLER
CSC SDRAMC
EXTERNAL BUS 2 ACCESS
17
BUILT-IN SRAM

FIG. 7

FIG. 8

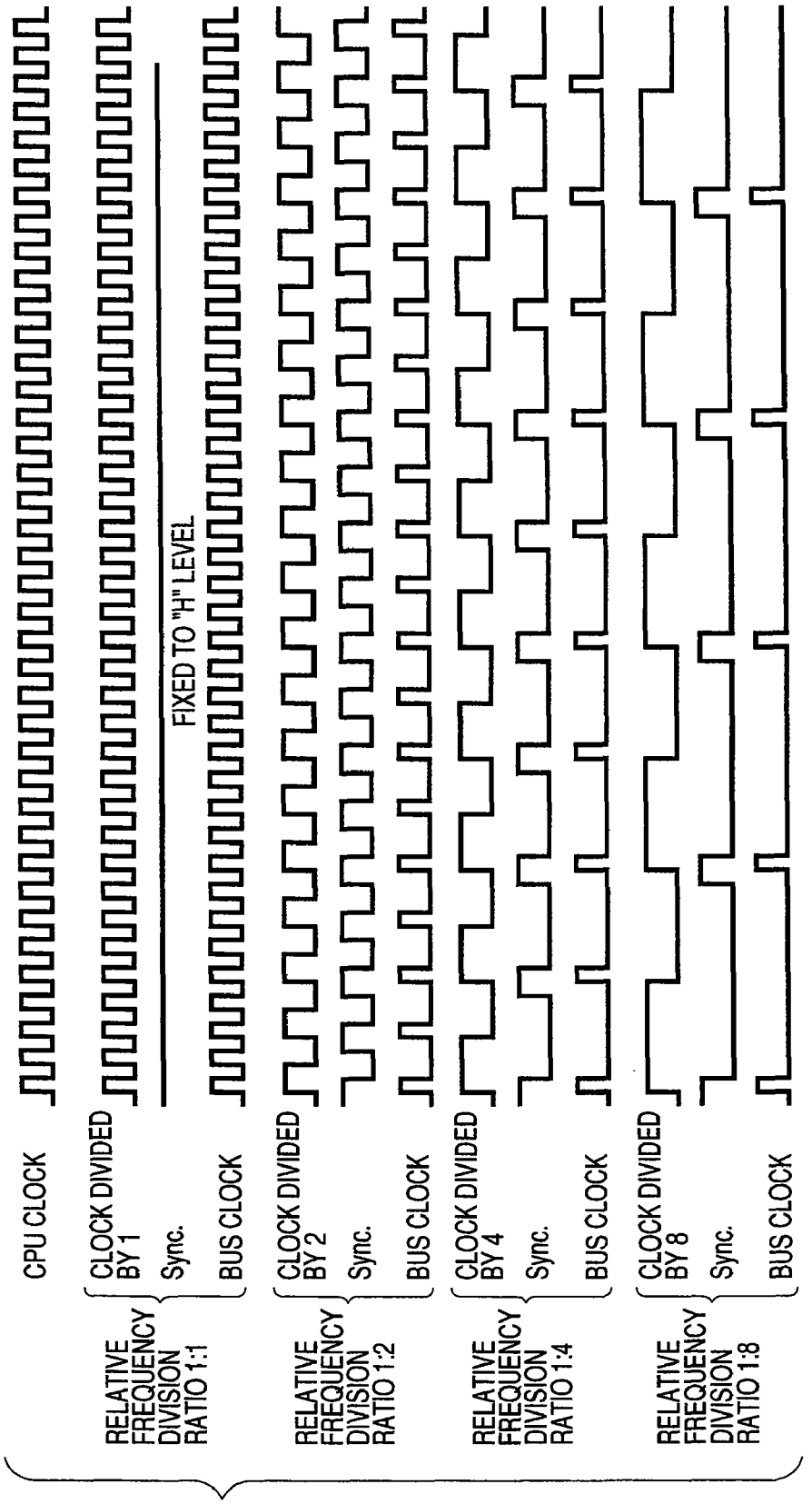

CPU CLOCK
CLOCK DIVIDED BY 1
Sync.
BUS CLOCK
FIXED TO "H" LEVEL
RELATIVE FREQUENCY DIVISION RATIO 1:1
CLOCK DIVIDED BY 2
Sync.
BUS CLOCK
RELATIVE FREQUENCY DIVISION RATIO 1:2
CLOCK DIVIDED BY 4
Sync.
BUS CLOCK
RELATIVE FREQUENCY DIVISION RATIO 1:4
CLOCK DIVIDED BY 8
Sync.
BUS CLOCK
RELATIVE FREQUENCY DIVISION RATIO 1:8

FIG. 9

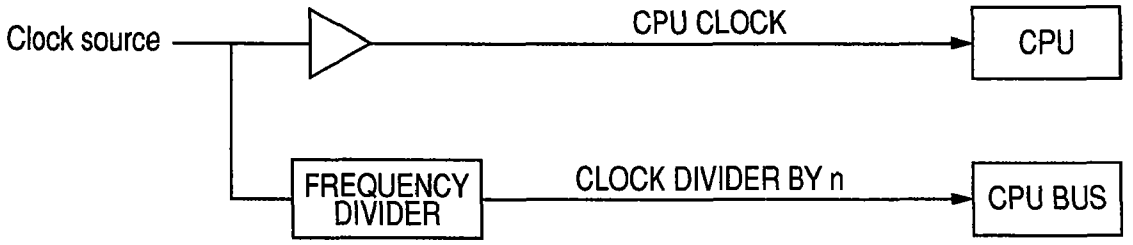

Clock source
CPU CLOCK
CPU
FREQUENCY DIVIDER
CLOCK DIVIDER BY n
CPU BUS

FIG. 10

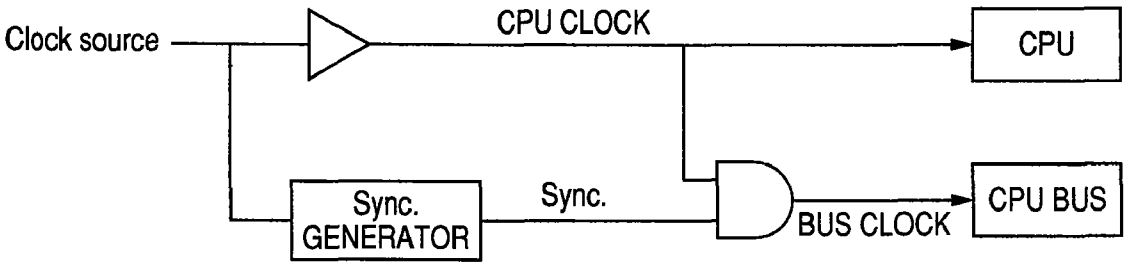

Clock source
CPU CLOCK
CPU
Sync. GENERATOR
Sync.
BUS CLOCK
CPU BUS

FIG. 11

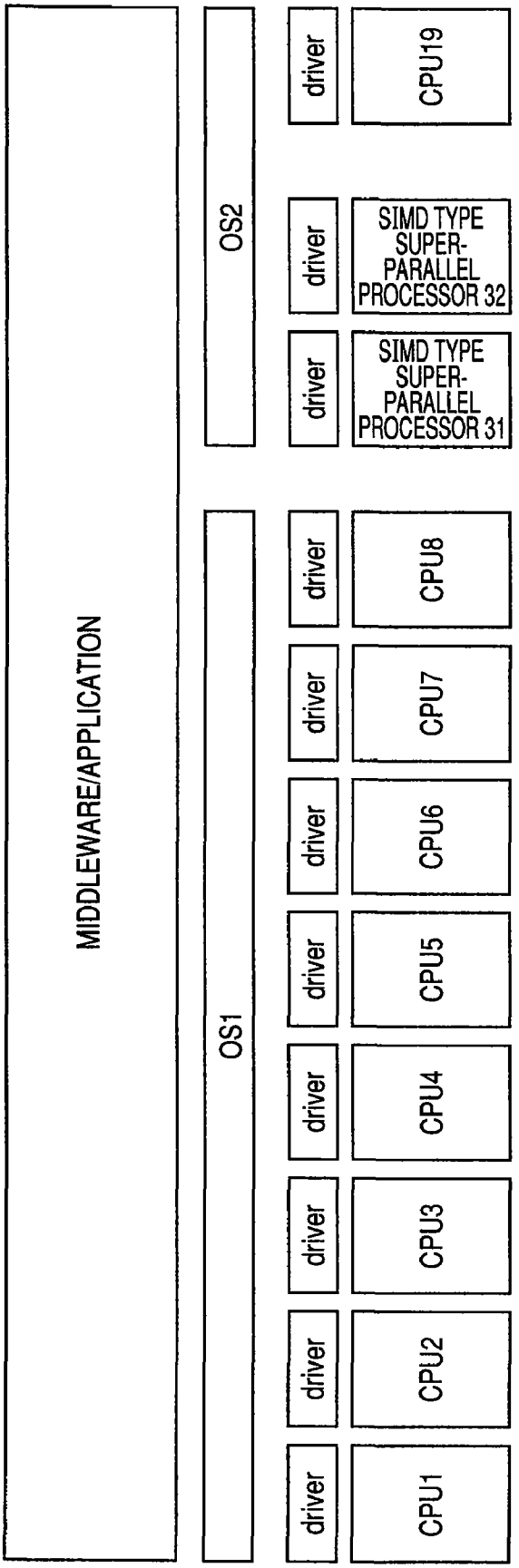
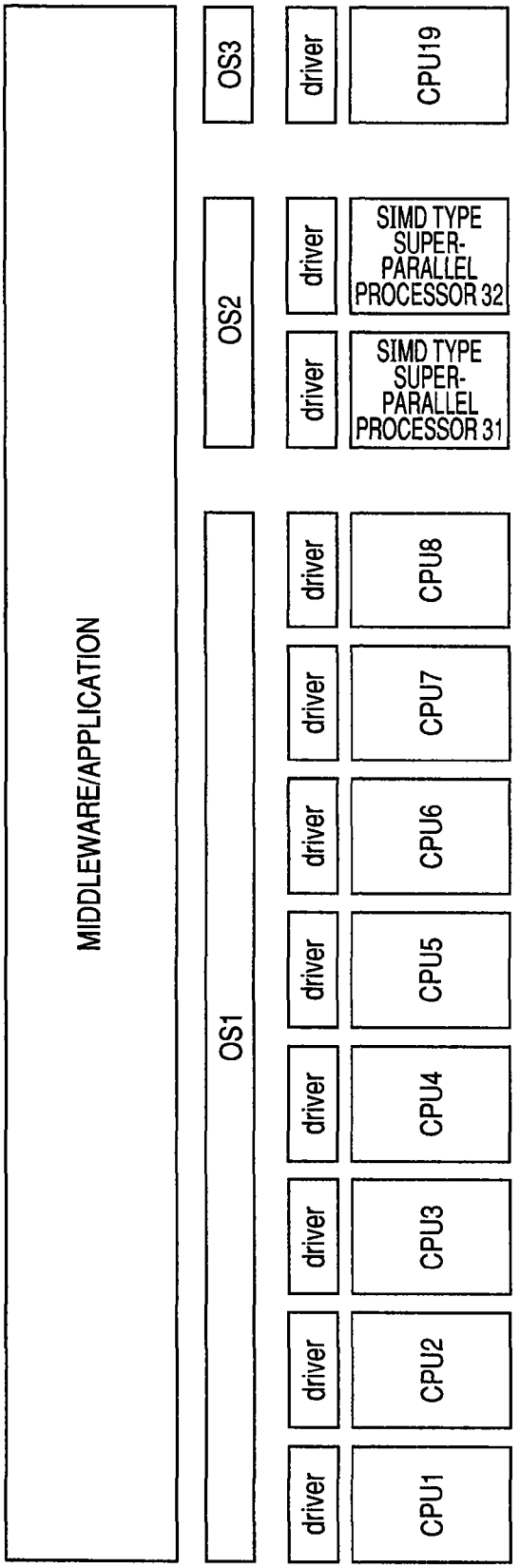

MIDDLEWARE/APPLICATION
OS1
OS2
driver
CPU1
driver
CPU2
driver
CPU3
driver
CPU4
driver
CPU5
driver
CPU6
driver
CPU7
driver
CPU8
driver
SIMD TYPE SUPER-PARALLEL PROCESSOR 31
driver
SIMD TYPE SUPER-PARALLEL PROCESSOR 32
driver
CPU19

FIG. 12


MIDDLEWARE/APPLICATION
OS1
OS2
OS3
driver
CPU1
CPU2
CPU3
CPU4
CPU5
CPU6
CPU7
CPU8
SIMD TYPE SUPER-PARALLEL PROCESSOR 31
SIMD TYPE SUPER-PARALLEL PROCESSOR 32
CPU19

MULTI-PROCESSOR DEVICE WITH GROUPS OF PROCESSORS CONSISTING OF RESPECTIVE SEPARATE EXTERNAL BUS INTERFACES

CROSS-REFERENCE TO RELATED APPLICATIONS

The disclosure of Japanese Patent Application No. 2007-11367 filed on Jan. 22, 2007 including the specification, drawings and abstract is incorporated herein by reference in its entirety

BACKGROUND OF THE INVENTION

The present invention relates to optimal bus configurations and layouts of components of a multi-processor device in which a plurality of groups of processors are implemented in a single LSI.

In multi-processor devices in which multiple processors of the same architecture and multiple processors of different architectures such as CPU and DSP are implemented over a single semiconductor chip, bus configurations as below have been used. In one configuration, all multiple processors are coupled to a single bus, as described in Non-Patent Document 1 mentioned below. In another configuration, to couple multiple processors using the same protocol to a bus, local buses are provided for each CPU and the local buses are coupled together with a bridge, as described in Non-Patent Document 2 mentioned below.

In the case where all multiple processors are coupled to a single bus, the processors are coupled to the same bus, whether the LSI multi-processor device is equipped with one external bus interface or multiple external bus interfaces.

In the case where multiple local buses are coupled together with a bridge, one processor is coupled to a local bus, the respective local buses are coupled to a single bus master, and a single bus is coupled to an external bus interface.

[Non-Patent Document 1]

Toshiba, EmotionEngine, SCE/IBM/Toshiba, Cell, Feb. 9, 2005, [searched on Jan. 9, 2007] Internet <http://ascii24.com/news/i/tech/article/2005/02/09/654178-000.html>

[Non-Patent Document 2]

Renesas, G1, February 2006, ISSCC2006 FIG. 29.5.1 "A Power Management Scheme Controlling 20 Power Domains for a Single-Chip Mobile Processor"

SUMMARY OF THE INVENTION

However, if multiple processors including different architectures are coupled to a single bus, as different-architecture processors generally differ in processing performance and speed, the following problem was posed: the operation of high-speed processors is impaired by low-speed processors and the performance of high-speed processors is deteriorated. If the multi-processor device includes CPUs and processors that are mainly for data processing, such as DSPs and SIMD type super-parallel processors, due to that DSPs and SIMD type super-parallel processors handle a large amount of data, the following problem was posed: the CPUs have to wait long before accessing the bus and the benefit of the enhanced performance of the multi-processor device is not available well.

With regard to a problem of coherency between caches, the coherency is ensured for multiple processors of the same architecture, but the cache coherency between different-architecture processors is not ensured practically and an inconsistency problem was presented.

If a multi-processor oriented OS is run, it is often enabled only for processors of the same architecture, as different-architecture processors are supplied by different developers and an OS designed for these processors is hardly made. Therefore, separate OSs must be provided for different-architecture processors. A situation where processors on which different OSs are connecting to a single bus means that the processors are coupled to a bus master IP connection which is unknown to the OSs on the same bus. A problem was posed in which enhanced performance such as scheduling of the multi-processor oriented OS is impaired.

Even when multiple local buses are coupled together with a bridge, the respective local buses are coupled to a single bus master and, therefore, a combination of a CPU and a local bus is considered as a single CPU. This posed the same problem as the above problem with the situation where different-architecture processors are connecting to the same bus.

Due to that the processors are coupled to the same bus, whether the LSI multi-processor device is equipped with one external bus interface or multiple external bus interfaces, the following problem was presented. A bus portion to which an external bus interface is coupled is blocked by a request for access to the external bus from another bus and cannot yield desired performance. A bus portion to which an external bus interface is not coupled experiences performance deterioration when access to the external bus interface from another bus occurs.

Therefore, the present invention has been made to solve the above problems and intends to provide a high-performance multi-processor device in which independent buses and external bus interfaces are provided for each group of processors of different architectures.

In one embodiment of the present invention, a multi-processor device comprises, over a single semiconductor chip, a plurality of processors including a first group of processors and a second group of processors, a first bus to which the first group of processors is coupled, a second bus to which the second group of processors is coupled, a first external bus interface to which the first bus is coupled, and a second external bus interface to which the second bus is coupled.

According to one embodiment of the present invention, when a plurality of groups of processors are implemented on a single semiconductor chip, independent buses and external bus interfaces are provided for each group of processors of different architectures. By this configuration, each group of processors can operate independently and, therefore, coordination and bus contention between processors are reduced. It is possible to realize at low cost a high-performance multi-processor system consuming low power.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a diagram showing a configuration of a multi-processor device of Embodiment 1 of the present invention.

FIG. **2** is a layout view of components of the multi-processor device in Embodiment 2 of the invention.

FIG. **3** is another layout view of the components of the multi-processor device in Embodiment 2 of the invention.

FIG. **4** is yet another layout view of the components of the multi-processor device in Embodiment 2 of the invention.

FIG. **5** is a layout view of the components of the multi-processor device in Embodiment 3 of the invention.

FIG. **6** is a diagram showing a configuration of a multi-processor device of Embodiment 4 of the invention.

FIG. **7** is a diagram showing a configuration of a multi-processor device of Embodiment 5 of the invention.

FIG. **8** is a timing chart in Embodiment 6 of the invention.

FIG. **9** is a diagram showing a clock supply circuit of prior art.

FIG. **10** is a diagram showing a clock supply circuit in Embodiment 6 of the invention.

FIG. **11** is a block diagram of software in Embodiment 7 of the invention.

FIG. **12** is a block diagram of software in Embodiment 7 of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[Embodiment 1]

FIG. **1** is a diagram showing a configuration of a multi-processor device of Embodiment 1 of the present invention. This multi-processor device is formed over a single semiconductor chip **1**. Multiple processors, namely, CPUs CPU**1** through CPU**8** are arranged in parallel (a first group of processors), making a Symmetric Multiple Processor (SMP) structure. Each CPU includes primary caches (I-cache, D-cache), a local memory (U-LM), a memory management unit (MMU), and a debugger (SDI). Eight CPUs are coupled to a CPU bus **10** (a first bus) and the CPU bus **10** is coupled to a secondary cache **12** via a CPU bus controller **11**. The secondary cache **12** is coupled to an external bus **1** via a DDR2 I/F **13** (a first external bus interface).

The CPUs operate internally at 533 MHz at maximum. The operating frequency of each CPU is converted by a bus interface inside the CPU, so that the CPU is coupled to the CPU bus **10** at 266 MHz at maximum. The secondary cache **12** and the DDR2 I/F **13** operate at 266 MHz at maximum.

The LSI device of the present invention has an internal peripheral bus **14** (a second bus) in addition to the CPU bus **10** on the same semiconductor chip. To the internal peripheral bus **14**, a peripheral circuit **15** including ICU (interrupt controller), ITIM (interval timer), UART (Universal Asynchronous Receiver Transmitter: clock asynchronous serial I/O), CSIO (clock synchronous serial I/O), CLKC (clock controller), etc., a DMAC **16** (DMA controller), a built-in SRAM **17**, SMP-structure matrix type super-parallel processors (SIMD type super-parallel processors **31**, **32**, a second group of processors), an external bus controller **18** (a second external bus interface), and a CPU **19** of another architecture are coupled. The internal peripheral bus **14** is coupled to an external bus **2** via the external bus controller **18**, thereby forming an external bus access path for connection to external devices such as SDRAM, ROM, RAM, and IO.

The internal peripheral bus **14** operates at 133 MHz at maximum and the DMAC **16**, built-in SRAM **17**, and peripheral circuit **15** also operate at 133 MHz at maximum. The SIMD type super-parallel processors operate internally at 266 MHz at maximum. The operating frequency of each super-parallel processor is converted by a bus interface inside it to couple the processor to the internal peripheral bus **14**. Likewise, the CPU **19** operates internally at 266 MHz at maximum and this operating frequency is converted by a bus interface inside it to couple it to the internal peripheral bus **14**. Because there is a difference in processing performance and speed between the processor clusters, as described above, these processor clusters are controlled using separate clocks and differ in frequency and phase.

The CPU bus **10** and the internal peripheral bus **14** are coupled through the secondary cache **12**. Therefore, the CPUs CPU**1** through CPU**8** not only can get access to the external bus **1** through the secondary cache **12** and via the DDR2 I/F **13**, but also can access resources on the internal peripheral bus **14** through the secondary cache **12**. Thus, the CPUs CPU**1** through CPU**8** can get access to another external bus **2** via the external bus controller **18**, though this path is long and the frequency of the internal peripheral bus is lower thus resulting in lower performance of data transfer. The modules that are coupled to the internal peripheral bus **14** can get access to the external bus **2** via the external bus controller **18**, but cannot get access to the external bus **1**.

The CPUs CPU**1** through CPU**8** are of the same architecture. For coherency between primary and secondary caches, the contents of the primary and secondary caches are coherency controlled so as to be consistent and there is no need to worry about malfunction of the CPUs. Even in a case where a multi-processor oriented OS is used, high performance can be delivered, because eight CPUs of the same architecture and the secondary cache **12** are only connecting to the CPU bus **10** and the external bus **1** is accessible from only the CPUs CPU**1** through CPU**8**. Especially, the SIMD type super-parallel processors operate at lower speed than the CPUs and handle a large amount of data when they process data. Consequently, these processors are liable to occupy the bus for a long time. However, this does not affect the data transfer on the CPU bus **10**, because the SIMD type super-parallel processors have access to the external bus **2** through the internal peripheral bus **14**.

From the viewpoint of the SIMD type super-parallel processors, the CPUs primarily use the path of the external bus **1** from the CPU bus **10**. Therefore, there is no need to release the internal peripheral bus **14** for the CPUs during data transfer and efficient data transfer can be performed. This effect is significant especially because of the multi-processor consisting of a plurality of CPUs. In this embodiment example of the invention, there are eight CPUs in the multi-processor device. However, in a case where **16**, **32**, or more processors share the same bus with the SIMD type super-parallel processors oriented to data processing, data processing latency occurs. If the present invention is applied to such a case, its effect will be more significant.

The CPU **19** is a small microprocessor whose operating speed and processing performance are lower than the CPUs CPU**1** through CPU**8**, but it consumes smaller power and occupies a smaller area. This CPU can perform operations such as activating the peripheral circuit **15** and checking a timer, which do not require arithmetic processing performance such as power management using CLKC. Therefore, even if the CPU **19** shares the same bus with the SIMD type super-parallel processors, it does not pose a problem in which the performance of the SIMD type super-parallel processors is deteriorated.

[Embodiment 2]

FIGS. **2** through **4** are layout views of components of the multi-processor device in Embodiment 2 of the present invention. FIG. **2** illustrates an example of layout in which the modules constituting the multi-processor device of Embodiment 1 are actually arranged over a silicon wafer. FIG. **3** presents the layout example of FIG. **2** in another view in which the modules associated to the CPU bus (CPUs CPU**1** through CPU **8** and CPU bus controller) are represented collectively as a CPU bus region **20** and the modules associated to the internal peripheral bus (SIMD type super-parallel processors **31**, **32**, CPU **19**, built-in SRAM **17**, peripheral circuit **15**, external bus controller **18**, and DMAC **16**) are represented collectively as an internal peripheral bus region **21**. FIG. **4** is a layout view in which supply voltage/GND lines **2-2** are wired.

By laying out the components of the multi-processor device as illustrated in FIG. **2**, the internal peripheral bus **14** and the CPU bus **10** can be run across shortest distances as shown. This layout enables high-speed operation with less possibility of congestion due to complicated cross wiring and hence consumes smaller die area and is less costly. In the wiring, the number of crossing signal lines other than the buses decreases and speed down due to wiring congestion and long distance wiring is not likely to occur. Hence, an LSI device with low power consumption can be realized at low cost. The device area is divided into the bus regions that are easy to control for power shutdown and the like.

There is a difference in operating frequency and arithmetic processing capability between the internal peripheral bus region **21** and the CPU bus region **20** and, consequently, these regions have different power consumptions. Low-impedance wiring is required in the CPU bus region **20** with higher clock frequency and larger power consumption. Relatively high impedance is allowable in the internal peripheral bus region **21** with lower clock frequency and smaller power consumption. Low-impedance wiring in the region with larger power consumption can be implemented by wiring of wide lines or closely spaced wiring. As adverse effect of this, wired voltage supply/GND lines **22** occupy more area in the wiring layer and wiring of other signal lines and the like is hard to do. As a result, the LSI device area increases and cost increases, and additional roundabout wiring of signal lines increases wiring capacity, which in turn increases power consumption. If these regions are scattering and mixed, low-impedance wiring has to be performed throughout the device area to ensure stable operation. However, this makes the device area larger and the cost higher.

In the layout where the device area is divided into the CPU bus region **20** with larger power consumption and the internal peripheral bus region **21** with smaller power consumption, as shown in FIG. **3**, it is solely required to apply low-impedance wiring of voltage supply/GND lines **22** only in the CPU bus region **20**. For example, wiring can be performed such that wide lines are closely spaced in the CPU bus region **20** and narrow lines are sparsely spaced in the internal peripheral bus region **21**, as shown in FIG. **4**. By doing in this way, unnecessary wiring of voltage supply lines is avoided and stable operation can be assured at low cost. Similarly, voltage supply terminals can be allocated such that voltage supply/GND terminals **23** in the CPU bus region **20** are closely spaced and voltage supply/GND terminals **23** in the internal peripheral bus region **21** are sparsely spaced.

In FIG. **4**, lines with widths drawn over each region are voltage supply or GND lines and circles at outer edges of the chip are voltage supply or GND terminals. Although a number of simulative, somewhat wide lines are drawn, a great number of extra-fine lines are wired actually. For example, in a manufacturing process for wiring of signal lines with a minimum width of 0.2 μm, 1 μm wide lines are wired at pitches of 4 μm in the CPU bus region **20** and 0.4 μm wide lines are wired at pitches of 100 μm in the internal peripheral bus region **21**. This way of wiring enables assuring stable operation, while avoiding unnecessary wiring of voltage supply/GND lines **23**. Since no external bus is coupled to the CPU bus region **20** from FIG. **1**, even this region is provided with not so large number of terminals. Application of the layout of the present embodiment can realize the multi-processor device in which adverse effects are reduced to an insignificant level.

In the present embodiment, the external bus **1** and the external bus **2** are disposed apart from each other at the top and bottom edges of the chip. Because the external bus controller **18** or the DDR2 I/F **13** has high driving capability, they consume large power and are prone to produce power-supply noise or the like. However, in the layout of the present embodiment, the external bus controller **18**, DDR2 I/F **13**, and CPUs which carry large current are disposed apart from each other. Local concentration of power does not take place and therefore heat generation is uniform throughout the chip. The external bus controller **18**, DDR2 I/F, and CPUs are sensitive to noise and temperature change. However, as they are placed apart from each other, influence of noise and heat generation on each other is reduced.

By thus disposing the modules with larger power consumption, which are sensitive to noise, apart from each other, mutual noise interference is reduced. Hence, the multi-processor device can be designed with an estimate of a smaller margin for noise. Since power consumption is uniform throughout the device and there is no local power concentration, wiring of voltage supply lines can be simplified. Besides, there is no local heat generation and the device can be designed with an estimate of a smaller margin for temperature change. Therefore, it is possible to realize at low cost the LSI device occupying a small area and consuming low power, while assuring stable operation.

[Embodiment 3]

FIG. **5** is an example of layout of the modules of the multi-processor device of Embodiment 1 configured on an actual silicon wafer. In comparison with Embodiment 2, changes are the positional relationship between the CPU bus controller module and the peripheral circuit module, the position and size of the built-in SRAM **17**, and the shapes of the CPU **19** and the secondary caches **12**.

As regards the positional relationship between the CPU bus controller module, in most cases of layout using an automatic wiring tool, buses are wired between each CPU and the CPU bus controller module as shown in FIG. **5**, not a straight bus wiring that divides the CPU region into exactly two parts as shown in FIG. **2**. In such cases, although some of the CPU buses slightly overlap with the internal peripheral bus **14**, almost the same effect as in Embodiment 2 can be obtained. It may be preferred to place the CPU bus controller module in the vicinity of the centroid of the area compassing the CPUs and the secondary caches **12** as shown in FIG. **5**. For example, the built-in SRAM **17** may be smaller than that provided in Embodiment 2 and, if the SRAM is infrequently accessed and its high operating speed is not required, its position may be changed flexibly as shown in FIG. **5**. This can make the overall device area smaller and the cost lower.

In bus wiring to the built-in SRAM **17**, a buffer circuit **24** is placed at a branch point from the internal peripheral bus **14**. Doing so can prevent a decrease in the speed of the internal peripheral bus **14** and an increase in its power consumption due to extended wiring of the internal peripheral bus **14**. Insertion of the buffer circuit **24** poses no problem, because high-speed access to the built-in SRAM **17** is not required.

[Embodiment 4]

FIG. **6** is a diagram showing a configuration of a multi-processor device of Embodiment 4 of the present invention. Differences from Embodiment 1 are described below. The CPU bus **10** and the internal peripheral bus **14** are coupled through a bus bridge **25** circuit. Therefore, the CPUs CPU**1** through CPU**8** not only can get access to the external bus **1** through the secondary cache **12** and via the DDR2 I/F **13**, but also can access resources on the internal peripheral bus **14** through the bus bridge **25**. Thus, the CPUs CPU**1** through CPU**8** can get access to another external bus **2** via the external bus controller **18**, though this path is long and the frequency of the internal peripheral bus is lower, thus resulting in lower

performance of data transfer. The modules which are coupled to the internal peripheral bus **14** can get access to the external bus **2** via the external bus controller **18**, but cannot get access to the external bus **1**. However, data obtained by access to the external bus **2** and the internal peripheral bus **14** through the bus bridge **25** is excluded from caching in the secondary cache **12**. The modules that are coupled to the internal peripheral bus **14** also can get access to the external bus **2** via the external bus controller **18** and to the external bus **1** as well through the bus bridge.

The CPUs CPU**1** through CPU**8** are of the same architecture. For coherency between the primary and secondary caches, the contents of the primary and secondary caches are coherency controlled so as to be consistent and there is no need to worry about malfunction of the CPUs. Even in a case where a multi-processor oriented OS is used, high performance can be delivered, because eight CPUs of the same architecture, the secondary cache **12**, and the bus bridge **25** are only connecting to the CPU bus **10** and the external bus **1** is mostly accessed from the CPUs CPU**1** through CPU**8**, but infrequently accessed from the modules coupled to the internal peripheral bus **14**.

Other configuration details and effects are the same as for Embodiment 1 and, therefore, description thereof is not repeated.

[Embodiment 5]

FIG. **7** is a diagram showing a configuration of a multi-processor device of Embodiment 5 of the present invention. Difference from Embodiment 1 lies in that, instead of the SIMD type super-parallel processors **31**, **32**, DSPs **41**, **42** are coupled to the internal peripheral bus. Although, in this embodiment, the secondary cache **12** acts as a bridge between the CPU bus **10** and the internal peripheral bus **14**, a dedicated bus bridge **25** may be used as in Embodiment 4. Other configuration details and effects are the same as for Embodiment 1 and, therefore, description thereof is not repeated.

[Embodiment 6]

FIG. **8** is a timing chart representing relationship between the clock of the CPUs (CPU clock) in Embodiments 1 through 5 and the CPU bus clock (bus clock). Cases where the frequency of the CPU clock is higher than the frequency of the CPU bus clock are considered. In FIG. **8**, the cases where CPU clock frequency and bus clock frequency are at ratios of 1:1, 2:1, 4:1, 8:1 are shown as examples. Clocks divided by n (n=1, 2, 4, 8) are clocks obtained by dividing the frequency of the CPU clock according to the above ratios.

In the present invention, a bus clock which is presented in FIG. **8** is used as the clock of the CPU bus **10** (see FIG. **1**), instead of a clock divided by n. A clock supply circuit, when a clock divided by n is used, is shown in FIG. **9**. A clock supply circuit, when Sync. and a bus clock are used, is shown in FIG. **10**. Both a frequency divider in FIG. **9** and a sync. generator in FIG. **10** produce outputs from CLKC input thereto. Usually, there is only a single CLKC in LSI and, hence, a clock divided by n or Sync. may be transmitted on a long path to some CPUs and actually a buffer or the like may be inserted.

When a clock divided by n and Sync. are compared, the number of times of switching (switching frequency) is the same for both, but the phase of a clock divided by n must be exactly aligned with the phase of the CPU clock, whereas this is not required for Sync. Therefore, using Sync. eliminates a need for an unnecessarily large buffer and a buffer for generating a delay which introduces inefficiency, thus making it possible to realize at low cost the LSI device occupying a small area and consuming low power.

As regards the quality of the clock of the CPU bus **10**, in the case of FIG. **9** where a clock divided by n is generated, a branch point from the CPU clock is far and the frequency divider is inserted. In the case of FIG. **10** where a bus clock is generated, a branch point from the CPU clock is near and only an AND circuit is inserted. Therefore, in the latter case, a phase difference (skew) with regard to the CPU clock can be smaller and operation at a higher frequency is enabled. To facilitate transfer between each CPU and the CPU bus **10**, no or fewer buffers for ensuring a hold are needed. Thus, it is possible to realize at low cost the LSI device occupying a small area and consuming low power.

While the relationship between the CPU clock and CPU bus clock was explained in the present embodiment, the same is true for the relationship between the clock of the SIMD type super-parallel processors and the clock of the internal peripheral bus **14** as well as the relationship between the clock of the CPU **19** and the clock of the internal peripheral bus **14**.

[Embodiment 7]

FIG. **11** is a block diagram of software for a system using the multi-processor device according to any of Embodiments 1 through 6. The software structure includes device drivers (drivers) for each processor and OSs at a layer on top of the driver layer. OS**1** is responsible for control of the CPUs CPU**1** through CPU**8** and OS**2** for control of the SIMD type super-parallel processors **31**, **32** and the CPU **19**. It is conceivable that one OS, for example, OS**1** is non-realtime OS such as Linux and the other OS**2** is realtime OS such as ITRON. OS**1** is optimized for CPU architecture and eight CPUs of the same architecture, the secondary cache **12**, and the bus bridge **25** are only connecting to the CPU bus **10**. High performance can be delivered, because the external bus **1** is mostly accessed from the CPUs CPU**1** through CPU**8**, but infrequently accessed from the modules coupled to the internal peripheral bus **14**. The contents of the primary and secondary caches are coherency controlled by OS**1** so as to be consistent and the coherency problem can be coped with optimally. Meanwhile, the OS**2** side has the external bus **2** independently of OS**1** and, therefore, there is almost no need for coordination for resources with OS**1**, and high performance can be delivered.

FIG. **12** shows another software structure including an additional OS**3** for CPU**12**. In addition to the effects described for FIG. **11**, this software structure is more efficient, as each OS is dedicated to governing the processors or processor of the same architecture.

What is claimed is:

1. A multi-processor device comprising, over a single semiconductor chip:

a plurality of processors including a plurality of a first type of processors and a plurality of a second type of processors, each said first type of processor having a first architecture, and each said second type of processor having a second architecture which is different from the first architecture of said first type of processor;

a first bus to which the plurality of the first type of processors is coupled;

a second bus to which the plurality of the second type of processors is coupled;

a first external bus interface to which the first bus is coupled;

a second external bus interface to which the second bus is coupled; and

a secondary cache over the single semiconductor chip that couples the first bus and the second bus to each other,

wherein said first bus has a first maximum operating frequency, and said second bus has a second maximum operating frequency different from said first maximum operating frequency,

wherein, in plan view, the first external bus interface is disposed at a first edge of the single semiconductor chip and the second external bus interface is disposed at a second edge of the single semiconductor chip different from said first edge,

wherein said secondary cache is located between the first bus and the first external bus interface, or between the second bus and the second external bus interface, and

wherein the plurality of the first type of processors and the plurality of the second type of processors are disposed separately in a layout region which includes the first bus and the plurality of the first type of processors and a layout region which includes the second bus and the plurality of the second type of processors, over the single semiconductor chip in plan view.

2. The multi-processor device according to claim **1**, further comprising a bus bridge circuit that couples the first bus and the second bus.

3. The multi-processor device according to claim **1**, wherein the first type of processor is a Central Processing Unit (CPU) and the second type of processor is a matrix type processor.

4. The multi-processor device according to claim **3**, wherein a CPU of another architecture is also coupled to the bus to which the matrix type processors are coupled.

5. The multi-processor device according to claim **1**, wherein the first type of processor is a Central Processing Unit (CPU) and the second type of processor is a Digital Signal Processor (DSP).

6. The multi-processor device according to claim **1**, wherein the plurality of the first type of processors and the plurality of the second type of processors are controlled with separate clocks which differ in frequency or phase.

7. The multi-processor device according to claim **1**, wherein, of the plurality of the first type of processors and the plurality of the second type of processors, the region of the plurality of the first type of processors is controlled with a high frequency clock and has closely spaced wiring of voltage supply lines, and the region of the plurality of the second type of processors is controlled with a low frequency clock and has sparse wiring of voltage supply lines.

8. The multi-processor device according to claim **1**,

wherein, of the plurality of the first type of processors and the plurality of the second type of processors, the region of the plurality of the first type of processors is controlled with a high frequency clock, and the region of the plurality of the second type of processors is controlled with a low frequency clock, and

wherein the region of the first type of processors has a larger number of voltage supply terminals than the region of the second type of processors.

9. The multi-processor device according to claim **1**, wherein, the CPU region and the external bus interface of the plurality of the first type of processors which are controlled with a high frequency clock, of the plurality of the first type of processors and the plurality of the second type of processors, are disposed far apart from each other over the single semiconductor chip.

10. The multi-processor device according to claim **9**, wherein a high rate clock is supplied to the CPUs in the plurality of the first type of processors controlled with the high frequency clock, and a clock for the bus to which the external bus interface and processors for data processing are coupled is generated by gating a part of the clock.

11. The multi-processor device according to claim **1**, wherein the plurality of the first type of processors and the plurality of the second type of processors operate using different operating systems.

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