Low-power High-speed Level Shifter Design for Block-level Dynamic Voltage Scaling Environment

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Abstract

Two novel level shifters that are suitable for block-level dynamic voltage scaling environment (namely, V_{DD}-hopping) are proposed. In order to achieve reduction in power consumption and delay, the first proposed level shifter which is called Contention Mitigated Level Shifter (CMLS) uses a contention-reduction technique. The simulation results with 65-nm CMOS model show 24% reduction in power and 50% decrease in delay with 4% area increase compared with the conventional level shifter. The second proposed level shifter which is called Bypassing Enabled Level Shifter (BELS) implements a bypass function and it is fabricated using 0.35μm CMOS technology. The measurement results show that the power and delay of the proposed BELS are reduced by 50% and 65%, respectively with 60% area overhead over the conventional level shifter.

Introduction

Power dissipation, especially leakage power, has become one of the most important design metrics in the deep submicron era. Dynamic Voltage Scaling (DVS) or V_{DD}-hopping [1] is an effective technique that reduces not only dynamic power but also leakage power. A logic-swing level shifter is a key circuit component in the DVS implementation because even for a chip-level DVS system, I/O blocks are operated under fixed V_{DD} and consequently level shifters are required between core circuits and I/O circuits. When the V_{DD}-hopping technique is applied on a "block level" as shown in Figure 1, each block on a chip could be operated under either high V_{DD} (V_{DDH}) or low V_{DD} (V_{DDL}). Thus, voltage level shifters are needed among blocks in order to avoid static crowbar current at a receiver side.

Several level shifters have been proposed for use in I/O blocks [2] and in multi-V_{DD} technology [3]. Since these level shifters have a contention problem, the delay and power at low voltage becomes larger and they are not suitable for use with V_{DDL}. In this paper, the design of novel level shifters is described. The advantage of the proposed level shifters is verified by simulation and measurement.

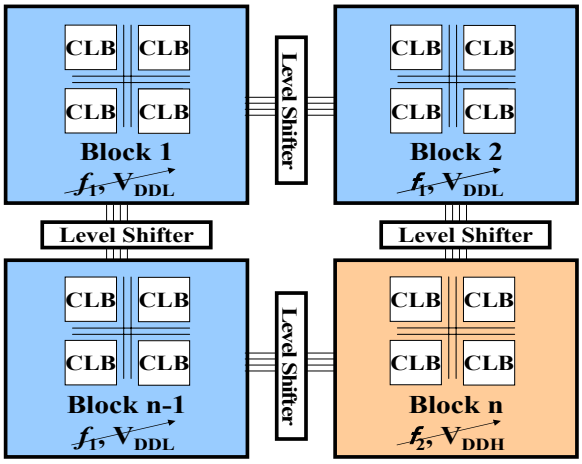

Figure 1 Block-level V_{DD}-hopping

Novel Level Shifter Design

The conventional level shifter is shown in Figure 2(a). The two PMOS transistors MP1 and MP2 act as a swing-restoring load. Assuming that initially input signal, IN, is "L", MN1 is turned on and provides a conducting path to ground while MN2 is cut off. Therefore, node A is pulled down to ground, which makes MP2 on and node B is pulled up to "H". Thus, the output signal, OUT, becomes "L". The operation reverses when the input signal, IN, is switched to "H".

This conventional level shifter has large delay because it suffers from contention between the pull-down transistors (MN1 and MN2) and the pull-up transistors (MP1 and MP2). The contention problem gives rise to the increase in both delay and power consumption. In particular, when the low voltage, V_{DDL}, changes, the problem of contention gets severer because we can not get rid of the contention in both cases where V_{DDL} is relatively high and low by proper sizing of transistors. Figure 2(b) shows the first proposed level shifter, namely Contention Mitigated Level Shifter (CMLS).

In the CMLS, the above-mentioned contention is reduced, since MN1 and MP3 (MN2 and MP4) comprise a quasi-inverter. Therefore the logical values of node A and B are established faster than that of the conventional level shifter. Thus the delay of CMLS is less than that of the conventional level shifter. The power consumption of the CMLS is reduced compared with that of the conventional level shifter, because the contention reduction also brings in the crowbar current reduction.

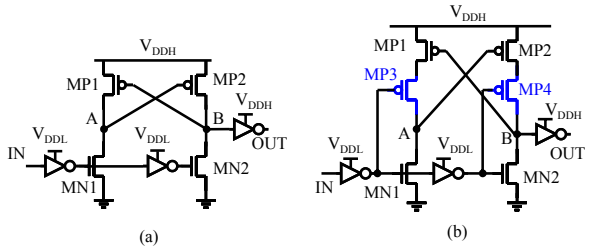

Figure 2 (a) Conventional level shifter. (b) Contention mitigated level shifter (CMLS).

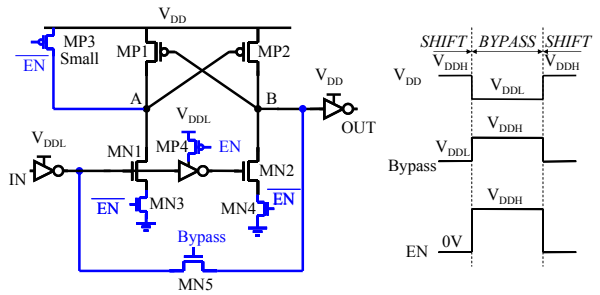

Figure 3 Bypassing enabled level shifter (BELS). The waveforms of the signals Bypass and EN are also shown.

In the block-level V_{DD}-hopping scheme, V_{DD} in one block is changed according to the performance needed for the block and it is known that for most of the multimedia applications, the blocks are operated at V_{DDL} for most of the time. Therefore, the speed and power at V_{DDL} is very important. If the speed of shifter is faster in low-V_{DD} environment, the V_{DDL} can be reduced more aggressively, which in turn reduces power consumption further.

Figure 3 shows the second proposed level shifter, namely a Bypassing Enabled Level Shifter (BELS). Two PMOS and three NMOS transistors are added to the conventional shifter. The BELS has two operation modes: *"SHIFT"* mode and *"BYPASS"* mode. When the output voltage V_{DD} is high, that is, V_{DDH}, the BELS is in a *"SHIFT"* mode. In the *"SHIFT"* mode, by setting the Bypass signal to V_{DDL}, the contention at node B will be reduced and the logic value of node B is established faster. Therefore, the delay is less than the case of Bypass signal being set to 0V. When the V_{DD} is low voltage, V_{DDL}, the shifting function is not required and the BELS is switched to *"BYPASS"* mode. In the *"BYPASS"* mode, signal EN is set to V_{DDH} to cut off used transistors. Because the Bypass signal is set to V_{DDH} in the *"BYPASS"* mode, MN5 can pass through signal without threshold voltage loss (Assuming that $V_{DDH} > V_{DDL} + V_{TH}$).

Simulation and Measurement Results

(A) Contention Mitigated Level Shifter (CMLS)

Figure 4 shows the simulated delay of the conventional level shifter and the CMLS. The BPTM (Berkeley predictive technology model) for 65-nm CMOS, where V_{DD} of 0.7V and V_{TH} of 0.1V, are assumed [4]. When V_{DDH} is set to 0.7V and V_{DDL} is varied, the delay of the CMLS is always less than that of the conventional level shifter. The difference between the delay of the CMLS and that of the conventional level shifter becomes larger as V_{DDL} lowers. The reason is that the contention of the conventional level shifter becomes greater than the contention of the CMLS, especially at low voltage region. At V_{DDL} = 0.3V, the delay of the CMLS is 307ps, which is a half of delay of the conventional level shifter of 617ps.

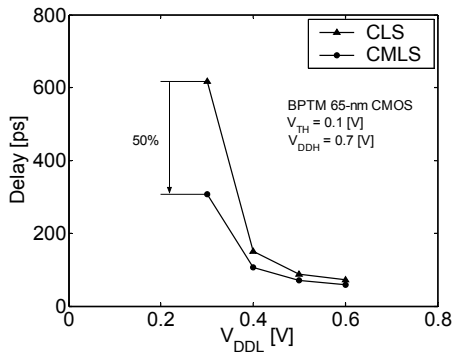

Figure 4 Simulated delay of the conventional level shifter and the CMLS when V_{DDL} is varied and V_{DDH} is fixed. The CLS stands for conventional level shifter. The BPTM 65-nm CMOS model is used.

Figure 5 shows the simulated power consumption of the conventional level shifter and the CMLS. Although two PMOS transistors are added, the CMLS still has the advantage in power compared with the conventional level shifter. This is because the contention problem in the CMLS has been mitigated and crowbar current flows when there is the contention. For a typical CMOS gate, the dynamic power decreases in proportion to the square of the supply voltage. In case of the level shifter, the dynamic power is not only

simply proportional to the square of the supply voltage, but also depends on the contention. Therefore, even if the voltage is reduced, the power consumption is not decreased because the contention becomes severer. At V_{DDL} of 0.3V, the power consumption of the CMLS is 0.29μW, which is 24% smaller than that of the conventional level shifter.

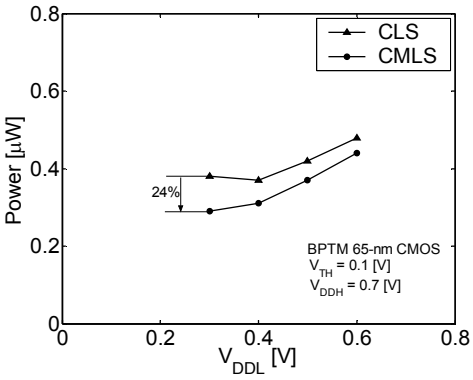

Figure 5 Simulated power consumption of the conventional level shifter and CMLS when V_{DDL} is varied and V_{DDH} is fixed. The CLS stands for conventional level shifter. The BPTM 65-nm CMOS model is used. The area overhead of the CMLS is estimated at a value of 4%.

Since MP1 and MP3, or MP2 and MP4 are in off-off states, leakage current of the CMLS is reduced compared with that of the conventional level shifter. At V_{DDH}=0.7V and V_{DDL}=0.3V, the leakage current of the CMLS is 79nA, which is 72% of leakage current of the conventional level shifter of 109nA.

(B) Bypassing Enabled Level Shifter (BELS)

The conventional level shifter and the BELS have been fabricated using the 0.35μm CMOS process. Figure 6 shows the delay of the conventional level shifter and the BELS when V_{DD} = V_{DDH}, that is "*SHIFT*" mode. By setting the Bypass signal to V_{DDL}, the contention is reduced somewhat, but because the adding some transistors increases the capacitance, the delay of the BELS is almost the same as that of the conventional level shifter.

When V_{DD} = V_{DDL}, the BELS is in the "*BYPASS*" mode. Since the signal is passed through MN5, the contention problem does not occur in the BELS. Thus, the delay of BELS is improved. From Figure 7, when V_{DDL} = 1V, the delay of the BELS is reduced by 65%.

Figure 8 shows the power consumption of the conventional and proposed level shifter when V_{DD} = V_{DDL}. In the "*SHIFT*" mode, the BELS power is slightly higher than the conventional level shifter. This is because addition of the extra transistors increases capacitance.

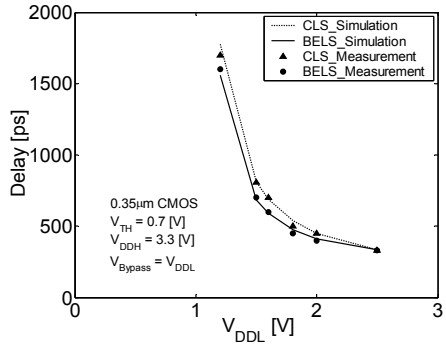

Figure 6 Delay of the conventional and proposed level shifter when output voltage V_{DD} = V_{DDH}. The CLS stands for conventional level shifter.

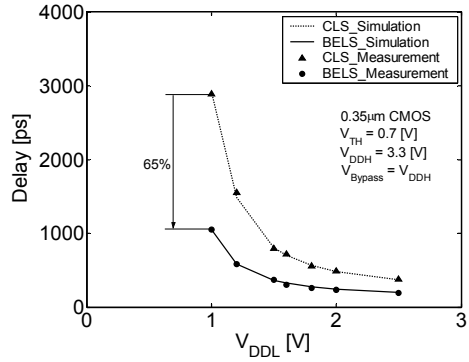

Figure 7 Delay of the conventional and proposed level shifter when the output voltage V_{DD}=V_{DDL}. The CLS stands for the conventional level shifter.

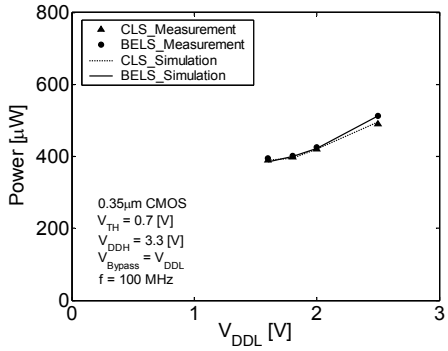

Figure 8 Power of the conventional and proposed level shifter when output voltage V_{DD} = V_{DDH}. The CLS stands for conventional level shifter.

From Fig. 9, in the "*BYPASS*" mode, the power consumption of the BELS is reduced to a half. There are two factors that reduce the power consumption of the BELS. The first one is that the contention problem is eliminated. The second factor is that transistors that are not in operation are cut off, which

results in reduction of dynamic charging and discharging current.

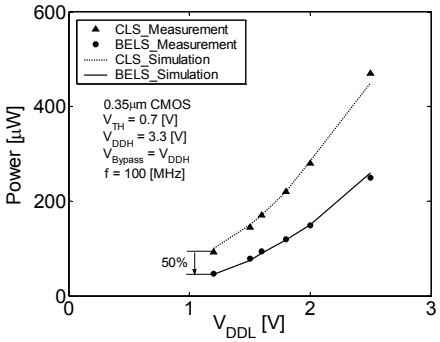

Figure 9 Power of the conventional and proposed level shifter when output voltage V_{DD}=V_{DDL}. CLS stands for conventional level shifter.

Figure 10 shows the schematics and microphotographs of the level shifter ring oscillators and level shifter chain for delay and power measurements. The delay and power of the inverters are measured using another inverter ring oscillator and inverter chain fabricated elsewhere on the same chip.

The area overhead of the BELS is 60% as a shifter cell but for the overall area overhead at a chip level will be less than a percent since the level shifters occupy less than a few percent of a chip area. The leakage current of the BELS is 56nA, which is 51% of leakage current of the conventional level shifter which is 109nA.

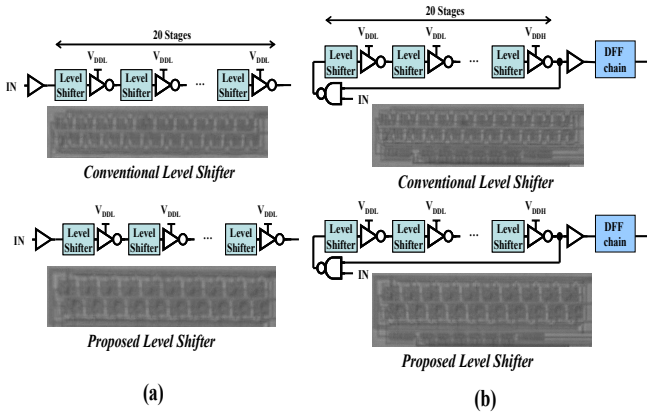

Figure 10 (a) Schematics and microphotographs of level shifter chains for power measurement. (b) Schematics and microphotographs of level shifter ring oscillators for delay measurement.

SUMMARY

Two level shifters for bock-level V_{DD}-hopping, namely Contention Mitigated Level Shifter (CMLS) and Bypass Enabled Level Shifter (BELS) are proposed. In the CMLS, by adding two extra PMOS transistors, the contention between the pull-up PMOSFET's and pull-down NMOSFET's becomes less and thus the operation margin, especially when input voltage swing is small, is improved as well as the delay and the power. When the input voltage V_{DDL} is 0.3V, the delay and power consumption of the CMLS are reduced by 50% and 24% respectively, compared with the conventional level shifter. The area overhead of the CMLS is estimated to be 4%. Leakage current of the CMLS is 72% of that of the conventional level shifter.

The second proposed level shifter, BELS, has a bypass function that passes through a signal through a transfer gate when both of the input and output are V_{DDL}, which often occurs in V_{DD}-hopping environment. With this bypass function, the simulation and measurement results show that the delay and power consumption of the proposed level shifter are reduced by 65% and 50%, respectively. The area overhead is 60% as a shifter itself but the overall area overhead at a chip level will be less than a percent. Leakage current of the BELS is 51% of that of the conventional level shifter.

ACKNOWLEDGEMENT

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