

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NXP USA, INC. and QUALCOMM INCORPORATED.,
Petitioner,

v.

REDSTONE LOGICS LLC,
Patent Owner.

Case IPR2025-00485
Patent 8,549,339

**PATENT OWNER'S REQUEST FOR DISCRETIONARY DENIAL OF
INSTITUTION**

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	OVERVIEW OF THE '339 PATENT	1
III.	DENIAL OF INSTITUTION UNDER §314 IS WARRANTED.....	3
	A. <i>Fintiv</i> Factor 1: The district court has not granted a stay, nor is there any evidence that a stay will be granted.	4
	B. <i>Fintiv</i> Factor 2: The district court trial will occur more than three months before the deadline for a final written decision in this proceeding.....	6
	C. <i>Fintiv</i> Factor 3: By the time an institution decision is reached, the Court will have held the <i>Markman</i> hearing and fact discovery will be nearing completion.....	8
	D. <i>Fintiv</i> Factor 4: There is substantial overlap between this IPR and the district court proceeding.	10
	E. <i>Fintiv</i> Factor 5: Petitioner is a defendant in the district court litigation.	14
	F. <i>Fintiv</i> Factor 6: Other circumstances weigh strongly against institution, including the weakness of the Petition and Petitioner's delay.....	14
IV.	The PTAB Workload Management Factors Weigh Against Institution	15
	A. Prior Adjudication.....	16
	B. No Changes in the Law Support Reconsideration of Validity.....	21
	C. The Petition is Particularly Weak and Overly Reliant on Unreliable Expert Testimony.....	22
	D. The Patent Has Been In Force As Long As The IPR Regime	30
	E. Significant Weakness on Other Discretionary Denial Regime Also Favors Denial.....	31

V.	CONCLUSION	31
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TABLE OF AUTHORITIES

Cases

<i>Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH,</i> IPR2019-01469, Paper 6 (Feb. 13, 2020)	18, 19
<i>Apple Inc. v. Fintiv, Inc.,</i> IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020)	passim
<i>Apple Inc. v. Fintiv, Inc.,</i> IPR2020-00019, Paper 15 (PTAB May 13, 2020).....	3, 8, 14
<i>BOE Tech. Grp. Co. v. Element Capital Commercial Co.,</i> IPR2023-00808, Paper 9 (PTAB Nov. 15, 2023)	7, 9
<i>Datanet LLC v. Dropbox Inc.,</i> No. 622CV01142OLGDTG, 2023 WL 9005604 (W.D. Tex. Dec. 28, 2023)	5
<i>EClinicalWorks, LLC v. Decapolis LLC,</i> IPR2022-00229, Paper 10 (PTAB Apr. 13, 2022).....	7, 10
<i>Facebook v. Windy City Innovations, LLC,</i> 973 F.3d 1321 (Fed. Cir. 2020).....	28
<i>Ingenico Inc. v. IOENGINE, LLC,</i> No. 2023-1367, 2025 WL 1318188 (Fed. Cir. May 7, 2025)	11
<i>Intel Corp. v. PACT XPP Schweiz AG,</i> 61 F.4th 1373 (Fed. Cir. 2023)	28
<i>Motorola Solutions, Inc. v. Stellar, LLC,</i> IPR2024-01205, Paper 19 (PTAB Mar. 28, 2025)	11
<i>Multimedia Content Mgmt. LLC v. Dish Network L.L.C.,</i> No. 6:18-CV-00207-ADA, 2019 WL 11706231 (W.D. Tex. May 30, 2019)	5
<i>NHK Spring Co. v. Intri-Plex Techs., Inc.,</i> IPR2018-00752, Paper 8 (PTAB Sept. 12, 2018).....	3
<i>NXP USA, Inc. v. Impinj, Inc.,</i> PGR2022-00005, Paper 20 (PTAB Aug. 25, 2022).....	8
<i>Pharaoh Energy Servs., LLC v. Flex-Chem Holding Co.,</i> IPR2024-00815, Paper 7 (PTAB Sept. 20, 2024).....	10

IPR2025-00485 Request for Discretionary Denial
U.S. Patent No. 8,549,339

<i>Roku, Inc. v. IOEngine, LLC</i> , IPR2022-01551, Paper 11 (PTAB May 5, 2023).....	7, 9
<i>Samsung Elecs. Co. v. Mojo Mobility Inc.</i> , IPR2023-01094, Paper 11 (PTAB Feb. 9, 2024)	7, 9
<i>Smart Mobile Techs. LLC v. Samsung Elecs. Co.</i> , No. 6:21-CV-00701-ADA, 2023 WL 11999028 (W.D. Tex. Oct. 24, 2023).....	5
<i>Vector Flow, Inc. v. HID Global Corp.</i> , IPR2023-00353, Paper 8 (PTAB July 17, 2023)	7, 10
<i>Xerox Corp. v. Bytemark, Inc.</i> , IPR2022-00624, Paper 9 (PTAB August 24, 2022)	27

Statutes

35 U.S.C. § 102	13
35 U.S.C. § 103	13
35 U.S.C. § 112	16
35 U.S.C. § 314(a).....	3, 31
35 U.S.C. § 325(d).....	16, 18, 21, 31

Other Authorities

37 C.F.R. § 42.100(c).....	6
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PATENT OWNER’S EXHIBIT LIST

No.	Description
Ex. 2001	<i>Redstone v NXP USA, Inc.</i> , No. 7:24-cv-00028 ADA-DTG, Dkt. No. 36 Scheduling Order
Ex. 2002	<i>Redstone v Qualcomm, Inc., Qualcomm Technologies, Inc.</i> , No. 7:24-cv-00231 ADA, Dkt. No. 24 Scheduling Order
Ex. 2003	Motion to Stay before Judge Albright, Docket Navigator
Ex. 2004	Guidance on USPTO’s recission of “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation”
Ex. 2005	Western District of Texas Case Management Statistics
Ex. 2006	Excerpts of NXP’s Preliminary Invalidity Contentions
Ex. 2007	Excerpts of NXP’s Amended Invalidity Contentions
Ex. 2008	Excerpts of Qualcomm’s Invalidity Contentions
Ex. 2009	Exhibit B to NXP’s Amended Invalidity Contentions
Ex. 2010	Exhibit B to Qualcomm’s Invalidity Contentions
Ex. 2011	3/26/2025 email from Eric Green, Redstone Logics LLC v. NXP USA, Inc., Case No. 7:24-cv-00028-ADA-DG, in the United States District Court for the Western District of Texas
Ex. 2012	3/26/2025 Email from Daniel Leventhal, Redstone Logics LLC v. Qualcomm Incorporated, et al., Case No. 7:24-cv-00231-ADA, in the United States District Court for the Western District of Texas
Ex. 2013	Interim Processes for PTAB Workload Management
Ex. 2014	<i>Redstone v NXP USA, Inc.</i> , No. 7:24-cv-00028 ADA-DTG, Dkt. No. 50 Claim Construction Order
Ex. 2015	<i>Redstone v MediaTek Inc., et al</i> , No. 7:24-cv-00029 ADA-DTG, Dkt. No. 40 Claim Construction Order
Ex. 2016	Intentionally Omitted
Ex. 2017	US Patent No. 7,853,808 to Kim et al (“’808 Kim”)
Ex. 2018	US Patent Publication No. 2009/0138737 to Kim et al (“Kim”)

IPR2025-00485 Request for Discretionary Denial
U.S. Patent No. 8,549,339

No.	Description
Ex. 2019	US Patent Publication No. 2009/0106576 to Jacobowitz et al (“Jacobowitz”)
Ex. 2020	3/31/2025 Email from Joshua Scheufler, Re: Redstone Logics LLC v. Qualcomm Incorporated, et al., Case No. 7:24-cv-00231-ADA, in the United States District Court for the Western District of Texas
Ex. 2021	4/20/2025 Email from Daniel Leventhal, Re: Redstone Logics LLC v. Qualcomm Incorporated, et al., Case No. 7:24-cv-00231-ADA, in the United States District Court for the Western District of Texas
Ex. 2022	<i>MediaTek, Inc. et al v Redstone Logics LLC</i> , IPR2025-00085, Paper 7 (April 22, 2025)
Ex. 2023	NXP Motion to Stay Pending Settlement
Ex. 2024	MediaTek Motion to Stay Pending Settlement
Ex. 2025	Crouch Dennis. “Reference Recycling and the Case for Sua Sponte Rehearing in Igenico”
Ex. 2026	Crouch, Dennis. “Estoppel Gutted: A Pelican’s Guide to Patent Litigation.”

I. INTRODUCTION

The Director should deny institution of *inter partes* review (“IPR”) of U.S. Patent No. 8,549,339 (“the ’339 patent”) under her discretion under *Fintiv* and more generally under §314. Trial against Qualcomm¹ is set for several months prior to the deadline for a Final Written Decision and the Petition’s grounds are too weak, propped up by unreliable expert testimony or have been already considered by the office, to justify the expenditure of the Board’s limited resources.

II. OVERVIEW OF THE ’339 PATENT

At a high level, the ’339 Patent is directed to a novel operation of a multi-core processor enabling coordination of groups of multiple cores operating at different supply voltages and clock signals. *See* Ex. 1001 at 2:4–3:15.

The ’339 Patent explains: a “multi-core processor [] may be divided into stripes... [where e]ach stripe may be associated with an independent power profile ... and/or may be associated with an independent clock domain defined by a clock signal received from a clock control block.” *Id.* at 2:25–31. However, “[t]o maintain the limited differential relationship discussed above, adjusting the supply voltage to one stripe may involve adjusting the supply voltages to the other stripes.” *Id.* at 3:8–10.

¹ The district court action against NXP has been stayed pending settlement. Ex. 2023.

To address this, the '339 Patent describes an architecture to achieve this wherein “the stripe [] may be powered by a supply voltage received from a power control block[] and/or may be associated with an independent clock domain defined by a clock signal received from a clock control block[].” *Id.* at 2:26–31.

This solution to the prior art problem of dynamic management of sets of processor cores is reflected, for example, in claim 1 of the '339 Patent, which recites:

1. A multi-core processor, comprising:
a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input;
a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and
an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.

Ex. 1001 at claim 1.

All challenged dependent claims, claims 2-3, 5, 8, 10-11, and 14, depend from

claim 1 and claim 21 reads similarly to claim 1.

III. DENIAL OF INSTITUTION UNDER §314 IS WARRANTED.

35 U.S.C. § 314(a) gives the Director discretion to deny institution of IPR due to the advanced state of parallel district court litigation regarding the same issues. *See NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 19-21 (PTAB Sept. 12, 2018) (precedential) (“*NHK*”). The Board has set forth six factors for determining whether discretionary denial in light of such parallel litigation is appropriate, and in analyzing them, “takes a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5-6 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv I*”); *see also Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 at 7-17 (PTAB May 13, 2020) (informative) (“*Fintiv II*”).

Each of these six *Fintiv* factors weigh in favor of the Board exercising its discretion to deny institution here. For Factor 1, no stay of the parallel district court litigation in favor of this IPR has been granted or requested, and such a stay is unlikely given the advanced stage of the case. For Factor 2, the district court trial will occur three months before the deadline for a final written decision in this proceeding. For Factor 3, largely due to Petitioner’s delay in filing the Petition, there will be much investment by the parties and the district court—by the time the Board issues its institution decision, the *Markman* hearing will have occurred, and fact

discovery will be nearing completion. For Factor 4, there is substantial overlap in both the patent claims and art at issue in this proceeding and in the district court, and Petitioner's *Sotera* stipulation does not quell the concerns of inefficiency and inconsistent rulings. For Factor 5, Petitioners are defendants in the parallel litigations. And for Factor 6, not only did Petitioners unduly delay in filing the Petition, but the Petition fails to present a compelling challenge on the merits. Each of these factors is addressed in more detail below.

A. *Fintiv* Factor 1: The district court has not granted a stay, nor is there any evidence that a stay will be granted.

In the parallel district court action involving the same claims of the '339 patent, the district court has not granted a stay pending IPR. Further, Qualcomm has not requested such a stay, there is no indication it will do so, and there is no evidence that a stay will be granted.

Moreover, the facts here indicate that it is unlikely that the district court would grant a stay pending IPR even if this IPR were instituted, given the late stage of litigation. In the Qualcomm² action final contentions will be exchanged and claim construction concluded by the time of the institution decision while fact discovery will be halfway finished. Ex. 2002. Further, trial is currently set for June 22, 2026,

² Because the NXP action has been stayed pending settlement, Ex. 2023, and any settlement can be reasonably expected to moot NXP's involvement in this IPR, only the Qualcomm district court case is relevant for *Finitiv* considerations.

three months before the institution decision respectively. *Id.*

Even if Qualcomm were to file a motion for a stay pending this proceeding, it is highly unlikely Judge Albright or Judge Gilliland would grant a stay at this late juncture in the cases. *See, e.g., Smart Mobile Techs. LLC v. Samsung Elecs. Co.*, No. 6:21-CV-00701-ADA, 2023 WL 11999028, at *3 (W.D. Tex. Oct. 24, 2023) (Albright, J.) (denying motion to stay pending IPR, where, when defendants’ motion was filed, a claim construction hearing had already occurred, noting “the Court and the Parties have already expended significant resources in furtherance of these proceedings and any future expense that the parties might incur is outweighed by the delay in filing this Motion.”); *Multimedia Content Mgmt. LLC v. Dish Network L.L.C.*, No. 6:18-CV-00207-ADA, 2019 WL 11706231, at *3 (W.D. Tex. May 30, 2019) (Albright, J.) (same); *Datanet LLC v. Dropbox Inc.*, No. 622CV01142OLGDTG, 2023 WL 9005604, at *3 (W.D. Tex. Dec. 28, 2023) (Gilliland, M.J.) (finding the case had “reached a stage by which postponing resolution of the matter until the conclusion of IPR would come at substantial cost” when the Court had already conducted a *Markman* hearing). Moreover, Judge Albright’s rate of granting contested motions to stay pending an IPR is less than 20%. *See* Ex. 2003.

Where the district court litigation has not been stayed, and any stay is speculative and unlikely, allowing this IPR to proceed in parallel would be wasteful and inefficient. Factor 1 weighs against institution.

B. *Fintiv* Factor 2: The district court trial will occur more than three months before the deadline for a final written decision in this proceeding.

“If the court’s trial date is earlier than the projected statutory deadline, the Board generally has weighed this fact in favor of exercising authority to deny institution under *NHK*.” *Fintiv I* at 9.

Here, the deadline for a final written decision in this IPR is September 12, 2026, which may be extended into 2027, for good cause or in the case of joinder. 37 C.F.R. § 42.100(c). Meanwhile, the district court litigation is set for trial on June, 22, 2026 for Qualcomm. *See* Ex. 2002. The timeframe set by the district court is consistent with the Federal Court Management Statistics for the Western District of Texas. *See* Ex. 2004 at 3 (encouraging use of these statistics in evaluating this factor). Those statistics indicate that on average, over the past six years, a civil case in the district was brought to trial 27.26 months after filing. Ex. 2005 (indicating median times to trial for civil cases for the twelve-month period ending in December for 2019-2024 as 27.9, 18.5, 25.5, 29.5, 28.3, and 33.9). Here, trial is set approximately 28 months after filing of the complaint in NXP and 21 months after

filing in Qualcomm³. Exs. 2001, 2002.

Thus, consistent with historical statistics, the district court trial is set to occur **three months** before the deadline for a final written decision, and possibly nearly a year before the deadline if extended. This weighs heavily against institution. *See, e.g., Samsung Elecs. Co. v. Mojo Mobility Inc.*, IPR2023-01094, Paper 11 at 8-9 (PTAB Feb. 9, 2024) (“*Mojo*”) (denying institution when trial was set before the final written decision would issue); *BOE Tech. Grp. Co. v. Element Capital Commercial Co.*, IPR2023-00808, Paper 9 at 21-22 (PTAB Nov. 15, 2023) (“*BOE*”) (same); *Vector Flow, Inc. v. HID Global Corp.*, IPR2023-00353, Paper 8 at 19-20 (PTAB July 17, 2023) (“*Vector Flow*”) (same); *Roku, Inc. v. IOEngine, LLC*, IPR2022-01551, Paper 11 at 10-11 (PTAB May 5, 2023) (“*Roku*”) (same).

Indeed, the Board has denied institution on account of even smaller gaps between the final written decision and trial. *See, e.g., EClinicalWorks, LLC v. Decapolis LLC*, IPR2022-00229, Paper 10 at 9 (PTAB Apr. 13, 2022) (“*EClinicalWorks*”) (finding this factor weighed in favor of discretionary denial and denying institution where “the beginning of the jury trial in the WDTX Cases is roughly **one or two months** before any final decision would have been due had *inter*

³ Notably, the Qualcomm action asserts the same claims of the same patent against Qualcomm’s use of the same ARM big.LITTLE architecture as the earlier-filed NXP action, and Qualcomm is likewise represented by the same counsel as NXP was in the earlier-filed action. *See* Exs. 1034, 1035. Such overlap and obvious cooperation of Petitioners more than justifies the somewhat faster than median time to trial in the Qualcomm action.

partes review been instituted”); *Fintiv II* at 13 (finding this factor weighed in favor of discretionary denial and denying institution where the district court trial was scheduled to occur **two months** before the deadline for the Board to reach a final written decision); *NXP USA, Inc. v. Impinj, Inc.*, PGR2022-00005, Paper 20 at 5-6 (PTAB August 25, 2022) (“*NXP*”) (same).

Because the district court trial is currently set to occur three months before the earliest deadline for a final written decision in this IPR, the set date is consistent with current time-to-trial statistics, and there is no evidence that this date may change, this factor weighs heavily against institution. *Fintiv II* at 13.

C. *Fintiv* Factor 3: By the time an institution decision is reached, the Court will have held the *Markman* hearing and fact discovery will be nearing completion.

Factor 3 relates to the “amount and type of work already completed in the parallel litigation by the court and the parties ***at the time of the institution decision.***” *Fintiv I* at 9. For example, “if, at the time of the institution decision, the district court has issued substantive orders related to the patent at issue in the petition,” this factor favors denial. *Id.* at 9-10. “Likewise, district court claim construction orders may indicate that the court and parties have invested sufficient time in the parallel proceeding to favor denial.” *Id.* at 10.

Here, by the time the institution decision issues, the *Markman* hearings will be complete and a *Markman* order will have issued or will soon issue. The *Markman*

decision would clearly qualify as a “substantive order.” But even if the *Markman* order does not issue prior to the institution decision, in any event, claim construction proceedings will be complete, and the district judge would have taken these substantive issues under submission. Exs. 2001, 2002. Fact discovery will also be about half-completed in the Qualcomm action. Ex. 2002.

These investments by the parties and district court weigh against institution because they ensure that this IPR cannot be an efficient alternative to district court litigation. This favors discretionary denial, and panels have found this factor to favor denial when the parallel litigation was at a similarly advanced stage as here. *See, e.g., BOE* at 23-24 (denying institution in part because claim construction was complete and fact discovery was nearly completed); *Roku* at 12 (same); *Mojo* at 9 (same).

Of course, the reason that the district court litigation will be so far along at the time of institution is because Petitioners unduly delayed in filing the Petition. For NXP, the Petition comes a matter of weeks before the statutory bar date. *See* Ex. 1014. For Qualcomm, the Petition is somewhat more timely, though Qualcomm is taking advantage of their counsel’s work for NXP and thus could have easily filed much sooner. *See* Ex. 2006 (NXP’s Invalidity Contentions served October 25, 2024, one month after the Qualcomm action was filed, citing all IPR references except *Ozer* and *Williams*.) The Petition offers no explanation for either Petitioner’s delay.

Because there has been substantial investment in the parallel proceeding, and Petitioners delayed in filing the Petition, Factor 3 weighs heavily against institution.

D. *Fintiv* Factor 4: There is substantial overlap between this IPR and the district court proceeding.

This factor looks at “whether all or some of the claims challenged in the petition are also at issue in district court” and whether the “petition includes the same or substantially the same claims, grounds, arguments, and evidence” as the parallel district court case. *Fintiv I* at 12-13. Here, the challenged and asserted claims are identical, and the prior art relied upon in the Petition and at the district court is substantially overlapping.

First, the Petition challenges claims 1-3, 5, 8-11, 14, and 21 of the ’339 patent; this differs from the claims currently asserted in the district court actions by three dependent claims. *Compare* Pet. at 7 (challenging claims 1-3, 5, 8-11, 14, and 21) *with* Exs. 1034, 1035 (infringement contentions asserting claims 1, 5, 8-10, 14, 21); *see also Pharaoh Energy Servs., LLC v. Flex-Chem Holding Co.*, IPR2024-00815, Paper 7 at 13-14 (PTAB Sept. 20, 2024) (denying institution in part because the same claims were challenged at the PTAB and asserted in litigation); *Vector Flow* at 22 (same); *EClinicalWorks* at 12 (same).

Second, all of the references relied upon by the Petition are also relied upon by both Petitioners at the district court. Exs. 2007, 2008. Indeed, both Petitioners

identify the same or similar combinations of these references at the district Court. Ex. 2009, 2010 (offering 500 pages of combinations, with White combinations beginning on 368 and Elgebaly combinations at 467).

Petitioners' *Sotera* stipulations, Exs. 2011, 2012, do nothing to assuage this concern. Such stipulations are inherently ineffective. First, the Board has no ability to enforce such a stipulation as its impact is before the district court. Previously, this led to inconsistent applications, but now the Federal Circuit has weighed in to explain "IPR estoppel does not preclude a petitioner from relying on the same patents and printed publications as evidence in asserting a ground that could not be raised during the IPR, such as that the claimed invention was known or used by others, on sale, or in public use." *Ingenico Inc. v. IOENGINE, LLC*, No. 2023-1367, 2025 WL 1318188, at *7 (Fed. Cir. May 7, 2025). The Director has already found that even if not the same "ground" where "invalidity arguments in the district court are more expansive and include combinations of the prior art asserted in these proceedings with unpublished system prior art, which Petitioner's stipulation is not likely to moot," a *Sotera* stipulation does not weigh in favor of institution. *See Motorola Solutions, Inc. v. Stellar, LLC*, IPR2024-01205, Paper 19 at 3-4 (PTAB Mar. 28, 2025). As one commenter explained, this is a dramatic shift from how many district courts previously addressed estoppel and allows a patent challenger to "take the exact same printed publications that were (or could have been used) in an IPR

proceeding and simply repackage them under a different statutory label in district court litigation.” Ex. 2025, *see also* Ex. 2025. With the Federal Circuit’s narrow interpretation of IPR estoppel, a *Sotera* stipulation, on its own has nearly no value in preventing overlap between an IPR and district court actions.

As Petitioners made their *Sotera* stipulation before the Federal Circuit’s clarification, Patent Owner requested Petitioners clarify to what extend their stipulation would cover arguments “cumulative of grounds that could have been brought before the PTAB.” Ex. 2020. Petitioners were unable to provide any reasonable clarity and conceded “[t]he applicability of that statute to a specific item of system art in view of specific items or printed publication art is fact-specific, and what [was] laid out [] is too vague to be workable at this stage.” Ex. 2021.

Patent Owner agrees. Petitioners’ *Sotera* and addition stipulations are too vague to provide any assurance that there will be no substantial overlap between the district court proceedings and the proposed IPR proceedings. Petitioners additionally stipulated to not raise “system art where ‘there is no substantive difference between’ a printed publication and the system art.” Ex. 2021. But there is no clarity in how that can be applied. Instead of preserving resources, the stipulations will only create further disputes: What is a “substantive difference”? How much of the system art is needed in the new ground? Is it sufficient to merely point to a single feature not disclosed in the printed publications? Both Petitioners have already shown how they

intend to prosecute their invalidity defense, with 500 pages of obviousness combinations based on 57 references and 3 “systems” so far. Exs. 2009, 2010. In light of such an obscenely excessive number of invalidity grounds, it is clear Petitioners will not be satisfied with a narrow, efficient invalidity case.

Both Petitioners already argue invalidity of the '339 Patent based on three different processors in various combinations with White, Talwar, Cho, Vajada, Elgebaly, Ozer, and Williams. Exs. 2009, 2010 at 400-34. Moreover, each of White, Talwar, Vajada, Elgebaly, and Ozer are or were owned by major players in the development of multi-core processors, AMD, HP, Ericsson, ARM, and Qualcomm. *See*. Ex. 1004, 1006, 1010, 1011. These are fertile grounds for Petitioners to maintain multiple §§102, 103 invalidity grounds, not to efficiently consolidate those arguments into a single proceeding. Petitioners' lack of willingness to provide a definite stipulation considered with their excessive invalidity contentions outweighs any impact of their stipulations.

Moreover, there is nothing to bar the Petitioners from seeking *ex parte* reexamination should it not receive its preferred outcome here. As the director has recognized, the resources of the PTAB are limited, Ex. 2013, why then, should this IPR be instituted when the Petitioners may, if they do not receive a favorable outcome, simply choose another avenue? Even if Petitioners' stipulation were considered to be an effective tool in ensuring no overlap between the district court

and the instant Petition, such a stipulation has no bearing on an *ex parte* reexamination, even on the exact same grounds. *See* Exs. 2011, 2012.

In short, the Petition challenges the same patent claims that are asserted in the parallel litigation, and Petitioner relies on substantially overlapping prior art at the district court. This raises substantial “concerns of inefficiency and the possibility of conflicting decisions,” weighing against institution. *See Fintiv I* at 12.

E. *Fintiv* Factor 5: Petitioner is a defendant in the district court litigation.

Petitioners are defendants in the parallel litigation. *See* Exs. 1014, 1015; *see, e.g., Fintiv II* at 15 (“Because the petitioner and the defendant in the parallel proceeding are the same party, this factor weighs in favor of discretionary denial.”).

F. *Fintiv* Factor 6: Other circumstances weigh strongly against institution, including the weakness of the Petition and Petitioner’s delay.

This factor looks at “other circumstances that impact the Board’s exercise of discretion, including the merits.” *Fintiv I* at 9. This factor also weighs heavily against institution.

First, the merits of this Petition suffer from significant weaknesses and gaps in proof, as discussed below. *See infra* § IV.C. Thus, the Petition fails to present a “compelling unpatentability challenge” and fails to establish a reasonable likelihood of success.

Second, many of the other relevant considerations identified by the Interim

Processes for PTAB Workload Management memorandum, Ex. 2013, weigh against institution. *See Infa* §IV.

These factors demonstrate and reinforce that efficiency and system integrity considerations weigh overwhelmingly in favor of a discretionary denial here.

IV. The PTAB Workload Management Factors Weigh Against Institution

Consistent with and in addition to the factors identified in *Finitiv*, the Interim Processes for PTAB Workload Management Memorandum (“Workload Memo”) provides enumerates seven relevant considerations (“Workload Management Factors”):

- Whether the PTAB or another forum has already adjudicated the validity or patentability of the challenged patent claims;
- Whether there have been changes in the law or new judicial precedent issued since issuance of the claims that may affect patentability;
- The strength of the unpatentability challenged;
- The extent of the petition’s reliance on expert testimony;
- Settled expectations of the parties, such as the length of time the claims have been in force;
- Compelling economic, public health, or national security interests; and
- Any other considerations bearing on the Director’s discretion.

Ex. 2013 at 2-3.

These considerations weigh strongly in favor of a discretionary denial. The Petition cites no changes in the law or precedent impacting patentability. Instead, the Petition attempts to have the Patent Office reconsider art that was already at issue during prosecution in a combination that is substantially the same as what was previously considered. Moreover, the Petition heavily relies on Dr. Annavaram to overcome the teachings of the prior art itself but to make matters worse, Dr. Annavaram largely parrots the petition. Considering the '339 Patent has been in force since 2013 and was filed before the IPR regime was created, Redstone should not be subjected to yet another attack on its hard-earned patent rights. Such a Petition is a poor candidate to take up the Board's limited capacity

A. Prior Adjudication

The first consideration asks “whether the PTAB or another forum has already adjudicated the validity or patentability of the challenged patent claims.” Ex. 2013 at 2. Here, the PTAB has already denied institution on the merits of a prior IPR challenge and the district court will rule on §112 grounds three times prior to institution. Furthermore, the Petition seeks to have the Board reconsider art the examiner already considered based on arguments the examiner rejected contrary to §325(d).

First, MediaTek recently brought an IPR petition to invalidate the same claims Petitioners now challenged. Ex. 2022 at 1. The PTAB denied institution, not on any

procedural grounds, but on the merits. *See Id.* In both grounds, MediaTek failed to demonstrate the prior art in either of its main grounds taught or suggested “a first and second PLL with respective first and second clock signals as inputs where the first clock signal is independent from the second clock signal.” *See id.* at 19, 28. In both instances considered by the Board, the prior art on its own failed to disclose the claimed clock arrangement. *Id.* The Board went on to explain that while MediaTek’s expert argued either that the arrangement was disclosed or would have been obvious, such testimony was entitled to no credit as it was entirely conclusory. *Id.* at 19-20, 29. The instant Petition suffers from the same deficiencies, there is no disclosure of two PLLs as claimed and expert testimony otherwise is entirely conclusory. *See Infra* §IV.C. With such close similarities to an already denied petition, the Board’s prior institution decision weighs in favor of discretionary denial.

Second, each of MediaTek, NXP, and Qualcomm challenge the patentability of the asserted claims in the district court actions. Exs. 2006, 2007. For NXP and MediaTek, the district court has already ruled on their indefiniteness challenges. *See* Exs. 2014, 2015. For Qualcomm, these challenges will be adjudicated three months before any institution decision. *See* Ex. 2002. This is in addition to both Petitioners’ other validity challenges in district court, which will be adjudicated before a final written decision, as noted *Supra* §III.B.

Beyond these challenges that either have been adjudicated such as the indefiniteness arguments and MediaTek's IPR challenge or will adjudicated prior to the instant IPR, the Patent Office has already considered White and grounds substantially the same as Grounds 1-3. §325(d) presents the same concerns as this consideration and asks "whether the petition presents to the Office the same or substantially the same art previously presented to the Office, or whether the petition presents to the Office the same or substantially the same argument previously presented to the Office." *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 7 (Feb. 13, 2020)(precedential) ("*Advanced Bionics*"). Both concerns are present here. White was disclosed by the Applicant over a year before the first office action and White in combination with Talwar is substantial the same as the Jacobowitz and Kim combination that was considered in that office action.

During prosecution, the Applicant listed three references in an information disclosure statement on August 2, 2011, including White. Ex. 1005 at 102. A year later, the examiner issued an office action primarily based on two references, Jacobowitz and Kim. *Id.* at 91-100. Notably, this Kim reference was cited on the face of the Kim reference (U.S. 7,853,808) disclosed by the applicant's IDS. *See* Ex. 2017 at 2. As the Board has held "[p]reviously presented art includes ... art provided

to the Office by an applicant, such as on an Information Disclosure Statement,”
White is clearly, previously presented art. *See Advanced Bionics* at 7-8.

However, even ignoring that White was previously presented, and assuming White was not actually considered by the Examiner, unlikely given it was only one of three references disclosed at the time, the White-Talwar grounds present nothing new. For the purposes of the Petition, White offers nothing different than Kim and Talwar offers nothing more than Jacobowitz. As such, Grounds 1-3 present substantially the same arguments as grounds the Office has already considered.

As the Petition describes White, it mirrors the relevant architecture of Kim. The Petition contends “[f]requency regulator 140 includes ‘various sorts of clock sources such as an oscillator or phase locked loop (PLL) to generate a reference clock’ and uses those ‘multiple clock sources in order to supply multiple, independent clock signals of different frequencies.’” Petition at 22. This further includes “each ‘logic core may generate its internal clock using a phase-locked loop (PLL) locked to an externally provided clock signal’ from ‘frequency regulator 140.’” *Id.* This is substantially the same as what Kim disclosed. Kim teaches a “main PLL 260 comprises ... *one or more frequency dividers*” and “the multi-core processor comprises additional PLLS, which receive an input from the main PLL 260 ... indicated by respective arrows 262, 264, 266, and 268.” Ex. 2018 at [0025]. Both teach a central clock structure providing clock signals to individual PLLs

associated with individual cores. Indeed, the similarity extends to voltage as well. The Petition explains White provides a voltage regulator that “may be configured to supply independent voltages to each logic core,” each of which can be “different from the voltage levels at which other logic cores are operated.” Petition at 21-22. Kim teaches each core has “its own separate power supply voltage.” Ex. 2018 at [0025]. Last, the Petition points to White’s “common bridge logic” that is “configured to communicate with the logic cores as well as with other elements or peripherals.” Petition at 24. Kim teaches a “main controller 250” connected to each of the cores with “a voltage level-translating communication transceiver ... that is configured to enable communications between the main controller 25 and the plurality of cores 210, 220, 230 and 240.” Ex. 2018 at [0025]. Given all the Petition points to Talwar for is clusters of cores, Petition at 24-25, and Jacobowitz provides sets of “four cores 102,” Ex. 2019 (Jacobowitz) at [0025], Talwar is not a source for anything new.

In light of the above, the White-Talwar grounds are substantially the same as Jacobowitz and Kim. As noted above, Kim and White are substantially the same for purposes of the Petition’s arguments, both provide a central clock structure providing multiple clock signals to PLLs associated with individual cores, both teach providing each core with a separate voltage, and both provide a means for communicating between the cores. While Jacobowitz was cited for much more than

Talwar, both include grouped cores. As such the similarities are substantial and the differences immaterial. While the examiner did not expressly consider the application of Jacobowitz's core groups to Kim's architecture, the examiner did consider the combination of Jacobowitz and Kim. Ex. 1005 at 96-98. Given the Petition identifies no error by the examiner, instead vaguely pointing to independent voltages, for which the Petition offers much the same as Kim, there is no basis to revisit the Office's prior determination of patentability on Grounds 1-3. Institution should be denied under §325(d).

In light of four earlier validity challenges, many having already been adjudicated, and all scheduled to complete prior to this IPR, and the Office's prior examination of several of the instant grounds, there is little basis for the Patent Office to expend its limited resources on the instant challenge.

B. No Changes in the Law Support Reconsideration of Validity

The second consideration asks "whether there have been changes in the law or new judicial precedent issued since issuance of the claims that may affect patentability." Ex. 2013 at 2. No such changes exist. This is all the more striking when, as noted above, the Petition seeks reconsideration of material the Office considered when granting the '339 Patent in the first instance. The lack of such a change here is thus particularly damning.

C. The Petition is Particularly Weak and Overly Reliant on Unreliable Expert Testimony.

The third and fourth consideration tests the “strength of the unpatentability challenge” and the “extent of the petition’s reliance on expert testimony.” Ex. 2013 at 2. Here, the unpatentability challenge has severe facial flaws, many related to its reliance on expert testimony. Grounds 1-3 present a central motivation to combine that violates the express teachings of White and relies on an expert testimony that merely parrots the petition to fill in a missing limitation. Grounds 4-8 rely on such testimony for multiple limitations and blatantly create disclosures of claimed limitations from whole cloth. Moreover, these points will ultimately be subject to a battle of the experts as will be addressed in the upcoming Patent Owner Preliminary Response. The Board should not expend its limited resources on a such a facially weak petition.

Grounds 1-3 all rely on the same primary combination of White and Talwar, in particular, the architecture of White with the clusters taught by Talwar. *See* Petition at 26-28. But the only basis the Petition enumerates for making such a modification of White is that a POSITA would supposedly “have understood such a design would *need* to be adapted as the number of cores increases due to chip space constraints associated with adding an additional voltage and clock control and supply circuitry for each additional core.” *Id.* at 25 (emphasis added). But this

“*need*” does not exist in White. In fact, White itself explains the device it teaches may “include *any number* of logic cores configured to operate at *independent voltages and/or frequencies*.” Ex. 1006 at 6:56-60 (emphasis added). If any number of cores may be configured to operate with their own independent voltages and frequencies, there is no *need* for an architecture that provides grouped voltages and frequencies as the number of logic cores increases. A POSITA considering White would have no *need* to alter it, much less a motivation to achieve any particular configuration.

The Petition relies on Dr. Annavaram to create this need and rewrite White, but Dr. Annavaram cannot rescue this combination. First, to create a need not found in White, Dr. Annavaram cites to tertiary references that only offhandedly acknowledge a design constraint but whose discussion reveals why a POSITA would specifically choose White, as taught, over some other architecture. Dr. Annavaram points to two academic references that each acknowledge “it may not be practical to implement multiple power domains using off-chip voltage regulators.” *See* Ex. 1002 at ¶73 (citing Ex. 1029 at 3-4, Ex. 1019 at 52-53). But each of these references examine the outcome of per-core, like White, and chip-wide DVFS domains, not a per-cluster domain, and weigh the results. The first determines “depending on the heterogeneity of workload characteristics, per-core DVFS offers *substantial additional savings* compared to global DVFS schemes by better adapting to the

different requirements of each core.” Ex. 1029 at 4 (emphasis added). The second found “on a four-core CMP in which DVFS was being employed to avoid thermal emergencies (rather than simply to save power), a per core approach had **2.5X better throughput** than a per-chip approach.” Ex. 1019 at 53 (emphasis added). Notably, temperature management is the primary concern White discusses with its DVFS system. *See e.g.* Ex. 1006 at 1:37-52 (“Since complex ICs such as microprocessors tend to be expensive, it is typically desirable to protect them from damage due to overheating.”); 2:29-44 (“Also, rather than simply shutting down a processor that is operating to warmly(as is generally done in the prior art), one or more of the logic cores in the processor may be adjusted to operate at a lower frequency and/or voltage so that the processor may generate less heat, and therefore may cool down to an acceptable temperature.”); Claims 2-10, 13-14, 16-24, 26-29, 31-32 (all claiming a temperature control limitation). A POSITA considering White’s teaching that its techniques to manage thermal emergencies “may be applied to systems or devices that include any number of logic cores,” seeing such greater throughput than the available alternative, would not alter White.

All the Petition cites from White is that its “independently controlling operating voltages and/or frequencies may be applied to any integrated circuit or component...” *See* Petition at 26 (citing Ex. 1006 at 8:44-49). But that application to “any integrated circuit” is explained and does not relate to cores. White explains

“[f]or instance, a controller, bridge or other components configured to interface to, or communicate with multiple components may be configured to independently control the frequency and or voltages of those interfaces.” Ex. 1006 at 8:49-53. White teaches its technique of interoperating or interfacing components at different frequencies and voltages can be applied to any such interfacing components, not that it can be applied to any arrangement of cores.

Without any real motivation to combine White and Talwar, it is no wonder then that there is no explanation for why a POSITA would be motivated to apply Talwar’s “clusters” how the Petition suggests. In particular, the use of a cluster-wide PLL where no reference teaches the use of a PLL to supply a final clock frequency to multiple cores. These newly invented cluster-wide PLLs are what the Petition identifies as the claimed first and second PLLs in each of the three “configurations.” Petition at 29-31. But despite their importance, the Petition devote only part of a parenthetical to explain them, much less justify their use. Petition at 27 (“Further, clock control circuitry that White describes at the core level (e.g., a PLL at the core and accompanying ‘control registers’ storing ‘PLL configuration parameters’) would operate at the cluster level.”). Dr. Annavaram offers no better and merely concludes “frequency regulator 140 provides on clock signal to a local PLL shared by cores 120A and 120C and an independent clock signal to a separate, local PLL shared by cores 120B and 120D.” Ex. 1002 at ¶78. But White *only* uses a one-to-

one arrangement of local PLLs and cores. Ex. 1006 at 9:62-10:10. Talwar, where a POSITA would more reasonably expect to derive a cluster architecture, provides *no* explanation for how to provide a cluster-wide frequency. *See* Ex. 1007. Only hindsight provides an explanation for why a cluster-wide PLL would be used, because it meets the limitation.

The Petition's Grounds 1-3 lack a motivation to combine or an explanation for key limitations in the independent claims. To make up for these holes, the Petition heavily relies on unsupported expert conclusions. Beyond a lack of support, Patent Owner's expert is expected to offer competing testimony explaining how a POSITA would reach the opposite conclusion as Dr. Annavaram. The Director should consider this "battle of the experts" when considering this request for discretionary denial. This weighs heavily against institution under both considerations.

Grounds 4-8 fair even worse. Where Grounds 1-3 present a tenuous motivation to combine references, Grounds 4-8 conjure multiple limitations from thin air. These grounds cite Elegebaly for the first and second sets of processor cores and the first and second PLLs but Elegebaly does not disclose either. Instead, the Petition must allege they were "known design choices," but there is no evidence that these design choices were known and Dr. Annavaram cannot show otherwise.

First, Elgebaly does not teach any particular clock/frequency architecture. Instead, Elgebaly provides an amorphous block, clock generator 140, that “may include one or more phase locked loops (PLLs) that control the oscillators used to generate the clocks.” Ex. 1004 at [0028]. Elgebaly teaches that each core provides a target frequency to the clock generator and the clock generate provides a clock signal at that frequency. *Id.* at [0032]. Nothing more is explained as to the structure of Elgebaly’s clock generator, just a function and a handful of components. Despite this, the Petition contends a reference to “oscillators” and PLLs means the claimed architecture is rendered obvious. Petition at 52-53. Not so.

The Petition offers that “multiple PLLs each receiving a distinct clock signal from a different external oscillator crystal and, in turn outputting one of the desired clock signals” would be a “known clock distribution channel” or an “obvious design choice.” *Id.* at 53. To support these conclusions, the Petition relies on the Declaration of Dr. Annavaram, *id.*, but all Dr. Annavaram provides is a near copy of the petition. He offers some minor phrasing changes, “two PLLs” instead of “multiple PLLs,” “the clock for each core ‘may be set independently’” instead of “clocks ‘may be set independently’ for each core,” but it is still a mere parroting in substance. *Compare* Petition at 53 *with* Ex. 1002 at ¶¶141-42. Dr. Annavaram’s declaration is entitled to little weight. *See Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15-17 (PTAB August 24, 2022) (designated precedential) (expert declaration that merely

repeats “the conclusory assertion for which it is offered to support” “is entitled to little weight”). Conclusory attorney argument based on a conclusory expert declaration does not support an obviousness argument. *See Facebook v. Windy City Innovations, LLC*, 973 F.3d 1321, 1340-41 (Fed. Cir. 2020) (affirming expert testimony “did not ‘add materially to Petitioner’s unpersuasive attorney argument’ because it ‘merely repeated Petitioner’s argument, nearly verbatim, without citation to the basis for his testimony.’”)

Even if Dr. Annavaram’s “known technique” argument is considered, it is legally deficient. A “known technique” argument requires several showings. There must be a “known technique to address a known problem using ‘prior art elements according to their established functions.’” *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023). Neither the Petition nor Dr. Annavaram address any of these requirements. In particular, there is no showing that applying a single PLL to multiple cores is an established function. The only evidence either the Petition or Dr. Annavaram can cite to is a Figure from a tertiary reference not part of any ground. Ex. 1002 at ¶¶141-42. But this Figure only provides how two clock domains might be created, not how they would be implemented or be applied to any arrangement of cores. *See Id.*, Ex. 1008, Fig. 1. But how a clock domain is applied to a set of cores is critical, the claims mandate a single PLL providing an output clock signal to a set cores. But because this feature is absent from every single reference

cited in the Petition, the Petition must rely on Dr. Annavaram to provide it in every ground. The Petition's Grounds 4-8 cannot show the claimed first and second PLLs are obvious and thus cannot show any claim is invalid.

But this is not the only flaw with Grounds 4-8. The Petition attempts the same something-from-nothing argument with the first and second set of processor cores. As the parties agree, a "set of processor cores" means a group of two or more processor cores. But Elgebaly teaches no such thing.

Elgebaly instead teaches providing two cores with individual clock and voltage controls and that the cores could instead have a single clock and a single voltage signal. Ex. 1004 at [0033]. In other words, Elgebaly teaches per-core or chip-wide voltage and clock systems. These were very well known in the art as either a per-core or chip-wide DVFS scheme. *See e.g.* Exs. 1019, 1029. But individual cores and a single group of cores does not teach subdivisions larger than individual cores as will be further explored by Patent Owner's expert.

To draw out the claimed element, the Petition offers just two paragraphs, again parroted by Dr. Annavaram. *Compare* Petition at 54-55 with Ex. 1002 at ¶¶144-45. The Petition contends the claimed first and second set of processor cores is "a well-known approach to balancing competing design factors," but can only point to Talwar⁴ as demonstrating that design. Petition at 54-55. To the extent the Petition is

⁴ Notably, Talwar is not part of Grounds 4-8.

again arguing “known technique,” one example hardly establishes a “known technique to address a known problem.” The de minimis source of proof is only underlined by Dr. Annavaram broadly parroting Petition yet again, and thus being entitled to little weight. Grounds 4-8 thus cannot demonstrate that a first and second set of processor cores are obvious.

The Petition cannot, under any ground, demonstrate that it would be obvious to implement the claimed first and second PLL or claimed first and second sets of processor cores. Recognizing this, the Petition relies heavily on expert testimony to fill in these gaps, but does so only by parroting the Petition. Because the merits of the Petition do not warrant institution without heavy reliance on an unreliable expert declaration, these considerations favor discretionary denial.

D. The Patent Has Been In Force As Long As The IPR Regime

This consideration looks to the “[s]ettled expectations of the parties, such as the length of time the claims have been in force.” Here, the ’339 Patent has been in force since 2013 and was filed in 2010. Ex. 1001 at 1. Considering this filing predates the America Invents Act and the IPR regime itself, the settled expectation is that the ’339 Patent is valid. But moreover, of the three parties that have now challenged the ’339 Patent in an IPR, two are in the process of settling their infringement of the ’339 Patent. Exs. 2023, 2024. While NXP and MediaTek will doubtlessly proclaim their settlement is not a concession that the ’339 Patent is valid,

the fact of the matter is only valid patents are infringed and moneys are only owed on infringed patents.

E. Significant Weakness on Other Discretionary Denial Regime Also Favors Denial

As discussed above, the Petition presents serious efficiency concerns under *Fintiv*, half of the grounds are the same or substantial the same as those considered in prosecution, and no ground shows a substantial likelihood of success. Each of these presents an independent basis to deny institution or at least seriously question the expenditure of limited Patent Office resources, together they present a clear basis for the Director deny institution under her discretion.

V. CONCLUSION

Patent Owner respectfully requests that the Director exercise her discretion under Sections 314(a) or 325(d) to deny institution. First, the Director should exercise her discretion under Section 314(a) to deny institution because of the status of the co-pending lawsuits in light of Petitioner's delay in filing the Petition. Second, the Director should exercise her discretion more generally under Sections 314(a) and 325(d) to deny institution because the Petition does not present a new or compelling basis for institution.

Date: May 12, 2025

Respectfully submitted,

IPR2025-00485 Request for Discretionary Denial
U.S. Patent No. 8,549,339

/Neil A. Rubin/

Reza Mirzaie, Reg. No. 69,138

Neil A. Rubin, Reg. No. 67,030

Christian Conkle, (PHV to be Filed)

RUSS, AUGUST & KABAT

12424 Wilshire Blvd., 12th Floor

Los Angeles, CA 90025

Qi (Peter) Tong, Reg. No. 74,292

ptong@raklaw.com

Russ August & Kabat

8080 N. Central Expy., Suite 1503

Dallas, TX 75206

Counsel for Patent Owner

CERTIFICATION REGARDING WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner certifies that there are 7,589 words in the paper excluding the portions exempted under 37 C.F.R. §42.24(a)(1).

Date: May 12, 2025

/Neil A. Rubin/

Reza Mirzaie, Reg. No. 69,138

Neil A. Rubin, Reg. No. 67,030

Christian Conkle, (PHV to be Filed)

RUSS, AUGUST & KABAT

12424 Wilshire Blvd., 12th Floor

Los Angeles, CA 90025

Qi (Peter) Tong, Reg. No. 74,292

ptong@raklaw.com

Russ August & Kabat

8080 N. Central Expy., Suite 1503

Dallas, TX 75206

Counsel for Patent Owner

CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e)(1))

The undersigned hereby certifies that the above document was served on April 12, 2025, by filing this document through the Patent Trial and Appeal Case Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

Eagle H. Robinson
eagle.robinson@nortonrosefulbright.com
Norton Rose Fulbright US LLP
98 San Jacinto Blvd., Ste. 1100
1550 Lamar Street, Ste. 2000
Austin, TX 78746
Houston, TX 77010-4106
512.536.3083 (telephone)
713.651.8360 (telephone)

Daniel S. Leventhal
daniel.leventhal@nortonrosefulbright.com
Eric C. Green
eric.green@nortonrosefulbright.com
G. Duncan Waldrop
duncan.waldrop@nortonrosefulbright.com
Norton Rose Fulbright US LLP
98 San Jacinto Blvd., Ste. 1100
Austin, TX 78746
512.536.3009 (telephone)

Richard S. Zembek
richard.zembek@nortonrosefulbright.com
Norton Rose Fulbright US LLP
1550 Lamar Street, Ste. 2000
Houston, TX 77010-4106
713.651.5283 (telephone)

Date: May 12, 2025

/Neil A. Rubin/
Neil A. Rubin, Reg. No. 67,030
RUSS, AUGUST & KABAT
12424 Wilshire Blvd., 12th Floor
Los Angeles, CA 90025

Counsel for Patent Owner