

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND/ODESSA DIVISION**

REDSTONE LOGICS LLC,

Plaintiff,

v.

NXP USA, INC.

NO. 7:24-cv-00028-DC-DTG

Defendants.

DEFENDANT'S AMENDED INVALIDITY CONTENTIONS

Pursuant to the First Amended Scheduling Order (Dkt. 36), Defendant NXP USA, Inc. (“NXP”) provides the following Invalidity Contentions for U.S. Patent Nos. 8,549,339 (the “’339 Patent”) (the “Asserted Patent”). As of the date of these contentions, Plaintiff Redstone Logics LLC (“Plaintiff”) asserts the following claims (“the Asserted Claims”) of the Asserted Patent against NXP in its Amended Infringement Contentions (“Infringement Contentions”).

Asserted Patent	Asserted Claims
’339 Patent	Claims 1, 5, 8, 9, 10, 14, 21

NXP provides these Invalidity Contentions for at least the Asserted Claims that Plaintiff has identified in its Infringement Contentions. NXP’s exclusion from these Invalidity Contentions of any patent claims that Plaintiff has not asserted in its Infringement Contentions is not an admission that those unasserted patent claims are valid. NXP reserves the right to amend and supplement these Invalidity Contentions, including in the event that Plaintiff is permitted to later amend or supplement its Infringement Contentions.

I. INTRODUCTION

A. Preliminary Statement

These Invalidity Contentions are based on information reasonably available to NXP and of which NXP is aware at this time. These are not, and are not intended to be, final statements or admissions.

This case is still at an early stage. Discovery has just begun, the Court has not issued a claim construction order, and Plaintiff has so far provided little information and few documents in discovery. Moreover, the vast majority of Plaintiff’s infringement allegations in the Infringement Contentions are based on third party literature in general and not the accused products in particular. NXP’s investigations and discovery into third party sources of prior art

Architecture Techniques for Power Efficiency” by Kaxiras, and “Adaptive Techniques for Dynamic Processor Optimization Theory and Practice” by Wang), standards specifications (e.g., ACPI Revision 4.0, and ACPI Revision 5.0), technical publications (e.g., “Configurable On_Line Global Energy Optimization in Multi_Core Embedded” by Deniz; “How to Approach Inter-Core Communication on TMS320C6474” by Mathes; “Multiple clock and Voltage Domains for chip multi processors” by Rotem; NVIDIA tegra_multiprocessor_architecture” by NVIDIA; “Homogenous Dual-Processor core with Shared L1 Cache for Mobile Multimedia SoC” by Nakajima), and state available product systems as demonstrating the knowledge that a person of ordinary skill in the art would have been familiar with and the obvious design choices that a person of ordinary skill in the art would have been able to make when improving upon prior art systems.

1. The '339 Patent

a. Prior Art Patents and Published Patent Applications

NXP identifies the following prior art patents and published patent applications, and their underlying inventions, that anticipate and/or render obvious the Asserted Claims of the '339 Patent.

Ref.	Patent Number / Patent Publication	Country of Origin	Filing Date	Date of Issue/ Publication	Production Number
“Knoth”	US20090158078A1	United States	12/12/2007	6/18/2009	DEFS-RED-PA000000001
	US8051320	United States	12/12/2007	11/1/2011	DEFS-RED-PA000000021
“Flautner”	US20050034002A1	United States	8/4/2003	2/10/2005	DEFS-RED-PA000004124
	US7134031	United States	8/4/2003	11/7/2006	DEFS-RED-PA000000041
“Ramaraju”	US20110119672A1	United States	11/13/2009	5/19/2011	DEFS-RED-PA000000057

CONFIDENTIAL BUSINESS INFORMATION, SUBJECT TO PROTECTIVE ORDER

Ref.	Patent Number / Patent Publication	Country of Origin	Filing Date	Date of Issue/ Publication	Production Number
	US8566836	United States	11/13/2009	10/22/2013	DEFS-RED-PA000000068
"White"	US20070156370A1	United States	1/3/2006	7/5/2007	DEFS-RED-PA000000079
	US7263457	United States	1/3/2006	8/28/2007	DEFS-RED-PA000000105
"Finkelstein"	US20100115304A1	United States	10/31/2008	5/6/2010	DEFS-RED-PA000000132
	US8402290	United States	10/31/2008	3/19/2013	DEFS-RED-PA000000145
"Branover"	US20080276026A1	United States	5/2/2007	11/6/2008	DEFS-RED-PA000000159
	US7856562	United States	5/2/2007	12/21/2010	DEFS-RED-PA000000169
"Naffziger"	US20100122101A1	United States	11/11/2008	5/13/2010	DEFS-RED-PA000000178
	US8195962	United States	11/11/2008	6/5/2012	DEFS-RED-PA000000192
"Gunther"	US20080104425A1	United States	11/1/2006	5/1/2008	DEFS-RED-PA000000205
	US7949887	United States	11/1/2006	5/24/2011	DEFS-RED-PA000000215
"Elgebaly"	US20070096775A1	United States	11/22/2005	5/3/2007	DEFS-RED-PA000000226
	US7417482	United States	11/22/2005	8/26/2008	DEFS-RED-PA000000250
"Jacobowitz"	US20080256381A1	United States	4/12/2007	10/16/2008	DEFS-RED-PA000000273
	US8161314	United States	4/12/2007	4/17/2012	DEFS-RED-PA000000285
"Titiano"	US20080162770A1	United States	12/11/2007	7/3/2008	DEFS-RED-PA000000298
	US8327158	United States	12/11/2007	12/4/2012	DEFS-RED-PA000000343
"Jong"	US20080046770A1	United States	7/5/2007	2/21/2008	DEFS-RED-PA000000388
	US7870413	United States	7/5/2007	1/11/2011	DEFS-RED-PA000000398
"Cho"	US20100073068A1	United States	9/22/2008	3/25/2010	DEFS-RED-PA000000408
"Nussbaum"	US20110022356A1	United States	7/24/2009	1/27/2011	DEFS-RED-PA000000420

CONFIDENTIAL BUSINESS INFORMATION, SUBJECT TO PROTECTIVE ORDER

Ref.	Patent Number / Patent Publication	Country of Origin	Filing Date	Date of Issue/ Publication	Production Number
"Vajda"	US20120060170A1	United States	5/26/2009	3/8/2012	DEFS-RED- PA000000433
	US8984523	United States	5/26/2009	3/17/2015	DEFS-RED- PA000000447
"Kim"	US20060190755A1	United States	2/16/2006	8/24/2006	DEFS-RED- PA000000462
	US7373540	United States	2/16/2006	5/13/2008	DEFS-RED- PA000000473
"Allarey"	US20100083021A1	United States	9/29/2008	4/1/2010	DEFS-RED- PA000000484
	US8122270	United States	9/29/2008	2/21/2012	DEFS-RED- PA000000495
"Kumar"	US20070080696A1	United States	10/11/2005	4/12/2007	DEFS-RED- PA000000506
	US7327150	United States	10/11/2005	2/5/2008	DEFS-RED- PA000000523
"Oh"	US20060282692	United States	6/6/2006	12/14/2006	DEFS-RED- PA000000539
	US7664971	United States	6/6/2006	2/16/2010	DEFS-RED- PA000000550
"Nordquist"	US7447873	United States	11/29/2005	11/4/2008	DEFS-RED- PA000000561
"Bhandarker"	US20050289365	United States	6/29/2004	12/29/2005	DEFS-RED- PA000000595
	US7249268	United States	6/29/2004	7/24/2007	DEFS-RED- PA000000609
"Talwar"	US20090271646A1	United States	10/31/2008	10/29/2009	DEFS-RED- PA000000621
"Kruglick"	US20110093733A1	United States	10/20/2009	4/21/2011	DEFS-RED- PA000000630
	US8892931	United States	10/20/2009	11/18/2014	DEFS-RED- PA000000644
"Kim II"	US20090138737A1	United States	11/28/2007	5/28/2009	DEFS-RED- PA000000672
	US8578193	United States	11/28/2007	11/5/2013	DEFS-RED- PA000000697
"Soni"	US7526666	United States	9/6/2006	4/28/2009	DEFS-RED- PA000000660
"Onouchi"	US20100083011A1	United States	5/15/2009	4/1/2010	DEFS-RED- PA000000723
	US8239695	United States	5/15/2009	8/7/2012	DEFS-RED- PA000000760

CONFIDENTIAL BUSINESS INFORMATION, SUBJECT TO PROTECTIVE ORDER

Ref.	Patent Number / Patent Publication	Country of Origin	Filing Date	Date of Issue/ Publication	Production Number
"Rusu"	US20040037346A1	United States	8/23/2002	2/26/2004	DEFS-RED-PA000000797
	US6908227	United States	8/23/2002	6/21/2005	DEFS-RED-PA000000805
"Nakajima"	US20060123251A1	United States	12/2/2004	6/8/2006	DEFS-RED-PA000000813
	US7526661	United States	12/2/2004	4/28/2009	DEFS-RED-PA000000821
"Thurston"	US20070008011A1	United States	6/29/2005	1/11/2007	DEFS-RED-PA000001411
"Borkar"	US20070074011A1	United States	9/28/2005	3/29/2007	DEFS-RED-PA000000829
	US7412353	United States	9/28/2005	8/12/2008	DEFS-RED-PA000000849
"Borkar II"	US20070070673A1	United States	9/28/2005	3/29/2007	DEFS-RED-PA000000869
	US7568115	United States	9/28/2005	7/28/2009	DEFS-RED-PA000000885
"Shumarayev"	US20070127616A1	United States	12/2/2005	6/7/2007	DEFS-RED-PA000000901
	US7539278	United States	12/2/2005	5/26/2009	DEFS-RED-PA000000916
"John"	US20070168651A1	United States	2/22/2006	7/19/2007	DEFS-RED-PA000000931
	US7581087	United States	2/22/2006	8/25/2009	DEFS-RED-PA000000943
"Dickinson"	US20070260823A1	United States	4/4/2006	11/8/2007	DEFS-RED-PA000000956
	US7610537	United States	4/4/2006	10/27/2009	DEFS-RED-PA000000974
"Trautman"	US20080005591A1	United States	6/28/2006	1/3/2008	DEFS-RED-PA000000992
"Sistla"	US20080126707A1	United States	11/29/2006	5/29/2008	DEFS-RED-PA000001008
	US8151059	United States	11/29/2006	4/3/2012	DEFS-RED-PA000001025
"Conti"	US20090049220A1	United States	4/10/2008	2/19/2009	DEFS-RED-PA000001042
	US7934036	United States	4/10/2008	4/26/2011	DEFS-RED-PA000001153
"Wolfe"	US20110153984A1	United States	12/21/2009	6/23/2011	DEFS-RED-PA000001260

Ref.	Patent Number / Patent Publication	Country of Origin	Filing Date	Date of Issue/ Publication	Production Number
“Gold”	US20090063888A1	United States	8/31/2007	3/5/2009	DEFS-RED-PA000004149-
“Ozer”	US20080209133A1	United States	2/22/2007	8/28/2008	DEFS-RED-PA000004161
	US7937535	United States	2/22/2007	5/3/2011	DEFS-RED-PA000004205
“Wolfe II”	US20100262742A1	United States	4/14/2009	10/14/2010	DEFS-RED-PA000004249
	US7996595	United States	4/14/2009	8/9/2011	DEFS-RED-PA000004263
“Pelley”	US7777330	United States	2/5/2008	8/17/2010	DEFS-RED-PA000004510
“Cesky”	US7538625	United States	2/27/2008	5/26/2009	DEFS-RED-PA000004520
“Kato”	US20040210738A1	United States	4/27/2004	10/21/2004	DEFS-RED-PA000004529
“Ishimi”	US20080282012A1	United States	1/8/2008	11/13/2008	DEFS-RED-PA000004577
	US8200878	United States	1/8/2008	6/12/2012	DEFS-RED-PA000004559
“Albonesi”	US20050060597A1	United States	1/23/2004	3/17/2005	DEFS-RED-PA000004594
	US7089443	United States	1/23/2004	8/8/2006	DEFS-RED-PA000004613

NXP reserves the right to rely on materials cited on the face of the '339 Patent or cited during the prosecution or within the file history of the '339 Patent.

b. Prior Art Publications

NXP identifies the following prior art non-patent publications that anticipate and/or render obvious the Asserted Claims of the '339 Patent. NXP also identifies all of the patents and patent applications identified in the prior section and all documents cited in the charts describing prior art systems as prior art publications that anticipate and/or render obvious the Asserted Claims of the '339 Patent.

Title	Author/Publisher	Date of Publication	Production Number
Configurable On-Line Global Energy Optimization in Multi-Core Embedded ("Toprak")	Zeynep Toprak Deniz, Yusuf Leblebici, Eric Vittoz Ecole Polytechnique Fédérale de Lausanne Lausanne,	2006	DEFS-RED-PA000002953
How to Approach Inter-Core Communication on TMS320C6474 ("Mathes")	Juergen Mathes	January 2009	DEFS-RED-PA000002959
Multiple clock and Voltage Domains for Chip Multi Processors ("Rotem")	Efraim Rotem Avi Mendelson Ran Ginosar Uri Weiser	December 2009	DEFS-RED-PA000002973
"Whitepaper NVIDIA Tegra Multi-processor Architecture," ("NVIDIA Whitepaper")	NVIDIA	February 2010	DEFS-RED-PA000002983
ARM1176JZF – Technical Reference Manual (Revision: r0p0) ("ARM Processor Ref. Man. r0p0")	ARM	August 31, 2007	DEFS-RED-PA000002995
ARM1176JZF-S – Technical Reference Manual (Revision: r0p7) ("ARM Processor Ref. Man. r0p7")	ARM	November 27, 2009	DEFS-RED-PA000003287
CoreTile Express™ A9x4 Cortex™-A9 MPCore (V2P-CA9) Technical Reference Manual	ARM	November 27, 2009	DEFS-RED-PA000004046

Title	Author/Publisher	Date of Publication	Production Number
(“ARM Processor Ref. Man. Cortex”)			
Low Latency Clock Domain Transfer for Simultaneously Mesochronous, Plesiochronous and Heterochronous Interfaces (“Williams”)	Wade L. Williams, Philip E. Madrid, Scott C. Johnson	May 3, 2007	DEFS-RED-PA000004140
System Level Analysis of Fast, Per-Core DVFS using On-Chip Switching Regulators, 14 th International Symposium on High Performance Computer Architecture (“Kim Paper”)	Wonyoung Kim, Meeta S. Gupta, Gu-Yeon Wei, David Brooks	February 2008	DEFS-RED-PA000004279
Computer Architecture Techniques for Power-Efficiency (“Kaxiras”)	Stefanos Kaxiras, Margaret Martonosi	2008	DEFS-RED-PA000004291
P. Senstrom, A Survey of Cache Coherence Schemes for Multiprocessors, Computer, Volume 23, Issue 6 (“Stenstrom”)	Per Stenstrom	June 1990	DEFS-RED-PA000004632

c. Prior Art Systems

NXP identifies the following prior art systems and their underlying technologies that anticipate and/or render obvious the Asserted Claims of the '339 Patent. A chart mapping

known features of these prior art systems to the Asserted Claims of the '339 Patent is included in Exhibits A. Each of the prior art documents listed in the corresponding chart can separately be considered invalidating prior art publications that anticipates and/or renders obvious the Asserted Claims of the '339 Patent.

System	Offer/Use Date	Manufacturer
Microprocessors (“Processor”)	Sold, offered for sale, used, or publicly disclosed at least as early as August 2009 ²	
ARM1176JZF Microprocessors (“ARM ARM1176JZF Processor”)	Sold, offered for sale, used, or publicly disclosed at least as early as August 2007 ³	ARM
“NVIDIA Tegra 2 System”	Sold, offered for sale, used, or publicly disclosed at least as early as February 2010 ⁴	NVIDIA

NXP reserves the right to rely on additional materials describing the identified systems and/or corroborating that they were known, used, or sold and/or the materials describing them were publicly available prior to the priority date of the Asserted Claims, including materials that may be produced in response to several third-party subpoenas and any systems described in the publications listed above. NXP will serve subpoenas on companies believed to have information regarding these and related products and reserves the right to supplement these contentions based on the information so obtained. Additionally, Plaintiff may have materials regarding certain prior art systems in its possession from current or previous litigations.

² [REDACTED]

³ <https://www.anandtech.com/show/2782>

⁴ https://www.nvidia.com/docs/io/90715/tegra_multiprocessor_architecture_white_paper.pdf
(DEFS-RED-PA000002983)

B. Charts Showing Bases for Anticipation and/or Obviousness

The accompanying claim charts (Exhibits A) set forth bases for anticipation and obviousness, including identifying where exemplary prior art references disclose, alone or in combination with other references, each element of each Asserted Claim on a limitation-by-limitation basis. NXP's claim charts are exemplary and are not intended to be exhaustive.

Each prior art reference identified in Exhibits A anticipates or renders obvious one or more of the claims of the Asserted Patent, either alone or in combination with other prior art references as set forth herein or the knowledge of those of ordinary skill in the art at the time of the alleged invention, including at least the knowledge reflected in the references identified in Exhibits A as set forth herein. Each of the prior art references included in Exhibits A can be combined with one or more other prior art references in Exhibits A to render obvious one or more claims of the Asserted Patent as set forth herein.

1. The '339 Patent

In the table below, NXP identifies a non-exhaustive list of prior art references that, alone, or in combination, anticipate or render obvious the Asserted Claims of the '339 Patent.

References	Claims	Grounds	Exhibit
US20090158078A1 ("Knoth")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-1
US20050034002A1 ("Flautner")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-2
US20110119672A1 ("Ramaraju")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-3
US20070156370A1 ("White")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-4
US20100115304A1 ("Finkelstein")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-5
US20080276026A1 ("Branover")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-6
US20100122101A1 ("Naffziger")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-7

CONFIDENTIAL BUSINESS INFORMATION, SUBJECT TO PROTECTIVE ORDER

References	Claims	Grounds	Exhibit
US20080104425A1 ("Gunther")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-8
US20070096775A1 ("Elgebaly")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-9
US20080256381A1 ("Jacobowitz")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-10
US20080162770A1 ("Titiano")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-11
US20080046770A1 ("Jong")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-12
US20100073068A1 ("Cho")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-13
US20110022356A1 ("Nussbaum")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-14
US20120060170A1 ("Vajda")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-15
US20060190755A1 ("Kim")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-16
US8122270 ("Allarey")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-17
US20070080696A1 ("Kumar")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-18
US20060282692 ("Oh")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-19
US7447873 ("Nordquist")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-20
US7249268 ("Bhandarker")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-21
US20090271646A1 ("Talwar")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-22
US20110093733A1 ("Kruglick")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-23
US20090138737A1 ("Kim II")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-24
Microprocessor ("Processor")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	[CBI] A-25
ARM Microprocessor ("ARM ARM1176JZF Processor")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-26
NVIDIA Microprocessor ("NVIDIA Tegra 2 System")	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-27

References	Claims	Grounds	Exhibit
Omnibus Chart	1, 5, 8, 9, 10, 14, and 21	35 U.S.C. §§ 102, 103	A-28

The accompanying claim charts (Exhibits A) set forth the example bases for anticipation and obviousness, identifying where each reference discloses, alone or in combination with other references, each element of each Asserted Claim on a limitation-by-limitation basis. NXP's claim charts are exemplary and are not intended to be exhaustive.

In addition to the foregoing prior art and grounds of anticipation and obviousness, all of the prior art cited and all grounds disclosed during the prosecution of the Asserted Patent, its family members, or foreign counterparts, either during initial prosecution or during subsequent post grant proceedings, and all arguments made by Patentee during such proceedings, are incorporated by reference herein. Plaintiff is and has been involved in other proceedings involving the Asserted Patent. Any statements made by Plaintiff are fairly within the scope of NXP's Invalidity Contentions and are incorporated by reference herein.

NXP may rely on all past, present, co-pending, and future litigation involving the Asserted Patent (collectively, the "Other Litigations"), and any statements made or to be made by Plaintiff or other Defendants in the Other Litigations. For the avoidance of doubt, and without limitation, NXP incorporates by reference all relevant statements, contentions (including invalidity contentions) made or to be made by Plaintiff or other Defendants (including analysis and explanations regarding obviousness, combinations, motivations to combine, etc.) in the Other Litigations, which include but are not limited to the following:

Title	#
<i>Redstone Logics LLC v. Samsung Electronics Co., Ltd. et al</i>	2-23-CV-00485 (EDTX)
<i>Redstone Logics LLC v. MediaTek Inc. et al</i>	7-24-CV-00029 (WDTX)
<i>Redstone Logics LLC v. Qualcomm Inc. et al</i>	7-24-CV-02311

February 14, 2025

Respectfully submitted,

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